NOTES:
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

VELLFIRE

2020.06.05

DATE	CHANGE NO.	REV
21-OCT-2002		

DESIGN / DRAWER	XXX	DATE	21-OCT-2002
CHECK			
APPROVAL			
FILE NAME			
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION MAIN BOARD		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 1 of 139			

TABLE OF CONTENTS

SMALL BOARD1&2

SMALL BOARD3

FOR 17 SMALL BOARD1&2

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
TABLE OF THE CONTENT

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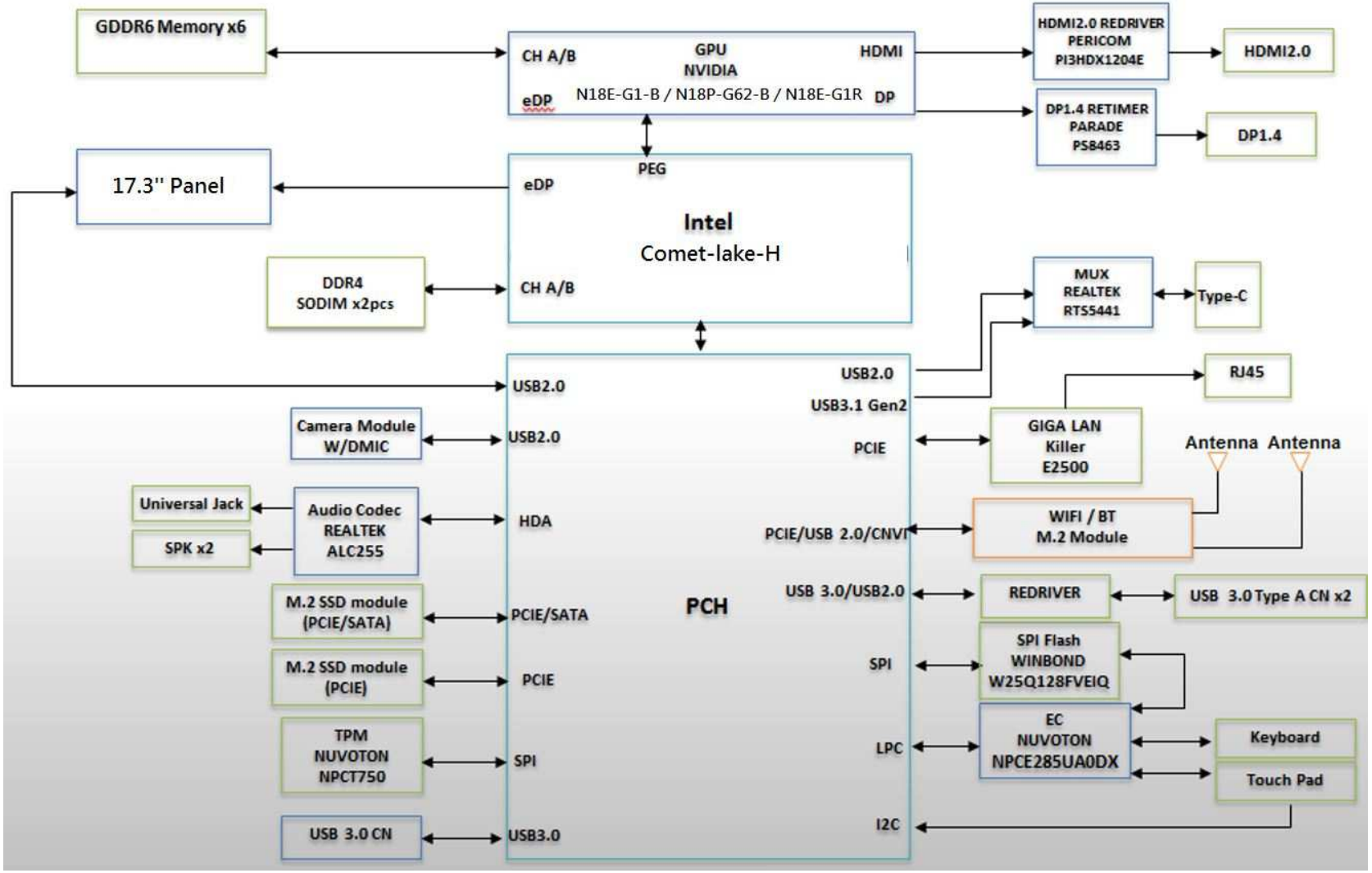
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 2 of 139			



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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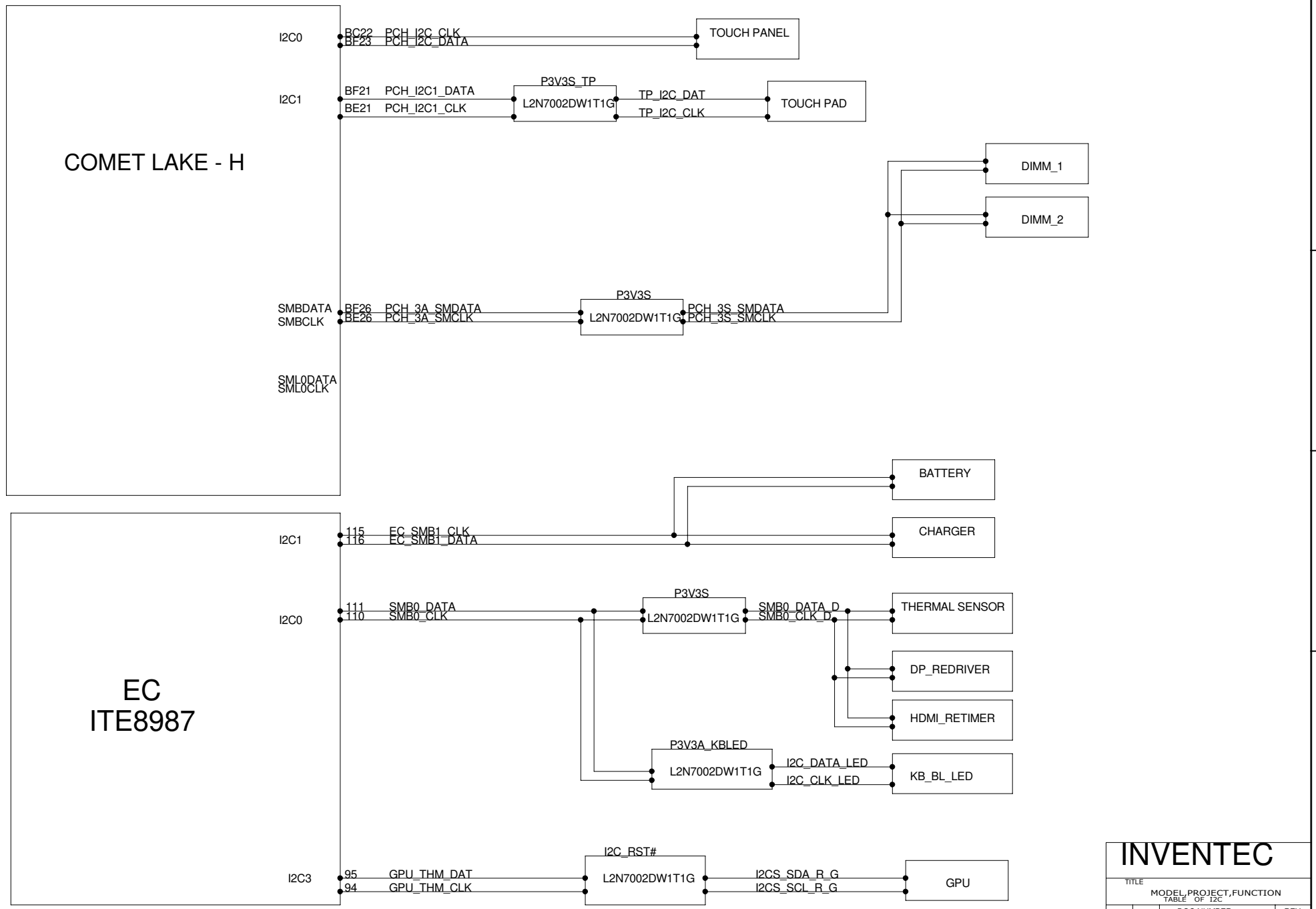

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
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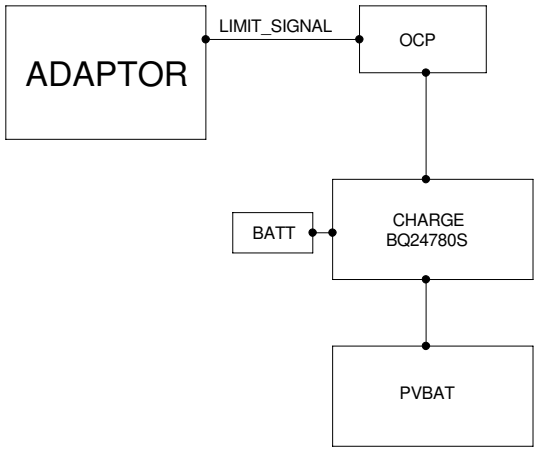
POWER BLOCK



IN/EN		OUT
PVBAT, EN_5V	SY8288CRAC	P5V0DS
PVBAT, EN_5V0	SY8284CRAC	P5V0
PVBAT, EN_3V	NB680AGD	P3V3DS
PVBAT, EN_VDDQ, EN_VTT	NB685AGQ	P1V2, P0V6S
PVBAT, EN_1V05V	SY8288CRAC	P1V05A
PVBAT, EN_VCCIO	NB681GD	PVCCIO
PVBAT, EN_PVCORE	NCP81215MNTXG	PVCORE
PVBAT, VRACPU_DRVON	NCP81151MNTBG	PVCCGT
PVBAT, VRACPU_DRVON	NCP81253MNTBG	PVCCSA

IN/EN		OUT
P5V0DS, EN_2V5	RT8097ALGE	P2V5
P3V3DS, EN_1V8	SY8088AAC	P1V8A
P3V3DS, P3V3A_5A_PWEN, CORE_PWEN	APL3523A	P3V3A, P3V3S
P5V0DS, CORE_PWEN, P1V8A, CORE_PWEN	APL3523A	P5V0S, P1V8S
P1V2, VCCPLL_OC_EN	PM514BA	VCCPLL_OC
P1V05A, RESUME_PWEN, CORE_PWEN	APL3523A	PVCCSTG, PVCCST

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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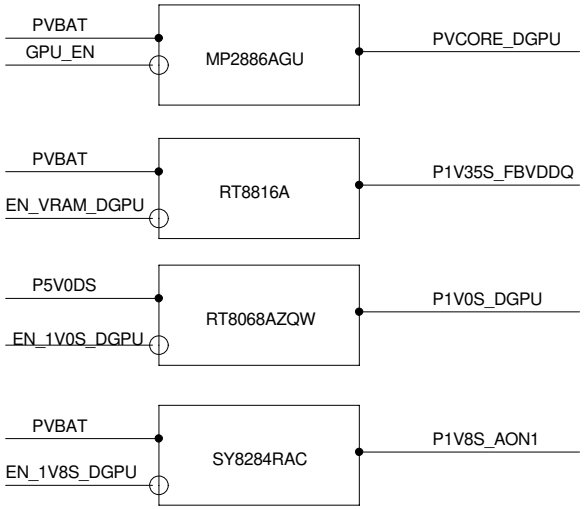
GPU POWER BLOCK

IN/EN OUT



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
TABLE OF I2C

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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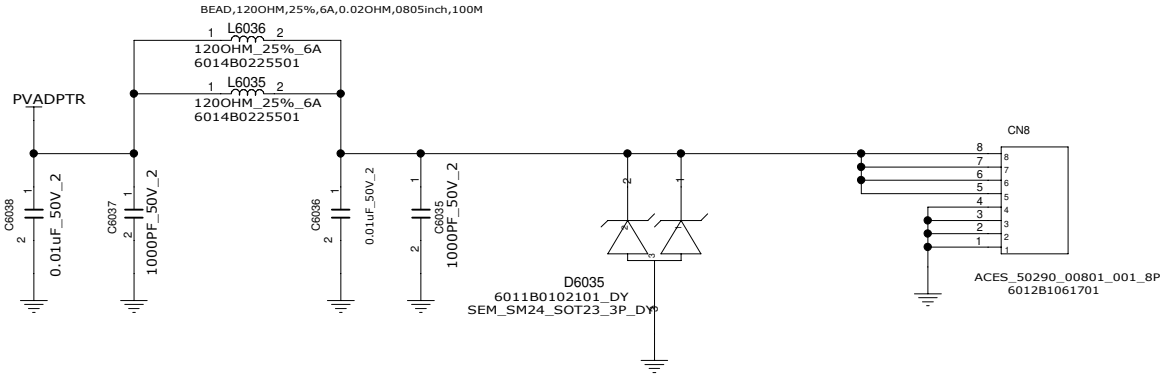

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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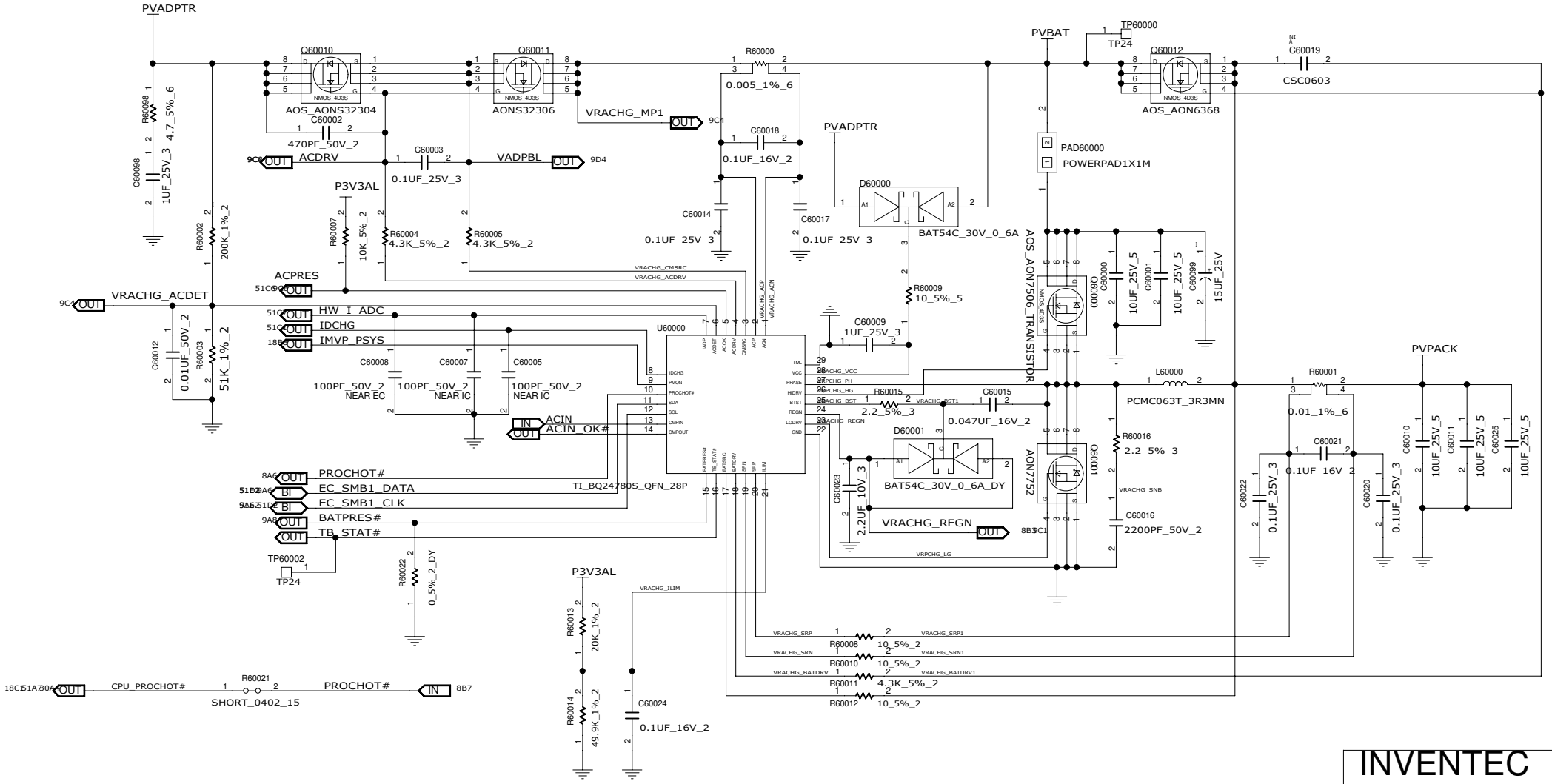

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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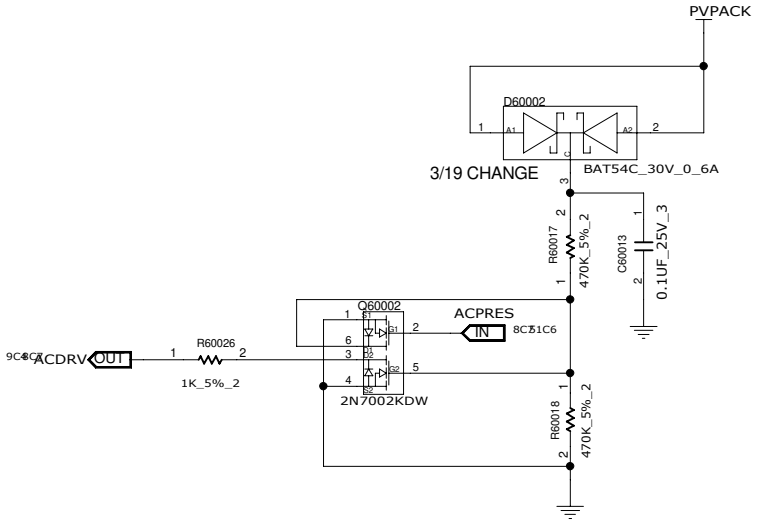
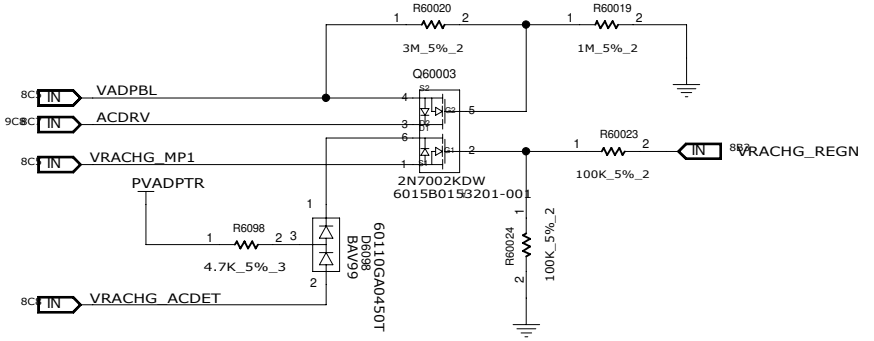
FOR CHARGER

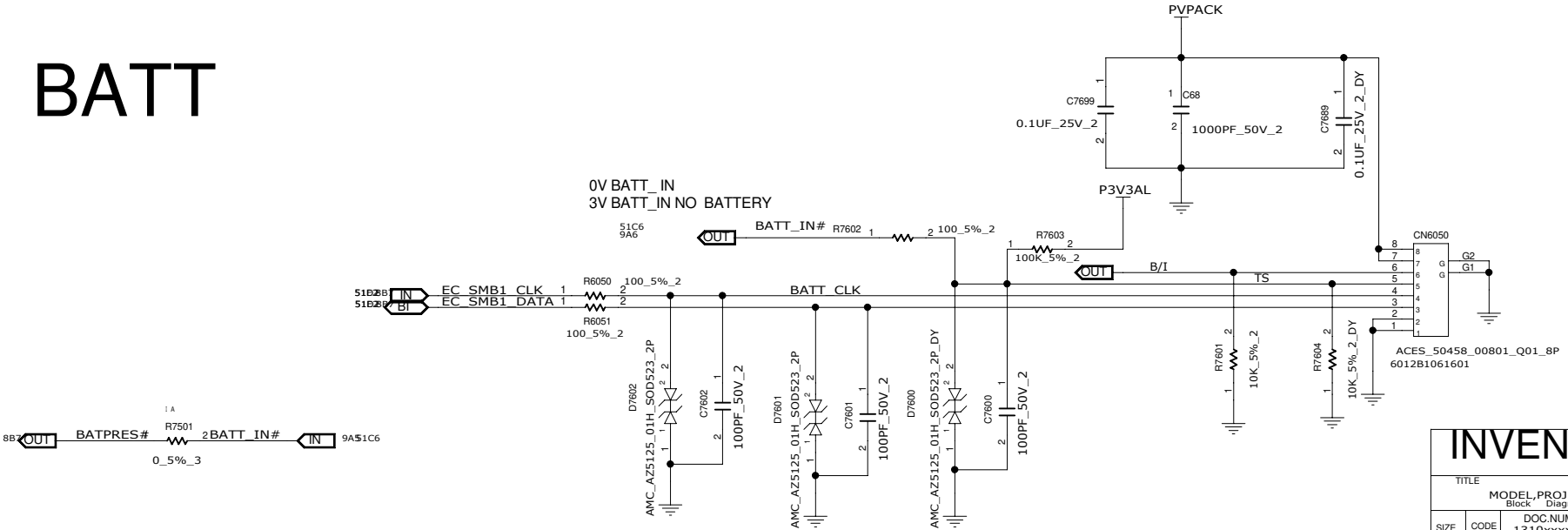
SCP



ARP



BATT



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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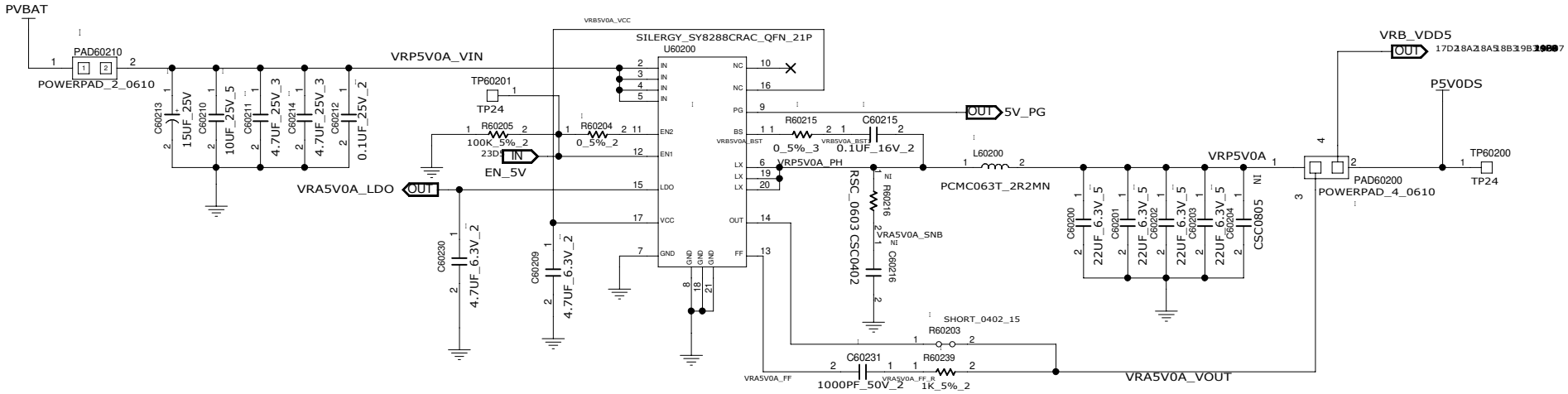

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
P5V0DS

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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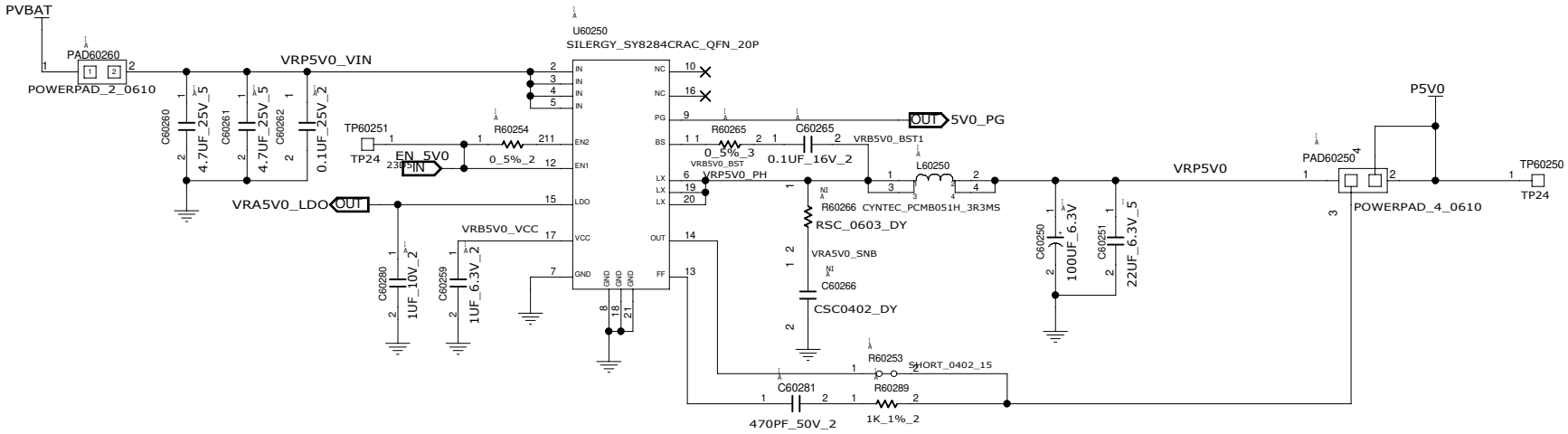
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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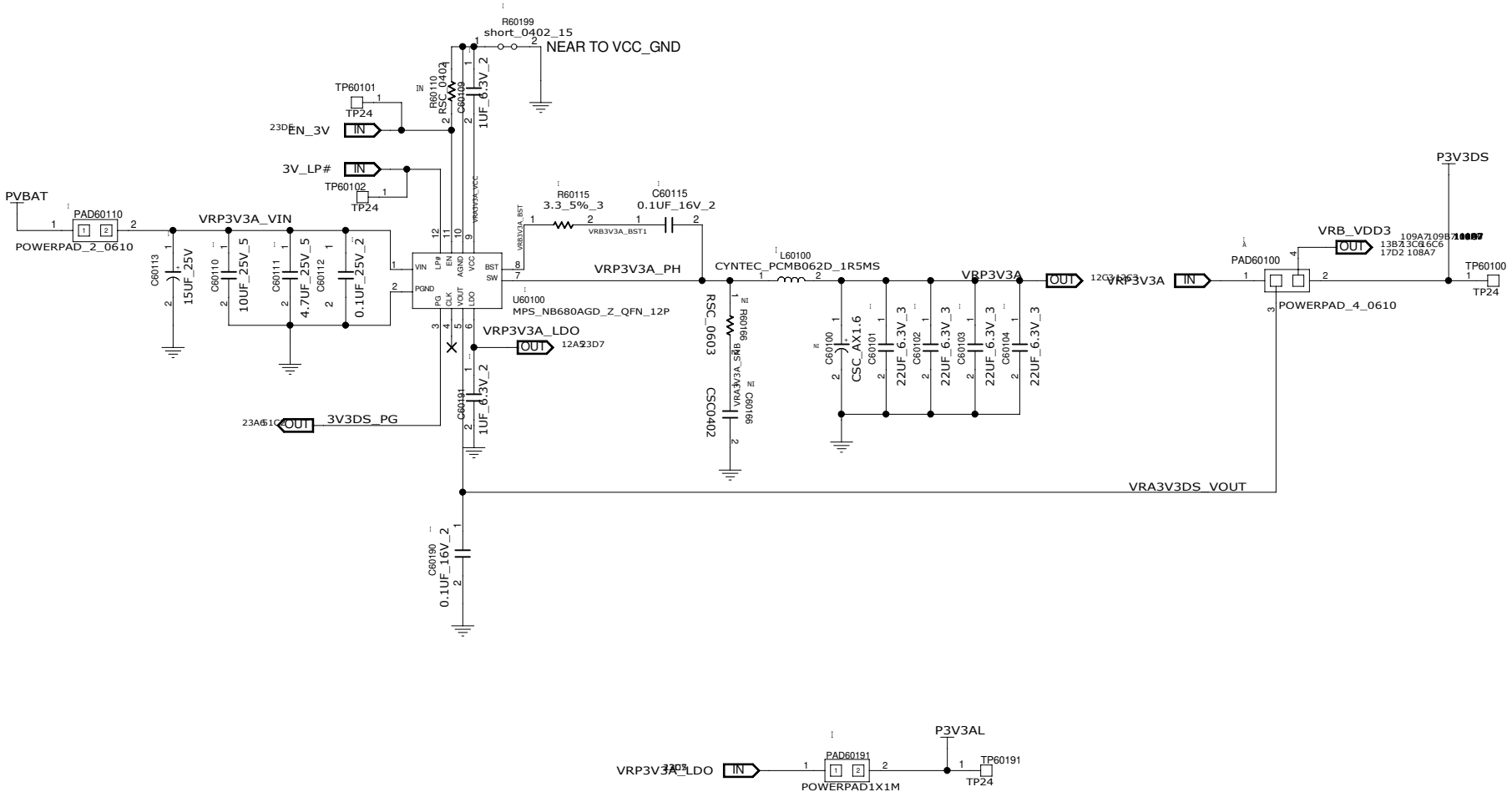

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P3V3DS_NB680A		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
SHEET 12 of 139			

CHANGE by	XXX	DATE	21-OCT-2002
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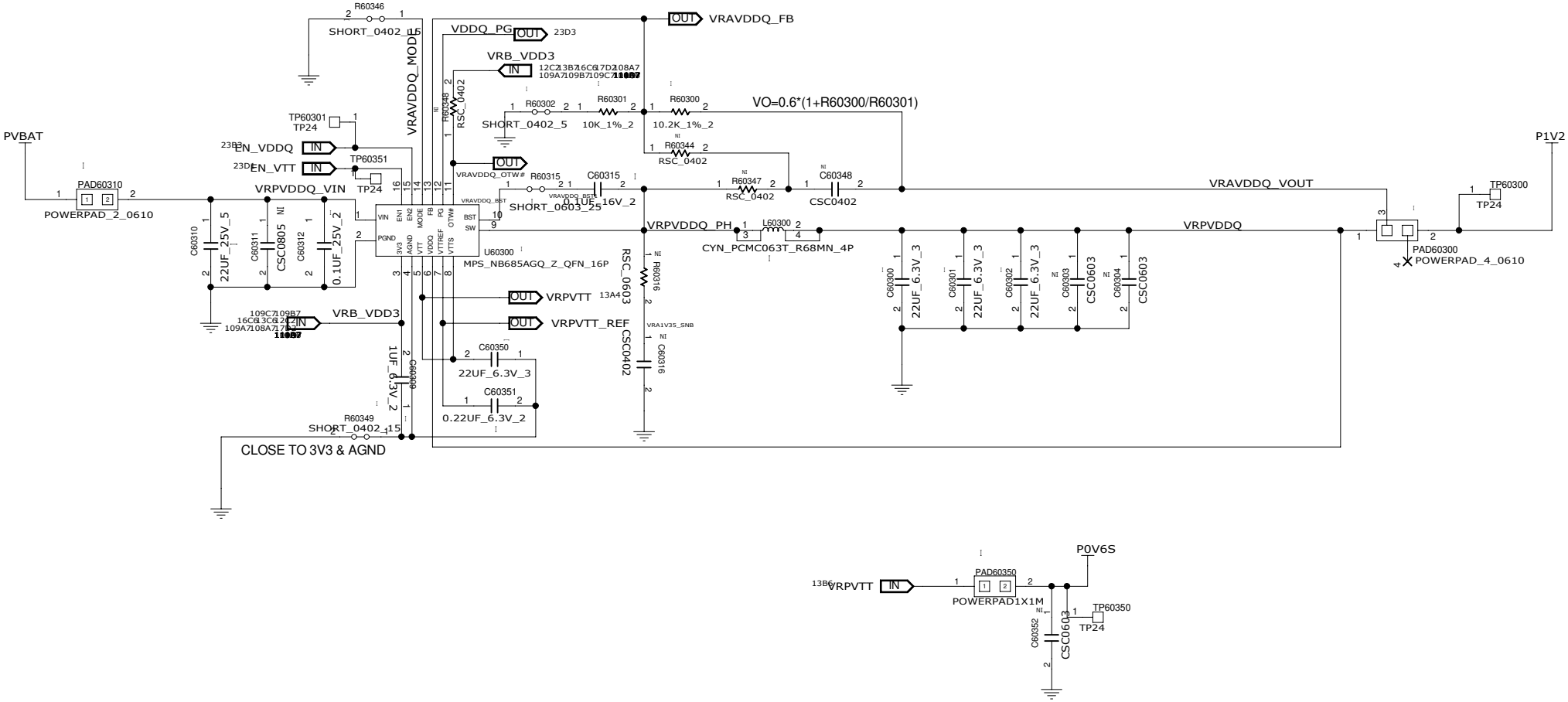
Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
VDDQ

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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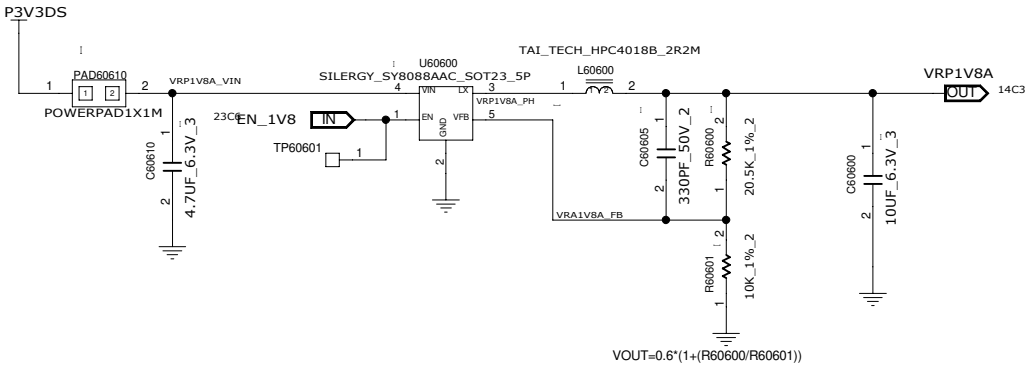

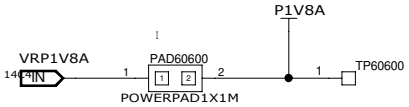

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION P1V8DS		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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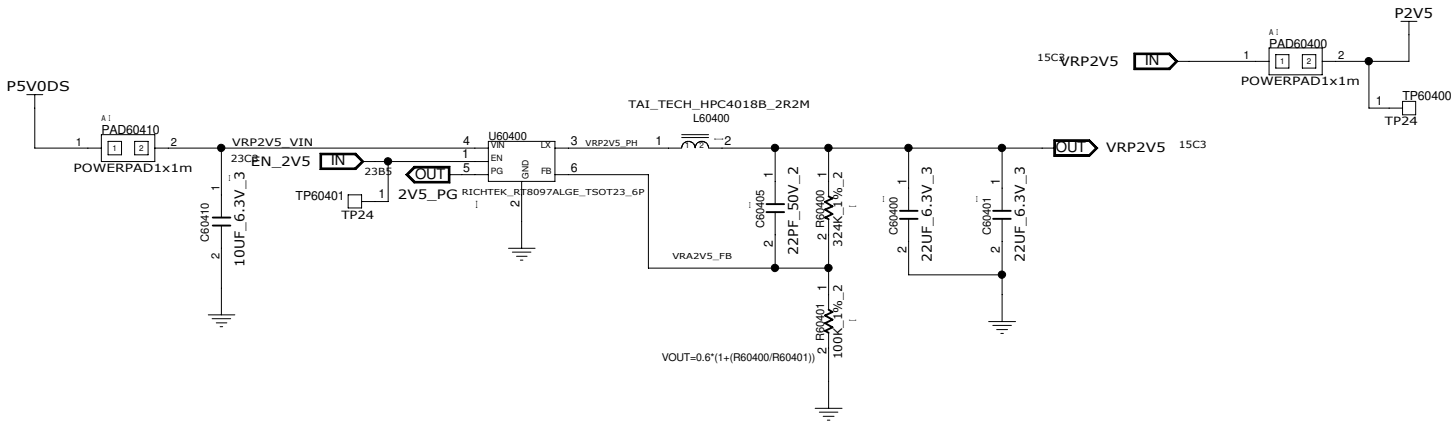
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
P2V5

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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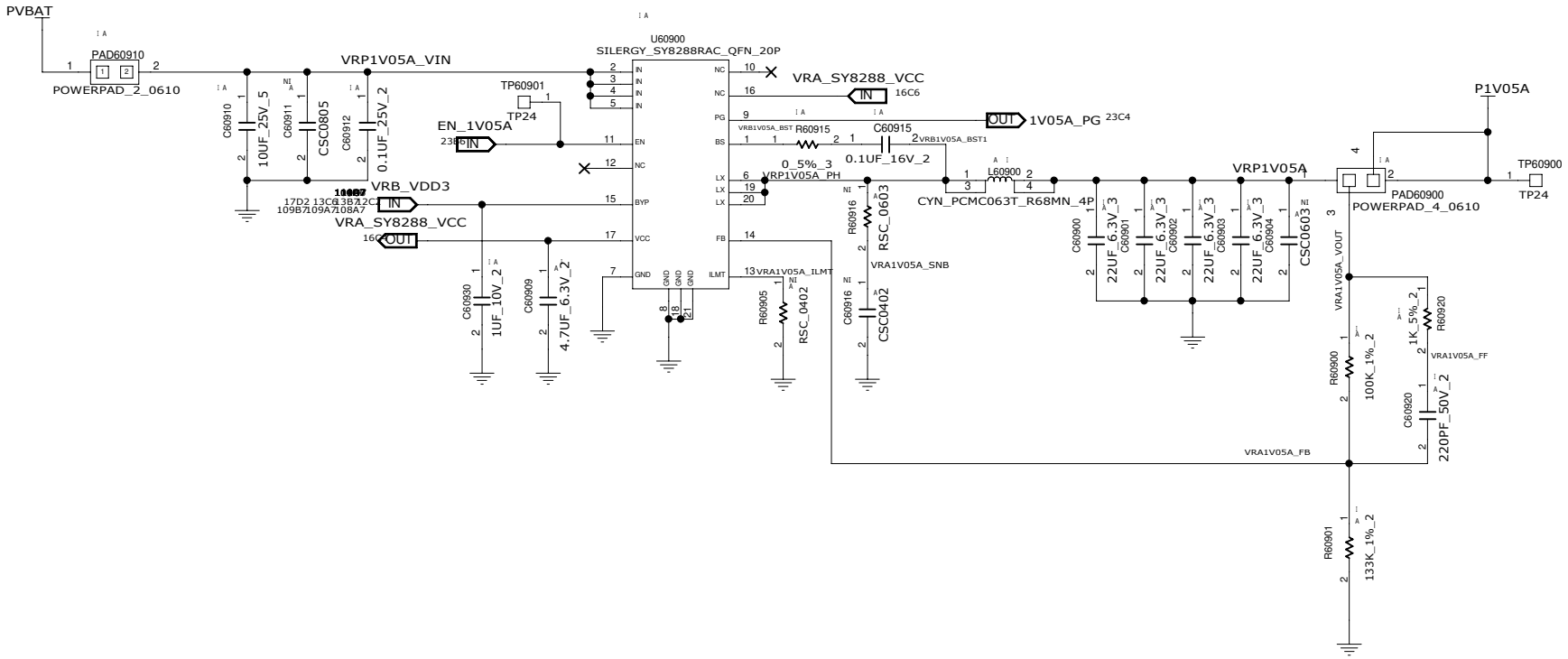

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
P1V0A

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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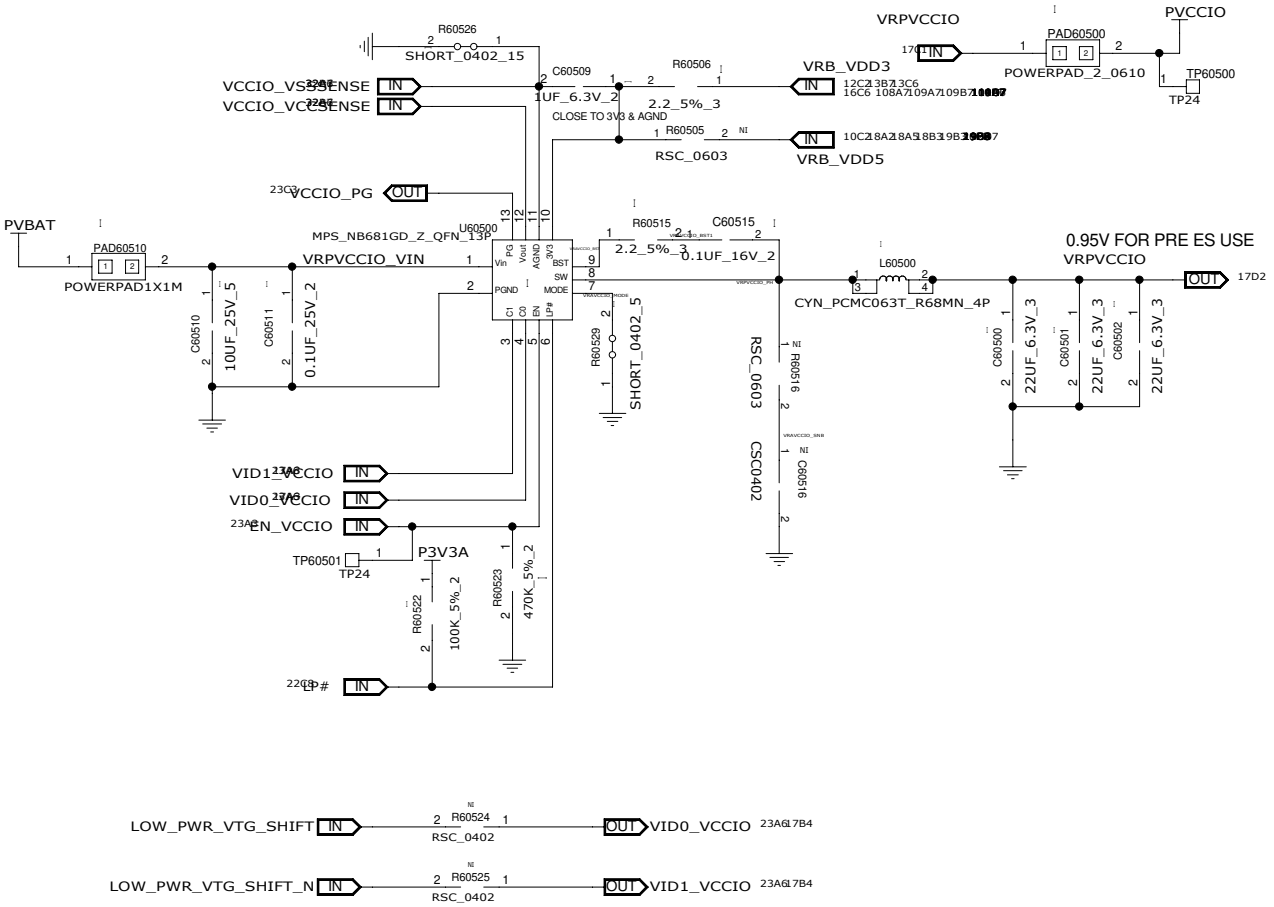
MODE	VR Rail	Resistor to GND (1% accuracy)
M1	VCCIO	0
M2	PRIMCORE	Float or > 230 K
M3	EDRAM/V1.0A/EOPIO	100 K
M4	Others	150 K

	LP#	C1	C0	VOUT(V)
VCCIO	0	X	X	0
	1	0	0	0.85
	1	0	1	0.875
	1	1	0	0.95
	1	1	1	0.975
VCCPRIM CORE	0	X	X	0.7
	1	0	0	0.85
	1	0	1	0.9
	1	1	0	0.95
	1	1	1	1.00
EDRAM/ EOPIO	0	X	X	0
	1	0	0	0.8(MSM)
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05
Others	0	X	X	0
	1	0	0	1.0
	1	0	1	1.075
	1	1	0	1.15
	1	1	1	1.2



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCCIO

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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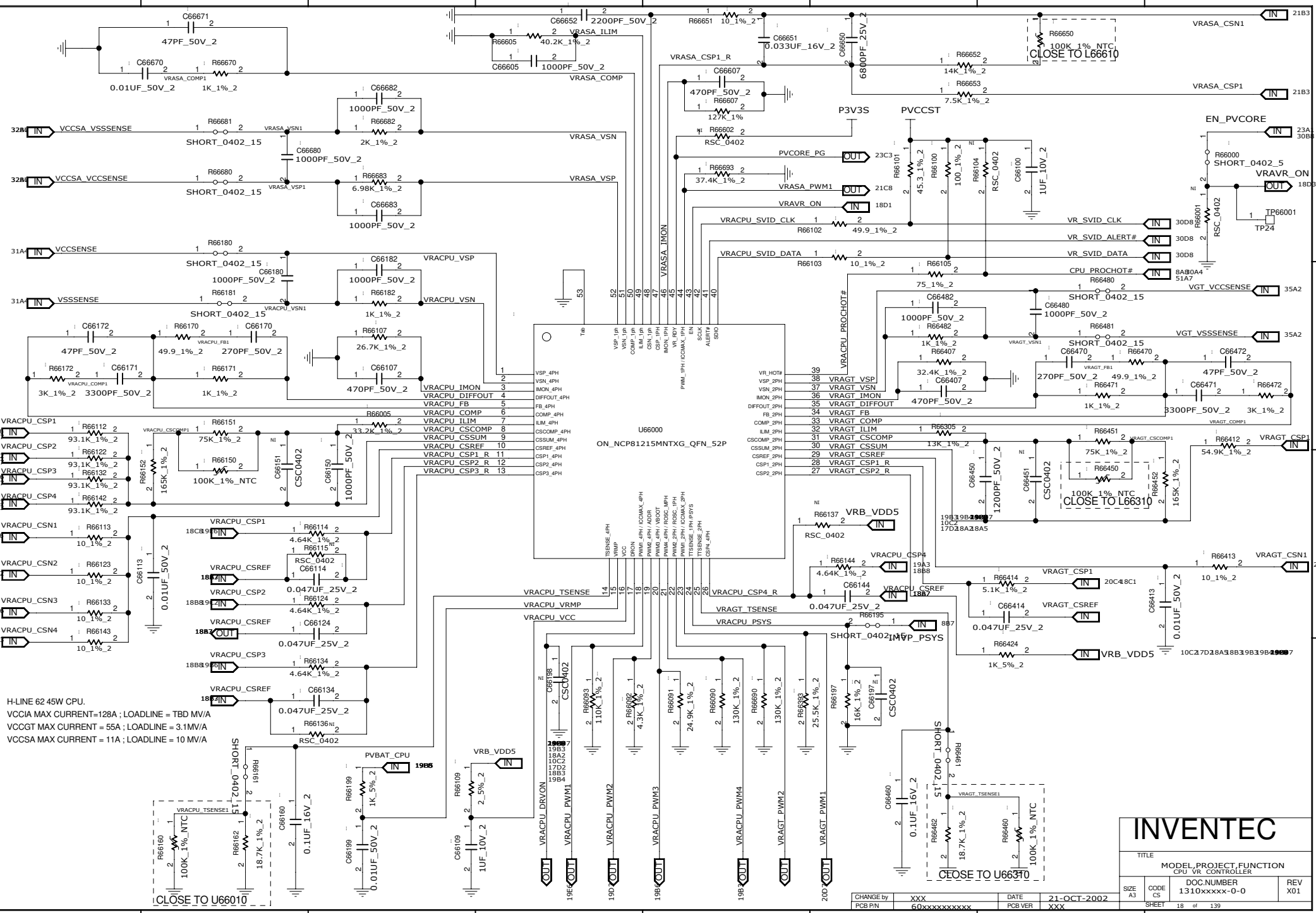
U66000
ON_NCP81215MNTXG_QFN_52P
H-LINE 62 45W CPU.
VCCIA MAX CURRENT=128A ; LOADLINE = TBD MV/A
VCCGT MAX CURRENT = 55A ; LOADLINE = 3.1MV/A
VCCSA MAX CURRENT = 11A ; LOADLINE = 10 MV/A
CLOSE TO L66610
CLOSE TO L66310
CLOSE TO U66310
CLOSE TO U66010
INVENTEC
MODEL,PROJECT,FUNCTION
CPU_VR_CONTROLLER
DOC.NUMBER
1310xxxxx-0-0
REV
X01
CHANGE by
XXX
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21-OCT-2002
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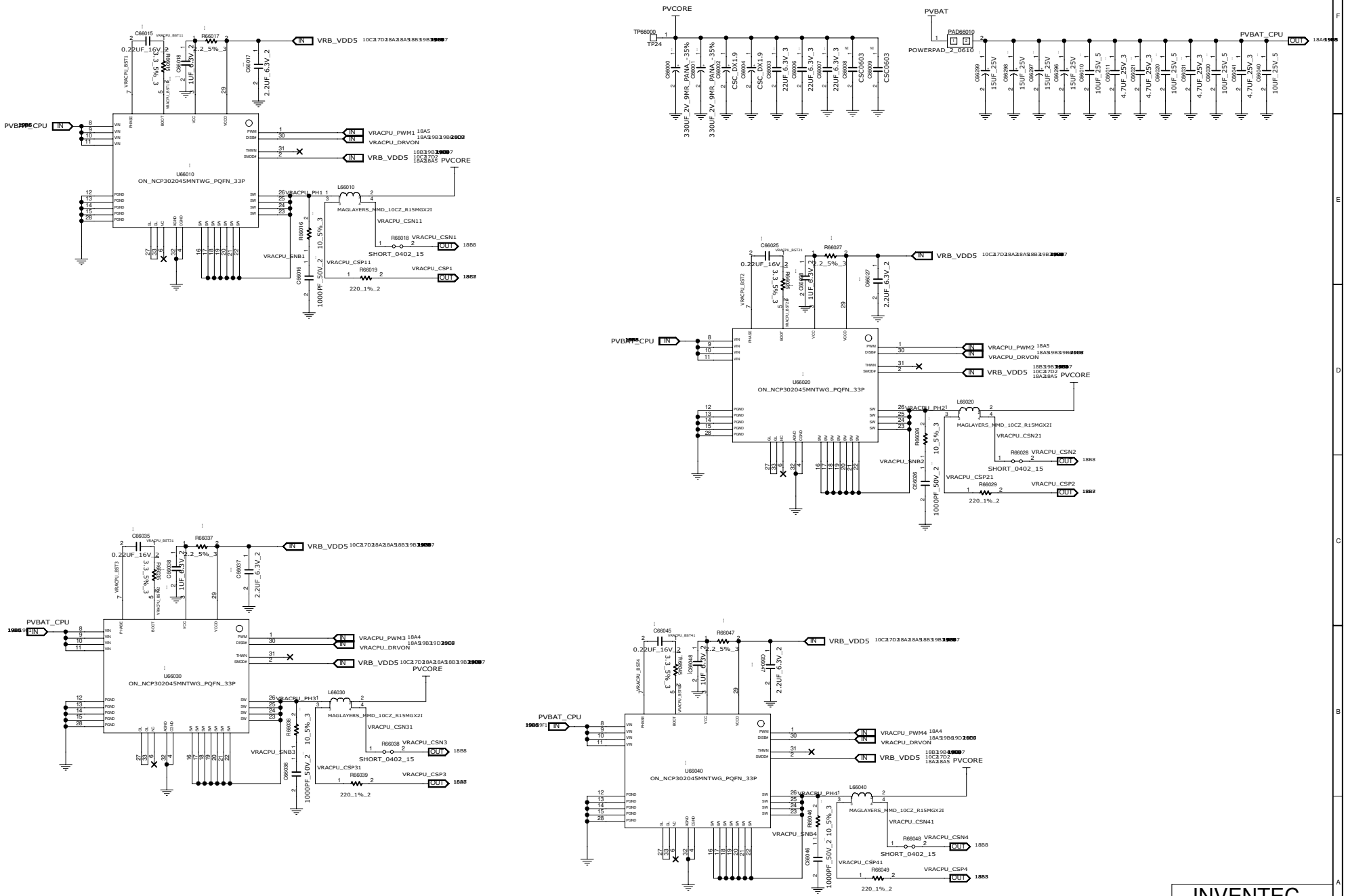

INVENTEC

MODEL,PROJECT,FUNCTION
PVCORE

CHANGE By	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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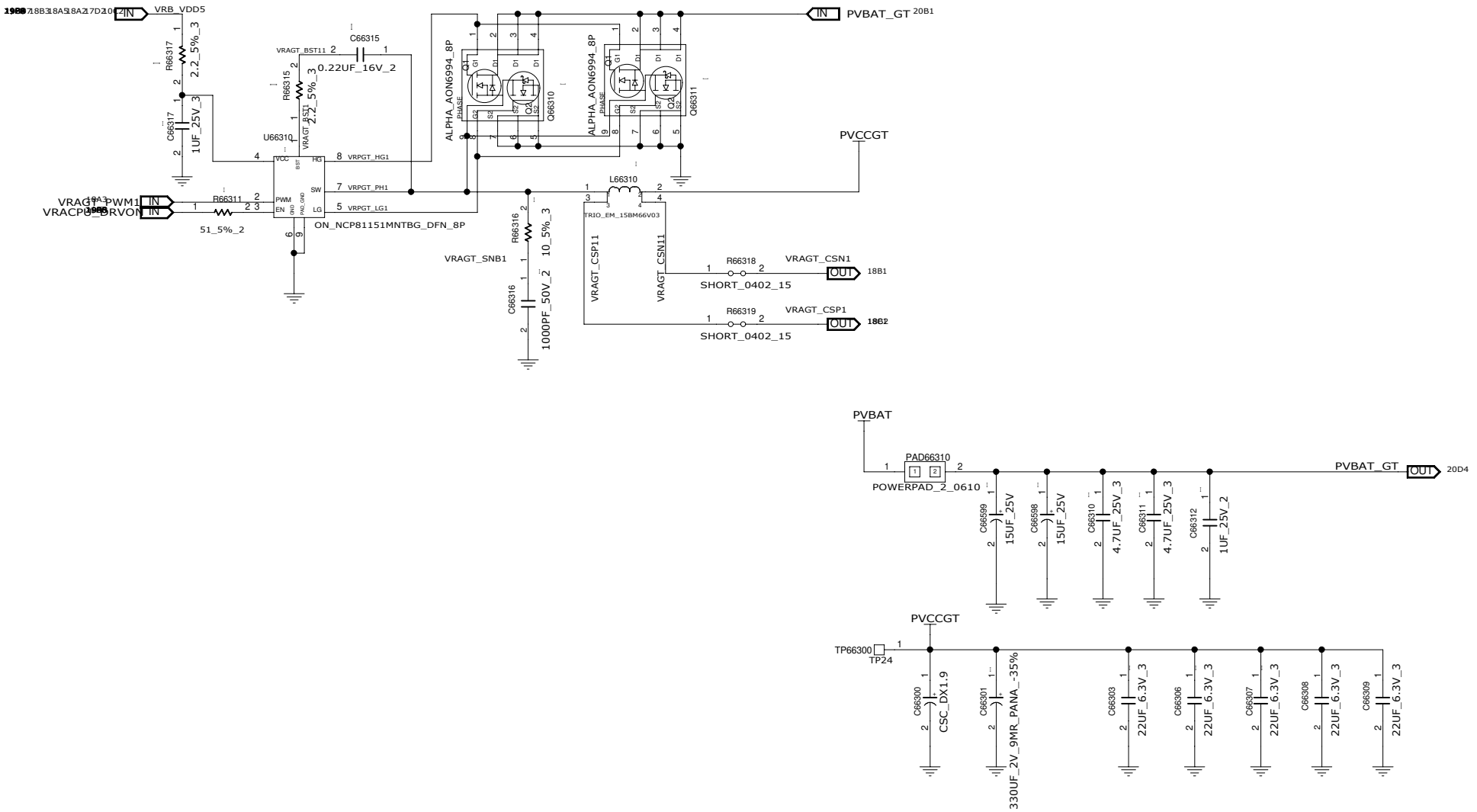

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PVCCGT

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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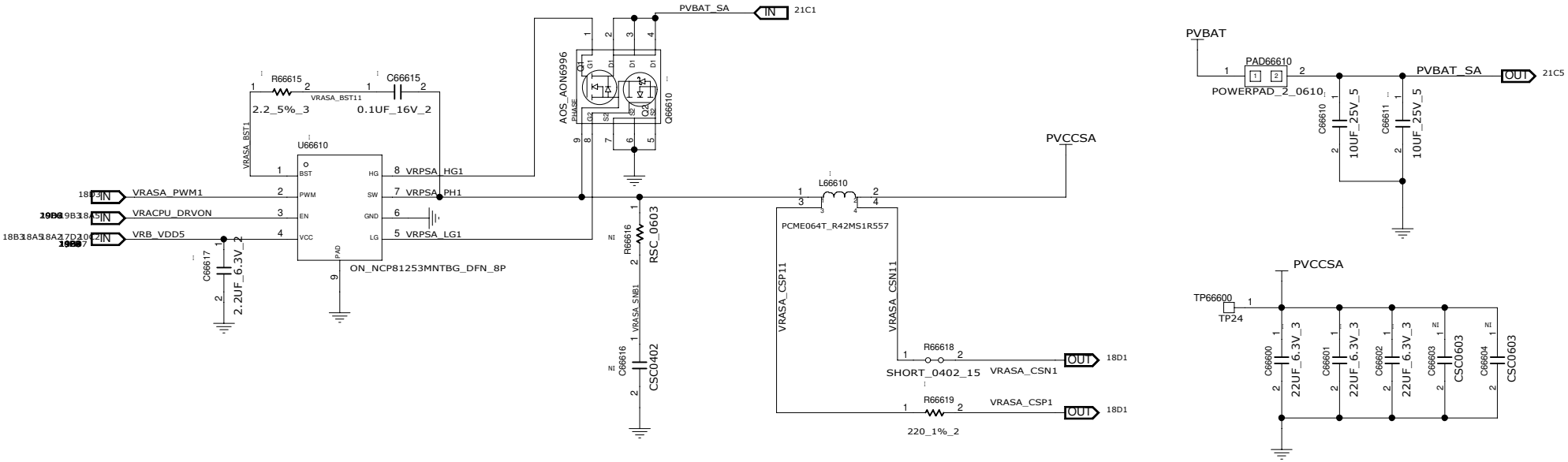

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
PVCCSA

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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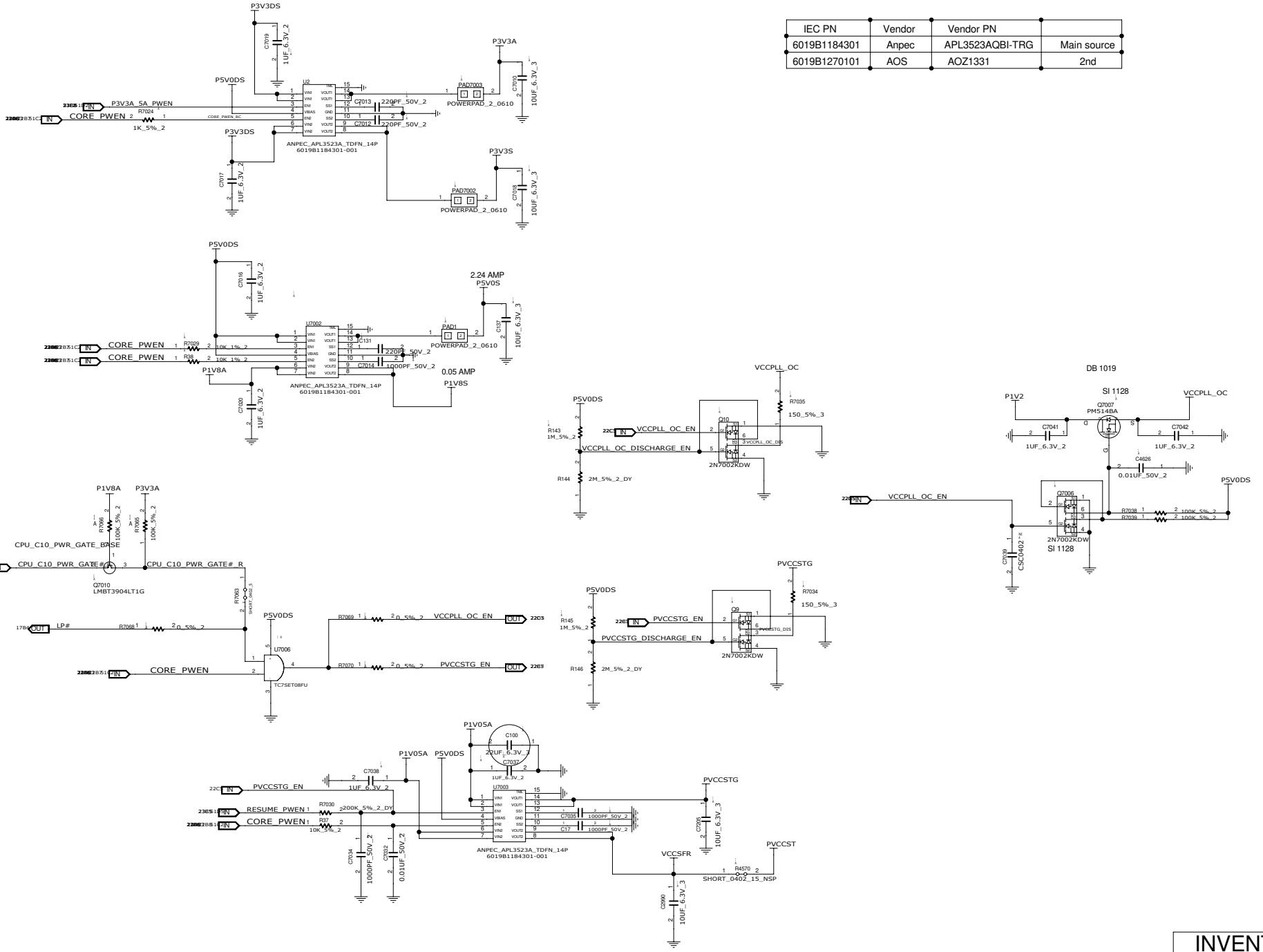

IEC PN	Vendor	Vendor PN	
6019B1184301	Anpec	APL3523AQBI-TRG	Main source
6019B1270101	AOS	AOZ1331	2nd

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
DDR3_SO-DIMM0

SIZE	CODE	DOC.NUMBER	REV
C	CS	1310xxxxx-0-0	X01

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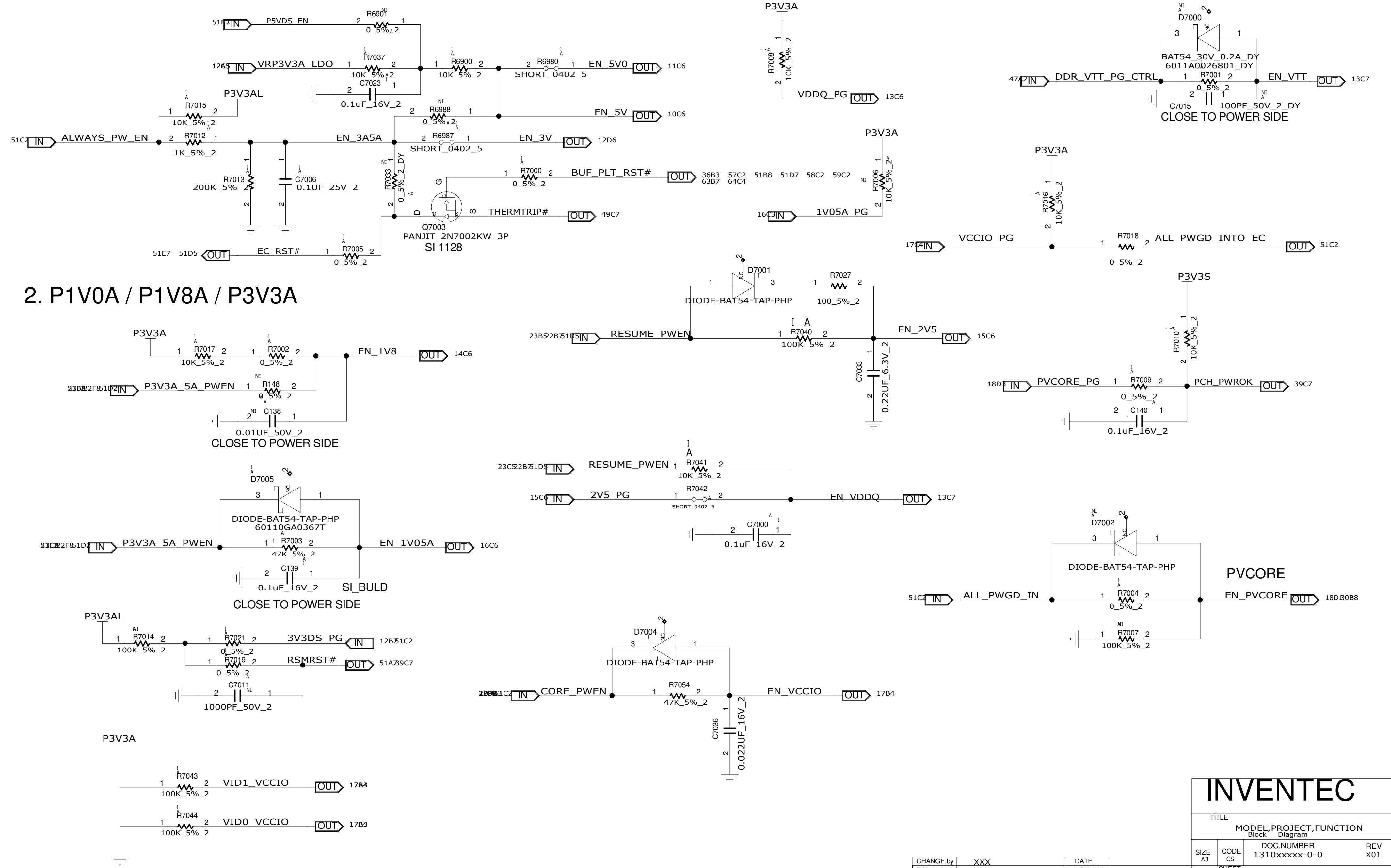
CHANGE by		DATE	
PCB P/N	60xxxxxxxxx	PCB VER 2.1	

1. P3V3DS / P5V0DS

2. P1V0A / P1V8A / P3V3A

3. P1V2 / P1V8 / VCCSFR(PVCCST)



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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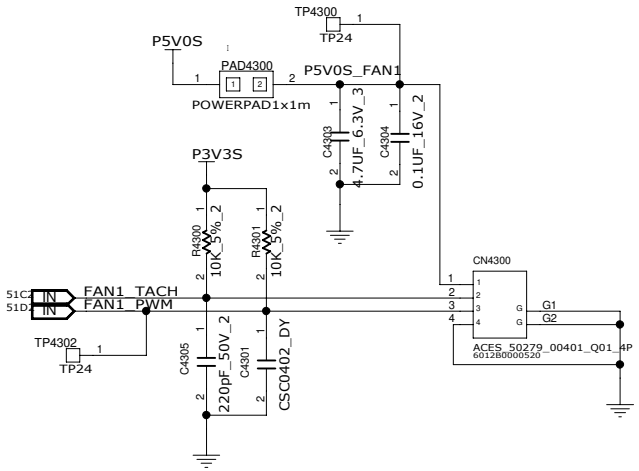
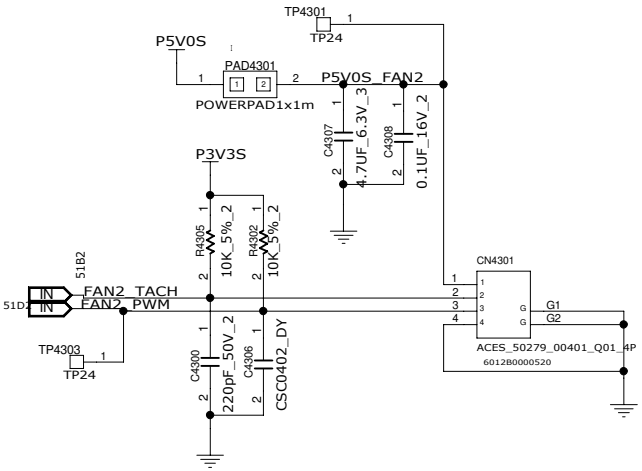
PCB P/N 6050xxxxxxxx	PCB VER XXX		

REFERENCE 4300~4349(FAN)
REFERENCE 4411~4449(THERMAL)



FAN1 CN CPU



FAN2 CN CPU

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
FAN & THERMAL

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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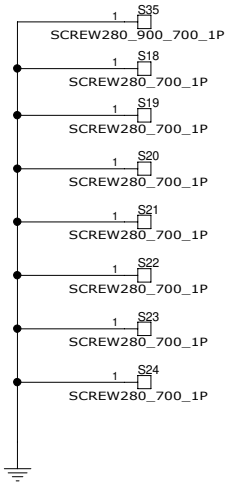
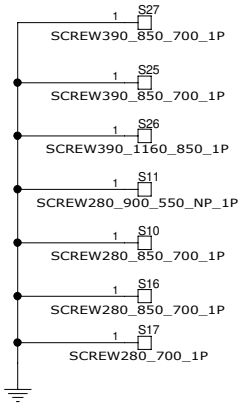
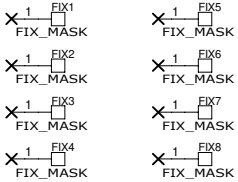
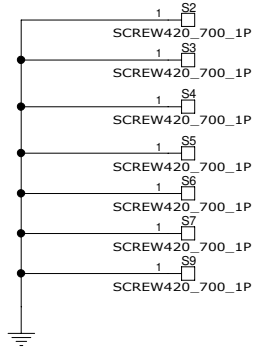
REFERENCE 0~49(PCB SCREW)







PCB



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
XDP & ME CONN.

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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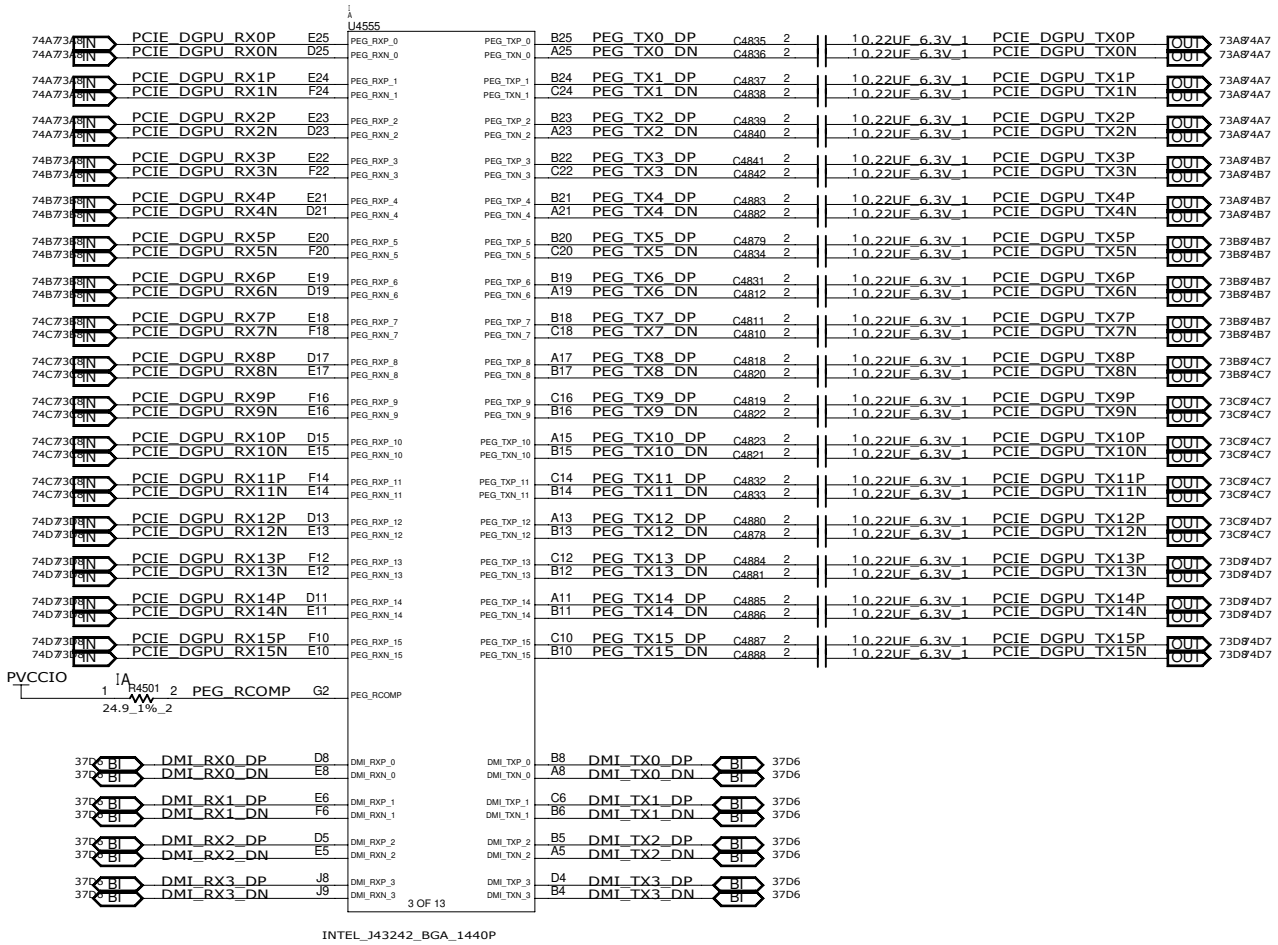

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE1_H-PEG,HDMI

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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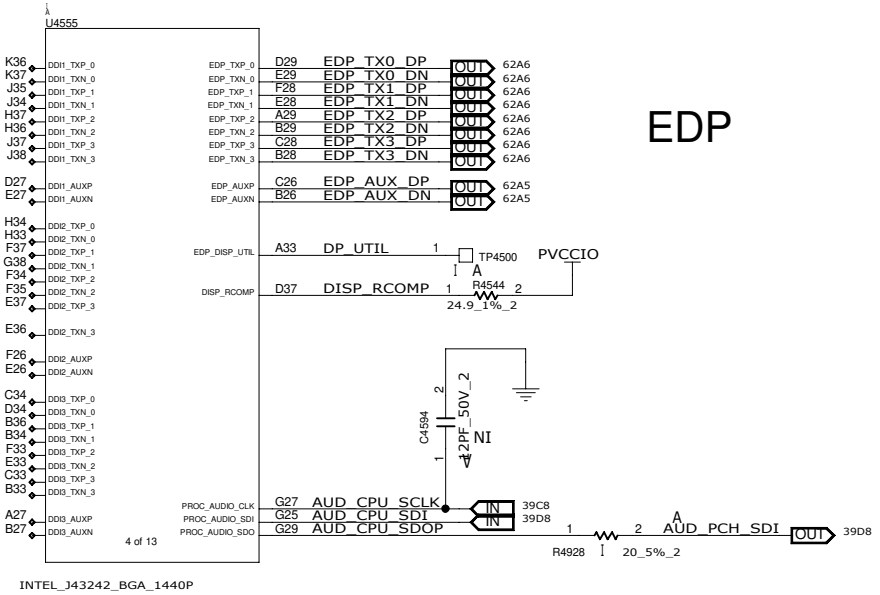
EDP



INTEL_J43242_BGA_1440P

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SKYLAKE2_H-DDI,EDP

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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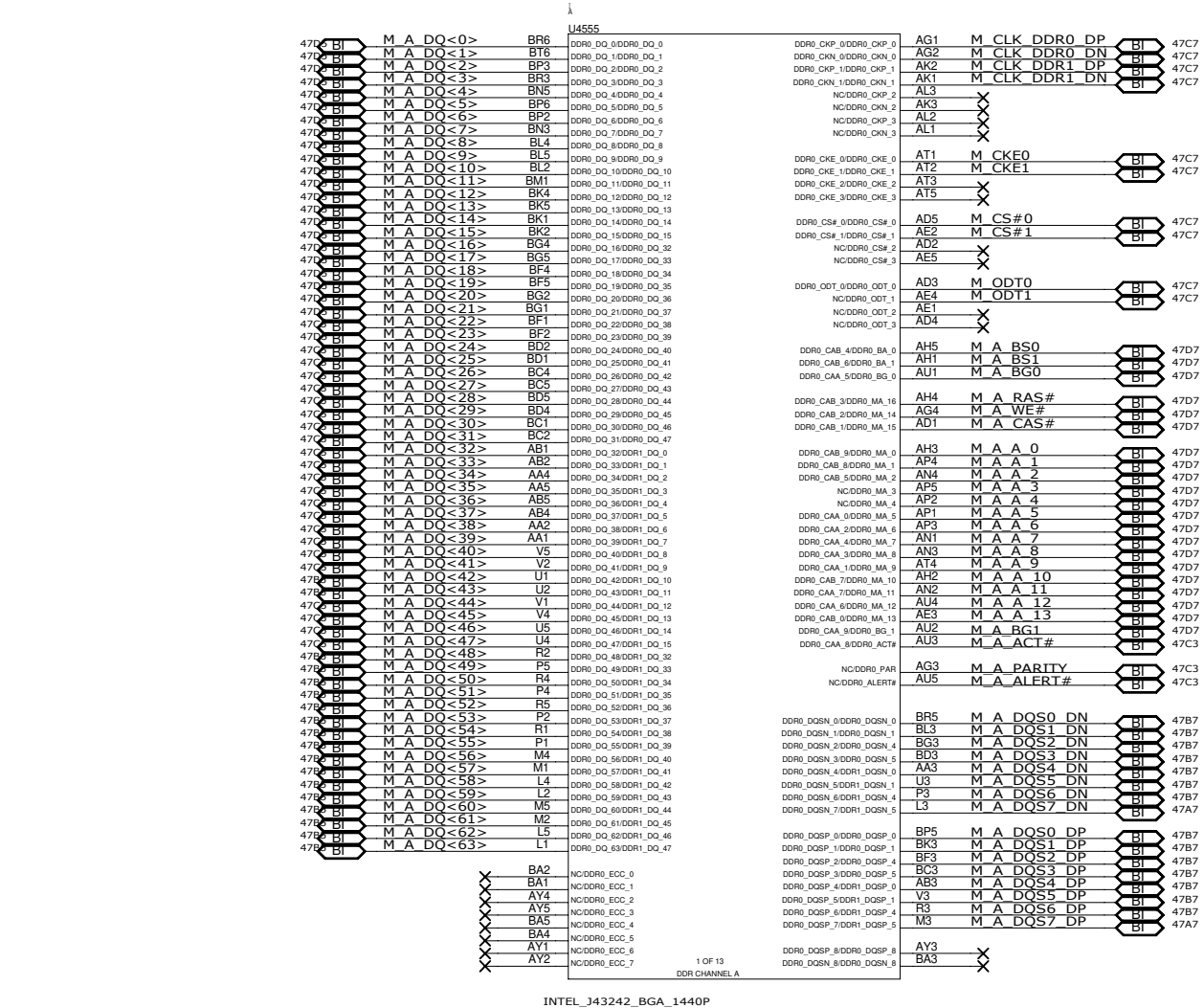

INTEL_J43242_BGA_1440P

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SKYLAKE_H-DDR-1

CHANGE by	XXX	DATE	21-OCT-2002
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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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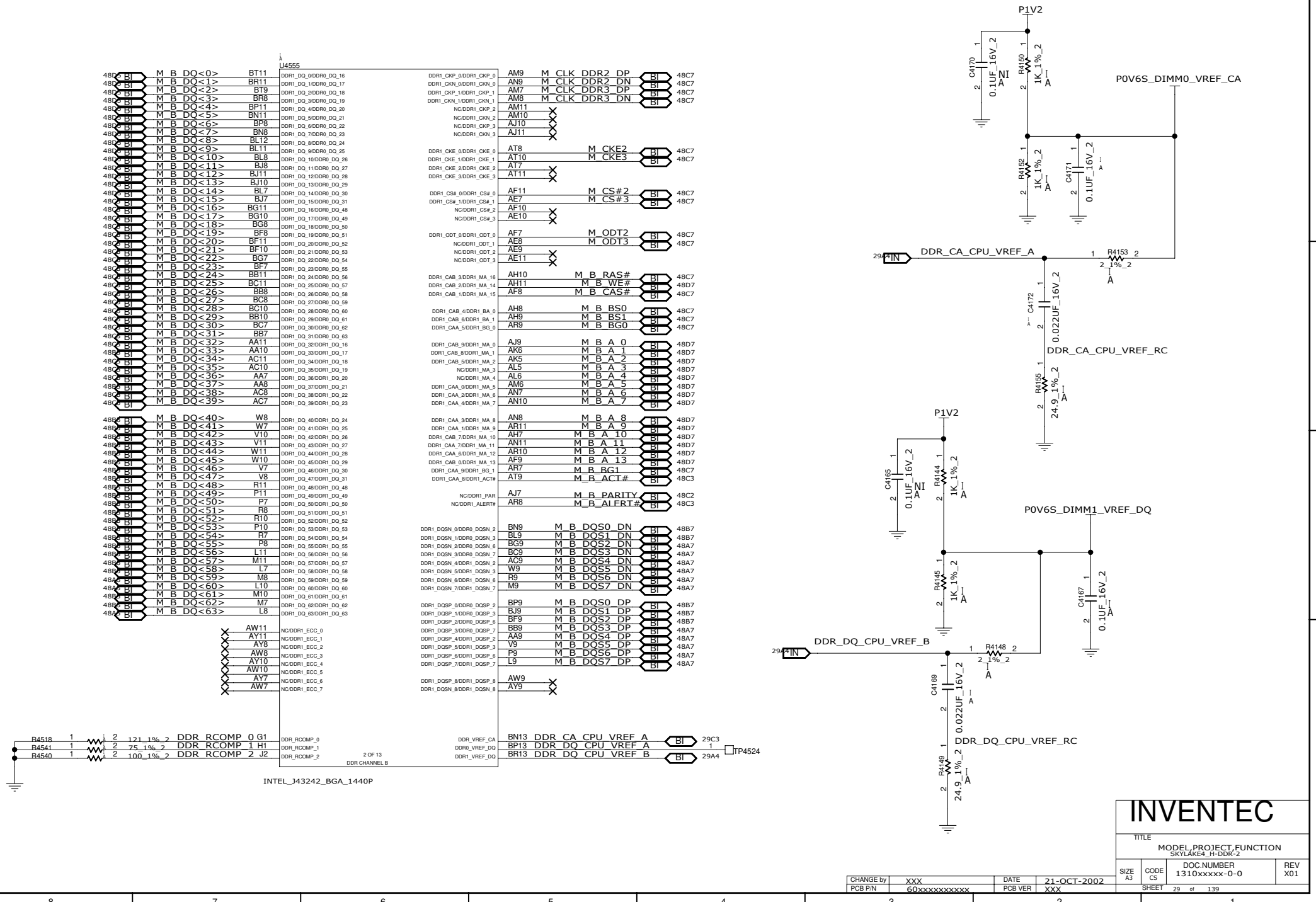
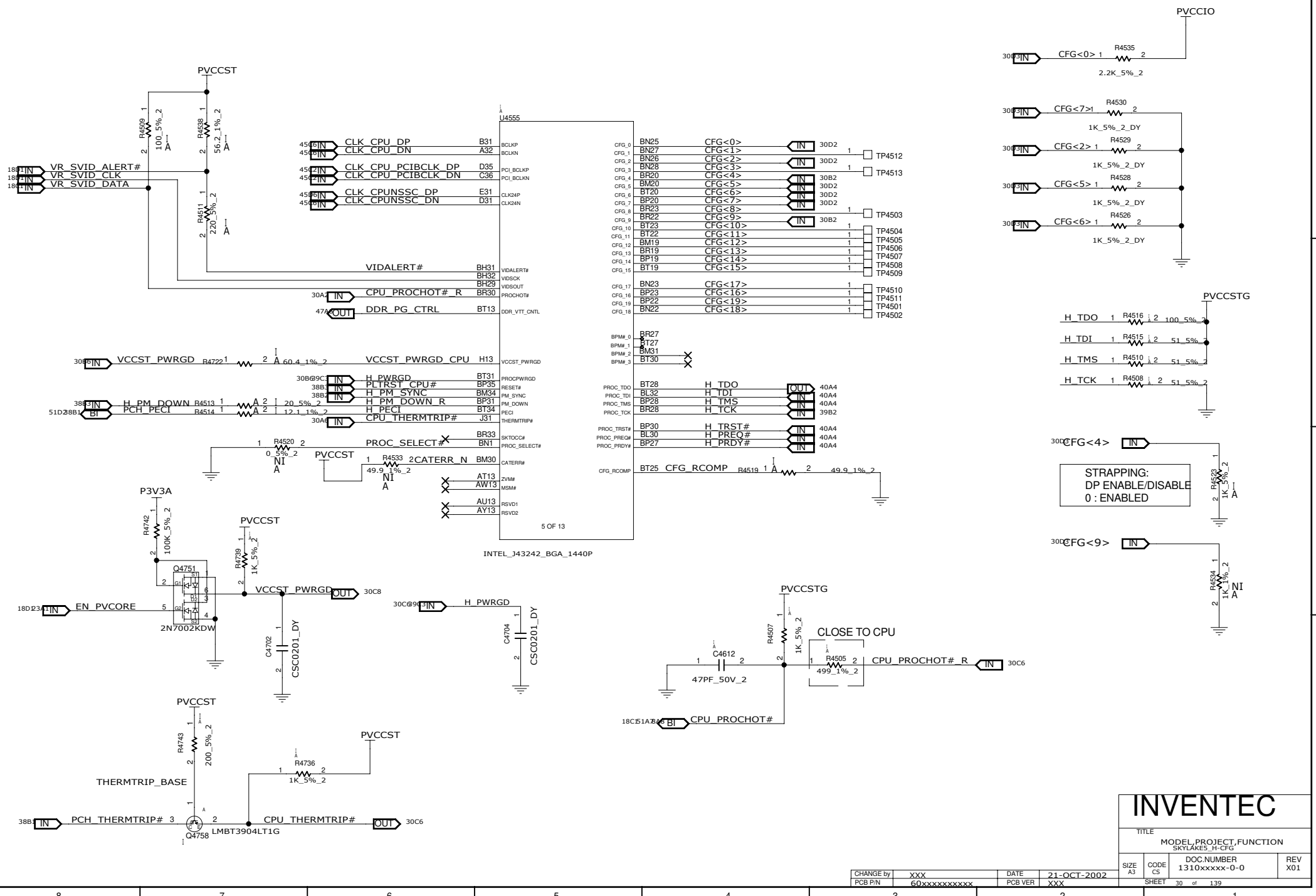
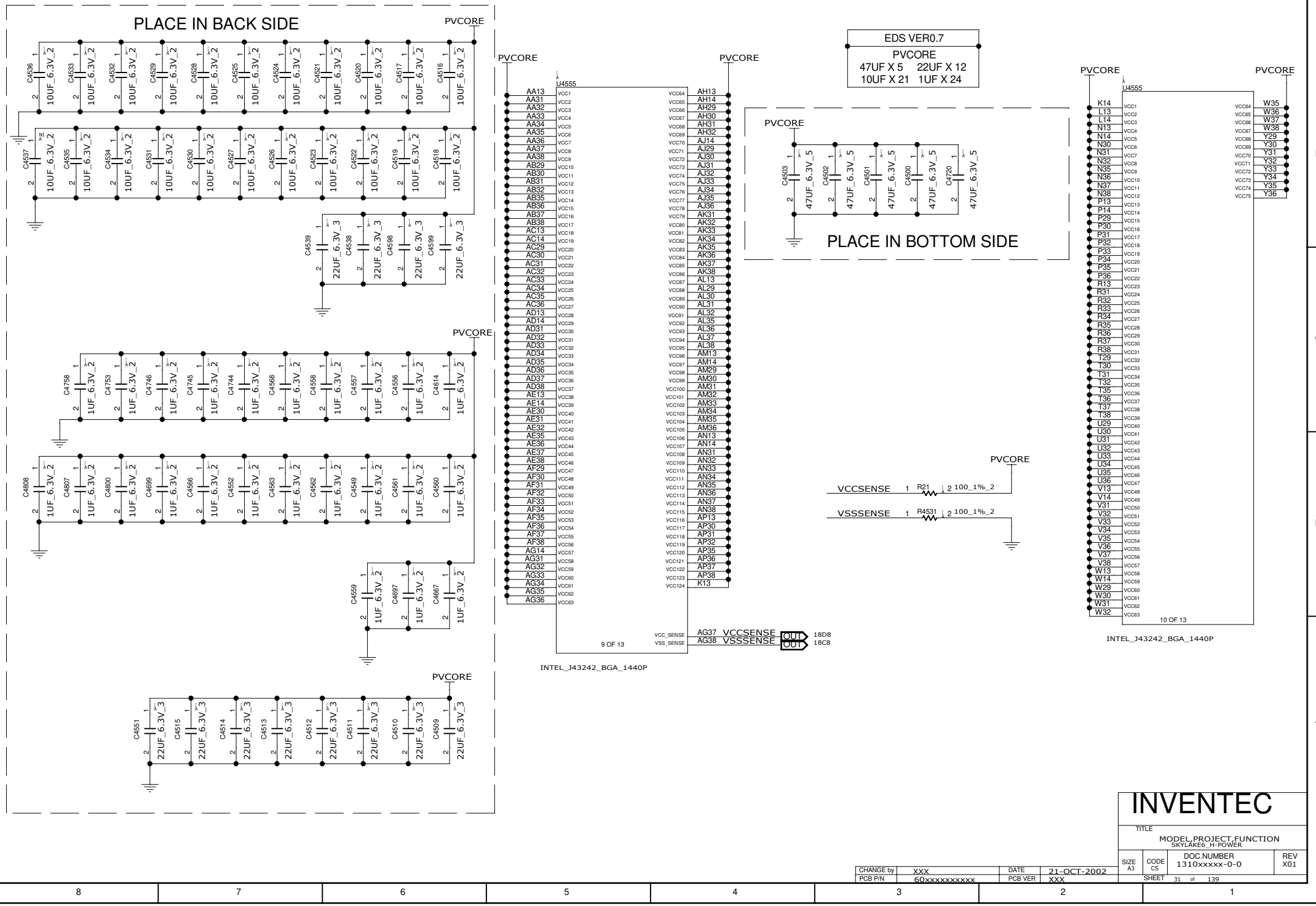


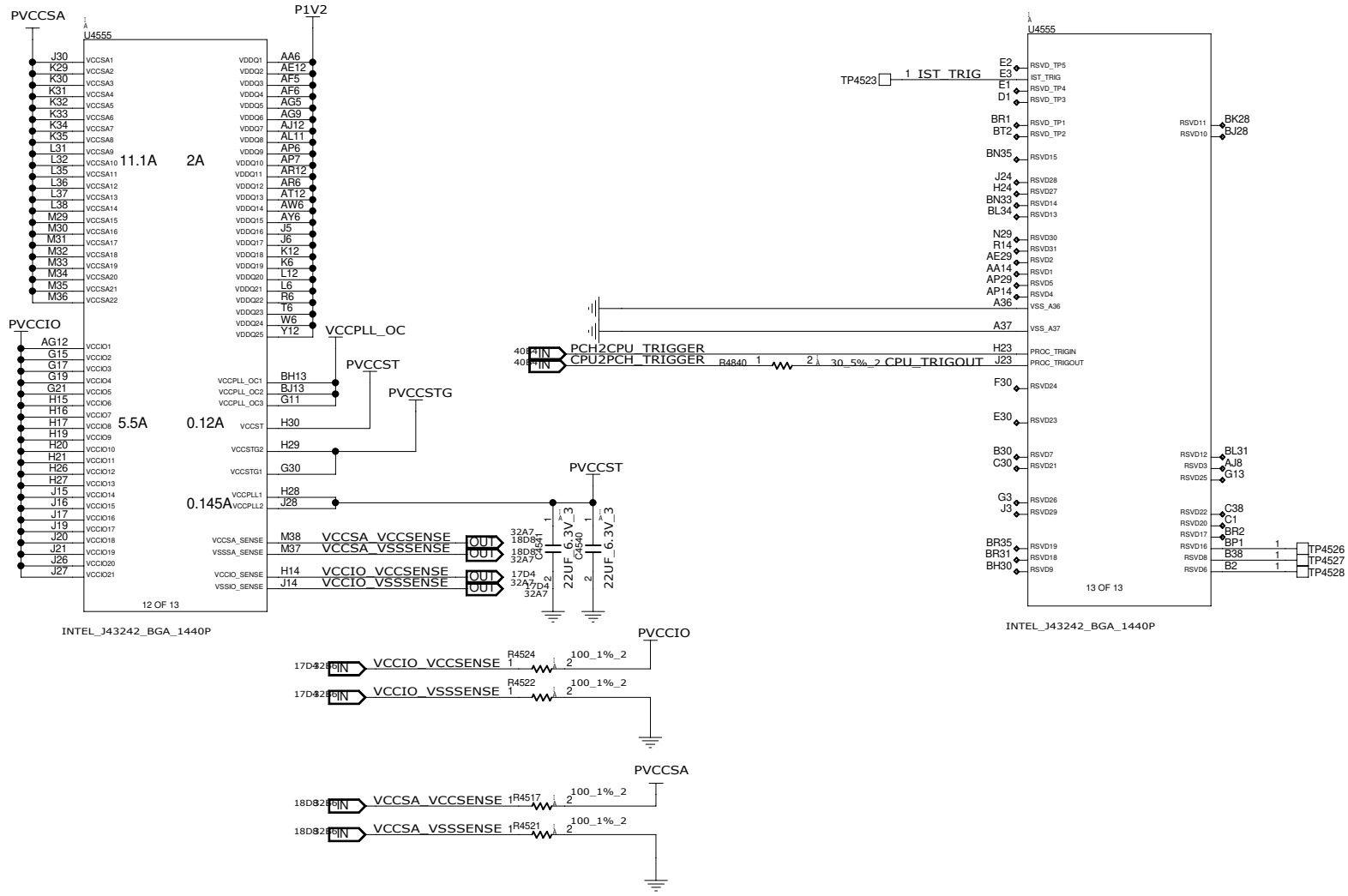
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE4_H-DDR-2

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	SHEET 29 of 139			


PVCCIO
CFG<0>
R4535
2.2K_5%_2
CFG<7>
R4530
1K_5%_2_DY
CFG<2>
R4529
1K_5%_2_DY
CFG<5>
R4528
1K_5%_2_DY
CFG<6>
R4526
1K_5%_2_DY
PVCCSTG
H_TDO
R4516
100_5%_2
H_TDI
R4515
51_5%_2
H_TMS
R4510
51_5%_2
H_TCK
R4508
51_5%_2
CFG<4>
R4533
1K_5%_2
STRAPPING:
DP ENABLE/DISABLE
0 : ENABLED
CFG<9>
R4534
1K_5%_2
NI
PVCCST
R4539
100_5%_2
R4538
56.2_1%_2
R4511
220_5%_2
VR_SVID_ALERT#
VR_SVID_CLK
VR_SVID_DATA
U4555
CLK_CPU_DP
CLK_CPU_DN
CLK_CPU_PCIBCLK_DP
CLK_CPU_PCIBCLK_DN
CLK_CPUNSSC_DP
CLK_CPUNSSC_DN
VIDALERT#
CPU_PROCHOT#_R
DDR_PG_CTRL
VCCST_PWRGD
R4722
60.4_1%_2
VCCST_PWRGD_CPU
H_PWRGD
PLTRST_CPU#
H_PM_SYNC
H_PM_DOWN_R
H_PECI
CPU_THERMTRIP#
H_PM_DOWN
PCH_PECI
R4513
R4514
20_5%_2
12.1_1%_2
PROC_SELECT#
R4520
0_5%_2
CATERR_N
R4533
49.9_1%_2
CFG_RCOMP
R4519
49.9_1%_2
5 OF 13
INTEL_J43242_BGA_1440P
TP4512
TP4513
TP4503
TP4504
TP4505
TP4506
TP4507
TP4508
TP4509
TP4510
TP4511
TP4501
TP4502
H_TDO
H_TDI
H_TMS
H_TCK
H_TRST#
H_PREQ#
H_PRDY#
P3V3A
R4742
100K_5%_2
R4739
1K_5%_2
Q4751
2N7002KDW
EN_PVCORE
VCCST_PWRGD
C4702
CSC0201_DY
H_PWRGD
C4704
CSC0201_DY
PVCCSTG
R4507
1K_5%_2
CLOSE TO CPU
C4612
47PF_50V_2
R4505
499_1%_2
CPU_PROCHOT#_R
CPU_PROCHOT#
PVCCST
R4743
200_5%_2
R4736
1K_5%_2
THERMTRIP_BASE
PCH_THERMTRIP#
CPU_THERMTRIP#
Q4758
LMBT3904LT1G
INVENTEC
TITLE
MODEL,PROJECT,FUNCTION
SKYLAKES_H-CFG
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET 30 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX


PLACE IN BACK SIDE
PVCORE
10UF_6.3V_2
22UF_6.3V_3
1UF_6.3V_2
EDS VER0.7
PVCORE
47UF X 5 22UF X 12
10UF X 21 1UF X 24
PLACE IN BOTTOM SIDE
47UF_6.3V_5
U4555
9 OF 13
10 OF 13
INTEL_J43242_BGA_1440P
VCCSENSE
VSSSENSE
R21
R4531
100_1%_2
AG37 VCCSENSE OUT 18D8
AG38 VSSSENSE OUT 18C8
INVENTEC
MODEL,PROJECT,FUNCTION
SKYLAKE6_H-POWER
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
CHANGE by XXX
PCB P/N 60xxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX
SHEET 31 of 139



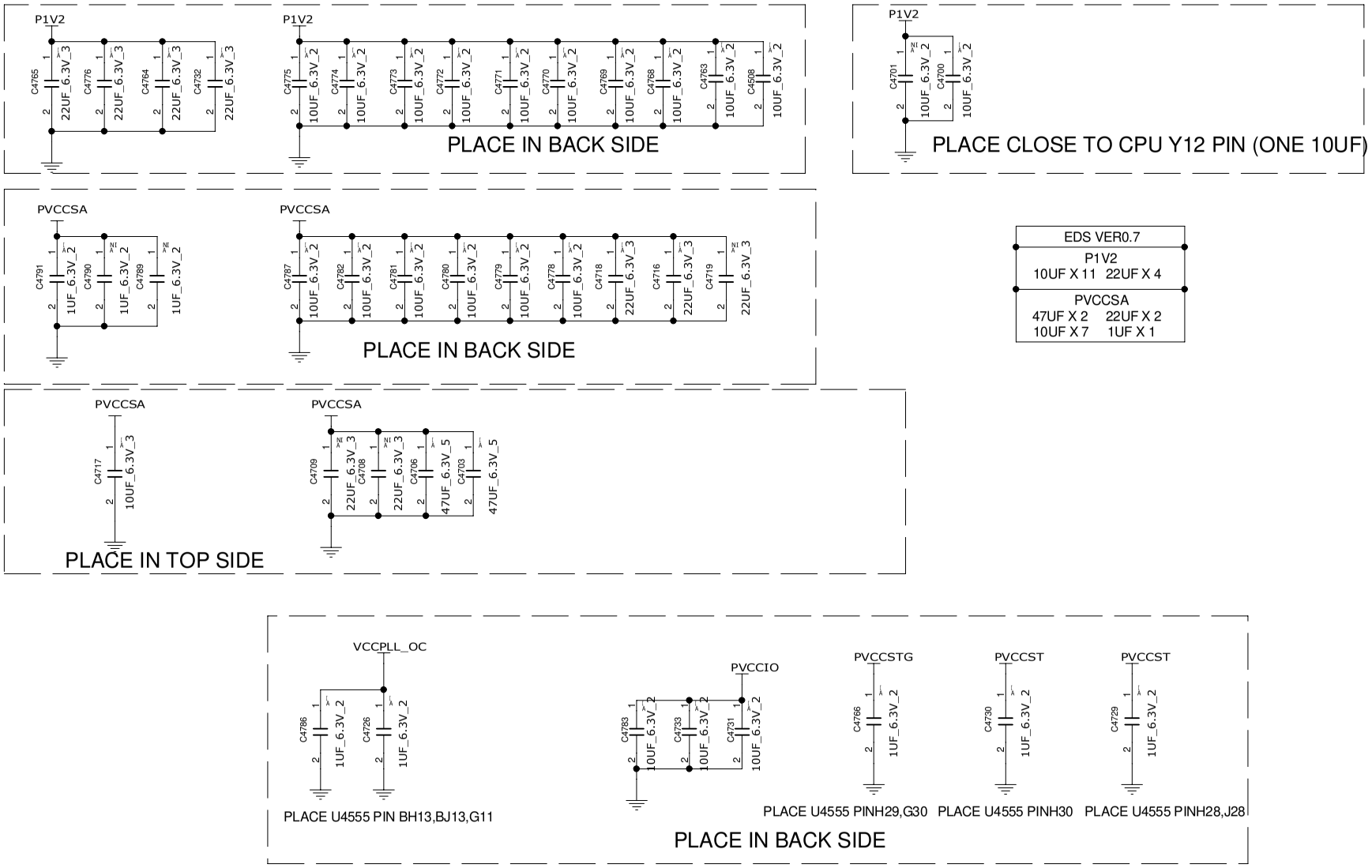
CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE7_H-POWER

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 32 of 139



INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
SKYLAKE8_H-DECOUPLING

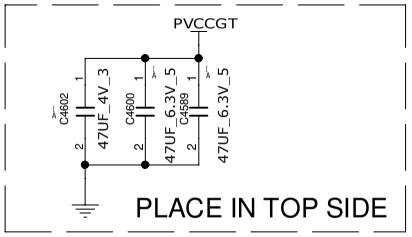
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

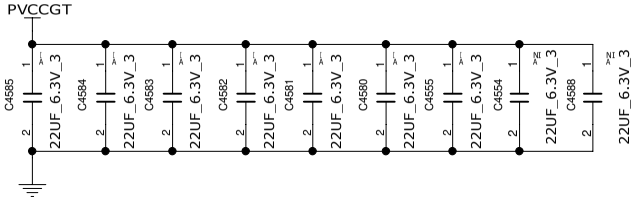
SHEET 33 of 139

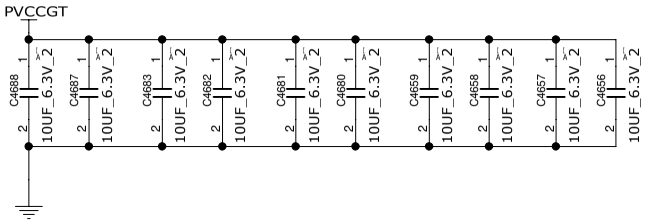
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

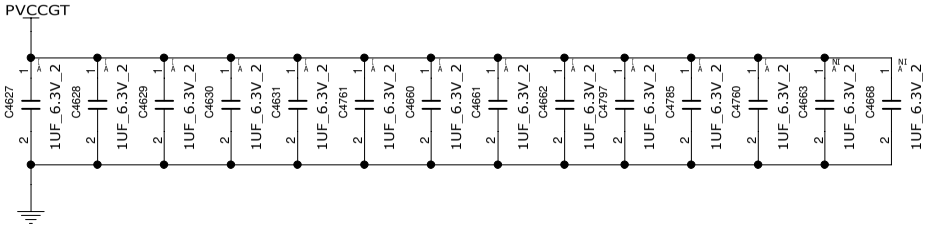
EDS VER0.7

PVCCGT
47UF X 3 22UF X 7
10UF X 10 1UF X 12

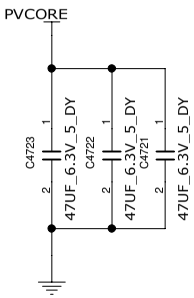


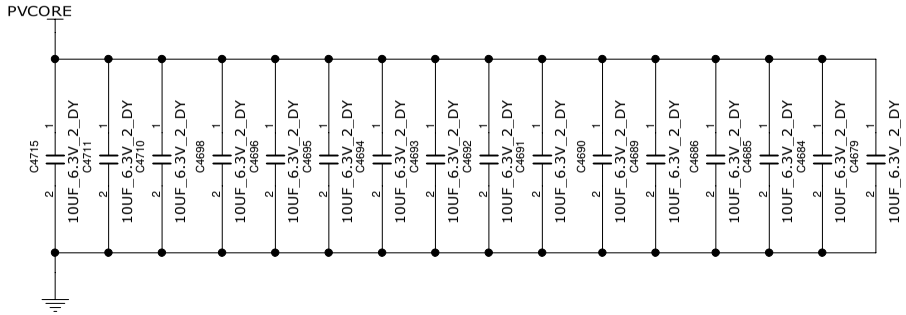


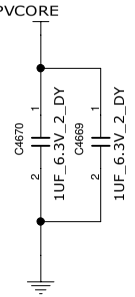




H82 CPU







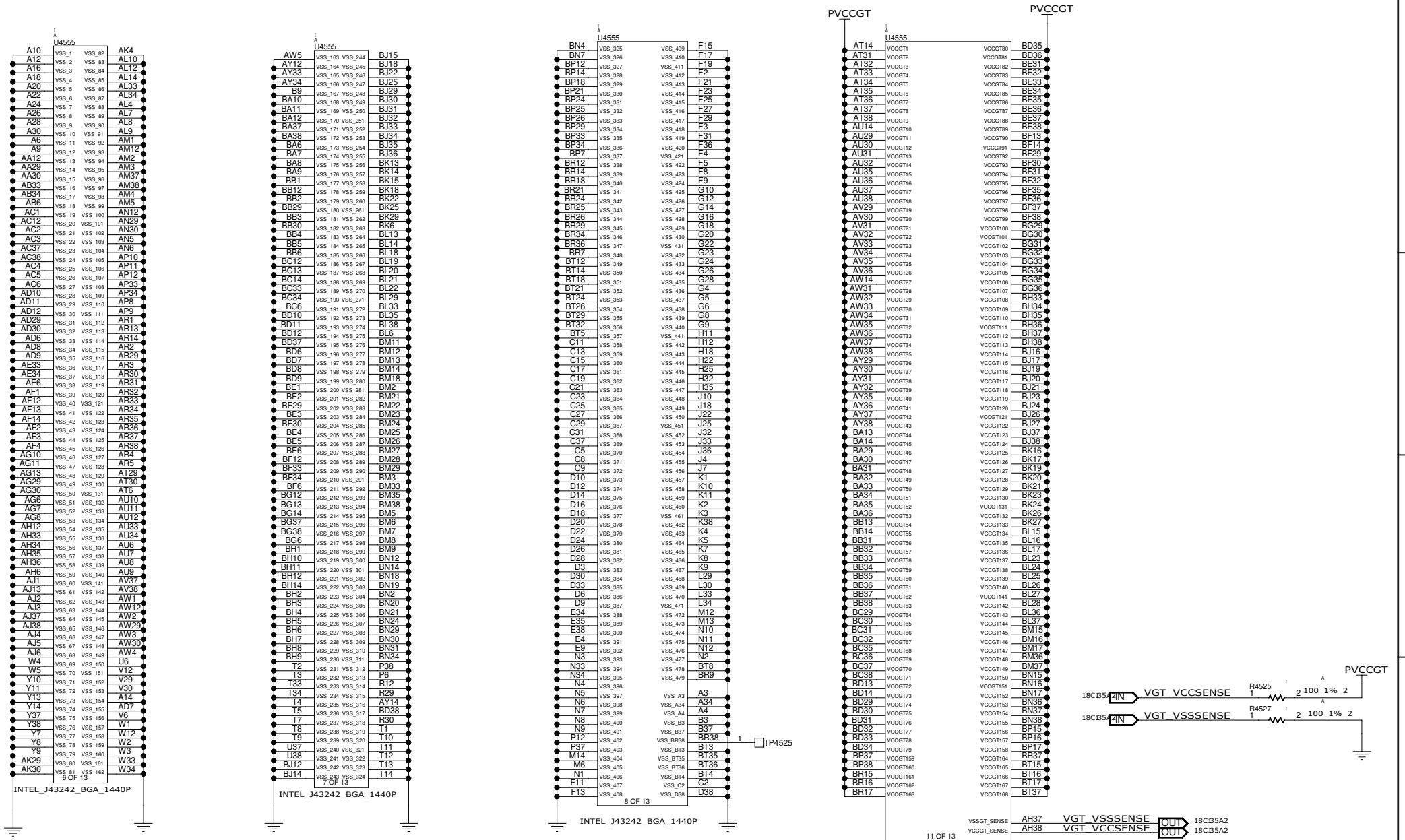
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE9_H-GT DECOUPLING

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 34 of 139



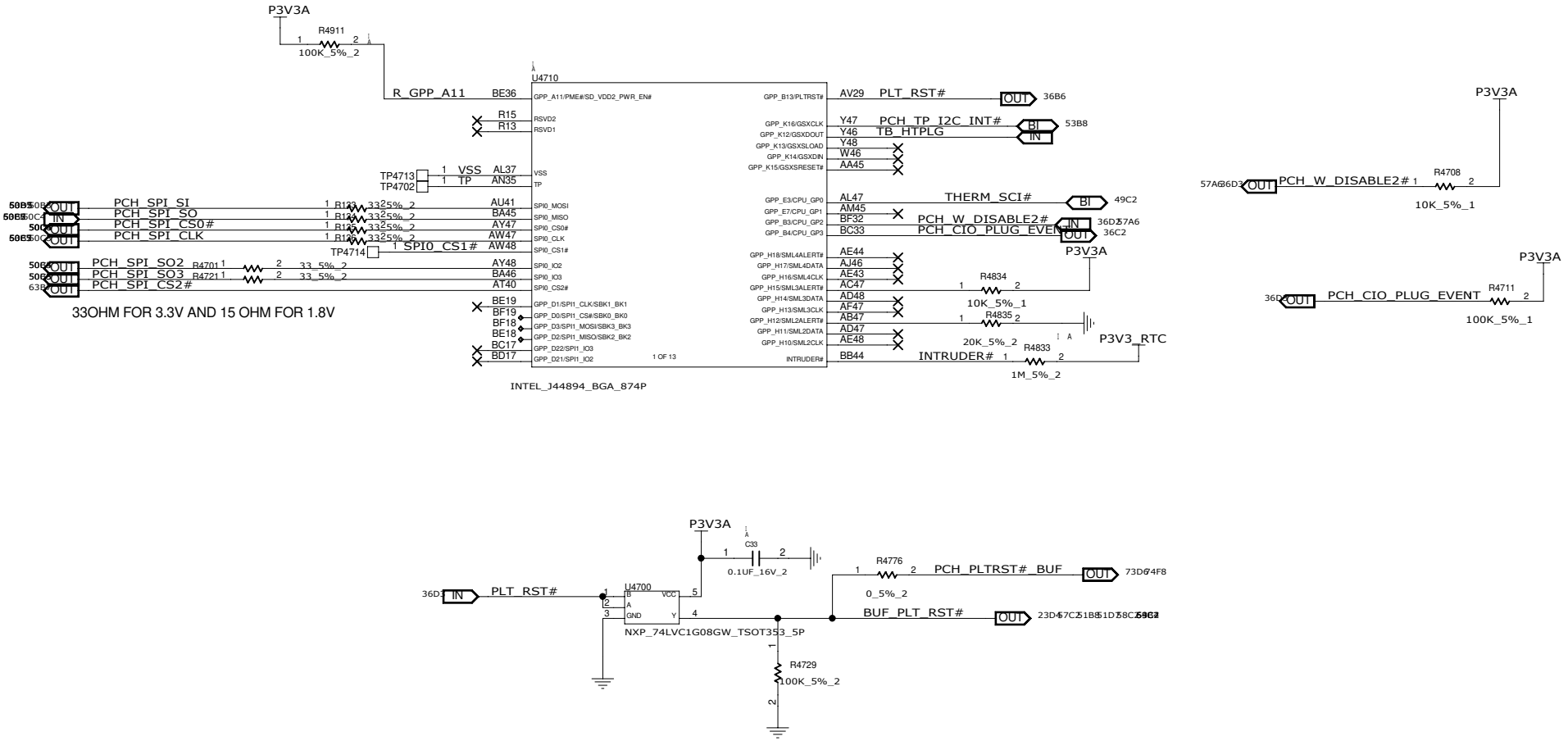
CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SKYLAKE10_H-GND

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

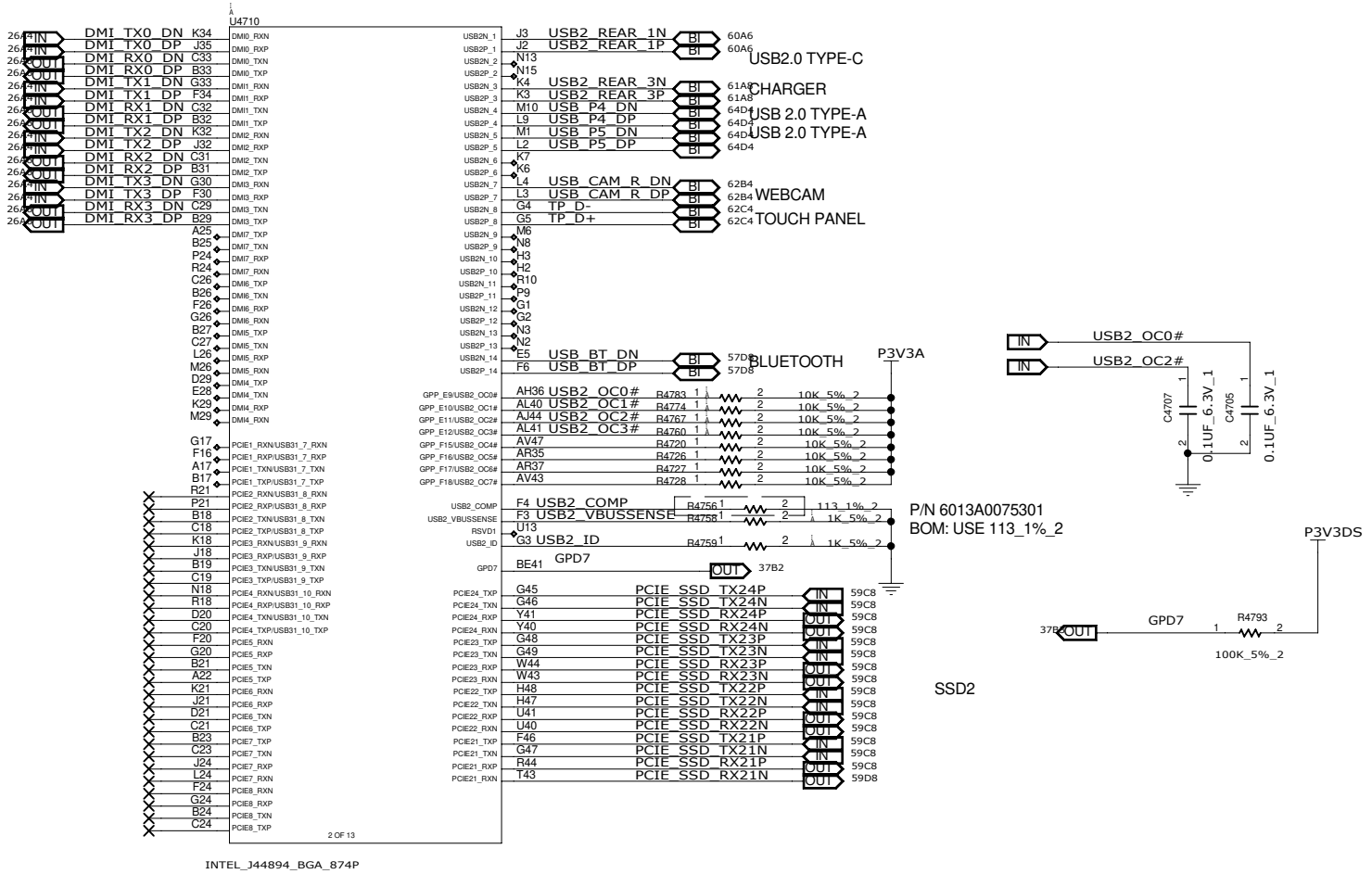
SHEET 35 of 139



INVENTEC

TITLE	MODEL,PROJECT,FUNCTION PCH-SPI,GPP
SIZE A3	CODE CS
DOC.NUMBER	1310xxxxx-0-0
REV	X01
SHEET	36 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



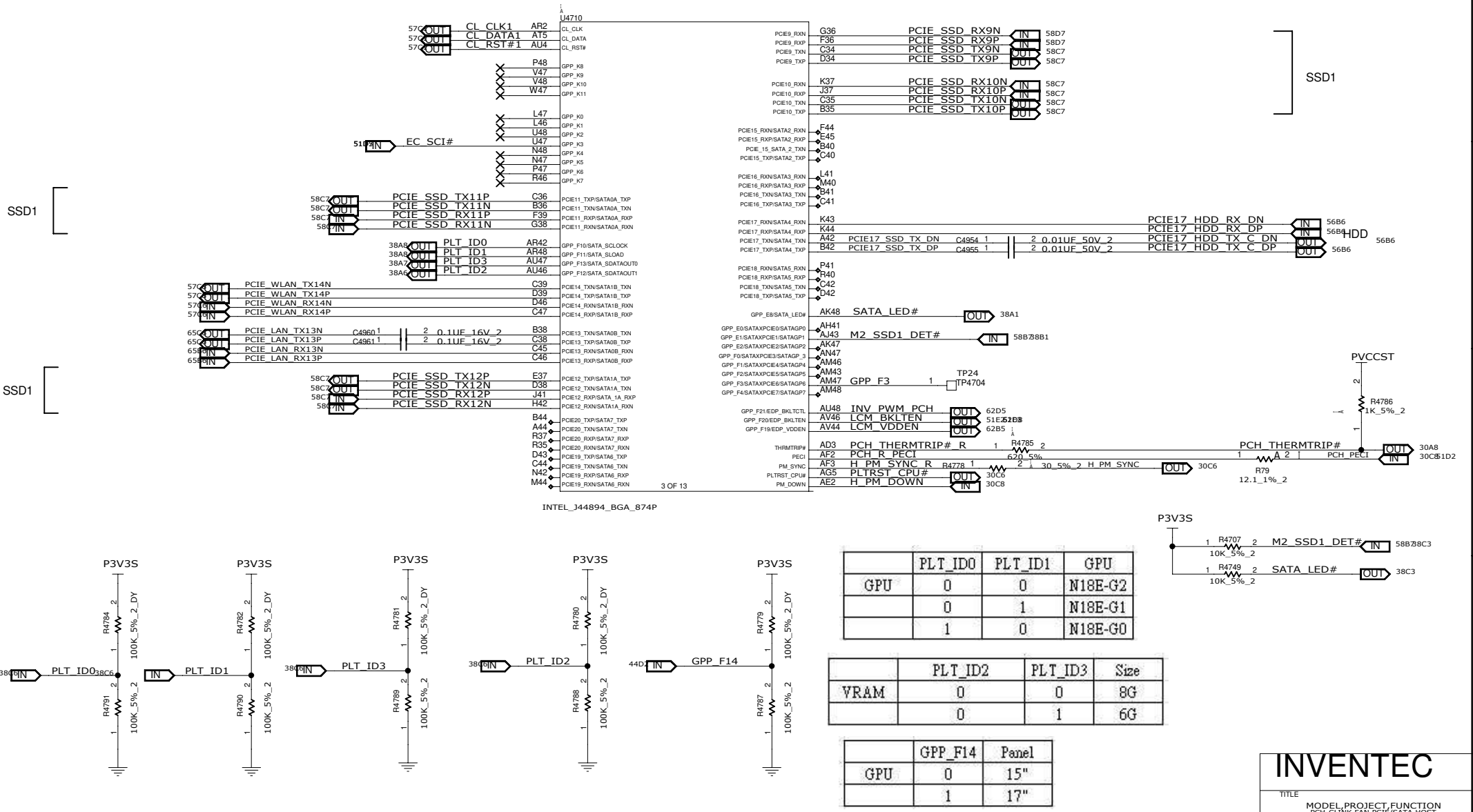
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-DMI,USB2,USB3

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 37 of 139



	PLT_ID0	PLT_ID1	GPU
GPU	0	0	N18E-G2
	0	1	N18E-G1
	1	0	N18E-G0

	PLT_ID2	PLT_ID3	Size
VRAM	0	0	8G
	0	1	6G

	GPP_F14	Panel
GPU	0	15"
	1	17"

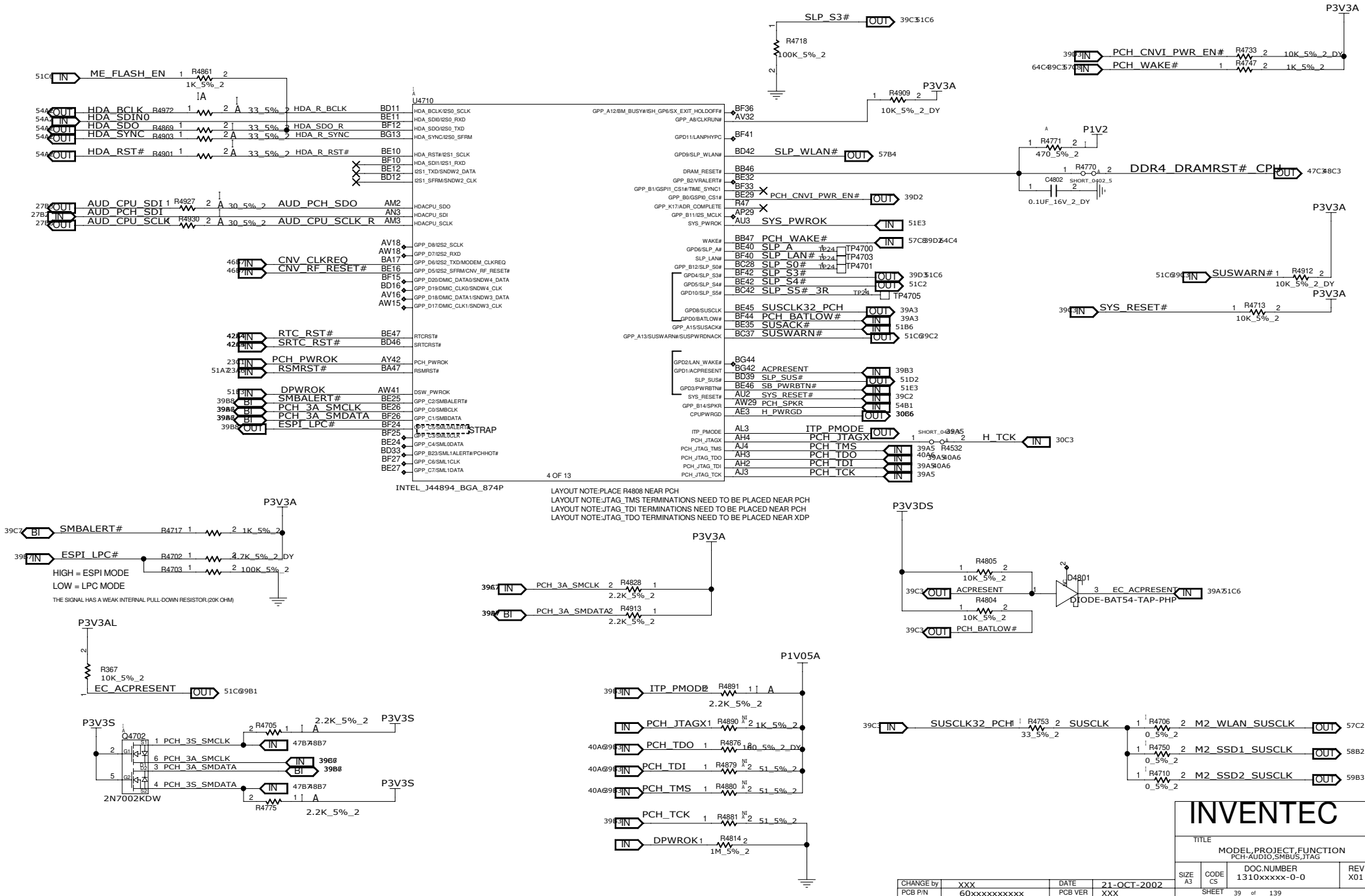
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-CLINK,FAN,PCIE/SATA,HOST

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 38 of 139



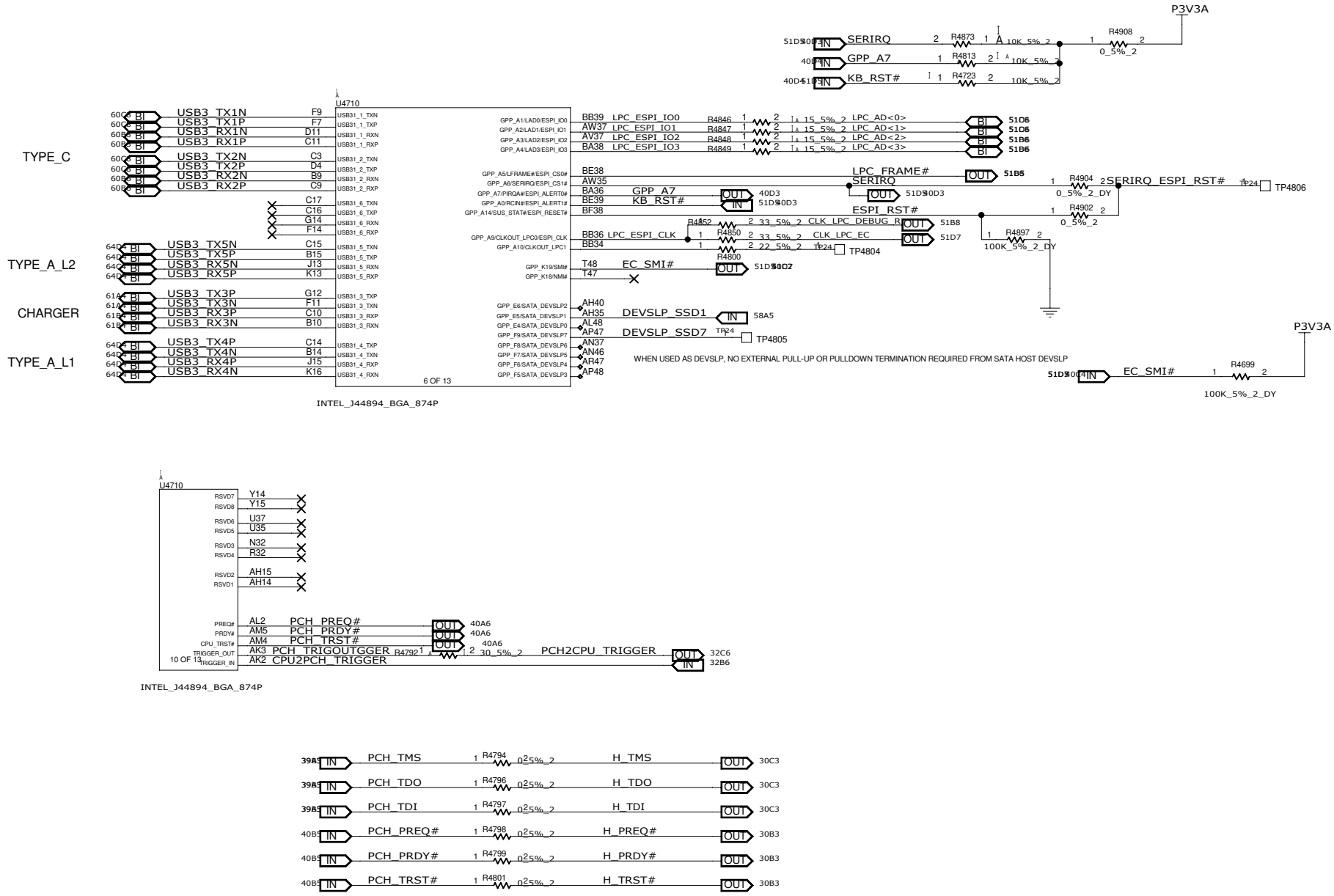
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-AUDIO,SMBUS,JTAG

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 39 of 139



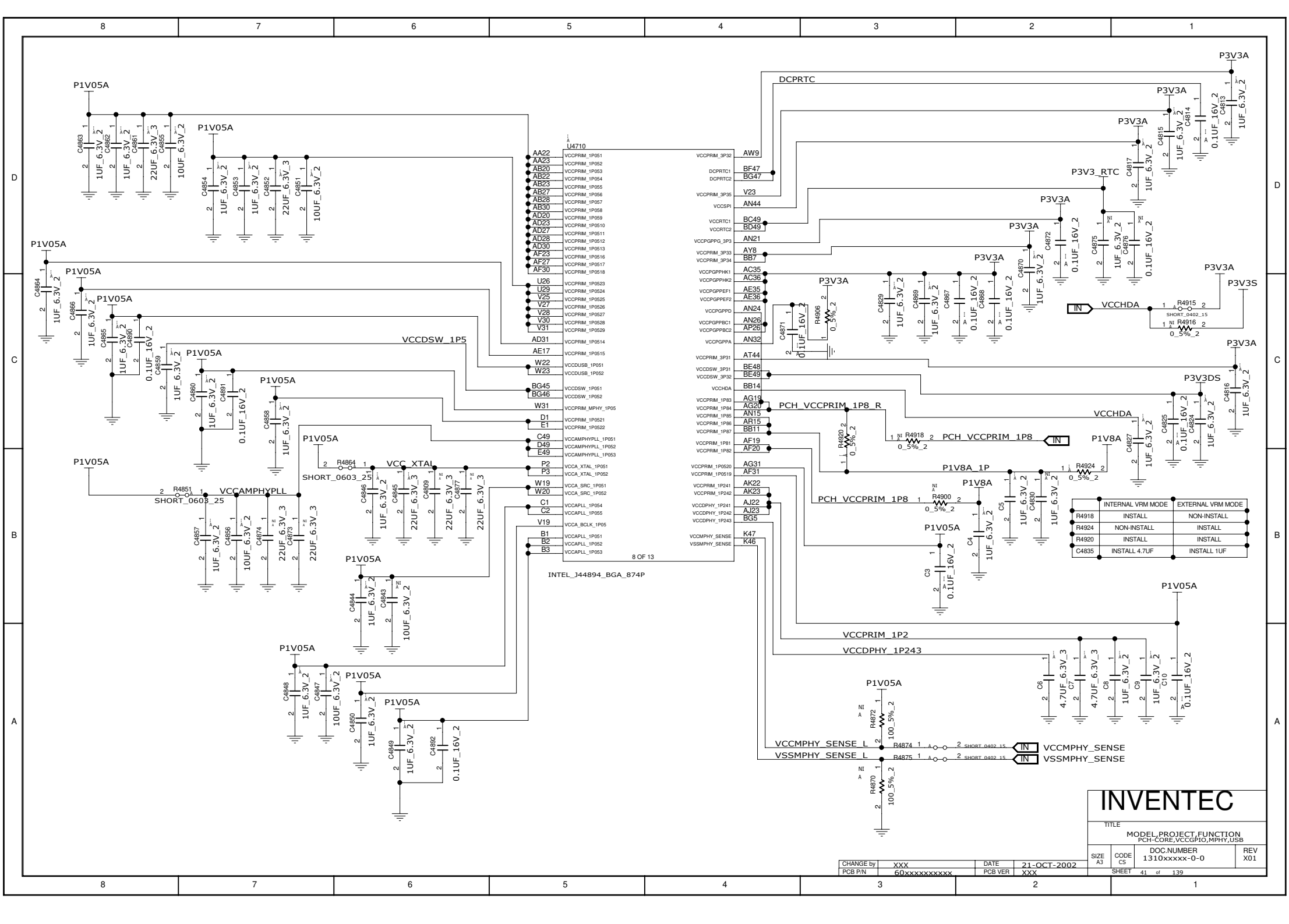
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

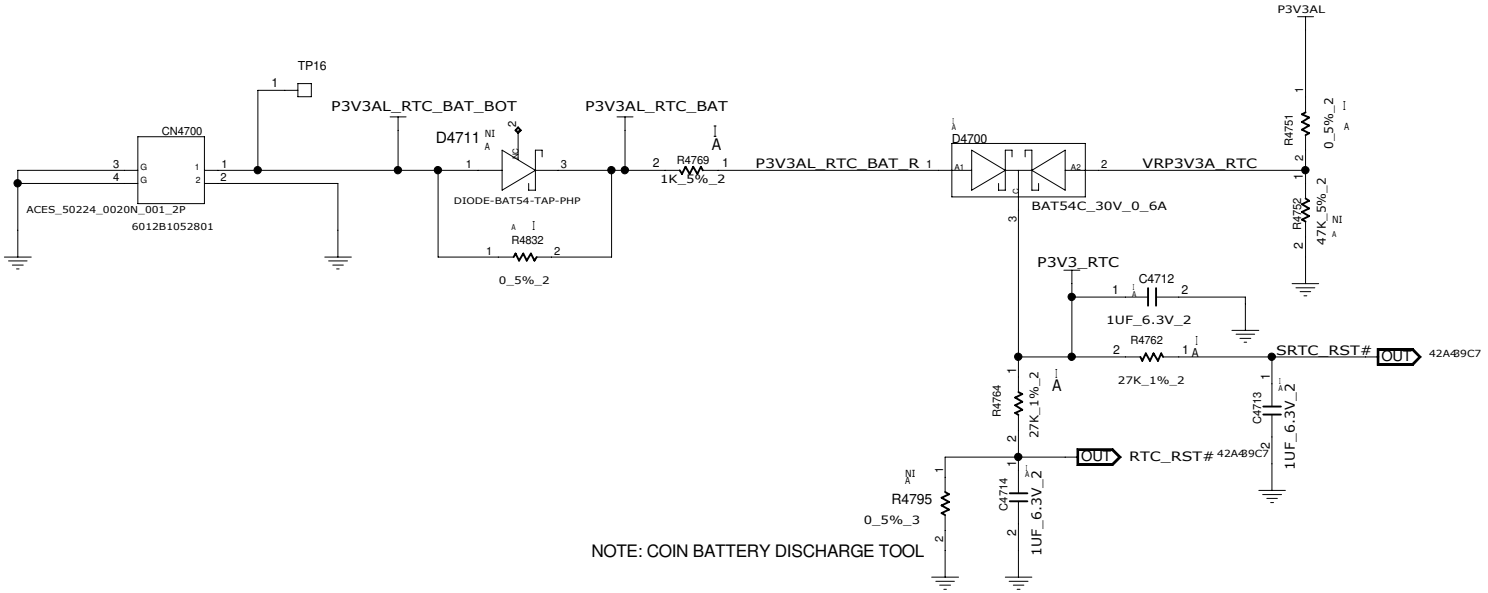
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-LPC/ESPI,USB,SATA

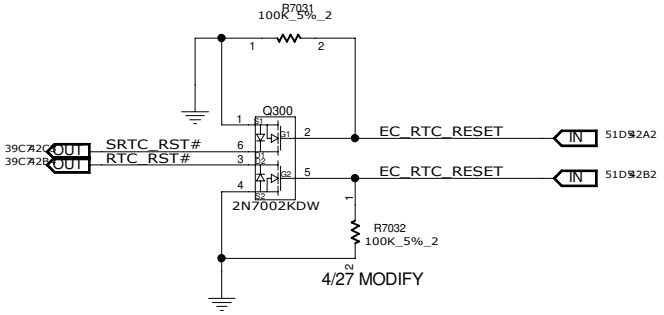
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 40 of 139


U4710
INTEL_J44894_BGA_874P
8 OF 13
P1V05A
P3V3A
P3V3_RTC
P3V3S
P3V3DS
P1V8A
VCCDSW_1P5
VCC_XTAL
VCCAMPHYPLL
DCPRTC
PCH_VCCPRIM_1P8_R
PCH_VCCPRIM_1P8
P1V8A_1P
VCCHDA
VCCPRIM_1P2
VCCDPHY_1P243
VCCMPHY_SENSE_L
VSSMPHY_SENSE_L
VCCMPHY_SENSE
VSSMPHY_SENSE
SHORT_0603_25
SHORT_0402_15
INTERNAL VRM MODE
EXTERNAL VRM MODE
R4918 INSTALL NON-INSTALL
R4924 NON-INSTALL INSTALL
R4920 INSTALL INSTALL
C4835 INSTALL 4.7UF INSTALL 1UF
INVENTEC
MODEL,PROJECT,FUNCTION
PCH-CORE,VCCGPIO,MPHY,USB
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET 41 of 139
CHANGE by XXX
DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx
PCB VER XXX



LPC & ESPI TABLE		
	LPC MODE	ESPI MODE
R4710	INSTAL	UNINSTAL
R4709	UNINSTAL	INSTAL



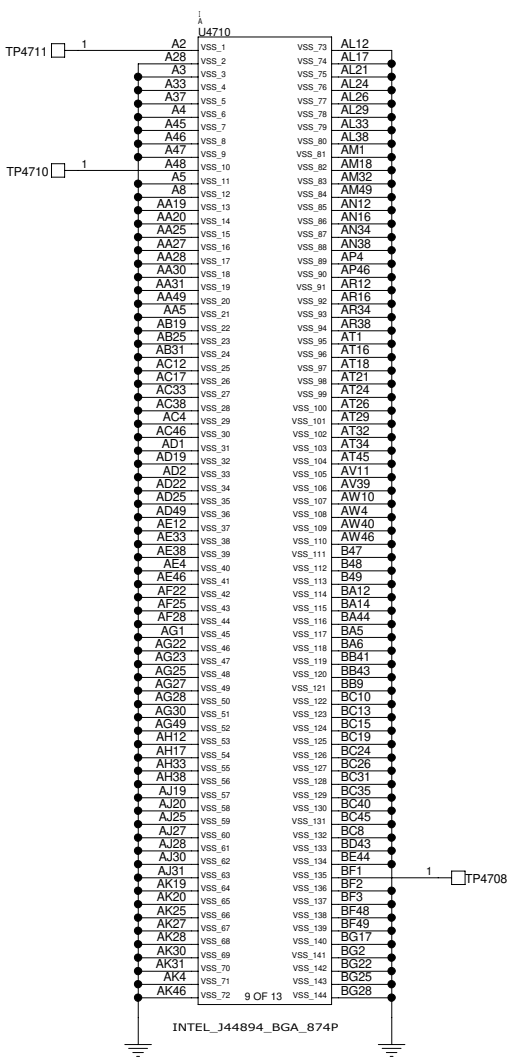
INVENTEC

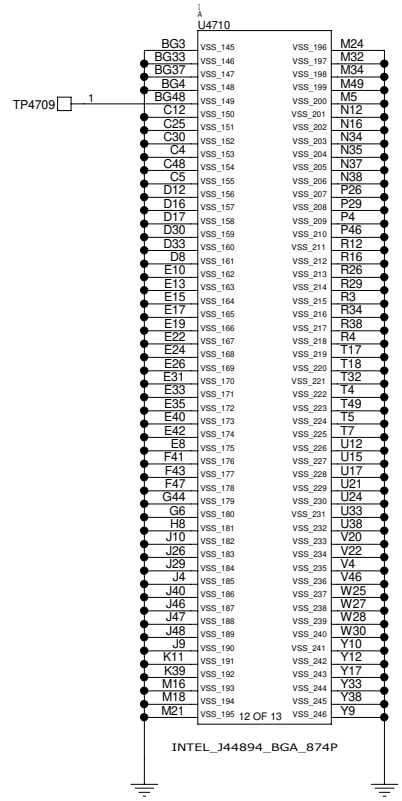
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 42 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX





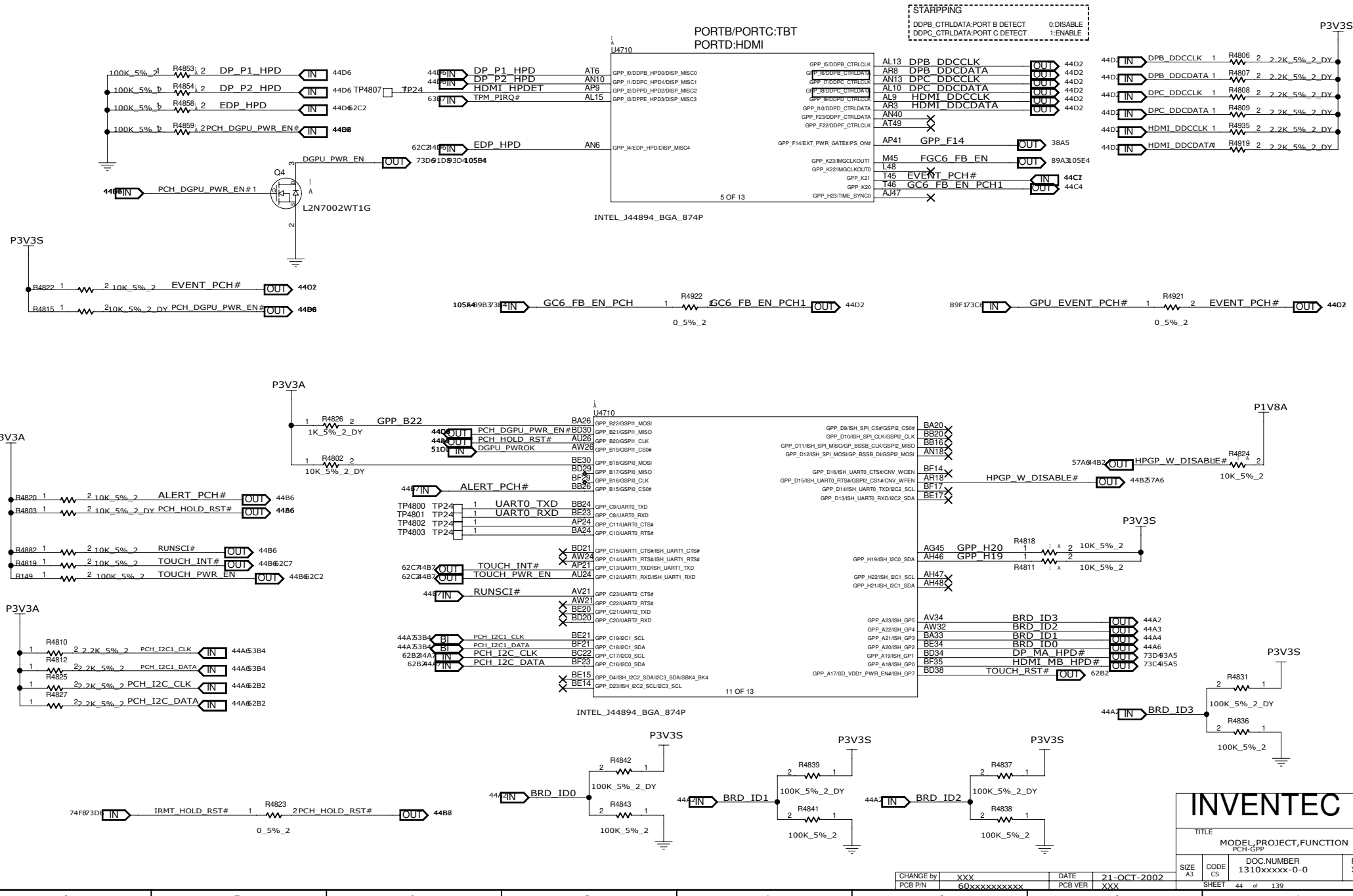
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
PCH-GND

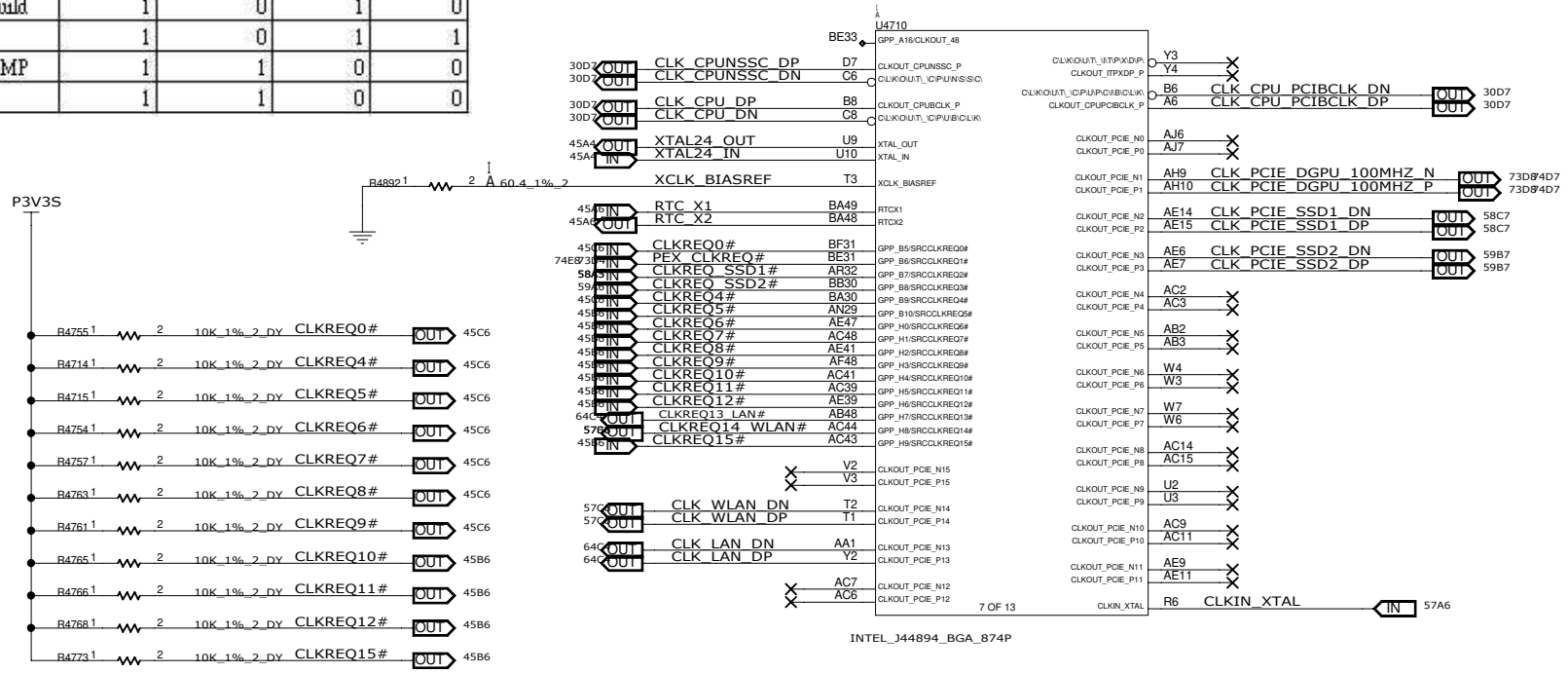
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

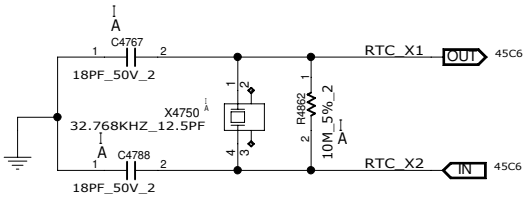
SHEET 43 of 139

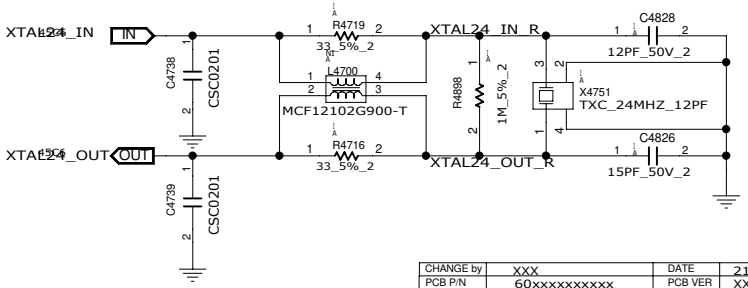

STARPPING
DDPB_CTRLDATA:PORT B DETECT 0:DISABLE
DDPC_CTRLDATA:PORT C DETECT 1:ENABLE
PORTB/PORTC:TBT
PORTD:HDMI
U4710
INTEL_J44894_BGA_874P
5 OF 13
11 OF 13
P3V3S
P3V3A
P1V8A
DP_P1_HPD
DP_P2_HPD
EDP_HPD
PCH_DGPU_PWR_EN#
DGPU_PWR_EN
Q4
L2N7002WT1G
EVENT_PCH#
GC6_FB_EN_PCH
GC6_FB_EN_PCH1
GPU_EVENT_PCH#
GPP_B22
PCH_DGPU_PWR_EN#
PCH_HOLD_RST#
DGPU_PWROK
ALERT_PCH#
UART0_TXD
UART0_RXD
TOUCH_INT#
TOUCH_PWR_EN
RUNSCI#
PCH_I2C1_CLK
PCH_I2C1_DATA
PCH_I2C_CLK
PCH_I2C_DATA
IRMT_HOLD_RST#
HPGP_W_DISABLE#
GPP_H20
GPP_H19
BRD_ID3
BRD_ID2
BRD_ID1
BRD_ID0
DP_MA_HPD#
HDMI_MB_HPD#
TOUCH_RST#
DPB_DDCCLK
DPB_DDCDATA
DPC_DDCCLK
DPC_DDCDATA
HDMI_DDCCLK
HDMI_DDCDATA
HDMI_HPDET
TPM_PIRQ#
FGC6_FB_EN
GPP_F14
INVENTEC
MODEL,PROJECT,FUNCTION
PCH-GPP
DOC.NUMBER 1310xxxxx-0-0
REV X01
SIZE A3
CODE CS
SHEET 44 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX

	GPP_A23	GPP_A22	GPP_A21	GPP_A20
A build0	0	0	0	0
A build1	0	0	0	1
B build0	0	1	0	0
B build1	0	1	0	1
B build2	0	1	1	0
	0	1	1	1
C build0	1	0	0	0
	1	0	0	1
D build	1	0	1	0
	1	0	1	1
Pre-MP	1	1	0	0
MP	1	1	0	0

1. SSC = Spread Spectrum Clocking
2. The SRCCLKREQ#[15:0] signals can be configured to map to any of the PCH-H PCI Express* Root Ports
3. SRCCLKREQ#[15:0] to CLKOUT_PCIE_P/N[15:0] Mapping Requirements
   - SRCCLKREQ#[7:0] signals can be mapped to any of the CLKOUT_PCIE_P/N[7:0] differential clock pairs
   - SRCCLKREQ#[15:8] signals can be mapped to any of the CLKOUT_PCIE_P/N[15:8] differential clock pairs







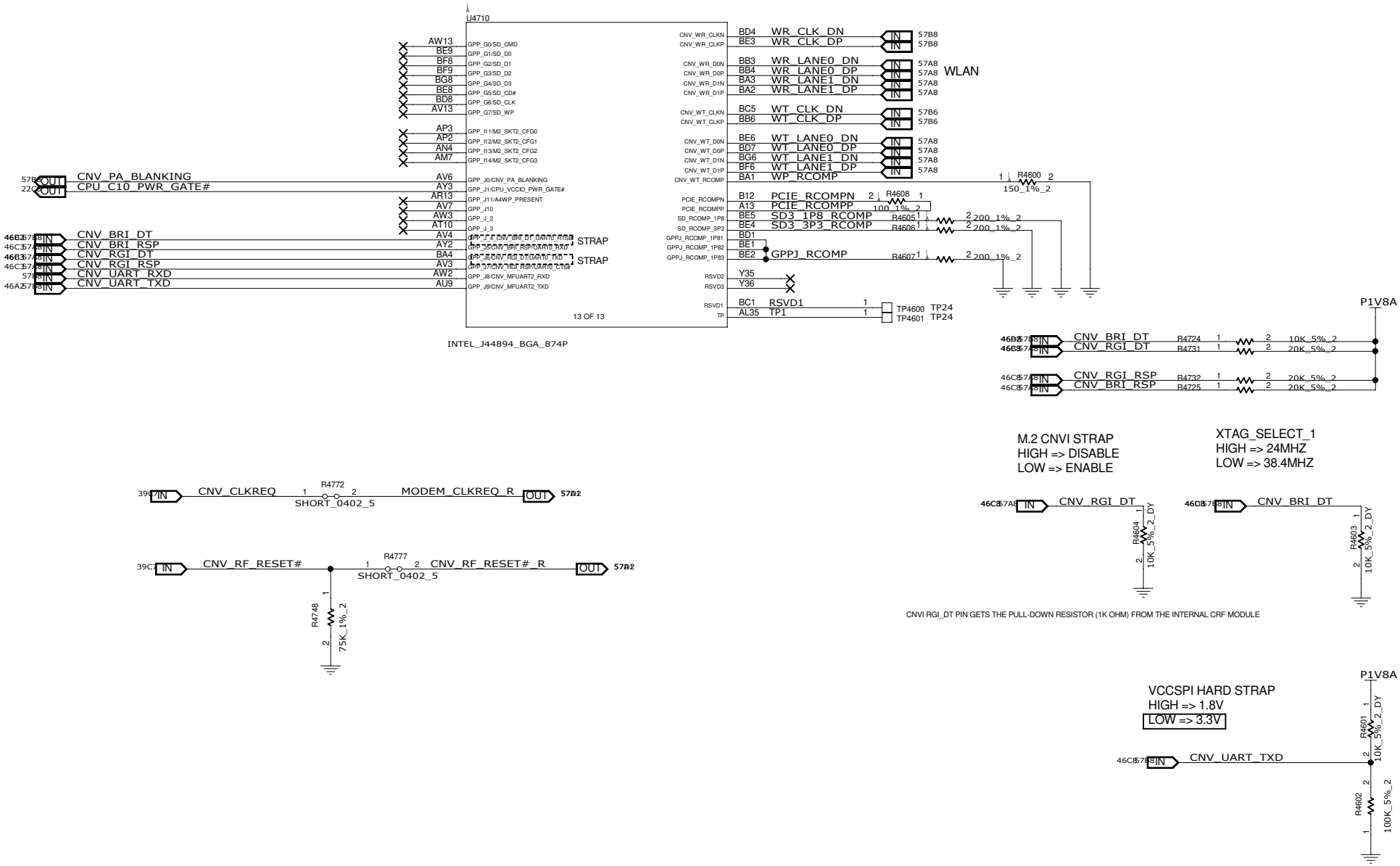
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
PCH-GPP,CLKOUT

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 45 of 139



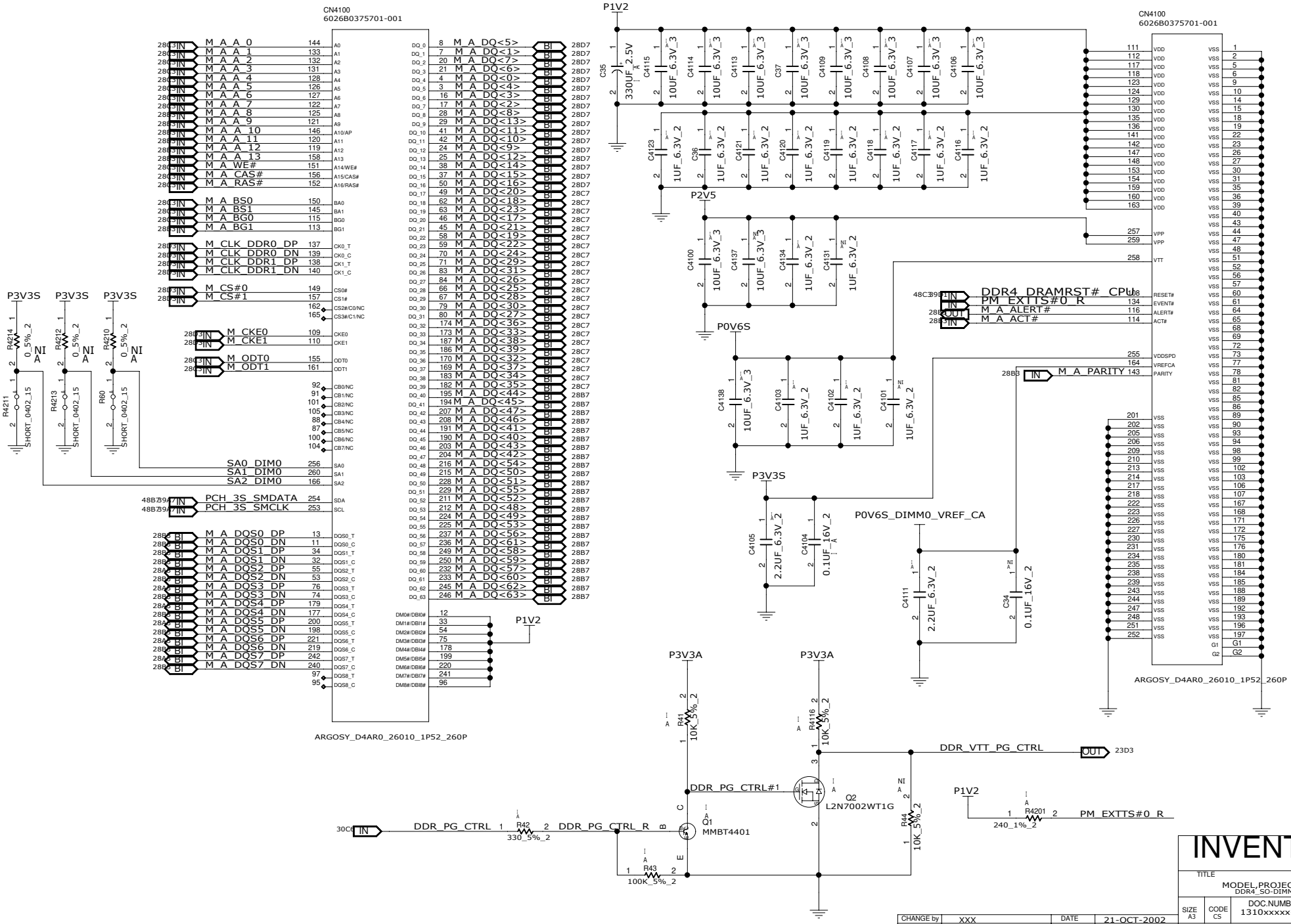
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 46 of 139


CN4100
6026B0375701-001
M_A_A_0
M_A_A_1
M_A_A_2
M_A_A_3
M_A_A_4
M_A_A_5
M_A_A_6
M_A_A_7
M_A_A_8
M_A_A_9
M_A_A_10
M_A_A_11
M_A_A_12
M_A_A_13
M_A_WE#
M_A_CAS#
M_A_RAS#
M_A_BS0
M_A_BS1
M_A_BG0
M_A_BG1
M_CLK_DDR0_DP
M_CLK_DDR0_DN
M_CLK_DDR1_DP
M_CLK_DDR1_DN
M_CS#0
M_CS#1
M_CKE0
M_CKE1
M_ODT0
M_ODT1
SA0_DIM0
SA1_DIM0
SA2_DIM0
PCH_3S_SMDATA
PCH_3S_SMCLK
M_A_DQS0_DP
M_A_DQS0_DN
M_A_DQS1_DP
M_A_DQS1_DN
M_A_DQS2_DP
M_A_DQS2_DN
M_A_DQS3_DP
M_A_DQS3_DN
M_A_DQS4_DP
M_A_DQS4_DN
M_A_DQS5_DP
M_A_DQS5_DN
M_A_DQS6_DP
M_A_DQS6_DN
M_A_DQS7_DP
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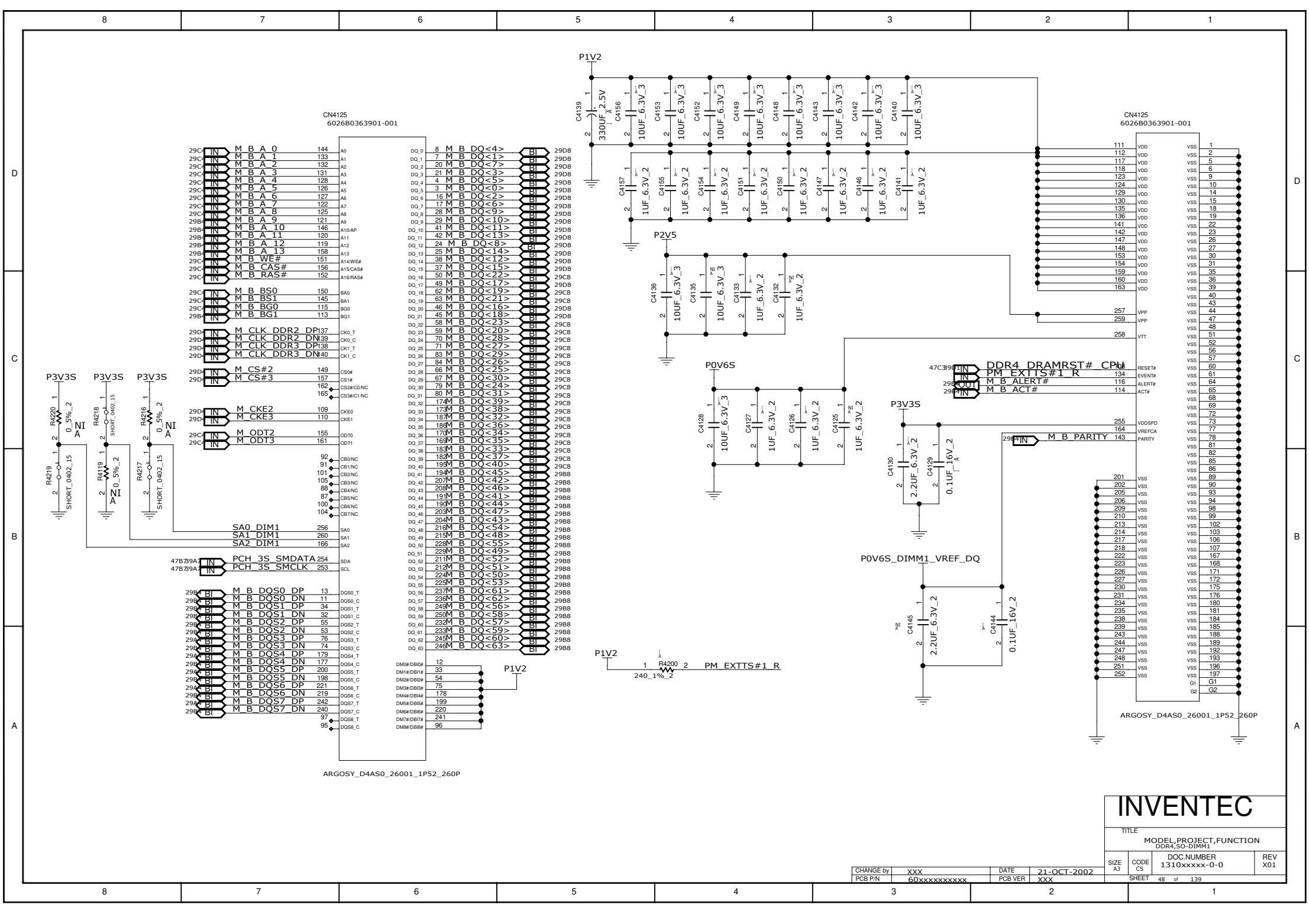
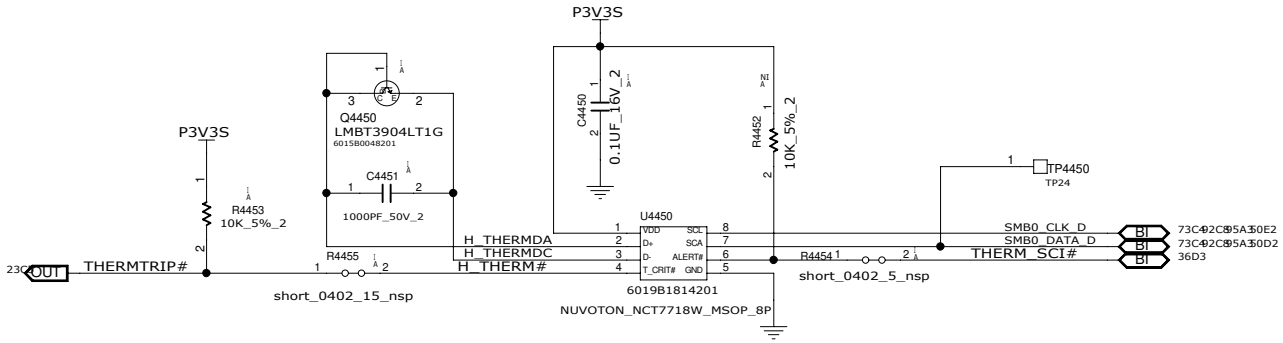
M_A_DQ<57>
M_A_DQ<60>
M_A_DQ<62>
M_A_DQ<63>
ARGOSY_D4AR0_26010_1P52_260P
P3V3S
P1V2
P2V5
P0V6S
P3V3A
R4214
R4212
R4210
R4211
R4213
R60
SHORT_0402_15
0_5%_2
NI
C35
330UF_2.5V
10UF_6.3V_3
10UF_6.3V_2
1UF_6.3V_2
1UF_6.3V_3
2.2UF_6.3V_2
0.1UF_16V_2
DDR4_DRAMRST#_CPU
PM_EXTTS#0_R
M_A_ALERT#
M_A_ACT#
M_A_PARITY
P0V6S_DIMM0_VREF_CA
DDR_VTT_PG_CTRL
DDR_PG_CTRL#1
DDR_PG_CTRL
DDR_PG_CTRL_R
R41
R4116
R42
R43
R44
R4201
10K_5%_2
330_5%_2
100K_5%_2
240_1%_2
Q1
MMBT4401
Q2
L2N7002WT1G
INVENTEC
MODEL,PROJECT,FUNCTION
DDR4_SO-DIMM0
SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
SHEET 47 of 139
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX


CN4125
6026B0363901-001
ARGOSY_D4AS0_26001_1P52_260P
P1V2
P2V5
P0V6S
P3V3S
M_B_A_0
M_B_A_1
M_B_A_2
M_B_A_3
M_B_A_4
M_B_A_5
M_B_A_6
M_B_A_7
M_B_A_8
M_B_A_9
M_B_A_10
M_B_A_11
M_B_A_12
M_B_A_13
M_B_WE#
M_B_CAS#
M_B_RAS#
M_B_BS0
M_B_BS1
M_B_BG0
M_B_BG1
M_CLK_DDR2_DP
M_CLK_DDR2_DN
M_CLK_DDR3_DP
M_CLK_DDR3_DN
M_CS#2
M_CS#3
M_CKE2
M_CKE3
M_ODT2
M_ODT3
SA0_DIM1
SA1_DIM1
SA2_DIM1
PCH_3S_SMDATA
PCH_3S_SMCLK
M_B_DQS0_DP
M_B_DQS0_DN
M_B_DQS1_DP
M_B_DQS1_DN
M_B_DQS2_DP
M_B_DQS2_DN
M_B_DQS3_DP
M_B_DQS3_DN
M_B_DQS4_DP
M_B_DQS4_DN
M_B_DQS5_DP
M_B_DQS5_DN
M_B_DQS6_DP
M_B_DQS6_DN
M_B_DQS7_DP
M_B_DQS7_DN
DDR4_DRAMRST#_CPU
PM_EXTTS#1_R
M_B_ALERT#
M_B_ACT#
M_B_PARITY
P0V6S_DIMM1_VREF_DQ
PM_EXTTS#1_R
INVENTEC
MODEL,PROJECT,FUNCTION
DDR4,SO-DIMM1
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SIZE
A3
CODE
CS
SHEET 48 of 139
CHANGE by XXX
DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx
PCB VER XXX

REFERENCE NUMBER:4450~4499

THERM SENSOR



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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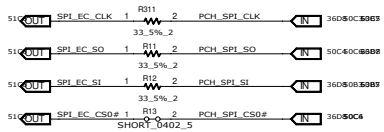
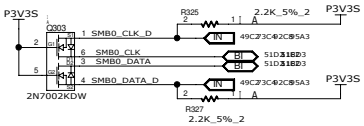
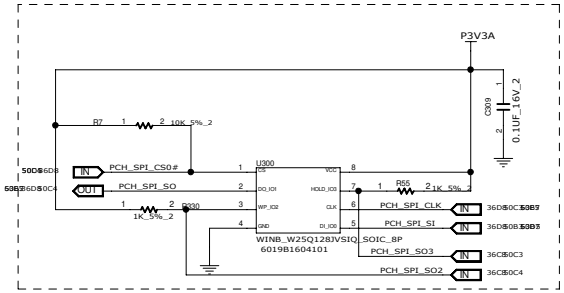
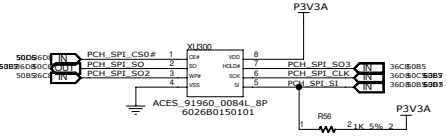
REFERENCE 300~389(KBC)





THERMAL SENSOR
HDMI
DP





R390 FOR INTEL DEBUG

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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EC

Location 300 ~ 2013EE1B Ver.05_20120824

	VCC(1.8V OR 3.3V)	VSTBY_FSPI(1.8V OR 3.3V)
IT8987E_CX	PIN13 : LPCCLK/GPM4(3) PIN10 : LAD0/GPM0(3) PIN9 : LAD1/GPM1(3) PIN8 : LAD2/GPM2(3) PIN7 : LAD3/GPM3(3) PIN6 : LFRAME#/GPM5(3)	PIN5 : SERIRQ/GPM6(3) PIN105 : FSCK/GPG7 PIN101 : FSCE#/GPG3 PIN102 : FMOSI/GPG4 PIN103 : FMISO/GPG5

FOR DPTF

Intel DS3 function support

U1

ITE_IT8987E_CX_LQFP_128P_HP

6019B1650401

LPC

GPIO

SMBUS

PS/2

CIR

PWM

UART port

WAKE UP

EXTERNAL SERIAL FLASH

A/D D/A

SPI ENABLE

KBMX

CLOCK

Platform | Intel | AMD
R319,R318 | 10KΩ | NA

Platform | Intel | AMD
R315 | 330Ω | 0Ω

noise cap

For Intel platform

Phase_ID	B	A	C / D
R337	10K_short	10K_short	10K_open
R322	10K_open	10K_short	10K_short
	3V	1.5V	0V

GPU_ID	G2	G1	G0
R343	10K_short	10K_open	10K_short
R338	10K_open	10K_short	10K_short

KEYBOARD_ID	RGB	BL
R392	MOUNT	OPEN
R393	OPEN	MOUNT

ACES_50696_0100M_001_10P
6012B0430403

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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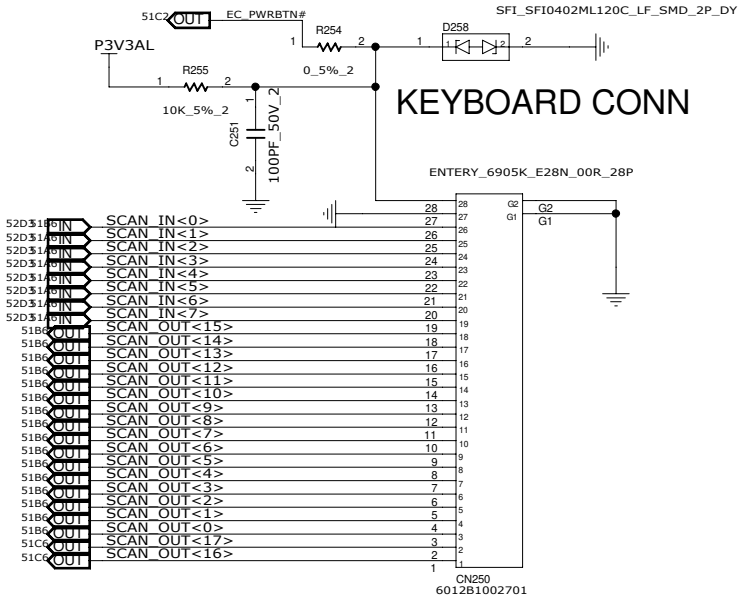
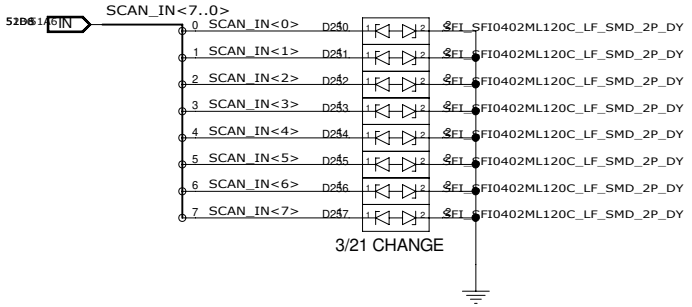
REFERENCE 200~249(POWER CONN)
REFERENCE 250~299(KB/TP CONN)



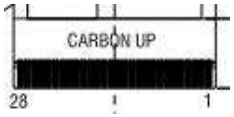
KEYBOARD CONN

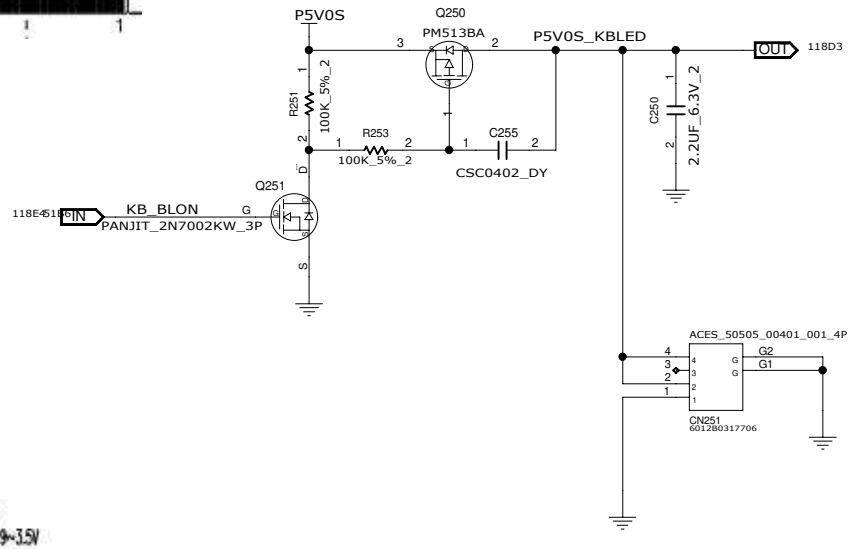
NEE TO CHANGE 6012B1002701
5/2 REVERSE

	14"
1	NC
2	NC
3	C08
4	C07
5	C06
6	C05
7	C04
8	C03
9	C02
10	C01
11	R16
12	R15
13	R14
14	R13
15	R12
16	R11
17	R10
18	R09
19	R08
20	R07
21	R06
22	R05
23	R04
24	R03
25	R02
26	R01
27	R18
28	R17



3/21 CHANGE





KEYBOARD LED CONN

VCC : +5V
LED Vf : 2.9~3.5V

	Min(LED Vf : 3.5V)	Max(LED Vf : 2.9V)
Power consumption	228.71mA	320.2mA

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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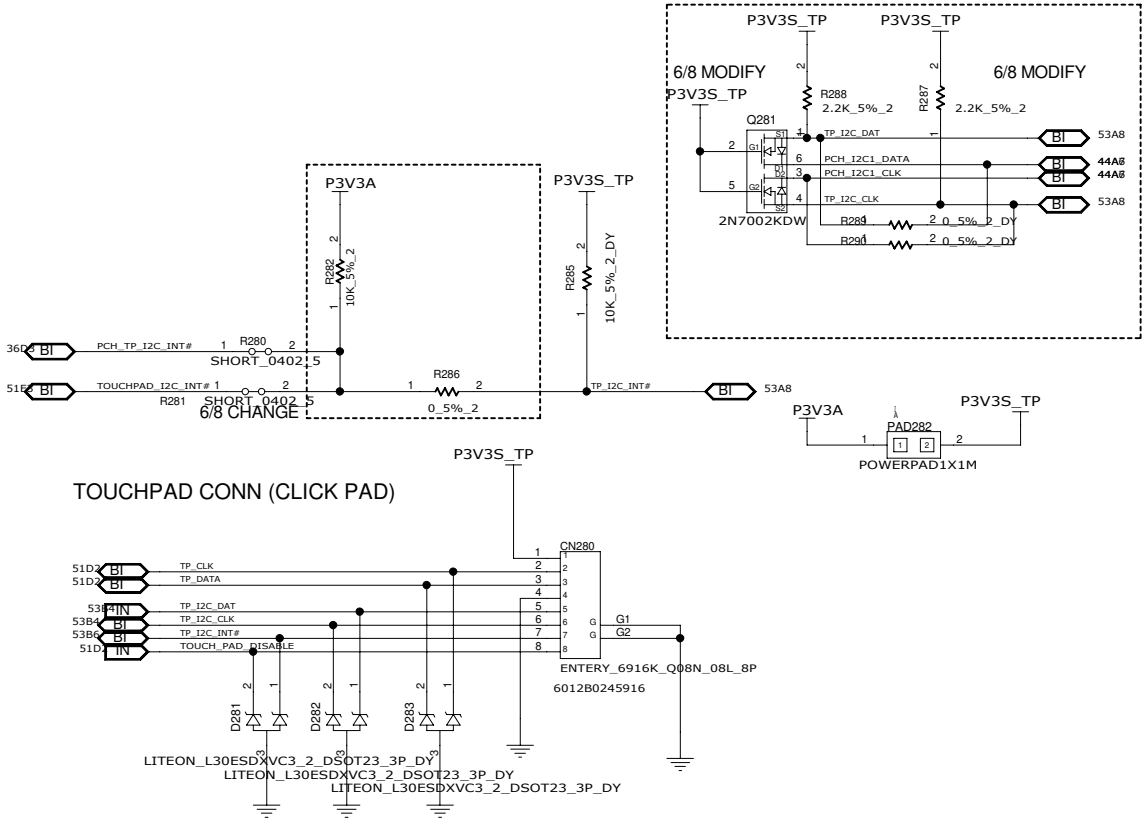


CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

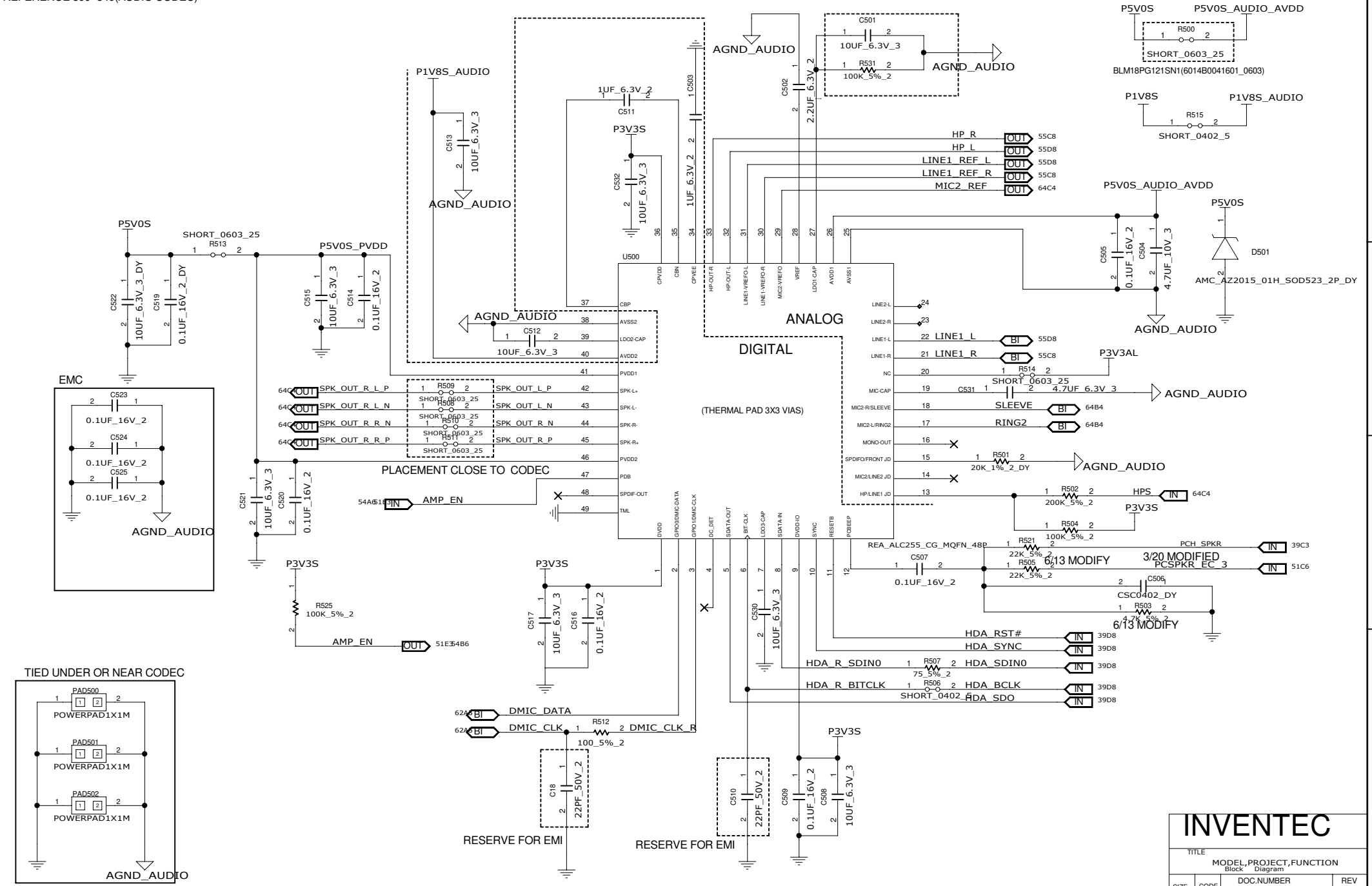
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 53 of 139

REFERENCE 500~549(AUDIO CODEC)



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

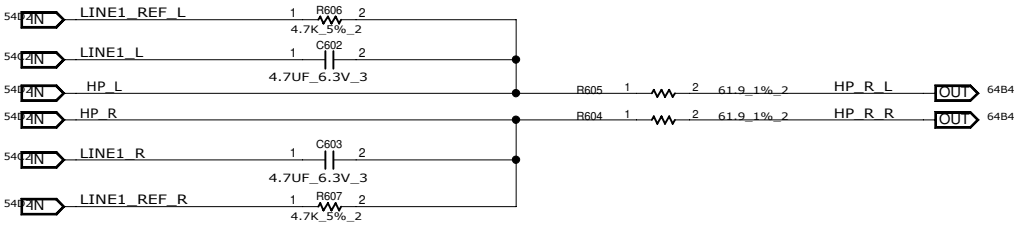
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 54 of 139

REFERCE 600~649(JACK/MIC/SPEAKER)

AUDIO JACKS



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

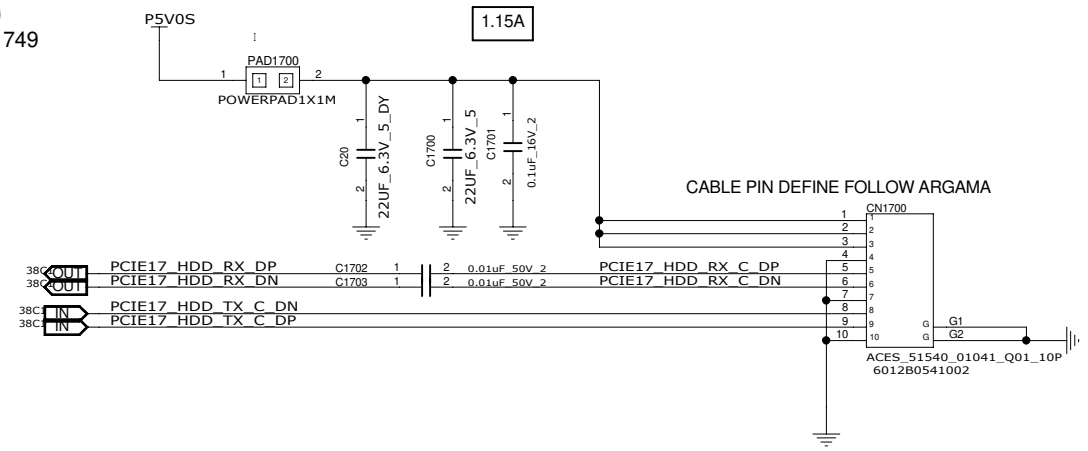
TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 55 of 139

SATA HDD CABLE CONN on MB

SATA HDD
Location 1700 ~ 1749



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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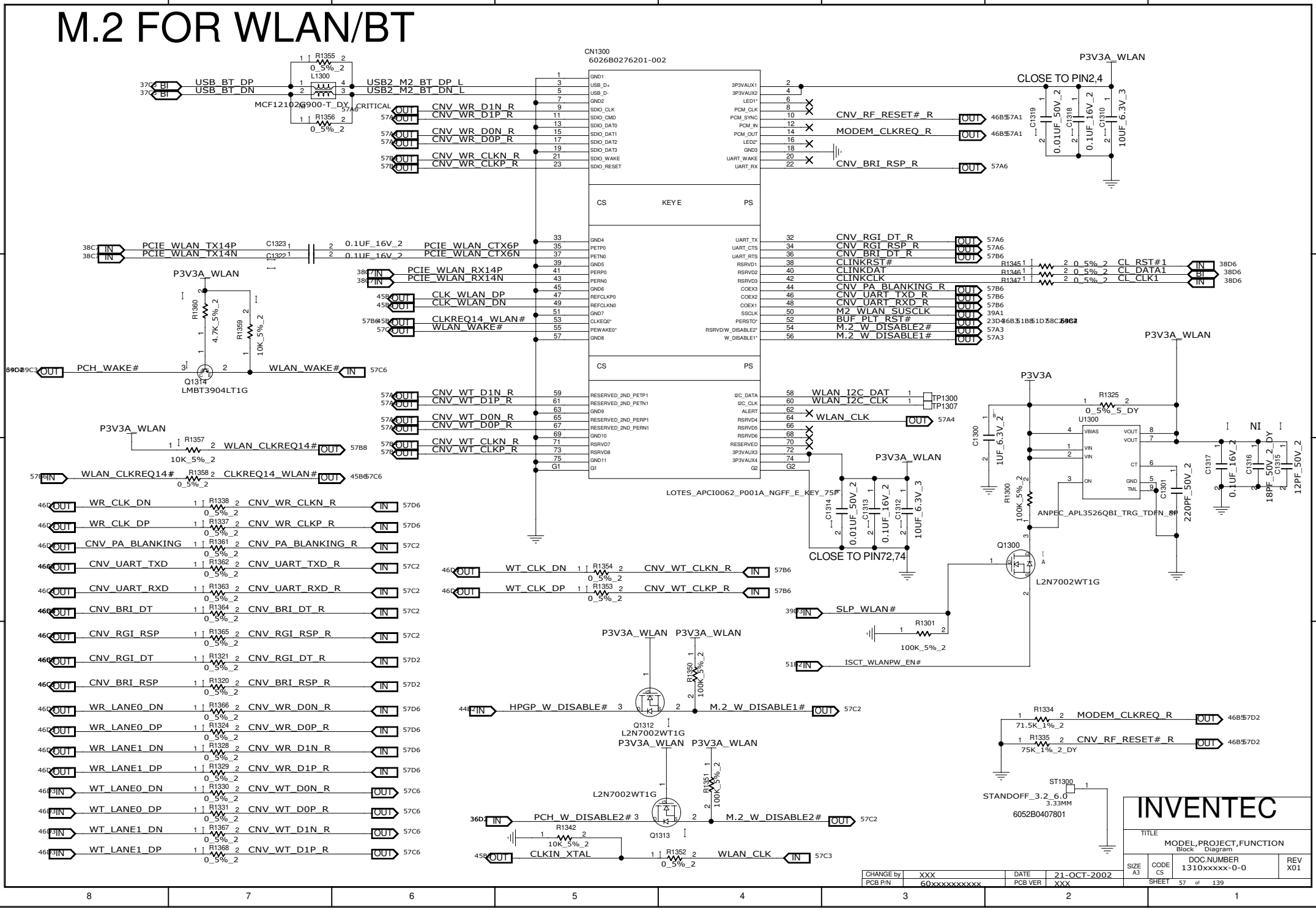
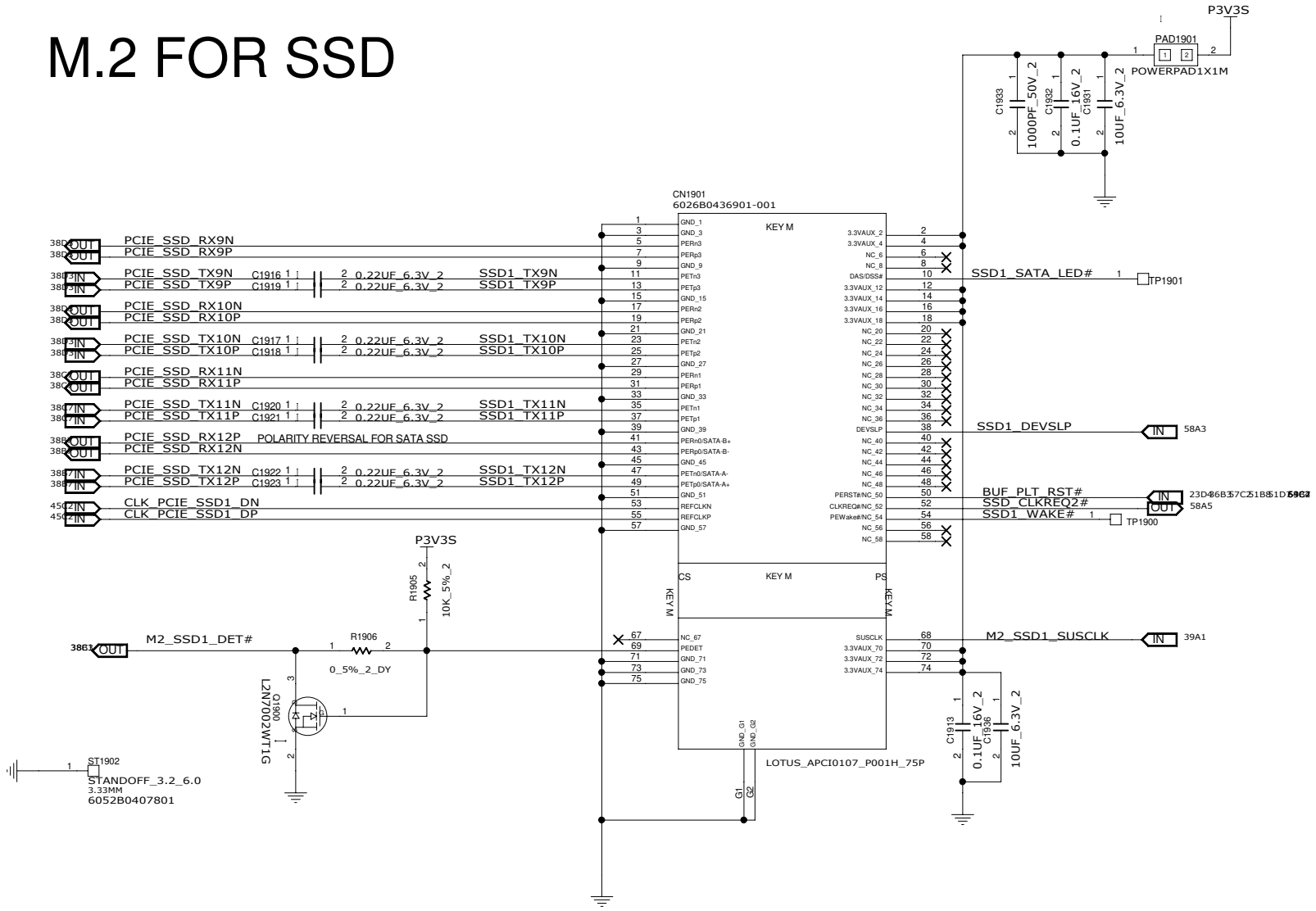
M.2 FOR WLAN/BT



M.2 FOR SSD



CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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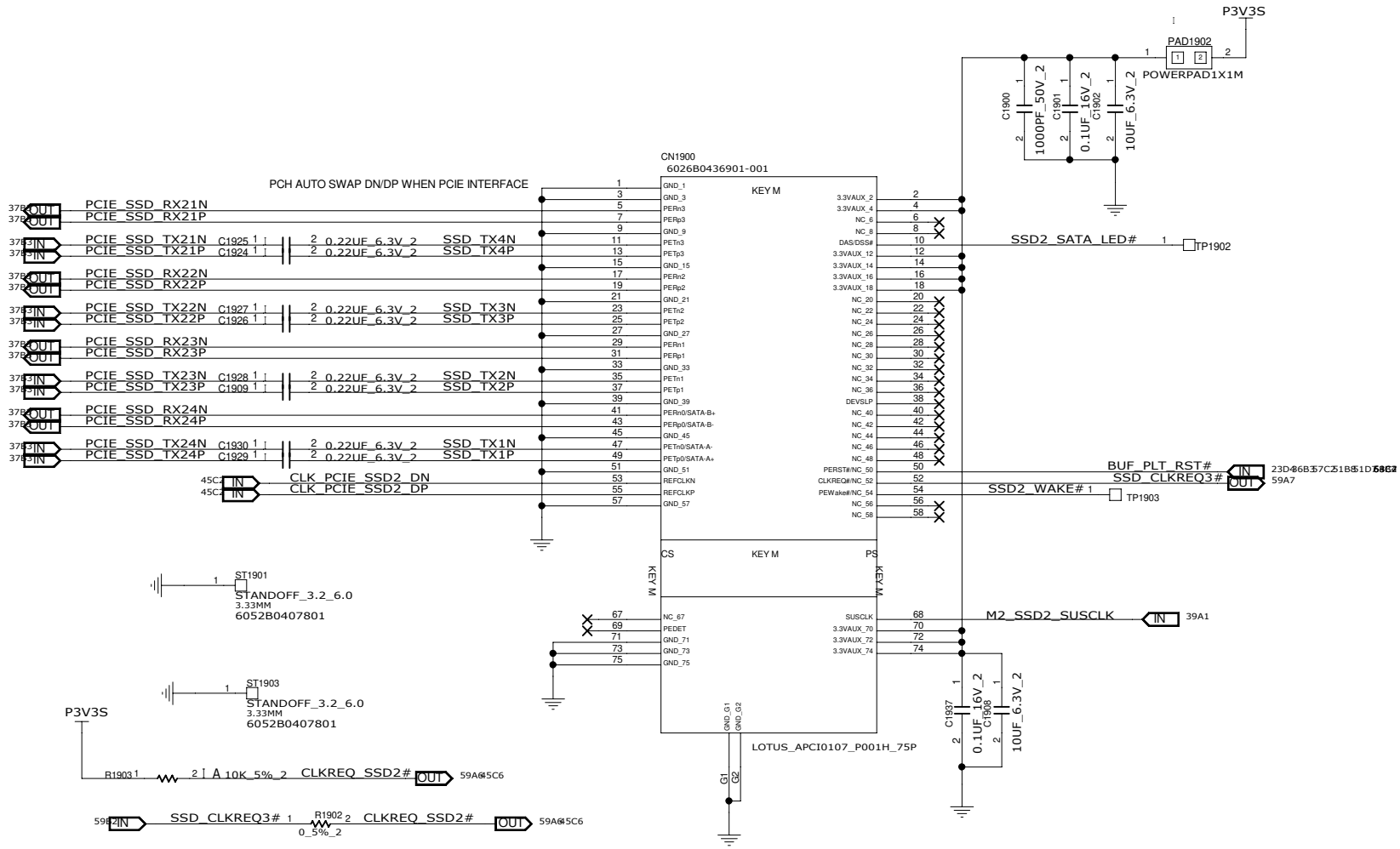
NGFF SSD2(PCIE/SATA 2X)



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

REFERENCE NUMBER:1950~1999

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
SATA HDD CONN.

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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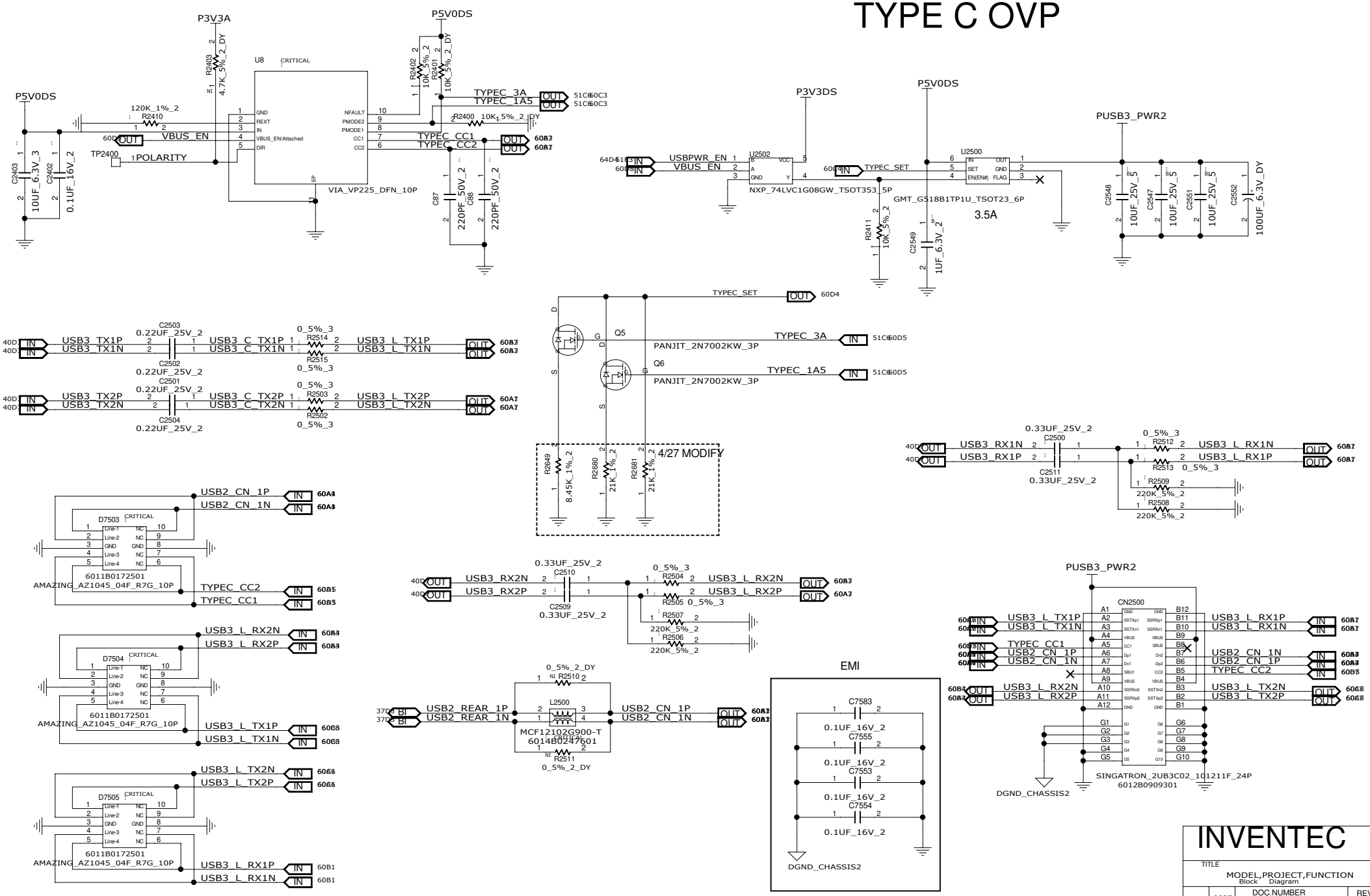
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

TYPE C OVP



CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	cs	1310xxxxx-0-0	X01

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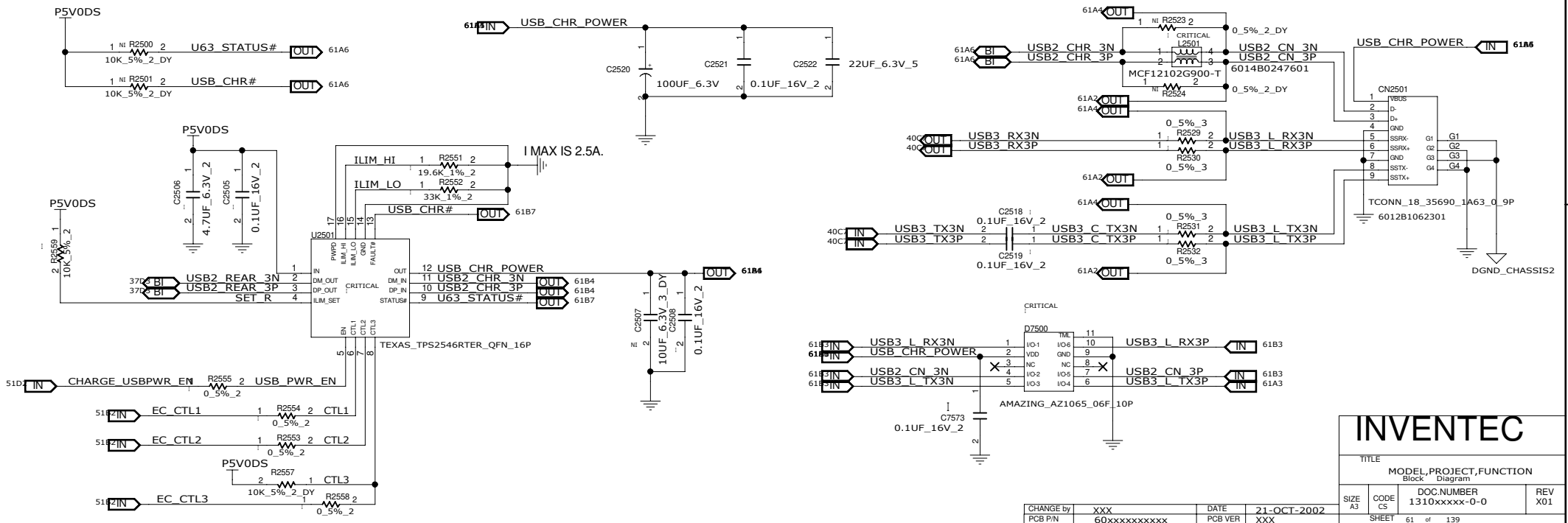
USB CHARGER

USB Faster Charger in S4/S5	USB Charger controller: TI2546	Ctrl-Pin (CTL1/CTL2/CTL3/ILIM_SEL)	Mode	ILIM	Note
Enable	S0	1/1/1/1	CDP	ILIM=2510mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
Disable	S0	1/1/1/1	CDP	ILIM=1525mA	w/ Data lines connected w/ USB charger
	S3	0/1/1/1	DCP	ILIM=2510mA	w/ Data lines disconnected and load detect function active w/ USB charger
	S4/S5	0/0/0/0	Turn off switch	ILIM=1525mA	No support charger



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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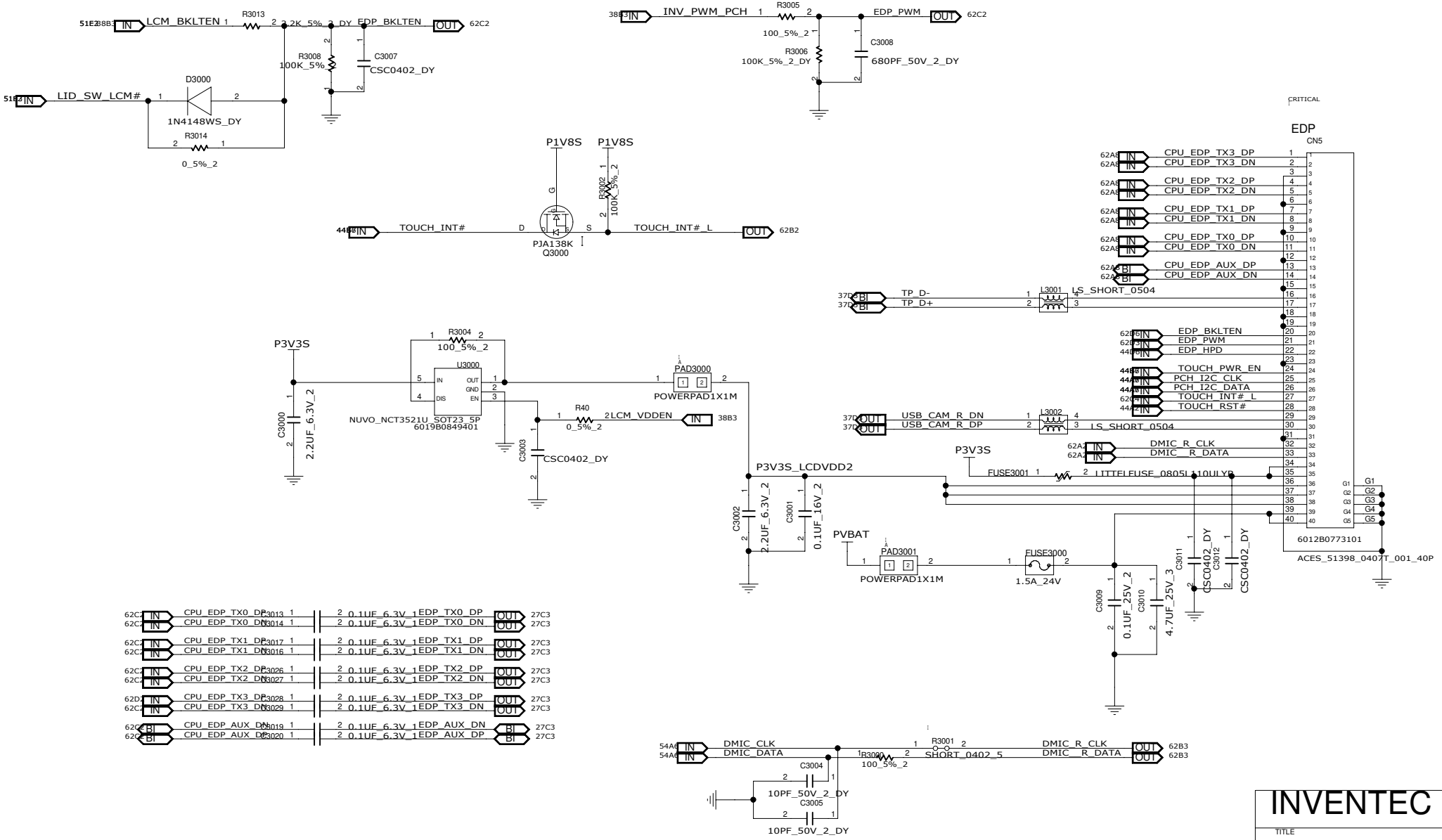
REFFERENCE 3000~3049(LCM)

EDP CONN



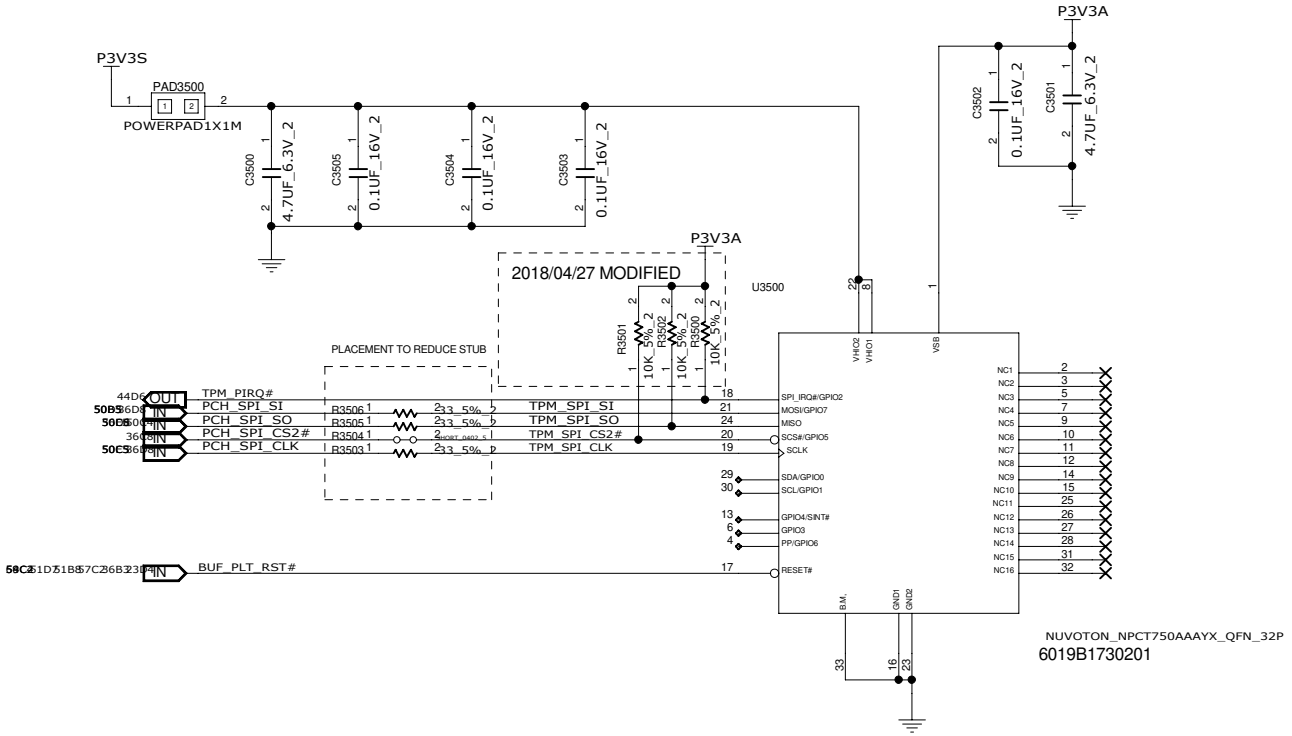
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 62 of 139



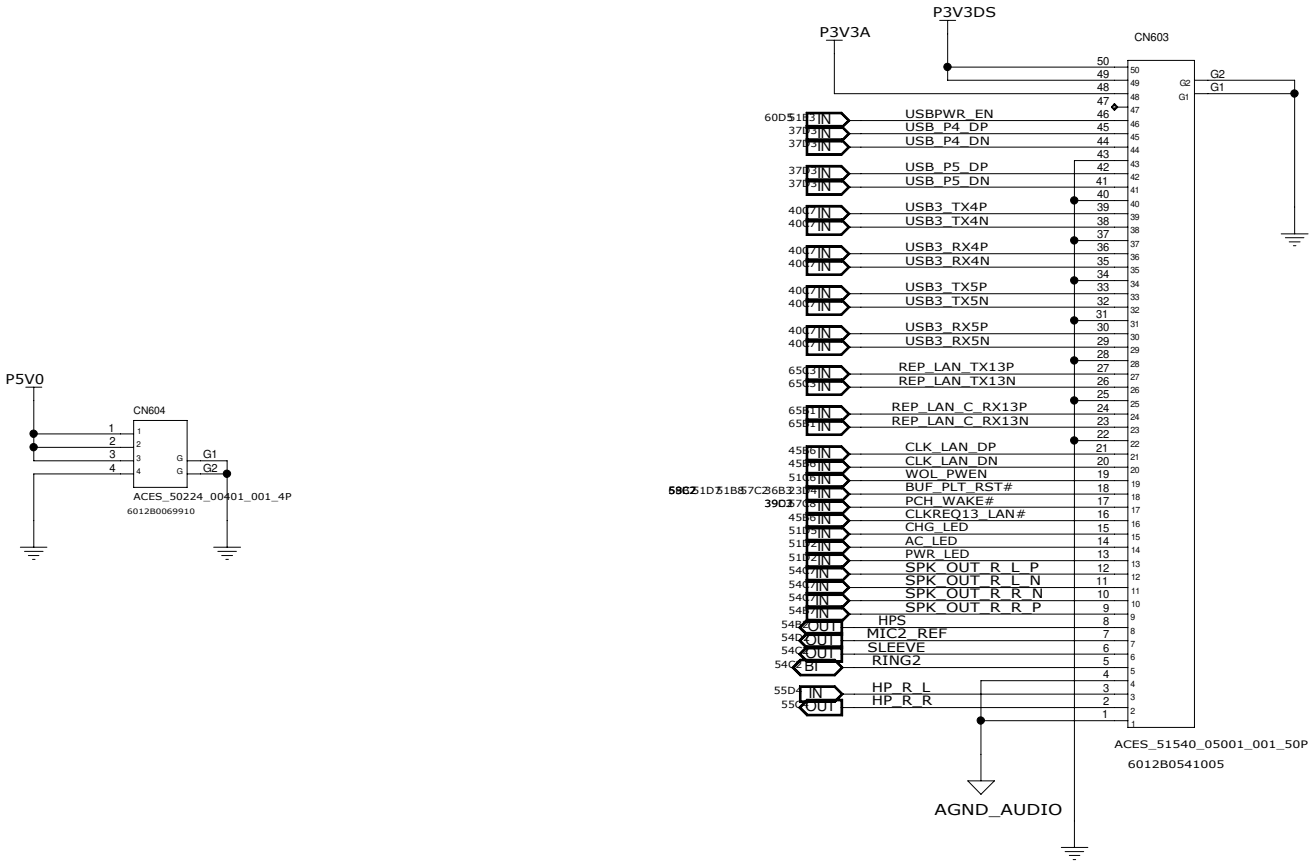
CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 63 of 139



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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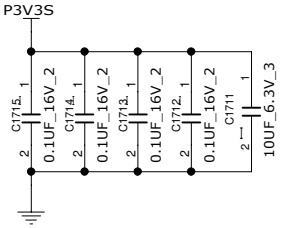
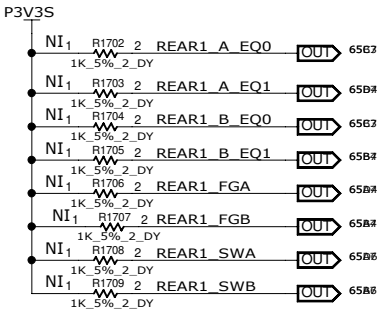
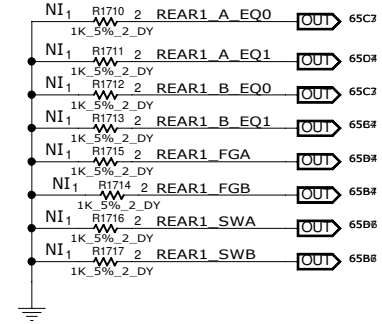
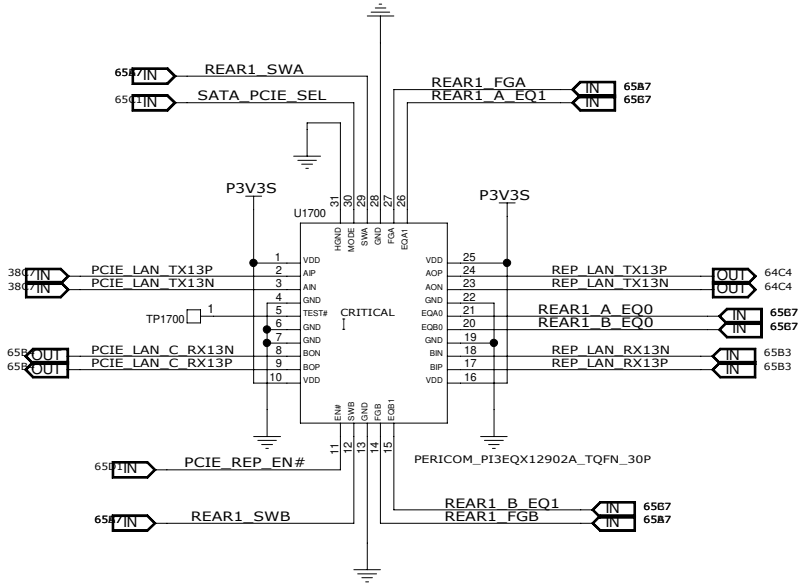
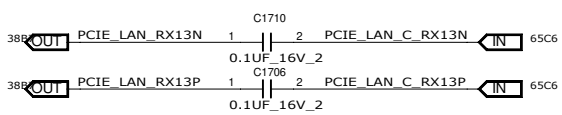
PCIE REPEATER

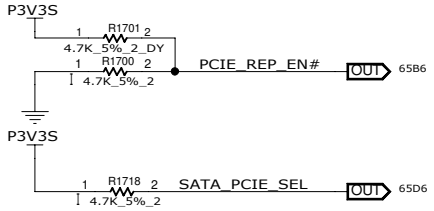


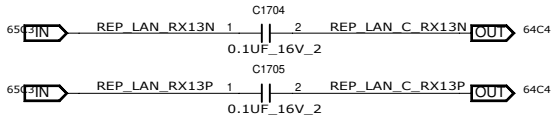












INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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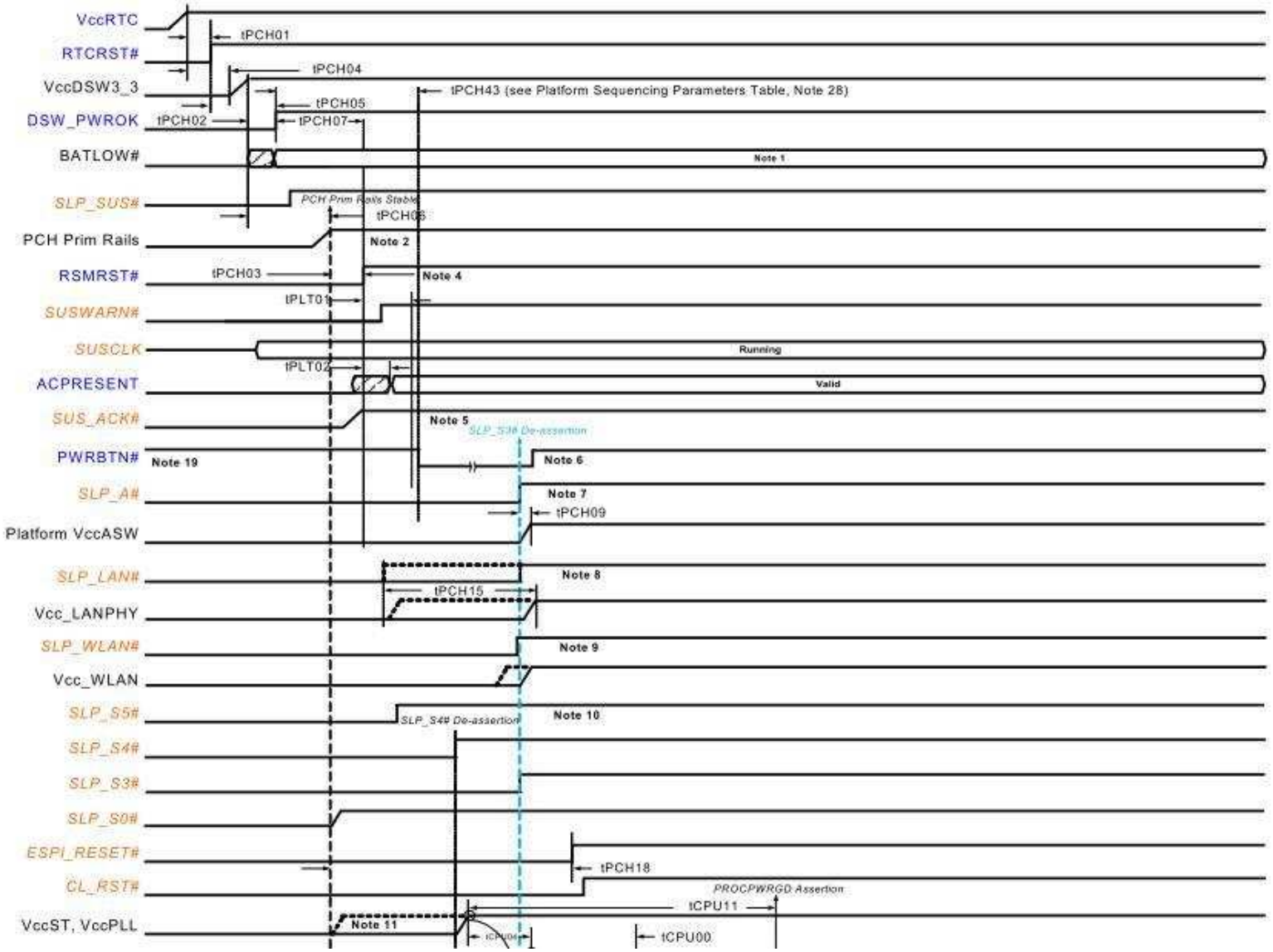
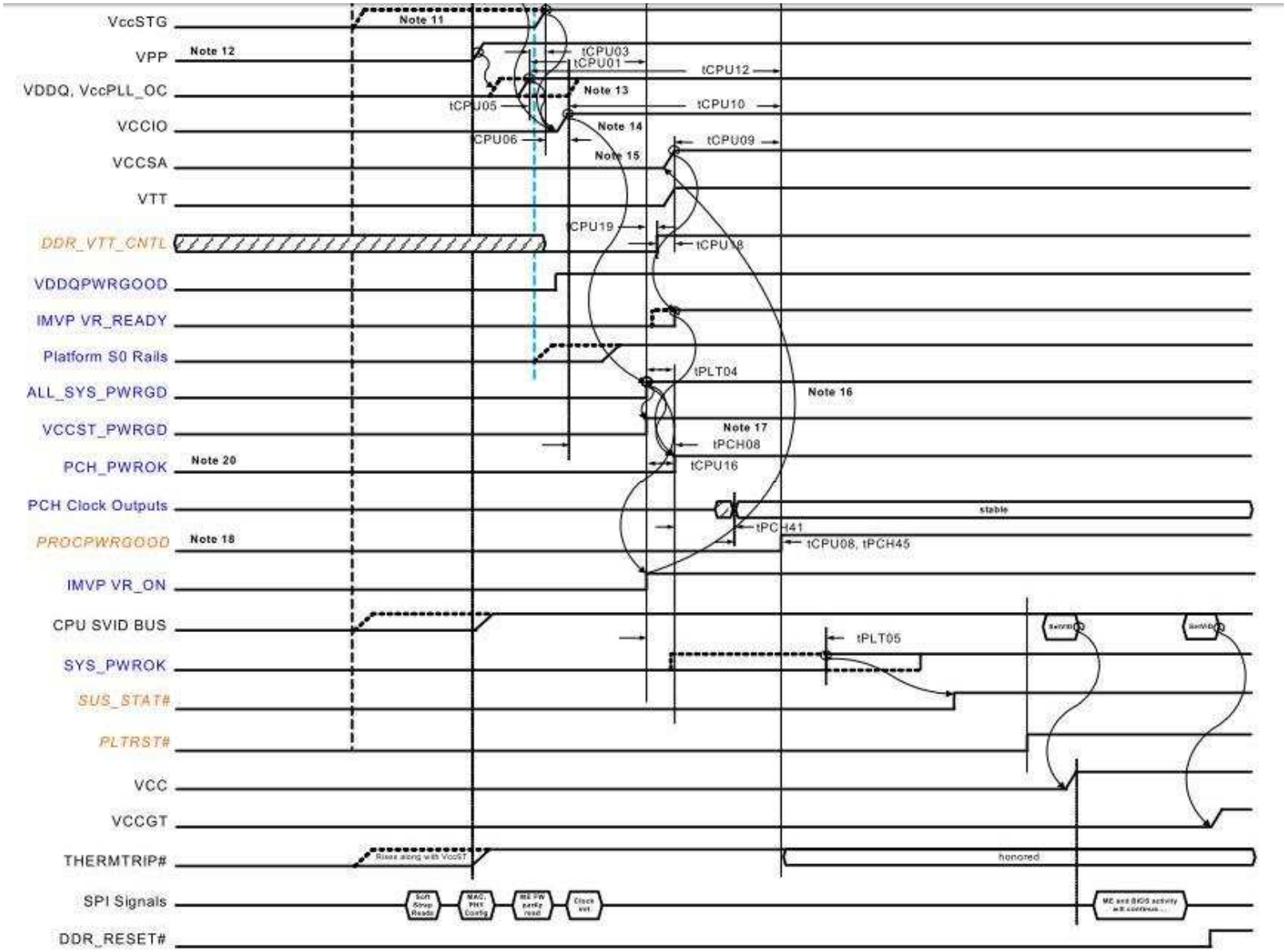


INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram				
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0			REV X01
SHEET 66 of 139					
CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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N18E-G0
N18E-G1
N18E-G2 MAX-Q

8GB DDR5 256M X 16 X 2 X6

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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PCA CODE NAME： N18E-G0/G1/G2 MAX-Q

G0 : 6019B1850001
G1 : 6019B1849201
G2 MAXQ:6019B1849301

PCB VERSION：X01
BOARD SIZE:

SCH P/N:
PCB P/N:
PCA P/N:

BOM ATTRIBUTE TRUTH TABLE

I: INSTALL
NI: NON-INSTALL
DY: NON-INSTALL
MP: PRODUCTION
PROTO: PRE-PRODUCTION
CRITICAL: CRITICAL PART

PVCORE_DGPU = NVVDD

P1V35 S_DGPU= FBVDD

P1V0S_DGPU = PEX_VDD

SAMSUNG K4Z80325BC-HC14
6019B1847601

MICRON MT61K256M32JE-14:A
6019B1847701

INVENTEC

TITLE: MODEL, PROJECT, FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CONNECTION TO MAINBOARD

CLK_PCIE_DGPU_100MHZ_P
CLK_PCIE_DGPU_100MHZ_N
PCIE_DGPU_RX15P
PCIE_DGPU_RX15N
PCIE_DGPU_TX15P
PCIE_DGPU_TX15N
PCIE_DGPU_RX14P
PCIE_DGPU_RX14N
PCIE_DGPU_TX14P
PCIE_DGPU_TX14N
PCIE_DGPU_RX13P
PCIE_DGPU_RX13N
PCIE_DGPU_TX13P
PCIE_DGPU_TX13N
PCIE_DGPU_RX12P
PCIE_DGPU_RX12N
PCIE_DGPU_TX12P
PCIE_DGPU_TX12N
PCIE_DGPU_RX11P
PCIE_DGPU_RX11N
PCIE_DGPU_TX11P
PCIE_DGPU_TX11N
PCIE_DGPU_RX10P
PCIE_DGPU_RX10N
PCIE_DGPU_TX10P
PCIE_DGPU_TX10N
PCIE_DGPU_RX9P
PCIE_DGPU_RX9N
PCIE_DGPU_TX9P
PCIE_DGPU_TX9N
PCIE_DGPU_RX8P
PCIE_DGPU_RX8N
PCIE_DGPU_TX8P
PCIE_DGPU_TX8N
PCIE_DGPU_RX7P
PCIE_DGPU_RX7N
PCIE_DGPU_TX7P
PCIE_DGPU_TX7N
PCIE_DGPU_RX6P
PCIE_DGPU_RX6N
PCIE_DGPU_TX6P
PCIE_DGPU_TX6N
PCIE_DGPU_RX5P
PCIE_DGPU_RX5N
PCIE_DGPU_TX5P
PCIE_DGPU_TX5N
PCIE_DGPU_RX4P
PCIE_DGPU_RX4N
PCIE_DGPU_TX4P
PCIE_DGPU_TX4N
PCIE_DGPU_RX3P
PCIE_DGPU_RX3N
PCIE_DGPU_TX3P
PCIE_DGPU_TX3N
PCIE_DGPU_RX2P
PCIE_DGPU_RX2N
PCIE_DGPU_TX2P
PCIE_DGPU_TX2N
PCIE_DGPU_RX1P
PCIE_DGPU_RX1N
PCIE_DGPU_TX1P
PCIE_DGPU_TX1N
PCIE_DGPU_RX0P
PCIE_DGPU_RX0N
PCIE_DGPU_TX0P
PCIE_DGPU_TX0N

DGPU_PWR_EN

GPU PWR ENABLE COME FROM PCH/EC
MAKE SURE 10K P3V3S PULL UP

PCH_PLTRST#_BUF

PCH PLATFORM RESET#
MAKE SURE 100K PULL TO GND

IRMT_HOLD_RST#

PCH HOLD RESET#
MAKE SURE 100K PULL TO GND

TO PCH

GPU_EVENT_PCH#

PCH INFORM GPU WILL EXIT GC6 MODS

DGPU_PWRLEVEL

15.3.2 PWR_LEVEL* (GPIO12)

The POWER_LEVEL input signal triggers an immediate GPU hardware slow-down, followed by the driver capping the GPU power state to the appropriate limit. There are two events that can trigger this signal assertion: AC to battery power transition or total system power overdraw event.

PEX_CLKREQ#

PCIE CLK REQUESTD#

ALL_POWER_GOOD

GPU ALL S RAIL GOOD
MAKE SURE 10K P3V3S PULL UP

DP_MA_HPD#

DP HPD TO MAINBOARD
MAKE SURE 10K P3V3S PULL UP

SMB0_DATA_D
SMB0_CLK_D

DP REDRIVER I2C CONNECT TO MOBARD
MAINBOARD NEED TO PULL UP

HDMI_MB_HPD#

HDMI HPD TO MB

SMB0_DATA_D
SMB0_CLK_D

HDMI RETIMER I2C TO MB
MAINBOARD NEED TO PULL UP

GPU_OVERT_EC#

3.3V LEVEL
OVER TEMPERATURE TO PCH OR EC

GC6_FB_EN_PCH

3.3V LEVEL
GC6 ENABLE SIGNAL TO PCH OR EC

EC

EC_SMBDATA0
EC_SMBCLK0

GPU I2C, COMMUNCATED WITH EC
THIS SIGNAL REQUIRE AN EXTERNAL PULL UP

INVENTEC

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	DOC.NUMBER 1310xxxxx-0-0
PCB P/N	60xxxxxxxxx	PCB VER	XXX	CODE CS	REV X01

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

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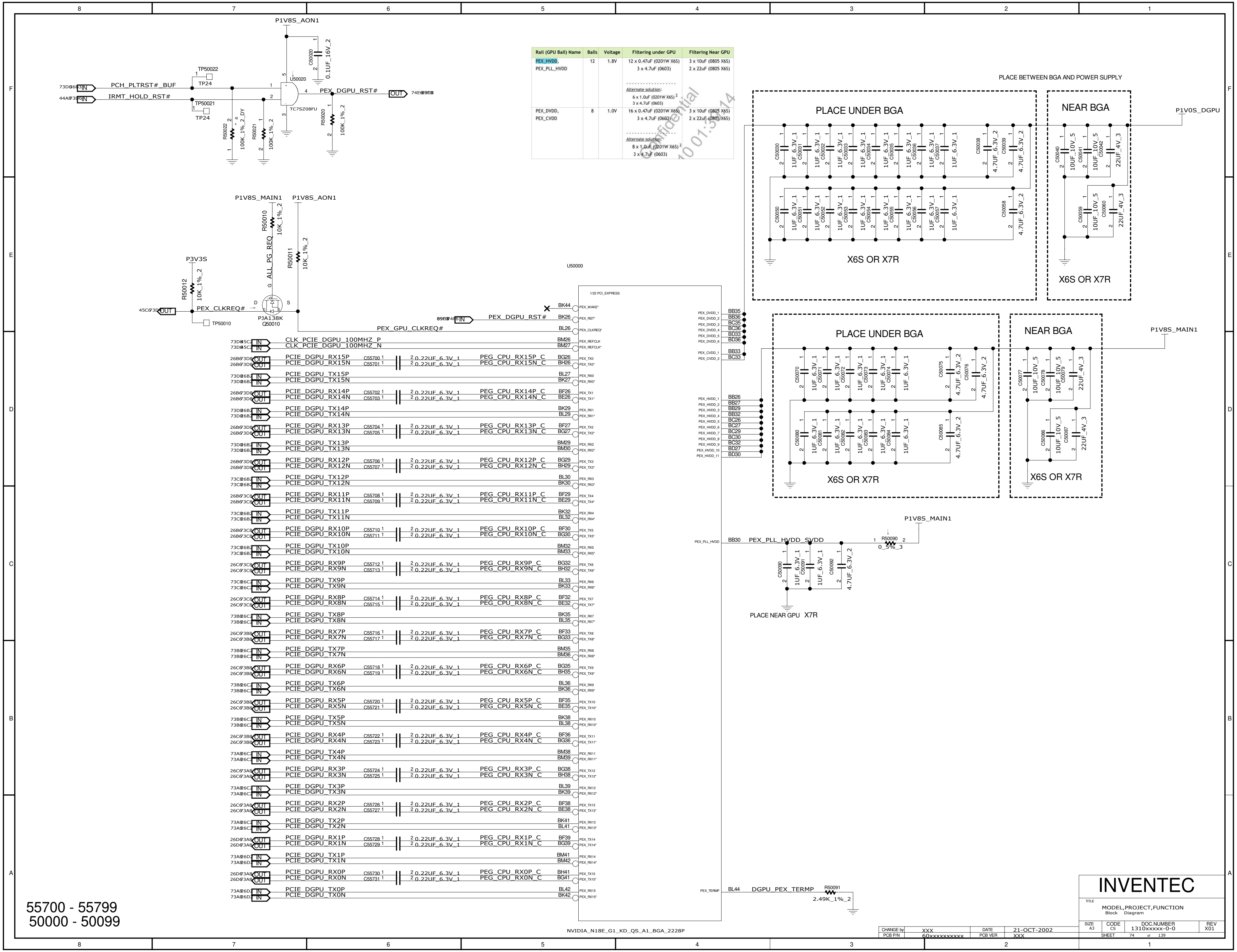

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD, PEX_PLL_HVDD	12	1.8V	12 x 0.47uF (0201W X6S) 3 x 4.7uF (0603) - - - - - - - - - - - - - - - - - - - Alternate solution: 6 x 1.0uF (0201W X6S) 2 3 x 4.7uF (0603)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)
PEX_DVDD, PEX_CVDD	8	1.0V	16 x 0.47uF (0201W X6S) 3 x 4.7uF (0603) - - - - - - - - - - - - - - - - - - - Alternate solution: 8 x 1.0uF (0201W X6S) 2 3 x 4.7uF (0603)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)

INVENTEC

TITLE MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by XXX | DATE 21-OCT-2002
PCB P/N 60xxxxxxxxxx | PCB VER XXX

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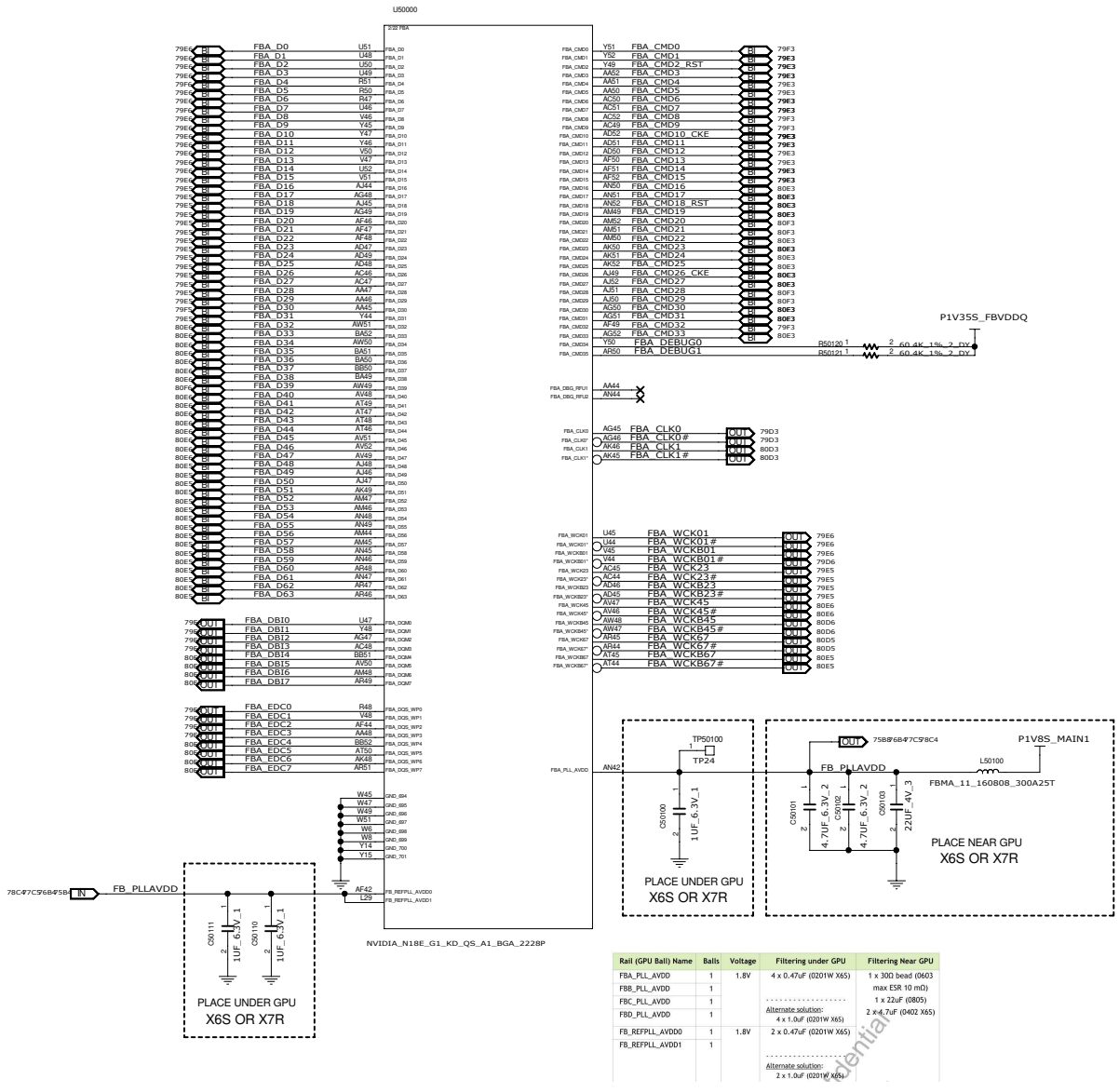
GPU FRAME BUFFER A

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603
FBB_PLL_AVDD	1			max ESR 10 mΩ)
FBC_PLL_AVDD	1		- - - - - - - - - - - - - - - - -	1 x 22uF (0805)
FBD_PLL_AVDD	1		Alternate solution:	2 x 4.7uF (0402 X6S)
			4 x 1.0uF (0201W X6S)	
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1			
			- - - - - - - - - - - - - - - - -	
			Alternate solution:	
			2 x 1.0uF (0201W X6S)	



Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
FBA_PLL_AVDD	1	1.8V	4 x 0.47uF (0201W X6S)	1 x 30Ω bead (0603
FBB_PLL_AVDD	1			max ESR 10 mΩ)
FBC_PLL_AVDD	1		- - - - - - - - - - - - - - - - -	1 x 22uF (0805)
FBD_PLL_AVDD	1		Alternate solution:	2 x 4.7uF (0402 X6S)
			4 x 1.0uF (0201W X6S)	
FB_REFPLL_AVDD0	1	1.8V	2 x 0.47uF (0201W X6S)	
FB_REFPLL_AVDD1	1			
			- - - - - - - - - - - - - - - - -	
			Alternate solution:	
			2 x 1.0uF (0201W X6S)	

50100 - 50199

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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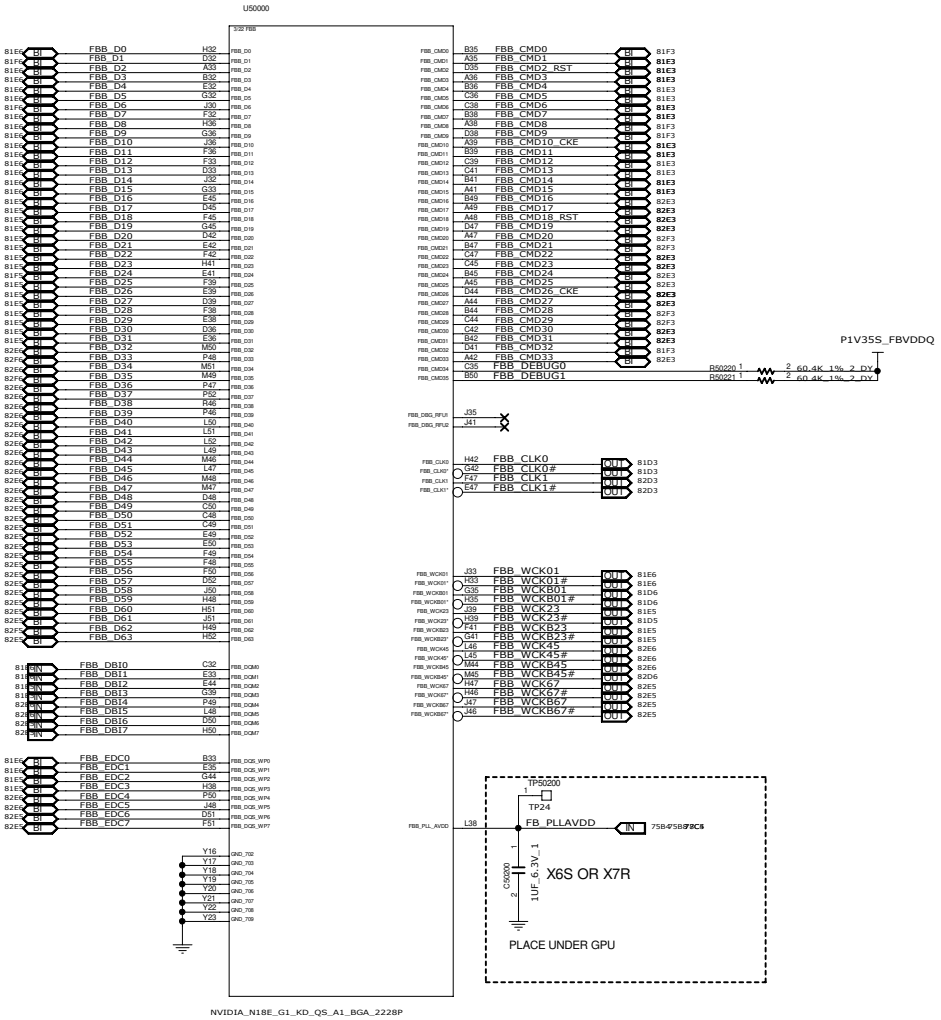
GPU FRAME BUFFER B



50200 - 50299

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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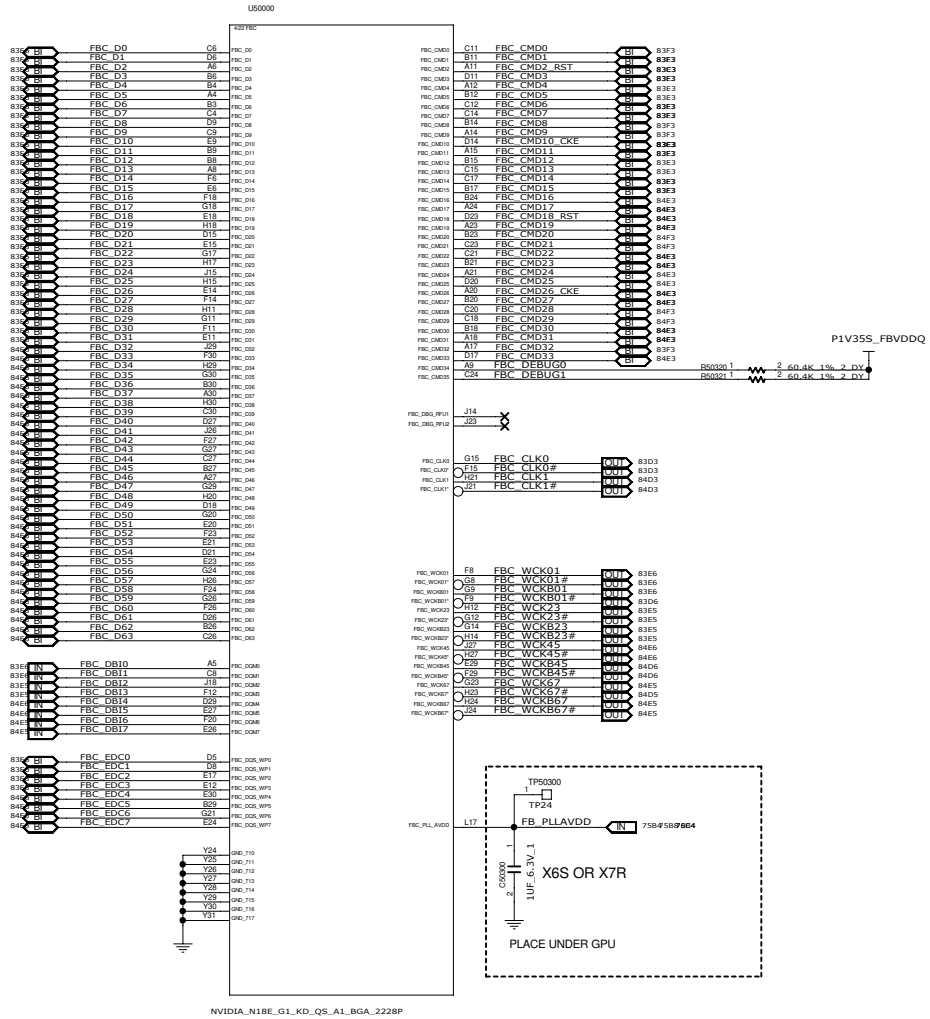
GPU FRAME BUFFER C



50300 - 50399

CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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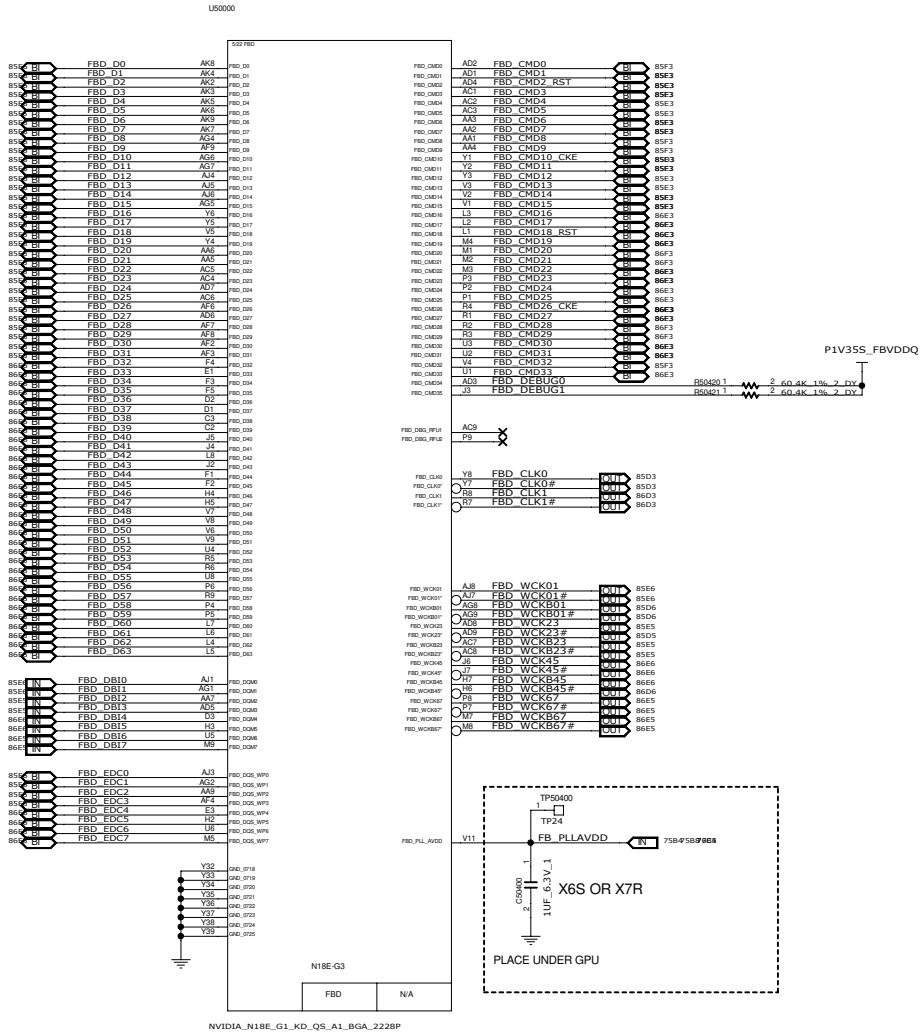
GPU FRAME BUFFER D



50400 - 50499

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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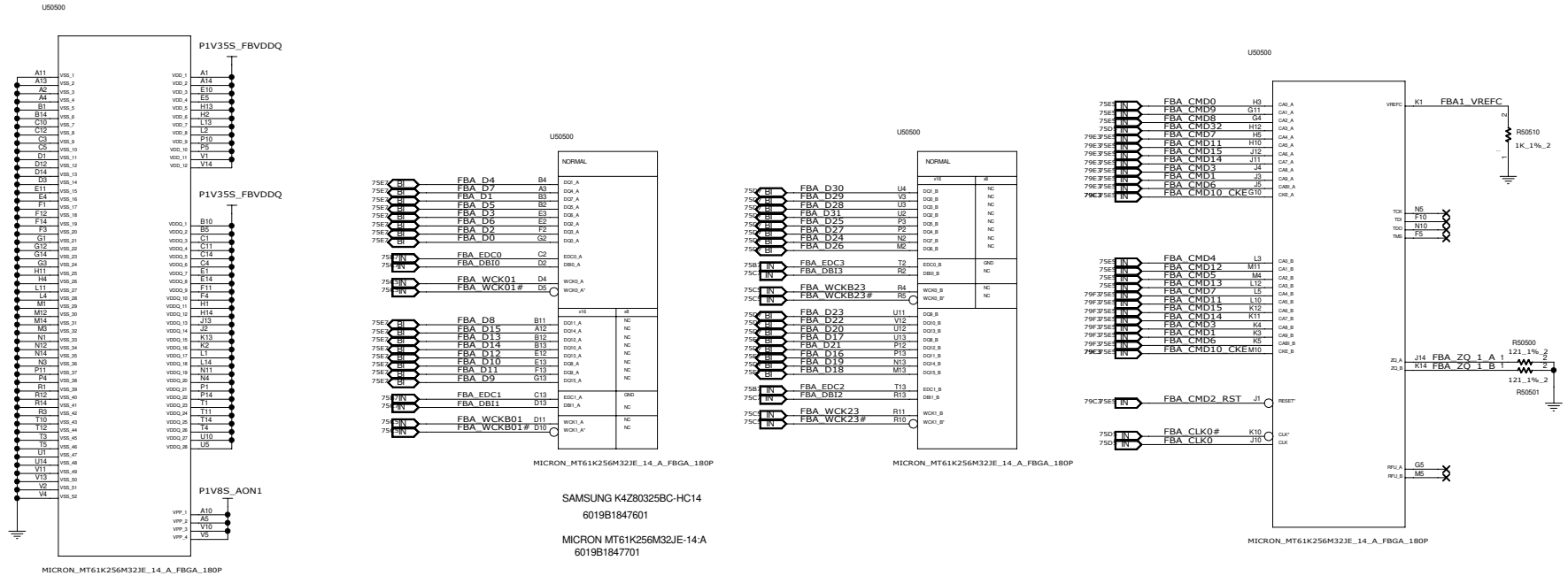

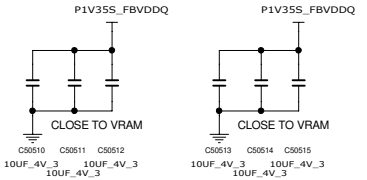

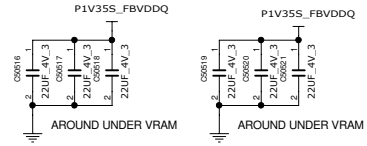

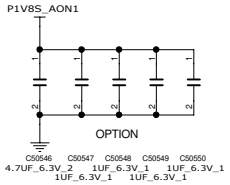

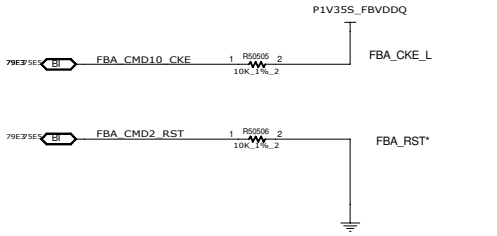

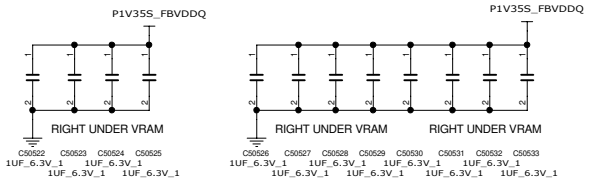

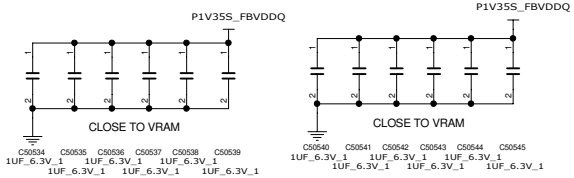

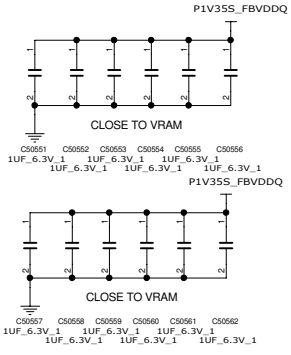

Table 8.12 DRAM-Side Decoupling

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type, [Size NOTE 1]	Quantity	Placement
VDD/VDDQ Rail			
0.47 uF NOTE 2	X6S [0201W]	36	Under or very close to DRAM
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Around DRAM
22 uF	X6S [0603]	6	
VPP Rail			
0.47 uF NOTE 3	X6S [0201W]	4	Under or very close to DRAM
4.7 uF	X6S [0603]	1	

NOTE 1: NVIDIA reference designs use and recommend 0201 or 0201W capacitors where needed. PCB design teams should ensure that component placement equipment can support the smaller package size.

NOTE 2: Alternatively, instead of using 36 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 18 capacitors of value 1.0 uF (X6S, 0201W).

NOTE 3: Alternatively, instead of using 4 capacitors of value 0.47uF (X6S, 0201W), Notebook designs may use 4 capacitors of value 1.0uF (X6S, 0201W), one per VPP ball.

50500 - 50599

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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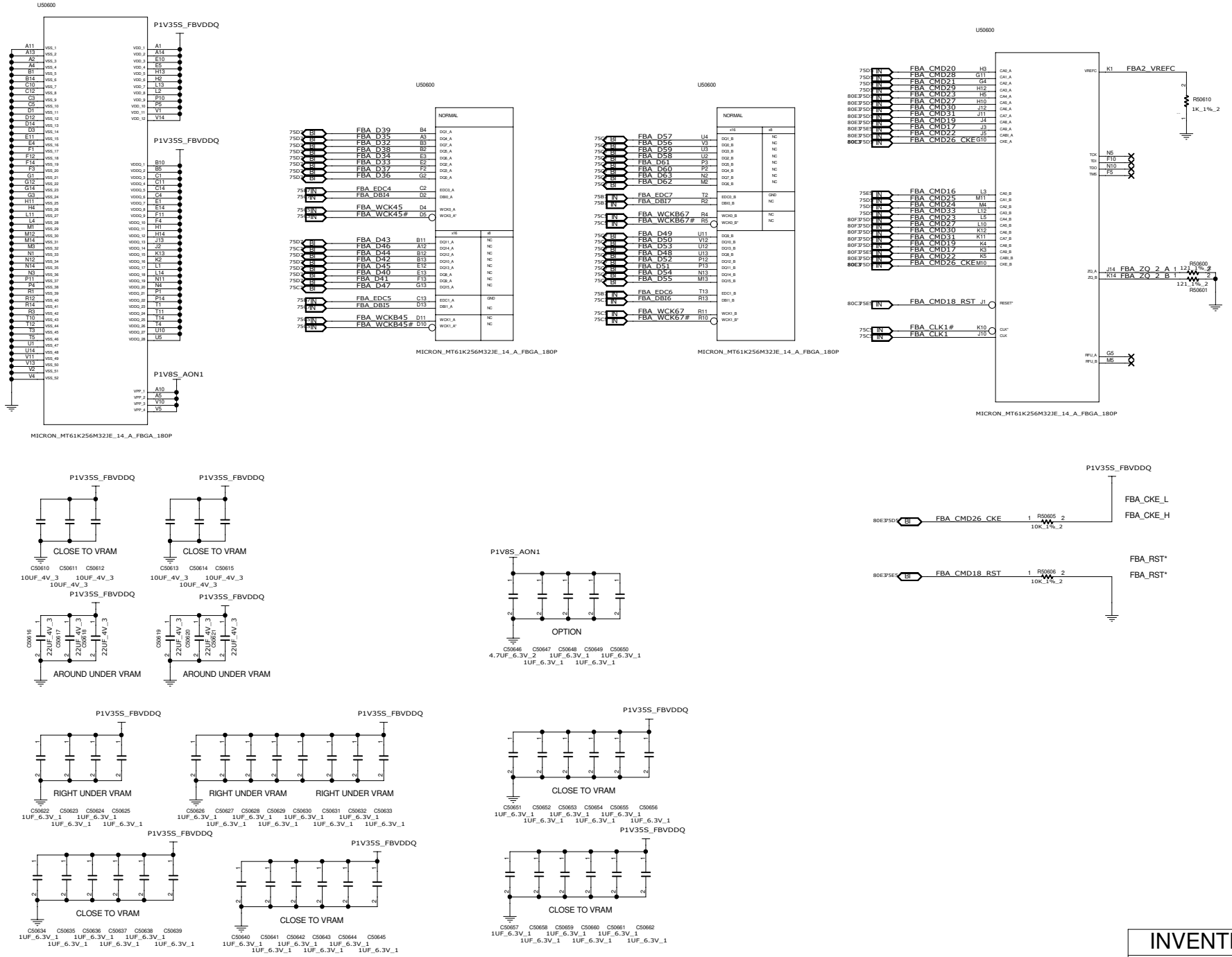
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



50600 - 50699

CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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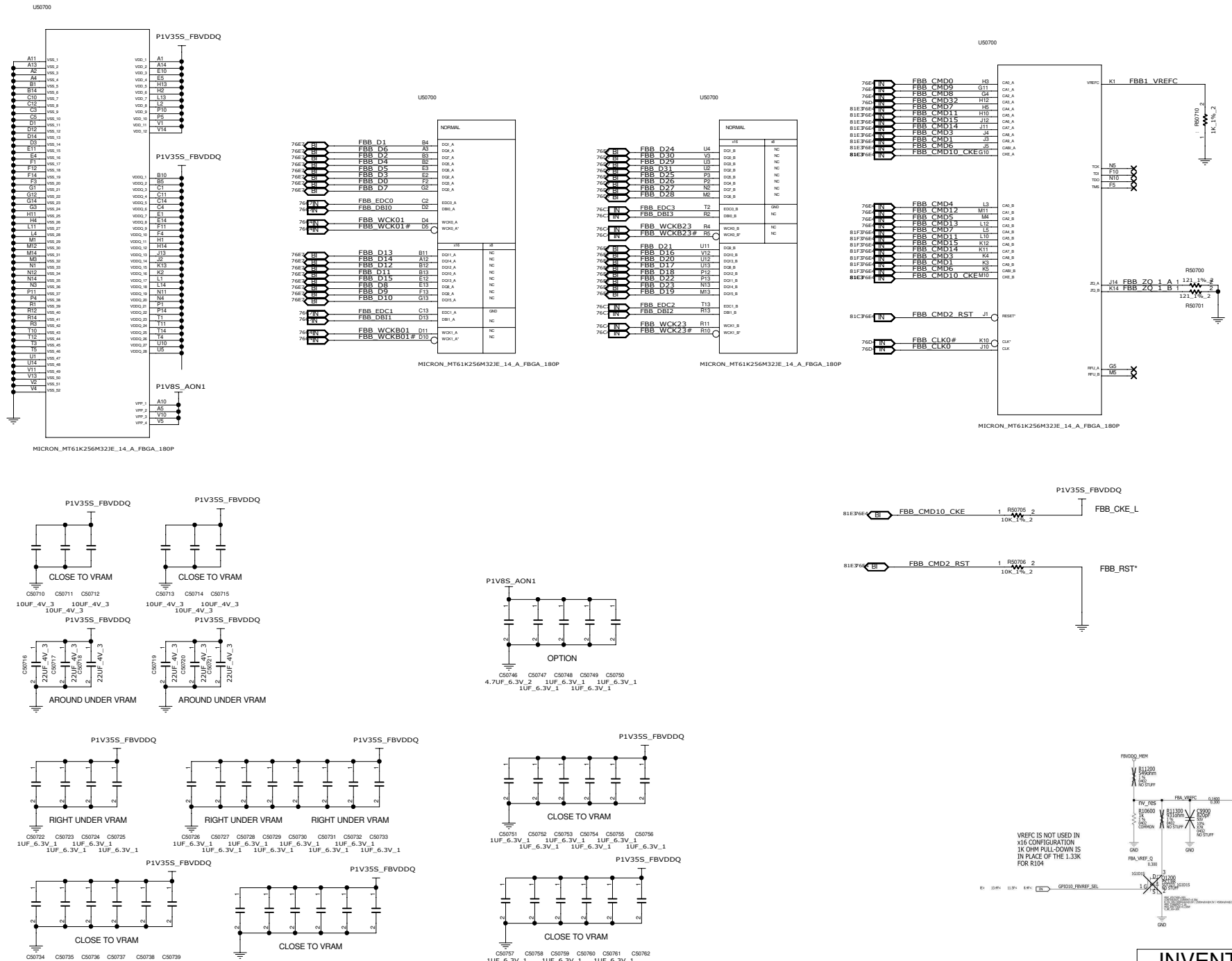
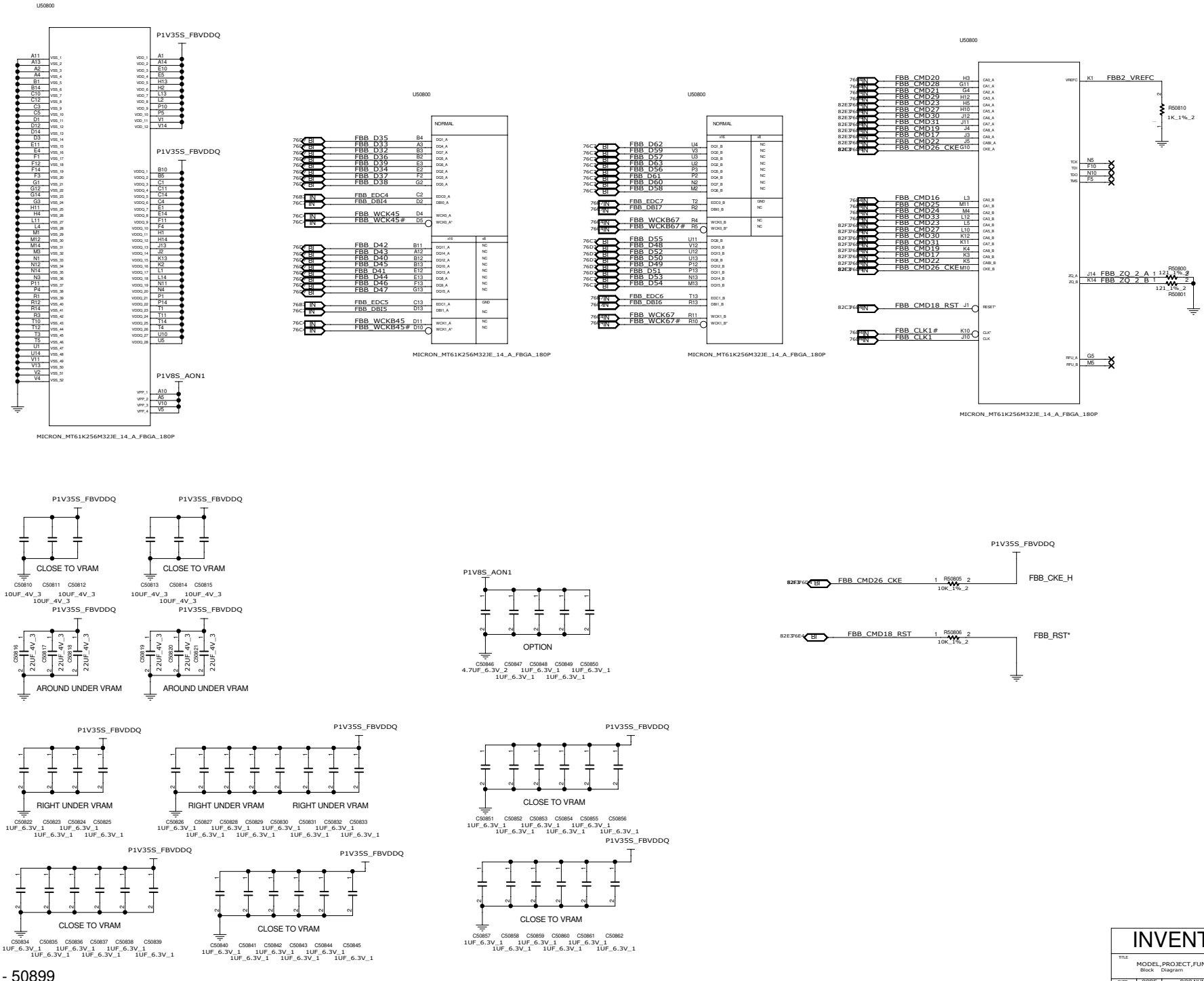


50700 - 50799

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE C5	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxx	PCB VER	XXX			SHEET B1 of 139	

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram



50800 - 50899

CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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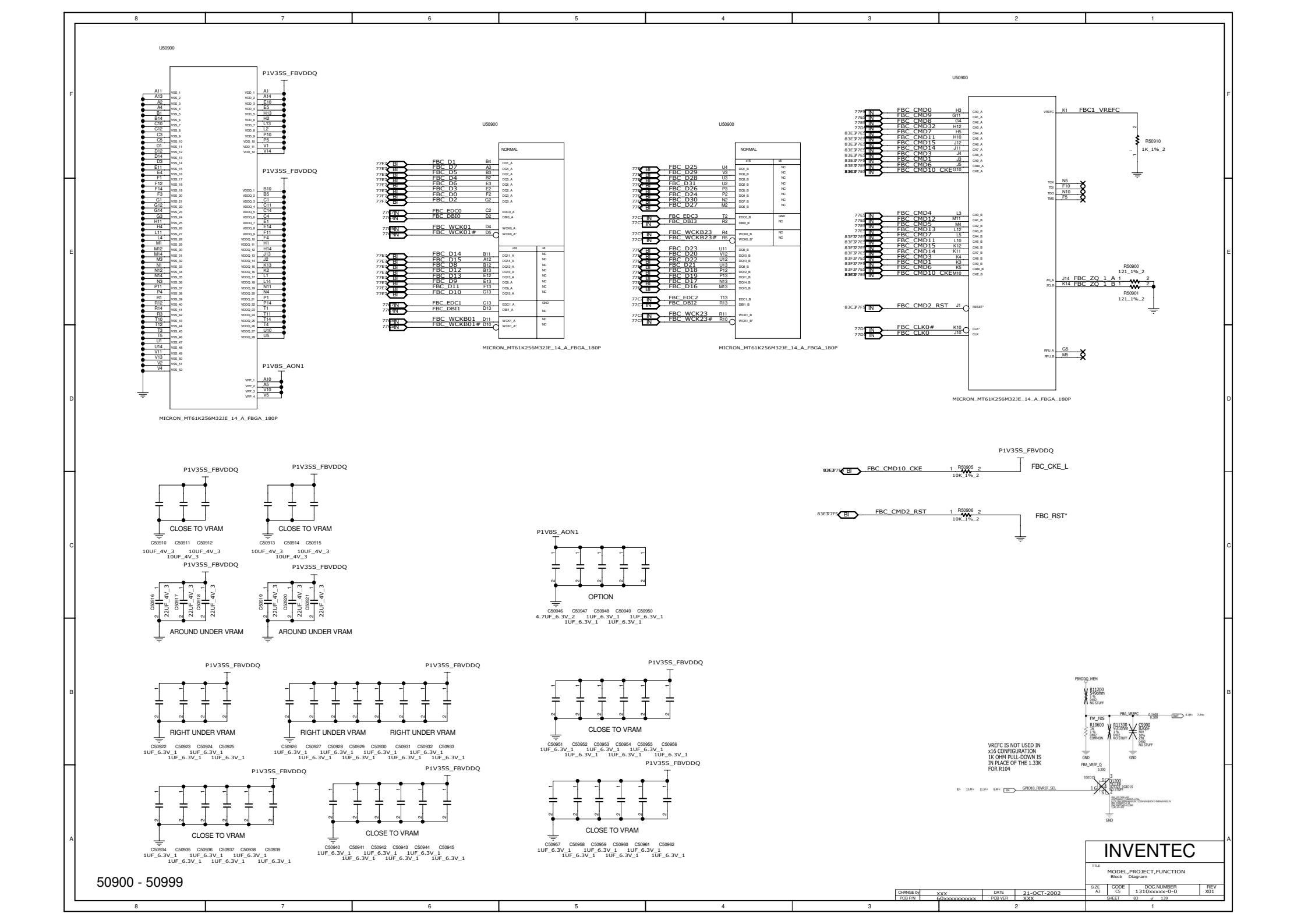
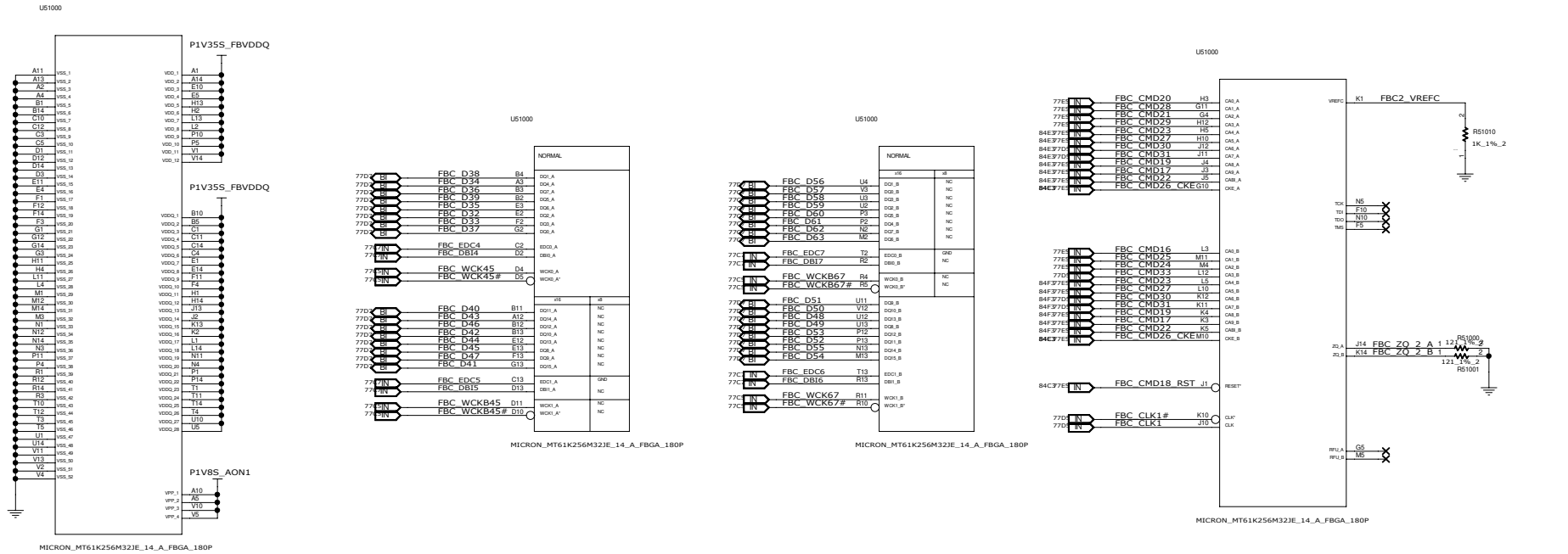

U50900
P1V35S_FBVDDQ
P1V8S_AON1
MICRON_MT61K256M32JE_14_A_FBGA_180P
FBC_D1
FBC_D7
FBC_D5
FBC_D4
FBC_D6
FBC_D3
FBC_D0
FBC_D2
FBC_EDC0
FBC_DBI0
FBC_WCK01
FBC_WCK01#
FBC_D14
FBC_D15
FBC_D8
FBC_D12
FBC_D13
FBC_D9
FBC_D11
FBC_D10
FBC_EDC1
FBC_DBI1
FBC_WCKB01
FBC_WCKB01#
FBC_D25
FBC_D29
FBC_D28
FBC_D31
FBC_D26
FBC_D24
FBC_D30
FBC_D27
FBC_EDC3
FBC_DBI3
FBC_WCKB23
FBC_WCKB23#
FBC_D23
FBC_D20
FBC_D22
FBC_D21
FBC_D18
FBC_D19
FBC_D17
FBC_D16
FBC_EDC2
FBC_DBI2
FBC_WCK23
FBC_WCK23#
FBC_CMD0
FBC_CMD9
FBC_CMD8
FBC_CMD32
FBC_CMD7
FBC_CMD11
FBC_CMD15
FBC_CMD14
FBC_CMD3
FBC_CMD1
FBC_CMD6
FBC_CMD10_CKE
FBC_CMD4
FBC_CMD12
FBC_CMD5
FBC_CMD13
FBC_CMD7
FBC_CMD11
FBC_CMD15
FBC_CMD14
FBC_CMD3
FBC_CMD1
FBC_CMD6
FBC_CMD10_CKE
FBC_CMD2_RST
FBC_CLK0#
FBC_CLK0
FBC_VREFC
R50910
1K_1%_2
R50900
121_1%_2
R50901
121_1%_2
FBC_ZQ_1_A
FBC_ZQ_1_B
FBC_CKE_L
FBC_RST*
R50905
10K_1%_2
R50906
10K_1%_2
CLOSE TO VRAM
AROUND UNDER VRAM
OPTION
RIGHT UNDER VRAM
VREFC IS NOT USED IN x16 CONFIGURATION 1K OHM PULL-DOWN IS IN PLACE OF THE 1.33K FOR R104
GPIO10_FBVREF_SEL
50900 - 50999
INVENTEC
MODEL,PROJECT,FUNCTION
Block Diagram
CHANGE by
XXX
PCB P/N
60xxxxxxxxx
DATE
21-OCT-2002
PCB VER
XXX
SIZE
A3
CODE
CS
DOC.NUMBER
1310xxxxx-0-0
REV
X01
SHEET
83
of
139



51000 - 51099

CHANGE by	XXX	DATE	21-OCT-2002		
PCB P/N	60xxxxxxxxx	PCB VER	XXX		

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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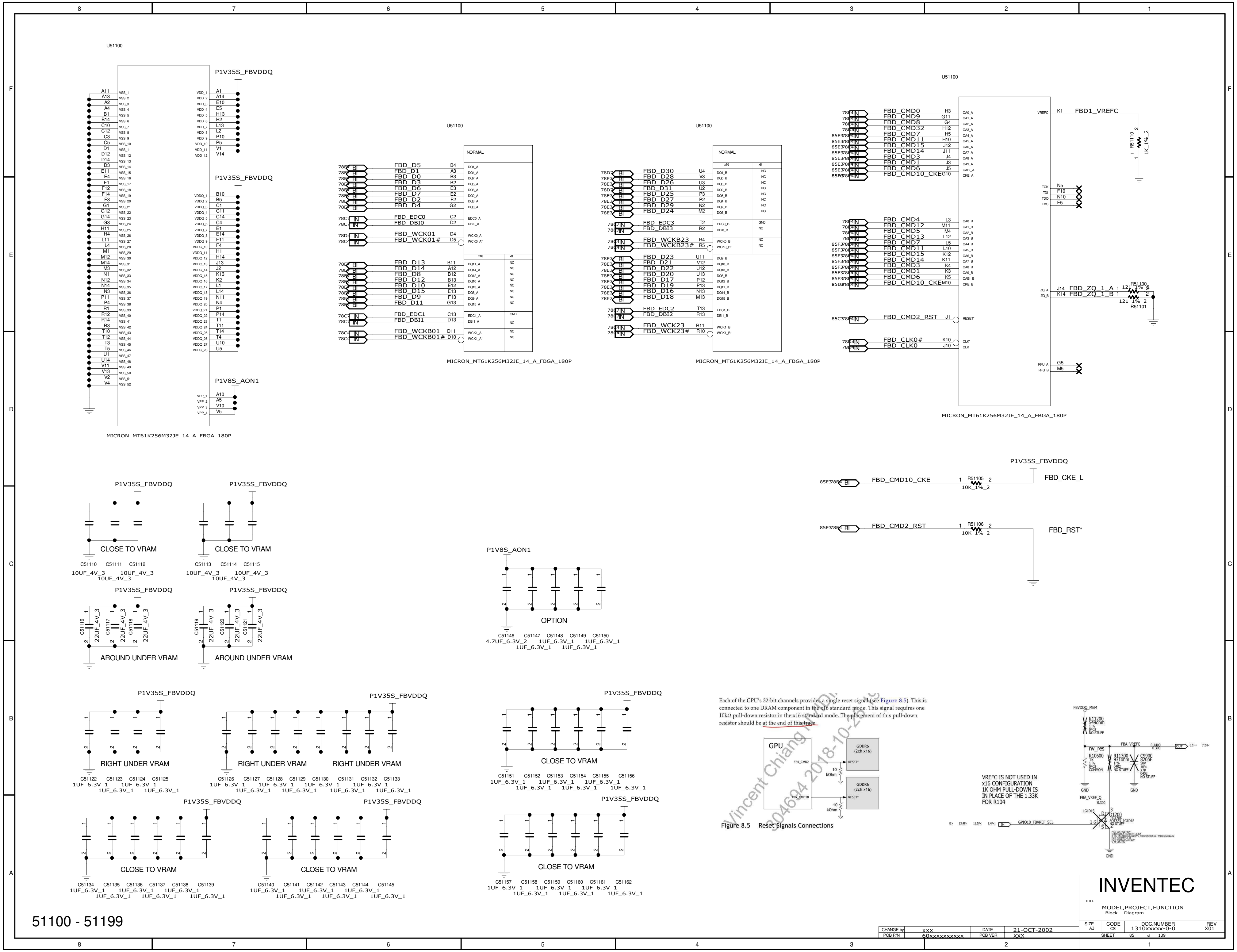

Each of the GPU's 32-bit channels provides a single reset signal (see Figure 8.5). This is connected to one DRAM component in the x16 standard mode. This signal requires one 10kΩ pull-down resistor in the x16 standard mode. The placement of this pull-down resistor should be at the end of this trace.

Figure 8.5 Reset Signals Connections

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION — Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

CHANGE by: XXX — DATE: 21-OCT-2002
PCB P/N: 60xxxxxxxxxx — PCB VER: XXX

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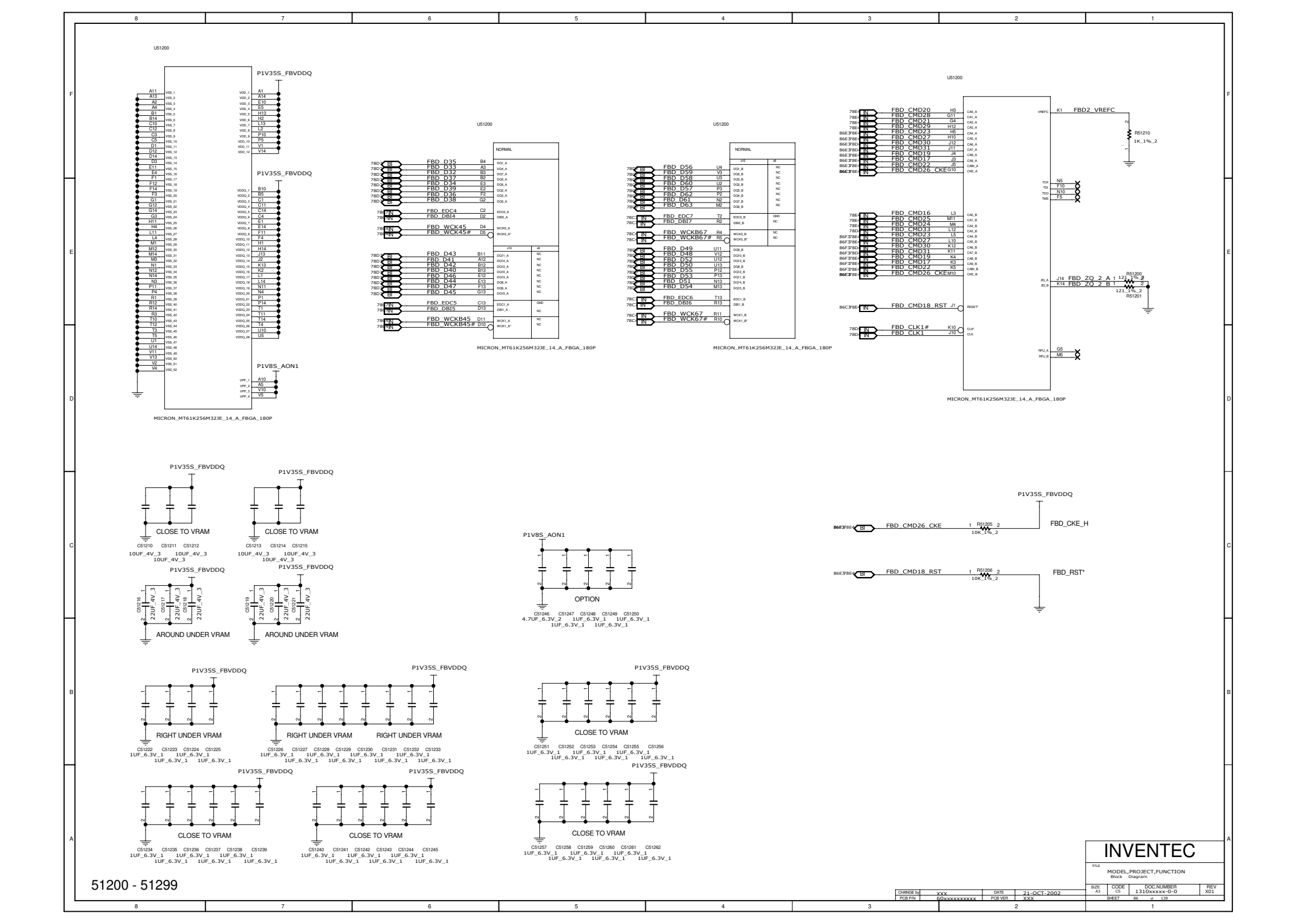

51200 - 51299

CHANGE by	XXX	DATE	21-OCT-2002	
PCB P/N	60xxxxxxxxx	PCB VER	XXX	

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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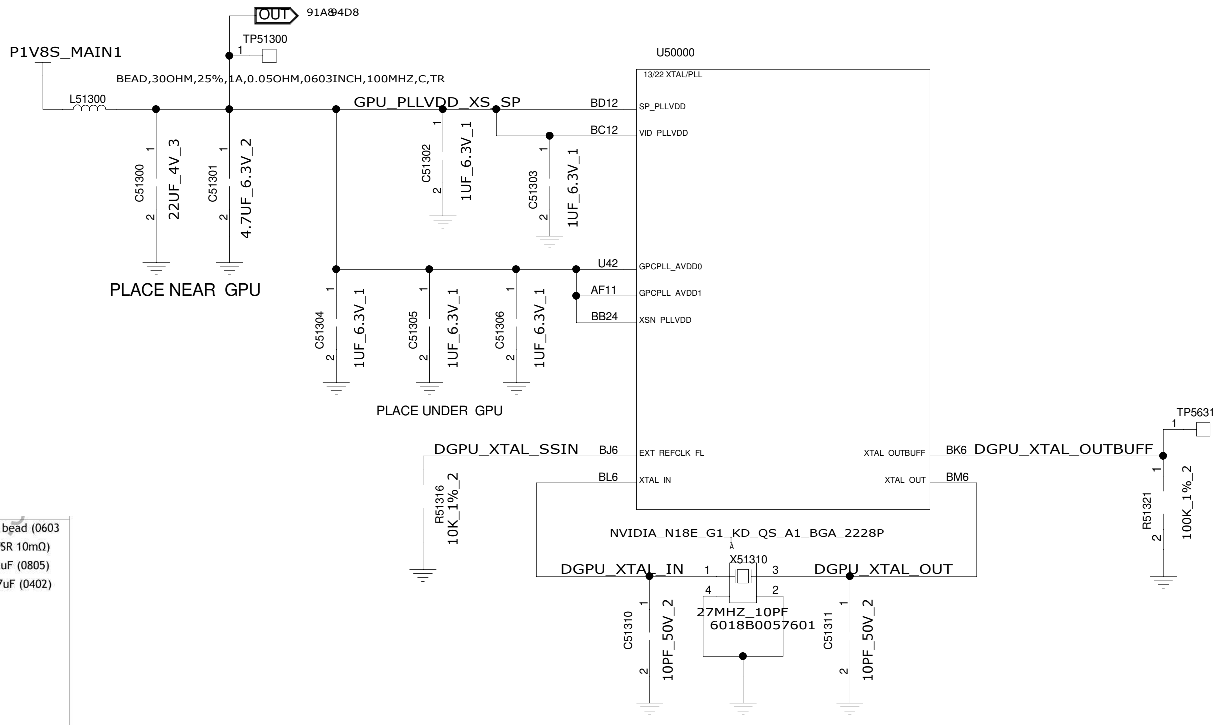
27 MHZ XTAL



CL=2*10-(5+3)=12

CL_trim = 2 × CLoad - (Cstray + Ci)

Where:

- C_{Load} is the crystal load capacitance (from data sheet of XTAL used)
- C_{stray} is ~ 3pF (Stray capacitance of XTAL pads and any significant trace routing)
- C_i is pin capacitance (5 pF)

Typical CL_trim = 28 pF when crystal load = 18 pF, stray Capacitance = 3 pF, and XTAL pins capacitance = 5 pF

IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S) - - - - - - - - - - - - - - - - Alternate solution: 3 x 1.0uF (0201W X6S)	1 x 30Ω bead (0603 max ESR 10mΩ) 1 x 22uF (0805) 1 x 4.7uF (0402)
IFPCD_PLLVDD	1			
IFPEF_PLLVDD	1			
GPCPLL_AVDDx XSN_PLLVDD	3		3 x 0.47uF (0201W X6S) - - - - - - - - - - - - - - - - Alternate solution: 3 x 1.0uF (0201W X6S)	
SP_PLLVDD	1		1 x 0.47uF (0201W X6S) - - - - - - - - - - - - - - - - Alternate solution: 1 x 1.0uF (0201W X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S) - - - - - - - - - - - - - - - - Alternate solution: 1 x 1.0uF (0201W X6S)	

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION — Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	
PCB P/N	60xxxxxxxxxx	PCB VER	XXX	
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01	

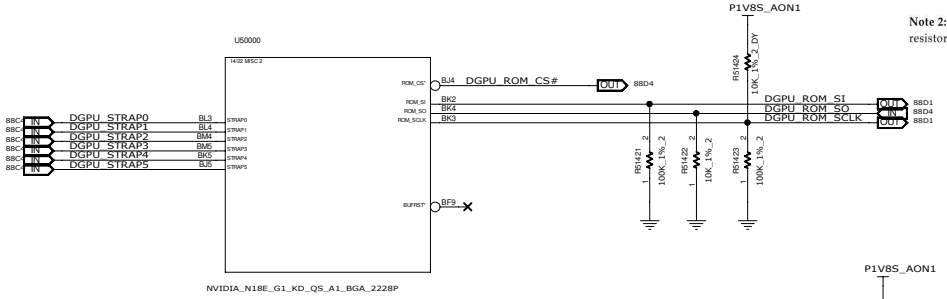
GPU VBIOS, EXTERNAL STRAPS

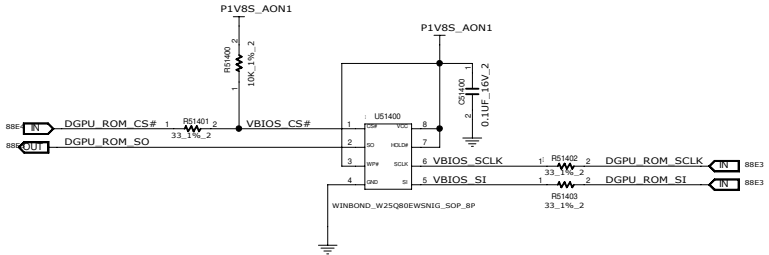
Table 12.4 FS_OVERT* Strap Enablement

Strap Pins see Note 1			FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK	
L	L	L	FS_OVERT* function **ENABLED**
L	L	H	FS_OVERT* function **DISABLED** (Reserved; do not configure)
all other configurations			(Invalid; do not configure)

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to strap inputs may result.

Note 2: The ROM_SO pin should be pulled low using a 10 kΩ resistor instead of a 100 kΩ resistor.





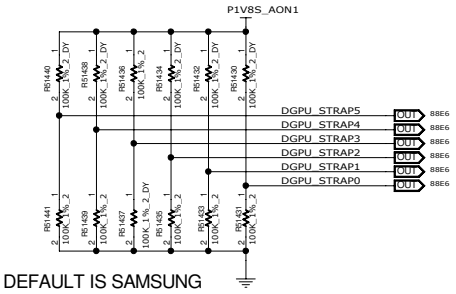


Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0

Table 12.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins See Note			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1
H	L	M				
H	M	L				
H	M	H				
H	H	M				
L	M	M				
M	L	M				
M	M	L				
M	M	M				
M	H	M				
H	M	M				
M	M	M				

Reserved

DEFAULT IS SAMSUNG

SAMSUNG K4Z80325BC-HC14
6019B1847601
STRAP 0X0=000
SAMSUNG:R51431 STUFF
R51430 NOT STUFF

MICRON MT61K256M32JE-14:A
6019B1847701
STRAP 0X1=001
MICRON :R51430 STUFF
R51431 NOT STUFF

Table 2. N18E-G2/G1 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDDI/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.25V and 1.35V[1]	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	N/A	Full	Production candidate
			Samsung	K4ZB0325BC-HC14	C-die	0x0	14 Gbps	N/A	Full	Production candidate

Notes:
1. For N18E-G2/G1, the maximum allowable memory case temperature is 95 °C.
2. DVS is required. WCK: TBD

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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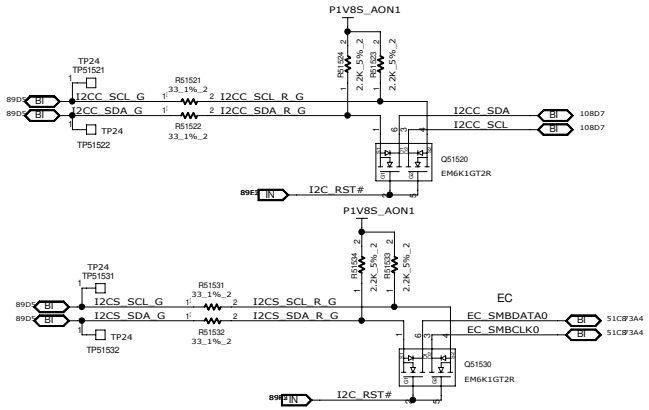
GPU GPIO

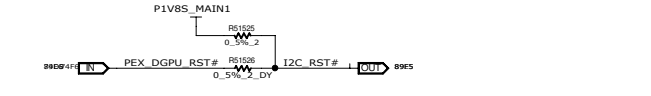
Table 7 Thermal Specifications

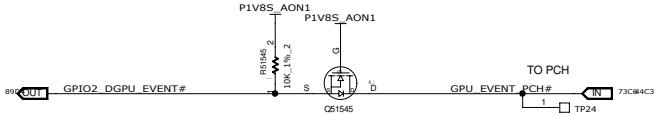
Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
Thermal Resistance (Junction to Case, $R_{\Theta JC}$)	0.014	0.017	0.017	TBD	°C/W
Thermal Resistance (Junction to PCB Board, $R_{\Theta JB}$)	0.64	0.96	0.96	TBD	°C/W
GPU Shutdown Temperature (OVERT)[1]	99	99	99	TBD	°C
GPU Slowdown Temperature (THERM_ALERT)[2]	94	94	94	TBD	°C

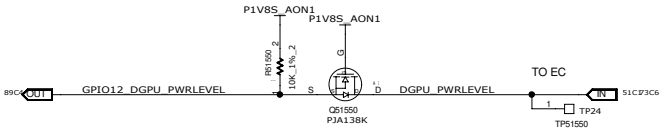
Parameter	N18E-G3	N18E-G2	N18E-G1	N18E-G0	Units
GPU Maximum Operating Temperature[3]	89	89	89	TBD	°C
GPU Target Temperature	87 (Default) 75 (Min)	87 (Default) 75 (Min)	87 (Default) 75 (Min)	TBD	°C

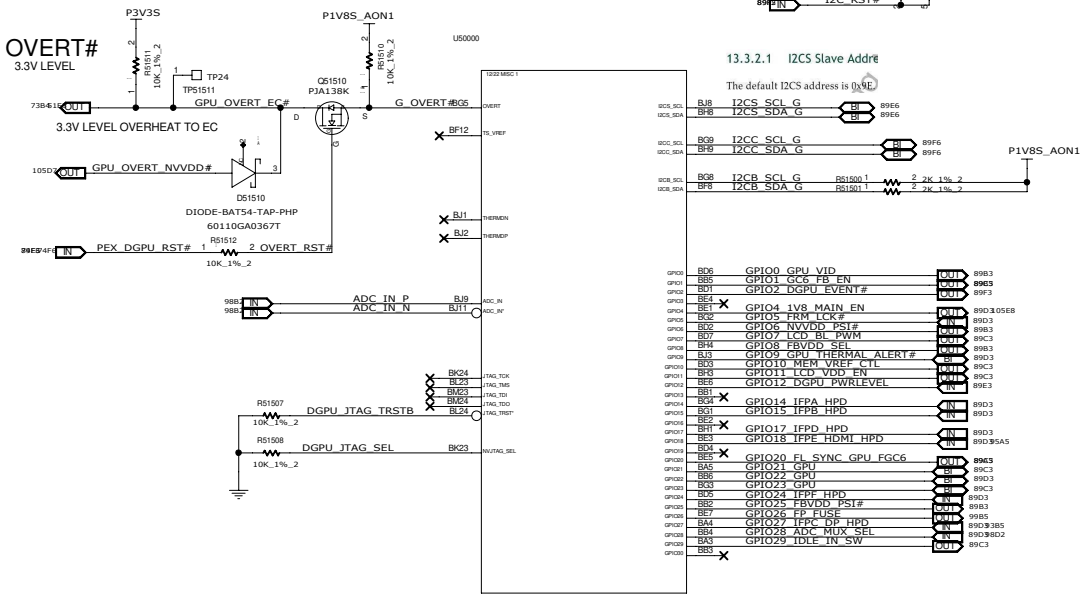
Notes:
1. OVERT results in an 87.5% (-8) hardware clock slowdown.
2. THERM_ALERT results in a 50% (-2) hardware clock slowdown.
3. The GPU maximum operating temperature is the maximum GPU temperature at which the GPU is guaranteed to operate at the target performance (base clocks) under the total board power level.



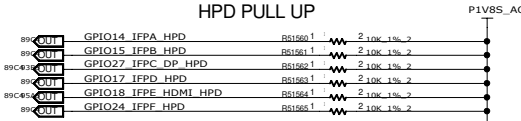




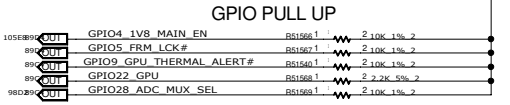




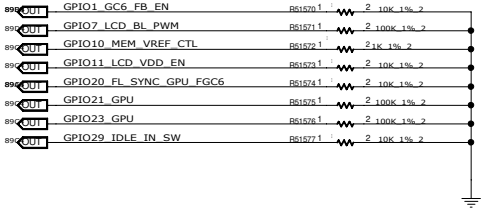
HPD PULL UP

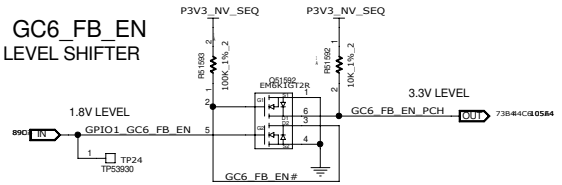


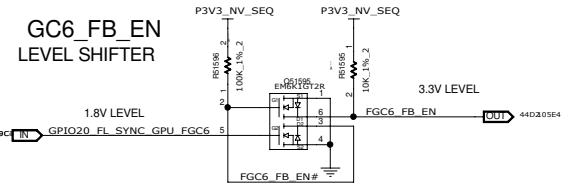
GPIO PULL UP

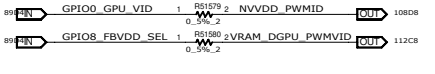


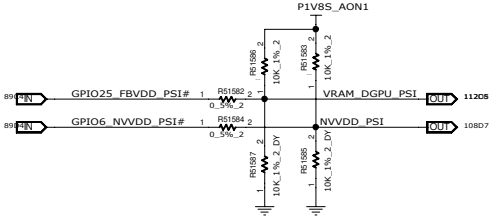
GPIO PULL DOWN











53900 - 54199
51500 - 51599

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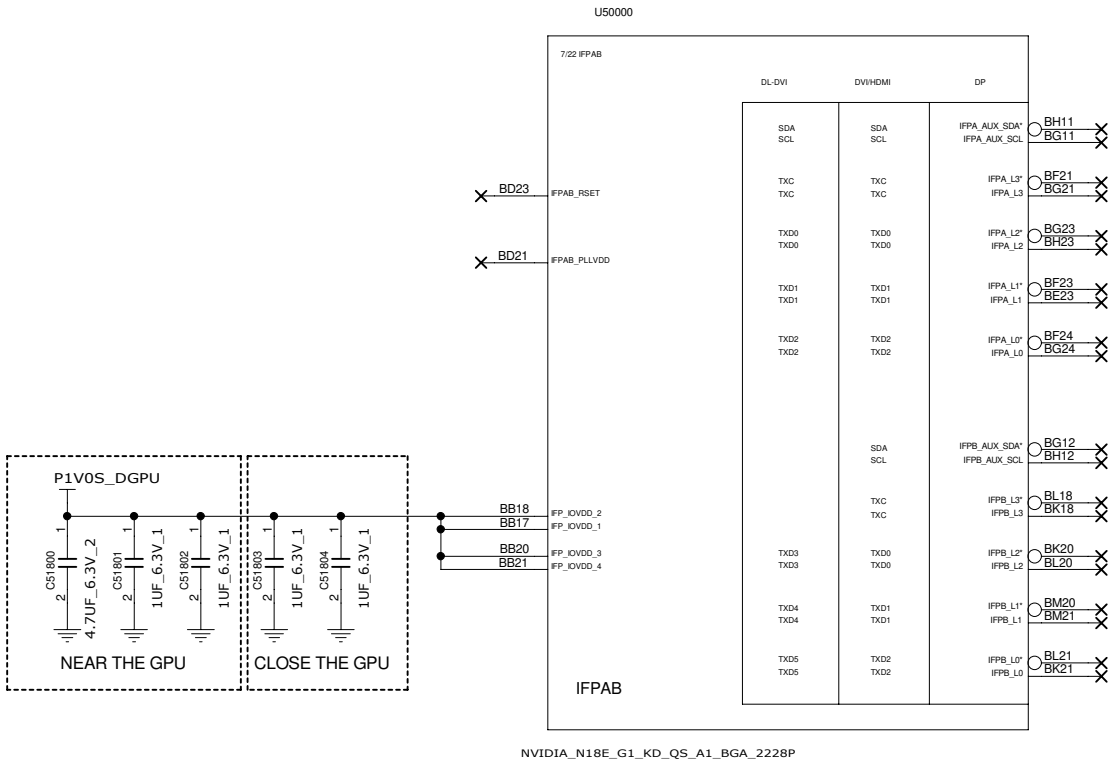
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxx	PCB VER	XXX			SHEET 89 of 139	



51800 - 51899

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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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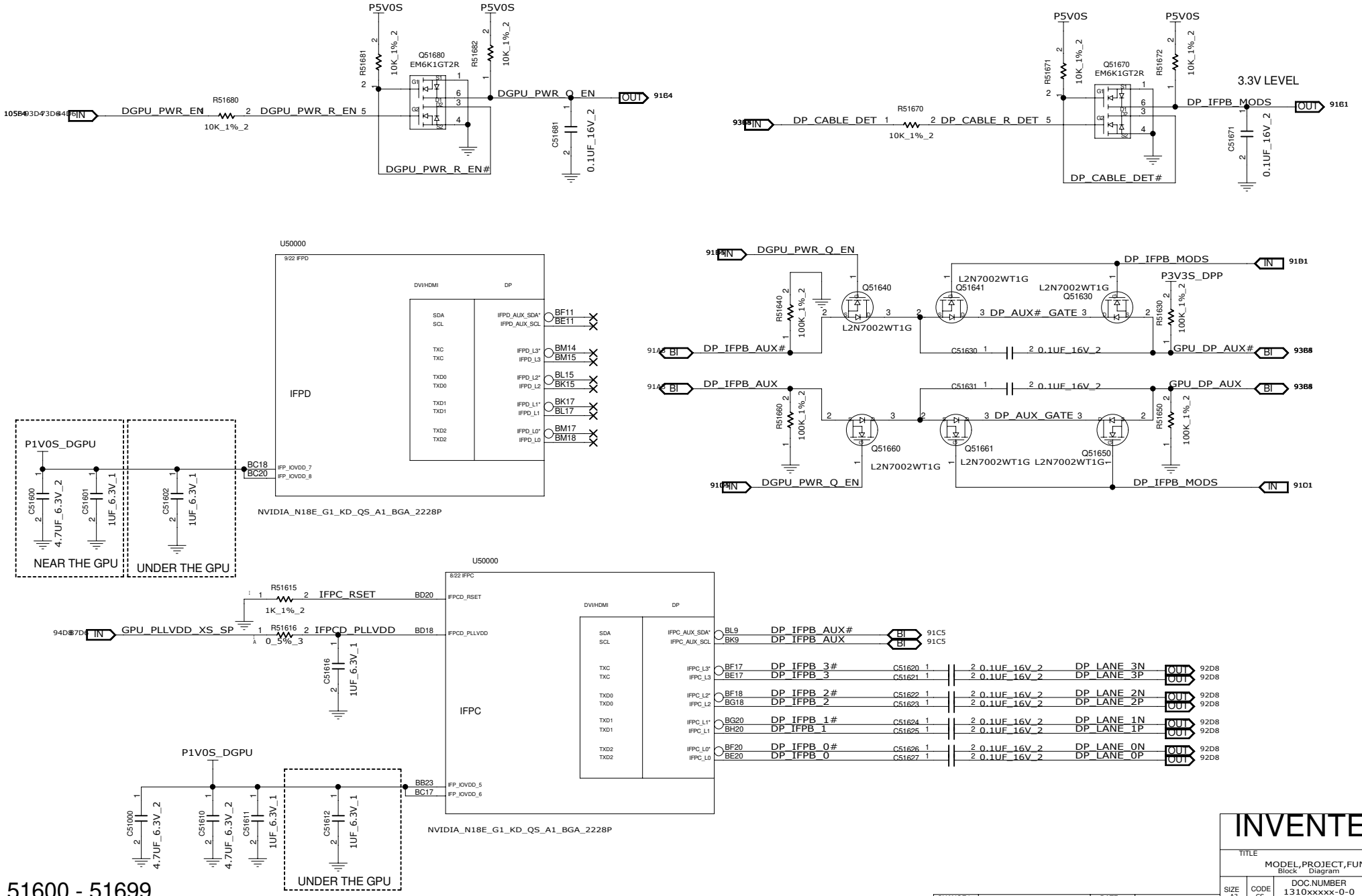

51600 - 51699

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PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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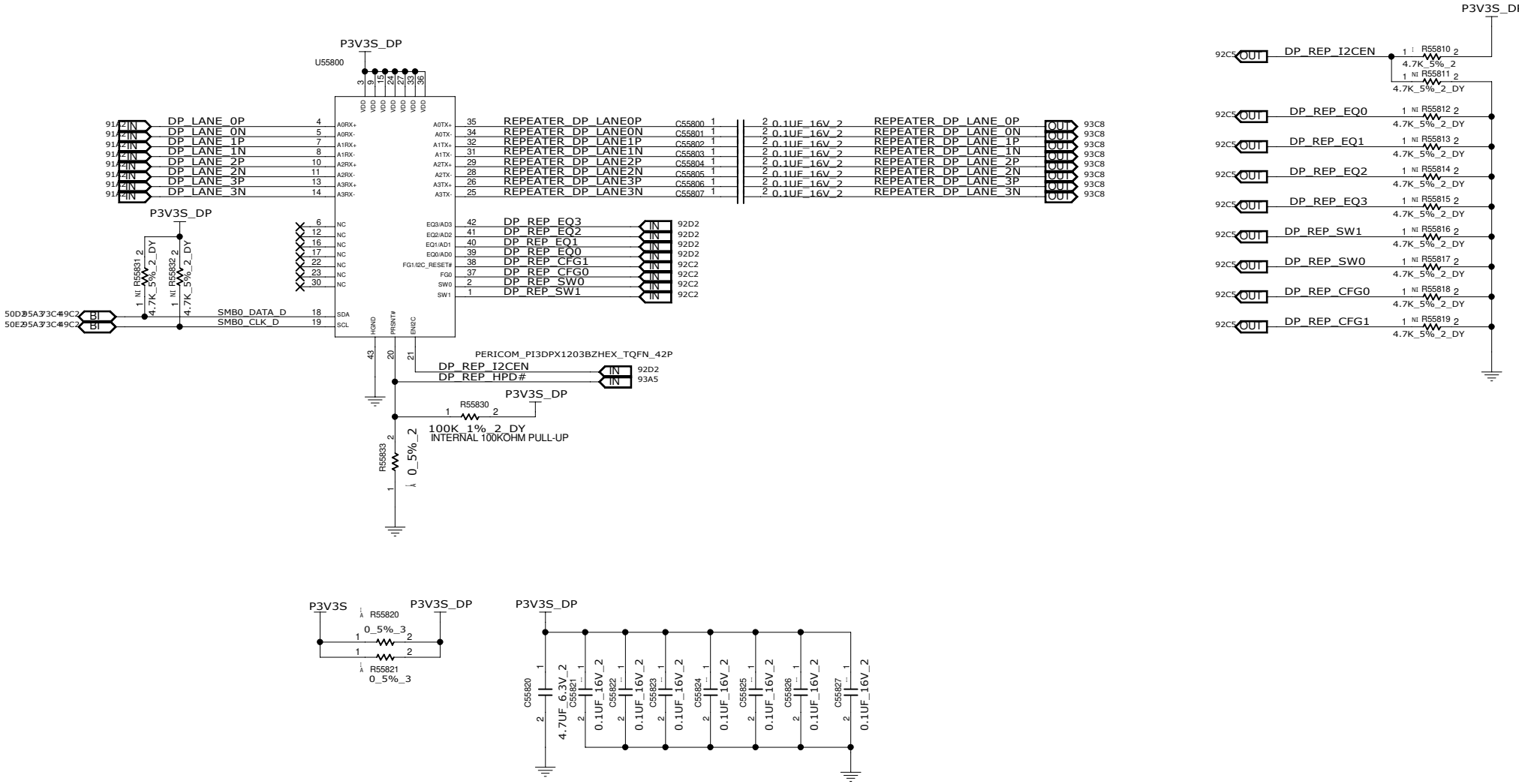
DP REDRIVER



55800 - 55999 56000 - 56199

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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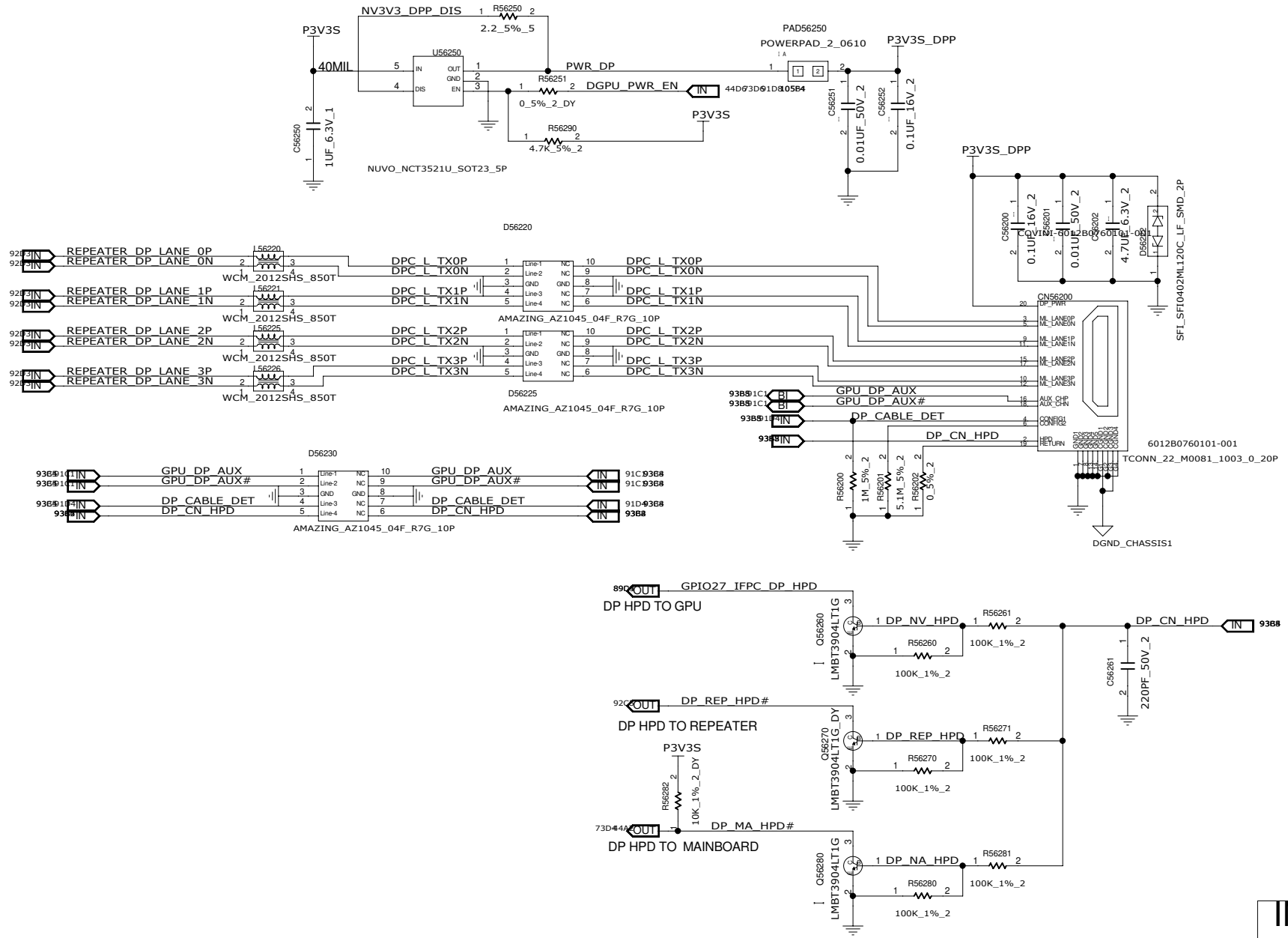

56200 - 56399

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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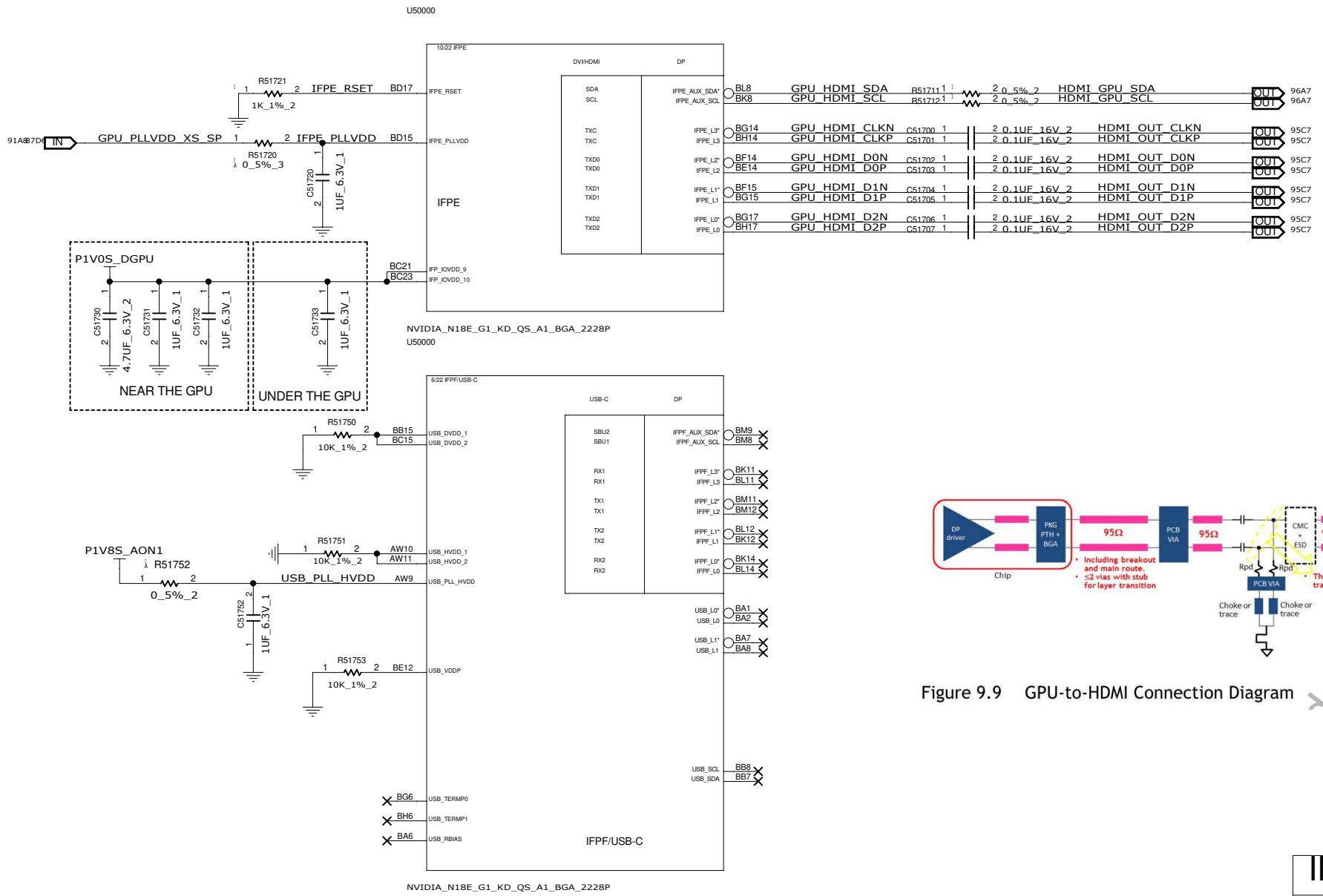

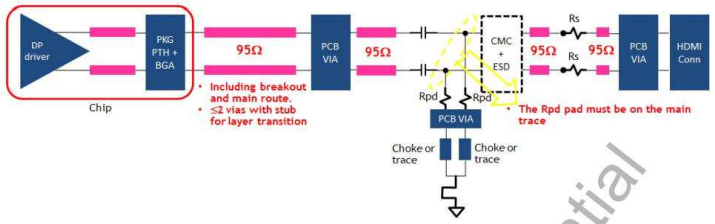

Figure 9.9 GPU-to-HDMI Connection Diagram

51700 - 51799

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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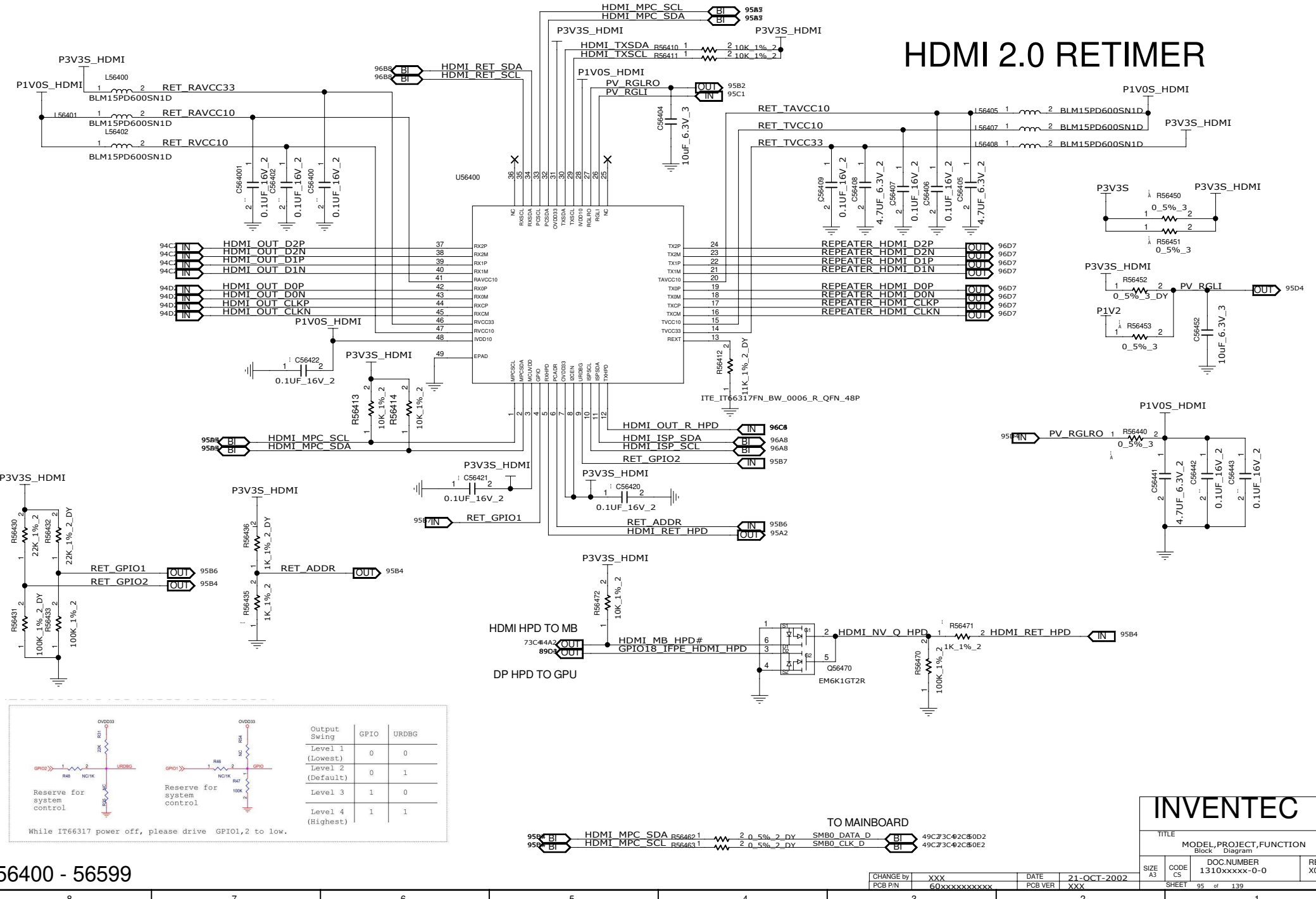
HDMI 2.0 RETIMER



Output Swing	GPIO	URDBG
Level 1 (Lowest)	0	0
Level 2 (Default)	0	1
Level 3	1	0
Level 4 (Highest)	1	1

56400 - 56599

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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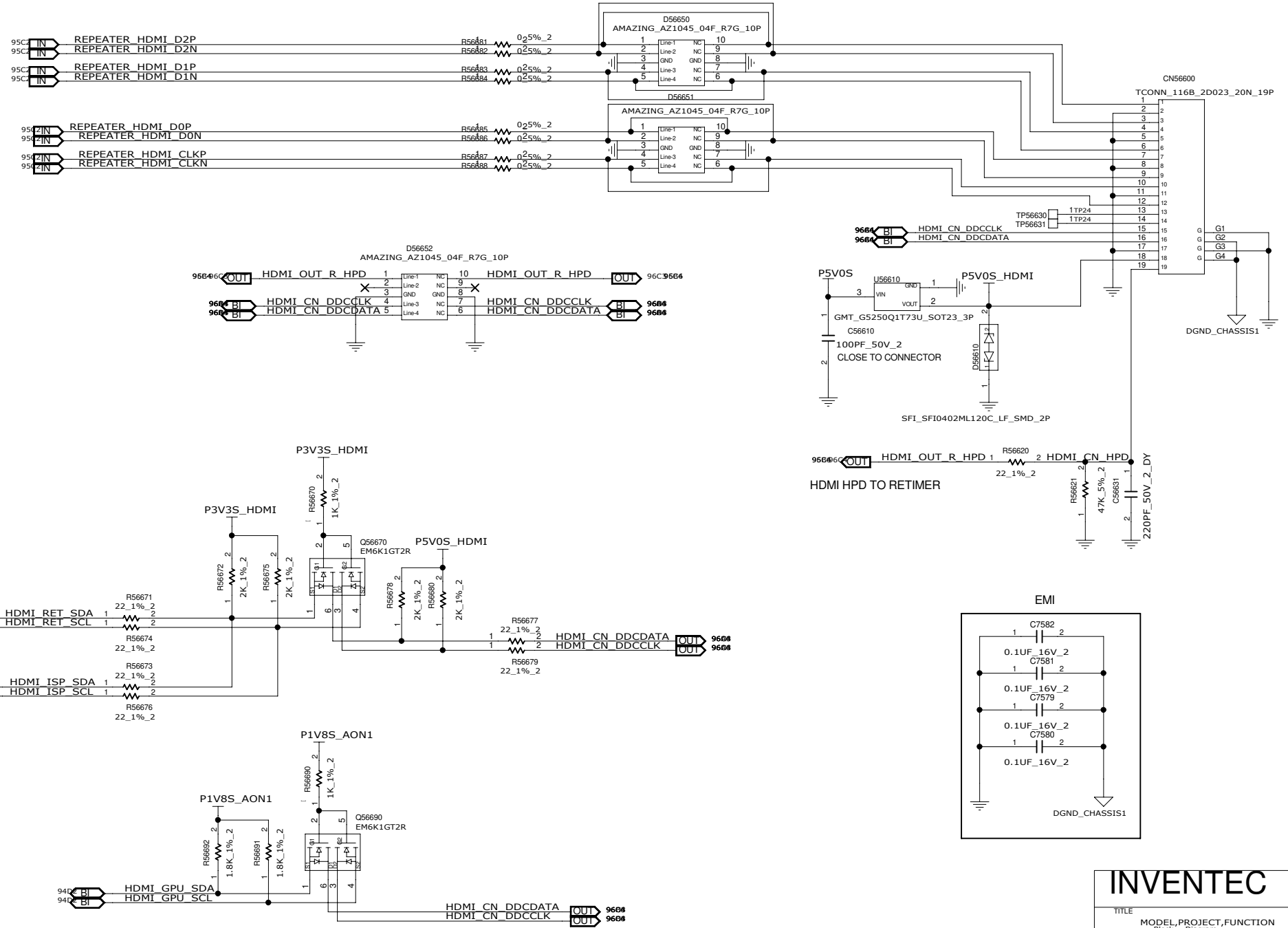
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



56600 - 56799

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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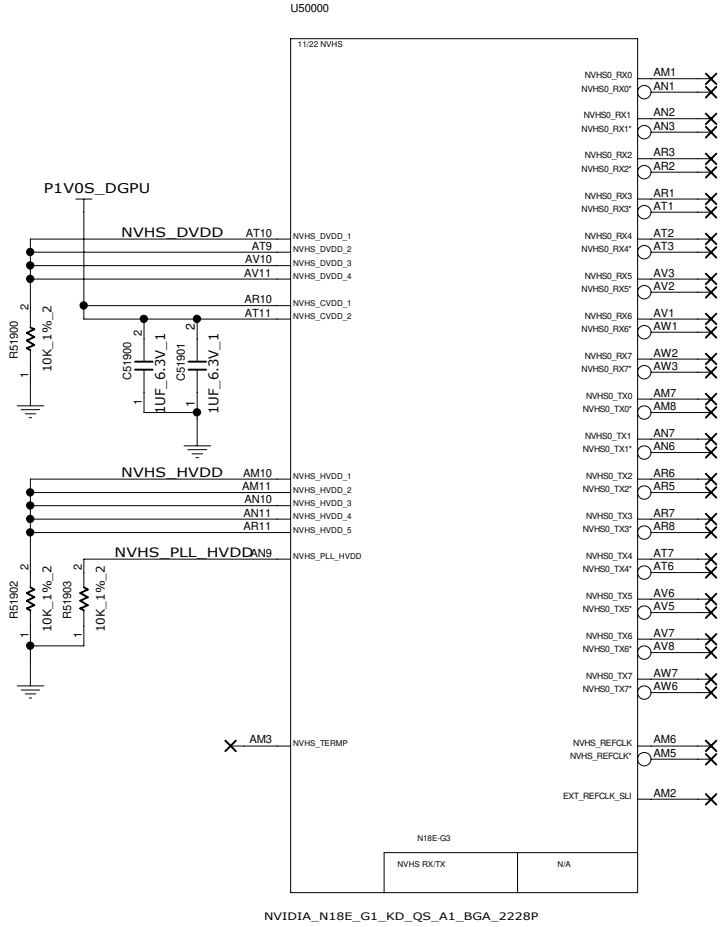
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



NVIDIA_N18E_G1_KD_QS_A1_BGA_2228P

51900 - 51999

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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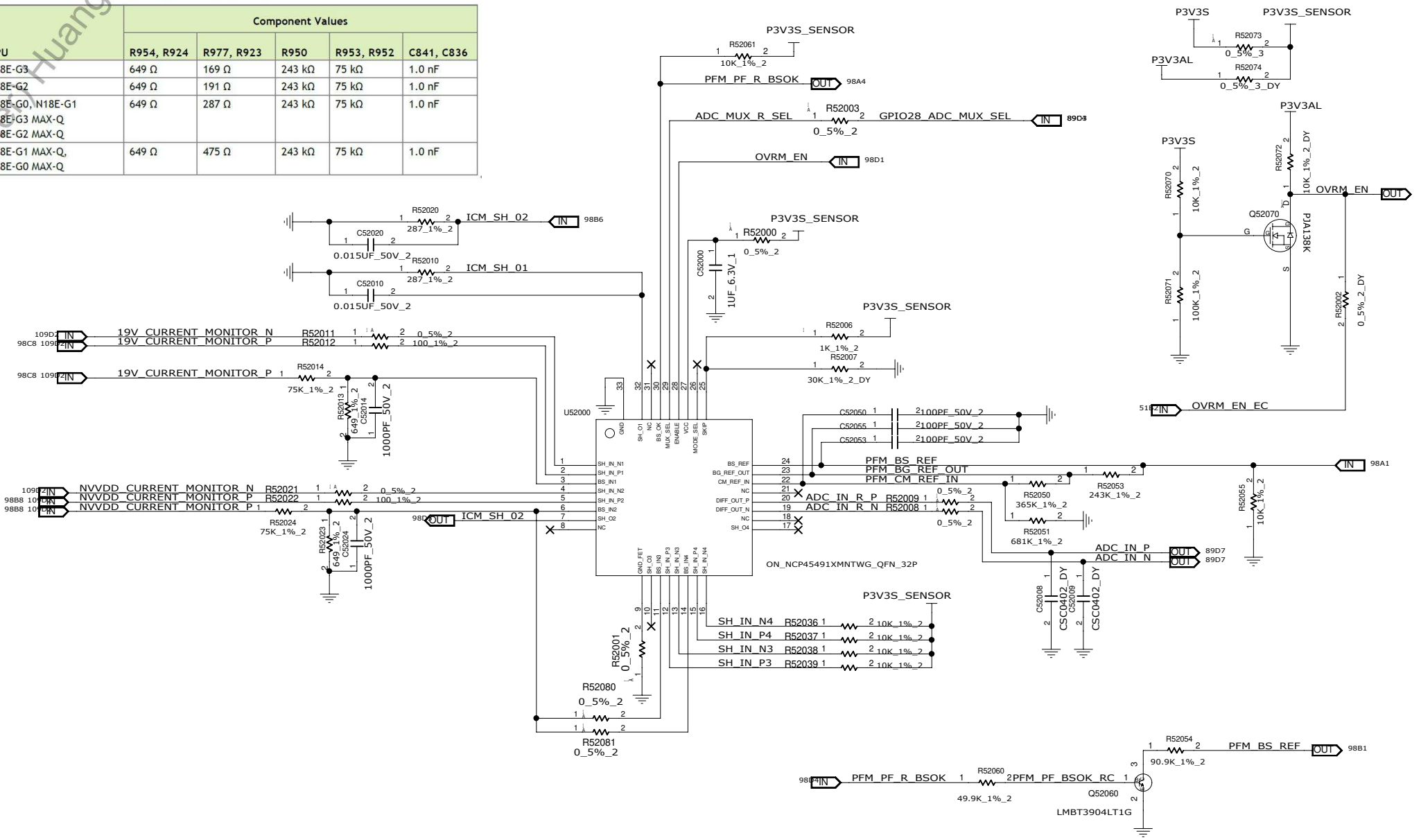
Table 13. Power Monitoring with OnSemi OVR-M

GPU	Component Values				
	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18E-G3	649 Ω	169 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G2	649 Ω	191 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G0, N18E-G1 N18E-G3 MAX-Q N18E-G2 MAX-Q	649 Ω	287 Ω	243 kΩ	75 kΩ	1.0 nF
N18E-G1 MAX-Q, N18E-G0 MAX-Q	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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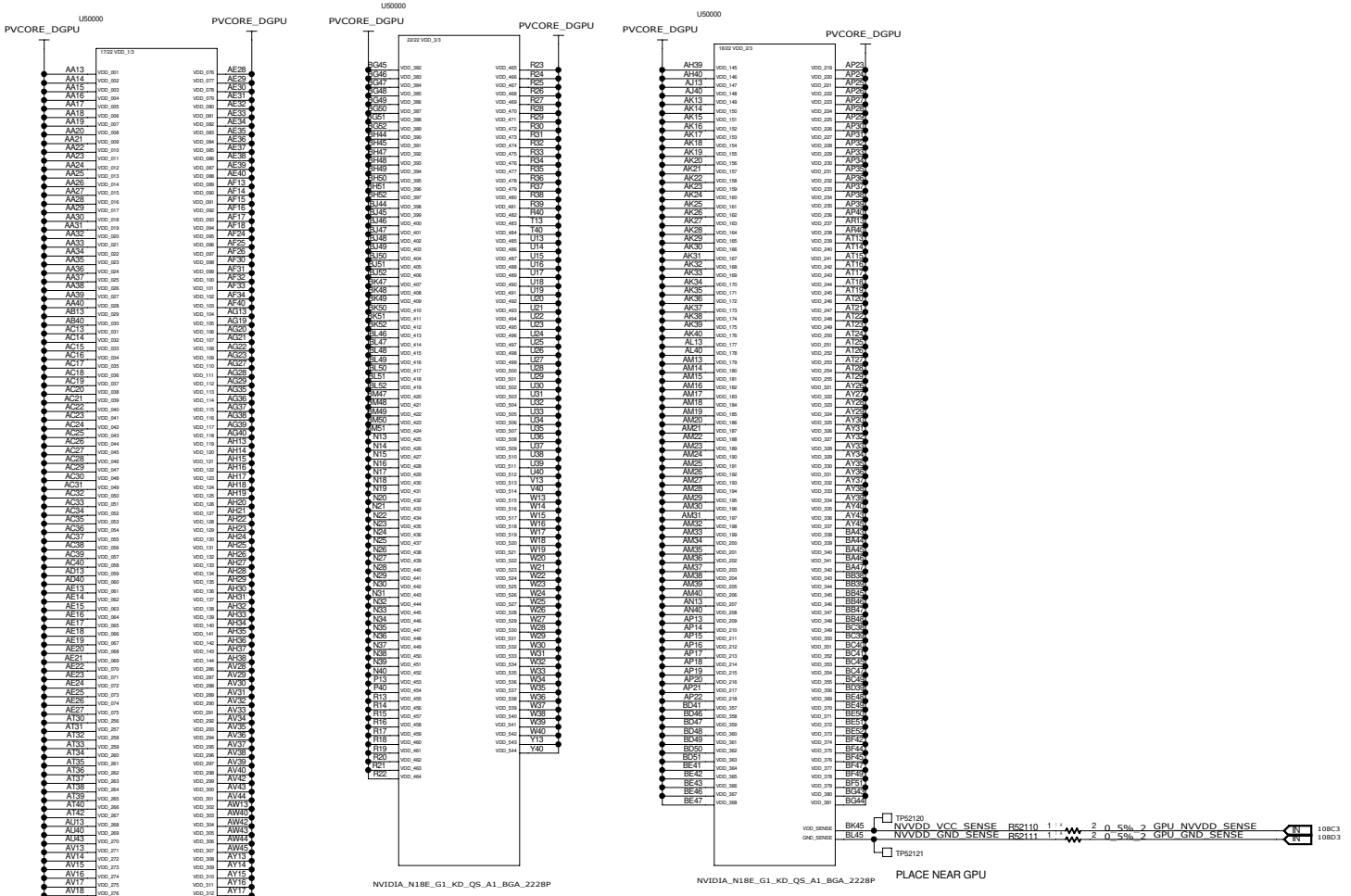
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

52000 - 52099



The required subcircuit is shown in detail in Figure 15.6.

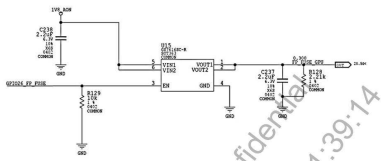
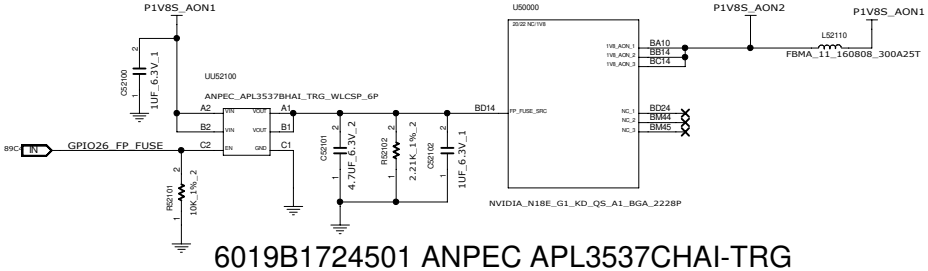
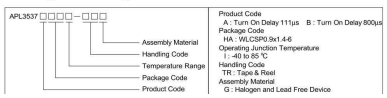


Figure 15.6 Subcircuit Schematic



6019B1724501 ANPEC APL3537CHAI-TRG



In Figure 15.6, the component labeled "U15" is an active switch; devices equivalent to the GS76165C-R are acceptable as long as they meet the following requirements:

- The active switch must be capable of driving 100mA or more.
- The timing delay from GPIO26_FP_FUSE assertion to FP_FUSE_GPU (active switch output) must be 100msec or less.
- There must be no glitch during power up or GC6/GC-OFF entry or exit.
- The FP_FUSE_GPU (output) trace width must be 0.25 mm (10 mil) or greater.

52100 - 52199

INVENTEC

MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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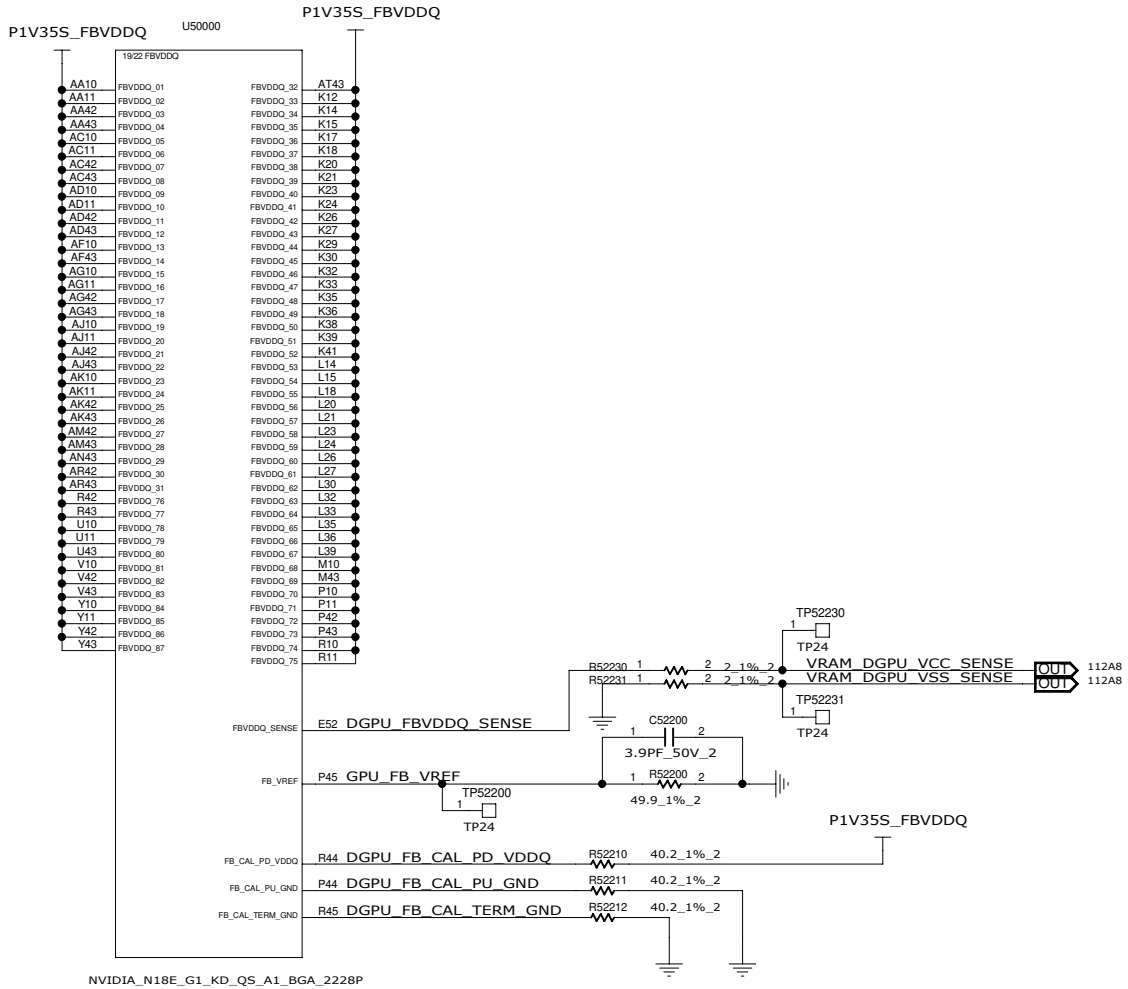

55600 - 55699

52200 - 52299

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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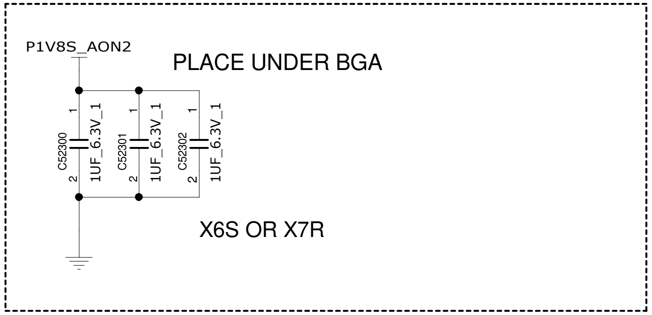
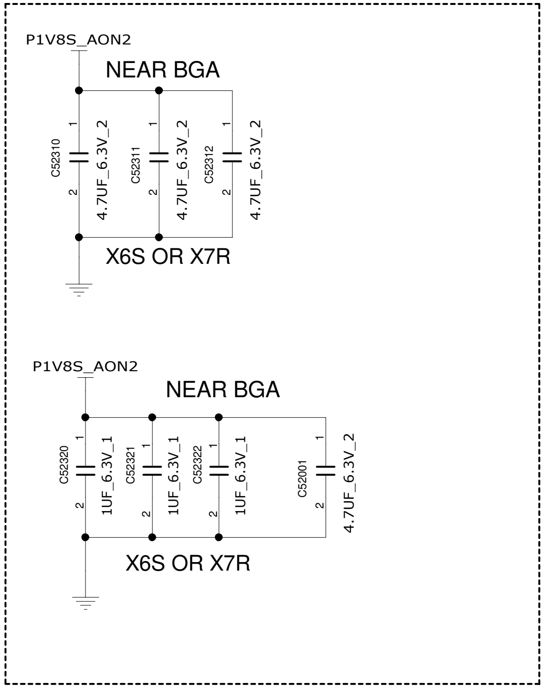
GPU 1V8_AON DECOUPLING





1V8_AON	3	1.8V	3 x 0.47uF (0201W X6S) - - - - - - - - - - - - - - - - Alternate solution: 3 x 1.0uF (0201W X6S)	3 x 1uF (0402 X6S) 3 x 4.7uF (0603 X6S)

52300 - 52399

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
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CHANGE by	XXX	DATE	21-OCT-2002
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52400 - 52999

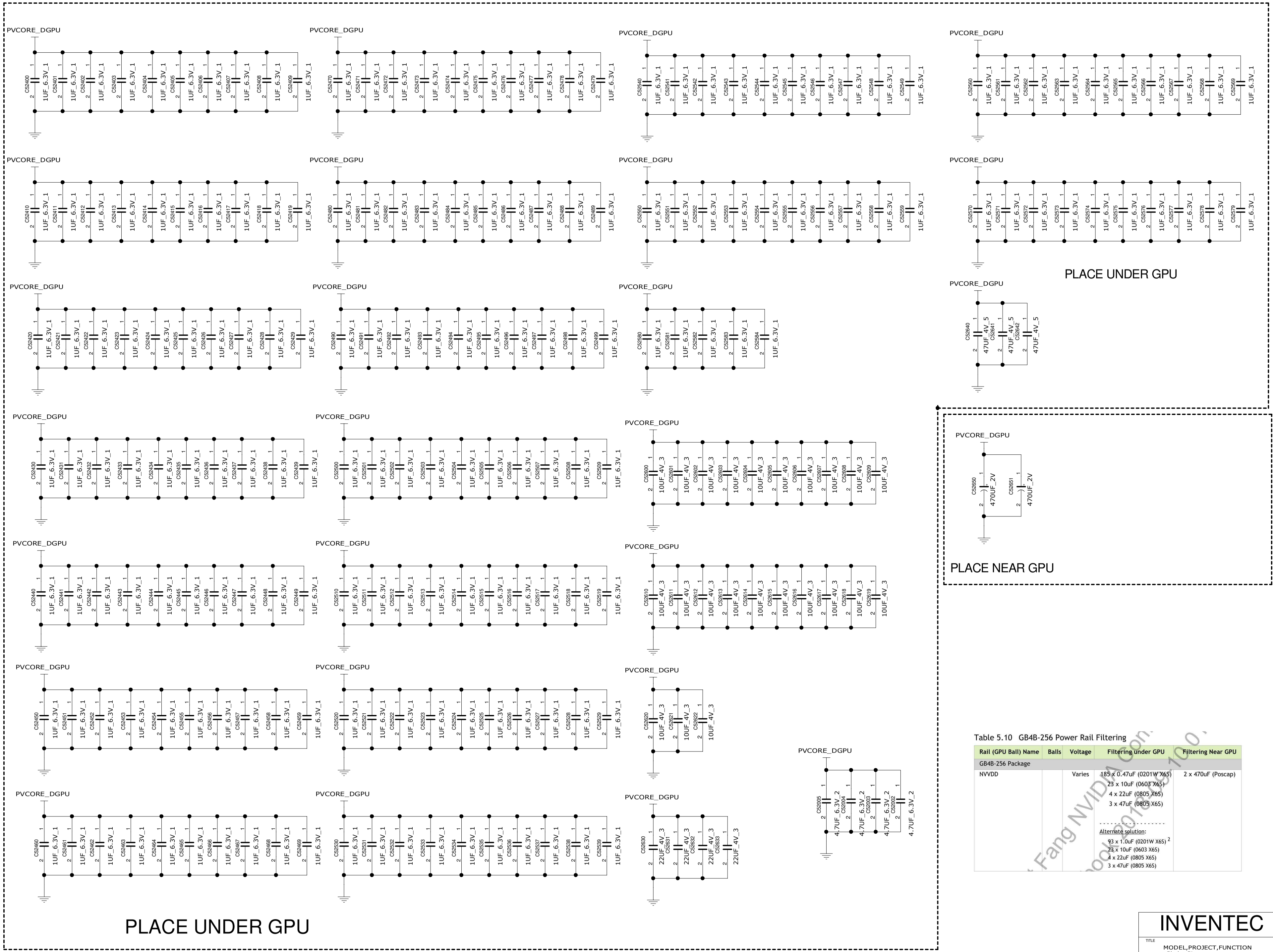

Table 5.10 GB4B-256 Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 x 0.47uF (0201W X6S) 23 x 10uF (0603 X6S) 4 x 22uF (0805 X6S) 3 x 47uF (0805 X6S) - - - - - - - - - - - - - - - - - - Alternate solution: 93 x 1.0uF (0201W X6S) 2 23 x 10uF (0603 X6S) 4 x 22uF (0805 X6S) 3 x 47uF (0805 X6S)	2 x 470uF (Poscap)

INVENTEC

TITLE MODEL,PROJECT,FUNCTION
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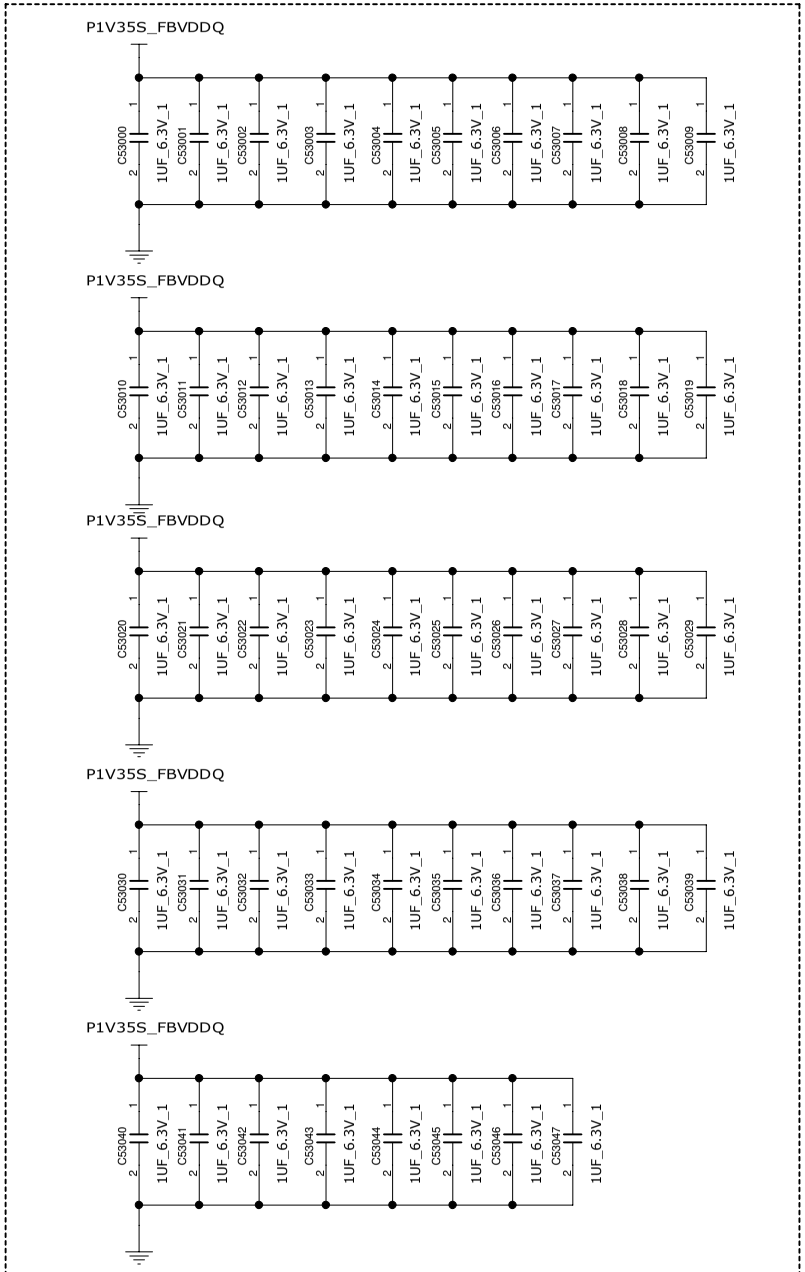

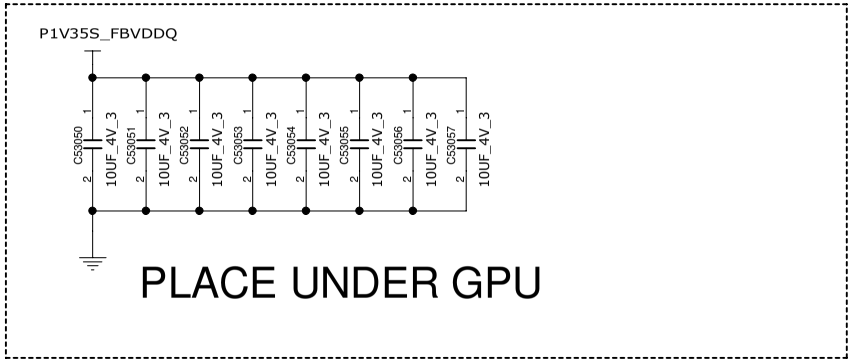

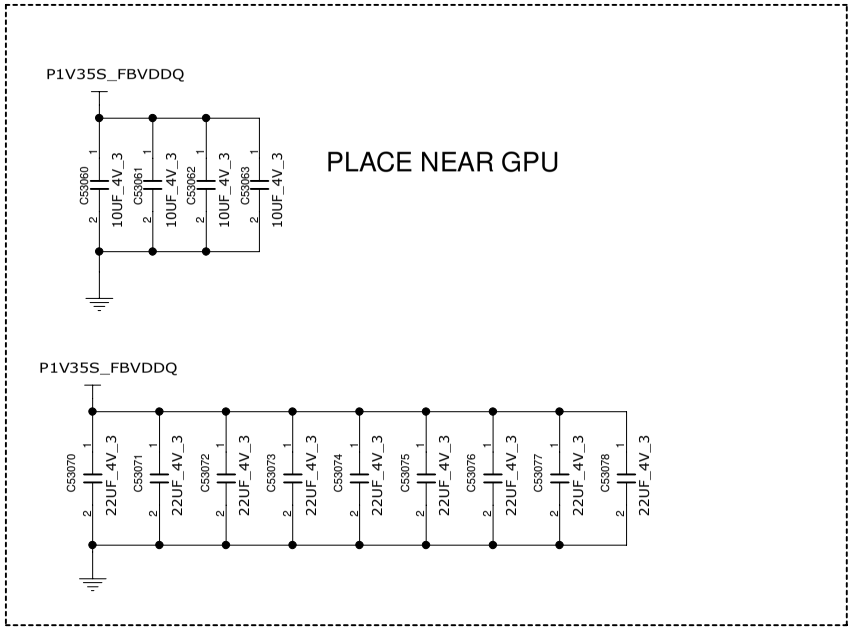

FBVDDQ (GPU side)	1.25V	48 x 0.47uF (0201W X6S)	4 x 10uF (0603 X6S)
	1.35V	8 x 10uF (0603 X6S)	9 x 22uF (0603 X6S)
		Alternate solution:	
		24 x 1.0uF (0201W X6S) [2]	
		8 x 10uF (0603 X6S)	

53000 - 53299

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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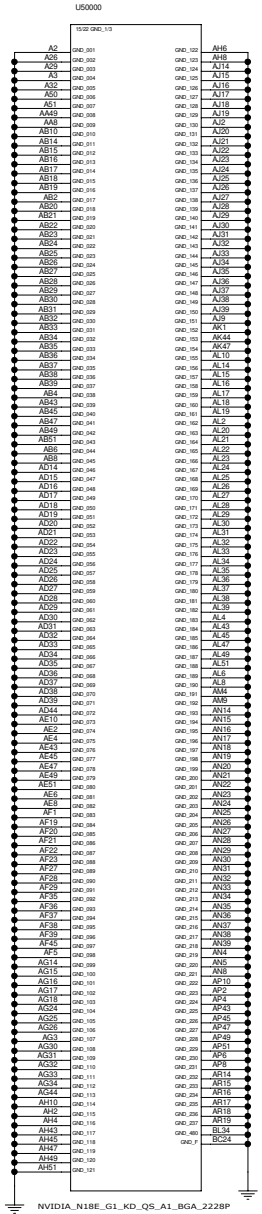
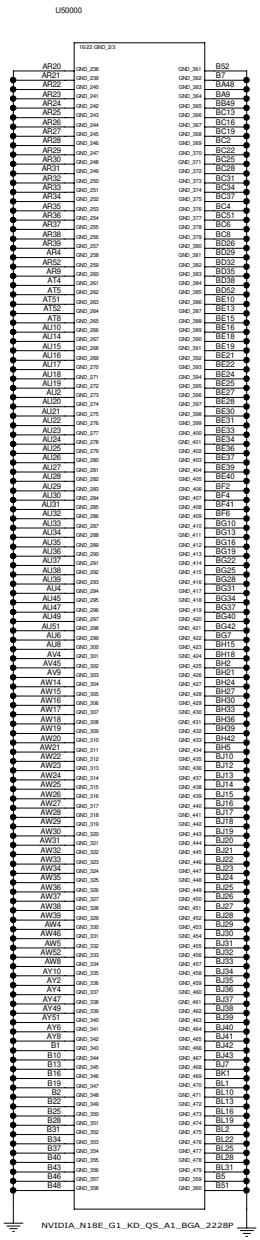
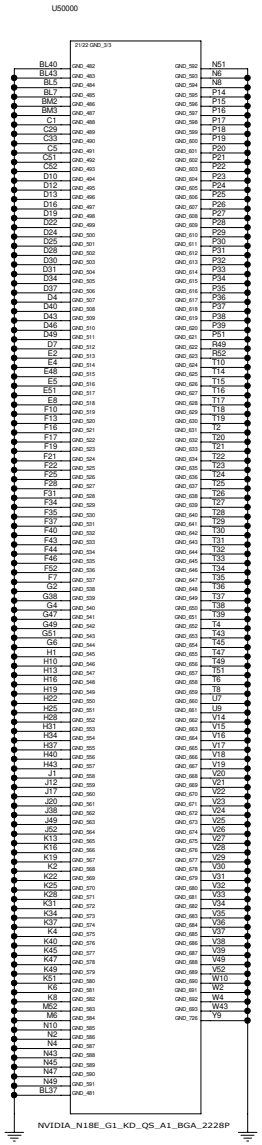
GND







53300 - 53499

CHANGE by	XXX	DATE	21-OCT-2002
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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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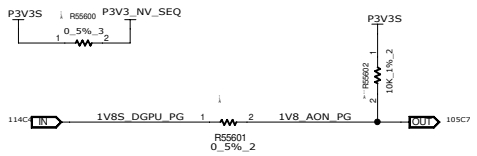
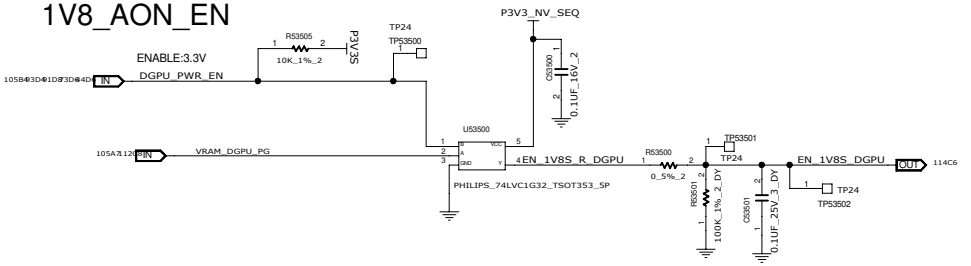
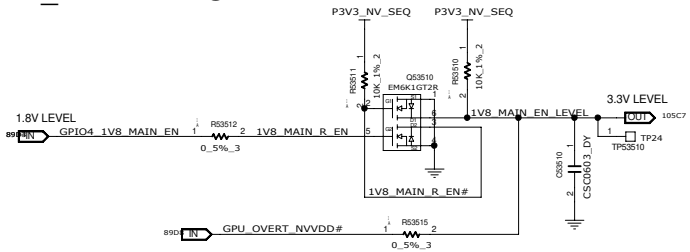


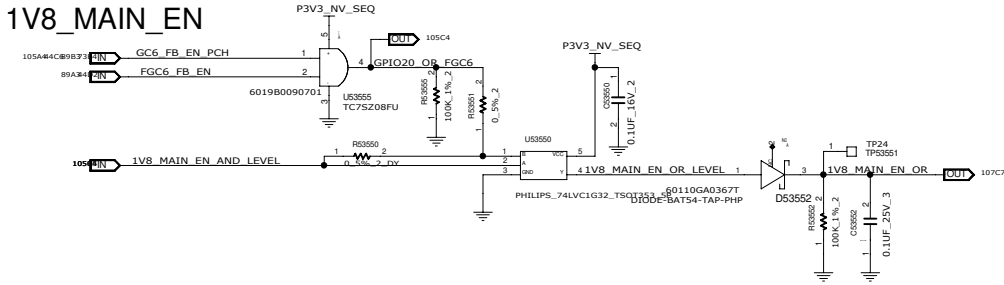
1V8_AON_EN



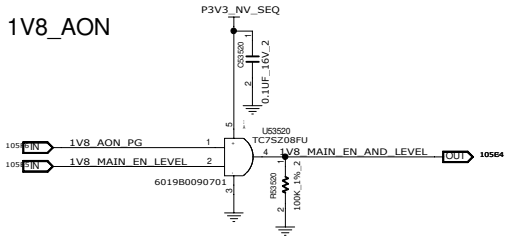
1V8_MAIN_EN LEVEL SHIFT



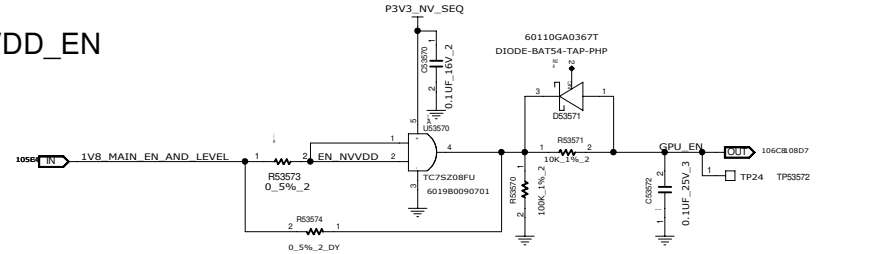
1V8_MAIN_EN



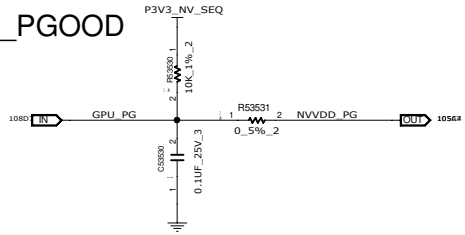
1V8_MAIN_EN AND WITH 1V8_AON



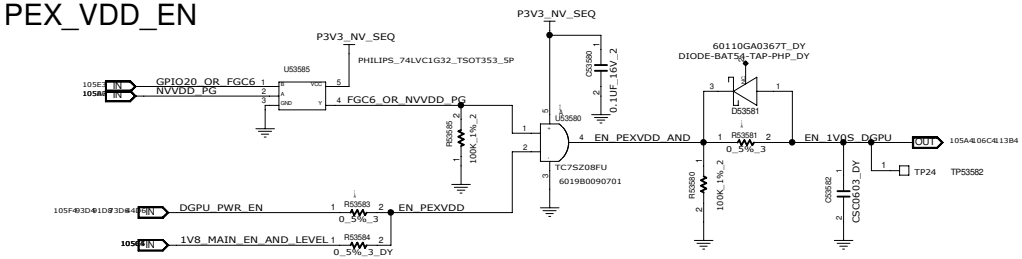
NVVDD_EN



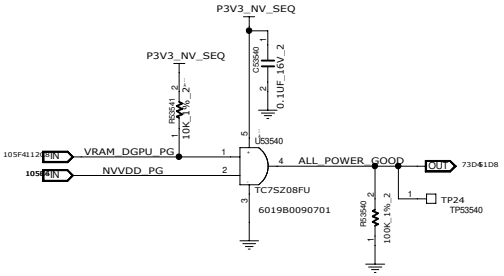
NVVDD_PGOOD



PEX_VDD_EN



ALL POWER GOOD

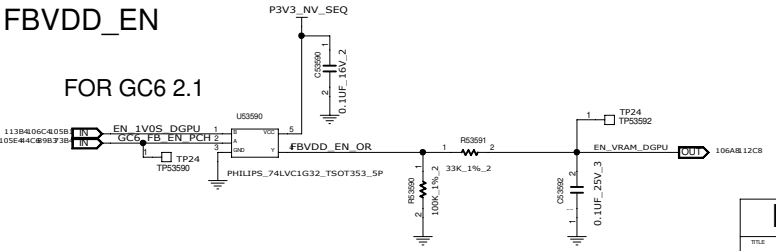


55600 - 55699

53500 - 53899

FBVDD_EN

FOR GC6 2.1



INVENTEC

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Block Diagram

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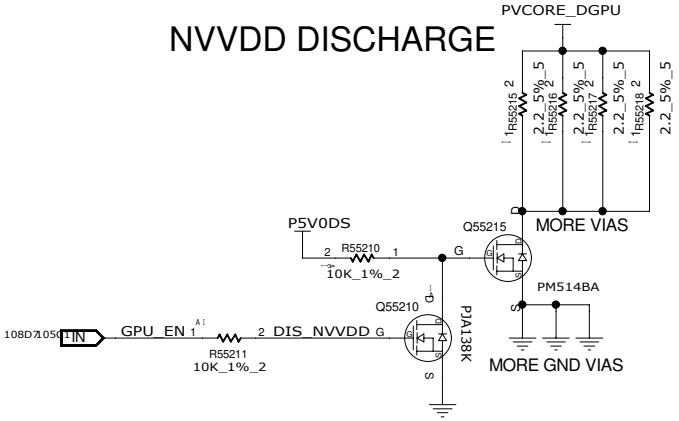
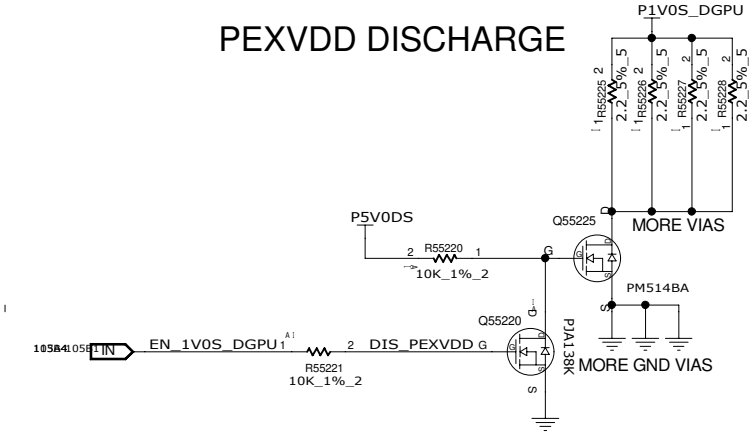
DISCHARGE CIRCUIT

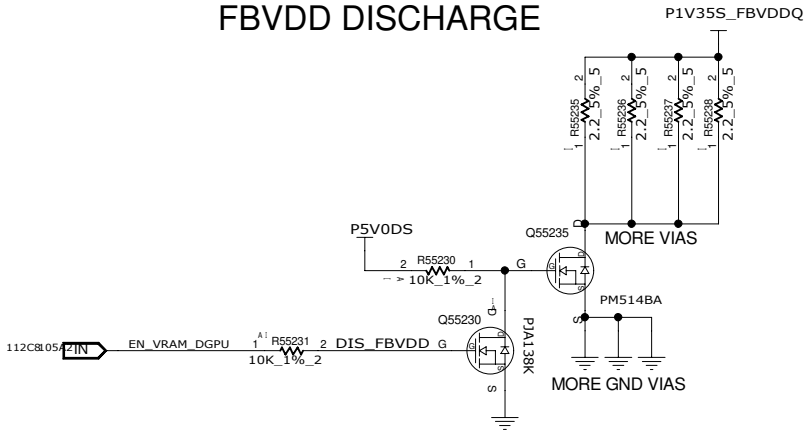
NVVDD DISCHARGE



PEXVDD DISCHARGE



FBVDD DISCHARGE



55200 - 55299

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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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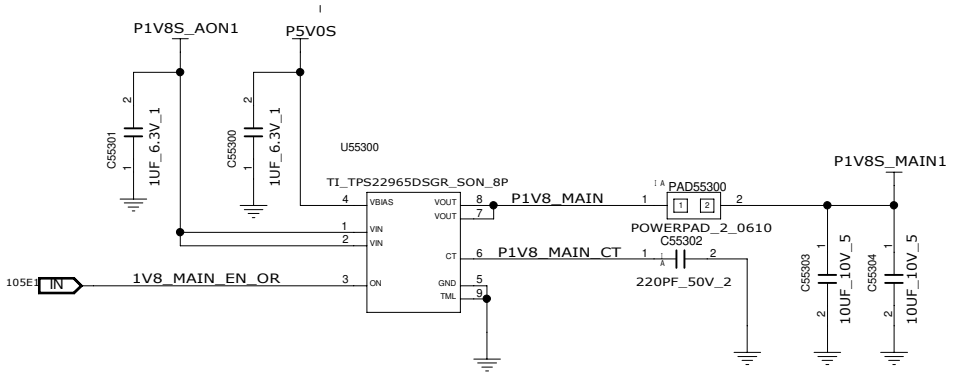
1V8_MAIN



55300 - 55399

CHANGE by	XXX	DATE	21-OCT-2002
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TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

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A3	CS	1310xxxxx-0-0	X01

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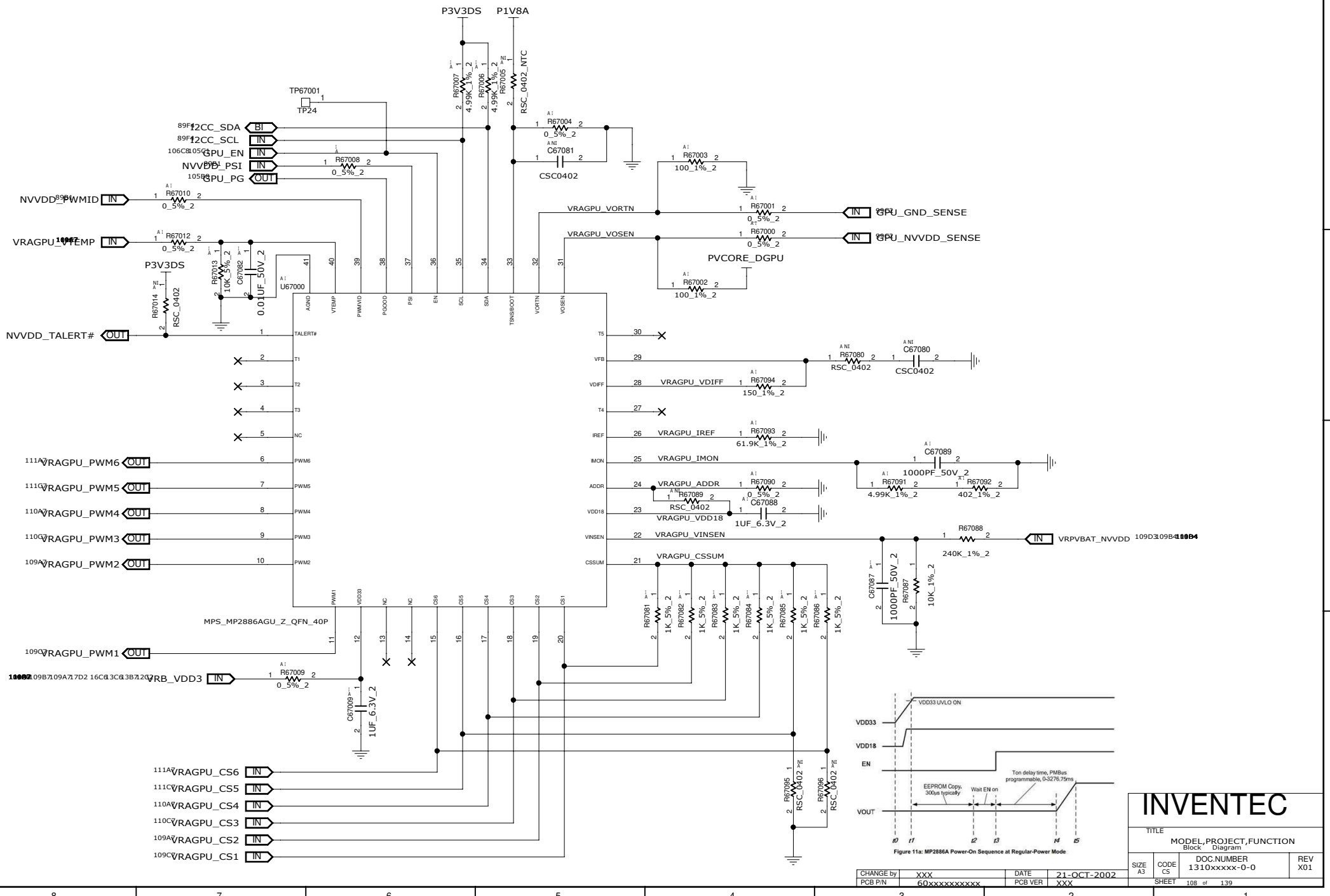

Figure 11a: MP2886A Power-On Sequence at Regular-Power Mode

INVENTEC

TITLE	MODEL,PROJECT,FUNCTION Block Diagram		
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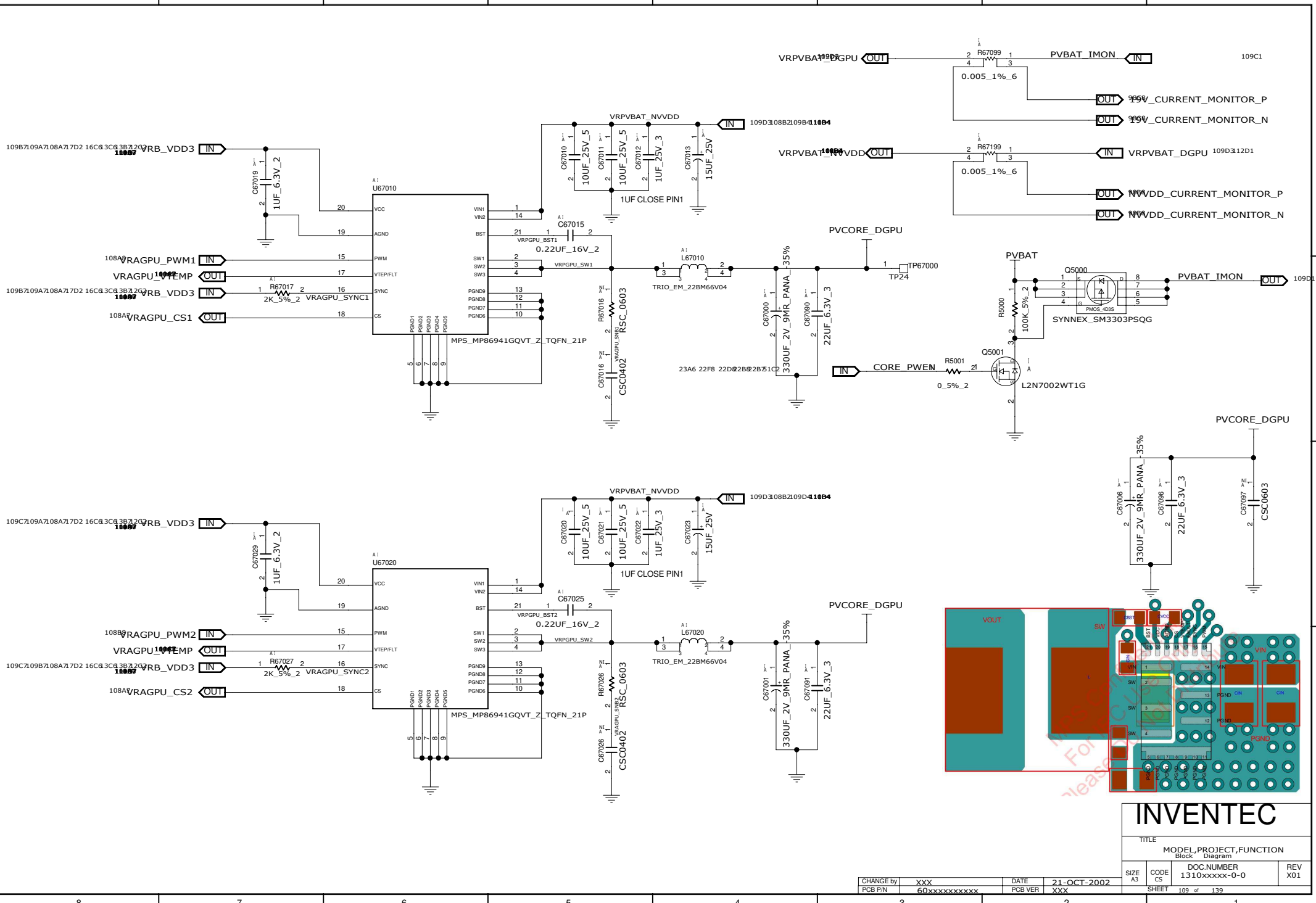
VRPVBAT_DGPU
R67099
PVBAT_IMON
0.005_1%_6
19V_CURRENT_MONITOR_P
19V_CURRENT_MONITOR_N
VRPVBAT_NVVDD
R67199
VRPVBAT_DGPU
NVVDD_CURRENT_MONITOR_P
NVVDD_CURRENT_MONITOR_N
VRB_VDD3
U67010
C67019
1UF_6.3V_2
C67010
C67011
C67012
C67013
10UF_25V_5
1UF_25V_3
15UF_25V
1UF CLOSE PIN1
C67015
0.22UF_16V_2
VRPGPU_BST1
VRPGPU_SW1
L67010
TRIO_EM_22BM66V04
PVCORE_DGPU
TP67000
TP24
PVBAT
Q5000
PMOS_4D3S
SYNNEX_SM3303PSQG
R5000
100K_5%_2
Q5001
L2N7002WT1G
R5001
0_5%_2
CORE_PWEN
VRAGPU_PWM1
VRAGPU_VTEMP
VRAGPU_SYNC1
VRAGPU_CS1
R67017
2K_5%_2
R67016
RSC_0603
C67016
CSC0402
VRAGPU_SW1
MPS_MP86941GQVT_Z_TQFN_21P
C67000
C67090
330UF_2V_9MR_PANA_35%
22UF_6.3V_3
U67020
C67029
C67020
C67021
C67022
C67023
C67025
VRPGPU_BST2
VRPGPU_SW2
L67020
C67001
C67091
R67027
R67026
C67026
VRAGPU_PWM2
VRAGPU_SYNC2
VRAGPU_CS2
C67006
C67096
C67097
CSC0603
VOUT
SW
VIN
PGND
CIN
INVENTEC
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SIZE A3
CODE CS
DOC.NUMBER 1310xxxxx-0-0
REV X01
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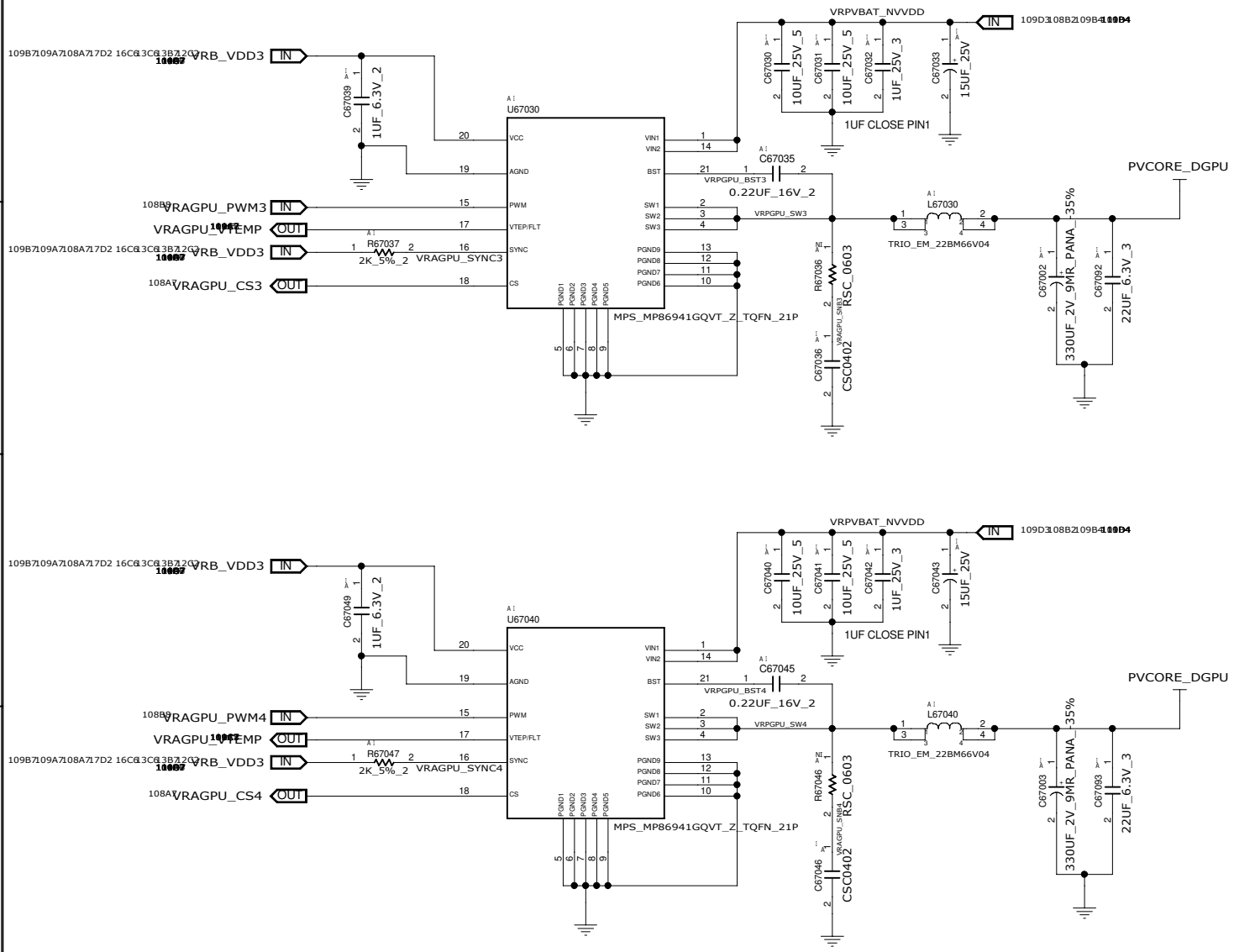
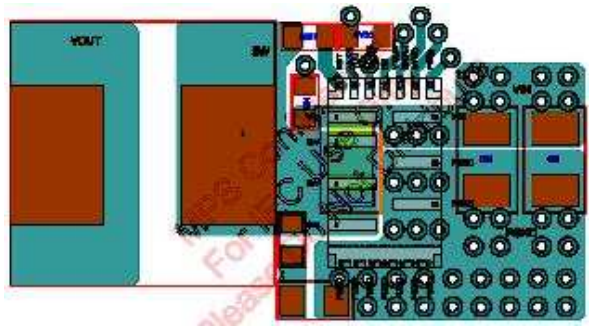
CHANGE by XXX
PCB P/N 60xxxxxxxxxx
DATE 21-OCT-2002
PCB VER XXX





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TITLE	MODEL,PROJECT,FUNCTION Block Diagram
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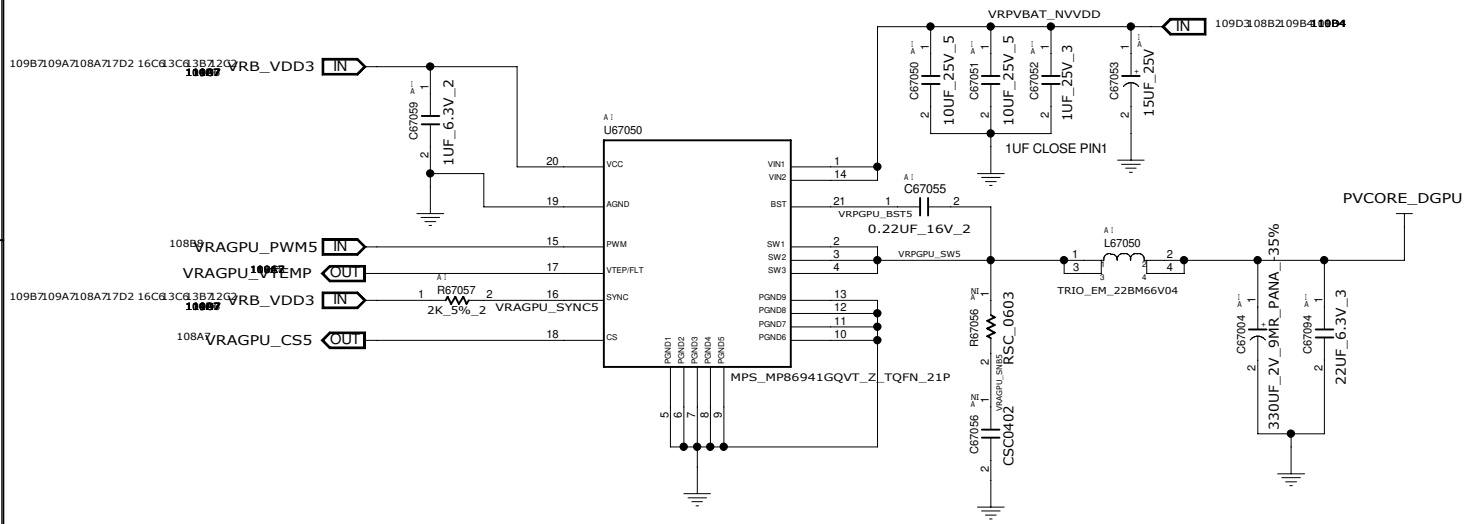

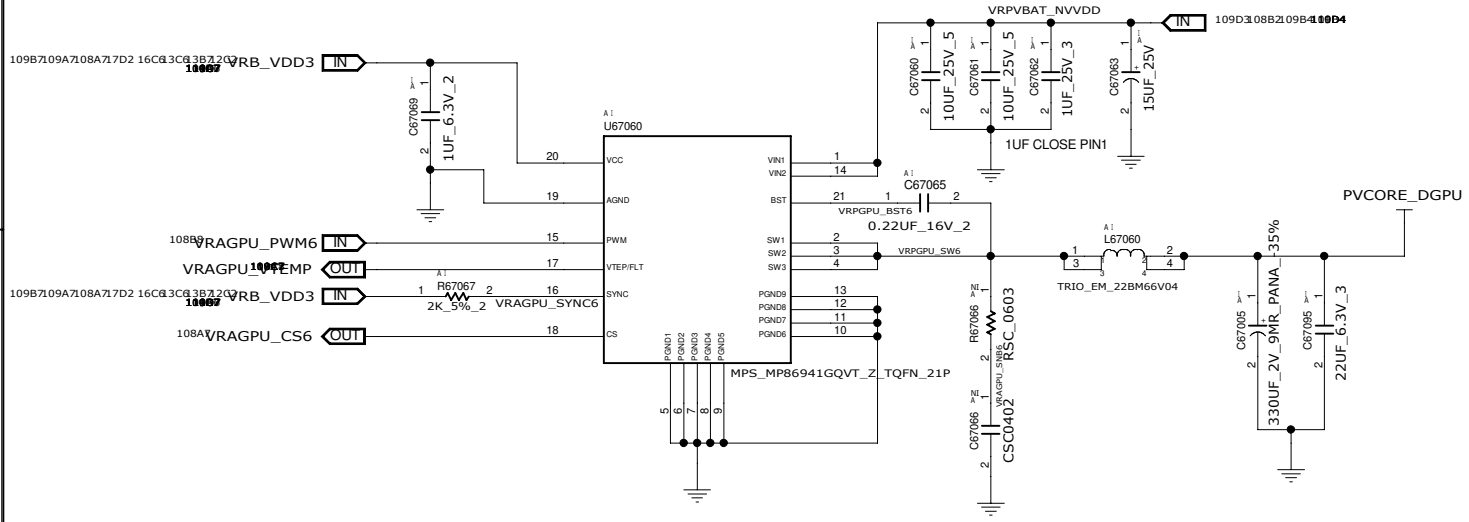

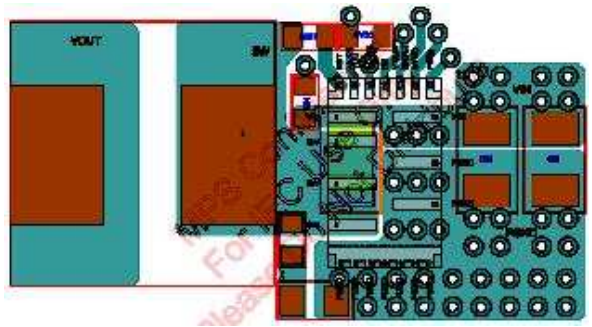

CHANGE by	XXX	DATE	21-OCT-2002
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A3	CS	1310xxxxx-0-0	X01

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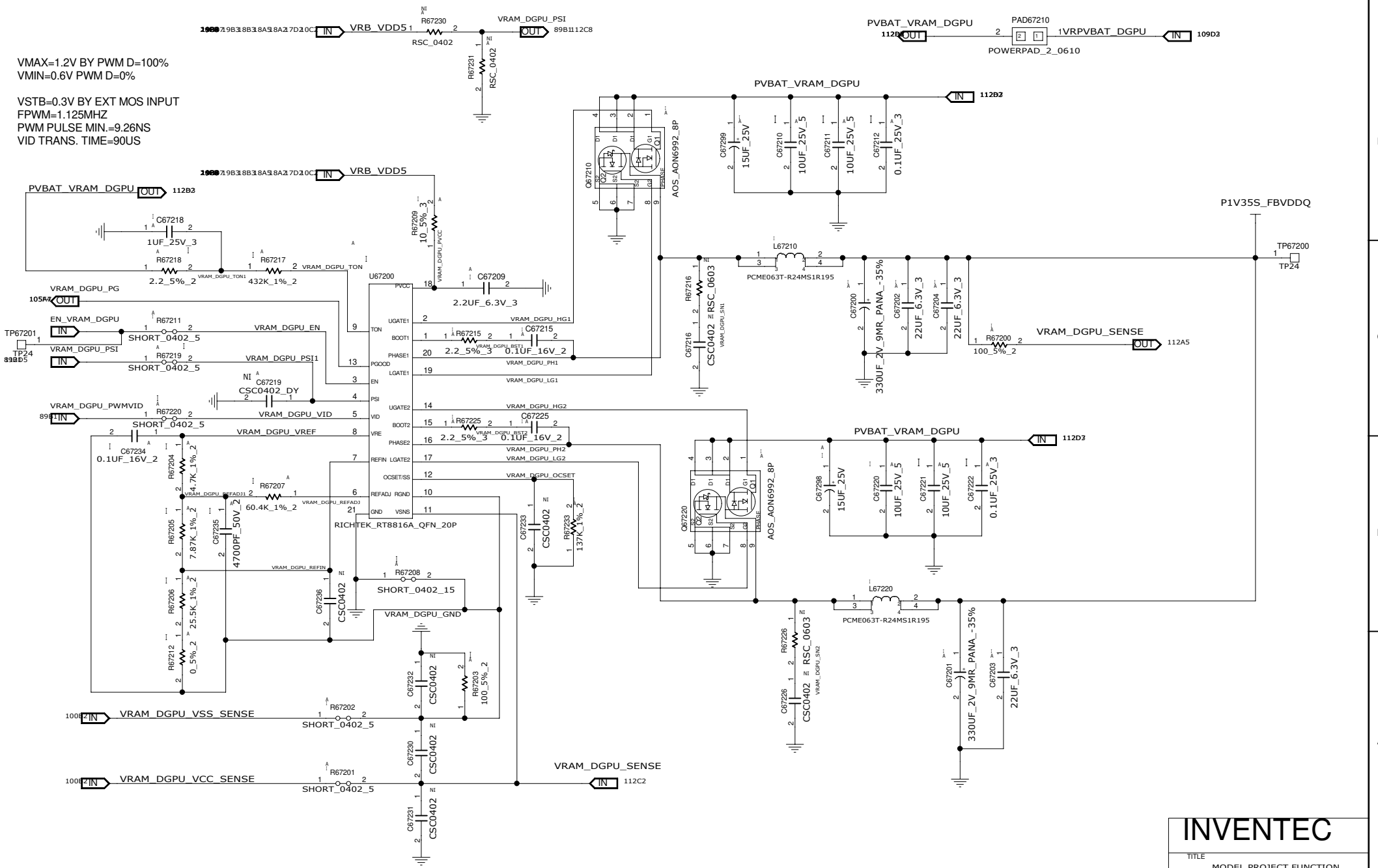

CHANGE by	XXX	DATE	21-OCT-2002
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INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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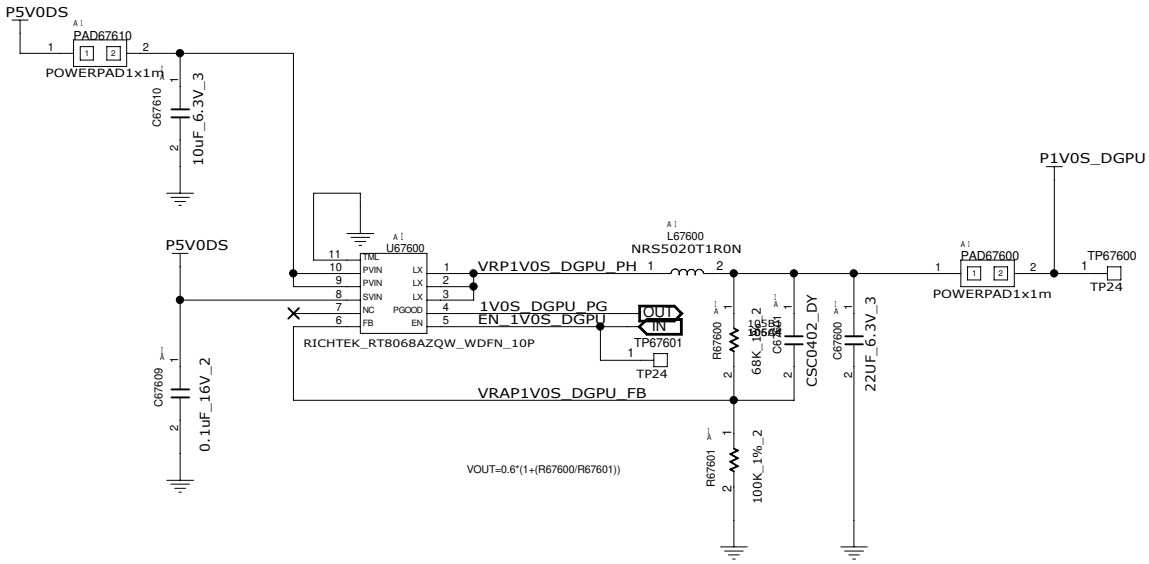

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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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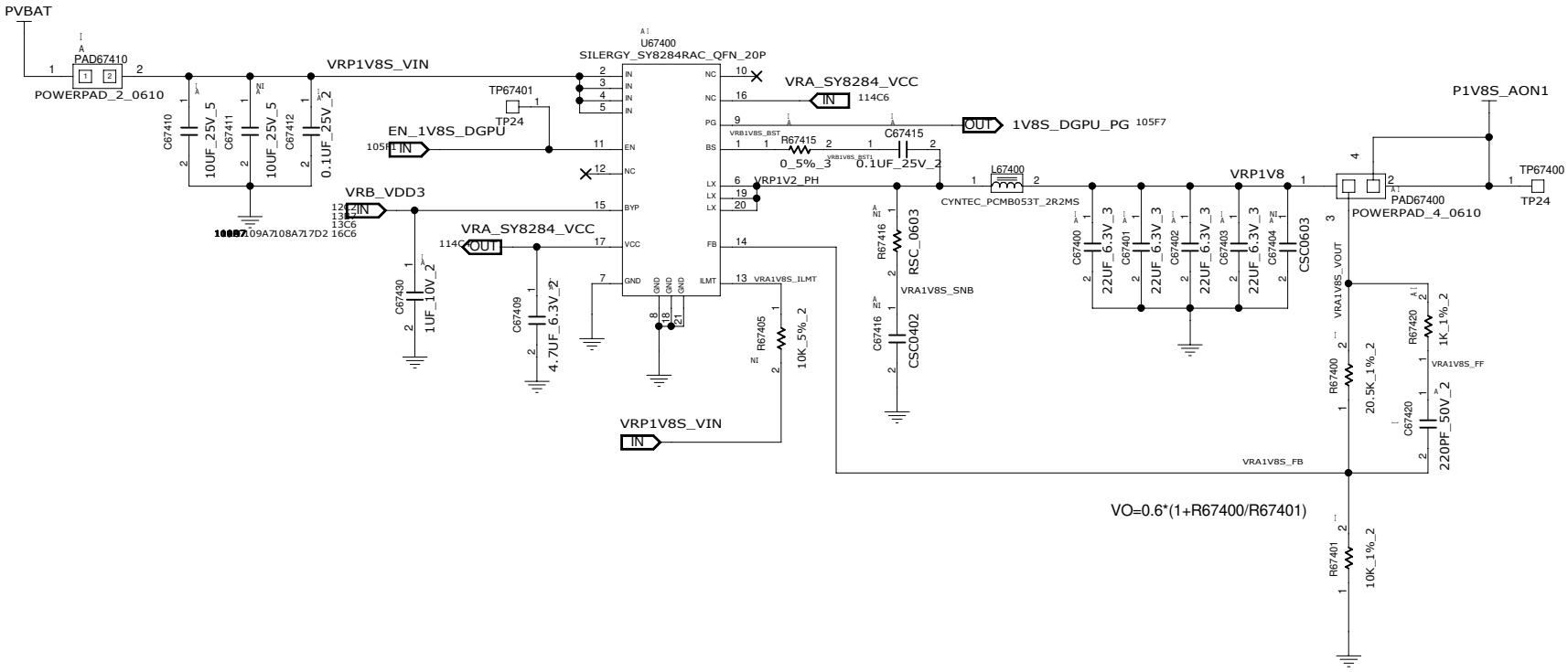

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Input EDPp and EDPc Specifications

Table 11. Input EDPp and EDPc Specification

GPU	Power Source and Input Voltage (V)	Input EDPp (1ms)[2] (A)	Input EDPp (5ms)[2] (A)	Input EDPc (1sec)[1] (W)
N18E-G3	AC adapter (19V)	20	17	150
N18E-G3 MAX-Q	AC adapter (19V)	14	10	80
N18E-G2	AC adapter (19V)	18	15	115
N18E-G2 MAX-Q	AC adapter (19V)	12	10	80
N18E-G1	AC adapter (19V)	12	10	80
N18E-G1 MAX-Q	AC adapter (19V)	10	8	65
N18E-G0	AC adapter (19V)	12	10	80
N18E-G0 MAX-Q	AC adapter (19V)	10	7	60

Notes:

1. Input EDPc current can be calculated with the following equation:

$$Input\ EDPc\ Current\ (A) = \frac{\text{Input EDPc Power (W)}}{\text{Input Voltage (V)}}$$

2. Input EDPp current at different input voltage can be calculated with the following equation:

$$Input\ EDPp\ (A) at\ V_{new} = Input\ EDPp(A)\ at\ 19V x\ \frac{19V}{V_{new}(V)}$$

Table 12. Output EDP-Continuous

Product	TGP (W)	NVVDD — (A)	FB TOTAL[5] 1.35V[3, 4] (A)	1.0V Total[1] 1.0V[3] (A)	1.8V Total[2] 1.8V[3] (A)
N18E-G3	150	144	46	1.6	2.3
	160	152			
	170	160			
	180	168			
	190	175			
	200	180			
N18E-G3 MAX-Q	80	84	40	1.6	2.3
N18E-G2	115	116	46	1.6	2.3
N18E-G2 MAX-Q	80	84	40	1.6	2.3
N18E-G1	80	82	35	1.6	2.3
N18E-G1 MAX-Q	65	68	30	1.6	2.3
N18E-G0	80	82	35	1.6	2.3
N18E-G0 MAX-Q	60	63	30	1.6	2.3

Table 14. Output EDP-Peak

Product	TGP (W)	NVVDD - (A)	FB TOTAL[4] 1.35V[2, 3] (A)	1.0V Total[1] 1.0V[2] (A)	1.8V Total[2] 1.8V[5] (A)
N18E-G3	150	450	63	2.20	3.8
N18E-G3 MAX-Q	80	300	54	2.20	3.8
N18E-G2	115	375	63	2.20	3.8
N18E-G2 MAX-Q	80	300	54	2.20	3.8
N18E-G1	80	225	47	2.20	3.8
N18E-G1 MAX-Q	65	225	40	2.20	3.8
N18E-G0	80	225	47	2.20	3.8

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A3	CS	1310xxxxx-0-0	X01

HISTORY

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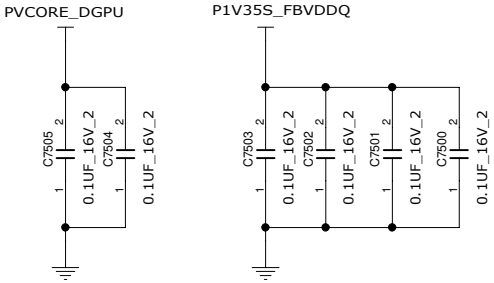
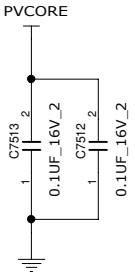
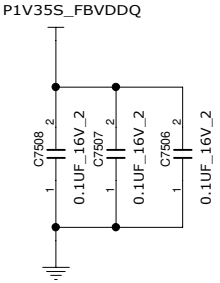
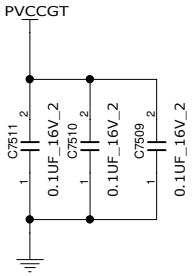
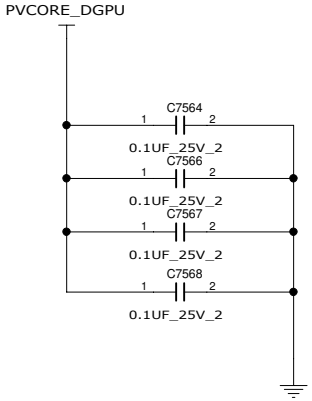
EMI

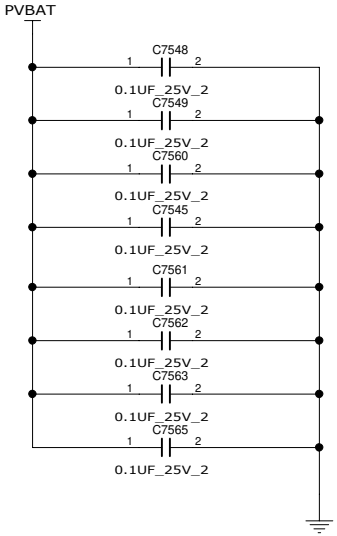


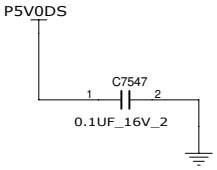


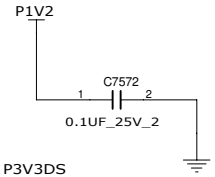


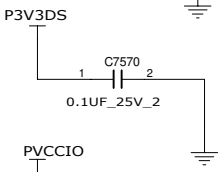


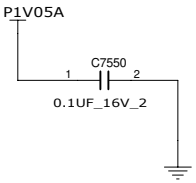


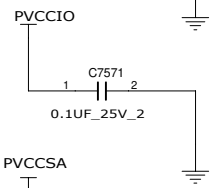


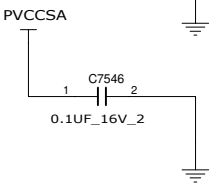


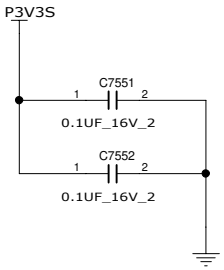












CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
NFC CNNN.

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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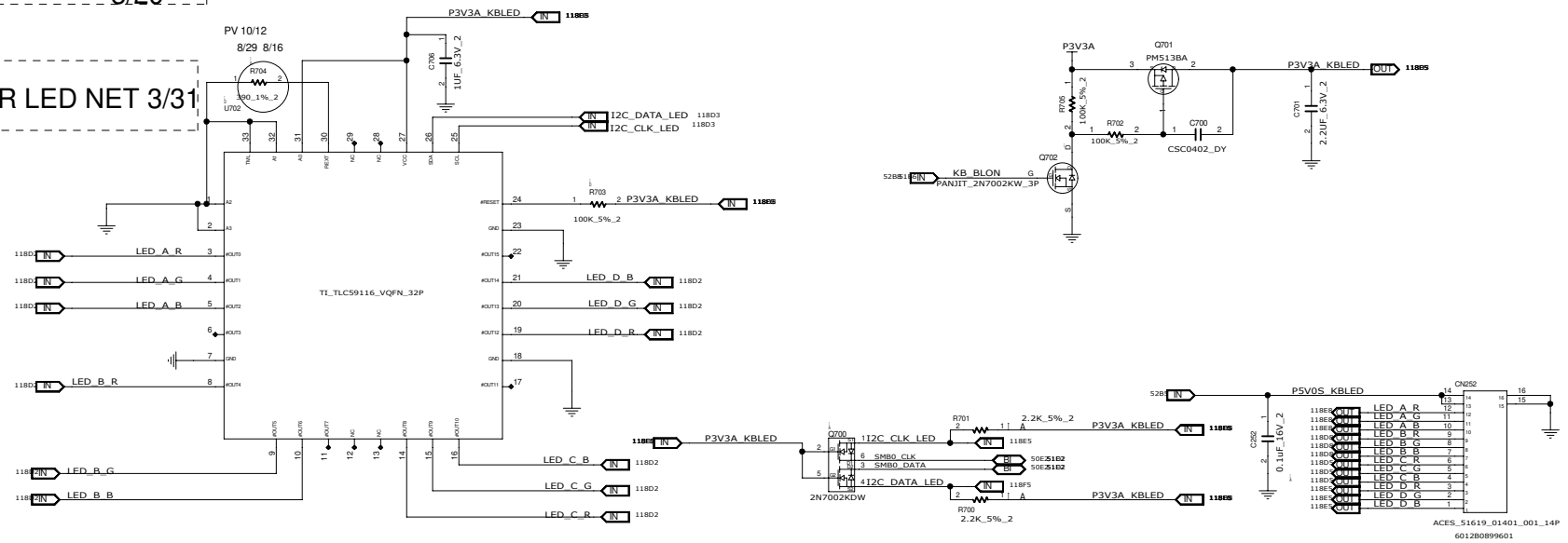
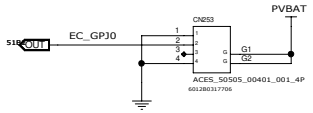
ADJUST LED RES 8/16
8/29

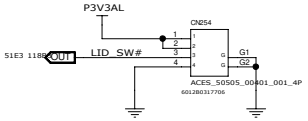
RE-ORDER LED NET 3/31

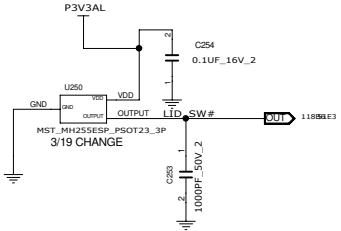


TURBO#



HALL_SENSOR





REFERENCE NUMBER:700~800

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
RING LED

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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TURBO# BOARD

CHANGE by	XXX
PCB P/N	60xxxxxxxxxx
DATE	21-OCT-2002
PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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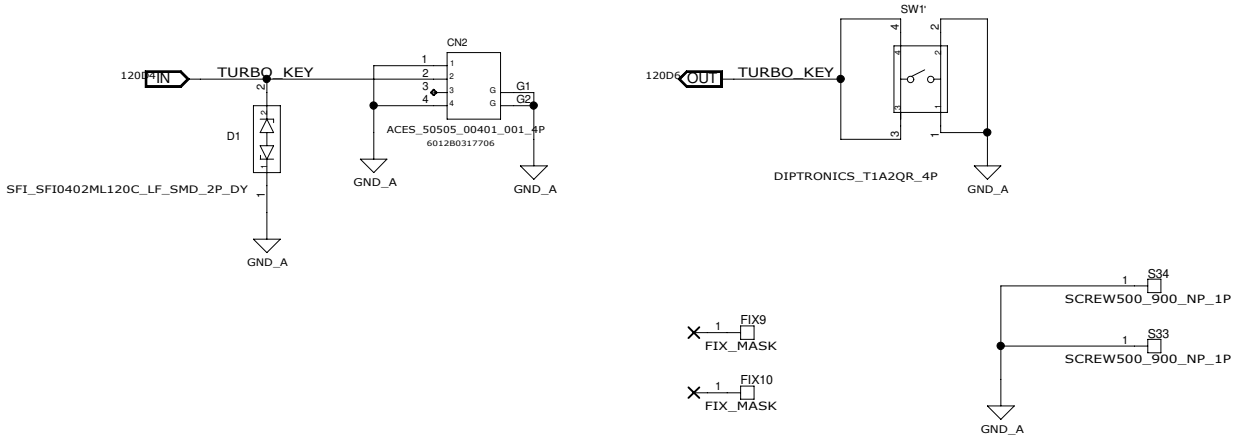
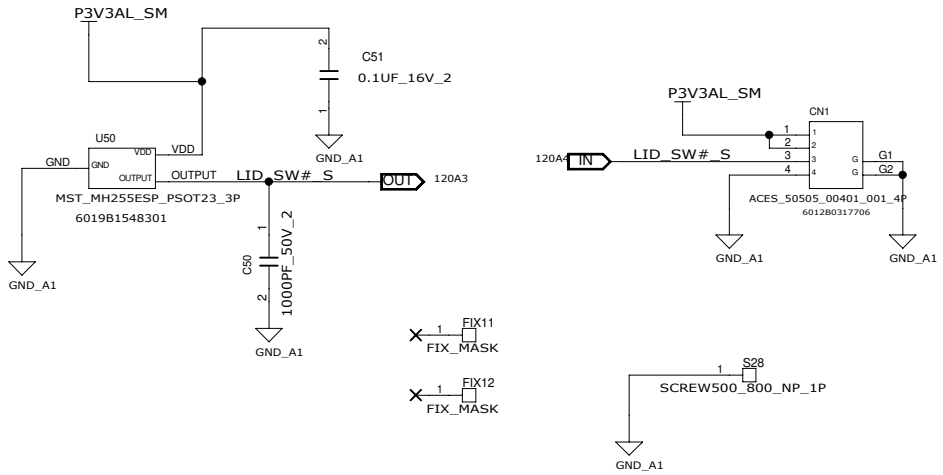
TURBO#



HALL_SENSOR



INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

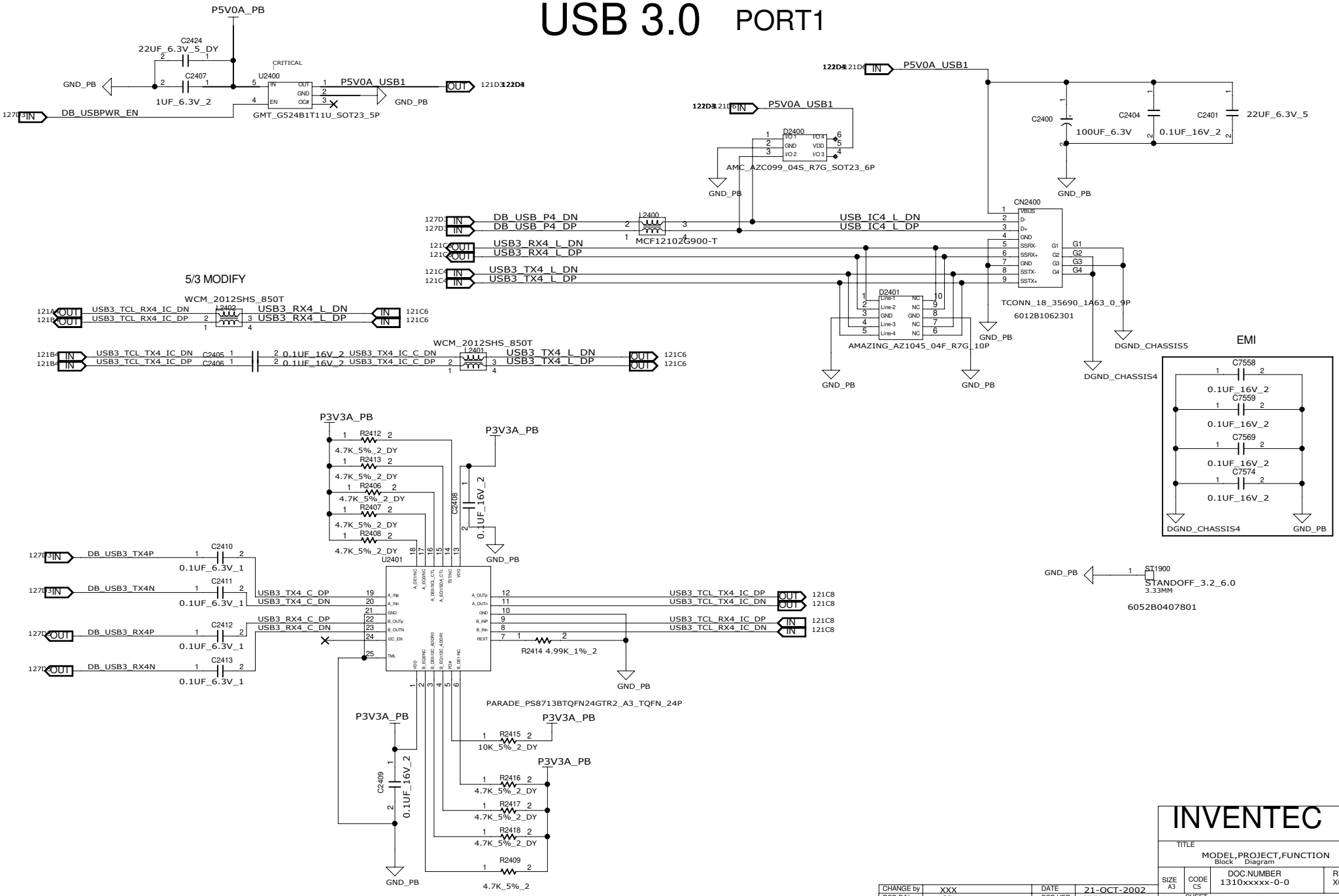
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 120 of 139

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

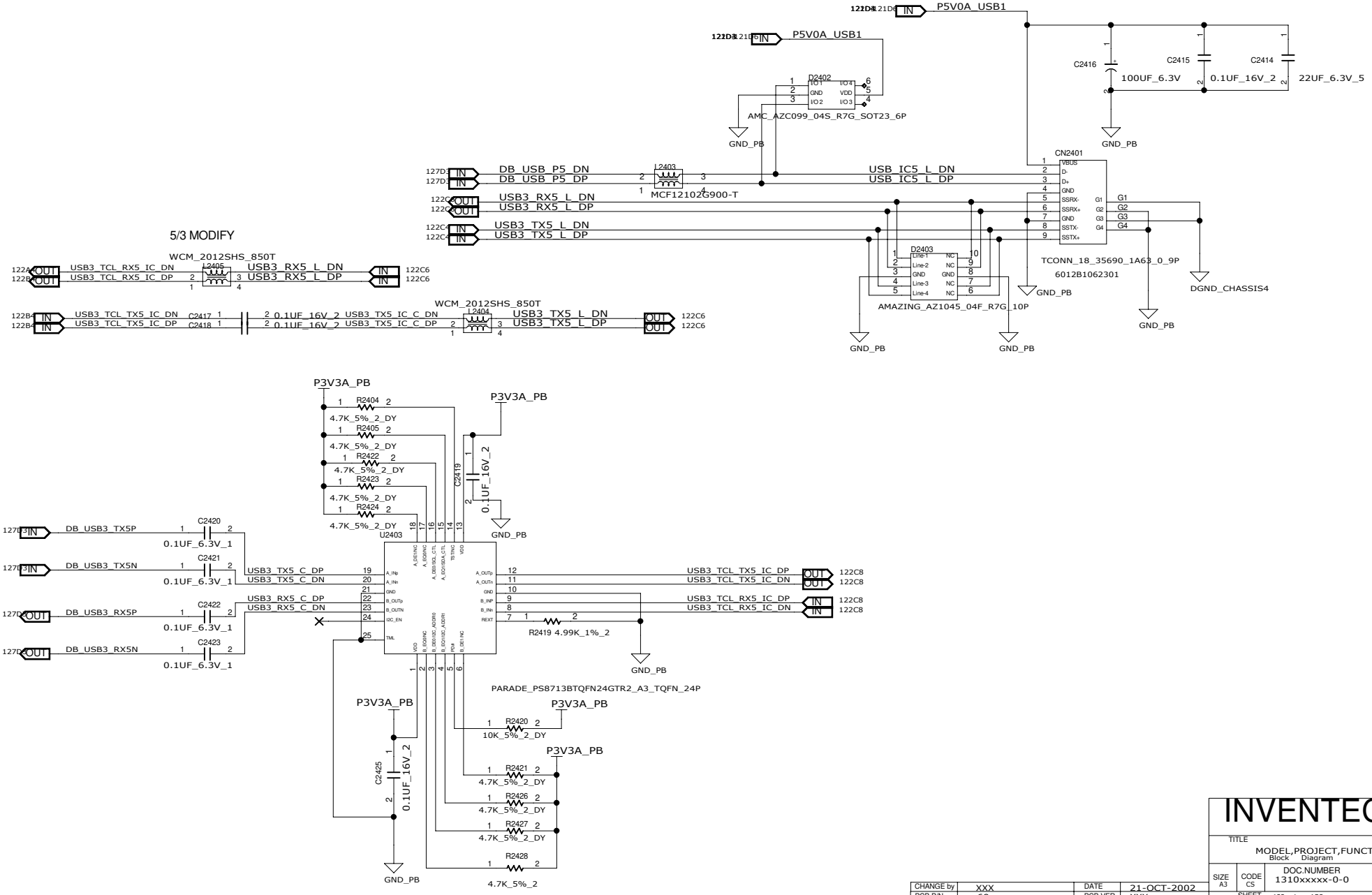
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 121 of 139

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT2



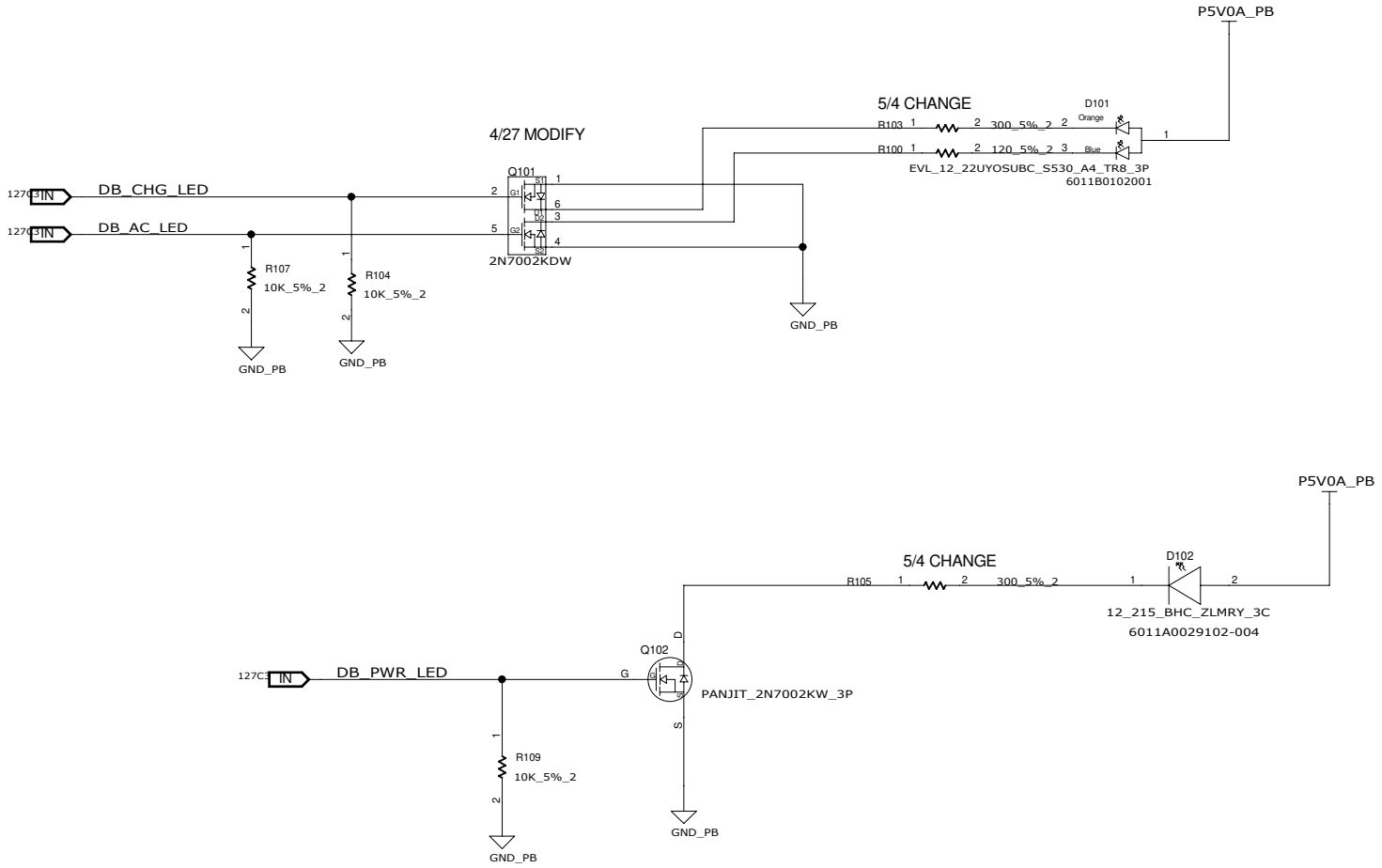
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 122 of 139



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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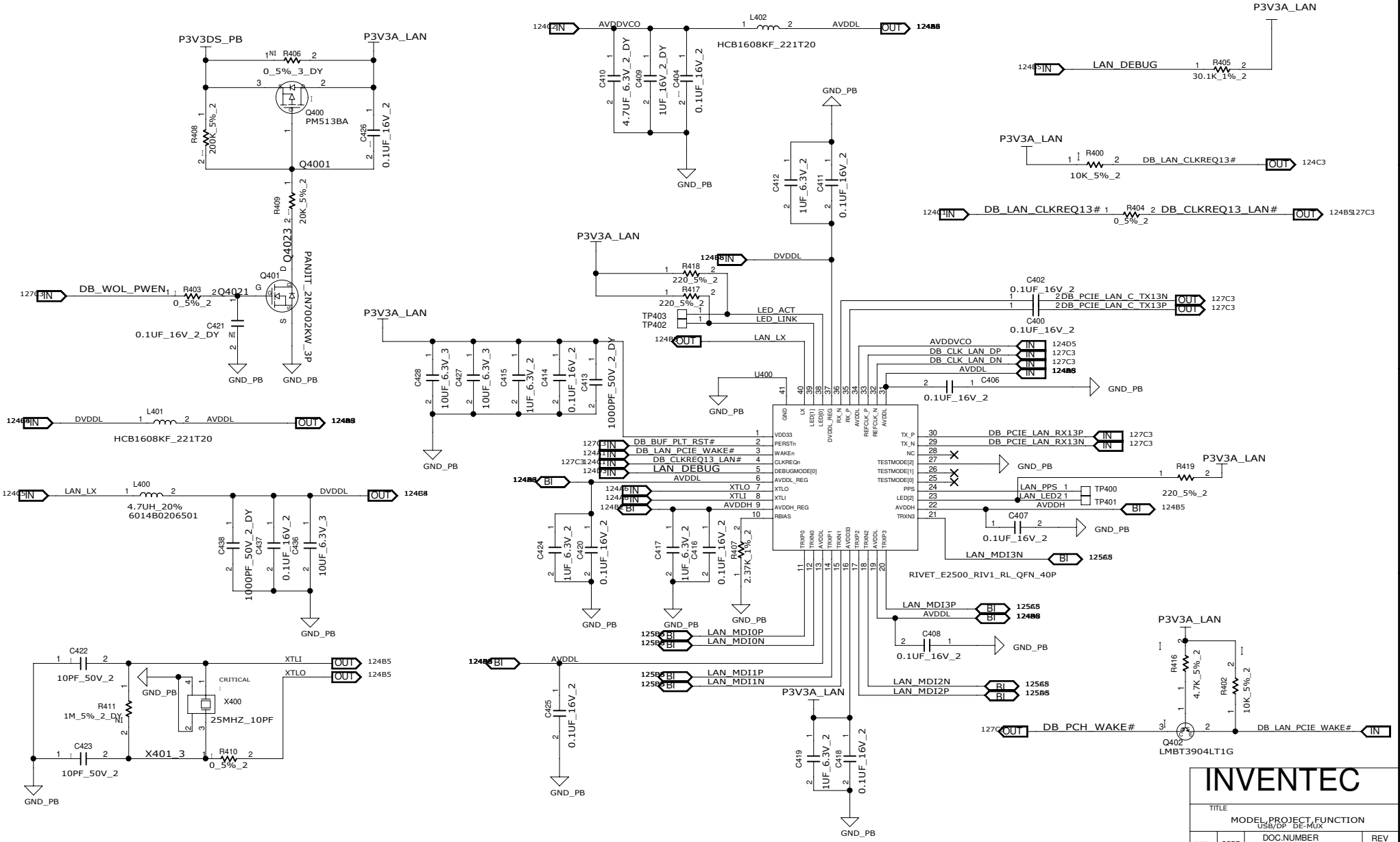
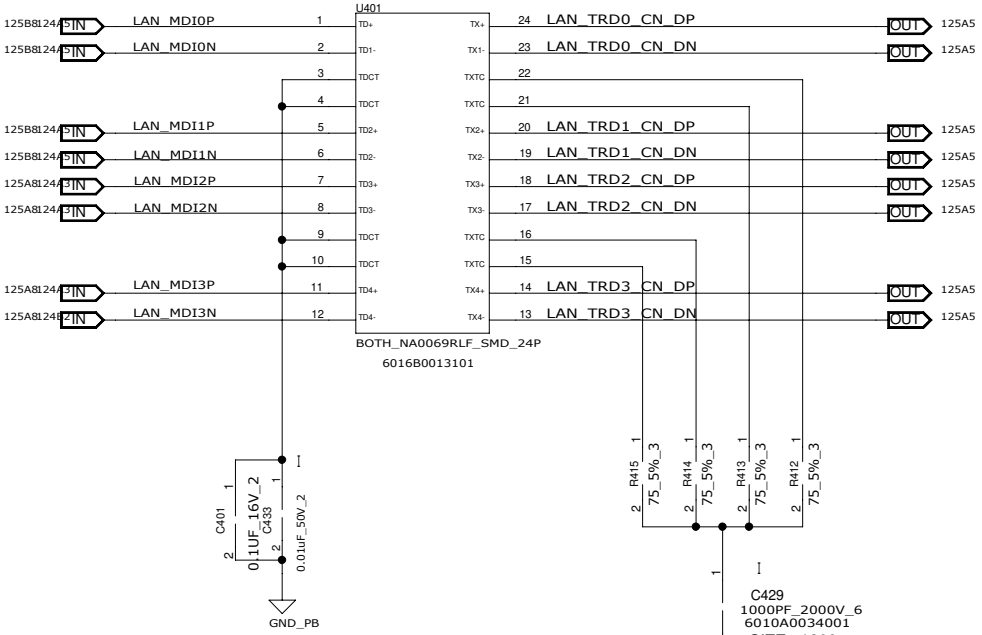
LAN (CONTROLLER)
E2500



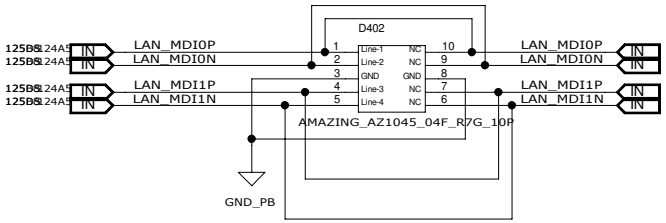
INVENTEC

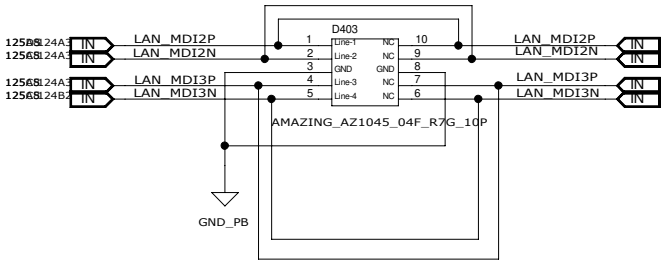
TITLE: MODEL_PROJECT_FUNCTION (USB/DP DE-MUX)					
CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	DOC.NUMBER 1310xxxxx-0-0
PCB P/N	60xxxxxxxxx	PCB VER	XXX	CODE CS	REV X01
				SHEET	124 of 139

TRANSFORMER

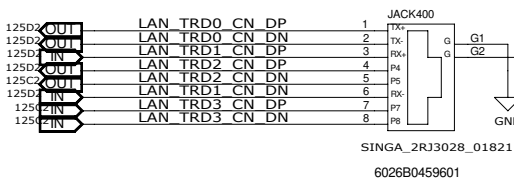


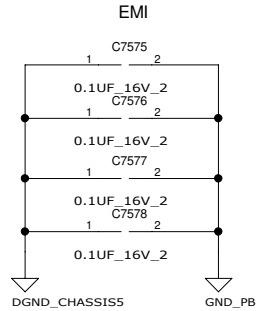
ESD





RJ-45





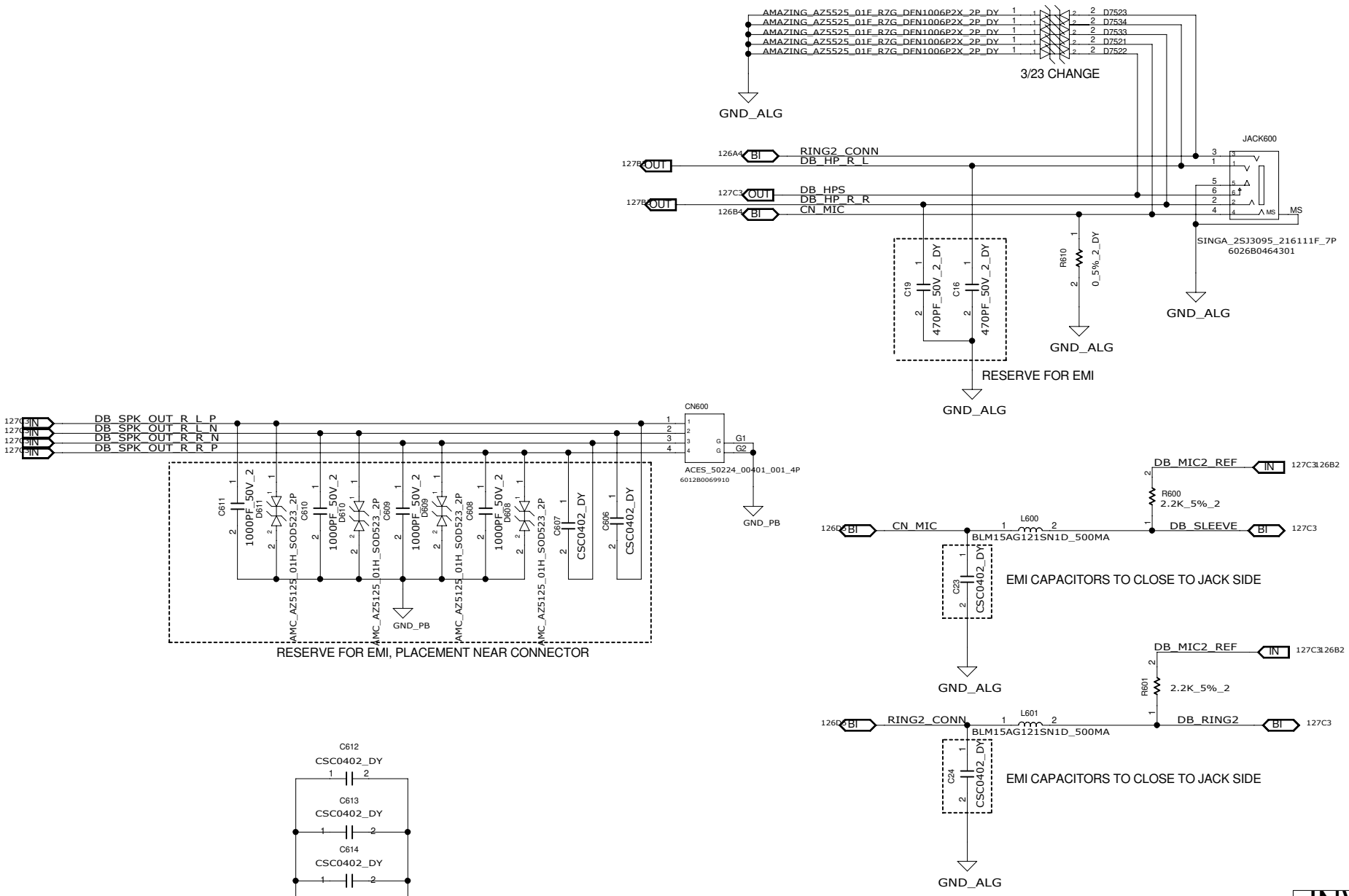
CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 125 of 139



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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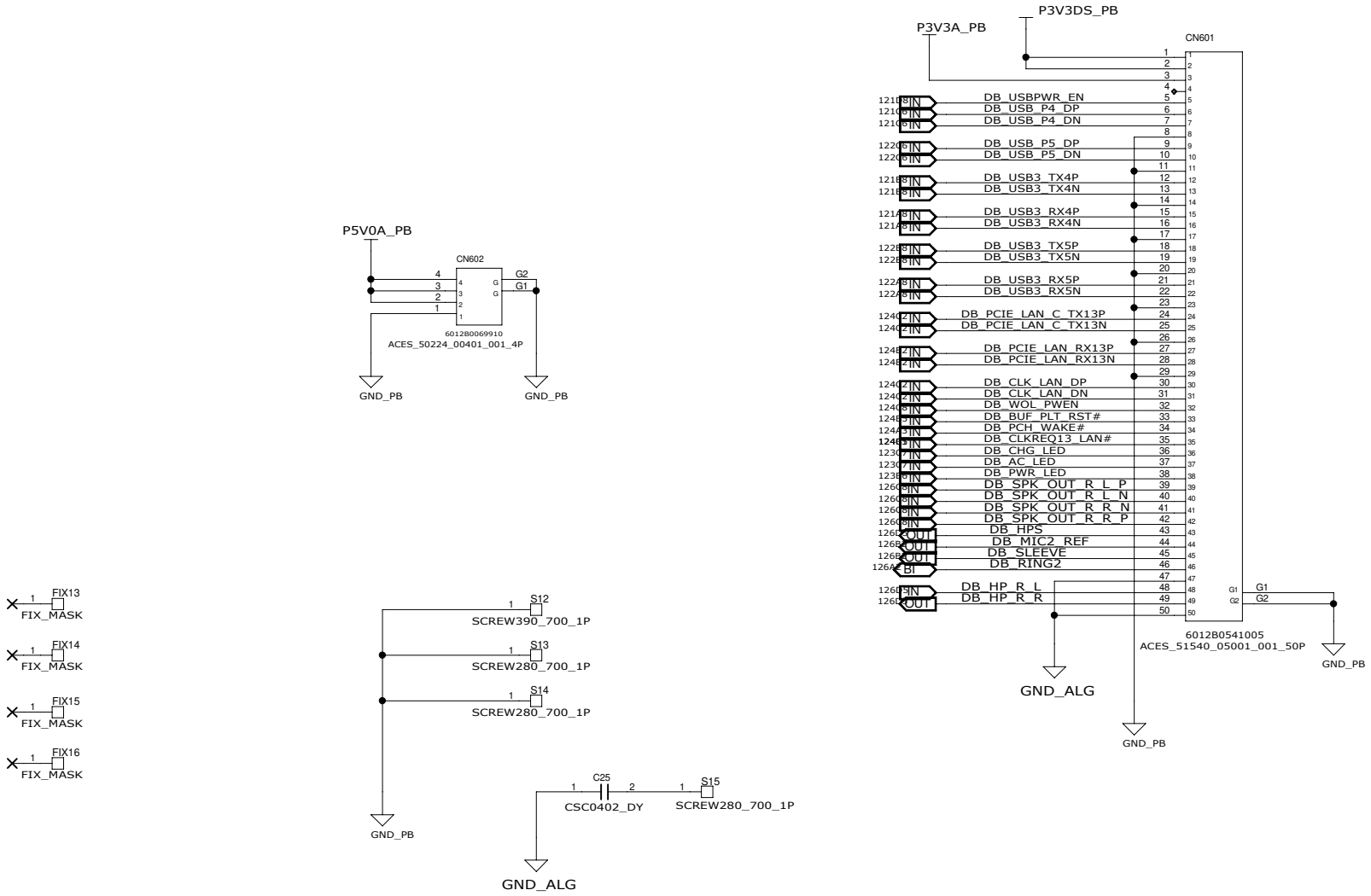

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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FOR 17 SMALL BOARD

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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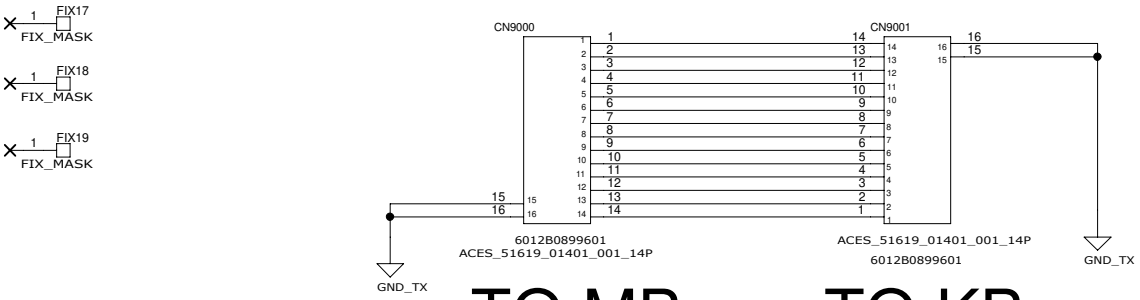
6050A3090601



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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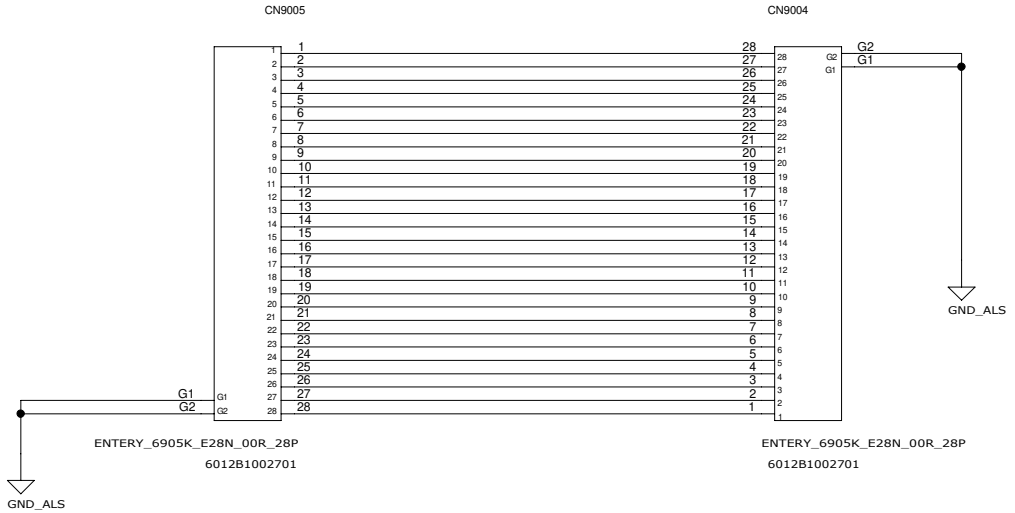
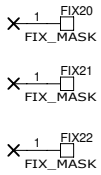
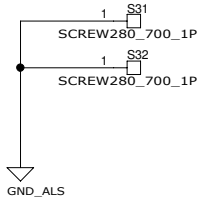
6050A3090501



TO MB

TO KB





INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX

FOR 15 AUDIO BOARD

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

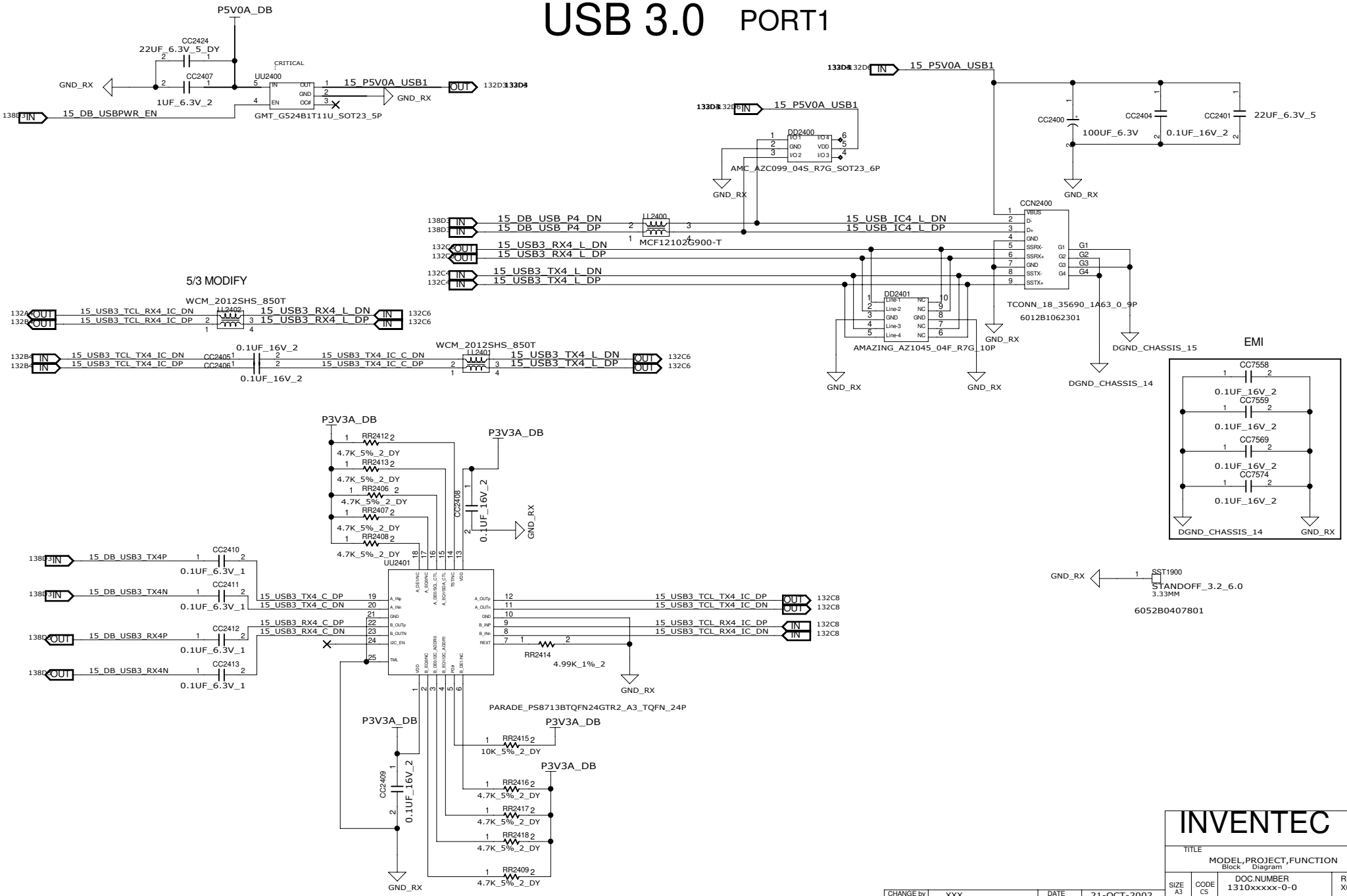
TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 131 of 139

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT1



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

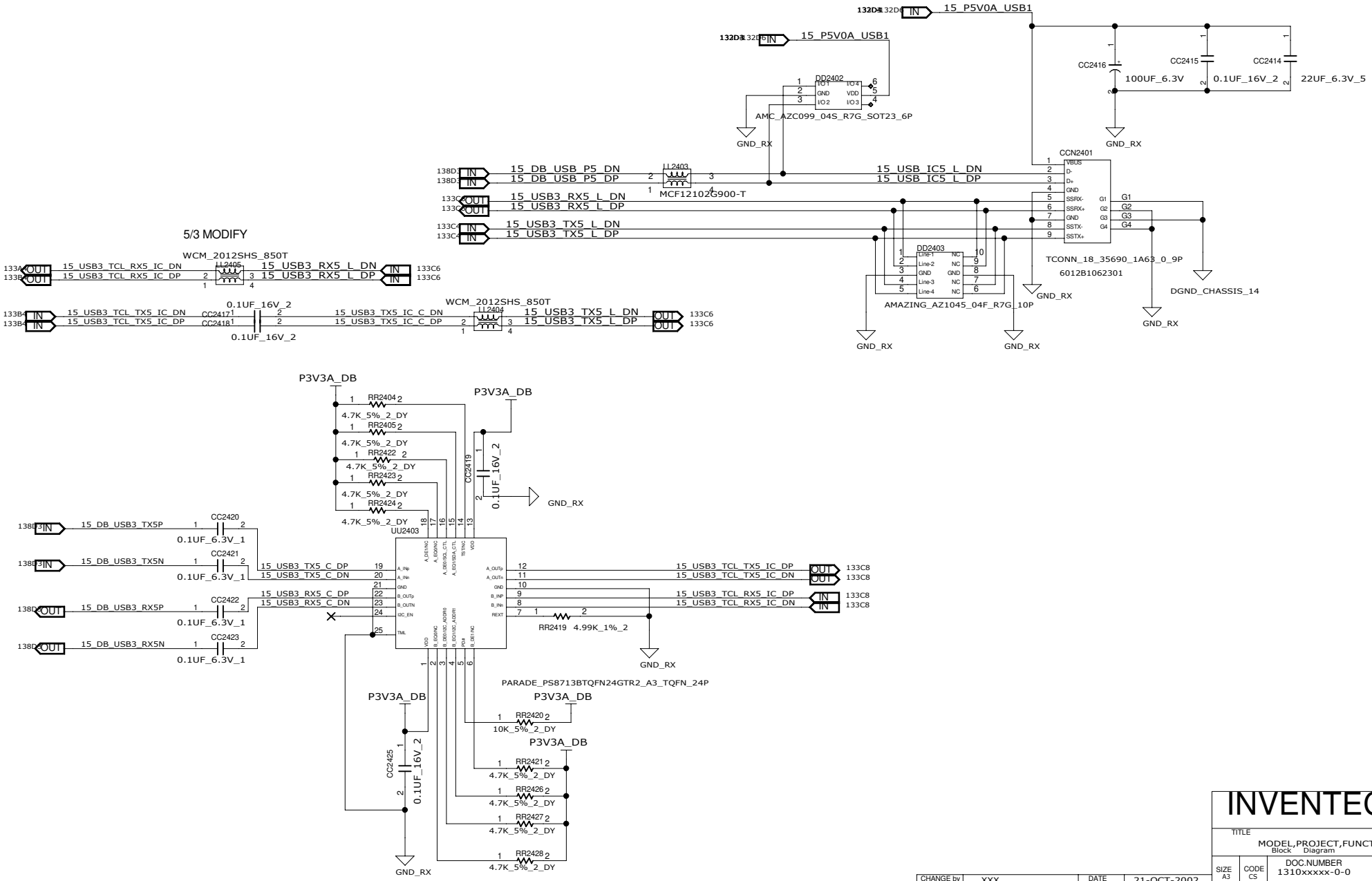
TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 132 of 139

REFERENCE 2400~2450(USB3.0)

USB 3.0 PORT2



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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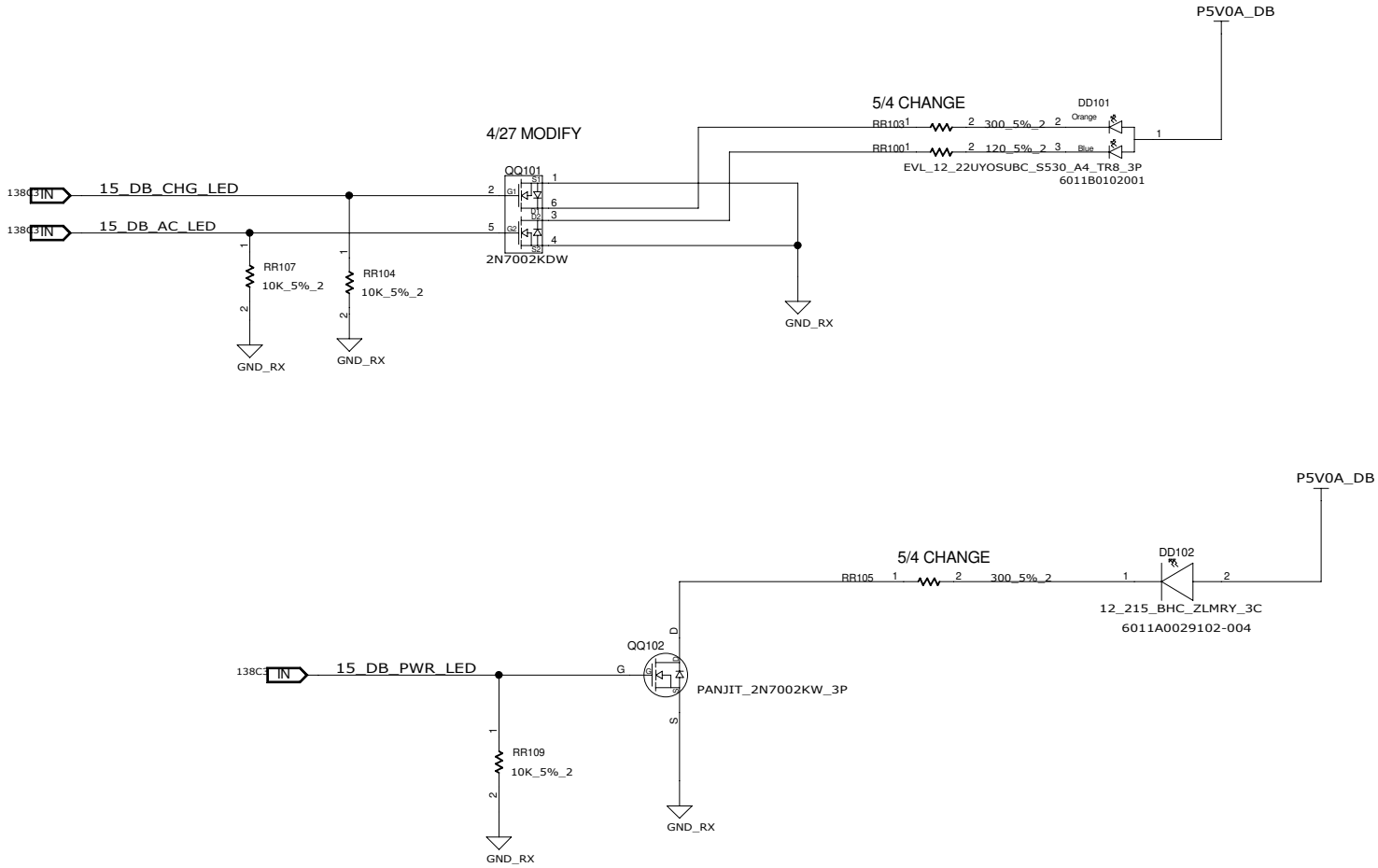


CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

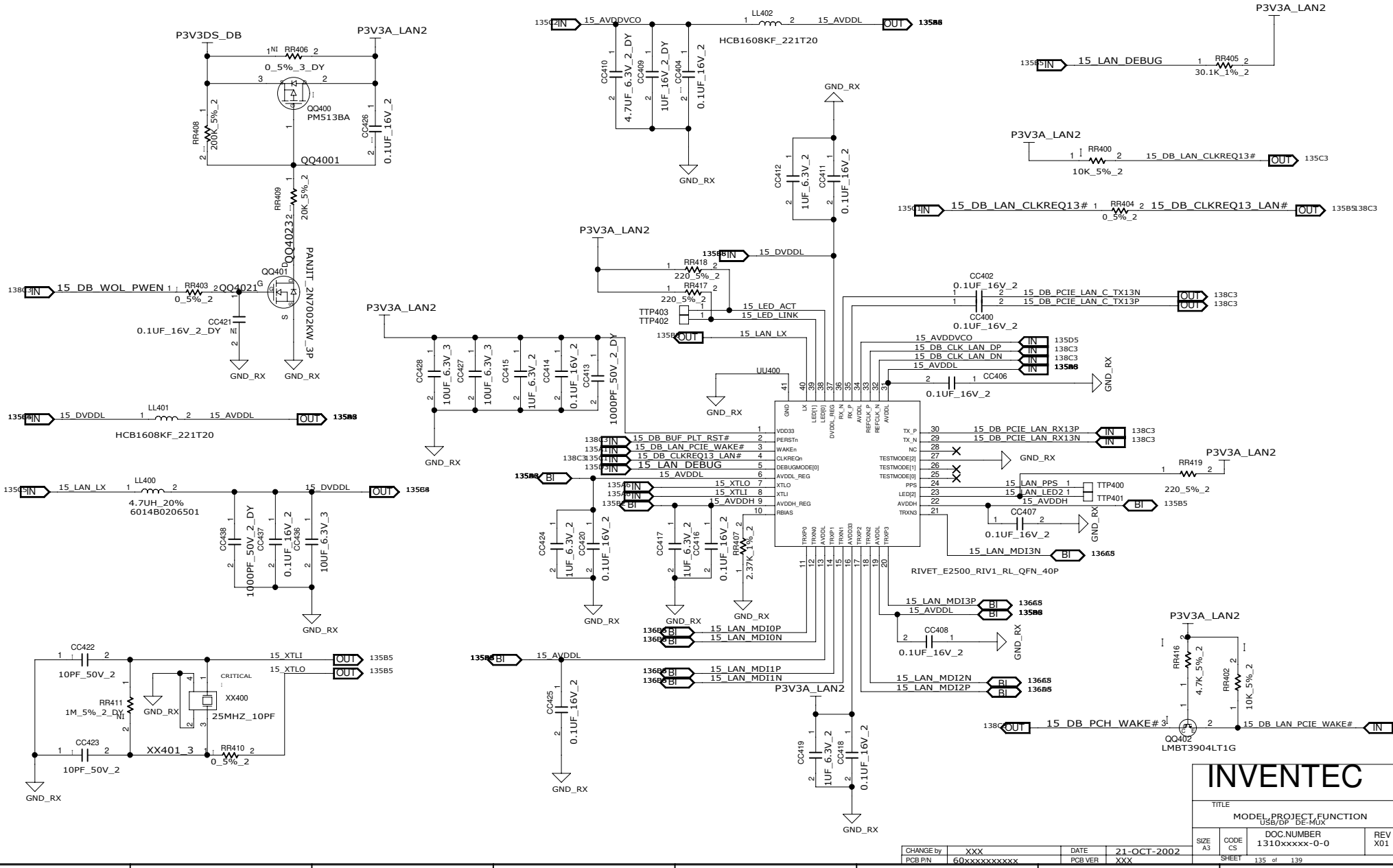
INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 134 of 139

LAN (CONTROLLER)
E2500

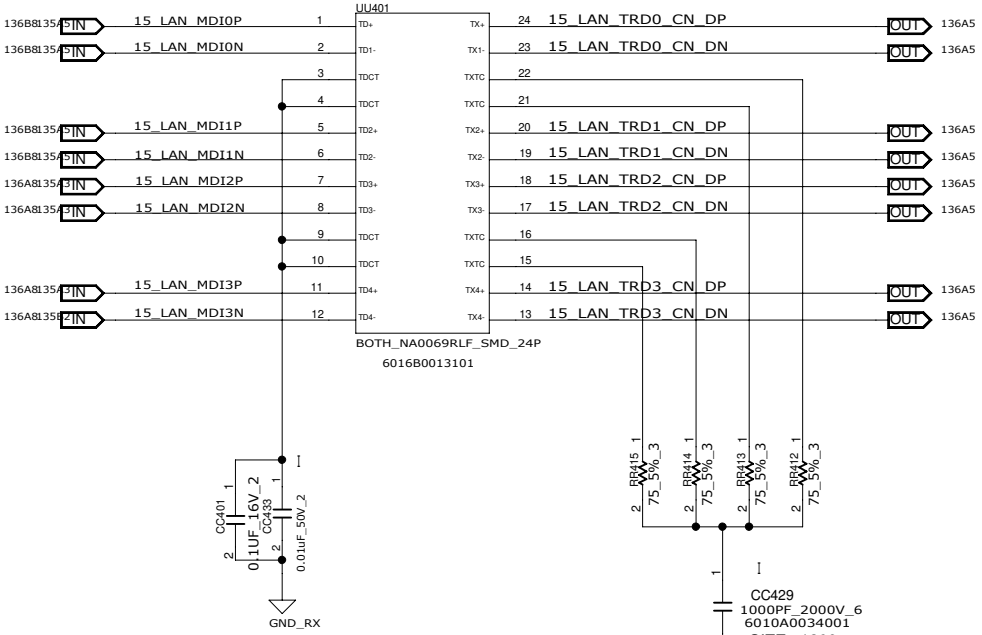


INVENTEC

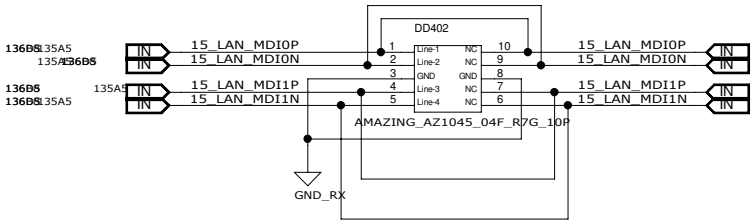
TITLE: MODEL_PROJECT_FUNCTION
USB/DP DE-MUX

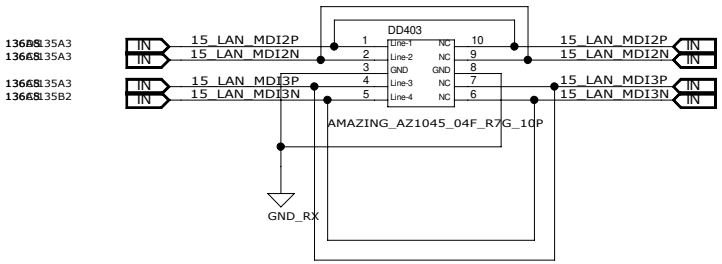
CHANGE by	XXX	DATE	21-OCT-2002	SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
PCB P/N	60xxxxxxxxx	PCB VER	XXX			SHEET 135 of 139	

TRANSFORMER

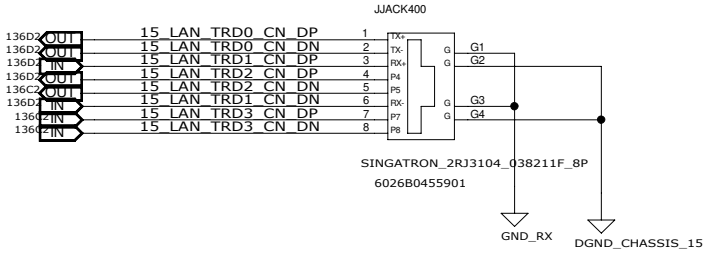


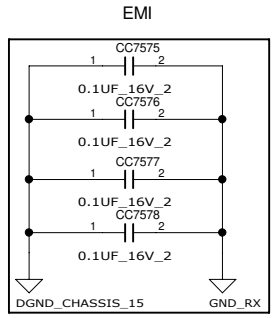
ESD





RJ-45





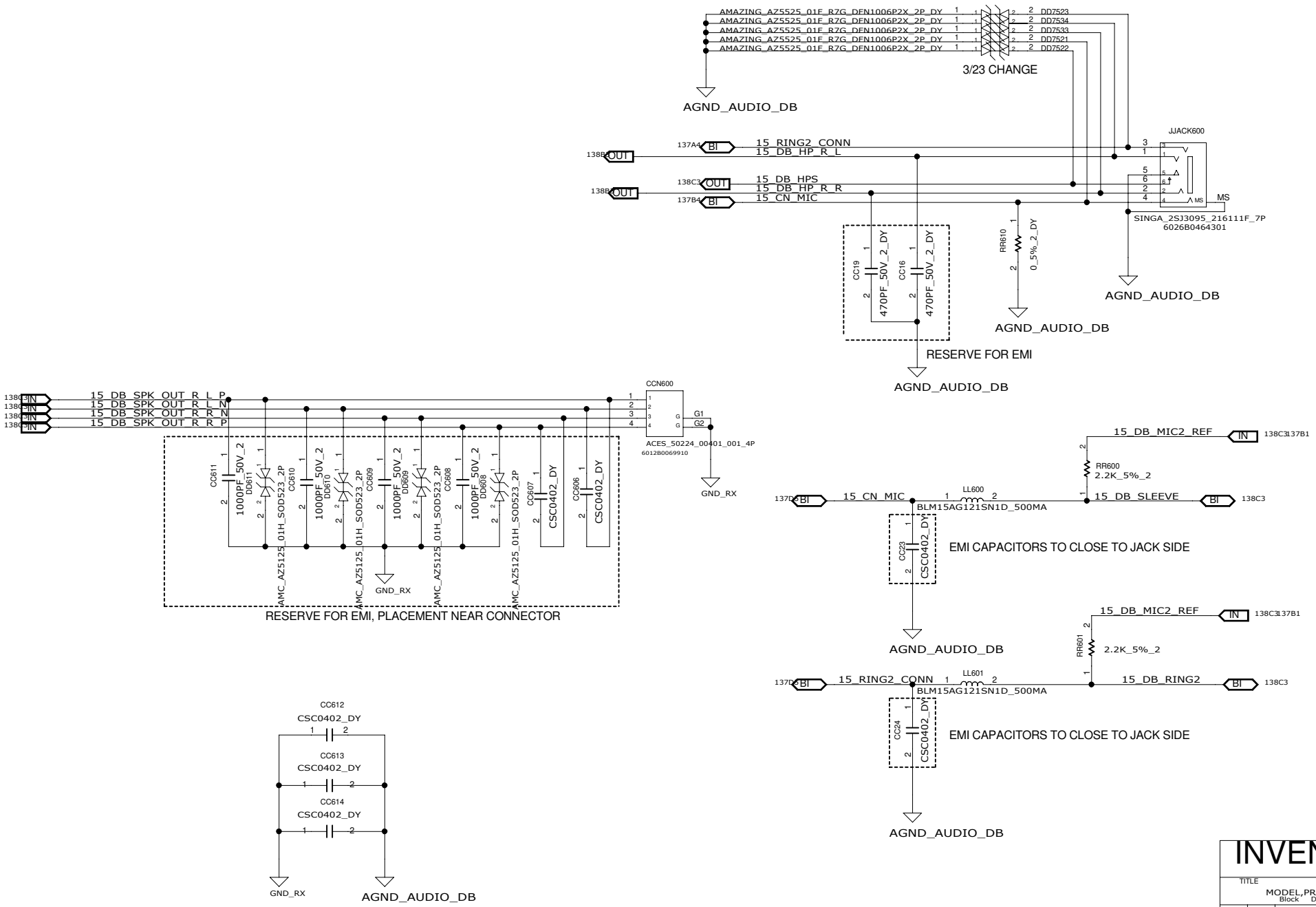
INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

SHEET 136 of 139

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxx	PCB VER	XXX



CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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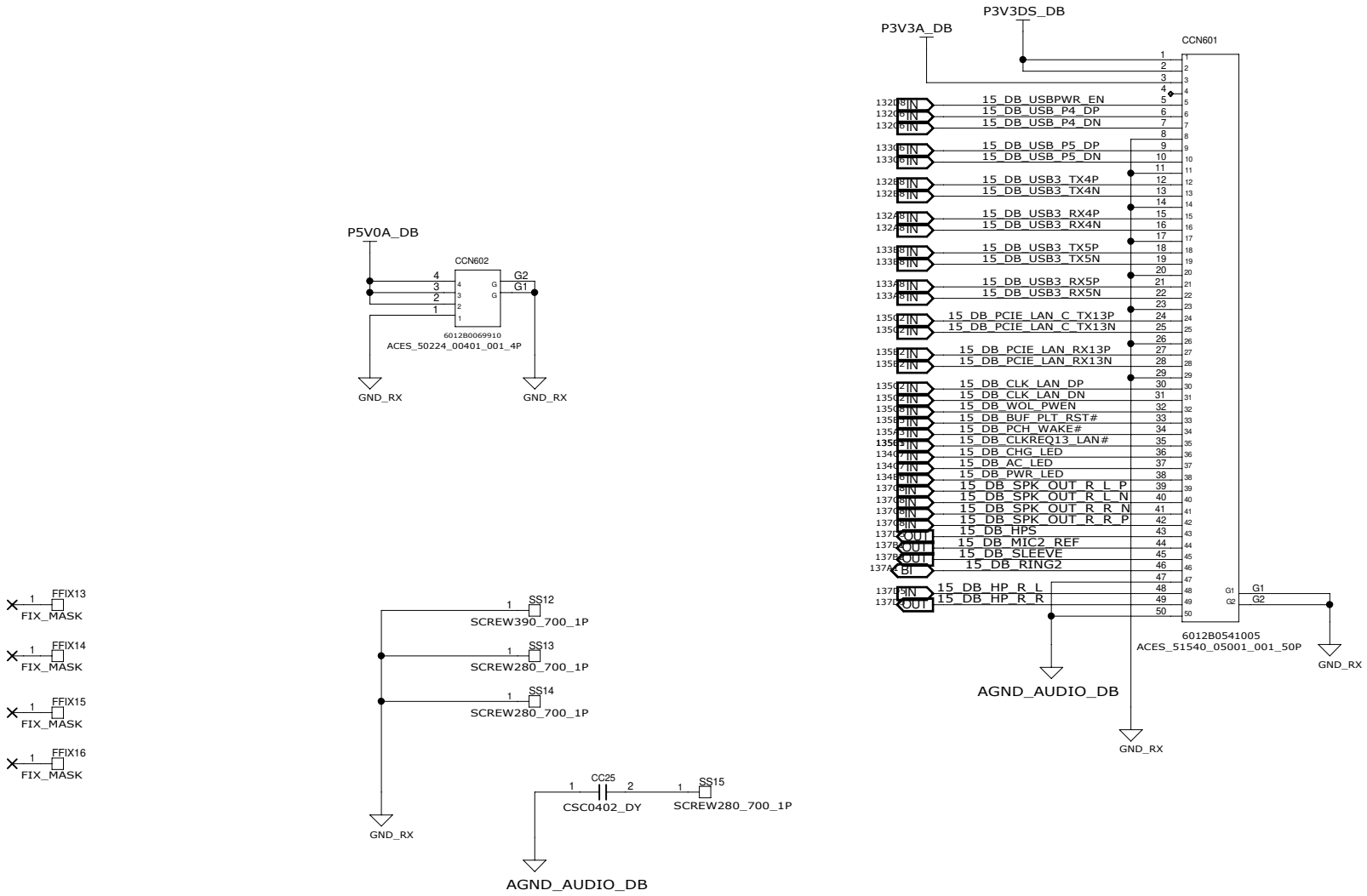

INVENTEC

TITLE: MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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INVENTEC

TITLE
MODEL,PROJECT,FUNCTION
Block Diagram

CHANGE by	XXX	DATE	21-OCT-2002
PCB P/N	60xxxxxxxxxx	PCB VER	XXX

SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxxx-0-0	X01

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