

P1314\_A00

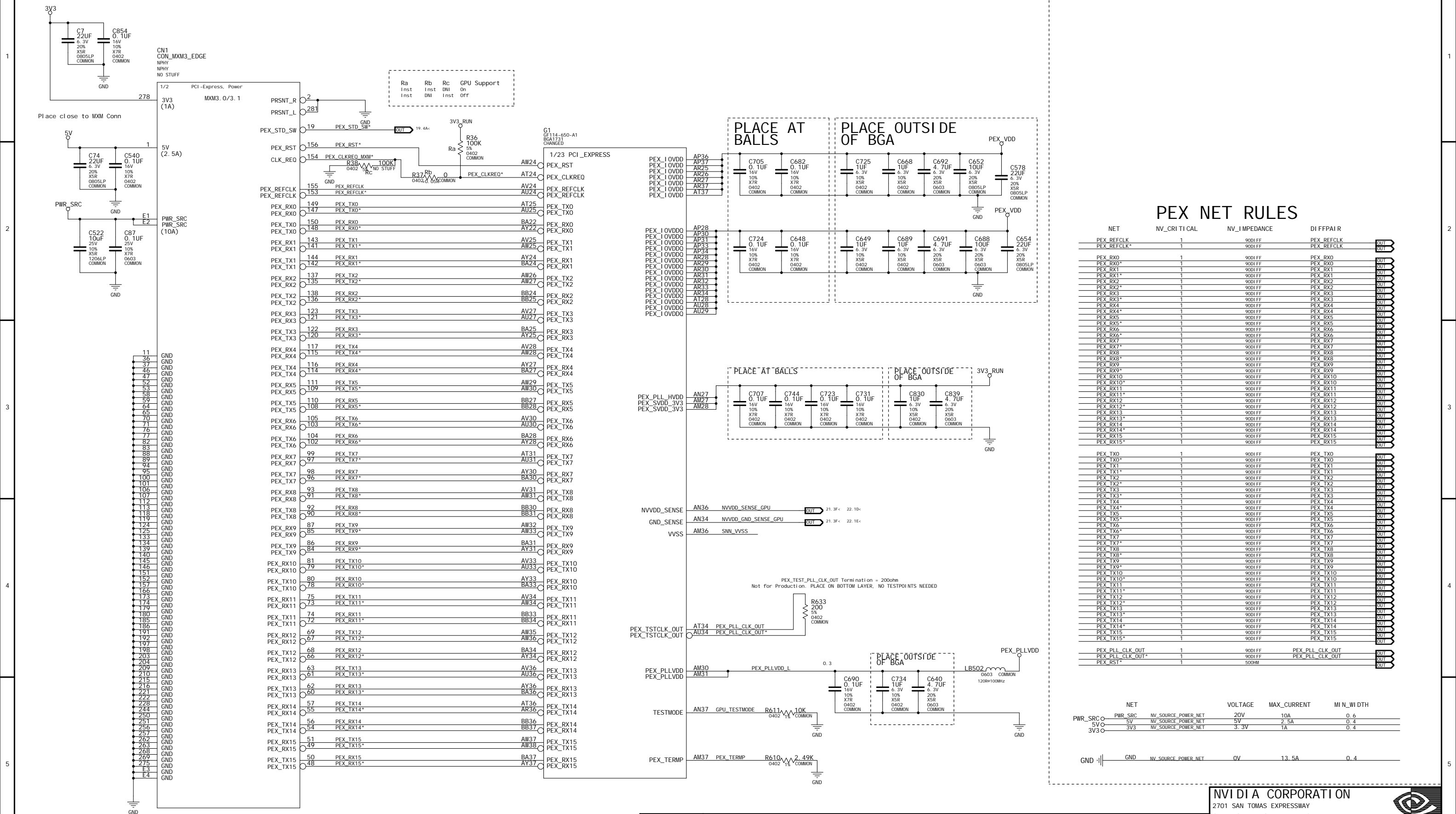
GF114, GDDR5, MXM TYPE B

LVDS/TMDS, DACA, DP\_A, DP\_B, DP\_C, DP\_D

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	PCI Express
3	GPU Frame Buffer Partition A/B
4	Frame Buffer Partition A
5	Frame Buffer Partition B
6	Frame Buffer Partition A/B Decoupling
7	GPU Frame Buffer Partition C/D
8	Frame Buffer Partition C
9	Frame Buffer Partition D
10	Frame Buffer Partition C/D Decoupling
11	Frame Buffer Constraints
12	GPU Decoupling
13	MXM IO and IO/DAC/I2C
14	DACA Interface and Unused DACB
15	IFP A/B Interface
16	IFP C/D and E/F Interfaces
17	Multi-use IO(MIO) Interface
18	Misc-GPIO/I2C/ROM/XTAL
19	Multi-Level Straps
20	GPU NVVDD, FBVDDQ and GND
21	PEX_VDD, IFPAB_IOVDD, 3V3_RUN, MXM SCHM00, and MXM Mounting Holes
22-23	NVVDD and FBVDDQ controller, NVVDD phase 1 and FBVDDQ driver stages

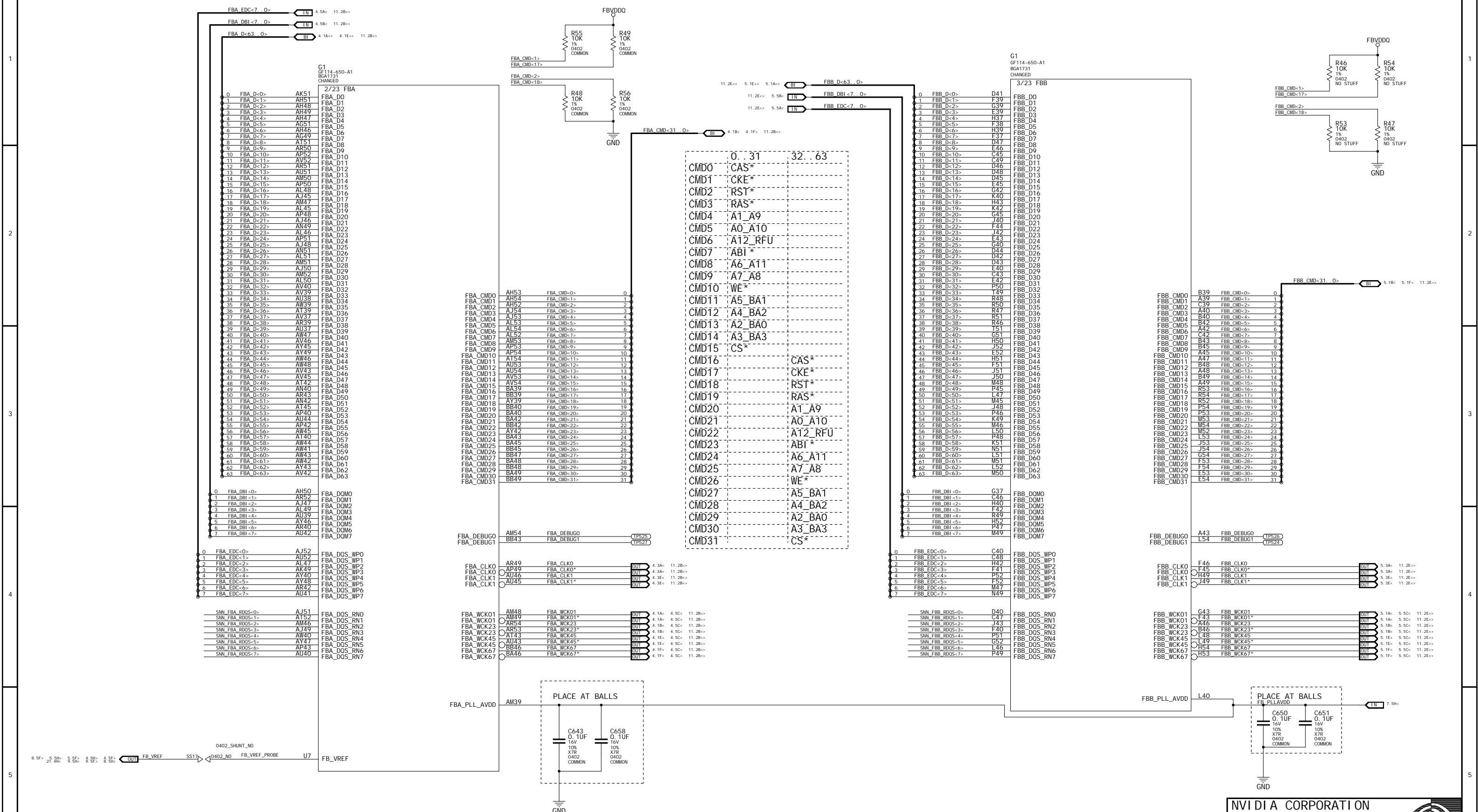
## PAGE2: MXM PCI EXPRESS



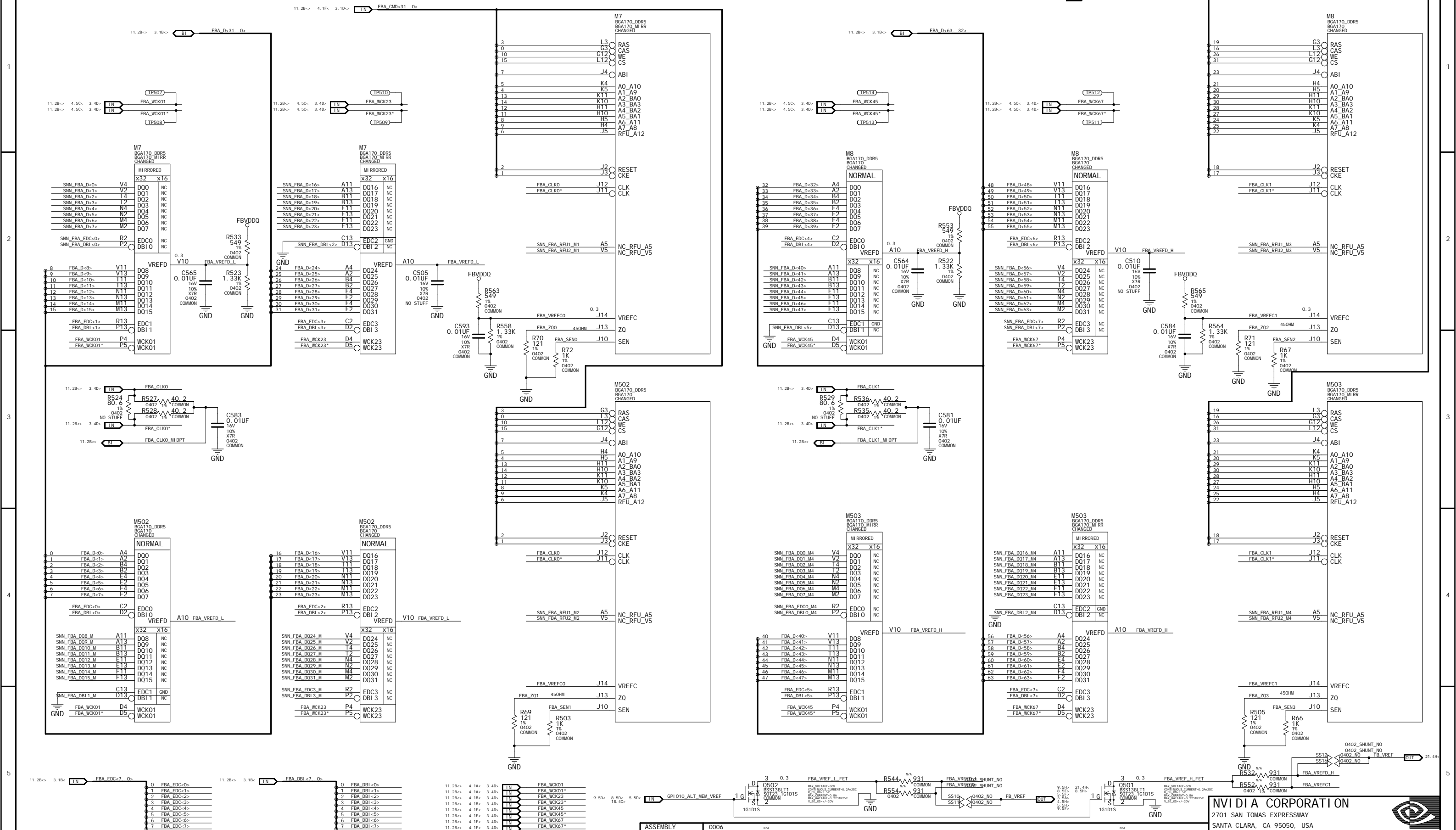
PEX NET RULES				
NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAIR R	
PEX_REFCLK	1	90DI FF	PEX_REFCLK	OUT
PEX_REFCLK*	1	90DI FF	PEX_REFCLK	OUT
PEX_RX0	1	90DI FF	PEX_RX0	OUT
PEX_RX0*	1	90DI FF	PEX_RX0	OUT
PEX_RX1	1	90DI FF	PEX_RX1	OUT
PEX_RX1*	1	90DI FF	PEX_RX1	OUT
PEX_RX2	1	90DI FF	PEX_RX2	OUT
PEX_RX2*	1	90DI FF	PEX_RX2	OUT
PEX_RX3	1	90DI FF	PEX_RX3	OUT
PEX_RX3*	1	90DI FF	PEX_RX3	OUT
PEX_RX4	1	90DI FF	PEX_RX4	OUT
PEX_RX4*	1	90DI FF	PEX_RX4	OUT
PEX_RX5	1	90DI FF	PEX_RX5	OUT
PEX_RX5*	1	90DI FF	PEX_RX5	OUT
PEX_RX6	1	90DI FF	PEX_RX6	OUT
PEX_RX6*	1	90DI FF	PEX_RX6	OUT
PEX_RX7	1	90DI FF	PEX_RX7	OUT
PEX_RX7*	1	90DI FF	PEX_RX7	OUT
PEX_RX8	1	90DI FF	PEX_RX8	OUT
PEX_RX8*	1	90DI FF	PEX_RX8	OUT
PEX_RX9	1	90DI FF	PEX_RX9	OUT
PEX_RX9*	1	90DI FF	PEX_RX9	OUT
PEX_RX10	1	90DI FF	PEX_RX10	OUT
PEX_RX10*	1	90DI FF	PEX_RX10	OUT
PEX_RX11	1	90DI FF	PEX_RX11	OUT
PEX_RX11*	1	90DI FF	PEX_RX11	OUT
PEX_RX12	1	90DI FF	PEX_RX12	OUT
PEX_RX12*	1	90DI FF	PEX_RX12	OUT
PEX_RX13	1	90DI FF	PEX_RX13	OUT
PEX_RX13*	1	90DI FF	PEX_RX13	OUT
PEX_RX14	1	90DI FF	PEX_RX14	OUT
PEX_RX14*	1	90DI FF	PEX_RX14	OUT
PEX_RX15	1	90DI FF	PEX_RX15	OUT
PEX_RX15*	1	90DI FF	PEX_RX15	OUT
PEX_TX0	1	90DI FF	PEX_TX0	OUT
PEX_TX0*	1	90DI FF	PEX_TX0	OUT
PEX_TX1	1	90DI FF	PEX_TX1	OUT
PEX_TX1*	1	90DI FF	PEX_TX1	OUT
PEX_TX2	1	90DI FF	PEX_TX2	OUT
PEX_TX2*	1	90DI FF	PEX_TX2	OUT
PEX_TX3	1	90DI FF	PEX_TX3	OUT
PEX_TX3*	1	90DI FF	PEX_TX3	OUT
PEX_TX4	1	90DI FF	PEX_TX4	OUT
PEX_TX4*	1	90DI FF	PEX_TX4	OUT
PEX_TX5	1	90DI FF	PEX_TX5	OUT
PEX_TX5*	1	90DI FF	PEX_TX5	OUT
PEX_TX6	1	90DI FF	PEX_TX6	OUT
PEX_TX6*	1	90DI FF	PEX_TX6	OUT
PEX_TX7	1	90DI FF	PEX_TX7	OUT
PEX_TX7*	1	90DI FF	PEX_TX7	OUT
PEX_TX8	1	90DI FF	PEX_TX8	OUT
PEX_TX8*	1	90DI FF	PEX_TX8	OUT
PEX_TX9	1	90DI FF	PEX_TX9	OUT
PEX_TX9*	1	90DI FF	PEX_TX9	OUT
PEX_TX10	1	90DI FF	PEX_TX10	OUT
PEX_TX10*	1	90DI FF	PEX_TX10	OUT
PEX_TX11	1	90DI FF	PEX_TX11	OUT
PEX_TX11*	1	90DI FF	PEX_TX11	OUT
PEX_TX12	1	90DI FF	PEX_TX12	OUT
PEX_TX12*	1	90DI FF	PEX_TX12	OUT
PEX_TX13	1	90DI FF	PEX_TX13	OUT
PEX_TX13*	1	90DI FF	PEX_TX13	OUT
PEX_TX14	1	90DI FF	PEX_TX14	OUT
PEX_TX14*	1	90DI FF	PEX_TX14	OUT
PEX_TX15	1	90DI FF	PEX_TX15	OUT
PEX_TX15*	1	90DI FF	PEX_TX15	OUT
PEX_PLL_CLK_OUT	1	90DI FF	PEX_PLL_CLK_OUT	OUT
PEX_PLL_CLK_OUT*	1	90DI FF	PEX_PLL_CLK_OUT	OUT
PEX_RST*	1	50OHM		OUT

NET		VOLTAGE	MAX_CURRENT	MI_N_WI_DTH
PWR_SRC_O	PWR_SRC NV_SOURCE_POWER_NET	20V	10A	0.6
5V_O	5V NV_SOURCE_POWER_NET	5V	2.5A	0.4
3V3_O	3V3 NV_SOURCE_POWER_NET	3.3V	1A	0.4
GND	GND NV_SOURCE_POWER_NET	0V	13.5A	0.4

## PAGE3: GPU FRAME BUFFER PARTITION A/B



## PAGE4: FRAME BUFFER PARTITION A



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

**NVIDIA CORPORATION**  
2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA



NV PN	600-11314-0006-000
-------	--------------------

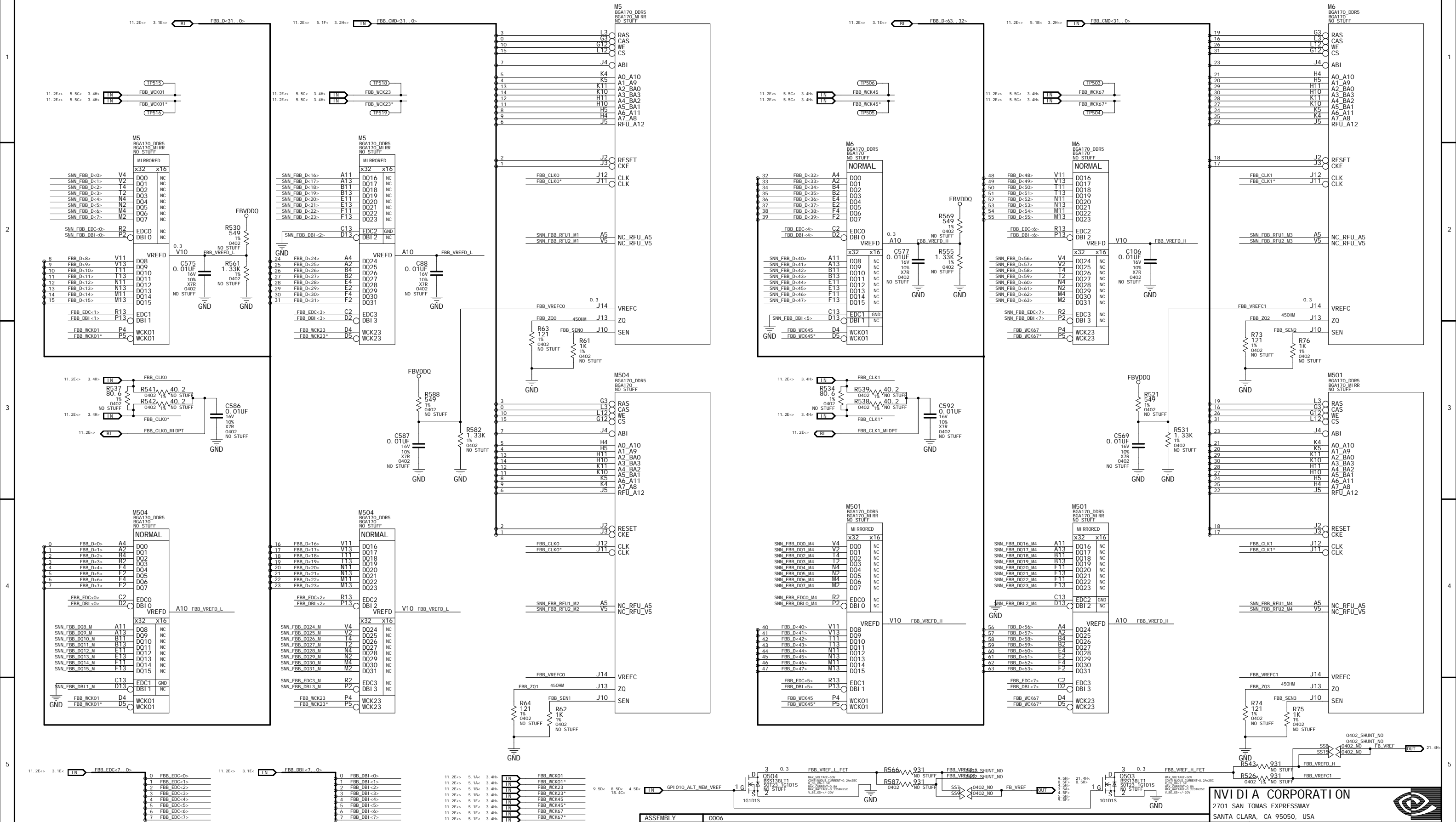
PCB REV	P1314-A00	PAGE	4 OF 23
---------	-----------	------	---------

BOM REV	A	DATE	28-SEP-2011
---------	---	------	-------------

<http://sualaptop365.edu.vn>

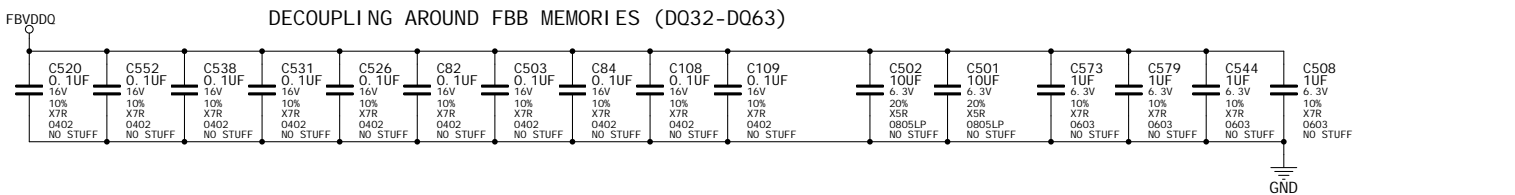
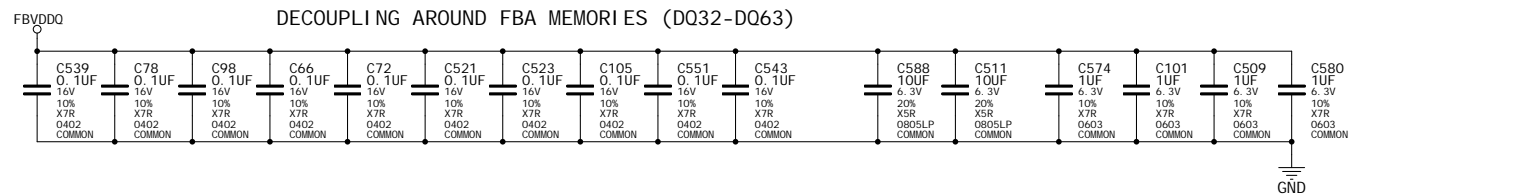
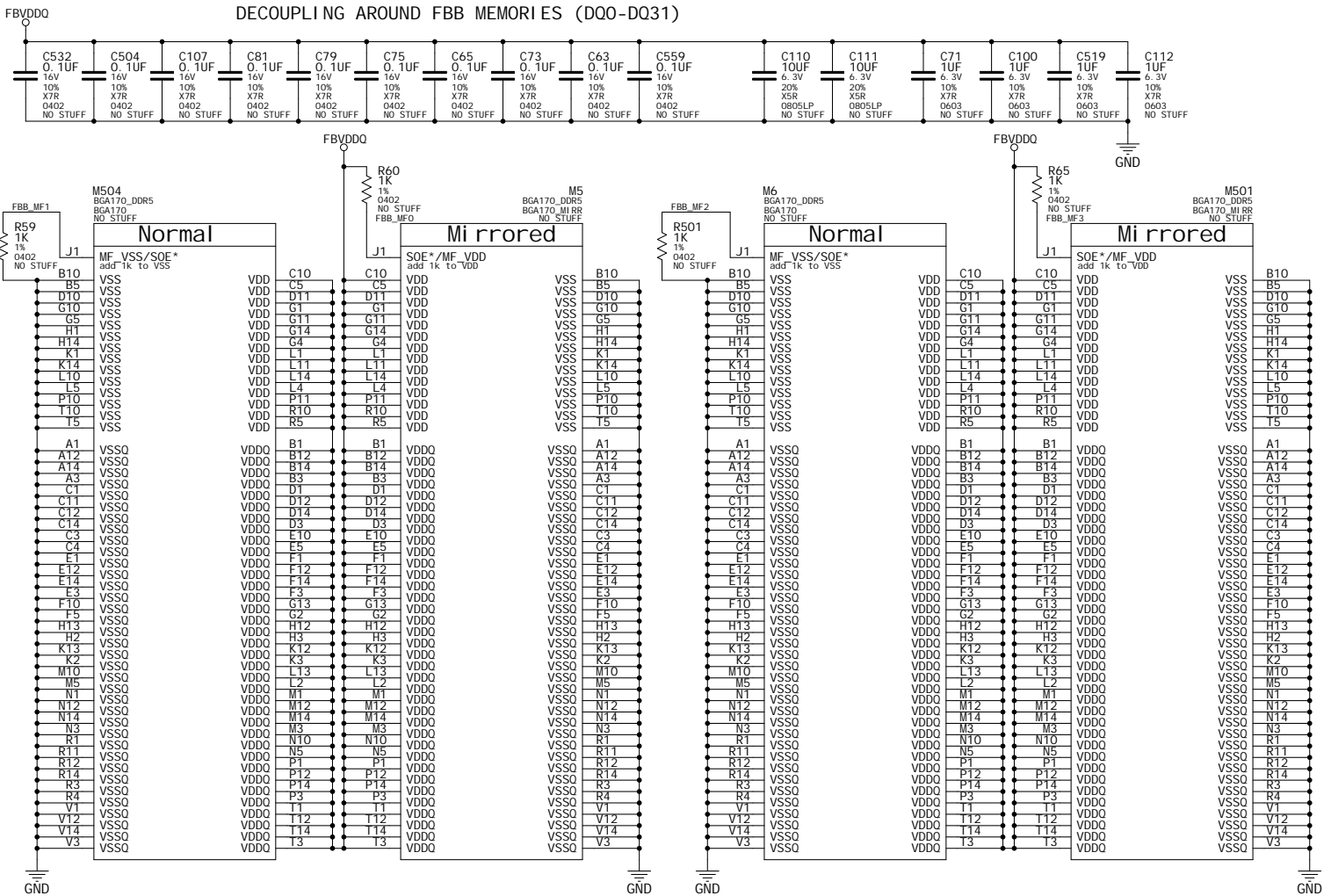
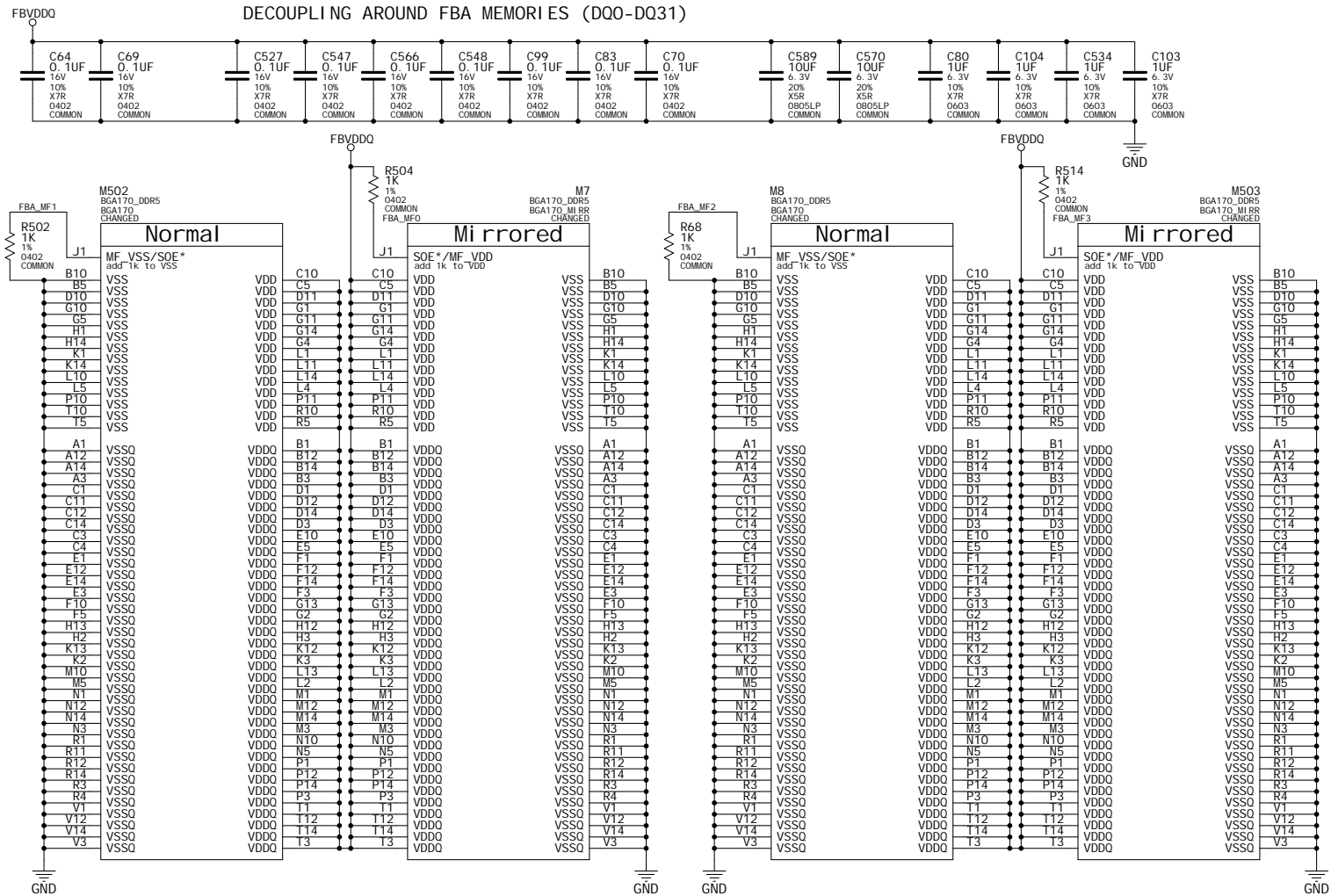


PAGE5: FRAME BUFFER PARTITION B



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

PAGE6: FRAME BUFFER PARTITION A/B DECOUPLING



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA



NV\_PN 600-11314-0006-000

PCB REV P1314-A00

PAGE 6 OF 23

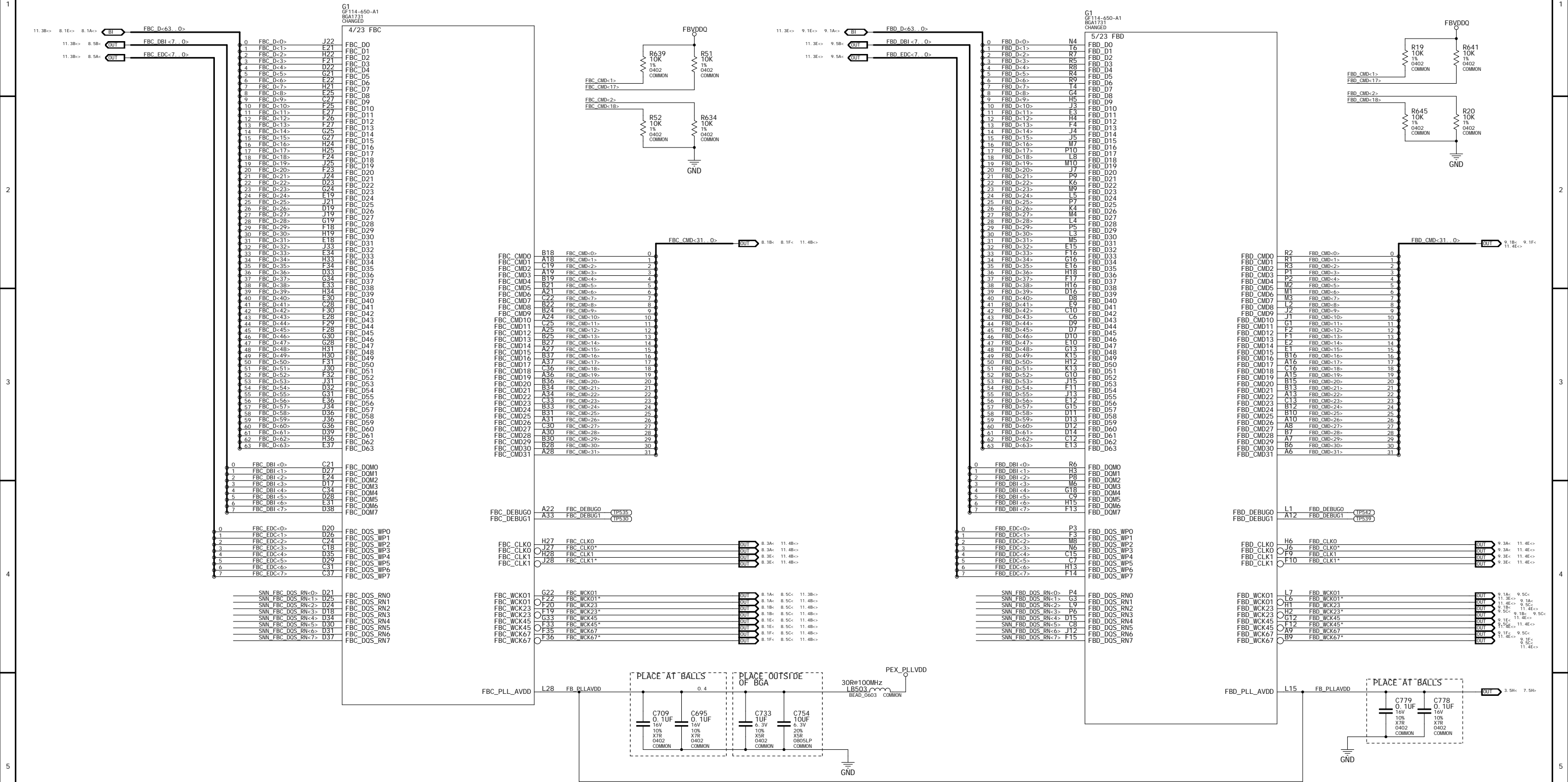
BOM REV A

DATE 28-SEP-2011

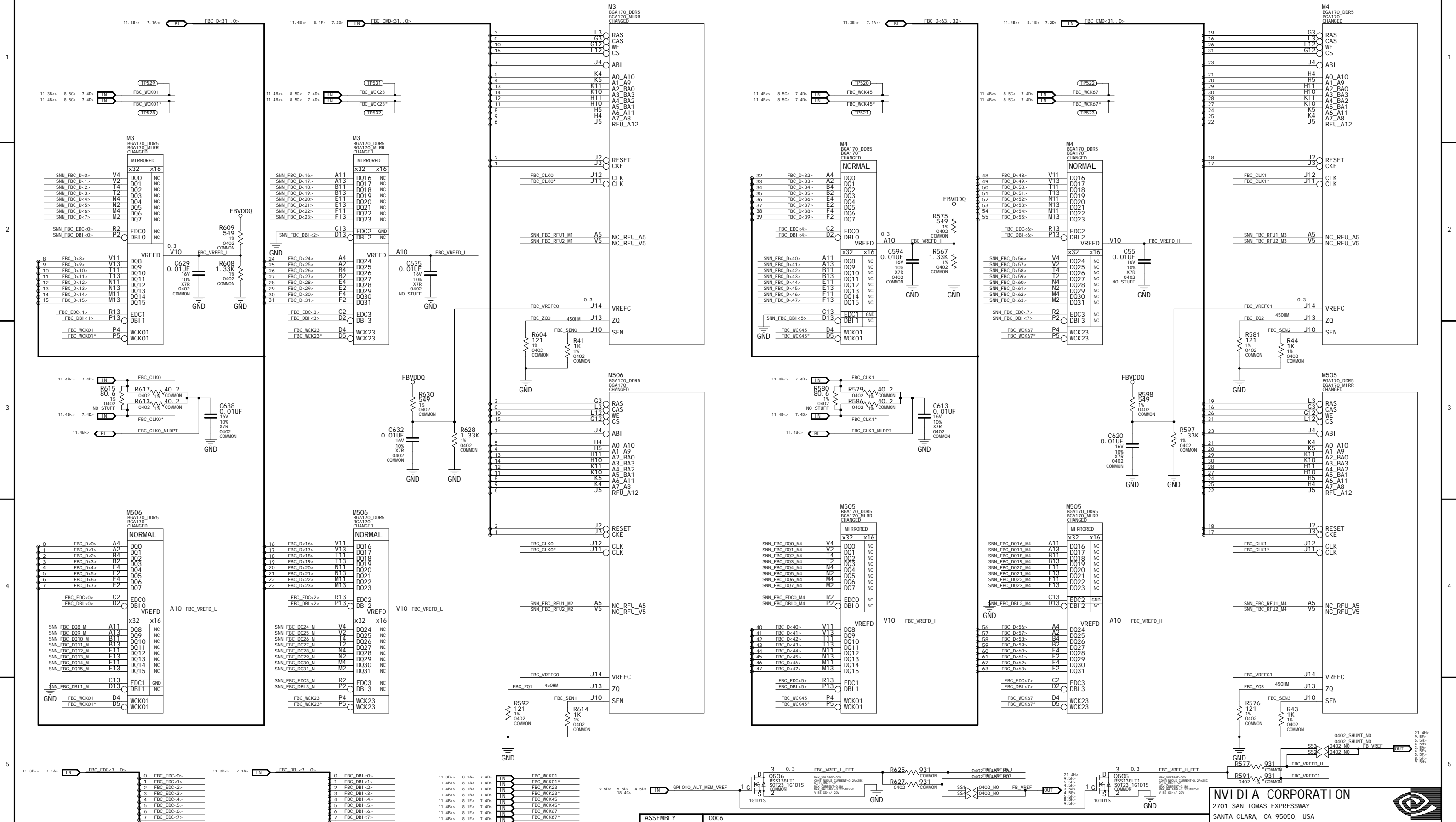
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

<http://sualaptop365.edu.vn>

PAGE7: GPU FRAME BUFFER PARTITION C/D



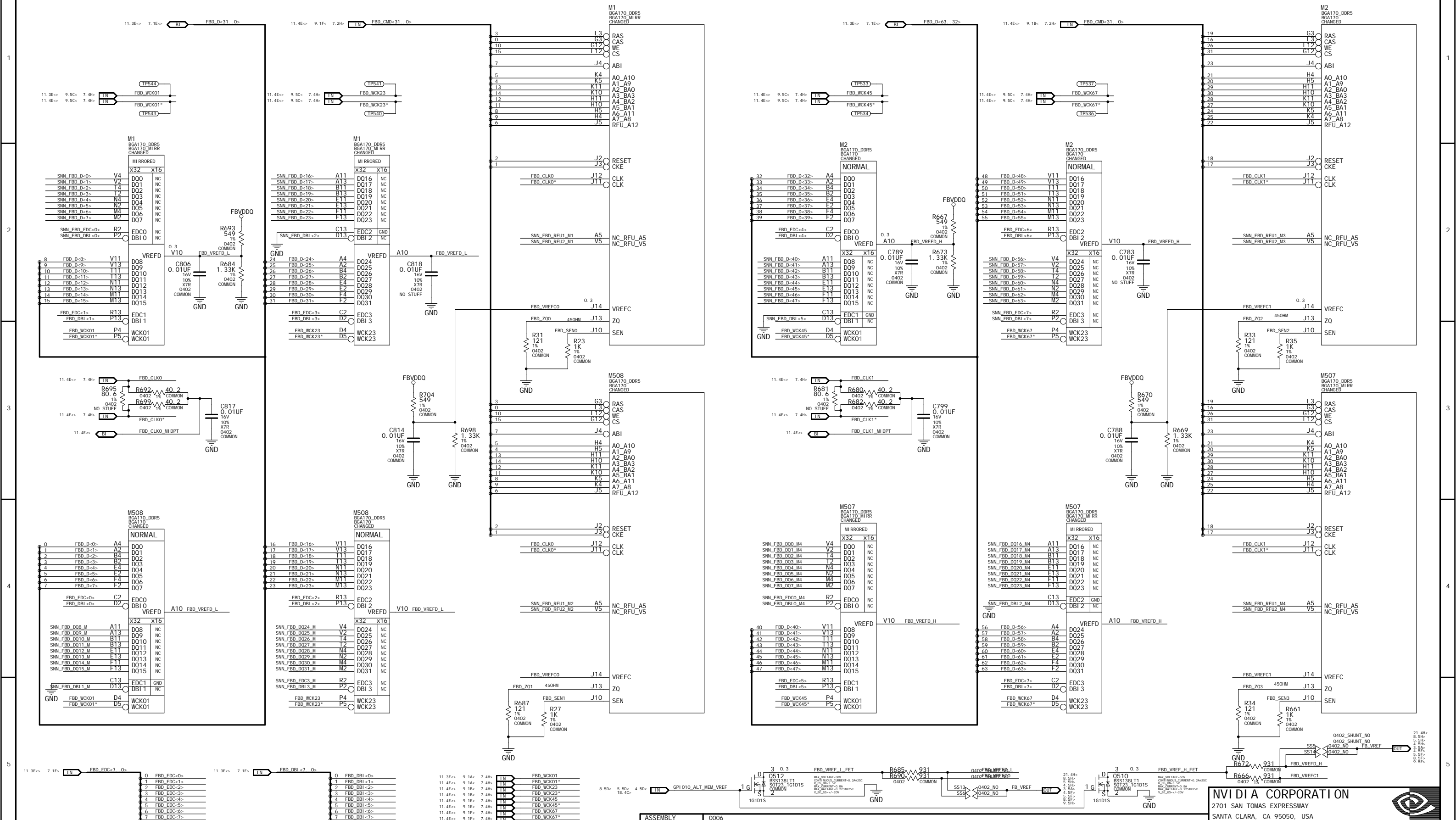
PAGE8: FRAME BUFFER PARTITION C



<http://sualaptop365.edu.vn>

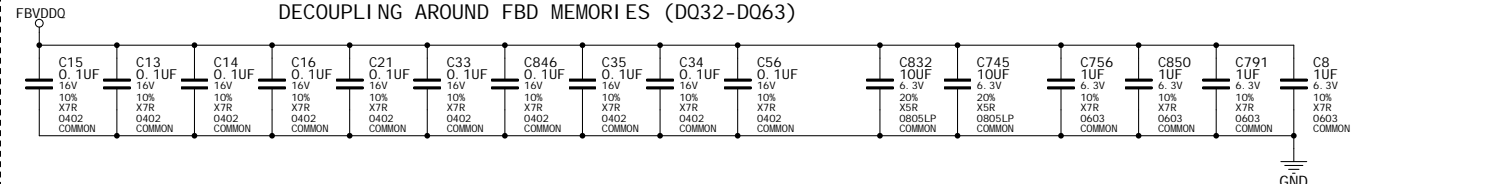
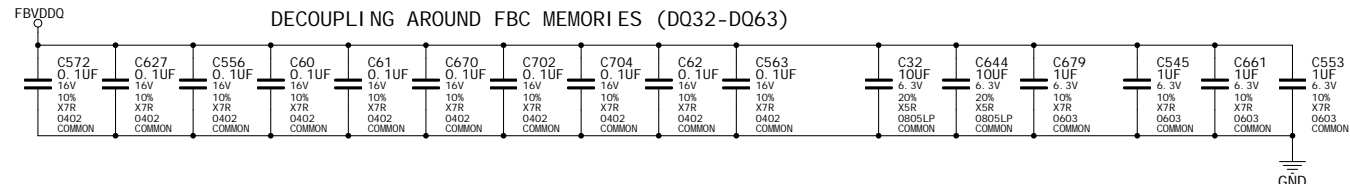
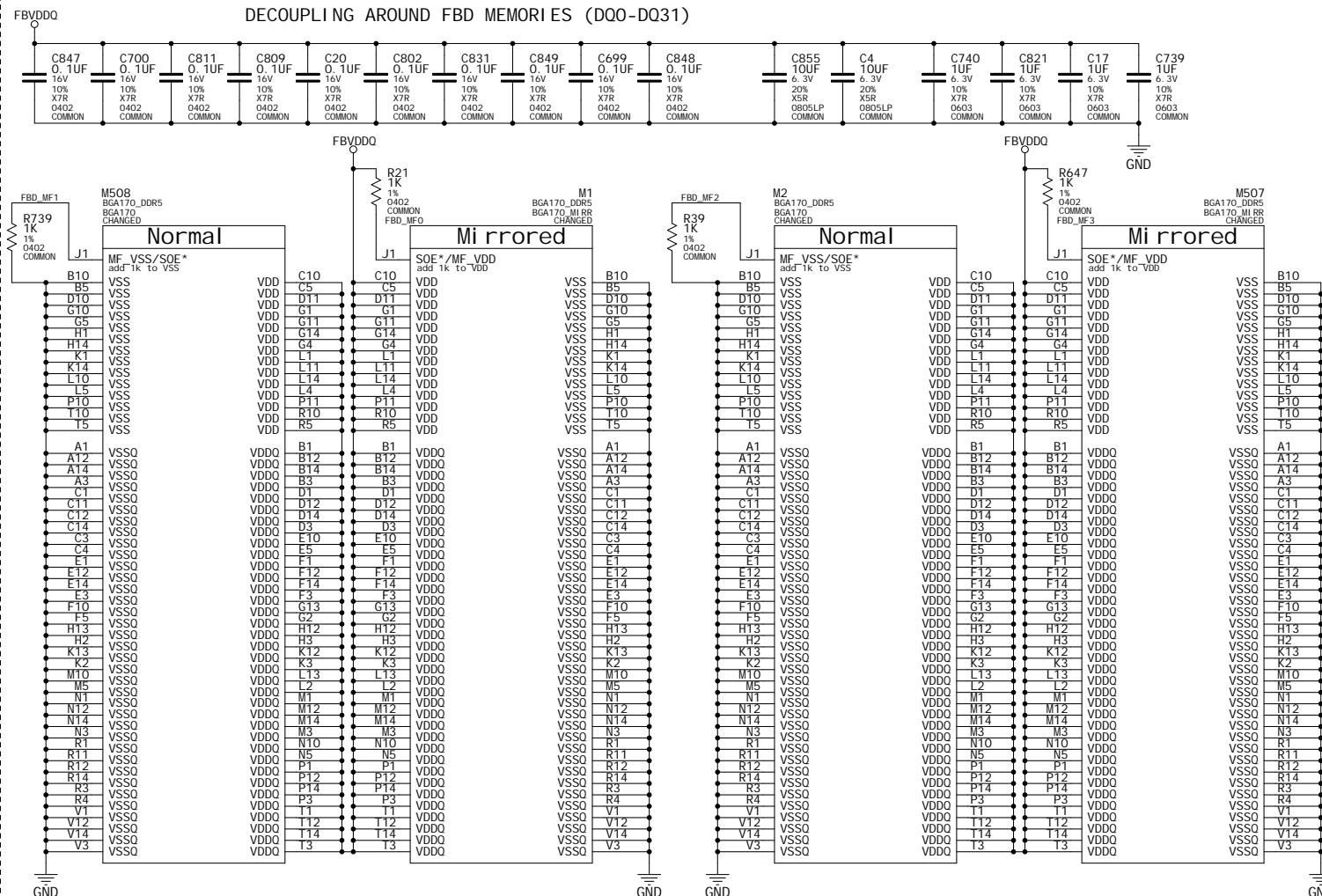
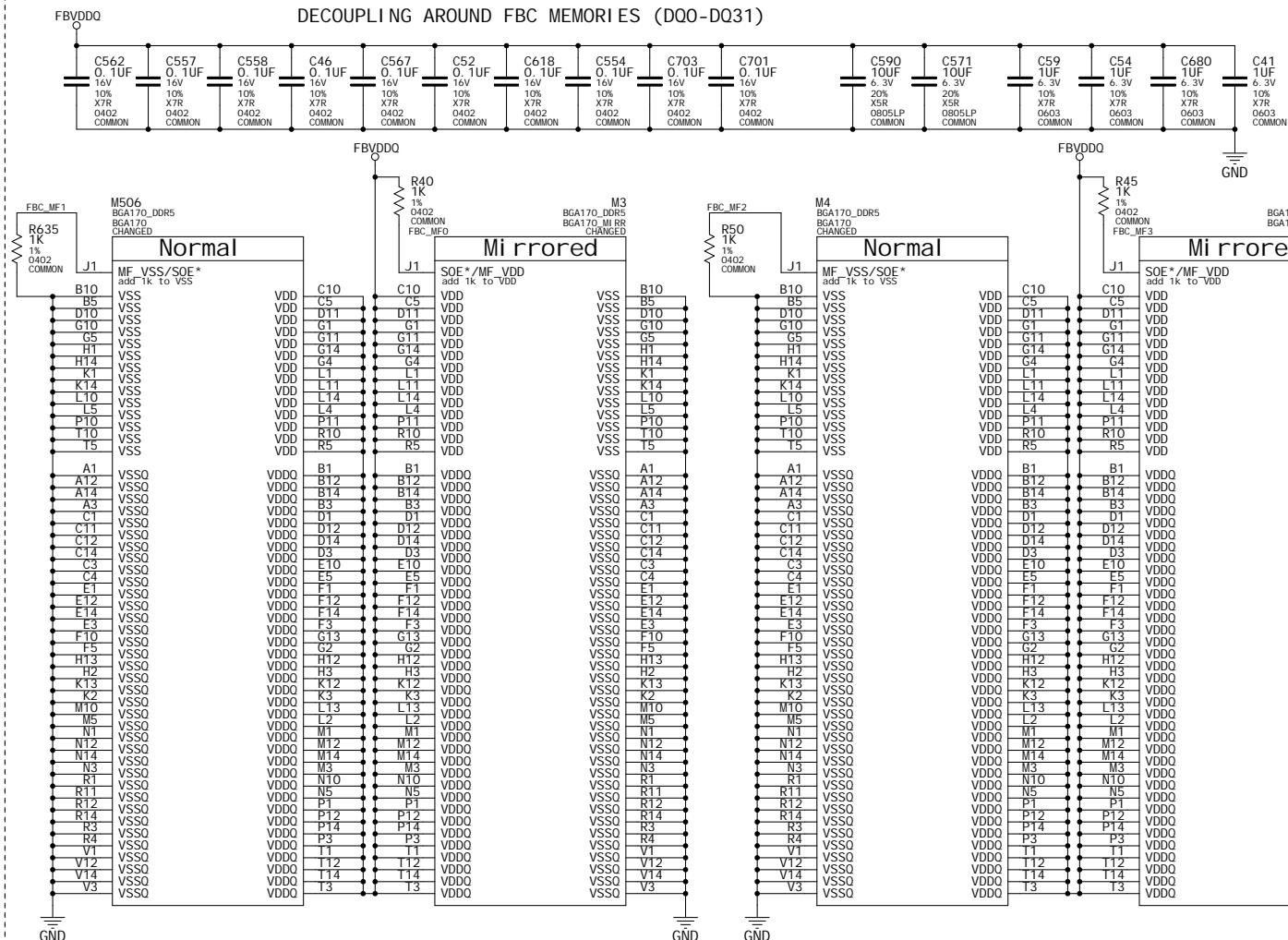


## PAGE9: FRAME BUFFER PARTITION D



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

## PAGE10: FRAME BUFFER PARTITION C/D DECOUPLING



NET RULES FOR PARTITION A  
DATA, DBI , EDC, WCL, CMD/ADDR, CLK

		NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
4. 1A<>	3. 1B<>	[BI] FBA D<63 , O>	1	450HM	
4. 5B<	3. 1B<	[BI] FBA DBI<7 , O>	1	450HM	
	4. 5A<	[BI] FBA EDC<7 , O>	1	450HM	
4. 5C<	4. 1A<	[BI] FBA_WCK01	1	80DI FF	FBA_WCK01
4. 5C<	4. 1A<	[BI] FBA_WCK01*	1	80DI FF	FBA_WCK01
4. 5C<	4. 1B<	[BI] FBA_WCK23	1	80DI FF	FBA_WCK23
4. 5C<	4. 1B<	[BI] FBA_WCK23*	1	80DI FF	FBA_WCK23
4. 5C<	4. 1E<	[BI] FBA_WCK45	1	80DI FF	FBA_WCK45
4. 5C<	4. 1E<	[BI] FBA_WCK45*	1	80DI FF	FBA_WCK45
4. 5C<	4. 1F<	[BI] FBA_WCK67	1	80DI FF	FBA_WCK67
4. 5C<	4. 1F<	[BI] FBA_WCK67*	1	80DI FF	FBA_WCK67
4. 1F<	4. 1B<	[BI] FBA_CMD<31 , O>	2	450HM	
4. 3A<	3. 4D>	[BI] FBA_CLK0	1	80DI FF	FBA_CLK0
4. 3A<	3. 4D>	[BI] FBA_CLK0*	1	80DI FF	FBA_CLK0
4. 3E<	3. 4D>	[BI] FBA_CLK1	1	80DI FF	FBA_CLK1
4. 3E<	3. 4D>	[BI] FBA_CLK1*	1	80DI FF	FBA_CLK1
		NET	VOLTAGE		
4. 3A<>	[BI]	FBA_CLK0_MIDPT	0. 100V		
4. 3E<>	[BI]	FBA_CLK1_MIDPT	0. 100V		

NET RULES FOR PARTITION B  
DATA, DBI , EDC, WCL, CMD/ADDR, CLK

		NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
5. 1A<>	3. 1E<>	[BI] FBB D<63 , O>	1	450HM	
5. 5B<	3. 1E<	[BI] FBB DBI<7 , O>	1	450HM	
	5. 5A<	[BI] FBB EDC<7 , O>	1	450HM	
5. 5C<	5. 1A<	[BI] FBB_WCK01	1	80DI FF	FBB_WCK01
5. 5C<	5. 1A<	[BI] FBB_WCK01*	1	80DI FF	FBB_WCK01
5. 5C<	5. 1B<	[BI] FBB_WCK23	1	80DI FF	FBB_WCK23
5. 5C<	5. 1B<	[BI] FBB_WCK23*	1	80DI FF	FBB_WCK23
5. 5C<	5. 1E<	[BI] FBB_WCK45	1	80DI FF	FBB_WCK45
5. 5C<	5. 1E<	[BI] FBB_WCK45*	1	80DI FF	FBB_WCK45
5. 5C<	5. 1F<	[BI] FBB_WCK67	1	80DI FF	FBB_WCK67
5. 5C<	5. 1F<	[BI] FBB_WCK67*	1	80DI FF	FBB_WCK67
5. 1F<	5. 1B<	[BI] FBB_CMD<31 , O>	2	450HM	
5. 3A<	3. 4B>	[BI] FBB_CLK0	1	80DI FF	FBB_CLK0
5. 3A<	3. 4B>	[BI] FBB_CLK0*	1	80DI FF	FBB_CLK0
5. 3E<	3. 4B>	[BI] FBB_CLK1	1	80DI FF	FBB_CLK1
5. 3E<	3. 4B>	[BI] FBB_CLK1*	1	80DI FF	FBB_CLK1
		NET	VOLTAGE		
5. 3A<>	[BI]	FBB_CLK0_MIDPT	0. 100V		
5. 3E<>	[BI]	FBB_CLK1_MIDPT	0. 100V		

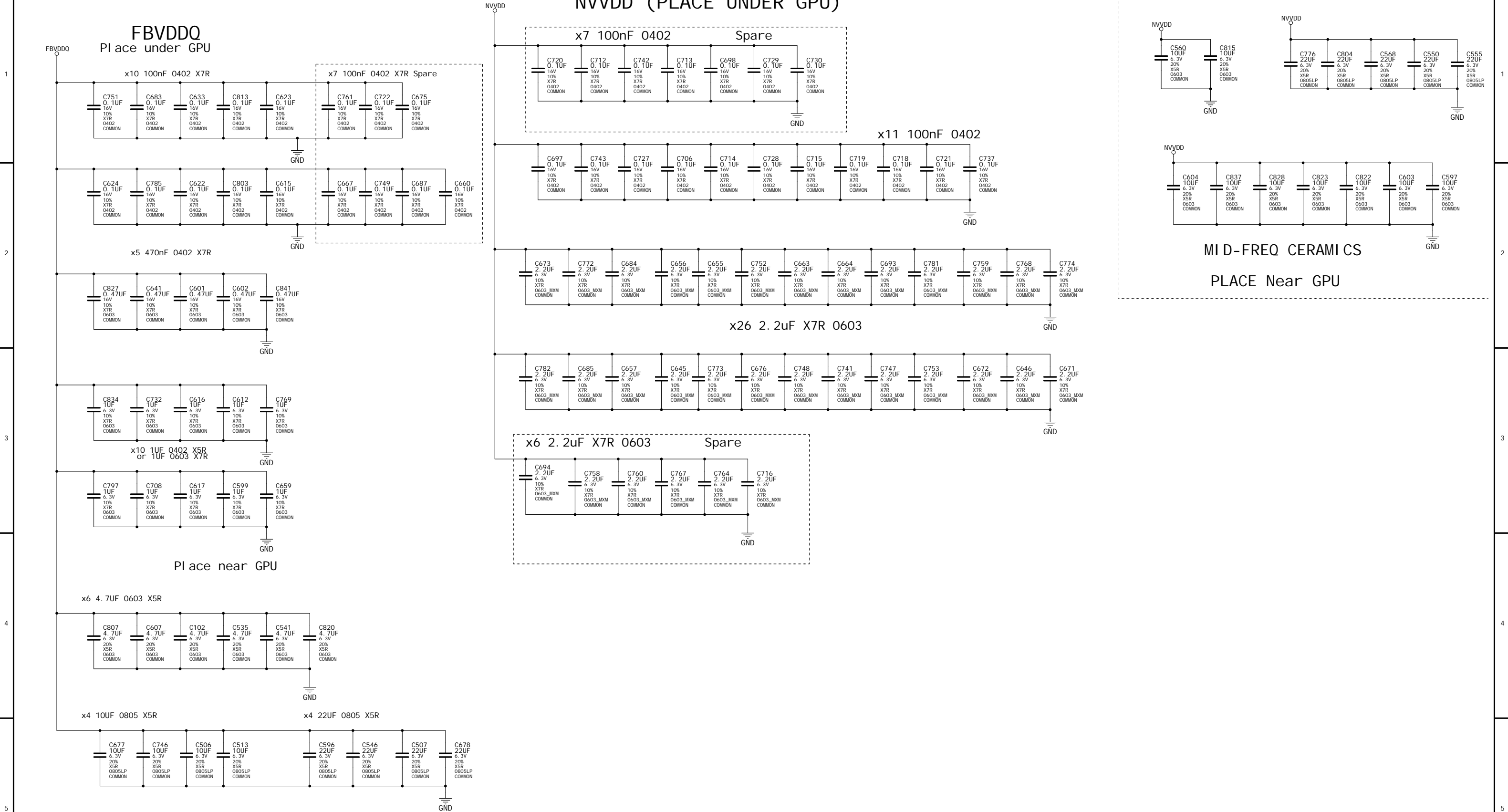
NET RULES FOR PARTITION C  
DATA, DBI , EDC, WCL, CMD/ADDR, CLK

		NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
8. 1A<>	7. 1A<>	[BI] FBC D<63 , O>	1	450HM	
8. 5B<	7. 1A<	[BI] FBC DBI<7 , O>	1	450HM	
	8. 5A<	[BI] FBC EDC<7 , O>	1	450HM	
8. 5C<	8. 1A<	[BI] FBC_WCK01	1	80DI FF	FBC_WCK01
8. 5C<	8. 1A<	[BI] FBC_WCK01*	1	80DI FF	FBC_WCK01
8. 5C<	8. 1B<	[BI] FBC_WCK23	1	80DI FF	FBC_WCK23
8. 5C<	8. 1B<	[BI] FBC_WCK23*	1	80DI FF	FBC_WCK23
8. 5C<	8. 1E<	[BI] FBC_WCK45	1	80DI FF	FBC_WCK45
8. 5C<	8. 1E<	[BI] FBC_WCK45*	1	80DI FF	FBC_WCK45
8. 5C<	8. 1F<	[BI] FBC_WCK67	1	80DI FF	FBC_WCK67
8. 5C<	8. 1F<	[BI] FBC_WCK67*	1	80DI FF	FBC_WCK67
8. 1F<	8. 1B<	[BI] FBC_CMD<31 , O>	2	450HM	
8. 3A<	7. 4D>	[BI] FBC_CLK0	1	80DI FF	FBC_CLK0
8. 3A<	7. 4D>	[BI] FBC_CLK0*	1	80DI FF	FBC_CLK0
8. 3E<	7. 4D>	[BI] FBC_CLK1	1	80DI FF	FBC_CLK1
8. 3E<	7. 4D>	[BI] FBC_CLK1*	1	80DI FF	FBC_CLK1
		NET	VOLTAGE		
8. 3A<>	[BI]	FBC_CLK0_MIDPT	0. 100V		
8. 3E<>	[BI]	FBC_CLK1_MIDPT	0. 100V		

NET RULES FOR PARTITION D  
DATA, DBI , EDC, WCL, CMD/ADDR, CLK

		NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
9. 1A<>	7. 1E<>	[BI] FBD D<63 , O>	1	450HM	
9. 5B<	7. 1E<	[BI] FBD DBI<7 , O>	1	450HM	
	9. 5A<	[BI] FBD EDC<7 , O>	1	450HM	
9. 5C<	9. 1A<	[BI] FBD_WCK01	1	80DI FF	FBD_WCK01
9. 5C<	9. 1A<	[BI] FBD_WCK01*	1	80DI FF	FBD_WCK01
9. 5C<	9. 1B<	[BI] FBD_WCK23	1	80DI FF	FBD_WCK23
9. 5C<	9. 1B<	[BI] FBD_WCK23*	1	80DI FF	FBD_WCK23
9. 5C<	9. 1E<	[BI] FBD_WCK45	1	80DI FF	FBD_WCK45
9. 5C<	9. 1E<	[BI] FBD_WCK45*	1	80DI FF	FBD_WCK45
9. 5C<	9. 1F<	[BI] FBD_WCK67	1	80DI FF	FBD_WCK67
9. 5C<	9. 1F<	[BI] FBD_WCK67*	1	80DI FF	FBD_WCK67
9. 1F<	9. 1B<	[BI] FBD_CMD<31 , O>	2	450HM	
9. 3A<	7. 4B>	[BI] FBD_CLK0	1	80DI FF	FBD_CLK0
9. 3A<	7. 4B>	[BI] FBD_CLK0*	1	80DI FF	FBD_CLK0
9. 3E<	7. 4B>	[BI] FBD_CLK1	1	80DI FF	FBD_CLK1
9. 3E<	7. 4B>	[BI] FBD_CLK1*	1	80DI FF	FBD_CLK1
		NET	VOLTAGE		
9. 3A<>	[BI]	FBD_CLK0_MIDPT	0. 100V		
9. 3E<>	[BI]	FBD_CLK1_MIDPT	0. 100V		

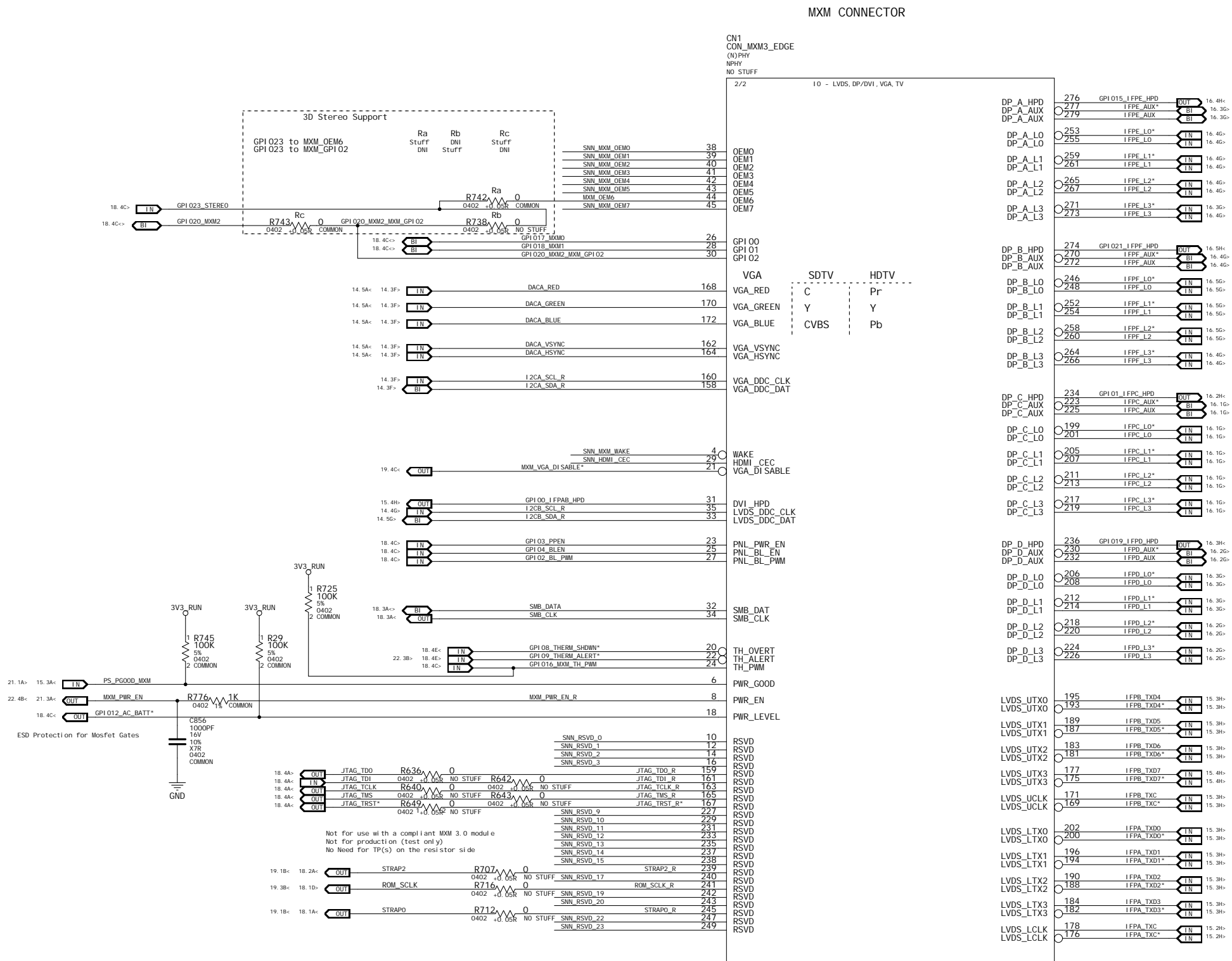
PAGE12: GPU DECOUPLING



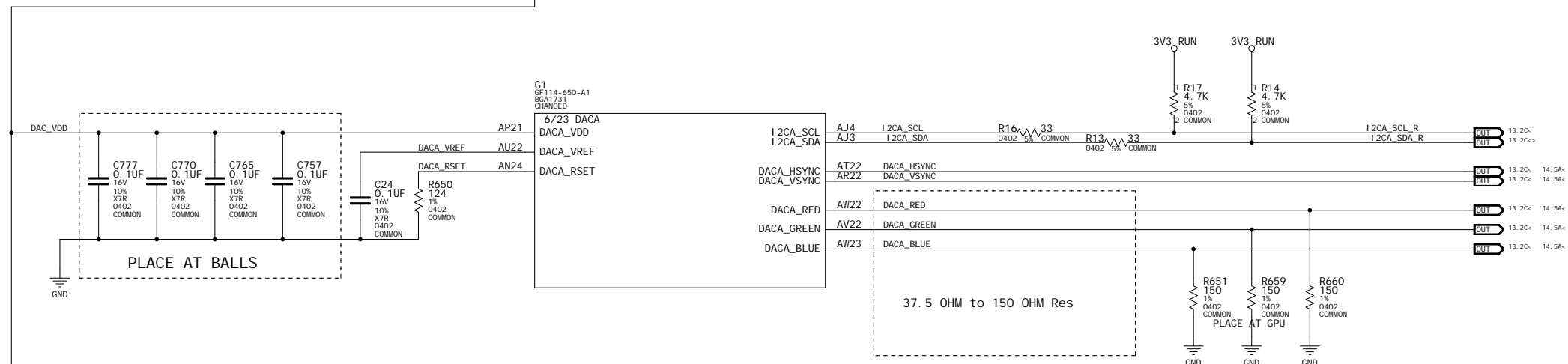
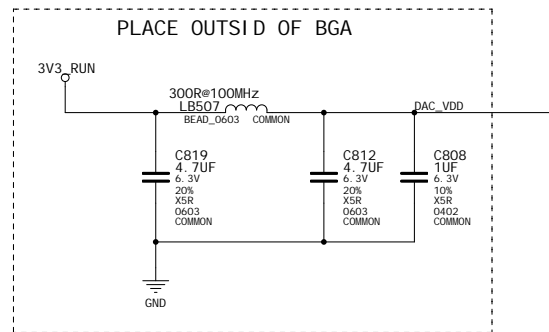
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-11314-0006-000		
PCB REV	P1314-A00	PAGE	12 OF 23
BOM REV	A	DATE	28-SEP-2011






## PAGE14: DACA INTERFACE AND UNUSED DACB

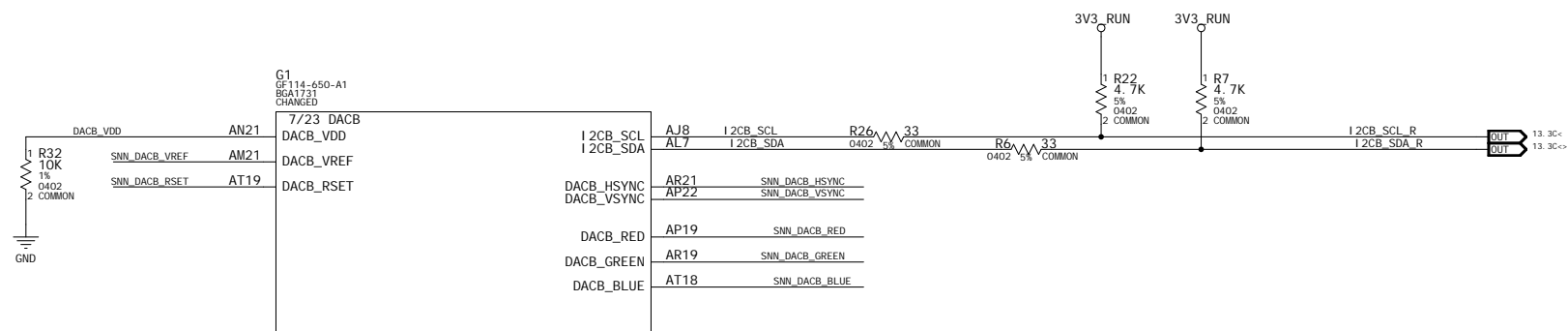


## DACA NET RULES

	NET	NV_CRI TICAL	NV_IMPEDANCE	ECSet
14, 3F, 13, 2C	DACA_RED	1	500HM	DAC_RGB_CSET
14, 3F, 13, 2C	DACA_GREEN	1	500HM	DAC_RGB_CSET
14, 3F, 13, 2C	DACA_BLUE	1	500HM	DAC_RGB_CSET

14, 3F>	13, 2C<		DACA_HSYNC	2	500HM
14, 3F>	13, 2C<		DACA_VSYNC	2	500HM

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DAC_VDD	3.3V	0.25A	0.4



ASSEMBLY	0006
PAGE DETAIL	DACA Interface and Unused DACB

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

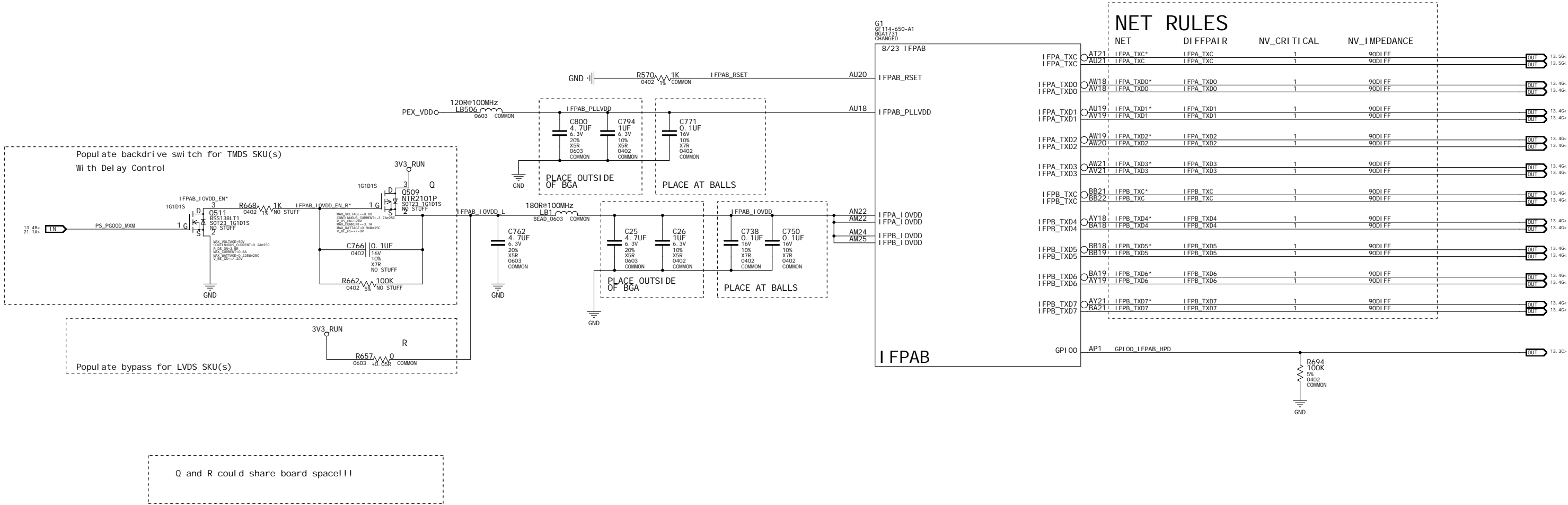
I FPABCD NET RULES

NET	NV_CRITICAL	NV_IMPEDANCE	DIFFPAIR
IFPAB_RSET	1	50OHM	

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IFPAB_I0VDD_L	3.3V	0.40A	0.5
IFPAB_I0VDD	3.3V	0.40A	0.5
IFPAB_PLLVDD	1.05V	0.03A	0.3
IFPAB_I0VDD_R	3.3V	0.15A	0.4

NET RULES

NET	DIFFPAIR	NV_CRITICAL	NV_IMPEDANCE
IFPA_TXC	IFPA_TXC*	1	90DIFF
IFPA_TXD0	IFPA_TXD0*	1	90DIFF
IFPA_TXD1	IFPA_TXD1*	1	90DIFF
IFPA_TXD2	IFPA_TXD2*	1	90DIFF
IFPA_TXD3	IFPA_TXD3*	1	90DIFF
IFPB_TXC	IFPB_TXC*	1	90DIFF
IFPB_TXD4	IFPB_TXD4*	1	90DIFF
IFPB_TXD5	IFPB_TXD5*	1	90DIFF
IFPB_TXD6	IFPB_TXD6*	1	90DIFF
IFPB_TXD7	IFPB_TXD7*	1	90DIFF



Q and R could share board space!!!

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA

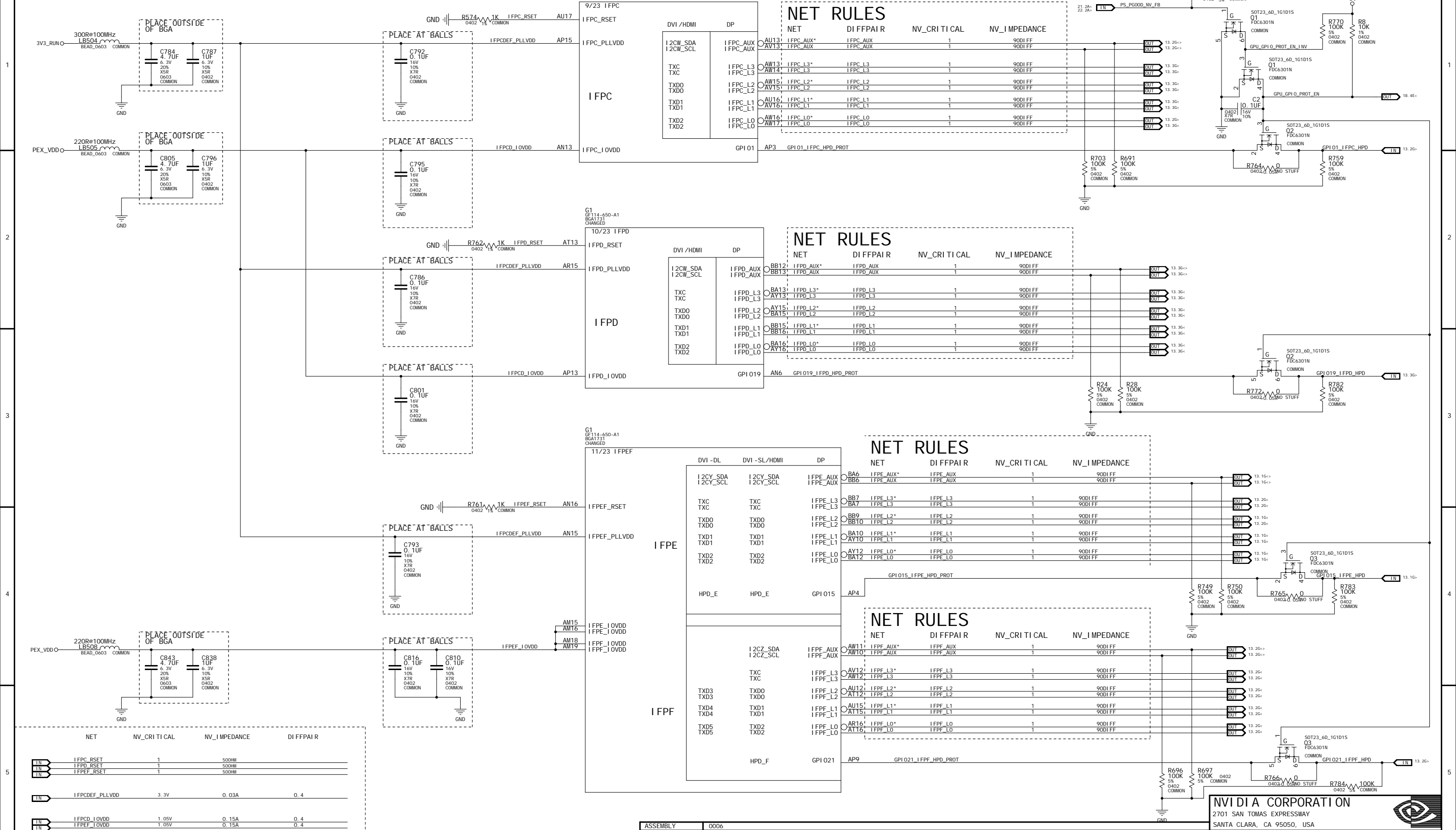


NV\_PN 600-11314-0006-000

PCB REV	P1314-A00	PAGE	15 OF 23
BOM REV	A	DATE	28-SEP-2011

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

PAGE16: I F P C/D AND E/F INTERFACES

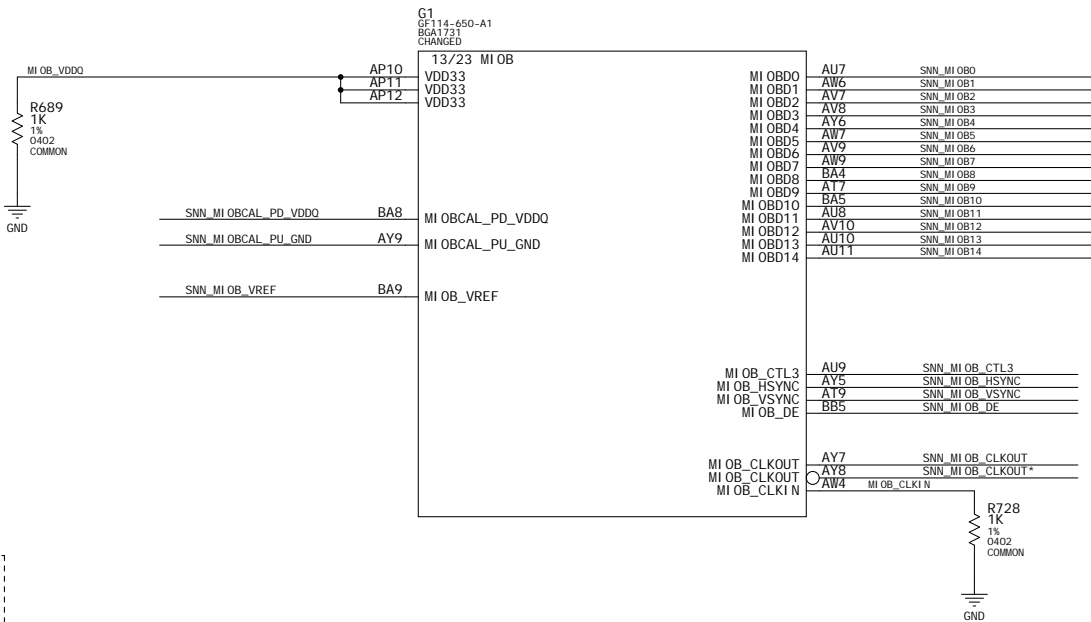
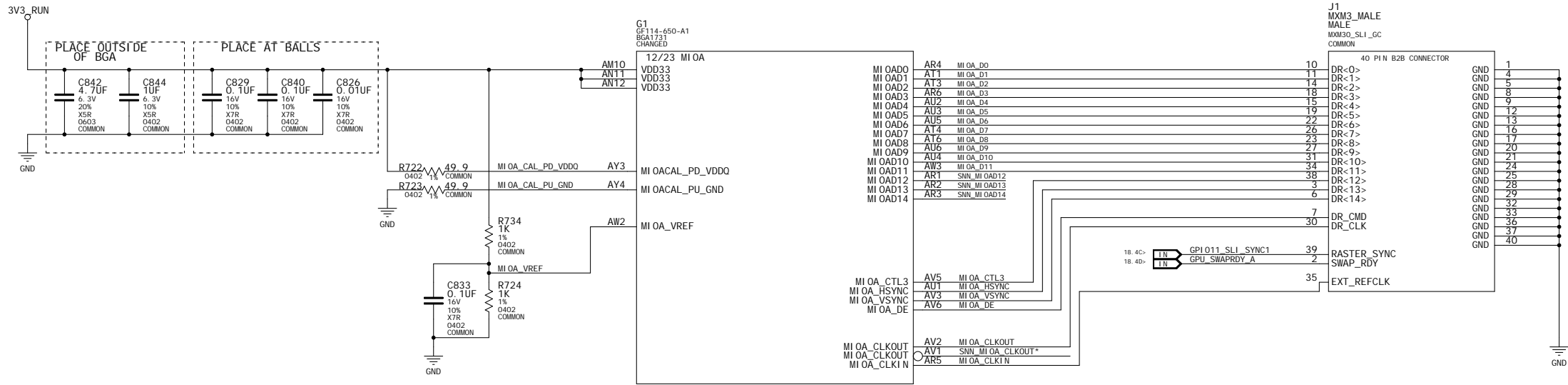


		PAGE DETAIL		IFP C/D and E/F Interfaces	
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, 'MATERIALS') ARE BEING PROVIDED 'AS IS'. THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.					
NV_PN		600-11314-0006-000			
PCB REV		P1314-A00		PAGE	16 OF 23
BOM REV		A		DATE	28-SEP-2011

<http://sualaptop365.edu.vn>







MI O NET RULES

NET	D I F F P A I R		
MI O A_C T L 3	MI O A_S I G N A L S		
MI O A_D_C T L 1_0 >	MI O A_S I G N A L S		
MI O A_H S Y N C	MI O A_S I G N A L S		
MI O A_V S Y N C	MI O A_S I G N A L S		
NET	V O L T A G E	M A X_C U R R E N T	M I N_W I D T H
MI O A_V R E F	1.65V		0.3
MI O A C A L_P D_V D D Q	2.5V		0.3
MI O A C A L_P U_G N D	0.0V		0.3

NV I D I A C O R P O R A T I O N

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA



NV\_P N 600-11314-0006-000

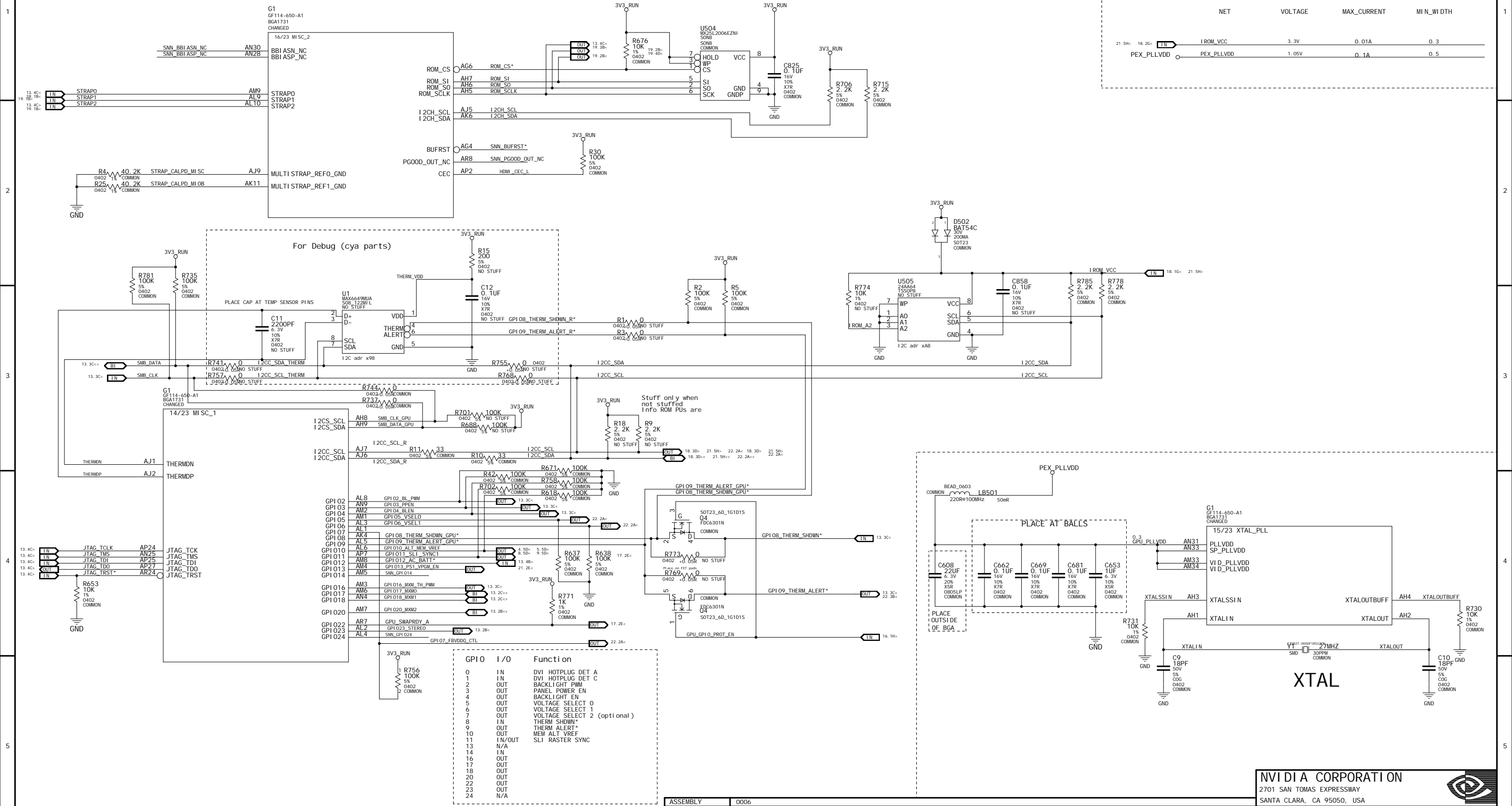
PCB REV P1314-A00 PAGE 17 OF 23

BOM REV A DATE 28-SEP-2011

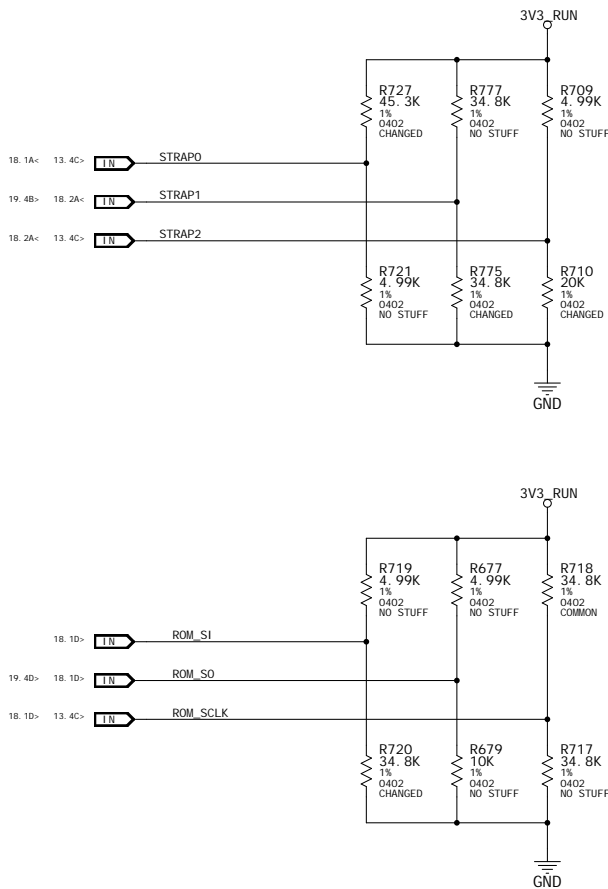
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

MI SC NET RULES

NET	NV_CRI TI CAL	NV_I MPEDANCE	DI FFPAI R
XTALIN XTALOUT	1	50OHM	50OHM
NET	VOLTAGE	MAX_CURRENT	MI N_WI DTH
IROM_VCC	3.3V	0.01A	0.3
PEX_PLLVDD	1.05V	0.1A	0.5



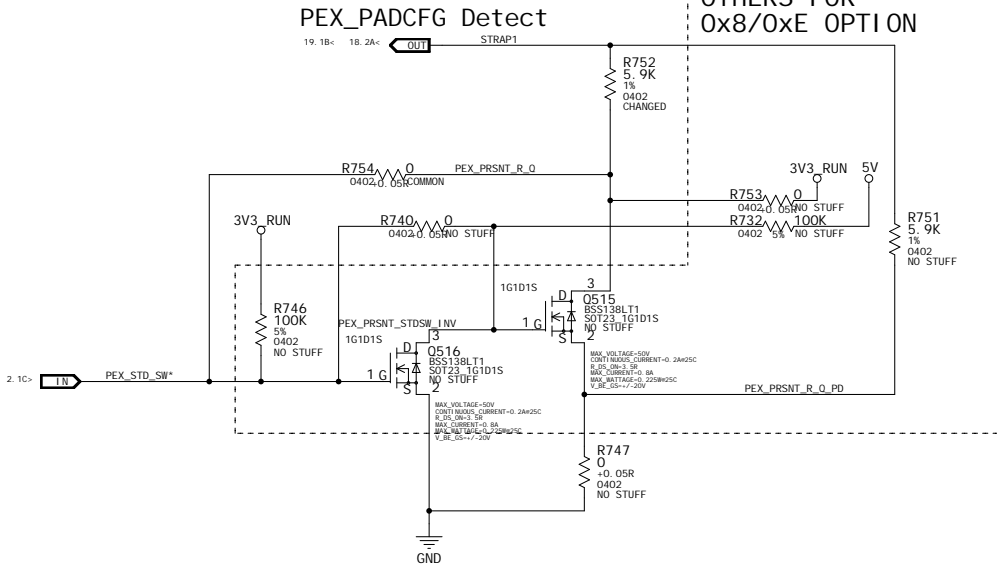
PAGE19: MULTI -LEVEL STRAPS



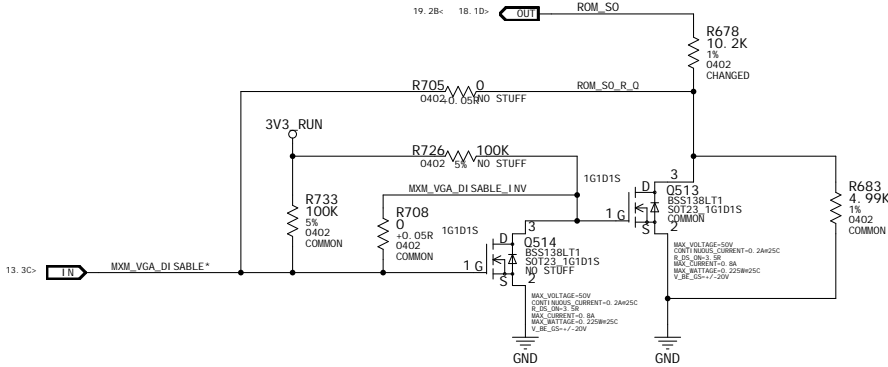
	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111

STRAP0	USER_BIT[3:0]	0xF: EDID used => 45K PU
STRAP1	3GIO_PADCFG_LUT_ADR[3:0]	0x06: GF114 Mobile => 35K PD
STRAP2	PCI_DEVICE[3:0]	0x121x is Set By GPU
	SKU0001	GF114-700-A1:0=> 0x1211 => 0x0001 = 10K PD
	SKU0002	GF114-600-A1:0=> 0x1210 => 0x0000 = 5K PD
	SKU0003	GF114-700-A1:0=> 0x1211 => 0x0001 = 10K PD
	SKU0004	GF114-600-A1:0=> 0x1210 => 0x0000 = 5K PD
VGA_DEVICE	1: VGA_DEVICE	
SMB_ALT_ADDR	0: 0x9E(POR)	0x0001 => 10K PD
FB_O_BAR_SIZE	0: 256MB(POR)	
XCLK_417	0: 277MHz(POR)	
RAM_CFG_0	SKU0001	0110 64Mx16 35K PD Hynix
RAM_CFG_1	SKU0002	0111 64Mx16 45K PD Samsung
RAM_CFG_2	SKU0003	0010 128Mx16 15K PD Hynix
RAM_CFG_3	SKU0004	0011 128Mx16 20K PD Samsung
PEX_PLL_EN_TERM100	0: DISABLED (POR)	
SLOT_CLK_CONFIG	1: GPU and MCH COMMON REFCLK	
SUB_VENDOR	1: BIOS ROM IS PRESENT	
PCI_DEVICE_EXT	1: PCDEVID[4] = 0 for 0x120x DEV IDs = 1 for 0x121x DEV IDs	
	SKU1/2/3/4 = 1110 =35k PU	

STUFF THESE AND STRAP1 PULLUP AS SPEC'D AND NO-STUFF ALL OTHERS FOR 0x8/0xE OPTION



VGA Device Disable



PEX_PRSTN_STDSW*	R_STRAP1	3_GIO_PADCFG_LUT<3..0>
FLOAT	35KPD	0x6 MOBILE_DEFAULT
GND	5kPD (5.9k  35k)	0x0 DESKTOP_DEFAULT
FLOAT	34.8KPU	0xE MOBILE_DEFAULT
GND	5kPU (34.8k  5.9k)	0x8 DESKTOP_DEFAULT

VGA_DISABLE*	R_ROM_SO	MODE
FLOAT	10k	0x1 VGA Device, STD SMBUS_ADDR
GND	15k (5K+10K)	0x2 3D Device, ALT SMBUS_ADDR
GND	5k (10K  10K)	0x0 3D Device

NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA



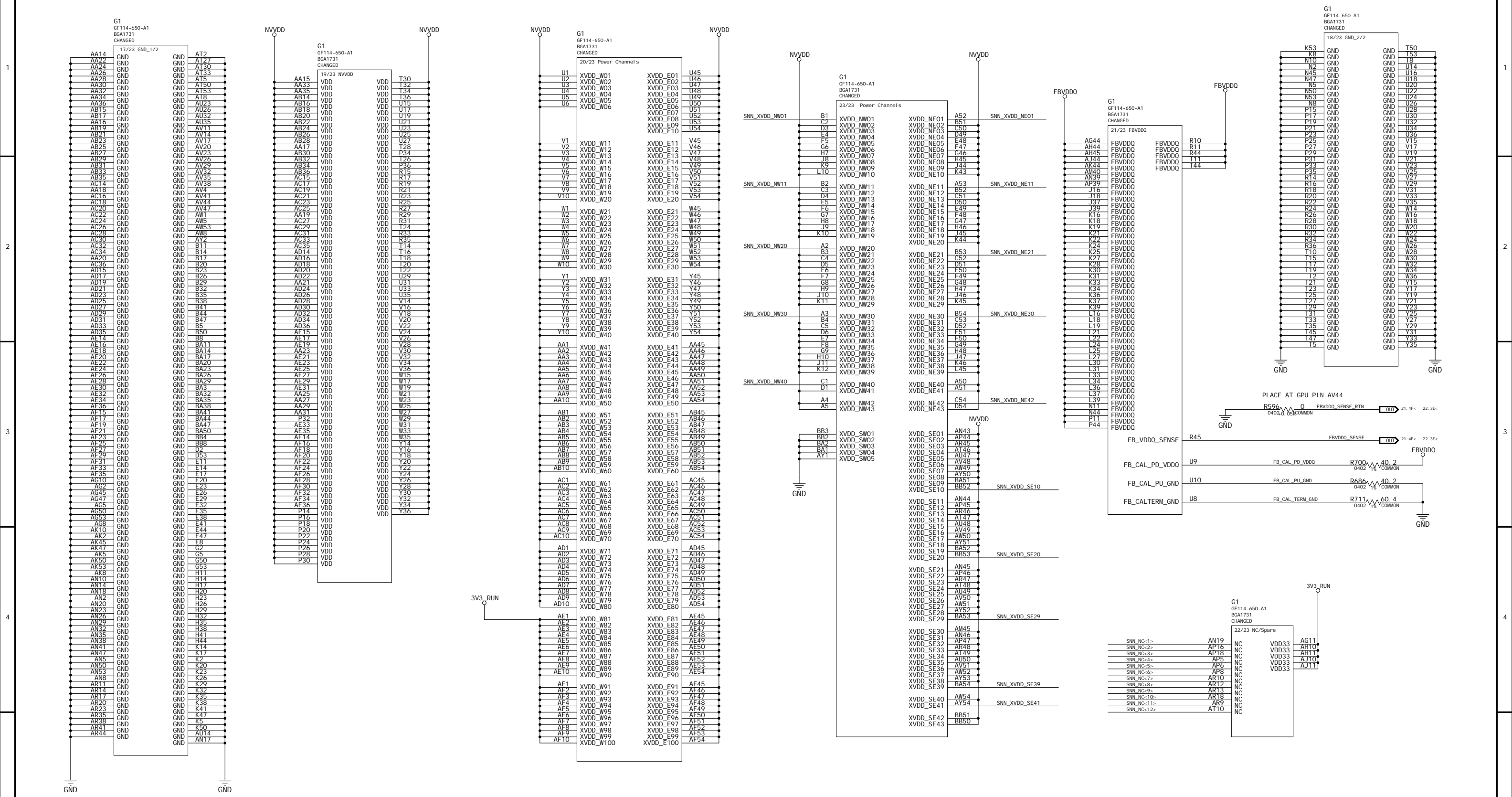
NV\_PN 600-11314-0006-000

PCB REV	P1314-A00	PAGE	19 OF 23
BOM REV	A	DATE	28-SEP-2011

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

<http://sualaptop365.edu.vn>

PAGE20: GPU NVVDD, FBVDDQ, AND GND



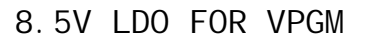
<http://sualaptop365.edu.vn>



PAGE21: PEX\_VDD, IFPAB\_I0VDD, 3V3\_RUN, MXM SCMOO, AND MXM MOUNTING HOLES



2. 6Amps @ 1.1V



THIS WILL WORK FOR PWR\_SRC GREATER THAN 10V.  
IN CIRCUIT PROGRAMMING IS NOT SUPPORTED  
FOR PWR\_SRC IN THE RANGE OF 7V TO 10V

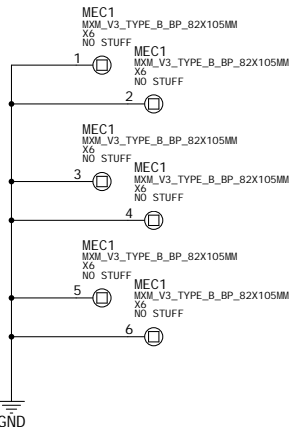
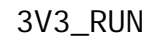
THIS MAY NOT BE STUFFED IN PRODUCTION  
THE CHIL CONTROLLER COULD BE REPLACED BY A  
PRE-PROGRAMMED PART



1.05V @ 100mA

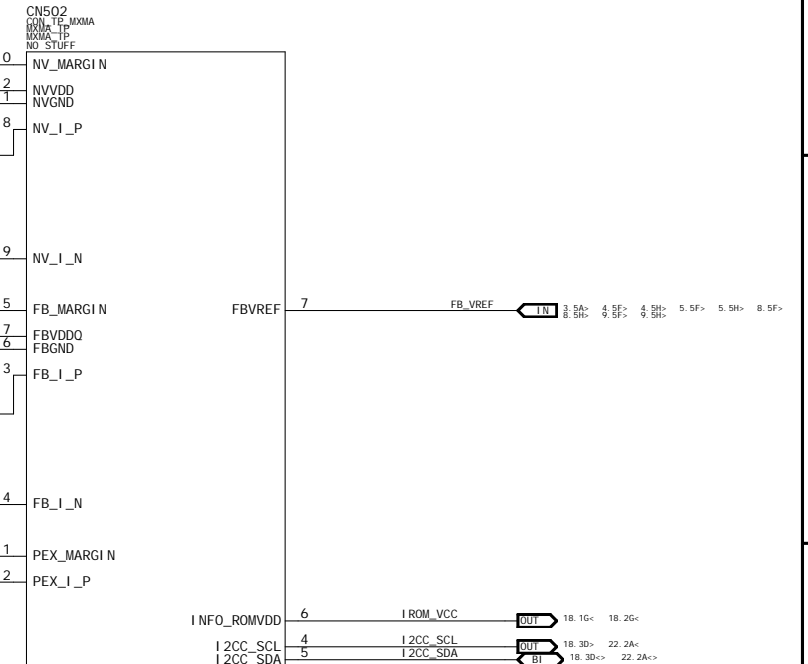
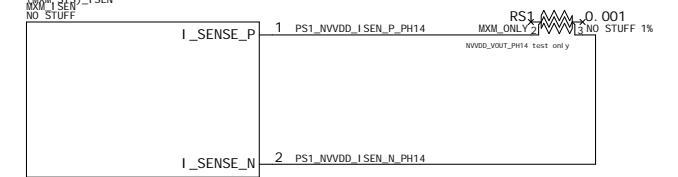
$$V_{out} = V_{ref} * (1 + R_t/R_b)$$

$$1.052V = 0.8V * (1 + 1.69K/5.36K)$$



ASSEMBLY	0006
PAGE DETAIL	PEX_VDD, IFPAB_IOVDD, 3V3_RUN, MXM SCHMOO, and MXM Mounting Holes

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



NVIDIA CORPORATION

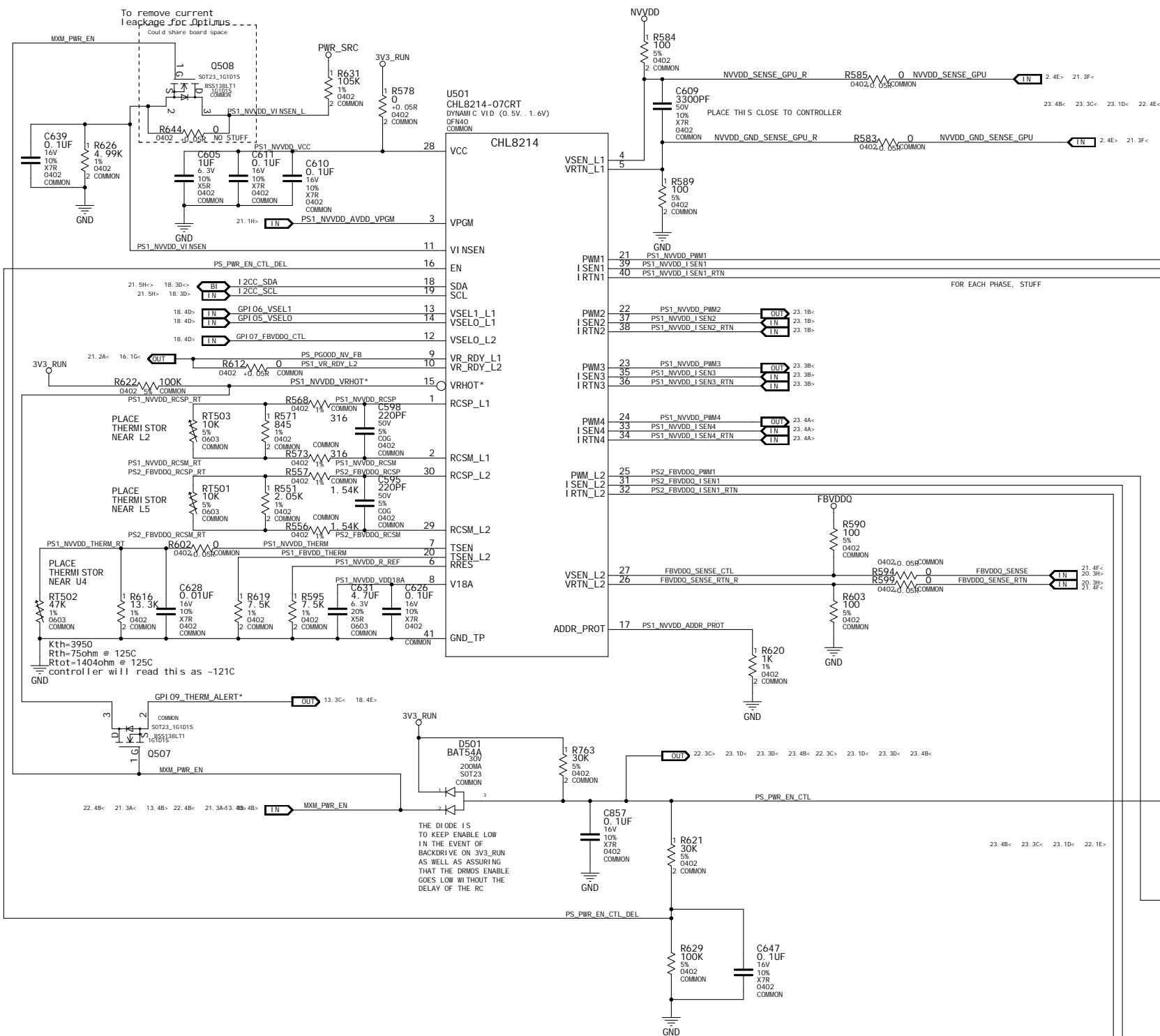
2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN	600-11314-0006-000
-------	--------------------

PCB REV	P1314-A00	PAGE	21 OF 23
BOM REV	A	DATE	28-SEP-2011

## PAGE22: NVVDD AND FBVDDQ CONTROLLER, NVVDD PHASE 1 AND FBVDDQ DRIVER STAGES



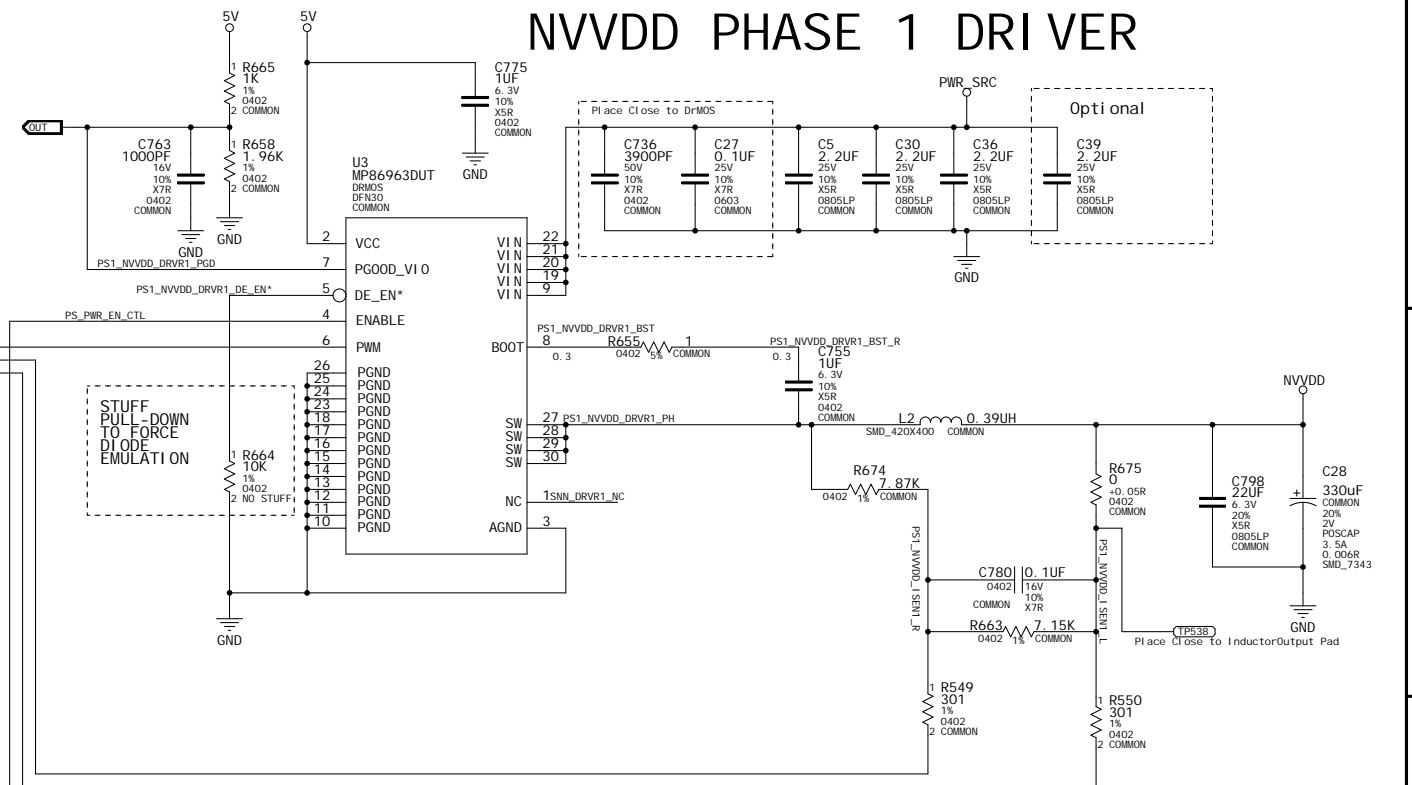
NET	VOLTAGE	CURRENT	LINE_WIDTH
PS2_FBVDD0_DVRV1_Ph	0.9V	20A	0.3
PS1_NVVDD_DVRV1_PH	0.9V	20A	0.3
NVDD	0.9V	100A	0.4
FBVDD	1.5V	20A	0.4
PS1_NVVDD_VCC	3.3V	0.1A	0.3
PS1_NVVDD_VD018A			0.3

RoFDES_#	1.8 mOhm LL	1 mOhm LL	0.3 mOhm LL
R639, R640	1.13K		
R655	1.21K		
C706	100pF		
R670, R678, R517, R554, R511, R547, R708, R719	301 Ohm		
R677, R523, R561, R720	3.74K		

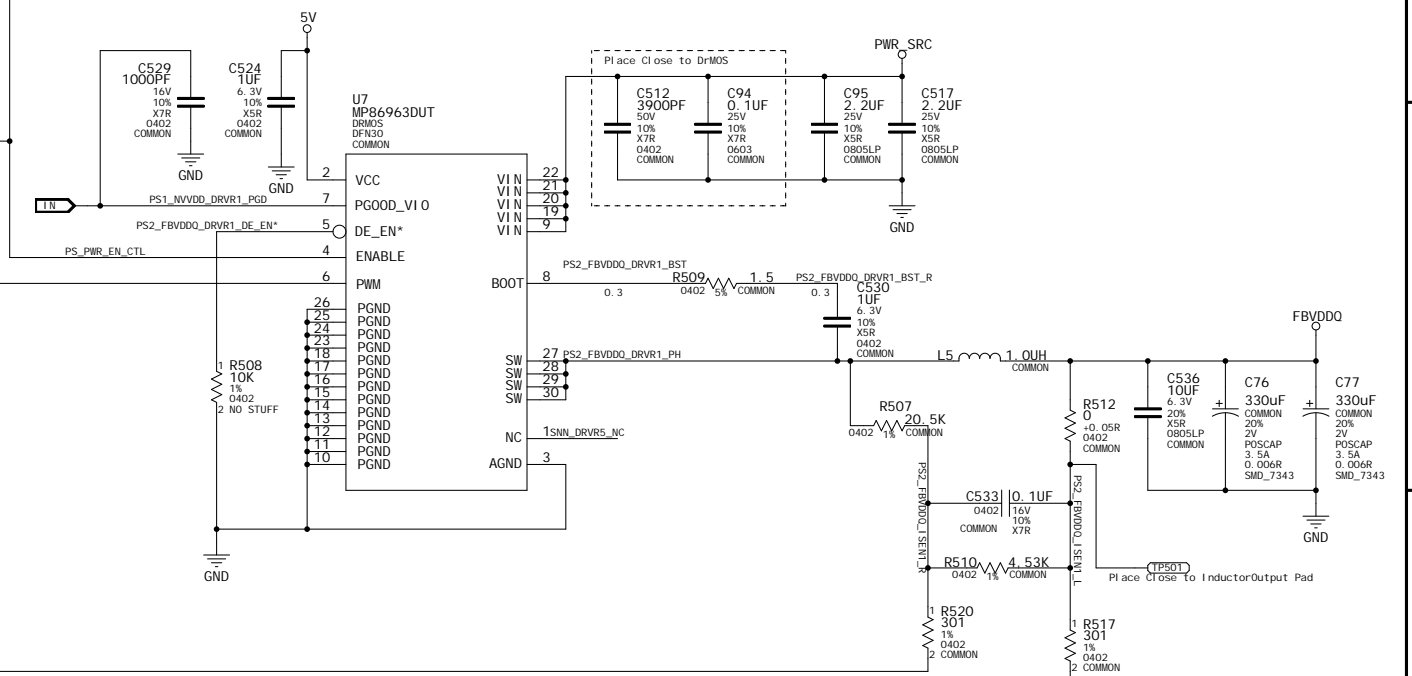
ASSEMBLY	0006
PAGE DETAIL	NVDD and FBVDDQ controller, NVDD phase 1 and FBVDDQ driver stages

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS, AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

# NVVDD PHASE 1 DRIVER



## FBVDDQ DRIVER



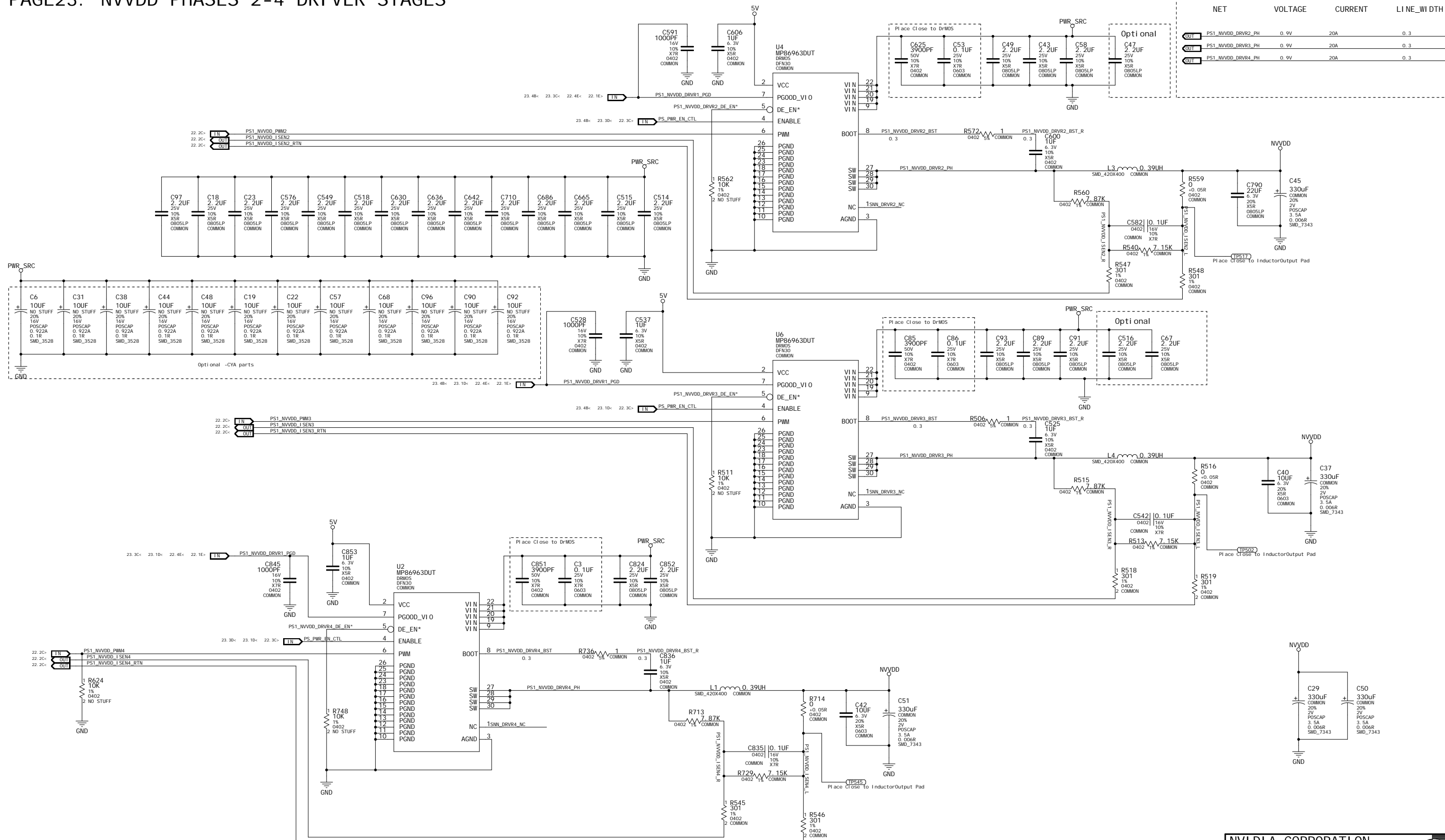
NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY  
SANTA CLARA, CA 95050, USA

NV_PN	600-11314-0006-000
-------	--------------------

PCB REV	P1314-A00	PAGE	22 OF 23
BOM REV	A	DATE	28-SEP-2011

PAGE23: NVVDD PHASES 2-4 DRIVER STAGES



NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA

NV_PN	600-11314-0006-000
-------	--------------------

PCB REV	P1314-A00	PAGE	23 OF 23
---------	-----------	------	----------

P&ID REV	110114 ASS	PAGE	28 OF 28
BOM REV	A	DATE	28-SEP-201

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

<http://sualaptop365.edu.vn>