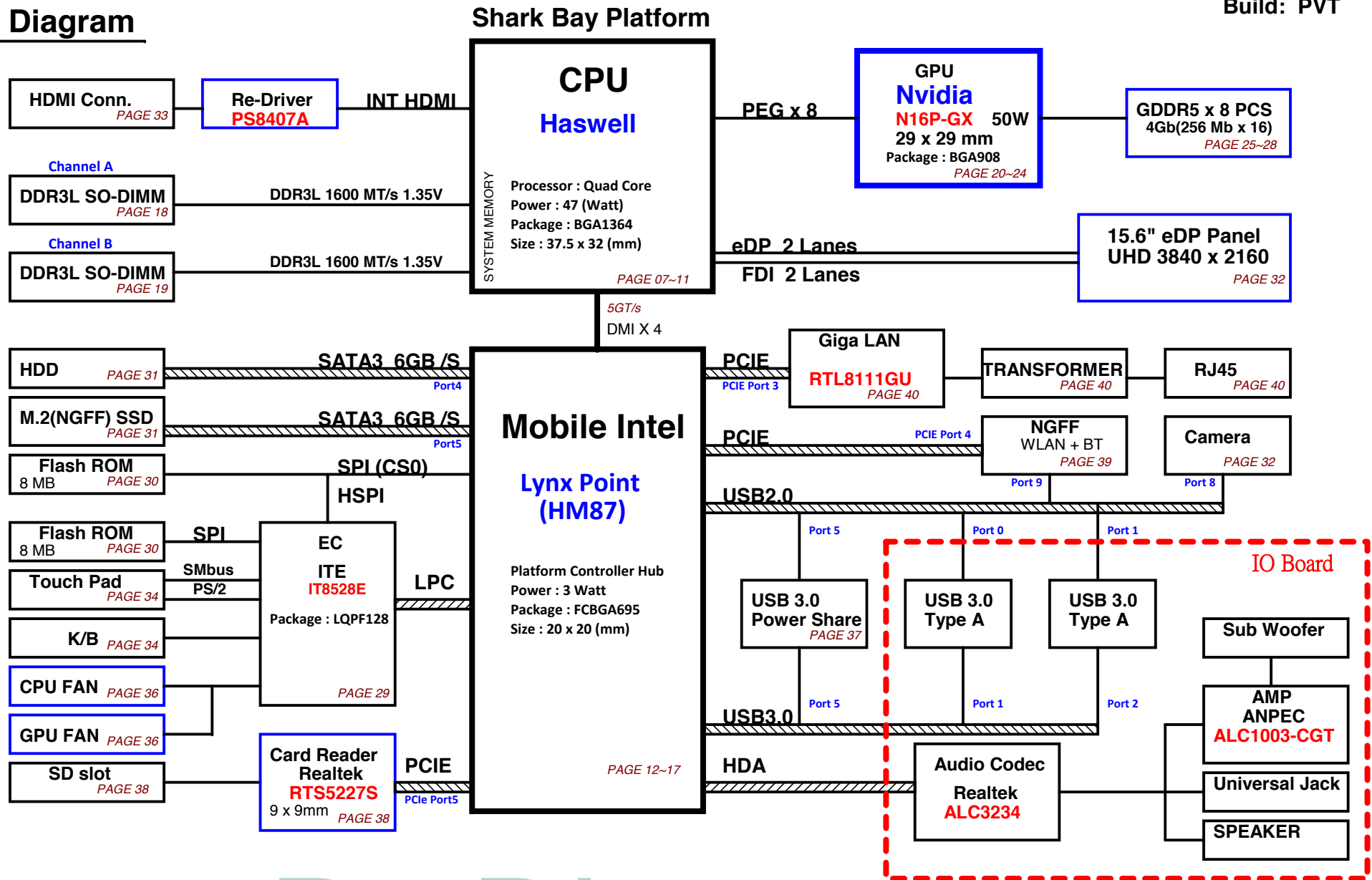
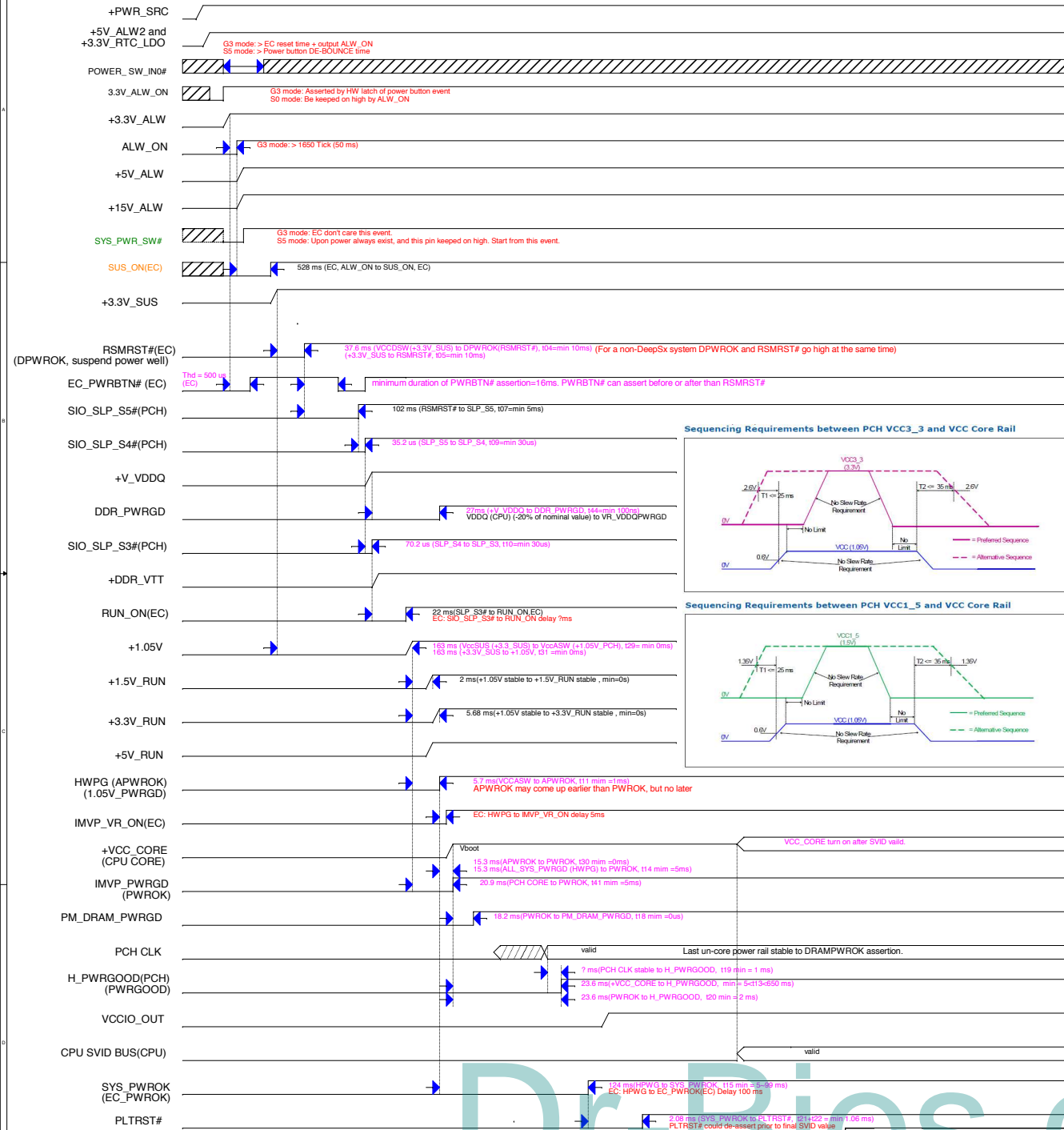
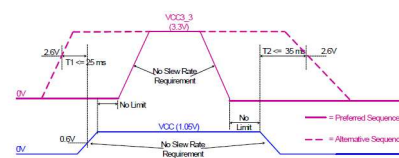


Block Diagram

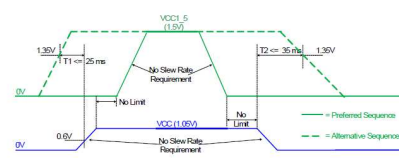




Sequencing Requirements between PCH VCC3_3 and VCC Core Rail

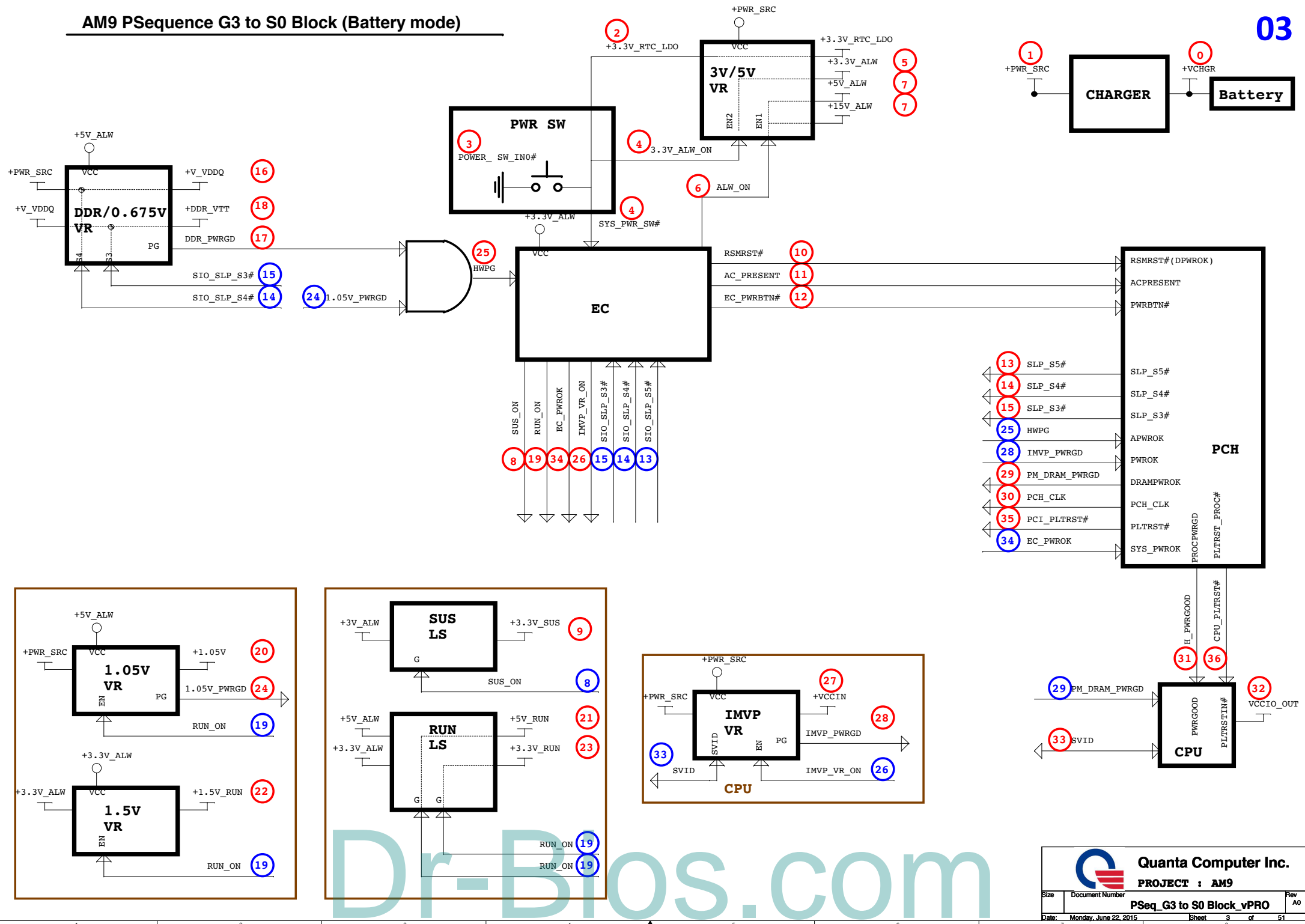


Sequencing Requirements between PCH VCC1_5 and VCC Core Rail

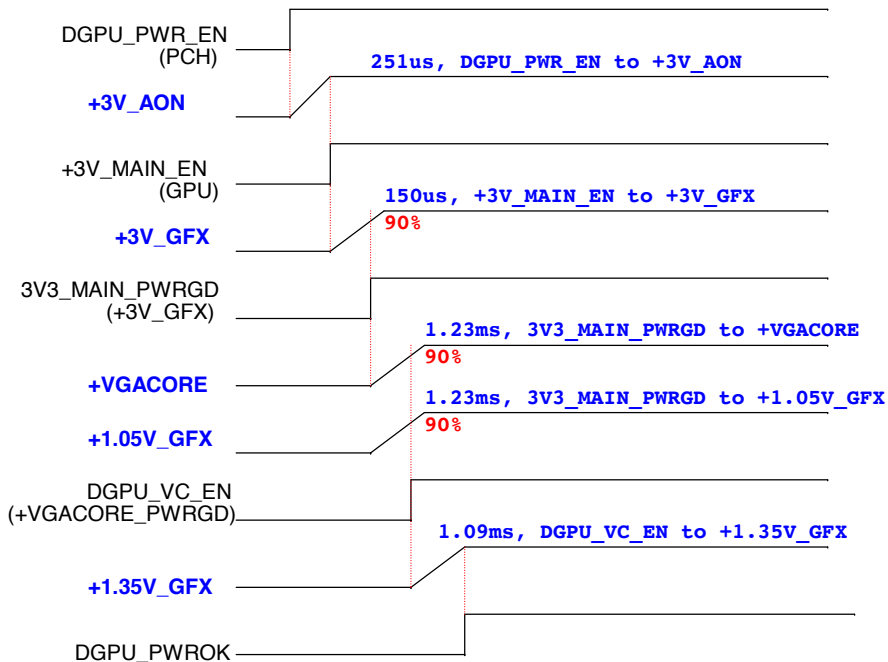


AM9 PSequence G3 to S0 Block (Battery mode)

03



AM9 GPU Power UP sequence

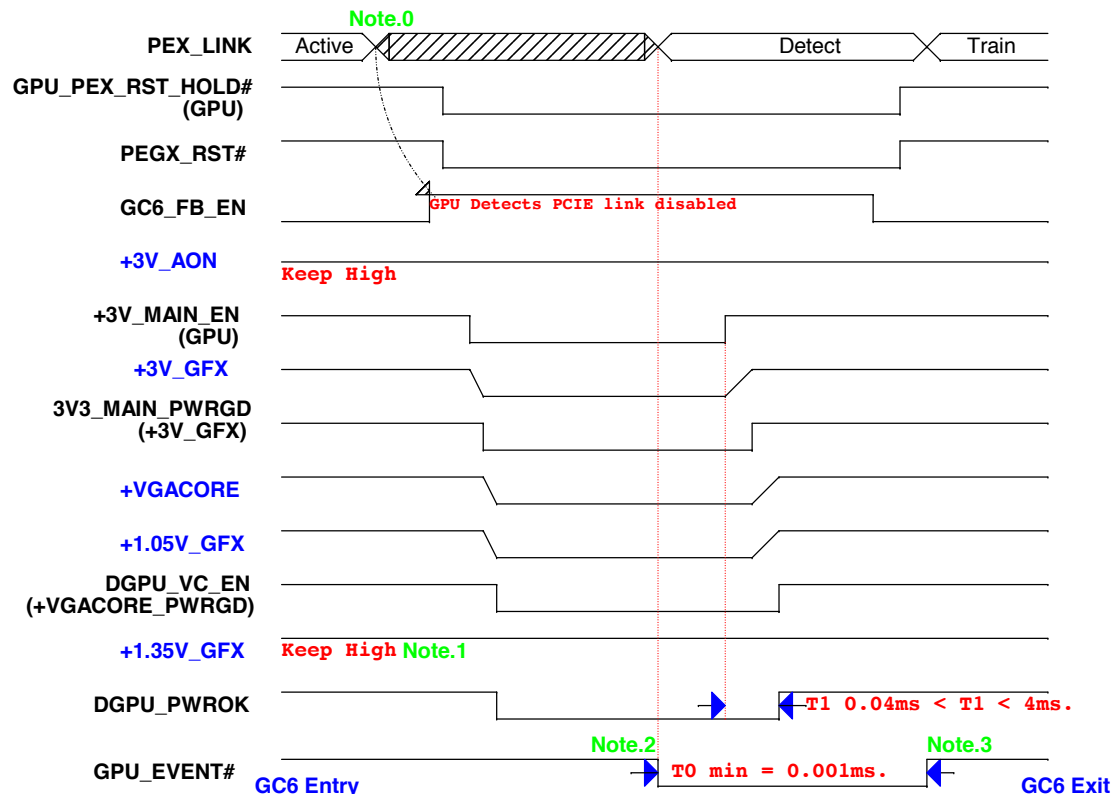


- The ramp time for any rail must be more than 40 μ s and is recommended to be less than 2ms.
- The ramp up overshoot should not exceed the silicon reliability limit voltage.
- A VDD33 must ramp up to 90% before NVVDD and PEXVDD in sequence can start ramping up. NVVDD must ramp up to 90% before FBVDD/Q in sequence can start ramping up

3.10.2.2 Power-Down Sequence

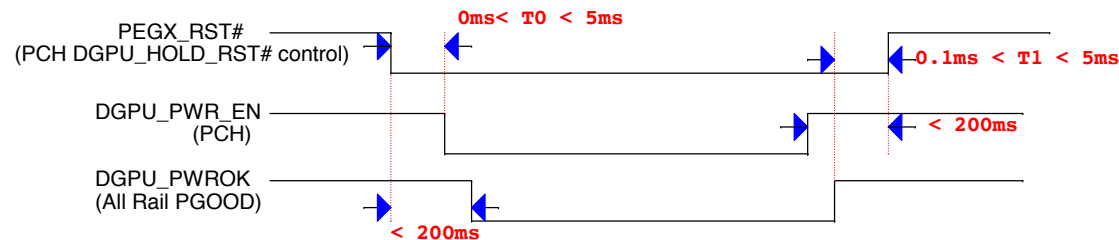
There is no specific power down sequence required. However, residual voltage from power down should not disrupt the power-up sequence when back to back GPU power-down and power-up take place.

AM9 GPU GC6 2.0 Entry/Exit sequence



AM9 Optimus GPU On/Off sequence

T0 = 220 us, PEGX_RST# to DGPU_PWR_EN
2.21 ms, DGPU_PWR_EN to DGPU_PWROK



P.S. The entire entry and exit sequence must complete within 200 ms

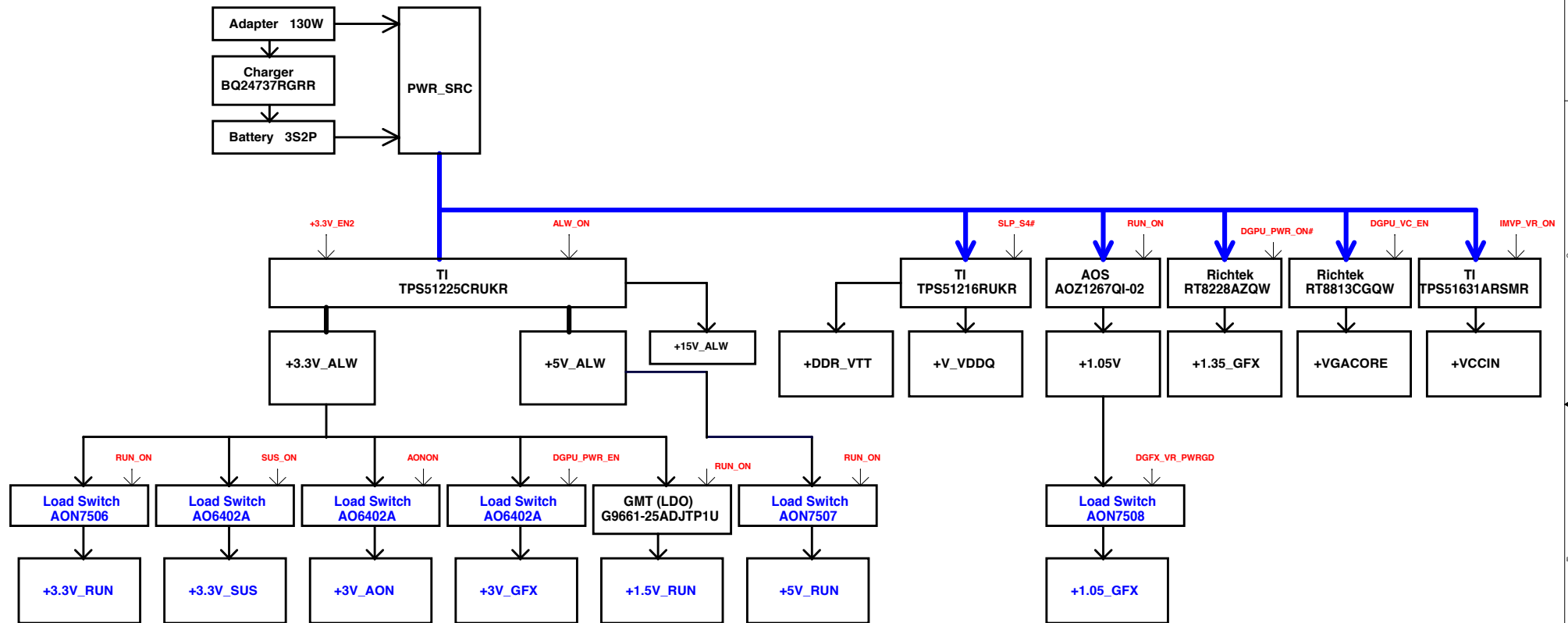


Quanta Computer Inc.

PROJECT : AM9

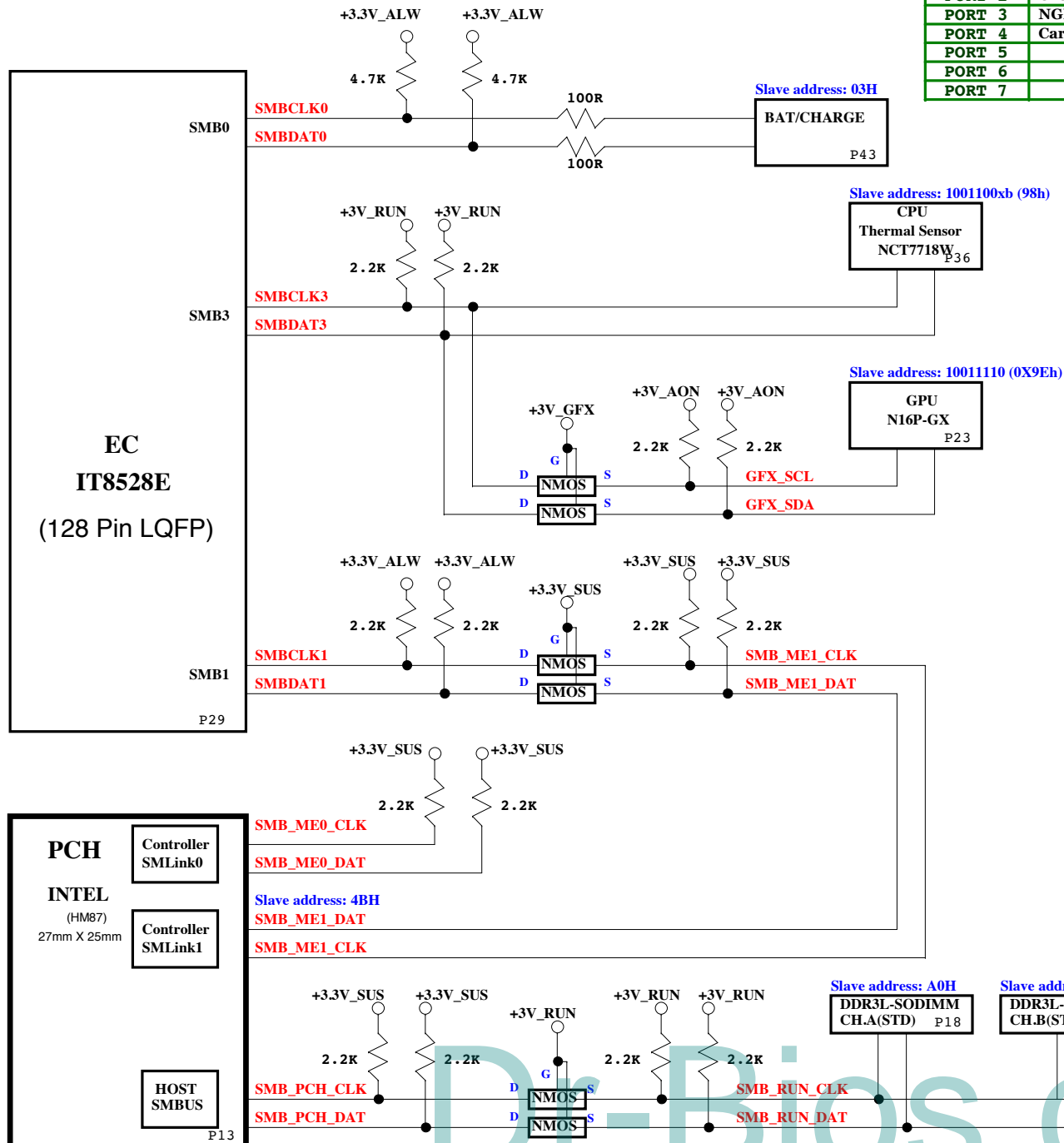
GPU Sequence

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		A0
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SMBus Block

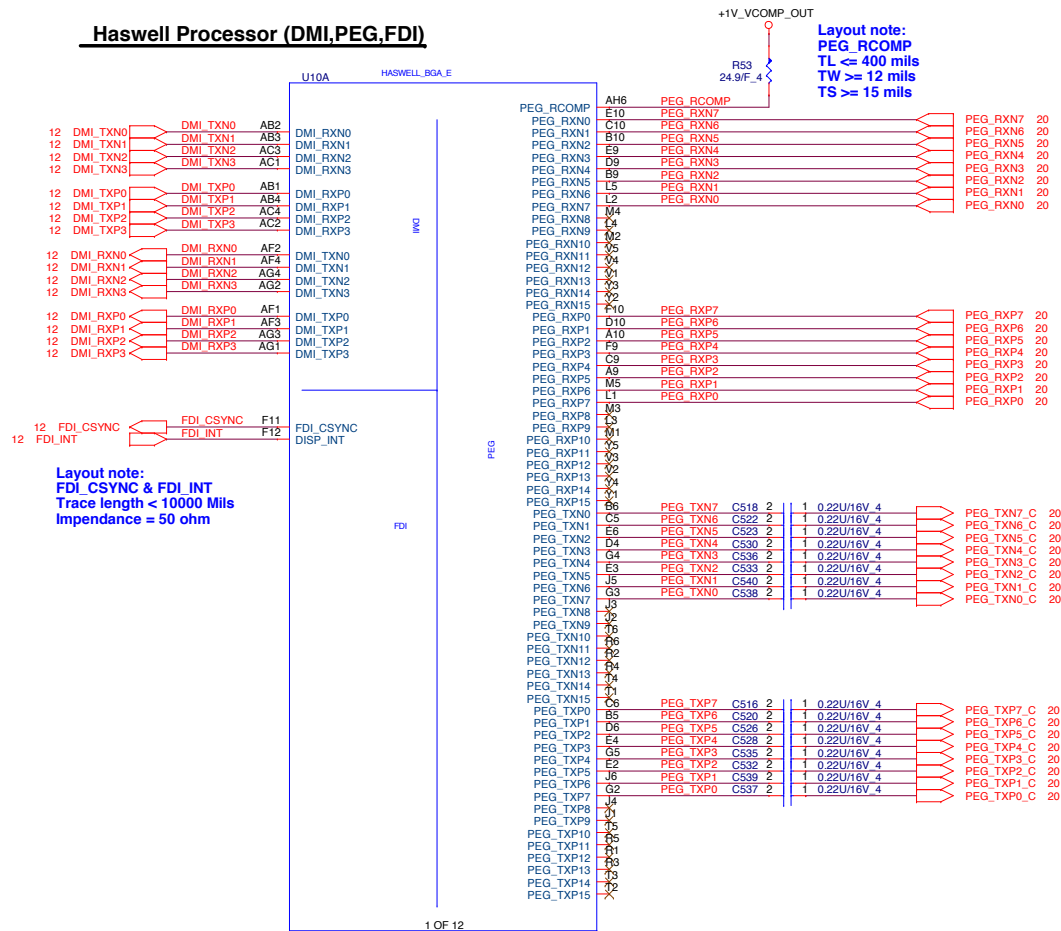


PCIe CLKOUT	
PORT 0	X
PORT 1	X
PORT 2	GIGA LAN
PORT 3	NGFF WLAN
PORT 4	Card reader
PORT 5	X
PORT 6	X
PORT 7	X

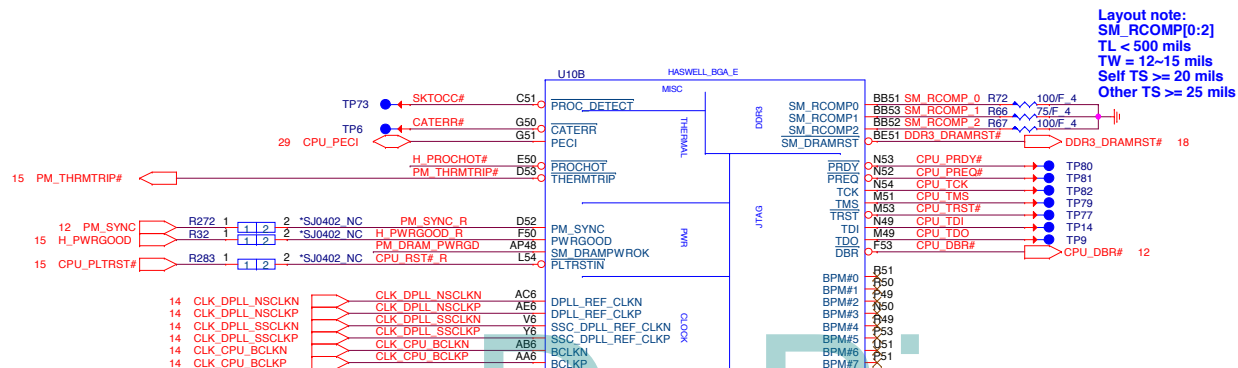
HSIO Port	HM87	AM9
PORT 1	USB3.0 PORT1	USB 3.0 CONN 1
PORT 2	USB3.0 PORT2	USB 3.0 CONN 2
PORT 3	USB3.0 PORT5	USB 3.0 CONN 3
PORT 4	USB3.0 PORT6	X
PORT 5	USB3.0 PORT3 PCIe* Port 1	X
PORT 6	USB3.0 PORT4 PCIe* Port 2	X
PORT 7	PCIe* Port 3	GIGA LAN
PORT 8	PCIe* Port 4	NGFF WLAN
PORT 9	PCIe* Port 5	Card Reader
PORT 10	PCIe* Port 6	X
PORT 11	PCIe* Port 7	X
PORT 12	PCIe* Port 8	X
PORT 13	PCIe* SATA 6Gb/s Port 1	SATA HDD
PORT 14	PCIe* SATA 6Gb/s Port 2	M.2(NGFF)SSD
PORT 15	SATA 6Gb/s Port 0	X
PORT 16	SATA 6Gb/s Port 1	X
PORT 17	SATA 3Gb/s Port 2	X
PORT 18	SATA 3Gb/s Port 3	X

USB 2.0			
EHCI #1		EHCI #2	
PORT 0	USB3.0 CONN / DB	PORT 8	Camera
PORT 1	USB3.0 Conn / DB	PORT 9	BT
PORT 2	X	PORT 10	Touch Panel
PORT 3	X	PORT 11	X
PORT 4	X	PORT 12	X
PORT 5	USB3.0 CONN / PS	PORT 13	X
PORT 6	X		
PORT 7	X		

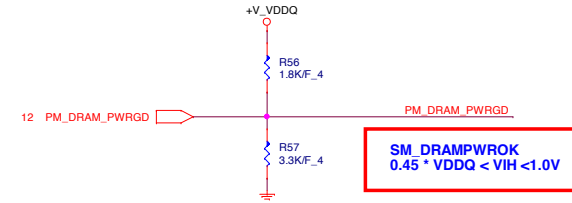
Haswell Processor (DMI,PEG,FDI)



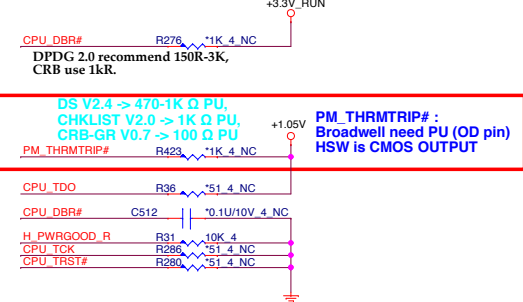
Haswell Processor (CLK,MISC,JTAG)



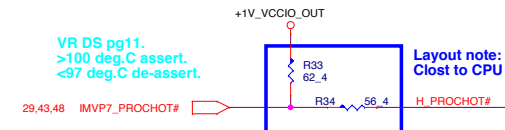
SM_DRAMPWROK# Topology



CPU PU/PD setting

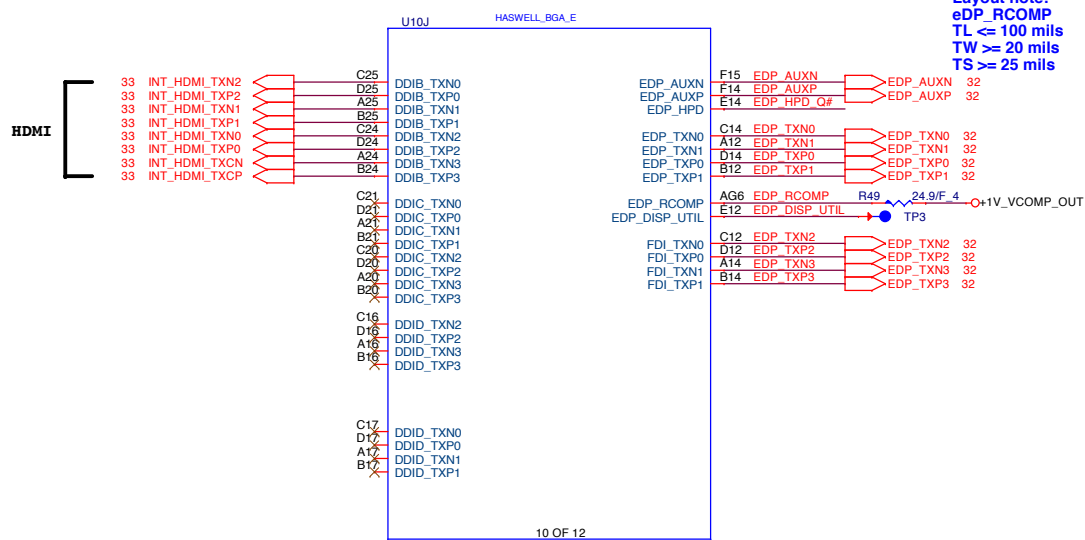


PROCHOT# Topology

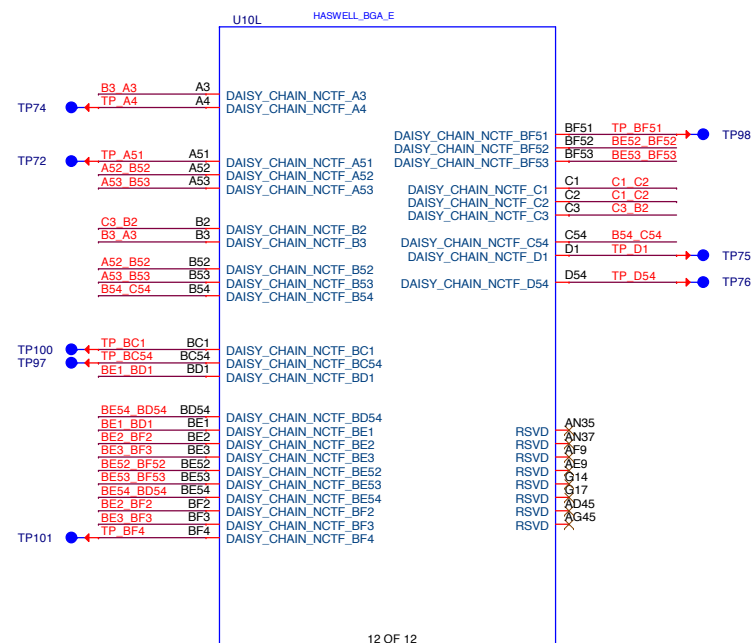




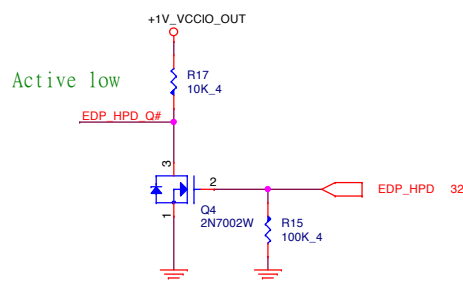
Haswell Processor (DDI,eDP,FDI)

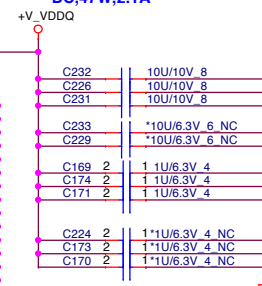


Layout note:
eDP_RCOMP
TL <= 100 mils
TW >= 20 mils
TS >= 25 mils



EDP_HPDP Level Shift



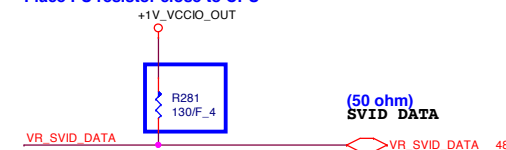


SVID

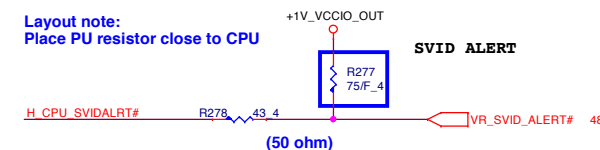
Layout note:
need routing
together and ALERT need
between CLK and DATA



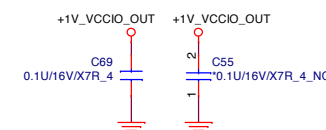
Layout note:
Place PU resistor close to CPU



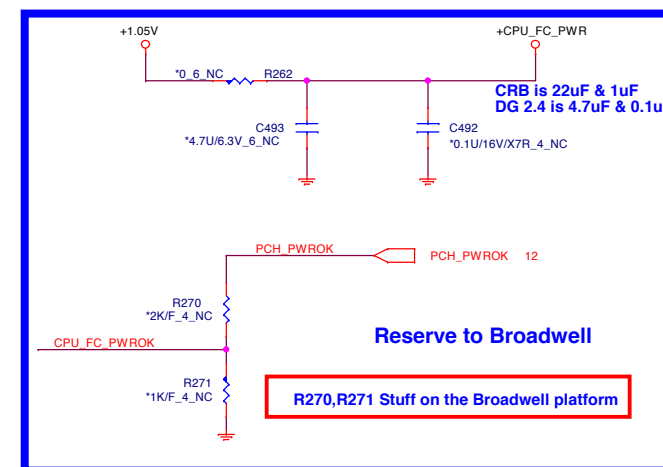
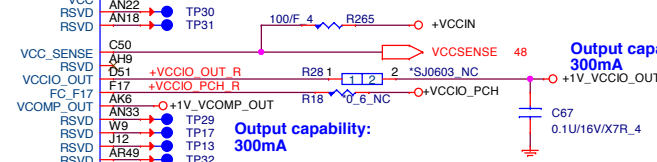
Layout note:
Place PU resistor close to CPU



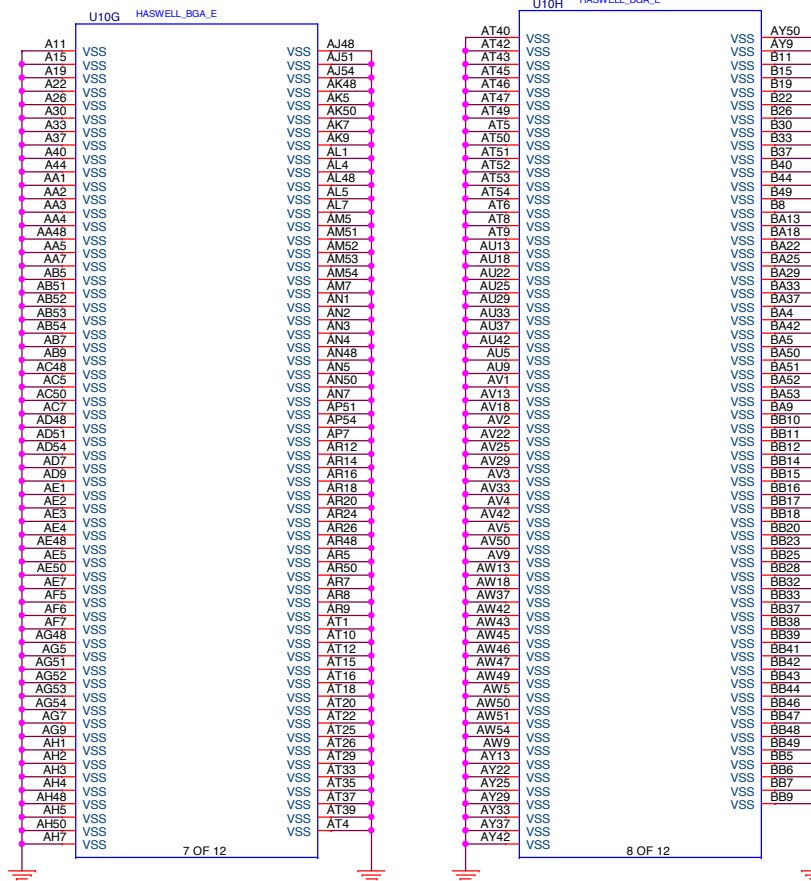
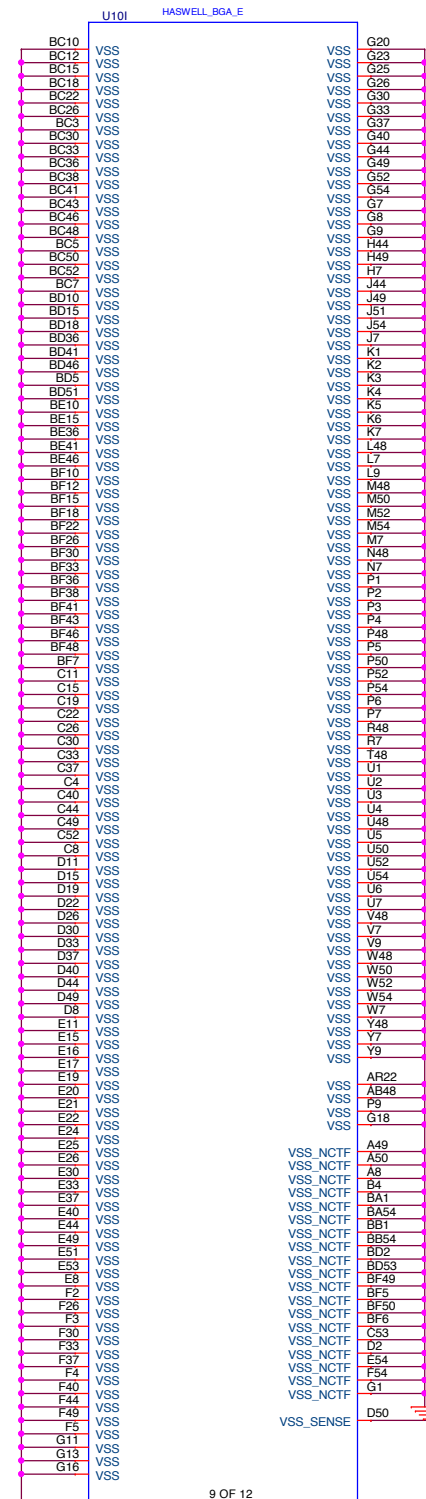
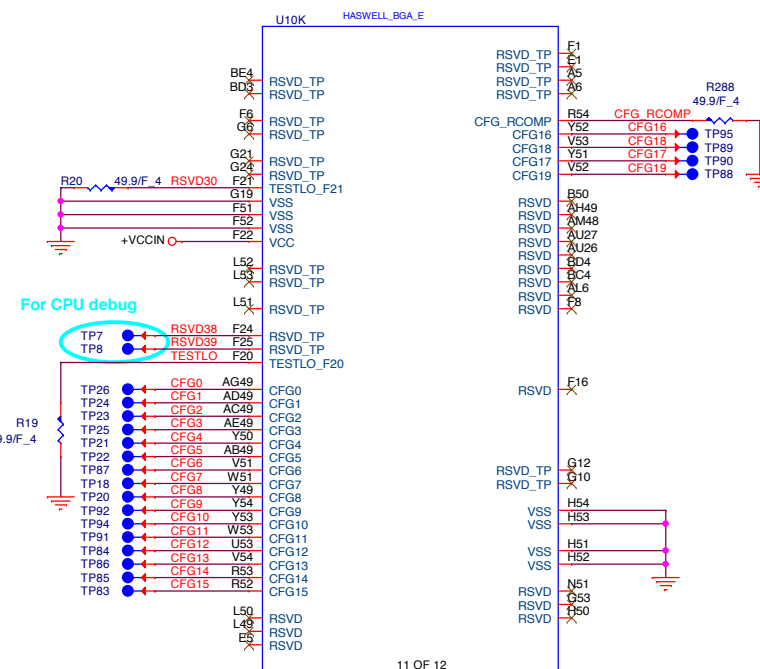
Output capability:



Output capability:
300mA



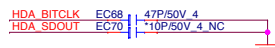
Haswell Processor (GND)

**Haswell Processor (CFG,RSVD)**

Configuration Signals:		The CFG signals have a default value of '1' if not terminated on the board.
CFG[2]	PCI Express Static Lane Reversal	<p>x1 = Normal operation x0 = Lane numbers reversed</p>
CFG[3]	MSR Privacy Bit Feature	<p>x1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting x0 = IA32_Debug_Interface_MSR (0xC80) bit[0]. Default setting overridden</p>
CFG[4]	eDP enable	<p>x1 = Disabled x0 = Enabled</p>
CFG[6:5]	PCI Express Bifurcation	<p>x00 = 1 x8 & 2 x4 PCI Express x01 = reserved x10 = 2 x8 PCI Express x11 = 1 x16 PCI Express</p>



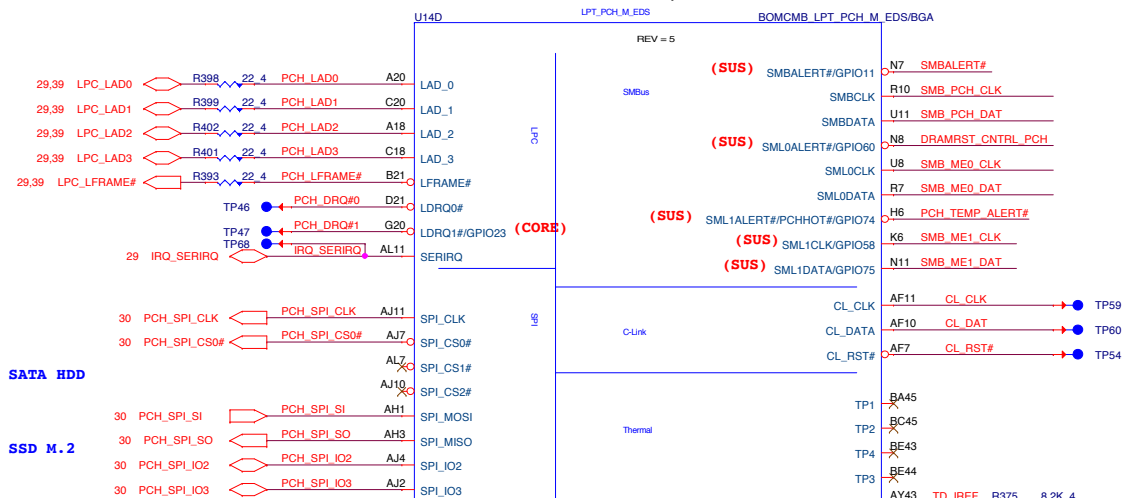
EMI



PCH STRAPING

Pin Name	Usage	Sampled	Configuration	Circuitry
SPKR	No Reboot	PWROK	0 = Disable (Int PD) 1 = Enable	
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	RSMRST#	0 = Disable 1 = Enable (Int PU)	
GPIO55	Top-Block Swap Override	PWROK	0 = Top-Block Swap mode 1 = Default (Int PU)	
INTVRMEN	Integrated VRM Enable	Always	0 = Disable 1 = Enable	
GPIO51	Boot BIOS Strap bit 1	PWROK	Bit1 Bit0 4 0 Reserved 1 1 SPI (default) 0 0 LPC	
SATA1GP/GPIO19	Boot BIOS Strap bit 0	PWROK		
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
DSWVREN	On Die DSW VR Enable	Always	0 = Disable 1 = Enable Must be PU to VCCRTC	
GPIO53	DMI AC / DC-Coupling Mode	PWROK	0 = DMI is in AC-coupling mode 1 = DMI is in DC-coupling mode (int PU)	
HDA_DOCK_EN# / GPIO33	DMI TX Termination	PWROK	0 = DMI TX is terminated to VSS (int PD) 1 = DMI TX is terminated to VCC/2	

Lynx Point (LPC,SPI,SMBUS,C-LINK,THERMAL)

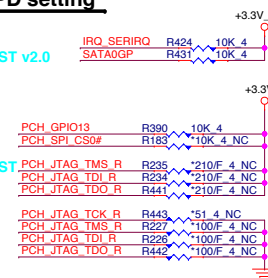


PCH PU/PD setting

Follow SCH CHKRST v2.0

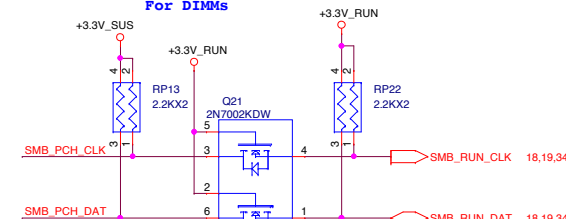
Follow DG v2.4

Follow SCH CHKRST
v2.0 pg27



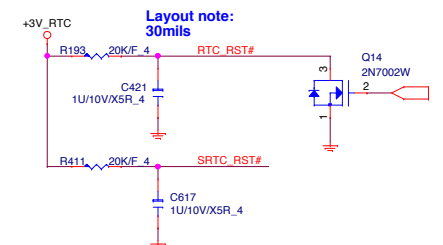
Leakage Isolation

For DIMMs

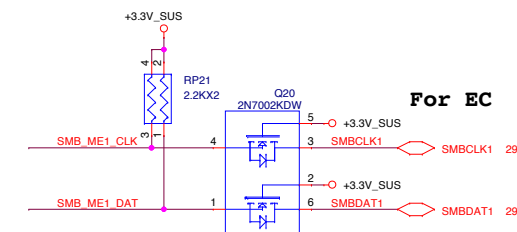
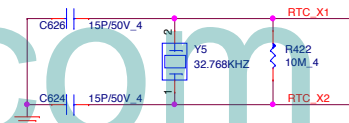


RTC Circuitry

Layout note:
30mils

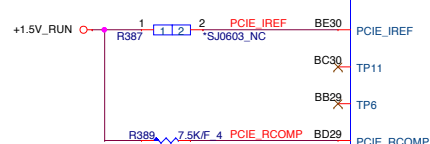
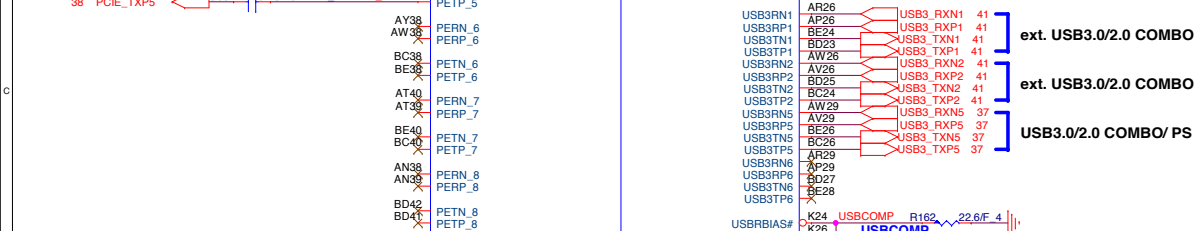
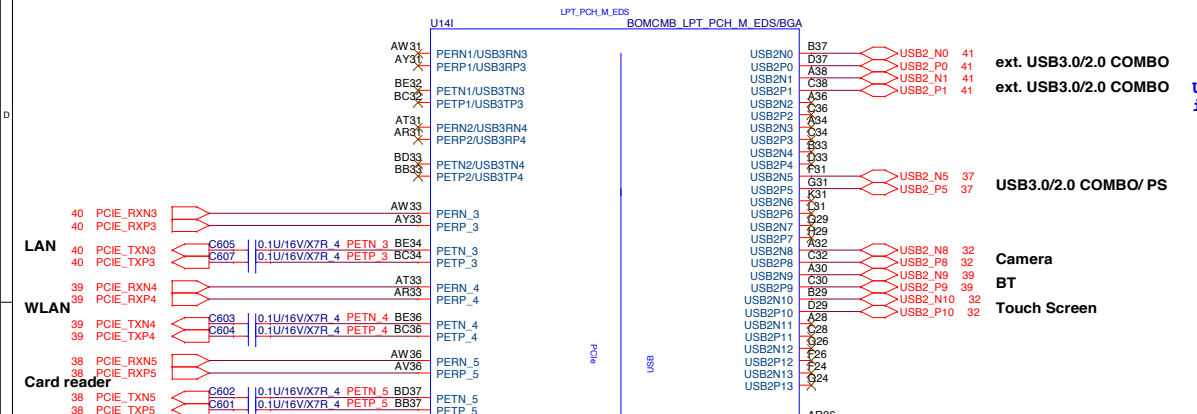


RTC Clock 32.768KHz

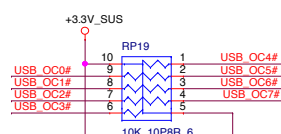


Lynx Point (PCIe, USB3.0, USB2.0)

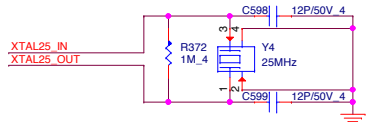
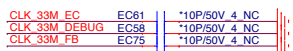
PCH PU/PD setting



Layout note:
PCIE_RCOMP/PCIE_IREF
(DC resistance routing < 0.2R)
BO TL <= 100 mils
TL <= 500 mils
BO TW >= 4 mils
TW = 12-15 mils
TS >= 12 mils



EMI



USB2.0 Port 1 & port 9
is debug port.

USB3.0/2.0 COMBO/ PS

Camera

BT

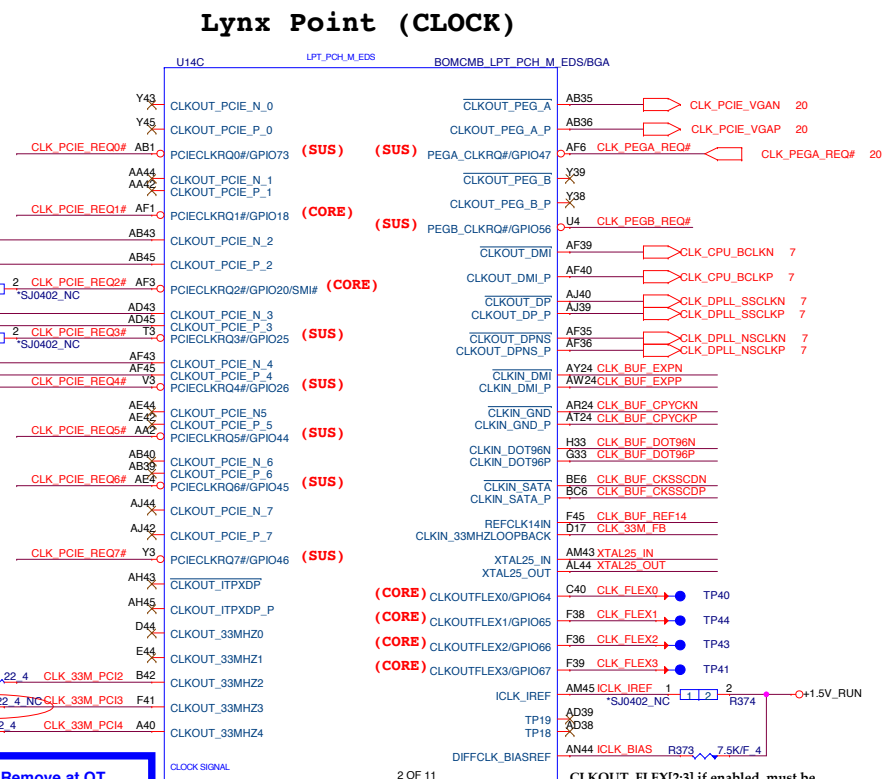
Touch Screen

ext. USB3.0/2.0 COMBO

ext. USB3.0/2.0 COMBO

USB3.0/2.0 COMBO/ PS

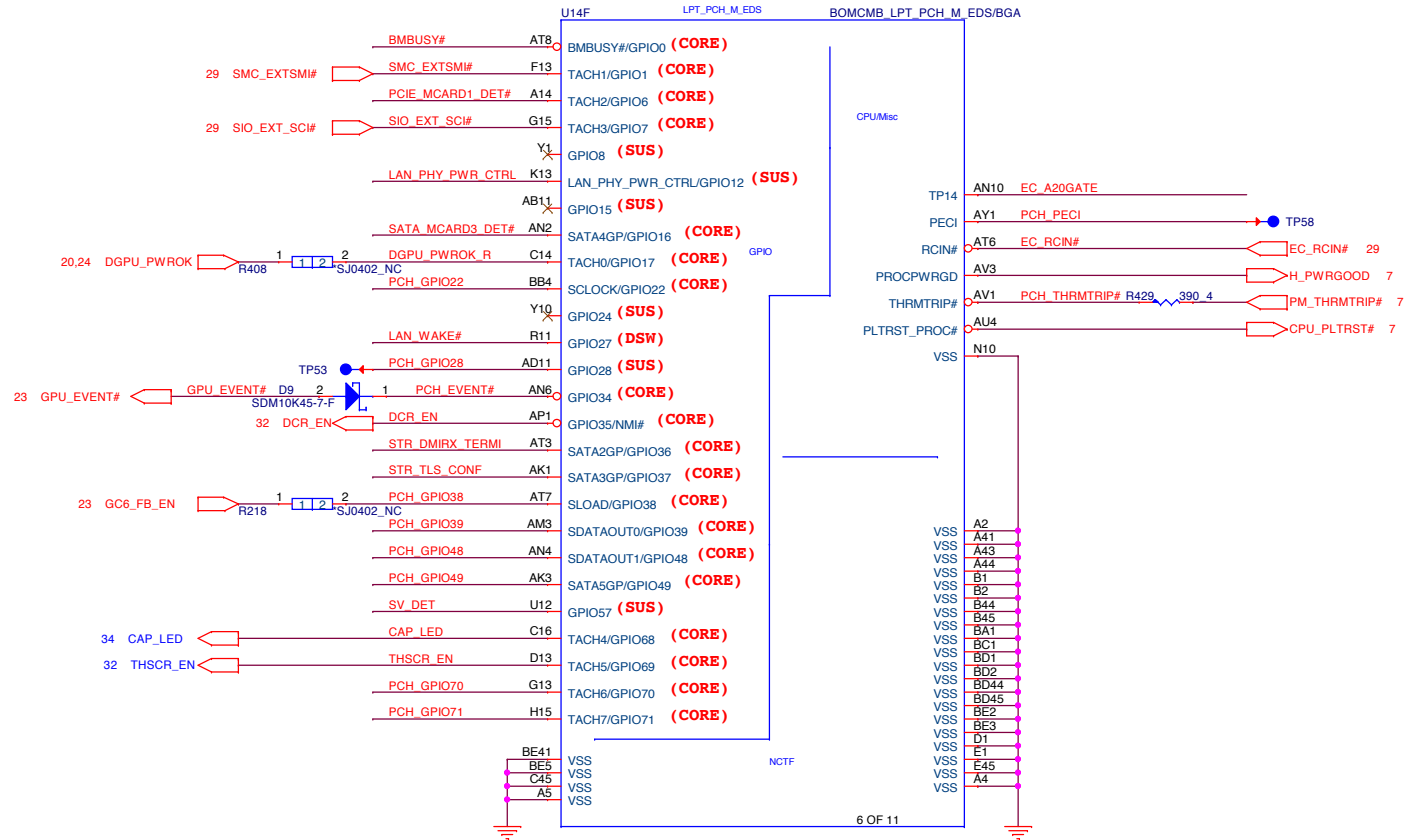
USBCOMP
Impedance = 50 Ohm
Trace length <= 500 mils
Trace spacing >= 15 mils



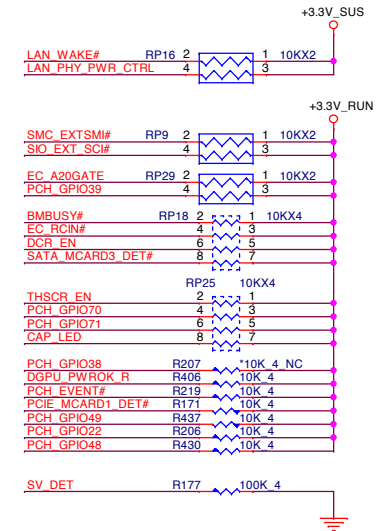
CLKOUT_FLEX[2:3] if enabled, must be programmed to the same clock frequency due to sharing the same internal power rail.

R380 For Debug Only, Remove at QT

Lynx Point (GPIO,CPU/MISC,NCTF)



PCH PU/PD setting



NOTE:

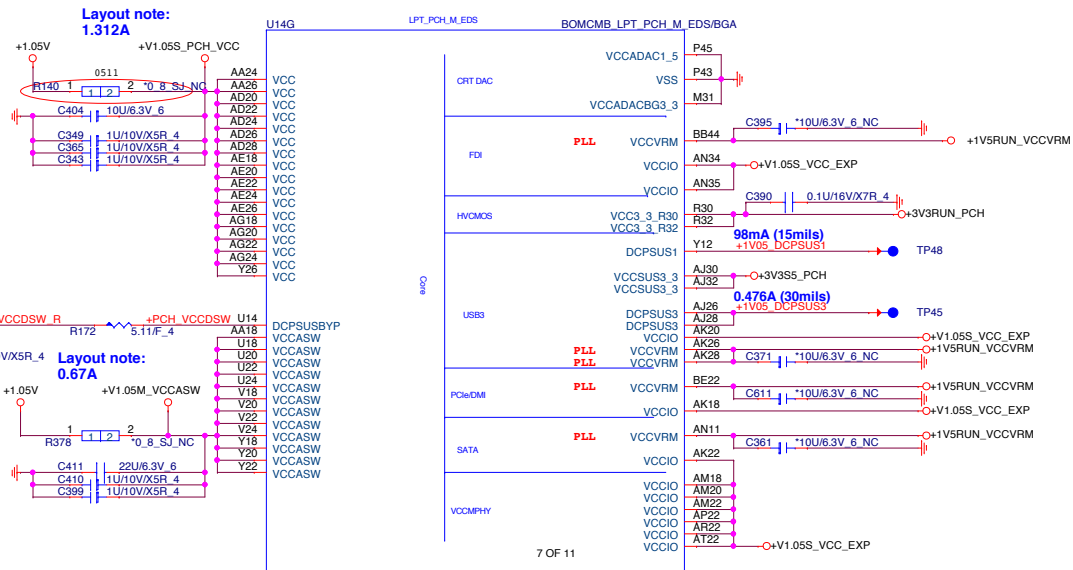
- 1.SATA_5_GP(GPIO49)CAN BE USE AS PCIE 2/MSATA 5 MUX SELECT IN LPT
- 2.Default GPI,can NOT be left floating

PCH Strap

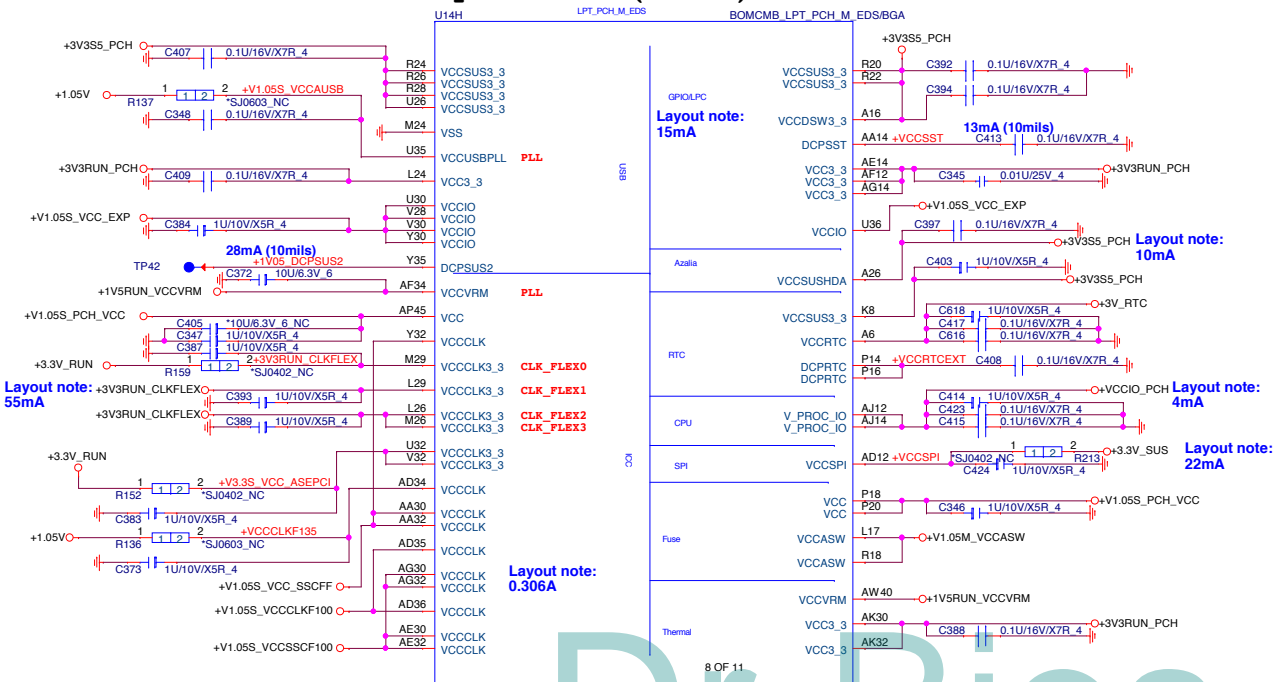
Pin Name	Usage	Sampled	Configuration	Ref. Doc.	Circuitry
SATA2GP / GPIO36	DMI RX Termination	Rising edge of PWROK	0 = DMI RX is terminated to VSS. 1 = DMI RX is terminated to VCC/2.	PCH EDS v2.3 SCH CHKLST v2.0	STR_DMIRX_TERMI R439 10K 4 R432 200K/F 4 NC +3.3V_RUN
SATA3GP / GPIO37	TLS Confidentiality	Rising edge of PWROK	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	PCH EDS v2.3 SCH CHKLST v2.0	STR_TLS_CONF R232 10K 4 R427 200K/F 4 NC +3.3V_RUN



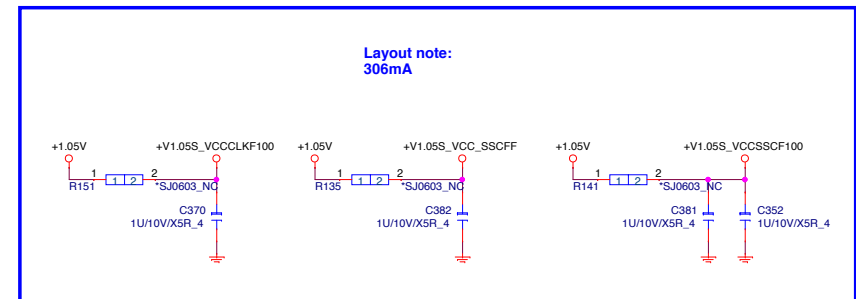
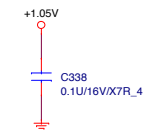
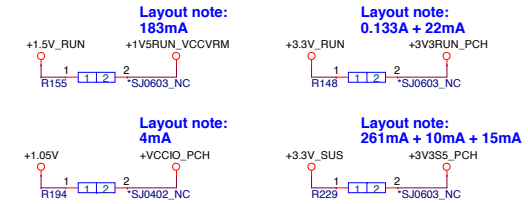
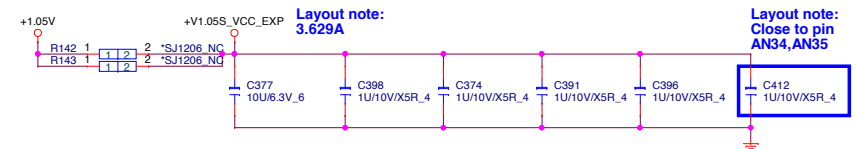
Lynx Point (Power)



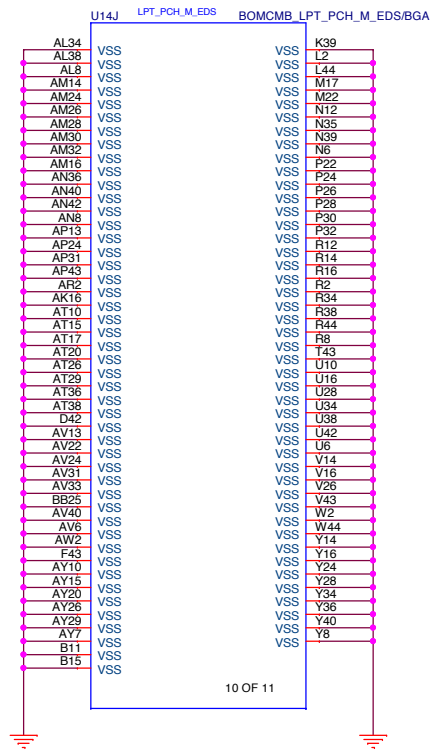
Lynx Point (Power)



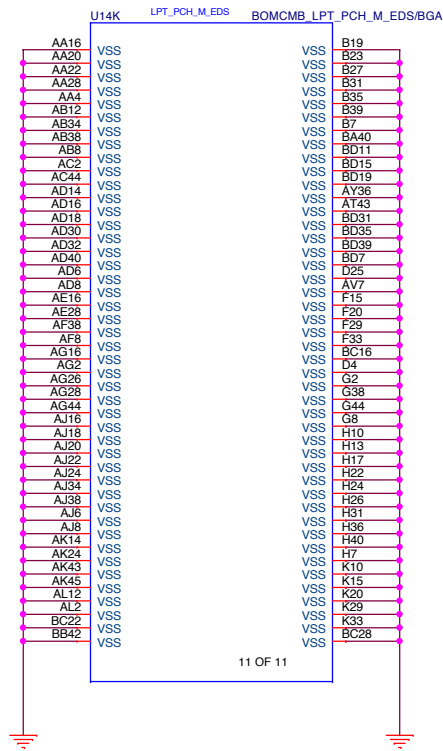
PCH VCCIO Power



Lynx Point (GND)



Lynx Point (GND)





1

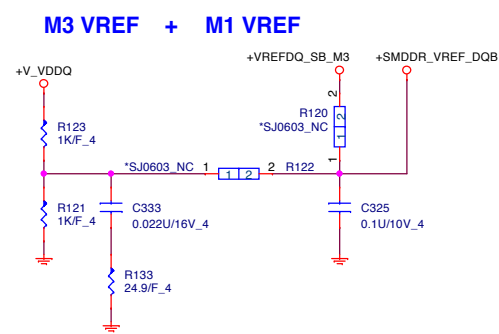
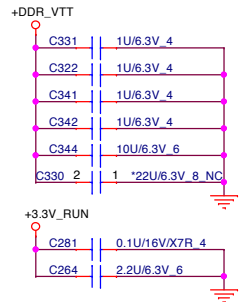
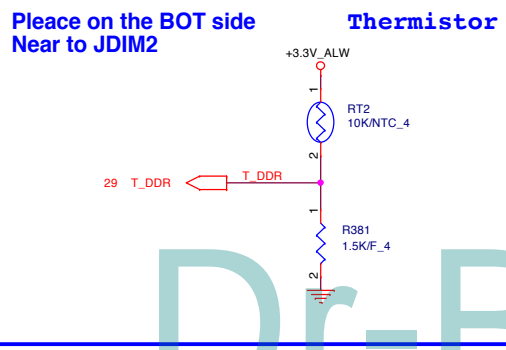
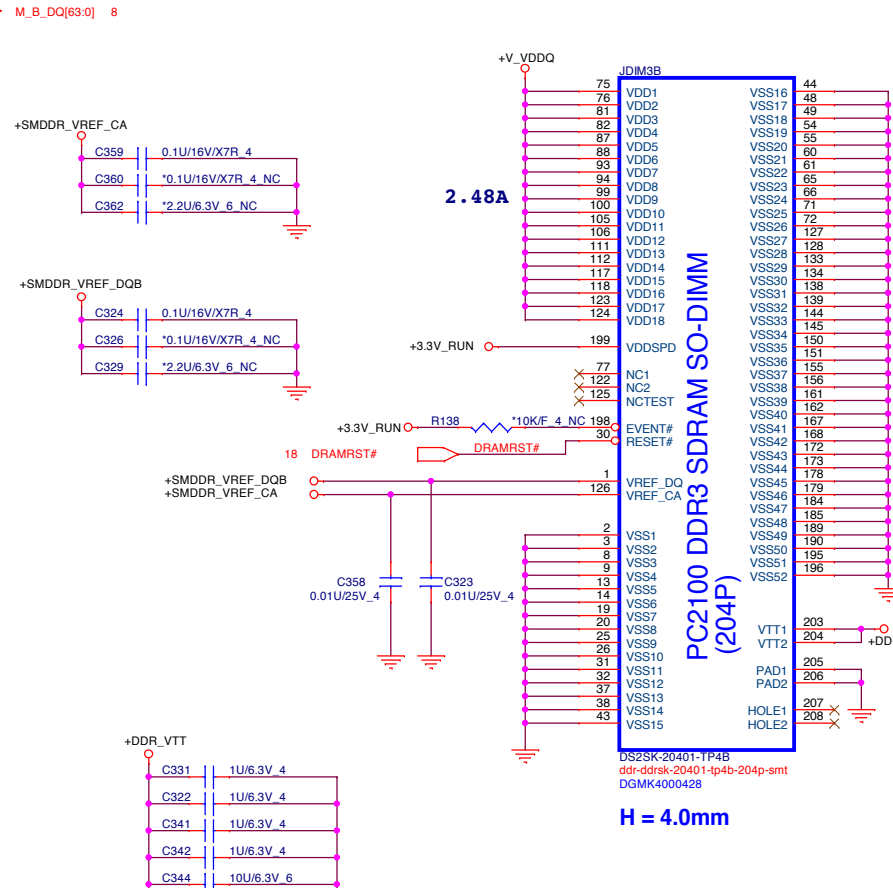


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PROJECT : AM9

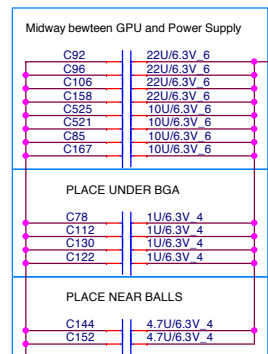
	B
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DG-07158-001 V05 PG51

PEX_IOVDD/Q : 3300mA

+1.05V_GFX

U11A
N16P-GX

[PEG Interface]

AG19 PEX_IOVDD_1
AG21 PEX_IOVDD_2
AG22 PEX_IOVDD_3
AG24 PEX_IOVDD_4
AH21 PEX_IOVDD_5
AH25 PEX_IOVDD_6
AG13 PEX_IOVDDQ_1
AG15 PEX_IOVDDQ_2
AG16 PEX_IOVDDQ_3
AG18 PEX_IOVDDQ_4
AG25 PEX_IOVDDQ_5
AH15 PEX_IOVDDQ_6
AH18 PEX_IOVDDQ_7
AH26 PEX_IOVDDQ_8
AH27 PEX_IOVDDQ_9
AJ27 PEX_IOVDDQ_10
AK27 PEX_IOVDDQ_11
AL27 PEX_IOVDDQ_12
AM28 PEX_IOVDDQ_13
AN28 PEX_IOVDDQ_14

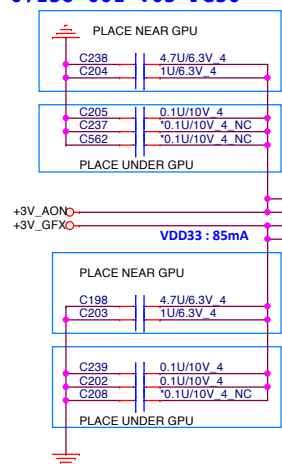
AN12 PEG_TXP0_C
AM12 PEG_TXN0_C
AN14 PEG_TXP1_C
AM14 PEG_TXN1_C
AP14 PEG_TXP2_C
AM15 PEG_TXN2_C
AN15 PEG_TXP3_C
AM15 PEG_TXN3_C
AN17 PEG_TXP4_C
AM17 PEG_TXN4_C
AP17 PEG_TXP5_C
AM18 PEG_TXN5_C
AN18 PEG_TXP6_C
AM20 PEG_TXN6_C
AN20 PEG_TXP7_C
AP20 PEG_TXN7_C

AP21 PEG_TXP0_C
AN21 PEG_TXN0_C
AM21 PEG_TXP1_C
AN23 PEG_TXN1_C
AP23 PEG_TXP2_C
AN24 PEG_TXN2_C
AM24 PEG_TXN3_C
AN26 PEG_TXN4_C
AP26 PEG_TXN5_C
AN27 PEG_TXN6_C
AM27 PEG_TXN7_C

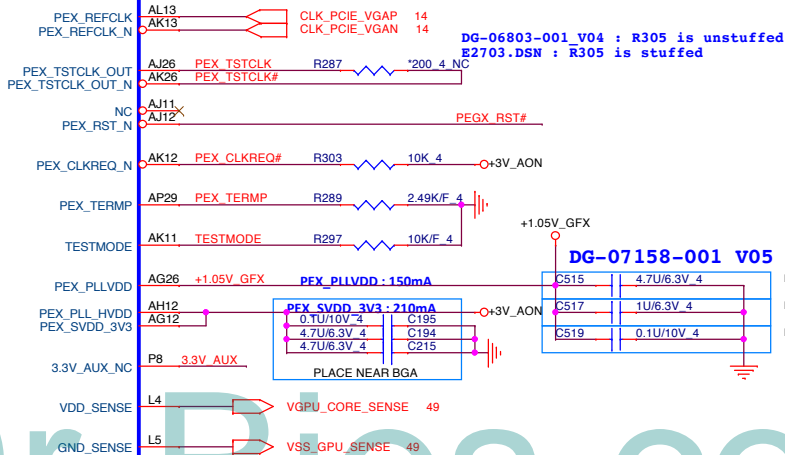
AK14 PEG_RXP0_C C192 2 1 0.22U/16V 4
AJ14 PEG_RXN0_C C199 2 1 0.22U/16V 4
AH14 PEG_RXP1_C C201 2 1 0.22U/16V 4
AG14 PEG_RXN1_C C211 2 1 0.22U/16V 4
AK15 PEG_RXP2_C C189 2 1 0.22U/16V 4
AJ15 PEG_RXN2_C C182 2 1 0.22U/16V 4
AL16 PEG_RXP3_C C164 2 1 0.22U/16V 4
AK16 PEG_RXN3_C C188 2 1 0.22U/16V 4
AK17 PEG_RXP4_C C181 2 1 0.22U/16V 4
AJ17 PEG_RXN4_C C175 2 1 0.22U/16V 4
AH17 PEG_RXP5_C C155 2 1 0.22U/16V 4
AG17 PEG_RXN5_C C163 2 1 0.22U/16V 4
AK18 PEG_RXP6_C C154 2 1 0.22U/16V 4
AJ18 PEG_RXN6_C C145 2 1 0.22U/16V 4
AL19 PEG_RXP7_C C143 2 1 0.22U/16V 4
AK19 PEG_RXN7_C C137 2 1 0.22U/16V 4

AC6 NC. 1
AJ28 NC. 2
AJ4 NC. 3
AJ5 NC. 4
AL11 NC. 5
C15 NC. 6
D19 NC. 7
D20 NC. 8
D23 NC. 9
D26 NC. 10
H31 NC. 11
T8 NC. 12
V32 NC. 13
Y1 NC. 14
Y2 NC. 15
AA1 NC. 16
AA2 NC. 17
AA3 NC. 18
AA4 NC. 19
AA5 NC. 20
AA6 NC. 21
AA7 NC. 22
AA8 NC. 23
AA8 NC. 24

DG-07158-001 V05 PG56



+3V_AON
+3V_GFX
VDD33 : 85mA



DG-07158-001 V05 PG52

+1.05V_GFX

PEX_PLIVDD : 150mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

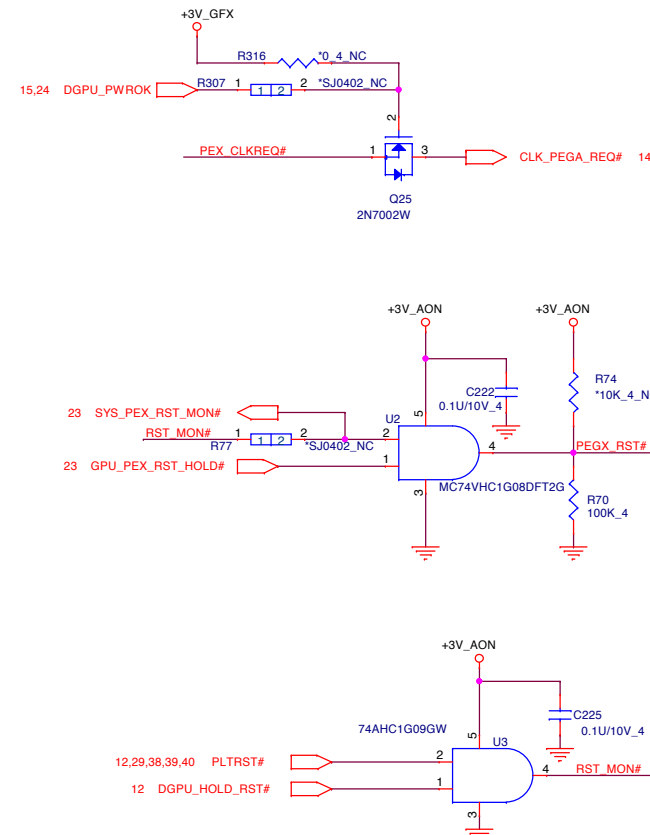
PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA

PEX_SVDD_3V3 : 210mA



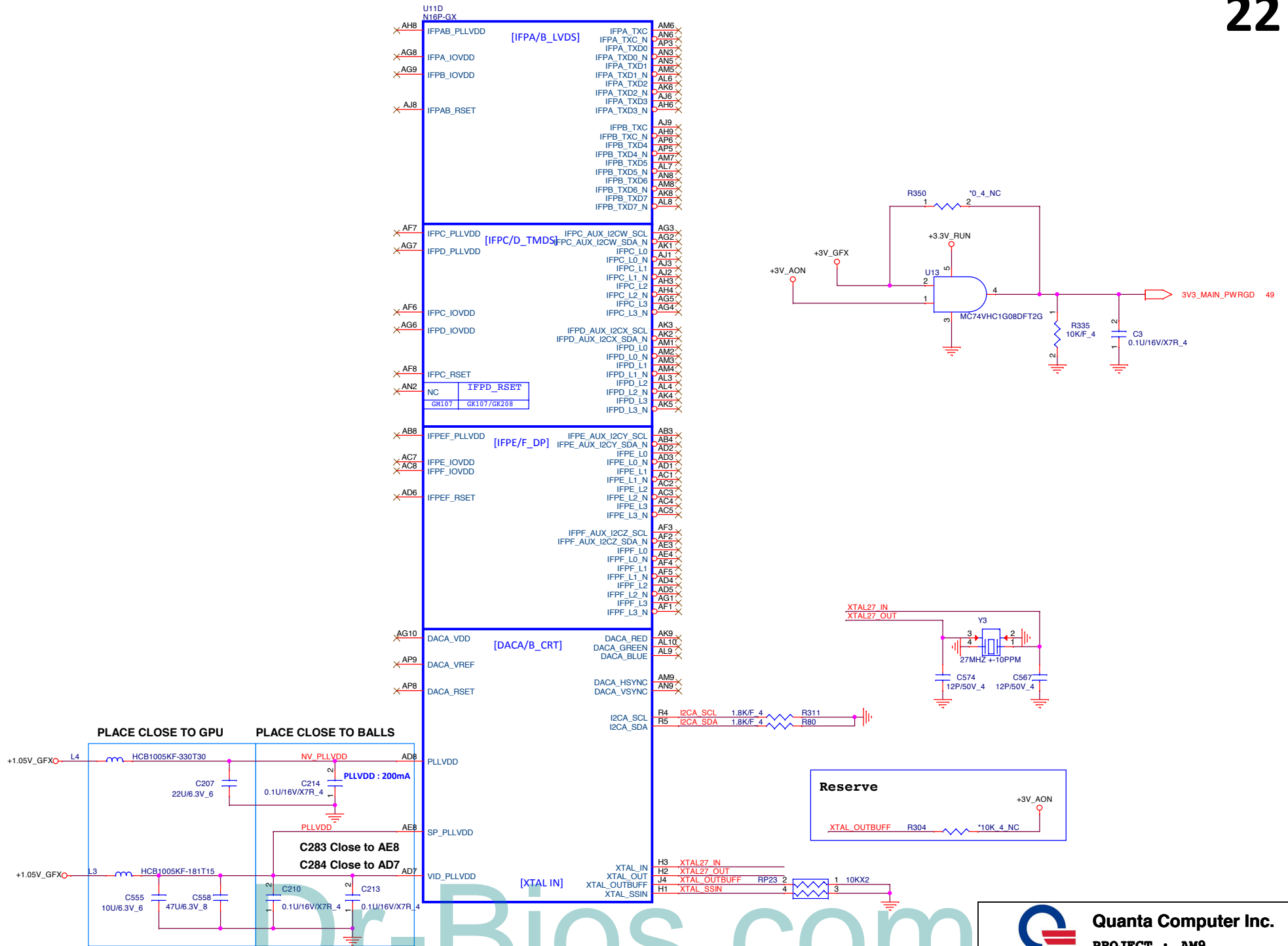
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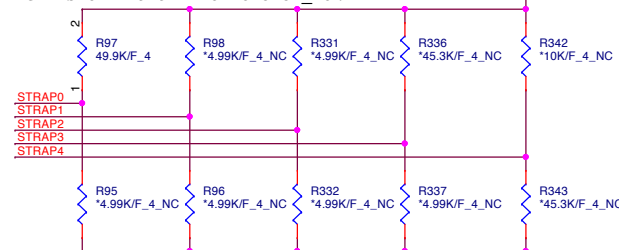
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U11E
N16P-GX

[MIOA]

STRAP0
DG : STUFF 49.9KΩ PU TO 3.3V_AON

Default : Sam 4Gb VRAM (Hynix : Strap = 0X6H ;Micron = 0X4H;SAMSUNG = 0X3H)

Vendor	Q : P/N	Mfr. P/N	ROM_SI	
Hynix (1.35V)	AKG5PWUTW14	H5GC4H24AJR-R0C	0110	34.8K PD
Micron (1.35V)	AKG5PW0TL01	EDW4032BABG-60-F	0100	24.9K PD
Samsung (1.35V)	AKG5PGDT500	K4G41325FC-HC03	0011	20K PD

4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1% (0402)
 10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
 15K/F 4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
 20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)
 24.9K/F 4: CS32492FB16 RES CHIP 24.9K 1/16W +1% (0402)
 30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)
 34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)
 45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

Logical Strap Bit Mapping

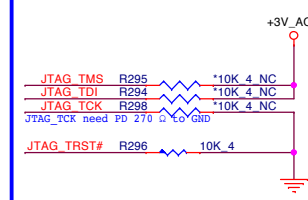
STRAP DECODE ACCORDING TO
TERMINATION RESISTANCE/VOLTAGE

TERMINATION RESISTANCE	TERMINATION VOLTAGE	
	3V3 [3:0]	GND [3:0]
5K	1000 8	0000 0
10K	1001 9	0001 1
15K	1010 A	0010 2
20K	1011 B	0011 3
25K	1100 C	0100 4
30K	1101 D	0101 5
35K	1110 E	0110 6
45K	1111 F	0111 7

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

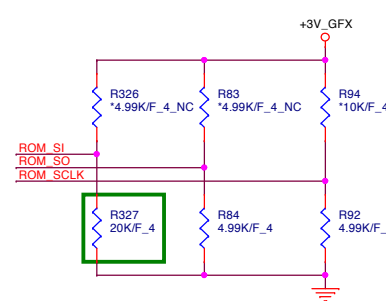
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				

Reserve PU/PD for Debug

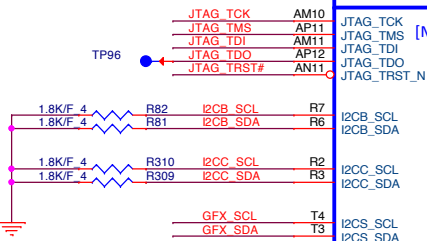
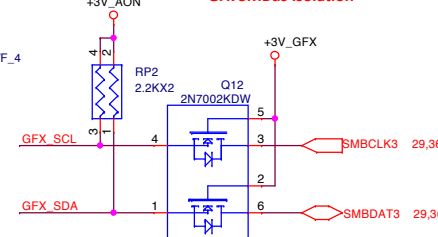


N16P-GX device ID= 0x139b

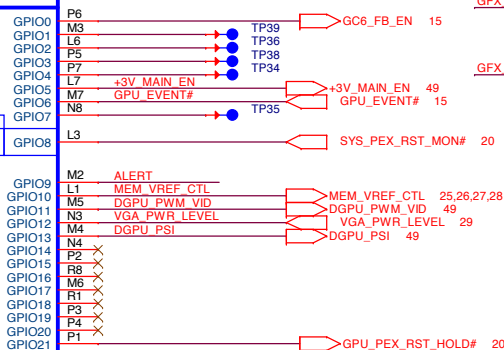
Netname	N16P-GX
ROM_SCLK	4.99K PD 0000
ROM_SO	4.99K PD 0000
STRAP0	49.9K PU



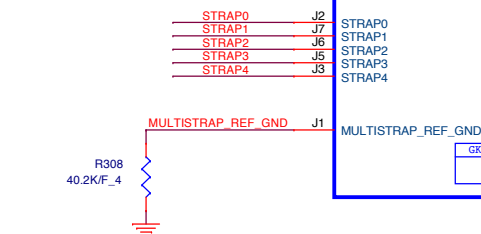
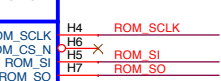
Gfx SMBus Isolation



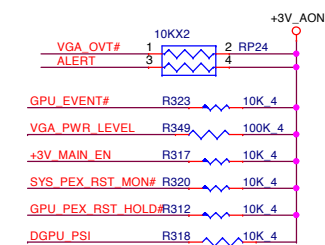
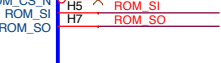
[MISC_GPIO/I2C/JTAG/THER]



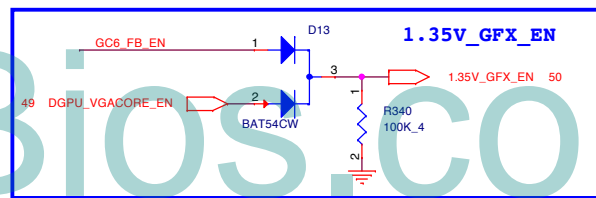
[MISC2_ROM]



[MISC2_ROM]



DG-07158--001 V05 PG182



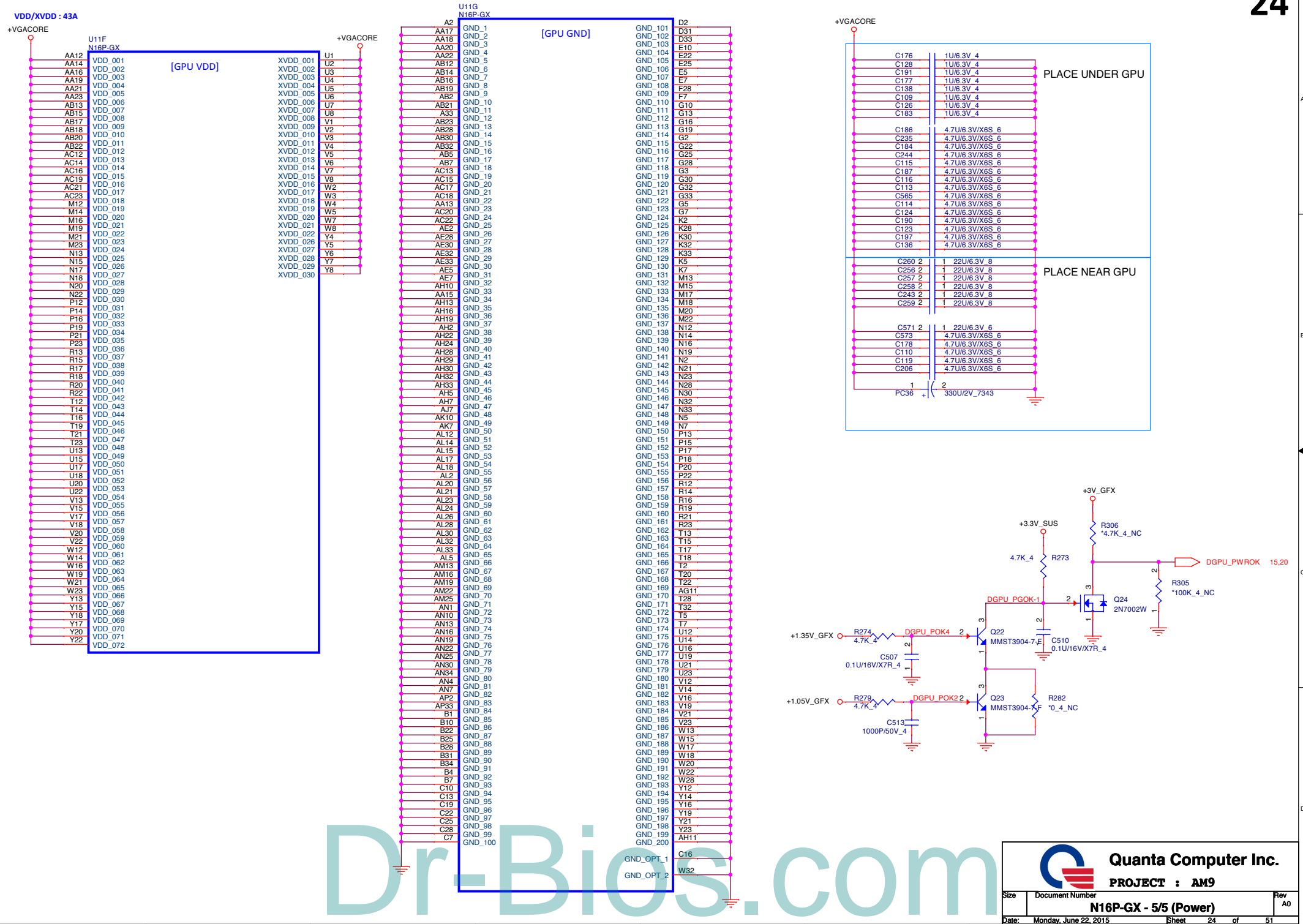
GPIO	GM107/GM108	GK208/GK107
GPIO 0	GC6_FB_EN	FB_CLAMP_MON
GPIO 1	MEM_VDD_CTL	MEM_VDD_CTL
GPIO 2	LCD_BL_PWM	LCD_BL_PWM
GPIO 3	LCD_PWR_EN	LCD_PWR_EN
GPIO 4	LCD_BL_EN	LCD_BL_EN
GPIO 5	GC6_PWR_EN	DBGCLAMP_TGL_REQ
GPIO 6	GPU_EVENT*	DBGCLAMP_TGL_REQ
GPIO 7	3D STEREO/DEBUG_SRVC	3D STEREO
GPIO 8	SYS_PEX_RST_MON*	OVERT*
GPIO 9	THERM_ALERT*/ERR_CORR	THERM_ALERT*/ERR_CORR
GPIO 10	MEM_VREF_CTL	MEM_VREF_CTL
GPIO 11	NVDDO_PWM_VID	NVDDO_PWM_VID
GPIO 12	AC DETECT	AC DETECT
GPIO 13	NVDDO_PSI	NVDDO_PSI
GPIO 14	IFPA HDP(not used for GM108)	IFPA HDP/FBCLAMP_TGL_REQ
GPIO 15	IFPC HDP(not used for GM108)	IFPC HDP
GPIO 16	FRAME LOCK	FRAME LOCK
GPIO 17	IFPD HDP(not used for GM108)	IFPD HDP
GPIO 18	IFPEF HDP(not used for GM108)	IFPEF HDP(not used for GK208)
GPIO 19	IFPB HDP(not used for GM108)	IFPB HDP
GPIO 20	GC6_MODE	N/A
GPIO 21	GPU_PEX_RST_HOLD*	N/A



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CHANNEL A: 2G/4G GDDR5

25

21,26 VMA_DQ[83..0] → VMA_DQ[83..0]
21,26 FBA_CMD[31..0] → FBA_CMD[31..0]
21,26 FBA_DB[7..0] → FBA_DB[7..0]
21,26 FBA_EDC[7..0] → FBA_EDC[7..0]

Channel 0
<0-7,16-23>
MF=0 Non-mirrored

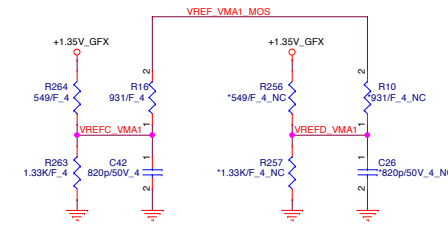
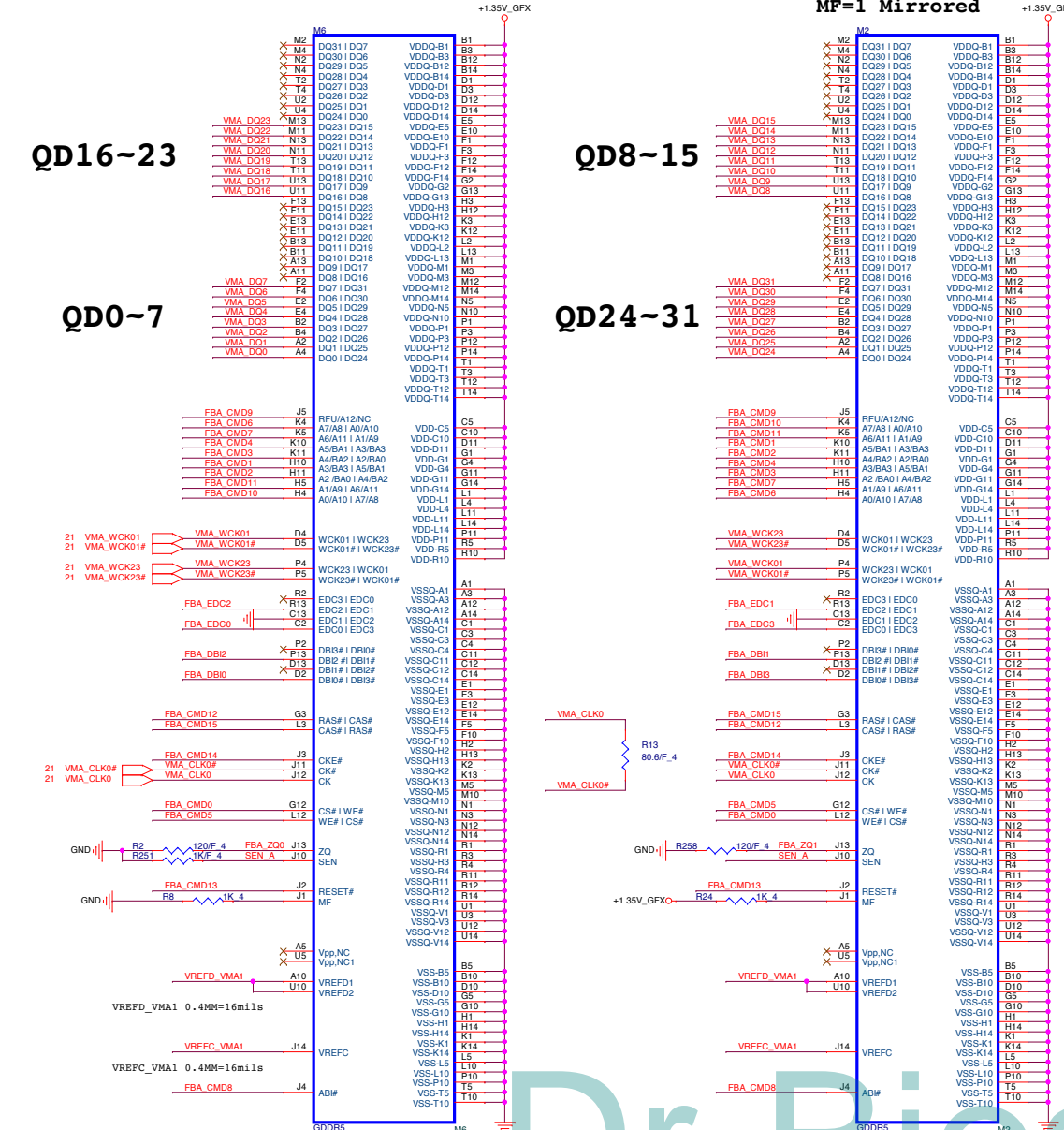
Channel 0
<8-15,24-31>
MF=1 Mirrored

QD16-23

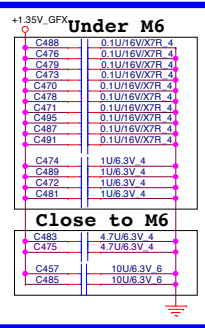
QD8-15

QD0-7

QD24-31



DG-07158-001 V05 PG49
Please close to M6



Please close to M2

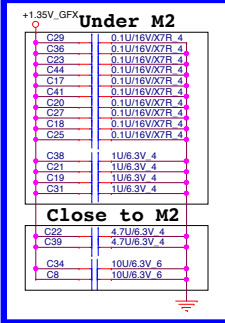


Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

CKE* is strap pin to set ODT value of memory chip
RST PD place @ the end of daisy-chain.

CHANNEL A: 2G/4G GDDR5

Channel 1

<32-39,48-55>

MF=0 Non-mirrored

Channel 1

<40-47,56-63>

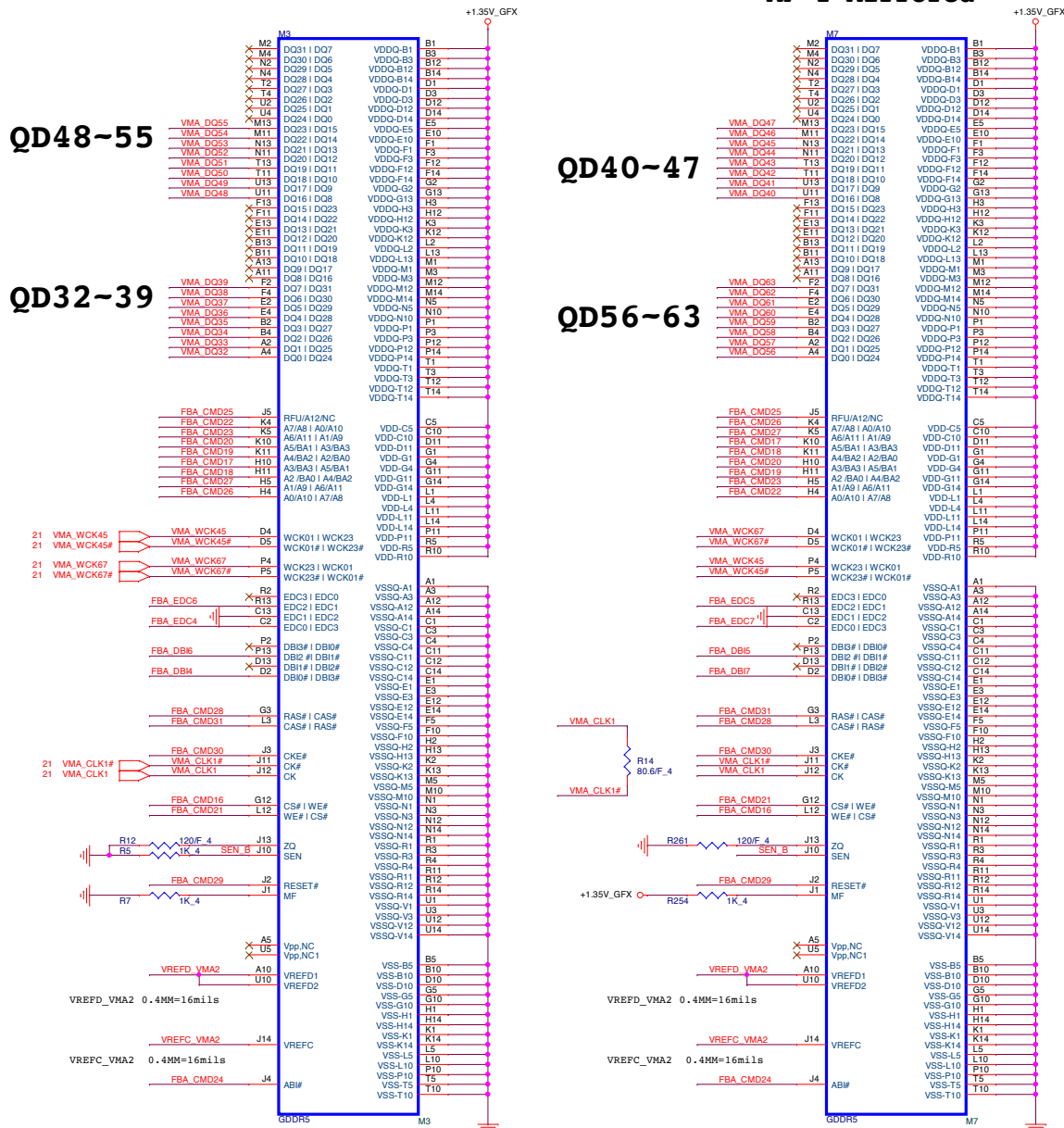
MF=1 Mirrored

QD48-55

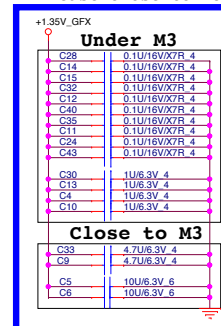
QD32-39

QD40-47

QD56-63



Please close to M3



Please close to M7

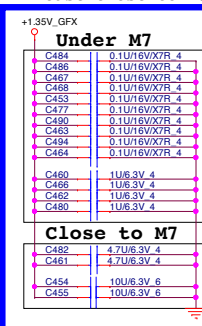
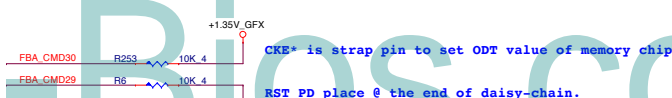


Table 4 Vendor ID to DQ mapping

Bit	7	6	5	4	3	2	1	0
MF=0	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
MF=1	DQ31	DQ30	DQ29	DQ28	DQ27	DQ26	DQ25	DQ24
Feature	Revision Identification				Manufacturers Vendor Code			
Bit	15	14	13	12	11	10	9	8
MF=0	DQ23	DQ22	DQ21	DQ20	DQ19	DQ18	DQ17	DQ16
MF=1	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8
Feature	RFU				Density			



21,28 VMC_DQ[63..0] VMC_DQ[63..0]
 21,28 FBC_CMD[31..0] FBC_CMD[31..0]
 21,28 FBC_DB[7..0] FBC_DB[7..0]
 21,28 FBC_EDC[7..0] FBC_EDC[7..0]

Channel 0
<0-7,16-23>
MF=0 Non-mirrored

QD16-23

QD0-7

FBC_CMD9 J5
 FBC_CMD8 K4
 FBC_CMD7 K5
 FBC_CMD4 K10
 FBC_CMD3 K11
 FBC_CMD1 H10
 FBC_CMD2 H11
 FBC_CMD11 H5
 FBC_CMD10 H4
 RFU/A12/NC
 A7/A8 | A9/A10
 A5/A11 | A3/BA3
 A4/BA2 | A2/BA0
 A3/BA1 | A5/BA1
 A2 | BA0 | A4/BA2
 A1/A9 | A6/A11
 A0/A10 | A7/A8

21 VMC_WCK01# VMC_WCK01#
 21 VMC_WCK01# VMC_WCK01#
 21 VMC_WCK23# VMC_WCK23#
 21 VMC_WCK23# VMC_WCK23#
 WCK01 | WCK23
 WCK01# | WCK23#
 WCK23 | WCK01
 WCK23# | WCK01#

FBC_EDC2 X R13
 FBC_EDC0 C13
 FBC_EDC0 C2
 FBC_DB2 X P13
 FBC_DB2 DB1# | DB2#
 FBC_DB0 X D2
 FBC_DB0 DB0# | DB3#

FBC_CMD12 G3
 FBC_CMD15 L3
 FBC_CMD14 J3
 VMC_CLK0# J11
 VMC_CLK0 J12

FBC_CMD0 G12
 FBC_CMD5 L12
 CS# | WE#
 WE# | CS#
 ZQ
 RESET#
 MF

R88 120F 4
 R79 1K 4
 SEN C J10
 R80 1K 4

VREFD_VMC1 A10
 VREFD2 U10

VREFC_VMC1 J14
 VREFC

FBC_CMD8 J4
 AB#

GDDR5 M9

+1.35V_GFX
 FBC_CMD14 R88 10K 4
 FBC_CMD13 R299 10K 4
 CKE* is strap pin to set ODT value of memory chip
 RST PD place @ the end of daisy-chain.

Channel 0
<8-15,24-31>
MF=1 Mirrored

QD8-15

QD24-31

FBC_CMD9 J5
 FBC_CMD8 K4
 FBC_CMD7 K5
 FBC_CMD4 K10
 FBC_CMD3 K11
 FBC_CMD1 H10
 FBC_CMD2 H11
 FBC_CMD11 H5
 FBC_CMD10 H4
 RFU/A12/NC
 A7/A8 | A9/A10
 A5/A11 | A3/BA3
 A4/BA2 | A2/BA0
 A3/BA1 | A5/BA1
 A2 | BA0 | A4/BA2
 A1/A9 | A6/A11
 A0/A10 | A7/A8

VMC_WCK33# D4
 VMC_WCK33# D5
 VMC_WCK01# P4
 VMC_WCK01# P5
 WCK01 | WCK23
 WCK01# | WCK23#
 WCK23 | WCK01
 WCK23# | WCK01#

FBC_EDC1 X R13
 FBC_EDC0 C13
 FBC_EDC0 C2
 FBC_DB1 X P13
 FBC_DB1 DB0# | DB3#
 FBC_DB3 X D2
 FBC_DB3 DB0# | DB3#

FBC_CMD15 G3
 FBC_CMD12 L3
 FBC_CMD14 J3
 VMC_CLK0# J11
 VMC_CLK0 J12

FBC_CMD5 G12
 FBC_CMD0 L12
 CS# | WE#
 WE# | CS#
 ZQ
 RESET#
 MF

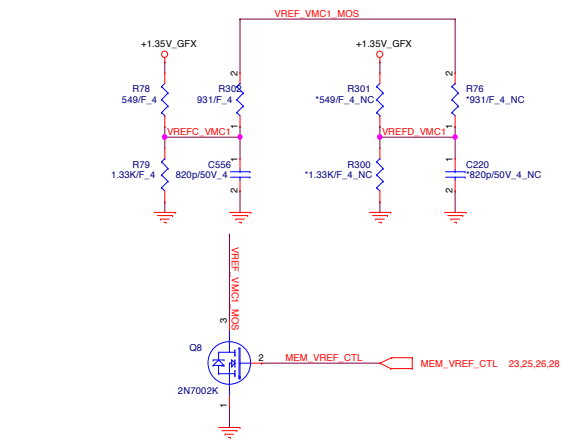
R87 120F 4
 R79 1K 4
 SEN C J10
 R80 1K 4

VREFD_VMC1 A10
 VREFD2 U10

VREFC_VMC1 J14
 VREFC

FBC_CMD8 J4
 AB#

GDDR5 M5



Please close to M9

Under M9

C581	0.1u/16V/X7R 4
C545	0.1u/16V/X7R 4
C547	0.1u/16V/X7R 4
C559	0.1u/16V/X7R 4
C549	0.1u/16V/X7R 4
C548	0.1u/16V/X7R 4
C576	0.1u/16V/X7R 4
C563	0.1u/16V/X7R 4
C577	0.1u/16V/X7R 4
C350	1u/6.3V 4
C572	1u/6.3V 4
C579	1u/6.3V 4
C566	1u/6.3V 4

Close to M9

C580	4.7u/6.3V 4
C575	4.7u/6.3V 4
C578	10u/6.3V 6
C551	10u/6.3V 6

Please close to M5

Under M5

C245	0.1u/16V/X7R 4
C160	0.1u/16V/X7R 4
C161	0.1u/16V/X7R 4
C233	0.1u/16V/X7R 4
C188	0.1u/16V/X7R 4
C162	0.1u/16V/X7R 4
C235	0.1u/16V/X7R 4
C247	0.1u/16V/X7R 4
C179	0.1u/16V/X7R 4
C228	0.1u/16V/X7R 4
C246	1u/6.3V 4
C234	1u/6.3V 4
C196	1u/6.3V 4
C252	1u/6.3V 4

Close to M5

C251	4.7u/6.3V 4
C242	4.7u/6.3V 4
C249	10u/6.3V 6
C209	10u/6.3V 6

Channel 1 <32-39,48-55>

MF=0 Non-mirrored

21.27 VMC_DQ[63..0] VMC_DQ[63..0]
21.27 FBC_CMD[31..0] FBC_CMD[31..0]
21.27 FBC_DB[7..0] FBC_DB[7..0]
21.27 FBC_EDC[7..0] FBC_EDC[7..0]

QD48-55

QD32-39

21 VMC_WCK45 VMC_WCK45#
21 VMC_WCK45# VMC_WCK45#
21 VMC_WCK67 VMC_WCK67#
21 VMC_WCK67# VMC_WCK67#

FBC_EDC8 FBC_EDC8#
FBC_EDC4 FBC_EDC4#
FBC_DB16 FBC_DB16#
FBC_DB14 FBC_DB14#

FBC_CMD28 FBC_CMD28#
FBC_CMD31 FBC_CMD31#

FBC_CMD30 FBC_CMD30#
FBC_CMD29 FBC_CMD29#

FBC_CMD16 FBC_CMD16#
FBC_CMD21 FBC_CMD21#

21 VMC_CLK1# VMC_CLK1#
21 VMC_CLK1 VMC_CLK1

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

Channel 1 <40-47,56-63>

MF=1 Mirrored

21.27 VMC_DQ[63..0] VMC_DQ[63..0]
21.27 FBC_CMD[31..0] FBC_CMD[31..0]
21.27 FBC_DB[7..0] FBC_DB[7..0]
21.27 FBC_EDC[7..0] FBC_EDC[7..0]

QD40-47

QD56-63

21 VMC_WCK45 VMC_WCK45#
21 VMC_WCK45# VMC_WCK45#
21 VMC_WCK67 VMC_WCK67#
21 VMC_WCK67# VMC_WCK67#

FBC_EDC8 FBC_EDC8#
FBC_EDC4 FBC_EDC4#
FBC_DB16 FBC_DB16#
FBC_DB14 FBC_DB14#

FBC_CMD28 FBC_CMD28#
FBC_CMD31 FBC_CMD31#

FBC_CMD30 FBC_CMD30#
FBC_CMD29 FBC_CMD29#

FBC_CMD16 FBC_CMD16#
FBC_CMD21 FBC_CMD21#

21 VMC_CLK1# VMC_CLK1#
21 VMC_CLK1 VMC_CLK1

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

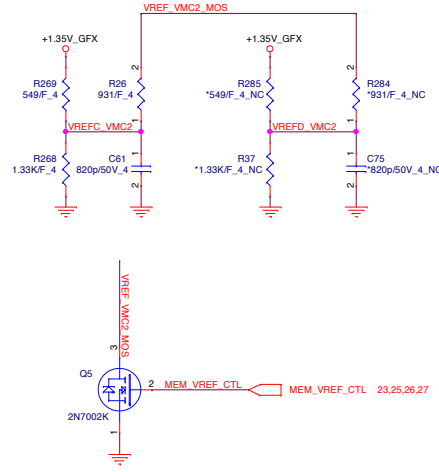
FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#

FBC_CMD29 FBC_CMD29#
FBC_CMD29 FBC_CMD29#



Please close to M4

Under M4

C58	0.1u/16V/X7R_4
C57	0.1u/16V/X7R_4
C100	0.1u/16V/X7R_4
C53	0.1u/16V/X7R_4
C141	0.1u/16V/X7R_4
C107	0.1u/16V/X7R_4
C140	0.1u/16V/X7R_4
C62	0.1u/16V/X7R_4
C139	0.1u/16V/X7R_4
C56	0.1u/16V/X7R_4
C68	1u/6.3V_4
C54	1u/6.3V_4
C94	1u/6.3V_4
C60	1u/6.3V_4

Close to M4

C59	4.7u/6.3V_4
C70	4.7u/6.3V_4
C56	10u/6.3V_6
C91	10u/6.3V_6

Please close to M8

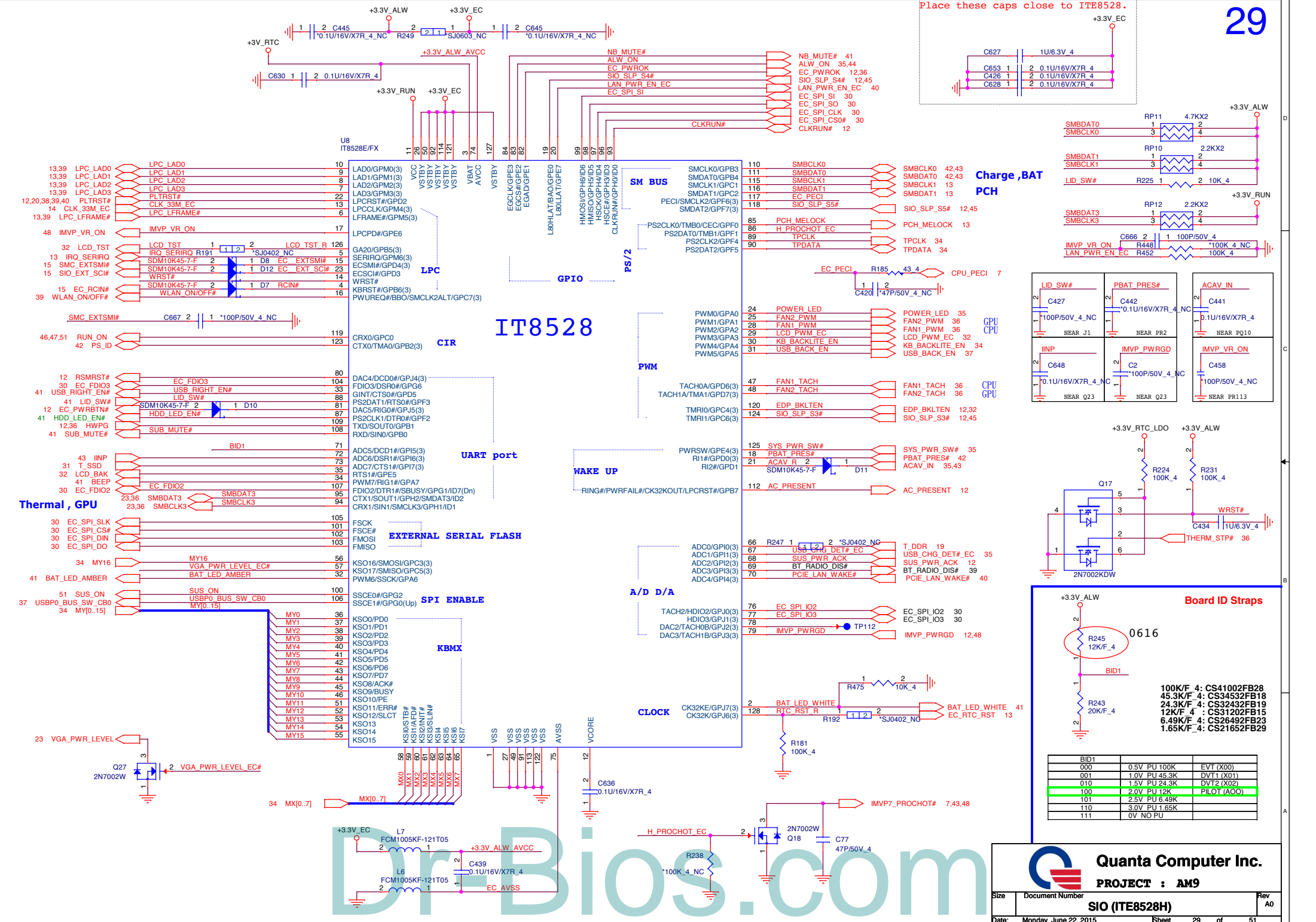
Under M8

C501	0.1u/16V/X7R_4
C543	0.1u/16V/X7R_4
C508	0.1u/16V/X7R_4
C531	0.1u/16V/X7R_4
C534	0.1u/16V/X7R_4
C542	0.1u/16V/X7R_4
C505	0.1u/16V/X7R_4
C500	0.1u/16V/X7R_4
C504	0.1u/16V/X7R_4
C502	1u/6.3V_4
C509	1u/6.3V_4
C541	1u/6.3V_4
C506	1u/6.3V_4

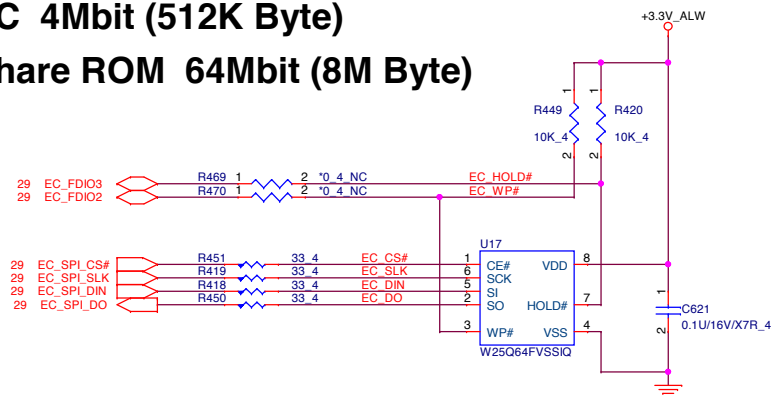
Close to M8

C503	4.7u/6.3V_4
C511	4.7u/6.3V_4
C524	10u/6.3V_6
C499	10u/6.3V_6

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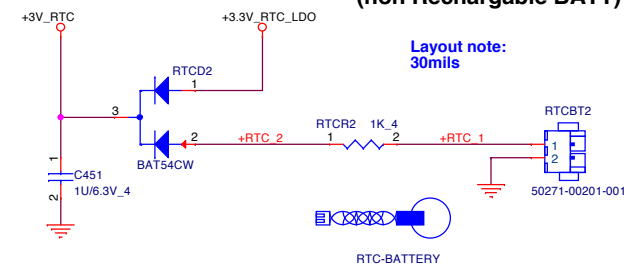


For EC 4Mbit (512K Byte)
For Share ROM 64Mbit (8M Byte)

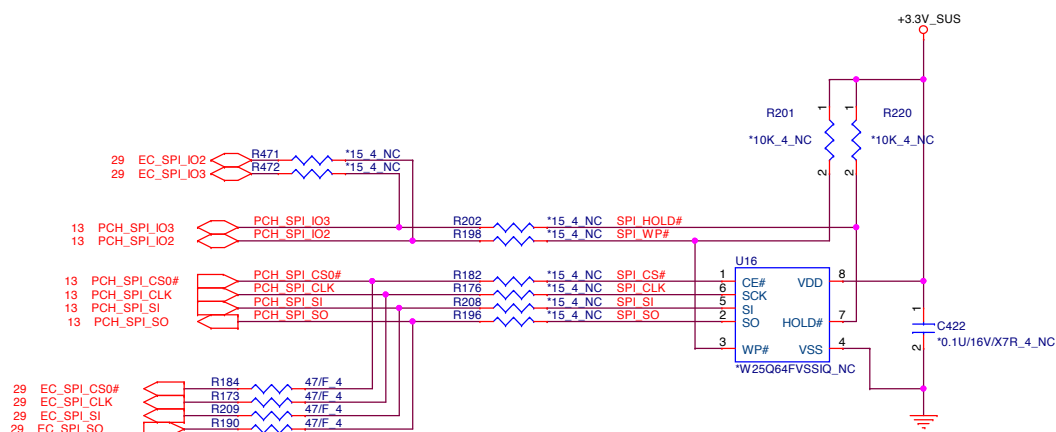


RTC BATTERY

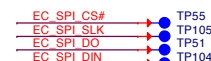
(non Rechargeable BATT)



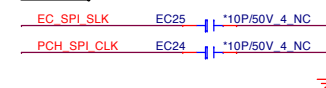
For PCH 32Mbit (4M Byte)



TP for ICT flash BIOS process



EMI



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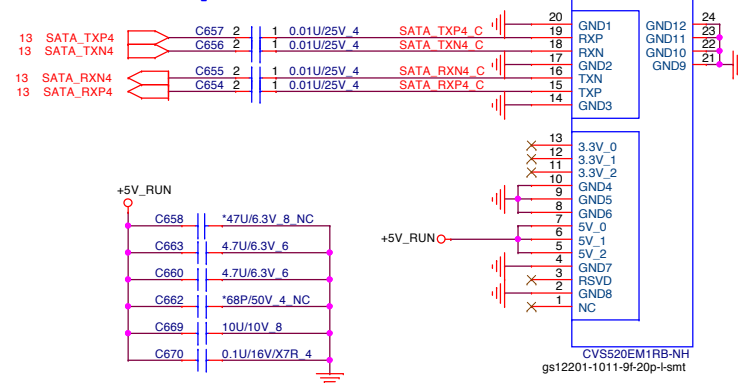


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FLASH / RTC
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SATA HDD Connector

DG: Place TX cap close to connector



NGFF M.2 SSD B-KEY

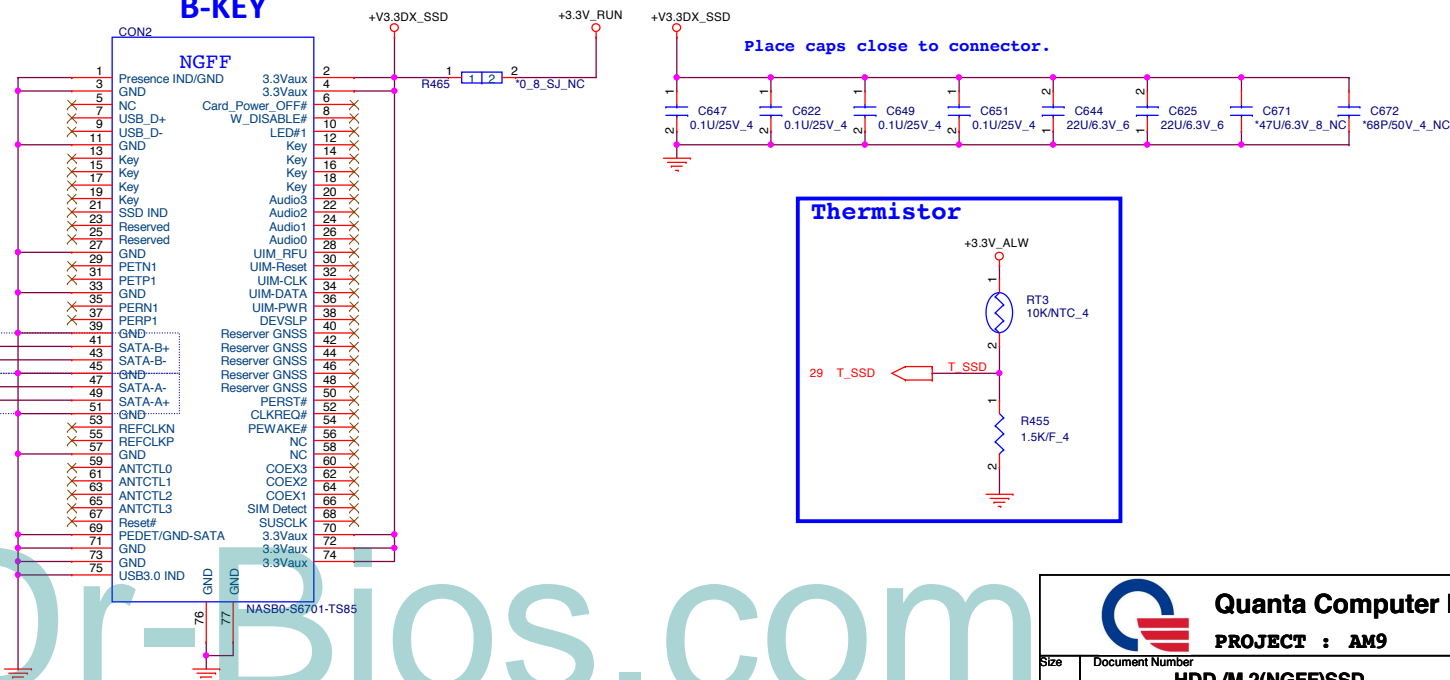
Max = 6000 mils
Min = 1000 mils

DG: Place TX cap close to connector

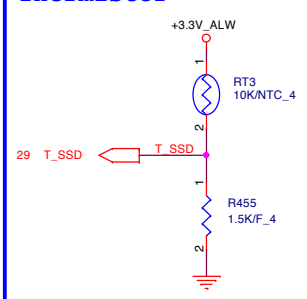
TX- based on SSD



RX- based on SSD



Thermistor



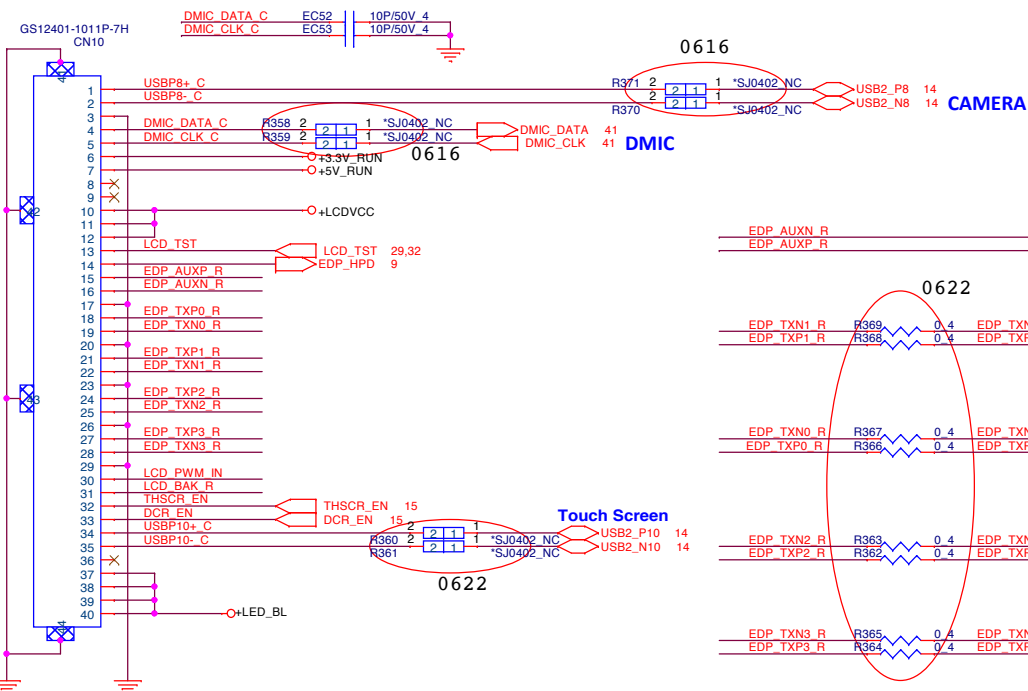
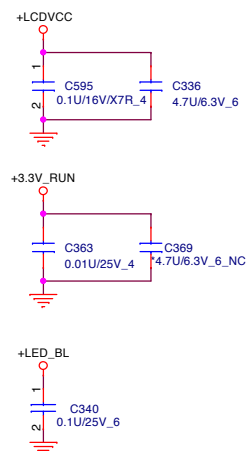
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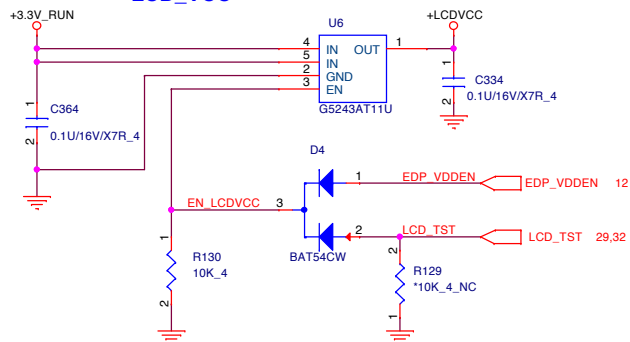
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Size	Document Number	Rev
	HDD/M.2(NGFF)SSD	A0
Date:	Monday, June 22, 2015	Sheet 31 of 51

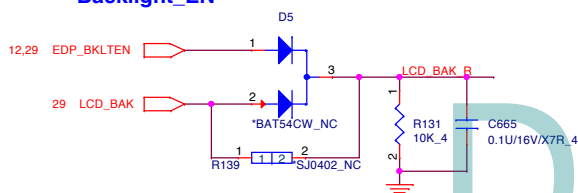
Close to CN18



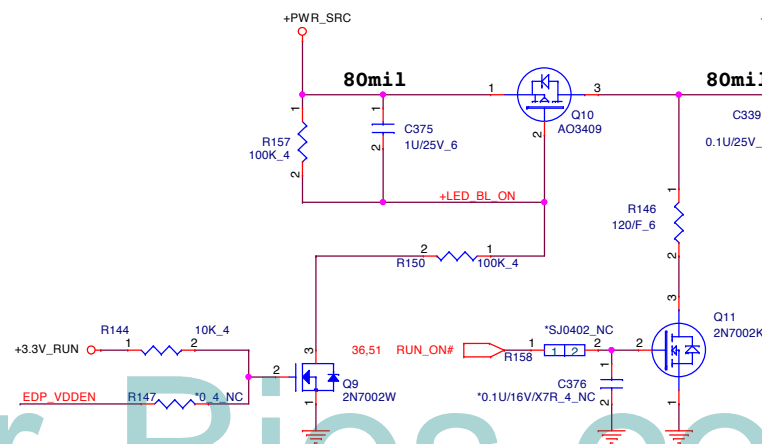
LCD_VCC



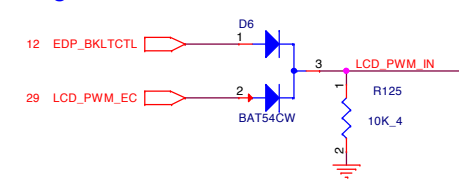
Backlight_EN



Backlight Power



Brightness Control

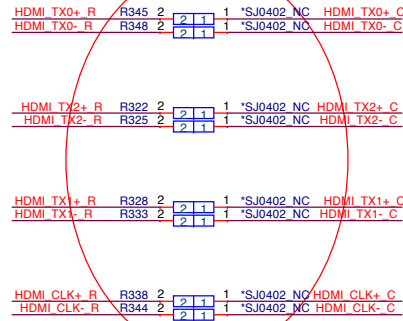


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PROJECT : AM9

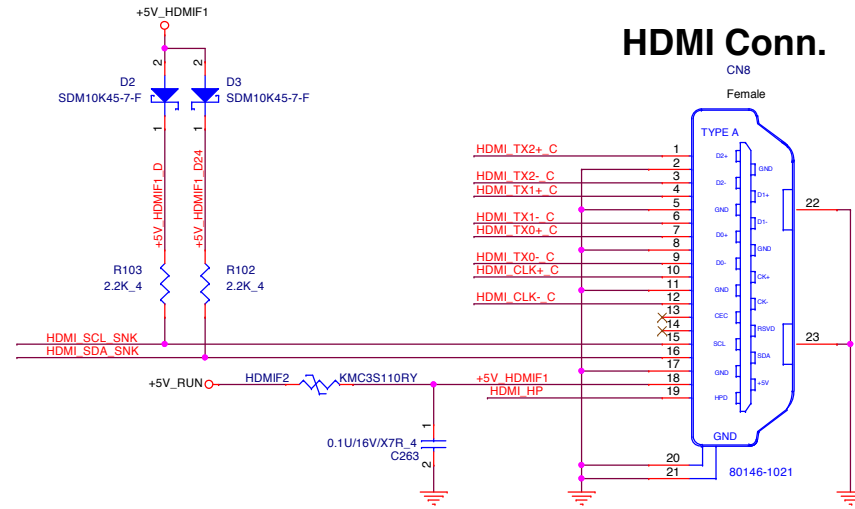
Size	Document Number	Rev
	EDP/CCD	A0
Date: Monday, June 22, 2015	Sheet 32 of 51	

Chock change to AM6 USB3 compoent

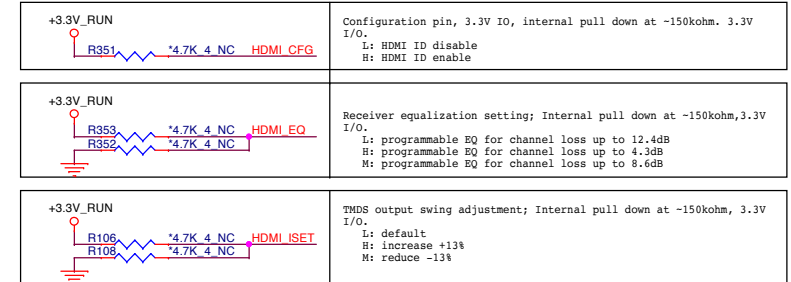
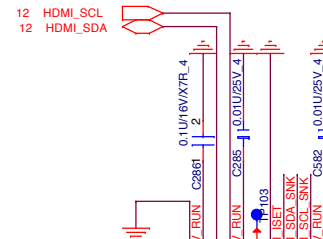
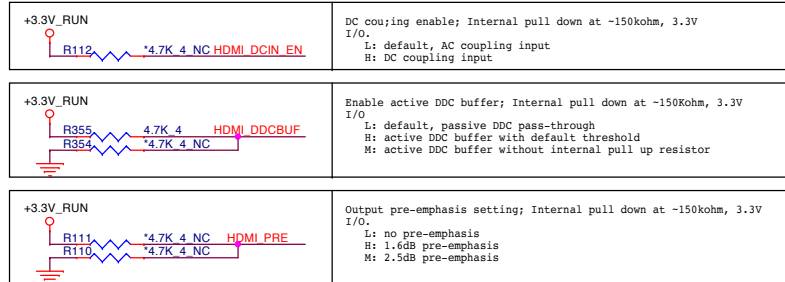
close to HDMI CONN for EMI



0616

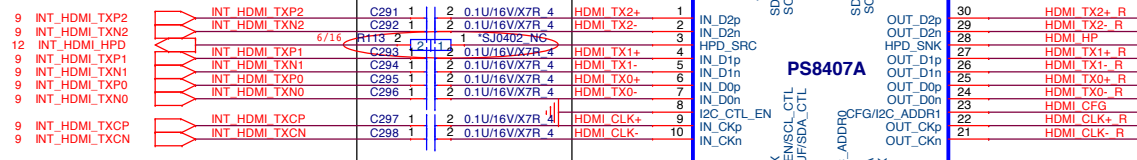


HDMI HPD :
1. PS8407A internal PD 150kohm
2. PS8407A has implement level shifter



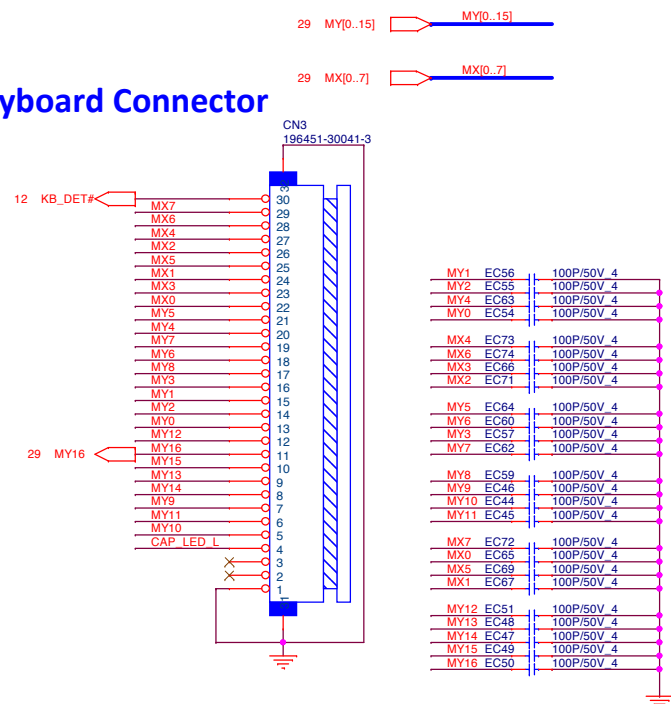
INT HDMI

Near PS8407A



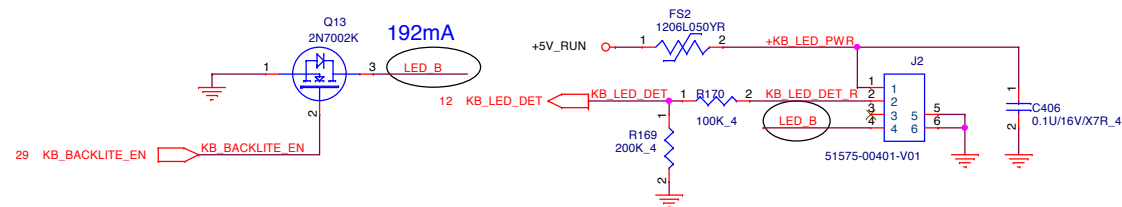
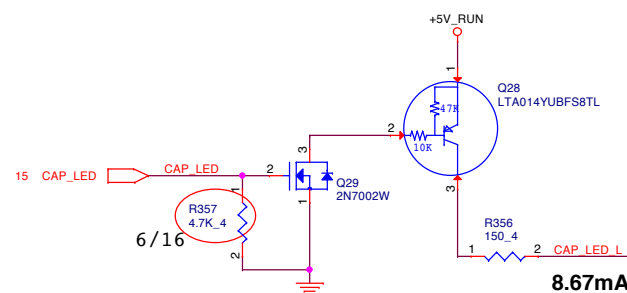
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Keyboard Connector

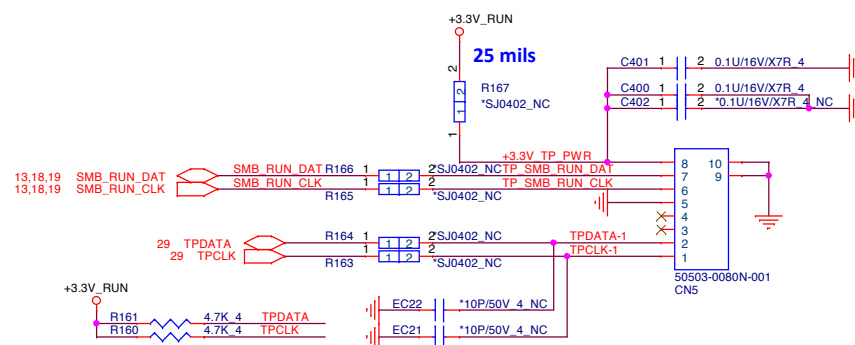


Key board illumination

+KB_LED power trace width >10 mil


 $V_{i(on_max)} = -1.4V$
 $V_{i(off_min)} = -0.3$


Touch Pad Connector



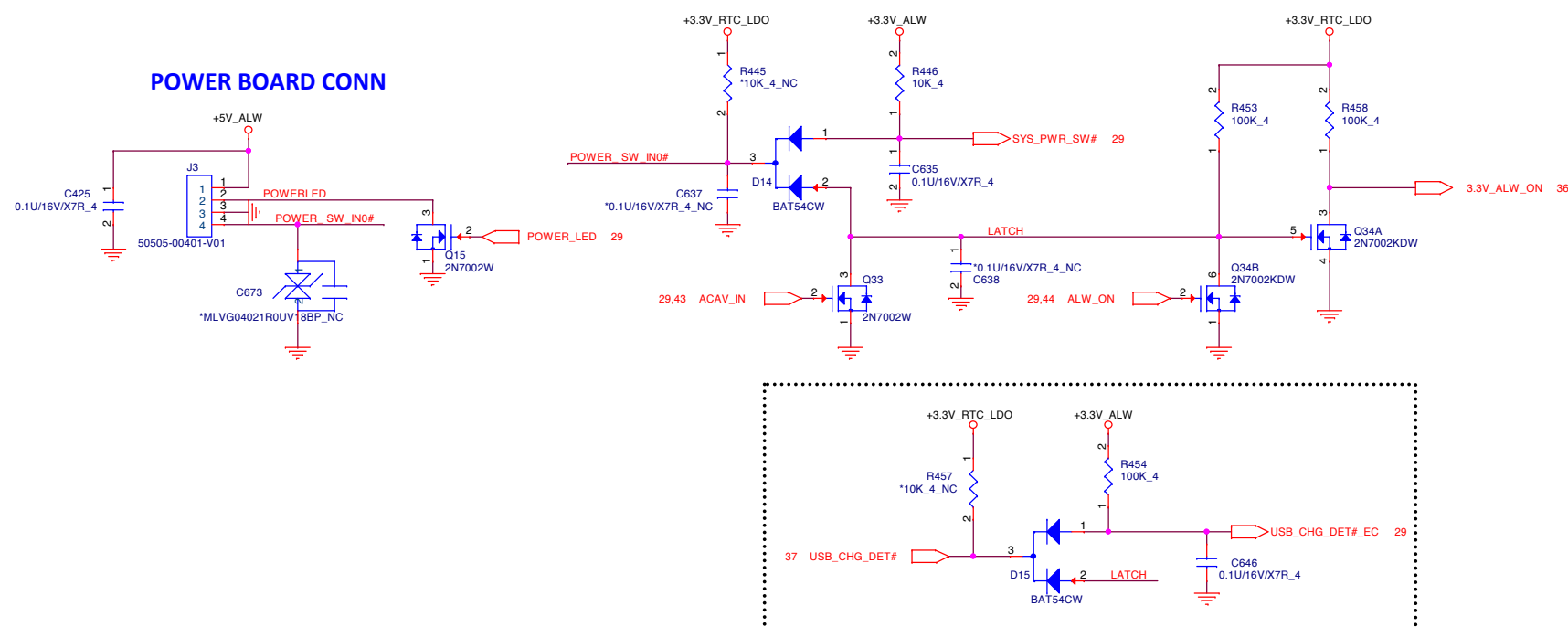
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3V ALW_ON POWER LOGIC



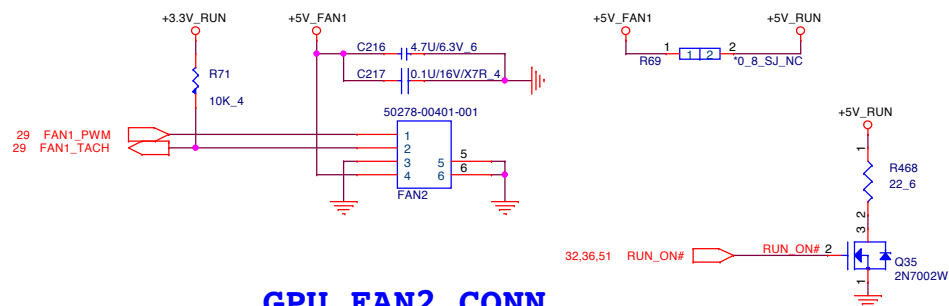
Dr-Bios.com



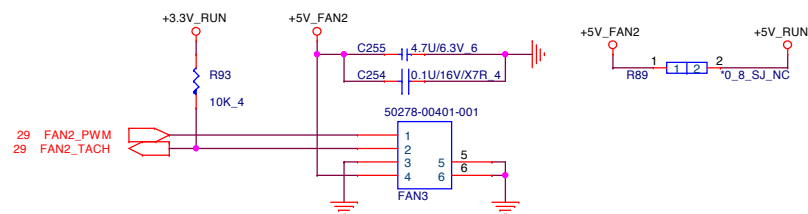
Quanta Computer Inc.
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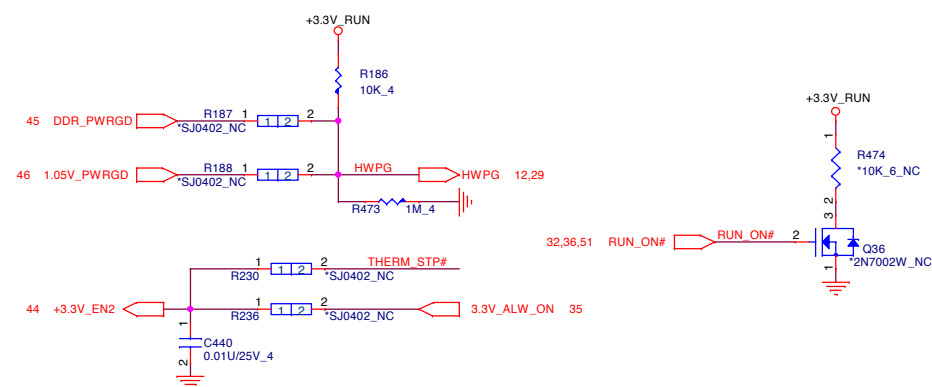
CPU FAN1 CONN



GPU FAN2 CONN



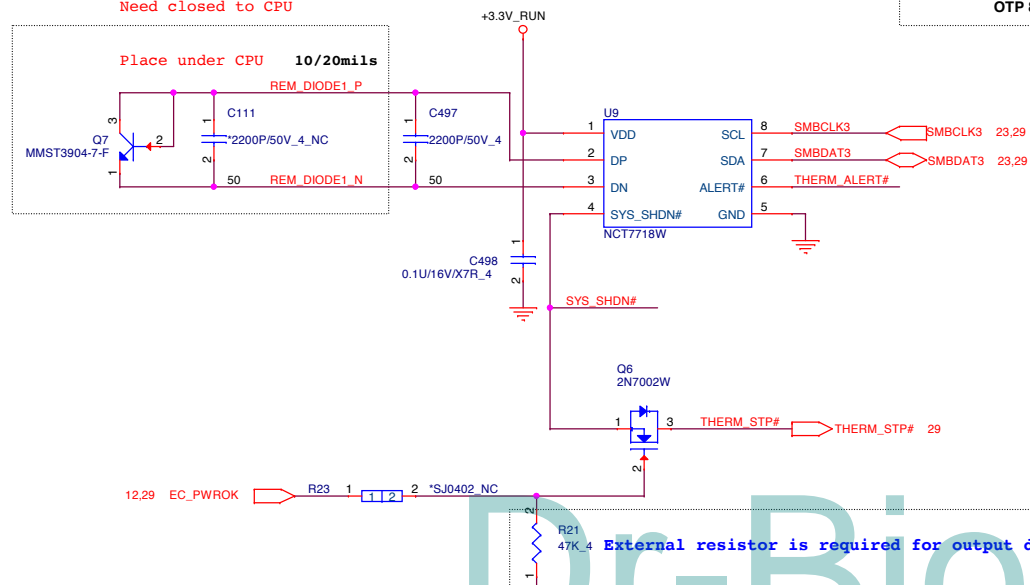
HWPG



THERMAL IC

Need closed to CPU

Place under CPU 10/20mils



OTP 85 degree C



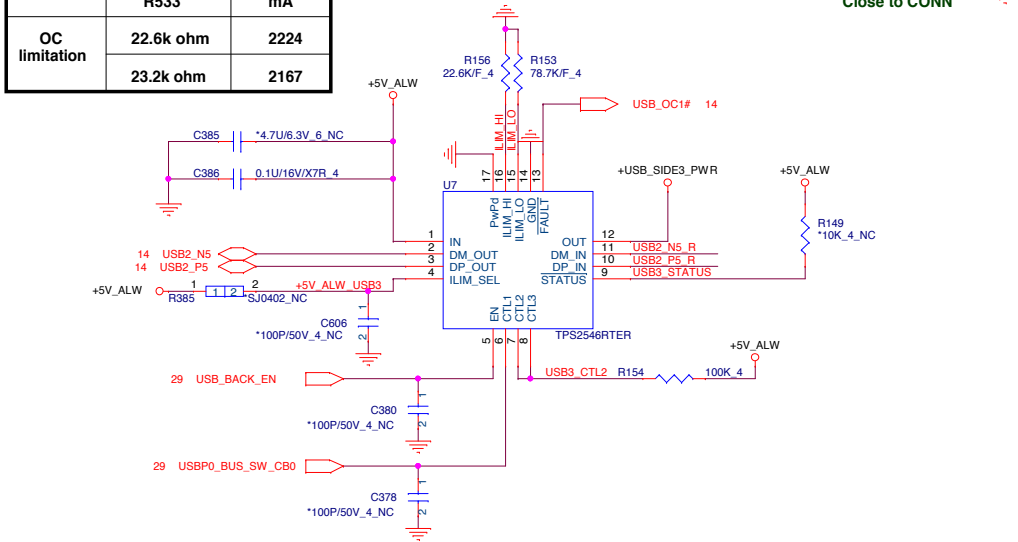
OTP 85 degree : R526= 18.7K, R527= 2K

SYS_SHD#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77 'C	87 'C	97 'C	107 'C	117 'C
7.5K	79 'C	89 'C	99 'C	109 'C	119 'C
10.5K	81 'C	91 'C	101 'C	111 'C	121 'C
14K	83 'C	93 'C	103 'C	113 'C	123 'C
18.7K	85 'C	95 'C	105 'C	115 'C	125 'C

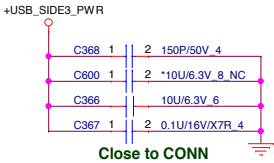


USBP0_BUS_SW_CB0	Mode	Operating at
High	CDP	S0, 1.5 A
Low	DCP, Auto-detect	S3/S4/S5, 2.1/1.5 A

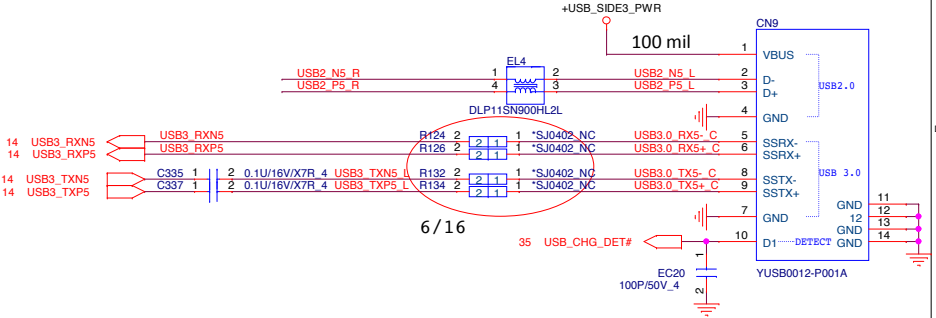
	R533	mA
OC limitation	22.6k ohm	2224
	23.2k ohm	2167



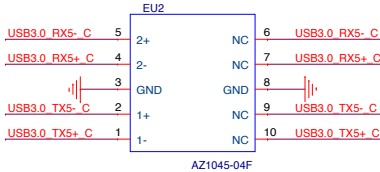
USB Power share

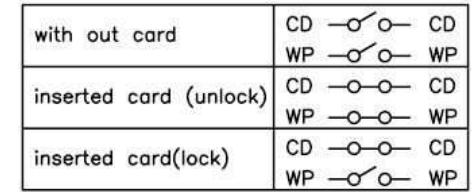


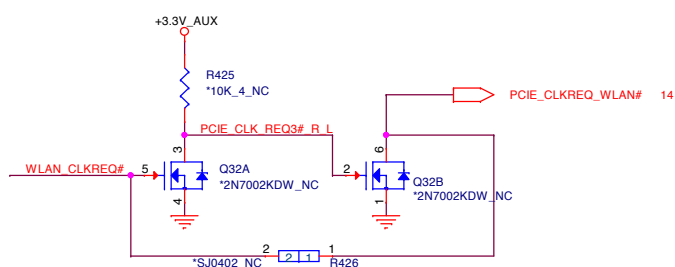
USB3.0/2.0 COMBO X 1

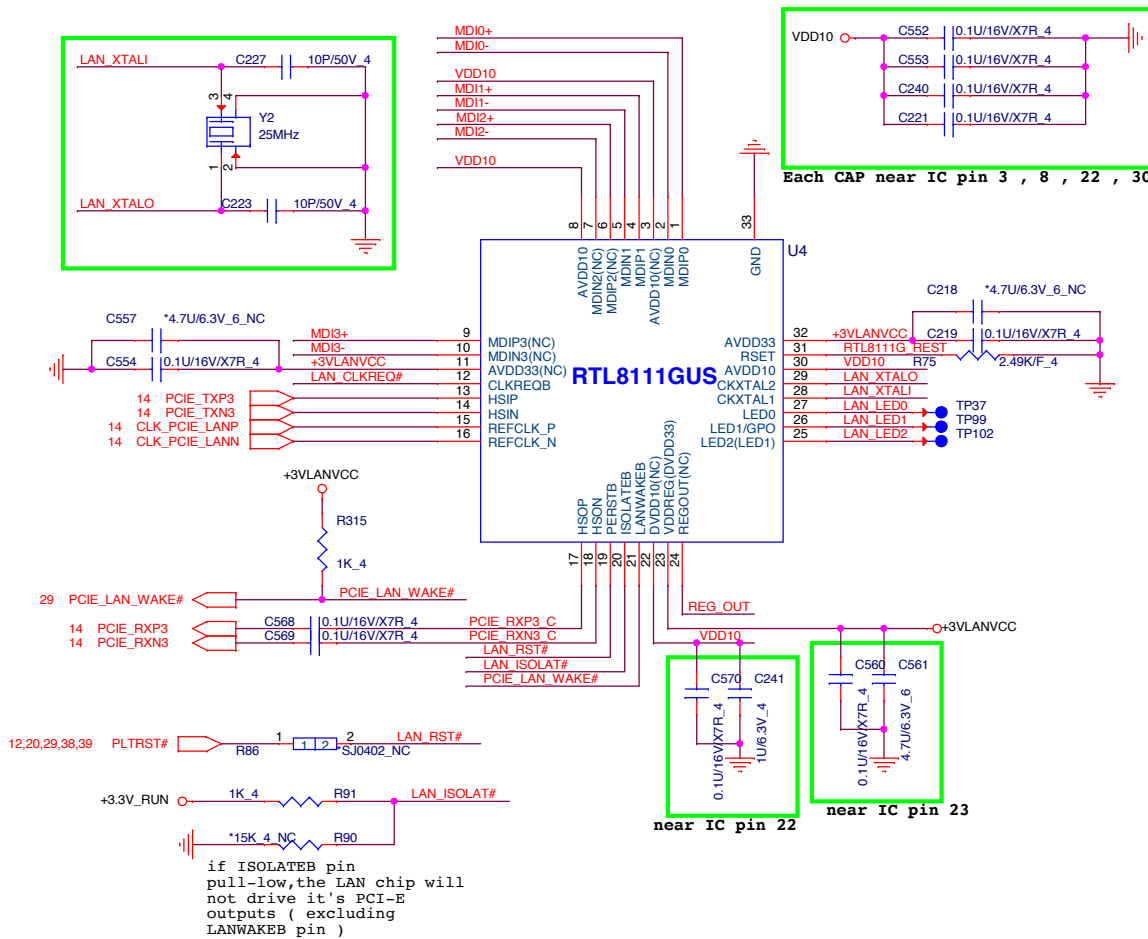


Need closed to CN9

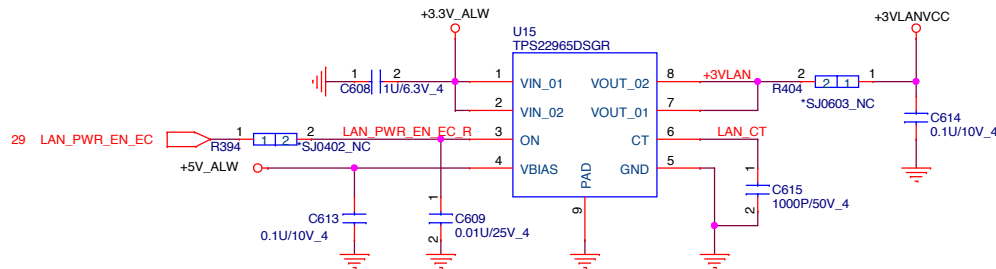




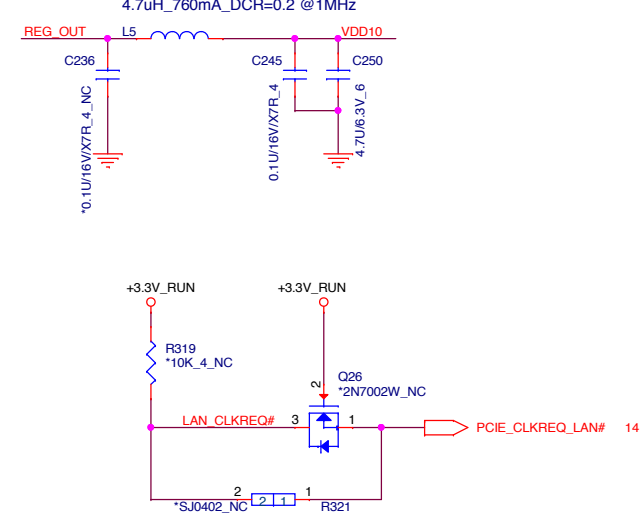




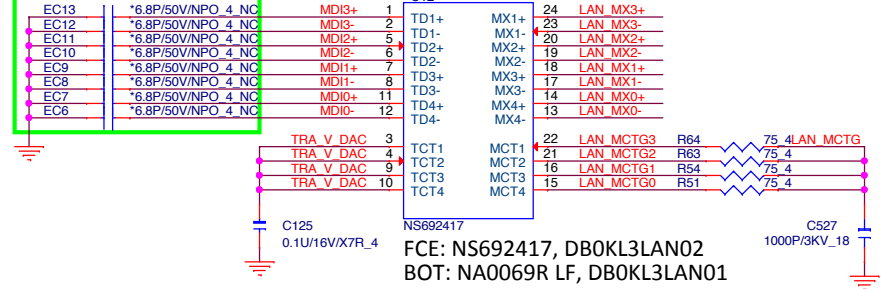
LAN POWER



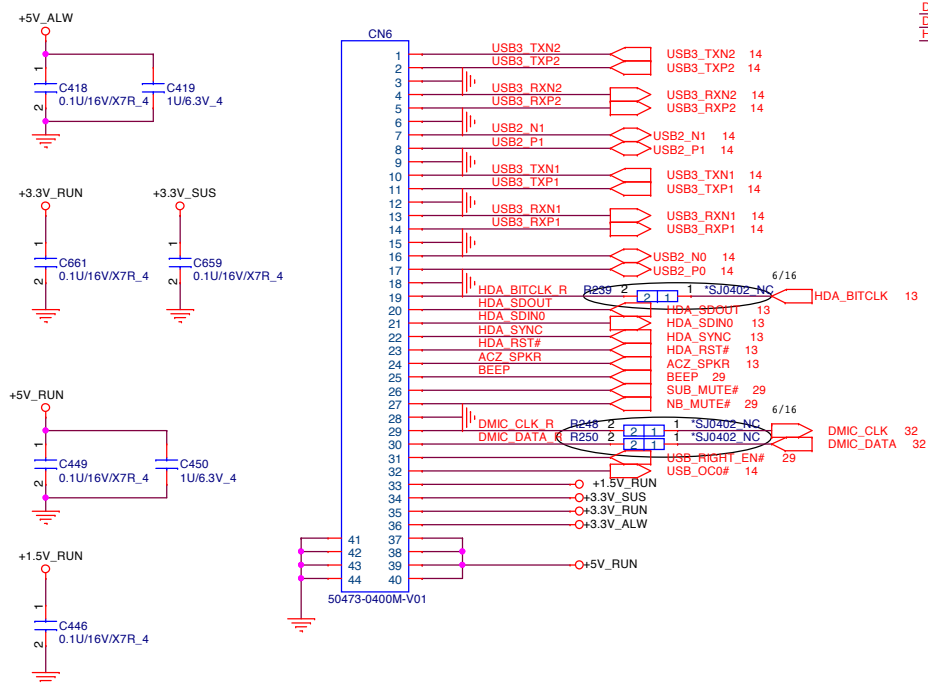
SW mode



EMI

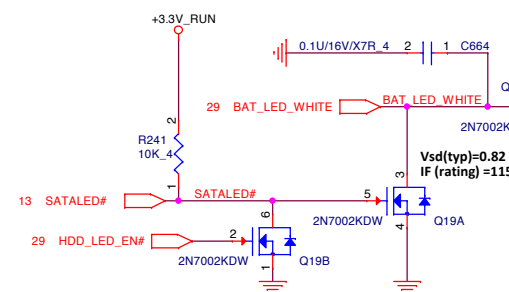


MB to IO Connector

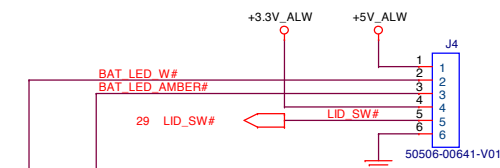


DMIC_DATA_R	EC31	*10P/50V_4 NC
DMIC_CLK_R	EC30	*10P/50V_4 NC
HDA_BITCLK_R	EC26	*10P/50V_4 NC

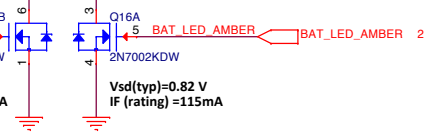
Battery LED



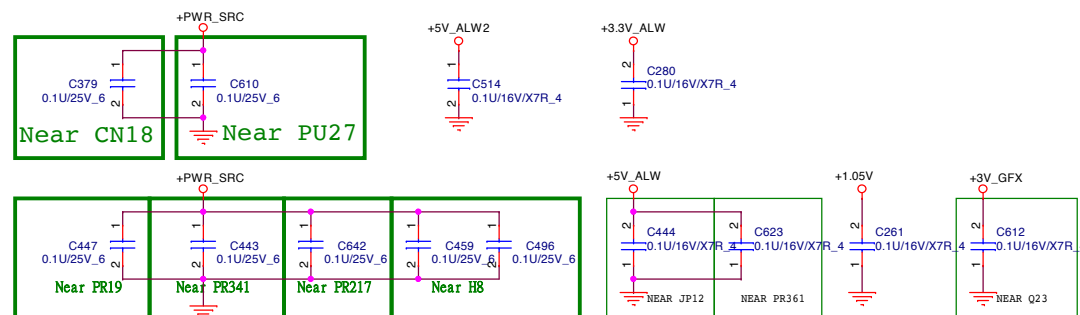
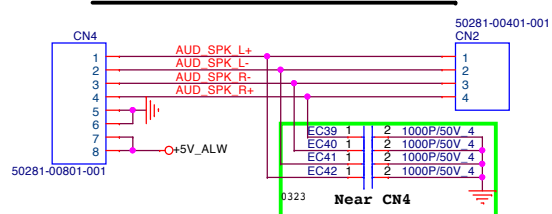
LED Board CONN



Battrey charger LED



POWER & AUDIO SPEAKER CON

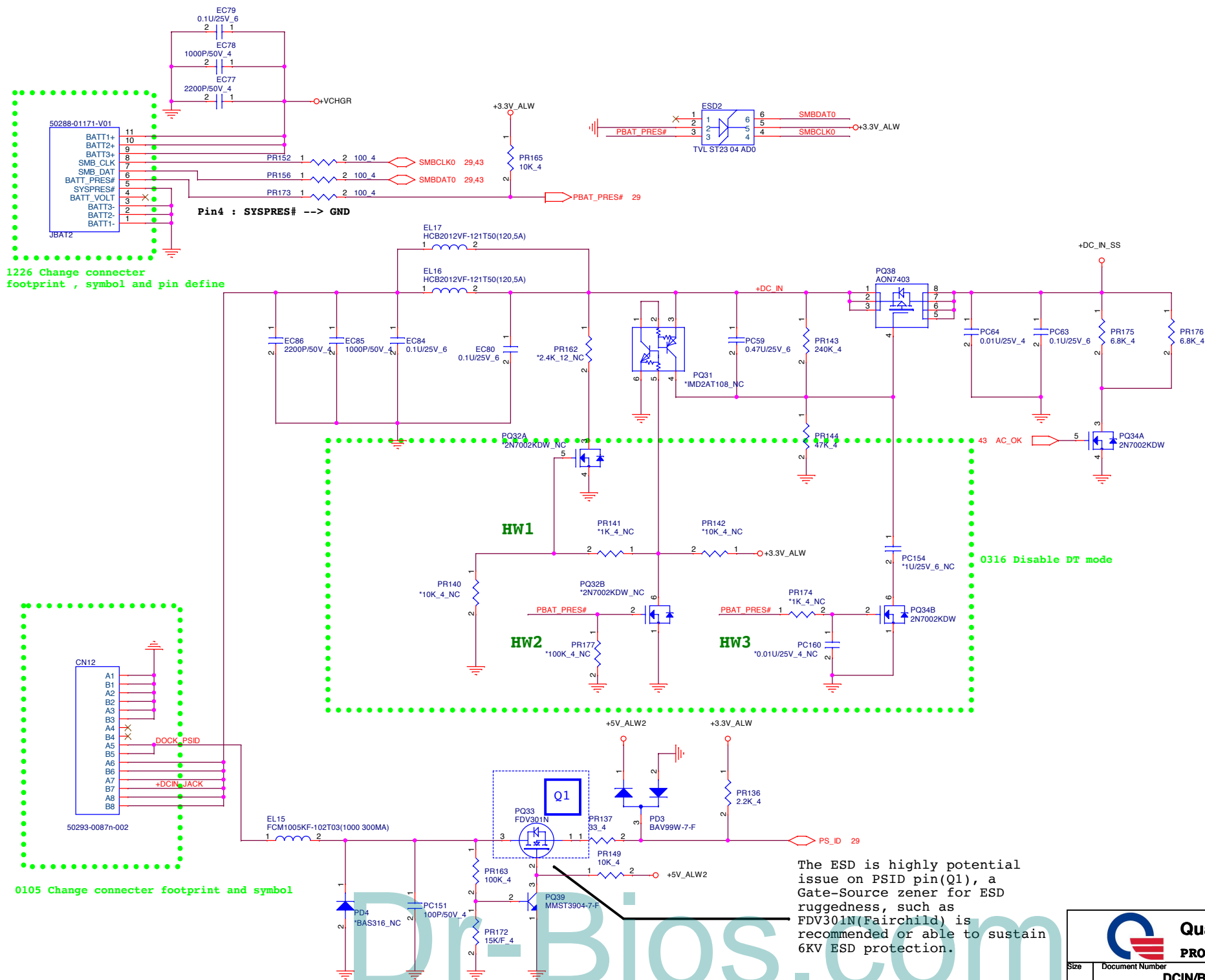


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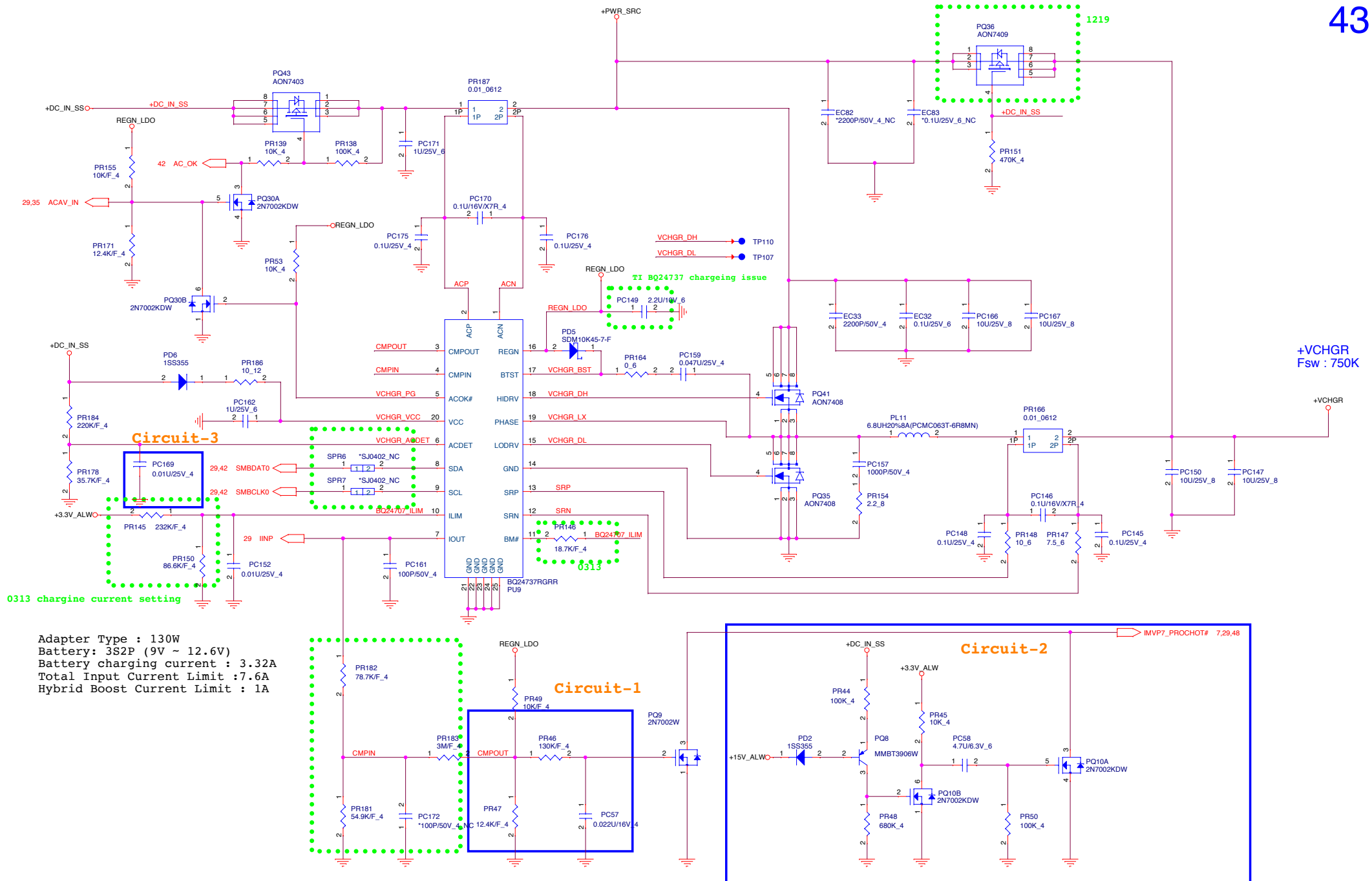
Size	Document Number	Rev
	IO BD CONN/LED	A0
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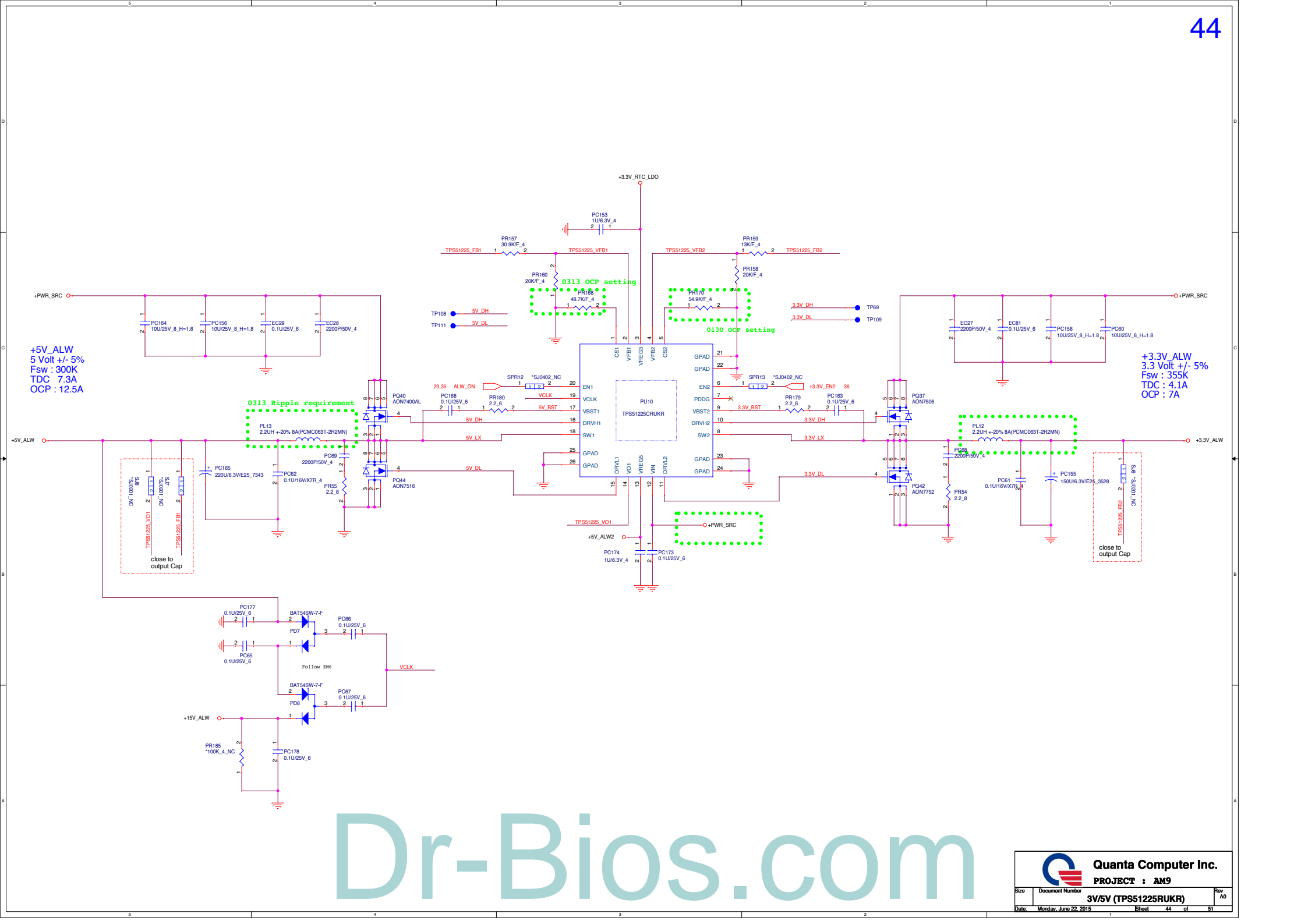
PROJECT : AM9

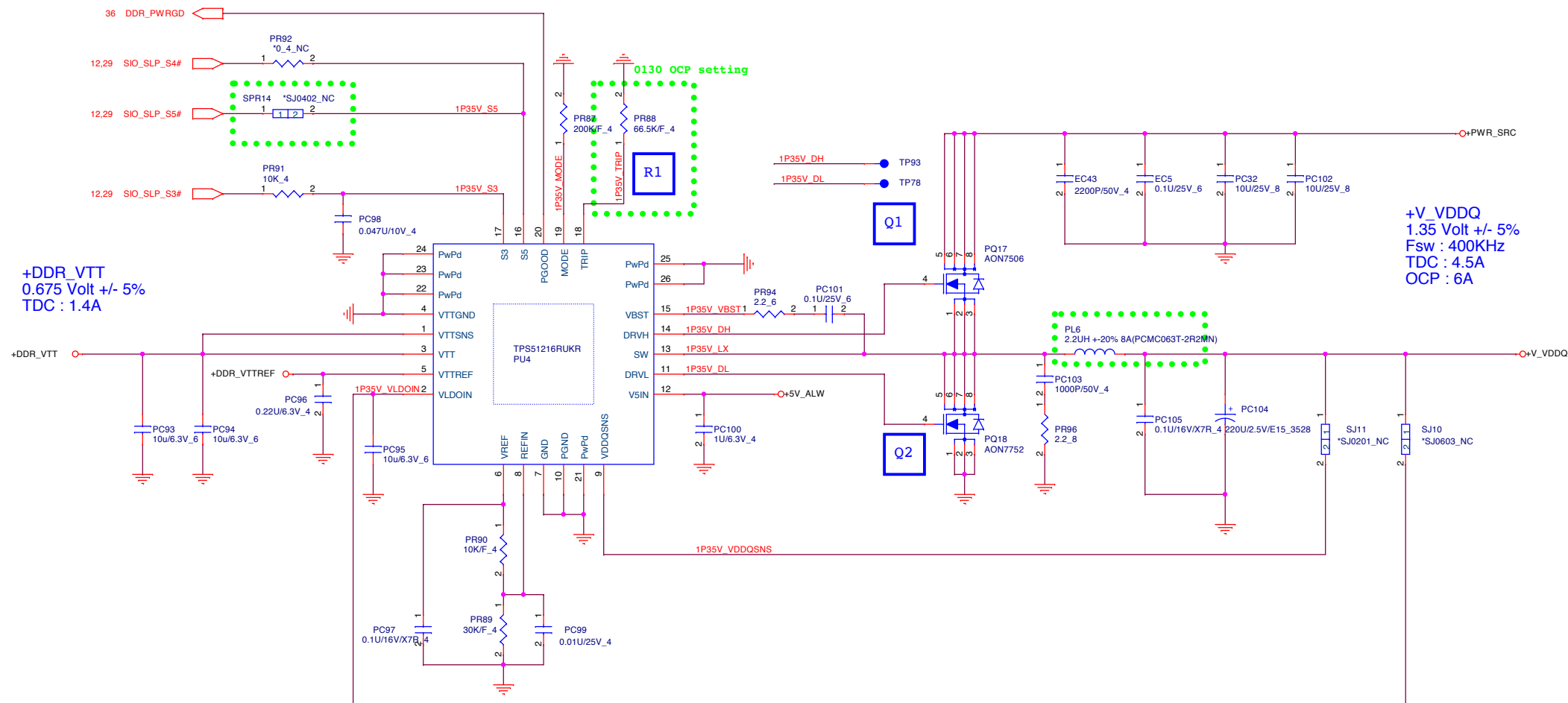
Size	Document Number	Rev
	DCIN/BATT	A0
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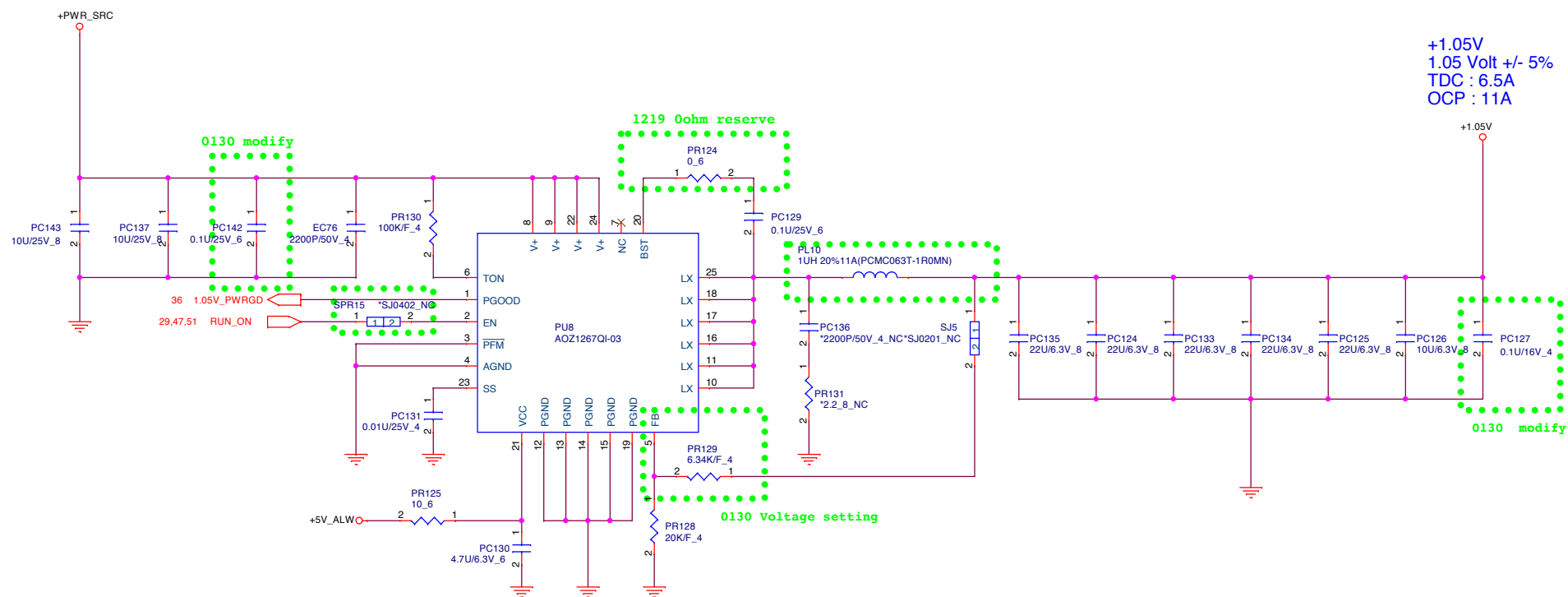


```
Adapter Type : 130W
Battery: 3S2P (9V ~ 12.6V)
Battery charging current : 3.32A
Total Input Current Limit :7.6A
Hybrid Boost Current Limit : 1A
```

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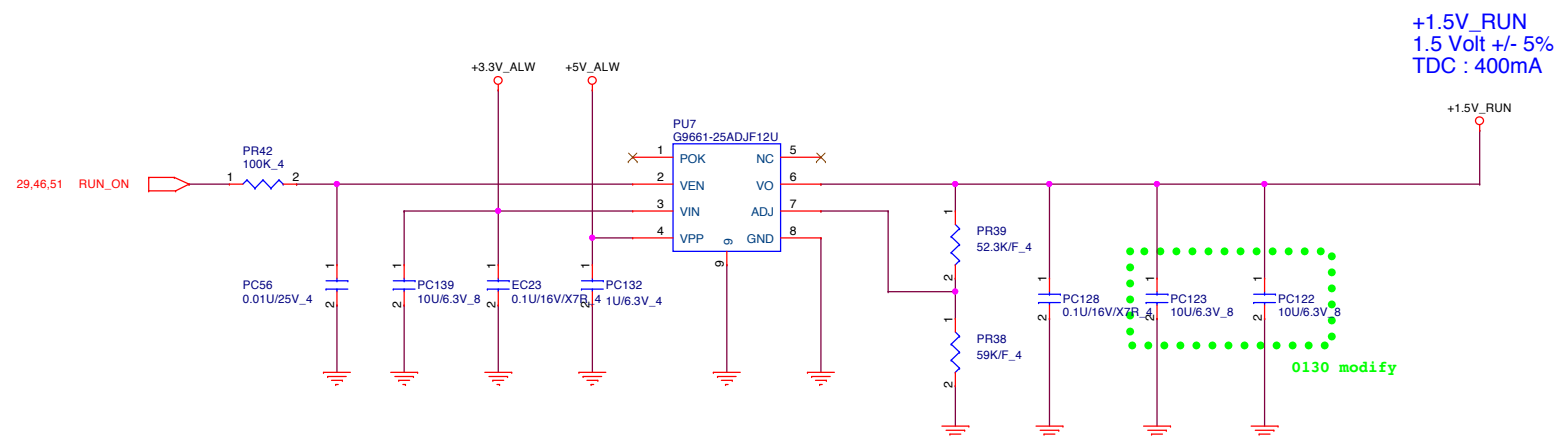
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Size	Document Number	Rev
	1.05V_RUN (RT8228AZQW)	A0
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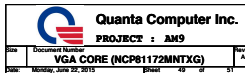
Dr-Bios.com

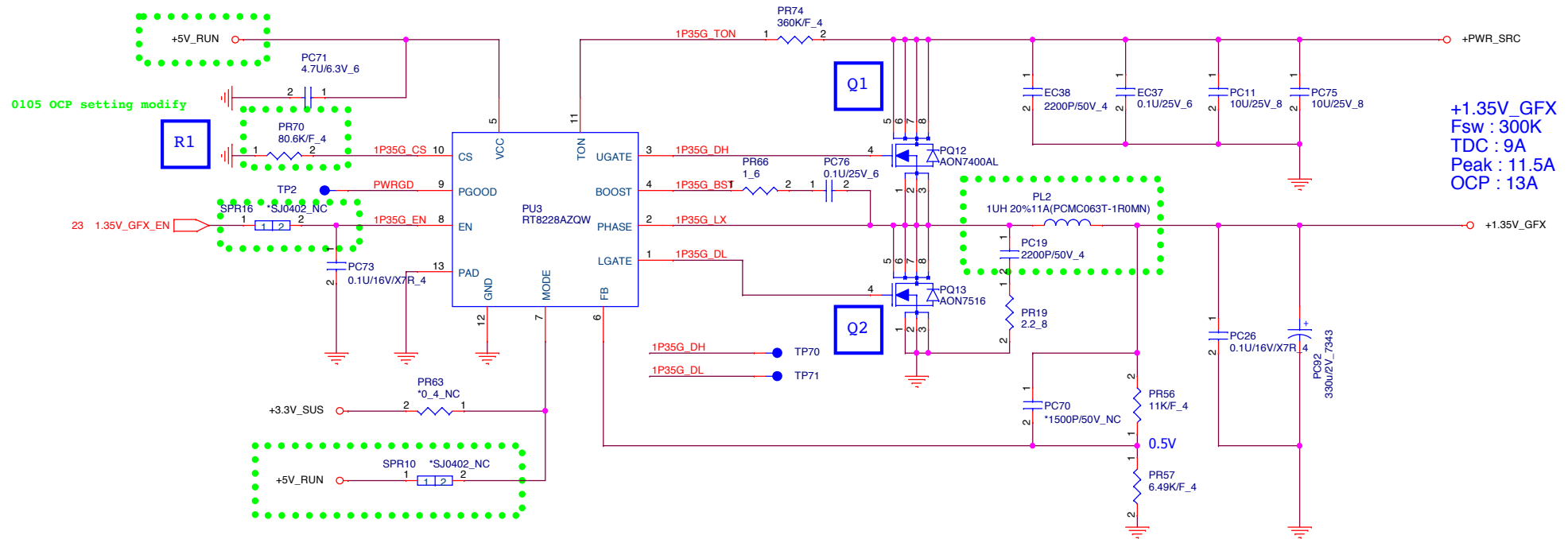


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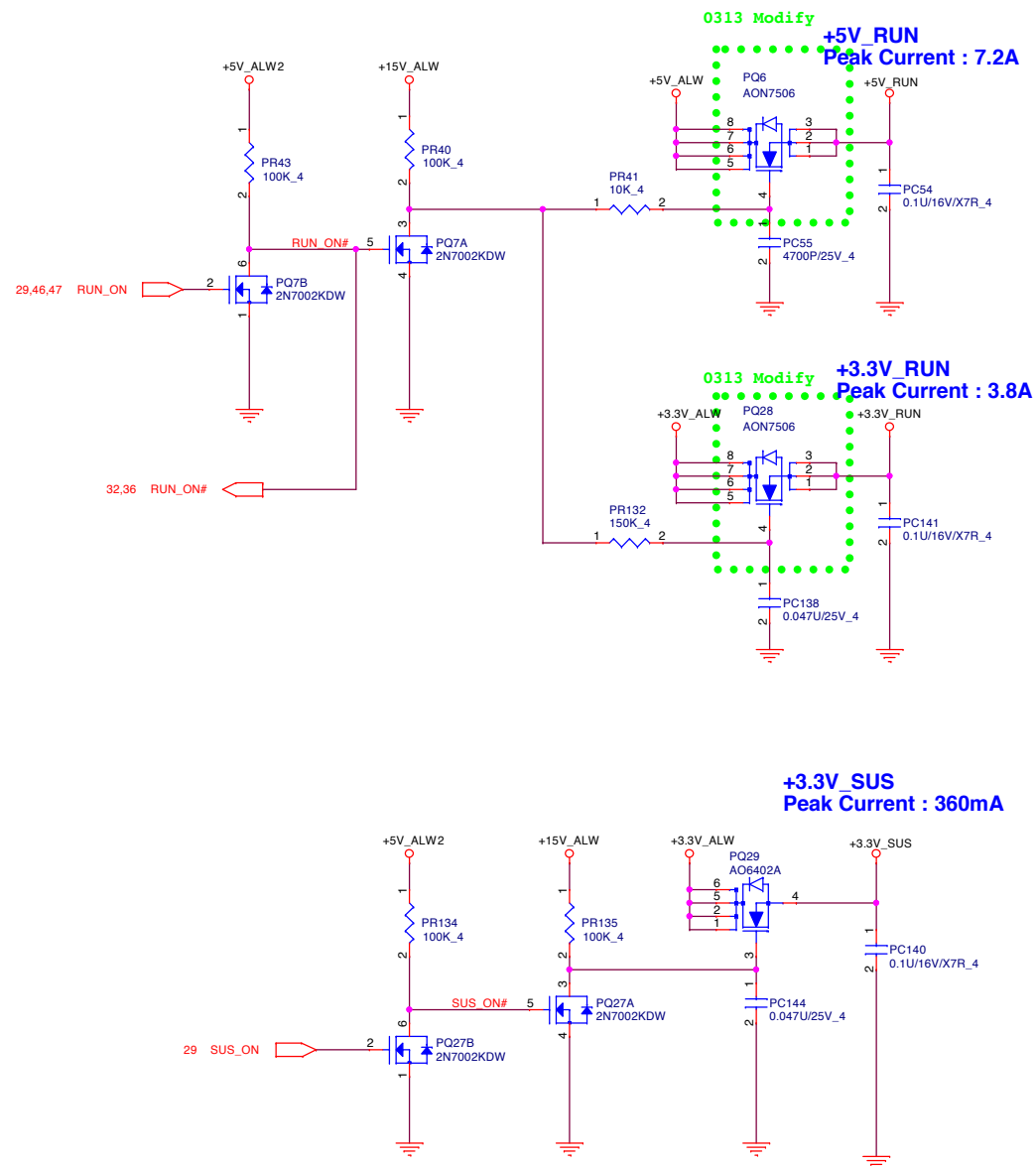
Size	Document Number	Rev
	1.5V (G9661)	A0
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Title		
AM9		
Size	Document Number	Rev
B	1.35V_GPU(RT8228AZ)	A0
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SUS_RUN Power Switch

Size	Document Number	Rev
		A0

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