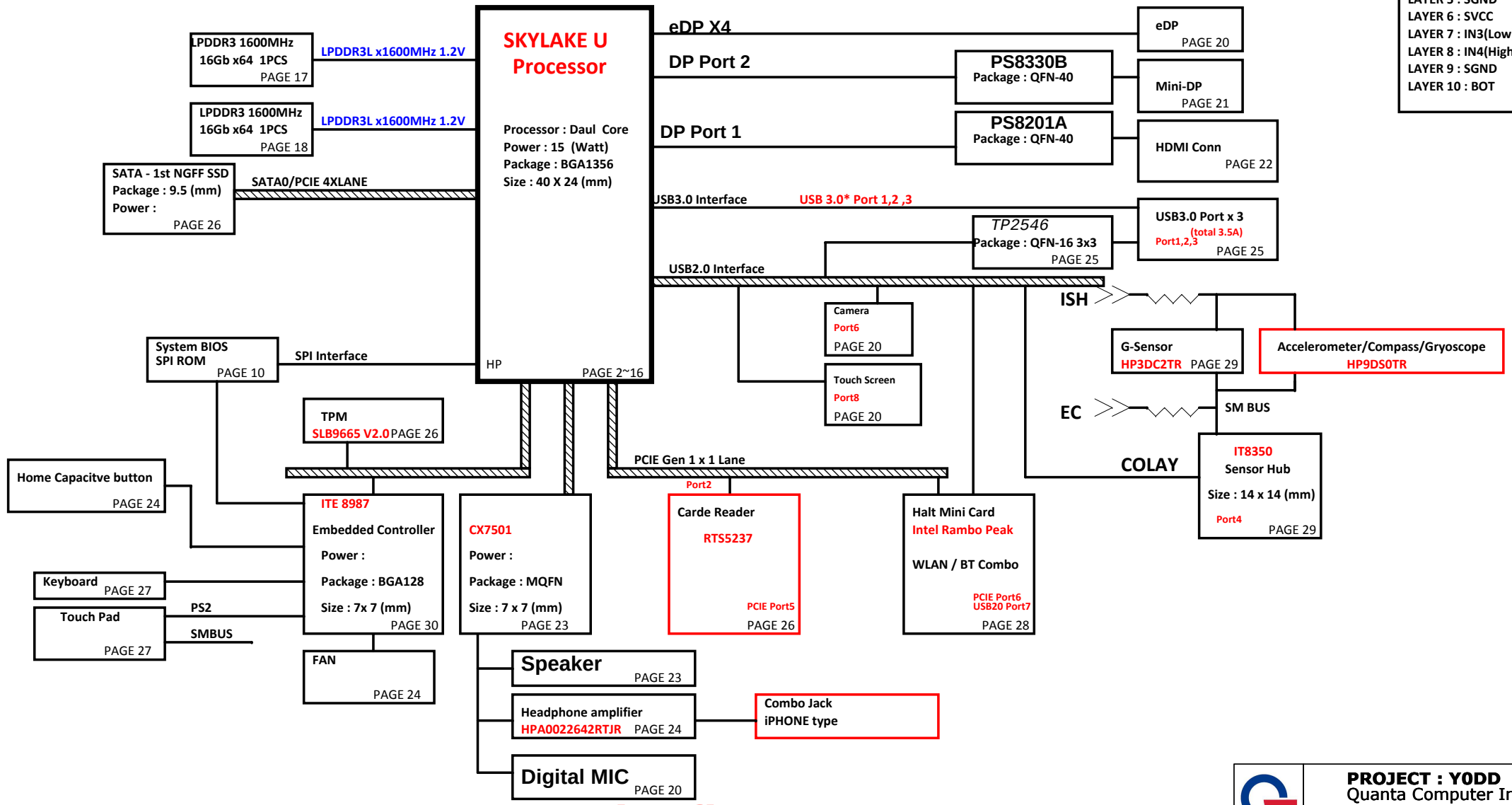
Pike Intel SKYLAKE ULT Platform Block Diagram

PCB 10L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(High)
LAYER 5 : SGND
LAYER 6 : SVCC
LAYER 7 : IN3(Low)
LAYER 8 : IN4(High)
LAYER 9 : SGND
LAYER 10 : BOT



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PROJECT : Y0DD
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Size	Document Number	Rev
Custom	Block Diagram	1A

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+3V <4,10,11,12,13,14,15,16,20,21,22,23,25,26,27,29,30,31,37,38>
+1.0V <4,6,16,30,36>
+VCCSTPLL <4,5,6,9,36,38>
+VCCIO <6,16,36>

HDMI

INT_DP_SCL R245 2.2K_2
INT_DP_SDA R246 2.2K_2 +3V

DDPB_CTRLDATA/ GPP_E19
Display Port B Detected
This signal has a weak internal pull-down.
0 = Port B is not detected.
1 = Port B is detected.

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.

DDPD_CTRLDATA R51 10K_2

U11A SKL_ULT ? **Need apply PN**

<22> IN_D2# E55
<22> IN_D2 F55
<22> IN_D1# E58
<22> IN_D1 F58
<22> IN_D0# F53
<22> IN_D0 G53
<22> IN_CLK# F56
<22> IN_CLK C56
DDI1_TXN[0]
DDI1_TXP[0]
DDI1_TXN[1]
DDI1_TXP[1]
DDI1_TXN[2]
DDI1_TXP[2]
DDI1_TXN[3]
DDI1_TXP[3]

<21> INT_DP_TXN0 C50
<21> INT_DP_TXP0 D50
<21> INT_DP_TXN1 C52
<21> INT_DP_TXP1 D52
<21> INT_DP_TXN2 A50
<21> INT_DP_TXP2 B50
<21> INT_DP_TXN3 D51
<21> INT_DP_TXP3 C51
DDI2_TXN[0]
DDI2_TXP[0]
DDI2_TXN[1]
DDI2_TXP[1]
DDI2_TXN[2]
DDI2_TXP[2]
DDI2_TXN[3]
DDI2_TXP[3]

DDI
EDP
DISPLAY SIDEBANDS

<22> SDVO_CLK L13
<22> SDVO_DATA L12
GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA

<21> INT_DP_SCL N7
<21> INT_DP_SDA N8
GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA

DDPD_CTRLDATA N11
N12
GPP_E22/DDPD_CTRLCLK
GPP_E23/DDPD_CTRLDATA

+VCCIO R47 24.9/F_2 EDP_RCOMP E52
EDP_RCOMP

*SKL_ULT
REV = 1
1 OF 20

EDP_TXN[0] C47 INT_EDP_TXN0 → INT_EDP_TXN0 <20>
EDP_TXP[0] C46 INT_EDP_TXP0 → INT_EDP_TXP0 <20>
EDP_TXN[1] D46 INT_EDP_TXN1 → INT_EDP_TXN1 <20>
EDP_TXP[1] C45 INT_EDP_TXP1 → INT_EDP_TXP1 <20>
EDP_TXN[2] A45 INT_EDP_TXN2 → INT_EDP_TXN2 <20>
EDP_TXP[2] B45 INT_EDP_TXP2 → INT_EDP_TXP2 <20>
EDP_TXN[3] A47 INT_EDP_TXN3 → INT_EDP_TXN3 <20>
EDP_TXP[3] B47 INT_EDP_TXP3 → INT_EDP_TXP3 <20>

EDP_AUXN E45 INT_EDP_AUXN → INT_EDP_AUXN <20>
EDP_AUXP F45 INT_EDP_AUXP → INT_EDP_AUXP <20>

EDP_DISP_UTIL B52 EDP_DISP_UTIL → TP46

DDI1_AUXN G50
DDI1_AUXP E50
DDI2_AUXN E48 → INT_DP_AUXN <21>
DDI2_AUXP F48 → INT_DP_AUXP <21>
DDI3_AUXN G46
DDI3_AUXP E46

GPP_E13/DDPB_HPD0 L9 HDMI_HPD_CON → HDMI_HPD_CON <22>
GPP_E14/DDPC_HPD1 L7 → INT_DP_HPD_Q <21>
GPP_E15/DDPD_HPD2 L6
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 ULT_EDP_HPD → ULT_EDP_HPD <20>

EDP_BKLTEN R12 PCH_LVDS_BLON → PCH_LVDS_BLON <20>
EDP_BKLTCTL R11 PCH_DPST_PWM → PCH_DPST_PWM <20>
EDP_VDDEN U13 PCH_DISP_ON → PCH_DISP_ON <20>

?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Mini-DP

Reserve EDP_HPD opposites circuit!

+3V
R188 10K_2
ULT_EDP_HPD
R187 100K_2

U11D SKL_ULT ? **Need apply PN**

<30,32,38> H_PROCHOT# R164 499/F_4 <30> EC_PECI
<30> PM_THRMTRIP#

CATERR# D63
EC_PECI A54
PROCHOT# C65
PM_THRMTRIP# C63
A65
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#

CPU MISC

<16> XDP_BPM0 C55
<16> XDP_BPM1 D55
B54
C56
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]

+VCCSTPLL
R165 *49.9/F_2 CATERR#

TP45 CPU_GP0 A6
TP47 CPU_GP1 A7
TP35 CPU_GP2 BA5
TP34 CPU_GP3 AY5
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

+1.0V
R61 49.9/F_2 PROC_POPIRCOMP AT16
R58 49.9/F_2 PCH_OPI_RCOMP AU16
R48 49.9/F_2 EDRAM_OPIO_RCOMP H66
R45 49.9/F_2 EOPIO_RCOMP H65
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

*SKL_ULT
REV = 1
4 OF 20

JTAG

PROC_TCK B61 XDP_TCK0 → XDP_TCK0 <16>
PROC_TDI D60 XDP_TDI_CPU → XDP_TDI_CPU <16>
PROC_TDO A61 XDP_TDO_CPU → XDP_TDO_CPU <16>
PROC_TMS C60 XDP_TMS_CPU → XDP_TMS_CPU <16>
PROC_TRST# B59 XDP_TRST#_CPU → XDP_TRST#_CPU <2,16>

PCH_JTAG_TCK B56 JTAG_TCK_PCH → JTAG_TCK_PCH <16>
PCH_JTAG_TDI D59 JTAG_TDI_PCH → JTAG_TDI_PCH <16>
PCH_JTAG_TDO A56 JTAG_TDO_PCH → JTAG_TDO_PCH <16>
PCH_JTAG_TMS C59 JTAG_TMS_PCH → JTAG_TMS_PCH <16>
PCH_TRST# C61 XDP_TRST#_CPU → XDP_TRST#_CPU <2,16>
JTAGX A59 JTAGX_PCH → JTAGX_PCH <16>

+1.0V
R29 51_2 JTAGX_PCH
R30 51_2 JTAG_TMS_PCH
R35 51_2 JTAG_TDI_PCH
R25 51_2 JTAG_TDO_PCH
R23 51_2 JTAG_TCK_PCH
Close to Chipset

Close to EC

+VCCSTPLL
PM_THRMTRIP# R213 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V
XDP_TMS_CPU R36 *51_2
XDP_TDI_CPU R31 *51_2
XDP_TDO_CPU R28 *51_2

+1.0V
H_PROCHOT# R142 1K_2
XDP_TCK0 R177 51_2
XDP_TRST#_CPU R27 51_2

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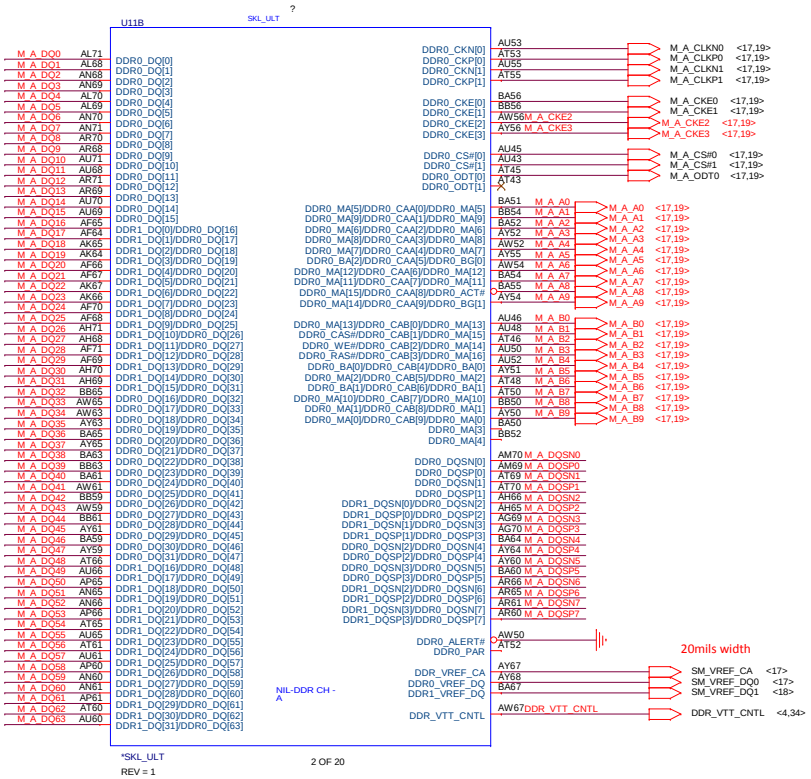
SkyLake ULT Processor (DDR3L)

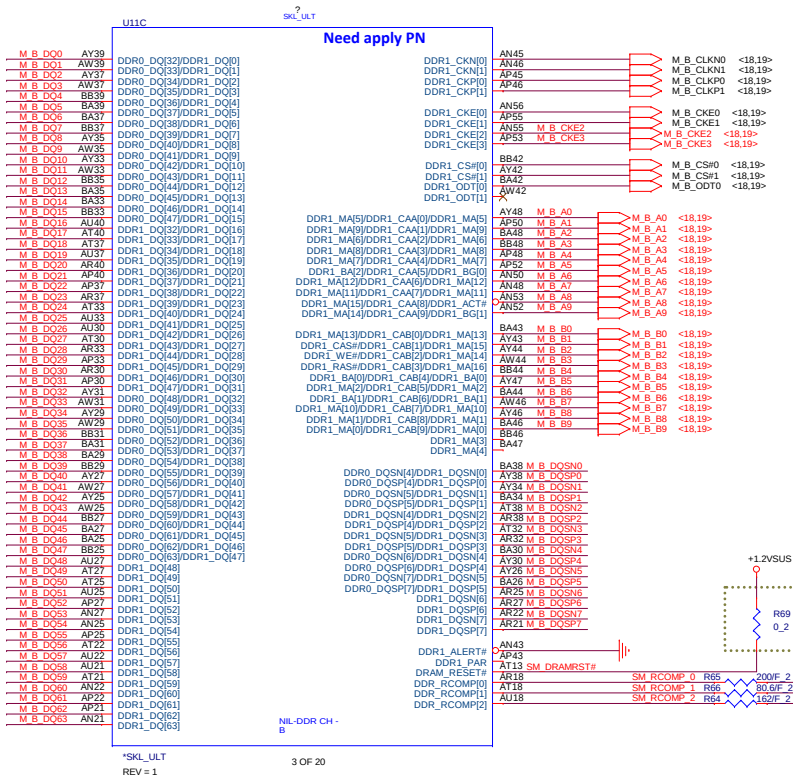
<17> M_A_DQSN[7:0]
<17> M_A_DQSP[7:0]
<18> M_B_DQSN[7:0]
<18> M_B_DQSP[7:0]
<17> M_A_DQ[63:0]
<18> M_B_DQ[63:0]

+1.2VSUS <6,17,18,34,36>

Need apply PN



Need apply PN



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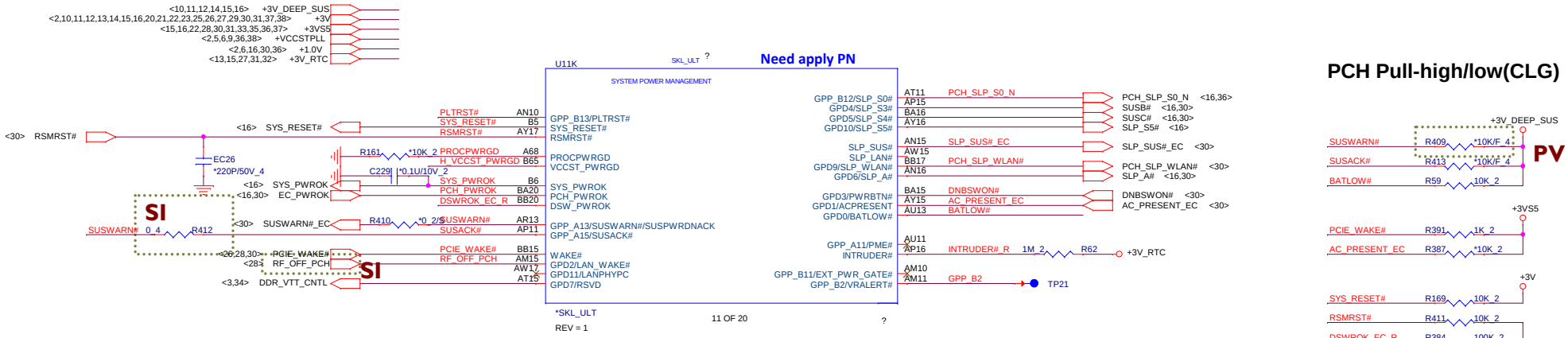
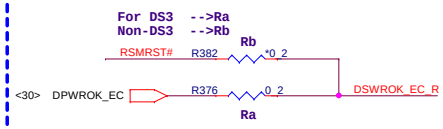
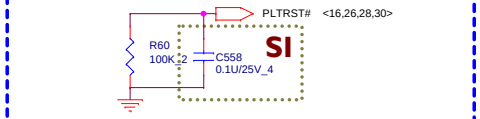


For DS3 Sequence

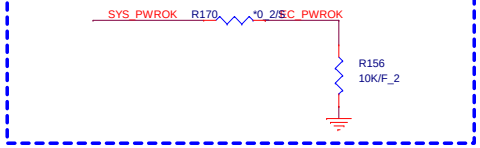


PLTRST#(CLG)

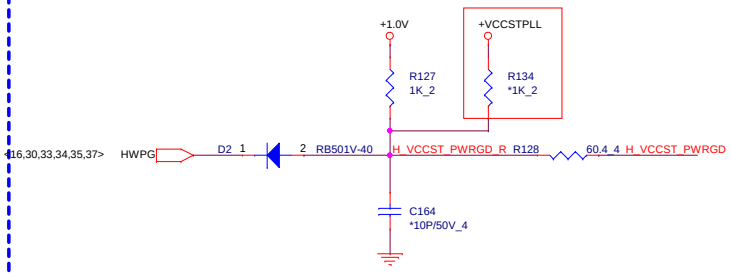
Check Q2010 Rise/Fall time less than 100ns



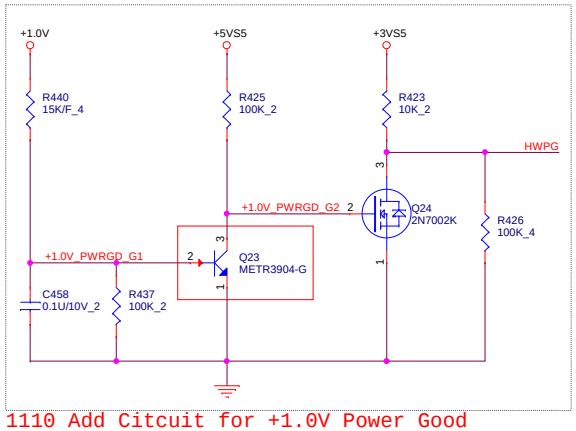
System PWR_OK(CLG)



1218 Reserve
+VCCSTPLL and R523



R10479 close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



1110 Add Citcuit for +1.0V Power Good

1118 Change Change Q7062 P/N from BA051440000 to BA039040020, Del D7002,D7003, R10526, R10527

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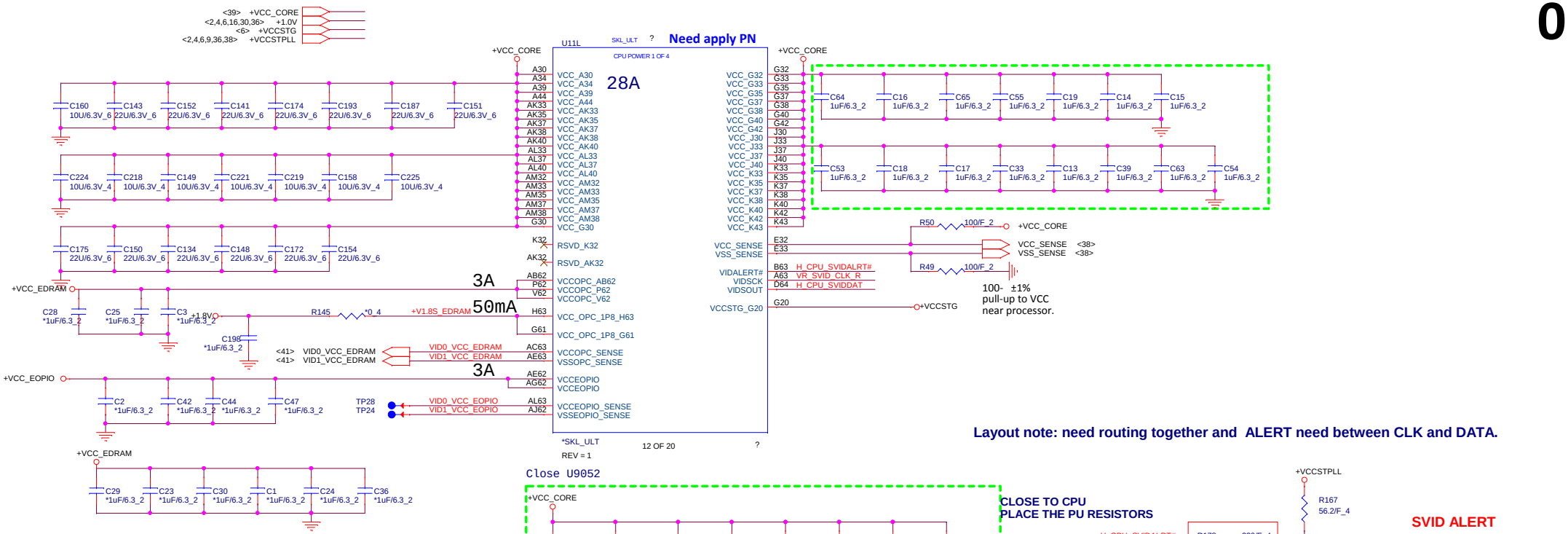
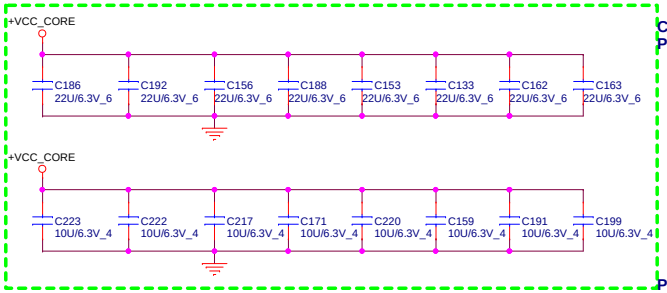
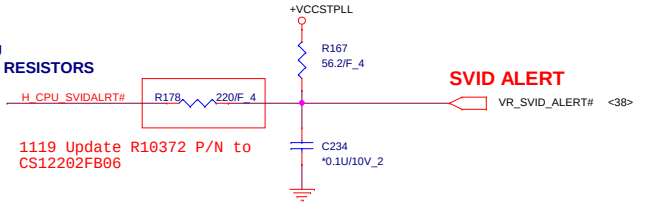


Close U9052



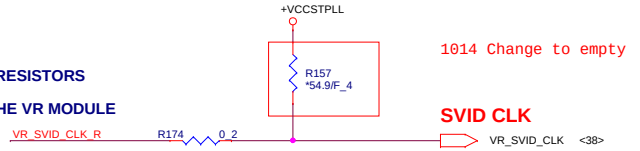
Layout note: need routing together and ALERT need between CLK and DATA.

CLOSE TO CPU
PLACE THE PU RESISTORS

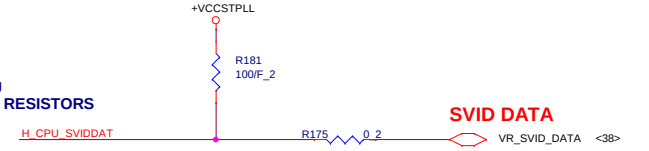


1119 Update R10372 P/N to CS12202FB06

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE



CLOSE TO CPU
PLACE THE PU RESISTORS



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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+VCCSTPLL <2,4,5,9,36,38>
+VCCSA <38,39>
+1.2VSUS <3,17,18,34,36>
+1.0V_DEEP_SUS <9,13,15,16,35,36>
+1.0V <2,4,16,30,36>
+3VPCU <13,15,27,28,30,31,32,33,41>
+1.2V_VCCPLL_OC <36>

Need apply PN

U11N SKL_ULT
CPU POWER 3 OF 4
14 OF 20
*SKL_ULT
REV = 1

VDDQ_AU23 VDDQ_AU28 VDDQ_AU35 VDDQ_AU42 VDDQ_BB23 VDDQ_BB32 VDDQ_BB41 VDDQ_BB47 VDDQ_BB51 — 2A
VDDQC
VCCST — 0.12A
VCCSTG_A22 — 0.04A
VCCPLL_OC
VCCPLL_K20 / VCCPLL_K21 — 0.12A
VCCIO — 3.1A
VCCSA — 5A
VCCIO_SENSE
VSSIO_SENSE
VSSSA_SENSE
VCCSA_SENSE

+1.2VSUS
+VCCIO
+VCCSA
+VCCSTPLL
+VCCSTG
+VCCPLL_OC
+VCCPLL
+1.0V
+1.2V_VCCPLL_OC
Close U11
Under U11
120mA
PV
VCCIO_VCCSENSE
VCCIO_VSSSENSE
VSSSA_SENSE <38>
VCCSA_SENSE <38>

Under U11

Close U11

Close A18 Ball

IO Thrm Protect

For 65 degree, 1.8v limit, (SW)

For 75 degree, 1.2v limit, (HW)

+3VPCU
PV
R137 20K/F_4
THRM_MOINTOR1 <30>
C178 0.1U/10V_4
THER_CPU
R138 100K_4 NTC

Power Rail	Description	Control
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$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

+1.2VSUS
Close to CPU

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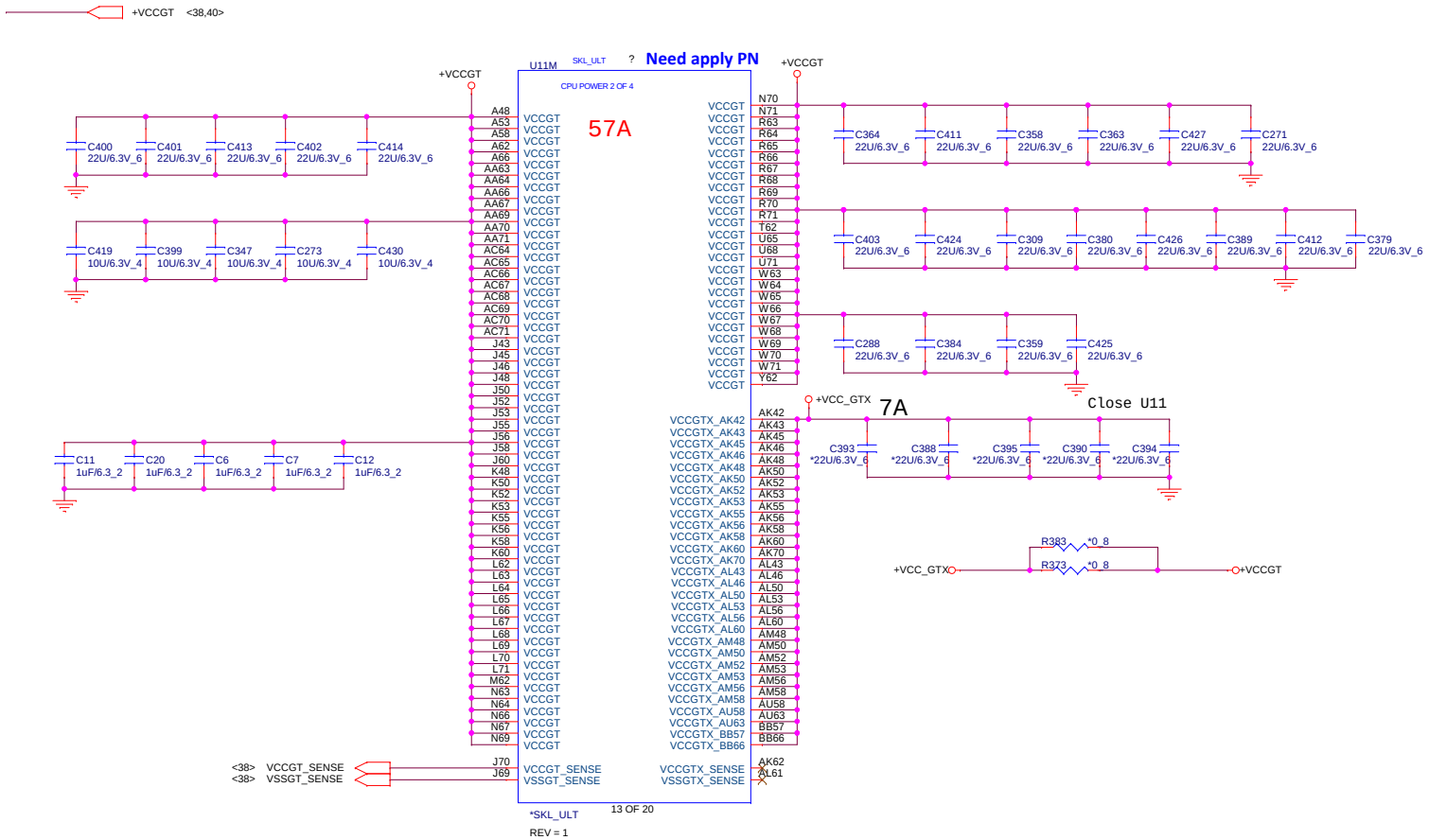

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Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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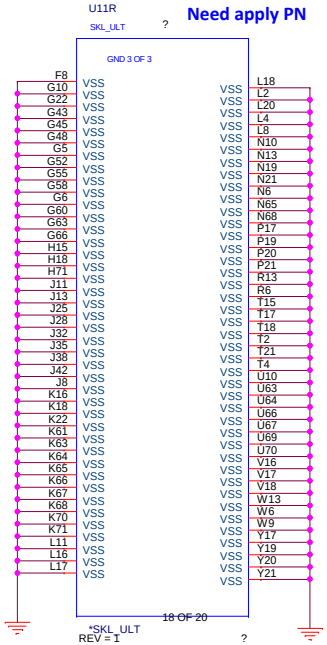

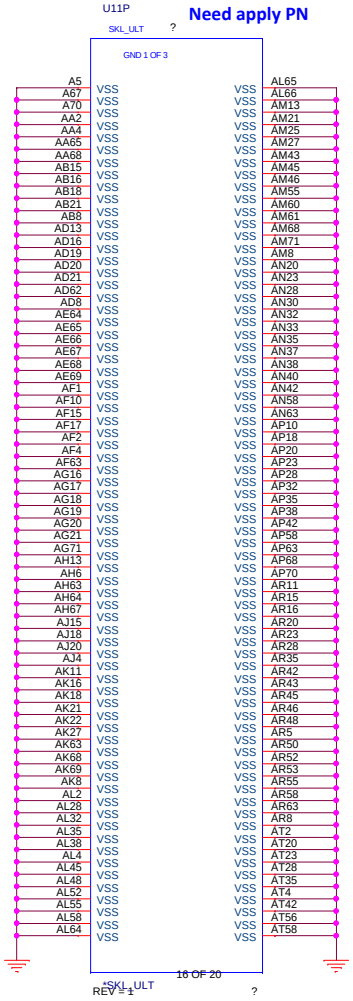

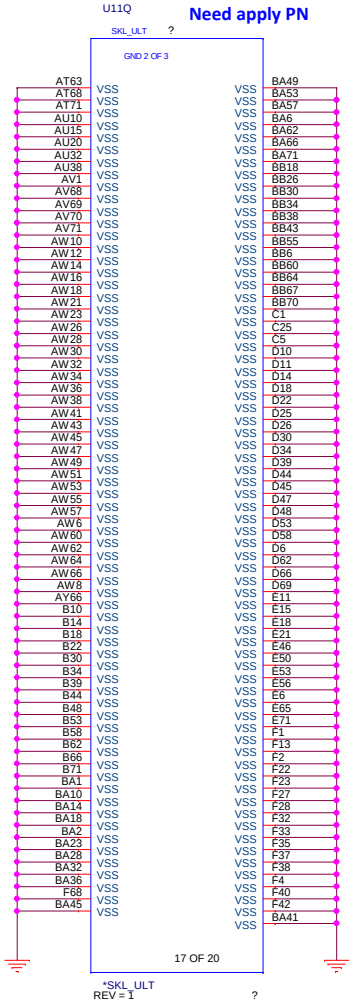

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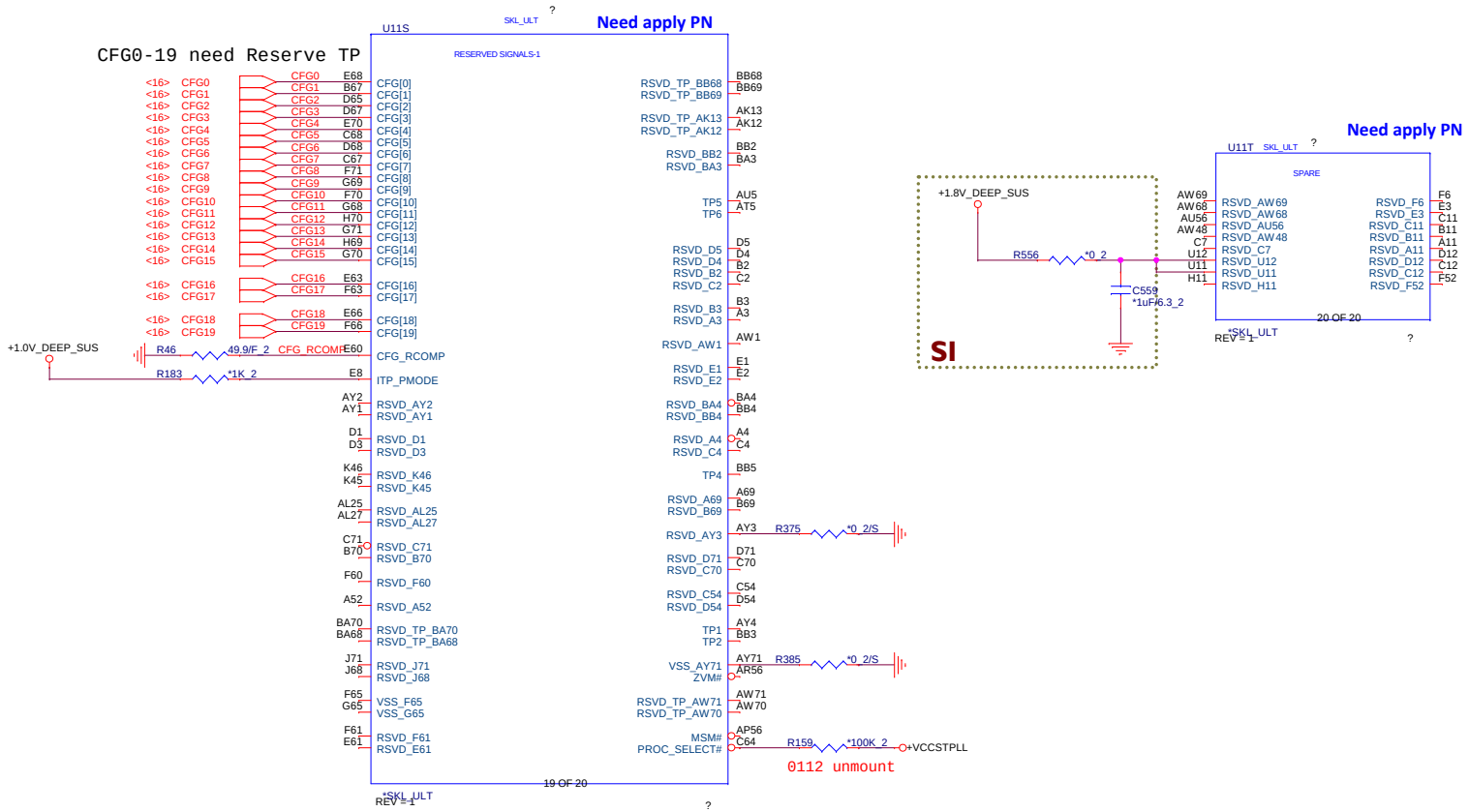

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R143 *1K_2
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R42 *1K_2

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+3V_DEEP_SUS <4,11,12,14,15,16>
+3V <2,4,11,12,13,14,15,16,20,21,22,23,25,26,27,29,30,31,37,38>
+5V <22,23,24,27,37,38>
+1.0V <2,4,6,16,30,36>
+3VS5 <4,15,16,22,28,30,31,33,35,36,37>

U11E SKL_ULT

Need apply PN

SPI - FLASH
PCH_SPI1_CLK AV2 SPI0_CLK
PCH_SPI1_SO AW3 SPI0_MISO
PCH_SPI1_SI AV3 SPI0_MOSI
PCH_SPI_IO2 AW2 SPI0_IO2
PCH_SPI_IO3 AU4 SPI0_IO3
PCH_SPI_CS0# AU3 SPI0_CS0#
AU2 SPI0_CS1#
AU1 SPI0_CS2#

SPI - TOUCH
<21> GPP_D1 GPP_D1 M2 GPP_D1/SPI1_CLK
<30> SIO_EXT_SMI# SIO_EXT_SMI# M3 GPP_D2/SPI1_MISO
<30> PCI_SERR# PCI_SERR# J4 GPP_D3/SPI1_MOSI
<24> GPP_D21 GPP_D21 V1 GPP_D21/SPI1_IO2
<24> GPP_D22 GPP_D22 V2 GPP_D22/SPI1_IO3
<24> GPP_D0 GPP_D0 M1 GPP_D0/SPI1_CS#

Support Vpro

C LINK
<28> CL_CLK G3 CL_CLK
<28> CL_DAT G2 CL_DATA
<28> CL_RST# G1 CL_RST#

<30> EC_RCIN# AW13 GPP_A0/RCIN#
<26,30> SERIRQ AY11 GPP_A6/SERIRQ

*SKL_ULT
REV = 1

5 OF 20

SMBUS, SMLINK
R7 SMB_PCH_CLK GPP_C0/SMBCLK
R8 SMB_PCH_DAT GPP_C1/SMBDATA
R10 SML0ALERT# GPP_C2/SMBALERT#
SML0ALERT# <11>
R9 SMB_ME0_CLK GPP_C3/SML0CLK
W2 SMB_ME0_DAT GPP_C4/SML0DATA
W1 SML1ALERT# GPP_C5/SML0ALERT#
SML1ALERT# <11>
W3 SMB_ME1_CLK GPP_C6/SML1CLK
V3 SMB_ME1_DAT GPP_C7/SML1DATA
AM7 GPP_B23 GPP_B23/SML1ALERT#/PCHHOT#
TP15

LPC
AY13 LAD0 <26,28,30> GPP_A1/LAD0/ESPI_IO0
BA13 LAD1 <26,28,30> GPP_A2/LAD1/ESPI_IO1
BB13 LAD2 <26,28,30> GPP_A3/LAD2/ESPI_IO2
AY12 LAD3 <26,28,30> GPP_A4/LAD3/ESPI_IO3
BA12 LFRAME# <26,28,30> GPP_A5/LFRAME#/ESPI_CS#
BA11 GPP_A14/SUS_STAT#/ESPI_RESET#

AW9 CLK_PCI_EC_R R408 22/F_4
AY9 CLK_PCI_LPC_R R404 22/F_4
AW11 CLKRUN# CLKRUN# <30>
GPP_A9/CLKOUT_LPC0/ESPI_CLK
GPP_A10/CLKOUT_LPC1
GPP_A8/CLKRUN#

EC25 18P/50V_4
CLK_24M_KBC <30>
CLK_24M_DEBUG <28>
EMI(near PCH)
EC24 18P/50V_4
R409 22/F_4
CLK_PCI_TPM <26>
EC23 18P/50V_4
EMI(near PCH)

GPIO Pull UP

+3V
SERIRQ R377 10K_2
CLKRUN# R380 8.2K/F_4
SIO_EXT_SMI# R205 10K_2
EC_RCIN# R378 10K_2
PCI_SERR# R202 10K_2

+3V_DEEP_SUS
SMB_PCH_CLK R360 2.2K_2
SMB_PCH_DAT R366 2.2K_2
SMB_ME0_CLK R232 499/F_4
SMB_ME0_DAT R257 499/F_4
SMB_ME1_CLK R341 1K_2
SMB_ME1_DAT R333 1K_2
<12> ACC_LED# R173 10K_2
SI

SMBus/Pull-up(CLG)

SI 2
DEL Q20

+3V
R356 4.7K_2
<16,27> SMB_RUN_DAT
R364 4.7K_2
<16,27> SMB_RUN_CLK
Q21
SMB_PCH_DAT
SMB_PCH_CLK
2N7002KDW

Touch Pad
XDP
LPDDR3 thermal sensor

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PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket

<30> PCH_SPI_CS0#_R PCH_SPI_CS0# R
<30> PCH_SPI1_CLK_R PCH_SPI1_CLK_R
<30> PCH_SPI1_SI_R PCH_SPI1_SI_R
<30> PCH_SPI1_SO_R PCH_SPI1_SO_R
BIOS_WP#
+3VSPI
SI
HOLD#

U23&U24 footprint 要重疊

TP66-71 need place to TOP
TP65 PCH_SPI_CS0# R
TP68 PCH_SPI1_CLK_R
TP71 PCH_SPI1_SI_R
TP67 PCH_SPI1_SO_R
TP70 BIOS_WP#
TP66 HOLD#

PCH SPI ROM(CLG)

<15> +3V_M

+3V_M
U17
PCH_SPI_CS0# R340 15/F_4 PCH_SPI_CS0# R
PCH_SPI1_CLK R381 15/F_4 PCH_SPI1_CLK_R
PCH_SPI1_SI R387 15/F_4 PCH_SPI1_SI_R
PCH_SPI1_SO R384 15/F_4 PCH_SPI1_SO_R
CE# VDD +3VSPI
SCK
SI
SO HOLD# 7HOLD# R343 1K_4
WP# VSS R342 15/F_4
GD25B64BSIGR
AKE3EFP0N07
R457/R453/R450/R451/R546/R548 close to U15 pin
C373 22P/50V_4
C346 0.1U/10V_4
C376 1U/10V_4 +3VSPI R359 1K_4
PCH_SPI_IO2 R365 15/F_4 BIOS_WP#
PCH_SPI_IO3

NB5

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Quanta Computer Inc.

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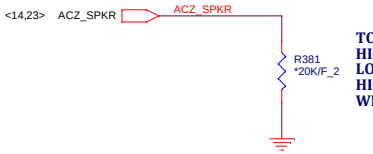
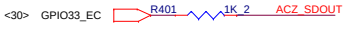
Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET

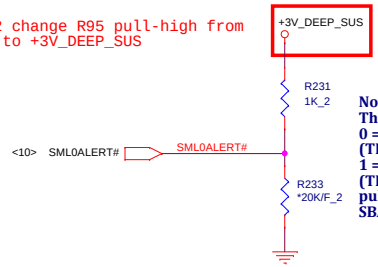


TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

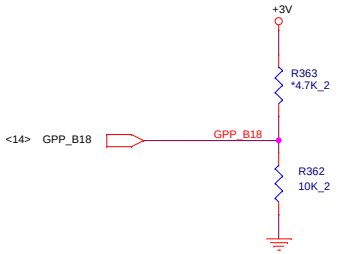
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



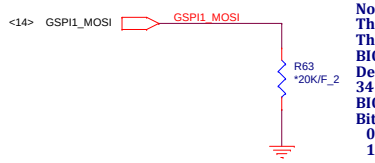
1212 change R95 pull-high from +3V to +3V_DEEP_SUS



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

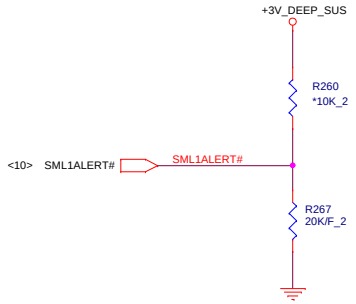


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO
Timer system reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

NB5

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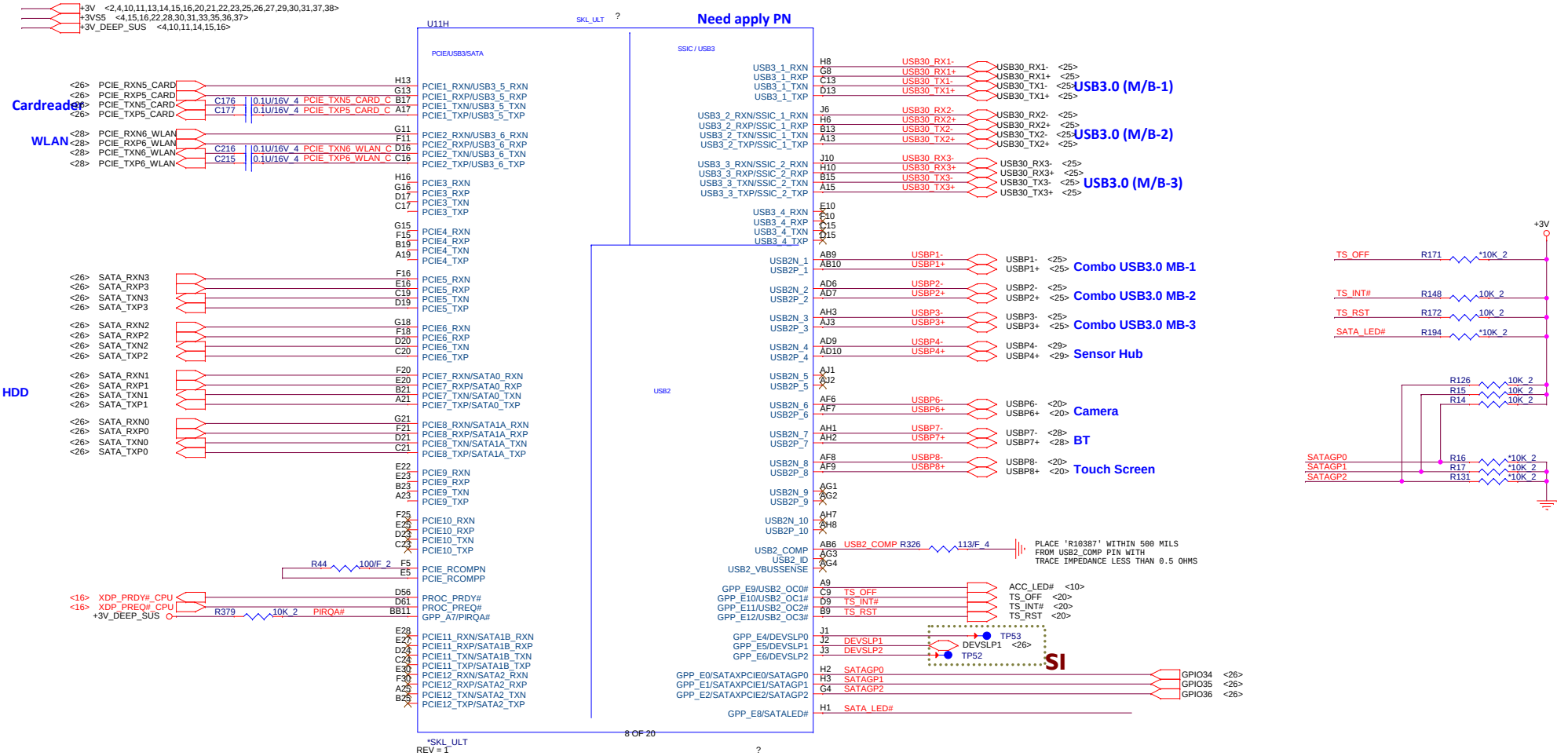

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	CardReader	Port0	Un-used
Port2	WLAN	Port1	CardReader
Port3	Un-used	Port2	WLAN
Port4	Un-used	Port3	Un-used
Port5	SSD	Port4	Un-used
Port6	SSD	Port5	SSD
Port7	SSD		
Port8	SSD		
Port9	Un-used		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 MB-2
PORT-3	USB3.0 MB-3
PORT-4	Sensor Hub
PORT-5	NC
PORT-6	Camera
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

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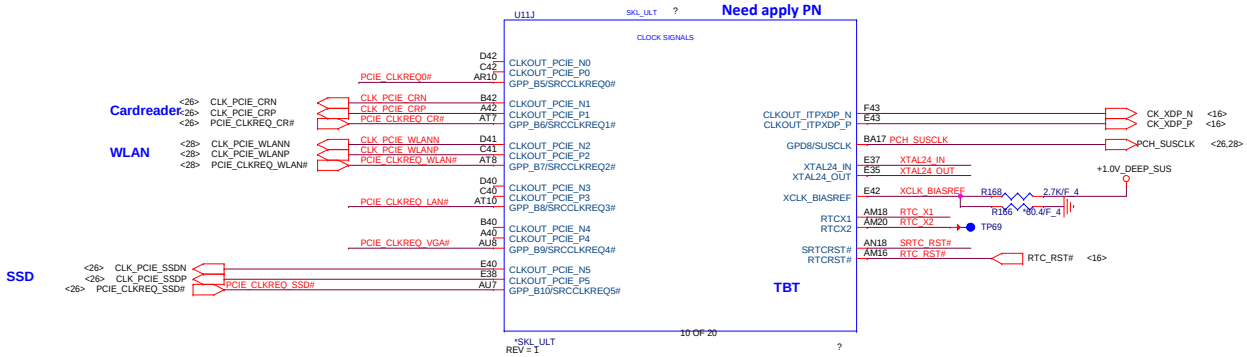
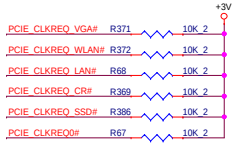
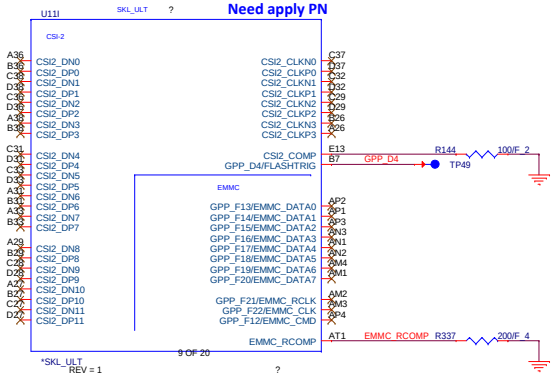
+1.8V_DEEP_SUS <9,15,35,37>
+3V <2,4,10,11,12,14,15,16,20,21,22,23,25,26,27,29,30,31,37,38>

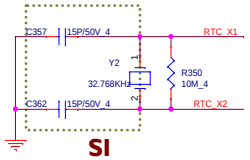


CLK_REQ/Strap Pin(CLG)





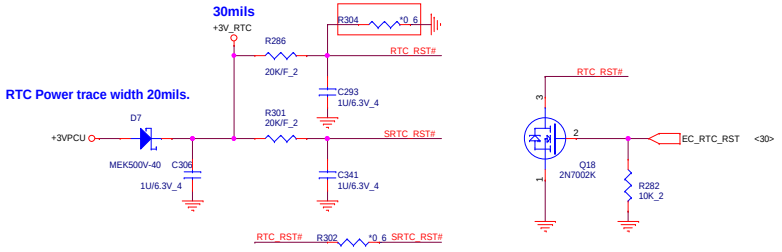
RTC Clock 32.768KHz



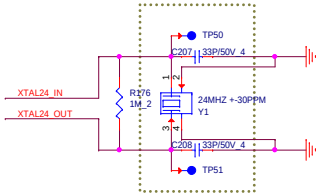
SI

RTC Circuitry(RTC)

+3V_RTC <4,15,27,31,32>
+3VPCU <6,15,27,28,30,31,32,33,41>



External Crystal



SI 2

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Skylake (GPIO)

+3V <2,4,10,11,12,13,15,16,20,21,22,23,25,26,27,29,30,31,37,38>
+3V_DEEP_SUS <4,10,11,12,15,16>

+3V_DEEP_SUS

BT_OFF R219 10K_2
PCH_TEMPALERT# R249 10K_2
SIO_EXT_SCI# R338 10K_2
ACCEL_INTA# R327 *10K_2
UART2_RXD R306 49.9K_4
UART2_TXD R314 49.9K_4

PV

1227 Add R536 and R537 for UART2 function reserved

U11F SKL_ULT ? **Need apply PN**

LPSS

TP18 GPP_B15 AN8 GPP_B15/GSPI0_CS#
TP30 GPP_B16 AP7 GPP_B16/GSPI0_CLK
TP33 GPP_B17 AP8 GPP_B17/GSPI0_MISO
<11> GPP_B18 GPP_B18 AR7 GPP_B18/GSPI0_MOSI
TP25 GPP_B19 AM5 GPP_B19/GSPI1_CS#
TP27 GPP_B20 AN7 GPP_B20/GSPI1_CLK
TP29 GPP_B21 AP5 GPP_B21/GSPI1_MISO
<11> GSPI1_MOSI GSPI1_MOSI AN5 GPP_B22/GSPI1_MOSI
TP64 GPP_C8 AB1 GPP_C8/UART0_RXD
TP62 GPP_C9 AB2 GPP_C9/UART0_TXD
TP61 GPP_C10 W4 GPP_C10/UART0_RTS#
TP12 GPP_C11 AB3 GPP_C11/UART0_CTS#
<25> UART2_RXD UART2_RXD AD1 GPP_C20/UART2_RXD
<25> UART2_TXD UART2_TXD AD2 GPP_C21/UART2_TXD
ACCEL_INTA# AD3 GPP_C22/UART2_RTS#
<30> SIO_EXT_SCI# SIO_EXT_SCI# AD4 GPP_C23/UART2_CTS#

U7
U6
GPP_C16/I2C0_SDA
GPP_C17/I2C0_SCL
TP9 I2C1_SDA U8 GPP_C18/I2C1_SDA
TP10 I2C1_SCL U9 GPP_C19/I2C1_SCL
AH9 GPP_F4/I2C2_SDA
AH10 GPP_F5/I2C2_SCL
AH11 GPP_F6/I2C3_SDA
AH12 GPP_F7/I2C3_SCL
AF11 GPP_F8/I2C4_SDA
AF12 GPP_F9/I2C4_SCL

*SKL_ULT
REV = 1

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ISH

P2 GPP_D9 TP76 GPP_D9
P3 GPP_D10 TP77 GPP_D10
P4 GPP_D11 GPP_D11 <26> BT_OFF BT_OFF <28> GPP_D11
P1 GPP_D12
M4 ISH_I2C0_SDA ISH_I2C0_SDA <29> GPP_D5/ISH_I2C0_SDA
N3 ISH_I2C0_SCL ISH_I2C0_SCL <29> GPP_D6/ISH_I2C0_SCL
N1 ISH_I2C1_SDA GPP_D7/ISH_I2C1_SDA
N2 ISH_I2C1_SCL GPP_D8/ISH_I2C1_SCL
AD11 ISH_I2C2_SDA TP14 GPP_F10/I2C5_SDA/ISH_I2C2_SDA
AD12 ISH_I2C2_SCL TP11 GPP_F11/I2C5_SCL/ISH_I2C2_SCL
U1 PCH_TEMPALERT# TP59 GPP_D13/ISH_UART0_RXD/SML0BDATA/I2C4B_SDA
U2 SML0BDATA TP58 GPP_D14/ISH_UART0_TXD/SML0BCLK/I2C4B_SCL
U3 SML0BCLK TP57 GPP_D15/ISH_UART0_RTS#
U4 SML0BALERT# TP60 GPP_D16/ISH_UART0_CTS#/SML0BALERT#
AC1 UART1_RXD TP19 GPP_C12/UART1_RXD/ISH_UART1_RXD
AC2 UART1_TXD TP20 GPP_C13/UART1_TXD/ISH_UART1_TXD
AC3 UART1_RTS TP23 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
AB4 UART1_CTS TP17 GPP_C15/UART1_CTS#/ISH_UART1_CTS#

R8 *10K_2 COOL SENSE R2 *10K_2 COOL SENSE
R6 *10K_2 ISH_GYRO_DRDY R9 *10K_2 ISH_GYRO_DRDY
R4 *10K_2 ISH_GYRO_INT R7 10K_2 ISH_GYRO_INT
ISH_AE_INT R5 10K_2 ISH_AE_INT
ISH_ACC_INT R3 10K_2 ISH_ACC_INT
DISABLE KB R1 *10K_2 DISABLE KB
GPP_A12 R414 *10K_2 GPP_A12
ISH_I2C0_SDA R210 10K_2 ISH_I2C0_SDA
ISH_I2C0_SCL R212 10K_2 ISH_I2C0_SCL
ISH_I2C2_SDA R53 10K_2 ISH_I2C2_SDA
ISH_I2C2_SCL R52 10K_2 ISH_I2C2_SCL

AY8 COOL SENSE ISH_GYRO_DRDY <29>
BA8 ISH_GYRO_INT <29>
BB7 ISH_AE_INT <29>
BA7 ISH_ACC_INT <29>
AY7 DISABLE KB DISABLE KB <29>
AW7 GPP_A12
AP13

R311 10K_2 BOARD_ID0 R313 *10K_2
R307 10K_2 BOARD_ID1 R322 *10K_2
R315 10K_2 BOARD_ID2 R328 *10K_2
R274 10K_2 BOARD_ID3 R275 *10K_2
R289 10K_2 BOARD_ID4 R273 *10K_2
R291 10K_2 BOARD_ID5 R288 *10K_2
R290 10K_2 BOARD_ID6 R303 *10K_2
R317 10K_2 BOARD_ID7 R316 *10K_2
R392 *10K_2 BOARD_ID8 R396 10K_2

+3V_DEEP_SUS

HDA Bus(CLG)

+3V_DEEP_SUS R390 *1K_4 ACZ_SYNC
<23> ACZ_SYNC_AUDIO R394 33_4 ACZ_SYNC
<23> ACZ_RST#_AUDIO R388 33_4 ACZ_RST#
<23> ACZ_SDOUT_AUDIO R400 33_4 ACZ_SDOUT
<23> BIT_CLK_AUDIO R402 33_4 ACZ_BCLK
C423 *10P/50V_4

CN1
1 ISH_I2C0_SCL
2 ISH_I2C0_SDA
3 ISH_I2C1_SCL
4 ISH_I2C1_SDA
5
6 ISH_GYRO_DRDY
7 ISH_GYRO_INT
8 ISH_AE_INT
9 ISH_ACC_INT
10
11 COOL SENSE
12 DISABLE KB
13 TP5
14 TP3
15 TP2
16 TP1
17 +3V
18
*ACES_88511-180N

1207
Add Sensors Debug CONN

1209
Change CN5012 footprint from 88511-180n-18p-l to fg-12x59-20-18p

U11G SKL_ULT ? **Need apply PN**

AUDIO

<11> ACZ_SDOUT ACZ_SYNC BA22 HDA_SYNC/I2S0_SFRM
<23> ACZ_SDIN0 ACZ_BCLK AY22 HDA_BLK/I2S0_SCLK
ACZ_SDOUT BB22 HDA_SDO/I2S0_TXD
ACZ_SDIN0 BA21 HDA_SDI0/I2S0_RXD
AY21 HDA_SDI1/I2S1_RXD
ACZ_RST# AW22 HDA_RST#/I2S1_SCLK
J5 GPP_D23/I2S_MCLK
AY20 I2S1_SFRM
AW20 I2S1_TXD
TP22 SSP2_SFRM AK7 GPP_F1/I2S2_SFRM
TP16 SSP2_SCLK AK6 GPP_F0/I2S2_SCLK
TP13 SSP2_TXD AK9 GPP_F2/I2S2_TXD
TP26 SSP2_RXD AK10 GPP_F3/I2S2_RXD
TP7 GPP_D19 H5 GPP_D19/DMIC_CLK0
TP44 GPP_D20 D7 GPP_D20/DMIC_DATA0
TP48 GPP_D17 D8 GPP_D17/DMIC_CLK1
TP43 GPP_D18 C8 GPP_D18/DMIC_DATA1
<11,23> ACZ_SPKR ACZ_SPKR AW5 GPP_B14/SPKR

*SKL_ULT
REV = 1

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SDIO/SDXC

GPP_G0/SD_CMD AB11 BOARD_ID0
GPP_G1/SD_DATA0 AB13 BOARD_ID1
GPP_G2/SD_DATA1 AB12 BOARD_ID2
GPP_G3/SD_DATA2 W12 BOARD_ID3
GPP_G4/SD_DATA3 W11 BOARD_ID4
GPP_G5/SD_CD# W10 BOARD_ID5
GPP_G6/SD_CLK W8 BOARD_ID6
GPP_G7/SD_WP W7 BOARD_ID7
GPP_A17/SD_PWR_EN#/ISH_GP7 BA9 BOARD_ID8
GPP_A16/SD_1P8_SEL BB9 GPP_A16 GPP_A16 <25>
SD_RCOMP AB7 R54 200/F_2
GPP_F23 AF13

Model	BOARD_ID8	BOARD_ID7	Board ID [6:4]	BOARD_ID[3:1]	BOARD_ID0
Y0DD	0:VPRO 1:non-VPRO	0:2+2 CPU 1:2+3E CPU	Reserve (Default = 00)	000:H9CCNNNBKTMLBR-NTD Hynix 4G 1600 001:EDFA164A2MA-GD-F ELPIDA 4G 1600 010:K3QF2F20EM-AGCF Samsung 4G 1866 011: Hynix 4G 1866 100:ELPIDA 4G 1866 000:H9CCNNNCPTMLBR-NTD Hynix 8G 1600 001:EDFB164A1MA-GD-F Micron 8G 1600 010: Samsung 8G 1866 011:H9CCNNNCPTMLBR-NUD Hynix 8G 1866 100: ELPIDA 8G 1866	0:4G 1:8G

NB5

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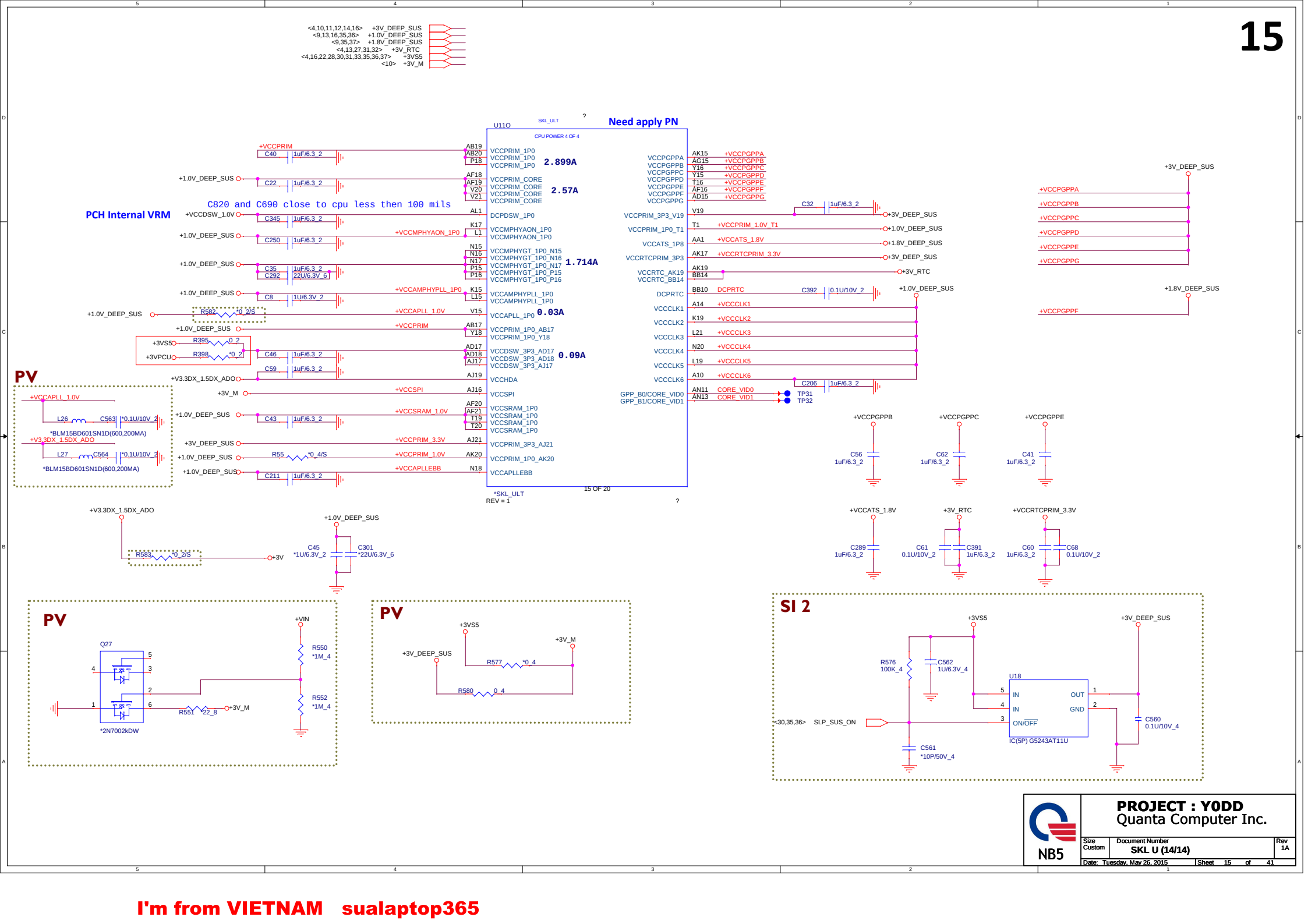

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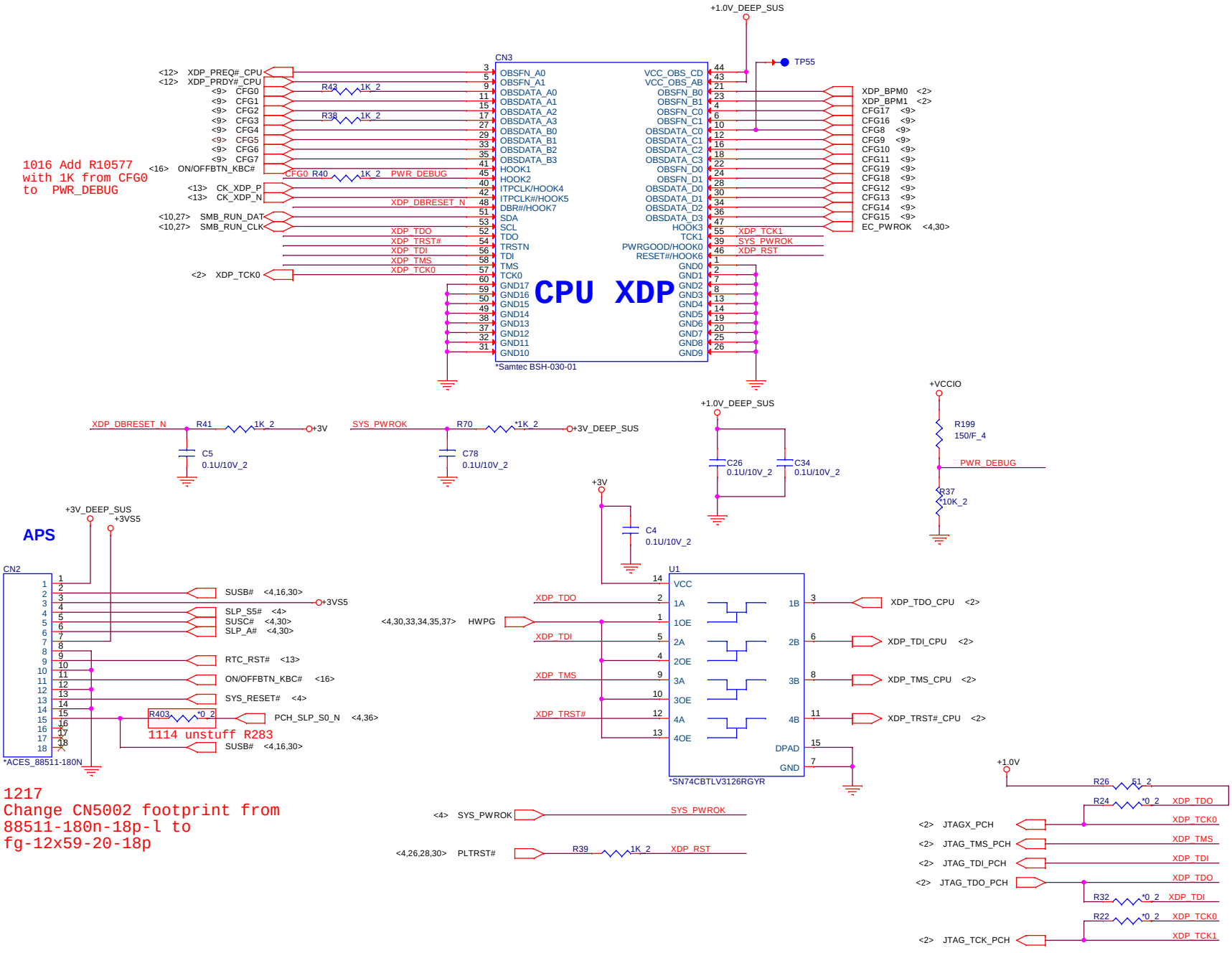

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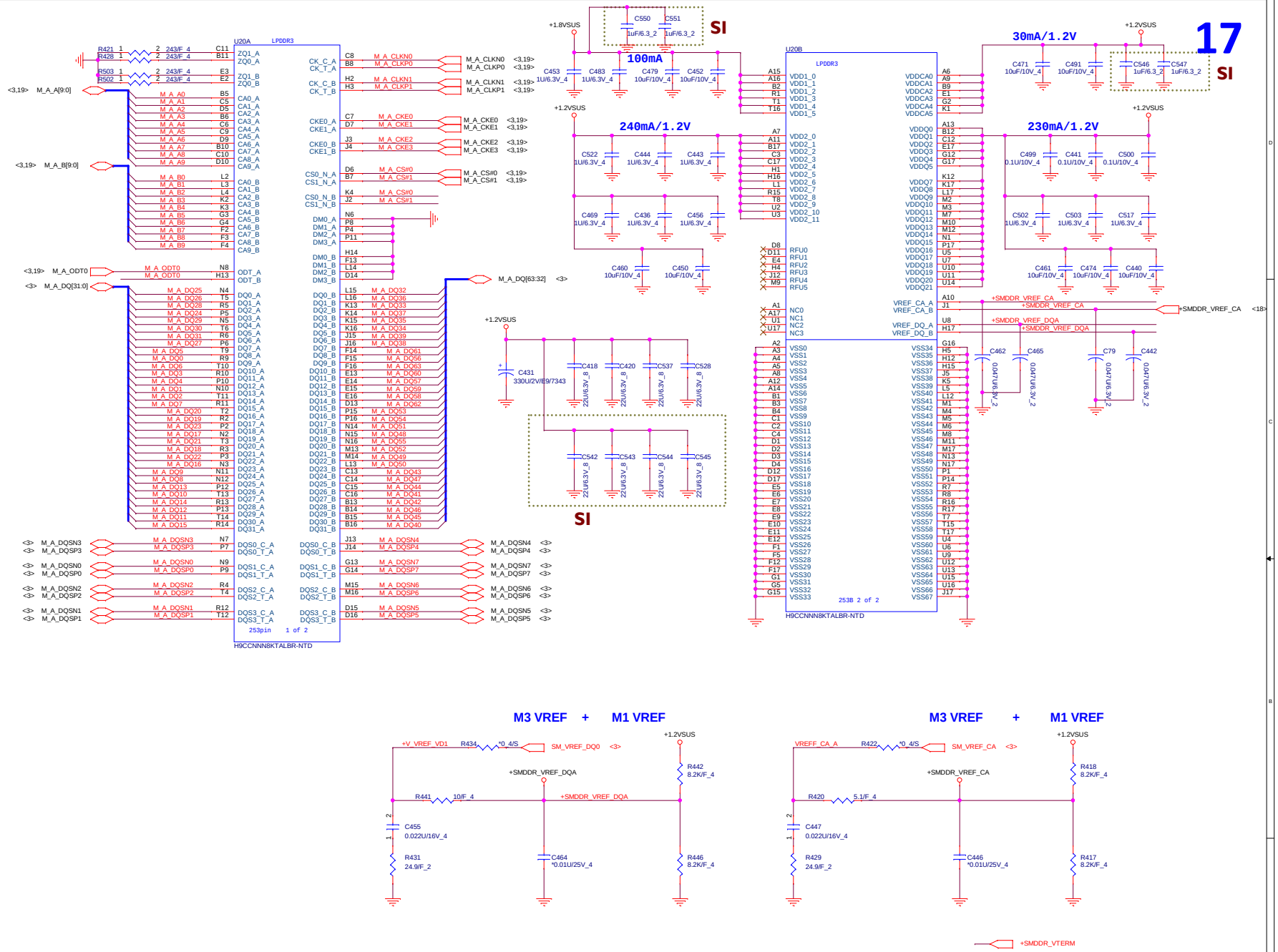
17
SI
U20A
LPDDR3
H9CCNNN8KTALBR-NTD
253pin 1 of 2
U20B
253B 2 of 2
100mA
240mA/1.2V
30mA/1.2V
230mA/1.2V
+1.8VSUS
+1.2VSUS
M_A_A[9:0]
M_A_B[9:0]
M_A_ODT0
M_A_DQ[31:0]
M_A_DQ[63:32]
M_A_CLKN0
M_A_CLKP0
M_A_CLKN1
M_A_CLKP1
M_A_CKE0
M_A_CKE1
M_A_CKE2
M_A_CKE3
M_A_CS#0
M_A_CS#1
+SMDDR_VREF_CA
+SMDDR_VREF_DQA
M3 VREF + M1 VREF
+V_VREF_VD1
SM_VREF_DQ0
VREFF_CA_A
SM_VREF_CA
+SMDDR_VTERM
PROJECT : Y0DD
Quanta Computer Inc.
LPDDR3 CHA
Date: Tuesday, May 26, 2015
Sheet 17 of 41
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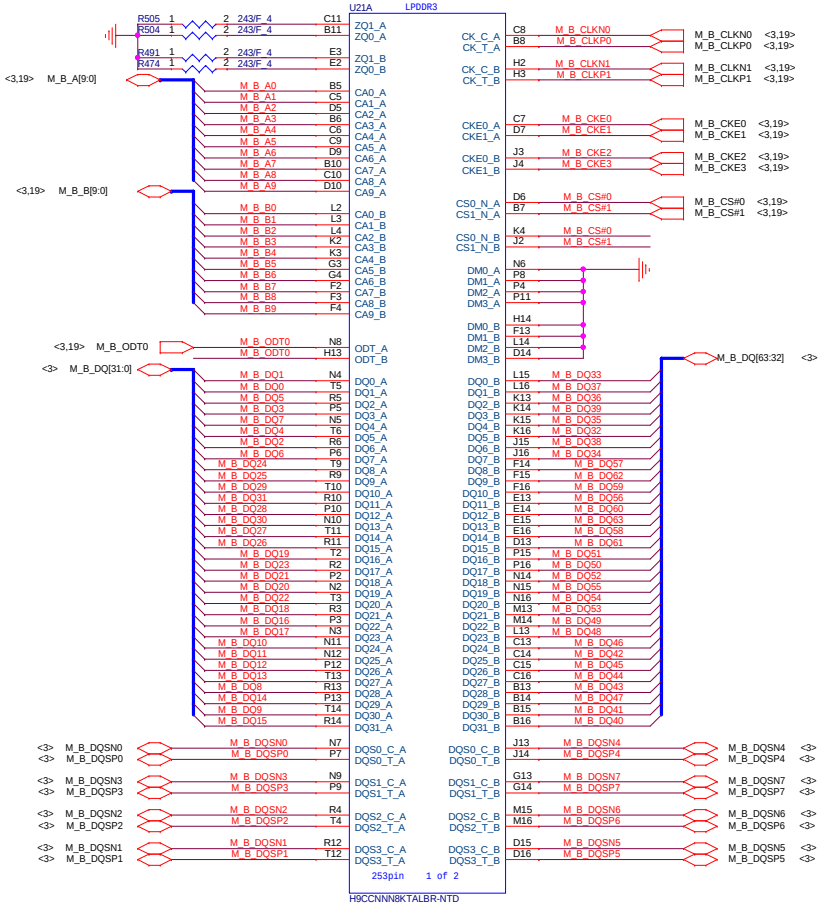

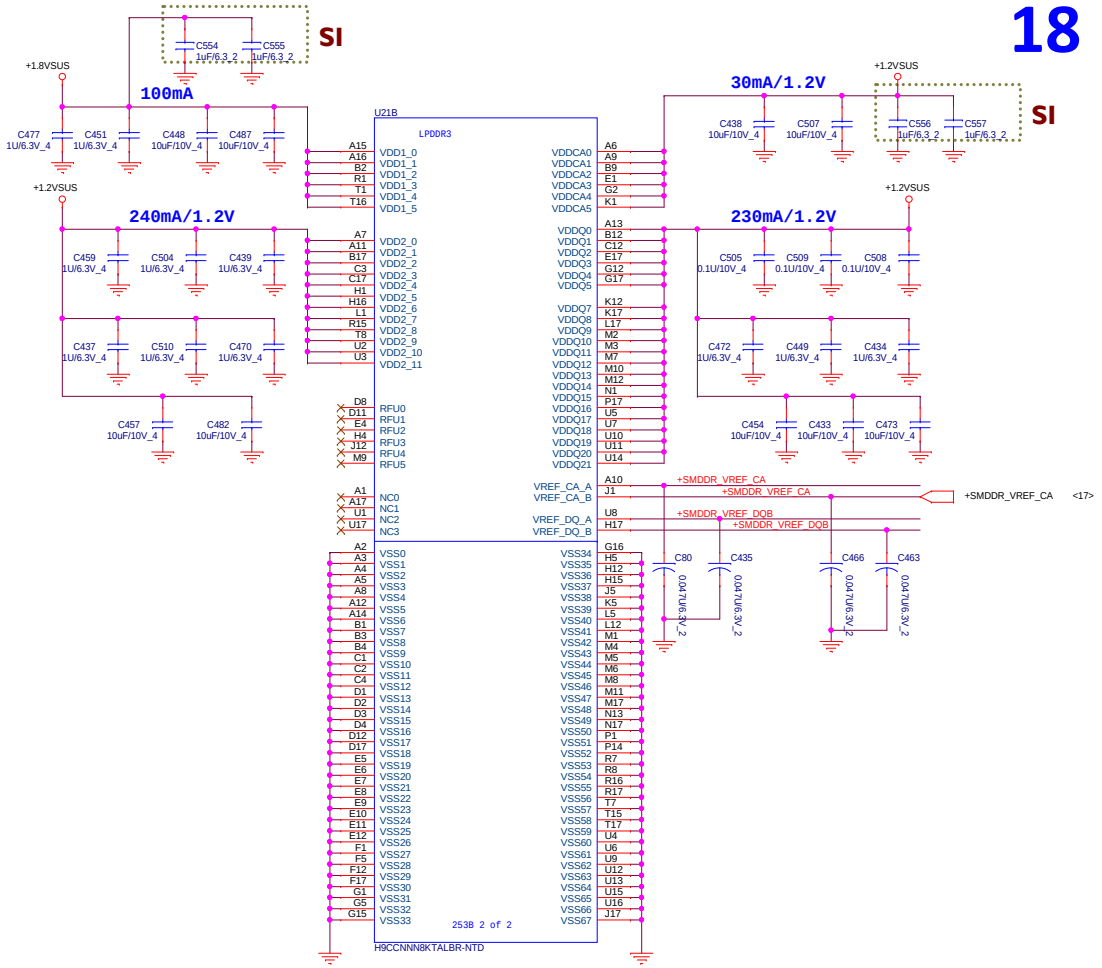

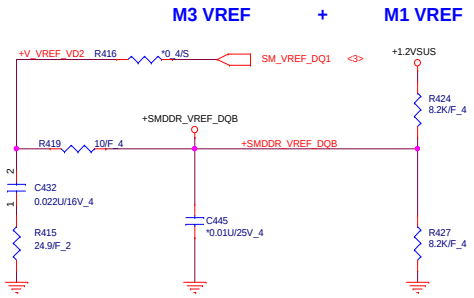

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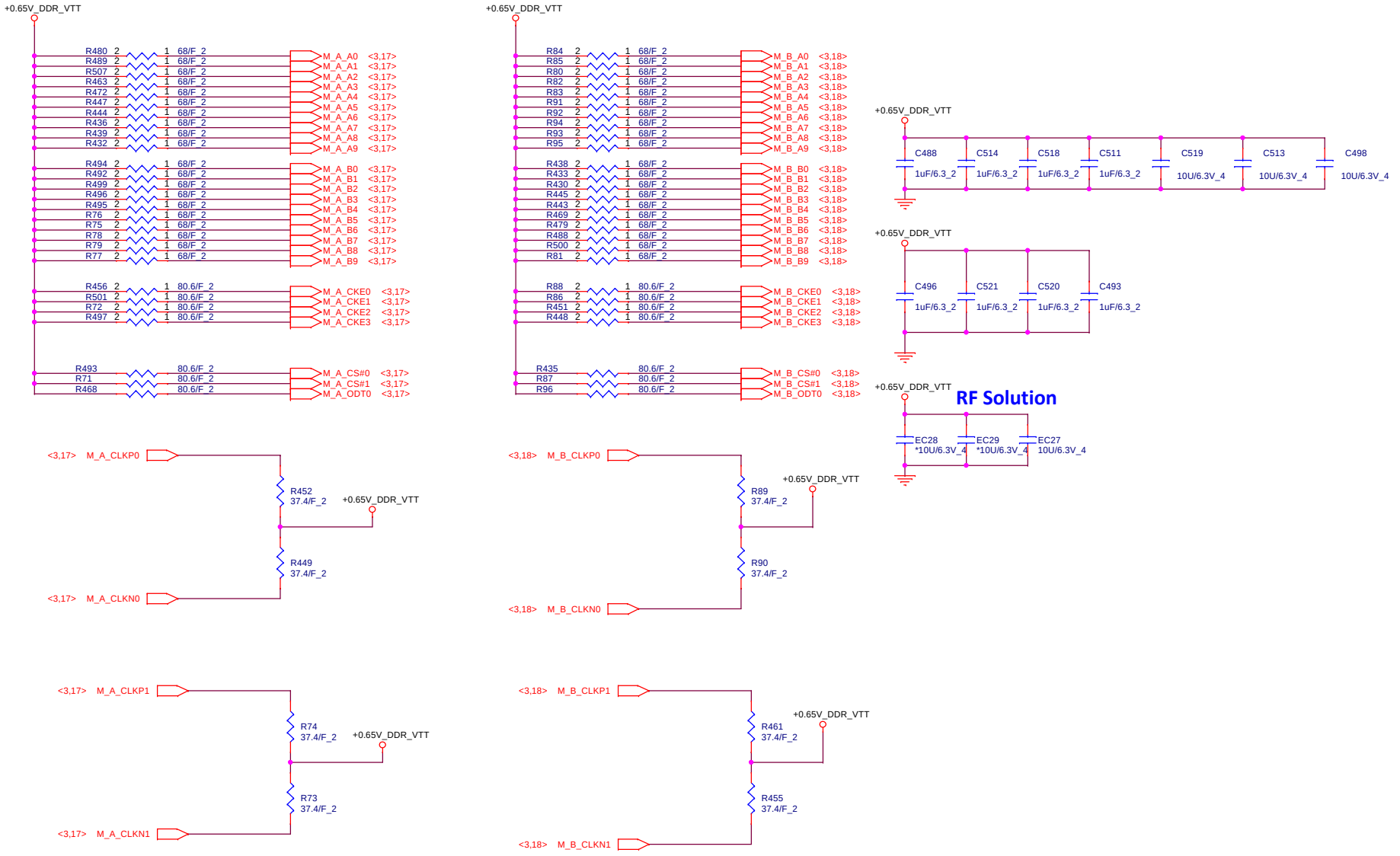
NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: LPDDR3 CHB	Rev: 1A
Date: Tuesday, May 26, 2015	Sheet 18 of 41	



NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LPDDR3 TERMINATION	1A

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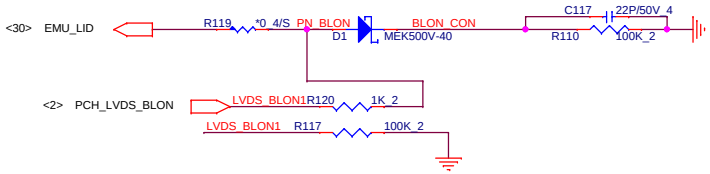
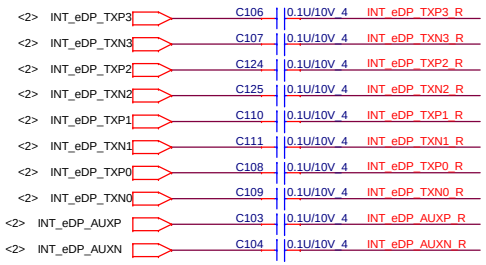
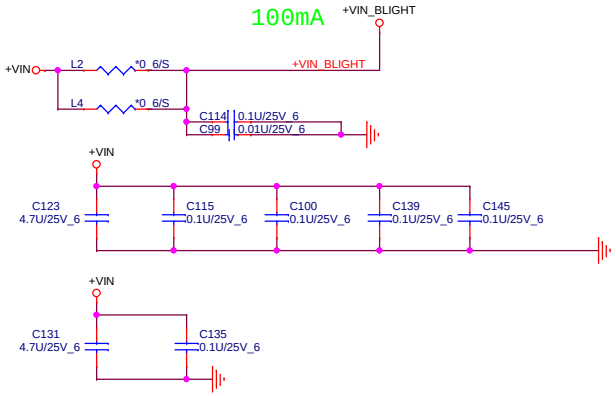
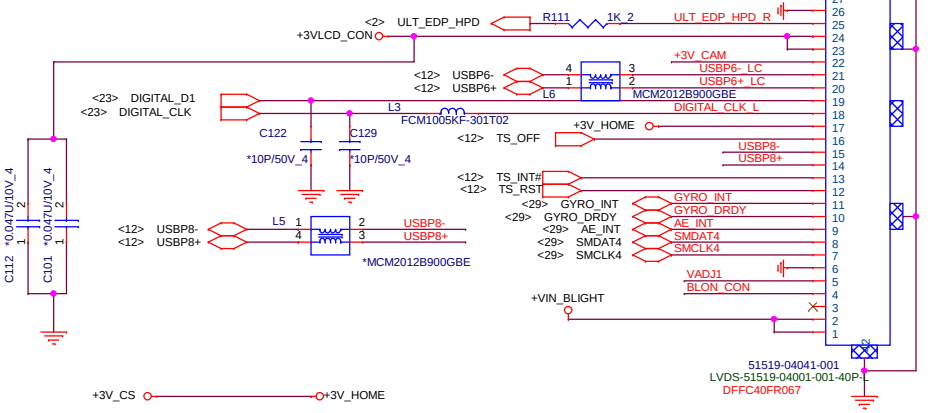
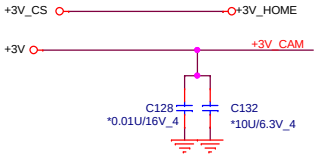
LID Switch

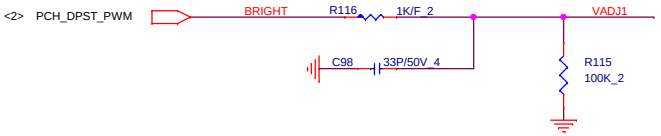


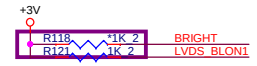




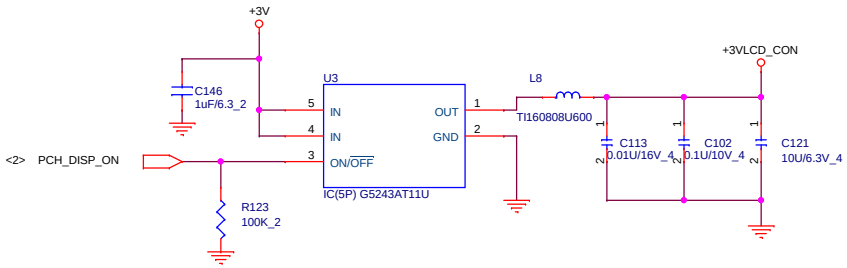








SI modify
R74 non-stuff



<2,4,10,11,12,13,14,15,16,21,22,23,25,26,27,29,30,31,37,38> +3V
<6,13,15,27,28,30,31,32,33,41> +3VPCU
<22,23,24,27,37,38> +5V
<15,27,30,32,33,34,35,38,39,40,41> +VIN

NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN/CAM/LID	Rev: 1A
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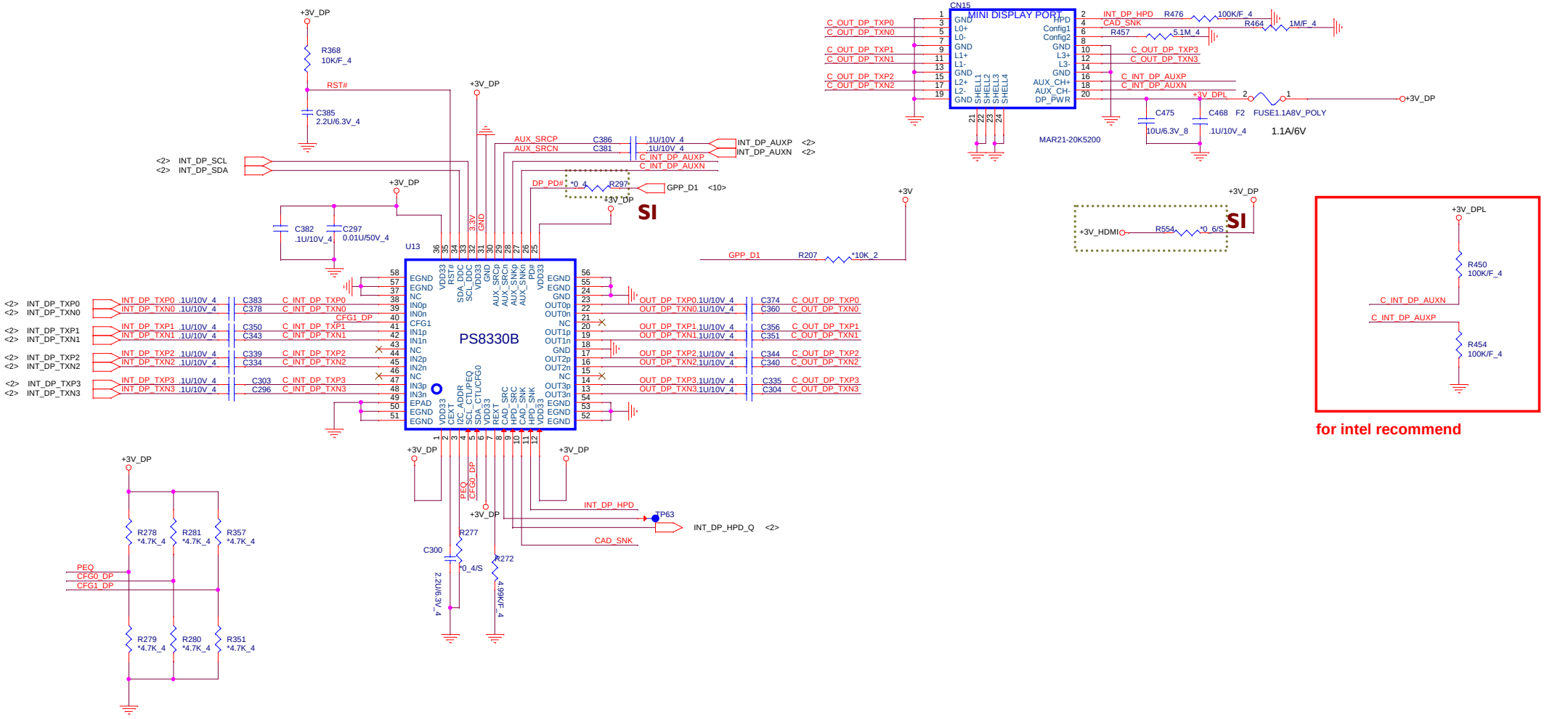
Mini Display

+5V <22,23,24,27,37,38>
+3V <2,4,10,11,12,13,14,15,16,20,22,23,25,26,27,29,30,31,37,38>



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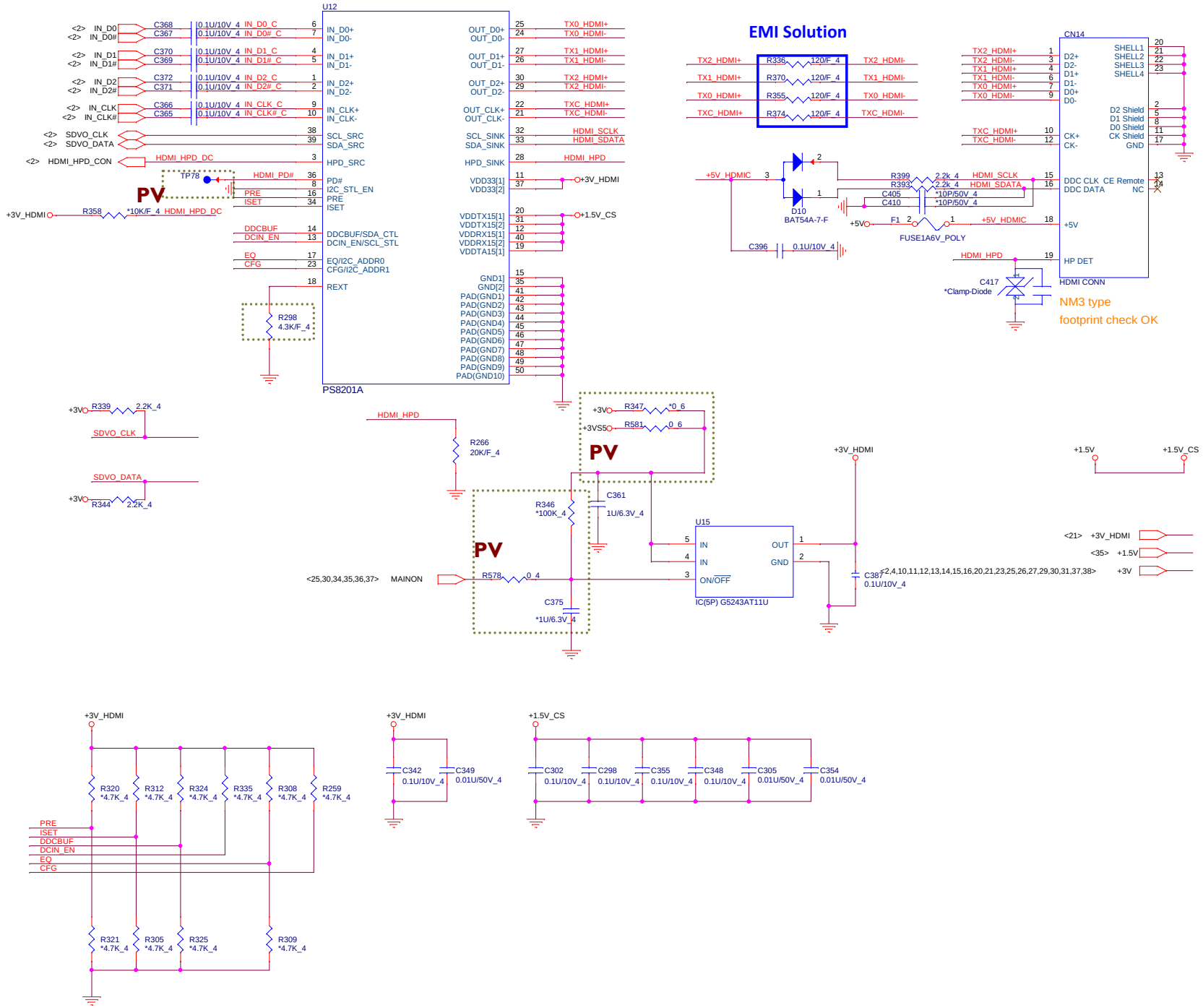

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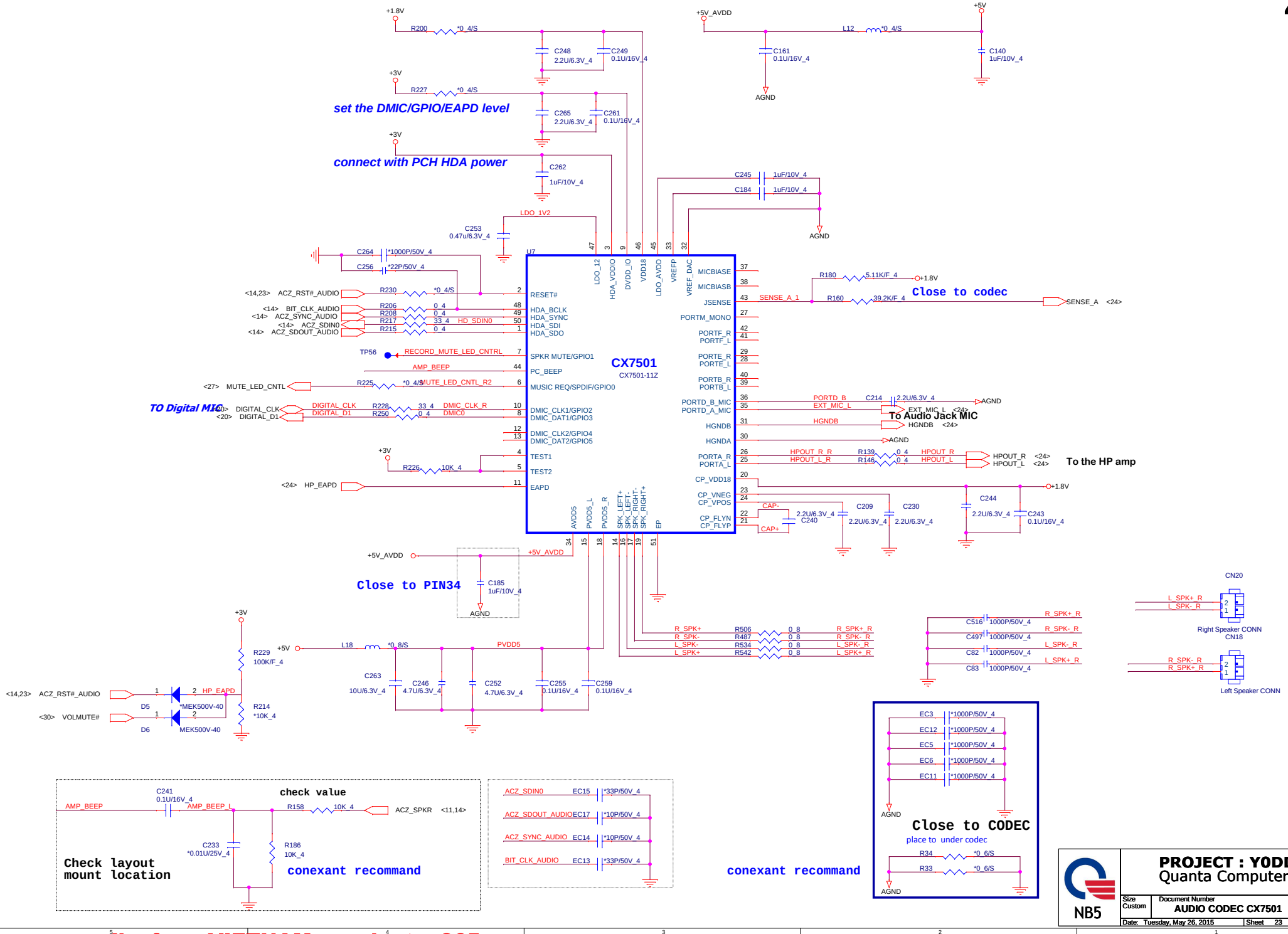
NB5	PROJECT : Y0DD Quanta Computer Inc.		
	Size: Custom	Document Number: HDMI	Rev: 1A
	Date: Tuesday, May 26, 2015	Sheet 22 of 41	



PROJECT : Y0DD	Quanta Computer Inc.
NB5	Size: Custom
Document Number: AUDIO CODEC CX7501	Rev: 1A
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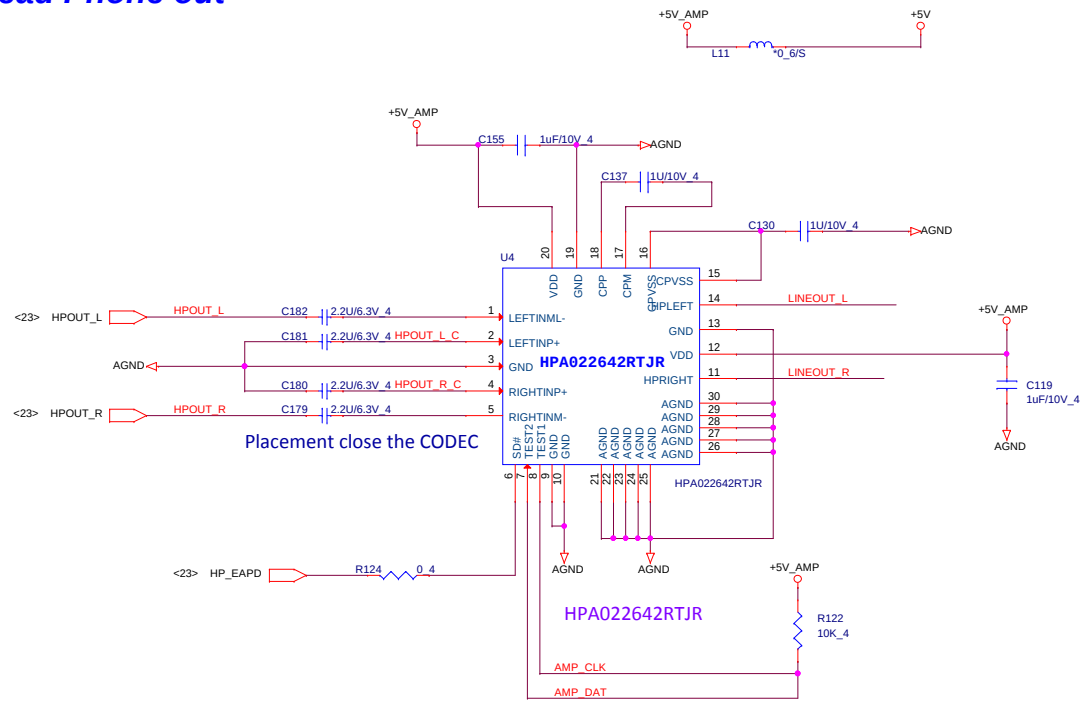
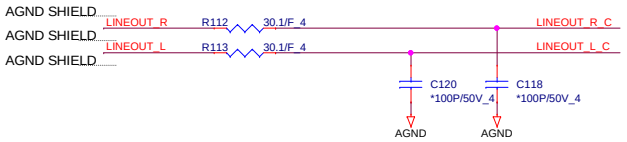
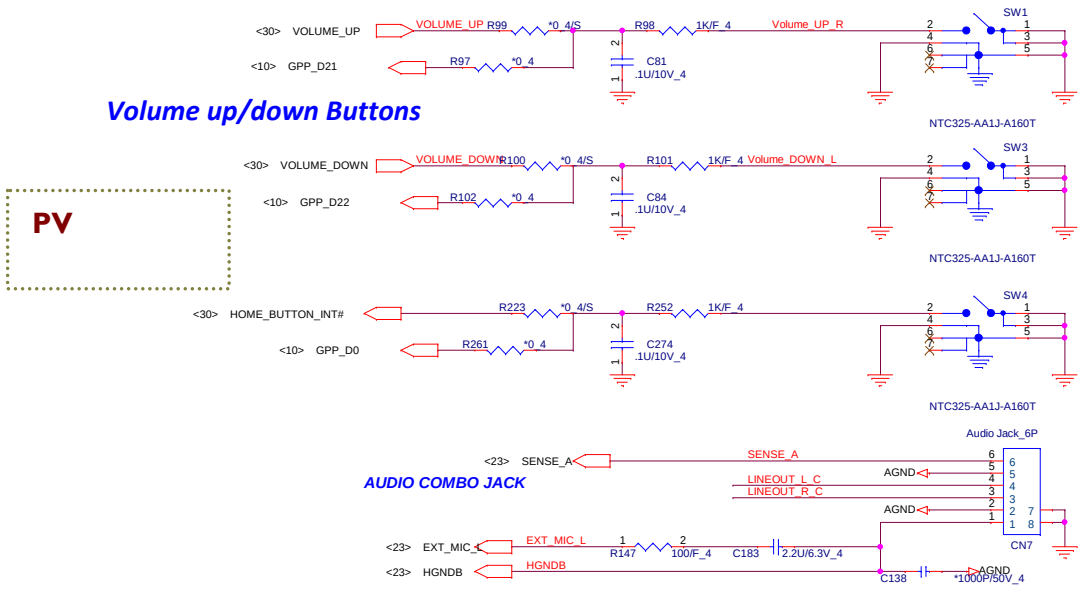
Head Phone out

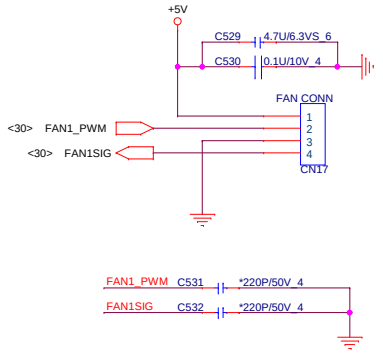




Audio combo JACK & Volume up/down Button



FAN



<2,4,10,11,12,13,14,15,16,20,21,22,23,25,26,27,29,30,31,37,38> +3V
<22,23,27,37,38> +5V
<4,25,33,34,35,36,37> +5VS

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AUDIO AMP	1A
Date: Tuesday, May 26, 2015	Sheet 24 of 41	

NB5

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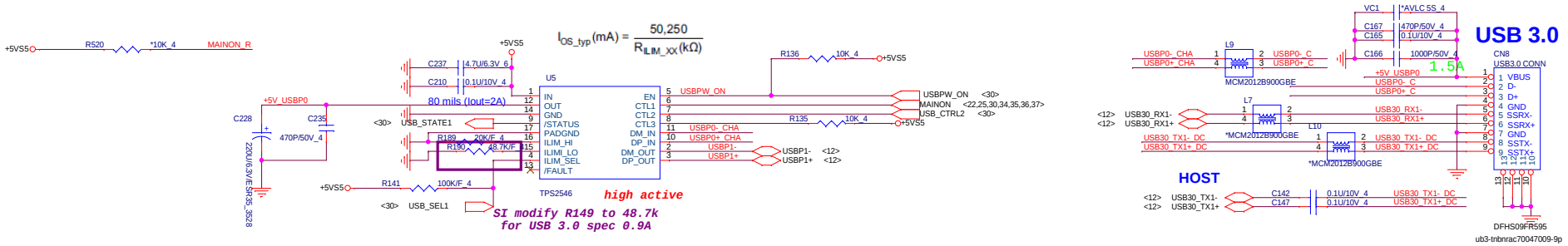
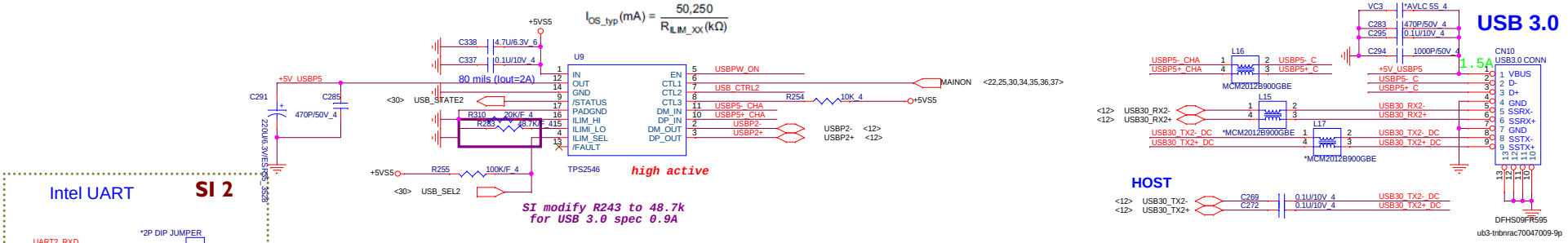
Right side USB 2.0/3.0 Combo

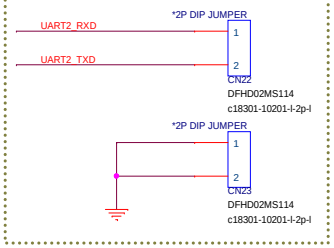
PV ADD R554/R555/R556 10k for USB 3.0 PU





Intel UART

SI 2



Left side USB 2.0/3.0 Combo

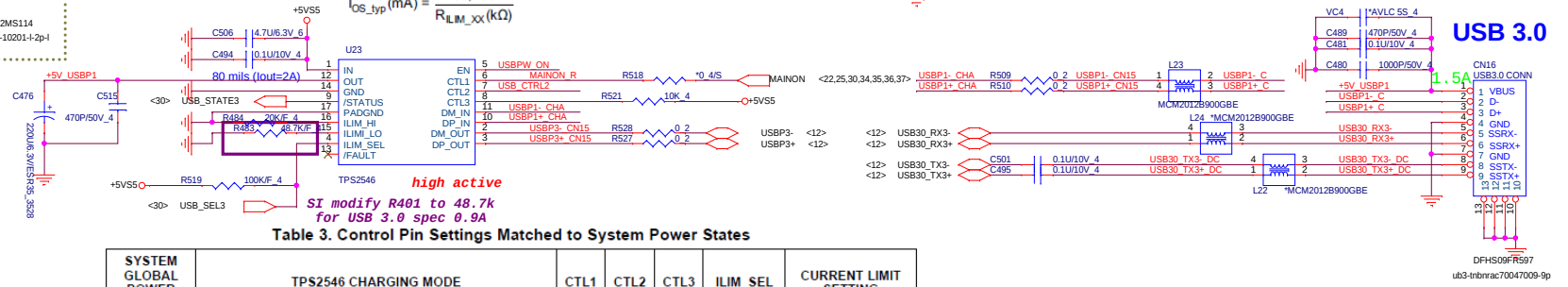


Table 3. Control Pin Settings Matched to System Power States

SYSTEM GLOBAL POWER STATE	TPS2546 CHARGING MODE	CTL1	CTL2	CTL3	ILIM_SEL	CURRENT LIMIT SETTING
S0	SDP1	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP2, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, load detection with ILIM_LO + 60mA thresholds or if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S4/S5	Auto mode, load detection with power wake thresholds	0	0	1	1	ILIM_HI
S3/S4/S5	Auto mode, no load detection	0	0	1	0	ILIM_HI
S3	Auto mode, keyboard/mouse wake up, load detection with ILIM_LO + 60 mA thresholds	0	1	1	1	ILIM_HI
S3	Auto mode, keyboard/mouse wake-up, no load detection	0	1	1	0	ILIM_HI
S3	SDP1, keyboard/mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

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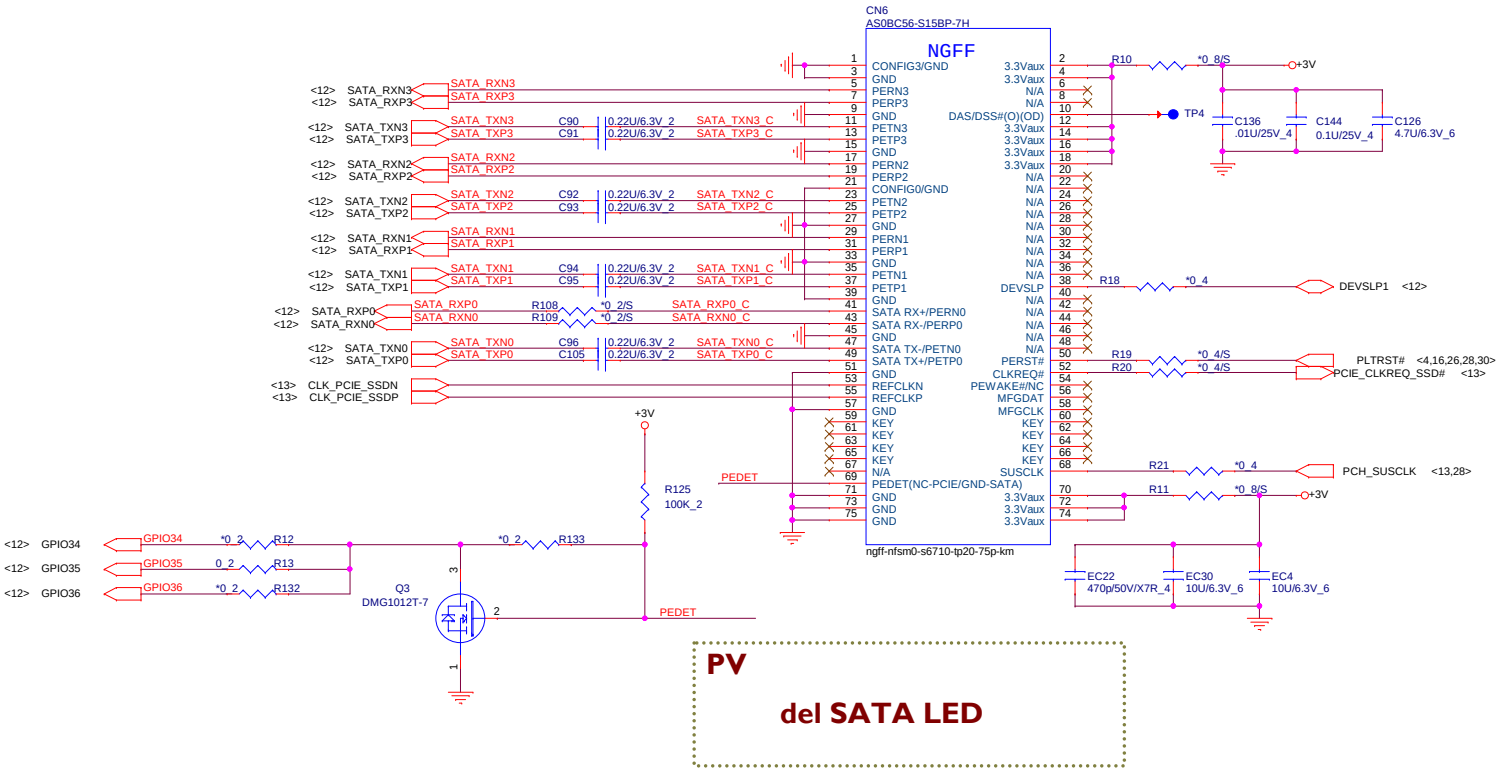
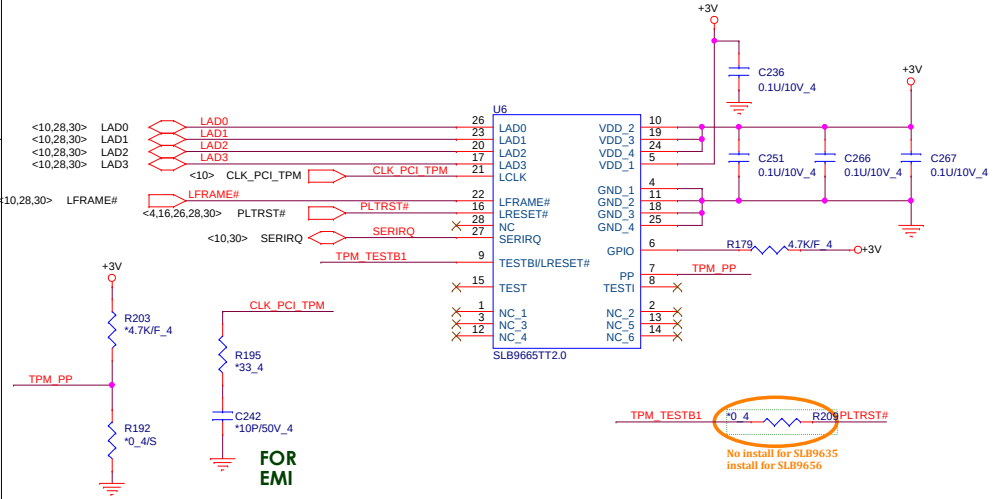


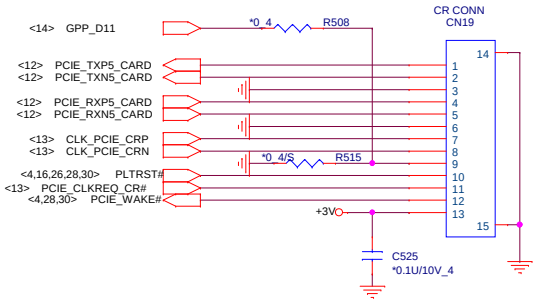
PV

del SATA LED

TPM (2.0)



Card Reader CON



<2,4,10,11,12,13,14,15,16,20,21,22,23,25,27,29,30,31,37,38> +3V
<22,23,24,27,37,38> +5V
<6,13,15,27,28,30,31,32,33,41> +3VPCU

NB5	**PROJECT : Y0DD** Quanta Computer Inc.	
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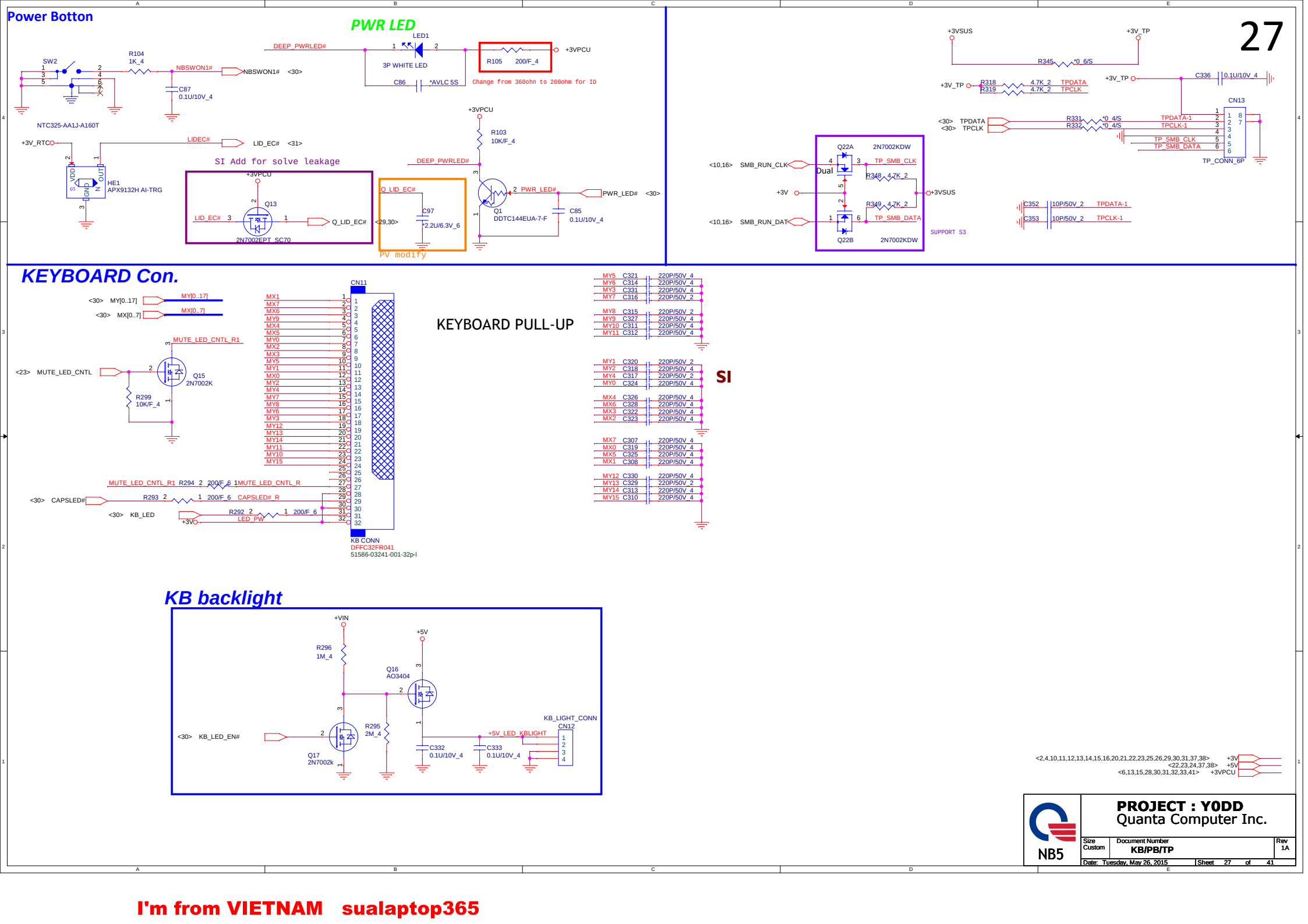

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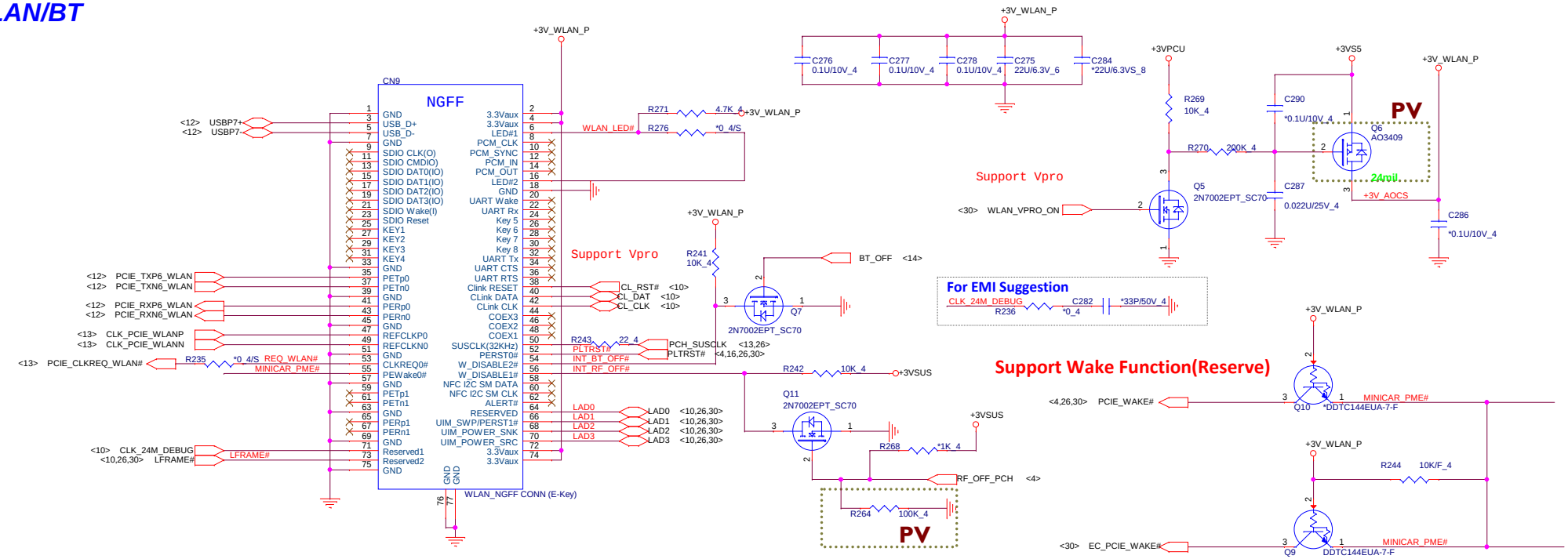
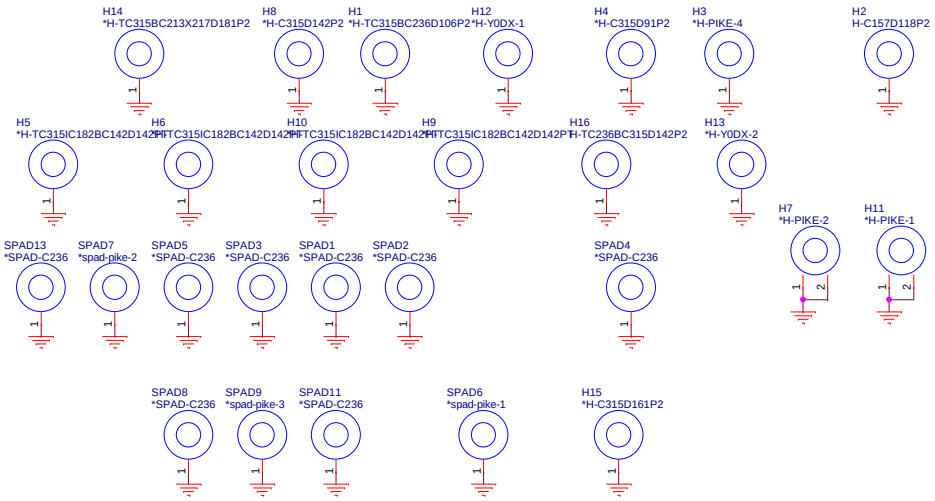
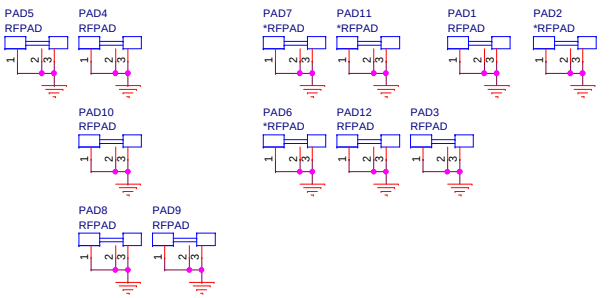
WLAN/BT



Hole



GND GUARD



<2,4,10,11,12,13,14,15,16,20,21,22,23,25,26,27,29,30,31,37,38> +3V
<22,23,24,27,37,38> +5V
<6,13,15,27,30,31,32,33,41> +3VPCU

NB5

PROJECT : Y0DD
Quanta Computer Inc.

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Accelerometer Sensor

Put it on MB side

Note: Place all capacitors close to IT8350.

20MIL

20MIL

20MIL

10MIL (For PLL Power)

U24
*IT8350E_LQFP-48

IT8350E
LQFP-48

Reserved SMBus channel 0 for debugging & updating FW

Reserved

SMbus channel 4 for connecting the Sensor (G-sensor)

Reserved TX/RX for debugging

if no use ADC function,
please pull down to GND

SMINTx for sensor interrupt

GPG2 can't floating

GPG2 Pull High Enable mirror function.
GPG2 Pull Low Disable mirror function.

To Sensor Hub SMBUS

External crystal is must be item when USB func. is used !

PV add for EC request

SM BUS
PWM
UART
A/D
SSPI
CLOCK
FSPI
USB
GPIO

Project	PROJECT : Y0DD Quanta Computer Inc.
Size / Custom	Document Number: SENSOR HUB
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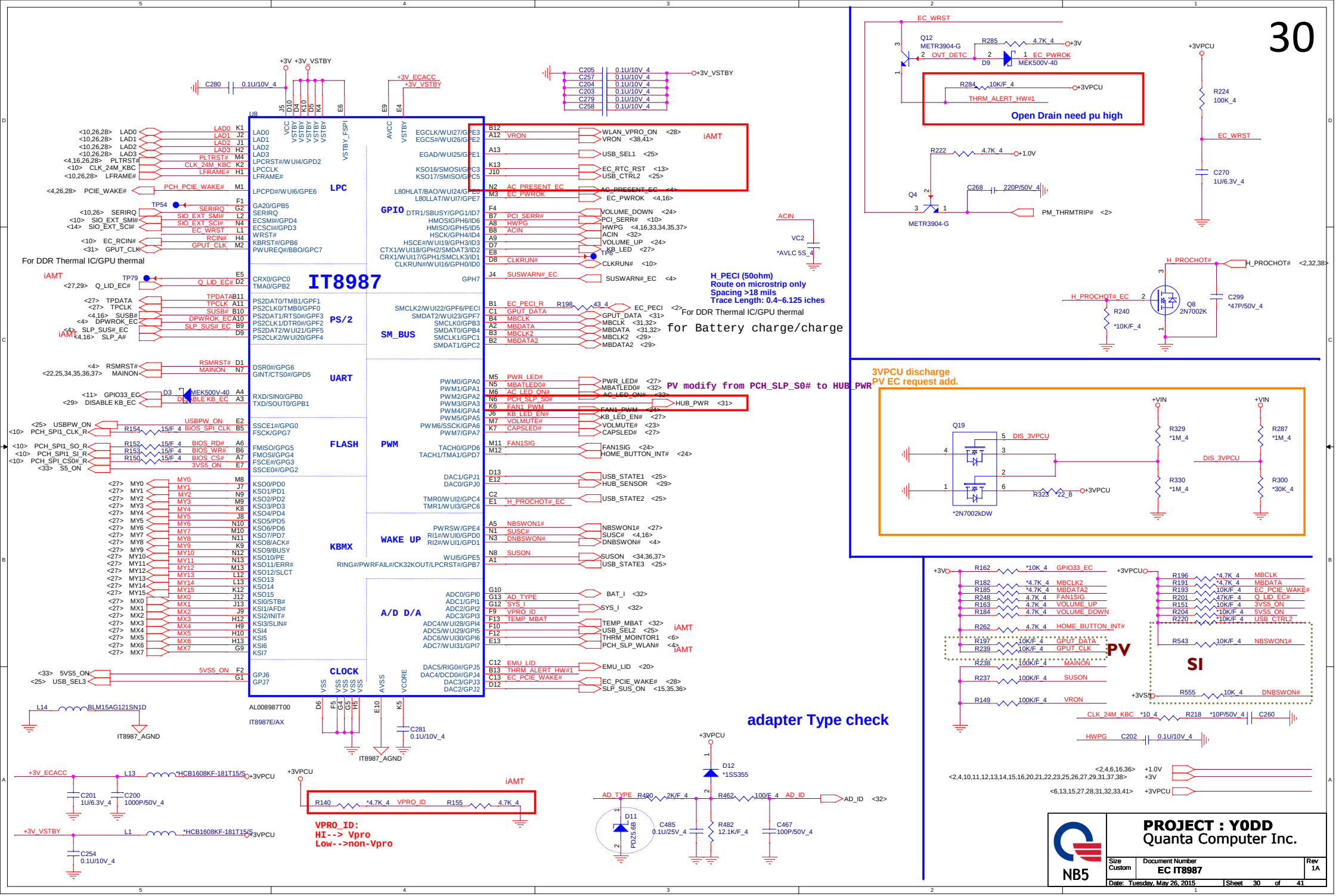
IT8987
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
iAMT
For DDR Thermal IC/GPU thermal
for Battery charge/charge
PV modify from PCH_SLP_S0# to HUB_PWR
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
adapter Type check
Open Drain need pu high
3VPCU discharge
PV EC request add.
PV
SI
PROJECT : Y0DD
Quanta Computer Inc.
NB5
Size Custom
Document Number
EC IT8987
Rev 1A
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VPRO_ID:
HI--> Vpro
Low-->non-Vpro
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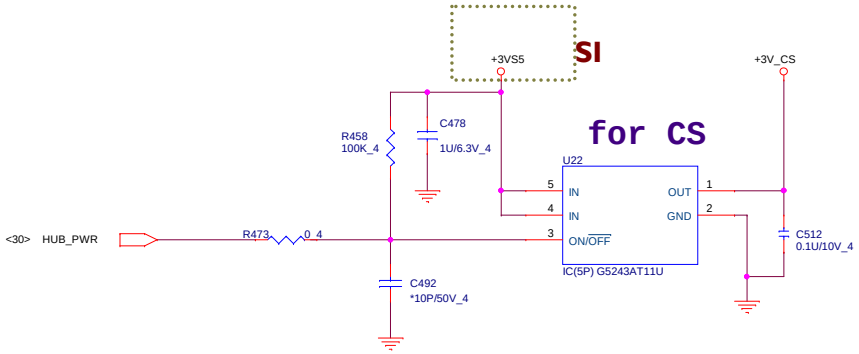

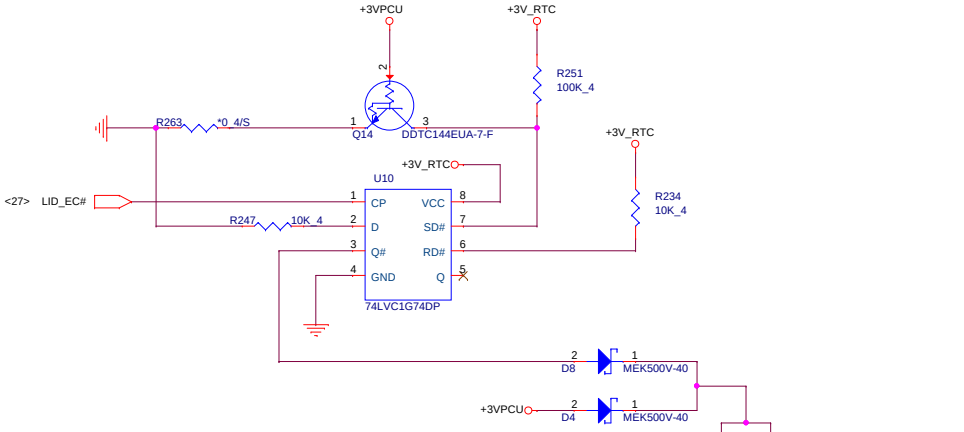

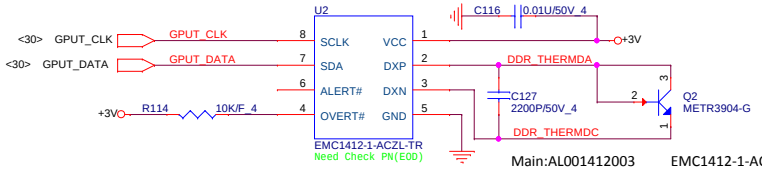

Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
2nd:AL000781039

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care.

Input				Output	
$\overline{SD}$	$\overline{RD}$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

[1] H = HIGH voltage level;
L = LOW voltage level;
↑ = LOW-to-HIGH CP transition;
Q_{n+1} = state after the next LOW-to-HIGH CP transition.

NB5

PROJECT : Y0DD
Quanta Computer Inc.

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Custom	CS	1A

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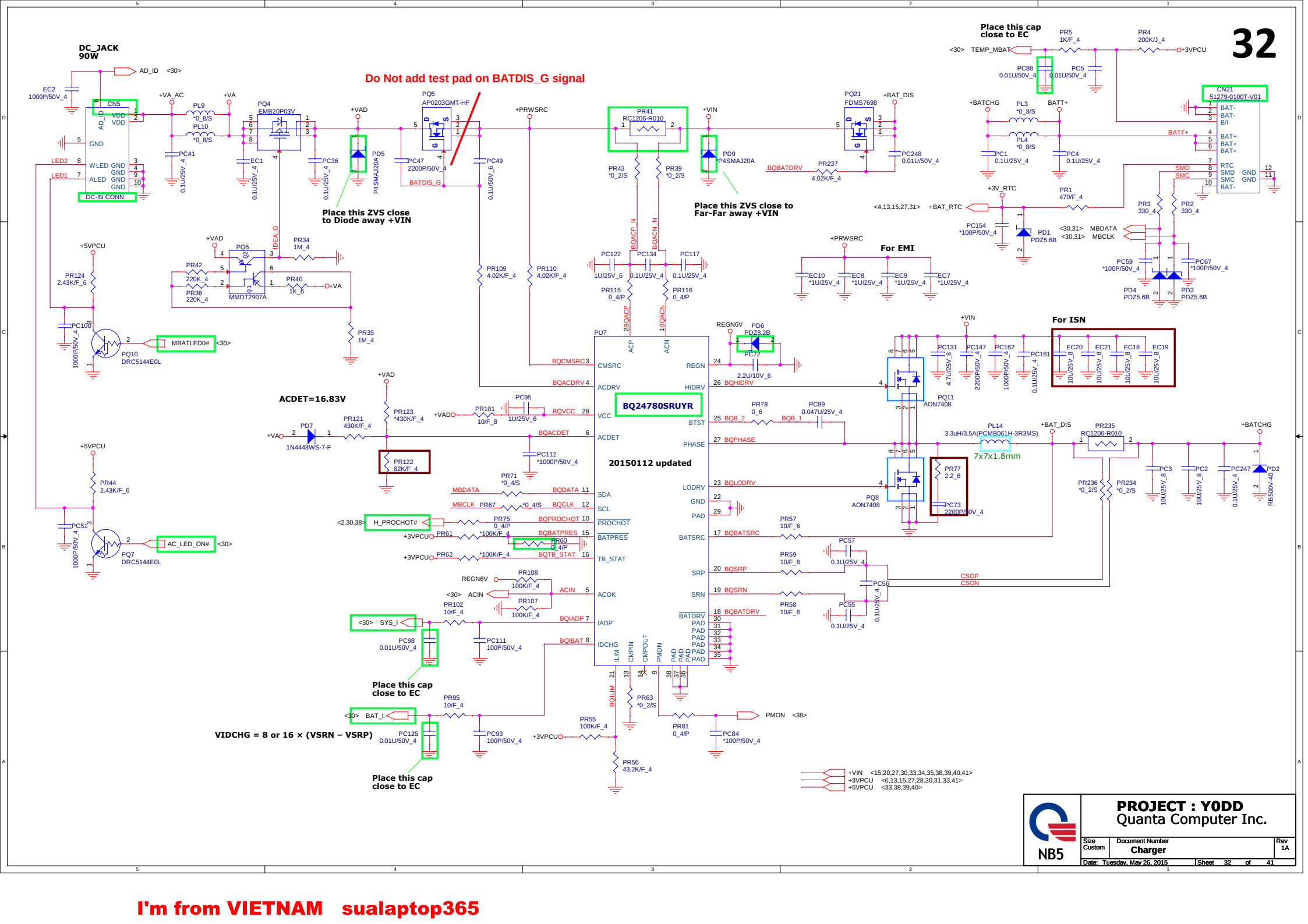
32
DC_JACK
90W
Do Not add test pad on BATDIS_G signal
Place this cap close to EC
Place this ZVS close to Diode away +VIN
Place this ZVS close to Far-Far away +VIN
For EMI
For ISN
ACDET=16.83V
BQ24780SRUYR
20150112 updated
VIDCHG = 8 or 16 × (VSRN – VSRP)
7x7x1.8mm
+VIN <15,20,27,30,33,34,35,38,39,40,41>
+3VPCU <6,13,15,27,28,30,31,33,41>
+5VPCU <33,38,39,40>
PROJECT : Y0DD
Quanta Computer Inc.
NB5
Charger
Tuesday, May 26, 2015
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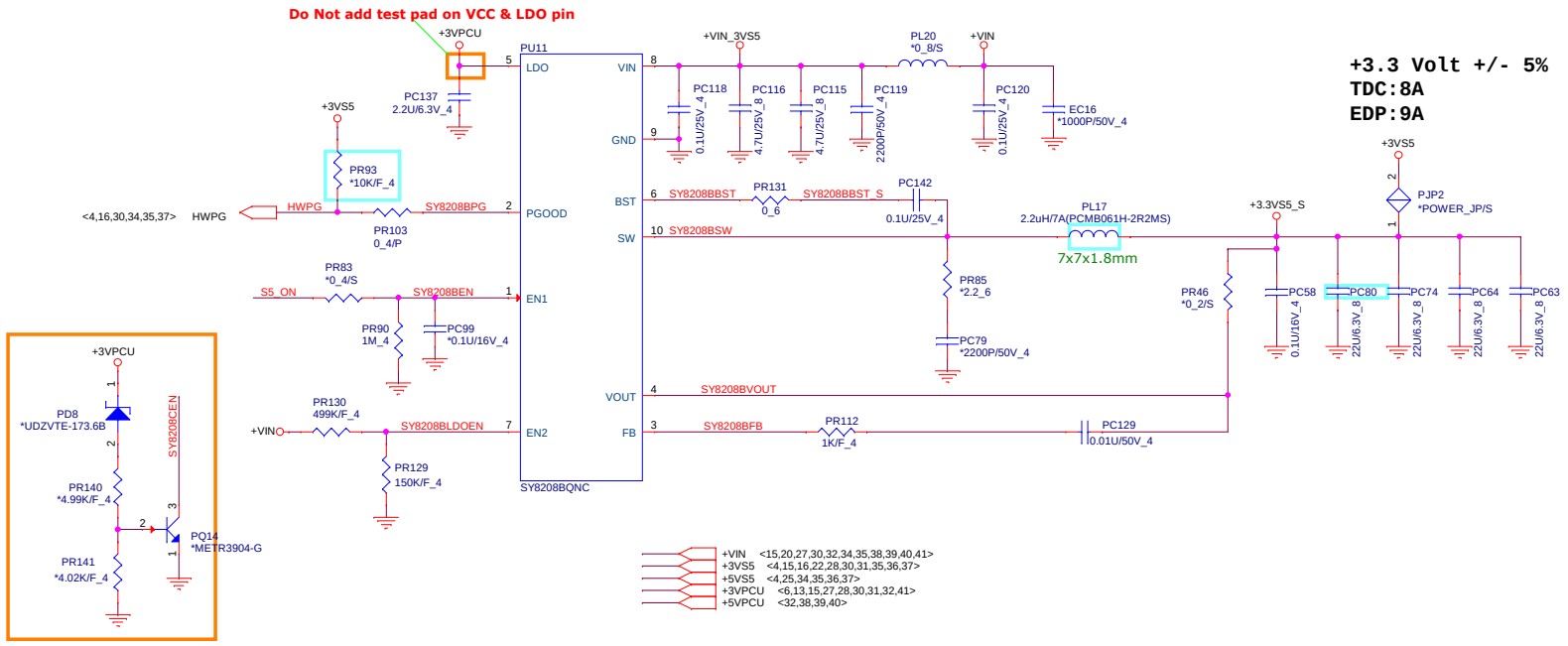

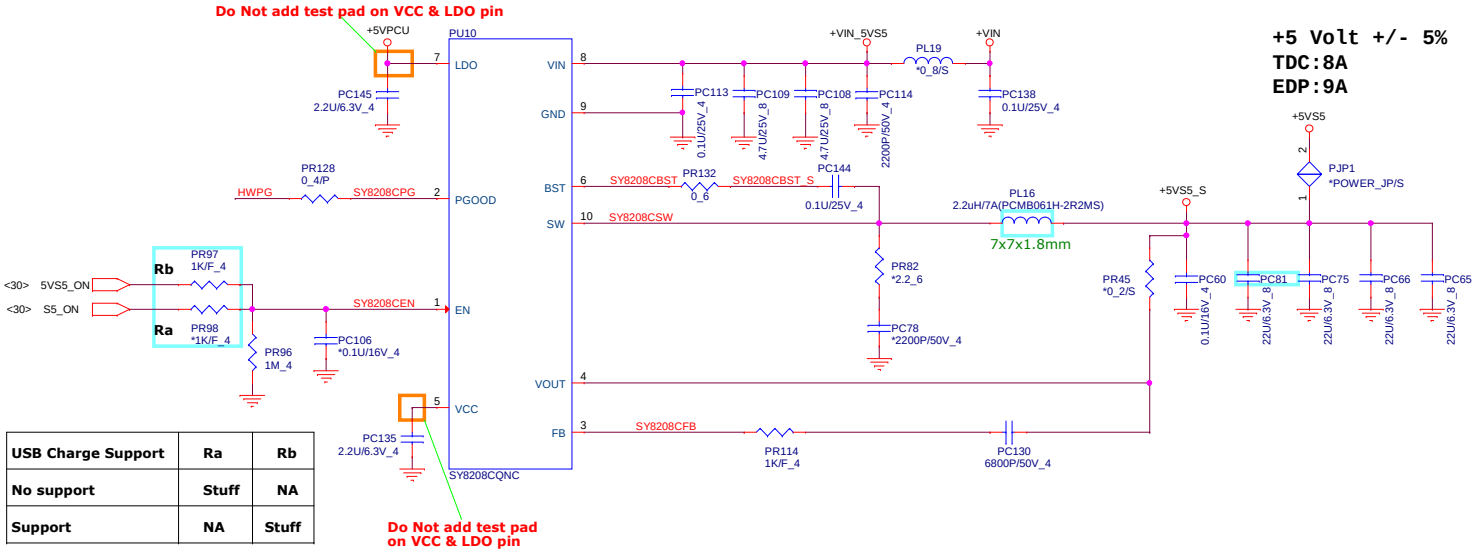

USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: 3/5S5	Rev: 1A
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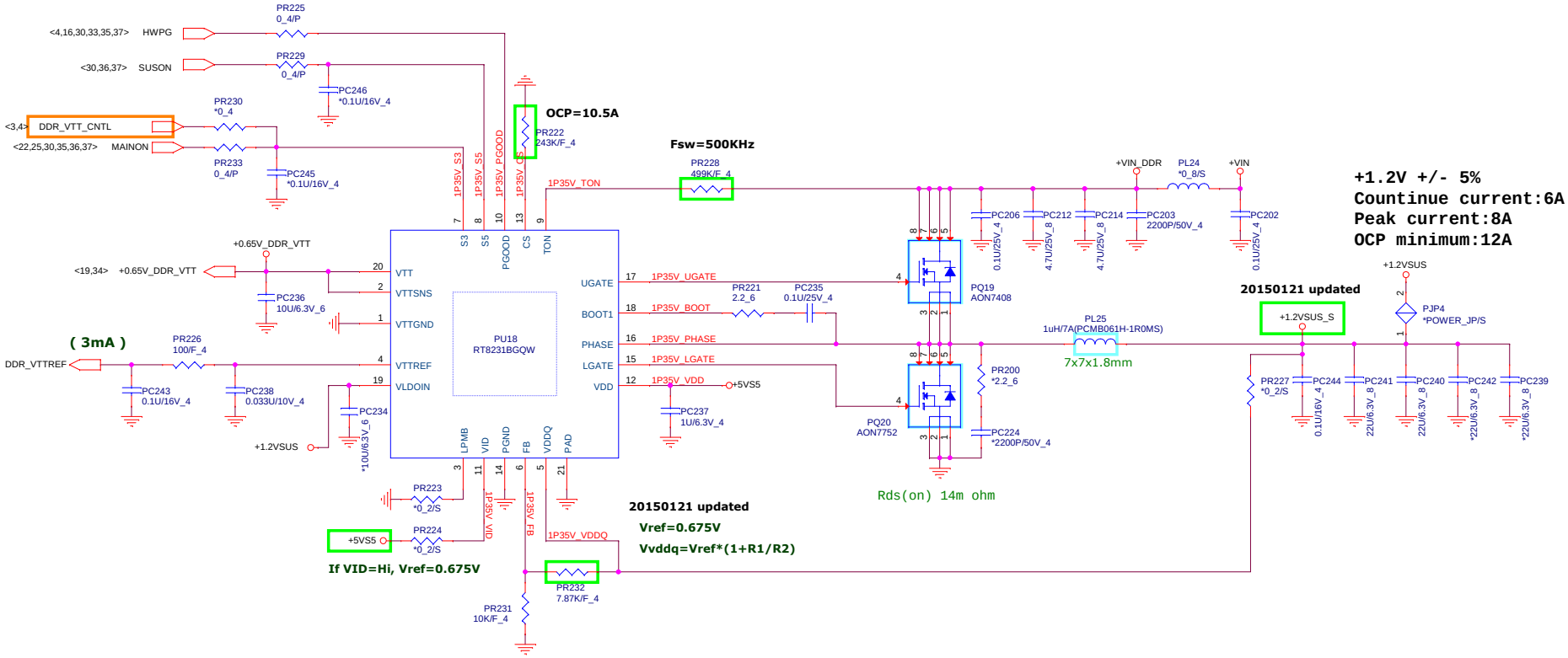
+VIN <15,20,27,30,32,33,35,38,39,40,41>
+5VS5 <4,25,33,35,36,37>
+1.2VSUS <3,6,17,18,36>
+0.65V_DDR_VTT <19,34>



NB5	**PROJECT : Y0DD** Quanta Computer Inc.	
Size: Custom	Document Number: DDR	Rev: 1A
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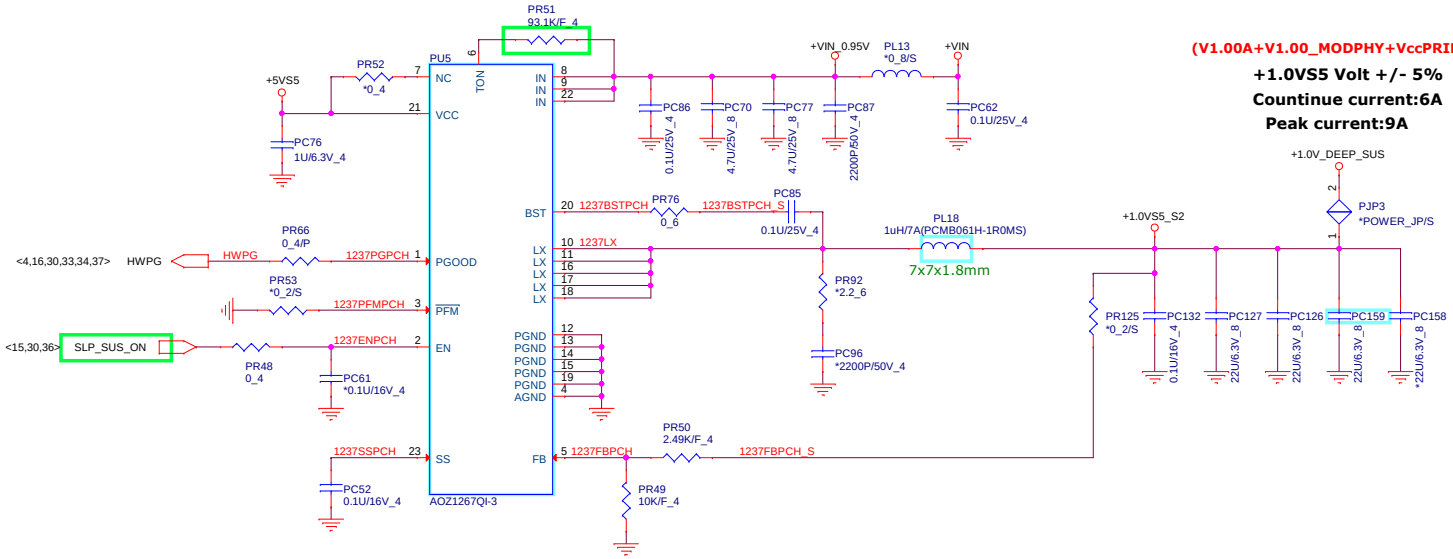
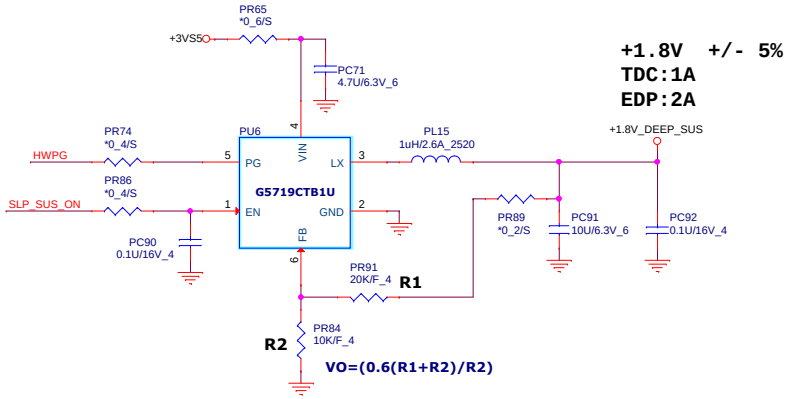
+VIN <15,20,27,30,32,33,34,38,39,40,41>
+3VS5 <4,15,16,22,28,30,31,33,36,37>
+5VS5 <4,25,33,34,36,37>
+1.0V_DEEP_SUS <9,13,15,16,36>
+1.8V_DEEP_SUS <9,15,37>



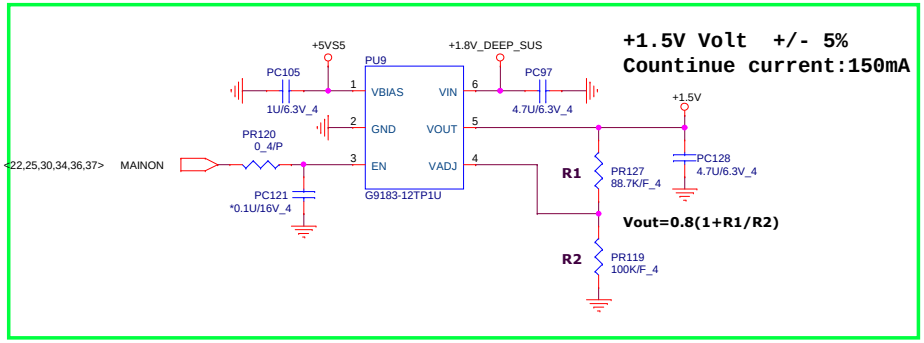
(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0VS5 Volt +/- 5%
Countinue current:6A
Peak current:9A



+1.8V +/- 5%
TDC:1A
EDP:2A

VO=(0.6(R1+R2)/R2)

20150116 updated



+1.5V Volt +/- 5%
Countinue current:150mA

Vout=0.8(1+R1/R2)

NB5	**PROJECT : Y0DD** Quanta Computer Inc.	
Size: Custom	Document Number: **+1.0/+1.5V/+1.8V_DEEP_SUS**	Rev: 1A
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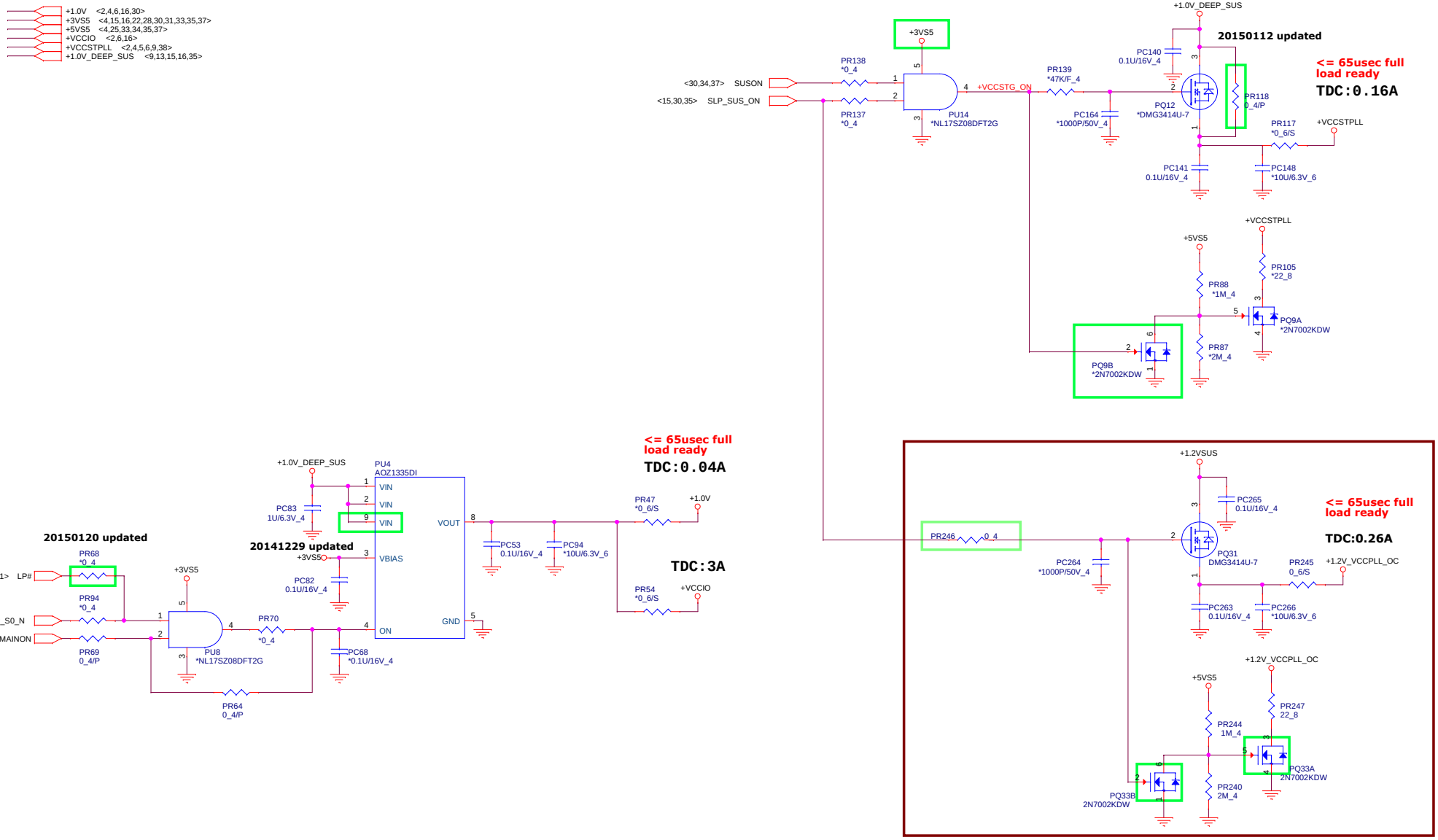

NB5	PROJECT : Y0DD Quanta Computer Inc.	
Size: Custom	Document Number: +1.0V/+VCCSTPLL	Rev: 1A
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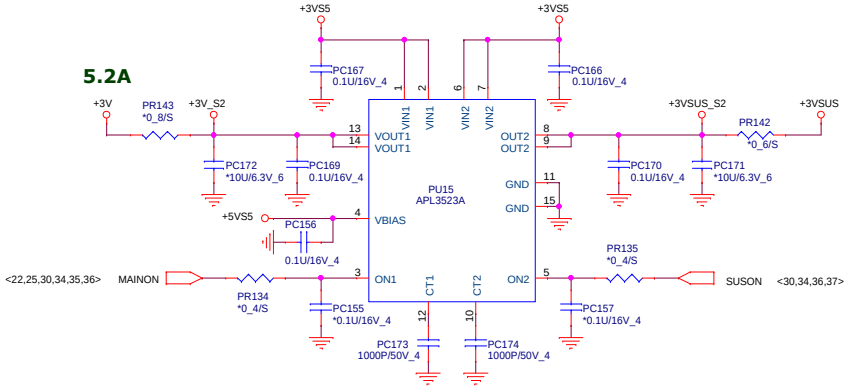
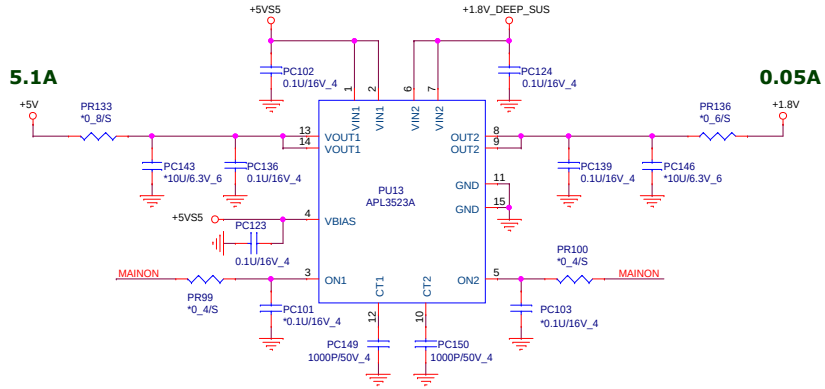
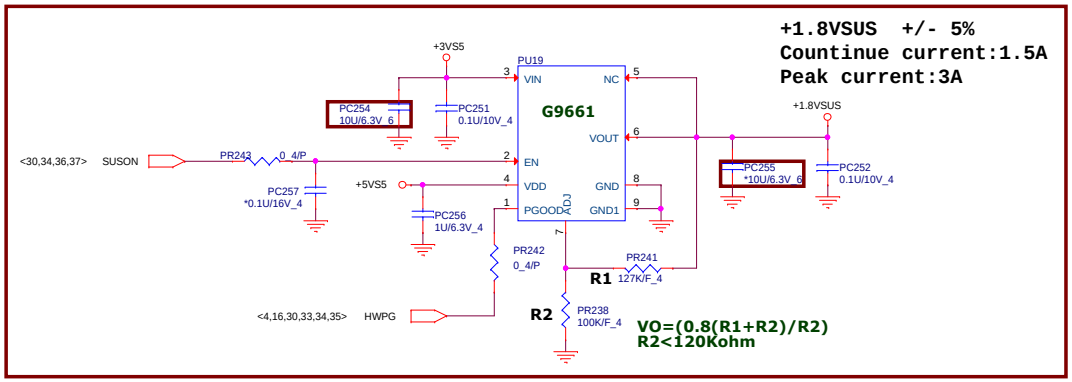
+3V <2,4,10,11,12,13,14,15,16,20,21,22,23,25,26,27,29,30,31,38>
+5V <22,23,24,27,37,38>
+3VS5 <4,15,16,22,28,30,31,33,35,36>
+5VS5 <4,25,33,34,35,36>
+3VSUS <27,28>
+1.8V_DEEP_SUS <9,15,35>
+1.8V <5,23>
+5V <22,23,24,27,37,38>
+VIN <15,20,27,30,32,33,34,35,38,39,40,41>
+1.8VSUS <17,18>







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NB5

PROJECT : Y0DD
Quanta Computer Inc.

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Custom	Load switch IC	1A

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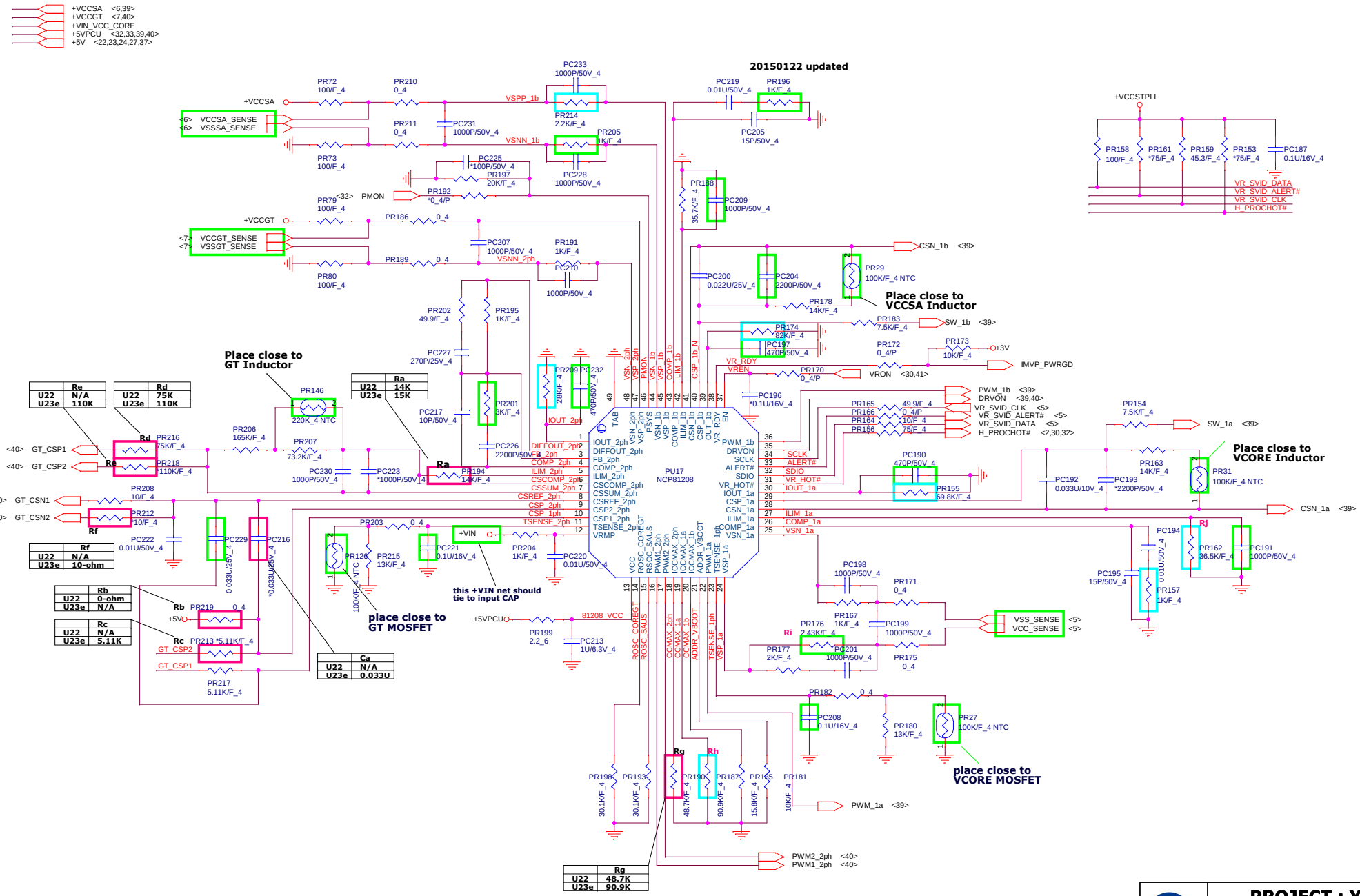

Re	
U22	N/A
U23e	110K

Rd	
U22	75K
U23e	110K

Ra	
U22	14K
U23e	15K

Rf	
U22	N/A
U23e	10-ohm

Rb	
U22	0-ohm
U23e	N/A

Rc	
U22	N/A
U23e	5.11K

Ca	
U22	N/A
U23e	0.033U

Rg	
U22	48.7K
U23e	90.9K

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU VR IC (NCP81208)	1A

NB5

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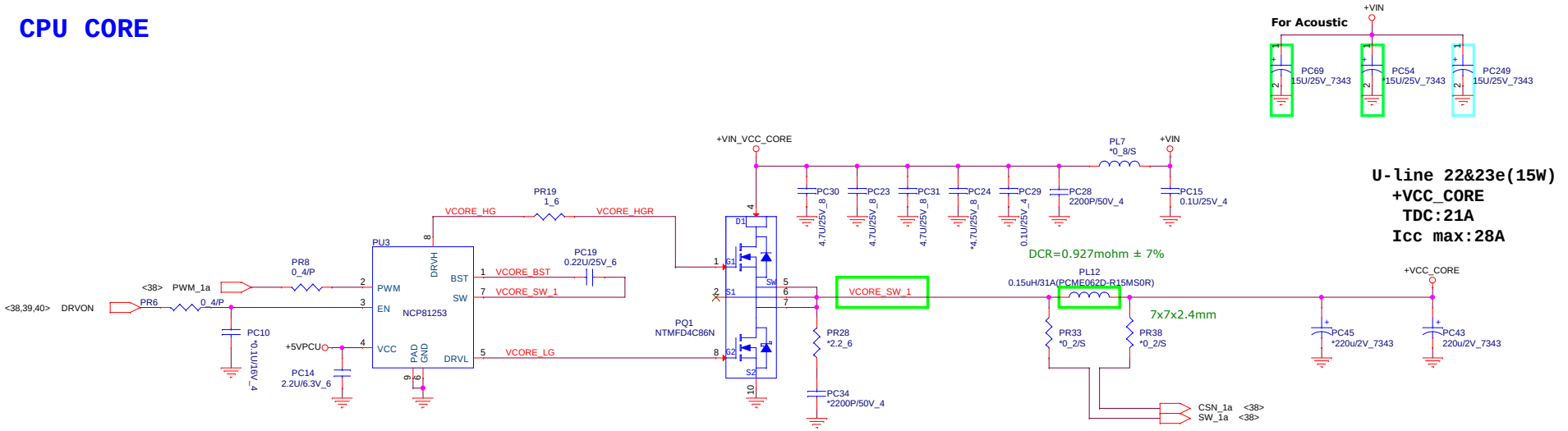
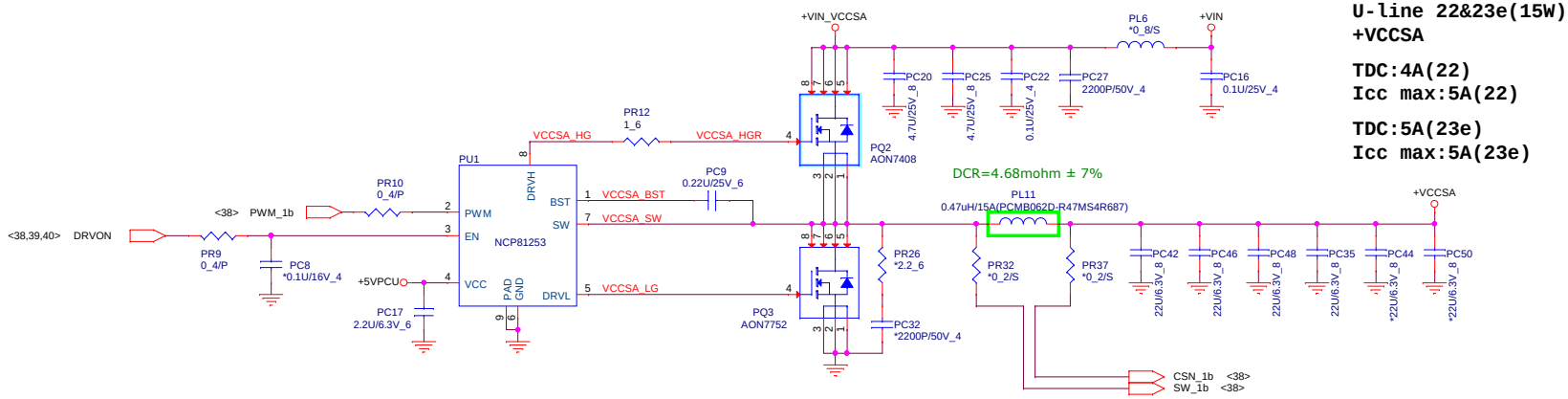
CPU CORE



VCCSA



NB5	**PROJECT : Y0DD** Quanta Computer Inc.	
Size: Custom	Document Number: +VCORE/VCCSA (NCP81253)	Rev: 1A
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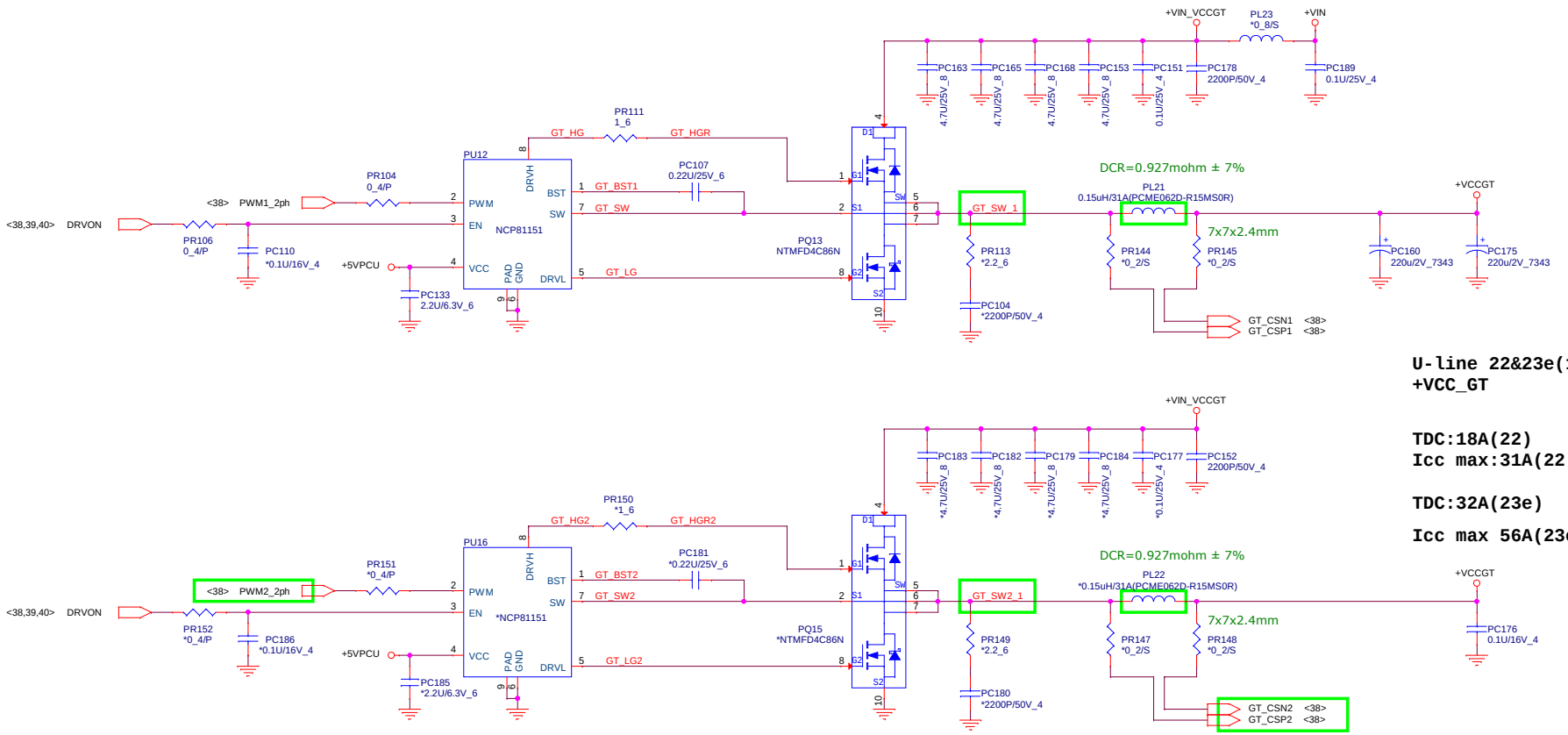
+VIN <15,20,27,30,32,33,34,35,38,39,41>
+VCCGT <7,38>
+VIN_VCC_CORE
+5VPCU <32,33,38,39>
+5V <22,23,24,27,37,38>



U-line 22&23e(15W)
+VCC_GT

TDC:18A(22)
Icc max:31A(22)

TDC:32A(23e)

Icc max 56A(23e)

NB5	**PROJECT : Y0DD** Quanta Computer Inc.	
Size: Custom	Document Number: **+VCCGT (NCP81151)**	Rev: 1A
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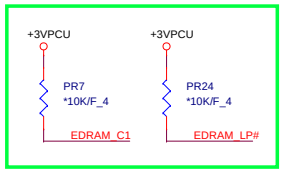

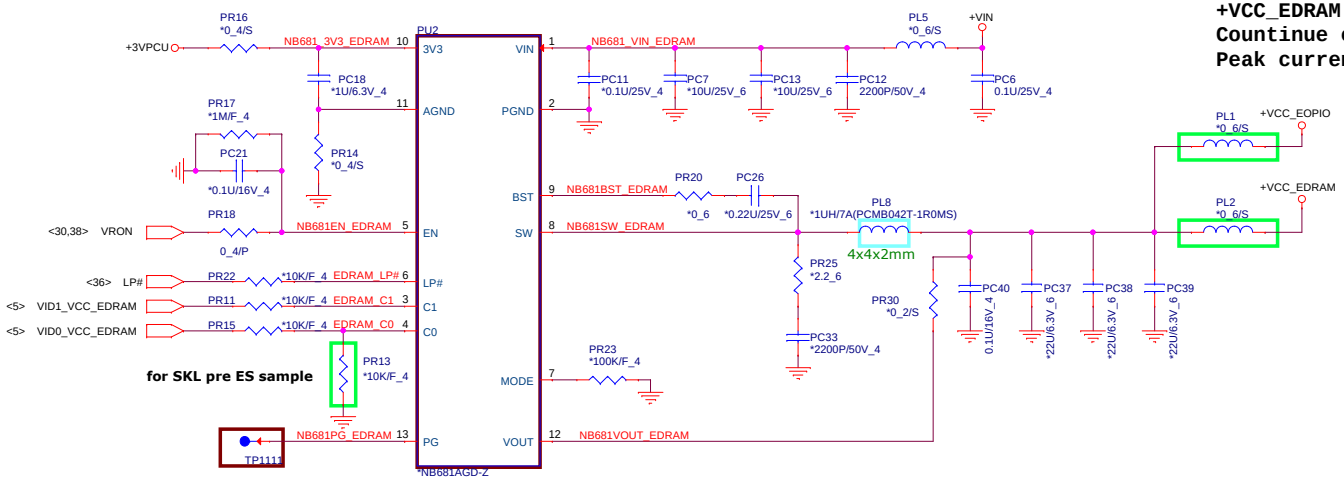

+VCC_EDRAM +/- 5%
Countinue current:4.5A
Peak current:6A

VCC_EDRAM

LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

MODE

	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K

NB5

PROJECT : Y0DD
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCC_EDRAM (NB681)_23E	1A

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