QL4 (15.6W) BLOCK DIAGRAM

01

PCB STACK UP

8L Dis. & UMA

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

DDRIII-SODIMM1 PAGE 12 — DDRIII 800/1066 MT/s, 1333MT/s CFD only

DDRIII-SODIMM2 PAGE 13 — DDRIII 800/1066 MT/s, 1333MT/s CFD only

CPU
Auburndale 35W
Clarksfield 45W
PAGE 3~6

27MHz

PCI-Express 16X

nVIDIA (40nm)
N10M-GE
N10P-GE
128 Bit
969p
PAGE 41~42

Switchable IC
PAGE 32~33

- HDMI CON PAGE 22
- CRT PAGE 22
- LCD CONN PAGE 21

DMI LINK

32.768KHz 25MHz

- SATA - HDD PAGE 31 — SATA0 150MB
- SATA - CD-ROM PAGE 31 — SATA1 150MB
- E-SATA PAGE 30 — SATA5 150MB

PCH
Ibex-M
PAGE 7~11

HDMI
CRT
LVDS

CLOCK GEN
9LRS3197
PAGE 2
14.318MHz

Mini PCI-E Card x2
Express Card x1
7,10,11

USB2.0

- 0,1,2 — USB2.0 Ports X3 PAGE 24
- 8 — BlueTooth PAGE 24
- 9 — Webcam PAGE 21
- 6 — RTS5159 PAGE 23

PCI-E

- X1 — Mini PCI-E Card — WWAN/TV PAGE 30
- X1 — LAN — Atheros PCIE-LAN AR8131(M) GagaLAN PAGE 26 — 25MHz — RJ45 PAGE 26
- X1 — Express Card PAGE 27

Azalia

Analog
ALC272
PAGE 24

- AUDIO Amplifier TPA6017A2 PAGE 25
  - microphone PAGE 24
  - Audio Jacks (Phone/ MIC) PAGE 24
  - Jack to Speaker PAGE 25

32.768KHz

Keyboard PAGE 28
Touch Pad PAGE 27

ENE KBC
KB3926 C0
PAGE 29

LPC

- GMT G9931P1U FAN PAGE 28
- SPI PAGE 29

ONFI

- Braidwood PAGE 31
- SPI PAGE 7
- MDC CONN PAGE 26

- UMA GPU CORE (RT8152A) PAGE 32
- SYSTEM POWER RT8206B PAGE 33
- VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204) PAGE 34
- CPU CORE ISL6288 PAGE 35
- VGACORE(1.025V) RT8208A PAGE 36
- DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 37
- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 39

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	E

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CLOCK GENERATOR

+1.05V — L23 HCB1608KF-181T15_6 — +VDDIO_CLK

C459 .1U/10V_4
C453 .1U/10V_4
C450 10U/6.3V_6S
C458 10U/6.3V_6S

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

U19 — RTM875N-632-GRT — QFN32

+3V
C451 4.7U/6.3V_6
C471 4.7U/6.3V_6
C452 .1U/10V_4
C454 .1U/10V_4
C470 .1U/10V_4
C469 .1U/10V_4
C464 .1U/10V_4

VDD_USB, VDD_LCD, VDD_SRC, VDD_CPU, VDD_REF
+VDDIO_CLK
VDD_CPU_IO, VDD_SRC_IO

[8,12,13,27,30] CGDAT_SMB
[8,12,13,27,30] CGCLK_SMB
SDATA, SCLK

[8] CLK_ICH_14M — R296 10K/F_4 — R300 33_4 — CPU_SEL
C465 10P/50V_4

CPU_STOP#, REF_0/CPU_SEL, CK_PWRGD_R, CK_PWRGD/PD#_3.3

XTAL_OUT, XTAL_IN — XOUT, XIN

VSS_SATA, VSS_USB, VSS_LCD

CPU-0, CPU-0#, CPU-1, CPU-1#
DOT96T_LPR, DOT96C_LPR
SRC-1, SRC-1#
SATA, SATA#
27MHz_nonSS, 27MHz_SS
GND, VSS_REF, VSS_CPU, VSS_SRC

CLK_BUF_BCLK_P [8]
CLK_BUF_BCLK_N [8]
133 or 100 Mhz output to PCH

CLK_BUF_DREFCLK [8]
CLK_BUF_DREFCLK# [8]
96Mhz output for generate 48Mhz (USB) and 24 Mhz (HDA)clk

CLK_BUF_PCIE_3GPLL [8]
CLK_BUF_PCIE_3GPLL# [8]
100Mhz output for DMI reference clk

CLK_BUF_DREFSSCLK [8]
CLK_BUF_DREFSSCLK# [8]
100Mhz output for SATA reference clk

CLK_VGA_27M_NONSS R308 33_4 → CLK_27M_NONSS [16]
CLK_VGA_27M_SS R309 33_4 → CLK_27M_SS [16]

Place the 33 ohm resistors close to the CK 505

Discrete and Hybrid

+3V — R295 1K/F_4 — CK_PWRGD_R — Q10 2N7002E — R297 100K/F_4
[37] VR_PWRGD_CLKEN#

Y3 14.318MHZ
XTAL_IN — C461 33P/50V_4
XTAL_OUT — C457 33P/50V_4

+3V — R303 *10K/F_4 — CPU_SEL — R306 10K/F_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

CPU bracket Hole.

H5 *h-tc295c220d161p2
H6 *h-tc295c220d161p2
H10 *h-tc295c220d161p2
H11 *h-tc295c220d161p2

B-stage change

VGA bracket Hole.

H8 *h-tc295c220d161p2
H12 *h-tc295c220d161p2
H13 *h-tc295c220d161p2

B-stage change

PAD and HOLE

H1 *h-ql4-1
H7 *h-c315d106p2
H2 *h-c315d106p2
H22 *h-ql4-3
H25 *H-C315D106P2
H15 *h-c315d106p2
H16 *h-c315d106p2
H18 *H-HC130bc197d130pb
H14 *O-O236X669D236X669N
H17 *h-tc421x335bc315d106p2
H23 *h-c315d106p2
H4 *H-C315D106P2
H9 *h-ql4-2
H3 *H-C315D130P2
H24 *H-TC130BC197D130PB

PAD2 MDC_SPRING
PAD1 MDC_SPRING
PAD3 *EMI_PAD
PAD4 *EMI_PAD
PAD5 *EMI_PAD
PAD6 *EMI_PAD
PAD7 *EMI_PAD
PAD8 *EMI_PAD

MINI CARD Hole.

H26 *h-t67bc276d67p2
H30 *H-TC161BC276D161P2
H27 *H-TC161BC276D161P2
H29 *h-t67bc276d67p2
H28 *h-t67bc276d67p2
H20 *H-TC161BC276D161P2

H31 *EMIPAD236X591B
H32 *emipad6472x1220
H33 *emipad236x591b

[7,8,9,11,29,34,36,42] +1.05V
[3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V

MDC Hole.

H21 *h-tc146bc256d146p2
H19 *h-tc146bc256d146p2

EMI solution.

B-stage change

C773 .1U/25V_4 — +VIN
C966 .1U/25V_4 — +VIN
LAN_AGND1 — R796 0_4

NB5

PROJECT : QL4
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Custom	CLOCK & Screw Holes	E
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	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

U29A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R1P0

2.7GT/s data rate

U29B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

PV 0616 DEL debug Con.

For ITP CLk

JTAG MAPPING

Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89

Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

NB5

PROJECT : QL4
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Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	E

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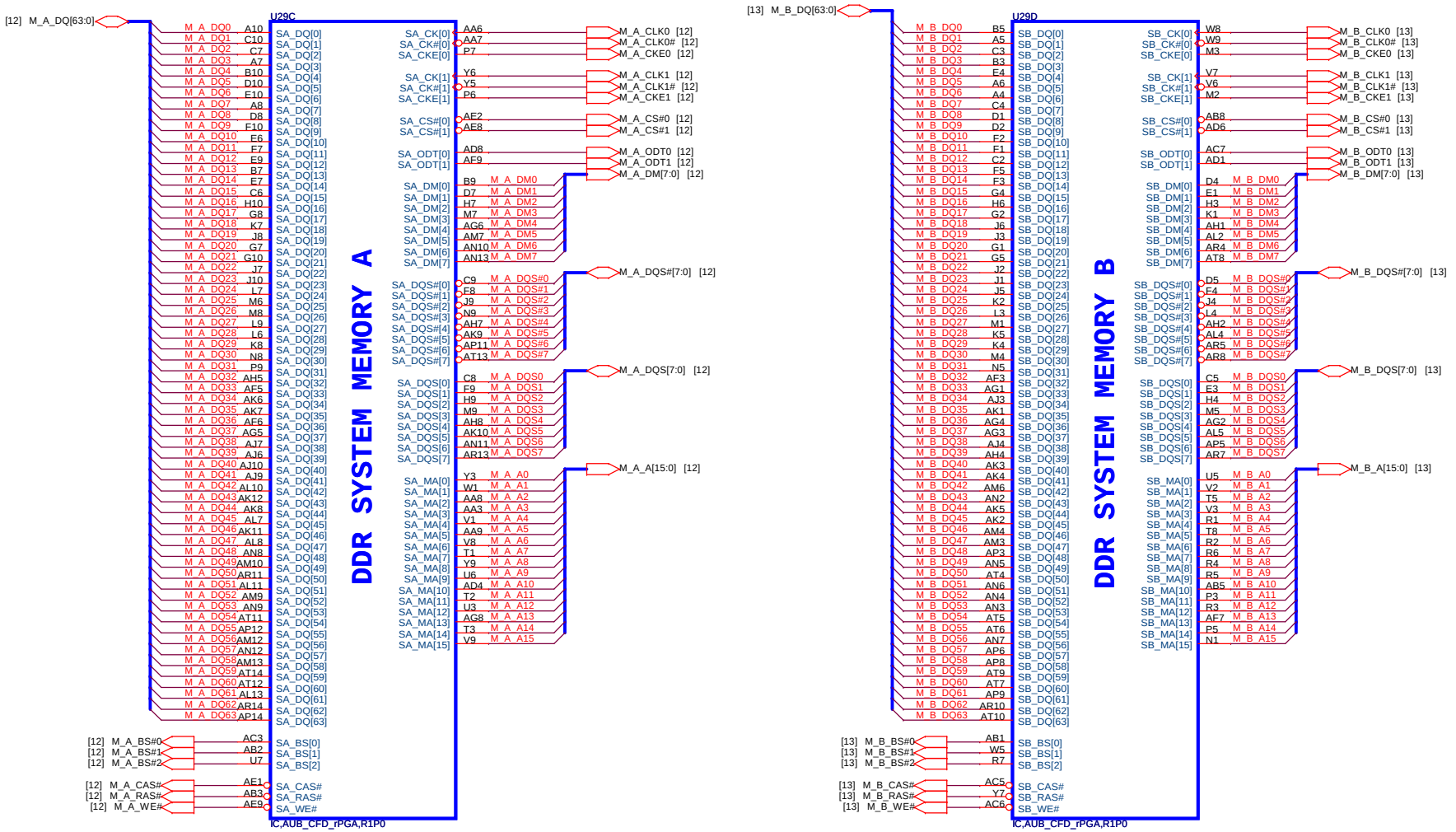
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	E

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	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

U29F

CPU CORE SUPPLY POWER

1.1V RAIL POWER

CPU VIDS

SENSE LINES

IC,AUB_CFD_rPGA,R1P0

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

	DIS	UMA
Ra	0 ohm	NA

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

U29G

POWER

GRAPHICS

SENSE LINES

GRAPHICS VIDS

DDR3 - 1.5V RAILS

FDI & DMI

1.1V

1.8V

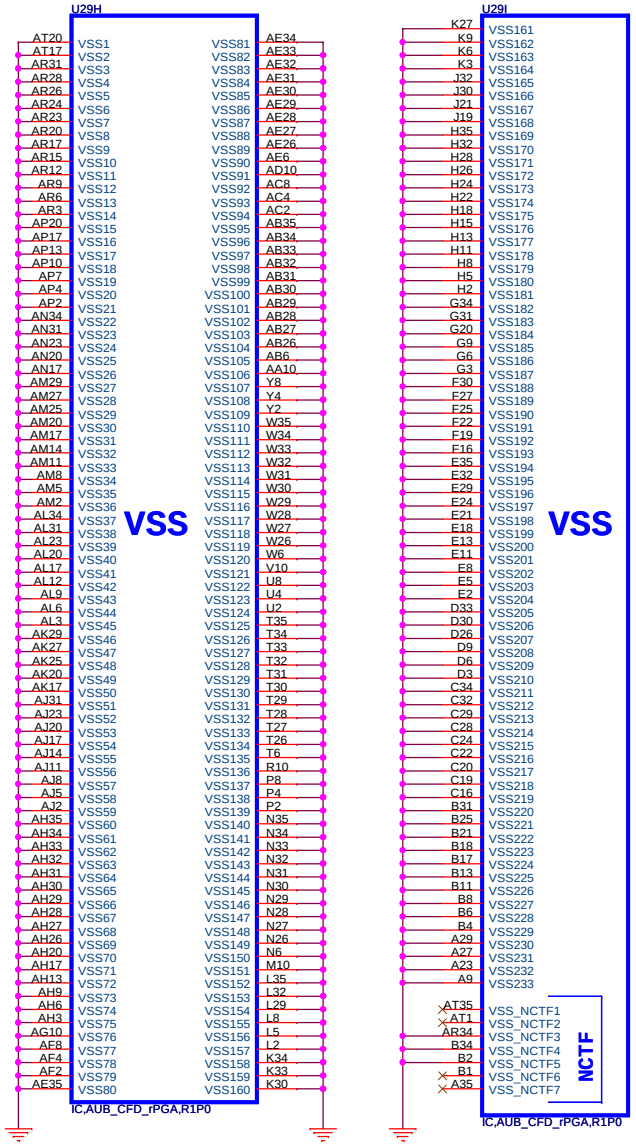
IC,AUB_CFD_rPGA,R1P0

PROJECT : QL4
Quanta Computer Inc.

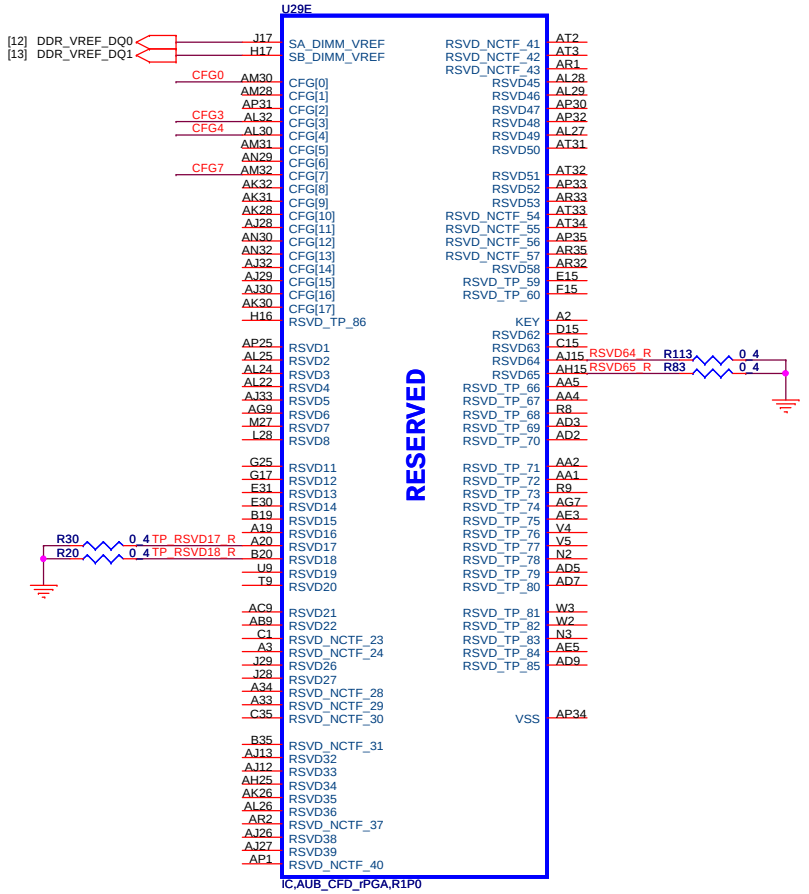
NB5

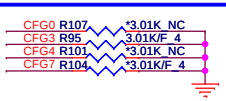
Size: Custom
Document Number: PROCESSER 3/4(POWER)
Rev: E
Date: Friday, October 09, 2009
Sheet 5 of 44

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)





For Discrete only

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	E

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INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U35A

Ibex-M 1 OF 10

RTC
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN

LPC
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
(+3V) LDRQ1# / GPIO23
SERIRQ

IHDA
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33 (+3V)
HDA_DOCK_RST# / GPIO13 (+3V_S5)

SATA
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED#
(+3V) SATA0GP / GPIO21
(+3V_S5) SATA1GP / GPIO19

JTAG
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#

SPI
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO

IbexPeak-M_Rev1_0

12PF/50V_4 C667
Y5 32.768KHZ
R492 10M_4
C665 12PF/50V_4
RTC_X1 B13
RTC_X2 D13
RTC_RST# C14
SRTC_RST# D17
SM_INTRUDER# A16
+RTC_CELL R497 330K_6 PCH_INVRMEN A14
ACZ_BCLK A30
ACZ_SYNC D29
[10,24] SPKR P1
ACZ_RST# C30
[24] ACZ_SDIN0 G30
[25] ACZ_SDIN1 F30
E32
F32
ACZ_SDOUT B29
[10] PCH_GPIO33 H32
J30
R248 51_4
TP40 PCH_JTAG_TCK_BUF M3
TP37 PCH_JTAG_TMS K3
TP43 PCH_JTAG_TDI K1
TP42 PCH_JTAG_TDO J2
TP41 PCH_JTAG_RST# J4
must add test point.
SPI_CLK_R BA2
SPI_CS0#_R AV3
TP38 SPI_CS1# AY3
SPI_SI_R AY1
SPI_SO AV1

FWH0 / LAD0 D33
FWH1 / LAD1 B33
FWH2 / LAD2 C32
FWH3 / LAD3 A32
FWH4 / LFRAME# C34
LDRQ0# A34
(+3V) LDRQ1# / GPIO23 F34
SERIRQ AB9
R255 10K/F_4 +3V

SATA HDD1
SATA0RXN AK7
SATA0RXP AK6
SATA0TXN AK11
SATA0TXP AK9
SATA_RXN0_C [27]
SATA_RXP0_C [27]
SATA_TXN0 [27]
SATA_TXP0 [27]

SATA1RXN AH6
SATA1RXP AH5
SATA1TXN AH9
SATA1TXP AH8
SATA_RXN1_C [27]
SATA_RXP1_C [27]
SATA_TXN1 [27]
SATA_TXP1 [27]

SATA ODD
Port2 and Port3 HM55 not support

E-SATA
SATA2RXN AF11
SATA2RXP AF9
SATA2TXN AE7
SATA2TXP AF6
SATA_RXN5_C [28]
SATA_RXP5_C [28]
SATA_TXN5 [28]
SATA_TXP5 [28]

SATAICOMPO AF16
SATAICOMPI AF15
SATA_COMP R213 37.4/F_4
+1.05V [16,22,32] CRT_B
SATALED# T3
SATA_LED# [25]
Y9 SATA_DET0#
V1 SATA_DET1#

Stuff on Hybrid and UMA
+3V
R783 *2.2K_4 EDIDCLK_PCH
R785 *2.2K_4 EDIDDATA_PCH

UMA and Hybird_LVDS & CRT signals
[17,21,32] LVDS_BLON
[17,21,32] DISP_ON
[17,21,32] DPST_PWM
[17,21,32] EDIDCLK
[17,21,32] EDIDDATA
No stuff on Hybrid
+3V
R181 *0_4 LVDS_BLON_PCH
R168 *0_4 DISP_ON_PCH
R182 *0_4 DPST_PWM_PCH
R183 *0_4 EDIDCLK_PCH
R139 *0_4 EDIDDATA_PCH
R170 *10K/F_4 L_CTRL_CLK
R169 *10K/F_4 L_CTRL_DATA
R176 *2.37K/F_4 LVDS_IBG
LVDS_VBG
TP3

IBEX PEAK-M (LVDS,DDI)

U35D

Ibex-M 4 OF 10

SDVO
SDVO_TVCLKINN
SDVO_TVCLKINP
SDVO_STALLN
SDVO_STALLP
SDVO_INTN
SDVO_INTP
SDVO_CTRLCLK
SDVO_CTRLDATA

Digital Display Interface
DISPLAY PORT B
DDPB_AUXN
DDPB_AUXP
DDPB_HPD
DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P

DISPLAY PORT C
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPC_AUXN
DDPC_AUXP
DDPC_HPD
DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P

DISPLAY PORT D
DDPD_CTRLCLK
DDPD_CTRLDATA
DDPD_AUXN
DDPD_AUXP
DDPD_HPD
DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P

LVDS--A
L_BKLTEN
L_VDD_EN
L_BKLTCTL
L_DDC_CLK
L_DDC_DATA
L_CTRL_CLK
L_CTRL_DATA
L_IBG
L_VBG
L_VREFH
L_VREFL
LVDSA_CLK#
LVDSA_CLK
LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3

LVDS--B
LVDSB_CLK#
LVDSB_CLK
LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA#3
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3

CRT
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
DAC_IREF
CRT_IRTN

IbexPeak-M_Rev1_0

[21,32] LA_CLK#
[21,32] LA_CLK
[21,32] LA_DATAN0
[21,32] LA_DATAN1
[21,32] LA_DATAN2
[21,32] LA_DATAP0
[21,32] LA_DATAP1
[21,32] LA_DATAP2
[21,32] LB_CLK#
[21,32] LB_CLK
[21,32] LB_DATAN0
[21,32] LB_DATAN1
[21,32] LB_DATAN2
[21,32] LB_DATAP0
[21,32] LB_DATAP1
[21,32] LB_DATAP2
No stuff on Hybrid
R399 *0_4 CRT_B_PCH
R400 *0_4 CRT_G_PCH
R401 *0_4 CRT_R_PCH
R396 *0_4 DDCCLK_PCH
R397 *0_4 DDCDATA_PCH
[16,22,32] CRT_G
[16,22,32] CRT_R
[16,22,32] DDCCLK
[16,22,32] DDCDATA
[16,22,32] HSYNC_COM
[16,22,32] VSYNC_COM
R167 *0_4 HSYNC_PCH
R191 *0_4 VSYNC_PCH
R448 *0_4 CRT_B_1
R449 *0_4 CRT_G_1
R453 *0_4 CRT_R_1
R446 *0_4 DDCCLK_INT
R447 *0_4 DDCDATA_INT
R454 *150/F_4
R455 *150/F_4
R452 *150/F_4
R147 *0_4 HSYNC
R141 *0_4 VSYNC
R154 1K/F_4 DAC_IREF

[32] LVDS_BLON_PCH
[32] DISP_ON_PCH
[32] DPST_PWM_PCH
[32] EDIDCLK_PCH
[32] EDIDDATA_PCH
[32] CRT_B_PCH
[32] CRT_G_PCH
[32] CRT_R_PCH
[32] DDCCLK_PCH
[32] DDCDATA_PCH
[32] HSYNC_PCH
[32] VSYNC_PCH

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.
+3V
R557 10K/F_4 SATA_LED#
R270 *10K/F_4 SATA_DET0#
R559 *10K/F_4 SATA_DET1#
R274 10K/F_4
R632 10K/F_4

UMA HDMI signals
+3V
Q4 *2N7002K
DPB_HPD_Q
HDMI_HPD_CON [33]
R159 *100K_4
R158 *0_4

DPB_CTRL_CLK R444 *0_4 SDVO_CLK [33]
DPB_CTRL_DATA R445 *0_4 SDVO_DATA [33]
DPB_LANE0_N C291 *.1U/10V_4 IN_D2# [33]
DPB_LANE0_P C324 *.1U/10V_4 IN_D2 [33]
DPB_LANE1_N C630 *.1U/10V_4 IN_D1# [33]
DPB_LANE1_P C633 *.1U/10V_4 IN_D1 [33]
DPB_LANE2_N C325 *.1U/10V_4 IN_D0# [33]
DPB_LANE2_P C328 *.1U/10V_4 IN_D0 [33]
DPB_LANE3_N C335 *.1U/10V_4 IN_CLK# [33]
DPB_LANE3_P C331 *.1U/10V_4 IN_CLK [33]

For AUDIO
[24] ACZ_RST#_AUDIO
[24] ACZ_SDOUT_AUDIO
[24] ACZ_SYNC_AUDIO
[24] BIT_CLK_AUDIO
R462 33_4 ACZ_RST#
R467 33_4 ACZ_SDOUT
C641 *10P/50V_4
R477 33_4 ACZ_SYNC
C656 *10P/50V_4
R192 33_4 ACZ_BCLK
C339 10P/50V_4
PV 0616

For MDC
[25] ACZ_RST#_MDC
[25] ACZ_SDOUT_MDC
[25] ACZ_SYNC_MDC
[25] BIT_CLK_MDC
R465 33_4 ACZ_RST#
R469 33_4 ACZ_SDOUT
C645 *10P/50V_4
R474 33_4 ACZ_SYNC
C652 *10P/50V_4
R198 33_4 ACZ_BCLK
C347 *10P/50V_4

RTC

+RTC_CELL
+3VPCU
RB500V-40 D27
+3VRTC_2
RB500V-40 D26
C655 1U/6.3V_4
R482 20K/F_4 RTC_RST#
C660 1U/6.3V_4
G2 *SHORT_PAD1
R487 20K/F_4 SRTC_RST#
C664 1U/6.3V_4
G3 *SHORT_PAD1
R476 1M_4 SM_INTRUDER#
R489 1K/F_4 +3VRTC_1
BT1
BAT_CONN

2M byte SPI ROM for ME

U40
+3V
SPI_HOLD#
R568 10K/F_4
C440 .1U/10V_4
VDD CE# SCK SI HOLD# SO VSS WP#
SPI_CS0# R538 short0402*0_4/S SPI_CS0#_R
SPI_CLK R564 short0402*0_4/S SPI_CLK_R
SPI_SI R563 short0402*0_4/S SPI_SI_R
SPI_SO_R R539 short0402*0_4/S SPI_SO
SPI_WP# R540 10K/F_4 +3V
2M SPI ROM
AKE38FP0Z00
X6179-10XXXX-8P-SOCKET

2M byte SPI ROM for ME
MXIC: AKE38FP0Z00
WINBOND: AKE38FP0N01
AIT: AKE38ZN0800
SPI ROM Socket
DG008000031

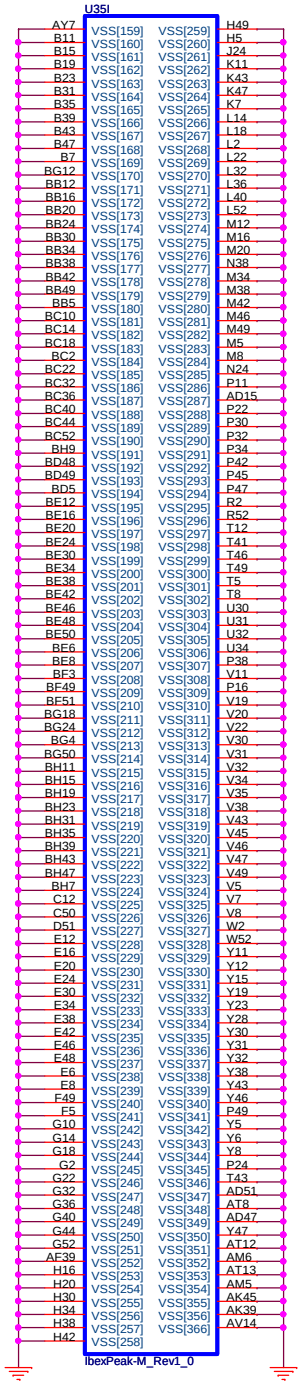
[2,8,9,11,29,34,36,42] +1.05V
[2,3,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[3,21,25,28,29,30,34,35,36,38,40,41,42] +3VPCU

NB5

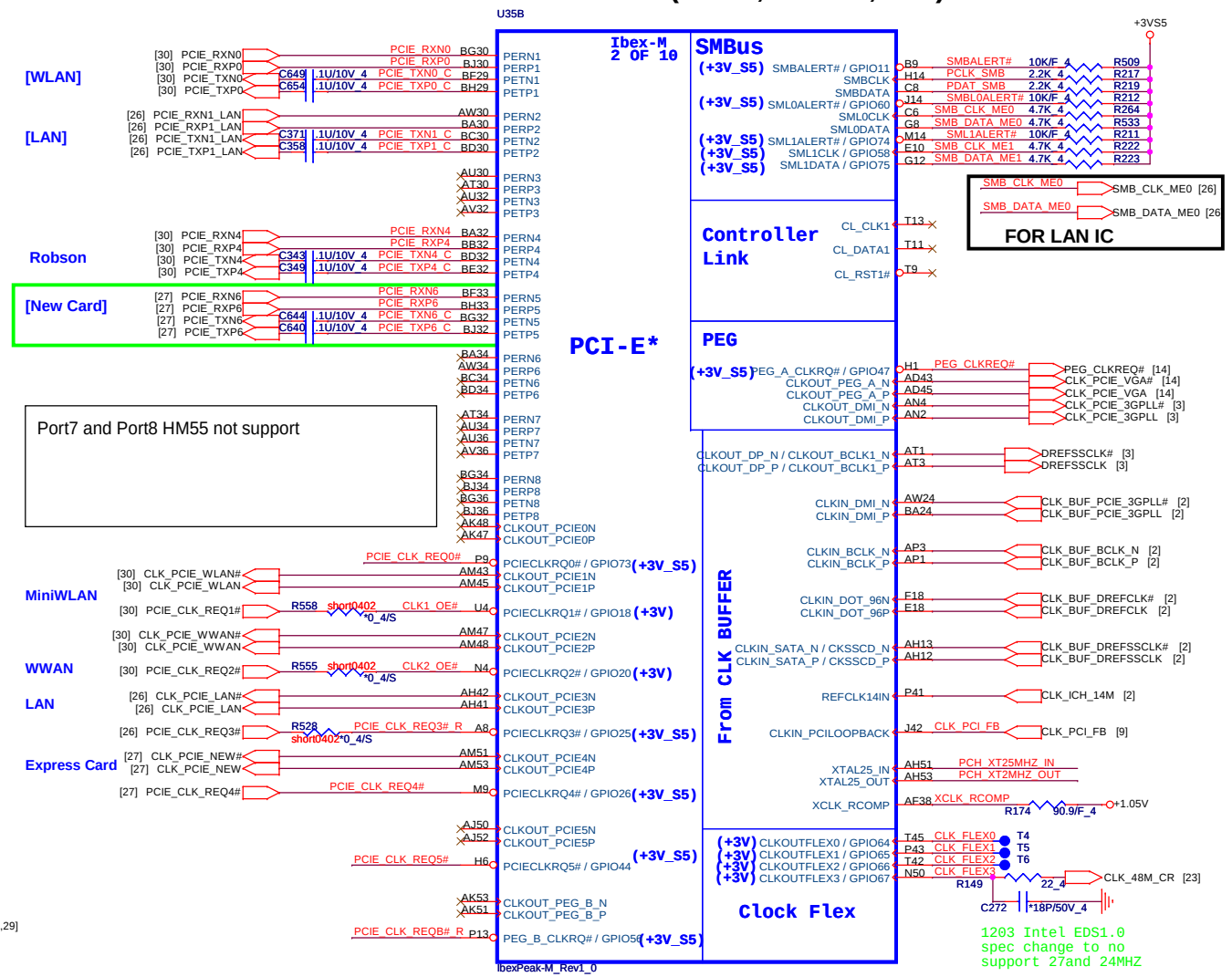
PROJECT : QL4
Quanta Computer Inc.

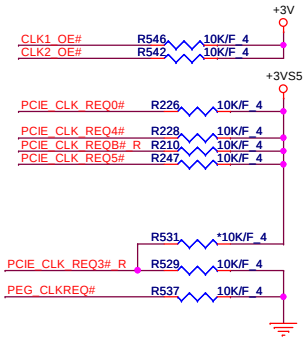
Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	E
Date: Friday, October 09, 2009	Sheet 7 of 44	

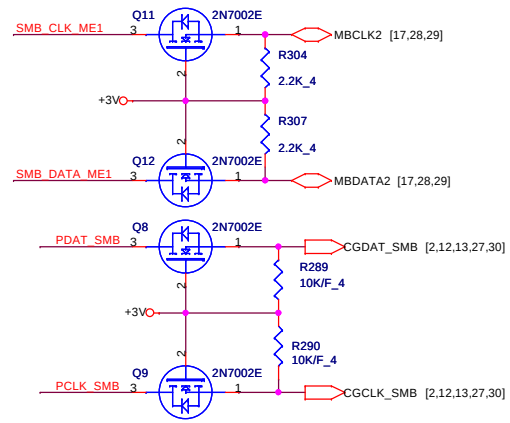
IBEX PEAK-M (GND)

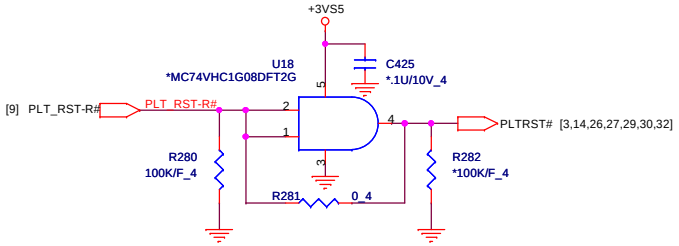


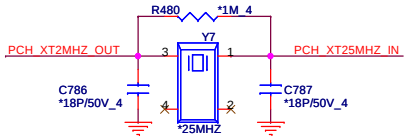
IBEX PEAK-M (PCI-E,SMBUS,CLK)











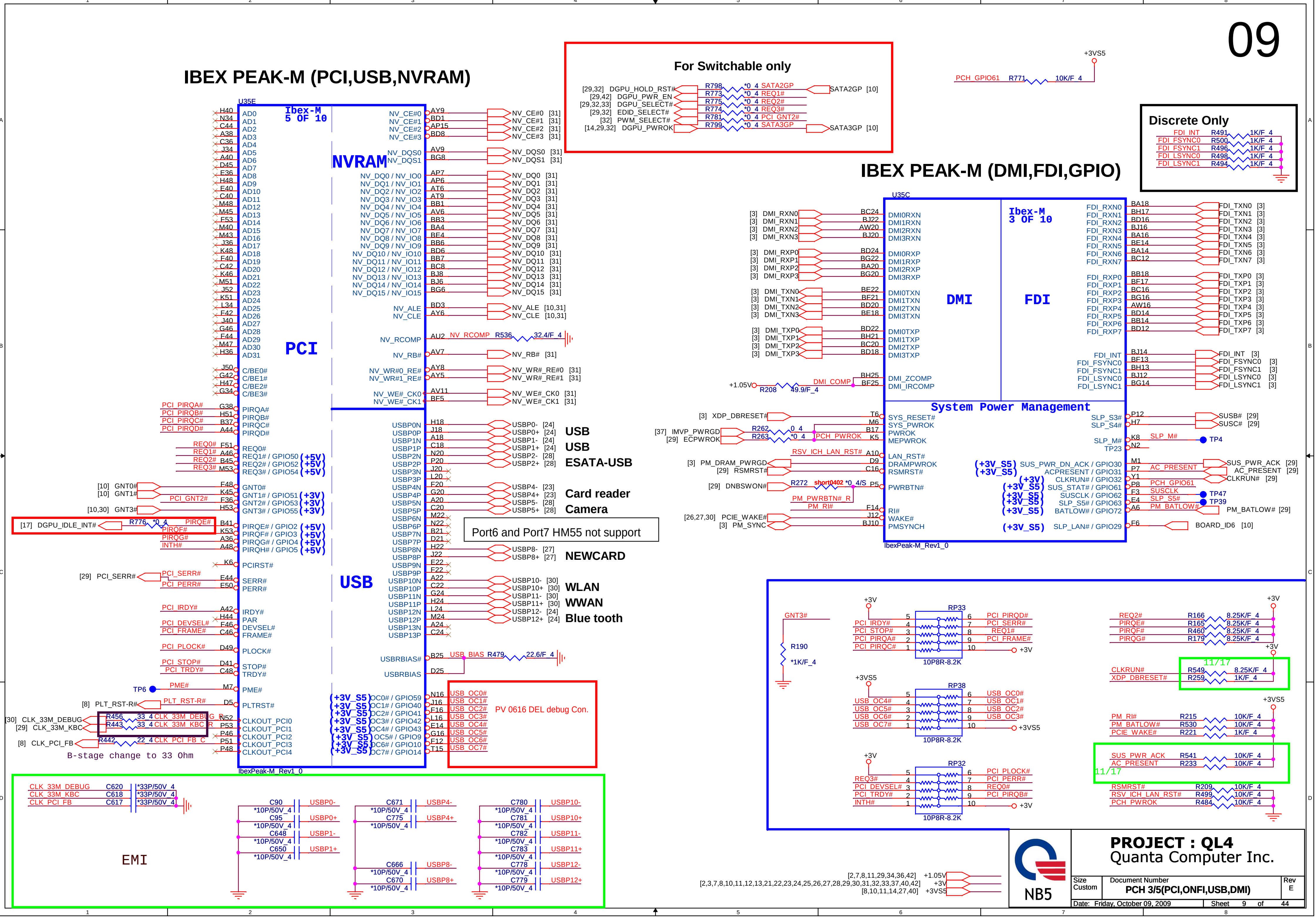
[2,7,9,11,29,34,36,42] +1.05V
[2,3,7,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[9,10,11,14,27,40] +3VS5

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS,CK)	E
Date: Friday, October 09, 2009	Sheet 8 of 44	

08



09
IBEX PEAK-M (PCI,USB,NVRAM)
U35E
Ibex-M 5 OF 10
NVRAM
PCI
USB
For Switchable only
DGPU_HOLD_RST#
DGPU_PWR_EN
DGPU_SELECT#
EDID_SELECT#
PWM_SELECT#
DGPU_PWROK
SATA2GP
SATA3GP
Discrete Only
FDI_INT
FDI_FSYNC0
FDI_FSYNC1
FDI_LSYNC0
FDI_LSYNC1
IBEX PEAK-M (DMI,FDI,GPIO)
U35C
Ibex-M 3 OF 10
DMI
FDI
System Power Management
USB
USB
ESATA-USB
Card reader
Camera
Port6 and Port7 HM55 not support
NEWCARD
WLAN
WWAN
Blue tooth
PV 0616 DEL debug Con.
B-stage change to 33 Ohm
IbexPeak-M_Rev1_0
EMI
11/17
PROJECT : QL4
Quanta Computer Inc.
NB5
Size Custom
Document Number
PCH 3/5(PCI,ONFI,USB,DMI)
Rev E
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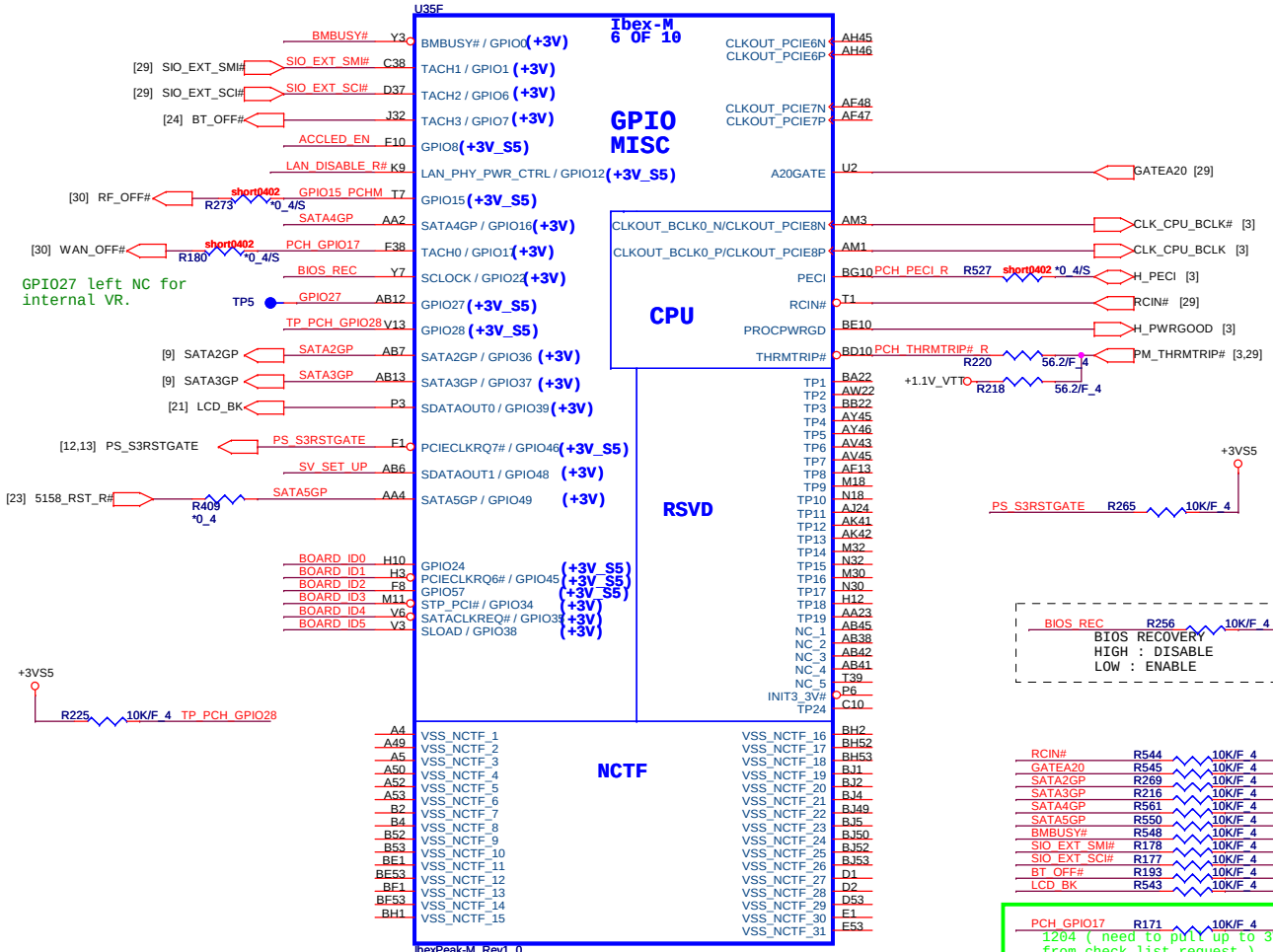
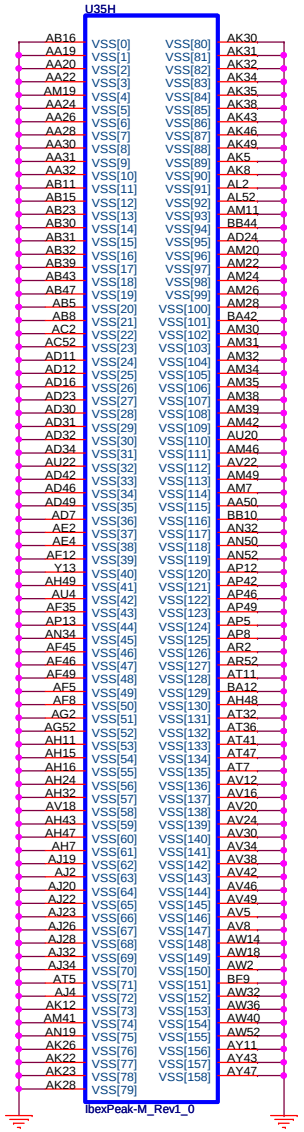
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



10

[9,30] GNT3# R461 *10K_NC

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R271 10K/F_4 +3V

SV_SET_UP	1-X High = Strong (Default)

[9] GNT0# GNT0# R155 *1K/F_4
[9] GNT1# GNT1# R157 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

[9,31] NV_ALE R534 *1K/F_4
[9,31] NV_CLE R535 *1K/F_4 +1.8V
11/17

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

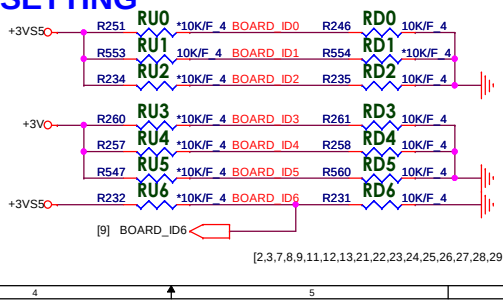
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

[7,24] SPKR SPKR *1K/F_4 R556 +3V
[7] PCH_GPIO33 R194 *100K/F_4

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6"/ 14"			0=QL4/TW9 1=QL2/SW9				
Switchable						1=YES 0=NO	

BOARD ID SETTING



Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

[3,5,11,34,38] +1.1V_VTT
[5,11,31,36,40,42] +1.8V
[2,3,7,8,9,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[8,9,11,14,27,40] +3VS5

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	E
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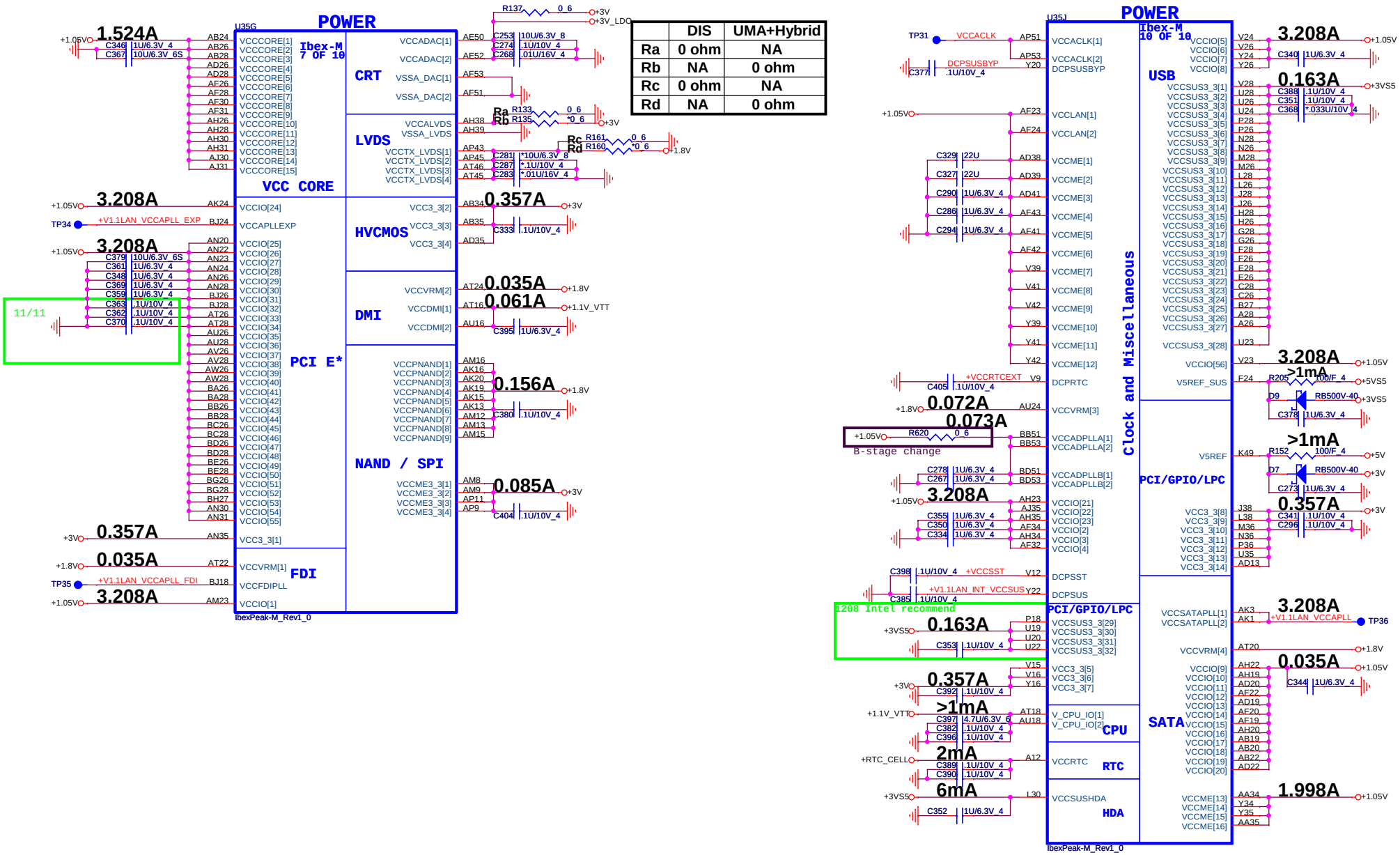


	DIS	UMA+Hybrid
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

[2,7,8,9,29,34,36,42] +1.05V
[3,5,10,34,38] +1.1V_VTT
[5,10,31,36,40,42] +1.8V
[2,3,7,8,9,10,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[8,9,10,14,27,40] +3VS5
[22,24,25,27,28,30,32,40] +5V
[40] +5VS5

PROJECT : QL4
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	E

Date: Friday, October 09, 2009 | Sheet 11 of 44

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

JDIM2A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM0

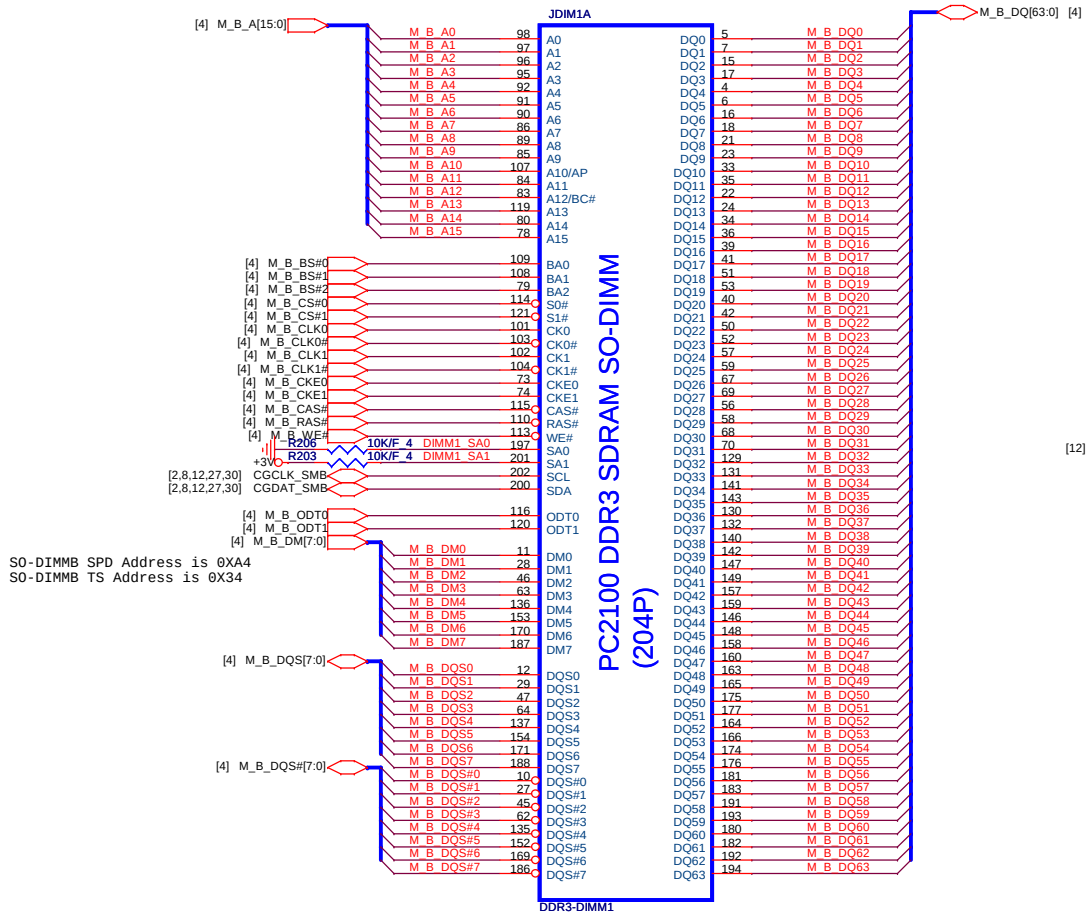
JDIM2B

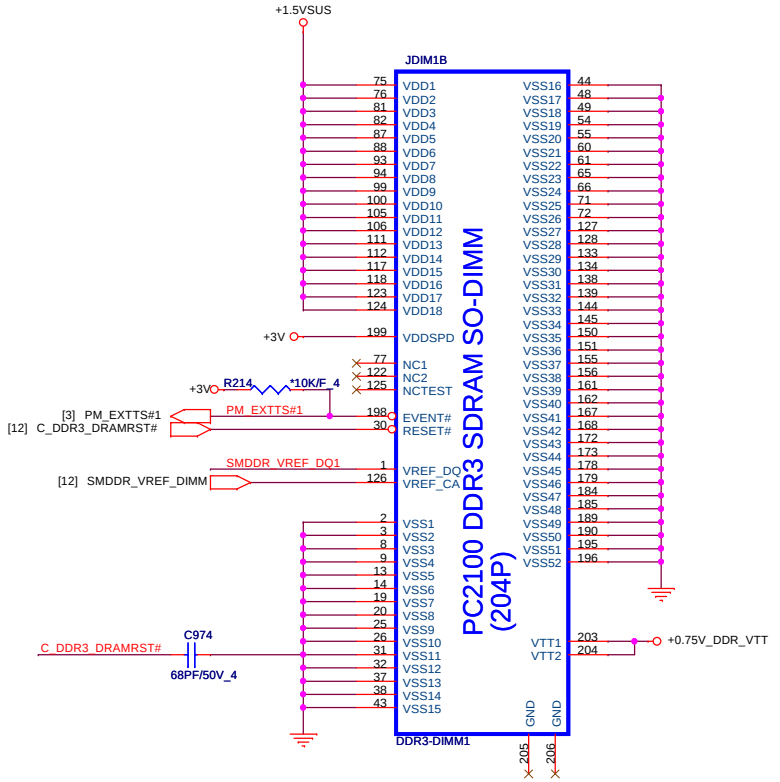
PC2100 DDR3 SDRAM SO-DIMM (204P)

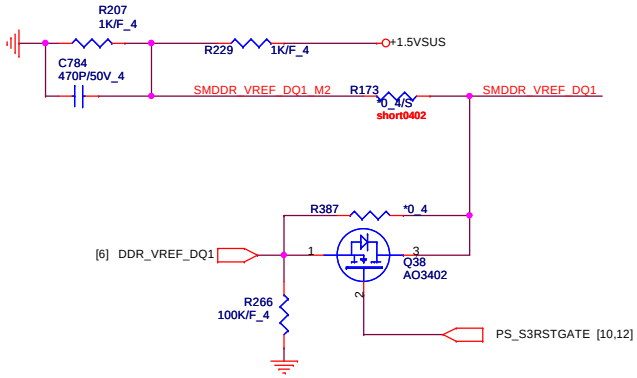
DDR3-DIMM0

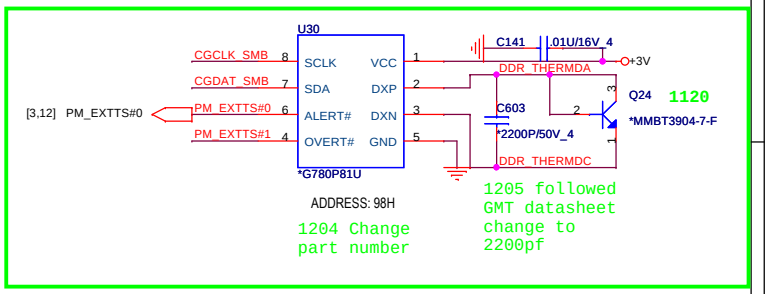
Place these Caps near So-Dimm0.

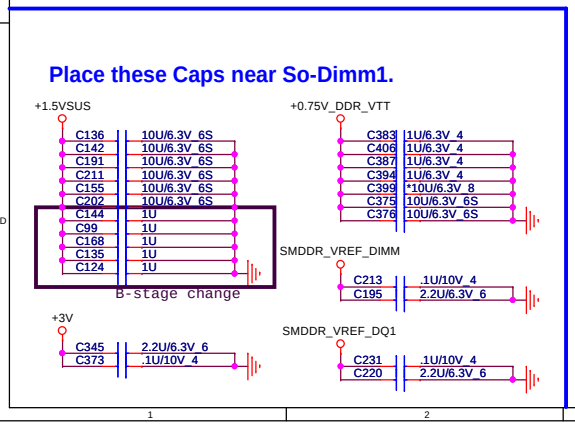
B-stage change











[12,39] +0.75V_DDR_VTT
[5,12,39,40,42] +1.5VSUS
[2,3,7,8,9,10,11,12,21,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[3,7,21,25,28,29,30,34,35,36,38,40,41,42] +3VPCU
[29,34,35,36,37,38,39,40] +5VPCU

NB5	PROJECT : QL4 Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM-1	Rev: E
Date: Friday, October 09, 2009	Sheet 13 of 44	

PEX_IOVDD+PEX_IOVDDQ+PEX_PLLVDD >2.2A

~ 500mA

1600mA

Near BGA

11/4

12~16 mils width

110mA

B-stage change to 100nH

12~16 mils width

11/12

PCI EXPRESS

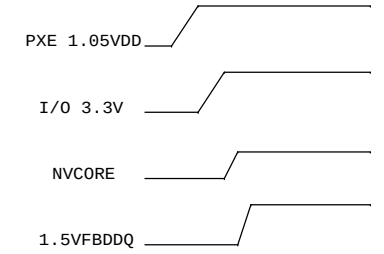
U33A
BGA969-NVIDIA-NB9P-GS
COMMON

R450 un-mount for switchable function

1211 for Nvidia request
add transition cap

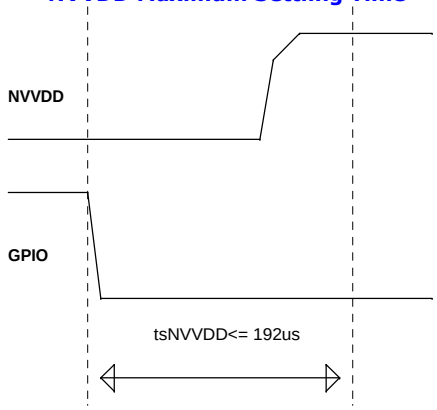
Only for Hybrid

power up sequence

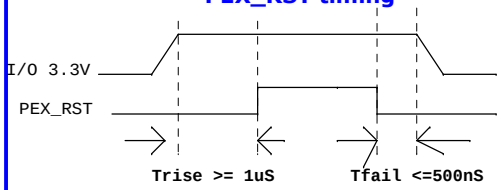


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing



[15,16,32,42] +1.05V_GFX
[16,17,22,32,33,38,42] +3V_GFX

NB5	PROJECT : QL4 Quanta Computer Inc.	
Size: Custom	Document Number: N10M-GE (PCIE I/F) 1/5	Rev: E
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U33B
BGA969-NVIDIA-NB9P-GS
COMMON

12/02 modify
package for N10

[19] FBA_CMD0 V32 FBA_CMD0
[19] FBA_CMD1 W31 FBA_CMD1
[19] FBA_CMD2 U31 FBA_CMD2
[19] FBA_CMD3 Y32 FBA_CMD3
[19] FBA_CMD4 AB35 FBA_CMD4
[19] FBA_CMD5 AB34 FBA_CMD5
[19] FBA_CMD6 W35 FBA_CMD6
[19] FBA_CMD7 W33 FBA_CMD7
[19] FBA_CMD8 W30 FBA_CMD8
[19] FBA_CMD9 T34 FBA_CMD9
[19] FBA_CMD10 T35 FBA_CMD10
[19] FBA_CMD11 AB31 FBA_CMD11
[19] FBA_CMD12 Y30 FBA_CMD12
[19] FBA_CMD13 Y34 FBA_CMD13
[19] FBA_CMD14 W32 FBA_CMD14
[19] FBA_CMD15 AA30 FBA_CMD15
[19] FBA_CMD16 AA32 FBA_CMD16
[19] FBA_CMD17 Y33 FBA_CMD17
[19] FBA_CMD18 U32 FBA_CMD18
[19] FBA_CMD19 Y31 FBA_CMD19
[19] FBA_CMD20 U34 FBA_CMD20
[19] FBA_CMD21 Y35 FBA_CMD21
[19] FBA_CMD22 W34 FBA_CMD22
[19] FBA_CMD23 V30 FBA_CMD23
[19] FBA_CMD24 U35 FBA_CMD24
[19] FBA_CMD25 U30 FBA_CMD25
[19] FBA_CMD26 U33 FBA_CMD26
[19] FBA_CMD27 AB30 FBA_CMD27
[19] FBA_CMD28 AB33 FBA_CMD28
[19] FBA_CMD29 T33 FBA_CMD29
[19] FBA_CMD30 W29 FBA_CMD30

12/02 modify
package for N10

VMA_DM0 P32 FBA_DQM0
VMA_DM1 H34 FBA_DQM1
VMA_DM2 J30 FBA_DQM2
VMA_DM3 P30 FBA_DQM3
VMA_DM4 AE32 FBA_DQM4
VMA_DM5 AL32 FBA_DQM5
VMA_DM6 AL34 FBA_DQM6
VMA_DM7 AE35 FBA_DQM7

VMA_WDQS0 L34 FBA_DQS_WP0
VMA_WDQS1 H35 FBA_DQS_WP1
VMA_WDQS2 J32 FBA_DQS_WP2
VMA_WDQS3 N31 FBA_DQS_WP3
VMA_WDQS4 AE31 FBA_DQS_WP4
VMA_WDQS5 AJ32 FBA_DQS_WP5
VMA_WDQS6 AJ34 FBA_DQS_WP6
VMA_WDQS7 AC33 FBA_DQS_WP7

VMA_RDQS0 L35 FBA_DQS_RN0
VMA_RDQS1 G35 FBA_DQS_RN1
VMA_RDQS2 H31 FBA_DQS_RN2
VMA_RDQS3 N32 FBA_DQS_RN3
VMA_RDQS4 AD32 FBA_DQS_RN4
VMA_RDQS5 AJ31 FBA_DQS_RN5
VMA_RDQS6 AJ35 FBA_DQS_RN6
VMA_RDQS7 AC34 FBA_DQS_RN7

P29 FBA_WCK0
R29 FBA_WCK0_N
L29 FBA_WCK1
M29 FBA_WCK1_N
AG29 FBA_WCK2
AH29 FBA_WCK2_N
AD29 FBA_WCK3
AE29 FBA_WCK3_N

+1.5V_GFX
AA27 FBVDDQ_1
AA29 FBVDDQ_2
AA31 FBVDDQ_3
AB27 FBVDDQ_4
AB29 FBVDDQ_5
AC27 FBVDDQ_6
AD27 FBVDDQ_7
AE27 FBVDDQ_8
AJ28 FBVDDQ_9
B18 FBVDDQ_10
E21 FBVDDQ_11
G17 FBVDDQ_12
G18 FBVDDQ_13
G22 FBVDDQ_14
G8 FBVDDQ_15
G9 FBVDDQ_16
H29 FBVDDQ_17
J14 FBVDDQ_18
J15 FBVDDQ_19
J16 FBVDDQ_20
J17 FBVDDQ_21
J20 FBVDDQ_22
J21 FBVDDQ_23
J22 FBVDDQ_24
J23 FBVDDQ_25
J24 FBVDDQ_26
J29 FBVDDQ_27

MEMORY I/F A

12/02 modify
package for N10

FBA_D00 L32 VMA_DQ0
FBA_D01 N33 VMA_DQ1
FBA_D02 L33 VMA_DQ2
FBA_D03 N34 VMA_DQ3
FBA_D04 N35 VMA_DQ4
FBA_D05 P35 VMA_DQ5
FBA_D06 P33 VMA_DQ6
FBA_D07 P34 VMA_DQ7
FBA_D08 K35 VMA_DQ8
FBA_D09 K33 VMA_DQ9
FBA_D10 K34 VMA_DQ10
FBA_D11 H33 VMA_DQ11
FBA_D12 G34 VMA_DQ12
FBA_D13 G33 VMA_DQ13
FBA_D14 E34 VMA_DQ14
FBA_D15 E33 VMA_DQ15
FBA_D16 G31 VMA_DQ16
FBA_D17 F30 VMA_DQ17
FBA_D18 G30 VMA_DQ18
FBA_D19 G32 VMA_DQ19
FBA_D20 K30 VMA_DQ20
FBA_D21 K32 VMA_DQ21
FBA_D22 H30 VMA_DQ22
FBA_D23 K31 VMA_DQ23
FBA_D24 L31 VMA_DQ24
FBA_D25 L30 VMA_DQ25
FBA_D26 M32 VMA_DQ26
FBA_D27 N30 VMA_DQ27
FBA_D28 M30 VMA_DQ28
FBA_D29 P31 VMA_DQ29
FBA_D30 R32 VMA_DQ30
FBA_D31 R30 VMA_DQ31
AG30 VMA_DQ32
AG32 VMA_DQ33
AH31 VMA_DQ34
AF31 VMA_DQ35
AE30 VMA_DQ36
AE30 VMA_DQ37
AC32 VMA_DQ38
AD30 VMA_DQ39
AN33 VMA_DQ40
AL31 VMA_DQ41
AM33 VMA_DQ42
AL33 VMA_DQ43
AK30 VMA_DQ44
AK32 VMA_DQ45
AJ30 VMA_DQ46
AH30 VMA_DQ47
AH33 VMA_DQ48
AH35 VMA_DQ49
AH34 VMA_DQ50
AH32 VMA_DQ51
AJ33 VMA_DQ52
AL35 VMA_DQ53
AM34 VMA_DQ54
AM35 VMA_DQ55
AF33 VMA_DQ56
AE32 VMA_DQ57
AF34 VMA_DQ58
AE35 VMA_DQ59
AE34 VMA_DQ60
AE33 VMA_DQ61
AB32 VMA_DQ62
AC35 VMA_DQ63

FBA_CLK0 T32 VMA_CLK0
FBA_CLK0* T31 VMA_CLK0#
FBA_CLK1 AC31 VMA_CLK1
FBA_CLK1* AC30 VMA_CLK1#

VMA_CLK0 [19]
VMA_CLK0# [19]
VMA_CLK1 [19]
VMA_CLK1# [19]

FB_VREF J27 +FB_VREF1 TP2
15mils width

For Debug only
FBA_DEBUG T30 FBA_DEBUG R140 *10K/F_4 +1.5V_GFX
15mils width

FB_DLLAVDD0 AG27 +FB_PLLAVDD L17 PBY160808T-301Y-N_6 +1.05V_GFX
FB_PLLAVDD0 AF27
C259 4.7U/6.3V_6
C249 1U/6.3V_4
C248 .1U/10V_4

[19] VMA_DQ[63..0]
[19] VMA_DM[7..0]
[19] VMA_WDQS[7..0]
[19] VMA_RDQS[7..0]
[20] VMC_DQ[63..0]
[20] VMC_DM[7..0]
[20] VMC_WDQS[7..0]
[20] VMC_RDQS[7..0]

FBA_CMD28 R515 10K/F_4
FBC_CMD28 R156 10K/F_4
FBA_CMD7 R514 10K/F_4
FBA_CMD15 R519 10K/F_4
FBA_CMD18 R523 10K/F_4
FBA_CMD30 R522 10K/F_4
FBC_CMD7 R164 10K/F_4
FBC_CMD15 R134 10K/F_4
FBC_CMD18 R84 10K/F_4
FBC_CMD30 R94 10K/F_4

All need stuff for N10P

2/16
+1.5V_GFX
C181 .01U/16V_4
C250 .01U/16V_4
C251 .01U/16V_4
C254 .01U/16V_4
C260 .1U/10V_4
C239 .1U/10V_4
C247 .1U/10V_4
C246 0.047U/10V
C222 0.047U/10V
C256 0.047U/10V
C255 4.7U/6.3V_6
C205 4.7U/6.3V_6
All need stuff for N10P

U33C
BGA969-NVIDIA-NB9P-GS
COMMON

12/02 modify
package for N10

[20] FBC_CMD0 C17 FBC_CMD0
[20] FBC_CMD1 B19 FBC_CMD1
[20] FBC_CMD2 D18 FBC_CMD2
[20] FBC_CMD3 F21 FBC_CMD3
[20] FBC_CMD4 A23 FBC_CMD4
[20] FBC_CMD5 D21 FBC_CMD5
[20] FBC_CMD6 B23 FBC_CMD6
[20] FBC_CMD7 E20 FBC_CMD7
[20] FBC_CMD8 G21 FBC_CMD8
[20] FBC_CMD9 F20 FBC_CMD9
[20] FBC_CMD10 F19 FBC_CMD10
[20] FBC_CMD11 F23 FBC_CMD11
[20] FBC_CMD12 A22 FBC_CMD12
[20] FBC_CMD13 C22 FBC_CMD13
[20] FBC_CMD14 B17 FBC_CMD14
[20] FBC_CMD15 F24 FBC_CMD15
[20] FBC_CMD16 C25 FBC_CMD16
[20] FBC_CMD17 E22 FBC_CMD17
[20] FBC_CMD18 C20 FBC_CMD18
[20] FBC_CMD19 B22 FBC_CMD19
[20] FBC_CMD20 A19 FBC_CMD20
[20] FBC_CMD21 D22 FBC_CMD21
[20] FBC_CMD22 D20 FBC_CMD22
[20] FBC_CMD23 E19 FBC_CMD23
[20] FBC_CMD24 D19 FBC_CMD24
[20] FBC_CMD25 F18 FBC_CMD25
[20] FBC_CMD26 C19 FBC_CMD26
[20] FBC_CMD27 E22 FBC_CMD27
[20] FBC_CMD28 C23 FBC_CMD28
[20] FBC_CMD29 B20 FBC_CMD29
[20] FBC_CMD30 A20 FBC_CMD30

12/02 modify
package for N10

VMC_DM0 A16 FBC_DQM0
VMC_DM1 D10 FBC_DQM1
VMC_DM2 F11 FBC_DQM2
VMC_DM3 D15 FBC_DQM3
VMC_DM4 D27 FBC_DQM4
VMC_DM5 D34 FBC_DQM5
VMC_DM6 A34 FBC_DQM6
VMC_DM7 D28 FBC_DQM7

VMC_WDQS0 C14 FBC_DQS_WP0
VMC_WDQS1 A10 FBC_DQS_WP1
VMC_WDQS2 E10 FBC_DQS_WP2
VMC_WDQS3 D14 FBC_DQS_WP3
VMC_WDQS4 E26 FBC_DQS_WP4
VMC_WDQS5 D32 FBC_DQS_WP5
VMC_WDQS6 A32 FBC_DQS_WP6
VMC_WDQS7 B26 FBC_DQS_WP7

VMC_RDQS0 B14 FBC_DQS_RN0
VMC_RDQS1 B10 FBC_DQS_RN1
VMC_RDQS2 D9 FBC_DQS_RN2
VMC_RDQS3 E14 FBC_DQS_RN3
VMC_RDQS4 F26 FBC_DQS_RN4
VMC_RDQS5 D31 FBC_DQS_RN5
VMC_RDQS6 A31 FBC_DQS_RN6
VMC_RDQS7 A26 FBC_DQS_RN7

G14 FBC_WCK0
G15 FBC_WCK0_N
G11 FBC_WCK1
G12 FBC_WCK1_N
G27 FBC_WCK2
G28 FBC_WCK2_N
G24 FBC_WCK3
G25 FBC_WCK3_N

+1.5V_GFX
N27 FBVDDQ_28
P27 FBVDDQ_29
R27 FBVDDQ_30
T27 FBVDDQ_31
U27 FBVDDQ_32
U29 FBVDDQ_33
V27 FBVDDQ_34
V29 FBVDDQ_35
V34 FBVDDQ_36
W27 FBVDDQ_37
Y27 FBVDDQ_38

MEMORY I/F C

FBC_D00 B13 VMC_DQ0
FBC_D01 D13 VMC_DQ1
FBC_D02 A13 VMC_DQ2
FBC_D03 A14 VMC_DQ3
FBC_D04 C16 VMC_DQ4
FBC_D05 B16 VMC_DQ5
FBC_D06 A17 VMC_DQ6
FBC_D07 D16 VMC_DQ7
FBC_D08 C13 VMC_DQ8
FBC_D09 B11 VMC_DQ9
FBC_D10 C11 VMC_DQ10
FBC_D11 A11 VMC_DQ11
FBC_D12 C10 VMC_DQ12
FBC_D13 C8 VMC_DQ13
FBC_D14 B8 VMC_DQ14
FBC_D15 A8 VMC_DQ15
FBC_D16 E8 VMC_DQ16
FBC_D17 F8 VMC_DQ17
FBC_D18 F10 VMC_DQ18
FBC_D19 F9 VMC_DQ19
FBC_D20 F12 VMC_DQ20
FBC_D21 D8 VMC_DQ21
FBC_D22 D11 VMC_DQ22
FBC_D23 E11 VMC_DQ23
FBC_D24 D12 VMC_DQ24
FBC_D25 E13 VMC_DQ25
FBC_D26 F13 VMC_DQ26
FBC_D27 E14 VMC_DQ27
FBC_D28 F15 VMC_DQ28
FBC_D29 E16 VMC_DQ29
FBC_D30 F16 VMC_DQ30
FBC_D31 F17 VMC_DQ31
FBC_D32 D29 VMC_DQ32
FBC_D33 F27 VMC_DQ33
FBC_D34 F28 VMC_DQ34
FBC_D35 E28 VMC_DQ35
FBC_D36 D26 VMC_DQ36
FBC_D37 F25 VMC_DQ37
FBC_D38 D24 VMC_DQ38
FBC_D39 E25 VMC_DQ39
FBC_D40 E32 VMC_DQ40
FBC_D41 F32 VMC_DQ41
FBC_D42 D33 VMC_DQ42
FBC_D43 E31 VMC_DQ43
FBC_D44 C33 VMC_DQ44
FBC_D45 F29 VMC_DQ45
FBC_D46 D30 VMC_DQ46
FBC_D47 E29 VMC_DQ47
FBC_D48 B29 VMC_DQ48
FBC_D49 C31 VMC_DQ49
FBC_D50 C29 VMC_DQ50
FBC_D51 B31 VMC_DQ51
FBC_D52 C32 VMC_DQ52
FBC_D53 B32 VMC_DQ53
FBC_D54 B35 VMC_DQ54
FBC_D55 B34 VMC_DQ55
FBC_D56 A29 VMC_DQ56
FBC_D57 B28 VMC_DQ57
FBC_D58 A28 VMC_DQ58
FBC_D59 C28 VMC_DQ59
FBC_D60 C26 VMC_DQ60
FBC_D61 D25 VMC_DQ61
FBC_D62 B25 VMC_DQ62
FBC_D63 A25 VMC_DQ63

FBC_CLK0 E17 VMC_CLK0
FBC_CLK0* D17 VMC_CLK0#
FBC_CLK1 D23 VMC_CLK1
FBC_CLK1* E23 VMC_CLK1#

VMC_CLK0 [20]
VMC_CLK0# [20]
VMC_CLK1 [20]
VMC_CLK1# [20]

FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ R130 40.2/F_4 +1.5V_GFX
FB_CAL_PU_GND L27 FB_CAL_PU_GND R131 40.2/F_4
FB_CAL_TERM_GND M27 FB_CAL_TERM_GND R146 40.2/F_4
11/4
12/16 Modified
FBC_DEBUG G19 FBC_DEBUG R117 *10K/F_4 +1.5V_GFX
NC/ FB_DLLAVDD1 J19
NC/ FB_PLLAVDD1 J18
R92 no stuff

[14,16,32,42] +1.05V_GFX
[19,20,32,42] +1.5V_GFX

NB5

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Quanta Computer Inc.

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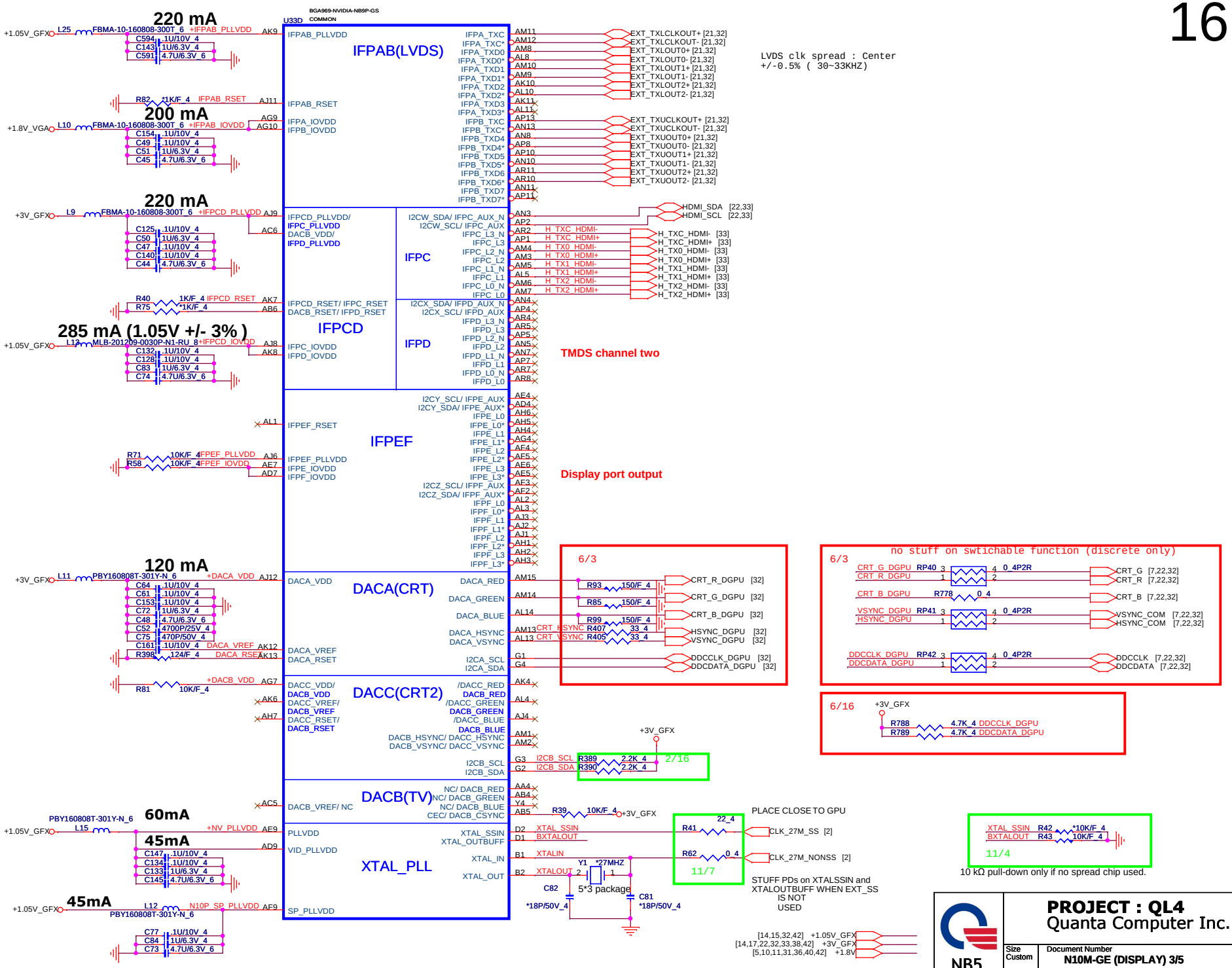
BGA969-NVIDIA-NB9P-GS
U33D COMMON
IFPAB(LVDS)
IFPCD
IFPC
IFPD
IFPEF
DACA(CRT)
DACC(CRT2)
DACB(TV)
XTAL_PLL
220 mA
200 mA
220 mA
285 mA (1.05V +/- 3%)
120 mA
60mA
45mA
45mA
TMDS channel two
Display port output
LVDS clk spread : Center
+/-0.5% (30~33KHZ)
no stuff on swtichable function (discrete only)
PLACE CLOSE TO GPU
STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED
10 kΩ pull-down only if no spread chip used.
PROJECT : QL4
Quanta Computer Inc.
NB5
N10M-GE (DISPLAY) 3/5
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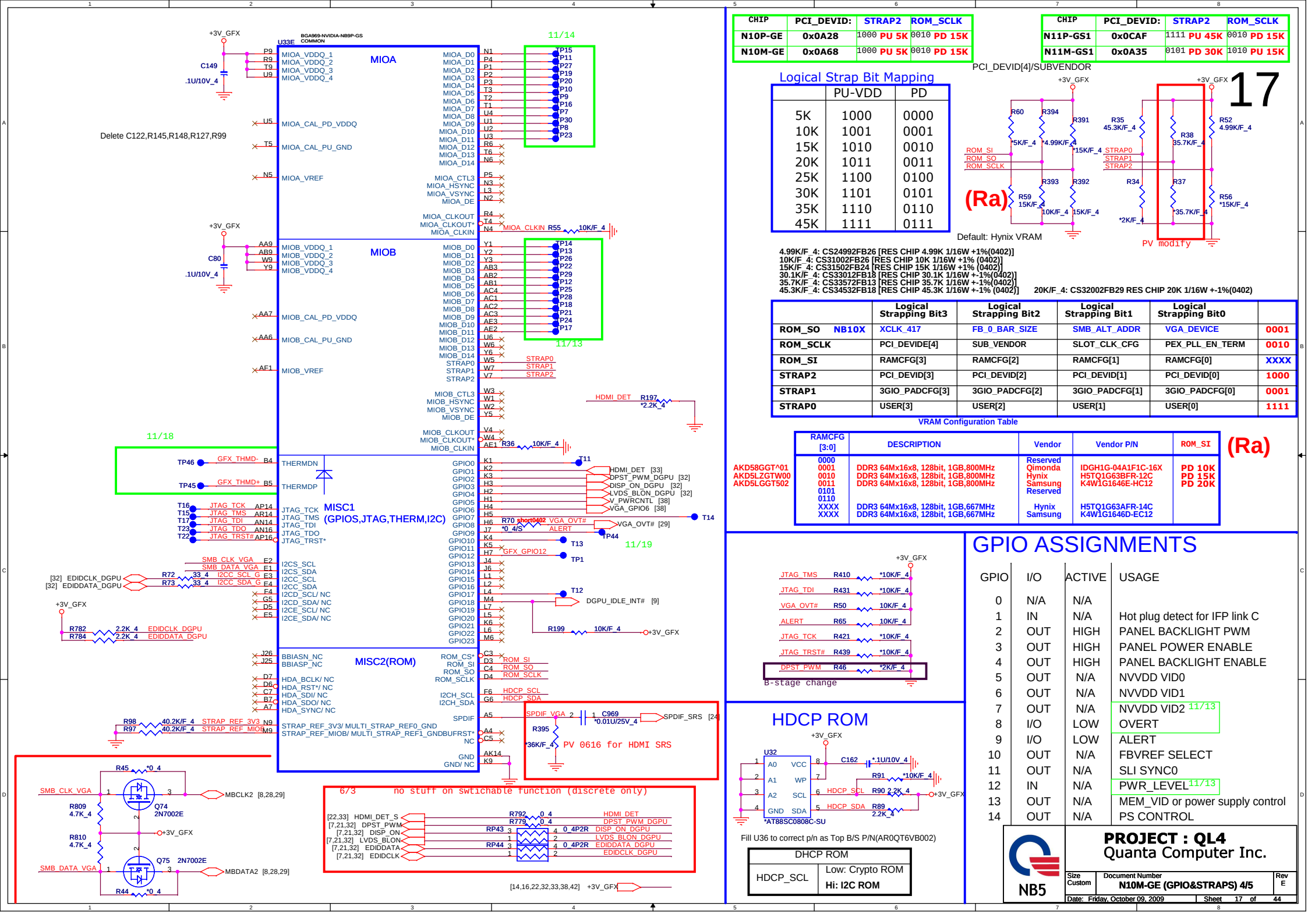

CHIP	PCI_DEVID:	STRAP2	ROM_SCLK
N10P-GE	0x0A28	1000 PU 5K	0010 PD 15K
N10M-GE	0x0A68	1000 PU 5K	0010 PD 15K

CHIP	PCI_DEVID:	STRAP2	ROM_SCLK
N11P-GS1	0x0CAF	1111 PU 45K	0010 PD 15K
N11M-GS1	0x0A35	0101 PD 30K	1010 PU 15K

PCI_DEVID[4]/SUBVENDOR

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

(Ra)

Default: Hynix VRAM

PV modify

17

4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)]
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]
20K/F_4: CS32002FB29 RES CHIP 20K 1/16W +-1%(0402)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

VRAM Configuration Table

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
	0000		Reserved		
AKD58GGT^01	0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
AKD5LZGTW00	0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
AKD5LGGT502	0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-HC12	PD 20K
	0101		Reserved		
	0110				
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

HDCP ROM

*AT88SC0808C-SU

Fill U36 to correct p/n as Top B/S P/N(AR0QT6VB002)

DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

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Quanta Computer Inc.

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U33F

BGA969-NVIDIA-NB9P-GS
COMMON

+VGACORE

+VGACORE

NVVDD

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

NVVDD Decoupling

+VGACORE

2/16

PLACE UNDER BALLS

C235	.01U/16V_4
C226	.01U/16V_4
C164	.01U/16V_4
C179	.01U/16V_4
C223	.01U/16V_4
C193	.01U/16V_4
C158	.033U/10V_4
C199	.033U/10V_4
C166	.033U/10V_4
C227	.047U/25V_4
C200	.047U/25V_4
C212	.047U/25V_4
C165	.1U/10V_4
C182	1U/6.3V_4
C170	1U/6.3V_4
C163	1U/6.3V_4

PLACE NEAR BALLS

C169	4.7U/6.3V_6
C215	10U/6.3V_8
C184	10U/6.3V_8

C131 330U/2.5V_6032

U33G

BGA969-NVIDIA-NB9P-GS
COMMON

GROUND

AA11	GND_1	GND_096	E15
AA12	GND_2	GND_097	E18
AA13	GND_3	GND_098	E24
AA14	GND_4	GND_099	E27
AA15	GND_5	GND_100	E30
AA16	GND_6	GND_101	E6
AA17	GND_7	GND_102	E9
AA18	GND_8	GND_103	F2
AA19	GND_9	GND_104	F31
AA2	GND_10	GND_105	F34
AA20	GND_11	GND_106	F5
AA21	GND_12	GND_107	J2
AA22	GND_13	GND_108	J31
AA23	GND_14	GND_109	J34
AA24	GND_15	GND_110	J5
AA25	GND_16	GND_111	L9
AA34	GND_17	GND_112	M11
AA5	GND_18	GND_113	M13
AB12	GND_19	GND_114	M15
AB14	GND_20	GND_115	M17
AB16	GND_21	GND_116	M19
AB18	GND_22	GND_117	M2
AB20	GND_23	GND_118	M21
AB22	GND_24	GND_119	M23
AB24	GND_25	GND_120	M25
AC9	GND_26	GND_121	M31
AD11	GND_27	GND_122	M34
AD13	GND_28	GND_123	M5
AD15	GND_29	GND_124	N11
AD17	GND_30	GND_125	N12
AD2	GND_31	GND_126	N13
AD21	GND_32	GND_127	N14
AD23	GND_33	GND_128	N15
AD25	GND_34	GND_129	N16
AD31	GND_35	GND_130	N17
AD34	GND_36	GND_131	N18
AD5	GND_37	GND_132	N19
AE11	GND_38	GND_133	N20
AE12	GND_39	GND_134	N21
AE13	GND_40	GND_135	N22
AE14	GND_41	GND_136	N23
AE15	GND_42	GND_137	N24
AE16	GND_43	GND_138	N25
AE17	GND_44	GND_139	P12
AE18	GND_45	GND_140	P14
AE19	GND_46	GND_141	P16
AE20	GND_47	GND_142	P18
AE21	GND_48	GND_143	P20
AE22	GND_49	GND_144	P22
AE23	GND_50	GND_145	P24
AE24	GND_51	GND_146	R2
AE25	GND_52	GND_147	R31
AG2	GND_53	GND_148	R34
AG31	GND_54	GND_149	R5
AG34	GND_55	GND_150	T11
AG5	GND_56	GND_151	T13
AK2	GND_57	GND_152	T15
AK31	GND_58	GND_153	T17
AK34	GND_59	GND_154	T19
AK5	GND_60	GND_155	T21
AL12	GND_61	GND_156	T23
AL15	GND_62	GND_157	T25
AL18	GND_63	GND_158	U11
AL21	GND_64	GND_159	U12
AL24	GND_65	GND_160	U13
AL27	GND_66	GND_161	U14
AL30	GND_67	GND_162	U15
AL6	GND_68	GND_163	U16
AL9	GND_69	GND_164	U17
AN2	GND_70	GND_165	U18
AN34	GND_71	GND_166	U19
AP12	GND_72	GND_167	U20
AP15	GND_73	GND_168	U21
AP18	GND_74	GND_169	U22
AP21	GND_75	GND_170	U23
AP24	GND_76	GND_171	U24
AP27	GND_77	GND_172	U25
AP3	GND_78	GND_173	V12
AP30	GND_79	GND_174	V14
AP33	GND_80	GND_175	V16
AP6	GND_081	GND_176	V18
AP9	GND_082	GND_177	V2
B12	GND_083	GND_178	V20
B15	GND_084	GND_179	V22
B21	GND_085	GND_180	V24
B24	GND_086	GND_181	V31
B27	GND_087	GND_182	V5
B3	GND_088	GND_183	V9
B30	GND_089	GND_184	Y11
B33	GND_090	GND_185	Y13
B6	GND_091	GND_186	Y15
B9	GND_092	GND_187	Y17
C2	GND_093	GND_188	Y19
C34	GND_094	GND_189	Y21
E12	GND_095	GND_190	Y23
		GND_191	Y25

[38] +VGACORE

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Quanta Computer Inc.

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CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

U15 / U37 / U16 / U36 — VRAM _DDR3 — 96-BALL SDRAM DDR3 — SWAP

Should be 240 Ohms +-1%

R464 243/F_4 (U15)
R524 243/F_4 (U37)
R516 243/F_4 (U16)
R463 243/F_4 (U36)

11/12 — VMA_WDQS2 / VMA_RDQS2 — DQSL
11/12 — VMA_WDQS3 / VMA_RDQS3 — DQSL
11/12 — VMA_WDQS0 / VMA_RDQS0 — DQSU
11/12 — VMA_WDQS1 / VMA_RDQS1 — DQSU
11/17 Swap — VMA_WDQS5 / VMA_RDQS5 — DQSL
11/17 Swap — VMA_WDQS4 / VMA_RDQS4 — DQSU
11/17 Swap — VMA_WDQS7 / VMA_RDQS7 — DQSL
11/17 Swap — VMA_WDQS6 / VMA_RDQS6 — DQSU

+1.5V_GFX

2/19 — VMA_CLK0 — R511 243/F_4 — VMA_CLK0#
2/19 — VMA_CLK1 — R510 243/F_4 — VMA_CLK1#

11/11 — R520 1.33K/F_4 — VREFC_VMA1 — R521 1.33K/F_4 — C676 .1U/10V_4
11/11 — R526 1.33K/F_4 — VREFD_VMA1 — R525 1.33K/F_4 — C677 .1U/10V_4
11/11 — R518 1.33K/F_4 — VREFC_VMA3 — R517 1.33K/F_4 — C674 .1U/10V_4
11/11 — R512 1.33K/F_4 — VREFD_VMA3 — R513 1.33K/F_4 — C673 .1U/10V_4

+1.5V_GFX — C271 C663 C639 C615 1U/6.3V_4
+1.5V_GFX — C697 10U/6.3V_6S; C635 C266 C612 C609 C636 .1U/10V_4
+1.5V_GFX — C624 C616 C625 C228 C623 C607 C695 C680 .1U/10V_4
+1.5V_GFX — C634 C638 C619 C637 C693 C236 C685 C692 .1U/10V_4
+1.5V_GFX — C683 C678 C686 C675 .1U/10V_4

1211 for Nvidia request add transition cap

[15,20,32,42] +1.5V_GFX

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CHANNEL B: 256MB/512MB DDR3

[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]

U31 / U8 / U13 / U34 — VRAM _DDR3 — 96-BALL SDRAM DDR3 — SWAP

Should be 240 Ohms +-1%

R402 243/F_4 (VMC_ZQ1)
R411 243/F_4 (VMC_ZQ2)
R150 243/F_4 (VMC_ZQ3)
R457 243/F_4 (VMC_ZQ4)

2/19
R102 243/F_4 (VMC_CLK0 / VMC_CLK0#)
R153 243/F_4 (VMC_CLK1 / VMC_CLK1#)

11/11
R118 1.33K/F_4, R106 1.33K/F_4, C183 .1U/10V_4 (VREFC_VMC1)
R69 1.33K/F_4, R74 1.33K/F_4, C139 .1U/10V_4 (VREFD_VMC1)
R138 1.33K/F_4, R142 1.33K/F_4, C264 .1U/10V_4 (VREFC_VMC3)
R459 1.33K/F_4, R458 1.33K/F_4, C626 .1U/10V_4 (VREFD_VMC3)

+1.5V_GFX

C219 1U/6.3V_4
C295 1U/6.3V_4
C606 1U/6.3V_4
C608 1U/6.3V_4

C210 10U/6.3V_6S
C342 .1U/10V_4
C632 .1U/10V_4
C696 .1U/10V_4
C614 .1U/10V_4
C621 .1U/10V_4

C613 .1U/10V_4
C599 .1U/10V_4
C661 .1U/10V_4
C336 .1U/10V_4
C622 .1U/10V_4
C658 .1U/10V_4
C605 .1U/10V_4
C330 .1U/10V_4

C684 .1U/10V_4
C201 .1U/10V_4
C600 .1U/10V_4
C602 .1U/10V_4
C326 .1U/10V_4
C610 .1U/10V_4
C611 .1U/10V_4
C629 .1U/10V_4

[15,19,32,42] +1.5V_GFX

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE VRAM-2(DDR3 BGA96	E
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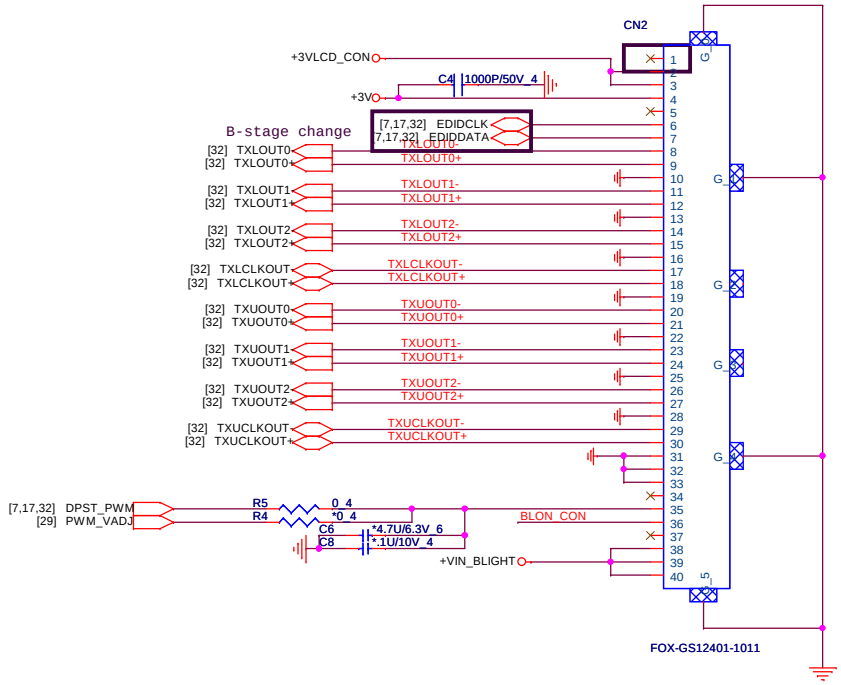
1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

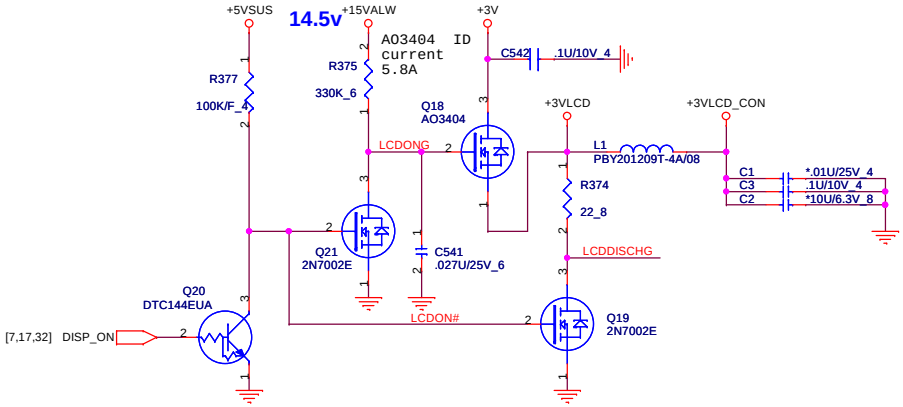
OPTION SIGNAL FROM NB FOR UMA VGA

[7,32] LA_CLK#	RP8	*0_4P2R	TXLCLKOUT-	
[7,32] LA_CLK			TXLCLKOUT+	
[7,32] LA_DATAP0	RP2	*0_4P2R	TXLOUT0+	
[7,32] LA_DATAN0			TXLOUT0-	
[7,32] LA_DATAP1	RP4	*0_4P2R	TXLOUT1+	
[7,32] LA_DATAN1			TXLOUT1-	
[7,32] LA_DATAN2	RP6	*0_4P2R	TXLOUT2-	
[7,32] LA_DATAP2			TXLOUT2+	
[7,32] LB_CLK	RP16	*0_4P2R	TXUCLKOUT+	
[7,32] LB_CLK#			TXUCLKOUT-	
[7,32] LB_DATAN0	RP10	*0_4P2R	TXUOUT0-	
[7,32] LB_DATAP0			TXUOUT0+	
[7,32] LB_DATAN1	RP12	*0_4P2R	TXUOUT1-	
[7,32] LB_DATAP1			TXUOUT1+	
[7,32] LB_DATAP2	RP14	*0_4P2R	TXUOUT2+	
[7,32] LB_DATAN2			TXUOUT2-	

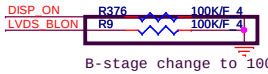
OPTION SIGNAL FROM Nvidia to VGA

[16,32] EXT_TXLCLKOUT-	RP7	0_4P2R	TXLCLKOUT-	
[16,32] EXT_TXLCLKOUT+			TXLCLKOUT+	
[16,32] EXT_TXLOUT0-	RP1	0_4P2R	TXLOUT0-	
[16,32] EXT_TXLOUT0+			TXLOUT0+	
[16,32] EXT_TXLOUT1-	RP3	0_4P2R	TXLOUT1+	
[16,32] EXT_TXLOUT1+			TXLOUT1-	
[16,32] EXT_TXLOUT2-	RP5	0_4P2R	TXLOUT2-	
[16,32] EXT_TXLOUT2+			TXLOUT2+	
[16,32] EXT_TXUCLKOUT-	RP15	0_4P2R	TXUCLKOUT-	
[16,32] EXT_TXUCLKOUT+			TXUCLKOUT+	
[16,32] EXT_TXUOUT0-	RP9	0_4P2R	TXUOUT0-	
[16,32] EXT_TXUOUT0+			TXUOUT0+	
[16,32] EXT_TXUOUT1-	RP11	0_4P2R	TXUOUT1+	
[16,32] EXT_TXUOUT1+			TXUOUT1-	
[16,32] EXT_TXUOUT2-	RP13	0_4P2R	TXUOUT2+	
[16,32] EXT_TXUOUT2+			TXUOUT2-	

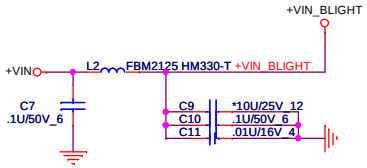


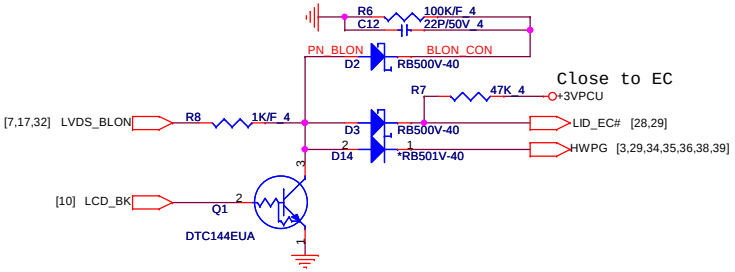


Delete in PV 0622



B-stage change to 100k Ohm





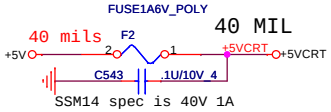
[2,3,7,8,9,10,11,12,13,22,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[3,7,25,28,29,30,34,35,36,38,40,41,42] +3VPCU
[11,22,24,25,27,28,30,32,40] +5V
[24,27,28,40] +5VSUS
[35,40] +15VALW
[2,34,35,36,37,38,39,40,41,42] +VIN

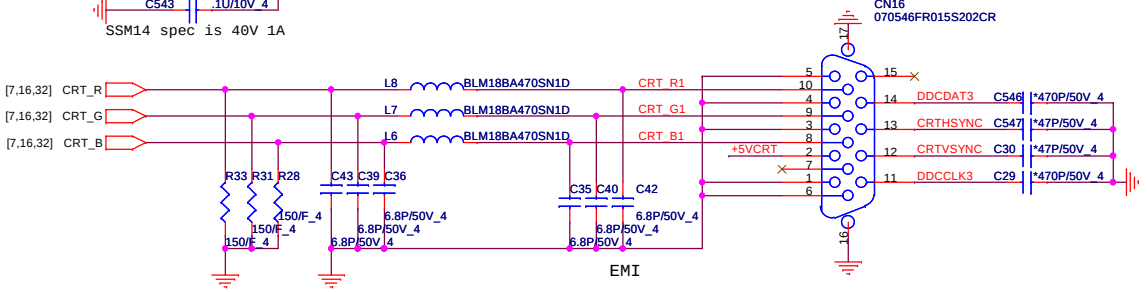
NB5

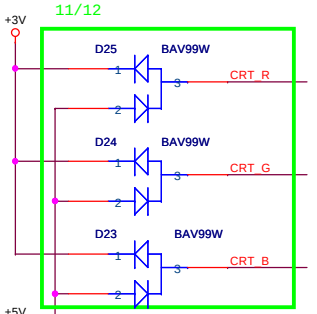
PROJECT : QL4
Quanta Computer Inc.

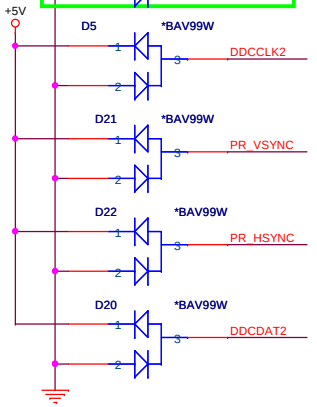
Size	Document Number	Rev
Custom	LCD CONN	E
Date: Friday, October 09, 2009	Sheet 21 of 44	

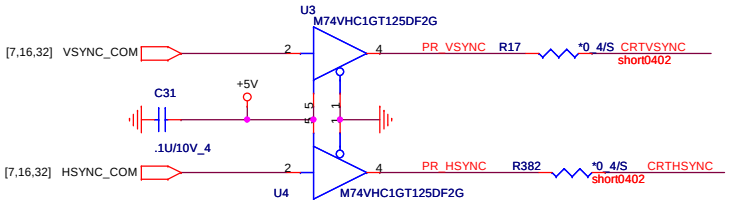
CRT PORT









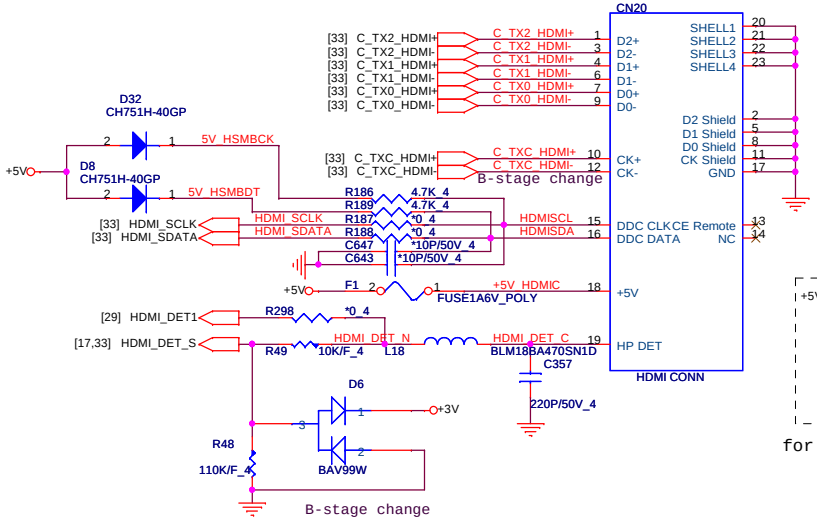


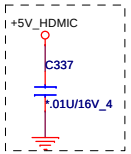
PV change,
UMA only
Not mount on Switchable

B-stage change for EMI

C_TX2_HDMI+ R616 *0_4 C_TX2_HDMI-
C_TX1_HDMI+ R618 *0_4 C_TX1_HDMI-
C_TX0_HDMI+ R617 *0_4 C_TX0_HDMI-
C_TXC_HDMI+ R619 *0_4 C_TXC_HDMI-

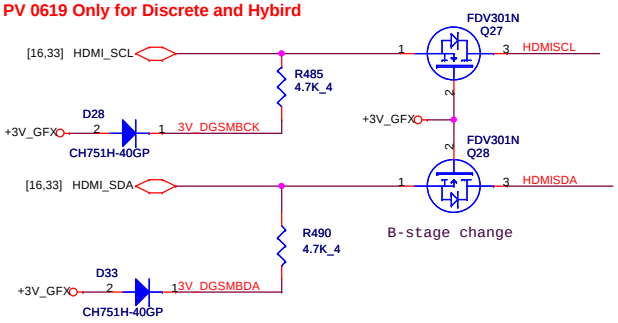
HDMI PORT





for EMI request

PV 0619 Only for Discrete and Hybird



R187 / R188 for Switchable / UMA

[2,3,7,8,9,10,11,12,13,21,23,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V
[11,24,25,27,28,30,32,40] +5V

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	E
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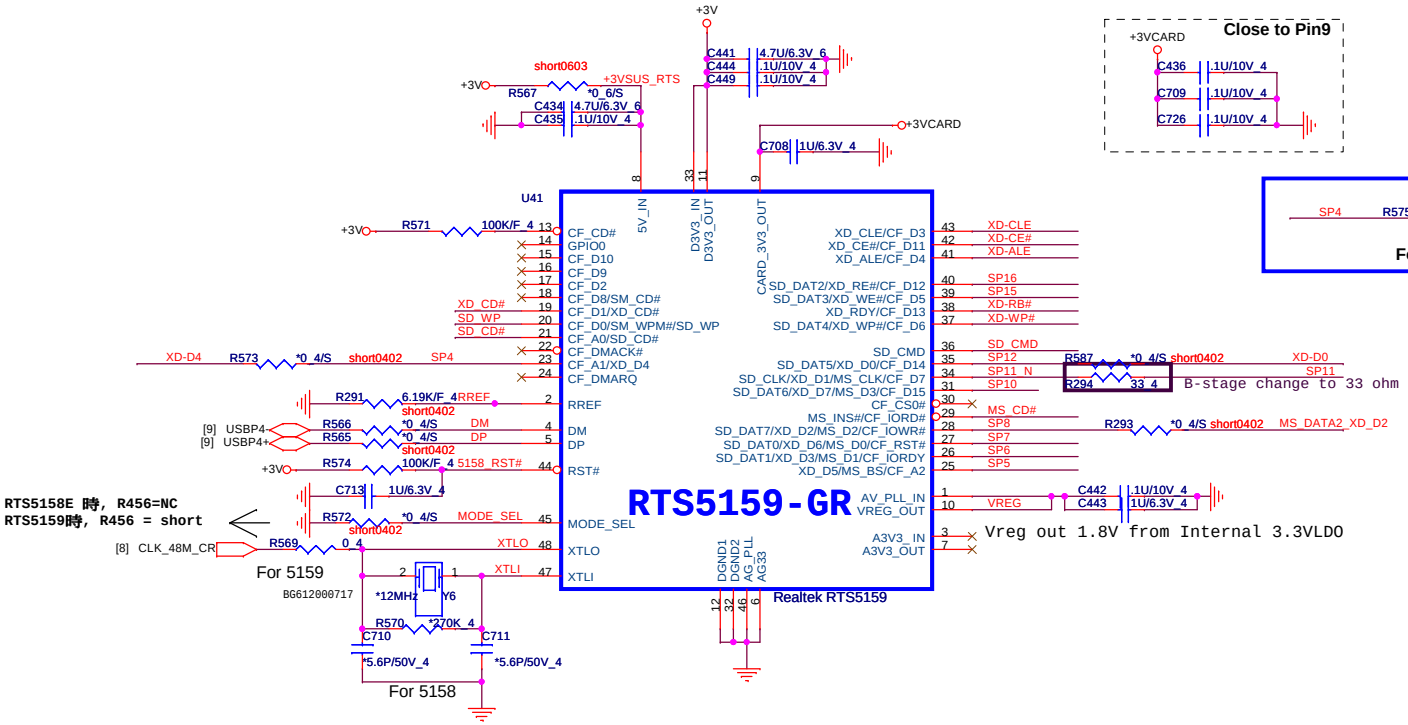
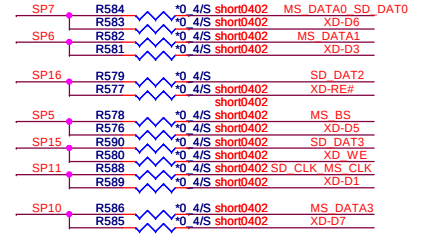


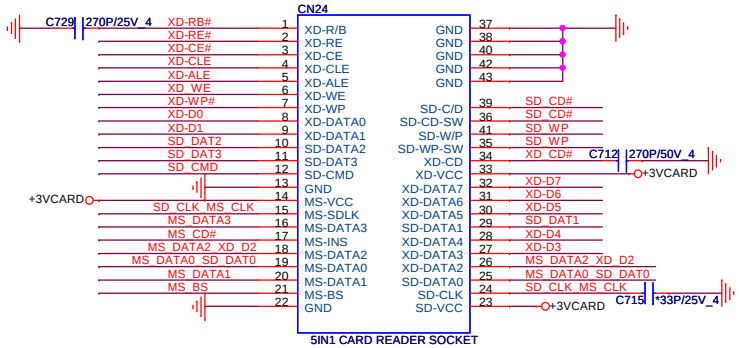
Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

For RTS5159

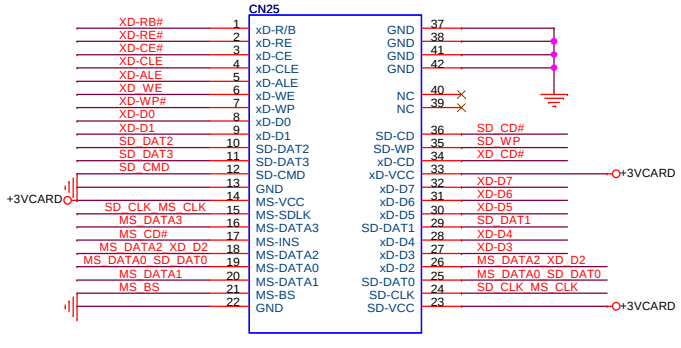


5 IN1 CARD READER
XD,MMC/SD,MS/MSP

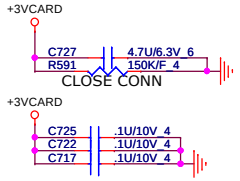


PV change footprint

DV2 add 2'nd source



PV change footprint



[2,3,7,8,9,10,11,12,13,21,22,24,25,26,27,28,29,30,31,32,33,37,40,42] +3V

NB5	PROJECT : QL4 Quanta Computer Inc.	
	Size: Custom Document Number: RTS5159 &CR SOCKET	Rev: E
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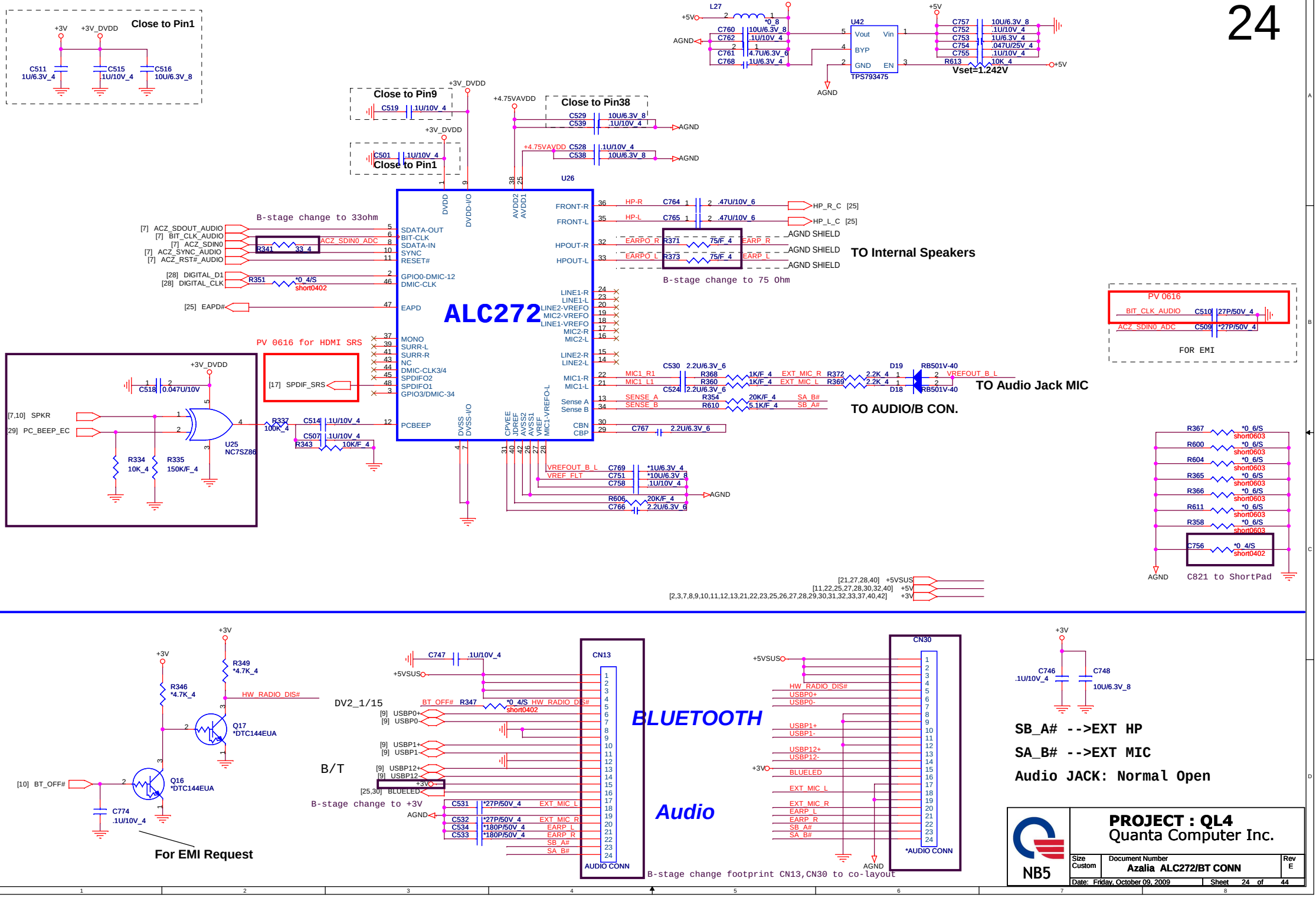
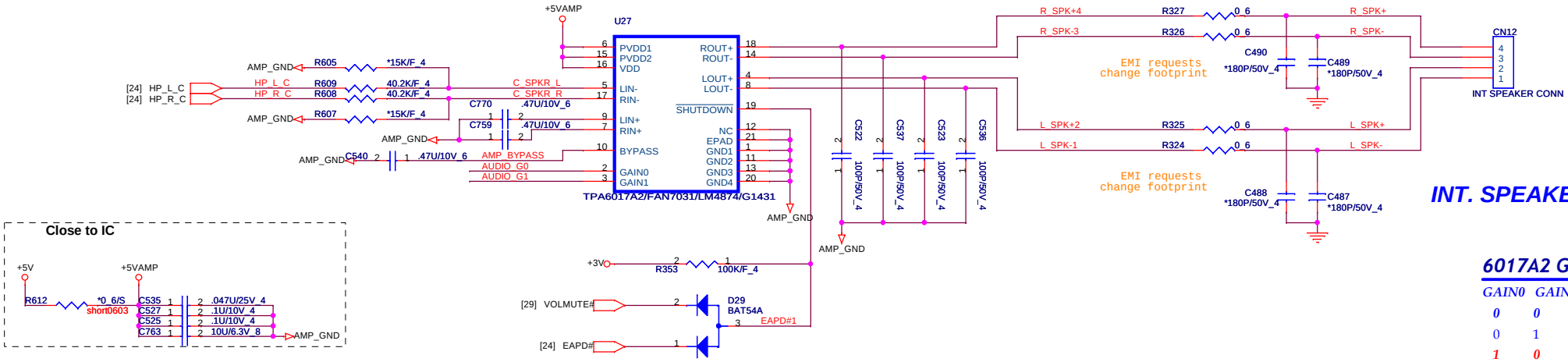
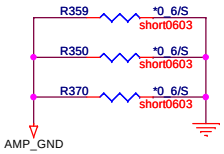

Close to Pin1
+3V
+3V_DVDD
C511 1U/6.3V_4
C515 .1U/10V_4
C516 10U/6.3V_8
+4.75VAVDD
+5V
L27 *0_8
C760 10U/6.3V_8
C762 .1U/10V_4
C761 4.7U/6.3V_6
C768 .1U/6.3V_4
AGND
U42
Vout Vin
BYP
GND EN
TPS793475
C757 10U/6.3V_8
C752 .1U/10V_4
C753 1U/6.3V_4
C754 .047U/25V_4
C755 .1U/10V_4
R613 10K_4
Vset=1.242V
Close to Pin9
C519 .1U/10V_4
Close to Pin1
C501 .1U/10V_4
Close to Pin38
C529 10U/6.3V_8
C539 .1U/10V_4
C528 1U/10V_4
C538 10U/6.3V_8
U26
DVDD
DVDD-I/O
AVDD2
AVDD1
B-stage change to 33ohm
[7] ACZ_SDOUT_AUDIO
[7] BIT_CLK_AUDIO
[7] ACZ_SDIN0
[7] ACZ_SYNC_AUDIO
[7] ACZ_RST#_AUDIO
R341 33_4
ACZ_SDIN0_ADC
SDATA-OUT
BIT-CLK
SDATA-IN
SYNC
RESET#
[28] DIGITAL_D1
[28] DIGITAL_CLK
R351 *0_4/S short0402
GPIO0-DMIC-12
DMIC-CLK
[25] EAPD#
EAPD
ALC272
FRONT-R
FRONT-L
HPOUT-R
HPOUT-L
HP-R C764 .47U/10V_6
HP-L C765 .47U/10V_6
HP_R_C [25]
HP_L_C [25]
EARPO_R R371 75/F_4 EARP_R
EARPO_L R373 75/F_4 EARP_L
AGND SHIELD
TO Internal Speakers
B-stage change to 75 0hm
LINE1-R
LINE1-L
LINE2-VREFO
MIC2-VREFO
LINE1-VREFO
MIC2-R
MIC2-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
Sense A
Sense B
CBN
CBP
C767 2.2U/6.3V_6
PV 0616
BIT_CLK_AUDIO C510 27P/50V_4
ACZ_SDIN0_ADC C509 *27P/50V_4
FOR EMI
PV 0616 for HDMI SRS
[17] SPDIF_SRS
MONO
SURR-L
SURR-R
NC
DMIC-CLK3/4
SPDIFO2
SPDIFO1
GPIO3/DMIC-34
PCBEEP
DVSS
DVSS-I/O
CPVEE
JDREF
AVSS2
AVSS1
VREF
MIC1-VREFO-L
C518 0.047U/10V
[7,10] SPKR
[29] PC_BEEP_EC
U25 NC7SZ86
R334 10K_4
R335 150K/F_4
R337 100K_4
C514 1U/10V_4
C507 1U/10V_4
R343 10K/F_4
MIC1_R1
MIC1_L1
C530 2.2U/6.3V_6
C524 2.2U/6.3V_6
R368 1K/F_4
R360 1K/F_4
EXT_MIC_R
EXT_MIC_L
R372 2.2K_4
R369 2.2K_4
D19 RB501V-40
D18 RB501V-40
VREFOUT_B_L
TO Audio Jack MIC
SENSE_A
SENSE_B
R354 20K/F_4
R610 5.1K/F_4
SA_B#
SB_A#
TO AUDIO/B CON.
VREFOUT_B_L
VREF_FLT
C769 *1U/6.3V_4
C751 *10U/6.3V_8
C758 .1U/10V_4
R606 20K/F_4
C766 2.2U/6.3V_6
R367 *0_6/S short0603
R600 *0_6/S short0603
R604 *0_6/S short0603
R365 *0_6/S short0603
R366 *0_6/S short0603
R611 *0_6/S short0603
R358 *0_6/S short0603
C756 *0_4/S short0402
C821 to ShortPad
[21,27,28,40] +5VSUS
[11,22,25,27,28,30,32,40] +5V
[2,3,7,8,9,10,11,12,13,21,22,23,25,26,27,28,29,30,31,32,33,37,40,42] +3V
R349 *4.7K_4
R346 *4.7K_4
HW_RADIO_DIS#
Q17 *DTC144EUA
Q16 *DTC144EUA
[10] BT_OFF#
C774 .1U/10V_4
For EMI Request
DV2_1/15
B/T
C747 .1U/10V_4
BT_OFF#
R347 *0_4/S short0402
[9] USBP0+
[9] USBP0-
[9] USBP1+
[9] USBP1-
[9] USBP12+
[9] USBP12-
[25,30] BLUELED
B-stage change to +3V
C531 *27P/50V_4 EXT_MIC_L
C532 *27P/50V_4 EXT_MIC_R
C534 *180P/50V_4 EARP_L
C533 *180P/50V_4 EARP_R
SB_A#
SA_B#
CN13
AUDIO CONN
BLUETOOTH
Audio
CN30
*AUDIO CONN
B-stage change footprint CN13,CN30 to co-layout
C746 .1U/10V_4
C748 10U/6.3V_8
SB_A# -->EXT HP
SA_B# -->EXT MIC
Audio JACK: Normal Open
NB5
PROJECT : QL4
Quanta Computer Inc.
Size Custom
Document Number
Azalia ALC272/BT CONN
Rev E
Date: Friday, October 09, 2009
Sheet 24 of 44

AUDIO AMPLIFIER



INT. SPEAKER

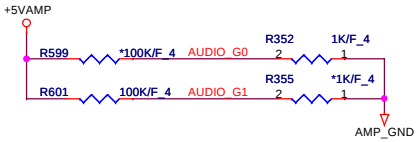
Close to IC



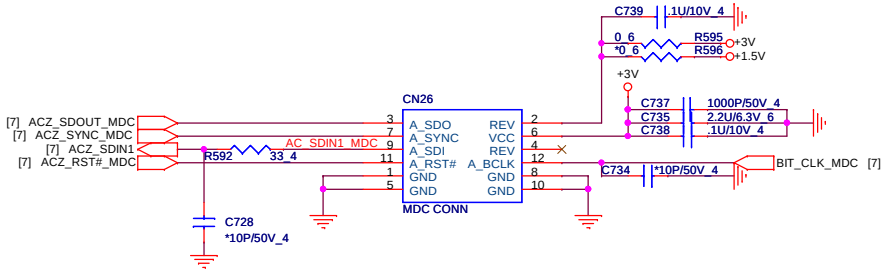
AL001431K04
AL6017A2K12
APA2031 ,AL002031K00

6017A2 Gain Table

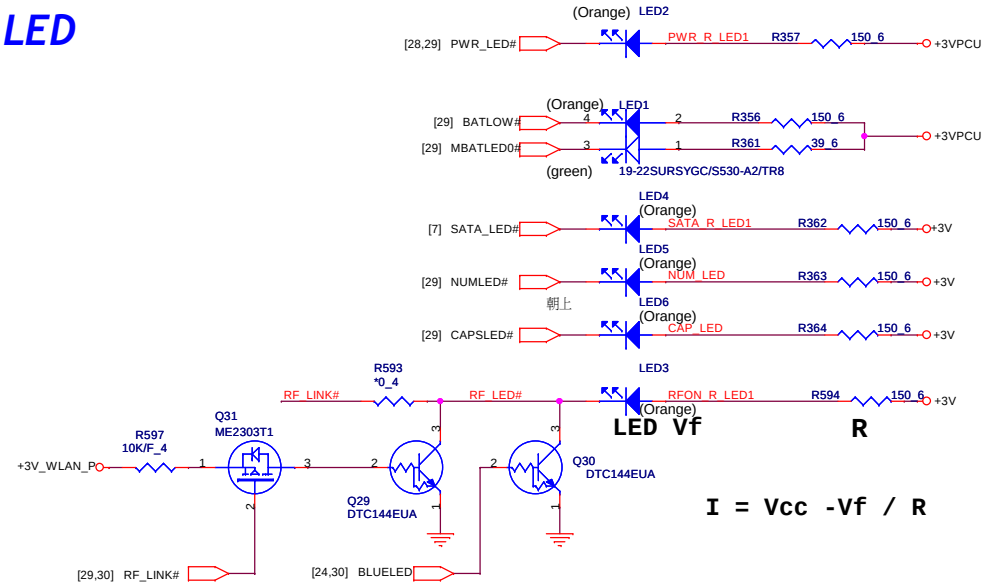
GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



MDC CONNECTOR



LED

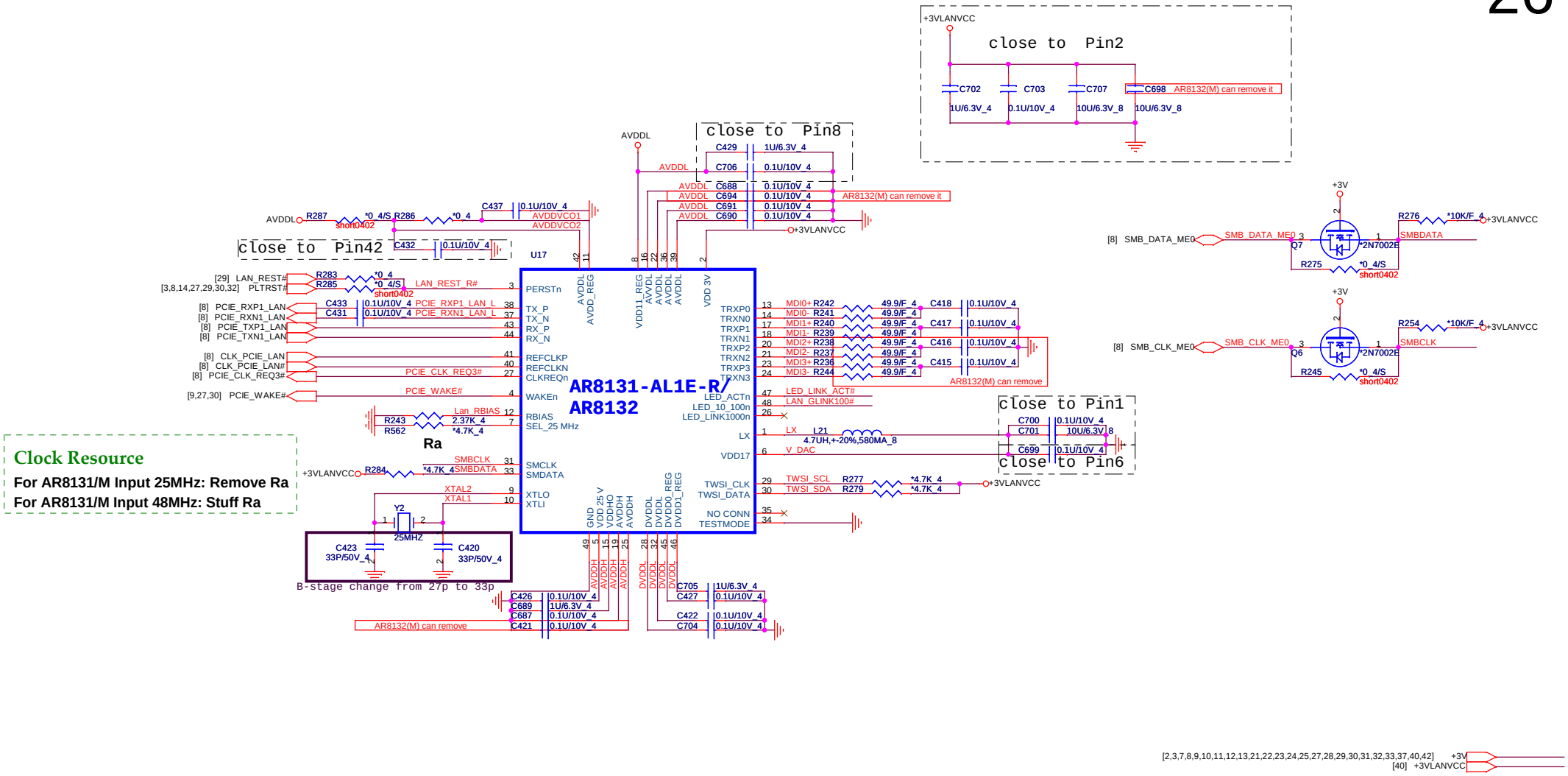


[11,22,24,27,28,30,32,40] +5V
[3,7,21,28,29,30,34,35,36,38,40,41,42] +3VPCU
[2,3,7,8,9,10,11,12,13,21,22,23,24,26,27,28,29,30,31,32,33,37,40,42] +3V

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/SPK/MDC/LED	E
Date: Friday, October 09, 2009	Sheet 25 of 44	

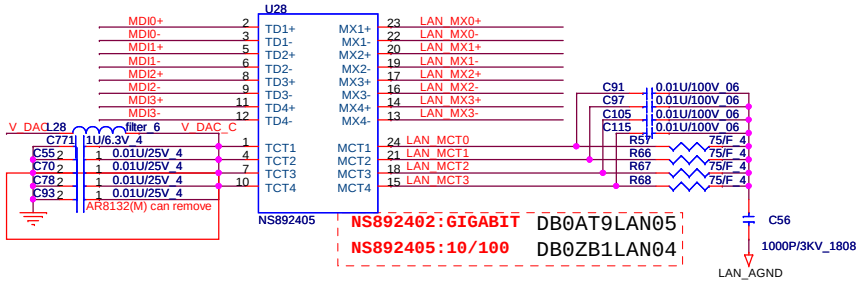


Clock Resource

For AR8131/M Input 25MHz: Remove Ra

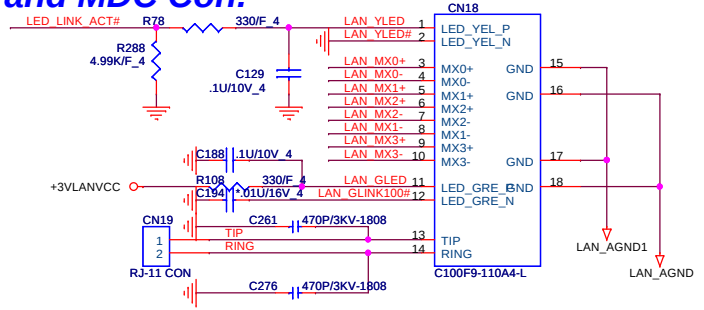
For AR8131/M Input 48MHz: Stuff Ra

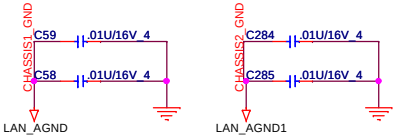
Transformer for 10/100/1000



Lan and MDC Con.

RJ45





NB5

PROJECT : QL4
Quanta Computer Inc.

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Custom	AR8131(M)/RJ45	E
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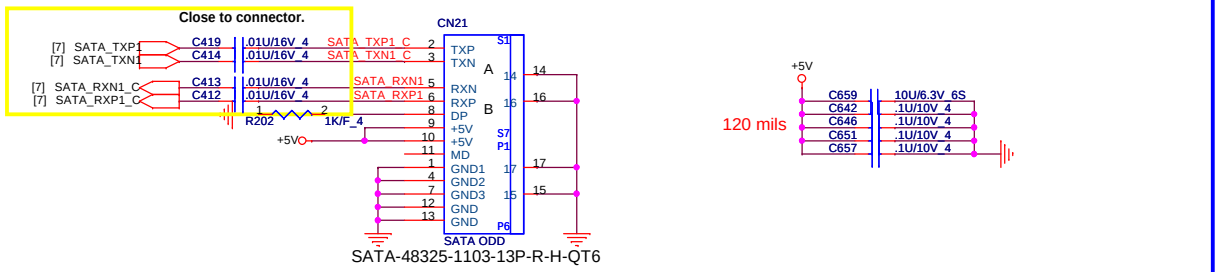
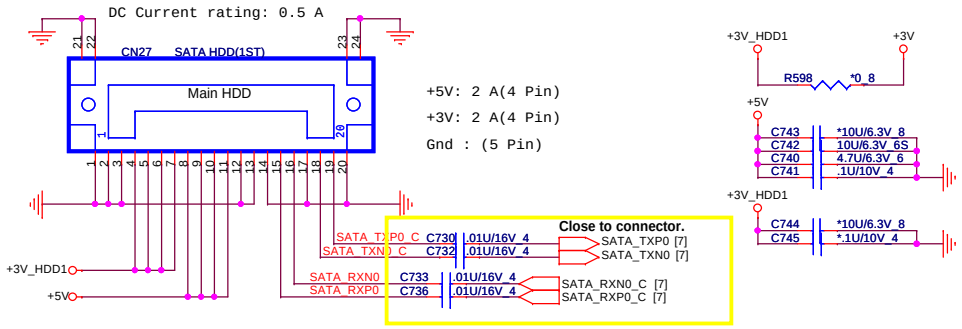
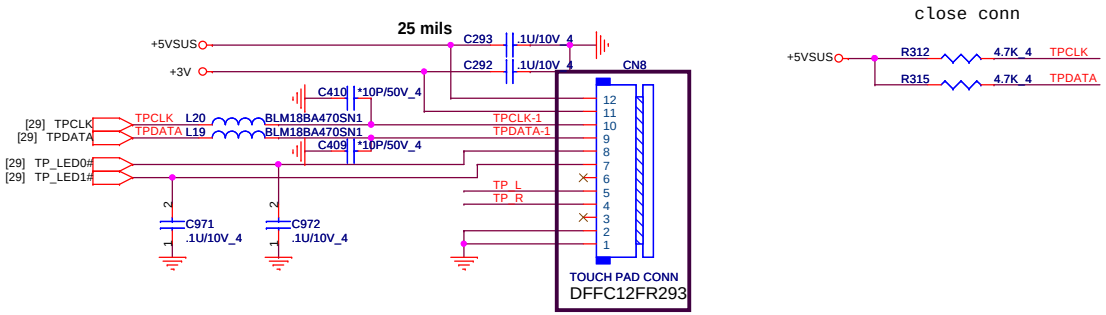
SATA ODD



SATA_1 CONNECTOR

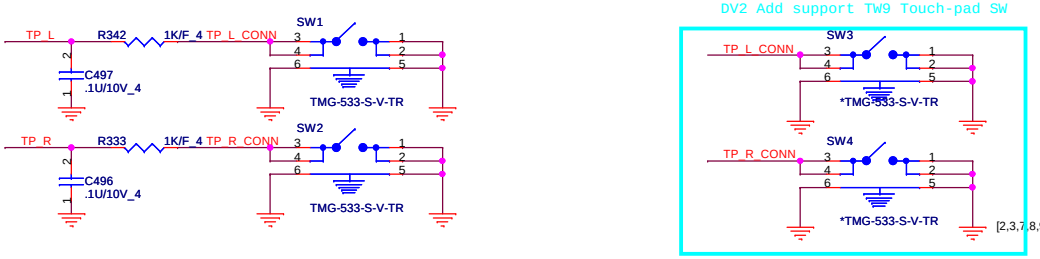


TOUCH PAD CONNECTOR



B-stage change footprint to BL121-12R-TAND-12P-L

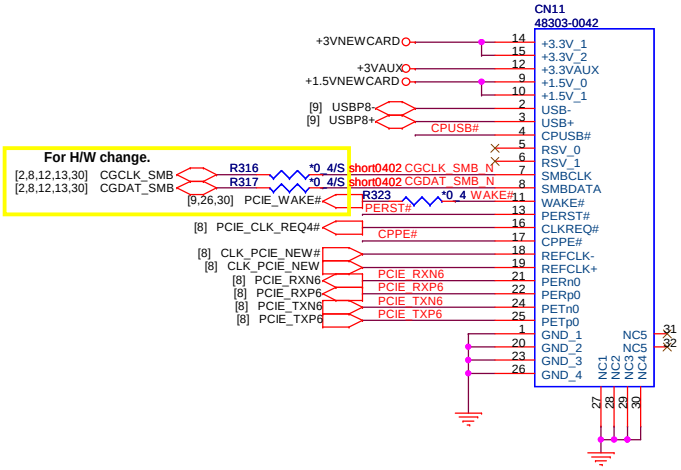
TOUCH PAD L/R SW1,SW2 in QL4 use, SW3,SW4 in TW9 use



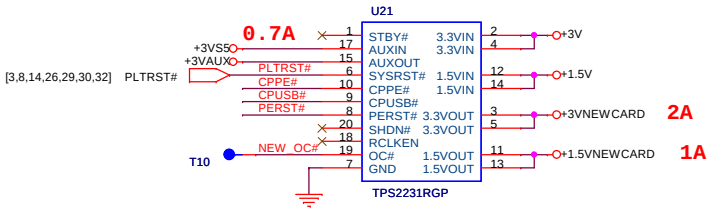
NEWCARD

NEWCARD (PCIEXPRESS*1 + USB*1)

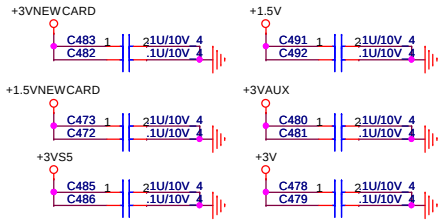
27



Change CN15#31,32 as ME request for Hole pad
expcard-48303-0042-26p-l-qt6 as ME modify Pad size(pin31,32)
Move CN15#29,30 Pin as ME request(Molex confirm drawing)



Change net name from 3V_NEWAUX to 3VAUX



[25,30,40] +1.5V
[2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,28,29,30,31,32,33,37,40,42] +3V
[11,22,24,25,28,30,32,40] +5V
[21,24,28,40] +5VSUS

NB5

PROJECT : QL4
Quanta Computer Inc.

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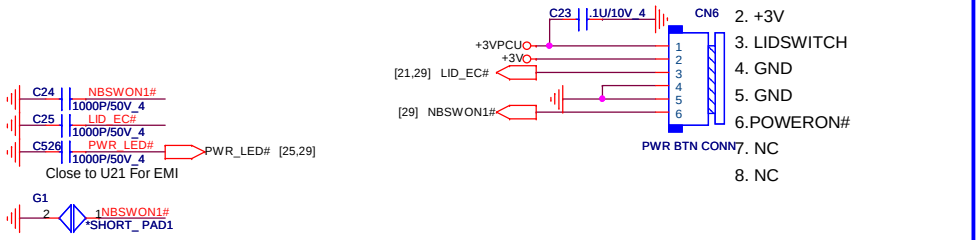
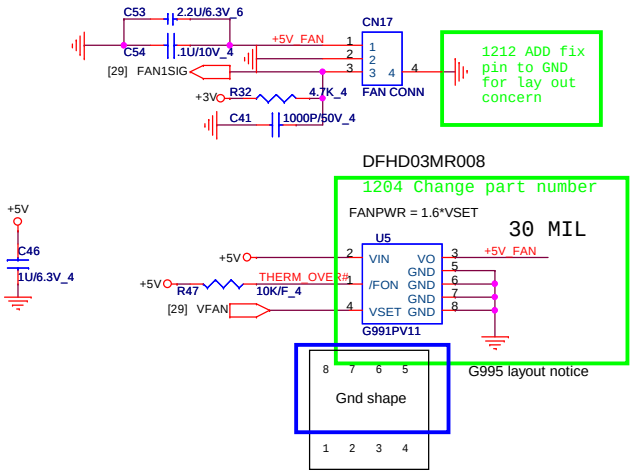
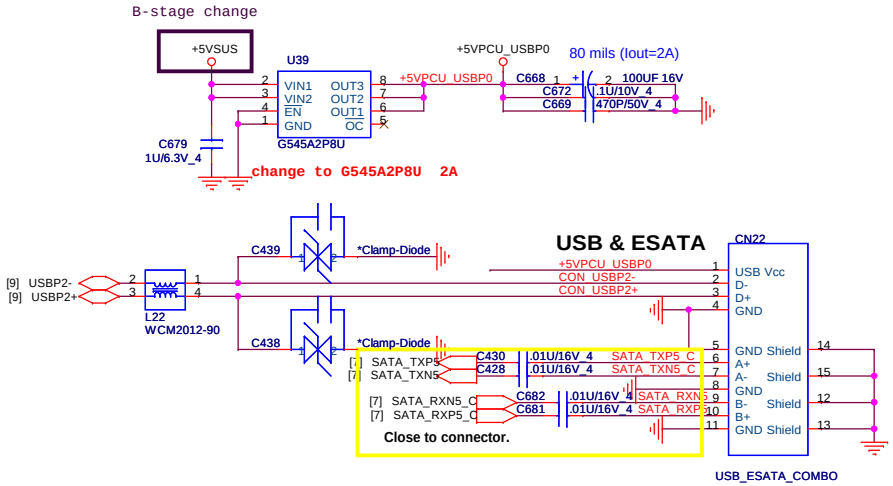
POWER BOTTON CONNECT



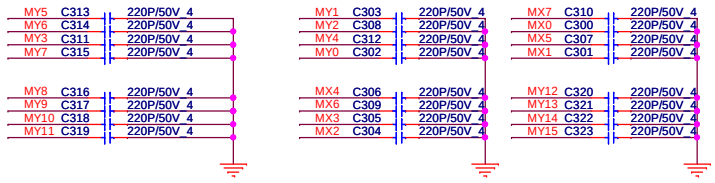
CPU FAN



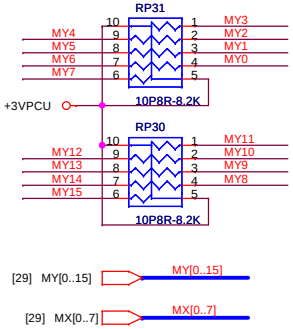
E-SATA/USB COMBO

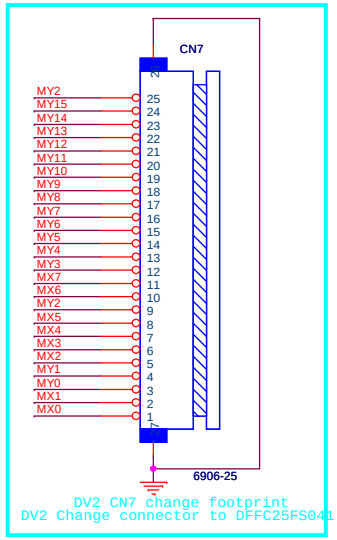


KEYBOARD Con.

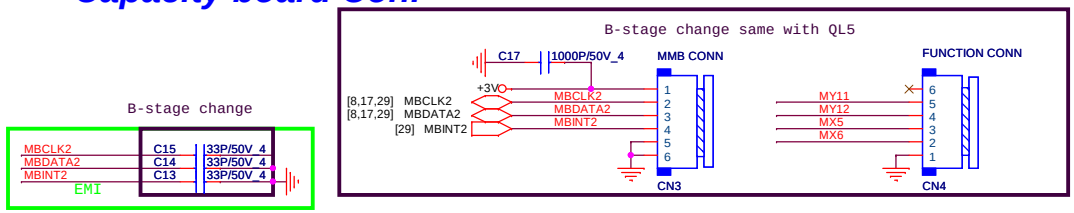


KEYBOARD PULL-UP

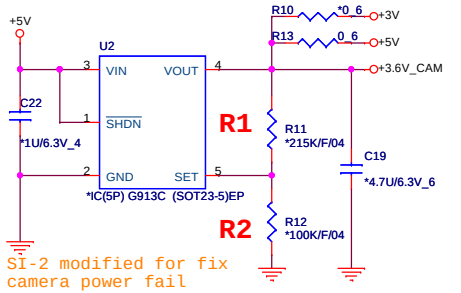


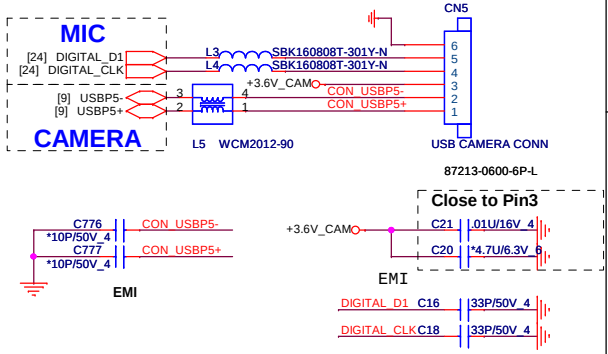


Capacity board Con.



USB CAMERA POWER





[11,22,24,25,27,30,32,40] +5V
[2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,29,30,31,32,33,37,40,42] +3V
[3,7,21,25,29,30,34,35,36,38,40,41,42] +3VPCU
[29,34,35,36,37,38,39,40] +5VPCU

NB5

PROJECT : QL4
Quanta Computer Inc.

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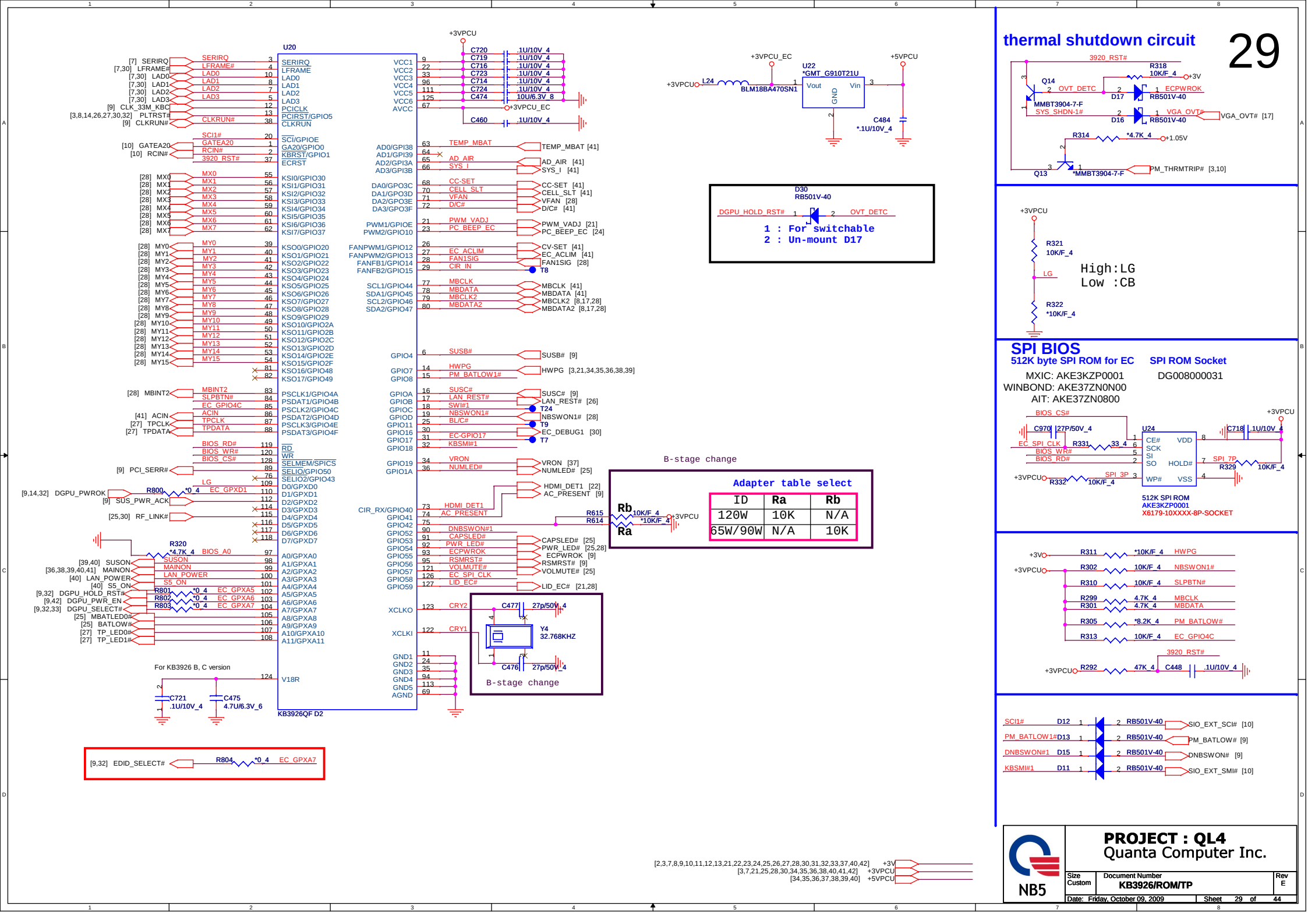
U20
KB3926QF D2
SERIRQ
LFRAME
LAD0
LAD1
LAD2
LAD3
PCICLK
PCIRST/GPIO5
CLKRUN
SCI/GPIOE
GA20/GPIO0
KBRST/GPIO1
ECRST
VCC1
VCC2
VCC3
VCC4
VCC5
VCC6
AVCC
+3VPCU
+3VPCU_EC
C720 .1U/10V_4
C719 .1U/10V_4
C716 .1U/10V_4
C723 .1U/10V_4
C714 .1U/10V_4
C724 .1U/10V_4
C474 10U/6.3V_8
C460 .1U/10V_4
TEMP_MBAT
AD_AIR
SYS_I
CC-SET
CELL_SLT
VFAN
D/C#
PWM_VADJ
PC_BEEP_EC
CV-SET
EC_ACLIM
FAN1SIG
CIR_IN
T8
MBCLK
MBDATA
MBCLK2
MBDATA2
SUSB#
HWPG
PM_BATLOW1#
SUSC#
LAN_REST#
SWI#1
T24
NBSWON1#
BL/C#
T9
EC_DEBUG1
EC-GPIO17
T7
KBSMI#1
VRON
NUMLED#
HDMI_DET1
AC_PRESENT
DNBSWON#1
CAPSLED#
PWR_LED#
ECPWROK
RSMRST#
VOLMUTE#
EC_SPI_CLK
LID_EC#
CRY2
CRY1
C477 27p/50V_4
Y4
32.768KHZ
C476 27p/50V_4
B-stage change
V18R
For KB3926 B, C version
C721 .1U/10V_4
C475 4.7U/6.3V_6
R320 *4.7K_4 BIOS_A0
R800 *0_4 EC_GPXD1
R801 *0_4 EC_GPXA5
R802 *0_4 EC_GPXA6
R803 *0_4 EC_GPXA7
R804 *0_4 EC_GPXA7
R615 10K/F_4
R614 *10K/F_4
Rb
Ra
Adapter table select
ID | Ra | Rb
120W | 10K | N/A
65W/90W | N/A | 10K
U22
*GMT_G910T21U
Vout
Vin
GND
L24
BLM18BA470SN1
C484 *.1U/10V_4
+5VPCU
D30
RB501V-40
DGPU_HOLD_RST#
OVT_DETC
1 : For switchable
2 : Un-mount D17
High:LG
Low :CB
R321 10K/F_4
R322 *10K/F_4
LG
thermal shutdown circuit
3920_RST#
R318 10K/F_4
+3V
Q14
MMBT3904-7-F
SYS_SHDN-1#
ECPWROK
VGA_OVT#
D17
D16
RB501V-40
R314 *4.7K_4
+1.05V
Q13
*MMBT3904-7-F
PM_THRMTRIP# [3,10]
SPI BIOS
512K byte SPI ROM for EC
SPI ROM Socket
MXIC: AKE3KZP0001
WINBOND: AKE37ZN0N00
AIT: AKE37ZN0800
DG008000031
BIOS_CS#
C970 27P/50V_4
EC_SPI_CLK
R331 33_4
BIOS_WR#
BIOS_RD#
SPI_3P
R332 10K/F_4
U24
CE#
SCK
SI
SO
WP#
VDD
HOLD#
VSS
C718 .1U/10V_4
SPI_7P
R329 10K/F_4
512K SPI ROM
AKE3KZP0001
X6179-10XXXX-8P-SOCKET
R311 *10K/F_4 HWPG
R302 10K/F_4 NBSWON1#
R310 10K/F_4 SLPBTN#
R299 4.7K_4 MBCLK
R301 4.7K_4 MBDATA
R305 *8.2K_4 PM_BATLOW#
R313 10K/F_4 EC_GPIO4C
3920_RST#
R292 47K_4
C448 .1U/10V_4
SCI1# D12 RB501V-40 SIO_EXT_SCI# [10]
PM_BATLOW1# D13 RB501V-40 PM_BATLOW# [9]
DNBSWON#1 D15 RB501V-40 DNBSWON# [9]
KBSMI#1 D11 RB501V-40 SIO_EXT_SMI# [10]
[2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,30,31,32,33,37,40,42] +3V
[3,7,21,25,28,30,34,35,36,38,40,41,42] +3VPCU
[34,35,36,37,38,39,40] +5VPCU
PROJECT : QL4
Quanta Computer Inc.
NB5
Size Custom
Document Number KB3926/ROM/TP
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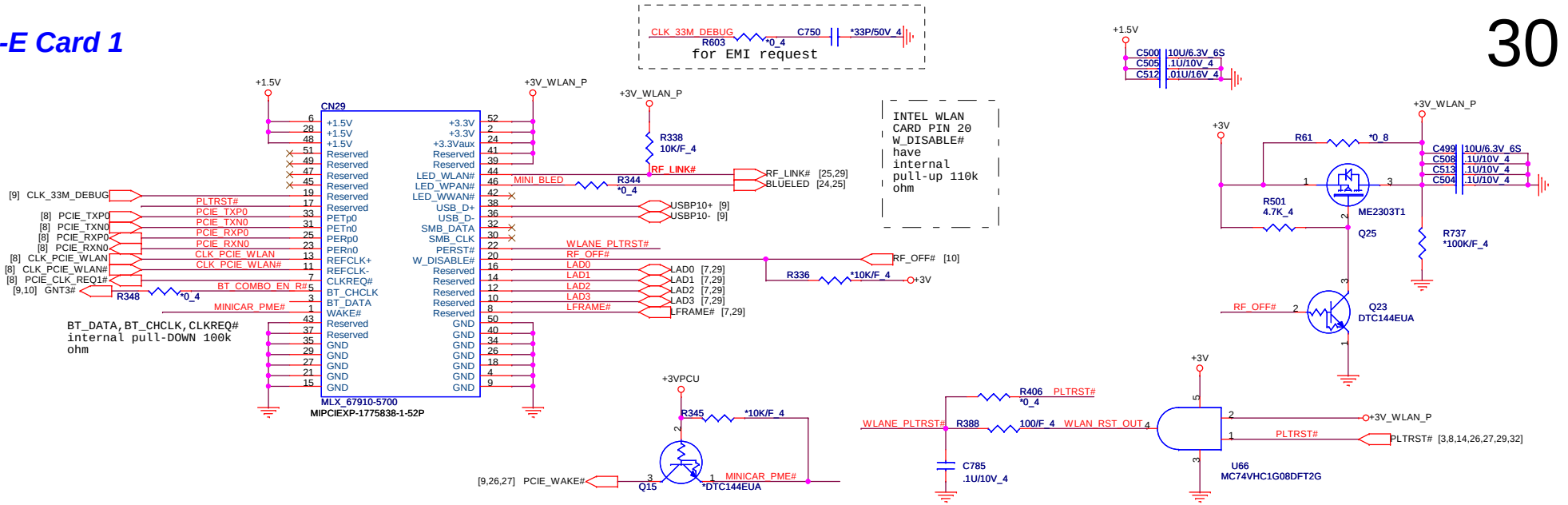
29

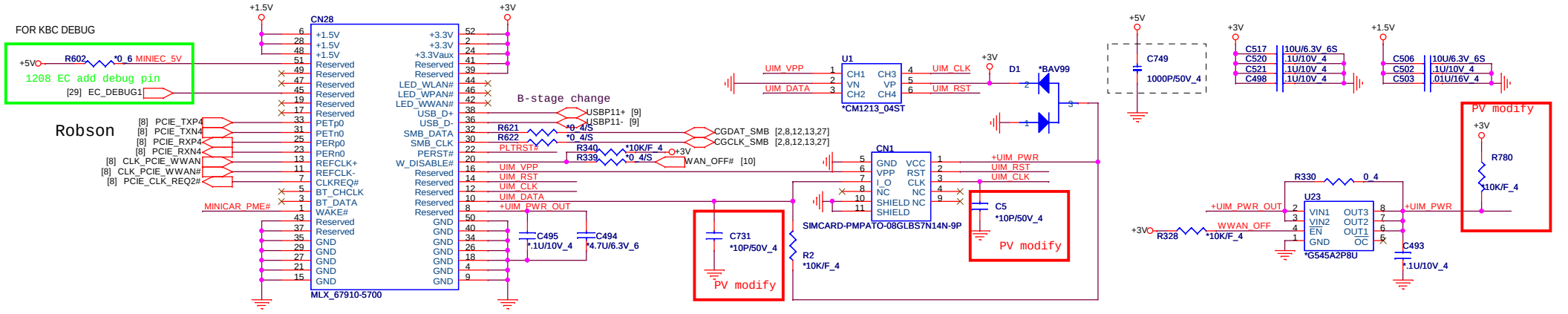
Mini PCI-E Card 1

WLAN



Mini PCI-E Card 2

WWAN& Robson



[25,27,40] +1.5V
[2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,31,32,33,37,40,42] +3V
[3,7,21,25,28,29,34,35,36,38,40,41,42] +3VPCU
[11,22,24,25,27,28,32,40] +5V

NB5	PROJECT : QL4 Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN X2	Rev: E
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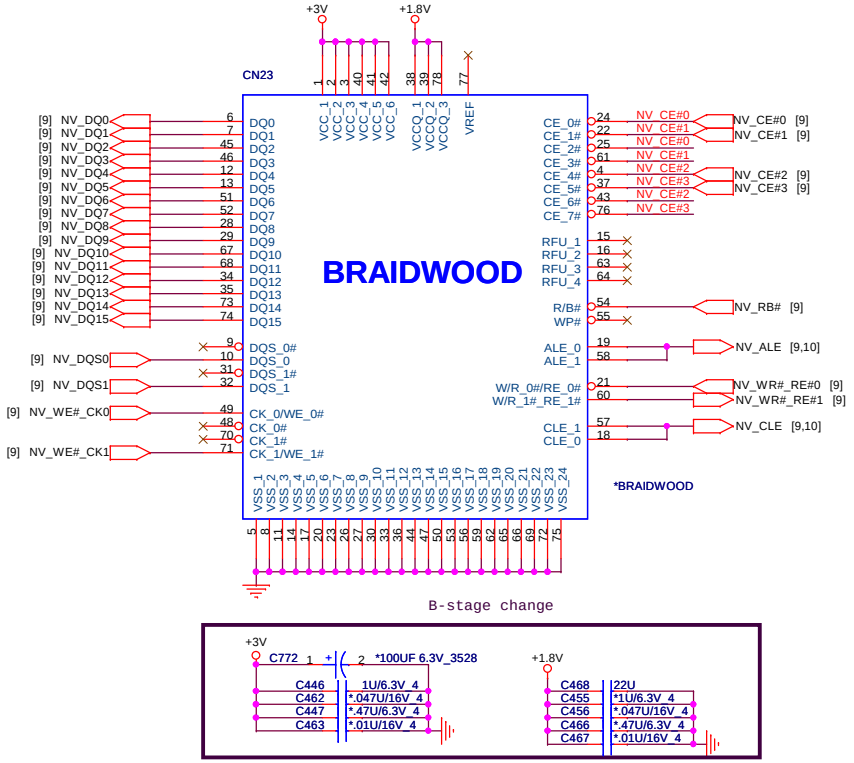
PV 0616 DEL debug Con.



PV 0616 DEL debug Con.

[3,5,10,11,34,38] +1.1V_VTT
[2,7,8,9,11,29,34,36,42] +1.05V
[5,10,11,36,40,42] +1.8V
[2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,32,33,37,40,42] +3V
[8,9,10,11,14,27,40] +3VS5

NB5

PROJECT : QL4
Quanta Computer Inc.

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Custom	XDP/BRAIDWOOD	E
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LVDS Channel Switch

DGPU_Channel-A/B

U38

[16,21] EXT_TXUCLKOUT+
[16,21] EXT_TXUCLKOUT-
[16,21] EXT_TXUOUT2+
[16,21] EXT_TXUOUT2-
[16,21] EXT_TXUOUT1+
[16,21] EXT_TXUOUT1-
[16,21] EXT_TXUOUT0+
[16,21] EXT_TXUOUT0-
[16,21] EXT_TXLCLKOUT+
[16,21] EXT_TXLCLKOUT-
[16,21] EXT_TXLOUT2+
[16,21] EXT_TXLOUT2-
[16,21] EXT_TXLOUT1+
[16,21] EXT_TXLOUT1-
[16,21] EXT_TXLOUT0+
[16,21] EXT_TXLOUT0-
[17] LVDS_BLON_DGPU
[17] DISP_ON_DGPU

0B1 1B1 2B1 3B1 4B1 5B1 6B1 7B1 8B1 9B1 10B1 11B1 12B1 13B1 14B1 15B1 16B1 17B1 18B1 19B1

VDD ×8
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9
SEL1 OE1#

DGPU_SELECT#

PI3LVD1012

IGPU_Channel-A /B

[7,21] LB_CLK
[7,21] LB_CLK#
[7,21] LB_DATAP2
[7,21] LB_DATAN2
[7,21] LB_DATAP1
[7,21] LB_DATAN1
[7,21] LB_DATAP0
[7,21] LB_DATAN0
[7,21] LA_CLK
[7,21] LA_CLK#
[7,21] LA_DATAP2
[7,21] LA_DATAN2
[7,21] LA_DATAP1
[7,21] LA_DATAN1
[7,21] LA_DATAP0
[7,21] LA_DATAN0
[7] LVDS_BLON_PCH
[7] DISP_ON_PCH

0B2 1B2 2B2 3B2 4B2 5B2 6B2 7B2 8B2 9B2 10B2 11B2 12B2 13B2 14B2 15B2 16B2 17B2 18B2 19B2

A10 A11 A12 A13 A14 A15 A16 A17 A18 A19
SEL2 OE2#

DGPU_SELECT# [9,29,33]

GND ×9

+3V

C941 0.1U/10V_4
C942 0.1U/10V_4
C943 0.1U/10V_4
C944 0.1U/10V_4

To LVDS Conn.

TXUCLKOUT+ [21]
TXUCLKOUT- [21]
TXUOUT2+ [21]
TXUOUT2- [21]
TXUOUT1+ [21]
TXUOUT1- [21]
TXUOUT0+ [21]
TXUOUT0- [21]

BKLTCTL_PWM

To LVDS Conn.

TXLCLKOUT+ [21]
TXLCLKOUT- [21]
TXLOUT2+ [21]
TXLOUT2- [21]
TXLOUT1+ [21]
TXLOUT1- [21]
TXLOUT0+ [21]
TXLOUT0- [21]
LVDS_BLON [7,17,21]
DISP_ON [7,17,21]

BKLTEN / LVDDEN

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

SELx	Ay
LOW	B1
HIGH	B2

+3V
R787 2.2K_4 DDCCLK_PCH
R786 2.2K_4 DDCDATA_PCH

LVDS_BLON_PCH R758 100K/F_4
DISP_ON_PCH R759 100K/F_4
LVDS_BLON_DGPU R791 100K/F_4
DISP_ON_DGPU R790 100K/F_4

LVDS/CRT DDC Switch

U59

[17] EDIDCLK_DGPU
[7] EDIDCLK_PCH
[17] EDIDDATA_DGPU
[7] EDIDDATA_PCH
[16] DDCCLK_DGPU
[7] DDCCLK_PCH
[16] DDCDATA_DGPU
[7] DDCDATA_PCH
[9,29] EDID_SELECT#

IA0 IA1 IB0 IB1 IC0 IC1 ID0 ID1 SEL /E
YA YB YC YD
VCC GND

74CBT3257

EDIDCLK [7,17,21]
EDIDDATA [7,17,21]
DDCCLK [7,16,22]
DDCDATA [7,16,22]

+5V
C939 .1U/10V_4

VGA SWITCH

U62

[16] CRT_R_DGPU
[16] CRT_G_DGPU
[16] CRT_B_DGPU
[16] HSYNC_DGPU
[16] VSYNC_DGPU
[7] CRT_R_PCH
[7] CRT_G_PCH
[7] CRT_B_PCH
[7] HSYNC_PCH
[7] VSYNC_PCH

IA0 IB0 IC0 ID0 IE0
IA1 IB1 IC1 ID1 IE1
SEL
YA YB YC YD YE
GND ×4
VDD3 ×4

DGPU_SELECT#

CRT_R [7,16,22]
CRT_G [7,16,22]
CRT_B [7,16,22]
HSYNC_COM [7,16,22]
VSYNC_COM [7,16,22]

PI3V512

+3V
C946 .1U/10V_4
C947 .1U/10V_4

S	Yn
0	B0
1	B1

C965 .1U/10V_4

U65

VCC S B0 YA B1 GND

[17] DPST_PWM_DGPU
[7] DPST_PWM_PCH
DPST_PWM

PWM_SELECT# [9]
DPST_PWM [7,17,21]

74LVC1G3157GW

+1.05V_GFX R742 4.7K_4 DGPU_POK2 Q67 MMBT3904-7-F C960 *1000P/50V_4
+1.8V_VGA R746 4.7K_4 DGPU_POK4 Q70 MMBT3904-7-F C963 *1000P/50V_4
+1.5V_GFX R745 4.7K_4 DGPU_POK3 Q69 MMBT3904-7-F C961 *1000P/50V_4

DGPU_PGOK-1

+3V R744 4.7K_4
+3V_GFX R747 4.7K_4
Q71 MMBT3904-7-F
R736 100K/F_4
C964 *1000P/50V_4

DGPU_PWROK [9,14,29]

U63 MC74VHC1G08DFT2G

[3,8,14,26,27,29,30] PLTRST#
[9,29] DGPU_HOLD_RST#
R806 330/F_4 DGPU_HIN_RST#

PEGX_RST# [14]
R733 100K/F_4

DGPU_PGOK-1
Q73 *MMBT3904-7-F

C948 .1U/10V_4

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI Switch / Power CRTL	E
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DGPU_HDMI

[16] H_TXC_HDMI+ — C374 .1U/10V_4 — DGPU_TXC_HDMI+
[16] H_TXC_HDMI- — C360 .1U/10V_4 — DGPU_TXC_HDMI-
[16] H_TX0_HDMI+ — C386 .1U/10V_4 — DGPU_TX0_HDMI+
[16] H_TX0_HDMI- — C381 .1U/10V_4 — DGPU_TX0_HDMI-
[16] H_TX1_HDMI+ — C401 .1U/10V_4 — DGPU_TX1_HDMI+
[16] H_TX1_HDMI- — C393 .1U/10V_4 — DGPU_TX1_HDMI-
[16] H_TX2_HDMI+ — C403 .1U/10V_4 — DGPU_TX2_HDMI+
[16] H_TX2_HDMI- — C408 .1U/10V_4 — DGPU_TX2_HDMI-

HDMISwitch

U64 — PI3HDMI201

DGPU_TXC_HDMI- 55 — CLK-A
DGPU_TXC_HDMI+ 56 — CLK+A
DGPU_TX0_HDMI- 2 — D0-A
DGPU_TX0_HDMI+ 3 — D0+A
DGPU_TX1_HDMI- 5 — D1-A
DGPU_TX1_HDMI+ 6 — D1+A
DGPU_TX2_HDMI- 8 — D2-A
DGPU_TX2_HDMI+ 9 — D2+A

+3V → 48, 41, 35, 19, 13, 7, 1 (VDD)

HPD_SINK 47 — HDMI_DET_S — HDMI_DET_S [17,22]
SDA_SINK 46 — HDMI_SDATA [22]
SCL_SINK 45 — HDMI_SCLK [22]

[17] HDMI_DET — 51 HPDA
[16,22] HDMI_SDA — 52 SDAA
[16,22] HDMI_SCL — 53 SCLA
[7] HDMI_HPD_CON — 23 HPDB
[7] SDVO_DATA — 24 SDAB
[7] SDVO_CLK — 25 SCLB

CLK- 43 — C_TXC_HDMI- [22]
CLK+ 42 — C_TXC_HDMI+ [22]
D0- 40 — C_TX0_HDMI- [22]
D0+ 39 — C_TX0_HDMI+ [22]
D1- 37 — C_TX1_HDMI- [22]
D1+ 36 — C_TX1_HDMI+ [22]
D2- 34 — C_TX2_HDMI- [22]
D2+ 33 — C_TX2_HDMI+ [22]

PAD_GND 57
GND 4, 10, 16, 22, 32, 38, 44, 54

To HDMI Conn.

[7] IN_CLK# — 11 CLK-B
[7] IN_CLK — 12 CLK+B
[7] IN_D0# — 14 D0-B
[7] IN_D0 — 15 D0+B
[7] IN_D1# — 17 D1-B
[7] IN_D1 — 18 D1+B
[7] IN_D2# — 20 D2-B
[7] IN_D2 — 21 D2+B

EQ_S1 — 26 — HSW_EQS1
EQ_S0 — 28 — HSW_EQS0
OC_S2 — 29 — HSW_OCS2
OC_S1 — 30 — HSW_OCS1
OC_S0 — 31 — HSW_OCS0
OE — 50 — HSW_ON#
SEL2 — 27 — HSW_SEL2
SEL1 — 49 — HSW_SEL1

IGPU_HDMI

+3V
R507 2.2K/F_4 SDVO_DATA
R508 2.2K/F_4 SDVO_CLK

+3V
C955 0.1U/10V_4
C954 0.1U/10V_4
C945 0.1U/10V_4
C950 0.1U/10V_4

OC SETTING
S2 S1 S0 = 1 : 1 : 1 500mV 0dB Defualt
S2 S1 S0 = 1 : 1 : 0 750mV 0dB
S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
S2 S1 S0 = 1 : 0 : 0 600mV 0dB
S2 S1 S0 = 0 : 1 : 1 500mV 0dB
S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
S2 S1 S0 = 0 : 0 : 0 500mV 6dB

EQ SETTING
S1 S0 = 1 : 1 3dB Defualt
S1 S0 = 1 : 0 8dB
S1 S0 = 0 : 1 3dB
S1 S0 = 0 : 0 15dB

OE#	SEL2	SEL1	Ay
0	X	1	A
0	1	0	B

HSW_EQS1 R629 *4.7K_4
HSW_EQS0 R628 *4.7K_4
HSW_OCS2 R627 *4.7K_4
HSW_OCS1 R626 *4.7K_4
HSW_OCS0 R624 *4.7K_4
HSW_ON# R623 4.7K_4

+3V
R630 4.7K_4
HSW_SEL1
R793 *4.7K_4
Q33 DTC144EUA
DGPU_SELECT# — DGPU_SELECT# [9,29,32]
R631 0_4 HSW_SEL2
R794 *4.7K_4
+3V

Mount R793 and R794 for UMA only

Only for NVIDIA

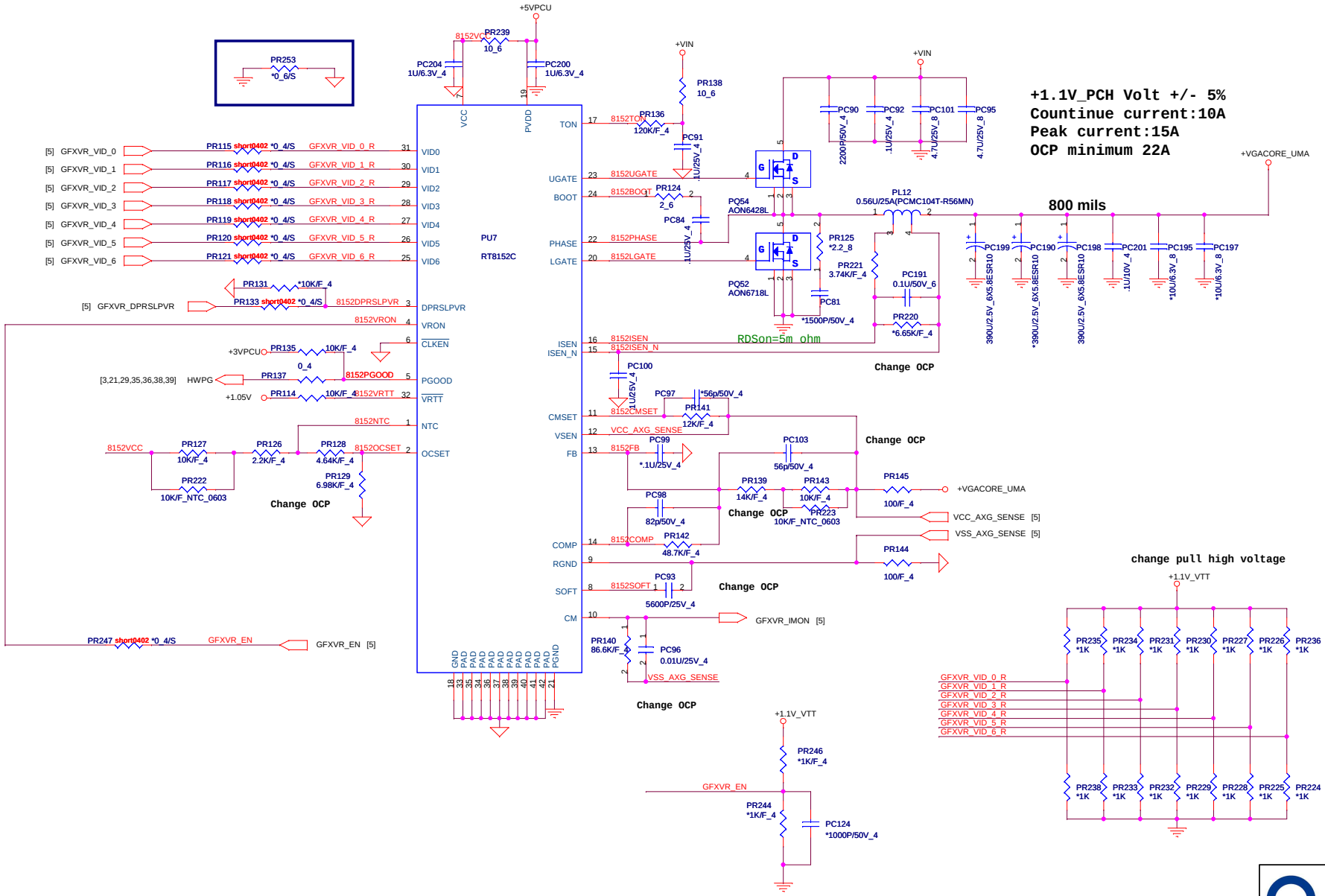
+3V_GFX
Q26 2N7002E

R493 499/F_4 DGPU_TXC_HDMI+
R495 499/F_4 DGPU_TXC_HDMI-
R488 499/F_4 DGPU_TX0_HDMI+
R486 499/F_4 DGPU_TX0_HDMI-
R483 499/F_4 DGPU_TX1_HDMI+
R481 499/F_4 DGPU_TX1_HDMI-
R478 499/F_4 DGPU_TX2_HDMI+
R475 499/F_4 DGPU_TX2_HDMI-

DGPU_TXC_HDMI- RP19 0_4P2R C_TXC_HDMI-
DGPU_TXC_HDMI+ C_TXC_HDMI+
DGPU_TX0_HDMI- RP18 0_4P2R C_TX0_HDMI-
DGPU_TX0_HDMI+ C_TX0_HDMI+
DGPU_TX1_HDMI- RP20 0_4P2R C_TX1_HDMI-
DGPU_TX1_HDMI+ C_TX1_HDMI+
DGPU_TX2_HDMI+ RP17 0_4P2R C_TX2_HDMI+
DGPU_TX2_HDMI- C_TX2_HDMI-

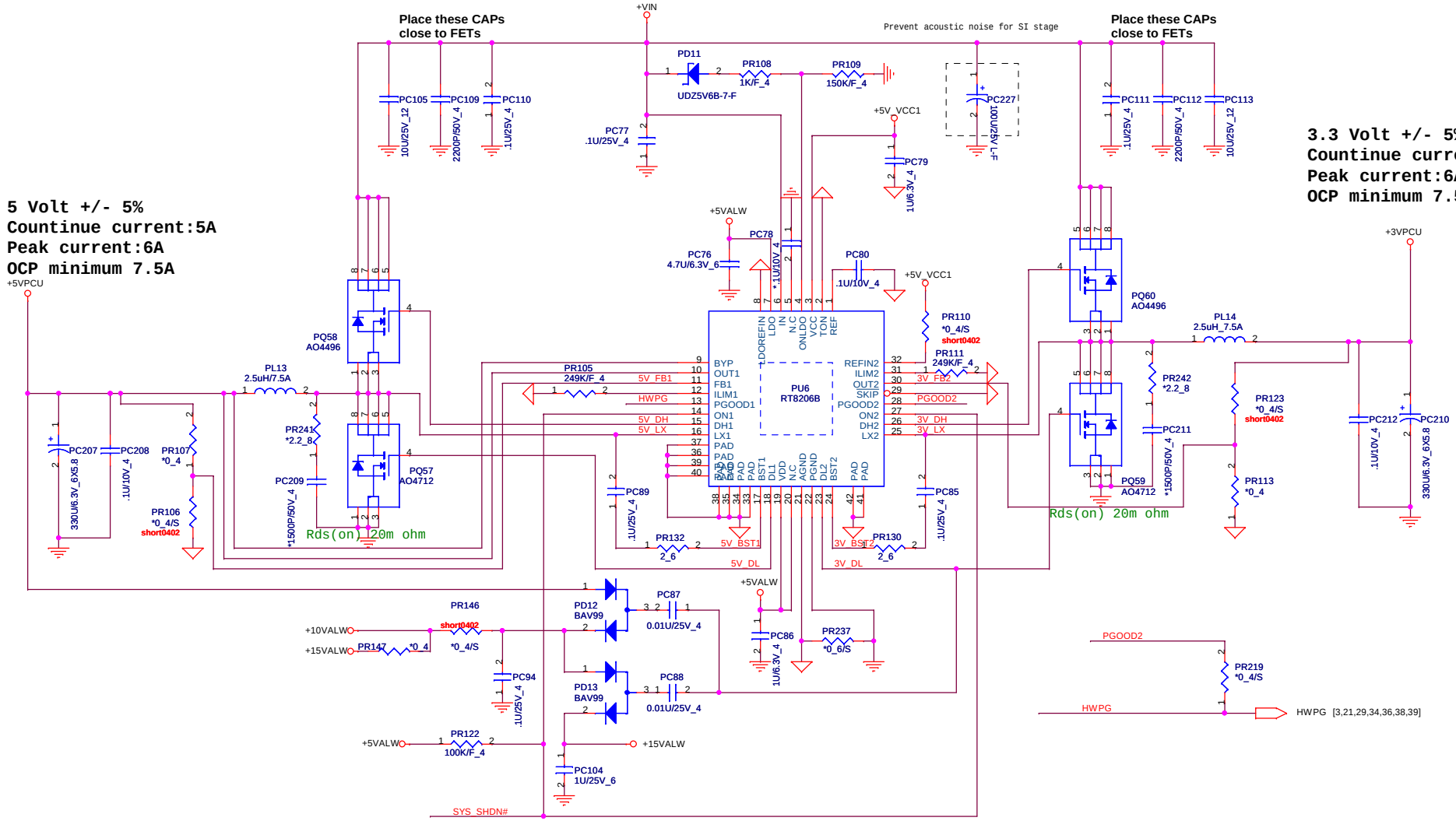
Un-mount for switchable function

NB5	**PROJECT : QL4** Quanta Computer Inc.	
Size A3	Document Number **HDMI Switch / Power CRTL**	Rev E
Date: Friday, October 09, 2009	Sheet 33 of 44	



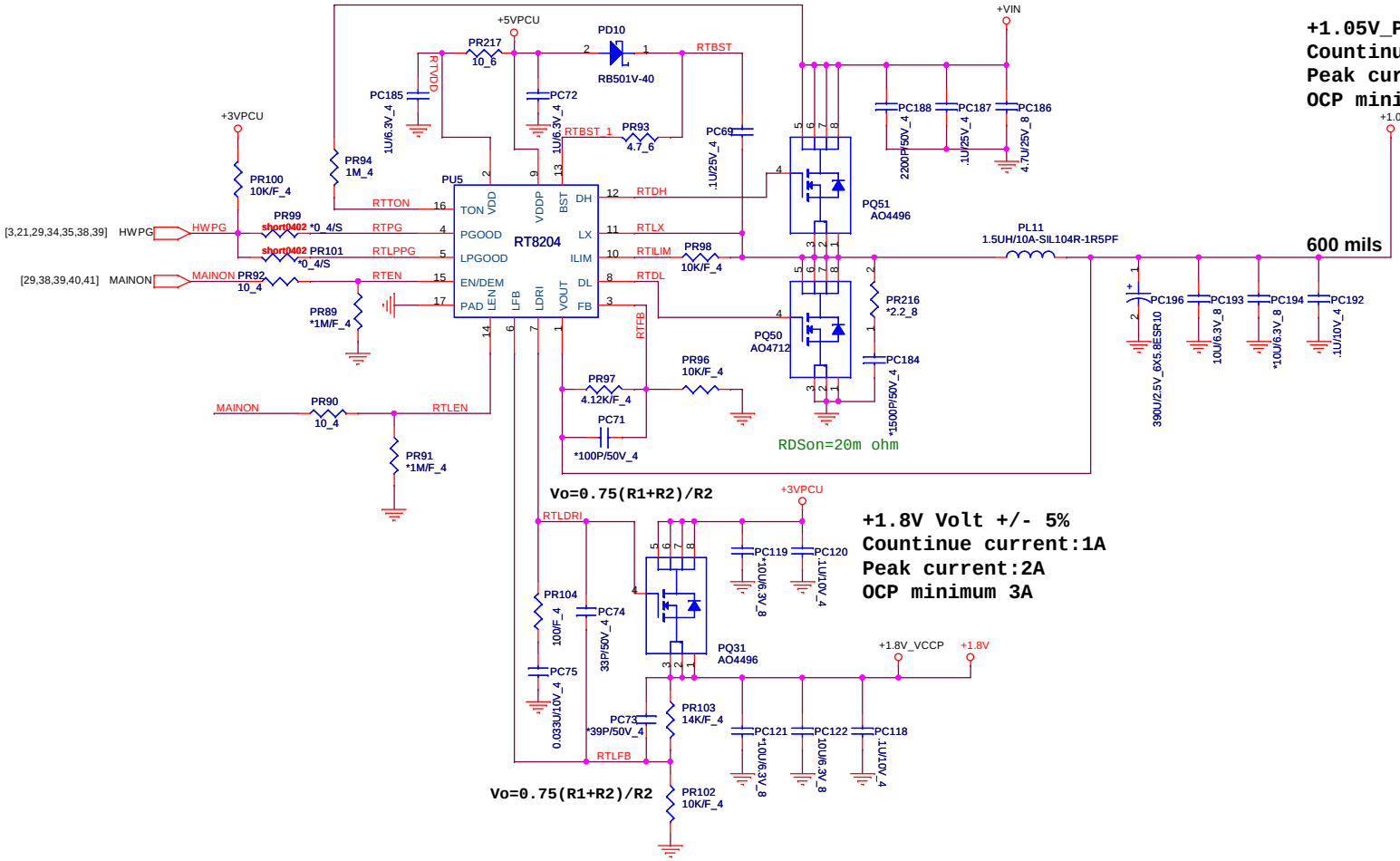
NB5	**PROJECT : QL4** Quanta Computer Inc.		
	Size: Custom	Document Number: **UMA GPU CORE (RT8152A)**	Rev: E
	Date: Friday, October 09, 2009	Sheet 34 of 44	

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

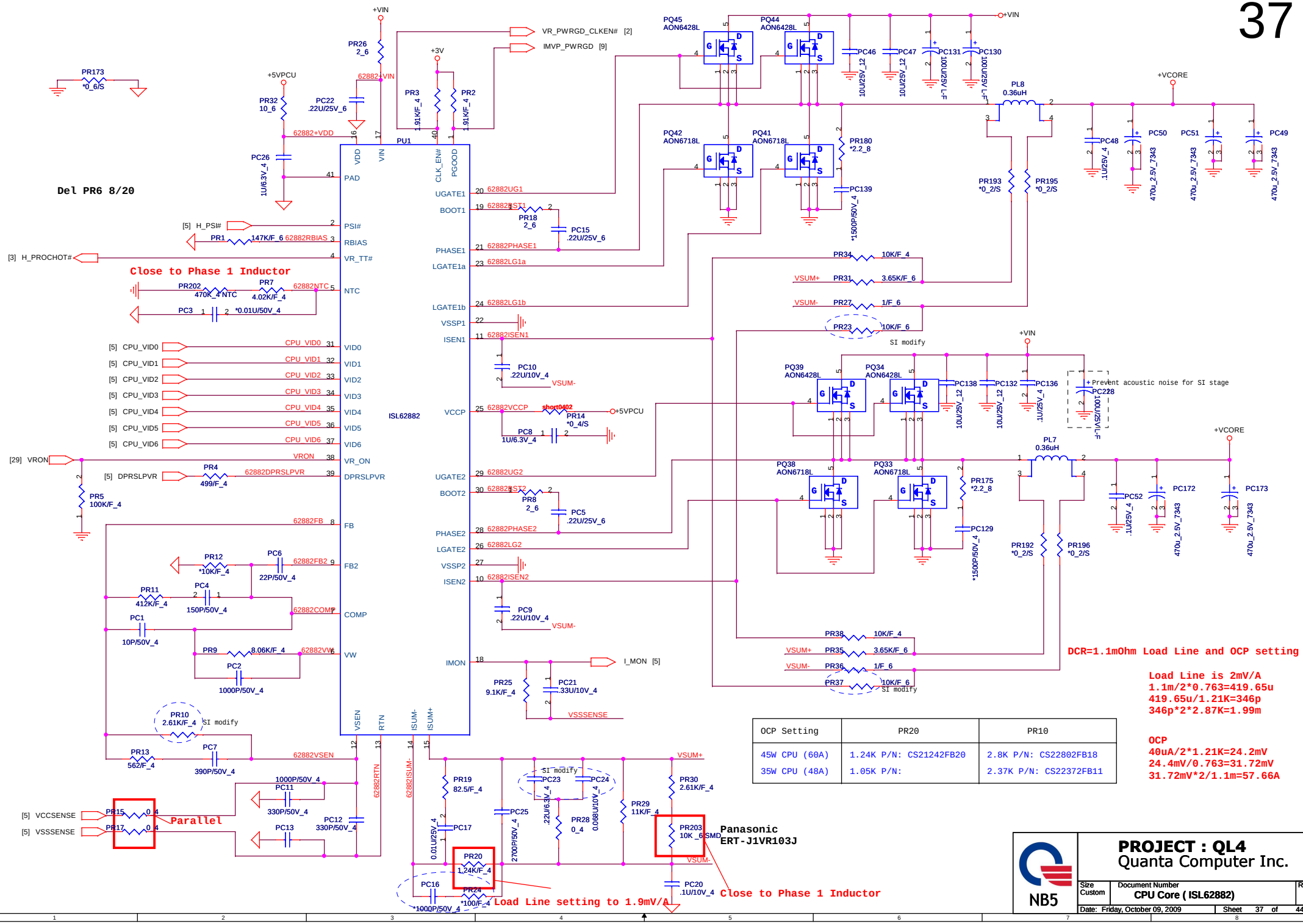


PROJECT : QL4	Quanta Computer Inc.
Size: Custom	Document Number: +5V/+3V (RT8206B)
Rev: E	
Date: Friday, October 09, 2009	Sheet 35 of 44

NB5



NB5	**PROJECT : QL4** Quanta Computer Inc.	
Size: Custom	Document Number: **PCH +1.05V (RT8204)**	Rev: E
Date: Friday, October 09, 2009	Sheet 36 of 44	



OCP Setting	PR20	PR10
45W CPU (60A)	1.24K P/N: CS21242FB20	2.8K P/N: CS22802FB18
35W CPU (48A)	1.05K P/N:	2.37K P/N: CS22372FB11

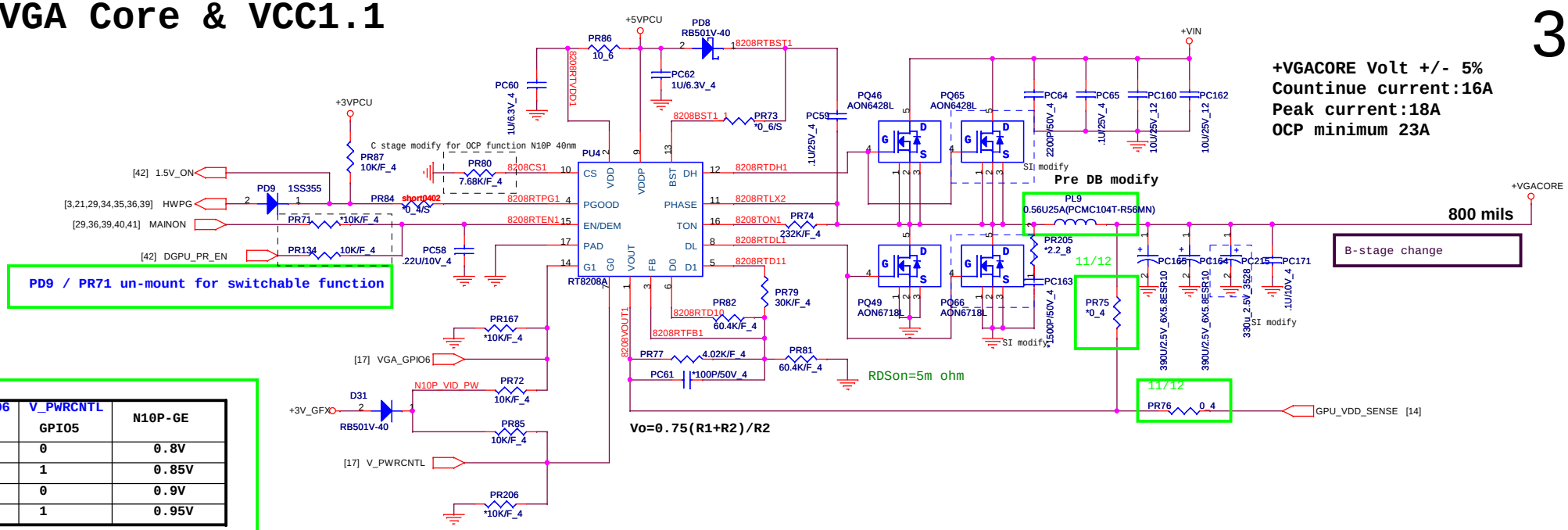
PROJECT : QL4
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	CPU Core (ISL62882)	E
Date: Friday, October 09, 2009	Sheet 37 of 44	

VGA Core & VCC1.1

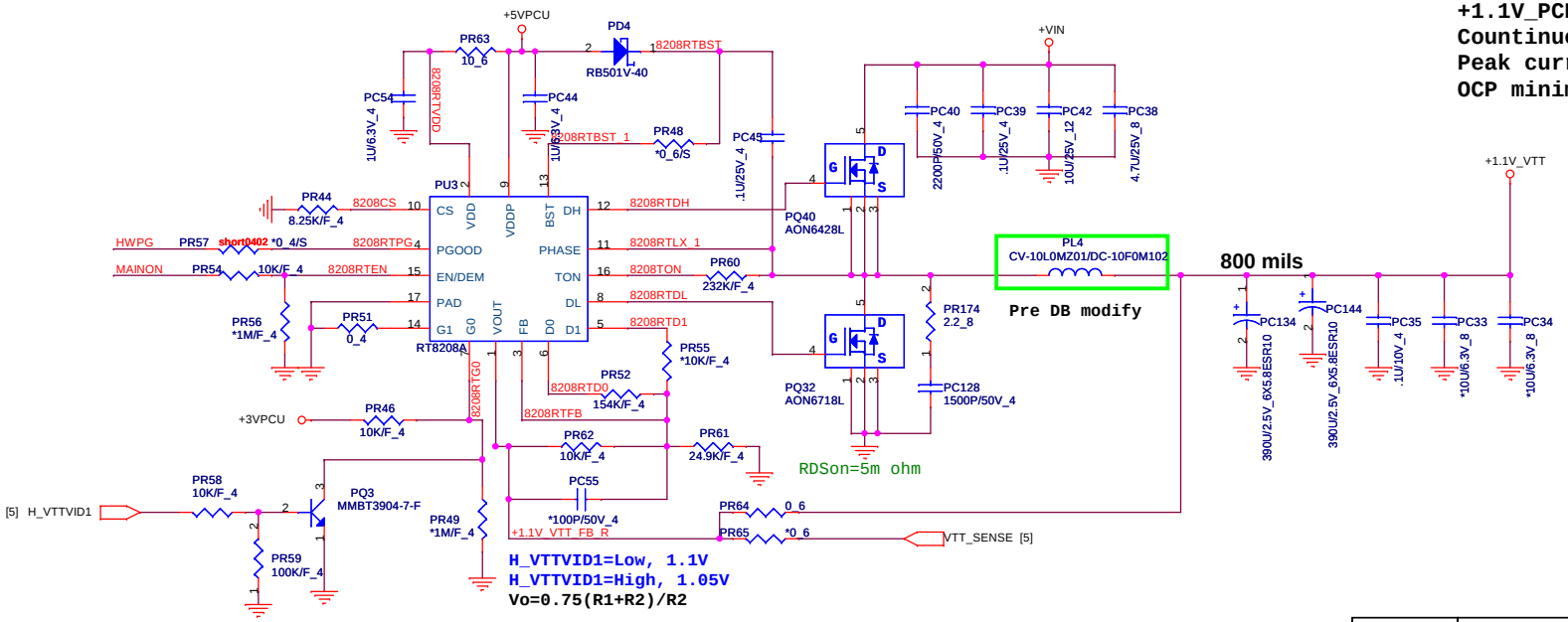
+VGACORE Volt +/- 5%
Countinue current:16A
Peak current:18A
OCP minimum 23A



11/13

VGA_GPIO6	V_PWRCNTL	N10P-GE
GPIO6	GPIO5	
0	0	0.8V
0	1	0.85V
1	0	0.9V
1	1	0.95V

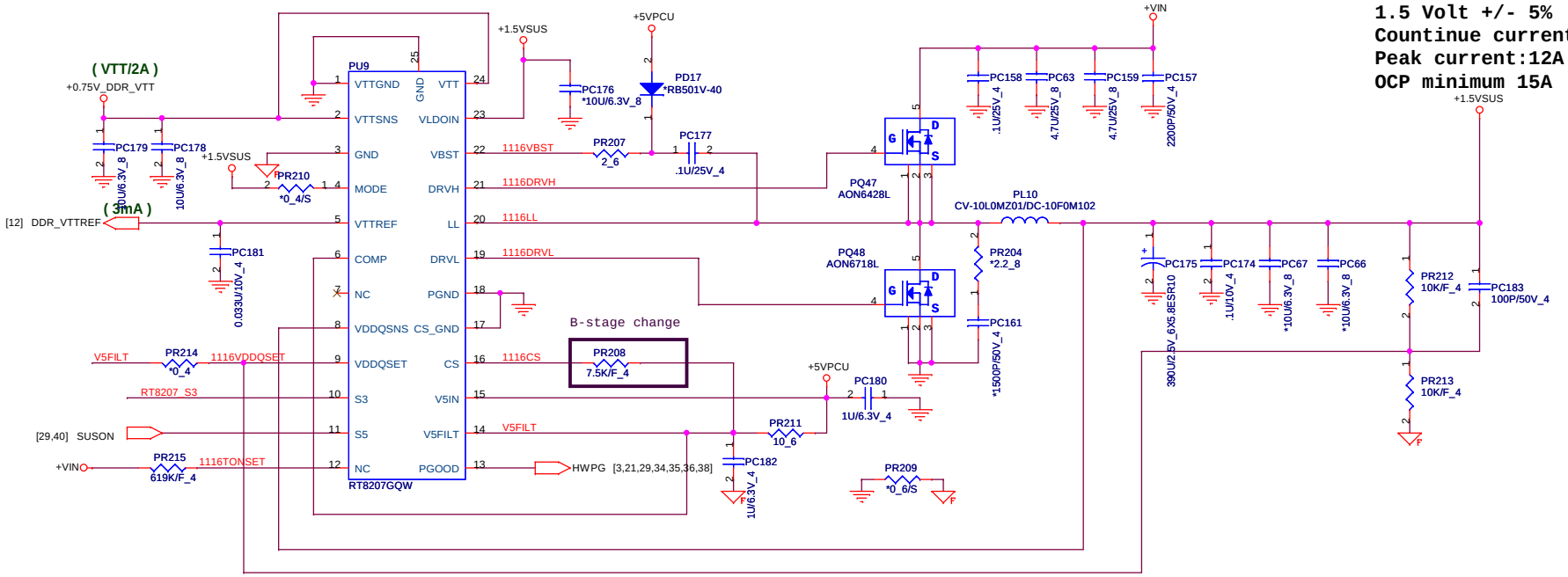
+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A



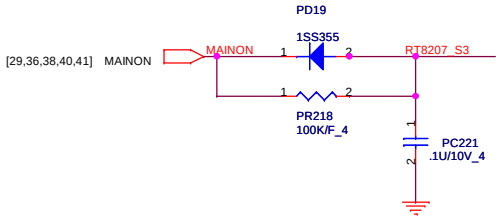
NB5

PROJECT : QL4
Quanta Computer Inc.

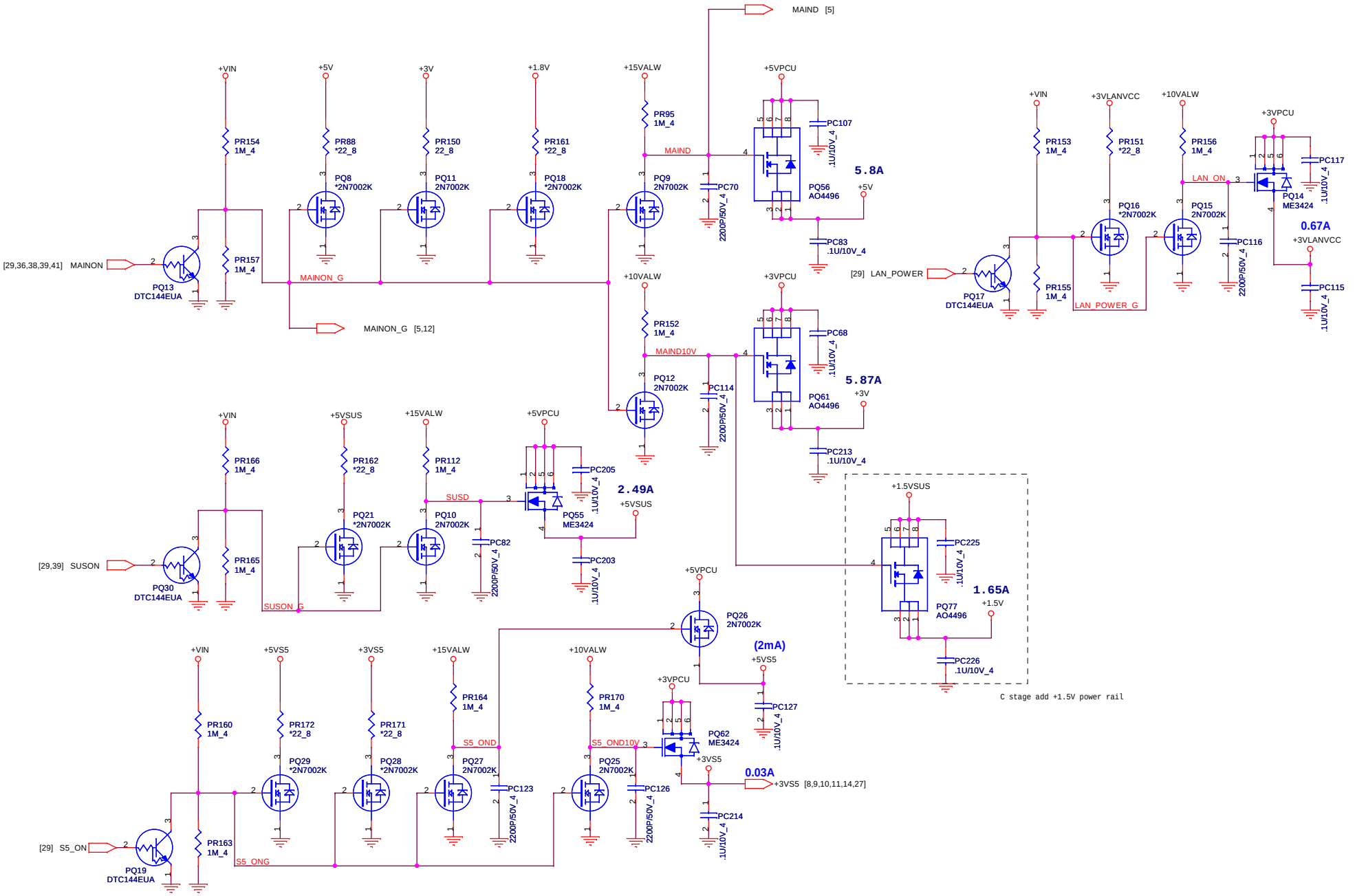
Size	Document Number	Rev
Custom	+1.1V_VTT/VGA Core RT820A	E
Date: Friday, October 09, 2009	Sheet 38 of 44	



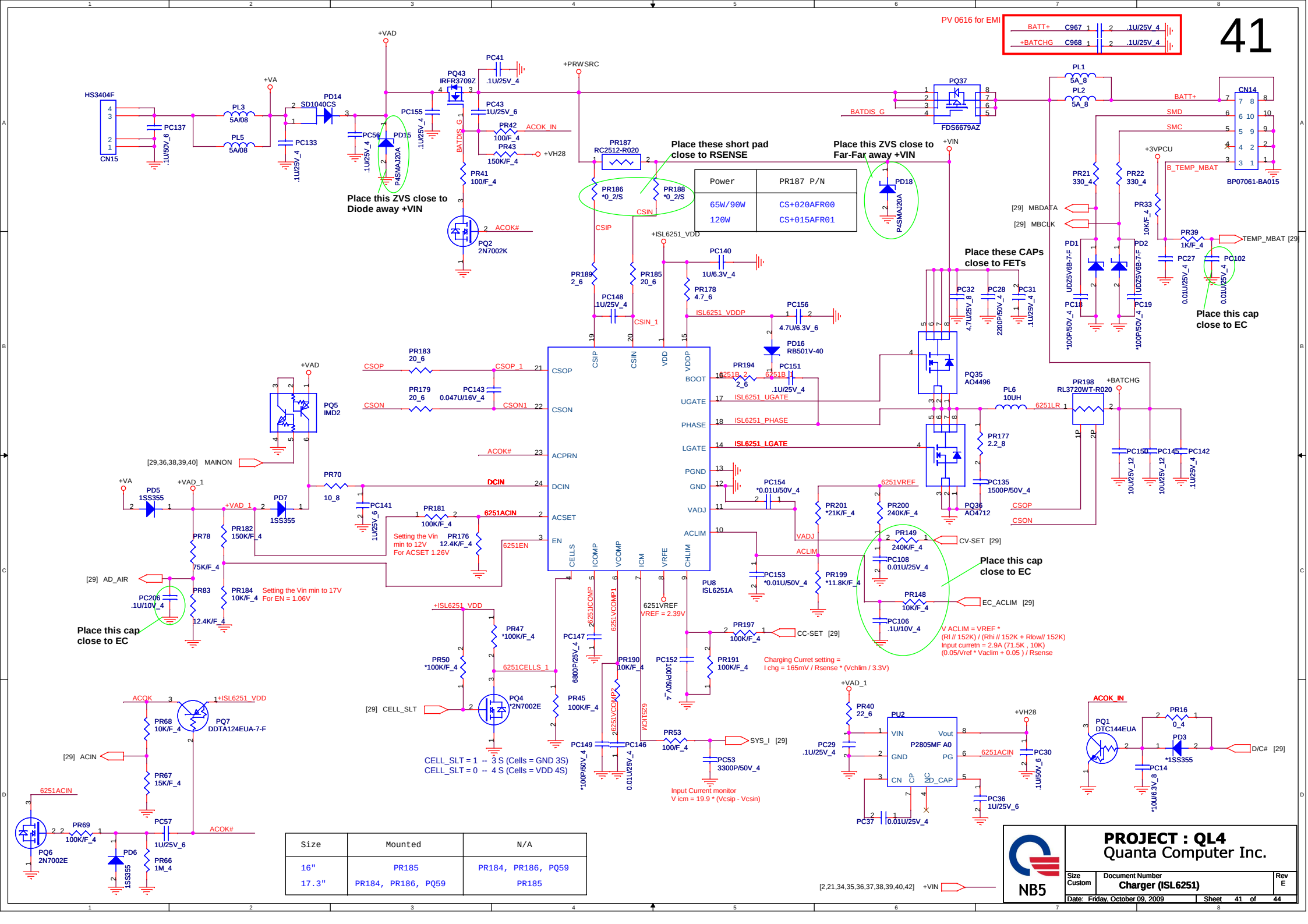
1.5 Volt +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A



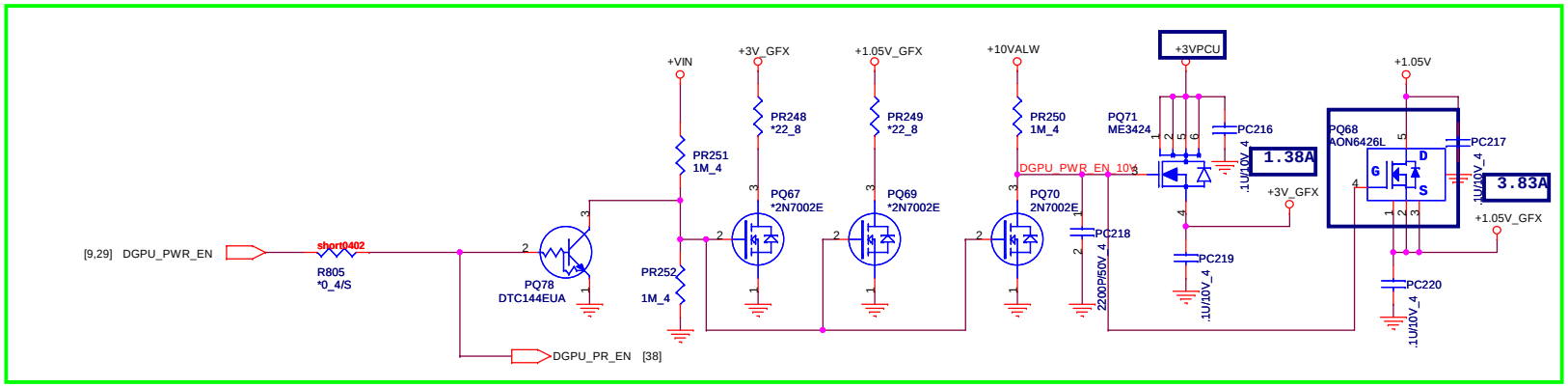
NB5	**PROJECT : QL4** Quanta Computer Inc.	
Size: Custom	Document Number: **DDR3 (RT8207)**	Rev: E
Date: Friday, October 09, 2009	Sheet 39 of 44	



NB5	**PROJECT : QL4** Quanta Computer Inc.	
	Size: Custom Document Number: DISCHARGE/3VS5/5VS5/LAN	Rev: E
	Date: Friday, October 09, 2009	Sheet 40 of 44

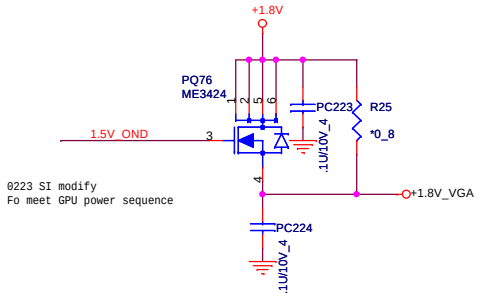


Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

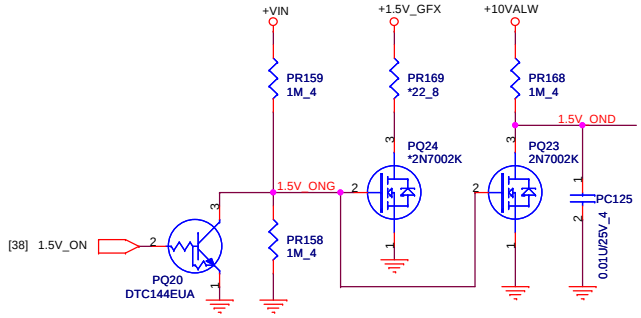


For Discrete or switchable Only

+1.8 Volt +/- 0.1V
Countinue current:0.3A
Peak current:1A

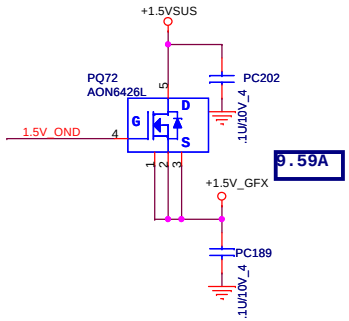


For Discrete or switchable Only



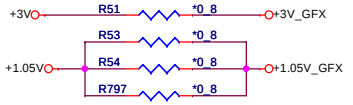
Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete or switchable Only



R51 co-lay PQ71
R53/R54 co-lay PQ68

For Discrete Only



SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

For Hybrid DGPU Power Rails Sequence
1. **+3V_GFX, +1.05V_GFX**
2. **+VGA_CORE -> DGPU_PG**
3. **1.5V_GFX, +1.8V_GFX**

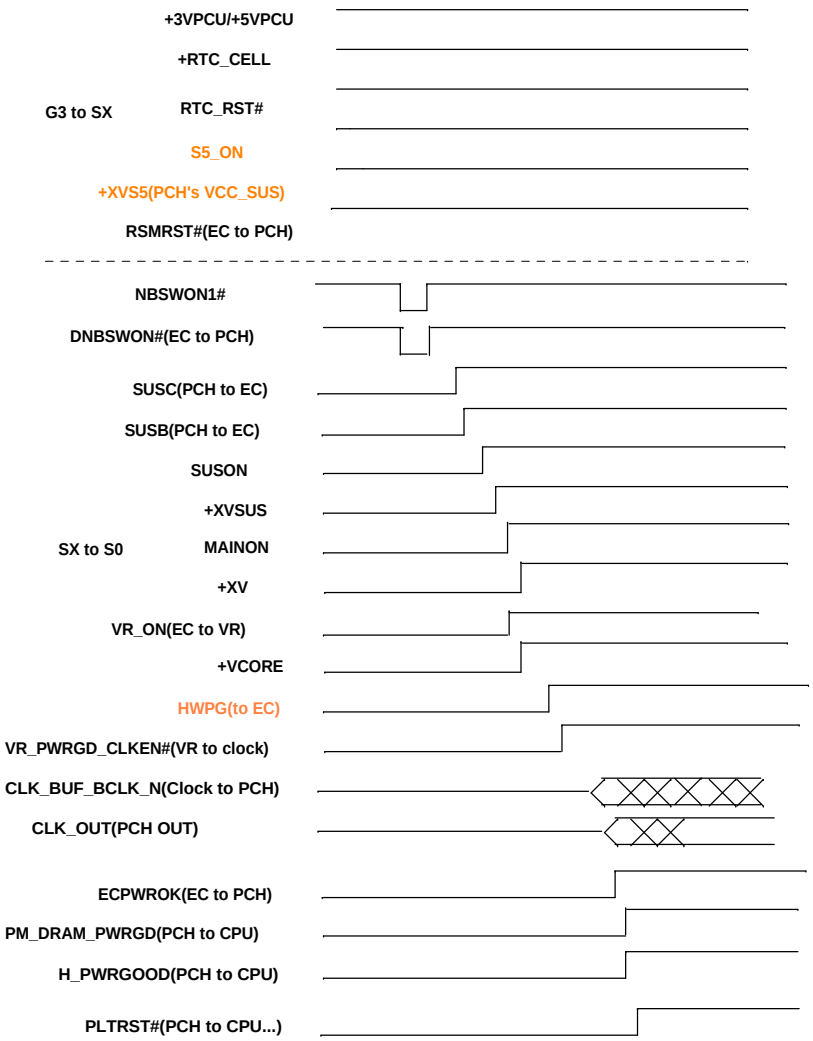
PROJECT : QL4
Quanta Computer Inc.

NB5

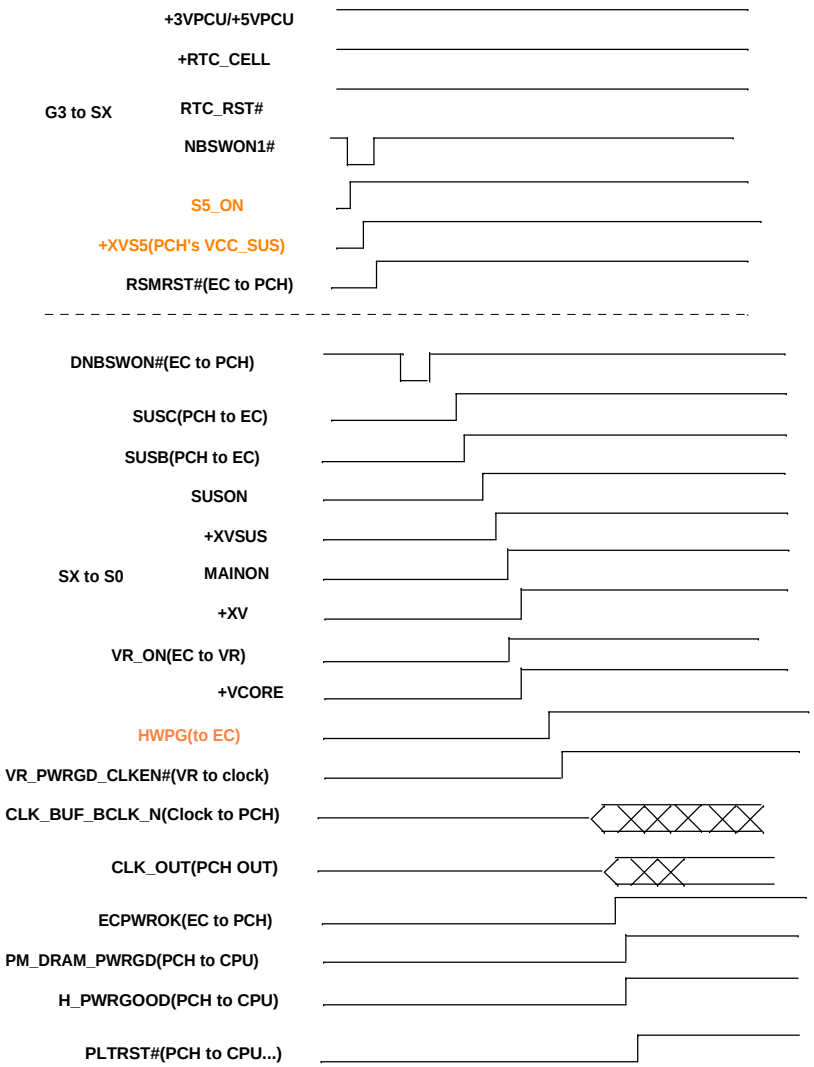
Size	Document Number	Rev
A3	Switchable Power	E
Date: Friday, October 09, 2009	Sheet 42 of 44	

Power up sequence

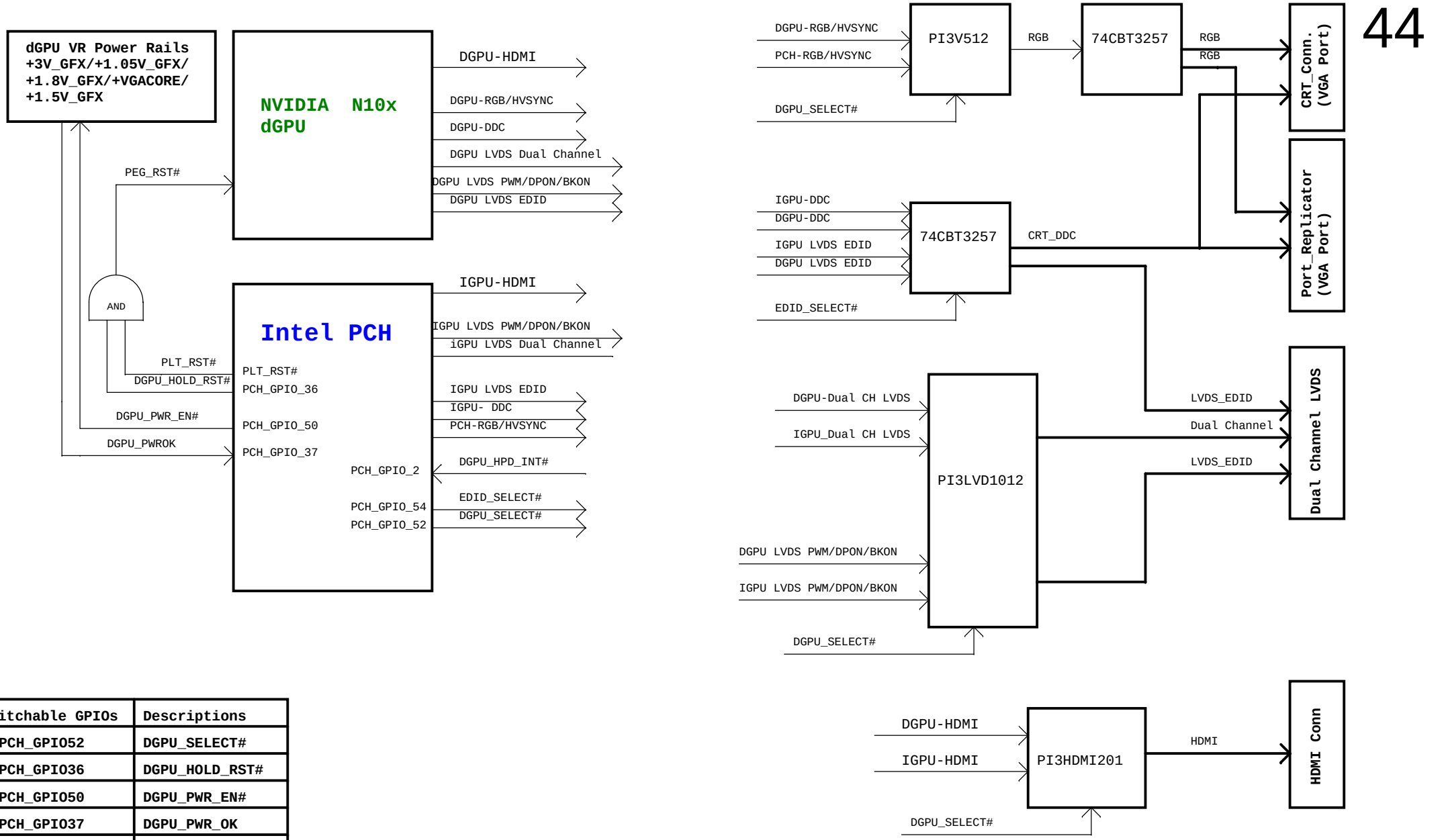
LAN/RTC WAKE UP ENABLE.



LAN/RTC WAKE UP DISABLE.



NB5	**PROJECT : QL4** Quanta Computer Inc.	
Size: Custom	Document Number: **Power up sequence**	Rev: E
Date: Friday, October 09, 2009	Sheet 43 of 44	



Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO36	DGPU_HOLD_RST#
PCH_GPIO50	DGPU_PWR_EN#
PCH_GPIO37	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#

NB5

PROJECT : QL4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Switch Blockdiagram	E
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