18734 Woody_WL

18753 Slinky_WL

Schematics Document

DY : None Installed
UMA: UMA only installed
DIS: DISCRTE OPTIMUS installed

<Core Design>

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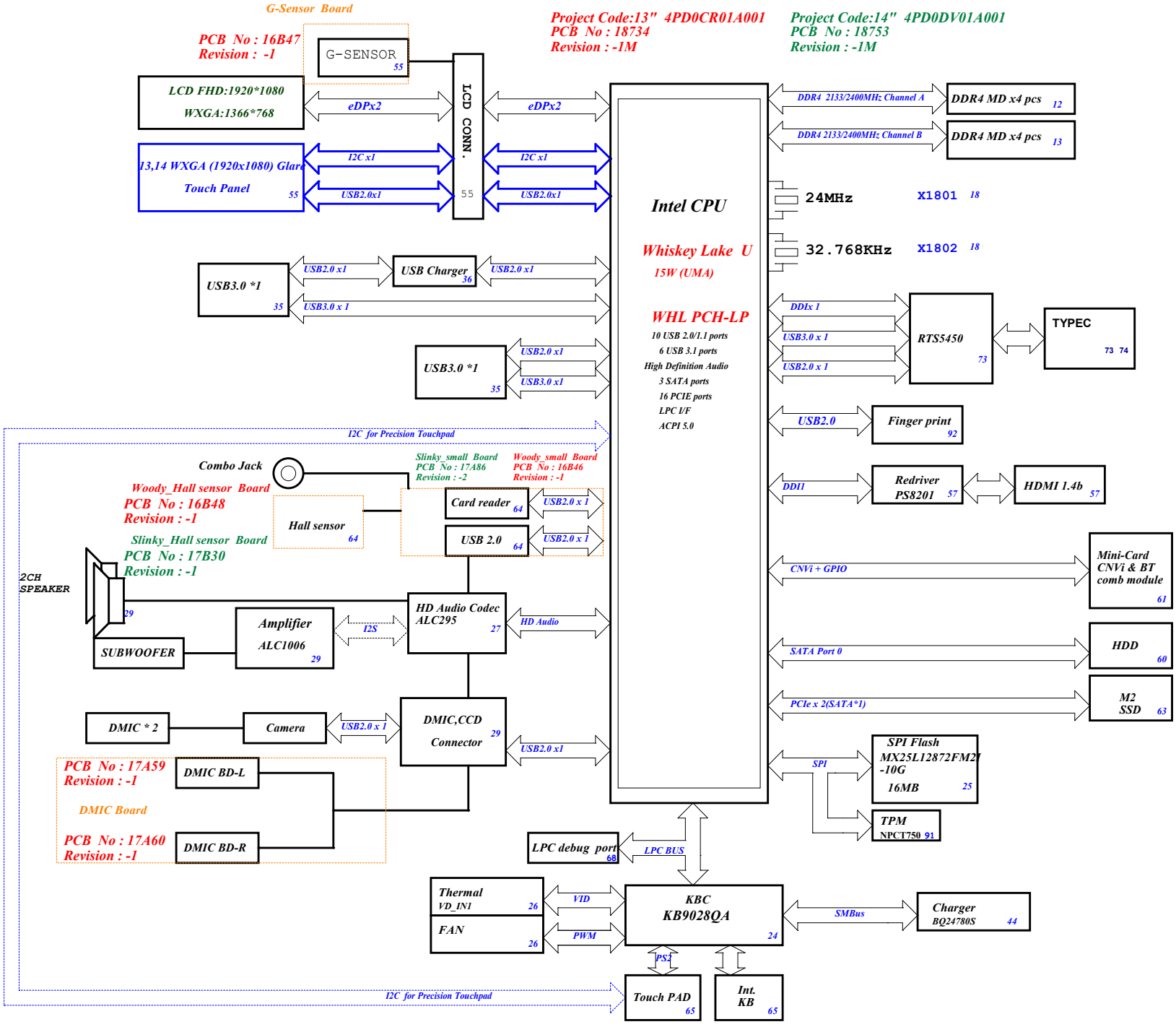
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A3	Document Number: Woody_WL/Slinky_WL	Rev: -1m
Date: Friday, September 07, 2018	Sheet 1 of 106	



CHARGER BQ24780SRUYR-GP 44	
INPUTS	OUTPUTS
19V_AD+ BT+	19V_DCBATOUT

SYSTEM DC/DC SY8288CRAC-GP 45	
INPUTS	OUTPUTS
19V_DCBATOUT	5V_AUX_S5 5V_S5

SYSTEM DC/DC SY8288BRAC-GP 45	
INPUTS	OUTPUTS
19V_DCBATOUT	3D3V_AUX_S5 3D3V_S5

CPU DC/DC RT3602AJGQW-GP 46	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_VCCST

CPU DC/DC AOZ5038QI-GP 47	
INPUTS	OUTPUTS
19V_DCBATOUT	1V_CPU_CORE

CPU DC/DC AOZ5049QI-1-GP 48	
INPUTS	OUTPUTS
5V_S5	1V_VCCGT

CPU DC/DC RT9610BZQW-GP 50	
INPUTS	OUTPUTS
5V_S5	1V_VCCSA

CPU DC/DC G5416QS1U-GP 51	
INPUTS	OUTPUTS
19V_DCBATOUT	PWR_VDDQ

SYSTEM DC/DC AOZ2262QI-10-GP-U 52	
INPUTS	OUTPUTS
19V_DCBATOUT	PWR_1D0V

SYSTEM DC/DC G9661-25ADJRE1U-GP 53	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

SYSTEM Load switch TPS22976 40	
INPUTS	OUTPUTS
3D3V_S5	3D3V_S0
5V_S5	5V_S0
1D0V_S5	1V_VCCST
1D8V_S5	1D8V_S0

SYSTEM Load switch APE8939 40	
INPUTS	OUTPUTS
1D0V_S5	1V_VCCIO

<Core Design>

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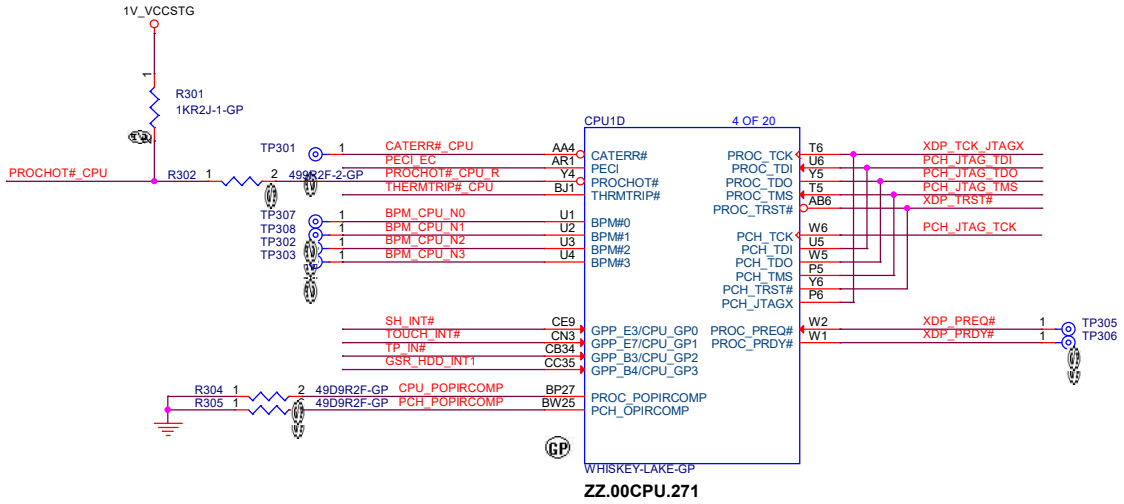
Title: Block Diagram

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

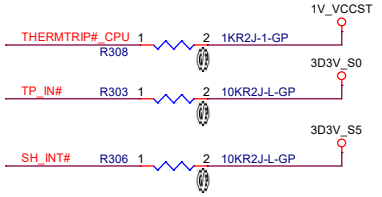
Date: Friday, September 07, 2018 | Sheet 2 of 106

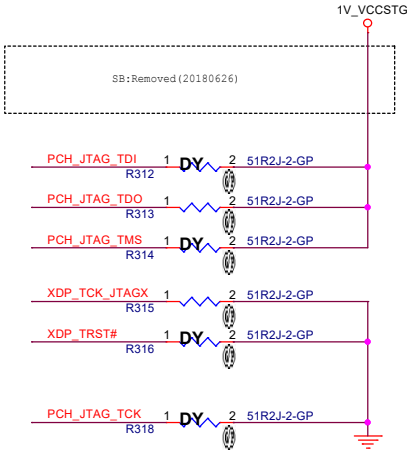
SSID = CPU

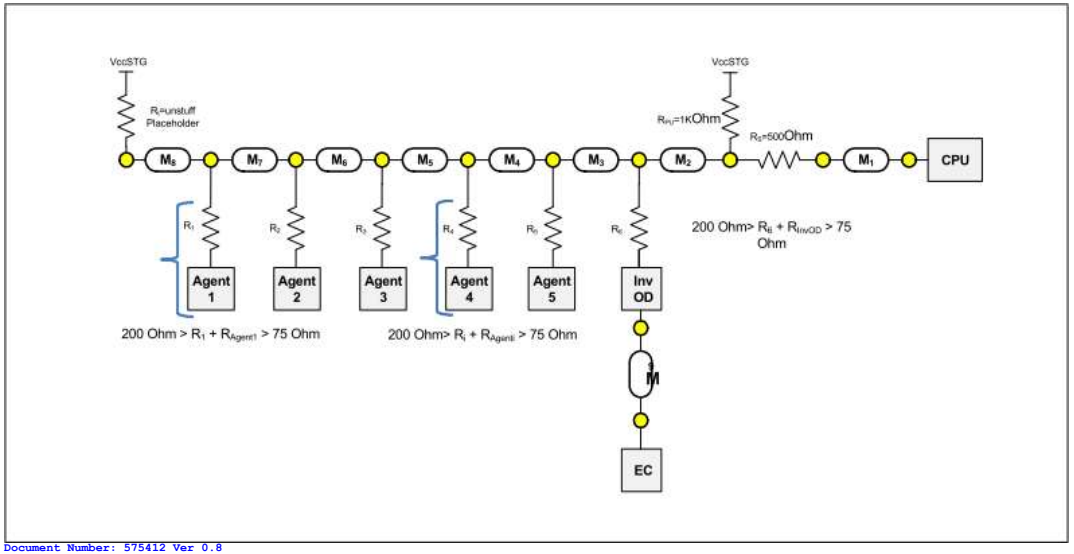
24 PECI_EC
24,44,46 PROCHOT#_CPU
65 TP_IN#
24 SH_INT#
55 TOUCH_INT#
69 GSR_HDD_INT1



ZZ.00CPU.271







Document Number: 575412 Ver 0.8

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (THML/JTAG)**

Size: A3 | Document Number: **Woody_WL/Slinky_WL** | Rev: **-1m**

Date: Friday, September 07, 2018 | Sheet 3 of 106

Main Func = CPU

HDMI

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3
57 HDMI_SCL_CPU
57 HDMI_SDA_CPU
57 HDMI_DET_CPU

Type-C

72 DP2_DDI_TX_N0
72 DP2_DDI_TX_P0
72 DP2_DDI_TX_N1
72 DP2_DDI_TX_P1
72 DP2_DDI_TX_N2
72 DP2_DDI_TX_P2
72 DP2_DDI_TX_N3
72 DP2_DDI_TX_P3
72 DP2_AUX_CPU_P
72 DP2_AUX_CPU_N

eDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 eDP_HPD_CPU
72 DP_HPD_CON
24 eDP_BLEN_CPU
55 eDP_BLCTRL_CPU
55 eDP_VDDEN_CPU

Other

15 GPP_H17_STRAP
24 EC_SMI#
24 EC_SCI#

3D3V_S0 — SRN2K2J-1-GP — RN401 (GP)
HDMI_SDA_CPU
HDMI_SCL_CPU

3D3V_S0 — RN403 (CB) — SRN2K2J-1-GP
CPU_DP2_CTRL_CLK
CPU_DP2_CTRL_DATA

(#575412) 1.3.2Digital Display Interface Signal Mapping

Table 1-4. Digital Display Interface Signal Mapping

Port	DDI PROCESSOR Pin Names	Display Port Mapping	HDMI* Mapping
Port 1	DDI1_TXN[0]	DDI1_LANE0_DN	HDMIxC_TX2_DN
	DDI1_TXP[0]	DDI1_LANE0_DP	HDMIxC_TX2_DP
	DDI1_TXN[1]	DDI1_LANE1_DN	HDMIxC_TX1_DN
	DDI1_TXP[1]	DDI1_LANE1_DP	HDMIxC_TX1_DP
	DDI1_TXN[2]	DDI1_LANE2_DN	HDMIxC_TX0_DN
	DDI1_TXP[2]	DDI1_LANE2_DP	HDMIxC_TX0_DP
	DDI1_TXN[3]	DDI1_LANE3_DN	HDMIxC_CLK_DN
	DDI1_TXP[3]	DDI1_LANE3_DP	HDMIxC_CLK_DP
	DDPB_HPD	DDI1_HPD_Q	DDI1_HPD_Q
	DDPB_CTRLCLK	NA	DDI1_CTRL_CK
	DDPB_CTRLDATA	NA	DDI1_CTRL_DATA

HDMI 1.4b

TYPEC

CPU1A — 1 OF 20 — WHISKEY-LAKE-GP

HDMI_DDI_TX_N2	AL5	DDI1_TXN0	AG4	eDP_TX_CPU_N0
HDMI_DDI_TX_P2	AL6	DDI1_TXP0	AG3	eDP_TX_CPU_P0
HDMI_DDI_TX_N1	AJ5	DDI1_TXN1	AG2	eDP_TX_CPU_N1
HDMI_DDI_TX_P1	AJ6	DDI1_TXP1	AG1	eDP_TX_CPU_P1
HDMI_DDI_TX_N0	AF6	DDI1_TXN2	AJ4	
HDMI_DDI_TX_P0	AF5	DDI1_TXP2	AJ3	
HDMI_DDI_TX_N3	AE5	DDI1_TXN3	AJ2	
HDMI_DDI_TX_P3	AE6	DDI1_TXP3	AJ1	
DP2_DDI_TX_N0	AC4	DDI2_TXN0		
DP2_DDI_TX_P0	AC3	DDI2_TXP0	EDP_AUX_N	AH4 eDP_AUX_CPU_N
DP2_DDI_TX_N1	AC1	DDI2_TXN1	EDP_AUX_P	AH3 eDP_AUX_CPU_P
DP2_DDI_TX_P1	AC2	DDI2_TXP1	DISP_UTILS	AM7
DP2_DDI_TX_N2	AE4	DDI2_TXN2	DDI1_AUX_N	AC7
DP2_DDI_TX_P2	AE3	DDI2_TXP2	DDI1_AUX_P	AC6
DP2_DDI_TX_N3	AE1	DDI2_TXN3	DDI2_AUX_N	AD4 DP2_AUX_CPU_N
DP2_DDI_TX_P3	AE2	DDI2_TXP3	DDI2_AUX_P	AD3 DP2_AUX_CPU_P
			DDI3_AUX_N	AG7
			DDI3_AUX_P	AG6

GPP_E13/DDPB_HPD0/DISP_MISC0 CN6 HDMI_DET_CPU
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6 DP_HPD_CON
GPP_E15/DPPD_HPD2/DISP_MISC2 CP7 EC_SMI#
GPP_E16/DPPE_HPD3/DISP_MISC3 CP6 EC_SCI#
GPP_E17/EDP_HPD/DISP_MISC4 CM7 eDP_HPD_CPU

EDP_BKLTEN CK11 eDP_BLEN_CPU
EDP_VDDEN CG11 eDP_VDDEN_CPU
EDP_BKLTCTL CH11 eDP_BLCTRL_CPU

eDP

ZZ.00CPU.271

1V_VCCIO
CHECK WHL design guide: DISP_RCOMP
R401 — 24D9R2F-L-GP
eDP_RCOMP_CPU AM6 DISP_RCOMP

HDMI_SCL_CPU CC8 GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
HDMI_SDA_CPU CC9 GPP_E19/DPPB_CTRLDATA
CPU_DP2_CTRL_CLK CH4 GPP_E20/DPPC_CTRLCLK
CPU_DP2_CTRL_DATA CH3 GPP_E21/DPPC_CTRLDATA
CP4 GPP_E22/DPPD_CTRLCLK
CN4 GPP_E23/DPPD_CTRLDATA
GPP_H17_STRAP CR26 GPP_H16/DDPF_CTRLCLK
CP26 GPP_H17/DDPF_CTRLDATA

(#575412 PDG 0.9) eDP_RCOMP Guideline for WHL & CFL.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	Max = 600 mils

(#575412 PDG 0.9) eDP_RCOMP Guideline for CNL.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	5 mils	25 mils	100 Ω ±1%	Max = 600 mils

(#575412 PDG 0.9)DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

SB:20180626
3D3V_S0
EC_SMI# — R402 10KR2J-3-GP — DY
3D3V_S0
EC_SCI# — R407 2K2R2J-L1-GP

eDP_BLEN_CPU — R408 100KR2J-3-GP
DP_HPD_CON — R409 100KR2J-3-GP

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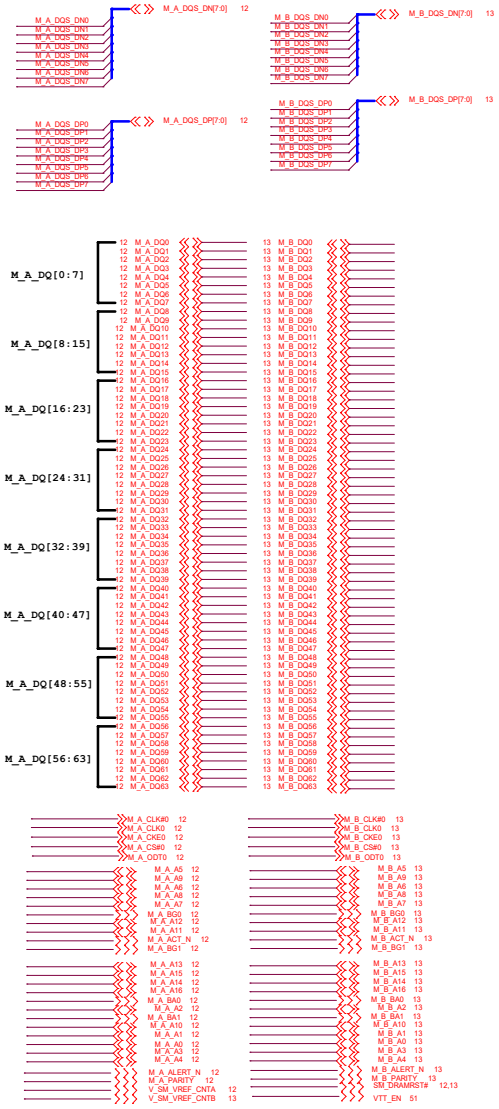
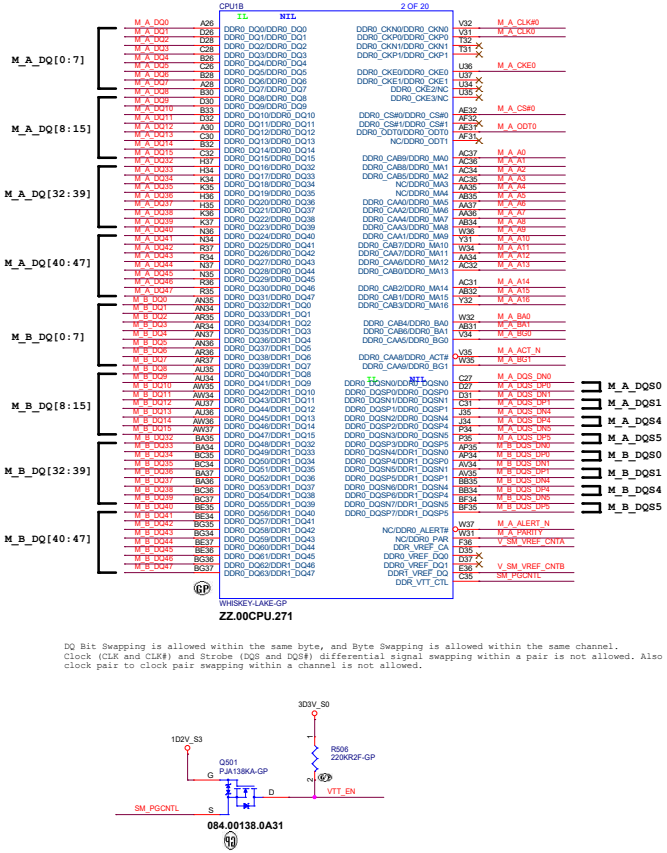
Taipei Hsien 221, Taiwan, R.O.C.

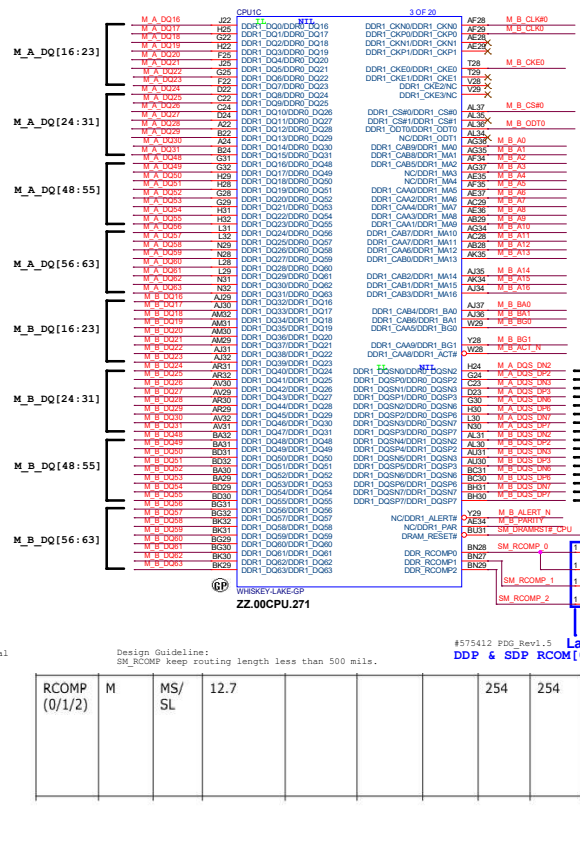
Title: CPU (DDI/EDP)
Size: A3 | Document Number: Woody_WL/Slinky_WL | Rev: -1m
Date: Friday, September 07, 2018 | Sheet 4 of 106

Main Func = CPU

DDR4 ball type: Non-Interleaved Type

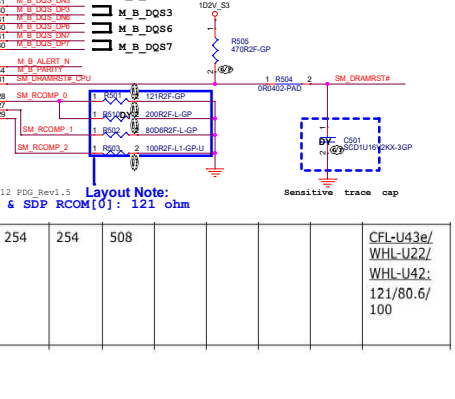






DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.



#575412 PDG_Rev1.5

Layout Note:
DDP & SDP RCOM[0]: 121 ohm

RCOMP (0/1/2)	M	MS/ SL	12.7			254	254	508				CFL-U43e/ WHL-U22/ WHL-U42: 121/80.6/ 100

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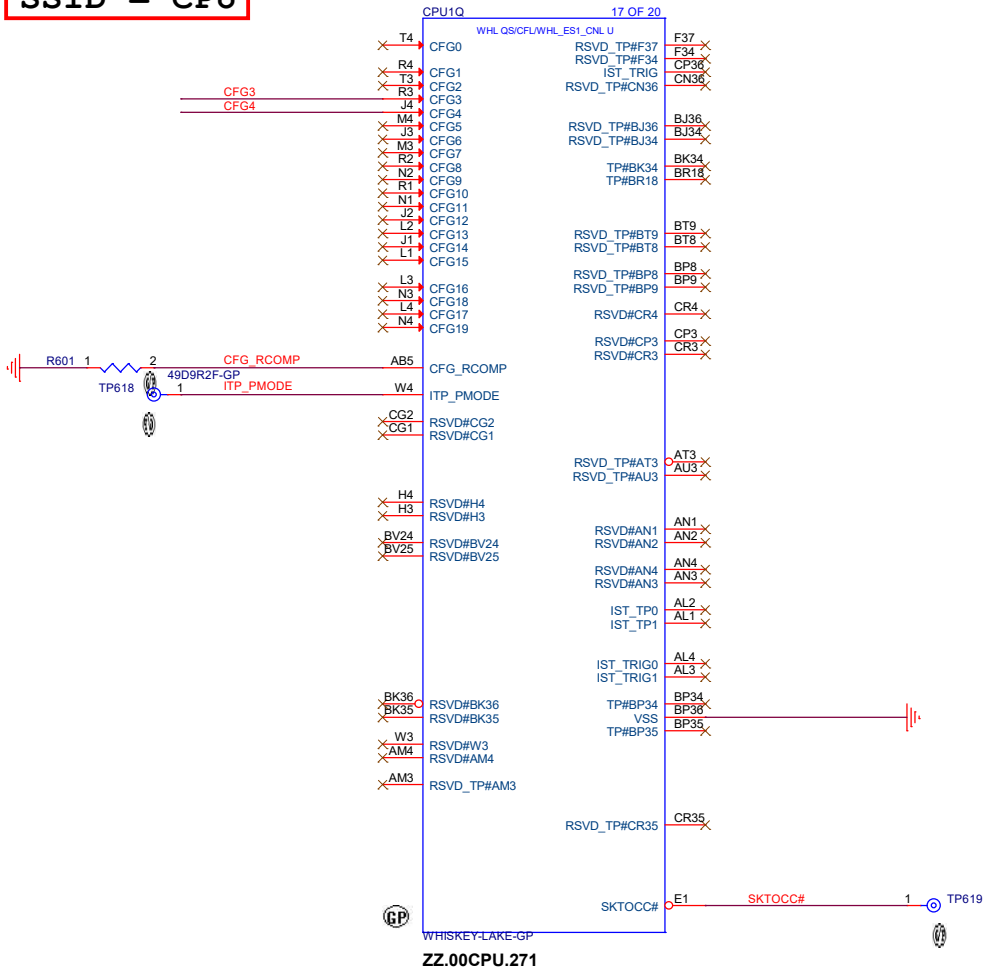
Title: CPU (DDR)

Size	Document Number	Rev
Custom	Woody_WL/Slinky_WL	-1m
Date: Friday, September 07, 2018	Sheet 5 of 106	

15 CFG3
15 CFG4

SSID = CPU



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Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I	GTL	SE	U - Processor Lines. CFG[2], CFG[6:5] and CFG[7] are not relevant for U - Processor Lines.

Document Number: 575418 Ver 1.0

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Title: CPU (CFG/IST)

Size: A3 | Document Number: Woody_WL/Slinky_WL | Rev: -1m

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SSID = CPU

46 VCORE_VSEN
46 VCORE_RTN

46 PWR_VCORE_ALERT#
46 VIDSCK_CPU_R
46 VIDSOUT_CPU_R

1V_CPU_CORE

CPU1L 12 OF 20

AN9	VCCCORE	VCCCORE	AW24
AN10	VCCCORE	VCCCORE	AW25
AN24	VCCCORE	VCCCORE	AW26
AN26	VCCCORE	VCCCORE	AW27
AN27	VCCCORE	VCCCORE	AY24
AP2	VCCCORE	VCCCORE	AY26
AP9	VCCCORE	VCCCORE	BA5
AP24	VCCCORE	VCCCORE	BA7
AP26	VCCCORE	VCCCORE	BA8
AR5	VCCCORE	VCCCORE	BA25
AR6	VCCCORE	VCCCORE	BA27
AR7	VCCCORE	VCCCORE	BB2
AR8	VCCCORE	VCCCORE	BB26
AR10	VCCCORE	VCCCORE	BC5
AR25	VCCCORE	VCCCORE	BC6
AR27	VCCCORE	VCCCORE	BC7
AT9	VCCCORE	VCCCORE	BC9
AT24	VCCCORE	VCCCORE	BC10
AT26	VCCCORE	VCCCORE	BC26
AU5	VCCCORE	VCCCORE	BC27
AU6	VCCCORE	VCCCORE	BD5
AU7	VCCCORE	VCCCORE	BD8
AU8	VCCCORE	VCCCORE	BD10
AU9	VCCCORE	VCCCORE	BD25
AU24	VCCCORE	VCCCORE	BD27
AU25	VCCCORE	VCCCORE	BE9
AU26	VCCCORE	VCCCORE	BE24
AU27	VCCCORE	VCCCORE	BE25
AV2	VCCCORE	VCCCORE	BE26
AV5	VCCCORE	VCCCORE	BE27
AV7	VCCCORE	VCCCORE	BF2
AV10	VCCCORE	VCCCORE	BF9
AV27	VCCCORE	VCCCORE	BF24
AW5	VCCCORE	VCCCORE	BF26
AW6	VCCCORE	VCCCORE	BG27
AW7	VCCCORE	VCCCORE	
AW8	VCCCORE	VCC_SENSE	AN6
AW9	VCCCORE	VSS_SENSE	AN5
AW10	VCCCORE	VIDALERT#	AA3
		VIDSCK	AA1
		VIDSOUT	AA2
		RSVD#Y3	Y3
		VCCSTG	BG3

VCORE_VSEN
VCORE_RTN
SVID_ALERT#_CPU_R
SVID_CLK_CPU_R
SVID_DATA_CPU_R

1V_CPU_CORE
1V_VCCSTG

Document Number: 575418 Ver 1.0
Vcc 70A(Max)

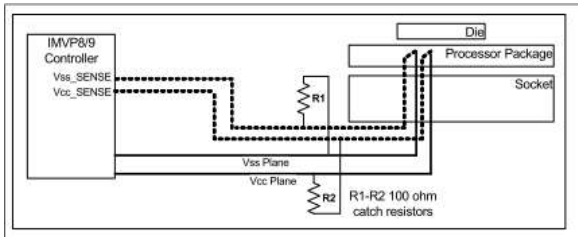
BB9 RSVD#BB9
BC24 RSVD#BC24
AY9 RSVD#AY9
BB24 RSVD#BB24

WHISKEY-LAKE-GP

ZZ.00CPU.271

1V_CPU_CORE

R1 R719 100R2F-L1-GP-U
VCORE_VSEN
VCORE_RTN
R2 R720 100R2F-L1-GP-U



Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
	100Ω	50Ω	<25 mils
Vcc_SENSE /Vss_SENSE			
Vcc_{GT}_SENSE / Vss_{GT}_SENSE			
Vcc_{SA}_SENSE / Vss_{SA}_SENSE			
Vcc_{IO}_SENSE / Vss_{IO}_SENSE[1]		NA	

R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

Document Number: 575412 Ver 0.8

SVID ALERT

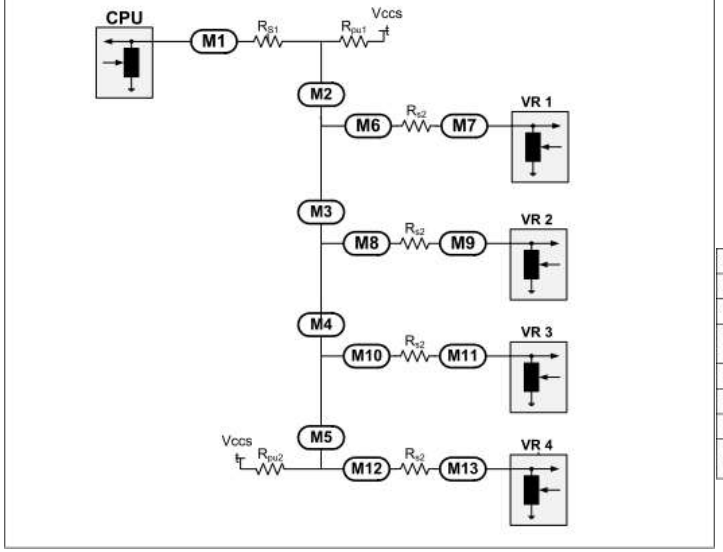
1V_VCCST
R727 56R2J-4-GP
SVID_ALERT#_CPU_R — R728 220R2J-L2-GP — PWR_VCORE_ALERT#

SVID CLOCK

1V_VCCST
DY R723 54D9R2F-L1-GP
SVID_CLK_CPU_R — R732 0R0402-PAD-1-GP — VIDSCK_CPU_R

SVID DATA

1V_VCCST
R726 100R2F-L1-GP-U
SVID_DATA_CPU_R — R709 0R0402-PAD-1-GP — VIDSOUT_CPU_R



SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock
Length Matching Rules	
Length Matching between VIDSOUT and VIDSCK	± 100mils

<Core Design>

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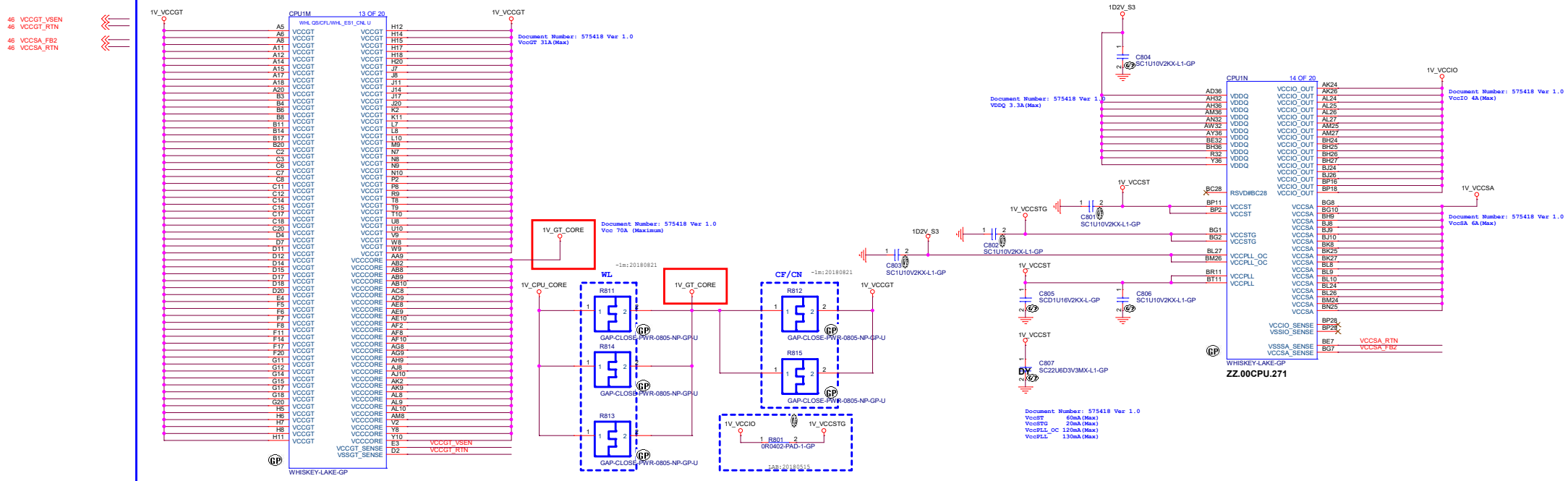
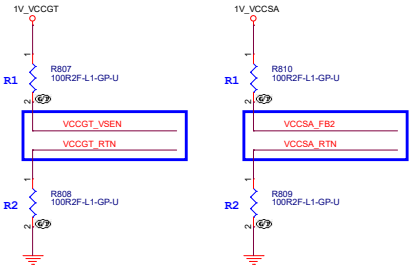
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCORE/VID)
Size: A3 | Document Number: Woody_WL/Slinky_WL | Rev: -1m
Date: Friday, September 07, 2018 | Sheet 7 of 106



Date	Revision	Description		
		Ball#	Old Name	New Name
01/Nov/2017	1.0	Initial revision	Initial revision	Initial revision
22/Dec/2017	1.1	AA9, AB10, AB2, AB8, AB9, AC8, AD9, AE10, AE8, AE9, AF10, AF2, AF8, AG8, AG9, AH9, AJ10, AJ8, AK2, AK9, AL10, AL8, AL9, AM8, V2, Y10, Y8	VCCGT	VCCCORE
	1.2	AL1	IST_TP[1]	RSVD
		AL2	IST_TP[0]	RSVD
		AL3	IST_TRIG[1]	RSVD
		AL4	IST_TRIG[0]	RSVD
		AM3, AT3, AU3, BJ34, BJ36, BP8, BP9, BT8, BT9, CR35	RSVD_TP	RSVD
		CF25	GPP_H21	GPP_H21 / XTAL_FREQ_SELECT

Document Number: 575414 Ver 1.2



R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

Bulk Decoupling Locations	Example	Notes
Vcc_{CORE} Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Domain	Primary Side cap	Secondary Side cap	Placement guideline
Vcc_{CORE}		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.
Vcc_{GT}	15x 22uF 0603		Place as close to the package as possible
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
Vcc_{SA}		*4x 0402*	*Placeholder only.*
		7x 10uF 0402	
	6x 10uF 0402		
	2x 47uF 0805 (6.3V)		
	2x 0805		*Placeholder Only*

Document Number: 575412 Ver 0.8

Domain	Primary Side cap	Secondary Side cap	Placement guideline
V_{DDQ}		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
Vcc_{IO}	4x 1uF 0201		Place as close to the package as possible
	6x 10uF 0402		Place as close to the package as possible
	4x 0402		*Placeholder Only*
Vcc_{PLL_OC}	1x 1uF 0402		Do not merge Vcc_{PLL}, Vcc_{PLL_OC} and Vcc_{GT} to any noisy and high current power rail and do not route them close/ adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
Vcc_{PLL}	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		*Placeholder Only.* Can be placed on as either Primary or back side cap.
Vcc_{ST}	1x 1uF 0402		
Vcc_{STG}	1x 1uF 0402		

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(VCCGT/VCCIO/VDDQ/VCCSA)

Size: A2 | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 8 of 106

Blanking

<Core Design>

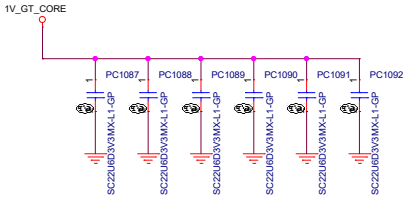
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
Date: Friday, September 07, 2018	Sheet 9 of 106	

Main Func = CPU

GT_VCORE WHL_U42

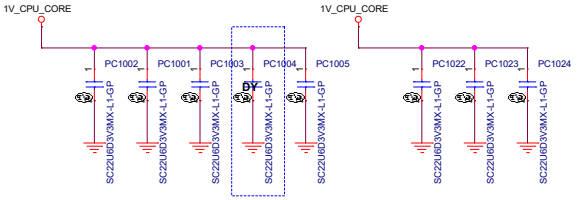
22uF	PCS	Cap
U42	6	

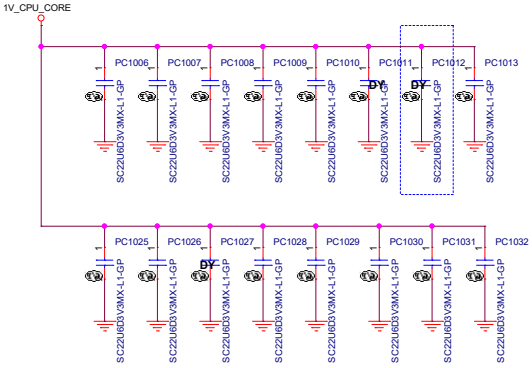


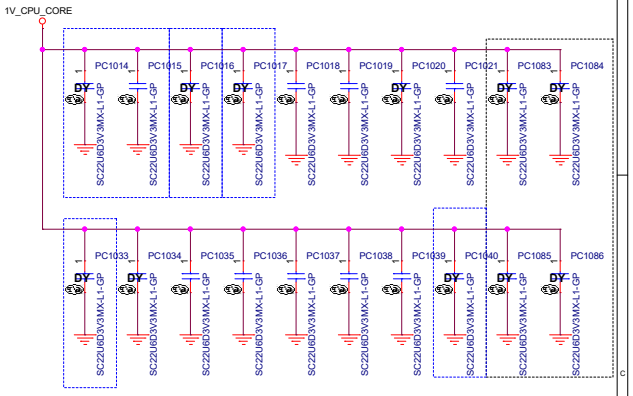
VCORE WHL_U42

U42
IccMax current-10ms max = 70 A

22uF	PCS	Cap
U42	39	330uF*2



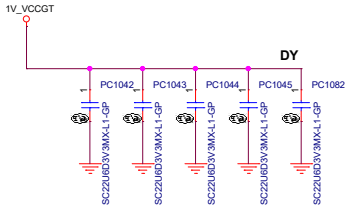


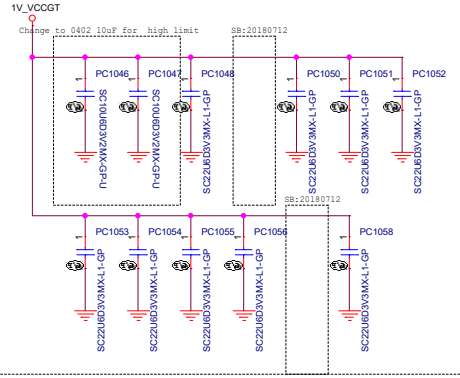


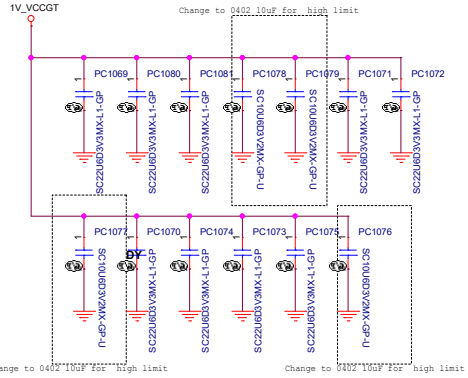
VCCGT WHL_U42

U42
IccMax current-10ms max = 31 A

22uF	PCS	Cap
RT	26	330uF*1



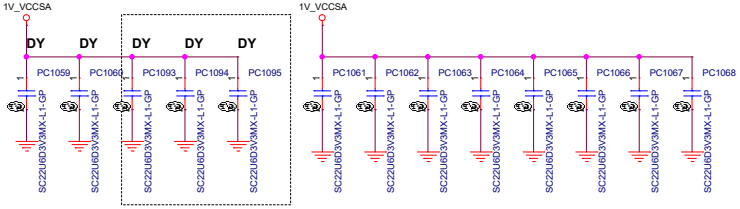




VCCSA WHL_U42

U42
IccMax current-10ms max = 5 A

22uF	PCS
RT	8

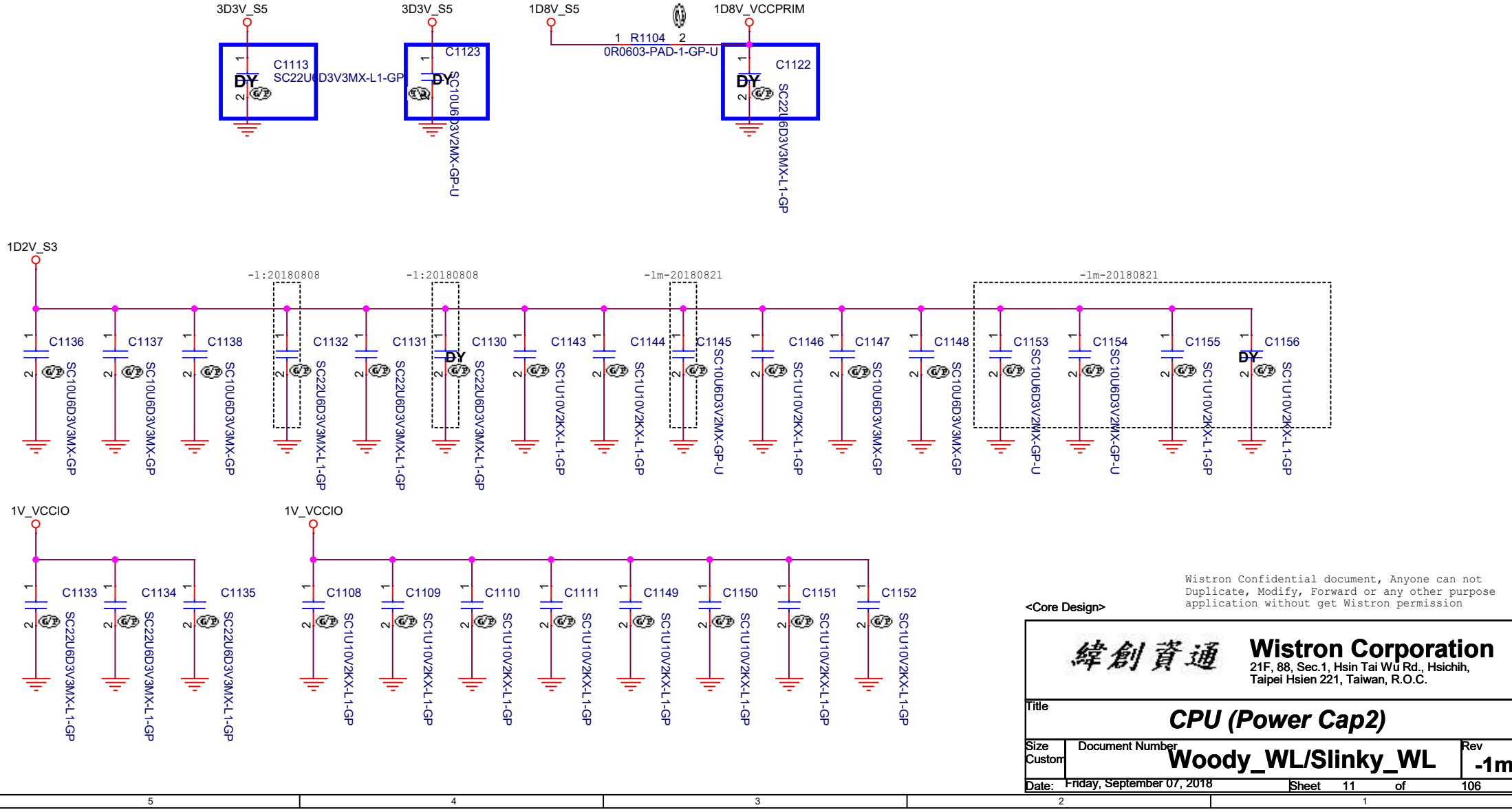


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CPU_(Power CAP1)*	
Size: Custom	Document Number: Woody_WL/Slinky_WL	Rev: -1m
Date: Friday, September 07, 2018	Sheet 10 of 106	

SSID = PCH



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (Power Cap2)**

Size	Document Number	Rev
Custom	Woody_WL/Slinky_WL	-1m

Date: Friday, September 07, 2018 Sheet 11 of 106

Main Func = MEMORY

SSID = DDR4 CHA

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63

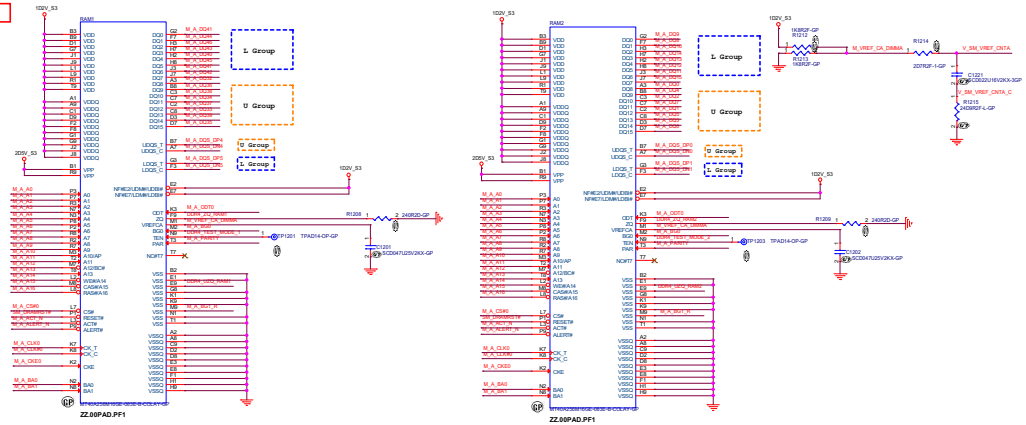


Figure 4-8. WHL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

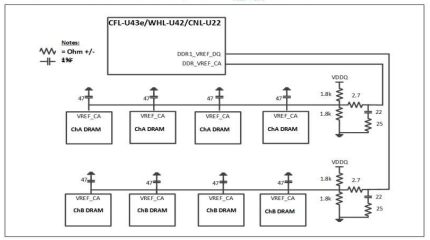


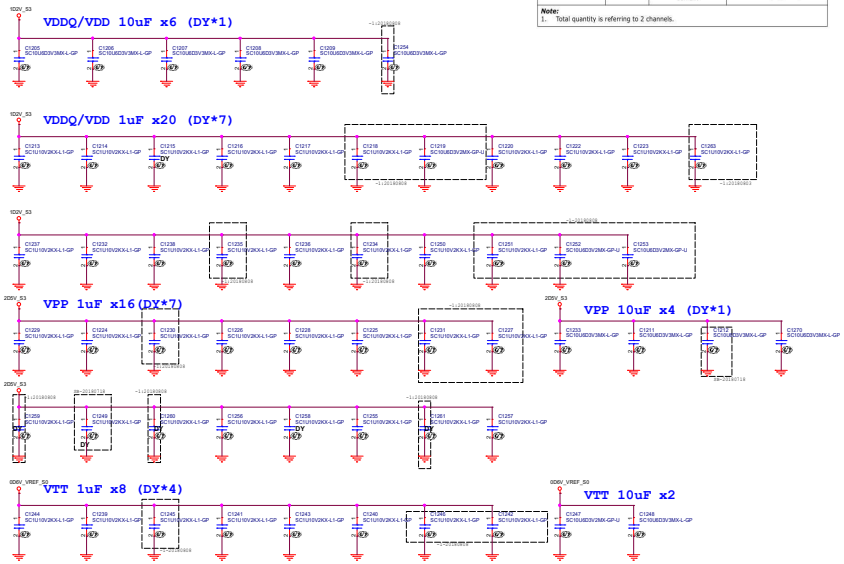
Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 per dram, as close as possible	32x 1µF (0402) (All stuffed)
		distribute evenly across domain, close by Drams	10x 10µF (0603) (All stuffed)
	VPP	2 per dram, as close as possible	16x 1µF (0402)
		distribute evenly across domain, close by Drams	5x 10µF (0603)
	VTT	distributed along termination resistors	16x 1µF (0402)
		distribute evenly across domain	4x 10µF (0603)

Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 2 of 2)

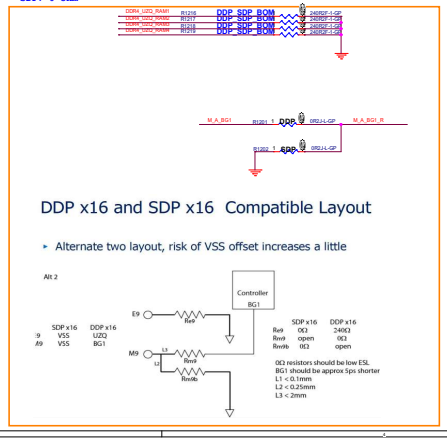
Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 Memory Down x8 - 8 Devices per Channel	VDDQ/VDD (shorted)	4 per dram, as close as possible	64x 1µF (0402) (min of 48 stuffed)
		distribute evenly across domain, close by Drams	20x 10µF (0603) (min of 12 stuffed)
	VPP	2 per dram, as close as possible	32x 1µF (0402)
		distribute evenly across domain, close by Drams	10x 10µF (0603)
	VTT	distributed along termination resistors	32x 1µF (0402)
		distribute evenly across domain	8x 10µF (0603)

Note:
1. Total quantity is referring to 2 channels.



SDP & DDP SETTING

DDP: 240 ohm
SDP: 0 ohm



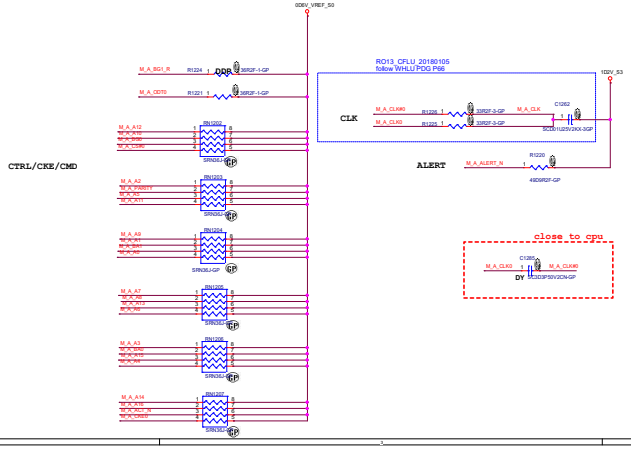
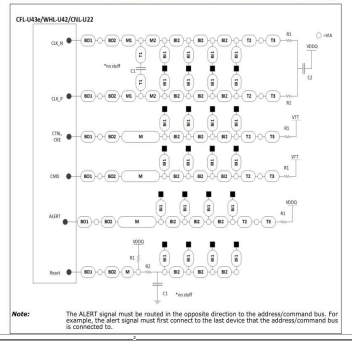


Figure 4-7. WHL U DDR4 x16 Memory Down CLK/CTRL/CKE/CMD/Reset Signal Topology



Note: The ALERT signal must be routed in the opposite direction to the address/command bus. For example, the alert signal must first connect to the last device that the address/command bus is connected to.

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

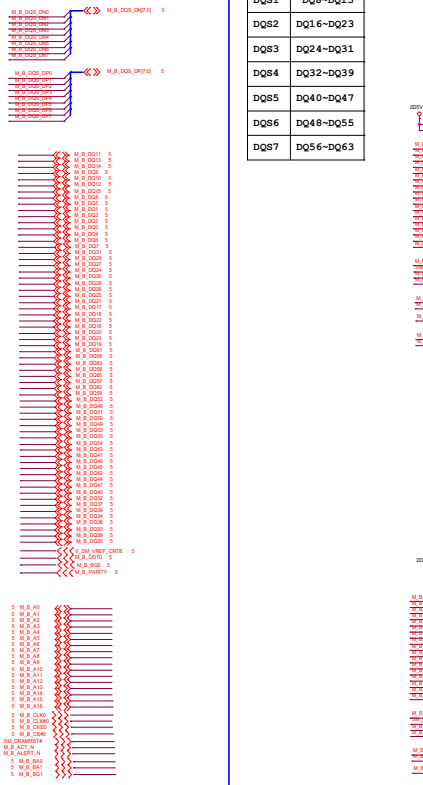
DDR (DDR4-CHA)

Woody WL/Slinky WL -1m

Main Func = MEMORY

SSID = DDR4 CHB

DQS0	DQ0~DQ7
DQS1	DQ8~DQ15
DQS2	DQ16~DQ23
DQS3	DQ24~DQ31
DQS4	DQ32~DQ39
DQS5	DQ40~DQ47
DQS6	DQ48~DQ55
DQS7	DQ56~DQ63



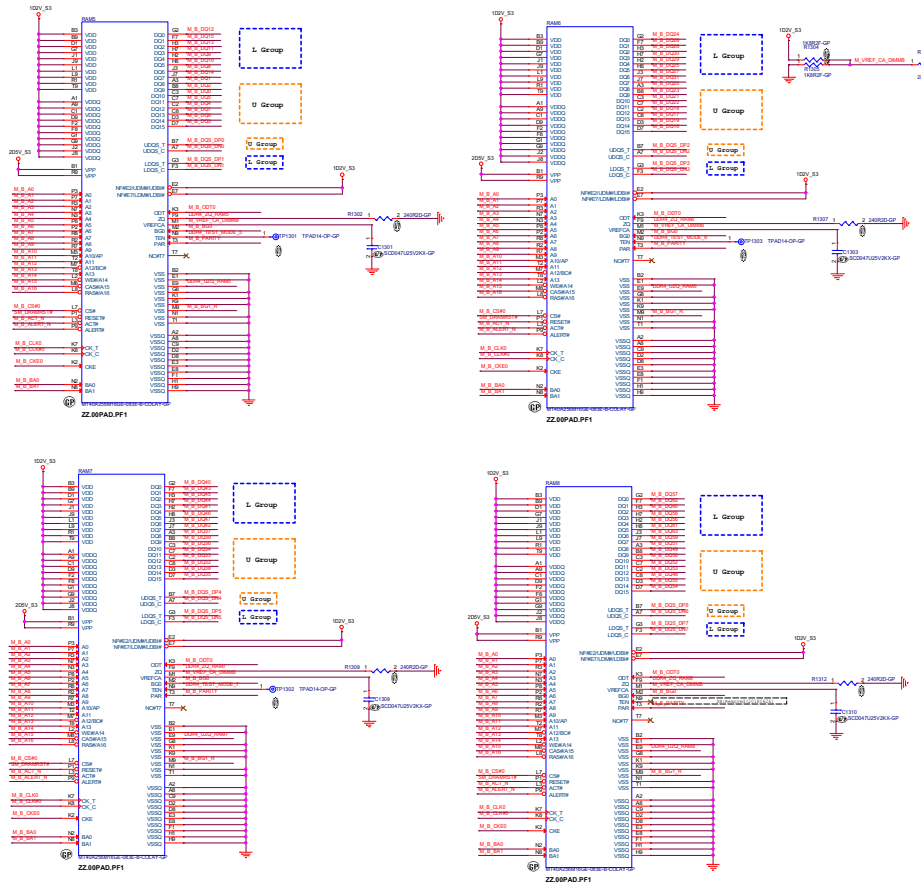


Figure 4-8. WHL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

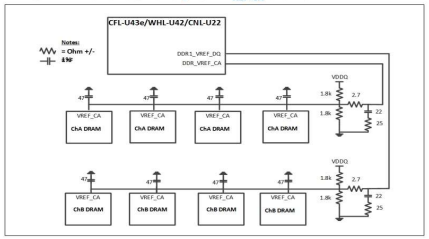


Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 1 of 2)

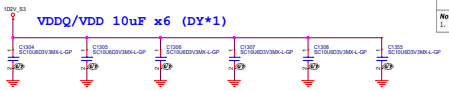
Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 Memory Down x16 - 4 Devices per Channel	VDDQ/VDD (shorted)	4 per dram, as close as possible	32x 1uF (0402) (All stuffed)
		distribute evenly across domain, close by Drams	10x 10uF (0603) (All stuffed)
	VPP	2 per dram, as close as possible	16x 1uF (0402)
		distribute evenly across domain, close by Drams	5x 10uF (0603)
	VTT	distributed along termination resistors	16x 1uF (0402)
		distribute evenly across domain	4x 10uF (0603)

Table 4-22. DDR4 Memory Down Power Plane Decoupling (Sheet 2 of 2)

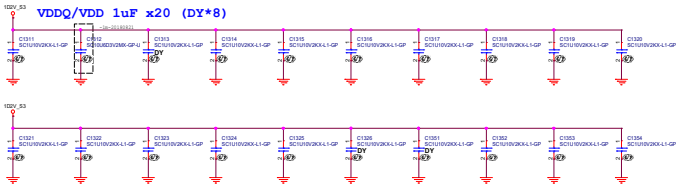
Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)
DDR4 Memory Down x8 - 8 Devices per Channel	VDDQ/VDD (shorted)	4 per dram, as close as possible	64x 1uF (0402) (min of 48 stuffed)
		distribute evenly across domain, close by Drams	20x 10uF (0603) (min of 12 stuffed)
	VPP	2 per dram, as close as possible	32x 1uF (0402)
		distribute evenly across domain, close by Drams	10x 10uF (0603)
	VTT	distributed along termination resistors	32x 1uF (0402)
		distribute evenly across domain	8x 10uF (0603)

Note:
1. Total quantity is referring to 2 channels.

VDDQ/VDD 10uF x6 (DY*1)

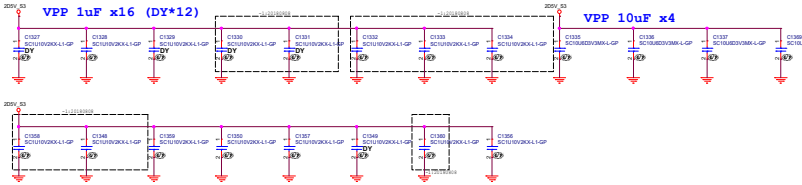


VDDQ/VDD 1uF x20 (DY*8)



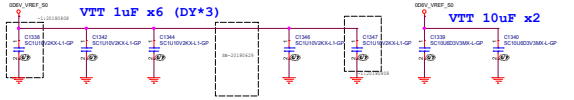
VPP 1uF x16 (DY*12)

VPP 10uF x4



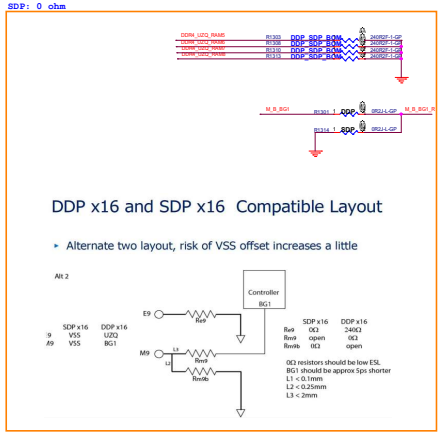
VTT 1uF x6 (DY*3)

VTT 10uF x2



SDP & DDP SETTING

DDP: 240 ohm
SDP: 0 ohm



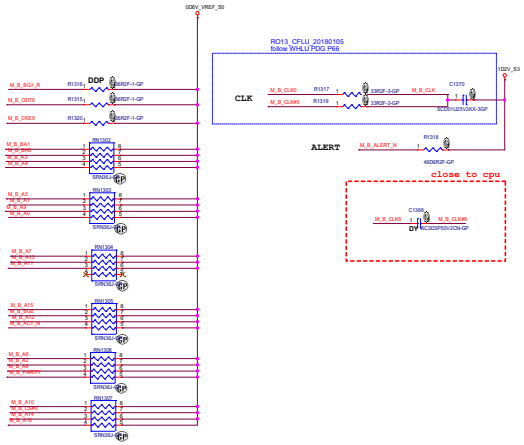
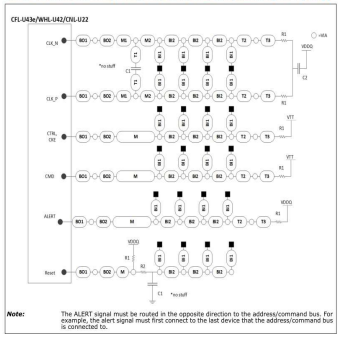


Figure 4-7. WHL U DDR4 x16 Memory Down CLK/CTRL/CKE/CMD/Reset Signal Topology



Note: The ALERT signal must be routed in the opposite direction to the address/command bus. For example, the alert signal must first connect to the last device that the address/command bus is connected to.

鋒創資通 Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

DDR (DDR4-CHB)

Woody_WL/Slinky_WL -1m

Friday, September, 2018

(Blanking)

<Core Design>

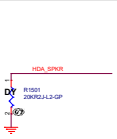
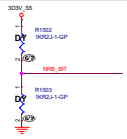
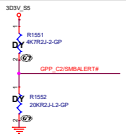
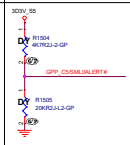
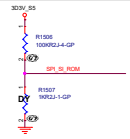
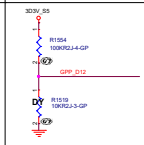
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

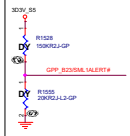
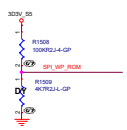
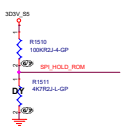
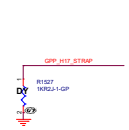
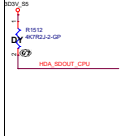
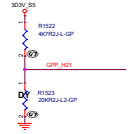
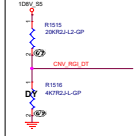
Title	***DDR (RSVD) (DDR4-CHA1)***	
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
Date: Friday, September 07, 2018	Sheet 14 of 106	

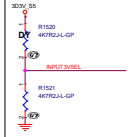
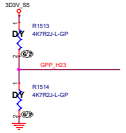
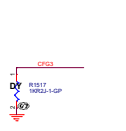
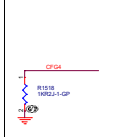
19,27 HDA_SPKR
20 NRB_BIT
18 GPP_C2/SMBALERT#
20 GPP_B22_GSPI1_MOSI
18 GPP_C5/SML0ALERT#
18,24,25,91 SPI_SI_ROM
20 GPP_D12
18 GPP_B23/SML1ALERT#
18,25 SPI_WP_ROM
18,25 SPI_HOLD_ROM
19 HDA_SDOUT_CPU
4 GPP_H17_STRAP
21 GPP_H21
20 CNV_RGI_DT
17 INPUT3VSEL
21 GPD_7
21 GPP_H23

6 CFG3
6 CFG4

Main Func = PCH

Description	Top Swap Override	No Reboot	TLS Confidentiality	Boot BIOS	eSPI or LPC	Reserved	Reserved
GPIO	GPP_B14	GPP_B18	GPP_C2	GPP_B22	GPP_C5	SPI0_MOSI	GPP_D12
Schematic							
High	Enable	Enable	Enable	LPC	eSPI		
Low	Disable	Disable	Disable	SPI	LPC		
	internal pull-down	internal pull-down	internal pull-down	internal pull-down	internal pull-down		

Description	Intel DCI-OOB	Reserved	Reserved	Reserved	Flash Descriptor Security Override	XTAL Frequency Select	CNV Mode select
GPIO	GPP_B23	SPI0_IO2	SPI0_IO3	GPP_H17	HDA_SDOUT	GPP_H21	GPP_F6
Schematic							
High	Enable			Enable	Disable	24MHz	Disable
Low	Disable			Disable	Enable	38.4Hz	Enable
	internal pull-down				internal pull-down	internal pull-down	internal pull-down

Description	3.0V Select	Reserved	eSPI_Flash shareing mode	Reserved	eDP enable		
GPIO	INPUT3VSEL	GPD_7	GPP_H23	CFG3	CFG4		
Schematic							
High	3.0V +/-5%		Enable		Disable		
Low	3.3V +/-5%		Disable		Enable		
	internal pull-down		internal pull-down		internal pull-up		

GPP_B14 / SPKR	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_B22 / GSPI1_MOSI	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset DCh, bit 6). **Bit 6 — Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
GPP_C5 / SML0ALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_B23 / SML1ALERT# / PCHHOT#	Intel® DCI-OOB	Rising edge of RSMRST#	This signal has an internal pull-down. 0 = Disable Intel® DCI-OOB (Default) 1 = Enable Intel® DCI-OOB ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling. This signal is in the primary well.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	A weak external pull-up is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable. ***Note:*** When a RF companion chip is connected to the PCH CNVi interface, the device internal pull-down resistor will pull the strap load to enable CNVi interface.
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* (SAFS is configured to '0' (eSPI is disabled)**

SML1ALERT#/ PCHHOT#/GPP_B23	•If USB 1.0 Port 1 is used for 4-wire DCI.OOB (BSSB), and alternate functionality is also used on the pin, pull up to V3.3S with >100K resistor to avoid noise. •If USB 3.1 Port 1 is used for DCI.OOB (BSSB) 4-wire BSSB, and NO alternate functionality is used, leave float. •If DCI.OOB (BSSB) 2+2 functionality is used, pull up to V3.3S with a 4.7K resistor.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (STRAP)

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 15 of 106

Main Func = PCH

USB3.0 port1

35 USB1_USB30_RX_N
35 USB1_USB30_RX_P
35 USB1_USB30_TX_N
35 USB1_USB30_TX_P
35 USB1_USB20_N
35 USB1_USB20_P

USB3.0 port2

35 USB2_USB30_RX_N
35 USB2_USB30_RX_P
35 USB2_USB30_TX_N
35 USB2_USB30_TX_P
36 USB2_USB20_N
36 USB2_USB20_P

TypeC

72 USB3_USB30_RX_N
72 USB3_USB30_RX_P
72 USB3_USB30_TX_N
72 USB3_USB30_TX_P
73 USB3_USB20_N
73 USB3_USB20_P

Small Board(USB2.0)

66,89 USB4_USB20_N
66,89 USB4_USB20_P

Others(USB2.0)

29 CCD_USB20_N
29 CCD_USB20_P
66,89 CARD1_USB20_N
66,89 CARD1_USB20_P
92 FP_USB20_N
92 FP_USB20_P
55 TS_USB20_N
55 TS_USB20_P

63 SSD_DEVSLP

M.2 SSD PCIE

63 SSD_PCIE_RX_N15
63 SSD_PCIE_RX_P15
63 SSD_PCIE_TX_N15
63 SSD_PCIE_TX_P15
63 SSD_PCIE_RX_N16
63 SSD_PCIE_RX_P16
63 SSD_PCIE_TX_N16
63 SSD_PCIE_TX_P16

HDD SATA

60 HDD_SATA_RX_N
60 HDD_SATA_RX_P
60 HDD_SATA_TX_N
60 HDD_SATA_TX_P

Document Number: 575412 Ver 0.9
220 nF nominal capacitors are recommended for Gen 3
100 nF nominal capacitors are recommended for Gen 2

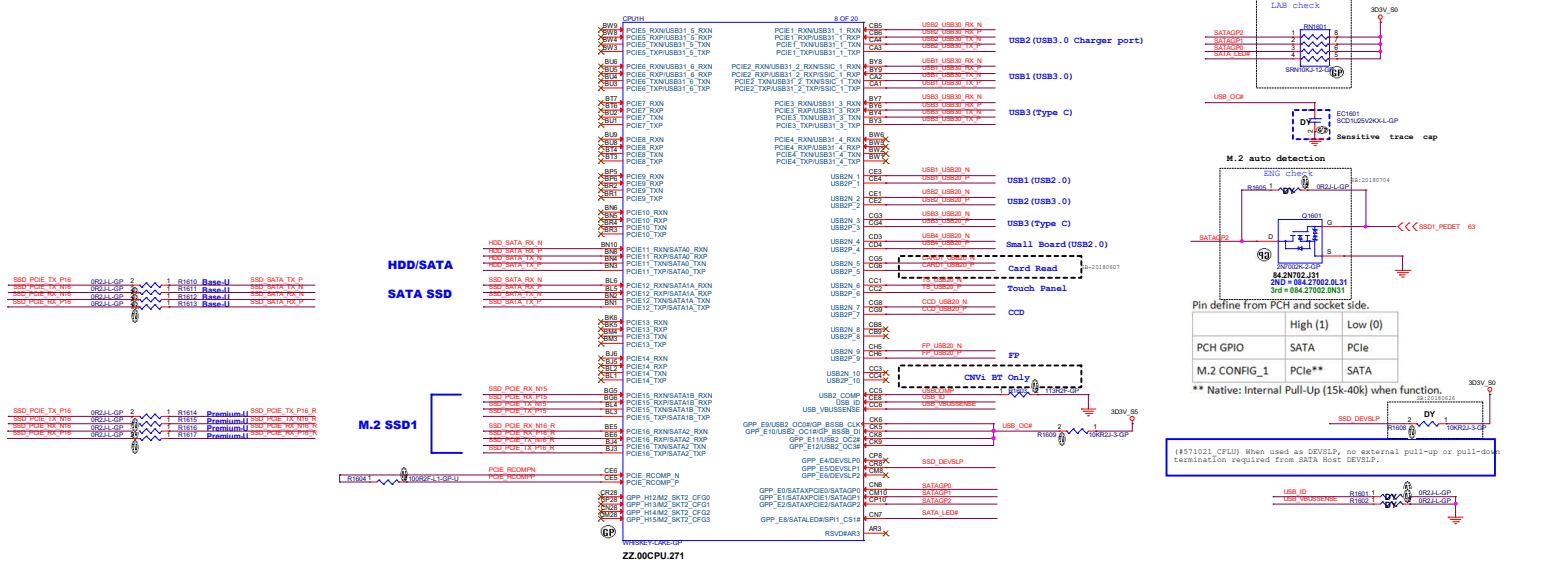


Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL U PCH-LP

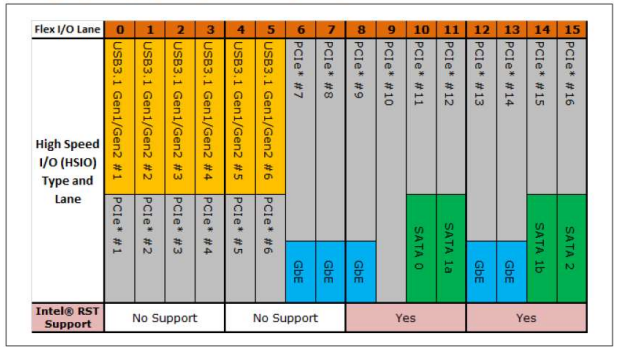


Figure 6-2. Supported PCH PCI Express* Link Configurations

PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3 Cycle Router #2				PCIe* Controller #4 Cycle Router #3			
Flex I/O Lane		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PCIe* Lane		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Premium-U	1x4	RP1				RP5				RP9				RP13			
	1x4 LR	RP1				RP5				RP9				RP13			
	2x2	RP1		RP3		RP5		RP7		RP9		RP11		RP13		RP15	
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12	RP13		RP15	RP16
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9		RP16	RP15	RP13	
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12	RP13	RP14	RP15	RP16

Table 1-3. PCH HSIO Detail

SKU	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Mainstream/ Base-U	USB 3.1 Gen1	USB 3.1 Gen1	USB 3.1 Gen1	USB 3.1 Gen1	PCIe*	PCIe*	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	SATA 0/ PCIe*	SATA 1A/ PCIe*	GbE 0D/ PCIe*	GbE 0E/ PCIe*	PCIe*	PCIe*
Premium-U	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0	PCIe*/ SATA 1A	GbE 0D/ PCIe*	GbE 0E/ PCIe*	PCIe*/ SATA 1B	PCIe*/ SATA 2
Premium-Y	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	PCIe*/ USB 3.1 Gen1/ Gen2	GbE 0A/ PCIe*	GbE 0B/ PCIe*	GbE 0C/ PCIe*	PCIe*	PCIe*/ SATA 0	PCIe*/ SATA 1A	GbE 0D/ PCIe*	GbE 0E/ PCIe*	Not Available	Not Available

CHIPSET SKU	Max Number of USB 2.0 Ports	USB 2.0 Port # 1	USB 2.0 Port # 2	USB 2.0 Port # 3	USB 2.0 Port # 4	USB 2.0 Port # 5	USB 2.0 Port # 6	USB 2.0 Port # 7	USB 2.0 Port # 8	USB 2.0 Port # 9	USB 2.0 P10 / Integrated Intel® Wireless-AC
Cannon Lake Y Intel® Core™ Processors	6										
Coffee Lake U Intel® Core™ Processors and Intel® Core™ U Intel® Core™ Processors	10										
Cannon Lake U Intel® Pentium™ Processors and Cannon Lake U Intel® Celeron™ Processors	8										

(#543016) Unused SATAGP[2:0]/GPP_E[2:0] pins must be terminated to either 3.3 V rail or GND using 8.2 KΩ to 10 KΩ on the motherboard.
Do not use both pull-up and pull-down. Either pull-up or pull-down is acceptable.

6.4.5 PCH PCI Express* Impedance Compensation Guidelines

Figure 6-6. PCH PCIE_RCOMPP and PCIE_RCOMPN Connections

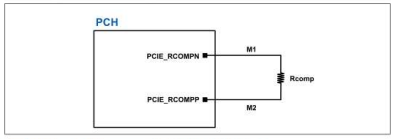


Table 6-10. PCH PCI Express* Compensation Routing Guidelines

Parameter	Segment	Stack-up (MS/SL/DSL)	Units	2.5 GT/s Routing	5 GT/s Routing	8 GT/s Routing
Reference Plane	M1, M2	MS/SL/DSL	NA	GND	GND	GND
Series Resistor	M1, M2	MS	Ohms	100 +/-1%	100 +/-1%	100 +/-1%
Motherboard Max Via Count	M1, M2	NA	vias	2	2	2
Motherboard Length Matching	M1, M2	MS/SL/DSL	mm(mils)	M1- M2 = ± 0.127mm (± 5mils)		

Notes:
1. Recommended placing a VSS shield of at least 4mils (0.1016mm) wide between the RCOMP signals and any adjacent I/O signal
2. Avoid routing close to any clocks
3. Micro-Vias within the breakout area are not counted against maximum via total
4. Must maintain low DC resistance routing (<0.1 ohm)

Bluetooth USB host bus (positive) for standard CNV. Optional to connect to a Bluetooth USB+ pin on the Bluetooth module. Port 10 is the recommended port but other USB2 ports can be selected for this function.

CNVi :

Bluetooth USB host bus (positive) for standard CNV. Optional to connect to a Bluetooth USB+ pin on the Bluetooth module. Port 10 is the recommended port but other USB2 ports can be selected for this function.

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCIE/SATA/USB)
Size: Custom | Document Number: Woody WL/Slinky WL | Rev: -1m
Date: Friday, September 07, 2018 | Sheet 16 of 106

SSID = PCH

24,63,68,89,91 PLT_RST#
24 RSMRST#_KBC
45,53,72 PWR_3D3V_PG
24,40 ALL_SYS_PWRGD
24 SYS_PWROK
40 PCH_PWROK
24,63 PCIE_WAKE#
24,40,53,60 PM_SLP_S3#
24,40,51 PM_SLP_S4#
24 PM_PWRBTN#
24 AC_PRESENT
15 INPUT3VSEL

CPU1K — 11 OF 20 — WHISKEY-LAKE-GP

PLT_RST# BJ35 — GPP_B13/PLTRST#
XDP_DBRESET# CN10 — SYS_RESET#
PM_RSMRST# BR36 — RSMRST#
H_CPUPWRGD AR2 — PROCPWRGD
VCCST_PWRGD BJ2 — VCCST_PWRGOOD
SYS_PWROK CR10 — SYS_PWROK
PM_PCH_PWROK BP31 — PCH_PWROK
PCH_DPWROK BP30 — DSW_PWROK
BV34 — GPP_A13/SUSWARN#/SUSPWRDACK
BY32 — GPP_A15/SUSACK#
PCIE_WAKE# BU30 — WAKE#
LAN_WAKE# BU32 — GPD2/LAN_WAKE#
GPD11/LANPHYPC BU34 — GPD11/LANPHYPC

GPP_B12/SLP_S0# BJ37 — SB:20180627
GPD4/SLP_S3# BU36 — PM_SLP_S3#
GPD5/SLP_S4# BU27 — PM_SLP_S4#
GPD10/SLP_S5# BT29
SLP_SUS# BU29
SLP_LAN# BT31
GPD9/SPL_WLAN# BT30
GPD6/SLP_A# BU37
GPD3/PWRBTN# BU28 — PM_PWRBTN#
GPD1/ACPRESENT BU35 — AC_PRESENT
GPD0/BATLOW# BV36 — BATLOW#
INTRUDER# BR35 — SM_INTRUDER#
GPP_B11/EXT_PWR_GATE# CC37 — EXT_PWR_GATE#
GPP_B2/VRALERT# CC36 — SB:20180627
Strap — INPUT3VSEL BT27 — INPUT3VSEL

PCH_PWROK R1706 1 2 0R0402-PAD-1-GP
PM_RSMRST# R1704 1 2 0R0402-PAD-1-GP
SB:20180627

3D3V_S5

RSMRST#_KBC 1
PWR_3D3V_PG 2
U1701 DY
A VCC 5
B
3 GND Y 4 PM_RSMRST#
U74LVC1G08G-AL5-R-GP-U
73.01G08.EHG
2nd = 73.01G08.DHG
C1710 SCD1U25V2KX-L-GP

RSMRST#_KBC 1 R1707 2 PM_RSMRST#
0R0402-PAD
SB:20180627

3D3V_S0

R1718 1KR2F-L1-GP
ALL_SYS_PWRGD 1 R1716 2 10KR2F-L1-GP
VCCST_PWRGD
R1719 4K7R2J-L-GP
C1711 SC100P50V2JN-L-GP

SB:20180627

3D3V_S0

XDP_DBRESET# R1701 1 2 10KR2J-3-GP
PM_RSMRST# R1702 1 2 10KR2F-L1-GP
PCH_PWROK R1703 1 DY 2 10KR2J-3-GP
H_CPUPWRGD R1714 1 DY 2 10KR2J-3-GP
SYS_PWROK R1705 1 DY 2 10KR2J-3-GP

3D3V_S5

RN1701
AC_PRESENT 1
PM_PWRBTN# 2
4
3
SRN10KJ-L-GP

3D3V_S5

RN1704
PCIE_WAKE# 1
LAN_WAKE# 2
GPD11/LANPHYPC 3
BATLOW# 4
8
7
6
5
SRN10KJ-L-GP

3D3V_RTC_AUX

SM_INTRUDER# R1730 1 2 1MR2J-1-GP

3D3V_S5

EXT_PWR_GATE# R1731 1 2 100KR2F-L1-GP
H_CPUPWRGD
DY EC1701 SCD1U25V2KX-L-GP
Sensitive trace cap

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PMU)
Size: Custom
Document Number: Woody_WL/Slinky_WL
Rev: -1m
Date: Friday, September 07, 2018
Sheet 17 of 106

SSID = PCH

24,25,91 SPI_CLK_ROM
24,25,91 SPI_SO_ROM
15,24,25,91 SPI_SI_ROM
15,25 SPI_WP_ROM
15,25 SPI_HOLD_ROM
24,25 SPI_CS_CPU_N0
91 SPI_CS_CPU_N2

24 H_RCIN#
24,68 INT_SERIRQ
69 SMB_DATA_CPU
69 SMB_CLK_CPU
24,55,70,72 SML1_CLK
24,55,70,72 SML1_DATA
15 GPP_C2/SMBALERT#
15 GPP_C5/SML0ALERT#
15 GPP_B23/SML1ALERT#
24,68 LPC_AD_CPU_P0
24,68 LPC_AD_CPU_P1
24,68 LPC_AD_CPU_P2
24,68 LPC_AD_CPU_P3
24,68 LPC_FRAME#_CPU
24 LPC_CLK_KBC
68 LPC_CLK_DBG
24 PM_CLKRUN#_EC

CPU1E 5 OF 20
WHISKEY-LAKE-GP
ZZ.00CPU.271

Strap
HDD_G-sensor
KBC /G-SENSOR/TYPE-C

SB:20180627

Q1801 2N7002KDW-1-GP
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.27002.0E7C

R1809 22R2J-L1-GP
R1810 22R2J-L1-GP
LAB
EC1802 EC1801
SC22P50V2JN4GP

RN1803 SRN10KJ-L-GP
RN1802 SRN10KJ-L-GP
RN1811 SRN2K2J-1-GP
RN1807 SRN2K2J-1-GP
R1811 8K2R2F-1-GP

63 SSD1_CLK_CPU_N
63 SSD1_CLK_CPU_P
63 SSD1_CLKREQ_CPU_N
24 RTCRST_ON
61 SUS_CLK_CPU
61 PULSAR_38P4M_REFCLK

CPU1J 10 OF 20
WHISKEY-LAKE-GP
ZZ.00CPU.271

NGFF1

R1831 60D4R2F-GP
CNVi
0R2J-L-GP
Close to CM3
R1812 10KR2J-3-GP
LAB Verify for EMC

R1801 10KR2J-3-GP
RN1801 SRN20KJ-1-GP
RTC Reset
G1801 GAP-OPEN
SC1U10V2KX-L1-GP
SC1U10V2KX-L1-GP

For AFR
Q1802 2N7002K-2-GP
R1804 100KR2F-L-3-GP
R1816 2K2R2J-L1-GP
84.2N702.J31
2nd = 084.27002.0L31
3rd = 084.27002.0N31

XTL_24M_X1_CPU R1839 0R0402-PAD-1-GP XTL_24M_X1_R
XTL_24M_X2_CPU R1840 0R0402-PAD-1-GP XTL_24M_X2_R
C1807 SC15P50V2JN-L-GP
C1808 SC15P50V2JN-L-GP
R1841 200KR2F-L-3-GP
X1801 XTAL-24MHZ-182-GP
082.30006.0531
2nd = 082.30006.0561

XTL_32K_X1_CPU R1815 10MR2J-L-GP XTL_32K_X2_CPU
X1802 XTAL-32D768KHZ-98-GP
082.30003.0301
2nd = 082.30003.0191
C1804 SC15P50V2JN-L-GP
C1803 SC15P50V2JN-L-GP

LAB: Removed TVS 20180424

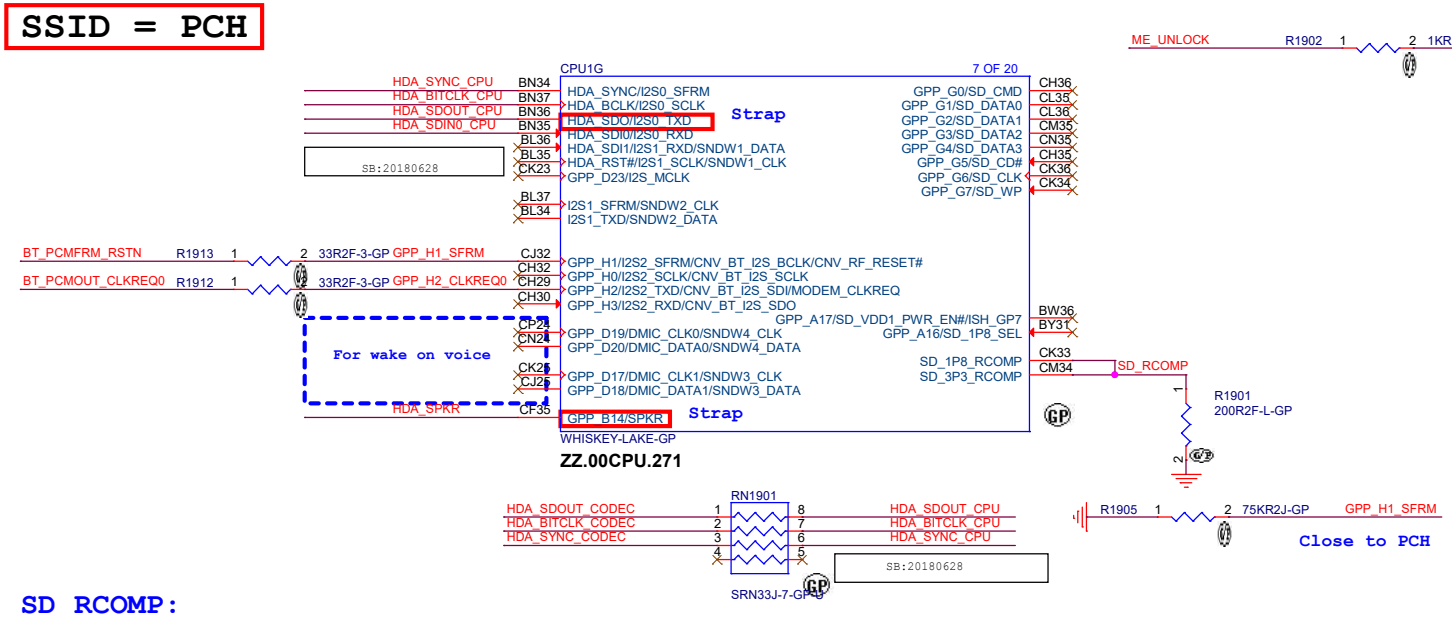
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(SPI/ESPI/SMBS/XTAL/CLK)
Size: A2
Document Number: Woody_WL/Slinky_WL
Rev: -1m
Date: Friday, September 07, 2018
Sheet 18 of 106

SSID = PCH

27 HDA_SYNC_CODEC
27 HDA_BITCLK_CODEC
15 HDA_SDOUT_CPU
27 HDA_SDOUT_CODEC
24 ME_UNLOCK
27 HDA_SDIN0_CPU
15,27 HDA_SPKR
61 BT_PCMFRM_RSTN
61 BT_PCMOUT_CLKREQ0

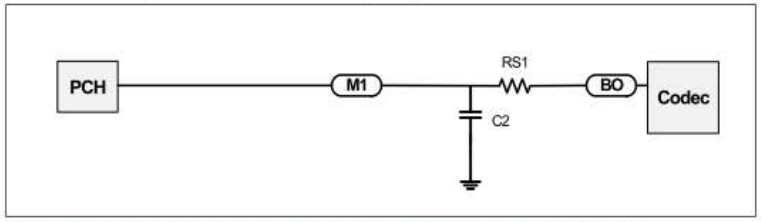


SD_RCOMP:

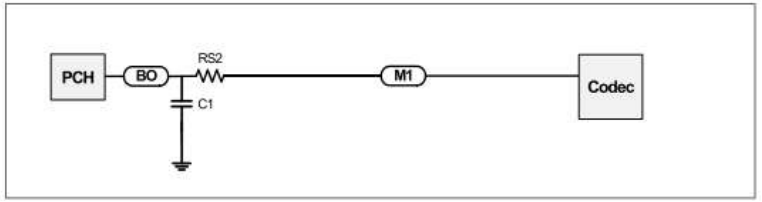
SD_3P3_RCOMP and SD_1P8_RCOMP precision resistors are still needed, even if SDXC interface is not used.

Document Number: 575412 Ver 0.8

HDA_SDI Single Load Audio Down Topology



HDA_SDO/HDA_SYNC/HDA_BCLK/HDA_RST# Audio Down Topology



Document Number: 566439 Ver 2.0

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (HDA/I2S/SD/DMIC)**

Size: Custom | Document Number: **Woody_WL/Slinky_WL** | Rev: **-1m**

Date: Friday, September 07, 2018 | Sheet 19 of 106

SSID = PCH

15 NRB_BIT
25 RTC_DET#
15 GPP_B22_GSPI1_MOSI
68 LPSS_UART2_RXD
68 LPSS_UART2_TXD
68 LPSS_UART2_RTS#
68 LPSS_UART2_CTS#
65 PM_TP_DATA
65 PM_TP_CLK
24,55 TS_I2C0_SDA_CON
24,55 TS_I2C0_SCL_CON
15 GPP_D12
55 TOUCH_S_RST#
55 TOUCH_DET#
61 CNV_BRI_RSP
61 CNV_RGI_DT_R
61 CNV_BRI_DT_R
61 CNV_RGI_RSP
15,20 CNV_RGI_DT
15,20 CNV_RGI_DT
91 PIRQA#

CPU1F — 6 OF 20

TOUCH_DET# CC27 GPP_B15/GSPI0_CS0#
PIRQA# CC32 GPP_A7/PIRQA#/GSPI0_CS1#
CE28 GPP_B16/GSPI0_CLK
CE27 GPP_B17/GSPI0_MISO
NRB_BIT CE29 GPP_B18/GSPI0_MOSI Strap
RTC_DET# CA31 GPP_B19/GSPI1_CS0#
CA32 GPP_A11/PME#/GSPI1_CS1#/SD_VDD2_PWR_EN#
PSW_CLR# CC29 GPP_B20/GSPI1_CLK
CC30 GPP_B21/GSPI1_MISO
GPP_B22_GSPI1_MOSI CA30 GPP_B22/GSPI1_MOSI Strap
CNV_BRI_RSP CK20 GPP_F5/CNV_BRI_RSP
CNV_RGI_DT_R 1 R2014 2 0R0402-PAD-1-GP CNV_RGI_DT CG19 GPP_F6/CNV_RGI_DT Strap
CNV_BRI_DT_R 1 R2015 2 0R0402-PAD-1-GP CNV_BRI_DT CJ20 GPP_F4/CNV_BRI_DT
CNV_RGI_RSP CH19 GPP_F7/CNV_RGI_RSP

LAB verify
Intel checklist suggest 75ohm

LPSS_UART2_RXD CR12 GPP_C20/UART2_RXD
LPSS_UART2_TXD CP12 GPP_C21/UART2_TXD
LPSS_UART2_RTS# CN12 GPP_C22/UART2_RTS#
LPSS_UART2_CTS# CM12 GPP_C23/UART2_CTS#

Touch Panel

TS_I2C0_SDA_CON CM11 GPP_C16/I2C0_SDA
TS_I2C0_SCL_CON CN11 GPP_C17/I2C0_SCL

Touch Pad

PM_TP_DATA CK12 GPP_C18/I2C1_SDA
PM_TP_CLK CJ12 GPP_C19/I2C1_SCL

CF27 GPP_H4/I2C2_SDA
CF29 GPP_H5/I2C2_SCL
CH27 GPP_H6/I2C3_SDA
CH28 GPP_H7/I2C3_SCL
CJ30 GPP_H8/I2C4_SDA
CJ31 GPP_H9/I2C4_SCL

WHISKEY-LAKE-GP

GPP_D9/ISH_SPI_CS#/GSPI2_CS0# CN22 TPM_ID
GPP_D10/ISH_SPI_CLK/GSPI2_CLK CR22 TOUCH_S_RST#
GPP_D11/ISH_SPI_MISO/GSPI2_MISO CM22
GPP_D12/ISH_SPI_MOSI/GSPI2_MOSI CP22 GPP_D12 Strap

GPP_D5/ISH_I2C0_SDA CK22
GPP_D6/ISH_I2C0_SCL CH20
GPP_D7/ISH_I2C1_SDA CH22
GPP_D8/ISH_I2C1_SCL CJ22
GPP_H10/I2C5_SDA/ISH_I2C2_SDA CJ27
GPP_H11/I2C5_SCL/ISH_I2C2_SCL CJ29

GPP_D13/ISH_UART0_RXD CM24
GPP_D14/ISH_UART0_TXD CN23
GPP_D15/ISH_UART0_RTS#/GSPI2_CS1# CM23
GPP_D16/ISH_UART0_CTS#/SML0BALERT# CR24

GPP_C12/UART1_RXD/ISH_UART1_RXD CG12
GPP_C13/UART1_TXD/ISH_UART1_TXD CH12
GPP_C14/UART1_RTS#/ISH_UART1_RTS# CF12
GPP_C15/UART1_CTS#/ISH_UART1_CTS# CG14

GPP_A18/ISH_GP0 BW35 CONFIG3
GPP_A19/ISH_GP1 BW34 CONFIG4
GPP_A20/ISH_GP2 CA37 CONFIG1
GPP_A21/ISH_GP3 CA36 CONFIG2
GPP_A22/ISH_GP4 CA35
GPP_A23/ISH_GP5 CA34
GPP_A12/ISH_GP6/BM_BUSY#/SX_EXIT_HOLDOFF# BW37

Pass Word Clear

3D3V_S0
PSW_CLR# R2020 1 2 2K2R2J-L1-GP
G2001 GAP-OPEN

PIRQA# R2053 1 DY 2 10KR2F-L1-GP 3D3V_S0
TOUCH_S_RST# R2001 1 DY 2 10KR2F-L1-GP 3D3V_S0
RTC_DET# R2003 1 2 10KR2F-L1-GP 3D3V_S5

3D3V_S5
R2021 10KR2F-L1-GP NON_TPM
TPM_ID
R2002 10KR2F-L1-GP TPM

SB:20180627

3D3V_S5
R2004 10KR2J-3-GP
CONFIG3
R2005 10KR2J-3-GP DY

3D3V_S5
R2006 10KR2J-3-GP
CONFIG4
R2007 10KR2J-3-GP DY

1D8V_S5
R6138 0R0402-PAD
CNV_RGI_RSP
CNV_BRI_RSP
DY RN2001 SRN20KJ-1-GP
1D8V_3D3V

3D3V_S0
RN2011 SRN2K2J-4-GP
TS_I2C0_SDA_CON
TS_I2C0_SCL_CON
PM_TP_CLK
PM_TP_DATA

Close to PCH

3D3V_S5
R2008 10KR2J-3-GP
CONFIG1
R2009 10KR2J-3-GP DY

3D3V_S5
R2010 10KR2J-3-GP
CONFIG2
R2011 10KR2J-3-GP DY

Vendor	CONFIG4	CONFIG3	CONFIG2	CONFIG1	WISTRON PN	Vendor PN	Capacity	DDP/SDP
HYNIX	0	0	0	0	KN.8GB0G.049	H5AN8G6NAFR-UHC	8Gb	SDP
MICRON	0	0	0	1	KN.8GB04.013	MT40A512M16JY-083E:B	8Gb	SDP
SAMSUNG	0	0	1	0	KN.8GB0B.048	K4A8G165WB-BCRC	8Gb	SDP
HYNIX	0	0	1	1	KN.0040G.015	H5AN4G6NAFR-TFC	4Gb	SDP
HYNIX	0	1	0	0	KN.0040G.016	H5AN4G6NAFR-UHC	4Gb	SDP
MICRON	0	1	0	1	KN.00404.010	MT40A256M16GE-083E:B	4Gb	SDP
SAMSUNG	0	1	1	0	KN.0040B.014	K4A4G165WE-BCRC	4Gb	SDP
HYNIX	0	1	1	1	KN.0160G.010	H5ANAG6NAMR-UHC	16Gb	SDP
MICRON	1	0	0	0	KN.01604.001	MT40A1G16WBU-083E:B	16Gb	DDP
MICRON	1	0	0	1	KN.8GB04.027	MT40A512M16LY-075:E LF+HF	8Gb	SDP
HYNIX	1	0	1	0	KN.8GB0G.061	H5AN8G6NCJR-VKC LF+HF	8Gb	SDP
MICRON	1	0	1	1	KN.01604.003	MT40A1G16KNR-075:E LF+HF	16Gb	DDP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (UART/I2C/ISH)
Size: A3 | Document Number: Woody_WL/Slinky_WL | Rev: -1m
Date: Friday, September 07, 2018 | Sheet 20 of 106

SSID = PCH

Primary Well Group F (1.8 V Only)

Document Number: 566439 Ver.2.0

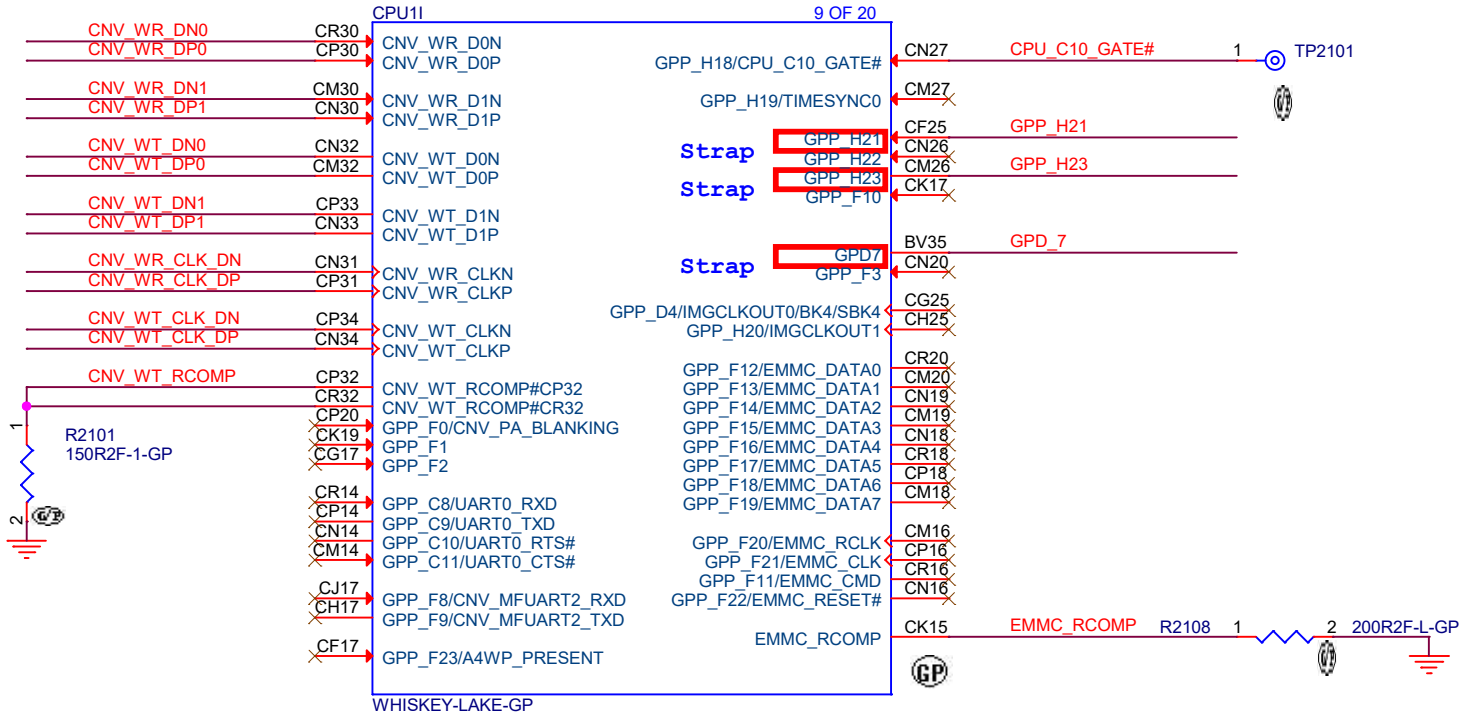
15 GPP_H21
15 GPP_H23
15 GPD_7

61 CNV_WR_DN0
61 CNV_WR_DP0
61 CNV_WR_DN1
61 CNV_WR_DP1

61 CNV_WT_DN0
61 CNV_WT_DP0
61 CNV_WT_DN1
61 CNV_WT_DP1

61 CNV_WR_CLK_DN
61 CNV_WR_CLK_DP

61 CNV_WT_CLK_DN
61 CNV_WT_CLK_DP



ZZ.00CPU.271

Table 7-23. eMMC RCOMP Routing Guidelines

Signal	Trace Width	Resistor Value	Isolation Spacing	Max Length
EMMC_RCOMP	M1: 0.10mm/4 mils min(breakout); typically 0.203-0.305mm/ 8-12 mils trace. Must maintain low DC resistance of <0.1 Ohm.	200 Ohm +/- 1% external resistor pull down to GND.	At least 0.308mm/12 mils to any adjacent I/O.	NA

Document Number: 575412 Ver 0.8

<Core Design>

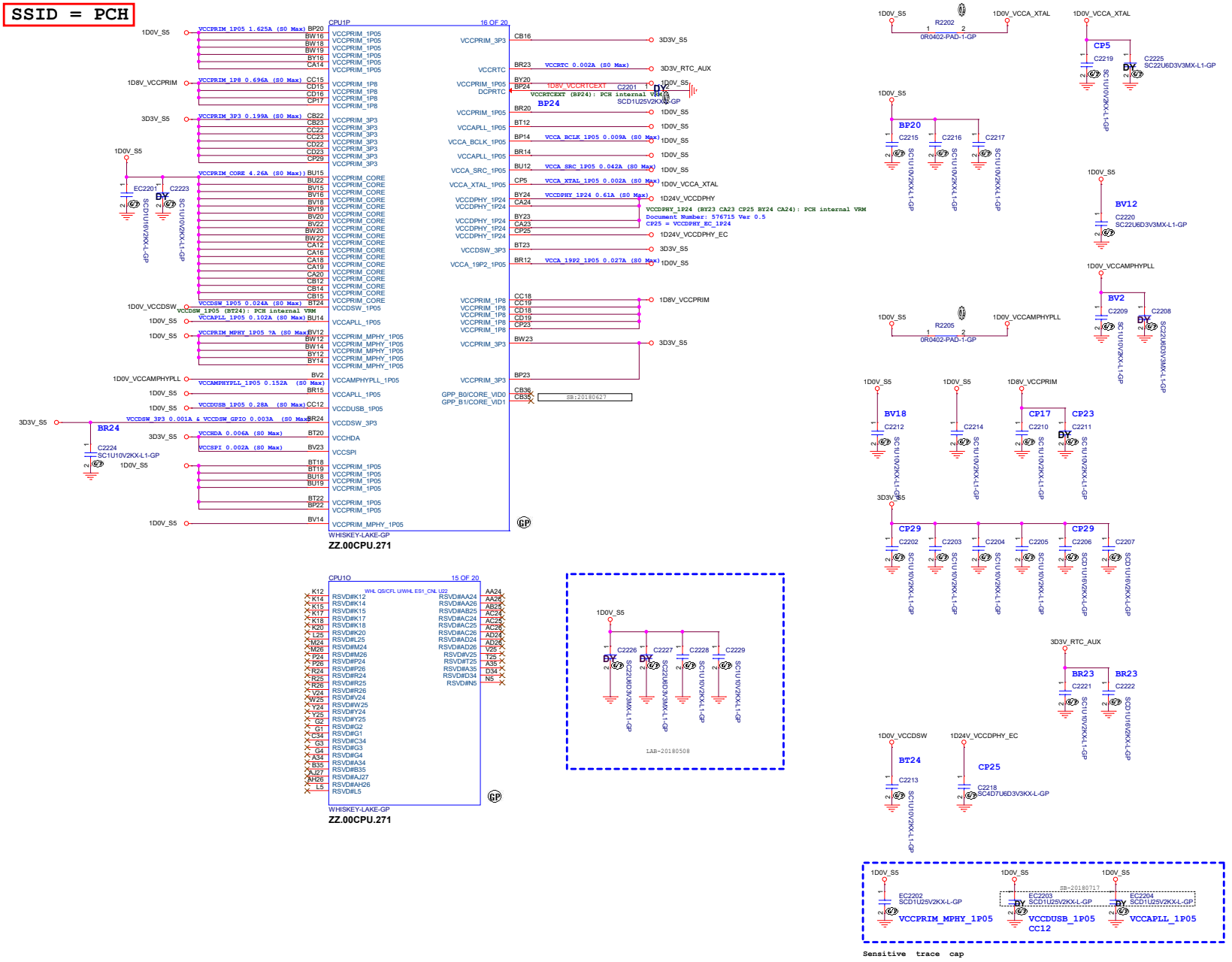
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (EMMC/CNVi)

Size: A4 | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 21 of 106

SSID = PCH



Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.05A	VCCA_19P2_1P05	BR12	-	-	-	-	-
	VCCA_OC_1P05	BP14	-	-	-	-	-
	VCCA_SRC_1P05	BU12	-	-	-	-	-
	VCCA_XTAL_1P05	CP5	1uF	0402	1	E	CP5
	VCCDUSB_1P05	CC12	-	-	-	-	
	VCCPRIM_1P05	BT12, BR14, BR15, BU14, BT22, BP22, BP20, BW16, BW18, BW19, BY16, CA14, BR20, BY20, BT18, BT19, BU18, BU19	1uF	0402	1	E	BP20
	VCCMPHYGTAON_1P05	BV12, BW12, BW14, BY12, BY14, BV14	22uF	0603	1	E	BV12
	VCCAMPHYPLL_1P05	BV2	1uF	0402	1	E	BV2
V1.05A / V0.75A	VCCPRIM_CORE	BU15, BU22, BV15, BV16, BV18, BV19, BV20, BV22, BW20, BW22, CA12, CA16, CA18, CA19, CA20, CB12, CB14, CB15	1uF	0402	1	E	BV18, Note 1

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (R)unway / (E)dge	Place capacitor(s) near ball(s)
V1.8A	VCCPRIM_1P8	CC18, CC19, CD18, CD19, CP23,CC15, CD15, CD16, CP17	1uF	0402	1	E	CP17
			1uF	0402	1	E	CP23, Note 1
V3.3A	VCCPRIM_3P3	CB22, CB23, CC22, CC23, CD22, CD23, CP29,BW23, BP23, CB16	0.1uF	0402	1	E	CP29, Note 1
			1uF	0402	1	E	CP29, Note 1
V3.3A/ V1.8A	VCCSPI	BV23	-	-	-	-	-
V3.3A/ V1.5A/ V1.8A	VCCHDA	BT20	-	-	-	-	-
V3.3DSW	VCCDSW_GPIO	BR24, BT23	1uF	0402	1	E	BR24, Note 1
V3.3RTC	VCCRTC	BR23	1uF	0402	1	E	BR23
			0.1uF	0402	1		
PCH Internal VRM	VCCDSW_1P05	BT24	1uF	0402	1	E	BT24
	VCCRTCEXT	BP24	1uF	0201	1	E	BP24, Note 1
	VCCDPHY_1P24	BY23, CA23, CP25, BY24, CA24	4.7uF	0402	1	E	CP25

Supply	Value	Quantity	Type	Notes
VCCA_XTAL_1P05 (Pin CP5) Note 1, 3	2.2uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47uF	1	Filter Capacitor 0603	X5R rating capacitor recommended
VCCAMPHYPLL_1P05 (Pin BV2) Note 1, 3	2.2uH	1	Series Inductor 0603	Rated at least 100 mA DCR = 0.33ohm +/- 30%
	47uF	1	Filter Capacitor 0603	X5R rating capacitor recommended

Document Number: 566439 Ver 2.0

<Core Design>

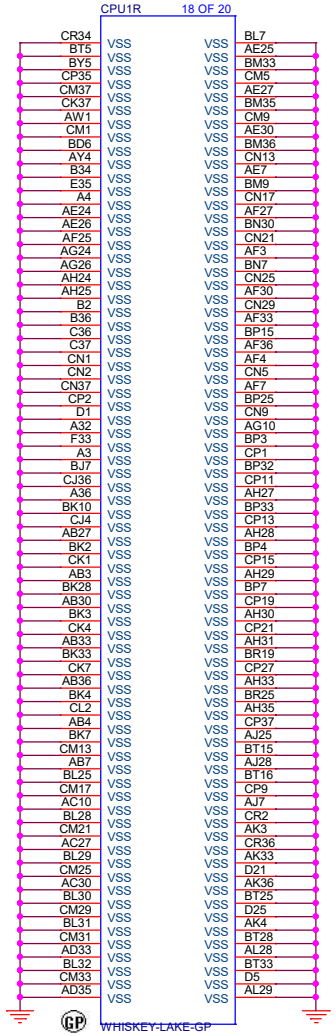
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCH-LP PWR&Caps)

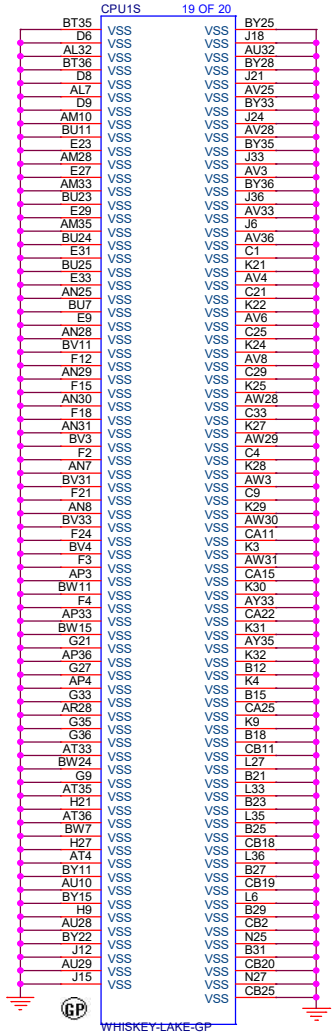
Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 22 of 106

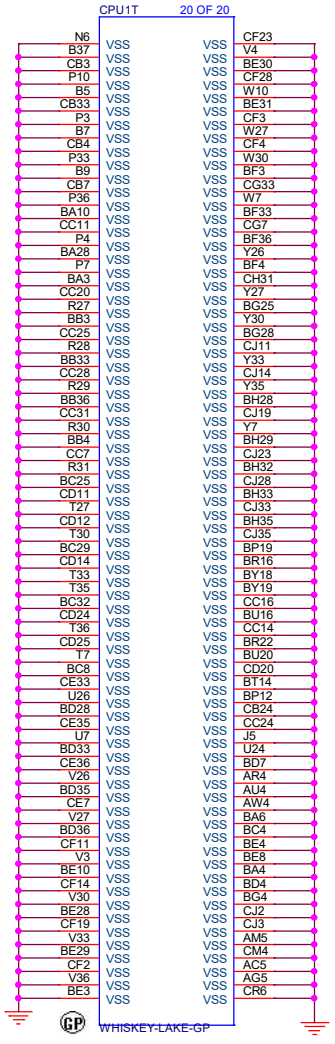
Main Func = PCH



ZZ.00CPU.271



ZZ.00CPU.271



ZZ.00CPU.271

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size	Document Number	Rev
A3	Woody_WL/Slinky_WL	-1m

Date: Friday, September 07, 2018 Sheet 23 of 106

SSID = KBC

Power

- 3D3V_AUX_S5
- 3D3V_S0
- 3D3V_RTC_AUX

Signal

- H_RCIN# 18
- FUN_OFF# 65,89
- LPC_FRAME#_CPU 18,68
- LPC_AD_CPU_P3 18,68
- LPC_AD_CPU_P2 18,68
- LPC_AD_CPU_P1 18,68
- LPC_AD_CPU_P0 18,68
- LPC_CLK_KBC 18
- PLT_RST# 17,63,68,89,91

- LID_CLOSE# 66
- LID_CLOSE2# 66
- PTP_PWR_EN 65
- PURE_HW_SHUTDOWN# 26,40
- PM_CLKRUN#_EC 18
- ES1_TXD 61,68
- SH_INT# 3

- EC_TP_IN# 24,65
- KBC_BEEP 27
- KB_BL_DET 65
- FAN1_PWM 26,89
- FAN_TACH1 26,89
- Value+ 66
- Value- 66

- KSI0 65,89
- KSI1 65,89
- KSI2 65,89
- KSI3 65,89
- KSI4 65,89
- KSI5 65,89
- KSI6 65,89
- KSI7 65,89
- KSO0 65,89
- KSO1 65,89
- KSO2 65,89
- KSO3 65,89
- KSO4 65,89
- KSO5 65,89
- KSO6 65,89
- KSO7 65,89
- KSO8 65,89
- KSO9 65,89
- KSO10 65,89
- KSO11 65,89
- KSO12 65,89
- KSO13 65,89
- KSO14 65,89
- KSO15 65,89
- KSO16 65,89
- KSO17 65,89

- AC_IN# 44,74
- DC_Protect_EC 44
- KBC_PWRBTN# 66,89
- BAT_IN# 43,44
- DC_IN_OK 44,72,74

- AD_IA 44
- BT_IA 44
- ALL_SYS_PWRGD 17,40
- MODEL_ID_AD 55

- STDBY_LED 66,89
- POWER_LED 66,89
- CHARGE_LED 66,89
- DC_BATFULL 66,89

- SML1_CLK 18,55,70,72
- SML1_DATA 18,55,70,72
- BAT_SCL 43,44
- BAT_SDA 43,44
- SPI_WP_ROM 15,18,25

- EC_TPCLK 65
- EC_TPDATA 65
- ME_UNLOCK 19
- EC_TP_IN# 24,65

- RTCRST_ON 18
- BLON_OUT 55
- AD_OFF 43
- VD_IN1 26
- VD_OUT1 26
- PROCHOT#_CPU 3,44,46
- RSMRST#_KBC 17
- AMP_MUTE# 27
- 5V_EN 40,45
- KB_BL_PWM 65
- TOUCH_EN 55
- 3V_5S_ENABLE 40

- AC_PRESENT 17
- eDP_BLEN_CPU 4
- PM_PWRBTN# 17
- PCIE_WAKE# 17,63

- INT_SERIRQ 18,68
- EC_SMI# 4
- EC_SCI# 4

3.3V

- PM_SLP_S3# 17,40,53,60
- PM_SLP_S4# 17,40,51

LPC BUS=>3.3V
SPI BUS=>3.3V/1.8V (VCC_IO2 PIN:124 OPTION)

Type_C

- PD_INT# 72

Charger

- USB_CHARGER_EN 36
- USB_CHAR_SEL 36
- USB_CHAR_CT1 36

- WIFI_RF_EN 61
- BLUETOOTH_EN 61,89
- USB_PWR_EN 35,66

- CHG_ON# 44
- PECI_EC 3

- TS_I2C0_SCL_CON 20,55
- TS_I2C0_SDA_CON 20,55
- SYS_PWROK 17

- SPI_SO_ROM 18,25,91
- SPI_SI_ROM 15,18,25,91
- SPI_CLK_ROM 18,25,91
- SPI_CS_CPU_N0 18,25

Close to the EC

VCC_LPC(Pin9)

For EC power consumption reserver

CPU/G-sensor/Type C --->
BATTER /CHARGER --->
CPU<---
Touch Pad--->

SYS_PWROK(S0_PWR_GOOD) ==DELAY 99ms

close RN2407

Woody 45W,Buzz UMA 65W Setting

GPIO0 High Active

Sensitive trace cap

PCB_VER_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
SA	100.0 K	10.0 K	3.000 V	3.005 V	>= 2.875 V	
SB	100.0 K	20.0 K	2.750 V	2.759 V	>= 2.616 V	< 2.875 V
SC	100.0 K	33.0 K	2.481 V	2.493 V	>= 2.363 V	< 2.616 V
-1	100.0 K	47.0 K	2.245 V	2.259 V	>= 2.123 V	< 2.363 V
-1M	100.0 K	64.9 K	2.001 V	2.017 V	>= 1.934 V	< 2.123 V
Reserved for project use	100.0 K	76.8 K	1.867 V	1.883 V	>= 1.758 V	< 1.934 V
Reserved for project use	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.504 V	< 1.758 V
Reserved for project use	100.0 K	143.0 K	1.358 V	1.374 V	>= 1.281 V	< 1.504 V
Reserved for project use	100.0 K	174.0 K	1.204 V	1.220 V	>= 1.126 V	< 1.281 V
Reserved for project use	100.0 K	215.0 K	1.048 V	1.062 V	>= 0.524 V	< 1.126 V

ADT_TYPE_AD	Pull-Low Register	Pull-High Register	Typical Voltage	Max Voltage	KBC Firmware Setting	
65W	NA	100.0 K	3.300 V		>= 3.000 V	
58W	100.0 K	NA	0.000 V			< 0.150 V
36W	10.0 K	100.0 K	0.300 V	0.308 V	>= 0.150 V	< 0.425 V
45W	20.0 K	100.0 K	0.550 V	0.559 V	>= 0.425 V	< 0.664 V
120W	33.0 K	100.0 K	0.819 V	0.831 V	>= 0.664 V	< 0.937 V
150W	47.0 K	100.0 K	1.055 V	1.070 V	>= 0.937 V	< 1.177 V
180W	64.9 K	100.0 K	1.299 V	1.315 V	>= 1.177 V	< 1.366 V
Reserved	76.8 K	100.0 K	1.433 V	1.450 V	>= 1.366 V	< 1.542 V
Reserved	100.0 K	100.0 K	1.650 V	1.667 V	>= 1.542 V	< 1.942 V

MODEL_ID_AD	Pull-Low Register	Pull-High Register	Typical Voltage
Woody 13"	/	10.0K	
Buzz UMA 15"	0K	/	
Slinky 14"	100.0K	64.9K	2.001V
Reserved for project use	100.0K	76.8K	1.867V
Reserved for project use	100.0K	100.0K	1.650V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

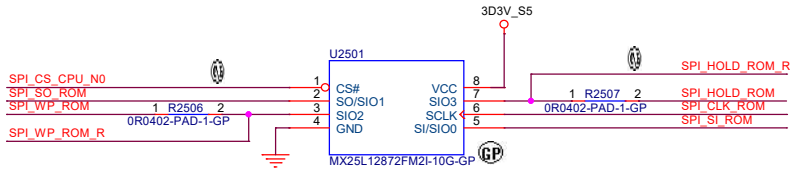
Title: KBC_KB9028
Size: B3/Bottom
Document Number: Woody_WL/Slinky_WL
Rev: 1m
Date: Friday, September 07, 2018
Sheet 24 of 106

18,24 SPI_CS_CPU_N0
18,24,91 SPI_SO_ROM
15,18 SPI_WP_ROM
15,18 SPI_HOLD_ROM
18,24,91 SPI_CLK_ROM
15,18,24,91 SPI_SI_ROM
20 RTC_DET#

Main Func = SPI Flash

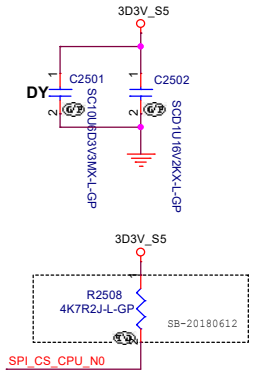
SPI FLASH ROM (16M byte) for PCH

SPI ROM Equal length need to less than 500mil

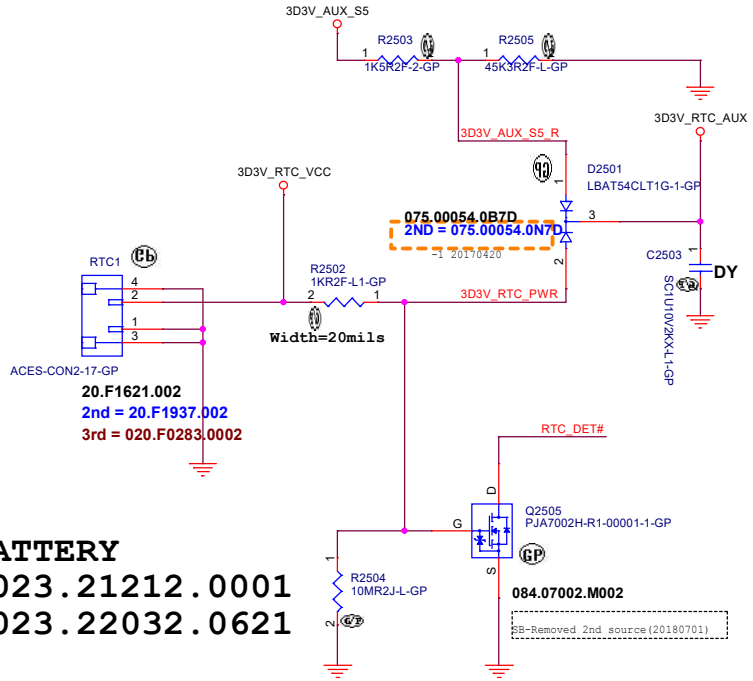


072.25128.0D61_MX25L12872FM2I-10G_MXIC
072.25128.0B51_W25Q128JVSIQ _WINBOND

SB-Removed U2502(20180702)



Main Func = RTC



RTC BATTERY
1st= 023.21212.0001
2nd= 023.22032.0621

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash(KBC+PCH)/RTC
Size: Custom
Document Number: Woody_WL/Slinky_WL
Rev: -1m
Date: Friday, September 07, 2018
Sheet 25 of 106

24 VD_IN1

24,26,89 FAN1_PWM

24,89 FAN_TACH1

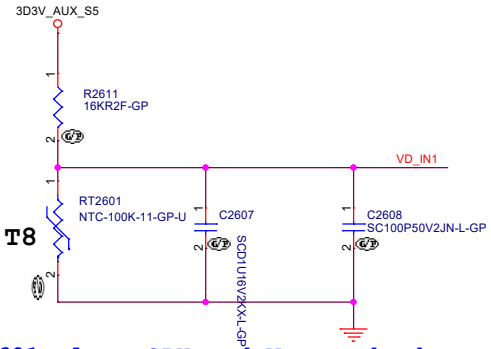
24,40 PURE_HW_SHUTDOWN#

24 VD_OUT1

40,46 PWR_IMVP_PWRGD

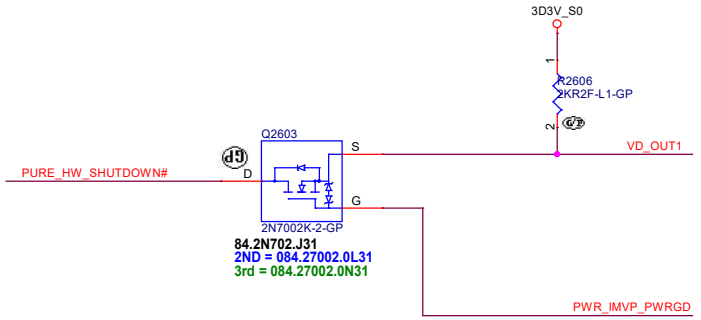
24,26,89 FAN1_PWM

SSID = Thermal

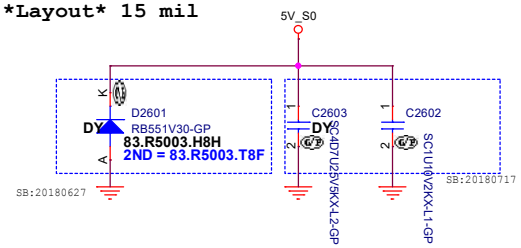


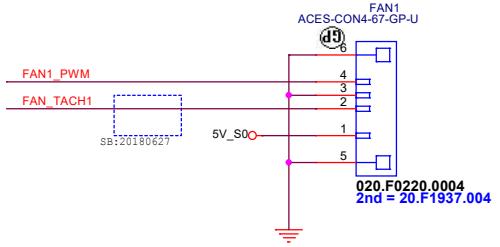
RT2601 close CPU and Vcore chock

VD_IN1 trace 10 mli



Layout 15 mil





<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal 7718/Fan Controllor P2793		
Size: Custom	Document Number: Woody_WL/Slinky_WL	Rev: -1m
Date: Friday, September 07, 2018	Sheet 26 of 106	

SSID = AUDIO

29,89 AUD_SPK1_R_L+
29,89 AUD_SPK1_R_L-
29,89 AUD_SPK1_R_R+
29,89 AUD_SPK1_R_R-

19 HDA_BITCLK_CODEC
19 HDA_SYNC_CODEC
19 HDA_SDIN0_CPU
19 HDA_SDOUT_CODEC

29 SML0_DATA_CPU
29 SML0_CLK_CPU
29 AMP_PD
24 KBC_BEEP
15,19 HDA_SPKR
24 AMP_MUTE#

29 DMIC2_DATA_CON
29 DMIC_CLK_CON
29 DMIC1_DATA_CON

66,89 AUD_HP1_JACK_L2
66,89 AUD_HP1_JACK_R2
66,89 AUD_HP1_JD#
66,89 RING2
66,89 SELEEVE

29 Smart_AMP_DOUT
29 Smart_AMP_DIN
29 Smart_AMP_BCLK
29 Smart_AMP_MCLK
29 Smart_AMP_LRCK

5V_S0 R2719 0R0603-PAD-1-GP-U Close to Pin40 5V_AVDD1
C2709 SCD1U16V2KX-L-GP C2708 SC10U6D3V3MX-GP AUD_AGND

1D8V_S0 R2739 0R0402-PAD 1D8V_AVDD2 Close to pin20
C2732 SCD1U16V2KX-L-GP C2733 SC10U6D3V3MX-GP AUD_AGND

3D3V_S0 R2737 0R0402-PAD-1-GP 3D3V_DVDD Close to pin3
C2726 SCD1U16V2KX-L-GP

3D3V_S0 R2736 0R0402-PAD 3D3V_DVDD_IO_U2701 Close to pin18
C2717 SCD1U16V2KX-L-GP DY C2716 SCD1U16V2KX-L-GP SB-20180717

5V_S0 R2738 0R0402-PAD-1-GP 5V_PVDD1 Close to Pin41
C2727 SCD1U16V2KX-L-GP C2728 SC10U6D3V3MX-GP
C2729 SCD1U16V2KX-L-GP DY C2730 SC10U6D3V3MX-GP SB-20180717 Close to Pin46

G2703 GAP-CLOSE G2701 GAP-CLOSE G2702 GAP-CLOSE AUD_AGND
AUD_AGND close to codec IC

C2725 AUDIO_PC_BEEP KBC_BEEP_C SCD1U16V2KX-L-GP
placed nearby codec PIN34
RN2701 SRN47K-2-GP-U KBC_BEEP HDA_SPKR
R2730 10KR2F-2-GP

U2701 ALC295-CG-GP 071.00295.0003

5V_AVDD1 1D8V_AVDD2 3D3V_DVDD 3D3V_DVDD_IO_U2701 5V_PVDD1 5V_STB 5VSTB/AUX_MODE
DVDD DVDD-IO PVDD1 PVDD2 AVDD1 CPVDD/AVDD2 DMIC-CLK-IN/I2S-EN/SPDIF-OUT/GPIO2/DMIC-DATA34
5V_S5 R2757 0R0402-PAD-1-GP

HDA_SDIN0_CPU R2718 33R2J-2-GP
HDA_BITCLK_CODEC HDA_SYNC_CODEC HDA_SDIN0_CODEC HDA_SDOUT_CODEC
AUDIOLINK_BCLK AUDIOLINK_SYNC AUDIOLINK_SDATA-IN AUDIOLINK_SDATA-OUT
SML0_DATA_CPU SML0_CLK_CPU Smart_AMP_DOUT_R Smart_AMP_DIN_R Smart_AMP_BCLK_R Smart_AMP_MCLK_R Smart_AMP_LRCK_R
I2C-DATA I2C-CLK I2S-IN I2S-OUT I2S-BCLK I2S-MCLK I2S-LRCK
LDO1_CAP LDO2_CAP LDO3_CAP LDO1-CAP LDO2-CAP LDO3-CAP

AMP_MUTE# R2731 0R0402-PAD-1-GP
P25_CPVEE AMP_PD AUDIO_PC_BEEP EAPD# VREF CPVEE DC-DET/EAPD PCBEEP PDB VREF

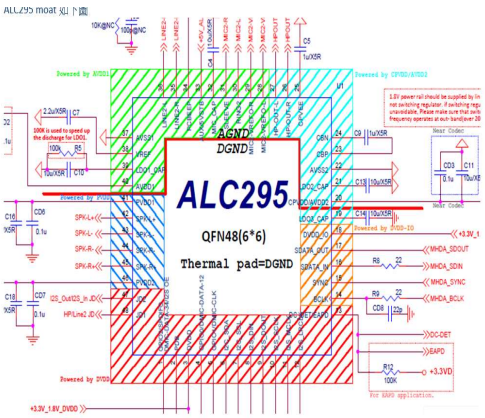
GPIO0/DMIC-DATA12 GPIO1/DMIC-CLK DMIC2_DATA_CON DMIC_CLK_CON DMIC1_DATA_CON
HPOUT-L/PORT-I-L HPOUT-R/PORT-I-R AUD_HP1_JACK_L2 AUD_HP1_JACK_R2
LINE1-L/PORT-C-L LINE1-R/PORT-C-R LINE1_L LINE1_R
C2723 C2724 SC4D7U6D3V3KX-L-GP SC4D7U6D3V3KX-L-GP SRN2K2J-5-GP AUD_HP1_JACK_L2 AUD_HP1_JACK_R2
MIC2-VREFO-L MIC2-VREFO-R MIC2-VREFO-L MIC2-VREFO-R
MIC2-L/PORT-F-L/RING2 MIC2-R/PORT-F-R/SLEEVE RING2 SELEEVE
MIC2-CAP MIC2_CAP
SPK-OUT-L+ SPK-OUT-L- SPK-OUT-R+ SPK-OUT-R- AUD_SPK1_R_L+ AUD_SPK1_R_L- AUD_SPK1_R_R+ AUD_SPK1_R_R-
HP/LINE1-JD/JD1 I2S-IN/I2S-OUT-JD/JD2 AUD_SENSE_A I2S_IN_OUT
R2702 100KR2F-L1-GP 3D3V_DVDD
R2713 200KR2F-L-3-GP R2701 100KR2F-L1-GP DY AUD_HP1_JD# 3D3V_DVDD
CBN CBP C2703 SC2D2U10V3KX-L-GP
AVSS1 AVSS2 GND AUD_AGND

R2727 is need to connect.To prvent the beep sound

LDO1_CAP R2711 10KR2F-L1-GP C2702 SC10U6D3V3MX-L-GP AUD_AGND
LDO3_CAP C2718 SC10U6D3V3MX-L-GP
HDA_BITCLK_CODEC DY C2701 SC220P50V2JN-L-GP
LDO2_CAP C2712 SC10U6D3V3MX-L-GP AUD_AGND
P25_CPVEE C2710 SC1U10V2KX-L1-GP SB-20180724 AUD_AGND
VREF C2731 SC2D2U10V3KX-L-GP AUD_AGND
MIC2_CAP C2713 SC10U6D3V3MX-L-GP AUD_AGND

Smart_AMP_DOUT Smart_AMP_DIN Smart_AMP_BCLK Smart_AMP_MCLK Smart_AMP_LRCK
R2756 R2755 R2754 R2753 R2752 33R2J-2-GP
Smart_AMP_DOUT_R Smart_AMP_DIN_R Smart_AMP_BCLK_R Smart_AMP_MCLK_R Smart_AMP_LRCK_R
AMP C2753 C2752 C2751 C2750 C2754 SC220P50V2JN-L-GP

Closed U2701



AUD_HP1_JACK_L2 AUD_HP1_JACK_R2 ED2703 AZ5125-02S-R7G-GP 75.05125.07D 2nd = 075.05125.007D DY 75.05125.07D
SELEEVE RING2 ED2701 AZ5125-02S-R7G-GP 75.05125.07D 2nd = 075.05125.007D DY 75.05125.07D

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC295
Size: Custom Document Number: Woody_WL/Slinky_WL Rev: -1m
Date: Friday, September 07, 2018 Sheet 27 of 106

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<Core Design>

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Title	***Reserved***	
Size A4	Document Number **Woody_WL/Slinky_WL**	Rev -1m
Date: Friday, September 07, 2018	Sheet 28 of 106	

Amplifiers

27 SML0_CLK_CPU
27 SML0_DATA_CPU
27 Smart_AMP_MCLK
27 Smart_AMP_BCLK
27 Smart_AMP_LRCK
27 Smart_AMP_DIN
27 Smart_AMP_DOUT
27 AMP_PD
27,89 AUD_SPK1_R_L-
27,89 AUD_SPK1_R_L+
27,89 AUD_SPK1_R_R-
27,89 AUD_SPK1_R_R+
89 OUT_RN_CON
89 OUT_RP
89 SPK_RINRVP

CCD

16 CCD_USB20_P
16 CCD_USB20_N
89 CCD_USB20_CON_P
89 CCD_USB20_CON_N

DMIC

27 DMIC_CLK_CON
27 DMIC1_DATA_CON
27 DMIC2_DATA_CON
89 DMIC_CLK_CON_C
89 DMIC1_DATA_CON_C
89 DMIC2_DATA_CON_C

SSID = AUDIO

SML0_CLK_CPU R2917.1 2 0R0402-PAD AMP_SCL
SML0_DATA_CPU R2918.1 2 0R0402-PAD AMP_SDA
Smart_AMP_MCLK R2916.1 2 0R0402-PAD AMP_MCLK
Smart_AMP_BCLK R2915.1 2 0R0402-PAD AMP_BCLK
Smart_AMP_LRCK R2914.1 2 0R0402-PAD AMP_LRCK
Smart_AMP_DIN R2913.1 2 0R0402-PAD AMP_DACDAT
Smart_AMP_DOUT 1 R2940 2 0R0402-PAD

AMP_PD
3D3V_DVDD_IO
1D8V_AMP_VDD
1D8V_AMP_AVDD2
3D3V_AUDIO_AMP_ASEL
LDO_A1_5_R
AMP_VREF

U2905
ALC1006-VB-CGT-GP
AMP
074.01006.0A13

SPK_RIP R2928.1 2 0R0402-PAD
SPK_RINRVP R2927.1 2 0R0402-PAD
SPK_RVN R2926.1 2 0R0402-PAD

-SB 20170314 EMC SUGGEST
Main source:68.00230.041
Second source:68.00206.021
change main source 20170330

ER2914 1 HCB1608KF121T30-GP
ER2915 1 HCB1608KF121T30-GP
ER2916 1 HCB1608KF121T30-GP
ER2917 1 HCB1608KF121T30-GP

Trace width=40mil

Speaker 20170314 SB Change
SPK1
HR-CON5-6-GP
020.F000M.0006
2nd = 020.F1038.0006
Need change 20170405
Main:020.F000M.0006
2nd:020.F1038.0006
PIN5: SUBWOOFER -
PIN6: SUBWOOFER +

Figure 30. Application Diagram With Speaker Protection

Wait Check
ED2901 AZ5125-02S-R7G-GP
ED2902 AZ5125-02S-R7G-GP
ED2903 AZ5125-02S-R7G-GP
75.05125.07D
2nd = 075.05125.007D
75.05125.07D

3D3V_S0 R2934 2 0R0402-PAD 3D3V_DVDD_IO
1D8V_S0 R2935 2 0R0402-PAD 1D8V_AMP_VDD
1D8V_AMP_VDD R2936 2 0R0402-PAD 1D8V_AMP_AVDD2
5V_S0 R2937 2 0R0402-PAD 5V_SPK_VDD
R2938 20KR2F-L3-GP DY

MICBD1
ACES-CON14-9-GP
20.F1633.014
2nd = 20.F1261.014
3D3V_CAMERA_S0
CCD_USB20_CON_N
CCD_USB20_CON_P
DMIC2_DATA_CON_C ER2957 1 33R2J-L1-GP DMIC2_DATA_CON
DMIC_CLK_CON_C ER2955 1 BLM15AG121SN1D DMIC_CLK_CON
68.00084.921
2nd = 68.00217.401
-1 20170505 EMC SUGGEST
DMIC1_DATA_CON_C ER2956 1 33R2J-L1-GP DMIC1_DATA_CON

A. Pin define

Note

CCD Module

MB Connecter		CCD connector pin	MIC-R PCB	MIC-L PCB
Pin 1	3D3V_CAMERA_S0	1		
Pin 2	3D3V_CAMERA_S0		1	
Pin 3	3D3V_CAMERA_S0			1
Pin 4	CCD_USB20_CON_N	2		
Pin 5	CCD_USB20_CON_P	3		
Pin 6	GND	4		
Pin 7	DMIC2_DATA_CON	6		
Pin 8	DMIC_CLK_CON	5		
Pin 9	DMIC_CLK_CON		3	
Pin 10	DMIC_CLK_CON			3
Pin 11	GND		4	
Pin 12	DMIC1_DATA_CON		2	
Pin 13	DMIC1_DATA_CON			2
Pin 14	GND			4

MB Connecter — CCD Connecter

Camera Power
3D3V_S0 F2901 POLYSW-1D1A6V-9-GP-U
69.48001.081
2nd = 69.50011.081
3D3V_CAMERA_S0 C2958 C2959 SC1U16V3KX-GP

EU2905 AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

EL2901 DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0001

EC2963 EC2961 EC2962 SC220P50V2JH-L-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/AMP/DMIC
Size: Custom
Document Number: Woody_WL/Slinky_WL
Rev: -1m
Date: Friday, September 07, 2018
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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
Date: Friday, September 07, 2018	Sheet 30 of 106	

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Woody_WL/Slinky_WL	-1m

Date: Friday, September 07, 2018 Sheet 31 of 106

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Woody_WL/Slinky_WL	-1m

Date: Friday, September 07, 2018 Sheet 32 of 106

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
Date: Friday, September 07, 2018	Sheet 33 of 106	

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

Size	Document Number	Rev
A4	Woody_WL/Slinky_WL	-1m

Date: Friday, September 07, 2018 Sheet 34 of 106

USB1

16 USB1_USB20_N
16 USB1_USB20_P

16 USB1_USB30_RX_N
16 USB1_USB30_RX_P

16 USB1_USB30_TX_N
16 USB1_USB30_TX_P

89 USB1_CON_USB20_N
89 USB1_CON_USB20_P

USB2

36 Charger_USB20_N
36 Charger_USB20_P

16 USB2_USB30_RX_N
16 USB2_USB30_RX_P

16 USB2_USB30_TX_N
16 USB2_USB30_TX_P

89 USB2_CON_USB20_N
89 USB2_CON_USB20_P

USB Power enable

24,66 USB_PWR_EN

High Active 2A

5V_S5 — C3501 SC1U10V2KX-L1-GP (DY) SB:20180717 — USB_PWR_EN — U3501 IN/EN/OUT/GND/OC# — G517F1T12U-GP
074.51712.009F
2nd = 074.22811.009F

5V_USB30 — DR3F-1-GP-U 1 — R3501 — 5V_USB30_CHARGER
NON USB CHARGE

C3502 SCD1U16V2KX-L-GP (DY) SB:20180717

5V_USB30 — C3504 SC100U6D3V6MX-GP
5V_USB30_CHARGER — C3516 SC100U6D3V6MX-GP

USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

EU3501 — L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

USB1_USB30_TX_N — SCD1U16V2KX-L-GP — C3508
USB1_USB30_TX_P — SCD1U16V2KX-L-GP — C3509

USB1
5V_USB30
USB1_CON_USB20_N / USB1_CON_USB20_P
USB1_USB30_RX_N / USB1_USB30_RX_P
USB1_USB30_TX_CON_N / USB1_USB30_TX_CON_P
VBUS, D-, D+, GND-DRAIN, CHASSIS#12, CHASSIS#13, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+, GND
USB3.0
SKT-USB13-347-GP
022.10005.08Q1

EL3501 — DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0001

EU3503 — AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

EU3502 — L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073

USB2_USB30_TX_N — SCD1U16V2KX-L-GP — C3510
USB2_USB30_TX_P — SCD1U16V2KX-L-GP — C3511

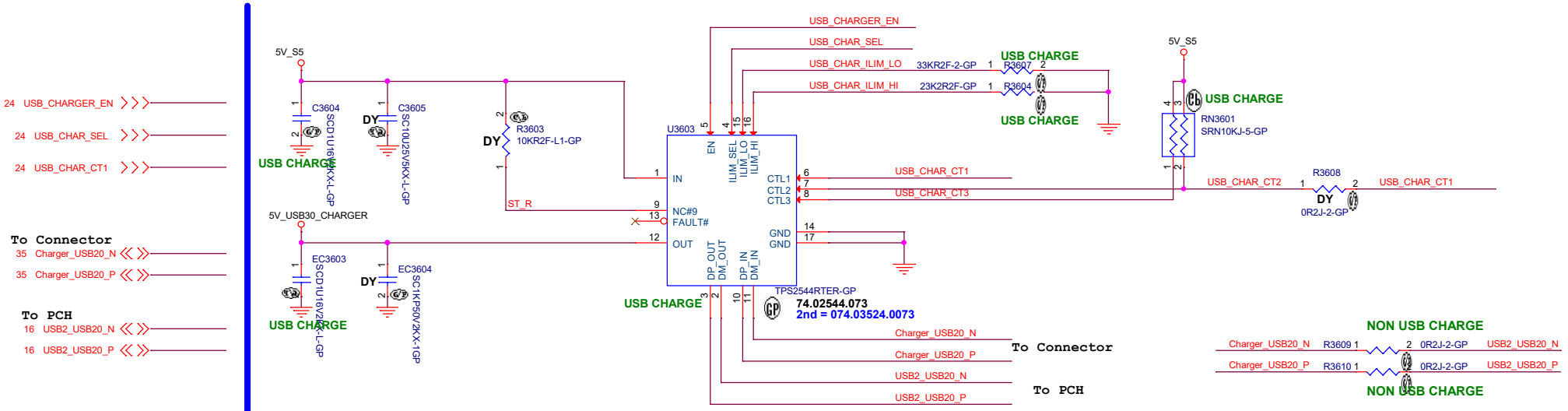
5V_USB30_CHARGER
USB2
USB2_CON_USB20_N / USB2_CON_USB20_P
USB2_USB30_RX_N / USB2_USB30_RX_P
USB2_USB30_TX_CON_N / USB2_USB30_TX_CON_P
VBUS, D-, D+, GND-DRAIN, CHASSIS#12, CHASSIS#13, STDA_SSRX-, STDA_SSRX+, STDA_SSTX-, STDA_SSTX+, GND
USB3.0
SKT-USB13-347-GP
022.10005.08Q1

EL3502 — DLM0NSN900HY2D-GP
068.09002.2001
2nd = 68.02002.061
3rd = 068.00104.0001

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0**
Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m
Date: Friday, September 07, 2018 | Sheet 35 of 106



CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	Comment
0	0	0	0	Discharge	NA	OUT held low
0	0	0	1	Discharge	NA	
0	0	1	0	DCP_Auto	ILIM_HI	Data Lines Disconnected
0	1	1	X			
0	1	0	0	SDP1	ILIM_LO	Data Lines connected
0	1	0	1		ILIM_HI	
1	0	0	0	DCP Forced Shorted	ILIM_LO	Device Forced to stay in DCP BC 1.2 charging mode
1	0	0	1		ILIM_HI	
1	0	1	0	DCP / Divider1	ILIM_LO	Device Forced to stay in DCP Divider 1 Charging Mode
1	0	1	1		ILIM_HI	
1	1	0	0	SDP1	ILIM_LO	Data Lines Connected
1	1	0	1	SDP1	ILIM_HI	
1	1	1	0	SDP2 (1)	ILIM_LO	
1	1	1	1	CDP (1)	ILIM_HI	Data Lines Connected

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB CHARGER

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

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<Core Design>

緯創資通 **Wistron Corporation**
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Title ***Reserved***

Size	Document Number	Rev
A4	Woody_WL/Slinky_WL	-1m

Date: Friday, September 07, 2018 Sheet 37 of 106

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<Core Design>

緯創資通 **Wistron Corporation**
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Title: ***Reserved***

Size	Document Number	Rev
A4	Woody_WL/Slinky_WL	-1m

Date: Friday, September 07, 2018 Sheet 38 of 106

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Title: ***Reserved***		
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
Date: Friday, September 07, 2018	Sheet 39 of 106	

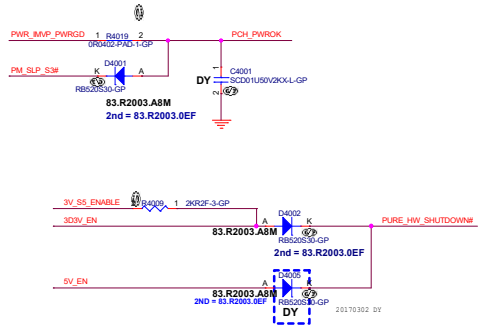
Power Sequence

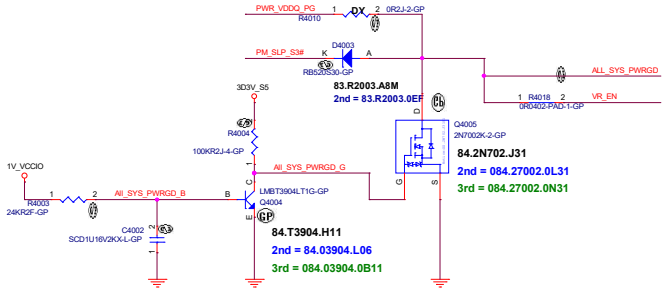
26,46 PWR_IMVP_PWRGD
17 PCH_PWROK
17,24,40,53,60 PM_SLP_S3#
24 3V_S5_ENABLE
45 3D3V_EN
24,45 5V_EN
24,26 PURE_HW_SHUTDOWN#
17,24 ALL_SYS_PWRGD
46 VR_EN
51 PWR_VDDQ_PG

Run Power

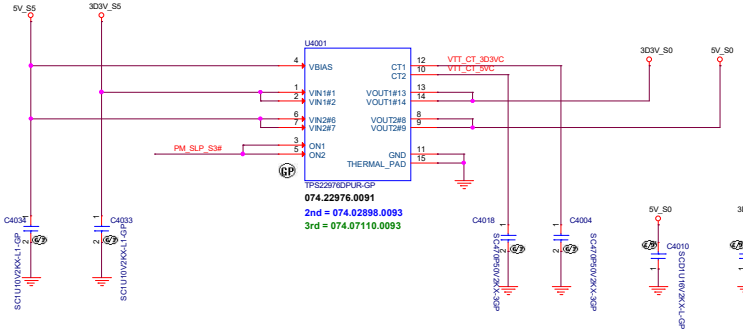
17,24,51 PM_SLP_S4#
17,24,40,53,60 PM_SLP_S3#

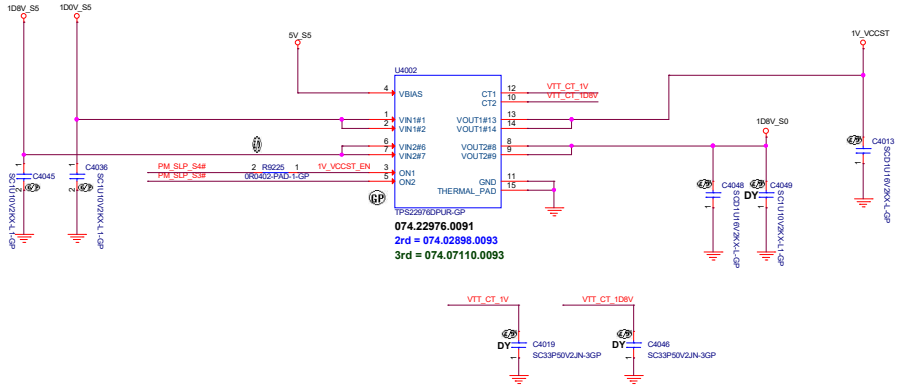
Power Sequence

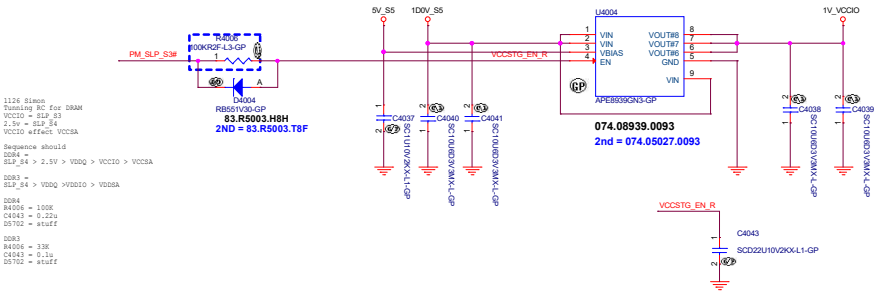




ANNIE Run Power







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable & SEQUENCE

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

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Blanking

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
Date: Friday, September 07, 2018	Sheet 41 of 106	

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Woody_WL/Slinky_WL	-1m

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24 AD_OFF

24,44 BAT_IN#

24,44 BAT_SCL
24,44 BAT_SDA

89 BAT_G

89 BAT_IN#_1

89 BATA_SCL_1

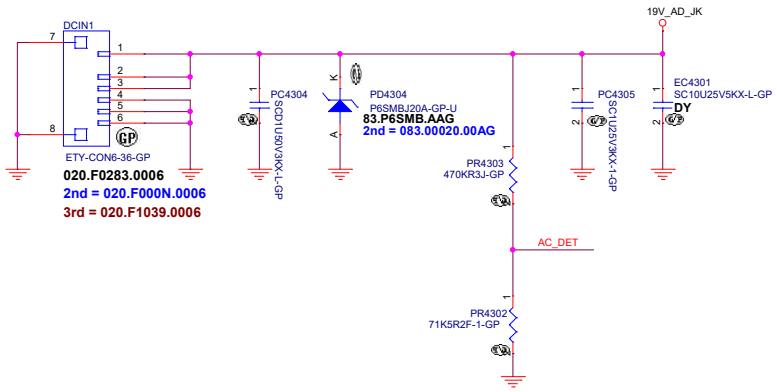
89 BATA_SDA_1

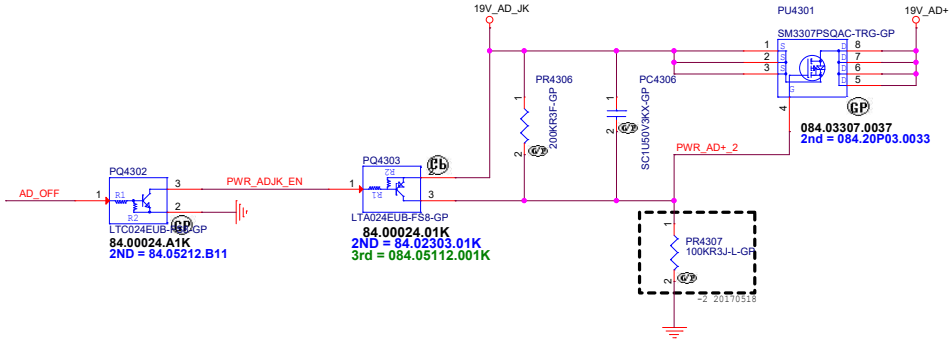
66 BAT_RST

74 AC_DET

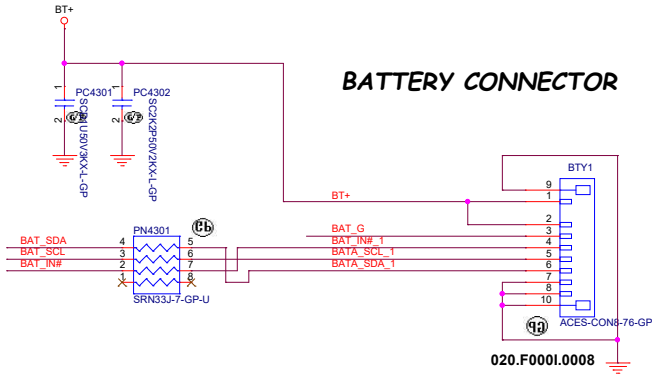
ANNIE solution

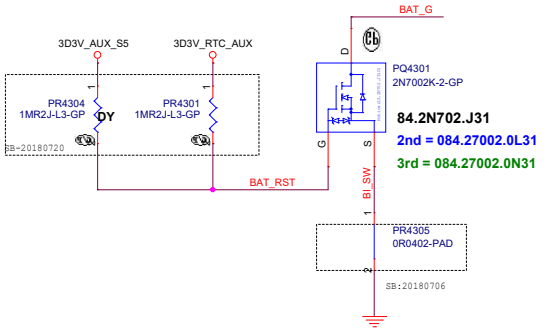
Adaptor in to generate DCBATOUT





BATTERY CONNECTOR

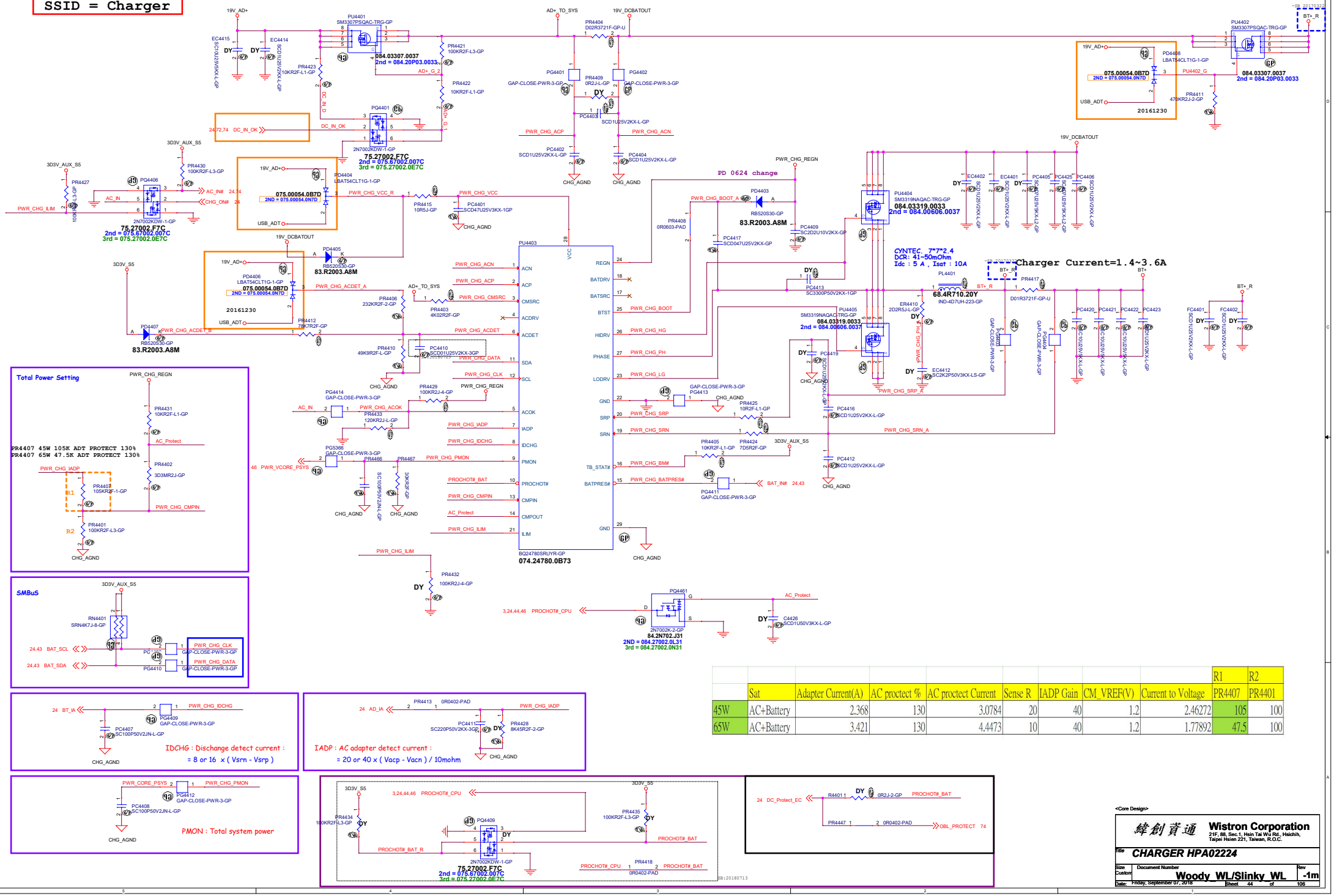




<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BATT CONN
Size: Custom	Document Number: Woody_WL/Slinky_WL
Rev	-1m
Date: Friday, September 07, 2018	Sheet 43 of 106

SSID = Charger



									R1	R2
	Sat	Adapter Current(A)	AC proctect %	AC proctect Current	Sense R	IADP Gain	CM_VREF(V)	Current to Voltage	PR4407	PR4401
45W	AC+Battery	2.368	130	3.0784	20	40	1.2	2.46272	105	100
65W	AC+Battery	3.421	130	4.4473	10	40	1.2	1.77892	47.5	100

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER HPA02224

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

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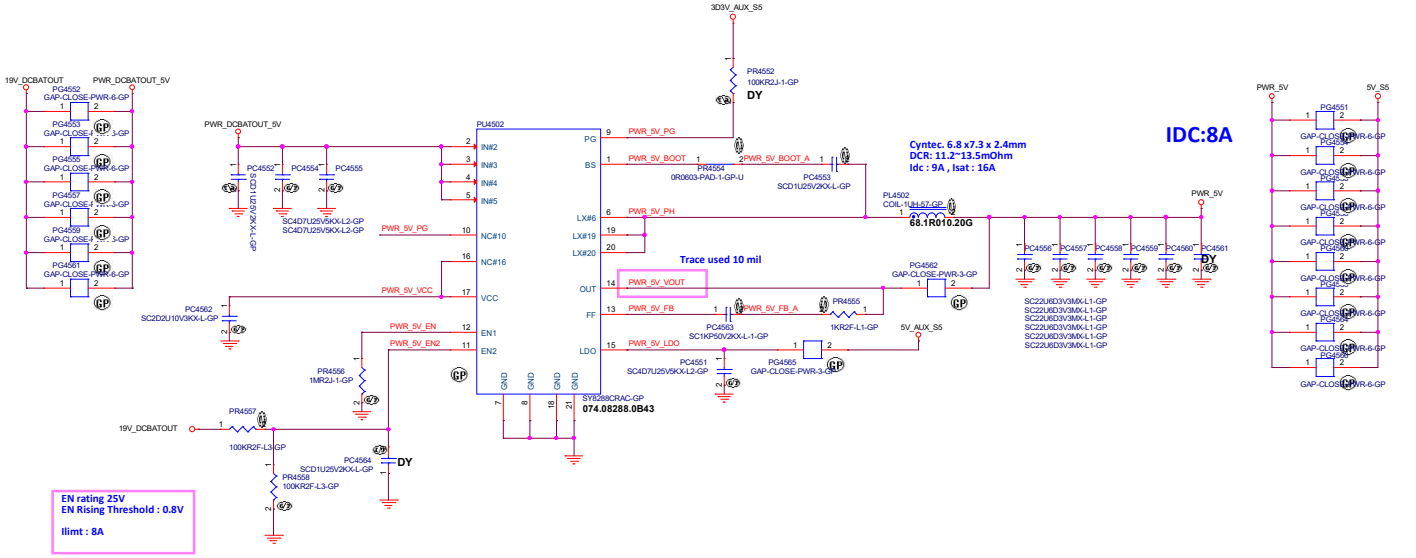
OFFPAGE

24,40 5V_EN — PR4560 — PWR_5V_EN

0R0402-PAD-1-GP

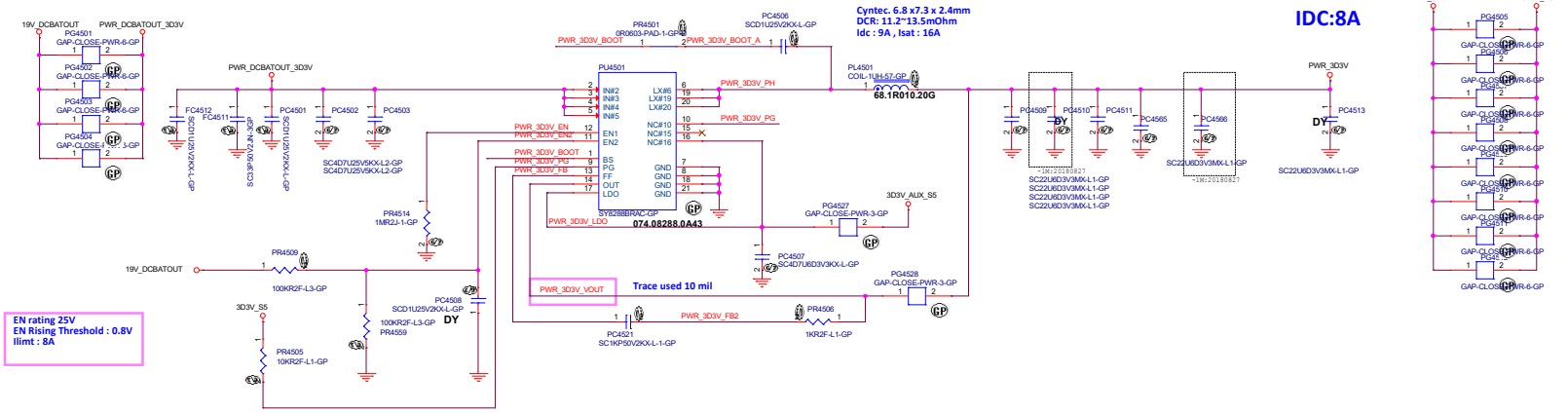


OFFPAGE

40 3D3V_EN — PR4561 — PWR_3D3V_EN

0R0402-PAD-1-GP

53,72 PWR_3D3V_PG — PWR_3D3V_PG



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power (6258C&6256B_5V/3D3V)

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Main Func = CPU_CORE

OFFPAGE

PH on CPU side

- 3,24,44 PROCHOT#_CPU — PR4696 0R0402-PAD-1-GP — PWR_CPU_PROCHOT#
- 7 PWR_VCORE_ALERT# — PWR_VCORE_ALERT#
- 7 VIDSCK_CPU_R — VIDSCK_CPU_R
- 7 VIDSOUT_CPU_R — VIDSOUT_CPU_R

PH on EE side

- 26,40 PWR_IMVP_PWRGD — PWR_IMVP_PWRGD
- 40 VR_EN — PR4689 0R0402-PAD-1-GP — PWR_VR_EN
- VSSCORE_SENSE
- 7 VCORE_RTN — PR4691 0R0402-PAD-1-GP — PWR_VCORE_RTN
- 7 VCORE_VSEN — PR4690 0R0402-PAD-1-GP — PWR_VCORE_VSEN
- VCCCORE_SENSE
- VCCGT_SENSE
- 8 VCCGT_VSEN — PR4692 0R0402-PAD-1-GP — PWR_VCCGT_VSEN
- 8 VCCGT_RTN — PR4693 0R0402-PAD-1-GP — PWR_VCCGT_RTN
- VSSGT_SENSE
- VSSSA_SENSE
- 8 VCCSA_RTN — PR4695 0R0402-PAD-1-GP — PWR_VCCSA_RTN
- 8 VCCSA_FB2 — PR4694 0R0402-PAD-1-GP — PWR_VCCSA_FB2
- VCCSA_SENSE
- 44 PWR_VCORE_PSYS — PWR_VCORE_PSYS

EE side Link

SVID Pull High V

1V_VCCST — PG4601 GAP-CLOSE-PWR-3-GP — PWR_CORE_VCCST

PWR_CORE_VCCST — PC4602 SCD1U25V2KX-L-GP — DY — PR4611 0R0402-PAD-1-GP — PR4610 0R0402-PAD-1-GP — PC4603 SC4D7U6D3V3KX-L-GP — PC4604 SCD47U25V3KX-1GP — PC4605 SCD1U25V2KX-L-GP — VIDSOUT_CPU_R, PWR_VCORE_ALERT#, VIDSCK_CPU_R

PWR_CORE_VCCST — PR4619 1KR2F-3-GP — DY — PR4601 100R2F-L3-GP — PWR_CPU_PROCHOT# — PWR_VCORE_VRHOT#

PWR_VREF

PR4604 4K22R2F-GP — PWR_VCORE_SET1
PR4605 9K53R2F-GP — PWR_VCORE_SET2
PR4606 35K7R2F-GP — PWR_VCORE_SET3
PR4613 226R2F-GP — PWR_VCORE_SET1_A
PR4614 0R0402-PAD-1-GP — PWR_VCORE_SET2_A
PR4615 392R2F-GP — PWR_VCORE_SET3_A
PR4620 4K22R2F-GP — PWR_VCORE_SET1_B
PR4621 9K1R2F-1-GP — PWR_VCORE_SET2_B
PR4622 18K2R2F-L-GP — PWR_VCORE_SET3_B
PR4629 95D3R2F-GP — PWR_CORE_SET1_B
PR4630 143R2F-1-GP — PWR_CORE_SET2_B
PR4626 130R2F-1-GP — PWR_CORE_SET3_B

PWR_VREF — PR4624 40K2R2F-GP — PR4628 2D2R3F-L-GP — PC4606 SCD22U25V3KX-GP — PC4608 SCD1U25V2KX-2-GP — DY — 19V_DCBATOUT

5V_S5 — PR4618 8D2R3F-GP — PC4603 SC4D7U6D3V3KX-L-GP

PC4688 SCD1U25V2KX-L-GP — DY — PR4688 10K2F-L1-GP — PWR_VCORE_PSYS

PWR_VREF — PR4633 40K2R2F-GP — PC4610 SC1KP50V2JN-2GP — DY — 3D3V_S0 — PR4636 10K2F-L1-GP — PR4638 49D9R2F-L1-GP — PR4639 10R2F-L1-GP — VIDSCK_CPU_R, VIDSOUT_CPU_R

PWR_VREF — PR4640 33KR2F-GP — PWR_VCORE_IMON_A — PR4641 5K76R2F-2-GP — PC4612 SC1KP50V2JN-2GP — DY — PR4678 NTC-100K-12-GP-U — B = 4250 — PR4642 47K5R2F-GP — PWR_VCORE_IMON_B

PR4604 4K22R2F-GP — PR4605 9K53R2F-GP — PR4606 35K7R2F-GP — PR4613 226R2F-GP — PR4614 0R0402-PAD-1-GP — PR4615 392R2F-GP — PR4620 4K22R2F-GP — PR4621 9K1R2F-1-GP — PR4622 18K2R2F-L-GP — PR4629 95D3R2F-GP — PR4630 143R2F-1-GP — PR4626 130R2F-1-GP

PWR_VCORE_VSEN — PR4648 10KR2F-L1-GP — PWR_VCCGT_COMP_B — PR4649 0R0402-PAD-1-GP — PR4650 29K4R2F-GP — PWR_VCCGT_COMP_A — PR4651 0R0402-PAD-1-GP — PC4616 SC220P50V2KX-3GP — PC4617 SC68P50V2JN-1GP — PC4618 SC1KP50V2JN-2GP — PWR_VCCGT_FB_A — PR4653 0R2F-1-GP — DY

5V_S5 — PR4645 0R0402-PAD-1-GP — PWR_VCORE_DRVEN_SET

PWR_VCORE_VSEN — PR4657 10KR2F-L1-GP — PWR_VCORE_COMP_B — PR4658 0R0402-PAD-1-GP — PR4659 63K4R2F-2-GP — PWR_VCORE_COMP_A — PR4660 0R0402-PAD-1-GP — PC4619 SC330P50V2KX-3GP — PR4683 0R0402-PAD-1-GP — PC4620 SC68P50V2JN-1GP — PC4621 SC1KP50V2JN-2GP — DY — PWR_VCORE_FB_A — 0R2F-1-GP — DY

PWR_VCCSA_FB2 — PR4666 10KR2F-L1-GP — PWR_VCCSA_COMP_B — PR4667 0R0402-PAD-1-GP — PR4668 71K5R2F-1-GP — PWR_VCCSA_COMP_A — PR4669 0R0402-PAD-1-GP — PC4622 SC470P50V2KX-3GP — PC4623 SC68P50V2JN-1GP — PC4624 SC1KP50V2JN-2GP — DY — PWR_VCCSA_FB_A — PR4673 0R2F-1-GP — DY

PU4601 RT3602AJGQW-GP 074.03602.0A73

PSYS	46
VCC	13
SET1	2
SET2	5
SET3	6
VIN	12
VREF06/PSET	42
IMON_AUXI	30
IMON_MAIN	1
IMON_SA	39
VR_READY	38
VR_HOT#	31
VCLK	34
VDIO	32
ALERT#	33
EN	37
VSEN_AUXI	27
COMP_AUXI	26
FB_AUXI	24
RGND_AUXI	25
DRVEN_SET	18
COMP_MAIN	4
FB_MAIN	3
RGND_MAIN	48
VSEN_MAIN	47
COMP_SA	43
FB_SA	45
RGND_SA	44
NC#14	14
NC#15	15
NC#19	19
NC#20	20
NC#21	21
PWM_SA	36
ISENP_SA	40
ISENN_SA	41
PWM_AUXI	22
ISENP_AUXI	29
ISENN_AUXI	28
PWM2_MAIN	16
ISEN1P_MAIN	10
ISEN1N_MAIN	7
PWM1_MAIN	17
ISEN2P_MAIN	9
ISEN2N_MAIN	8
DRVEN	35
TSEN_AUXI	23
TSEN_MAIN	11
GND	49

PWR_VCCSA_PWM 50 — PWR_VCCSA_ISUMP 50 — PWR_VCCSA_ISUMN 50 — PC4801 SC1KP50V2JN-2GP — PC4805 SCD1U25V2KX-L-GP — DY

PWR_VCCGT_PWM 48 — PWR_VCCGT_ISUMP 48 — PWR_VCCGT_ISUMN 48 — PC4807 SC1KP50V2JN-2GP — PC4809 SCD1U25V2KX-L-GP — DY

PWR_VCORE_PWMB 47 — PWR_VCORE_ISUMP_A 47 — PWR_VCORE_ISUMN_A 47 — PR4683 1R2F-GP — PC4611 SC1KP50V2JN-2GP — PC4613 SCD1U25V2KX-L-GP — DY

PWR_VCORE_PWMA 47 — PWR_VCORE_ISUMP_B 47 — PWR_VCORE_ISUMN_B 47 — PR4682 0R2F-1-GP — PR4684 1R2F-1-GP — PR4652 10R2F-1-GP — DY — 5V_S5

PWR_VCORE_FCCM# 47,48,50 — PC4615 SCD1U25V2KX-L-GP

	PR4652	PR4682	PR4684
U22	0	0	DY
U42	DY	DY	1R

PWR_VCCGT_TSEN — PWR_VCORE_TSEN

PR4676 NTC-100K-12-GP-U — B = 4250 — PR4664 10KR2F-L-GP — PWR_VCCGT_TSEN_A

PR4681 NTC-100K-12-GP-U — B = 4250 — PR4677 10KR2F-L-GP — PWR_VCORE_TSEN_A

PWR_VREF

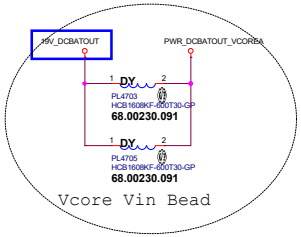
PR4654 12KR2F-L-GP — PR4655 15K8R2F-GP — PWR_VCCGT_TSEN_B — PWR_VCORE_TSEN_B
PR4661 845R2F-GP — PR4662 174R2F-GP
PR4670 22K6R2F-1-GP — PR4671 16K9R2F-GP — PWR_VCCGT_TSEN_C — PWR_VCORE_TSEN_C
PR4674 432R2F-GP — PR4675 143R2F-1-GP

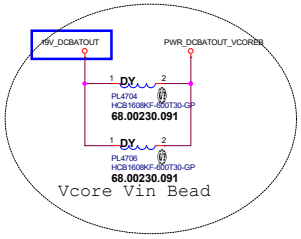
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

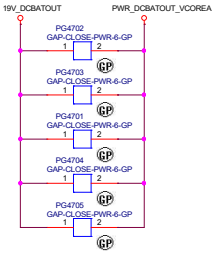
Title: POWER (RT3602AJ_VCORE(1/3))
Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m
Date: Friday, September 07, 2018 | Sheet 46 of 106

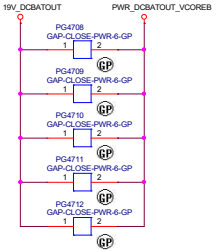
Main Func = CPU_CORE

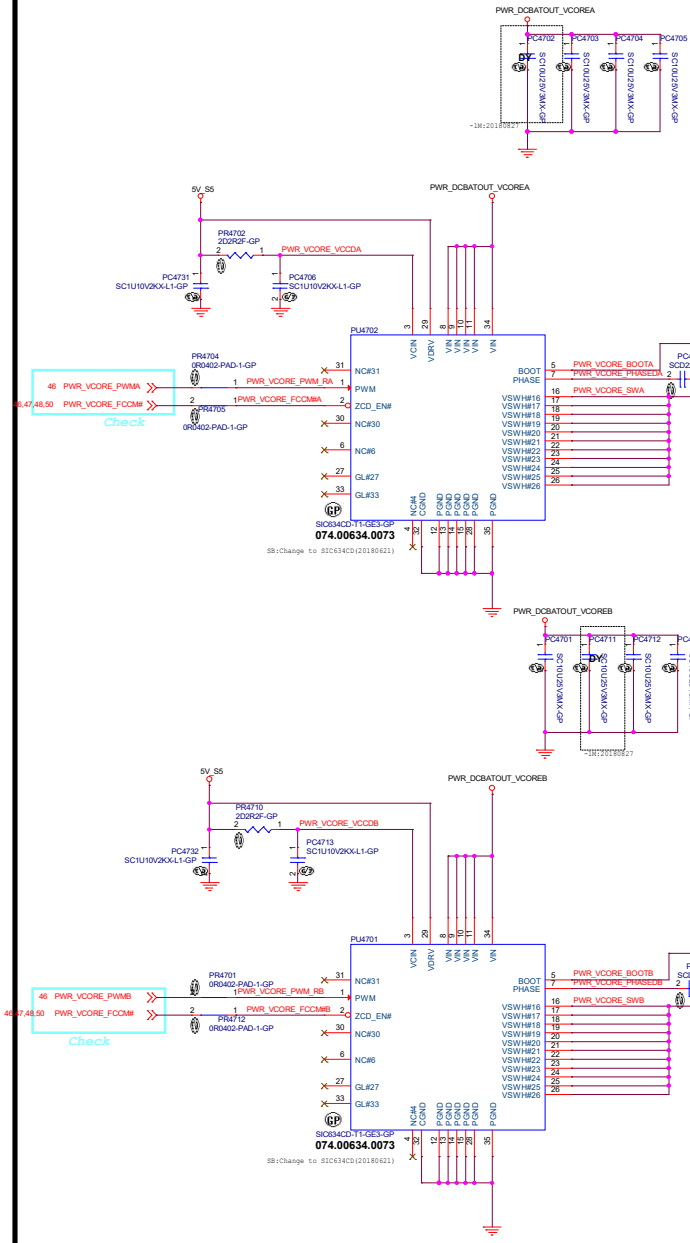




Co-Layer
Close-Gap







WHL_U42
Icc(max)=70A
TDC=48A

22uF/0603 total 35pcs
+22uF_DY * 5pcs

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (AOZ5038Q_VCORE(2/3))

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 47 of 105

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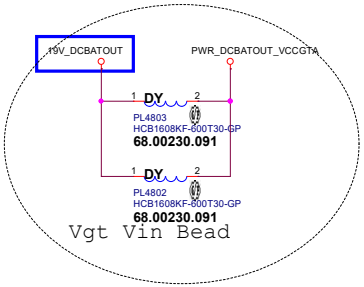
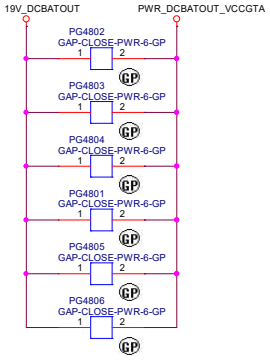
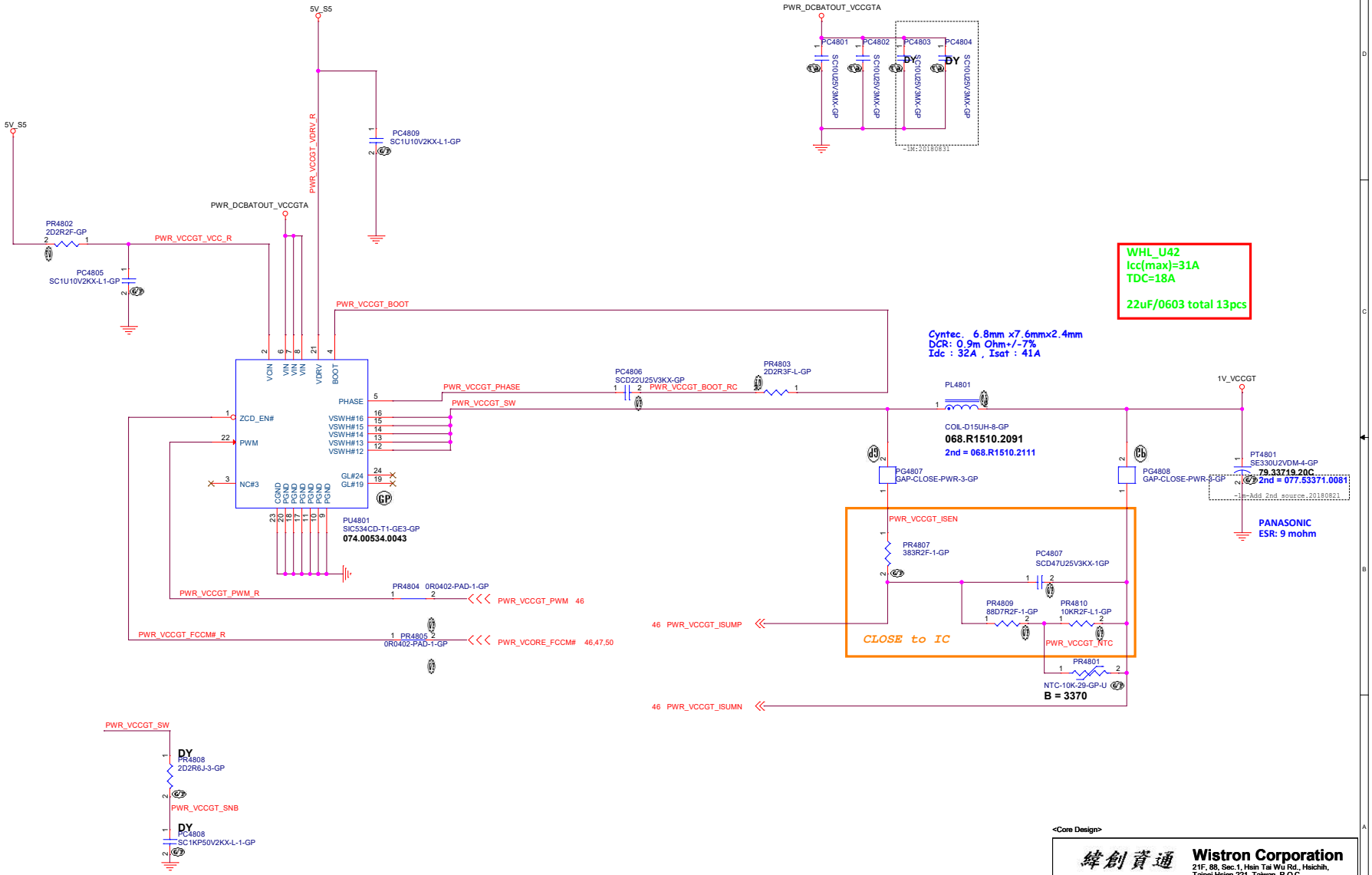


Co-Layer
Close-Gap





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

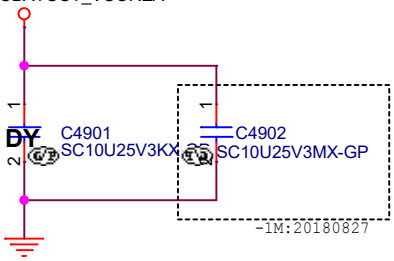
Title: POWER (AOZ5049Q_VCCGT(3/3))

Size	Document Number	Rev
Custom	Woody_WL/Slinky_WL	-1m

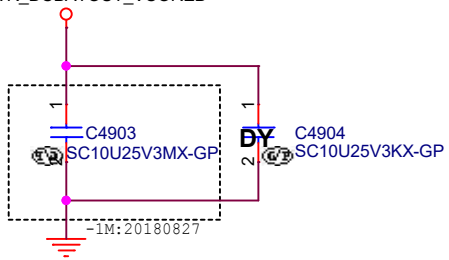
Date: Friday, September 07, 2018 Sheet 48 of 106

Low Noise MLCC

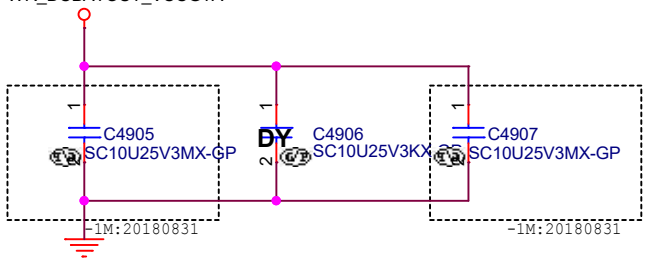
PWR_DCBATOUT_VCOREA



PWR_DCBATOUT_VCOREB



PWR_DCBATOUT_VCCGTA



<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power (EE Reserved)***

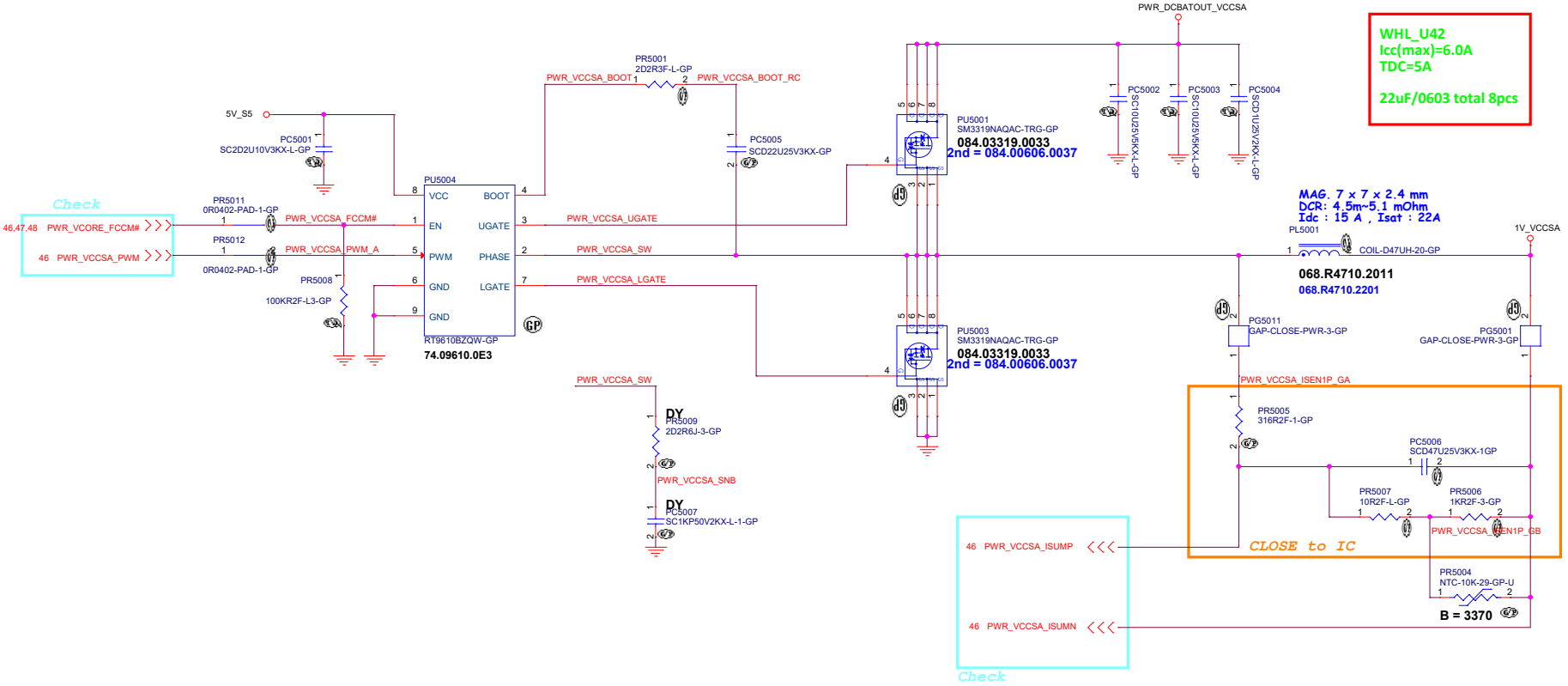
Size	Document Number	Rev
A4	**Woody_WL/Slinky_WL**	**-1m**

Date: Friday, September 07, 2018 Sheet 49 of 106

Main Func = CPU_CORE

OFFPAGE

19V_DCBATOUT — PG5002 GAP-CLOSE-PWR-6-GP — PWR_DCBATOUT_VCCSA
PG5003 GAP-CLOSE-PWR-6-GP



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP1)
Size: Custom
Document Number: Woody_WL/Slinky_WL
Rev: -1m
Date: Friday, September 07, 2018
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OFFPAGE

S5
17,24,40 PM_SLP_S4# 1 PR5102 2 PWR_VDDQ_EN
0R0402-PAD-1-GP

S3
5 VTT_EN 1 PR5114 2 PWR_VTT_EN
0R0402-PAD-1-GP

PH on EE Side

40 PWR_VDDQ_PG PWR_VDDQ_PG

OFFPAGE_GAP

19V_DCBATOUT PWR_DCBATOUT_VDDQ
PG5101 GAP-CLOSE-PWR-6-GP
PG5102 GAP-CLOSE-PWR-6-GP
PG5103 GAP-CLOSE-PWR-6-GP

LAB:20180508

1D2V_S3 PWR_VDDQ_VLDOIN
PG5115 GAP-CLOSE-PWR-6-GP

0D6V_VREF_S0 PWR_VDDQ_VTT
PG5111 GAP-CLOSE-PWR-6-GP
PG5122 GAP-CLOSE-PWR-6-GP
-1:20180803

3D3V_S5 PWR_VDDQ_V3V
PG5119 GAP-CLOSE-PWR-6-GP

2D5V_S3 PWR_VDDQ_V2P5
PG5118 GAP-CLOSE-PWR-6-GP
PG5121 GAP-CLOSE-PWR-6-GP
-1:20180802

PC5104因為layout關係所以直接下PGND即可
獨立下地並遠離NOISE

5V_S5 PR5101 10R2J-L-GP
PR5108 620KR2F-GP
PWR_VDDQ_PH PWR_VDDQ_TON PWR_VDDQ_VCC
PWR_VDDQ_V3V
DDR_AGND
DY PC5102 SC4D7U6D3V3KX-L-GP
If 5V has droop Please mount it
PC5104 SC10U6D3V3MX-L-GP
PC5117 SC10U6D3V2MX-GP-U
PWR_VTT_EN PWR_VDDQ_EN
PWR_VDDQ_PG
TP5101 -1m:20180821
PWR_VDDQ_VLDOIN
PC5118 SC10U6D3V3MX-L-GP
PWR_VDDQ_VTT
PWR_VDDQ_VTTSNS
PWR_VDDQ_VTTREF
PC5111 PC5112 SC10U6D3V3MX-L-GP SC10U6D3V3MX-L-GP
PC5114 SCD1U16V2KX-L-GP
PG5120 GAP-CLOSE-PWR-3-GP
PR5112 0R0402-PAD-1-GP
-1:20180803

PU5101
TON VCC GND V3V S3 S5 PGOOD VLODIN VTT VTTGND VTTSNS VTTREF
V+ V+ V+ V+ V+ BST LX#12 LX#11 LX#10 LX#9 LX#32 V2P5 PGND PGND PGND PGND PGND PGND VDDQSNS VDDQSET
G5416QS1U-GP
074.05416.0073

PWR_DCBATOUT_VDDQ
PR5111 0R0805-PAD-1-GP-U
PWR_VDDQ_BOOT
PC5110 SCD1U25V2KX-L-GP
PC5108 PC5101 PC5105 SC10U25V5KX-L-GP
SCD1U25V2KX-L-GP
PL5101 COIL-1UH-57-GP
68.1R010.20G
2nd = 068.1R010.2351
MAG. 7 x 7 x 2.4 mm
DCR: 11.2m~13.5mOhm
Idc : 9 A , Isat : 16A
TDC : 8A
PWR_VDDQ_V2P5
PC5116 SC22U6D3V3MX-L-GP
PR5110 2D2R6J-3-GP
PWR_VDDQ_SNB
PR5113 0R0402-PAD-1-GP
PC5115 SC1500P50V2KX-2GP
PG5104 GAP-CLOSE-PWR-3-GP
Close to PC5113
PC5106 PC5107 PC5109 PC5113
SC22U6D3V3MX-L-GP SC22U6D3V3MX-L-GP SC22U6D3V3MX-L-GP SC22U6D3V3MX-L-GP
1D2V_S3
PWR_VDDQ_VDDQSET_A
PWR_VDDQ_VDDQSNS
PWR_VDDQ_VDDQSET
R1 PR5105 8K25R2F-1-GP
PC5124 SC10P50V2JN-L-GP
R2 PR5106 12K7R2F-GP
-1:20180815
Vout= 0.75*(1+R1/R2) = 1.237
DDR_AGND

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR (RSVD)
Size: A2 Document Number: Woody_WL/Slinky_WL Rev: -1m
Date: Friday, September 07, 2018 Sheet 51 of 106

OFFPAGE

53 1D8V_S5_PWRGD — PR5209 1 2 PWR_1D0V_EN — 0R0402-PAD-1-GP

OFFPAGE_GAP

19V_DCBATOUT — PG5201 GAP-CLOSE-PWR-6-GP — PWR_DCBATOUT_1D0V

PG5202 GAP-CLOSE-PWR-6-GP

PG5203 GAP-CLOSE-PWR-6-GP

1D0V_S5 — PG5204 GAP-CLOSE-PWR-6-GP — PWR_1D0V

PG5205 GAP-CLOSE-PWR-8-GP

PG5206 GAP-CLOSE-PWR-8-GP

PG5207 GAP-CLOSE-PWR-8-GP

PG5208 GAP-CLOSE-PWR-8-GP

PG5209 GAP-CLOSE-PWR-8-GP

PG5211 GAP-CLOSE-PWR-6-GP

PG5212 GAP-CLOSE-PWR-8-GP

PG5213 GAP-CLOSE-PWR-8-GP

PG5214 GAP-CLOSE-PWR-8-GP

SSID = PWR.Plane.Regulator_1p0v

IC / COM	AOZ2262(10A) 074.02262.0043	AOZ2261(8A) 074.02261.0A73	AOZ2260(6A) 074.02260.0043
Chock	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A	68.1R01A.20B IDC : 10A
Output CAP	22uF/6.3V * 5pcs DY*1	22uF/6.3V * 4pcs DY*1	22uF/6.3V * 4pcs DY*1

AOZ2262 for 1D05V

OCP :15A
TDC : 10A

3D3V_S5 — PR5208 100KR2J-1-GP DY — SB:20180627 — PWR_1D0V_PG

5V_S5 — PC5202 SC4D7U25V5KX-L2-GP

PWR_DCBATOUT_1D0V — PC5208 SCD1U25V2KX-L-GP — PC5209 — PC5210 SC10U25V5KX-L-GP SC10U25V5KX-L-GP

PR5201 95K3R2F-GP

PU5201 AOZ2262QI-10-GP-U 074.02262.0043

Pin	Name
21	VCC
7	IN#7
8	IN#8
9	IN#9
6	TON
1	PGOOD
2	EN
3	PFM#
22	SS
18	LX#18
17	LX#17
16	LX#16
11	LX#11
10	LX#10
20	BST
5	FB
4	AGND
19	PGND
14	PGND
13	PGND
12	PGND
15	PGND

PWR_1D0V_TON — PWR_1D0V_PG — PWR_1D0V_EN — PWR_1D0V_PFM — PWR_1D0V_SS

PC5214 SC1KP50V2KX-L-1-GP — PR5203 100KR2F-L3-GP — PC5213 SCD01U25V2KX-3GP — SB:20180723

PWR_1D0V_PH — PC5204 SCD1U25V2KX-L-GP

PWR_1D0V_BT — PWR_1D0V_VFB

PL5201 COIL-1UH-57-GP

MAG. 7 x 7 x 2.4 mm
DCR: 11.2m~13.5mOhm
Idc : 9 A , Isat : 16A

68.1R010.20G
2nd = 068.1R010.2351

PWR_1D0V

PG5210 GAP-CLOSE-PWR-3-GP

PC5201 PC5203 PC5205 PC5207 PC5206

SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP
SC22U6D3V3MX-L1-GP

PWR_1D0V_VFB_A

PR5202 3K16R2F-GP R1 — SB-20180725

DY — PC5212 SC220P50V2KX-3GP

PR5204 10KR2F-L1-GP R2

Vo=0.8x(1+R1/R2)
=0.8x(1+3.16/10)
=1.05

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (G5416_VDDQ/VTT/VPP)

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 52 of 106

1D8V_S5

1D8V_S5 POWER GOOD

52 1D8V_S5_PWRGD

17,45,72 PWR_3D3V_PG

17,24,40,60 PM_SLP_S3#

PD = (Vin Vout) x Iout
= (3.3 - 1.8) x 0.5A = 0.75W
PD de-rating(%) = 0.75W/1.33W = 56.4%

1125 Simon
Vendor suggest to replace 74.09025.A3D by 74.09025.D3D

5V_S5
PR5302 2D2R2F-GP
PC5302 SC1U10V2KX-L1-GP
PU5301
PWR_1D8V_S5_VDD
PWR_1D8V_S5_PVDD
PWR_1D8V_S5_EN
VPP NC#9 VIN VEN GND
NC#1 VO#2 VO#3 ADJ POK
PWR_1D8V_S5_FB
1D8V_S5_PWRGD
G9661-25ADJRE1U-GP
074.09661.0033

3D3V_S5
PG5301 GAP-CLOSE-PWR-6-GP
PG5302 GAP-CLOSE-... 6-GP
PC5303 SC10U6D3V3MX-L-GP
DY
PC5304 SC10U6D3V3MX-L-GP
FC5301 DY SCD1U25V2KX-L-GP
PWR_3D3V_PG
PR5301 0R0402-PAD-1-GP
PWR_1D8V_S5_EN
PC5307 SC1U10V2KX-L1-GP DY

R1 PR5303 12K7R2F-GP
PC5305 SC22P50V2JN-L-GP
PWR_1D8V_S5_FB
R2 PR5304 10KR2F-L1-GP

Vout Setting
Vout = 0.8 * (1 + R1/R2)
= 0.8 * (1 + 12K7 / 10K)
= 1.816V

DY
PC5306 SC10U6D3V3MX-L-GP
PC5301 SC10U6D3V3MX-L-GP

PWR_1D8V
PG5303 GAP-CLOSE-PWR-6-GP
PG5304 GAP-CLOSE-... 6-GP
1D8V_S5
PWR_1D8V
FC5310 DY SCD1U25V2KX-L-GP

3D3V_S5
PR5305 10KR2F-L1-GP
1D8V_S5_PWRGD

TLV70215 for 1D5V_S0
Enable=1.5V
Disable=0.4V

3D3V_S5
PC5309 SC1U10V2KX-L1-GP
Iomax=300mA
1D5V_S0
PU5302
VIN VSS ON/OFF VOUT NC#4
S-1339D15-M5001-GP
74.01339.B3F
2nd = 074.09078.0A3F
-SB 20170324
PC5308 SC1U10V2KX-L1-GP

PM_SLP_S3#
PR5315 0R0402-PAD
1D5V_PWR_EN
PWR_1D5V_S0_EN
PC5310 DY SC22P50V2JN-L-GP
PR5314 100KR2J-4-GP

Fix Vout=1D5V
Imax=300mA
OCP = 400mA

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: POWER (G5416_VDDQ/VTT/VPP)

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 53 of 106

Blanking

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved		
Size: A4	Document Number: Woody_WL/Slinky_WL	Rev: -1m
Date: Friday, September 07, 2018	Sheet 54 of 106	

Main Func = LCD

24 MODEL_ID_AD
4 eDP_AUX_CPU_P
4 eDP_AUX_CPU_N
4 eDP_TX_CPU_P0
4 eDP_TX_CPU_N0
4 eDP_TX_CPU_P1
4 eDP_TX_CPU_N1
18,24,70,72 SML1_DATA
18,24,70,72 SML1_CLK
3 TOUCH_INT#
24 TOUCH_EN
20 TOUCH_DET#
4 eDP_VDDEN_CPU
24 BLON_OUT
4 eDP_HPD_CPU
4 eDP_BLCTRL_CPU
16 TS_USB20_P
16 TS_USB20_N
20,24 TS_I2C0_SDA_CON
20,24 TS_I2C0_SCL_CON
20 TOUCH_S_RST#
89 eDP_HPD_CON
89 eDP_BLEN_CON
89 eDP_BLCTRL_CON
89 TOUCH_DET#_R
89 5V_TS_S0
89 eDP_TX_CON_P0
89 eDP_TX_CON_N0
89 eDP_TX_CON_P1
89 eDP_TX_CON_N1
89 eDP_AUX_CON_P
89 eDP_AUX_CON_N
89 TOUCH_INTR#

EDP1
STAR-CON40-1-GP

MODEL_ID_AD
eDP_AUX_CON_P C5511 SCD1U16V2KX-L-GP eDP_AUX_CPU_P
eDP_AUX_CON_N C5512 SCD1U16V2KX-L-GP eDP_AUX_CPU_N
eDP_TX_CON_P0 C5513 SCD1U16V2KX-L-GP eDP_TX_CPU_P0
eDP_TX_CON_N0 C5514 SCD1U16V2KX-L-GP eDP_TX_CPU_N0
eDP_TX_CON_P1 C5515 SCD1U16V2KX-L-GP eDP_TX_CPU_P1
eDP_TX_CON_N1 C5516 SCD1U16V2KX-L-GP eDP_TX_CPU_N1
SML1_DATA
SML1_CLK
TOUCH_INTR# R5508 R5509 TS_I2C 33R2J-L1-GP 0R0402-PAD TOUCH_INT# TOUCH_EN eDP_HPD_CON
To PCH
To EC
3D3V_S5 FOR G-SENSOR
3D3V_LCDVDD_S0
TOUCH_DET#_R R5505 DY 33R2J-L1-GP TOUCH_DET# TOUCH_S_RST#_R
5V_TS_S0
TS_USB20_CON_N
TS_USB20_CON_P
eDP_BLCTRL_CON R5502 33R2J-L1-GP eDP_BLEN_CON eDP_BLCTRL_CPU
19V_DCBATOUT_LCD

20.K0809.040
2nd = 20.K0678.040
3rd = 020.K0160.0040

FOR G-SENSOR
SML1_DATA
SML1_CLK
ED5501
AZ5125-02S-R7G-GP
GSENSOR_1
75.05125.07D
2nd = 075.05125.007D

EU5501
TS_USB20_CON_N
TS_USB20_CON_P
5V_S0
I/O1 I/O4 GND VDD I/O2 I/O3
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

Inverter Power
19V_DCBATOUT_LCD
19V_DCBATOUT
F5501
POLYSW-1D1A24V-GP-U
69.50007.A31
2nd = 069.41101.0001
C5501 SC4D7U25V5KX-L2-GP
C5502 DY SCD1U50V3KX-L-GP
SB-20180725

TOUCH_S_RST#_R
DY C5518 SC10P50V2JN-L1-GP
TOUCH_INT#
DY C5517 SC10P50V2JN-L1-GP
eDP_BLEN_CON
eDP_HPD_CON
RN5501
SRN1KJ-7-GP
BLON_OUT
eDP_HPD_CPU
eDP_HPD_CON
eDP_BLEN_CON
RN5502
SRN100KJ-6-GP

3D3V_S5
U5501
IN EN OUT GND OC#
G517F1T12U-GP
074.51712.009F
2nd = 074.22811.009F
eDP_VDDEN_CPU
C5506 SC1U10V2KX-L-GP
R5503 100KR2F-L3-GP
3D3V_LCDVDD_S0
C5505 DY SC4D7U6D3V3KX-L-GP
C5503 DY SCD1U25V2KX-L-GP
C5504 SC1U10V2KX-L-GP
20170303 change 1uF

Touch panel Power
TS_I2C
R5506 0R2J-L-GP TS_I2C0_SDA_CON
R5507 0R2J-L-GP TS_I2C0_SCL_CON
TS_USB20_CON_P
TS_USB20_CON_N
R5512 0R0402-PAD TS_USB20_P
R5513 0R0402-PAD TS_USB20_N
TS_USB
TOUCH_S_RST#_R
R5515 33R2J-L1-GP TOUCH_S_RST#
R5514 0R0402-PAD
TS_USB
5V_S0 3D3V_S0
5V_TS_S0
TS_I2C
R5510 0R3J-L1-GP
R5511 0R0402-PAD
TS_USB
C5509 SC10U6D3V3MX-GP
DY C5510 SC1U10V2KX-L1-GP
SB-20180717

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: LCD CONN
Size: Custom
Document Number: Woody_WL/Slinky_WL
Rev: -1m
Date: Friday, September 07, 2018
Sheet 55 of 106

Blanking

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A4 | Document Number: Woody_WL/Slinky_WL | Rev: -1m

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SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN

4 HDMI_DDI_TX_P0
4 HDMI_DDI_TX_N0
4 HDMI_DDI_TX_P1
4 HDMI_DDI_TX_N1
4 HDMI_DDI_TX_P2
4 HDMI_DDI_TX_N2

4 HDMI_DDI_TX_P3
4 HDMI_DDI_TX_N3

4 HDMI_SCL_CPU
4 HDMI_SDA_CPU
4 HDMI_DET_CPU

89 HDMI_DDI_TX_CON_N3
89 HDMI_DDI_TX_CON_P3

89 HDMI_DDI_TX_CON_P0
89 HDMI_DDI_TX_CON_N0
89 HDMI_DDI_TX_CON_P1
89 HDMI_DDI_TX_CON_N1
89 HDMI_DDI_TX_CON_P2
89 HDMI_DDI_TX_CON_N2

89 HDMI_CLK_CON
89 HDMI_DATA_CON
89 HDMI_DET_CON

5V_HDMI_S0 — F5701 POLYSW-1206/8V-9-GP-U — 5V_S0
C5733 SCD1U16V2KX-L-GP
69.48001.081
2ND = 69.50011.081

HDMI1 SKT-HDMI23-92-GP-U
20170302 Change
22.10296.981
2nd = 022.10025.00S1

3D3V_S0 — 4K7R2J-L-GP — R5727 PS8201_EN
R5728 PS8201_DDCBUF
R5731
-SB DY
R5713 PS8201_PRE
R5714
R5724 PS8201_CFG
R5726 PS8201_EQ
R5709
R5730 PS8201_ISET
R5712

ER5701 ER5702 ER5703 ER5704 — 150R2J-L1-GP-U

5V_HDMI_S0 — D5701 BAW56-9-GP-U
75.00056.07D
2nd = 83.00056.Y11
5V_DDC_HDMI1 5V_DDC_HDMI2
RN5701 SRN2K2J-5-GP
HDMI_CLK_CON HDMI_DATA_CON

EMI Request:
ED5701 L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
ED5702 L05ESDL5V0NA-4-GP
075.00550.0071
2nd = 075.08809.0073
3rd = 075.01043.0073
ED5703 AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C
20170208 ENG change to 5V_HDMI_S0

1D5V_S0 — C5713 C5712 C5714 SCD01U25V2KX-3GP / SCD01U25V2KX-GP

U5701 PS8201ATQFN40GTR2-A0-GP
71.08201.G03
VDD33 VDD15 VDD15 VDD15 VDD15
OUT_CKN OUT_CKP OUT_D0P OUT_D0N OUT_D1P OUT_D1N OUT_D2P OUT_D2N
SCL_SNK SDA_SNK HPD_SNK
SCL_SRC SDA_SRC HPD_SRC
I2C_CTL_EN PRE
IN_D0P IN_D0N IN_D1P IN_D1N IN_D2P IN_D2N IN_CKP IN_CKN
DCIN_EN/SCL_CTL DDCBUF/SDA_CTL EQ/I2C_ADDR CFG REXT
NC#12 NC#15 NC#37 NC#34
GND GND PD#

HDMI_DDI_TX_P0 HDMI_DDI_TX_N0 HDMI_DDI_TX_P1 HDMI_DDI_TX_N1 HDMI_DDI_TX_P2 HDMI_DDI_TX_N2 HDMI_DDI_TX_P3 HDMI_DDI_TX_N3 — LS — C5724 C5723 C5726 C5725 C5728 C5727 C5722 C5721 — SCD1U16V2KX-L-GP — HDMI_DDI_TX_P0_C HDMI_DDI_TX_N0_C HDMI_DDI_TX_P1_C HDMI_DDI_TX_N1_C HDMI_DDI_TX_P2_C HDMI_DDI_TX_N2_C HDMI_DDI_TX_P3_C HDMI_DDI_TX_N3_C

HDMI_SCL_CPU HDMI_SDA_CPU HDMI_DET_CPU
HDMI_HPD_E — R5722 0R0402-PAD-1-GP
I2C_CTL_EN — R5723 4K7R2J-L-GP
PS8201_PRE
PS8201_PD# — R5725 4K7R2J-L-GP
PS8201_EN PS8201_DDCBUF PS8201_EQ PS8201_CFG PS8201_REXT — R5721 4K02R2F-GP
PS8201_ISET

1D5V_S0 — C5710 C5709 C5711 SCD1U16V2KX-L-GP / SCD1U25V2KX-L-GP
3D3V_S0 — C5716 C5715 SCD1U25V2KX-3GP / SCD1U16V2KX-L-GP

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: HDMI Level Shifter/Connector
Size: Custom
Document Number: Woody_WL/Slinky_WL
Rev: -1m
Date: Friday, September 07, 2018
Sheet 57 of 106

Blanking

<Core Design>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**		
Size: A	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
Date: Friday, September 07, 2018	Sheet 58 of 106	

Blanking

<Core Design>

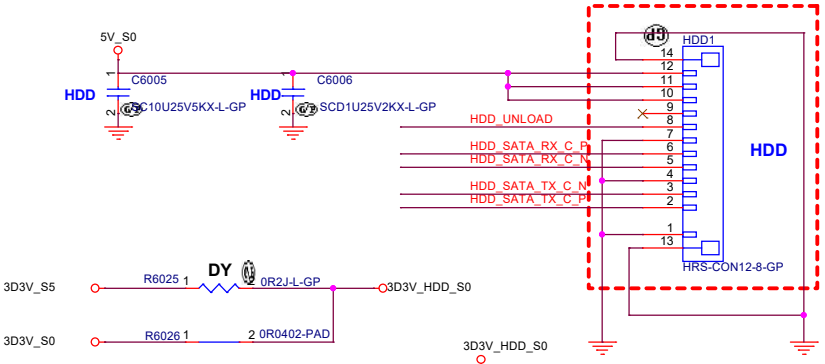
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

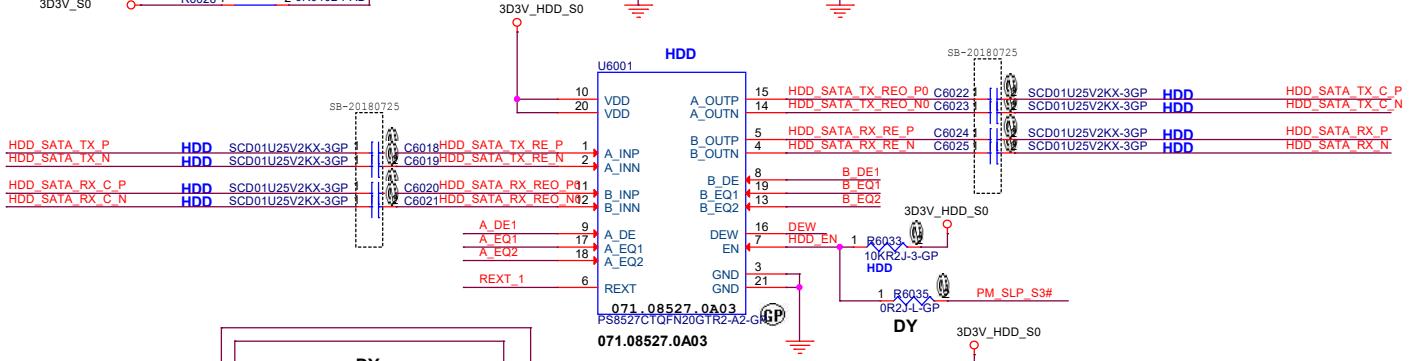
Title: ***DVI(Reserved)***		
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
Date: Friday, September 07, 2018	Sheet 59 of 106	

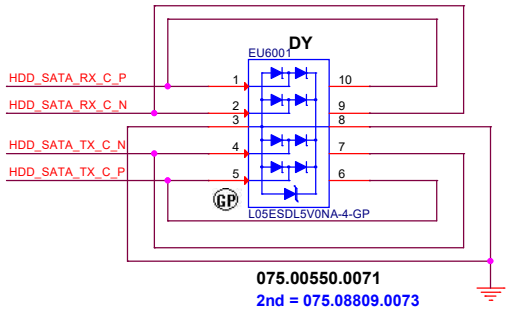
HDD_SATA_RX_P 16
HDD_SATA_RX_N 16
HDD_SATA_TX_N 16
HDD_SATA_TX_P 16
HDD_UNLOAD 69
PM_SLP_S3# 17,24,40,53

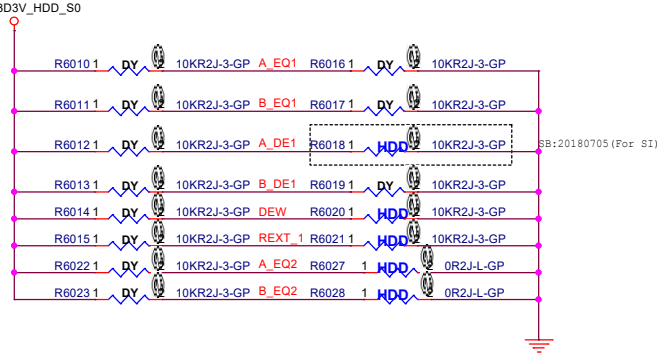
SSID = SATA

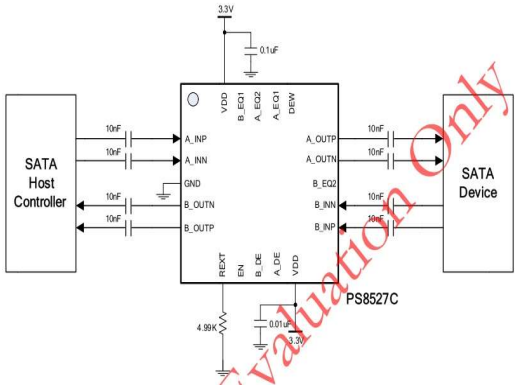
SATA HDD Connector











9	A_DE	I	Programmable output de-emphasis level setting for channel A. Internally tied to VDD/2(M status).

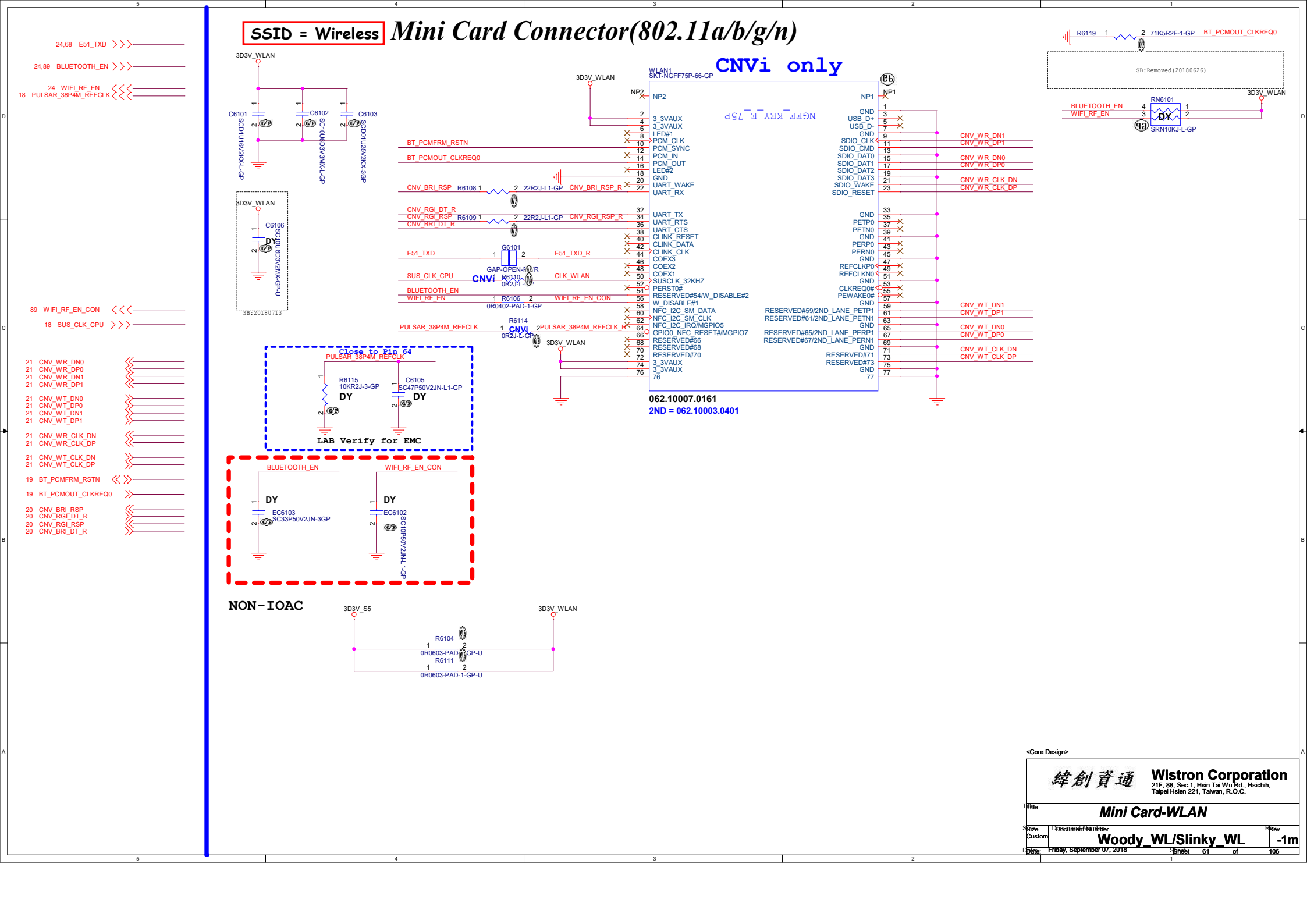
A_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-6dB

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD_GSENSOR
Size: A3
Document Number: Woody_WL/Slinky_WL
Rev: -1m
Date: Friday, September 07, 2018
Sheet 60 of 106

SSID = Wireless Mini Card Connector(802.11a/b/g/n)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Mini Card-WLAN

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 61 of 106

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<Core Design>

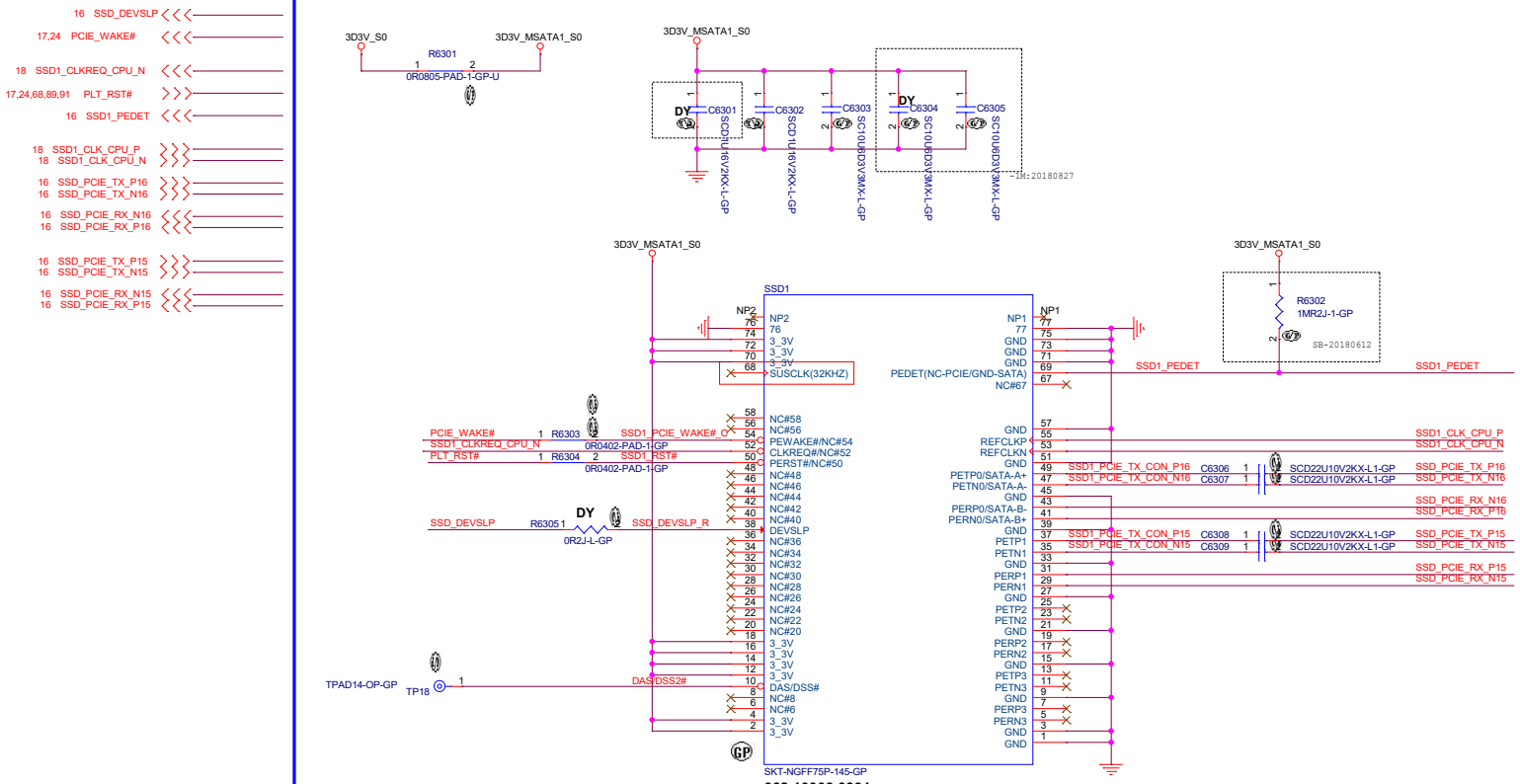
緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
Date: Friday, September 07, 2018	Sheet 62 of 106	

SSID = mSATA

Mini Card Connector(mSATA)



062.10003.0991

2ND = 062.10003.00A1

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the 10 nF capacitor on Rx can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer tChapter 3, "General Differential Signals Design Guidelines" " along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration where the motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

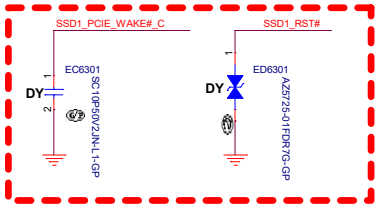


Table 27. Socket 2 Module Configuration

State #	Module Configuration Decodes				Module Type and Main Host Interface[1]	Port Configuration[2]
	CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)		
0	GND	GND	GND	GND	SSD – SATA	N/A
1	GND	N/C	GND	GND	SSD – PCIe	N/A

Pin define from PCH and socket side.

	High (1)	Low (0)
PCH GPIO	SATA	PCIe
M.2 CONFIG_1	PCIe**	SATA

** Native: Internal Pull-Up (15k-40k) when function.

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: mSTATA

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 63 of 106

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<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

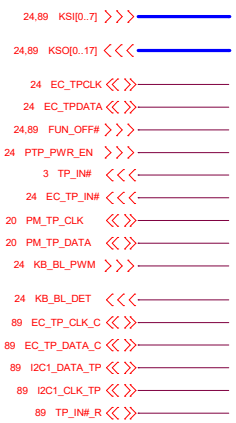
Size	Document Number	Rev
A4	Woody_WL/Slinky_WL	-1m

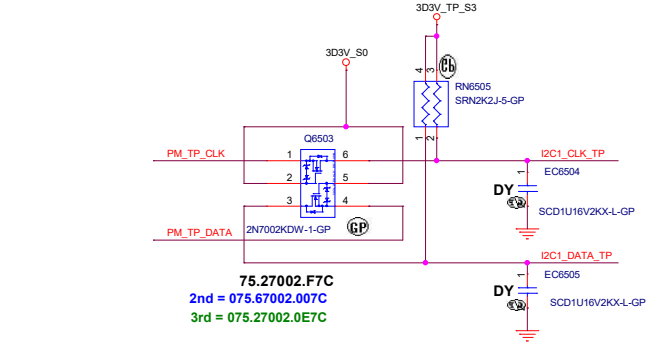
Date: Friday, September 07, 2018 Sheet 64 of 106

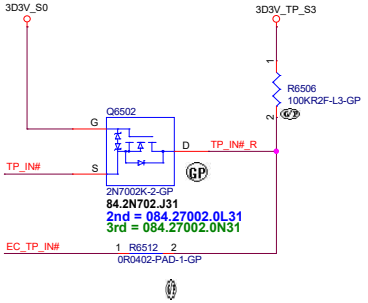
SSID = KBC

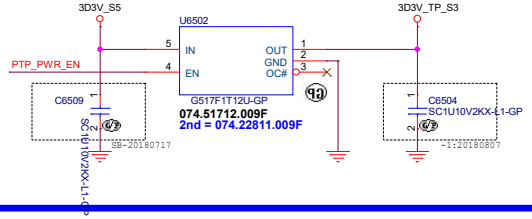
TOUCH PAD

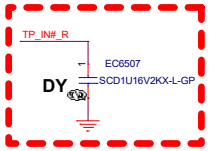
Internal KeyBoard Connector

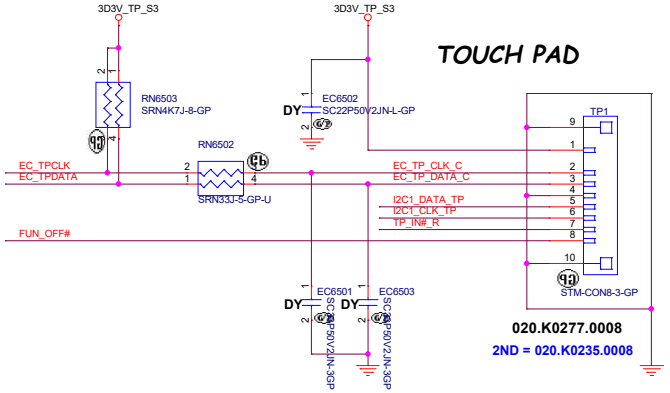


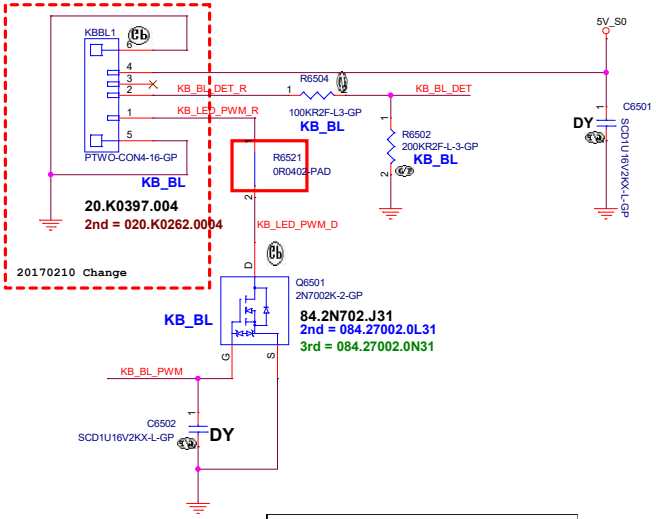


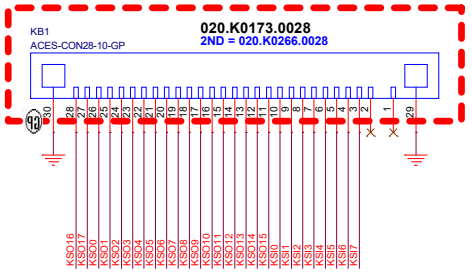


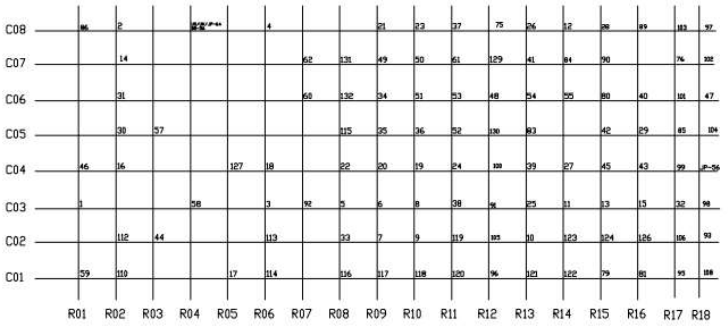


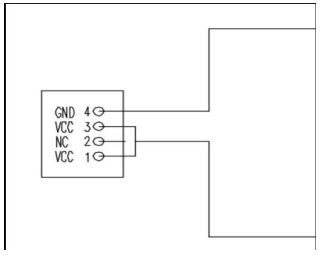












<core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 65 of 106

24,89 STDBY_LED
24,89 POWER_LED
24,89 CHARGE_LED
24,89 DC_BATFULL
24 Value+
24 Value-
24 LID_CLOSE#
24 LID_CLOSE2#
16,89 USB4_USB20_N
16,89 USB4_USB20_P
16,89 CARD1_USB20_N
16,89 CARD1_USB20_P
43 BAT_RST
24,89 KBC_PWRBTN#
24,35 USB_PWR_EN
27,66,89 RING2
27,66,89 RING2
27,66,89 SELEEVE
27,66,89 SELEEVE
27,89 AUD_HP1_JACK_R2
27,89 AUD_HP1_JACK_L2
27,89 AUD_HP1_JD#

SSID = User.Interface

High Active 2A

5V_S5
C6601 SC1U10V2KX-L1-GP
USB_PWR_EN
U6601
IN
EN
OUT
GND
OC#
G517F1T12U-GP
074.51712.009F
2nd = 074.22811.009F
5V_USB20
DY C6602 SCD1U16V2KX-L-GP
SB-20160717

Close connector

EU6601
USB4_USB20_N
CARD1_USB20_N
I/O1
GND
I/O2
I/O3
I/O4
VDD
USB4_USB20_P
5V_USB20
CARD1_USB20_P
AZC099-04S-2-GP
075.09904.0A7C
2nd = 075.01256.007C
3rd = 75.09904.07C

PWRBT1
KBC_PWRBTN#
SW-TACT-124-GP
62.40078.001
LAB

Close SMB1

IOBD1
STAR-CON40-1-GP
USB4_USB20_N
USB4_USB20_P
CARD1_USB20_N
CARD1_USB20_P
Value+_R
Value-_R
BAT_RST
KBC_PWRBTN#
LID_CLOSE#
LID_CLOSE2#
RING2
RING2
SELEEVE
SELEEVE
AUD_HP1_JACK_R2
AUD_HP1_JACK_L2
AUD_HP1_JD#
STDBY_LED
POWER_LED
DC_BATFULL
CHARGE_LED
3D3V_S0
RN6601
SRN2K2J-5-GP
3D3V_AUX_S5
5V_S5
5V_AUX_S5
5V_USB20
AUD_AGND
20.K0809.040
2ND = 20.K0678.040
3rd = 020.K0160.0040

3D3V_S5
RN6602
SRN100KJ-6-GP
KBC_PWRBTN#
ED6601
AZ5725-01FDR7G-GP

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button
Size: Custom
Document Number: Woody_WL/Slinky_WL
Rev: -1m
Date: Friday, September 07, 2018
Sheet 66 of 106

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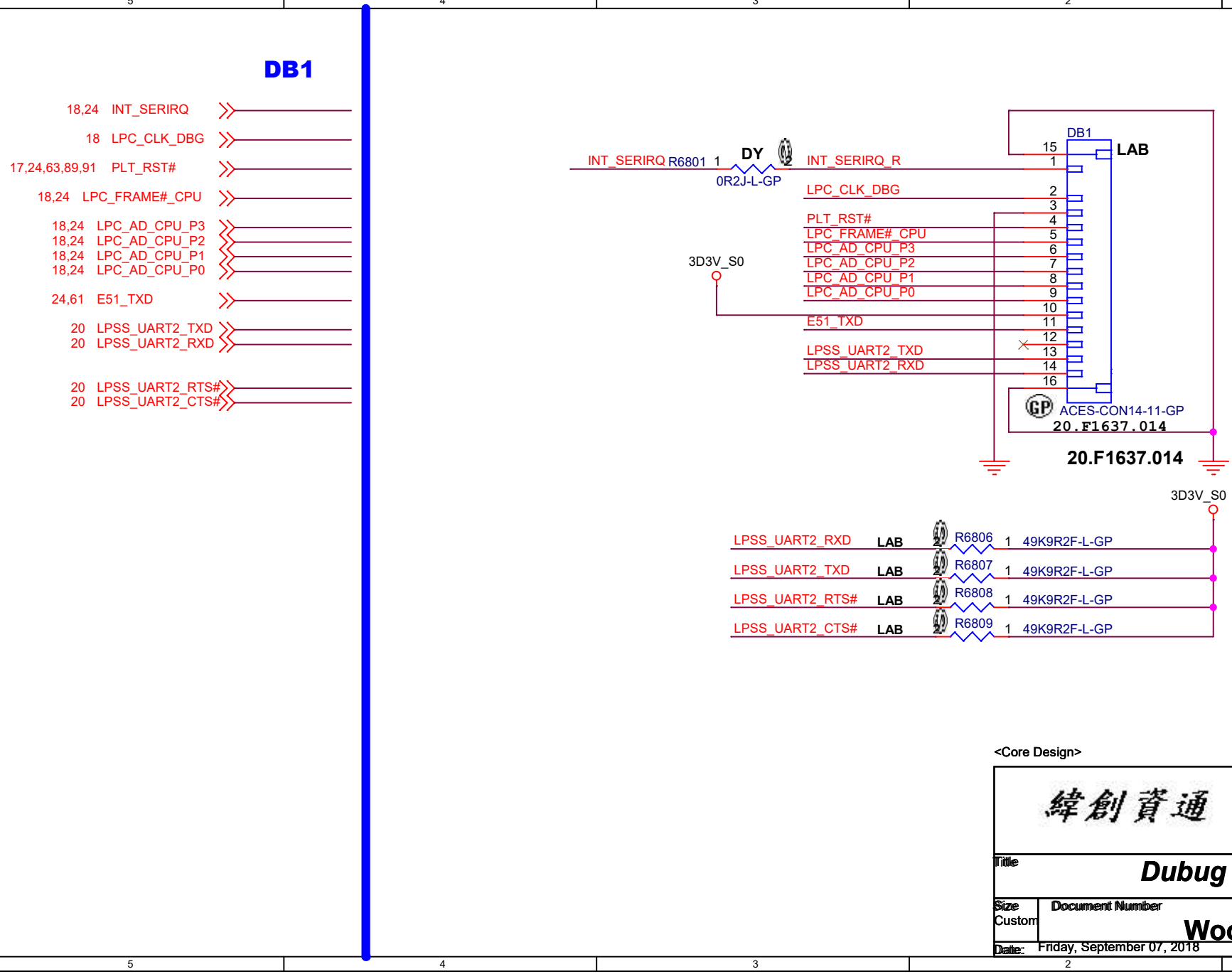
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Woody_WL/Slinky_WL	-1m

Date: Friday, September 07, 2018 Sheet 67 of 106



<Core Design>

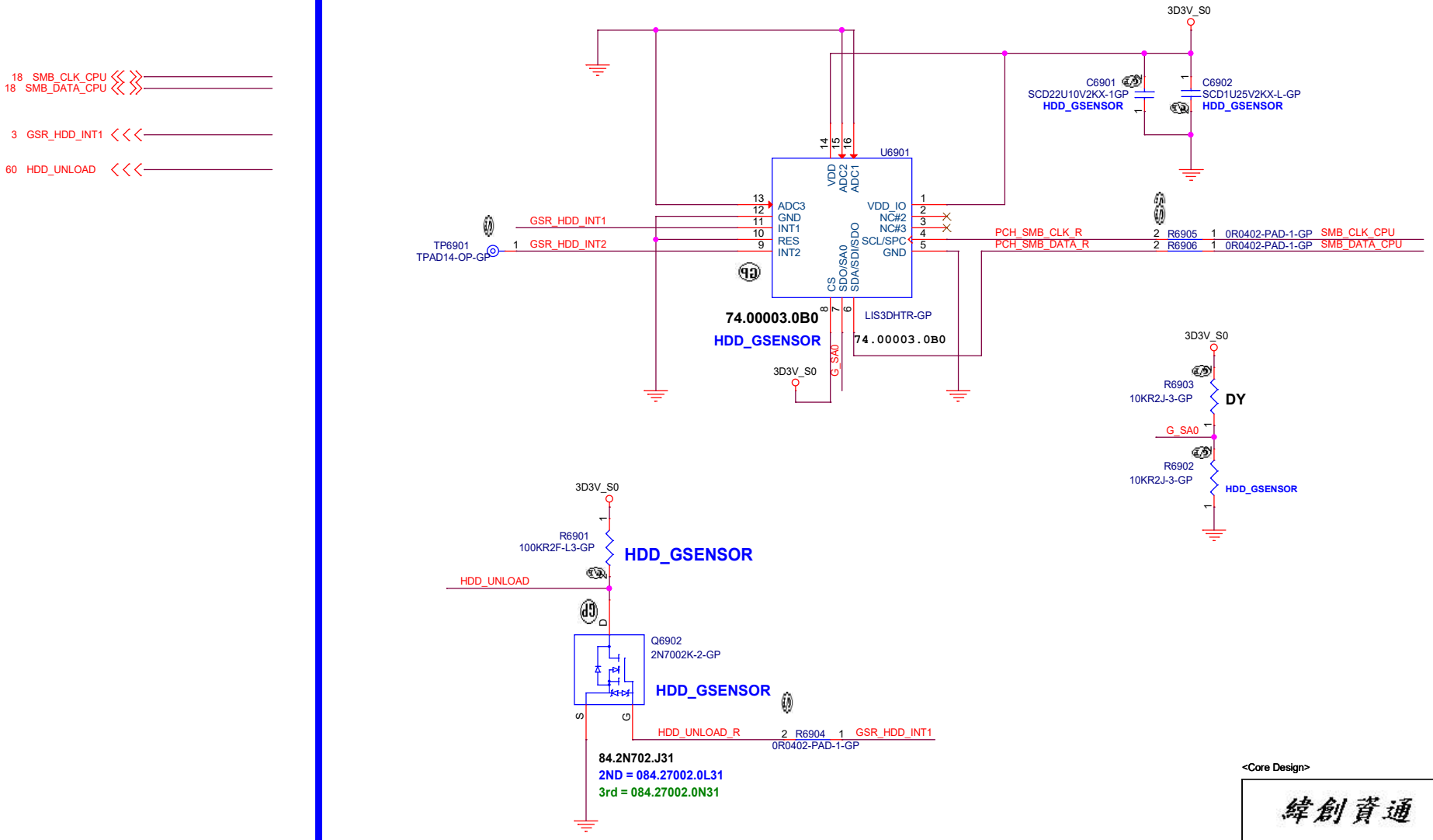
緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
Custom	Woody_WL/Slinky_WL	-1m
Date: Friday, September 07, 2018	Sheet 68 of 106	



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD_G_Sensor

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 69 of 106

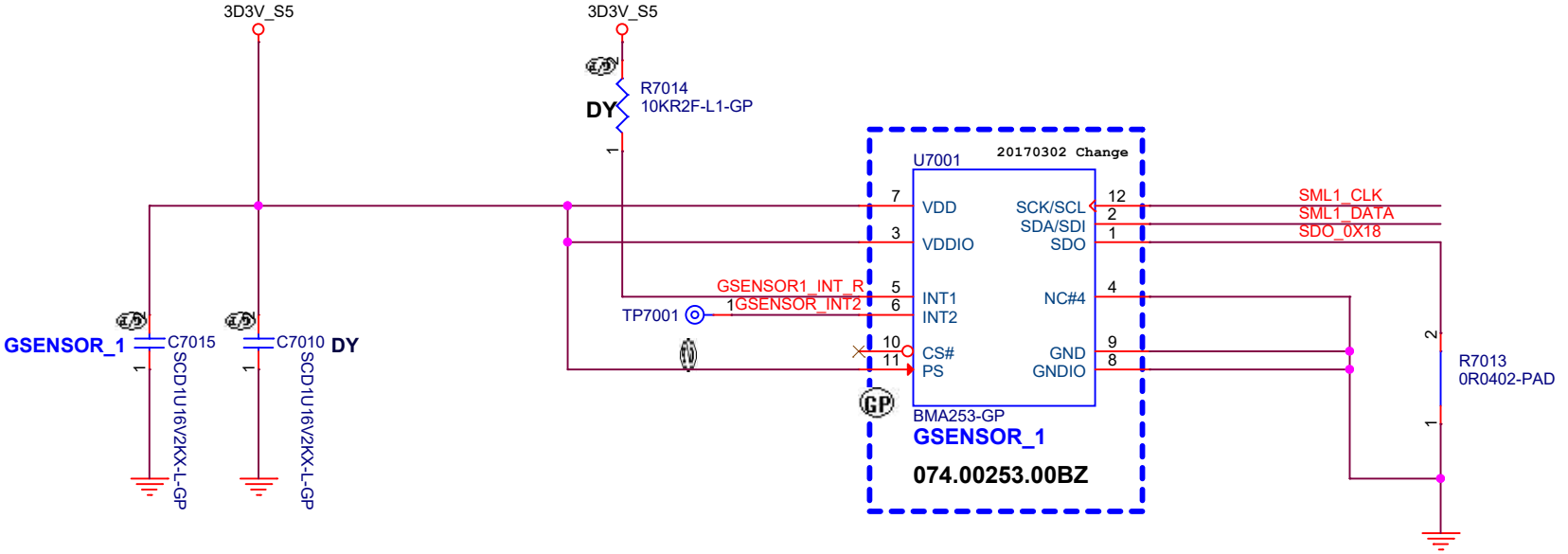
18,24,55,72 SML1_CLK
18,24,55,72 SML1_DATA

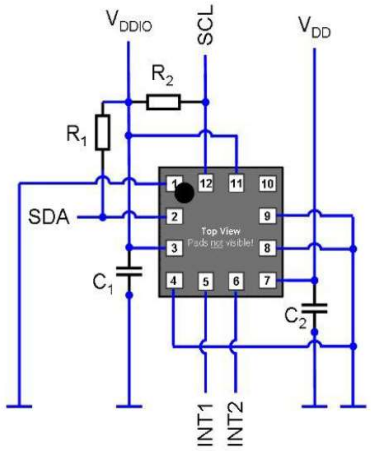
Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SSID = User.Interface

G Sensor

The default I²C address of the device is 0011000b (0x18). It is used if the SDO pin is pulled to 'GND'. The alternative address 0011001b (0x19) is selected by pulling the SDO pin to 'V_{DDIO}'.





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *G SENSOR*

Size	Document Number	Rev
Custom	Woody_WL/Slinky_WL	-1m

Date: Friday, September 07, 2018 Sheet 70 of 106

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<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	Woody_WL/Slinky_WL	-1m

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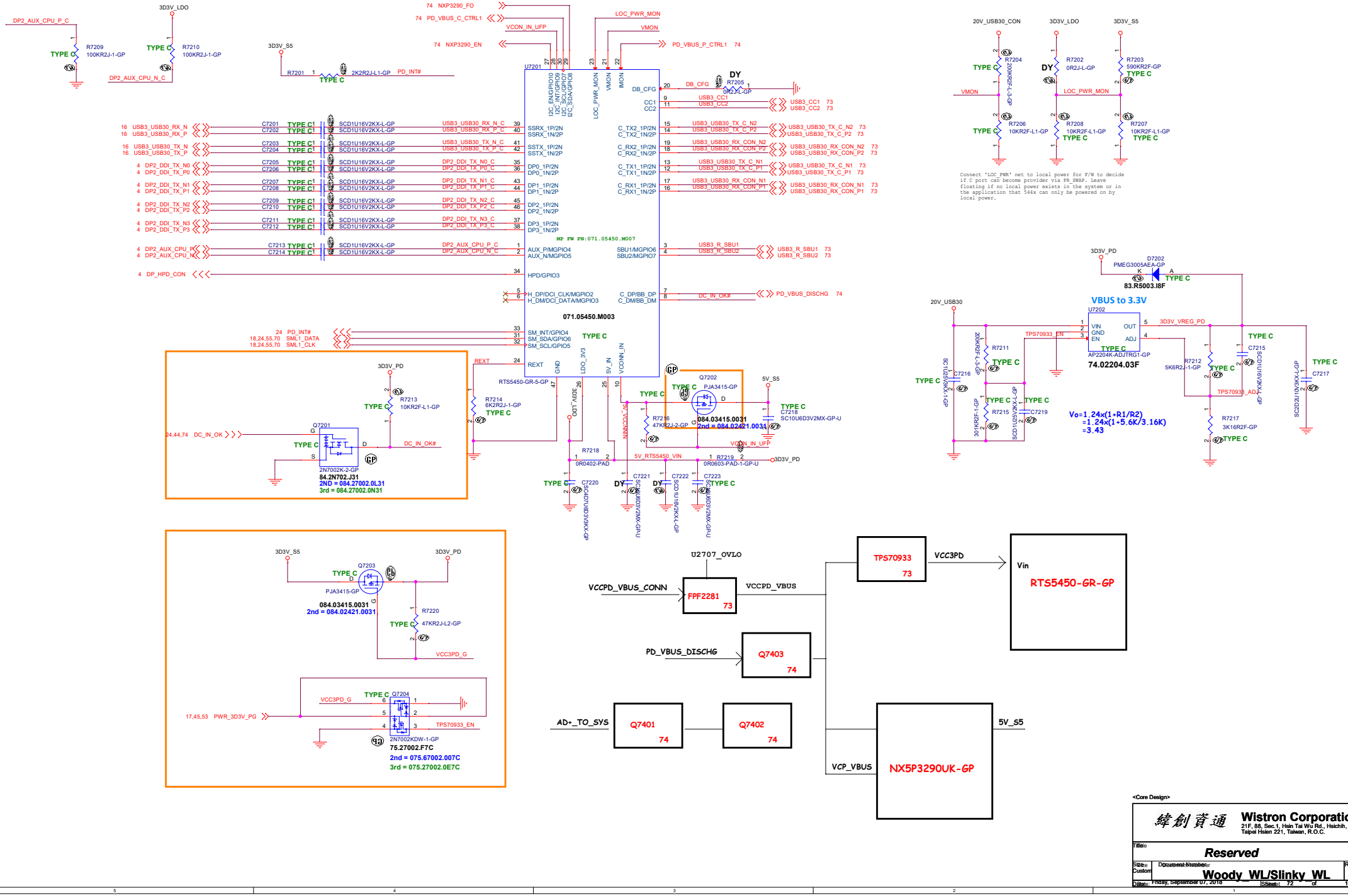
U7201
071.05450.M003
MP FW PN:071.05450.M007
RTS5450-GR-5-GP
Q7201
2N7002K-2-GP
84.2N702.J31
2ND = 084.27002.0L31
3rd = 084.27002.0N31
Q7202
PJA3415-GP
084.03415.0031
2nd = 084.02421.0031
Q7203
PJA3415-GP
084.03415.0031
2nd = 084.02421.0031
Q7204
2N7002KDW-1-GP
75.27002.F7C
2nd = 075.67002.007C
3rd = 075.27002.0E7C
U2707_OVLO
FPF2281
73
VCCPD_VBUS_CONN
VCCPD_VBUS
TPS70933
73
VCC3PD
Vin
RTS5450-GR-GP
PD_VBUS_DISCHG
Q7403
74
AD+_TO_SYS
Q7401
74
Q7402
74
VCP_VBUS
NX5P3290UK-GP
5V_S5
U7202
AP2204K-ADJTRG1-GP
74.02204.03F
VBUS to 3.3V
Vo=1.24x(1+R1/R2)
=1.24x(1+5.6K/3.16K)
=3.43
D7202
PMEG3005AEA-GP
83.R5003.I8F
Connect 'LOC_PWR' net to local power for F/W to decide if C port can become provider via PR_SWAP. Leave floating if no local power exists in the system or in the application that 544x can only be powered on by local power.
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Reserved
Woody_WL/Slinky_WL
-1m
Friday, September 07, 2018
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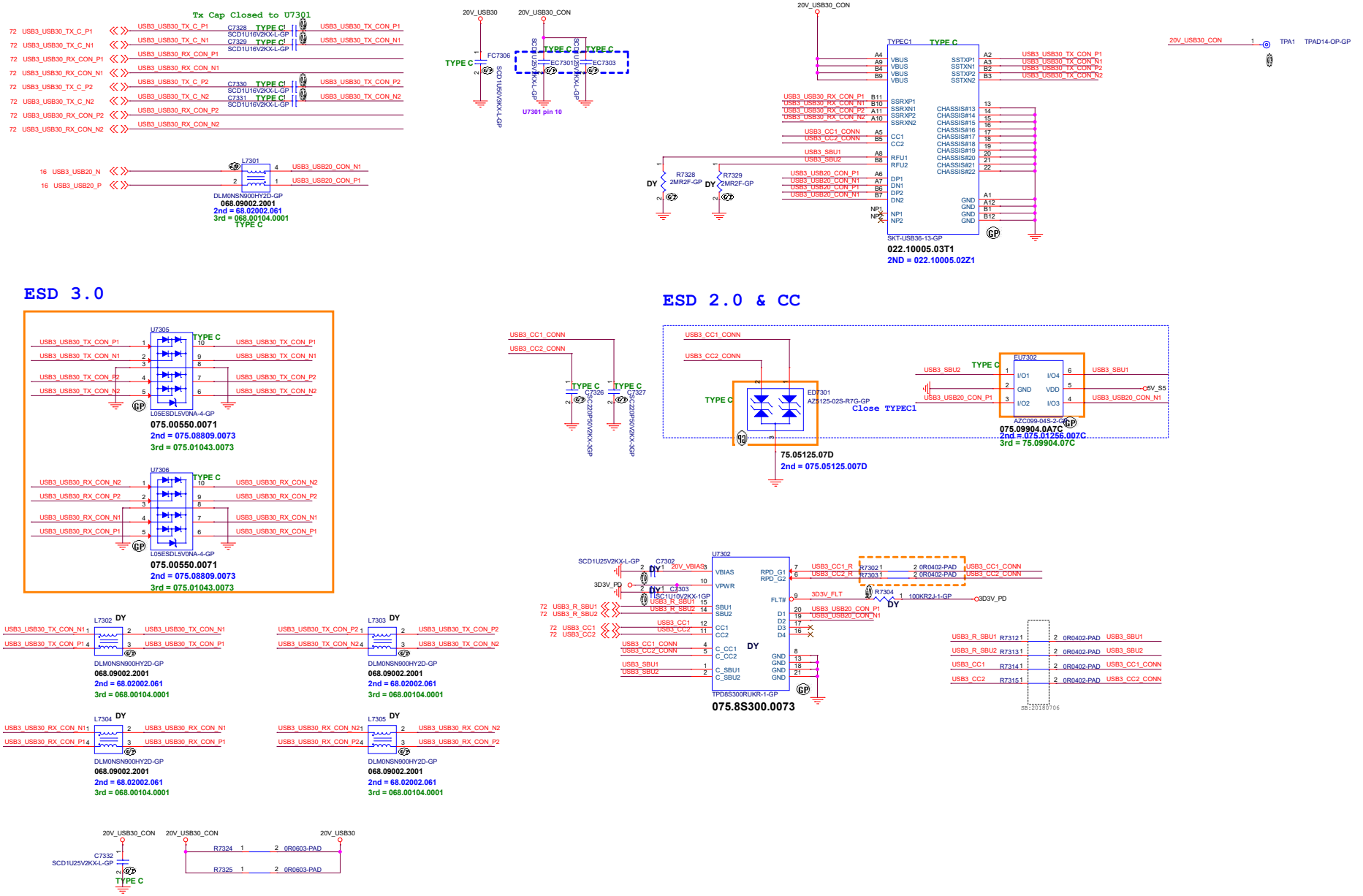
106



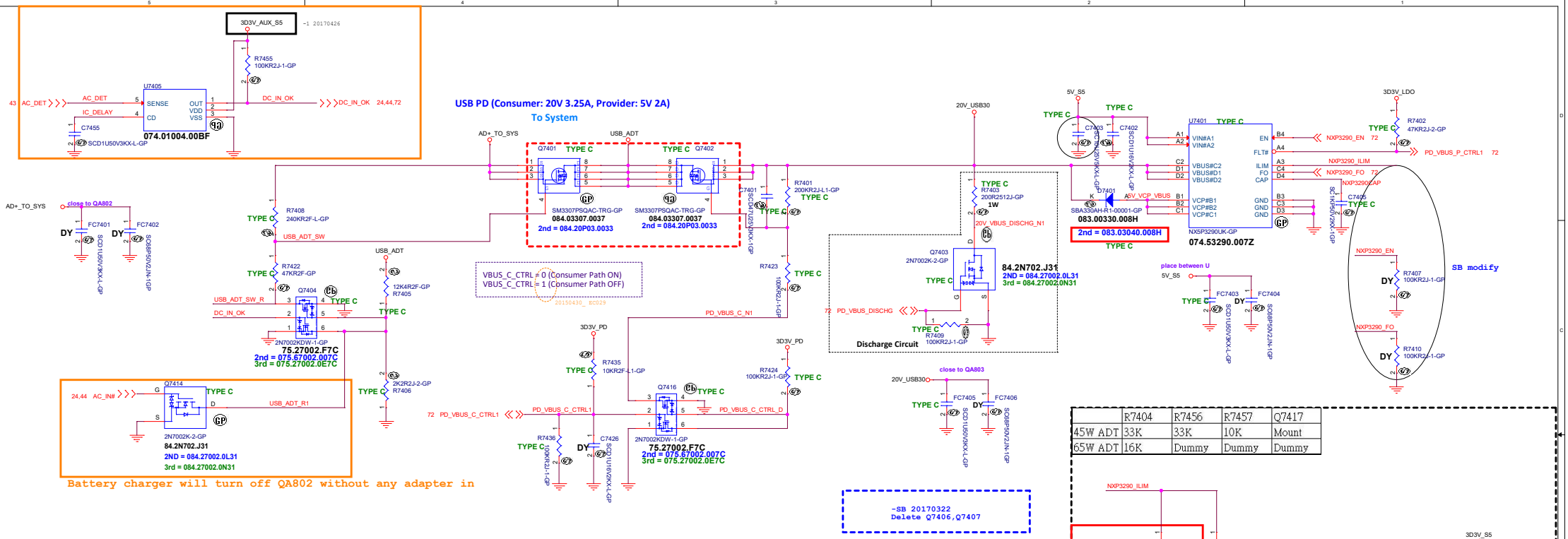
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

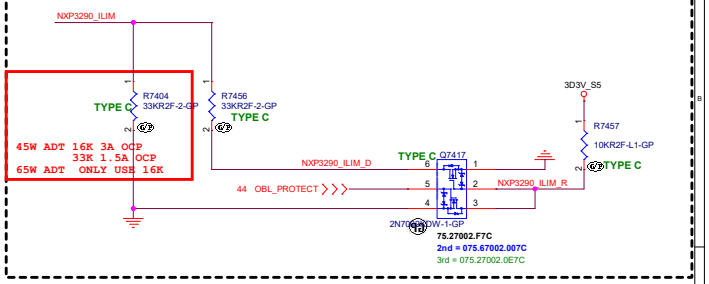
Title: TYPEC_RTS5450

Size: A2 | Document Number: Woody_WL/Slinky_WL | Rev: -1m

Date: Friday, September 07, 2018 | Sheet 73 of 106



	R7404	R7456	R7457	Q7417
45W ADT	33K	33K	10K	Mount
65W ADT	16K	Dummy	Dummy	Dummy



19V Power source type	Control Pin				PMOS Location	Status	Remark
	Net name	Status	Net name	Status			
Normal adapter Only	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	Control by DC_IN_OK
					Q7402	OFF	Control by PD_VBUS_C_CTRL1
					PU4401	ON	
					PU4402	OFF	
Type-C adapter Only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	Low	Q7401	ON	
					Q7402	ON	
					PU4401	OFF	
					PU4402	OFF	
Normal adapter + Type-C	DC_IN_OK	High	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	ON	
					PU4402	OFF	
Battery only	DC_IN_OK	Low	PD_VBUS_C_CTRL1	High	Q7401	OFF	
					Q7402	OFF	
					PU4401	OFF	
					PU4402	ON	Battery 放電到DCBATOUT

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Title: TYPEC_Control

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

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Title: ***Reserved***		
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
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Title: *GPU_PEG(Reserved)*

Size | Project Name: **Woody_WL/Slinky_WL** | Rev: -1m

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GPU_DIGITALOUT(Reserved)***	
Size A4	Document Number **Woody_WL/Slinky_WL**	Rev **-1m**
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Title: *Reserved*		
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Title	*GPU_GPIO/STRAP(Reserved)*	
Size	Project Name: **Woody_WL/Slinky_WL**	Rev: *-1m*
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Title	GPU_POWER/GND(Reserved)	
Size	Project Name: Woody_WL/Slinky_WL	Rev: -1m
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Title	***Reserved***	
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
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Title	*GPU-VRAM3,4(Reserved)*	
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Title	*GPU-VRAM5,6(Reserved)*	
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Title	GPU-VRAM7,8(Reserved)	
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Title	***VGA_CORE(Reserved)***
Size: A4	Document Number: **Woody_WL/Slinky_WL** Rev:
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Title	***DIS VGA POWER(Reserved)***
Size: A4	Document Number: **Woody_WL/Slinky_WL**
Rev: **-1m**	
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Title: *GFX_LCD(1/2)(Reserved)*

Size	Document Number	Rev
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Size A4	Document Number Woody_WL/Slinky_WL	Rev -1m
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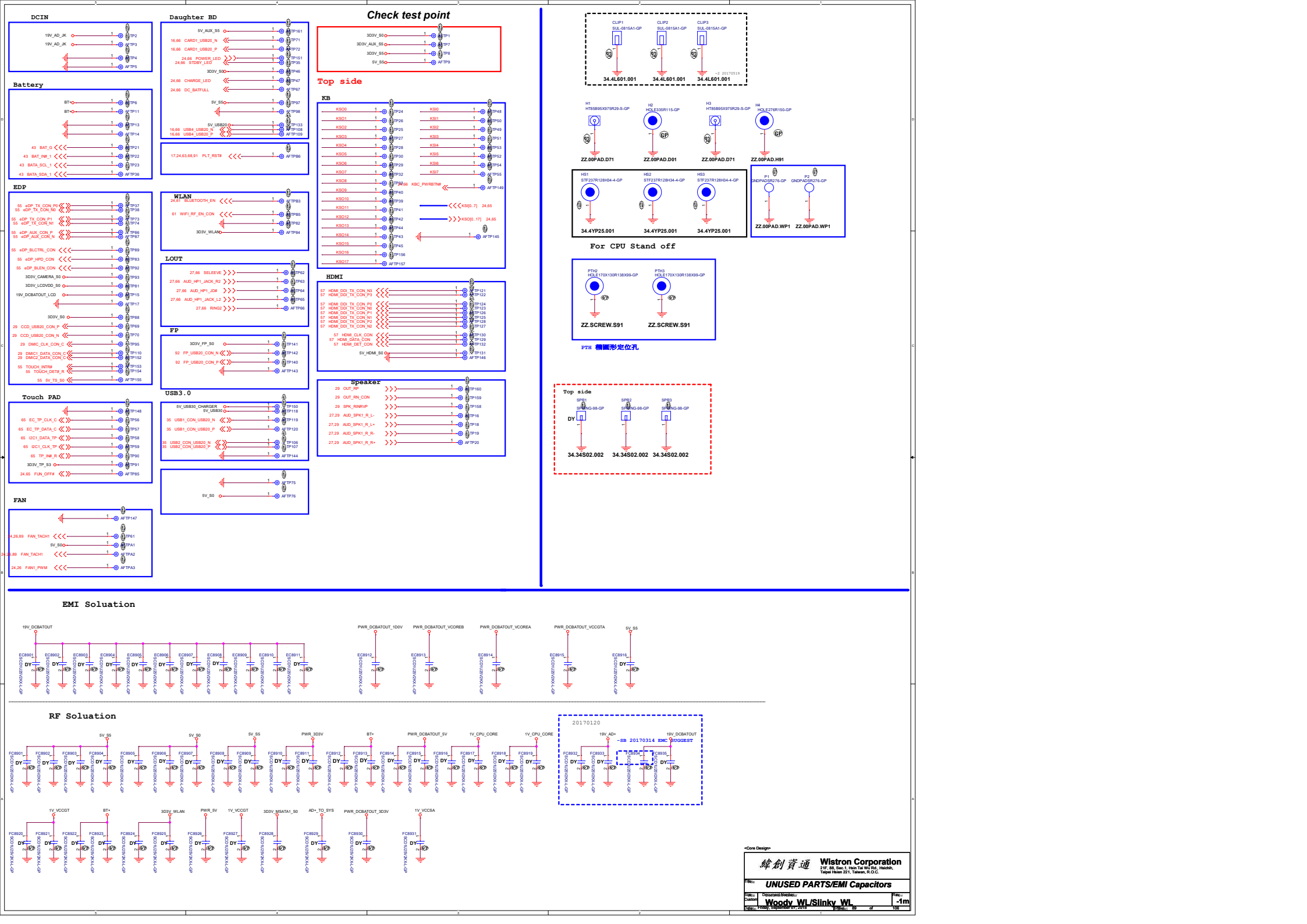
DCIN
Daughter BD
Check test point
Top side
Battery
KB
EDP
WLAN
LOUT
HDMI
FP
Speaker
Touch PAD
USB3.0
FAN
For CPU Stand off
PTH 橢圓形定位孔
EMI Soluation
RF Soluation
20170120
-SB 20170314 EMC SUGGEST
Wistron Corporation
UNUSED PARTS/EMI Capacitors
Woody_WL/Slinky_WL
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Title	***NFC(Reserved)***	
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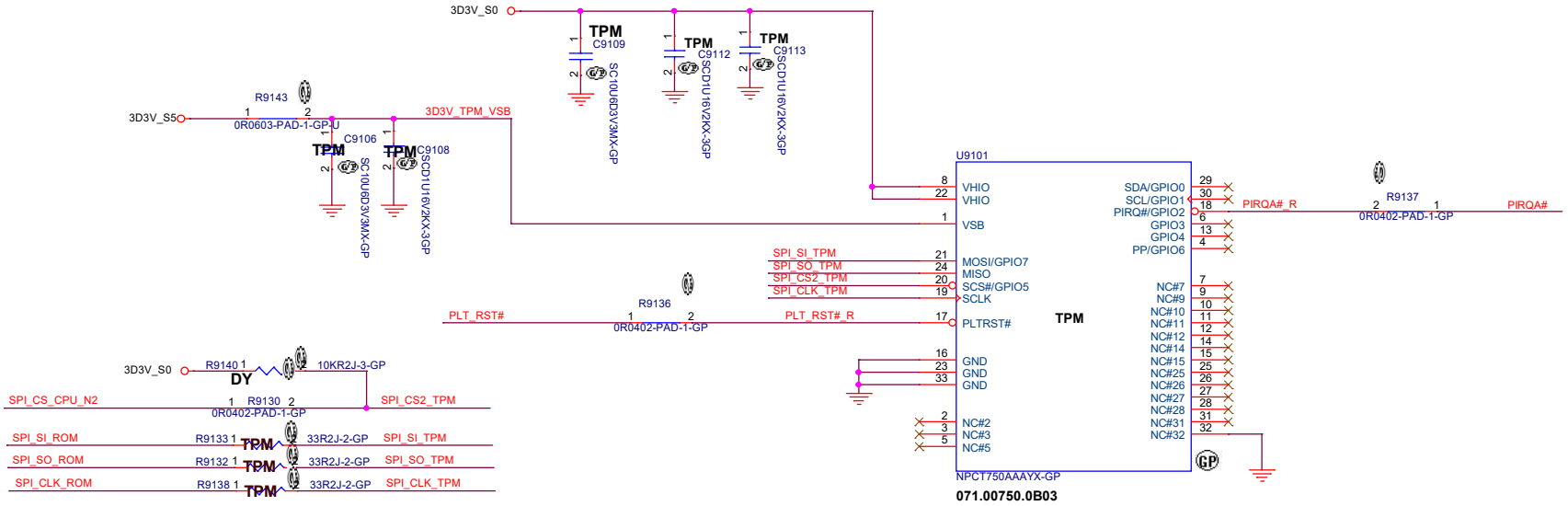
Main Func = TPM

20 PIRQA#
17,24,63,68,89 PLT_RST#
18 SPI_CS_CPU_N2
18,24,25 SPI_CLK_ROM
18,24,25 SPI_SO_ROM
15,18,24,25 SPI_SI_ROM



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Title: TPM2.0

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16 FP_USB20_N

16 FP_USB20_P

89 FP_USB20_CON_N

89 FP_USB20_CON_P

3D3V_S0 — 1 R9201 2 — 3D3V_FP_S0

0R0603-PAD

20170329 change

3D3V_FP_S0

FP_USB20_CON_P

FP_USB20_CON_N

FP1

10 8 7 6 5 4 3 2 1 9

FP

PTWO-CON8-17-GP

020.K0312.0008

2nd = 20.K0481.008

FP_USB20_P — R9202 1 2 0R0402-PAD — FP_USB20_CON_P

FP_USB20_N — R9203 1 2 0R0402-PAD — FP_USB20_CON_N

FP

EU9201

FP_USB20_CON_P 1 I/O1 — I/O4 6 FP_USB20_CON_N

2 GND — VDD 5 5V_S0

3 I/O2 — I/O3 4

AZC099-04S-2-GP

075.09904.0A7C

2nd = 075.01256.007C

3rd = 75.09904.07C

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Title: Finger Print		
Size: Custom	Document Number: Woody_WL/Slinky_WL	Rev: -1m
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Title	***Express_Card(Reserved)***	
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Title	***Smart Card scoket(Reserved)***	
Size: A	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
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Title	***GFX eDP(Reserved)***	
Size: A	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
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Title	***Bottom Docking(Reserved)***	
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Title	***Inter LAN WG1217LM(Reservrd)***	
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Title	***CPU_CFG STRAP(Reserved)***	
Size: A	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
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Title	***CPU_XDP(Reserved)***	
Size: A4	Document Number: **Woody_WL/Slinky_WL**	Rev: **-1m**
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Title	***table of content***	
Size A4	Document Number **Woody_WL/Slinky_WL**	Rev **-1m**
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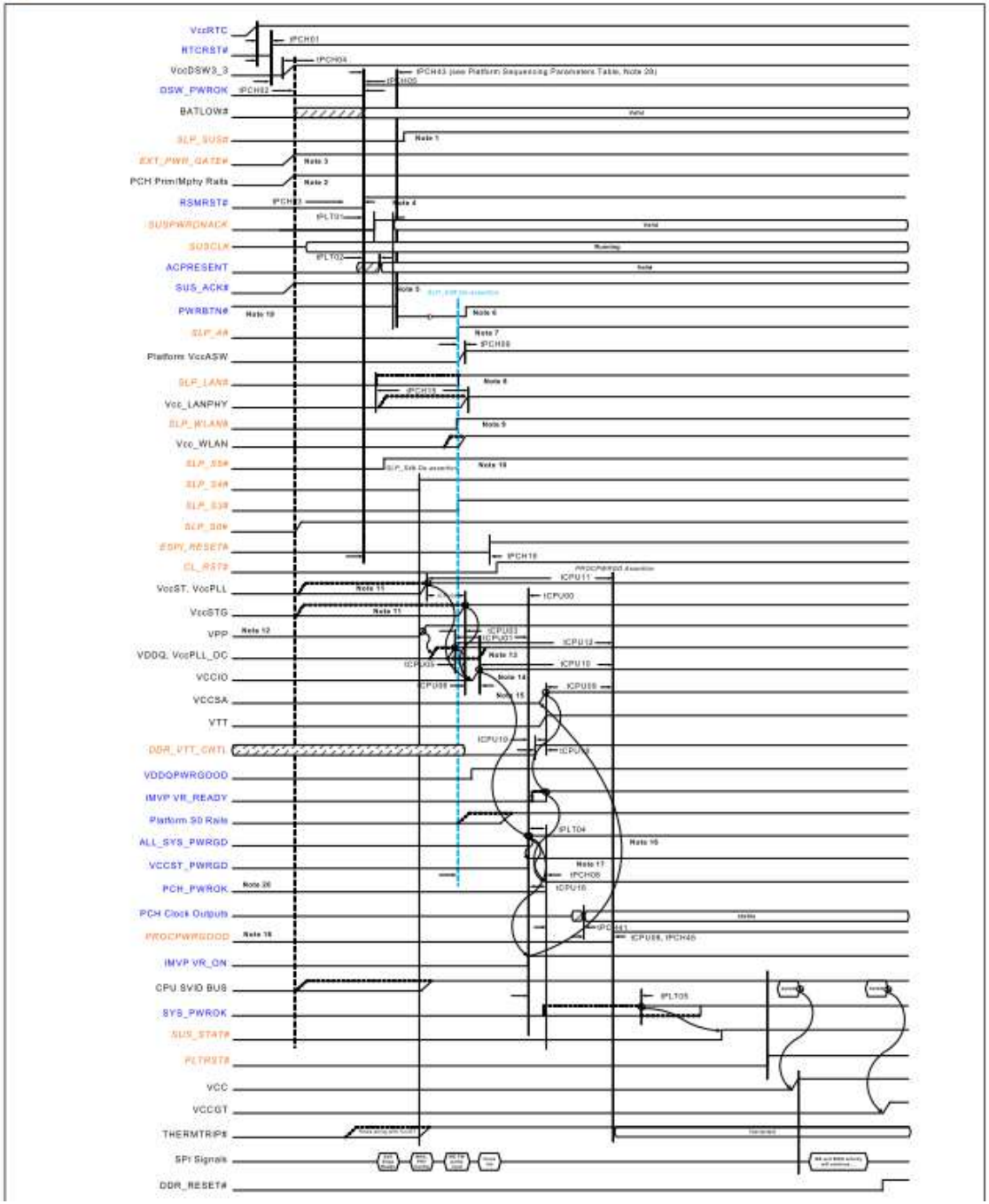
Figure 41-5. KBL R U Timing Diagram for G3 to S0/M0 [Non-Deep Sx Platform] (Sheet 1 of 2)



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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Change History*		
Size: A4	Document Number: Woody_WL/Slinky_WL	Rev: -1m
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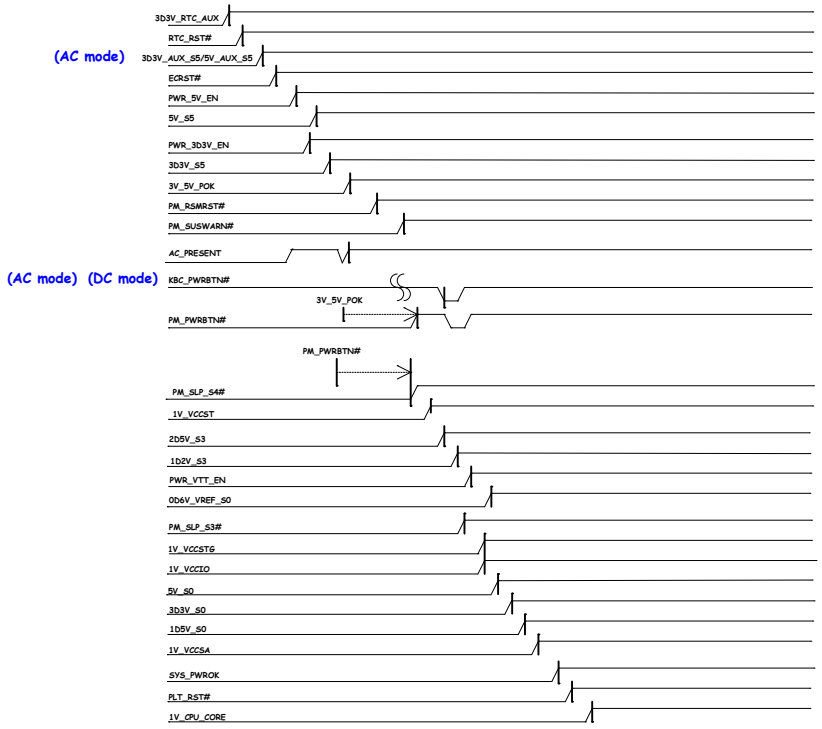
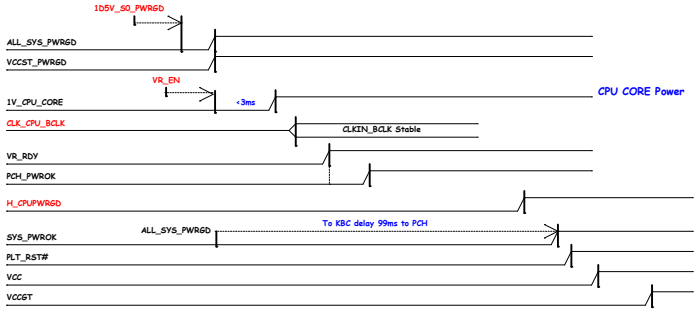
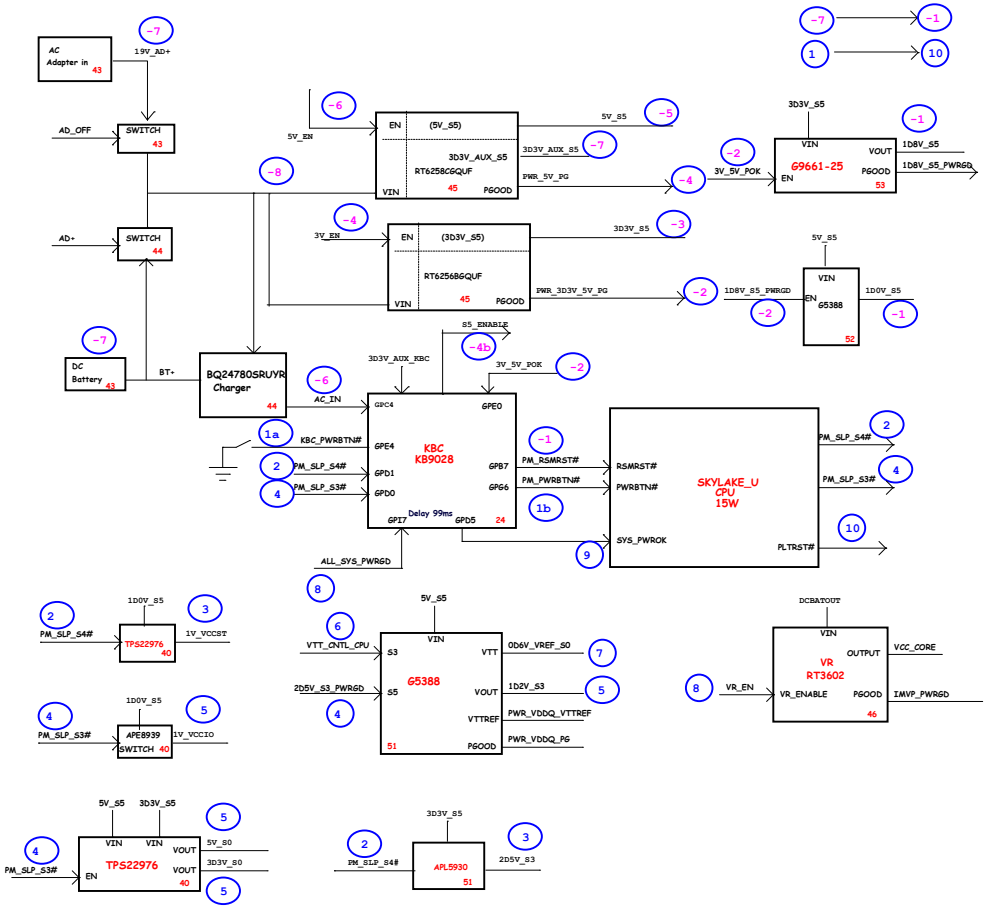
Intel-Power Up Sequence







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Title: Power Sequence

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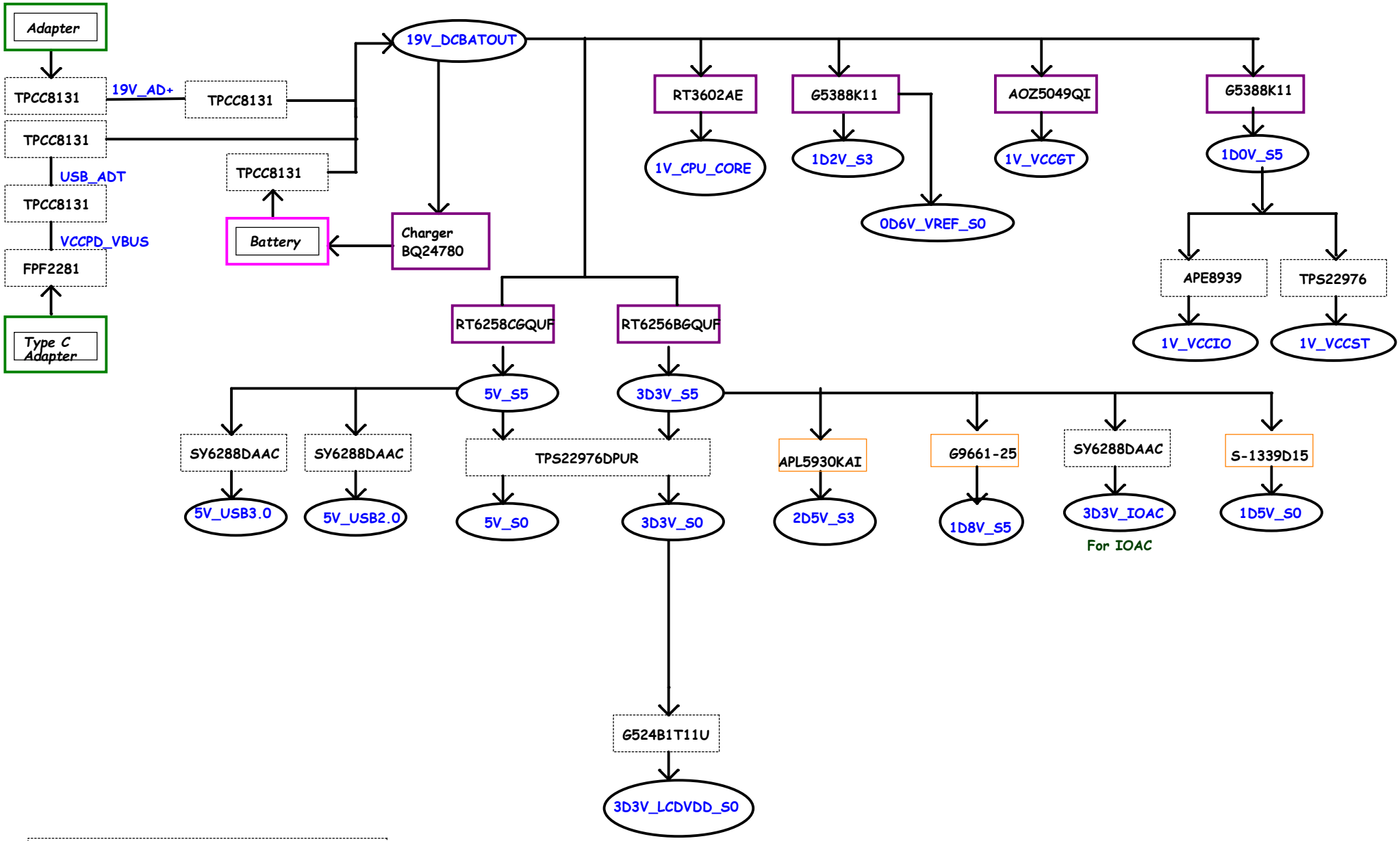

Power Shape

Regulator | LDO | Switch

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Title: Power Block Diagram

Size: A3 | Document Number: Woody_WL/Slinky_WL | Rev: -1m

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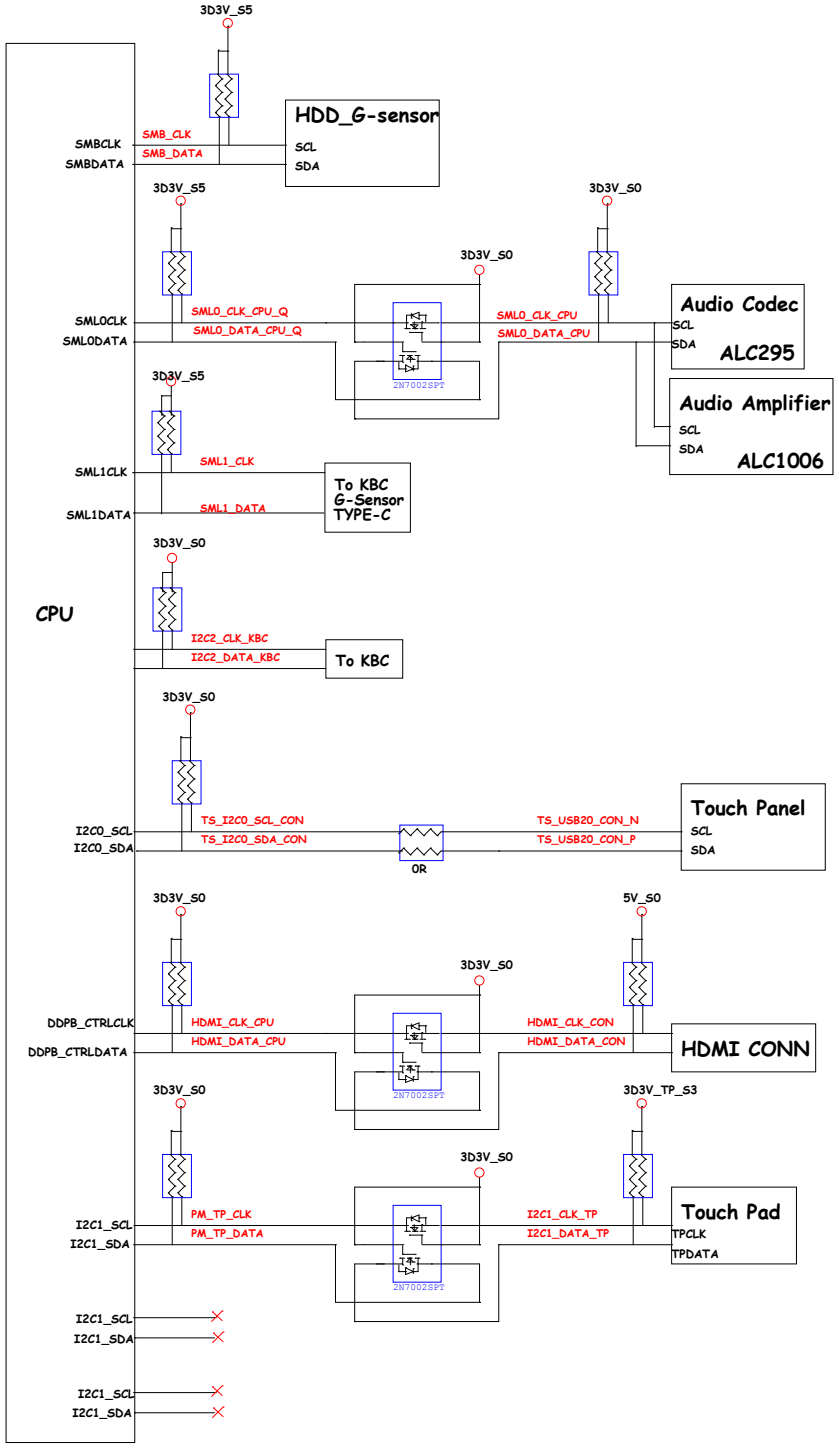
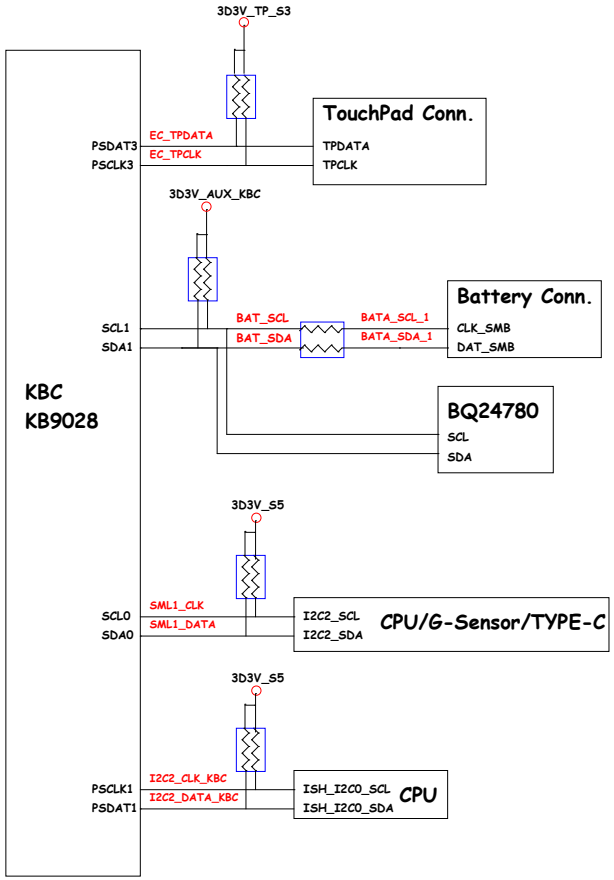
PCH SMBus/I2C Block Diagram



KBC SMBus/I2C Block Diagram



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Title: SMBUS BLOCK DIAGRAM

Size	Document Number	Rev
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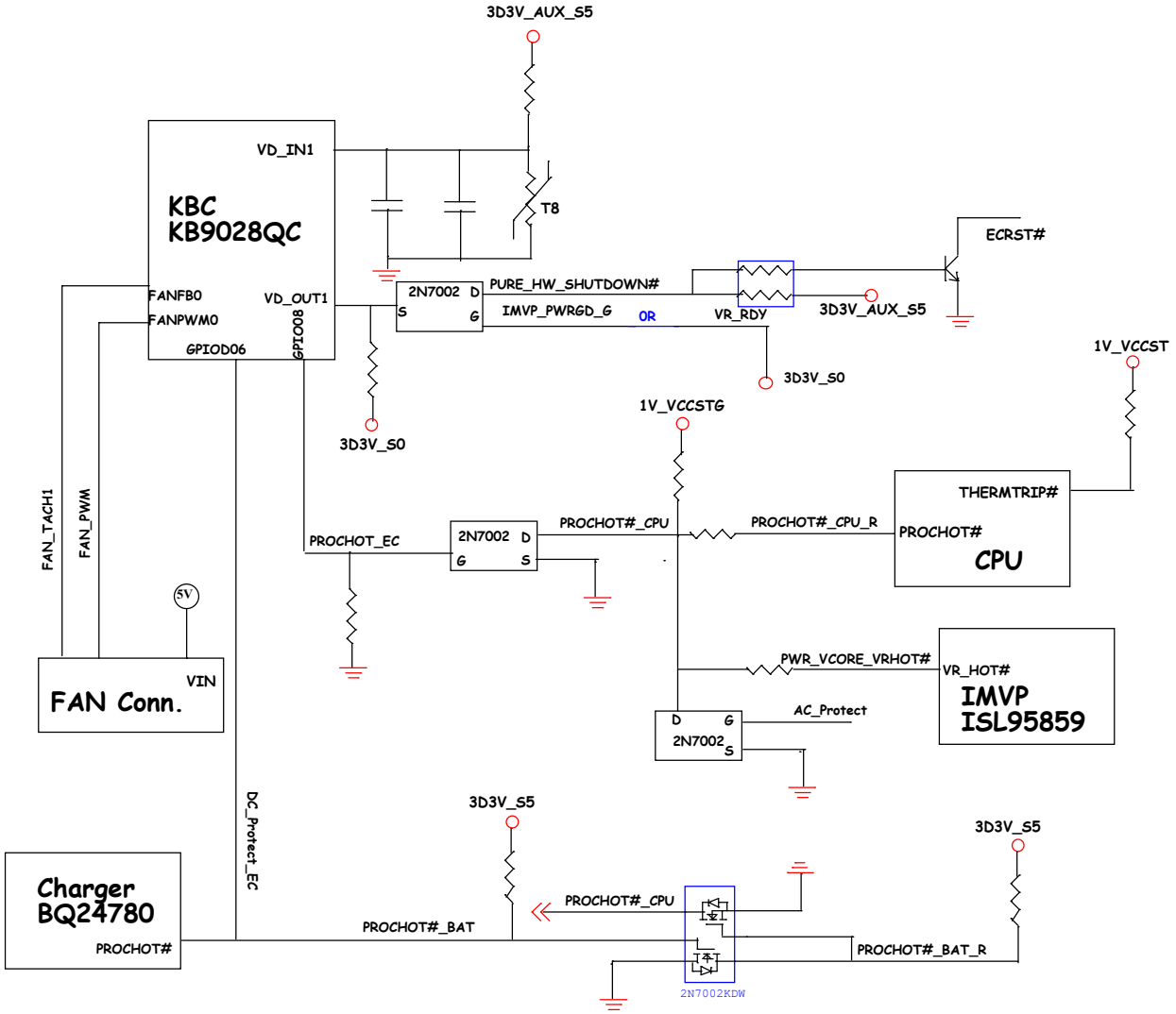
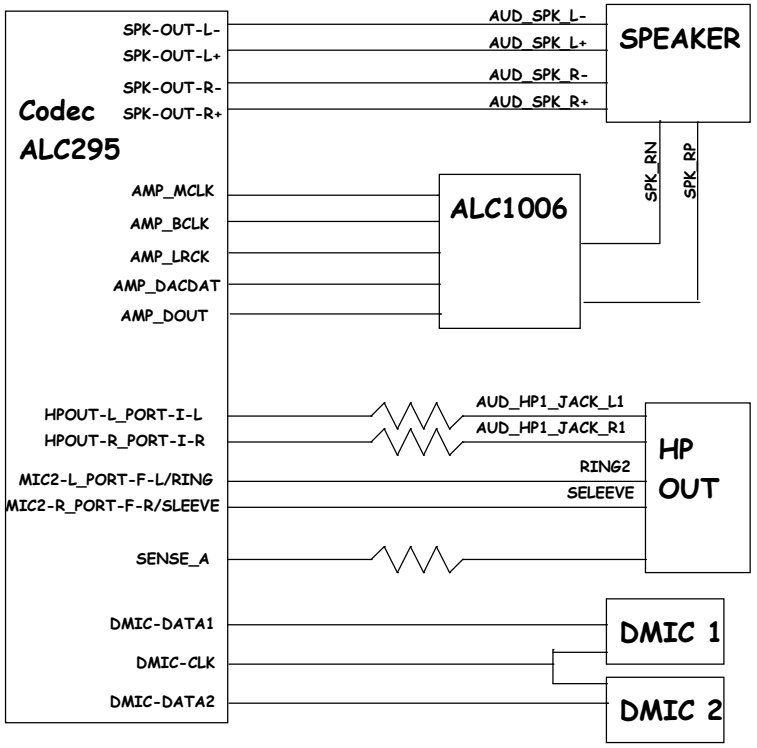
Thermal Block Diagram



Audio Block Diagram



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Title: THERMAL/AUDIO BLOCK DIAGRAM

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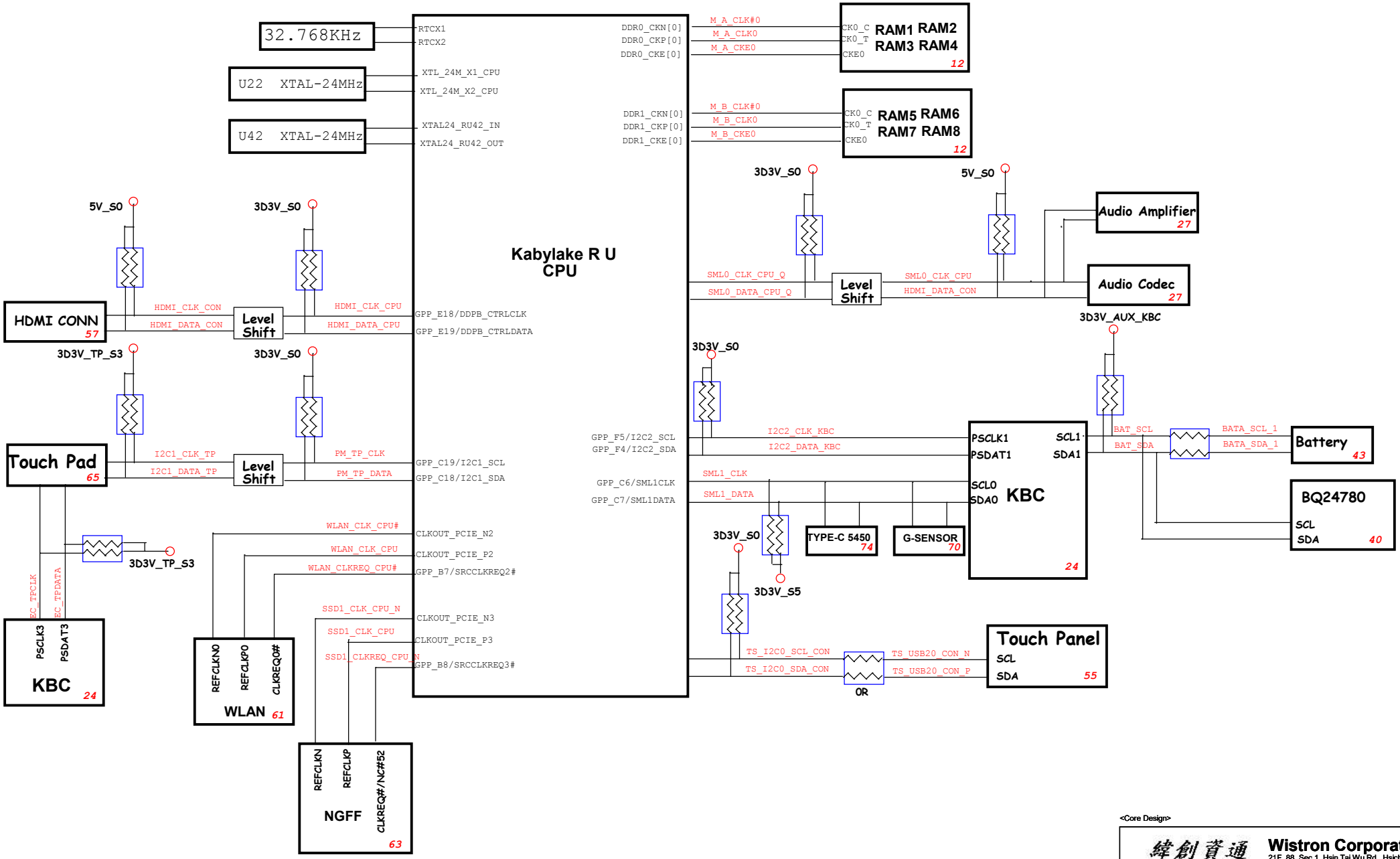
CLOCK BLOCK DIAGRAM



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Title: CLK Block

Size: Custom | Document Number: Woody_WL/Slinky_WL | Rev: -1m

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