

QingDao_Int

CPU : Intel Penryn
Chip Set : Intel Cantiga & ICH9M
Remarks : Montevina Platform

Model Name : QingDao_Int
PBA Name : MAIN
PCB Code : BA41-01084A NANYA
BA41-01085A HANNST
BA41-01086A GCE
Dev. Step : ADV
Revision : 1.0
T.R. Date : 2009.02.13

Design	CHECK	APPROVAL
XIAOHONG ZHANG	RUJIN ZHENG	BC LEE

Owner : SESC Mobile R & D Signature : X

BLOCK DESIGN

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Mobile Processor
Penryn-6M
FSB 1067
478pin
L2 Cache : 6/3MB
FSB 667/800 MT/S

MCH-M
Cantiga-GM
GM47
1299 FCBGA

ICH9-M
676 BGA

ON BOARD
CPU DC/DC IMVP-6
Charging Circuit
Smart Battery Module
DC/DC

Termination
VCCP / DC-DC
DDR II SODIMM 0
DDR II SODIMM 1
DDR II Power

Channel A (Standard) DDR II 667/800
Dual channel
Channel B (Reverse) DDR II 667/800

HDMI
LCD
CRT

Clocking
CK-505

FAN
CPU Thermistor (TBD)

Direct Media Interface
x4, 1.5V
CLINK

USB 0,2,6
USB 5
USB 8
Camera
HD Primary
HD Secondary
SPI
SATA 0
SATA 1
SATA 4
eSATA

Audio
ALC272
High Definition Audio
Aud. AMP
INT MIC
HP MIC-IN
SPKR R
SPKR L

8057
RJ45
Mini Card (WLAN)
Express Card
3 IN 1 AU6336
SD(SDHC)
MMC

MICOM
H8S-2110B
TMKBC (TBD)
Touch PAD
KBD

80 Port
LED

3.3V LPC, 33MHz

DESIGN SUN XIAO
CHECK WU SHIJIANG
APPROVAL BC LEE
MODULE CODE

DATE 2/13/2009
DEV. STEP PV
REV 1.0

TITLE QING DAO INT
MAIN
BLOCK DIAGRAM

SAMSUNG
ELECTRONICS
PART NO. BA41-XXXXX

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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
CPU_CORE	Core Voltage for CPU
EGFX_CORE	Core Voltage for GPU
P1.05V	VTT for CPU, Cantiga & ICH9-M
P1.1	VTT for N10M_GE1
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail
P12.0V_ALW	12.0V always power rail

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	Intel LAN

I²C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 0010	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	Mini PCI Express
2	SYSTEM PORT 1
3	NC
4	3 IN 1
5	Bluetooth
6	SYSTEM PORT 2
7	EXPRESS CARD
8	Camera
9	NC
10	NC

PCI Express Assign

PORT #	ASSIGNED TO
1	Mini Card 1 (WLAN)
2	NC
3	EXPRESS CARD
4	LOM
5	NC
6	NC

LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0(strap0)
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REVISION HISTORY

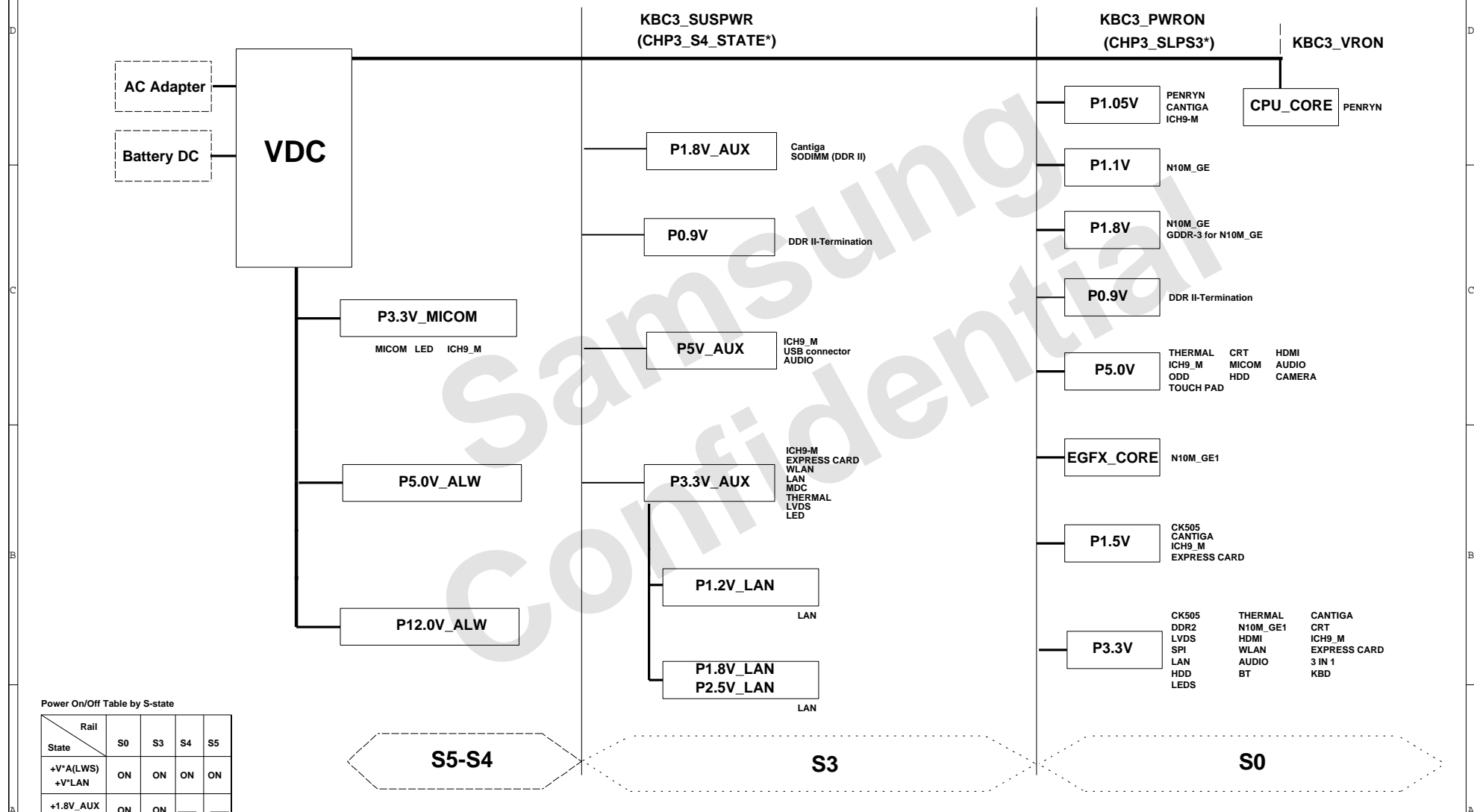
See rev notes for more information.

DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV	MAIN		
APPROVAL	BC LEE	REV	1.0	BOARD INFO	PART NO. BA41-XXXXXX	
MODULE CODE		LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	3 OF 13	

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POWER DIAGRAM

Rev 0.1



Power On/Off Table by S-state

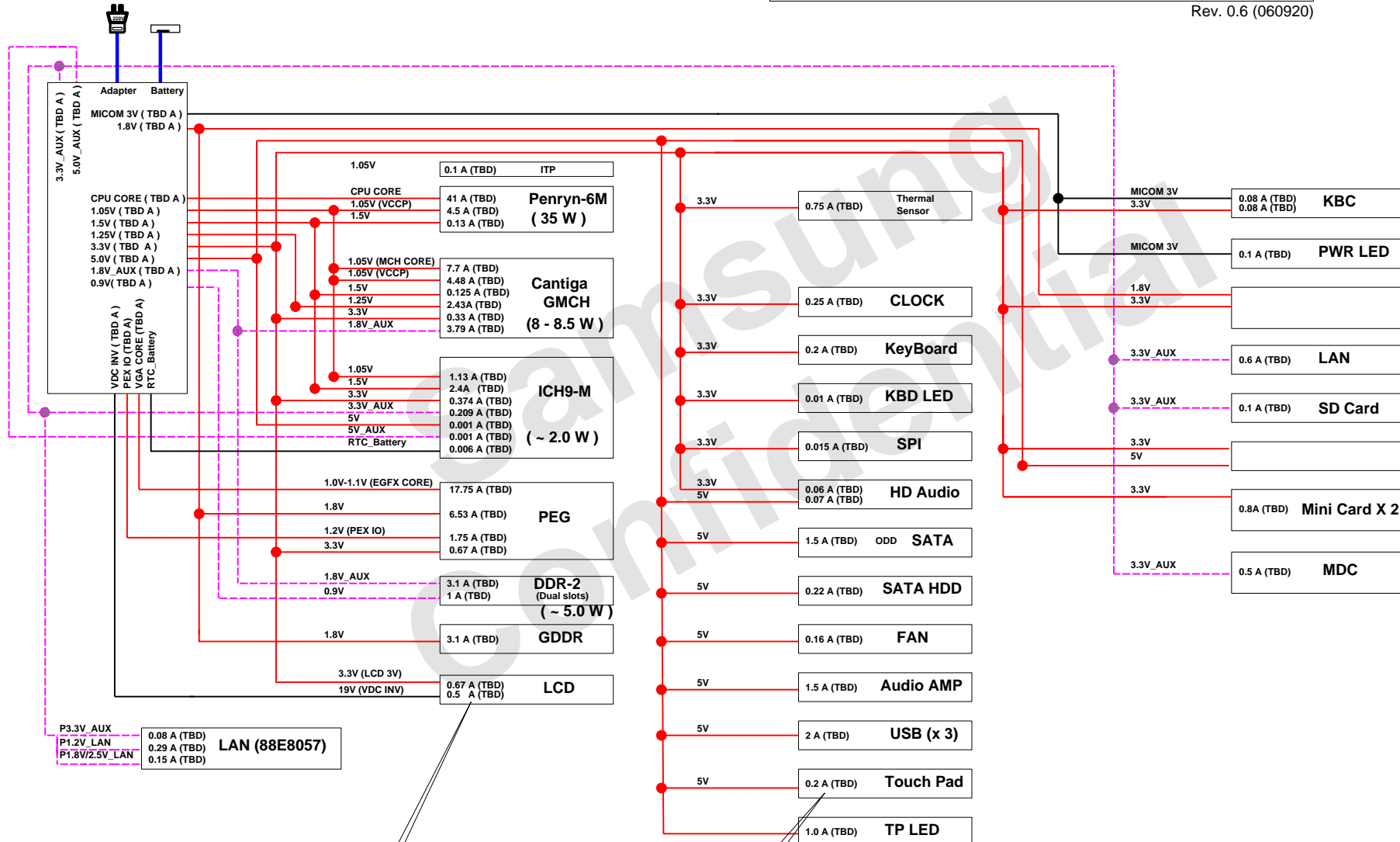
Rail State	S0	S3	S4	S5
+V*A(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	—	—
+V*AUX	ON	ON	—	—
+V	ON	—	—	—
+V* (CORE)	ON	—	—	—

DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT MAIN POWER DIAGRAM	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV	REV	1.0	PART NO. BA41-XXXXXX
APPROVAL	BC LEE	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	4	OF 13
MODULE CODE						

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POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT MAIN POWER RAILS	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			PART NO. BA41-XXXXXX
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT		March 25, 2009 10:15:14 AM	PAGE 5 OF 13	

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Host Boot / ME Off

(SLPS4* = S4_STATE*) > (SLPM* = SLPS3*)

M-1) KBC3_DDR_PWRON (TBD) = 8) KBC3_SUSPWR

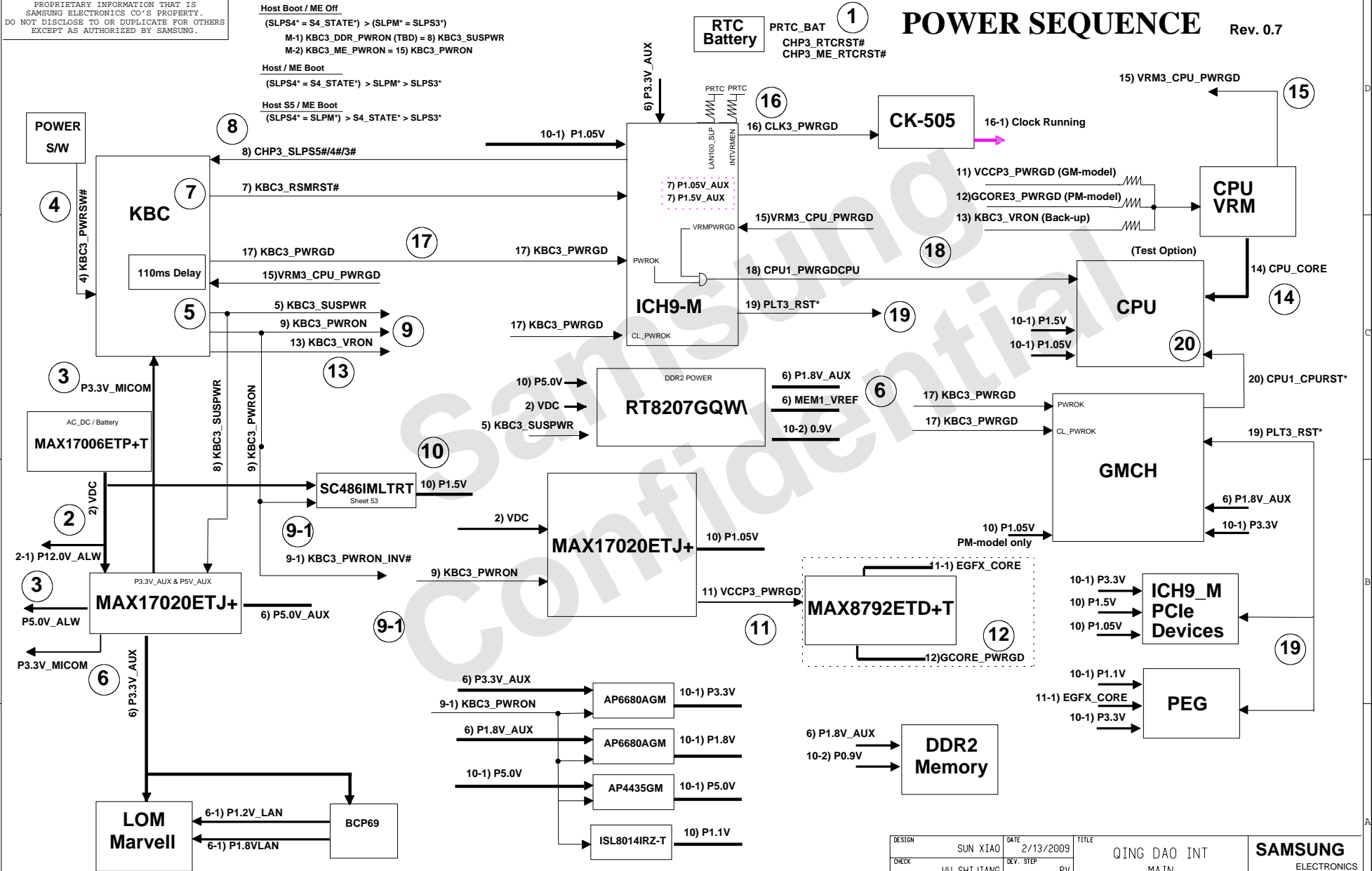
M-2) KBC3_ME_PWRON = 15) KBC3_PWRON

Host / ME Boot

(SLPS4* = S4_STATE*) > SLPM* > SLPS3*

Host S5 / ME Boot

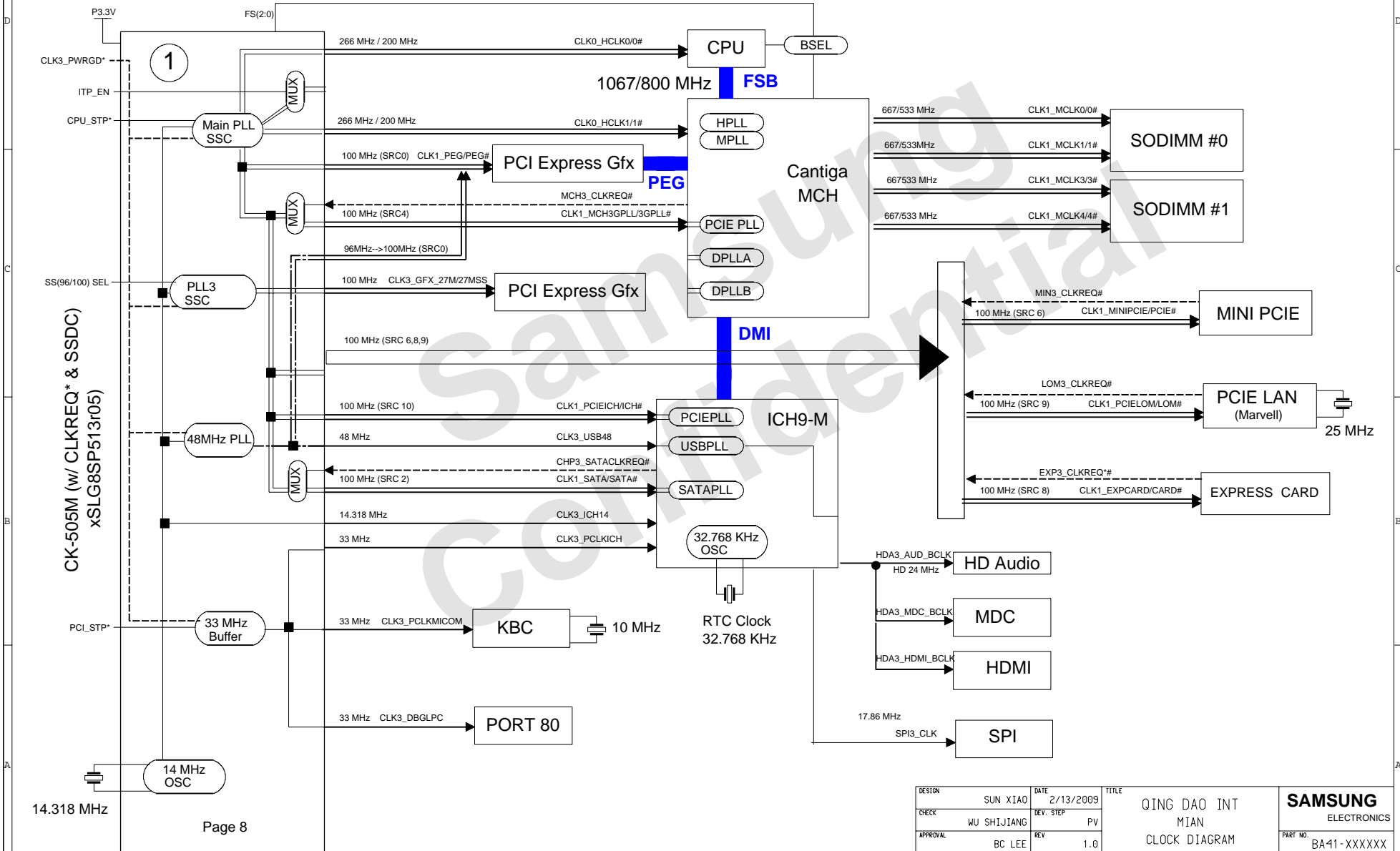
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*



DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT MAIN POWER SEQUENCE	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			PART NO. BA41-XXXXXX
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT				
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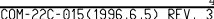
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CLOCK DISTRIBUTION Rev. 0.1

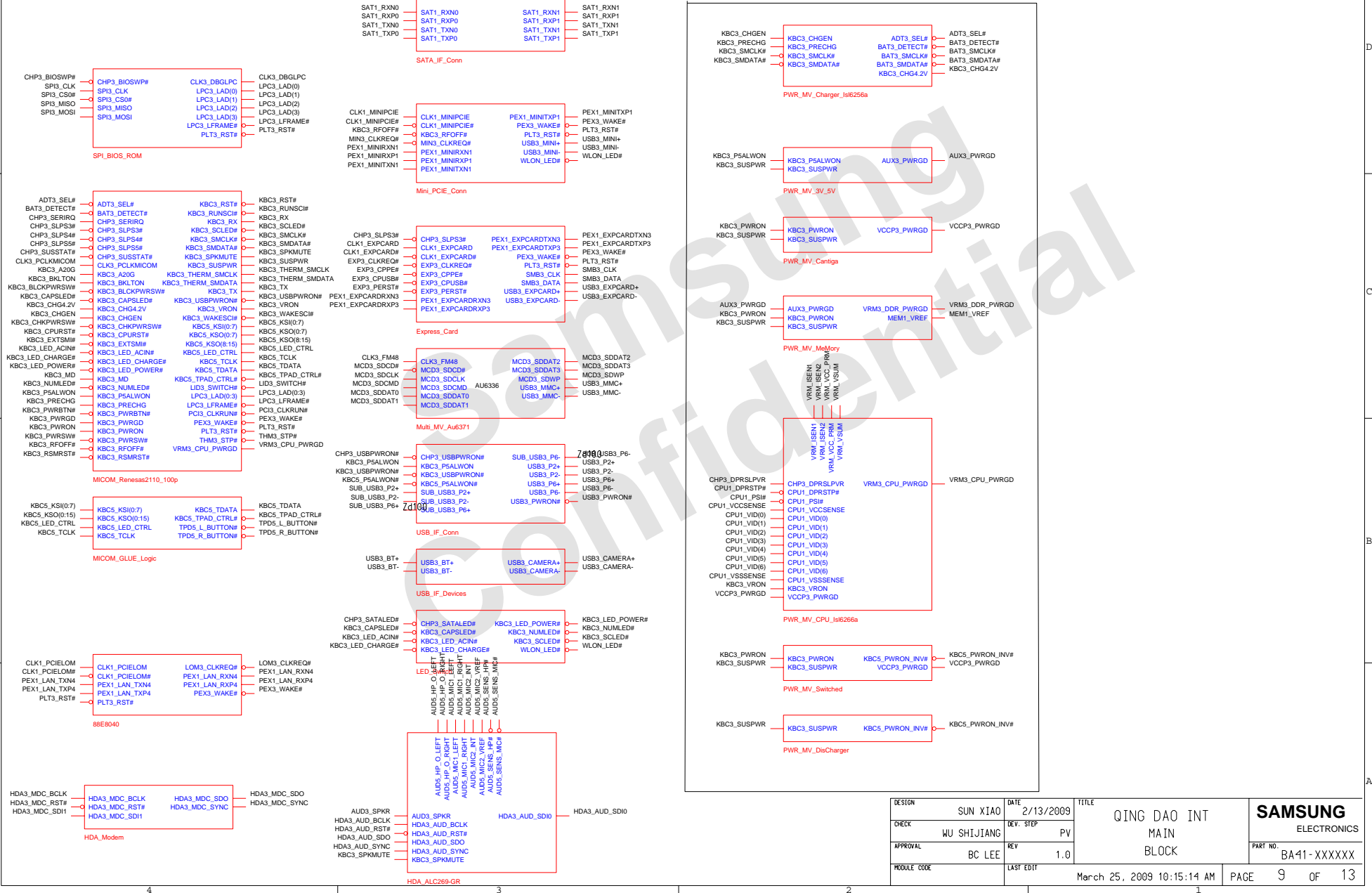


DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT MIAN CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			PART NO. BA41-XXXXXX
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	7	OF 13

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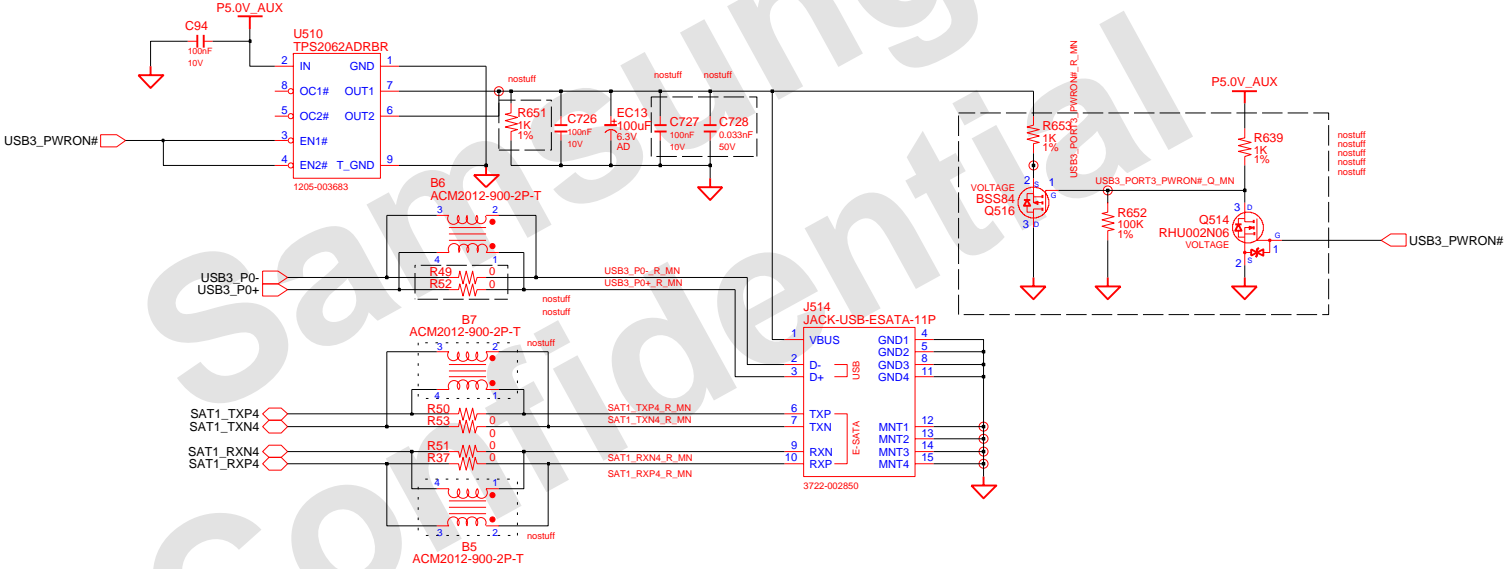
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DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
CHECK	WU SHIJIANG	DEV. STEP	PV	MAIN	BLOCK	
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT		March 25, 2009 10:15:14 AM	PAGE 9 OF 13	

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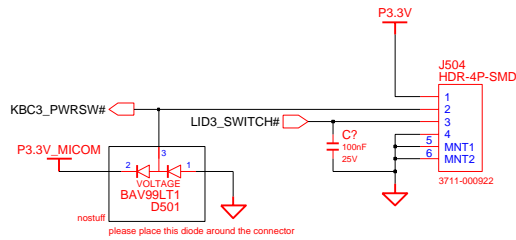
ESATA FUNCTION



DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
CHECK	WU SHIJIANG	DEV. STEP	PV		MAIN	
APPROVAL	BC LEE	REV	1.0		eSATA	
MODULE CODE		LAST EDIT				
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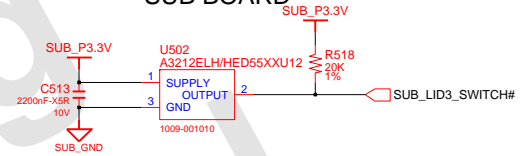
MAIN BOARD



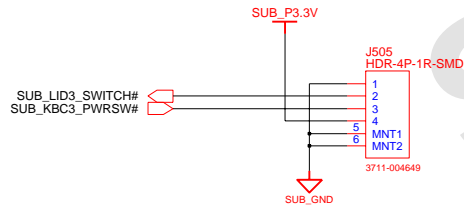
Power LED SUB BOARD



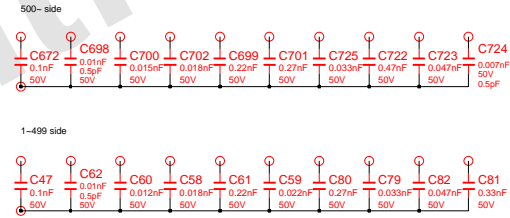
LID_SWITCH SUB BOARD



SUB BOARD



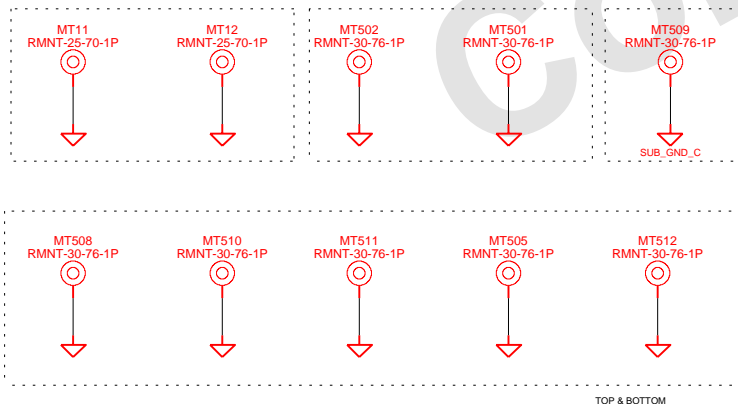
Power Switch SUB BOARD



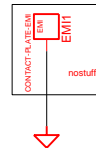
PCB & BOTTOM

KBD & BOTTOM

USB_SUB & BOTTOM



USB S/B MT



REV1
1 O
2 O O3

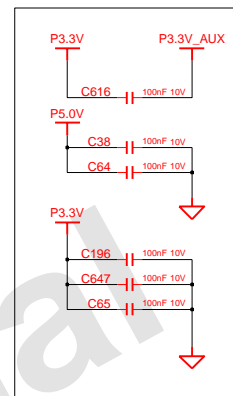
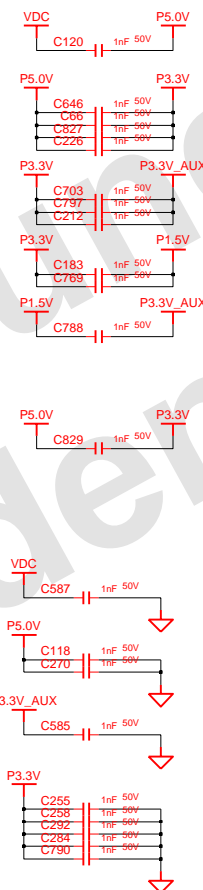
PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV		MAIN	
APPROVAL	BC LEE	REV	1.0		PWR SW SUB	PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT		March 25, 2009 10:15:14 AM	PAGE 12 OF 13	

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☐ KBC3_THERM_SM

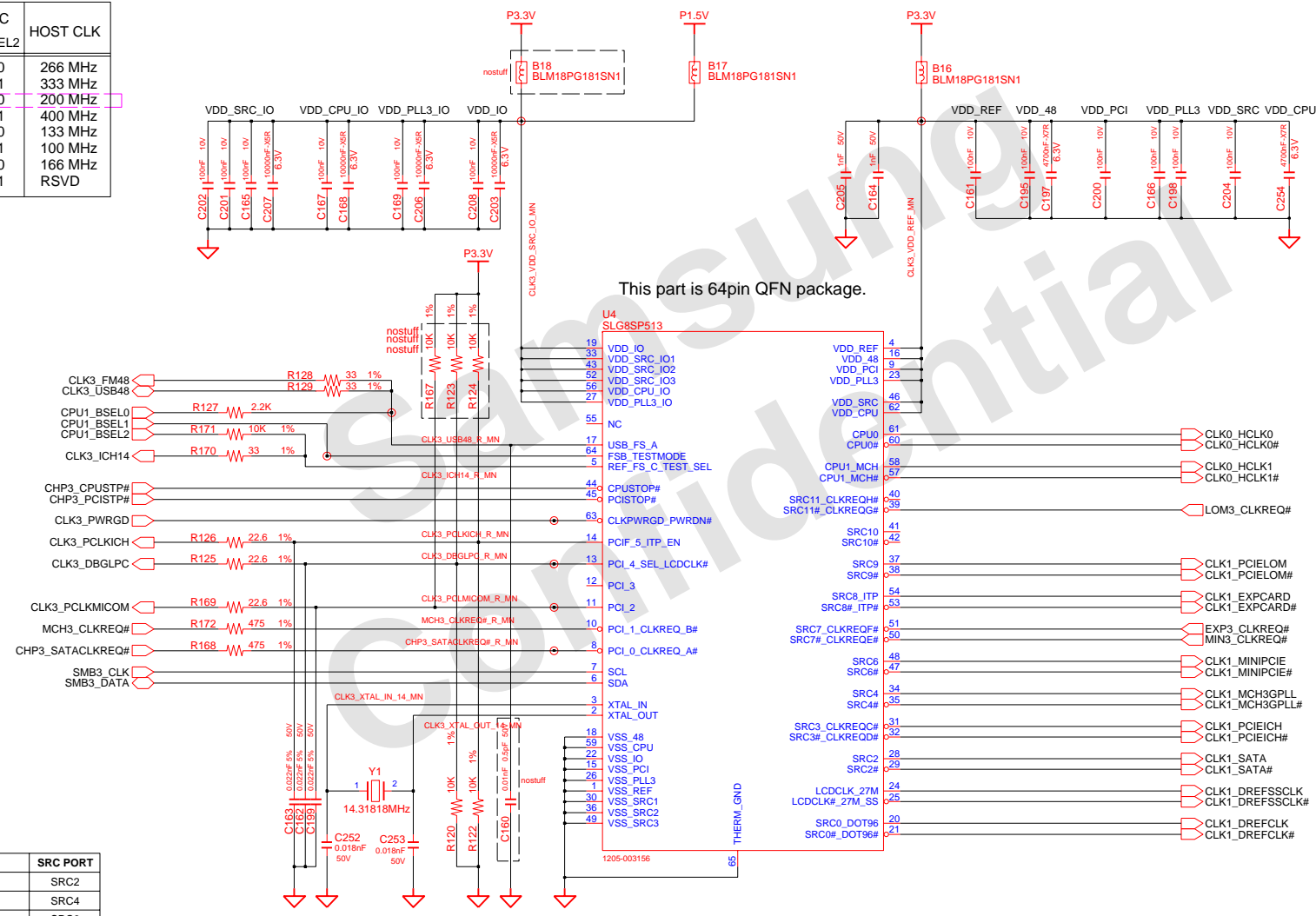
○P5.0V_AUX



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CK505M

FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



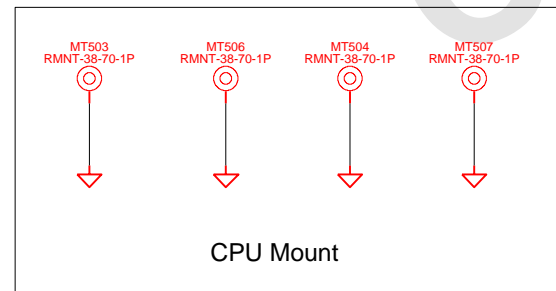
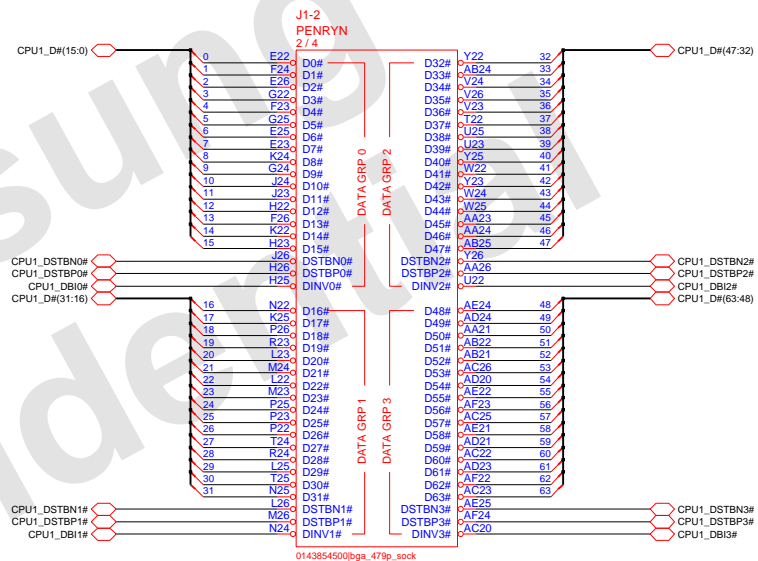
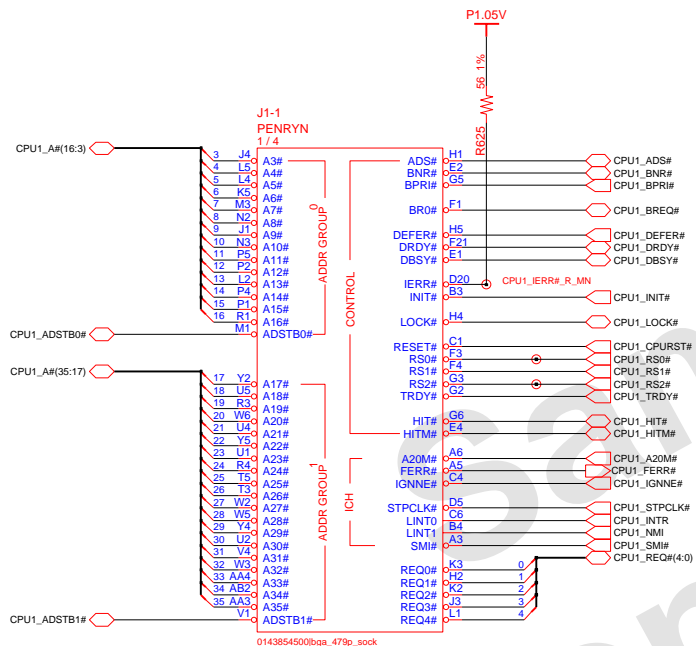
CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

Place 14.318MHz within 500mils of CK-505

DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
CHECK	WU SHIJIANG	DEV. STEP	PV	Main_Clock_Circuit		
APPROVAL	BC LEE	REV	1.0	CK_Clock_505M		
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE 1 OF 1		

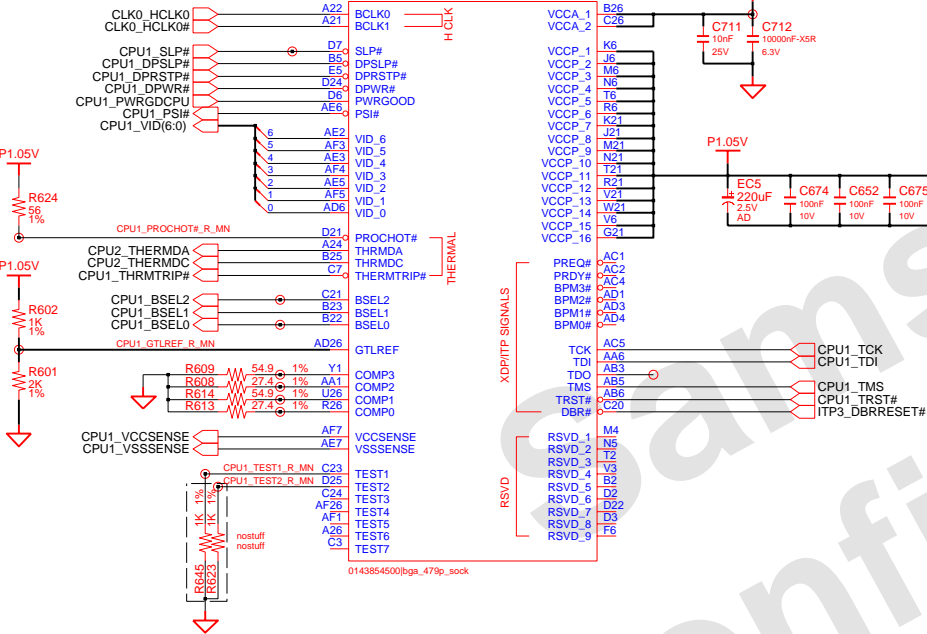
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DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT CPU PENRYN (1/3)	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
CHECK	WU SHIJIANG	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	1 OF 3	

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J1-3
PENRYN
3 / 4



CPU Core Voltage Table IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 1 0 0	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 1	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 1 0 0	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 1	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 1 0 0 0		1 0 0 1 1 0 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V
				**1111111*: 0V power good asserted.	
Active		Deeper Slp			
DPRSLPVR	0	DPRSLPVR	1		
DPRSTP*	1	DPRSTP*	0		
PSI2*	0 or 1	PSI2*	0 or 1		

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5°
of the first GTLREF0 pin with Zo=55ohm trace.
Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm)
trace shorter than 1/2" to their respective Banias socket pins.

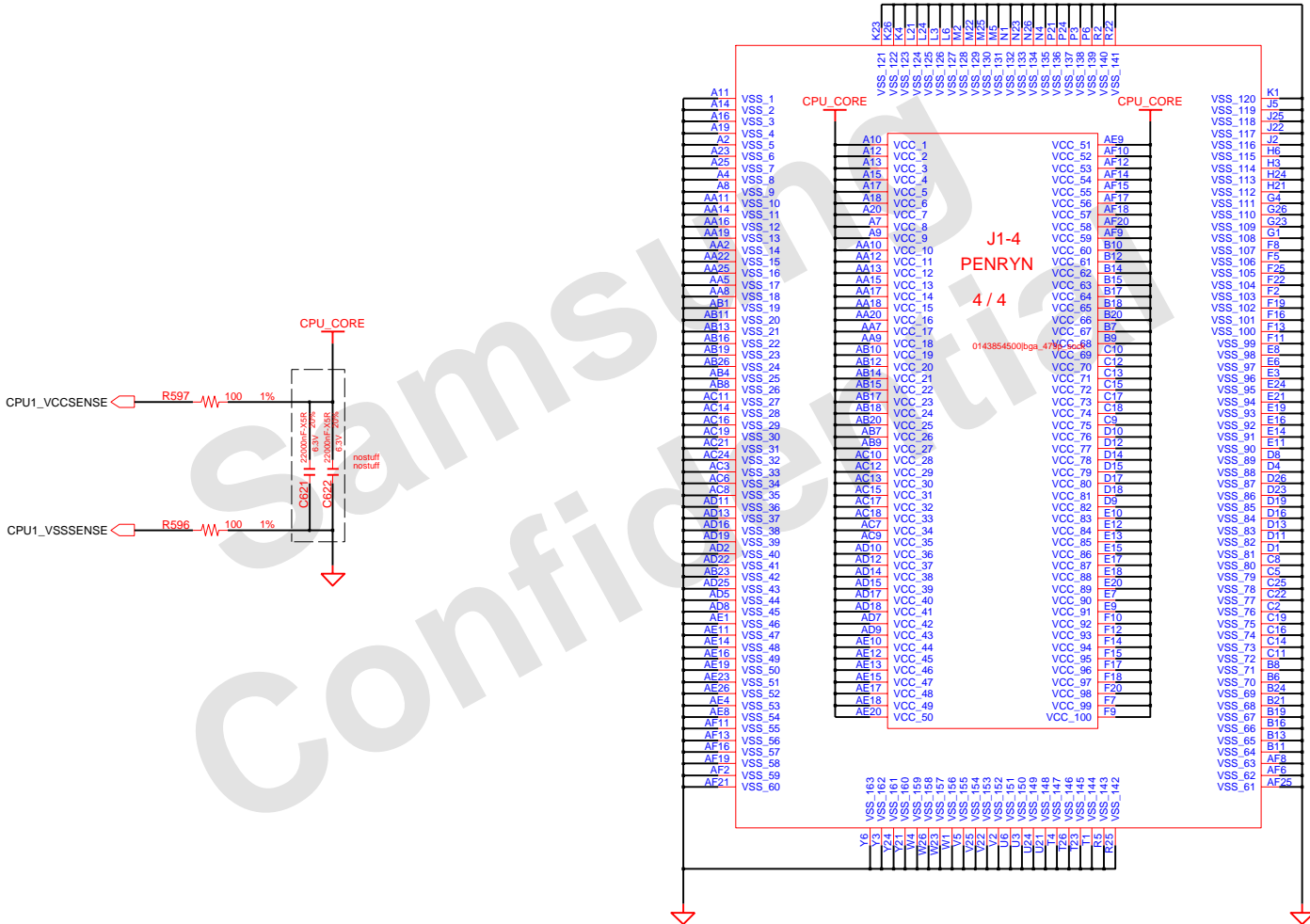
GND test points within 100mil of the VCC/VSSsense at the end of the line.
Route the VCC/VSSsense as a Zo=55ohm traces with equal length.
Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away
(preferred 50mil) from any other signal. And GND via 100mil away
from each of the VCC/VSS test point vias.

BSEL

FSB 1067 MHz		Pull-down
FSB 800 MHz		BSEL0, BSEL1, BSEL2
		BSEL0, BSEL2

DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV		CPU	
APPROVAL	BC LEE	REV	1.0		PENRYN (2/3)	PART NO. BA41-XXXXXX
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	2	OF 3

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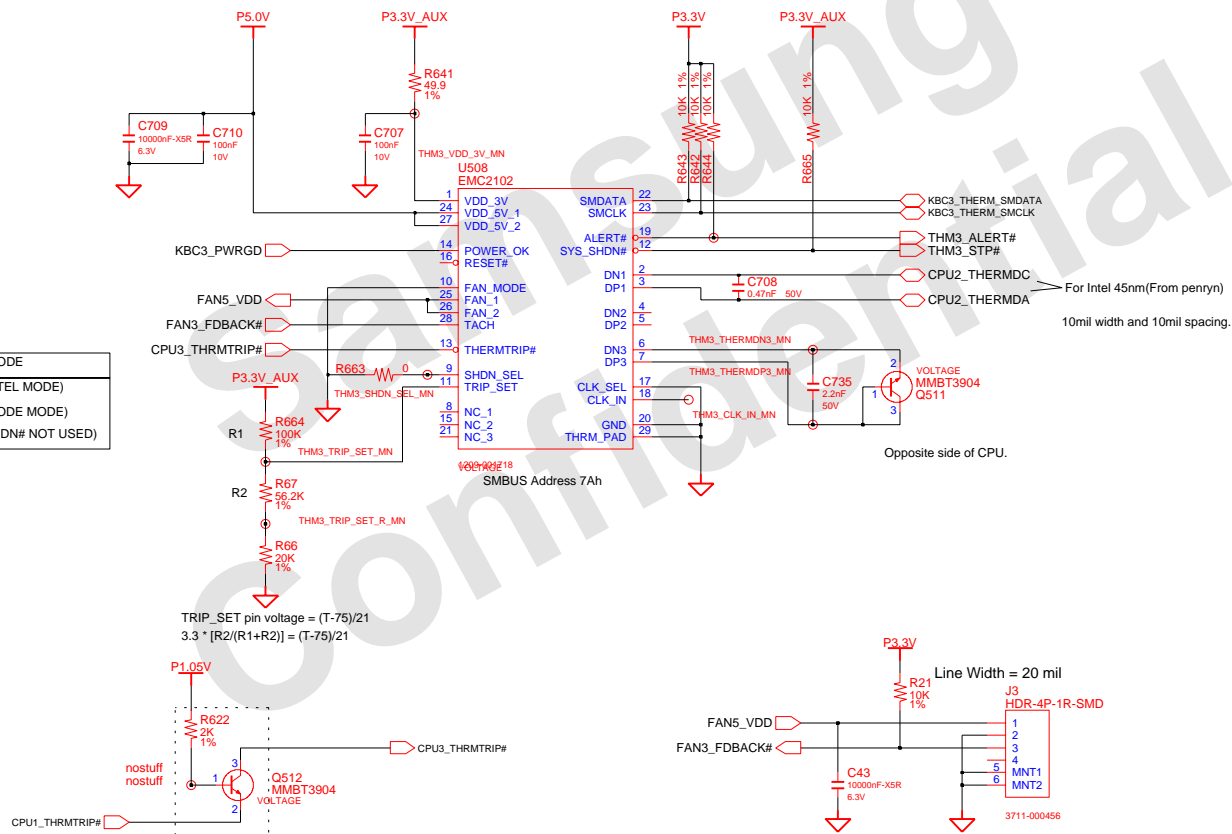


DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT CPU PENRYN (3/3)	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			PART NO. BA41-XXXXXX
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	3 OF 3	

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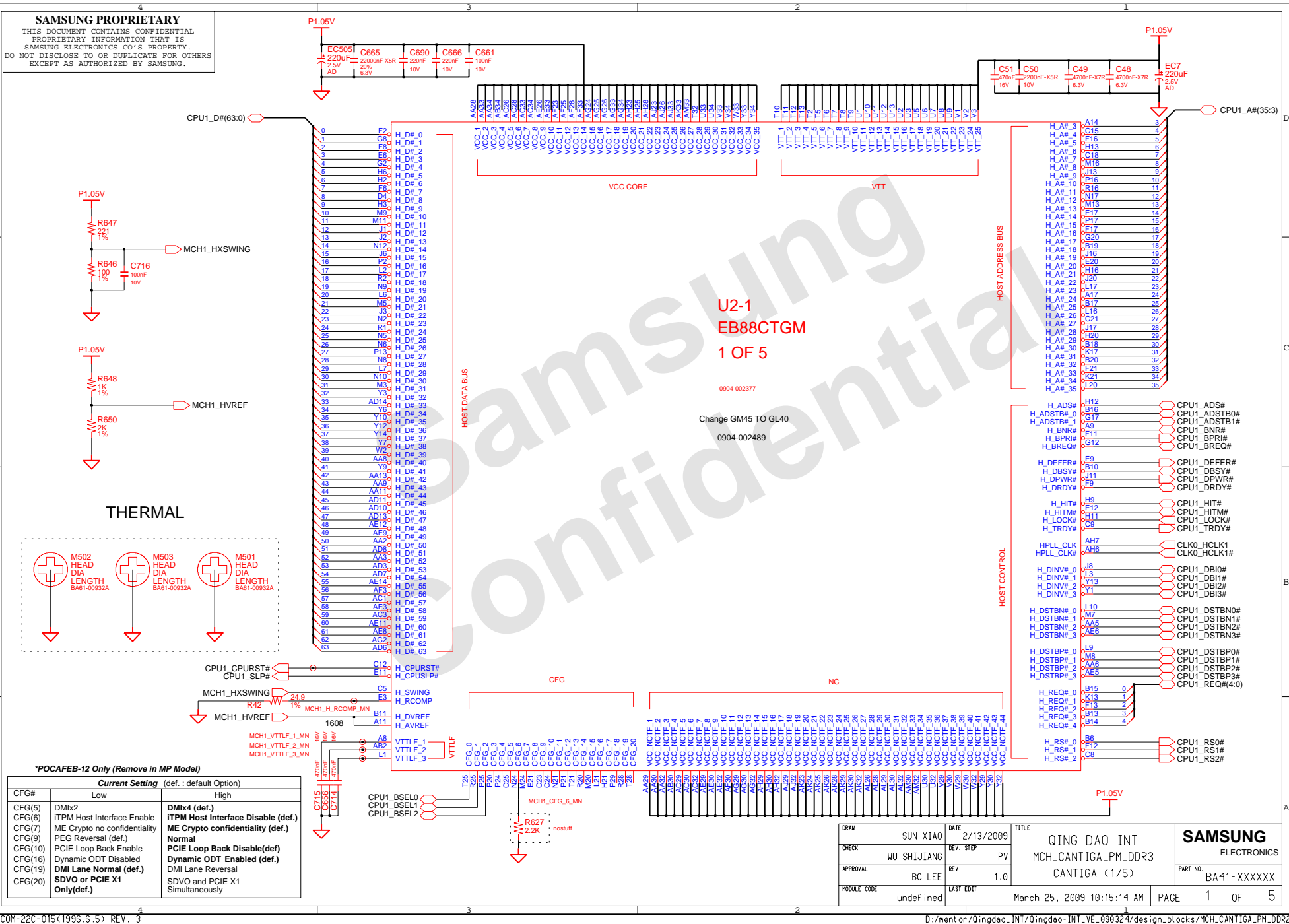
THERMAL SENSOR & FAN CONTROL

SHDN_SEL MODE	
0	CH1(INTEL MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)



DESIGN	XIAOHONG, ZHANG	DATE	12/3/2008	TITLE	QingDao_Ext	SAMSUNG ELECTRONICS
CHECK	RUJIN, ZHENG	DEV. STEP	ADV1		THERMAL SENSOR EMC2102	
APPROVAL	BC, LEE	REV	1.0			PART NO.
MODULE CODE		LAST EDIT	December, 3, 2008 12:55:11 PM	PAGE	1 OF 1	BA41-xxxxxA

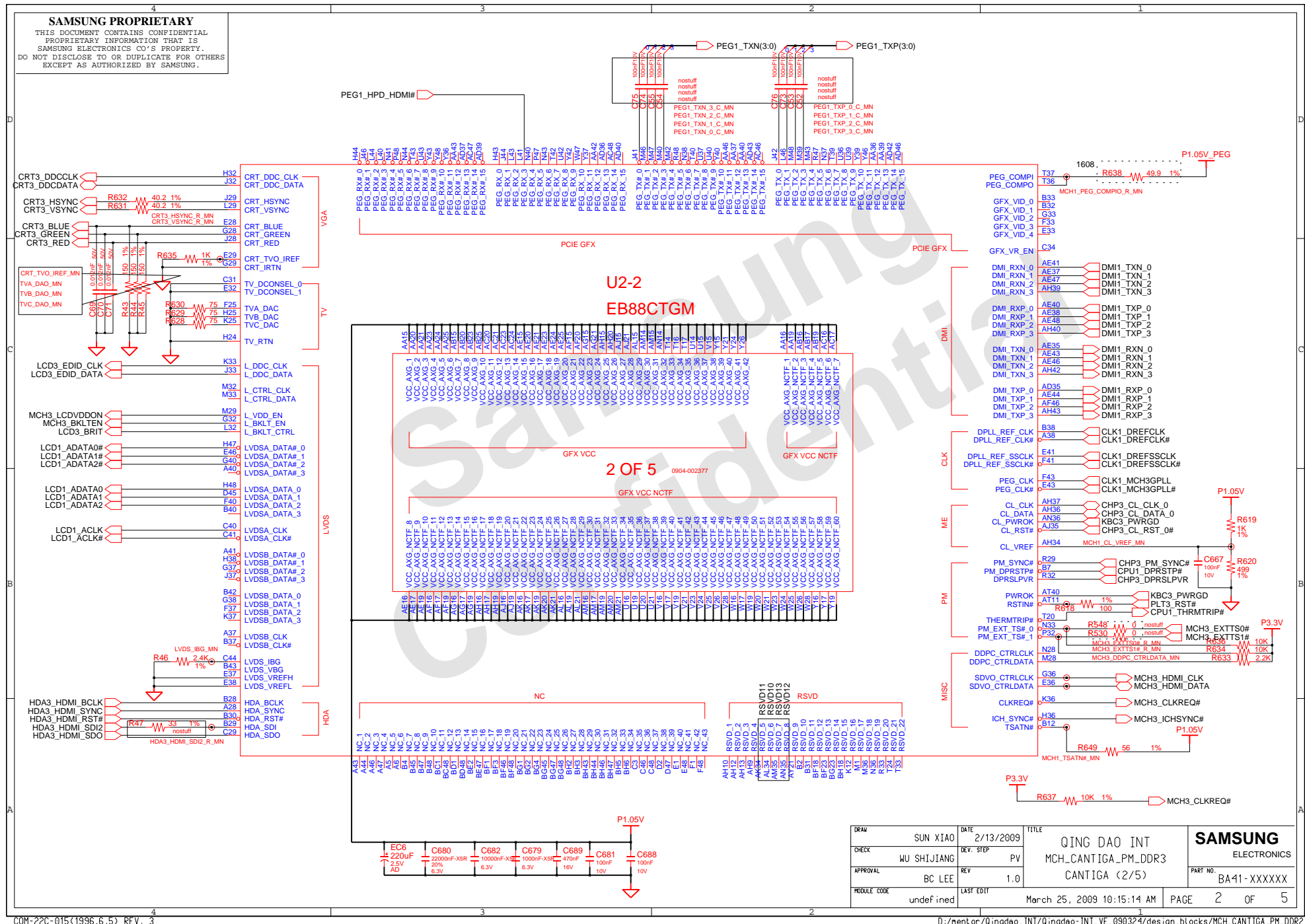
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DATE	SUN XIAO	2/13/2009	TITLE	QING DAO INT
CHECK	WU SHIJIANG	PV	MCH_CANTIGA_PM_DDR3	
APPROVAL	BC LEE	REV	1.0	CANTIGA (1/5)
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE 1 OF 5

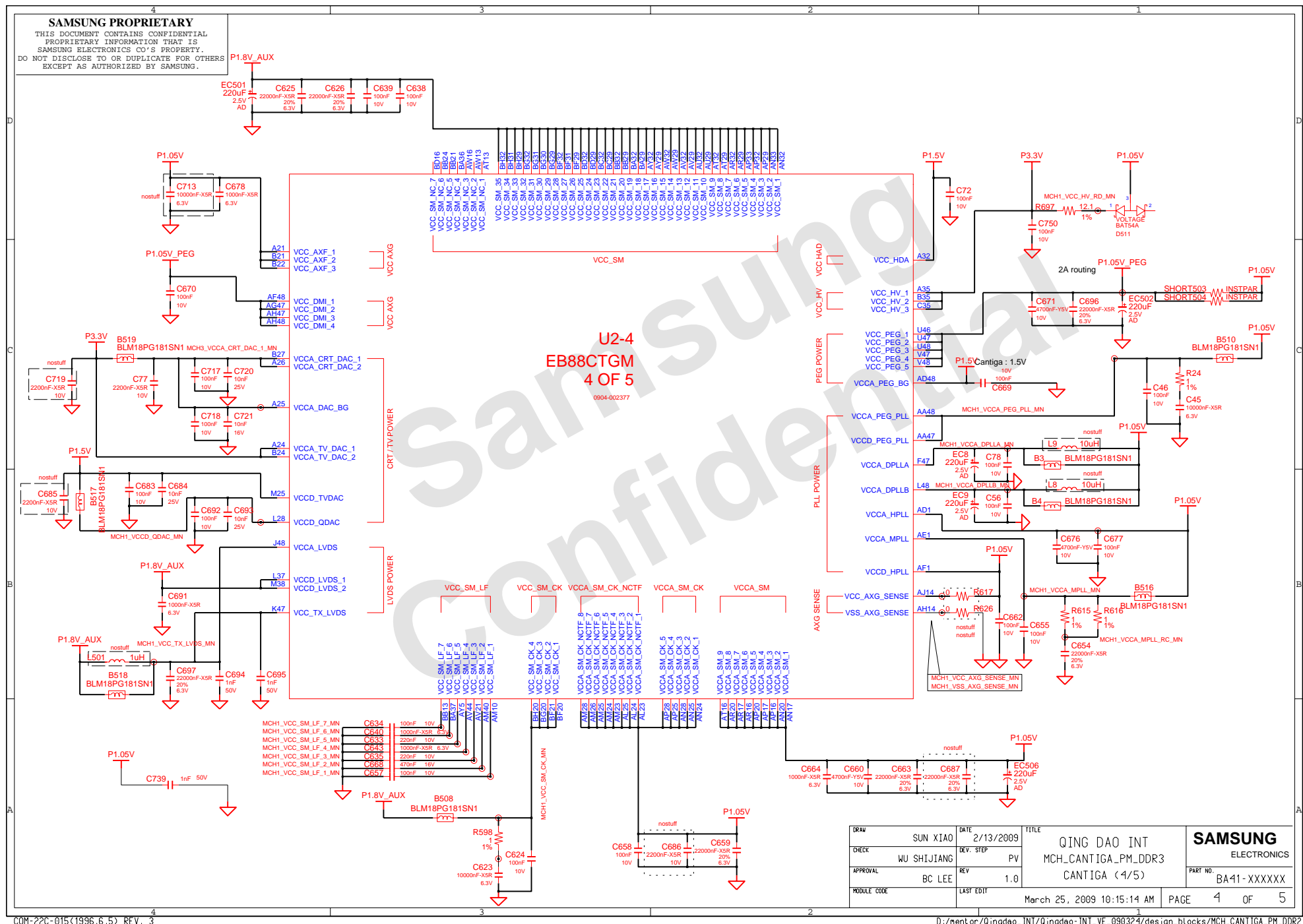
SAMSUNG
ELECTRONICS
PART NO. BA41-XXXXXX

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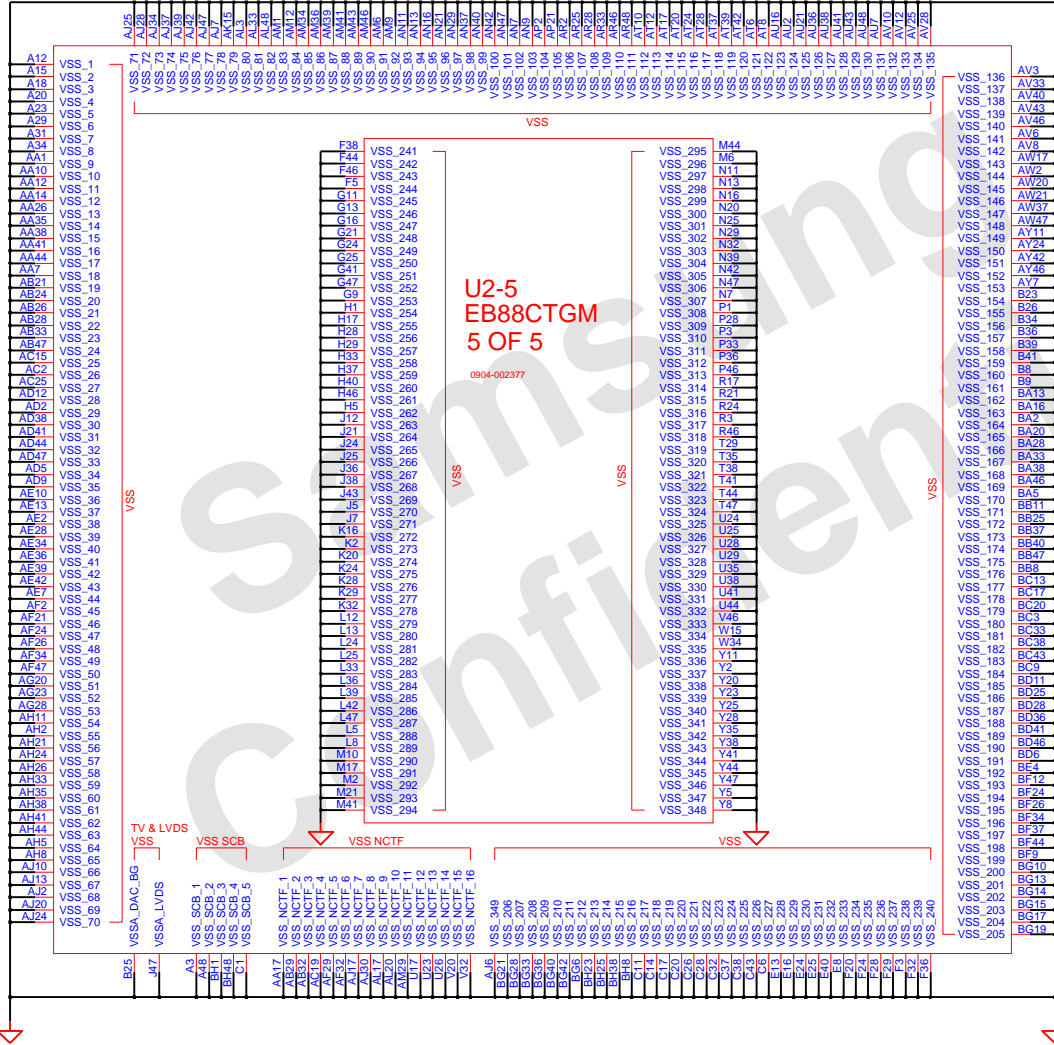
DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT MCH_CANTIGA_PM_DDR3 CANTIGA (2/5)	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT		March 25, 2009 10:15:14 AM	PAGE	2 OF 5

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DRAW		DATE		TITLE		SAMSUNG	
SUN XIAO		2/13/2009		QING DAO INT		ELECTRONICS	
CHECK		REV. STEP		MCH_CANTIGA_PM_DDR3			
WU SHIJIANG		PV		CANTIGA (4/5)		PART NO.	
APPROVAL		REV				BA41-XXXXXX	
BC LEE		1.0					
MODULE CODE		LAST EDIT		March 25, 2009 10:15:14 AM		PAGE 4 OF 5	

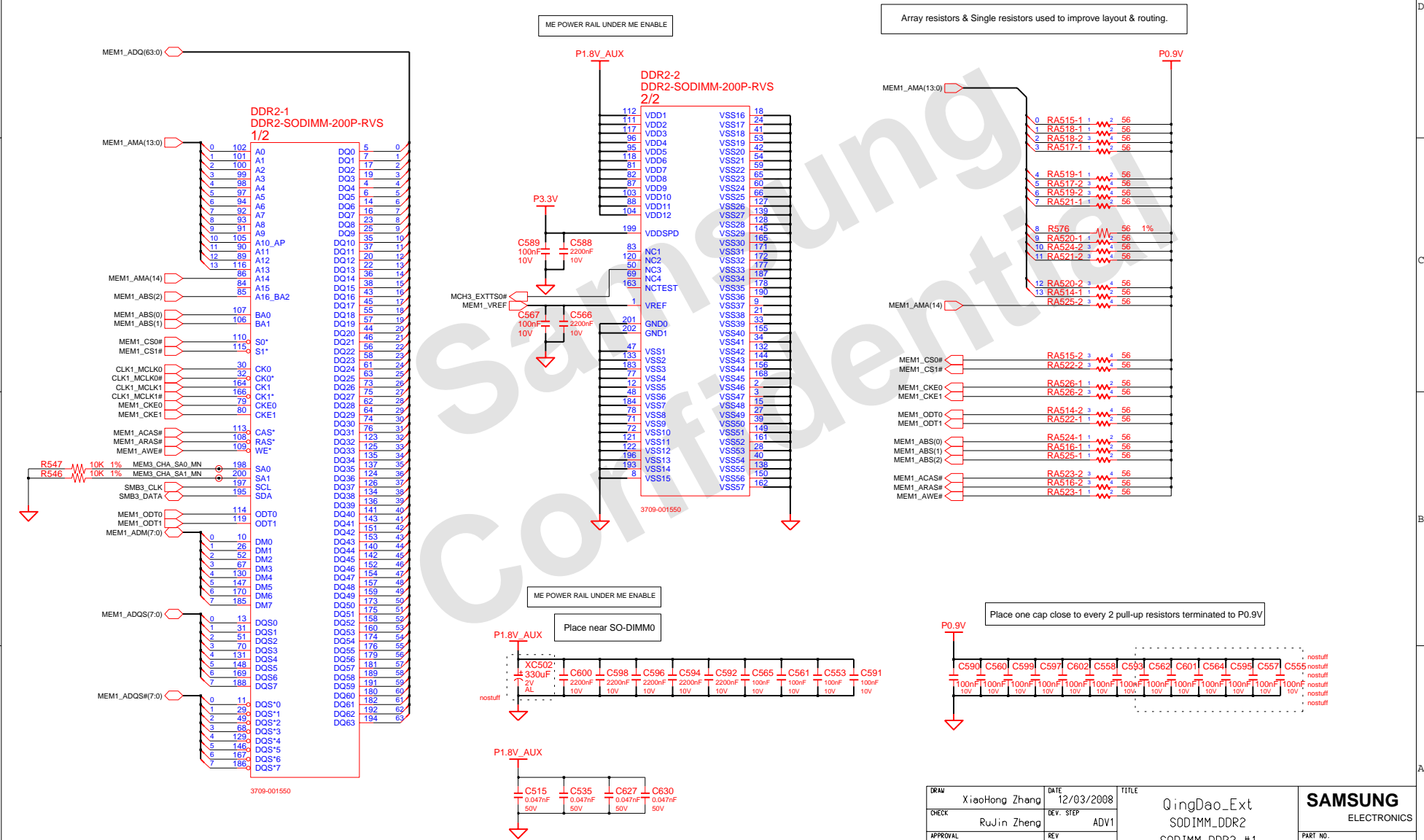
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DRAW SUN XIAO		DATE 2/13/2009	TITLE QING DAO INT MCH_CANTIGA_PM_DDR3 CANTIGA (5/5)		SAMSUNG ELECTRONICS	
CHECK WU SHIJIANG	DEV. STEP PV					
APPROVAL BC LEE	REV 1.0					
MODULE CODE			LAST EDIT March 25, 2009 10:15:14 AM		PART NO. BA41-XXXXXX	
			PAGE 5		OF 5	

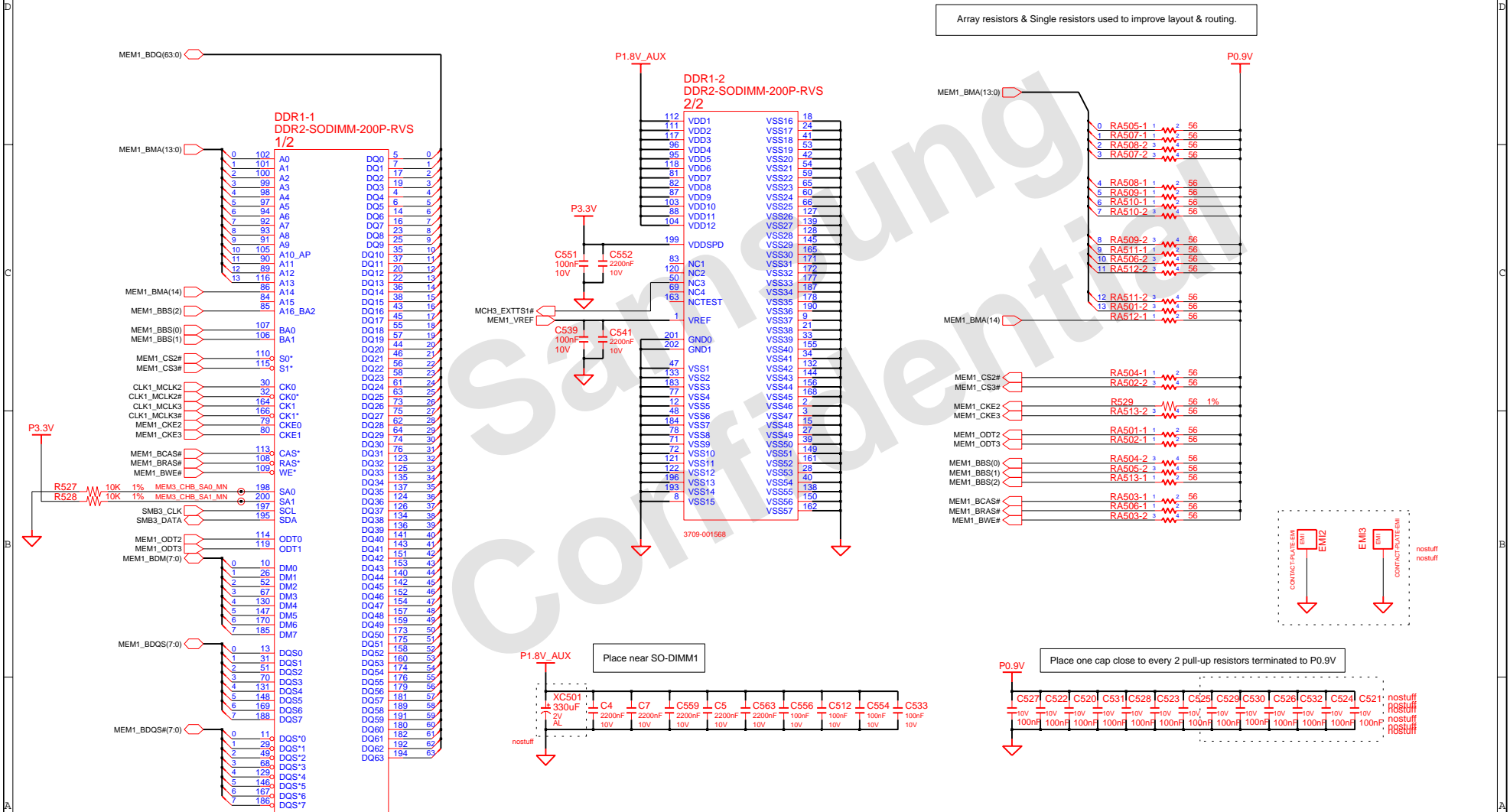
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DDR SO-DIMM #0

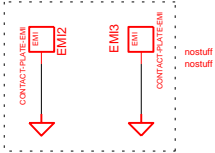


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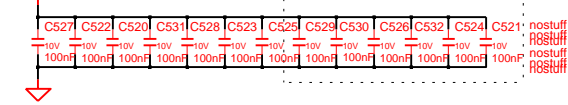
DDR SO-DIMM #1



Array resistors & Single resistors used to improve layout & routing.



Place one cap close to every 2 pull-up resistors terminated to P0.9V

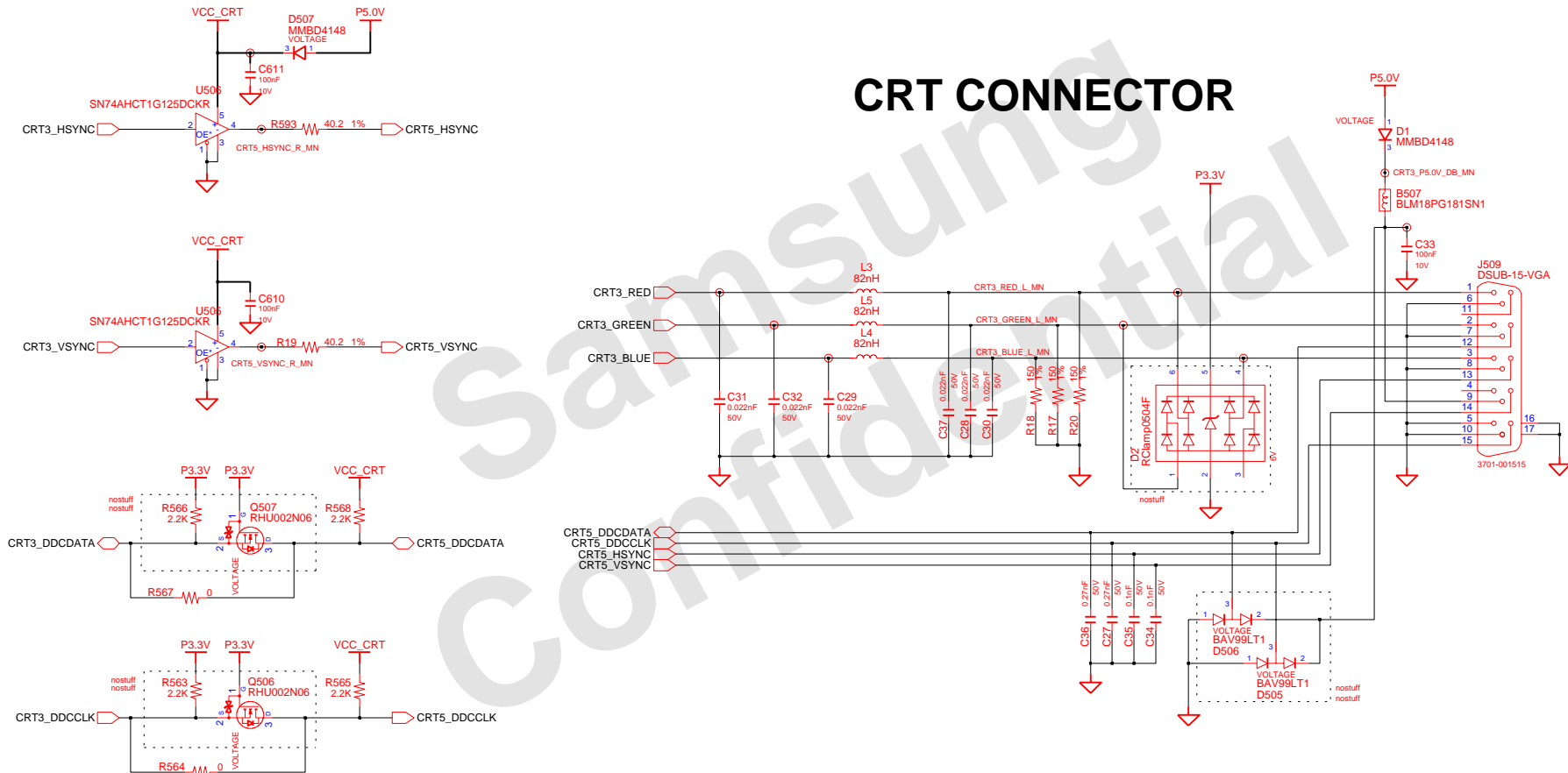


DRW	XiaoHong Zheng	DATE	12/03/2008	TITLE	QingDao_Ext	SAMSUNG ELECTRONICS
CHECK	RuJin Zheng	REV. STEP	ADV1	SODIMM_DDR2	PART NO.	
APPROVAL	BC LEE	REV	1.0	SODIMM_DDR2 #2	BA41-xxxxxA	
MODULE CODE		LAST EDIT	December 03, 2008 20:55:25 PM	PAGE	2 OF 2	

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CRT

CRT CONNECTOR



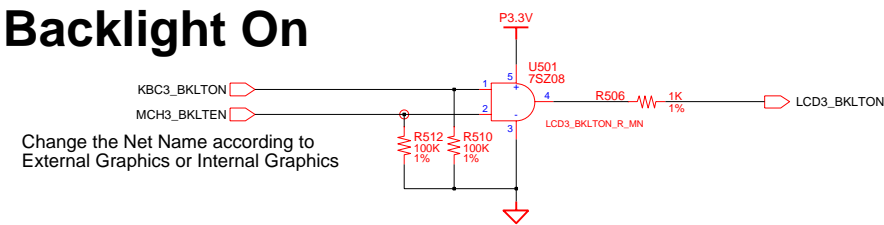
Check "CRT3_DDCCLK/DATA" Voltage Level
2N06 Can be replaced with SM6K2

DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT GRAPHICS_IF	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			PART NO. BA41-XXXXXX
MODULE CODE		LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	undef ined	

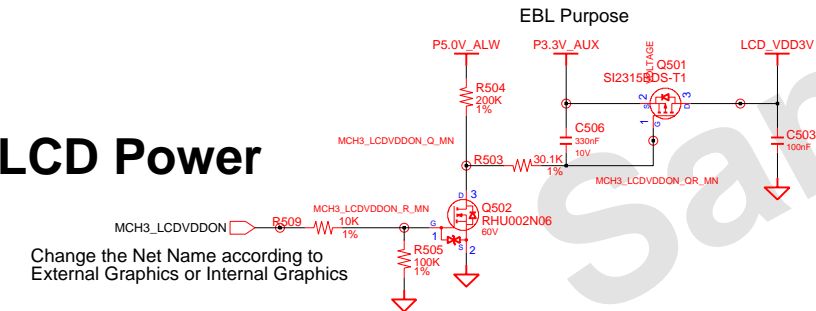
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LVDS

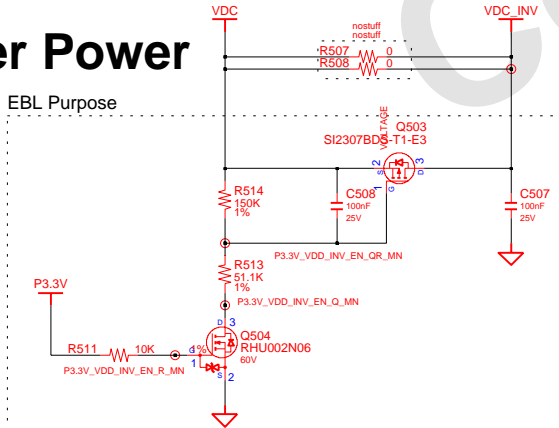
Backlight On



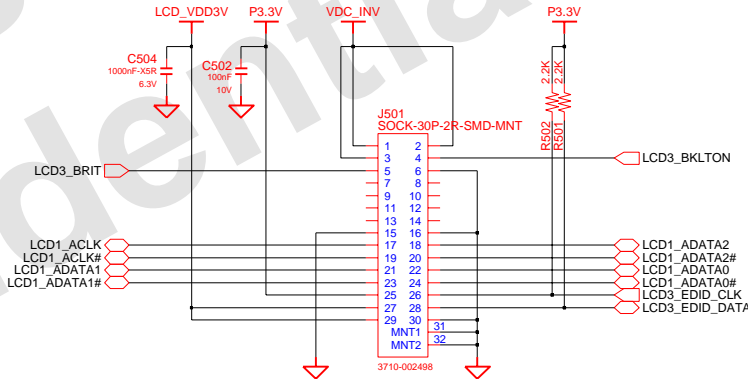
LCD Power



Inverter Power



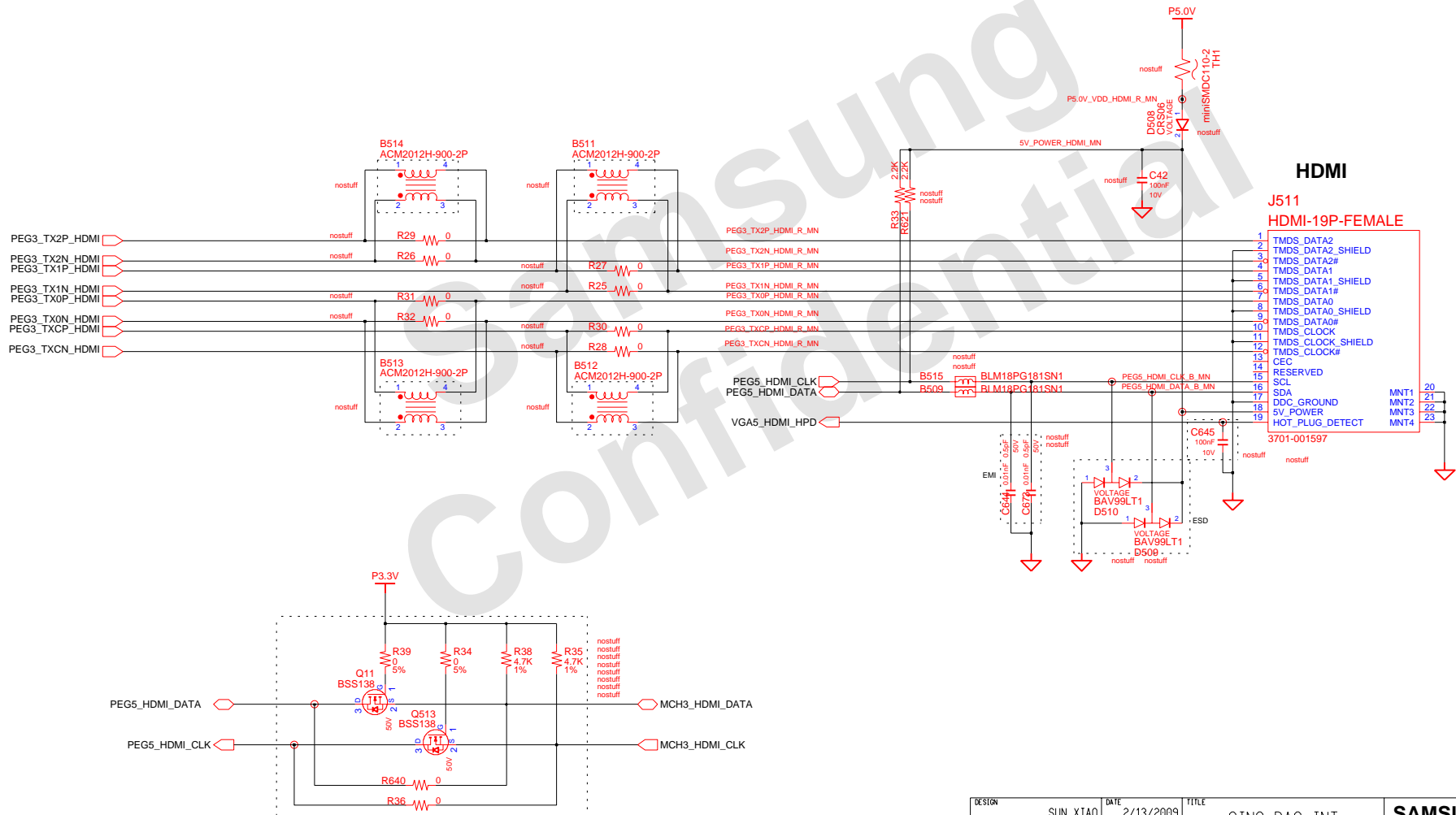
1Ch. LCD Connector



DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT GRAPHICS_IF LCD	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			PART NO. BA41-XXXXXX
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	2 of 2	defined

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HDMI NOSTUFF

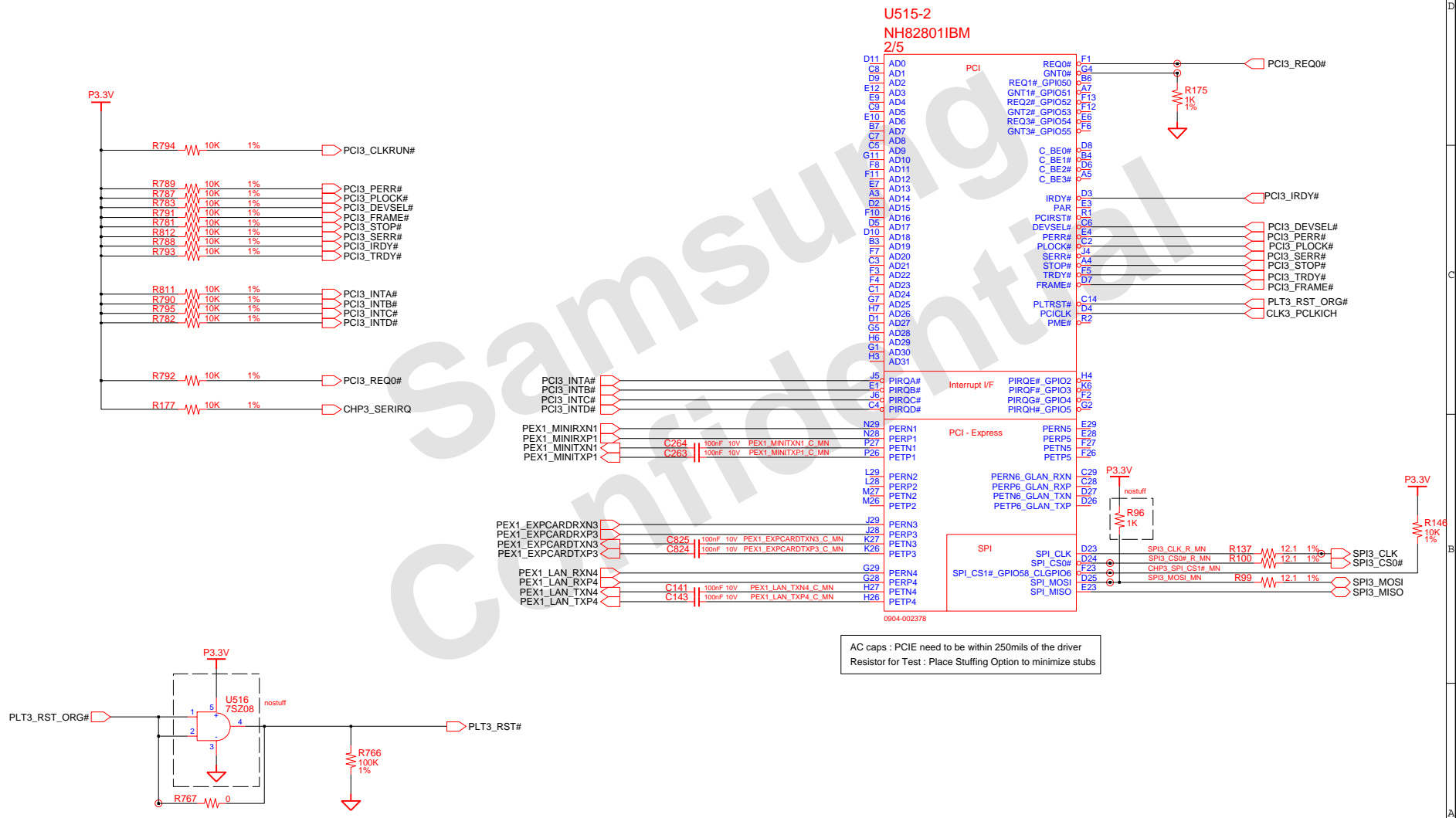


DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT GRAPHICS_IF HDMI	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			PART NO. BA41-XXXXX
APPROVAL	BC LEE	REV	1.0			
MODULE CODE		LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	3	undefined

[illegible]

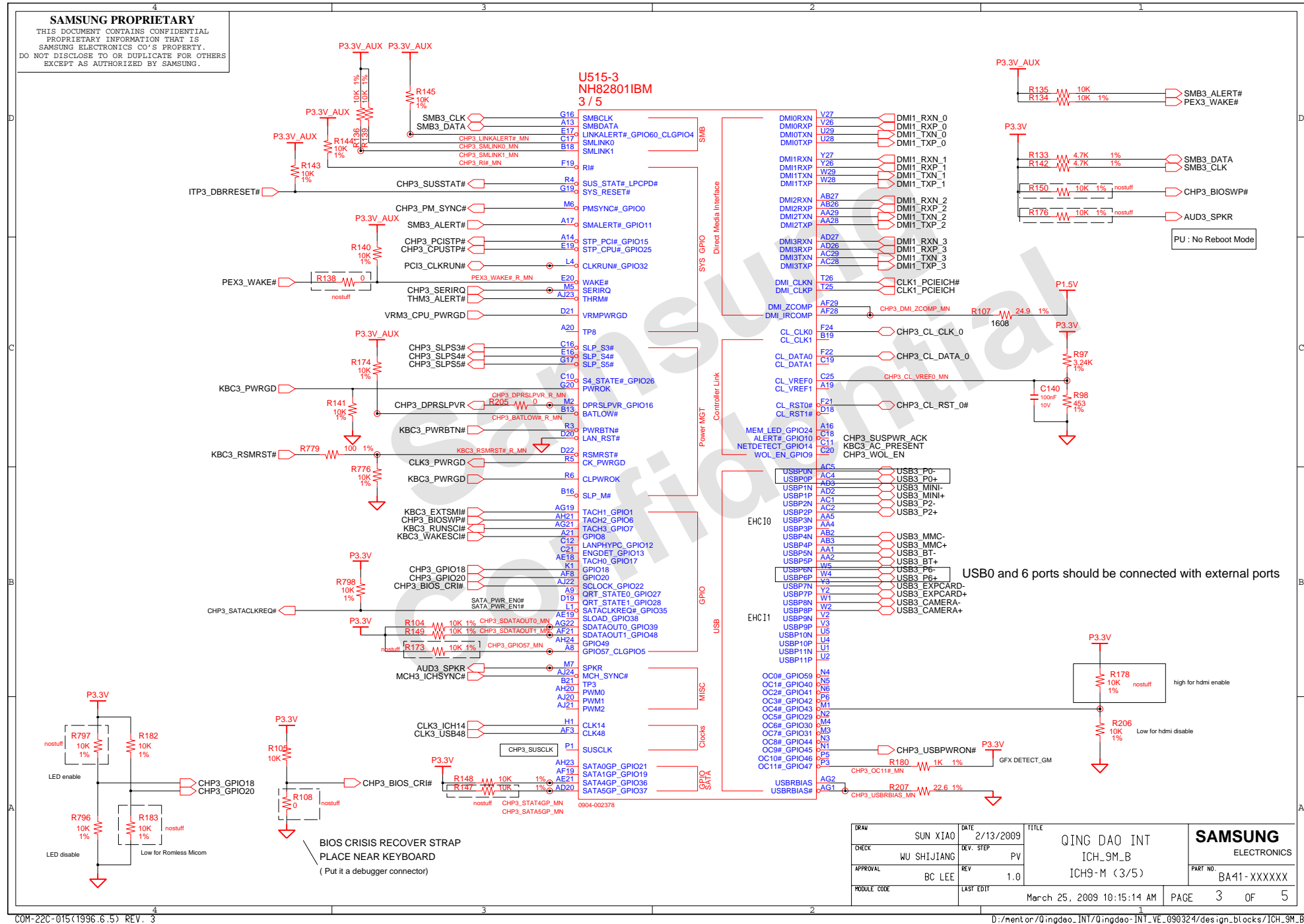
					D:\ment.or\Qingdao_INT\Qingdao-INT_VE_090324\design_blocks\ICH_9M_B
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DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT ICH_9M_B ICH9-M (2/5)	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
CHECK	WU SHIJIANG	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	2 OF 5	

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DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
CHECK	WU SHIJIANG	DEV. STEP	PV	ICH9M_B		
APPROVAL	BC LEE	REV	1.0	ICH9-M (3/5)		
MODULE CODE		LAST EDIT				
March 25, 2009 10:15:14 AM					PAGE	3 OF 5

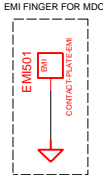
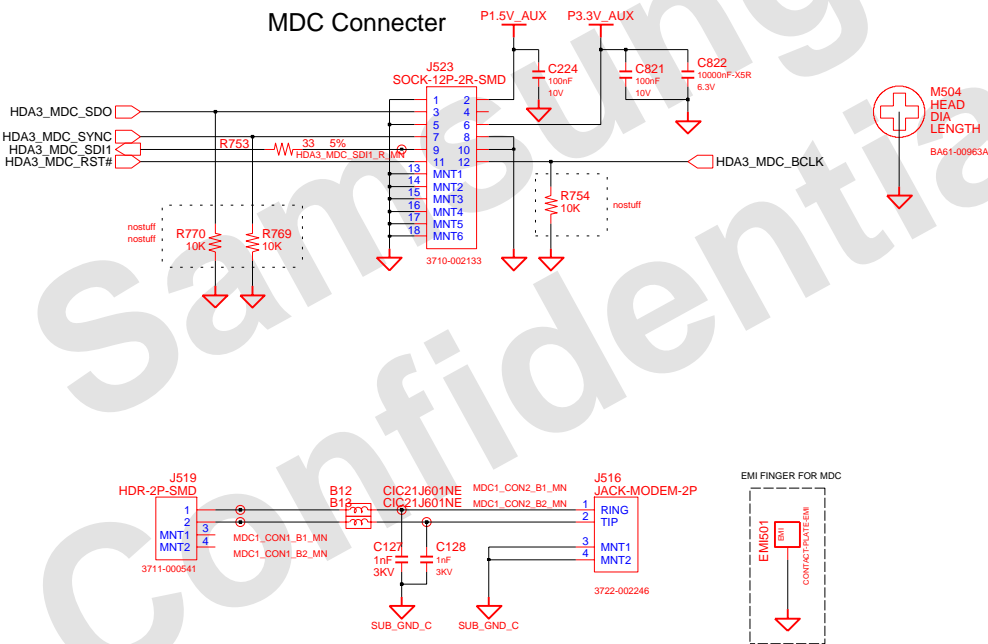
A



D:/mentor/Qingdao-INT/Qingdao-INT_VE_090324/design_blocks/ICH_9M_E

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MDC FUNCTION FOR OPTION



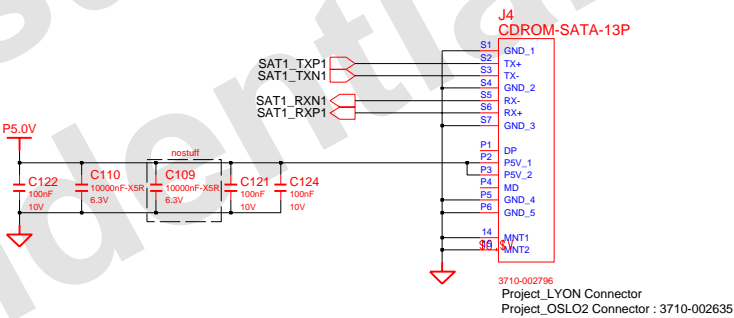
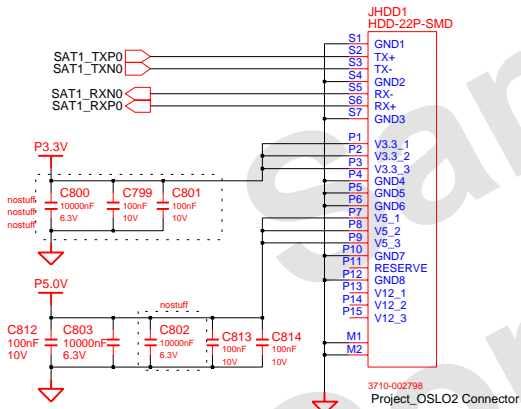
DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
CHECK	WU SHIJIANG	DEV. STEP	PV		HDA_Modem	
APPROVAL	BC LEE	REV	1.0		HDA_Modem	
MODULE CODE		LAST EDIT				
March 25, 2009 10:15:14 AM						PAGE 1 OF 1

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SATA I/F CONN

SATA HDD CONN

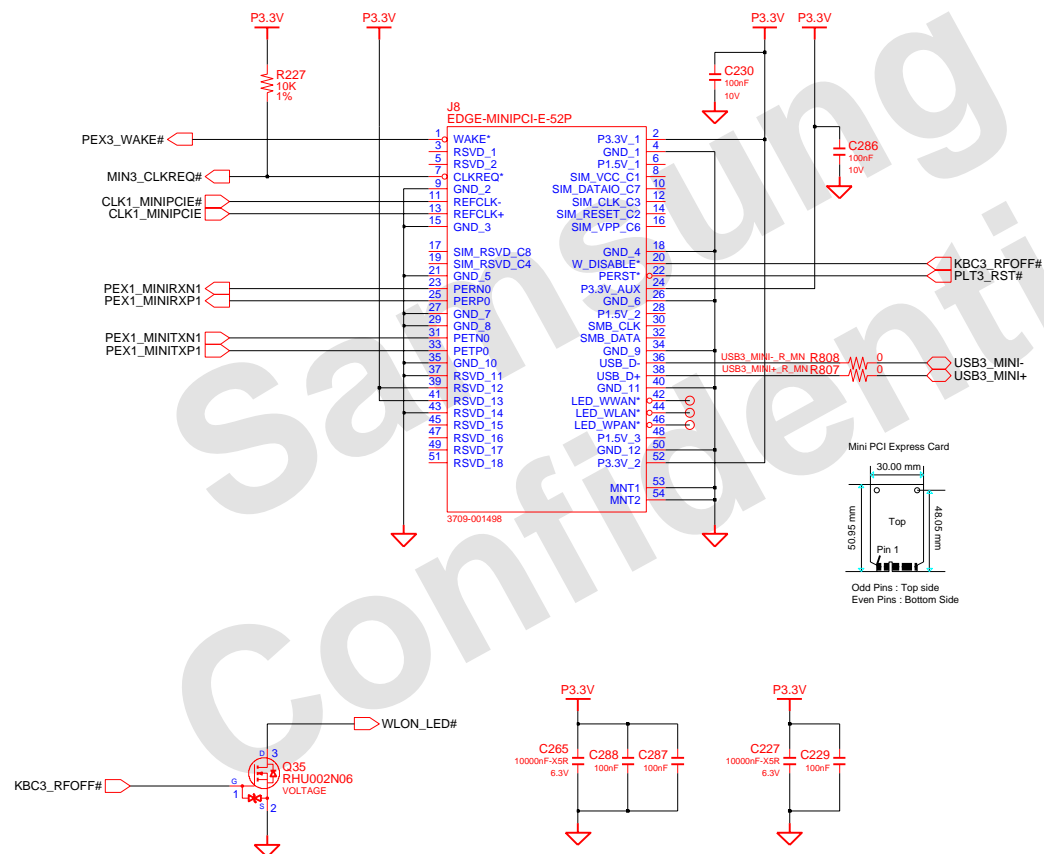
SATA ODD CONN



DESIGN	XiaoHong Zheng	DATE	12/3/2008	TITLE	QingDao_Ext SATA_DEVICES HDD ODD	SAMSUNG ELECTRONICS
CHECK	RuJin Zheng	DEV. STEP	ADV1			PART NO. BA41-xxxxxA
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	December, 3, 2008 12:06:51 PM	PAGE	1	OF

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WLAN, 7mm

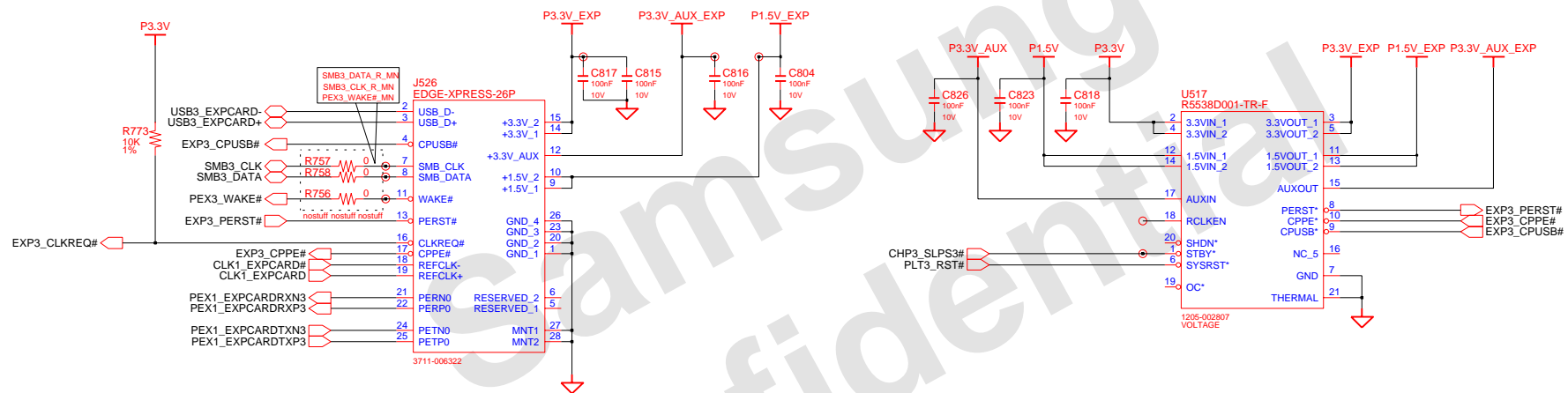


DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT MINI_PCIE_CONN	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
CHECK	WU SHIJIANG	DEV. STEP	PV			
APPROVAL	BC LEE	REV	1.0	WLAN		
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	1 OF	

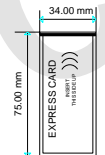
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Express Card

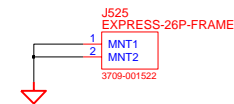
Express Card Power Switch



Type 1 module



34.00 mm W
X
75.00 mm L
X
5.00 mm H

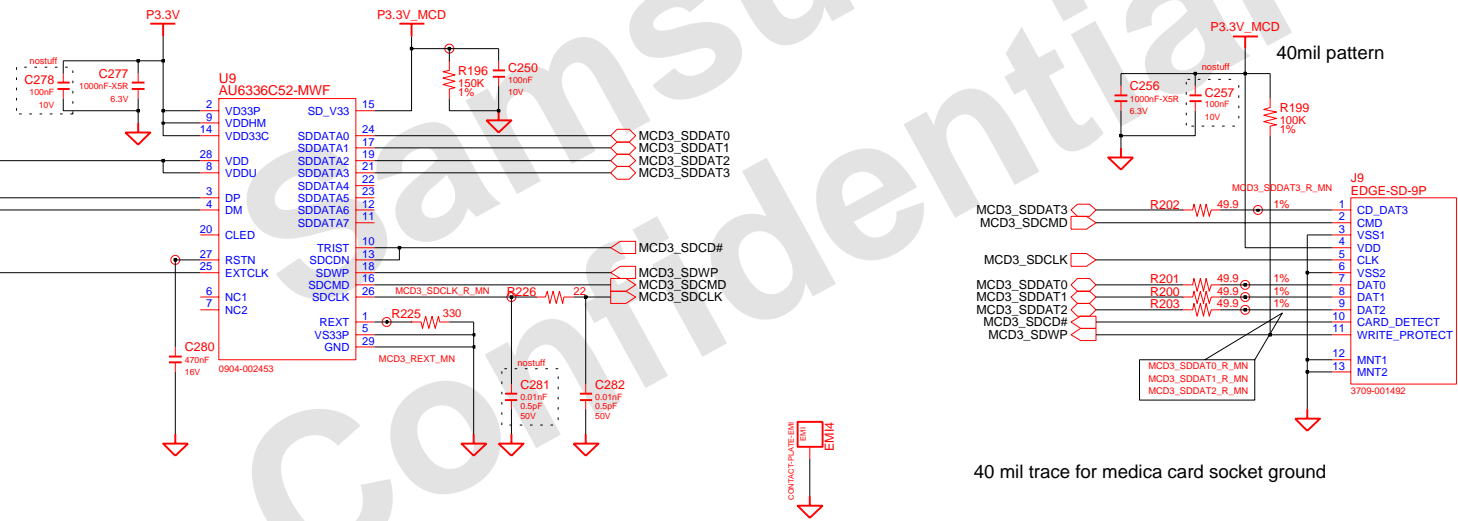


DESIGN	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT EXPRESS CARD	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV			PART NO. BA41-XXXXXX
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	1	OF

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CARDREADER AU6366

P3.3V_MCD distance between R5U880 and socket should be less than 2 inches



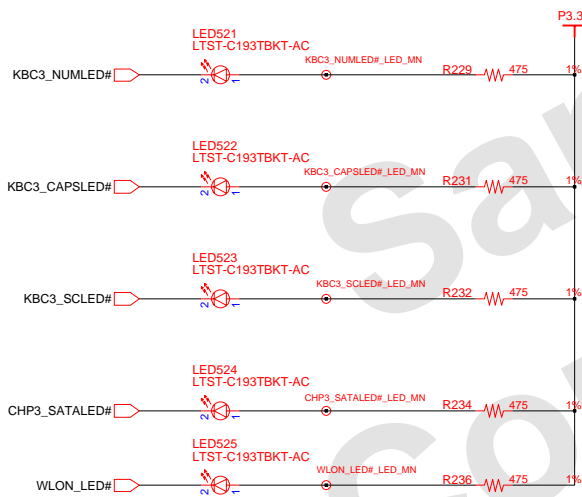
MSEL5	SD Write Protec Selection
Connected to VCC	High Enable
Connected to GND	Low Enable
MSEL7	PLL BASE CLOCK SELECTION
Connected to VCC	12MHz
Connected to GND	48MHz

DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV		AU6336	
APPROVAL	BC LEE	REV	1.0			
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	1 OF	

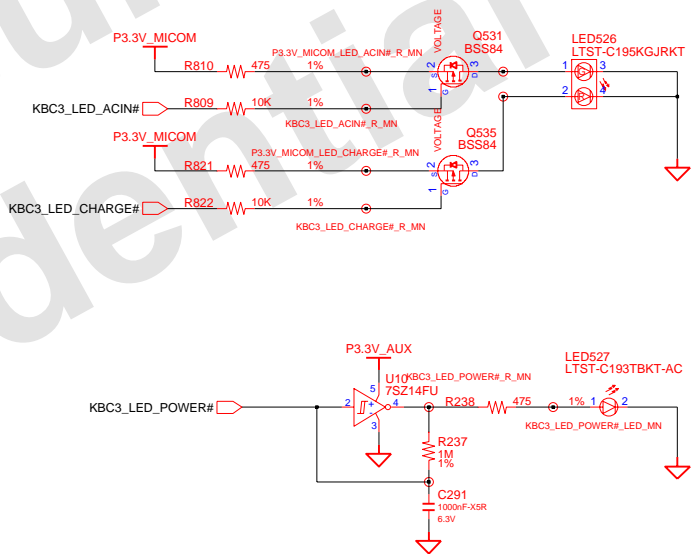
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LED SWITCH LOGIC

Function Key LEDs

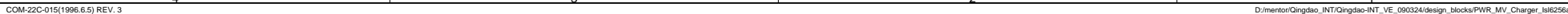


ADAPTERIN/CHARGING LED

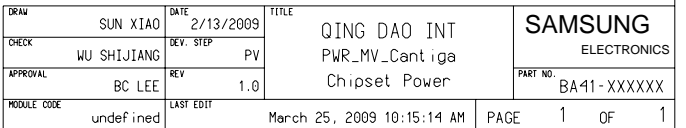


DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXX
CHECK	WU SHIJIANG	DEV. STEP	PV	LED_Switch	LED_Switch	
APPROVAL	BC LEE	REV	1.0	LED_Switch		
MODULE CODE		LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	1 OF 1	

CHARGER & POWER MANAGEMENT

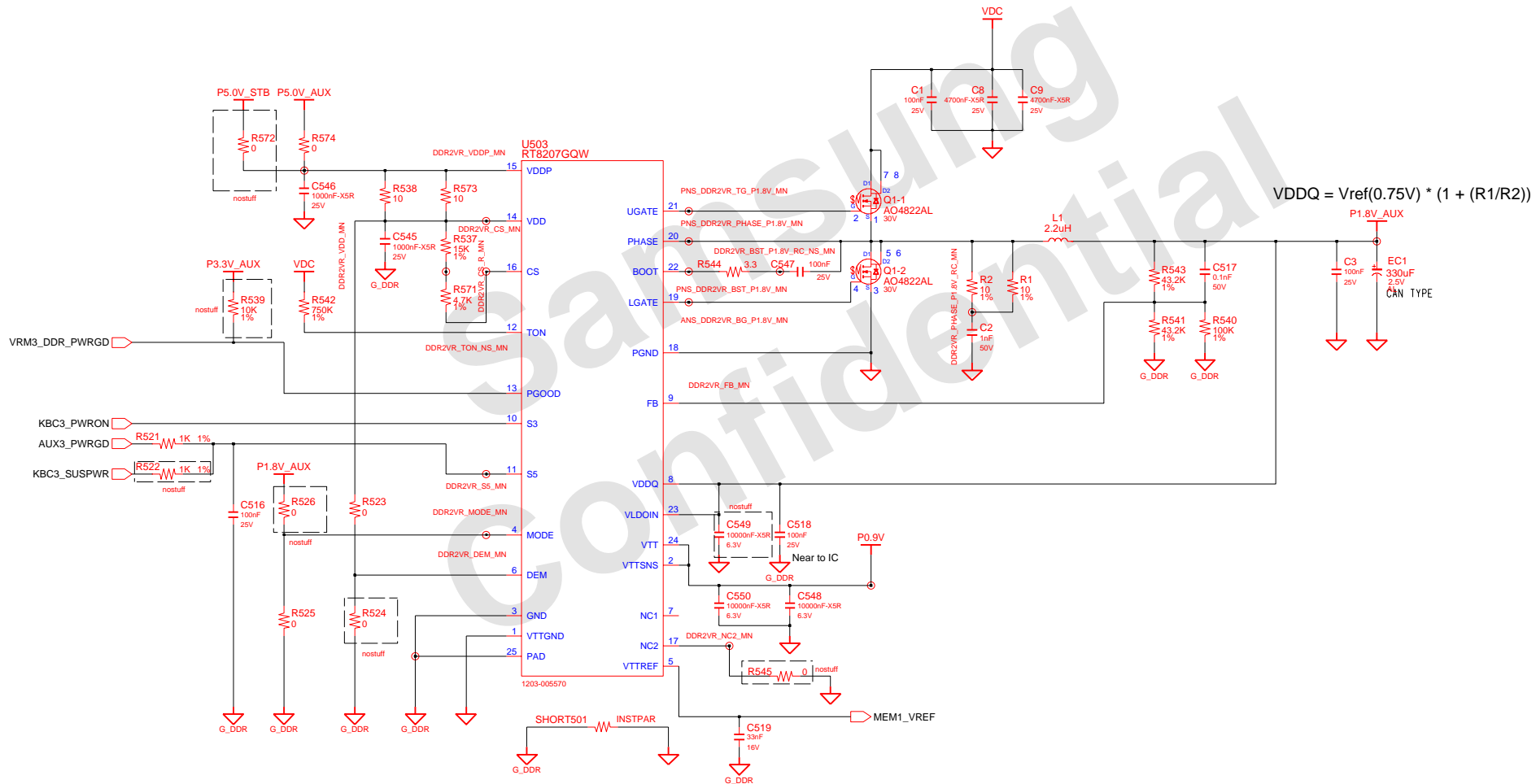


1.05V & P1.5V



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DDR2 Power

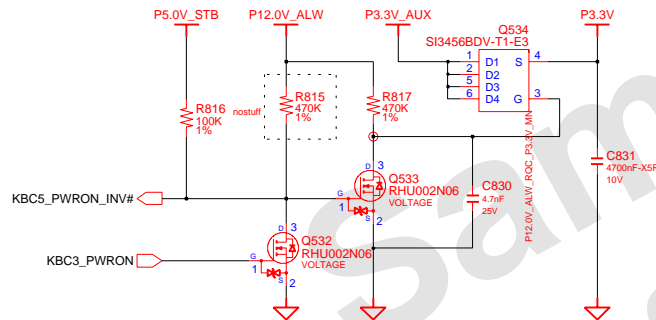


DRW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG
CHECK	WU SHIJIANG	DEV. STEP	PV		PWR_MV_MeMory	ELECTRONICS
APPROVAL	BC LEE	REV	1.0		DDR3 POWER (P1.5V_AUX)	PART NO. BA41-XXXXXX
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM	PAGE	1	OF 1

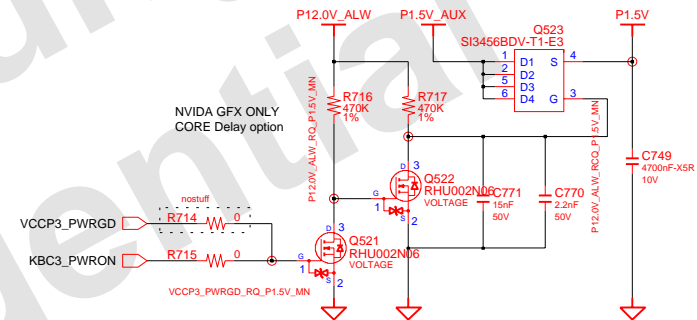
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Switched Power

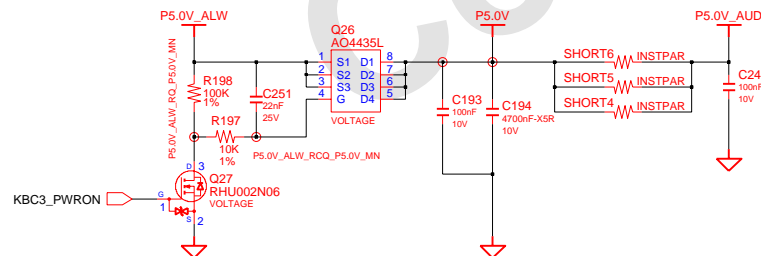
Switched Power On (P3.3V)



Switched Power On (P1.5V)



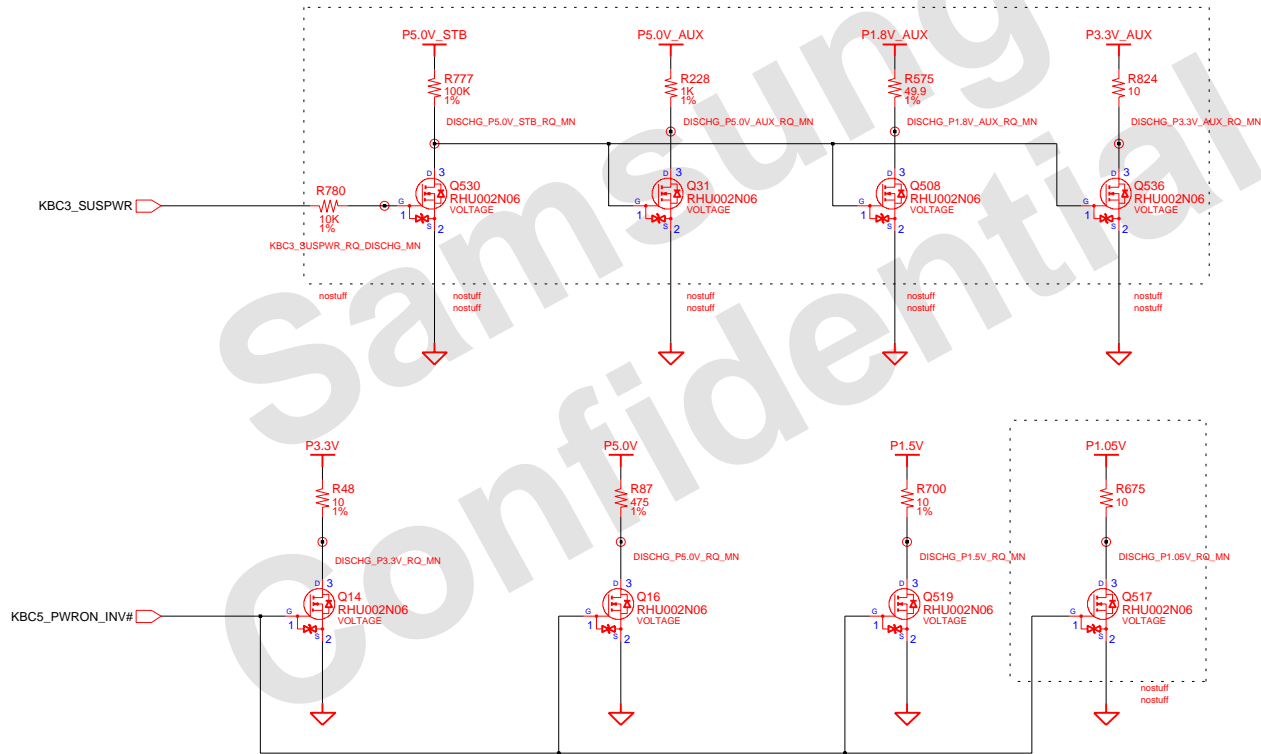
Switched Power On (P5.0V)



DESIGN	XIAOHONG, ZHANG	DATE	12/3/2008	TITLE	QingDao_Ext PWR_MV_SWITCHED Switched Power	SAMSUNG ELECTRONICS PART NO. BA41-xxxxxA
CHECK	RUJIN, ZHENG	DEV. STEP	ADV1			
APPROVAL	BC, LEE	REV	1.0			
MODULE CODE		LAST EDIT	December, 3, 2008 3:39:16 PM	PAGE	2 OF	

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POWER DISCHARGER

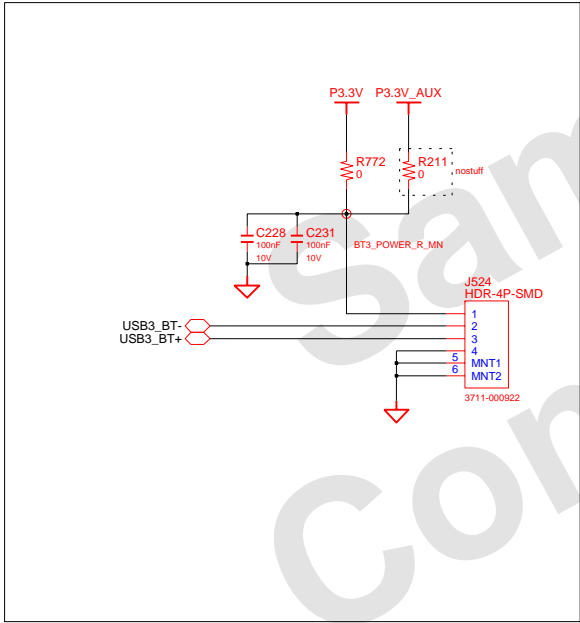


DRAW	SUN XIAO	DATE	2/13/2009	TITLE	QING DAO INT	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG	DEV. STEP	PV		PWR_MV_DisCharger	
APPROVAL	BC LEE	REV	1.0		DISCHARGING LOGIC	
MODULE CODE	undefined	LAST EDIT	March 25, 2009 10:15:14 AM			
PAGE 1 OF 1						PART NO. BA41-XXXXXX

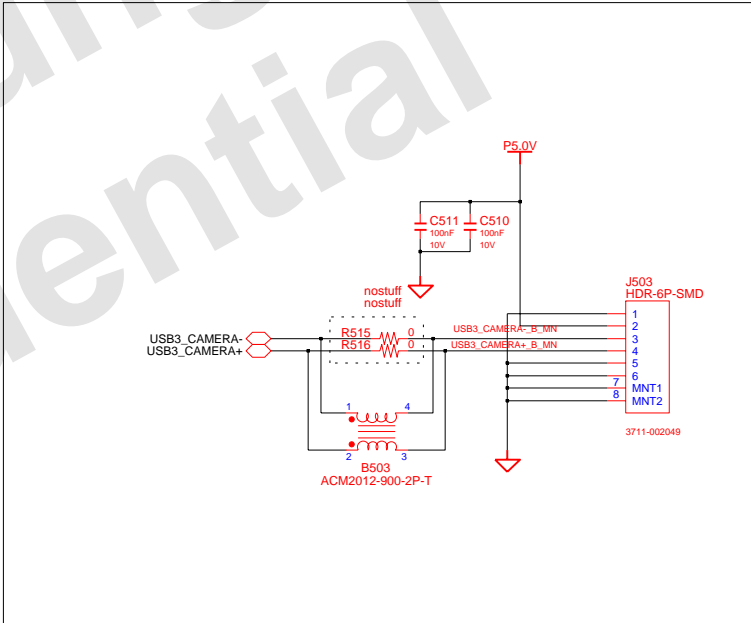
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USB I/F Devices_NOSTUFF

Bluetooth Interface



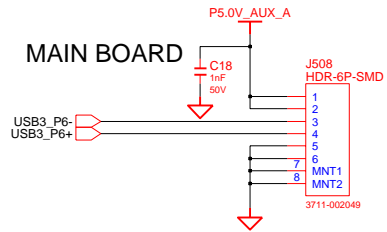
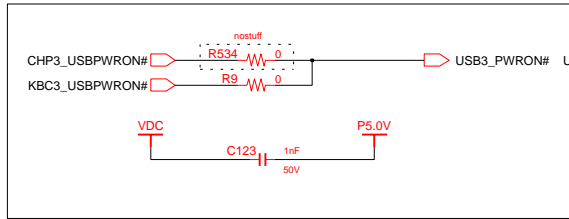
CAMERA



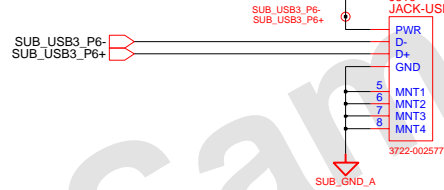
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CHECK	RuJin Zheng	DEV. STEP	ADV1			PART NO.
APPROVAL	BC LEE	REV	1.0			BA41-xxxxxA
MODULE CODE		LAST EDIT	December , 3, 2008 12:12:55 PM	PAGE	undefined	

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MAIN BOARD

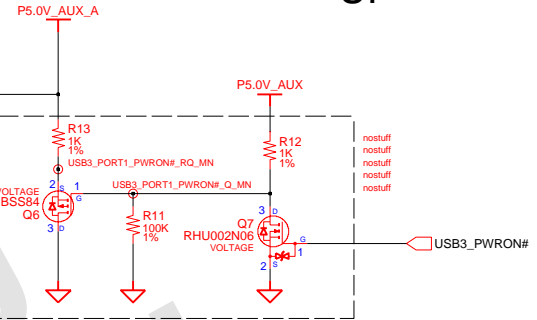
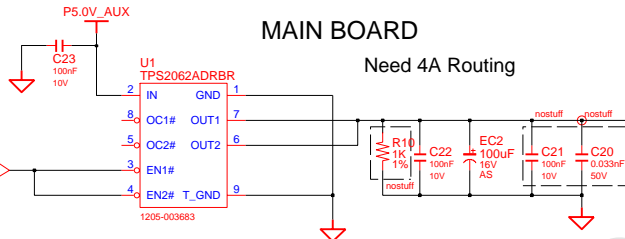


SUB BOARD

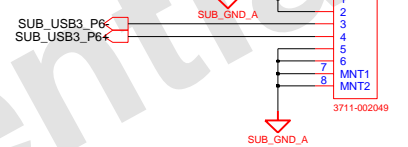


MAIN BOARD

Need 4A Routing

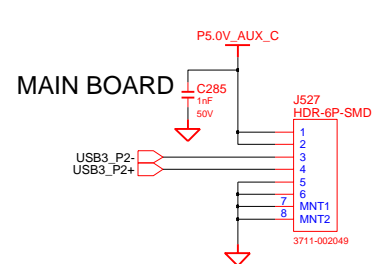
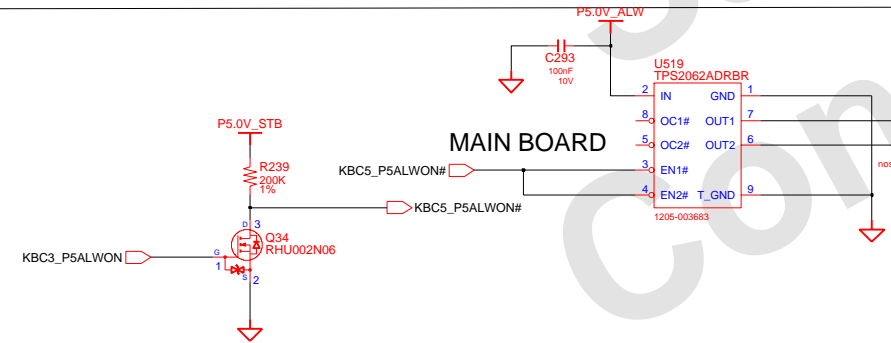


SUB BOARD

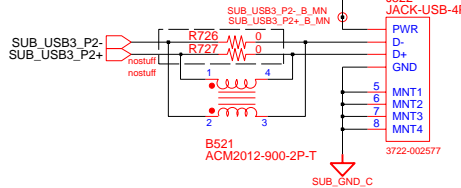


MAIN BOARD

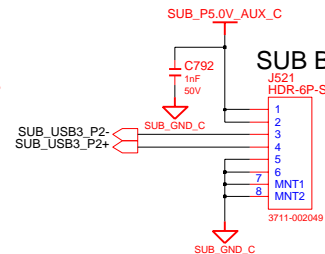
Need 4A Routing



SUB BOARD



SUB BOARD



UP

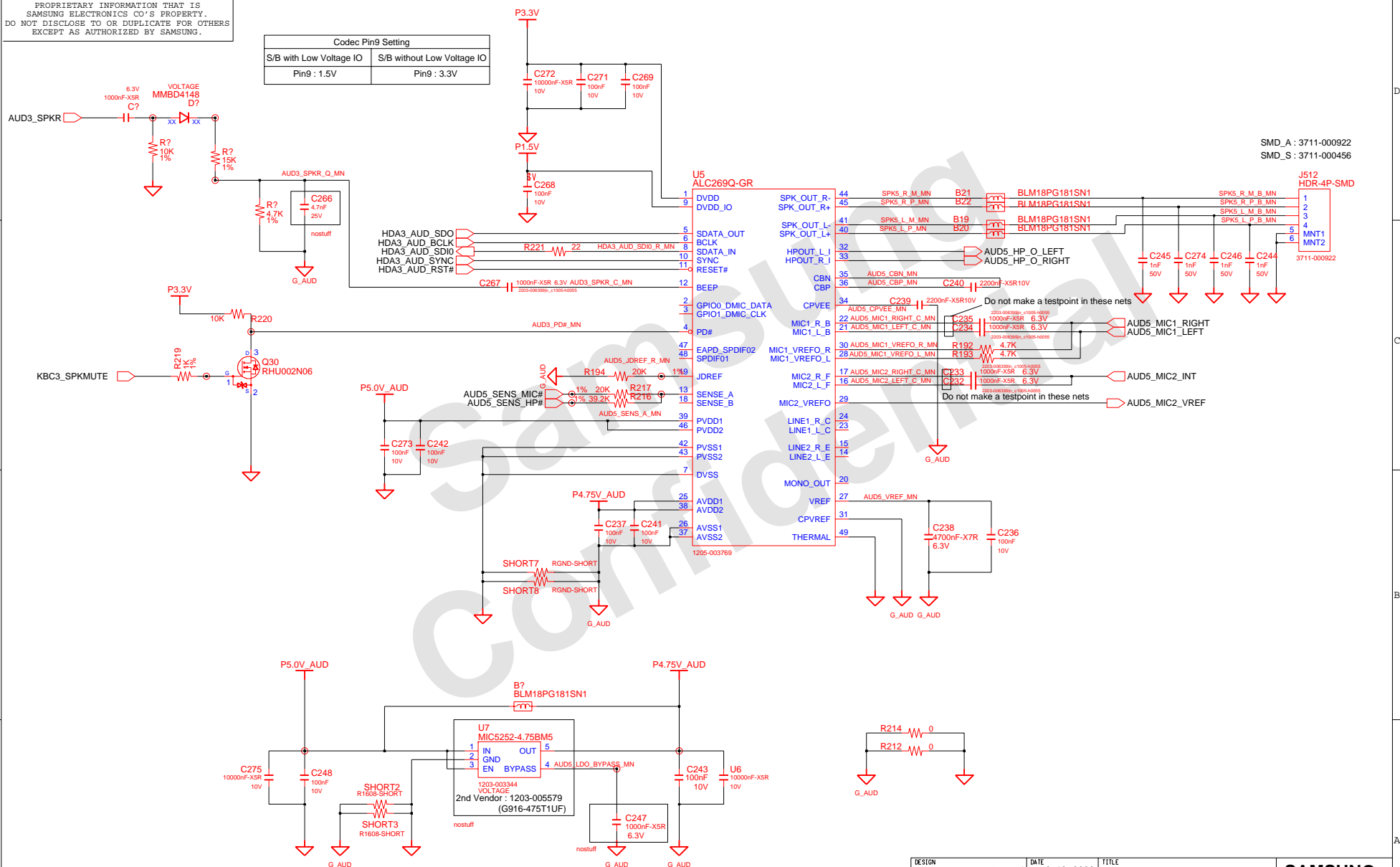
DOWN

DESIGN	XiaoHong Zhang	DATE	12/3/2008	TITLE	To RJ11 cable. (Connect with BA39-00593A)
CHECK	RuWen Zheng	DEV. STEP	ADV1		
APPROVAL	BC LEE	REV	1.0		
MODULE CODE	undefined	LAST EDIT	December , 3, 2008 12:12:18 PM	PAGE	1 OF

SAMSUNG
ELECTRONICS
PART NO. BA41-xxxxxA

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Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V

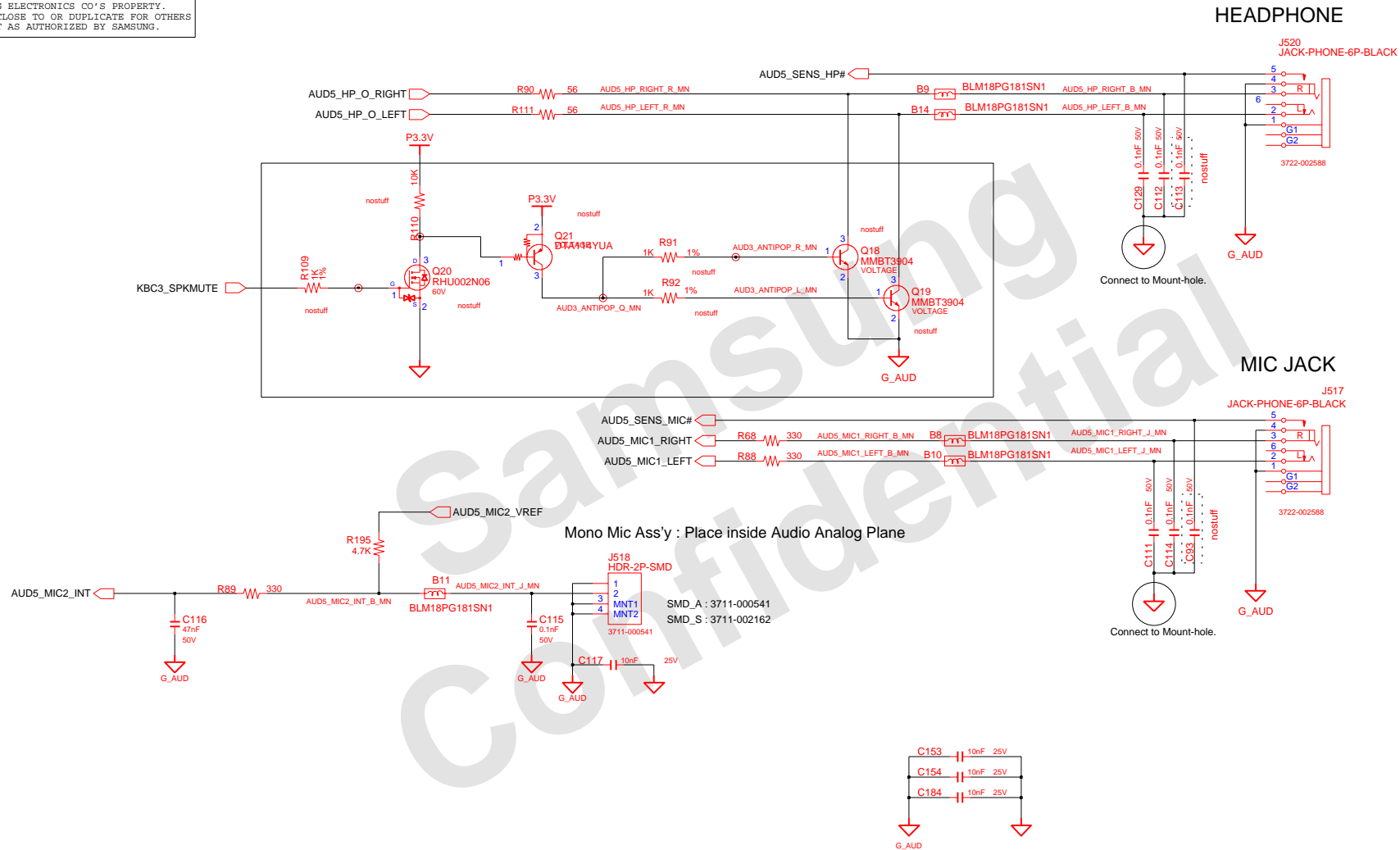


SMD_A : 3711-000922
SMD_S : 3711-000456

J512 HDR-4P-SMD
1
2
3
4
5
6
MNT1
MNT2
3711-000922

DESIGN	AVN, HW1	DATE	3/13/2009	TITLE	HD Audio HDA_ALC269_GR AUDIO CODEC	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXXH
CHECK	AVN, HW1	DEV. STEP				
APPROVAL	AVN, HW1	REV	1.0			
MODULE CODE		LAST EDIT	March, 13, 2009 10:34:10 AM	PAGE	1 OF 2	

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DESIGN	AVN, HW1	DATE	3/13/2009	TITLE	HD Audio HDA_ALC269_GR AUDIO INPUT/OUTPUT	SAMSUNG ELECTRONICS PART NO. BA41-XXXXXH
CHECK	AVN, HW1	DEV. STEP				
APPROVAL	AVN, HW1	REV	1.0			
MODULE CODE		LAST EDIT	March, 13, 2009 10:35:26 AM	PAGE	2 OF 2	

