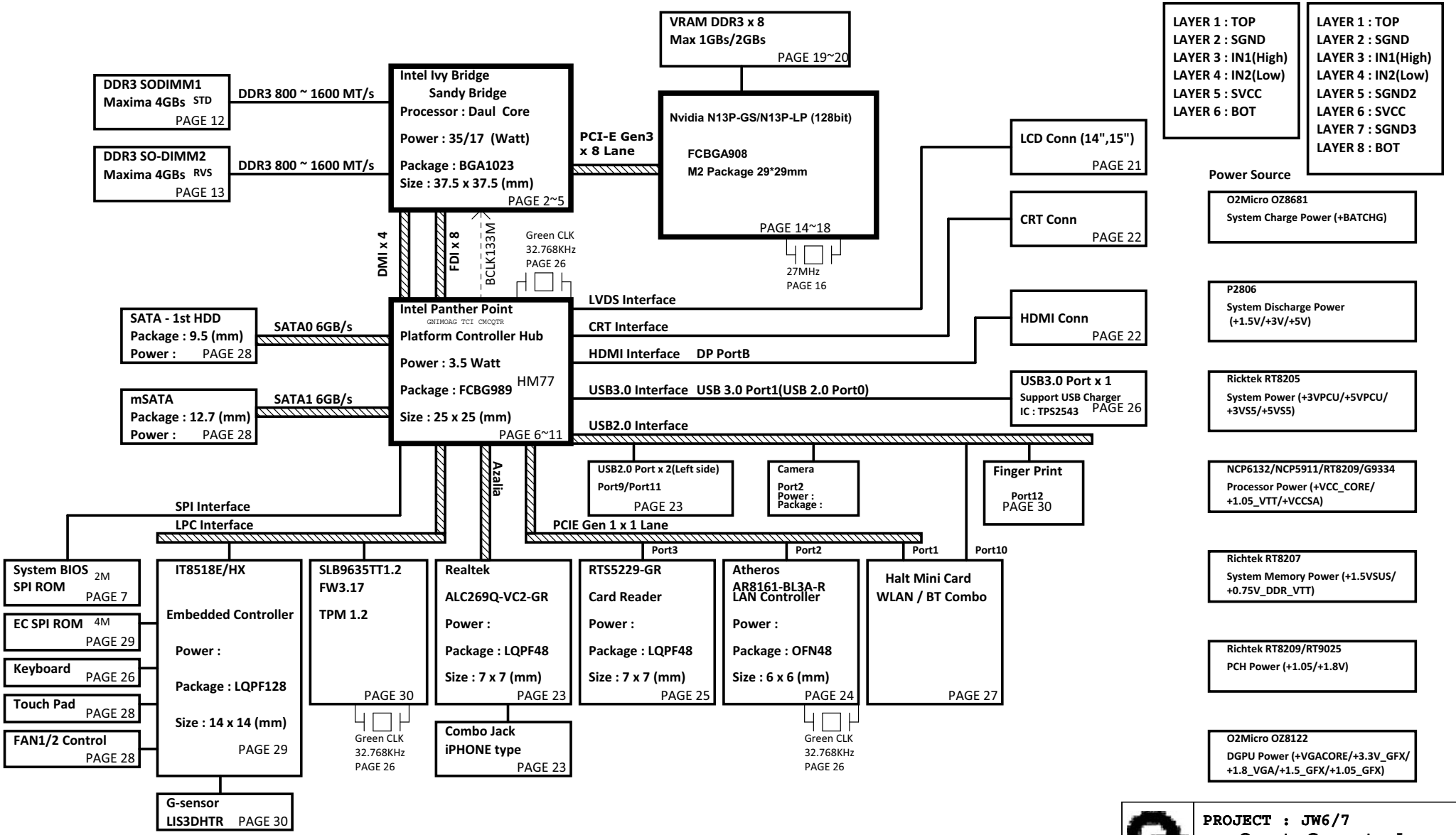
JW6/7 DIS/UMA (14",15") Ultra
Intel Chief River Platform Block Diagram

01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SGND2
LAYER 6 : SVCC
LAYER 7 : SGND3
LAYER 8 : BOT

Power Source

O2Micro OZ8681
System Charge Power (+BATCHG)

P2806
System Discharge Power
(+1.5V/+3V/+5V)

Ricktek RT8205
System Power (+3VPCU/+5VPCU/
+3VS5/+5VS5)

NCP6132/NCP5911/RT8209/G9334
Processor Power (+VCC_CORE/
+1.05_VTT/+VCCSA)

Richtek RT8207
System Memory Power (+1.5VSUS/
+0.75V_DDR_VTT)

Richtek RT8209/RT9025
PCH Power (+1.05/+1.8V)

O2Micro OZ8122
DGPU Power (+VGACORE/+3.3V_GFX/
+1.8_VGA/+1.5_GFX/+1.05_GFX)

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
A3	Block Diagram	B
Date: Thursday, May 17, 2012	Sheet 1 of 42	

Ivy Bridge Processor (DMI,PEG,FDI)

02

PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

U14A

DMI
Intel(R) FDI
eDP
PCI EXPRESS - GRAPHICS

IC,IVB_2CBGA,0P7

U14B

MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM

IC,IVB_2CBGA,0P7

Place C626 Close to R394

Placement close to EC.

20120411,MV

SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

CPU XDP

PEG x8

CPU RESET#

20110816 modify:
REGULATOR DEL FOR SHORT

Intel DG request

DDR3 DRAM RESET

20110816 modify:
REGULATOR DEL FOR SHORT

SM_DRAMPWROK
Processor Input.

Processor pull-up (CPU)

eDP_COMPIO and ICOMPO signals should be shorted
near balls and routed with typical impedance <25 mohms

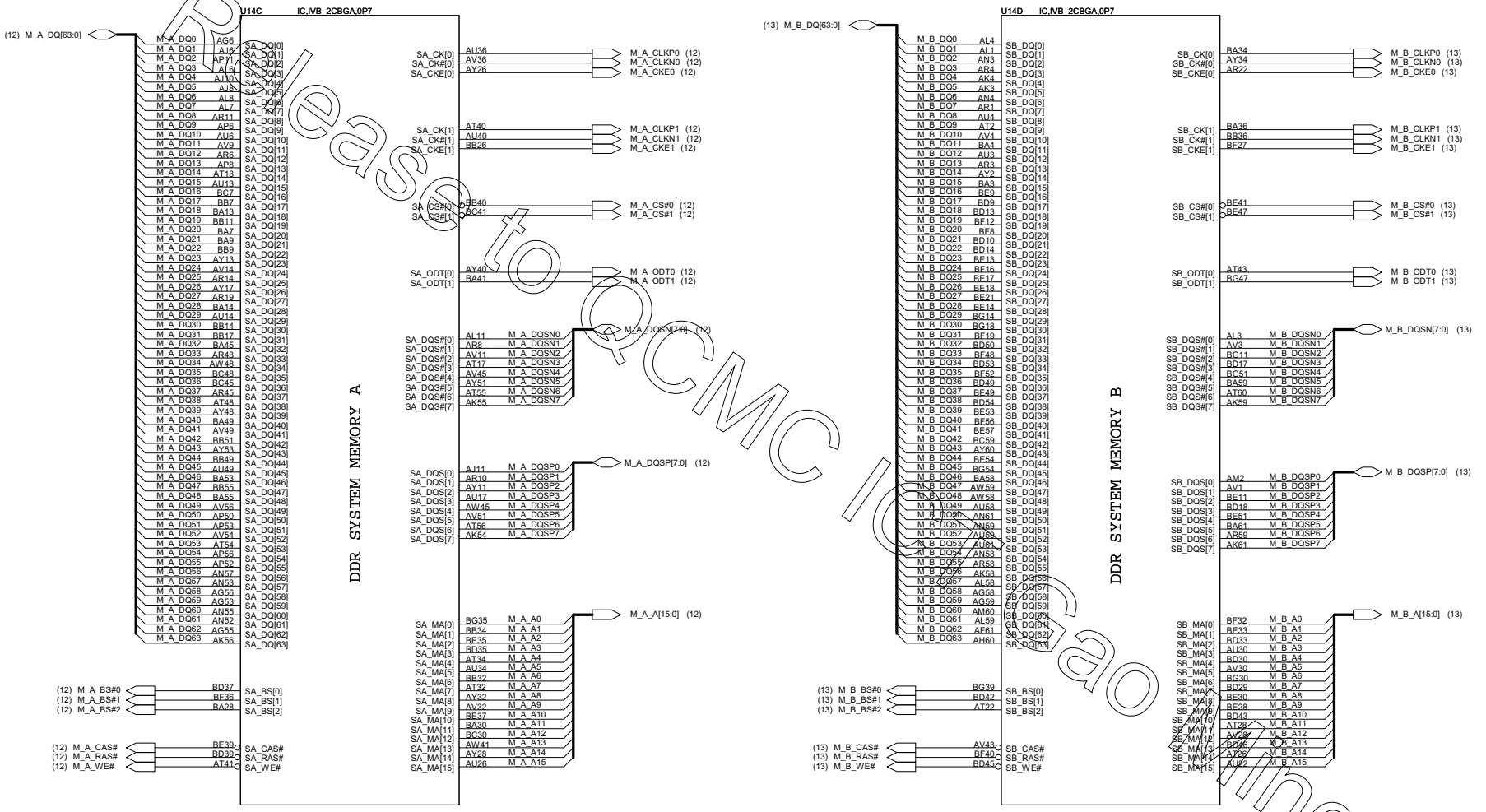
For iFDIM
Trigger Point

Connect a Test Point on BPM# 6 signal, very close to processor.

Connect a Test Point on BPM# 7 signal, very close to processor.

PROJECT : JW6/7			
Quanta Computer Inc.			
NB5	Size: Custom	Document Number: Processor 1/4 (Host/GPU)	Rev: A
	Date: Friday, May 11, 2012	Sheet: 2 of 42	

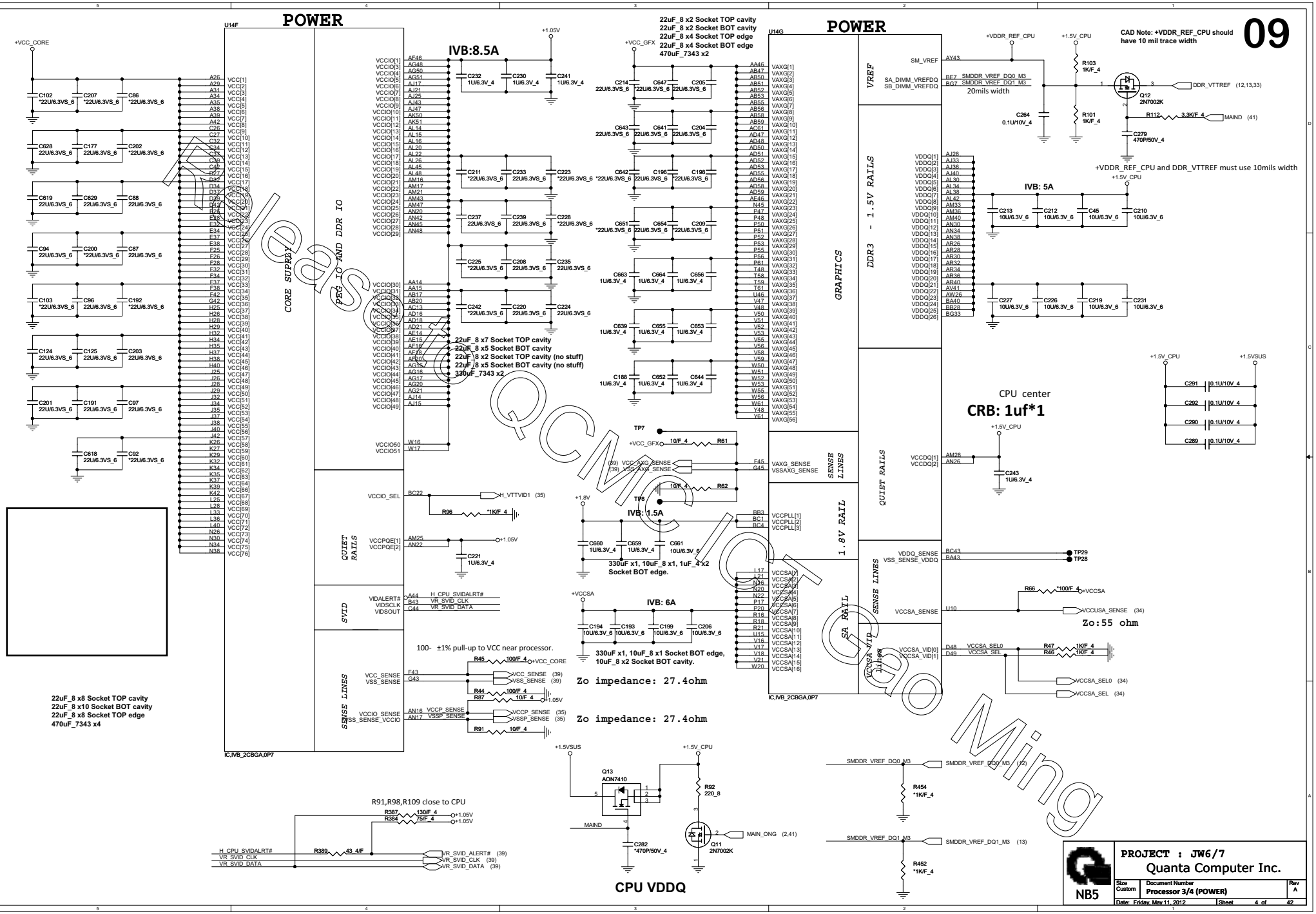
Ivy Bridge Processor (DDR3)



PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Processor 2/5 (DDR3 I/F)	A
Date: Friday, May 11, 2012	Sheet 3 of 42	

NB5


POWER
U14F
CORE SUPPLY
PEG IO AND DDR IO
IVB:8.5A
22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2
22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4
IC,IVB_2CBGA,0P7
QUIET RAILS
SVID
SENSE LINES
100- ±1% pull-up to VCC near processor.
Zo impedance: 27.4ohm
Zo impedance: 27.4ohm
R91,R98,R109 close to CPU
CPU VDDQ
POWER
U14G
GRAPHICS
DDR3 - 1.5V RAILS
VREF
SENSE LINES
1.8V RAIL
QUIET RAILS
SA RAIL
VCCSA VID
22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2
IVB: 1.5A
330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.
IVB: 6A
330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.
IVB: 5A
CRB: 1uf*1
CPU center
CAD Note: +VDDR_REF_CPU should
have 10 mil trace width
20mils width
+VDDR_REF_CPU and DDR_VTTREF must use 10mils width
Zo:55 ohm
IC,IVB_2CBGA,0P7
PROJECT : JW6/7
Quanta Computer Inc.
NB5
Processor 3/4 (POWER)
Size Custom
Rev A
Date: Friday, May 11, 2012
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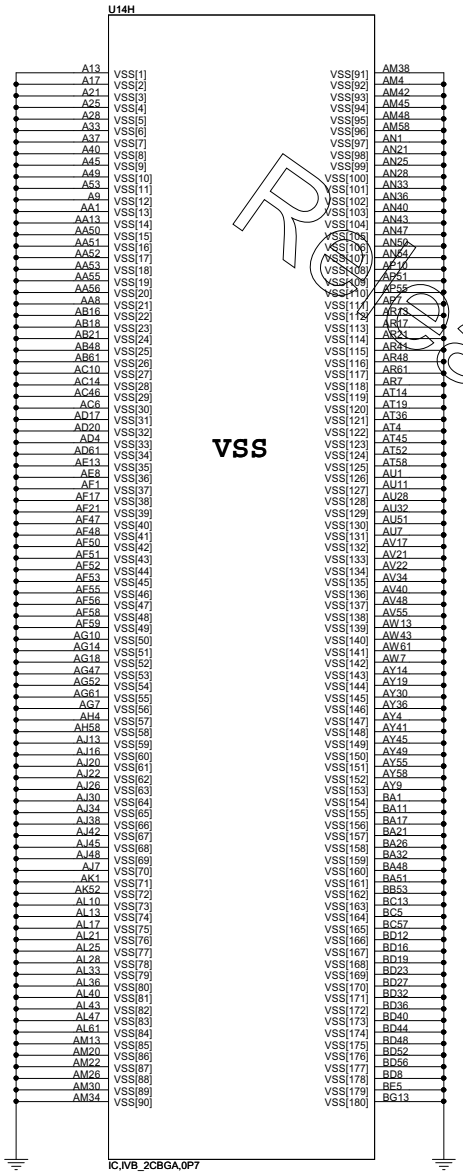
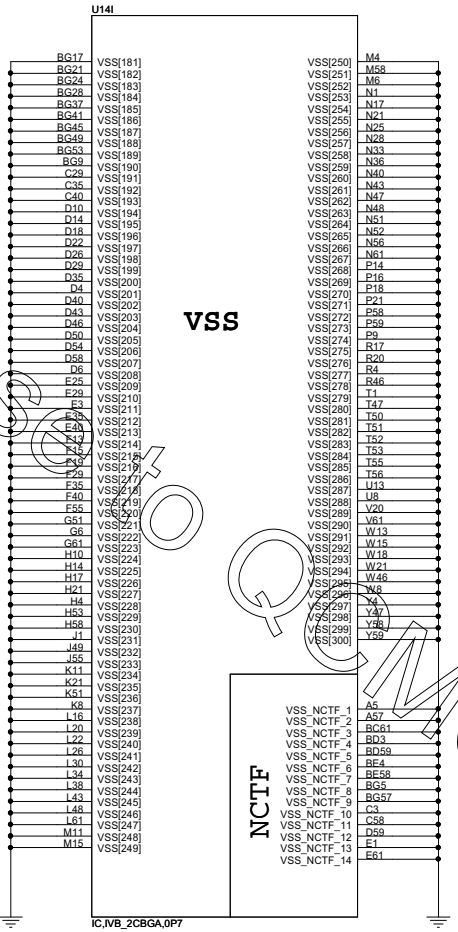
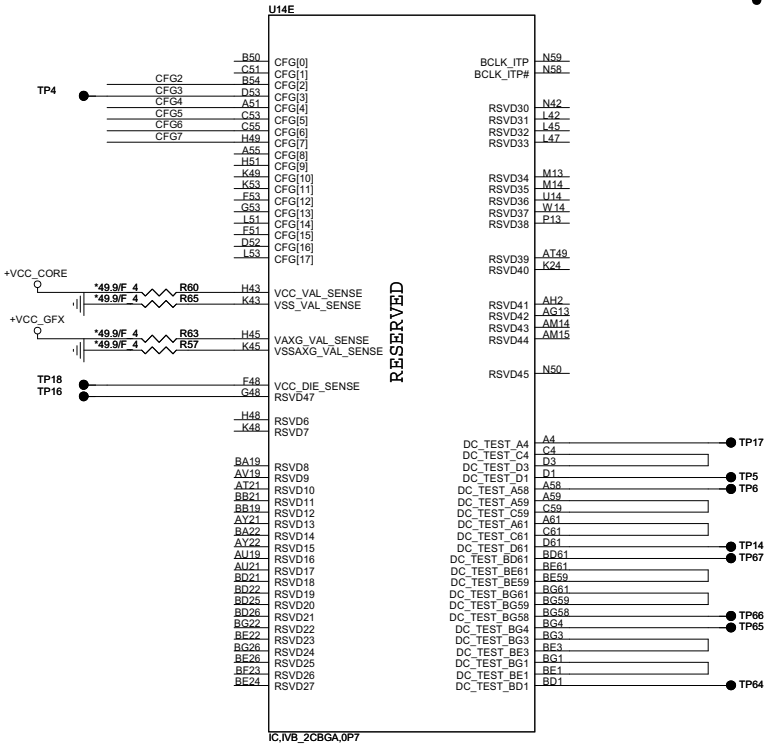
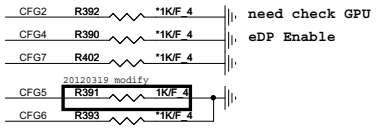
09









CFG[6:5] (PCIE Port Bifurcation Straps)

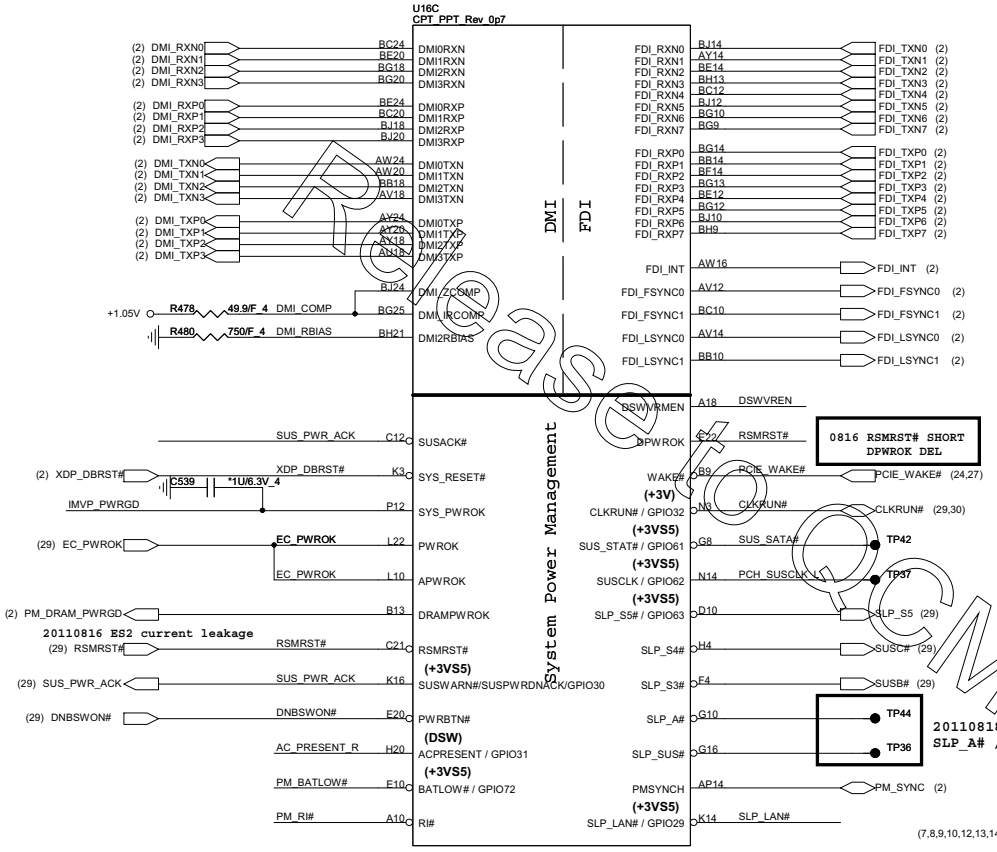
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled , function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

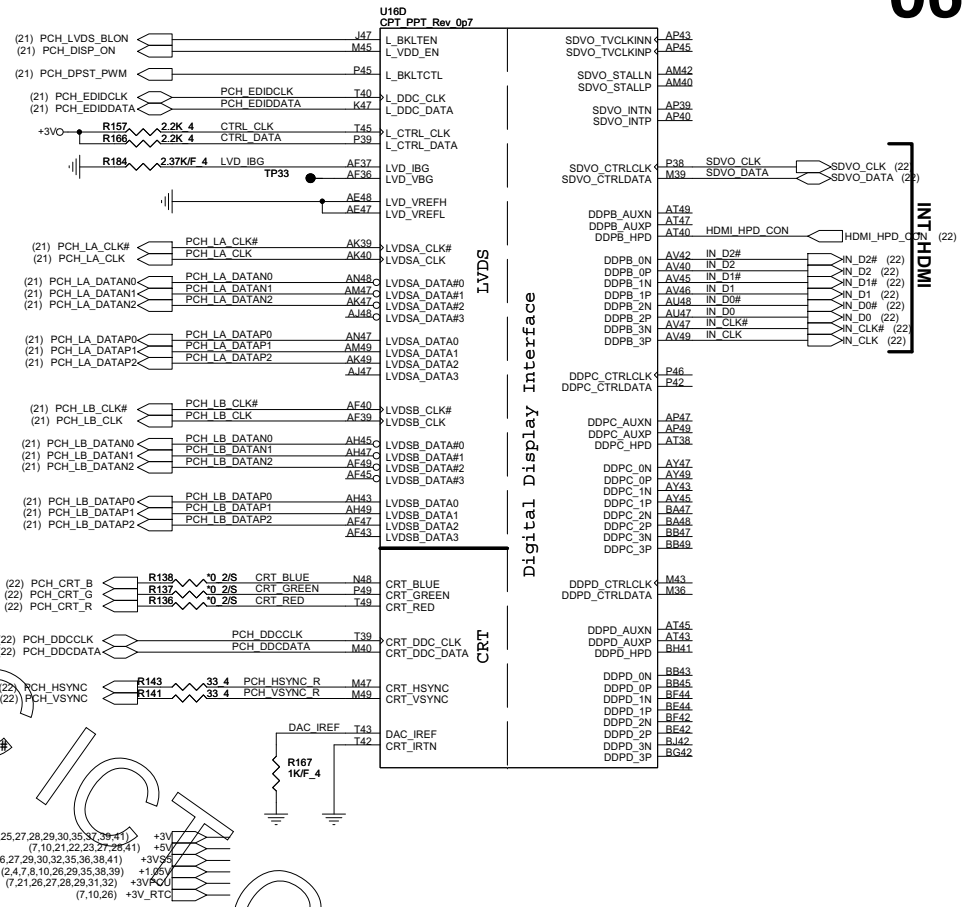
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal.)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

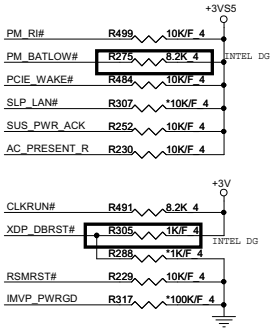
Cougar Point/Panther Point (DMI,FDI,PM)



Cougar Point/Panther Point (LVDS,DDI)

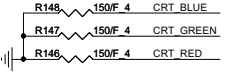


PCH Pull-high/low(CLG)

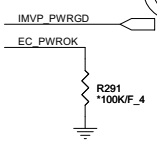


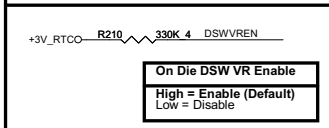
PD Res place close to PCH

PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.



System PWR_OK(CLG)





On Die DSW VR Enable
High = Enable (Default)
Low = Disable

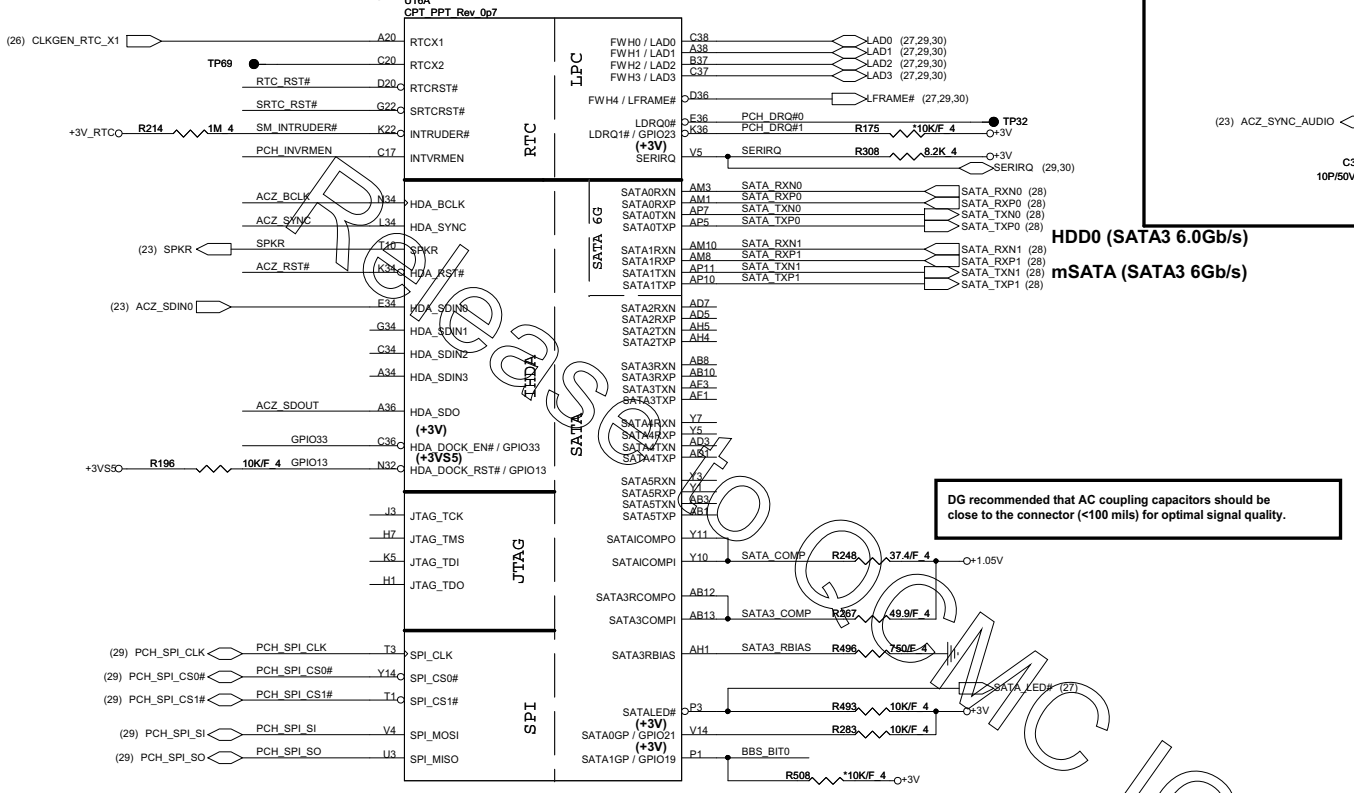
NB5

PROJECT : JW6/7

Quanta Computer Inc.

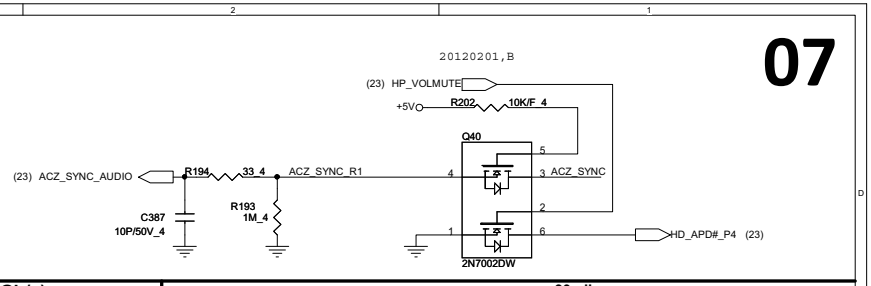
Size	Document Number	Rev
Custom	PCH 1/6 (Host/Display)	A
Date: Monday, May 14, 2012	Sheet 6 of 42	

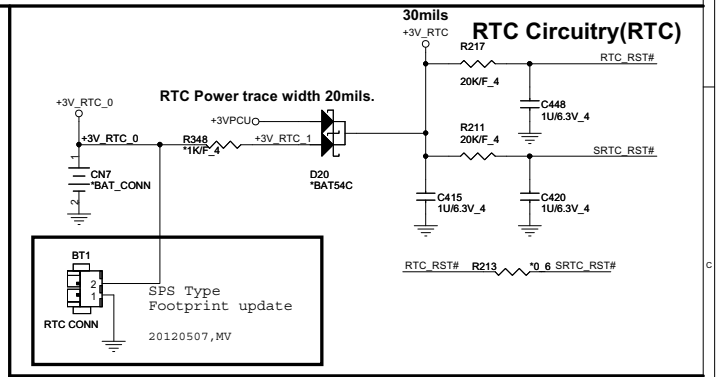
Cougar Point/Panther Point (HDA,JTAG,SATA)

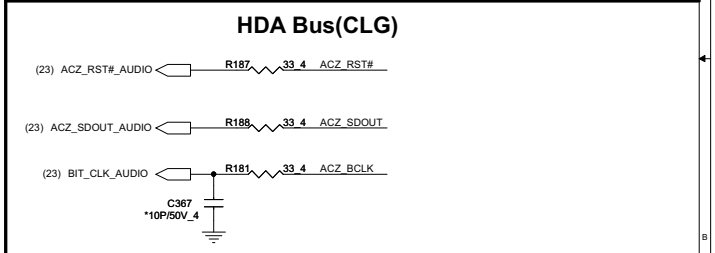


PCH Strap Table

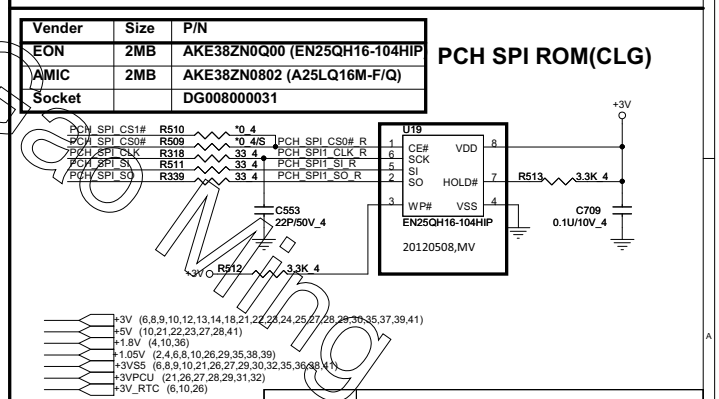
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R286 *1K/F_4 SPKR
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R121 *1K/F_4, R119 10K/F_4 PCI_GNT3# (8)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R223 330K_4 PCH_INVRMEN
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R177 *1K/F_4 ACZ_SDOUT ACZ_SDOUT (29)
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 1 SPI; 1 0 LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1# R492 *1K/F_4 BBS_BIT0; R126 *1K/F_4 BBS_BIT1 (8)
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R262 *1K/F_4 NV_ALE (8)
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm	+1.8V R479 2.2K_4, R477 1K/F_4 DF_TVS (9), H_SNB_IVB# (2)
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R186 1K/F_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	Rising edge of PWROK	1 = Override 0 = Default (weak pull-down 20K)	+3VS5 R182 *1K/F_4 ACZ_SDOUT







Vender	Size	P/N
EON	2MB	AKE38ZN0Q00 (EN25QH16-104HIP
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
Socket		DG008000031



NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: PCH 2/6 (HDA/RTC/SATA/SPI)	Rev: A
Date: Friday, May 11, 2012	Sheet: 7 of 42	

Cougar Point-M/Panther Point (PCI,USB,NVRAM)

Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

08

PCI/USBOC# Pull-up(CLG)

+3V

PCI_PIRQA#	R156	8.2K_4
PCI_PIRQB#	R170	8.2K_4
PCI_PIRQC#	R172	8.2K_4
PCI_PIRQD#	R173	8.2K_4
PCH_GPIO4	R464	10K/F_4
MPC_PWR_CTRL#	R153	10K/F_4
BT_COMBO_EN#	R118	10K/F_4
LCD_BK	R174	10K/F_4
PCH_GPIO52	R9114	8.2K_4
PCH_GPIO54	R9115	8.2K_4

20120327 add

+3VS5

RP5 10K_10P8R_6

USB_OC4#	10 / 1	USB_OC6#
USB_OC1#	9 / 2	USB_OC0#
USB_OC2#	8 / 3	USB_OC7#
USB_OC3#	7 / 4	USB_OC5#
	6 / 5	

USB3.0

20111130 Modify USB3.0 for HM70

(26) USB30_RX1- → USB3Rn1
(26) USB30_RX1+ → USB3Rp1
(26) USB30_TX1- → USB3Tn1
(26) USB30_TX1+ → USB3Tp1

USB2.0 R_down / USB2.0 R_up / Finger Print

USBP0- (26) / USBP0+ (26) — USB3.0
USBP2- (21) / USBP2+ (21) — Camera
USBP9- (23) / USBP9+ (23) — WLAN
USBP10- (27) / USBP10+ (27) — LAN
USBP11- (23) / USBP11+ (23) — Cardreader
USBP12- (30) / USBP12+ (30) — Finger Print

20120131_B

USBRBIAS# C33 — USB_BIAS — R176 22.6/F_4
USBRBIAS B33

PCI

PCI_PIRQA#	K40	PIRQA#
PCI_PIRQB#	K38	PIRQB#
PCI_PIRQC#	H38	PIRQC#
PCI_PIRQD#	G38	PIRQD#
BT_COMBO_EN#	C46	REQ1# / GPIO50 (+3V)
PCH_GPIO52	C44	REQ2# / GPIO52 (+3V)
PCH_GPIO54	E40	REQ3# / GPIO54 (+3V)
(7) BBS_BIT1	D47	GNT1# / GPIO51 (+3V)
(7) PCI_GNT3#	F42	GNT2# / GPIO53 (+3V)
	F46	GNT3# / GPIO55 (+3V)
(21) LCD_BK	G42	PIRQE# / GPIO2 (+3V)
	G40	PIRQF# / GPIO3 (+3V)
	C42	PIRQG# / GPIO4 (+3V)
(30) INTH#	D44	PIRQH# / GPIO5 (+3V)
	K10	PME#
	C6	PLTRST#
(30) CLK_PCI_TPM	H49	CLKOUT_PCI0
CLK_PCI_FB	H43	CLKOUT_PCI1
	J48	CLKOUT_PCI2
CLK_PCI_FB_R	K42	CLKOUT_PCI3
	H40	CLKOUT_PCI4

TP45 — PCI_PME# — PCI_PLTRST# — MPC_PWR_CTRL# — PCH_GPIO4 — INTH# — R155 8.2K_4 — +3V

C713 18P/50V_4 (20120131_B / 20120131_B)

R514 *22_4 CLK_PCI_TPM_R — R469 22_4

R149 22_4 CLK_PCI_LPC_R (27) CLK_33M_DEBUG
R165 22_4 CLK_PCI_EC_R (29) CLK_33M_KBC

C338 18P/50V_4 — C353 18P/50V_4

EMI(near PCH)

USB

USBP0N	C24	USBP0- (26)
USBP0P	A24	USBP0+ (26)
USBP1N	C25	
USBP1P	B25	
USBP2N	C26	USBP2- (21)
USBP2P	A26	USBP2+ (21)
USBP3N	K28	
USBP3P	H28	
USBP4N	E28	
USBP4P	D28	
USBP5N	C28	
USBP5P	A28	
USBP6N	B29	
USBP6P	N28	
USBP7N	M28	
USBP7P	L30	
USBP8N	K30	
USBP8P	G30	USBP9- (23)
USBP9N	E30	USBP9+ (23)
USBP9P	C30	USBP10- (27)
USBP10N	A30	USBP10+ (27)
USBP10P	L32	USBP11- (23)
USBP11N	K32	USBP11+ (23)
USBP11P	G32	USBP12- (30)
USBP12N	E32	USBP12+ (30)
USBP12P	C32	
USBP13N	A32	
USBP13P		

SMBus/Pull-up(CLG)

Q39 2N7002DW

(17,29,30) MBCLK2 → R309 2.2K_4 → +3VS5 → SMB_ME1_CLK
(17,29,30) MBDATA2 → R293 2.2K_4 → SMB_ME1_DAT

PLTRST#(CLG)

PCI_PLTRST# — R486 *0_4/S — PLTRST# — PLTRST# (2,14,24,25,27,29,30)
R501 100K/F_4

Q38 2N7002DW

+3V → R329 4.7K_4 → SMB_RUN_DAT (12,13,28) → SMB_PCH_DAT
+3V → R327 4.7K_4 → SMB_RUN_CLK (12,13,28) → SMB_PCH_CLK

CLK_REQ/Strap Pin(CLG)

PCIE_CLKREQ_LAN#	R506	10K/F_4
PCIE_CLKREQ_CR#	R284	10K/F_4
PCIE_CLKREQ_WLAN#	R488	10K/F_4
CLK_PCIE_REQ3#	R500	10K/F_4
CLK_PCIE_REQ4#	R259	10K/F_4
		Intel DG reques
CLK_PEGB_REQ#	R278	10K/F_4
CLK_PEGA_REQ#	R306	10K/F_4
CLK_PEGA_REQ#	R290	*10K/F_4
CLK_PEGB_REQ#	R279	*10K/F_4
CLK_BUF_BCLK_N	R475	10K/F_4
CLK_BUF_BCLK_P	R476	10K/F_4
CLK_BUF_PCIE_3GPLL#	R219	10K/F_4
CLK_BUF_PCIE_3GPLL	R227	10K/F_4
CLK_BUF_DREFCLK#	R206	10K/F_4
CLK_BUF_DREFCLK	R207	10K/F_4
CLK_BUF_DREFSSCLK#	R282	10K/F_4
CLK_BUF_DREFSSCLK	R281	10K/F_4
CLK_PCH_14M	R151	10K/F_4

CLOCK TERMINATION for FCIM

WLAN / LAN / Cardreader

(27) PCIE_RXN1 → C362 0.1U/10V_4 → PCIE_TXN1_C → PERN1
(27) PCIE_RXP1 → C363 0.1U/10V_4 → PCIE_TXP1_C → PERP1
(27) PCIE_TXN1 → PETN1
(27) PCIE_TXP1 → PETP1

(24) PCIE_RXN2_LAN → C411 0.1U/10V_4 → PCIE_TXN2_LAN_C → PERN2
(24) PCIE_RXP2_LAN → C410 0.1U/10V_4 → PCIE_TXP2_LAN_C → PERP2
(24) PCIE_TXN2_LAN → PETN2
(24) PCIE_TXP2_LAN → PETP2

(25) PCIE_RXN3_CR → C516 0.1U/10V_4 → PCIE_TXN3_CR_C → PERN3
(25) PCIE_RXP3_CR → C517 0.1U/10V_4 → PCIE_TXP3_CR_C → PERP3
(25) PCIE_TXN3_CR → PETN3
(25) PCIE_TXP3_CR → PETP3

MPC Switch Control

MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R154 *1K/F_4

PCI-E*

PERN1	BG34	
PERP1	BJ34	
PETN1	AV32	
PETP1	AU32	
PERN2	BE34	
PERP2	BF34	
PETN2	BB32	
PETP2	AY32	
PERN3	BG36	
PERP3	BJ36	
PETN3	AV34	
PETP3	AU34	
PERN4	BF36	
PERP4	BE36	
PETN4	AY34	
PETP4	BB34	
PERN5	BG37	
PERP5	BH37	
PETN5	AY36	
PETP5	BB36	
PERN6	BJ38	
PERP6	BG38	
PETN6	AU36	
PETP6	AV36	
PERN7	BG40	
PERP7	BJ40	
PETN7	AY40	
PETP7	BB40	
PERN8	BE38	
PERP8	BC38	
PETN8	AW38	
PETP8	AY38	

SMBUS

(+3VS5) SMBALERT# / GPIO11 E12 — SMBALERT# R51 *0_4 — SMB_INT# (28)
SMBCLK H14 — SMB_PCH_CLK — SMB_PCH_CLK (28)
SMBDATA C9 — SMB_PCH_DAT — SMB_PCH_DAT (28)

(+3VS5) SML0ALERT# / GPIO60 A12 — DRAMRST_CNTRL_PCH — DRAMRST_CNTRL_PCH (2,12,13)
SML0CLK C8 — SMB_ME0_CLK
SML0DATA G12 — SMB_ME0_DAT

(+3VS5) SML1ALERT# / PCHHOT# / GPIO74 C13 — SML1ALERT#_R — TP40
(+3VS5) SML1CLK / GPIO58 E14 — SMB_ME1_CLK
(+3VS5) SML1DATA / GPIO75 M16 — SMB_ME1_DAT

Controller Link

CL_CLK1 M7
CL_DATA1 T11
CL_RST1# P10

CLOCKS

(+3VS5) PEG_A_CLKRQ# / GPIO47 M10 — CLK_PEGA_REQ# — CLK_PEGA_REQ# (14)

CLK_PCIE_WLANN Y40 — CLKOUT_PCIE0N
CLK_PCIE_WLANP Y39 — CLKOUT_PCIE0P
PCIE_CLKREQ_WLAN# J2 — PCIECLKRQ0# / GPIO73

(+3VS5)
CLK_PCIE_LANN AB49 — CLKOUT_PCIE1N
CLK_PCIE_LANP AB47 — CLKOUT_PCIE1P
PCIE_CLKREQ_LAN# M1 — PCIECLKRQ1# / GPIO18

(+3V)
CLK_PCIE_CRN AA48 — CLKOUT_PCIE2N
CLK_PCIE_CRP AA47 — CLKOUT_PCIE2P
PCIE_CLKREQ_CR# V10 — PCIECLKRQ2# / GPIO20

(+3V)
Y37 — CLKOUT_PCIE3N
Y36 — CLKOUT_PCIE3P
CLK_PCIE_REQ3# A8 — PCIECLKRQ3# / GPIO25

(+3VS5)
Y43 — CLKOUT_PCIE4N
Y45 — CLKOUT_PCIE4P
CLK_PCIE_REQ4# L12 — PCIECLKRQ4# / GPIO26

(+3VS5)
V45 — CLKOUT_PCIE5N
V46 — CLKOUT_PCIE5P
(9) BOARD_ID0 L14 — PCIECLKRQ5# / GPIO44

(+3VS5)
AB42 — CLKOUT_PEG_B_N
AB40 — CLKOUT_PEG_B_P
CLK_PEGB_REQ# F6 — PEG_B_CLKRQ# / GPIO56

(+3VS5)
V40 — CLKOUT_PCIE6N
V42 — CLKOUT_PCIE6P
(27) INT_BT_COMBO_EN# T13 — PCIECLKRQ6# / GPIO45

(+3VS5)
V38 — CLKOUT_PCIE7N
V37 — CLKOUT_PCIE7P
(9) BOARD_ID2 K12 — PCIECLKRQ7# / GPIO46

(+3VS5)
AK14 — CLKOUT_ITPXDP_N
AK13 — CLKOUT_ITPXDP_P

FLEX CLOCKS

(+3VS5)
CLK_CPU_BCLKN (2) — CLKOUT_DMI_N AV22
CLK_CPU_BCLKP (2) — CLKOUT_DMI_P AU22

CLKOUT_DP_N AM12 — CLK_DPLL_SSCLKN_R
CLKOUT_DP_P AM13 — CLK_DPLL_SSCLKP_R — TP39 TP38 — 0809 CLK_SSCLK DEL

CLKIN_DMI_N BF18 — CLK_BUF_PCIE_3GPLL#
CLKIN_DMI_P BE18 — CLK_BUF_PCIE_3GPLL

CLKIN_GND1_N BJ30 — CLK_BUF_BCLK_N
CLKIN_GND1_P BG30 — CLK_BUF_BCLK_P

CLKIN_DOT_96N G24 — CLK_BUF_DREFCLK#
CLKIN_DOT_96P E24 — CLK_BUF_DREFCLK

CLKIN_SATA_N AK7 — CLK_BUF_DREFSSCLK#
CLKIN_SATA_P AK5 — CLK_BUF_DREFSSCLK

REFCLK14IN K45 — CLK_PCH_14M
CLKIN_PCILOOPBACK H45 — CLK_PCI_FB

XTAL25_IN V47
XTAL25_OUT V49 — TP68 — PCH_XTAL25_IN (26)

XCLK_RCOMP Y47 — XCLK_RCOMP R472 90.9/F_4 — +1.05V

(+3V)
CLKOUTFLEX0 / GPIO64 K43
CLKOUTFLEX1 / GPIO65 F47
CLKOUTFLEX2 / GPIO66 H47
CLKOUTFLEX3 / GPIO67 K49

PCIE Clock

WLAN: (27) CLK_PCIE_WLANN / (27) CLK_PCIE_WLANP / (27) PCIE_CLKREQ_WLAN# → CLK_PCIE_WLANN / CLK_PCIE_WLANP / PCIE_CLKREQ_WLAN#
LAN: (24) CLK_PCIE_LANN / (24) CLK_PCIE_LANP / (24) PCIE_CLKREQ_LAN# → CLK_PCIE_LANN / CLK_PCIE_LANP / PCIE_CLKREQ_LAN#
GPU: (14) CLK_PCIE_VGA# / (14) CLK_PCIE_VGA → CLK_PCIE_VGA# / CLK_PCIE_VGA
Cardreader: (25) CLK_PCIE_CRN / (25) CLK_PCIE_CRP / (25) PCIE_CLKREQ_CR# → CLK_PCIE_CRN / CLK_PCIE_CRP / PCIE_CLKREQ_CR#

(6,7,9,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41) +3V
(6,7,9,10,21,26,27,29,30,32,35,36,38,41) +3VS5

SMBus/Pull-up(CLG)

+3VS5

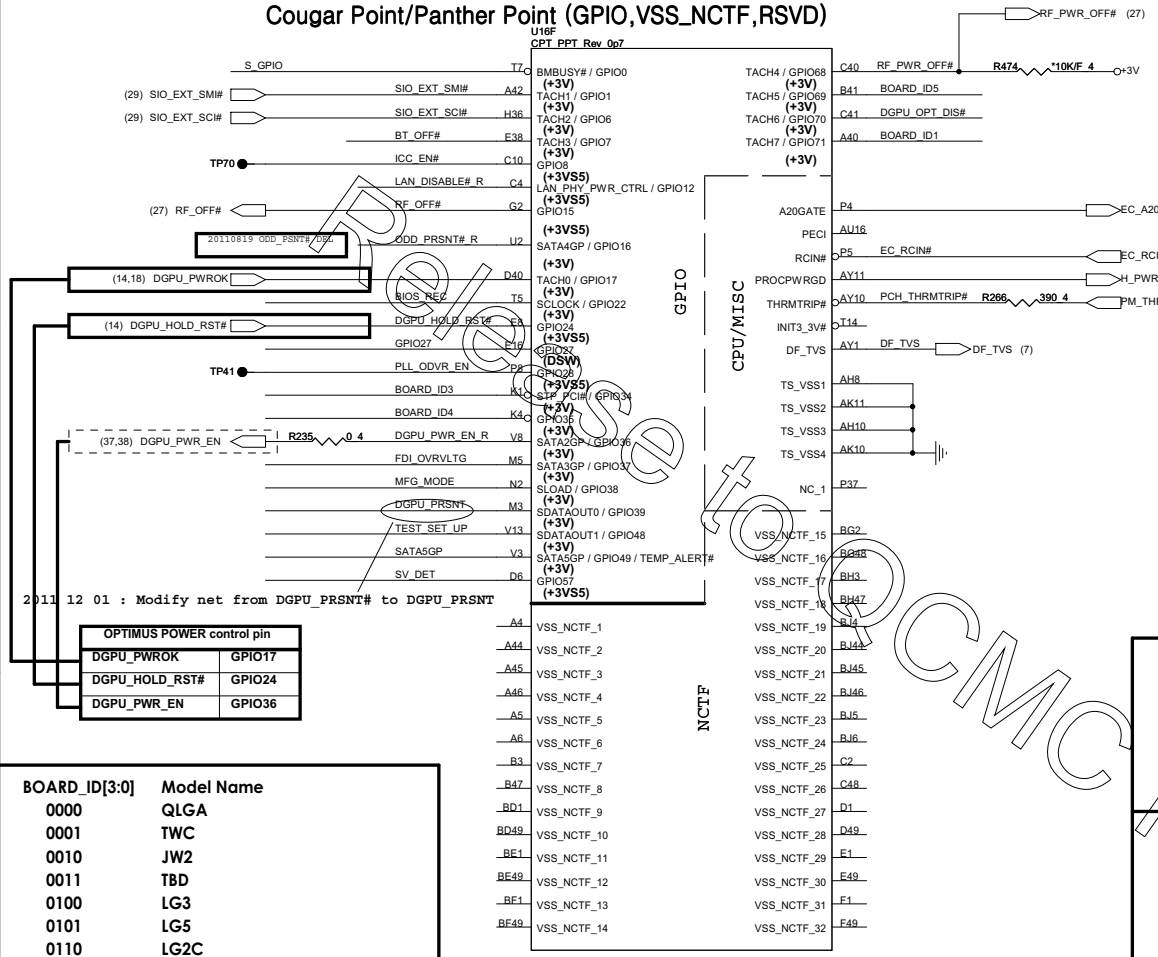
R498	1K/F_4	DRAMRST_CNTRL_PCH
R270	10K/F_4	SMBALERT#
R292	2.2K_4	SMB_PCH_CLK
R296	2.2K_4	SMB_PCH_DAT
R485	2.2K_4	SMB_ME0_CLK
R260	2.2K_4	SMB_ME0_DAT
R251	10K/F_4	SML1ALERT#_R

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/6 (Clock/PCI/PCIE/USB)	A
Date: Friday, May 11, 2012	Sheet 8 of 42	

Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



2011 12 01 : Modify net from DGPU_PRSNT# to DGPU_PRSNT

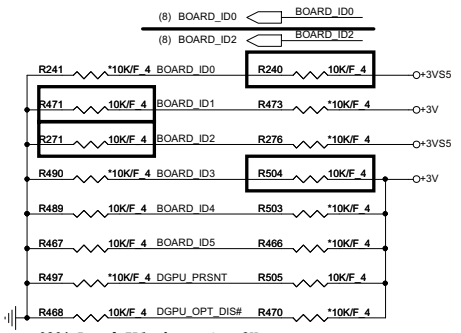
OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

BOARD_ID[3:0]	Model Name
0000	QLGA
0001	TWC
0010	JW2
0011	TBD
0100	LG3
0101	LG5
0110	LG2C
0111	LG4C
1000	TBD
1001	JW6/JW7
1010	JW3
1011	JW6H/JW6L
1100	JW3H

Chief River BOARD ID SETTING

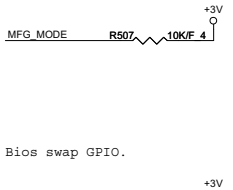
BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
~~BOARD_ID3~~	~~GPIO34~~	~~MODEL BIT3~~
BOARD_ID4	GPIO35	Reserve and pull low
BOARD_ID5	GPIO69	HM77=0,HM70=1
DGPU_PRSNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

20110816 Define BRD_ID[3:0]

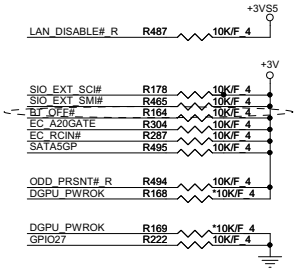


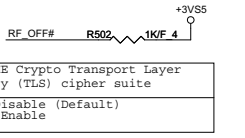
0804 Board_ID1 change to +3V
Board_ID5 change to +3V

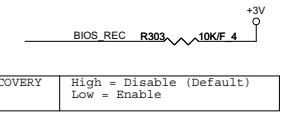
MFG-TEST

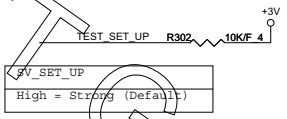


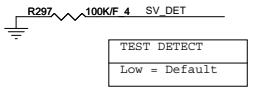
GPIO Pull-up/Pull-down(CLG)

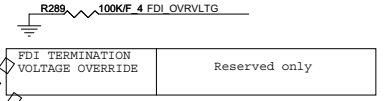












(6,7,8,10,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41) +3V
(6,7,8,10,21,26,27,29,30,32,35,36,38,41) +3VS5

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO)	A
Date: Tuesday, May 15, 2012	Sheet 9 of 42	

Cougar Point/Panther Point (POWER)

Cougar Point/Panther Point (POWER)

U16J CPT_PPT_Rev_0p7 POWER

U16G CPT_PPT_Rev_0p7 POWER

Clock and Miscellaneous | USB | PCI/GPIO/LPC | SATA | MISC | CPU | RTC | HDA

VCC CORE | CRT | LVDS | HVCMOS | VCCIO | DMI | DFT / SPI | FDI

3mA (10mils) | VCCASW:803mA (40mils) | 1mA (10mils) | 119mA (15mils) | 266mA (20mils) | 70mA | 350mA | 30mA | 1.01A (60mils) | 10mA (10mils) | V_PROC_IO=2mA (10mils) | VCCRTC<1mA (10mils)

VCCCore:1.73 A (100mils) | 6.3mA (10mils) | 1mA (10mils) | 60mA (10mils) | SG & UMA : Ra DIS : Rb | VCCIO:3.799 A (140mils) | 42mA (10mils) | 178m A (20mils) | (Mobile 1.5V) | 160mA (15mils) | 2 mA (10mils) | 10mA (10mils) | 20mA (10mils) | V5REF= 1mA | VCC5REFSUS=1mA

PROJECT : JW6/7

Quanta Computer Inc.

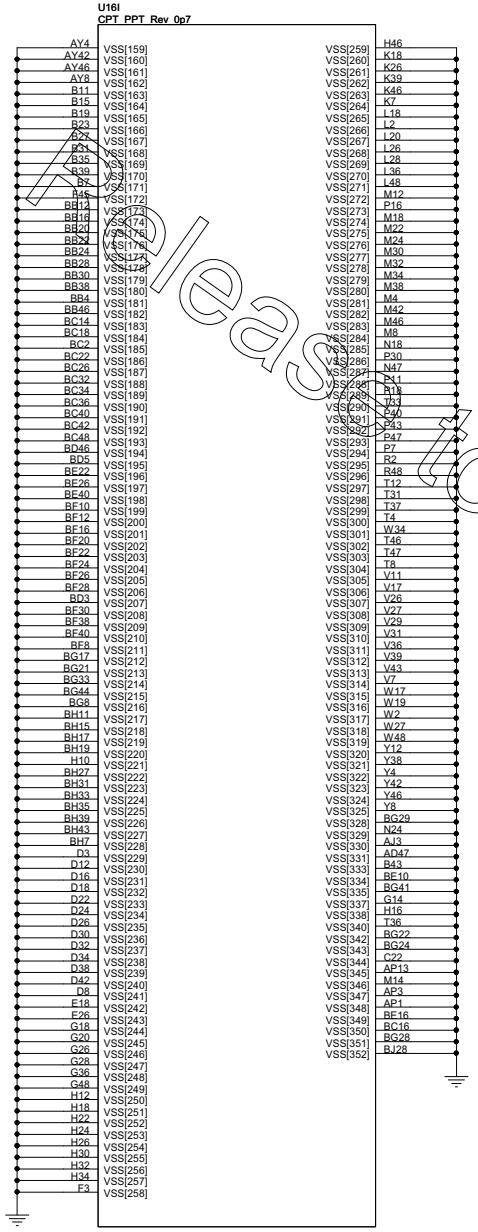
NB5

PCH 5/6 (Power)

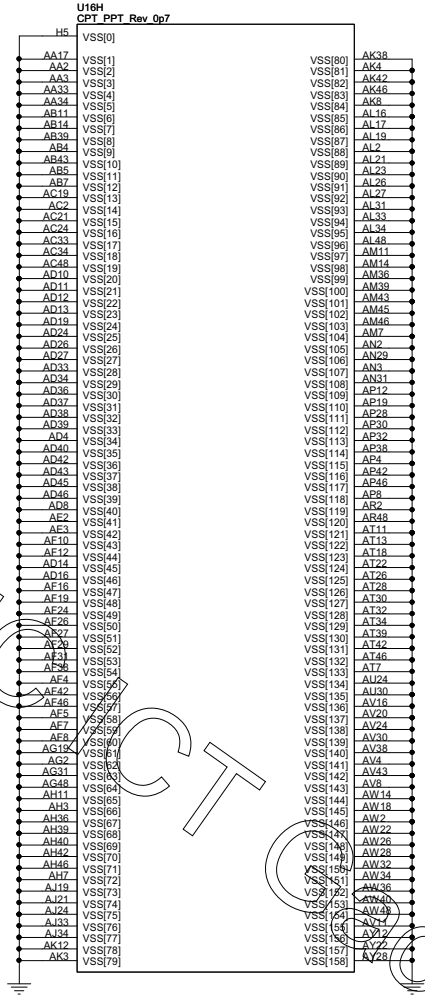
Size: Custom | Document Number | Rev: A

Date: Friday, May 11, 2012 | Sheet 10 of 42

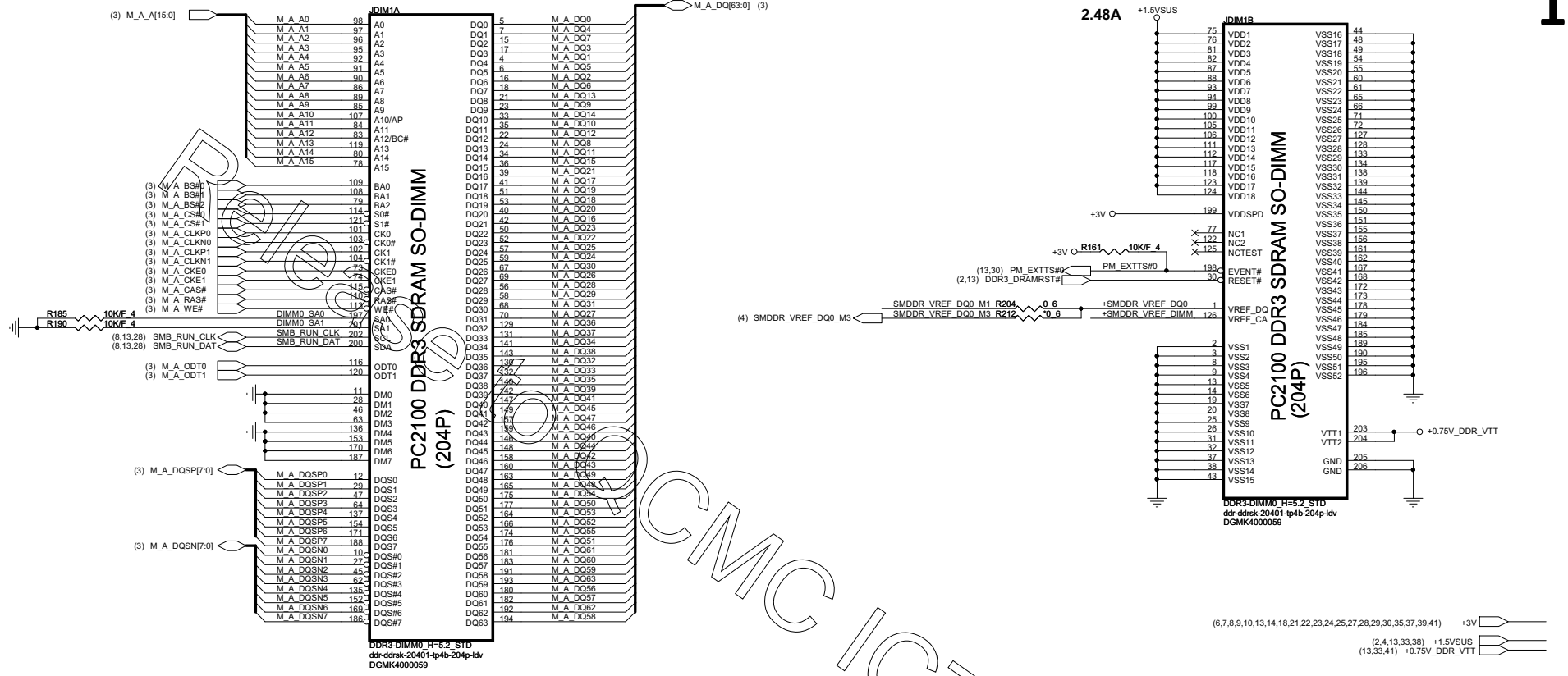
Cougar Point/Panther Point (GND)



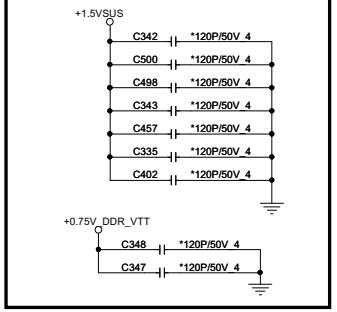
Cougar Point/Panther Point (GND)



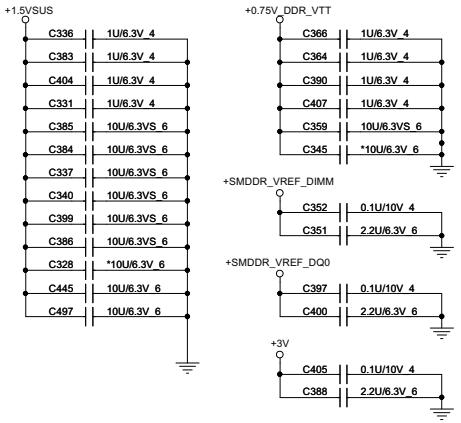
NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: PCH 6/6 (Ground)	Rev: A
Date: Friday, May 11, 2012	Sheet: 11of 42	



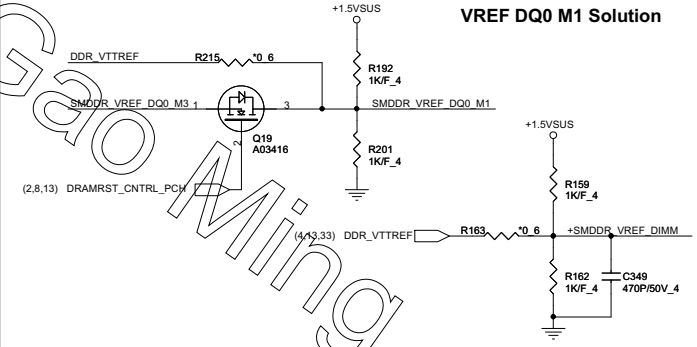
For EMI RESERVE 8/30



Place these Caps near So-Dimm0.



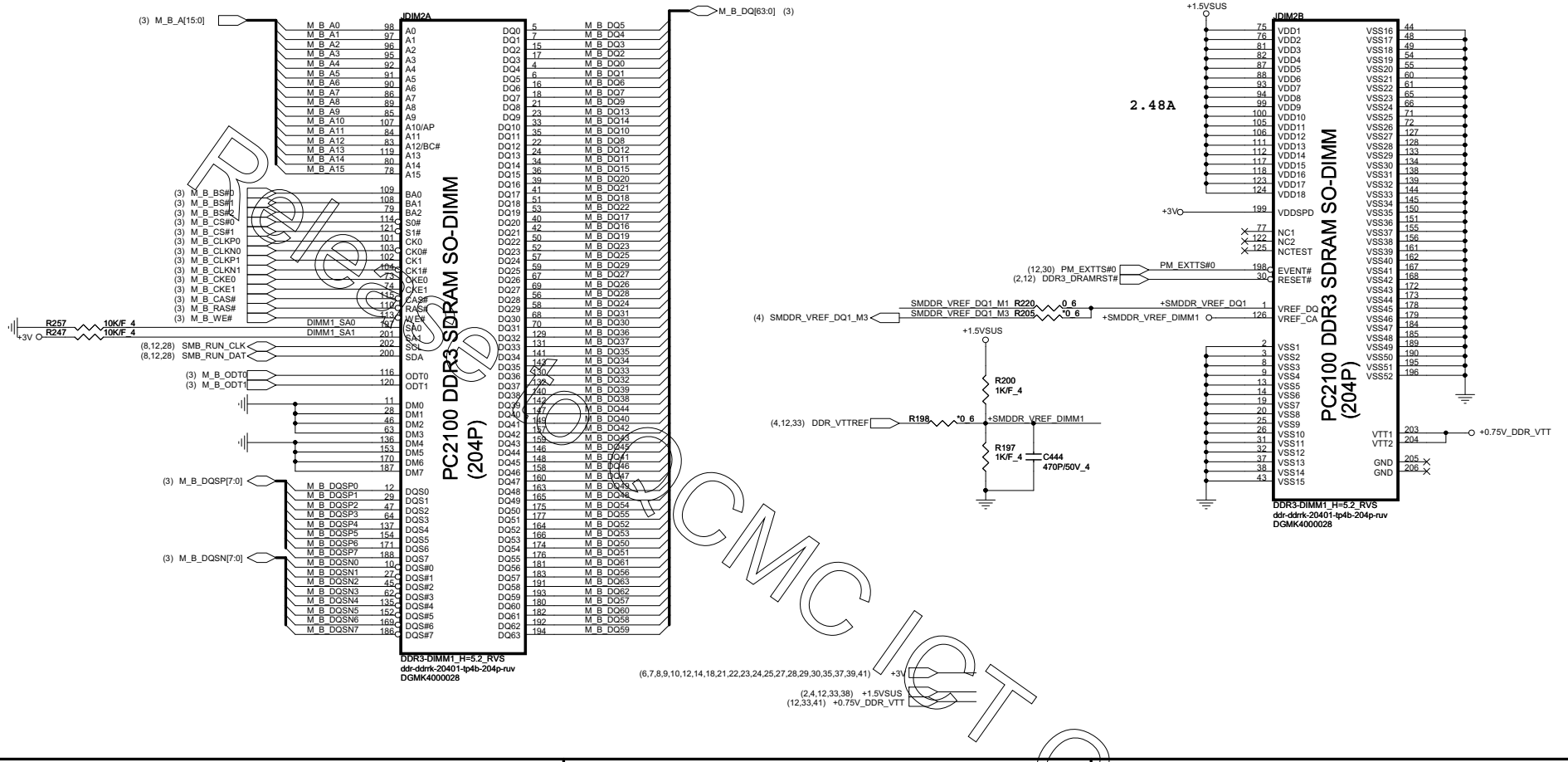
VREF DQ0 M1 Solution



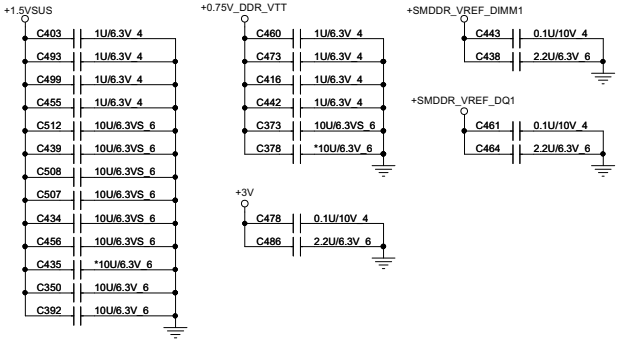
PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 1/2 (5.2H)	A
Date: Friday, May 11, 2012	Sheet 12of 42	

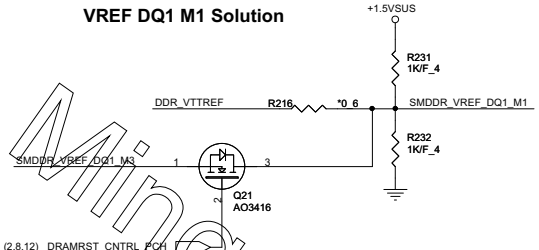
NB5



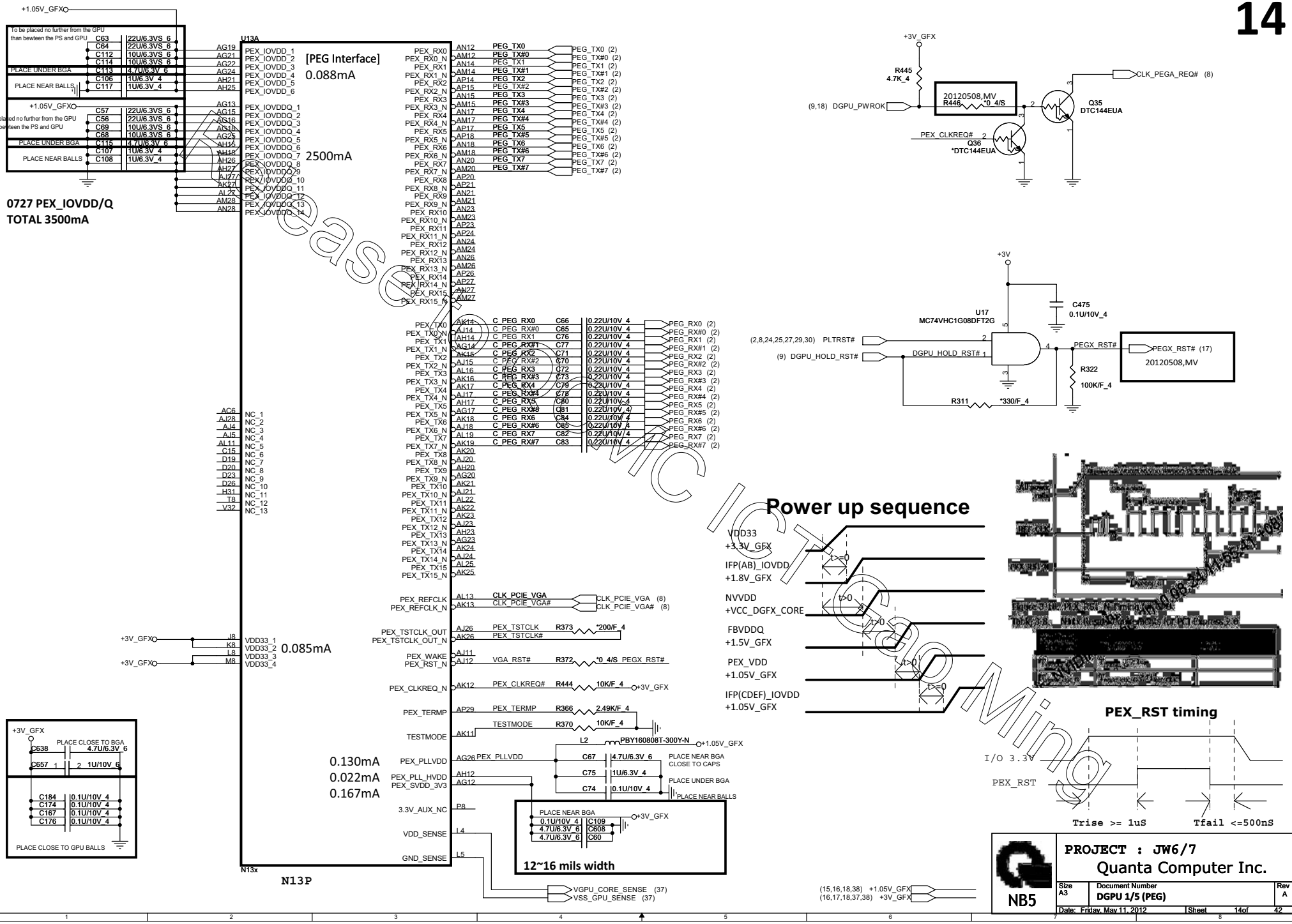
Place these Caps near So-Dimm1.

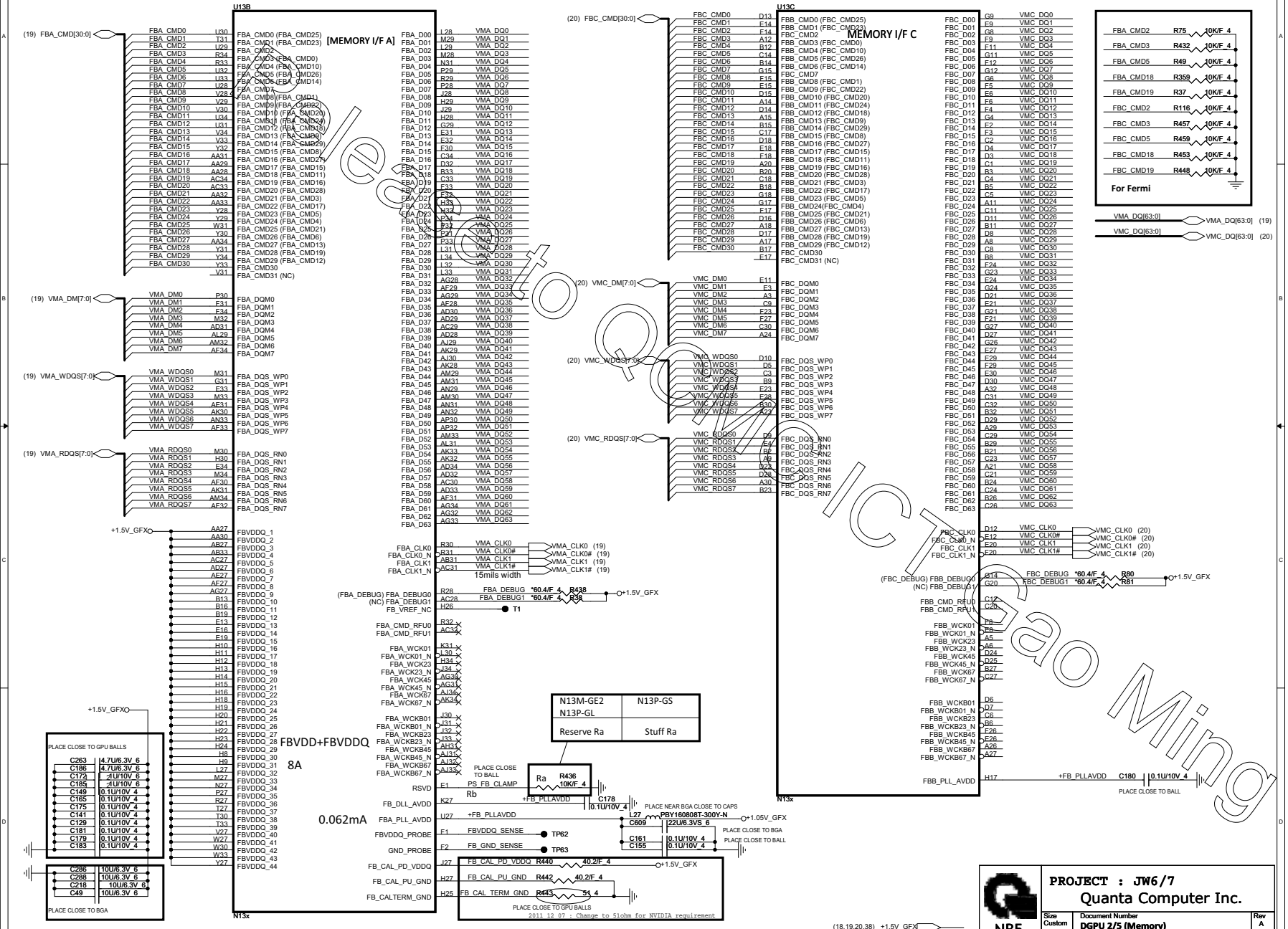


VREF DQ1 M1 Solution



NB5	PROJECT : JW6/7 Quanta Computer Inc.	
	Size: Custom Document Number: System Memory 2/2 (9.2H)	Rev: A
	Date: Friday, May 11, 2012	Sheet 13 of 42




U13B
[MEMORY I/F A]
U13C
MEMORY I/F C
For Fermi
FBVDDQ+FBVDDQ
8A
0.062mA
N13M-GE2 N13P-GS
N13P-GL
Reserve Ra Stuff Ra
PLACE CLOSE TO GPU BALLS
PLACE CLOSE TO BGA
PLACE CLOSE TO BALL
PLACE NEAR BGA CLOSE TO CAPS
PLACE CLOSE TO BGA
15mils width
2011 12 07 : Change to 51ohm for NVIDIA requirement
N13x
PROJECT : JW6/7
Quanta Computer Inc.
NB5
DGPU 2/5 (Memory)
Date: Friday, May 11, 2012
Sheet 15of 42

(14,15,18,38) +1.05V_GFX
(14,17,18,37,38) +3V_GFX

0824 Update Symbol

U13D

[IFPA/B_LVDS]
IFPAB_PLLVDD AH8 (R364 10K/F_4)
IFPAB_IOVDD AG8
IFPA_IOVDD
IFPB_IOVDD AG9 (R362 10K/F_4)
IFPAB_RSET AJ8 (R363 *1K/F_4)
IFPA_TXC AM6
IFPA_TXC_N AN6
IFPA_TXD0 AP3
IFPA_TXD0_N AN3
IFPA_TXD1 AN5
IFPA_TXD1_N AM5
IFPA_TXD2 AL6
IFPA_TXD2_N AK6
IFPA_TXD3 AJ6
IFPA_TXD3_N AH6
IFPB_TXC AJ9
IFPB_TXC_N AH9
IFPB_TXD4 AP6
IFPB_TXD4_N AP5
IFPB_TXD5 AM7
IFPB_TXD5_N AL7
IFPB_TXD6 AN8
IFPB_TXD6_N AM8
IFPB_TXD7 AK8
IFPB_TXD7_N AL8

[IFPC/D_TMDS]
IFPC_PLLVDD AF7
IFPD_PLLVDD AG7 (R378 10K/F_4 IFPCD_PLLVDD)
IFPC_IOVDD AF6
IFPD_IOVDD AG6 (R377 10K/F_4 IFPCD_IOVDD)
IFPC_RSET AF8 (R365 *1K/F_4)
IFPD_RSET AN2
IFPC_AUX_I2CW_SCL AG3
IFPC_AUX_I2CW_SDA_N AG2
IFPC_L0 AK1
IFPC_L0_N AJ1
IFPC_L1 AJ3
IFPC_L1_N AJ2
IFPC_L2 AH3
IFPC_L2_N AH4
IFPC_L3 AG5
IFPC_L3_N AG4
IFPD_AUX_I2CX_SCL AK3
IFPD_AUX_I2CX_SDA_N AK2
IFPD_L0 AM1
IFPD_L0_N AM2
IFPD_L1 AM3
IFPD_L1_N AM4
IFPD_L2 AL3
IFPD_L2_N AL4
IFPD_L3 AK4
IFPD_L3_N AK5

[IFPE/F_DP]
IFPEF_PLLVDD AB8 (R381 10K/F_4 IFPEF_PLLVDD)
IFPE_IOVDD AC7
IFPF_IOVDD AC8 (R379 10K/F_4 IFPEF_IOVDD)
IFPEF_RSET AD6
IFPE_AUX_I2CY_SCL AB3
IFPE_AUX_I2CY_SDA_N AB4
IFPE_L0 AD2
IFPE_L0_N AD1
IFPE_L1 AC1
IFPE_L1_N AC2
IFPE_L2 AC3
IFPE_L2_N AC4
IFPE_L3 AC5
IFPE_L3_N
IFPF_AUX_I2CZ_SCL AF3
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_L0 AE3
IFPF_L0_N AE4
IFPF_L1 AF4
IFPF_L1_N AF5
IFPF_L2 AD4
IFPF_L2_N AD5
IFPF_L3 AG1
IFPF_L3_N AF1

[DACA/B_CRT]
DACA_VDD AG10 (R361 10K/F_4 DACA_VDD)
DACA_VREF AP9 (T3)
DACA_RSET AP8 (T2)
DACA_RED AK9
DACA_GREEN AL10
DACA_BLUE AL9
DACA_HSYNC AM9
DACA_VSYNC AN9
I2CA_SCL R4 I2CA_SCL R59 2.2K_4 +3V_GFX
I2CA_SDA R5 I2CA_SDA R64 2.2K_4 +3V_GFX

+1.05V_GFX L28 PBY160808T-300Y-N NV_PLLVDD AD8
PLLVDD 0.052mA
C625 22U/6.3VS_6
C624 0.1U/10V_4
AE8
SP_PLLVDD 0.067mA
PLACE CLOSE TO GPU
AD7
0.041mA
VID_PLLVDD
C150 C135
C130 22U/6.3VS_6 4.7U/6.3V_6 0.1U/10V_4
PLACE CLOSE TO BALLS
within 150mils

[XTAL IN]
XTAL_IN H3 CLK_27M_XTAL_IN
XTAL_OUT H2 CLK_27M_XTAL_OUT
XTAL_OUTBUFF J4 R67 10K/F_4
XTAL_SSIN H1 R427 10K/F_4
Y2 27MHZ +-10PPM
C197 12P/50V_4
C190 12P/50V_4
20120328,Change to 12pf

N13x

NB5	PROJECT : JW6/7	
	Quanta Computer Inc.	
	Size A3 / Document Number: DGPU 3/5 (Display)	Rev A
	Date: Friday, May 11, 2012 / Sheet 16 of 42	

Net name	N13M-GE2	N13P-GS(QS)
ROM_SI		
ROM_SO	PD 10K	PU 10K
ROM_SCLK	PD 15K	PU 5K
STRAP0	PU 45K	PU 45K
STRAP1	PD 45K	PD 5K
STRAP2	PU 15K	PD 15K
STRAP3	UN-STUFF	PD 5K
STRAP4	UN-STUFF	PD 45K

Net name	N13P-GL
ROM_SI	
ROM_SO	PD 10K
ROM_SCLK	PD 15K
STRAP0	PU 45K
STRAP1	PD 5K
STRAP2	PU 10K
STRAP3	UN-STUFF
STRAP4	UN-STUFF

For N13M-GE2
ROM_SO PD 10K
ROM_SCLK PD 15K

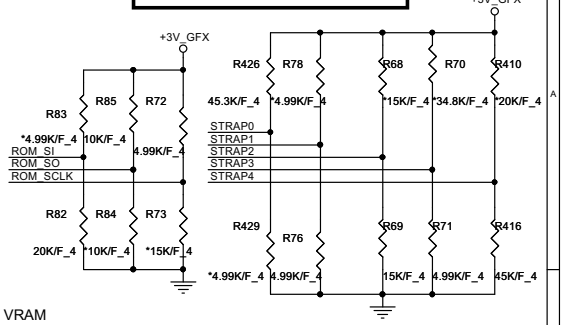
For N13P-GS
ROM_SO PU 10K
ROM_SCLK PU 5K

N13M-GE2-A1 ID:0X0DEA
N13P-GS ID:0X0FD2
N13P-GL-A1 ID:0X0DE9

17

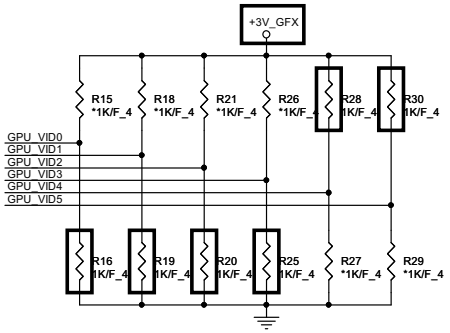
Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



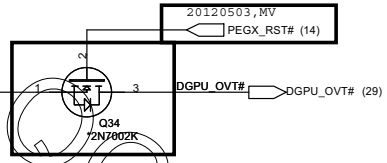
Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0011
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0111
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	XXXX
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	XXXX



VID 0 0 0 0 0 1 1 0 ---> 0.9V N13P-GS-A2

VID 0 0 1 1 0 1 0 ---> 0.95V N13P-GL-A1



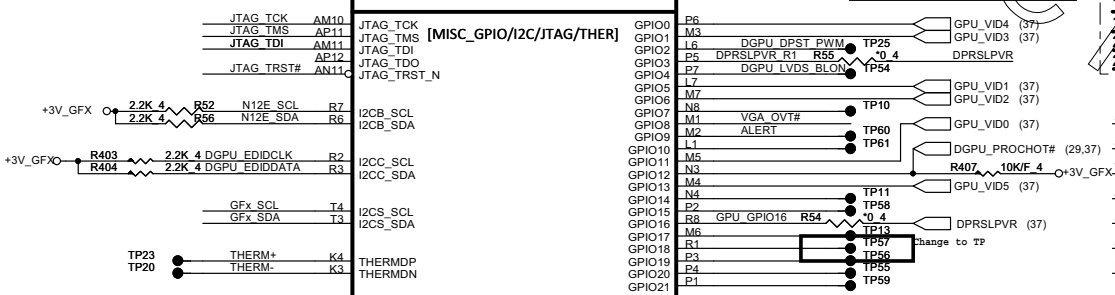
	N13M-GE2	N13P-GS
Ra	Un-Stuff	Stuff
Qa	Stuff	Un-Stuff

For N13M-GE2, N13M-GS (QS)
Defult : 2G Samsung

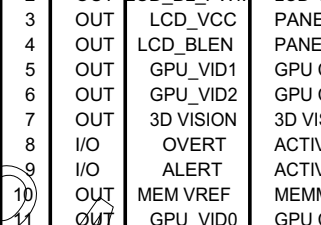
VRAM Configuration Table

ROM_SI

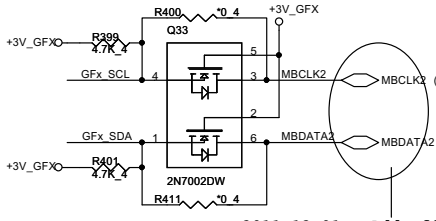
1G Hynix 64Mx16 -->15K PD
1G Samsung 64Mx16 -->20K PD
2G Hynix 128Mx16 -->35K PD
2G Samsung 128Mx16 -->45K PD



	N13M-GE2 N13P-GL	N13P-GS
	Stuff Rc	Un-stuff Rc



GFx SMBus Isolation * *



2011 12 01 : Add off-page connector

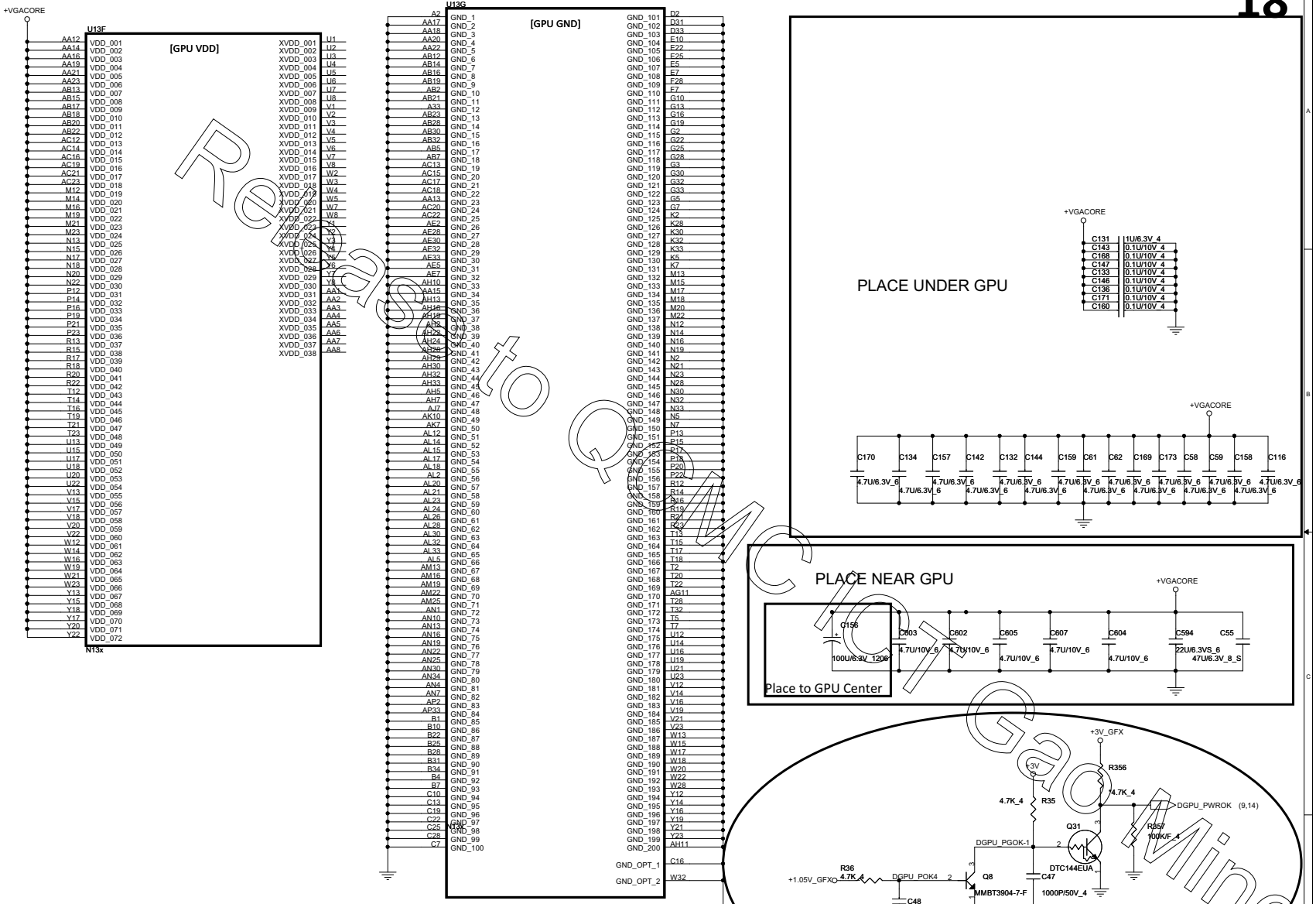
GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU 4/5 (MIO/GPIO)	A
Date: Tuesday, May 15, 2012	Sheet 17of 42	



PROJECT :	JW6/7
Quanta Computer Inc.	
Size: Custom	Document Number: DGPU 5/5 (Power/Ground)
Rev: A	
Date: Friday, May 11, 2012	Sheet: 18 of 42

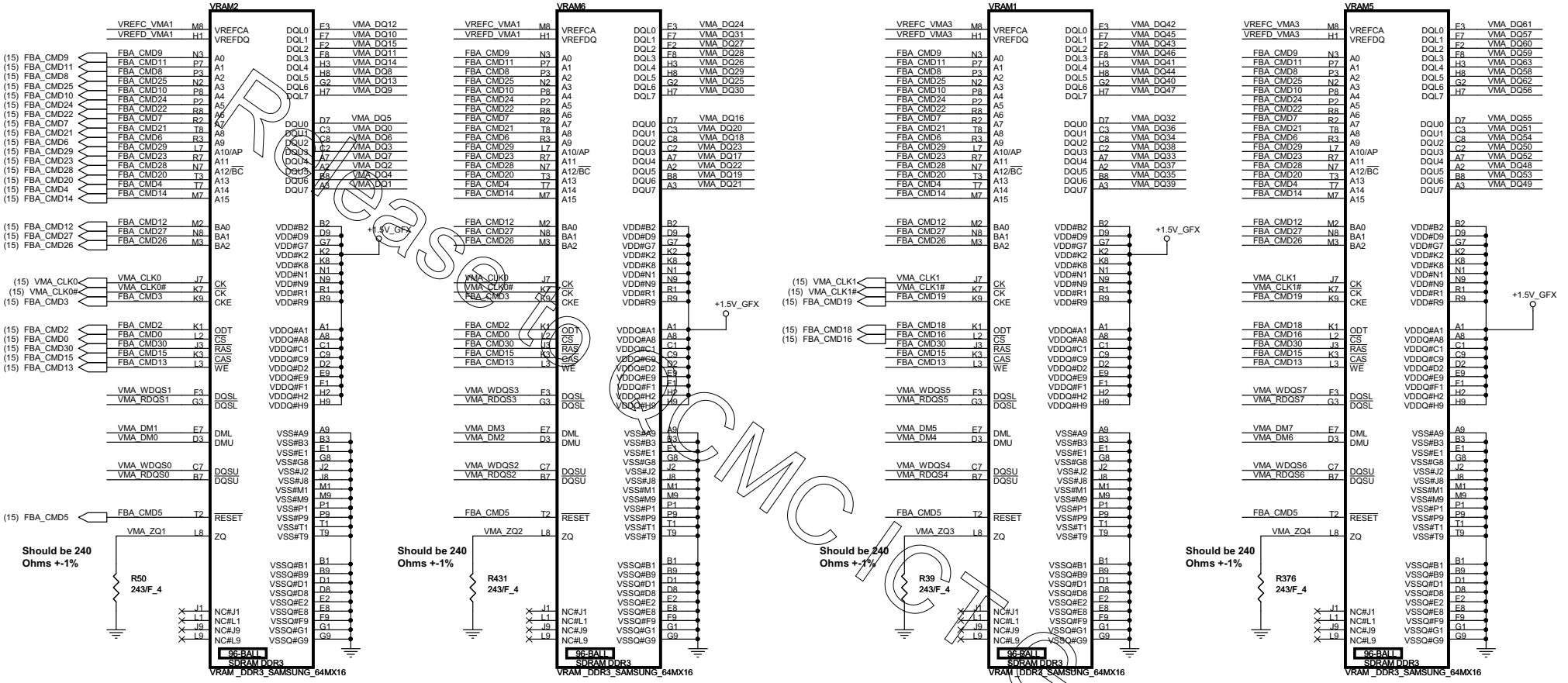
NB5

(37) +VGACORE
(14,15,16,38) +1.05V_GFX
(15,19,20,38) +1.5V_GFX
(14,16,17,37,38) +3V_GFX
(6,7,8,9,10,12,13,14,21,22,23,24,25,27,28,29,30,35,37,39,41) +3V

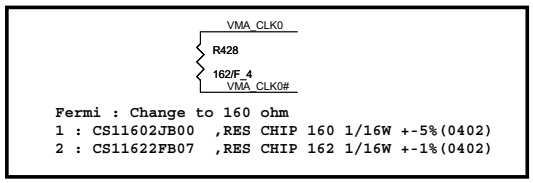
CHANNEL A: 256MB/512MB DDR3

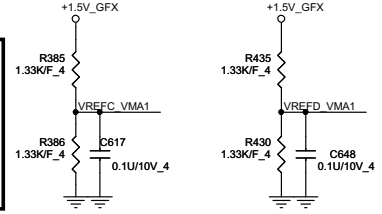
(15) VMA_DQ[63..0]
(15) VMA_DM[7..0]
(15) VMA_WDQS[7..0]
(15) VMA_RDQS[7..0]

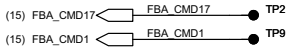
900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00



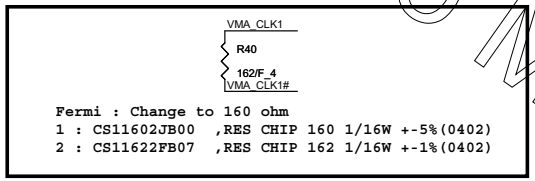
Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

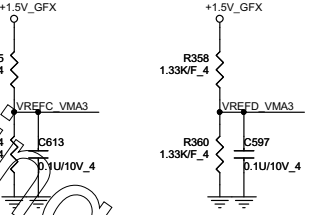


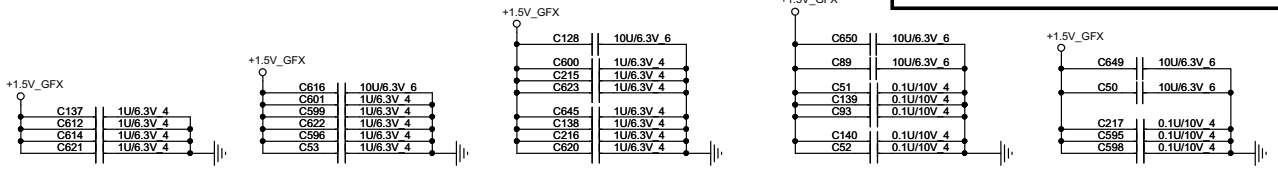




Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)







(15,18,20,38) +1.5V_GFX

NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: DGPU Memory 1/2 (DDR3)	Rev: 1A
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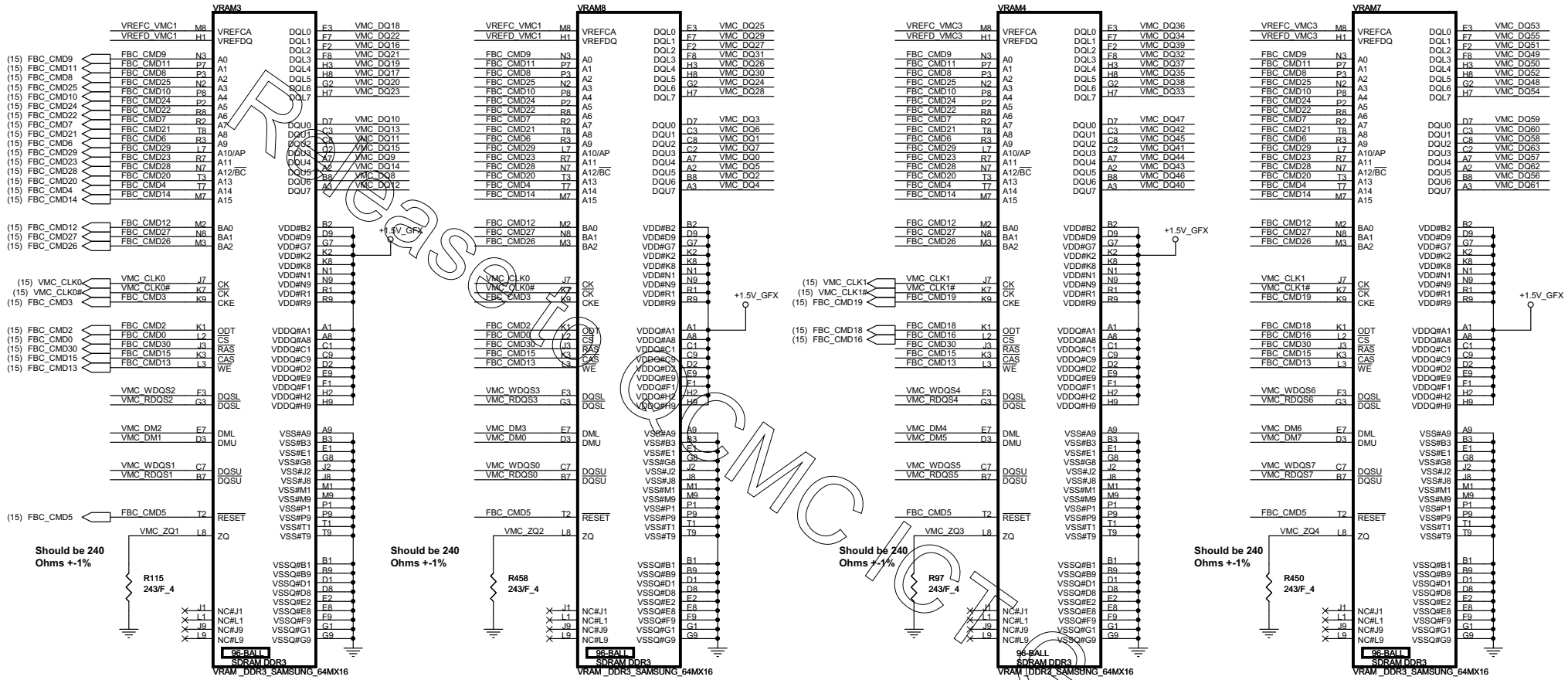
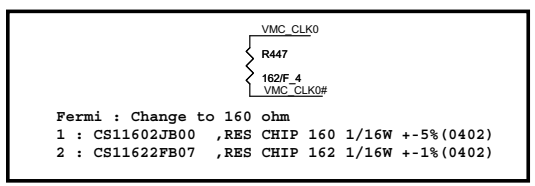
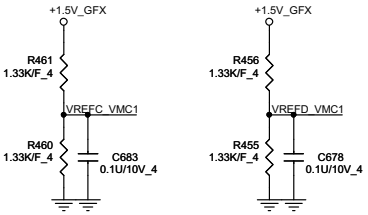
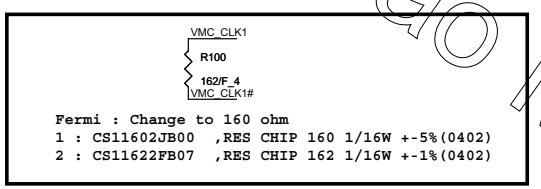
CHANNEL B: 256MB/512MB DDR3

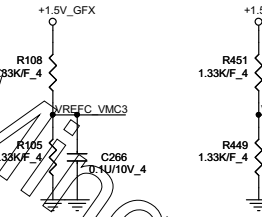
(15) VMC_DQ[63..0]
(15) VMC_DM[7..0]
(15) VMC_WDQS[7..0]
(15) VMC_RDQS[7..0]

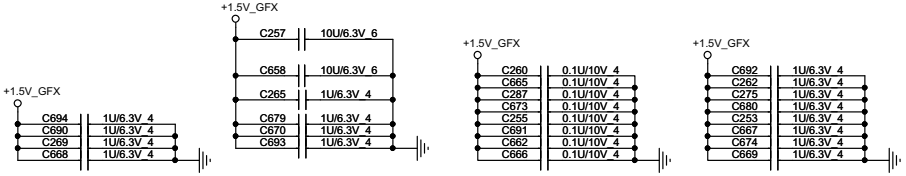












(15) FBC_CMD17 — FBC_CMD17 — TP26
(15) FBC_CMD1 — FBC_CMD1 — TP27

900MHz VRAM size:
Samsung 64Mx16, P/N = AKD5EGGT500
Samsung 128Mx16, P/N = AKD5MGWT500
Hynix 64Mx16, P/N = AKD5LZWTW02
Hynix 128Mx16, P/N = AKD5MGWTW00

(15,18,19,38) +1.5V_GFX

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DGPU Memory 2/2 (DDR3)	1A
Date: Friday, May 11, 2012	Sheet 20 of 42	

USB Camera Connector

MIC

(23) DIGITAL_D1 — L26 FCM1608KF-301T02 DIGITAL_D1_R
(23) DIGITAL_CLK — L25 FCM1608KF-301T02 DIGITAL_CLK_R

C582 100P/50V_4
C581 100P/50V_4
EMI request

(8) USBP2-
(8) USBP2+
CAMERA
L1 *WCM2012-90
USBP2-
USBP2+

C33	*10P/50V_4	USBP2-
C40	*10P/50V_4	USBP2+
C589	33P/50V_4	DIGITAL_D1
C588	33P/50V_4	DIGITAL_CLK

Change from +5V to +3V
+3V — C38 0.01U/16V_4
C587 *4.7U/6.3V_6

+3V — R24 2.2K_4 — R23 2.2K_4
(6) PCH_EDIDCLK — PCH_EDIDCLK
(6) PCH_EDIDDATA — PCH_EDIDDATA

+3V — C586 1U/6.3V_4
U10 IC(5P) G5243AT11U: IN, IN, ON/OFF, OUT, GND
+LCDVCC
+3VLCD_CON
L22 *0_6/S 20120314 modify
C39 *10U/6.3V_6
C36 *0.1U/16V_4
C35 0.1U/10V_4
(6) PCH_DISP_ON — PCH_DISP_ON
R351 100K/F_4

CN1 H=2.0
+3VLCD_CON — C37 1000P/50V_4
+3V
PCH_EDIDCLK
PCH_EDIDDATA
(6) PCH_LA_DATAN0 — PCH_LA_DATAN0
(6) PCH_LA_DATAP0 — PCH_LA_DATAP0
(6) PCH_LA_DATAN1 — PCH_LA_DATAN1
(6) PCH_LA_DATAP1 — PCH_LA_DATAP1
(6) PCH_LA_DATAN2 — PCH_LA_DATAN2
(6) PCH_LA_DATAP2 — PCH_LA_DATAP2
(6) PCH_LA_CLK# — PCH_LA_CLK#
(6) PCH_LA_CLK — PCH_LA_CLK
(6) PCH_LB_DATAN0 — PCH_LB_DATAN0
(6) PCH_LB_DATAP0 — PCH_LB_DATAP0
(6) PCH_LB_DATAN1 — PCH_LB_DATAN1
(6) PCH_LB_DATAP1 — PCH_LB_DATAP1
(6) PCH_LB_DATAN2 — PCH_LB_DATAN2
(6) PCH_LB_DATAP2 — PCH_LB_DATAP2
(6) PCH_LB_CLK# — PCH_LB_CLK#
(6) PCH_LB_CLK — PCH_LB_CLK
DIGITAL_D1_R
DIGITAL_CLK_R
Change from +5V to +3V
+3V — USBP2-
USBP2+
(6) PCH_DPST_PWM — R353 1K/F_4 — PCH_DPST_PWM_R
C584 22P/50V_4
BLON_CON
+VIN_BLIGHT
GS12407-11141-9F

(29) LID_CONTROL — LID_CONTROL — D21 RB500V-40 — BLON_CON
R352 100K/F_4
C583 22P/50V_4
R350 47K/F_4 — +3VPCU
(6) PCH_LVDS_BLON — PCH_LVDS_BLON — R354 1K/F_4 — D22 *RB500V-40 — LID_EC# (28,29)
R355 100K/F_4
(8) LCD_BK — Q30 *DTC144EUA

+VIN_BLIGHT
+VIN — L24 *TI160808U600 — L23 *0_6/S 20120314 modify — +VIN_BLIGHT
C580 0.1U/50V_6
C585 *4.7U/25V_8
C590 0.1U/50V_6
C591 0.01U/25V_4

EMI/ESD

Stitching Cap(each 1" place one cap)

+5V: C148 C54 C449 C267 C576 C566 — 0.1U/10V_4
+3VS5: C551 C358 C548 C529 C537 C540 — 0.1U/10V_4
+3V: C195 C339 C249 C309 C522 C513 — 0.1U/10V_4
+5V: C570 C261 C406 C567 C569 C189 — 0.1U/10V_4
+5VS5
+3VS5: C560 C554 C357 C562 C563 C703 — 0.1U/10V_4
+5VS5

(6,7,8,9,10,12,13,14,18,22,23,24,25,27,28,29,30,35,37,39,41) +3V
(7,26,27,28,29,31,32) +3VPCU
(7,10,22,23,27,28,41) +5V
(31,32,33,35,37,38,40,41) +VIN
(38,41) +12VALW
(10,23,26,32,33,34,35,37,39,40,41) +5VS5

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	A

Date: Friday, May 11, 2012 | Sheet 21of 42

CRT PORT

40 MIL

40 mils F1 FUSE1A6V_POLY +5V +5VCRT +5VCRT
C145 0.1U/10V_4
SSM14 spec is 40V 1A

(6) PCH_CRT_R
(6) PCH_CRT_G
(6) PCH_CRT_B
20120505,MV
L5 SBK160808T-680Y-N
L4 SBK160808T-680Y-N
L3 SBK160808T-680Y-N
CRT_R_CON
CRT_G_CON
CRT_B_CON
+5VCRT
CRT CONN CN12

R58 150/F_4 R53 150/F_4 R48 150/F_4
C182 6.8P/50V_4 C164 6.8P/50V_4 C127 6.8P/50V_4
C126 6.8P/50V_4 C166 6.8P/50V_4 C187 6.8P/50V_4
EMI

C611 .1U/10V_4
(6) PCH_VSYNC PCH_VSYNC
U11 M74VHC1GT125DF2G
(6) PCH_HSYNC PCH_HSYNC
U12 M74VHC1GT125DF2G

CRTVSYNC1 R380 *0_4/S CRTVSYNC2
CRTHSYNC1 R396 *0_4/S CRTHSYNC2
R43 *0_4/S DDCCLK3
R405 *0_4/S DDCDAT3

C90 *470P/50V_4 C615 *47P/50V_6 C630 *470P/50V_4 C631 *47P/50V_6

R42 10K/F_4 R415 10K/F_4
(6) PCH_DDCCLK
(6) PCH_DDCDATA
Q42 2N7002DW
DDCCLK2 DDCDATA2
20120201,B
R41 2.2K_4 R397 2.2K_4
D25 RB500V-40 +5VCRT +5V_CRT2

PCH_CRT_R PCH_CRT_G PCH_CRT_B DDCCLK3 DDCDAT3 CRTHSYNC2 CRTVSYNC2
D5 *BAV99W D4 *BAV99W D3 *BAV99W D2 *BAV99W D28 *BAV99W D27 *BAV99W D26 *BAV99W

inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect

HDMI PORT

HDMI SMBus Isolation

R171 2.2K_4 Q17
(6) SDVO_CLK HDMI_SCL_R HDMI_SCLK
(6) SDVO_DATA HDMI_SDA_R HDMI_SDATA
R189 2.2K_4
2N7002DW
Close to HDMI connector

EMI Solution

C_TX2_HDMI+ R150 100/F_4 C_TX2_HDMI-
C_TX1_HDMI+ R133 100/F_4 C_TX1_HDMI-
C_TX0_HDMI+ R139 100/F_4 C_TX0_HDMI-
C_IN_CLK R125 100/F_4 C_IN_CLK#
C_IN_CLK# R122 *0_4/S C_TXC_HDMI-
C_IN_CLK R127 *0_4/S C_TXC_HDMI+
20120508,MV

(6) IN_D2 IN_D2 C341 0.1U/10V_4 C_TX2_HDMI+
(6) IN_D2# IN_D2# C332 0.1U/10V_4 C_TX2_HDMI-
(6) IN_D1 IN_D1 C323 0.1U/10V_4 C_TX1_HDMI+
(6) IN_D1# IN_D1# C319 0.1U/10V_4 C_TX1_HDMI-
(6) IN_D0 IN_D0 C327 0.1U/10V_4 C_TX0_HDMI+
(6) IN_D0# IN_D0# C324 0.1U/10V_4 C_TX0_HDMI-
(6) IN_CLK IN_CLK C315 0.1U/10V_4 C_IN_CLK C_TXC_HDMI+
(6) IN_CLK# IN_CLK# C310 0.1U/10V_4 C_IN_CLK# C_TXC_HDMI-
RB500V-40
+5V D8 D7 RB500V-40
5V_HSMBCK R131 2.2K_4
5V_HSMBDT R130 2.2K_4
HDMI_SCLK HDMI_SDATA
C311 *10P/50V_4 C312 *10P/50V_4
+5VCRT
HDMI_HPD R117 *0_4/S HDMI_DET_C
C302 220P/50V_4
D6 *BAV99W +5V
20120423,MV
R124 110K/F_4
B-stage change

CN16
SHELL3 SHELL1 22 20
1 D2+
2 D2 Shield
3 D2-
4 D1+
5 D1 Shield
6 D1-
7 D0+
8 D0 Shield
9 D0-
10 CK+
11 CK Shield
12 CK-
13 CE Remote
14 NC
15 DDC CLK
16 DDC DATA
17 GND
18 +5V
19 HP DET
SHELL2 SHELL4 21 23
HDMI CONN_4 pin GND
add for EMI

DGPU_CL_HDMIP
R152 510/F_4 C_TX2_HDMI+
R144 510/F_4 C_TX2_HDMI-
R134 510/F_4 C_TX1_HDMI+
R132 510/F_4 C_TX1_HDMI-
R142 510/F_4 C_TX0_HDMI+
R135 510/F_4 C_TX0_HDMI-
R128 510/F_4 C_IN_CLK
R123 510/F_4 C_IN_CLK#
R179 100K/F_4 Q16 2N7002K
C354 0.1U/10V_4
Close to Q24

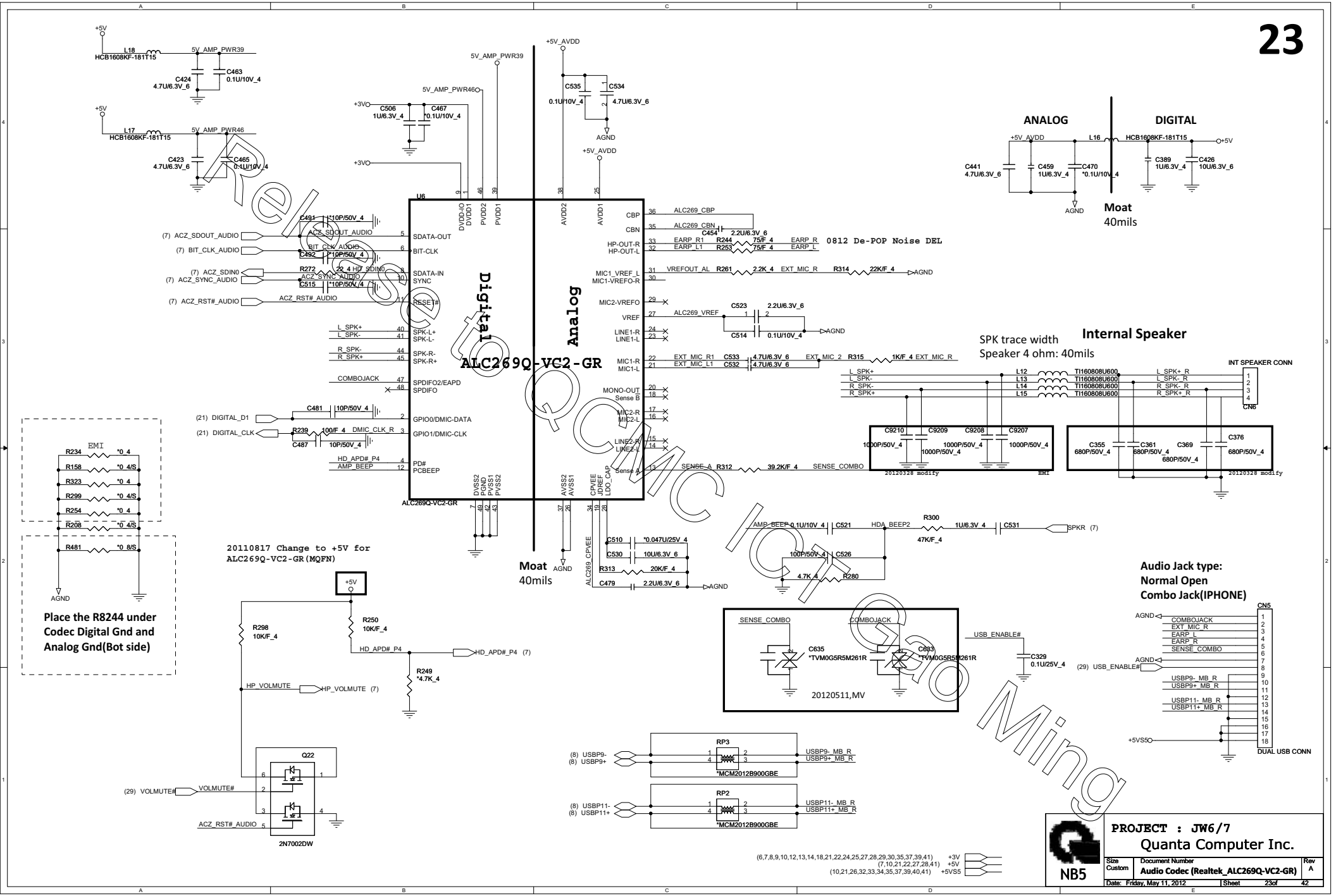
Q14 MMBT3904-7-F R120 150K/F_4
HDMI_DET_P HDMI_HPD
(6) HDMI_HPD_CON HDMI_HPD_CON
R129 10K/F_4

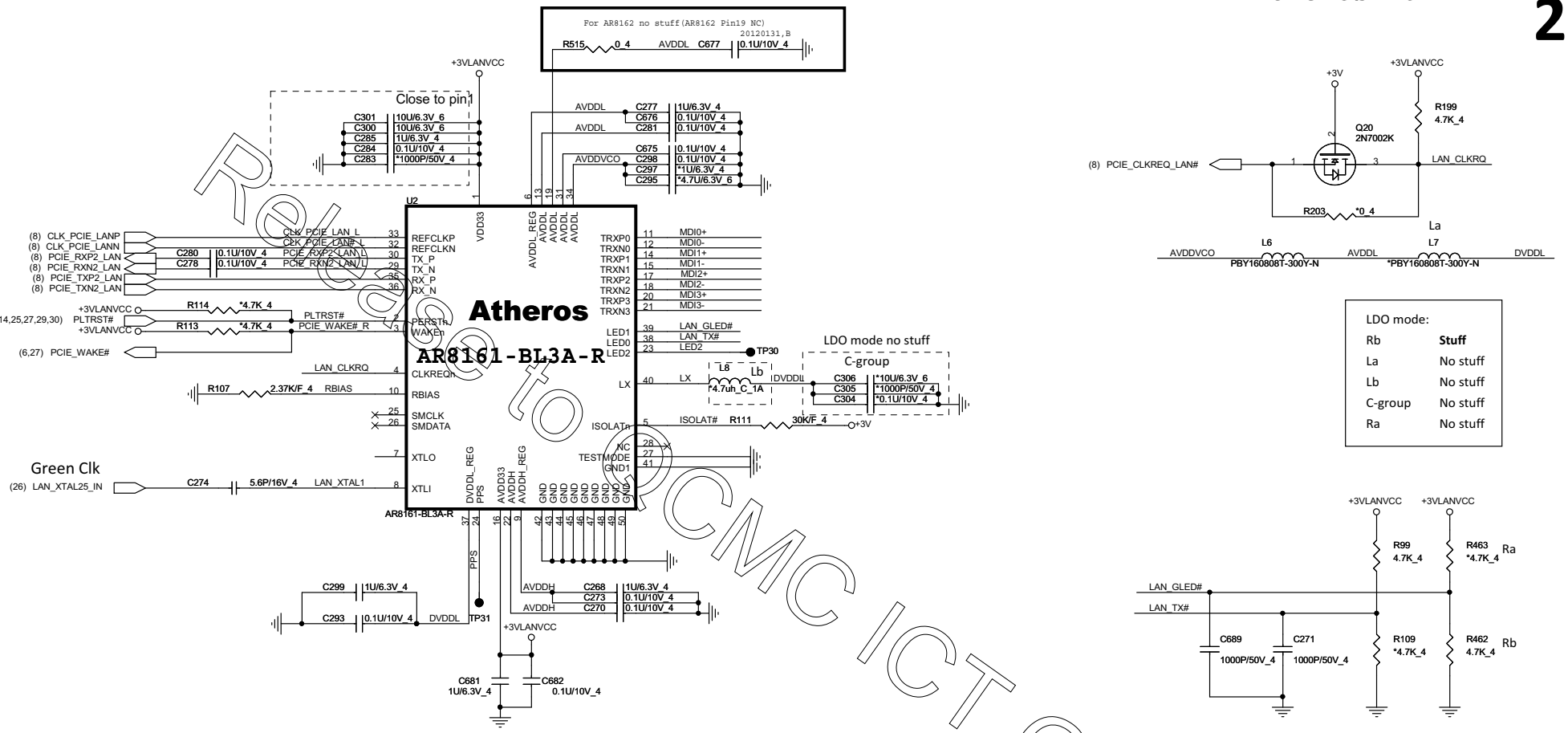
+5VCRT
C276 *0.01U/16V_4
for EMI request

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Connector	A
Date: Friday, May 11, 2012	Sheet 22of 42	

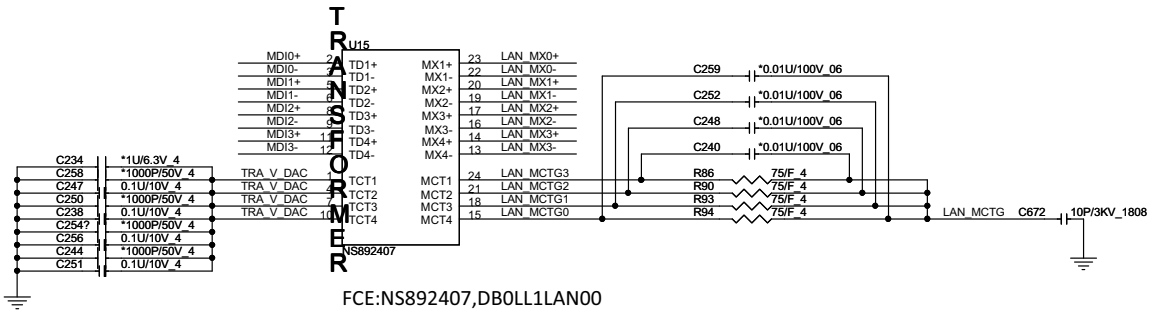

ALC269Q-VC2-GR
Digital
Analog
U6
0812 De-POP Noise DEL
Internal Speaker
SPK trace width
Speaker 4 ohm: 40mils
ANALOG
DIGITAL
Moat
40mils
20110817 Change to +5V for
ALC269Q-VC2-GR(MQFN)
Place the R8244 under
Codec Digital Gnd and
Analog Gnd(Bot side)
Audio Jack type:
Normal Open
Combo Jack(IPHONE)
20120511,MV
2N7002DW
DUAL USB CONN
INT SPEAKER CONN
PROJECT : JW6/7
Quanta Computer Inc.
NB5
Audio Codec (Realtek_ALC269Q-VC2-GR)
Date: Friday, May 11, 2012
Sheet 23of 42

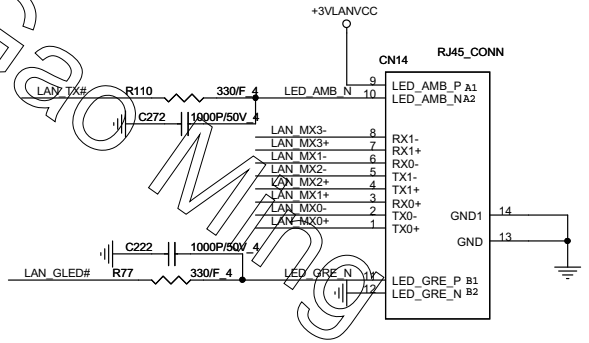


Atheros

AR8161-BL3A-R

LDO mode:	
Rb	**Stuff**
La	No stuff
Lb	No stuff
C-group	No stuff
Ra	No stuff





FCE:NS892407,DB0LL1LAN00

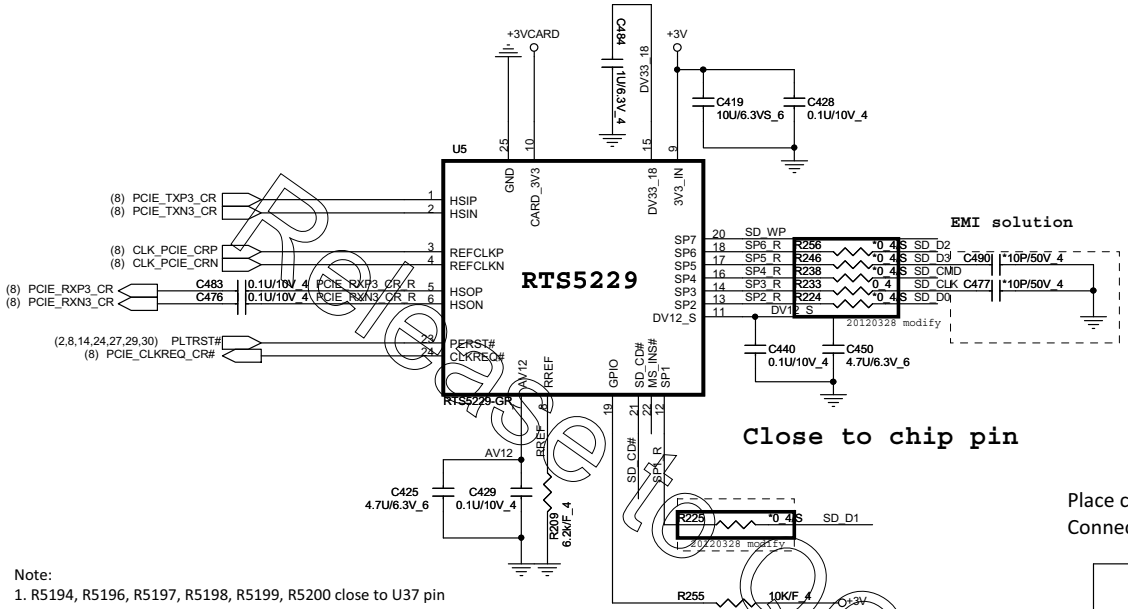
BOT:GST5009B LF,DB0Z06LAN00

NB5

PROJECT : JW6/7

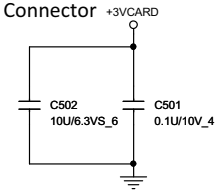
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**LAN Controller (Atheros_AR8161)**	A
Date: Friday, May 11, 2012	Sheet 24of 42	

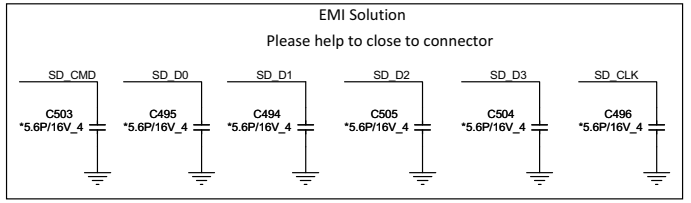


Note:
1. R5194, R5196, R5197, R5198, R5199, R5200 close to U37 pin
2. C5265, C5202 close to U37 pin7
3. C1021, C1022 close to U37 pin11
4. C1089, C1090 close to U37 pin9
5. C1019 close to U37 pin15
6. C1026, C1027 close to CN27 pin11
7. C1025 close to CN27 pin4

Place close to Connector

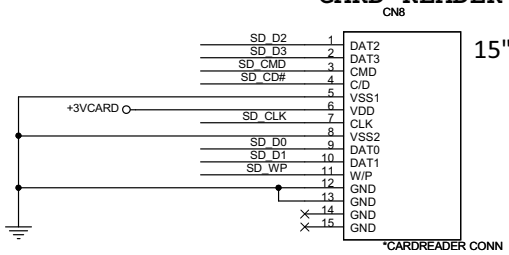


Share Pin

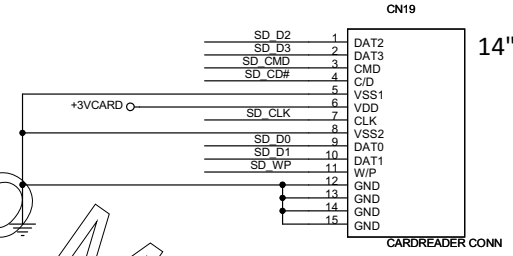


SD / MMC CARD READER

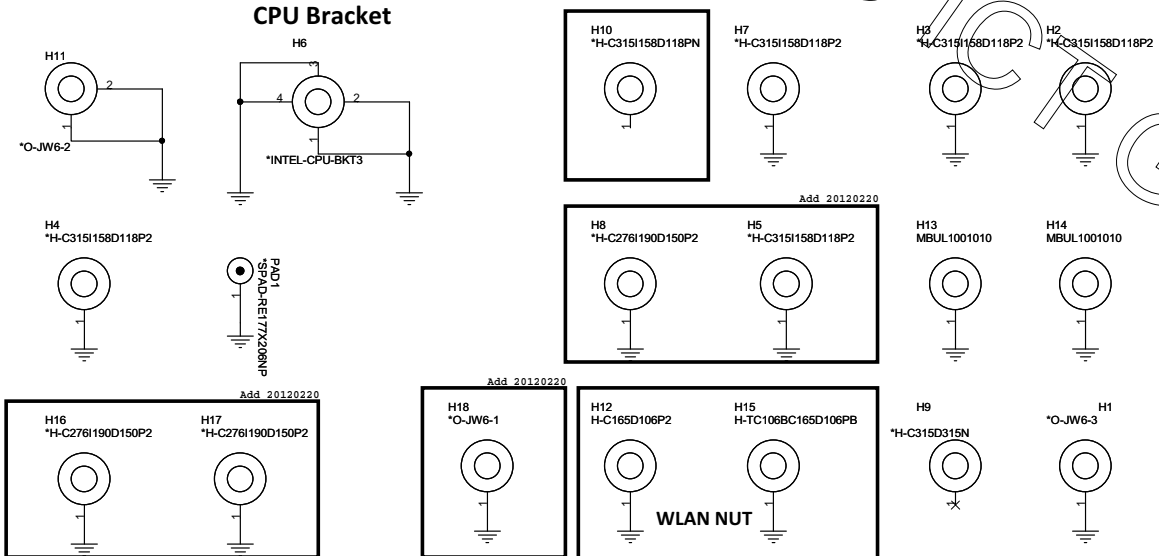
15" Only



14" Only

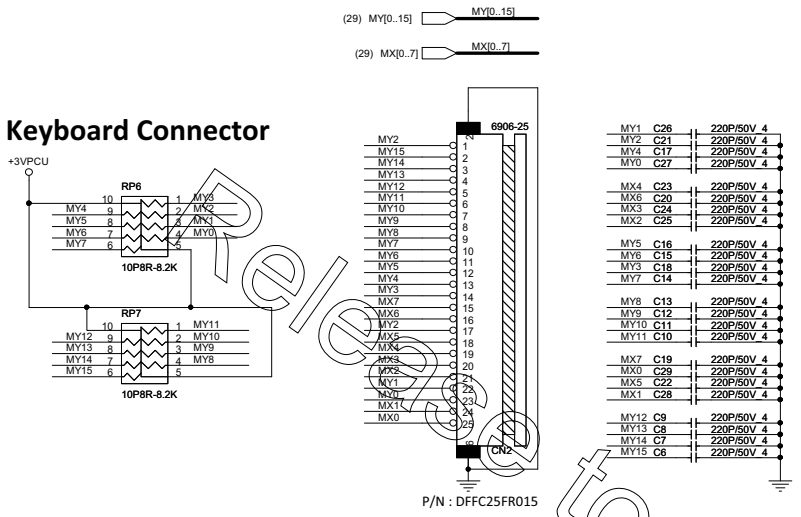


CPU Bracket

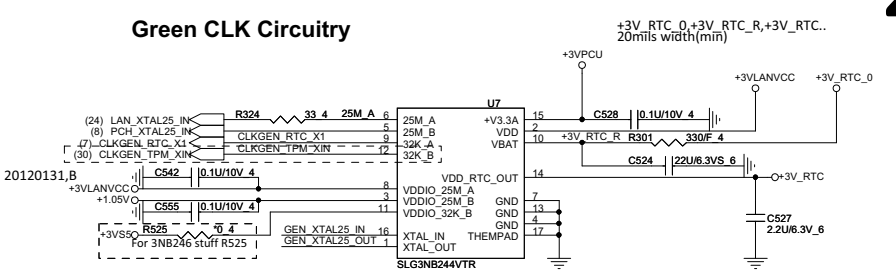


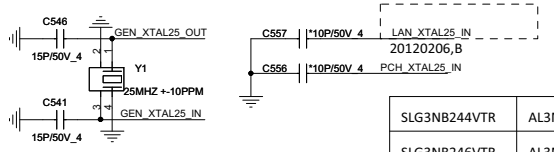
NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: Card Reader control (RTS5229-GR)	Rev: A
Date: Tuesday, May 15, 2012	Sheet: 25of 42	

Keyboard Connector



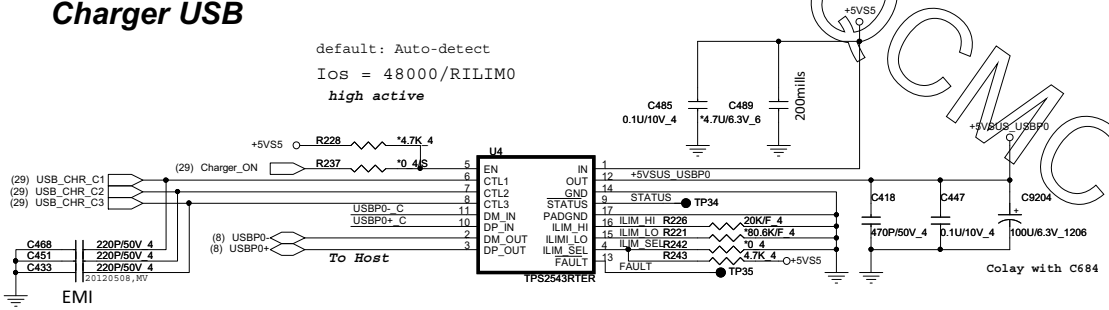
Green CLK Circuitry





SLG3NB244VTR	AL3NB244000	
SLG3NB246VTR	AL3NB246000	TPM

Charger USB



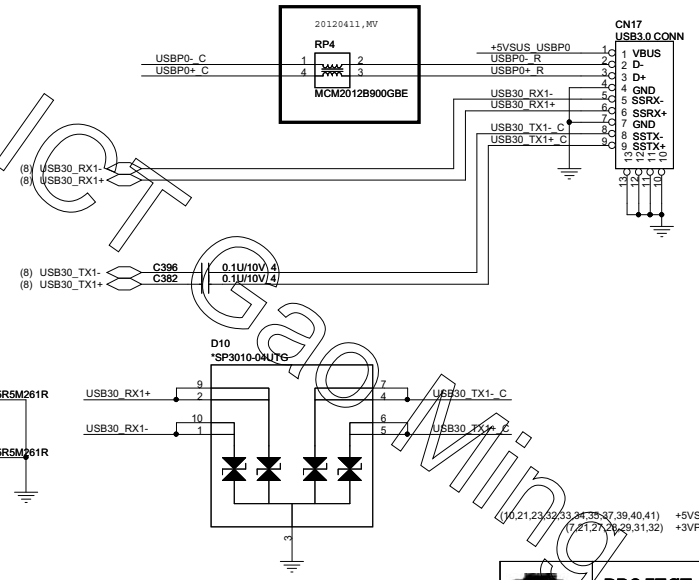
TPS2543/45 Control Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	1	Discharge	NA	off
0	0	1	1	DCP/auto	IOS_PW & ILIM_HI (1)	DCP load present
0	1	0	1	SDP	ILIM_HI	off
0	1	1	1	DCP/auto	ILIM_HI	DCP load present
1	1	0	1	SDP	ILIM_HI	off
1	1	1	1	CDP	ILIM_HI	CDP load present

(1) ILIM_HI: 20K(R5233), 2.4A

USB3.0 X 1/USB2.0 COMBO

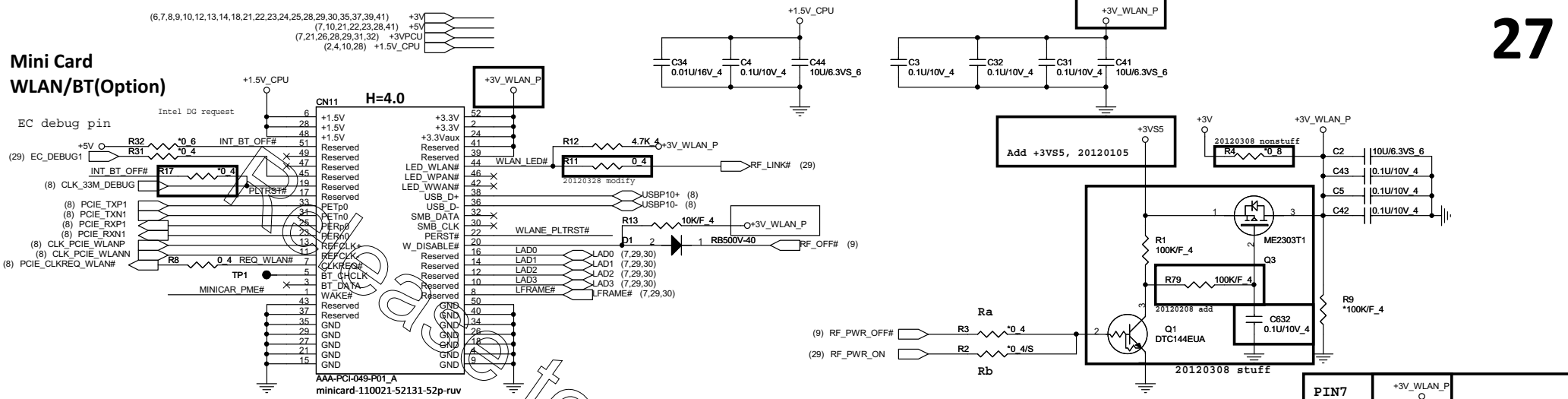
USB 3.0



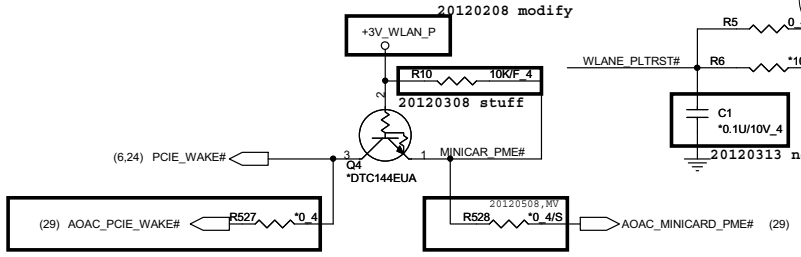
PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB 3.0/KB/Green CLK	A
NB5	Date: Friday, May 11, 2012	Sheet 26of 42

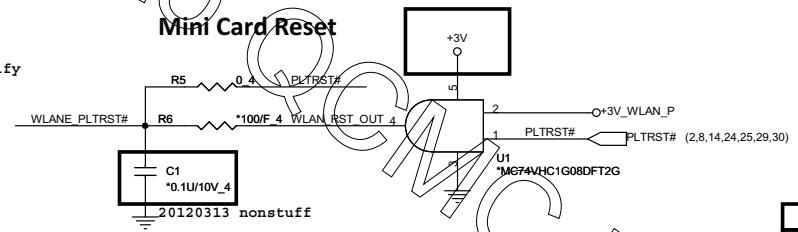
Mini Card WLAN/BT(Option)



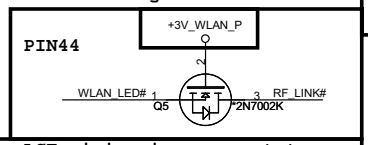
Support Wake Function(Reserve)

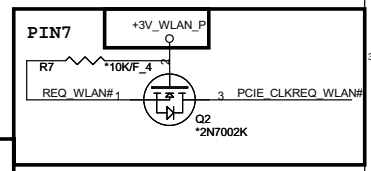


Mini Card Reset



Avoid leakage issue

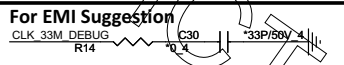




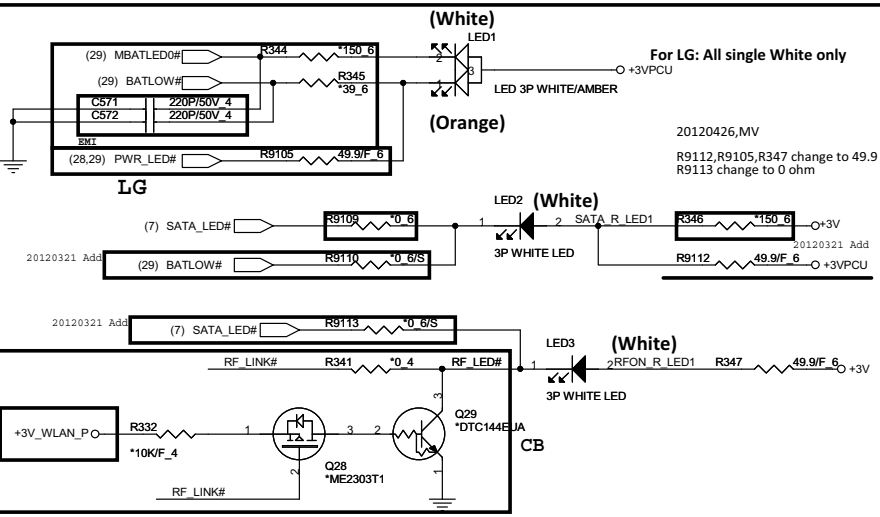
LGE mini-pcie power status

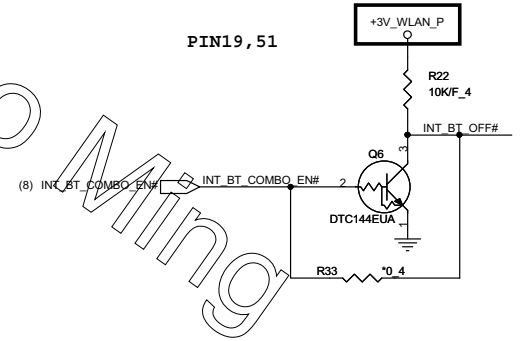
WLAN	Bluetooth	+3V_WLAN_P
Radio-ON	Radio-ON	Power-ON
Radio-ON	**Radio-OFF**	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	**Radio-OFF**	**Power-OFF**

For EMI Suggestion



LED Status





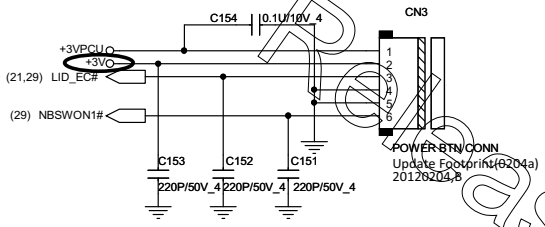
NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: MINI-PCIE/LED	Rev: A
Date: Monday, May 14, 2012	Sheet 27of 42	

Left side

Power Botton Connector(1)

For CB

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



20120507,MV
Change CN3/CN20#2 to +3V

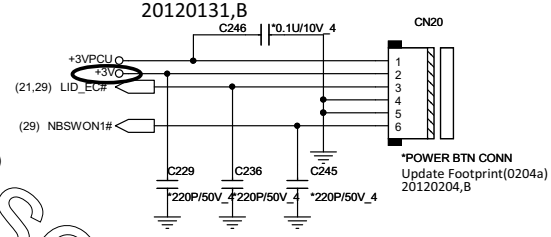
Right side

Power Botton Connector(2)

For LG

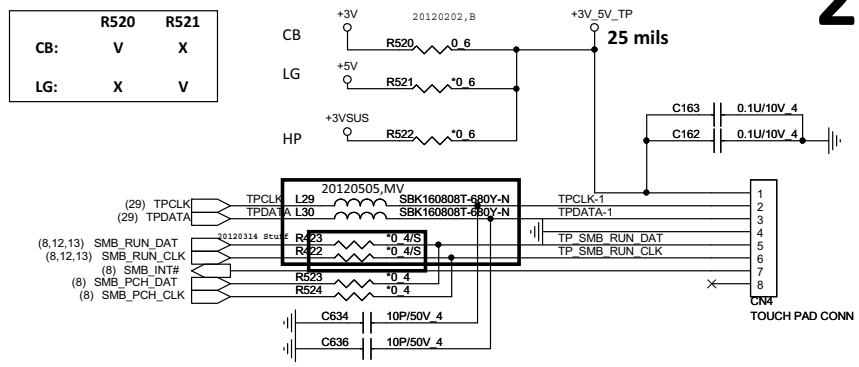
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

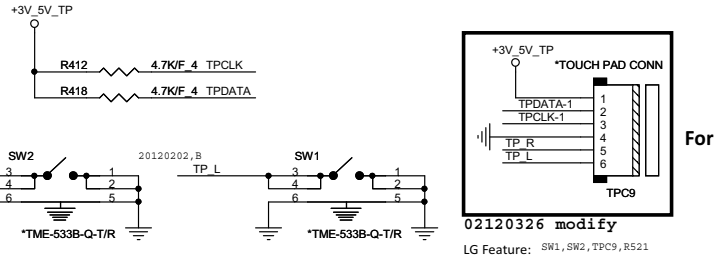
20120131,B



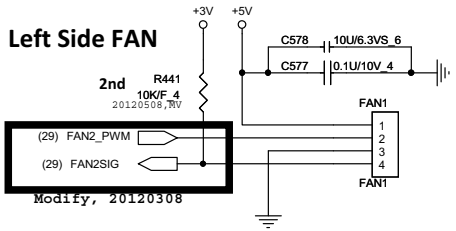
Touch Pad Connector

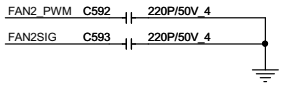
	R520	R521
CB:	V	X
LG:	X	V



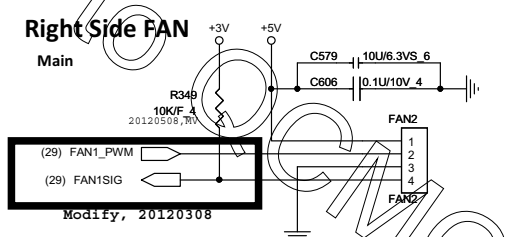


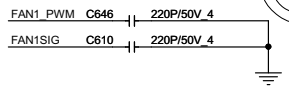
Left Side FAN





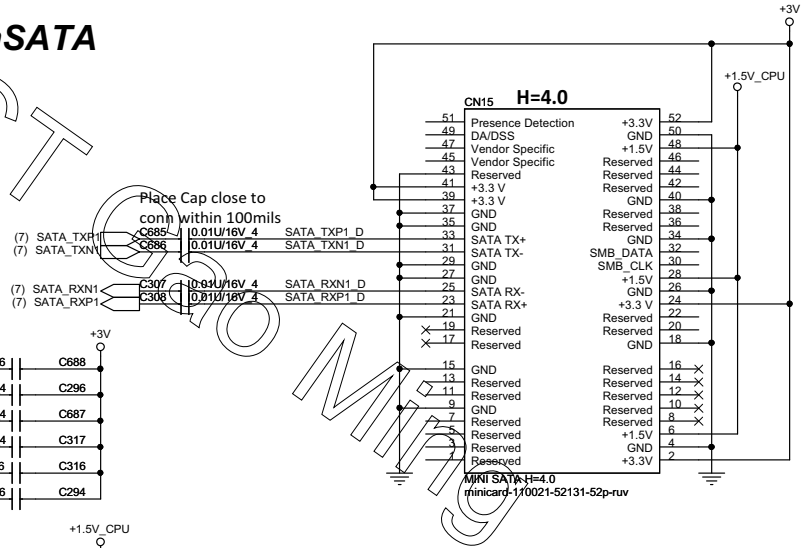
Right Side FAN

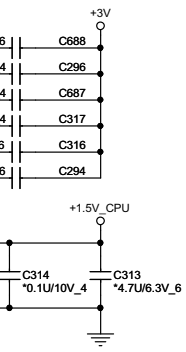


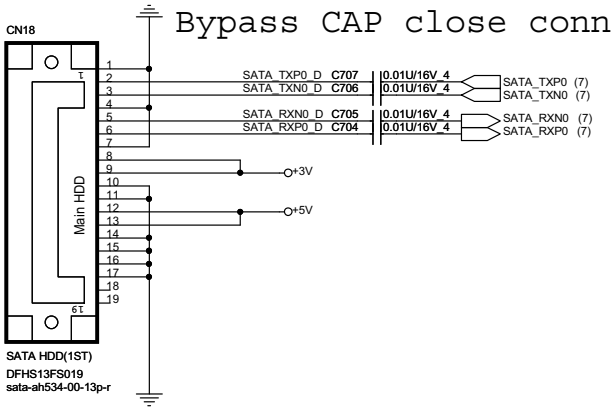


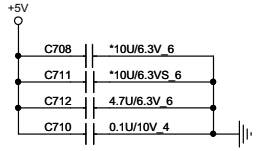
Mini PCI-E Card 2- Full size

mSATA









+5V: 2 A(4 Pin)
+3V: 2 A(4 Pin)
Gnd : (5 Pin)

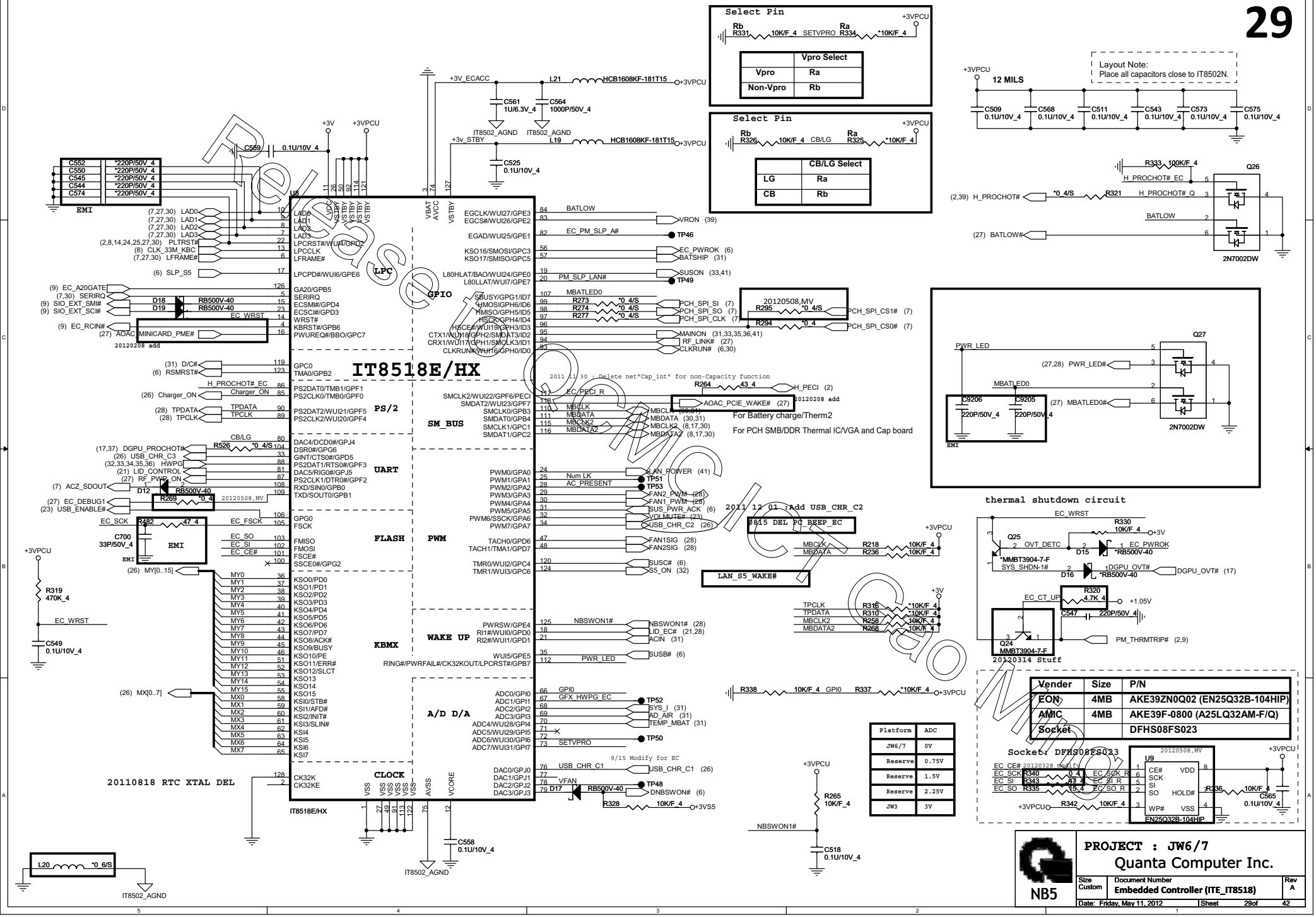
(6,7,8,9,10,12,13,14,18,21,22,23,24,25,27,29,30,35,37,39,41) +3V
(7,10,21,22,23,27,41) +5V
(7,21,26,27,29,31,32) +3VPCU
(2,4,10,27) +1.5V_CPU
(38,41) +12VALW

SATA HDD Connector(Cable type)

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/mSATA CONN	A
Date: Tuesday, May 15, 2012	Sheet 28of 42	


IT8518E/HX
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
Select Pin
Vpro Select
Vpro Ra
Non-Vpro Rb
CB/LG Select
LG Ra
CB Rb
Layout Note:
Place all capacitors close to IT8502N.
12 MILS
For Battery charge/Therm2
For PCH SMB/DDR Thermal IC/VGA and Cap board
thermal shutdown circuit
20120314 Stuff
Socket: DFHS08FS023
Vender Size P/N
EON 4MB AKE39ZN0Q02 (EN25Q32B-104HIP)
AMIC 4MB AKE39F-0800 (A25LQ32AM-F/Q)
Socket DFHS08FS023
20110818 RTC XTAL DEL
Platform ADC
JW6/7 0V
Reserve 0.75V
Reserve 1.5V
Reserve 2.25V
JW3 3V
PROJECT : JW6/7
Quanta Computer Inc.
NB5
Size Custom
Document Number
Embedded Controller (ITE_IT8518)
Rev A
Date: Friday, May 11, 2012
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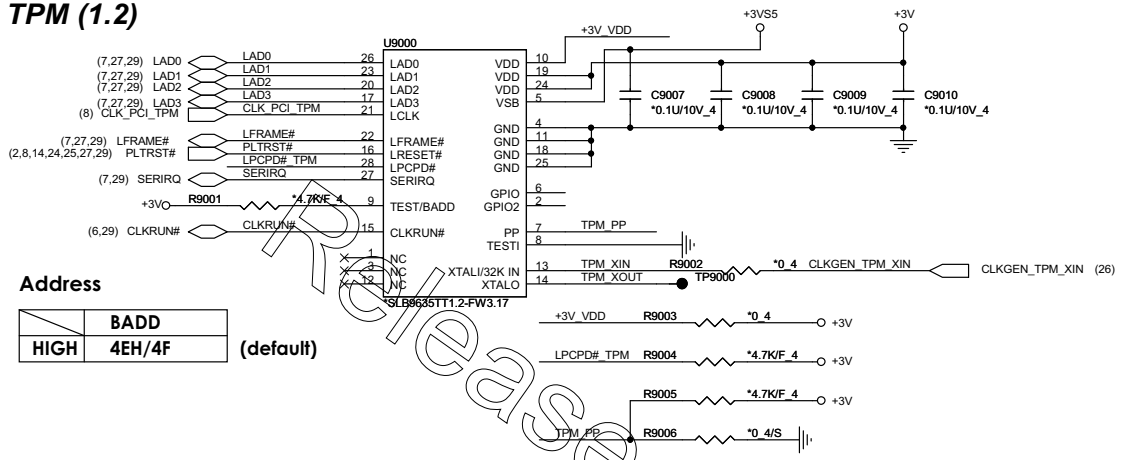
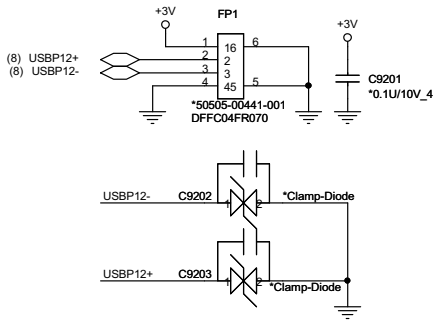
TPM (1.2)



Address

	BADD
HIGH	4EH/4F (default)

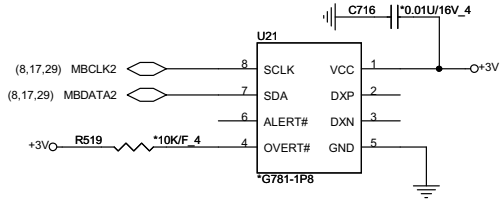
Finger Printer



Local Thermal Sensor

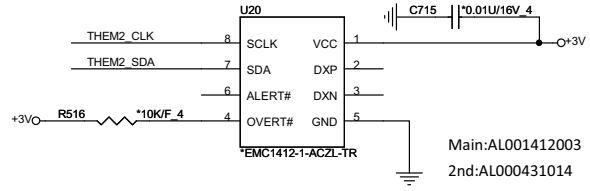
20120131,B

Thermal Solution(Close to GPU)

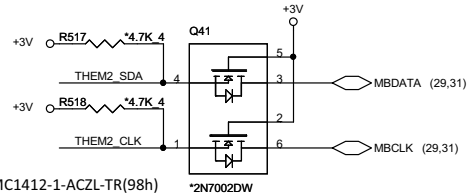


Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

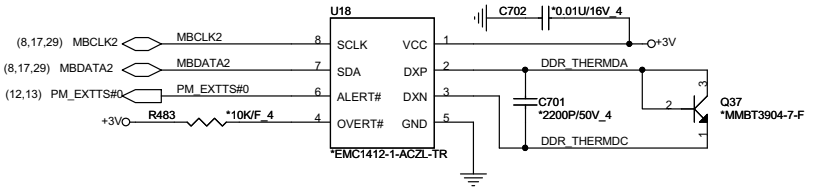
Thermal Solution(Close to CRT)



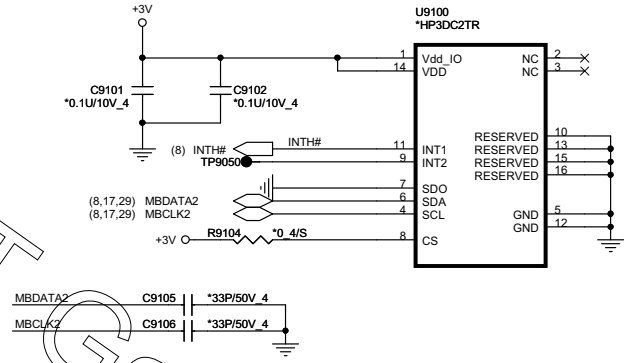
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)



DDR3 Thermal Sensor



Accelerometer Sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

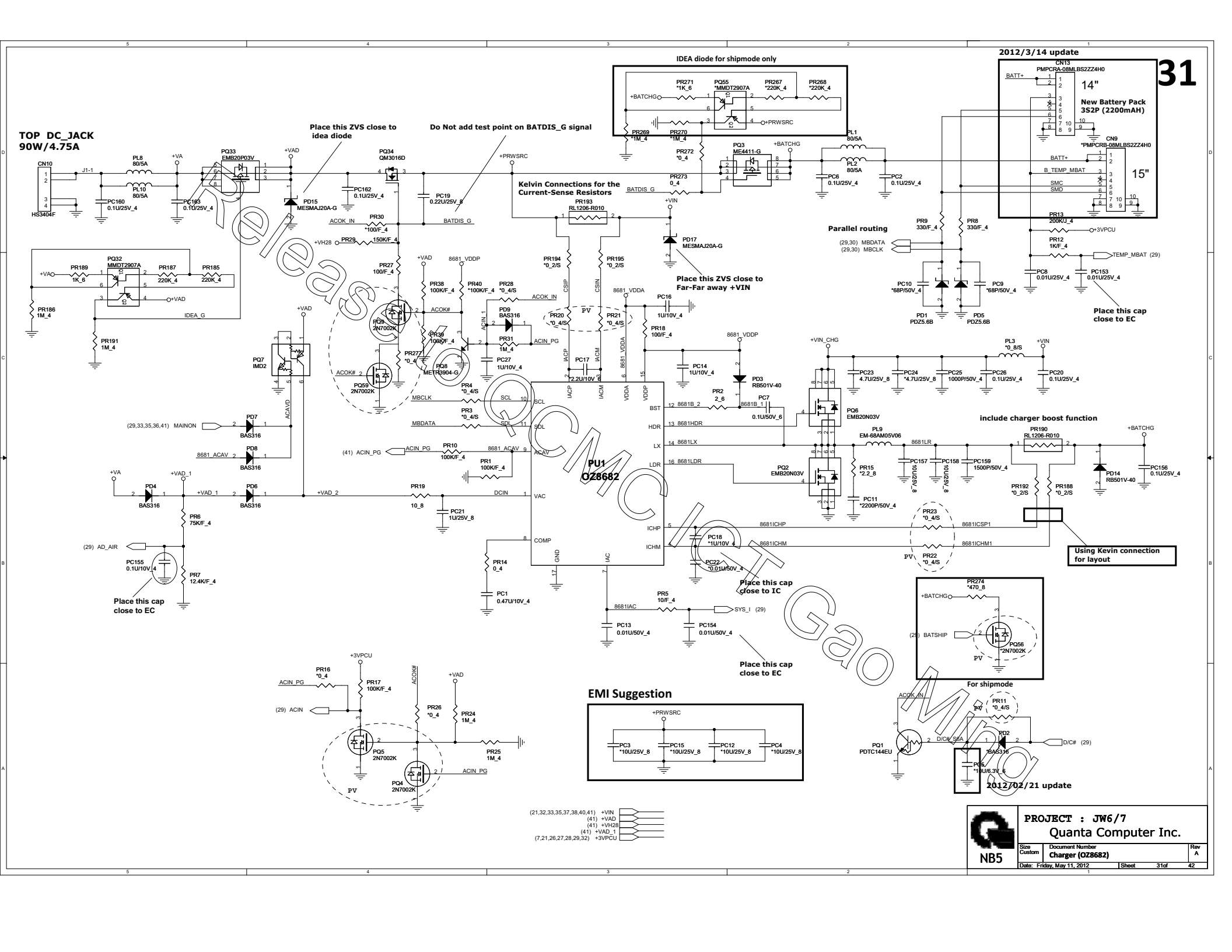
I2C (ST HP3DC2) SDO,Pin7	
0x50	Gnd Default
0x52	VDD

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	G-sensor/FP/TPM/THEM	A

Date: Friday, May 11, 2012 Sheet 30 of 42


2012/3/14 update
31
TOP DC_JACK
90W/4.75A
IDEA diode for shipmode only
Place this ZVS close to idea diode
Do Not add test point on BATDIS_G signal
Kelvin Connections for the Current-Sense Resistors
Parallel routing
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
include charger boost function
Using Kevin connection for layout
Place this cap close to IC
Place this cap close to EC
For shipmode
EMI Suggestion
New Battery Pack 3S2P (2200mAH)
14"
15"
PU1
OZ8682
2012/02/21 update
Quanta Computer Inc.
PROJECT : JW6/7
Charger (OZ8682)
NB5
Date: Friday, May 11, 2012
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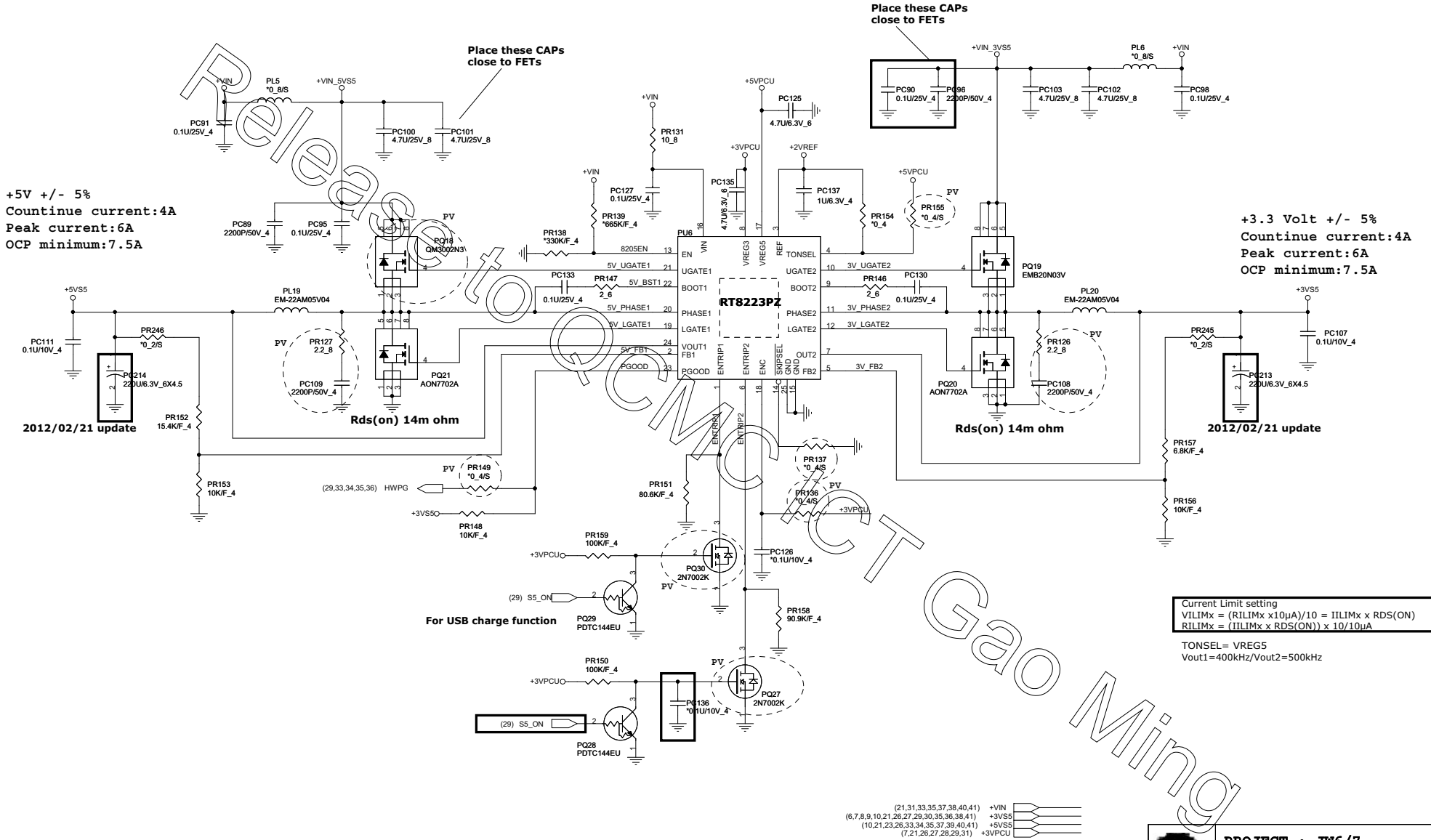
Rev A

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: 3/5VS5 (RT8223P)	Rev: A
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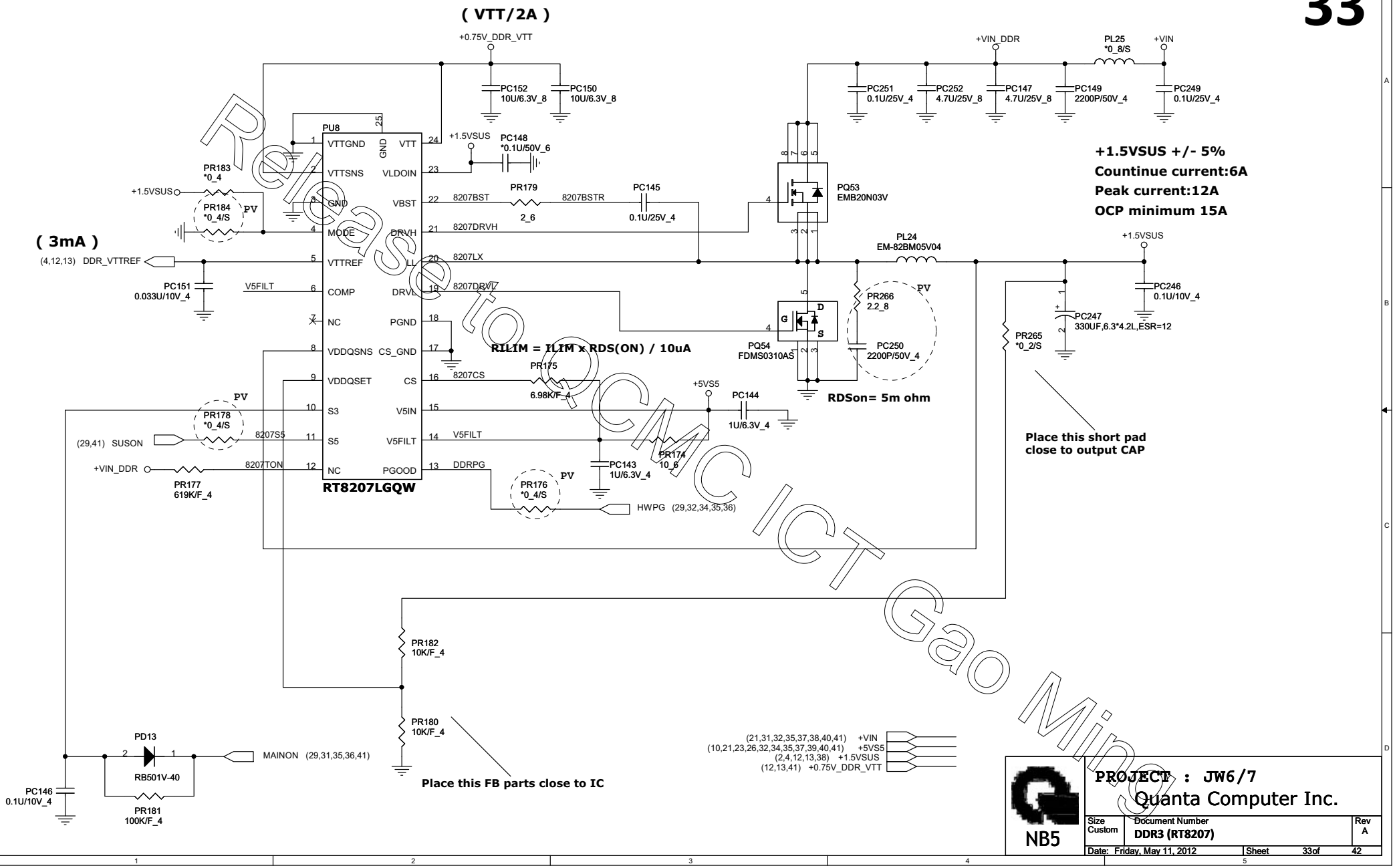

NB5

PROJECT : JW6/7

Quanta Computer Inc.

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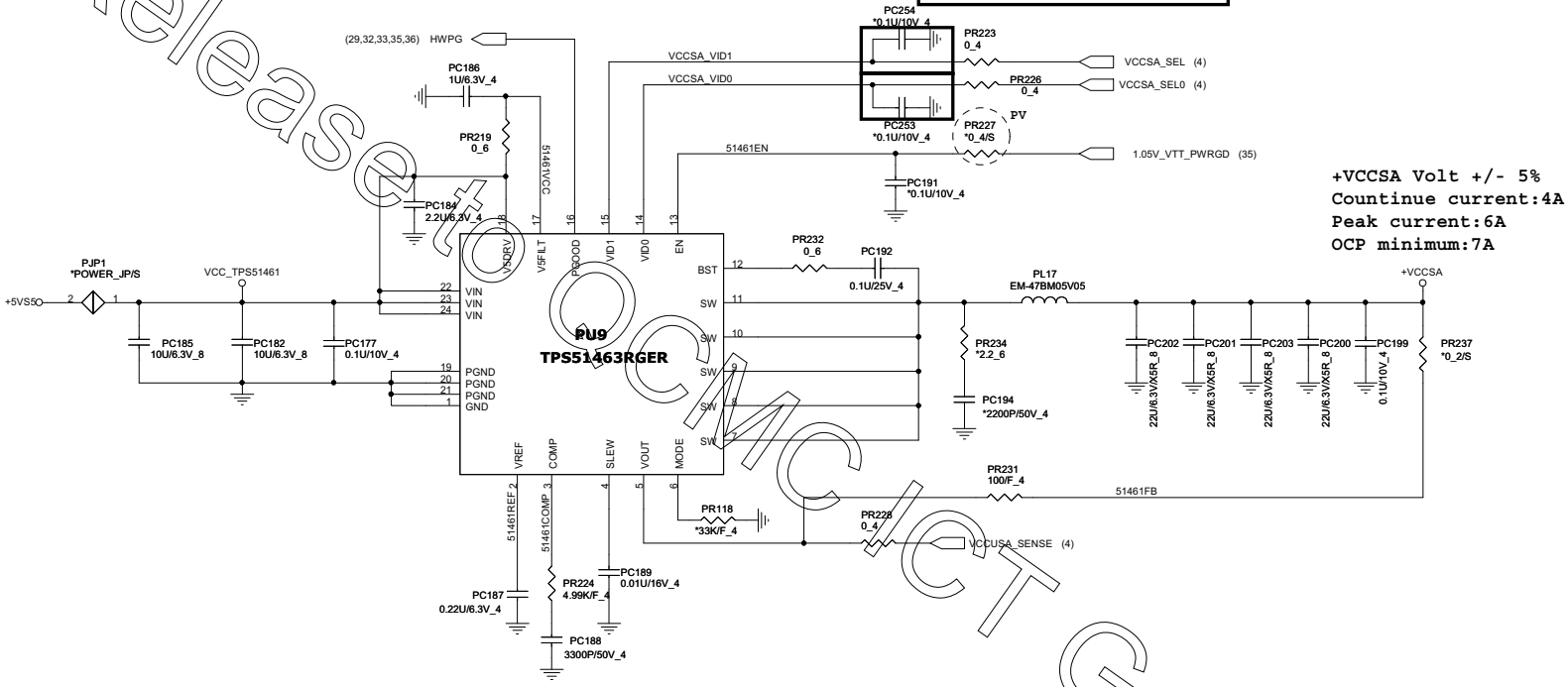
ULV
17W

CPU system agent voltage slew rate of 0.5 -10 mV/µs

SEL0	SEL1	+VCCSA
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

VCCSA	PU9
35W	TPS51462RGER
ULV 17W	TPS51463RGER



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	Quanta Computer Inc.
Size: Custom	Document Number: +VCCSA (TPS51462RGER)
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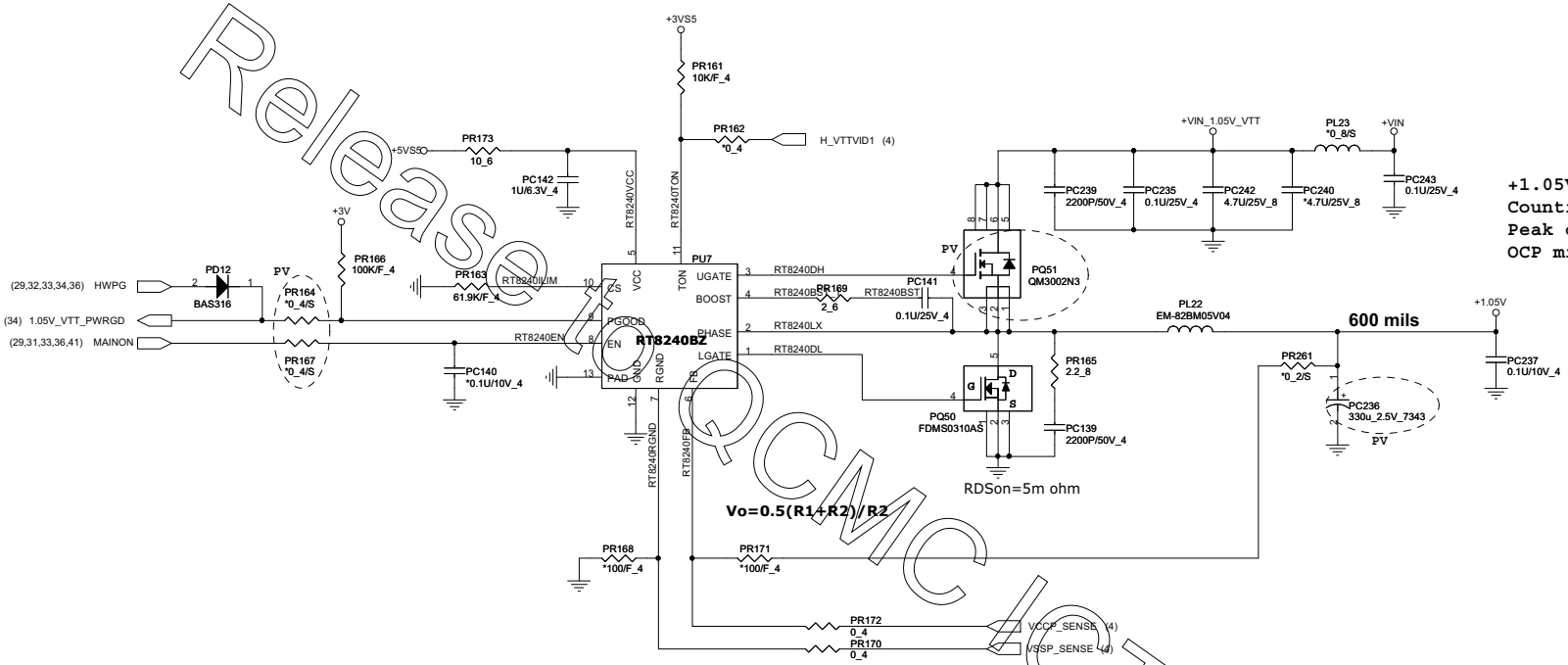
NB5



+1.05V_VTT +/- 5%
Countinue current:10A
Peak current: 12A
OCP minimum: 14.5A

NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: +1.05V (RT8240B)	Rev: A
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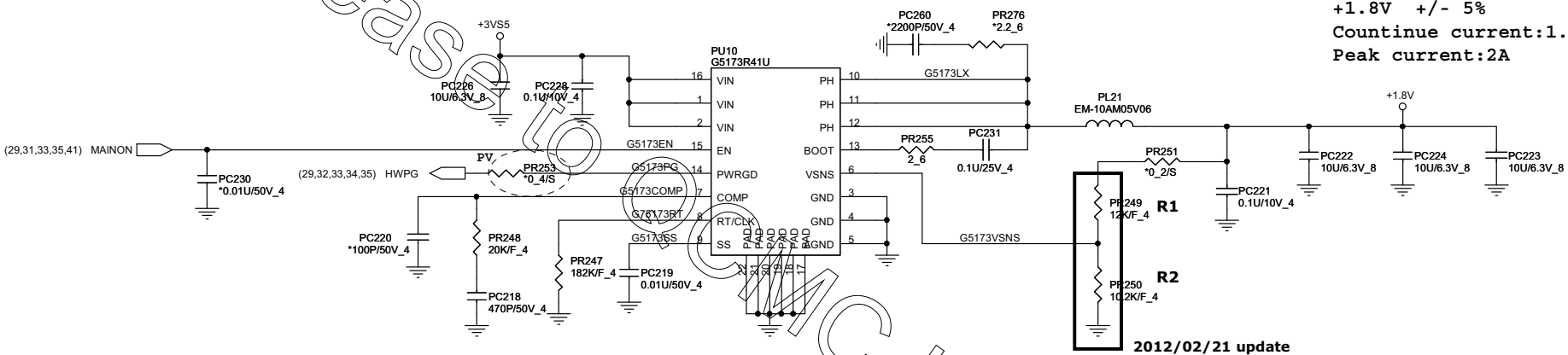

+1.8V +/- 5%
Countinue current:1.2A
Peak current:2A

2012/02/21 update
V0=0.827*(R1+R2)/R2

NB5

PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.8V (G9661)	A

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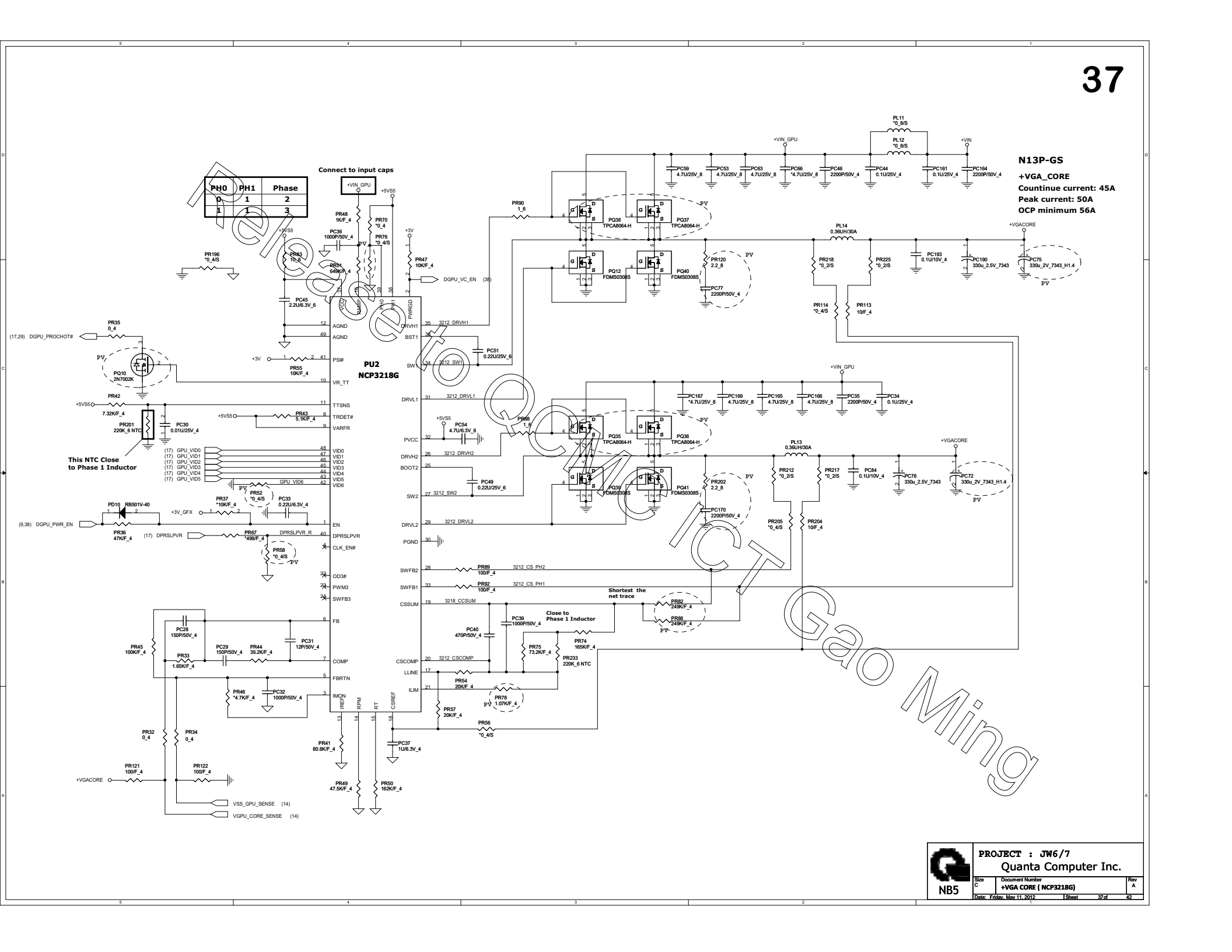
N13P-GS
+VGA_CORE
Countinue current: 45A
Peak current: 50A
OCP minimum 56A
PU2
NCP3218G
Connect to input caps
This NTC Close to Phase 1 Inductor
Close to Phase 1 Inductor
Shortest the net trace
PH0 PH1 Phase
0 1 2
1 1 3
PROJECT : JW6/7
Quanta Computer Inc.
NB5
+VGA CORE (NCP3218G)
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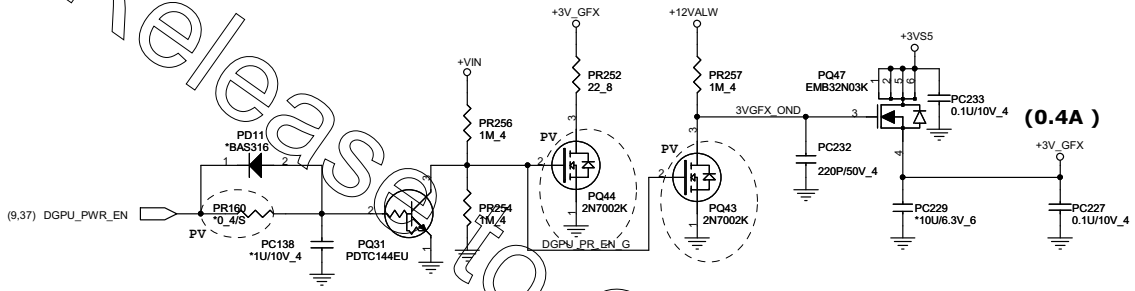
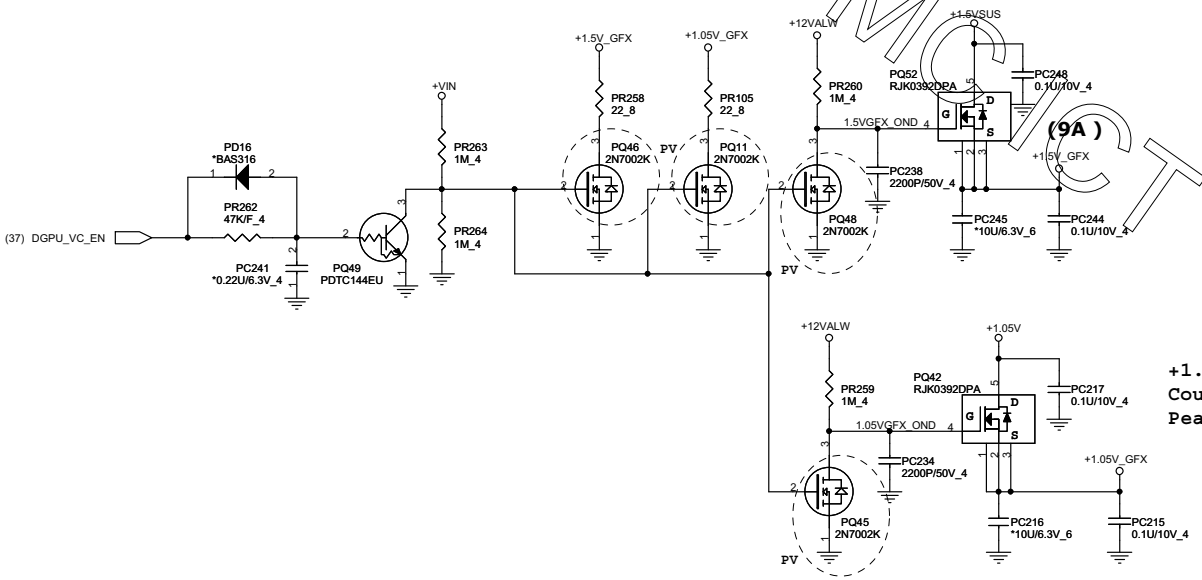
Confidential
Quanta Computer Inc.
Go Ming

VGA

(2,4,12,13,33) +1.5VSUS
(3,9,10,21,26,27,29,30,32,35,36,41) +3VS5
(14,16,17,18,37) +3V_GFX
(15,18,19,20) +1.5V_GFX
(14,15,16,18) +1.05V_GFX
(41) +12VALW
(2,4,6,7,8,10,26,29,35,39) +1.05V





+1.05V +/- 3%
Countinue current:2.1A
Peak current:3A

NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: +VGA POWER	Rev: A
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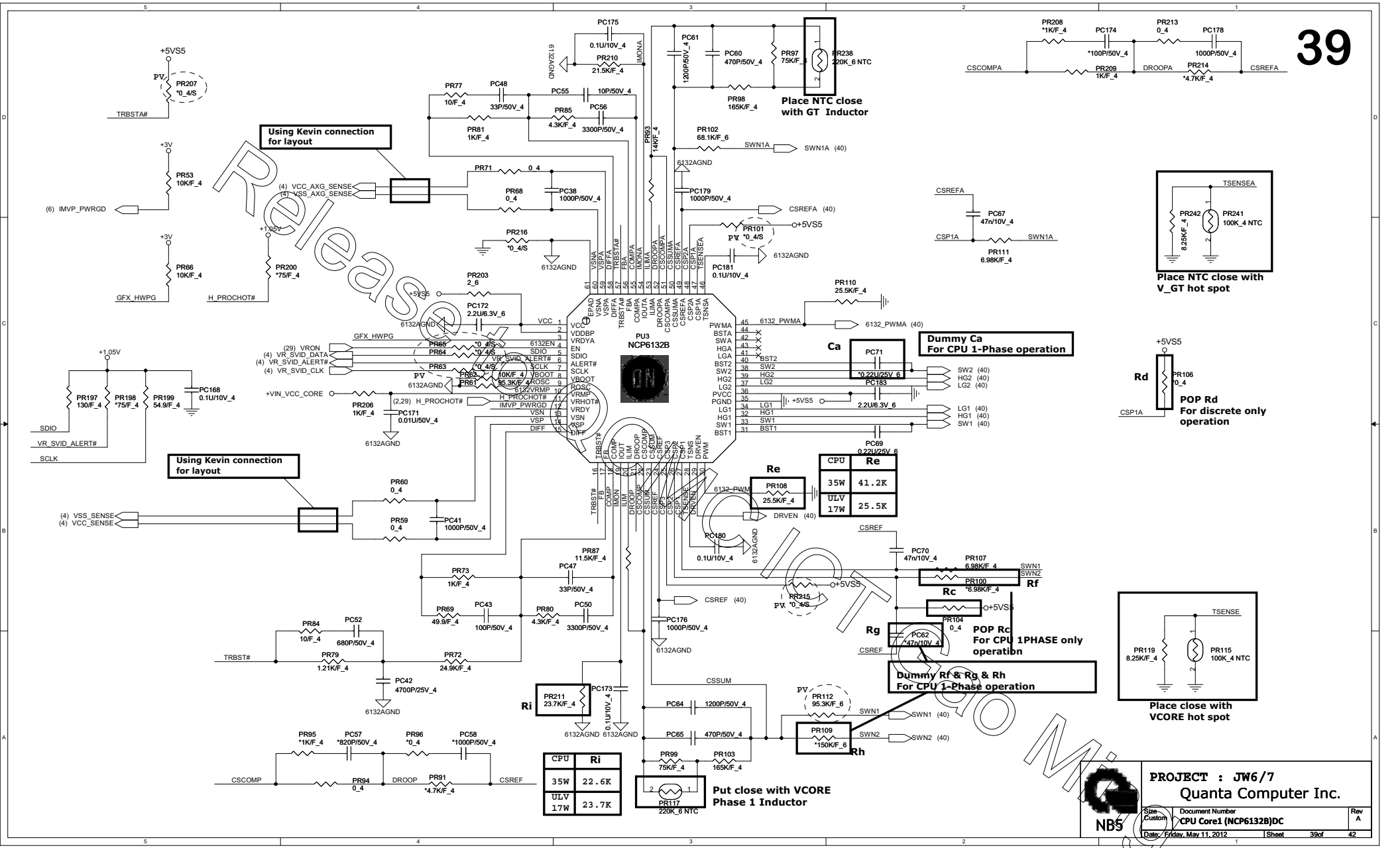
Using Kevin connection for layout
Using Kevin connection for layout
Place NTC close with GT Inductor
Dummy Ca For CPU 1-Phase operation
Place NTC close with V_GT hot spot
POP Rd For discrete only operation
POP Rc For CPU 1PHASE only operation
Dummy Rf & Rg & Rh For CPU 1-Phase operation
Place close with VCORE hot spot
Put close with VCORE Phase 1 Inductor
PU3 NCP6132B
Ca
Rd
Re
Rc
Rf
Rg
Rh
Ri
CPU Re
35W 41.2K
ULV 17W 25.5K
CPU Ri
35W 22.6K
ULV 17W 23.7K
Release
Quanta Computer Inc.
PROJECT : JW6/7
CPU Core1 (NCP6132B)DC
Date: Friday, May 11, 2012
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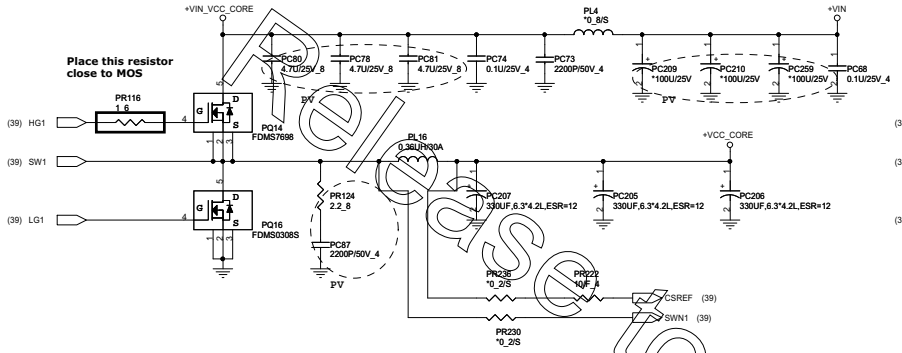
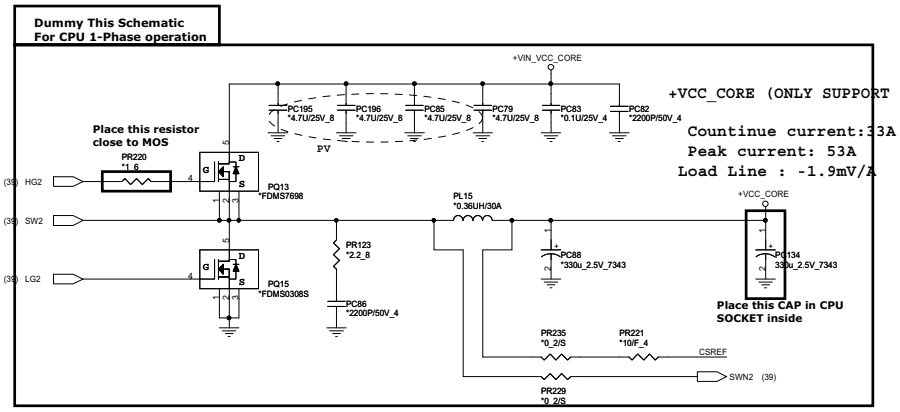


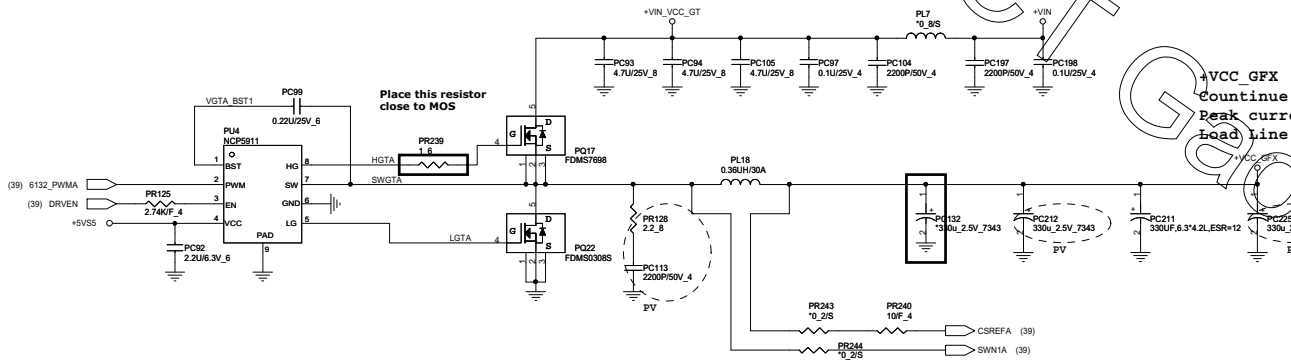


+VCC_CORE (ONLY SUPPORT 35W)

Countinue current:33A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ULV 17W)

TDC : 25A
Peak current: 33A
Load Line : -2.9mV/A



+VCC_GFX
Countinue current:21.5A
Peak current: 33A
Load Line : -3.9mV/A

NB5	PROJECT : JW6/7 Quanta Computer Inc.		
	Size: C	Document Number: CPU Core2 (NCP5911)DC	Rev: A
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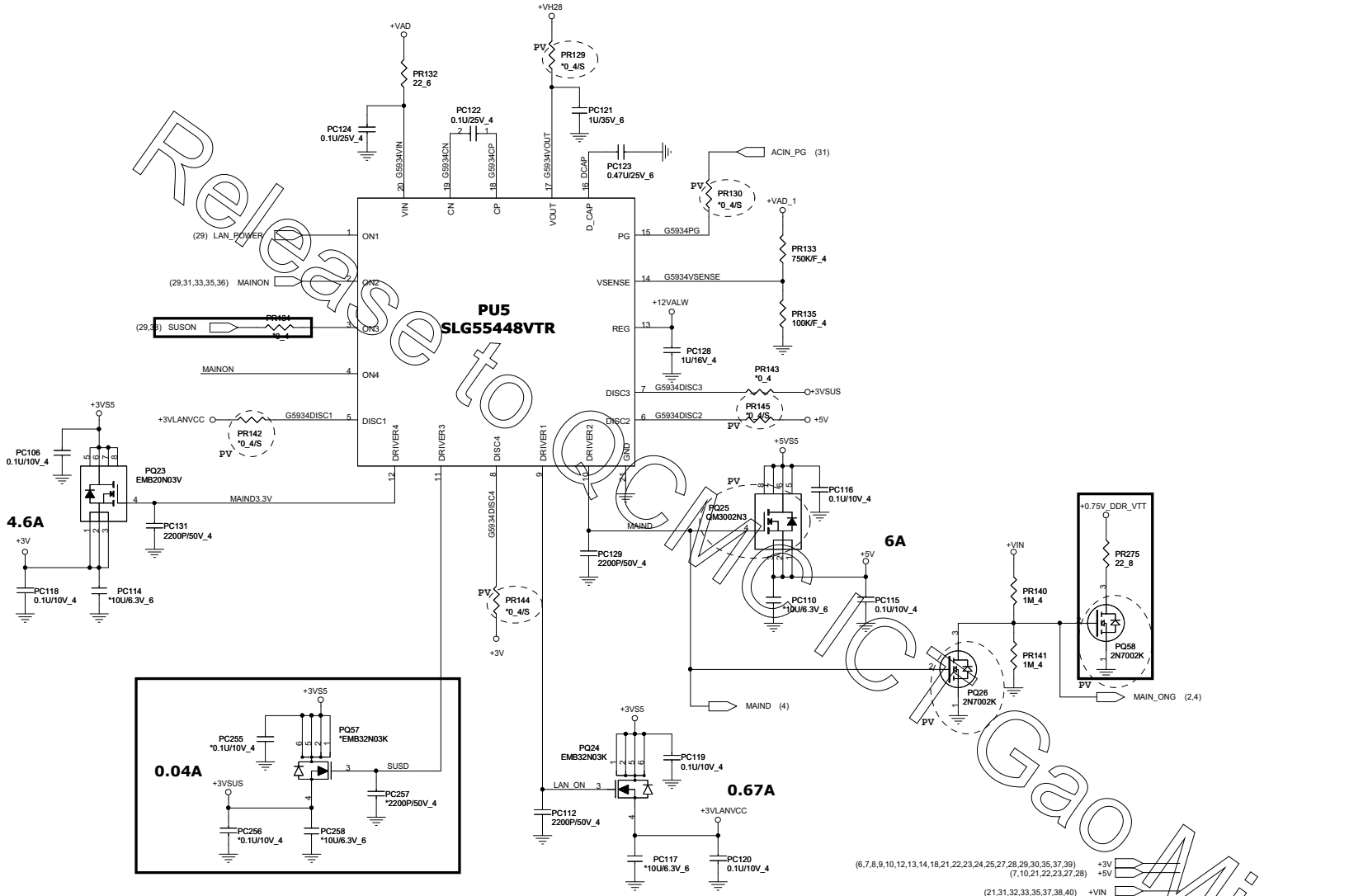

NB5	PROJECT : JW6/7 Quanta Computer Inc.	
Size: Custom	Document Number: Dis-charge IC (SLG55448V)	Rev: A
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Release to QCMC ICT Gao Ming

NB5	PROJECT : JW6/7 Quanta Computer Inc.	
	Size: C Document Number: History	Rev: A
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