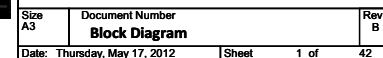
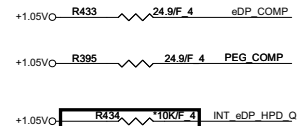


01



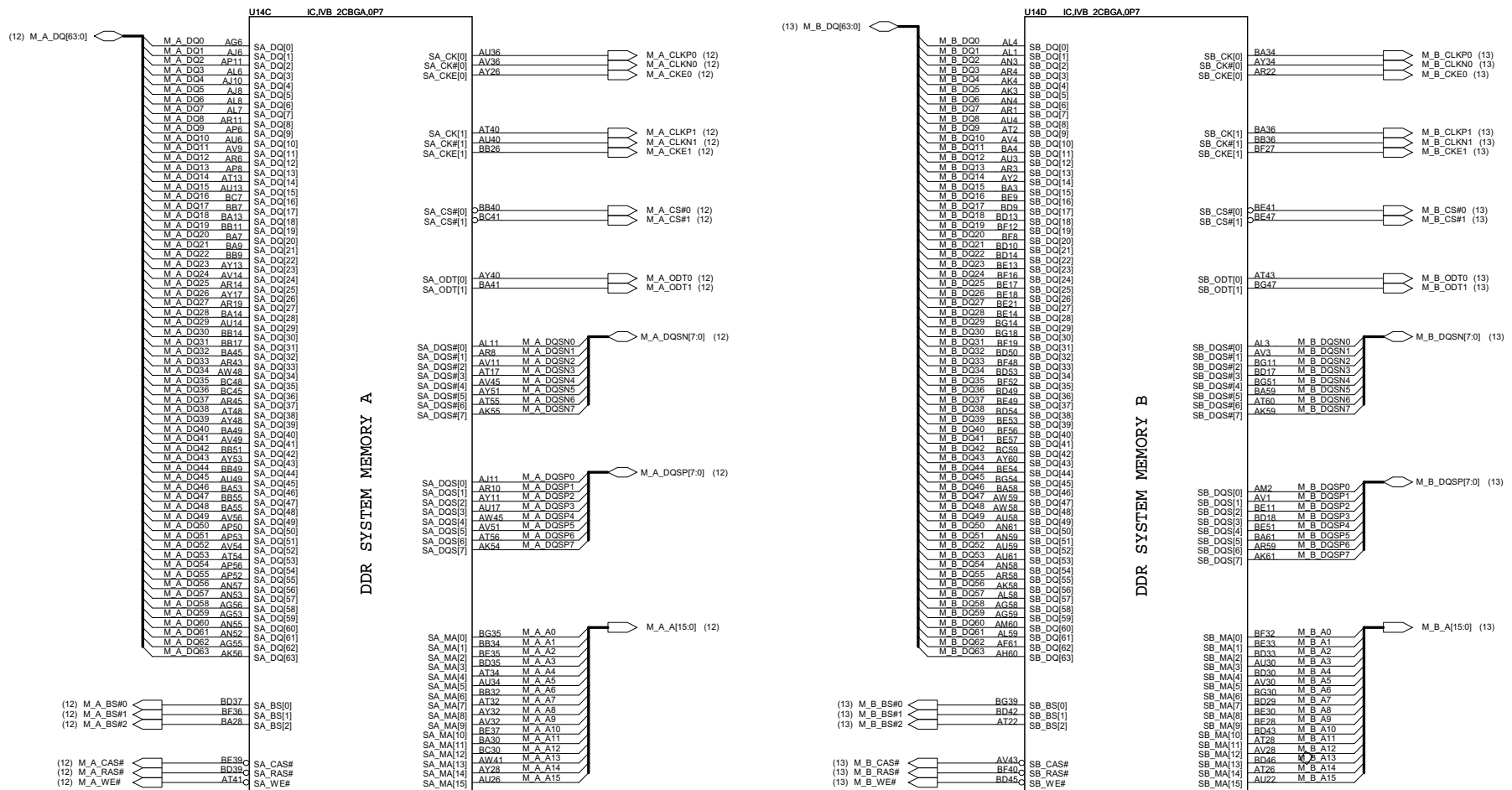


t **Connect a Test Point on BPM# 7 signal, very close to processor.**



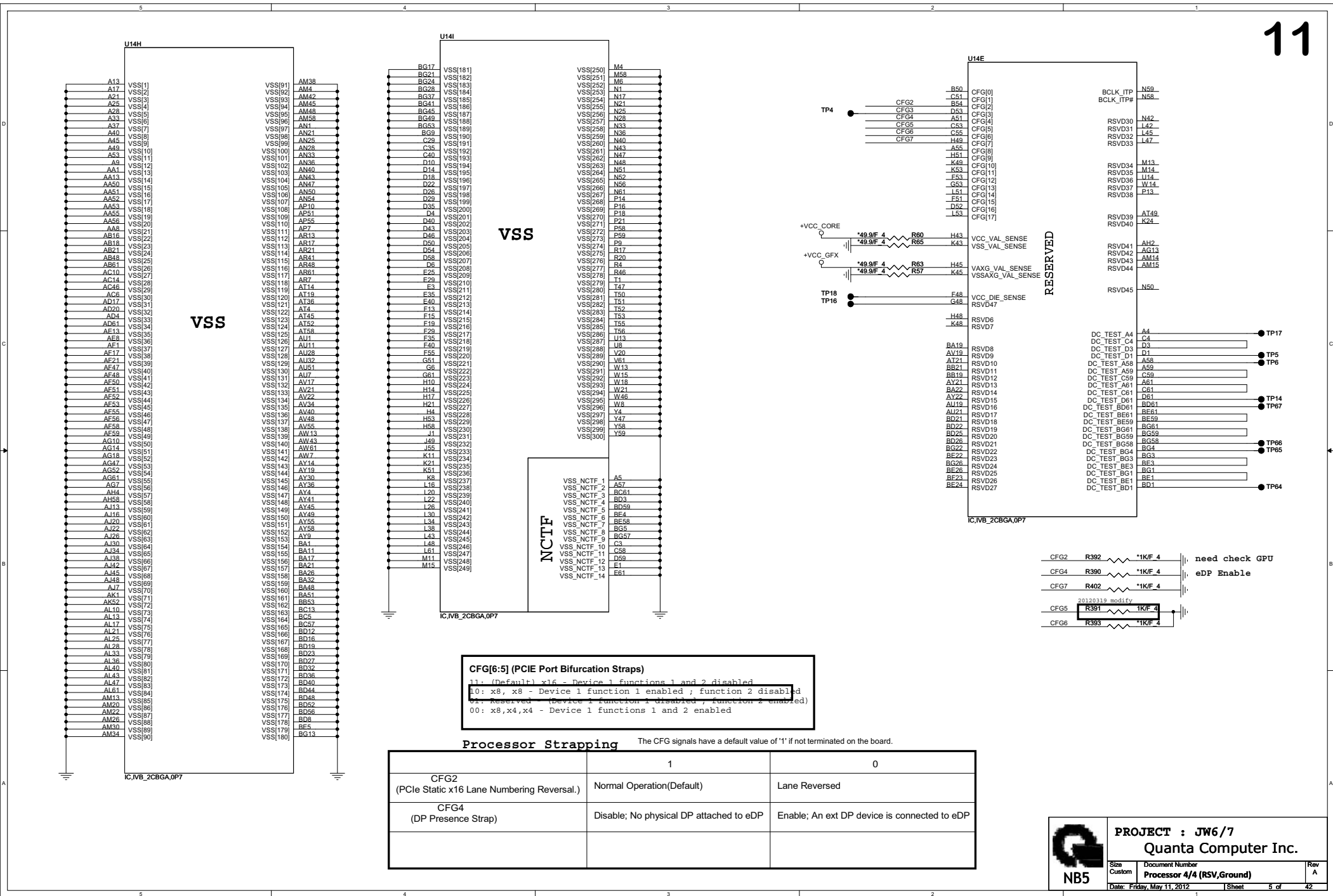
Size Custom	Document Number Processor 1/4 (Host/GPU)	Rev A
Date: Friday, May 11, 2012	Sheet	2 of 42

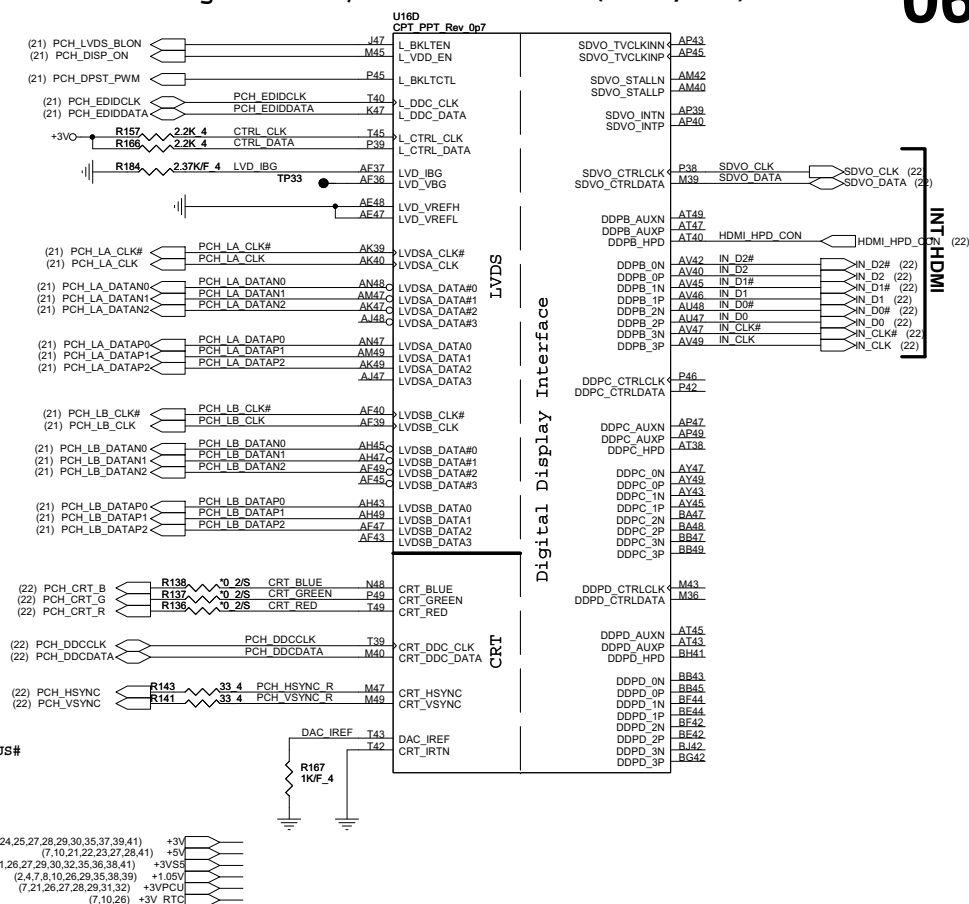
Ivy Bridge Processor (DDR3)



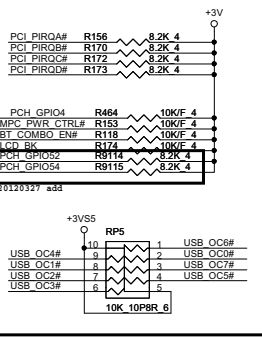
PROJECT : JW6/7
Quanta Computer Inc.

Size Custom	Document Number Processor 2/5 (DDR3 I/F)	Rev A
Date: Friday, May 11, 2012	Sheet	3 of 42

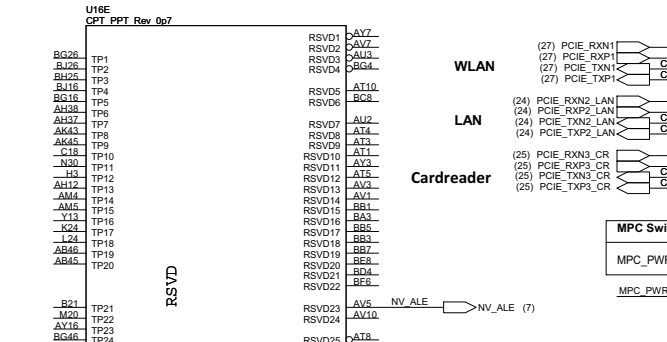




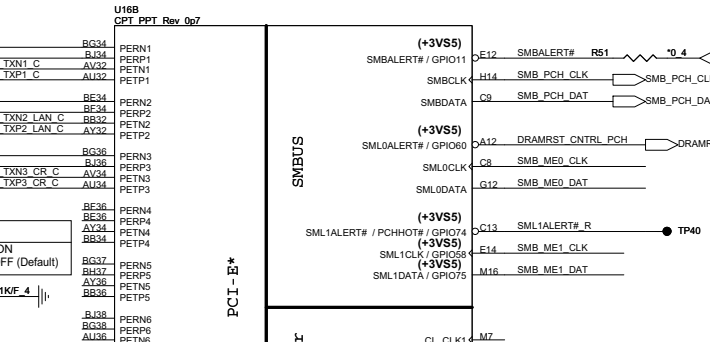
PCI/USB0C# Pull-up(CLG)



Cougar Point-M/Panther Point (PCI,USB,NVRAM)



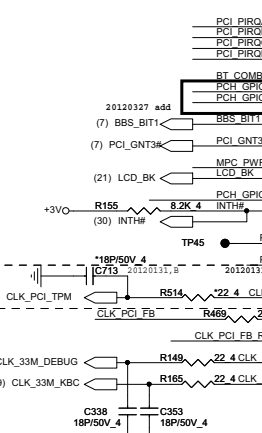
Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



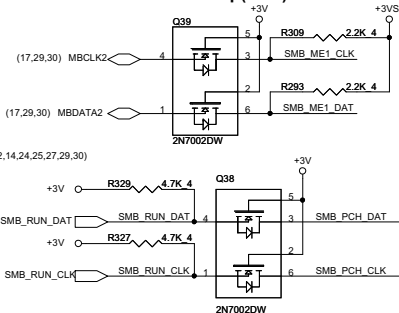
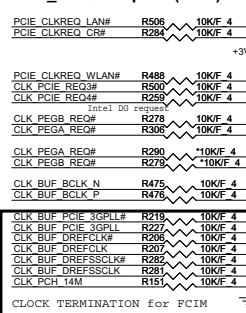
USB3.0



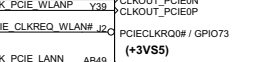
130 Modify USB3.0 for HM70



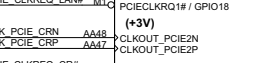
SMBus/Pull-up(CLG)

**CLK_REQ/Strap Pin(CL**

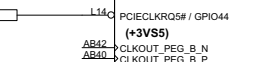
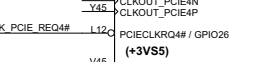
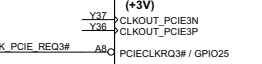
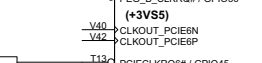
K_PCIE WLAN



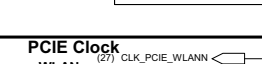
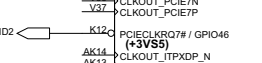
IE CLKREQ_I



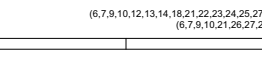
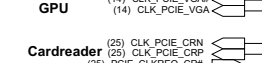
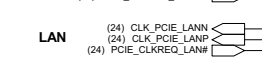
E_CLKREQ_C

K_PEGB_REQ

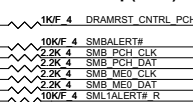
7



WLA



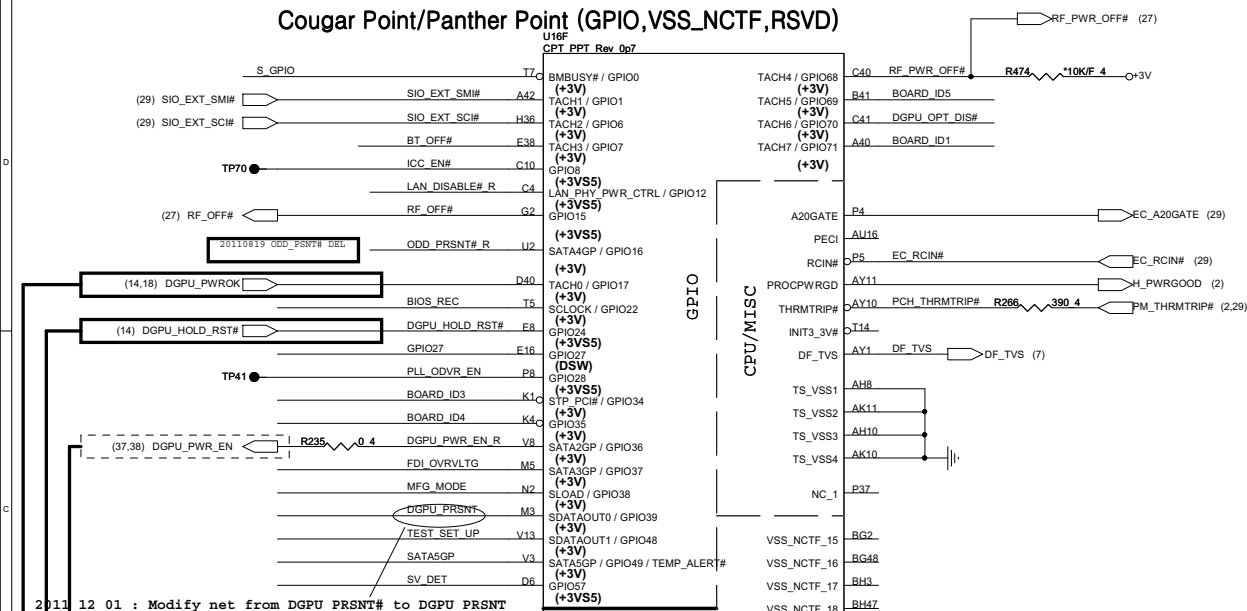
SMBus/Pull-up(CLG)



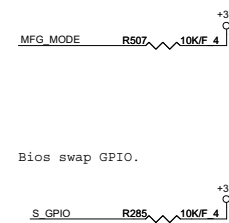
PROJECT : JW6/7
Quanta Computer Inc.

Size Custom	Document Number PCH 3/6 (Clock/PCI/PCIE/USB)
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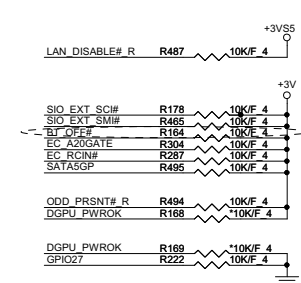
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



MFG-TEST



GPIO Pull-up/Pull-down(CLG)



Intel ME Crypto Transport Layer Security (TLS) cipher suite

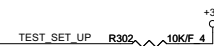
Low = Disable (Default)

High = Enable

BIOS RECOVERY

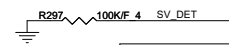
High = Disable (Default)

Low = Enable



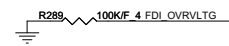
SV_SET_UP

High = Strong (Default)



TEST DETECT

Low = Default



FDI TERMINATION VOLTAGE OVERRIDE

Reserved only

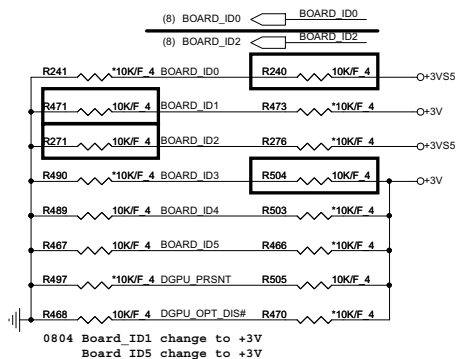
BOARD_ID[3:0] Model Name

0000	QLGA
0001	TWC
0010	JW2
0011	TBD
0100	LG3
0101	LG5
0110	LG2C
0111	LG4C
1000	TBD
1001	JW6/JW7
1010	JW3
1011	JW6H/JW6L
1100	JW3H

Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO71	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO34	MODEL BIT3
BOARD_ID4	GPIO35	Reserve and pull low
BOARD_ID5	GPIO69	HM77=0, HM70=1
DGPU_PRNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

20110816 Define BRD_ID[3:0]



PROJECT : JW6/7

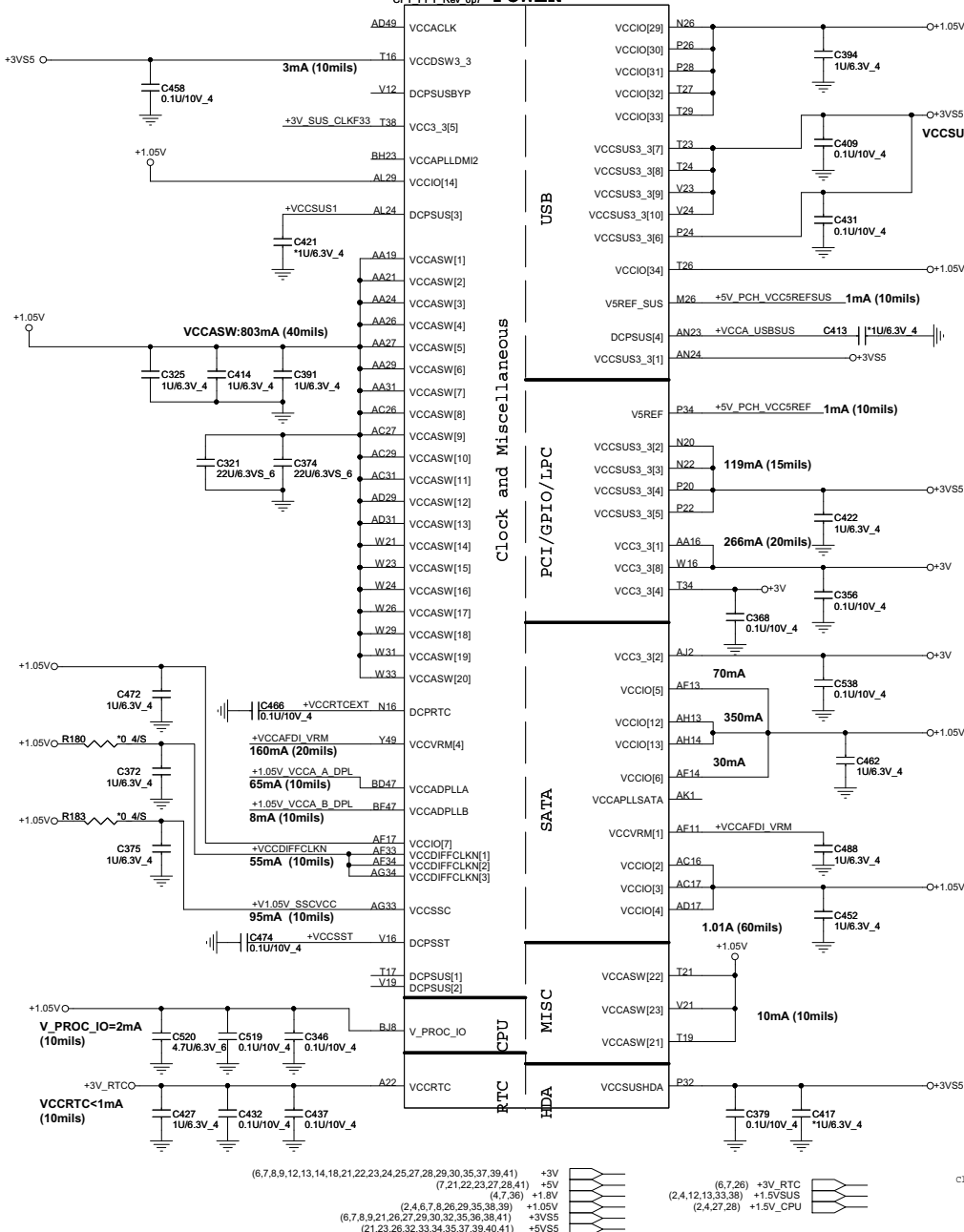
Quanta Computer Inc.

Size Custom Document Number PCH 4/6 (GPIO) Rev A

Date: Tuesday, May 15, 2012 Sheet 9 of 42

Cougar Point/Panther Point (POWER)

U16J
CPT PPT Rev 0p7 **POWER**

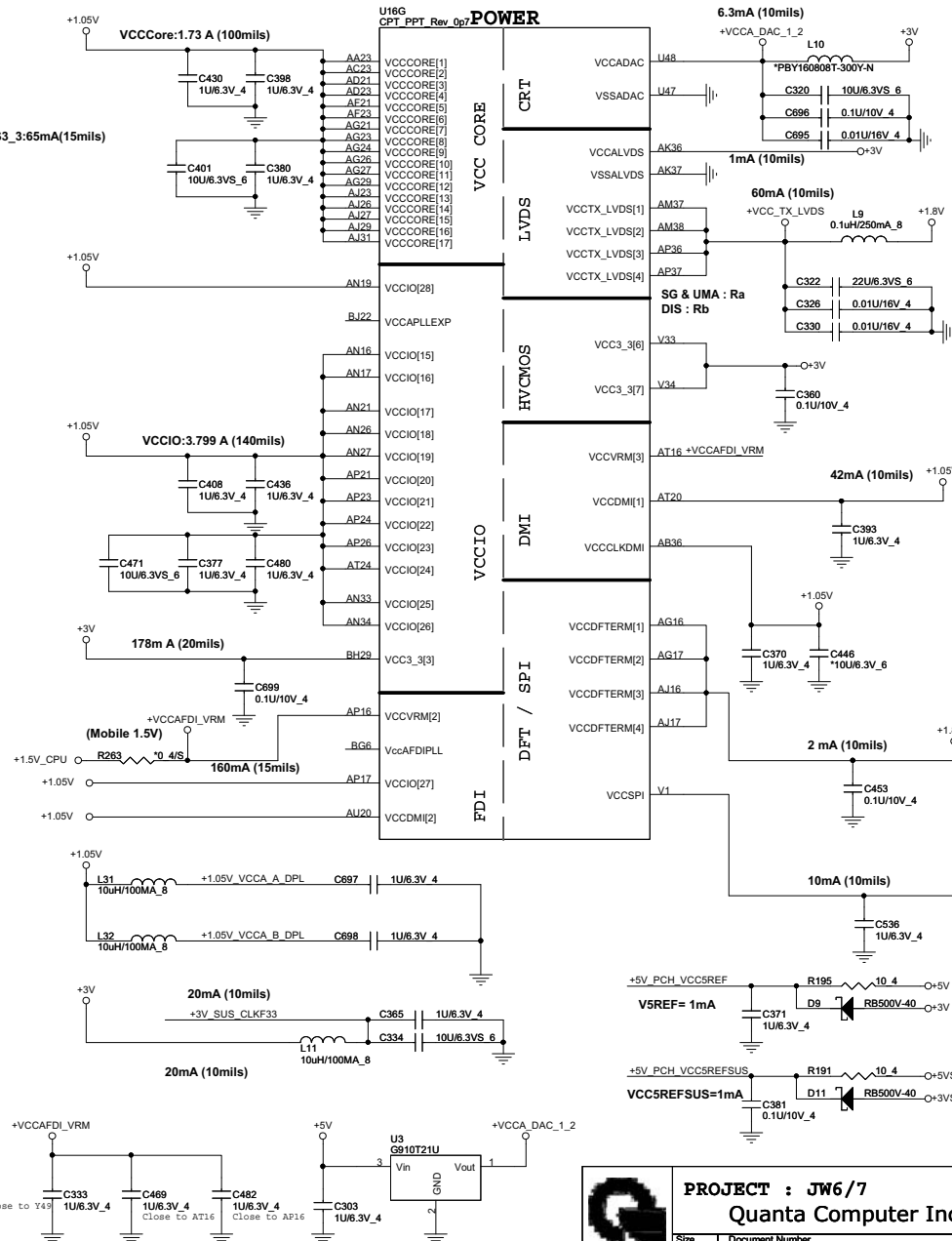


(6,7,8,9,12,13,14,18,21,22,23,24,25,27,28,29,30,35,37,39,41)
(7,21,22,23,27,28,41)
(4,7,36)
(2,4,6,7,8,26,29,35,38,39)
(6,7,8,9,21,26,27,29,30,32,35,36,38,41)
(21,23,26,32,33,34,37,39,40,41)

(6,7,26) +3V_RTC
(2,4,12,13,33,38) +1.5VSUS
(2,4,27,28) +1.5V_CPU

Cougar Point/Panther Point (POWER)

U16G
CPT PPT Rev 0n7



Close to Y49 C333 1U/6.3V_4 C469 1U/6.3V_4 Close to AT16 C482 1U/6.3V_4 Close to AP16 C303 1U/6.3V_4



PROJECT : JW6/7
Quanta Computer Inc.

Size Custom	Document Number PCH 5/6 (Power)	Re A
Date: Friday, May 11, 2012	Sheet 10 of 42	

Cougar Point/Panther Point (GND)

U16I
CPT_PPT_Rev_0p7

AY4	VSS[159]	H46	VSS[259]
AY42	VSS[160]	K18	VSS[260]
AY46	VSS[161]	K26	VSS[261]
AY8	VSS[162]	K39	VSS[262]
B11	VSS[163]	K46	VSS[263]
B15	VSS[164]	K7	VSS[264]
B19	VSS[165]	L18	VSS[265]
B23	VSS[166]	L2	VSS[266]
B27	VSS[167]	L20	VSS[267]
B31	VSS[168]	L26	VSS[268]
B35	VSS[169]	L28	VSS[269]
B39	VSS[170]	L36	VSS[270]
B7	VSS[171]	L48	VSS[271]
F45	VSS[172]	M12	VSS[272]
B812	VSS[173]	P16	VSS[273]
B816	VSS[174]	M18	VSS[274]
B820	VSS[175]	M22	VSS[275]
B822	VSS[176]	M24	VSS[276]
B824	VSS[177]	M30	VSS[277]
B826	VSS[178]	M32	VSS[278]
B830	VSS[179]	M34	VSS[279]
B838	VSS[180]	M38	VSS[280]
B84	VSS[181]	M4	VSS[281]
B846	VSS[182]	M42	VSS[282]
BC14	VSS[183]	M46	VSS[283]
BC18	VSS[184]	M6	VSS[284]
BC2	VSS[185]	N18	VSS[285]
BC22	VSS[186]	P30	VSS[286]
BC26	VSS[187]	N47	VSS[287]
BC32	VSS[188]	P11	VSS[288]
BC34	VSS[189]	P18	VSS[289]
BC36	VSS[190]	T33	VSS[290]
BC40	VSS[191]	P40	VSS[291]
BC42	VSS[192]	P43	VSS[292]
BC48	VSS[193]	P47	VSS[293]
BD46	VSS[194]	P7	VSS[294]
BD5	VSS[195]	R2	VSS[295]
BE22	VSS[196]	R48	VSS[296]
BE26	VSS[197]	T12	VSS[297]
BE40	VSS[198]	T31	VSS[298]
BE10	VSS[199]	T37	VSS[299]
BE12	VSS[200]	T4	VSS[300]
BF16	VSS[201]	W34	VSS[301]
BF20	VSS[202]	T46	VSS[302]
BF22	VSS[203]	T47	VSS[303]
BF24	VSS[204]	T8	VSS[304]
BF26	VSS[205]	V11	VSS[305]
BF28	VSS[206]	V17	VSS[306]
BD3	VSS[207]	V26	VSS[307]
BF30	VSS[208]	V27	VSS[308]
BF38	VSS[209]	V29	VSS[309]
BF40	VSS[210]	V21	VSS[310]
BF8	VSS[211]	V36	VSS[311]
BG17	VSS[212]	V39	VSS[312]
BG21	VSS[213]	V43	VSS[313]
BG23	VSS[214]	V7	VSS[314]
BG33	VSS[215]	W17	VSS[315]
BG44	VSS[216]	W19	VSS[316]
BH11	VSS[217]	W2	VSS[317]
BH15	VSS[218]	W27	VSS[318]
BH17	VSS[219]	W48	VSS[319]
BH18	VSS[220]	Y38	VSS[320]
H10	VSS[221]	Y4	VSS[321]
BH27	VSS[222]	Y42	VSS[322]
BH31	VSS[223]	Y46	VSS[323]
BH33	VSS[224]	Y8	VSS[324]
BH35	VSS[225]	Y8	VSS[325]
BH39	VSS[226]	BG29	VSS[326]
BH43	VSS[227]	N24	VSS[327]
BH7	VSS[228]	A13	VSS[328]
D3	VSS[229]	AD47	VSS[329]
D12	VSS[230]	B43	VSS[330]
D16	VSS[231]	BE10	VSS[331]
D18	VSS[232]	BG41	VSS[332]
D22	VSS[233]	G14	VSS[333]
D24	VSS[234]	H18	VSS[334]
D26	VSS[235]	T36	VSS[335]
D30	VSS[236]	BG22	VSS[336]
D32	VSS[237]	BG24	VSS[337]
D34	VSS[238]	AP13	VSS[338]
D38	VSS[239]	M14	VSS[339]
D42	VSS[240]	AP3	VSS[340]
D8	VSS[241]	AP21	VSS[341]
E18	VSS[242]	BE16	VSS[342]
E26	VSS[243]	BC16	VSS[343]
G18	VSS[244]	BG28	VSS[344]
G20	VSS[245]	B128	VSS[345]
G26	VSS[246]		
G28	VSS[247]		
G36	VSS[248]		
G46	VSS[249]		
H12	VSS[250]		
H18	VSS[251]		
H22	VSS[252]		
H24	VSS[253]		
H26	VSS[254]		
H30	VSS[255]		
H32	VSS[256]		
H34	VSS[257]		
F3	VSS[258]		

Cougar Point/Panther Point (GND)

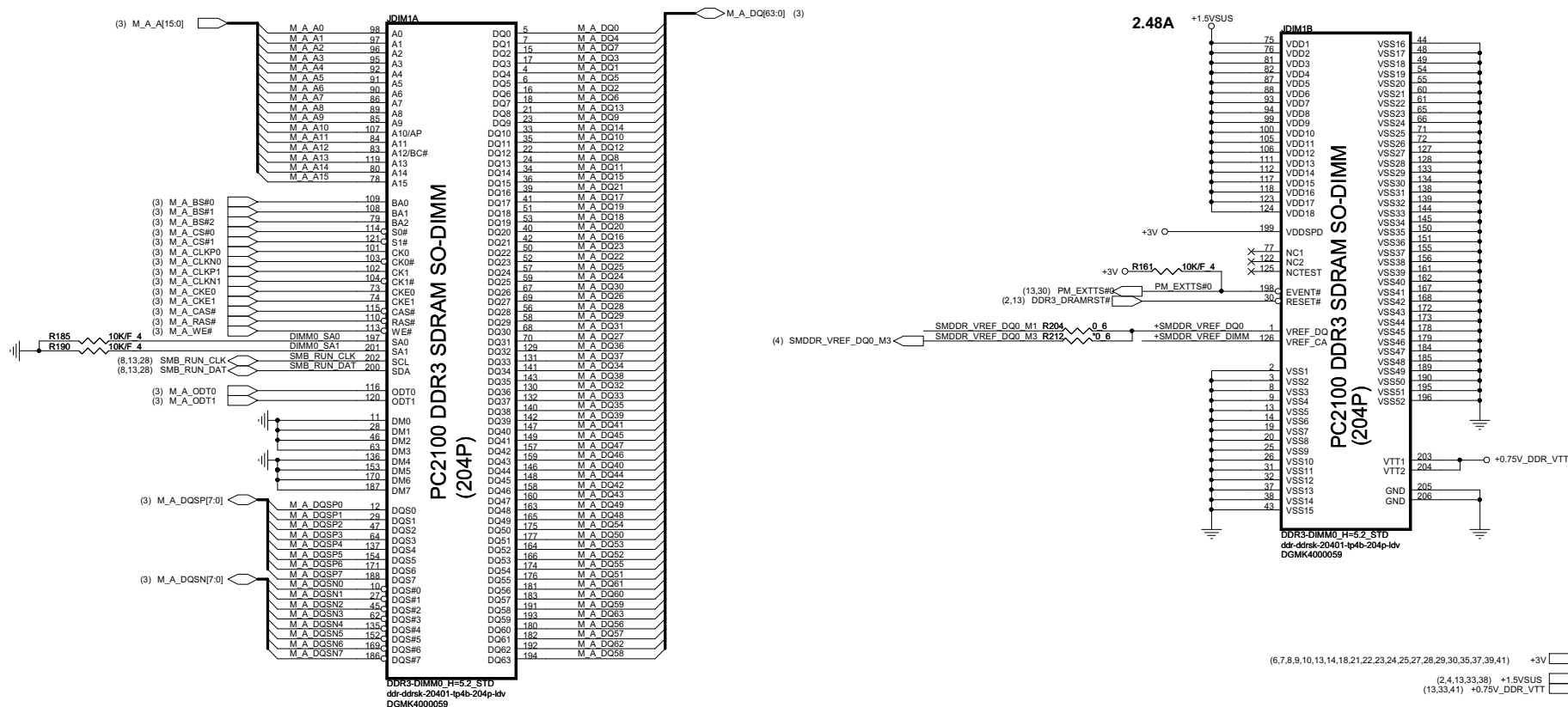
U16H
CPT_PPT_Rev_0p7

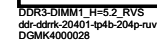
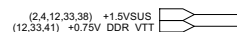
H5	VSS[0]	VSS[80]	AK38
AA17	VSS[1]	VSS[81]	AK4
AA2	VSS[2]	VSS[82]	AK42
AA3	VSS[3]	VSS[83]	AK46
AA33	VSS[4]	VSS[84]	AK6
AA34	VSS[5]	VSS[85]	AL16
AB11	VSS[6]	VSS[86]	AL17
AB14	VSS[7]	VSS[87]	AL19
AB30	VSS[8]	VSS[88]	AL2
AB4	VSS[9]	VSS[89]	AL21
AB43	VSS[10]	VSS[90]	AL23
AB5	VSS[11]	VSS[91]	AL26
AB7	VSS[12]	VSS[92]	AL27
AC19	VSS[13]	VSS[93]	AL31
AC2	VSS[14]	VSS[94]	AL33
AC21	VSS[15]	VSS[95]	AL34
AC24	VSS[16]	VSS[96]	AL48
AC33	VSS[17]	VSS[97]	AM11
AC34	VSS[18]	VSS[98]	AM14
M4	VSS[19]	VSS[99]	AM36
AD10	VSS[20]	VSS[100]	AM39
AD11	VSS[21]	VSS[101]	AM43
AD12	VSS[22]	VSS[102]	AM46
AD13	VSS[23]	VSS[103]	AM7
AD19	VSS[24]	VSS[104]	AN2
AD24	VSS[25]	VSS[105]	AN29
P11	VSS[26]	VSS[106]	AN3
AD27	VSS[27]	VSS[107]	AN31
AD33	VSS[28]	VSS[108]	AP12
AD34	VSS[29]	VSS[109]	AP19
AD36	VSS[30]	VSS[110]	AP28
AD37	VSS[31]	VSS[111]	AP32
AD38	VSS[32]	VSS[112]	AP38
AD39	VSS[33]	VSS[113]	AP4
AD4	VSS[34]	VSS[114]	AP46
AD40	VSS[35]	VSS[115]	AP8
AD42	VSS[36]	VSS[116]	AR2
AD43	VSS[37]	VSS[117]	AR48
AD45	VSS[38]	VSS[118]	AT11
AD46	VSS[39]	VSS[119]	AT13
AD8	VSS[40]	VSS[120]	AT18
AE2	VSS[41]	VSS[121]	AT22
AE3	VSS[42]	VSS[122]	AT26
AE10	VSS[43]	VSS[123]	AT28
AE12	VSS[44]	VSS[124]	AT30
AD14	VSS[45]	VSS[125]	AT32
AD16	VSS[46]	VSS[126]	AT34
AE16	VSS[47]	VSS[127]	AT38
AF19	VSS[48]	VSS[128]	AT42
AF24	VSS[49]	VSS[129]	AT46
AF26	VSS[50]	VSS[130]	AT7
AF27	VSS[51]	VSS[131]	AU24
AF28	VSS[52]	VSS[132]	AV16
AF31	VSS[53]	VSS[133]	AV20
AF38	VSS[54]	VSS[134]	AV22
W2	VSS[55]	VSS[135]	AV24
AF4	VSS[56]	VSS[136]	AV30
AF42	VSS[57]	VSS[137]	AV38
AF5	VSS[58]	VSS[138]	AV43
AF7	VSS[59]	VSS[139]	AV8
AF8	VSS[60]	VSS[140]	AW14
AG19	VSS[61]	VSS[141]	AW18
AG2	VSS[62]	VSS[142]	AW2
AG31	VSS[63]	VSS[143]	AW22
AG48	VSS[64]	VSS[144]	AW26
AH11	VSS[65]	VSS[145]	AW28
AH3	VSS[66]	VSS[146]	AW32
AH36	VSS[67]	VSS[147]	AW34
AH39	VSS[68]	VSS[148]	AW36
AH40	VSS[69]	VSS[149]	AW40
AH42	VSS[70]	VSS[150]	AW48
AH46	VSS[71]	VSS[151]	AY11
AH7	VSS[72]	VSS[152]	AY12
T36	VSS[73]	VSS[153]	AY22
A119	VSS[74]	VSS[154]	AY28
A121	VSS[75]	VSS[155]	
A124	VSS[76]	VSS[156]	
A133	VSS[77]	VSS[157]	
A134	VSS[78]	VSS[158]	
AK12	VSS[79]		
AK3	VSS[80]		



PROJECT : JW6/7
Quanta Computer Inc.

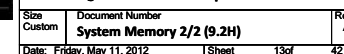
Size	Document Number	Rev
Custom	PCH 6/6 (Ground)	A
Date: Friday, May 11, 2012	Sheet	11 of 42

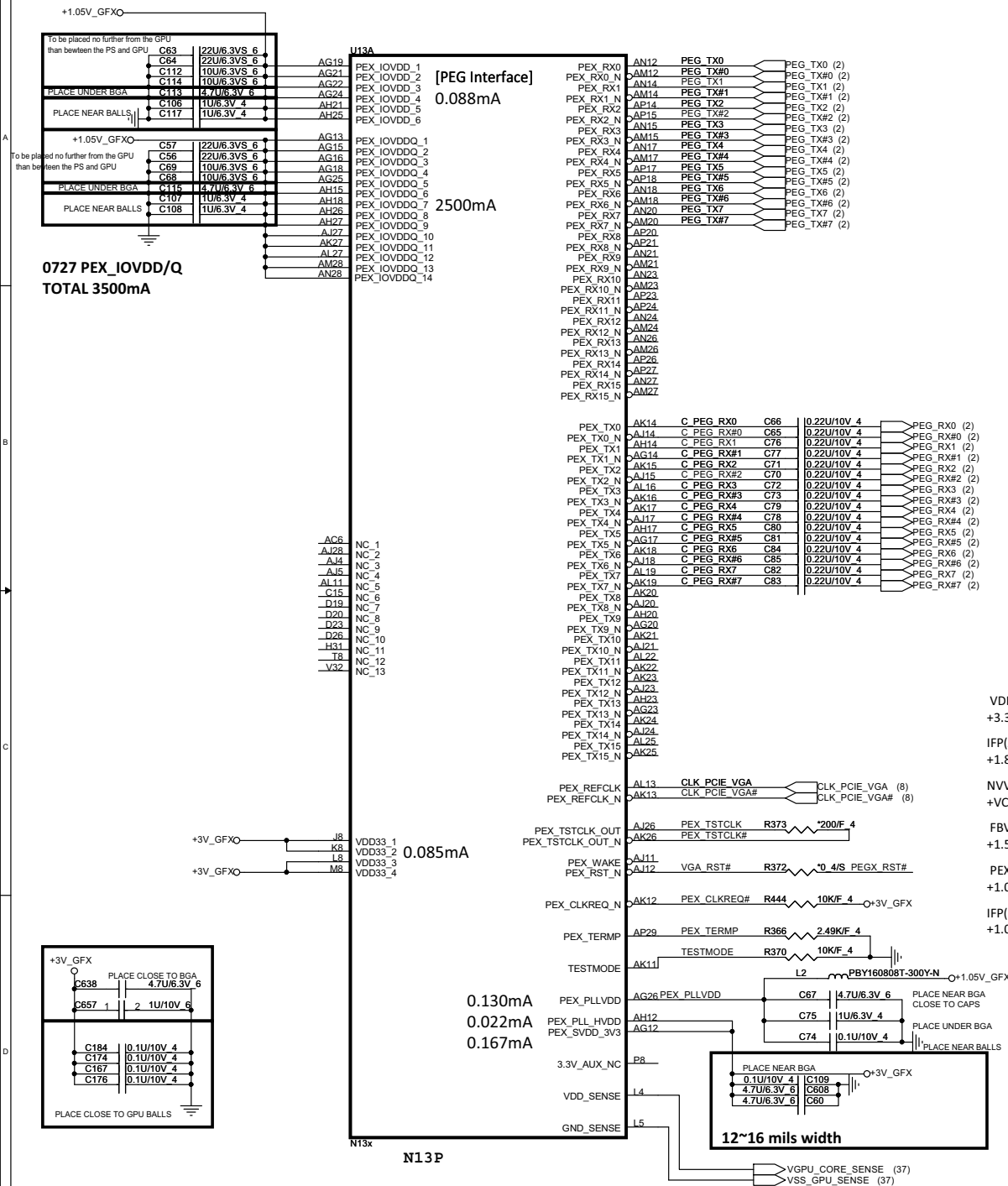




VREF DQ1 M1 Solution

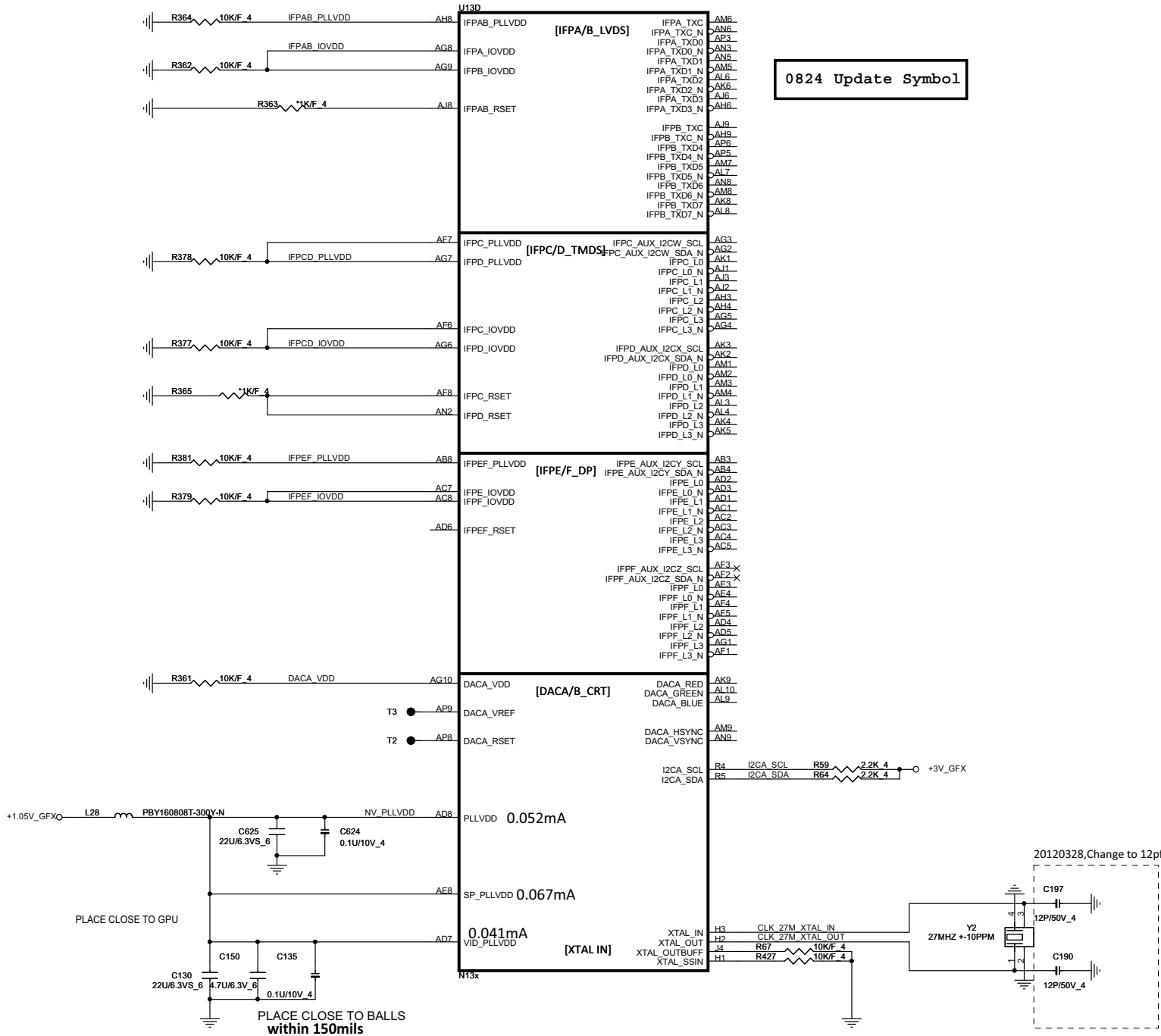
The diagram illustrates the VREF DQ1 M1 solution. It features a circuit where the SMDR_VREF_DQ1_M1 signal is connected to the gate of an NMOS transistor Q21 (AO3416). The source of Q21 is connected to ground. The drain of Q21 is connected to the DDR_VTTREF signal through a resistor R216 (0.6 ohms). Additionally, the drain of Q21 is connected to a +1.5VSUS supply through a resistor R231 (1K/4) and to ground through a resistor R232 (1K/4).





(14,15,18,38) +1.05V_GFX
(14,17,18,37,38) +3V_GFX

0824 Update Symbol



PROJECT : JW6/7

Quanta Computer Inc.

Size A3	Document Number DGPU 3/5 (Display)	Rev A
Date: Friday, May 11, 2012		
Sheet 16 of 42		

Net name	N13M-GE2	N13P-GS (QS)
ROM_SI		
ROM_SO	PD 10K	PU 10K
ROM_SCLK	PD 15K	PU 5K
STRAP0	PU 45K	PU 45K
STRAP1	PD 45K	PD 5K
STRAP2	PU 15K	PD 15K
STRAP3	UN-STUFF	PD 5K
STRAP4	UN-STUFF	PD 45K

Net name	N13P-GL
ROM_SI	
ROM_SO	PD 10K
ROM_SCLK	PD 15K
STRAP0	PU 45K
STRAP1	PD 5K
STRAP2	PU 10K
STRAP3	UN-STUFF
STRAP4	UN-STUFF

For N13M-GE2
ROM_SO PD 10K
ROM_SCLK PD 15K

For N13P-GS
ROM_SO PU 10K
ROM_SCLK PU 5K

N13M-GE2-A1 ID:0X0DEA
N13P-GS ID:0X0FD2
N13P-GL-A1 ID:0X0DE9

Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

Default: Hynix VRAM

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	1001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0011
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFCG[3]	3GIO_PADCFCG[2]	3GIO_PADCFCG[1]	3GIO_PADCFCG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	0111
STRAP3	SOR2_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	XXXX
STRAP4	RESERVED	PCI SPEED CHANGE GEN3	PCI_MAX SPEED	DP_PLL_VDD33	XXXX

For N13M-GE2, N13M-GS (QS)
Default : 2G Samsung

VRAM Configuration Table

ROM_SI
1G Hynix 64Mx16 -->15K PD
1G Samsung 64Mx16 -->20K PD
2G Hynix 128Mx16 -->35K PD
2G Samsung 128Mx16 -->45K PD

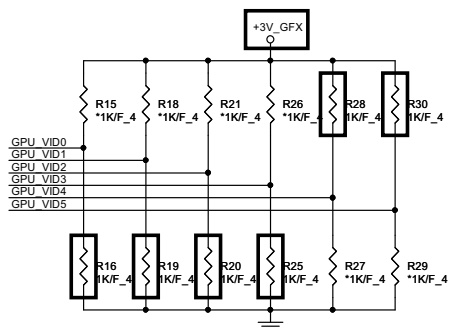
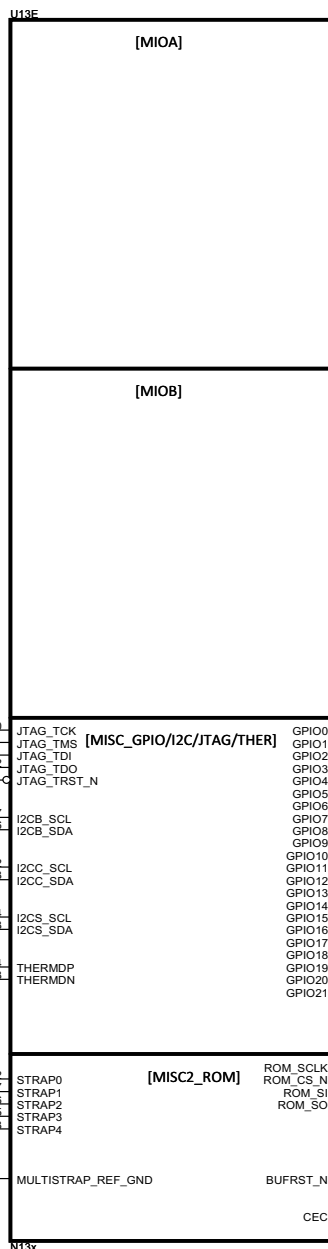
GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

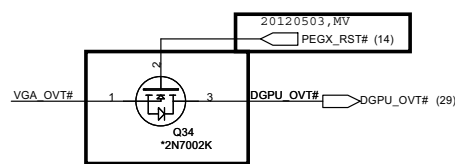


PROJECT : JW6/7
Quanta Computer Inc.

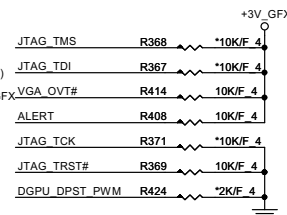
Size Custom	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	A
Date: Tuesday, May 15, 2012	Sheet	17 of 42



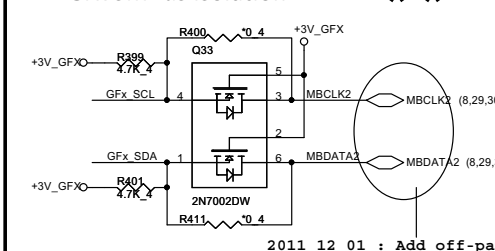
VID 0 0 0 0 1 1 0 ---> 0.9V N13P-GS-A2
VID 0 0 1 1 0 1 0 ---> 0.95V N13P-GL-A1



	N13M-GE2	N13P-GS
Ra	Un-Stuff	Stuff
Qa	Stuff	Un-Stuff



GFx SMBus Isolation

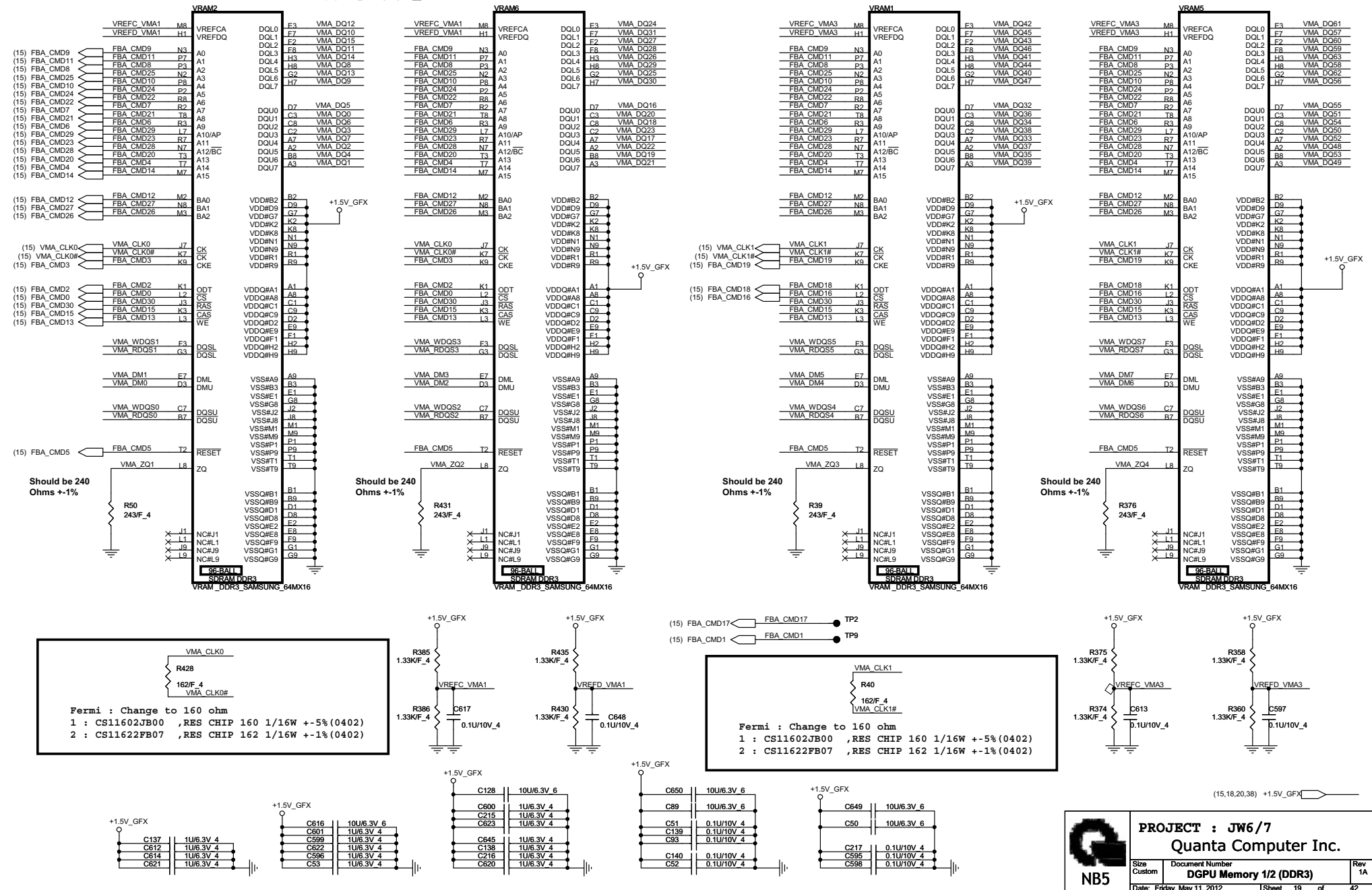


2011 12 01 : Add off-page connector

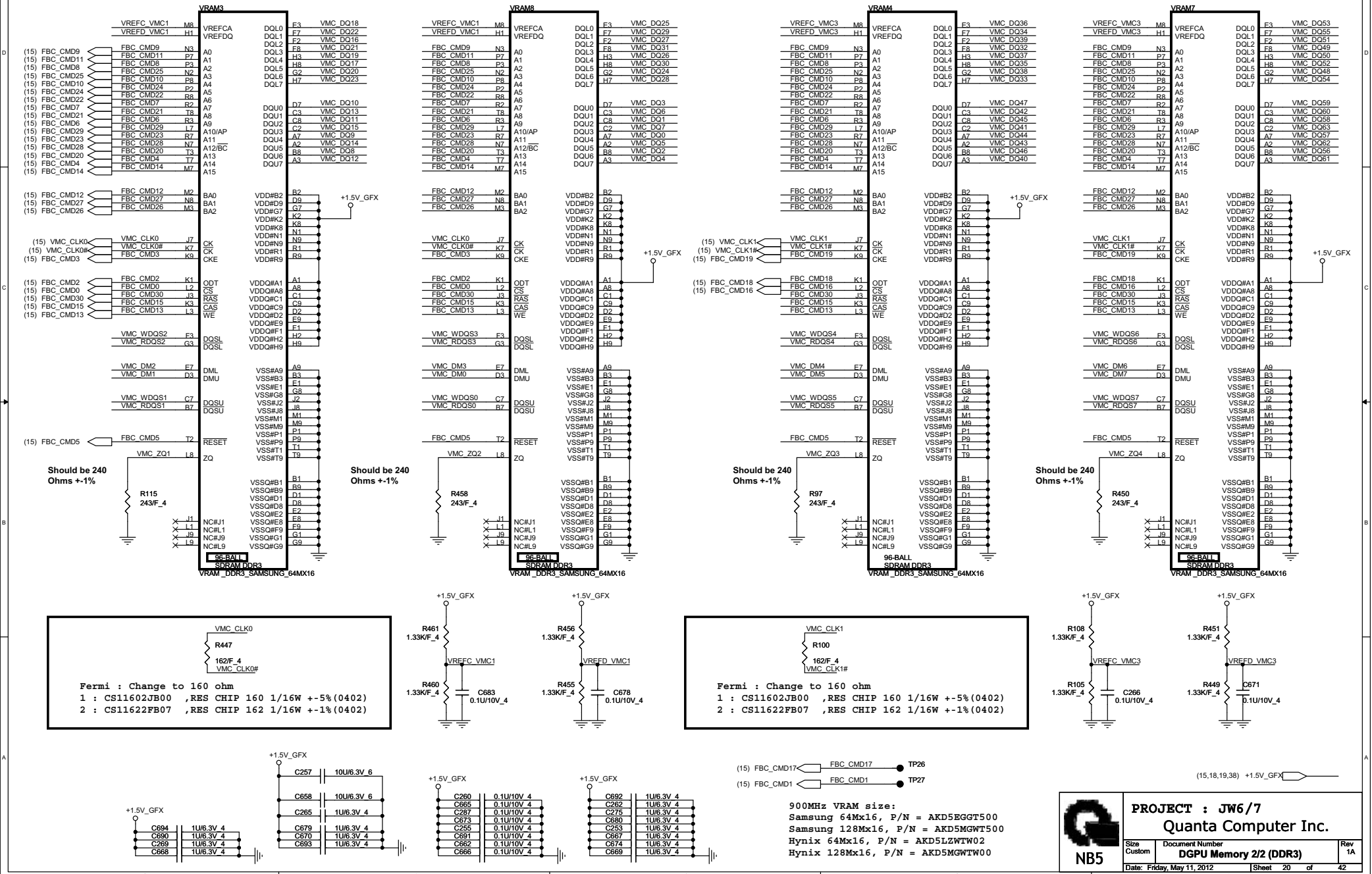
	N13M-GE2	N13P-GS
Stuff Rc		Un-stuff Rc

900MHz VRAM size:
 Samsung 64Mx16, P/N = AKD5EGGT500
 Samsung 128Mx16, P/N = AKD5MGWT500
 Hynix 64Mx16, P/N = AKD5LZWTW02
 Hynix 128Mx16, P/N = AKD5MGWTW00

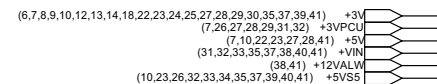
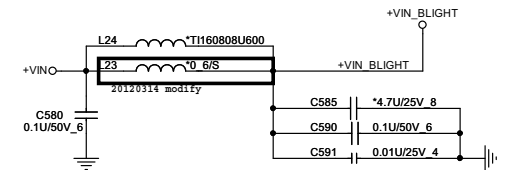
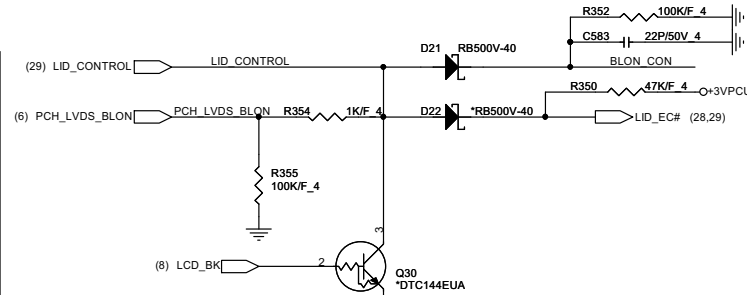
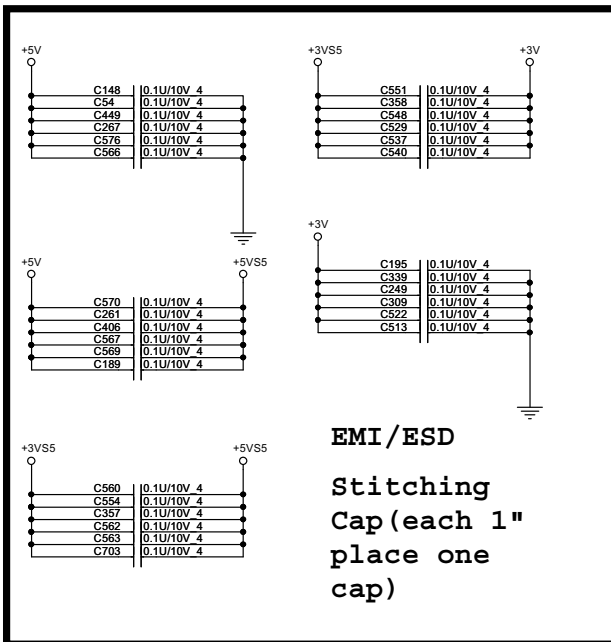
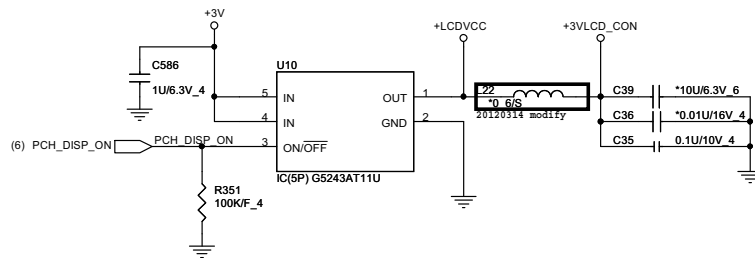
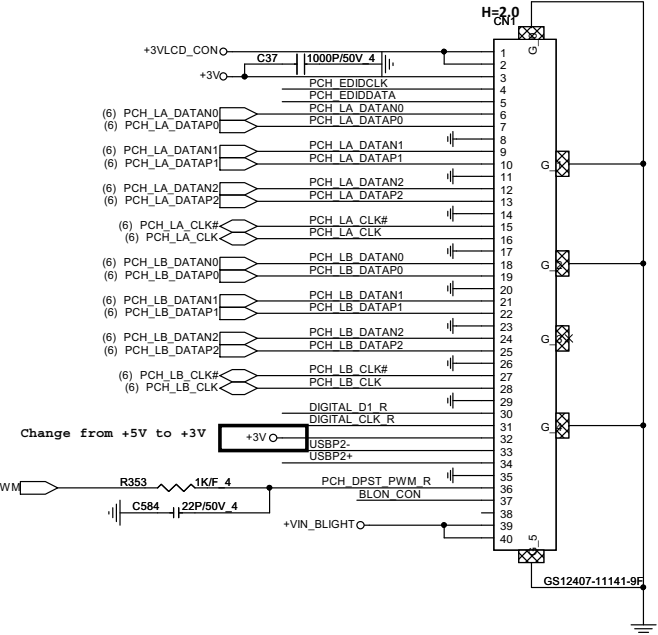
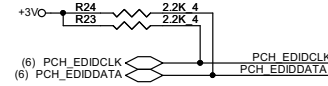
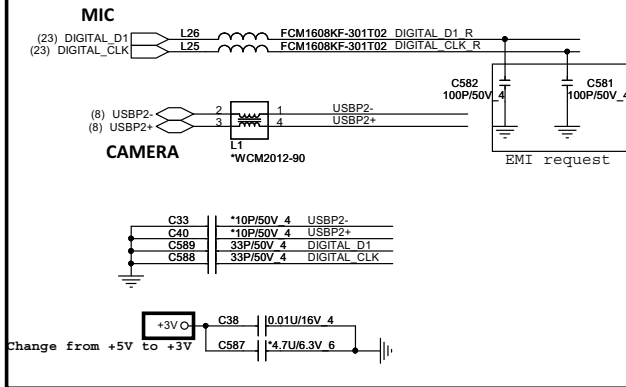
CHANNEL A: 256MB/512MB DDR3



CHANNEL B: 256MB/512MB DDR3



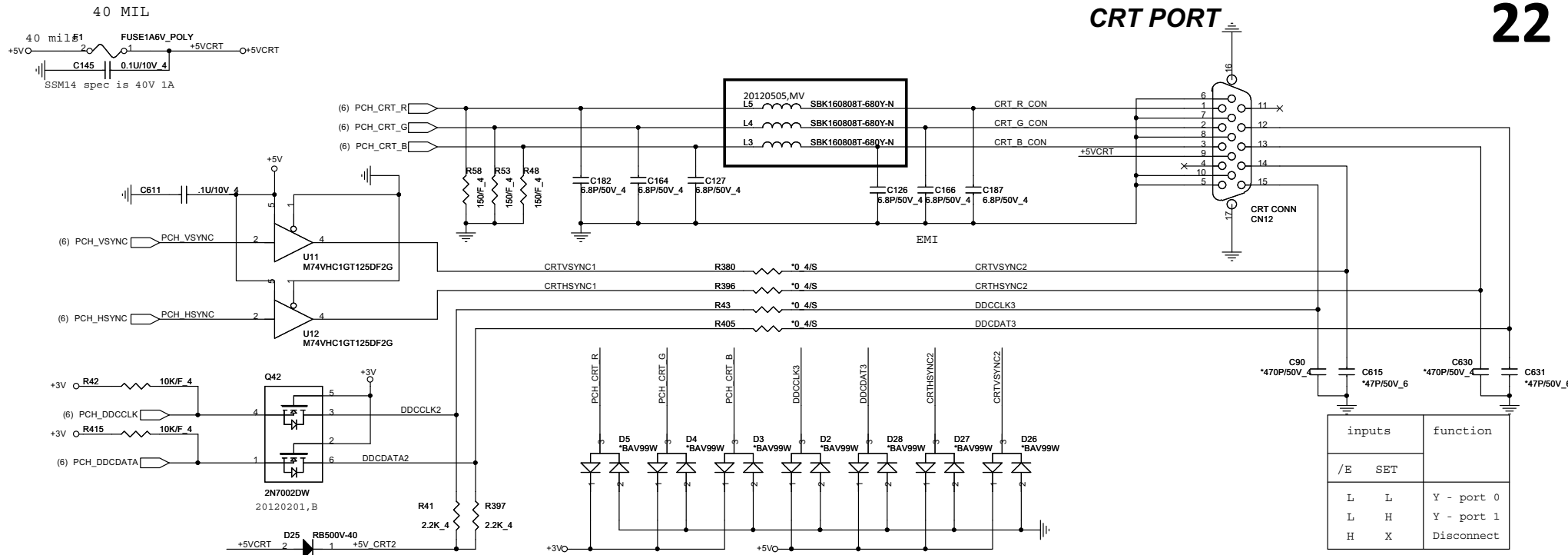
USB Camera Connector



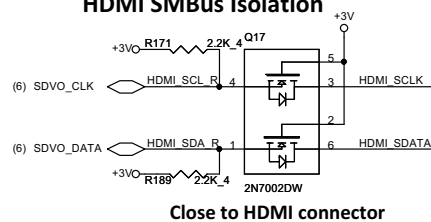
PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	A
Date: Friday, May 11, 2012	Sheet 21 of 42	

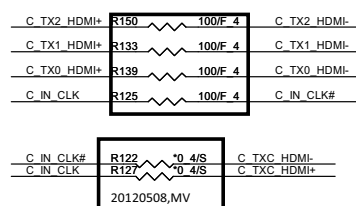
CRT PORT



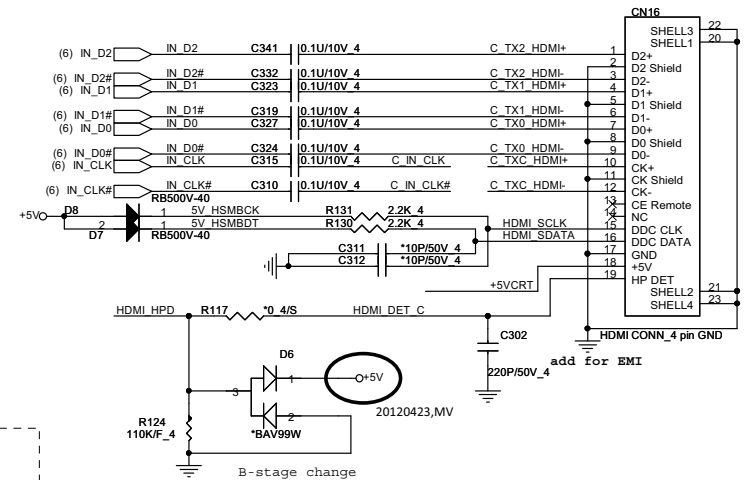
HDMI SMBus Isolation



EMI Solution

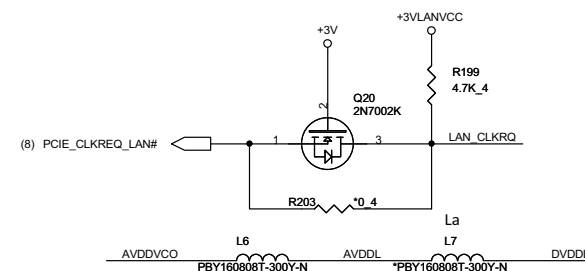


HDMI PORT

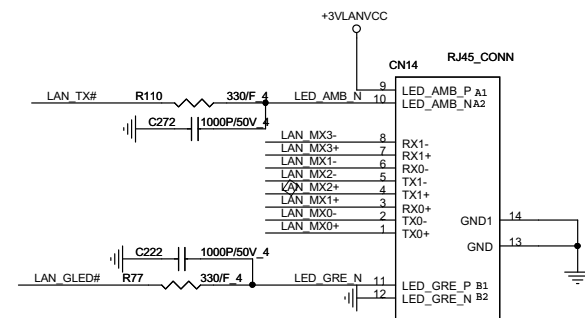
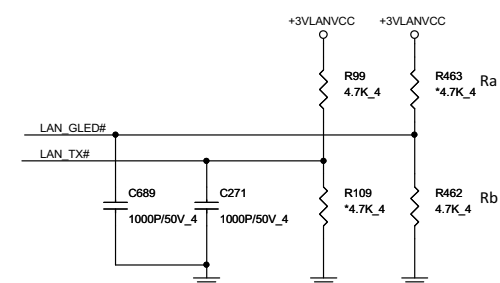


PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Connector	A
Date: Friday, May 11, 2012	Sheet 22of 42	

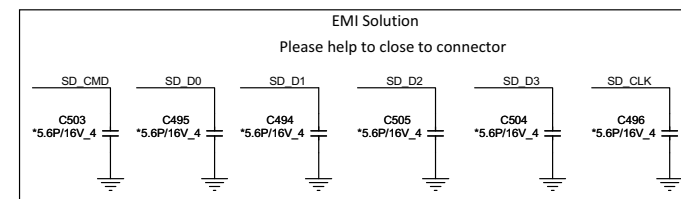


Rb	Stuff
La	No stuff
Lb	No stuff
C-group	No stuff
Ra	No stuff



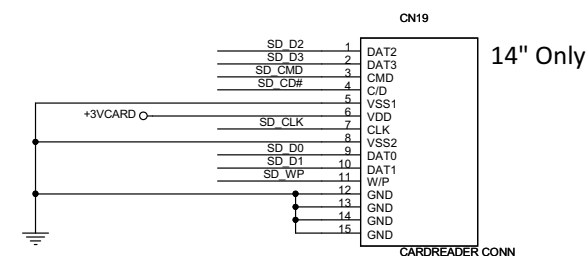
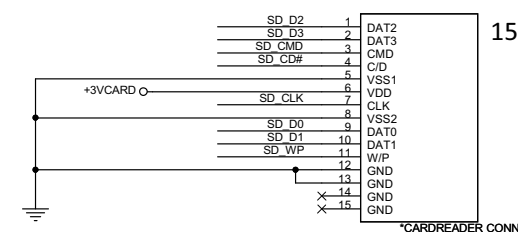
Size Custom	Document Number LAN Controller (Atheros AR8161)
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Size Custom	Document Number LAN Controller (Atheros_AR8161)	Re /
Date: Friday, May 11, 2012	Sheet 24 of 42	



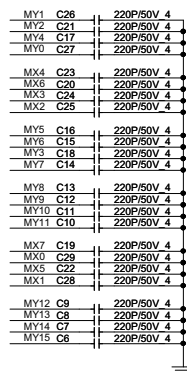
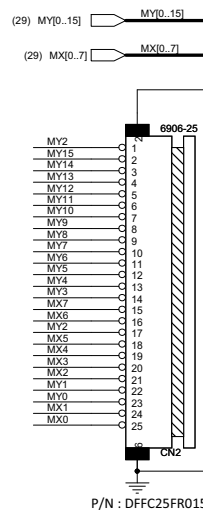
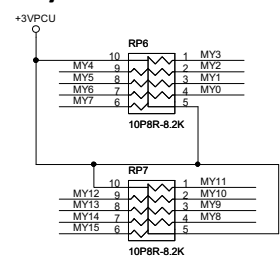
Close to chip pin

SD / MMC
CARD READER

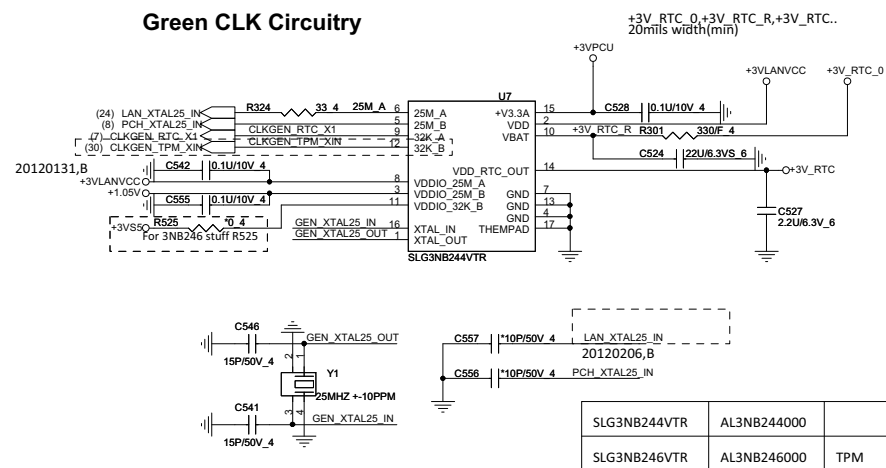


Size Custom	Document Number Card Reader control (RTS5229-GR)	Rev A
Date: Tuesday, May 15, 2012	Sheet 25 of 42	

Keyboard Connector

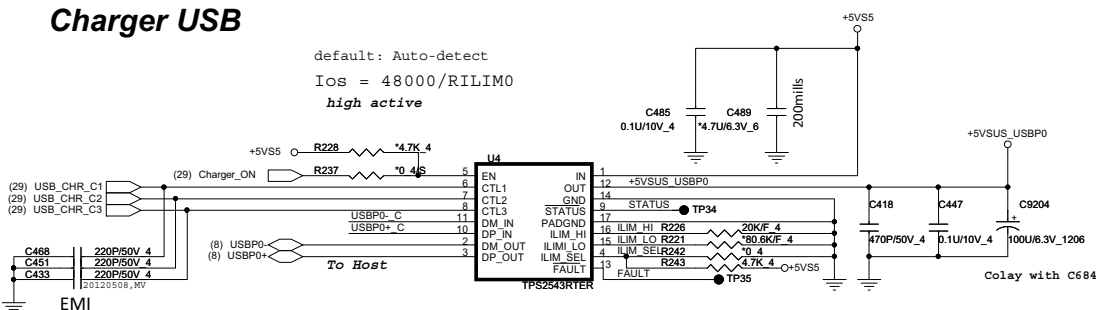


Green CLK Circuitry



Charger USB

default: Auto-detect
Ios = 48000/RILIM0
high active



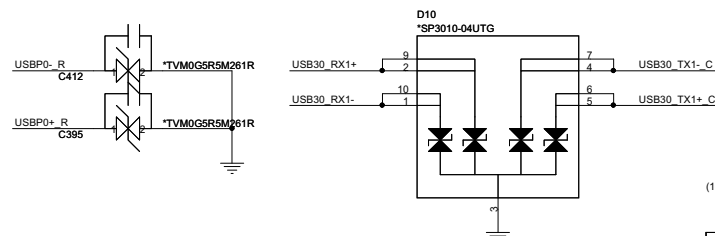
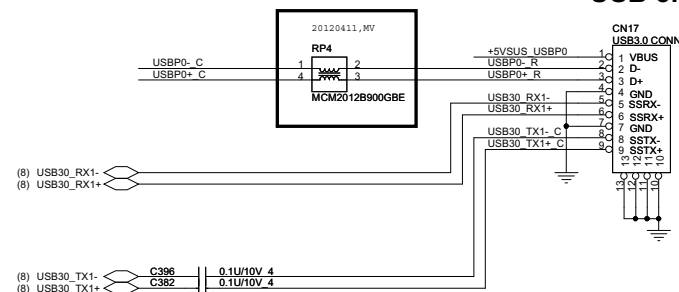
TPS2543/45 Control Truth Table

CTL1	CTL2	CTL3	ILIM_SEL	Charging Mode	Current Limit Setting	TPS2543 STATUS Output (active low)
0	0	0	1	Discharge	NA	off
0	0	1	1	DCP/auto	IOS_PW & ILIM_HI (1)	DCP load present
0	1	0	1	SDP	ILIM_HI	off
0	1	1	1	DCP/auto	ILIM_HI	DCP load present
1	1	0	1	SDP	ILIM_HI	off
1	1	1	1	CDP	ILIM_HI	CDP load present

(1) ILIM_HI: 20K(R5233), 2.4A

USB3.0 X 1/USB2.0 COMBO

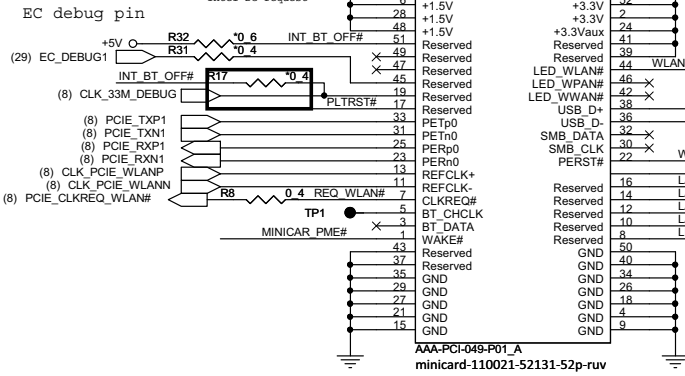
USB 3.0

(10,21,32,33,34,35,37,39,40,41) +5VS5
(7,21,27,28,29,31,32) +3VPCU

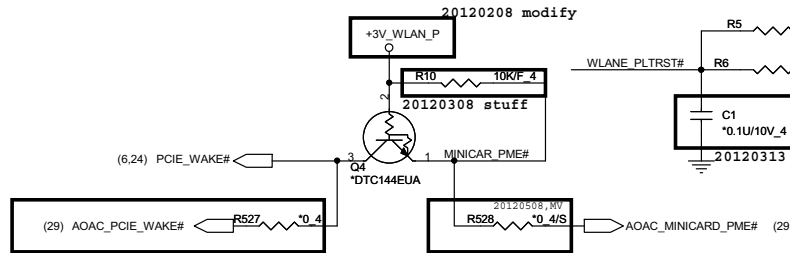
PROJECT : JW6/7
Quanta Computer Inc.

Size Custom Document Number USB 3.0/KB/Green CLK Rev A
Date: Friday, May 11, 2012 Sheet 26 of 42

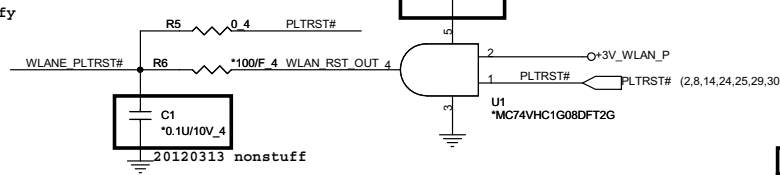
Mini Card WLAN/BT(Optional)



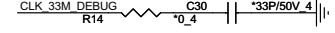
Support Wake Function(Reserve)



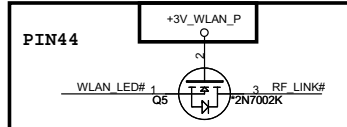
Mini Card Reset



For EMI Suggestion



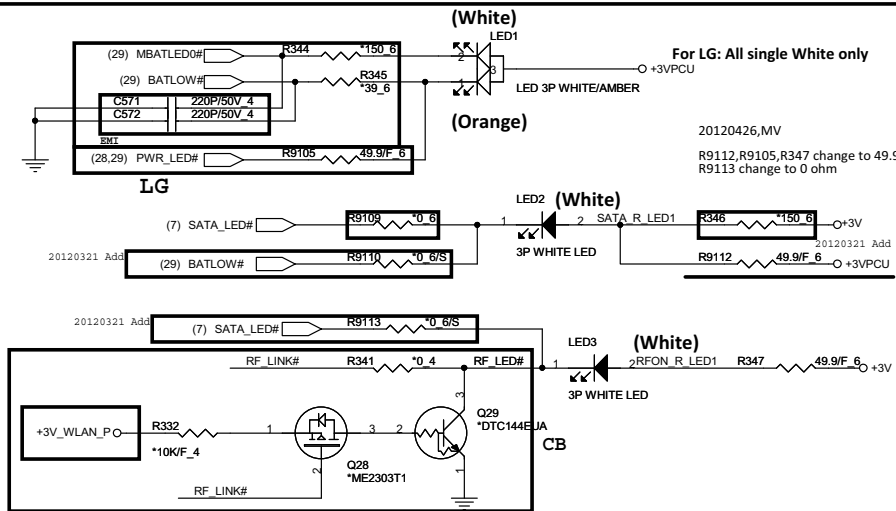
Avoid leakage issue



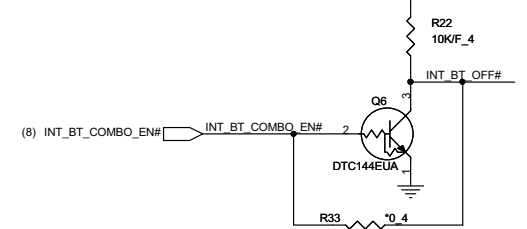
LG mini-pcie power status

WLAN	Bluetooth	+3V WLAN P
Radio-ON	Radio-ON	Power-ON
Radio-ON	Radio-OFF	Power-ON
Radio-OFF	Radio-ON	Power-ON
Radio-OFF	Radio-OFF	Power-OFF

LED Status



PIN19, 51



PROJECT : JW6/7
Quanta Computer Inc.

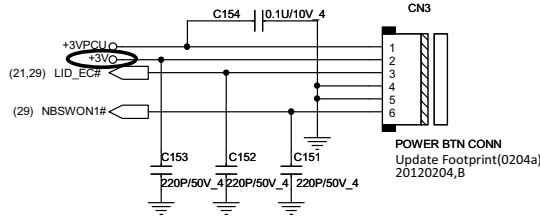
Size	Document Number	Rev
Custom	MINI-PCIE/LED	A
Date: Monday, May 14, 2012	Sheet	27 of 42

Left side Power Button Connector(1)

For CB

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

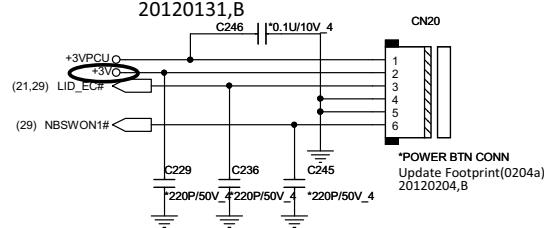
20120507,MV
Change CN3/CN20#2 to +3V



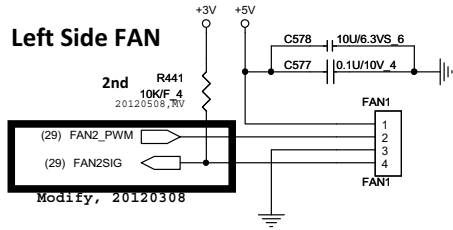
Right side Power Button Connector(2)

For LG

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : +3V
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

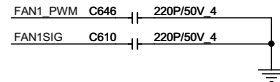
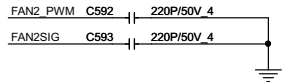
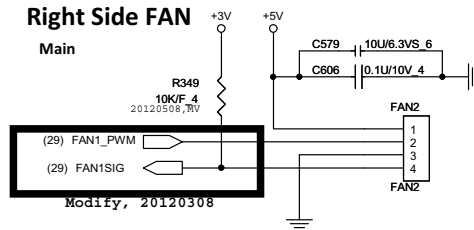


Left Side FAN

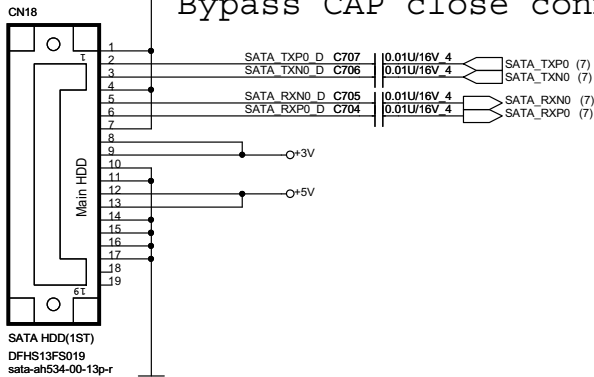


Right Side FAN

Main



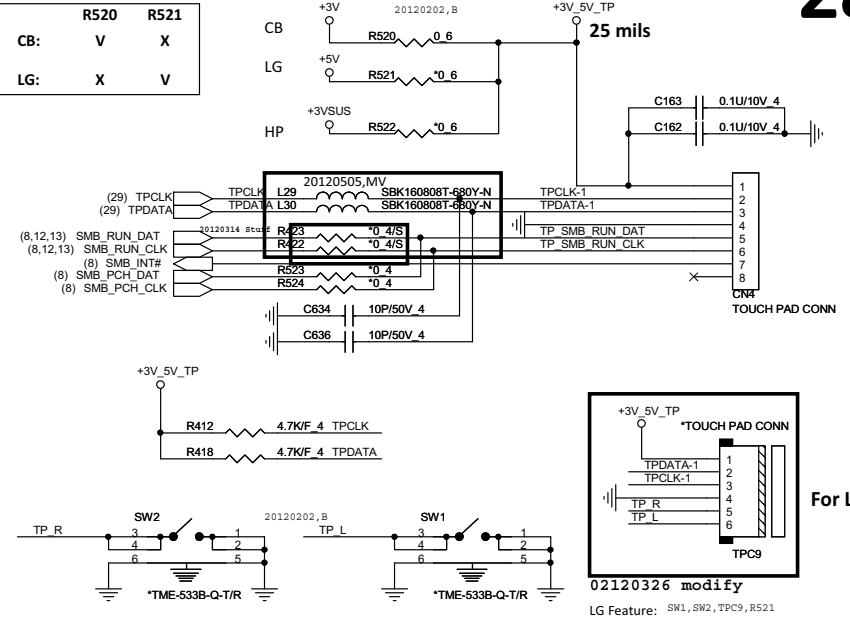
Bypass CAP close conn



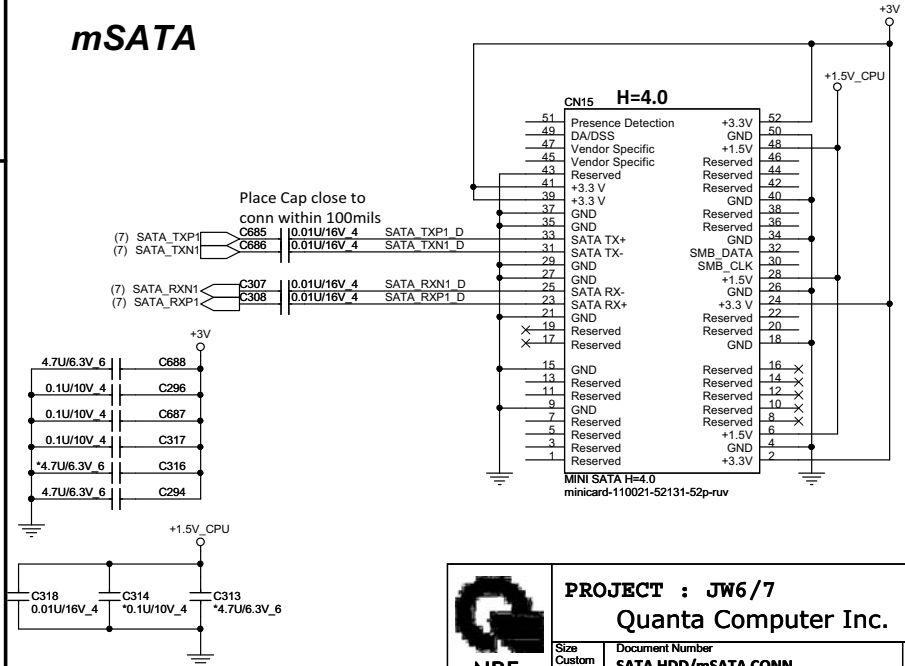
SATA HDD Connector(Cable type)

Touch Pad Connector

	R520	R521
CB:	V	X
LG:	X	V



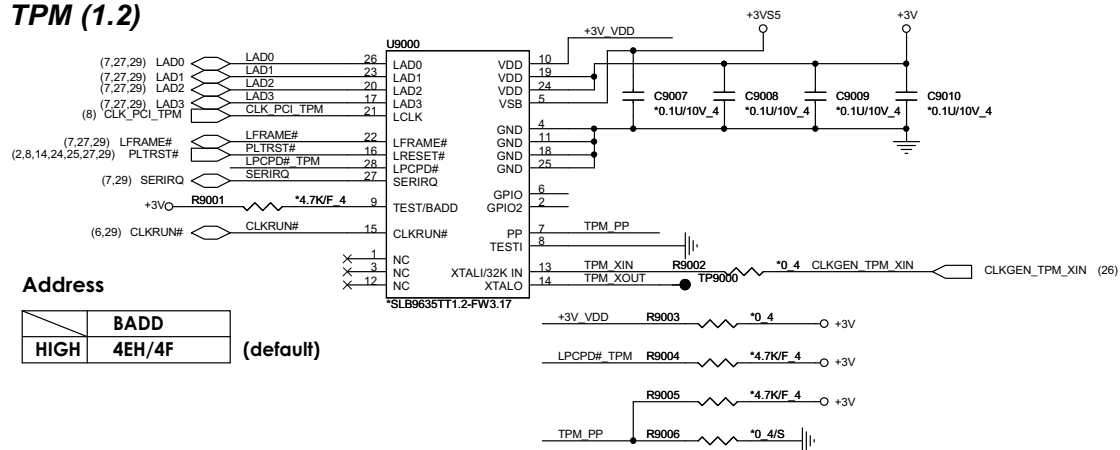
Mini PCI-E Card 2- Full size mSATA



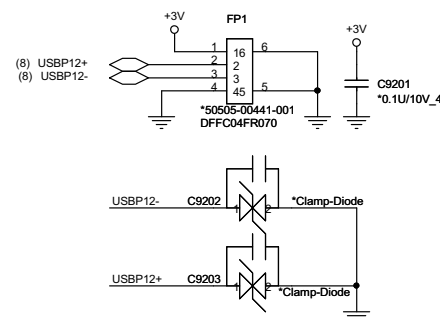
PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/mSATA CONN	A
Date: Tuesday, May 15, 2012	Sheet	28 of 42

TPM (1.2)



Finger Printer

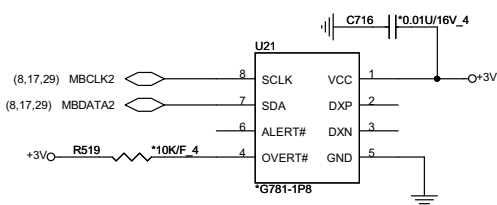


30

Local Thermal Sensor

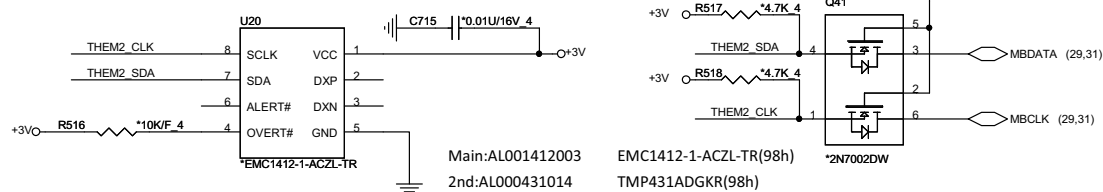
20120131,B

Thermal Solution(Close to GPU)



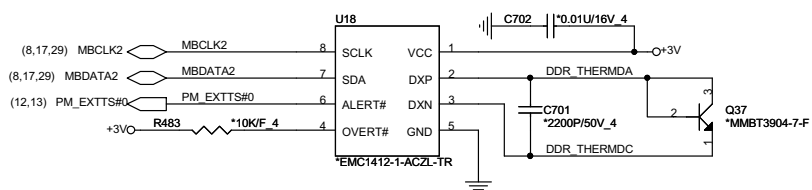
Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

Thermal Solution(Close to CRT)

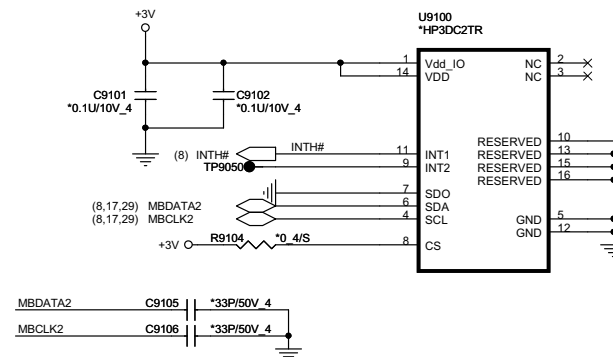


Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

DDR3 Thermal Sensor



Accelerometer Sensor



SGT-LIS302DLTR interrupt pin default is low / active Hi , BIOS need to programming 22h to change status from active Hi to low

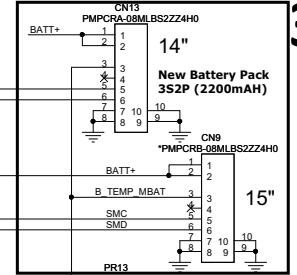
I2C (ST HP3DC2) SDO,Pin7

0x50	Gnd Default
0x52	VDD

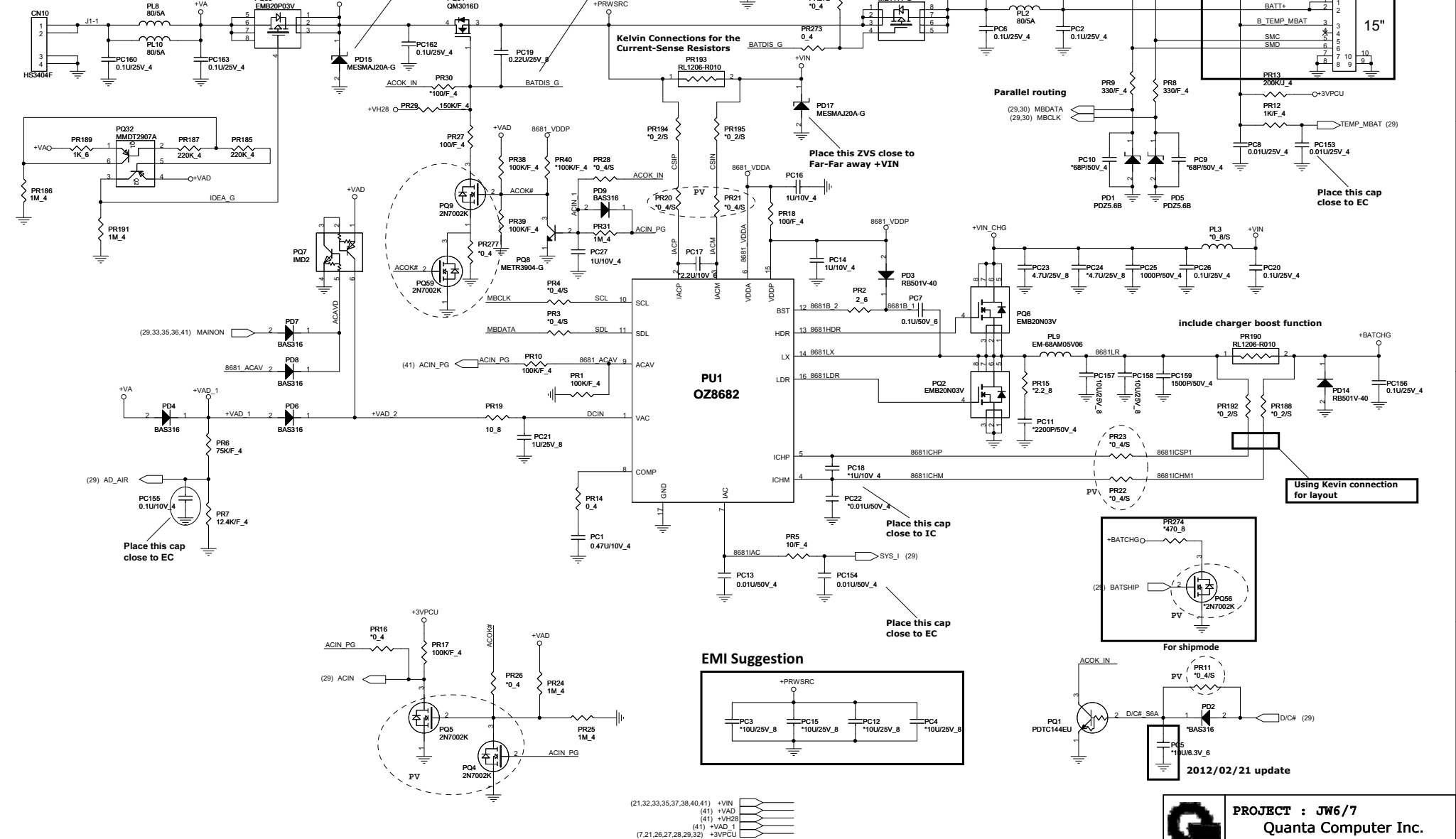


PROJECT : JW6/7
Quanta Computer Inc.

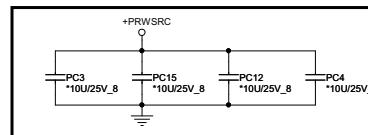
Size	Document Number	Rev
Custom	G-sensor/FP/TPM/THEM	A
Date: Friday, May 11, 2012	Sheet 30 of 42	



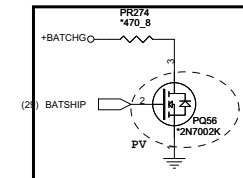
**Place this cap
close to EC**



EMI Suggestion



For shipmode



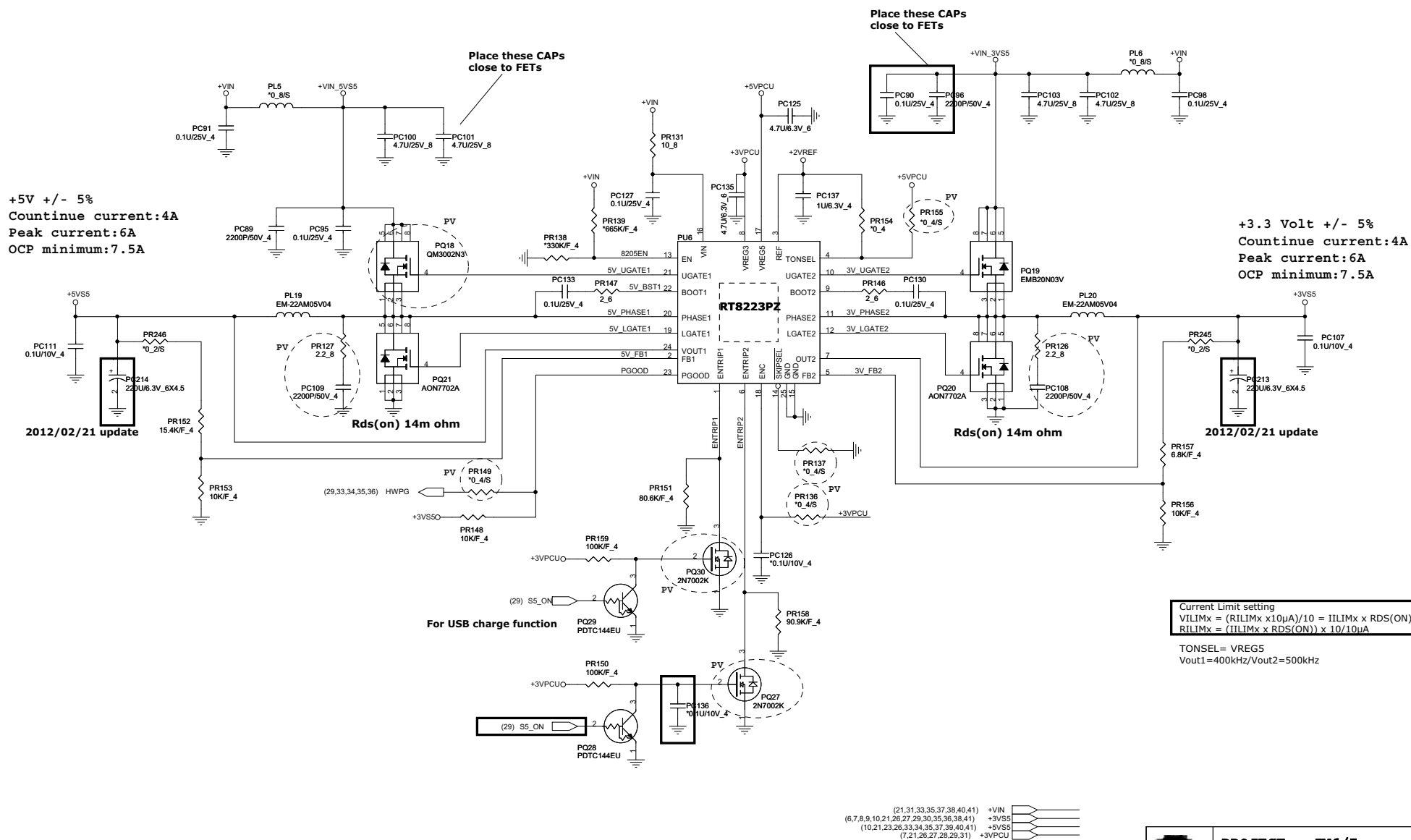
2012/02/21 update



PROJECT : JW6/7
Quanta Computer Inc.

Size Custom	Document Number Charger (OZ8682)	Rev A
Date: Friday, May 11, 2012	Sheet 31 of	42

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VSS (RT8223P)	A
Date: Friday, May 11, 2012	Sheet	32 of 42

(VTT/2A)

+0.75V_DDR_VTT

PC152 10U/6.3V_8
PC150 10U/6.3V_8
+1.5VSUS PC148 0.1U/50V_6

+VIN_DDR

PL25 0.8/S

+VIN

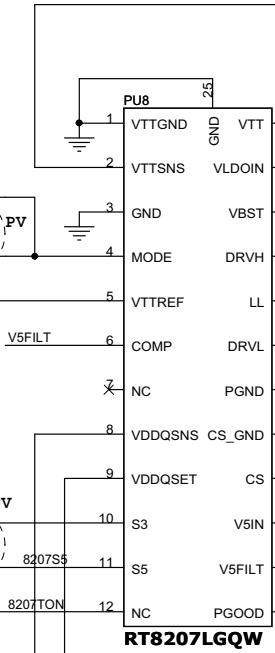
PC251 0.1U/25V_4
PC252 4.7U/25V_8
PC147 4.7U/25V_8
PC149 2200P/50V_4
PC249 0.1U/25V_4

+1.5VSUS +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

(3mA)

(4,12,13) DDR_VTTREF

PR183 0.4
PR184 0.4/S
PC151 0.033U/10V_4



$$RILIM = ILIM \times RDS(ON) / 10\mu A$$

PQ53 EMB20N03V

PL24 EM-82BM05V04

PQ54 FDMS0310AS

RDSon = 5m ohm

Place this short pad
close to output CAP

RT8207LGQW

PR175 6.98K/F_4
PR176 0.4/S
PC143 1U/6.3V_4
PR174 10_6

+5VS5

PC144 1U/6.3V_4

(21,31,32,35,37,38,40,41) +VIN
(10,21,23,26,32,34,35,37,39,40,41) +5VS5
(2,4,12,13,38) +1.5VSUS
(12,13,41) +0.75V_DDR_VTT

PR182 10K/F_4

PR180 10K/F_4

Place this FB parts close to IC

PD13

RB501V-40

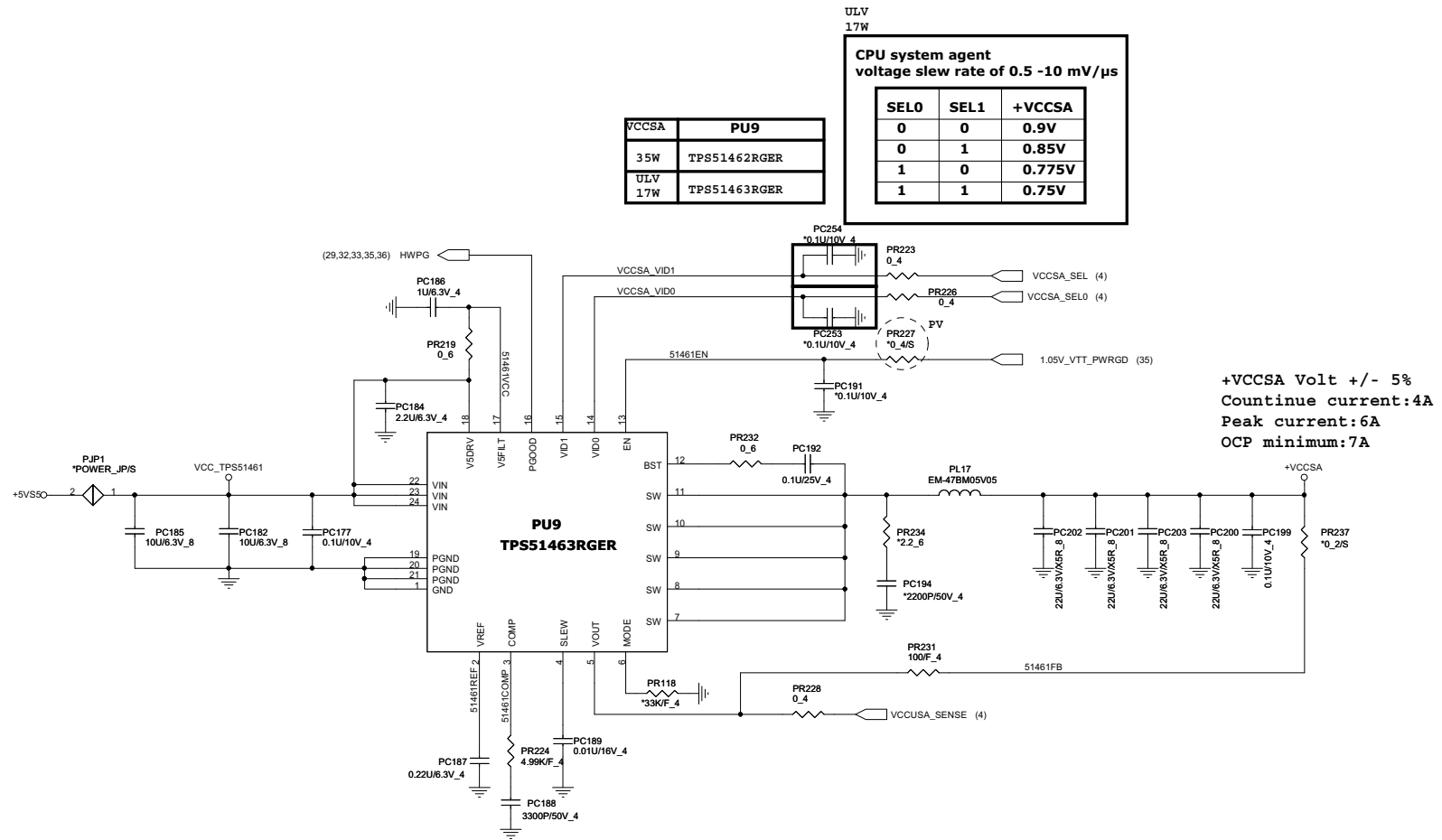
PR181 100K/F_4

PC146 0.1U/10V_4



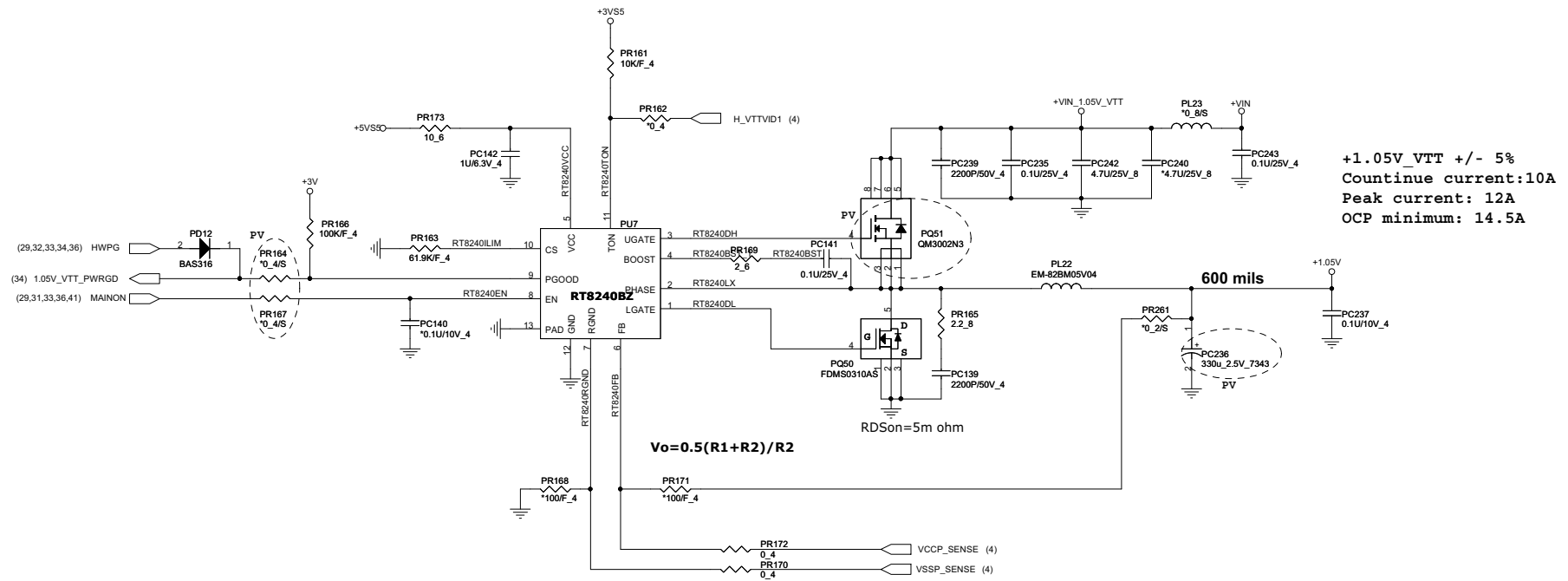
PROJECT : JW6/7
Quanta Computer Inc.

Size Custom	Document Number DDR3 (RT8207)	Rev A
Date: Friday, May 11, 2012	Sheet 33	42



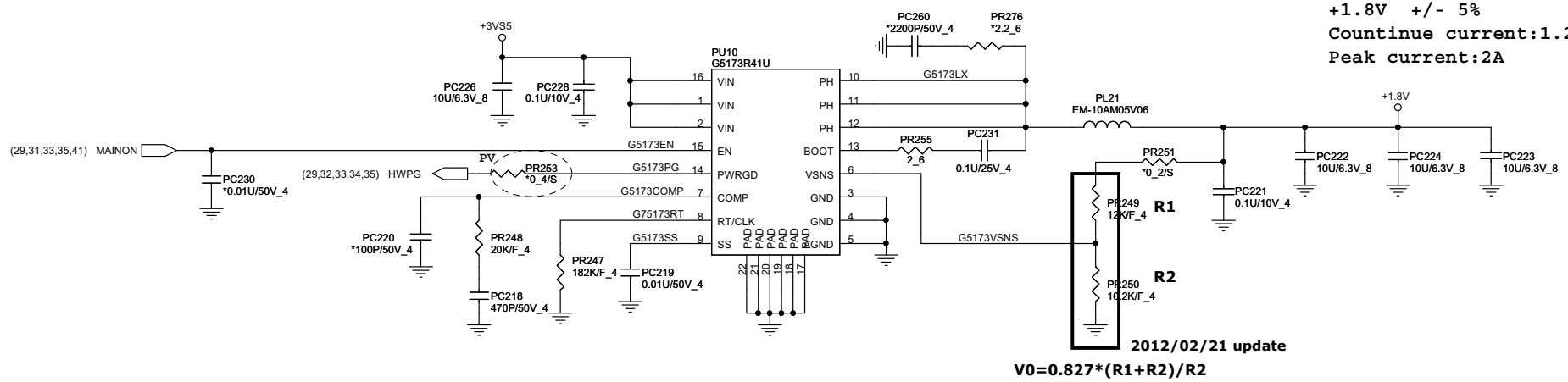
PROJECT : JW6/7
Quanta Computer Inc.

Size Custom	Document Number +VCCSA (TPS51462RGER)	Rev A
Date: Friday, May 11, 2012	Sheet 34 of 42	



PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V (RT8240B)	A
Date: Friday, May 11, 2012	Sheet 35 of 42	



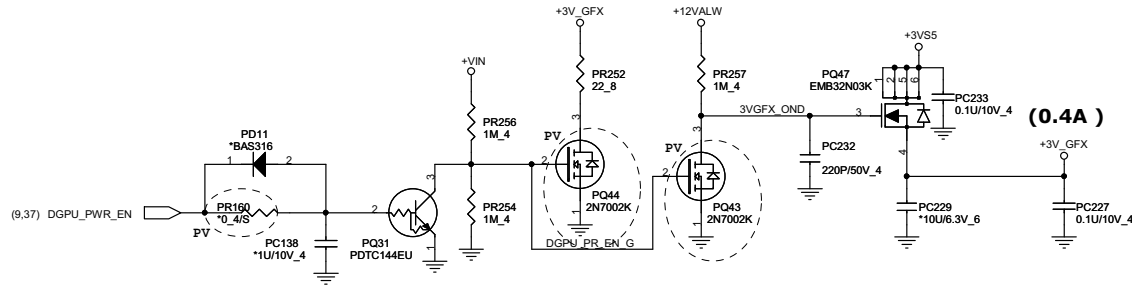
PROJECT : JW6/7
 Quantia Computer Inc.

Size B	Document Number +1.8V (G9661)	Rev A
Date: Friday, May 11, 2012	Sheet 36 of 42	

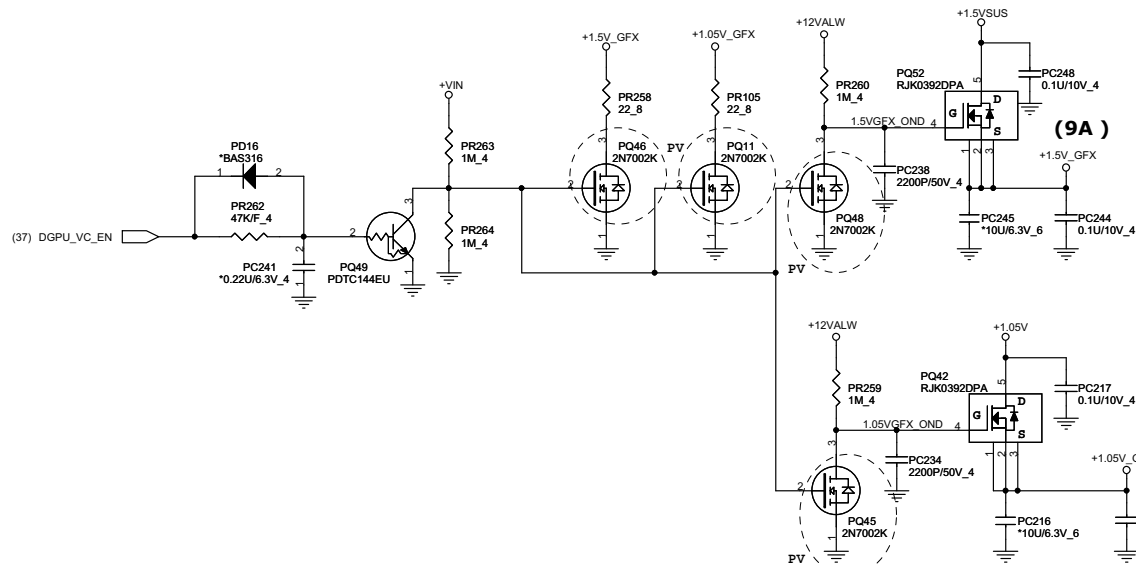
VGA

38

(2,4,12,13,33) +1.5VSUS
(9,10,21,26,27,29,30,32,35,36,41) +3VS5
(14,16,17,18,37) +3V_GFX
(15,18,19,20) +1.5V_GFX
(14,15,16,18) +1.05V_GFX
(41) +12VALW
(2,4,6,7,8,10,26,29,35,39) +1.05V



(0.4A)



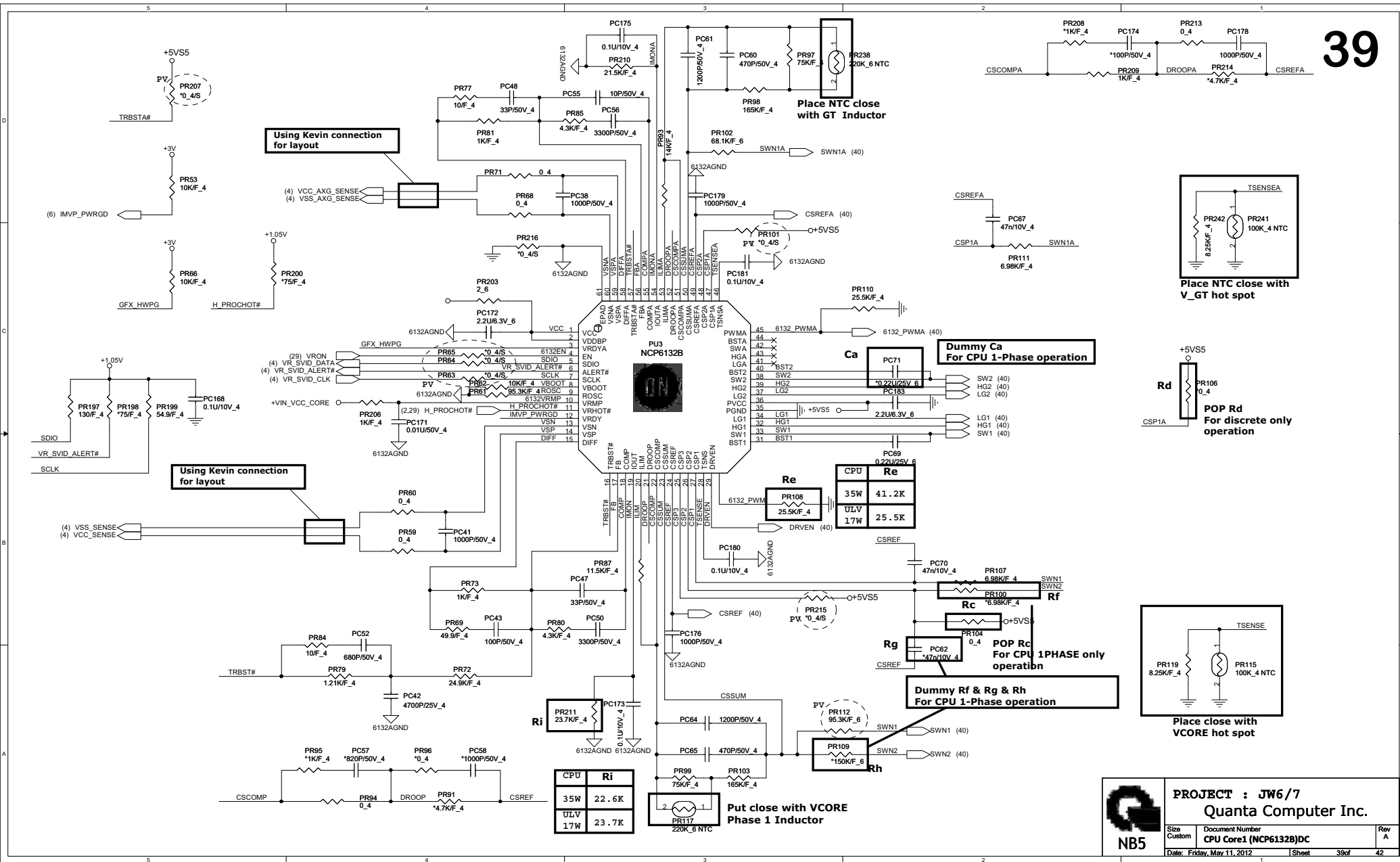
(9A)

+1.05V +/- 3%
Continue current: 2.1A
Peak current: 3A



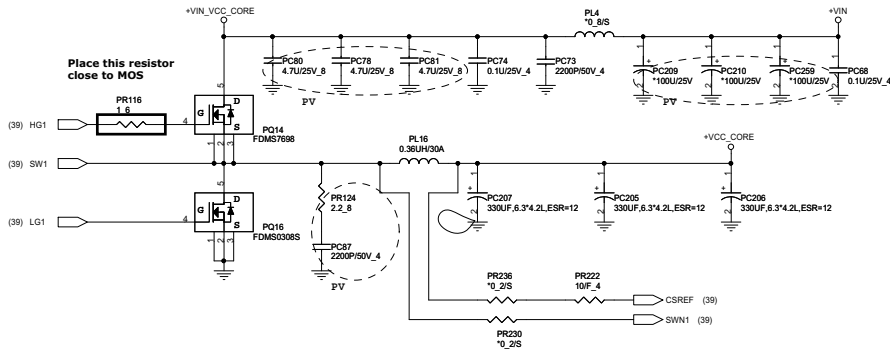
PROJECT : JW6/7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGA POWER	A
Date: Friday, May 11, 2012	Sheet	38 of 42

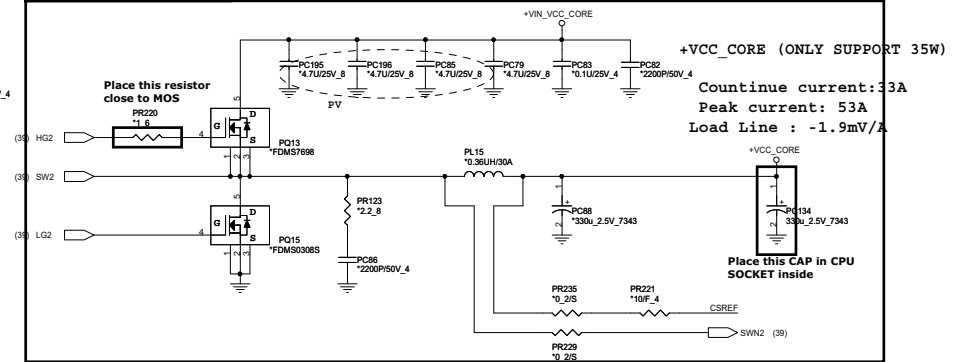


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Size Custom	Document Number CPU Core1 (NCP6132B)DC	Rev A
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Dummy This Schematic
For CPU 1-Phase operation

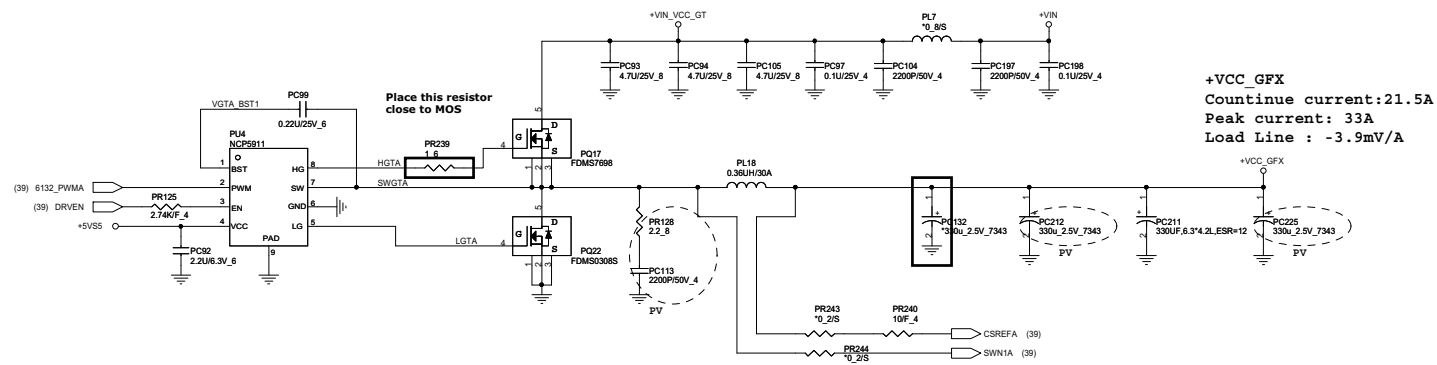


+VCC_CORE (ONLY SUPPORT 35W)

Countinue current:33A
Peak current: 53A
Load Line : -1.9mV/A

+VCC_CORE (ULV 17W)

TDC : 25A
Peak current: 33A
Load Line : -2.9mV/A



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Size C	Document Number CPU Core2 (NCP5911)DC	Rev A
Date: Friday, May 11, 2012	1Sheet	40 of 42

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