1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

"LOHWILL" MLB SCHEMATIC

LAST_MODIFICATION = 2016-10-23 12:22:45 PROTO1A : PRELIMINARY TEST

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
9	00069**41568**	ENGINEERING RELEASED	2016-10-23

PAGE	CSA	CONTENTS	SYNC	DATE
1	1	Table of Contents		
2	2	BOM Configuration	SHART_J44	11/27/2012
3	3	BOM Configuration	J79_JACK	04/07/2016
4	4	PD Parts	LDUNN_J44	01/13/2013
5	5	CPU GFX	J130_DEV_MLB_U	04/29/2015
6	6	CPU MISC/JTAG/CFG/RSVD	J130_DEV_MLB_U	04/28/2015
7	7	CPU LPDDR3 Interface	J52_MLB	05/12/2015
8	8	CPU & PCH Power	J79_JSHAO	03/14/2016
9	9	CPU & PCH Grounds	J79_ALFRED	05/12/2015
10	10	CPU Core Decoupling	J79_JSHAO	08/28/2015
11	11	CPU GT Decoupling	J79_JSHAO	08/28/2015
12	12	PCH Decoupling	J79_JSHAO	03/14/2016
13	13	PCH Audio/LPC/SPI/SMBus	J130_MLB	02/22/2016
14	14	PCH Power Management	J130_MLB	05/04/2016
15	15	PCH PCIE/USB/CLKS	J130_MLB	06/23/2015
16	16	PCH SPI/UART/GPIO	J130_MLB	12/08/2015
17	18	CPU/PCH Merged XDP	J130_MLB	12/08/2015
18	19	Chipset Support 1	J79_GREG	09/09/2015
19	20	Chipset Support 2	J79_GREG	07/05/2016
20	22	LPDDR3 VREF Margining	J52_MLB	05/12/2015
21	23	LPDDR3 DRAM Channel A (00-31)	J52_MLB	05/12/2015
22	24	LPDDR3 DRAM Channel A (32-63)	J52_MLB	05/12/2015
23	25	LPDDR3 DRAM Channel B (00-31)	J52_MLB	05/12/2015
24	26	LPDDR3 DRAM Channel B (32-63)	J52_MLB	05/12/2015
25	27	LPDDR3 DRAM Termination	J52_MLB	05/12/2015
26	28	USB-C HIGH SPEED 1	J79_GREG	07/27/2015
27	29	USB-C HIGH SPEED 2	J79_GREG	09/09/2015
28	30	USB-C Support	J79_GREG	08/08/2016
29	31	USB-C PORT CONTROLLER A	J79_GREG	08/08/2016
30	32	USB-C PORT CONTROLLER B	J79_GREG	02/28/2016
31	33	USB-C CONNECTOR A	J79_GREG	07/05/2016
32	34	USB-C CONNECTOR B	J79_GREG	03/24/2016
33	35	TBT 5V REGULATOR	J79_JSHAO	12/18/2015
34	36	Display Mux	J79_GREG	02/28/2016
35	37	WIFI/BT: MODULE 1	J79_METE	05/17/2016
36	38	WIFI/BT: MODULE 2	J79_METE	03/02/2016
37	39	Camera/DFR 1	J80_MLB_BAFFIN	07/22/2016
38	40	Camera/DFR 2	J79_ANDREW	03/22/2016
39	41	Camera/DFR 3	J79_ANDREW	04/25/2016
40	42	Berkelium - 1	J79_ANDREW	03/14/2016
41	43	Berkelium - 2	J79_ANDREW	02/01/2016
42	44	T208 Support	J79_ANDREW	07/01/2016
43	45	Connectors&ESD	J79_GAREN	11/21/2015
44	46	Empty	J79_DAYU	05/26/2015
45	47	Empty	J79_DAYU	05/26/2015
46	48	Empty	J79_DAYU	05/12/2015
47	49	MESA	J79_ANDREW	01/06/2016
48	50	SMC	J79_JACK	04/11/2016
49	51	SMC Shared Support	J79_JACK	04/14/2016
50	52	SMC Project Support	J79_JACK	04/11/2016
51	53	SMBus Connections	J79_JACK	03/31/2016
52	54	Power Sensors: High Side	J79_JACK	12/07/2015
53	55	Power Sensors: Load Side	J79_JACK	04/03/2016
54	56	Power Sensors: Extended	J79_JACK	01/08/2016
55	57	Power Sensors: Extended 2	J79_JACK	05/10/2016
56	58	Thermal Sensors	J79_JACK	09/24/2015
57	59	Power Sensors:Extended 3	J79_JACK	04/14/2016
58	60	Fans	J79_JACK	08/21/2015
59	61	SPI Debug Connector	J52_MLB	05/12/2015
60	62	HDA Bridge	J79_JCURCIO	03/24/2016
61	63	AUDIO JACK CODEC	J79_JCURCIO	05/13/2016
62	64	Left Speaker Amps & Conn	J79_JCURCIO	11/18/2015
63	65	Right Speaker Amps & Conn	J79_JCURCIO	12/03/2015
64	66	AUDIO JACK CONNECTOR	J79_JCURCIO	12/18/2015
65	69	DC-In & Battery Connectors	J79_JSHAO	12/03/2015
66	70	PBUS Supply & Battery Charger	J79_JSHAO	12/03/2015
67	71	CORE & SA IMVP IC	J79_JSHAO	03/02/2016
68	72	CORE & SA IMVP POWER BLOCK	J79_JSHAO	12/03/2015
69	73	Empty	J79_SILUCHEN	04/02/2015
70	74	GT & GTX IMVP POWER BLOCK	J79_JSHAO	09/25/2015
71	75	Empty	J79_SILUCHEN	03/27/2015
72	76	Power - 5V 3.3V Supply	J79_JSHAO	03/23/2016
73	77	Power - EOPIO EDRAM Supply	J79_JSHAO	04/12/2016
74	78	PMIC-1 & Power Control	J79_JSHAO	09/09/2015
75	79	PMIC-1 1.2V 0.6V VCCIO	J79_JSHAO	12/03/2015
76	80	PMIC-1 1V 1.8V VCCPCH	J79_JSHAO	12/03/2015
77	81	PMIC-1 Aliases & TPs	J79_SILUCHEN	07/17/2015
78	82	Power FETs	J79_JSHAO	03/14/2016
79	84	LCD Backlight Driver	J79_RUENJOU	09/09/2015
80	85	eDP Display Connector	J79_RUENJOU	09/12/2015
81	86	S3X CORE PCIE	J79_RUENJOU	08/20/2015
82	87	S3X POWER	J79_RIO	06/18/2015
83	88	S3X GND	J79_RIO	06/18/2015
84	89	Connector	J79_RUENJOU	09/09/2015
85	90	NAND VR, I2C ROM, TEMP SENSORS	J79_RUENJOU	09/12/2015
86	91	ANI[3:0]	J79_RUENJOU	09/25/2015
87	92	ANI[7:4]	J79_RUENJOU	09/25/2015
88	93	PICCOLO PMIC	J79_RUENJOU	09/24/2015
89	94	SSD NAND VR	J79_JSHAO	12/18/2015
90	95	Empty	J14	10/23/2012
91	96	LIFEBOAT	J79_RUENJOU	09/09/2015
92	110	USB-C HIGH SPEED 1	J79_GREG	07/28/2015
93	111	USB-C HIGH SPEED 2	J79_GREG	08/28/2015
94	112	USB-C Support	J79_GREG	07/05/2016
95	113	USB-C PORT CONTROLLER A	J79_GREG	02/28/2016
96	114	USB-C PORT CONTROLLER B	J79_GREG	02/28/2016
97	115	USB-C CONNECTOR A	J79_GREG	07/05/2016
98	116	USB-C CONNECTOR B	J79_GREG	03/24/2016
99	117	TBT 5V REGULATOR	J79_JSHAO	12/18/2015
100	120	Power Aliases - 1	J79_ALFRED	06/17/2015
101	121	Power Aliases - 2	J79_ALFRED	06/18/2015
102	122	Signal Aliases	SHART_J44	11/19/2012
103	123	LPDDR3 Bit & Byte Swizzle	AHARTMAN_J52	10/29/2013
104	124	ICT FCT 1	YHARTANTO_J44	12/18/2012
105	125	ICT FCT 2	YHARTANTO_J44	12/18/2012
106	127	Desense Capacitors	YHARTANTO_J44	01/09/2013
107	129	Empty	J79_RIO	06/18/2015
108	130	PCB Rule Definitions	YHARTANTO_J44	12/14/2012
109	131	CPU Constraints	YHARTANTO_J44	01/13/2013
110	132	PCH Constraints	YHARTANTO_J44	01/08/2013
111	133	Memory Constraints	YHARTANTO_J44	01/02/2013
112	134	TBT DP HDMI Constraints	J79_JACK	05/19/2015
113	135	PCIe Constraints	J79_JACK	05/19/2015
114	136	USB Constraints	J79_JACK	05/21/2015
115	137	SMC Constraints	YHARTANTO_J44	01/02/2013
116	138	Camera Constraints	YHARTANTO_J44	01/09/2013
117	139	Sensors & Audio Constraints	YHARTANTO_J44	01/04/2013
118	140	References	J79_RUENJOU_CONSTRAINTS	09/11/2015
119	145	Alternates BOM Table	J80_MLB	12/12/2015

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00777	1	SCHEM,MLB,Lohwill	SCH	CRITICAL	
820-00923	1	PCBF,MLB,Lohwill	PCB	CRITICAL	xTN20JE19

DRAWING TITLE: SCHEM,MLB,Lohwill

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D

REVISION: 9.0.0

BRANCH: dvt-fab09-0

PAGE: 1 OF 145

SHEET: 1 OF 119

BOM Groups

BOM GROUP	BOM OPTIONS
Lohwill_COMMON	ALTERNATE,COMMON,Lohwill_COMMON1,Lohwill_COMMON2,Lohwill_COMMON3,Lohwill_PROGPARTS
Lohwill_COMMON1	SE:PROD,BOARD_ID:8,T208_PROG:REV5,TBTTHRM_SNS,S3XCLK:INT
Lohwill_COMMON2	EDP_ENABLE,XDP:YES,PCH_CLK:GRNCLK,TBT_DBG,SAMCONN,SKIP_5V3V3:AUDIBLE,SOC_BOOT:SPI
Lohwill_COMMON3	CPUTHRM:ALRT,TBTTHRM:ALRT,LOADRC:NO,CUMULUS_IPD,S3_STATE:YES,VCCPLLOC:S3
Lohwill_PROGPARTS	BOOTROM_PROG,SMC_PROG,AR_LT_PROG,AR_RT_PROG,WIFI_PROG,BTROM_PROG
Lohwill_DEVEL:ENG	ALTERNATE,DBGLED,USBC_DBG,XDP_CONN:YES,WIFI_DBG,S3X_DBG,DEBUG_BUTTON,LOADISNS
Lohwill_DEVEL:DVT	ALTERNATE,USBC_DBG,XDP_CONN:YES,WIFI_DBG
Lohwill_DEVEL:PVT	ALTERNATE

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00717	1	CPU,KBLU,SR362,PRQ,3.1,28W,B1356	U0500	CRITICAL	CPU_KBL24:3.1G
337S00718	1	CPU,KBLU,SR360,PRQ,3.3,28W,B1356	U0500	CRITICAL	CPU_KBL24:3.3G
337S00719	1	CPU,KBLU,SR367,PRQ,3.5,28W,B1356	U0500	CRITICAL	CPU_KBL24:3.5G
998-04195	1	INTERPOSER,VTT ADAPTER,KBL-U,BGA1356	U0500	CRITICAL	CPU_SOCKET
338S00254	2	IC,TBT,ALPINE RIDGE,QSTY,PRQ,C1,CSP337	U2800,UB000	CRITICAL	
353S00961	4	IC,CD3215,ACE,C00,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	
338S00276	1	IC,CNTLR,S3X,B1,FCBGA900	U8600	CRITICAL	
333S00055	1	IC,LPDDR3-2133,4GBIT,25NM,A,276B	POP8600	CRITICAL	POP_4GBIT
333S00056	1	IC,LPDDR3-2133,8GBIT,25NM,A,276B	POP8600	CRITICAL	POP_8GBIT
343S00147	1	IC,SLG4AP41172,PAK3,STQFN20	U3620	CRITICAL	
338S00221	1	IC,PMU,SN650839,7X7MM,BGA168	U7800	CRITICAL	
353S01016	1	IC,ISL9239HIZ,PMU,TUBA,WCSP40,2.1X3.3MM	U7000	CRITICAL	
338S00227	1	IC,PMU,PICCOLO,D2231A0,OTP-AK,WLCSP96	U9300	CRITICAL	

Programmables (All Builds)

EFI ROM

341S00698	1	IC,EFI ROM (V0193) DVT,X362	U6100	CRITICAL	BOOTROM_PROG

SMC ROM

341S00700	1	IC,SMC-B1,EXT (V2.37F6) PVT,X362	U5000	CRITICAL	SMC_PROG

TBT ROMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00717	1	T29,AR1 (VTBD) PVT,X362	U2890	CRITICAL	AR_LT_PROG
341S00718	1	T29,AR2 (VTBD) PVT,X362	UB090	CRITICAL	AR_RT_PROG

WIFI/BT ROM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S00715	1	IC,BT ROM (V32) PVT,X362/X363	U3750	CRITICAL	BTROM_PROG
341S00716	1	WIFI ROM (P108) PVT,WW1,X362/X363	U3710	CRITICAL	WIFI_PROG

Variable BOM Groups
Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00055	1	COMMON PARTS,MLB,X362	BASE	CRITICAL	BASE_BOM
985-00070	1	DEV,MLB,X362	DEVEL	CRITICAL	DEVEL_BOM

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00069	4	IC,SDRAM,LPDDR3-2133,16GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	8G_MICRON_2133
333S00070	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_MICRON_2133
333S00068	4	IC,SDRAM,LPDDR3-2133,16GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	8G_SAMSUNG_2133
333S00050	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_SAMSUNG_2133

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_8G_MICRON_2133	8G_MICRON_2133,RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L
RAM_16G_MICRON_2133	16G_MICRON_2133,RAMCFG4_L,RAMCFG3_L,RAMCFG1_L
RAM_8G_SAMSUNG_2133	8G_SAMSUNG_2133,RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG0_L
RAM_16G_SAMSUNG_2133	16G_SAMSUNG_2133,RAMCFG4_L,RAMCFG3_L,RAMCFG0_L

NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00124	4	NAND,1ZNM,64GB,TOGG,HPN,128G,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_SDISK_256GB
335S00125	4	NAND,1ZNM,128GB,TOGG,HPN,128G,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_SDISK_512GB
335S00126	4	NAND,1ZNM,256GB,TOGG,HPN,128G,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_SDISK_1TB
335S00261	4	NAND,TGDDR2,128GX4,15NM,HP,USHD,T2,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_TSHBA_256GB
335S00262	4	NAND,TGDDR2,128GX8,15NM,HP,USHD,T2,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_TSHBA_512GB
335S00263	4	NAND,TGDDR2,128GX16,15NM,HP,UHD,T2,LGA60	U9100,U9120,U9200,U9220	CRITICAL	NAND_TSHBA_1TB

NAND Straps

BOM GROUP	BOM OPTIONS
SAND_256G	ALTERNATE,NAND_SDISK_256GB,POP_4GBIT,CAPACITY1,CAPACITY0
SAND_512G	ALTERNATE,NAND_SDISK_512GB,POP_4GBIT,CAPACITY2
SAND_1T	ALTERNATE,NAND_SDISK_1TB,POP_8GBIT,CAPACITY2,CAPACITY0
TOSH_256G	ALTERNATE,NAND_TSHBA_256GB,POP_4GBIT,CAPACITY1,CAPACITY0
TOSH_512G	ALTERNATE,NAND_TSHBA_512GB,POP_4GBIT,CAPACITY2
TOSH_1T	ALTERNATE,NAND_TSHBA_1TB,POP_8GBIT,CAPACITY2,CAPACITY0

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00266	08	CPU
337S00267	08	CPU
337S00268	08	CPU
333S00050	07	MEMORY
333S00068	07	MEMORY
333S00069	07	MEMORY
333S00070	07	MEMORY
335S00124	02	NAND
335S00125	02	NAND
335S00126	02	NAND
335S00261	02	NAND
335S00262	02	NAND
335S00263	02	NAND
333S00025	02	S3X DRAM
333S00026	02	S3X DRAM
333S00055	02	S3X DRAM
333S00056	02	S3X DRAM
333S00107	02	S3X DRAM
333S00108	02	S3X DRAM
998-06736	02	S3X CONTROLLER

PART#	STRATEGIC VALUE	COMMENT
338S00227	02	PICCOLO
343S00135	10	T208
343S00136	10	T208
343S00137	10	T208
343S00138	10	T208
338S00193	09	BERKELIUM
353S3978	02	MOJAVE
338S00147	02	SECURE ELEMENT
338S00254	08	ALPINE RIDGE
353S00961	09	ACE
338S00142	09	CLIFDEN
353S00685	07	AUDIO AMP
353S4316	08	BAYSIDE
338S00221	08	BANJO
353S01016	09	TUBA
339S00056	05	ICEBOCK
343S00147	08	PAK
359S00006	08	GREEN CLOCK
353S00795	09	DEBUG MUX

CPU DRAM CFG Chart

DIE REV	CFG 4
A	0
B	1

SPEED	CFG 3
2133	0
1866	1

CAPACITY	CFG 2
8GB	0
16GB	1

VENDOR	CFG 1	CFG 0
HYNIX	0	0
MICRON	0	1
SAMSUNG	1	0
N/A	1	1

SYNC_MASTER=SHART_344 SYNC_DATE=11/27/2013

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 2 OF 145

SHEET 2 OF 119

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00055	COMMON PARTS,MLB,X362	X362_COMMON
985-00070	DEV,MLB,X362	X362_DEVEL:DVT
639-01870	MLB,2.9G,SAM-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_256G
639-01871	MLB,2.9G,SAM-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_256G
639-01872	MLB,2.9G,MIC-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_256G
639-01873	MLB,2.9G,MIC-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_256G
639-01984	MLB,2.9G,SAM-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_512G
639-01985	MLB,2.9G,SAM-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_512G
639-01986	MLB,2.9G,MIC-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_512G
639-01987	MLB,2.9G,MIC-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_512G
639-02517	MLB,2.9G,SAM-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,SAND_1T
639-02518	MLB,2.9G,SAM-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,SAND_1T
639-02519	MLB,2.9G,MIC-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,SAND_1T
639-02520	MLB,2.9G,MIC-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,SAND_1T
639-01874	MLB,3.1G,SAM-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_256G
639-01875	MLB,3.1G,SAM-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_256G
639-01876	MLB,3.1G,MIC-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_256G
639-01877	MLB,3.1G,MIC-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_256G
639-01883	MLB,3.1G,SAM-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_512G
639-01884	MLB,3.1G,SAM-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_512G
639-01885	MLB,3.1G,MIC-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_512G
639-01886	MLB,3.1G,MIC-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_512G
639-01887	MLB,3.1G,SAM-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,SAND_1T
639-01888	MLB,3.1G,SAM-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,SAND_1T
639-01889	MLB,3.1G,MIC-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,SAND_1T
639-01890	MLB,3.1G,MIC-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,SAND_1T
639-02221	MLB,3.3G,SAM-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_256G
639-02222	MLB,3.3G,SAM-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_256G
639-02223	MLB,3.3G,MIC-8G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_256G
639-02224	MLB,3.3G,MIC-16G,SAND-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_256G
639-01891	MLB,3.3G,SAM-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_512G
639-01892	MLB,3.3G,SAM-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_512G
639-01893	MLB,3.3G,MIC-8G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_512G
639-01894	MLB,3.3G,MIC-16G,SAND-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_512G
639-01895	MLB,3.3G,SAM-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,SAND_1T
639-01896	MLB,3.3G,SAM-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,SAND_1T
639-01897	MLB,3.3G,MIC-8G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,SAND_1T
639-01898	MLB,3.3G,MIC-16G,SAND-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,SAND_1T

BOM NUMBER	BOM NAME	BOM OPTIONS
639-01988	MLB,NO CPU,X362	BASE_BOM,DEVEL_BOM,RAM_16G_SAMSUNG_2133,SAND_512G
639-01989	MLB,CPU SOCKET,X362	BASE_BOM,DEVEL_BOM,CPU_SOCKET,RAM_16G_SAMSUNG_2133,SAND_512G
639-02521	MLB,2.9G,SAM-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_256G
639-02522	MLB,2.9G,SAM-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_256G
639-02523	MLB,2.9G,MIC-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_256G
639-02524	MLB,2.9G,MIC-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_256G
639-02525	MLB,2.9G,SAM-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_512G
639-02526	MLB,2.9G,SAM-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_512G
639-02527	MLB,2.9G,MIC-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_512G
639-02528	MLB,2.9G,MIC-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_512G
639-02529	MLB,2.9G,SAM-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_SAMSUNG_2133,TOSH_1T
639-02530	MLB,2.9G,SAM-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_SAMSUNG_2133,TOSH_1T
639-02531	MLB,2.9G,MIC-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_8G_MICRON_2133,TOSH_1T
639-02532	MLB,2.9G,MIC-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:2.9G,RAM_16G_MICRON_2133,TOSH_1T
639-02533	MLB,3.1G,SAM-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_256G
639-02534	MLB,3.1G,SAM-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_256G
639-02535	MLB,3.1G,MIC-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_256G
639-02536	MLB,3.1G,MIC-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_256G
639-02537	MLB,3.1G,SAM-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_512G
639-02538	MLB,3.1G,SAM-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_512G
639-02539	MLB,3.1G,MIC-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_512G
639-02540	MLB,3.1G,MIC-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_512G
639-02541	MLB,3.1G,SAM-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_SAMSUNG_2133,TOSH_1T
639-02542	MLB,3.1G,SAM-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_SAMSUNG_2133,TOSH_1T
639-02543	MLB,3.1G,MIC-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_8G_MICRON_2133,TOSH_1T
639-02544	MLB,3.1G,MIC-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.1G,RAM_16G_MICRON_2133,TOSH_1T
639-02545	MLB,3.3G,SAM-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_256G
639-02546	MLB,3.3G,SAM-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_256G
639-02547	MLB,3.3G,MIC-8G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_256G
639-02548	MLB,3.3G,MIC-16G,TOSH-256G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_256G
639-02549	MLB,3.3G,SAM-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_512G
639-02550	MLB,3.3G,SAM-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_512G
639-02551	MLB,3.3G,MIC-8G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_512G
639-02552	MLB,3.3G,MIC-16G,TOSH-512G,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_512G
639-02553	MLB,3.3G,SAM-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_SAMSUNG_2133,TOSH_1T
639-02554	MLB,3.3G,SAM-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_SAMSUNG_2133,TOSH_1T
639-02555	MLB,3.3G,MIC-8G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_8G_MICRON_2133,TOSH_1T
639-02556	MLB,3.3G,MIC-16G,TOSH-1T,X362	BASE_BOM,DEVEL_BOM,CPU_SKL23:3.3G,RAM_16G_MICRON_2133,TOSH_1T

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
152S00367	152S00266		ALL		Text note to be updated
152S00368	152S00269		ALL		Text note to be updated
152S00370	152S00270		ALL		Text note to be updated
353S4068	353S4070		ALL		Text note to be updated
353S00772	353S4070		ALL		Text note to be updated
138S00086	138S0884		ALL		Text note to be updated
107S0248	107S0250		ALL		TFT alt to Cyntec
152S00434	152S1829		ALL		Text note to be updated
371S00019	371S0463		ALL		Rohm alt to Rohm
353S00107	353S3239	ANY	ALL		Onsemi alt to Intersil
353S00231	353S3987		ALL		NXP alt to TI
333S00025	333S00055	POP_4GBIT	ALL		MICRON SSD POP ALT for HYNIX
333S00026	333S00056	POP_8GBIT	ALL		MICRON SSD POP ALT for HYNIX
333S00107	333S00055	POP_4GBIT	ALL		HYNIX SSD POP REPLACEMENT for HYNIX
333S00108	333S00056	POP_8GBIT	ALL		HYNIX SSD POP REPLACEMENT for HYNIX

138S0701	138S0689		ALL		Text note to be updated
138S00012	138S0771		ALL		Text note to be updated
138S0772	138S00013		ALL		Text note to be updated
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152S2034	152S00190		ALL		Text note to be updated
197S0613	197S0612		ALL		Text note to be updated
311S00121	311S0398		ALL		Text note to be updated
371S0713	371S0558		ALL		Text note to be updated
371S00074	371S0602		ALL		Text note to be updated

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PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 3 OF 145

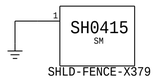
SHEET 3 OF 119

BOARD MECHANICALS

Shield Cans - BOTTOM SIDE

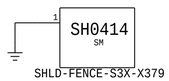
ALPINE RIDGE - LIO (U2800) - 806-06077

LPDDR3 (U2300 ~ U2600) - 806-06167



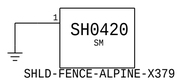
NAND - BOTTOM SOUTH (U9120) - 806-05945

S3X (U8600) - 806-06023



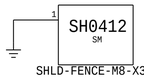
NAND - BOTTOM NORTH (U9200) - 806-06265

ALPINE RIDGE - RIO (UB000) - 806-06077



Shield Cans - TOP SIDE

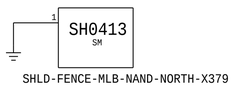
T208 (U3900) - 806-06264



DIPLEXERS - 806-06266

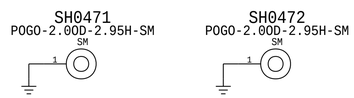
NAND - TOP SOUTH (U9100) - 806-06262

NAND - TOP NORTH (9220) - 806-06258

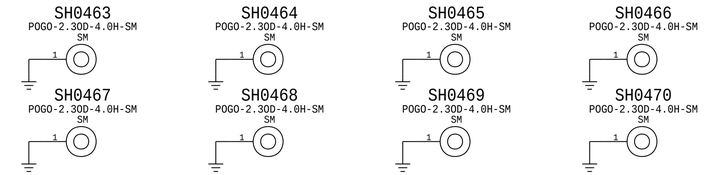


POGO PINS

LIO and RIO -2X (870-5071)

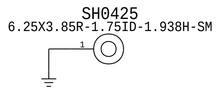


AROUND THE FAN AND CENTER - 8X (870-01518)

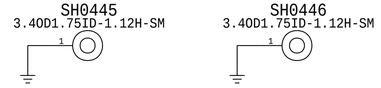


Cowling Bosses - BOTTOM SIDE

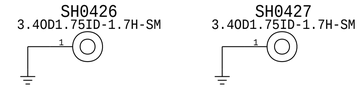
DFR TOUCH CONN (J4402) - 860-00414



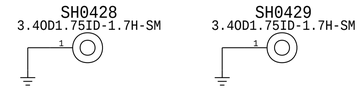
USB-C CONN - LIO (J3300) - 860-00392



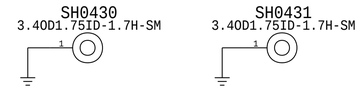
DFR DISPLAY CONN (J4401) - 860-00412



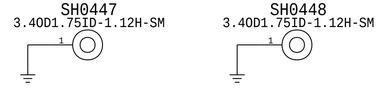
IPD CONN (J4501) - 860-00412



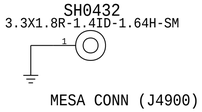
KBD CONN (J4500) - 860-00412



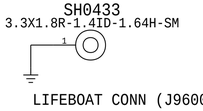
USB-C CONN - RIO (JB500) - 860-00392



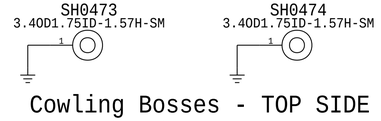
AUDIO JACK CONN (J6600) - 860-00399



MESA CONN (J4900) - 860-00399

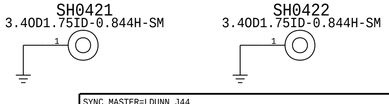


LIFEBOAT CONN (J9600) - 860-00413

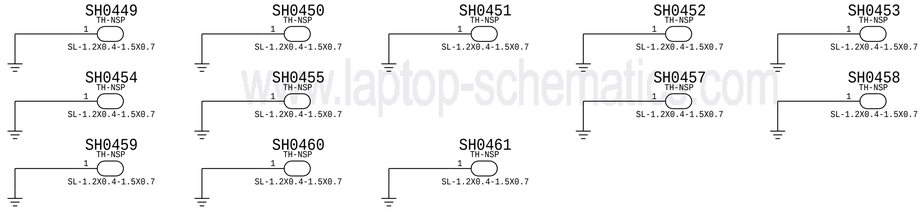


Cowling Bosses - TOP SIDE

eDP CONN (J8500) - 860-00415

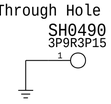


Shield CAN Alignment Slots 14X - 998-04440 (1.2mm X 0.4mm)

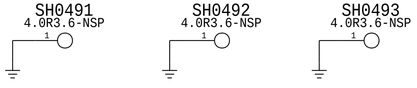


Thermal Stage Mounting Holes

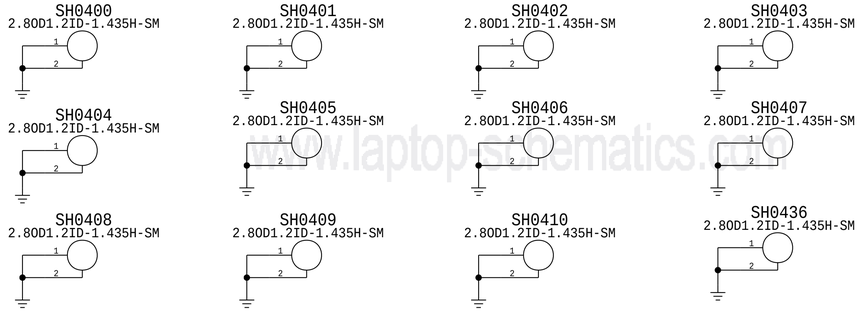
Plated Through Hole - 3.15mm - APN 998-0845



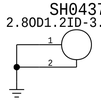
Plated Through Hole - 3.6mm - APN 998-03850



TOP Rubber Mount Standoffs - 12X - (860-00430)



Bottom Rubber Mount Standoffs - 1X - (860-00476)



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PD Parts

Apple Inc.

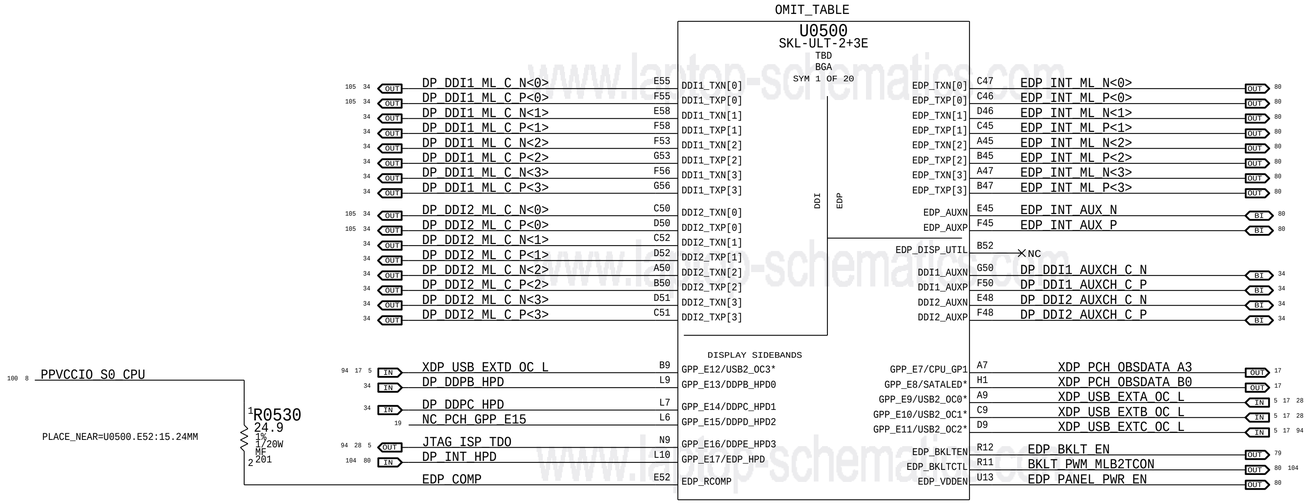
DRAWING NUMBER 051-00777 SIZE D

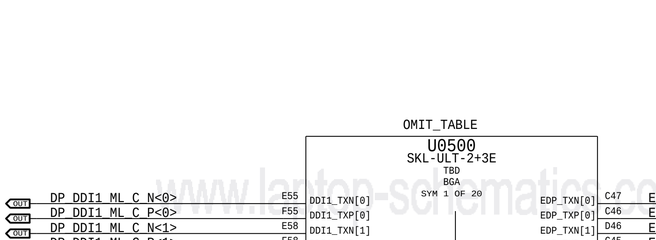
REVISION 9.0.0

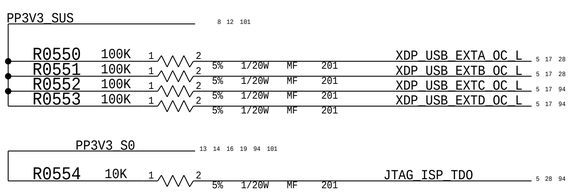
BRANCH dvt-fab09-0

PAGE 4 OF 145

SHEET 4 OF 119







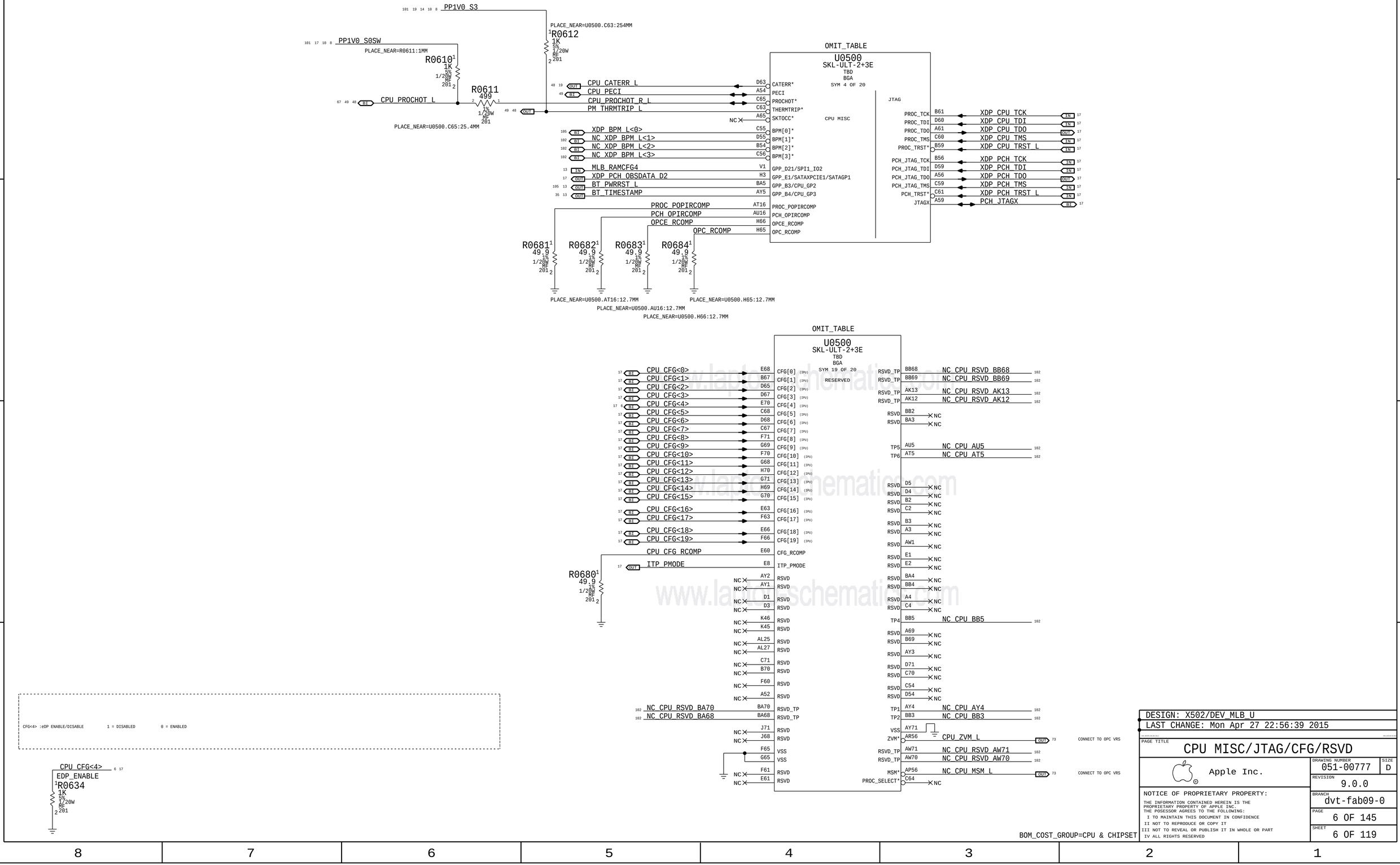
BOM_COST_GROUP=CPU & CHIPSET

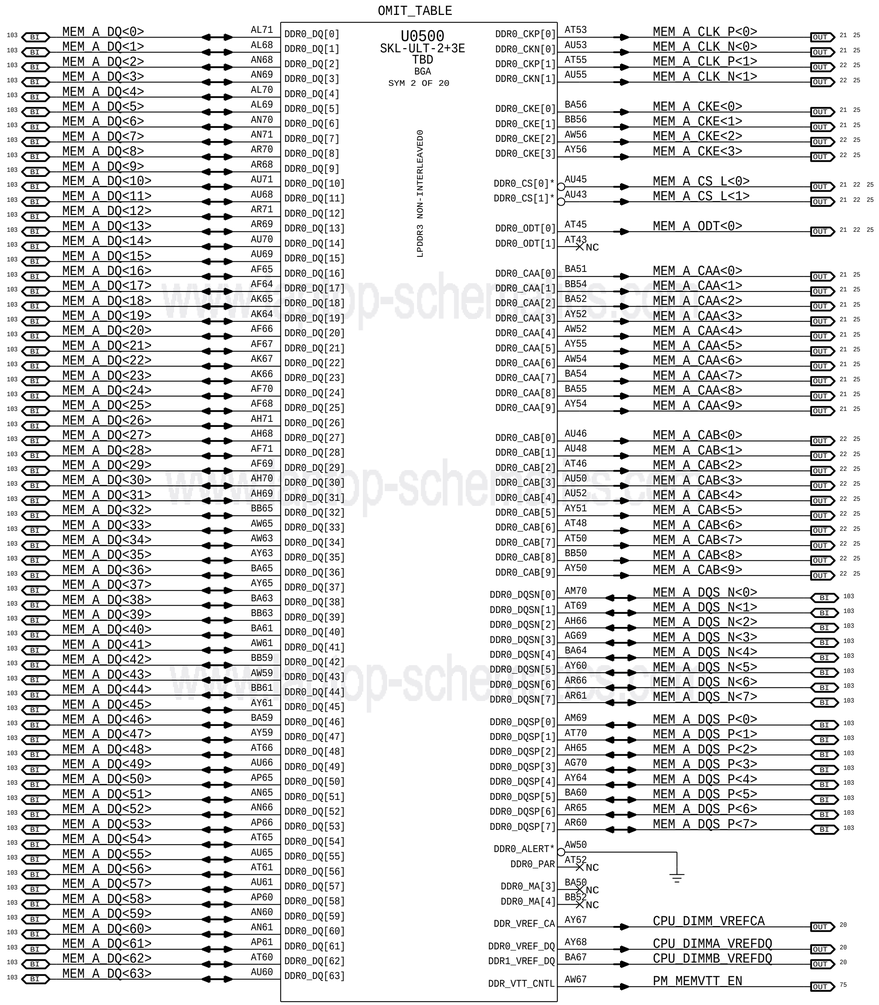
DESIGN: X502/DEV_MLB_U
LAST CHANGE: Tue Apr 28 20:32:21 2015

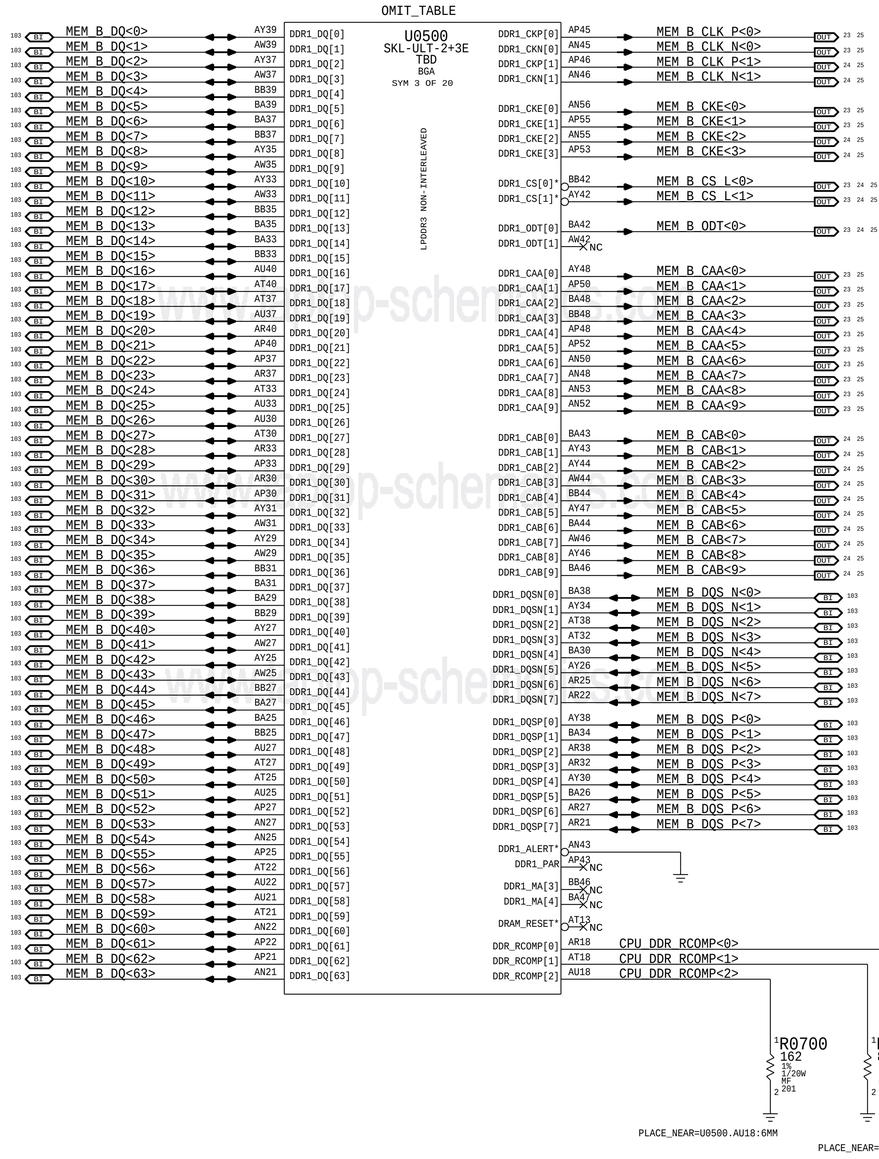
PAGE TITLE
CPU GFX

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 5 OF 145
SHEET 5 OF 119







BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE

CPU LPDDR3 Interface

Apple Inc.

DRAWING NUMBER	SIZE
051-00777	D
REVISION	
9.0.0	
BRANCH	
dvt-fab09-0	
PAGE	
7 OF 145	
SHEET	
7 OF 119	

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 14 OF 20
CPU POWER 3

100 PP1V2_S3_CPUDDR	AU23	VDDQ	VCCIO	AK28	PPVCCIO_S0_CPU 5 8 100
	AU28	VDDQ	VCCIO	AK30	
	AU35	VDDQ	VCCIO	AL30	
	AU42	VDDQ	VCCIO	AL42	
	BB23	VDDQ	VCCIO	AM28	
	BB32	VDDQ	VCCIO	AM30	
	BB41	VDDQ	VCCIO	AM42	
	BB47	VDDQ	VCCSA	AK23	PPVCCSA_S0_CPU 8 55 100
	BB51	VDDQ	VCCSA	AK25	
100 PP1V2_S3_CPUDDR	AM40	VDDQC	VCCSA	G23	
101 19 14 10 8 6 PP1V0_S3	A18	VCCST	VCCSA	G25	
101 17 10 8 6 PP1V0_S0SW	A22	VCCSTG	VCCSA	G27	
100 10 PP1V2_S0SW	AL23	VCCPLL_OC	VCCSA	G28	
101 10 PP1V0_S3	K20	VCCPLL	VCCSA	J22	
	K21	VCCPLL	VCCSA	J23	
			VCCSA	J27	
			VCCIO_SENSE	AM23	CPU_VCCIOSENSE_P OUT 8 75
			VSSIO_SENSE	AM22	CPU_VCCIOSENSE_N OUT 8 75
			VSSSA_SENSE	H21	CPU_VCCSASENSE_N OUT 8 67
			VCCSA_SENSE	H20	CPU_VCCSASENSE_P OUT 8 67
			VCCSA	K23	
			VCCSA	K25	
			VCCSA	K27	
			VCCSA	K28	
			VCCSA	K30	

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 15 OF 20
CPU POWER 4

101 12 8 PP1V0_SUS	AB19	VCCPRIM_1P0	VCCPGPPA	AK15	PP3V3_SUS 13 14 15 16 101
	AB20	VCCPRIM_1P0	VCCPGPPB	AG15	PP3V3_SUS 12 101
	P18	VCCPRIM_1P0	VCCPGPPC	Y16	PP3V3_SUS 12 101
100 55 12 PPVCCPRIMCORE_SUS_PCH	AF18	VCCPRIM_CORE	VCCPGPPD	Y15	PP3V3_SUS 101
	AF19	VCCPRIM_CORE	VCCPGPPE	T16	PP3V3_SUS 12 101
	V20	VCCPRIM_CORE	VCCPGPPF	AF16	PP1V8_SUS 14 19 100
	V21	VCCPRIM_CORE	VCCPGPPG	AD15	PP3V3_SUS 101
19 12 PP1V_S5_PCH_DCPDSW	AL1	DCPDSW_1P0	VCCPRIM_3P3	V19	PP3V3_SUS 5 8 12 101
101 12 PP1V0_SUS	K17	VCCMPHYAON_1P0	VCCPRIM_1P0	T1	PP1V0_SUS 8 12 101
	L1	VCCMPHYAON_1P0	VCCATS_1P8	AA1	PP1V8_SUS 12 100
101 12 PP1V0_SUSSW	N15	VCCMPHYGT_1P0	VCCRTCPRIM_3P3	AK17	PP3V3_SUS 12 101
	N16	VCCMPHYGT_1P0	VCCRTC	AK19	PP3V0_G3H 12 14 15 100
	N17	VCCMPHYGT_1P0	VCCRTC	BB14	
	P15	VCCMPHYGT_1P0	DCPRTC	BB10	PPDCPRTC_PCH 12 19
	P16	VCCMPHYGT_1P0	VCCCLK1	A14	PP1V0_SUS 101
12 PP1V_SUSSW_PCH_VCCAMPHYPLL_F	K15	VCCAMPHYPLL_1P0	VCCCLK2	K19	PP1V_SUS_PCH_VCCCLK2_F 12
	L15	VCCAMPHYPLL_1P0	VCCCLK3	L21	PP1V0_SUS 101
12 PP1V_SUS_PCH_VCCAPLL_F	V15	VCCAPLL_1P0	VCCCLK4	N20	PP1V_SUS_PCH_VCCCLK4_F 12
101 12 8 PP1V0_SUS	AB17	VCCPRIM_1P0	VCCCLK5	L19	PP1V_SUS_PCH_VCCCLK5_F 12
	Y18	VCCPRIM_1P0	VCCCLK6	A10	PP1V0_SUS 101
101 14 PP3V3_S5	AD17	VCCDSW_3P3	GPP_B0/CORE_VID0	AN11	NC_VCCPRIM_CORE_VID0 OUT 19
	AD18	VCCDSW_3P3	GPP_B1/CORE_VID1	AN13	NC_VCCPRIM_CORE_VID1 OUT 19
	AJ17	VCCDSW_3P3			
12 PP1V8_S0_PCH_VCCHDA_F	AJ19	VCCHDA			
101 13 PP3V3_SUS	AJ16	VCCSPI			
101 12 PP1V0_SUSSW	AF20	VCCSRAM_1P0			
	AF21	VCCSRAM_1P0			
	T19	VCCSRAM_1P0			
	T20	VCCSRAM_1P0			
101 12 8 5 PP3V3_SUS	AJ21	VCCPRIM_3P3			
78 12 PP1V0_SUSFUSE	AK20	VCCPRIM_1P0			
101 12 PP1V0_SUSSW	N18	VCCAPLLEBB_1P0			

100 8 5 PPVCCIO_S0_CPU	R0801	100 5% 1/20W MF 201	CPU_VCCIOSENSE_P 8 75
100 55 8 PPVCCSA_S0_CPU	R0804	100 5% 1/20W MF 201	CPU_VCCSASENSE_P 8 67
100 54 8 PPVCCGT_S0_CPU	R0811	100 5% 1/20W MF 201	CPU_VCCGTSENSE_P 8 67
100 8 PPVCCGT_S0_CPU	R0813	100 5% 1/20W MF 201	CPU_VCCGTXSENSE_P 8
100 8 PPVCCEDRAM_S0_CPU	R0821	100 5% 1/20W MF 201	CPU_VCCOPCSENSE_P 8
100 8 PPVCCEDRAM_S0_CPU	R0823	100 5% 1/20W MF 201	CPU_VCCEOPIOSENSE_P 8
104 100 54 8 PPVCC_S0_CPU	R0825	100 5% 1/20W MF 201	CPU_VCCSENSE_P 8 67

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PLACE_NEAR=U0500.H20:50.8MM
PLACE_NEAR=U0500.J70:50.8MM
PLACE_NEAR=U0500.AK62:50.8MM
PLACE_NEAR=U0500.AC63:50.8MM
PLACE_NEAR=U0500.AL63:50.8MM
PLACE_NEAR=U0500.E32:50.8MM

	R0802	100 5% 1/20W MF 201	CPU_VCCIOSENSE_N 8 75
	R0803	100 5% 1/20W MF 201	CPU_VCCSASENSE_N 8 67
	R0812	100 5% 1/20W MF 201	CPU_VCCGTSENSE_N 8 67
	R0814	100 5% 1/20W MF 201	CPU_VCCGTXSENSE_N 8
	R0822	100 5% 1/20W MF 201	CPU_VCCOPCSENSE_N 8
	R0824	100 5% 1/20W MF 201	CPU_VCCEOPIOSENSE_N 8
	R0826	100 5% 1/20W MF 201	CPU_VCCSENSE_N 8 67

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PLACE_NEAR=U0500.AJ62:50.8MM
PLACE_NEAR=U0500.E33:50.8MM

100 54 8 PPVCCGT_S0_CPU

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 13 OF 20
CPU POWER 2

A48	VCCGT		N70	VCCGT	
A53	VCCGT		N71	VCCGT	
A58	VCCGT		R63	VCCGT	
A62	VCCGT		R64	VCCGT	
A66	VCCGT		R65	VCCGT	
AA63	VCCGT		R66	VCCGT	
AA64	VCCGT		R67	VCCGT	
AA66	VCCGT		R68	VCCGT	
AA67	VCCGT		R69	VCCGT	
AA69	VCCGT		R70	VCCGT	
AA70	VCCGT		R71	VCCGT	
AA71	VCCGT		T62	VCCGT	
AC64	VCCGT		U65	VCCGT	
AC65	VCCGT		U68	VCCGT	
AC66	VCCGT		U71	VCCGT	
AC67	VCCGT		W63	VCCGT	
AC68	VCCGT		W64	VCCGT	
AC69	VCCGT		W65	VCCGT	
AC70	VCCGT		W66	VCCGT	
AC71	VCCGT		W67	VCCGT	
J43	VCCGT		W68	VCCGT	
J45	VCCGT		W69	VCCGT	
J46	VCCGT		W70	VCCGT	
J48	VCCGT		W71	VCCGT	
J50	VCCGT		Y62	VCCGT	
J52	VCCGT				
J53	VCCGT		AK42	VCCGTX	PPVCCGT_S0_CPU 8 100
J55	VCCGT		AK43	VCCGTX	
J56	VCCGT		AK45	VCCGTX	
J58	VCCGT		AK46	VCCGTX	
J60	VCCGT		AK48	VCCGTX	
K48	VCCGT		AK50	VCCGTX	
K50	VCCGT		AK52	VCCGTX	
K52	VCCGT		AK53	VCCGTX	
K53	VCCGT		AK55	VCCGTX	
K55	VCCGT		AK56	VCCGTX	
K56	VCCGT		AK58	VCCGTX	
K58	VCCGT		AK60	VCCGTX	
K60	VCCGT		AK70	VCCGTX	
L62	VCCGT		AL43	VCCGTX	
L63	VCCGT		AL46	VCCGTX	
L64	VCCGT		AL50	VCCGTX	
L65	VCCGT		AL53	VCCGTX	
L66	VCCGT		AL56	VCCGTX	
L67	VCCGT		AL60	VCCGTX	
L68	VCCGT		AM48	VCCGTX	
L69	VCCGT		AM50	VCCGTX	
L70	VCCGT		AM52	VCCGTX	
L71	VCCGT		AM53	VCCGTX	
M62	VCCGT		AM56	VCCGTX	
N63	VCCGT		AM58	VCCGTX	
N64	VCCGT		AU58	VCCGTX	
N66	VCCGT		AU63	VCCGTX	
N67	VCCGT		BB57	VCCGTX	
N69	VCCGT		BB66	VCCGTX	
67 8 OUT CPU_VCCGTSENSE_P	J70	VCCGT_SENSE	AK62	VCCGTX_SENSE	CPU_VCCGTXSENSE_P 8
67 8 OUT CPU_VCCGTSENSE_N	J69	VSSGT_SENSE	AL61	VSSGTX_SENSE	CPU_VCCGTXSENSE_N 8

PPVCC_S0_CPU 8 54 100 104

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 12 OF 20
CPU POWER 1

A30	VCC		VCC	G32	
A34	VCC		VCC	G33	
A39	VCC		VCC	G35	
A44	VCC		VCC	G37	
AK33	VCC		VCC	G38	
AK35	VCC		VCC	G40	
AK37	VCC		VCC	G42	
AK38	VCC		VCC	J30	
AK40	VCC		VCC	J33	
AL33	VCC		VCC	J37	
AL37	VCC		VCC	J40	
AL40	VCC		VCC	K33	
AM32	VCC		VCC	K35	
AM33	VCC		VCC	K37	
AM35	VCC		VCC	K38	
AM37	VCC		VCC	K40	
AM38	VCC		VCC	K42	
G30	VCC		VCC	K43	
NC K32	RSVD		VCC_SENSE	E32	CPU_VCCSENSE_P OUT 8 67
NC AK32	RSVD		VSS_SENSE	E33	CPU_VCCSENSE_N OUT 8 67
100 8 PPVCCEDRAM_S0_CPU	AB62	VCCOPC	VIDALERT*	B63	CPU_VIDALERT_R_L
100 PPVCCEDRAM_S0_CPU	P62	VCCOPC	VIDSCK	A63	CPU_VIDSCLK_R
100 PPVCCEDRAM_S0_CPU	V62	VCCOPC	VIDSOUT	D64	CPU_VIDSOUT_R
100 PP1V8_SUS	H63	VCC_OPC_1P8	VCCSTG	G20	PP1V0_S0SW 6 8 10 17 101
100 PP1V8_SUS	G61	VCC_OPC_1P8			
8 CPU_VCCOPCSENSE_P	AC63	VCCOPC_SENSE			
8 CPU_VCCOPCSENSE_N	AE63	VSSOPC_SENSE			
100 8 PPVCCEDRAM_S0_CPU	AE62	VCCEOPIO			
100 PPVCCEDRAM_S0_CPU	AG62	VCCEOPIO			
8 CPU_VCCEOPIOSENSE_P	AL63	VCCEOPIO_SENSE			
8 CPU_VCCEOPIOSENSE_N	AJ62	VSSEOPIO_SENSE			

PP1V0_S3 6 8 10 14 19 101

R0827	56 1% 1/20W MF 201		
R0828	100 1% 1/20W MF 201		
R0829	220 1% 1/20W MF 201		CPU_VIDALERT_L IN 67
R0830	0 5% 1/20W MF 0201		CPU_VIDSCLK OUT 67
R0831	0 5% 1/20W MF 0201		CPU_VIDSOUT BI 67

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PLACE_NEAR=U0500.A63:12.7MM
PLACE_NEAR=U0500.D64:12.7MM

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J79_JSHAO SYNC_DATE=03/14/2016

PAGE TITLE

CPU & PCH Power

Apple Inc.

DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	8 OF 145
SHEET	8 OF 119

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 16 OF 20
GND1

102 NC_CPU_NCTFVSS_A5	A5	VSS	VSS	AL65	
	A67	VSS	VSS	AL66	
102 NC_CPU_NCTFVSS_A70	A70	VSS	VSS	AM13	
	AA2	VSS	VSS	AM21	
	AA4	VSS	VSS	AM25	
	AA65	VSS	VSS	AM27	
	AA68	VSS	VSS	AM43	
	AB15	VSS	VSS	AM45	
	AB16	VSS	VSS	AM46	
	AB18	VSS	VSS	AM55	
	AB21	VSS	VSS	AM60	
	AB8	VSS	VSS	AM61	
	AD13	VSS	VSS	AM68	
	AD16	VSS	VSS	AM71	
	AD19	VSS	VSS	AM8	
	AD20	VSS	VSS	AN20	
	AD21	VSS	VSS	AN23	
	AD62	VSS	VSS	AN28	
	AD8	VSS	VSS	AN30	
	AE64	VSS	VSS	AN32	
	AE65	VSS	VSS	AN33	
	AE66	VSS	VSS	AN35	
	AE67	VSS	VSS	AN37	
	AE68	VSS	VSS	AN38	
	AE69	VSS	VSS	AN40	
	AF1	VSS	VSS	AN42	
	AF10	VSS	VSS	AN58	
	AF15	VSS	VSS	AN63	
	AF17	VSS	VSS	AP10	
	AF2	VSS	VSS	AP18	
	AF4	VSS	VSS	AP20	
	AF63	VSS	VSS	AP23	
	AG16	VSS	VSS	AP28	
	AG17	VSS	VSS	AP32	
	AG18	VSS	VSS	AP35	
	AG19	VSS	VSS	AP38	
	AG20	VSS	VSS	AP42	
	AG21	VSS	VSS	AP58	
	AG71	VSS	VSS	AP63	
	AH13	VSS	VSS	AP68	
	AH6	VSS	VSS	AP70	
	AH63	VSS	VSS	AR11	
	AH64	VSS	VSS	AR15	
	AH67	VSS	VSS	AR16	
	AJ15	VSS	VSS	AR20	
	AJ18	VSS	VSS	AR23	
	AJ20	VSS	VSS	AR28	
	AJ4	VSS	VSS	AR35	
	AK11	VSS	VSS	AR42	
	AK16	VSS	VSS	AR43	
	AK18	VSS	VSS	AR45	
	AK21	VSS	VSS	AR46	
	AK22	VSS	VSS	AR48	
	AK27	VSS	VSS	AR5	
	AK63	VSS	VSS	AR50	
	AK68	VSS	VSS	AR52	
	AK69	VSS	VSS	AR53	
	AK8	VSS	VSS	AR55	
	AL2	VSS	VSS	AR58	
	AL28	VSS	VSS	AR63	
	AL32	VSS	VSS	AR8	
	AL35	VSS	VSS	AT2	
	AL38	VSS	VSS	AT20	
	AL4	VSS	VSS	AT23	
	AL45	VSS	VSS	AT28	
	AL48	VSS	VSS	AT35	
	AL52	VSS	VSS	AT4	
	AL55	VSS	VSS	AT42	
	AL58	VSS	VSS	AT56	
	AL64	VSS	VSS	AT58	

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 17 OF 20
GND2

	AT63	VSS	VSS	BA49	
	AT68	VSS	VSS	BA53	
	AT71	VSS	VSS	BA57	
	AU10	VSS	VSS	BA6	
	AU15	VSS	VSS	BA62	
	AU20	VSS	VSS	BA66	
	AU32	VSS	VSS	BA71	102 NC_CPU_NCTFVSS_BA71
	AU38	VSS	VSS	BB18	
102 NC_CPU_NCTFVSS_AV1	AV1	VSS	VSS	BB26	
	AV68	VSS	VSS	BB30	
	AV69	VSS	VSS	BB34	
	AV70	VSS	VSS	BB38	
	AV71	VSS	VSS	BB43	
	AW10	VSS	VSS	BB55	
	AW12	VSS	VSS	BB6	
	AW14	VSS	VSS	BB60	
	AW16	VSS	VSS	BB64	
	AW18	VSS	VSS	BB67	
	AW21	VSS	VSS	BB70	102 NC_CPU_NCTFVSS_BB70
	AW23	VSS	VSS	C1	102 NC_CPU_NCTFVSS_C1
	AW26	VSS	VSS	C25	
	AW28	VSS	VSS	C5	
	AW30	VSS	VSS	D10	
	AW32	VSS	VSS	D11	
	AW34	VSS	VSS	D14	
	AW36	VSS	VSS	D18	
	AW38	VSS	VSS	D22	
	AW41	VSS	VSS	D25	
	AW43	VSS	VSS	D26	
	AW45	VSS	VSS	D30	
	AW47	VSS	VSS	D34	
	AW49	VSS	VSS	D39	
	AW51	VSS	VSS	D44	
	AW53	VSS	VSS	D45	
	AW55	VSS	VSS	D47	
	AW57	VSS	VSS	D48	
	AW6	VSS	VSS	D53	
	AW60	VSS	VSS	D58	
	AW62	VSS	VSS	D6	
	AW64	VSS	VSS	D62	
	AW66	VSS	VSS	D66	
	AW8	VSS	VSS	D69	
	AY66	VSS	VSS	E11	
	B10	VSS	VSS	E15	
	B14	VSS	VSS	E18	
	B18	VSS	VSS	E21	
	B22	VSS	VSS	E46	
	B30	VSS	VSS	E50	
	B34	VSS	VSS	E53	
	B39	VSS	VSS	E56	
	B44	VSS	VSS	E6	
	B48	VSS	VSS	E65	
	B53	VSS	VSS	E71	
	B58	VSS	VSS	F1	
	B62	VSS	VSS	F13	
	B66	VSS	VSS	F2	
102 NC_CPU_NCTFVSS_B71	B71	VSS	VSS	F22	
102 NC_CPU_NCTFVSS_BA1	BA1	VSS	VSS	F23	
	BA10	VSS	VSS	F27	
	BA14	VSS	VSS	F28	
	BA18	VSS	VSS	F32	
	BA2	VSS	VSS	F33	
	BA23	VSS	VSS	F35	
	BA28	VSS	VSS	F37	
	BA32	VSS	VSS	F38	
	BA36	VSS	VSS	F4	
	F68	VSS	VSS	F40	
	BA45	VSS	VSS	F42	
			VSS	BA41	

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 18 OF 20
GND 3

	F8	VSS	VSS	L18	
	G10	VSS	VSS	L2	
	G22	VSS	VSS	L20	
	G43	VSS	VSS	L4	
	G45	VSS	VSS	L8	
	G48	VSS	VSS	N10	
	G5	VSS	VSS	N13	
	G52	VSS	VSS	N19	
	G55	VSS	VSS	N21	
	G58	VSS	VSS	N6	
	G6	VSS	VSS	N65	
	G60	VSS	VSS	N68	
	G63	VSS	VSS	P17	
	G66	VSS	VSS	P19	
	H15	VSS	VSS	P20	
	H18	VSS	VSS	P21	
	H71	VSS	VSS	R13	
	J11	VSS	VSS	R6	
	J13	VSS	VSS	T15	
	J25	VSS	VSS	T17	
	J28	VSS	VSS	T18	
	J32	VSS	VSS	T2	
	J35	VSS	VSS	T21	
	J38	VSS	VSS	T4	
	J42	VSS	VSS	U10	
	J8	VSS	VSS	U63	
	K16	VSS	VSS	U64	
	K18	VSS	VSS	U66	
	K22	VSS	VSS	U67	
	K61	VSS	VSS	U69	
	K63	VSS	VSS	U70	
	K64	VSS	VSS	V16	
	K65	VSS	VSS	V17	
	K66	VSS	VSS	V18	
	K67	VSS	VSS	W13	
	K68	VSS	VSS	W6	
	K70	VSS	VSS	W9	
	K71	VSS	VSS	Y17	
	L11	VSS	VSS	Y19	
	L16	VSS	VSS	Y20	
	L17	VSS	VSS	Y21	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J79_ALFRED SYNC_DATE=05/12/2015

PAGE TITLE

CPU & PCH Grounds

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 9 OF 145

SHEET 9 OF 119

100 PPVCC_S0_CPU

C1000 1UF 20% 6.3V X6S-CERM 0201
C1001 1UF 20% 6.3V X6S-CERM 0201
C1002 1UF 20% 6.3V X6S-CERM 0201
C1003 1UF 20% 6.3V X6S-CERM 0201
C1004 1UF 20% 6.3V X6S-CERM 0201
C1005 1UF 20% 6.3V X6S-CERM 0201
C1006 1UF 20% 6.3V X6S-CERM 0201
C1007 1UF 20% 6.3V X6S-CERM 0201
C1008 1UF 20% 6.3V X6S-CERM 0201
C1009 1UF 20% 6.3V X6S-CERM 0201
C100A 1UF 20% 6.3V X6S-CERM 0201
C100B 1UF 20% 6.3V X6S-CERM 0201
C100C 1UF 20% 6.3V X6S-CERM 0201
C100D 1UF 20% 6.3V X6S-CERM 0201
C100E 1UF 20% 6.3V X6S-CERM 0201
C100F 1UF 20% 6.3V X6S-CERM 0201
C100G 1UF 20% 6.3V X6S-CERM 0201
C100H 1UF 20% 6.3V X6S-CERM 0201

C100I 1UF 20% 6.3V X6S-CERM 0201
C100J 1UF 20% 6.3V X6S-CERM 0201
C100K 1UF 20% 6.3V X6S-CERM 0201
C100L 1UF 20% 6.3V X6S-CERM 0201
C100M 1UF 20% 6.3V X6S-CERM 0201
C100N 1UF 20% 6.3V X6S-CERM 0201
C100O 1UF 20% 6.3V X6S-CERM 0201
C100P 1UF 20% 6.3V X6S-CERM 0201
C100Q 1UF 20% 6.3V X6S-CERM 0201
C100R 1UF 20% 6.3V X6S-CERM 0201
C100S 1UF 20% 6.3V X6S-CERM 0201
C100T 1UF 20% 6.3V X6S-CERM 0201
C100U 1UF 20% 6.3V X6S-CERM 0201
C100V 1UF 20% 6.3V X6S-CERM 0201
C100W 1UF 20% 6.3V X6S-CERM 0201
C100X 1UF 20% 6.3V X6S-CERM 0201
C100Y 1UF 20% 6.3V X6S-CERM 0201

C1010 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C1011 20UF 20% 2.5V X6S-CERM 0402-1
C1012 20UF 20% 2.5V X6S-CERM 0402-1
C1013 20UF 20% 2.5V X6S-CERM 0402-1
C1014 20UF 20% 2.5V X6S-CERM 0402-1
C1015 20UF 20% 2.5V X6S-CERM 0402-1
C1016 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C1017 20UF 20% 2.5V X6S-CERM 0402-1
C1018 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C1019 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF

C1020 20UF 20% 2.5V X6S-CERM 0402-1
C1021 20UF 20% 2.5V X6S-CERM 0402-1
C1022 20UF 20% 2.5V X6S-CERM 0402-1
C1023 20UF 20% 2.5V X6S-CERM 0402-1
C1024 20UF 20% 2.5V X6S-CERM 0402-1
C1025 20UF 20% 2.5V X6S-CERM 0402-1
C1026 20UF 20% 2.5V X6S-CERM 0402-1
C1027 20UF 20% 2.5V X6S-CERM 0402-1
C1028 20UF 20% 2.5V X6S-CERM 0402-1
C1029 20UF 20% 2.5V X6S-CERM 0402-1

C10G0 220UF 20% 2V ELEC SM-COMBO
C10G1 220UF 20% 2V ELEC SM-COMBO
C10H1 220UF 20% 2V ELEC SM-COMBO
C10G3 220UF 20% 2V ELEC SM-COMBO

100 PP1V2_S3_CPUDDR

C1050 20UF 20% 2.5V X6S-CERM 0402-1
C1051 20UF 20% 2.5V X6S-CERM 0402-1
C1052 1UF 20% 6.3V X6S-CERM 0201
C1053 1UF 20% 6.3V X6S-CERM 0201
C1054 1UF 20% 6.3V X6S-CERM 0201
C1055 1UF 20% 6.3V X6S-CERM 0201

C1060 20UF 20% 2.5V X6S-CERM 0402-1
C1061 20UF 20% 2.5V X6S-CERM 0402-1
C1062 20UF 20% 2.5V X6S-CERM 0402-1
C1063 20UF 20% 2.5V X6S-CERM 0402-1
C1064 20UF 20% 2.5V X6S-CERM 0402-1
C1065 20UF 20% 2.5V X6S-CERM 0402-1
C1066 20UF 20% 2.5V X6S-CERM 0402-1

100 PP1V2_S3_CPUDDR

C1070 20UF 20% 2.5V X6S-CERM 0402-1 Primary
C1071 1UF 20% 6.3V X6S-CERM 0201 Backside

100 PPVCCIO_S0_CPU

C1080 20UF 20% 2.5V X6S-CERM 0402-1
C1081 20UF 20% 2.5V X6S-CERM 0402-1
C1082 1UF 20% 6.3V X6S-CERM 0201
C1083 1UF 20% 6.3V X6S-CERM 0201
C1084 1UF 20% 6.3V X6S-CERM 0201
C1085 1UF 20% 6.3V X6S-CERM 0201

C1090 20UF 20% 2.5V X6S-CERM 0402-1
C1091 20UF 20% 2.5V X6S-CERM 0402-1
C1092 20UF 20% 2.5V X6S-CERM 0402-1
C1093 20UF 20% 2.5V X6S-CERM 0402-1
C1094 20UF 20% 2.5V X6S-CERM 0402-1
C1095 20UF 20% 2.5V X6S-CERM 0402-1

100 PPVCCSA_S0_CPU

C10A0 1UF 20% 6.3V X6S-CERM 0201
C10A1 1UF 20% 6.3V X6S-CERM 0201
C10A2 1UF 20% 6.3V X6S-CERM 0201
C10A3 1UF 20% 6.3V X6S-CERM 0201
C10A4 1UF 20% 6.3V X6S-CERM 0201
C10A5 1UF 20% 6.3V X6S-CERM 0201
C10A6 1UF 20% 6.3V X6S-CERM 0201

C10B0 20UF 20% 2.5V X6S-CERM 0402-1
C10B1 20UF 20% 2.5V X6S-CERM 0402-1
C10B2 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C10B3 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C10B4 20UF 20% 2.5V X6S-CERM 0402-1
C10B5 20UF 20% 2.5V X6S-CERM 0402-1

C10C0 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C10C1 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C10C2 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C10C3 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C10C4 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF
C10C5 20UF 20% 2.5V X6S-CERM 0402-1 NOSTUFF

C10H0 220UF 20% 2V ELEC SM-COMBO

100 PPVCCEDRAM_S0_CPU

C10D0 20UF 20% 2.5V X6S-CERM 0402-1
C10D1 1UF 20% 6.3V X6S-CERM 0201
C10D2 1UF 20% 6.3V X6S-CERM 0201
C10D3 1UF 20% 6.3V X6S-CERM 0201
C10D4 1UF 20% 6.3V X6S-CERM 0201
C10D5 1UF 20% 6.3V X6S-CERM 0201
C10D6 1UF 20% 6.3V X6S-CERM 0201

100 PPVCCEDRAM_S0_CPU

C10E0 20UF 20% 2.5V X6S-CERM 0402-1
C10E1 20UF 20% 2.5V X6S-CERM 0402-1

101 8 PP1V0_S3

C10F0 1UF 20% 6.3V X6S-CERM 0201

100 8 PP1V2_S0SW

C10F1 1UF 20% 6.3V X6S-CERM 0201

14 8 6 102 19 PP1V0_S3

C10F2 1UF 20% 6.3V X6S-CERM 0201

101 17 8 6 PP1V0_S0SW

C10F3 1UF 20% 6.3V X6S-CERM 0201

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J79_JSHAO SYNC_DATE=08/28/2015

PAGE TITLE

CPU Core Decoupling

Apple Inc.

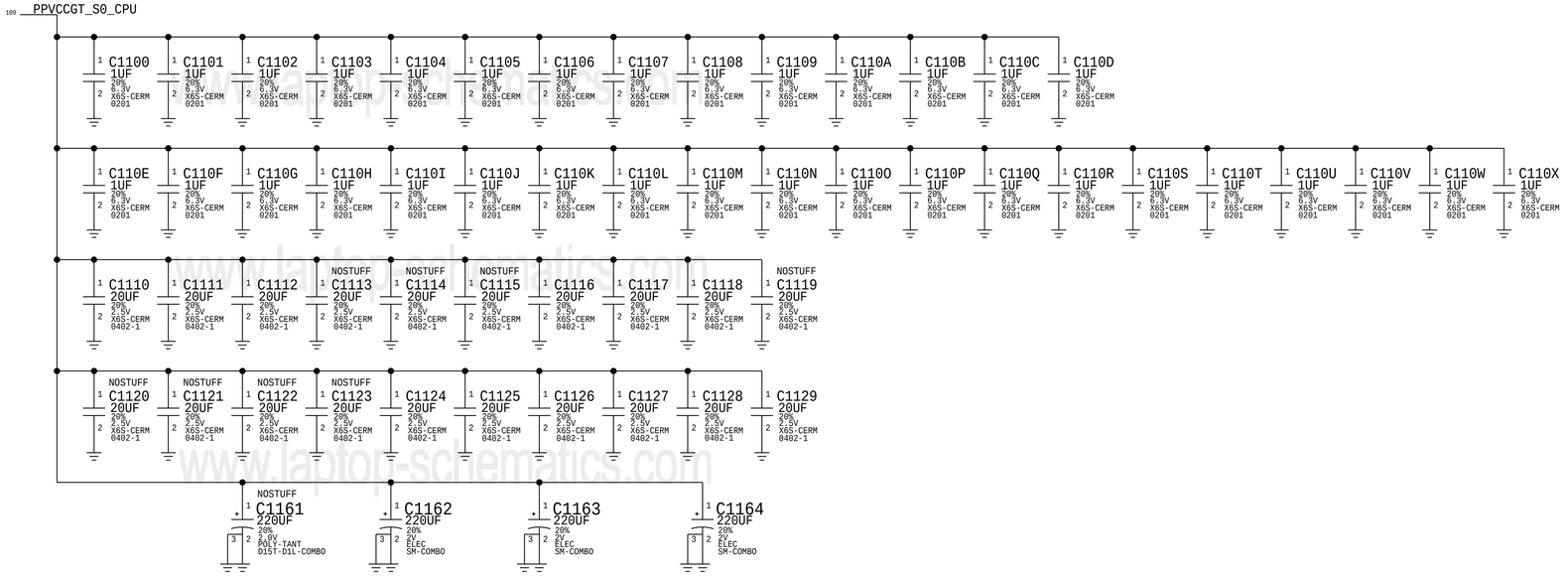
DRAWING NUMBER 051-00777 SIZE D

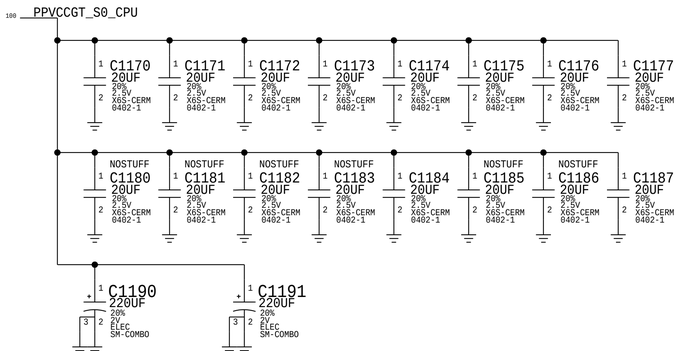
REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 10 OF 145

SHEET 10 OF 119





BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J79_JSHAO SYNC_DATE=08/28/2015

PAGE TITLE

CPU GT Decoupling

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 11 OF 145

SHEET 11 OF 119

PP1V0_SUSFUSE
BYPASS=U0500.AK20::10MM
C1208 1000PF 10% 25V X7R 0201

PP1V0_SUS
BYPASS=U0500.AB19::10MM
C1200 1000PF 10% 25V X7R 0201

PP1V0_SUS
BYPASS=U0500.K17::3MM
C1201 1UF 20% 6.3V X6S-CERM 0201

PP1V0_SUSSW
BYPASS=U0500.N15::3MM
C1202 1UF 20% 6.3V X6S-CERM 0201
CRITICAL NOSTUFF
C1203 47UF 20% 6.3V POLY-TANT 0805
BYPASS=U0500.N15::10MM

PP1V0_SUSSW
BYPASS=U0500.AF20::10MM
C1205 1000PF 10% 25V X7R 0201

PP1V0_SUSSW
BYPASS=U0500.N18::3MM
C1206 1UF 20% 6.3V X6S-CERM 0201

PPVCCPRIMCORE_SUS_PCH
BYPASS=U0500.AF18::10MM
C1210 1000PF 10% 25V X7R 0201

PPDCPRTC_PCH
BYPASS=U0500.BB10::3MM
C1231 0.1UF 10% 10V X5R-CERM 0201

PP3V3_SUS
BYPASS=U0500.T16::3MM
C1220 1000PF 10% 25V X7R 0201

PP3V3_SUS
BYPASS=U0500.AK17::3MM
C1221 1UF 20% 6.3V X6S-CERM 0201
C1222 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U0500.AK17::3MM

PP3V3_SUS
BYPASS=U0500.AG15::3MM
C1223 1000PF 10% 25V X7R 0201

PP3V3_SUS
BYPASS=U0500.V19::10MM
C1224 1000PF 10% 25V X7R 0201

PP3V3_SUS
BYPASS=U0500.Y16::10MM
C1225 1000PF 10% 25V X7R 0201

PP3V0_G3H
BYPASS=U0500.AK19::3MM
C1227 1UF 20% 6.3V X6S-CERM 0201
C1228 0.1UF 10% 10V X5R-CERM 0201
BYPASS=U0500.AK19::3MM

PP1V8_SUS
BYPASS=U0500.AA1::10MM
C1230 1UF 20% 6.3V X6S-CERM 0201

PP1V_S5_PCH_DCPDSW
BYPASS=U0500.AL1::3MM
C1232 1UF 20% 6.3V X6S-CERM 0201

PP1V8_S0
C1264 12PF 5% 25V C0G-C0G 0201
C1265 2.9PF +/-0.05PF 25V C0G-CERM 0201
R1260 0 5% 1/20W MF 0201
C1226 1000PF 10% 25V X7R 0201
C1260 2.9PF +/-0.05PF 25V C0G-CERM 0201
PP1V8_S0_PCH_VCCHDA_F
PP1V8_S0_PCH_VCCHDA_F
MAKE_BASE=TRUE
BYPASS=U0500.AJ19::10MM
BYPASS=U0500.AJ19::10MM

PP1V0_SUS
C1267 2.9PF +/-0.05PF 25V C0G-CERM 0201
R1261 0 5% 1/20W MF 0201
C1261 1000PF 10% 25V X7R 0201
C1262 2.9PF +/-0.05PF 25V C0G-CERM 0201
PP1V_SUS_PCH_VCCAPLL_F
PP1V_SUS_PCH_VCCAPLL_F
MAKE_BASE=TRUE
BYPASS=U0500.V15::10MM
BYPASS=U0500.V15::10MM

FILTER PLACEHOLDERS ONLY

RAIL SIDE PCH SIDE

PP1V0_SUSSW
OMIT_TABLE
L1250 2.2UH-240MA-0.221OHM 0603
C1204 1UF 20% 6.3V X6S-CERM 0201
CRITICAL NOSTUFF
C1250 47UF 20% 6.3V POLY-TANT 0805
BYPASS=U0500.K15::3MM
PP1V_SUSSW_PCH_VCCAMPHYPLL_F
PP1V_SUSSW_PCH_VCCAMPHYPLL_F
MAKE_BASE=TRUE

PP1V0_SUS
OMIT_TABLE
L1252 2.2UH-240MA-0.221OHM 0603
CRITICAL NOSTUFF
C1252 47UF 20% 6.3V POLY-TANT 0805
PP1V_SUS_PCH_VCCCLK5_F
PP1V_SUS_PCH_VCCCLK5_F
MAKE_BASE=TRUE

PP1V0_SUS
OMIT_TABLE
L1253 2.2UH-240MA-0.221OHM 0603
CRITICAL NOSTUFF
C1253 47UF 20% 6.3V POLY-TANT 0805
PP1V_SUS_PCH_VCCCLK4_F
PP1V_SUS_PCH_VCCCLK4_F
MAKE_BASE=TRUE

PP1V0_SUS
OMIT_TABLE
L1254 2.2UH-240MA-0.221OHM 0603
CRITICAL NOSTUFF
C1254 47UF 20% 6.3V POLY-TANT 0805
PP1V_SUS_PCH_VCCCLK2_F
PP1V_SUS_PCH_VCCCLK2_F
MAKE_BASE=TRUE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	4	RES,MF,1A MAX,0OHM,5%,0603	L1250,L1252,L1253,L1254		

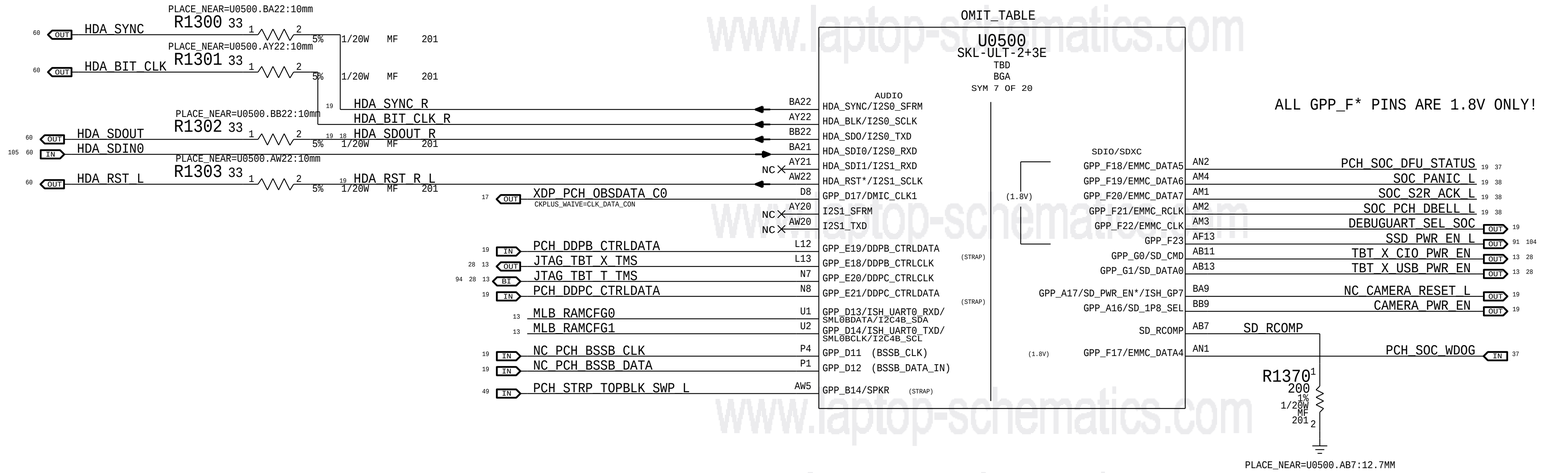
PP1V8_SUS
NOSTUFF
R1251 0 5% 1/20W MF 0201
BYPASS=U0500.U11::10MM
C1251 1UF 20% 6.3V X6S-CERM 0201
NOSTUFF
FOR FUTURE PRODUCT PER PDG
PP1V8_SUS_PCH_VCC1P8
PP1V8_SUS_PCH_VCC1P8
PP1V8_SUS_PCH_VCC1P8
MAKE_BASE=TRUE

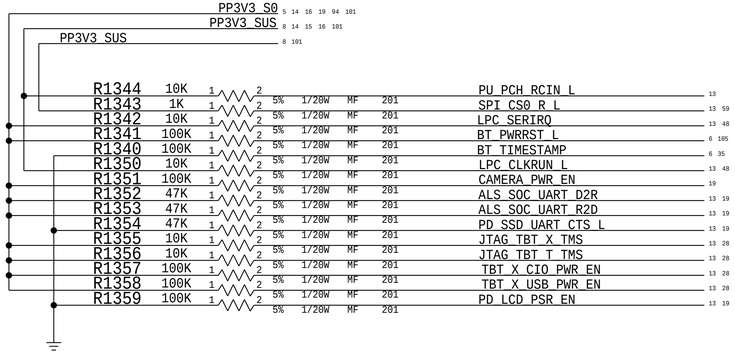
BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: PCH Decoupling

Apple Inc.

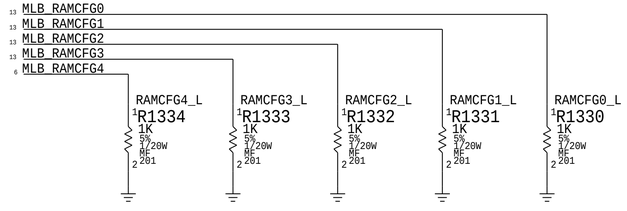
DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 12 OF 145
SHEET: 12 OF 119





MEMORY CONFIGURATION STRAPS.

PCH INTERNAL PULL-UPS ARE TO 3.3V.



BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4_L,RAMCFG3_L,RAMCFG2_L,RAMCFG1_L,RAMCFG0_L

BOM_COST_GROUP=CPU & CHIPSET

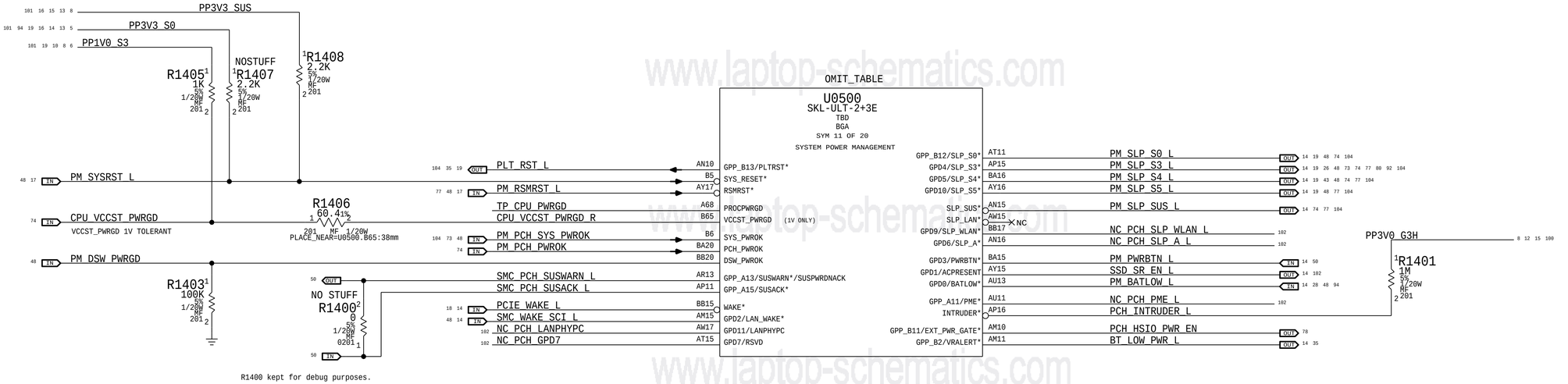
DESIGN: X502/MLB
LAST CHANGE: Tue Feb 2 13:18:21 2016

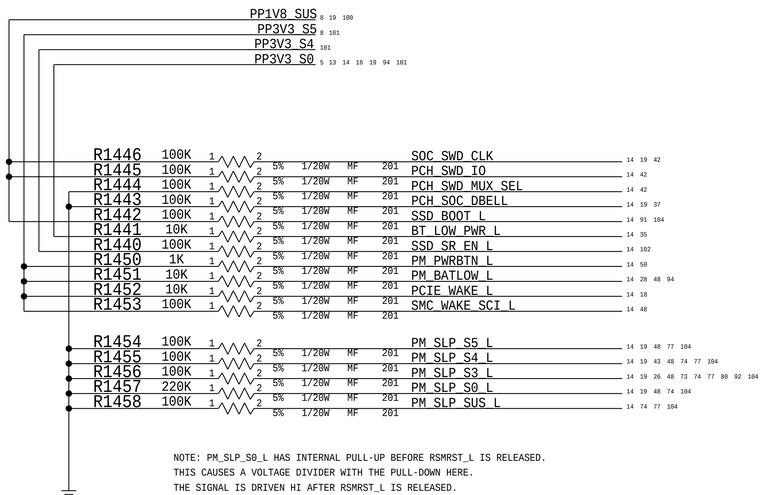
PAGE TITLE
PCH Audio/LPC/SPI/SMBus

Apple Inc.

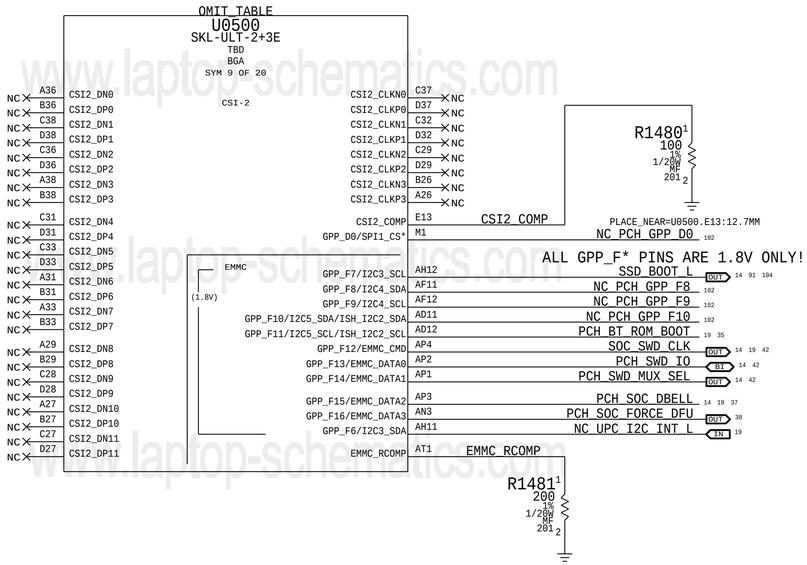
DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 13 OF 145
SHEET 13 OF 119

PCH Reset Button





NOTE: PM_SLP_S0_L HAS INTERNAL PULL-UP BEFORE RSMRST_L IS RELEASED.
THIS CAUSES A VOLTAGE DIVIDER WITH THE PULL-DOWN HERE.
THE SIGNAL IS DRIVEN HI AFTER RSMRST_L IS RELEASED.



BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Tue May 3 17:45:28 2016

PAGE TITLE
PCH Power Management

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 14 OF 145
SHEET 14 OF 119

PCIe Port Assignments:

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 8 OF 20

SSD LANE 0
- PCIE_SSD_D2R_N<0> — H13 PCIE1_RXN/USB3_5_RXN
- PCIE_SSD_D2R_P<0> — G13 PCIE1_RXP/USB3_5_RXP
- PCIE_SSD_R2D_C_N<0> — B17 PCIE1_TXN/USB3_5_TXN
- PCIE_SSD_R2D_C_P<0> — A17 PCIE1_TXP/USB3_5_TXP

SSD LANE 1
- PCIE_SSD_D2R_N<1> — G11 PCIE2_RXN/USB3_6_RXN
- PCIE_SSD_D2R_P<1> — F11 PCIE2_RXP/USB3_6_RXP
- PCIE_SSD_R2D_C_N<1> — D16 PCIE2_TXN/USB3_6_TXN
- PCIE_SSD_R2D_C_P<1> — C16 PCIE2_TXP/USB3_6_TXP

SSD LANE 2
- PCIE_SSD_D2R_N<2> — H16 PCIE3_RXN
- PCIE_SSD_D2R_P<2> — G16 PCIE3_RXP
- PCIE_SSD_R2D_C_N<2> — D17 PCIE3_TXN
- PCIE_SSD_R2D_C_P<2> — C17 PCIE3_TXP

SSD LANE 3
- PCIE_SSD_D2R_N<3> — G15 PCIE4_RXN
- PCIE_SSD_D2R_P<3> — F15 PCIE4_RXP
- PCIE_SSD_R2D_C_N<3> — B19 PCIE4_TXN
- PCIE_SSD_R2D_C_P<3> — A19 PCIE4_TXP

Thunderbolt X lane 0
- PCIE_TBT_X_D2R_N<0> — F16 PCIE5_RXN
- PCIE_TBT_X_D2R_P<0> — E16 PCIE5_RXP
- PCIE_TBT_X_R2D_C_N<0> — C19 PCIE5_TXN
- PCIE_TBT_X_R2D_C_P<0> — D19 PCIE5_TXP

Thunderbolt X lane 1
- PCIE_TBT_X_D2R_N<1> — G18 PCIE6_RXN
- PCIE_TBT_X_D2R_P<1> — F18 PCIE6_RXP
- PCIE_TBT_X_R2D_C_N<1> — D20 PCIE6_TXN
- PCIE_TBT_X_R2D_C_P<1> — C20 PCIE6_TXP

Thunderbolt X lane 2
- PCIE_TBT_X_D2R_N<2> — F20 PCIE7_RXN/SATA0_RXN
- PCIE_TBT_X_D2R_P<2> — E20 PCIE7_RXP/SATA0_RXP
- PCIE_TBT_X_R2D_C_N<2> — B21 PCIE7_TXN/SATA0_TXN
- PCIE_TBT_X_R2D_C_P<2> — A21 PCIE7_TXP/SATA0_TXP

Thunderbolt X lane 3
- PCIE_TBT_X_D2R_N<3> — G21 PCIE8_RXN/SATA1A_RXN
- PCIE_TBT_X_D2R_P<3> — F21 PCIE8_RXP/SATA1A_RXP
- PCIE_TBT_X_R2D_C_N<3> — D21 PCIE8_TXN/SATA1A_TXN
- PCIE_TBT_X_R2D_C_P<3> — C21 PCIE8_TXP/SATA1A_TXP

AirPort
- PCIE_AP_D2R_N — E22 PCIE9_RXN
- PCIE_AP_D2R_P — E23 PCIE9_RXP
- PCIE_AP_R2D_C_N — B23 PCIE9_TXN
- PCIE_AP_R2D_C_P — A23 PCIE9_TXP

CAMERA
- NC_PCIE_CAMERA_D2R_N — F25 PCIE10_RXN
- NC_PCIE_CAMERA_D2R_P — E25 PCIE10_RXP
- NC_PCIE_CAMERA_R2D_C_N — D23 PCIE10_TXN
- NC_PCIE_CAMERA_R2D_C_P — C23 PCIE10_TXP

PLACE_NEAR=U0500.F5:12.7mm
R1504 100 1% 1/20W MF 201

- PCH_PCIE_RCOMP_N — F5 PCIE_RCOMPN
- PCH_PCIE_RCOMP_P — E5 PCIE_RCOMPP

- XDP_CPU_PRDY_L — D56 PROC_PRDY*
- XDP_CPU_PREQ_L — D61 PROC_PREQ*
- SMC_RUNTIME_SCI_L — BB11 GPP_A7/PIRQA*

Thunderbolt T lane 0
- PCIE_TBT_T_D2R_N<0> — E28 PCIE11_RXN/SATA1B_RXN
- PCIE_TBT_T_D2R_P<0> — E27 PCIE11_RXP/SATA1B_RXP
- PCIE_TBT_T_R2D_C_N<0> — D24 PCIE11_TXN/SATA1B_TXN
- PCIE_TBT_T_R2D_C_P<0> — C24 PCIE11_TXP/SATA1B_TXP

Thunderbolt T lane 1
- PCIE_TBT_T_D2R_N<1> — E30 PCIE12_RXN/SATA2_RXN
- PCIE_TBT_T_D2R_P<1> — F30 PCIE12_RXP/SATA2_RXP
- PCIE_TBT_T_R2D_C_N<1> — A25 PCIE12_TXN/SATA2_TXN
- PCIE_TBT_T_R2D_C_P<1> — B25 PCIE12_TXP/SATA2_TXP

SSIC/USB3
- USB3_1_RXN — H8 USB3_EXTA_D2R_N ← IN 28
- USB3_1_RXP — G8 USB3_EXTA_D2R_P ← IN 28
- USB3_1_TXN — C13 USB3_EXTA_R2D_C_N → OUT 28
- USB3_1_TXP — D13 USB3_EXTA_R2D_C_P → OUT 28

EXT A (SS,DCI)

- USB3_2_RXN/SSIC_RXN — J6 NC_USB3_EXTB_D2R_N ← IN 102
- USB3_2_RXP/SSIC_RXP — H6 NC_USB3_EXTB_D2R_P ← IN 102
- USB3_2_TXN/SSIC_TXN — B13 NC_USB3_EXTB_R2D_C_N → OUT 102
- USB3_2_TXP/SSIC_TXP — A13 NC_USB3_EXTB_R2D_C_P → OUT 102

EXT B (SS)

- USB3_3_RXN — J10 TP_USB3_03_D2RN 104
- USB3_3_RXP — H10 TP_USB3_03_D2RP 104
- USB3_3_TXN — B15 TP_USB3_03_R2DN 104
- USB3_3_TXP — A15 TP_USB3_03_R2DP 104

- USB3_4_RXN — E10 NC_USB3_04_D2RN 19
- USB3_4_RXP — F10 NC_USB3_04_D2RP 19
- USB3_4_TXN — C15 NC_USB3_04_R2DN 19
- USB3_4_TXP — D15 NC_USB3_04_R2DP 19

USB2
- USB2N_1 — AB9 NC_USB_EXTA_N ↔ BI 102
- USB2P_1 — AB10 NC_USB_EXTA_P ↔ BI 102

EXT A (LS/FS/HS)

- USB2N_2 — AD6 NC_USB_EXTB_N ↔ BI 102
- USB2P_2 — AD7 NC_USB_EXTB_P ↔ BI 102

EXT B (LS/FS/HS)

- USB2N_3 — AH3 USB_CAMERA_DFR_N ↔ BI 38 105
- USB2P_3 — AJ3 USB_CAMERA_DFR_P ↔ BI 38 105
- USB2N_4 — AD9 TP_USB_TESTERN 104
- USB2P_4 — AD10 TP_USB_TESTERP 104
- USB2N_5 — AJ1 NC_USB2_05N 19
- USB2P_5 — AJ2 NC_USB2_05P 19
- USB2N_6 — AF6 USB_UPC_PCH_XA_N 28
- USB2P_6 — AF7 USB_UPC_PCH_XA_P 28
- USB2N_7 — AH1 USB_UPC_PCH_TA_N 94
- USB2P_7 — AH2 USB_UPC_PCH_TA_P 94
- USB2N_8 — AF8 USB_UPC_PCH_XB_N 28
- USB2P_8 — AF9 USB_UPC_PCH_XB_P 28
- USB2N_9 — AG1 USB_UPC_PCH_TB_N 94
- USB2P_9 — AG2 USB_UPC_PCH_TB_P 94
- USB2N_10 — AH7 NC_USB2_10N 19
- USB2P_10 — AH8 NC_USB2_10P 19

PCIE/USB3/SATA
- USB2_COMP — AB6 PCH_USB2_COMP
- USB2_ID — AG3
- USB2_VBUSSENSE — AG4 PCH_USB2_VBUSSENSE

GROUNDED PER SKYLAKE MOW 2015WW10.

R1503 1K 5% 1/20W MF 201 — PLACE_NEAR=U0500.AG4:12.7MM

R1501 113 1% 1/20W MF 201 — PLACE_NEAR=U0500.AB6:12.7MM

- GPP_E3/CPU_GP0 — A6 XDP_PCH_OBSFN_C1 ← IN 17
- GPP_E4/DEVSLP0 — J1 XDP_JTAG_ISP_TCK ← IN 17
- GPP_E5/DEVSLP1 — J2 XDP_JTAG_ISP_TDI ← IN 17
- GPP_E6/DEVSLP2 — J3 XDP_PCH_OBSDATA_A2 ← IN 17
- GPP_D22/SPI1_IO3 — V2 NC_SPKR_ID0 ← IN 19
- GPP_D23/I2S_MCLK — J5 XDP_PCH_OBSDATA_D0 ← IN 17 CKPLUS_WAIVE=CLK_DATA_CON
- GPP_E0/SATAXPCIE0/SATAGP0 — H2 XDP_PCH_OBSDATA_D1 ← IN 17
- GPP_D18/DMIC_DATA1 — C8 XDP_PCH_OBSDATA_C1 ← IN 17
- GPP_D19/DMIC_CLK0 — H5 XDP_PCH_OBSDATA_C2 ← IN 17 CKPLUS_WAIVE=CLK_DATA_CON
- GPP_D20/DMIC_DATA0 — D7 XDP_PCH_OBSDATA_C3 ← IN 17
- GPP_E2/SATAXPCIE2/SATAGP2 — G4 XDP_PCH_OBSDATA_D3 ← IN 17

OMIT_TABLE

U0500
SKL-ULT-2+3E
TBD
BGA
SYM 10 OF 20

CLOCK SIGNALS

ANY CLKREQ CAN MAP TO ANY CLK.
ANY CLKREQ OR CLK CAN MAP TO ANY PCIE PORT.
UNUSED CLKREQS AND CLKS SHOULD BE DISABLED.
PER SKYLAKE PDG, SKYLAKE PCH EDS.

- PCIE_CLK100M_SSD_N — D42 CLKOUT_PCIE_N0
- PCIE_CLK100M_SSD_P — C42 CLKOUT_PCIE_P0
- SSD_CLKREQ_L_R — AR10 GPP_B5/SRCCLKREQ0*
- PCIE_CLK100M_TBT_X_N — B42 CLKOUT_PCIE_N1
- PCIE_CLK100M_TBT_X_P — A42 CLKOUT_PCIE_P1
- TBT_X_CLKREQ_L_R — AT7 GPP_B6/SRCCLKREQ1*
- PCIE_CLK100M_TBT_T_N — D41 CLKOUT_PCIE_N2
- PCIE_CLK100M_TBT_T_P — C41 CLKOUT_PCIE_P2
- TBT_T_CLKREQ_L_R — AT8 GPP_B7/SRCCLKREQ2*
- PCIE_CLK100M_AP_N — D40 CLKOUT_PCIE_N3
- PCIE_CLK100M_AP_P — C40 CLKOUT_PCIE_P3
- AP_CLKREQ_L_R — AT10 GPP_B8/SRCCLKREQ3*
- NC_PCIE_CLK100M_CAMERA_N — B40 CLKOUT_PCIE_N4
- NC_PCIE_CLK100M_CAMERA_P — A40 CLKOUT_PCIE_P4
- NC_PCH_CLKREQ4_L — AU8 GPP_B9/SRCCLKREQ4*
- NC_PCIE_CLK100M5N — E40 CLKOUT_PCIE_N5
- NC_PCIE_CLK100M5P — E38 CLKOUT_PCIE_P5
- NC_PCH_CLKREQ5_L — AU7 GPP_B10/SRCCLKREQ5*

- CLKOUT_ITPXDP_N — F43 NC_ITPXDP_CLK100M_N 19
- CLKOUT_ITPXDP_P — E43 NC_ITPXDP_CLK100M_P 19
- GPD8/SUSCLK — BA17 PM_CLK32K_SUSCLK_R → OUT 49
- XTAL24_IN — E37 PCH_CLK24M_XTALIN ← IN 19
- XTAL24_OUT — E35 NC_PCH_CLK24M_XTALOUT → OUT 19
- XCLK_BIASREF — E42 PCH_DIFFCLK_BIASREF
- RTCX1 — AM18 SYSCLK_CLK32K_PCH ← IN 19
- RTCX2 — AM20 NC_PCH_CLK32K_RTCX2 → OUT 19
- SRTCRST* — AN18 PCH_SRTCRST_L
- RTCRST* — AM16 RTC_RESET_L

PP1V0_SUS 12 101
PLACE_NEAR=U0500.E42:2.54mm
R1520 2.7K 1% 1/20W MF 201

PP3V0_G3H 8 12 14 100
R1530 20K 1% 1/20W MF 201
R1531 20K 1% 1/20W MF 201

C1530 1UF 20% 6.3V X6S-CERM 0201
C1531 1UF 20% 6.3V X6S-CERM 0201

PP3V3_SUS 8 13 14 16 101
R1550 100K 5% 1/20W MF 201 — SMC_RUNTIME_SCI_L 15 48

BOM_COST_GROUP=CPU & CHIPSET

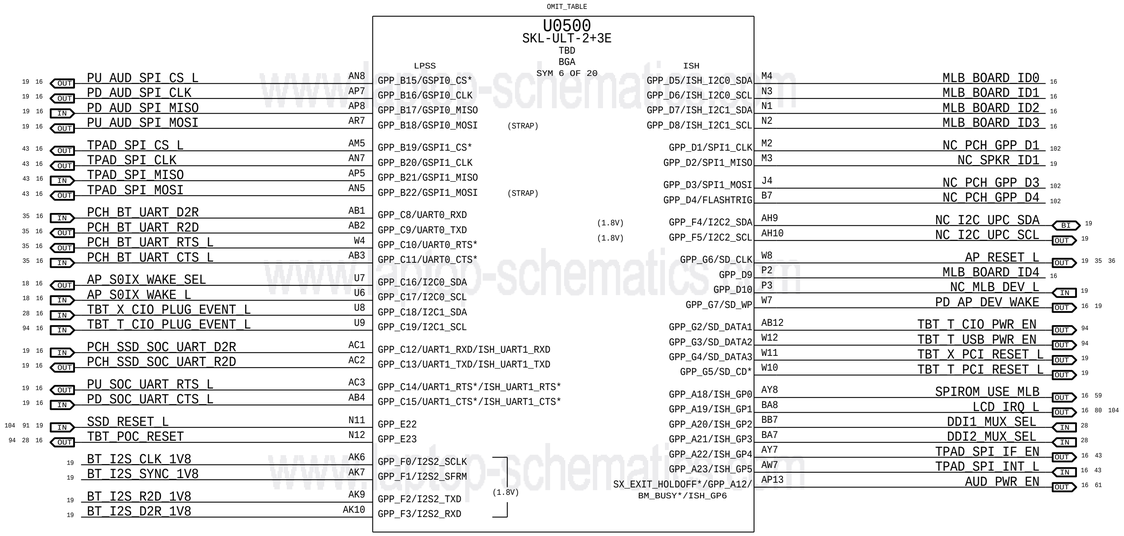
DESIGN: X502/MLB
LAST CHANGE: Thu Jun 18 20:05:18 2015

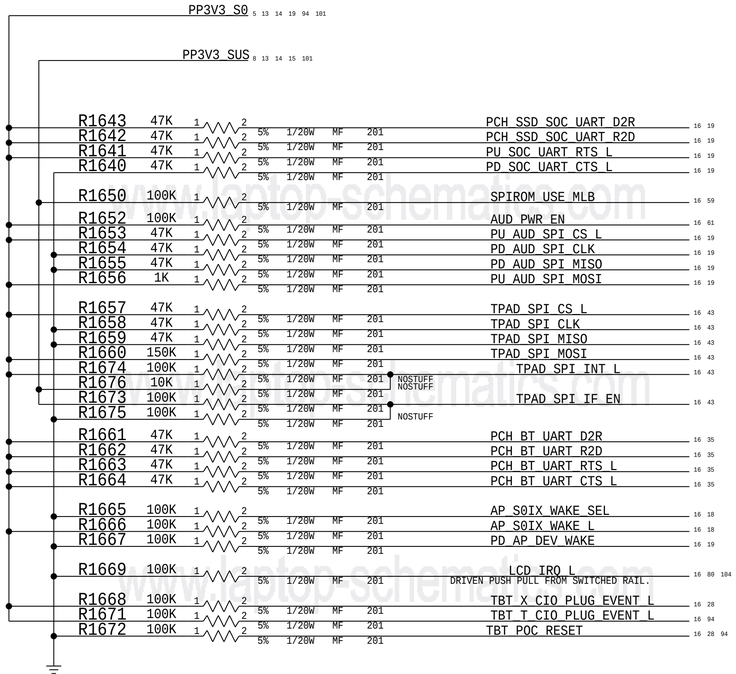
PAGE TITLE
PCH PCIE/USB/CLKS

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 15 OF 145
SHEET 15 OF 119

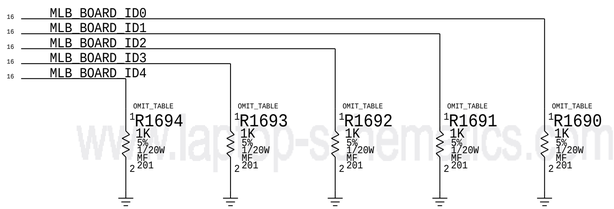
ALL GPP_F* PINS ARE 1.8V ONLY!





MLB ID STRAPS.

PCH INTERNAL PULL-UPS ARE TO VCCGPPD = 3.3V.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	CODE
117S0006	0	RES,MF,1/20W/1K OHM,5,0201,SMD		BOARD_ID:0	<11111>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1690	BOARD_ID:1	<11110>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691	BOARD_ID:2	<11101>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1691,R1690	BOARD_ID:3	<11100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692	BOARD_ID:4	<11011>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1690	BOARD_ID:5	<11010>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691	BOARD_ID:6	<11001>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1692,R1691,R1690	BOARD_ID:7	<11000>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693	BOARD_ID:8	<10111>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1690	BOARD_ID:9	<10110>
117S0006	2	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691	BOARD_ID:10	<10101>
117S0006	3	RES,MF,1/20W/1K OHM,5,0201,SMD	R1693,R1691,R1690	BOARD_ID:11	<10100>
117S0006	1	RES,MF,1/20W/1K OHM,5,0201,SMD	R1694	BOARD_ID:16	<01111>

BOM_COST_GROUP=CPU & CHIPSET

DESIGN: X502/MLB
LAST CHANGE: Wed Oct 28 12:50:22 2015

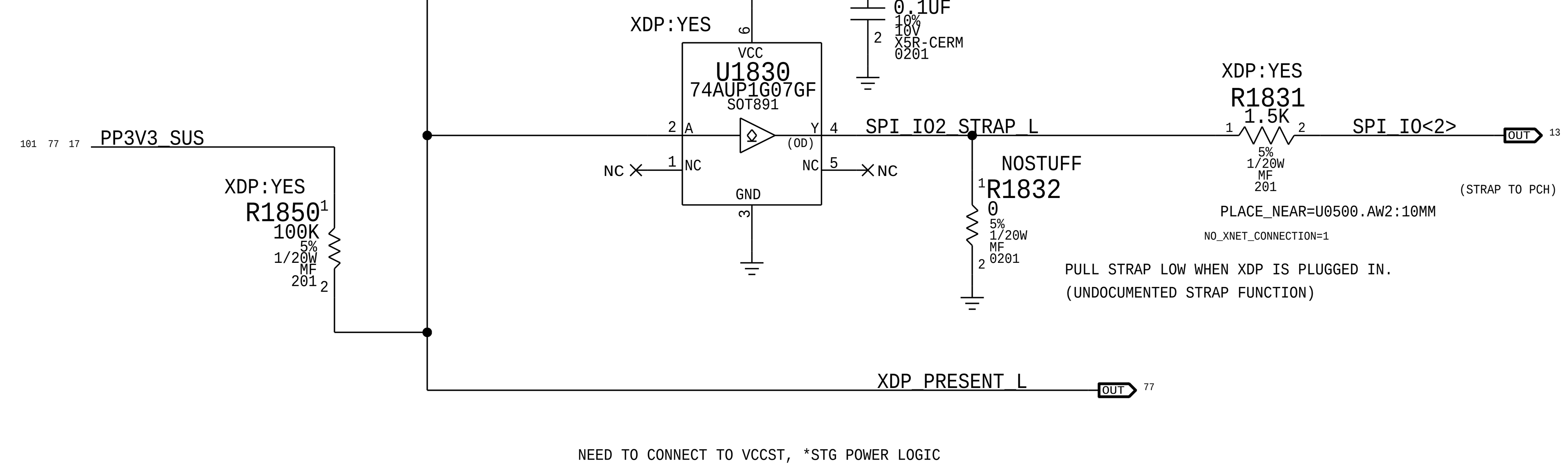
PAGE TITLE
PCH SPI/UART/GPIO

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 16 OF 145
SHEET 16 OF 119

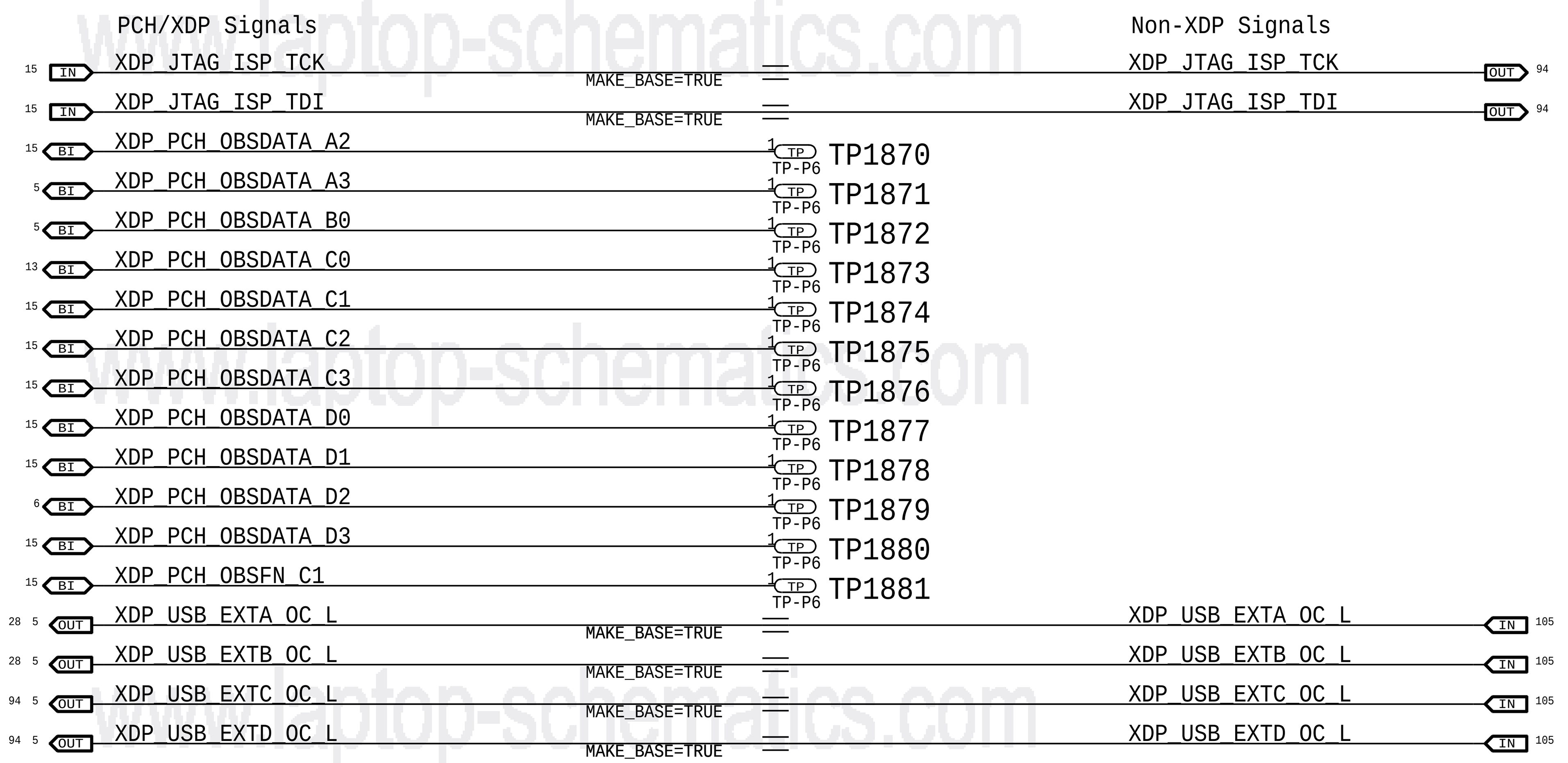
Primary / Merged (CPU/PCH) Micro2-XDP

PP1V0_SUS
XDP_CONN:YES
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847
NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.
PLACE_NEAR=U0500.D67:2.54MM
XDP:YES
R1801
1K
PULL CFG<3> LOW
WHEN XDP PRESENT
XDP_PRESENT_CPU
XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
CPU_CFG<17>
CPU_CFG<16>
CPU_CFG<8>
CPU_CFG<9>
CPU_CFG<10>
CPU_CFG<11>
CPU_CFG<19>
CPU_CFG<18>
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
PM_RSMRST_L
R1800 1K
PLACE_NEAR=U0500.AY17:18MM
PM_PWRBTN_L
R1802 10
PLACE_NEAR=U0500.BA15:2.54MM
XDP_PM_RSMRST_L
XDP_CPU_PWRBTN_L
XDP_CPU_TCK
XDP_PCH_TCK
PCH_JTAGX
R1835 0
PLACE_NEAR=J1800.58:28MM
XDP:YES C1804 0.1UF
PLACE_NEAR=J1800.42:28MM
XDP:YES C1800 0.1UF
PLACE_NEAR=J1800.44:28MM
XDP:YES C1801 0.1UF
PLACE_NEAR=J1800.43:28MM
XDP:YES C1806 0.1UF
PLACE_NEAR=J1800.47:28MM
PP1V0_S0SW
XDP_PCH_TDO R1890 51 PLACE_NEAR=U0500.A56:28MM
XDP_PCH_TDI R1891 51 PLACE_NEAR=U0500.D59:28MM
XDP_PCH_TMS R1892 51 PLACE_NEAR=U0500.C59:28MM
XDP_CPU_TDO R1810 51 PLACE_NEAR=U0500.A61:28MM
XDP_CPU_TCK R1813 51 PLACE_NEAR=U0500.B61:28MM
NOSTUFF
XDP_PCH_TCK R1897 51 PLACE_NEAR=U0500.C61:28MM
R1830 1K
ITP_PMODE
XDP_DBRESET_L
XDP:YES R1806 0
PLACE_NEAR=U0500.E8:2.54MM
PM_SYSRST_L
ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.
R1821 0 PLACE_NEAR=J1800.51:2.54MM XDP_CPU_TDO
R1822 0 PLACE_NEAR=J1800.53:2.54MM XDP_CPU_TRST_L
R1823 0 PLACE_NEAR=J1800.55:2.54MM XDP_CPU_TDI
R1824 0 PLACE_NEAR=J1800.57:2.54MM XDP_CPU_TMS
XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS
PP3V3_SUS
XDP:YES C1830 0.1UF
XDP:YES
U1830
74AUP1G07GF
SOT891
SPI_IO2_STRAP_L
NOSTUFF R1832 0
XDP:YES R1831 1.5K
SPI_IO<2>
(STRAP TO PCH)
PLACE_NEAR=U0500.AW2:10MM
NO_XNET_CONNECTION=1
PULL STRAP LOW WHEN XDP IS PLUGGED IN.
(UNDOCUMENTED STRAP FUNCTION)
XDP:YES R1850 100K
XDP_PRESENT_L
NEED TO CONNECT TO VCCST, *STG POWER LOGIC



PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.



PCH/XDP Signals
Non-XDP Signals
XDP_JTAG_ISP_TCK
XDP_JTAG_ISP_TDI
MAKE_BASE=TRUE
XDP_PCH_OBSDATA_A2 TP1870
XDP_PCH_OBSDATA_A3 TP1871
XDP_PCH_OBSDATA_B0 TP1872
XDP_PCH_OBSDATA_C0 TP1873
XDP_PCH_OBSDATA_C1 TP1874
XDP_PCH_OBSDATA_C2 TP1875
XDP_PCH_OBSDATA_C3 TP1876
XDP_PCH_OBSDATA_D0 TP1877
XDP_PCH_OBSDATA_D1 TP1878
XDP_PCH_OBSDATA_D2 TP1879
XDP_PCH_OBSDATA_D3 TP1880
XDP_PCH_OBSFN_C1 TP1881
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

BOM_COST_GROUP=DEBUG

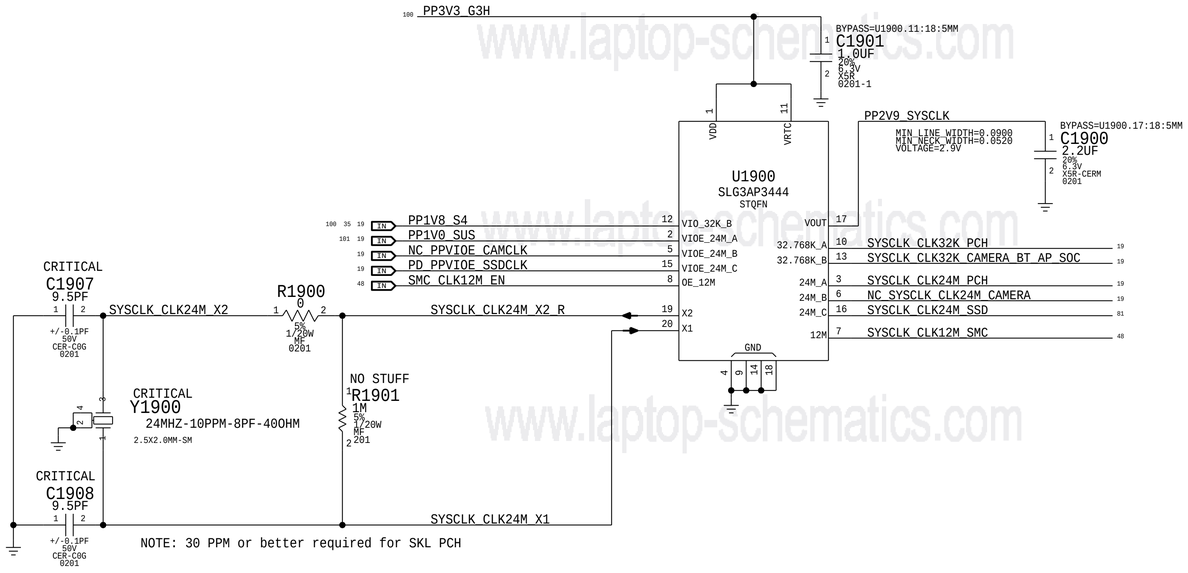
DESIGN: X502/MLB
LAST CHANGE: Thu Oct 22 19:53:09 2015

PAGE TITLE: CPU/PCH Merged XDP

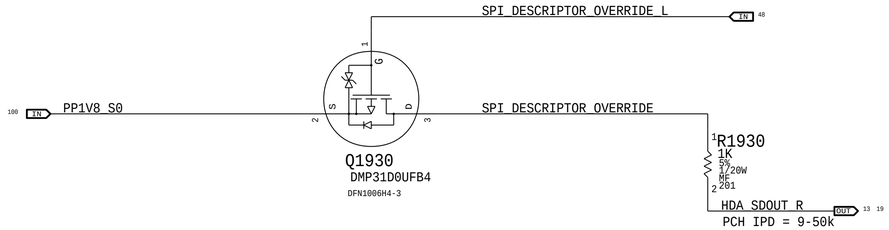
Apple Inc.

DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	18 OF 145
SHEET	17 OF 119

System 32kHz / 12MHz / 24MHz Clock Generator

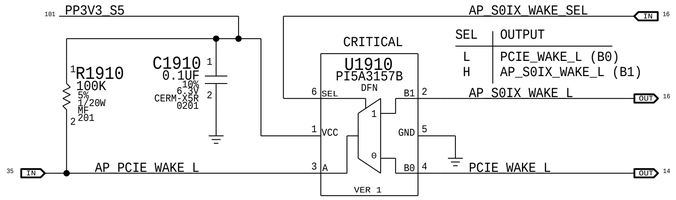


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: Chipset Support 1

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 19 OF 145
SHEET: 18 OF 119

Platform Reset Connections

Unbuffered

PLT_RST_L → R2000 100K → TBT_X_PCI_RESET_L → MAKE_BASE=TRUE TBT_X_PCI_RESET_L
R2001 100K → TBT_T_PCI_RESET_L → MAKE_BASE=TRUE TBT_T_PCI_RESET_L
R2002 100K → AP_RESET_L
R2003 100K → SSD_RESET_L
R2004 100K → SMC_LRESET_L

PCIE CLKREQS

PP3V3_S0

R2080 47K	SSD_CLKREQ_L	R2084 1K	SSD_CLKREQ_L_R	MAKE_BASE=TRUE SSD_CLKREQ_L_R
R2081 47K	TBT_X_CLKREQ_L	R2085 1K	TBT_X_CLKREQ_L_R	MAKE_BASE=TRUE TBT_X_CLKREQ_L_R
R2082 47K	TBT_T_CLKREQ_L	R2086 1K	TBT_T_CLKREQ_L_R	MAKE_BASE=TRUE TBT_T_CLKREQ_L_R
R2083 47K	AP_CLKREQ_L	R2087 1K	AP_CLKREQ_L_R	MAKE_BASE=TRUE AP_CLKREQ_L_R

ENABLE DDPB DDPC INTERFACES

PP3V3_S0
R2050 2.2K → PCH_DDPB_CTRLDATA
R2051 2.2K → PCH_DDPC_CTRLDATA

CATERR PU

PP1V0_S3
R2059 51 → CPU_CATERR_L

WIFI GPIO PD

R2058 100K → PCH_BT_ROM_BOOT

T208 PCH GPIO PUs/PDs & ALIASES

PP1V8_SUS

R2054 100K	SOC_PANIC_L	
R2055 100K	SOC_S2R_ACK_L	
R2056 100K	SOC_PCH_DBELL_L	MAKE_BASE=TRUE SOC_PCH_DBELL_L
	PCH_SOC_DBELL	MAKE_BASE=TRUE PCH_SOC_DBELL
	SOC_SWD_CLK	MAKE_BASE=TRUE SOC_SWD_CLK
R2053 100K	PCH_SOC_DFU_STATUS	
	SOC_TO_STOCKHOLM_EN	

NOSTUFF C2050 100PF 5% 25V C0G 0201

Desense Decoupling Caps on HDA Lines

HDA_SYNC_R	NOSTUFF C2020 3.0PF ±0.1PF 25V NP0-C0G 0201	
HDA_SDOUT_R	NOSTUFF C2021 3.0PF ±0.1PF 25V NP0-C0G 0201	
HDA_RST_R_L	NOSTUFF C2022 3.0PF ±0.1PF 25V NP0-C0G 0201	

Power State Debug LEDs

(For development only)

PP3V3_S5 → R2090 20K DBGLED → DBGLED_S5 → D2090 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM SILK_PART=S5_ON) → DBGLED_S4_D → Q2090 DMN5L06VK-7 SOT563 VER 3 → PM_SLP_S5_L
R2091 20K DBGLED → DBGLED_S4 → D2091 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM SILK_PART=STBY_ON) → DBGLED_S4_D → Q2090 DMN5L06VK-7 SOT563 VER 3 → PM_SLP_S4_L
R2092 20K DBGLED → DBGLED_S3 → D2092 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM SILK_PART=S3_ON) → DBGLED_S3_D → Q2090 DMN5L06VK-7 SOT563 VER 3 → PM_SLP_S3_L
R2093 20K DBGLED → DBGLED_S0I3 → D2093 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM SILK_PART=S0I3_ON) → DBGLED_S0I3_D → Q2091 DMN5L06VK-7 SOT563 VER 3 → PM_SLP_S3_L
R2095 20K DBGLED → DBGLED_S0 → D2095 GRN-90MCD-5MA-2.85V 0402 (PLACE_SIDE=BOTTOM SILK_PART=S0_ON) → DBGLED_S0_D → Q2091 DMN5L06VK-7 SOT563 VER 3 → PM_SLP_S0_L

GREENCLK VIOEs

NO_TEST=1 MAKE_BASE=TRUE NC_PPVIOE_CAMCLK → NC_PPVIOE_CAMCLK
PP1V0_SUS
PP1V8_S4
MAKE_BASE=TRUE PP1V8_SSD_COLD → R2010 0 → PD_PPVIOE_SSDCLK
NOSTUFF C2002 0.1UF 10% 6.3V CERM-X5R 0201
C2001 0.1UF 10% 6.3V CERM-X5R 0201
C2000 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U1900.02:18:5MM
BYPASS=U1900.12:18:5MM
BYPASS=U1900.15:18:5MM

GREENCLK CLOCK OUT ALIASES

MAKE_BASE=TRUE SYSCLK_CLK32K_PCH → SYSCLK_CLK32K_PCH
NC_PCH_CLK32K_RTCX2 → NC_PCH_CLK32K_RTCX2
MAKE_BASE=TRUE NO_TEST=1

PCH_CLK:GRNCLK
SYSCLK_CLK24M_PCH → R2024 0 → PCH_CLK24M_XTALIN
PLACE_NEAR=U1900.3:5MM

MAKE_BASE=TRUE SYSCLK_CLK32K_CAMERA_BT_AP_SOC → NOSTUFF R2042 0 → SYSCLK_CLK32K_WIFIBT
SYSCLK_CLK32K_CAMERA_BT_AP_SOC
R2043 0 → SOC_PMU_CLK_32K
NOSTUFF R2044 0
SYSCLK_CLK32K_OSC_OUT

x100 I2S Level Translator

PP1V8_S0 → C2010 0.1UF 10% 6.3V CERM-X5R 0201
PP3V3_S0 → C2011 0.1UF 10% 6.3V CERM-X5R 0201
U2010 NLSX5014MU_G UQFN (VCC, EN, IOLV[1], IOLV[2], IOLV[3], IOLV[4], GND, IOVCC[1], IOVCC[2], IOVCC[3], IOVCC[4])

BT_I2S_SYNC_1V8	MAKE_BASE=TRUE BT_I2S_SYNC_1V8	BT_I2S_SYNC	BT
BT_I2S_R2D_1V8	MAKE_BASE=TRUE BT_I2S_R2D_1V8	BT_I2S_R2D	OUT
BT_I2S_D2R_1V8	MAKE_BASE=TRUE BT_I2S_D2R_1V8	BT_I2S_D2R	IN
BT_I2S_CLK_1V8	MAKE_BASE=TRUE BT_I2S_CLK_1V8	BT_I2S_CLK	BI

BT/SSD DEBUG UART MUX

PP3V3_S0
PP1V8_S0
C2060 0.1UF 10% 6.3V CERM-X5R 0201
R2060 100K 5% 1/20W MF 201
R2061 100K 5% 1/20W MF 201
R2062 100K 5% 1/20W MF 201
R2063 100K 5% 1/20W MF 201

MAKE_BASE=TRUE PCH_SSD_SOC_UART_D2R → PCH_SSD_SOC_UART_D2R
PCH_SSD_SOC_UART_R2D → PCH_SSD_SOC_UART_R2D
U2060 CRITICAL PI3USB102EZLE TQFN (VCC, Y+, Y-, M+, M-, D+, D-, SEL, OE*, GND)
SSD_DBG_UART_D2R
SSD_DBG_UART_R2D_R
SOC_DBG_UART_D2R
SOC_DBG_UART_R2D
R2066 100K 5% 1/20W MF 201 → DEBUGUART_SEL_SOC
NO STUFF R2067 0 5% 1/20W MF 0201
NO STUFF R2068 0 5% 1/20W MF 0201

BOM_COST_GROUP=CPU & CHIPSET

Voltage Props

VOLTAGE=1.0V PP1V_SUS_PCH_VCCCLK2_F
PP1V_SUS_PCH_VCCCLK4_F
PP1V_SUS_PCH_VCCCLK5_F
PP1V_S5_PCH_DCPDSW
PP1V_SUS_PCH_VCCAPLL_F
VOLTAGE=1.8V PP1V_SUSSW_PCH_VCCAMPHYPLL_F
VOLTAGE=1.0V PP1V8_SUS_PCH_VCC1P8
VOLTAGE=3.0V PP1V8_S0_PCH_VCCHDA_F
PPDCPRTC_PCH

NO TEST

NC_USB2_10N NO_TEST=1
NC_USB2_10P NO_TEST=1
NC_USB2_05N NO_TEST=1
NC_USB2_05P NO_TEST=1

Unused GPIOs with PUs/PDs

PD_AP_DEV_WAKE	MAKE_BASE=TRUE	PD_AP_DEV_WAKE
PU_AUD_SPI_CS_L	MAKE_BASE=TRUE	PU_AUD_SPI_CS_L
PD_AUD_SPI_CLK	MAKE_BASE=TRUE	PD_AUD_SPI_CLK
PD_AUD_SPI_MISO	MAKE_BASE=TRUE	PD_AUD_SPI_MISO
PU_AUD_SPI_MOSI	MAKE_BASE=TRUE	PU_AUD_SPI_MOSI
PD_LCD_PSR_EN	MAKE_BASE=TRUE	PD_LCD_PSR_EN
PD_SSD_UART_CTS_L	MAKE_BASE=TRUE	PD_SSD_UART_CTS_L
PU_SOC_UART_RTS_L	MAKE_BASE=TRUE	PU_SOC_UART_RTS_L
PD_SOC_UART_CTS_L	MAKE_BASE=TRUE	PD_SOC_UART_CTS_L

SIGNAL ALIASES

PD_PPVIOE_SSDCLK	MAKE_BASE=TRUE	PD_PPVIOE_SSDCLK
CAMERA_PWR_EN	MAKE_BASE=TRUE	CAMERA_PWR_EN
ALS_SOC_UART_D2R	MAKE_BASE=TRUE	ALS_SOC_UART_D2R
ALS_SOC_UART_R2D	MAKE_BASE=TRUE	ALS_SOC_UART_R2D

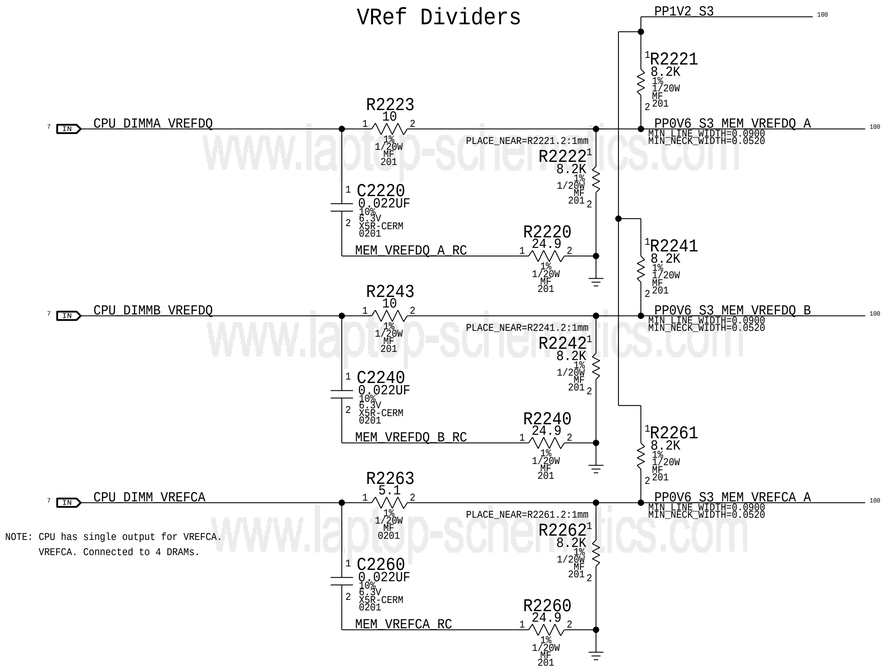
NC SIGNAL ALIASES

NC_PCH_CLKREQ4_L	MAKE_BASE=TRUE	NC_PCH_CLKREQ4_L
NC_PCIE_CLK100M5N	MAKE_BASE=TRUE NO_TEST=1	NC_PCIE_CLK100M5N
NC_PCIE_CLK100M5P	MAKE_BASE=TRUE NO_TEST=1	NC_PCIE_CLK100M5P
NC_PCH_CLKREQ5_L	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_CLKREQ5_L
NC_SPKR_ID1	MAKE_BASE=TRUE NO_TEST=1	NC_SPKR_ID1
NC_PCH_CLK24M_XTALOUT	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_CLK24M_XTALOUT
NC_PCH_GPP_E15	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_GPP_E15
NC_PCH_BSSB_CLK	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_BSSB_CLK
NC_PCH_BSSB_DATA	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_BSSB_DATA
NC_ITPXDP_CLK100M_N	MAKE_BASE=TRUE NO_TEST=1	NC_ITPXDP_CLK100M_N
NC_ITPXDP_CLK100M_P	MAKE_BASE=TRUE NO_TEST=1	NC_ITPXDP_CLK100M_P
NC_UPC_I2C_INT_L	MAKE_BASE=TRUE NO_TEST=1	NC_UPC_I2C_INT_L
NC_SPKR_ID0	MAKE_BASE=TRUE NO_TEST=1	NC_SPKR_ID0
NC_USB3_04_D2RN	MAKE_BASE=TRUE NO_TEST=1	NC_USB3_04_D2RN
NC_USB3_04_D2RP	MAKE_BASE=TRUE NO_TEST=1	NC_USB3_04_D2RP
NC_USB3_04_R2DN	MAKE_BASE=TRUE NO_TEST=1	NC_USB3_04_R2DN
NC_USB3_04_R2DP	MAKE_BASE=TRUE NO_TEST=1	NC_USB3_04_R2DP
NC_I2C_UPC_SDA	MAKE_BASE=TRUE NO_TEST=1	NC_I2C_UPC_SDA
NC_I2C_UPC_SCL	MAKE_BASE=TRUE NO_TEST=1	NC_I2C_UPC_SCL
NC_MLB_DEV_L	MAKE_BASE=TRUE NO_TEST=1	NC_MLB_DEV_L
NC_SYSCLK_CLK24M_CAMERA	NO_TEST=1	NC_SYSCLK_CLK24M_CAMERA
NC_PCH_STRP_TLSCONF	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_STRP_TLSCONF
NC_PCH_STRP_ESPI	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_STRP_ESPI
NC_PCH_STRP_BSSB_SEL_GPIO	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_STRP_BSSB_SEL_GPIO
NC_PCH_CLKOUT_LPC1	MAKE_BASE=TRUE NO_TEST=1	NC_PCH_CLKOUT_LPC1
NC_VCCPRIM_CORE_VID0	MAKE_BASE=TRUE NO_TEST=1	NC_VCCPRIM_CORE_VID0
NC_VCCPRIM_CORE_VID1	MAKE_BASE=TRUE NO_TEST=1	NC_VCCPRIM_CORE_VID1
NC_CAMERA_RESET_L	MAKE_BASE=TRUE NO_TEST=1	NC_CAMERA_RESET_L

PAGE TITLE	Chipset Support 2
Apple Inc.	
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	20 OF 145
SHEET	19 OF 119

CPU-Based Margining

VRef Dividers



NOTE: CPU has single output for VREFCA.
VREFCA. Connected to 4 DRAMs.

BOM_COST_GROUP=CPU & CHIPSET

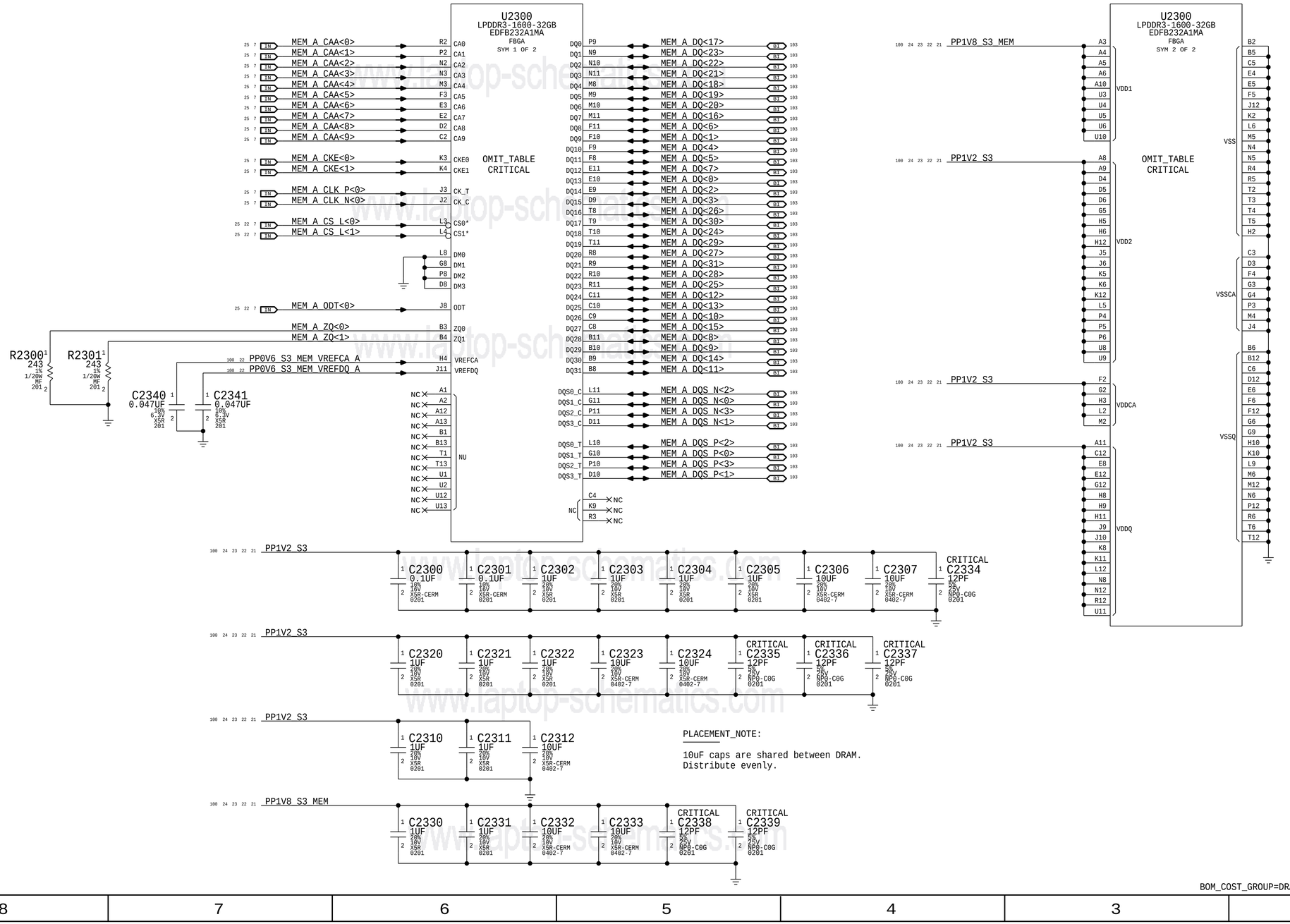
SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE: LPDDR3 VREF Margining

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 22 OF 145
SHEET: 20 OF 119

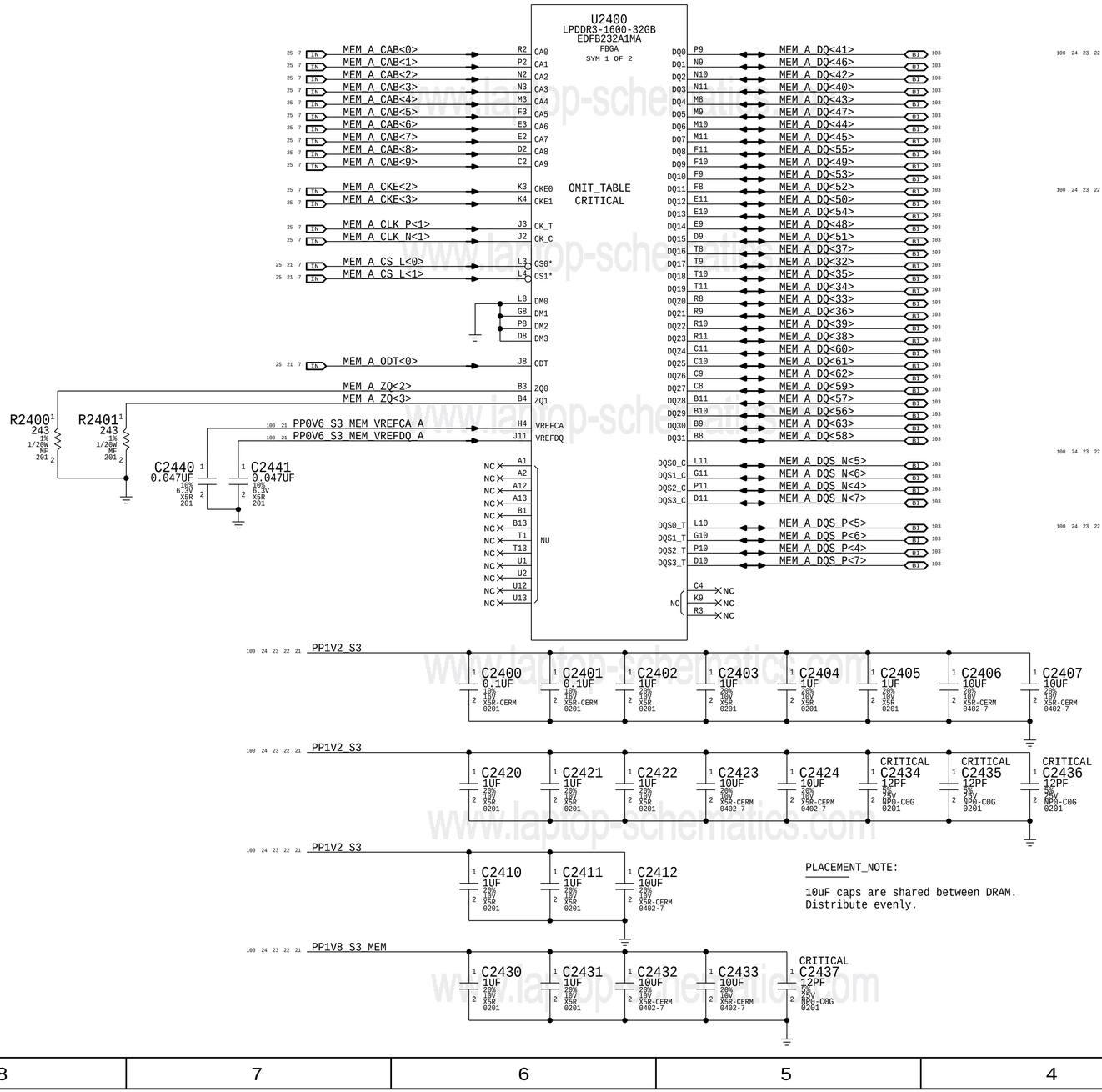
LPDDR3 CHANNEL A (0-31)



BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB	SYNC_DATE=05/12/2015
PAGE TITLE	LPDDR3 DRAM Channel A (00-31)
Apple Inc.	DRAWING NUMBER 051-00777 / SIZE D
	REVISION 9.0.0
	BRANCH dvt-fab09-0
	PAGE 23 OF 145
	SHEET 21 OF 119

LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

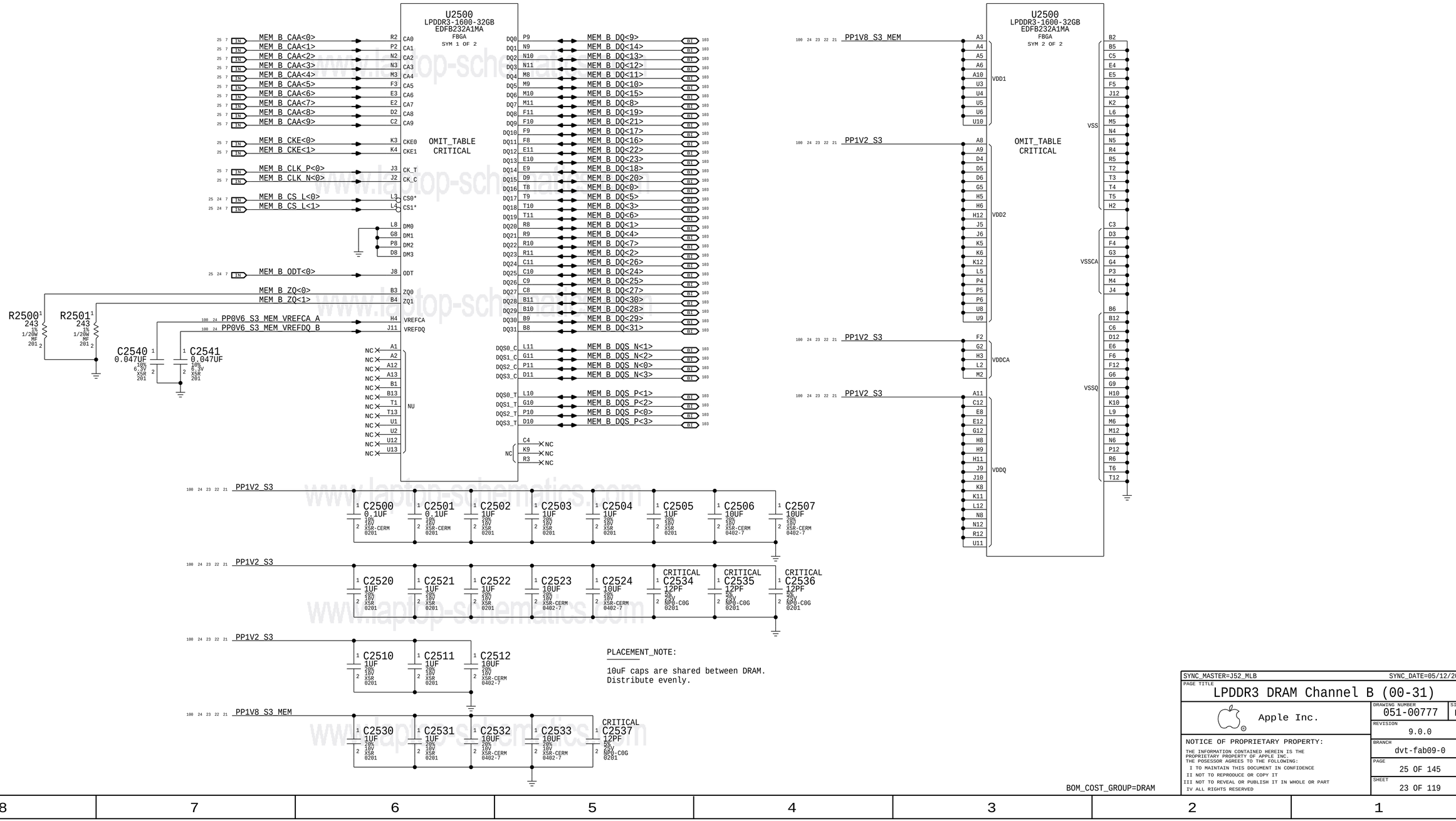
10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

Vinafix

SYNC_MASTER=J52_MLB	SYNC_DATE=05/12/2015
PAGE TITLE	LPDDR3 DRAM Channel A (32-63)
Apple Inc.	DRAWING NUMBER 051-00777 / SIZE D
	REVISION 9.0.0
	BRANCH dvt-fab09-0
	PAGE 24 OF 145
	SHEET 22 OF 119

LPDDR3 CHANNEL B (0-31)



BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE: LPDDR3 DRAM Channel B (00-31)

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D

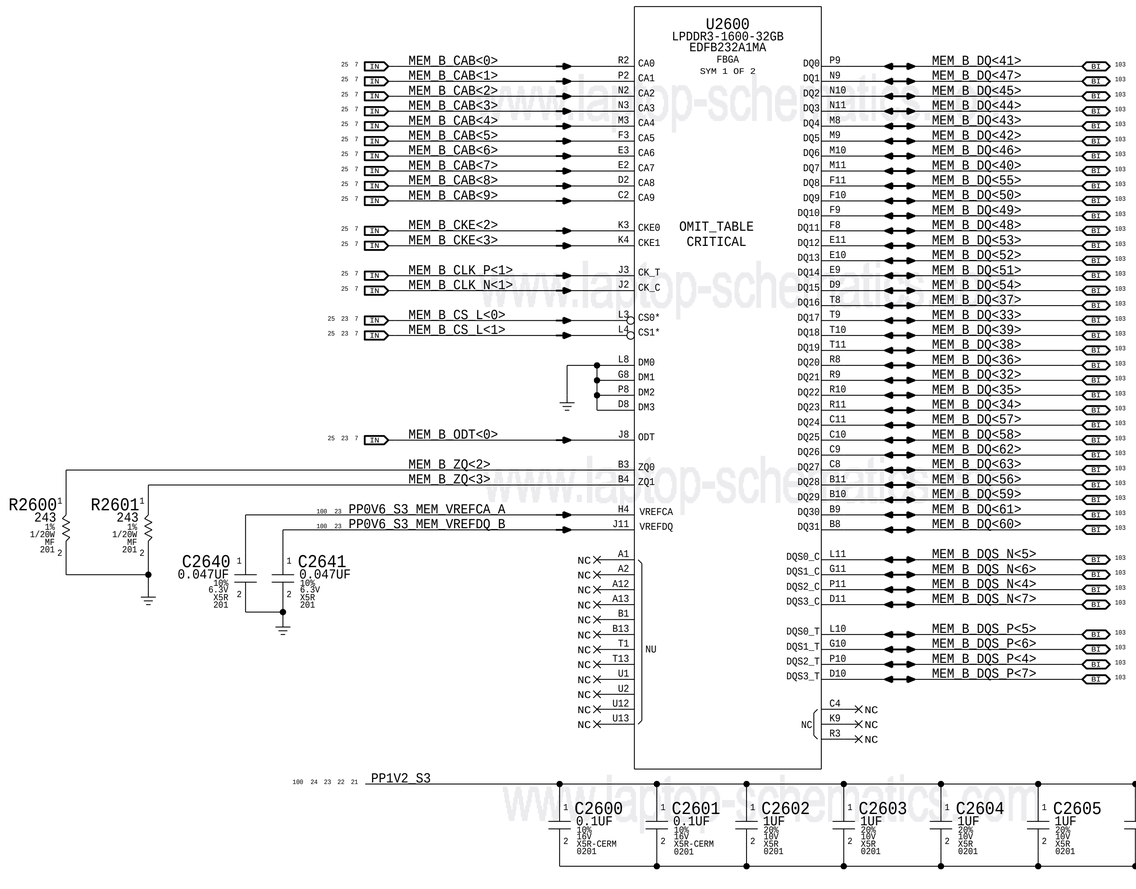
REVISION: 9.0.0

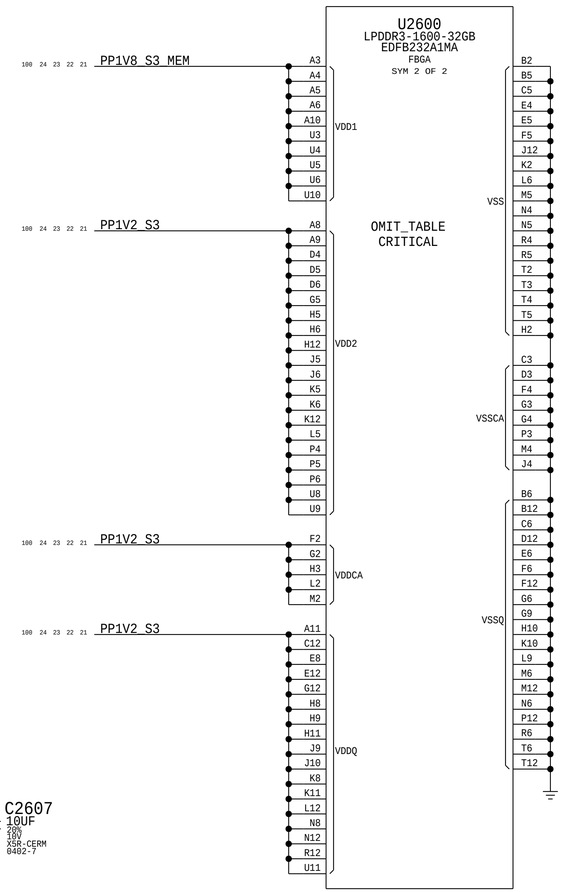
BRANCH: dvt-fab09-0

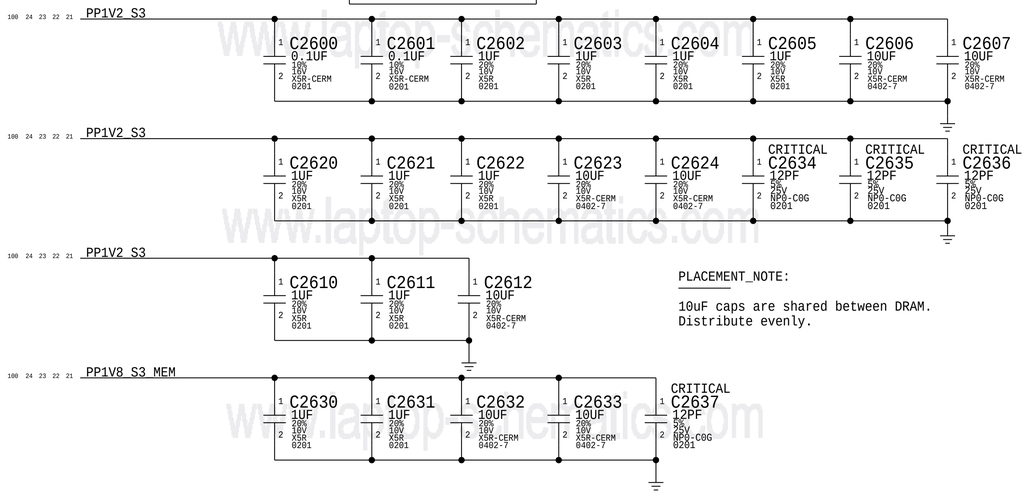
PAGE: 25 OF 145

SHEET: 23 OF 119

LPDDR3 CHANNEL B (32-63)







PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

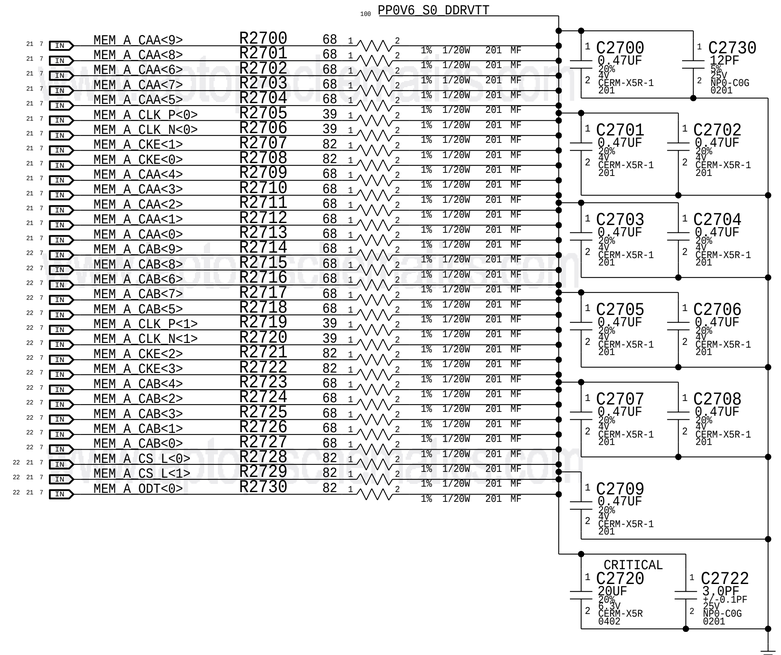
SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

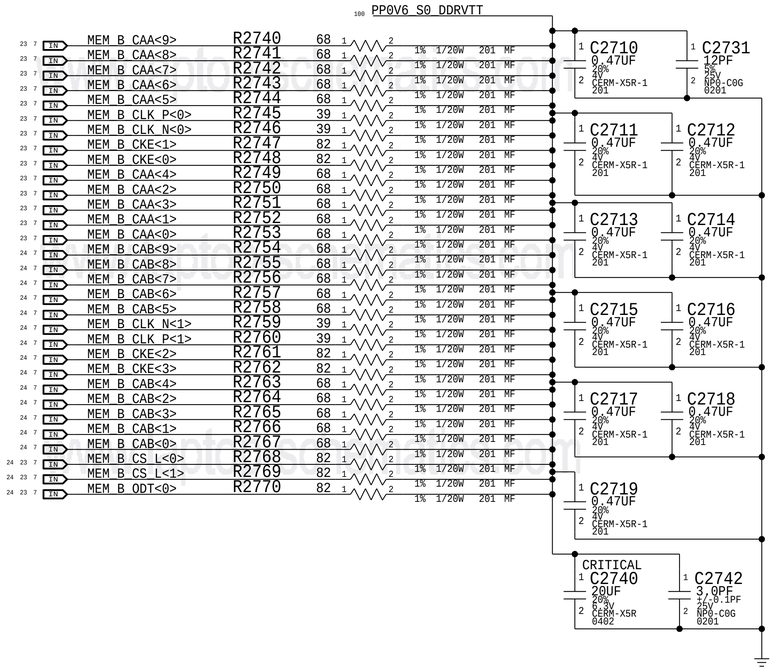
PAGE TITLE: LPDDR3 DRAM Channel B (32-63)

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 26 OF 145
SHEET: 24 OF 119

Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





BOM_COST_GROUP=DRAM

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE: LPDDR3 DRAM Termination

Apple Inc.

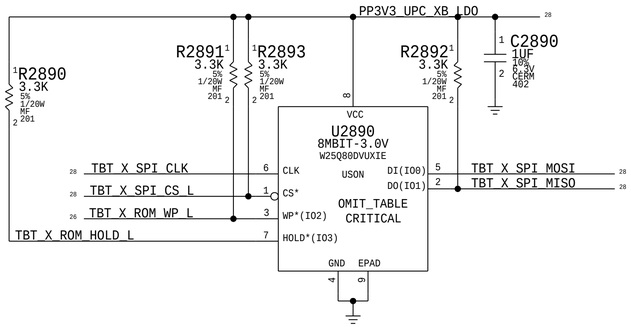
DRAWING NUMBER: 051-00777 SIZE: D

REVISION: 9.0.0

BRANCH: dvt-fab09-0

PAGE: 27 OF 145

SHEET: 25 OF 119

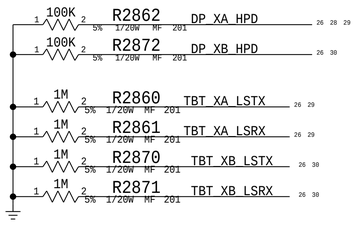


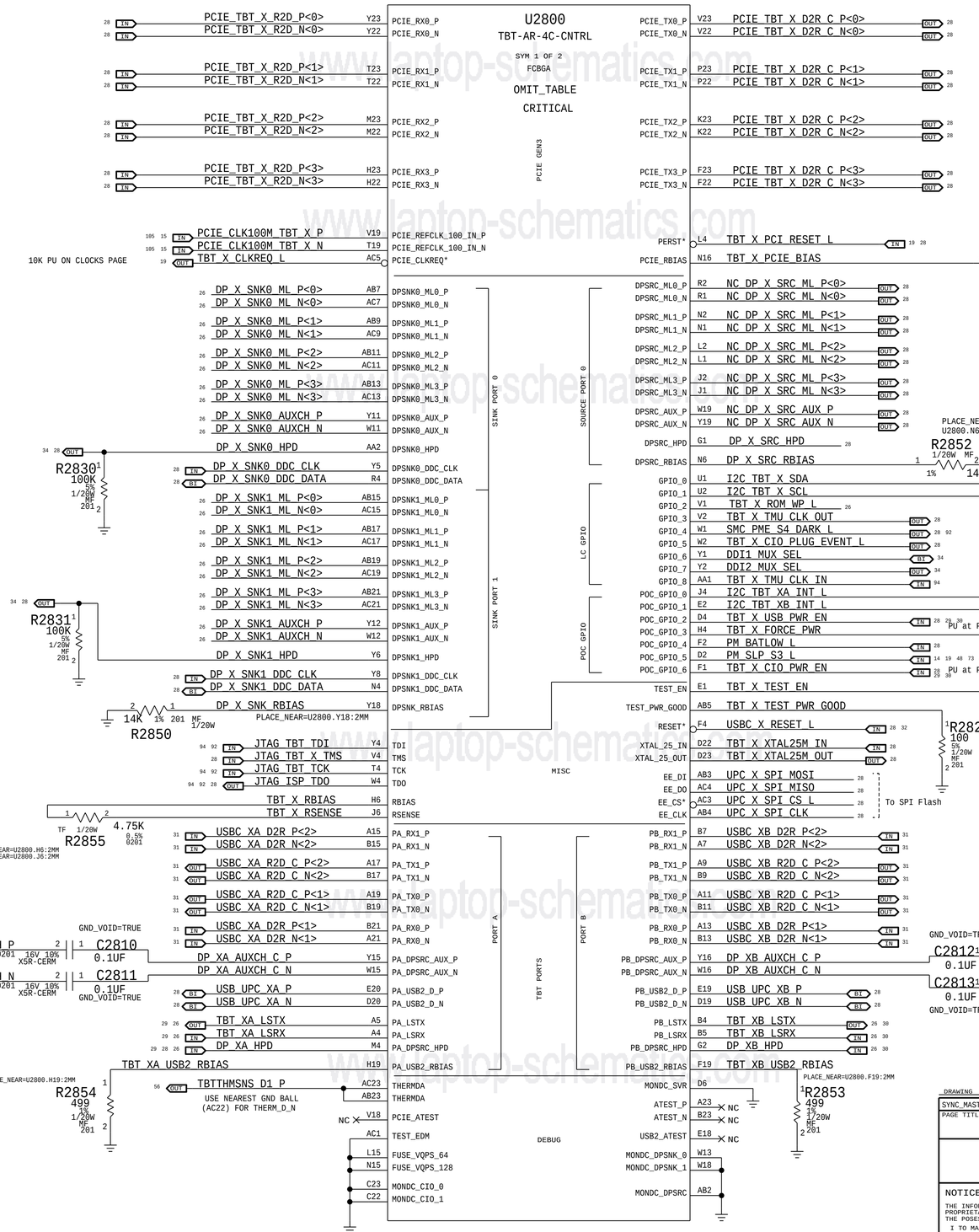
SNK0 AC Coupling

DP_X_SNK0_ML_C_P<0>	C2820	0.1UF	DP_X_SNK0_ML_P<0>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<0>	C2821	0.1UF	DP_X_SNK0_ML_N<0>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<1>	C2822	0.1UF	DP_X_SNK0_ML_P<1>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<1>	C2823	0.1UF	DP_X_SNK0_ML_N<1>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<2>	C2824	0.1UF	DP_X_SNK0_ML_P<2>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<2>	C2825	0.1UF	DP_X_SNK0_ML_N<2>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<3>	C2826	0.1UF	DP_X_SNK0_ML_P<3>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<3>	C2827	0.1UF	DP_X_SNK0_ML_N<3>	GND_VOID=TRUE
DP_X_SNK0_AUXCH_C_P	C2828	0.1UF	DP_X_SNK0_AUXCH_P	GND_VOID=TRUE
DP_X_SNK0_AUXCH_C_N	C2829	0.1UF	DP_X_SNK0_AUXCH_N	

SNK1 AC Coupling

DP_X_SNK1_ML_C_P<0>	C2830	0.1UF	DP_X_SNK1_ML_P<0>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<0>	C2831	0.1UF	DP_X_SNK1_ML_N<0>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<1>	C2832	0.1UF	DP_X_SNK1_ML_P<1>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<1>	C2833	0.1UF	DP_X_SNK1_ML_N<1>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<2>	C2834	0.1UF	DP_X_SNK1_ML_P<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<2>	C2835	0.1UF	DP_X_SNK1_ML_N<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<3>	C2836	0.1UF	DP_X_SNK1_ML_P<3>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<3>	C2837	0.1UF	DP_X_SNK1_ML_N<3>	GND_VOID=TRUE
DP_X_SNK1_AUXCH_C_P	C2838	0.1UF	DP_X_SNK1_AUXCH_P	GND_VOID=TRUE
DP_X_SNK1_AUXCH_C_N	C2839	0.1UF	DP_X_SNK1_AUXCH_N	





BOM_COST_GROUP=TBT

DRAWING	LAST_MODIFIED=Tue Aug 30 11:06:20 2016
SYNC_MASTER=J79_GREG	SYNC_DATE=07/27/2015
PAGE TITLE	USB-C HIGH SPEED 1
Apple Inc.	DRAWING NUMBER 051-00777 · SIZE D
	REVISION 9.0.0
	BRANCH dvt-fab09-0
	PAGE 28 OF 145
	SHEET 26 OF 119

U2800
TBT-AR-4C-CNTRL
SYM 2 OF 2
FCBGA
OMIT_TABLE
CRITICAL

SOURCED BY INTERNAL SWITCH
PP0V9_TBT_X_DP
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.9V

C2930 1.0UF 20% 6.3V X5R 0201-1
C2931 1.0UF 20% 6.3V X5R 0201-1
C2932 1.0UF 20% 6.3V X5R 0201-1
C2933 1.0UF 20% 6.3V X5R 0201-1
C2934 1.0UF 20% 6.3V X5R 0201-1
C2935 1.0UF 20% 6.3V X5R 0201-1
C2936 1.0UF 20% 6.3V X5R 0201-1

SOURCED BY INTERNAL SWITCH
28 PP0V9_TBT_X_PCIE
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.9V

C2964 1.0UF 20% 6.3V X5R 0201-1
C2965 1.0UF 20% 6.3V X5R 0201-1
C2966 1.0UF 20% 6.3V X5R 0201-1
C2967 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.9V
SOURCED BY INTERNAL SWITCH
28 PP0V9_TBT_X_USB

C2984 1.0UF 20% 6.3V X5R 0201-1
C2985 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.9V
SOURCED BY INTERNAL SWITCH
28 PP0V9_TBT_X_CIO

C2945 1.0UF 20% 6.3V X5R 0201-1
C2946 1.0UF 20% 6.3V X5R 0201-1
C2947 1.0UF 20% 6.3V X5R 0201-1

SOURCED BY INTERNAL SWITCH
PP3V3_TBT_X_ANA_PCIE
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
PP3V3_TBT_X_ANA_USB2
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V

C2920 1.0UF 20% 6.3V X5R 0201-1
C2921 1.0UF 20% 6.3V X5R 0201-1
SOURCED BY INTERNAL SWITCH

L8	VCC0P9_DP	VCC3P3_LC	R6
L11	VCC0P9_DP	VCC3P3_SX	F8
L12	VCC0P9_DP	VCC3P3_S0	R13
M8	VCC0P9_DP	VCC3P3A	H9
T11	VCC0P9_DP	VCC3P3_SVR	A2
T12	VCC0P9_DP	VCC3P3_SVR	A3
L6	VCC0P9_ANA_DPSRC	VCC3P3_SVR	B3
M6	VCC0P9_ANA_DPSRC	VCC0P9_SVR	L9
V11	VCC0P9_ANA_DPSNK	VCC0P9_SVR	M9
V12	VCC0P9_ANA_DPSNK	VCC0P9_SVR_ANA	E12
V13	VCC0P9_ANA_DPSNK	VCC0P9_SVR_ANA	E13
M13	VCC0P9_PCIE	VCC0P9_SVR_ANA	F11
M15	VCC0P9_PCIE	VCC0P9_SVR_ANA	F12
M16	VCC0P9_PCIE	VCC0P9_SVR_ANA	F13
L19	VCC0P9_ANA_PCIE_1	VCC0P9_SVR_ANA	F15
N19	VCC0P9_ANA_PCIE_1	VCC0P9_SVR_SENSE	J9
L18	VCC0P9_ANA_PCIE_2	SVR_IND	C1
M18	VCC0P9_ANA_PCIE_2	SVR_IND	C2
N18	VCC0P9_ANA_PCIE_2	SVR_IND	D1
R15	VCC0P9_USB	SVR_VSS	A1
R16	VCC0P9_USB	SVR_VSS	B1
R8	VCC0P9_CIO	SVR_VSS	B2
R9	VCC0P9_CIO	VCC0P9_LVR	F18
R11	VCC0P9_CIO	VCC0P9_LVR	H18
R12	VCC0P9_CIO	VCC0P9_LVR	J11
L16	VCC3P3_ANA_PCIE	VCC0P9_LVR_SENSE	H11
J16	VCC3P3_ANA_USB2		
A6	VSS_ANA	VSS_ANA	R23
A8	VSS_ANA	VSS_ANA	T1
A10	VSS_ANA	VSS_ANA	T2
A12	VSS_ANA	VSS_ANA	T5
A14	VSS_ANA	VSS_ANA	T20
A16	VSS_ANA	VSS_ANA	U23
A18	VSS_ANA	VSS_ANA	U22
A20	VSS_ANA	VSS_ANA	V5
A22	VSS_ANA	VSS_ANA	V6
B6	VSS_ANA	VSS_ANA	V8
B8	VSS_ANA	VSS_ANA	V9
B10	VSS_ANA	VSS_ANA	V15
B12	VSS_ANA	VSS_ANA	V16
B14	VSS_ANA	VSS_ANA	V20
B16	VSS_ANA	VSS_ANA	W5
B18	VSS_ANA	VSS_ANA	W6
B20	VSS_ANA	VSS_ANA	W8
B22	VSS_ANA	VSS_ANA	W9
D8	VSS_ANA	VSS_ANA	W20
D9	VSS_ANA	VSS_ANA	W22
D11	VSS_ANA	VSS_ANA	W23
D12	VSS_ANA	VSS_ANA	Y9
D13	VSS_ANA	VSS_ANA	Y13
D15	VSS_ANA	VSS_ANA	Y20
D16	VSS_ANA	VSS_ANA	AA22
D18	VSS_ANA	VSS_ANA	AA23
E8	VSS_ANA	VSS_ANA	AB6
E9	VSS_ANA	VSS_ANA	AB8
E11	VSS_ANA	VSS_ANA	AB10
E15	VSS_ANA	VSS_ANA	AB12
E16	VSS_ANA	VSS_ANA	AB14
E22	VSS_ANA	VSS_ANA	AB16
E23	VSS_ANA	VSS_ANA	AB18
F9	VSS_ANA	VSS_ANA	AB20
F20	VSS_ANA	VSS_ANA	AB22
F16	VSS_ANA	VSS_ANA	AC6
G22	VSS_ANA	VSS_ANA	AC8
G23	VSS_ANA	VSS_ANA	AC10
H1	VSS_ANA	VSS_ANA	AC12
H2	VSS_ANA	VSS_ANA	AC14
H12	VSS_ANA	VSS_ANA	AC16
H13	VSS_ANA	VSS_ANA	AC18
H15	VSS_ANA	VSS_ANA	AC20
H16	VSS_ANA	VSS_ANA	AC22
H20	VSS_ANA	VSS	D5
J5	VSS_ANA	VSS	E4
J19	VSS_ANA	VSS	E5
J20	VSS_ANA	VSS	E6
J18	VSS_ANA	VSS	F5
J22	VSS_ANA	VSS	F6
J23	VSS_ANA	VSS	H5
K1	VSS_ANA	VSS	H8
K2	VSS_ANA	VSS	J8
L5	VSS_ANA	VSS	J12
L20	VSS_ANA	VSS	J13
L22	VSS_ANA	VSS	J15
L23	VSS_ANA	VSS	L13
M1	VSS_ANA	VSS	M12
M2	VSS_ANA	VSS	N8
M5	VSS_ANA	VSS	N9
M19	VSS_ANA	VSS	N11
M20	VSS_ANA	VSS	N12
N5	VSS_ANA	VSS	N13
N20	VSS_ANA	VSS	T6
N22	VSS_ANA	VSS	T8
N23	VSS_ANA	VSS	T9
P1	VSS_ANA	VSS	T13
P2	VSS_ANA	VSS	T15
R5	VSS_ANA	VSS	T16
R18	VSS_ANA	VSS	T18
R19	VSS_ANA	VSS	AB1
R20	VSS_ANA	VSS	AC2
R22	VSS_ANA	VSS	M11

VCC
GND

PP3V3_TBT_X_LC
PP3V3_TBT_X_SW
PP3V3_TBT_X_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520

C2991 1.0UF 20% 6.3V X5R 0201-1

C2990 1.0UF 20% 6.3V X5R 0201-1
C2994 47UF 20% 6.3V CER-X5R 0603
C2995 47UF 20% 6.3V CER-X5R 0603

L2990
1.0UH-20%-2.1A-0.128OHM
CRITICAL
0603

28 32 FROM USB-C PORT CONTROLLER (UPC)

C2981 1.0UF 20% 6.3V X5R 0201-1

28 C2980 0.1UF 10% 16V X5R-CERM 0201

SOURCED BY INTERNAL SWITCH
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V

PP3V3_TBT_X_S0
28 101

C2975 10UF 20% 6.3V X5R-CERM 0402-4
C2976 10UF 20% 6.3V X5R-CERM 0402-4
C2977 10UF 20% 6.3V X5R-CERM 0402-4
C2978 10UF 20% 6.3V X5R-CERM 0402-4
BYPASS=U2800.A2:A1:3MM

PP0V9_TBT_X_SVR
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.9V

C2917 12PF 5% 25V NP0-C0G 0201
C2910 1.0UF 20% 6.3V X5R 0201-1
C2911 1.0UF 20% 6.3V X5R 0201-1
C2912 1.0UF 20% 6.3V X5R 0201-1
C2913 1.0UF 20% 6.3V X5R 0201-1
C2914 1.0UF 20% 6.3V X5R 0201-1
C2915 1.0UF 20% 6.3V X5R 0201-1
C2916 1.0UF 20% 6.3V X5R 0201-1

CRITICAL
L2950
0.68UH-20%-6.1A-0.020OHM
1210
DIDT=TRUE
SWITCH_NODE=TRUE
VR0V9_IND_TBT_X

C2950 47UF 20% 6.3V CER-X5R 0603
C2951 47UF 20% 6.3V CER-X5R 0603
C2952 47UF 20% 6.3V CER-X5R 0603
INTERNAL SWITCHING VR OUTPUT

PP0V9_TBT_X_LVR
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.9V

SOURCED BY INTERNAL SWITCH

C2992 1.0UF 20% 6.3V X5R 0201-1
C2993 1.0UF 20% 6.3V X5R 0201-1
C2954 10UF 20% 6.3V CERM-X5R 0402-4
C2955 10UF 20% 6.3V CERM-X5R 0402-4
2x 10uF outside BGA area

Add XW or alias on support page
XW
28

P0V9_TBT_X_SVR_AGND
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0V

ISOLATE GND OF SVR_IND CAPS
AND GND OF VCC3P3_SVR CAPS
FROM SYSTEM GND IN LAYOUT
(SEE INTEL LAYOUT GUIDELINES)

XW2900
SM
1 2
TBTTHMSNS_D1_N
OUT 56
PLACE_NEAR=U2800.AC22:2MM
NO_XNET_CONNECTION=1

BOM_COST_GROUP=TBT

SYNC_MASTER=J79_GREG SYNC_DATE=09/09/2015
PAGE TITLE
USB-C HIGH SPEED 2

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 29 OF 145
SHEET 27 OF 119

TMU CLKs

TBT_X_TMU_CLK_OUT (MAKE_BASE=TRUE) — R3025 15 5% 1/20W MF 201 (PLACE_NEAR=U2800.V2:5mm) — TBT_T_TMU_CLK_IN (MAKE_BASE=TRUE)

TBT_X_TMU_CLK_OUT — TBT_T_TMU_CLK_IN

R3024 100K 5% 1/20W MF 201

Ridge 0.9V SVR XW

P0V9_TBT_X_SVR_AGND — XW3000 SHORT-L6-SM (NO_XNET_CONNECTION=1)

DP SRC OPTIONS

IF DP SRC NOT USED

DP_X_SRC_HPD — R3040 1M 5% 1/20W MF 201

NC_DP_X_SRC_ML_P<0>	NC_DP_X_SRC_ML_P<0>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_ML_P<1>	NC_DP_X_SRC_ML_P<1>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_ML_P<2>	NC_DP_X_SRC_ML_P<2>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_ML_P<3>	NC_DP_X_SRC_ML_P<3>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_ML_N<0>	NC_DP_X_SRC_ML_N<0>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_ML_N<1>	NC_DP_X_SRC_ML_N<1>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_ML_N<2>	NC_DP_X_SRC_ML_N<2>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_ML_N<3>	NC_DP_X_SRC_ML_N<3>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_AUX_P	NC_DP_X_SRC_AUX_P	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_AUX_N	NC_DP_X_SRC_AUX_N	MAKE_BASE=TRUE, NO_TEST=1

AR xtal

TBT_X_XTAL25M_OUT — R3007 0 5% 1/20W MF 201 — TBT_X_XTAL25M_OUT_R

R3006 1M 5% 1/20W MF 201 (NOSTUFF)

Y3000 CRITICAL 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM

C3002 20PF 5% 25V C0G 0201

C3003 20PF 5% 25V C0G 0201

TBT_X_XTAL25M_IN

RIDGE DEBUG CONN

J3001 USBC_DBG 505070-1220 M-ST-SM

TBT_X_CIO_PLUG_EVENT_L	1	2	TBT_X_PCI_RESET_L
DP_X_SNK0_HPD	3	4	USBC_X_RESET_L
DP_X_SNK1_HPD	5	6	PP3V3_S5_TBT_X_SW
DP_XA_HPD	7	8	PP0V9_TBT_X_PCIE
TBT_POC_RESET	9	10	PP0V9_TBT_X_USB
PP3V3_TBT_X_LC	11	12	PP0V9_TBT_X_CIO
	15	16	

X ACE-SMC I2C SERIES R'S

I2C_UPC_X_SDA2 — R3041 33 5% 1/20W MF 201 (PLACE_NEAR=U5000:5mm) — SMBUS_SMC_4_G3H_SDA

I2C_UPC_X_SDA2 (MAKE_BASE=TRUE) — I2C_UPC_X_SDA2 — SMBUS_SMC_4_G3H_SDA

I2C_UPC_X_SCL2 — R3042 33 5% 1/20W MF 201 (PLACE_NEAR=U5000:5mm) — SMBUS_SMC_4_G3H_SCL

I2C_UPC_X_SCL2 (MAKE_BASE=TRUE) — I2C_UPC_X_SCL2 — SMBUS_SMC_4_G3H_SCL

ACE A/B RPD STRAPPING

USBC_XA_CC1	USBC_XA_CC1	MAKE_BASE=TRUE
USBC_XA_CC2	USBC_XA_CC2	MAKE_BASE=TRUE
USBC_XB_CC1	USBC_XB_CC1	MAKE_BASE=TRUE
USBC_XB_CC2	USBC_XB_CC2	MAKE_BASE=TRUE

ACE PDs

UPC_X_5V_EN — R3032 100K 5% 1/20W MF 201

ACE Debug Support

UPC_XA_DBG_UART_TX — R3089 NOSTUFF (OMIT) — UPC_XA_DBG_UART_RX

UPC_XB_DBG_UART_TX — R3088 NOSTUFF (OMIT) — UPC_XB_DBG_UART_RX

ACE DEBUG CONN

J3000 USBC_DBG 505070-1220 M-ST-SM

I2C_TBT_XB_INT_L	1	2	I2C_TBT_XA_INT_L
I2C_UPC_X_SCL2	3	4	I2C_TBT_X_SDA
I2C_UPC_X_SDA2	5	6	I2C_TBT_X_SCL
SMC_USBC_INT_L	7	8	I2C_UPC_XA_DBG_CTL_SDA
TBT_X_SPI_CLK_DBG	9	10	I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_UART_TX	11	12	UPC_XA_UART_RX
	15	16	

Ridge PDs

DP_X_SNK0_DDC_CLK	R3067 100K	DP_X_SNK0_DDC_CLK
DP_X_SNK0_DDC_DATA	R3068 100K	DP_X_SNK0_DDC_DATA
DP_X_SNK1_DDC_CLK	R3069 100K	DP_X_SNK1_DDC_CLK
DP_X_SNK1_DDC_DATA	R3070 100K	DP_X_SNK1_DDC_DATA

FUSES FOR UPC

PP20V_USBC_XA_VBUS — F3000 CRITICAL 0603 6AMP-32V-0.0095OHM (PLACE_NEAR=Q3100:5MM) — PP20V_USBC_XA_VBUS_F

PP20V_USBC_XB_VBUS — F3001 CRITICAL 0603 740S0135 6AMP-32V-0.0095OHM (PLACE_NEAR=Q3200:5MM) — PP20V_USBC_XB_VBUS_F

DCI ALIASES

DCI PCH USB3

USB3_EXTA_R2D_C_P — C3020 0.1UF 10% 16V X5R-CERM 0201

USB3_EXTA_R2D_C_N — C3021 0.1UF 10% 16V X5R-CERM 0201

USB3_EXTA_D2R_P	USB3_EXTA_D2R_P	MAKE_BASE=TRUE
USB3_EXTA_D2R_N	USB3_EXTA_D2R_N	MAKE_BASE=TRUE
USB3_EXTA_R2D_P	USB3_EXTA_R2D_P	MAKE_BASE=TRUE
USB3_EXTA_R2D_N	USB3_EXTA_R2D_N	MAKE_BASE=TRUE

DCI Ace

USB2 AR PDs

USB_UPC_XA_P	R3020 0	5% 1/20W MF 201
USB_UPC_XA_N	R3021 0	5% 1/20W MF 201
USB_UPC_XB_P	R3022 0	5% 1/20W MF 201
USB_UPC_XB_N	R3023 0	5% 1/20W MF 201

GND ALIASES

GND GND GND GND GND GND

GND GND GND GND GND GND

NC ALIASES / NO TEST

NO_TEST=1 NC_UPC_XB_I2C_ADDR

SIGNAL ALIASES

UPC_X_5V_EN	UPC_X_5V_EN	MAKE_BASE=TRUE
UPC_X_5V_EN		
TBT_X_CIO_PWR_EN	TBT_X_CIO_PWR_EN	MAKE_BASE=TRUE
TBT_X_USB_PWR_EN	TBT_X_USB_PWR_EN	MAKE_BASE=TRUE
PM_BATLOW_L	PM_BATLOW_L	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L	MAKE_BASE=TRUE
SMC_PME_S4_DARK_L		
UPC_X_SPI_CLK	UPC_X_SPI_CLK	MAKE_BASE=TRUE
UPC_X_SPI_CS_L	UPC_X_SPI_CS_L	MAKE_BASE=TRUE
UPC_X_SPI_MOSI	UPC_X_SPI_MOSI	MAKE_BASE=TRUE
UPC_X_SPI_MISO	UPC_X_SPI_MISO	MAKE_BASE=TRUE
UPC_T_SPI_CLK	UPC_T_SPI_CLK	MAKE_BASE=TRUE
UPC_T_SPI_CS_L	UPC_T_SPI_CS_L	MAKE_BASE=TRUE
UPC_T_SPI_MOSI	UPC_T_SPI_MOSI	MAKE_BASE=TRUE
UPC_T_SPI_MISO	UPC_T_SPI_MISO	MAKE_BASE=TRUE
JTAG_ISP_TDO	JTAG_ISP_TDO	MAKE_BASE=TRUE
TBT_POC_RESET	TBT_POC_RESET	MAKE_BASE=TRUE
DDI1_MUX_SEL	DDI1_MUX_SEL	MAKE_BASE=TRUE
DDI2_MUX_SEL	DDI2_MUX_SEL	MAKE_BASE=TRUE
TBT_X_CIO_PLUG_EVENT_L	TBT_X_CIO_PLUG_EVENT_L	MAKE_BASE=TRUE
XDP_USB_EXTA_OC_L	XDP_USB_EXTA_OC_L	MAKE_BASE=TRUE
XDP_USB_EXTB_OC_L	XDP_USB_EXTB_OC_L	MAKE_BASE=TRUE
JTAG_TBT_X_TMS	JTAG_TBT_X_TMS	MAKE_BASE=TRUE
JTAG_TBT_T_TMS	JTAG_TBT_T_TMS	MAKE_BASE=TRUE
SMC_DEBUGPRT_TX_L	SMC_DEBUGPRT_TX_L	MAKE_BASE=TRUE
SMC_DEBUGPRT_RX_L	SMC_DEBUGPRT_RX_L	MAKE_BASE=TRUE
NC_USBC_XA_RESET_L	NC_USBC_XA_RESET_L	MAKE_BASE=TRUE
USB_UPC_PCH_XA_N	USB_UPC_PCH_XA_N	MAKE_BASE=TRUE
USB_UPC_PCH_XA_N		
USB_UPC_PCH_XA_P	USB_UPC_PCH_XA_P	MAKE_BASE=TRUE
USB_UPC_PCH_XA_P		
USB_UPC_PCH_XB_N	USB_UPC_PCH_XB_N	MAKE_BASE=TRUE
USB_UPC_PCH_XB_N		
USB_UPC_PCH_XB_P	USB_UPC_PCH_XB_P	MAKE_BASE=TRUE
USB_UPC_PCH_XB_P		

POWER ALIASES

PP3V3_UPC_XA_LDO	PP3V3_UPC_XA_LDO	MAKE_BASE=TRUE
PP3V3_UPC_XA_LDO		
PP3V3_UPC_XA_LDO		
PP3V3_UPC_XB_LDO	PP3V3_UPC_XB_LDO	MAKE_BASE=TRUE
PP3V3_UPC_XB_LDO		
PP3V3_UPC_XB_LDO		
PP3V3_UPC_XB_LDO		
PP20V_USBC_XA_VBUS	PP20V_USBC_XA_VBUS	MAKE_BASE=TRUE
PP20V_USBC_XB_VBUS	PP20V_USBC_XB_VBUS	MAKE_BASE=TRUE
PP5V_S4_X_USBC	PP5V_S4_X_USBC	MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.0000 MIN_NECK_WIDTH=0.0520 VOLTAGE=5V
PP5V_S4_X_USBC		
PP5V_S4_X_USBC		
PP3V3_TBT_X_S0	PP3V3_TBT_X_S0	MAKE_BASE=TRUE; MIN_LINE_WIDTH=0.0000 MIN_NECK_WIDTH=0.0520 VOLTAGE=3.3V

BOM_COST_GROUP=TBT

AR/ACE SPI BUS SERIES R'S

USBC DEBUG CONN

TBT_X_SPI_CLK	R3094 100	TBT_X_SPI_CLK_DBG	
TBT_X_SPI_CS_L	R3095 15	UPC_XB_SPI_CLK	IN
TBT_X_SPI_MOSI	R3096 15	UPC_XB_SPI_CS_L	IN
TBT_X_SPI_MISO	R3097 15	UPC_XB_SPI_MOSI	IN
ROM	R3098 15	UPC_XB_SPI_MISO	OUT
	R3090 15	UPC_X_SPI_CLK	IN
	R3091 15	UPC_X_SPI_CS_L	IN
	R3092 15	UPC_X_SPI_MOSI	IN
	R3093 15	UPC_X_SPI_MISO	OUT

Ace AR

TBT to ACE

TBT — Alpine Ridge U2800 (MASTER)

I2C_TBT_X_SCL	I2C_TBT_X_SCL	MAKE_BASE=TRUE
I2C_TBT_X_SDA	I2C_TBT_X_SDA	MAKE_BASE=TRUE
I2C_TBT_XA_INT_L	I2C_TBT_XA_INT_L	MAKE_BASE=TRUE
I2C_TBT_XB_INT_L	I2C_TBT_XB_INT_L	MAKE_BASE=TRUE

Pri ACE — U3100 (Write: 0x70 Read: 0x71)

I2C_TBT_X_SCL	I2C_TBT_X_SCL
I2C_TBT_X_SDA	I2C_TBT_X_SDA
I2C_TBT_XA_INT_L	I2C_TBT_XA_INT_L

Sec ACE — U3200 (Write: 0x7E Read: 0x7F)

I2C_TBT_X_SCL	I2C_TBT_X_SCL
I2C_TBT_X_SDA	I2C_TBT_X_SDA
I2C_TBT_XB_INT_L	I2C_TBT_XB_INT_L

Ridge PCIE Caps D2R

PCIE_TBT_X_D2R_C_P<0>	C3050 0.22UF	PCIE_TBT_X_D2R_P<0>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_N<0>	C3051 0.22UF	PCIE_TBT_X_D2R_N<0>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_P<1>	C3052 0.22UF	PCIE_TBT_X_D2R_P<1>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_N<1>	C3053 0.22UF	PCIE_TBT_X_D2R_N<1>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_P<2>	C3054 0.22UF	PCIE_TBT_X_D2R_P<2>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_N<2>	C3055 0.22UF	PCIE_TBT_X_D2R_N<2>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_P<3>	C3056 0.22UF	PCIE_TBT_X_D2R_P<3>	GND_VOID=TRUE
PCIE_TBT_X_D2R_C_N<3>	C3057 0.22UF	PCIE_TBT_X_D2R_N<3>	GND_VOID=TRUE

0201 X5R 6.3V 20%

R2D

PCIE_TBT_X_R2D_C_P<0>	C3040 0.22UF	PCIE_TBT_X_R2D_P<0>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_N<0>	C3041 0.22UF	PCIE_TBT_X_R2D_N<0>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_P<1>	C3042 0.22UF	PCIE_TBT_X_R2D_P<1>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_N<1>	C3043 0.22UF	PCIE_TBT_X_R2D_N<1>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_P<2>	C3044 0.22UF	PCIE_TBT_X_R2D_P<2>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_N<2>	C3045 0.22UF	PCIE_TBT_X_R2D_N<2>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_P<3>	C3046 0.22UF	PCIE_TBT_X_R2D_P<3>	GND_VOID=TRUE
PCIE_TBT_X_R2D_C_N<3>	C3047 0.22UF	PCIE_TBT_X_R2D_N<3>	GND_VOID=TRUE

0201 X5R 6.3V 20%

PAGE TITLE	USB-C Support
	Apple Inc.
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	30 OF 145
SHEET	28 OF 119

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

CRITICAL
Q3100
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

PP20V_USBC_XA_VBUS_F
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=20V

PP20V_USBC_XA_VBUS
C3101 1UF 10% 35V X5R 0402

PPDCIN_G3H
MAX 100uF TOTAL ON RAIL

UPC_XA_GATE1
TP_Q3100_DRAIN
UPC_XA_GATE2

PP3V3_UPC_XA_LDO
PP3V3_G3H
GND
PP5V_S4_X_USBC
CAP FOR PP_5V0 ON VR PAGE
C3100 10UF 20% 6.3V CERM-X5R 0402-1

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
PP3V3_UPC_XA_LDO

P3V3_TBT_X_SX_EN_R
PP1V8_UPC_XA_LDOA
PP1V8_UPC_XA_LDOD
PP1V1_UPC_XA_LDO_BMC
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.1V

C3104 2.2UF 20% 4V X5R-CERM 0201
C3105 1.0UF 20% 6.3V X5R 0201-1
C3106 0.47UF 10% 6.3V CERM-X5R 0201
C3108 10UF 20% 6.3V CERM-X5R 0402-1

PULL R3109 AND R3108 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES

PP3V3_UPC_XA_LDO
R3109 1M 5% 1/20W MF 201 — I2C_UPC_XA_DBG_CTL_SCL
R3108 1M 5% 1/20W MF 201 — I2C_UPC_XA_DBG_CTL_SDA

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR

USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS

U3100
CD3215A
BGA
CRITICAL
OMIT_TABLE

TBT_POC_RESET	E11	MRESET
NC_USBC_XA_RESET_L	F11	RESET*
UPC_XA_DBG_UART_TX	B2	GPIO0
UPC_XA_DBG_UART_RX	C2	GPIO1
TBT_X_CIO_PWR_EN	D10	GPIO2
TBT_X_USB_PWR_EN	G11	GPIO3
DP_XA_HPD	C10	GPIO4
GND	E10	GPIO5
UPC_X_5V_EN	G10	GPIO6
SMC_PME_S4_DARK_L	D7	GPIO7
XDP_USB_EXTA_OC_L	H6	GPIO8
GND	F10	BUSPOWERZ
GND	F1	I2C_ADDR
UPC_XA_R_OSC	G2	R_OSC
I2C_UPC_XA_DBG_CTL_SCL	E4	DEBUG_CTL1
I2C_UPC_XA_DBG_CTL_SDA	D5	DEBUG_CTL2
I2C_TBT_X_SDA	D1	I2C_SDA1
I2C_TBT_X_SCL	D2	I2C_SCL1
I2C_TBT_XA_INT_L	C1	I2C_IRQ1*
I2C_UPC_X_SDA2	A5	I2C_SDA2
I2C_UPC_X_SCL2	B5	I2C_SCL2
SMC_USBC_INT_L	B6	I2C_IRQ2*
GND	A3	SPI_CLK
GND	B4	SPI_MOSI
GND	A4	SPI_MISO
GND	B3	SPI_SSZ
TP_UPC_XA_SWD_DATA	F4	SWD_DATA
TP_UPC_XA_SWD_CLK	G4	SWD_CLK
UPC_XA_UART_RX	F2	UART_RX
UPC_XA_UART_TX	E2	UART_TX
TBT_XA_LSTX	L4	LSX_R2P
TBT_XA_LSRX	K4	LSX_P2R
USB_UPC_XA_F_P	L5	USB_RP_P
USB_UPC_XA_F_N	K5	USB_RP_N
DP_XA_AUXCH_P	J1	AUX_P
DP_XA_AUXCH_N	J2	AUX_N
USB3_EXTA_D2R_P	L2	DEBUG1
USB3_EXTA_D2R_N	K2	DEBUG2
USB3_EXTA_R2D_P	L3	DEBUG3
USB3_EXTA_R2D_N	K3	DEBUG4

PRIMARY ONLY
PRIMARY ONLY

DIGITAL CORE I/O AND CONTROL
PORT MUX

HV FET/SENSE
TYPE-C

SS	H7	UPC_XA_SS
SENSEP	B10	
SENSEN	A10	
HV_GATE1	B9	
HV_GATE2	A9	
C_CC1	L9	USBC_XA_CC1
C_CC2	L10	USBC_XA_CC2
RPD_G1	K9	USBC_XA_CC1
RPD_G2	K10	USBC_XA_CC2
C_USB_TP	K6	USBC_XA_USB_DBG_TOP_P
C_USB_TN	L6	USBC_XA_USB_DBG_TOP_N
C_USB_BP	K7	USBC_XA_USB_DBG_BOT_P
C_USB_BN	L7	USBC_XA_USB_DBG_BOT_N
C_SBU1	K8	USBC_XA_SBU1
C_SBU2	L8	USBC_XA_SBU2
NC	L11	GROUND

C3109 0.47UF 10% 6.3V CERM-X5R 0201
C3114 220PF 10% 16V CER-X7R 0201
C3113 220PF 10% 16V CER-X7R 0201

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.2000

NC or GND to dissipate heat

CRITICAL
R3103 15K 0.1% 1/20W TF-LF 0201

GND_I2C_ADDR
PRIMARY ONLY

R3105 1M 5% 1/20W MF 201 — UPC_XA_UART_RX

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

L3100
90-OHM-0.1A
EXC4ACE
USB_UPC_PCH_XA_P
USB_UPC_PCH_XA_N
PLACE_NEAR=U3100:5mm

PP3V3_UPC_XA_LDO
PU to PP3V3_S4 if convenient for layout
Otherwise PU to PP3V3_UPC_XA_LDO
NO_XNET_CONNECTION=1
R3110 100K 5% 1/20W MF 201

NO_XNET_CONNECTION=1
R3111 100K 5% 1/20W MF 201

GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C PORT CONTROLLER A
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	31 OF 145
SHEET	29 OF 119

Apple Inc.

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

CRITICAL
Q3200
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

28 PP20V_USBC_XB_VBUS_F
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=20V

28 PP20V_USBC_XB_VBUS
C3201 1UF 10% 25V X5R 0402

NC

UPC_XB_GATE1
TP_Q3200_DRAIN
UPC_XB_GATE2

PPDCIN_G3H 29 94 95 96 100
MAX 100uF TOTAL ON RAIL

28 PP3V3_UPC_XB_LDO
100 PP3V3_G3H
96 95 29 28 GND
28 PP5V_S4_X_USBC
CAP FOR PP_5V0 ON VR PAGE
C3200 10UF 20% 6.3V CERM-X5R 0402-1

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
PP3V3_UPC_XB_LDO 28
P3V3_TBT_X_SX_EN_R 32
PP1V8_UPC_XB_LDOA
PP1V8_UPC_XB_LDOD
PP1V1_UPC_XB_LDO_BMC

MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=1.1V
C3204 2.2UF 20% 4V X5R-CERM 0201
MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=1.8V
C3205 1.0UF 20% 6.3V X5R 0201-1
MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=1.8V
C3206 0.47UF 10% 6.3V CERM-X5R 0201
MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=3.3V
C3208 10UF 20% 6.3V CERM-X5R 0402-1

A11 PP_5V0
B11 PP_5V0
C11 PP_5V0
D11 PP_5V0
A6 PP_HV
A7 PP_HV
A8 PP_HV
B7 PP_HV
H10 PP_CABLE
H11 VBUS
J10 VBUS
J11 VBUS
K11 VBUS
H1 VIN_3V3
B1 VDDIO
G1 LDO_3V3
H2 VOUT_3V3
K1 LDO_1V8A
A2 LDO_1V8D
E1 LDO_BMC

CRITICAL
OMIT_TABLE

U3200
CD3215A
BGA

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

29 28 EN	TBT_POC_RESET	E11	MRESET
32 OUT	USBC_X_RESET_L_R	F11	RESET*
28	UPC_XB_DBG_UART_TX	B2	GPIO0
28	UPC_XB_DBG_UART_RX	C2	GPIO1
29 28 26 EN	TBT_X_CIO_PWR_EN	D10	GPIO2
29 28 26 EN	TBT_X_USB_PWR_EN	G11	GPIO3
28 OUT	DP_XB_HPD	C10	GPIO4
28	GND	E10	GPIO5
28 OUT	UPC_X_5V_EN	G10	GPIO6
96 95 29 28 OUT	SMC_PME_S4_DARK_L	D7	GPIO7
28 OUT	XDP_USB_EXTB_OC_L	H6	GPIO8
28 EN	GND	F10	BUSPOWERZ
28	NC_UPC_XB_I2C_ADDR	F1	I2C_ADDR
	UPC_XB_R_OSC	G2	R_OSC
30	I2C_UPC_XB_DBG_CTL_SCL	E4	DEBUG_CTL1
30	I2C_UPC_XB_DBG_CTL_SDA	D5	DEBUG_CTL2
28 BI	I2C_TBT_X_SDA	D1	I2C_SDA1
28 BI	I2C_TBT_X_SCL	D2	I2C_SCL1
28 OUT	I2C_TBT_XB_INT_L	C1	I2C_IRQ1*
28 BI	I2C_UPC_X_SDA2	A5	I2C_SDA2
28 BI	I2C_UPC_X_SCL2	B5	I2C_SCL2
51 OUT	SMC_USBC_INT_L	B6	I2C_IRQ2*
28 OUT	UPC_XB_SPI_CLK	A3	SPI_CLK
28 OUT	UPC_XB_SPI_MOSI	B4	SPI_MOSI
28 IN	UPC_XB_SPI_MISO	A4	SPI_MISO
28 OUT	UPC_XB_SPI_CS_L	B3	SPI_SSZ
	TP_UPC_XB_SWD_DATA	F4	SWD_DATA
	TP_UPC_XB_SWD_CLK	G4	SWD_CLK
30 29 28 IN	UPC_XA_UART_TX	F2	UART_RX
29 28 OUT	UPC_XA_UART_RX	E2	UART_TX
26 IN	TBT_XB_LSTX	L4	LSX_R2P
26 OUT	TBT_XB_LSRX	K4	LSX_P2R
	USB_UPC_XB_F_P	L5	USB_RP_P
	USB_UPC_XB_F_N	K5	USB_RP_N
	DP_XB_AUXCH_P	J1	AUX_P
	DP_XB_AUXCH_N	J2	AUX_N
42 BI	SOC_SWCLK_DBG	L2	DEBUG1
42 BI	SOC_SWDIO_DBG	K2	DEBUG2
28 BI	SMC_DEBUGPRT_TX_L	L3	DEBUG3
28 BI	SMC_DEBUGPRT_RX_L	K3	DEBUG4

PULL R3209 AND R3208 UP TO ACEs LDOs FOR 1ST BTDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

PP3V3_UPC_XB_LDO 28
R3209 1M 5% 1/20W MF 201 — I2C_UPC_XB_DBG_CTL_SCL 30
R3208 1M 5% 1/20W MF 201 — I2C_UPC_XB_DBG_CTL_SDA 30
R3205 1M 5% 1/20W MF 201 — UPC_XA_UART_TX 28 29 30

CRITICAL
R3203 15K 0.1% 1/20W TF-LF 0201 — NEED 0.1%

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

L3200
90-OHM-0.1A
EXCX4CE
USB_UPC_PCH_XB_P 28 BI — 1 — 4 — PLACE_NEAR=U3200.L5:5mm
USB_UPC_PCH_XB_N 28 BI — 2 — 3 — PLACE_NEAR=U3200.K5:5mm

28 PP3V3_UPC_XB_LDO
PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_XB_LDO
NO_XNET_CONNECTION=1
R3210 100K 5% 1/20W MF 201
26 BI
26 BI
R3211 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

HV FET/SENSE

SS H7 — UPC_XB_SS
SENSEP B10
SENSEN A10
HV_GATE1 B9
HV_GATE2 A9
C3209 0.47UF 10% 6.3V CERM-X5R 0201

DIGITAL CORE I/O AND CONTROL

TYPE-C

C_CC1 L9 — USBC_XB_CC1 — BI 28 31 104 — MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.2000
C_CC2 L10 — USBC_XB_CC2 — BI 28 31 104 — MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.2000
RPD_G1 K9 — USBC_XB_CC1 — BI 28
RPD_G2 K10 — USBC_XB_CC2 — BI 28
C3214 220PF 10% 16V CER-X7R 0201
C3213 220PF 10% 16V CER-X7R 0201
C_USB_TP K6 — USBC_XB_USB_TOP_P — BI 31
C_USB_TN L6 — USBC_XB_USB_TOP_N — BI 31
C_USB_BP K7 — USBC_XB_USB_BOT_P — BI 31
C_USB_BN L7 — USBC_XB_USB_BOT_N — BI 31
C_SBU1 K8 — USBC_XB_SBU1 — BI 31
C_SBU2 L8 — USBC_XB_SBU2 — BI 31

GROUND
NC L11
NC or GND to dissipate heat

PORT MUX

GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND GND
A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7

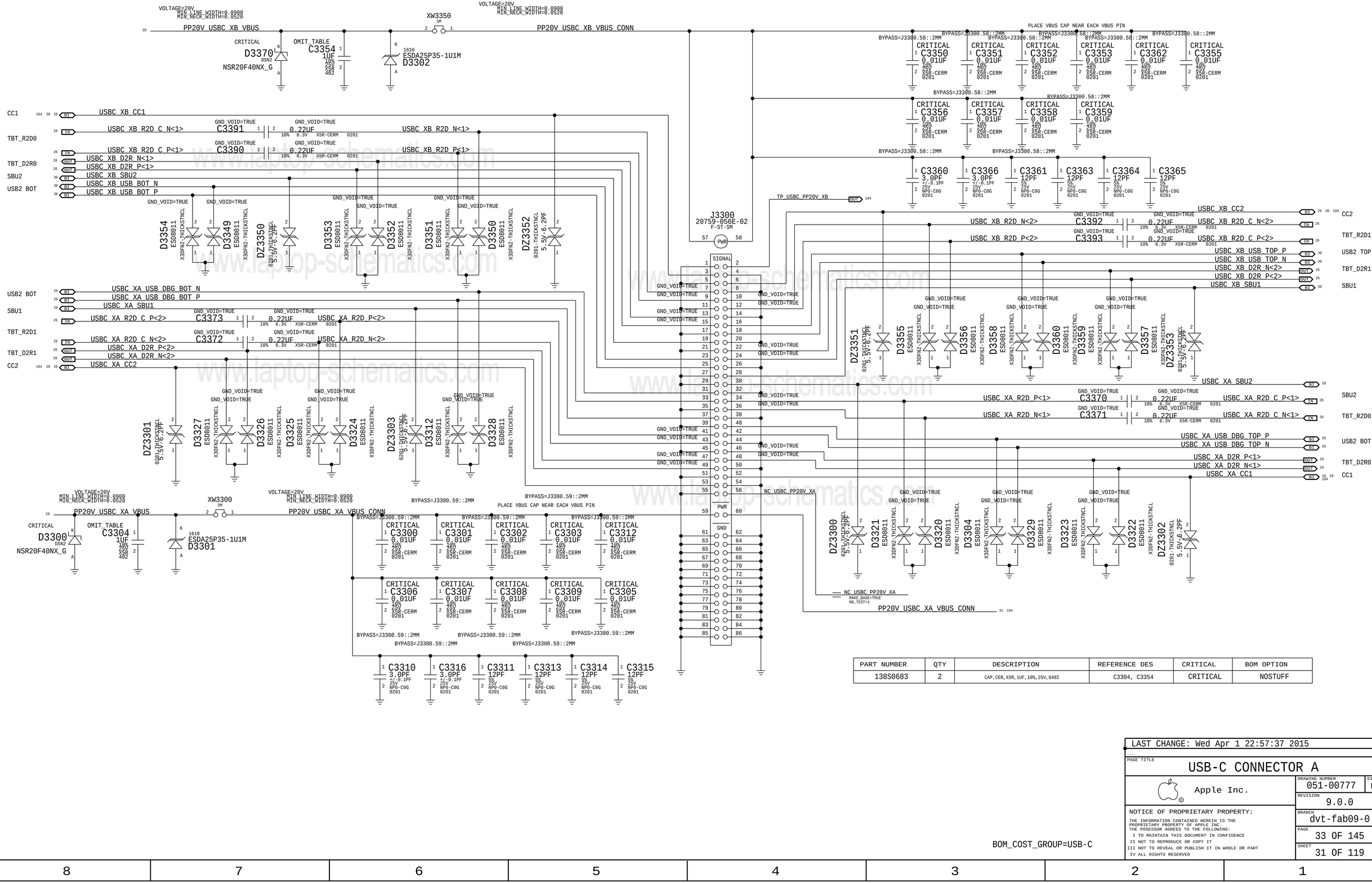
GND 28
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

SYNC_MASTER=J79_GREG SYNC_DATE=02/28/2019
PAGE TITLE: USB-C PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 32 OF 145
SHEET 30 OF 119



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	C3304, C3354	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE

USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER 051-00777 | SIZE D

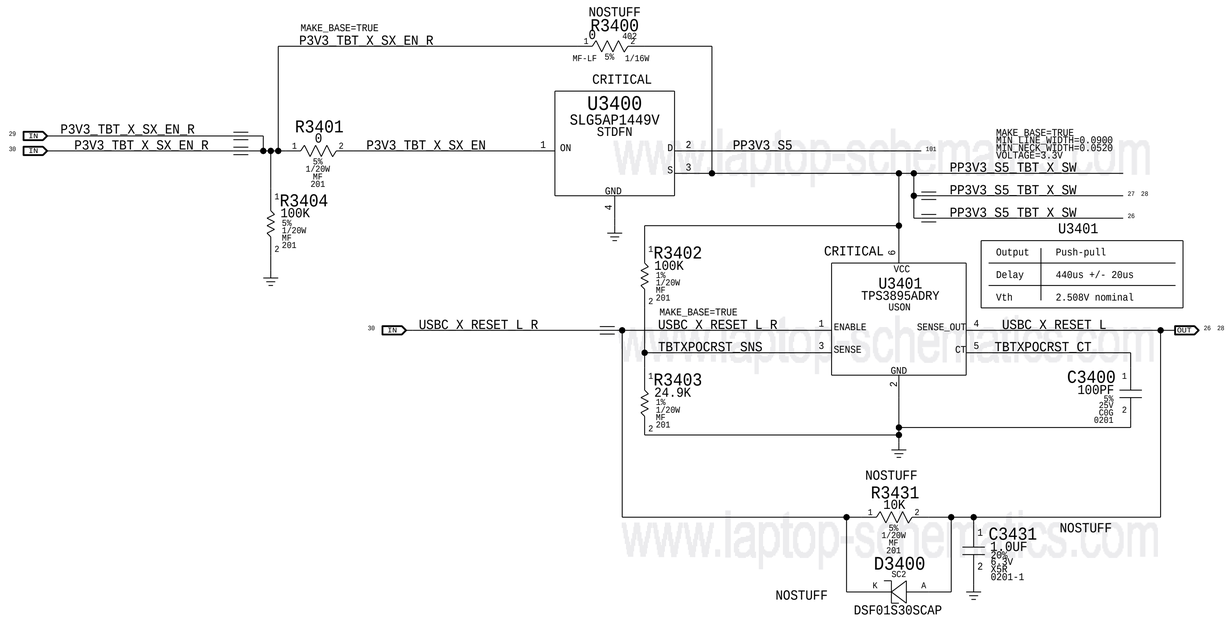
REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 33 OF 145

SHEET 31 OF 119

TBT X "POC" Power-up Reset



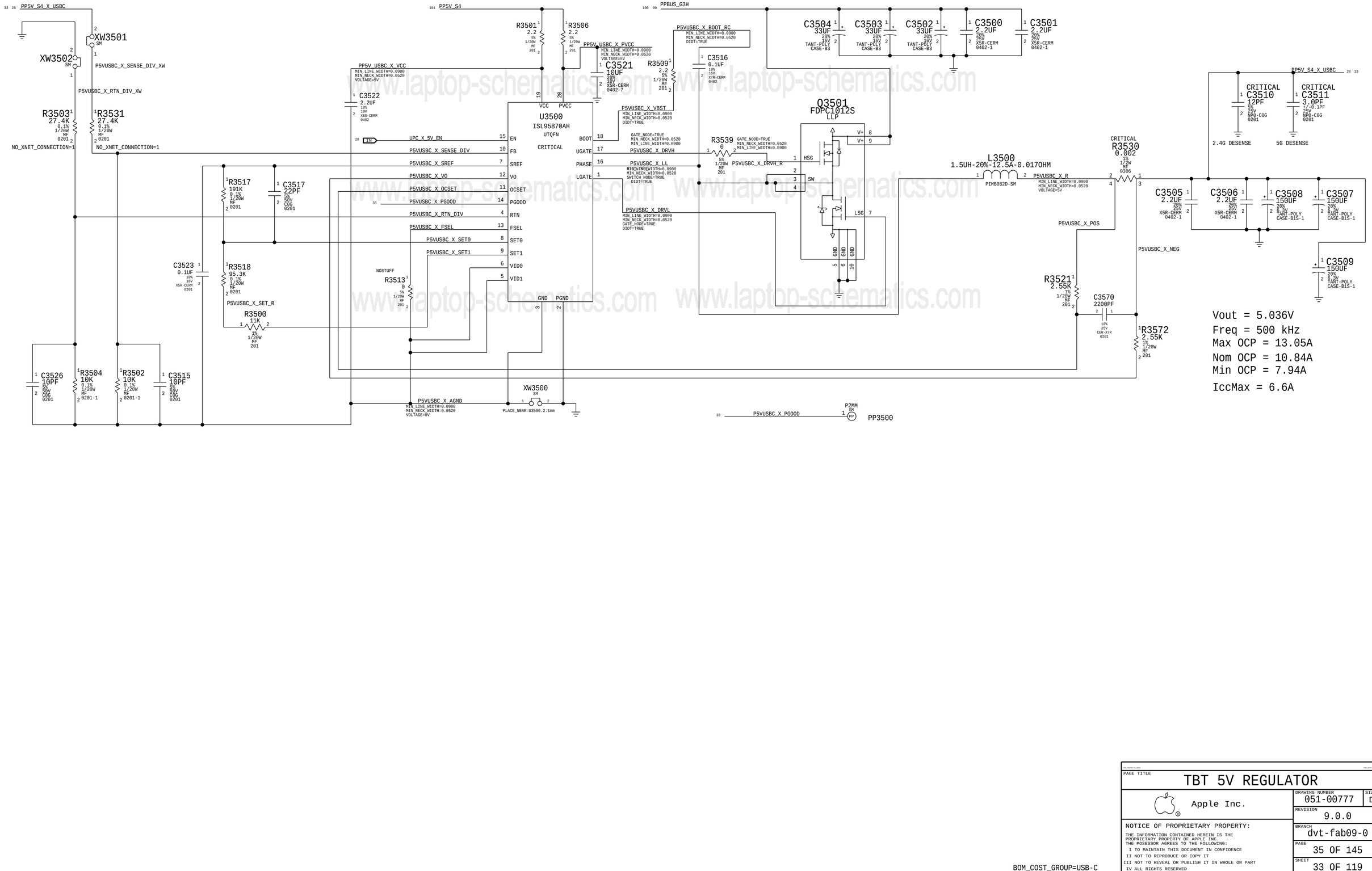
BOM_COST_GROUP=USB-C

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015
SYNC_MASTER=J79_GREG SYNC_DATE=03/24/2016

PAGE TITLE
USB-C CONNECTOR B

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 34 OF 145
SHEET 32 OF 119



BOM_COST_GROUP=USB-C

PAGE TITLE

TBT 5V REGULATOR

Apple Inc.

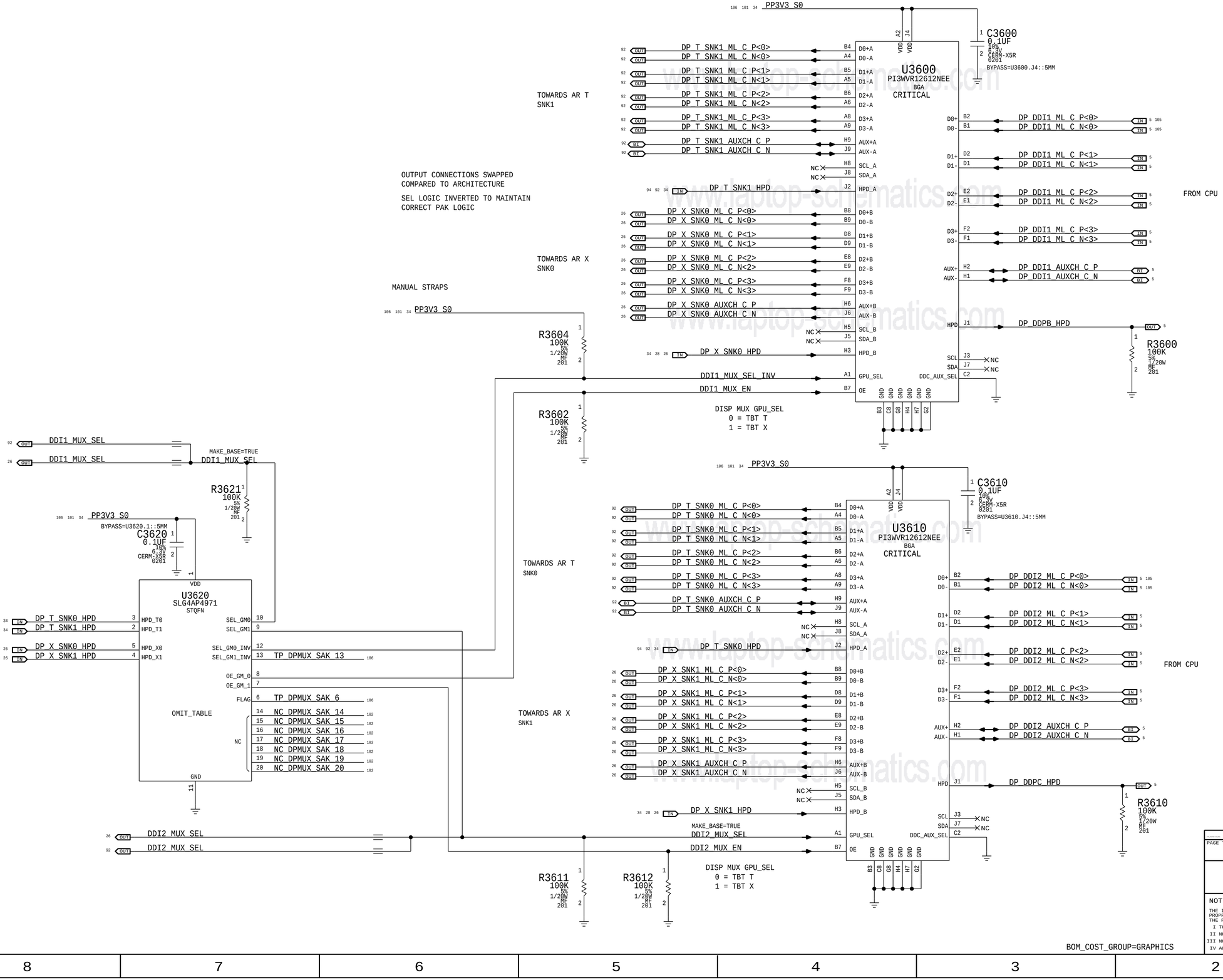
DRAWING NUMBER 051-00777 | SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 35 OF 145

SHEET 33 OF 119



PAGE TITLE: Display Mux

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 36 OF 145
SHEET: 34 OF 119

U3730 LBEE5UQ1HG-844 LGA

SYM 2 OF 2

THRM_PAD THRM_PAD

PP3V3_S4_BT MAKE_BASE=TRUE

PP3V3_S4_WLAN_SW MAKE_BASE=TRUE VOLTAGE=3.3V

FEM SUPPLY SHUNT CAPACITORS
PLACE ON THE TOP SIDE CLOSE TO U3730

C3761 3.0PF ±0.1PF 25V NPO-C0G 0201
C3740 12PF 5% 25V NPO-C0G 0201
C3736 10UF 20% 6.3V CERM-X5R 0402-4
C3762 3.0PF ±0.1PF 25V NPO-C0G 0201
C3763 3.0PF ±0.1PF 25V NPO-C0G 0201
C3742 12PF 5% 25V NPO-C0G 0201
C3741 12PF 5% 25V NPO-C0G 0201
C3737 10UF 20% 6.3V CERM-X5R 0402-4
C3738 10UF 20% 6.3V CERM-X5R 0402-4

FOR JTAG MODE REMOVE R3735

R3735 0 5% 1/20W MF 201 NO_XNET_CONNECTION=1

C3758 12PF 5% 25V NPO-C0G 0201
C3757 12PF 5% 25V NPO-C0G 0201
C3704 10UF 20% 6.3V CERM-X5R 0402-4
C3705 0.1UF 10% 35V CER-X5R 0201

C3739 10UF 20% 6.3V CERM-X5R 0402-4
C3701 0.1UF 10% 35V CER-X5R 0201
C3703 0.1UF 10% 35V CER-X5R 0201
C3702 0.1UF 10% 35V CER-X5R 0201
C3759 0.1UF 10% 6.3V X7R 0201
C3760 0.1UF 10% 6.3V X7R 0201

SROM_STRAPS

R3731 10K 5% 1/20W MF 201
R3734 10K 5% 1/20W MF 201

STRAP_0 HI:SROM (Default)
STRAP_1 LO:16kb SROM

U3730 LBEE5UQ1HG-844 LGA

SYM 1 OF 2 CRITICAL

95	1P2V_EN	
2	VDD3P3	
89	VDD3P3_PAD	
96	VDD3P3_REG1P2	
88	VDD3P3_REGLP0	
68	VDD3P3_FEM_CORE1	
81	VDD3P3_FEM_CORE2	
55	VDD3P3_FEM_CORE0	
24	VDD_BT	
32	BT_VDDIO	
30	BT_OTP_VDD3P3V	
19	WL_VDDIO	

45	BT_RF1	NC
47	2G_ANT_CORE0	50_G_0_MATCH
63	2G_ANT_CORE1	50_G_1_MATCH
78	2G_ANT_CORE2	50_G_2_MATCH
61	5G_ANT_CORE0	50_A_0_MATCH
74	5G_ANT_CORE1	50_A_1_MATCH
85	5G_ANT_CORE2	50_A_2_MATCH
22	WL_GPIO_6/UART_RX	WLAN_UART_RX
23	WL_GPIO_7/UART_TX	WLAN_UART_TX
93	WL_JTAG_TDI/GPIO_3	WLAN_JTAG_TDI
72	WL_JTAG_TMS	WLAN_JTAG_TMS
71	WL_JTAG_TCK	WLAN_JTAG_TCK
70	WL_JTAG_TRST*	WLAN_JTAG_TRST_L
94	WL_JTAG_SEL	WLAN_JTAG_SEL
21	WLAN_EXT_POR*	WLAN_EXT_POR_L
92	WL_JTAG_TDO	CORE2_5G_CTL2_WLAN_JTAG_TDO
91	C0_FEMCTRL_2/STRAP_0	WLAN_STRAP_0
90	C2_FEMCTRL_2/STRAP_1	WLAN_STRAP_1
97	SPROM_CLK	SPROM_CLK
98	SPROM_DOUT	SPROM_DOUT
99	SPROM_CS	SPROM_CS
100	SPROM_DIN	SPROM_DIN
58	BT_SPI2_MOSI	BT_SPI2_MOSI
59	BT_SPI2_CSN	BT_SPI2_CSN
65	BT_SPI2_MISO	BT_SPI2_MISO
66	BT_SPI2_CLK	BT_SPI2_CLK
29	BT_GPIO_2/BT_JTAG_TRST_N	NC
28	BT_GPIO_3	BT_ROM_BOOT_L
27	BT_GPIO_4	BT_TIMESTAMP

GND pins: 1, 3, 5, 8, 11, 14, 18, 20, 26, 38, 39, 40, 44, 46, 48, 51, 54, 60, 62, 64, 67, 69, 73, 75, 76, 77, 79, 80, 82, 83, 84, 86, 87

R3701 1K 5% 1/20W MF 201 NOSTUFF
R3759 270K 5% 1/20W MF 201

Q3701 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
PCH_BT_ROM_BOOT

BLUETOOTH SERIAL FLASH

R3751 100K 5% 1/20W MF 201
R3752 100K 5% 1/20W MF 201
R3753 100K 5% 1/20W MF 201
R3754 1K 5% 1/20W MF 201

U3750 2MBIT USON MX25L2006EZUI-12G OMIT_TABLE

6	SCLK
5	SI/SIO0
2	SO/SIO1
1	CS*
3	WP*
7	HOLD*
4	GND
9	THRM PAD

BT_SPI2_CLK, BT_SPI2_CSN, BT_SPI2_MOSI, BT_SPI2_MISO, BT_SFLASH_CS_L, BT_SFLASH_WP_L, BT_SFLASH_HOLD_L

C3756 0.1UF 10% 35V CER-X5R 0201

WLAN SERIAL EEPROM

U3710 CAS93C86B UDFN8 OMIT_TABLE

3	DI	SPROM_DOUT
1	CS	SPROM_CS
2	SK	SPROM_CLK
7	PE	NC
4	DO	SPROM_DIN
6	ORG	WIFI_SROM_ORG
5	GND	
9	EPAD	

C3711 0.1UF 10% 35V CER-X5R 0201
R3712 10K 5% MF 201

PRECISION ELPO

U3780 32.768KHZ-25PPM-15PF-5.5V 2.50X2.00-SM-COMBO CRITICAL

1	EN/DIS	
3	OUT	SYSCLK_CLK32K_OSC_OUT
2	GND	
4	VCC	PP1V8_S4

C3780 0.1UF 10% 25V C0G-CERM 0201 BYPASS=U3780.4::5MM
R3780 0 5% 1/20W MF 201 SYSCLK_CLK32K_WIFIBT

R3781 0 5% 1/20W MF 201 WIFI_DBG BT_SPI2_CLK
R3782 0 5% 1/20W MF 201 WIFI_DBG BT_SPI2_CSN
R3783 0 5% 1/20W MF 201 WIFI_DBG BT_SPI2_MISO
R3784 0 5% 1/20W MF 201 WIFI_DBG BT_SPI2_MOSI

DEBUG CONNECTOR

WIFI_DBG J3701 AA25D-S038VA1 F-ST-SM

1	BT_LOW_PWR_L	2	BT_LOW_PWR_L
3	SMC_PME_S4_DARK_L	4	SMC_PME_S4_DARK_L
5	SMC_WIFI_PWR_EN	6	SMC_BT_PWR_EN
7	WLAN_UART_TX	8	BT_UART_D2R
9	WLAN_UART_RX	10	BT_UART_R2D
11		12	BT_UART_CTS_R2D_L
13		14	BT_UART_RTS_D2R_L
15	WLAN_JTAG_TCK	16	BT_SPI2_CLK_R
17	WLAN_JTAG_TMS	18	BT_SPI2_CSN_R
19	WLAN_JTAG_TDI	20	BT_SPI2_MISO_R
21	CORE2_5G_CTL2_WLAN_JTAG_TDO	22	BT_SPI2_MOSI_R
23	WLAN_JTAG_TRST_L	24	BT_ROM_BOOT_L
25	WLAN_JTAG_SEL	26	BT_TIMESTAMP
27		28	BT_SWDIO
29		30	BT_SWDCLK
31	AP_CLKREQ_L	32	SYSCLK_CLK32K_WIFIBT
33	AP_RESET_L	34	
35	AP_PCIE_WAKE_L	36	PP3V3_S4_WLAN_SW
37	PP3V3_S4_WLAN_SW	38	
39		40	
41		42	

BOM_COST_GROUP=WIRELESS

U3730 LBEE5UQ1HG-844 LGA

SYM 1 OF 2 CRITICAL

6	PCIE_RDP	PCIE_AP_R2D_P
7	PCIE_RDN	PCIE_AP_R2D_N
10	PCIE_TDP	PCIE_AP_D2R_P
9	PCIE_TDN	PCIE_AP_D2R_N
13	PCIE_REFCLK_PC	PCIE_CLK100M_AP_P
12	PCIE_REFCLK_NC	PCIE_CLK100M_AP_N
15	PCIE_WAKE_CL	AP_PCIE_WAKE_L
16	PCIE_CLKREQ*	AP_CLKREQ_L
17	PCIE_PRST*	AP_RESET_CONN_L
43	BT_RX_ACTIVE/BT_GPIO_5	BT_RX_ACTIVE
41	BT_UART_CTS*/BT_JTAG_TMS	BT_UART_CTS_R2D_L
42	BT_UART_RTS*/BT_JTAG_TCK	BT_UART_RTS_D2R_L
36	BT_UART_RXD/BT_JTAG_TDI	BT_UART_R2D
37	BT_UART_TXD/BT_JTAG_TDO	BT_UART_D2R
57	BT_SWDIO	BT_SWDIO
56	BT_SWDCLK	BT_SWDCLK
4	WL_XTAL32	WL_CLK32K
25	BT_XTAL32	
33	BT_HOST_WAKE/BT_HOST_WAKE*	SMC_PME_S4_DARK_L
35	BT_DEV_WAKE	BT_LOW_PWR_L
49	BT_PCM_SYNC	BT_I2S_SYNC
50	BT_PCM_IN	BT_I2S_R2D
52	BT_PCM_OUT	BT_I2S_D2R
53	BT_PCM_CLK	BT_I2S_CLK
31	BT_RST*	SMC_BT_PWR_EN
34	BT_JTAG_SEL	NC

R3762 10K 5% MF 201

Q3702 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3

SYSCLK_CLK32K_WIFIBT

BT UART TX & RTS ISOLATION CIRCUIT

R3766 100K 5% 1/20W MF 201
R3767 100K 5% 1/20W MF 201
R3776 100K 5% 1/20W MF 201
R3777 100K 5% 1/20W MF 201

BT_UART_CTS_R2D_L, BT_UART_RTS_D2R_L, BT_UART_R2D, BT_UART_D2R

BT UART RX & CTS ISOLATION CIRCUIT

U3760 74LVC2G126 X2-DFN2010 CRITICAL

1	1OE	
2	A1	PCH_BT_UART_CTS_L
5	A2	PCH_BT_UART_D2R
7	2OE	PLT_RST_L
6	Y1	BT_UART_CTS_L
3	Y2	PCH_BT_UART_D2R
4	GND	
8	VCC	PP3V3_S4_BT

C3764 0.1UF 10% 35V CER-X5R 0201

U3770 74LVC2G126 X2-DFN2010 CRITICAL

1	1OE	
2	A1	PCH_BT_UART_RTS_L
5	A2	PCH_BT_UART_R2D
7	2OE	PLT_RST_L
6	Y1	BT_UART_CTS_R2D_L
3	Y2	BT_UART_R2D
4	GND	
8	VCC	PP3V3_S4_BT

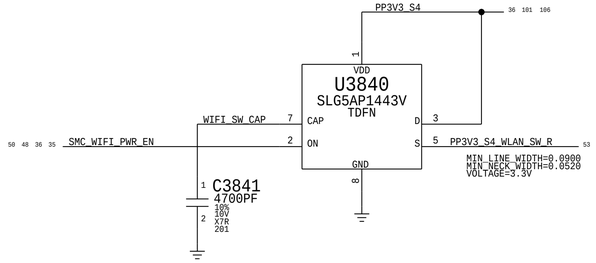
C3774 0.1UF 10% 35V CER-X5R 0201

PAGE TITLE: WIFI/BT: MODULE 1

Apple Inc.

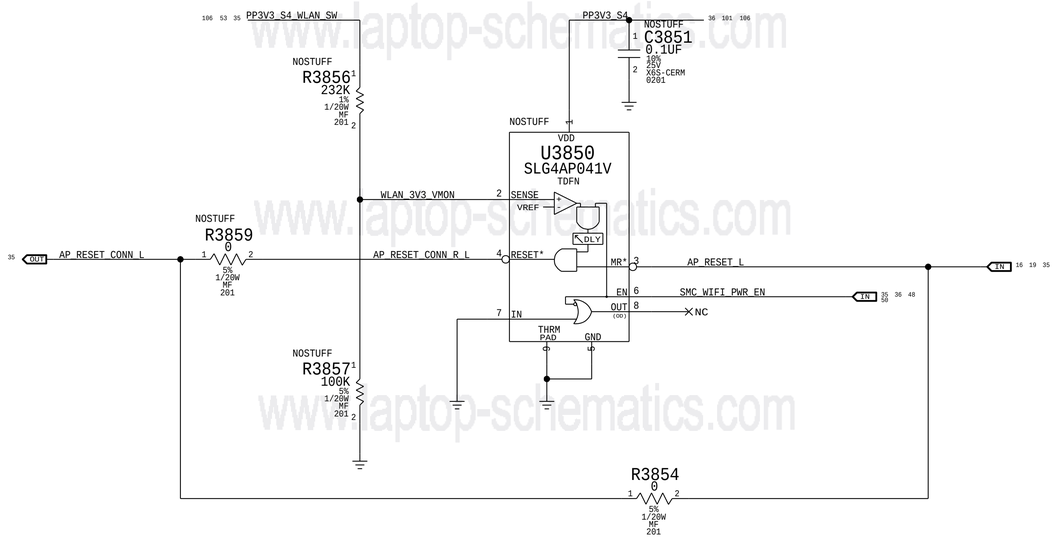
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	37 OF 145
SHEET	35 OF 119

WLAN Power Switch

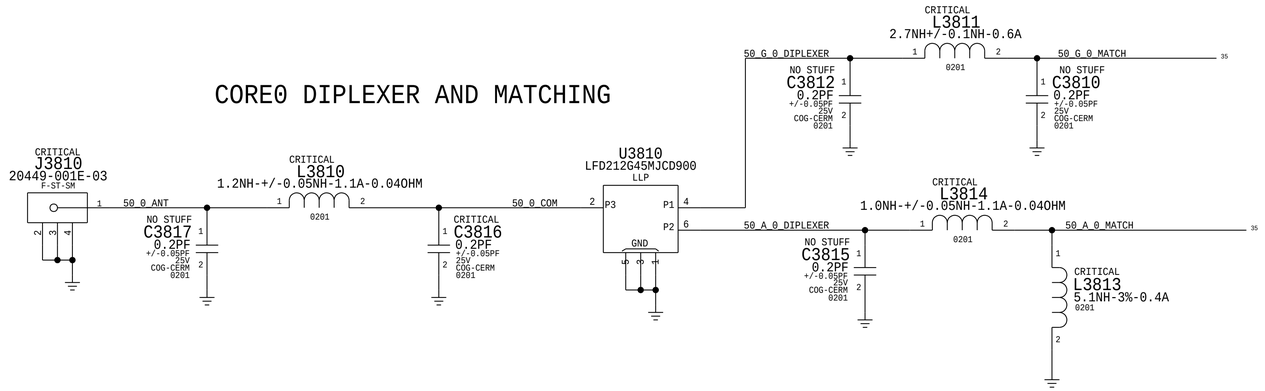


Supervisor & CLKREQ# Isolation

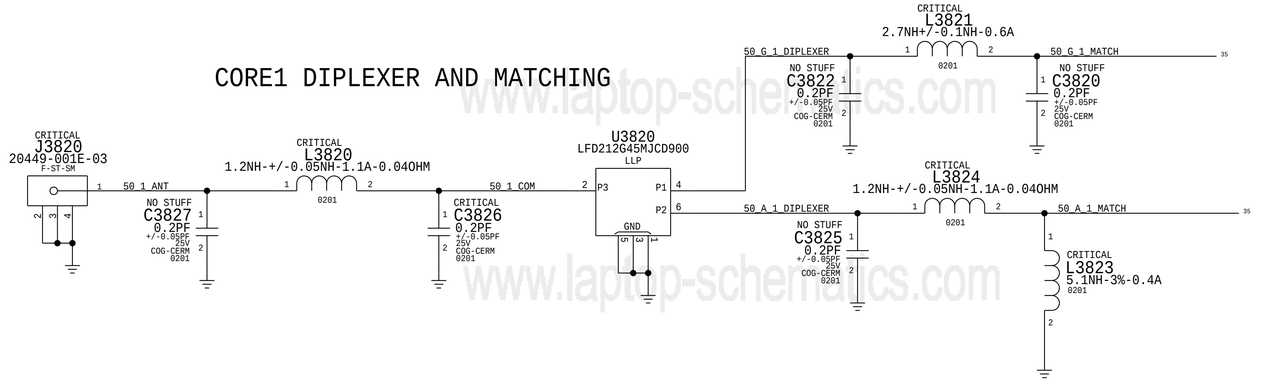
Delay = 130ms +/- 20%



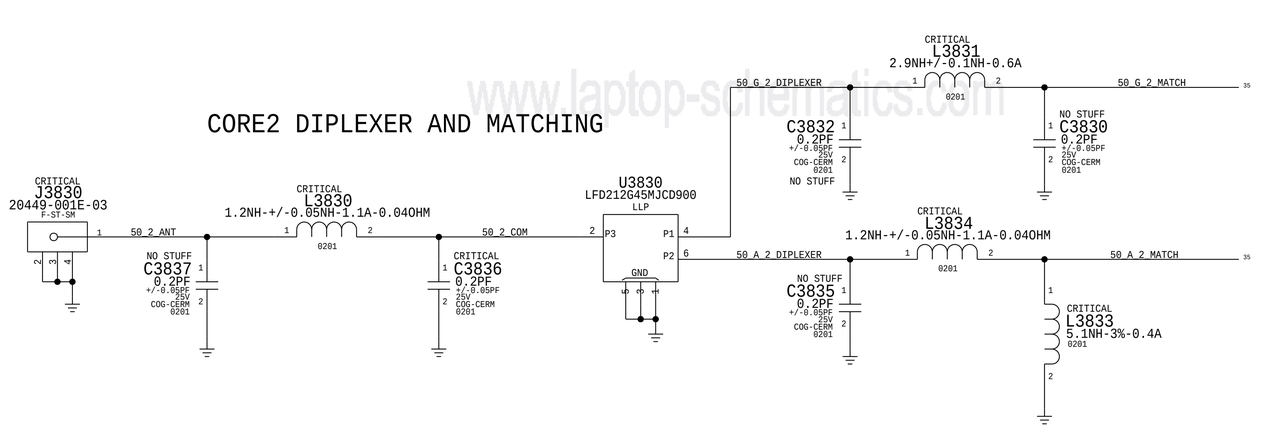
CORE0 DIPLEXER AND MATCHING



CORE1 DIPLEXER AND MATCHING



CORE2 DIPLEXER AND MATCHING



BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J79_METE SYNC_DATE=03/02/2016

PAGE TITLE

WIFI/BT: MODULE 2

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 38 OF 145

SHEET 36 OF 119

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00135	1	IC,M8+512MB 20NM DDR,A12,S,SCK,BGA700	U3900	CRITICAL	

T208

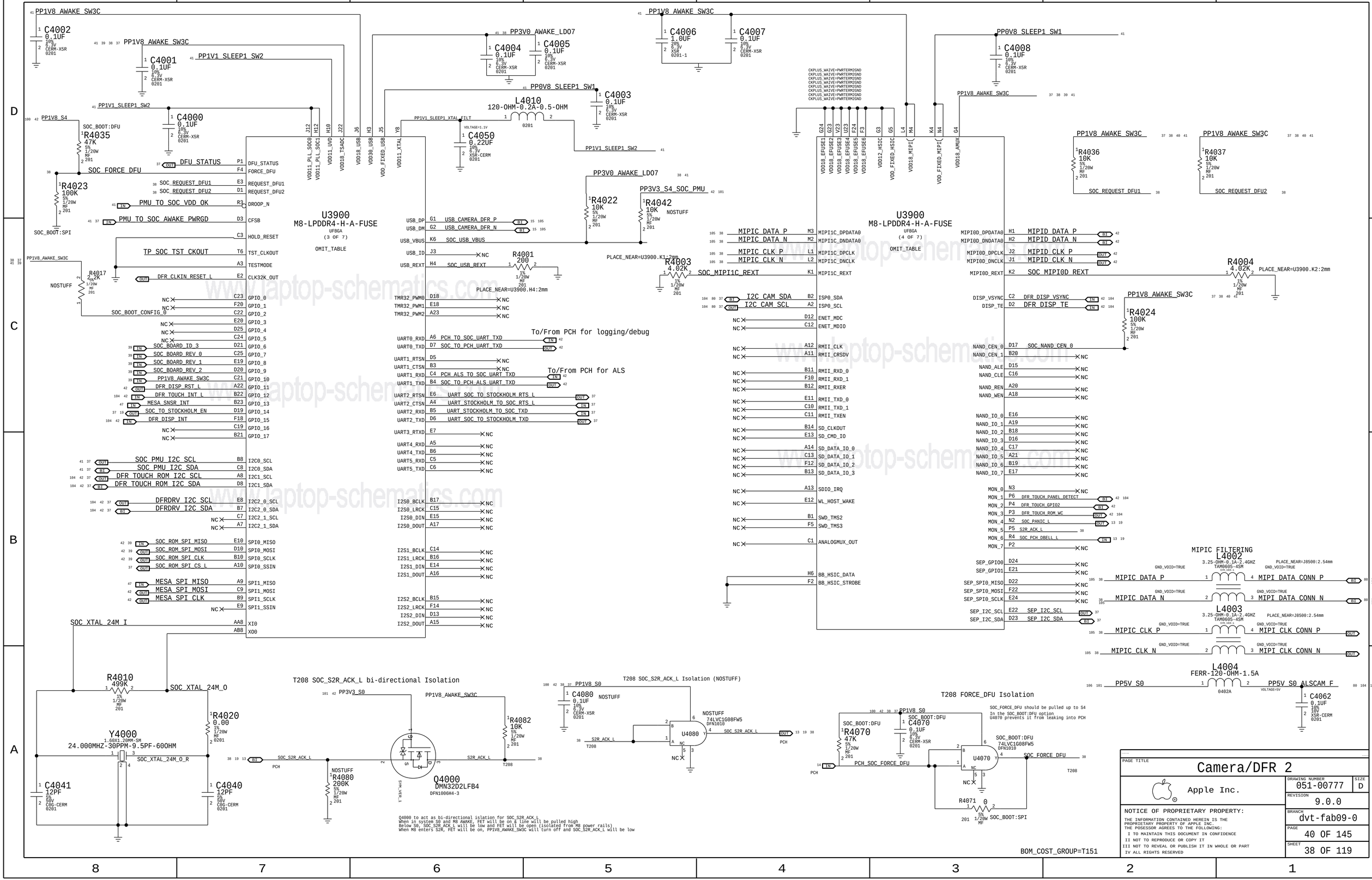
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00147	1	IC,RTM2,DEV,PN549A1,P61D0	U3905	CRITICAL	SE:DEV
338S00097	1	IC,RTM2,MP,PN549A1,P61D0	U3905	CRITICAL	SE:PROD

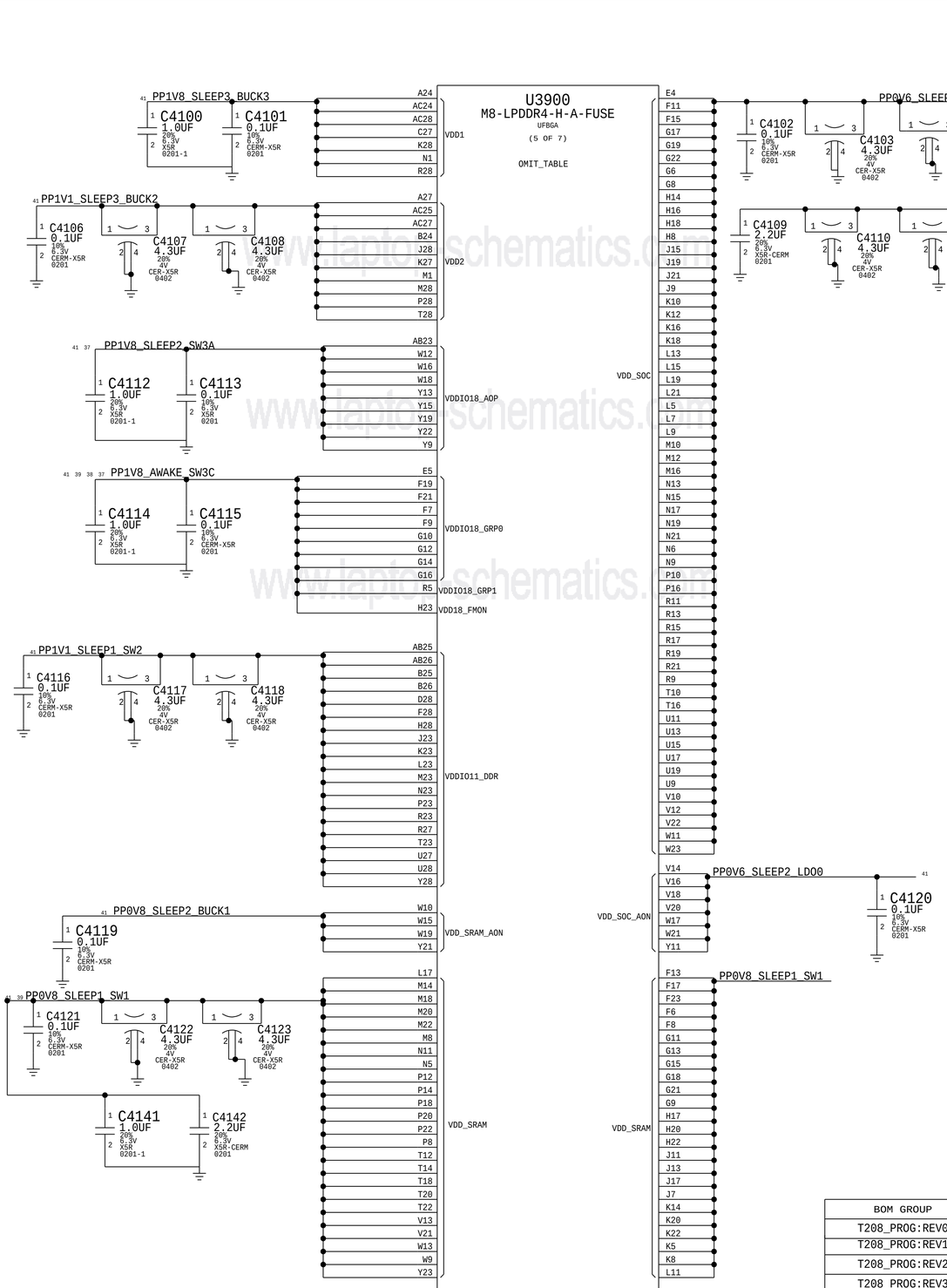
L3900 120-OHM-0.1A-1.5-OHM 0201
C3900 0.22UF 10% 6.3V X5R-CERM 0201
C3903 0.1UF 10% 6.3V CERM-X5R 0201
SEP ROM
U3901 M24128 EEPROM MLP
R3970 10K 5% 1/20W MF 201
R3900 499 1% 1/20W MF 201
C3902 0.47UF 10% 6.3V CERM-X5R 0201
C3919 4.7UF 20% 6.3V X5R 402
C3918 1.0UF 20% 6.3V X5R 0201-1
C3925 1.0UF 20% 6.3V X5R 0201-1
C3916 0.1UF 10% 6.3V CERM-X5R 0201
C3917 1.0UF 20% 6.3V X5R 0201-1
C3915 0.1UF 10% 6.3V CERM-X5R 0201
STOCKHOLM
OMIT_TABLE
U3905 PN66VEU3-A101D004 UFLGA
OMIT_TABLE
U3900 M8-LPDDR4-H-A-FUSE UFBGA (1 OF 7)
OMIT_TABLE
U3900 M8-LPDDR4-H-A-FUSE UFBGA (2 OF 7)
R3952 1K 5% 1/20W MF 201
R3951 10K 5% 1/20W MF 201
R3953 1K 5% 1/20W MF 201
R3973 10K 5% 1/20W MF 201
C3960 100PF 5% 25V C0G 0201
R3901 240 1% 1/20W MF 201
R3902 240 1% 1/20W MF 201
32K CLK OPTION
R3990 0 5% 1/20W MF 0201
R3925 0 5% 1/20W MF 0201
R3981 0 5% 1/20W MF 0201
R3980 0 5% 1/20W MF 0201
U3910 74LVC2G08GT/SS505 SOT833
C3950 0.1UF 10% 6.3V CERM-X5R 0201
R3972 300K 5% 1/20W MF 201
R3971 100K 5% 1/20W MF 201
R3960 3.0K 5% 1/20W MF 201
R3961 3.0K 5% 1/20W MF 201
R3906 1K 5% 1/20W MF 201
R3907 1K 5% 1/20W MF 201
R3917 4.7K 5% 1/20W MF 201
R3918 4.7K 5% 1/20W MF 201
R3940 100K 5% 1/20W MF 201
4MB SPI ROM
C3920 0.1UF 10% 6.3V CERM-X5R 0201
R3942 10K 5% 1/20W MF 201
R3941 10K 5% 1/20W MF 201
U3906 4MX8-1.8V UFDFPN N25Q032A11E
I2C Pullups
R3904 2.2K 5% 1/20W MF 201
R3905 2.2K 5% 1/20W MF 201
R3911 2.2K 5% 1/20W MF 201
R3912 2.2K 5% 1/20W MF 201
R3915 2.2K 5% 1/20W MF 201
R3916 2.2K 5% 1/20W MF 201
R3943 78.7K 1% 1/20W MF 201

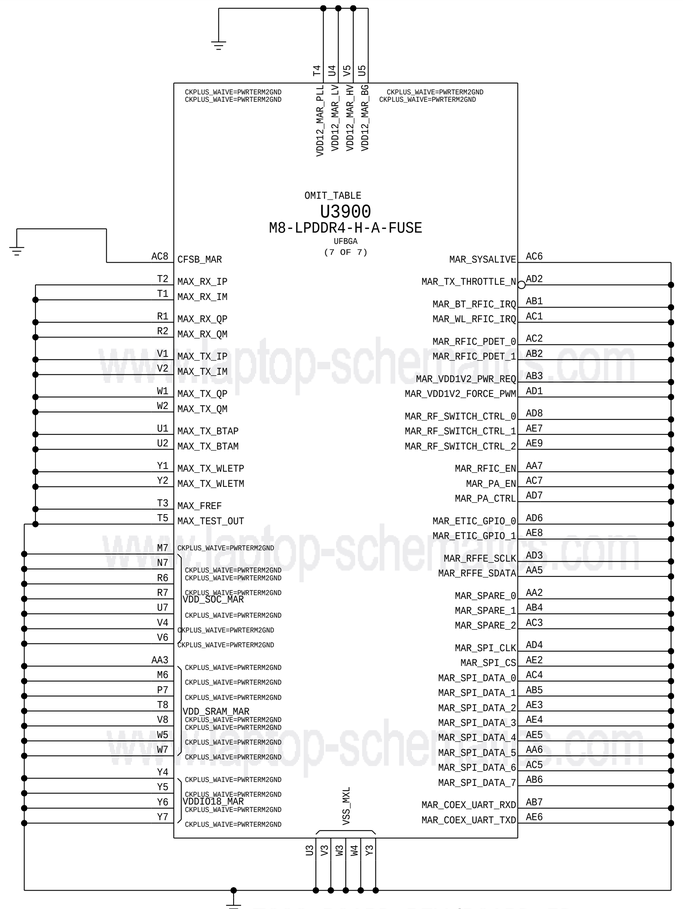
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00203	1	IC,FLASH,SERIAL,SPI,4MX8,4X3MM,DFN8	U3906		

BOM_COST_GROUP=T151

PAGE TITLE	Camera/DFR 1
Apple Inc.	
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	39 OF 145
SHEET	37 OF 119



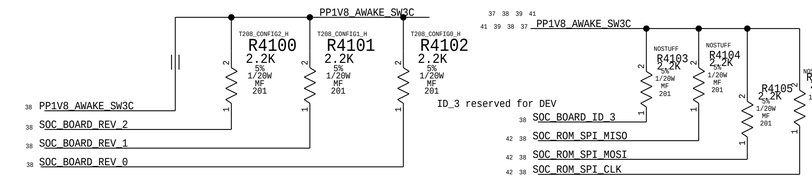




T208 BOARD REV/BOARD ID

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ
4. DISABLE PD AND ENABLE PU



BOARD REV[3:0]	MODE
1111	T208_Rev0 (X362 P0)
1110	T208_Rev1 (X363 P0)
1101	T208_Rev2 (X362 P1)
1100	T208_Rev3 (X362 P2)
1011	T208_Rev4 (X363 P2/X362 localEVT)
1010	T208_Rev5 (X363 EVT/X362 EVT1)

BOARD ID[3:0]	MODE
1XXX	T202 DEV
0010	T208

BOM GROUP	BOM OPTIONS
T208_PROG:REV0	T208_CONFIG2_H,T208_CONFIG1_H,T208_CONFIG0_H
T208_PROG:REV1	T208_CONFIG2_H,T208_CONFIG1_H
T208_PROG:REV2	T208_CONFIG2_H,T208_CONFIG0_H
T208_PROG:REV3	T208_CONFIG2_H
T208_PROG:REV4	T208_CONFIG1_H, T208_CONFIG0_H
T208_PROG:REV5	T208_CONFIG1_H

BOM_COST_GROUP=T151

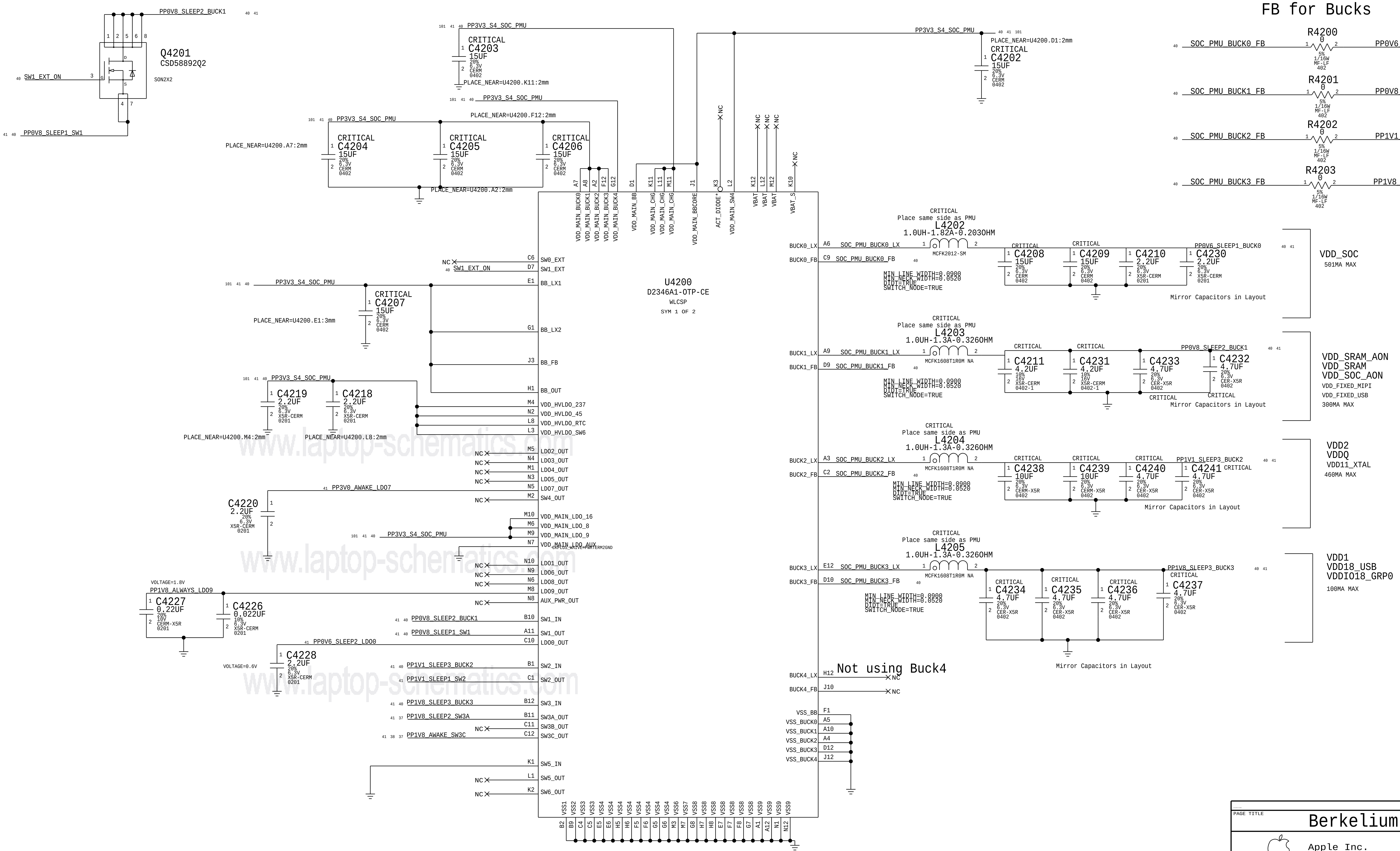
PAGE TITLE: Camera/DFR 3

Apple Inc.

DRAWING NUMBER: 051-00777 | SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 41 OF 145
SHEET: 39 OF 119

8 7 6 5 4 3 2 1

Berkelium



FB for Bucks
R4200 0 SOC_PMU_BUCK0_FB PP0V6_SLEEP1_BUCK0
R4201 0 SOC_PMU_BUCK1_FB PP0V8_SLEEP1_SW1
R4202 0 SOC_PMU_BUCK2_FB PP1V1_SLEEP3_BUCK2
R4203 0 SOC_PMU_BUCK3_FB PP1V8_SLEEP3_BUCK3
5% 1/16W MF-LF 402
Q4201 CSD58892Q2 SON2X2
PP0V8_SLEEP2_BUCK1
SW1_EXT_ON
PP0V8_SLEEP1_SW1
PP3V3_S4_SOC_PMU
CRITICAL C4203 15UF
PLACE_NEAR=U4200.K11:2mm
CRITICAL C4202 15UF
PLACE_NEAR=U4200.D1:2mm
CRITICAL C4204 15UF
CRITICAL C4205 15UF
CRITICAL C4206 15UF
PLACE_NEAR=U4200.A7:2mm
PLACE_NEAR=U4200.F12:2mm
PLACE_NEAR=U4200.A2:2mm
U4200 D2346A1-OTP-CE WLCSP SYM 1 OF 2
VDD_MAIN_BUCK0 VDD_MAIN_BUCK1 VDD_MAIN_BUCK2 VDD_MAIN_BUCK3 VDD_MAIN_BUCK4 VDD_MAIN_BB VDD_MAIN_CHG VDD_MAIN_BBCORE ACT_DIODE VDD_MAIN_SW4 VBAT VBAT_S
SW0_EXT SW1_EXT BB_LX1 BB_LX2 BB_FB BB_OUT
VDD_HVLDO_237 VDD_HVLDO_45 VDD_HVLDO_RTC VDD_HVLDO_SW6
LDO2_OUT LDO3_OUT LDO4_OUT LDO5_OUT LDO7_OUT SW4_OUT
VDD_MAIN_LDO_16 VDD_MAIN_LDO_8 VDD_MAIN_LDO_9 VDD_MAIN_LDO_AUX
LDO1_OUT LDO6_OUT LDO8_OUT LDO9_OUT AUX_PWR_OUT
SW1_IN SW1_OUT LDO0_OUT SW2_IN SW2_OUT SW3_IN SW3A_OUT SW3B_OUT SW3C_OUT SW5_IN SW5_OUT SW6_OUT
CRITICAL C4207 15UF PLACE_NEAR=U4200.E1:3mm
C4219 2.2UF C4218 2.2UF PLACE_NEAR=U4200.M4:2mm PLACE_NEAR=U4200.L8:2mm
C4220 2.2UF PP3V0_AWAKE_LDO7
VOLTAGE=1.8V PP1V8_ALWAYS_LDO9 C4227 0.22UF C4226 0.022UF
PP0V8_SLEEP2_BUCK1 PP0V8_SLEEP1_SW1 PP0V6_SLEEP2_LDO0
VOLTAGE=0.6V C4228 2.2UF
PP1V1_SLEEP3_BUCK2 PP1V1_SLEEP1_SW2 PP1V8_SLEEP3_BUCK3 PP1V8_SLEEP2_SW3A PP1V8_AWAKE_SW3C
BUCK0_LX BUCK0_FB BUCK1_LX BUCK1_FB BUCK2_LX BUCK2_FB BUCK3_LX BUCK3_FB BUCK4_LX BUCK4_FB
VSS_BB VSS_BUCK0 VSS_BUCK1 VSS_BUCK2 VSS_BUCK3 VSS_BUCK4
CRITICAL Place same side as PMU L4202 1.0UH-1.82A-0.203OHM MCFK2012-SM
C4208 15UF C4209 15UF C4210 2.2UF C4230 2.2UF PP0V6_SLEEP1_BUCK0
MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 DIDT=TRUE SWITCH_NODE=TRUE
Mirror Capacitors in Layout
VDD_SOC 501MA MAX
CRITICAL Place same side as PMU L4203 1.0UH-1.3A-0.326OHM MCFK1608T1R0M NA
C4211 4.2UF C4231 4.2UF C4233 4.7UF C4232 4.7UF PP0V8_SLEEP2_BUCK1
VDD_SRAM_AON VDD_SRAM VDD_SOC_AON VDD_FIXED_MIPI VDD_FIXED_USB 300MA MAX
CRITICAL Place same side as PMU L4204 1.0UH-1.3A-0.326OHM
C4238 10UF C4239 10UF C4240 4.7UF C4241 4.7UF PP1V1_SLEEP3_BUCK2
VDD2 VDDQ VDD11_XTAL 460MA MAX
CRITICAL Place same side as PMU L4205 1.0UH-1.3A-0.326OHM
C4234 4.7UF C4235 4.7UF C4236 4.7UF C4237 4.7UF PP1V8_SLEEP3_BUCK3
VDD1 VDD18_USB VDDIO18_GRP0 100MA MAX
Not using Buck4

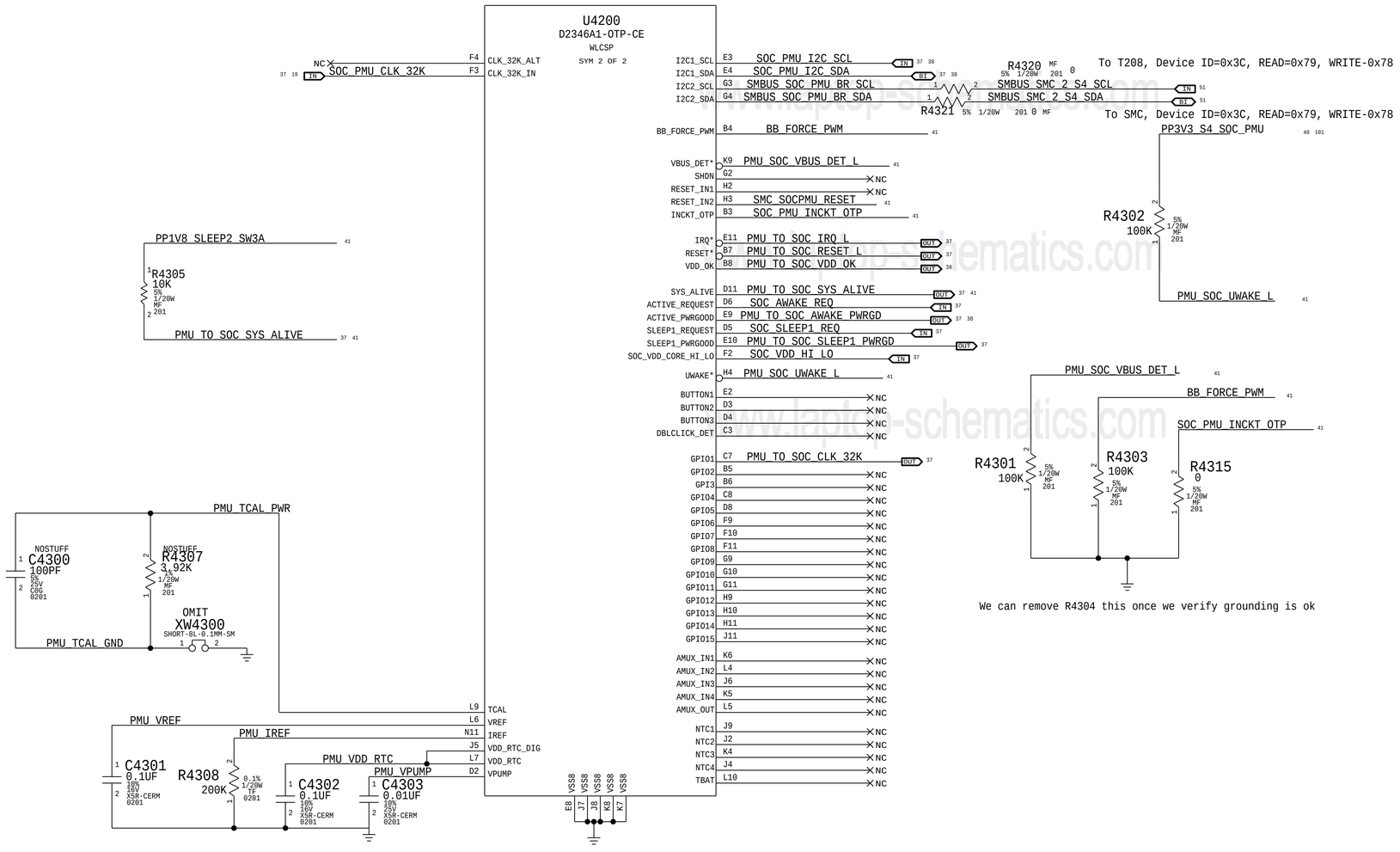
BOM_COST_GROUP=T151

PAGE TITLE	Berkelium - 1
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	42 OF 145
SHEET	40 OF 119

Apple Inc.

8 7 6 5 4 3 2 1

Berkelium - 2



T208 POWER ALIASES

BUCK0
- PP0V6_SLEEP1_BUCK0 = PP0V6_SLEEP1_BUCK0 (VOLTAGE=0.6V, MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE)

BUCK1
- PP0V8_SLEEP2_BUCK1 = PP0V8_SLEEP2_BUCK1 (VOLTAGE=0.8V, MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE)
- LDO0
  - PP0V6_SLEEP2_LDO0 = PP0V6_SLEEP2_LDO0 (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE, VOLTAGE=0.6V)
- SW1
  - PP0V8_SLEEP1_SW1 = PP0V8_SLEEP1_SW1 (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE, VOLTAGE=0.8V)
  - PP0V8_SLEEP1_SW1
  - PP0V8_SLEEP1_SW1
  - PP0V8_SLEEP1_SW1

BUCK2
- PP1V1_SLEEP3_BUCK2 = PP1V1_SLEEP3_BUCK2 (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE, VOLTAGE=1.1V)
- PP1V1_SLEEP3_BUCK2
- SW2
  - PP1V1_SLEEP1_SW2 = PP1V1_SLEEP1_SW2 (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE, VOLTAGE=1.1V)
  - PP1V1_SLEEP1_SW2
  - PP1V1_SLEEP1_SW2
  - PP1V1_SLEEP1_SW2
  - PP1V1_SLEEP1_SW2
  - PP1V1_SLEEP1_SW2

BUCK3
- PP1V8_SLEEP3_BUCK3 = PP1V8_SLEEP3_BUCK3 (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE, VOLTAGE=1.8V)
- SW3A
  - PP1V8_SLEEP2_SW3A = PP1V8_SLEEP2_SW3A (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE, VOLTAGE=1.8V)
  - PP1V8_SLEEP2_SW3A
  - PP1V8_SLEEP2_SW3A
- SW3C
  - PP1V8_AWAKE_SW3C = PP1V8_AWAKE_SW3C (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE, VOLTAGE=1.8V)
  - PP1V8_AWAKE_SW3C
  - PP1V8_AWAKE_SW3C

LDO7
- PP3V0_AWAKE_LDO7 = PP3V0_AWAKE_LDO7 (MIN_LINE_WIDTH=0.0900, MIN_NECK_WIDTH=0.0520, MAKE_BASE=TRUE, VOLTAGE=3.0V)

Signal Aliases

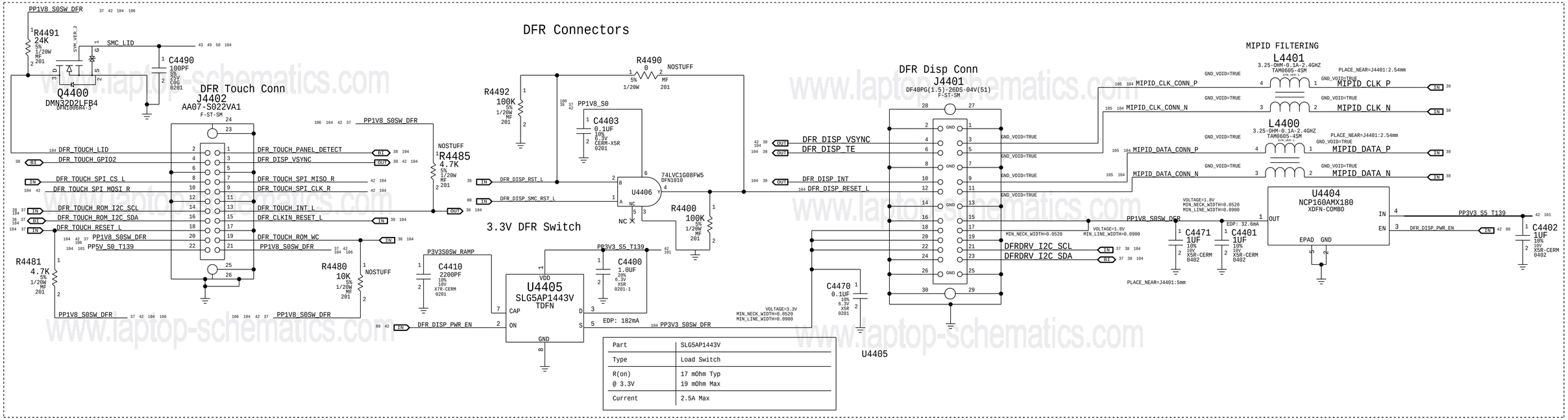
- SMC_SOCPMU_RESET = SMC_SOCPMU_RESET (MAKE_BASE=TRUE)

BOM_COST_GROUP=T151

PAGE TITLE	Berkelium - 2
	Apple Inc.
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	43 OF 145
SHEET	41 OF 119

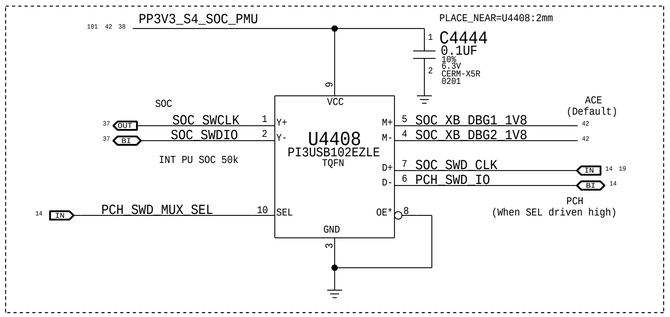
T208 Support

DFR Connectors



Part	SLG5AP1443V
Type	Load Switch
R(on) @ 3.3V	17 mOhm Typ 19 mOhm Max
Current	2.5A Max

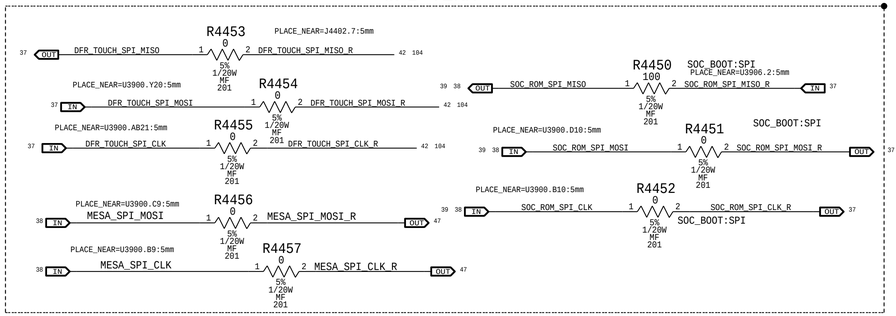
SWD DEBUG MUX



T208 I2C Mapping

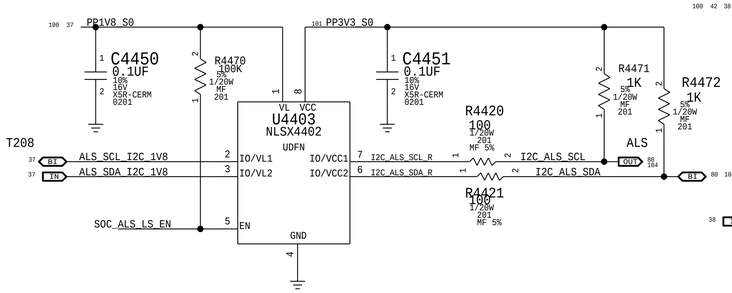
Bus	Device	7-bit Address	8-bit Address Read	8-bit Address Write
AP0	PMU	0011110 (0x3C)	0x79	0x78
AP1	Touch EEPROM	1010000 (0x50)	0xA1	0xA0
AP2_0	Tesla	1010100 (0x4C)	0x99	0x98
AOP0	Mesa EEPROM	101000x (0x50/0x51)	0xA1/A3	0xA0/A2
AOP1	ALS	0111001 (0x39)	0x73	0x72
SEP	M34128 EEPROM	1010001 (0x51)	0xA3	0xA2

SPI TERM

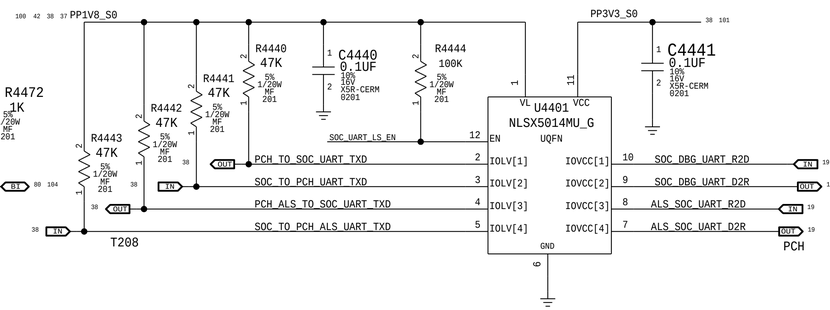


T208 LEVEL SHIFTING

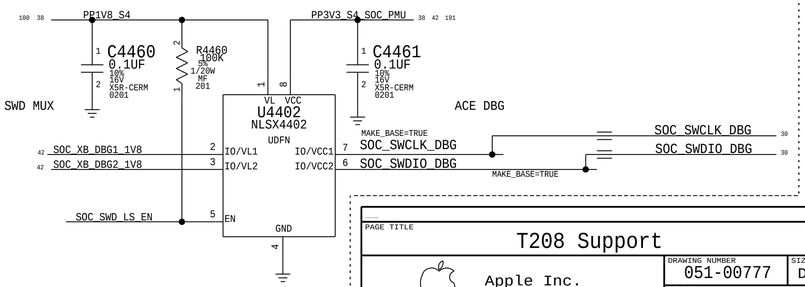
ALS I2C



ALS/DEBUG UART



ACE SWD DBG



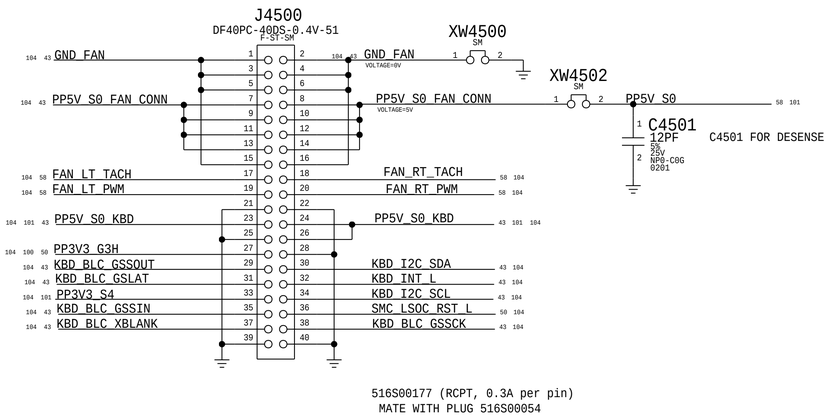
BOM_COST_GROUP=T151

PAGE TITLE: T208 Support

Apple Inc.

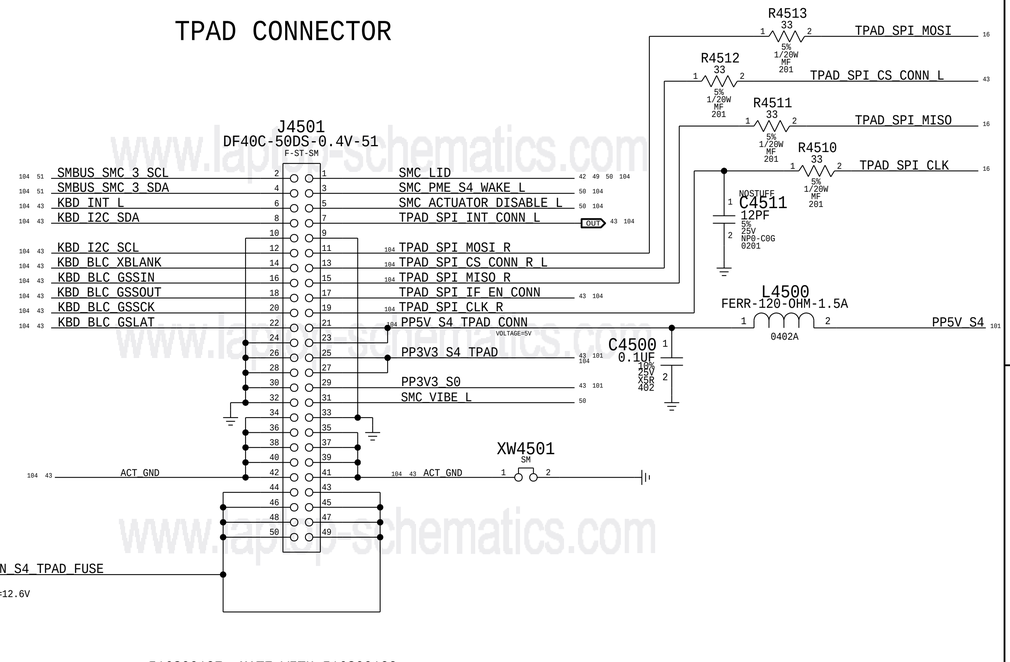
DRAWING NUMBER: 051-00777 | SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 44 OF 145
SHEET: 42 OF 119

KBD CONNECTOR



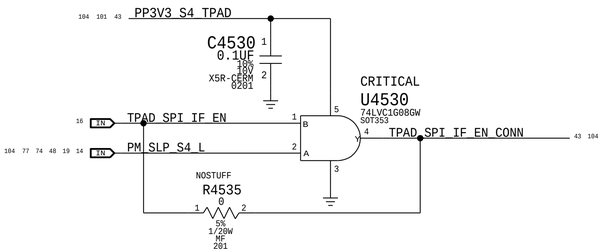
516S00177 (RCPT, 0.3A per pin)
MATE WITH PLUG 516S00054

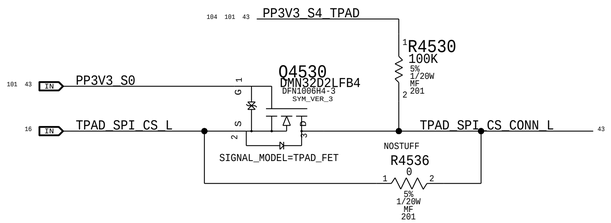
TPAD CONNECTOR

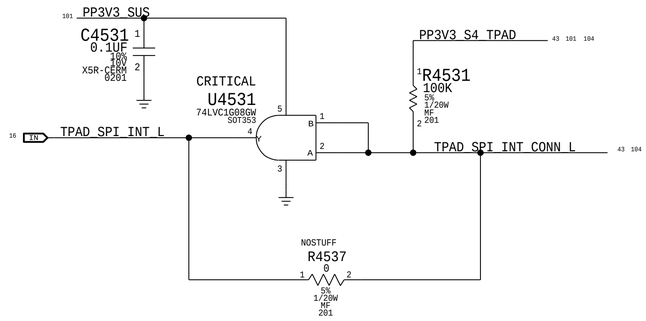


516S00187, MATE WITH 516S00188

TRACKPAD ISOLATION







BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=J79_GAREN SYNC_DATE=11/21/2015

PAGE TITLE: Connectors&ESD

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 45 OF 145
SHEET: 43 OF 119

8	7	6	5	4	3	2	1

D

C

B

A

SYNC_MASTER=J79_DAYU SYNC_DATE=05/26/2015

PAGE TITLE

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Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 46 OF 145

SHEET 44 OF 119

SYNC_MASTER=J79_DAYU	SYNC_DATE=05/26/2015
PAGE TITLE: Empty	
Apple Inc.	DRAWING NUMBER: 051-00777 / SIZE: D
	REVISION: 9.0.0
	BRANCH: dvt-fab09-0
	PAGE: 47 OF 145
	SHEET: 45 OF 119

8	7	6	5	4	3	2	1

D

C

B

A

SYNC_MASTER=J79_DAYU SYNC_DATE=05/12/2015

PAGE TITLE

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DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

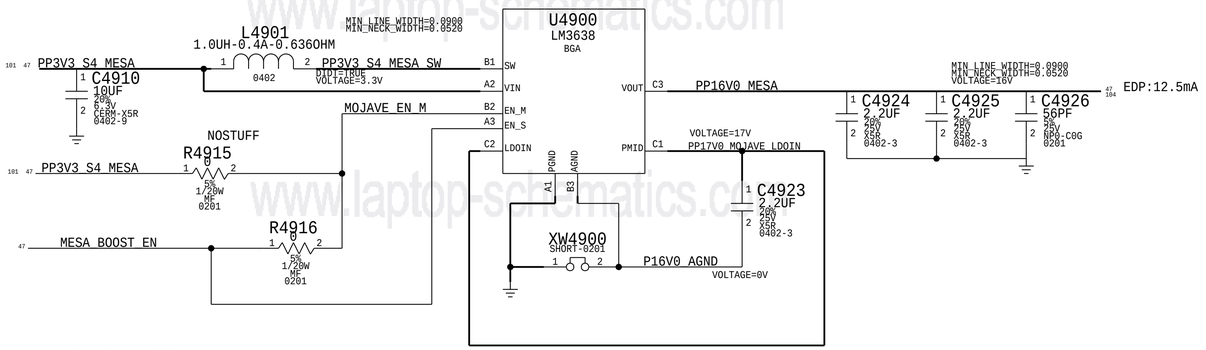
PAGE 48 OF 145

SHEET 46 OF 119

8 7 6 5 4 3 2 1

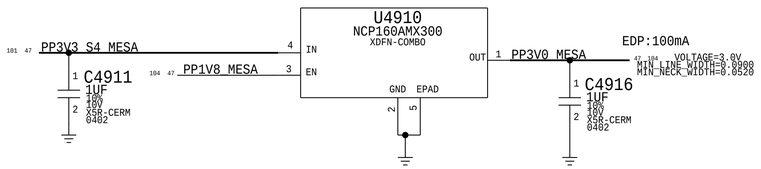
ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

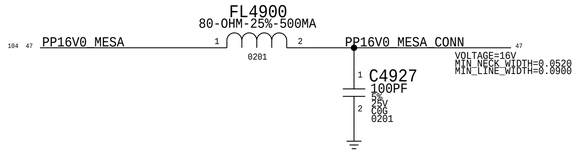
MOJAVE 16V BOOST

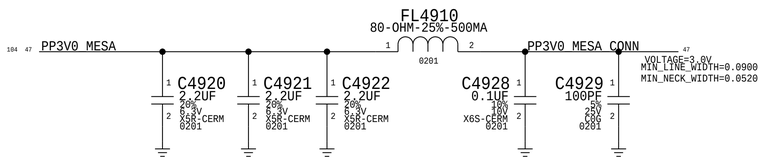


3.0V MESA

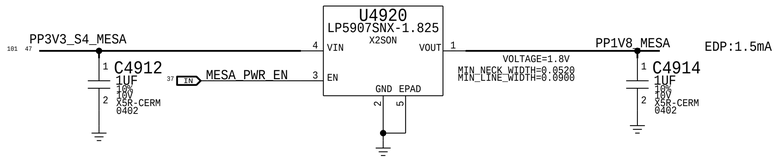
Option to feed LDO from 5V in case of dropout issue

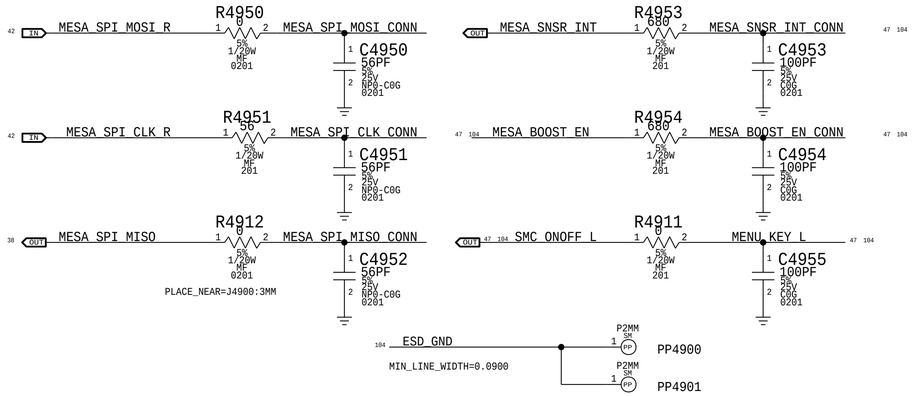






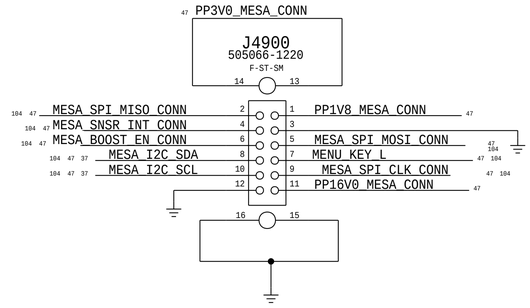
1.8V MESA





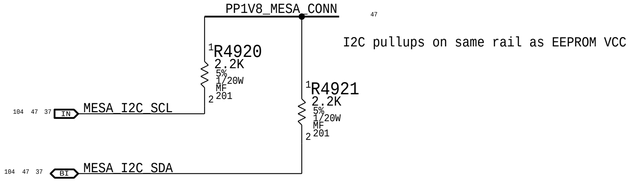
MESA FLEX CONNECTOR

Proto1 Connector for X434/X435 Support
PLUG (516S00115) - X434/ X435 Jumper
Recptacle (516S00203) - X362/X363 MLB



Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0



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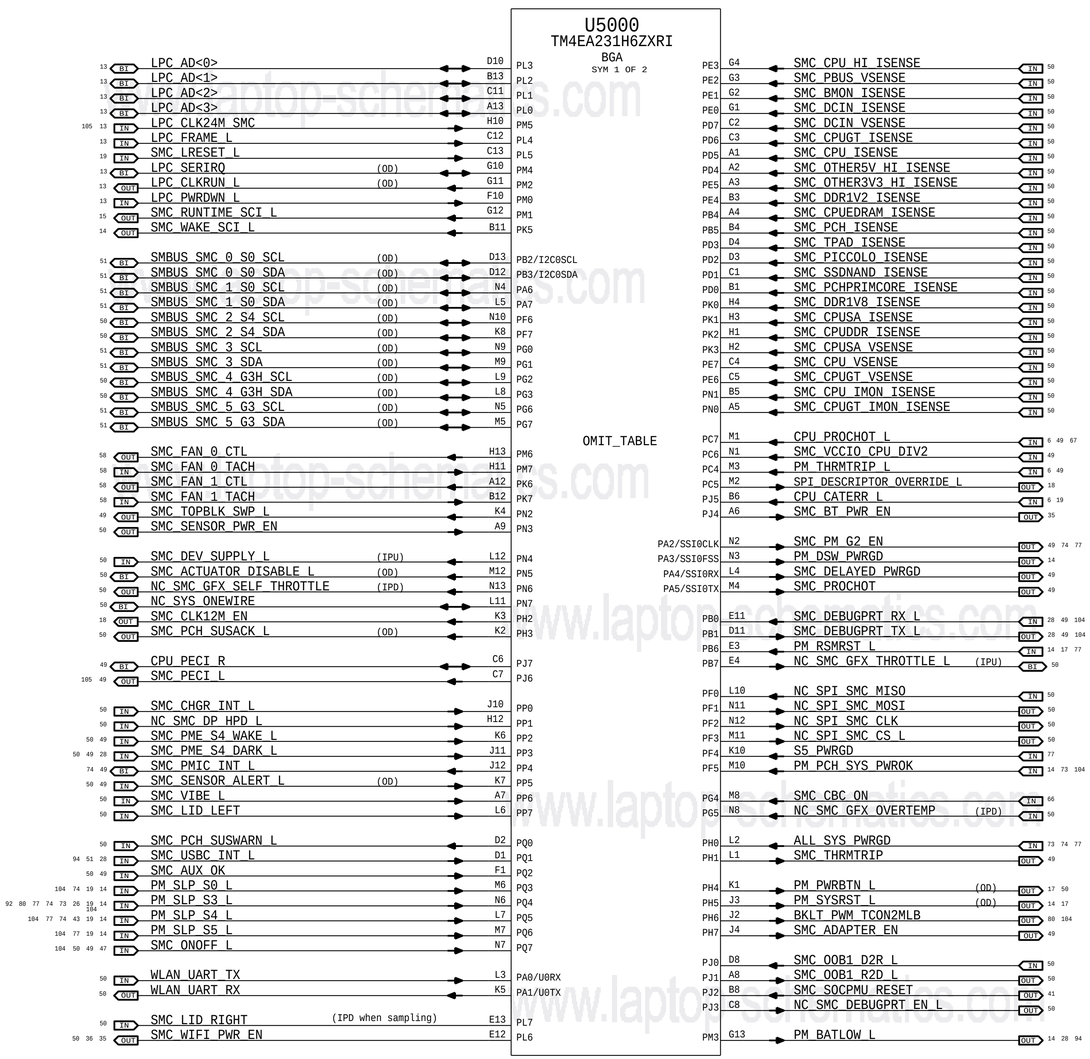
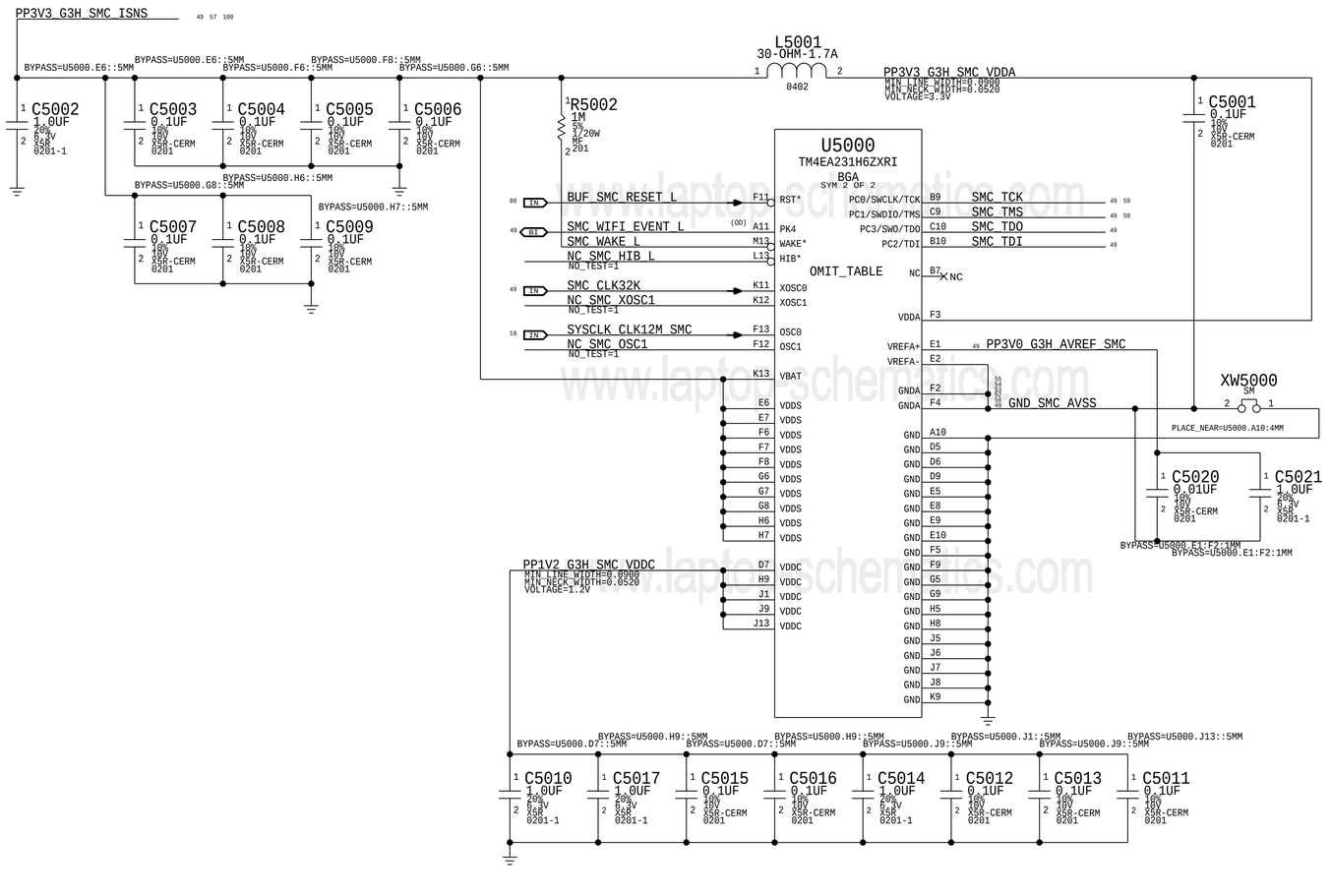
PAGE TITLE: MESA

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 49 OF 145
SHEET: 47 OF 119





NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

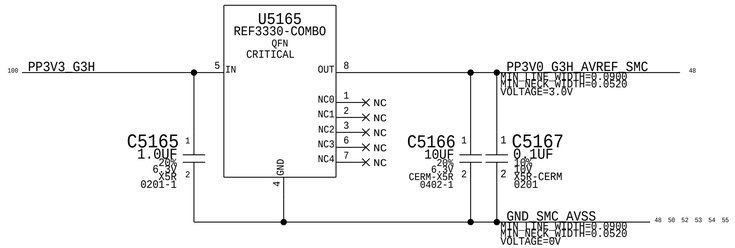
NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

PAGE TITLE
SMC

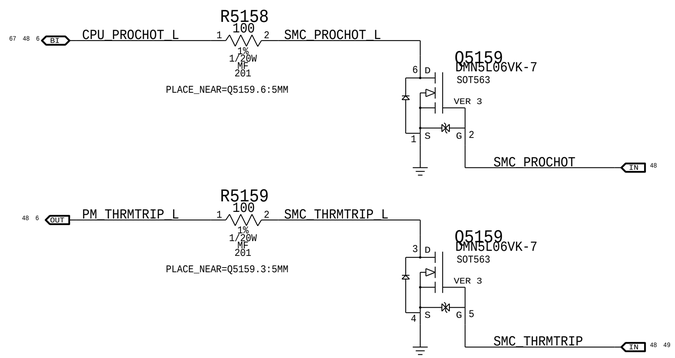
Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 50 OF 145
SHEET 48 OF 119

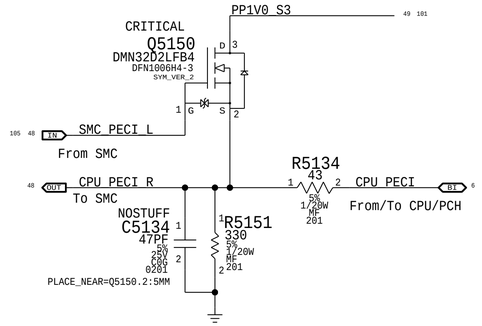
SMC AVREF Supply



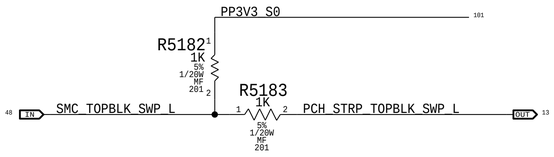
PROCHOT/THRMTRIP Support

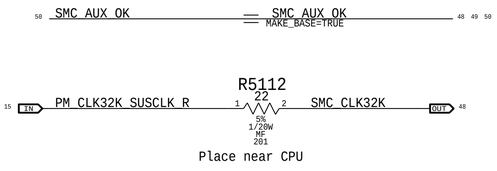


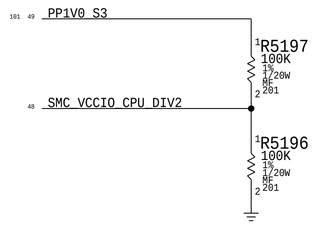
PECI Support

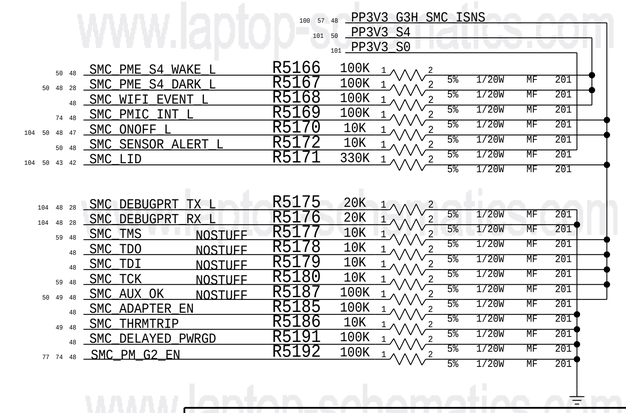


Top-Block Swap









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SYNC_MASTER=J79_JACK SYNC_DATE=04/14/2016

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 51 OF 145
SHEET: 49 OF 119

SMC12 ADC Assignments

SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE	MAKE_BASE=TRUE	
SMC_BMON_ISENSE	SMC_BMON_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE	MAKE_BASE=TRUE	
SMC_CPUGT_ISENSE	SMC_CPUGT_ISENSE	MAKE_BASE=TRUE	
SMC_CPU_ISENSE	SMC_CPU_ISENSE	MAKE_BASE=TRUE	
SMC_OTHER5V_HI_ISENSE	SMC_OTHER5V_HI_ISENSE	MAKE_BASE=TRUE	
SMC_OTHER3V3_HI_ISENSE	SMC_OTHER3V3_HI_ISENSE	MAKE_BASE=TRUE	
SMC_DDR1V2_ISENSE	SMC_DDR1V2_ISENSE	MAKE_BASE=TRUE	
SMC_CPUEDRAM_ISENSE	SMC_CPUEDRAM_ISENSE	MAKE_BASE=TRUE	
SMC_PCH_ISENSE	SMC_PCH_ISENSE	MAKE_BASE=TRUE	
SMC_TPAD_ISENSE	SMC_TPAD_ISENSE	MAKE_BASE=TRUE	
SMC_PICCOLO_ISENSE	SMC_PICCOLO_ISENSE	MAKE_BASE=TRUE	
SMC_SSDNAND_ISENSE	SMC_SSDNAND_ISENSE	MAKE_BASE=TRUE	
SMC_PCHPRIMCORE_ISENSE	SMC_PCHPRIMCORE_ISENSE	MAKE_BASE=TRUE	
SMC_DDR1V8_ISENSE	SMC_DDR1V8_ISENSE	MAKE_BASE=TRUE	
SMC_CPUSA_ISENSE	SMC_CPUSA_ISENSE	MAKE_BASE=TRUE	
SMC_CPUDDR_ISENSE	SMC_CPUDDR_ISENSE	MAKE_BASE=TRUE	
SMC_CPUSA_VSENSE	SMC_CPUSA_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_VSENSE	SMC_CPU_VSENSE	MAKE_BASE=TRUE	
SMC_CPUGT_VSENSE	SMC_CPUGT_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_IMON_ISENSE	SMC_CPU_IMON_ISENSE	MAKE_BASE=TRUE	
SMC_CPUGT_IMON_ISENSE	SMC_CPUGT_IMON_ISENSE	MAKE_BASE=TRUE	

SMC12 Pin Assignments

NC_SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NO_TEST=1
NC_SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	MAKE_BASE=TRUE	NO_TEST=1
NC_SMC_GFX_SELF_THROTTLE	NC_SMC_GFX_SELF_THROTTLE	MAKE_BASE=TRUE	NO_TEST=1
NC_SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE	NO_TEST=1
NC_SYS_ONEWIRE	NC_SYS_ONEWIRE	MAKE_BASE=TRUE	NO_TEST=1
NC_SMC_DEBUGPRT_EN_L	NC_SMC_DEBUGPRT_EN_L	MAKE_BASE=TRUE	NO_TEST=1
SMC_LID_RIGHT	SMC_LID_RIGHT	MAKE_BASE=TRUE	
NC_SPI_SMC_MISO	NC_SPI_SMC_MISO	NO_TEST=1	TRUE
NC_SPI_SMC_MOSI	NC_SPI_SMC_MOSI	NO_TEST=1	TRUE
NC_SPI_SMC_CLK	NC_SPI_SMC_CLK	NO_TEST=1	TRUE
NC_SPI_SMC_CS_L	NC_SPI_SMC_CS_L	NO_TEST=1	TRUE
SMC_VIBE_L	SMC_VIBE_L	MAKE_BASE=TRUE	
SMC_PCH_SUSWARN_L	SMC_PCH_SUSWARN_L	MAKE_BASE=TRUE	
SMC_PCH_SUSACK_L	SMC_PCH_SUSACK_L	MAKE_BASE=TRUE	
SMC_SENSOR_PWR_EN	SMC_SENSOR_PWR_EN	MAKE_BASE=TRUE	
WLAN_UART_RX	WLAN_UART_RX	MAKE_BASE=TRUE	
WLAN_UART_TX	WLAN_UART_TX	MAKE_BASE=TRUE	
SMC_AUX_OK	SMC_AUX_OK	MAKE_BASE=TRUE	
PM_PWRBTN_L	PM_PWRBTN_L	MAKE_BASE=TRUE	
SMC_AUX_OK	SMC_AUX_OK	MAKE_BASE=TRUE	
SMBUS_SMC_4_G3H_SCL	SMBUS_SMC_4_G3H_SCL	MAKE_BASE=TRUE	
SMBUS_SMC_4_G3H_SDA	SMBUS_SMC_4_G3H_SDA	MAKE_BASE=TRUE	
SMBUS_SMC_2_S4_SCL	SMBUS_SMC_2_S4_SCL	MAKE_BASE=TRUE	
SMBUS_SMC_2_S4_SDA	SMBUS_SMC_2_S4_SDA	MAKE_BASE=TRUE	
SMC_OOB1_D2R_L	SMC_OOB1_D2R_L	MAKE_BASE=TRUE	
SMC_OOB1_R2D_L	SMC_OOB1_R2D_L	MAKE_BASE=TRUE	
SMC_ACTUATOR_DISABLE_L	SMC_ACTUATOR_DISABLE_L	MAKE_BASE=TRUE	
SMC_CHGR_INT_L	SMC_CHGR_INT_L	MAKE_BASE=TRUE	

Debug Power "Buttons"

DEBUG_BUTTON
PLACE_SIDE=TOP
SILK_PART=PWR_BTN
CRITICAL
R5226 SOX-152HNT SM
SMC_ONOFF_L
PLACE_SIDE=BOTTOM
SILK_PART=PWR_BTN
CRITICAL
R5225 SOX-152HNT SM
DEBUG_BUTTON

Debug RESET "Buttons"

DEBUG_BUTTON
PLACE_SIDE=BOTTOM
SILK_PART=RESET_BTN
CRITICAL
SW5227 SOX-152HNT SM
SMC_RESET_L

Thermal Alerts

NOSTUFF R5217 100 5% 1/20W MF 201
R5216 100 5% 1/20W MF 201
R5214 100 5% 1/20W MF 201
R5220 100 5% 1/20W MF 201
R5210 100 5% 1/20W MF 201
R5221 100 5% 1/20W MF 201
R5211 100 5% 1/20W MF 201

SMC_CPUHI_COMP_ALERT_L	
CPUTHMSNS_THM_L	CPUTHRM_THRM:SMC
CPUTHMSNS_ALERT_L	CPUTHRM_ALRT:SMC
TBTTHMSNS_THM_L	TBTTHRM_THRM:SMC
TBTTHMSNS_ALERT_L	TBTTHRM_ALRT:SMC
TBTTHMSNS_THM_T_L	TBTTHRM_THRM:SMC
TBTTHMSNS_ALERT_T_L	TBTTHRM_ALRT:SMC
	SMC_SENSOR_ALERT_L

PP3V3_G3H
BYPASS=U5256.5::5MM
R5258 100K 5% 1/20W MF 201
C5256 0.1UF 10% 10V X5R-CERM 0201
SN74LVC1G02 SOT553-5
SMC_LSOC_RST_L
SMC_ONOFF_L
SMC_4FINGERS_RST
U5256 CRITICAL

S4 SMC Wake Sources

SMC_PME_S4_WAKE_L	SMC_PME_S4_WAKE_L
SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L

R5256 0 5% 1/20W MF 0201
SMC_LID_LEFT_R
SMC_LID_LEFT
PP3V3_G3H
BYPASS=U5255.6::5MM
C5255 0.1UF 10% 10V X5R-CERM 0201
NOSTUFF R5257 0 5% 1/20W MF 0201
R5251 10K 5% 1/20W MF 201
HALL_SENSOR_LEFT
U5255 74LVC1G32 SOT891
SMC_LID_R
R5255 10K 5% 1/20W MF 201
SMC_LID
R5261 10K 5% 1/20W MF 201
HALL_SENSOR_RIGHT
NC
CRITICAL
SMC_LID_RIGHT
R5259 0 5% 1/20W MF 0201
SMC_DEV_SUPPLY_L
TP_SMC_DEV_SUPPLY_L

Hall Effect Pads - Left

J5250 AMR-MLB-X502 SM
HALL_SENSOR_LEFT
PP3V3_G3H
OMIT_TABLE
NOSTUFF C5250 1000PF 10% 10V X7R-1 0201

Hall Effect Pads - Right

J5260 AMR-MLB-X502 SM
HALL_SENSOR_RIGHT
PP3V3_G3H
OMIT_TABLE
NOSTUFF C5260 1000PF 10% 10V X7R-1 0201

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-04255	2	SUBASSY (T&R) PCBA,HES INTERPOSER,X502	J5250, J5260	CRITICAL	

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:PU
CPUTHRM:ALRT	CPUTHRM_ALRT:SMC
CPUTHRM:NONE	CPUTHRM_ALRT:PU

Specify one of these BOM GROUPs.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU

Requires EMC1412-1 or EMC1412-2 instead of EMC1412-A, new APN needs to be created.

R5273 10K 5% 1/20W MF 201
WLAN_UART_RX
R5274 100K 5% 1/20W MF 201
WLAN_UART_TX
PP3V3_S4

R5295 10K 5% 1/20W MF 201
SMC_WIFI_PWR_EN
R5294 10K 5% 1/20W MF 201
SMC_SENSOR_PWR_EN

NOSTUFF C5270 1000PF 10% 10V X7R-CERM 0201
SMC_RESET_L
GND_SMC_AVSS

BOM_COST_GROUP=SMC

PAGE TITLE
PAGE_TITLE=SMC Project Support

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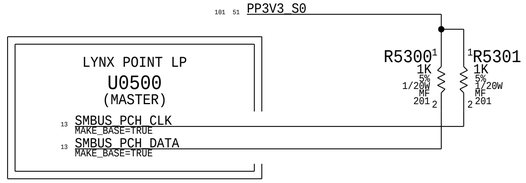
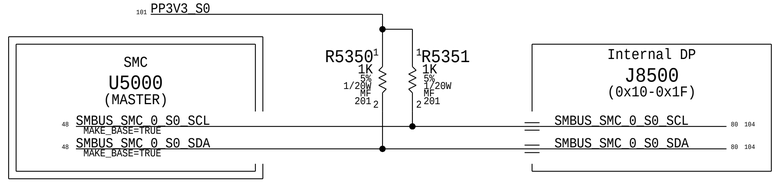
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	52 OF 145
SHEET	50 OF 119

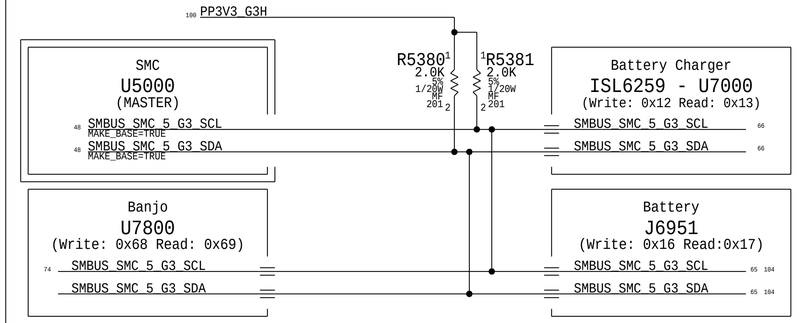
LYNX POINT LP S0 "SMBus 0" Connections



SMC SMBus "0" S0 Connections

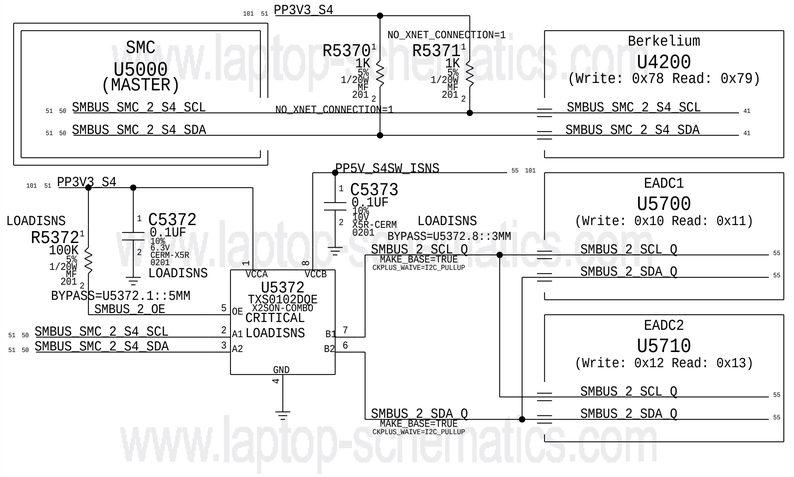


SMC SMBus "5" G3H Connections

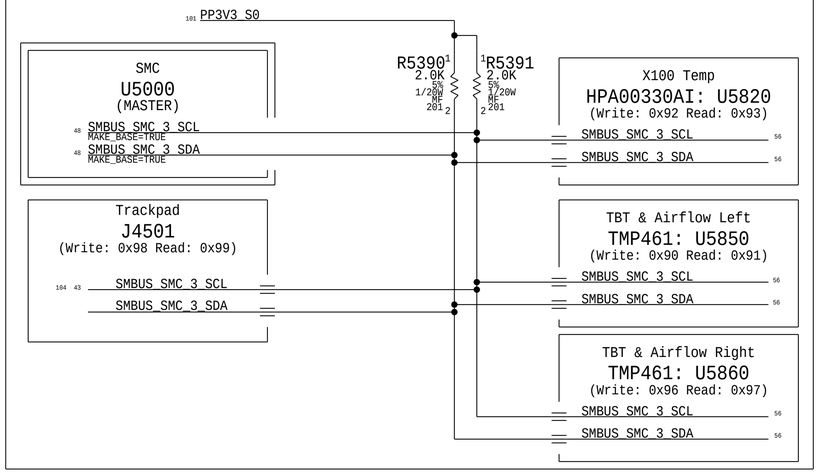


ACE I2C Interrupt

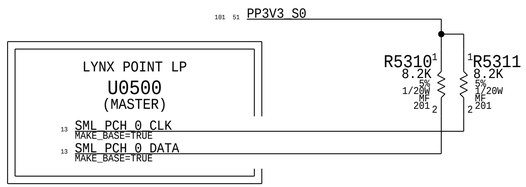
SMC SMBus "2" S4 Connections



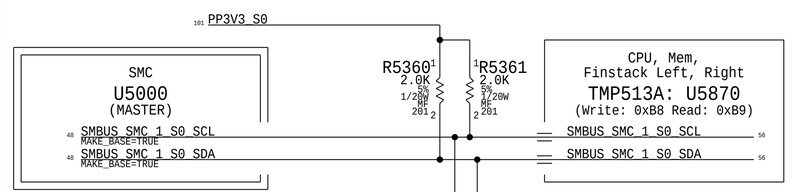
SMC SMBus "3" S0 Connections



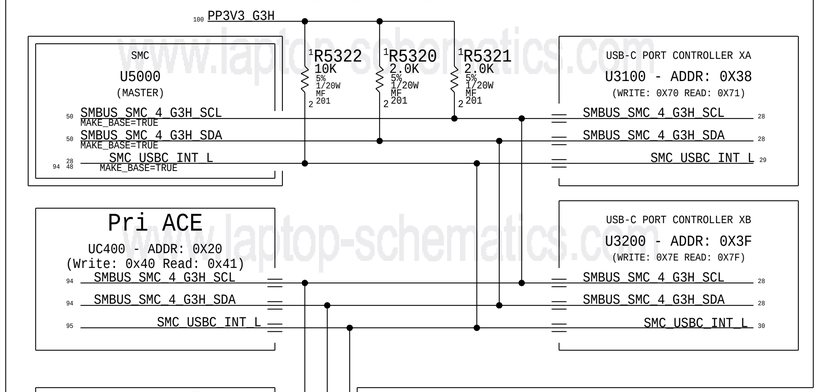
LYNX POINT LP S0 "SMLink 0" Connections



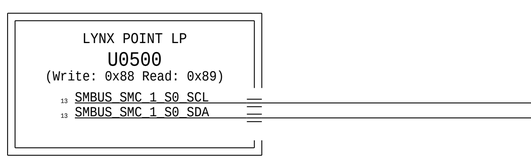
SMC SMBus "1" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



LYNX POINT LP S0 "SMLink 1" Connections



SMLink 1 is slave port to
access PCH.

BOM_COST_GROUP=SMC

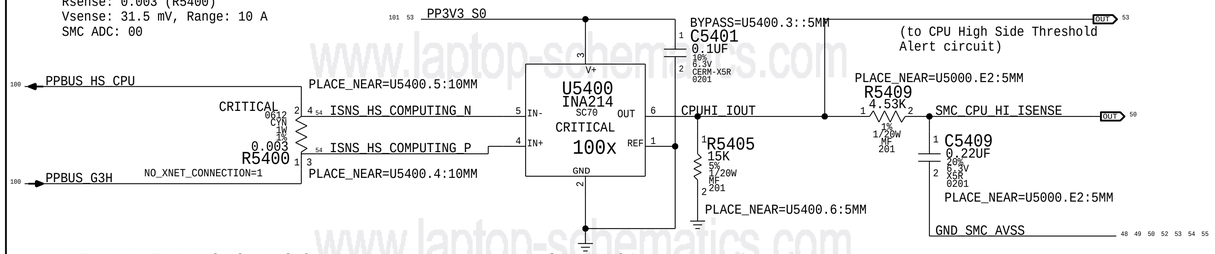
PAGE TITLE: SMBus Connections

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 53 OF 145
SHEET: 51 OF 119

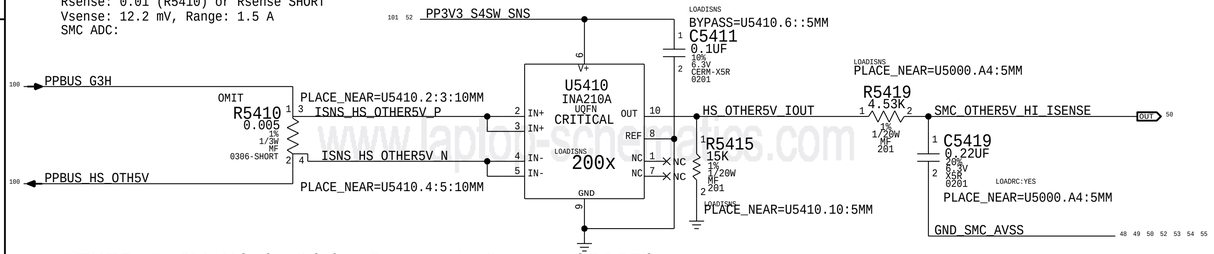
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 10.5 A
Rsense: 0.003 (R5400)
Vsense: 31.5 mV, Range: 10 A
SMC ADC: 00



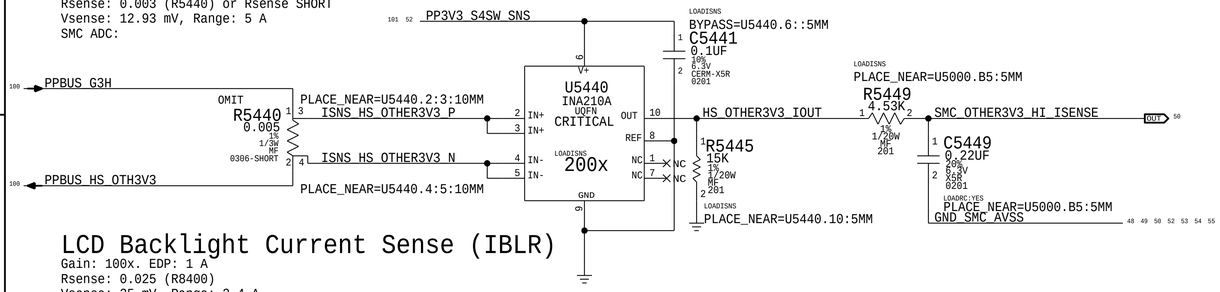
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.22 A
Rsense: 0.01 (R5410) or Rsense SHORT
Vsense: 12.2 mV, Range: 1.5 A
SMC ADC:



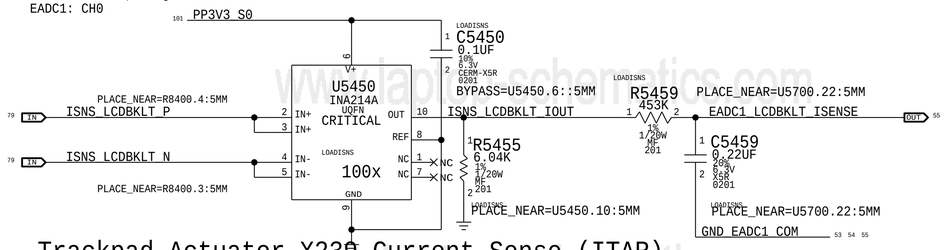
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 4.31 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 12.93 mV, Range: 5 A
SMC ADC:



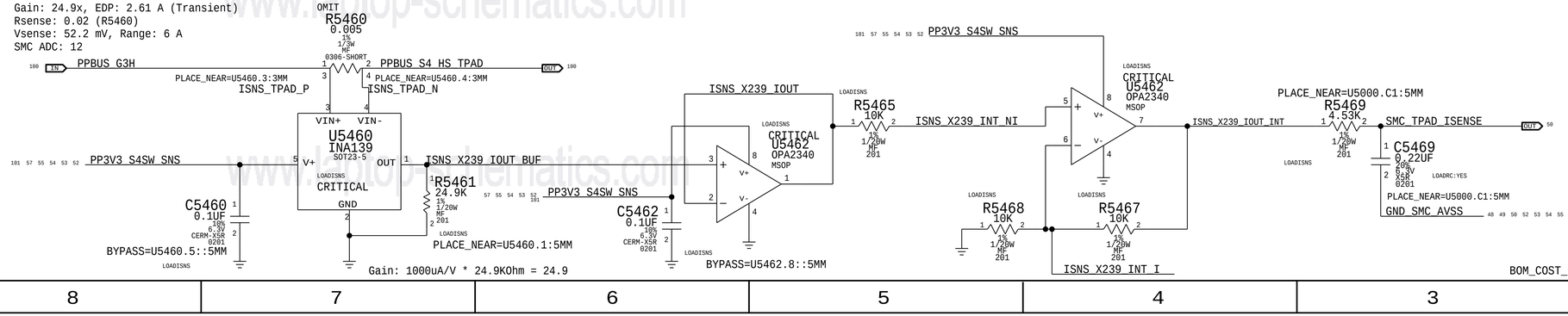
LCD Backlight Current Sense (IBLR)

Gain: 100x. EDP: 1 A
Rsense: 0.025 (R8400)
Vsense: 25 mV, Range: 2.4 A
EADC1: CH0



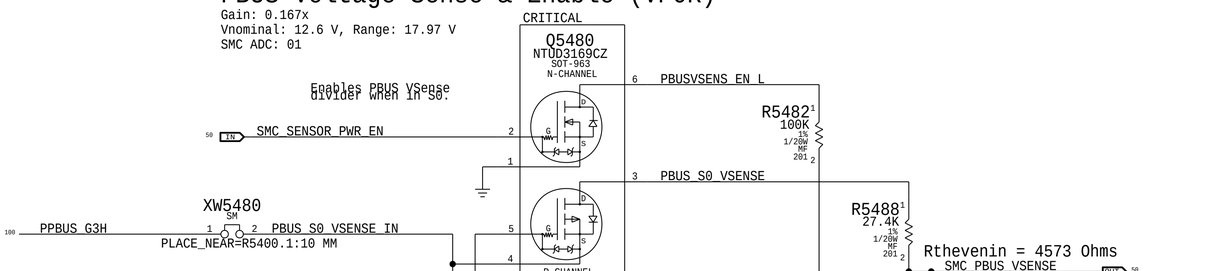
Trackpad Actuator X239 Current Sense (ITAR)

Gain: 24.9x, EDP: 2.61 A (Transient)
Rsense: 0.02 (R5460)
Vsense: 52.2 mV, Range: 6 A
SMC ADC: 12



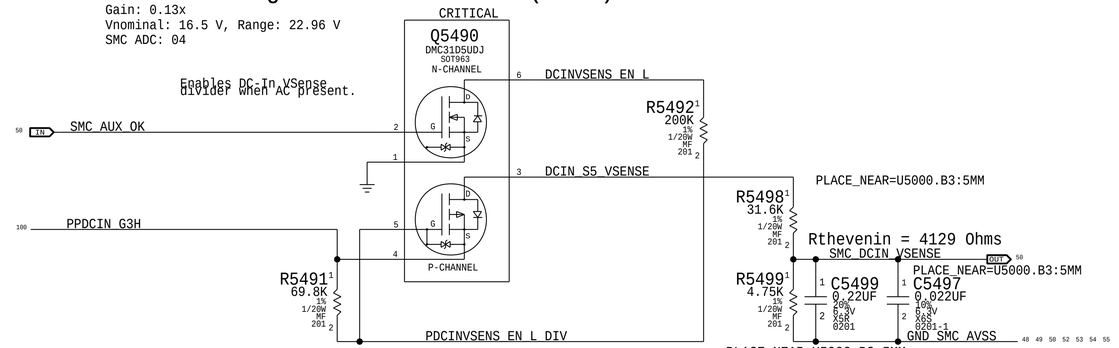
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 17.97 V
SMC ADC: 01



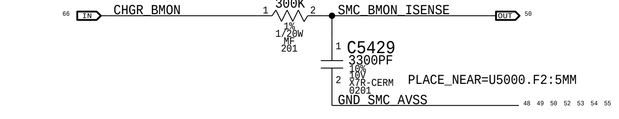
DC In Voltage Sense & Enable (VD0R)

Gain: 0.13x
Vnominal: 16.5 V, Range: 22.96 V
SMC ADC: 04



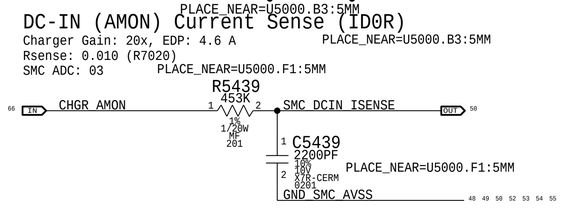
Charger (BMON) Current Sense (IPBR)

Charger Gain: 20x, EDP: 7.2 A
Rsense: 0.005 (R7060)
SMC ADC: 02



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.010 (R7020)
SMC ADC: 03



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		LOADRC:NO

BOM_COST_GROUP=SENSORS

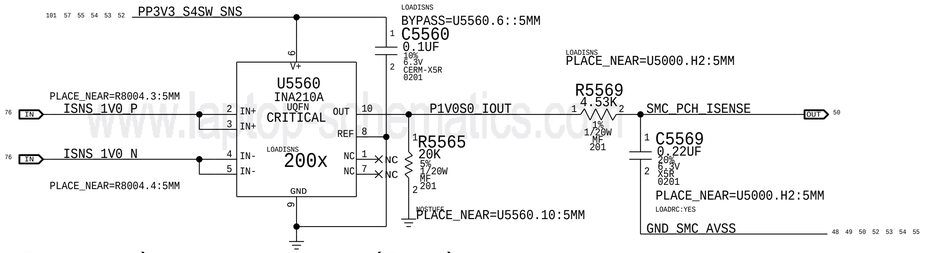
PAGE TITLE
Power Sensors: High Side

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 54 OF 145
SHEET 52 OF 119

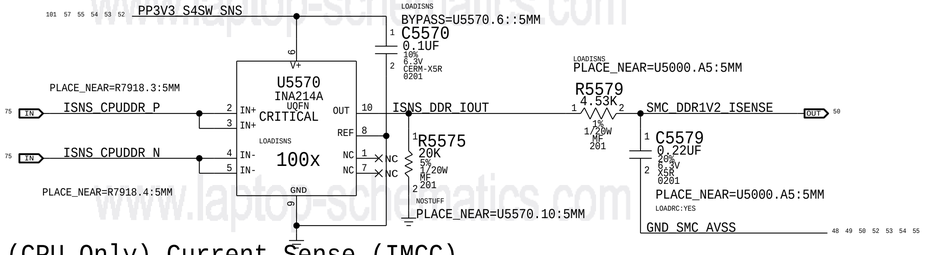
PCH 1.0V Current Sense (IS1C)

Gain: 200x, EDP: 3.29 A
Rsense: 0.003 (R8004) or Rsense SHORT
Vsense: 9.87 mV, Range: 5 A
SMC ADC: 11



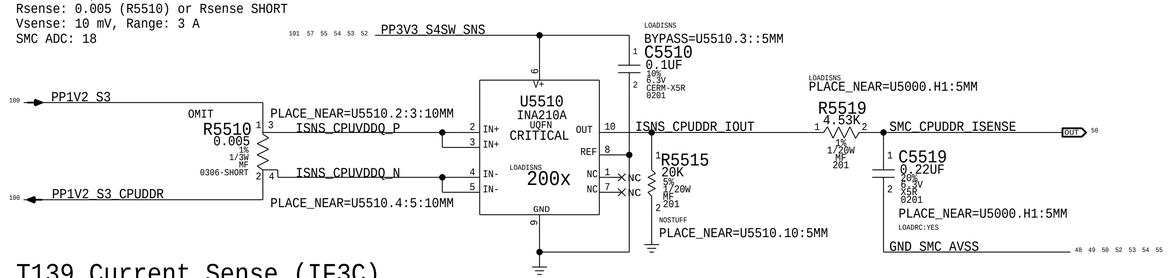
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 100x, EDP: 8.21 A
Rsense: 0.003 (R7918) or XWTBD
Vsense: 24.63 mV, Range: 10 A
SMC ADC: 09



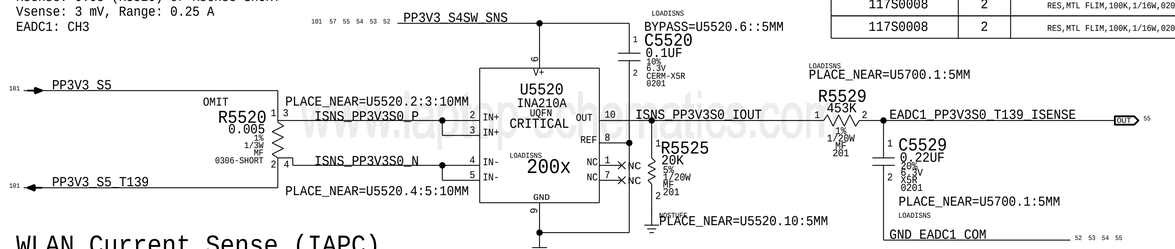
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 10 mV, Range: 3 A
SMC ADC: 18



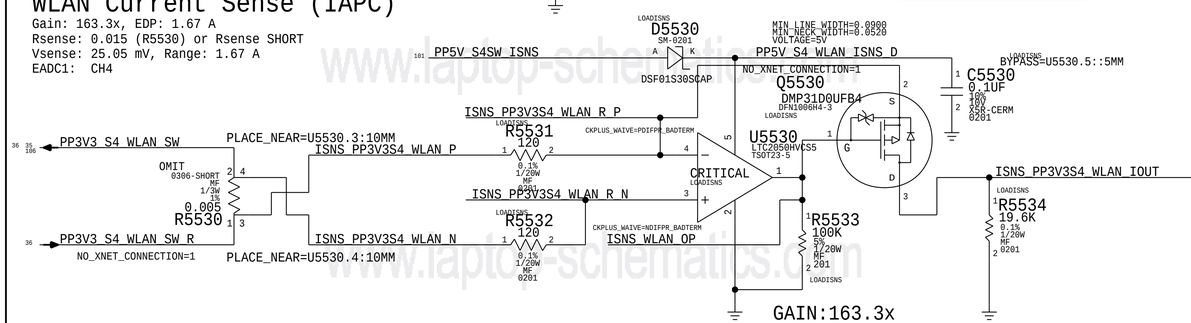
T139 Current Sense (IF3C)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5520) or Rsense SHORT
Vsense: 3 mV, Range: 0.25 A
EADC1: CH3



WLAN Current Sense (IAPC)

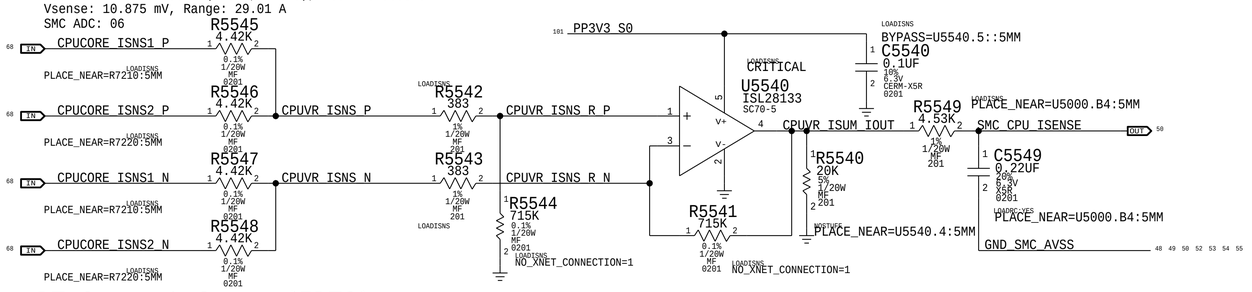
Gain: 163.3x, EDP: 1.67 A
Rsense: 0.015 (R5530) or Rsense SHORT
Vsense: 25.05 mV, Range: 1.67 A
EADC1: CH4



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5569,C5519		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5549,C5579		LOADRC:NO

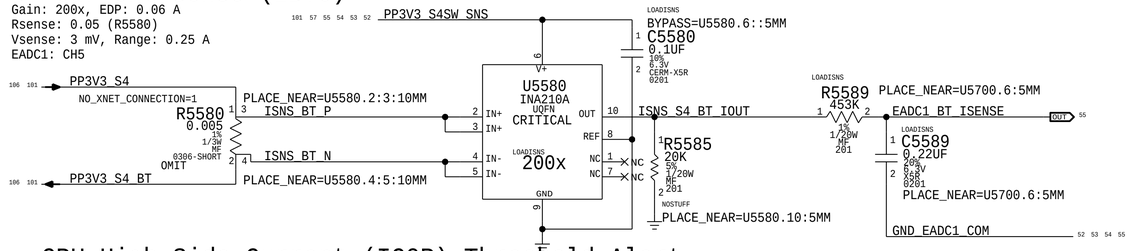
CPU Fixed Current Sense (ICAC)

Gain: 275.74x, EDP: 29 A
Rsense: 2x of 0.00075 (R7310, R7320), Rsum: 0.000375
Vsense: 10.875 mV, Range: 29.01 A
SMC ADC: 06



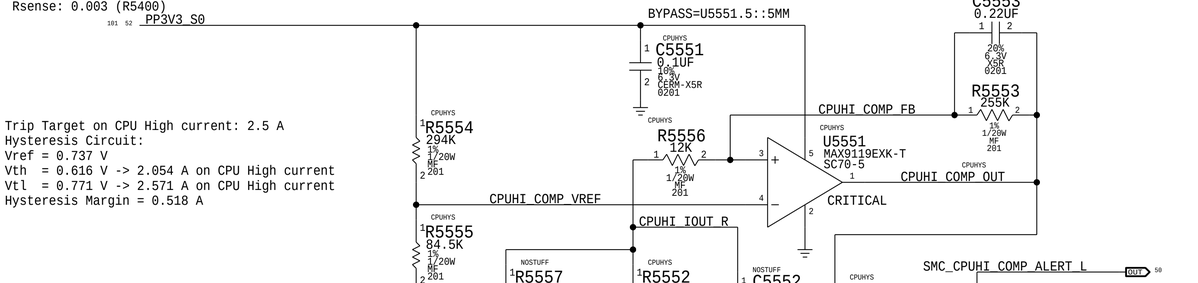
BT Current Sense (IBTC)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5580)
Vsense: 3 mV, Range: 0.25 A
EADC1: CH5



CPU High Side Current (IC0R) Threshold Alert

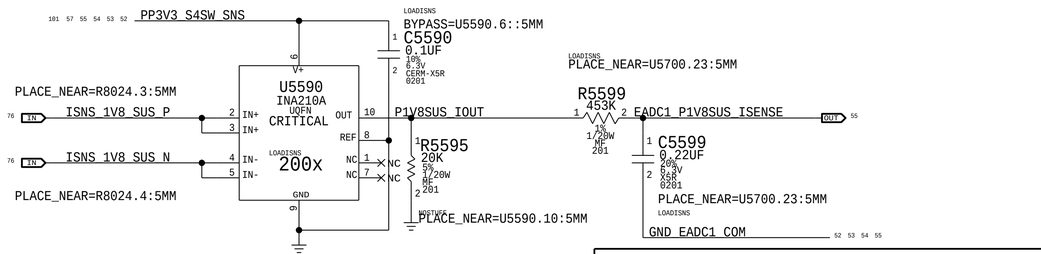
Gain: 100x
Rsense: 0.003 (R5400)



Trip Target on CPU High current: 2.5 A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vtl = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A

1.8V Current Sense (I18C)

Gain: 200x, EDP: 0.7 A
Rsense: 0.025 (R8024) or Rsense SHORT
Vsense: 17.5 mV, Range: 0.6 A
SMC ADC: 16

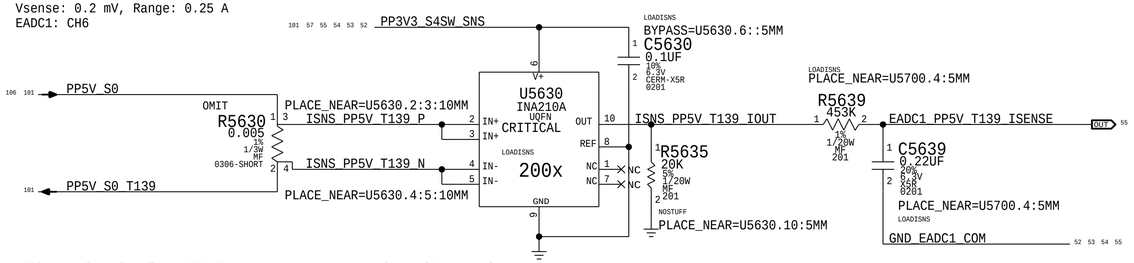


BOM_COST_GROUP=SENSORS

PAGE TITLE		
Power Sensors: Load Side		
Apple Inc.	DRAWING NUMBER 051-00777	SIZE D
	REVISION 9.0.0	
	BRANCH dvt-fab09-0	
	PAGE 55 OF 145	
	SHEET 53 OF 119	

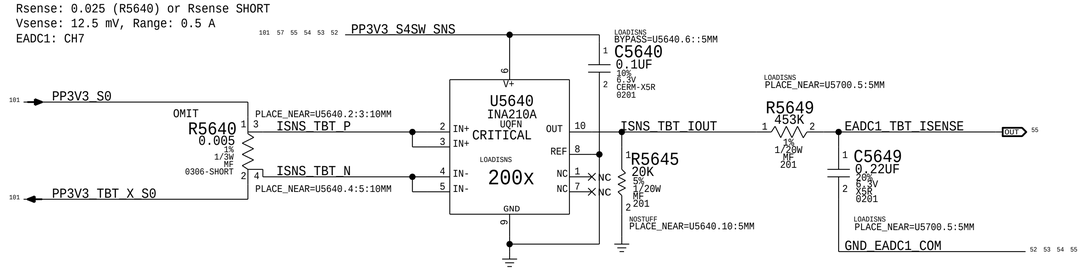
T139 5V Current Sense (IF5C)

Gain: 200x, EDP: 0.004 A
Rsense: 0.05 (R5630) or Rsense SHORT
Vsense: 0.2 mV, Range: 0.25 A
EADC1: CH6



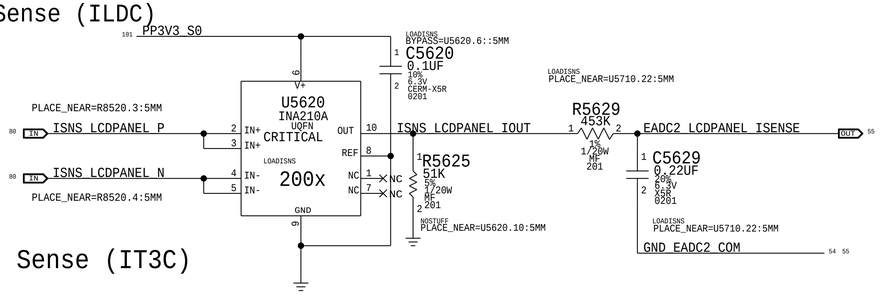
Thunderbolt TBT Current Left (IULC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5640) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH7



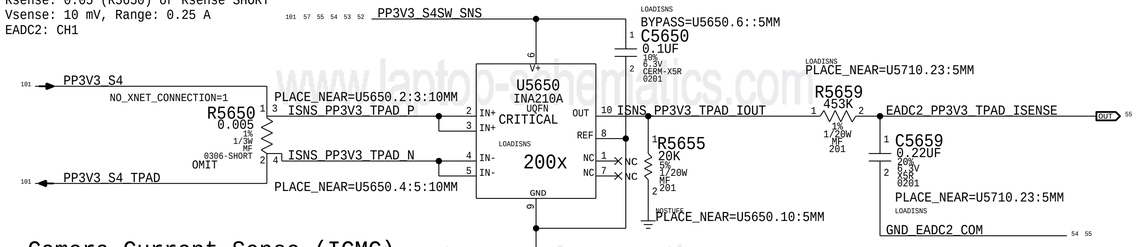
LCD Panel Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC2: CH0



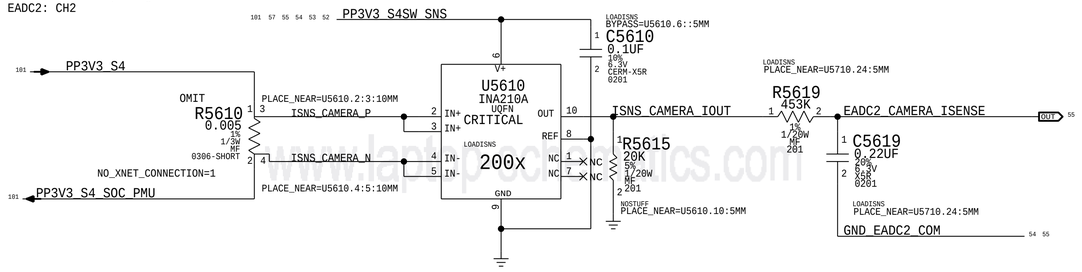
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.2 A
Rsense: 0.05 (R5650) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH1

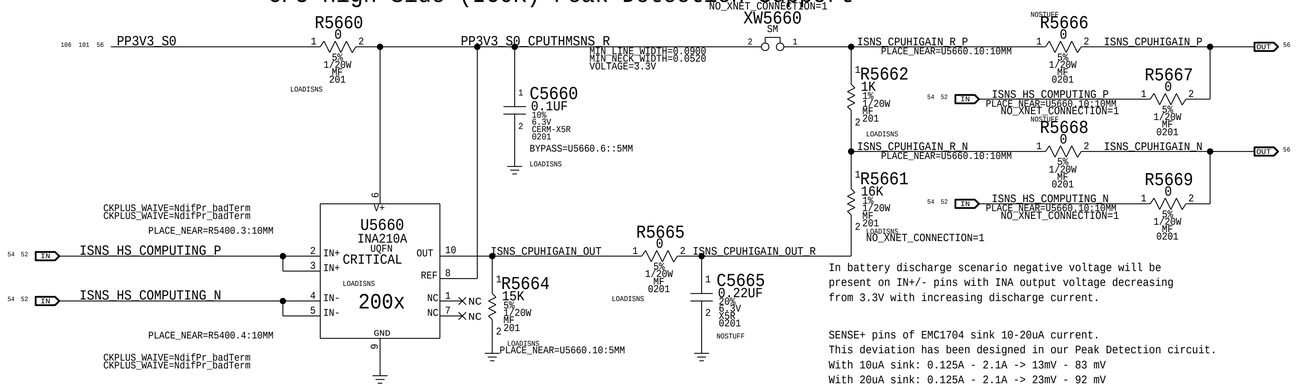


Camera Current Sense (ICMC)

Gain: 200x. EDP: 0.82 A
Rsense: 0.015 (R5610) or XW5610
Vsense: 12.3 mV, Range: 0.83 A
EADC2: CH2



CPU High Side (IC0R) Peak Detection Support

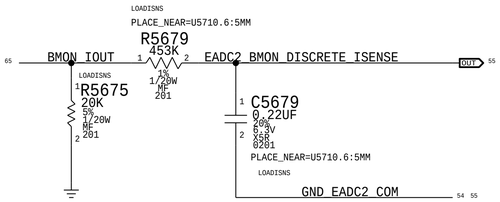


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit.
With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV
With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

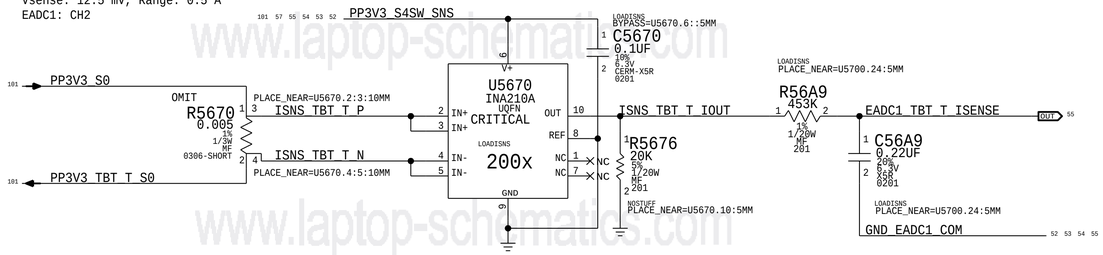
Battery Discrete Current Sense (IB0L)

Gain: 2940x. EDP: 8 A
Rsense: 0.003 (R501//R502)
Vsense: 24 mV, Range: 0.28 A
EADC2: CH5



Thunderbolt TBT Current Right (IURC)

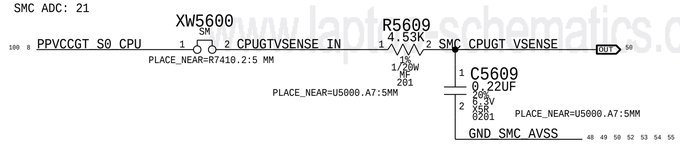
Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5670) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5608, C5699		LOADRC:NO

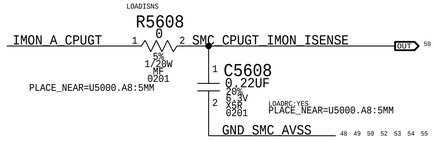
CPU GT Voltage Sense (VCGC)

SMC ADC: 21



CPU GT IMON Current Sense (ICGM)

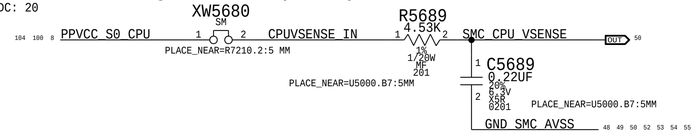
Gain: 1 A / 17.963 mV, Range: 64 A.
SMC ADC: 23



With R7154 (Ri) set to 294 Ohm,
R7410 (Rsen) set to 0.75 mOhm,
R7194 set to 84.5 kOhm,
Num Phases (N) is 3, and Io (ICCmax) is 64A,
then 1A of Io gives 17.963mV at the Vimon.

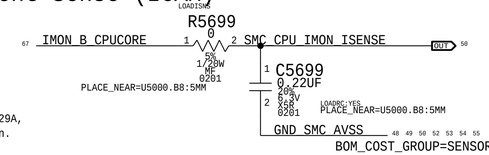
CPU Core Voltage Sense (VCAC)

SMC ADC: 20



CPU Core IMON Current Sense (ICAM)

Gain: 1 A / 34.223 mV, Range: 29 A.
SMC ADC: 22



With R7150 (Ri) set to 226 Ohm,
R7210 (Rsen) set to 0.75 mOhm,
R7160 set to 82.5 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 29A,
then 1A of Io gives 34.223mV at the Vimon.

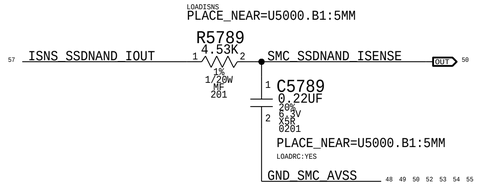
BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensors: Extended

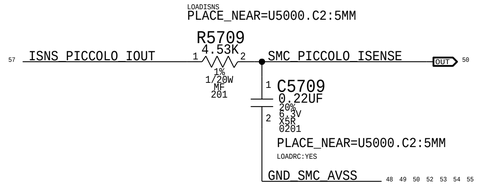
Apple Inc.

DRAWING NUMBER 051-00777 | SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 56 OF 145
SHEET 54 OF 119

NAND Current Sense (IHNC)

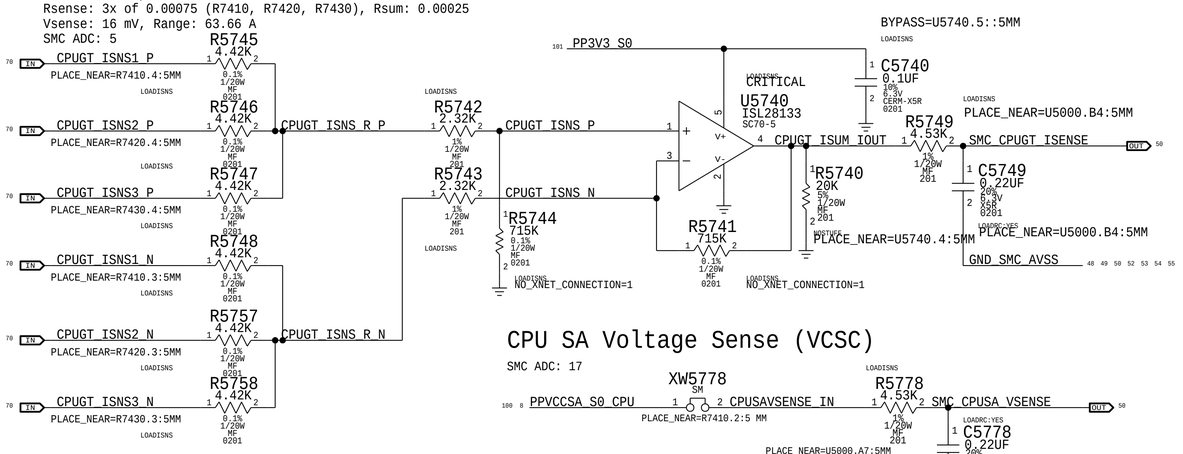


PICCOLO Current Sense (IHCC)



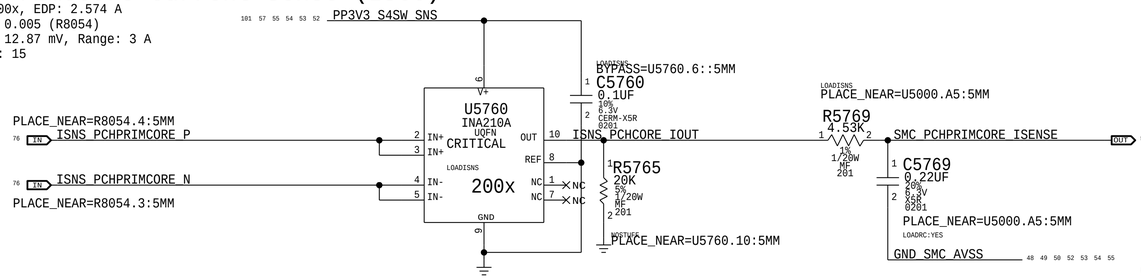
CPU GT+GTX Current Sense (ICGC)

Gain: 188.49x, EDP: 64 A
Rsense: 3x of 0.00075 (R7410, R7420, R7430), Rsum: 0.00025
Vsense: 16 mV, Range: 63.66 A
SMC ADC: 5



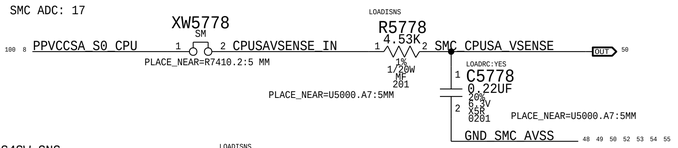
PCH PrimeCore Current Sense (ISCC)

Gain: 200x, EDP: 2.574 A
Rsense: 0.005 (R8054)
Vsense: 12.87 mV, Range: 3 A
SMC ADC: 15



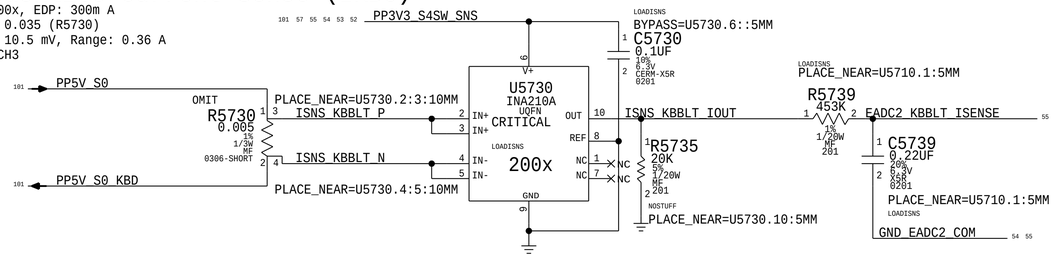
CPU SA Voltage Sense (VCSC)

SMC ADC: 17



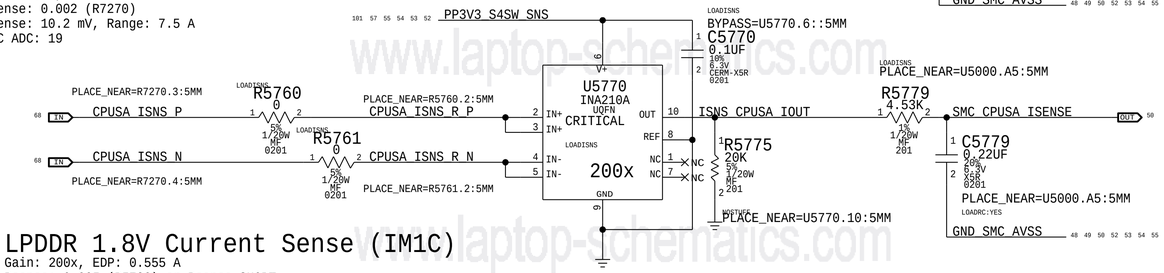
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 300 m A
Rsense: 0.035 (R5730)
Vsense: 10.5 mV, Range: 0.36 A
EADC2: CH3



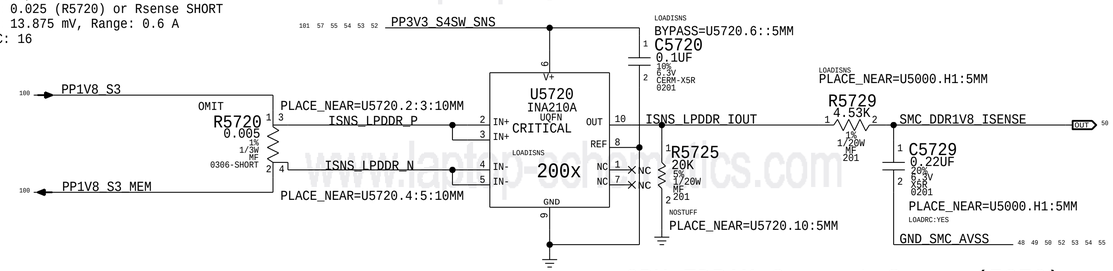
CPU SA Current Sense (ICSC)

Gain: 200x, EDP: 5.1 A
Rsense: 0.002 (R7270)
Vsense: 10.2 mV, Range: 7.5 A
SMC ADC: 19



LPDDR 1.8V Current Sense (IM1C)

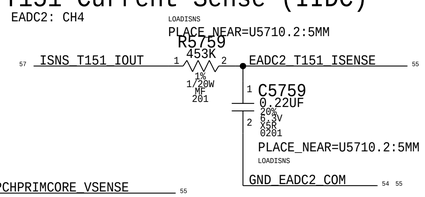
Gain: 200x, EDP: 0.555 A
Rsense: 0.025 (R5720) or Rsense SHORT
Vsense: 13.875 mV, Range: 0.6 A
SMC ADC: 16



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5769,C5778		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5749,C5779		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5729,C5799		LOADRC:NO
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5709,C5789		LOADRC:NO

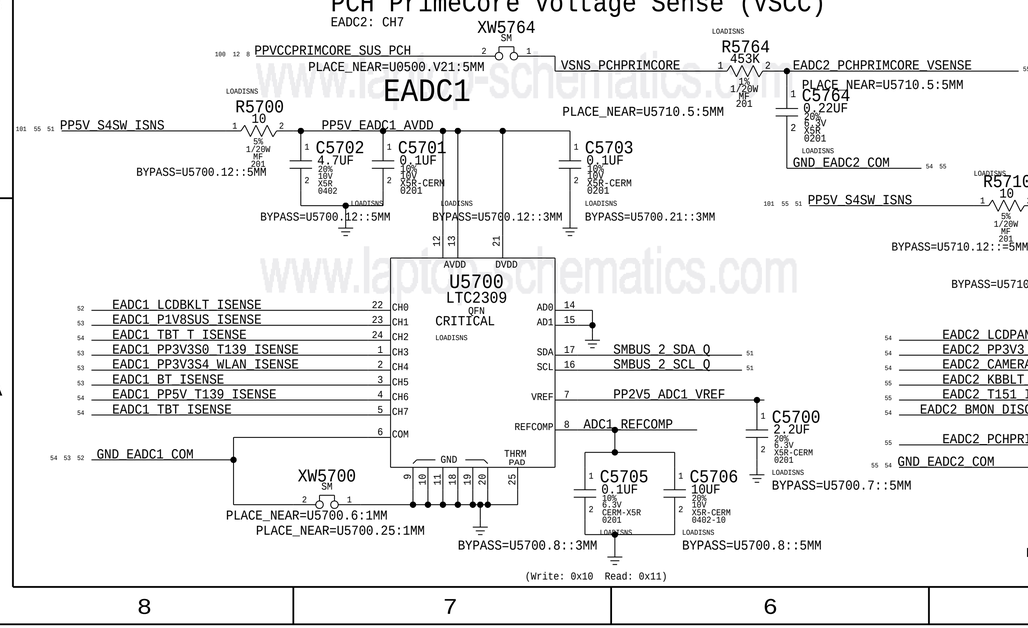
T151 Current Sense (IIDC)

EADC2: CH4

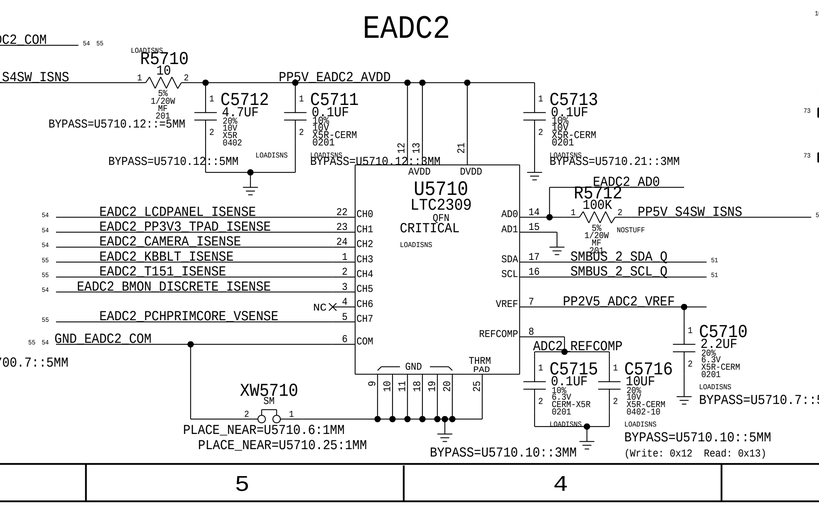


PCH PrimeCore Voltage Sense (VSCC)

EADC2: CH7

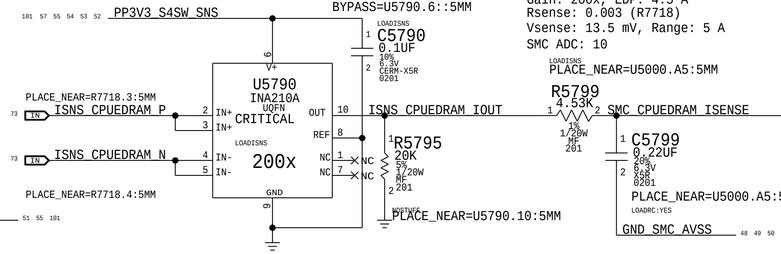


EADC2



CPU EDRAM Current Sense (ICEC)

Gain: 200x, EDP: 4.5 A
Rsense: 0.003 (R7718)
Vsense: 13.5 mV, Range: 5 A
SMC ADC: 10



BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Extended 2

Apple Inc.

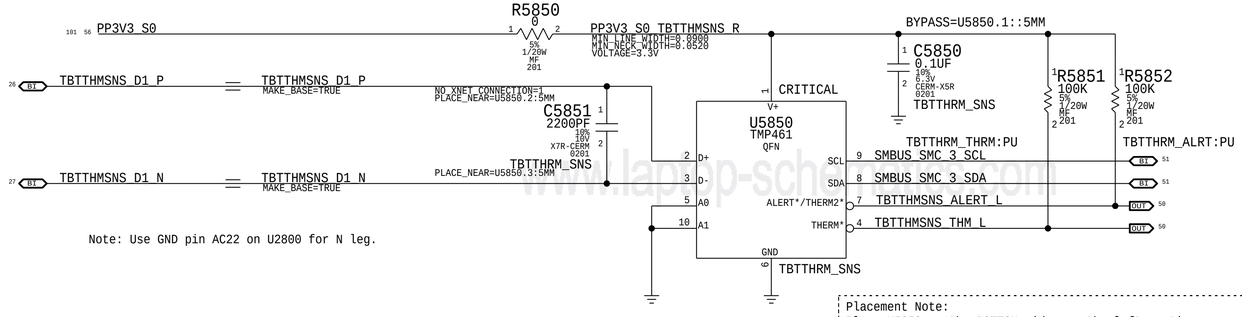
DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 57 OF 145
SHEET: 55 OF 119

Thermal Sensor A: Thunderbolt Die, Airflow Left

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TBT1)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.

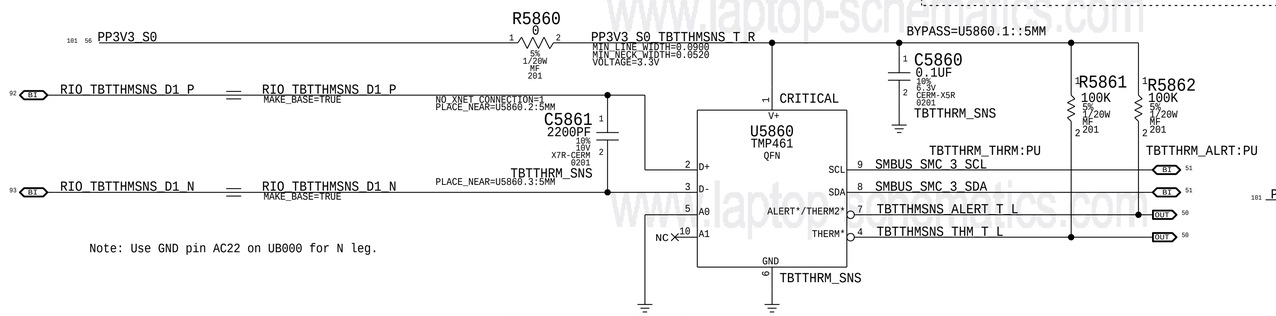


Thermal Sensor C: Thunderbolt Die, Air Flow Right

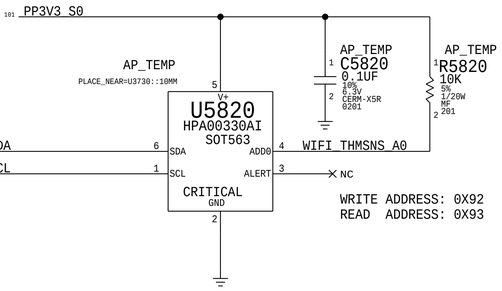
I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: TBT Die (TBT2)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



X100 PROXIMITY



Thermal Sensor B & CPU High Peak Detection: CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right

I2C Write: 0xB8, I2C Read: 0xB9

Thermal Diode: Fin Stack Left (Th2H)

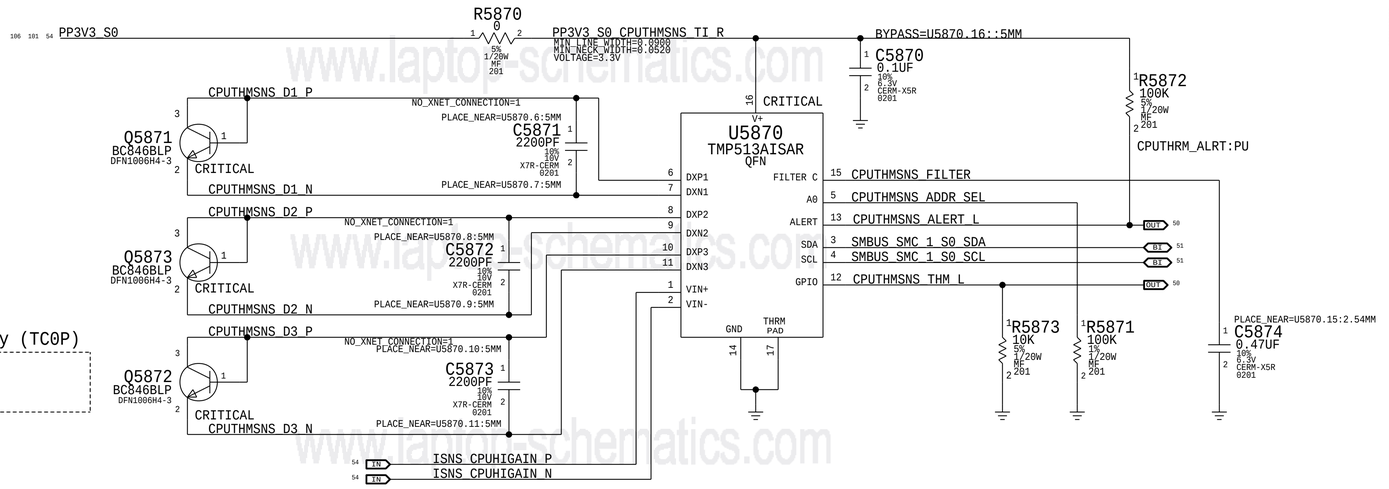
Placement Note:
Place Q5871, Airflow thermal indicator, above the X100, on the TOP side.

Thermal Diode: CPU Proximity (TC0P)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

Thermal Diode: Memory Proximity (TM0P)

Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.



Thermal Sensor: Fin Stack Right (Th1H)

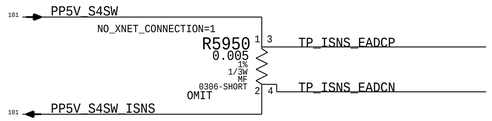
Placement Note:
Place U5870 at corner near right Fan, on the TOP side.

BOM_COST_GROUP=SENSORS

PAGE TITLE	Thermal Sensors
Apple Inc.	
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	58 OF 145
SHEET	56 OF 119

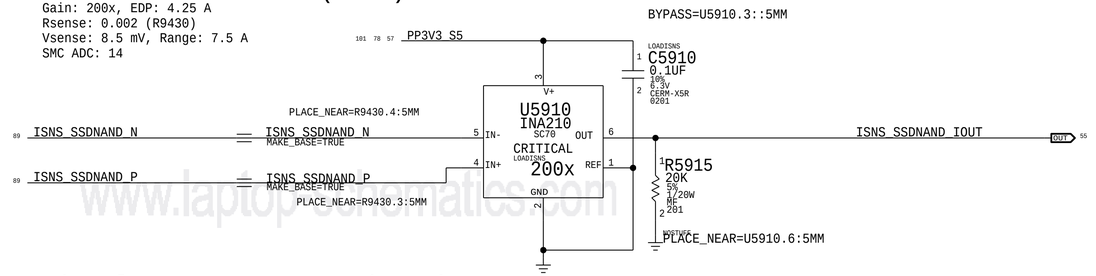
EADC Current Sense (IADC)

Gain: 200x, EDP: 200m A
Rsense: 0.050 (R5950) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH7



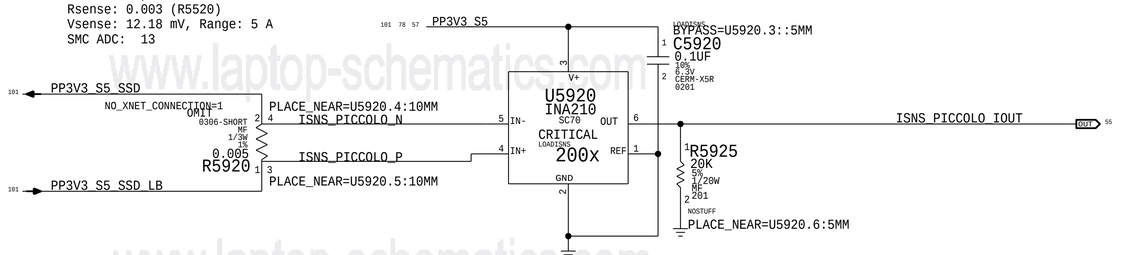
NAND Current Sense (IHNC)

Gain: 200x, EDP: 4.25 A
Rsense: 0.002 (R9430)
Vsense: 8.5 mV, Range: 7.5 A
SMC ADC: 14



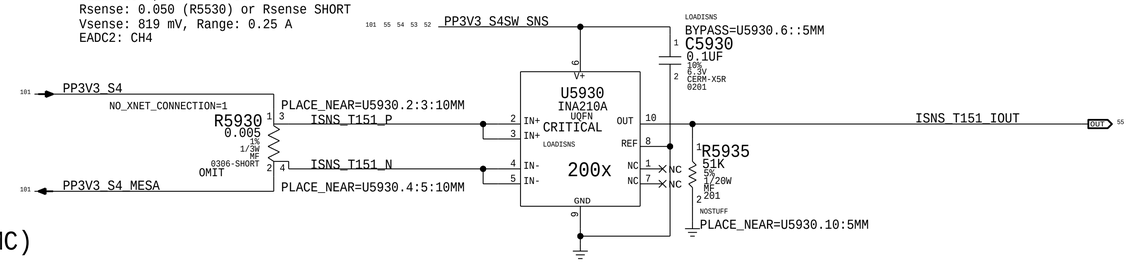
Piccolo Current Sense (IHCC)

Gain: 200x, EDP: 4.06 A
Rsense: 0.003 (R5520)
Vsense: 12.18 mV, Range: 5 A
SMC ADC: 13



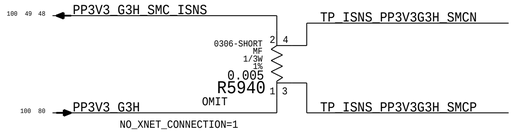
T151 Current Sense (IIDC)

Gain: 200x, EDP: 163.8m A
Rsense: 0.050 (R5530) or Rsense SHORT
Vsense: 819 mV, Range: 0.25 A
EADC2: CH4



SMC Current Sense (ISMC)

Gain: 391.67x, EDP: 0.2 A
Rsense: 0.05 (R5940) or Rsense SHORT
Vsense: 10 mV, Range: 0.21A
EADC2: CH6



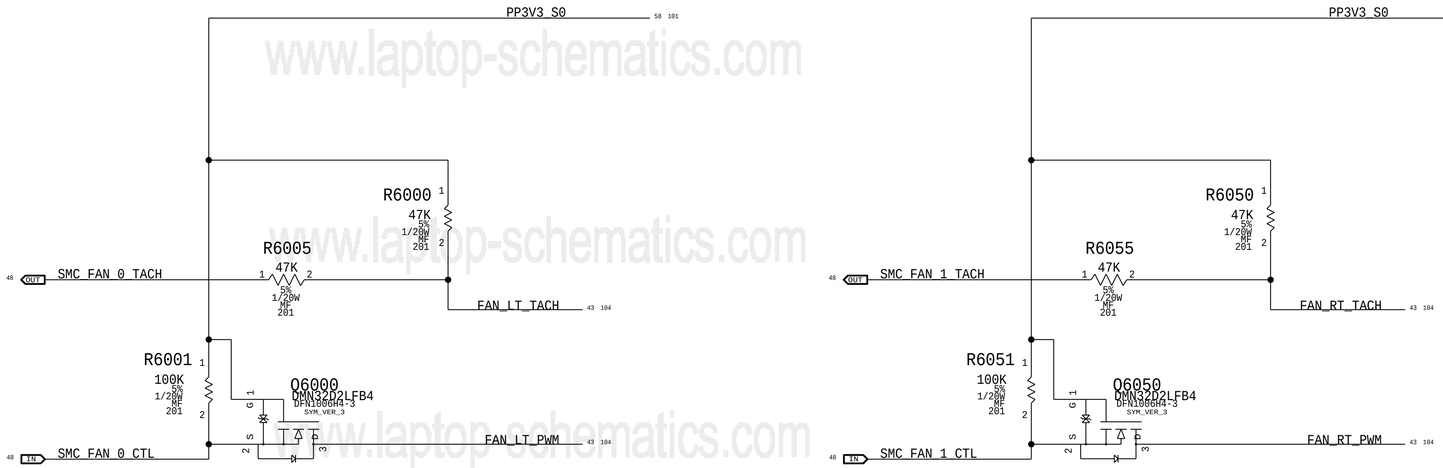
BOM_COST_GROUP=SENSORS

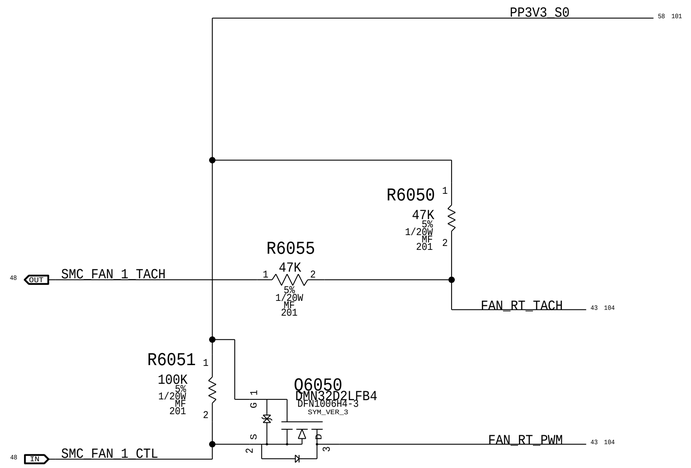
PAGE TITLE: Power Sensors:Extended 3

Apple Inc.

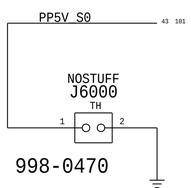
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	59 OF 145
SHEET	57 OF 119

FAN CONTROL





FOR DEBUG FAN POWER



BOM_COST_GROUP=FAN

SYNC_MASTER=J79_JACK SYNC_DATE=08/21/2015

PAGE TITLE: Fans

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

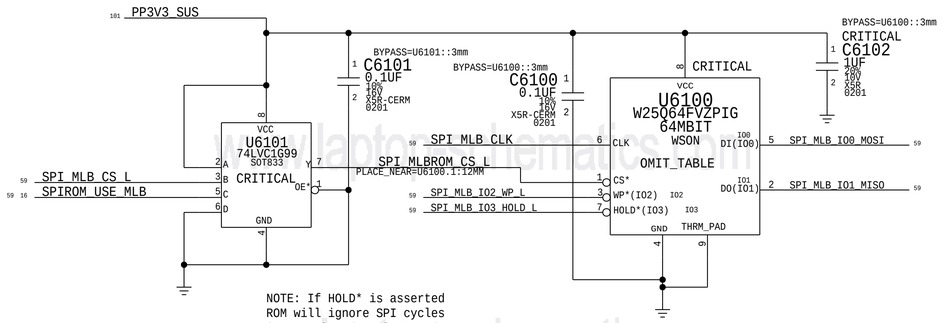
BRANCH dvt-fab09-0

PAGE 60 OF 145

SHEET 58 OF 119

SPI ROM

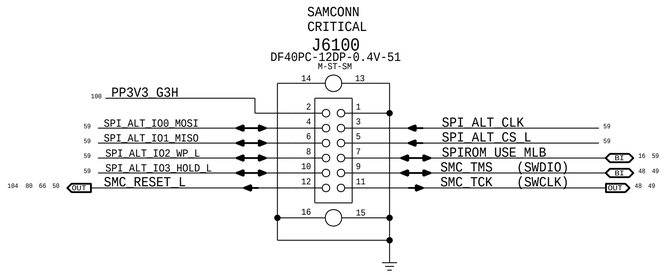
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

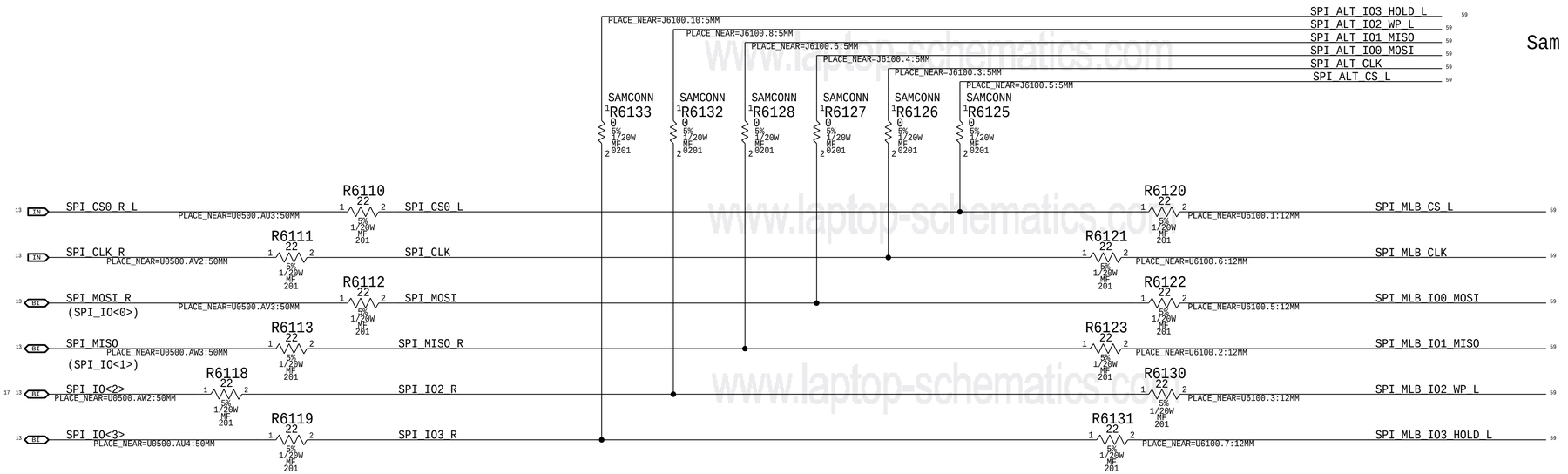
Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination (Modified per PDG)

CPU Master



Sam Card ROM Slave

SPI ROM Slave

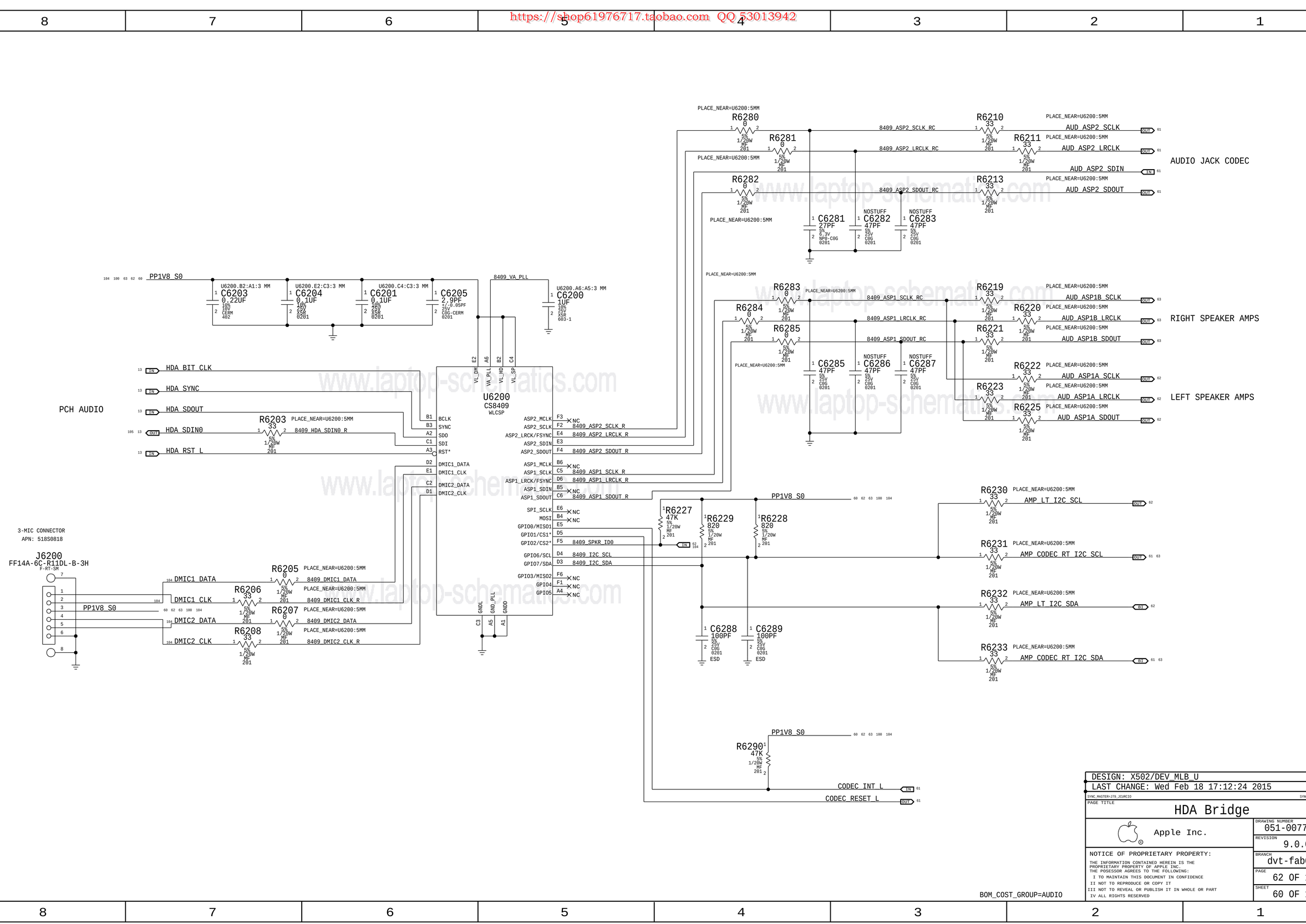
BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J52_MLB SYNC_DATE=05/12/2015

PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 61 OF 145
SHEET: 59 OF 119



BOM_COST_GROUP=AUDIO

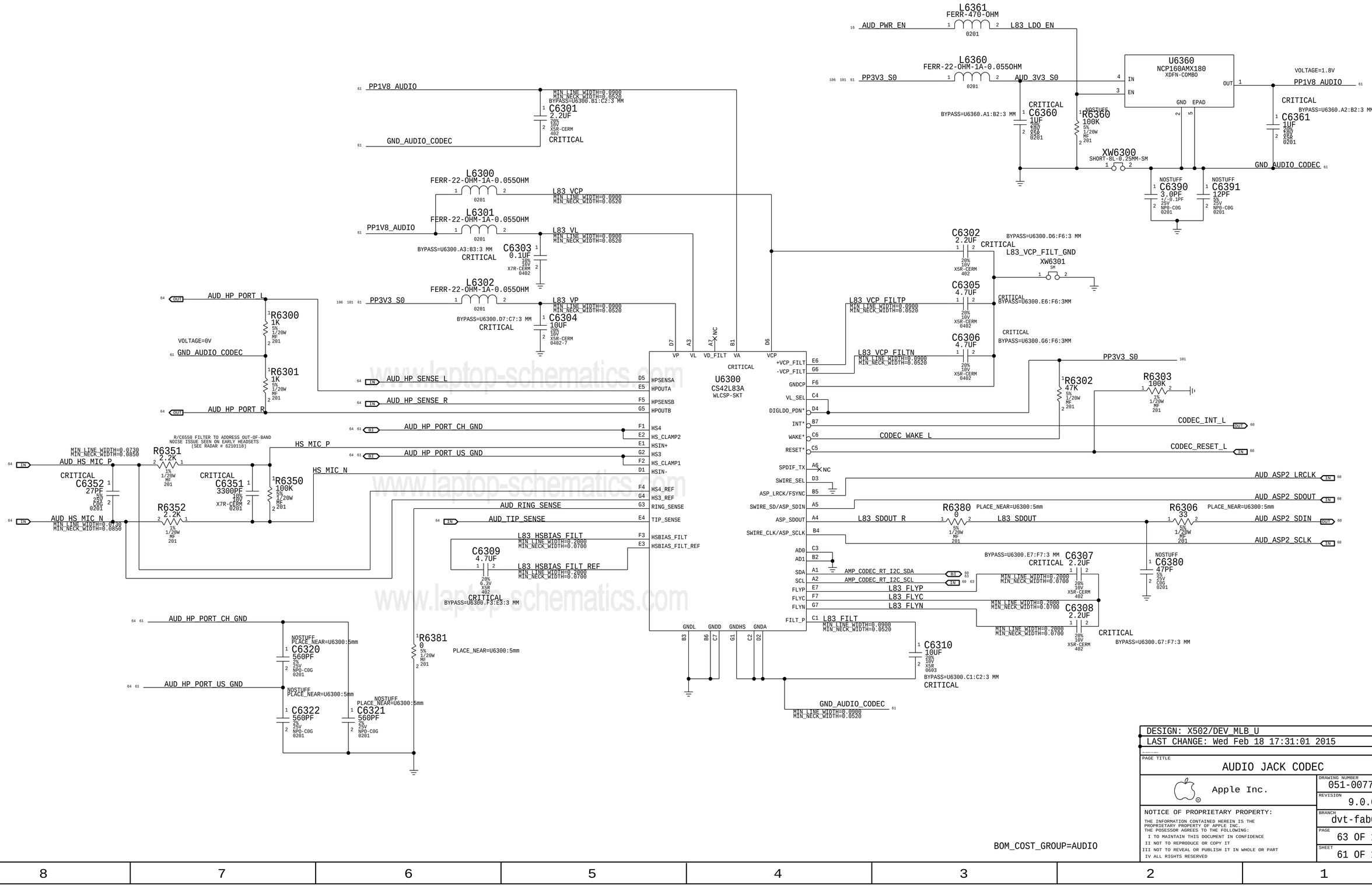
DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015
SYNC_MASTER=J79_JCURCIO SYNC_DATE=03/24/2016
PAGE TITLE
HDA Bridge

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 62 OF 145
SHEET 60 OF 119

AUDIO JACK CODEC I2C ADDRESS

AD1	AD0	ADDRESS
GND	GND	0x90 <--
GND	1.8V	0x92
1.8V	GND	0x94
1.8V	1.8V	0x96



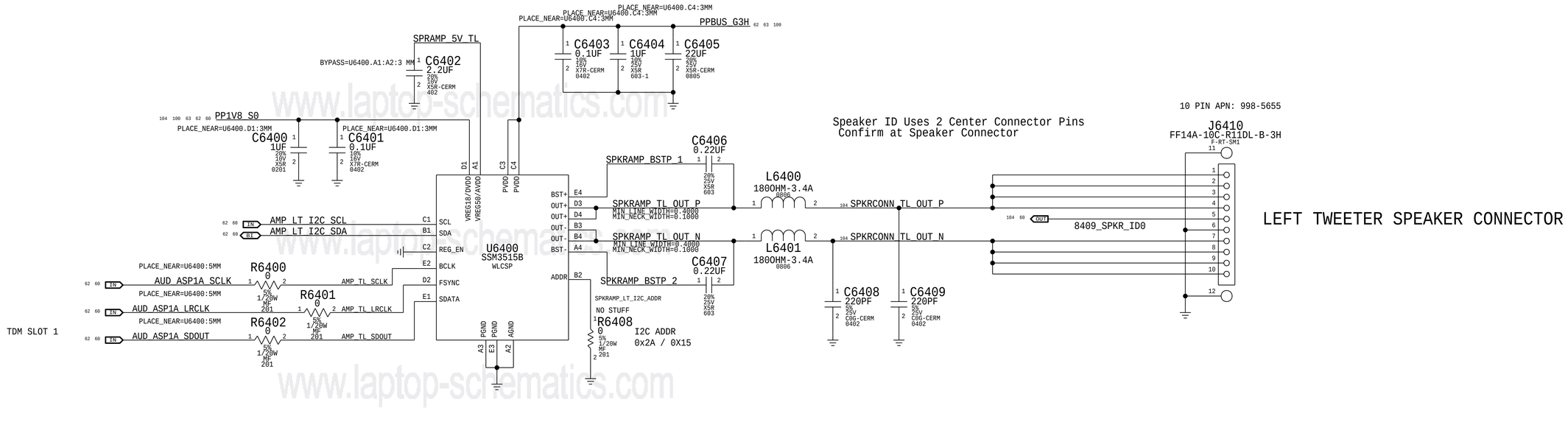
DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:31:01 2015

PAGE TITLE
AUDIO JACK CODEC

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 63 OF 145
SHEET 61 OF 119

2X MONO SPEAKER AMPLIFIERS
APN: 353S4074
GAIN = TBD



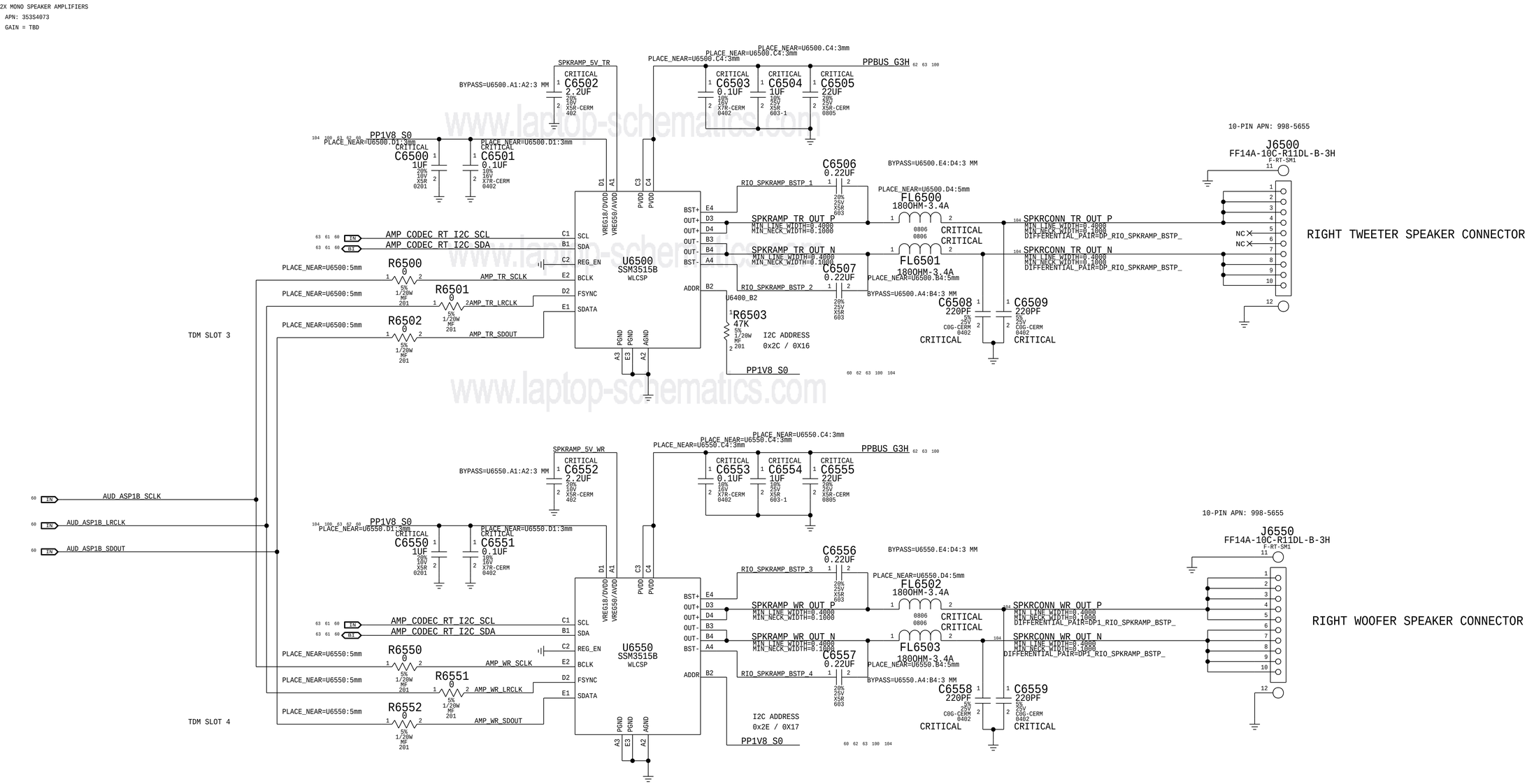
BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015
PAGE TITLE
Left Speaker Amps & Conn

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 64 OF 145
SHEET 62 OF 119

2X MONO SPEAKER AMPLIFIERS
APN: 353S4073
GAIN = TBD



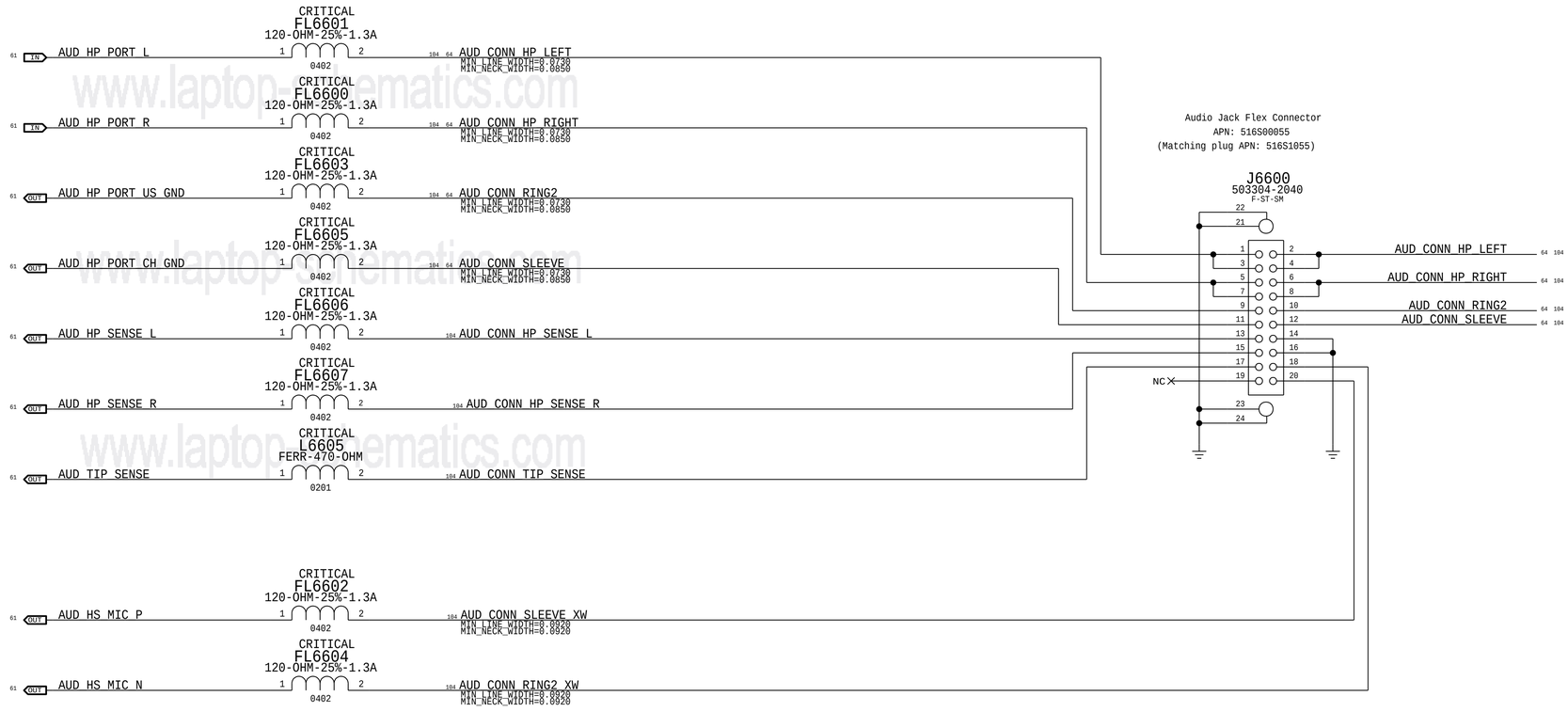
DESIGN	X502/DEV_MLB_U
LAST CHANGE	Wed Feb 18 17:12:24 2015
PAGE TITLE	Right Speaker Amps & Conn
	Apple Inc.
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	65 OF 145
SHEET	63 OF 119

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	OTHER CODEC GPIO LINES			
[redacted]	0X02 (2)	0X02 (2)	0X10 (16)	CODEC GPIO1	[redacted]	GPIO2	INPUT	HIGH = FG, LOW = MERRY
[redacted]	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0	LEFT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
[redacted]	0X04 (4)	0X04 (4)	0X13 (19)	VREG_EN	RIGHT SPEAKER ID	GPIO4	OUTPUT	HIGH = DFETs OPEN
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A	DFET CONTROL			

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC	0X05 (5)	0X1B (29)	3.3V
DMIC	0X06 (6)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V



BOM_COST_GROUP=AUDIO

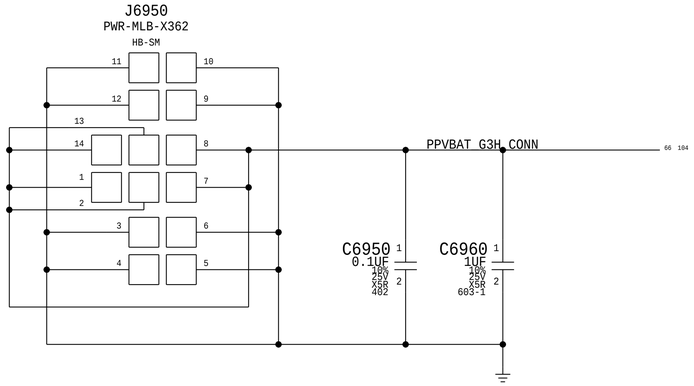
DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015

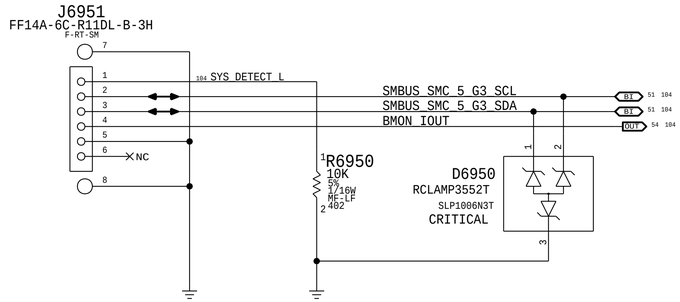
PAGE TITLE
AUDIO JACK CONNECTOR

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 66 OF 145
SHEET 64 OF 119

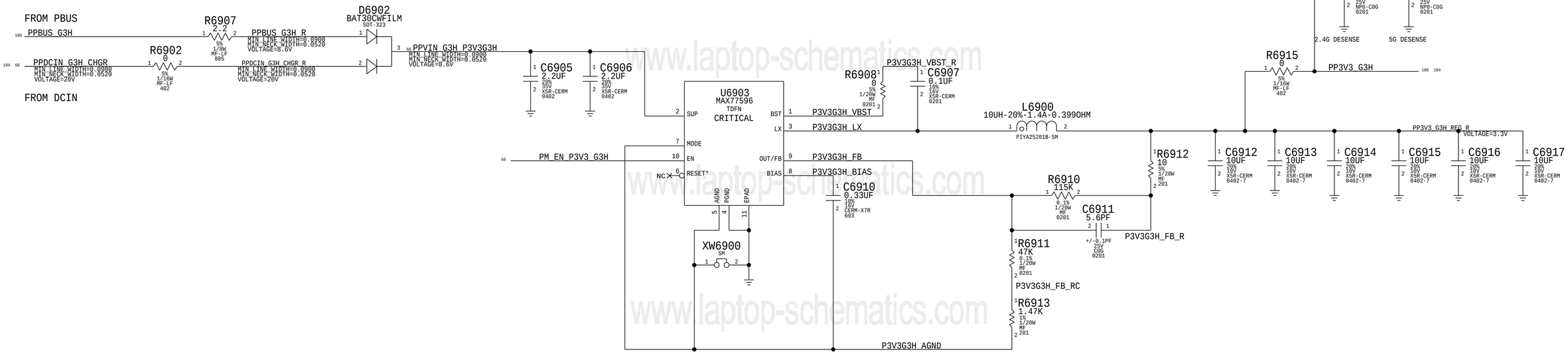
J79 Battery Hotbar Flex Pads





BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00566	1	PCBA,FLEX,BMU PWR,X362	J6950	CRITICAL	

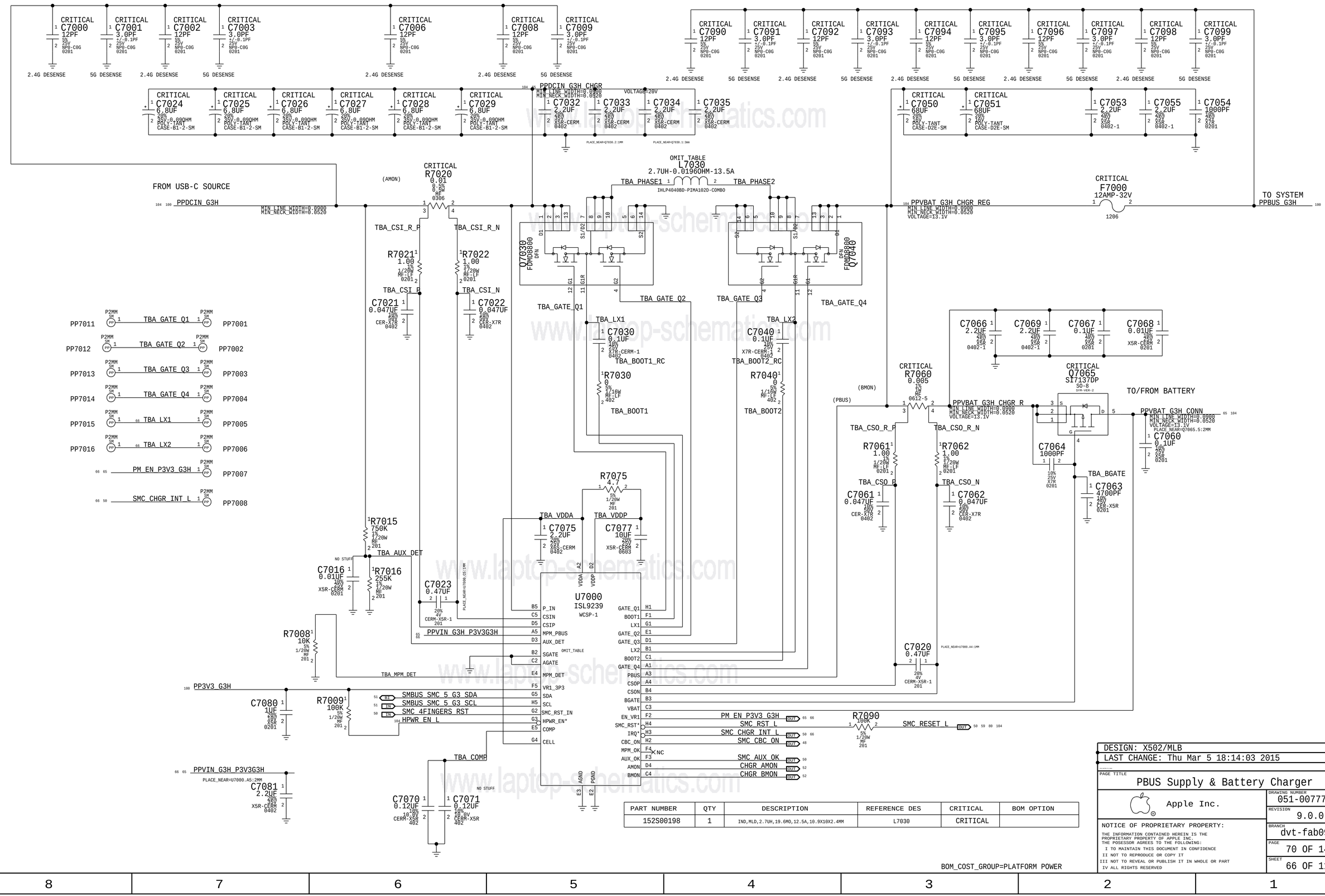


BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 69 OF 145
SHEET 65 OF 119



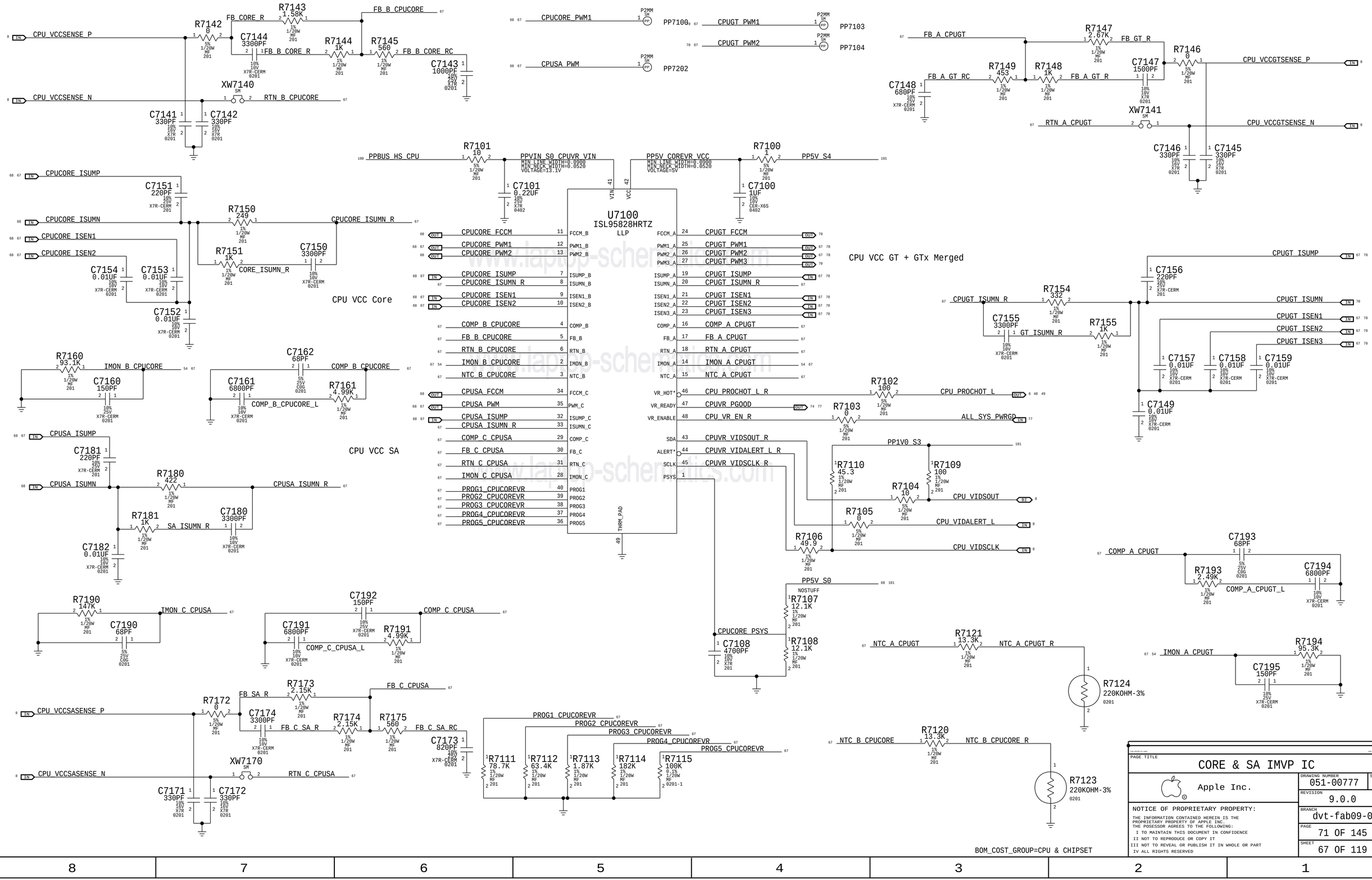
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00198	1	IND,MLD,2.7UH,19.6MO,12.5A,10.9X10X2.4MM	L7030	CRITICAL	

DESIGN: X502/MLB
LAST CHANGE: Thu Mar 5 18:14:03 2015

PAGE TITLE
PBUS Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 70 OF 145
SHEET 66 OF 119



PAGE TITLE

CORE & SA IMVP IC

Apple Inc.

DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	71 OF 145
SHEET	67 OF 119

CPU VCC Phase 1

PPBUS_HS_CPU
PP5V_S0
PP5V_S0_VCORE1
PVCCCORE_PH1_AGND
R7215 1 5% 1/10W MF-LF 402
C7217 2.2UF 20% 25V X6S-CERM 0402
C7216 2.2UF 20% 25V X6S-CERM 0402
U7210 FDMF5808A PQFN-COMBO-THICKSTNCL OMIT_TABLE CRITICAL
CPUCORE_FCCM
CPUCORE_PWM1
CPUCORE_SW1
L7210 0.22UH-35A-0.002550HM PPVCC_CPU_PH1 PILS062D-IHLP2525BD-SM-COMBO
CPUCORE_BOOT1
R7219 0 5% 1/16W MF-LF 402
CPUCORE1_GL0
CPUCORE_BP1
CPUCORE1_DRVH
C7219 0.22UF 10% 25V X7R 0402
CPUCORE_PHASE1
R7218 2.2 5% 1/10W MF-LF 603 NOSTUFF
CPUCORE_SW1_SNUB DIDT=TRUE
C7218 0.001UF 10% 50V X7R-CERM 0402 NOSTUFF
XW7210 SM
PLACE_NEAR=U7210.32:2MM
CRITICAL R7210 0.00075 1% 1W MF 0612-1 NO_XNET_CONNECTION=1
CPUCORE_ISNS1_P
CPUCORE_ISNS1_N
R7211 2.2 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUCORE_ISUMN
R7212 1K 1% 1/20W MF 201
R7213 200K 1% 1/20W MF 201
R7214 200K 1% 1/20W MF 201
CPUCORE_ISNS2_N
CPUCORE_ISEN1
CPUCORE_ISUMP
C7210 33UF 20% 16V TANT-POLY CASE-B3
C7211 33UF 20% 16V TANT-POLY CASE-B3
C7212 33UF 20% 16V TANT-POLY CASE-B3
C7213 2.2UF 20% 25V X6S-CERM 0402
C7214 2.2UF 20% 25V X6S-CERM 0402
C7215 12PF 5% 25V NP0-C0G 0201
PPVCC_S0_CPU
Vout = 0.55 - 1.5V
IccMax = 32A
F = 750kHz
CPUCORE1_GL0 → PP7210
CPUCORE2_GL0 → PP7220
CPUSA_GL0 → PP7270
CPUCORE1_DRVH → PP7211
CPUCORE2_DRVH → PP7221
CPUCORE_FCCM → PP7212
CPUSA_FCCM → PP7272
CPUSA_DRVH → PP7271

CPU VCC Phase 2

PPBUS_HS_CPU
PP5V_S0
PP5V_S0_VCORE2
PVCCCORE_PH2_AGND
R7225 1 5% 1/10W MF-LF 402
C7227 2.2UF 20% 25V X6S-CERM 0402
C7226 2.2UF 20% 25V X6S-CERM 0402
U7220 FDMF5808A PQFN-COMBO-THICKSTNCL OMIT_TABLE CRITICAL
CPUCORE_FCCM
CPUCORE_PWM2
CPUCORE_SW2
L7220 0.22UH-35A-0.002550HM PPVCC_CPU_PH2 PILS062D-IHLP2525BD-SM-COMBO
CPUCORE_BOOT2
R7229 0 5% 1/16W MF-LF 402
CPUCORE2_GL0
CPUCORE_BP2
CPUCORE2_DRVH
C7229 0.22UF 10% 25V X7R 0402
CPUCORE_PHASE2
R7228 2.2 5% 1/10W MF-LF 603 NOSTUFF
CPUCORE_SW2_SNUB DIDT=TRUE
C7228 0.001UF 10% 50V X7R-CERM 0402 NOSTUFF
XW7220 SM
PLACE_NEAR=U7220.32:2MM
CRITICAL R7220 0.00075 1% 1W MF 0612-1 NO_XNET_CONNECTION=1
CPUCORE_ISNS2_P
CPUCORE_ISNS2_N
R7221 2.2 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUCORE_ISUMN
R7222 1K 1% 1/20W MF 201
R7223 200K 1% 1/20W MF 201
R7224 200K 1% 1/20W MF 201
CPUCORE_ISNS1_N
CPUCORE_ISEN2
CPUCORE_ISUMP
C7220 33UF 20% 16V TANT-POLY CASE-B3
C7221 33UF 20% 16V TANT-POLY CASE-B3
C7223 2.2UF 20% 25V X6S-CERM 0402
C7224 2.2UF 20% 25V X6S-CERM 0402
C7225 12PF 5% 25V NP0-C0G 0201
CRITIICAL C7230 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITIICAL C7231 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE
CRITIICAL C7232 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITIICAL C7233 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE

CPU VCCSA

PPBUS_HS_CPU
PP5V_S0
PP5V_S0_VCCSA
PVCCCSA_AGND
R7275 1 5% 1/10W MF-LF 402
C7277 2.2UF 20% 25V X6S-CERM 0402
C7276 2.2UF 20% 25V X6S-CERM 0402
U7270 SIC535CD MLP4535
CPUSA_FCCM
CPUSA_PWM
CPUSA_DRVH
CPUVR_SWSA
L7270 0.47UH-20A-0.00494OHM PPVCCSA_CPU_R IHLP2020BD-SM
CPUSA_BOOTSA
R7279 0 5% 1/16W MF-LF 402
CPUSA_GL0
CPUSA_BPSA
C7279 0.22UF 10% 25V X7R 0402
CPUSA_PHASESA
R7278 2.2 5% 1/10W MF-LF 603 NOSTUFF
CPUSA_SW_SNUB DIDT=TRUE
C7278 0.001UF 10% 50V X7R-CERM 0402 NOSTUFF
XW7270 SM
PLACE_NEAR=U7270.13:2MM
CRITICAL R7270 0.002 1% 1W CYN 0612
CPUSA_ISNS_P
CPUSA_ISNS_N
R7272 0 5% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUSA_ISUMN
R7274 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUSA_ISUMP
C7270 33UF 20% 16V TANT-POLY CASE-B3
C7271 33UF 20% 16V TANT-POLY CASE-B3
C7272 2.2UF 20% 25V X6S-CERM 0402
C7273 2.2UF 20% 25V X6S-CERM 0402
C7274 12PF 5% 25V NP0-C0G 0201
PPVCCSA_S0_CPU
Vout = 0.55 - 1.15V
IccMax = 5.1A
F = 750kHz
CRITICAL C7280 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITICAL C7281 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	2	IC,FDMF5808A,DRMOS,IMVP8,50A,PQFN31,5X5	U7210, U7220	CRITICAL	
152S00241	1	IND,MLD,0.47UH,4.94MO,20A,5.4X5.2X2.4MM	L7270	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=I79_J9HAD
SYNC_DATE=12/03/2012

PAGE TITLE: CORE & SA IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 72 OF 145
SHEET: 68 OF 119

SYNC_MASTER=J79_SILUCHEN SYNC_DATE=04/02/2015

PAGE TITLE

Empty

Apple Inc.

DRAWING NUMBER 051-00777

SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 73 OF 145

SHEET 69 OF 119

CPU VCCGT/GTx Phase 1

PPBUS_HS_CPU
PP5V_S0
R7416 1 5% 1/10W MF-LF 402 VOLTAGE=5V PP5V_S0_VGT1
C7417 2.2UF 20% 25V X6S-CERM 0402
PVCCCGT_PH1_AGND
C7416 2.2UF 20% 25V X6S-CERM 0402
U7410 FDMF5808A VIN PQFN-COMBO-THICKSTNCL OMIT_TABLE CRITICAL
VIN VCC PVCC BOOT PHASE SW SW GL0 GL1 GH FCCM PWM NC NC NC NC AGND AGND PGND PGND
CPUGT_FCCM
CPUGT_PWM1
XW7410 SM
PLACE_NEAR=U7410.32:2MM
PVCCCGT_PH1_AGND
CPUGT_SW1 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 DIDT=TRUE SWITCH_NODE=TRUE
L7410 0.22UH-20%-44A-0.00190HM PILA082D-SM
NO_XNET_CONNECTION=1
PPVCCGT_CPU_PH1 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=1.5V
R7418 2.2 5% 1/10W MF-LF 603 NOSTUFF
CPUGT_SW1_SNUB DIDT=TRUE
C7418 0.001UF 10% 50V X7R-CERM 0402 NOSTUFF
CPUGT_BOOT1 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
R7419 0 5% 1/10W MF-LF 402
CPUGT1_DRVH DIDT=TRUE SWITCH_NODE=TRUE
CPUGT_BP1 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
C7419 0.22UF 10% 25V X7R 0402
MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
CPUGT_PHASE1
R7410 0.00075 1% 1W MF 0612-1
C7410 33UF 20% 16V TANT-POLY CASE-B3
C7411 33UF 20% 16V TANT-POLY CASE-B3
C7412 33UF 20% 16V TANT-POLY CASE-B3
C7413 2.2UF 20% 25V X6S-CERM 0402
C7414 33UF 20% 16V TANT-POLY CASE-B3
C7415 12PF 5% 25V NP0-C0G 0201
CPUGT_ISNS1_P
CPUGT_ISNS1_N
R7411 2.2 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUGT_ISUMN
R7412 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7413 200K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7414 200K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUGT_ISNS2_N
R7415 200K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUGT_ISNS3_N
CPUGT_ISEN1
CPUGT_ISUMP
PPVCCGT_S0_CPU
Vout = 0.55 - 1.5V
IccMax = 64A
F = 750kHz
C7440 CRITICAL 12PF 5% 25V NP0-C0G 0201 2.4G DESENSE
C7441 CRITICAL 3.0PF +/-0.1PF 25V NP0-C0G 0201 5G DESENSE

CPU VCCGT/GTx Phase 2

PPBUS_HS_CPU
PP5V_S0
R7426 1 5% 1/10W MF-LF 402 VOLTAGE=5V PP5V_S0_VGT2
C7427 2.2UF 20% 25V X6S-CERM 0402
PVCCCGT_PH2_AGND
C7426 2.2UF 20% 25V X6S-CERM 0402
U7420 FDMF5808A VIN PQFN-COMBO-THICKSTNCL OMIT_TABLE CRITICAL
VIN VCC PVCC BOOT PHASE SW SW GL0 GL1 GH FCCM PWM NC NC NC NC AGND AGND PGND PGND
CPUGT_FCCM
CPUGT_PWM2
XW7420 SM
PLACE_NEAR=U7420.32:2MM
PVCCCGT_PH2_AGND
CPUGT_SW2 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 DIDT=TRUE SWITCH_NODE=TRUE
L7420 0.22UH-20%-44A-0.00190HM PILA082D-SM
NO_XNET_CONNECTION=1
PPVCCGT_CPU_PH2 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=1.5V
R7428 2.2 5% 1/10W MF-LF 603 NOSTUFF
CPUGT_SW2_SNUB DIDT=TRUE
C7428 0.001UF 10% 50V X7R-CERM 0402 NOSTUFF
CPUGT_BOOT2 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
R7429 0 5% 1/16W MF-LF 402
CPUGT_BP2 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
C7429 0.22UF 10% 25V X7R 0402
MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
CPUGT_PHASE2
R7420 0.00075 1% 1W MF 0612-1
C7420 33UF 20% 16V TANT-POLY CASE-B3
C7421 33UF 20% 16V TANT-POLY CASE-B3
C7490 33UF 20% 16V TANT-POLY CASE-B3
C7423 2.2UF 20% 25V X6S-CERM 0402
C7424 2.2UF 20% 25V X6S-CERM 0402
C7425 12PF 5% 25V NP0-C0G 0201
CPUGT_ISNS2_P
CPUGT_ISNS2_N
R7421 2.2 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUGT_ISUMN
R7422 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7423 200K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7424 200K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUGT_ISNS1_N
R7425 200K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUGT_ISNS3_N
CPUGT_ISEN2
CPUGT_ISUMP
C7442 CRITICAL 12PF 5% 25V NP0-C0G 0201 2.4G DESENSE
C7443 CRITICAL 3.0PF +/-0.1PF 25V NP0-C0G 0201 5G DESENSE

CPU VCCGT/GTx Phase 3

PPBUS_HS_CPU
PP5V_S0
R7436 1 5% 1/10W MF-LF 402 VOLTAGE=5V PP5V_S0_VGT3
C7437 2.2UF 20% 25V X6S-CERM 0402
PVCCCGT_PH3_AGND
C7436 2.2UF 20% 25V X6S-CERM 0402
U7430 FDMF5808A VIN PQFN-COMBO-THICKSTNCL OMIT_TABLE CRITICAL
VIN VCC PVCC BOOT PHASE SW SW GL0 GL1 GH FCCM PWM NC NC NC NC AGND AGND PGND PGND
CPUGT_FCCM
CPUGT_PWM3
XW7430 SM
PLACE_NEAR=U7430.32:2MM
PVCCCGT_PH3_AGND
CPUGT_SW3 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 DIDT=TRUE SWITCH_NODE=TRUE
L7430 0.22UH-20%-44A-0.00190HM PILA082D-SM
NO_XNET_CONNECTION=1
PPVCCGT_CPU_PH3 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=1.5V
R7438 2.2 5% 1/10W MF-LF 603 NOSTUFF
CPUGT_SW_SNUB DIDT=TRUE
C7438 0.001UF 10% 50V X7R-CERM 0402 NOSTUFF
CPUGT_BOOT3 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
R7439 0 5% 1/16W MF-LF 402
CPUGT3_GL0 DIDT=TRUE SWITCH_NODE=TRUE
CPUGT_BP3 MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
C7439 0.22UF 10% 25V X7R 0402
CPUGT3_DRVH DIDT=TRUE SWITCH_NODE=TRUE
MIN_LINE_WIDTH=0.2500 MIN_NECK_WIDTH=0.2000 DIDT=TRUE
CPUGT_PHASE3
R7430 0.00075 1% 1W MF 0612-1
C7430 33UF 20% 16V TANT-POLY CASE-B3
C7431 33UF 20% 16V TANT-POLY CASE-B3
C7491 33UF 20% 16V TANT-POLY CASE-B3
C7433 2.2UF 20% 25V X6S-CERM 0402
C7434 2.2UF 20% 25V X6S-CERM 0402
C7435 12PF 5% 25V NP0-C0G 0201
CPUGT_ISNS3_P
CPUGT_ISNS3_N
R7431 2.2 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUGT_ISUMN
R7432 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7433 200K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
R7434 200K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUGT_ISNS1_N
R7435 200K 1% 1/20W MF 201 NO_XNET_CONNECTION=1
CPUGT_ISNS2_N
CPUGT_ISEN3
CPUGT_ISUMP

CPUGT_FCCM → P2MM SM PP7412
CPUGT1_DRVH → P2MM SM PP7411
CPUGT3_DRVH → P2MM SM PP7431
CPUGT3_GL0 → P2MM SM PP7430

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	3	IC,FDMF808A,DRMOS,IMVP8,50A,PQFN31,5X5	U7410, U7420, U7430	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: GT & GTX IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 74 OF 145
SHEET: 70 OF 119

8	7	6	5	4	3	2	1

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SYNC_MASTER=J79_SILUCHEN SYNC_DATE=03/27/2015

PAGE TITLE

Empty

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 75 OF 145

SHEET 71 OF 119

8 7 6 5 4 3 2 1

5V S4 - V5
5.14V Norm

3.3V DSW - V6

PPBUS_HS_OTH5V
PPBUS_HS_OTH3V3
PP5V_S4
PP5V_S5
PP3V3_S5

C7600 33UF 20% 16V TANT-POLY CASE-B3
C7601 2.2UF 20% 25V X6S-CERM 0402
C7602 2.2UF 20% 25V X6S-CERM 0402
C7603 12PF 5% 25V NP0-C0G 0201
C7650 1.0UF 10% 25V X5R 0402
C7651 CRITICAL 10UF 20% 16V X5R-CERM 0402-7
C7652 0.22UF 10% 16V CERM 402
C7653 2.2UF 20% 16V X5R-CERM 402
C7682 12PF 5% 25V NP0-C0G 0201
C7660 33UF 20% 16V TANT-POLY CASE-B3
C7661 33UF 20% 16V TANT-POLY CASE-B3
C7662 33UF 20% 16V TANT-POLY CASE-B3
C7675 33UF 20% 16V TANT-POLY CASE-B3
C7664 2.2UF 20% 25V X6S-CERM 0402
C7663 2.2UF 20% 25V X6S-CERM 0402

OMIT_TABLE
L7600 2.2UH-20%-4.5A-0.043OHM IHLP1616BZ-PIMA042T-COMBO
MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520

L7660 1.0UH-20%-14A-0.0107OHM PIMB062D-SM

U7600 CSD58879Q3D Q3D
VIN 1, TG 3, TGR 4, VSW 7, 8, BG 5, PGND 9

U7660 CSD58873Q3D Q3D
VIN 1, TG 3, TGR 4, VSW 7, 8, BG 5, PGND 9

CRITICAL U7650 TPS51980A QFN
SKIPSEL1 6, SKIPSEL2 19, OCSEL 14, VBST1 31, DRVH1 1, SW1 32, DRVL1 30, CSP1 7, CSN1 8, MODE 11, VFB1 9, COMP1 10, EN1 4, PGOOD1 5, GND 28, THRM_PAD 33
VBST2 26, DRVH2 24, SW2 25, DRVL2 27, CSP2 18, CSN2 17, RF 3, VFB2 16, COMP2 15, EN2 21, PGOOD2 20
VSW 2, VIN 23, VREG5 29, VREG3 22, VREF2 13
EN 12

P5VP3V3_VREG3
P5VP3V3_VREF2
P5VP3V3_SKIPSEL
SKIP_5V3V3:INAUDIBLE
SKIP_5V3V3:AUDIBLE

P5VS4_TG MIN_LINE_WIDTH=0.0800 MIN_NECK_WIDTH=0.2000 GATE_NODE=TRUE DIDT=TRUE
P5VS4_VBST_R MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520
P5VS4_VSW MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520
P5VS4_VBST SWITCH_NODE=TRUE DIDT=TRUE
P5VS4_DRVH DIDT=TRUE GATE_NODE=TRUE
P5VS4_SW DIDT=TRUE SWITCH_NODE=TRUE
P5VS4_DRVL DIDT=TRUE GATE_NODE=TRUE
P5VS4_CSP1 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520
P5VS4_CSN1 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520
P5VS4_VFB1 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520
P5VS4_COMP1 MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520
P5VS4_EN
P5VS4_PGOOD
P5VS5_EN
S5_PWRGD

P3V3S5_TG MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 GATE_NODE=TRUE
P3V3S5_VBST_R MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520
P3V3S5_VBST DIDT=TRUE SWITCH_NODE=TRUE
P3V3S5_DRVH DIDT=TRUE GATE_NODE=TRUE
P3V3S5_SW DIDT=TRUE SWITCH_NODE=TRUE
P3V3S5_DRVL DIDT=TRUE GATE_NODE=TRUE
P3V3S5_CSP2
P3V3S5_CSN2
P3V3S5_RF
P3V3S5_VFB2
P3V3S5_COMP2
P3V3S5_EN
P3V3S5_VSW MIN_NECK_WIDTH=0.0520 MIN_LINE_WIDTH=0.0900
P3V3S5_DRVL_R DIDT=TRUE GATE_NODE=TRUE
P3V3S5_SNUBR MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 DIDT=TRUE SWITCH_NODE=TRUE
P3V3S5_VFB2_R
P3V3S5_VFB2_RR
P3V3S5_COMP2_R
P3V3S5_CSP2_R DIDT=TRUE

R7650 0 5% 1/20W MF 0201
R7651 1 5% 1/20W MF 0201
R7665 1 5% 1/20W MF 201
R7609 0 5% 1/20W MF 201
R7685 1 5% 1/20W MF 201
R7669 0 5% 1/20W MF 201
R7686 0 5% 1/20W MF 201
R7694 10 1% 1/10W MF-LF 603
R7655 200K 1% 1/20W MF 201
R7693 1.58K 1% 1/20W MF 201
R7692 3.83K 1% 1/20W MF 201
R7695 3.92K 1% 1/20W MF 201
R7696 10K 1% 1/20W MF 201
R7675 3.92K 1% 1/20W MF 201
R7676 10K 1% 1/20W MF 201
R7672 4.87K 1% 1/20W MF 201
R7673 698 1% 1/20W MF 201
R7674 1 5% 1/10W MF-LF 603
R7677 200 1% 1/20W MF 201
R7678 41.2K 0.1% 1/16W MF 0402
R7679 10K 0.1% 1/16W MF 0402
R7697 402 1% 1/20W MF 201
R7698 23.2K 0.1% 1/16W MF 0402
R7699 10K 0.1% 1/16W MF 0402

C7609 0.1UF 10% 25V X6S-CERM 0201
C7671 0.1UF 10% 25V X6S-CERM 0201
C7673 0.1UF 10% 6.3V X7R 0201
C7693 0.1UF 10% 6.3V X7R 0201
C7674 0.0033UF 10% 16V X7R-CERM 402
C7694 0.001UF 10% 16V X7R-CERM 0402
C7678 270PF 10% 16V X7R-CERM 0201-1
C7679 4700PF 10% 16V X7R 201
C7699 2700PF 10% 16V X7R-CERM 201
C7698 330PF 10% 16V X7R 0201
C7606 2.2UF 20% 25V X6S-CERM 0402
C7607 150UF 20% 6.3V TANT-POLY CASE-B1S-1
C7608 2.2UF 20% 25V X6S-CERM 0402
C7605 150UF 20% 6.3V TANT-POLY CASE-B1S-1
C7665 150UF 20% 6.3V TANT-POLY CASE-B1S-1
C7666 150UF 20% 6.3V TANT-POLY CASE-B1S-1
C7667 150UF 20% 6.3V TANT-POLY CASE-B1S-1
C7668 150UF 20% 6.3V TANT-POLY CASE-B1S-1
C7672 150UF 20% 6.3V TANT-POLY CASE-B1S-1
C7676 150UF 20% 6.3V TANT-POLY CASE-B1S-1
C7669 2.2UF 20% 25V X6S-CERM 0402
C7670 2.2UF 20% 25V X6S-CERM 0402

XW7675 SM, XW7671 SM, XW7670 SM, XW7650 SM, XW7695 SM, XW7691 SM, XW7690 SM

PLACE_NEAR=L7600.1:3MM
PLACE_NEAR=L7600.2:3MM
PLACE_NEAR=U7650.28:1MM
PLACE_NEAR=L7660.1:3MM
PLACE_NEAR=L7660.2:3MM

5VS4_VFB1_RR
P5VS4_VFB1_R
P5VS4_CSP1_R
P5VS4_COMP1_R
P3V3S5_VFB2_R
P3V3S5_VFB2_RR
P3V3S5_COMP2_R
P3V3S5_CSP2_R

Change R7677 to 200 Ohm 1% and R7678 to 41.2K 0.1% in Proto-2.

GND_5V3V3_AGND MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=0V

CRITICAL C7610 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITICAL C7611 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE
CRITICAL C7612 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITICAL C7613 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE
CRITICAL C7614 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITICAL C7615 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE
CRITICAL C7683 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITICAL C7684 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE
CRITICAL C7685 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITICAL C7686 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE
CRITICAL C7687 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITICAL C7688 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00182	1	IND,PWR,2.2UH,20%,4.5A,43MOHM,4X4MM	L7600	CRITICAL	

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: Power - 5V 3.3V Supply

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 76 OF 145
SHEET: 72 OF 119

1V EDRAM & EOPIO

PPBUS_HS_CPU

PPVCCEDRAM_S0_REG_F

PP5V_S0

C7709 33UF 20% 16V TANT-POLY CASE-B3

C7700 33UF 20% 16V TANT-POLY CASE-B3

C7701 2.2UF 20% 25V X6S-CERM 0402

C7704 2.2UF 20% 25V X6S-CERM 0402

C7702 10UF 20% 16V X5R-CERM 0402-1

C7703 10UF 20% 16V X5R-CERM 0402-1

C7730 0.1UF 10% 25V X6S-CERM 0201

PVCCEDRAM_BOOT_RC

R7730 2.2 5% 1/20W MF 201

PVCCEDRAM_VBST

PVCCEDRAM_DRVH

R7731 1 5% 1/20W MF 201

P1VEDRAM_DRVH_R

Q7700 CSD58873Q3D Q3D

U7700 TPS51916 QFN CRITICAL

PVCCEDRAM_LL

R7732 1 5% 1/20W MF 201

P1VEDRAM_DRVL_R

PVCCEDRAM_DRVL

PVCCEDRAM_VTT

PVCCEDRAM_VTTREF

L7700 1UH-20%-11A-0.0127OHM IHLP2020BD-P1MA05ZD-COMBO

R7718 0.005 1% 1/2W MF 0306-SHORT

OMIT

VOLTAGE=1.00V MIN_NECK_WIDTH=0.0520 MIN_LINE_WIDTH=0.0900

PPVCCEDRAM_S0_REG_F

Vout = 1.05V

5.2A MAX OUTPUT

F = 500 KHZ

PPVCCEDRAM_PHASE

PPVCCEDRAM_S0_REG_R

ISNS_CPUEDRAM_P

ISNS_CPUEDRAM_N

R7710 2.2 5% 1/10W MF-LF 0603

PVCCEDRAM_LL_SNUB

C7710 0.001UF 10% 50V X7R-CERM 0402

C7705 10UF 20% 6.3V X6S 0402

C7706 10UF 20% 6.3V X6S 0402

C7707 220UF 20% 2V ELEC SM-COMBO

C7708 220UF 20% 2V ELEC SM-COMBO

C7711 220UF 20% 2V ELEC SM-COMBO

C7714 220UF 20% 2V ELEC SM-COMBO

C7712 270UF 20% 2V TANT CASE-B

XW7710 SM

C7715 0.1UF 10% 6.3V X6S 0201

R7711 30.9K 0.1% 1/20W MF 0201

R7719 3.09K 1% 1/20W MF 201

R7712 48.7K 0.1% 1/20W MF 0201

C7716 0.01UF 10% 16V X7R-CERM 0201

R7715 1K 1% 1/20W MF 201

R7713 33K 1% 1/20W MF 201

R7714 35.7K 1% 1/20W MF 201

C7740 0.22UF 20% 16V CERM-X5R 0201

XW7700 SM

PVCCEDRAM_AGND

PVCCEDRAM_VREF_R

PVCCEDRAM_S3_EN

PVCCEDRAM_VREF

PVCCEDRAM_REFIN

PVCCEDRAM_MODE

PVCCEDRAM_TRIP

ALL_SYS_PWRGD

Scrub S3 & S5 pins connections!

P1VOPC_SNS

R7741 10 5% 1/20W MF 201

P1VOPC_SNS_R

PM_PCH_SYS_PWROK

Calculated OCP: min=6.34A, typ=12.07A, max=22.35A

THE FOLLOWING SHORTCUTS ARE USED:
- OPC (EDRAM) IS POWERED FROM ONE VR.
- LOAD SWITCHES ARE USED TO MEET THE TURN-ON TIMING.
- MSM# IS NOT USED.

NC_CPU_MSM_L = NC_CPU_MSM_L MAKE_BASE=TRUE

PM_PCH_SYS_PWROK = PM_PCH_SYS_PWROK MAKE_BASE=TRUE

ALL_SYS_PWRGD = ALL_SYS_PWRGD MAKE_BASE=TRUE

LEVEL SHIFT

PP1V0_S3

PP3V3_S0

PM_SLP_S3_L

C7790 0.1UF 10% 10V X5R-CERM 0201

U7790 74AUP1G07GF SOT891

R7791 100K 5% 1/20W MF 201

R7792 100K 5% 1/20W MF 201

CPU_ZVM_L

PM_OPC_ZVM_L

ZVM is CMOS DC Output:
V_OL Max = Vcc * 0.1V
V_OH Min = Vcc * 0.9V
Vcc referred to in these specs refers to VccST/IO

SLG5AP031 EN:
V_IL Max = 1V
V_IH Min = 2V

PP5V_S0

C7760 0.1UF 10% 10V X5R-CERM 0201

U7760 SLG5AP031 TDFN

PM_OPC_ZVM_L

SWEOPIO_CNFG

R7760 2.2M 5% 1/20W MF 201

SWEOPIO_G

PPVCCEDRAM_S0_CPU

Q7760 FDMC7570S POWER33

Q7761 FDMC7570S POWER33

C7761 20UF 20% 25V X6S-CERM 0402-1

R7790 10K 1% 1/20W MF 201

PP3V3_S0

PM_PCH_SYS_PWROK

C7762 CRITICAL 12PF 5% 25V NP0-C0G 0201

C7763 CRITICAL 3.0PF +/-0.1PF 25V NP0-C0G 0201

2.4G DESENSE

5G DESENSE

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: Power - EOPIO EDRAM Supply

Apple Inc.

DRAWING NUMBER: 051-00777

SIZE: D

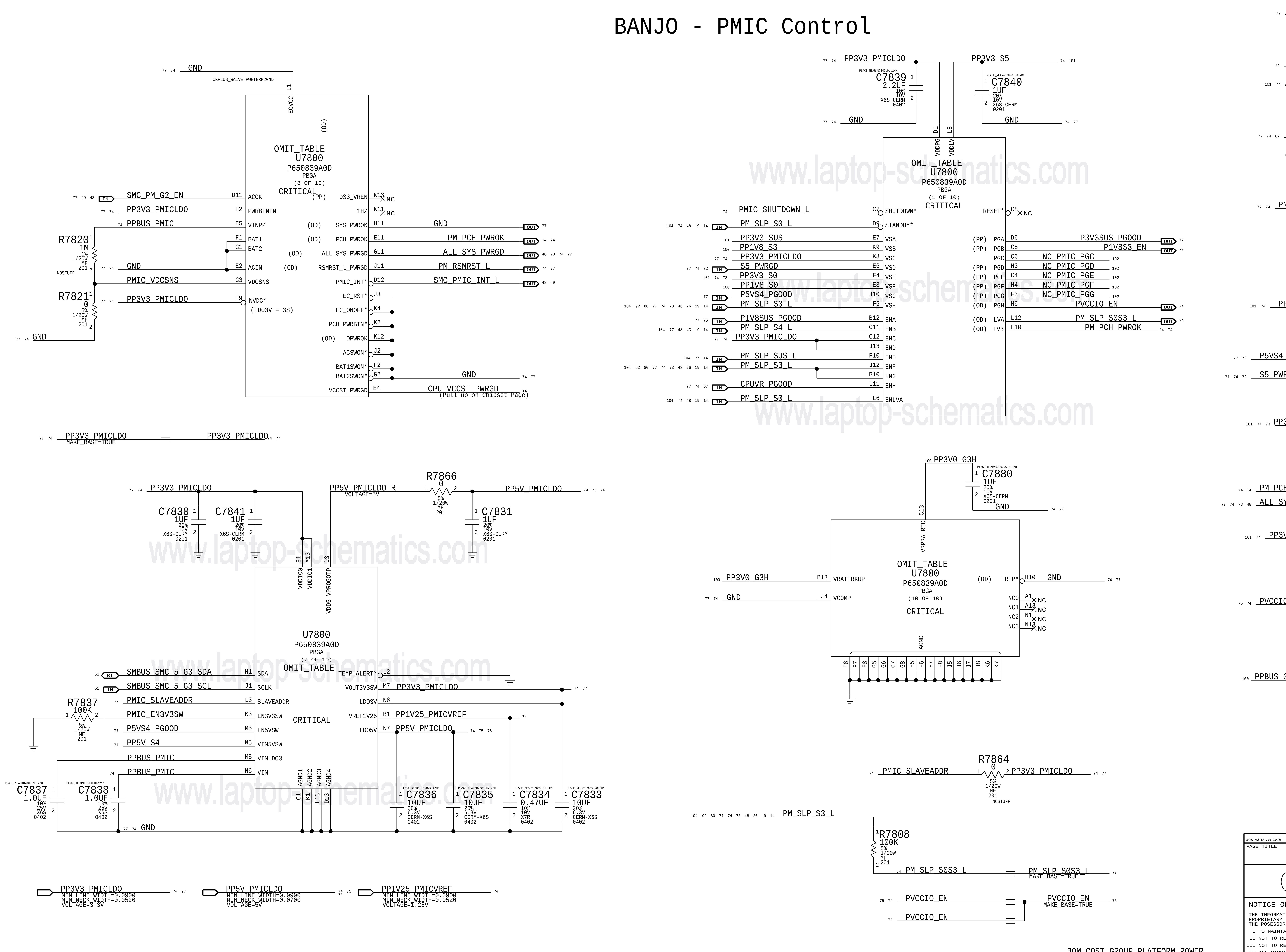
REVISION: 9.0.0

BRANCH: dvt-fab09-0

PAGE: 77 OF 145

SHEET: 73 OF 119

BANJO - PMIC Control



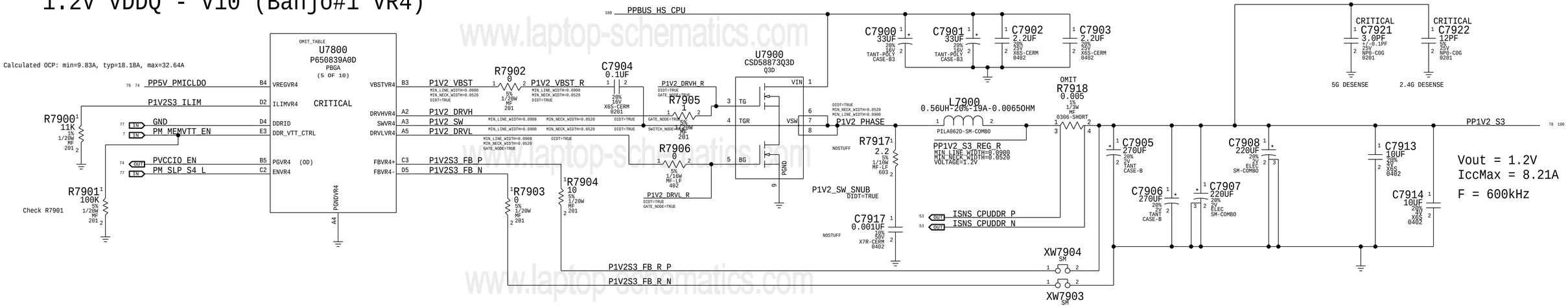
BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
PMIC-1 & Power Control

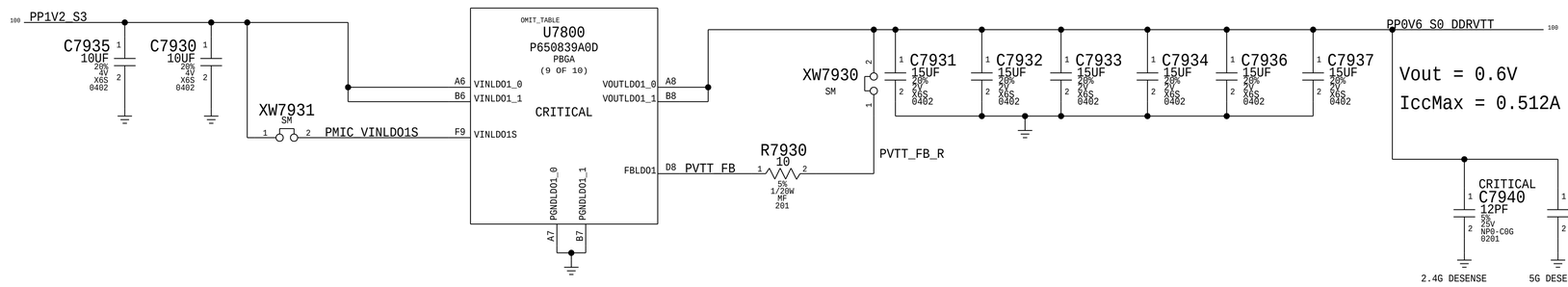
Apple Inc.

DRAWING NUMBER 051-00777 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 78 OF 145
SHEET 74 OF 119

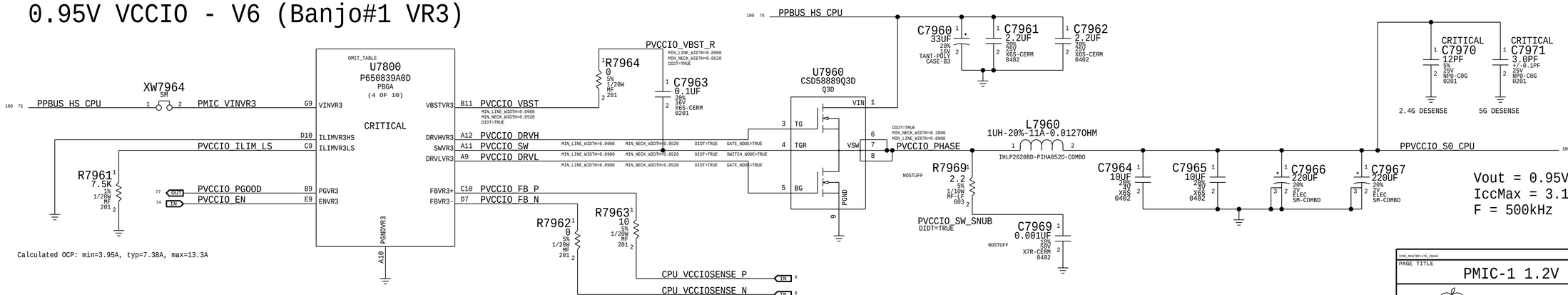
1.2V VDDQ - V10 (Banjo#1 VR4)



0.6V VTT - V13 (Banjo#1 LDO1)



0.95V VCCIO - V6 (Banjo#1 VR3)



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J79_J5940 SYNC_DATE=12/03/2010

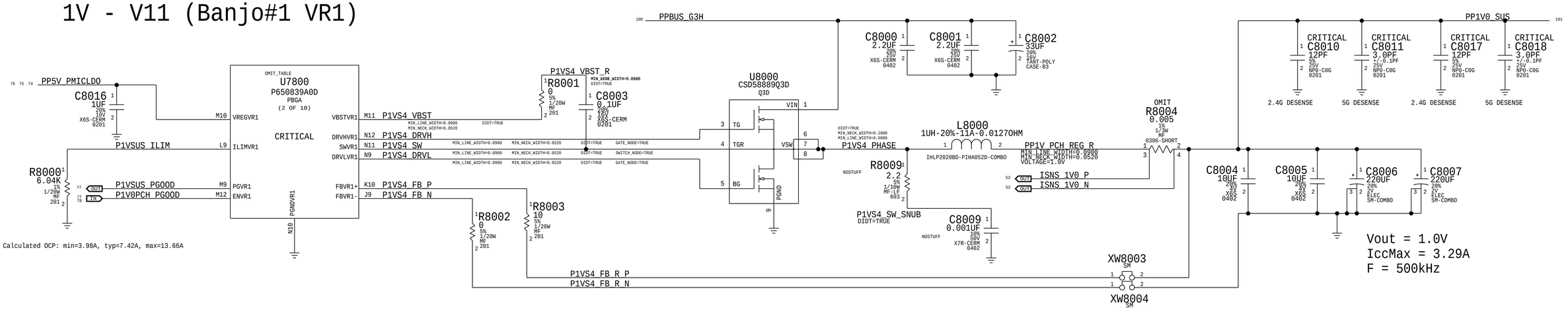
PAGE TITLE

PMIC-1 1.2V 0.6V VCCIO

Apple Inc.

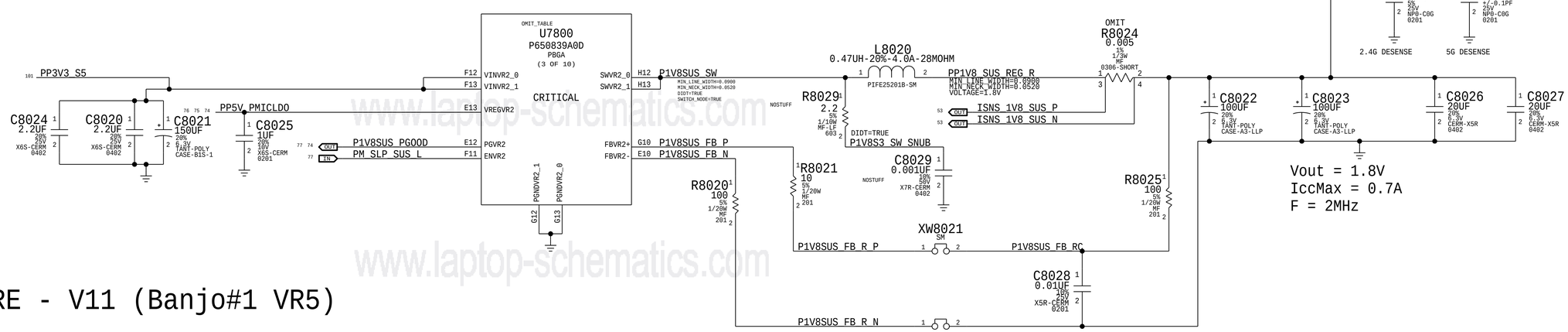
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	79 OF 145
SHEET	75 OF 119

1V - V11 (Banjo#1 VR1)

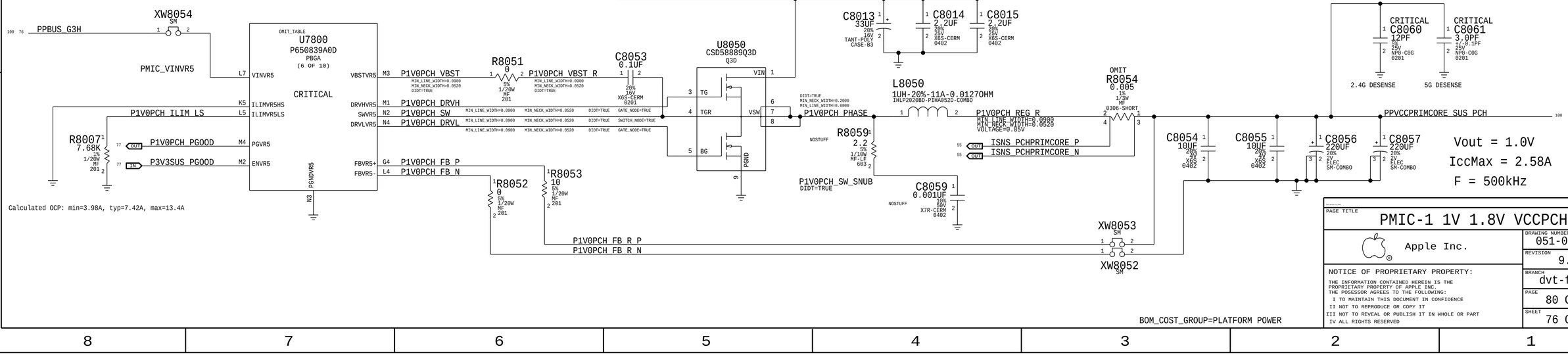


Calculated OCP: min=3.98A, typ=7.42A, max=13.66A

1.8V - V8 (Banjo#1 VR2)



1.0V PCH CORE - V11 (Banjo#1 VR5)
0.7V LPM



Calculated OCP: min=3.98A, typ=7.42A, max=13.4A

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE	PMIC-1 1V 1.8V VCCPCH
Apple Inc.	DRAWING NUMBER 051-00777
	SIZE D
	REVISION 9.0.0
	BRANCH dvt-fab09-0
	PAGE 80 OF 145
	SHEET 76 OF 119

S5 Enables

74 49 48 SMC_PM_G2_EN — R8110 0 5% 1/20W MF 201 — PMIC_EN_P3V3S5 77
MAKE_BASE=TRUE

SUS Enables

104 74 14 PM_SLP_SUS_L — PM_SLP_SUS_L 76; PM_SLP_SUS_L 78
MAKE_BASE=TRUE

S4 Enables

104 48 19 14 PM_SLP_S5_L — PM_SLP_S5_L 78; PM_SLP_S5_L 78; PM_SLP_S5_L 77
MAKE_BASE=TRUE

S3 Enables

104 77 74 48 43 19 14 PM_SLP_S4_L — PM_SLP_S4_L 75
MAKE_BASE=TRUE

S0 Enables

104 92 80 74 73 48 26 19 14 PM_SLP_S3_L — PM_SLP_S3_L 77; PM_SLP_S3_L 78; PM_SLP_S3_L 78
MAKE_BASE=TRUE

S0i Enables

77 IN P1VS0SW_EN_RC — P1VS0SW_EN_RC OUT 78
MAKE_BASE=TRUE

77 74 IN PM_SLP_S0S3_L — PM_SLP_S0S3_L OUT 78
MAKE_BASE=TRUE

74 PP3V3_PMICLDO — PP3V3_PMICLDO 74
MAKE_BASE=TRUE

101 PP5V_S4 — PP5V_S4 74

74 72 P5VS4_PGOOD — P5VS4_PGOOD 74; P5VS4_PGOOD 74
MAKE_BASE=TRUE

77 76 P1V0PCH_PGOOD — P1V0PCH_PGOOD 76 78
MAKE_BASE=TRUE

77 74 GND — GND 75
MAKE_BASE=TRUE

74 P3V3SUS_PGOOD — P3V3SUS_PGOOD 76
MAKE_BASE=TRUE

77 74 GND — GND 74
MAKE_BASE=TRUE

74 73 48 ALL_SYS_PWRGD — ALL_SYS_PWRGD 67
MAKE_BASE=TRUE

74 72 S5_PWRGD — S5_PWRGD 48
MAKE_BASE=TRUE

48 17 14 PM_RSMRST_L — PM_RSMRST_L 74
MAKE_BASE=TRUE

77 74 GND
MAKE_BASE=TRUE

77 SSD_PWR_REQ — SSD_PWR_REQ IN 84 88
MAKE_BASE=TRUE

74 67 CPUVR_PGOOD — P2MM SM PP — PP8100

117 75 PVCCIO_PGOOD — P2MM SM PP — PP8101

115 76 P1VSUS_PGOOD — P2MM SM PP — PP8102

120 76 74 P1V8SUS_PGOOD — P2MM SM PP — PP8106

129 77 76 P1V0PCH_PGOOD — P2MM SM PP — PP8107

KEEP THESE RAILS ON WHEN USING XDP

101 77 17 PP3V3_SUS
XDP:YES C8192 0.1UF 10% 10V X5R-CERM 0201
XDP:YES U8192 74AUP1T97GM SOT886 (S4# OR XDP)
77 17 IN XDP_PRESENT_L — (INV)
104 77 74 48 43 19 14 IN PM_SLP_S4_L
P1V0S3_EN OUT 78
XDP:YES R8192 100K 5% 1/20W MF 201
XDP:NO R8193 0 5% 1/20W MF 201

101 77 17 PP3V3_SUS
XDP:YES C8194 0.1UF 10% 10V X5R-CERM 0201
XDP:YES U8194 74AUP1T97GM SOT886 (S3# AND S0# OR XDP)
77 17 IN XDP_PRESENT_L — (INV)
77 74 IN PM_SLP_S0S3_L
P1VS0SW_EN_RC OUT 77
XDP:YES R8194 100K 5% 1/20W MF 201
XDP:NO R8195 0 5% 1/20W MF 201

100 PP3V3_G3H
C8190 0.1UF 10% 10V X5R-CERM 0201
U8190 74LVC1G32 SOT891
77 PMIC_EN_P3V3S5 — PM_EN_PVXS5 MAKE_BASE=TRUE
77 IN SSD_PWR_REQ — PM_EN_PVXS5 77; PM_EN_PVXS5 77
NC
R8190 100K 5% 1/20W MF 201

R8160 0 5% 1/20W MF 201
77 PM_EN_PVXS5 — P5VS5_EN OUT 72

77 PM_EN_PVXS5 — R8162 0 5% 1/20W MF 201 — P3V3S5_EN OUT 72
R8165 100 5% 1/20W MF 201
D8164 SM-201
NO STUFF P3V3S5_EN_RD
RB521ZS-30 NO STUFF
C8155 1UF 10% 10V X5S-CERM 0402 NO STUFF

77 PM_SLP_S5_L — R8163 0 5% 1/20W MF 201 — P5VS4_EN OUT 72
R8164 100 5% 1/20W MF 201
D8163 SM-201
NO STUFF P5VS4_EN_RD
RB521ZS-30 NO STUFF
C8154 1UF 10% 10V X5S-CERM 0402 NO STUFF

77 PM_SLP_S3_L — R8166 0 5% 1/20W MF 201 — P5VS0_EN OUT 78
R8167 100 5% 1/20W MF 201
D8165 SM-201
NO STUFF P5VS0_EN_RD
RB521ZS-30 NO STUFF
C8156 1UF 10% 10V X5S-CERM 0402 NO STUFF

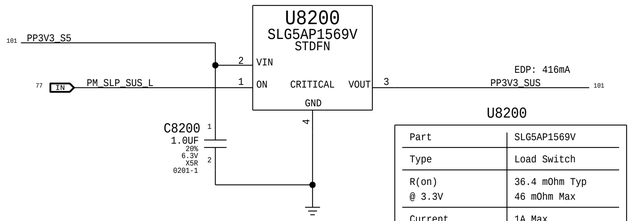
BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: PMIC-1 Aliases & TPs

Apple Inc.

DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	81 OF 145
SHEET	77 OF 119

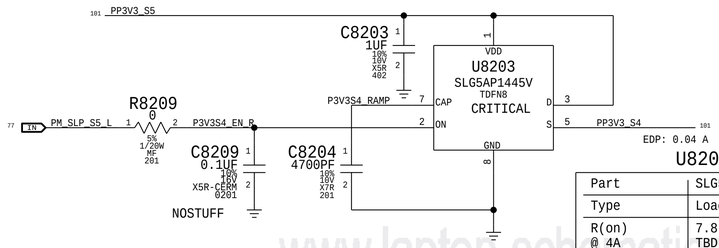
3.3V SUS Switch



U8200

Part	SLG5AP1569V
Type	Load Switch
R(on) @ 3.3V	36.4 mOhm Typ 46 mOhm Max
Current	1A Max

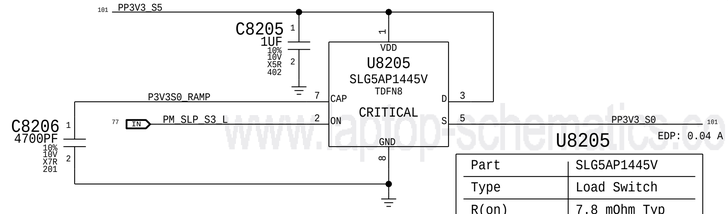
3.3V S4 Switch



U8203

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

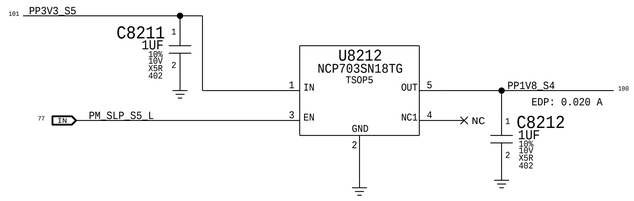
3.3V S0 Switch



U8205

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

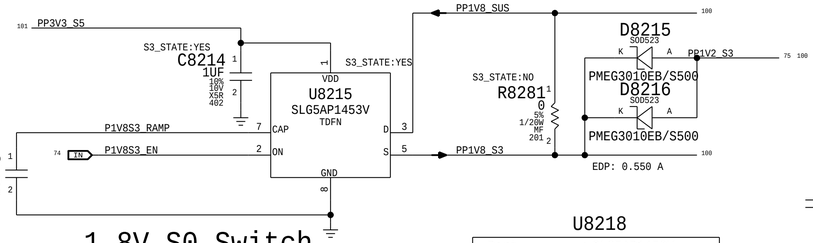
1.8V S4 LDO



U8215

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

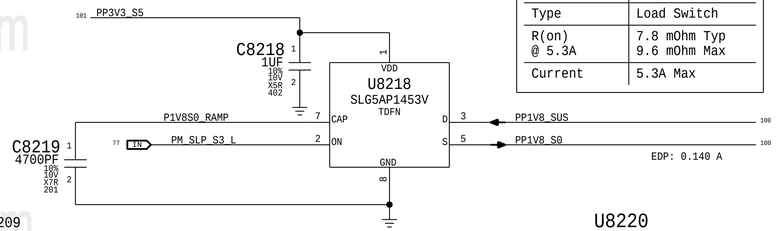
1.8V S3 Switch



U8218

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

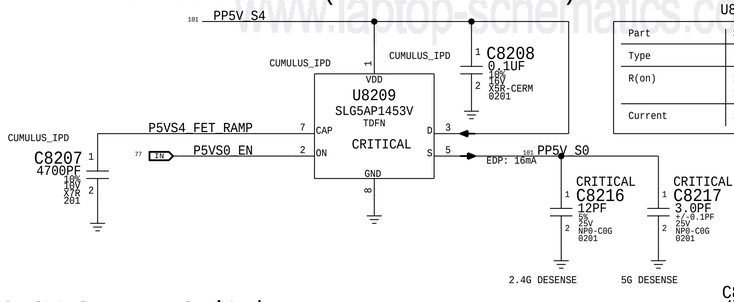
1.8V S0 Switch



U8209

Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

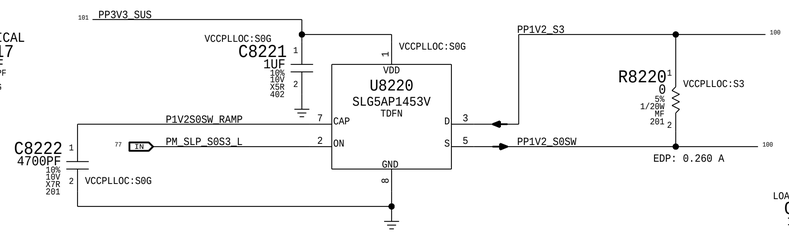
5V S0 Switch (Cumulus vs Kona)



U8220

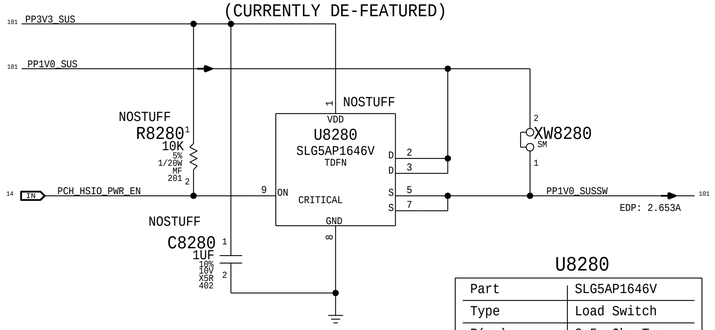
Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

1.2V S0 SW Switch



1.0V SUS SW Switch

(CURRENTLY DE-FEATURED)

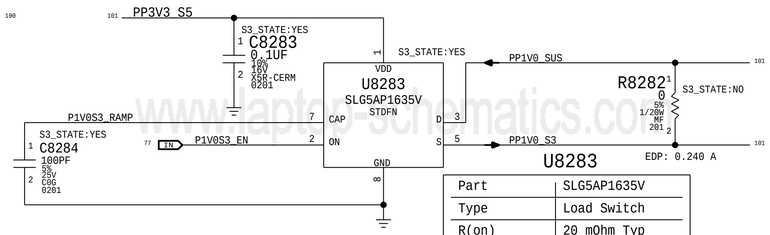


HSIO has turn-on requirement of
<0.1V/uS ramp rate and
<65uS from EN to 95% (1.05V)

U8280

Part	SLG5AP1646V
Type	Load Switch
R(on) @ 4V Vgs	8.5 mOhm Typ 9.8 mOhm Max
Current	6A Max

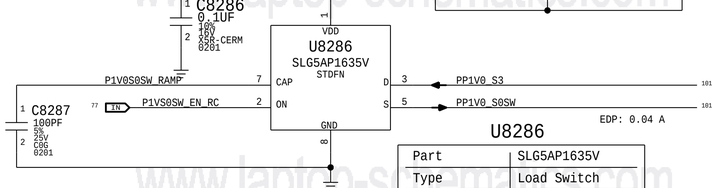
1.0V S3 Switch



U8283

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

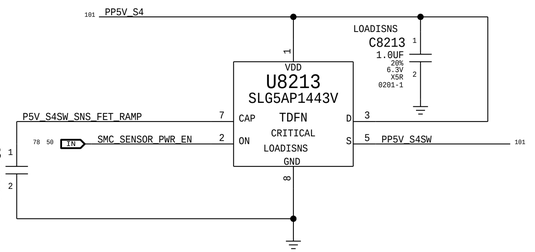
1.0V S0 SW Switch



U8286

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

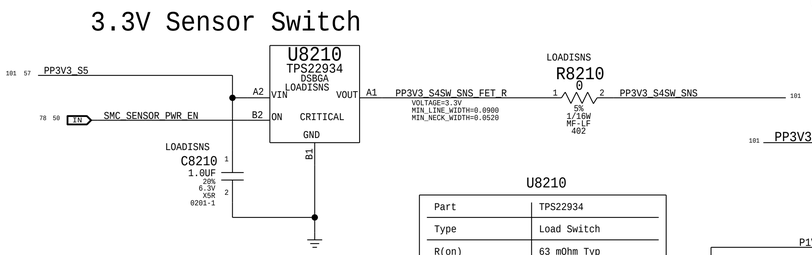
5V Sensor Switch



U8213

Part	SLG5AP1443V
Type	Load Switch
R(on)	17 mOhm Typ 19 mOhm Max
Current	2.5A

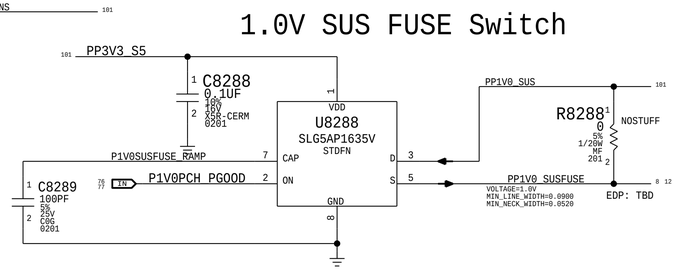
3.3V Sensor Switch



U8210

Part	TPS22934
Type	Load Switch
R(on) @ 3.6V	63 mOhm Typ 77 mOhm Max
Current	1A Max

1.0V SUS FUSE Switch



U8288

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V
R(discharge)	300 Ohm Max

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 82 OF 145
SHEET: 78 OF 119

Page Notes

Power aliases required by this page:
- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)

PPBUS_G3H
F8400 3AMP-32V 0603 740S0159
PPVIN_S0SW_LCDBKLT_F
R8400 0.025 1% 1W MF 0612-1 107S00034
PPVIN_S0SW_LCDBKLT_R
C8400 1000PF 10% 16V X7R-1 0201
R8401 80.6K 1% 1/16W MF-LF 402
Q8400 CRITICAL FDC638APZ_SBMS001 SSOT6-HF
C8401 NOSTUFF 0.001UF 10% 50V C0GNP 402
PPVIN_S0SW_LCDBKLT
MIN_LINE_WIDTH=2.0000
MIN_NECK_WIDTH=0.2000
VOLTAGE=12.9V
MAKE_BASE=TRUE
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
LCDBKLT_EN_L
R8402 63.4K 1% 1/16W MF-LF 402
PP5V_S0
R8444 0 5% 1/16W MF-LF 402
R8445 0 5% 1/16W MF-LF 402
PP5V_S0_BKLT_A
PP5V_S0_BKLT_D
C8440 1UF 10% 16V X5R 402
C8441 1UF 10% 16V X5R 402
GND_BKLT_SGND
R8440 1M 5% 1/20W MF 201
BKLT_SD
BKLT_SENSE_OUT
U8400 LLP LP8548B1SQ_-04
SD
VSENSE_N
VSENSE_P
SENSE_OUT
EN
PWM_KEYB
SCL (IPU)
SDA (IPU)
VDDD
VDDA
SW
SW
FB
GD
ISET_KEYB
KEYB1
KEYB2
SW2
FB2
GND_SW
GND_SW
GND_SW2
GNDD
GNDA
THRM PAD
LCDBKLT_SW
LCDBKLT_FB
LCDBKLT_FET_DRV
DIDT=TRUE
SWITCH_NODE=TRUE
VOLTAGE=55V
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=2.0000
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.2000
VOLTAGE=5V
GATE_NODE=TRUE
DIDT=TRUE
PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW
EDP_BKLT_EN
R8442 0 5% 1/20W MF 0201
BKLT_EN_R
C8442 NO STUFF 33PF 5% 25V NPO-C0G 0201
GND_BKLT_SGND
BKLT_PWM_KEYB
R8447 10K 5% 1/20W MF 201
XW8400 SM
GND_BKLT_SGND
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
VOLTAGE=0V
PP5V_S0
R8452 1.8K 5% 1/20W MF 201
R8453 1.8K 5% 1/20W MF 201
PLACE_NEAR=U8400.15:10MM
I2C_BKLT_SCL
I2C_BKLT_SDA
R8450 0 5% 1/20W MF 0201
R8451 0 5% 1/20W MF 0201
BKLT_SCL
BKLT_SDA
I2C ID DEDICATED.ONLY CONNECTS TO JERRY
PLACE_NEAR=U8400.16:10MM

PLACE_NEAR=Q8401.5:3MM
L8410 CRITICAL 15UH-20%-1.9A-0.24OHM PIME062D-SM 152S00253
C8410 4.7UF 10% 25V X6S-CERM 0603
C8411 4.7UF 10% 25V X6S-CERM 0603
C8412 0.1UF 10% 25V X5R 402
PLACEMENT_NOTE:
SANDWICH C8210 AND C8211
PLACE_NEAR=L8410.1:5MM
PLACE_NEAR=L8410.2:3MM
371S0704 or 371S00077 (Combo)
D8410 CRITICAL SOD123-COMBO PMEG10020ELR-DFLS2100
PPVIN_SW_LCDBKLT_SW
Q8401 CRITICAL SI7812DN PWRPK-1212-8
PLACE_NEAR=U8400.1:3MM
LCDBKLT_FET_DRV_R
R8433 10 5% 1/16W MF-LF 402
XW8410 SM
PLACE_NEAR=U8410.:2MM
LCDBKLT_TB_XWR
R8431 10.2K 1% 1/16W MF-LF 402
R8432 150K 1% 1/16W MF-LF 402
C8430 NOSTUFF 100PF 5% 100V C0G-CERM 0603
PPVOUT_S0_LCDBKLT
C8460 C8461 C8462 C8463 C8464 2.2UF 10% 100V X5R 1206
C8465 C8466 C8467 C8468 C8469 2.2UF 10% 100V X5R 1206
C8470 C8471 C8472 C8473 2.2UF 10% 100V X5R 1206
C8474 12PF 5% 100V C0G 0201
C8475 12PF 5% 100V C0G 0201
PLACE_NEAR=D8410.K:5MM

J79 DISPLAY
Vout = 46V Typ, 55V Max
Iout = 0.12A Typ, 0.15A Max
Fs = 625kHz Typ (+/- 7%)

LINE WIDTHS

PP5V_S0_BKLT_A: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
PP5V_S0_BKLT_D: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V
BKLT_SD: MIN_LINE_WIDTH=0.4500, MIN_NECK_WIDTH=0.2000

PBUS LINE WIDTHS

PPVIN_S0SW_LCDBKLT_F: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V
PPVIN_S0SW_LCDBKLT_R: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V
PPVIN_S0SW_LCDBKLT: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=12.9V

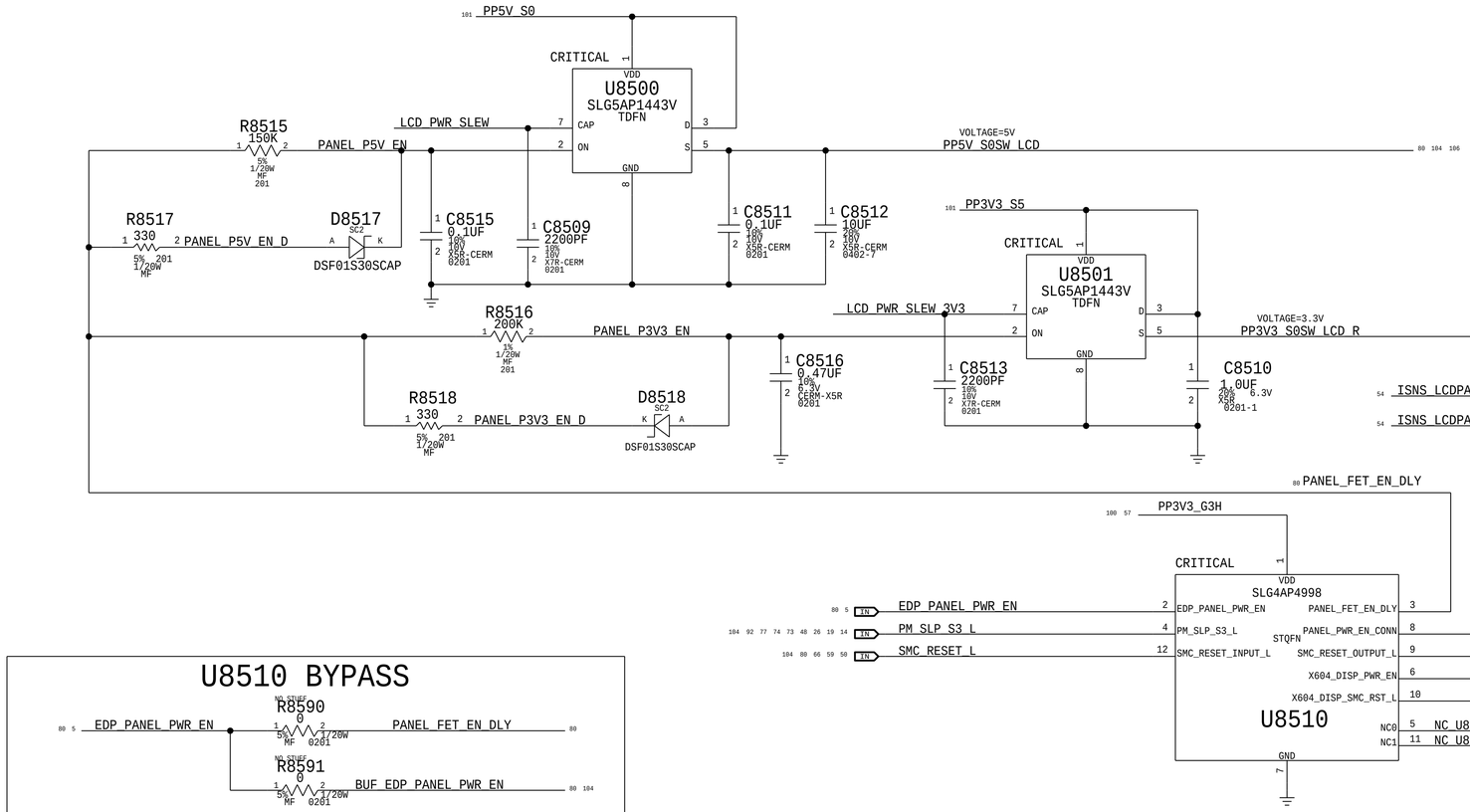
LCD BKLT LINE WIDTHS

LCDBKLT_FET_DRV_R: MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, VOLTAGE=5V, GATE_NODE=TRUE, DIDT=TRUE
PPVIN_SW_LCDBKLT_SW: MIN_LINE_WIDTH=2.0000, MIN_NECK_WIDTH=0.2000, VOLTAGE=55V, SWITCH_NODE=TRUE, DIDT=TRUE
PPVOUT_S0_LCDBKLT: MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.1500, VOLTAGE=5V

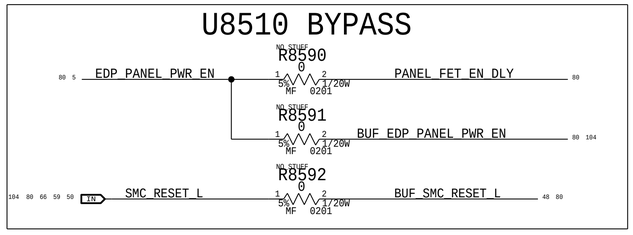
BOM_COST_GROUP=DISPLAY

PAGE TITLE: LCD Backlight Driver
Apple Inc.
DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 84 OF 145
SHEET: 79 OF 119

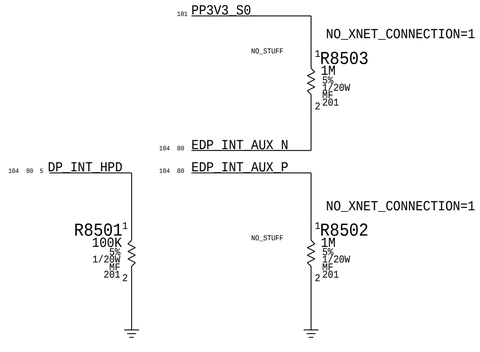
LCD PANEL INTERFACE (eDP) + Camera (MIPI)

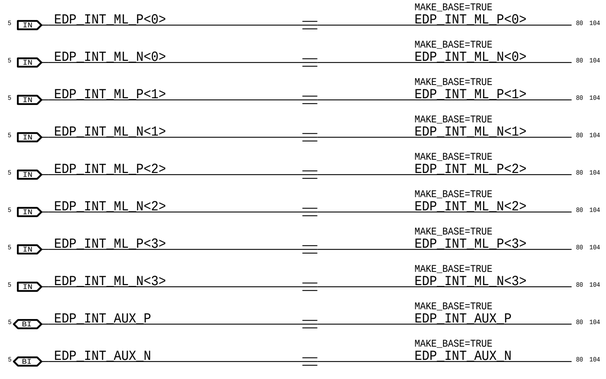


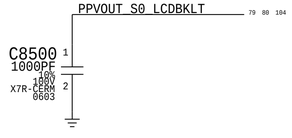
U8510 BYPASS



LCD Panel HPD & AUX strapping







PAGE TITLE	eDP Display Connector
	Apple Inc.
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	85 OF 145
SHEET	80 OF 119

BOM_COST_GROUP=DISPLAY

NAND LANDINGS

CONFIG	LANDING1 R8601	LANDING0 R8600
00 - 2	NOSTUFF	NOSTUFF
01 - 4	NOSTUFF	ASSEMBLE
10 - 8	ASSEMBLE	NOSTUFF
11 - RESERVED	ASSEMBLE	ASSEMBLE

OPERATION MODE (ODT, CLK FREQ, ETC)

CONFIG	OP_MODE2 R8614	OP_MODE1 R8615	OP_MODE0 R8680
000 - TEABERRY	NOSTUFF	NOSTUFF	NOSTUFF
001 - XB58 GS	NOSTUFF	NOSTUFF	ASSEMBLE
010 - RESERVED	NOSTUFF	ASSEMBLE	NOSTUFF
011 - RESERVED	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - RESERVED	ASSEMBLE	NOSTUFF	NOSTUFF
101 - RESERVED	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - RESERVED	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

NAND CONFIGURATION

CONFIG	ROMBOOT2 R8617	ROMBOOT1 R8618	ROMBOOT0 R8616
000 - MLC SD/TOS 1Y/1Z(W/ HARD RESET)	NOSTUFF	NOSTUFF	NOSTUFF
001 - MLC SD/TOS 1Y/1Z (W/O HARD RESET)	NOSTUFF	NOSTUFF	ASSEMBLE
010 - RESERVED	NOSTUFF	ASSEMBLE	NOSTUFF
011 - MLC HYNIX 3D-V2	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - RESERVED	ASSEMBLE	NOSTUFF	NOSTUFF
101 - RESERVED	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - RESERVED	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

PRODUCT CAPACITY

CONFIG	CAPACITY2 R8664	CAPACITY1 R8663	CAPACITY0 R8662
000 - 32GB	NOSTUFF	NOSTUFF	NOSTUFF
001 - 64GB	NOSTUFF	NOSTUFF	ASSEMBLE
010 - 128GB	NOSTUFF	ASSEMBLE	NOSTUFF
011 - 256GB	NOSTUFF	ASSEMBLE	ASSEMBLE
100 - 512GB	ASSEMBLE	NOSTUFF	NOSTUFF
101 - 1024GB	ASSEMBLE	NOSTUFF	ASSEMBLE
110 - 2048GB	ASSEMBLE	ASSEMBLE	NOSTUFF
111 - RESERVED	ASSEMBLE	ASSEMBLE	ASSEMBLE

OMIT_TABLE

U8600
S3X
BGA-H1P35
SYM 3 OF 7

REFCLK_P A19 PCIE_CLK100M_SSD_LB_P 91 105
REFCLK_M A18 PCIE_CLK100M_SSD_LB_N 91 105
PCIE_TX0_P A17 PCIE_SSD_D2R_C_P<0> 81
PCIE_TX0_M A16 PCIE_SSD_D2R_C_N<0> 81
PCIE_TX1_P A15 PCIE_SSD_D2R_C_P<1> 81
PCIE_TX1_M A14 PCIE_SSD_D2R_C_N<1> 81
PCIE_TX2_P A13 PCIE_SSD_D2R_C_P<2> 81
PCIE_TX2_M A12 PCIE_SSD_D2R_C_N<2> 81
PCIE_TX3_P A11 PCIE_SSD_D2R_C_P<3> 81
PCIE_TX3_M A10 PCIE_SSD_D2R_C_N<3> 81
PCIE_RX0_P C17 PCIE_SSD_R2D_LB_P<0> IN 84
PCIE_RX0_M C16 PCIE_SSD_R2D_LB_N<0> IN 84
PCIE_RX1_P C15 PCIE_SSD_R2D_P<1> IN 84
PCIE_RX1_M C14 PCIE_SSD_R2D_N<1> IN 84
PCIE_RX2_P C13 PCIE_SSD_R2D_P<2> IN 84
PCIE_RX2_M C12 PCIE_SSD_R2D_N<2> IN 84
PCIE_RX3_P C11 PCIE_SSD_R2D_P<3> IN 84
PCIE_RX3_M C10 PCIE_SSD_R2D_N<3> IN 84
DDR_ATO J21 NC_S3X_DDR_ATO 102
BOOT_FROM_LPSR AF17 S3X_COLD_BOOT_L IN 88
CLK_IN AG18 S3X_EXT_SE_24MHZ_CLK_IN
CLK_IN_SEL AD17 S3X_CLK_IN_SEL
PCIE_ATB0 G16 NC_S3X_PCIE_ATB0 102
PCIE_ATB1 G17 NC_S3X_PCIE_ATB1 102
PCIE_CLKREQ* F12 S3X_PCIE_CLKREQ_L BI 88
JTAG_TRST* AE18 S3X_JTAG_TRST_L IN 84 104
RESET* AF18 S3X_RESET_L IN 88
HOLD_RESET AH18 84 S3X_HOLD_RESET
PERST* E12 S3X_PERST_L IN 88
JTAG_SEL AG20 S3X_JTAG_SEL
JTAG_TCK AH19 S3X_JTAG_TCK IN 84 104
JTAG_TDI AH17 S3X_JTAG_TDI IN 84 104
JTAG_TDO AD20 S3X_JTAG_TDO OUT 84 104
JTAG_TMS AF19 S3X_JTAG_TMS BI 84 94 104
I2C_SCL E8 S3X_I2C_SCL OUT 85 88
I2C_SDA F8 S3X_I2C_SDA BI 85 88
PMIC_CTRL0 AF20 S3X_PMIC_CTRL0 88
PMIC_CTRL1 AE20 S3X_PMIC_CTRL1 88
PMIC_CTRL2 AG17 NC_S3X_PMIC_CTRL_2 102
PMIC_EXT_CLK_DIS AH20 S3X_PMIC_EXT_CLK_DIS 88
PMIC_LOW_PWR AD21 S3X_PMIC_LOW_PWR 88
RET_LPSR_CLEAR AE17 S3X_RET_LPSR_CLEAR 88
SPI_CLK F11 S3X_SPI_CLK
SPI_CS* G12 SSD_BOOT_LB_L 84 88 91
SPI_MISO E11 S3X_SPI_MISO
SPI_MOSI G10 S3X_SPI_MOSI
SPI_NOR_CLK E9 S3X_BOOTSTRAP0
SPI_NOR_CS* G11 NC_S3X_BOOTSTRAP1 102
SPI_NOR_SIO0 H10 ERN_L 81
SPI_NOR_SO1 C8 S3X_BOOTSTRAP3
SPI_NOR_SO2 F10 S3X_BOOTSTRAP4
SPI_NOR_SO3 G9 S3X_BOOTSTRAP5
SPI_NOR_RFN E10 NC_S3X_BOOTSTRAP6 102
UART0_RX B8 S3X_SMC_OOB_UART_R2D 88
UART0_TX A8 88 S3X_SMC_OOB_UART_D2R
UART1_RX B7 S3X_DEBUG_UART_R2D IN 88
UART1_TX A7 S3X_DEBUG_UART_D2R OUT 88
RETEN_EN H18 S3X_RET_EN_L IN 88
DDR_PHY_DATA_VREF AD12 S3X_DDR_PHY_DATA_VREF
DDR_PHY_ZQ G21 S3X_DDR_PHY_ZQ
DDR_VREFI_ALIVE B23 S3X_DDR_VREFI_ALIVE
DDR_VREFI_ZQ J20 S3X_DDR_VREFI_ZQ
DDR_VREF0 AH16 S3X_DDR_VREF0
DDR_ZQ B26 S3X_DDR_ZQ
DDR_CKE0 C20 S3X_DDR_CKE0
DDR_CKE1 C21 S3X_DDR_CKE1

NC_S3X_DT0 102 F18 DT00
NC_S3X_DT1 102 G18 DT01

PP1V8_SSD_COLD 19 81 82 84 85 86 87 88 104

C8657 0.01UF 10% 10V X7R-CERM 0201
C8658 0.01UF 10% 10V X7R-CERM 0201
C8659 0.01UF 10% 10V X7R-CERM 0201
C8660 0.01UF 10% 10V X7R-CERM 0201
C8650 0.01UF 10% 10V X7R-CERM 0201
C8652 0.01UF 10% 10V X7R-CERM 0201
C8654 0.01UF 10% 10V X7R-CERM 0201
C8656 0.01UF 10% 10V X7R-CERM 0201

ANI01_VREF 86
ANI23_VREF 86
ANI45_VREF 87
ANI67_VREF 87

PLACE_NEAR=U8600.AJ18:2.0MM
Y8600
1.6DX1.2DMM-SM
24MHZ-30PPM-60OHM
S3X_XTALI
S3X_XTALO
S3XCLK:INT
NC
R8600 1M 1% 1/20W MF 201
R8602 1K 1% 1/20W MF 201 S3XCLK:INT
PLACE_NEAR=U8600.AK18:2.0MM
PLACE_NEAR=Y8600.1:1.0MM
PLACE_NEAR=Y8600.3:1.0MM
C8600 9.5PF +/-0.1PF 50V C0G-C0G 0201
C8601 9.5PF +/-0.1PF 50V C0G-C0G 0201
OMIT_TABLE

AK18 XI0
AJ18 XO0
S3X_XTALO_R

PP1V8_SSD_COLD 104 88 87 86 85 84 82 81 19
R8615 10K 5% 1/20W MF 201

ANI47_ZQ
ANI03_ZQ
R8605 34.8 1% 1/20W MF 201
R8606 34.8 1% 1/20W MF 201
R8603 3.01K 1% 1/20W MF 201
S3X_PCIE_REF H17 REXT
S3X_GPIO0 AD11 GPIO0
NC_S3X_GPIO1 102 AD10 GPIO1
S3X_PFN IN 88 AE11 GPIO2
NC T26 ANI03_ZQ_PD
NC T25 ANI03_ZQ_PU
T5 ANI47_ZQ_PD
NC T6 ANI47_ZQ_PU

PP1V8_SSD_COLD 104 88 87 86 85 84 82 81 19
R8604 100K 0.1% 1/20W MF 0201-1
R8676 10K 5% 1/20W MF 201
R8677 10K 5% 1/20W MF 201
R8674 1K 5% 1/20W MF 201 S3XCLK:EXT
R8609 1K 5% 1/20W MF 201 S3XCLK:INT
R8698 33 5% 1/20W MF 201 S3XCLK:EXT
PLACE_NEAR=U1900.16:2.0MM
SYSCLK_CLK24M_SSD 18
R8699 0 5% 1/20W MF 201 S3XCLK:INT
R8624 10K 5% 1/20W MF 201
R8612 10K 5% 1/20W MF 201

PP1V8_SSD_COLD 104 88 87 86 85 84 82 81 19
NAND_CFG0 R8616 10K 5% 1/20W MF 201
NAND_CFG2 R8617 10K 5% 1/20W MF 201
NAND_CFG1 R8618 10K 5% 1/20W MF 201
R8660 10K 5% 1/20W MF 201
CAPACITY0 R8662 10K 5% 1/20W MF 201
CAPACITY1 R8663 10K 5% 1/20W MF 201
CAPACITY2 R8664 10K 5% 1/20W MF 201

R8629 10K 5% 1/20W MF 201

NOSTUFF R8610 1K 5% 1/20W MF 201
NOSTUFF R8611 1K 5% 1/20W MF 201
R8607 240 1% 1/20W MF 201
C8620 1000PF 10% 16V X7R-1 0201
C8621 1000PF 10% 16V X7R-1 0201
C8622 1000PF 10% 16V X7R-1 0201
C8623 1000PF 10% 16V X7R-1 0201
PLACE_NEAR=U8600.G21:3.0MM
R8608 240 1% 1/20W MF
PACK_TYPE=201
PLACE_NEAR=U8600.B26:3.0MM
BYPASS=U8600.AH16::3.0MM
BYPASS=U8600.J20::3.0MM
BYPASS=U8600.B23::3.0MM
BYPASS=U8600.AD12::3.0MM

GND_VOID=TRUE
C8610 0.22UF GND_VOID=TRUE
PCIE_SSD_D2R_LB_P<0> 91 OUT — PCIE_SSD_D2R_C_P<0> 81
C8611 0.22UF GND_VOID=TRUE
PCIE_SSD_D2R_LB_N<0> 91 OUT — PCIE_SSD_D2R_C_N<0> 81
C8613 0.22UF GND_VOID=TRUE
PCIE_SSD_D2R_P<1> 105 15 OUT — PCIE_SSD_D2R_C_P<1> 81
C8612 0.22UF GND_VOID=TRUE
PCIE_SSD_D2R_N<1> 105 15 OUT — PCIE_SSD_D2R_C_N<1> 81
C8614 0.22UF GND_VOID=TRUE
PCIE_SSD_D2R_P<2> 105 15 OUT — PCIE_SSD_D2R_C_P<2> 81
C8615 0.22UF GND_VOID=TRUE
PCIE_SSD_D2R_N<2> 105 15 OUT — PCIE_SSD_D2R_C_N<2> 81
C8617 0.22UF GND_VOID=TRUE
PCIE_SSD_D2R_P<3> 105 15 OUT — PCIE_SSD_D2R_C_P<3> 81
C8616 0.22UF GND_VOID=TRUE
PCIE_SSD_D2R_N<3> 105 15 OUT — PCIE_SSD_D2R_C_N<3> 81

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00077	1	CAP,9.5PF,50V,0201	C8601	CRITICAL	S3XCLK:INT
117S0002	1	RES,MF,0 OHM,1/20W,0201	C8601	CRITICAL	S3XCLK:EXT

BOM_COST_GROUP=SSD

Buffered SSD_RESET_L to Mitigate EPO Issue

PP1V8_SSD_COLD 104 88 87 86 85 84 82 81 19
C8602 0.1UF 10% 6.3V CERM-X5R 0201
U8601 74AUP1G08GF SOT891
VCC GND
91 88 84 IN SSD_RESET_LB_L
ERN_L 81
NC

SYNC_MASTER=J79_RUENJOU
PAGE TITLE
S3X CORE PCIE
Apple Inc.
DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 86 OF 145
SHEET 81 OF 119

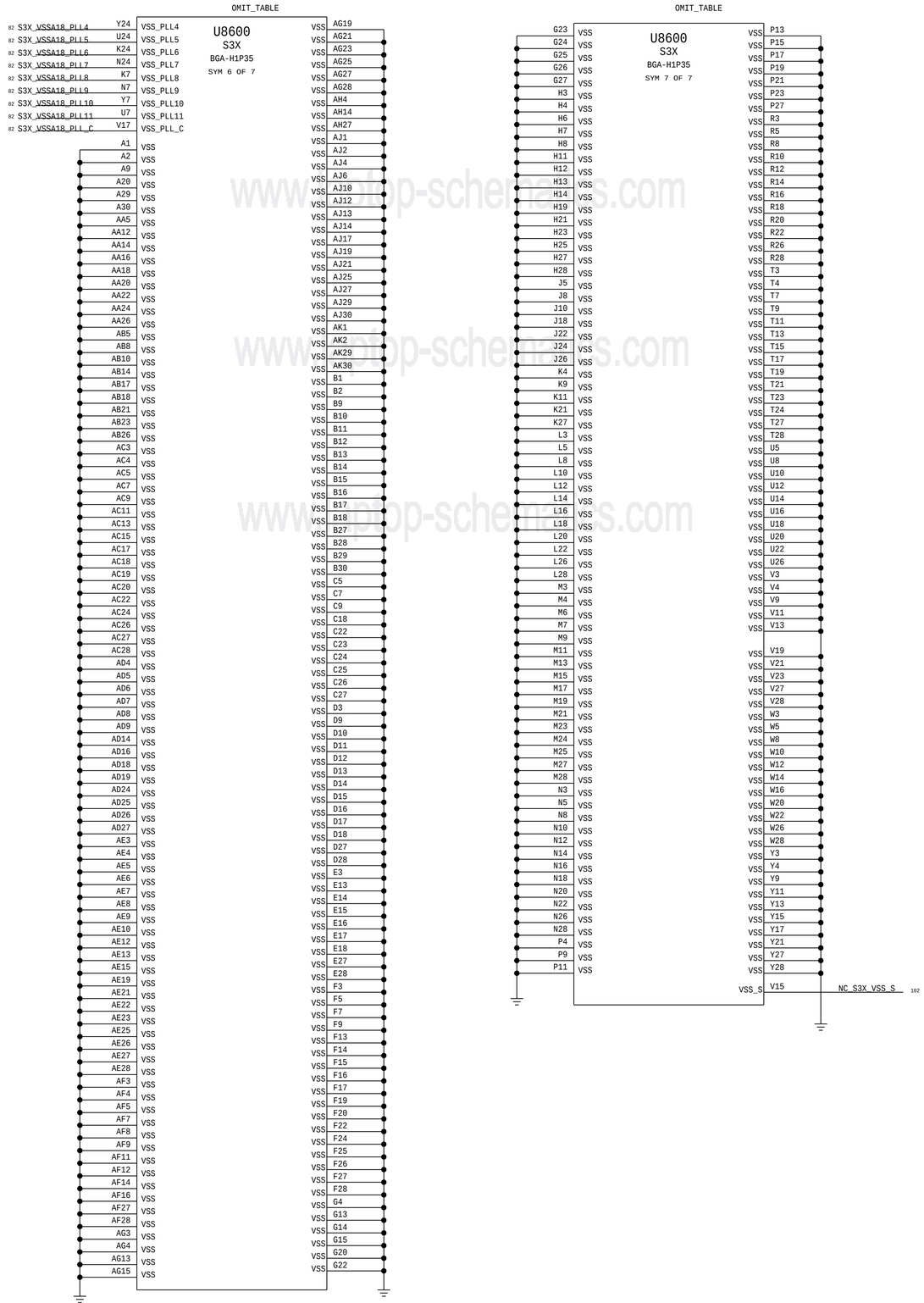
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	1	RES,MF,0 OHM,1/20W,0201	L8704	CRITICAL	

BOM_COST_GROUP=SSD

PAGE TITLE
S3X POWER

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 87 OF 145
SHEET 82 OF 119



BOM_COST_GROUP=SSD

SYNC_MASTER=J79_RIO
SYNC_DATE=06/18/2015

PAGE TITLE
PAGE_TITLE=S3X GND

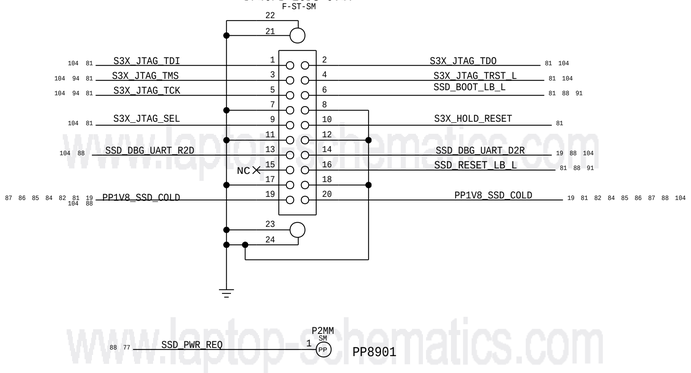
Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 88 OF 145
SHEET 83 OF 119

JTAG (DEBUG 1)

S3X_DBG

J8992
DF40PB-20DS-0.4V
F-ST-SM



P2MM
SM
PP

SSD_PWR_REQ — PP8901

PP3V3_S4 — R8901 100K 5% 1/20W MF 201 — STORAGE_EN

PP3V3_S5_SSD — R8902 100K 5% 1/20W MF 201 — PD_L

SSD_PWR_EN_LB_L — Q8901 DMN32D2LFB4 DFN1006H4-3 SYM_VER_1

R8903 100K 5% 1/20W MF 201

GND_VOID=TRUE

C8910	0.22UF	PCIE_SSD_R2D_LB_C_P<0>	PCIE_SSD_R2D_LB_P<0>	
C8911	0.22UF	PCIE_SSD_R2D_LB_C_N<0>	PCIE_SSD_R2D_LB_N<0>	
C8913	0.22UF	PCIE_SSD_R2D_C_P<1>	PCIE_SSD_R2D_P<1>	
C8912	0.22UF	PCIE_SSD_R2D_C_N<1>	PCIE_SSD_R2D_N<1>	
C8914	0.22UF	PCIE_SSD_R2D_C_P<2>	PCIE_SSD_R2D_P<2>	
C8915	0.22UF	PCIE_SSD_R2D_C_N<2>	PCIE_SSD_R2D_N<2>	
C8917	0.22UF	PCIE_SSD_R2D_C_P<3>	PCIE_SSD_R2D_P<3>	
C8916	0.22UF	PCIE_SSD_R2D_C_N<3>	PCIE_SSD_R2D_N<3>	

BOM_COST_GROUP=SSD

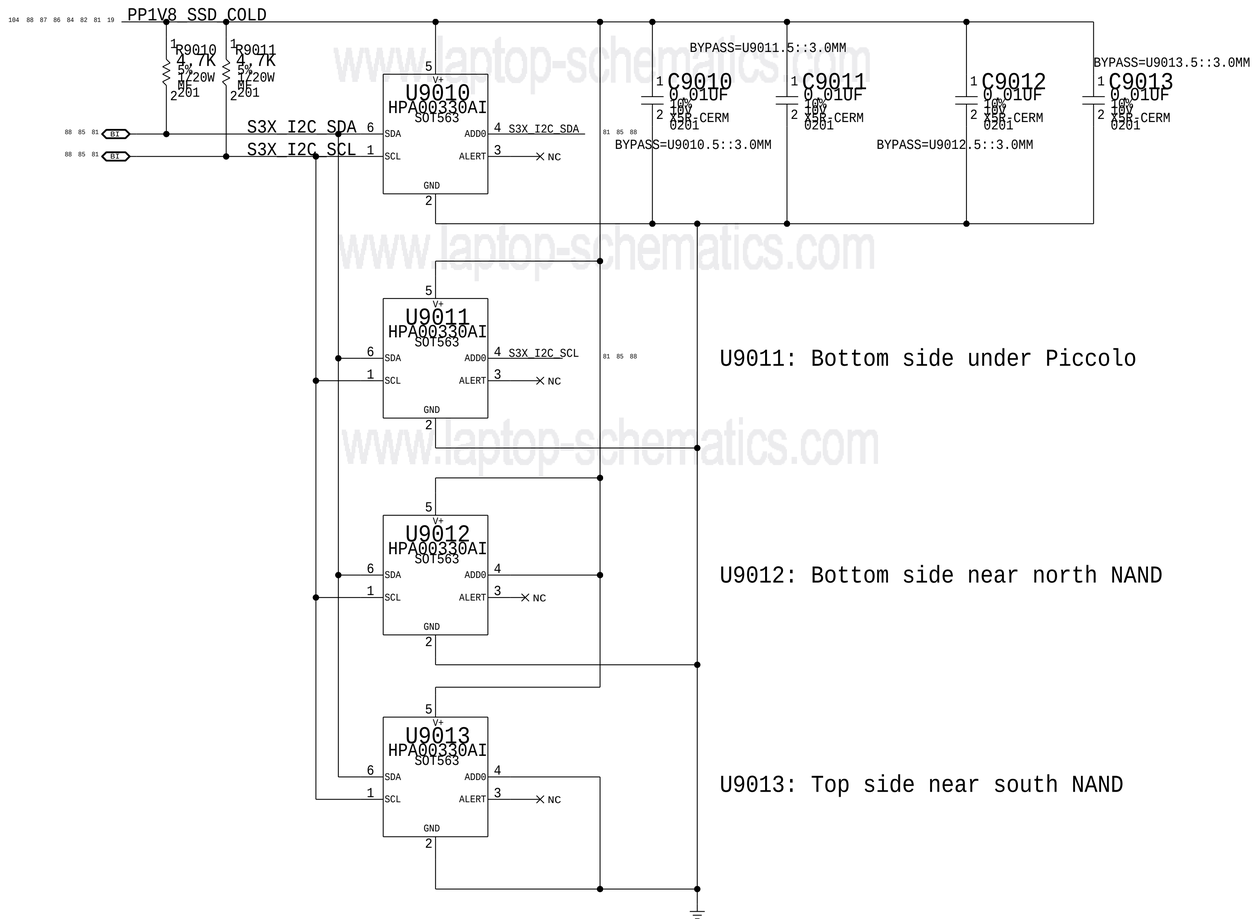
PAGE TITLE
Connector

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 89 OF 145
SHEET 84 OF 119

DEVICE 2-WIRE ADDRESS	ADD0 PIN CONNECTION
1001000	GND
1001001	V+
1001010	SDA
1001011	SCL

U9010: Top side under S3X



U9011: Bottom side under Piccolo

U9012: Bottom side near north NAND

U9013: Top side near south NAND

BOM_COST_GROUP=SSD

SYNC_MASTER=J79_BUCK2U2 SYNC_DATE=09/12/2015

PAGE TITLE
NAND VR, I2C ROM, TEMP SENSORS

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 90 OF 145
SHEET 85 OF 119

NAND INTERFACE 2/3 TOP

NAND INTERFACE 0/1 TOP

OMIT_TABLE

U8600
S3X
BGA-H1P35
SYM 1 OF 7

ANI0_IO<0>	AC29	ANI0_IO0	ANI1_IO0	T29	ANI1_IO<0>
ANI0_IO<1>	AD30	ANI0_IO1	ANI1_IO1	U30	ANI1_IO<1>
ANI0_IO<2>	AD29	ANI0_IO2	ANI1_IO2	U29	ANI1_IO<2>
ANI0_IO<3>	AD28	ANI0_IO3	ANI1_IO3	U28	ANI1_IO<3>
ANI0_IO<4>	AG30	ANI0_IO4	ANI1_IO4	Y30	ANI1_IO<4>
ANI0_IO<5>	AG29	ANI0_IO5	ANI1_IO5	Y29	ANI1_IO<5>
ANI0_IO<6>	AH30	ANI0_IO6	ANI1_IO6	AA30	ANI1_IO<6>
ANI0_IO<7>	AH29	ANI0_IO7	ANI1_IO7	AA29	ANI1_IO<7>
ANI0_NCE<0>	AG22	ANI0_NCE(0)	ANI1_NCE(0)	AJ24	ANI1_NCE<0>
ANI0_NCE<1>	AD23	ANI0_NCE(1)	ANI1_NCE(1)	AG26	ANI1_NCE<1>
ANI0_NCE<2>	AF21	ANI0_NCE(2)	ANI1_NCE(2)	AH26	ANI1_NCE<2>
ANI0_NCE<3>	AD22	ANI0_NCE(3)	ANI1_NCE(3)	AF24	ANI1_NCE<3>
NC_ANI0_NCE4	AF22	ANI0_NCE(4)	ANI1_NCE(4)	AF26	NC_ANI1_NCE4
NC_ANI0_NCE5	AF23	ANI0_NCE(5)	ANI1_NCE(5)	AK24	NC_ANI1_NCE5
NC_ANI0_NCE6	AJ20	ANI0_NCE(6)	ANI1_NCE(6)	AE24	NC_ANI1_NCE6
NC_ANI0_NCE7	AK20	ANI0_NCE(7)	ANI1_NCE(7)	AH24	NC_ANI1_NCE7
ANI0_ALE	AH23	ANI0_ALE	ANI1_ALE	AK26	ANI1_ALE
ANI0_CLE	AK22	ANI0_CLE	ANI1_CLE	AG24	ANI1_CLE
ANI0_NWE	AH28	ANI0_NWE	ANI1_NWE	AA28	ANI1_NWE
ANI0_RNB	AJ22	ANI0_RNB	ANI1_RNB	AJ26	NC_ANI1_RNB
NC	AH22	ANI0_PPM_IN	ANI1_PPM_IN	AE25	NC
NC	AH21	ANI0_PPM_OUT	ANI1_PPM_OUT	AH25	NC
ANI0_NRE_P	AF30	ANI0_NRE_P	ANI1_NRE_P	W30	ANI1_NRE_P
ANI0_NRE_N	AF29	ANI0_NRE_N	ANI1_NRE_N	W29	ANI1_NRE_N
ANI0_DQS_P	AE30	ANI0_DQS_P	ANI1_DQS_P	V30	ANI1_DQS_P
ANI0_DQS_N	AE29	ANI0_DQS_N	ANI1_DQS_N	V29	ANI1_DQS_N
ANI01_VREF	AC30	ANI0_VREF	ANI1_VREF	T30	ANI01_VREF
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ANI2_IO<3>	G30	ANI2_IO3	ANI3_IO3	P30	ANI3_IO<3>
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ANI2_IO<5>	D30	ANI2_IO5	ANI3_IO5	L30	ANI3_IO<5>
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ANI2_IO<7>	C30	ANI2_IO7	ANI3_IO7	K30	ANI3_IO<7>
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NC_ANI2_NCE5	D19	ANI2_NCE(5)	ANI3_NCE(5)	E24	NC_ANI3_NCE5
NC_ANI2_NCE6	D21	ANI2_NCE(6)	ANI3_NCE(6)	D26	NC_ANI3_NCE6
NC_ANI2_NCE7	E21	ANI2_NCE(7)	ANI3_NCE(7)	B25	NC_ANI3_NCE7
ANI2_ALE	E20	ANI2_ALE	ANI3_ALE	E25	ANI3_ALE
ANI2_CLE	A22	ANI2_CLE	ANI3_CLE	E26	ANI3_CLE
ANI2_NWE	C28	ANI2_NWE	ANI3_NWE	K28	ANI3_NWE
ANI2_RNB	D20	ANI2_RNB	ANI3_RNB	B24	NC_ANI3_RNB
NC	E19	ANI2_PPM_IN	ANI3_PPM_IN	F23	NC
NC	B20	ANI2_PPM_OUT	ANI3_PPM_OUT	E23	NC
ANI2_NRE_P	E29	ANI2_NRE_P	ANI3_NRE_P	M29	ANI3_NRE_P
ANI2_NRE_N	E30	ANI2_NRE_N	ANI3_NRE_N	M30	ANI3_NRE_N
ANI2_DQS_P	F29	ANI2_DQS_P	ANI3_DQS_P	N29	ANI3_DQS_P
ANI2_DQS_N	F30	ANI2_DQS_N	ANI3_DQS_N	N30	ANI3_DQS_N
ANI23_VREF	H30	ANI2_VREF	ANI3_VREF	R30	ANI23_VREF

OMIT_TABLE

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NAND-15NM-64GB-2.8V
1Z-64GB-2P-MLC-DDP

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ANI2_IO<5>	K6	IO5-0
ANI2_IO<6>	K2	IO6-0
ANI2_IO<7>	J3	IO7-0
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ANI3_IO<2>	B2	IO2-1
ANI3_IO<3>	B6	IO3-1
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NC_G1	G1	
NC_G0	G0	
NC_G5	G5	
ZQ	G3	
CE0*	N1	ANI2_NCE<0>
CLE0	L7	ANI2_CLE
ALE0	J7	ANI2_ALE
WE0*	N7	ANI2_NWE
RE0	J5	ANI2_NRE_N
RE0*	H4	ANI2_NRE_P
DQS0	M4	ANI2_DQS_P
DQS0*	L3	ANI2_DQS_N
R/B*	H6	ANI2_RNB
WP*	F6	NAND_WP_L
CE1*	N1	ANI3_NCE<0>
CLE1	L7	ANI3_CLE
ALE1	J7	ANI3_ALE
WE1*	N7	ANI3_NWE
RE1	J5	ANI3_NRE_N
RE1*	H4	ANI3_NRE_P
DQS1	M4	ANI3_DQS_P
DQS1*	L3	ANI3_DQS_N
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ANI0_IO<3>	M6	IO3-0
ANI0_IO<4>	L5	IO4-0
ANI0_IO<5>	K6	IO5-0
ANI0_IO<6>	K2	IO6-0
ANI0_IO<7>	J3	IO7-0
ANI1_IO<0>	A3	IO0-1
ANI1_IO<1>	A5	IO1-1
ANI1_IO<2>	B2	IO2-1
ANI1_IO<3>	B6	IO3-1
ANI1_IO<4>	C5	IO4-1
ANI1_IO<5>	D6	IO5-1
ANI1_IO<6>	D2	IO6-1
ANI1_IO<7>	E3	IO7-1
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NC_G1	G1	
NC_G0	G0	
NC_G5	G5	
ZQ	G3	
CE0*	N1	ANI0_NCE<0>
CLE0	L7	ANI0_CLE
ALE0	J7	ANI0_ALE
WE0*	N7	ANI0_NWE
RE0	J5	ANI0_NRE_N
RE0*	H4	ANI0_NRE_P
DQS0	M4	ANI0_DQS_P
DQS0*	L3	ANI0_DQS_N
R/B*	H6	ANI0_RNB
WP*	F6	NAND_WP_L
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CLE1	C7	ANI1_CLE
ALE1	E7	ANI1_ALE
WE1*	A7	ANI1_NWE
RE1	E5	ANI1_NRE_N
RE1*	F4	ANI1_NRE_P
DQS1	B4	ANI1_DQS_P
DQS1*	C3	ANI1_DQS_N
VREF	G8	ANI01_VREF
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BOM_COST_GROUP=SSD

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DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	91 OF 145
SHEET	86 OF 119

OMIT_TABLE

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BGA-H1P35
SYM 2 OF 7

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87 BI	ANI4_IO<3>	G1	ANI4_IO3	P1	ANI5_IO3
87 BI	ANI4_IO<4>	D2	ANI4_IO4	L2	ANI5_IO4
87 BI	ANI4_IO<5>	D1	ANI4_IO5	L1	ANI5_IO5
87 BI	ANI4_IO<6>	C2	ANI4_IO6	K2	ANI5_IO6
87 BI	ANI4_IO<7>	C1	ANI4_IO7	K1	ANI5_IO7
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87 OUT	ANI4_NCE<1>	E7	ANI4_NCE(1)	D4	ANI5_NCE<1>
87 OUT	ANI4_NCE<2>	E6	ANI4_NCE(2)	E4	ANI5_NCE<2>
87 OUT	ANI4_NCE<3>	G7	ANI4_NCE(3)	B4	ANI5_NCE<3>
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102 OUT	NC_ANI4_NCE5	A6	ANI4_NCE(5)	D5	NC_ANI5_NCE5
102 OUT	NC_ANI4_NCE6	H9	ANI4_NCE(6)	B5	NC_ANI5_NCE6
102 OUT	NC_ANI4_NCE7	G8	ANI4_NCE(7)	A5	NC_ANI5_NCE7
87	ANI4_ALE	D7	ANI4_ALE	F4	ANI5_ALE
87	ANI4_CLE	F6	ANI4_CLE	A3	ANI5_CLE
87	ANI4_NWE	C3	ANI4_NWE	K3	ANI5_NWE
87	ANI4_RNB	D6	ANI4_RNB	C4	NC_ANI5_RNB 102 BI
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NC		C6	ANI4_PPM_OUT	E5	NC ANI5_PPM_OUT
87	ANI4_NRE_P	E2	ANI4_NRE_P	M2	ANI5_NRE_P 87
87	ANI4_NRE_N	E1	ANI4_NRE_N	M1	ANI5_NRE_N 87
87	ANI4_DQS_P	F2	ANI4_DQS_P	N2	ANI5_DQS_P 87
87	ANI4_DQS_N	F1	ANI4_DQS_N	N1	ANI5_DQS_N 87
87 81 OUT	ANI45_VREF	H1	ANI4_VREF	R1	ANI45_VREF OUT 81 87
87 BI	ANI6_IO<0>	AC2	ANI6_IO0	T2	ANI7_IO<0>
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87 BI	ANI6_IO<7>	AH2	ANI6_IO7	AA2	ANI7_IO<7>
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87 OUT	ANI6_NCE<3>	AH9	ANI6_NCE(3)	AJ5	ANI7_NCE<3>
102 OUT	NC_ANI6_NCE4	AH12	ANI6_NCE(4)	AH5	NC_ANI7_NCE4
102 OUT	NC_ANI6_NCE5	AH11	ANI6_NCE(5)	AH7	NC_ANI7_NCE5
102 OUT	NC_ANI6_NCE6	AG9	ANI6_NCE(6)	AG7	NC_ANI7_NCE6
102 OUT	NC_ANI6_NCE7	AG11	ANI6_NCE(7)	AG5	NC_ANI7_NCE7
87	ANI6_ALE	AJ9	ANI6_ALE	AG6	ANI7_ALE
87	ANI6_CLE	AK9	ANI6_CLE	AH6	ANI7_CLE
87	ANI6_NWE	AH3	ANI6_NWE	AA3	ANI7_NWE
87	ANI6_RNB	AG12	ANI6_RNB	AF6	NC_ANI7_RNB 102 BI
NC		AG10	ANI6_PPM_IN	AG8	NC ANI7_PPM_IN
NC		AF10	ANI6_PPM_OUT	AH8	NC ANI7_PPM_OUT
87	ANI6_NRE_P	AF1	ANI6_NRE_P	W1	ANI7_NRE_P 87
87	ANI6_NRE_N	AF2	ANI6_NRE_N	W2	ANI7_NRE_N 87
87	ANI6_DQS_P	AE1	ANI6_DQS_P	V1	ANI7_DQS_P 87
87	ANI6_DQS_N	AE2	ANI6_DQS_N	V2	ANI7_DQS_N 87
87 81 OUT	ANI67_VREF	AC1	ANI6_VREF	T1	ANI67_VREF OUT 81 87

NAND INTERFACE 6/7

PP3V3_2V7_NAND_VCC

C9227 12PF 5% 25V NP0-C0G 0201
C9228 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9212 0.1UF 10% 6.3V CERM-XSR 0201
C9211 0.22UF 20% 6.3V X6S-CERM 0201
C9215 1.0UF 20% 6.3V XSR 0201-1
C9216 1.0UF 20% 6.3V XSR 0201-1

PP1V8_SSD_COLD

C9217 1.0UF 20% 6.3V XSR 0201-1
C9218 0.22UF 20% 6.3V X6S-CERM 0201
C9219 0.1UF 10% 6.3V CERM-XSR 0201
C9220 0.1UF 10% 6.3V CERM-XSR 0201
C9221 0.1UF 10% 6.3V CERM-XSR 0201

OA8 OC8 OD8 OF8 — VCC
OB8 OC8 OD8 OE8 — VCCQ

OMIT_TABLE

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NAND-15NM-64GB-2.8V
1Z-64GB-2P-MLC-DDP

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87 BI	ANI7_IO<2>	B2	IO2-1
87 BI	ANI7_IO<3>	B6	IO3-1
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87 BI	ANI7_IO<7>	E3	IO7-1
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NC		G0	NC_G0
NC		G5	NC_G5
		G3	ZQ

CE0*	N1	ANI6_NCE<0>	IN 87
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ALE0	J7	ANI6_ALE	87
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DQS0	M4	ANI6_DQS_P	87
DQS0*	L3	ANI6_DQS_N	87
R/B*	H6	ANI6_RNB	87
WP*	F6	NAND_WP_L	86 87 88
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VREF	G8	ANI67_VREF	IN 81 87
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CE7*	F2	ANI7_NCE<3>	IN 87

PP1V8_SSD_COLD
R9201 10K 5% 1/20W MF 201

NAND_ZQ_U9220
R9292 300 1% 1/20W MF 201

PP1V8_SSD_COLD
R9200 10K 5% 1/20W MF 201

D4 K4 OA8 OB8 OE8 OF8 — GND

NAND INTERFACE 4/5

PP3V3_2V7_NAND_VCC

C9200 0.1UF 10% 6.3V CERM-XSR 0201
C9201 0.22UF 20% 6.3V X6S-CERM 0201
C9202 1.0UF 20% 6.3V XSR 0201-1
C9203 1.0UF 20% 6.3V XSR 0201-1

PP1V8_SSD_COLD

C9204 1.0UF 20% 6.3V XSR 0201-1
C9205 0.22UF 20% 6.3V X6S-CERM 0201
C9206 0.1UF 10% 6.3V CERM-XSR 0201
C9213 0.1UF 10% 6.3V CERM-XSR 0201
C9214 0.1UF 10% 6.3V CERM-XSR 0201

OA8 OC8 OD8 OF8 — VCC
OB8 OC8 OD8 OE8 — VCCQ

OMIT_TABLE

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NAND-15NM-64GB-2.8V
1Z-64GB-2P-MLC-DDP

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87 BI	ANI5_IO<7>	E3	IO7-1
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NC		G1	NC_G1
NC		G0	NC_G0
NC		G5	NC_G5
		G3	ZQ

CE0*	N1	ANI4_NCE<0>	IN 87
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ALE0	J7	ANI4_ALE	87
WE0*	N7	ANI4_NWE	87
RE0	J5	ANI4_NRE_N	87
RE0*	H4	ANI4_NRE_P	87
DQS0	M4	ANI4_DQS_P	87
DQS0*	L3	ANI4_DQS_N	87
R/B*	H6	87 ANI4_RNB	
WP*	F6	NAND_WP_L	86 87 88
CE1*	A1	ANI5_NCE<0>	IN 87
CLE1	C7	ANI5_CLE	87
ALE1	E7	ANI5_ALE	87
WE1*	A7	ANI5_NWE	87
RE1	E5	ANI5_NRE_N	87
RE1*	F4	ANI5_NRE_P	87
DQS1	B4	ANI5_DQS_P	87
DQS1*	C3	ANI5_DQS_N	87
VREF	G8	ANI45_VREF	IN 81 87
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CE3*	C1	ANI5_NCE<1>	IN 87
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CE5*	E1	ANI5_NCE<2>	IN 87
CE6*	H2	ANI4_NCE<3>	IN 87
CE7*	F2	ANI5_NCE<3>	IN 87

R9290 300 1% 1/20W MF 201

D4 K4 OA8 OB8 OE8 OF8 — GND

BOM_COST_GROUP=SSD

PAGE TITLE: ANI[7:4]

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 92 OF 145
SHEET: 87 OF 119

PICCOLO I2C INTERFACE ADDRESSES
WRITE:78H
READ:79H

NEED PID GPIO OPTION TABLE

BOM_COST_GROUP=SSD

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Apple Inc.	
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	93 OF 145
SHEET	88 OF 119

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FREQ = 500 KHZ
MAX OCP = 8.51A
Nom OCP = 7.06A
MIN OCP = 5.16A

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XW9431 SM
P2V7NAND_RFB_N
P2V7NAND_RFB_P
R9403 10K 0.1% 1/20W MF 0201-1 NO_XNET_CONNECTION=1
R9431 10K 0.1% 1/20W MF 0201-1 NO_XNET_CONNECTION=1
Change R3505 and R3531 to 0.1% when available

PP5V_S4_P2V7NAND_LB
R9401 10 5% 1/20W MF 201
R9406 2.2 5% 1/10W MF 402
PP2V7_NAND_PVCC MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=2.7V
C9421 2.2UF 20% 10V CER-X6S 0402
PP2V7_NAND_VCC MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=2.7V
C9422 1UF 10% 10V CER-CERM 0402

PPVIN_2V7NAND_LB
P2V7NAND_BOOT_RC MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 DIDT=TRUE
C9416 0.1UF 10% 10V X7R-CERM 0402
R9409 2.2 5% 1/20W MF 201
C9403 33UF 20% 16V TANT-POLY CASE-B3
C9402 33UF 20% 16V TANT-POLY CASE-B3
C9400 2.2UF 20% 25V CER-X6S 0402
C9401 2.2UF 20% 25V CER-X6S 0402
C9404 1000PF 10% 16V X7R 0201

PICCOLO_VEN1 (EN, 88)
R9420 0 5% 1/20W MF 201

U9400 ISL95870AH UTQFN CRITICAL
VCC PVCC BOOT UGATE PHASE LGATE
EN FB SREF VO OCSET PGOOD RTN FSEL SET0 SET1 VID0 VID1 TGR BG VSW PGND GND PGND

P2V7NAND_EN
P2V7NAND_SENSE_DIV
P2V7NAND_SREF
P2V7NAND_VO
P2V7NAND_OCSET
P2V7NAND_PGOOD_R (89)
P2V7NAND_RTN_DIV
P2V7NAND_FSEL
P2V7NAND_SET0
P2V7NAND_SET1

P2V7NAND_VBST MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 DIDT=TRUE
P2V7NAND_DRVH_R MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 GATE_NODE=TRUE DIDT=TRUE
P2V7NAND_LL MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 SWITCH_NODE=TRUE DIDT=TRUE
P2V7NAND_DRVL_R MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 GATE_NODE=TRUE DIDT=TRUE

Q9401 CSD58873Q3D Q3D
R9414 0 5% 1/20W MF 201
P2V7NAND_DRVH MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 GATE_NODE=TRUE DIDT=TRUE
R9415 0 5% 1/20W MF 201
P2V7NAND_DRVL MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 GATE_NODE=TRUE DIDT=TRUE

L9400 2.2UH-20%-12A-0.02450HM PIMB062D-SM 152500270
P2V7NAND_SW MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 SWITCH_NODE=TRUE DIDT=TRUE
P2V7NAND_R MIN_LINE_WIDTH=0.1160 MIN_NECK_WIDTH=0.0600
NO_XNET_CONNECTION=1
R9430 0.003 1% 1/2W MF 0306
PP3V3_2V7_NAND_VCC (101)

NOSTUFF R9435 2.2 5% 1/10W MF-LF 603
P2V7NAND_SNUB DIDT=TRUE SWITCH_NODE=TRUE
NOSTUFF C9435 0.001UF 10% 50V CERM 402

NOSTUFF R9410 200 5% 1/10W MF-LF 402
C9405 2.2UF 20% 10V CER-X6S 0402
C9406 2.2UF 20% 10V CER-X6S 0402
C9410 1000PF 10% 25V X7R 0201
NOSTUFF C9409 150UF 20% 6.3V POLY-TANT CASE-BL-SM
C9408 150UF 20% 6.3V TANT-POLY CASE-BIS-1
C9407 150UF 20% 6.3V TANT-POLY CASE-BIS-1

ISNS_SSDNAND_P (97)
ISNS_SSDNAND_N (97)
R9421 2.49K 1/20W 1% 201 MF
C9470 0.01UF 10% 10V X7R-CERM 0201
R9472 2.49K 1/20W 1% 201 MF
NO_XNET_CONNECTION=1

R9417 191K 0.1% 1/20W MF 0201
C9417 22PF 5% 50V C0G 0201
C9423 0.01UF 10% 10V X7R-CERM 0201
R9418 95.3K 0.1% 1/20W MF 0201
P2V7NAND_SET_R
R9400 16.9K 1% 1/20W MF 201
R9413 100K 1% 1/20W MF 201

C9426 10PF 5% 50V C0G 0201
R9404 10K 0.1% 1/20W MF 0201-1
R9402 10K 0.1% 1/20W MF 0201-1
C9415 10PF 5% 50V C0G 0201

XW9400 SM
P2V7NAND_AGND MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000
PLACE_NEAR=U9400.3:1MM

CRITICAL C9430 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITICAL C9431 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE
CRITICAL C9432 12PF 5% 25V NP0-C0G 0201 — 2.4G DESENSE
CRITICAL C9433 3.0PF +/-0.1PF 25V NP0-C0G 0201 — 5G DESENSE

R9411 0 5% 1/20W MF 201
P2V7NAND_PGOOD (88) — P2V7NAND_PGOOD_R (89)

BOM_COST_GROUP=SSD

PAGE TITLE: SSD NAND VR

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 94 OF 145
SHEET: 89 OF 119

8	7	6	5	4	3	2	1

D

C

B

A

SYNC_MASTER=J14 SYNC_DATE=10/23/2012

PAGE TITLE

Empty

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DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 95 OF 145

SHEET 90 OF 119

8 7 6 5 4 3 2 1

LIFEBOAT

J9600
20759-042E-02
F-ST-SM

PCH Side

PPBUS_G3H 100 — 43 PWR

PP5V_S4 101 — 1 SIGNAL
SSD_BOOT_L 104 14 — 3
SSD_PWR_EN_L 104 13 — 5
STORAGE_EN 104 84 — 7
9
SSD_RESET_L 104 19 16 — 11
SSD_CLKREQ_L 102 — 13
15
PCIE_SSD_D2R_P<0> 105 15 — GND_VOID=TRUE 17
PCIE_SSD_D2R_N<0> 105 15 — GND_VOID=TRUE 19
21
PCIE_SSD_R2D_C_P<0> 105 15 — GND_VOID=TRUE 23
PCIE_SSD_R2D_C_N<0> 105 15 — GND_VOID=TRUE 25
27
PCIE_CLK100M_SSD_P 15 — GND_VOID=TRUE 29
PCIE_CLK100M_SSD_N 15 — GND_VOID=TRUE 31
33
SSD_SR_EN_L 104 102 — 35
37
39
41

PP3V3_S5 101 — 45 PWR

GND 47
49
51
53
55
57
59
61
63
65
67

SSD Side

44 PWR — PPVIN_2V7NAND_LB 88 89
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V

2 SIGNAL — PP5V_S4_P2V7NAND_LB 89
4 — SSD_BOOT_LB_L 81 84 88
6 — SSD_PWR_EN_LB_L 84
8 — STORAGE_LB_EN 88
10
12 — SSD_RESET_LB_L 81 84 88
14 — SSD_PCIE_CLKREQ_LB_L 88
16
GND_VOID=TRUE 18 — PCIE_SSD_D2R_LB_P<0> 81
GND_VOID=TRUE 20 — PCIE_SSD_D2R_LB_N<0> 81
22
GND_VOID=TRUE 24 — PCIE_SSD_R2D_LB_C_P<0> 84
GND_VOID=TRUE 26 — PCIE_SSD_R2D_LB_C_N<0> 84
28
GND_VOID=TRUE 30 — PCIE_CLK100M_SSD_LB_P 81 105
GND_VOID=TRUE 32 — PCIE_CLK100M_SSD_LB_N 81 105
34
36 — LPSR_EN_LB_L 88
38
40
42

46 PWR — PP3V3_S5_SSD_LB 101

48 GND
50
52
54
56
58
60
62
64
66
68

SIGNAL_MODEL=LIFEBOAT

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V

BOM_COST_GROUP=SSD

SYNC_MASTER=J79_RUENJOU SYNC_DATE=09/09/2015

PAGE TITLE: LIFEBOAT

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 96 OF 145
SHEET: 91 OF 119

SNK0 AC Coupling

DP_T_SNK0_ML_C_P<0>	CB020	0.1UF	DP_T_SNK0_ML_P<0>	GND_VOID=TRUE
DP_T_SNK0_ML_C_N<0>	CB021	0.1UF	DP_T_SNK0_ML_N<0>	GND_VOID=TRUE
DP_T_SNK0_ML_C_P<1>	CB022	0.1UF	DP_T_SNK0_ML_P<1>	GND_VOID=TRUE
DP_T_SNK0_ML_C_N<1>	CB023	0.1UF	DP_T_SNK0_ML_N<1>	GND_VOID=TRUE
DP_T_SNK0_ML_C_P<2>	CB024	0.1UF	DP_T_SNK0_ML_P<2>	GND_VOID=TRUE
DP_T_SNK0_ML_C_N<2>	CB025	0.1UF	DP_T_SNK0_ML_N<2>	GND_VOID=TRUE
DP_T_SNK0_ML_C_P<3>	CB026	0.1UF	DP_T_SNK0_ML_P<3>	GND_VOID=TRUE
DP_T_SNK0_ML_C_N<3>	CB027	0.1UF	DP_T_SNK0_ML_N<3>	GND_VOID=TRUE
DP_T_SNK0_AUXCH_C_P	CB028	0.1UF	DP_T_SNK0_AUXCH_P	GND_VOID=TRUE
DP_T_SNK0_AUXCH_C_N	CB029	0.1UF	DP_T_SNK0_AUXCH_N	GND_VOID=TRUE

SNK1 AC Coupling

DP_T_SNK1_ML_C_P<0>	CB030	0.1UF	DP_T_SNK1_ML_P<0>	GND_VOID=TRUE
DP_T_SNK1_ML_C_N<0>	CB031	0.1UF	DP_T_SNK1_ML_N<0>	GND_VOID=TRUE
DP_T_SNK1_ML_C_P<1>	CB032	0.1UF	DP_T_SNK1_ML_P<1>	GND_VOID=TRUE
DP_T_SNK1_ML_C_N<1>	CB033	0.1UF	DP_T_SNK1_ML_N<1>	GND_VOID=TRUE
DP_T_SNK1_ML_C_P<2>	CB034	0.1UF	DP_T_SNK1_ML_P<2>	GND_VOID=TRUE
DP_T_SNK1_ML_C_N<2>	CB035	0.1UF	DP_T_SNK1_ML_N<2>	GND_VOID=TRUE
DP_T_SNK1_ML_C_P<3>	CB036	0.1UF	DP_T_SNK1_ML_P<3>	GND_VOID=TRUE
DP_T_SNK1_ML_C_N<3>	CB037	0.1UF	DP_T_SNK1_ML_N<3>	GND_VOID=TRUE
DP_T_SNK1_AUXCH_C_P	CB038	0.1UF	DP_T_SNK1_AUXCH_P	GND_VOID=TRUE
DP_T_SNK1_AUXCH_C_N	CB039	0.1UF	DP_T_SNK1_AUXCH_N	GND_VOID=TRUE

RB062	100K	DP_TA_HPD
RB072	100K	DP_TB_HPD
RB060	1M	TBT_TA_LSTX
RB061	1M	TBT_TA_LSRX
RB070	1M	TBT_TB_LSTX
RB071	1M	TBT_TB_LSRX

BOM_COST_GROUP=TBT

RB090	3.3K	PP3V3_UPC_TA_LDO
RB091	3.3K	
RB093	3.3K	
RB092	3.3K	
CB090	1UF	

UB090 8MBIT-3.0V W25Q80DVUXIE USON OMIT_TABLE CRITICAL

TBT_T_SPI_CLK	CLK
TBT_T_SPI_CS_L	CS*
TBT_T_ROM_WP_L	WP*(IO2)
TBT_T_ROM_HOLD_L	HOLD*(IO3)
TBT_T_SPI_MOSI	DI(IO0)
TBT_T_SPI_MISO	DO(IO1)
GND EPAD	

UB000 TBT-AR-4C-CNTRL SYM 1 OF 2 FCBGA OMIT_TABLE CRITICAL

PCIE_TBT_T_R2D_P<0>	Y23	PCIE_RX0_P
PCIE_TBT_T_R2D_N<0>	Y22	PCIE_RX0_N
PCIE_TBT_T_R2D_P<1>	T23	PCIE_RX1_P
PCIE_TBT_T_R2D_N<1>	T22	PCIE_RX1_N
NC_PCIE_TBT_T_R2D_P<2>	M23	PCIE_RX2_P
NC_PCIE_TBT_T_R2D_N<2>	M22	PCIE_RX2_N
NC_PCIE_TBT_T_R2D_P<3>	H23	PCIE_RX3_P
NC_PCIE_TBT_T_R2D_N<3>	H22	PCIE_RX3_N
PCIE_CLK100M_TBT_T_P	V19	PCIE_REFCLK_100_IN_P
PCIE_CLK100M_TBT_T_N	T19	PCIE_REFCLK_100_IN_N
TBT_T_CLKREQ_L	AC5	PCIE_CLKREQ*
PCIE_TX0_P	V23	PCIE_TBT_T_D2R_C_P<0>
PCIE_TX0_N	V22	PCIE_TBT_T_D2R_C_N<0>
PCIE_TX1_P	P23	PCIE_TBT_T_D2R_C_P<1>
PCIE_TX1_N	P22	PCIE_TBT_T_D2R_C_N<1>
PCIE_TX2_P	K23	NC_PCIE_TBT_T_D2R_C_P<2>
PCIE_TX2_N	K22	NC_PCIE_TBT_T_D2R_C_N<2>
PCIE_TX3_P	F23	NC_PCIE_TBT_T_D2R_C_P<3>
PCIE_TX3_N	F22	NC_PCIE_TBT_T_D2R_C_N<3>
PERST*	L4	TBT_T_PCI_RESET_L
PCIE_RBIAS	N16	TBT_T_PCIE_BIAS

PCIE GEN3

DP_T_SNK0_ML_P<0>	AB7	DPSNK0_ML0_P
DP_T_SNK0_ML_N<0>	AC7	DPSNK0_ML0_N
DP_T_SNK0_ML_P<1>	AB9	DPSNK0_ML1_P
DP_T_SNK0_ML_N<1>	AC9	DPSNK0_ML1_N
DP_T_SNK0_ML_P<2>	AB11	DPSNK0_ML2_P
DP_T_SNK0_ML_N<2>	AC11	DPSNK0_ML2_N
DP_T_SNK0_ML_P<3>	AB13	DPSNK0_ML3_P
DP_T_SNK0_ML_N<3>	AC13	DPSNK0_ML3_N
DP_T_SNK0_AUXCH_P	Y11	DPSNK0_AUX_P
DP_T_SNK0_AUXCH_N	W11	DPSNK0_AUX_N
DP_T_SNK0_HPD	AA2	DPSNK0_HPD
DP_T_SNK0_DDC_CLK	Y5	DPSNK0_DDC_CLK
DP_T_SNK0_DDC_DATA	R4	DPSNK0_DDC_DATA

SINK PORT 0

DP_T_SNK1_ML_P<0>	AB15	DPSNK1_ML0_P
DP_T_SNK1_ML_N<0>	AC15	DPSNK1_ML0_N
DP_T_SNK1_ML_P<1>	AB17	DPSNK1_ML1_P
DP_T_SNK1_ML_N<1>	AC17	DPSNK1_ML1_N
DP_T_SNK1_ML_P<2>	AB19	DPSNK1_ML2_P
DP_T_SNK1_ML_N<2>	AC19	DPSNK1_ML2_N
DP_T_SNK1_ML_P<3>	AB21	DPSNK1_ML3_P
DP_T_SNK1_ML_N<3>	AC21	DPSNK1_ML3_N
DP_T_SNK1_AUXCH_P	Y12	DPSNK1_AUX_P
DP_T_SNK1_AUXCH_N	W12	DPSNK1_AUX_N
DP_T_SNK1_HPD	Y6	DPSNK1_HPD
DP_T_SNK1_DDC_CLK	Y8	DPSNK1_DDC_CLK
DP_T_SNK1_DDC_DATA	N4	DPSNK1_DDC_DATA
DP_T_SNK_RBIAS	Y18	DPSNK_RBIAS

SINK PORT 1

JTAG_TBT_TDI	Y4	TDI
JTAG_TBT_T_TMS	V4	TMS
JTAG_TBT_TCK	T4	TCK
JTAG_ISP_TDO	W4	TDO
TBT_T_RBIAS	H6	RBIAS
TBT_T_RSENSE	J6	RSENSE

USBC_TA_D2R_P<2>	A15	PA_RX1_P
USBC_TA_D2R_N<2>	B15	PA_RX1_N
USBC_TA_R2D_C_P<2>	A17	PA_TX1_P
USBC_TA_R2D_C_N<2>	B17	PA_TX1_N
USBC_TA_R2D_C_P<1>	A19	PA_TX0_P
USBC_TA_R2D_C_N<1>	B19	PA_TX0_N
USBC_TA_D2R_P<1>	B21	PA_RX0_P
USBC_TA_D2R_N<1>	A21	PA_RX0_N
DP_TA_AUXCH_C_P	Y15	PA_DPSRC_AUX_P
DP_TA_AUXCH_C_N	W15	PA_DPSRC_AUX_N
USB_UPC_TA_P	E20	PA_USB2_D_P
USB_UPC_TA_N	D20	PA_USB2_D_N
TBT_TA_LSTX	A5	PA_LSTX
TBT_TA_LSRX	A4	PA_LSRX
DP_TA_HPD	M4	PA_DPSRC_HPD
TBT_TA_USB2_RBIAS	H19	PA_USB2_RBIAS

PORT A

USBC_TB_D2R_P<2>	B7	PB_RX1_P
USBC_TB_D2R_N<2>	A7	PB_RX1_N
USBC_TB_R2D_C_P<2>	A9	PB_TX1_P
USBC_TB_R2D_C_N<2>	B9	PB_TX1_N
USBC_TB_R2D_C_P<1>	A11	PB_TX0_P
USBC_TB_R2D_C_N<1>	B11	PB_TX0_N
USBC_TB_D2R_P<1>	A13	PB_RX0_P
USBC_TB_D2R_N<1>	B13	PB_RX0_N
DP_TB_AUXCH_C_P	Y16	PB_DPSRC_AUX_P
DP_TB_AUXCH_C_N	W16	PB_DPSRC_AUX_N
USB_UPC_TB_P	E19	PB_USB2_D_P
USB_UPC_TB_N	D19	PB_USB2_D_N
TBT_TB_LSTX	B4	PB_LSTX
TBT_TB_LSRX	B5	PB_LSRX
DP_TB_HPD	G2	PB_DPSRC_HPD
TBT_TB_USB2_RBIAS	F19	PB_USB2_RBIAS

PORT B

TBT PORTS

DP_T_SRC_ML_P<0>	R2	DPSRC_ML0_P
DP_T_SRC_ML_N<0>	R1	DPSRC_ML0_N
DP_T_SRC_ML_P<1>	N2	DPSRC_ML1_P
DP_T_SRC_ML_N<1>	N1	DPSRC_ML1_N
DP_T_SRC_ML_P<2>	L2	DPSRC_ML2_P
DP_T_SRC_ML_N<2>	L1	DPSRC_ML2_N
DP_T_SRC_ML_P<3>	J2	DPSRC_ML3_P
DP_T_SRC_ML_N<3>	J1	DPSRC_ML3_N
DP_T_SRC_AUX_P	W19	DPSRC_AUX_P
DP_T_SRC_AUX_N	Y19	DPSRC_AUX_N
DP_T_SRC_HPD	G1	DPSRC_HPD
DP_T_SRC_RBIAS	N6	DPSRC_RBIAS

SOURCE PORT 0

I2C_TBT_T_SDA	U1	GPIO_0
I2C_TBT_T_SCL	U2	GPIO_1
TBT_T_ROM_WP_L	V1	GPIO_2
TBT_T_TMU_CLK_OUT	V2	GPIO_3
SMC_PME_S4_DARK_L	W1	GPIO_4
TBT_T_CIO_PLUG_EVENT_L	W2	GPIO_5
DDI2_MUX_SEL	Y1	GPIO_6
DDI1_MUX_SEL	Y2	GPIO_7
TBT_T_TMU_CLK_IN	AA1	GPIO_8
I2C_TBT_TA_INT_L	J4	POC_GPIO_0
I2C_TBT_TB_INT_L	E2	POC_GPIO_1
TBT_T_USB_PWR_EN	D4	POC_GPIO_2
TBT_T_FORCE_PWR	H4	POC_GPIO_3
PM_BATLOW_L	F2	POC_GPIO_4
PM_SLP_S3_L	D2	POC_GPIO_5
TBT_T_CIO_PWR_EN	F1	POC_GPIO_6

LC GPIO

POC GPIO

TEST_EN	E1	TBT_T_TEST_EN
TEST_PWR_GOOD	AB5	TBT_T_TEST_PWR_GOOD
RESET*	F4	USBC_T_RESET_L
XTAL_25_IN	D22	TBT_T_XTAL25M_IN
XTAL_25_OUT	D23	TBT_T_XTAL25M_OUT
EE_DI	AB3	UPC_T_SPI_MOSI
EE_DO	AC4	UPC_T_SPI_MISO
EE_CS*	AC3	UPC_T_SPI_CS_L
EE_CLK	AB4	UPC_T_SPI_CLK

MISC

THERMDA	AC23	THERMDA
THERMDA	AB23	THERMDA
PCIE_ATEST	V18	PCIE_ATEST
TEST_EDM	AC1	TEST_EDM
FUSE_VQPS_64	L15	FUSE_VQPS_64
FUSE_VQPS_128	N15	FUSE_VQPS_128
MONDC_CIO_0	C23	MONDC_CIO_0
MONDC_CIO_1	C22	MONDC_CIO_1
MONDC_SVR	D6	MONDC_SVR
ATEST_P	A23	ATEST_P
ATEST_N	B23	ATEST_N
USB2_ATEST	E18	USB2_ATEST
MONDC_DPSNK_0	W13	MONDC_DPSNK_0
MONDC_DPSNK_1	W18	MONDC_DPSNK_1
MONDC_DPSRC	AB2	MONDC_DPSRC

DEBUG

RB030	100K
RB031	100K
RB050	14K
RB055	4.75K
RB054	499
RB051	3.01K
RB052	14K
RB053	499
RB034	2.2K
RB035	2.2K
RB036	2.2K
RB037	2.2K
RB027	100K
RB029	100
RB025	100

CB010	0.1UF	DP_TA_AUXCH_P
CB011	0.1UF	DP_TA_AUXCH_N
CB012	0.1UF	DP_TB_AUXCH_P
CB013	0.1UF	DP_TB_AUXCH_N

PP3V3_S5_TBT_T_SW

PLACE_NEAR=UB000.N16:2MM

PLACE_NEAR=UB000.N6:2MM

PLACE_NEAR=UB000.H6:2MM

PLACE_NEAR=UB000.J6:2MM

PLACE_NEAR=UB000.H19:2MM

PLACE_NEAR=UB000.F19:2MM

10K PU ON CLOCKS PAGE

PU at PCH

not used

To SPI Flash

GND_VOID=TRUE

DRAWING LAST_MODIFIED=Tue Aug 30 11:06:29 2016

SYNC_MASTER=J79_GREG SYNC_DATE=07/28/2015

PAGE TITLE

USB-C HIGH SPEED 1

Apple Inc.

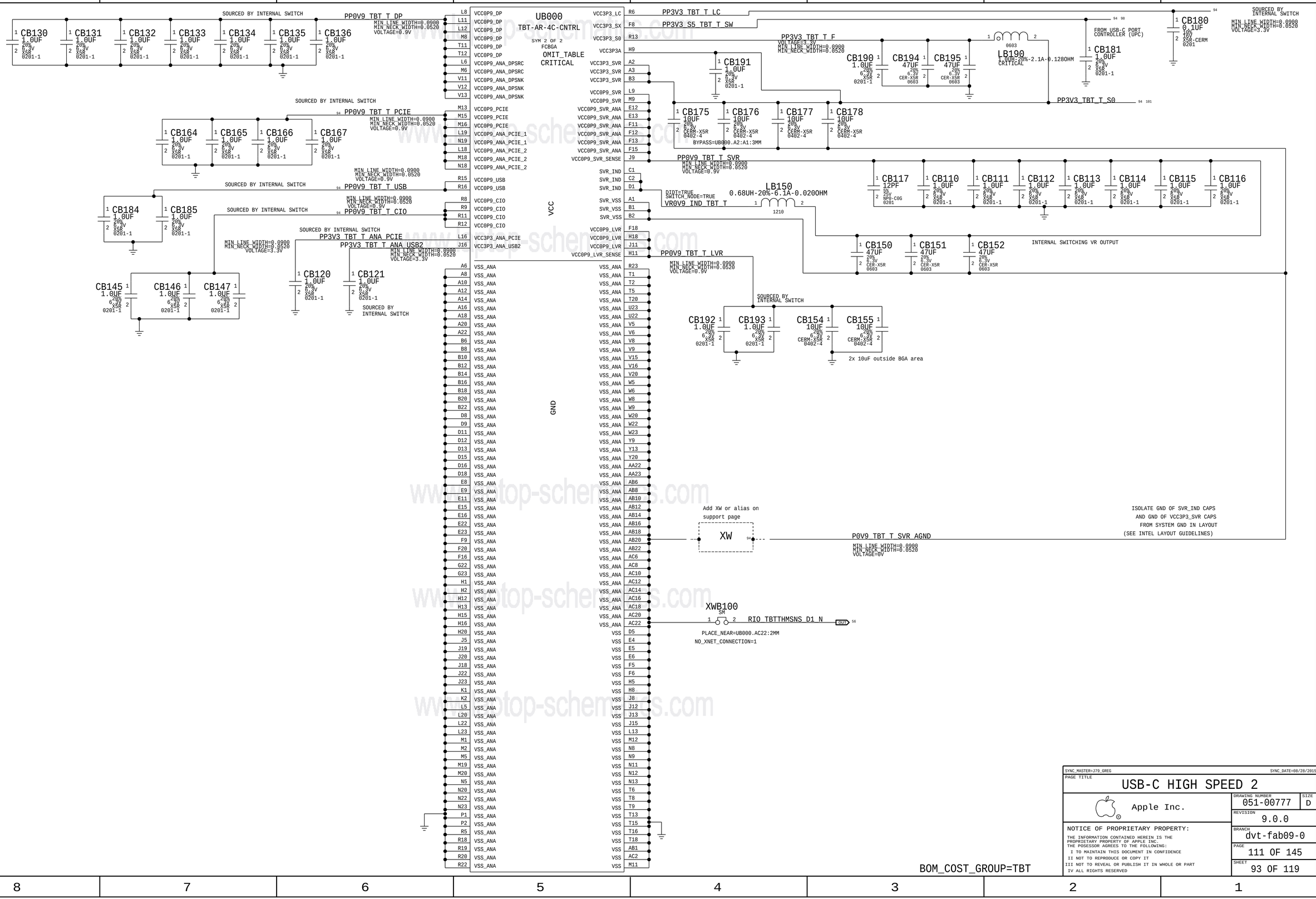
DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 110 OF 145

SHEET 92 OF 119



SYNC_MASTER=J79_GREG	SYNC_DATE=08/28/2015
PAGE TITLE	USB-C HIGH SPEED 2
Apple Inc.	DRAWING NUMBER 051-00777 · SIZE D
	REVISION 9.0.0
	BRANCH dvt-fab09-0
	PAGE 111 OF 145
	SHEET 93 OF 119

TMU CLKs

TBT_T_TMU_CLK_OUT — RB225 15 1/20W MF 201 — TBT_X_TMU_CLK_IN
PLACE_NEAR=UB000.V2:5mm
TBT_T_TMU_CLK_OUT — TBT_X_TMU_CLK_IN
RB224 100K 5% 1/20W MF 201

Ridge 0.9V SVR XW

NO_XNET_CONNECTION=1
XWB200 SHORT-L6-SM
P0V9_TBT_T_SVR_AGND

DP SRC OPTIONS

IF DP SRC NOT USED
DP_T_SRC_HPD — RB240 1M 5% 1/20W MF 201

NC_DP_T_SRC_ML_P<0>	NC_DP_T_SRC_ML_P<0>
NC_DP_T_SRC_ML_P<1>	NC_DP_T_SRC_ML_P<1>
NC_DP_T_SRC_ML_P<2>	NC_DP_T_SRC_ML_P<2>
NC_DP_T_SRC_ML_P<3>	NC_DP_T_SRC_ML_P<3>
NC_DP_T_SRC_ML_N<0>	NC_DP_T_SRC_ML_N<0>
NC_DP_T_SRC_ML_N<1>	NC_DP_T_SRC_ML_N<1>
NC_DP_T_SRC_ML_N<2>	NC_DP_T_SRC_ML_N<2>
NC_DP_T_SRC_ML_N<3>	NC_DP_T_SRC_ML_N<3>
NC_DP_T_SRC_AUX_P	NC_DP_T_SRC_AUX_P
NC_DP_T_SRC_AUX_N	NC_DP_T_SRC_AUX_N

MAKE_BASE=TRUE, NO_TEST=1

AR xtal

IN — TBT_T_XTAL25M_OUT — RB207 0 1/20W MF 201 — TBT_T_XTAL25M_OUT_R
NOSTUFF RB206 1M 1/20W MF 201
CRITICAL YB200 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
CB202 20PF 5% 25V C0G 0201
CB203 20PF 5% 25V C0G 0201
TBT_T_XTAL25M_IN — OUT

T RIDGE DEBUG CONN

USBC_DBG — JB201 505070-1220 M-ST-SM — Place on bottom

TBT_T_CIO_PLUG_EVENT_L	1	2	TBT_T_PCI_RESET_L
DP_T_SNK0_HPD	3	4	USBC_T_RESET_L
DP_T_SNK1_HPD	5	6	PP3V3_S5_TBT_T_SW
DP_TA_HPD	7	8	PP0V9_TBT_T_PCIE
TBT_POC_RESET	9	10	PP0V9_TBT_T_USB
PP3V3_TBT_T_LC	11	12	PP0V9_TBT_T_CIO
	13	14	
	15	16	

RIDGE JTAG ISOLATION

PLACE_NEAR=U0500.J1:10mm
TBT_DBG
JTAG_TBT_TCK — RB243 15 — XDP_JTAG_ISP_TCK
JTAG_TBT_TDI — RB244 15 — XDP_JTAG_ISP_TDI
RB246 100K 5% 1/20W MF 201
RB245 100K 5% 1/20W MF 201
TBT_DBG
PLACE_NEAR=U0500.J2:10mm

Ridge PWR ENs

PP3V3_S0
TBT_T_CIO_PWR_EN — RB271 100K
TBT_T_USB_PWR_EN — RB272 100K

Ridge PDs

DP_T_SNK0_DDC_CLK	RB267 100K
DP_T_SNK0_DDC_DATA	RB268 100K
DP_T_SNK1_DDC_CLK	RB269 100K
DP_T_SNK1_DDC_DATA	RB270 100K

ACE A/B RPD STRAPPING

USBC_TA_CC1	USBC_TA_CC1
USBC_TA_CC2	USBC_TA_CC2
USBC_TB_CC1	USBC_TB_CC1
USBC_TB_CC2	USBC_TB_CC2

MAKE_BASE=TRUE

ACE FET DCIN Bypass Caps

PPDCIN_G3H
CB211 0.1UF 10% 35V CER-X5R 0201
CB212 0.1UF 10% 35V CER-X5R 0201
CB213 0.1UF 10% 35V CER-X5R 0201
CB214 0.1UF 10% 35V CER-X5R 0201

ACE PDs

UPC_TA_DBG3	RB260 100K
UPC_TA_DBG4	RB261 100K
UPC_TB_DBG3	RB262 100K
UPC_TB_DBG4	RB263 100K
UPC_TA_DBG1	RB264 100K
UPC_TA_DBG2	RB265 100K
UPC_T_5V_EN	RB232 100K

5% 1/20W MF 201

FUSES FOR UPC

FB200 0603 6AMP-32V-0.00950HM CRITICAL PLACE_NEAR=QB300:5MM
PP20V_USBC_TA_VBUS — PP20V_USBC_TA_VBUS_F
FB201 0603 6AMP-32V-0.00950HM CRITICAL PLACE_NEAR=QB400:5MM
PP20V_USBC_TB_VBUS — PP20V_USBC_TB_VBUS_F

T ACEs DEBUG CONN

USBC_DBG — JB200 505070-1220 M-ST-SM — Place on bottom

I2C_TBT_TB_INT_L	1	2	I2C_TBT_TA_INT_L
I2C_UPC_T_SCL2	3	4	I2C_TBT_T_SDA
I2C_UPC_T_SDA2	5	6	I2C_TBT_T_SCL
SMC_USBC_INT_L	7	8	TBT_T_CIO_PWR_EN
TBT_T_SPI_CLK_DBG	9	10	TBT_T_USB_PWR_EN
UPC_TA_UART_TX	11	12	UPC_TA_UART_RX
	13	14	
	15	16	

T ACE-SMC I2C SERIES R'S

PLACE_NEAR=U5000:5mm
I2C_UPC_T_SDA2 — RB241 33 — SMBUS_SMC_4_G3H_SDA
PLACE_NEAR=U5000:5mm
I2C_UPC_T_SCL2 — RB242 33 — SMBUS_SMC_4_G3H_SCL

USB2 AR PDs

USB_UPC_TA_P	RB220 0
USB_UPC_TA_N	RB221 0
USB_UPC_TB_P	RB222 0
USB_UPC_TB_N	RB223 0

5% 1/20W MF 201

ACE Debug Support

UPC_TA_DBG_UART_TX — OMIT RB289 NOSTUFF 402
UPC_TA_DBG_UART_RX
UPC_TB_DBG_UART_TX — OMIT RB288 NOSTUFF 402
UPC_TB_DBG_UART_RX

GND ALIASES

GND

NC/NO TEST

NO_TEST=1
NC_UPC_TB_I2C_ADDR

SIGNAL ALIASES

TBT_T_CIO_PWR_EN	TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN	TBT_T_USB_PWR_EN
PM_BATLOW_L	PM_BATLOW_L
UPC_T_5V_EN	UPC_T_5V_EN
JTAG_ISP_TDO	JTAG_ISP_TDO
TBT_POC_RESET	TBT_POC_RESET
TBT_T_CIO_PLUG_EVENT_L	TBT_T_CIO_PLUG_EVENT_L
XDP_USB_EXTC_OC_L	XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L	XDP_USB_EXTD_OC_L
JTAG_TBT_T_TMS	JTAG_TBT_T_TMS
S3X_JTAG_TCK	S3X_JTAG_TCK
S3X_JTAG_TMS	S3X_JTAG_TMS
NC_USBC_TB_RESET_L	NC_USBC_TB_RESET_L
USB_UPC_PCH_TA_N	USB_UPC_PCH_TA_N
USB_UPC_PCH_TA_P	USB_UPC_PCH_TA_P
USB_UPC_PCH_TB_N	USB_UPC_PCH_TB_N
USB_UPC_PCH_TB_P	USB_UPC_PCH_TB_P

MAKE_BASE=TRUE

POWER ALIASES

PP3V3_UPC_TA_LDO	PP3V3_UPC_TA_LDO
PP3V3_UPC_TB_LDO	PP3V3_UPC_TB_LDO
PP20V_USBC_TA_VBUS	PP20V_USBC_TA_VBUS
PP20V_USBC_TB_VBUS	PP20V_USBC_TB_VBUS
PP5V_S4_T_USBC	PP5V_S4_T_USBC
PP3V3_TBT_T_S0	PP3V3_TBT_T_S0

MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=5V
MIN_LINE_WIDTH=0.0900 MIN_NECK_WIDTH=0.0520 VOLTAGE=3.3V

AR/ACE SPI BUS SERIES R'S

TBT_T_SPI_CLK	RB290 100	TBT_T_SPI_CLK_DBG	
TBT_T_SPI_CS_L	RB280 15	UPC_TA_SPI_CLK	IN
TBT_T_SPI_MOSI	RB281 15	UPC_TA_SPI_CS_L	IN
TBT_T_SPI_MISO	RB282 15	UPC_TA_SPI_MOSI	IN
ROM	RB283 15	UPC_TA_SPI_MISO	OUT
	RB284 15	UPC_T_SPI_CLK	IN
	RB285 15	UPC_T_SPI_CS_L	IN
	RB286 15	UPC_T_SPI_MOSI	IN
	RB287 15	UPC_T_SPI_MISO	OUT

Ace / AR

TBT to ACE

TBT
Alpine Ridge U2800
(MASTER)
I2C_TBT_T_SCL
I2C_TBT_T_SDA
I2C_TBT_TA_INT_L
I2C_TBT_TB_INT_L

Pri ACE
U3100
(Write: 0x70 Read: 0x71)
I2C_TBT_T_SCL
I2C_TBT_T_SDA
I2C_TBT_TA_INT_L

Sec ACE
U3200
(Write: 0x7E Read: 0x7F)
I2C_TBT_T_SCL
I2C_TBT_T_SDA
I2C_TBT_TB_INT_L

Ridge PCIE Caps D2R

PCIE_TBT_T_D2R_C_P<0>	CB250 0.22UF	PCIE_TBT_T_D2R_P<0>
PCIE_TBT_T_D2R_C_N<0>	CB251 0.22UF	PCIE_TBT_T_D2R_N<0>
PCIE_TBT_T_D2R_C_P<1>	CB252 0.22UF	PCIE_TBT_T_D2R_P<1>
PCIE_TBT_T_D2R_C_N<1>	CB253 0.22UF	PCIE_TBT_T_D2R_N<1>

0201 X5R 6.3V 20%
GND_VOID=TRUE

NC_PCIE_TBT_T_D2R_C_P<2>	NC_PCIE_TBT_T_D2R_C_P<2>
NC_PCIE_TBT_T_D2R_C_N<2>	NC_PCIE_TBT_T_D2R_C_N<2>
NC_PCIE_TBT_T_D2R_C_P<3>	NC_PCIE_TBT_T_D2R_C_P<3>
NC_PCIE_TBT_T_D2R_C_N<3>	NC_PCIE_TBT_T_D2R_C_N<3>

MAKE_BASE=TRUE, NO_TEST=1

R2D

PCIE_TBT_T_R2D_C_P<0>	CB240 0.22UF	PCIE_TBT_T_R2D_P<0>
PCIE_TBT_T_R2D_C_N<0>	CB241 0.22UF	PCIE_TBT_T_R2D_N<0>
PCIE_TBT_T_R2D_C_P<1>	CB242 0.22UF	PCIE_TBT_T_R2D_P<1>
PCIE_TBT_T_R2D_C_N<1>	CB243 0.22UF	PCIE_TBT_T_R2D_N<1>

0201 X5R 6.3V 20%
GND_VOID=TRUE

NC_PCIE_TBT_T_R2D_P<2>	NC_PCIE_TBT_T_R2D_P<2>
NC_PCIE_TBT_T_R2D_N<2>	NC_PCIE_TBT_T_R2D_N<2>
NC_PCIE_TBT_T_R2D_P<3>	NC_PCIE_TBT_T_R2D_P<3>
NC_PCIE_TBT_T_R2D_N<3>	NC_PCIE_TBT_T_R2D_N<3>

MAKE_BASE=TRUE, NO_TEST=1

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C Support
Apple Inc.
DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 112 OF 145
SHEET: 94 OF 119

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

QB300
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

94 PP20V_USBC_TA_VBUS_F
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=20V

94 PP20V_USBC_TA_VBUS
CB301 1UF 10% 35V X5R 0402

PPDCIN_G3H 29 30 94 96 100
MAX 100uF TOTAL ON RAIL

UPC_TA_GATE1
UPC_TA_GATE2

94 PP3V3_UPC_TA_LDO
100 PP3V3_G3H
96 30 29 28 GND
94 PP5V_S4_T_USBC
CAP FOR PP_5V0 ON VR PAGE
CB300 10UF 20% 6.3V CERM-X5R 0402-1

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
PP3V3_UPC_TA_LDO 94
P3V3_TBT_T_SX_EN_R 98
PP1V8_UPC_TA_LDOA
PP1V8_UPC_TA_LDOD
PP1V1_UPC_TA_LDO_BMC
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.1100
VOLTAGE=1.1V
CB304 2.2UF 20% 6.3V X5R-CERM 0201
CB305 1.0UF 20% 6.3V X5R 0201-1
CB306 0.47UF 10% 6.3V CERM-X5R 0201
CB308 10UF 20% 6.3V CERM-X5R 0402-1

PULL R3109 AND R3108 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES

GND 94
1M RB309 5% 1/20W MF 201 I2C_UPC_TA_DBG_CTL_SCL 95
1M RB308 5% 1/20W MF 201 I2C_UPC_TA_DBG_CTL_SDA 95

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

UB300
CD3215A
BGA

96 94 IN	TBT_POC_RESET	E11	MRESET	PRIMARY ONLY	
98 OUT	USBC_T_RESET_L_R	F11	RESET*	PRIMARY ONLY	
94	UPC_TA_DBG_UART_TX	B2	GPIO0		
94	UPC_TA_DBG_UART_RX	C2	GPIO1		
96 94 92 IN	TBT_T_CIO_PWR_EN	D10	GPIO2		
96 94 92 IN	TBT_T_USB_PWR_EN	G11	GPIO3		
94 92 OUT	DP_TA_HPD	C10	GPIO4		
94	GND	E10	GPIO5		
94 OUT	UPC_T_5V_EN	G10	GPIO6		
96 30 29 28 OUT	SMC_PME_S4_DARK_L	D7	GPIO7		
94 OUT	XDP_USB_EXTC_OC_L	H6	GPIO8		
94 IN	GND	F10	BUSPOWERZ		
GND I2C ADDR PRIMARY ONLY	GND	F1	I2C_ADDR		
CRITICAL RB303 15K 0.1% 1/20W TF-LF 0201 NEED 0.1%	UPC_TA_R_OSC	G2	R_OSC		
95	I2C_UPC_TA_DBG_CTL_SCL	E4	DEBUG_CTL1		
95	I2C_UPC_TA_DBG_CTL_SDA	D5	DEBUG_CTL2		
94 BI	I2C_TBT_T_SDA	D1	I2C_SDA1		
94 BI	I2C_TBT_T_SCL	D2	I2C_SCL1		
94 OUT	I2C_TBT_TA_INT_L	C1	I2C_IRQ1*		
TO SMC					
94 BI	I2C_UPC_T_SDA2	A5	I2C_SDA2		
94 BI	I2C_UPC_T_SCL2	B5	I2C_SCL2		
51 OUT	SMC_USBC_INT_L	B6	I2C_IRQ2*		
94 OUT	UPC_TA_SPI_CLK	A3	SPI_CLK		
94 OUT	UPC_TA_SPI_MOSI	B4	SPI_MOSI		
94 IN	UPC_TA_SPI_MISO	A4	SPI_MISO		
94 OUT	UPC_TA_SPI_CS_L	B3	SPI_SSZ		
REAR PORT: CONNECT UPC SPI TO ROM FRONT PORT: GROUND UPC SPI					
	TP_UPC_TA_SWD_DATA	F4	SWD_DATA		
	TP_UPC_TA_SWD_CLK	G4	SWD_CLK		
96 95 94 IN	UPC_TA_UART_RX	F2	UART_RX		
96 94 OUT	UPC_TA_UART_TX	E2	UART_TX		
92 IN	TBT_TA_LSTX	L4	LSX_R2P		
92 OUT	TBT_TA_LSRX	K4	LSX_P2R		
	USB_UPC_TA_F_P	L5	USB_RP_P		
	USB_UPC_TA_F_N	K5	USB_RP_N		
	DP_TA_AUXCH_P	J1	AUX_P		
	DP_TA_AUXCH_N	J2	AUX_N		
94 BI	UPC_TA_DBG1	L2	DEBUG1		
94 BI	UPC_TA_DBG2	K2	DEBUG2		
94 BI	UPC_TA_DBG3	L3	DEBUG3		
94 BI	UPC_TA_DBG4	K3	DEBUG4		

CRITICAL
OMIT_TABLE

HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX

SS H7 UPC_TA_SS
SENSEP B10
SENSEN A10
HV_GATE1 B9
HV_GATE2 A9
CB309 0.47UF 10% 6.3V CERM-X5R 0201

C_CC1 L9 USBC_TA_CC1 BI 94 97 104
C_CC2 L10 USBC_TA_CC2 BI 94 97 104
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.2000
CB314 220PF 10% 16V CER-X7R 0201
CB313 220PF 10% 16V CER-X7R 0201
RPD_G1 K9 USBC_TA_CC1 BI 94
RPD_G2 K10 USBC_TA_CC2 BI 94
C_USB_TP K6 USBC_TA_USB_TOP_P BI 97
C_USB_TN L6 USBC_TA_USB_TOP_N BI 97
C_USB_BP K7 USBC_TA_USB_BOT_P BI 97
C_USB_BN L7 USBC_TA_USB_BOT_N BI 97
C_SBU1 K8 USBC_TA_SBU1 BI 97
C_SBU2 L8 USBC_TA_SBU2 BI 97
NC L11 GROUND
NC or GND to dissipate heat

1M RB305 5% 1/20W MF 201 UPC_TA_UART_RX 94 95 96

LB300
90-OHM-0.1A
EXCX4CE
USB_UPC_PCH_TA_P 94 BI 1 4 PLACE_NEAR=UB300.L5:5mm
USB_UPC_PCH_TA_N 94 BI 2 3 PLACE_NEAR=UB300.K5:5mm

PP3V3_UPC_TA_LDO 94
PU to PP3V3_S4 if convenient for layout
Otherwise PU to PP3V3_UPC_TA_LDO
NO_XNET_CONNECTION=1
RB310 100K 5% 1/20W MF 201
92 BI
92 BI
RB311 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

A1 GND
D6 GND
E5 GND
E6 GND
E7 GND
F5 GND
G5 GND
H4 GND
H5 GND
G8 GND
H8 GND
L1 GND
B8 GND
D8 GND
E8 GND
F6 GND
F7 GND
F8 GND
G6 GND
G7 GND
GND 94
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C PORT CONTROLLER A
Apple Inc.	DRAWING NUMBER 051-00777
	SIZE D
	REVISION 9.0.0
	BRANCH dvt-fab09-0
	PAGE 113 OF 145
	SHEET 95 OF 119

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

PULL R3209 AND R3208 UP TO ACE1 LDO8 FOR 1ST BRIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

GND

1M RB409 I2C_UPC_TB_DBG_CTL_SCL
1M RB408 I2C_UPC_TB_DBG_CTL_SDA
5% 1/20W MF 201

1M RB405 UPC_TA_UART_TX
5% 1/20W MF 201

QB400
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

PP20V_USBC_TB_VBUS_F
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=20V

PP20V_USBC_TB_VBUS
CB401 1UF 10% 25V X5R 0402

PPDCIN_G3H
MAX 100uF TOTAL ON RAIL

UPC_TB_GATE1
UPC_TB_GATE2

PP3V3_UPC_TB_LDO
PP3V3_G3H
GND
PP5V_S4_T_USBC
CAP FOR PP_5V0 ON VR PAGE
CB400 10UF 20% 6.3V CERM-X5R 0402-1

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
PP3V3_UPC_TB_LDO
P3V3_TBT_T_SX_EN_R
PP1V8_UPC_TB_LDOA
PP1V8_UPC_TB_LDOD
PP1V1_UPC_TB_LDO_BMC
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.1V

CB404 2.2UF 20% 6.3V X5R CERM 0201
CB405 1.0UF 20% 6.3V X5R 0201-1
CB406 0.47UF 10% 6.3V CERM-X5R 0201
CB408 10UF 20% 6.3V CERM-X5R 0402-1

CRITICAL
OMIT_TABLE

UB400
CD3215A
BGA

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

TBT_POC_RESET	E11	MRESET
NC_USBC_TB_RESET_L	F11	RESET*
UPC_TB_DBG_UART_TX	B2	GPIO0
UPC_TB_DBG_UART_RX	C2	GPIO1
TBT_T_CIO_PWR_EN	D10	GPIO2
TBT_T_USB_PWR_EN	G11	GPIO3
DP_TB_HPD	C10	GPIO4
GND	E10	GPIO5
UPC_T_5V_EN	G10	GPIO6
SMC_PME_S4_DARK_L	D7	GPIO7
XDP_USB_EXTD_OC_L	H6	GPIO8
GND	F10	BUSPOWERZ
NC_UPC_TB_I2C_ADDR	F1	I2C_ADDR
UPC_TB_R_OSC	G2	R_OSC
I2C_UPC_TB_DBG_CTL_SCL	E4	DEBUG_CTL1
I2C_UPC_TB_DBG_CTL_SDA	D5	DEBUG_CTL2
I2C_TBT_T_SDA	D1	I2C_SDA1
I2C_TBT_T_SCL	D2	I2C_SCL1
I2C_TBT_TB_INT_L	C1	I2C_IRQ1*
I2C_UPC_T_SDA2	A5	I2C_SDA2
I2C_UPC_T_SCL2	B5	I2C_SCL2
SMC_USBC_INT_L	B6	I2C_IRQ2*
GND	A3	SPI_CLK
GND	B4	SPI_MOSI
GND	A4	SPI_MISO
GND	B3	SPI_SSZ
TP_UPC_TB_SWD_DATA	F4	SWD_DATA
TP_UPC_TB_SWD_CLK	G4	SWD_CLK
UPC_TA_UART_TX	F2	UART_RX
UPC_TA_UART_RX	E2	UART_TX
TBT_TB_LSTX	L4	LSX_R2P
TBT_TB_LSRX	K4	LSX_P2R
USB_UPC_TB_F_P	L5	USB_RP_P
USB_UPC_TB_F_N	K5	USB_RP_N
DP_TB_AUXCH_P	J1	AUX_P
DP_TB_AUXCH_N	J2	AUX_N
S3X_JTAG_TCK	L2	DEBUG1
S3X_JTAG_TMS	K2	DEBUG2
UPC_TB_DBG3	L3	DEBUG3
UPC_TB_DBG4	K3	DEBUG4

CRITICAL
RB403 15K 0.1% 1/20W TF-LF 0201
NEED 0.1%

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

LB400
90-OHM-0.1A
EXCX4CE

USB_UPC_PCH_TB_P
USB_UPC_PCH_TB_N
PLACE_NEAR=UB400.L5:5mm
PLACE_NEAR=UB400.K5:5mm

PP3V3_UPC_TB_LDO
PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_TB_LDO
NO_XNET_CONNECTION=1
RB410 100K 5% 1/20W MF 201
RB411 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

HV FET/SENSE

SS	H7	UPC_TB_SS
SENSEP	B10	
SENSEN	A10	
HV_GATE1	B9	
HV_GATE2	A9	

CB409 0.47UF 10% 6.3V CERM-X5R 0201

DIGITAL CORE I/O AND CONTROL

TYPE-C

C_CC1	L9	USBC_TB_CC1
C_CC2	L10	USBC_TB_CC2
RPD_G1	K9	USBC_TB_CC1
RPD_G2	K10	USBC_TB_CC2
C_USB_TP	K6	USBC_TB_USB_TOP_P
C_USB_TN	L6	USBC_TB_USB_TOP_N
C_USB_BP	K7	USBC_TB_USB_BOT_P
C_USB_BN	L7	USBC_TB_USB_BOT_N
C_SBU1	K8	USBC_TB_SBU1
C_SBU2	L8	USBC_TB_SBU2
NC	L11	GROUND

NC or GND to dissipate heat

CB414 220PF 10% 16V CER-X7R 0201
CB413 220PF 10% 16V CER-X7R 0201

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.2000

PORT MUX

GND pins: A1 D6 E5 E6 E7 F5 G5 H4 H5 D8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7

GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

SYNC_MASTER=J79_BRIS SYNC_DATE=02/28/2022

PAGE TITLE: USB-C PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER: 051-00777
SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 114 OF 145
SHEET: 96 OF 119

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	CB504, CB554	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE: USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D

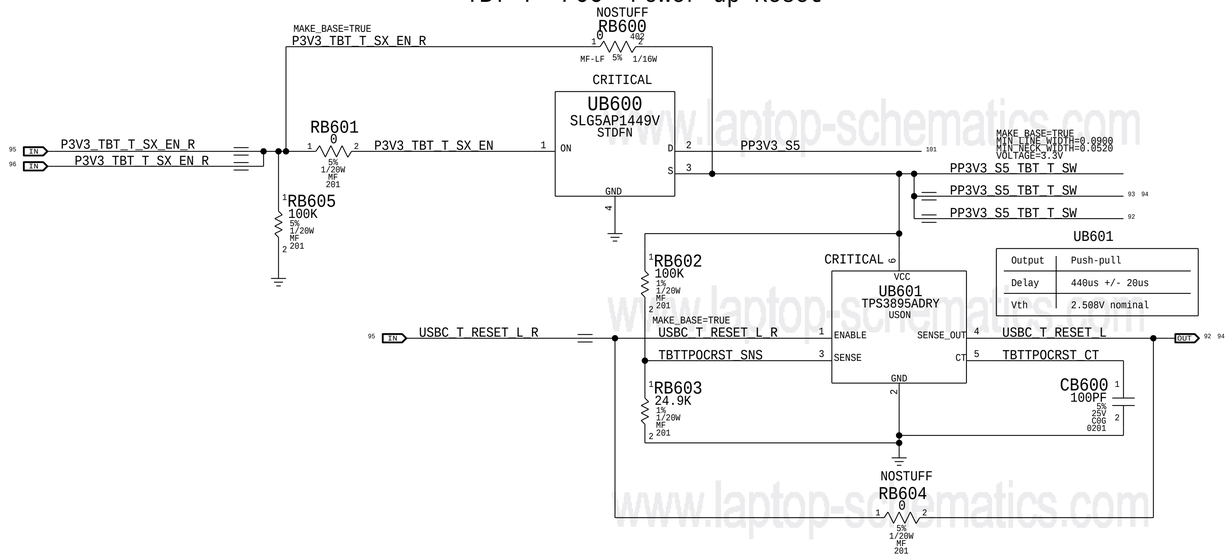
REVISION: 9.0.0

BRANCH: dvt-fab09-0

PAGE: 115 OF 145

SHEET: 97 OF 119

TBT T "POC" Power-up Reset



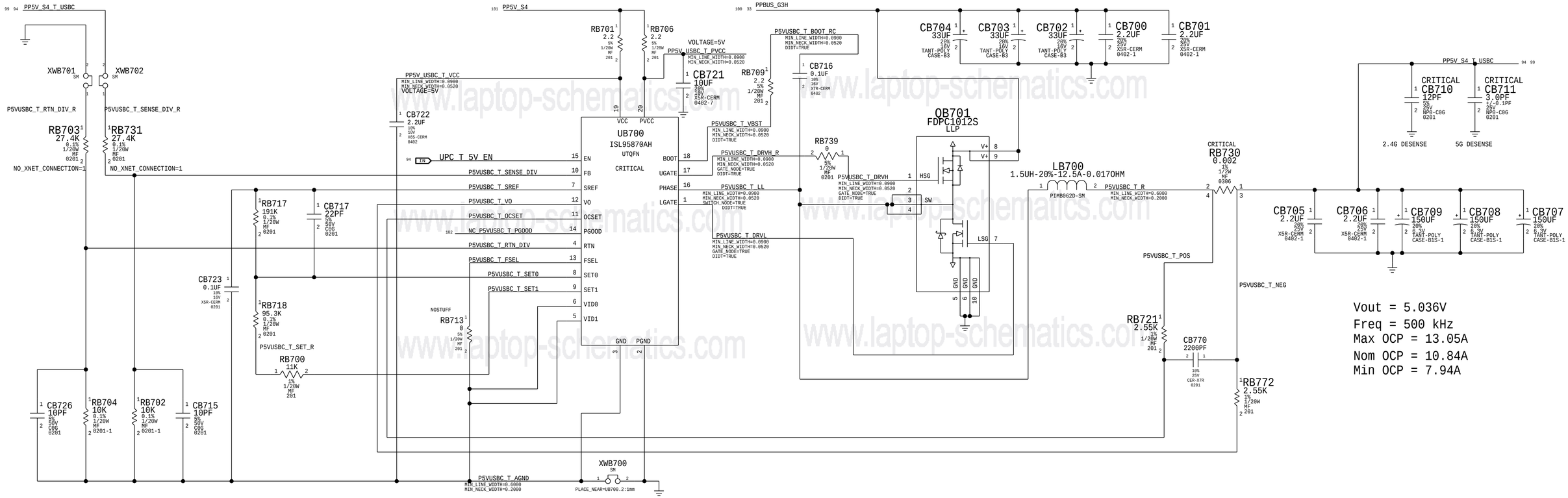
BOM_COST_GROUP=USB-C

DESIGN: j130/dev_mlb_u
LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR B

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 116 OF 145
SHEET 98 OF 119



PAGE TITLE

TBT 5V REGULATOR

Apple Inc.

DRAWING NUMBER 051-00777 | SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 117 OF 145

SHEET 99 OF 119

PBUS Rails

66 PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE
PPBUS_G3H 52
PPBUS_G3H 52
PPBUS_G3H 52
PPBUS_G3H 79
PPBUS_G3H 52
PPBUS_G3H 52
PPBUS_G3H 74
PPBUS_G3H 65
PPBUS_G3H 76
PPBUS_G3H 33 99
PPBUS_G3H 76
PPBUS_G3H 62 63
PPBUS_G3H 91

52 PPBUS_HS_CPU
PPBUS_HS_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.2V
MAKE_BASE=TRUE
PPBUS_HS_CPU 68
PPBUS_HS_CPU 68
PPBUS_HS_CPU 70
PPBUS_HS_CPU 75
PPBUS_HS_CPU 73
PPBUS_HS_CPU 75
PPBUS_HS_CPU 67

52 PPBUS_HS_OTH5V
PPBUS_HS_OTH5V
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE
PPBUS_HS_OTH5V 72

52 PPBUS_HS_OTH3V3
PPBUS_HS_OTH3V3
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE
PPBUS_HS_OTH3V3 72

52 PPBUS_S4_HS_TPAD
PPBUS_S4_HS_TPAD
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=13.1V
MAKE_BASE=TRUE
PPBUS_S4_HS_TPAD 43

MAKE_BASE=TRUE
96 95 94 30 29 PPDCIN_G3H
PPDCIN_G3H
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=20V
66 104
52 PPDCIN_G3H

3V3 G3H Rails

104 65 PP3V3_G3H
PP3V3_G3H
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_G3H 59
PP3V3_G3H 57 80
PP3V3_G3H 50 100
PP3V3_G3H 66
PP3V3_G3H 43 50 104
PP3V3_G3H 51
PP3V3_G3H 49
PP3V3_G3H 18
PP3V3_G3H 51
PP3V3_G3H 29
PP3V3_G3H 30
PP3V3_G3H 106
PP3V3_G3H 77
PP3V3_G3H 95
PP3V3_G3H 96
PP3V3_G3H 50 100

57 49 48 PP3V3_G3H_SMC_ISNS
PP3V3_G3H_SMC_ISNS
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

RTC Rails

74 PP3V0_G3H
PP3V0_G3H
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.0V
MAKE_BASE=TRUE
PP3V0_G3H 8 12 14 15
PP3V0_G3H 74

IMVP Rails

68 PPVCC_S0_CPU
PPVCC_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.5V
MAKE_BASE=TRUE
PPVCC_S0_CPU 8 54 104
PPVCC_S0_CPU 10

68 PPVCCSA_S0_CPU
PPVCCSA_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.5V
MAKE_BASE=TRUE
PPVCCSA_S0_CPU 8 55
PPVCCSA_S0_CPU 10

70 PPVCCGT_S0_CPU
PPVCCGT_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.5V
MAKE_BASE=TRUE
PPVCCGT_S0_CPU 8 54
PPVCCGT_S0_CPU 11
PPVCCGT_S0_CPU 8
PPVCCGT_S0_CPU 11

CPU VCCIO Rails

75 PPVCCIO_S0_CPU
PPVCCIO_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.95V
MAKE_BASE=TRUE
PPVCCIO_S0_CPU 5 8
PPVCCIO_S0_CPU 10

CPU EDRAM Rails

73 PPVCCEDRAM_S0_CPU
PPVCCEDRAM_S0_CPU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.05V
MAKE_BASE=TRIMF
PPVCCEDR[illegible] S0_CPU 8
PP[illegible] 8
PP[illegible] 8
PPVCCEDRAM_S0_CPU 10
PPVCCEDRAM_S0_CPU 8
PPVCCEDRAM_S0_CPU 8
PPVCCEDRAM_S0_CPU 10

PCH Prime Core Rails

76 PPVCCPRIMCORE_SUS_PCH
PPVCCPRIMCORE_SUS_PCH
MIN_LINE_WI [illegible] 0.0900
MIN [illegible]
VOL [illegible]
MAK [illegible]
PI [illegible] 8 1

1V2 Rails

78 75 PP1V2_S3
PP1V2_S3
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_S3 21 22 23 24
PP1V2_S3 75
PP1V2_S3 20
PP1V2_S3 21 22 23 24
PP1V2_S3 21 22 23 24
PP1V2_S3 53
PP1V2_S3 78

53 PP1V2_S3_CPUDDR
PP1V2_S3_CPUDDR
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_S3_CPUDDR 8
PP1V2_S3_CPUDDR 8
PP1V2_S3_CPUDDR 10
PP1V2_S3_CPUDDR 10

78 PP1V2_S0SW
PP1V2_S0SW
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.2V
MAKE_BASE=TRUE
PP1V2_S0SW 8 10

0V6 Rails

75 PP0V6_S0_DDRVTT
PP0V6_S0_DDRVTT
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=0.6V
MAKE_BASE=TRUE
PP0V6_S0_DDRVTT 25
PP0V6_S0_DDRVTT 25

20 PP0V6_S3_MEM_VREFDQ_A
PP0V6_S3_MEM_VREFDQ_A
MAKE_BASE=TRUE
VOLTAGE=0.6V
21 22
100 20 PP0V6_S3_MEM_VREFCA_A
PP0V6_S3_MEM_VREFCA_A
MAKE_BASE=TRUE
VOLTAGE=0.6V
21 22
20 PP0V6_S3_MEM_VREFDQ_B
PP0V6_S3_MEM_VREFDQ_B
MAKE_BASE=TRUE
VOLTAGE=0.6V
23 24
100 20 PP0V6_S3_MEM_VREFCA_A
PP0V6_S3_MEM_VREFCA_A
MAKE_BASE=TRUE
VOLTAGE=0.6V
23 24

1V8 Rails

76 PP1V8_SUS
PP1V8_SUS
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_SUS 8 14 19
PP1V8_SUS 8 12
PP1V8_SUS 78
PP1V8_SUS 78
PP1V8_SUS 8
PP1V8_SUS 8
PP1V8_SUS 12

78 PP1V8_S4
PP1V8_S4
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S4 38 42
PP1V8_S4 18 19 35

78 PP1V8_S3
PP1V8_S3
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S3 55
PP1V8_S3 74

55 PP1V8_S3_MEM
PP1V8_S3_MEM
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.8V
MAKE_BASE=TRUE
PP1V8_S3_MEM 21 22 23 24

78 PP1V8_S0
PP1V8_S0
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP1V8_S0 106
PP1V8_S0 12
PP1V8_S0 60 62 63 104
PP1V8_S0 19 106
PP1V8_S0 37 38 42
PP1V8_S0 74
PP1V8_S0 18
PP1V8_S0 37 42
PP1V8_S0 37
PP1V8_S0 19

PAGE TITLE
Power Aliases - 1

Apple Inc.

DRAWING NUMBER 051-00777
SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 120 OF 145
SHEET 100 OF 119

1V0 Rails

PP1V0_SUS
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.0V
MAKE_BASE=TRUE

PP1V0_SUSSW
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1V
MAKE_BASE=TRUE

PP1V0_S3
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1V
MAKE_BASE=TRUE

PP1V0_S0SW
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1V
MAKE_BASE=TRUE

T208 Rails

PP3V3_S5_T139
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4_SOC_PMU
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP5V_S0_T139
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

GND
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0700
VOLTAGE=0V

Digital Ground

GND
MIN_NECK_WIDTH=0.0700
MIN_LINE_WIDTH=0.0900

5V Rails

PP5V_S5
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4SW
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S4SW_ISNS
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_S0_KBD
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=5V
MAKE_BASE=TRUE

3V3 Rails

PP3V3_S5
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_SUS
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_TBT_X_S0

PP3V3_TBT_T_S0

PP3V3_S4_BT
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4_TPAD
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S4SW_SNS
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S5_SSD_LB
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=3.3V

PP3V3_S5_SSD
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=3.3V

PP3V3_S4_MESA
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_2V7_NAND_VCC
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=2.7V
MAKE_BASE=TRUE

PAGE TITLE	Power Aliases - 2
	Apple Inc.
DRAWING NUMBER	051-00777
SIZE	D
REVISION	9.0.0
BRANCH	dvt-fab09-0
PAGE	121 OF 145
SHEET	101 OF 119

UNUSED TP ALIASES

83	IN	NC_S3X_VSS_S	NC_S3X_VSS_S	MAKE_BASE=TRUE	NO_TEST=1
82	IN	NC_S3X_VDD_S	NC_S3X_VDD_S	MAKE_BASE=TRUE	NO_TEST=1
81	IN	NC_S3X_PMIC_CTRL_2	NC_S3X_PMIC_CTRL_2	MAKE_BASE=TRUE	NO_TEST=1
81	IN	NC_S3X_PCIE_ATB1	NC_S3X_PCIE_ATB1	MAKE_BASE=TRUE	NO_TEST=1
81	IN	NC_S3X_PCIE_ATB0	NC_S3X_PCIE_ATB0	MAKE_BASE=TRUE	NO_TEST=1
81	IN	NC_S3X_DT1	NC_S3X_DT1	MAKE_BASE=TRUE	NO_TEST=1
81	IN	NC_S3X_DT0	NC_S3X_DT0	MAKE_BASE=TRUE	NO_TEST=1
81	IN	NC_S3X_DDR_ATO	NC_S3X_DDR_ATO	MAKE_BASE=TRUE	NO_TEST=1
74	IN	NC_PMIC_PGG	NC_PMIC_PGG	MAKE_BASE=TRUE	NO_TEST=1
74	IN	NC_PMIC_PGF	NC_PMIC_PGF	MAKE_BASE=TRUE	NO_TEST=1
74	IN	NC_PMIC_PGE	NC_PMIC_PGE	MAKE_BASE=TRUE	NO_TEST=1
74	IN	NC_PMIC_PGD	NC_PMIC_PGD	MAKE_BASE=TRUE	NO_TEST=1
74	IN	NC_PMIC_PGC	NC_PMIC_PGC	MAKE_BASE=TRUE	NO_TEST=1
88	IN	NC_PICCOLO_24M_CLK_REQ	NC_PICCOLO_24M_CLK_REQ	MAKE_BASE=TRUE	NO_TEST=1
14	IN	NC_PCH_SLP_A_L	NC_PCH_SLP_A_L	MAKE_BASE=TRUE	NO_TEST=1
14	IN	NC_PCH_PME_L	NC_PCH_PME_L	MAKE_BASE=TRUE	NO_TEST=1
14	IN	NC_PCH_LANPHYPC	NC_PCH_LANPHYPC	MAKE_BASE=TRUE	NO_TEST=1
14	IN	NC_PCH_GPP_F9	NC_PCH_GPP_F9	MAKE_BASE=TRUE	NO_TEST=1
14	IN	NC_PCH_GPP_F8	NC_PCH_GPP_F8	MAKE_BASE=TRUE	NO_TEST=1
14	IN	NC_PCH_GPP_F10	NC_PCH_GPP_F10	MAKE_BASE=TRUE	NO_TEST=1
16	IN	NC_PCH_GPP_D4	NC_PCH_GPP_D4	MAKE_BASE=TRUE	NO_TEST=1
16	IN	NC_PCH_GPP_D3	NC_PCH_GPP_D3	MAKE_BASE=TRUE	NO_TEST=1
16	IN	NC_PCH_GPP_D1	NC_PCH_GPP_D1	MAKE_BASE=TRUE	NO_TEST=1
14	IN	NC_PCH_GPP_D0	NC_PCH_GPP_D0	MAKE_BASE=TRUE	NO_TEST=1
14	IN	NC_PCH_GPD7	NC_PCH_GPD7	MAKE_BASE=TRUE	NO_TEST=1
99	IN	NC_P5VUSBC_T_PGOOD	NC_P5VUSBC_T_PGOOD	MAKE_BASE=TRUE	NO_TEST=1
34	IN	NC_DPMUX_SAK_20	NC_DPMUX_SAK_20	MAKE_BASE=TRUE	NO_TEST=1
34	IN	NC_DPMUX_SAK_19	NC_DPMUX_SAK_19	MAKE_BASE=TRUE	NO_TEST=1
34	IN	NC_DPMUX_SAK_18	NC_DPMUX_SAK_18	MAKE_BASE=TRUE	NO_TEST=1
34	IN	NC_DPMUX_SAK_17	NC_DPMUX_SAK_17	MAKE_BASE=TRUE	NO_TEST=1
34	IN	NC_DPMUX_SAK_16	NC_DPMUX_SAK_16	MAKE_BASE=TRUE	NO_TEST=1
34	IN	NC_DPMUX_SAK_15	NC_DPMUX_SAK_15	MAKE_BASE=TRUE	NO_TEST=1
34	IN	NC_DPMUX_SAK_14	NC_DPMUX_SAK_14	MAKE_BASE=TRUE	NO_TEST=1

UNUSED TP ALIASES

6	IN	NC_CPU_RSVD_BB69	NC_CPU_RSVD_BB69	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_RSVD_BB68	NC_CPU_RSVD_BB68	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_RSVD_BA70	NC_CPU_RSVD_BA70	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_RSVD_BA68	NC_CPU_RSVD_BA68	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_RSVD_AW71	NC_CPU_RSVD_AW71	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_RSVD_AW70	NC_CPU_RSVD_AW70	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_RSVD_AK13	NC_CPU_RSVD_AK13	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_RSVD_AK12	NC_CPU_RSVD_AK12	MAKE_BASE=TRUE	NO_TEST=1
9	IN	NC_CPU_NCTFVSS_C1	NC_CPU_NCTFVSS_C1	MAKE_BASE=TRUE	NO_TEST=1
9	IN	NC_CPU_NCTFVSS_BB70	NC_CPU_NCTFVSS_BB70	MAKE_BASE=TRUE	NO_TEST=1
9	IN	NC_CPU_NCTFVSS_BA71	NC_CPU_NCTFVSS_BA71	MAKE_BASE=TRUE	NO_TEST=1
9	IN	NC_CPU_NCTFVSS_BA1	NC_CPU_NCTFVSS_BA1	MAKE_BASE=TRUE	NO_TEST=1
9	IN	NC_CPU_NCTFVSS_B71	NC_CPU_NCTFVSS_B71	MAKE_BASE=TRUE	NO_TEST=1
9	IN	NC_CPU_NCTFVSS_AV1	NC_CPU_NCTFVSS_AV1	MAKE_BASE=TRUE	NO_TEST=1
9	IN	NC_CPU_NCTFVSS_A70	NC_CPU_NCTFVSS_A70	MAKE_BASE=TRUE	NO_TEST=1
9	IN	NC_CPU_NCTFVSS_A5	NC_CPU_NCTFVSS_A5	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_BB5	NC_CPU_BB5	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_BB3	NC_CPU_BB3	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_AY4	NC_CPU_AY4	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_AU5	NC_CPU_AU5	MAKE_BASE=TRUE	NO_TEST=1
6	IN	NC_CPU_AT5	NC_CPU_AT5	MAKE_BASE=TRUE	NO_TEST=1
73	IN	NC_CPU_MSM_L	NC_CPU_MSM_L	MAKE_BASE=TRUE	NO_TEST=1
28	IN	NC_USBC_XA_RESET_L	NC_USBC_XA_RESET_L	MAKE_BASE=TRUE	NO_TEST=1
94	IN	NC_USBC_TB_RESET_L	NC_USBC_TB_RESET_L	MAKE_BASE=TRUE	NO_TEST=1

UNUSED SIGNALS

14	NC_PCH_SLP_WLAN_L	TRUE	NC_PCH_SLP_WLAN_L		105
102 13	NC_SPI_CS1_L	TRUE	NC_SPI_CS1_L		102 105
102 13	NC_SPI_CS2_L	TRUE	NC_SPI_CS2_L		102 105
102 13	NC_SPI_CS1_L	TRUE	NC_SPI_CS1_L		102 105
102 13	NC_SPI_CS2_L	TRUE	NC_SPI_CS2_L		102 105
15	NC_PCIE_CAMERA_D2R_N		NC_PCIE_CAMERA_D2R_N	TRUE	105
15	NC_PCIE_CAMERA_D2R_P		NC_PCIE_CAMERA_D2R_P	TRUE	105
15	NC_PCIE_CAMERA_R2D_C_N		NC_PCIE_CAMERA_R2D_C_N	TRUE	105
15	NC_PCIE_CAMERA_R2D_C_P		NC_PCIE_CAMERA_R2D_C_P	TRUE	105
15	NC_PCIE_CLK100M_CAMERA_N		NC_PCIE_CLK100M_CAMERA_N	105 TRUE	
15	NC_PCIE_CLK100M_CAMERA_P		NC_PCIE_CLK100M_CAMERA_P	105 TRUE	
15	NC_USB_EXTA_N		NC_USB_EXTA_N	TRUE	
15	NC_USB_EXTA_P		NC_USB_EXTA_P	NO_TEST=1 TRUE	
15	NC_USB_EXTB_N		NC_USB_EXTB_N	TRUE	
15	NC_USB_EXTB_P		NC_USB_EXTB_P	NO_TEST=1 TRUE	
6	NC_XDP_BPM_L<1>		NC_XDP_BPM_L<1>	TRUE	
6	NC_XDP_BPM_L<2>		NC_XDP_BPM_L<2>	NO_TEST=1 TRUE	
6	NC_XDP_BPM_L<3>		NC_XDP_BPM_L<3>	NO_TEST=1 TRUE	
15	NC_USB3_EXTB_D2R_N		NC_USB3_EXTB_D2R_N	NO_TEST=1 TRUE	
15	NC_USB3_EXTB_D2R_P		NC_USB3_EXTB_D2R_P	NO_TEST=1 TRUE	
15	NC_USB3_EXTB_R2D_C_N		NC_USB3_EXTB_R2D_C_N	NO_TEST=1 TRUE	
15	NC_USB3_EXTB_R2D_C_P		NC_USB3_EXTB_R2D_C_P	NO_TEST=1 TRUE	

UNUSED SIGNAL ALIAS

86	IN	NC_ANI0_NCE4	NC_ANI0_NCE4	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI0_NCE5	NC_ANI0_NCE5	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI0_NCE6	NC_ANI0_NCE6	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI0_NCE7	NC_ANI0_NCE7	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI1_NCE4	NC_ANI1_NCE4	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI1_NCE5	NC_ANI1_NCE5	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI1_NCE6	NC_ANI1_NCE6	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI1_NCE7	NC_ANI1_NCE7	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI2_NCE4	NC_ANI2_NCE4	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI2_NCE5	NC_ANI2_NCE5	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI2_NCE6	NC_ANI2_NCE6	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI2_NCE7	NC_ANI2_NCE7	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI3_NCE4	NC_ANI3_NCE4	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI3_NCE5	NC_ANI3_NCE5	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI3_NCE6	NC_ANI3_NCE6	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI3_NCE7	NC_ANI3_NCE7	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI4_NCE4	NC_ANI4_NCE4	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI4_NCE5	NC_ANI4_NCE5	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI4_NCE6	NC_ANI4_NCE6	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI4_NCE7	NC_ANI4_NCE7	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI5_NCE4	NC_ANI5_NCE4	MAKE_BASE=TRUE	NO_TEST=1
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87	IN	NC_ANI5_NCE6	NC_ANI5_NCE6	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI5_NCE7	NC_ANI5_NCE7	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI6_NCE4	NC_ANI6_NCE4	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI6_NCE5	NC_ANI6_NCE5	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI6_NCE6	NC_ANI6_NCE6	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI6_NCE7	NC_ANI6_NCE7	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI7_NCE4	NC_ANI7_NCE4	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI7_NCE5	NC_ANI7_NCE5	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI7_NCE6	NC_ANI7_NCE6	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI7_NCE7	NC_ANI7_NCE7	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI1_RNB	NC_ANI1_RNB	MAKE_BASE=TRUE	NO_TEST=1
86	IN	NC_ANI3_RNB	NC_ANI3_RNB	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI5_RNB	NC_ANI5_RNB	MAKE_BASE=TRUE	NO_TEST=1
87	IN	NC_ANI7_RNB	NC_ANI7_RNB	MAKE_BASE=TRUE	NO_TEST=1
81		NC_S3X_GPIO1	NC_S3X_GPIO1	MAKE_BASE=TRUE	NO_TEST=1
81		NC_S3X_BOOTSTRAP6	NC_S3X_BOOTSTRAP6	MAKE_BASE=TRUE	NO_TEST=1
81		NC_S3X_BOOTSTRAP1	NC_S3X_BOOTSTRAP1	MAKE_BASE=TRUE	NO_TEST=1

S3X Aliasing

19	SSD_CLKREQ_L	MAKE_BASE=TRUE	SSD_CLKREQ_L	91
14	SSD_SR_EN_L	MAKE_BASE=TRUE	SSD_SR_EN_L	91 104

EPD PANEL

79	I2C_BKLT_SCL	MAKE_BASE	TRUE	I2C_BKLT_SCL	80 104
79	I2C_BKLT_SDA		TRUE	I2C_BKLT_SDA	80 104

SYNC_MASTER=SHART_J44 SYNC_DATE=11/19/2012

PAGE TITLE

Signal Aliases

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 122 OF 145

SHEET 102 OF 119

Memory Bit & Byte Swizzle

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SYNC_MASTER=AHARTMAN_J52 SYNC_DATE=10/29/2013

PAGE TITLE

LPDDR3 Bit & Byte Swizzle

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 123 OF 145

SHEET 103 OF 119

Functional Test Points

J4401 - DFR Display Connector

104 42 38	IN	DFR_DISP_VSYNC	
42 38	IN	DFR_DISP_TE	FUNC_TEST=TRUE
42 38	IN	DFR_DISP_INT	FUNC_TEST=TRUE
42	IN	DFR_DISP_RESET_L	FUNC_TEST=TRUE
42	IN	PP3V3_S0SW_DFR	FUNC_TEST=TRUE 3 TPs
105 42	IN	MIPID_CLK_CONN_P	FUNC_TEST=TRUE
105 42	IN	MIPID_CLK_CONN_N	FUNC_TEST=TRUE
105 42	IN	MIPID_DATA_CONN_P	FUNC_TEST=TRUE
105 42	IN	MIPID_DATA_CONN_N	FUNC_TEST=TRUE
106 104 42 37	IN	PP1V8_S0SW_DFR	FUNC_TEST=TRUE 2 TPs
42 38 37	IN	DFRDRV_I2C_SCL	FUNC_TEST=TRUE
42 38 37	IN	DFRDRV_I2C_SDA	FUNC_TEST=TRUE
42 38 37	IN	GND	FUNC_TEST=TRUE
			FUNC_TEST=TRUE
		6 TPs	

J4402 - DFR Touch Connector

104 42	IN	DFR_TOUCH_LID	
104 42	IN	DFR_TOUCH_LID	FUNC_TEST=TRUE
42 37	IN	DFR_TOUCH_SPI_CS_L	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_MOSI_R	FUNC_TEST=TRUE
42 38 37	IN	DFR_TOUCH_ROM_I2C_SCL	FUNC_TEST=TRUE
42 38 37	IN	DFR_TOUCH_ROM_I2C_SDA	FUNC_TEST=TRUE
42 37	IN	DFR_TOUCH_RESET_L	FUNC_TEST=TRUE
106 104 42 37	IN	PP1V8_S0SW_DFR	FUNC_TEST=TRUE 2 TPs
101 42	IN	PP5V_S0_T139	FUNC_TEST=TRUE 1 TPs
42 38	IN	DFR_TOUCH_PANEL_DETECT	FUNC_TEST=TRUE
104 42 38	IN	DFR_DISP_VSYNC	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_MISO_R	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_CLK_R	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_INT_L	FUNC_TEST=TRUE
42 38	IN	DFR_CLKIN_RESET_L	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_ROM_WC	FUNC_TEST=TRUE
106 104 42 37	IN	PP1V8_S0SW_DFR	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		6 TPs	FUNC_TEST=TRUE

J4500 - Keyboard Connector

43	IN	PP5V_S0_FAN_CONN	FUNC_TEST=TRUE 8 TPs
43	IN	GND_FAN	FUNC_TEST=TRUE 8 TPs
58 43	IN	FAN_LT_TACH	FUNC_TEST=TRUE
58 43	IN	FAN_LT_PWM	FUNC_TEST=TRUE
58 43	IN	FAN_RT_TACH	FUNC_TEST=TRUE
58 43	IN	FAN_RT_PWM	FUNC_TEST=TRUE
101 43	IN	PP5V_S0_KBD	FUNC_TEST=TRUE
100 50 43	IN	PP3V3_G3H	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
101 43	IN	PP3V3_S4	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_XBLANK	FUNC_TEST=TRUE
104 43	IN	KBD_I2C_SDA	FUNC_TEST=TRUE
104 43	IN	KBD_INT_L	FUNC_TEST=TRUE
104 43	IN	KBD_I2C_SCL	FUNC_TEST=TRUE
50 43	IN	SMC_LSOC_RST_L	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		6 TPs	FUNC_TEST=TRUE

J4501 - Trackpad Connector

104 43	IN	KBD_I2C_SCL	
104 43	IN	KBD_I2C_SDA	FUNC_TEST=TRUE
104 43	IN	KBD_INT_L	FUNC_TEST=TRUE
51 43	IN	SMBUS_SMC_3_SDA	FUNC_TEST=TRUE
51 43	IN	SMBUS_SMC_3_SCL	FUNC_TEST=TRUE
101 43	IN	PP3V3_S4_TPAD	FUNC_TEST=TRUE
101	IN	PP3V3_S4_TPAD	FUNC_TEST=TRUE
43	IN	PP5V_S4_TPAD_CONN	FUNC_TEST=TRUE
43	IN	ACT_GND	FUNC_TEST=TRUE
43	IN	PPVIN_S4_TPAD_FUSE	FUNC_TEST=TRUE
43	IN	TPAD_SPI_CLK_R	FUNC_TEST=TRUE
43	IN	TPAD_SPI_IF_EN_CONN	FUNC_TEST=TRUE
43	IN	TPAD_SPI_MISO_R	FUNC_TEST=TRUE
43	IN	TPAD_SPI_CS_CONN_R_L	FUNC_TEST=TRUE
43	IN	TPAD_SPI_MOSI_R	FUNC_TEST=TRUE
43	IN	TPAD_SPI_INT_CONN_L	FUNC_TEST=TRUE
50 43	IN	SMC_ACTUATOR_DISABLE_L	FUNC_TEST=TRUE
50 43	IN	SMC_PME_S4_WAKE_L	FUNC_TEST=TRUE
49 43 42 50	IN	SMC_LID	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
104 43	IN	KBD_BLC_XBLANK	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		6 TPs	FUNC_TEST=TRUE

J4900 - Mesa Connector

47	IN	PP3V0_MESA	2 TPs
	IN	MESA_SPI_MISO_CONN	FUNC_TEST=TRUE
47	IN	MESA_SNSR_INT_CONN	FUNC_TEST=TRUE
47	IN	MESA_BOOST_EN_CONN	FUNC_TEST=TRUE
47 37	IN	MESA_I2C_SDA	FUNC_TEST=TRUE
47 37	IN	MESA_I2C_SCL	FUNC_TEST=TRUE
47	IN	ESD_GND	FUNC_TEST=TRUE 1 TPs
47	IN	PP1V8_MESA	FUNC_TEST=TRUE 1 TPs
47	IN	MESA_SPI_MOSI_CONN	FUNC_TEST=TRUE
47	IN	MENU_KEY_L	FUNC_TEST=TRUE
47	IN	MESA_SPI_CLK_CONN	FUNC_TEST=TRUE
47	IN	PP16V0_MESA	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE 1 TPs
		2 TPs	FUNC_TEST=TRUE

J6200 - MIC Connector

60	IN	DMIC1_DATA	
60	IN	DMIC1_CLK	FUNC_TEST=TRUE
	IN	PP1V8_S0	FUNC_TEST=TRUE 1 TPs
60	IN	DMIC2_DATA	FUNC_TEST=TRUE
60	IN	DMIC2_CLK	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	FUNC_TEST=TRUE

J6410 - Left Tweeter Connector

62	IN	SPKRCONN_TL_OUT_P	FUNC_TEST=TRUE 2 TPs
62	IN	SPKRCONN_TL_OUT_N	FUNC_TEST=TRUE 1 TPs
62 60	IN	8409_SPKR_ID0	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	FUNC_TEST=TRUE

J6430 - Left Woofer Connector

62	IN	SPKRCONN_WL_OUT_P	FUNC_TEST=TRUE
62	IN	SPKRCONN_WL_OUT_N	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	FUNC_TEST=TRUE

J6500 - Right Tweeter Connector

8 TPs 63	IN	SPKRCONN_TR_OUT_P	FUNC_TEST=TRUE
8 TPs 63	IN	SPKRCONN_TR_OUT_N	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		2 TPs	FUNC_TEST=TRUE

J6550 - Right Woofer Connector

3 TPs 63	IN	SPKRCONN_WR_OUT_P	FUNC_TEST=TRUE
1 TPs 63	IN	SPKRCONN_WR_OUT_N	FUNC_TEST=TRUE
1 TPs		GND	FUNC_TEST=TRUE
		2 TPs	FUNC_TEST=TRUE

J6600 - Audio Jack Connector

104 64	IN	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE
104 64	IN	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE
104 64	IN	AUD_CONN_RING2	FUNC_TEST=TRUE
104 64	IN	AUD_CONN_SLEEVE	FUNC_TEST=TRUE
64	IN	AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE
	IN	AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE
64	IN	AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE
64	IN	AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE
64	IN	AUD_CONN_RING2_XW	FUNC_TEST=TRUE
104 64	IN	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE
104 64	IN	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE
104 64	IN	AUD_CONN_RING2	FUNC_TEST=TRUE 2 TPs
104 64	IN	AUD_CONN_SLEEVE	FUNC_TEST=TRUE 1 TPs
		GND	FUNC_TEST=TRUE 1 TPs
		4 TPs	FUNC_TEST=TRUE 8 TPs
			8 TPs

J6950 - Battery Connector

66 65	IN	PPVBAT_G3H_CONN	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		8 TPs	

J6951 - Battery Sense Connector

65	IN	SYS_DETECT_L	
65 51	IN	SMBUS_SMC_5_G3_SCL	FUNC_TEST=TRUE
65 51	IN	SMBUS_SMC_5_G3_SDA	FUNC_TEST=TRUE
65 54	IN	BMON_IOUT	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		1 TPs	FUNC_TEST=TRUE

J8500 - eDP Connector

80 79	IN	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE
80 38 37	IN	I2C_CAM_SDA	FUNC_TEST=TRUE
80 38 37	IN	I2C_CAM_SCL	FUNC_TEST=TRUE
80 42	IN	I2C_ALS_SCL	FUNC_TEST=TRUE
80 42	IN	I2C_ALS_SDA	FUNC_TEST=TRUE
80 51	IN	SMBUS_SMC_0_S0_SCL	FUNC_TEST=TRUE
80 51	IN	SMBUS_SMC_0_S0_SDA	FUNC_TEST=TRUE
102 80	IN	I2C_BKLT_SCL	FUNC_TEST=TRUE
102 80	IN	I2C_BKLT_SDA	FUNC_TEST=TRUE
80 5	IN	BKLT_PWM_MLB2TCON	FUNC_TEST=TRUE
80 48	IN	BKLT_PWM_TCON2MLB	FUNC_TEST=TRUE
80 16	IN	LCD_IRQ_L	FUNC_TEST=TRUE
80 5	IN	DP_INT_HPD	FUNC_TEST=TRUE
80	IN	BUF_EDP_PANEL_PWR_EN	FUNC_TEST=TRUE
106 80	IN	PP3V3_S0SW_LCD	FUNC_TEST=TRUE 7 TPs
106 80	IN	PP5V_S0SW_LCD	FUNC_TEST=TRUE 1 TPs
106 80 38	IN	PP5V_S0_ALSCAM_F	FUNC_TEST=TRUE
105 80 38	IN	MIPI_CLK_CONN_P	FUNC_TEST=TRUE
105 80 38	IN	MIPI_CLK_CONN_N	FUNC_TEST=TRUE
105 80 38	IN	MIPI_DATA_CONN_P	FUNC_TEST=TRUE
105 80 38	IN	MIPI_DATA_CONN_N	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_P<3>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_N<3>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_P<2>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_N<2>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_P<1>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_N<1>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_P<0>	FUNC_TEST=TRUE
80	IN	EDP_INT_ML_N<0>	FUNC_TEST=TRUE
80	IN	EDP_INT_AUX_P	FUNC_TEST=TRUE
80	IN	EDP_INT_AUX_N	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		8 TPs	FUNC_TEST=TRUE

Probe Block Grid - WiPass and NAND Rack

15	IN	TP_USB_TESTERN	FUNC_TEST=TRUE
15	IN	TP_USB_TESTERP	FUNC_TEST=TRUE
15	IN	TP_USB3_03_D2RN	FUNC_TEST=TRUE
15	IN	TP_USB3_03_D2RP	FUNC_TEST=TRUE
15	IN	TP_USB3_03_R2DN	FUNC_TEST=TRUE
15	IN	TP_USB3_03_R2DP	FUNC_TEST=TRUE
	IN	SMC_DEBUGPRT_RX_L	FUNC_TEST=TRUE
49 48 28	IN	SMC_DEBUGPRT_TX_L	FUNC_TEST=TRUE
91 19 16	IN	SSD_RESET_L	FUNC_TEST=TRUE
91 84	IN	STORAGE_EN	FUNC_TEST=TRUE
102 91	IN	SSD_SR_EN_L	FUNC_TEST=TRUE
91 14	IN	SSD_BOOT_L	FUNC_TEST=TRUE
88 84	IN	SSD_DBG_UART_R2D	FUNC_TEST=TRUE
88 84 19	IN	SSD_DBG_UART_D2R	FUNC_TEST=TRUE
	IN	SSD_PWR_EN_L	FUNC_TEST=TRUE
84 81	IN	S3X_JTAG_SEL	FUNC_TEST=TRUE
94 84 81	IN	S3X_JTAG_TCK	FUNC_TEST=TRUE
84 81	IN	S3X_JTAG_TDI	FUNC_TEST=TRUE
84 81	IN	S3X_JTAG_TDO	FUNC_TEST=TRUE
94 84 81	IN	S3X_JTAG_TMS	FUNC_TEST=TRUE
84 81	IN	S3X_JTAG_TRST_L	FUNC_TEST=TRUE
88 87 86 85 84 82 81 19	IN	PP1V8_SSD_COLD	FUNC_TEST=TRUE
	IN	PPDCIN_G3H_CHGR	FUNC_TEST=TRUE
66	IN	PPVBAT_G3H_CHGR_REG	FUNC_TEST=TRUE
4 TPs 100 54 8	IN	PPVCC_S0_CPU	FUNC_TEST=TRUE
4 TPs 88 82	IN	PP0V9_SSD_REG	FUNC_TEST=TRUE
50 49 48 47	IN	SMC_ONOFF_L	FUNC_TEST=TRUE
50	IN	TP_SMC_DEV_SUPPLY_L	FUNC_TEST=TRUE
73 48 14	IN	PM_PCH_SYS_PWROK	FUNC_TEST=TRUE
101 72	IN	PP5V_S4	FUNC_TEST=TRUE
100 66	IN	PPDCIN_G3H	FUNC_TEST=TRUE
104 92 80 77 74 73 48 26 19 14	IN	PM_SLP_S3_L	FUNC_TEST=TRUE
35 19 14	IN	PLT_RST_L	FUNC_TEST=TRUE
100 65	IN	PP3V3_G3H	FUNC_TEST=TRUE
66	IN	HPWR_EN_L	FUNC_TEST=TRUE
80 66 59 50	IN	SMC_RESET_L	FUNC_TEST=TRUE
		GND	FUNC_TEST=TRUE
		3 TPs; 1x for USB2 pair, 1x for USB3 R2D, 1x for USB3 D2R	

Debug LEDs

77 48 19 14	IN	PM_SLP_S5_L	FUNC_TEST=TRUE
8 TPs 77 74 48 43 19 14	IN	PM_SLP_S4_L	FUNC_TEST=TRUE
104 92 80 77 74 73 48 26 19 14	IN	PM_SLP_S3_L	FUNC_TEST=TRUE
74 48 19 14	IN	PM_SLP_S0_L	FUNC_TEST=TRUE
	IN	PM_SLP_SUS_L	FUNC_TEST=TRUE

J3300 - Left USB-C Connector

31	IN	PP20V_USBC_XA_VBUS_CONN	FUNC_TEST=TRUE
		4 TPs	
31	IN	PP20V_USBC_XB_VBUS_CONN	FUNC_TEST=TRUE
		4 TPs	
31 29 28	IN	USBC_XA_CC1	
31 29 28	IN	USBC_XA_CC2	FUNC_TEST=TRUE
31 30 28	IN	USBC_XB_CC1	FUNC_TEST=TRUE
31 30 28	IN	USBC_XB_CC2	FUNC_TEST=TRUE
31	IN	TP_USBC_PP20V_XB	FUNC_TEST=TRUE
			FUNC_TEST=TRUE
		GND	
		4 TPs	FUNC_TEST=TRUE

JB500 - Right USB-C Connector

97	IN	PP20V_USBC_TA_VBUS_CONN	FUNC_TEST=TRUE
		4 TPs	
97	IN	PP20V_USBC_TB_VBUS_CONN	FUNC_TEST=TRUE
		4 TPs	
97 95 94	IN	USBC_TA_CC1	
97 95 94	IN	USBC_TA_CC2	FUNC_TEST=TRUE
97 96 94	IN	USBC_TB_CC1	FUNC_TEST=TRUE
97 96 94	IN	USBC_TB_CC2	FUNC_TEST=TRUE
97	IN	TP_USBC_PP20V_TB	FUNC_TEST=TRUE
97	IN	TP_USBC_PP20V_TA	FUNC_TEST=TRUE
			FUNC_TEST=TRUE
		GND	
		4 TPs	FUNC_TEST=TRUE

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=12/18/2012

PAGE TITLE

ICT FCT 1

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 124 OF 145

SHEET 104 OF 119

DP_DDI1_ML_C_N<0> OUT → PP9901
DP_DDI1_ML_C_P<0> OUT → PP9902
DP_DDI2_ML_C_N<0> OUT → PP9903
DP_DDI2_ML_C_P<0> OUT → PP9904
SMC_PECI_L IN → PP9918
PCIE_SSD_D2R_N<0> IN → PP9910
PCIE_SSD_D2R_P<0> IN → PP9911

MIPIC_DATA_P → PP9949
MIPIC_DATA_N → PP9950
MIPIC_CLK_P → PP9951
MIPIC_CLK_N → PP9952

PCIE_TBT_X_D2R_N<0> IN → PP9919
PCIE_TBT_X_D2R_P<0> IN → PP9920

PCIE_TBT_T_D2R_N<0> IN → PP9927
PCIE_TBT_T_D2R_P<0> IN → PP9928

MIPID_DATA_CONN_P → B1
MIPID_DATA_CONN_N → B1
MIPID_CLK_CONN_P → OUT
MIPID_CLK_CONN_N → OUT

MIPI_DATA_CONN_P → B1
MIPI_DATA_CONN_N → B1
MIPI_CLK_CONN_P → OUT
MIPI_CLK_CONN_N → OUT

PP9933 USB_CAMERA_DFR_N → BT
PP9934 USB_CAMERA_DFR_P → BT

NO_TESTs

NC_PCH_SLP_WLAN_L — NO_TEST=1
NC_SPI_CS1_L — NO_TEST=1
NC_SPI_CS2_L — NO_TEST=1
NC_SPI_CS1_L — NO_TEST=1
NC_SPI_CS2_L — NO_TEST=1
NC_PCIE_CAMERA_D2R_N — NO_TEST=1
NC_PCIE_CAMERA_D2R_P — NO_TEST=1
NC_PCIE_CAMERA_R2D_C_N — NO_TEST=1
NC_PCIE_CAMERA_R2D_C_P — NO_TEST=1
NC_PCIE_CLK100M_CAMERA_N — NO_TEST=1
NC_PCIE_CLK100M_CAMERA_P — NO_TEST=1
NC_PICCOLO_VEN2 — NO_TEST=1

NC_PCIE_TBT_T_D2R_C_P<2>
NC_PCIE_TBT_T_D2R_C_N<2>
NC_PCIE_TBT_T_D2R_C_P<3>
NC_PCIE_TBT_T_D2R_C_N<3>
NC_PCIE_TBT_T_R2D_P<2>
NC_PCIE_TBT_T_R2D_N<2>
NC_PCIE_TBT_T_R2D_P<3>
NC_PCIE_TBT_T_R2D_N<3>

High Speed NO_TEST

PCIE_SSD_R2D_C_P<3..0>
PCIE_SSD_R2D_C_N<3..0> TRUE
PCIE_SSD_D2R_P<3..0> TRUE
PCIE_SSD_D2R_N<3..0> TRUE

Unused nets with offpage

(Nets with offpages not used on this project)

BT_PWRRST_L

PCIE_CLK100M_SSD_LB_N → PP9941
PCIE_CLK100M_SSD_LB_P → PP9942
PCIE_CLK100M_TBT_X_N → PP9943
PCIE_CLK100M_TBT_X_P → PP9944
PCIE_CLK100M_TBT_T_N → PP9945
PCIE_CLK100M_TBT_T_P → PP9946
PCIE_CLK100M_AP_N → PP9947
PCIE_CLK100M_AP_P → PP9948

XDP_USB_EXTA_OC_L → PP9801
XDP_USB_EXTB_OC_L → PP9802
XDP_USB_EXTC_OC_L → PP9803
XDP_USB_EXTD_OC_L → PP9804
HDA_SDIN0 → PP9808
PLACE_NEAR=U0500.BA21:6MM
LPC_CLK24M_SMC → PP9819

XDP_BPM_L<0> → TP9820 (TP-P5)

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=12/18/2012

PAGE TITLE: ICT FCT 2

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0
PAGE 125 OF 145
SHEET 105 OF 119

PP5V_S0
- CC700 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC701 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC702 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC703 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP1V8_S0SW_DFR
- CC704 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC705 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC706 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V3_G3H
- CC707 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V3_S4
- CC708 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC709 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC710 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V3_S4_BT
- CC711 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V3_S4
- CC712 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC713 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP1V8_S0
- CC714 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V3_S0
- CC715 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC716 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC717 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC718 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC745 12PF 5% 25V NP0-C0G 0201
- CC746 12PF 5% 25V NP0-C0G 0201
- CC747 12PF 5% 25V NP0-C0G 0201
- CC748 12PF 5% 25V NP0-C0G 0201

PP3V3_S0
- CC719 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC720 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC721 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC722 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC723 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V3_S0
- CC724 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC725 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC726 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP5V_S0_ALSCAM_F
- CC727 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V3_S0SW_LCD
- CC728 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP5V_S0SW_LCD
- CC729 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V3_S4
- CC730 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC731 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC732 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC733 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC734 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP5V_S0
- CC735 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC736 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC737 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC738 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC739 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP1V8_S0
- CC740 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC741 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC742 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP3V3_S4_WLAN_SW
- CC743 3.0PF +/-0.1PF 25V NP0-C0G 0201
- CC744 3.0PF +/-0.1PF 25V NP0-C0G 0201

TP_DPMUX_SAK_6
- CC749 12PF 5% 25V NP0-C0G 0201

TP_DPMUX_SAK_13
- CC750 12PF 5% 25V NP0-C0G 0201

DDI1_MUX_SEL
- CC751 12PF 5% 25V NP0-C0G 0201
- CC752 12PF 5% 25V NP0-C0G 0201
- CC753 12PF 5% 25V NP0-C0G 0201

DDI2_MUX_SEL
- CC754 12PF 5% 25V NP0-C0G 0201
- CC755 12PF 5% 25V NP0-C0G 0201

BOM_COST_GROUP=WIRELESS

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE: Desense Capacitors

Apple Inc.

DRAWING NUMBER: 051-00777 SIZE: D
REVISION: 9.0.0
BRANCH: dvt-fab09-0
PAGE: 127 OF 145
SHEET: 106 OF 119

SYNC_MASTER=J79_RIO SYNC_DATE=06/18/2015

PAGE TITLE

Empty

Apple Inc.

DRAWING NUMBER 051-00777

SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 129 OF 145

SHEET 107 OF 119

J79 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=12/14/2012

PAGE TITLE

PCB Rule Definitions

Apple Inc.

DRAWING NUMBER 051-00777

SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 130 OF 145

SHEET 108 OF 119

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_08MIL	*	0.203 MM	?
CPU_12MIL	*	0.305 MM	?
CPU_18MIL	*	0.457 MM	?
CPU_25MIL	*	0.635 MM	?

CPU Signal Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/13/2013

PAGE TITLE

CPU Constraints

Apple Inc.

DRAWING NUMBER 051-00777

SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 131 OF 145

SHEET 109 OF 119

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
PCH_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_12MIL	*	0.305 MM	?
PCH_15MIL	*	0.381 MM	?
PCH_18MIL	*	0.457 MM	?
PCH_20MIL	*	0.508 MM	?

PCH Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/08/2013

PAGE TITLE

PCH Constraints

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 132 OF 145

SHEET 110 OF 119

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_75D	*	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF
MEM_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=4x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=6x_DIELECTRIC	?
MEM_CMD2CMD	*	=6x_DIELECTRIC	?
MEM_CMD2CTL	*	=6x_DIELECTRIC	?
MEM_CTL2CTL	*	=6x_DIELECTRIC	?
MEM_CLK2CLK	*	=12x_DIELECTRIC	?
MEM_DATA2OTHERMEM	*	=16x_DIELECTRIC	?
MEM_2OTHERMEM	*	=8x_DIELECTRIC	?
MEM_2PWR	*	=4x_DIELECTRIC	?
MEM_2GND	*	=4x_DIELECTRIC	?
MEM_2OTHER	*	=12x_DIELECTRIC	?
MEM_12MIL	*	0.305 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CMD2CTL	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CTL2CTL	TOP,BOTTOM	=10x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=16x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=16x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=20x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF_B	*	=1.5x_DIELECTRIC	?
MEM_DQS2OWNDATA_B	*	=1.5x_DIELECTRIC	?
MEM_CMD2CMD_B	*	=1.5x_DIELECTRIC	?
MEM_CMD2CTL_B	*	=1.5x_DIELECTRIC	?
MEM_CTL2CTL_B	*	=1.5x_DIELECTRIC	?
MEM_CLK2CLK_B	*	=1.5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2OTHERMEM_B	*	=1.5x_DIELECTRIC	?
MEM_2OTHERMEM_B	*	=1.5x_DIELECTRIC	?
MEM_2OTHER_B	*	=1.5x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	*	BGA_MEM	MEM_2OTHER_B
MEM_*_DQS_*	*	BGA_MEM	MEM_2OTHER_B
MEM_CMD	*	BGA_MEM	MEM_2OTHER_B
MEM_CTL	*	BGA_MEM	MEM_2OTHER_B
MEM_CLK	*	BGA_MEM	MEM_2OTHER_B
MEM_*	MEM_*	BGA_MEM	MEM_2OTHERMEM_B

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	=SAME	BGA_MEM	MEM_DATA2SELF_B

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	MEM_*	*	MEM_DATA2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DQBYTE_*	MEM_*	BGA_MEM	MEM_DATA2OTHERMEM_B

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTL	*	MEM_CMD2CTL
MEM_CTL	MEM_CTL	*	MEM_CTL2CTL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	BGA_MEM	MEM_CMD2CMD_B
MEM_CMD	MEM_CTL	BGA_MEM	MEM_CMD2CTL_B
MEM_CTL	MEM_CTL	BGA_MEM	MEM_CTL2CTL_B
MEM_CLK	MEM_CLK	BGA_MEM	MEM_CLK2CLK_B

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DQBYTE_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DQBYTE_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DQBYTE_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DQBYTE_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DQBYTE_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DQBYTE_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DQBYTE_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DQBYTE_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DQBYTE_7	*	MEM_DQS2OWNDATA

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DQBYTE_0	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_1	MEM_A_DQBYTE_1	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_2	MEM_A_DQBYTE_2	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_3	MEM_A_DQBYTE_3	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_4	MEM_A_DQBYTE_4	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_5	MEM_A_DQBYTE_5	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_6	MEM_A_DQBYTE_6	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_A_DQS_7	MEM_A_DQBYTE_7	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_0	MEM_B_DQBYTE_0	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_1	MEM_B_DQBYTE_1	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_2	MEM_B_DQBYTE_2	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_3	MEM_B_DQBYTE_3	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_4	MEM_B_DQBYTE_4	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_5	MEM_B_DQBYTE_5	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_6	MEM_B_DQBYTE_6	BGA_MEM	MEM_DQS2OWNDATA_B
MEM_B_DQS_7	MEM_B_DQBYTE_7	BGA_MEM	MEM_DQS2OWNDATA_B

Memory Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_70D	BGA_MEM	MEM_80D
MEM_40S	BGA_MEM	MEM_45S

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/02/2013

PAGE TITLE

Memory Constraints

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 133 OF 145

SHEET 111 OF 119

Thunderbolt, DP, HDMI Constraints

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt & DisplayPort Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	*	*	TBTDP_2OTHER
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_TX	*_RX	*	TBTDP_TXRX
TBTDP_RX	*_TX	*	TBTDP_TXRX

DisplayPort & HDMI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
HDMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

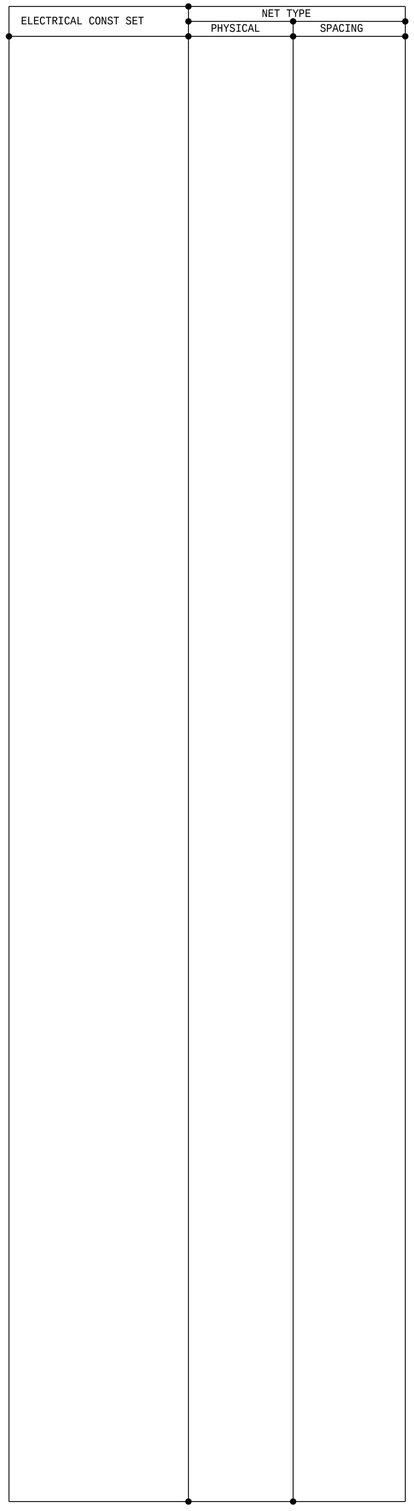
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?
HDMICLK_2DPHDMI	*	=4x_DIELECTRIC	?
HDMIDATA_2SAME	*	=3x_DIELECTRIC	?
HDMIDATA_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DPHDMI	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMIDATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
HDMIDATA_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDMI_DATA	*	*	HDMIDATA_2OTHER
HDMI_DATA	=SAME	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_TX	*	HDMIDATA_2SAME
HDMI_DATA	TBTDP_RX	*	TBTDP_TXRX
HDMI_CLK	*	*	HDMICLK_2OTHER
HDMI_CLK	HDMI_DATA	*	HDMICLK_2DPHDMI
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DPHDMI
HDMI_CLK	TBTDP_TX	*	HDMICLK_2DPHDMI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_2OTHER
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	HDMI_DATA	*	DP_2SAME
DISPLAYPORT	TBTDP_TX	*	DP_2SAME
DISPLAYPORT	TBTDP_RX	*	TBTDP_TXRX

Thunderbolt, DP, HDMI Net Properties



SYNC_MASTER=J79_JACK SYNC_DATE=05/19/2015

PAGE TITLE

TBT DP HDMI Constraints

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 134 OF 145

SHEET 112 OF 119

PCI Express Constraints

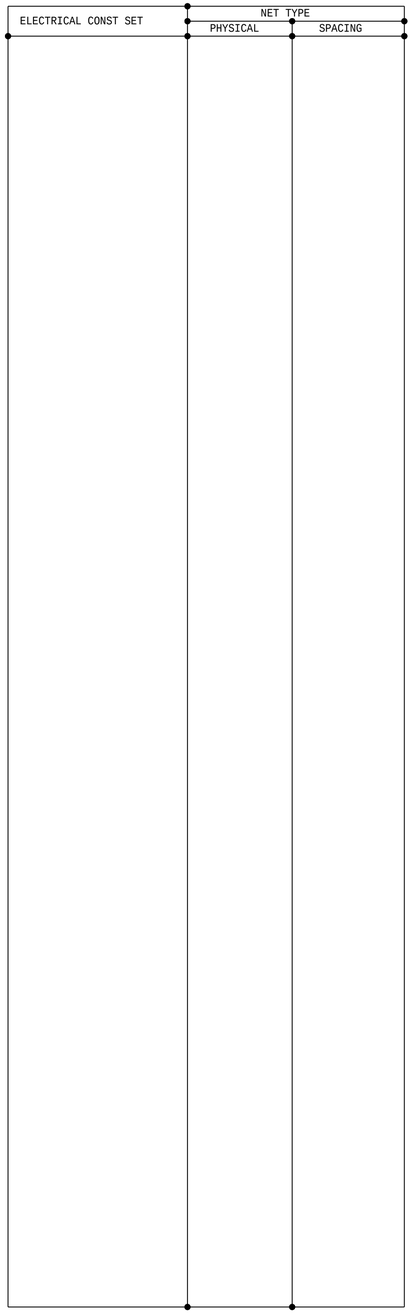
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=3X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER
PCIE_TX	*_RX	*	PCIE_TXRX
PCIE_RX	*_TX	*	PCIE_TXRX

PCI Express Properties



SYNC_MASTER=J79_JACK SYNC_DATE=05/19/2015

PAGE TITLE

PCIe Constraints

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 135 OF 145

SHEET 113 OF 119

USB 2 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?

USB 3 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	*	*	USB3_2OTHER
USB3_*	=SAME	*	USB3_2SAME
USB3_TX	*_RX	*	USB3_TXRX
USB3_RX	*_TX	*	USB3_TXRX

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5x_DIELECTRIC	?

SATA Interface Constraints (Not Used)

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	*	*	SATA_2OTHER
SATA_*	=SAME	*	SATA_2SAME
SATA_TX	*_RX	*	SATA_TXRX
SATA_RX	*_TX	*	SATA_TXRX

USB Constraints

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

SYNC_MASTER=J79_JACK SYNC_DATE=05/21/2015

PAGE TITLE

USB Constraints

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

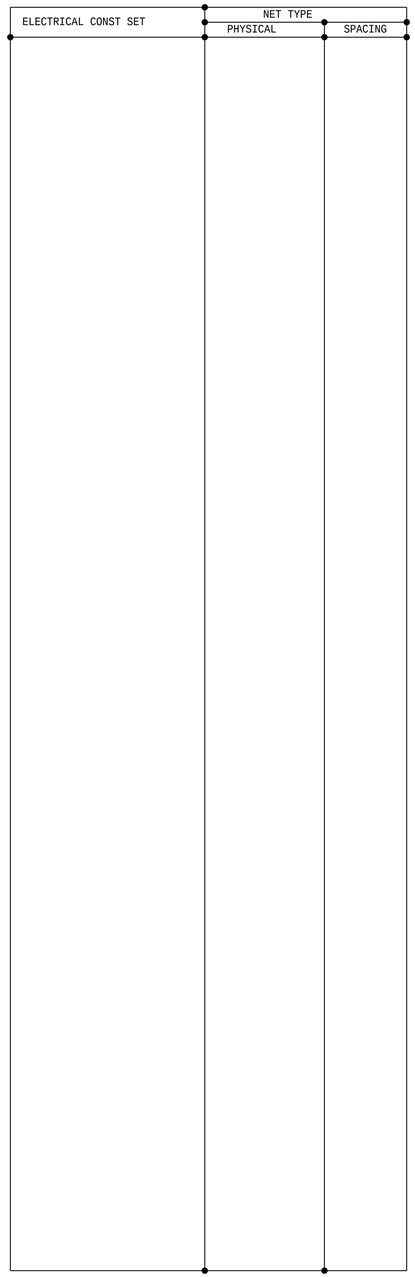
REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 136 OF 145

SHEET 114 OF 119

SMC SMBus & Charger Net Properties



SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/02/2013

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 137 OF 145

SHEET 115 OF 119

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2X_DIELECTRIC	?
S2_CMD2CMD	*	=2X_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4X_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6X_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4X_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/09/2013

PAGE TITLE

Camera Constraints

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 138 OF 145

SHEET 116 OF 119

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
THERM_45S	*	=1TO1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.1 MM	0.1 MM
DIG_AUDIO	*	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	=1TO1_DIFFPAIR	0.1 MM	0.1 MM
ANL_AUDIO	*	=1TO1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
ANL_AUDIO_WIDE	*	=1TO1_DIFFPAIR	0.3 MM	0.3 MM	10 MM	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.070 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.090 MM OVERRIDE	10 MM OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.100 MM	500 MIL		
CPU_27P4S	BOTTOM			0.230 MM	100 MIL		
USB3_85D	TOP			0.100 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

DP, SATA, HDMI, PCIE CONSTRAINT RELAXATIONS

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_85D	BGA	P65_BGA
PCIE_85D	BGA	P65_BGA
CLK_PCIE_85D	BGA	P65_BGA
HDMI_85D	BGA	P65_BGA

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SENSE_45S	*	SENSE_45S
THERM_45S	*	THERM_45S
DIG_AUDIO	*	DIG_AUDIO
ANL_AUDIO	*	ANL_AUDIO

J79 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

J79 Specific Net Properties

ELECTRICAL CONST SET	NET TYPE	
	PHYSICAL	SPACING

SYNC_MASTER=YHARTANTO_J44 SYNC_DATE=01/04/2013

PAGE TITLE

Sensors & Audio Constraints

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D

REVISION 9.0.0

BRANCH dvt-fab09-0

PAGE 139 OF 145

SHEET 117 OF 119

Change List:
<RDAR://COMPONENT/XXXXXX> LOHWILL SCHEMATIC | PROTO 1A

Kismet:
AFP://KISMET.APPLE.COM/KISMET-PROJECTS/LOHWILL

Useful Wiki Links:
Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions
Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design

MobileMac HW Radar:
<rdar://component/XXXXXX> MobileMac HW | Task
<rdar://component/XXXXXX> MobileMac HW | Schematic
<rdar://component/XXXXXX> MobileMac HW | New Bugs
<rdar://component/XXXXXX> MobileMac HW | Layout
<rdar://component/XXXXXX> MobileMac HW | Investigation
<rdar://component/XXXXXX> MobileMac HW | Architecture

Other Info:
Page Allocations - <rdar://problem/19817053> 2015 Schematic Page Allocations
Page Allocations - <rdar://problem/19818112> 2015 Schematic Page Allocations
Page Allocations - <rdar://problem/19818356> 2015 Schematic Page Allocations
Page Allocations - <rdar://problem/19818458> 2015 Schematic Page Allocations

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S00033	107S00034		ALL	
138S0738	138S1101		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
152S00359	152S00253		ALL	Chilisin alt to Cyntec
371S0704	371S00077		ALL	NXP alt to Diodes
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S1106	376S0678		ALL	Fairchild alt to Vishay
740S00027	740S0159		ALL	Bourns alt to Little Fuse
107S0249	107S0251		ALL	
107S00015	107S00011		ALL	
107S00071	107S00053		ALL	
128S0364	128S0264		ALL	Kemet w/ Panasonic
128S0325	128S0397		ALL	
128S00009	128S00007		ALL	
128S00029	128S00007		ALL	
128S00070	128S00007		ALL	
128S00010	128S00011		ALL	
128S00031	128S00011		ALL	
128S00026	128S00011		ALL	
132S00064	132S0409		ALL	
138S0614	138S0578		ALL	
138S0703	138S0648		ALL	
138S00032	138S0831		ALL	
138S00049	138S0831		ALL	
138S0863	138S0853		ALL	
138S0775	138S0860		ALL	
138S00084	138S00060		ALL	
152S00369	152S00268		ALL	Cyntec w/ NEC
155S00188	155S0275		ALL	Murata w/ Taiyo
155S0694	155S0387		ALL	
155S0660	155S0513		ALL	
155S00018	155S0664		ALL	Murata w/ Taiyo
155S00007	155S0667		ALL	

BLC

155S0914	155S0897		ALL	
155S00190	155S0897		ALL	
311S00004	311S0370		ALL	
311S00013	311S0508		ALL	NXP w/ Diodes
353S00107	353S3239		ALL	
353S00525	353S4471		ALL	
372S0186	372S0185		ALL	
376S00014	376S0761		ALL	
376S00086	376S0761		ALL	
376S1080	376S0820		ALL	
376S00074	376S0855		ALL	
376S1089	376S1128		ALL	
740S0144	740S0118		ALL	
740S00028	740S0118		ALL	
740S00003	740S0135		ALL	
998-04070	998-04071		ALL	Hynix alt to SS

T208

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00046	197S00036		ALL	Epson w/ TXC
197S00047	197S00036		ALL	Kyocera w/ TXC
197S00048	197S00036		ALL	Murata w/ TXC
197S00053	197S00050		ALL	Kyocera w/ TXC
197S00054	197S00050		ALL	NDK w/ TXC
197S00055	197S00050		ALL	Murata w/ TXC
311S0596	311S0593		ALL	NXP w/ Diodes
107S0276	107S00020		ALL	Cyntec w/ TFT
107S00021	107S0284		ALL	TFT w/ Yageo
152S00343	152S1682		ALL	NXP w/ Diodes
107S00087	107S00029		ALL	TFT w/ Yageo
128S00058	128S00018		ALL	NEC w/ Rohm
138S0706	138S0739		ALL	NEC w/ Vishay
138S0945	138S0739		ALL	NEC w/ Rohm
152S00358	152S00208		ALL	Murata w/ Chillisin
152S00400	152S00361		ALL	Murata w/ Cyntec
152S1872	152S00361		ALL	Murata w/ Cyntec
155S00034	155S0706		ALL	Taiyo w/ Murata

353S00711	353S2073		ALL	On Semi w/ TI

740S00019	740S00007		ALL	Bourns w/ Polytronics
155S00189	155S0342		ALL	Murata w/ Taiyo
138S0714	138S0713		ALL	Murata w/ Samsung
138S0715	138S0732		ALL	Murata w/ Samsung
107S00086	107S00056		ALL	TFT w/ Cyntec
138S0875	138S0678		ALL	Taiyo w/ Mur&SS
138S0786	138S0705		ALL	Murata w/ Samsung
152S2052	152S1954		ALL	Taiyo w/ Cyntec
152S2015	152S1958		ALL	Taiyo w/ Cyntec
138S0789	138S0941		ALL	Murata w/ SS
107S00101	107S00005		ALL	Cyntec w/ Yageo
107S00102	107S00017		ALL	Cyntec w/ Yageo
107S00100	107S00057		ALL	Cyntec w/ TFT
107S00103	107S00058		ALL	Cyntec w/ Yageo
107S00104	107S00061		ALL	Cyntec w/ Yageo
107S00105	107S00062		ALL	Cyntec w/ Yageo
152S00403	152S00322		ALL	Murata w/ Chillisin

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00104	138S0978		ALL	Murata w/ Taiyo
311S00072	311S0657		ALL	NXP w/ On Semi
311S00090	311S00028		ALL	On Semi w/ TI
353S00854	353S4342		ALL	TI w/ ST
377S0077	377S0183		ALL	Infineon w/ ST

138S0700	138S0641		ALL	Murata w/ SS&Taiyo
152S00363	152S00048		ALL	Cyntec w/ Vishay
155S0659	155S0382		ALL	Murata w/ TDK
376S00146	376S1061		ALL	NXP w/ Diodes

128S00062	128S00067		ALL	
128S00069	128S00067		ALL	
132S00012	132S0401		ALL	
138S0660	138S0684		ALL	
138S1103	138S0719		ALL	
138S00097	138S0750		ALL	
138S00111	138S00036		ALL	
155S00203	155S0894		ALL	
197S00082	197S00081		ALL	
311S00060	311S0273		ALL	
311S00118	311S0489		ALL	
311S0271	311S00008		ALL	
311S00104	311S00091		ALL	
311S0437	311S00112		ALL	
335S00213	335S0888		ALL	
343S00136	343S00135		ALL	
343S00137	343S00135		ALL	
343S00138	343S00135		ALL	
353S00880	353S3452		ALL	
353S00878	353S00599		ALL	
353S00879	353S00754		ALL	
353S00750	353S00877		ALL	
371S00089	371S00085		ALL	
377S0178	377S00031		ALL	

PAGE TITLE
Alternates BOM Table

Apple Inc.

DRAWING NUMBER 051-00777 SIZE D
REVISION 9.0.0
BRANCH dvt-fab09-0