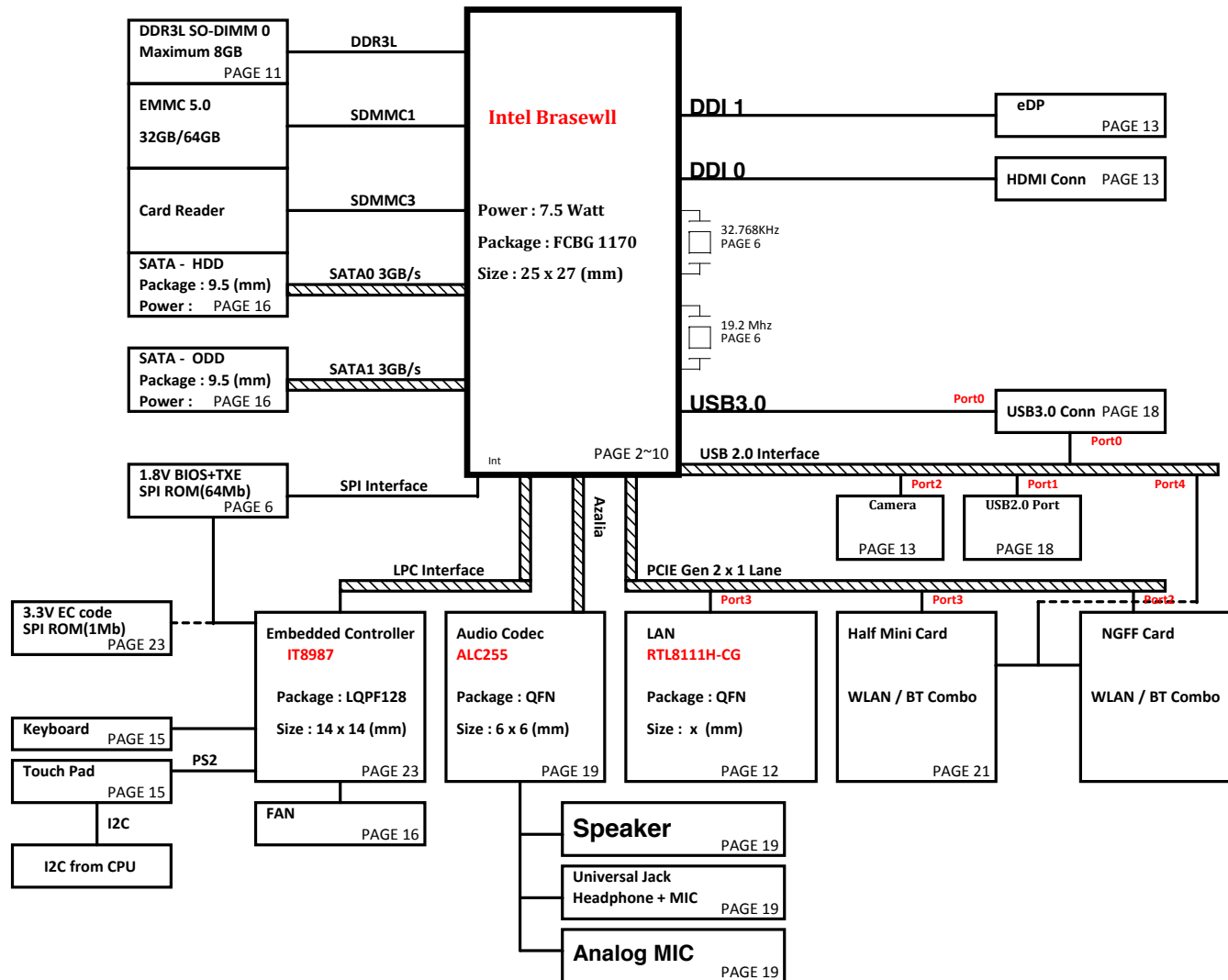


# Z8AD UMA(14")

## Intel Brasewll Platform Block Diagram

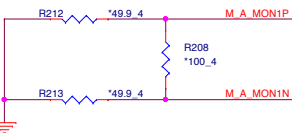
### BOM

EM@ : EMMc  
HD@ : HDD  
GS@ : G-sensor  
TPM@ : TPM  
TSI@ : TOUCH SCREEN I2C  
SP@ : Special

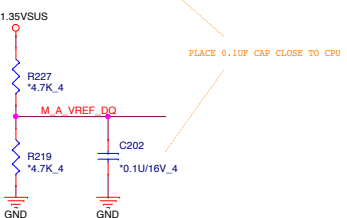
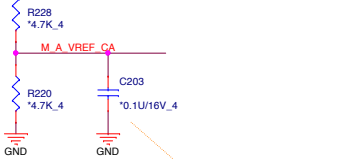


+1.35VSUS [3,9,11,27]  
+3V\_S5 [3,5,9,12,14,15,16,22,26]

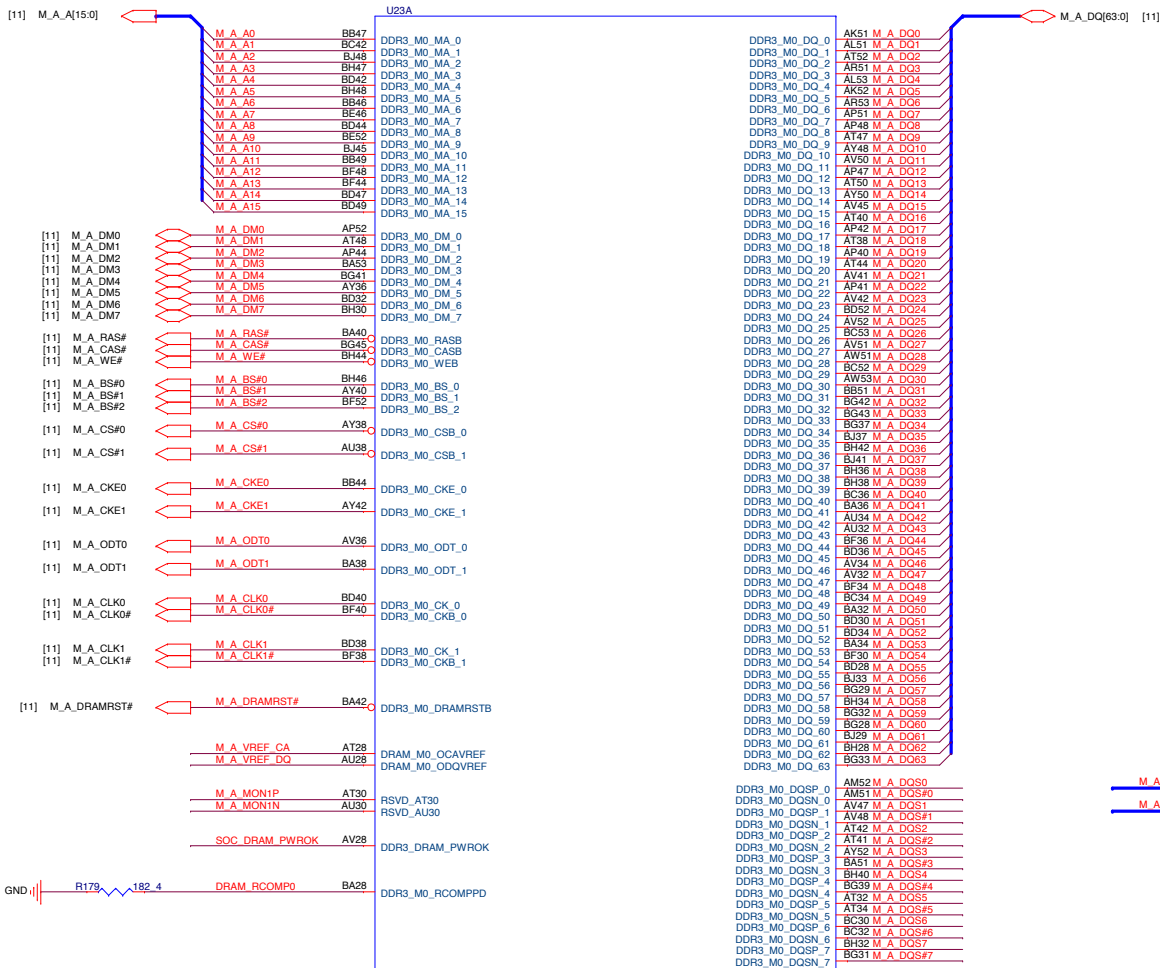
PLACE THE RESISTORS AS CLOSE AS POSSIBLE TO SOC(BSW)  
ROUTE THEM AS SINGLE SHEDD LINES



ROUTE ALL VREF POWER SIGNALS AS THICK TRACES  
PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M\_VREF  
ROUTE THE VREF POWER SIGNALS WITH THICK TRACES



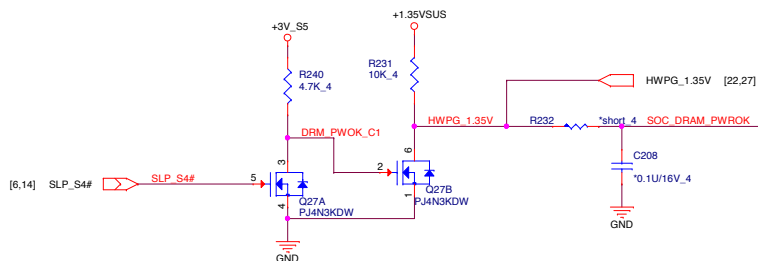
PLACE 0.1UF CAP CLOSE TO CPU



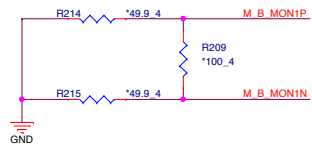
M\_A\_DQS[7:0] M\_A\_DQS[7:0] [11]  
M\_A\_DQS#7[0] M\_A\_DQS#7[0] [11]

Channel 0	Channel 1	SOC Supported Memory Operation Speed
1333 MHz	X	1066 MHz
1600 MHz	X	1600 MHz
1333 MHz	1333 MHz	1066 MHz
1600 MHz	1600 MHz	1600 MHz

Channel 0 need to  
be populated first for the platform to power on

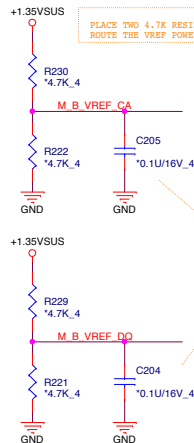


PLACE THE RESISTORS AS CLOSE AS POSSIBLE TO SOC(BSW)  
ROUTE THEM AS SINGLE ENDED LINES

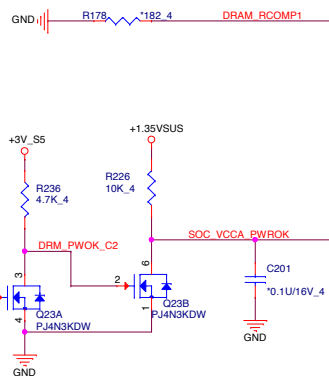


ROUTE ALL VREF POWER SIGNALS AS THICK TRACES

PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M\_VREF  
ROUTE THE VREF POWER SIGNALS WITH THICK TRACES



PLACE 0.1uF CAP CLOSE TO CPU



U23B		
BB7	DDR3_M1_MA_0	DDR3_M1_DQ_0
BC12	DDR3_M1_MA_1	DDR3_M1_DQ_1
B16	DDR3_M1_MA_2	DDR3_M1_DQ_2
BH7	DDR3_M1_MA_3	DDR3_M1_DQ_3
BD12	DDR3_M1_MA_4	DDR3_M1_DQ_4
B16	DDR3_M1_MA_5	DDR3_M1_DQ_5
BB8	DDR3_M1_MA_6	DDR3_M1_DQ_6
BB8	DDR3_M1_MA_7	DDR3_M1_DQ_7
BD10	DDR3_M1_MA_8	DDR3_M1_DQ_8
B25	DDR3_M1_MA_9	DDR3_M1_DQ_9
B16	DDR3_M1_MA_10	DDR3_M1_DQ_10
BB9	DDR3_M1_MA_11	DDR3_M1_DQ_11
B16	DDR3_M1_MA_12	DDR3_M1_DQ_12
BF10	DDR3_M1_MA_13	DDR3_M1_DQ_13
BD7	DDR3_M1_MA_14	DDR3_M1_DQ_14
BD5	DDR3_M1_MA_15	DDR3_M1_DQ_15
AP2	DDR3_M1_DM_0	DDR3_M1_DQ_16
AP6	DDR3_M1_DM_1	DDR3_M1_DQ_17
AP10	DDR3_M1_DM_2	DDR3_M1_DQ_18
BA0	DDR3_M1_DM_3	DDR3_M1_DQ_19
BG13	DDR3_M1_DM_4	DDR3_M1_DQ_20
AY18	DDR3_M1_DM_5	DDR3_M1_DQ_21
BD22	DDR3_M1_DM_6	DDR3_M1_DQ_22
BH24	DDR3_M1_DM_7	DDR3_M1_DQ_23
BA14	DDR3_M1_RASB	DDR3_M1_DQ_24
BC10	DDR3_M1_CASB	DDR3_M1_DQ_25
BH10	DDR3_M1_WEB	DDR3_M1_DQ_26
B16	DDR3_M1_BS_0	DDR3_M1_DQ_27
AY18	DDR3_M1_BS_1	DDR3_M1_DQ_28
BF2	DDR3_M1_BS_2	DDR3_M1_DQ_29
AY18	DDR3_M1_CSB_0	DDR3_M1_DQ_30
AU16	DDR3_M1_CSB_1	DDR3_M1_DQ_31
BB10	DDR3_M1_CKE_0	DDR3_M1_DQ_32
AY18	DDR3_M1_CKE_1	DDR3_M1_DQ_33
AV18	DDR3_M1_ODT_0	DDR3_M1_DQ_34
BA16	DDR3_M1_ODT_1	DDR3_M1_DQ_35
BD14	DDR3_M1_CK_0	DDR3_M1_DQ_36
BF16	DDR3_M1_CKB_0	DDR3_M1_DQ_37
BD16	DDR3_M1_CK_1	DDR3_M1_DQ_38
BF16	DDR3_M1_CKB_1	DDR3_M1_DQ_39
BA12	DDR3_M1_DRAMRSTB	DDR3_M1_DQ_40
AT26	DDR3_M1_OCAVREF	DDR3_M1_DQ_41
AU26	DDR3_M1_ODOVREF	DDR3_M1_DQ_42
AT24	RSVD_AT24	DDR3_M1_DQ_43
AU24	RSVD_AU24	DDR3_M1_DQ_44
AV26	SOC_VCCA_PWROK	DDR3_M1_DQ_45
BA26	DRAM_RCOMP1	DDR3_M1_DQ_46
		DDR3_M1_DQ_47
		DDR3_M1_DQ_48
		DDR3_M1_DQ_49
		DDR3_M1_DQ_50
		DDR3_M1_DQ_51
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		DDR3_M1_DQ_60
		DDR3_M1_DQ_61
		DDR3_M1_DQ_62
		DDR3_M1_DQ_63
		DDR3_M1_DQSP_0
		DDR3_M1_DQSN_0
		DDR3_M1_DQSP_1
		DDR3_M1_DQSN_1
		DDR3_M1_DQSP_2
		DDR3_M1_DQSN_2
		DDR3_M1_DQSP_3
		DDR3_M1_DQSN_3
		DDR3_M1_DQSP_4
		DDR3_M1_DQSN_4
		DDR3_M1_DQSP_5
		DDR3_M1_DQSN_5
		DDR3_M1_DQSP_6
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		DDR3_M1_DQSP_7
		DDR3_M1_DQSN_7

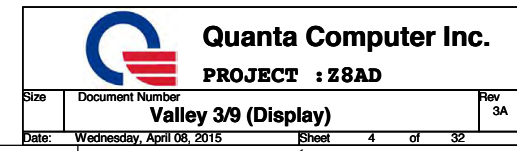
2 OF 12

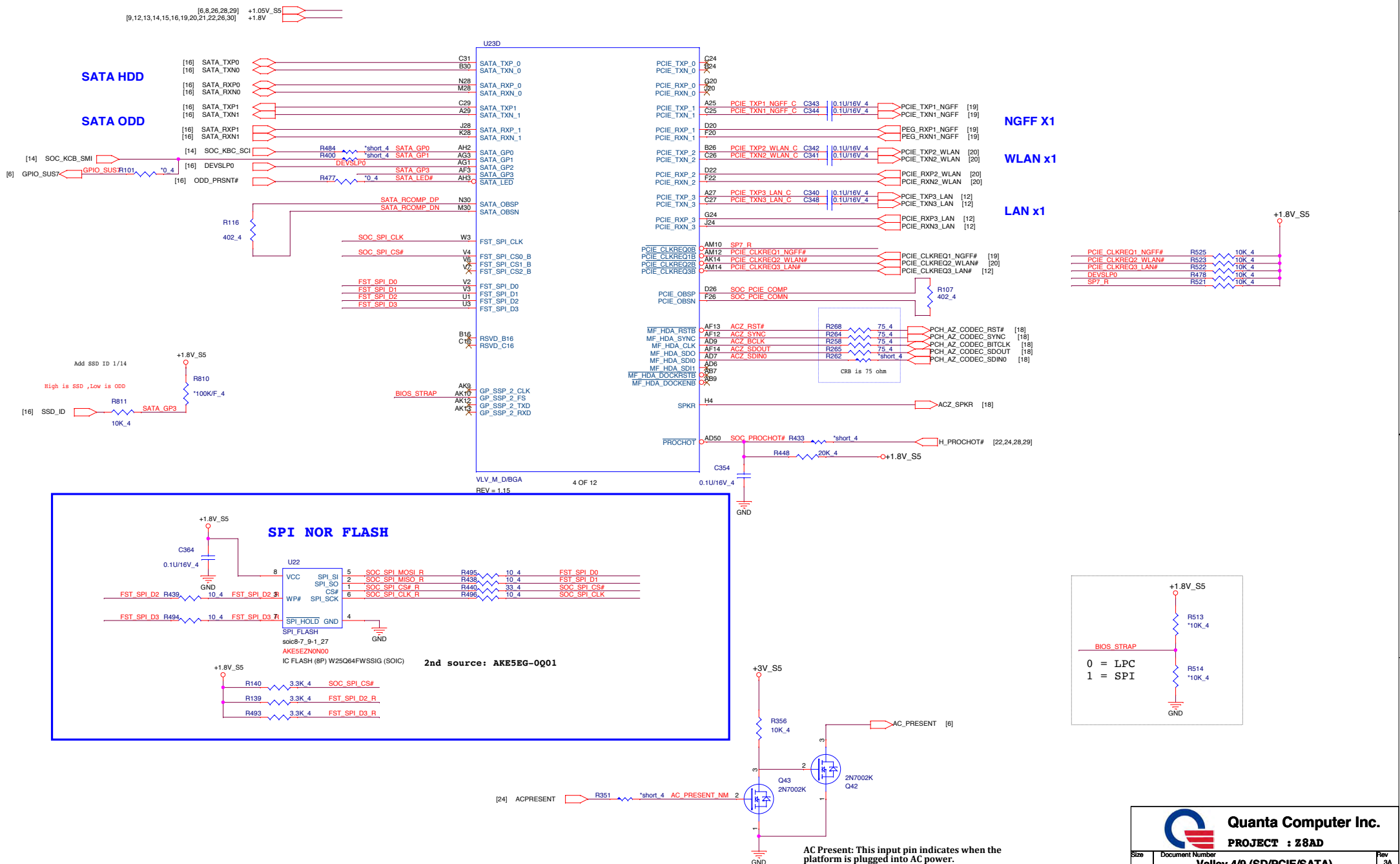
VLV\_M\_D/BGA  
REV = 1.15



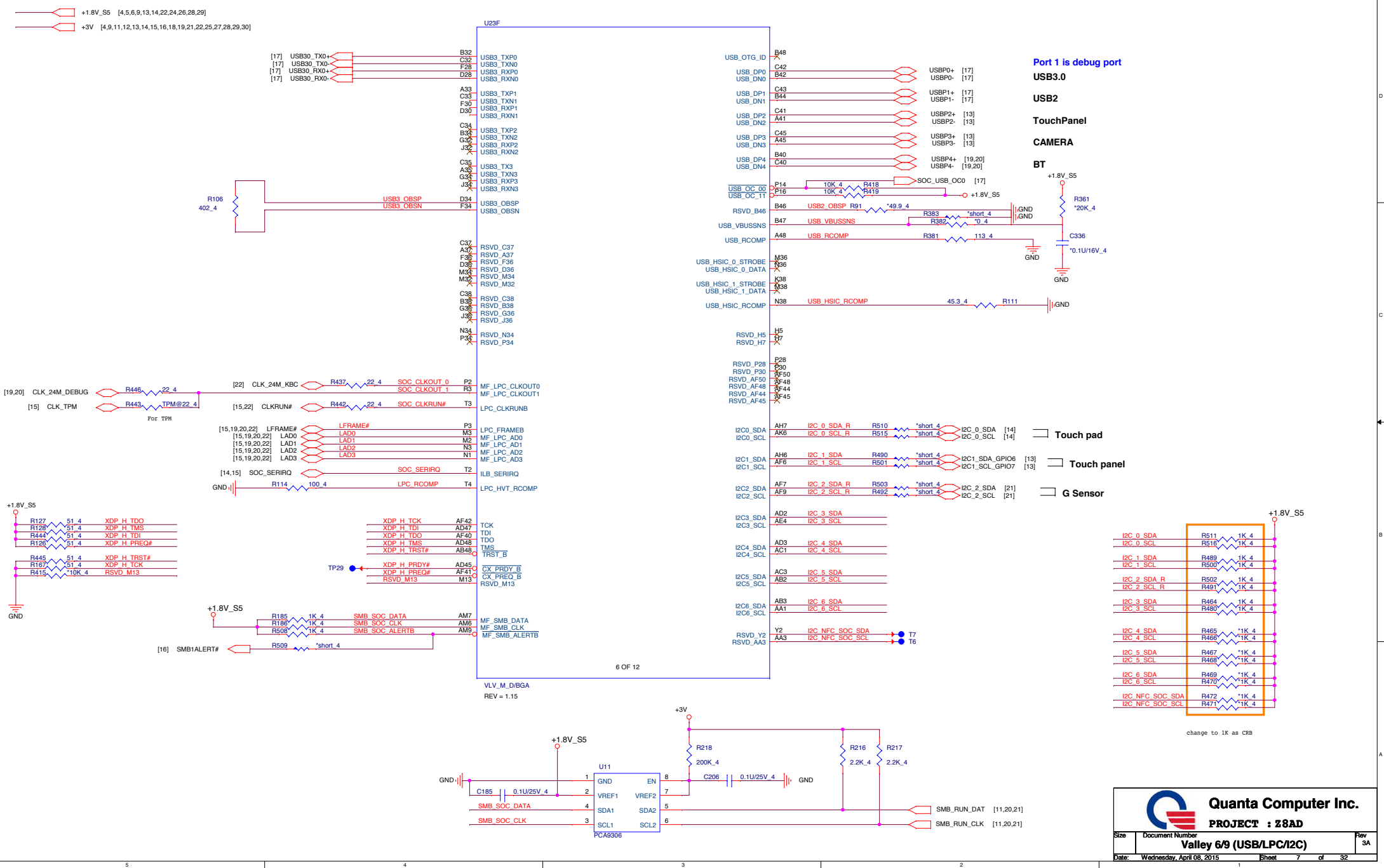
**Quanta Computer Inc.**  
**PROJECT : z8AD**

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	Valley 2/9 (DDR8)	3A
Date:	Wednesday, April 08, 2015	Sheet 3 of 32



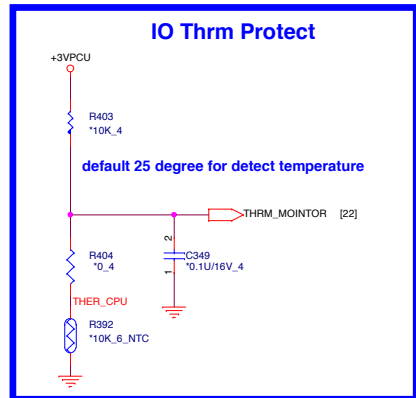
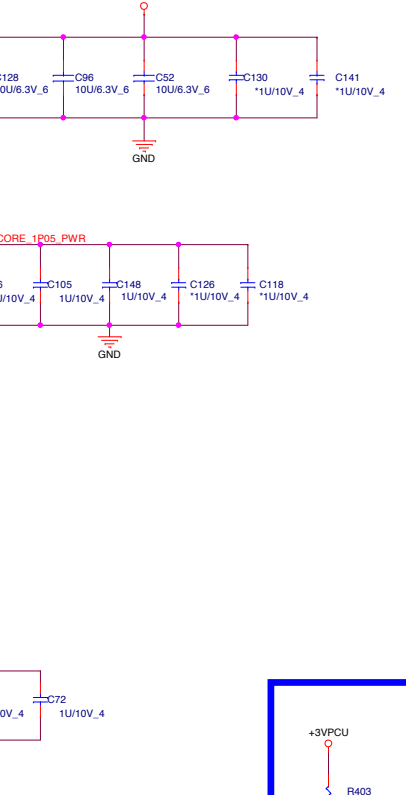
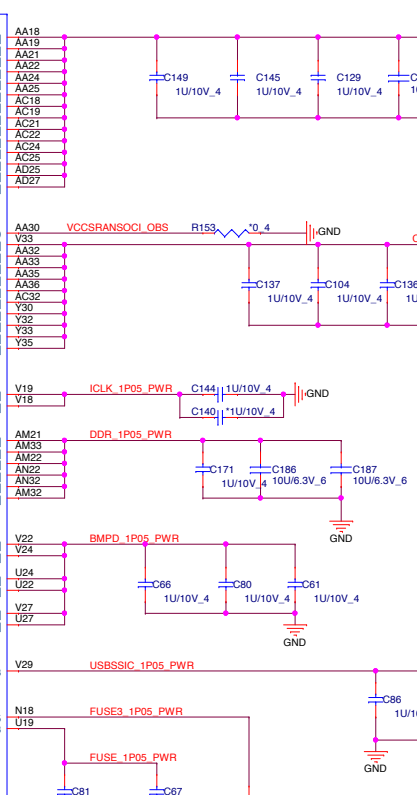
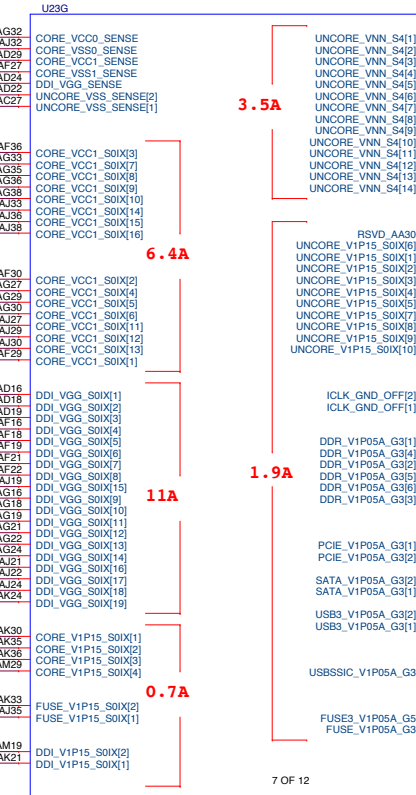
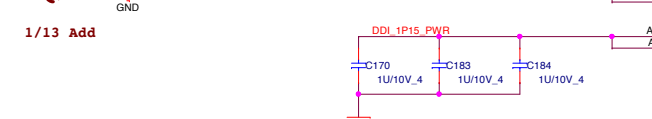
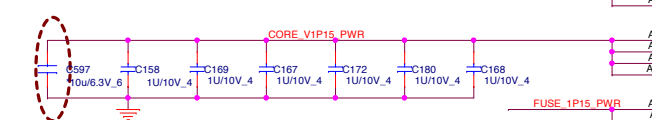
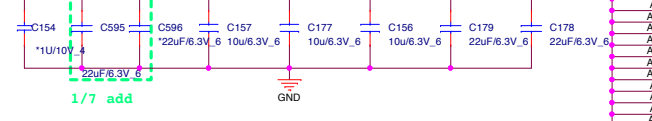
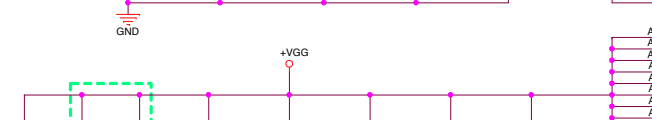
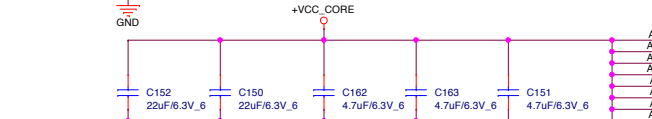
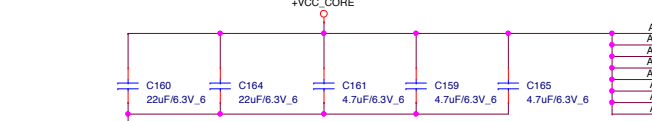
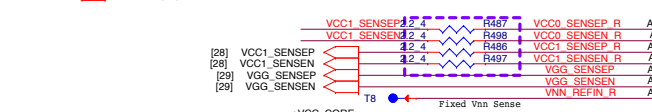






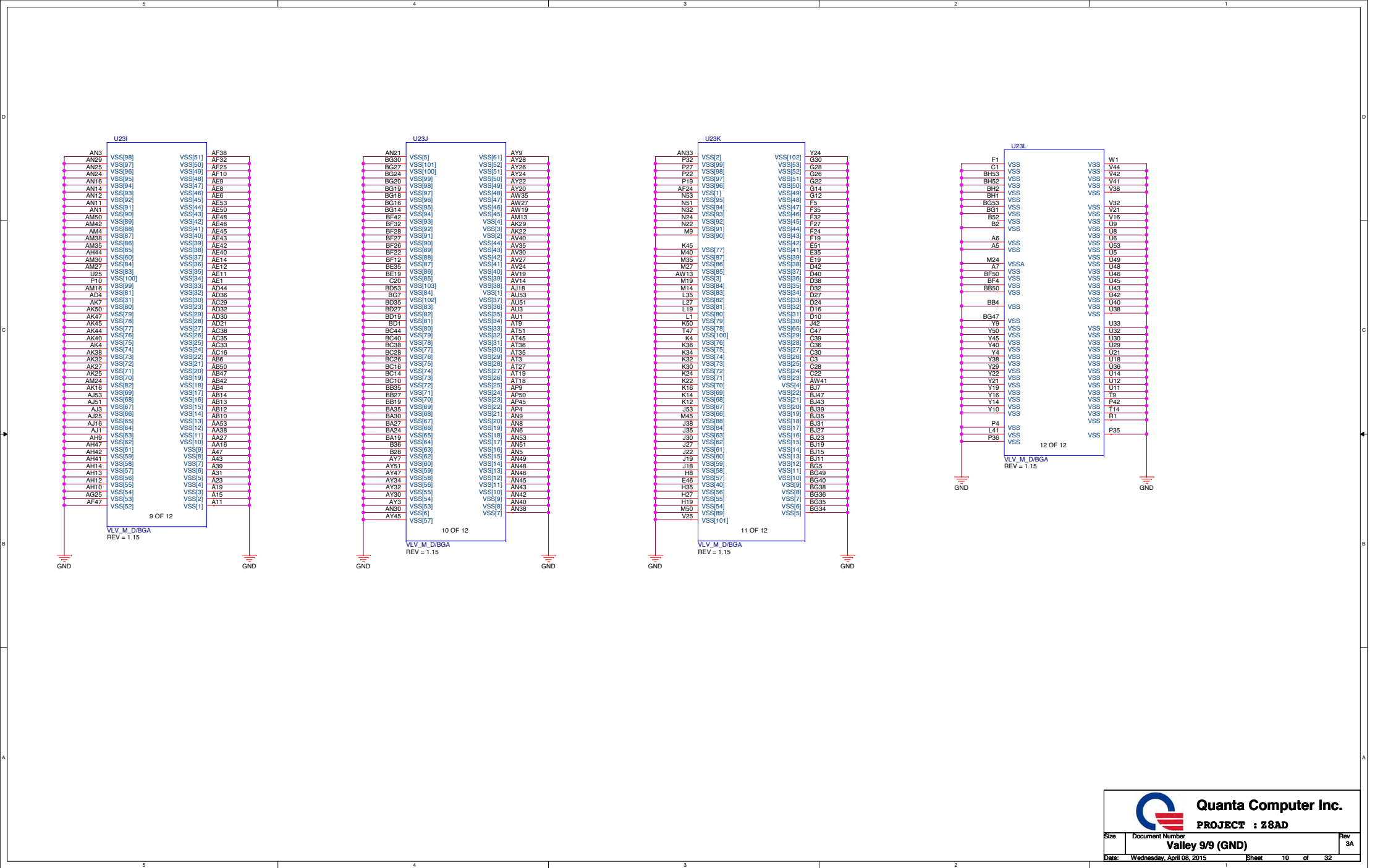
+VCC\_CORE [28]  
+VGG [29]  
+3V [4,7,9,11,12,13,14,15,16,18,19,21,22,25,27,28,29,30]  
+1.05V\_S5 [6,26,28,29]  
+1.15V [26]

3/16 change 0 ohm by acer



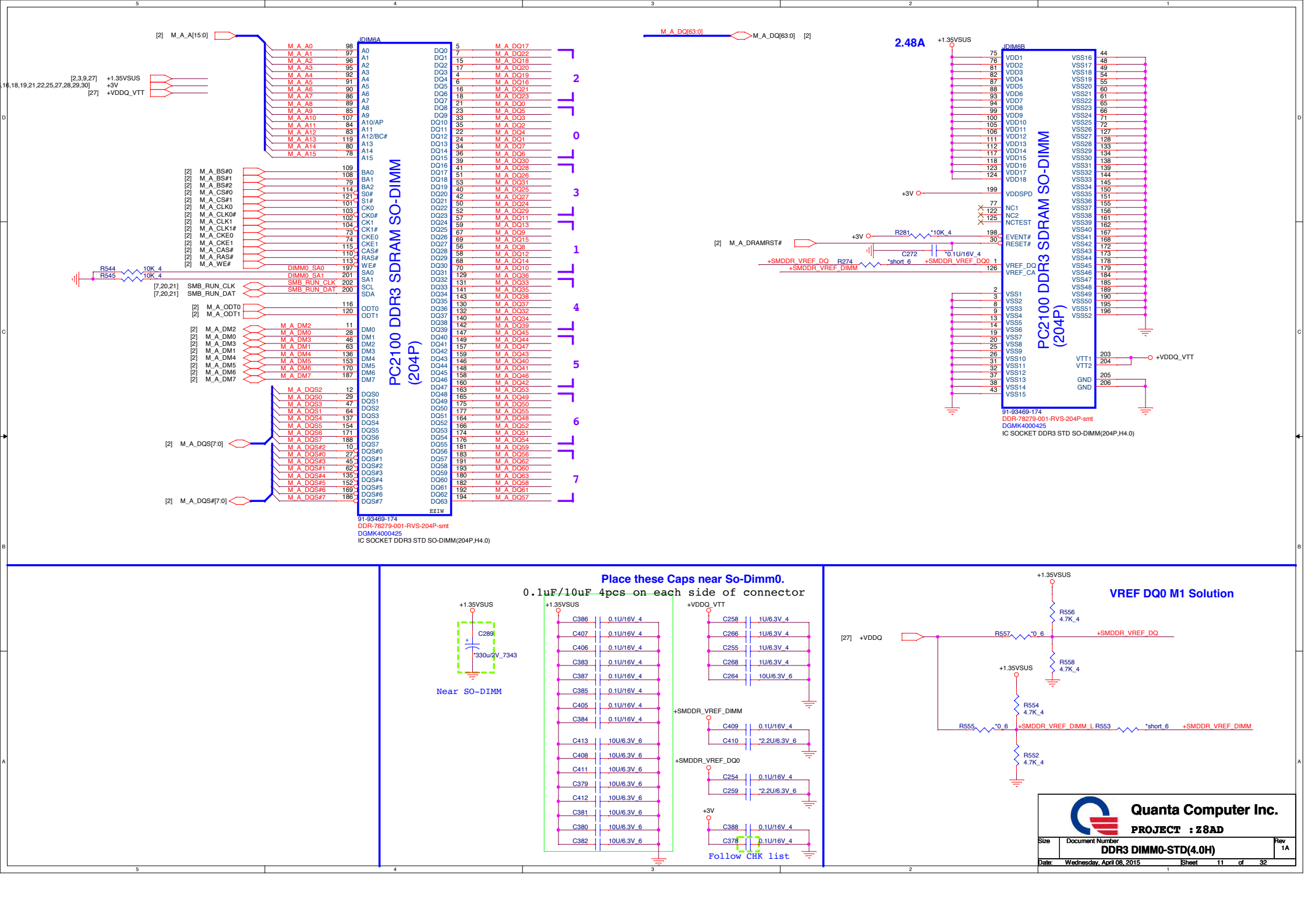




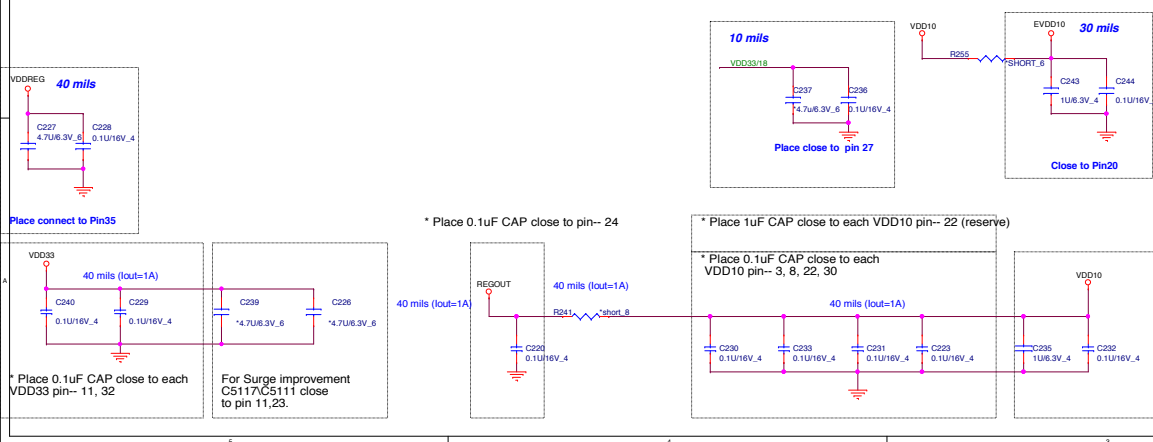
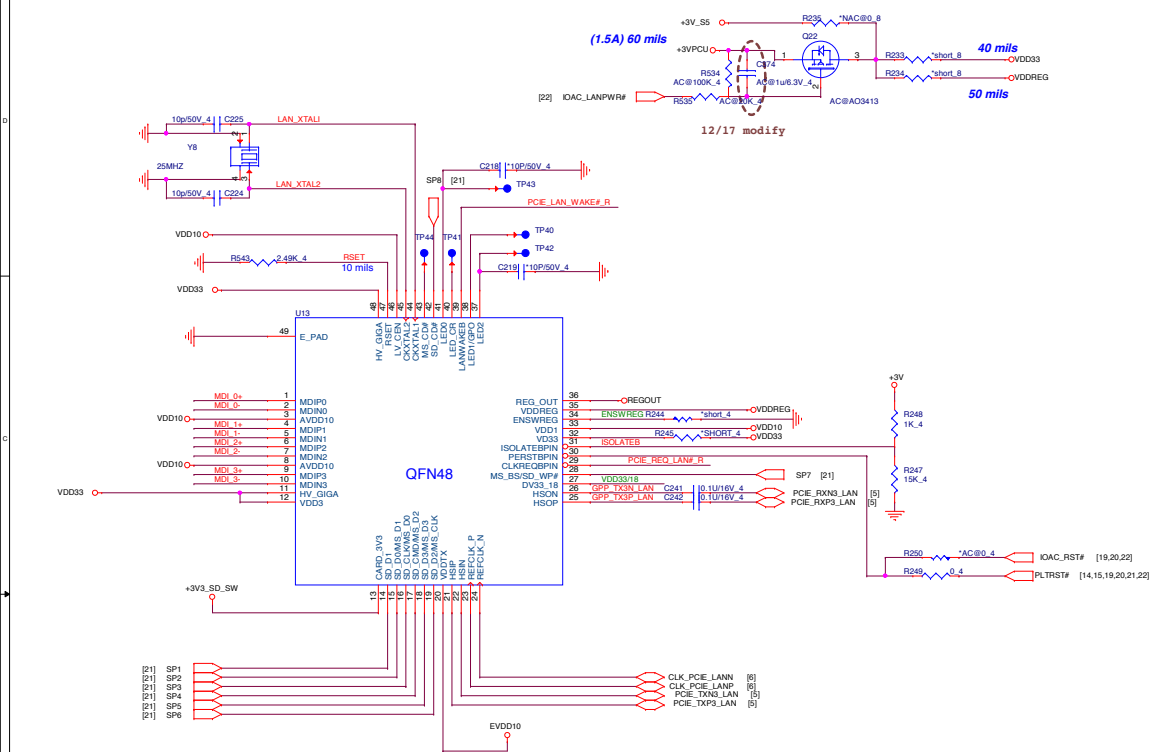


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**PROJECT : z8AD**

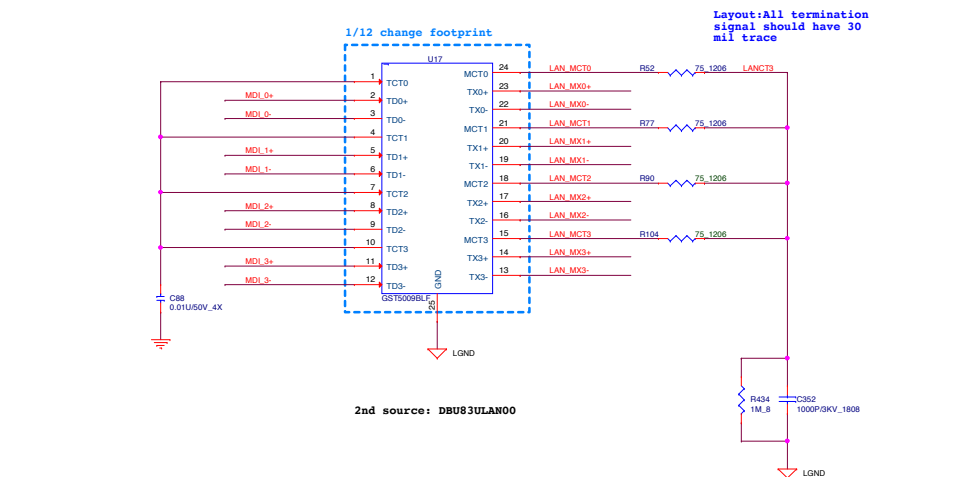
Size	Document Number	Rev
	Valley 9/9 (GND)	3A
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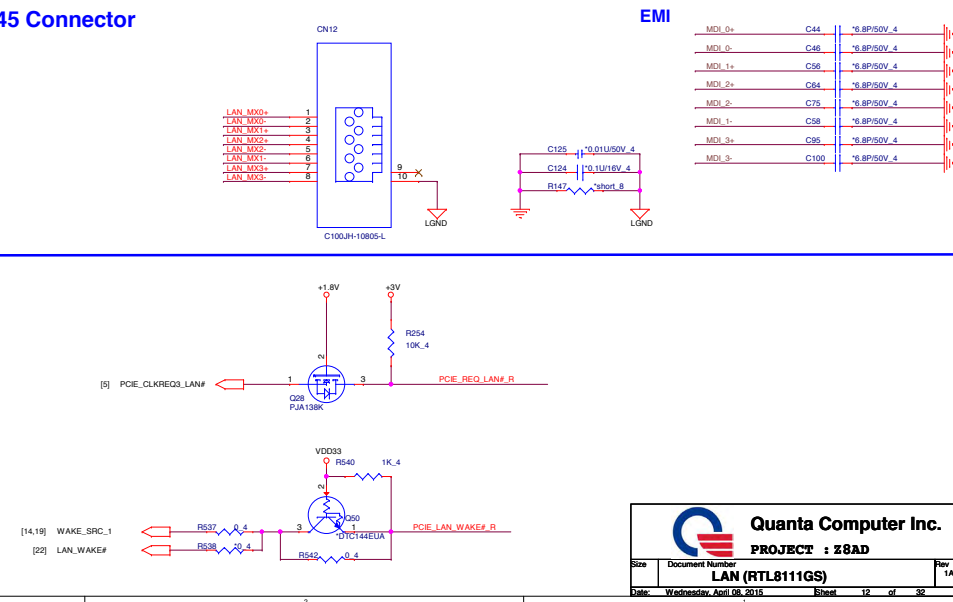
## LAN/Card reader (LAN)



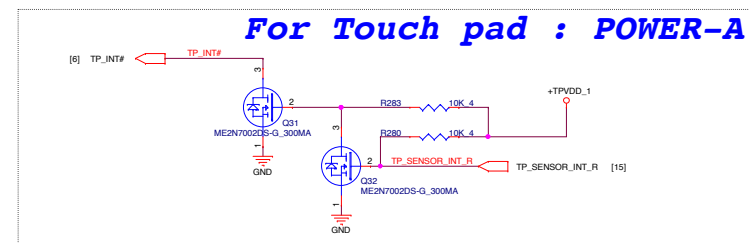
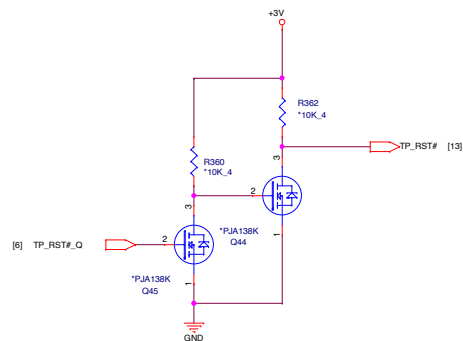
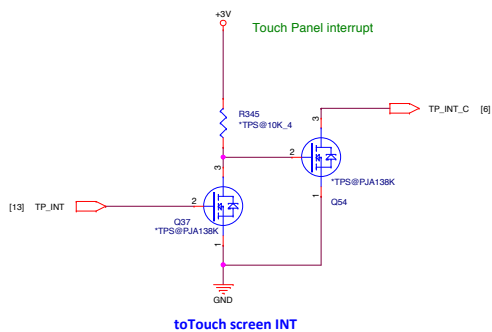
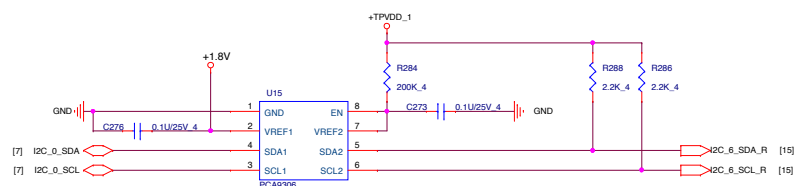
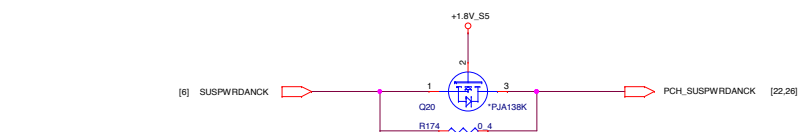
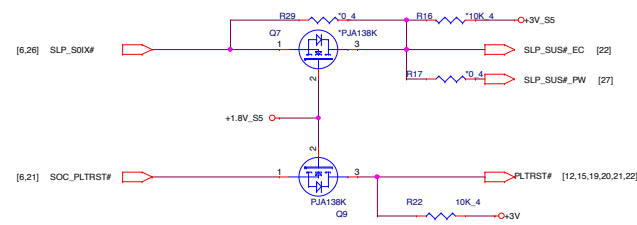
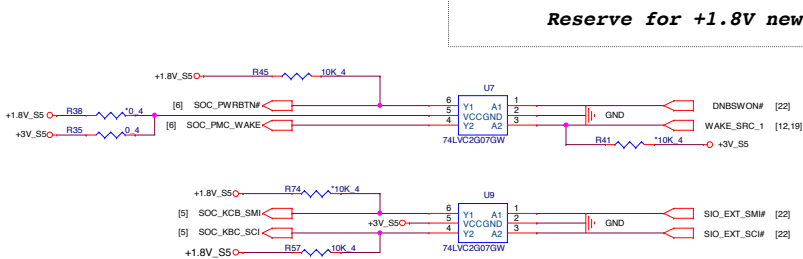
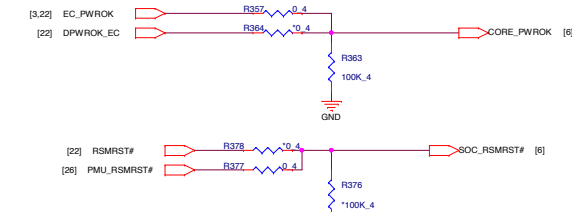
## Transformer (LAN)



## RJ45 Connector

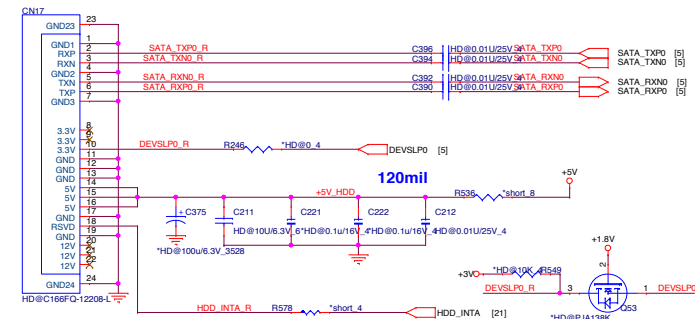




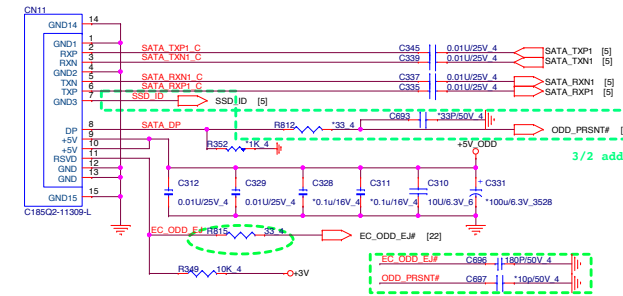




## 2.5" SATA HDD (HDD)

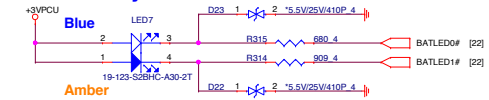


## SATA ODD Connector

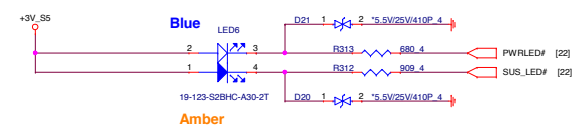


## LED/SW (UIF)

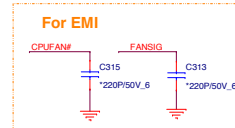
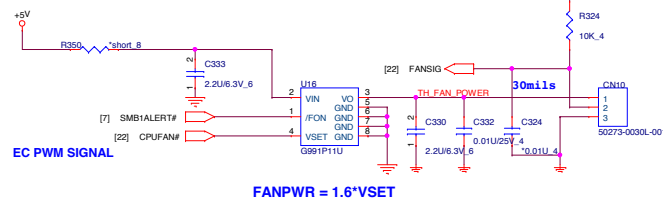
### Battery indicator



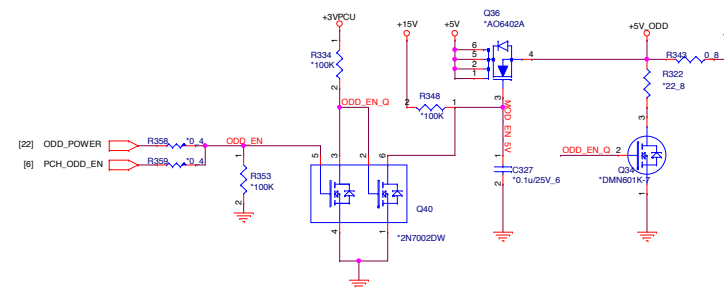
### PWR indicator



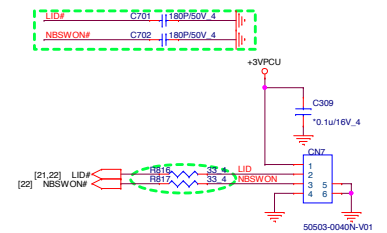
## CPU FAN CTRL(THM)



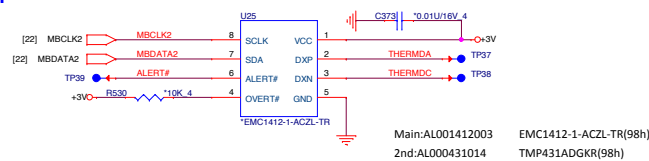
## ODD Power (SATA)



## PWR button DB CON

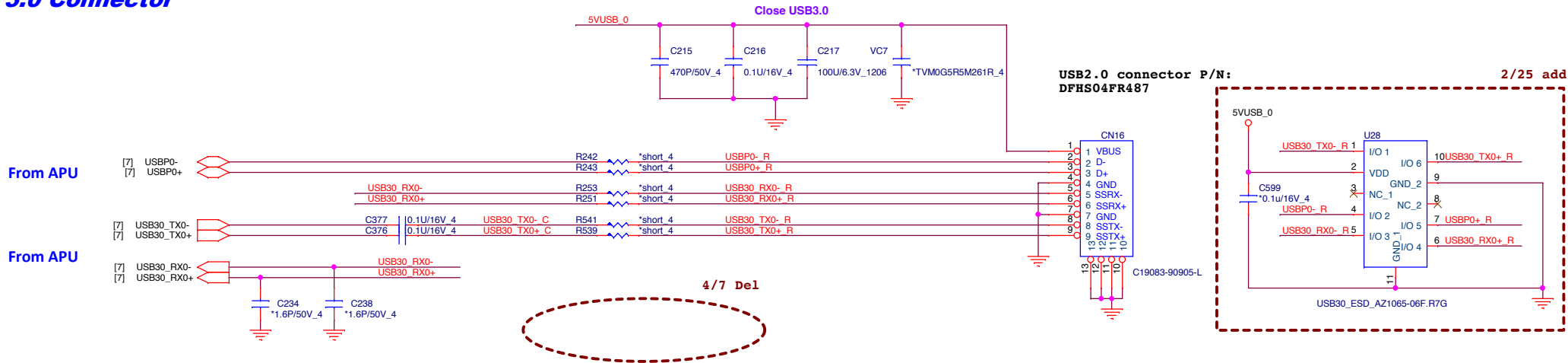


## CPU Thermal sensor(THS) / MB Local TEMP

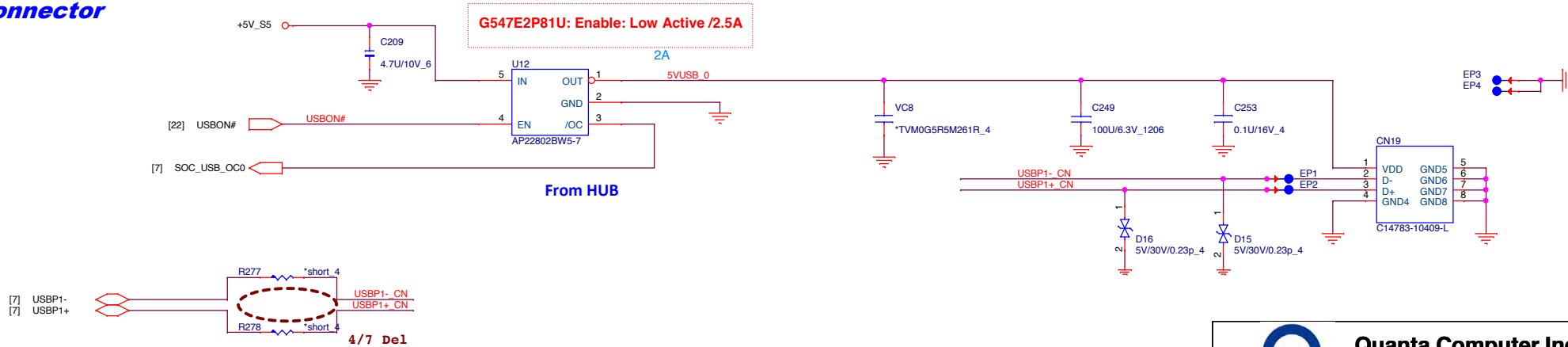




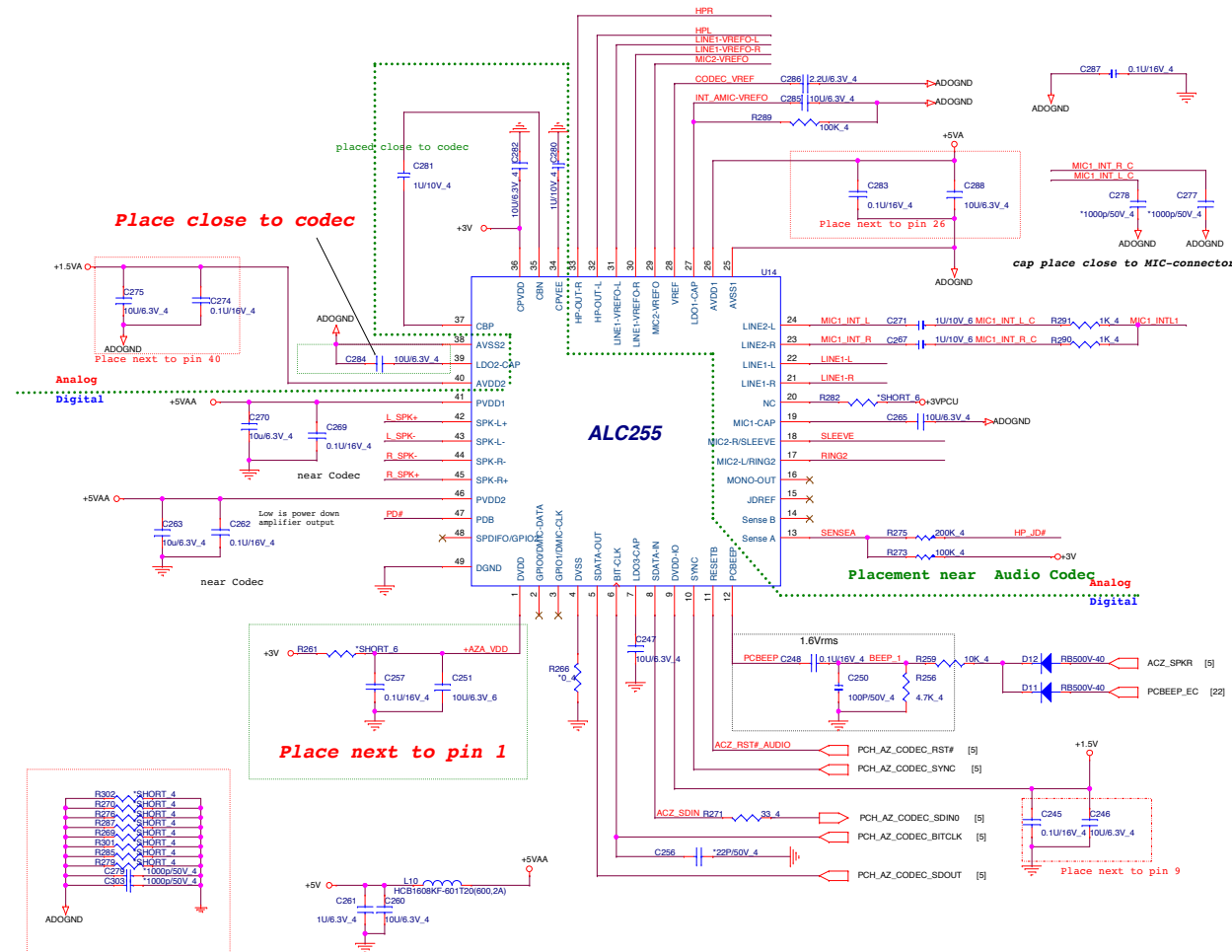
## USB 3.0 Connector



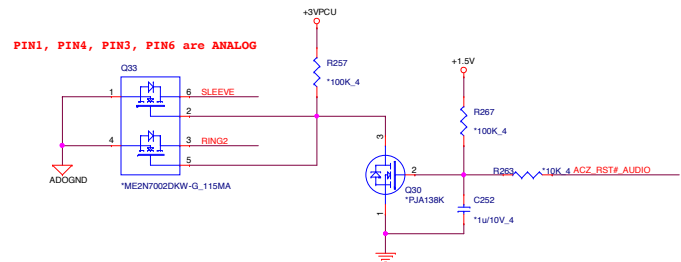
## USB 2.0 Connector



[13,16,25,30] +5V 

[illegible]

PIN1, PIN4, PIN3, PIN6 are ANALOG



DNO01542000  
mic-a-m-qtzea01hf-2p-top

U26  
1  
2

MIC1\_INTL1

R563 10K\_4

INT\_AMIC\_VREF0

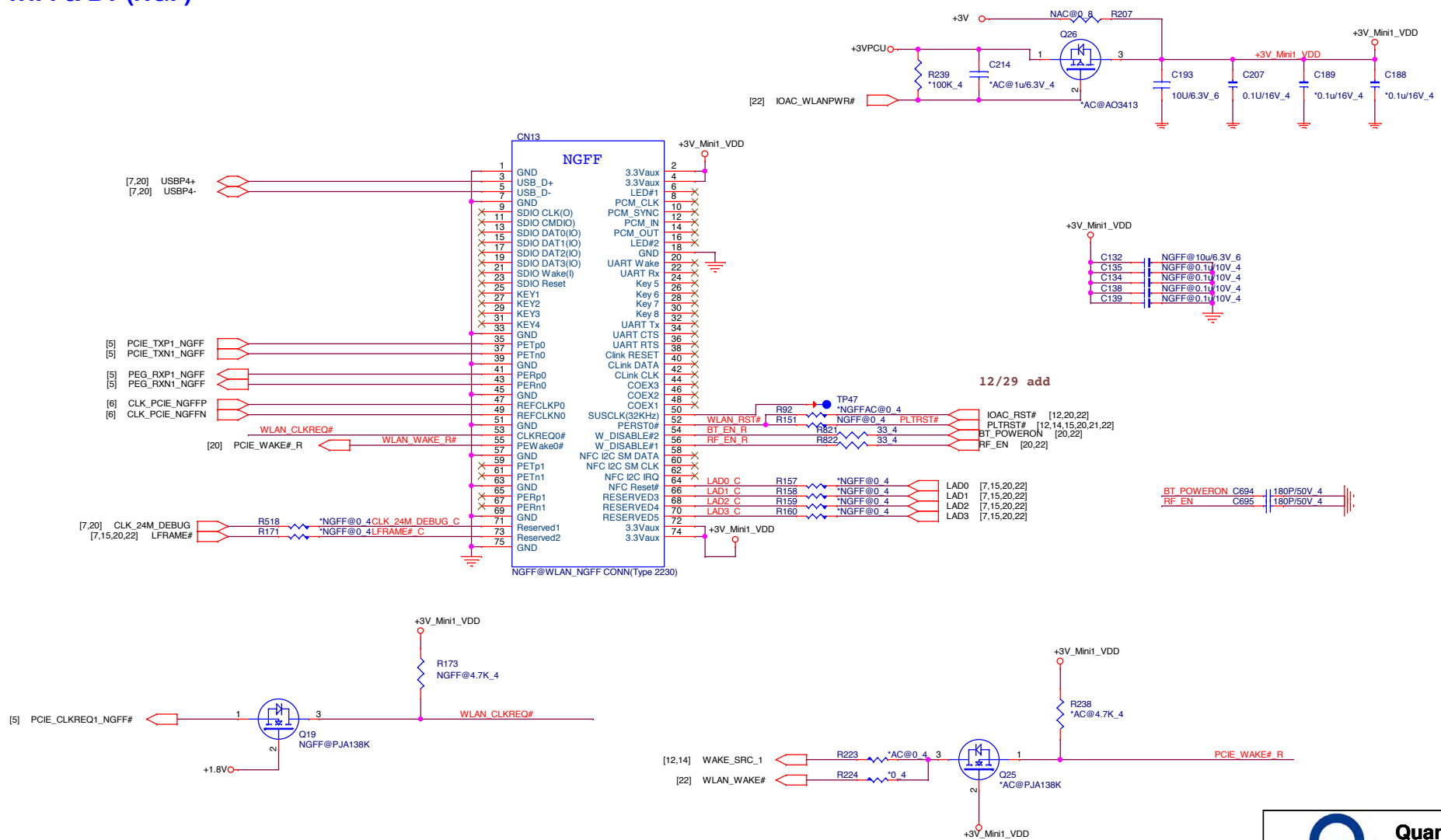
C415

\*22p/50V\_4

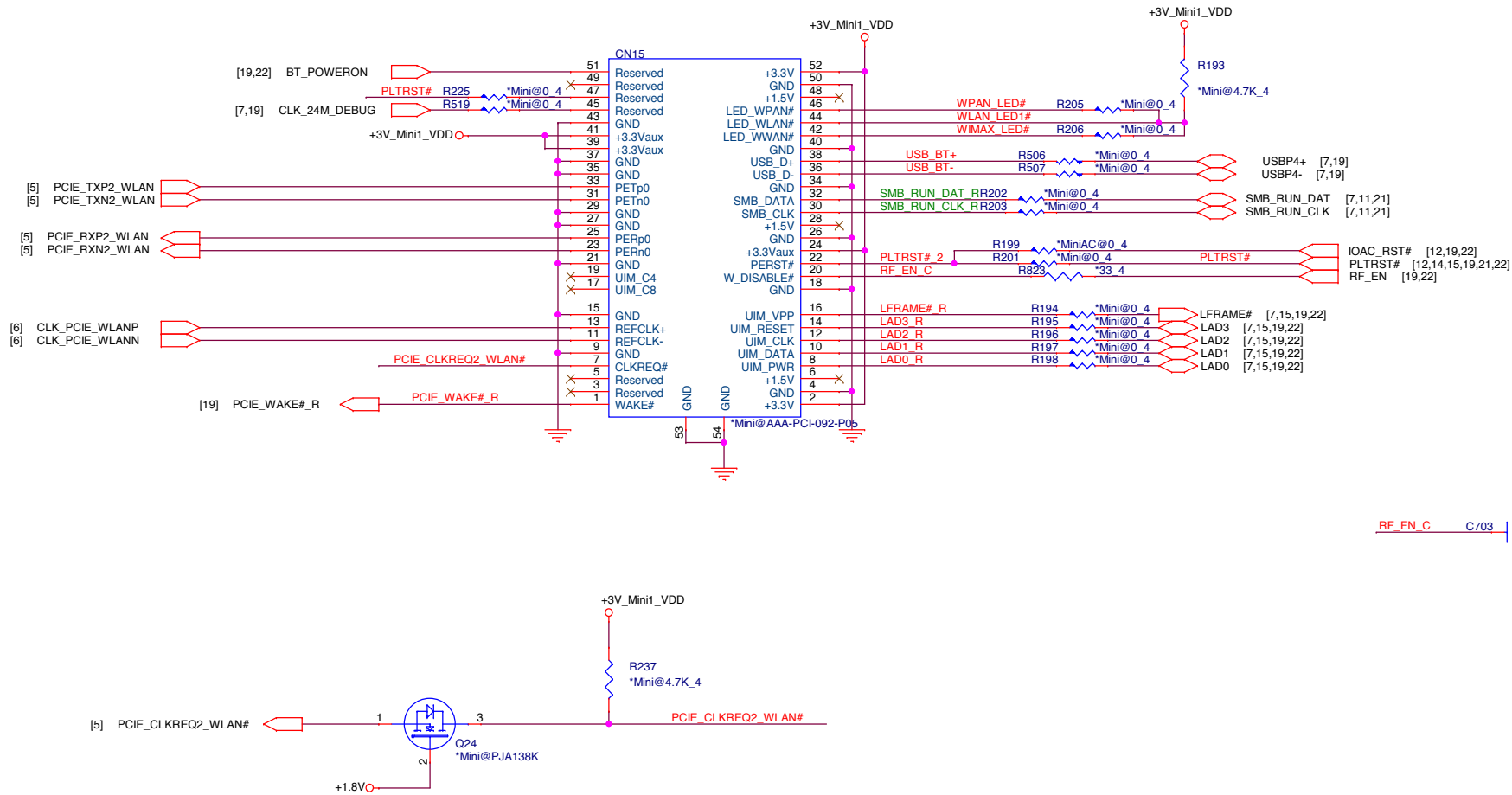
ADO\_GND

The diagram shows a circuit with a node labeled 'SHORT 6' connected to a ground symbol labeled 'ADOGND' through a resistor labeled 'R311'. This represents a short circuit condition.

NGFF WiFi & BT (NGF)



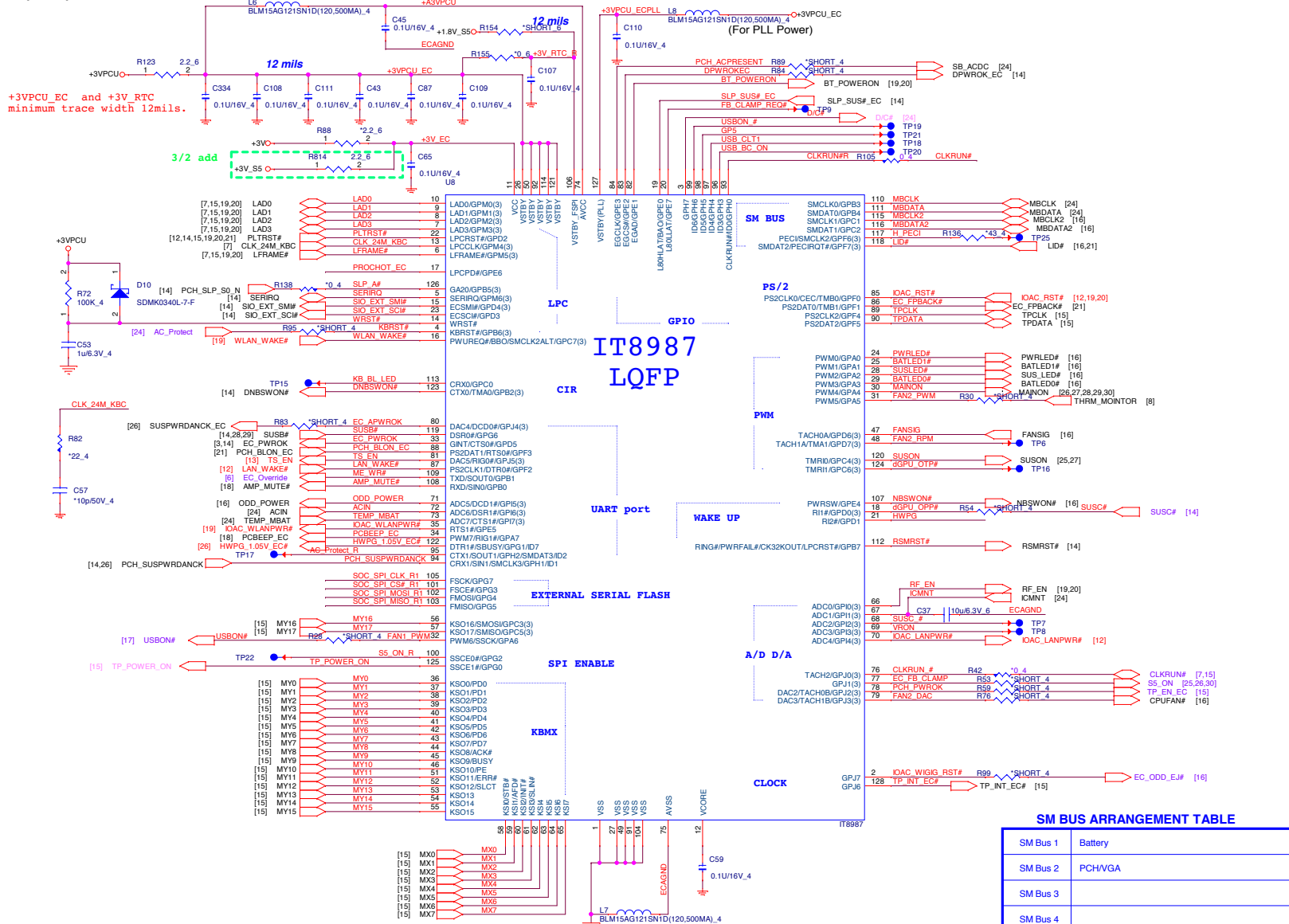
# WLAN



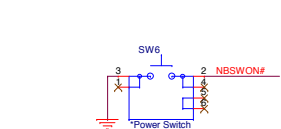
RF\_EN\_C C703 || \*10p/50V\_4



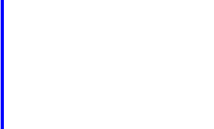
EC(KBC)



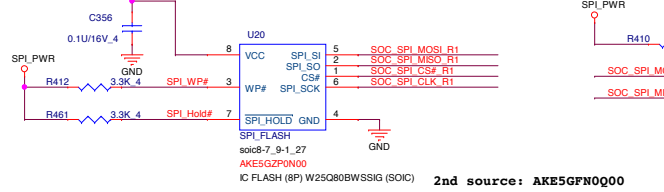
For test only



Reset SW (FSW)

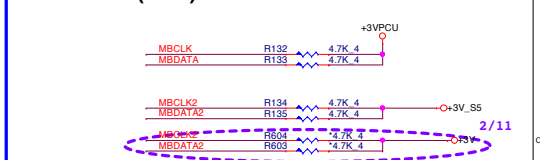


SPI NOR FLASH

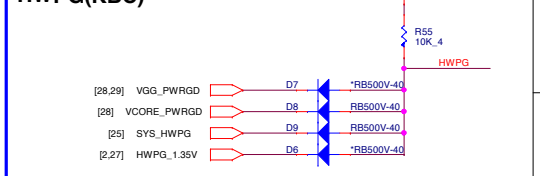



SM BUS ARRANGEMENT TABLE	
SM Bus 1	Battery
SM Bus 2	PCH/VGA
SM Bus 3	
SM Bus 4	

SM BUS PU(KBC)



HWP(KBC)





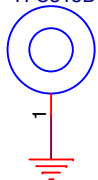
**Quanta Computer Inc.**  
**PROJECT : Z8AD**  
**KBC IT8987**

Size	Document Number	Rev
		3A

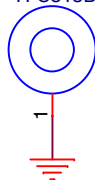
2nd source: AKE5GFNOQ00

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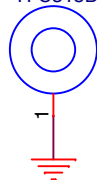
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\*H-C315D118P2



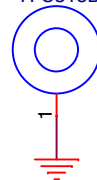
HOLE8  
\*H-C315D118P2



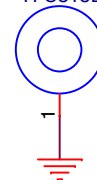
HOLE9  
\*H-C315D118P2



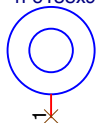
HOLE17  
\*H-C315D118P2



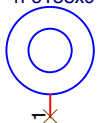
HOLE11  
\*H-C315D118P2



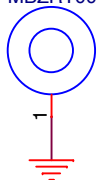
HOLE10  
\*h-o138x91d138x91n



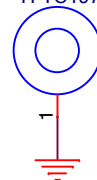
HOLE14  
\*h-o138x91d138x91n



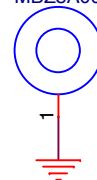
HOLE19  
MBZRT001010



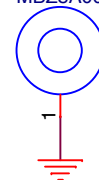
HOLE21  
\*H-TC197BC65D65P2



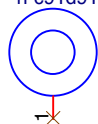
HOLE22  
MBZ8A001010



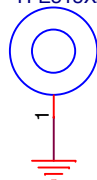
HOLE20  
MBZ8A001010



HOLE12  
\*h-c91d91n



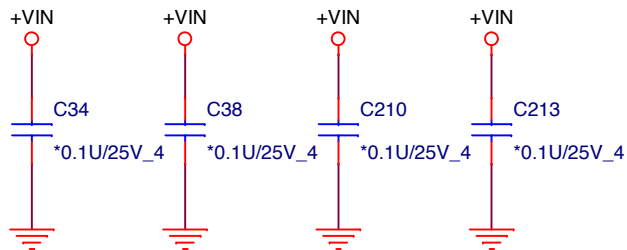
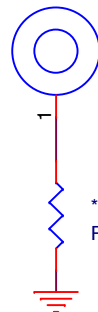
HOLE18  
\*H-E315X276D118P2



HOLE16  
\*H-C315D118P2



\*H-C276D118P2  
HOLE7

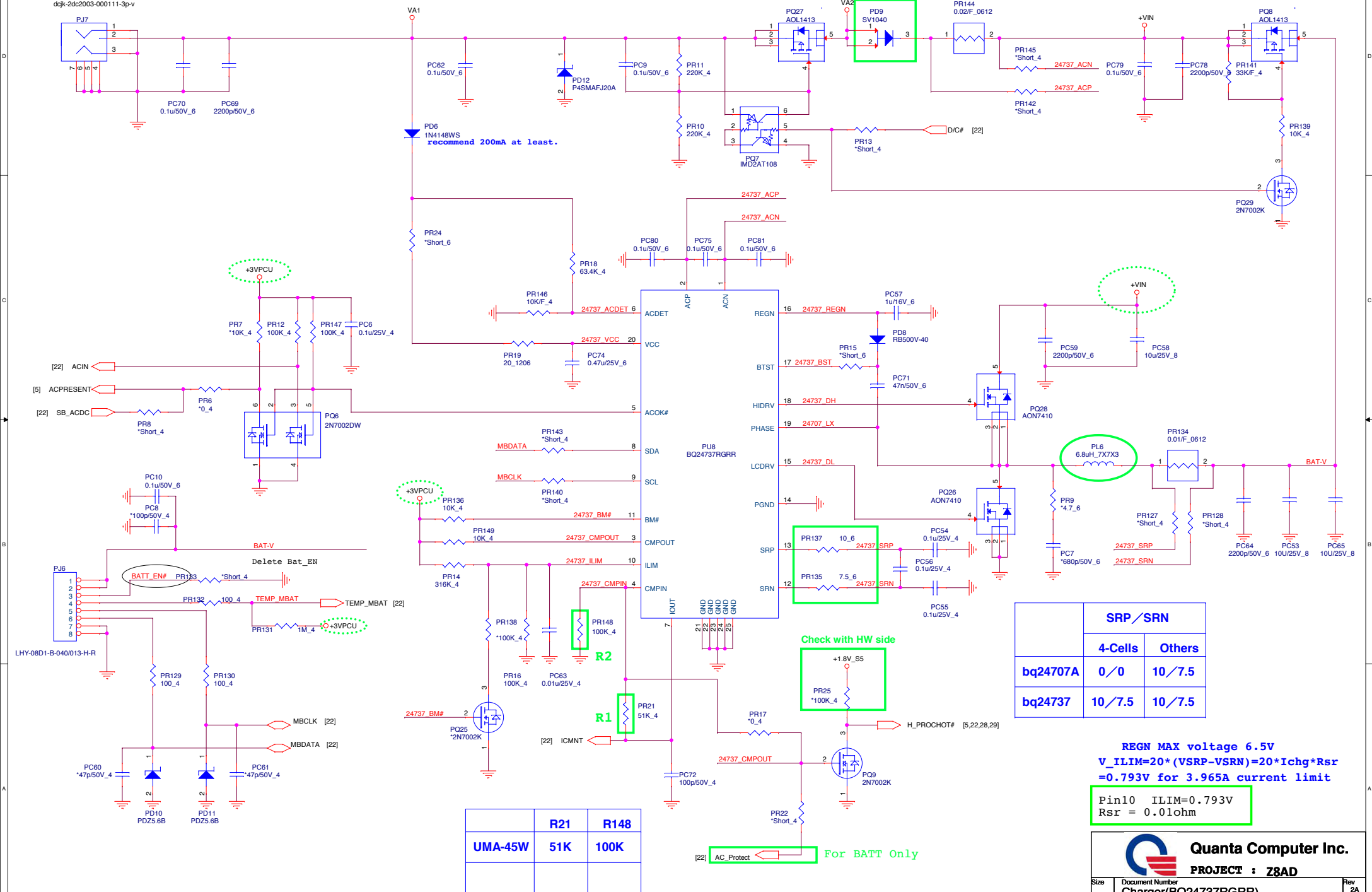


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**PROJECT : Z8AD**

Size	Document Number	Rev
	<b>Thermal / Hole</b>	1A
Date:	Wednesday, April 08, 2015	Sheet 23 of 32

2DC2003-002111F  
dcjk-2dc2003-000111-3p-v



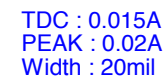
	SRP/SRN	
	4-Cells	Others
bq24707A	0/0	10/7.5
bq24737	10/7.5	10/7.5

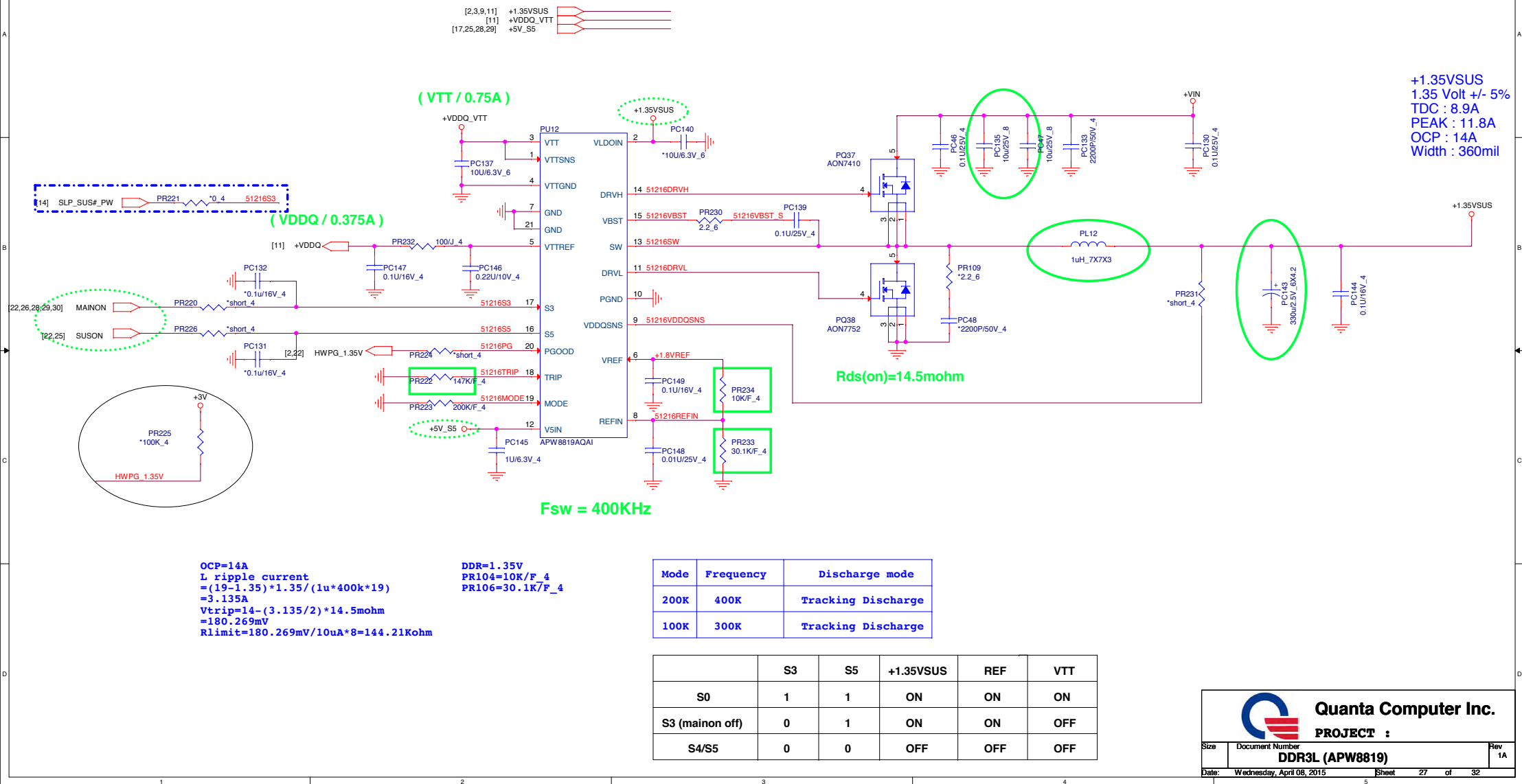
REGN MAX voltage 6.5V  
 $V_{ILIM} = 20 * (VSRP - VSRN) = 20 * I_{chg} * R_{sr}$   
 = 0.793V for 3.965A current limit

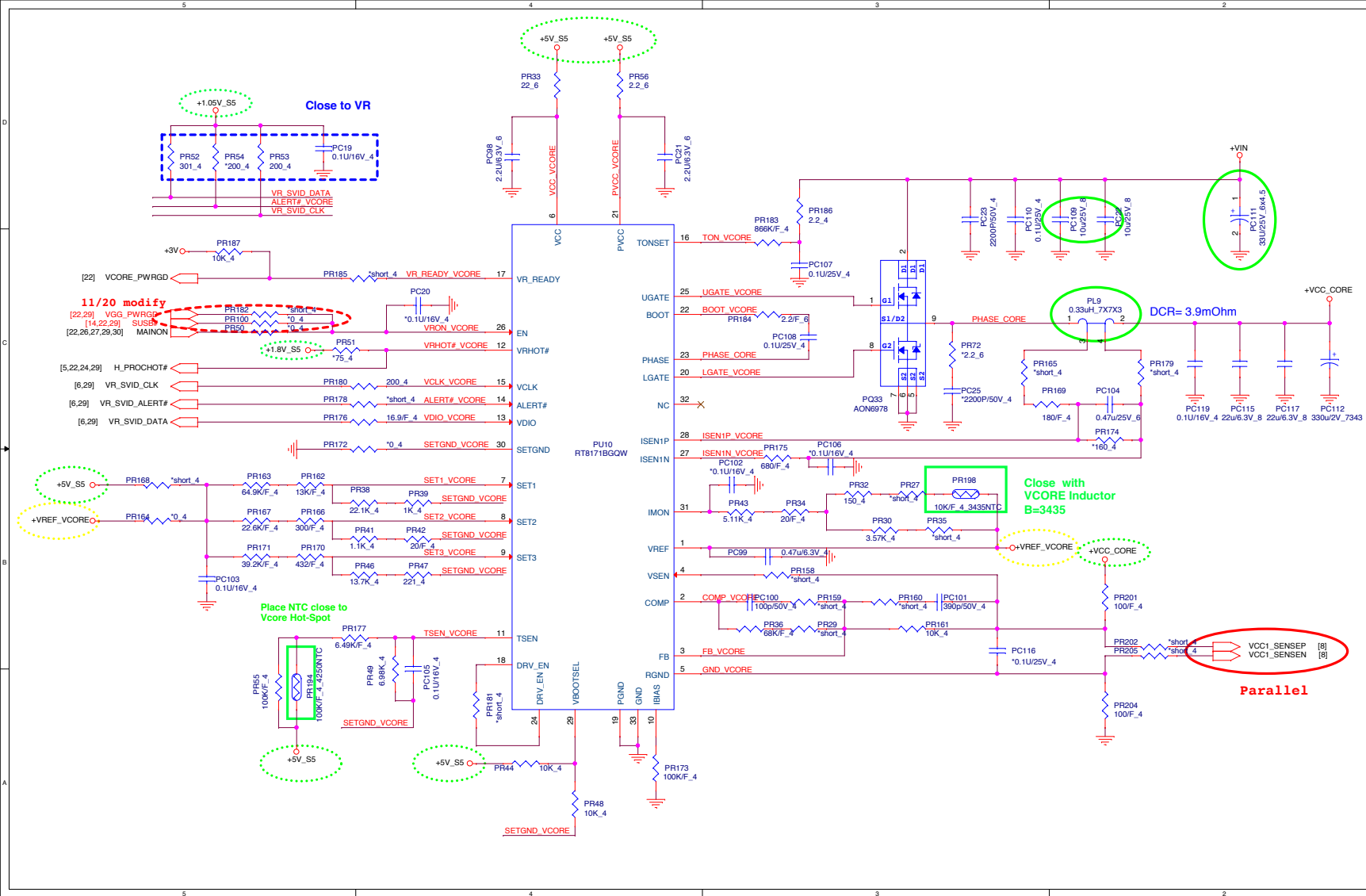
```
Pin10  ILIM=0.793V
Rsr = 0.01ohm
```











## VR 12.1

## Braswell - VCC0+1 (1 Phase)

Icc TDC PL2 : TBD

Icc Max : 7A

OCP : 12.4A

Fsw : 800KHz

Vboot : 1V

VR address : 0

## VCC0+1 L/L :

R\_DC\_LL : 0 mV/A

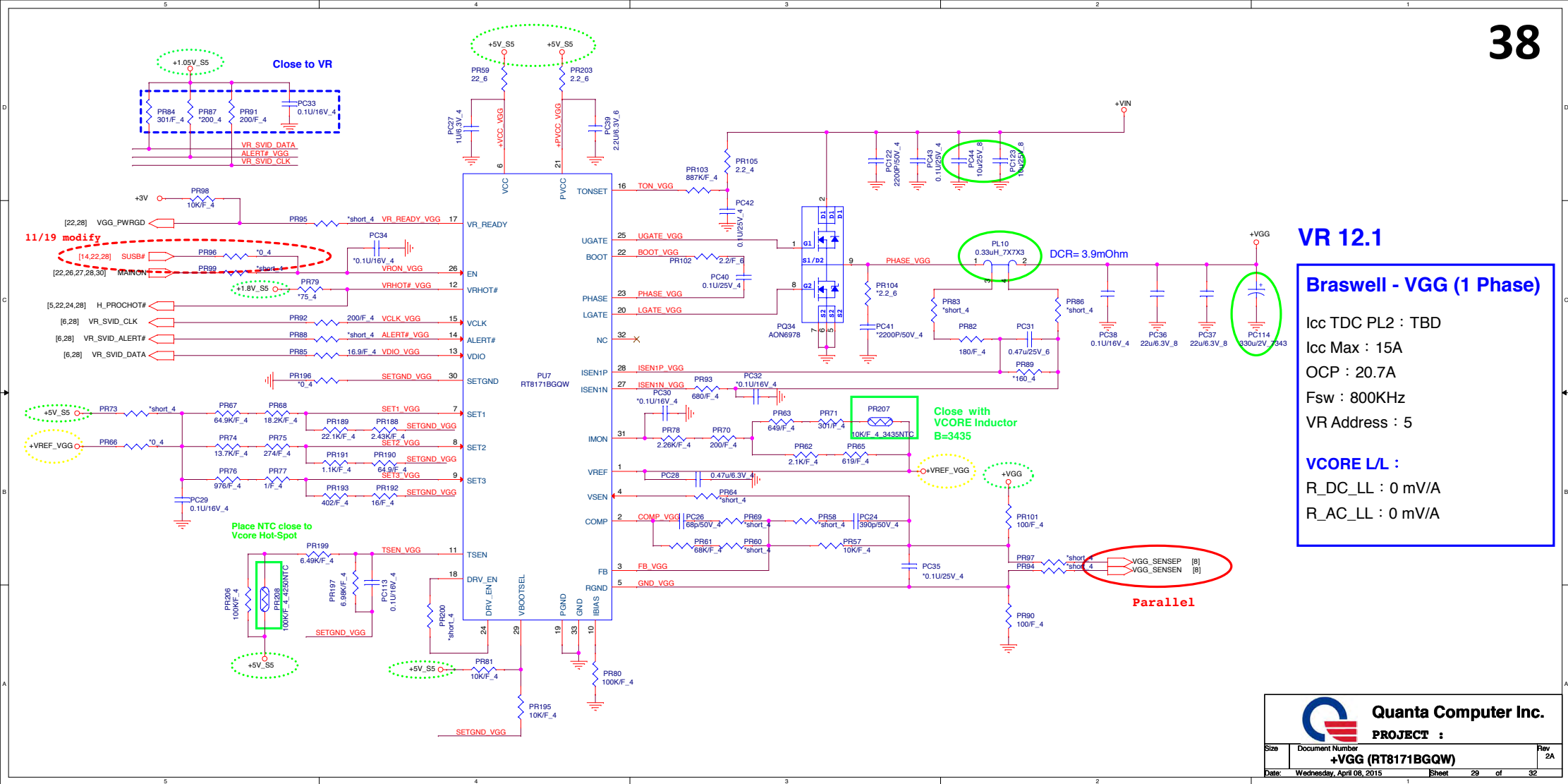
R\_AC\_LL : 0 mV/A

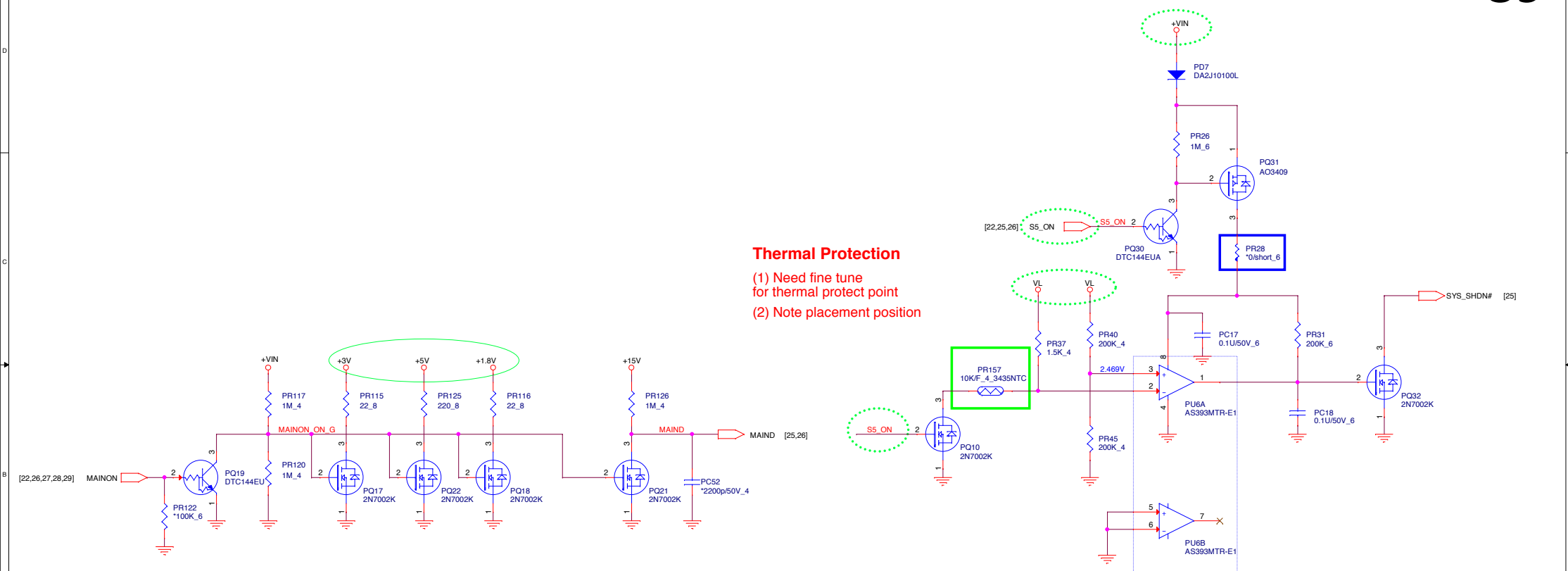


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PROJECT :

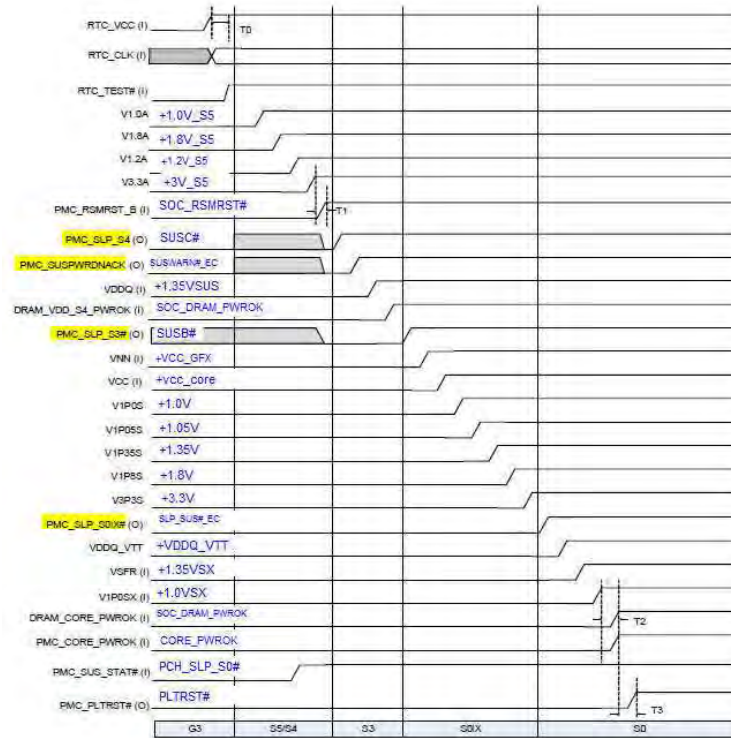
Size	Document Number	Rev
	VCC0+1 (RT817BGQW)	2A
Date:	Wednesday, April 08, 2015	Sheet 28 of 32





# Bay Trail-M S4/S5 to S0 (Power Up) Sequence

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Model	Version	CHANGE LIST
Z8AD	B	<p>1205</p> <p>page 6: change CPDQ_R337F not connect to SOC_R3CB_SMI not &amp; add R429</p> <p>page 12: change U13 pin34 connect to GND &amp; D4 PCIEB3TF not</p> <p>page 14: add Q24 &amp; R22</p> <p>page 19: D4 PCIEB3TF not &amp; change C214 connect +VFCU &amp; EMAC_WLANPWRM &amp; Q25 pin2 connect +3V_Mail_VDD</p> <p>page 20: D4 PCIEB3TF not</p> <p>page 21: add MAIN3TF not &amp; PC236</p> <p>1209</p> <p>page 6: add R581 connect to GND &amp; R585, PMU_WDT_RSTCLK_0 not</p> <p>page 14: add Q24 for Touch screen &amp; U13 circuit for Intel WDT card</p> <p>page 19: add WDT_RSTCLK not &amp; R584</p> <p>page 20: add XLP_239F not &amp; PC237 &amp; PC238 AMAS3TF not</p> <p>160</p> <p>page 6: Move SOC_R3CB_SMI to SATA_OP(pins A03)</p> <p>page 14: add R591</p> <p>page 15: add R594,R592,C594,R595</p> <p>page 16: D4 Q25,R579</p> <p>page 21: D4 Q25 &amp; add Q25,R592,R594,R595</p> <p>168</p> <p>page 3: D4 R515</p> <p>page 14: D4 R591</p> <p>page 6: D4 R499,R498 &amp; add C595,C596</p> <p>page 21: D4 R592</p>
	C	<p>1205</p> <p>page 6: add board ID 0 &amp; R800,R801</p> <p>page 22: add R802, R598 &amp; R599 AD4 R109</p> <p>30</p> <p>page 5: add OSD circuit OSD_PBSNTF connect to SATA_LEDW (134D A13) &amp; Add SSD ID at pin A07 (SATA_OP) Add R810,R811</p> <p>page 22: add R813</p> <p>page 16: add R812,C893 A0SD_PBSNTF not_SSD ID not</p> <p>page 22: add R814</p> <p>page 6: D4 R585 &amp; Add TP 24</p> <p>page 14: D4 U27,R583,R582,C583</p> <p>page 19: D4 R594 &amp; Add TP 47</p> <p>page 15: Add R815,R816,R817,C894,C895,C896</p> <p>page 16: Add R815,R816,R817,C894,C895,C896,C700,C702</p> <p>page 19: Add R821,R822,C894,C895</p>

DOC NO.

PROJECT MODEL


PART NUMBER:

APPROVED BY:

DRAWING BY:

DATE:

REVISION:



Quanta Computer Inc.

PROJECT : Z8AD

Change list

Project: Z8AD