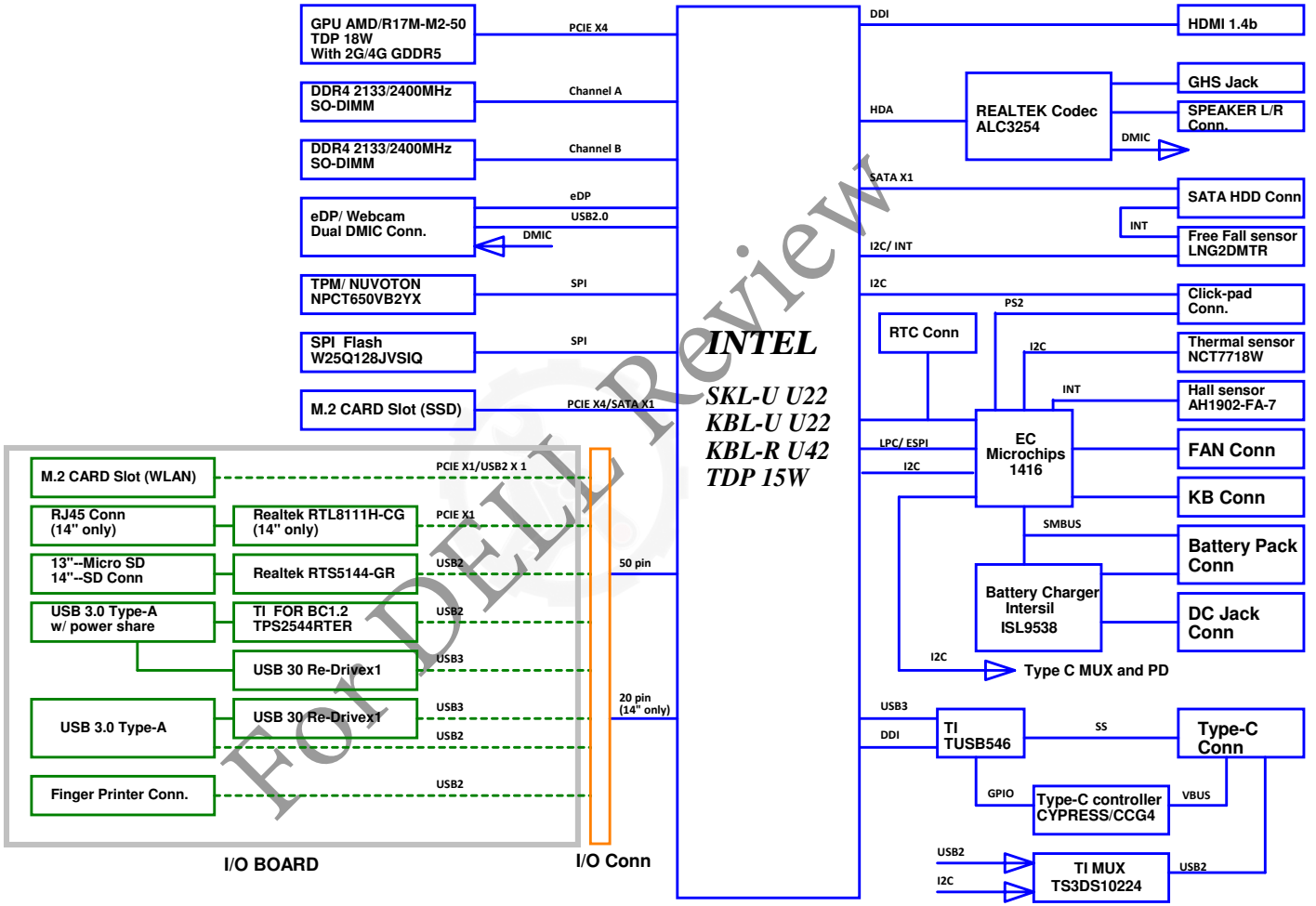
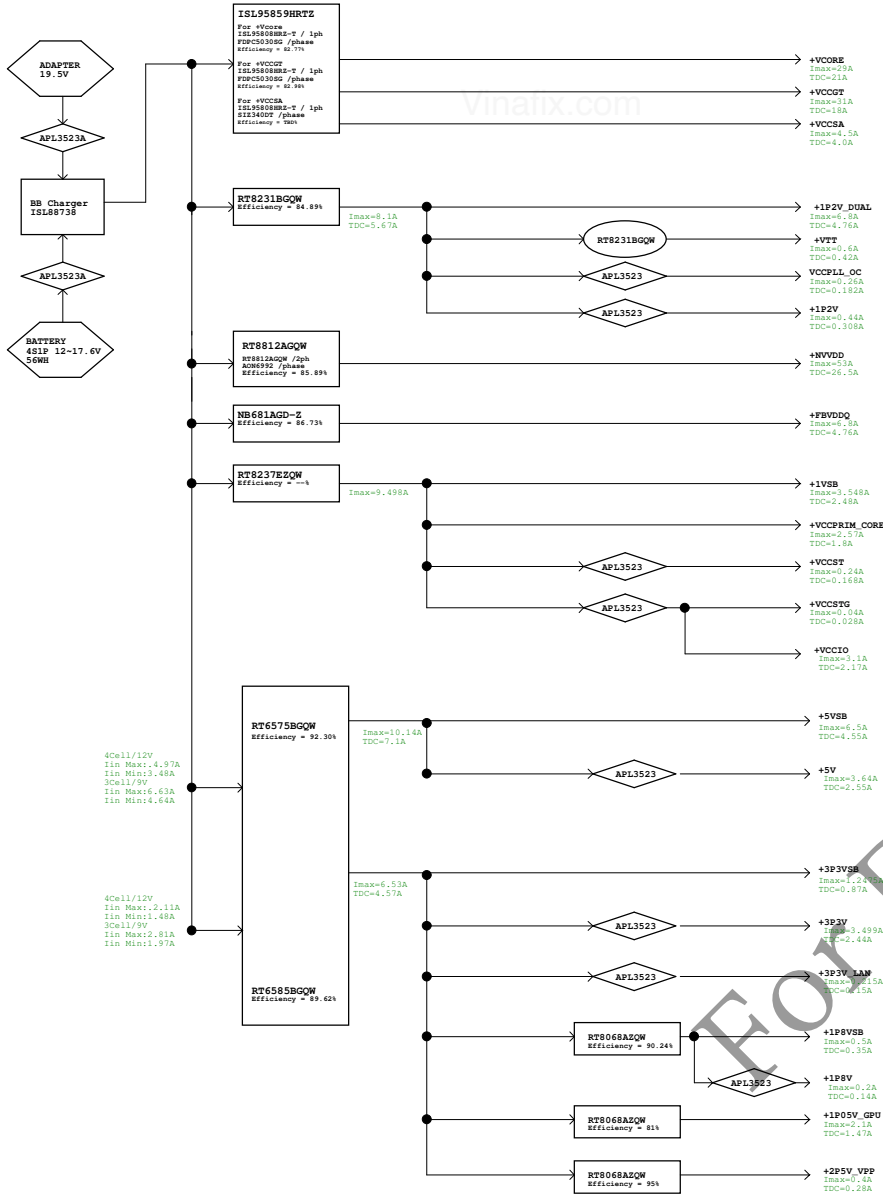
Block Diagram

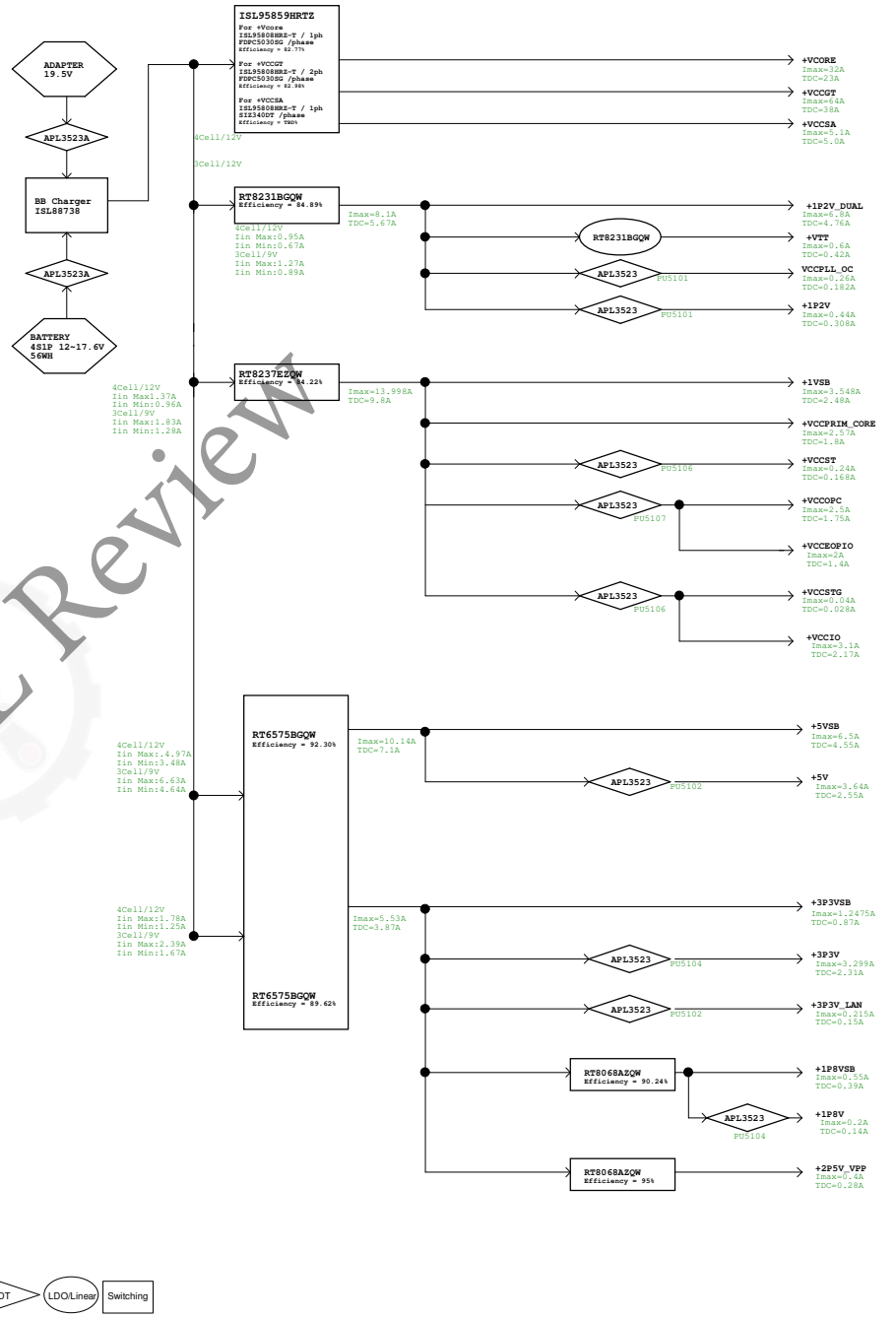


PEGATRON Title : BLOCK DIAGRAM
Pegatron Corp. Engineer: <OrgAddr1>
Size C | Project Name Loki/Armani | Rev A00
Date: Friday, August 25, 2017 Sheet 1 of 999

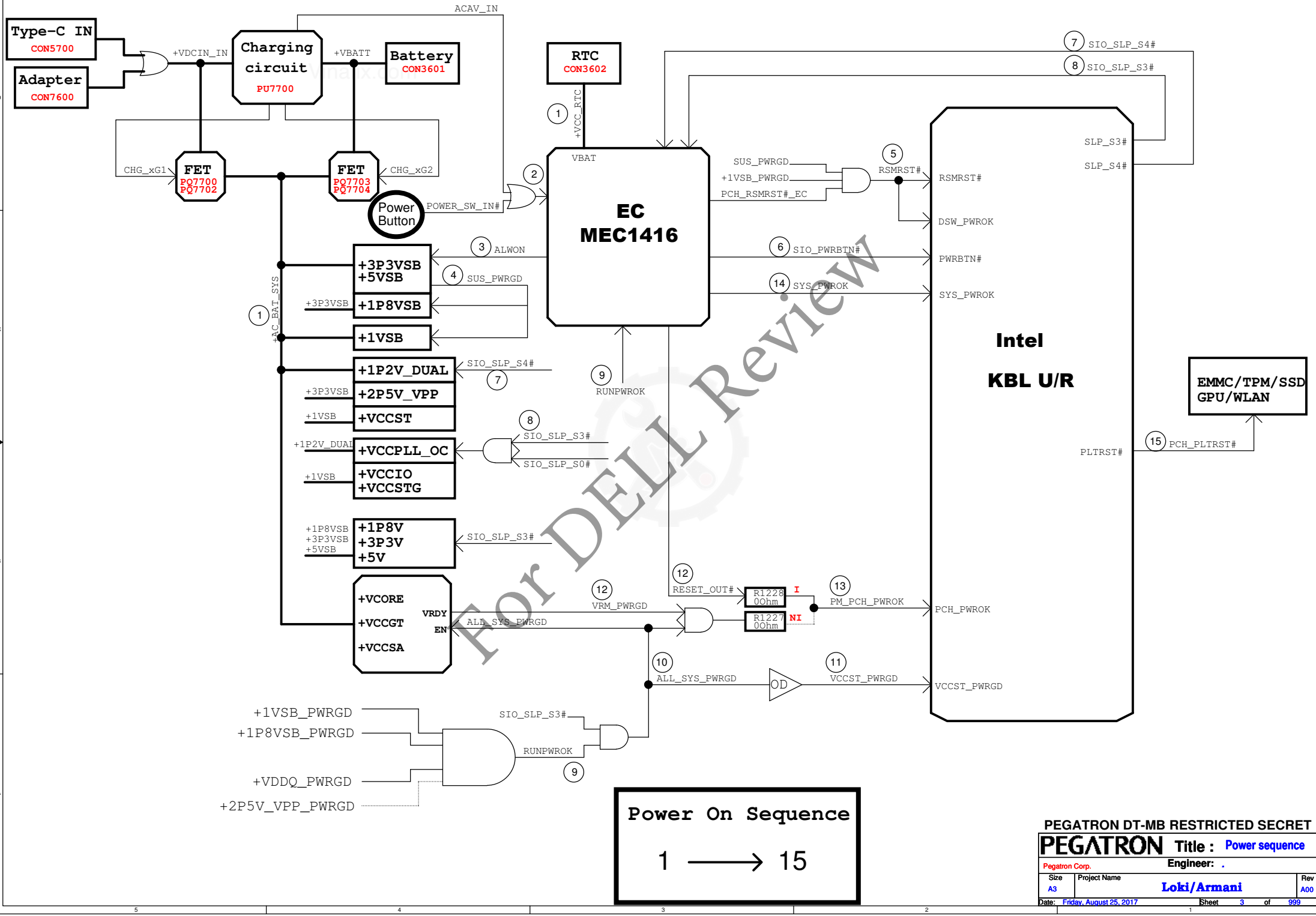
U22

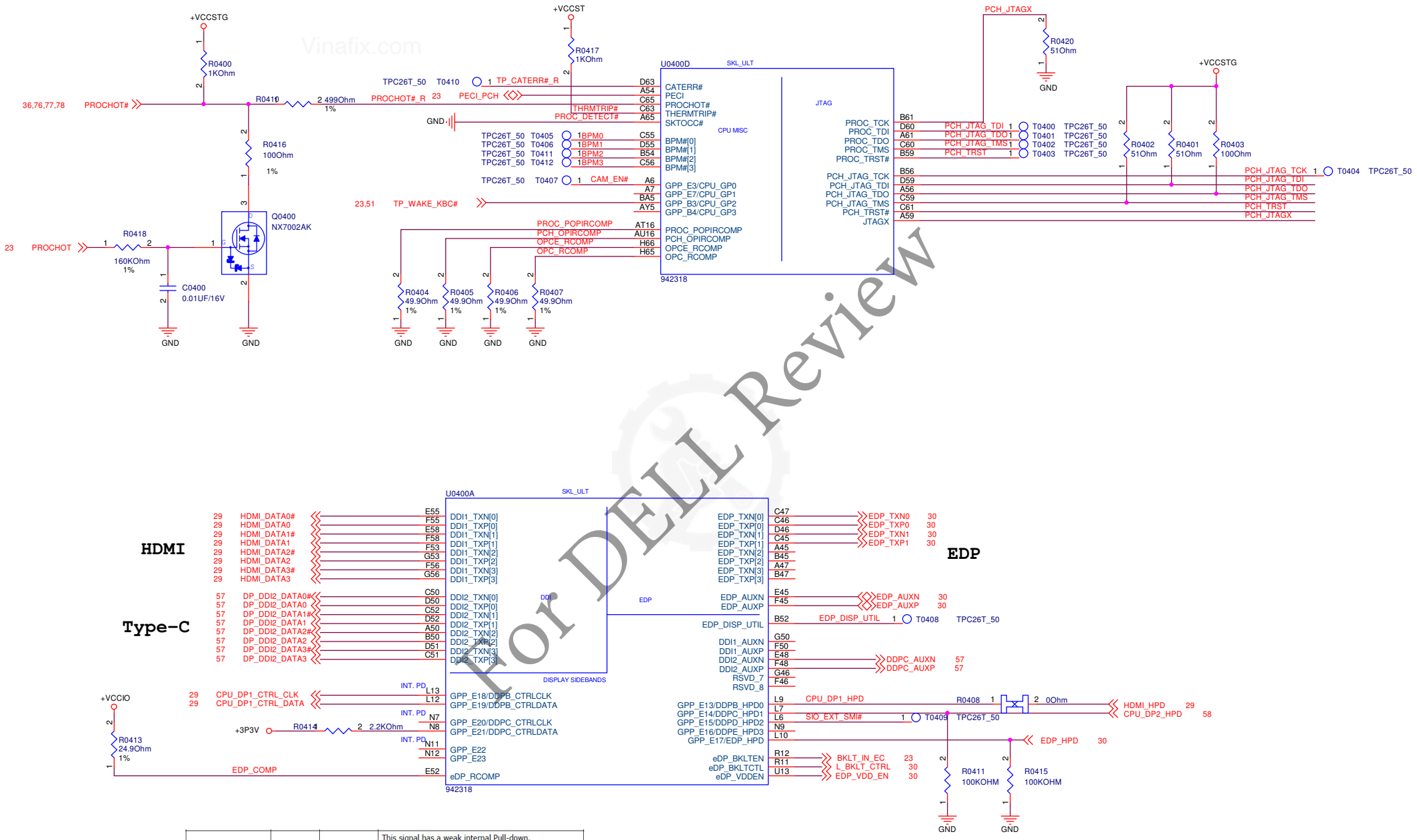


U23e



PEGATRON Title : POWER FLOW CHART
Engineer: -
Lolit/Armant


Type-C IN
CON5700
Adapter
CON7600
+VDCIN_IN
Charging circuit
PU7700
ACAV_IN
+VBATT
Battery
CON3601
RTC
CON3602
+VCC_RTC
CHG_xG1
FET
PQ7700
PQ7702
FET
PQ7703
PQ7704
CHG_xG2
Power Button
POWER_SW_IN#
VBAT
EC
MEC1416
ALWON
SUS_PWRGD
+AC_BAT_SYS
+3P3VSB
+5VSB
+1P8VSB
+1VSB
+1P2V_DUAL
+2P5V_VPP
+VCCST
+VCCPLL_OC
+VCCIO
+VCCSTG
+1P8V
+3P3V
+5V
SIO_SLP_S4#
SIO_SLP_S3#
SIO_SLP_S0#
RUNPWROK
+VCORE
+VCCGT
+VCCSA
VRDY
EN
VRM_PWRGD
ALL_SYS_PWRGD
RESET_OUT#
R1228 0Ohm
R1227 0Ohm
NI
PM_PCH_PWROK
OD
VCCST_PWRGD
+1VSB_PWRGD
+1P8VSB_PWRGD
+VDDQ_PWRGD
+2P5V_VPP_PWRGD
SUS_PWRGD
+1VSB_PWRGD
PCH_RSMRST#_EC
RSMRST#
SIO_PWRBTN#
SYS_PWROK
PCH_PWROK
PLTRST#
PCH_PLTRST#
SLP_S3#
SLP_S4#
DSW_PWROK
PWRBTN#
Intel
KBL U/R
EMMC/TPM/SSD
GPU/WLAN
Power On Sequence
1 ⟶ 15
For DELL Review
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : Power sequence
Pegatron Corp.
Engineer: .
Size A3
Project Name Loki/Armani
Rev A00
Date: Friday, August 25, 2017
Sheet 3 of 999



DDPC_CTRLDATA/ GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU(1)_MISC,JTAG,DDI,

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 4 of 999

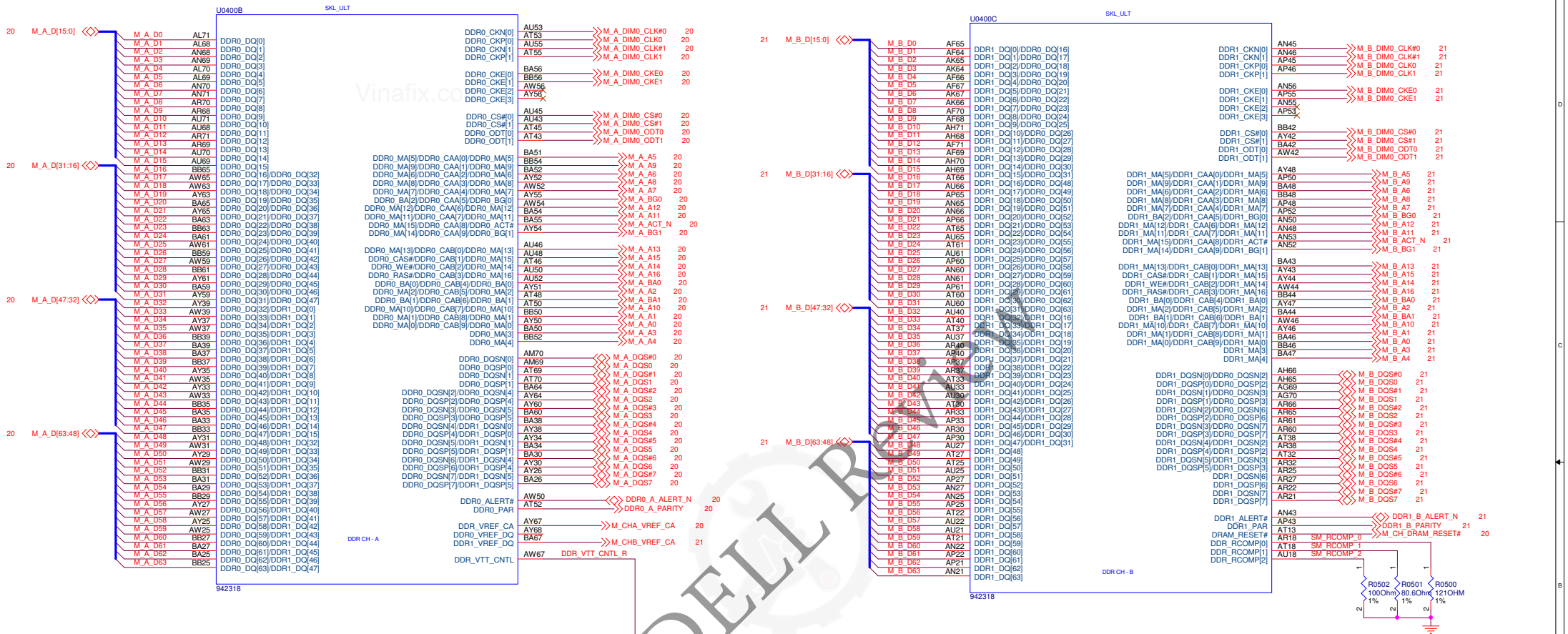
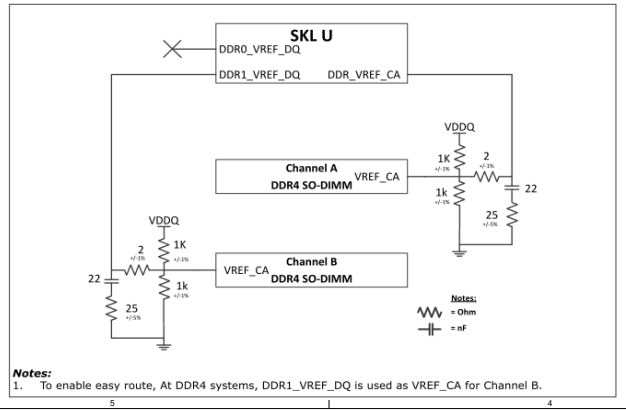


Figure 4-45. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



Notes:

1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

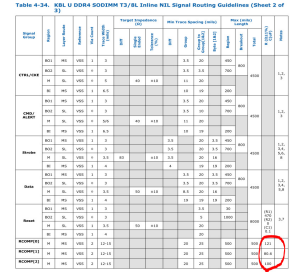
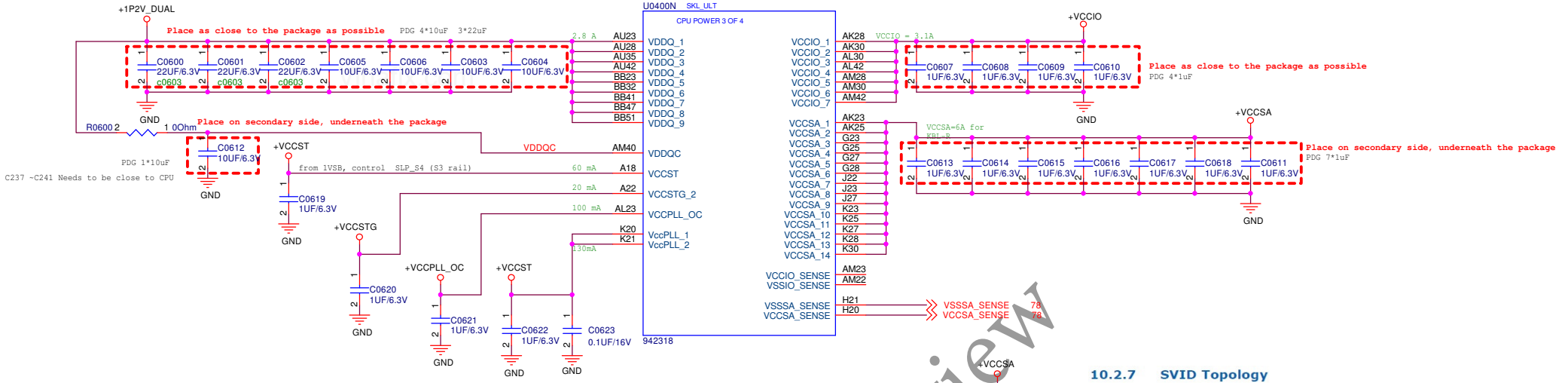
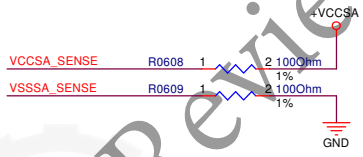


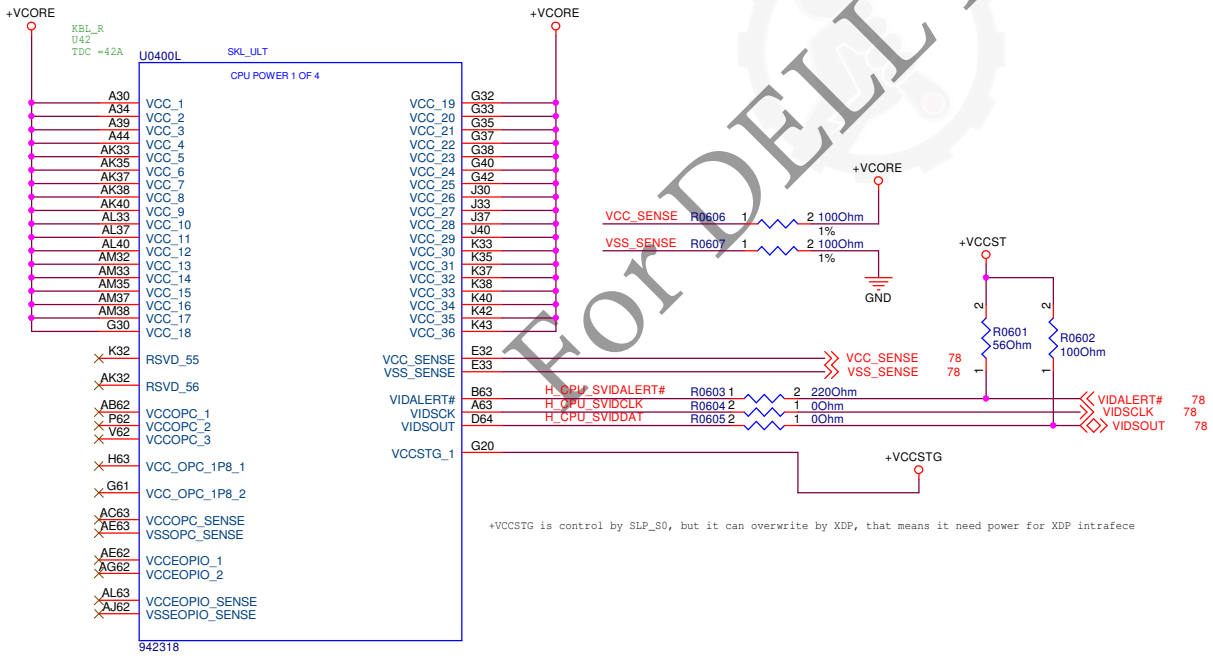
Table 4-34. KBL U DDR4 SODIMM T3/8L Inline NIL Signal Routing Guidelines (Sheet 2 of 4)

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : CPU(2)_DDR4		
Pegatron Corp.	Engineer: .		
Size: Custom	Project Name: Loki/Armani		Rev: A00
Date: Friday, August 25, 2017	Sheet 5 of 999		







+VCCSTG is control by SLP_S0, but it can overwrite by XDP, that means it need power for XDP intrafece

10.2.7 SVID Topology

Figure 10-5. Routing Illustration for SVID Topology

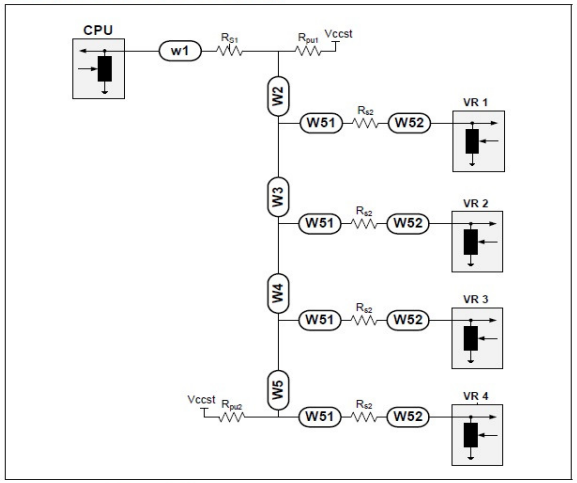


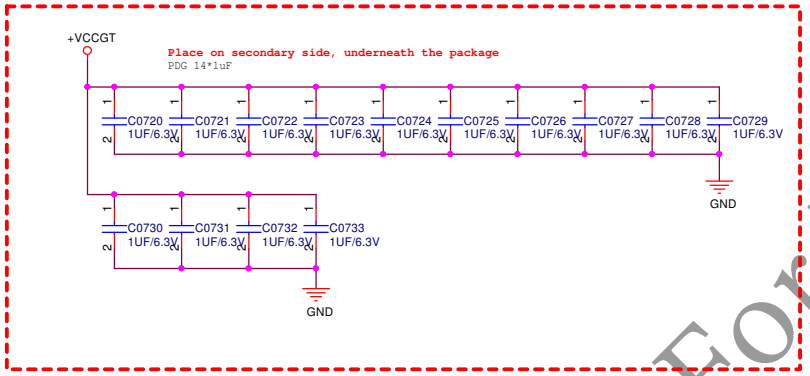
Table 10-8. SVID Bus Routing Guidelines

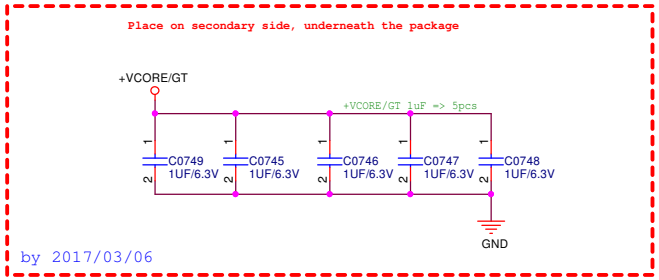
Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{PU1} [Ω]	R_{PU2} [Ω]	R_{G1} [Ω]	R_{G2} [Ω]	VCC_{ST} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

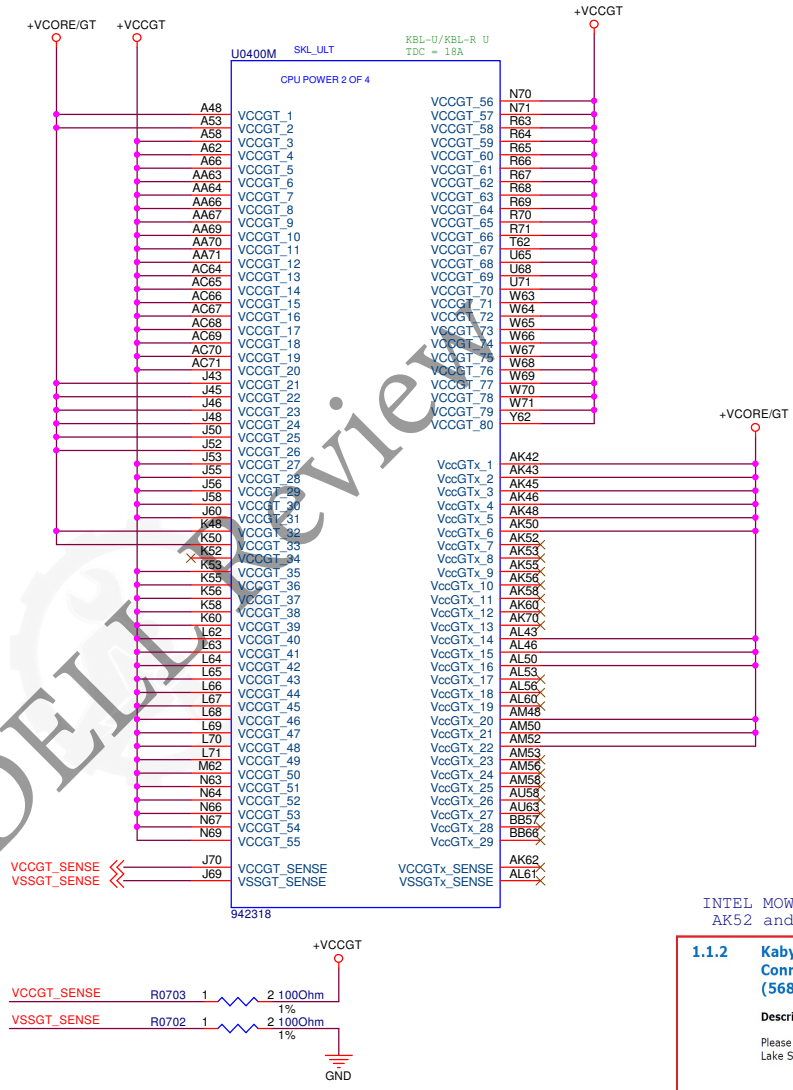
Note: For additional information regarding SVID and power management refer to Chapter 47, "Power Architecture Guide" in this document.

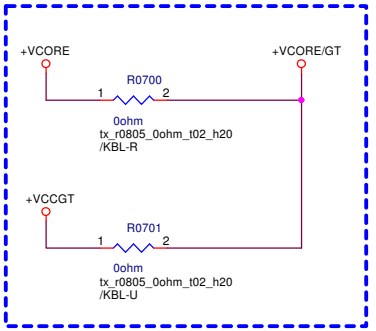
Table 10-9. SVID Minimum Spacing Guidelines

Coupling length [inches]	Stripline [mils]	Microstrip [mils]
<0.5	5	5
<2.5	10	10
>2.5	12	15









INTEL MOW WW09, March 2017 update
AK52 and K52 Keep NC

1.1.2 Kaby Lake U AK52 and K52 Kaby Lake Silicon Ball Connectivity Recap from PDG (568813_KBL_R_U42_PDG_Addendum_Rev0p9, Page 12)

Description:

Please ensure to follow the below Connectivity guidelines on AK52 and K52 Kaby Lake Silicon Balls for Compatible Design (KBL-R U42/KBL U22/KBL U23e).

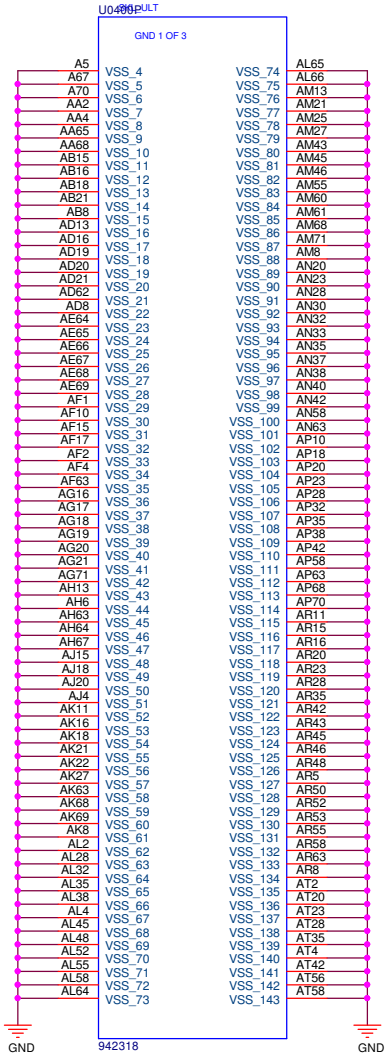
KBL-R U42 Only Design	Do not Connect AK52 and K52 Balls, Keep as NC
KBL-R U42 Compatible Design for (KBL-R U42/KBL U22/KBL U23e) Support	Do not Connect AK52 and K52 Balls, Keep as NC

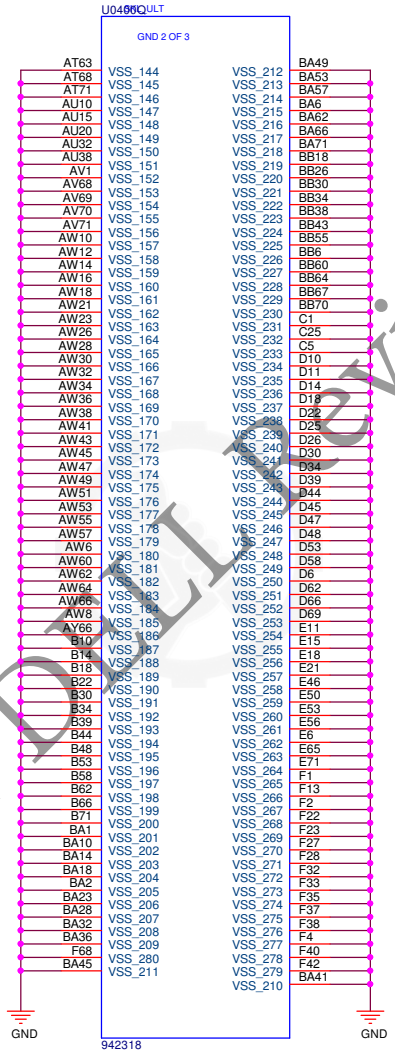
PEGATRON Title : CPU(4)_SKL_POWER2

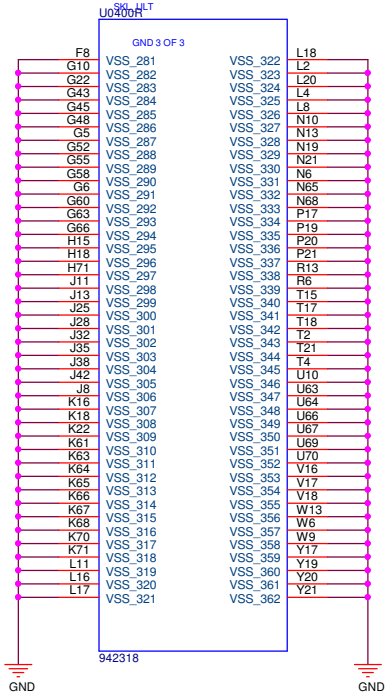
Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 7 of 999



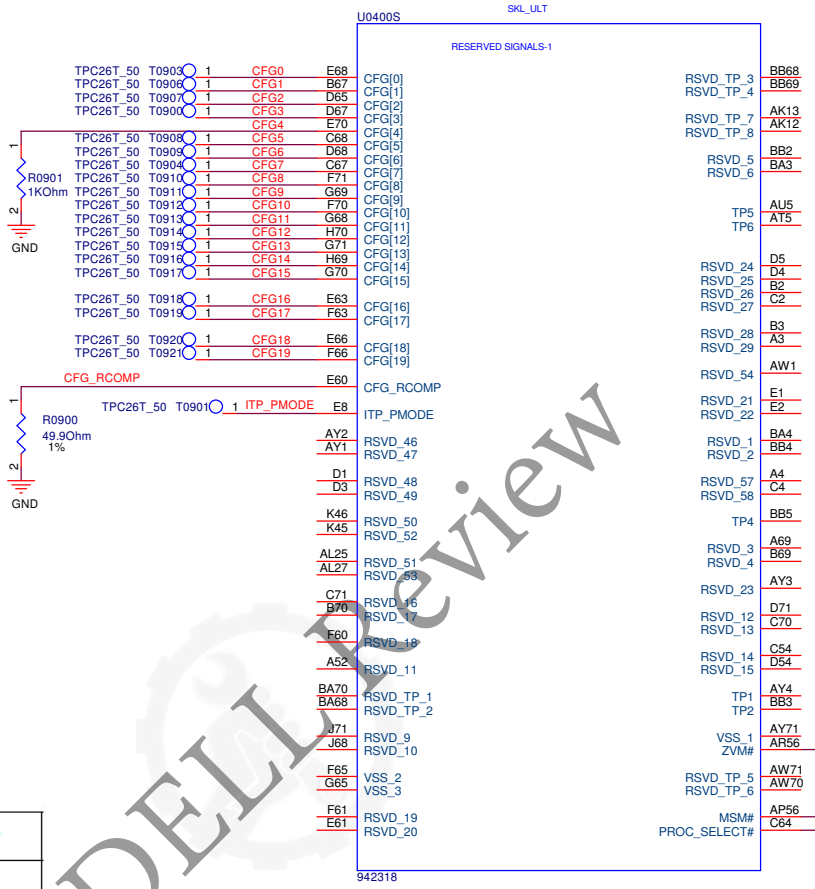




PEGATRON DT-MB RESTRICTED SECRET

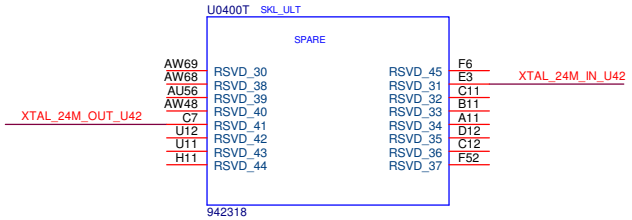
PEGATRON	Title : CPU(5)_GND	
Pegatron Corp.	Engineer: .	
Size: A3	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 8 of 999	

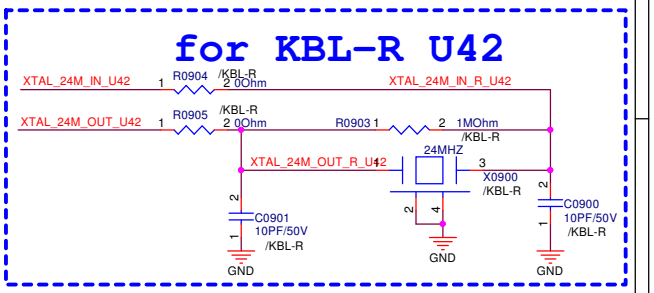
CFG4	
0 **Default**	Enable eDP
1	Disable eDP



Signal Name	Description
Vss	Processor ground node
Vss_NCTF	**Non-Critical To Function:** These signals are for package mechanical reliability.
RSVD RSVD_NCTF RSVD_TP	**Reserved:** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. Intel recommends that all RSVD_TP signals have via test points.

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[19:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP* enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[7]:** PEG Training: — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • **CFG[19:8]:** Reserved configuration lanes.	I	GTL	SE	All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them.
CFG_RCOMP	**Configuration Resistance Compensation**	N/A	N/A	SE	All processor lines
PROC_POPIRCOMP	**POPIO Resistance Compensation**	N/A	N/A	SE	Y and U-processor line
RESET#	Platform Reset pin driven by the PCH.	I	CMOS	SE	H and S-processor line
PROC_SELECT#	**Processor Select:** This pin is for compatibility with future platforms. It should be unconnected for KBL.			N/A	All processor lines





Ball #	Ball Names R-U42	Ball Names U22
C7	XTAL24_OUT	NC
E3	XTAL24_IN	NC
E35	NC	XTAL24_OUT
E37	NC	XTAL24_IN

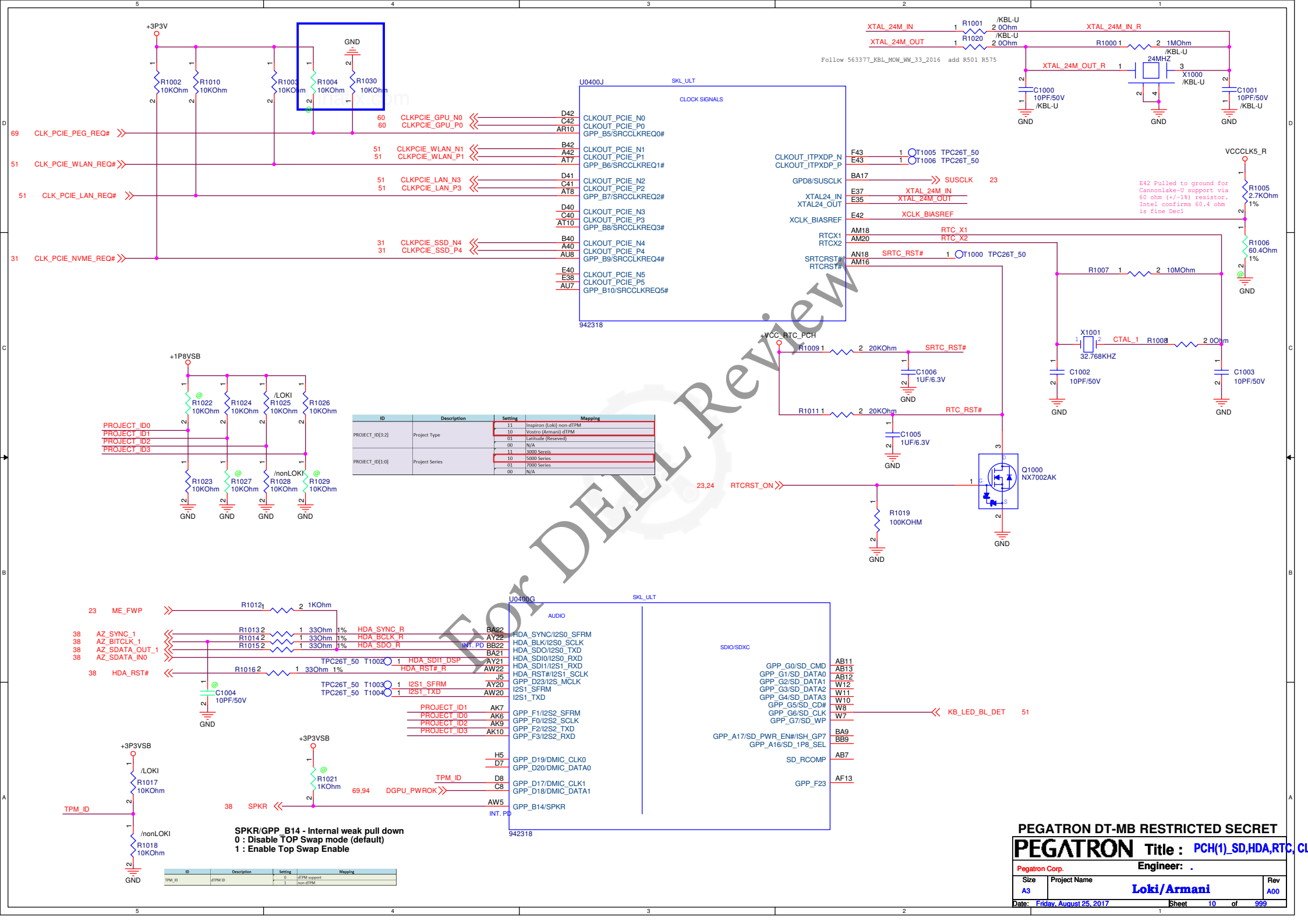
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU(6)_CFG_RESERVED

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 9 of 999



GPP_C2/SMBALERT#	
0 **Default**	Disable ME crypto TLS
1	Enable ME crypto TLS

GPP_C5/SML0ALERT#	
0 **Default**	LPC **(EC)**
1	eSPI **(EC)**

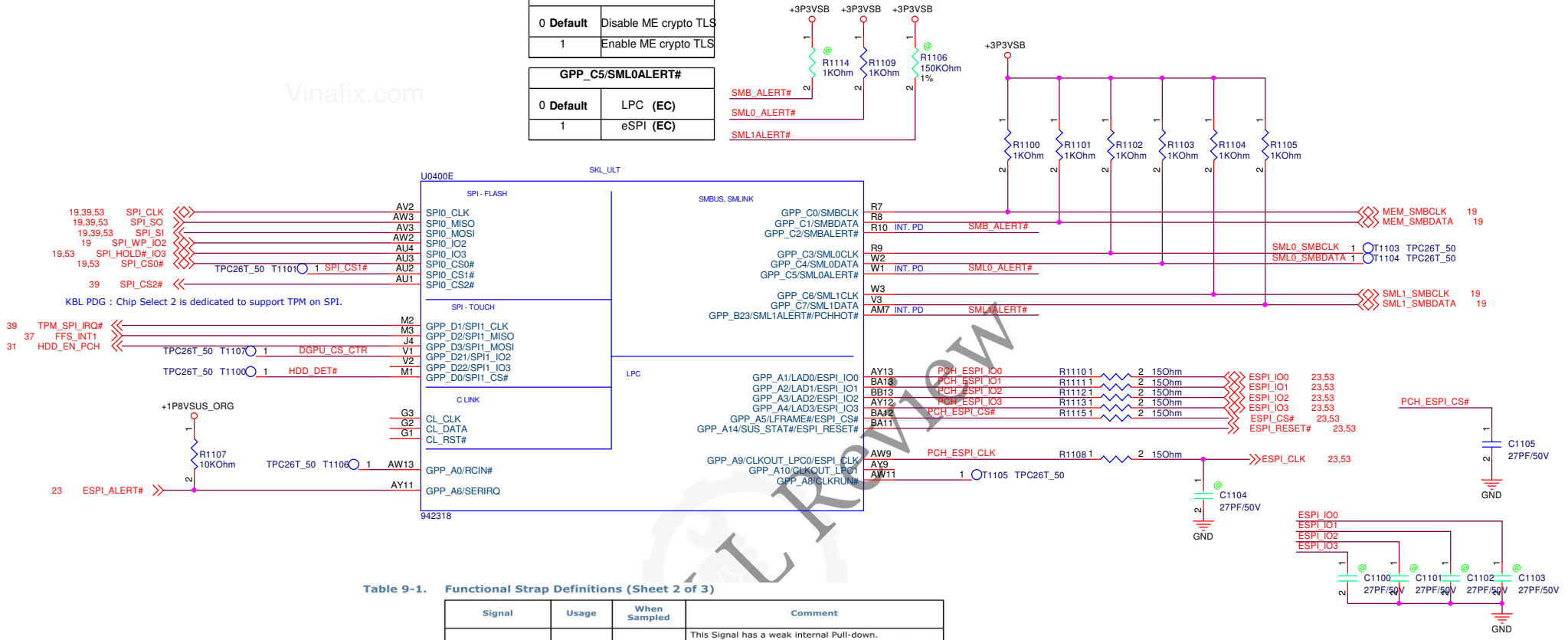


Table 9-1. Functional Strap Definitions (Sheet 1 of 3)

Signal	Usage	When Sampled	Comment
SPKR/GPP_B14	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal Pull-down. 0 = **Disable** "Top Swap" mode. (Default) 1 = **Enable** "Top Swap" mode. This inverts an address on access to SPI and firmware hub, so the processor believes it fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64-KB blocks in the FWH or the appropriate address lines (A16, A17, or A18) as selected in Top Swap Block size soft strap (See SPI Flash Programming Guide). ***Notes:*** 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. Software will not be able to clear the Top Swap bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Bus0, Device31, Function0, offset DCh, bit4). 4. This signal is in the primary well.
GSPI0_MOSI/ GPP_B18	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal Pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
SMBALERT#/ GPP_C2	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS. ***Notes:*** 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). **Bit 6** — **Boot BIOS Destination** 0 — SPI (Default) 1 — LPC ***Notes:*** 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT#/ GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = **LPC** Is selected for EC. (Default) 1 = **eSPI** Is selected for EC. ***Notes:*** 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
SPI0_MOSI	Reserved	Rising edge of RSMRST#	This signal has an internal Pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	Reserved	Rising edge of RSMRST#	This signal has an internal Pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SML1ALERT#/ PCHHOT#/ GPP_B23	Reserved	Rising edge of RSMRST#	This signal has an internal Pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Note:*** When used as PCHHOT#, a 150k weak board Pull-up is recommended to ensure it does not override the internal Pull-down strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	This signal has an internal Pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	This signal has an internal Pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Table 9-1. Functional Strap Definitions (Sheet 3 of 3)

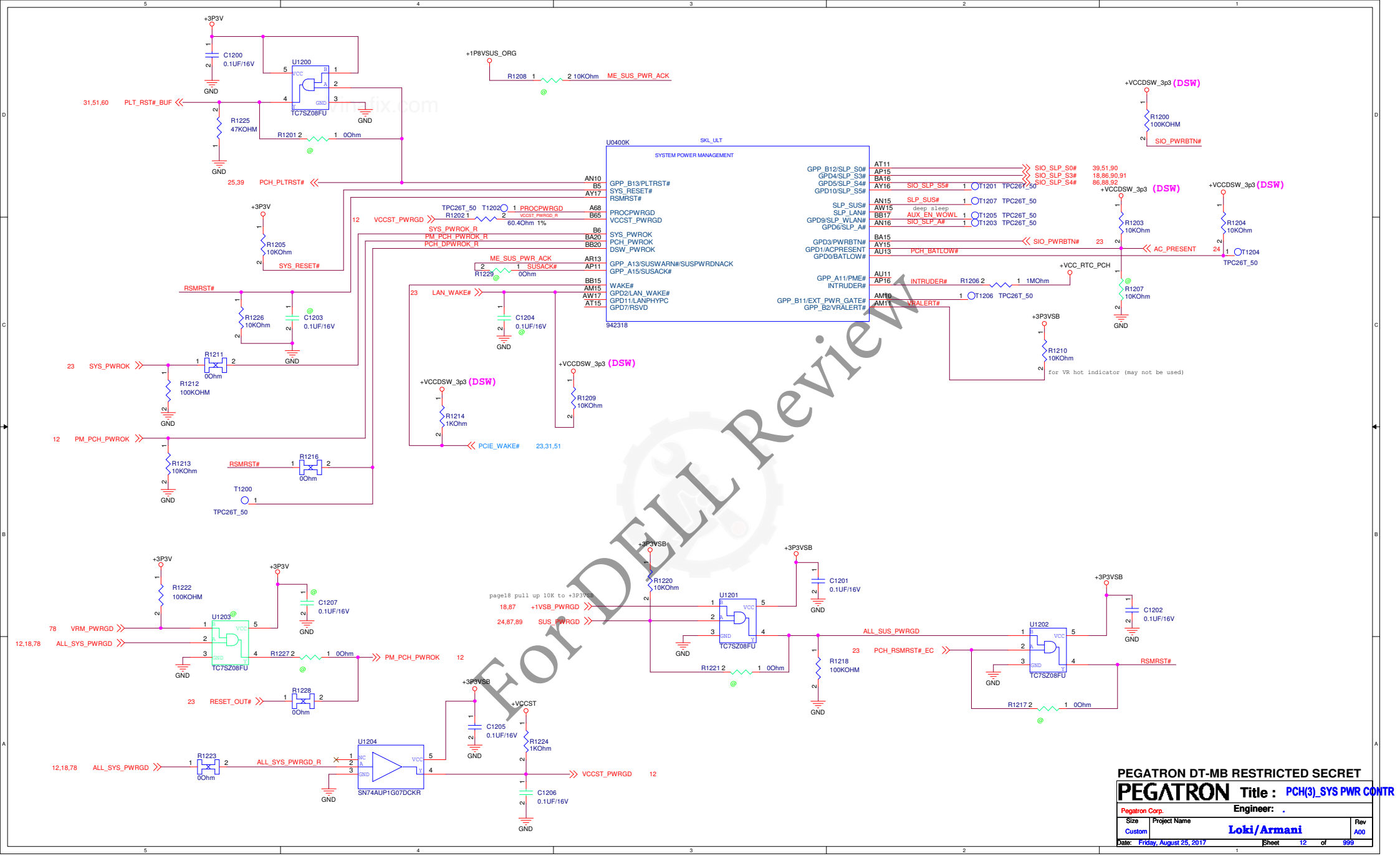
Signal	Usage	When Sampled	Comment
HDA_SDO / I2S_TXD0	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. Asserting HDA_SDO high on the rising edge of PCH_PWROK will also halt Intel Management Engine after Chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the primary well.
DDPB_CTRLDATA/ GPP_E19	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.
DDPC_CTRLDATA/ GPP_E21	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. This signal is in the primary well.

PEGATRON Title : PCH(2)_CLK,SMB,LPC, S

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 11 of 999



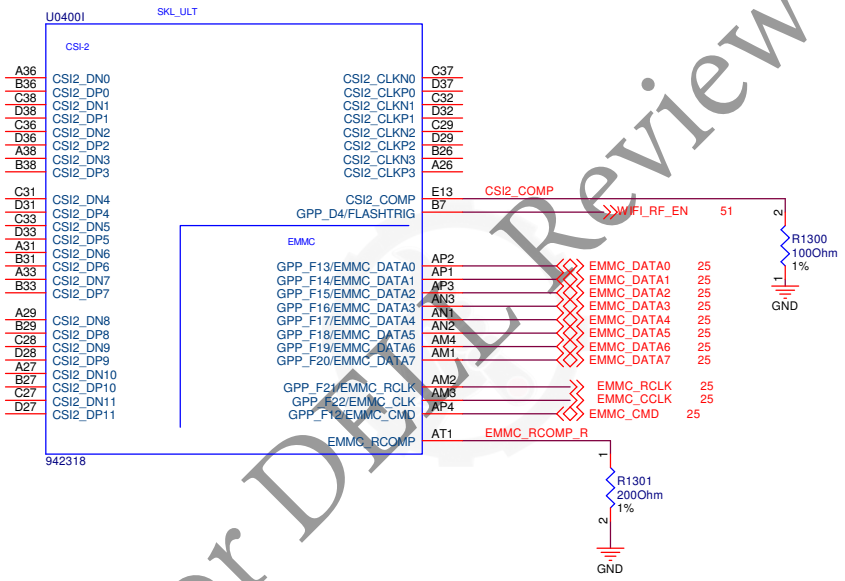
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH(3)_SYS PWR CONTR

Pegatron Corp. Engineer: .

Size	Project Name	Rev
Custom	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 12 of 999



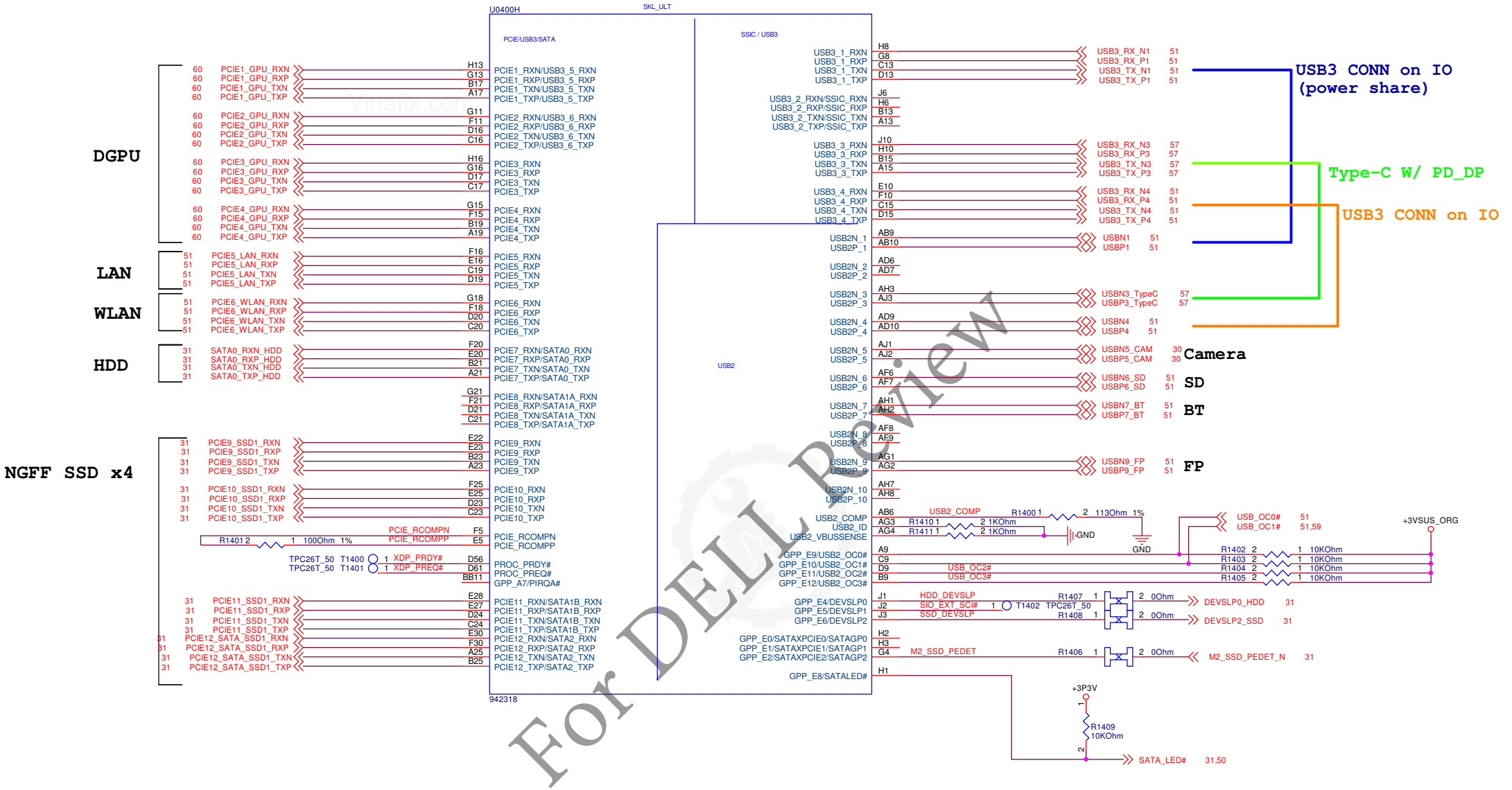
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH(4)_CCI, HWID

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 13 of 999



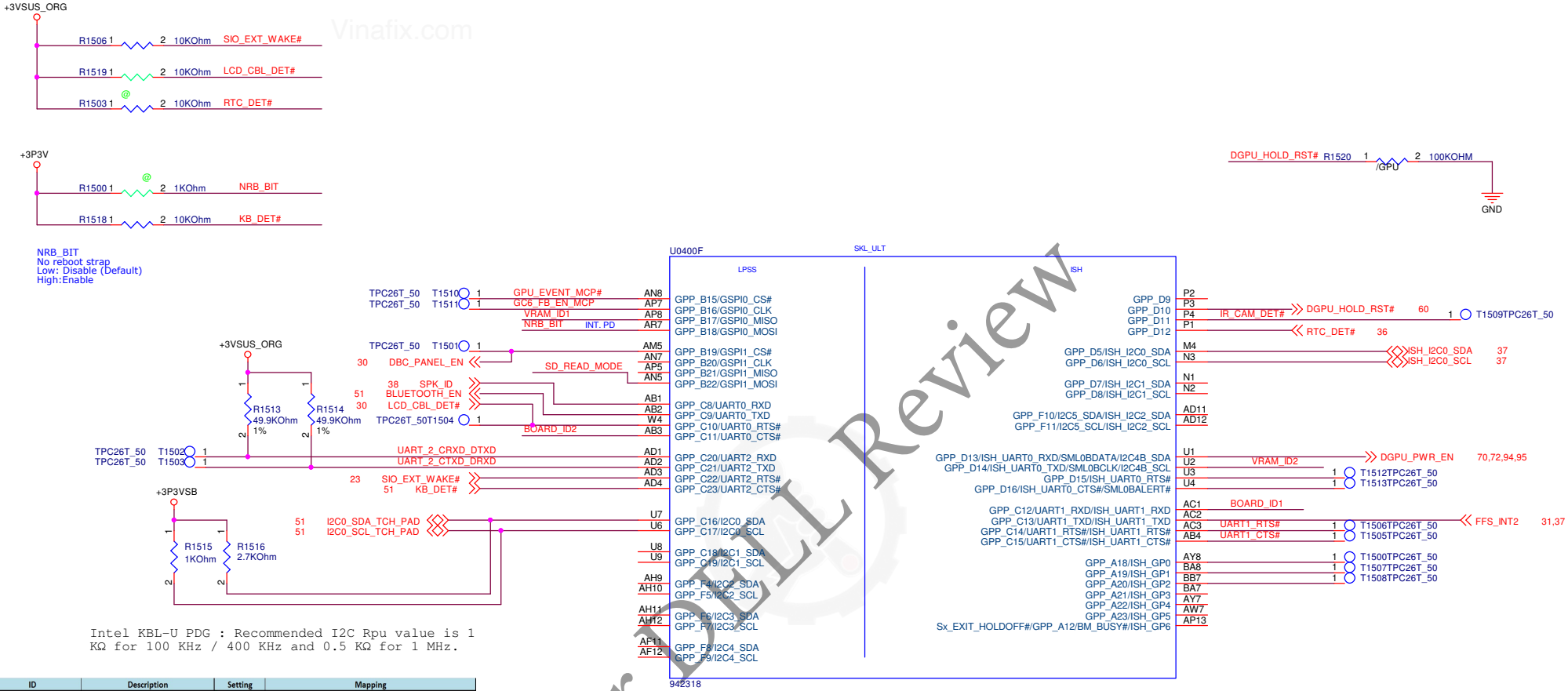
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH(5)_PCIE,USB

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 14 of 999

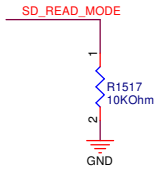


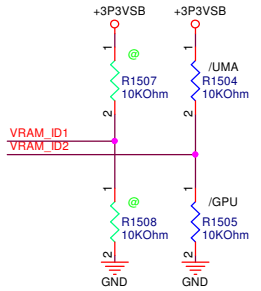
Intel KBL-U PDG : Recommended I2C Rpu value is 1 KΩ for 100 KHz / 400 KHz and 0.5 KΩ for 1 MHz.

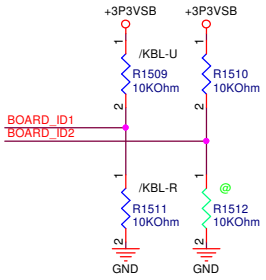
ID	Description	Setting	Mapping
MEM_CONFIG[4:3]	On-board memory configuration for chip vendor	11	DIMM Design
		10	Micron
		01	Hynix
		00	Samsung
MEM_CONFIG[2:1]	On-board memory configuration for total memory size per channel	11	N/A
		10	16GB
		01	8GB
		00	4GB
MEM_CONFIG[0]	SDP/DDP Configuration	1	SDP (Singel Die per Package)
		0	DDP (Dual Die per Package)

GPP_B22 : Boot BIOS Strap
Sampled on rising edge of PWROK.

Boot BIOS Strap	
GPP_B22	Boot BIOS Location
1	LPC
0	SPI **(PCH)**







ID	Description	Setting	Mapping
VRAM_ID[2:1]	dGPU VRAM size	11	UAM Board
		10	N/A
		01	DIS Board with 4GB VRAM
		00	DIS Board with 2GB VRAM

ID	Description	Setting	Mapping
BOARD_ID[2:1]	Board SKU ID	11	KBL-U
		10	KBL-R
		01	N/A
		00	SKL-U

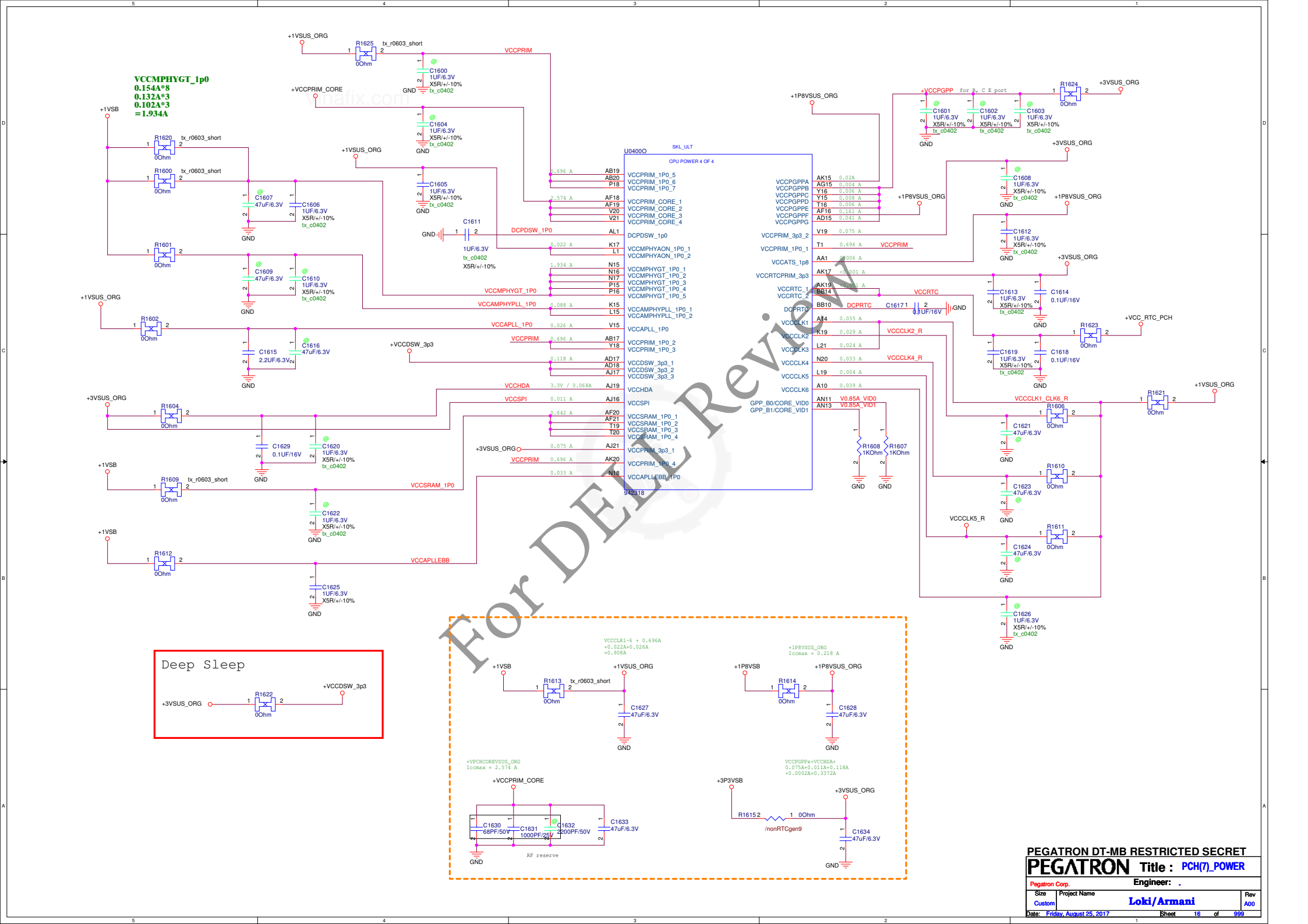
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCH(6)_CPU,GPIO,MISC

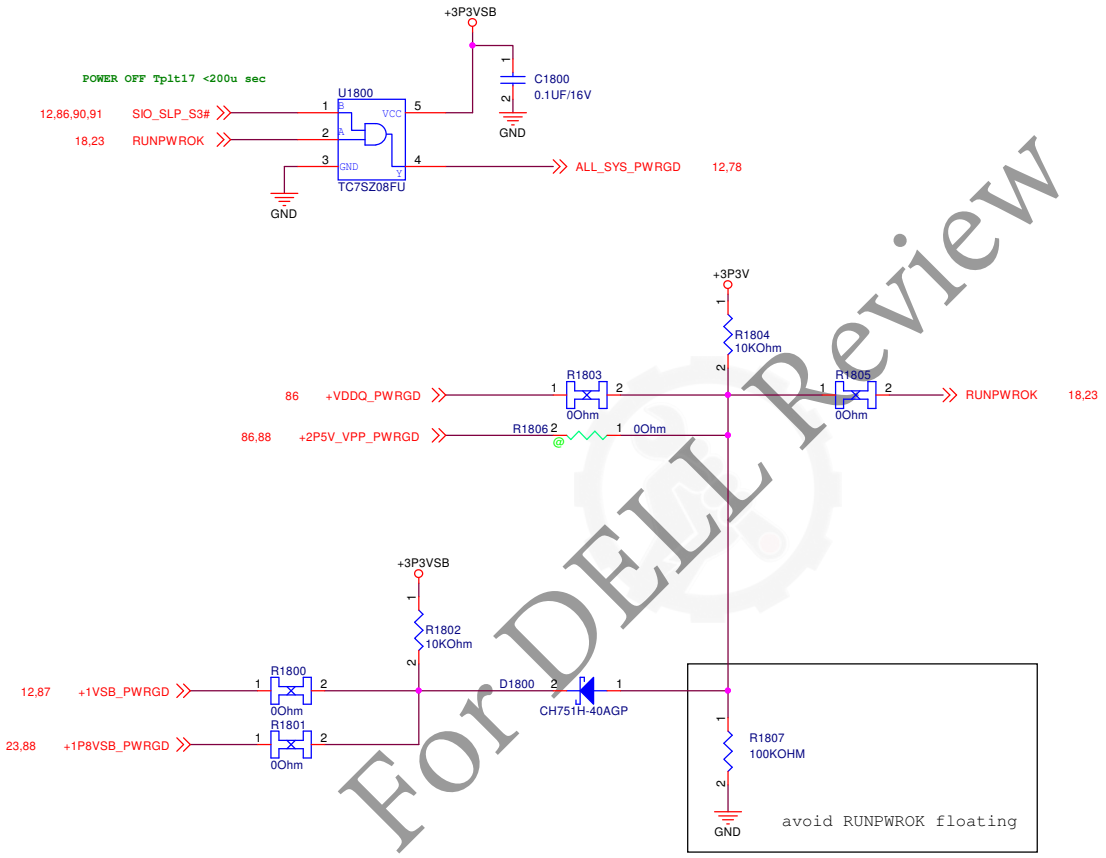
Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 15 of 999



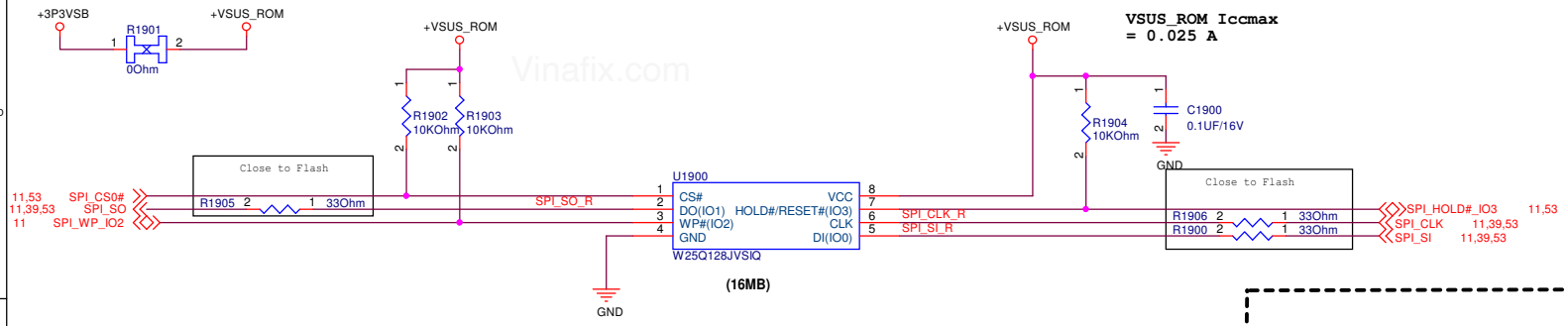
POWER GOOD DETECTER



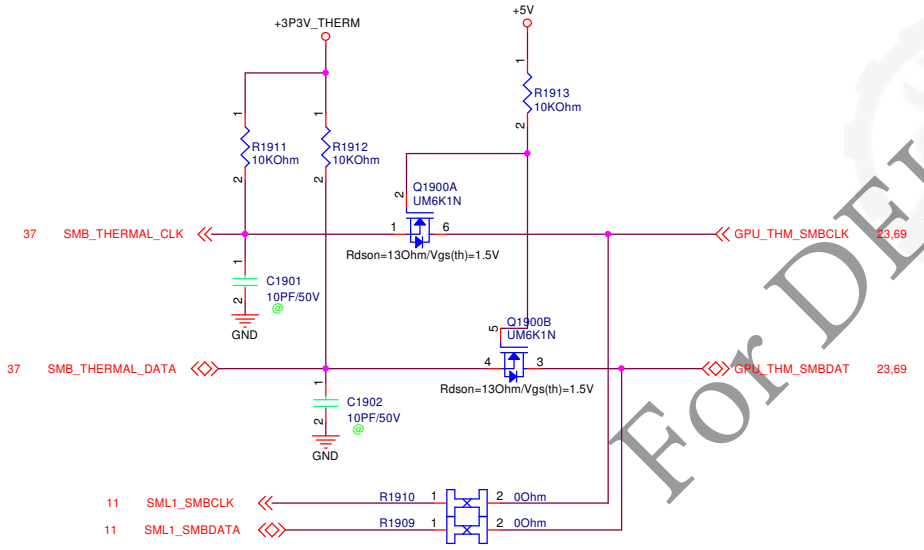
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PWRGD DETECT	
Pegatron Corp.	Engineer: .	
Size: A3	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 18 of 999	

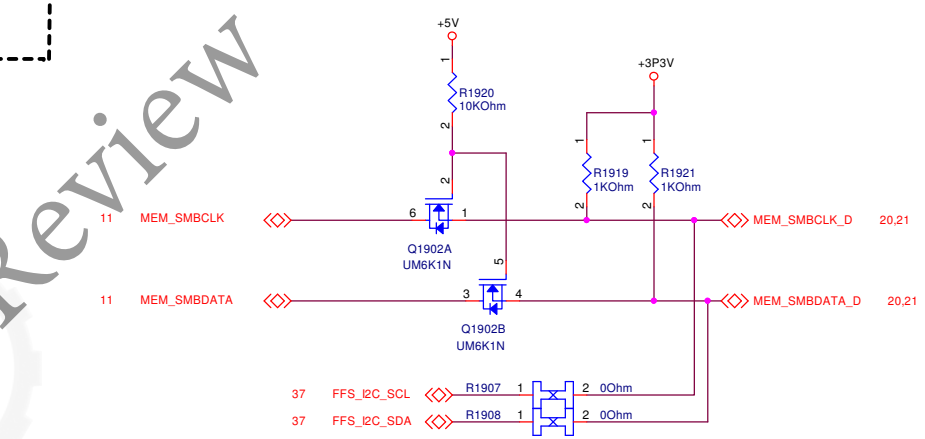
SPI ROM (Quad I/O Supported)

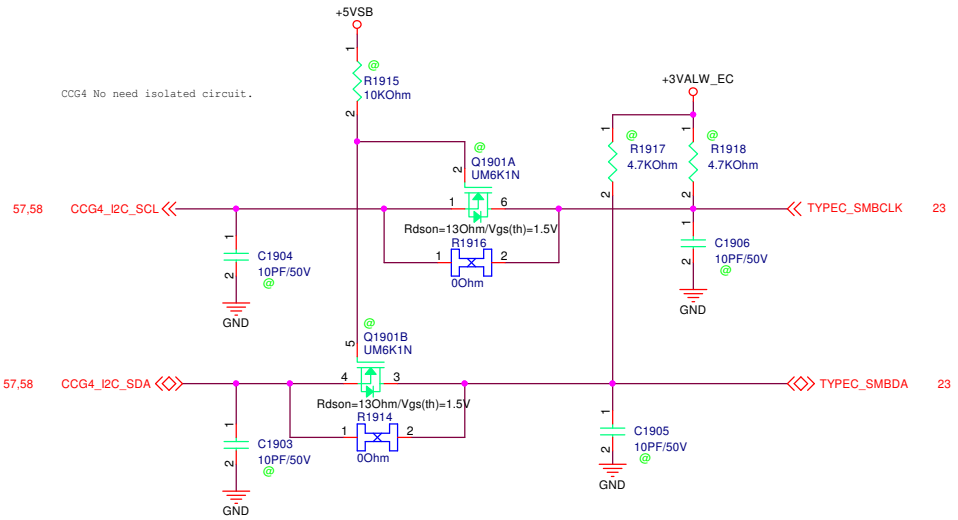


SM BUS



PCH side pull high +3P3VSB 1K





PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : SPI ROM & SM BUS	
Pegatron Corp.	Engineer: .	
Size: A3	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 19 of 999	

SO-DIMM CHA

DRAM reset

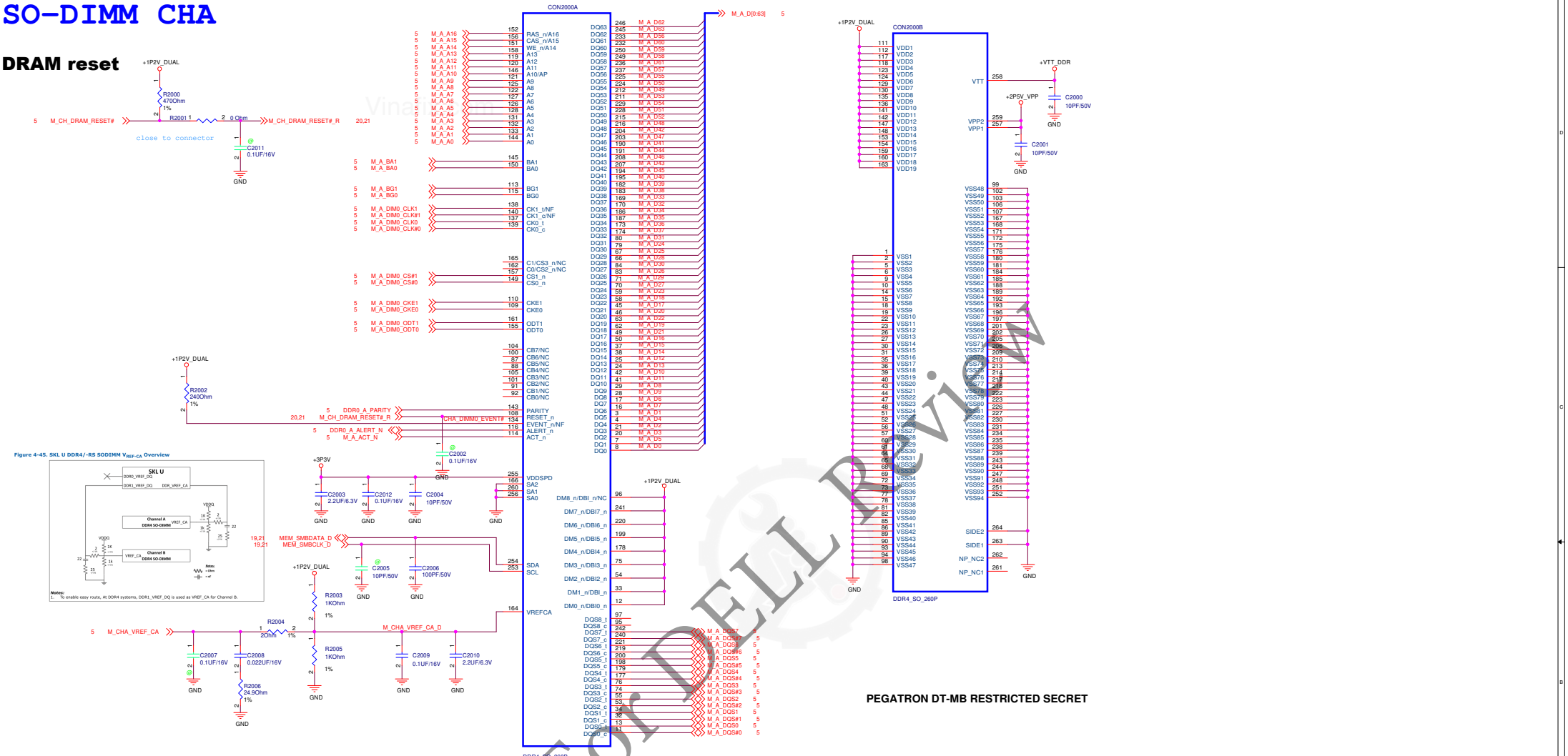


Figure 4-45. SKL U DDR4/-RS SODIMM V_{REF_CA} Overview

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DDR4_SO-DIMM0		
Pegatron Corp.	Engineer: .		
Size: A2	Project Name: Loki/Armani		Rev: A00
Date: Friday, August 25, 2017	Sheet 20 of 999		

SO-DIMM CHB

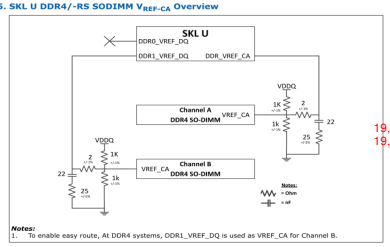


Figure 4-45. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview

CON2100A

DDR4_SO_260P

CON2100B

DDR4_SO_260P

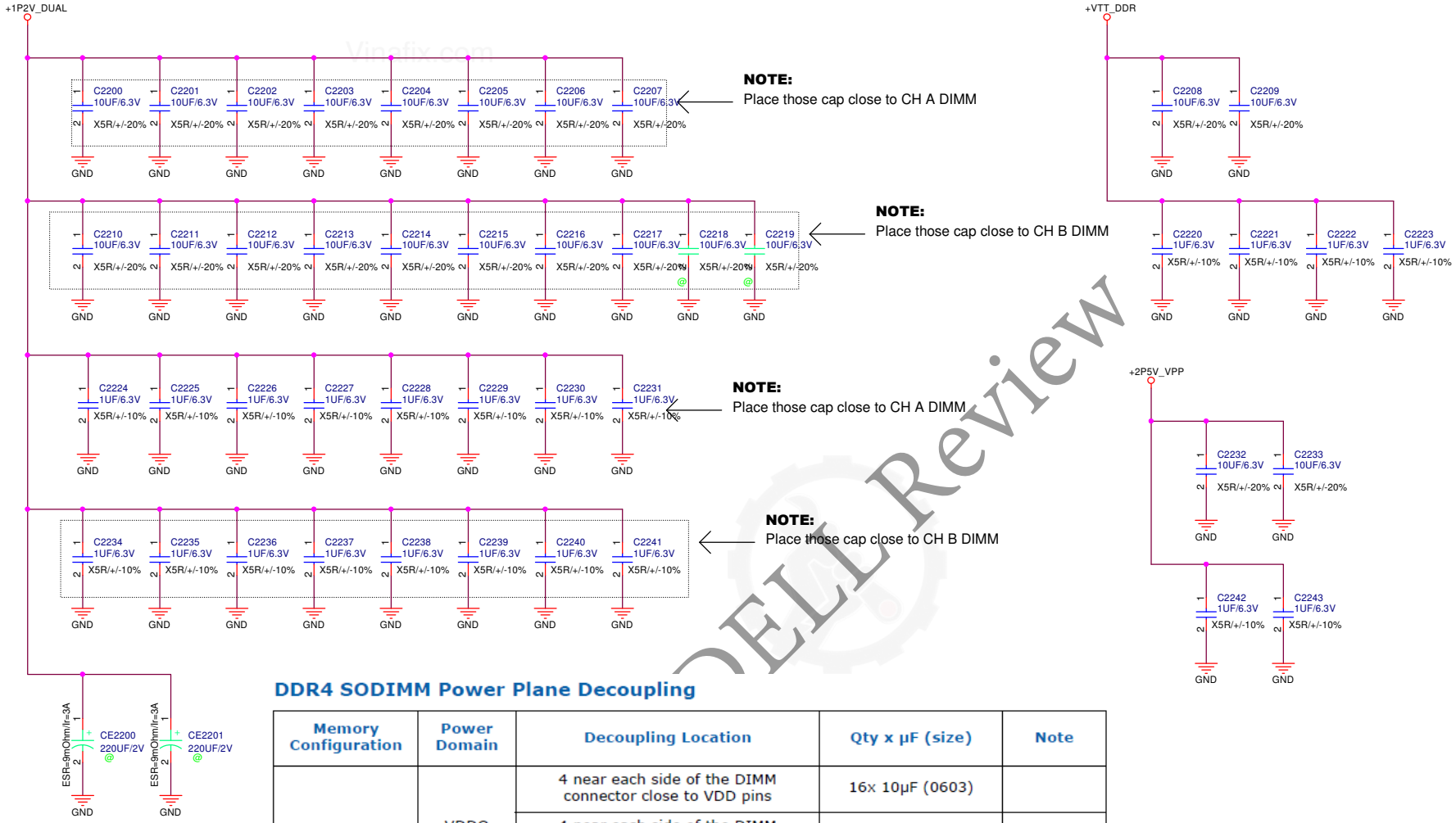
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR4_SO-DIMM1

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 21 of 999



DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM **1DPC**	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DRAM Side	2x 10µF (0603)	
		DRAM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	1x 0.1µF (0402)	
		Place close to DIMM	1x 22µF (0402)	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR4 TERMINATION A&

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 22 of 999

EC Power

Imax:12.5mA

+3P3VSB → R2301 0Ohm → +3VALW_EC

C2300 0.1UF/16V, C2301 0.1UF/16V, C2302 0.1UF/16V, C2303 0.1UF/16V, C2304 0.1UF/16V, C2305 0.1UF/16V, C2306 0.1UF/16V, C2307 0.1UF/16V, C2316 10UF/6.3V — GND

eSPI Strap

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note:

If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel.

If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

GPIO123/SHD_CS# [BSS_STRAP] — PCH_RSMRST# — R2322 100KOHM — GND

+3VALW_EC — R2320 100KOHM — KSO9 — GPIO102/KSO09[CR_STRAP]

debug test point placement together bottom side

HOST_DEBUG_TX, ICSP_CLK, ICSP_DAT, ICSP_CLR, +3VALW_EC — T2304 TPC40, T2306 TPC40, T2305 TPC40, T2307 TPC40, T2309 TPC40

Pull Up

+VCC_RTC — R2339 100KOHM — GPIO162

+1.8VALW_EC — R2331 10KOhm — ESPI_RESET# ; R2341 10KOhm — MASK_SATA_LED#

+3VALW_EC — R2334 TP_WAKE_KBC# ; R2326 USB_EN# ; R2333 CMP_VOUT0 ; R2335 TP_EN# ; R2342 BAT1_LED# ; R2343 BAT2_LED# ; R2349 BREATH_LED# ; R2347 KB_LED_PWM ; R2348 GC6_THM_DIS#

BKLT_IN_EC — R2344 100KOHM ; SYSPWR_PRES — R2332 100KOHM — GND

+VCC_RTC — R2308 0Ohm — +RTC_CELL_VBAT — C2308 0.1UF/16V — GND

+1P8VSB — R2336 0Ohm — +1.8VALW_EC — C2309 0.1UF/16V — GND

+3VALW_EC — R2319 4.7KOhm ; R2318 4.7KOhm

1% 100Ohm — R2316 — PBAT_SMBDAT 36

1% 100Ohm — R2317 — PBAT_SMBCLK 36

Adapter power monitor to EC ADC pin — Need very close to EC

I_ADP — R2311 1% 330Ohm — BB_AMON_BMON 23,77 — C2317 2200PF/50V X7R/+/-10% — EC_AGND

U2300 MEC1416-NU-D0 06T38M002NDE

VTR_33_18 — VBAT — VTR_3 — VTR_5 — VTR_1 — VTR_2 — VTR_4

GPIO027/KSO00/PVT_IO1 … GPIO102/KSO09[CR_STRAP] — KSO0 … KSO16

GPIO106/KSO10 … GPIO111/KSO12 — KSO10 … KSO15

GPIO112/PS2_CLK1A/KSO13 … GPIO125/KSO15 — KSO13 … KSO16

GPIO132/KSO16 … GPIO140/KSO17 — KSO16 … KSO17

GPIO143/KSI0/DTR# … GPIO005/SMB00_DATA/SMB00_DATA18/KSI2 — KSI0 … KSI2

GPIO006/SMB00_CLK/SMB00_CLK18/KSI3 … GPIO152/KSI7/CTS# — KSI3 … KSI7

GPIO007/SMB01_DATA/SMB01_DATA18 — PBAT_CHG_SMBDAT ; GPIO010/SMB01_CLK/SMB01_CLK18 — PBAT_CHG_SMBCLK

GPIO012/SMB02_DATA/SMB02_DATA18 — SPU_THM_SMBDAT 19,69 ; GPIO013/SMB02_CLK/SMB02_CLK18 — SPU_THM_SMBCLK 19,69

GPIO130/SMB03_DATA/SMB03_DATA18 — TYPEC_SMBDAT 18 ; GPIO131/SMB03_CLK/SMB03_CLK18 — TYPEC_SMBCLK 18

GPIO141/SMB04_DATA/SMB04_DATA18 — CHG_SMBDAT 77 ; GPIO142/SMB04_CLK/SMB04_CLK18 — CHG_SMBCLK 77

GPIO050/TACH0 — FAN_TACH 36 — T2302 TPC40

GPIO053/PWM0 — SLP_LED_PWM 51 ; GPIO054/PWM1 — SLEEP 18

GPIO056/PWM3 — FAN_PWM 36 — T2301 TPC40

GPIO030/BCM_INT0#/PWM4 — LANWAKE# — R2345 0Ohm — LAN_WAKE# 12

GPIO031/BCM_DAT0/PWM5 — PS_ID 76 ; GPIO032/BCM_CLK0/PWM6 — PCIE_WAKE# 12,31,51

GPIO002/PWM7

GPIO157/LED0/TST_CLK_OUT1 — BAT2_LED# 50 ; GPIO155/LED1 — BAT1_LED# 50

GPIO104/LED2 — BREATH_LED# 51

GPIO116/TFDP_DATA/UART_RX — ME_FWP 10 — HOST_DEBUG_TX ; GPIO117/TFDP_CLK/UART_TX

GPIO035/SB_TSI_CLK ; GPIO033/PECI_DAT/SB_TSI_DAT — PECI — R2300 43Ohm — PECI_PCH 4

D2300 1PS79SB30 — PTP_DIS# — PTP_DIS#_R 51

VREF_CPU — R2321 0Ohm — +VCCST — C2315 0.1UF/16V — GND

GPIO145/(ICSP_CLOCK) — ICSP_CLK ; GPIO146/(ICSP_DATA) — ICSP_DAT ; ICSP_MCLR — ICSP_CLR

+3P3VA — GND

BGPO/GPIO004 — NB_MUTE# — R2302 0Ohm ; SYSPWR_PRES — R2306 1KOhm — EC_MUTE# 38

VCI_OUT/GPIO036 — ALWON 24,87

VCI_IN1#/GPIO162 — POWER_SW_IN# ; VCI_IN0#/GPIO163 — HW_ACAV_IN — R2307 0Ohm — ACAV_IN_R 24

VCI_OVRD_IN/GPIO164

GPIO160/DAC_0 — GC6_THM_DIS# ; GPIO161/DAC_1 — HW_ACAVIN_NB 76

DAC_VREF — +3VALW_EC

+VCC_RTC — R2310 100KOHM — R2309 1KOhm — PWR_BTN# 51 — C2311 2.2UF/6.3V — GND

GPIO124/CMP_VOUT0 — CMP_VOUT0 24 ; GPIO020/CMP_VIN0 — CMP_VIN0 37 ; GPIO165/CMP_VREF0 — VCREF0 24

GPIO120/CMP_VOUT1 — PROCHOT 4 — T2310 TPC40 ; GPIO021/CMP_VIN1 — LCD_TST 30 ; GPIO166/CMP_VREF1/UART_CLK

GPIO024/ADC7 — USB_PWR_SHR_EN_L# 23,51 ; GPIO023/ADC6/A20M — PANEL_BKEN_EC 30 ; GPIO022/ADC5 — SIO_EXT_WAKE# 15

GPIO153/ADC4 — MODEL_ID ; GPIO154/ADC3 — I_ADP ; GPIO155/ADC2 — BOARD_ID

GPIO122/ADC1 — I_BATT ; GPIO121/ADC0 — LCD_VCC_TEST_EN 30 ; ADC_VREF — +3VALW_EC

Battery power monitor to EC ADC pin

R2305 1% 330Ohm — BB_AMON_BMON 23,77 — C2321 2200PF/50V X7R/+/-10% — EC_AGND

CAP_LED# — R2338 4.7KOhm ; R2337 4.7KOhm — +3VALW_EC

CLK_TP_SIO ; DAT_TP_SIO

SIO_PWRBTN# — VCCDSW_EN

ESPI_IO0 … ESPI_CLK — MASK_SATA_LED# ; CCG4_I2C_INT# ; SYS_PWROK ; PBAT_PRES# ; +1P8VSB_PWRGD ; RTCRST_ON ; PCH_RSMRST#_EC

ESPI_ALERT# — GPU_PWR_LEVEL ; TP_EN# ; ESPI_RESET# ; LID_CL_SIO#

PRIM_PWRGD — R2346 0Ohm ; PCH_RSMRST# — R2323 0Ohm

BKLT_IN_EC ; AC_DIS ; USB_POWERSHARE_VBUS_EN ; FPR_SCAN# ; TP_WAKE_KBC# ; AUX_ON

USB_EN# ; RUNPWROK ; RESET_OUT#

SUSCLK — 0Ohm R2329 — MEC_XTAL2 ; MEC_XTAL1_R

C2312 10PF/50V — GND ; R2330 0Ohm — MEC_XTAL2_R — X2300 32.768KHZ — C2318 10PF/50V — GND ; C2319 10PF/50V — GND

VSS_VBAT ; VSS_4 ; VSS_2 ; VSS_1 ; VSS_3 ; VSS_5 ; AVSS ; VR_CAP — R2328 0Ohm — EC_AGND ; C2310 1UF/6.3V — GND

BOARD_ID — +3VALW_EC — R2314 49.9KOhm 1% — C2314 0.1UF/16V — R2315 100KOhm 1% — GND

MODEL_ID — +3VALW_EC — R2312 27KOhm 1% /UMA ; R2351 82.5KOhm 1% /GPU — C2313 0.1UF/16V — R2313 100KOhm 1% — GND

+3VALW_EC — R2324 10KOhm — USB_PWR_SHR_EN_L# 23,51 — R2325 10KOhm — GND

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	**10.0K**	3
2	X01	100.0K	**17.8K**	2.801
3	X02	100.0K	**27.0K**	2.598
4	X03(reserve)	100.0K	**37.4K**	2.402
5	A00	100.0K	**49.9K**	2.201
6	A01	100.0K	**64.9K**	2.001
7	A02	100.0K	**82.5K**	1.808
8	A03	100.0K	**107K**	1.594
9	Reserve	100.0K	**154K**	1.299
10	Reserve	100.0K	**200K**	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

```
# if ENABLE_IDEAL_AD_CONVERT
*
* BOARD ID Voltage Step
*  Step   Pull Down   Pull Up   Ideal Voltage Divider   Ideal ADC count
*  00       100K       10.0K        1.000                  511
*  01       100K       17.8K        2.801                  869
*  02       100K       27.0K        2.598                  806
*  03       100K       37.4K        2.402                  745
*  04       100K       49.9K        2.201                  683
*  05       100K       64.9K        2.001                  621
*  06       100K       82.5K        1.808                  561
*  07       100K       107K         1.594                  495
*  08       100K       154K         1.299                  403
*  09       100K       200K         1.100                  341
*  10       Undefine
*
*  Ideal Voltage Divider = 3.3V * (Pull Down)/(Pull Down + Pull Up)
*  ADC count = [(ADC pin's Voltage Level)/(ADC_VREF voltage Level)]*1024
```

PEGATRON DT-MB RESTRICTED SECRET

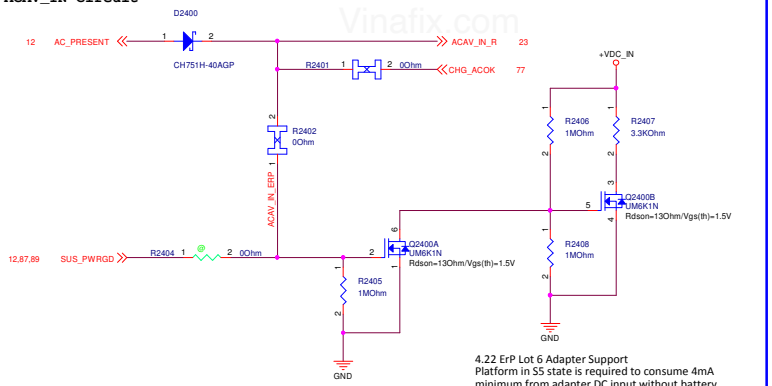
PEGATRON Title : EC#1

Pegatron Corp. Engineer: .

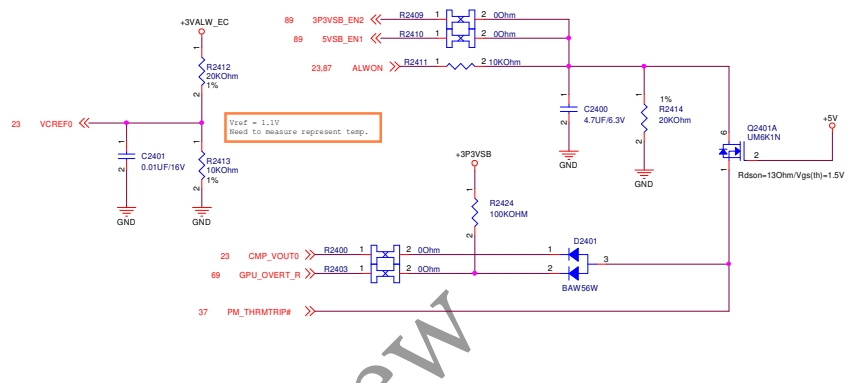
Size	Project Name	Rev
A2	Loki/Armani	A00

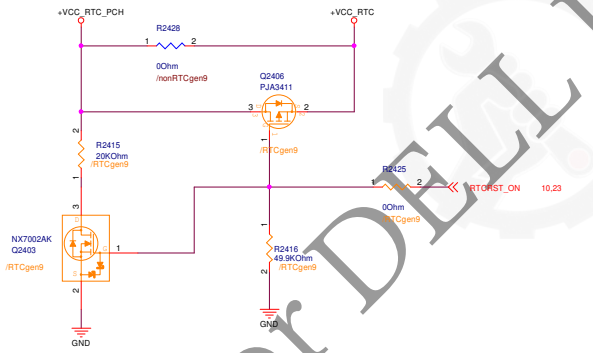
Date: Friday, August 25, 2017 Sheet 23 of 999

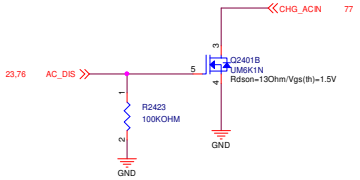
ACAV_IN Circuit



Thermal CMP Circuit



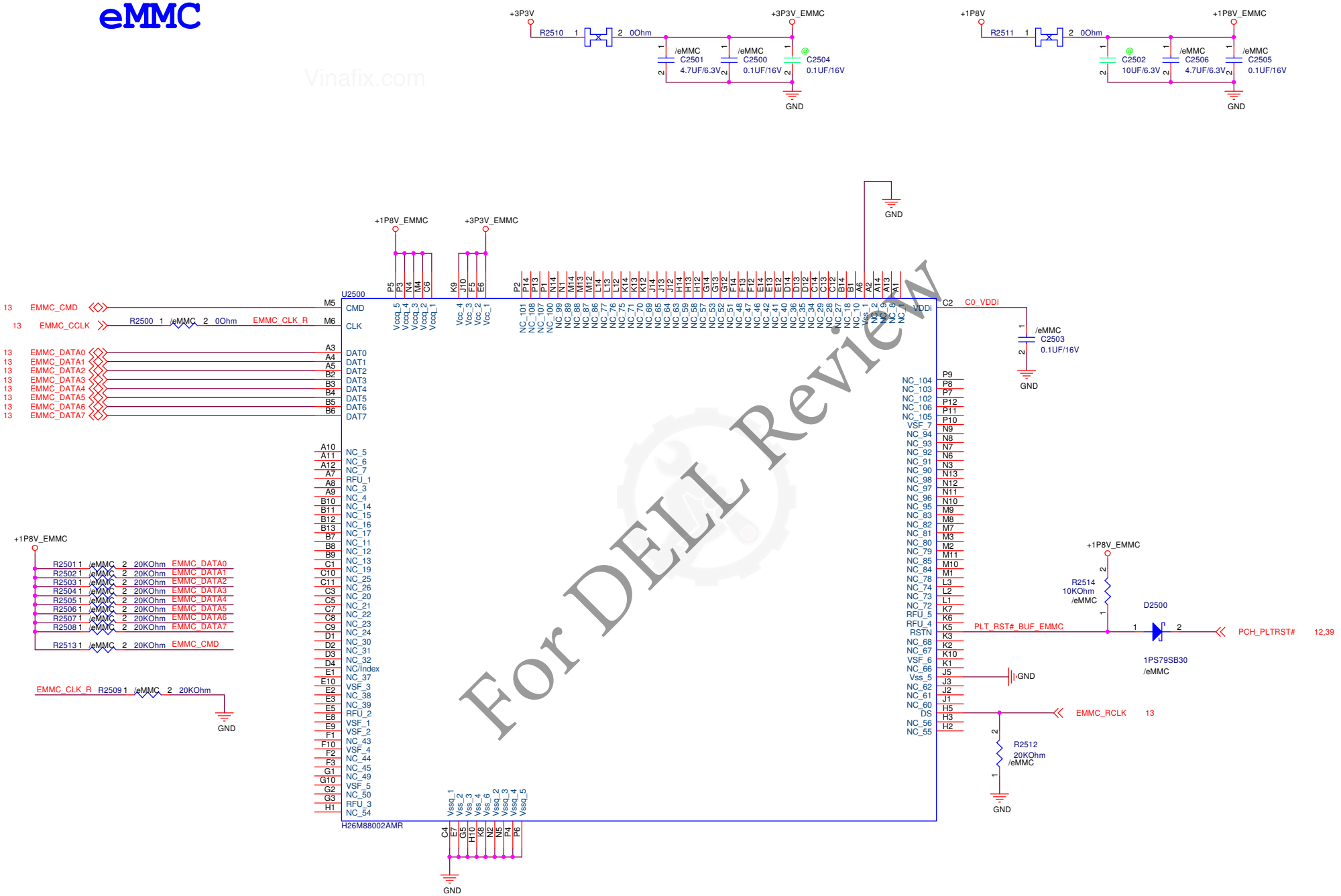




PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : EC#2	
Pegatron Corp.	Engineer: -	
Size: A2	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 24 of 999	

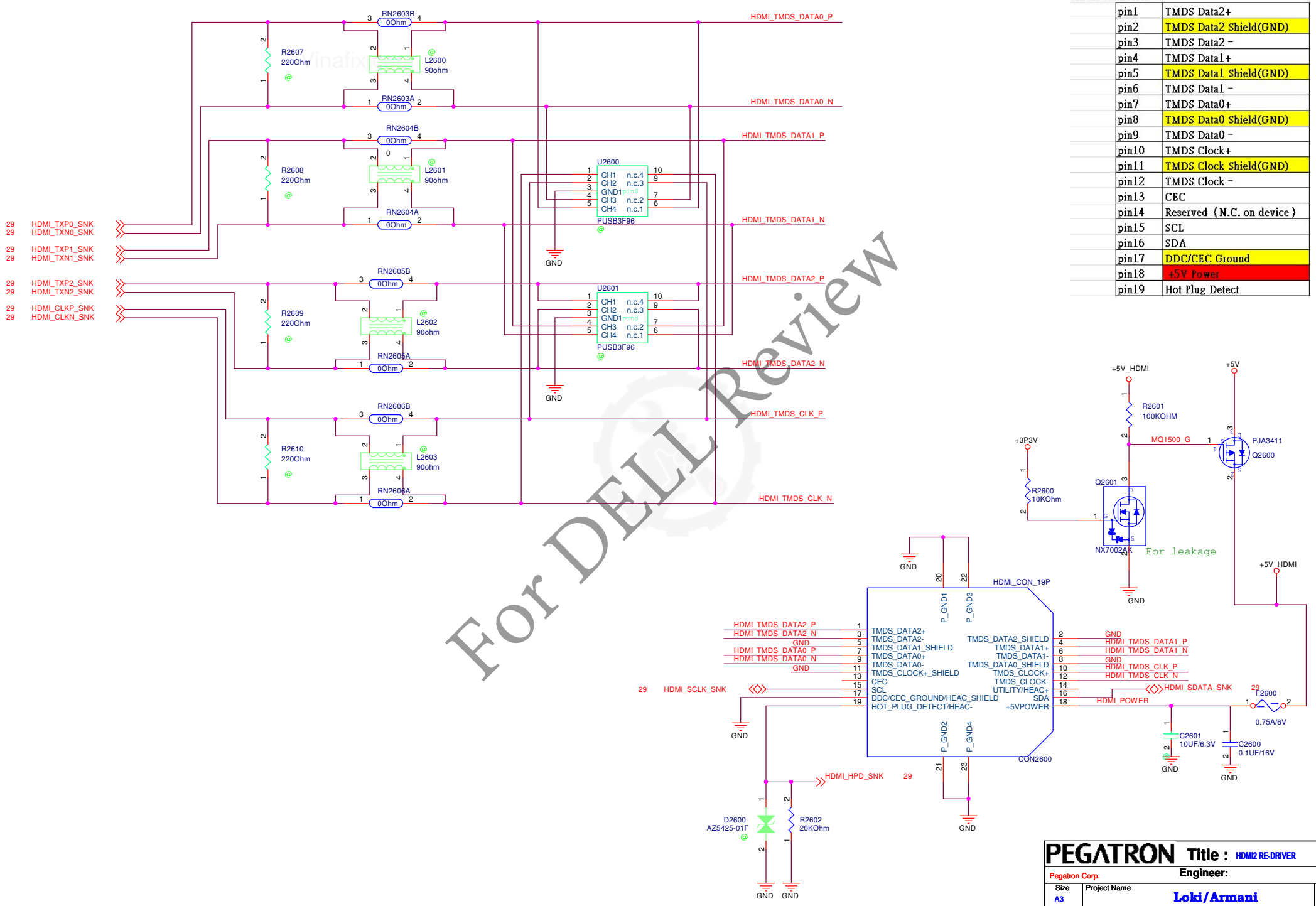
eMMC



Intel PDG R2.0 : If the interface is used, external pull-up resistors of 20 KΩ are required on the Data lines. A pull-down resistor of 20 KΩ is recommended on the Clock lines.

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : EMMC	
Pegatron Corp.	Engineer: .	
Size: A3	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 25 of 999	



HDMI connector

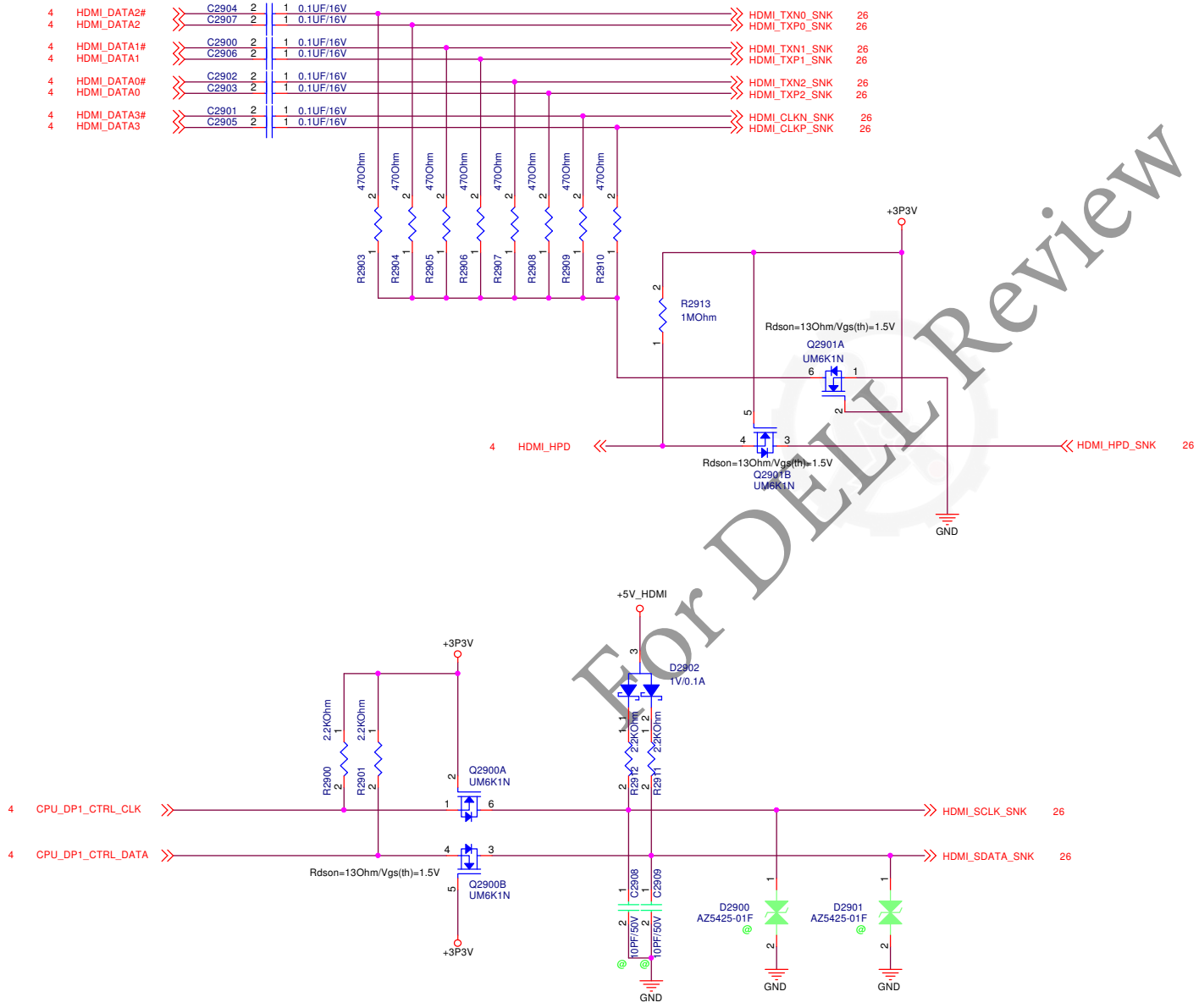
pin1	TMDS Data2+
pin2	TMDS Data2 Shield(GND)
pin3	TMDS Data2 -
pin4	TMDS Data1+
pin5	TMDS Data1 Shield(GND)
pin6	TMDS Data1 -
pin7	TMDS Data0+
pin8	TMDS Data0 Shield(GND)
pin9	TMDS Data0 -
pin10	TMDS Clock+
pin11	TMDS Clock Shield(GND)
pin12	TMDS Clock -
pin13	CEC
pin14	Reserved (N.C. on device)
pin15	SCL
pin16	SDA
pin17	DDC/CEC Ground
pin18	+5V Power
pin19	Hot Plug Detect

PEGATRON Title : HDMI2 RE-DRIVER

Pegatron Corp. Engineer:

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 26 of 999



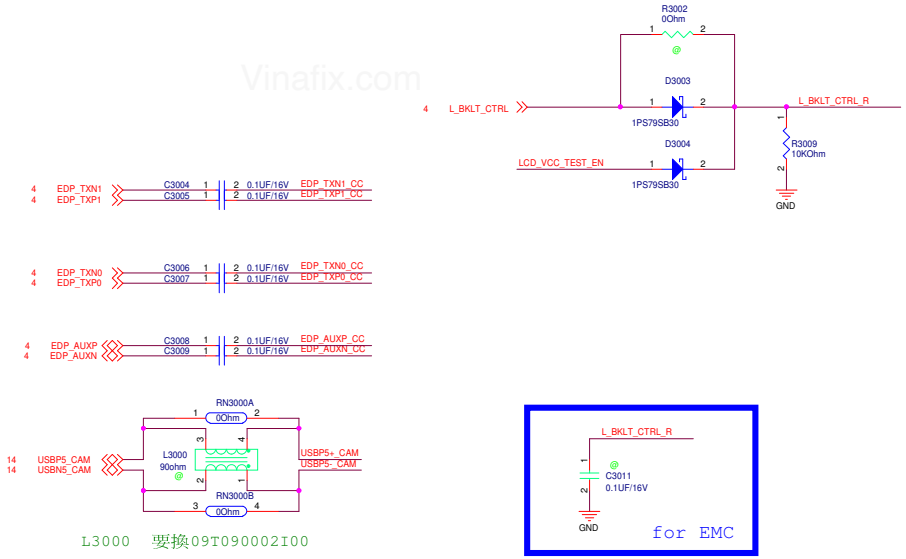
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : HDMI14b Active level shif

Pegatron Corp. Engineer: .

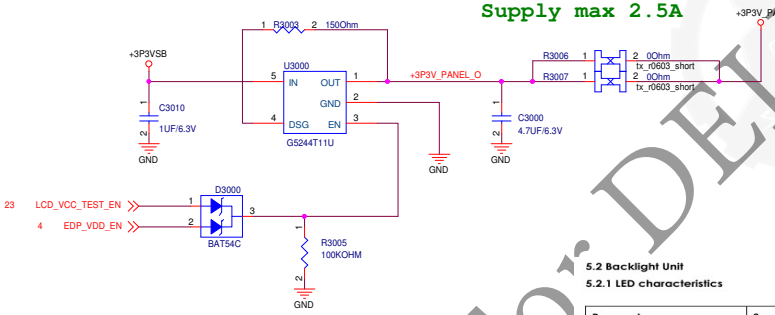
Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 29 of 999

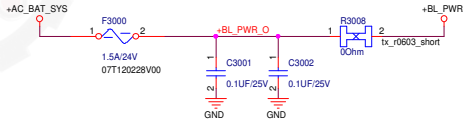


Panel power

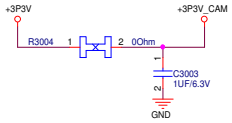
Supply max 2.5A



Backlight power



Cammera power



Symble	Parameter	Min	Typ	Max	Units	Note
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	
PDD	VDD Power	-	-	2.4	[Watt]	Note 1
IDD	IDD Current	-	-	800	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	5.6	[Watt]	(Ta=25℃), Note 1 Vin =12V
LED Life-Time	N/A	15,000	-	-	Hour	(Ta=25℃), Note 2 I_F=23 mA

Note 1: Calculator value for reference P_{LED} = VF (Normal Distribution) * IF (Normal Distribution) / Efficiency

Note 2: The LED life-time define as the estimated time to 50% degradation of initial luminous.

5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	10	12.0	21.0	[Volt]	

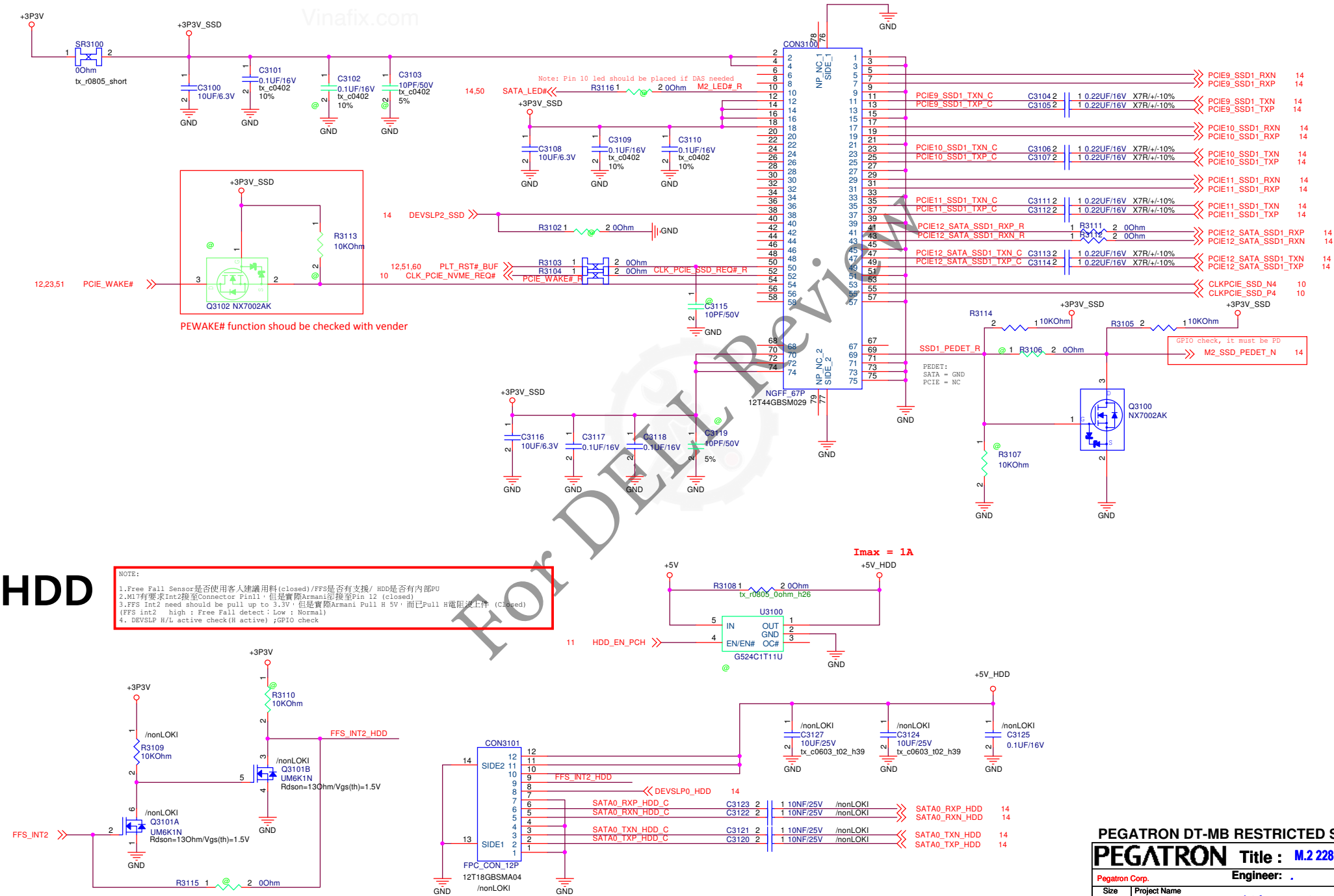
PEGATRON Title : EDP

Pegatron Corp. Engineer: -

Size C | Project Name Loki/Armani | Rev A00

Date: Friday, August 25, 2017 Sheet 30 of 999

M.2 KEY-M 2280 SSD #1(SATA+PCIE X4)



HDD

NOTE:

1.Free Fall Sensor是否使用客人建議用料(closed)/FFS是否有支援/ HDD是否有內部PU
2.M17有要求Int2接至Connector Pin11，但是實際Armani卻接至Pin 12 (closed)
3.FFS Int2 need should be pull up to 3.3V，但是實際Armani Pull H 5V，而已Pull H電阻設上件 (Closed)
(FFS int2 high : Free Fall detect；Low : Normal)
4. DEVSLP H/L active check(H active) ;GPIO check

PEGATRON DT-MB RESTRICTED SECRET

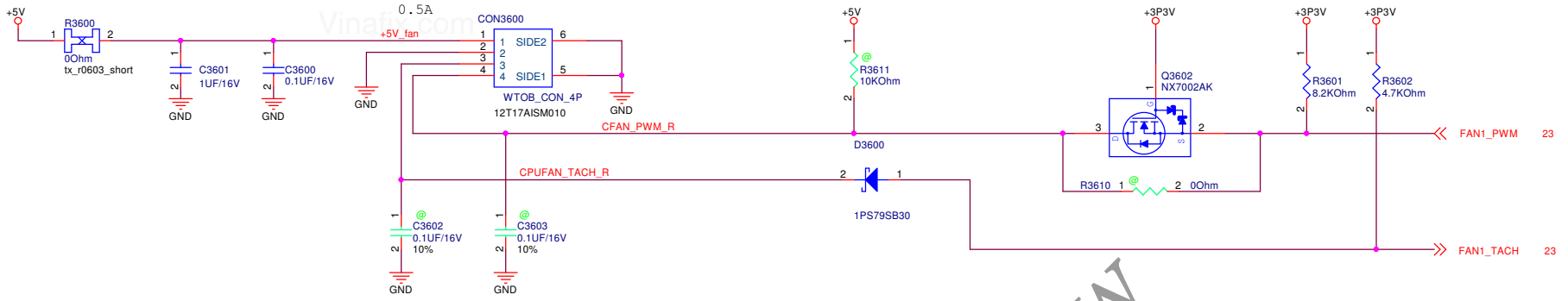
PEGATRON Title : M.2 2280 SSD/ HDD

Pegatron Corp. Engineer: .

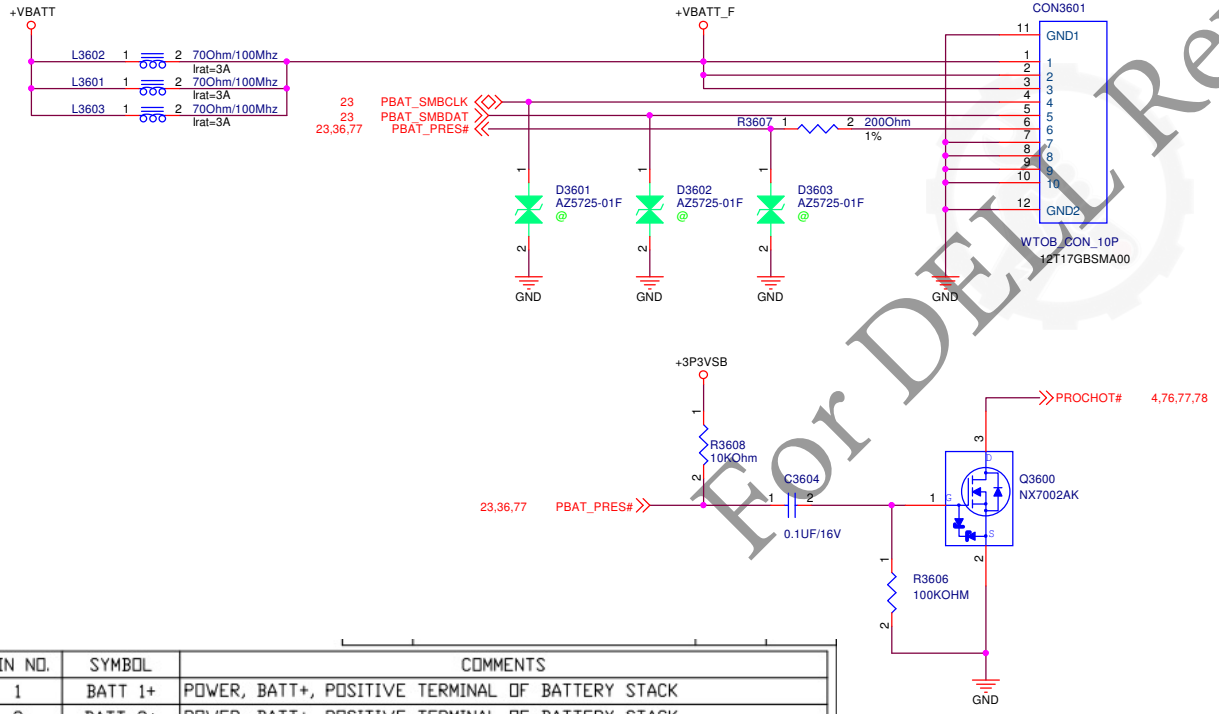
Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 31 of 999

FAN CONNECTOR

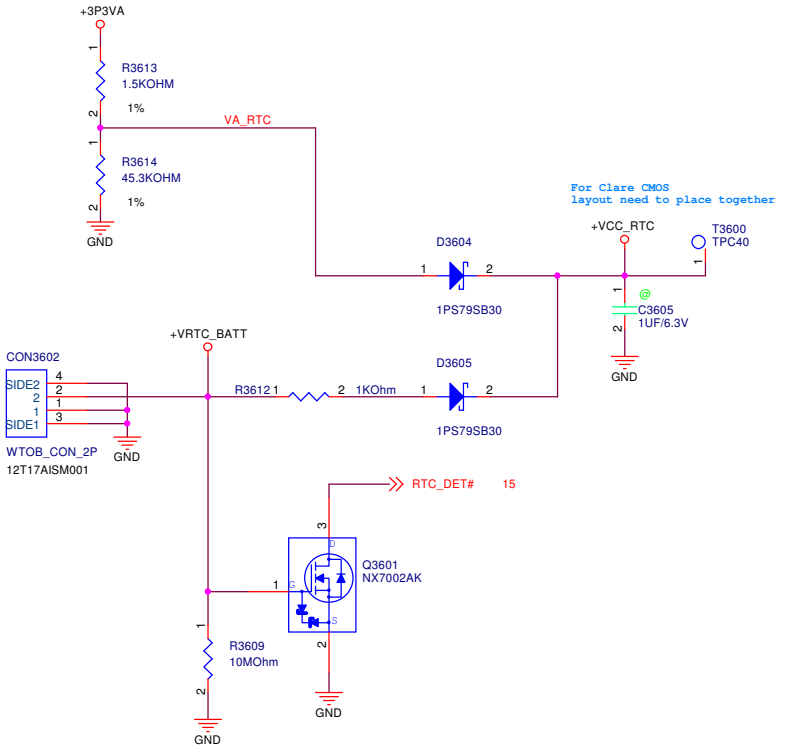


Battery CONNECTOR



PIN NO.	SYMBOL	COMMENTS
1	BATT 1+	POWER, BATT+, POSITIVE TERMINAL OF BATTERY STACK
2	BATT 2+	POWER, BATT+, POSITIVE TERMINAL OF BATTERY STACK
3	BATT 3+	POWER, BATT+, POSITIVE TERMINAL OF BATTERY STACK
4	CLK_SMB	SYSTEM MANAGEMENT BUS CLOCK
5	DAT_SMB	SYSTEM MANAGEMENT BUS CLOCK
6	BATT_PRS	BATTERY PRESENT (THIS IS TIED TO GROUND ON THE BATTERY PACK)
7	SYS_PRES	SYSTEM PRESENT (THIS IS TIED TO GROUND ON THE SYSTEM SIDE)
8	GND1	POWER, BATT-, NEGATIVE TERMINAL OF BATTERY STACK
9	GND2	POWER, BATT-, NEGATIVE TERMINAL OF BATTERY STACK
10	GND3	POWER, BATT-, NEGATIVE TERMINAL OF BATTERY STACK

RTC CONNECTOR



PEGATRON DT-MB RESTRICTED SECRET

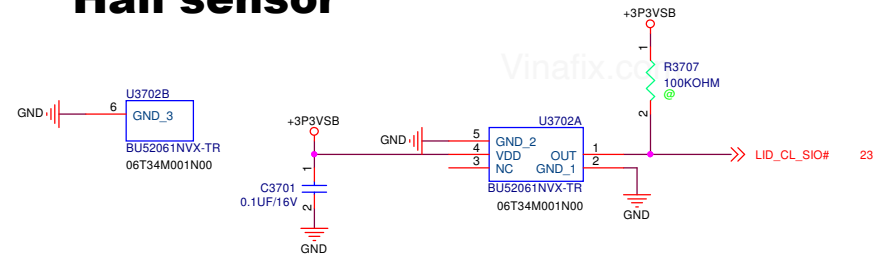
PEGATRON Title : Battery & FANConn

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 36 of 999

Hall sensor

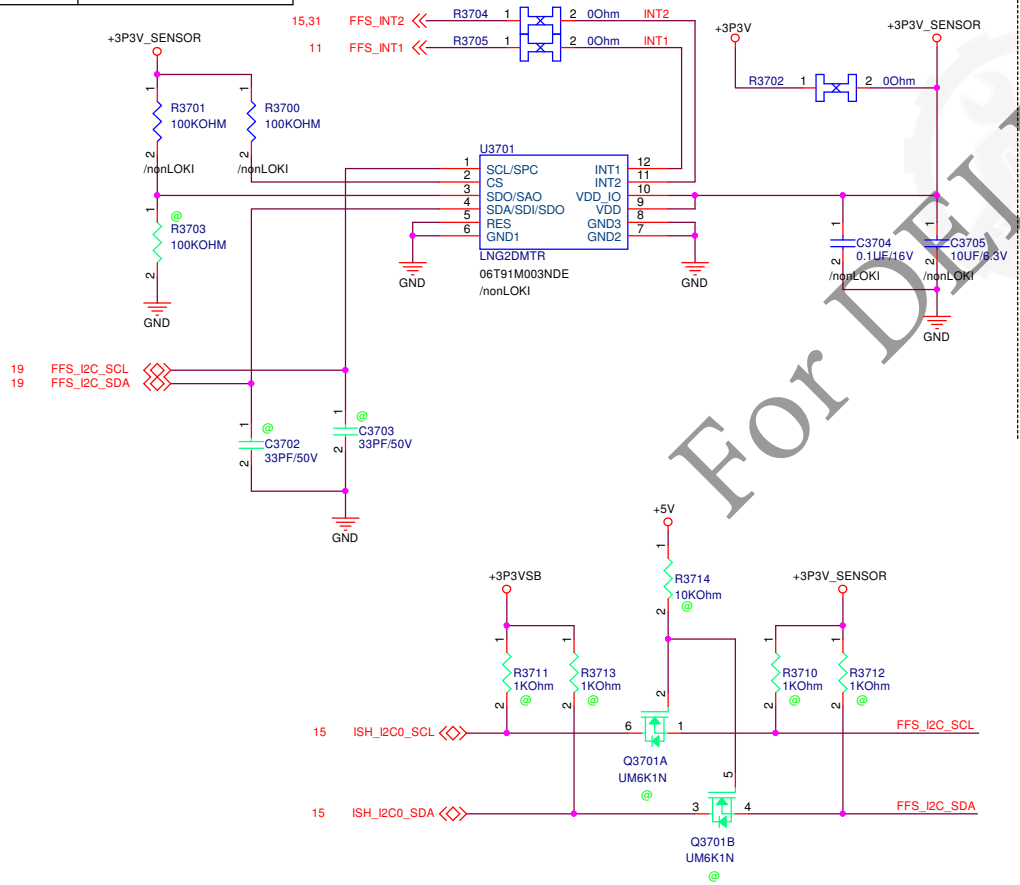


Free fall sensor

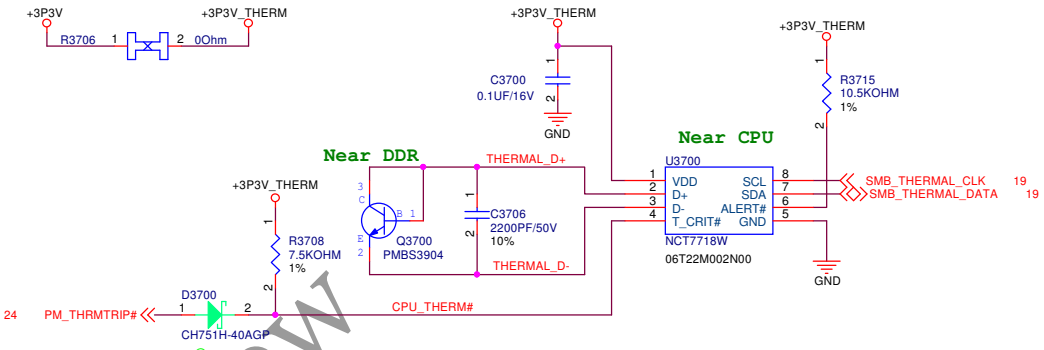
Slave address select

SA0	address
1	0101001b
0	0101000b

Default setting

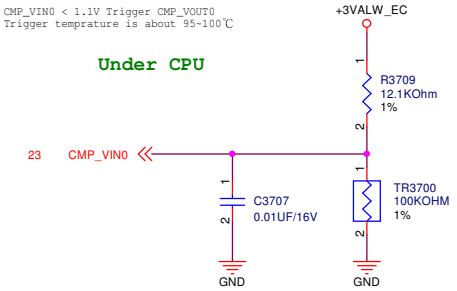


Thermal sensor



Thermistor Table

60	22.621
65	18.692
70	15.525
75	12.947
80	10.849
85	9.129
90	7.713
95	6.546
100	5.572
105	4.764
110	4.087
115	3.518
120	3.040
125	2.634



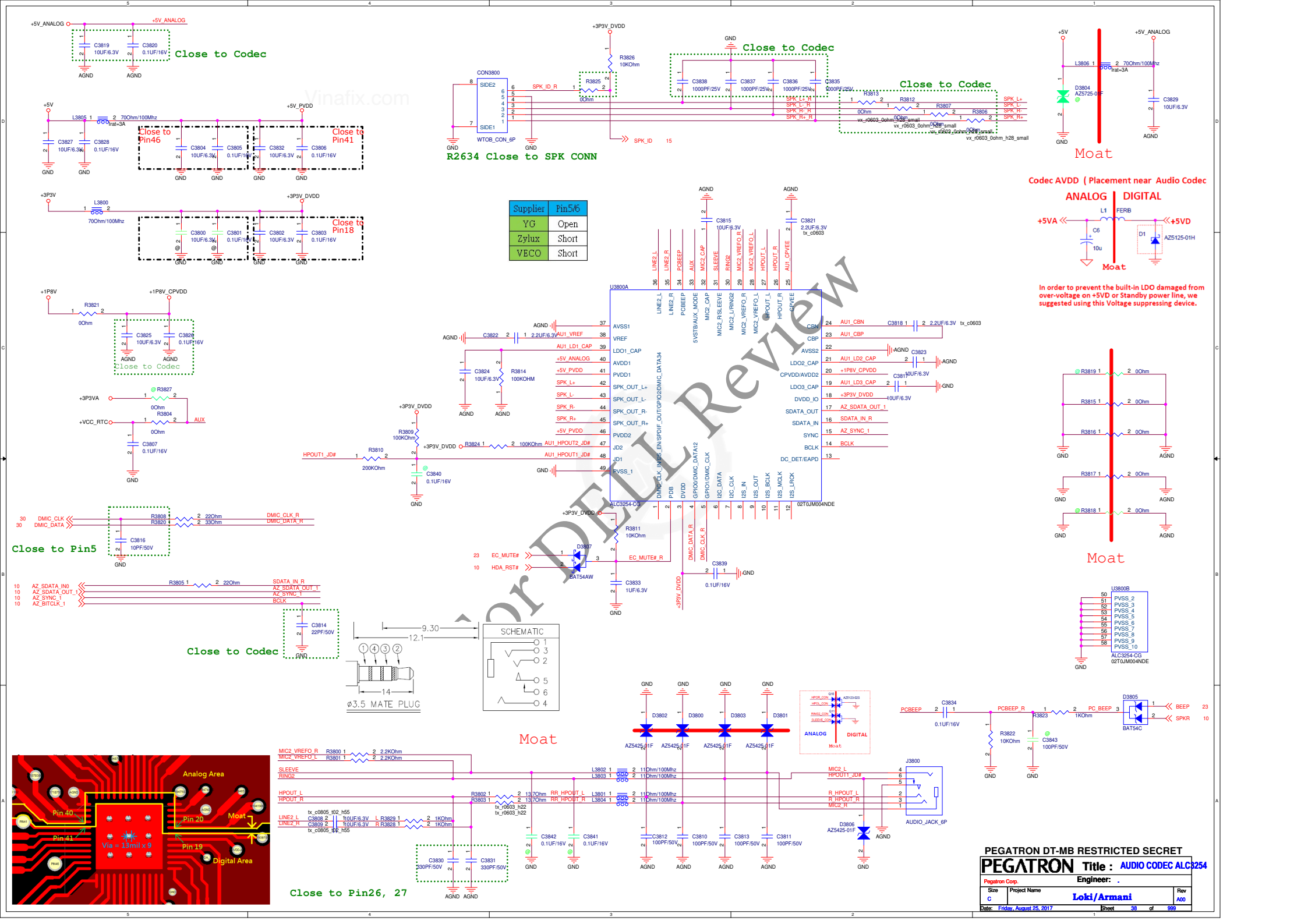
PEGATRON DT-MB RESTRICTED SECRET

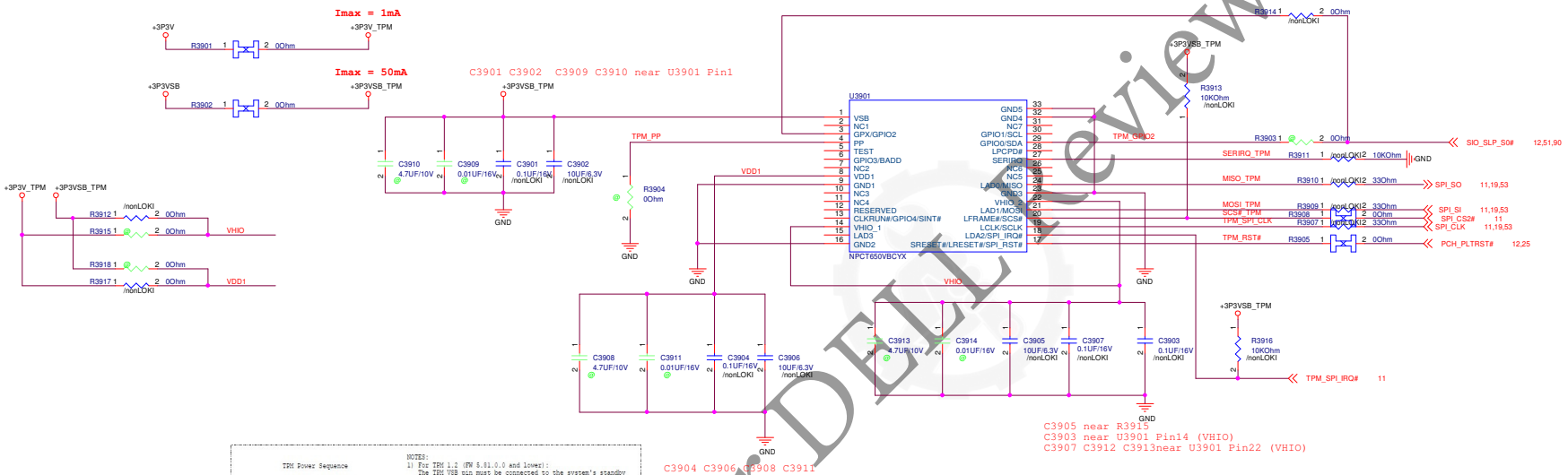
PEGATRON Title : Sensor

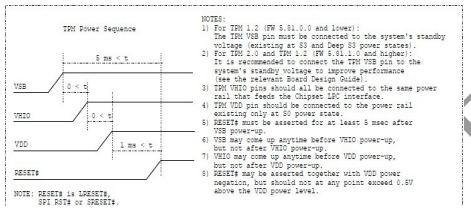
Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 37 of 999







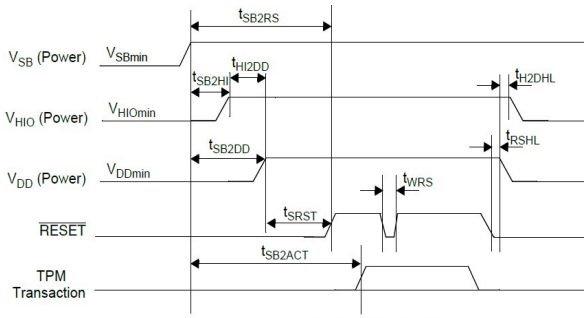


Figure 6. Reset Timing Diagram

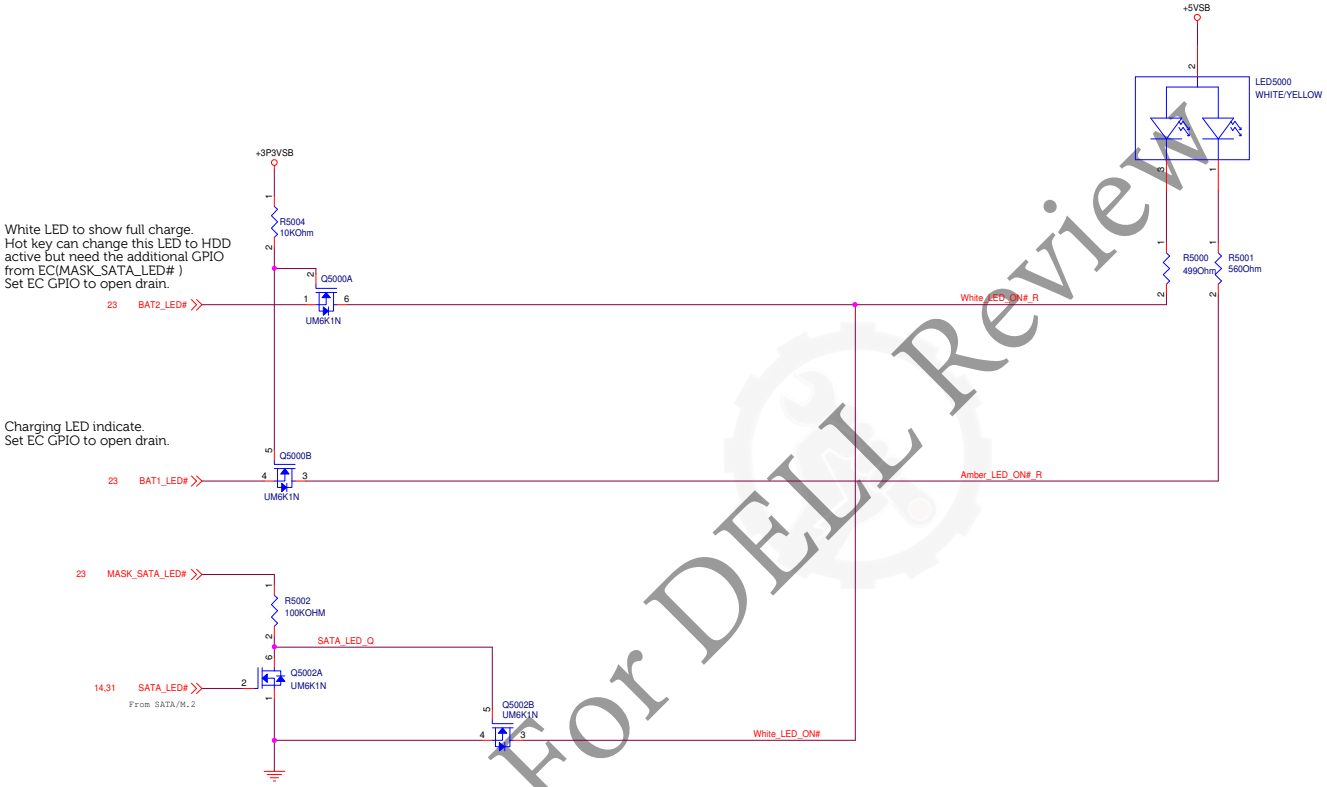
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : TPM

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A2	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 39 of 999



PEGATRON Title : LED

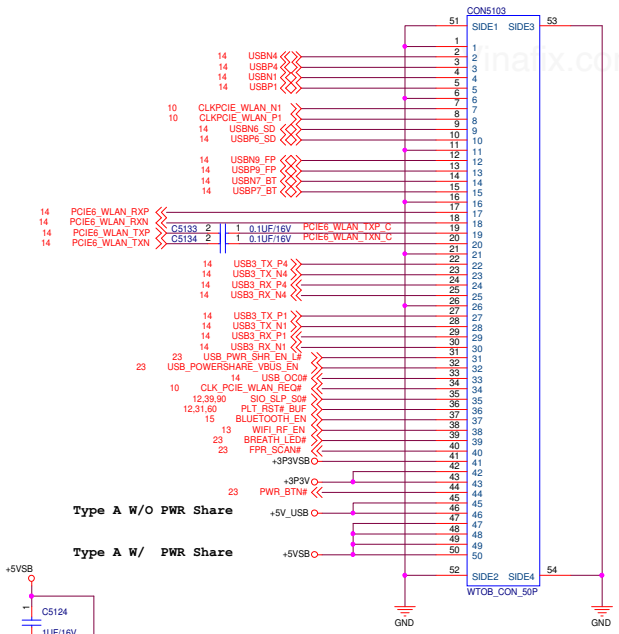
Pegatron Corp. Engineer: -

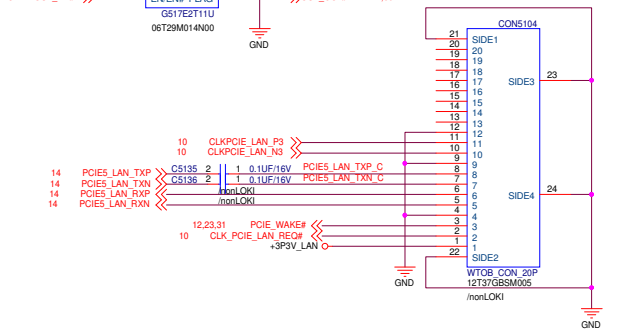
Size	Project Name	Rev
C	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 50 of 999

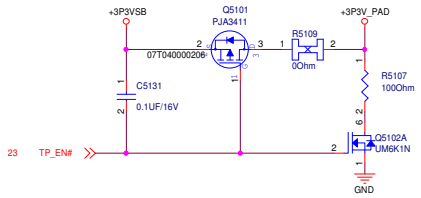
IO board Connector

Coax CONNECTOR 50 PIN

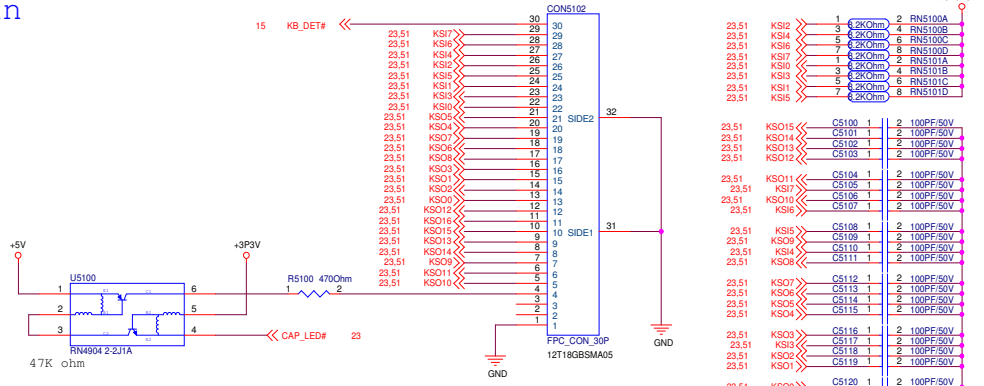




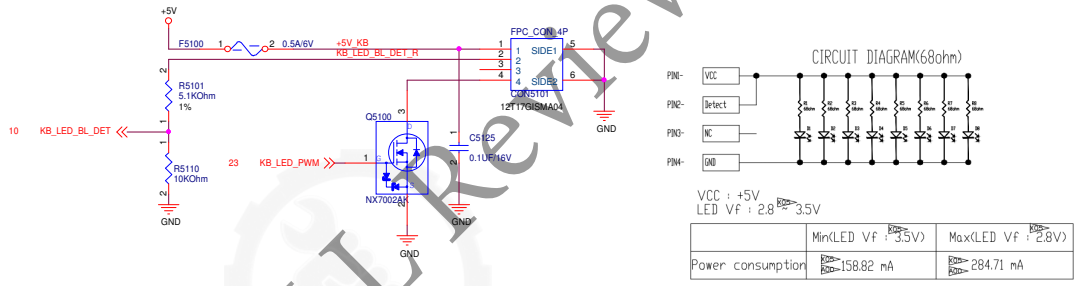
FFC CONNECTOR 12 PIN (for 14" LAN only)



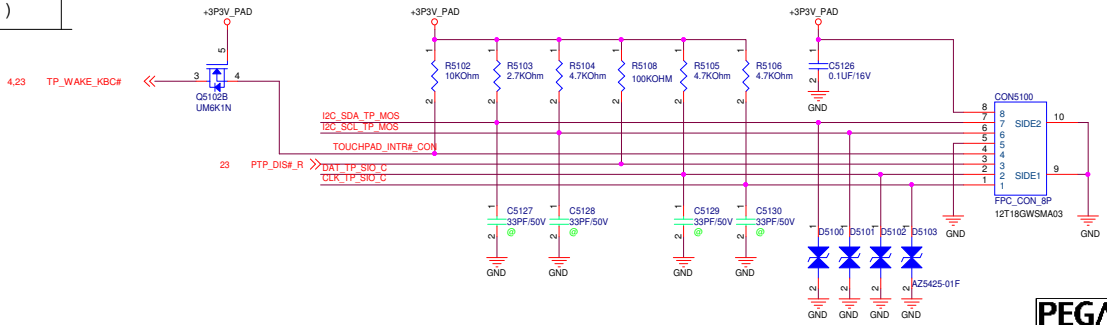
KB Conn



KB BL Conn



Click PAD Connector



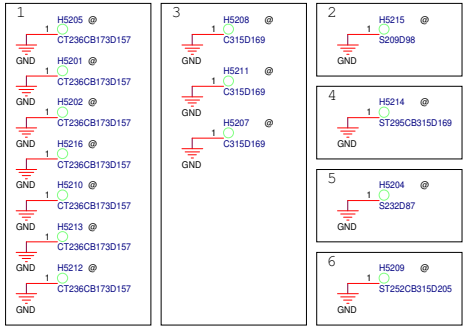
PEGATRON Title : Keyboard and IO connector

Pegatron Corp. Engineer:

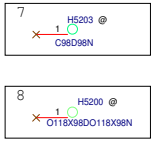
Size	Project Name	Rev
C	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 51 of 999

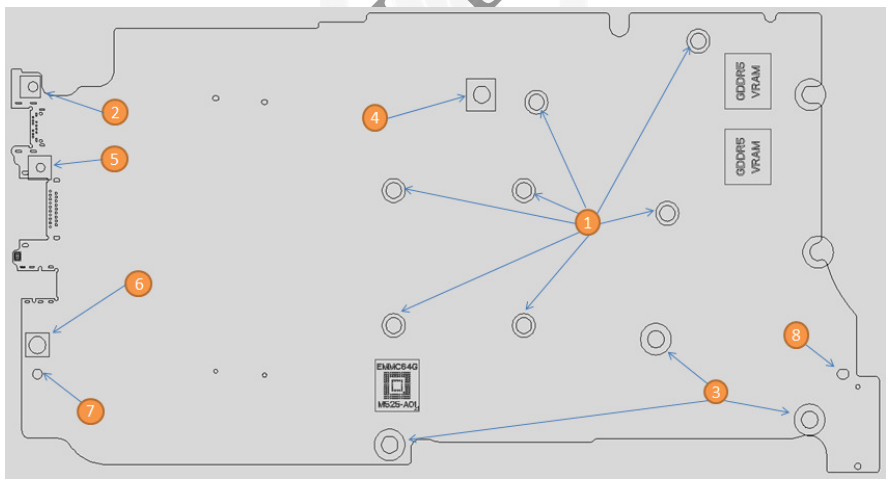
PTH Hole



NPTH Hole



	Ø	TOP PAD	BTM PAD	PTH/NPTH	REMARK
1	Ø=4.0	Ø=6.0	Ø=4.4	PTH	THERMAL BRKT
2	Ø=2.5	L=5.3	L=5.3	PTH	SCREW HOLE
3	Ø=4.3	Ø=8.0	Ø=8.0	PTH	SCREW HOLE
4	Ø=4.3	L=7.5	Ø=8.0	PTH	SCREW HOLE
5	Ø=2.2	L=5.9	L=5.9	PTH	SCREW HOLE
6	Ø=5.2	L=6.4	Ø=8	PTH	SCREW HOLE
7	Ø=2.5	N/A	N/A	NPTH	PCB FIXTURE
8	L=3.0 X Ø=2.5	N/A	N/A	NPTH	PCB FIXTURE



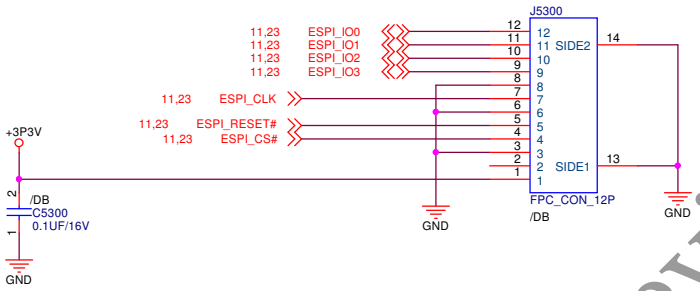
PEGATRON Title : Screw Hole and Nut

Pegatron Corp. Engineer: -

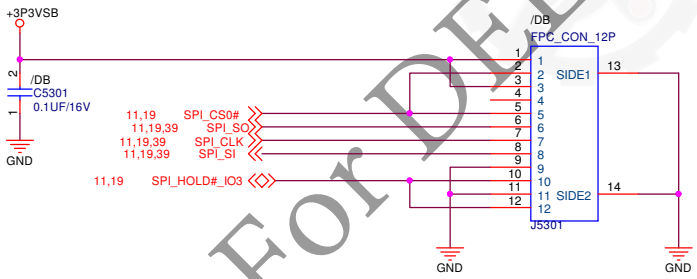
Size	Project Name	Rev
C	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 52 of 999

eSPI DEBUG PORT

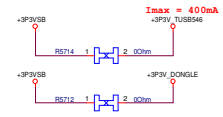


For BIOS Flash ROM



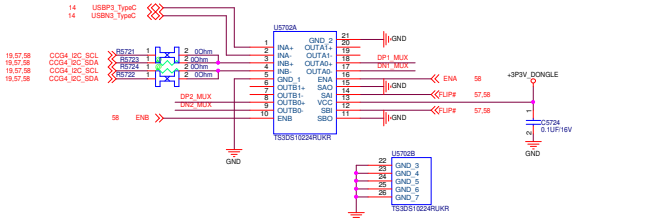
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DEBUG	
Pegatron Corp.	Engineer: .	
Size: A3	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 53 of 999	

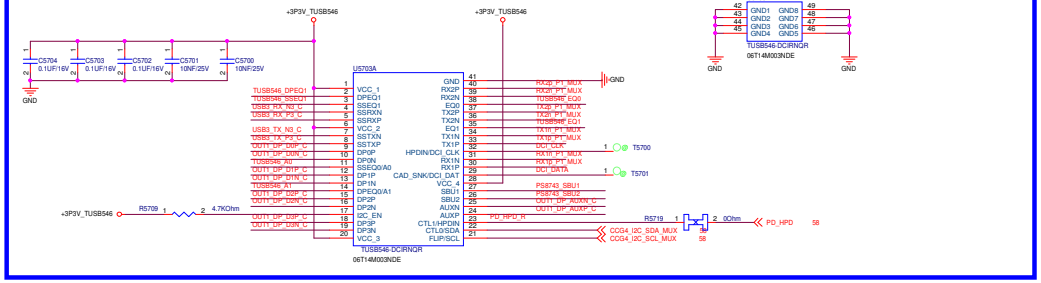


Dongle

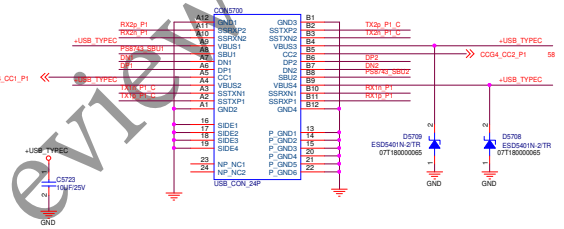
FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C



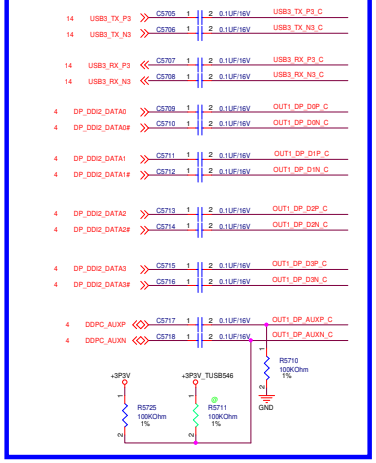
MUX



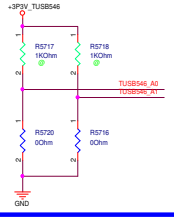
Type-C CONN



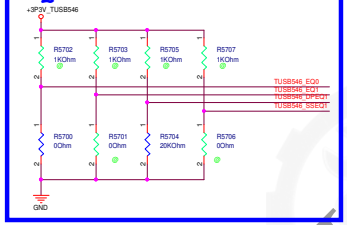
PCH Side



ADDRESS

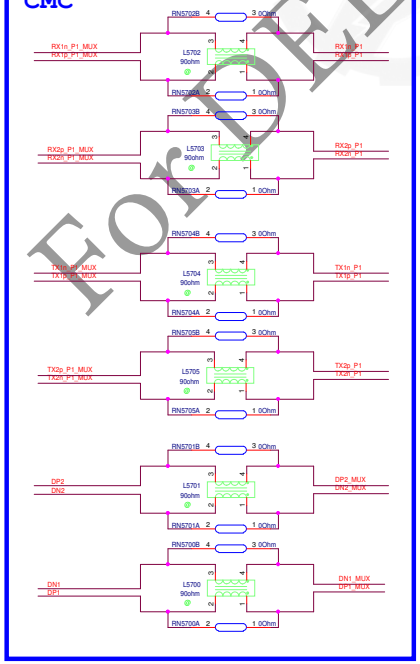


EQ STRAP

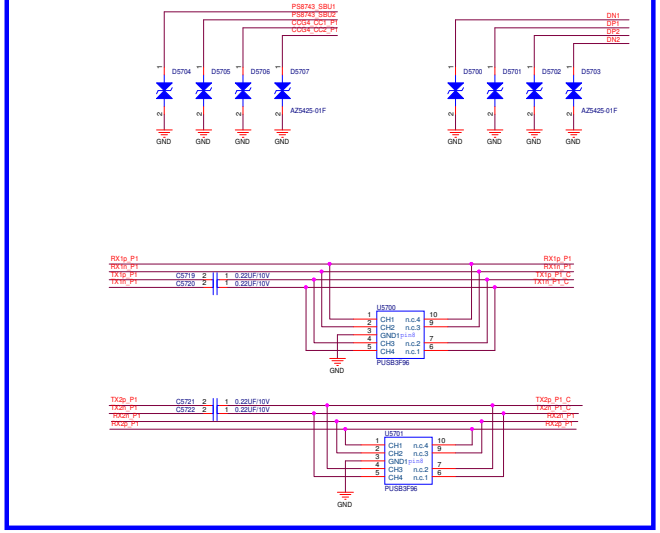


Level Control Pin Setting	
0	Option 1: Tie 1Kohm 5% to GND Option 2: Tie directly GND
R	Tie 20Kohm 5% to GND
F	Float (Leave pin open)
1	Option 1: Tie 1Kohm 5% to VCC Option 2: Tie directly VCC

CMC



ESD



PEGATRON DT-MB RESTRICTED SECRET

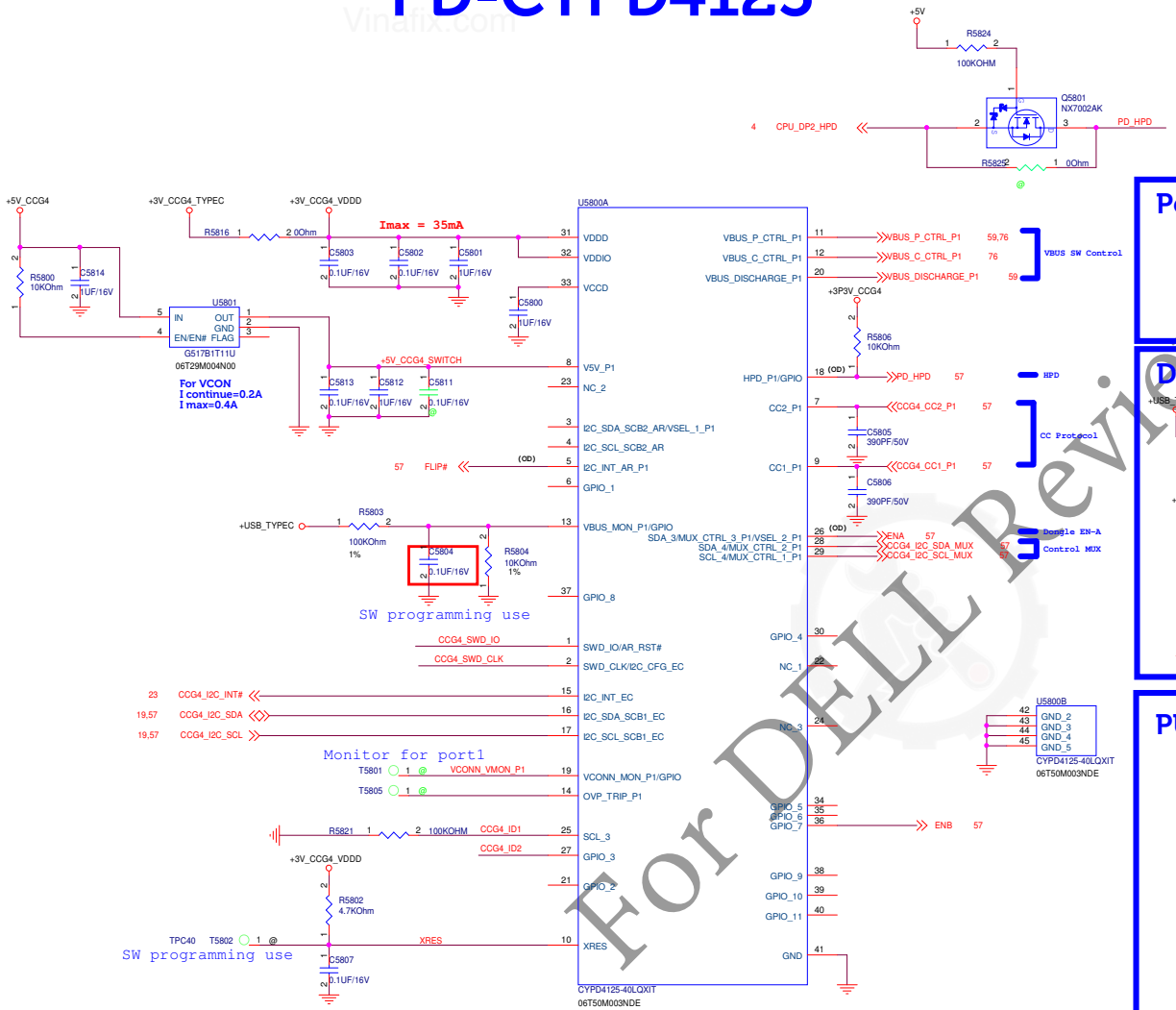
PEGATRON Title : Type-C MUX

Pegatron Corp. Engineer: .

Size	Project Name	Rev
Custom	Loki/Armani	A00

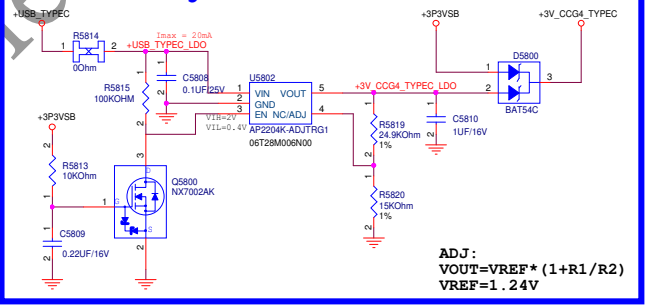
Date: Friday, August 25, 2017 Sheet 57 of 99

PD-CYPD4125

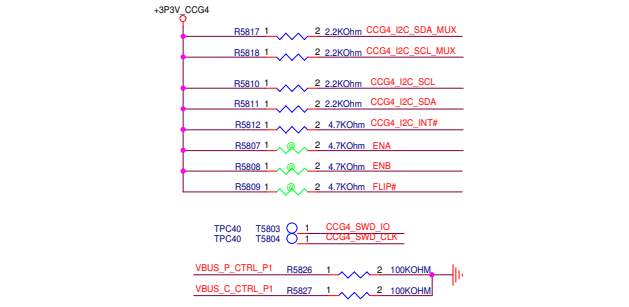


Power

Dead Battery

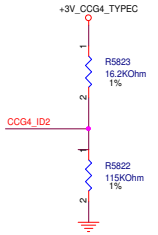


PU/PD resistor



#	Platform	Voltage on CCG4_ID_1	Voltage on CCG4_ID_2
1	Single Port - Intel - DDM support - Armani 13" & 14"	L0	L7
2	Single Port - Intel - DDM support - Kyloren	L0	L6
3	Single Port - Intel - DDM support - Miyake	L0	L5
4	Single Port - Intel - DDM support - Loki 13"	L0	L4
5	Single Port - Intel - DDM support - Loki 15" & 17" (Motherboard is same)	L0	L3
6	Single Port - Intel - DDM support - StarLord KBL - R	L0	L2
7	Single Port - AMD - DDM not supported - Loki 15" & 17" (Motherboard is same)	L4	L0

Voltage level	Voltage value
L0	0V
L1	3.3V/8
L2	2 * 3.3V/8
L3	3 * 3.3V/8
L4	4 * 3.3V/8
L5	5 * 3.3V/8
L6	6 * 3.3V/8
L7	7 * 3.3V/8



PEGATRON DT-MB RESTRICTED SECRET

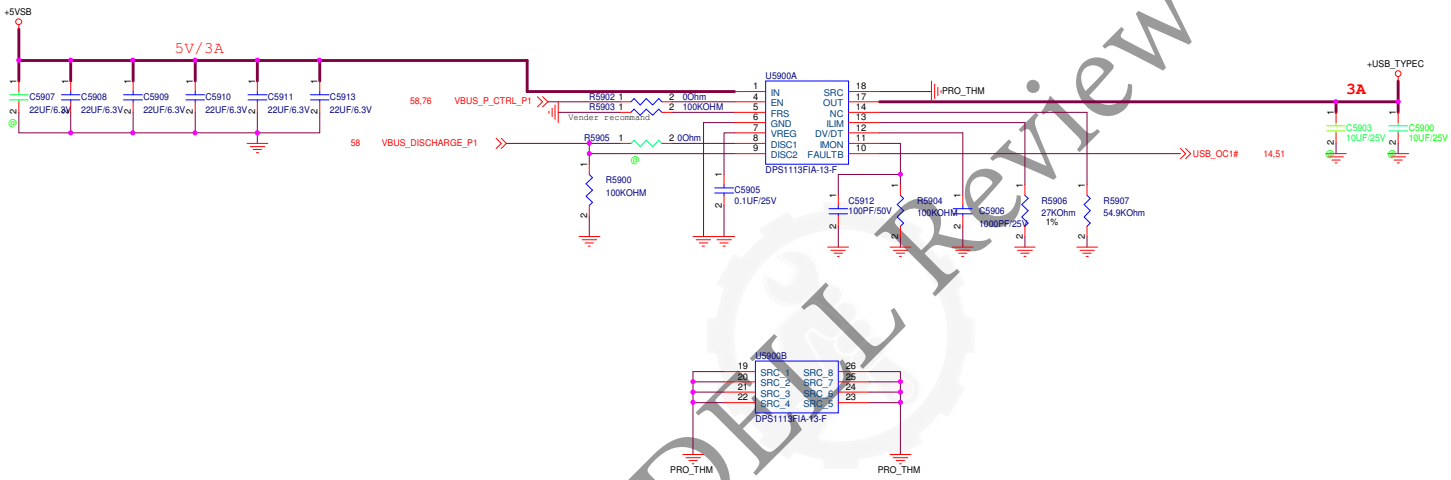
PEGATRON Title : Type-C PD

Pegatron Corp. Engineer:

Size	Project Name	Rev
C	Loki/Armani	A00

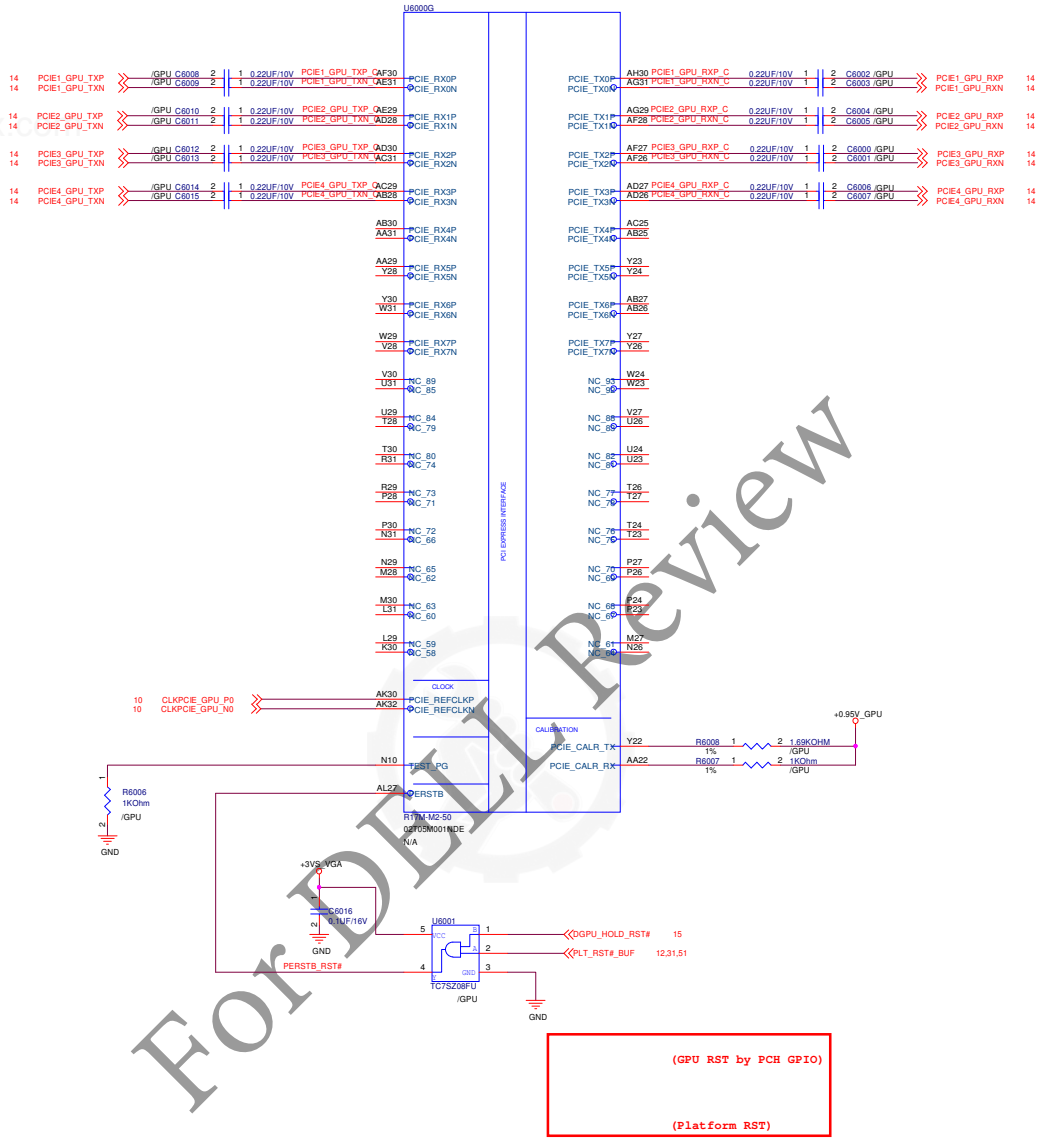
Date: Friday, August 25, 2017 Sheet 58 of 999

TYPE C VBUS Provider



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VBUS_Provider	
Pegatron Corp.	Engineer: .	
Size: C	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 59 of 999	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : dGPU_PCIEX8	
Pegatron Corp.	Engineer: .	
Size: A2	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 60 of 999	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : dGPU_IFPA/B LVDS	
Pegatron Corp.	Engineer: .	
Size: A4	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 61 of 999	

Straps Mapping

Table 3–22 Multi-level Pin Straps

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 26).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_ GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1

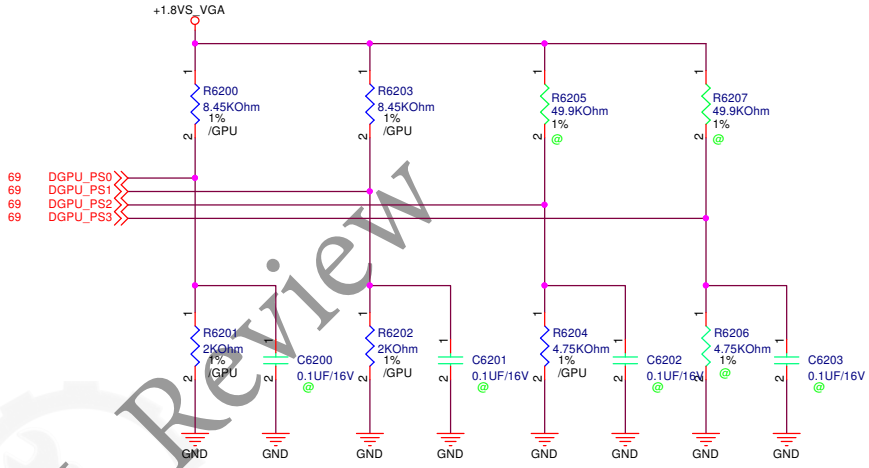


Table 3–23 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

Table 3–21 Resistor Divider Lookup Table for Bits [3:1]

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111
Note: 0402 1% resistors are required.		

Table 3–20 Capacitor Lookup Table for Bits [5:4]

Capacitor Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

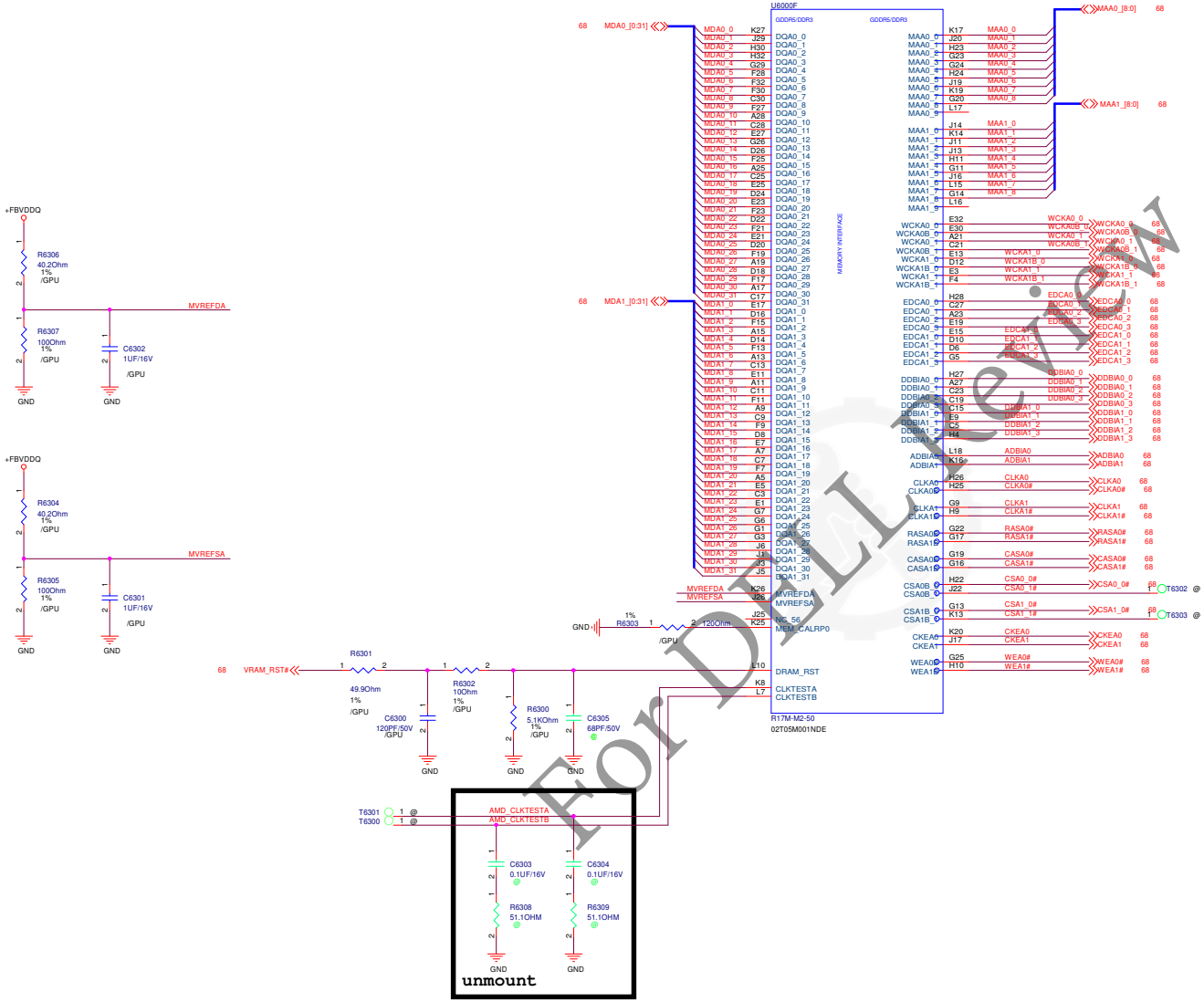
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : dGPU STRAPS

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 62 of 999



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : dGPU FBA

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A2	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 63 of 999

PEGATRON DT-MB RESTRICTED SECRET

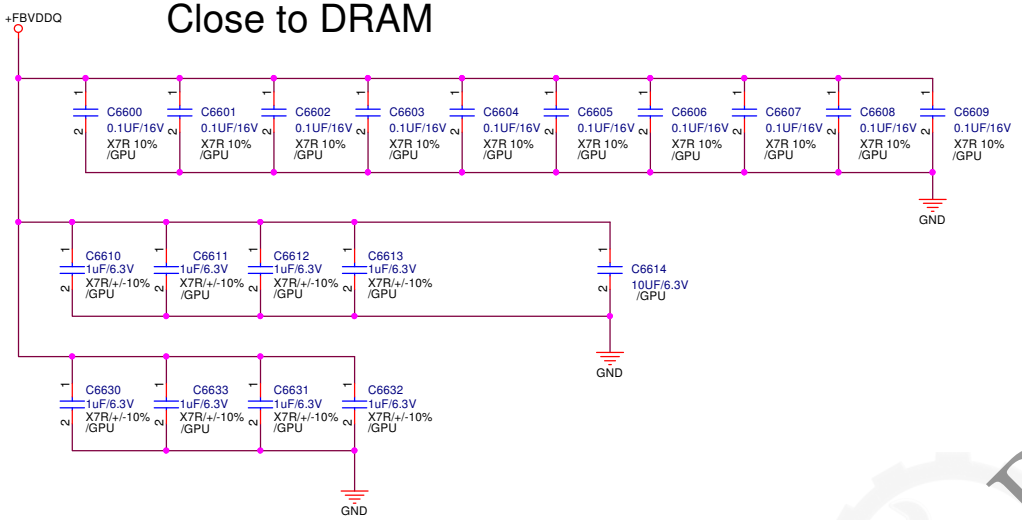
PEGATRON	Title : dGPU_NVVDD	
Pegatron Corp.	Engineer: .	
Size: A2	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 64 of 999	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : dGPU_FBVDDQ	
Pegatron Corp.	Engineer: .	
Size: A3	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 65 of 999	

Memory FBVDD/Q Decoupling

M1 & M3 Combined Close to DRAM

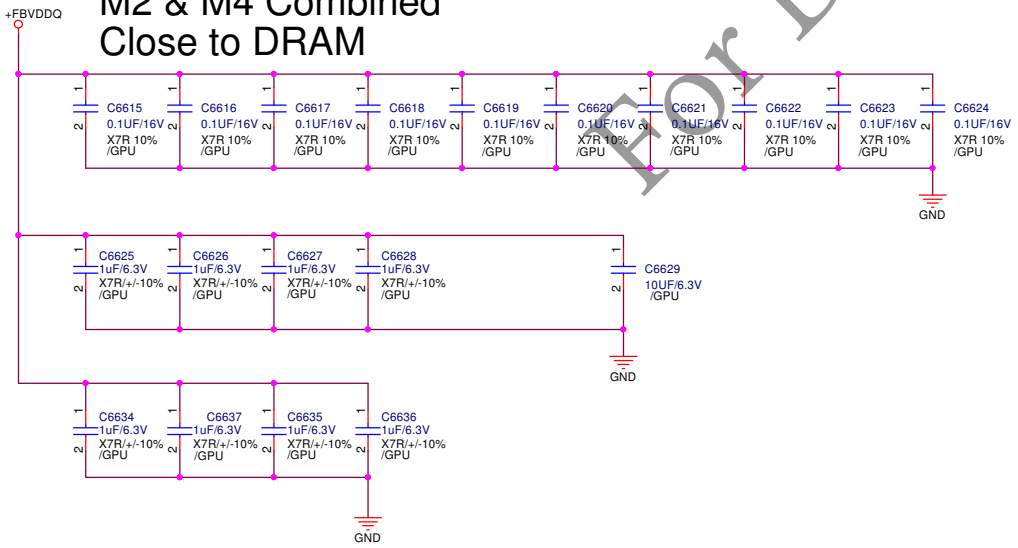


Capacitor Type	Footprint	Population[1]		Location[2]
		FBVDDQ	FBVDD	
FBVDD/Q Combined				
0.1 µF	X7R	0402	10	Under DRAM
1.0 µF	X7R	0603	4	Under DRAM
10 µF	X5R	0805	2	Close to DRAM
FBVDD/Q Separate				
0.1 µF	X7R	0402	6	6	0	Under DRAM
1.0 µF	X7R	0603	8	4	4	Under DRAM
10 µF	X5R	0805	2	1	1	Close to DRAM

Note:

1. Per sub-partition, for example, per two pieces of ×16 DRAM or one piece of ×32 DRAM.
2. Location is close to DRAM for all decoupling with ×16 DRAM.

M2 & M4 Combined Close to DRAM



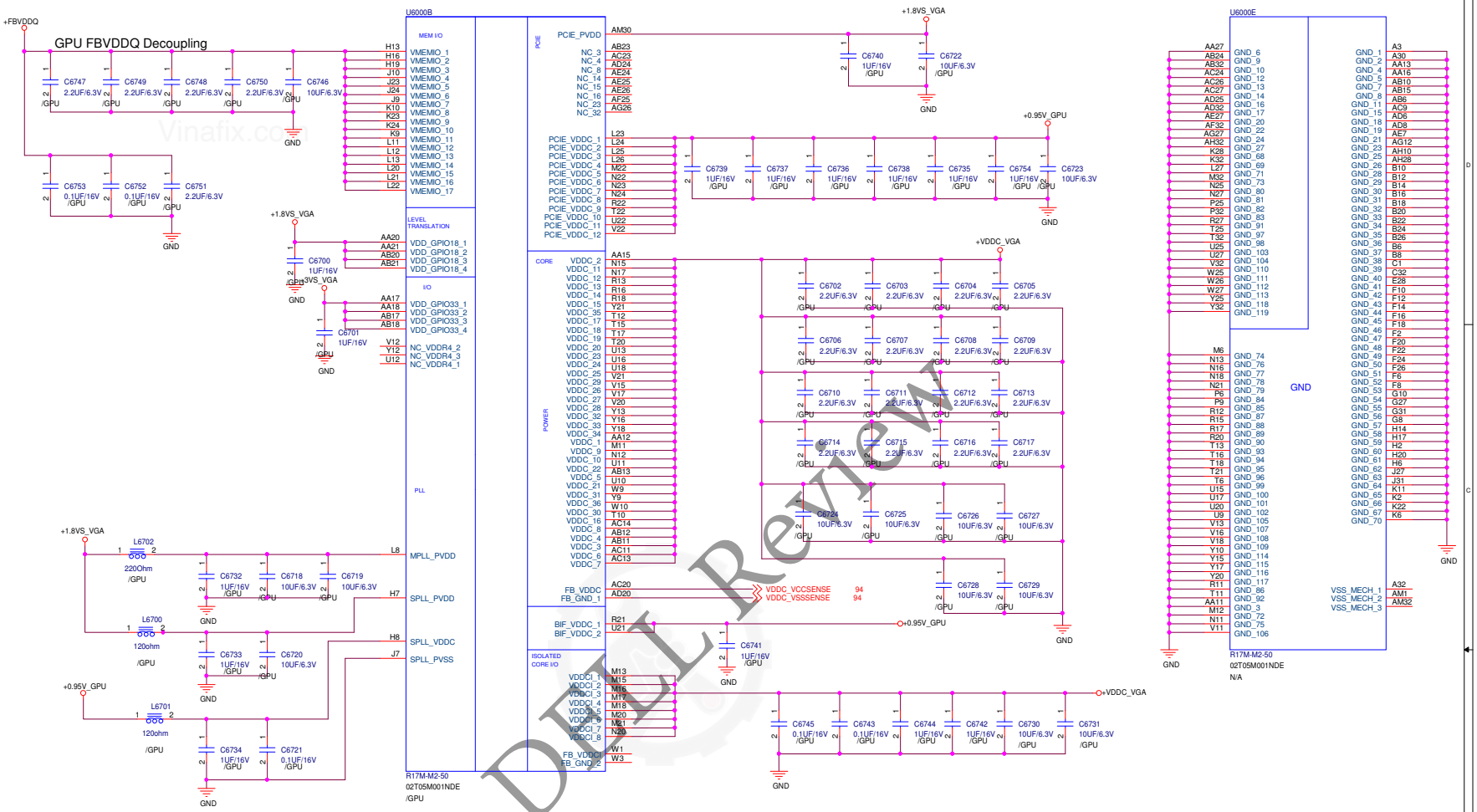
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : dGPU MEMORY DECOUP

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 66 of 999



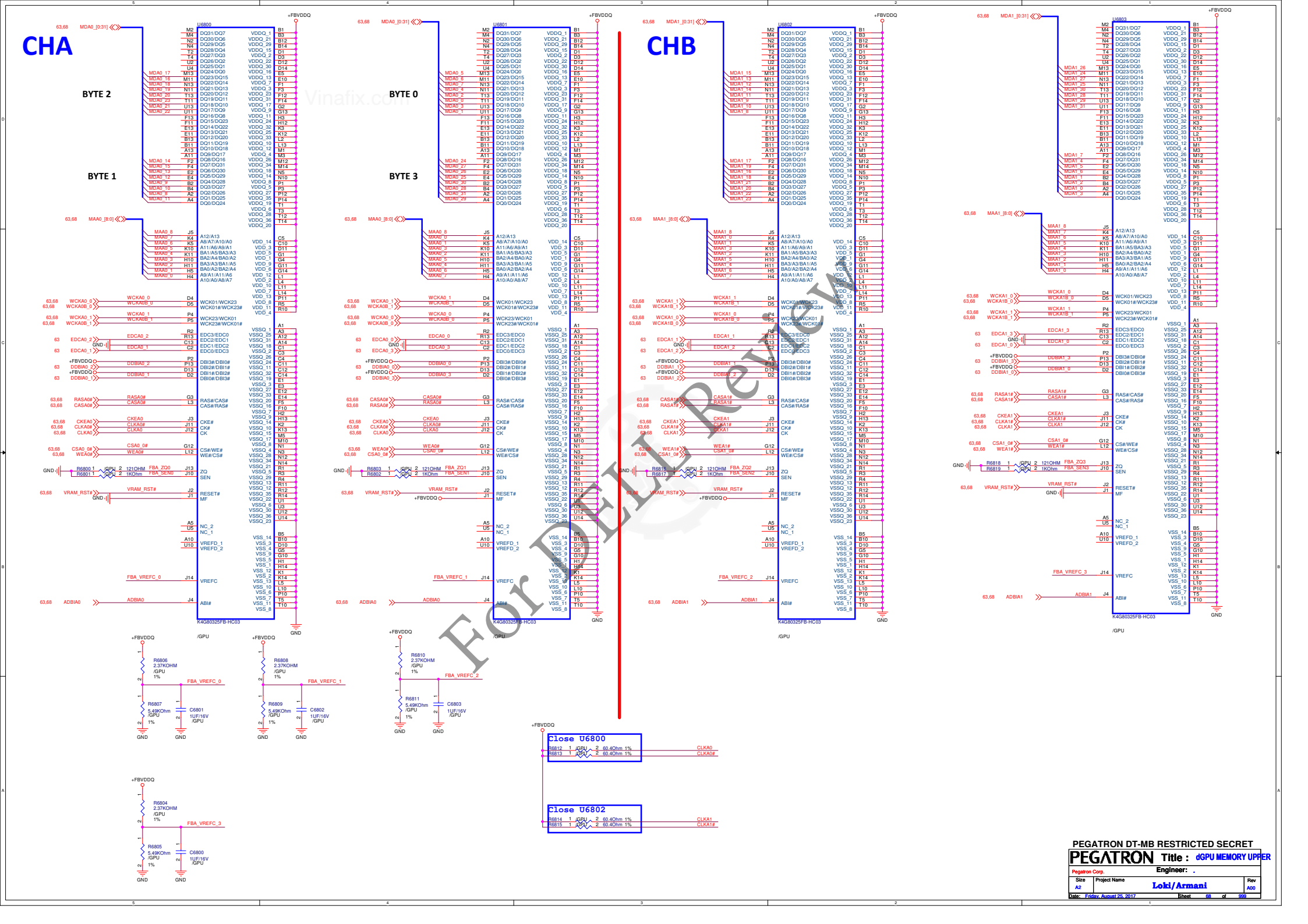
PEGATRON DT-MB RESTRICTED SECRET

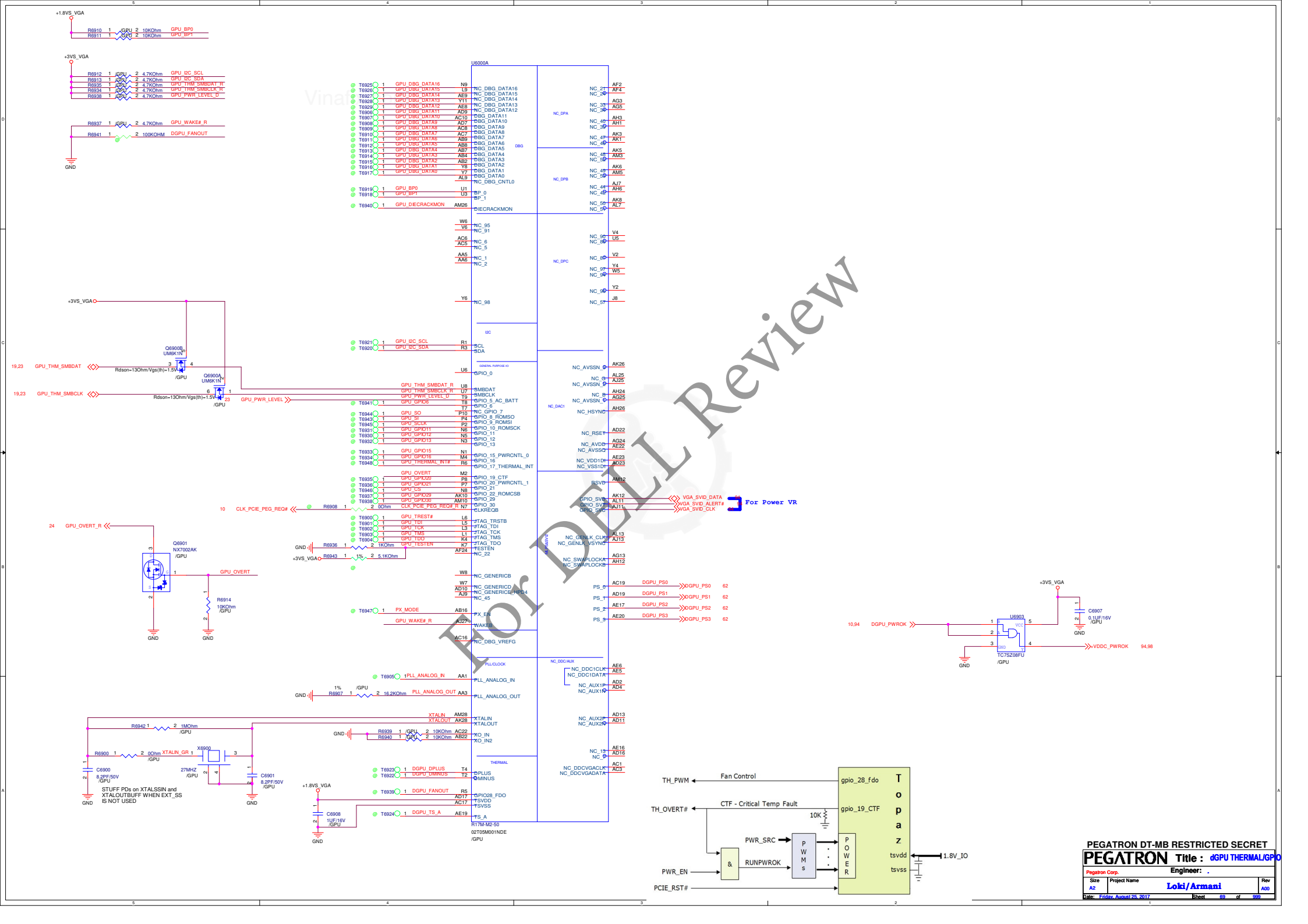
PEGATRON Title : AMD_NVVDD

Pegatron Corp. Engineer: .

Size	Project Name	Rev
C	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 67 of 999


CHA
CHB
BYTE 2
BYTE 1
BYTE 0
BYTE 3
U6800
U6801
U6802
U6803
K4G80325FB-HC03
+FBVDDQ
GND
/GPU
Close U6800
Close U6802
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : dGPU MEMORY UPPER
Pegatron Corp.
Engineer:
Size A2
Project Name Loki/Armani
Rev A00
Date: Friday, August 25, 2017
Sheet 68 of 999
For DELL Review



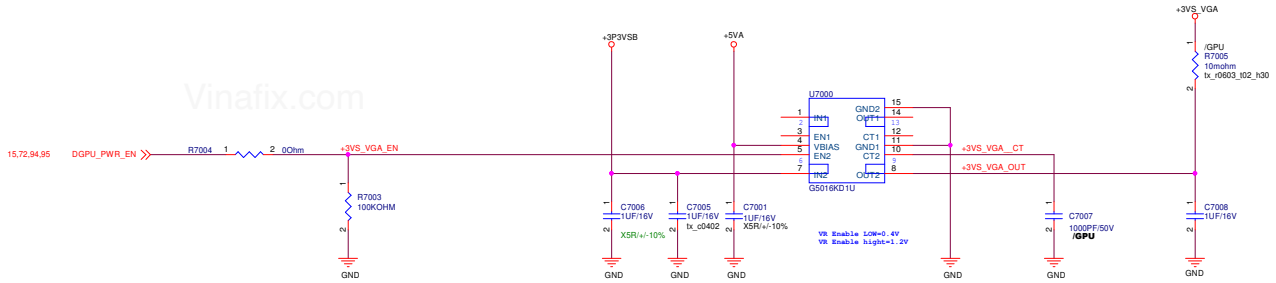
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : dGPU THERMAL/GPIO

Pegatron Corp. Engineer: .

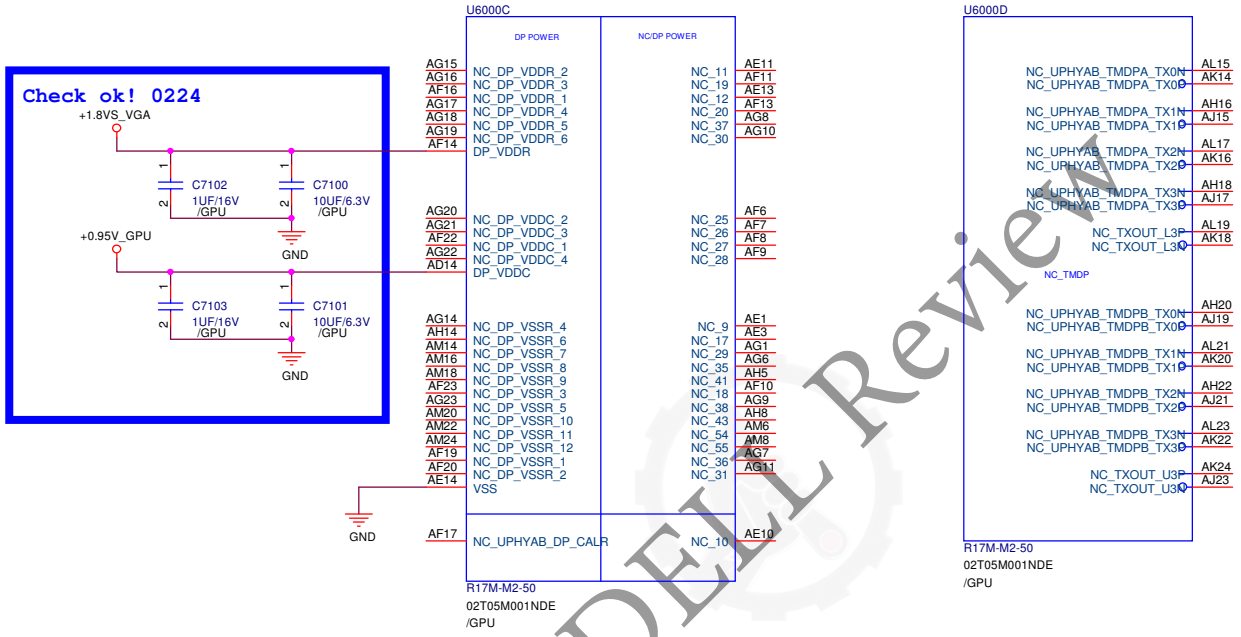
Size	Project Name	Rev
A2	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 69 of 99



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : 70.VRAM_SELF_REFRESH	
Pegatron Corp.	Engineer: .	
Size: A2	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 70 of 999	



PEGATRON DT-MB RESTRICTED SECRET

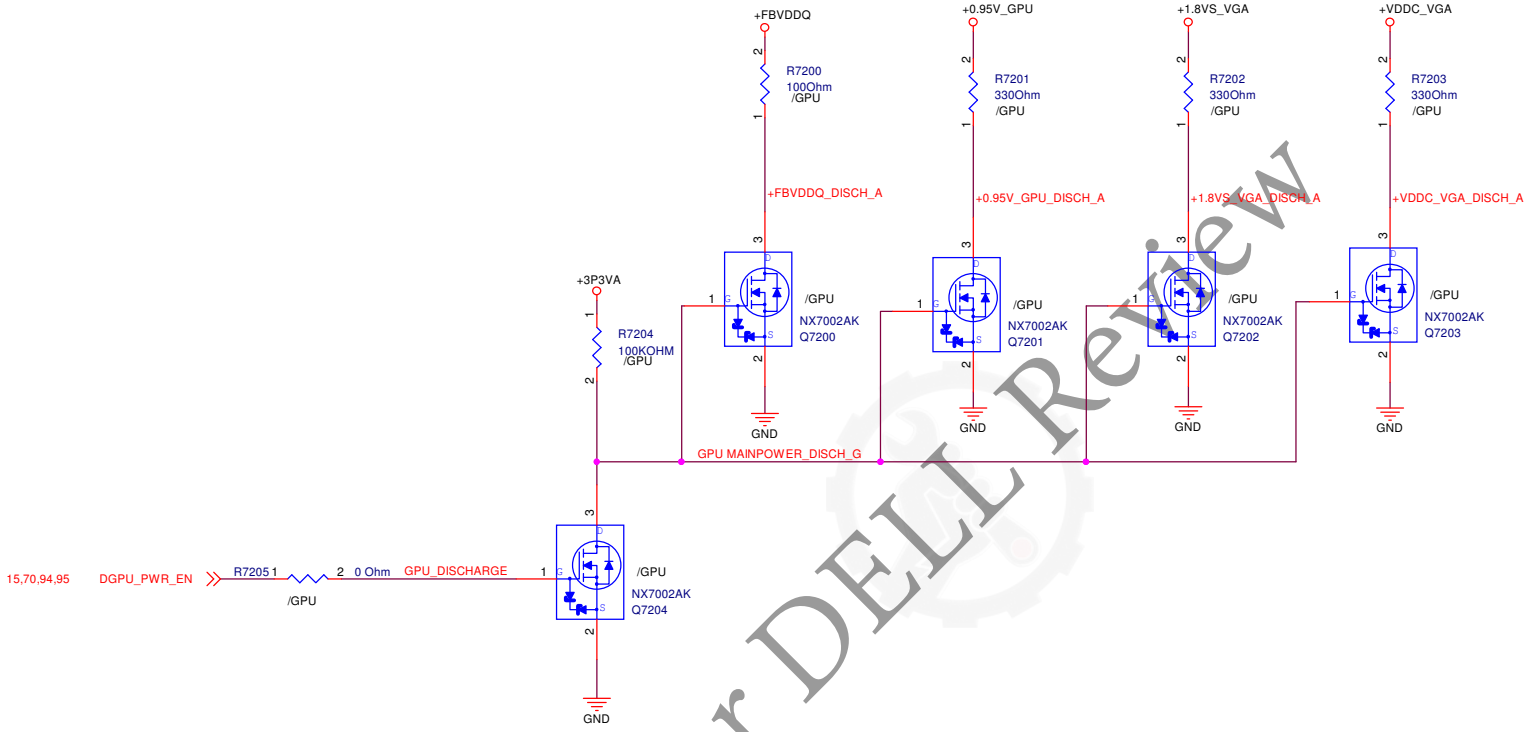
PEGATRON Title : dGPU_DP & DVI & HDMI

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 71 of 999

GPU POWER DISCHARGE



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : GPU POWER DISCHARG	
Pegatron Corp.	Engineer: .	
Size: A3	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 72 of 999	

VBUS Consumer

Imax =3A

2nd Input(USB PD 20V)
USB PD input

2 Input switch Circuit

Size:3*3;Spec.:8.6A

(3A)

EE Check Hight 单位的电源和时序 0601

DC-IN connector

Imax =3.42A

(3.42A)

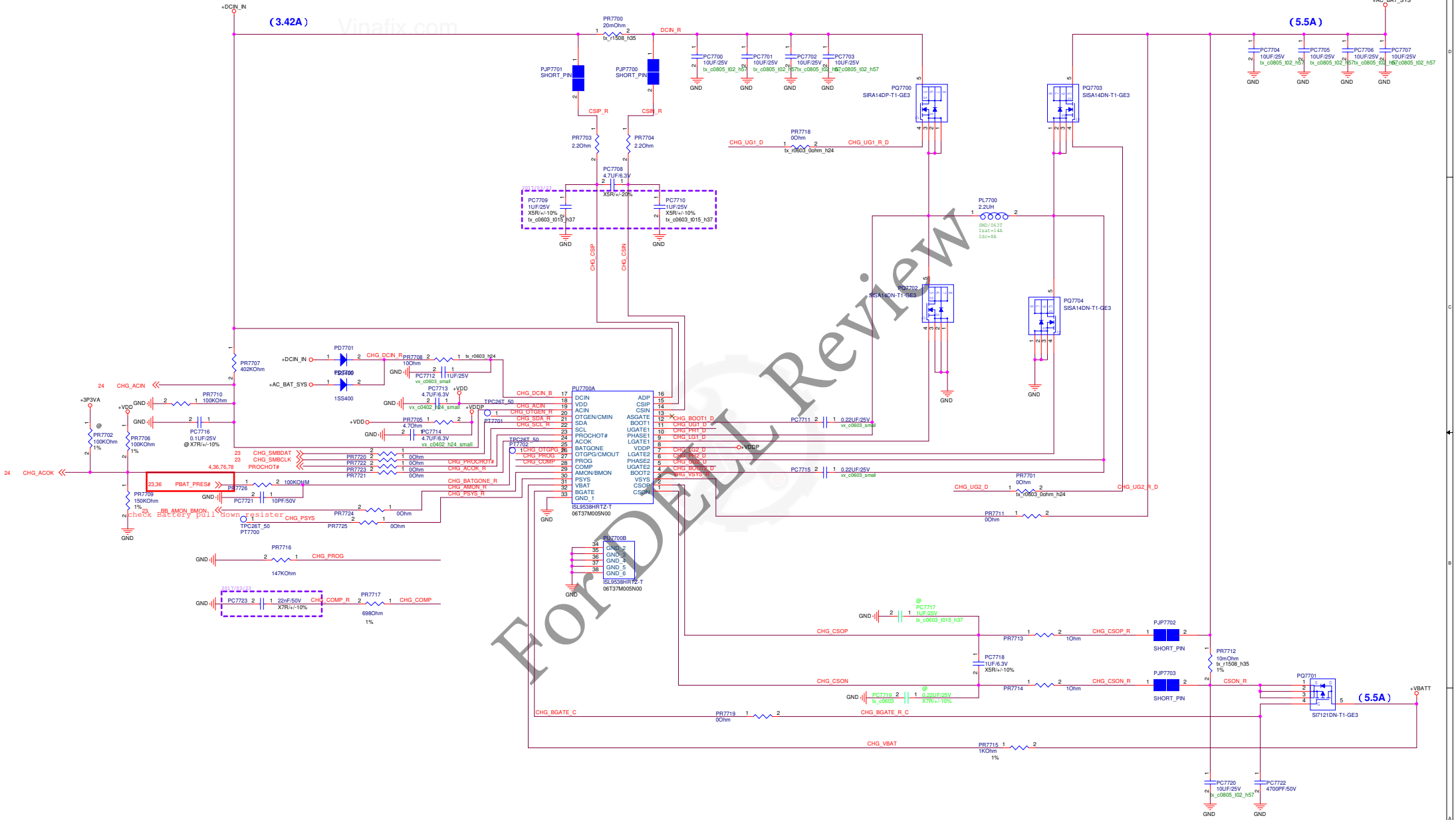
Main Input(AC Adapter 19V)

To Charger input

PSID Circuit

HW_ACAVIN_NB Circuit

Battery Protect Circuit



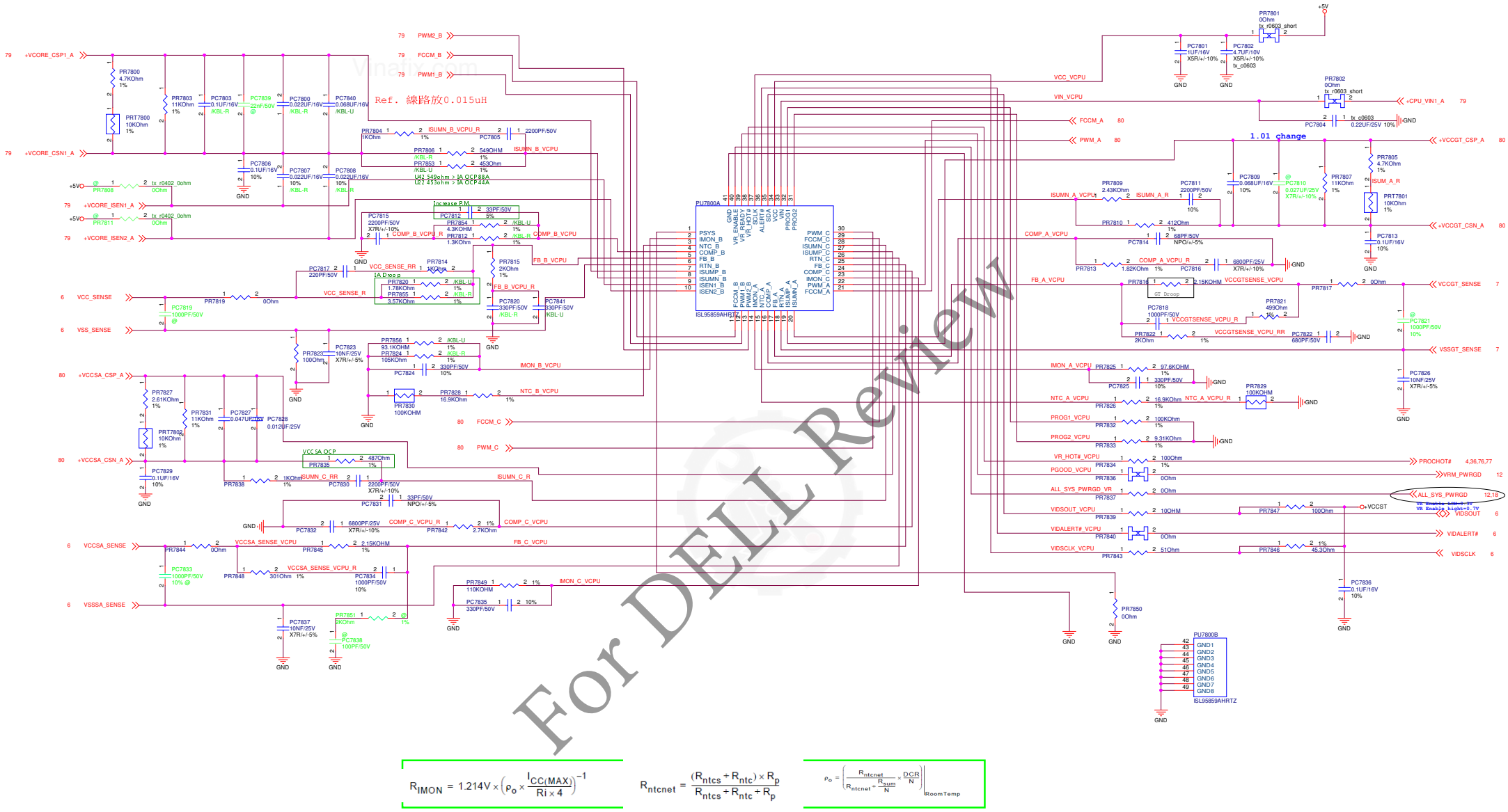
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : BB Charger

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A2	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 77 of 999



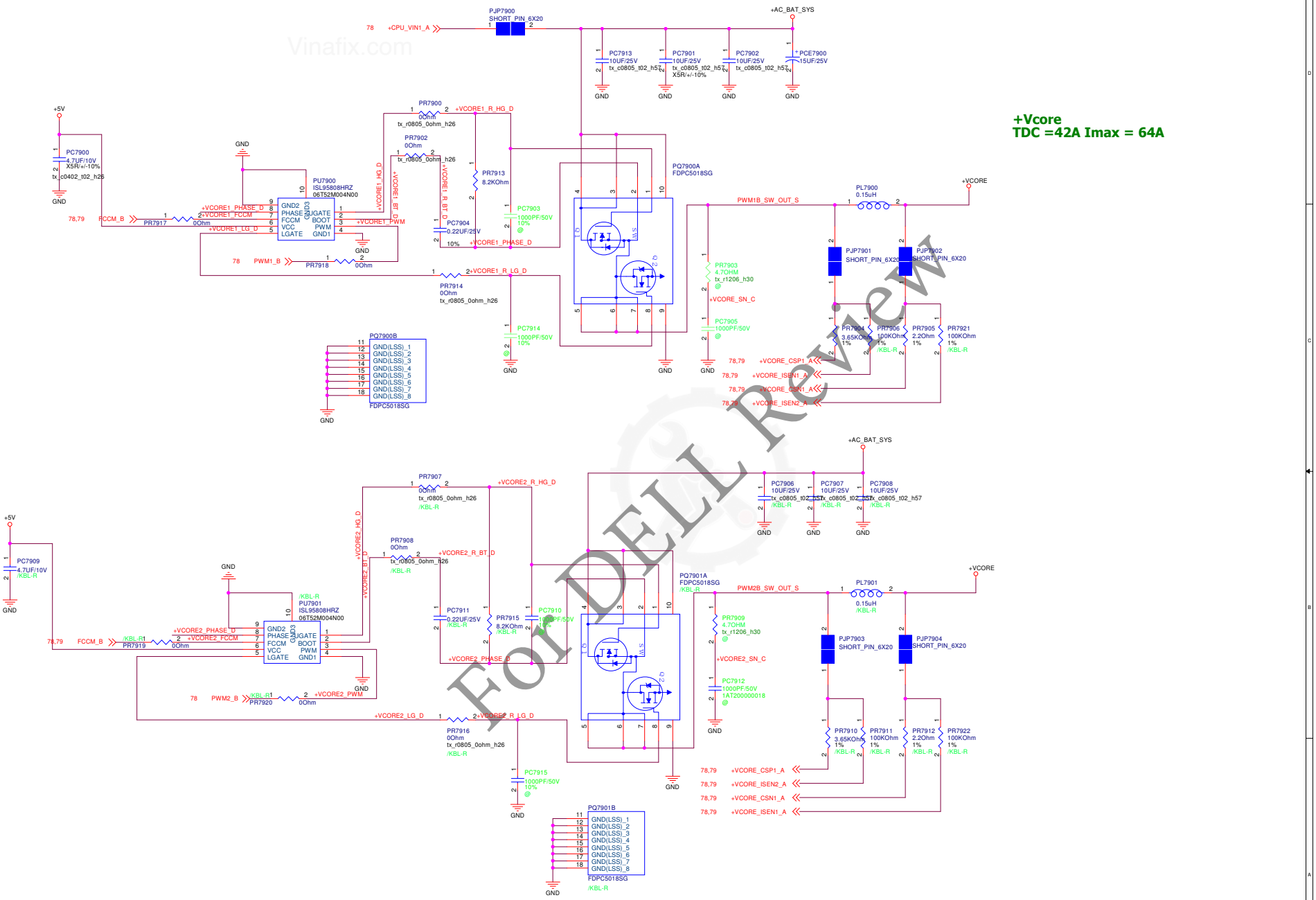
$$R_{IMON} = 1.214V \times \left(\rho_o \times \frac{I_{CC(MAX)}}{Ri \times 4}\right)^{-1}$$

$$R_{ntcnet} = \frac{(R_{ntcs} + R_{ntc}) \times R_p}{R_{ntcs} + R_{ntc} + R_p}$$

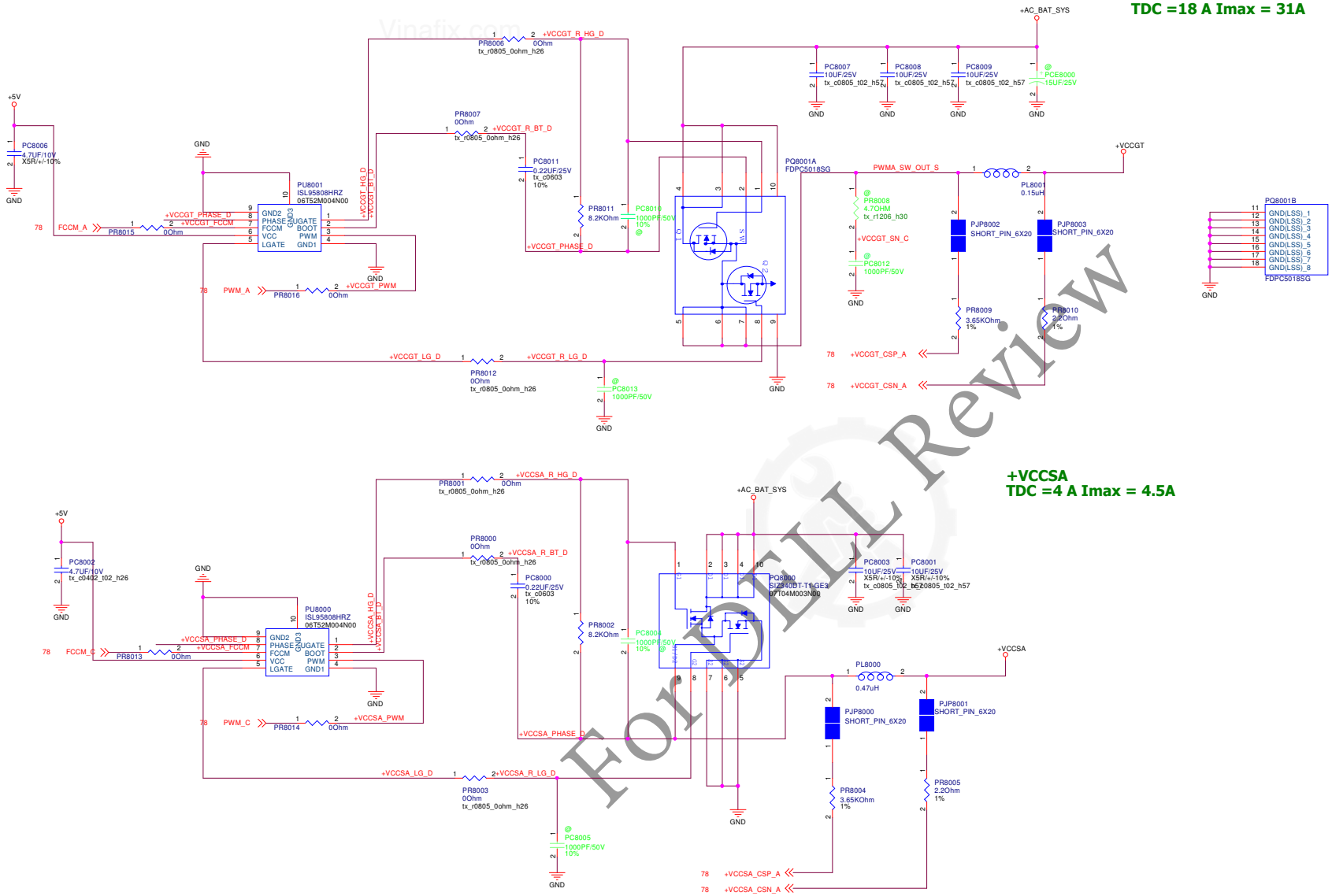
$$\rho_o = \left(\frac{R_{ntcnet}}{R_{ntcnet} + \frac{R_{sum}}{N}} \times \frac{DCR}{N}\right)\Big|_{RoomTemp}$$

PEGATRON DT-MB RESTRICTED SECRET

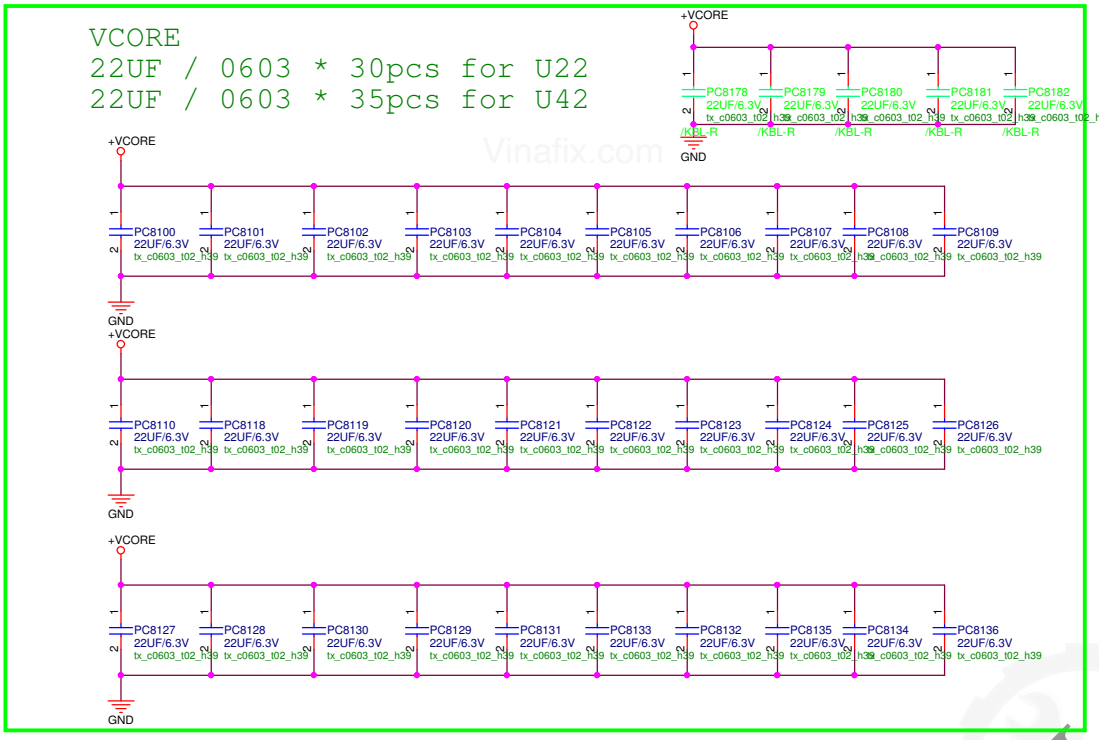
PEGATRON	Title : CPU CONTROLLER		
Pegatron Corp.	Engineer: .		
Size: A2	Project Name: Loki/Armani		Rev: A00
Date: Friday, August 25, 2017	Sheet 78 of 999		

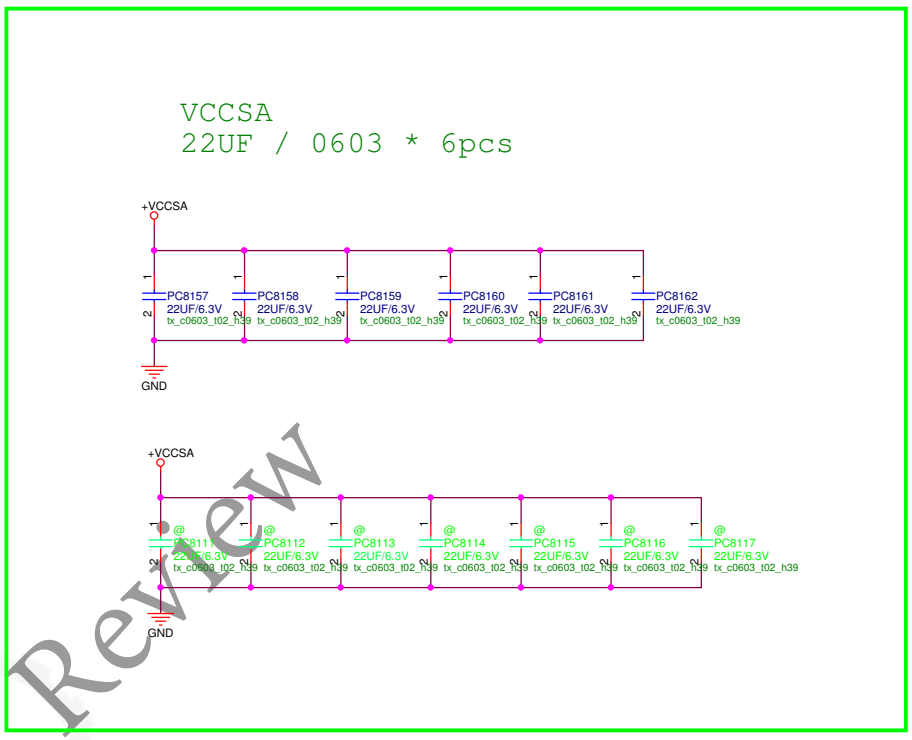


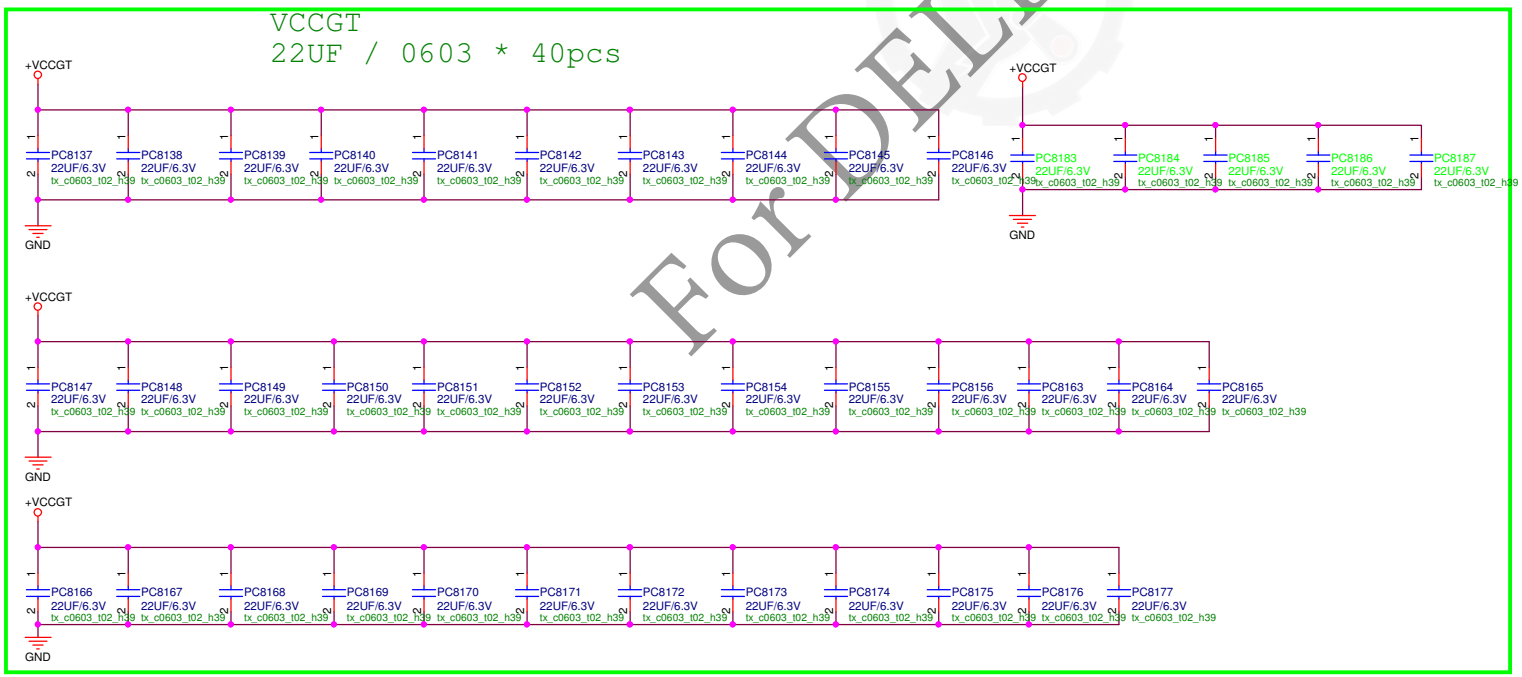
PEGATRON	Title : +VCORE		
Pegatron Corp.	Engineer: .		
Size: Custom	Project Name: Loki/Armani		Rev: A00
Date: Friday, August 25, 2017	Sheet 79 of 999		

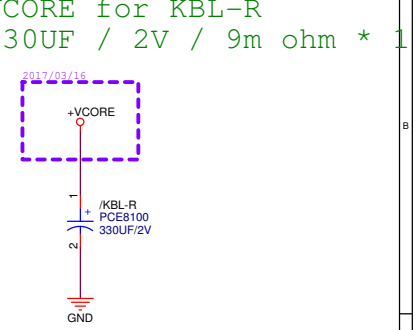


PEGATRON	Title : +VCCGT	
Pegatron Corp.	Engineer: .	
Size: Custom	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 80 of 999	









PEGATRON	Title : VR CAPACITORS	
Pegatron Corp.	Engineer: .	
Size: Custom	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 81 of 999	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +VCCIO

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A2	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 82 of 999

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +VCCPRIM_CORE

Pegatron Corp. Engineer: .

Size	Project Name	Rev
A2	Loki/Armani	A00

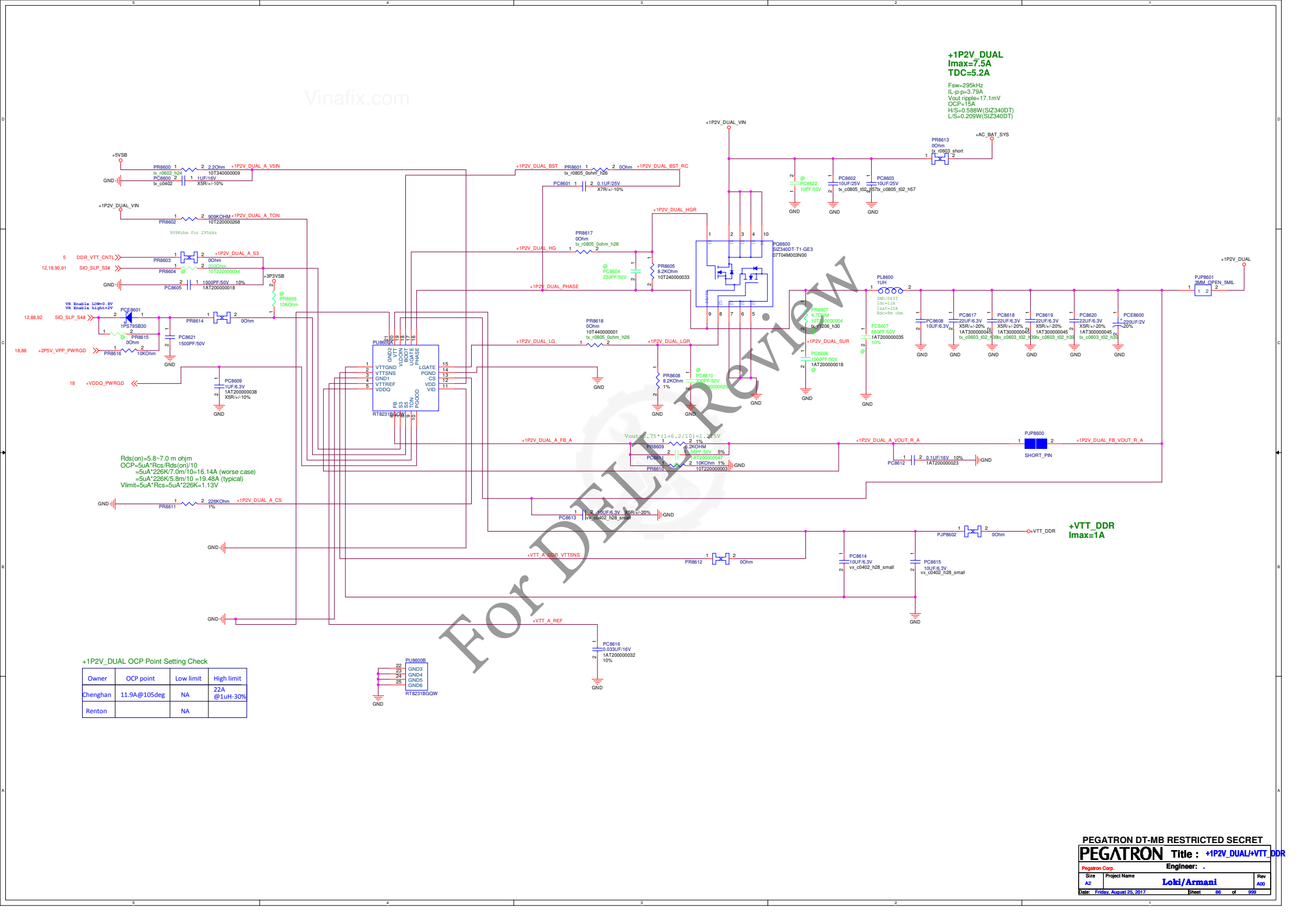
Date: Friday, August 25, 2017 Sheet 83 of 999

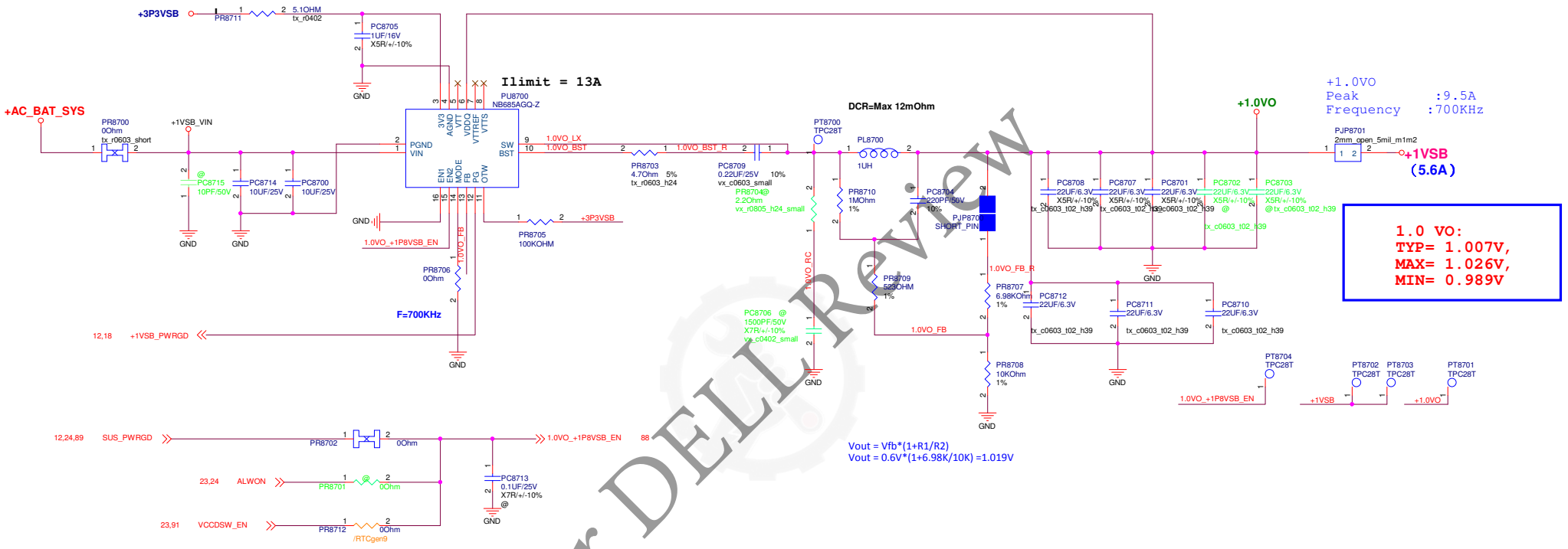
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +VCCEDRAM	
Pegatron Corp.	Engineer: .	
Size: A2	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 84 of 999	

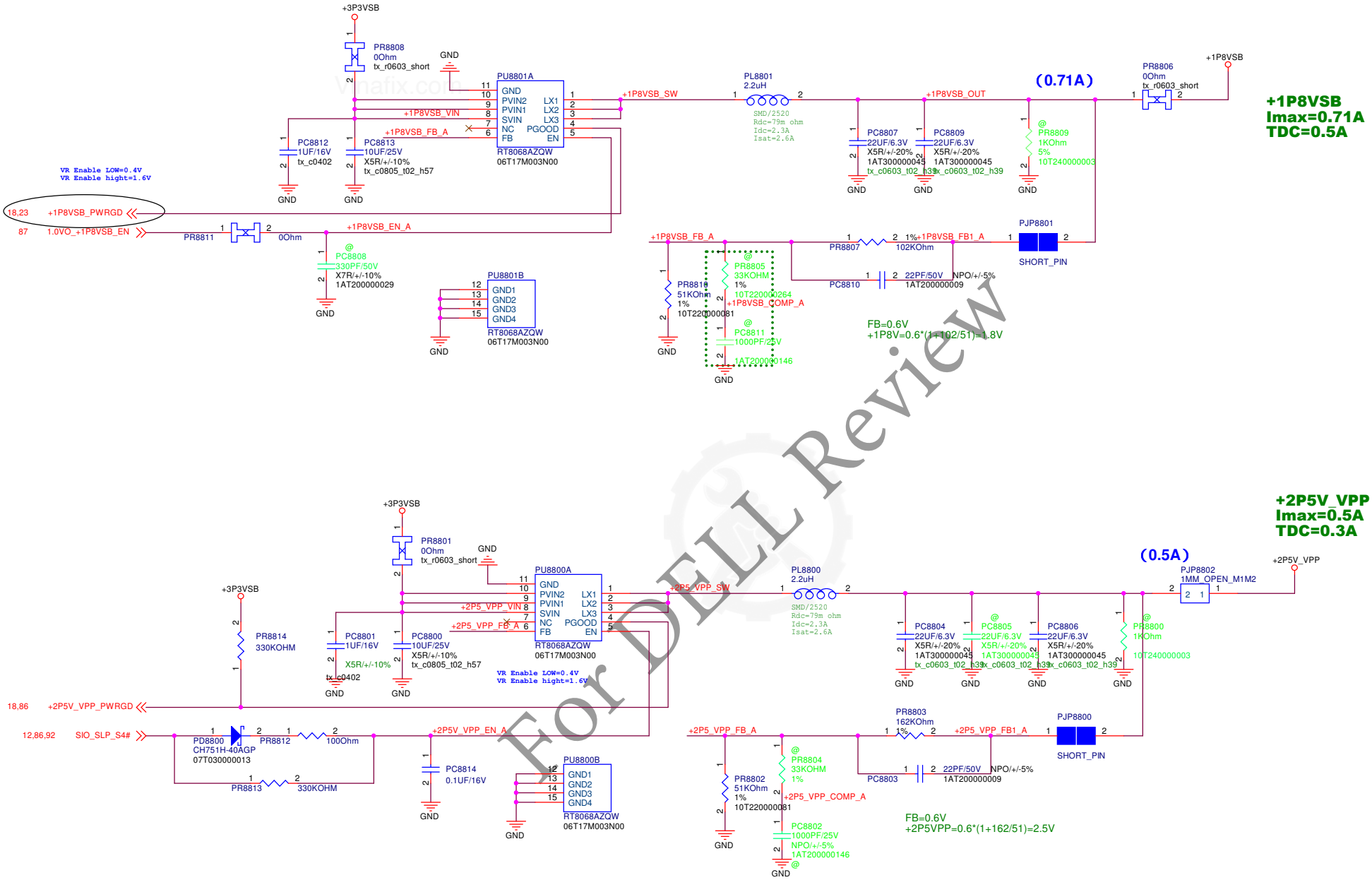
PEGATRON DT-MB RESTRICTED SECRET

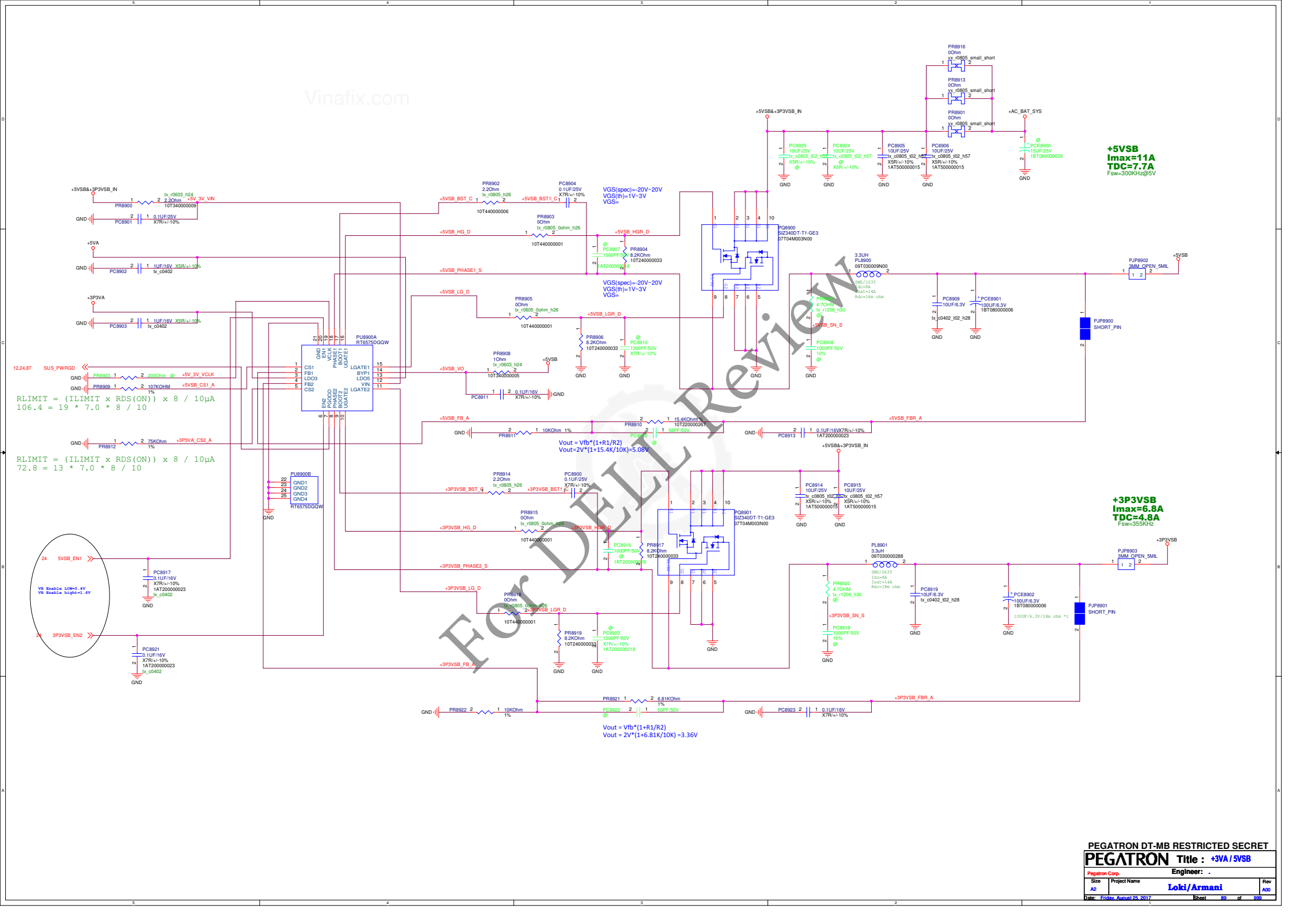
PEGATRON	Title : +VCCEOPIO	
Pegatron Corp.	Engineer: .	
Size: A2	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 85 of 999	

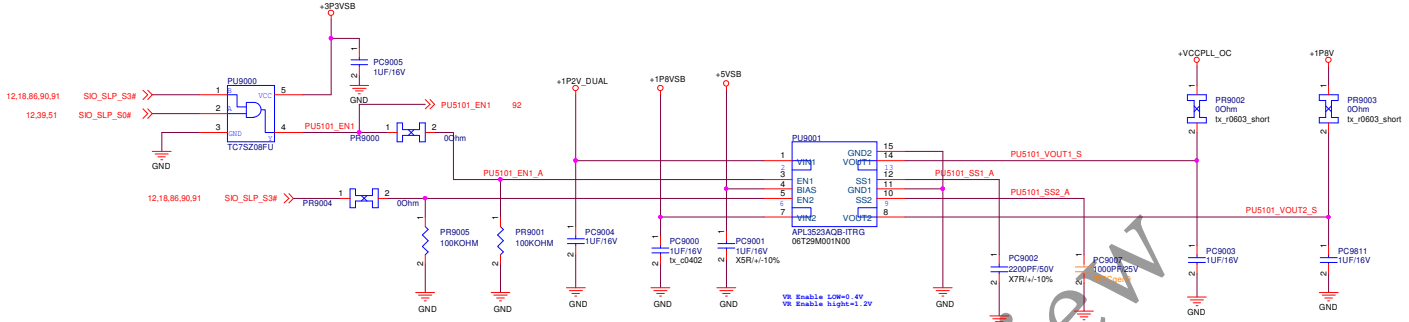

+1P2V_DUAL
Imax=7.5A
TDC=5.2A
Fsw=295kHz
IL-p-p=3.79A
Vout ripple=17.1mV
OCP=15A
H/S=0.588W(SIZ340DT)
L/S=0.209W(SIZ340DT)
+1P2V_DUAL_VIN
+AC_BAT_SYS
+5VSB
+3P3VSB
PR8600 2.2Ohm +1P2V_DUAL_A_VSIN
PR8601 0Ohm +1P2V_DUAL_BST_RC
PR8602 909KOHM +1P2V_DUAL_A_TON
909Kohm for 295kHz
PR8603 0Ohm DDR_VTT_CNTL
PR8604 200Ohm SIO_SLP_S3#
PC8605 1000PF/50V 10% 1AT200000018
PR8606 10KOhm
PR8607 4.7Ohm
PR8608 8.2KOhm 1%
PR8609 6.2KOHM 1%
PR8610 10KOhm 1% 10T220000003
PR8611 226KOhm 1%
PR8612 0Ohm
PR8613 0Ohm tx_r0603_short
PR8614 0Ohm SIO_SLP_S4#
PR8615 0Ohm
PR8616 10KOhm +2P5V_VPP_PWRGD
PR8617 0Ohm tx_r0805_0ohm_h26
PR8618 0Ohm 10T440000001
PC8601 0.1UF/25V X7R/+/-10%
PC8602 10UF/25V
PC8603 10UF/25V
PC8604 330PF/50V
PC8606 1000PF/50V 1AT200000018
PC8607 680PF/50V 10% 1AT200000035
PC8608 10UF/6.3V
PC8609 1UF/6.3V 1AT200000038 X5R/+/-10%
PC8610 33PF/50V 1AT200000025
PC8612 0.1UF/16V 10% 1AT200000023
PC8613 10UF/6.3V X5R/+/-20% vx_c0402_h28_small
PC8614 10UF/6.3V vx_c0402_h28_small
PC8615 10UF/6.3V vx_c0402_h28_small
PC8616 0.033UF/16V 1AT200000032
PC8621 1500PF/50V
PC8622 10PF/50V
PCE8601 1PS79SB30
PCE8600 220UF/2V
PL8600 1UH
PJP8600 SHORT_PIN
PJP8601 3MM_OPEN_5MIL
PJP8602 0Ohm
PQ8600 SIZ340DT-T1-GE3 07T04M003N00
PU8600A RT8231BGQW
PU8600B RT8231BGQW
+1P2V_DUAL_BST
+1P2V_DUAL_HGR
+1P2V_DUAL_HG
+1P2V_DUAL_PHASE
+1P2V_DUAL_LG
+1P2V_DUAL_LGR
+1P2V_DUAL_SUR
+1P2V_DUAL_A_FB_A
+1P2V_DUAL_A_VOUT_R_A
+1P2V_DUAL_FB_VOUT_R_A
+1P2V_DUAL_A_CS
+VTT_A_DDR_VTTSNS
+VTT_A_REF
+VTT_DDR
Imax=1A
Vout=0.75*(1+6.2/10)=1.215V
Rds(on)=5.8~7.0 m ohjm
OCP=5uA*Rcs/Rds(on)/10
=5uA*226K/7.0m/10~16.14A (worse case)
=5uA*226K/5.8m/10 =19.48A (typical)
Vlimit=5uA*Rcs=5uA*226K=1.13V
+1P2V_DUAL OCP Point Setting Check
Owner | OCP point | Low limit | High limit
Chenghan | 11.9A@105deg | NA | 22A @1uH-30%
Renton | | NA |
For DELL Review
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : +1P2V_DUAL/+VTT_DDR
Pegatron Corp. Engineer: .
Size A2 | Project Name Loki/Armani | Rev A00
Date: Friday, August 25, 2017 Sheet 86 of 999



PEGATRON	Title : 1VSB	
Pegatron Corp.	Engineer: .	
Size: Custom	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 87 of 999	



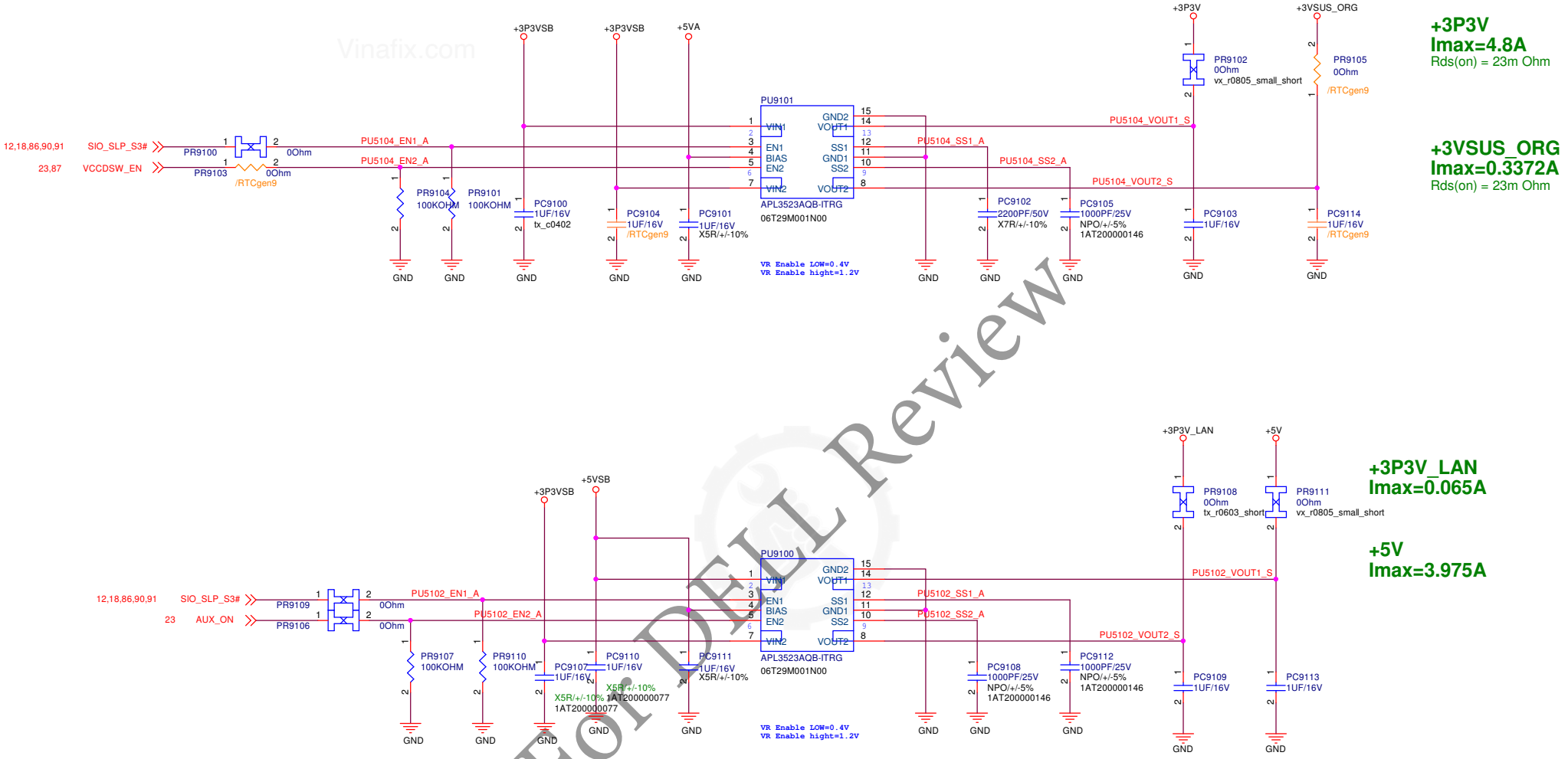

+5VSB
Imax=11A
TDC=7.7A
Fsw=300KHz@5V
+3P3VSB
Imax=6.8A
TDC=4.8A
Fsw=355KHz
RLIMIT = (ILIMIT x RDS(ON)) x 8 / 10µA
106.4 = 19 * 7.0 * 8 / 10
RLIMIT = (ILIMIT x RDS(ON)) x 8 / 10µA
72.8 = 13 * 7.0 * 8 / 10
Vout = Vfb*(1+R1/R2)
Vout=2V*(1+15.4K/10K)=5.08V
Vout = Vfb*(1+R1/R2)
Vout = 2V*(1+6.81K/10K) =3.36V
VGS(spec)=-20V~20V
VGS(th)=1V~3V
VGS=
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : +3VA / 5VSB
Pegatron Corp. Engineer: .
Size A2 | Project Name Loki/Armani | Rev A00
Date: Friday, August 25, 2017 Sheet 89 of 999
For DELL Review
Vinafix.com



+VCCPLL_OC
Imax=0.1A
Rds(on) = 23m Ohm

+1P8V
Imax=0.53A
Rds(on) = 23m Ohm

PEGATRON	Title : Load Switch 1	
Pegatron Corp.	Engineer: .	
Size: A2	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 90 of 999	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : Load Switch 2

Pegatron Corp. Engineer: .

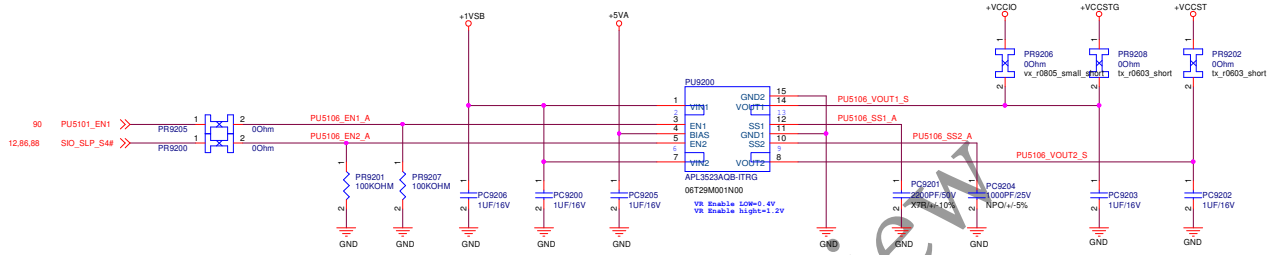
Size	Project Name	Rev
A3	Loki/Armani	A00

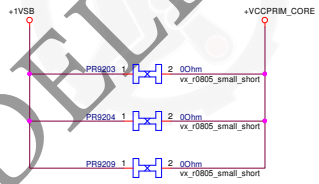
Date: Friday, August 25, 2017 Sheet 91 of 999

+VCCSTG
Imax=0.04A TDC=0.028A

+VCCST
Imax=0.24A TDC=0.168A

+VCCIO Imax=3.44A/ TDC=2.41A





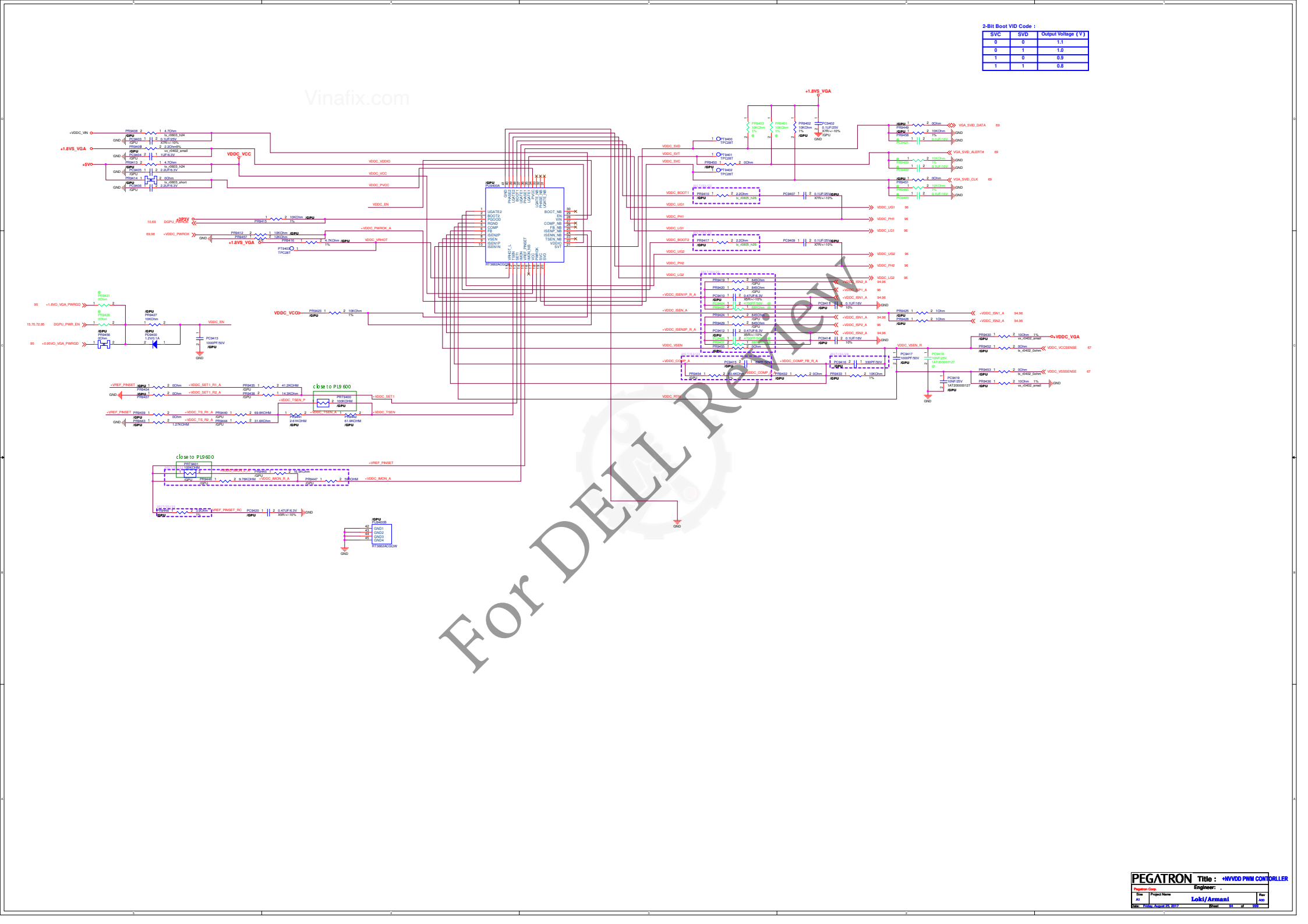
+VCCPRIM_CORE
Imax = 6.21A

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : Load Switch3	
Pegatron Corp.	Engineer: .	
Size: A2	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 92 of 999	

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : LDO1		
Pegatron Corp.	Engineer: .	
Size: A3	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 93 of 999	



PEGATRON Title : +NVVDD PWM CONTORLLER

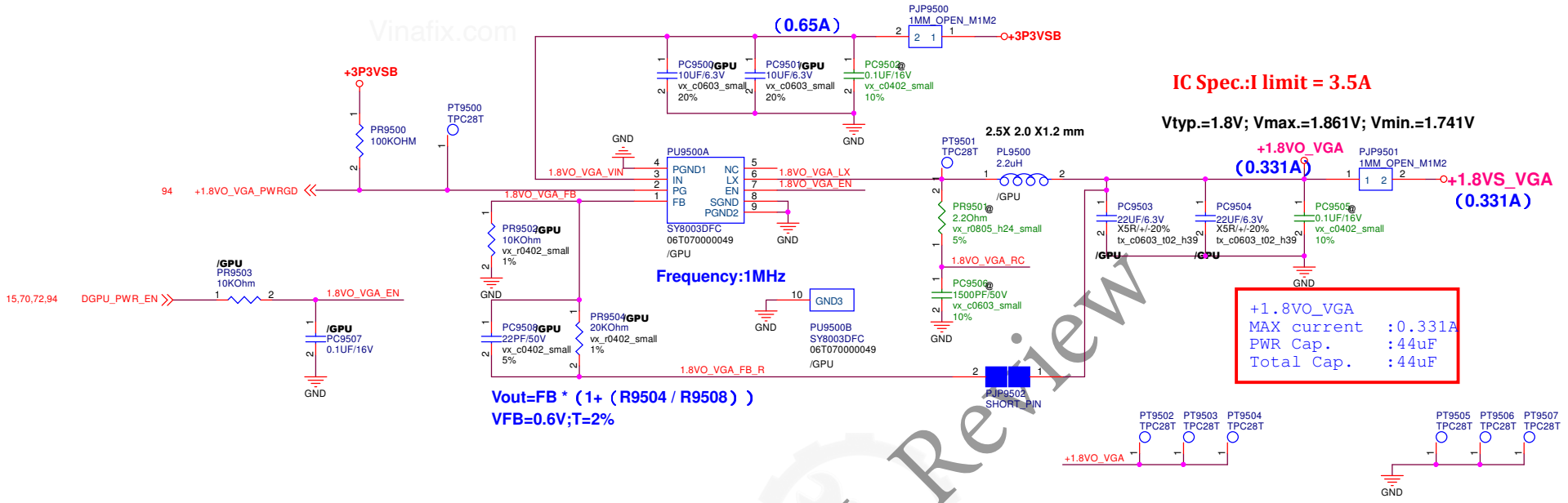
Engineer:

Pegatron Corp.

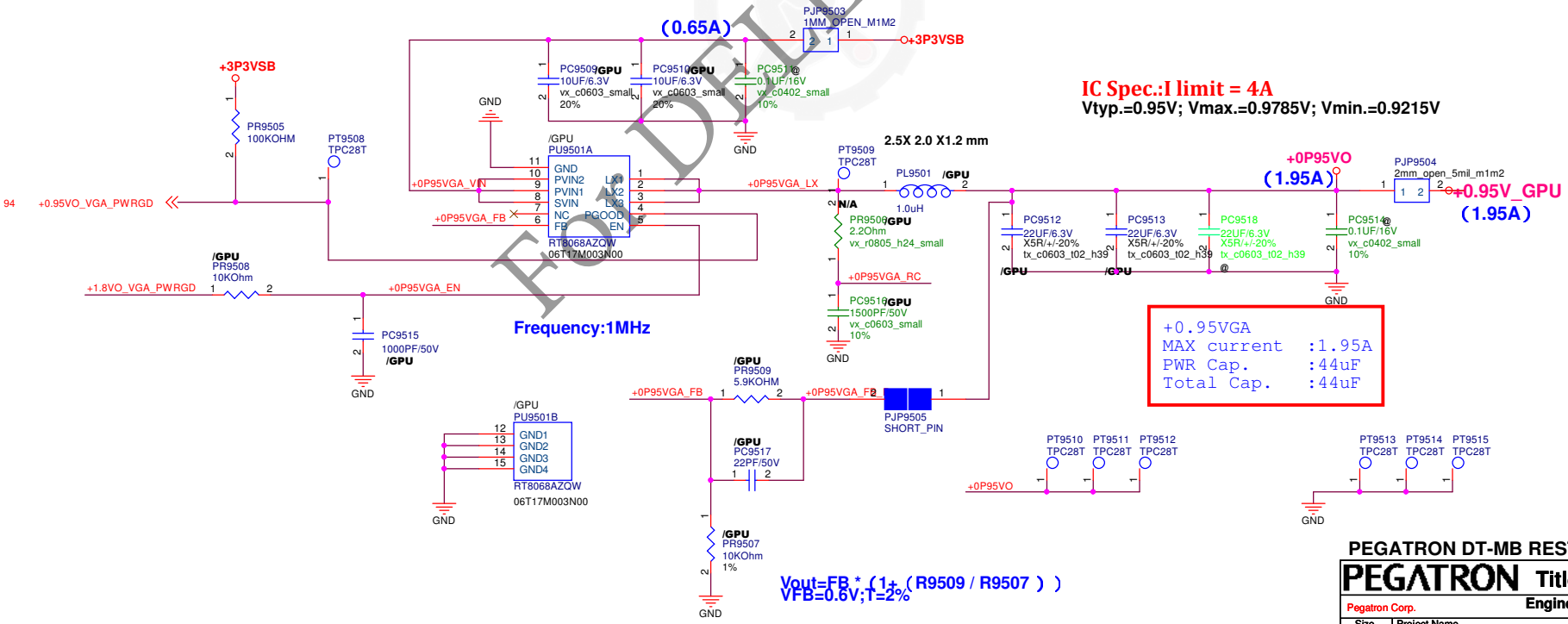
Size	Project Name	Rev
A1	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 94 of 99

+1.8VGA POWER SUPPLY



+0.95VGA POWER SUPPLY



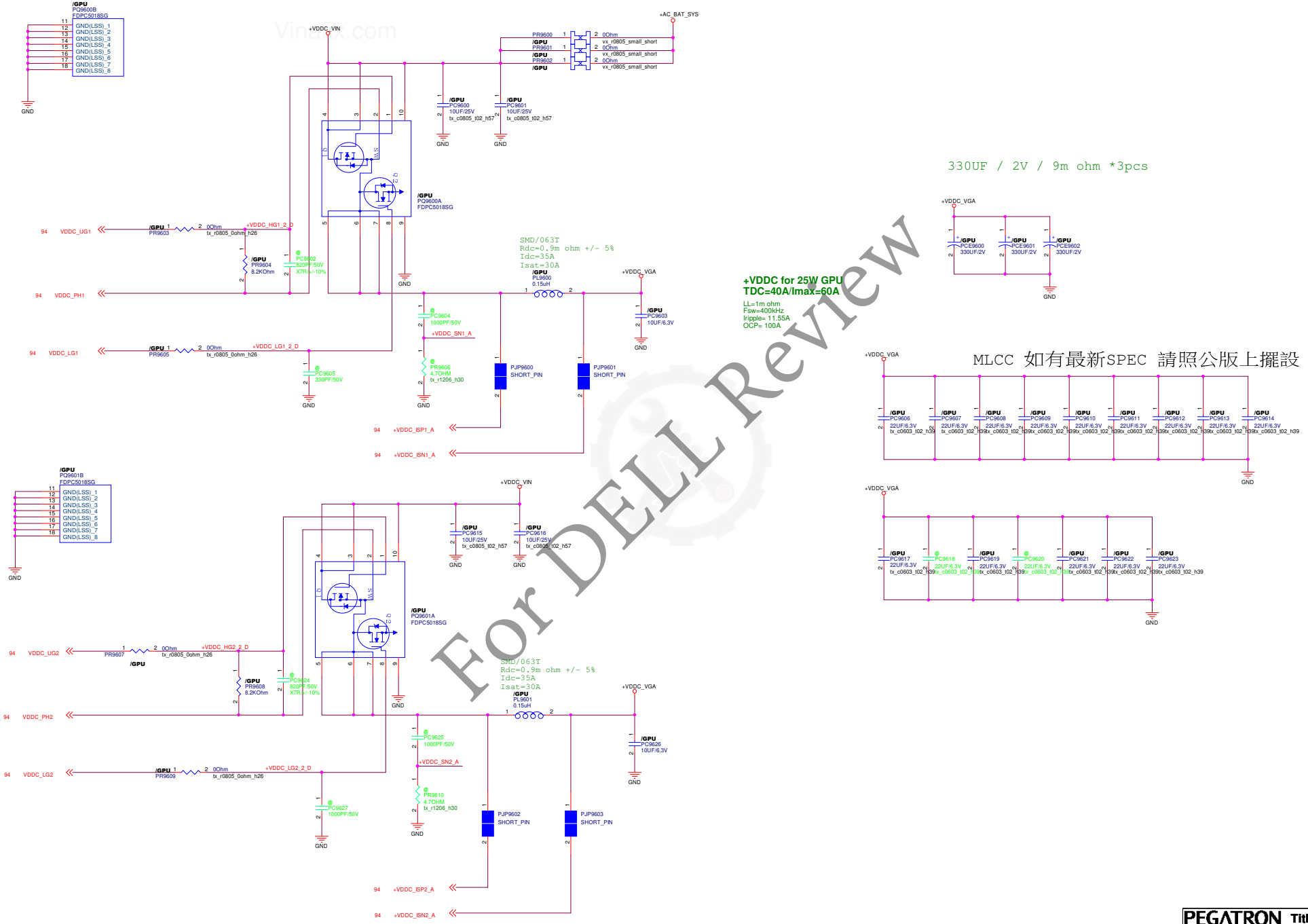
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +NVVDD PHASE

Pegatron Corp. Engineer: .

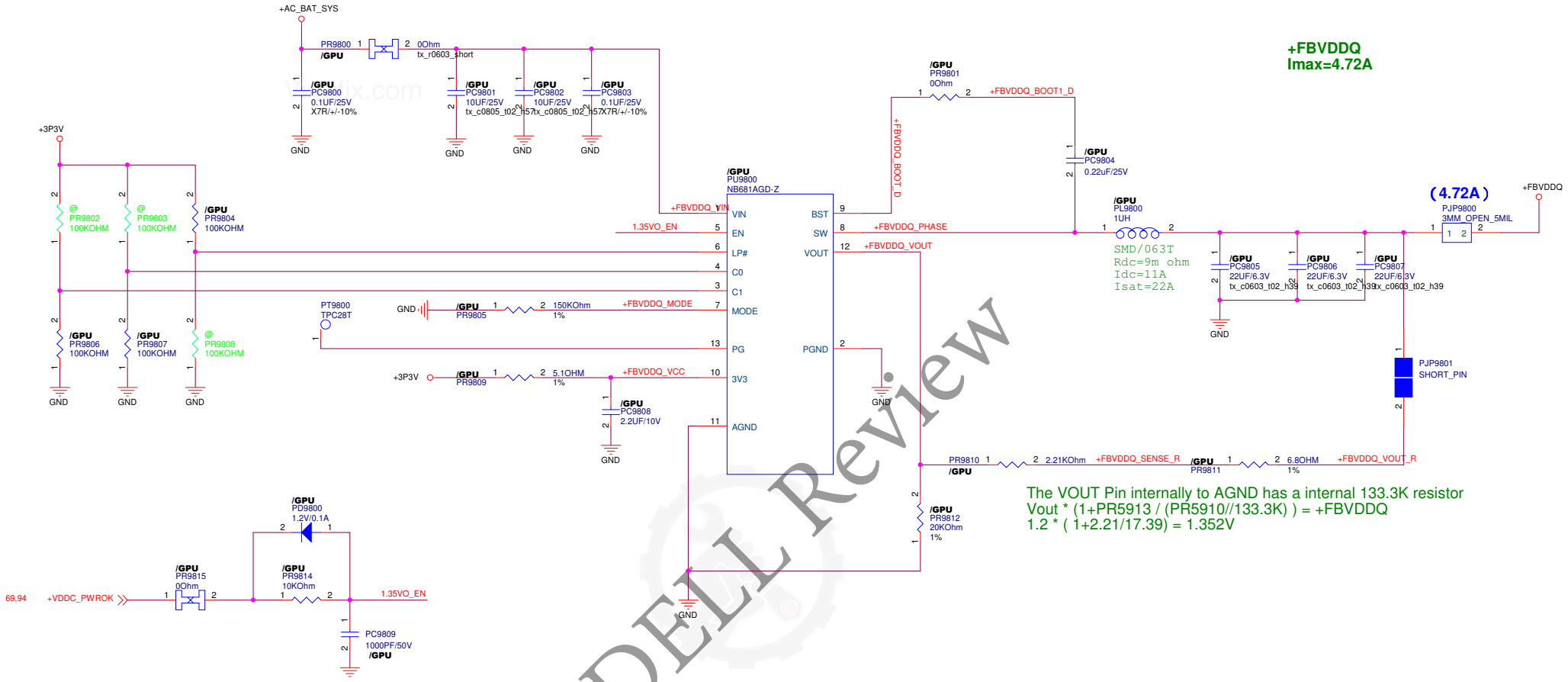
Size	Project Name	Rev
A3	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 95 of 999



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +1P05VSB	
Pegatron Corp.	Engineer: .	
Size: A3	Project Name: Loki/Armani	Rev: A00
Date: Friday, August 25, 2017	Sheet 97 of 999	



The VOUT Pin internally to AGND has a internal 133.3K resistor
Vout * (1+PR5913 / (PR5910//133.3K)) = +FBVDDQ
1.2 * (1+2.21/17.39) = 1.352V

	LP#	C1	C0	VOUT(V)
Others (Fixed design only, not allowed for changing on-the-fly)	0	0	0	1.59
	0	0	1	1.99
	0	1	0	2.38
	0	1	1	3.3
	1	0	0	1.2
	1	0	1	1.5
	1	1	0	1.8
	1	1	1	2.5

PEGATRON Title : FBVDDQ

Pegatron Corp. Engineer: .

Size	Project Name	Rev
Custom	Loki/Armani	A00

Date: Friday, August 25, 2017 Sheet 98 of 999