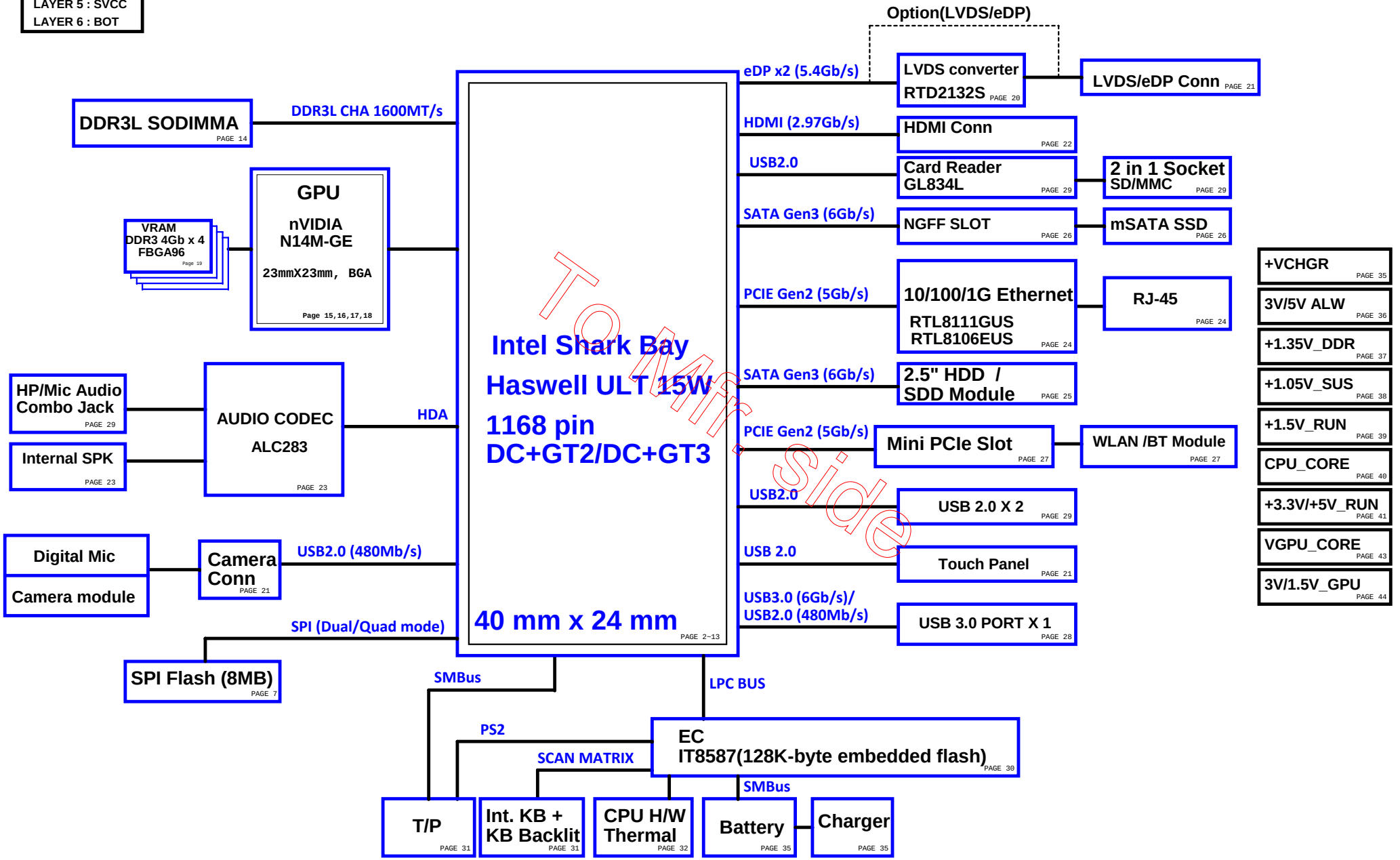
PCB STACK UP 6L

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

ST6/6A 14" OPTIMUS
INTEL SHARK BAY ULT ONE CHIP PLATFORM

1



PROJECT : ST6A
Quanta Computer Inc.
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System Block Diagram
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+VCCIOA_OUT 9
+3.3V_RUN 4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42

Haswell ULT (DISPLAY)

INT. HDMI

U26A — HSW_ULT_DDR3L — DDI — EDP — 1 OF 19

22 HDMI_TX2-_C	C450	0.1U/10V/X5R_4	INT_HDMI_TXN0	C51	DDI1_TXN0
22 HDMI_TX2+_C	C451	0.1U/10V/X5R_4	INT_HDMI_TXP0	C50	DDI1_TXP0
22 HDMI_TX1-_C	C447	0.1U/10V/X5R_4	INT_HDMI_TXN1	C53	DDI1_TXN1
22 HDMI_TX1+_C	C446	0.1U/10V/X5R_4	INT_HDMI_TXP1	B54	DDI1_TXP1
22 HDMI_TX0-_C	C453	0.1U/10V/X5R_4	INT_HDMI_TXN2	C49	DDI1_TXN2
22 HDMI_TX0+_C	C452	0.1U/10V/X5R_4	INT_HDMI_TXP2	B50	DDI1_TXP2
22 HDMI_CLK-_C	C449	0.1U/10V/X5R_4	INT_HDMI_TXCN	A53	DDI1_TXN3
22 HDMI_CLK+_C	C448	0.1U/10V/X5R_4	INT_HDMI_TXCP	B53	DDI1_TXP3

C54 DDI1_TXN0, C55 DDI1_TXP0, B56 DDI1_TXN1, C56 DDI1_TXP1, B55 DDI1_TXN2, A55 DDI1_TXP2, A57 DDI1_TXN3, B57 DDI1_TXP3

DDI2_TXN0, DDI2_TXP0, DDI2_TXN1, DDI2_TXP1, DDI2_TXN2, DDI2_TXP2, DDI2_TXN3, DDI2_TXP3

EDP_TXN0	C45	EDP_TXN0	20
EDP_TXP0	B46	EDP_TXP0	20
EDP_TXN1	A47	EDP_TXN1	20
EDP_TXP1	B47	EDP_TXP1	20
EDP_TXN2	C47	EDP_TXN2	T58
EDP_TXP2	C46	EDP_TXP2	T53
EDP_TXN3	A49	EDP_TXN3	T52
EDP_TXP3	B49	EDP_TXP3	T57
EDP_AUXN	A45	EDP_AUXN	20
EDP_AUXP	B45	EDP_AUXP	20
EDP_RCOMP	D20	EDP_COMP	
EDP_DISP_UTIL	A43	DP_UTIL	R393 *0_4 LCD_PWM

+VCCIOA_OUT
EDP_COMP — R116 24.9/F_4

+3.3V_RUN
PCH_GPIO78 — R432 10K_4
PCH_GPIO79 — R142 10K_4
PCH_GPIO80 — R422 10K_4
TOUCH_PANEL_RST# — R420 10K_4
PCH_GPIO53 — R421 10K_4

U26I — HSW_ULT_DDR3L — eDP SIDEBAND — DISPLAY — PCIE — 9 OF 19

20 LCD_PWM	B8	EDP_BKLCTL	
20,21 PANEL_BKEN	A9	EDP_BKLEN	
20 ENVDD	C6	EDP_VDDEN	
27 MPCIE_RST_N	U6	PIRQA/GPIO77	+3V
PCH_GPIO78	P4	PIRQB/GPIO78	+3V
PCH_GPIO79	N4	PIRQC/GPIO79	+3V
PCH_GPIO80	N2	PIRQD/GPIO80	+3V
	AD4	PME	
PCH_GPIO55	U7	GPIO55	+3V
21 TOUCH_PANEL_RST#	L1	GPIO52	+3V
PCH_GPIO54	L3	GPIO54	+3V
PCH_GPIO51	R5	GPIO51	+3V
PCH_GPIO53	L4	GPIO53	+3V

DDPB_CTRLCLK	B9	HDMI_SCL	22
DDPB_CTRLDATA	C9	HDMI_SDA	22
DDPC_CTRLCLK	D9		
DDPC_CTRLDATA	D11		
DDPB_AUXN	C5		
DDPB_AUXP	B6		
DDPC_AUXN	B5		
DDPC_AUXP	A6		
DDPB_HPD	C8		
DDPC_HPD	A8	INT_HDMI_HPD	
EDP_HPD	D6	EDP_HPD	

INT_HDMI_HPD — R383 1K_4 — EDP_HP 20,21
R385 100K_4
1K for LVDS converter

+3.3V_RUN — R376 1M_4 — INT_HDMI_HPD — Q32 2N7002K — HDMI_HPD 22
R372 20K/F_4

Board ID	GPIO51	GPIO54	GPIO55
SDV	1	1	1
SIV	1	1	0
SIT			
SVT			

+3.3V_RUN
PCH_GPIO51 — R141 10K_4, R418 10K_4, R166 *10K_4
PCH_GPIO54 — R140 *10K_4, R419 *10K_4, R167 10K_4
PCH_GPIO55

TO Mfr. Site

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Quanta Computer Inc.

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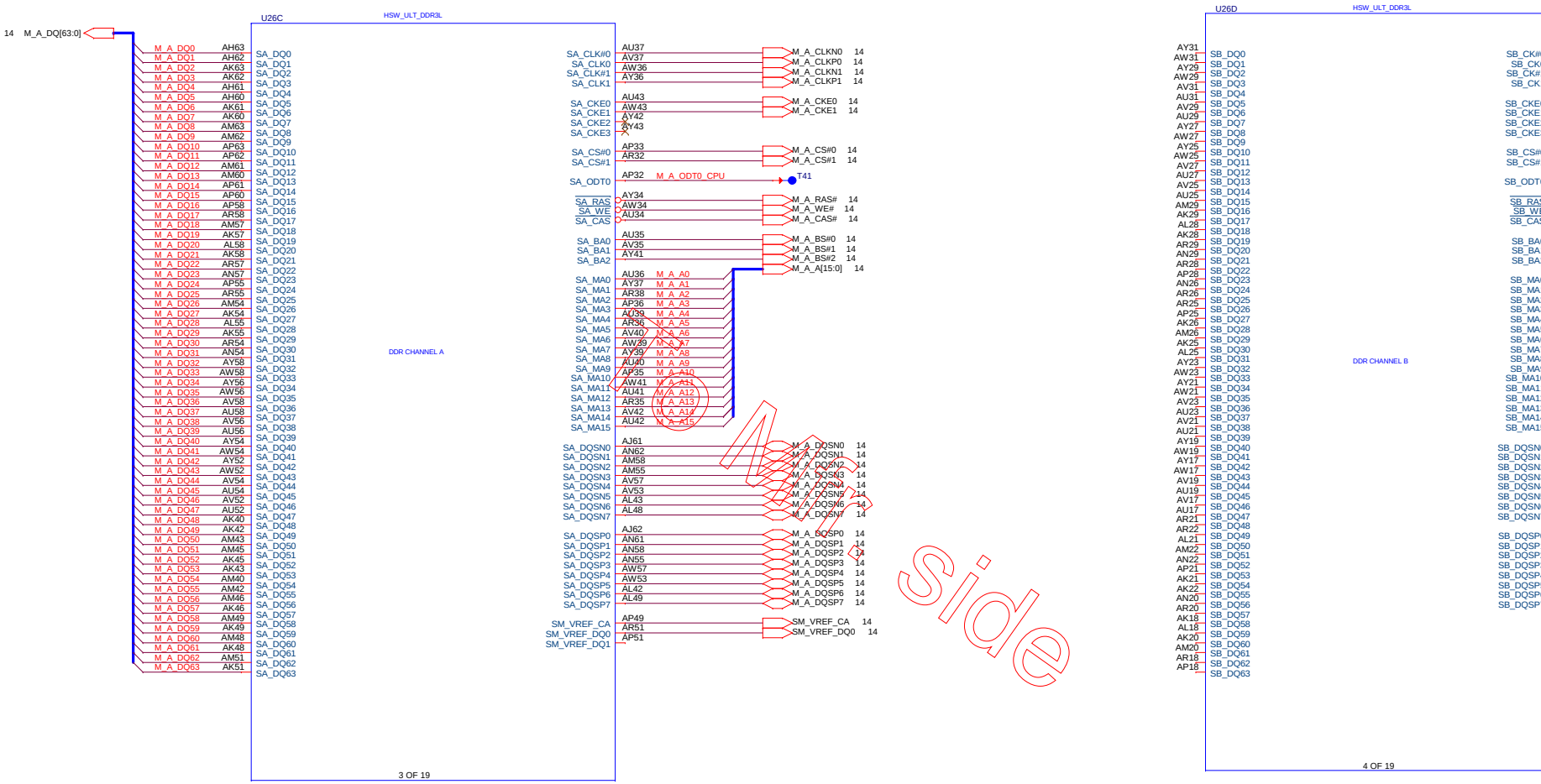
Haswell ULT (DDR3L)



PROJECT : ST6A			
Quanta Computer Inc.			
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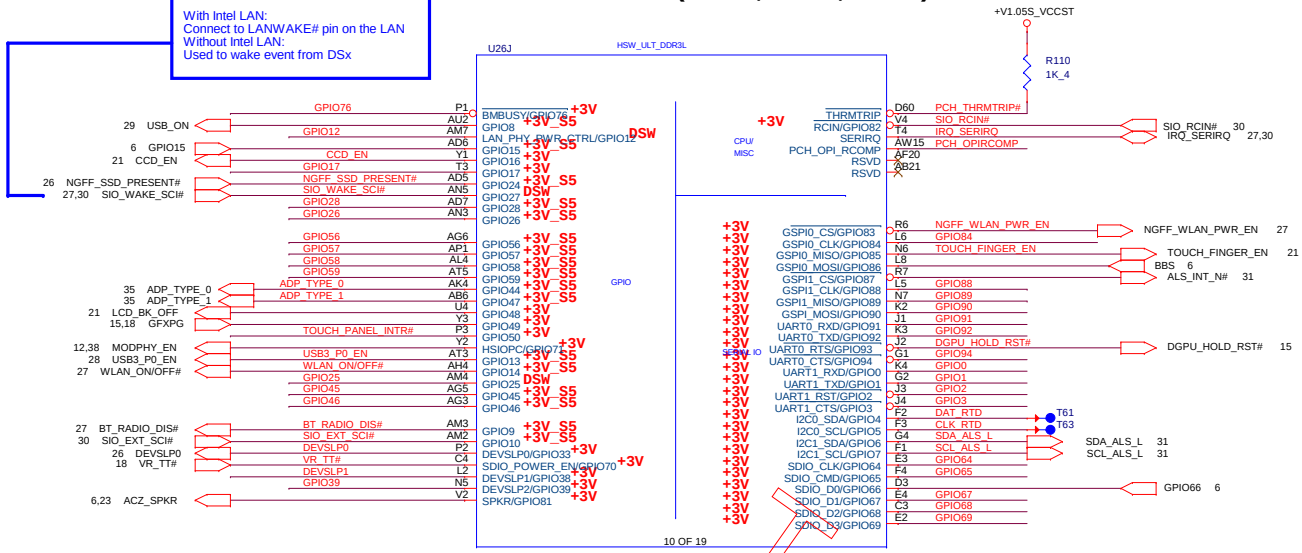
Hasswell ULT(GPIO,LPIO,MISC)

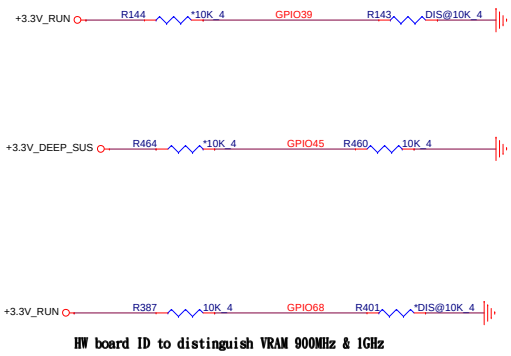
GPIO27
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx



DGPU SELECT	GPIO39
UMA	1
DIS	0

Model ID	GPIO45
S14	0
S15	1

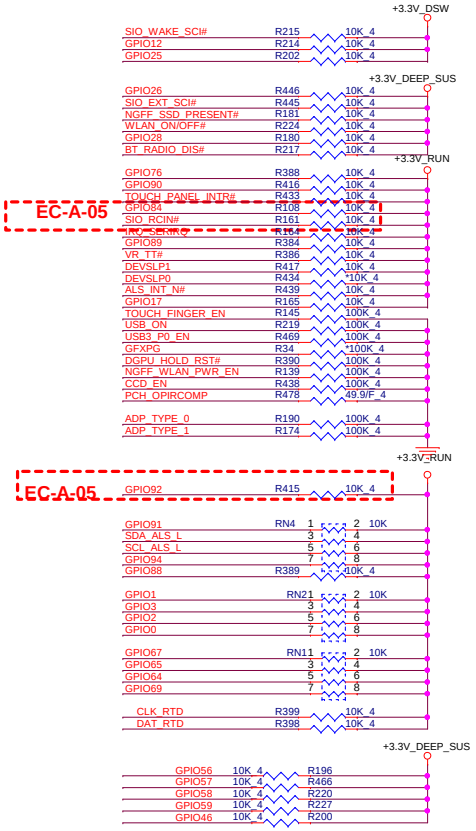
VRAM Freq.	GPIO68
1G	1
900M	0



HW board ID to distinguish VRAM 900MHz & 1GHz

+V1.05S_VCCST 9,13
+3.3V_DEEP_SUS 5,6,7,8,12,14,34
+3.3V_RUN 2,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42
+3.3V_DSW 6,8,12,23,24,27,29,31,35,36,41,44

GPIO Pull-up/Pull-down(CLG)



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SK hynix H5TC4G63AFR-PBA(D/4Gb/29nm) 4Gb x 16 AKD5JGETW00 1000

+3.3V_DEEP_SUS 4,6,7,8,12,14,34
+V1.05S_AUSB3PLL 12

5

Haswell ULT (PCIE,USB)

U26K HSW_ULT_DDR3L

GPU

15 PEG_RXN0 — F10 PERN5_L0
15 PEG_RXP0 — E10 PERP5_L0
15 PEG_TXN0 — C442 0.1U/10V/X5R_4 PEG_TXN0_C — C23 PETN5_L0
15 PEG_TXP0 — C441 0.1U/10V/X5R_4 PEG_TXP0_C — C22 PETP5_L0
15 PEG_RXN1 — F8 PERN5_L1
15 PEG_RXP1 — E8 PERP5_L1
15 PEG_TXN1 — C431 0.1U/10V/X5R_4 PEG_TXN1_C — B23 PETN5_L1
15 PEG_TXP1 — C432 0.1U/10V/X5R_4 PEG_TXP1_C — A23 PETP5_L1
15 PEG_RXN2 — H10 PERN5_L2
15 PEG_RXP2 — G10 PERP5_L2
15 PEG_TXN2 — C434 0.1U/10V/X5R_4 PEG_TXN2_C — B21 PETN5_L2
15 PEG_TXP2 — C433 0.1U/10V/X5R_4 PEG_TXP2_C — C21 PETP5_L2
15 PEG_RXN3 — E6 PERN5_L3
15 PEG_RXP3 — F6 PERP5_L3
15 PEG_TXN3 — C443 0.1U/10V/X5R_4 PEG_TXN3_C — B22 PETN5_L3
15 PEG_TXP3 — C444 0.1U/10V/X5R_4 PEG_TXP3_C — A21 PETP5_L3

WiFi/BT

27 PCIE_RXN3 — G11 PERN3
27 PCIE_RXP3 — F11 PERP3
27 PCIE_TXN3 — C457 0.1U/10V/X5R_4 PCIE_TXN3_C — C29 PETN3
27 PCIE_TXP3 — C456 0.1U/10V/X5R_4 PCIE_TXP3_C — B30 PETP3

PCIE

LAN

24 PCIE_RXN5 — G17 PERN1/USB3RN3
24 PCIE_RXP5 — F17 PERP1/USB3RP3
24 PCIE_TXN5 — C455 0.1U/10V/X5R_4 PCIE_TXN5_C — C30 PETN1/USB3TN3
24 PCIE_TXP5 — C454 0.1U/10V/X5R_4 PCIE_TXP5_C — C31 PETP1/USB3TP3

F13 PERN4
G13 PERP4
B29 PETN4
A29 PETP4
F15 PERN2/USB3RN4
G15 PERP2/USB3RP4
B31 PETN2/USB3TN4
A31 PETP2/USB3TP4

+V1.05S_AUSB3PLL
R112 3K/F_4 PCIE_RCOMP — E15 RSVD
R113 0_4 PCIE_IREF — E13 RSVD
A27 PCIE_RCOMP
B27 PCIE_IREF

USB

USB2N0 — AN8 — USB-_TPanel 21 — Touch Panel
USB2P0 — AM8 — USB+_TPanel 21
USB2N1 — AR7 — USBP1- 28 — USB3.0 Port 1 (CN7)
USB2P1 — AT7 — USBP1+ 28
USB2N2 — AR8 — USBP2- 29 — USB2.0 Port 2
USB2P2 — AP8 — USBP2+ 29
USB2N3 — AR10 — USBP3- 29 — USB2.0 Port 3
USB2P3 — AT10 — USBP3+ 29
USB2N4 — AM15 — USBP4- 21 — CAMERA
USB2P4 — AL15 — USBP4+ 21
USB2N5 — AM13 — USBP5- 27 — WLAN / BT NGFF
USB2P5 — AN13 — USBP5+ 27
USB2N6 — AP11 — USBP6- 29 — Card reader
USB2P6 — AN11 — USBP6+ 29
USB2N7 — AR13
USB2P7 — AP13

EC-A-05

USB3RN1 — G20 — USB30_RX1- 28 — USB3.0 Port 1 (CN7)
USB3RP1 — H20 — USB30_RX1+ 28
USB3TN1 — C33 — USB30_TX1- 28
USB3TP1 — B34 — USB30_TX1+ 28
USB3RN2 — E18
USB3RP2 — F18
USB3TN2 — B33
USB3TP2 — A33

USBRBIAS — AJ10 — USB_BIAS — R185 22.6/F_4
USBRBIAS — AJ11
RSVD — AN10 — USBPLLMON_N — R207 49.9/F_4
RSVD — AM10 — USBPLLMON_P — R210 49.9/F_4

+3V_S5 OC0/GPIO40 — AL3 — USB_OC0# — USB_OC0# 28
+3V_S5 OC1/GPIO41 — AT1 — USB_OC1# — USB_OC1# 29
+3V_S5 OC2/GPIO42 — AH2 — USB_OC2#
+3V_S5 OC3/GPIO43 — AV3 — USB_OC3#

+3.3V_DEEP_SUS
USB_OC3# 4 3
USB_OC1# 2 1
RP8 10K
USB_OC2# 4 3
USB_OC0# 2 1
RP4 10K

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	Haswell ULT 4/12	1A
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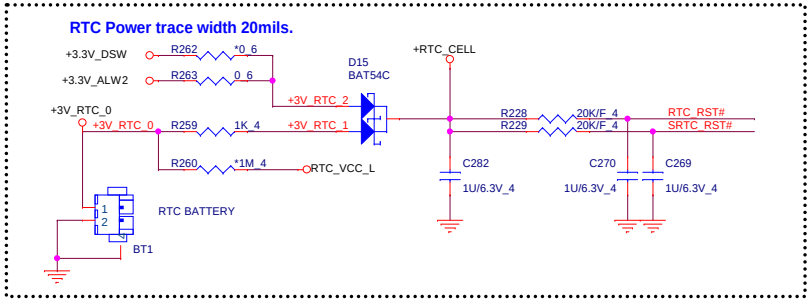
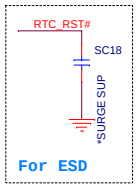
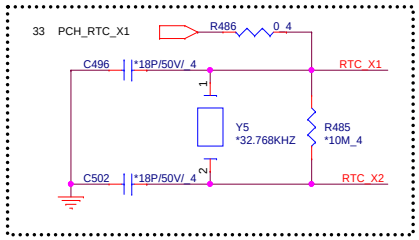
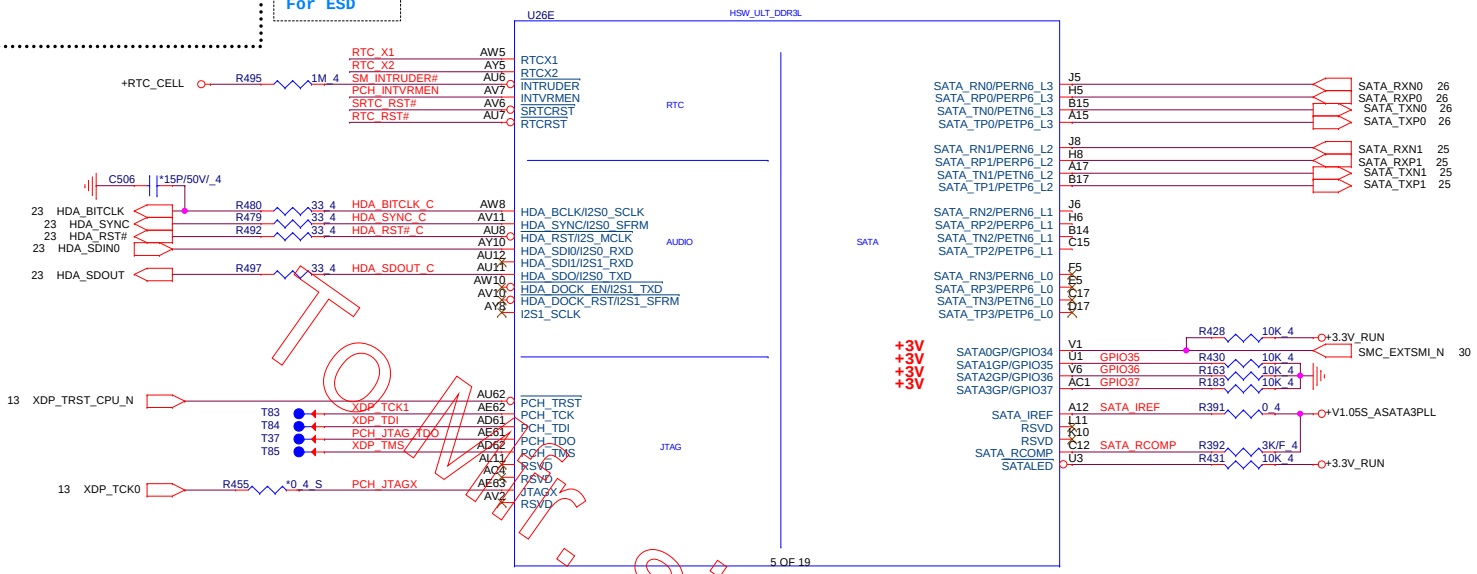
Haswell ULT (RTC, HDA, JTAG, SATA)







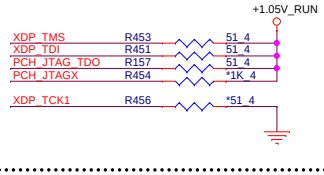


PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3.3V_RUN — R429 *1K_4 — ACZ_SPKR 4,23
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	30 ME_WR# — R491 1K_4 — HDA_SDOUT_C
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	**Should be always pull-up**	+RTC_CELL — R493 330K_4 — PCH_INTVRMEN — R481 *330K_4
GPIO66	Top-Block Swap override		**0 = Default disable (iPD 20K)** 1 = Enable TBS function	+V3.3S_1.8S_LPSS_SDIO — R394 *1K_4 — GPIO66 4 — R404 *1K_4
GPIO86	BBS(Boot BIOS Strap Bit)		**0 = Default SPI (iPD 20K)** 1 =LPC	+3.3V_RUN — R106 *1K_4 — BBS 4 — R105 *1K_4
GPIO15	TLS(Transport layer security)		**0 = Default enable w/o confidentiality(iPD 20K)** 1 =Default enable with confidentiality	+3.3V_DEEP_SUS — R182 *10K_4 — GPIO15 4
DSWVREN	Deep Sx well on die DSW VR enable		**1=Should be always pull-up**	+RTC_CELL — R483 330K_4 — DSWVRMEN 8

PCH JTAG Debug (CLG)

MP remove(Intel)



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Quanta Computer Inc.			
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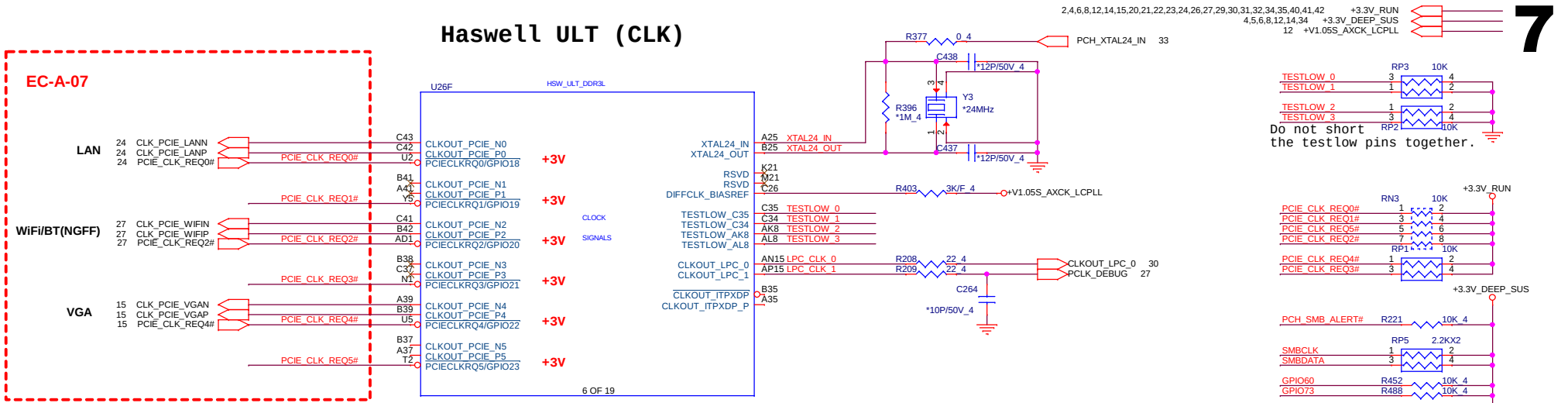
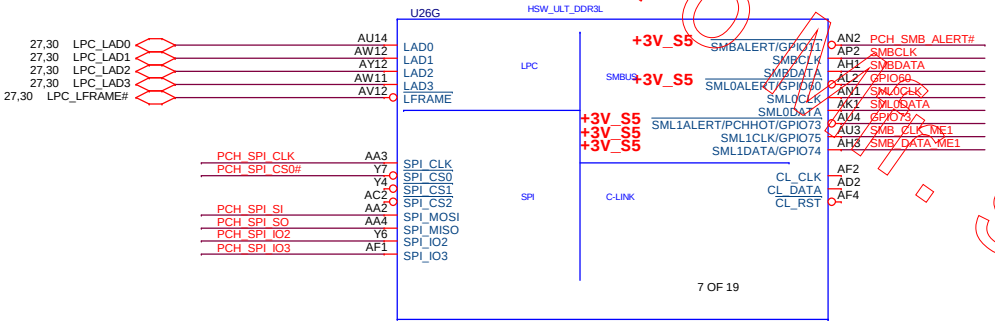
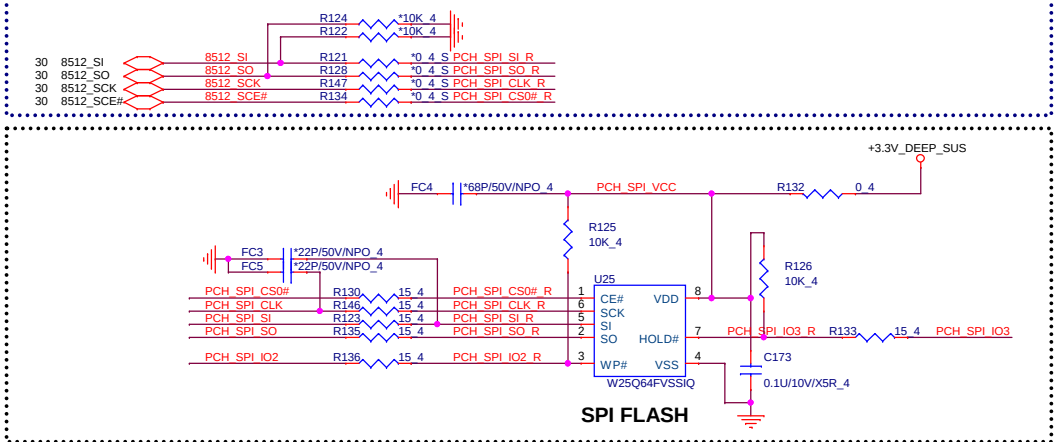
Haswell ULT (CLK)



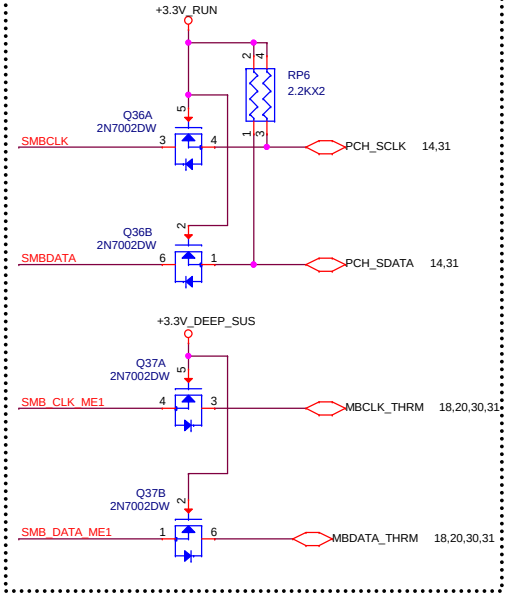
Haswell ULT (LPC/SPI/SMB/CLINK)



For EC(IT8587 e-flash) load code from BIOS flash ROM



SMBus/Pull-up(CLG)



PROJECT : ST6A

Quanta Computer Inc.

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	Haswell ULT 6/12	1A
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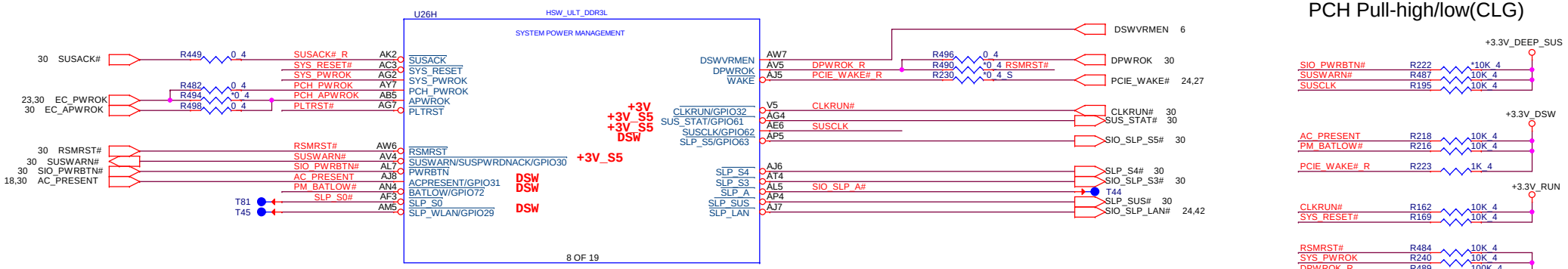
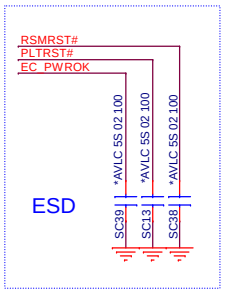
Haswell ULT (SYSTEM POWER MANAGEMENT)

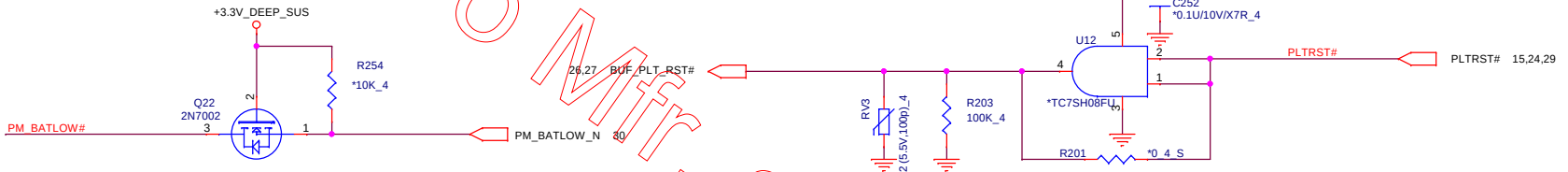
8

4,6,12,23,24,27,29,31,35,36,41,44 +3.3V_DSW
2,4,6,7,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN
4,5,6,7,12,14,34 +3.3V_DEEP_SUS

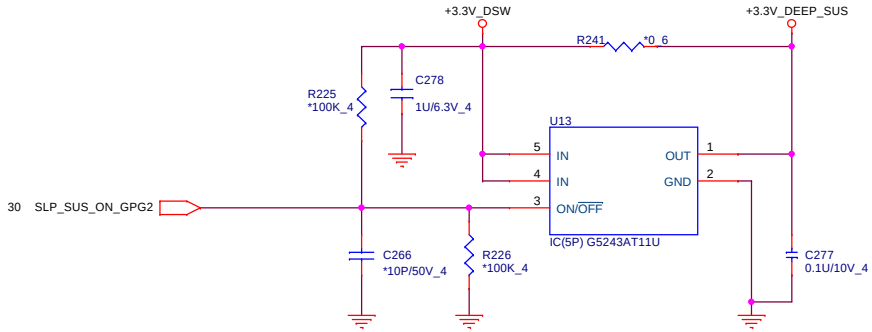


PCH Pull-high/low(CLG)

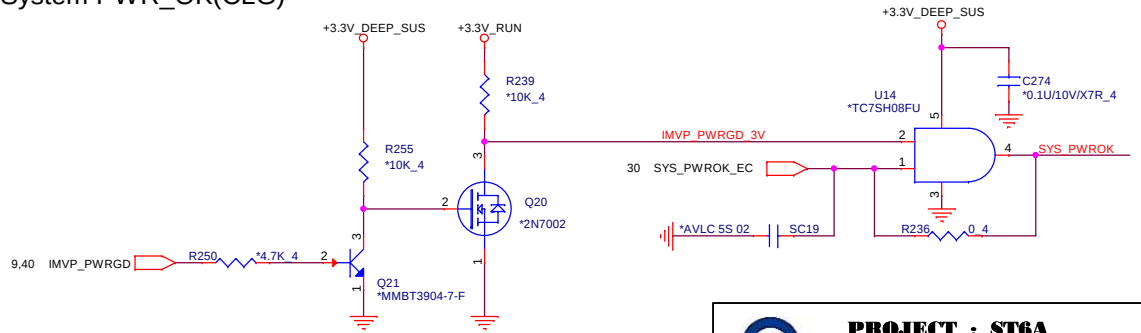




For DS3



System PWR_OK(CLG)



PROJECT : ST6A
Quanta Computer Inc.

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Haswell ULT MCP(POWER)

34,40 +VCCIN
14,37,42 +V_VDDQ_VR
13 +VCCIO_OUT
2 +VCCIOA_OUT
4,13 +V1.05S_VCCST
6,12,33,34,38,40,42,44 +1.05V_RUN

CPU VDDQ

Haswell ULT 15W : 1.4A

7X10UF MLCC
4X2.2UF MLCC

+V_VDDQ_VR

C232 10U/6.3V/X5R_6
C231 10U/6.3V/X5R_6
C230 10U/6.3V/X5R_6
C229 10U/6.3V/X5R_6
C504 10U/6.3V/X5R_6
C503 10U/6.3V/X5R_6
C505 10U/6.3V/X5R_6

C498 2.2U/6.3V/X5R_4
C497 2.2U/6.3V/X5R_4
C499 2.2U/6.3V/X5R_4
C500 2.2U/6.3V/X5R_4

+V1.05S_VCCST

R395 10K_4

VCCST_PWRGD_L

30 VCCST_PWRGD#

Q35 2N7002K

+VCCIOA_OUT

+VCCIO_OUT

C440 *0.1U/10V/X5R_4

40 H_VR_ENABLE_MCP

8,40 IMVP_PWRGD

R111 10K_4

+V1.05S_VCCST

R114 150_6

+1.05V_RUN

R179 0_0805

+V1.05S_VCCST

+VCCIN

+V_VDDQ_VR

+VCCIN

CPU VCC

Haswell ULT 15W : 32A

23 X 22UF

+VCCIN

C225 22U/6.3V/X5R_6
C236 22U/6.3V/X5R_6
C220 22U/6.3V/X5R_6
C208 22U/6.3V/X5R_6
C200 22U/6.3V/X5R_6
C195 22U/6.3V/X5R_6
C177 22U/6.3V/X5R_6
C214 22U/6.3V/X5R_6
C178 22U/6.3V/X5R_6
C184 22U/6.3V/X5R_6
C182 22U/6.3V/X5R_6
C181 22U/6.3V/X5R_6
C180 22U/6.3V/X5R_6
C179 22U/6.3V/X5R_6
C187 22U/6.3V/X5R_6
C188 22U/6.3V/X5R_6
C189 22U/6.3V/X5R_6
C183 22U/6.3V/X5R_6
C218 22U/6.3V/X5R_6
C217 22U/6.3V/X5R_6
C197 22U/6.3V/X5R_6
C213 22U/6.3V/X5R_6
C191 22U/6.3V/X5R_6
C210 22U/6.3V/X5R_6
C242 22U/6.3V/X5R_6
C190 22U/6.3V/X5R_6
C186 22U/6.3V/X5R_6
C185 22U/6.3V/X5R_6
C219 22U/6.3V/X5R_6
C211 22U/6.3V/X5R_6

C194 1 2 100P/50VNPO_4
C196 1 2 100P/50VNPO_4
C212 1 2 100P/50VNPO_4
C204 1 2 100P/50VNPO_4

U26L HSW_ULT_DDR3L

T20 MCP_RSVD_61 L59
T12 MCP_RSVD_62 J58
T22 MCP_RSVD_63 N58
T35 MCP_RSVD_64 AC58
T39 MCP_RSVD_68 AE59
H_CPU_SVIDALRT_N L62
VR_SVID_CLK N63
VR_SVID_DATA L63
F59
E63
D63
H59
P62
T70 MCP_RSVD_69 P60
T26 MCP_RSVD_70 P61
T23 MCP_RSVD_71 N60
T25 MCP_RSVD_72 N61
T27 MCP_RSVD_73 T59
T36 MCP_RSVD_74 AD60
T38 MCP_RSVD_75 AD59
T33 MCP_RSVD_76 AA59
T82 MCP_RSVD_77 AE60
T34 MCP_RSVD_78 AC59
T40 MCP_RSVD_79 AG58
T29 MCP_RSVD_80 U59
T32 MCP_RSVD_81 V59

AH26 AJ31 AJ33 AJ37 AN33 AP43 AR48 AY35 AY40 AY44 AY50 — VDDQ
F59 — VCC
N58 AC58 — RSVD
E63 — VCC_SENSE
AB23 A59 — RSVD
E20 — VCCIO_OUT
AD23 — VCCIOA_OUT
AA23 AE59 — RSVD
L62 — VIDALERT
N63 — VIDSCLK
L63 — VIDSOUT
B59 — VCCST_PWRGD
F60 — VR_EN
C59 — VR_READY
D63 — VSS
H59 — PWR_DEBUG
P62 — VSS
P60 P61 N60 N61 — RSVD_TP
T59 AD60 AD59 AA59 AE60 AC59 AG58 U59 V59 — RSVD
AC22 — VCCST
AE22 AE23 — VCCST
AB57 — VCC
AD57 AG57 C24 C28 C32 — VCC

HSW ULT POWER

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C36 C40 C44 C48 C52 C56 E23 E25 E27 E29 E31 E33 E35 E37 E39 E41 E43 E45 E47 E49 E51 E53 E55 E57 F24 F28 F32 F36 F40 F44 F48 F52 F56 G23 G25 G27 G29 G31 G33 G35 G37 G39 G41 G43 G45 G47 G49 G51 G53 G55 G57 H23 J23 K23 K57 L22 M23 M57 P57 U57 W57 — VCC

Mfr. Side

+V1.05S_VCCST

SVID ALERT

close to CPU

+V1.05S_VCCST

R500 75_4

H_CPU_SVIDALRT_N

R425 43_4

VR_SVID_ALERT# 40

SVID DATA

close to CPU

+V1.05S_VCCST

R424 130_4

VR_SVID_DATA

close to VR

+V1.05S_VCCST

R499 130_4

VR_SVID_DATA 40

+VCCIN

R405 100/F_4

40 VCCSENSE

VCCSENSE

SVID CLK

close to VR

+V1.05S_VCCST

R501 54.9_4

VR_SVID_CLK

VR_SVID_CLK 40

C463 0.1U/10V_4

+V1.05S_VCCST

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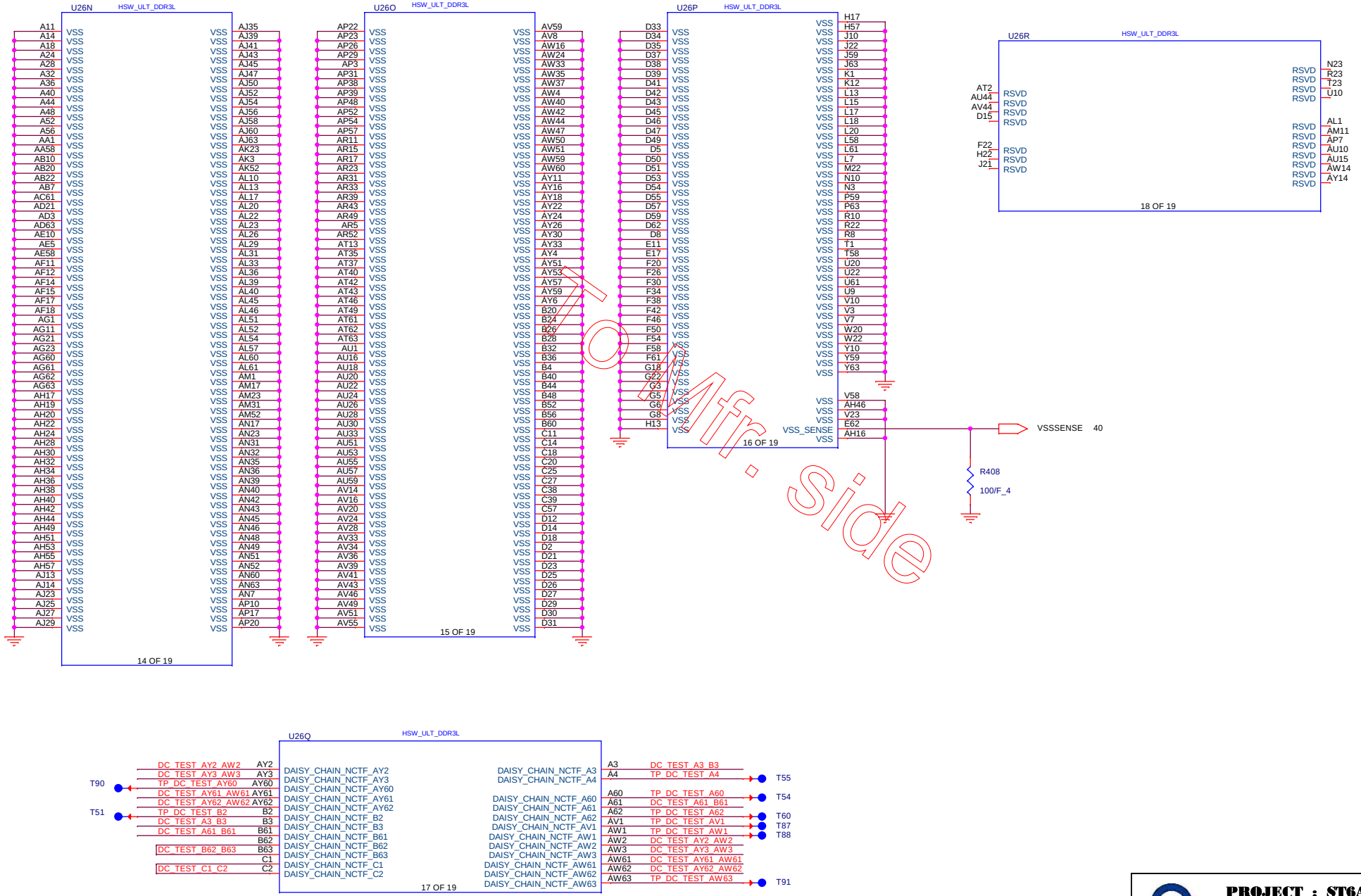
Haswell ULT (GND)



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Quanta Computer Inc.

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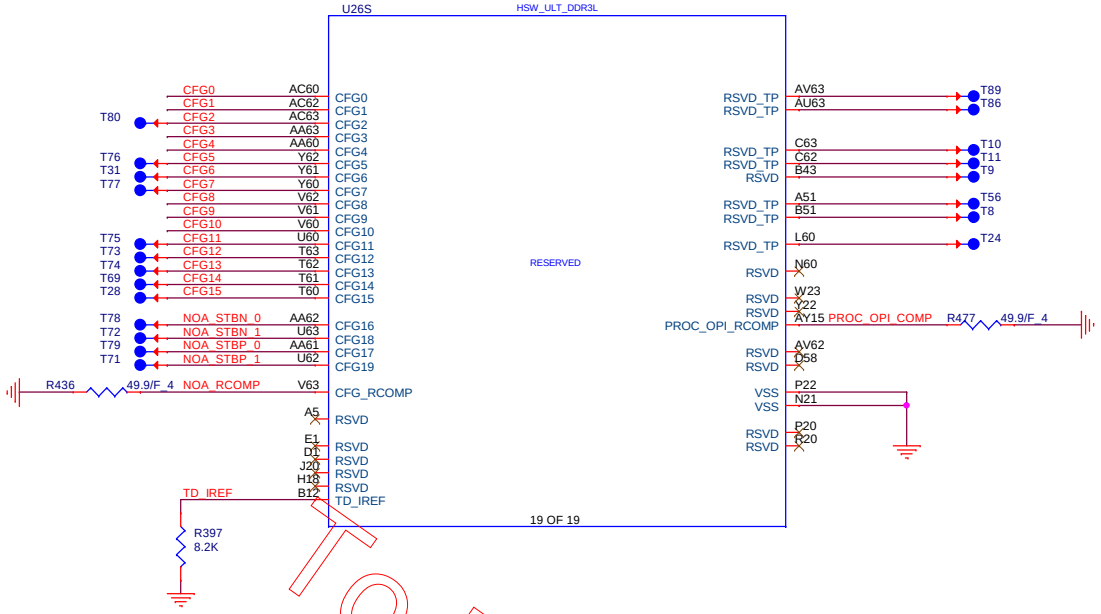
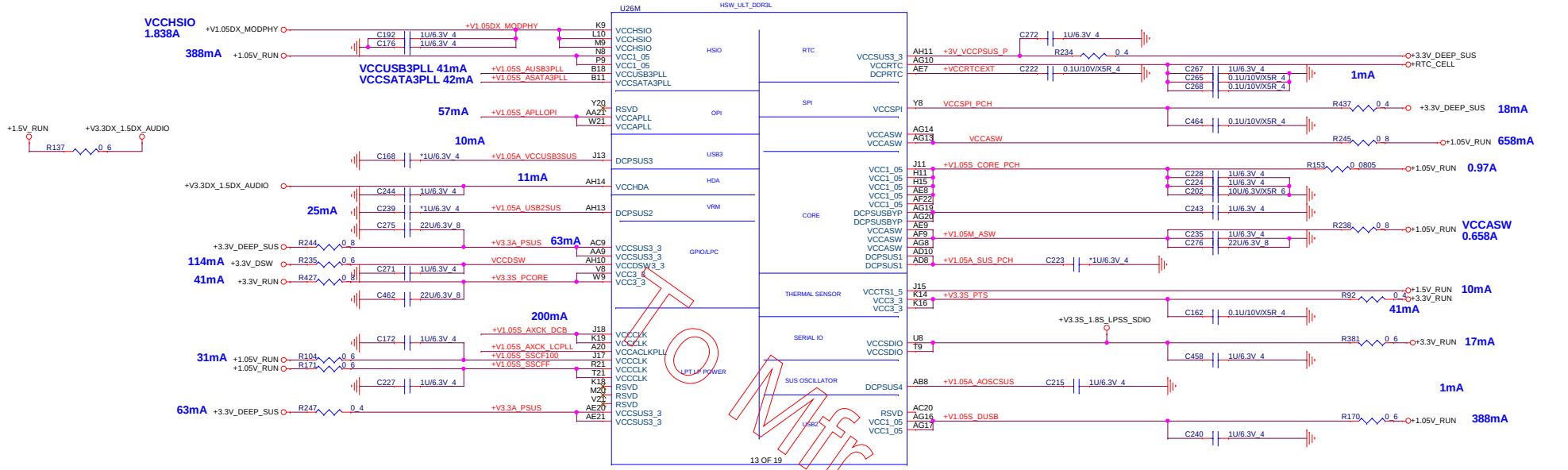


Processor Strapping

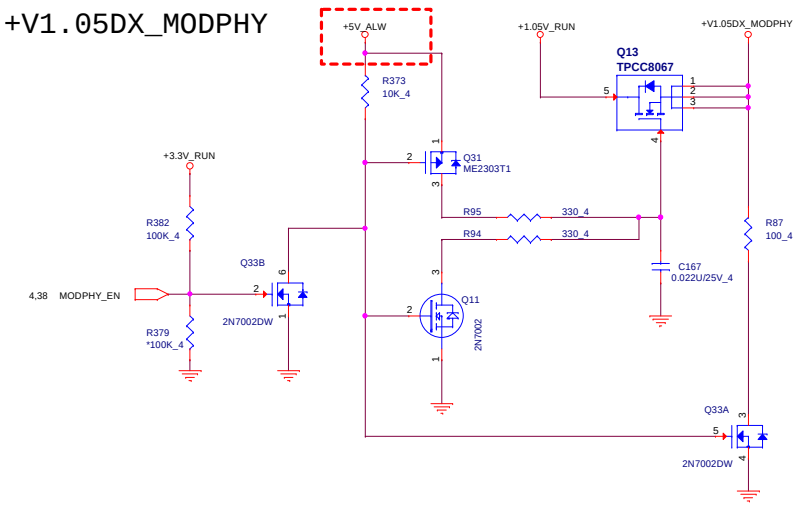
	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R178 *1K_4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R442 *1K_4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	CFG3 R441 *1K_4
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG4 R155 1K_4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R440 *1K_4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R435 *1K_4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R151 *1K_4

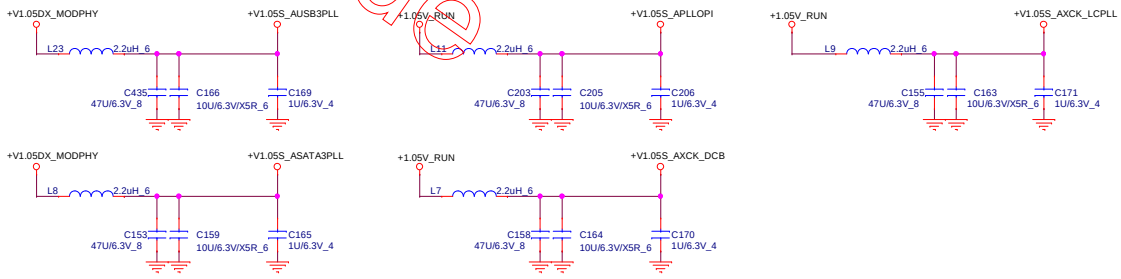
Haswell ULT PCH(POWER)



+V1.05DX_MODPHY

EC-A-14





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4,9 +V1.05S_VCCST
9 +VCCIO_OUT

U26B HSW_ULT_DDR3L

30 PECI_EC_R
+VCCIO_OUT R410 *62_4
30,35,40 IMVP7_PROCHOT# R423 56_4 H_PROCHOT# K63
+V1.05S_VCCST R411 62_4
R400 10K_4 H_CPUPWRGD C61
SC31 *AVLC 5S 02 100
For ESD
R212 200_4 SM_RCOMP_0 AU60
R213 120_4 SM_RCOMP_1 AV60
R211 100_4 SM_RCOMP_2 AU61
14 SM_DRAMRST# SM_DRAMRST# AV15
14 DDR_PG_CTRL DDR_PG_CTRL AV61

T59 PROC_DETECT# D61
T18 CATERR# K61
N62

PROC_DETECT
CATERR
PECI
MISC
PROCHOT
THERMAL
PROCPWRGD
PWR
SM_RCOMP0
SM_RCOMP1
SM_RCOMP2
SM_DRAMRST
SM_PG_CNTL1
DDR3L
DSW
JTAG
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For ESD
SC36 *AVLC 5S 02 100

PRDY J62 XDP_PRDY_N T15
PREQ K62 XDP_PREQ_N T21
PROC_TCK E60
PROC_TMS E61 XDP_TMS_CPU T62 XDP_TCK0 6
PROC_TRST E59 XDP_TRST_CPU_N 6
PROC_TDI F63 XDP_TDI_CPU T64
PROC_TDO F62 XDP_TDO_CPU T65

BPM#0 J60 XDP_BPM0_R T16
BPM#1 H60 XDP_BPM1_R T14
BPM#2 H61 XDP_BPM2_R T66
BPM#3 H62 XDP_BPM3_R T67
BPM#4 K59 XDP_BPM4_R T17
BPM#5 H63 XDP_BPM5_R T68
BPM#6 K60 XDP_BPM6_R T19
BPM#7 J61 XDP_BPM7_R T13

XDP_PREQ_N
SC11
*SURGE SUP
For ESD

SM_DRAMRST#
SC17
*SURGE SUP
For ESD

+V1.05S_VCCST
XDP_TDO_CPU R409 51/F_4
XDP_TDI_CPU R407 *51/F_4
XDP_TMS_CPU R406 *51/F_4
XDP_TCK0 R138 51/F_4
XDP_TRST_CPU_N R467 *51/F_4

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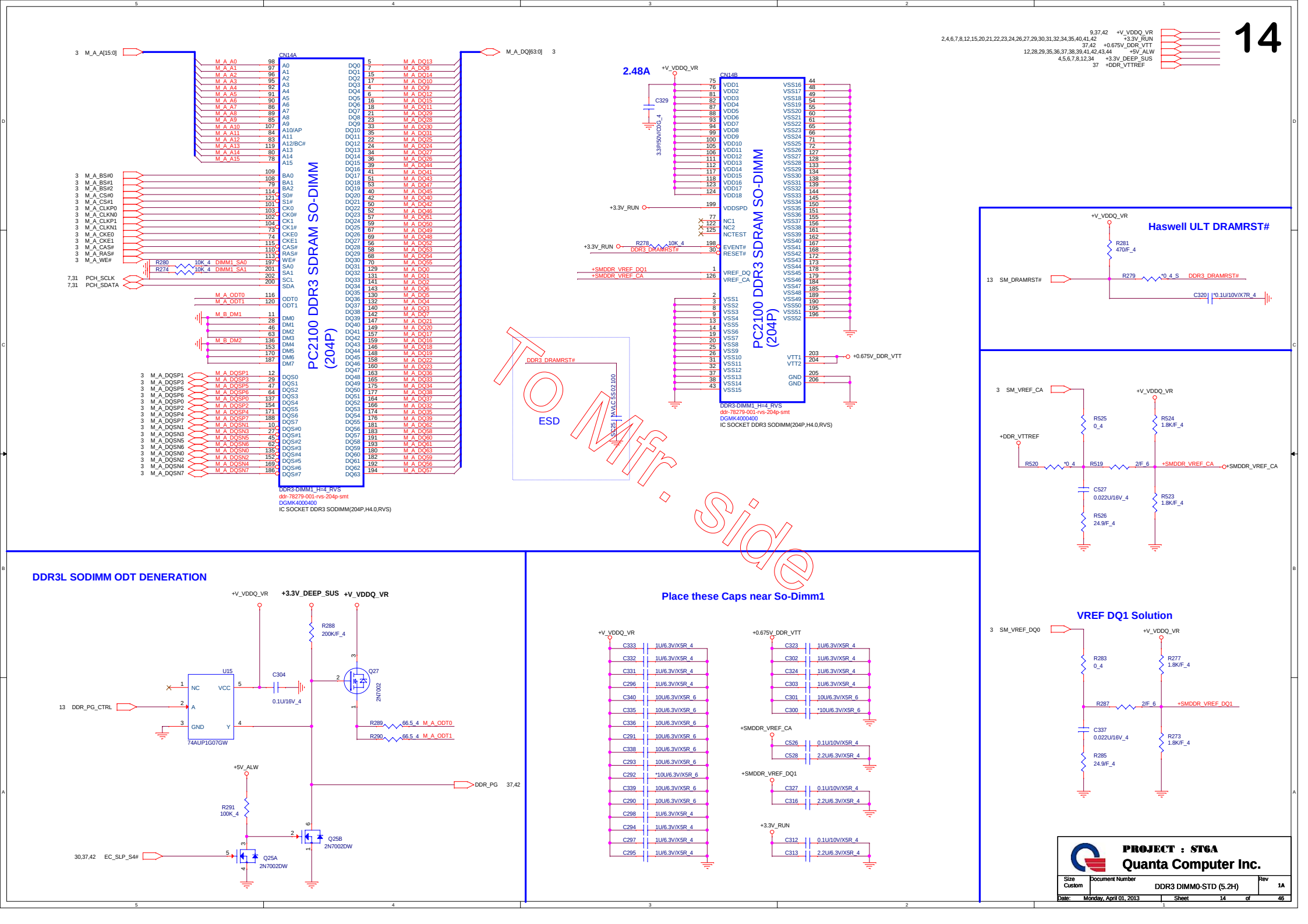
CN14A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=4_RVS
ddr-78279-001-rvs-204p-smt
DGMK4000400
IC SOCKET DDR3 SODIMM(204P,H4.0,RVS)
CN14B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM1_H=4_RVS
ddr-78279-001-rvs-204p-smt
DGMK4000400
IC SOCKET DDR3 SODIMM(204P,H4.0,RVS)
2.48A
ESD
To Mfr. Side
DDR3L SODIMM ODT DENERATION
74AUP1G07GW
Place these Caps near So-Dimm1
Haswell ULT DRAMRST#
VREF DQ1 Solution
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DDR3 DIMM0-STD (5.2H)
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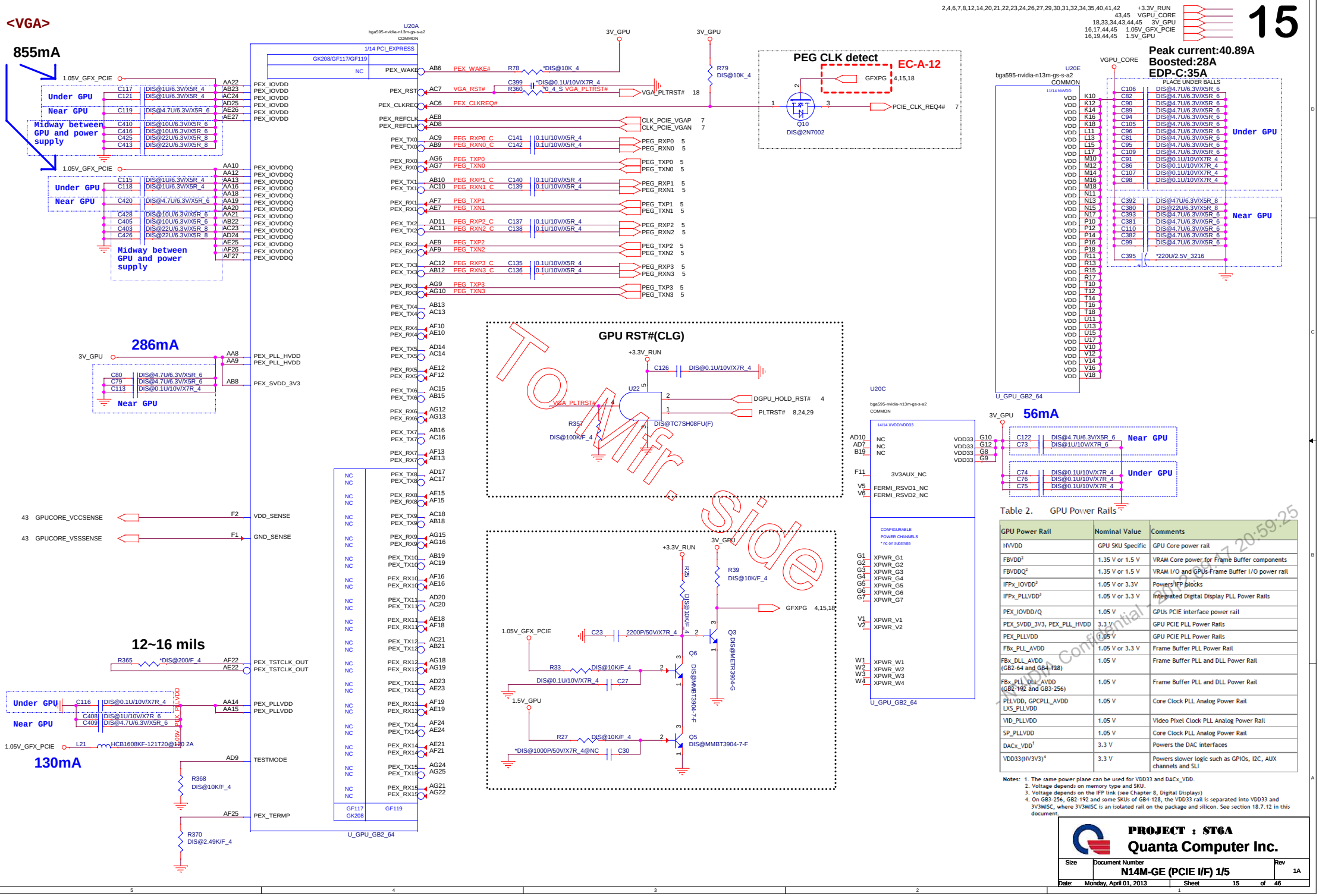
<VGA>
855mA
Under GPU
Near GPU
Midway between GPU and power supply
286mA
130mA
12~16 mils
56mA
PEG CLK detect
EC-A-12
GPU RST#(CLG)
To Wifi Side
Peak current:40.89A
Boosted:28A
EDP-C:35A
U20A
U20E
U20C
U_GPU_GB2_64
Table 2. GPU Power Rails
GPU Power Rail | Nominal Value | Comments
NVVDD | GPU SKU Specific | GPU Core power rail
FBVDD | 1.35 V or 1.5 V | VRAM Core power for Frame Buffer components
FBVDDQ | 1.35 V or 1.5 V | VRAM I/O and GPUs Frame Buffer I/O power rail
IFPx_IOVDD | 1.05 V or 3.3V | Powers IFP blocks
IFPx_PLLVDD | 1.05 V or 3.3 V | Integrated Digital Display PLL Power Rails
PEX_IOVDD/Q | 1.05 V | GPUs PCIE interface power rail
PEX_SVDD_3V3, PEX_PLL_HVDD | 3.3 V | GPU PCIE PLL Power Rails
PEX_PLLVDD | 1.05 V | GPU PCIE PLL Power Rails
FBx_PLL_AVDD | 1.05 V or 3.3 V | Frame Buffer PLL Power Rail
FBx_DLL_AVDD (GB2-64 and GB4-128) | 1.05 V | Frame Buffer PLL and DLL Power Rail
FBx_PLL_DLL_AVDD (GB2-192 and GB3-256) | 1.05 V | Frame Buffer PLL and DLL Power Rail
PLLVDD, GPCPLL_AVDD LXS_PLLVDD | 1.05 V | Core Clock PLL Analog Power Rail
VID_PLLVDD | 1.05 V | Video Pixel Clock PLL Analog Power Rail
SP_PLLVDD | 1.05 V | Core Clock PLL Analog Power Rail
DACx_VDD | 3.3 V | Powers the DAC interfaces
VDD33(NV3V3) | 3.3 V | Powers slower logic such as GPIOs, I2C, AUX channels and SLI
Notes: 1. The same power plane can be used for VDD33 and DACx_VDD.
2. Voltage depends on memory type and SKU.
3. Voltage depends on the IFP link (see Chapter 8, Digital Displays)
4. On GB3-256, GB2-192 and some SKUs of GB4-128, the VDD33 rail is separated into VDD33 and 3V3MISC, where 3V3MISC is an isolated rail on the package and silicon. See section 18.7.12 in this document.
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1A
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<VGA>

19 VMA_DQ[63..0] → VMA_DQ[63..0]
19 VMA_DM[7..0] → VMA_DM[7..0]
19 VMA_WDQS[7..0] → VMA_WDQS[7..0]
19 VMA_RDQS[7..0] → VMA_RDQS[7..0]

15,17,44,45 1.05V_GFX_PCIE
15,19,44,45 1.5V_GPU

U20B
bga595-nvidia-n13m-gs-s-a2
COMMON
2/14 FBA

F3 FB_CLAMP | NC
R351 GF117/GK208 | GF119
DIS@10K/F_4

FBA_D0	E18	VMA_DQ0
FBA_D1	F18	VMA_DQ1
FBA_D2	E16	VMA_DQ2
FBA_D3	F17	VMA_DQ3
FBA_D4	D20	VMA_DQ4
FBA_D5	D21	VMA_DQ5
FBA_D6	F20	VMA_DQ6
FBA_D7	E21	VMA_DQ7
FBA_D8	E15	VMA_DQ8
FBA_D9	D15	VMA_DQ9
FBA_D10	F15	VMA_DQ10
FBA_D11	F13	VMA_DQ11
FBA_D12	C13	VMA_DQ12
FBA_D13	B13	VMA_DQ13
FBA_D14	E13	VMA_DQ14
FBA_D15	D13	VMA_DQ15
FBA_D16	B15	VMA_DQ16
FBA_D17	C16	VMA_DQ17
FBA_D18	A13	VMA_DQ18
FBA_D19	A15	VMA_DQ19
FBA_D20	B18	VMA_DQ20
FBA_D21	A18	VMA_DQ21
FBA_D22	A19	VMA_DQ22
FBA_D23	C19	VMA_DQ23
FBA_D24	B24	VMA_DQ24
FBA_D25	C23	VMA_DQ25
FBA_D26	A25	VMA_DQ26
FBA_D27	A24	VMA_DQ27
FBA_D28	A21	VMA_DQ28
FBA_D29	B21	VMA_DQ29
FBA_D30	C20	VMA_DQ30
FBA_D31	C21	VMA_DQ31
FBA_D32	R22	VMA_DQ32
FBA_D33	R24	VMA_DQ33
FBA_D34	T22	VMA_DQ34
FBA_D35	R23	VMA_DQ35
FBA_D36	N25	VMA_DQ36
FBA_D37	N26	VMA_DQ37
FBA_D38	N23	VMA_DQ38
FBA_D39	N24	VMA_DQ39
FBA_D40	V23	VMA_DQ40
FBA_D41	V22	VMA_DQ41
FBA_D42	T23	VMA_DQ42
FBA_D43	U22	VMA_DQ43
FBA_D44	Y24	VMA_DQ44
FBA_D45	AA24	VMA_DQ45
FBA_D46	Y22	VMA_DQ46
FBA_D47	AA23	VMA_DQ47
FBA_D48	AD27	VMA_DQ48
FBA_D49	AB25	VMA_DQ49
FBA_D50	AD26	VMA_DQ50
FBA_D51	AC25	VMA_DQ51
FBA_D52	AA27	VMA_DQ52
FBA_D53	AA26	VMA_DQ53
FBA_D54	W26	VMA_DQ54
FBA_D55	Y25	VMA_DQ55
FBA_D56	R26	VMA_DQ56
FBA_D57	T25	VMA_DQ57
FBA_D58	N27	VMA_DQ58
FBA_D59	R27	VMA_DQ59
FBA_D60	V26	VMA_DQ60
FBA_D61	V27	VMA_DQ61
FBA_D62	W27	VMA_DQ62
FBA_D63	W25	VMA_DQ63

FBA_DQM0	D19	VMA_DM0
FBA_DQM1	D14	VMA_DM1
FBA_DQM2	C17	VMA_DM2
FBA_DQM3	C22	VMA_DM3
FBA_DQM4	P24	VMA_DM4
FBA_DQM5	W24	VMA_DM5
FBA_DQM6	AA25	VMA_DM6
FBA_DQM7	U25	VMA_DM7

FBA_DQS_WP0	E19	VMA_WDQS0
FBA_DQS_WP1	C15	VMA_WDQS1
FBA_DQS_WP2	B16	VMA_WDQS2
FBA_DQS_WP3	B22	VMA_WDQS3
FBA_DQS_WP4	R25	VMA_WDQS4
FBA_DQS_WP5	W23	VMA_WDQS5
FBA_DQS_WP6	AB26	VMA_WDQS6
FBA_DQS_WP7	T26	VMA_WDQS7

FBA_DQS_RN0	F19	VMA_RDQS0
FBA_DQS_RN1	C14	VMA_RDQS1
FBA_DQS_RN2	A16	VMA_RDQS2
FBA_DQS_RN3	A22	VMA_RDQS3
FBA_DQS_RN4	P25	VMA_RDQS4
FBA_DQS_RN5	W22	VMA_RDQS5
FBA_DQS_RN6	AB27	VMA_RDQS6
FBA_DQS_RN7	T27	VMA_RDQS7

19 FBA_CMD0	C27	FBA_CMD0
	C26	FBA_CMD1
19 FBA_CMD2	E24	FBA_CMD2
19 FBA_CMD3	F24	FBA_CMD3
19 FBA_CMD4	D27	FBA_CMD4
19 FBA_CMD5	D26	FBA_CMD5
19 FBA_CMD6	F25	FBA_CMD6
19 FBA_CMD7	F26	FBA_CMD7
19 FBA_CMD8	F23	FBA_CMD8
19 FBA_CMD9	G22	FBA_CMD9
19 FBA_CMD10	G23	FBA_CMD10
19 FBA_CMD11	G24	FBA_CMD11
19 FBA_CMD12	F27	FBA_CMD12
19 FBA_CMD13	G25	FBA_CMD13
19 FBA_CMD14	G27	FBA_CMD14
19 FBA_CMD15	G26	FBA_CMD15
19 FBA_CMD16	M24	FBA_CMD16
	M23	FBA_CMD17
19 FBA_CMD18	K24	FBA_CMD18
19 FBA_CMD19	K23	FBA_CMD19
19 FBA_CMD20	M27	FBA_CMD20
19 FBA_CMD21	M26	FBA_CMD21
19 FBA_CMD22	M25	FBA_CMD22
19 FBA_CMD23	K26	FBA_CMD23
19 FBA_CMD24	K22	FBA_CMD24
19 FBA_CMD25	J23	FBA_CMD25
19 FBA_CMD26	J25	FBA_CMD26
19 FBA_CMD27	J24	FBA_CMD27
19 FBA_CMD28	K27	FBA_CMD28
19 FBA_CMD29	K25	FBA_CMD29
19 FBA_CMD30	J27	FBA_CMD30
	J26	FBA_CMD31

For debug only 10mA

1.5V_GPU R48 *DIS@60.4/F_4 FBA_DEBUG0 F22 FBA_DEBUG0
R50 *DIS@60.4/F_4 FBA_DEBUG1 J22 FBA_DEBUG1

19 VMA_CLK0	D24	FBA_CLK0
19 VMA_CLK0#	D25	FBA_CLK0
19 VMA_CLK1	N22	FBA_CLK1
19 VMA_CLK1#	M22	FBA_CLK1

	D18	FBA_WCK01
	C18	FBA_WCK01
	D17	FBA_WCK23
	D16	FBA_WCK23
	T24	FBA_WCK45
	U24	FBA_WCK45
	V24	FBA_WCK67
	V25	FBA_WCK67

1.05V_GFX_PCIE 30ohm/100MHz ESR=0.01ohm
Near GPU 15mils width
L22 DIS@HCB1608KF-300T10_1A_6 +FB_PLLAVDD F16 FB_PLLAVDD
P22 FB_PLLAVDD
H22

FB_DLLAVDD | FB_PLLAVDD
GF119/GK208 | GF117

70mA

Under GPU
C71 DIS@0.1U/10V/X7R_4
C415 DIS@0.1U/10V/X7R_4
C67 DIS@0.1U/10V/X7R_4
Near GPU
C404 DIS@22U/6.3V/X5R_8

FB_VREF_PROBE D23 +FB_VREF1 TP3

U_GPU_GB2_64

2.97A
1.5V_GPU

U20D
bga595-nvidia-n13m-gs-s-a2
COMMON
12/14 FBVDDQ

FBVDDQ	B26	
FBVDDQ	C25	
FBVDDQ	E23	
FBVDDQ	E26	
FBVDDQ	F14	
FBVDDQ	F21	
FBVDDQ	G13	
FBVDDQ	G14	
FBVDDQ	G15	
FBVDDQ	G16	
FBVDDQ	G18	
FBVDDQ	G19	
FBVDDQ	G20	
FBVDDQ	G21	
FBVDDQ	H24	
FBVDDQ	H26	
FBVDDQ	J21	
FBVDDQ	K21	
FBVDDQ	L22	
FBVDDQ	L24	
FBVDDQ	L26	
FBVDDQ	M21	
FBVDDQ	N21	
FBVDDQ	R21	
FBVDDQ	T21	
FBVDDQ	V21	
FBVDDQ	W21	

Under GPU
C100 DIS@0.1U/10V/X7R_4
C93 DIS@0.1U/10V/X7R_4
C68 DIS@4.7U/6.3V/X5R_6
C77 DIS@1U/10V/X7R_6
C114 DIS@1U/10V/X7R_6
C78 DIS@4.7U/6.3V/X5R_6
C394 DIS@10U/6.3V/X5R_6
C390 DIS@22U/6.3V/X5R_8
Near GPU

1.5V_GPU R47 DIS@40.2/F_4 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
R345 DIS@42.2/F_4 FB_CAL_PU_GND C24 FB_CAL_PU_GND
R350 DIS@51.1/F_4 FB_CAL_TERM_GND B25 FB_CALTERM_GND
Near GPU

U_GPU_GB2_64

U20F
bga595-nvidia-n13m-gs-s-a2
COMMON
13/14 GND

M13	GND	A2
M15	GND	AB17
M17	GND	AB20
N10	GND	AB24
N12	GND	AC2
N14	GND	AC22
N16	GND	AC26
N18	GND	AC5
P11	GND	AC8
P13	GND	AD12
P15	GND	AD13
P17	GND	A26
P2	GND	AD15
P23	GND	AD16
P26	GND	AD18
P5	GND	AD19
R10	GND	AD21
R12	GND	AD22
R14	GND	AE11
R16	GND	AE14
R18	GND	AE17
T11	GND	AE20
T13	GND	AB11
T15	GND	AF1
T17	GND	AF11
U10	GND	AF14
U12	GND	AF17
U14	GND	AF20
U16	GND	AF23
U18	GND	AF5
U2	GND	AF8
U23	GND	AG2
U26	GND	AG26
U5	GND	AB14
V11	GND	B1
V13	GND	B11
V15	GND	B14
V17	GND	B17
Y2	GND	B20
Y23	GND	B23
Y26	GND	B27
Y5	GND	B5
	GND	B8
	GND	E11
	GND	E14
	GND	E17
	GND	E2
	GND	E20
	GND	E22
	GND	E25
	GND	E5
	GND	E8
	GND	H2
	GND	H23
	GND	H25
	GND	H5
	GND	K11
	GND	K13
	GND	K15
	GND	K17
	GND	L10
	GND	L12
	GND	L14
	GND	L16
	GND	L18
	GND	L2
	GND	L23
	GND	L25
	GND	L5
AA7	GND	M11
AB7	GND	

U_GPU_GB2_64

FBA_CMD2	R339	DIS@10K/F_4
FBA_CMD3	R335	DIS@10K/F_4
FBA_CMD5	R53	DIS@10K/F_4
FBA_CMD18	R359	DIS@10K/F_4
FBA_CMD19	R356	DIS@10K/F_4

DDR3 Command Bit	Data[31..0]	Data[63..32]	PD 10K
ODTx	FBA_CMD2	FBA_CMD18	Yes
CKEx	FBA_CMD3	FBA_CMD19	Yes
RST	FBA_CMD5	FBA_CMD5	Yes
CS*	FBA_CMD0	FBA_CMD16	No

PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	N14M-GE (MEMORY/GND) 2/5	1A
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<VGA> <HDM> <CRT>

Optimus:
All unstuff , one Cap stuff 10K ohm

Optimus:
All unstuff , one Cap stuff 10K ohm

U20G
bga595-nvidia-n13m-gs-s-a2
COMMON
4/14 IFPAB

IFPAB
U_GPU_GB2_64

U20K
bga595-nvidia-n13m-gs-s-a2
COMMON
3/14 DACA
U_GPU_GB2_64

U20I
bga595-nvidia-n13m-gs-s-a2
COMMON
6/14 IFPD

IFPD
U_GPU_GB2_64

U20H
bga595-nvidia-n13m-gs-s-a2
COMMON
5/14 IFPC

IFPC
U_GPU_GB2_64

U20J
bga595-nvidia-n13m-gs-s-a2
COMMON
7/14 IFPEF

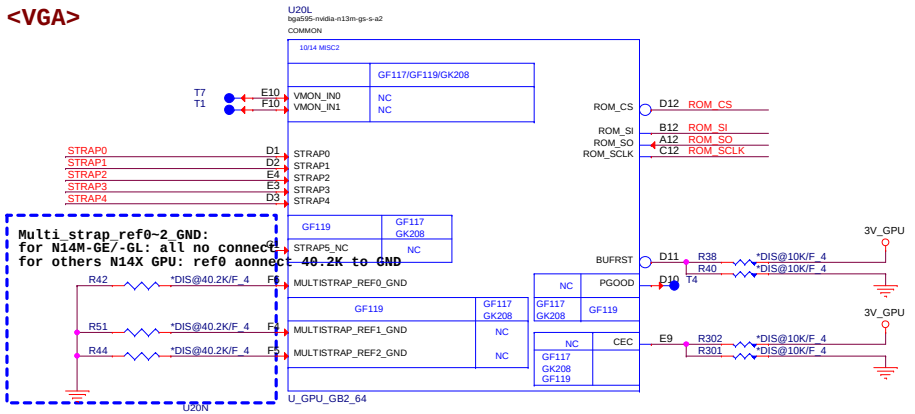
IFPE
IFPF
U_GPU_GB2_64

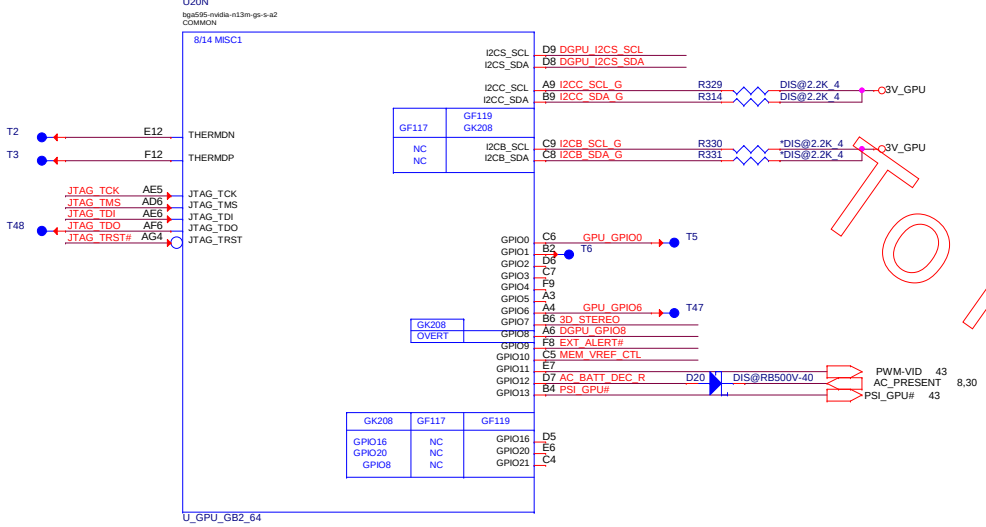
U20M
bga595-nvidia-n13m-gs-s-a2
COMMON
9/14 XTAL_PLL
U_GPU_GB2_64

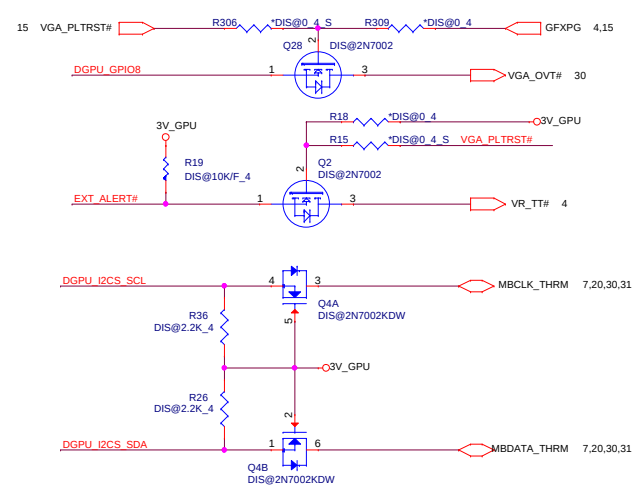
1.05V_GFX_PCIE
Near GPU 30ohm/100MHz ESR=0.01ohm
L20 DIS@HCB1608KF-300T10_1A_6
38mA
58mA
+NV_PLLVDD
Near GPU
L19 DIS@HCB1608KF-181T15 180/1500mA
+SP_PLLVDD
R57 *0_4
XTAL_SSIN A10
R332
C11
XTALIN
XTALOUTBUFF C10 BXTALOUT
XTALOUT B10
R313 DIS@10K/F_4
Y1
*DIS@27MHz
C363 *DIS@8.2P/50V/C0G_4
C366 *DIS@8.2P/50V/C0G_4
R300 0_4
DIS@10K/F_4
Under GPU
Near GPU
C376 C375 C379 C373 C97 C98
DIS@0.1U/10V/X7R_4
DIS@22U/6.3V/X5R_8
DIS@4.7U/6.3V/X5R_6
33 GPU_XTAL27_IN

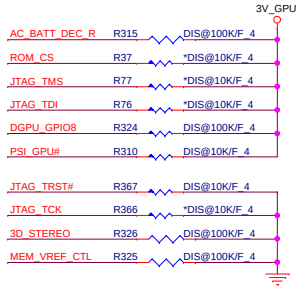
PROJECT : ST6A			
Quanta Computer Inc.			
Size	Document Number		Rev
	N14M-GE (DISPLAY) 3/5		1A
Date: Monday, April 01, 2013	Sheet 17	of 46	

<VGA>







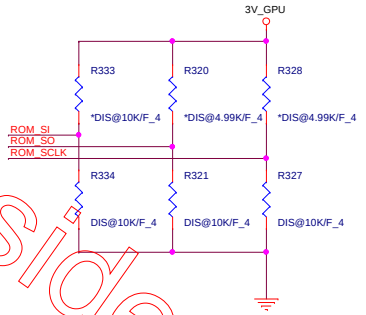


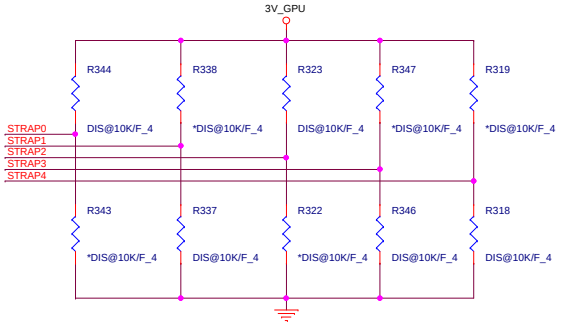
R496 and R498 could un-stuff for cost saving.
But need pull up for A-build, if no prolbem
then we can remove it at next build.

Res	PU	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	XXXX
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	PCI_DEVIDE[5]	PEX_PLL_EN_TERM	XXXX
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0110
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	XXXX
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP4	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0111

1GHz	Samsung	K4W2G1646E-BC1A	AKD5MGGT532
	Micron	MT41J128M16JT-093G:K	AKD5MGSTL15
	Hynix	Hynix 128x16 Vram H5TC2G63FFR-11C	AKD5MZDTW04
900MHz	Samsung	K4W4G1646B-HC11	AKD5MGWT516
	Micron	MT41K256M16HA-107G:E	AKD5PGSTL00





GF117 SKU	
Item	N14M-GE-B-A2
Device ID	0x1140
Package	GB4-128/GB2-64
Internal P/N	GF117, 28nm
ROM_SI	10kohm pull down
ROM_SO	10kohm pull down
ROM_SCLK	10kohm pull down
Strap0	Refer to N14x_RAM_Straps table
Strap1	
Strap2	
Strap3	
Strap4	10kohm pull down
Open_VRG SKU	Config C
NVVDD Boot Voltage	0.9V

DDR3 RAM_CFG													
GPU SKU	GPU	VRAM Vendor	Type		Config	VRAM P/N	Max Speed CLK	D/C Mini	RAM_CFG	Strap 3	Strap 2	Strap 1	Strap 0	Status
GF117	N14M-GE/GL	Micron	DDR3	1.5V/1.5V	128Mx16	MT41J128M16JT-093G:K	1000Mhz	1234	0x1	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
						MT41J128M16JT-107G:K	900Mhz	1150						Production ready
		Samsung	DDR3	1.5V/1.5V	128Mx16	K4W2G1646E-BC1A	1000Mhz	1204	0x5	PD 10K	PD 10K	PD 10K	PU 10K	Production ready
						K4W2G1646E-BC11	900Mhz	1204						Production ready
		Hynix	DDR3	1.5V/1.5V	128Mx16	H5TQ2G63DFR-N0C	1000Mhz	NA	0x6	PD 10K	PU 10K	PU 10K	PD 10K	Production ready
						H5TQ2G63DFR-11C	900Mhz							Production ready
		Hynix	DDR4	1.5V/1.5V	128Mx16	H5TC2G63FFR-11C	1000Mhz	NA	0XC	PU 10K	PD 10K	PU 10K	PD 10K	Post-production candidate
		Samsung	DDR3	1.5V/1.5V	256Mx16	K4W4G1646B-HC11	900Mhz	NA	0x8	PU 10K	PD 10K	PU 10K	PU 10K	
		Micron	DDR3	1.5V/1.5V	256Mx16	MT41K256M16HA-107G:E	900Mhz	NA	0xD	PU 10K	PU 10K	PU 10K	PU 10K	
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TQ4G63MFR-11C	900Mhz	NA	0x3	PD 10K	PU 10K	PU 10K	PU 10K	
		Hynix	DDR3	1.5V/1.5V	256Mx16	H5TQ4G63AFR-11C	900Mhz	NA	0x4	PD 10K	PD 10K	PD 10K	PD 10K	

PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	N14M-GE (GPIO/STRAPS) 4/5	1A
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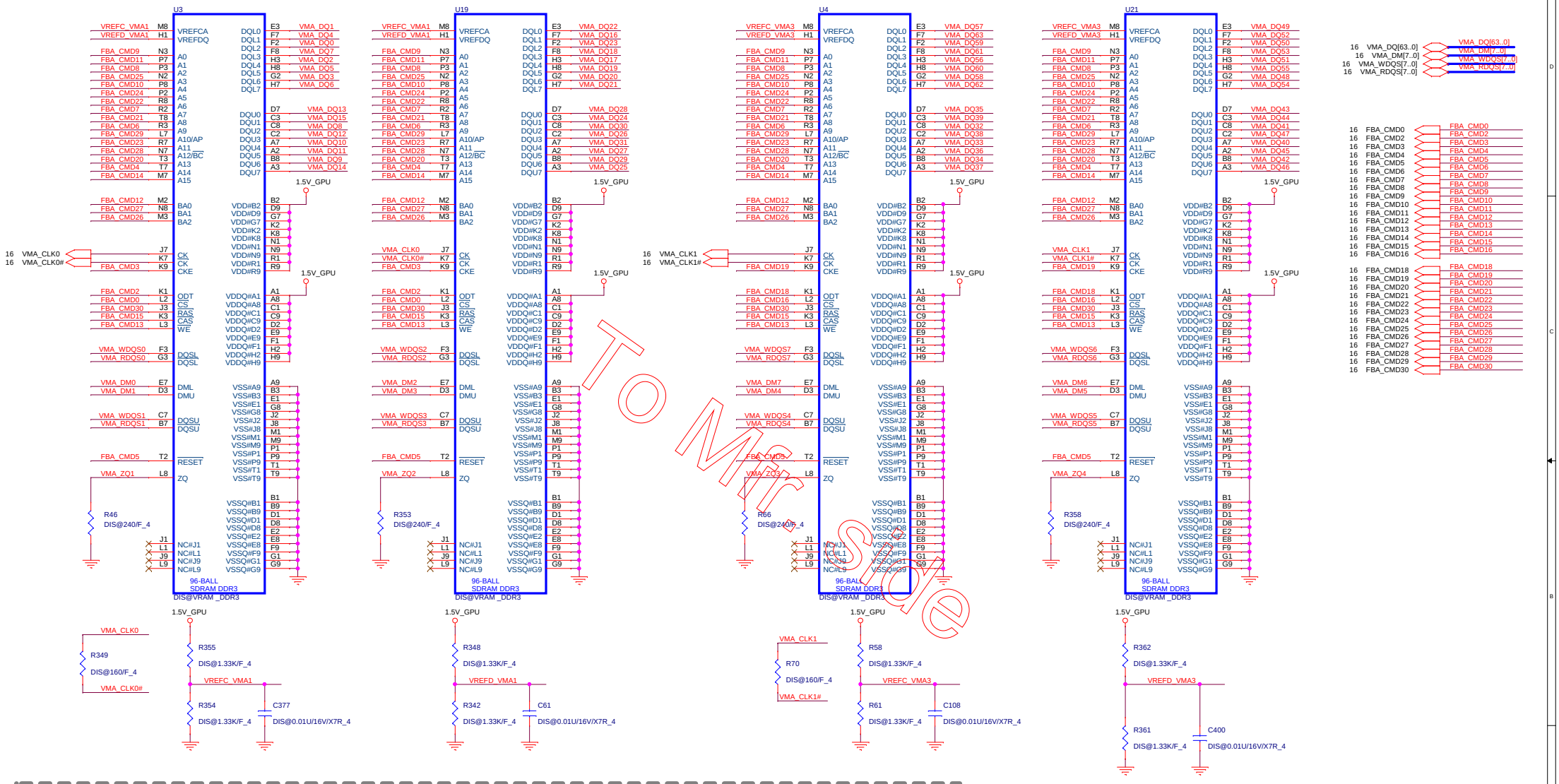
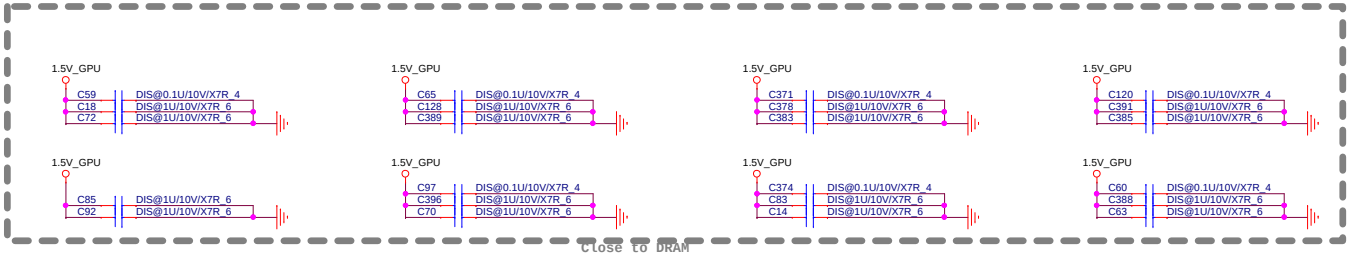
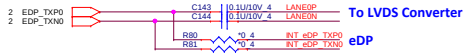
CHANNEL A: DDR3 4Gb x4
Double T Topology for DDR3 Memory

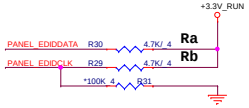




PROJECT : ST6A		
Quanta Computer Inc.		
Size	Document Number: DDR3 VRAM (BGA96) 5/5	Rev: 1A
Date: Monday, April 01, 2013	Sheet 19 of 46	



For EDP Only: stuff Resistor
For LVDS only stuff Cap



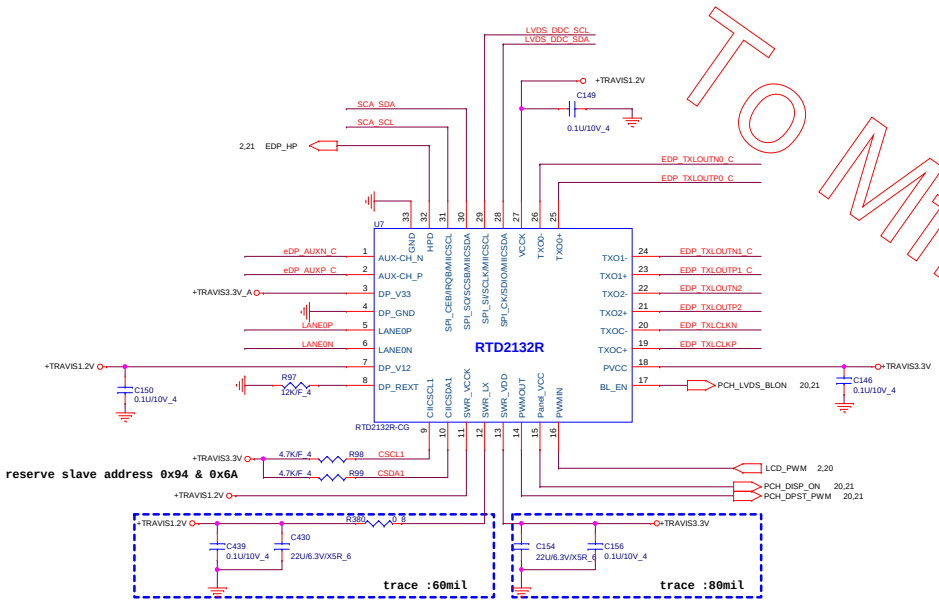
For LVDS stuff Ra=4.7k,Rb=4.7k

2,4,6,7,8,12,14,15,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN

SOURCE	Close to LVDS CONN		LVDS CONN
From LVDS Converter	EDP_TXLOUTP0_C	R304 0_4	EDP_TXLOUTP0 21
	EDP_TXLOUTN0_C	R303 0_4	EDP_TXLOUTN0 21
From CPU	INT_eDP_TXP0	C359 *0.1U/10V_4	
	INT_eDP_TXN0	C358 *0.1U/10V_4	
From LVDS Converter	LVDS_DDC_SDA	R317 0_4	PANEL_EDIDDATA 21
	LVDS_DDC_SCL	R316 0_4	PANEL_EDIDCLK 21
From CPU	INT_eDP_AUXN	C368 *0.1U/10V_4	
	INT_eDP_AUXP	C367 *0.1U/10V_4	
From LVDS Converter	EDP_TXLOUTP1_C	R308 0_4	EDP_TXLOUTP1 21
	EDP_TXLOUTN1_C	R307 0_4	EDP_TXLOUTN1 21
From CPU	EDP_TXP1	C362 *0.1U/10V_4	
	EDP_TXN1	C361 *0.1U/10V_4	
From LVDS Converter	EDP_TXLOUTP2		EDP_TXLOUTP2 21
	EDP_TXLOUTN2		EDP_TXLOUTN2 21
	EDP_TXLCLKN		EDP_TXLCLKN 21
	EDP_TXLCLKP		EDP_TXLCLKP 21

2 EDP_TXP1
2 EDP_TXN1

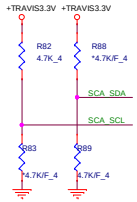
For eDP, close to U7

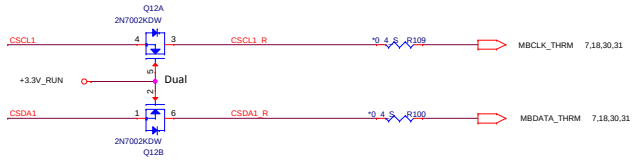


To Mfr. side

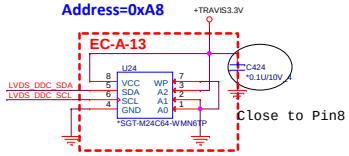
RTD2132R	SCA_SDA	
	0	1
SCA_SCL 0	X	EP MODE
SCA_SCL 1	ROM ONLY MODE	EEPROM MODE

R2132S--> only EEPROM mode
R2132R--> EP / EEPROM mode





Address=0xA8



PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	Custom RTD2132R	1A
Date: Monday, April 01, 2013	Sheet 20 of 46	

2,4,6,7,8,12,14,15,20,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN
6,23,30,31,33,35,36 +3.3V_ALW2
34,35,36,37,38,39,40,43 +PWR_SRC
23 +V3.3DX_AUDIO

LCDVCC

EC-A-09

PCH_DISP_ON
+3.3V_RUN
80mil
trace :80mil, reserve for RTD2132R
+LCDVCC
+LCDVCC_F
80mil
R13 0_8
R16 100K_4
C11 4.7U/6.3V/X5R_6
C5 *1U/6.3V_4
U1
IN
IN
ON/OFF
OUT
GND
R14 *0_6
C16 *10U/6.3V_6
C25 *0.01U/16V/X7R_4
C24 0.1U/10V_4
20 PCH_DISP_ON
R12 *100K/F_4
*IC(5P) G5243AT11U

Back light

+3.3V_ALW2
+3.3V_RUN
R3 10K_4
R8 *4.7K_4
30,31 LID#
D1 RB500V-40
D2 RB500V-40
DISPON
C8 0.1U/10V_4
R24 100K_4
C20 *47P/50V/NPO_4
PCH_LVDS_BLON_R
R9 2.2K_4
R6 100K_4
C7 *1U/10V/X7R_6
Q1
LTC044EUBFS8TL
LCD_BK_OFF 4

GFX_PWR_SRC

+PWR_SRC
GFX_PWR_SRC
40mil
R11 0_8
C12 *10U/25V/X6S_12
C9 0.1U/25V_6
C13 0.1U/25V_6

20 PCH_DPST_PWM
R35 *0_4_S
VADJ_PWM
C28 *47P/50V/NPO_4
R32 100K_4

EC-A-02

+3.3V_RUN
R22 Rc 0_4
2,20 EDP_HP
R23 *0_4
EDP_HPD_R
Rd
For LVDS Only: Stuff_Rc

For ESD
SC2 *0.1U/10V/X7R_4
C17 2.2U/10V/X5R_6

+LCDVCC
20 PANEL_EDIDCLK
20 PANEL_EDIDDATA
PANEL_EDIDCLK
PANEL_EDIDDATA
20 EDP_TXLOUTN0
20 EDP_TXLOUTP0
20 EDP_TXLOUTN1
20 EDP_TXLOUTP1
20 EDP_TXLOUTN2
20 EDP_TXLOUTP2
20 EDP_TXLCLKN
20 EDP_TXLCLKP
USB- TPanel_R
USB+ TPanel_R
VADJ_PWM
DISPON
2 TOUCH_PANEL_RST#
R7 *0_4
TOUCH_FINGER_EN_R
+V3DX_TCH_PNL
30 WIN_BTN#
R10 *0_4
GFX_PWR_SRC
CN3
LCD_CONN

Touch Panel

USB- TPanel_R
USB+ TPanel_R
FC12 *EGA-0402
FC13 *EGA-0402
For ESD

EDP_HP
TOUCH_PANEL_RST#
PANEL_EDIDCLK
PANEL_EDIDDATA
WIN_BTN#
SC3
SC4
SC1
SC40
SC5
*SURGE SUP
For ESD

PANEL_EDIDCLK
C32 *47P/50V/NPO_4
For RF

USB interface

EC-A-20

MCM2012D900FBE
CML7
5 USB-_TPanel
5 USB+_TPanel
USB- TPanel_R
USB+ TPanel_R
4 TOUCH_FINGER_EN
R5 *0_4_S
TOUCH_FINGER_EN_R

Touch Panel VCC Control

EC-A-01

+3.3V_RUN
R17 0_6
+V3DX_TCH_PNL

EC-A-21

+3.3V_RUN
*DIS@0.1U/10V/X7R_4 C529
U39
2,20 PANEL_BKEN
20 PCH_LVDS_BLON
*TC7SH08FU(F)
PCH_LVDS_BLON_R
R535 0_4

CAMERA VCC Control

+CAM_VCC
Max Current : 800mA
+3.3V_RUN
+V3.3DX_CAMERA
R336 4.7K_4
Q29 AOS3413
C372 2200P/50V/X7R_4
4 CCD_EN
Q30 LTC044EUBFS8TL
+V3.3DX_CAMERA_R
R305 0_6
C360 0.1U/10V_4

CAMERA/DMIC CONN

23 DMIC_CLK1_C
23 DMIC_DATA1_C
+V3.3DX_AUDIO
R312 FCM1005KF-601T02
R311 FCM1005KF-601T02
DMIC_CLK
DMIC_DATA
+V3.3DX_CAMERA
USBP4- R
USBP4+ R
CAMERA_CONN
CN4
C22 0.1U/10V_4

EC-A-15

FOR ESD

5 USBP4+
5 USBP4-
R340 0_4
*MCM2012D900FBE
CML5
R341 0_4
USBP4+ R
USBP4- R
U18
IO1 VIN
IO2 GND
*PJSR05
+V3.3DX_CAMERA

For EMI

DMIC_DATA
DMIC_CLK
C364 100P/50V/NPO_4
C365 100P/50V/NPO_4
SC28
SC29
*SURGE SUP

PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	LCD/CAMERA/Touch Panel	1A
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2,4,6,7,8,12,14,15,20,21,23,24,26,27,29,30,31,32,34,35,40,41,42
23,25,32,35,40,41,42
+3.3V_RUN
+5V_RUN

EC-A-10

R513 560/F_4 HDMI_TX2+_C
R512 560/F_4 HDMI_TX2-_C
R511 560/F_4 HDMI_TX1+_C
R510 560/F_4 HDMI_TX1-_C
R509 560/F_4 HDMI_TX0+_C
R506 560/F_4 HDMI_TX0-_C
R504 560/F_4 HDMI_CLK+_C
R502 560/F_4 HDMI_CLK-_C

HDMI_LE

+5V_RUN
Q23 2N7002K

close to HSW ULT:1500 mil

+3.3V_RUN
R507 2.2K_4
R508 2.2K_4

2 HDMI_SCL
2 HDMI_SDA
Q38 DMN5L06K-7
Q39 DMN5L06K-7

+5V_RUN
D18 RB500V-40
D17 RB500V-40
R503 2.2K_4
R505 2.2K_4

FUSE1A6V_POLY
F1
HDMIC_5V
2 HDMI_HPD

HDMI_DDC_CLK
HDMI_DDC_DAT

CN12
SHELL1
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL2
HDMI CONN

2 HDMI_TX2+_C
2 HDMI_TX2-_C
2 HDMI_TX1+_C
2 HDMI_TX1-_C
2 HDMI_TX0+_C
2 HDMI_TX0-_C
2 HDMI_CLK+_C
2 HDMI_CLK-_C

U34
U33
U32
*AZ1045-04F

HDMI_TX2+_C
HDMI_TX2-_C
HDMI_TX1+_C
HDMI_TX1-_C
HDMI_TX0+_C
HDMI_TX0-_C
HDMI_CLK+_C
HDMI_CLK-_C
HDMI_DDC_DAT
HDMI_DDC_CLK
HDMIC_5V
HDMI_HPD

For ESD

Layout note:Place close to HDMI Conn

To Mfr. Side

EMI reserve for HDMI

R267 150/F_4
R266 150/F_4
R265 150/F_4
R264 150/F_4
EC-A-17

EC11 *220P/50V/X7R_4

PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI CONN	1A
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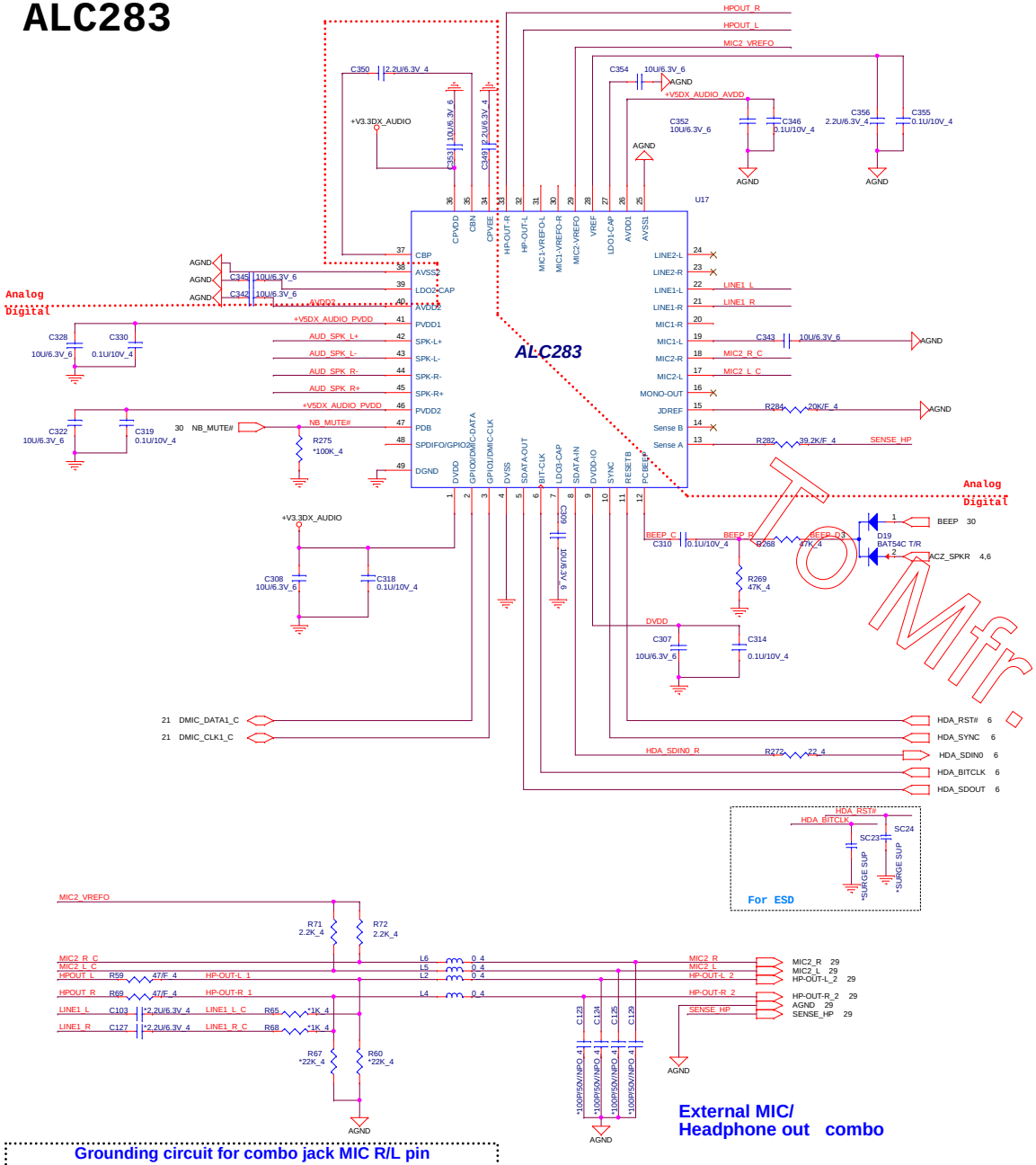
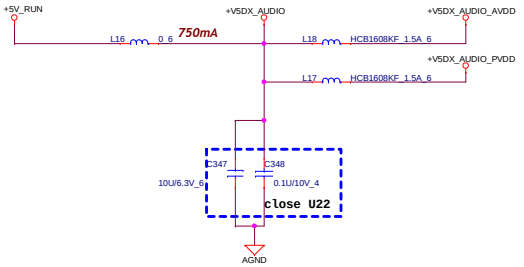
ALC283



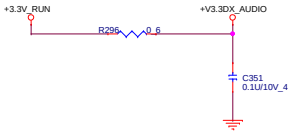
22,25,32,35,40,41,42 +5V_RUN
12,14,28,29,35,36,37,38,39,41,42,43,44 +5V_ALW
2,4,6,7,8,12,14,15,20,21,22,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN
4,6,8,12,24,27,29,31,35,36,41,44 +3.3V_DSW
21 +V3.3DX_AUDIO
12,27,34,39,42,44 +1.5V_RUN
6,21,30,31,33,35,36 +3.3V_ALW2

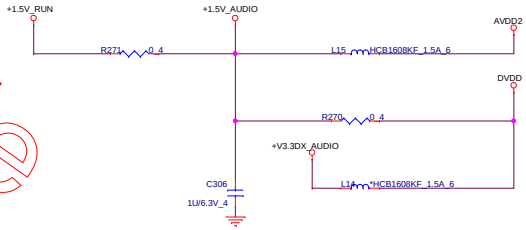
23

CODEC 5V POWER

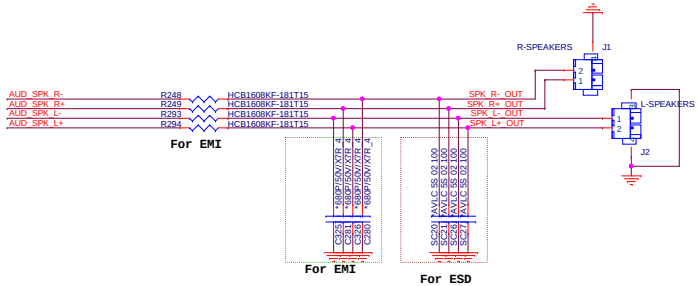


+3.3V_AUDIO_CODEC
Max Current : 419mA





INT Speaker



PROJECT : ST6A			
Quanta Computer Inc.			
Size	Document Number		Rev
	Audio(ALC283)		1A
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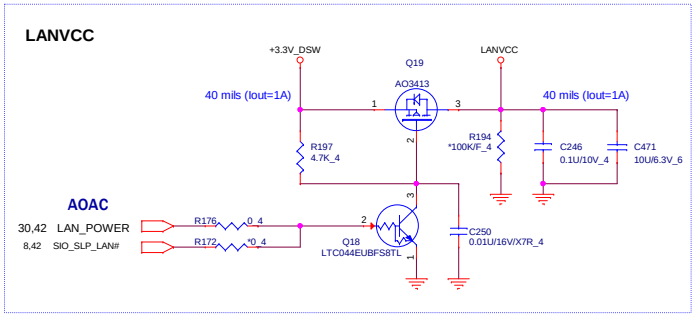
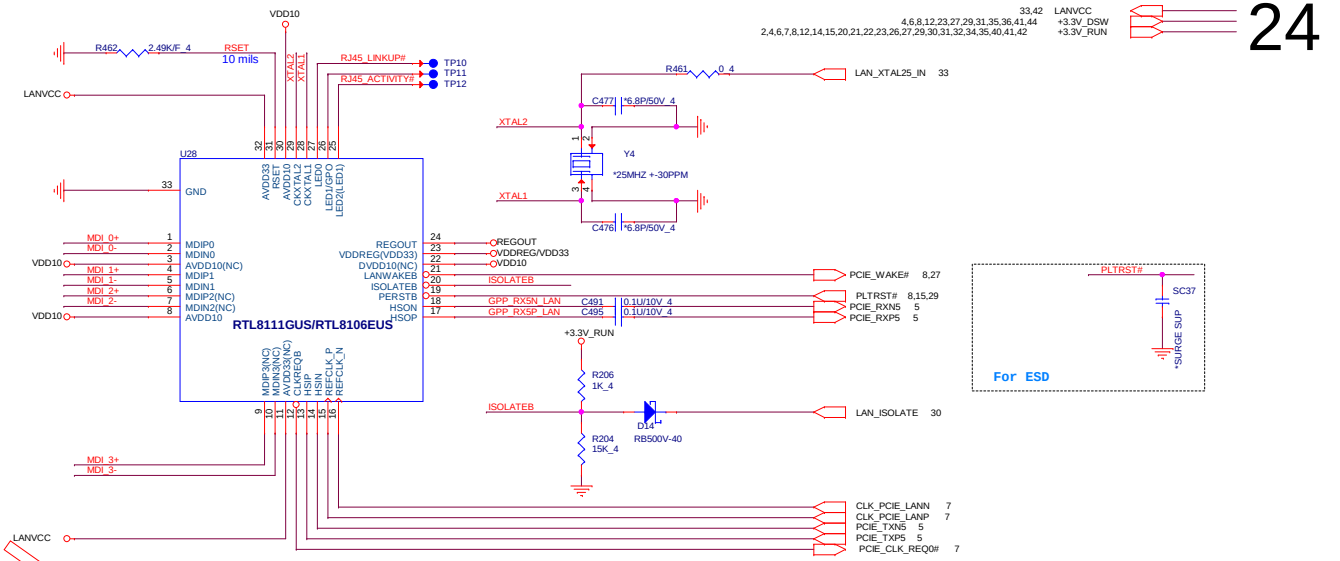
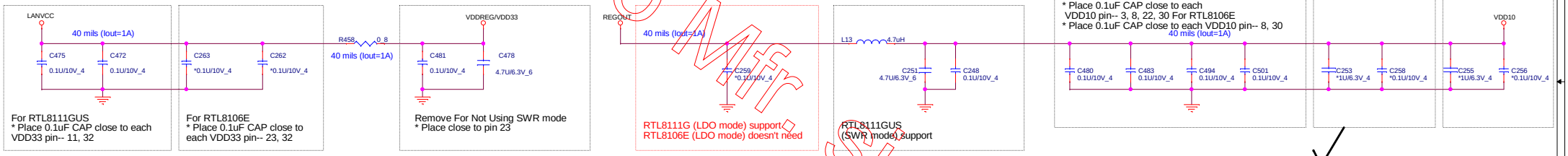


LANVCC
Trace width>60mil,
Trace length<200mil

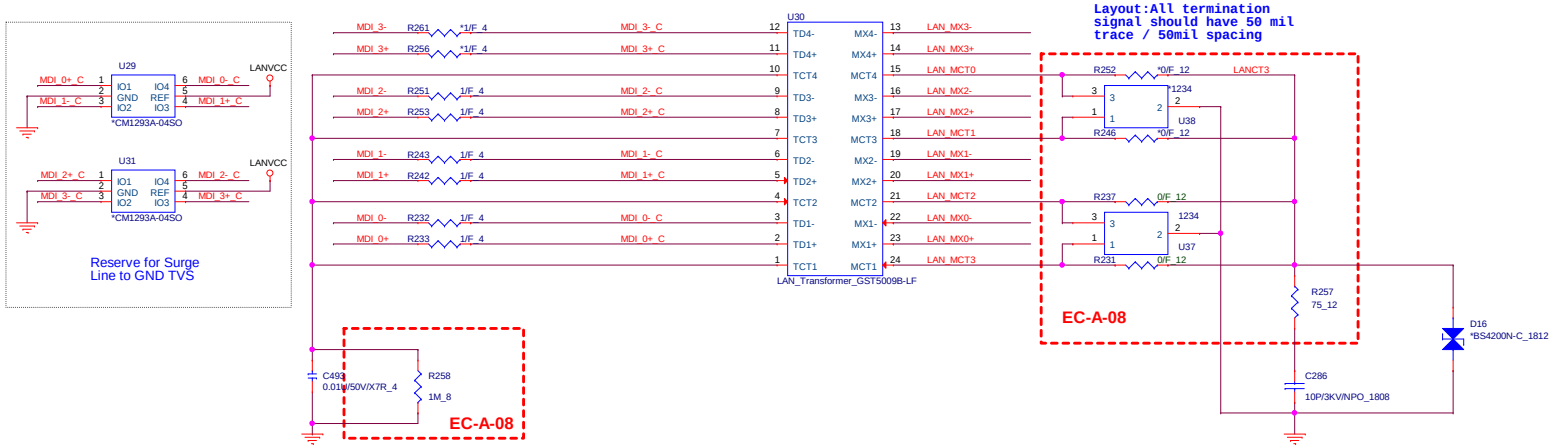


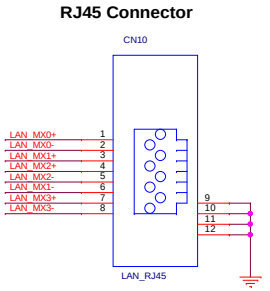
B-stage only 10/100 config.

10/100	RTL8106EUS-CG	AL008106002
1G	RTL8111GUS-CG	AL008111009



Tramsformer



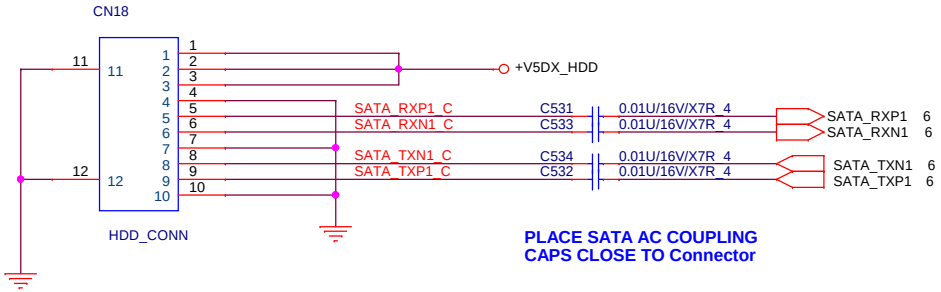


PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	LAN(RTL8111GUS)	1A
Date: Monday, April 01, 2013	Sheet 24 of 46	

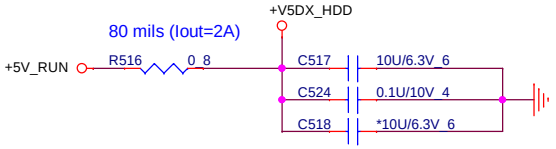
HDD

2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN
22,23,32,35,40,41,42 +5V_RUN



PLACE SATA AC COUPLING CAPS CLOSE TO Connector

DC Current rating: 2 A (MAX)

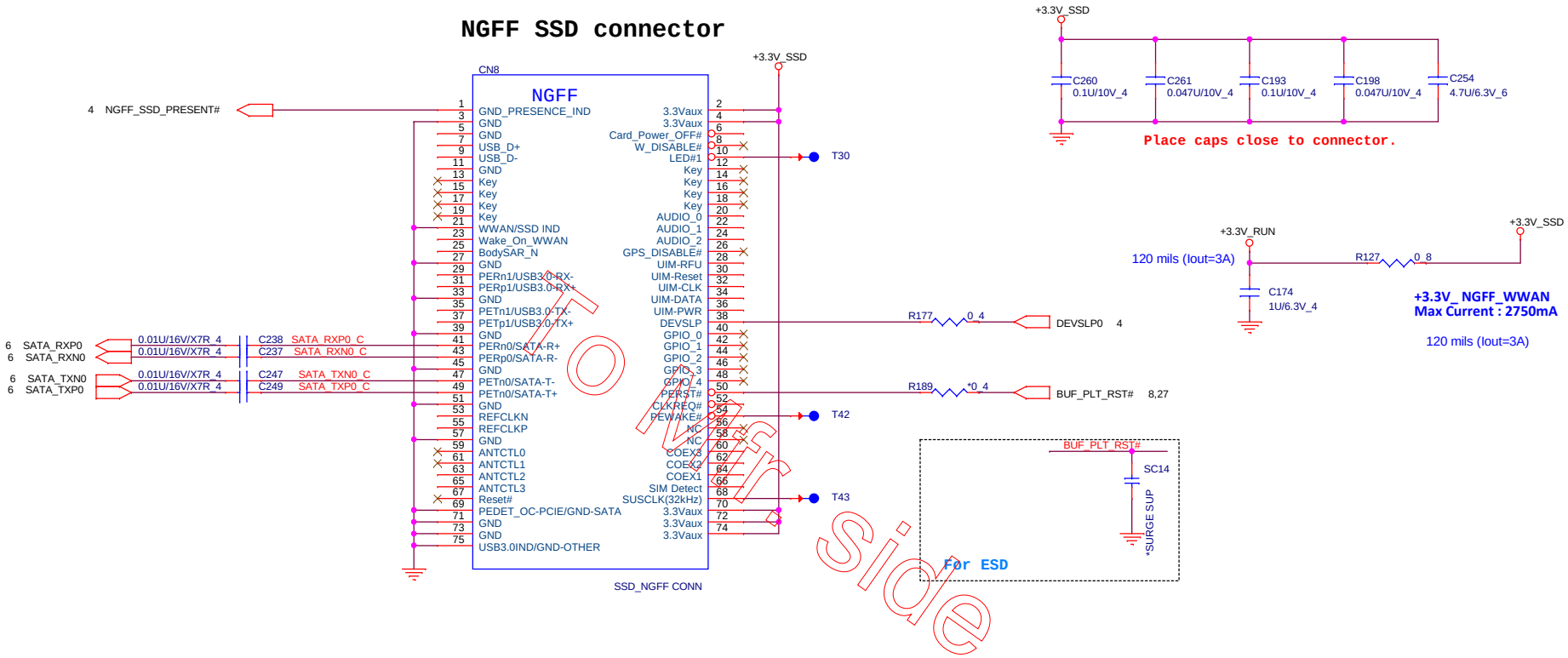


PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	SATA	1A
Date: Monday, April 01, 2013	Sheet 25 of 46	

2,4,6,7,8,12,14,15,20,21,22,23,24,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN

NGFF SSD connector



PROJECT : ST6A

Quanta Computer Inc.

Size	Document Number	Rev
	SSD NGFF	1A

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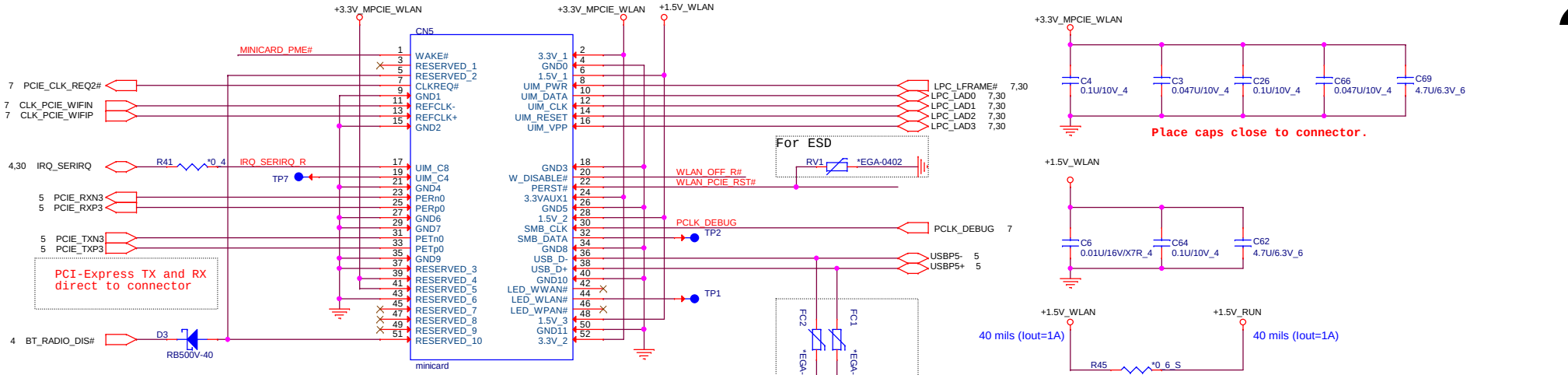
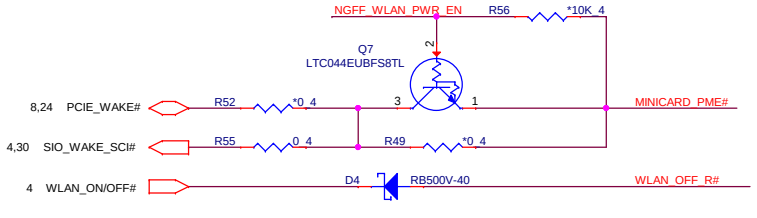
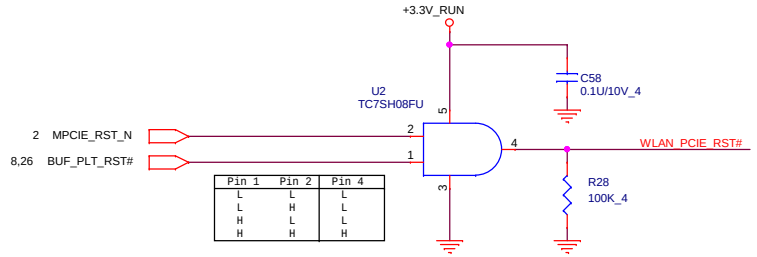
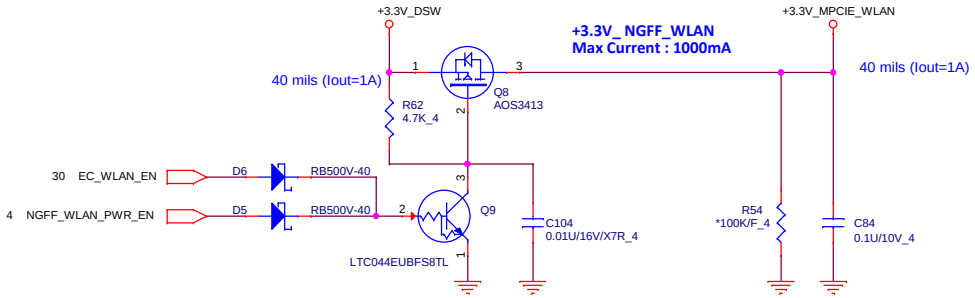
Mini PCIE Wifi/BT connector

2,4,6,7,8,12,14,15,20,21,22,23,24,26,29,30,31,32,34,35,40,41,42 +3.3V_RUN
4,6,8,12,23,24,29,31,35,36,41,44 +3.3V_DSW
12,23,34,39,42,44 +1.5V_RUN



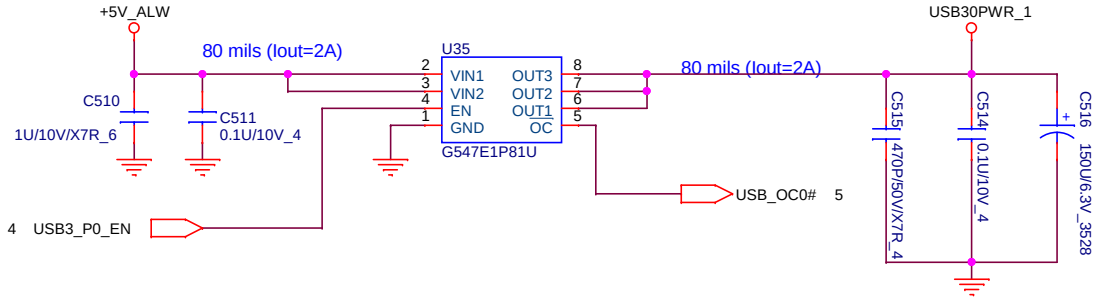


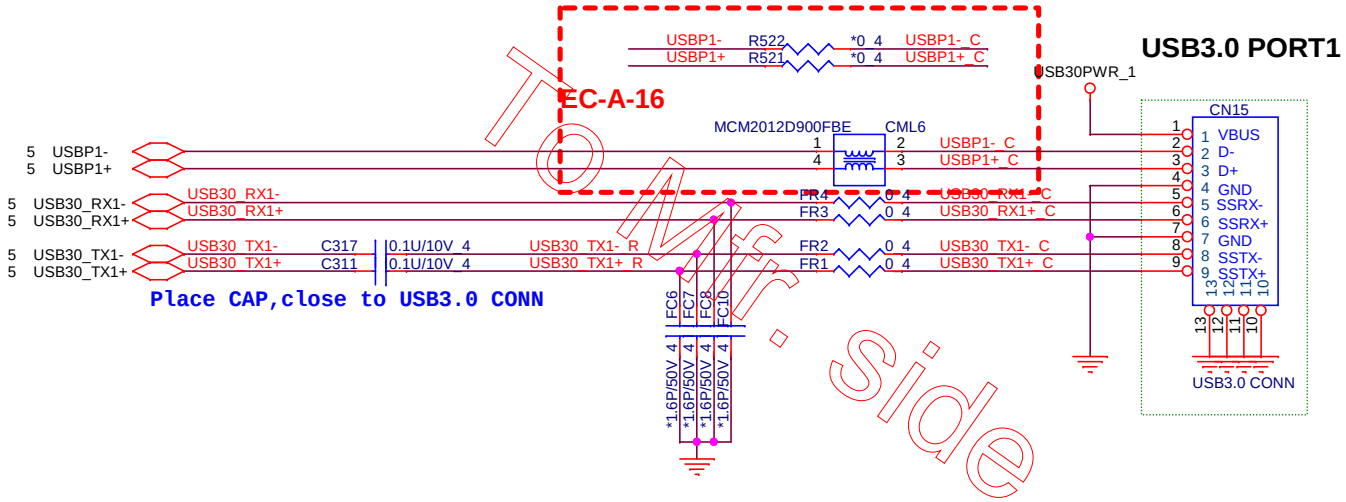


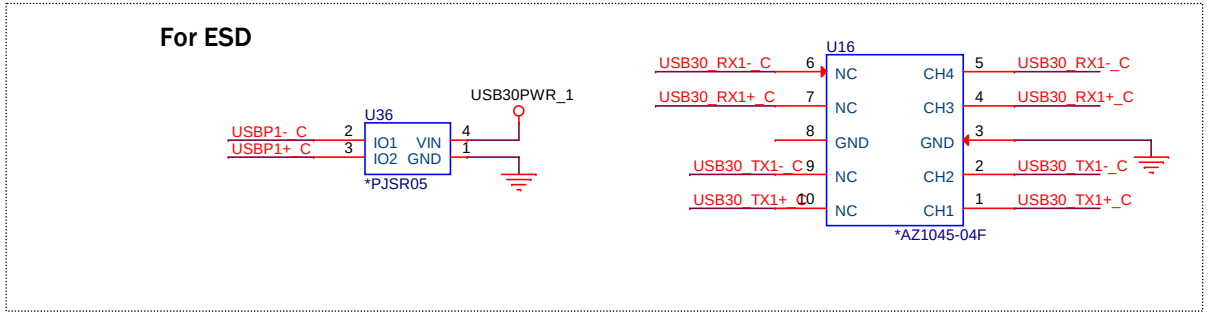


PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	Wifi/BT MiniPCIE	1A
Date: Monday, April 01, 2013	Sheet 27 of 46	







PROJECT : ST6A

Quanta Computer Inc.

Size	Document Number	Rev
	USB3.0 x1	1A
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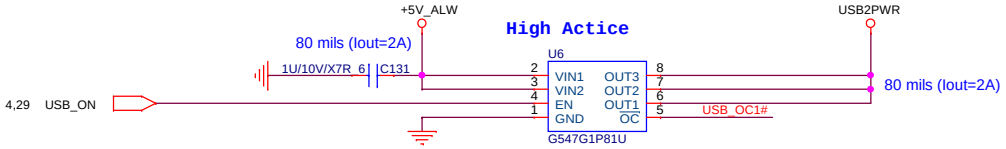
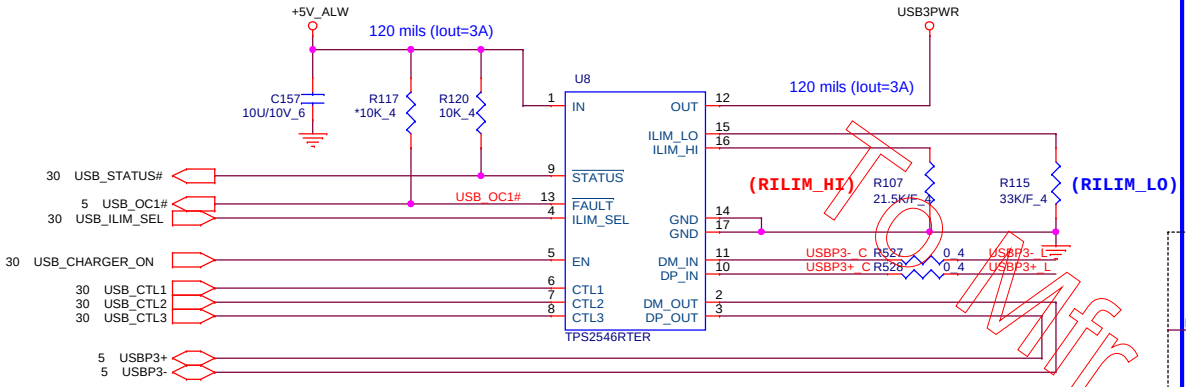
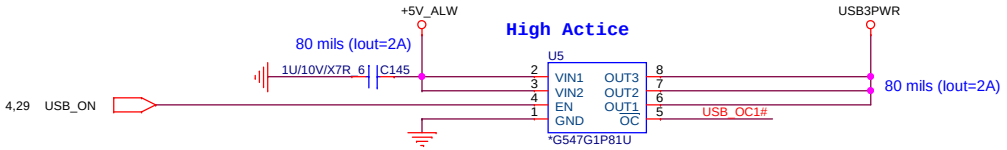
USB 2.0 Port *2





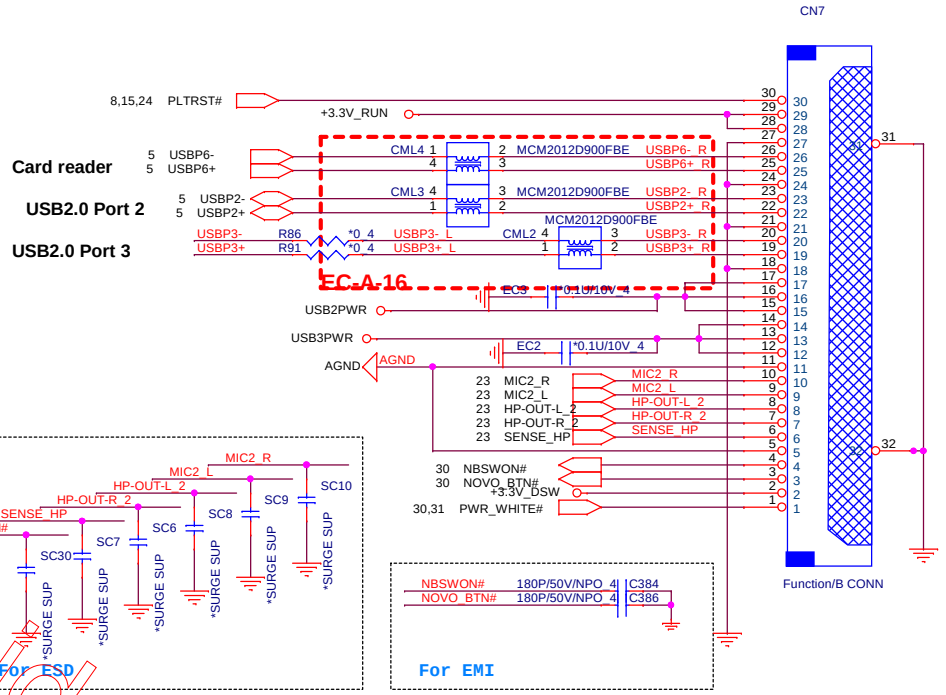
RILIM_LO is optional and the ILIM_LO pin may be left unconnected if the following conditions are met:
1. ILIM_SEL is always set high
2. Load Detection - Port Power Management is not used
3. Mouse / Keyboard wake function is not used
If conditions 1 and 2 are met but the mouse / keyboard wake function is also desired, it is recommended to use RILIM_LO < 80.6 kΩ.
The following equation programs the typical current limit:
(1)
RILIM_XX corresponds to either RILIM_HI or RILIM_LO as appropriate.

$$I_{OS\_typ}(mA) = \frac{50{,}500}{(R_{ILIM\_XX}(k\Omega) + 0.1)}$$



12,14,28,35,36,37,38,39,41,42,43,44 +5V_ALW
4,6,8,12,23,24,27,31,35,36,41,44 +3.3V_DSW
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,30,31,32,34,35,40,41,42 +3.3V_RUN

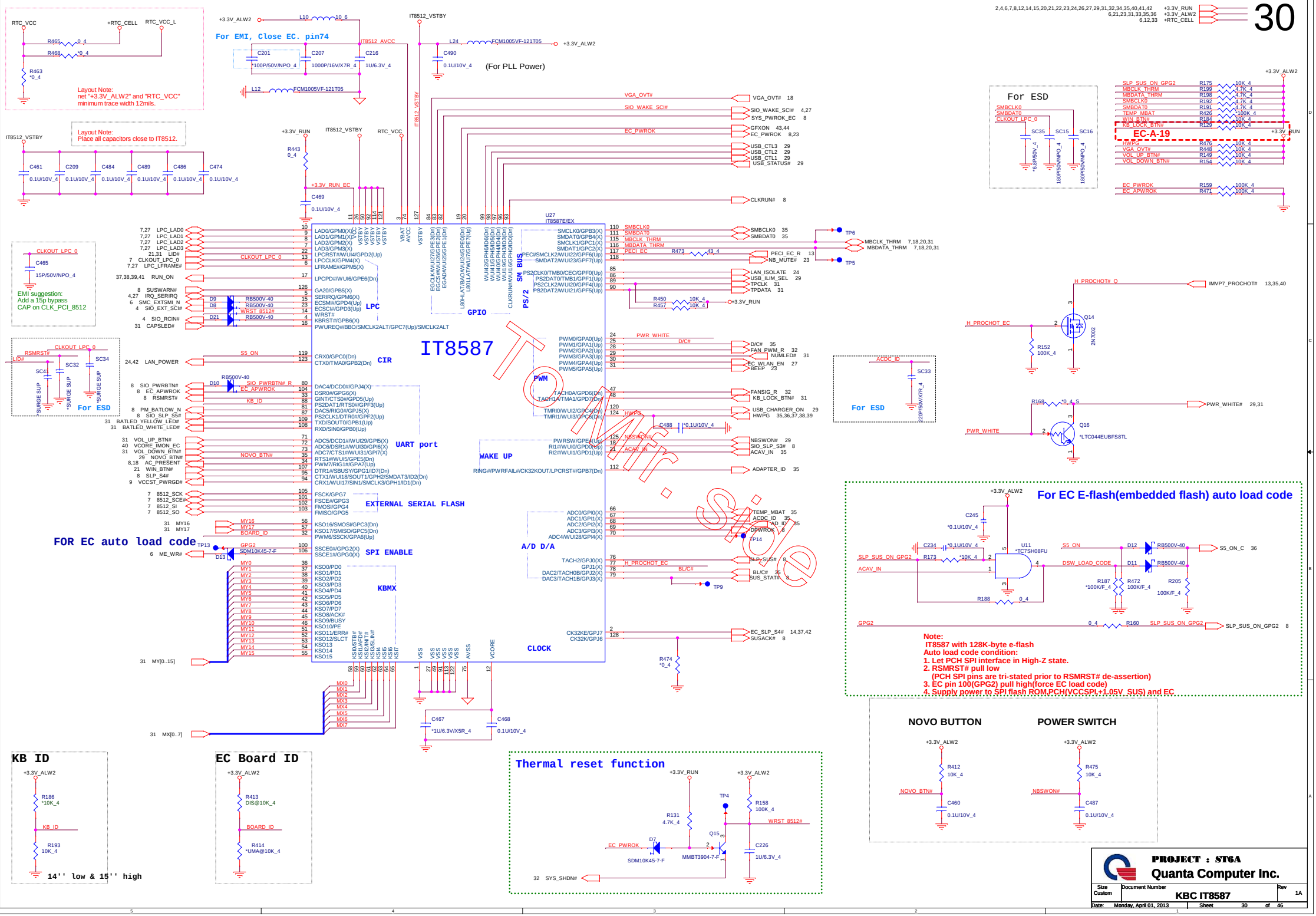
29



EC-A-04

PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	USB2.0--Audio Jack Conn	1A
Date: Monday, April 01, 2013	Sheet 29 of 46	



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBC IT8587	1A
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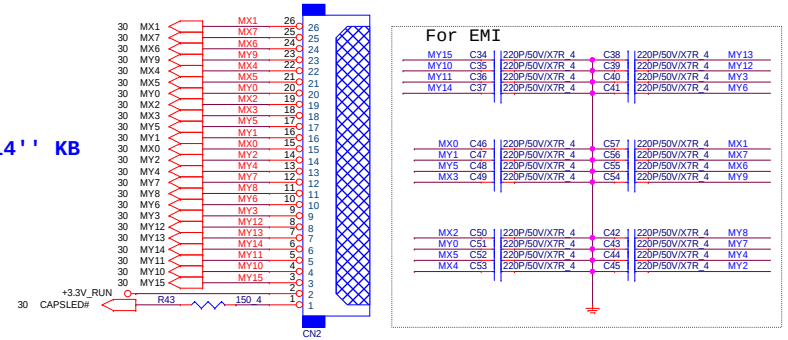
KEYBOARD

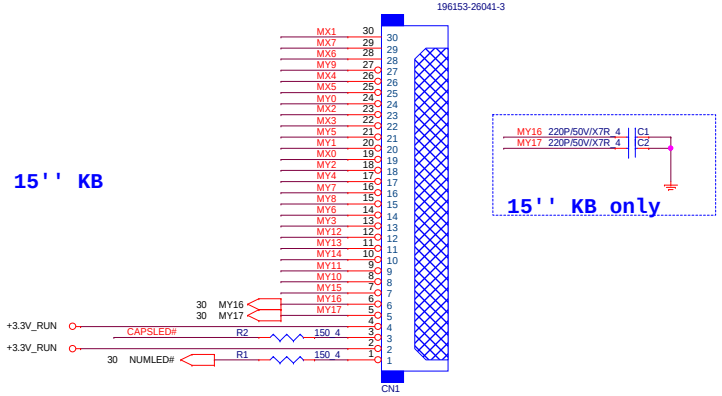
50584-02601-001

14'' KB



196153-26041-3

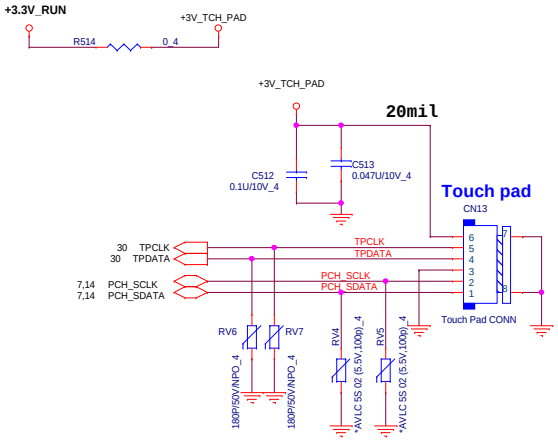
15'' KB



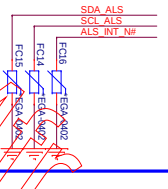
15'' KB only

TP Control

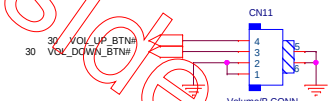
normal Current : 3mA



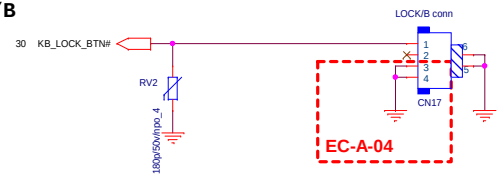
reserve for ESD



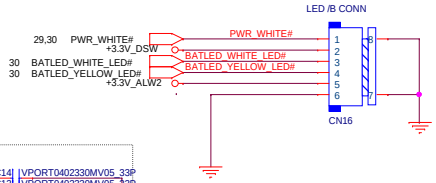
Volume/B

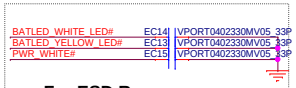


LOCK/B



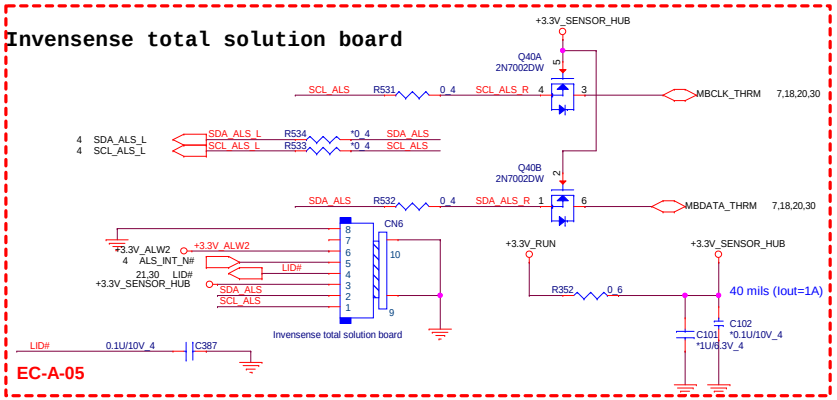
LED /B





DB CONN

Invensense total solution board



PROJECT : ST6A		
Quanta Computer Inc.		
Size	Document Number: KB/TP/LID	Rev: 1A
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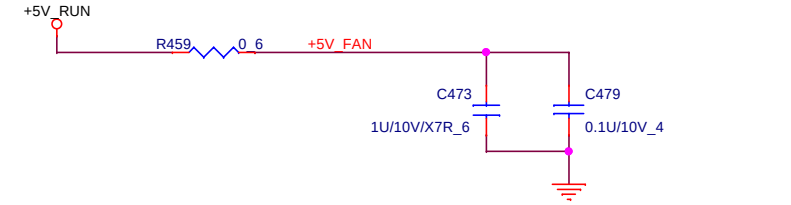
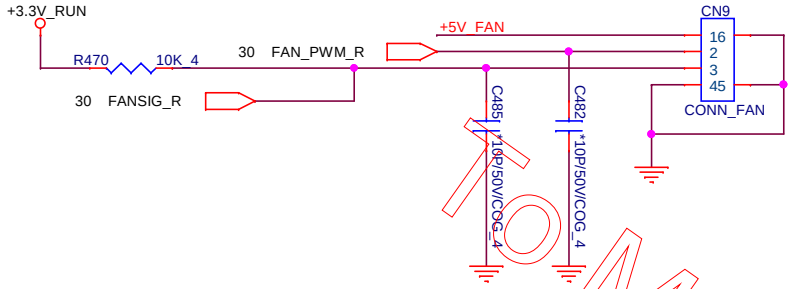
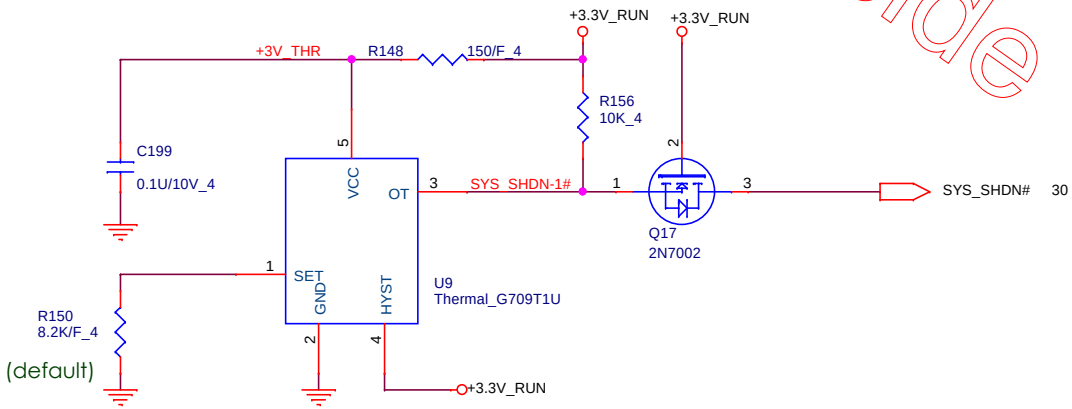
FAN CONTROL

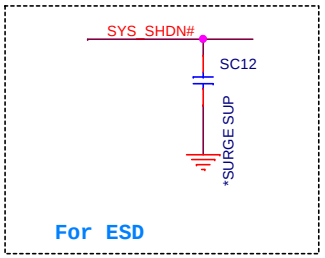
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,34,35,40,41,42 +3.3V_RUN
22,23,25,35,40,41,42 +5V_RUN





Thermal Sensor





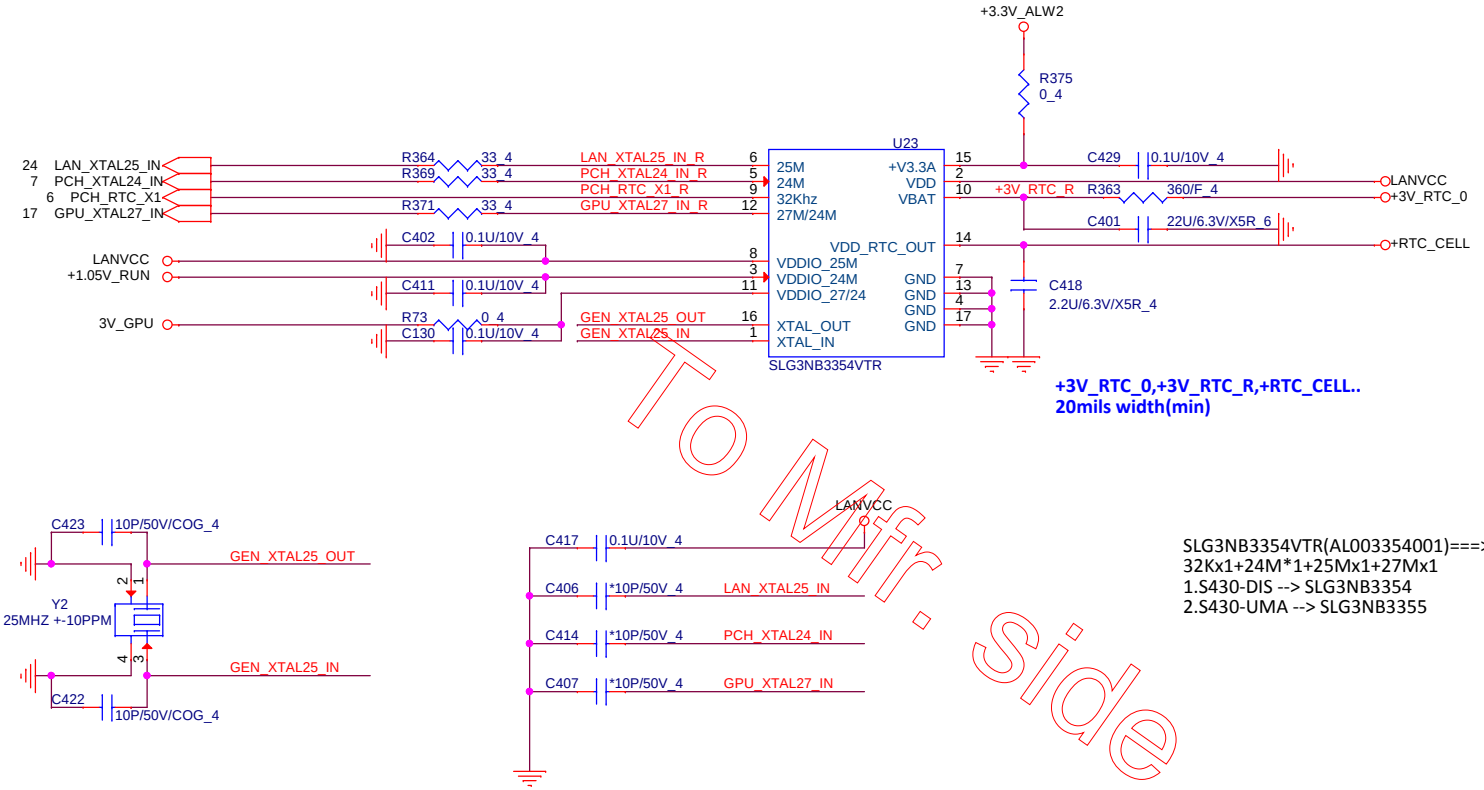
PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	FAN/Thermal	1A

Date: Monday, April 01, 2013 Sheet 32 of 46

6,21,23,30,31,35,36 +3.3V_ALW2
24,42 LANVCC
6 +3V_RTC_0
6,12,30 +RTC_CELL
6,9,12,34,38,40,42,44 +1.05V_RUN
15,18,34,43,44,45 3V_GPU

33



SLG3NB3354VTR(AL003354001)===>DIS
32Kx1+24M*1+25Mx1+27Mx1
1.S430-DIS --> SLG3NB3354
2.S430-UMA --> SLG3NB3355

PROJECT : ST6A

Quanta Computer Inc.

Size	Document Number	Rev
	Green Clock	1A
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HOLE6
*intel-bkt-shark-ult-type1

HOLE13
*hg-c296d110p2

HOLE7
*H-TC256BC276IC150D110P2

HOLE9
*H-C296IC150D110P2

HOLE3
*hg-c296d110p2

EC-A-18

HOLE12
*H-C296IC150D110P2

HOLE1
*hg-c276d110p2

HOLE5
*hg-c296d110p2

HOLE10
*H-C296IC150D110P2

+PWR_SRC
C398 *0.1U/10V_4
C459 0.1U/25V_4
C160 0.1U/25V_4
EC-A-18
C509 *0.1U/10V_4
C305 *0.1U/10V_4

HOLE8
*H-TC256BC110IC150D110P2

HOLE11
*H-C296IC150D110P2

+PWR_SRC
C357 0.1U/25V_4
EC-A-18
C334 0.1U/25V_4
C344 0.1U/25V_4
C508 *0.1U/10V_4
C257 0.1U/25V_4
EC-A-18

To Mfr. Side

3V_GPU
C134 *0.1U/10V_4
C370 *0.1U/10V_4
C530 180P/50V/NPO_4

+1.05V_RUN
C283 *0.1U/10V_4
C233 *0.1U/10V_4
C221 *0.1U/10V_4
C152 *0.1U/10V_4

+3.3V_RUN
C315 *0.1U/10V_4
C492 *0.1U/10V_4
C285 *0.1U/10V_4
C284 *0.1U/10V_4
C287 *0.1U/10V_4

+VCCIN
C273 *0.1U/10V_4
C241 *0.1U/10V_4
C445 *0.1U/10V_4

+3.3V_DEEP_SUS
C288 *0.1U/10V_4
C279 *0.1U/10V_4
C507 *0.1U/10V_4
C470 *0.1U/10V_4

+3.3V_RUN
C289 *0.1U/10V_4
C436 *0.1U/10V_4
C161 *0.1U/10V_4
C369 *0.1U/10V_4
C10 *0.1U/10V_4

+1.5V_RUN
C341 *0.1U/10V_4
C299 *0.1U/10V_4
C33 *0.1U/10V_4
C427 *0.1U/10V_4
C175 *0.1U/10V_4

EMI reserve

PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	Screw Hole/EMI	1A
Date: Monday, April 01, 2013	Sheet 34 of 46	

Footprint & P/N = okay = LZ1@1219 -- ALF

DC-IN

30 ACDC_ID

30 ACAV_IN

30,35 AD_ID

4 ADP_TYPE_0

4 ADP_TYPE_1

ADAPTER_ID 30

ACIN=17.5V

Place these CAPs close to FETs

Battery Low 7.5V

30 D/C#

BL/C# 30

30,36,37,38,39 HWPG

13,30,40 IMVP7_PROCHOT#

ACDC_det

	90W	65W	45W
ADP_TYPE_0	1	0	0
ADP_TYPE_1	0	1	0

10ms one-shot circuit

Pin Define = okay - @1224 -- ALF

Footprint okay - need check & P/N not ready @1216 -- ALF

PROJECT : ST6/6A

Quanta Computer Inc.

Size: Custom | Document Number: Charger (BQ24737) | Rev: 1A

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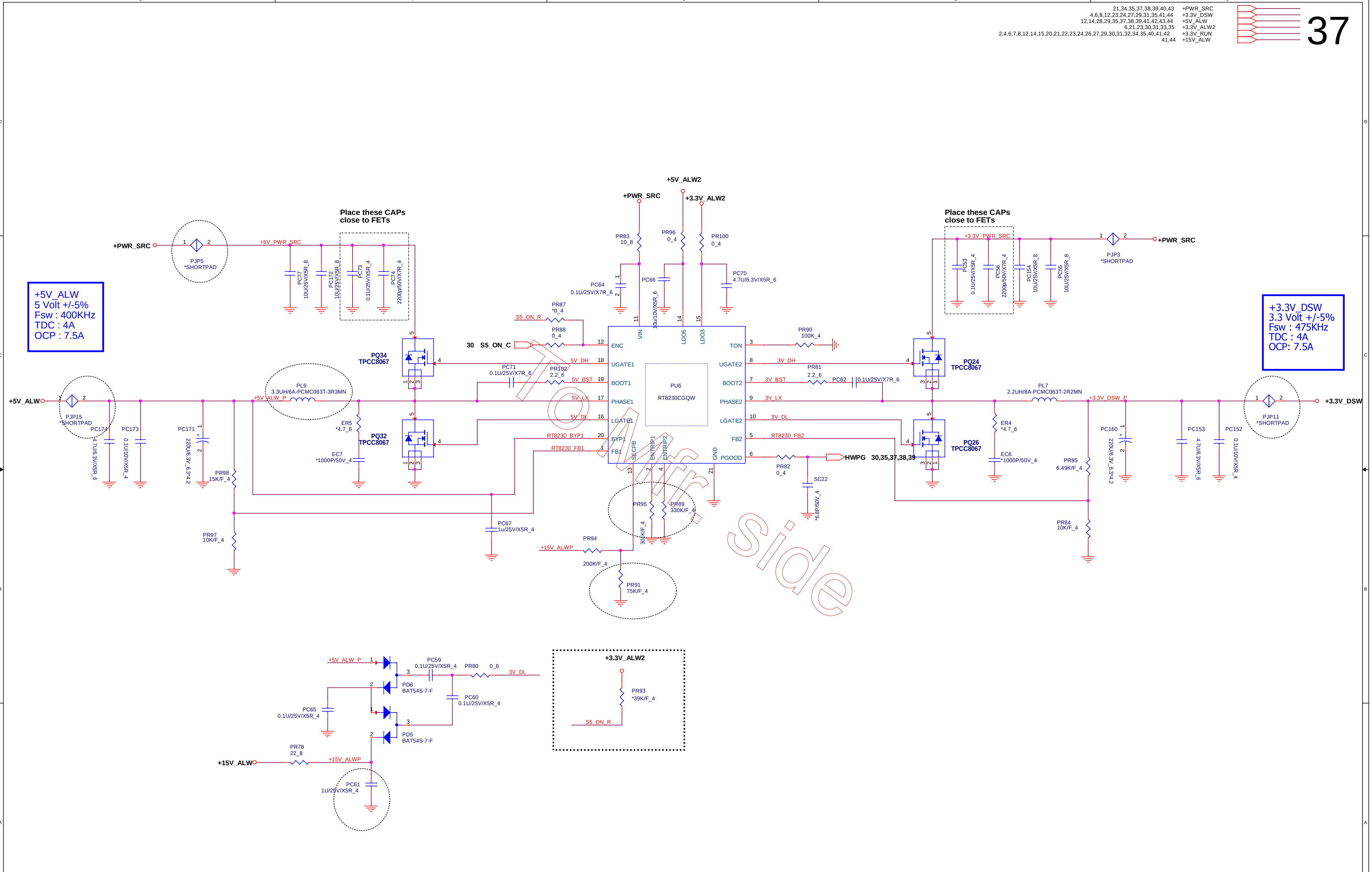
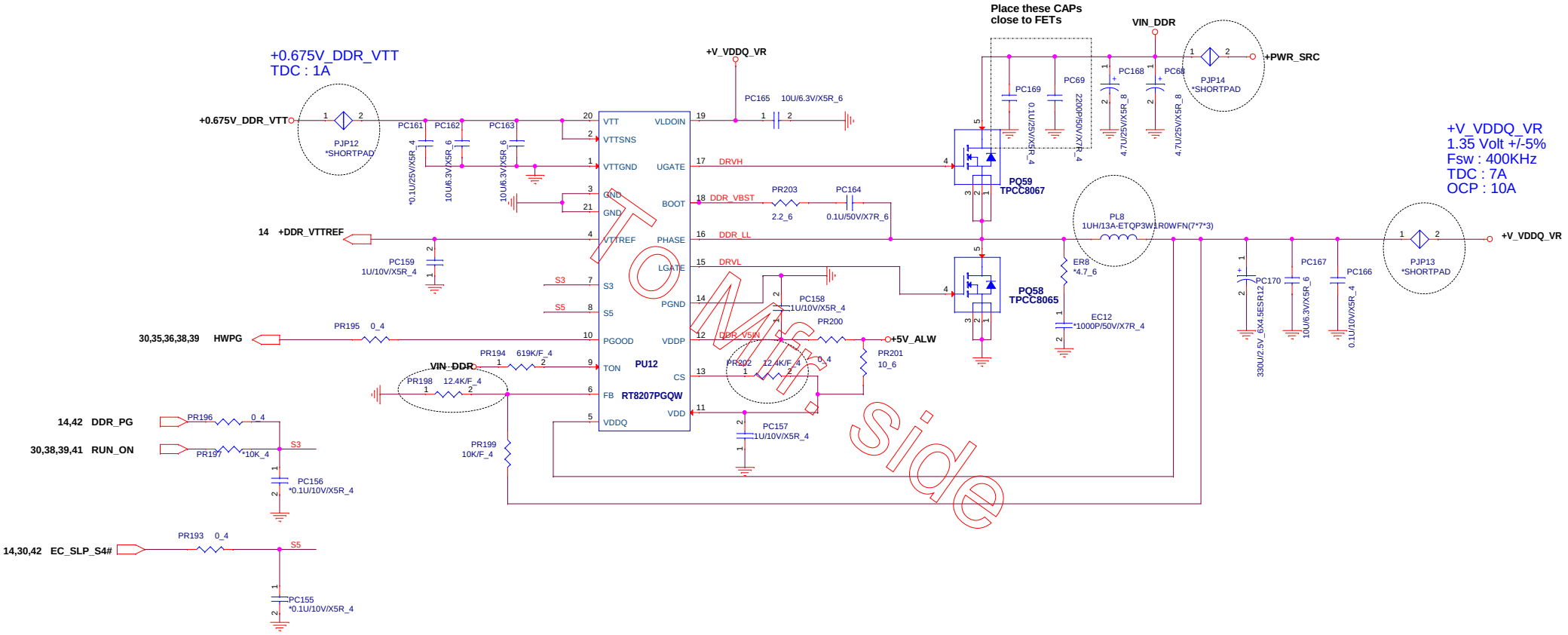
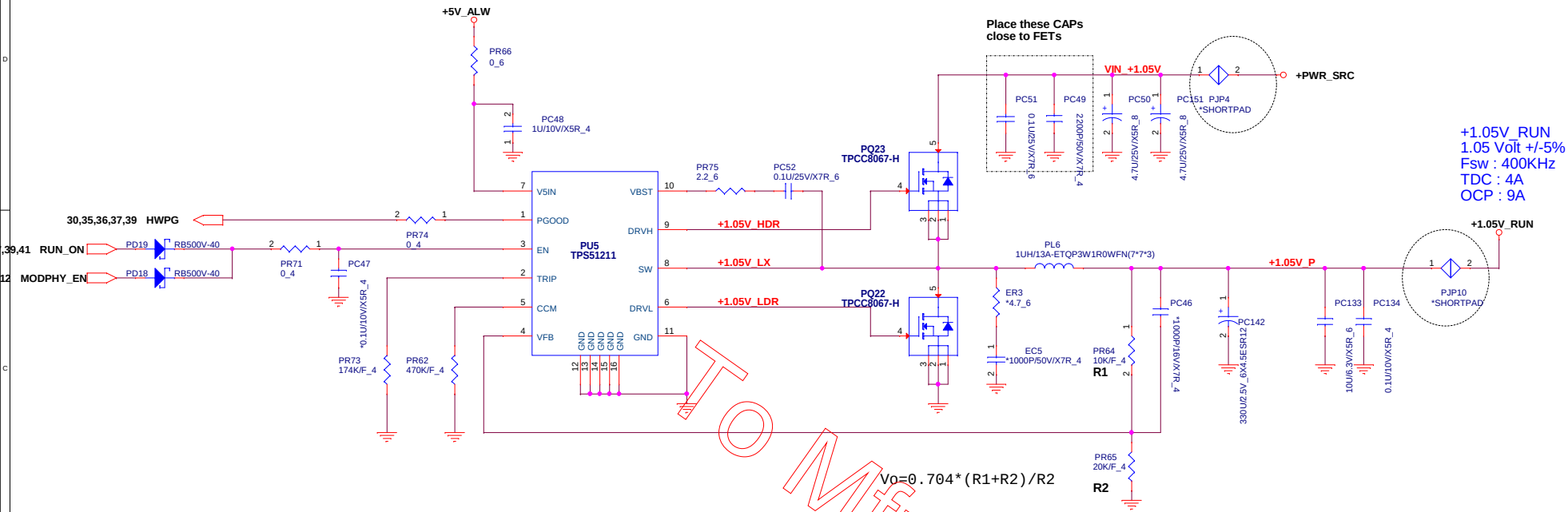


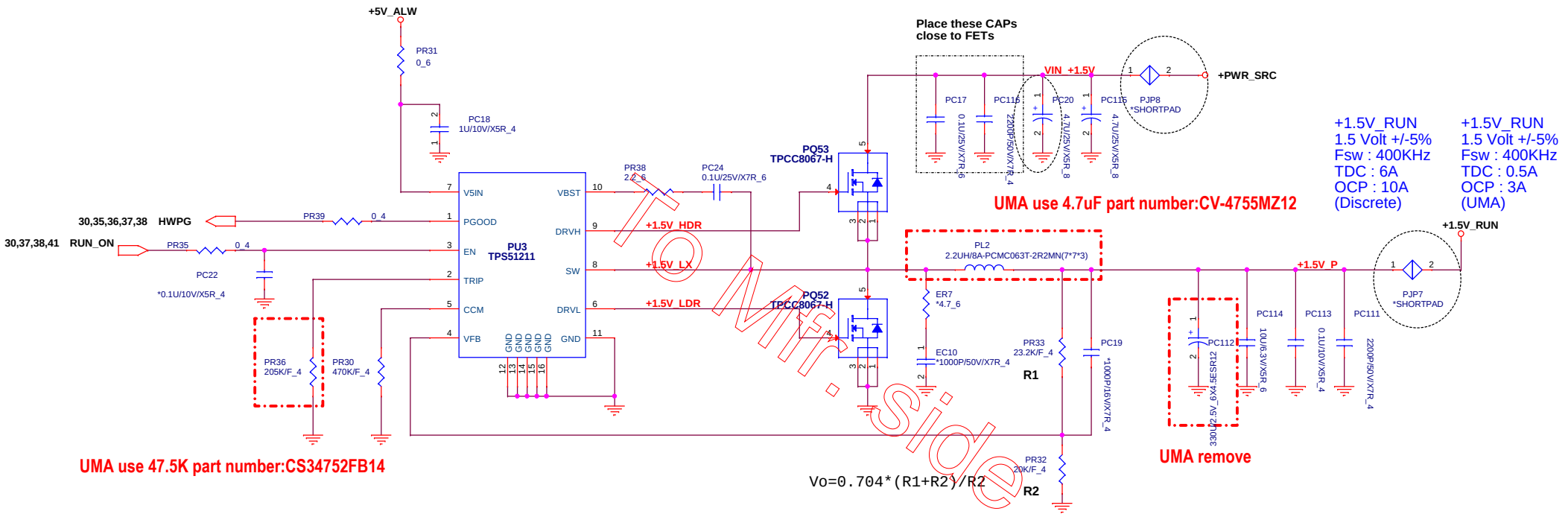
PROJECT : ST6A		
Quanta Computer Inc.		
Size	Document Number: 3V/5V (TPS51285)	Rev 1A
Date: Monday, April 01, 2013	Sheet 36 of 46	



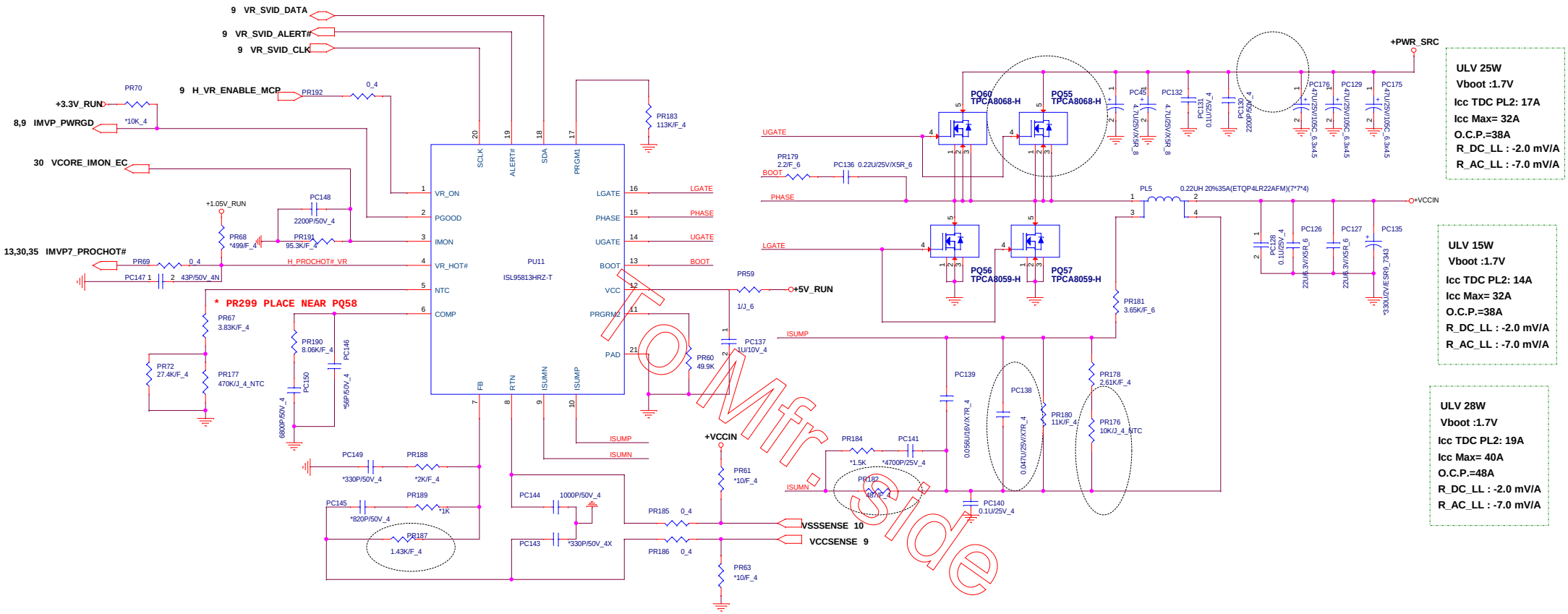
PROJECT LZ8 Chief River DIS		
Quanta Computer Inc.		
Size	Document Number: DDR3/0.75V (TPS51216)	Rev
Date: Monday, April 01, 2013	Sheet 37 of 46	



PROJECT : ST6A			
Quanta Computer Inc.			
Size: Custom	Document Number: +1.05V(TPS51211)		Rev: 1A
Date: Monday, April 01, 2013	Sheet 38 of 46		



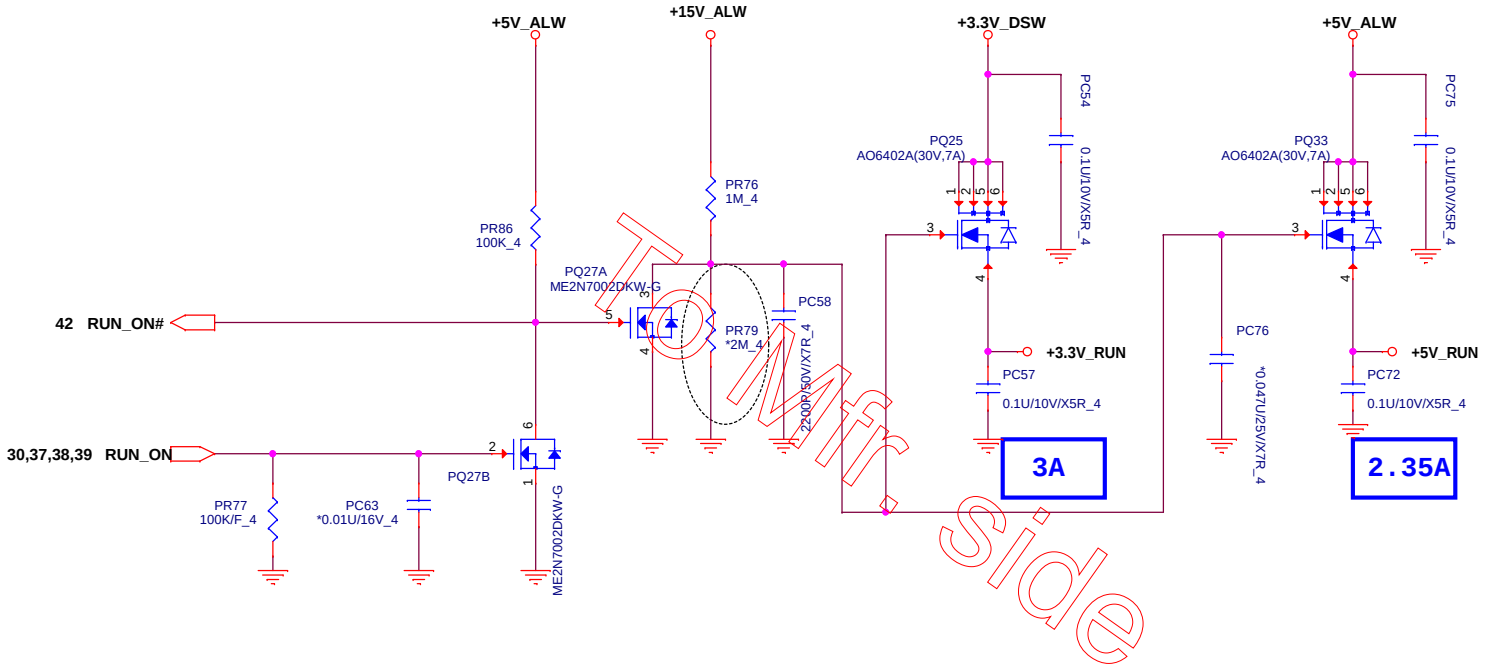
PROJECT : ST6A		
Quanta Computer Inc.		
Size: Custom	Document Number: +1.5V	Rev: 1A
Date: Monday, April 01, 2013	Sheet 39 of 46	



Quanta Computer Inc.		
PROJECT : PD5C		
Size	Document Number: +VCCIN (ISL95813) 15W	Rev: 1A
Date: Monday, April 01, 2013	Sheet 40 of 46	

12,14,28,29,35,36,37,38,39,42,43,44 +5V_ALW
36,44 +15V_ALW
22,23,25,32,35,40,42 +5V_RUN
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,42 +3.3V_RUN
4,6,8,12,23,24,27,29,31,35,36,44 +3.3V_DSW
6,9,12,33,34,38,40,42,44 +1.05V_RUN

42



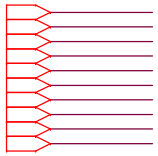
PROJECT : ST6A

Quanta Computer Inc.

Size	Document Number	Rev
	Load Switch	1A
Date: Monday, April 01, 2013	Sheet 41 of 46	

DISCHARGE

12,14,28,29,35,36,37,38,39,41,43,44	+5V_ALW
22,23,25,32,35,40,41	+5V_RUN
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41	+3.3V_RUN
12,23,27,34,39,44	+1.5V_RUN
6,9,12,33,34,38,40,44	+1.05V_RUN
14,37	+0.675V_DDR_VTT
4,5,6,7,8,12,14,34	+3.3V_DEEP_SUS
9,14,37	+V_VDDQ_VR
24,33	LANVCC
36,41,44	+15V_ALW



+5V_RUN +3.3V_RUN +1.5V_RUN +1.05V_RUN

41 RUN_ON# — RUN_ON#

PR99 22_8 — PQ28 2N7002
PR101 22_8 — PQ30 2N7002
PR103 22_8 — PQ31 2N7002
PR92 22_8 — PQ29 2N7002

+5V_ALW +0.675V_DDR_VTT

14,37 DDR_PG

PR108 100K/F_4
PR106 22_8
PQ35A ME2N7002DKW-G
PQ36A ME2N7002DKW-G

+5V_ALW +V_VDDQ_VR

14,30,37 EC_SLP_S4#

PR105 100K/F_4
PR107 22_8
PQ35B ME2N7002DKW-G
PR104 100K/F_4
PQ36B ME2N7002DKW-G

LANVCC

+5V_ALW LANVCC

24,30 LAN_POWER
8,24 SIO_SLP_LAN#

PR57 0_4
PR55 *0_4
PR58 100K/F_4
PR56 22_8
PQ20 2N7002
PQ21 2N7002

PROJECT : ST6A

Quanta Computer Inc.

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	Discharge	

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30,44 GFXON

PR170 0_4 8812EN

PC36 *0.022U/16V/X7R_4

+5V_ALW

PR41 1/F_6

PC30 1U/6.3V_4

RT8812A_1_VIN

PC42 0.01U/25V/X7R_4

PR54 1/F_6

PR52 499K/F_4

PU4 RT8812A

8812PVCC

8812TON

8812EN

18 PSI_GPU#

18 PWM-VID

PR48 0_4 8812PSI

PR49 0_4 8812VID

PC40 *33P/50V_4

PC44 0.1U/10V/X5R_4

8812VREF

8812REFADJ

PR175 30K/F_4

PR174 39K/F_4

PC125 1800P/50V/X7R_4

PR173 34K/F_4

8812REFIN

PC43 *47P/50V/NPO_4

8812SS

PC38 22P/50V/NPO_4

PR172 24K/F_4

PR171 3K/F_4

TON EN PSI VID REFADJ REFIN SS GND PVCC

BOOT1 8812BOOST1
UGATE1 8812UGATE1
PHASE1 8812PHASE1
LGATE1 8812LGATE1
BOOT2 8812BOOST2
UGATE2 8812UGATE2
PHASE2 8812PHASE2
LGATE2 8812LGATE2
PG 8812PG
VSNS 8812VSNS
RGND 8812RGND

8812BOOST1 PR43 2.2_6

PC32 0.22U/25V/X5R_6

8812UGATE1

PQ19 TPCA8068-H

8812PHASE1

PL4 ETQP4LR36AFM (7*7*3)

8812LGATE1

PQ16 TPCA8059-H

PR42 10.5K/F_4

ER2 *4.7_6

EC4 *1000P/50V/X7R_4

RT8812A_1_VIN

PC124 0.1U/25V_6

PC35 2200P/50V_4

PC34 4.7U/25V/X5R_8

PC123 4.7U/25V/X5R_8

PJP2 *SHORTPAD

+PWR_SRC

VGPU_CORE

PC120 560U/2V/ESR45_7343

PC21 10U/6.3V_6

PC118 0.1U/10V_4

8812BOOST2 PR44 2.2_6

PC33 0.22U/25V/X5R_6

8812UGATE2

PQ18 TPCA8068-H

8812PHASE2

PL3 ETQP4LR36AFM (7*7*3)

8812LGATE2

PQ15 TPCA8059-H

ER1 *4.7_6

EC1 *1000P/50V/X7R_4

RT8812A_2_VIN

PC122 0.1U/25V_6

PC31 2200P/50V_4

PC28 4.7U/25V/X5R_8

PC121 4.7U/25V/X5R_8

PJP1 *SHORTPAD

+PWR_SRC

PC119 330U/2V/ESR9_7343

PC23 10U/6.3V_6

PC117 0.1U/10V_4

VGPU_CORE
PEAK :30A
OCP :38A

3V_GPU

PR45 1.91K/F_4

PR47 0_4

8812PG

NVVDD_PG 44

VGPU_CORE

PC37 *47P/50V/NPO_4

8812VSNS

PR46 100/F_4

PR50 0_4

GPUCORE_VCCSENSE 15

PC39 *47P/50V/NPO_4

8812RGND

PR51 0_4

GPUCORE_VSSSENSE 15

PC41 *47P/50V/NPO_4

PR53 100/F_4

PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	GFX_CORE (RT8812A)	

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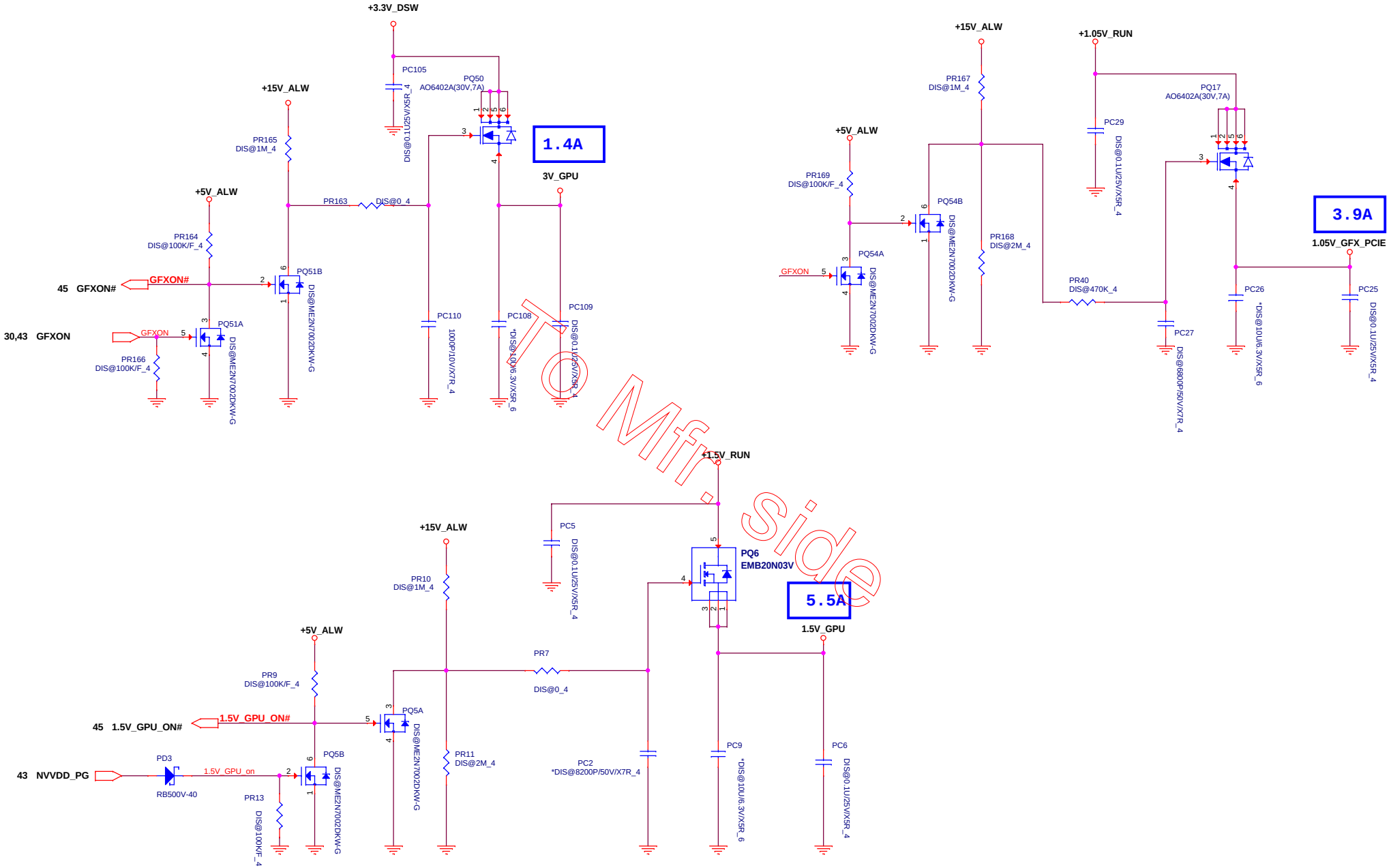
12,14,28,29,35,36,37,38,39,41,42,43 +5V_ALW
36,41 +15V_ALW
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42 +3.3V_RUN
4,6,8,12,23,24,27,29,31,35,36,41 +3.3V_DSW
6,9,12,33,34,38,40,42 +1.05V_RUN



PROJECT : ST6A
Quanta Computer Inc.

Size	Document Number	Rev
	DIS_Load Switch	1A
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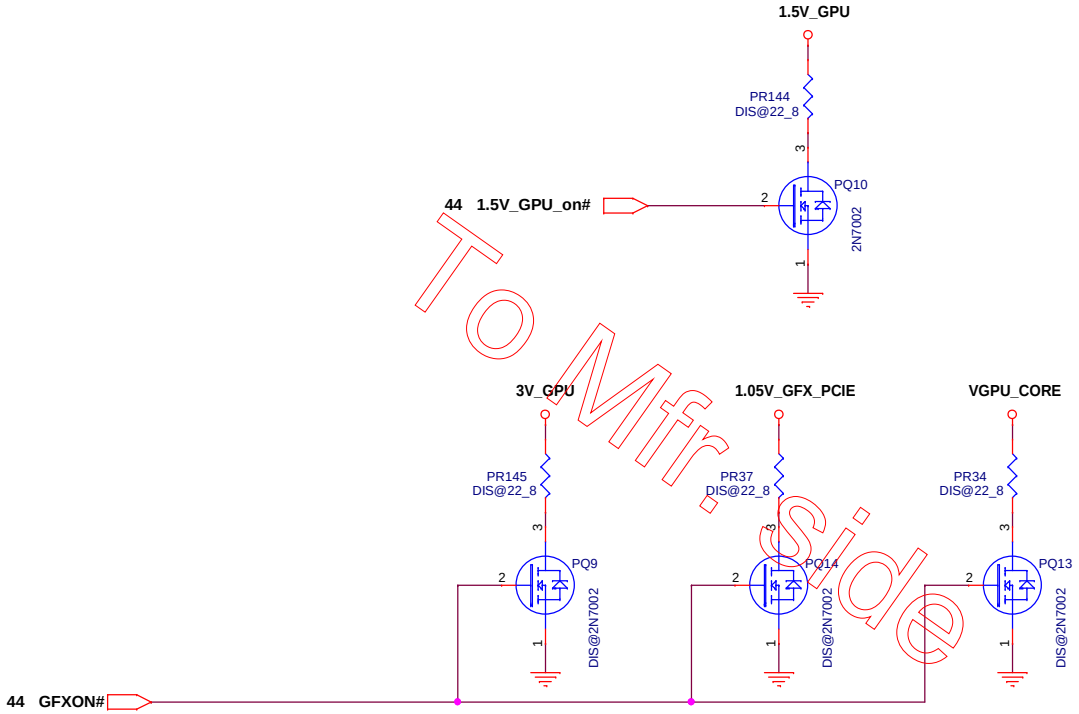
DISCHARGE

12,14,28,29,35,36,37,38,39,41,42,43,44	+5V_ALW
2,4,6,7,8,12,14,15,20,21,22,23,24,26,27,29,30,31,32,34,35,40,41,42	+3.3V_RUN
12,23,27,34,39,42,44	+1.5V_RUN
6,9,12,33,34,38,40,42,44	+1.05V_RUN
14,37,42	+0.675V_DDR_VTT
9,14,37,42	+V_VDDQ_VR
24,33,42	LANVCC
36,41,44	+15V_ALW



PROJECT : ST6A

Quanta Computer Inc.

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	Discharge	

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2013

SDV~SIV

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	21	02/07		Change touch panel VCC control to +3.3V_RUN and stuff R17
EC-A-02	21	02/07		Add +3.3V_RUN to provide LCD panel EDID VCC and stuff R22
EC-A-03	20	02/08	C147	depop C147 from vendor request
EC-A-04	29,31	02/22	U10,C466	remove U10,C466 for lid change to sensor B
EC-A-05	29,31	03/05		sensor hub remove and reserve light sensor for I2C interface
EC-A-06	29	03/05	R528,R528	add R527,R528 to avoid stub
EC-A-07	7	03/05		CLKREQ change
EC-A-08	24	03/05		lan surge solution change
EC-A-09	21	03/06		RTD2132R support initial PWM to product LCDVCC
EC-A-10	21	03/06	R502,R504,R506,R509 R510,R511,R512,R513	change value to meet design guide
EC-A-11	29	03/13	R107	change to 21.5K for charger limit setting
EC-A-12	15	03/15		Q10 pin2 change to GFXPG control
EC-A-13	20	03/11	U24	depop
EC-A-14	12	03/12		change to +5V_ALW
EC-A-15	21	03/12	CN4	Change to 10 pin conn.
EC-A-16	29	03/18	CML2,CML3,CML4,CML6 R85,R90,R96,R101,R118,R119,R521,R522	CML2,CML3,CML4,CML6 pop for EMI suggestion R85,R90,R96,R101,R118,R119,R521,R522 depop for EMI suggestion
EC-A-17	22	03/18	R264,R265,R266,R267	R264,R265,R266,R267 pop for EMI suggestion
EC-A-18	34	03/18	C160,C257,C334,C357 and C459	C160,C257,C334,C357 and C459 pop for EMI suggestion
EC-A-19	30	03/19		KB_LOCK_BTN# pull up to +3.3V_ALW2
EC-A-20	21	03/19	R20,R21,CML7	delete R20,R21 and add CML7
EC-A-21	21	03/22	U39,R535,C529	reserve to meet LCD off sequence

PROJECT : ST6A

Quanta Computer Inc.

Size	Document Number	Rev
	EC list-1	

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