LCFC Confidential

BE560 Rev1.0 Schematic

Intel SkyLake Processor with DDRIIIL + PCH-LP

AMD Litho XT GDDR5 2GB

2015-07-28 Rev1.0

Security Classification	LC Future Center Secret Data		
Issued Date	2013/11/04	Deciphered Date	2014/09/07

Title: COVER PAGE

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Custom	BE560	0.1

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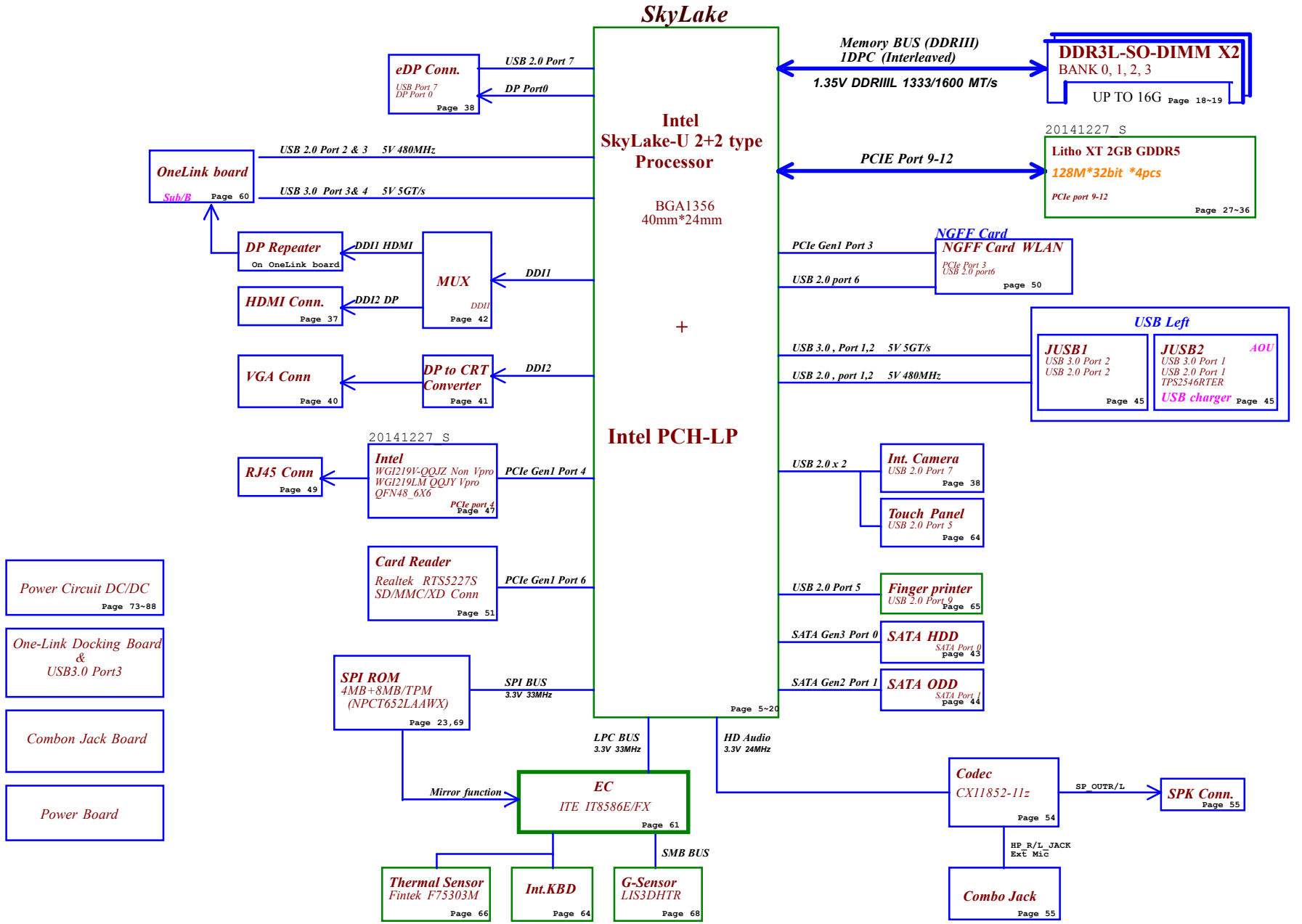

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Title: BLOCK DIAGRAM

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A2	BE560	0.1

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW +1.8VALW +1VALW	+1.35V	+5VS +3VS +VCC_CORE +VCC_IO +VCC_SA +VCC_ST +VCC_STG +VGA_CORE +3VS_VGA +1.8VS_VGA +1.35VS_VGA +0.675VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_A#	SLP_S3#	SLP_S4#	SLP_S5#	EC_ON2	EC_ON	SUSP#
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	ON	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	ON	OFF

SMBUS Control Table

	SOURCE	Main VGA	BATT	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	CP Module	Security ROM	LAN PHY	G sensor
EC_SMB_CK1 EC_SMB_DA1	IT8580F +3VL	X	V +3VALW	X	X	X	X	X	X	X	X
EC_SMB_CK3 EC_SMB_DA3	IT8580F +3VS	V +3VS_VGA	X	X	X	V +3VS	V +3V_PCH	X	X	X	V +3VALW_GS
PCH_SMB_CLK PCH_SMB_DATA	PCH +3V_PCH	X	X	V +3VS	X	X	X	V +5VS	V +3VS	X	X
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	X	X	X	X	X	X	X	V +3VALW	X

USB2 Port

Port	Device
1	JUSB2
2	JUSB3
3	Sub Board
4	Docking
5	Touch Panel
6	BT
7	CMOS
8	FP/Smart

USB3 Port

Port	Device
1	JUSB2
2	JUSB3
3	Sub Board
4	Docking
5	3D CCD(PCIE1)

PCIE Port

Port	Device
1	3D CCD(USB3)
2	X
3	WLAN
4	LAN
5	X
6	CardReader
7	X
8	X
9	GPU
10	GPU
11	GPU
12	GPU

SATA Port

Port	Device
1	HDD
2	ODD
3	X
4	X

Title: NOTE LIST

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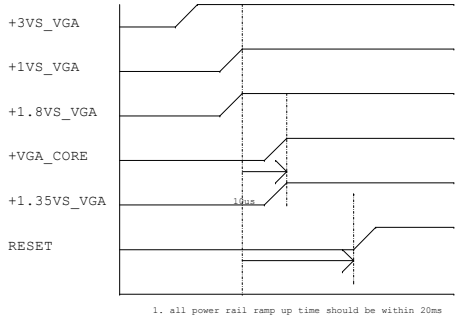
VGA and DDR3 Voltage Rails (Litho XT 2GB DDR3)

20141227_S

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	N/A	
GPIO5	IN	-	GPIO5_AC_BATT
GPIO6	IN	-	GPIO6
GPIO7	OUT	N/A	
GPIO8	OUT	-	GPIO8_ROMSO
GPIO9	OUT	-	GPIO9_ROMSI
GPIO10	OUT	-	GPIO10_ROMSCK
GPIO11	OUT	N/A	
GPIO12	OUT	N/A	
GPIO13	OUT	N/A	
GPIO15	IN	N/A	SVI2_SVD
GPIO16	OUT	N/A	
GPIO17	OUT	N/A	
GPIO19	OUT	N/A	GPIO19_CTF
GPIO20	IN	IN	GPIO20
GPIO21	OUT	N/A	
GPIO22	OUT	N/A	GPIO22_ROMCSB
GPIO29	OUT	N/A	
GPIO30	OUT	N/A	



1. all power rail ramp up time should be within 20ms

	Device ID
JET-XT	0xFFFF

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0xFF
	1	0xFF

BOM Structure Table

BOM Structure	NOTE
PCB@	For PCB load BOM
XDP@	Debug port
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
DIMM2@	For DIMM2 function
DIMM1@	For DIMM1 function
VPRO@	For VPRO function
ME@	ME Connector
EMC@	For EMC function
EMC_2D@	For EMC function
EMC_NS@	For EMC function
RF_NS@	For RF function
S2G@	For VRAM Strap
CHA@	For VRAMA function
CHB@	For VRAMB function
RANKA@	GPU DDR5 Setting
X76@	GPU VRAM Setting
3DCCD@	3D Camera Setting
VGA@	VGA Setting
MUX@	MUX Setting
ODD@	ODD Setting
TPM@	Trusted Platform Module (TPM)
NVPRO@	For Non-VPRO function
MIRROR@	For mirror function

GPU		Litho XT 2GB DDR3	
FB Memory (DDR3L)		PS_3 (RV114)	PS_3 (RV117)
Samsung 1000MHz	K4W4G1646D-BC1A		
	256Mx16	PH 3.4K	PD 10K
Hynix 1000MHz	H5TC4G63AFR-11C		
	256Mx16	PH 4.75K	NC
Micro 1000MHz	MT41J256M16HA-093G		
	256Mx16	PH 3.24K	PD 5.62K

vinafix

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Title: VGA NOTE

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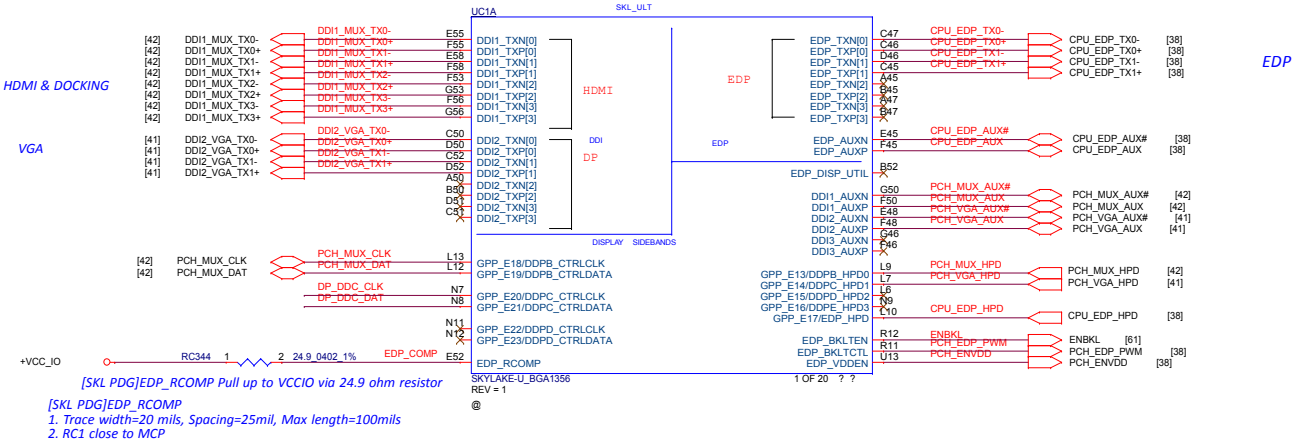
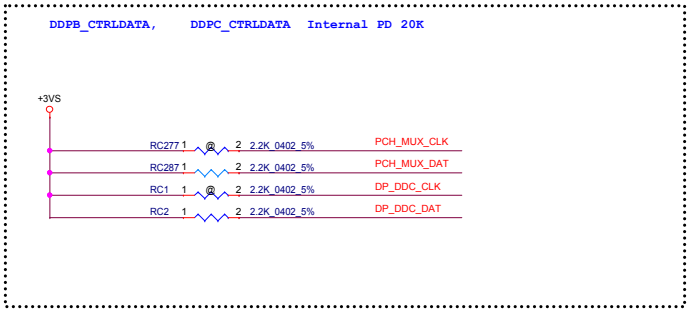
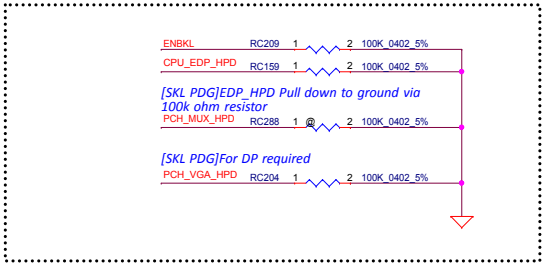




DDPB_CTRLDATA	Port B Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port B will be detected.
DDPC_CTRLDATA	Port C Detected	This signal has an integrated weak pull-down (20 KΩ nominal) resistor. When this signal is pulled up to VCC3_3 through a 1-3.6 KΩ ±5% resistor at the rising edge of PCH_PPWROK the Digital Display Port C will be detected.



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Title: SKL(1/16):DDI/EDP

Size	Document Number	Rev
Custom	BE560	0.1

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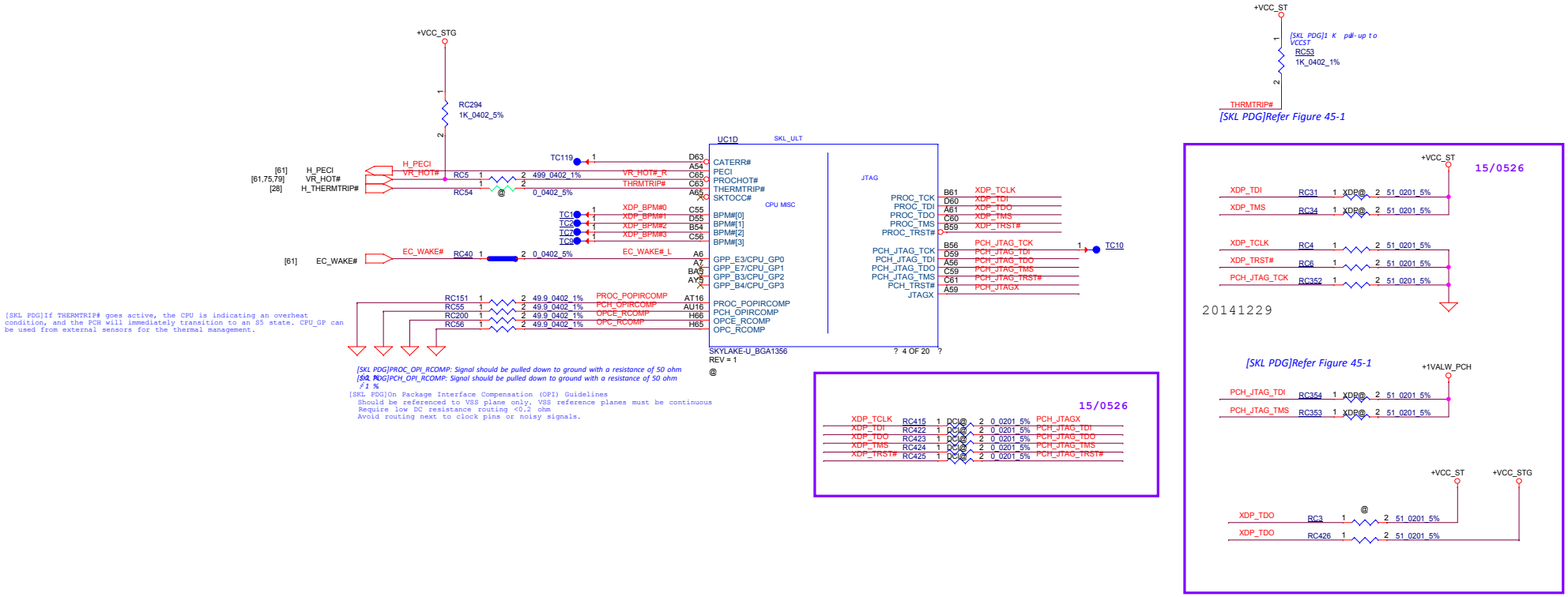

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Title: SKL(2/16):MISC/JTAG

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

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[25] DDR_A_D[0..63]
[25] DDR_A_DQS#[0..7]
[25] DDR_A_DQS[0..7]
[25] DDR_A_MA[0..15]

UC1B

SKL_ULT

DDR_A_D0 AL71
DDR_A_D1 AL68
DDR_A_D2 AN68
DDR_A_D3 AN69
DDR_A_D4 AL70
DDR_A_D5 AL69
DDR_A_D6 AN70
DDR_A_D7 AN71
DDR_A_D8 AR70
DDR_A_D9 AR68
DDR_A_D10 AU71
DDR_A_D11 AU68
DDR_A_D12 AR71
DDR_A_D13 AR69
DDR_A_D14 AU70
DDR_A_D15 AU69
DDR_A_D16 BB65
DDR_A_D17 AW65
DDR_A_D18 AW63
DDR_A_D19 AY63
DDR_A_D20 BA65
DDR_A_D21 AY65
DDR_A_D22 BA63
DDR_A_D23 BB63
DDR_A_D24 BA61
DDR_A_D25 AW61
DDR_A_D26 BB59
DDR_A_D27 AW59
DDR_A_D28 BB61
DDR_A_D29 AY61
DDR_A_D30 BA59
DDR_A_D31 AY59
DDR_A_D32 AY39
DDR_A_D33 AW39
DDR_A_D34 AY37
DDR_A_D35 AW37
DDR_A_D36 BB39
DDR_A_D37 BA39
DDR_A_D38 BA37
DDR_A_D39 BB37
DDR_A_D40 AY35
DDR_A_D41 AW35
DDR_A_D42 AY33
DDR_A_D43 AW33
DDR_A_D44 BB35
DDR_A_D45 BA35
DDR_A_D46 BA33
DDR_A_D47 BB33
DDR_A_D48 AY31
DDR_A_D49 AW31
DDR_A_D50 AY29
DDR_A_D51 AW29
DDR_A_D52 BB31
DDR_A_D53 BA31
DDR_A_D54 BA29
DDR_A_D55 BB29
DDR_A_D56 AY27
DDR_A_D57 AW27
DDR_A_D58 AY25
DDR_A_D59 AW25
DDR_A_D60 BB27
DDR_A_D61 BA27
DDR_A_D62 BA25
DDR_A_D63 BB25

DDR0_DQ[0]
DDR0_DQ[1]
DDR0_DQ[2]
DDR0_DQ[3]
DDR0_DQ[4]
DDR0_DQ[5]
DDR0_DQ[6]
DDR0_DQ[7]
DDR0_DQ[8]
DDR0_DQ[9]
DDR0_DQ[10]
DDR0_DQ[11]
DDR0_DQ[12]
DDR0_DQ[13]
DDR0_DQ[14]
DDR0_DQ[15]
DDR0_DQ[16]/DDR0_DQ[32]
DDR0_DQ[17]/DDR0_DQ[33]
DDR0_DQ[18]/DDR0_DQ[34]
DDR0_DQ[19]/DDR0_DQ[35]
DDR0_DQ[20]/DDR0_DQ[36]
DDR0_DQ[21]/DDR0_DQ[37]
DDR0_DQ[22]/DDR0_DQ[38]
DDR0_DQ[23]/DDR0_DQ[39]
DDR0_DQ[24]/DDR0_DQ[40]
DDR0_DQ[25]/DDR0_DQ[41]
DDR0_DQ[26]/DDR0_DQ[42]
DDR0_DQ[27]/DDR0_DQ[43]
DDR0_DQ[28]/DDR0_DQ[44]
DDR0_DQ[29]/DDR0_DQ[45]
DDR0_DQ[30]/DDR0_DQ[46]
DDR0_DQ[31]/DDR0_DQ[47]
DDR0_DQ[32]/DDR1_DQ[0]
DDR0_DQ[33]/DDR1_DQ[1]
DDR0_DQ[34]/DDR1_DQ[2]
DDR0_DQ[35]/DDR1_DQ[3]
DDR0_DQ[36]/DDR1_DQ[4]
DDR0_DQ[37]/DDR1_DQ[5]
DDR0_DQ[38]/DDR1_DQ[6]
DDR0_DQ[39]/DDR1_DQ[7]
DDR0_DQ[40]/DDR1_DQ[8]
DDR0_DQ[41]/DDR1_DQ[9]
DDR0_DQ[42]/DDR1_DQ[10]
DDR0_DQ[43]/DDR1_DQ[11]
DDR0_DQ[44]/DDR1_DQ[12]
DDR0_DQ[45]/DDR1_DQ[13]
DDR0_DQ[46]/DDR1_DQ[14]
DDR0_DQ[47]/DDR1_DQ[15]
DDR0_DQ[48]/DDR1_DQ[32]
DDR0_DQ[49]/DDR1_DQ[33]
DDR0_DQ[50]/DDR1_DQ[34]
DDR0_DQ[51]/DDR1_DQ[35]
DDR0_DQ[52]/DDR1_DQ[36]
DDR0_DQ[53]/DDR1_DQ[37]
DDR0_DQ[54]/DDR1_DQ[38]
DDR0_DQ[55]/DDR1_DQ[39]
DDR0_DQ[56]/DDR1_DQ[40]
DDR0_DQ[57]/DDR1_DQ[41]
DDR0_DQ[58]/DDR1_DQ[42]
DDR0_DQ[59]/DDR1_DQ[43]
DDR0_DQ[60]/DDR1_DQ[44]
DDR0_DQ[61]/DDR1_DQ[45]
DDR0_DQ[62]/DDR1_DQ[46]
DDR0_DQ[63]/DDR1_DQ[47]

DDR0_CKN[0] AU53 SA_CLK_DDR#0 → SA_CLK_DDR#0 [25]
DDR0_CKP[0] AT53 SA_CLK_DDR0 → SA_CLK_DDR0 [25]
DDR0_CKN[1] AU55 SA_CLK_DDR#1 → SA_CLK_DDR#1 [25]
DDR0_CKP[1] AT55 SA_CLK_DDR1 → SA_CLK_DDR1 [25]

DDR0_CKE[0] BA56 DDRA_CKE0_DIMMA → DDRA_CKE0_DIMMA [25]
DDR0_CKE[1] BB56 DDRA_CKE1_DIMMA → DDRA_CKE1_DIMMA [25]
DDR0_CKE[2] AW56
DDR0_CKE[3] AY56

DDR0_CS#[0] AU45 DDRA_CS0_DIMMA# → DDRA_CS0_DIMMA# [25]
DDR0_CS#[1] AU43 DDRA_CS1_DIMMA# → DDRA_CS1_DIMMA# [25]
DDR0_ODT[0] AT45 DDRA_ODT0_DIMMA# → DDRA_ODT0_DIMMA# [25]
DDR0_ODT[1] AT43 DDRA_ODT1_DIMMA# → DDRA_ODT1_DIMMA# [25]

DDR0_MA[5]/DDR0_CAA[0]/DDR0_MA[5] BA51 DDR_A_MA5
DDR0_MA[9]/DDR0_CAA[1]/DDR0_MA[9] BB54 DDR_A_MA9
DDR0_MA[6]/DDR0_CAA[2]/DDR0_MA[6] BA52 DDR_A_MA6
DDR0_MA[8]/DDR0_CAA[3]/DDR0_MA[8] AY52 DDR_A_MA8
DDR0_MA[7]/DDR0_CAA[4]/DDR0_MA[7] AY55 DDR_A_MA7
DDR0_BA[2]/DDR0_CAA[5]/DDR0_BG[0] AW54 DDR_A_BS2 → DDR_A_BS2 [25]
DDR0_MA[12]/DDR0_CAA[6]/DDR0_MA[12] BA54 DDR_A_MA12
DDR0_MA[11]/DDR0_CAA[7]/DDR0_MA[11] BA55 DDR_A_MA11
DDR0_MA[15]/DDR0_CAA[8]/DDR0_ACT# BA55 DDR_A_MA15
DDR0_MA[14]/DDR0_CAA[9]/DDR0_BG[1] AY54 DDR_A_MA14

DDR0_MA[13]/DDR0_CAB[0]/DDR0_MA[13] AU46 DDR_A_MA13
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15] AU48 DDR_A_CAS# → DDR_A_CAS# [25]
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14] AT46 DDR_A_WE# → DDR_A_WE# [25]
DDR0_RAS#/DDR0_CAB[3]/DDR0_MA[16] AU50 DDR_A_RAS# → DDR_A_RAS# [25]
DDR0_BA[0]/DDR0_CAB[4]/DDR0_BA[0] AU52 DDR_A_BS0 → DDR_A_BS0 [25]
DDR0_MA[2]/DDR0_CAB[5]/DDR0_MA[2] AY51 DDR_A_MA2
DDR0_BA[1]/DDR0_CAB[6]/DDR0_BA[1] AT48 DDR_A_BS1 → DDR_A_BS1 [25]
DDR0_MA[10]/DDR0_CAB[7]/DDR0_MA[10] AT50 DDR_A_MA10
DDR0_MA[1]/DDR0_CAB[8]/DDR0_MA[1] BB50 DDR_A_MA1
DDR0_MA[0]/DDR0_CAB[9]/DDR0_MA[0] AY50 DDR_A_MA0
DDR0_MA[3] BA50 DDR_A_MA3
DDR0_MA[4] BB52 DDR_A_MA4

DDR0_DQSN[0] AM70 DDR_A_DQS#0
DDR0_DQSP[0] AM69 DDR_A_DQS0
DDR0_DQSN[1] AT69 DDR_A_DQS#1
DDR0_DQSP[1] AT70 DDR_A_DQS1
DDR0_DQSN[2]/DDR0_DQSN[4] BA64 DDR_A_DQS#2
DDR0_DQSP[2]/DDR0_DQSP[4] AY64 DDR_A_DQS2
DDR0_DQSN[3]/DDR0_DQSN[5] AY60 DDR_A_DQS#3
DDR0_DQSP[3]/DDR0_DQSP[5] BA60 DDR_A_DQS3
DDR0_DQSN[4]/DDR1_DQSN[0] BA38 DDR_A_DQS#4
DDR0_DQSP[4]/DDR1_DQSP[0] AY38 DDR_A_DQS4
DDR0_DQSN[5]/DDR1_DQSN[1] AY34 DDR_A_DQS#5
DDR0_DQSP[5]/DDR1_DQSP[1] BA34 DDR_A_DQS5
DDR0_DQSN[6]/DDR1_DQSN[4] BA30 DDR_A_DQS#6
DDR0_DQSP[6]/DDR1_DQSP[4] AY30 DDR_A_DQS6
DDR0_DQSN[7]/DDR1_DQSN[5] AY26 DDR_A_DQS#7
DDR0_DQSP[7]/DDR1_DQSP[5] BA26 DDR_A_DQS7

DDR0_ALERT# AW50 → 20141201
DDR0_PAR AT52

DDR_VREF_CA AY67 SM_DIMM_VREFCA → SM_DIMM_VREFCA [25]
DDR0_VREF_DQ AY68 SA_DIMM_VREFDQ → SA_DIMM_VREFDQ [25]
DDR1_VREF_DQ BA67 SB_DIMM_VREFDQ → SB_DIMM_VREFDQ [26]

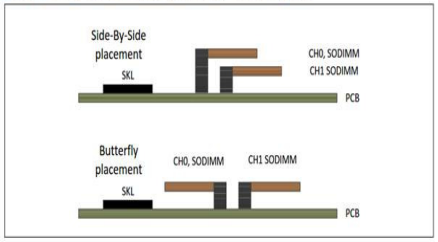
DDR_VTT_CNTL AW67 DDR_PG_CTRL → DDR_PG_CTRL [25]

DDR CH - A

SKYLAKE-U_BGA1356
REV = 1
@

2 OF 20 ?

Figure 4-14. SKL U DDR3L/-RS SODIMM T3/8L 1L Placement Options



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Title: SKL(3/16):DDR3L CH.A

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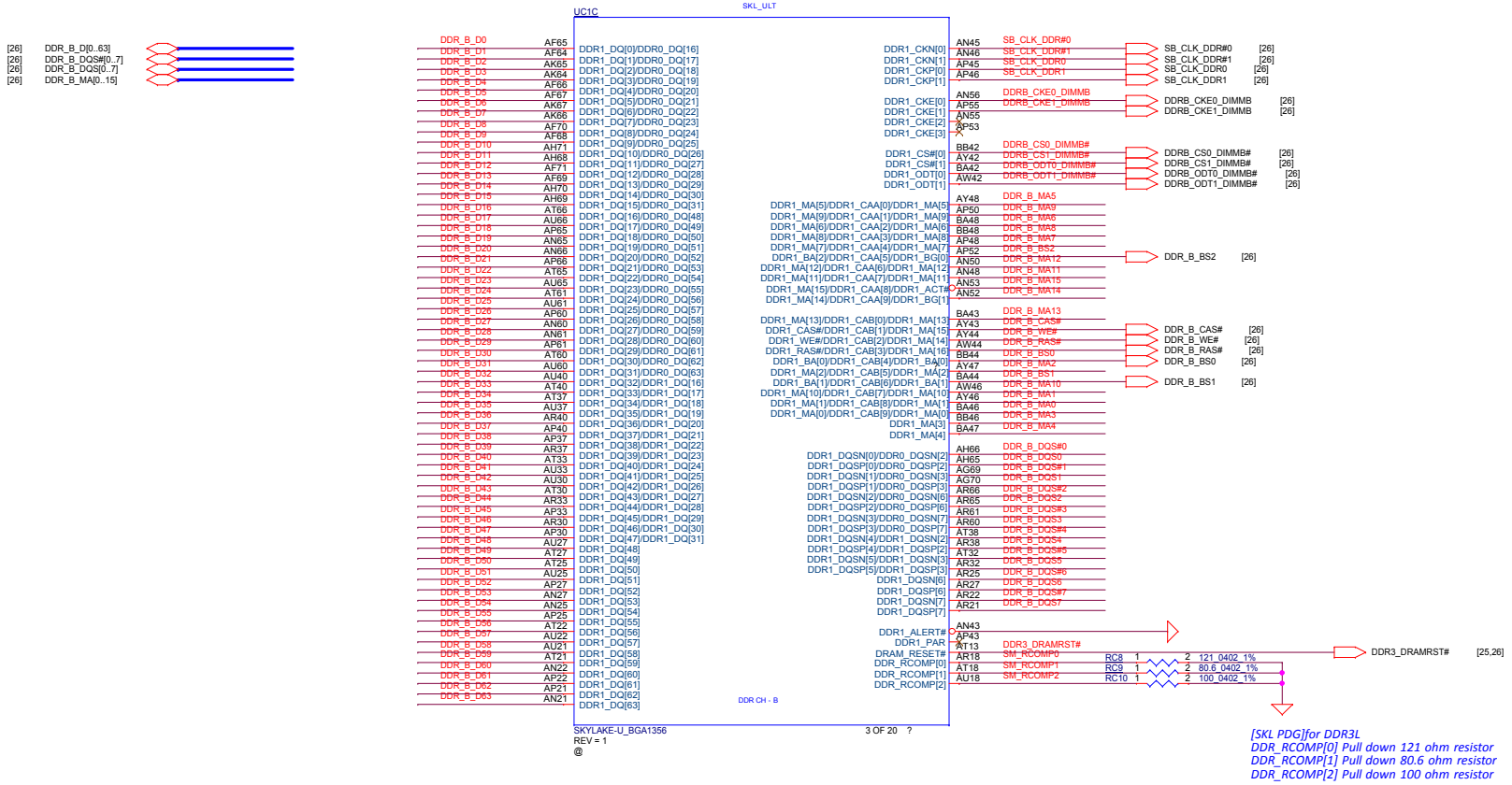

Title: **SKL(4/16):DDR3L CH.B**

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Custom	BE560	0.1

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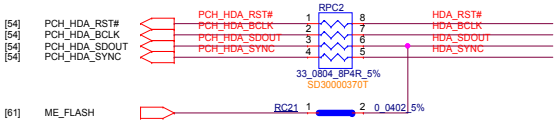
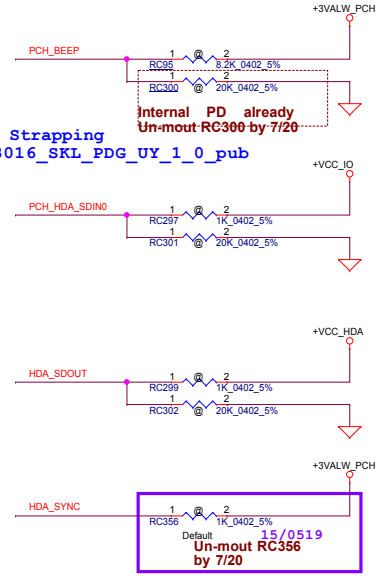
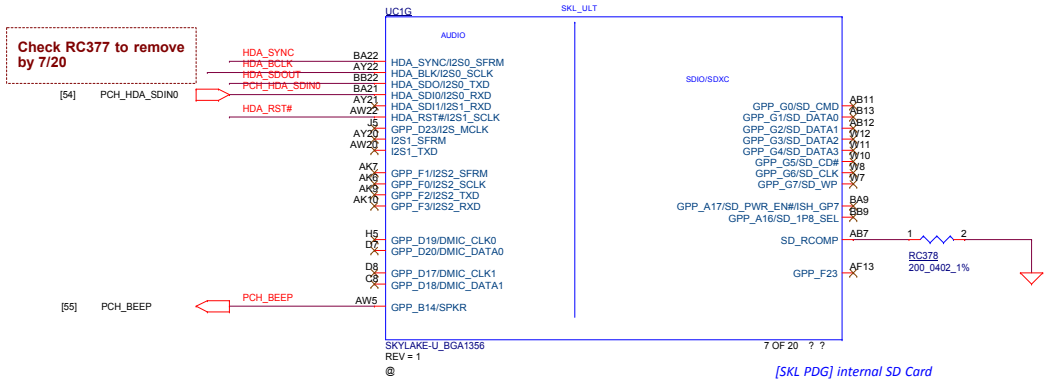
[SKL PDG]Manufacturing Mode Jumper
1. If strap is sampled low, the security measures defined in the flash Descriptor will be in effect (default)
2. If sampled high, the Flash Descriptor Security will be overridden.



GPP_B14, Internal PD 20K
No Reboot on TCO
Timer expiration
pull-up to VCC3_3 through a 18.2K ±5% resistor to disable this capability



Check RC377 to remove by 7/20



[SKL PDG] internal SD Card

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Title: **SKL(5/16):HDA/SDIO**

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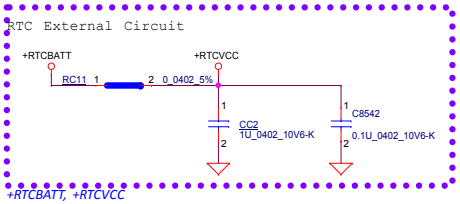
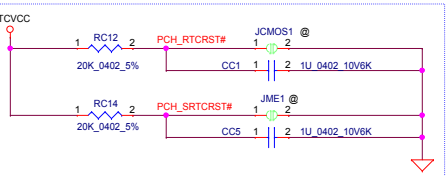
20150514

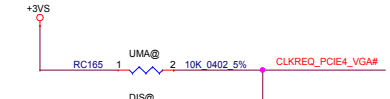
RTC External Circuit

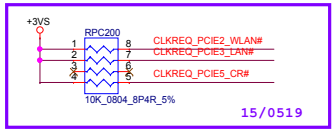


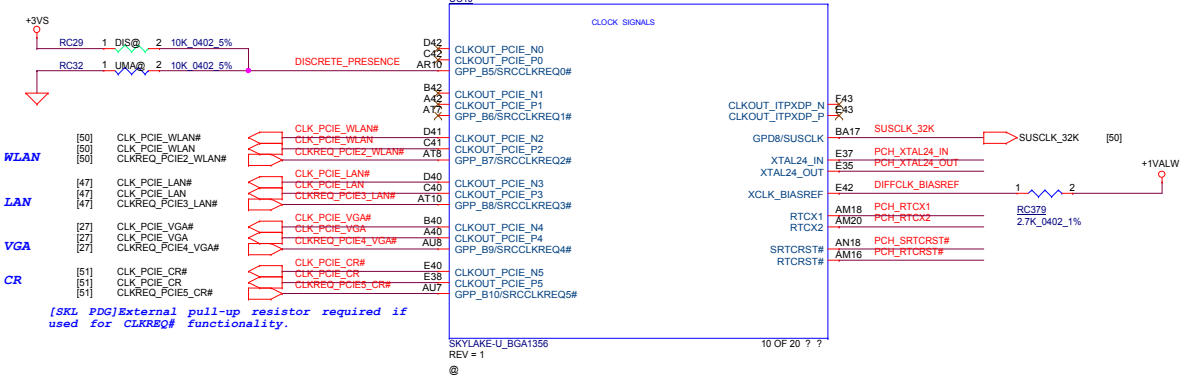
+RTCBATT, +RTCVCC
Trace width = 20mils

JCMOS, JME Setting, Need Under DDR Door





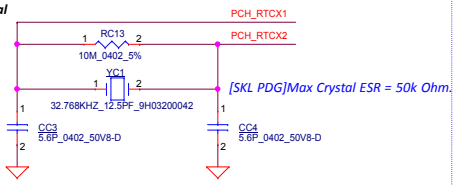




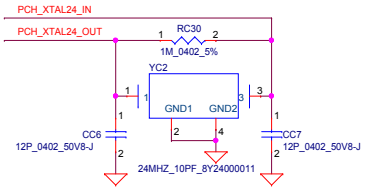
[SKL PDG]Used to set BIAS reference for differential clocks. Connect to a [RC379] 2.71K ∮ 0.5% precision resistor to 1.0v.

[SKL PDG]
1.Space > 15mils
2.No trace under crystal
3.Place on oppsosit side of MCP for temp inf l uence
4.The exact capacitor values forC1 and C2 must be based on the crystal maker recommendat i ons.
Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF.

RTC Crystal



[SKL PDG]
1.A 24 MHz crystal with crystal frequency tolerance and stability of +/-30 ppm
2.Two External Load Capacitors (Ce1 and Ce2)
3.A 1-Mohm bias resistor (Rf)



Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: **SKL(6/16):CLOCK SIGNALS**

Size	Document Number	Rev
Custom	BE560	0.1

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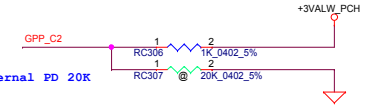
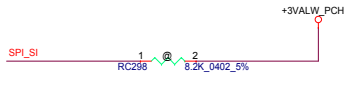
Functional Strap Definitions

L:Disable Intel ME Crypto TLS cipher suite (no confidentiality).
*H:Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).Support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

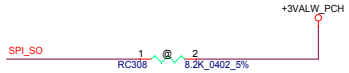


GPP_C2, Internal PD 20K

JTAG ODT

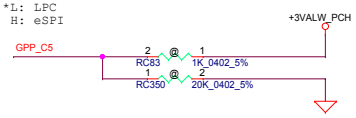


SPI0_MOSI

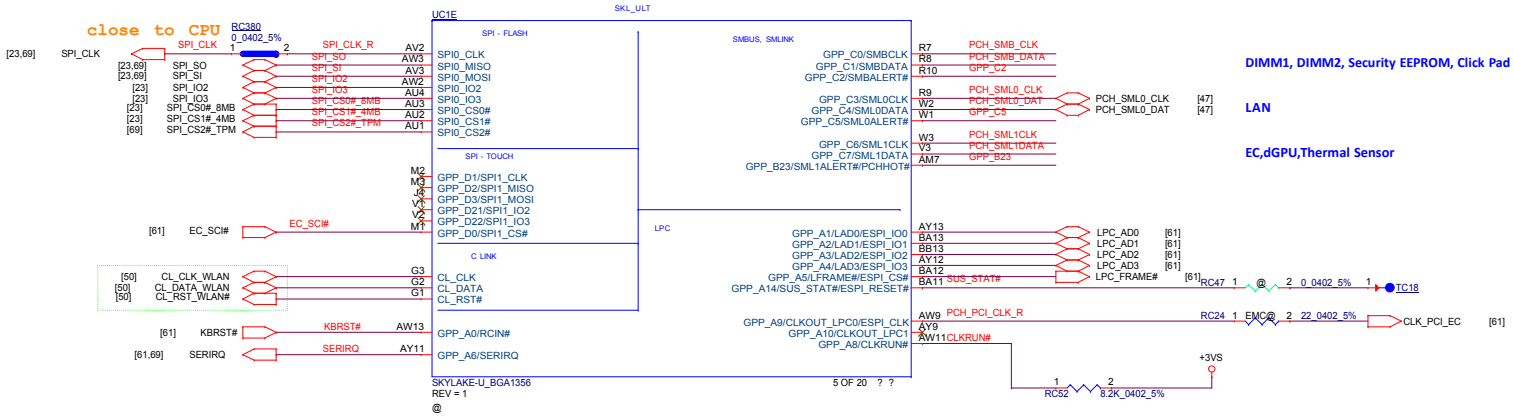


GPP_C5, Internal PD 20K

*L: LPC
H: eSPI



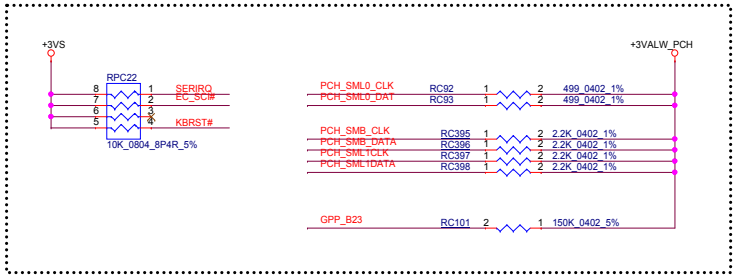
close to CPU RC380 0_0402_5%

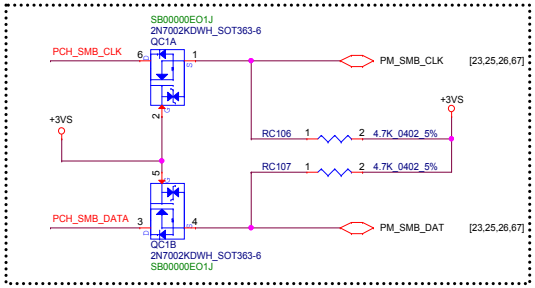


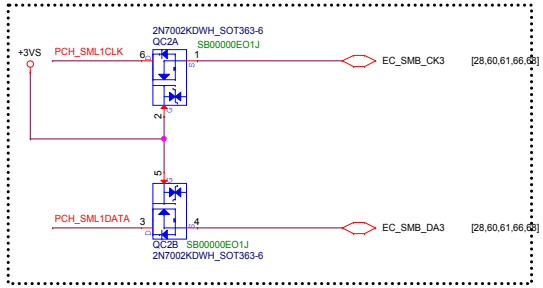
DIMM1, DIMM2, Security EEPROM, Click Pad

LAN

EC,dGPU,Thermal Sensor







Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(7/16):LPC/SPI/SMBUS/CL

Size	Document Number	Rev
Custom	BE560	0.1

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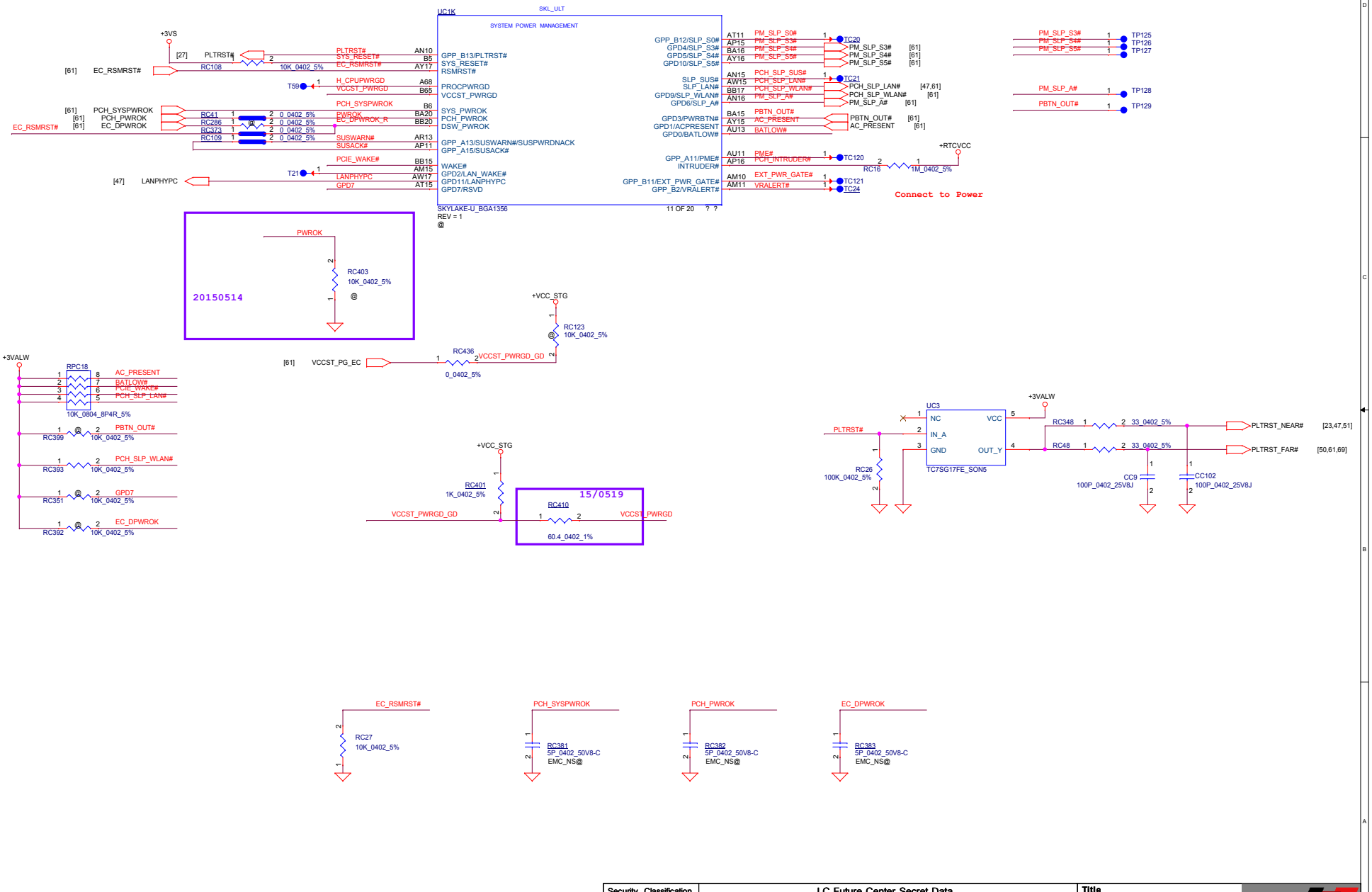

Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

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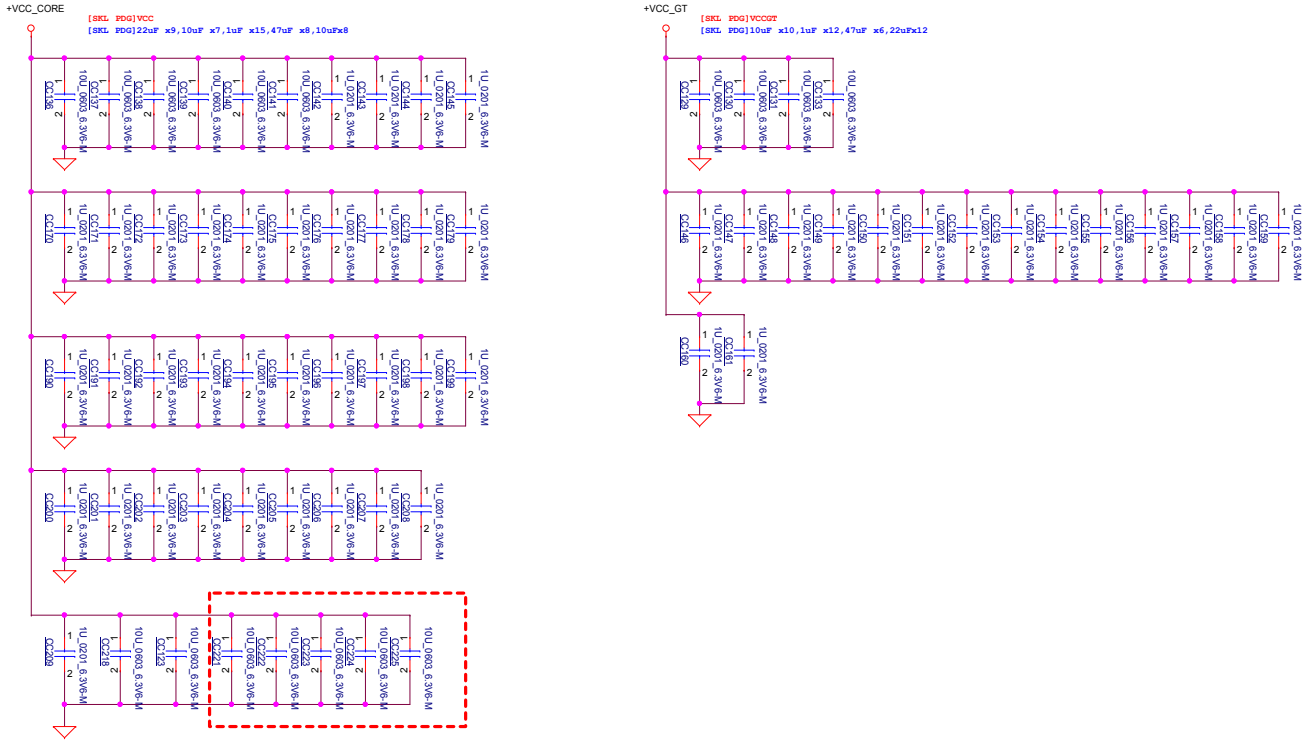
Title: SKL(8/16):SYSTEM PM

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 Sheet 12 of 99

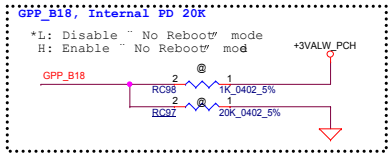


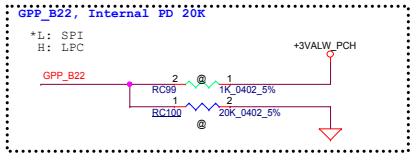
Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

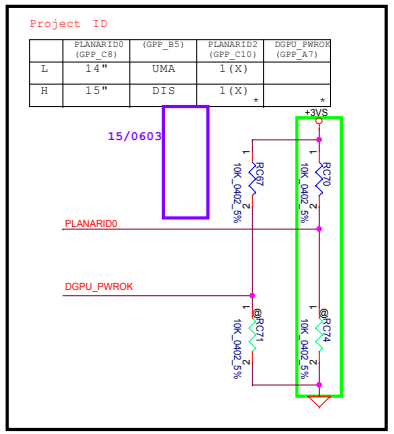
Title: **SKL(9/16):Decoupling**

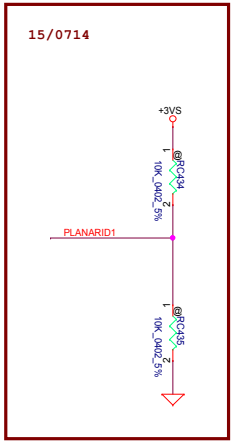
Size	Document Number	Rev
Custom	BE560	0.1

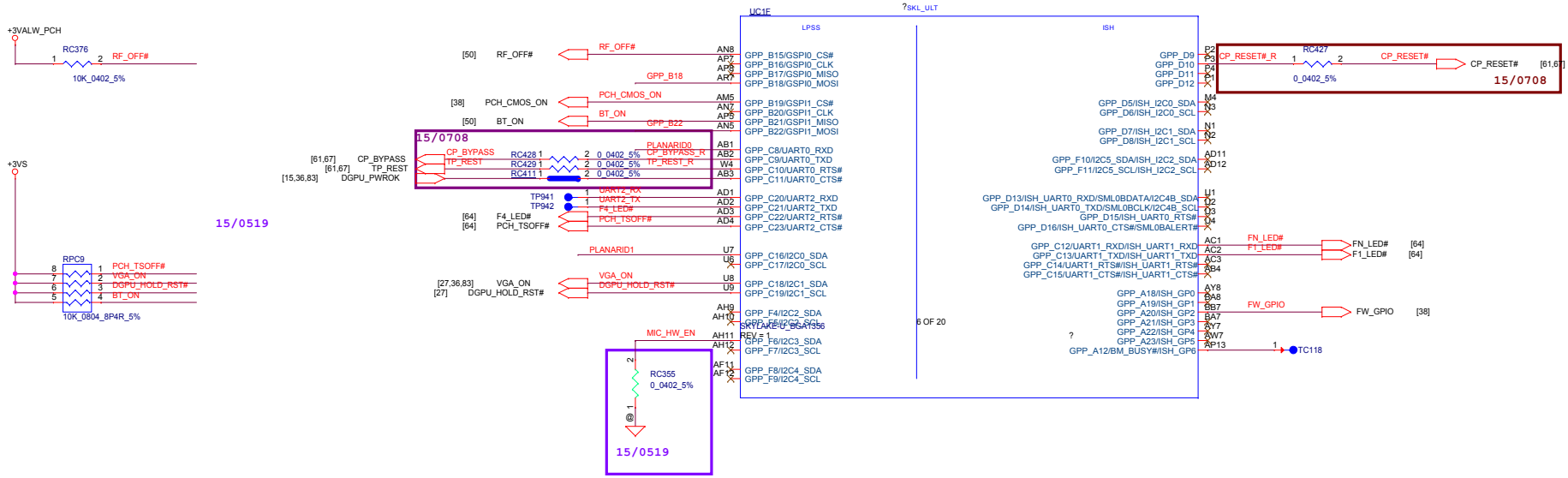
Date: Wednesday, September 23, 2015 | Sheet 13 of 99









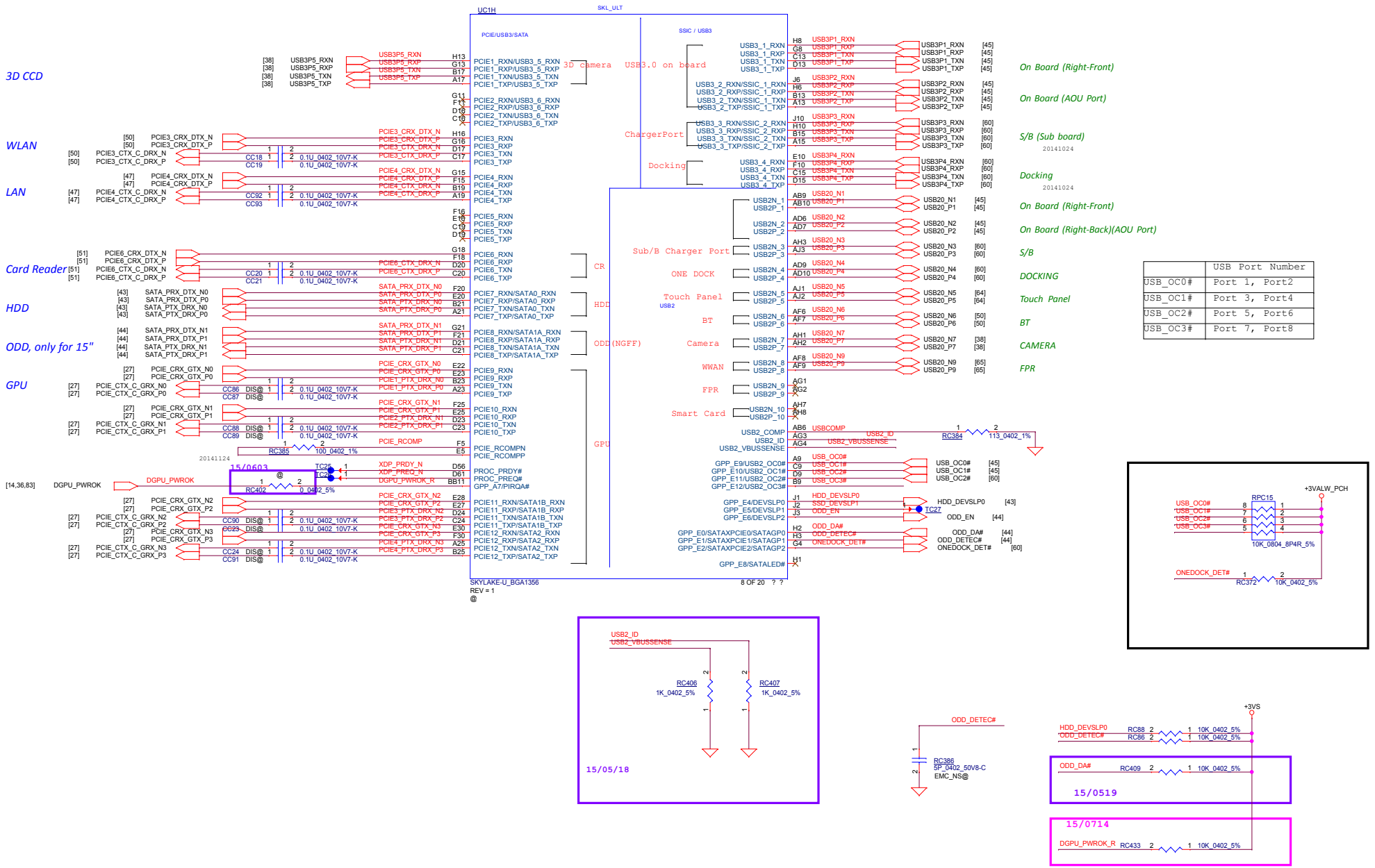


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(10/16):GPIO/CPU/MISC

Size: Custom | Document Number: BE560 | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 14 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(11/16):PCIE/USB/SATA

Size	Document Number	Rev
Custom	BE560	0.1

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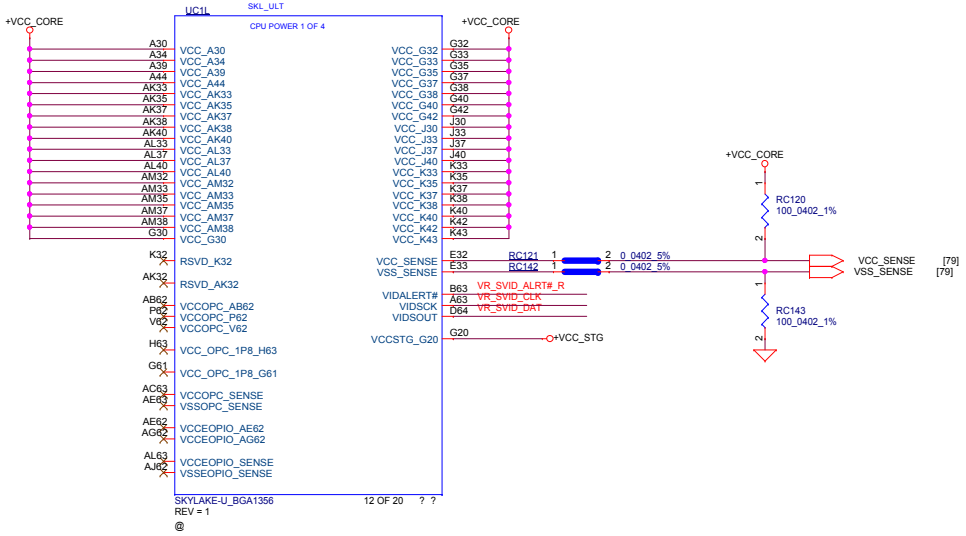
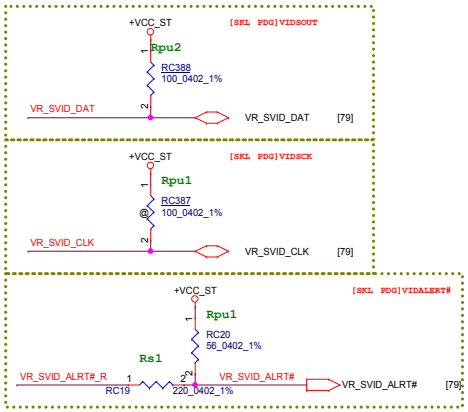
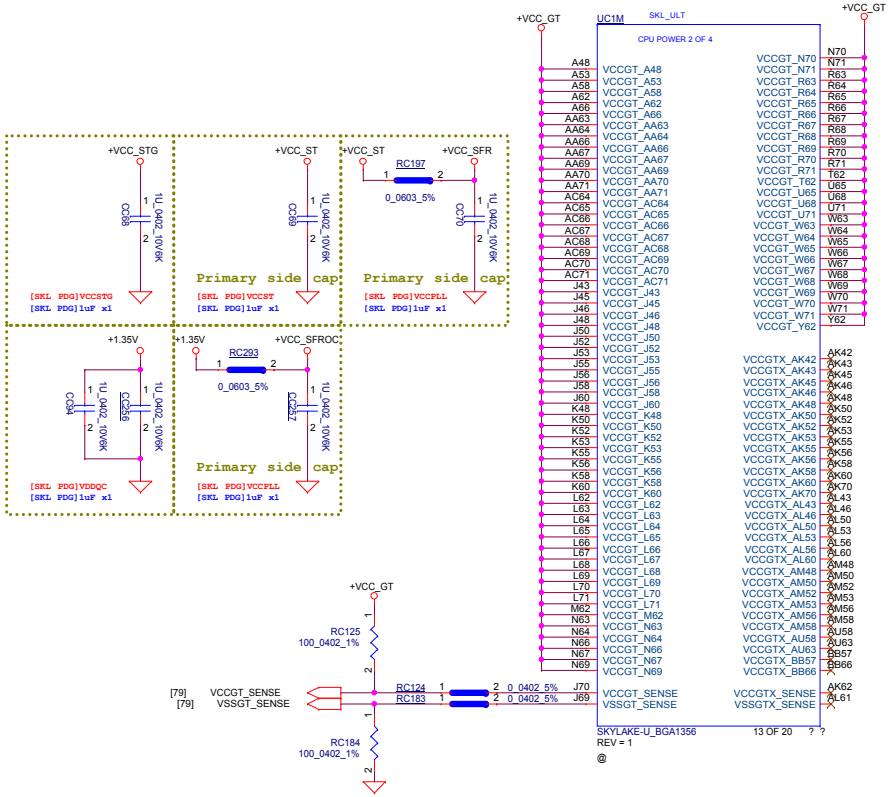
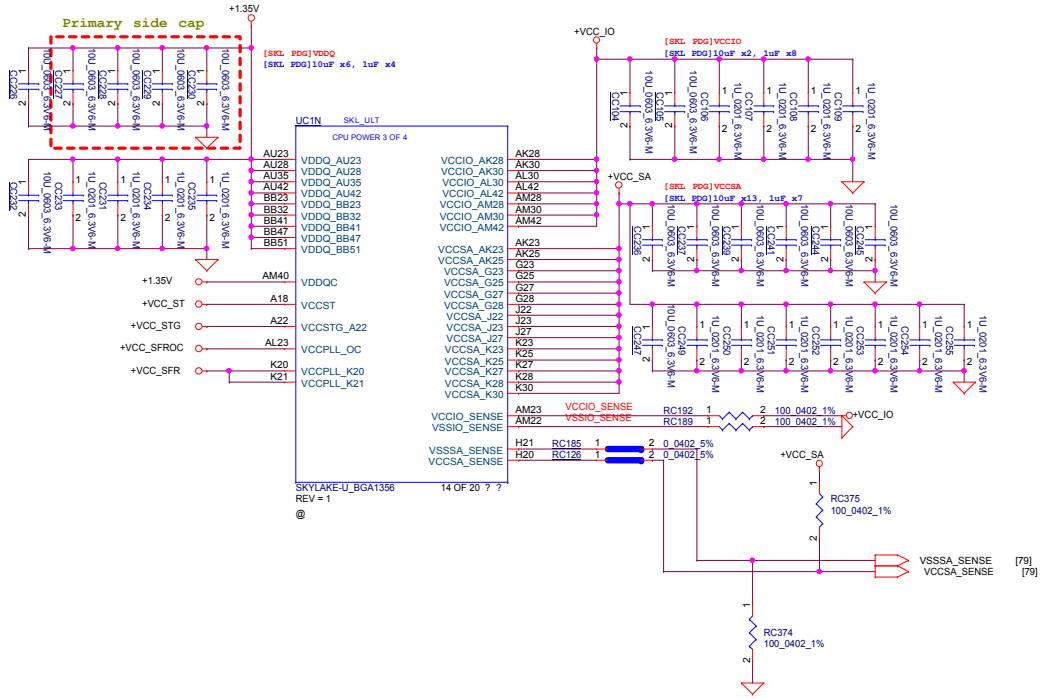
Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{pu1} [Ω]	R_{pu2} [Ω]	R_{s1} [Ω]	R_{s2} [Ω]	VCC_{ST} [V]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	







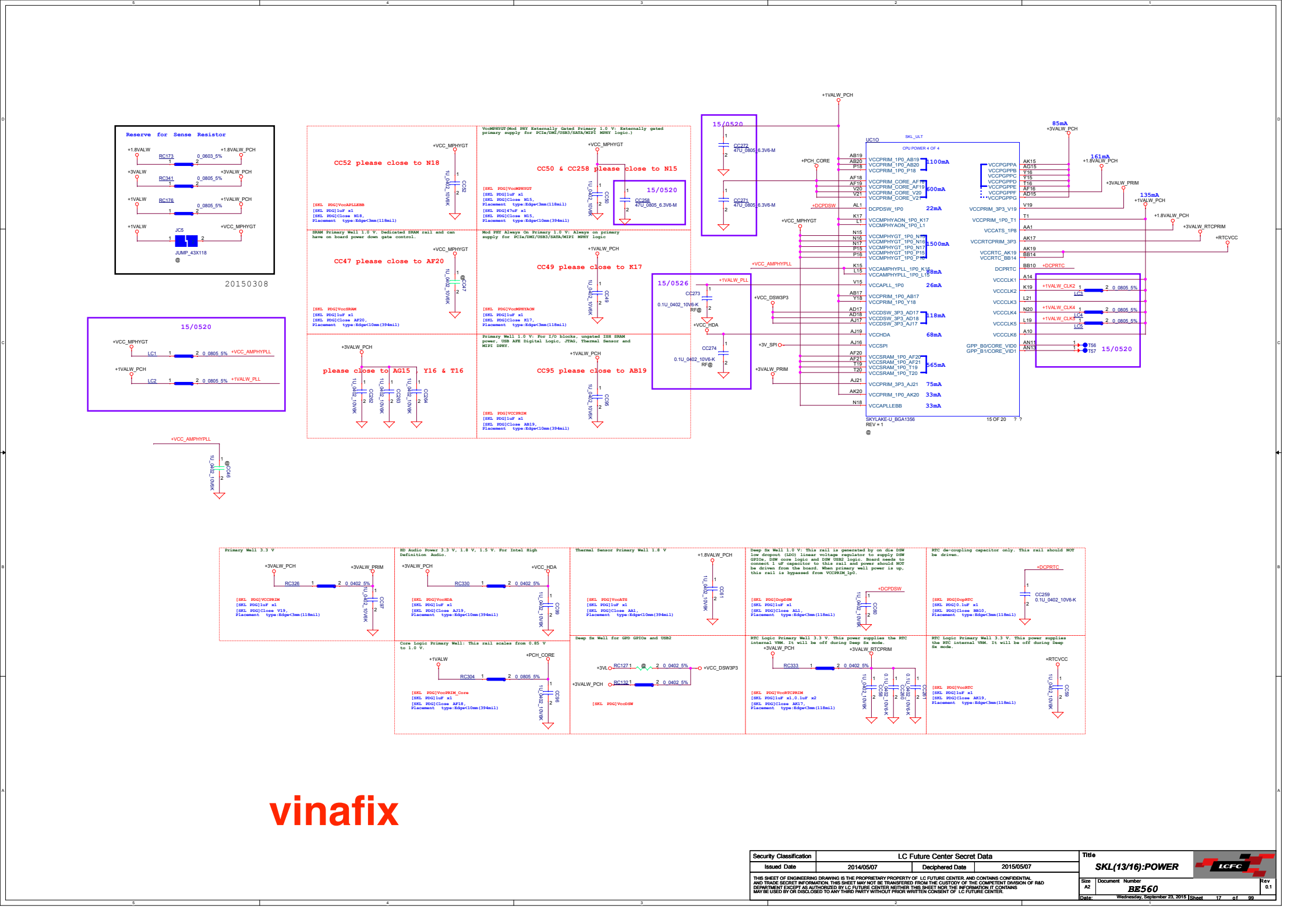


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: **SKL(12/16):POWER**

Size: Custom | Document Number: **BE560** | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 16 of 99

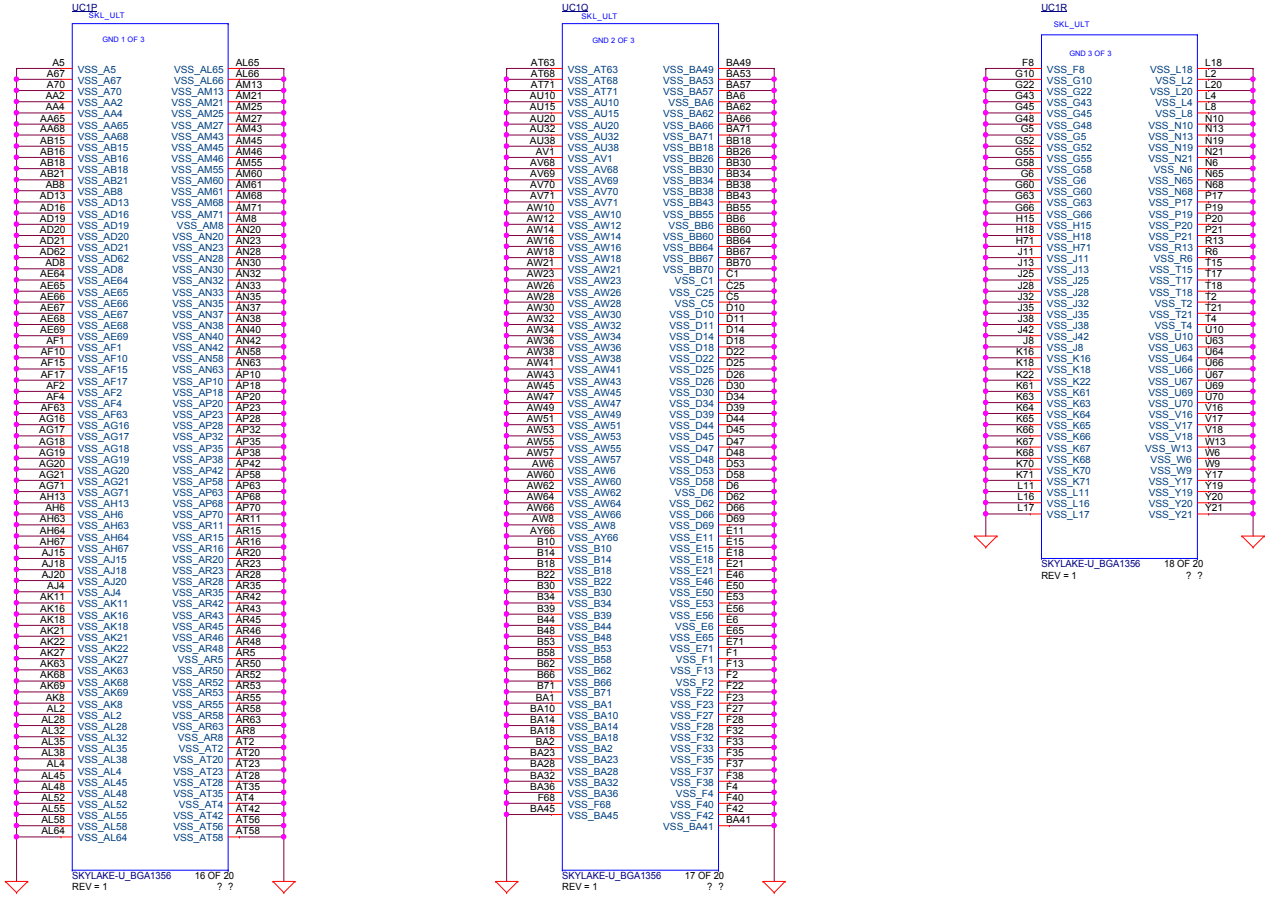


Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: SKL(13/16):POWER

Size: A2 | Document Number: BE5560 | Rev: 0.1

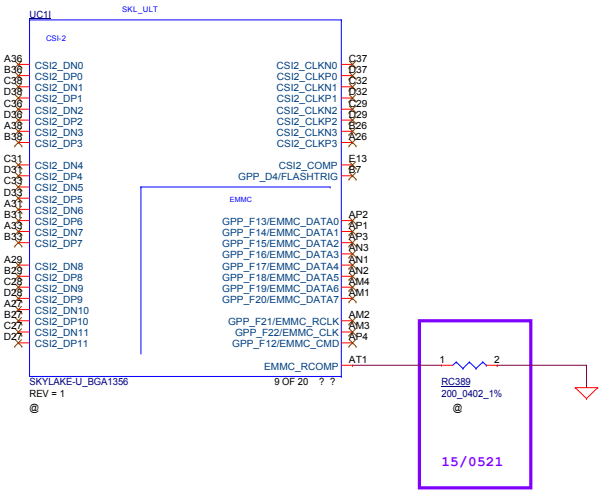
Date: Wednesday, September 23, 2015 | Sheet 17 of 99



Title: **SKL(14/16):GND**

Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 18 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2014/05/07	Deciphered Date	2015/05/07

Title: **SKL(15/16):CSI-2/EMMC**

Size	Document Number	Rev
Custom	BE560	0.1

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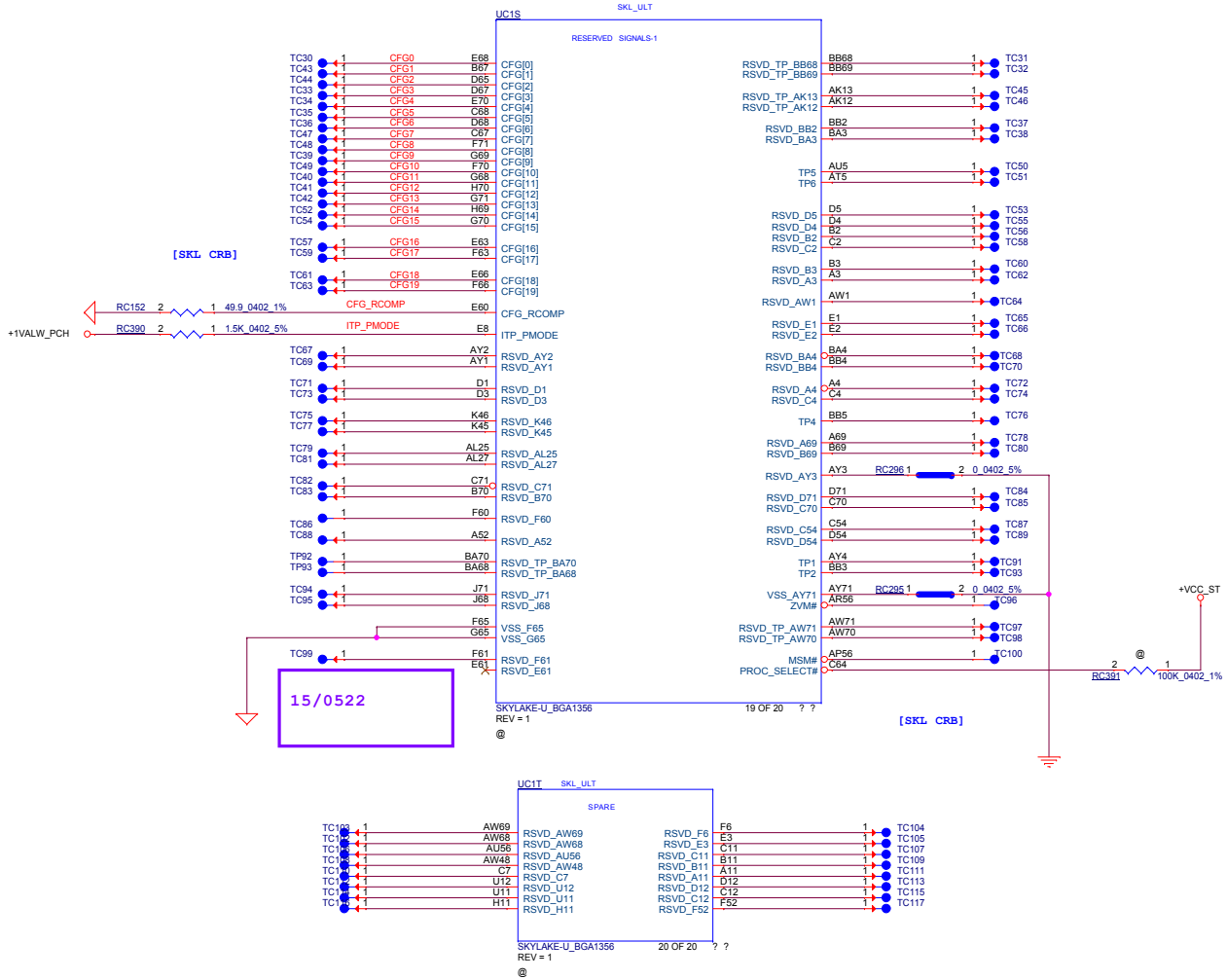

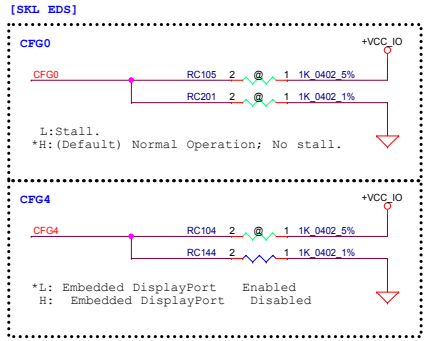

TABLE

CFG0 : Stall Reset Sequence after PCU PLL Lock until de-asserted **1 : No Stall** **0 : Stall**
CFG4 : eDP Enable **1 : Disabled** **0 : Enabled**
CFG9 : SVID Bus Communication **1 : Enabled** **0 : Disabled**

ZVM# state	VCCOPC
0V	0V
1V	1V

ZVM# state	MSM# state	VCCEOPIO
0V	X	0V
1V	0V	0.8V
1V	1V	1V

Title: SKL(16/16):CFG/RESERVED

Size	Document Number	Rev
Custom	BE560	0.1

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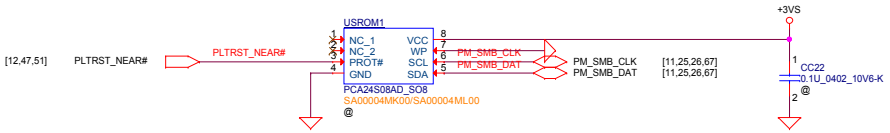
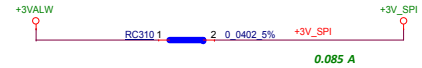
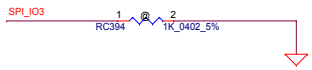
Security ROM



M3 Support + Intel LAN PHY / Wireless LAN Solut i on

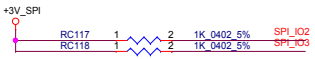


20141220

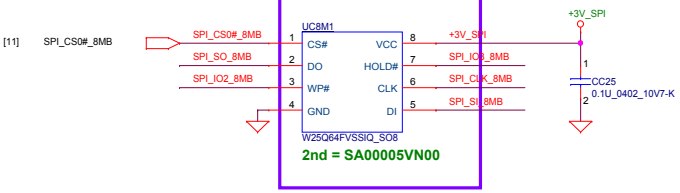


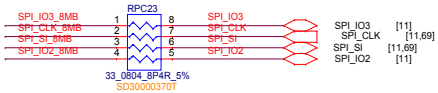
[SKL]SPI0_CS0#: SPI FLASH
SPI0_CS1#: SPI FLASH
SPI0_CS2#: SPI TPM

8MB(64Mb)



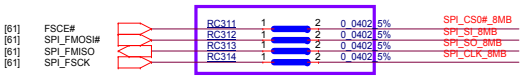
feedback to SDV rev..
15/0522





Near SPI ROM

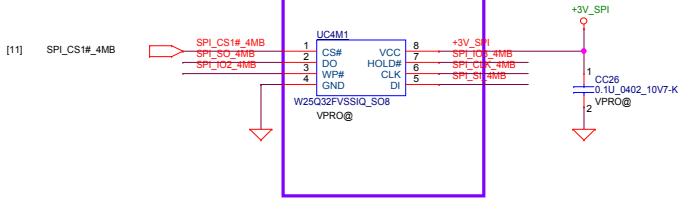
Mirror Code

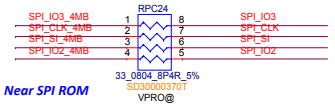


Close to SPI ROM (UC8M1).

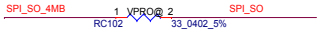
4MB(32Mb) for VPRO SKU

15/0525





Near SPI ROM



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **SPI ROM**

Size	Document Number	Rev
Custom	BE560	0.1

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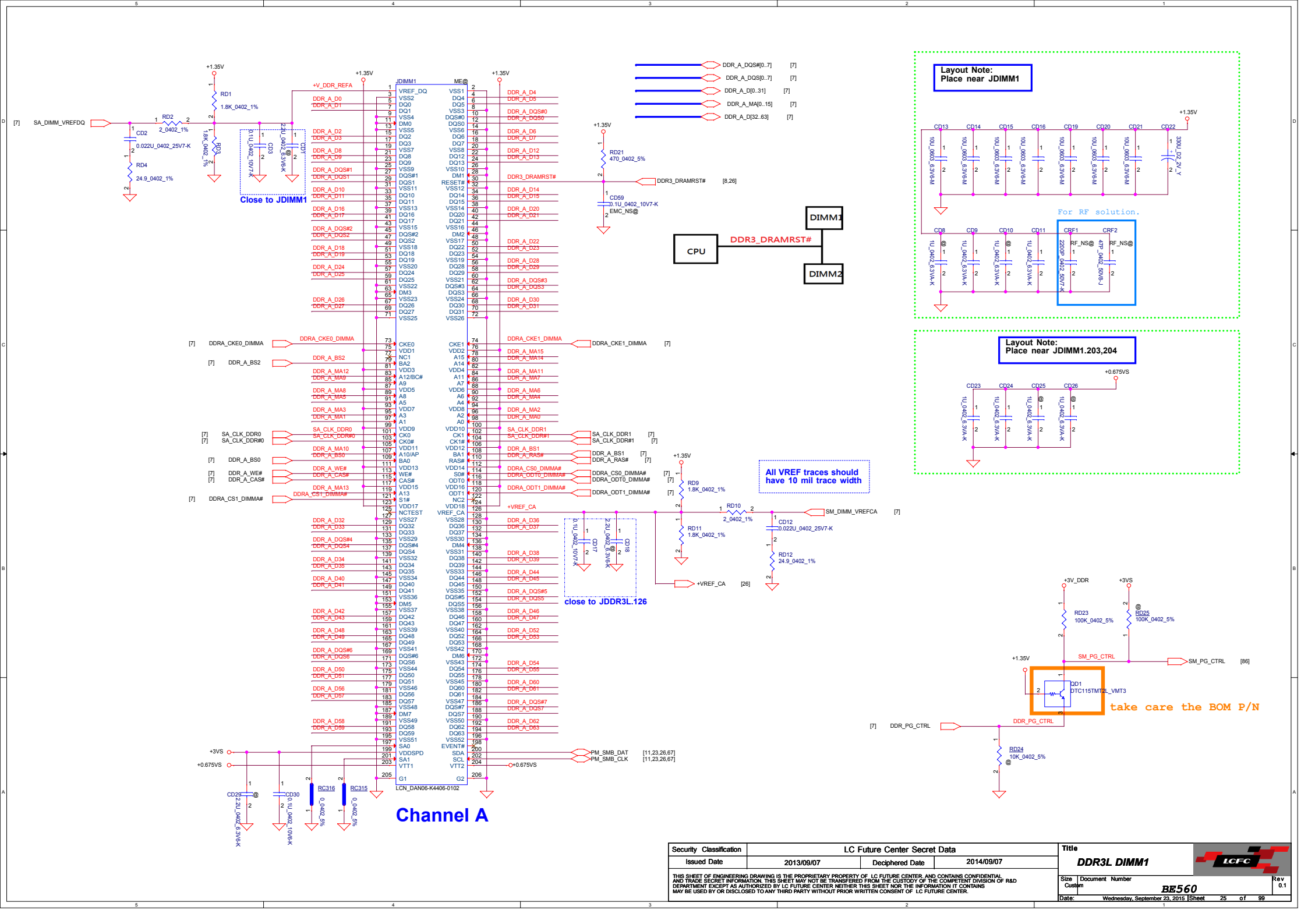

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: DDR3L DIMM1

Size: Custom | Document Number: BE560 | Rev: 0.1

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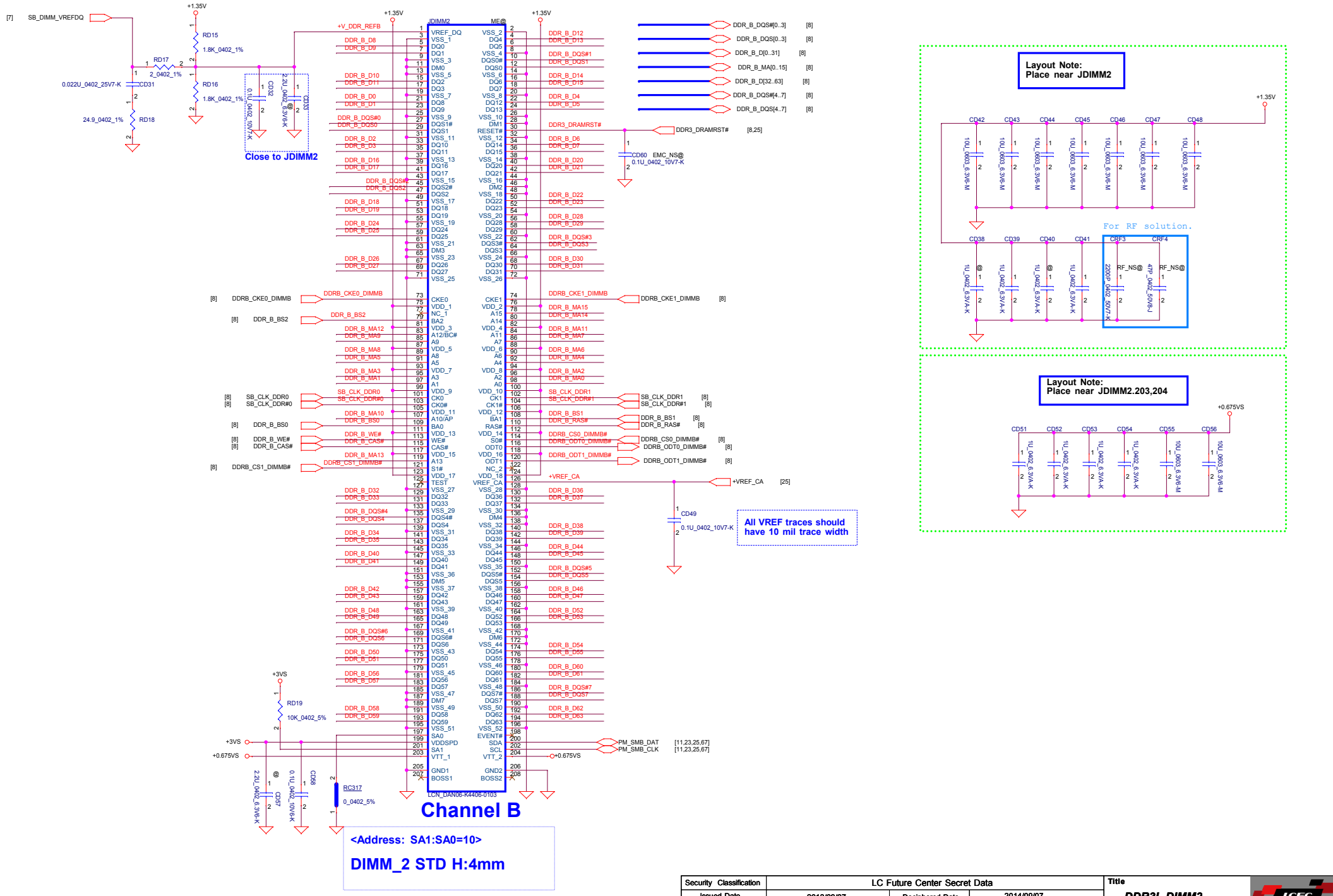
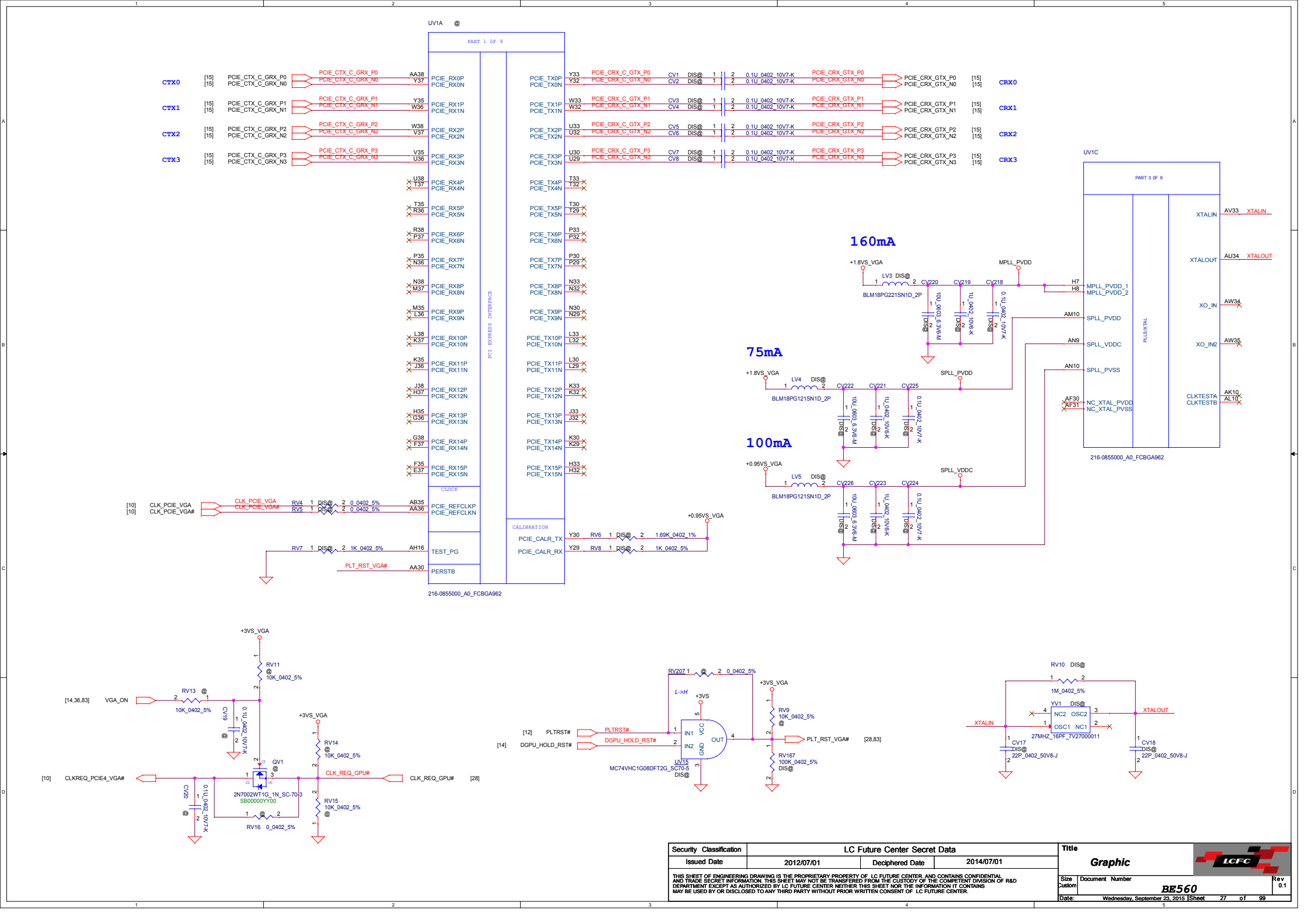


Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: DDR3L DIMM2

Size: Custom | Document Number: BE560 | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 26 of 99


UV1A @
PART 1 OF 9
PCI EXPRESS INTERFACE
CLOCK
CALIBRATION
CTX0
CTX1
CTX2
CTX3
CRX0
CRX1
CRX2
CRX3
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_RX4P
PCIE_RX4N
PCIE_RX5P
PCIE_RX5N
PCIE_RX6P
PCIE_RX6N
PCIE_RX7P
PCIE_RX7N
PCIE_RX8P
PCIE_RX8N
PCIE_RX9P
PCIE_RX9N
PCIE_RX10P
PCIE_RX10N
PCIE_RX11P
PCIE_RX11N
PCIE_RX12P
PCIE_RX12N
PCIE_RX13P
PCIE_RX13N
PCIE_RX14P
PCIE_RX14N
PCIE_RX15P
PCIE_RX15N
PCIE_REFCLKP
PCIE_REFCLKN
TEST_PG
PERSTB
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_TX4P
PCIE_TX4N
PCIE_TX5P
PCIE_TX5N
PCIE_TX6P
PCIE_TX6N
PCIE_TX7P
PCIE_TX7N
PCIE_TX8P
PCIE_TX8N
PCIE_TX9P
PCIE_TX9N
PCIE_TX10P
PCIE_TX10N
PCIE_TX11P
PCIE_TX11N
PCIE_TX12P
PCIE_TX12N
PCIE_TX13P
PCIE_TX13N
PCIE_TX14P
PCIE_TX14N
PCIE_TX15P
PCIE_TX15N
PCIE_CALR_TX
PCIE_CALR_RX
PCIE_CRX_C_GTX_P0
PCIE_CRX_C_GTX_N0
PCIE_CRX_C_GTX_P1
PCIE_CRX_C_GTX_N1
PCIE_CRX_C_GTX_P2
PCIE_CRX_C_GTX_N2
PCIE_CRX_C_GTX_P3
PCIE_CRX_C_GTX_N3
PCIE_CRX_GTX_P0
PCIE_CRX_GTX_N0
PCIE_CRX_GTX_P1
PCIE_CRX_GTX_N1
PCIE_CRX_GTX_P2
PCIE_CRX_GTX_N2
PCIE_CRX_GTX_P3
PCIE_CRX_GTX_N3
PCIE_CTX_C_GRX_P0
PCIE_CTX_C_GRX_N0
PCIE_CTX_C_GRX_P1
PCIE_CTX_C_GRX_N1
PCIE_CTX_C_GRX_P2
PCIE_CTX_C_GRX_N2
PCIE_CTX_C_GRX_P3
PCIE_CTX_C_GRX_N3
CLK_PCIE_VGA
CLK_PCIE_VGA#
PLT_RST_VGA#
+0.95VS_VGA
216-0855000_A0_FCBGA962
UV1C
PART 3 OF 9
PLL&XTAL
XTALIN
XTALOUT
XO_IN
XO_IN2
CLKTESTA
CLKTESTB
MPLL_PVDD_1
MPLL_PVDD_2
SPLL_PVDD
SPLL_VDDC
SPLL_PVSS
NC_XTAL_PVDD
NC_XTAL_PVSS
216-0855000_A0_FCBGA962
160mA
75mA
100mA
+1.8VS_VGA
MPLL_PVDD
SPLL_PVDD
SPLL_VDDC
BLM18PG221SN1D_2P
BLM18PG121SN1D_2P
+3VS_VGA
VGA_ON
CLKREQ_PCIE4_VGA#
CLK_REQ_GPU#
2N7002WT1G_1N_SC-70-3
SB00000YY00
PLTRST#
DGPU_HOLD_RST#
MC74VHC1G08DFT2G_SC70-5
27MHZ_16PF_7V27000011
Security Classification
LC Future Center Secret Data
Issued Date
2012/07/01
Deciphered Date
2014/07/01
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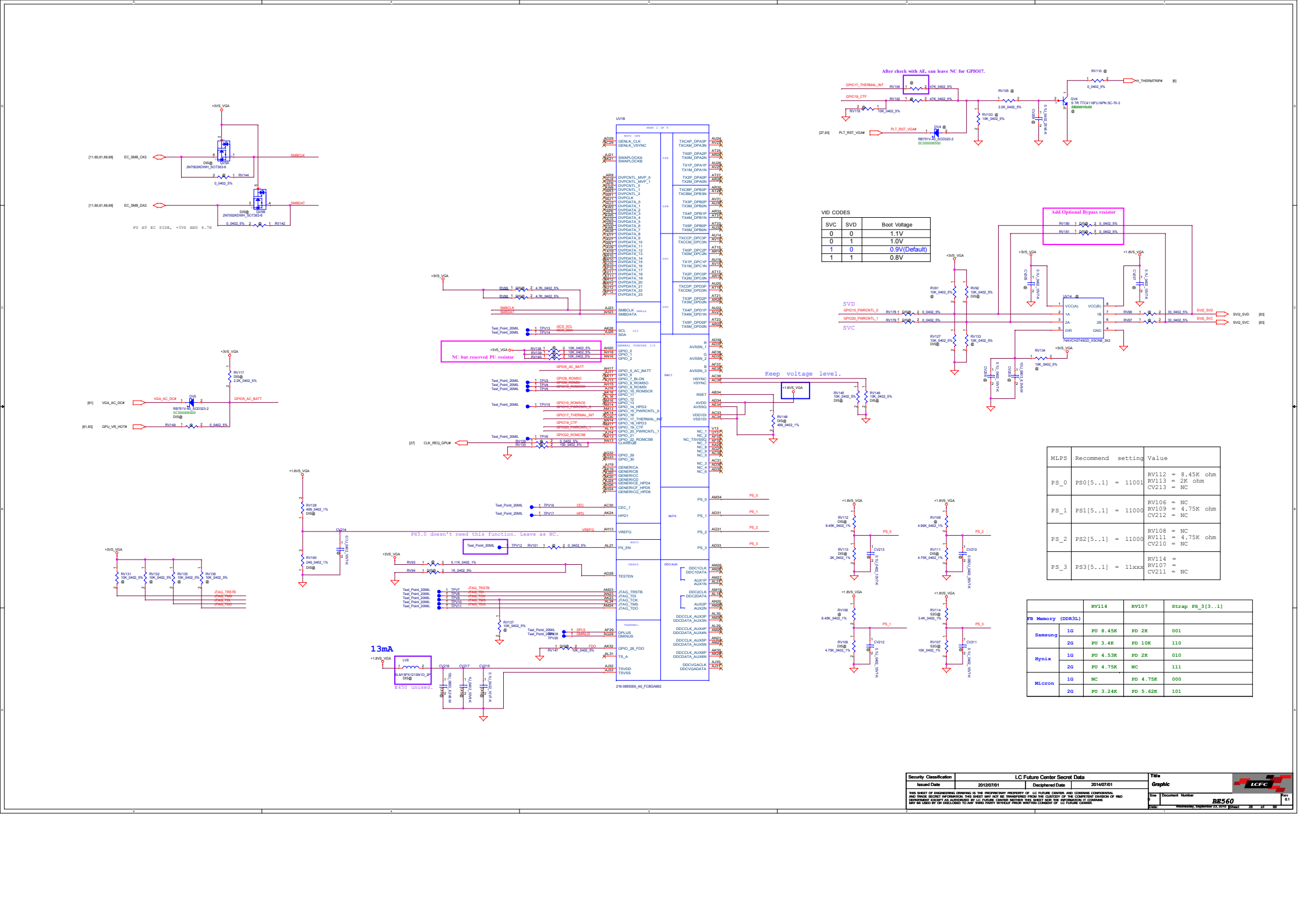
Title
Graphic
Size Custom
Document Number
BE560
Rev 0.1
Date: Wednesday, September 23, 2015
Sheet 27 of 99


After check with AE, can leave NC for GPIO17.
GPIO17_THERMAL_INT
GPIO19_CTF
PLT_RST_VGA#
H_THERMTRIP#
VID CODES
SVC SVD Boot Voltage
0 0 1.1V
0 1 1.0V
1 0 0.9V(Default)
1 1 0.8V
Add Optional Bypass resistor
SVD
SVC
SVI2_SVD
SVI2_SVC
Keep voltage level.
NC but reserved PU resistor
PX5.0 doesn't need this function. Leave as NC.
E450 unused.
13mA
PU AT EC SIDE, +3VS AND 4.7K
MLPS Recommend setting Value
PS_0 PS0[5..1] = 11001 RV112 = 8.45K ohm RV113 = 2K ohm CV213 = NC
PS_1 PS1[5..1] = 11000 RV106 = NC RV109 = 4.75K ohm CV212 = NC
PS_2 PS2[5..1] = 11000 RV108 = NC RV111 = 4.75K ohm CV210 = NC
PS_3 PS3[5..1] = 11xxx RV114 = RV107 = CV211 = NC
FB Memory (DDR3L) RV114 RV107 Strap PS_3[3..1]
Samsung 1G PU 8.45K PD 2K 001
Samsung 2G PU 3.4K PD 10K 110
Hynix 1G PU 4.53K PD 2K 010
Hynix 2G PU 4.75K NC 111
Micron 1G NC PD 4.75K 000
Micron 2G PU 3.24K PD 5.62K 101
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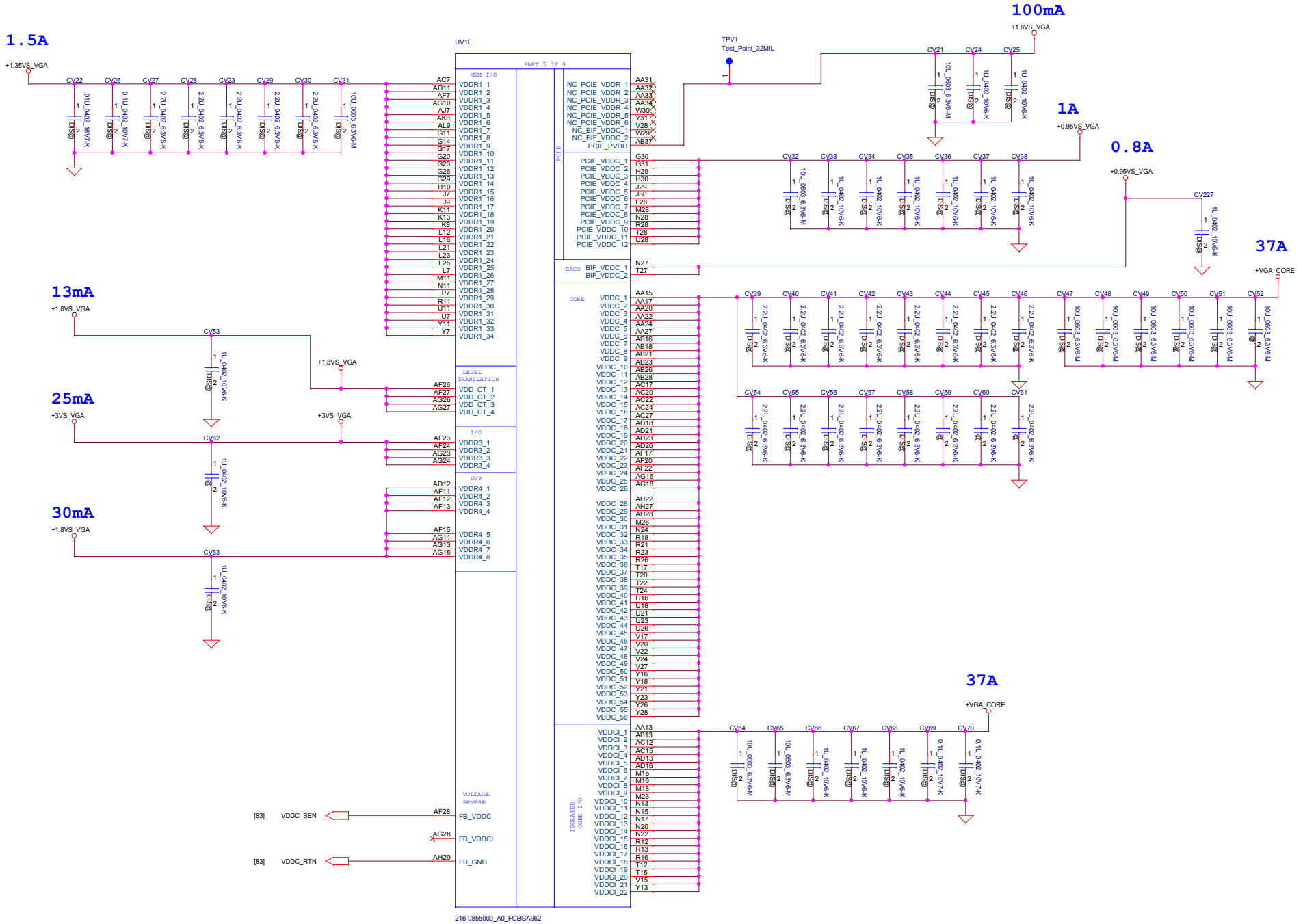
Title Graphic
Size D Document Number BE560 Rev 0.1
Date: Wednesday, September 25, 2013 Sheet 28 of 59

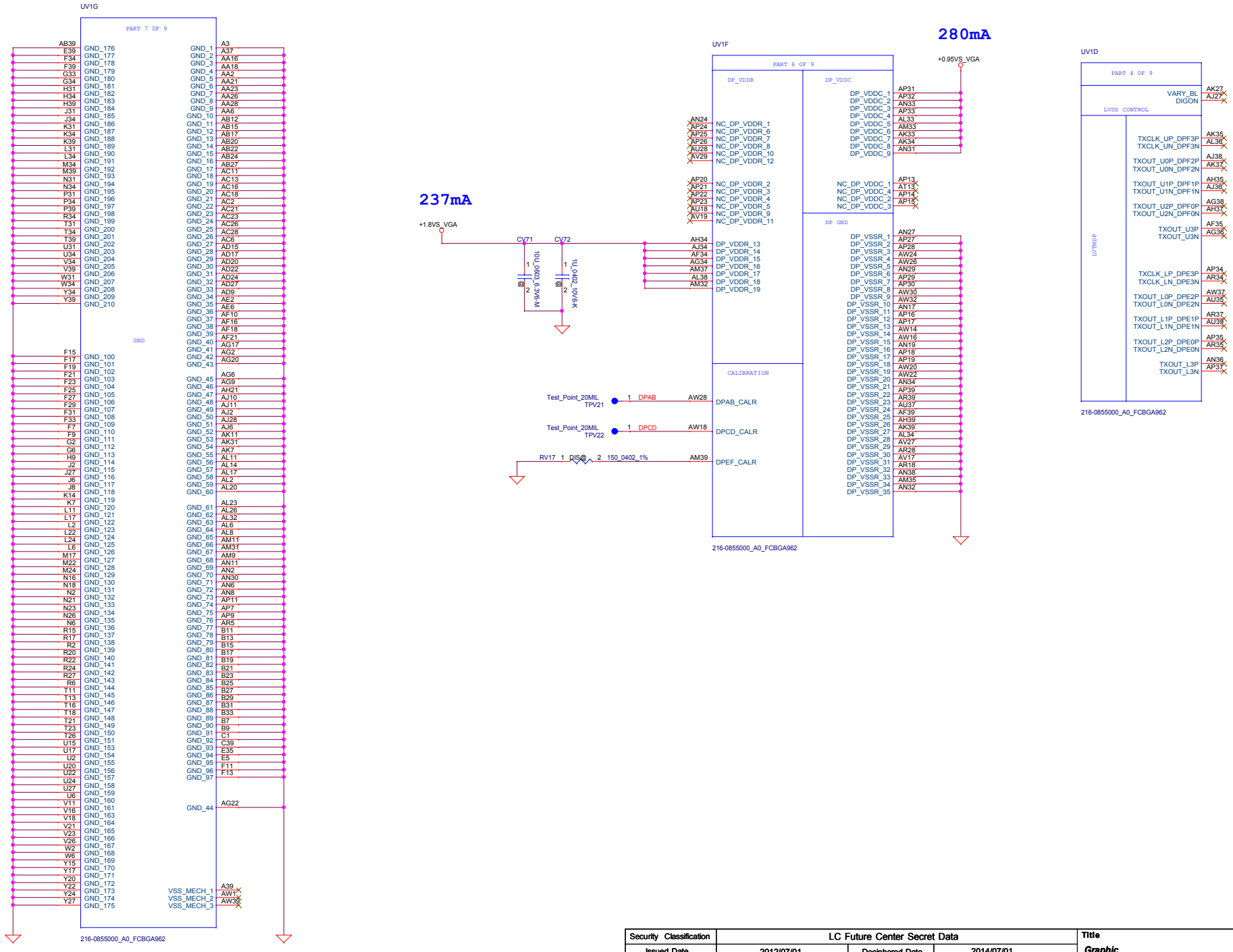


Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: Graphic

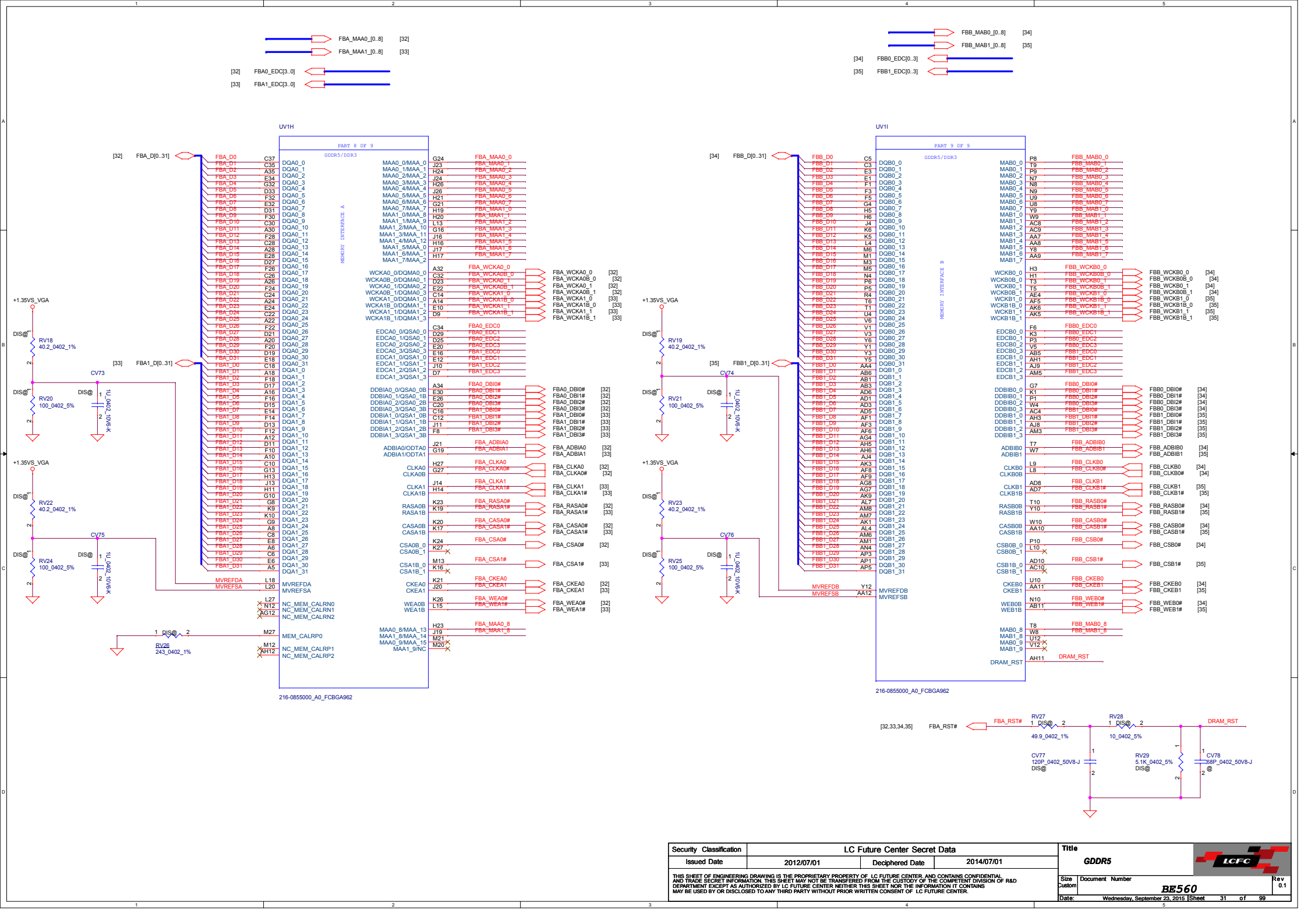
Size	Document Number	Rev
Custom	BE560	0.1

Date: Wednesday, September 23, 2015 | Sheet 29 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	Graphic		
Size: Custom	Document Number: BE560		Rev: 0.1
Date: Wednesday, September 23, 2015	Sheet 30 of 99		



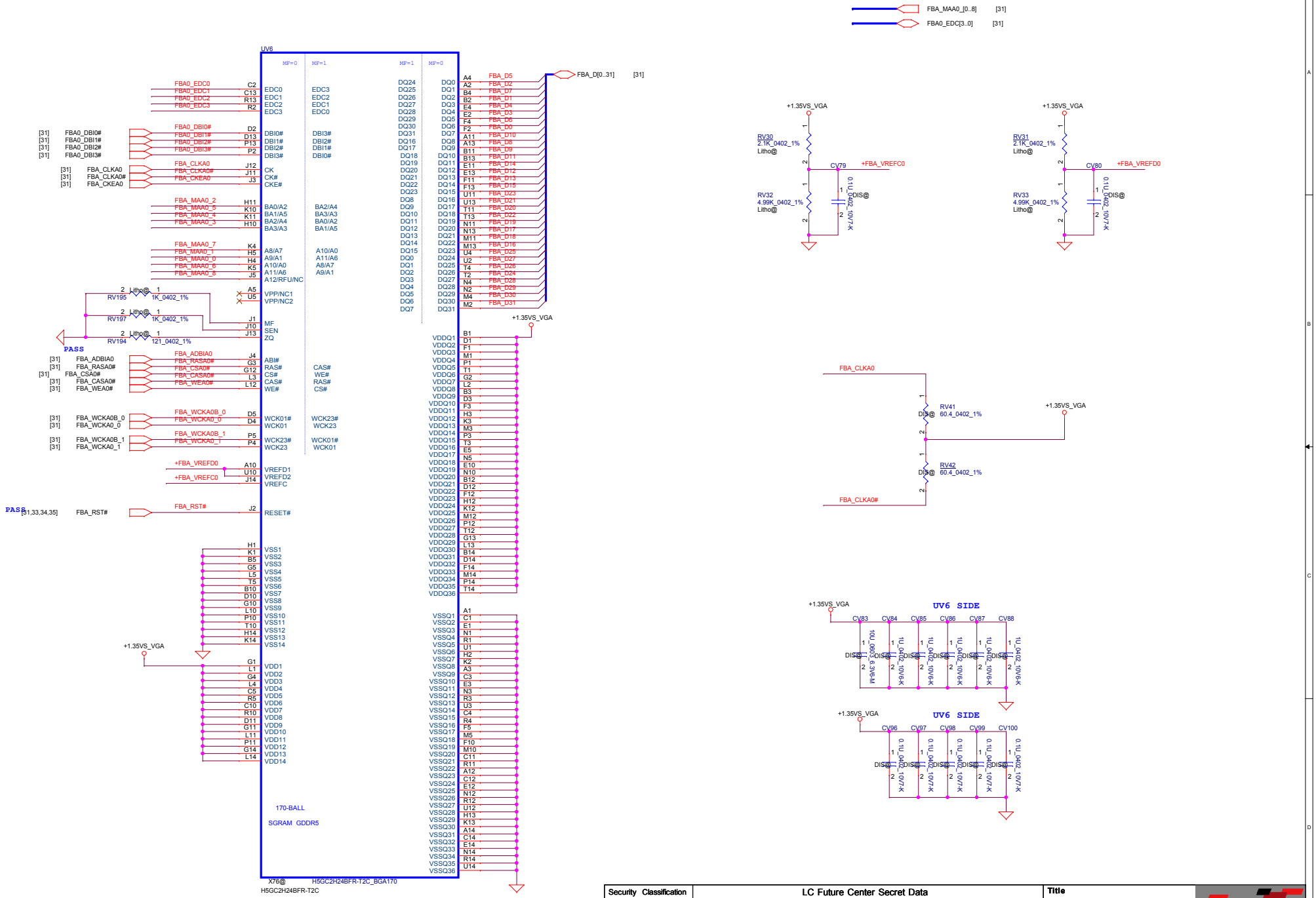
Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: GDDR5

Size: Custom | Document Number: BE560 | Rev: 0.1

Date: Wednesday, September 23, 2015 | Sheet 31 of 99

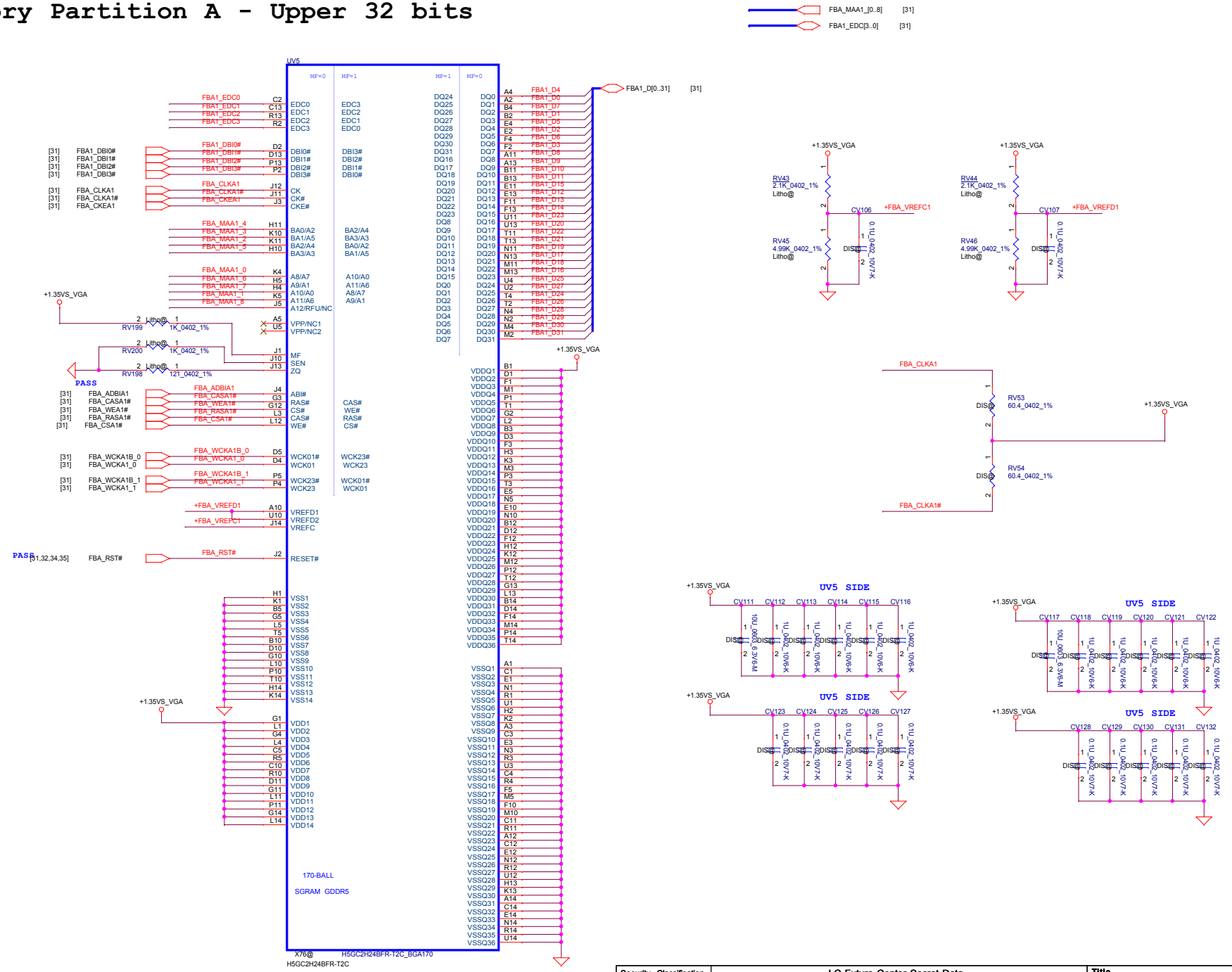
Memory Partition A - Lower 32 bits



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	GDDR5		
Size Custom	Document Number	BE560	Rev 0.1
Date:	Wednesday, September 23, 2015	Sheet 32 of 99	

Memory Partition A - Upper 32 bits



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title: GDDR5

Size	Document Number	Rev
Custom	BE560	0.1

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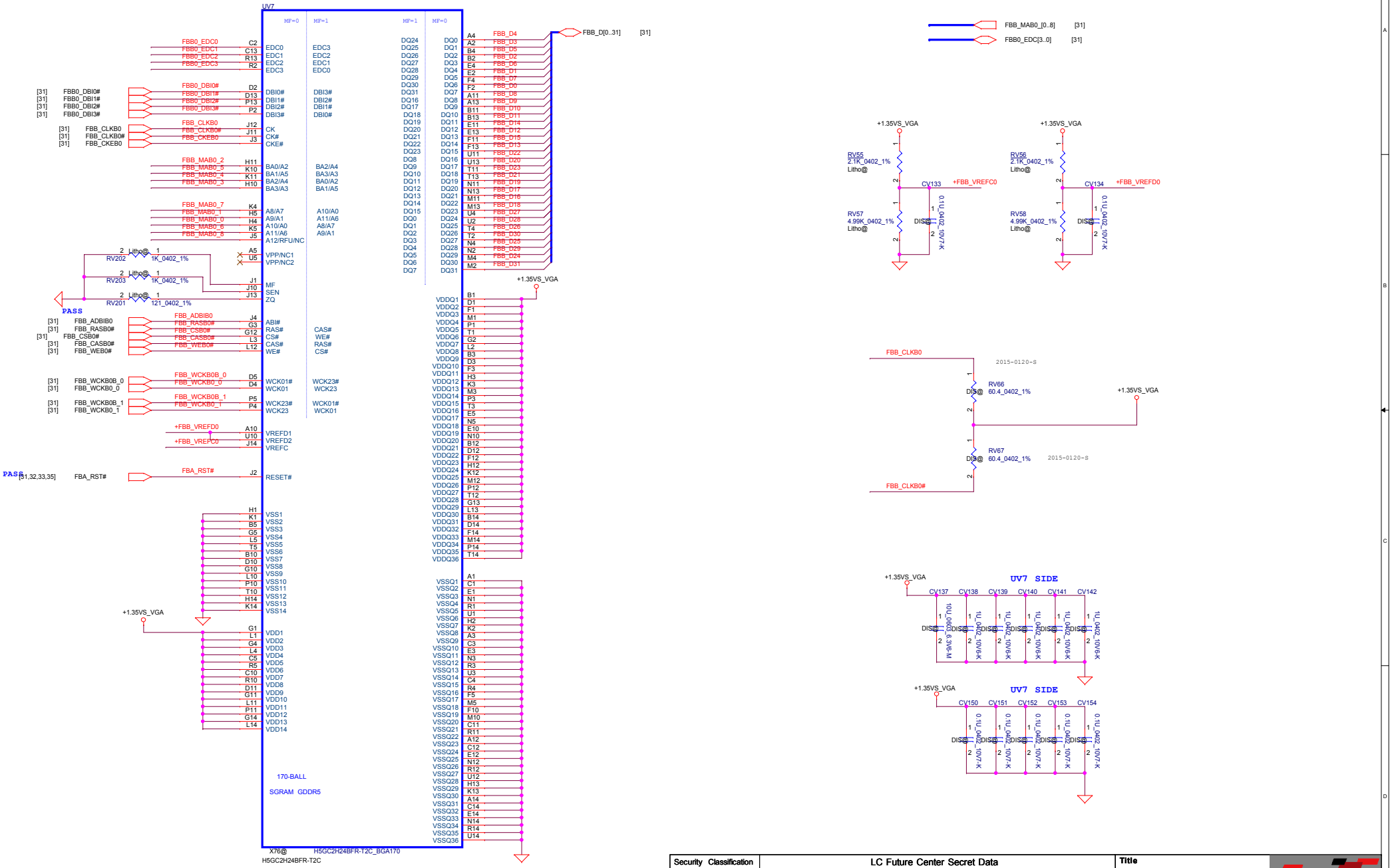
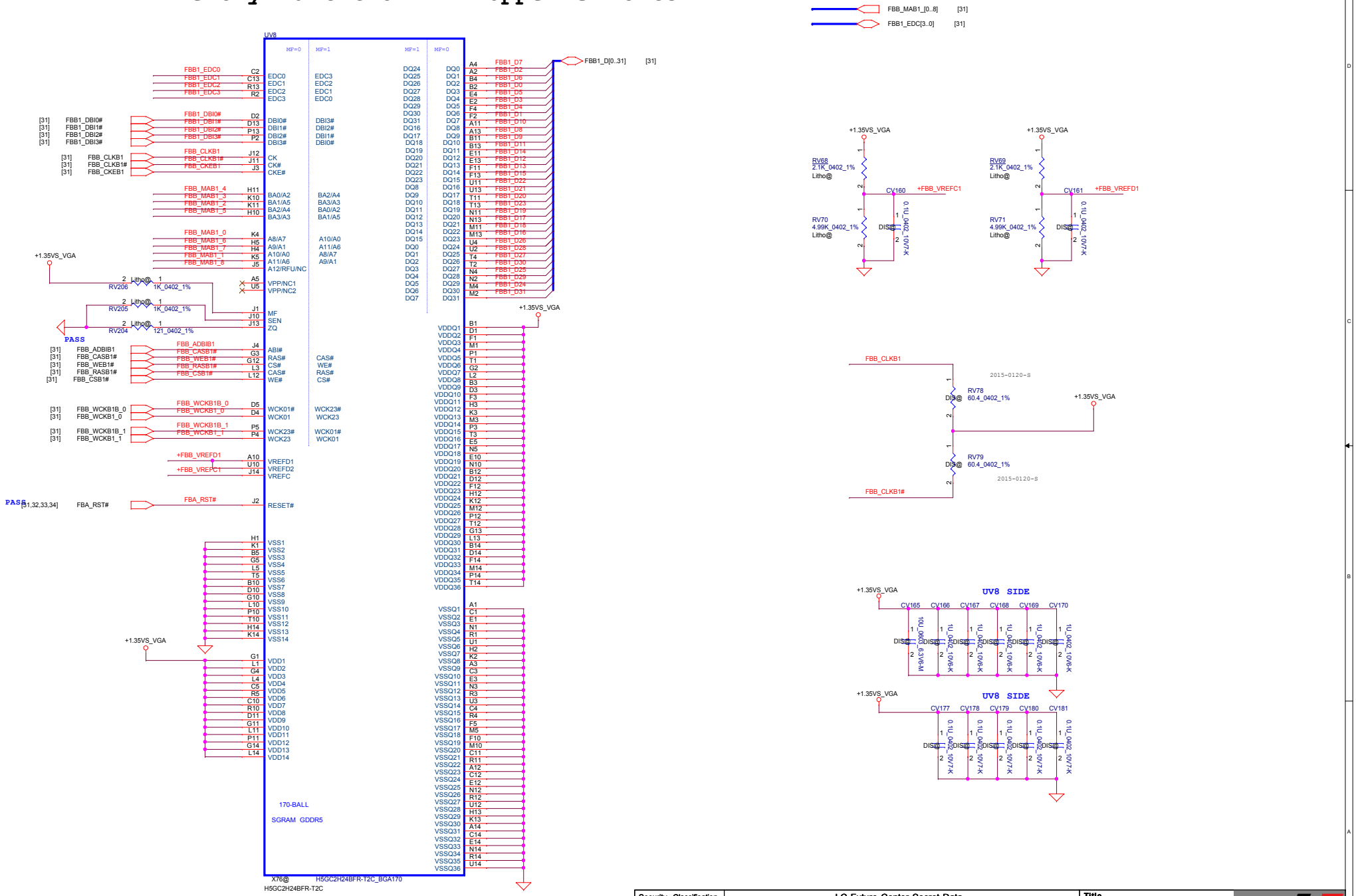
Memory Partition A - Lower 32 bits



Security Classification	LC Future Center Secret Data		
Issued Date	2012/07/01	Deciphered Date	2014/07/01

Title	GDDR5		
Size: Custom	Document Number: BE560		Rev: 0.1
Date: Wednesday, September 23, 2015	Sheet 34 of 99		

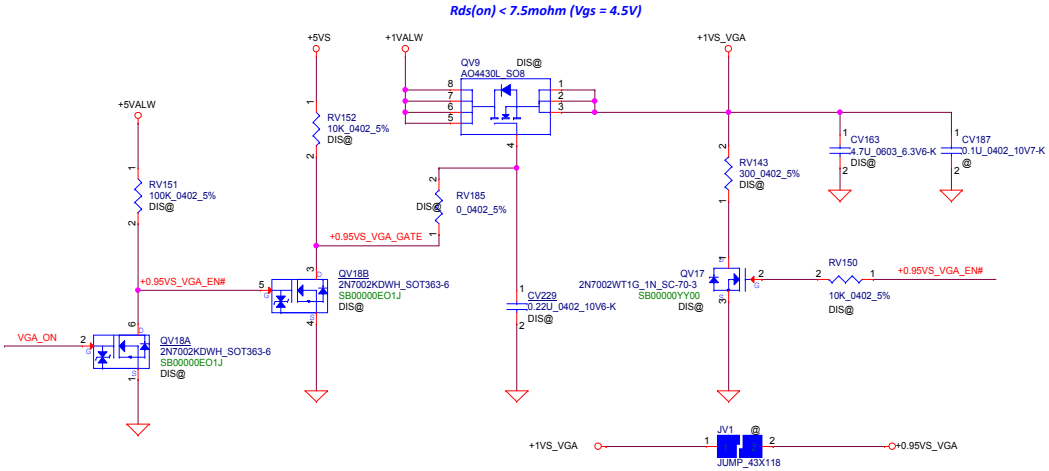
Memory Partition A - Upper 32 bits



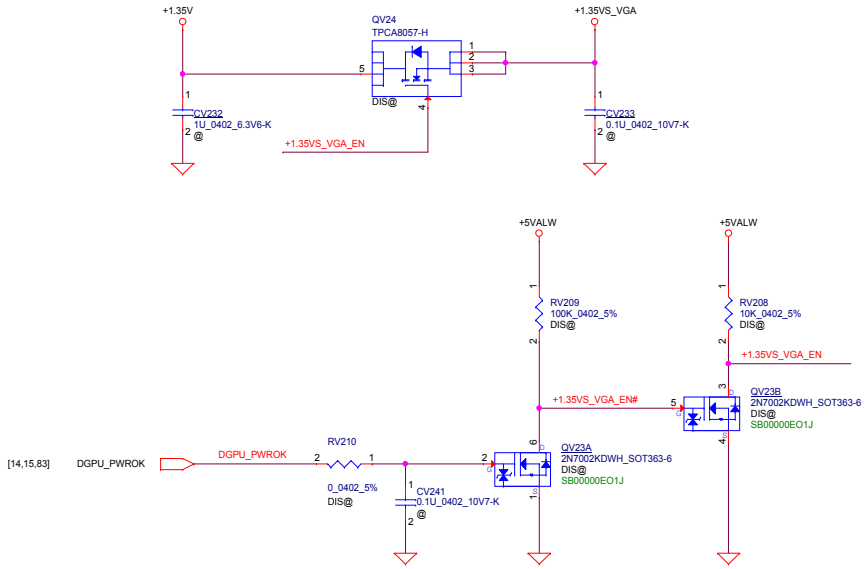
Security Classification	LC Future Center Secret Data		
Issued Date	2012/12/05	Deciphered Date	2014/12/05

Title	GDDR5		
Size: Custom	Document Number: BE560		Rev: 0.1
Date: Wednesday, September 23, 2015	Sheet 35 of 99		

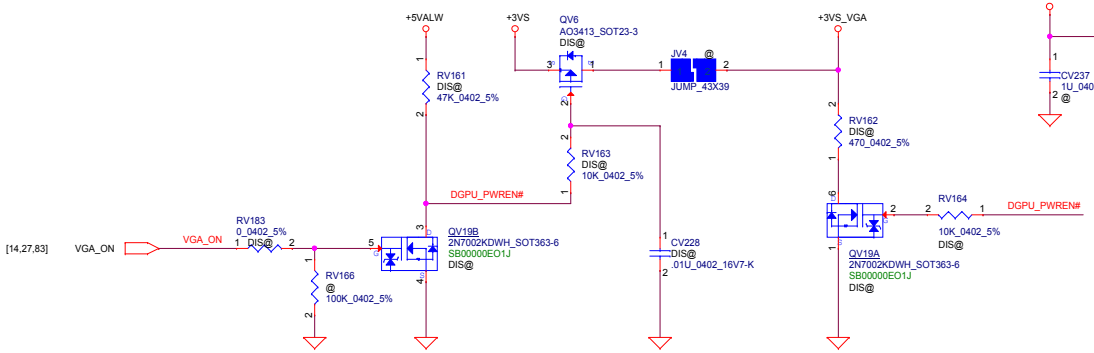
+1.0VALW to +0.95VS_VGA



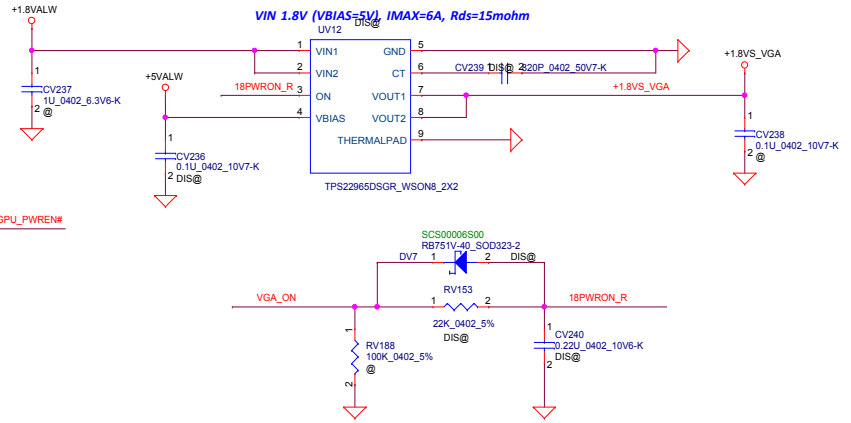
+1.35V to +1.35VS_VGA



+3VS to +3VS_VGA



+1.8VALW to +1.8VS_VGA



MLPS	Bit				
	5	4	3	2	1
PS_0[5:1]	1	1	0	0	1
PS_1[5:1]	1	1	0	0	0
PS_2[5:1]	1	1	0	0	0
PS_3[5:1]	1	1	X	X	X

Security Classification	LC Future Center Secret Data		
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Title: *Litho swich power*

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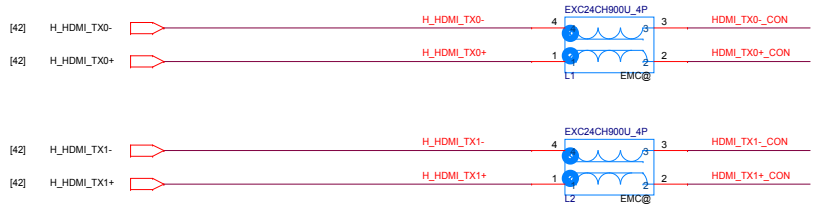

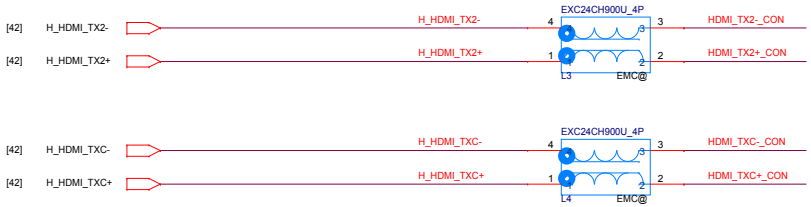

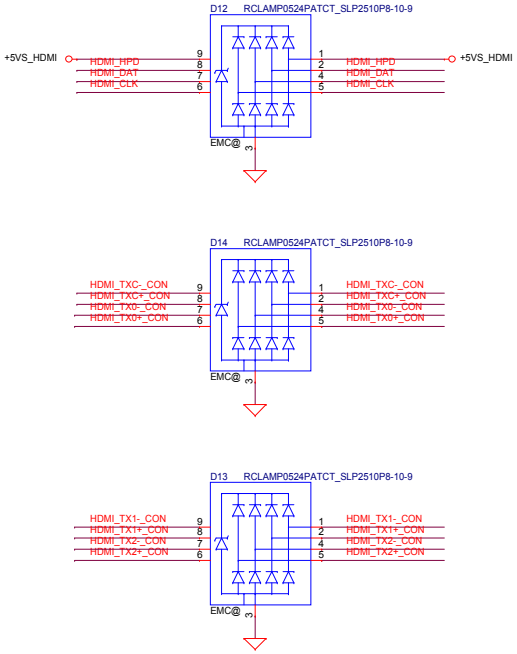

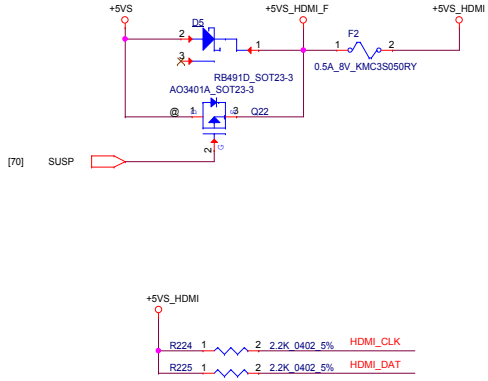

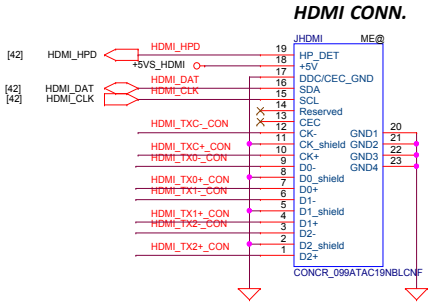

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Title: **HDMI CONN**

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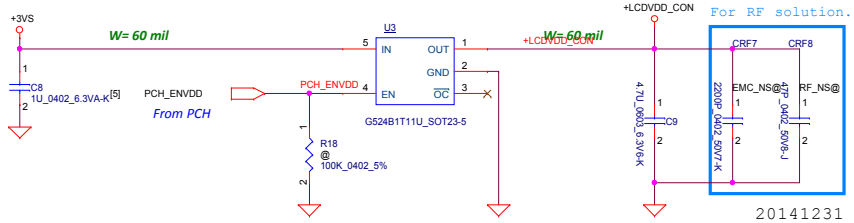
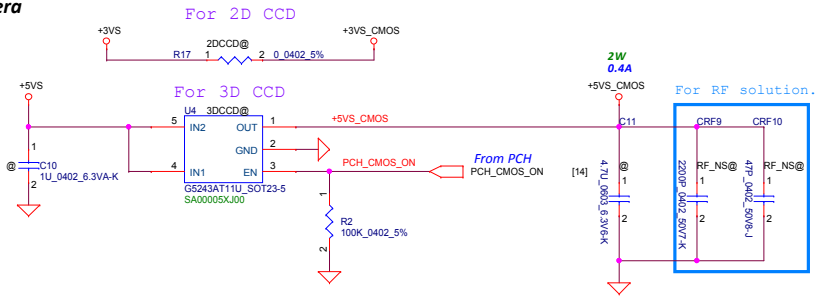
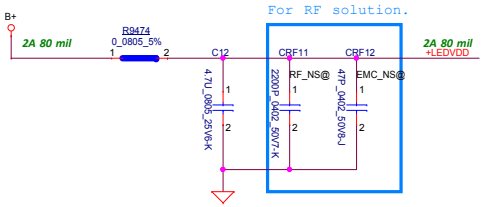
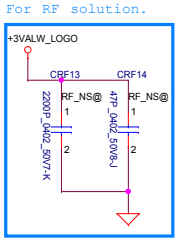
LCDVDD Circuit

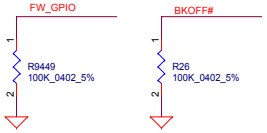


CMOS Camera

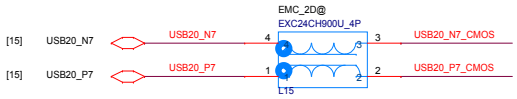


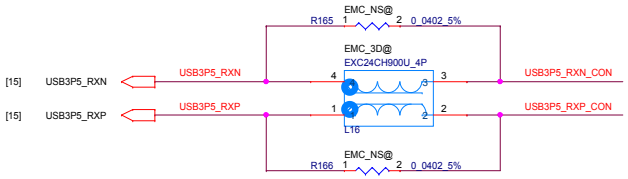


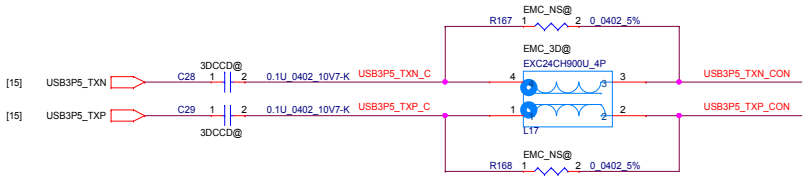




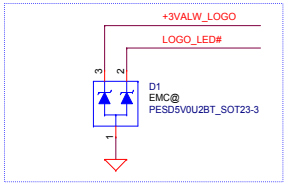
CMOS USB Port 2



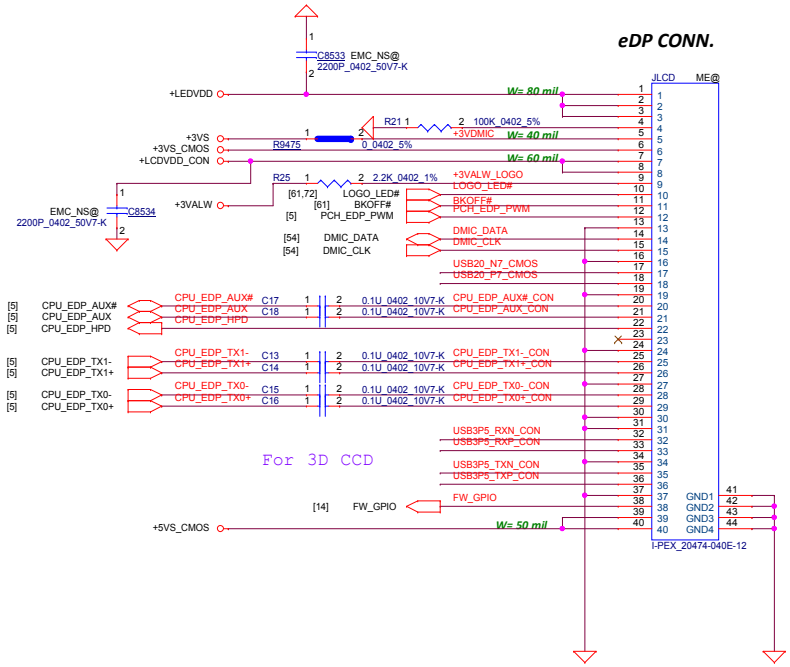




ESD request



eDP CONN.



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Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: eDP CONN

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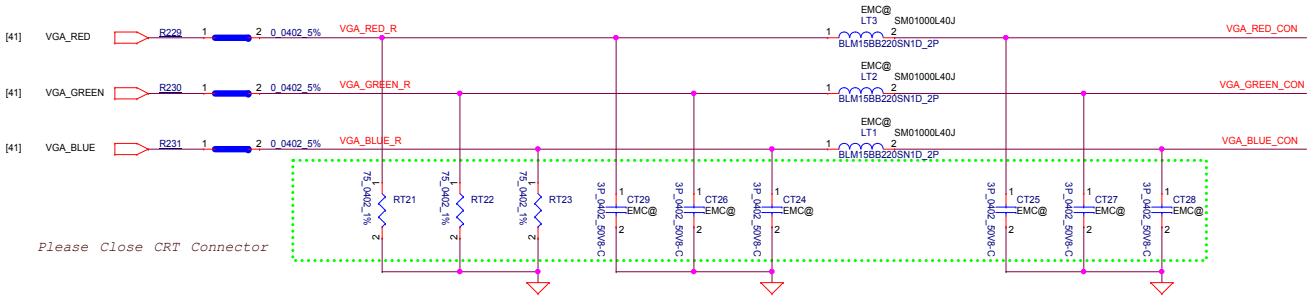
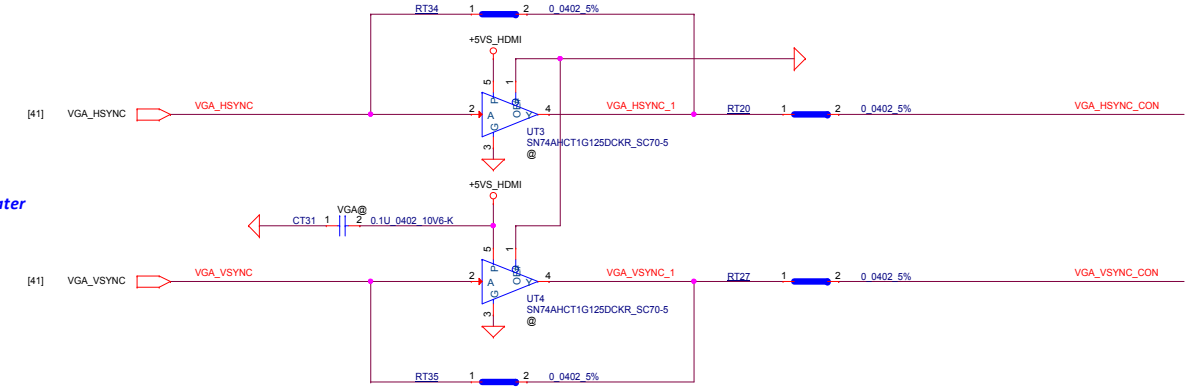
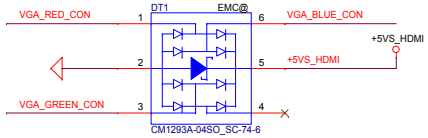
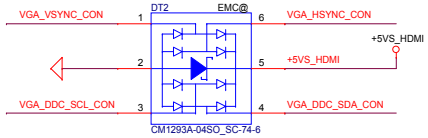
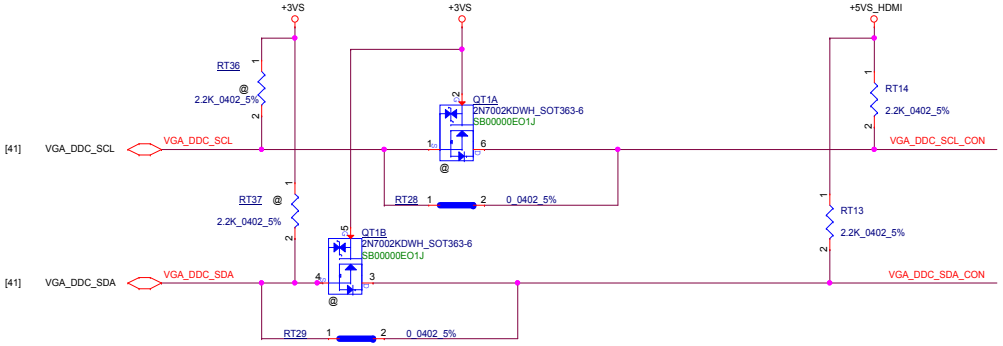


Traslater



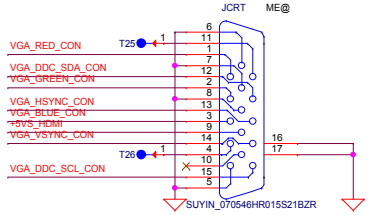






Only for 15'

CRT Connector



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **CRT CONN**

Size	Document Number	Rev
Custom	BE560	0.1

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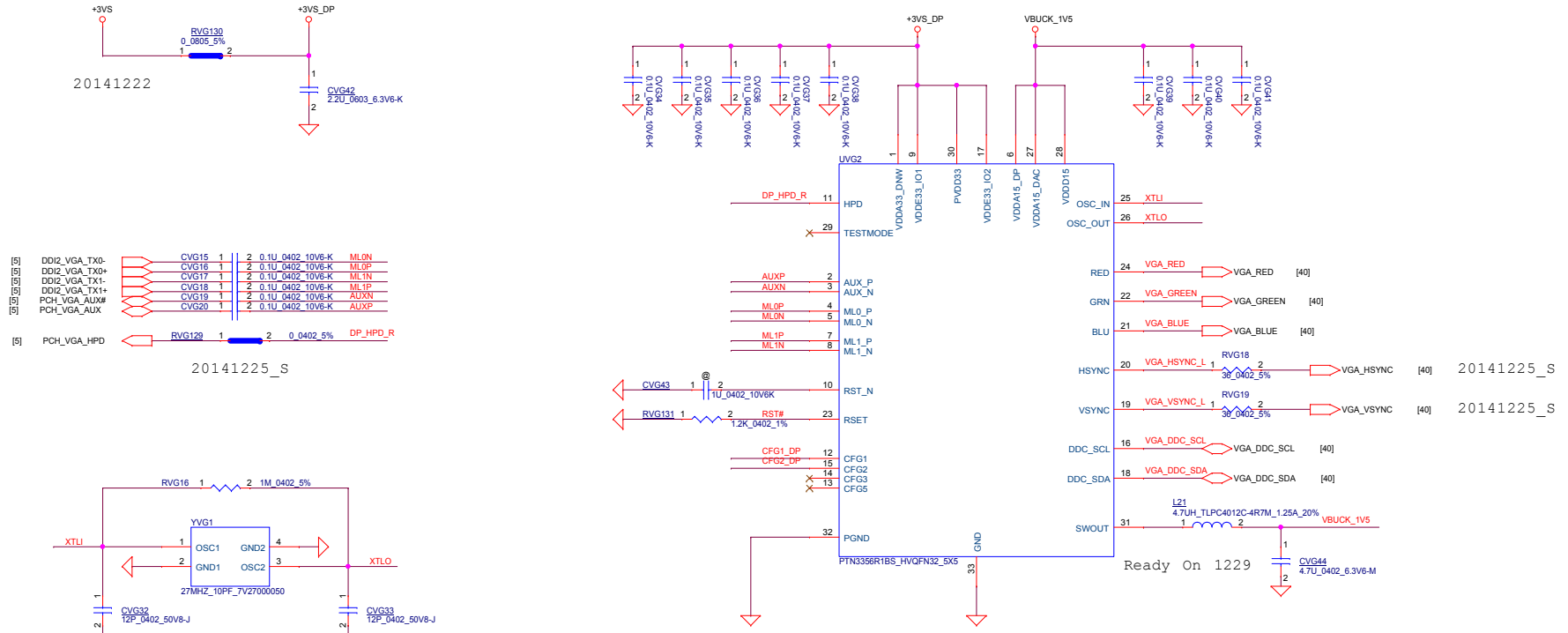

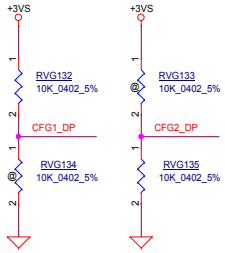

Table 7. CFG1/CFG2 pin definitions

Pin value	System behavior
00	Compliant HPD behavior
01	Most interoperable (non-compliant) HPD behavior
10	Most interoperable (non-compliant) HPD behavior
11	(Default) Compliant behavior

Security Classification	LC Future Center Secret Data		
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Title: DP to VGA

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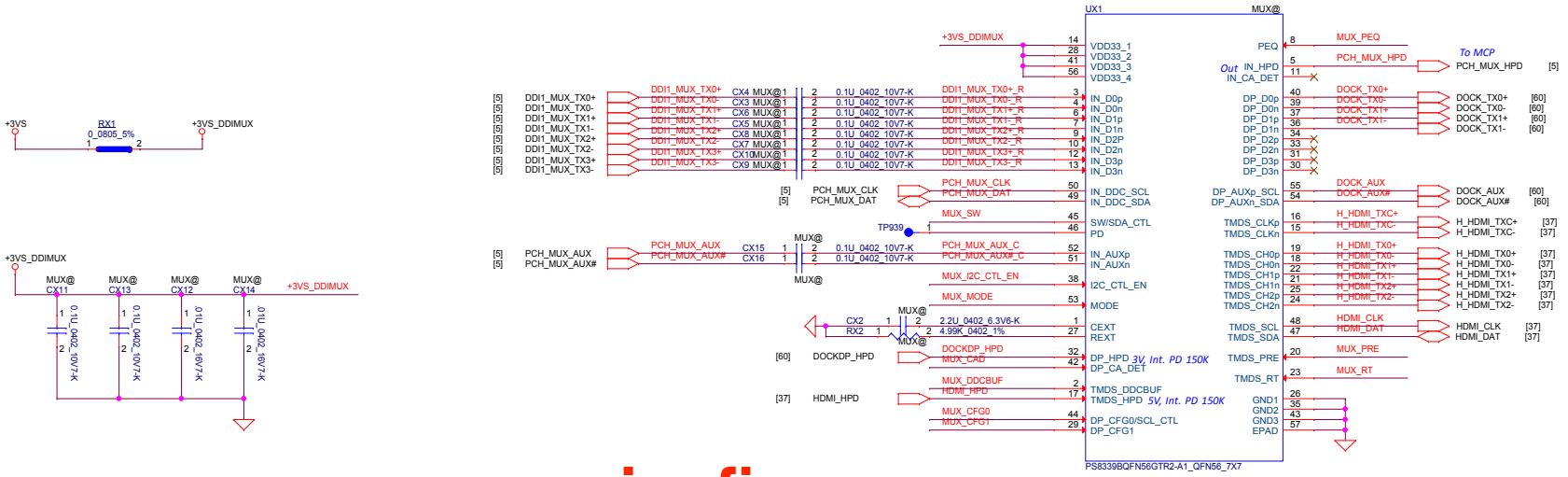
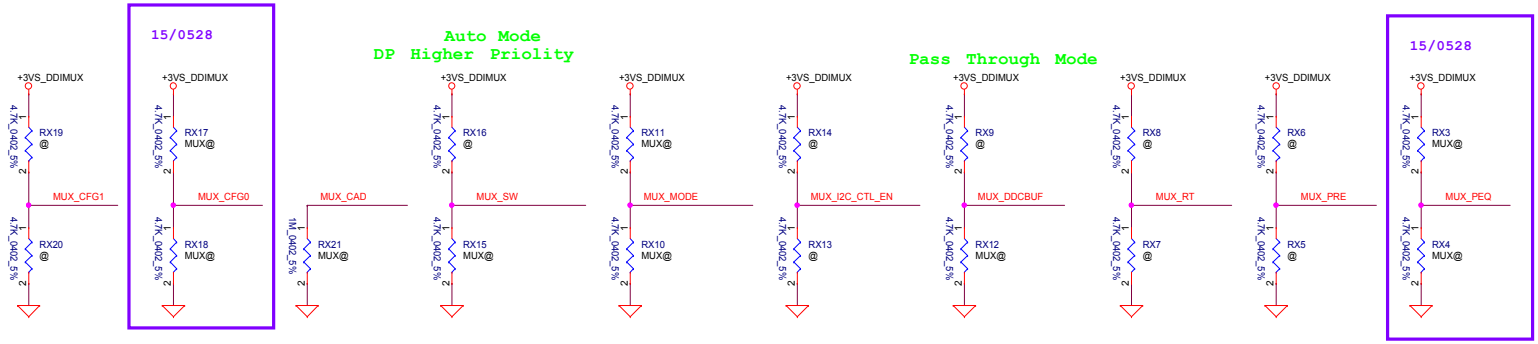


vinafix



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **Mux IC**

Size	Document Number	Rev
Custom	BE560	0.1
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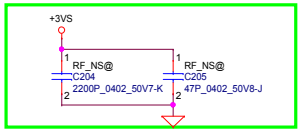
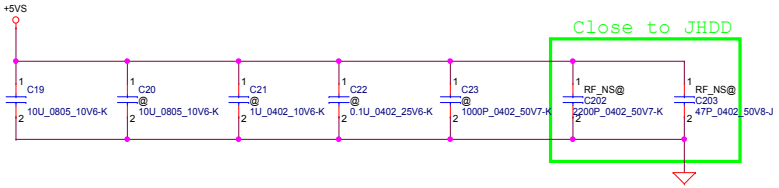
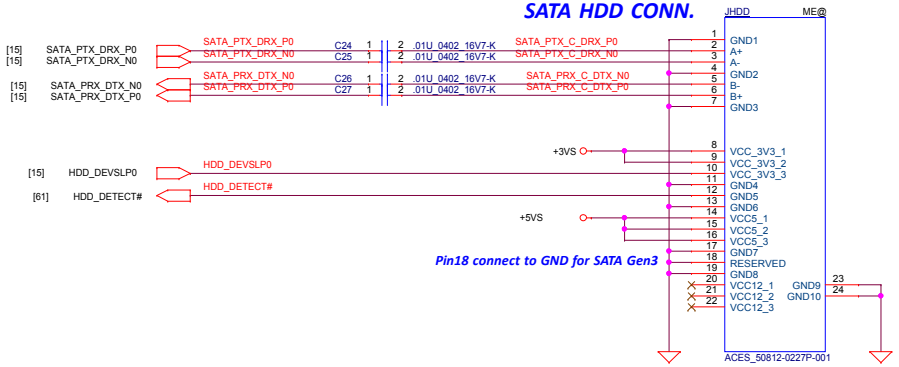
SATA HDD CONN.

Close to JHDD





SATA HDD CONN.



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **SATA HDD**

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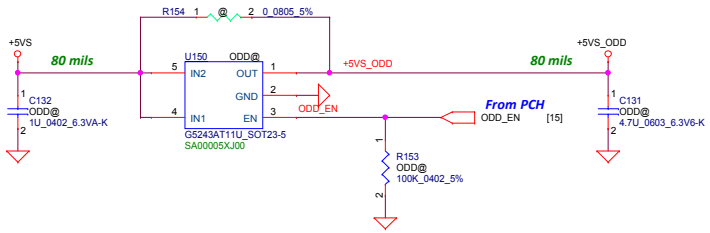
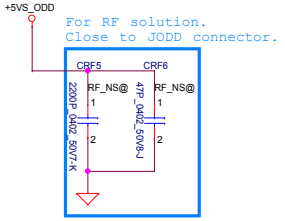
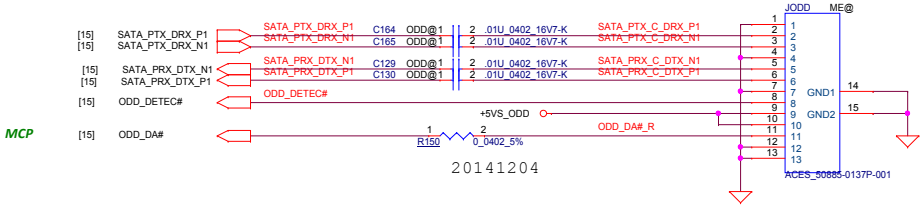
+5VS TO +5VS_ODD





SATA ODD CONN



20141204

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: ODD

Size	Document Number	Rev
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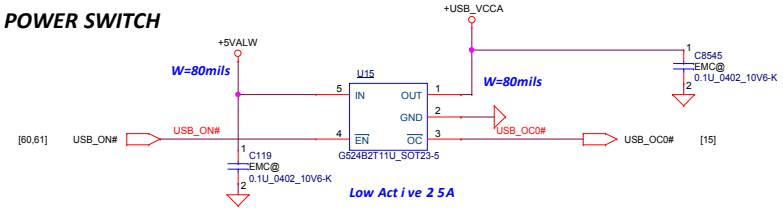
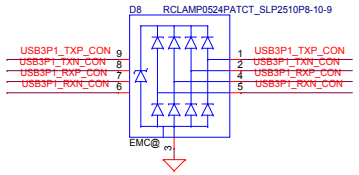
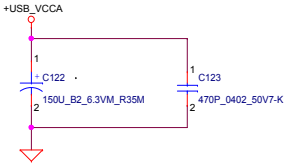
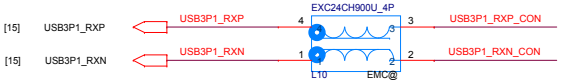
USB3 PORT1

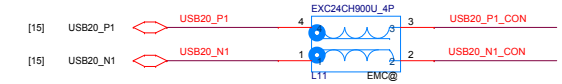
POWER SWITCH

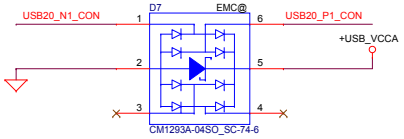


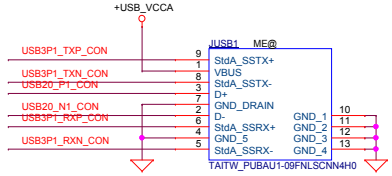




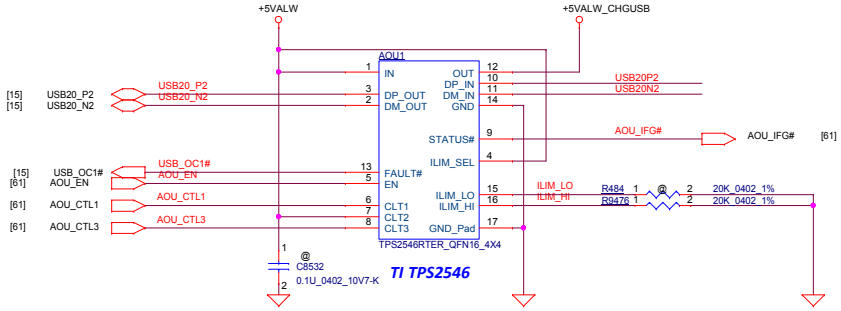




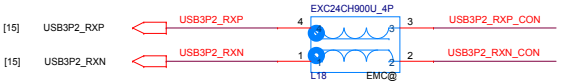


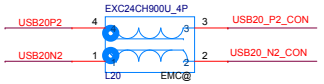


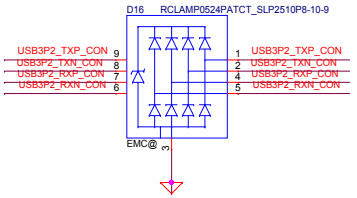
PORT2 (AOU)

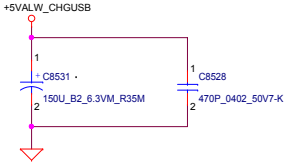


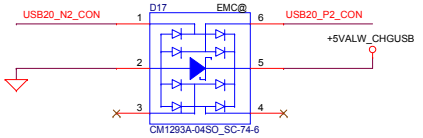
CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
1	1	1	0	SDP2	Data Connected
1	1	0	X	SDP1	Data Connected
0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

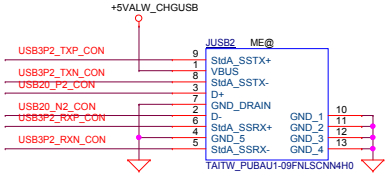












Title: USB3 PORT1/PORT2(AOU)

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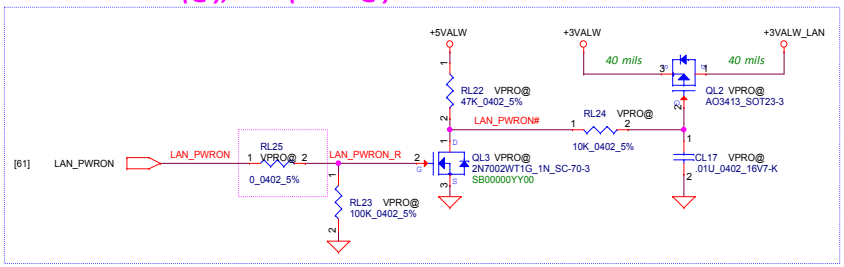
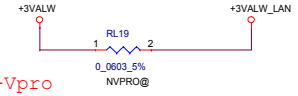
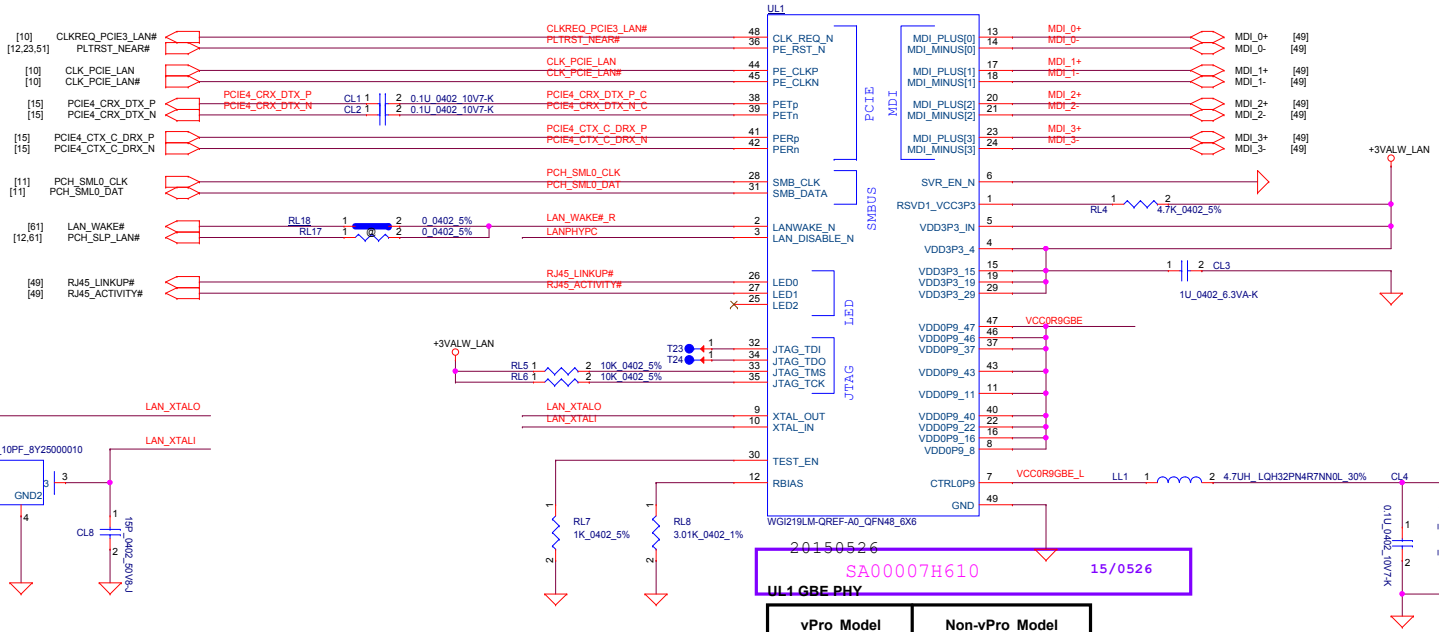
VPRO SKU : RL2 (@), RL25(VPRO@)





For Non-Vpro

20141209



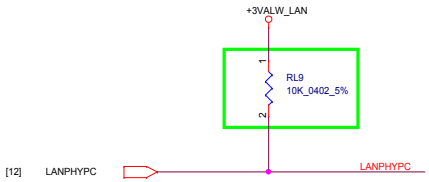
20150526

SA00007H610 15/0526

UL1 GBE PHY

vPro Model	Non-vPro Model
I219LM	I219V

ST-1_SWG_SDV-SWG_EC062
Add vPro/Non-vPro table.



When use Native function, intel recommend pull high 10K ohm
This part is un-mount in Sting.

Security Classification	LC Future Center Secret Data		
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Title: **LAN**

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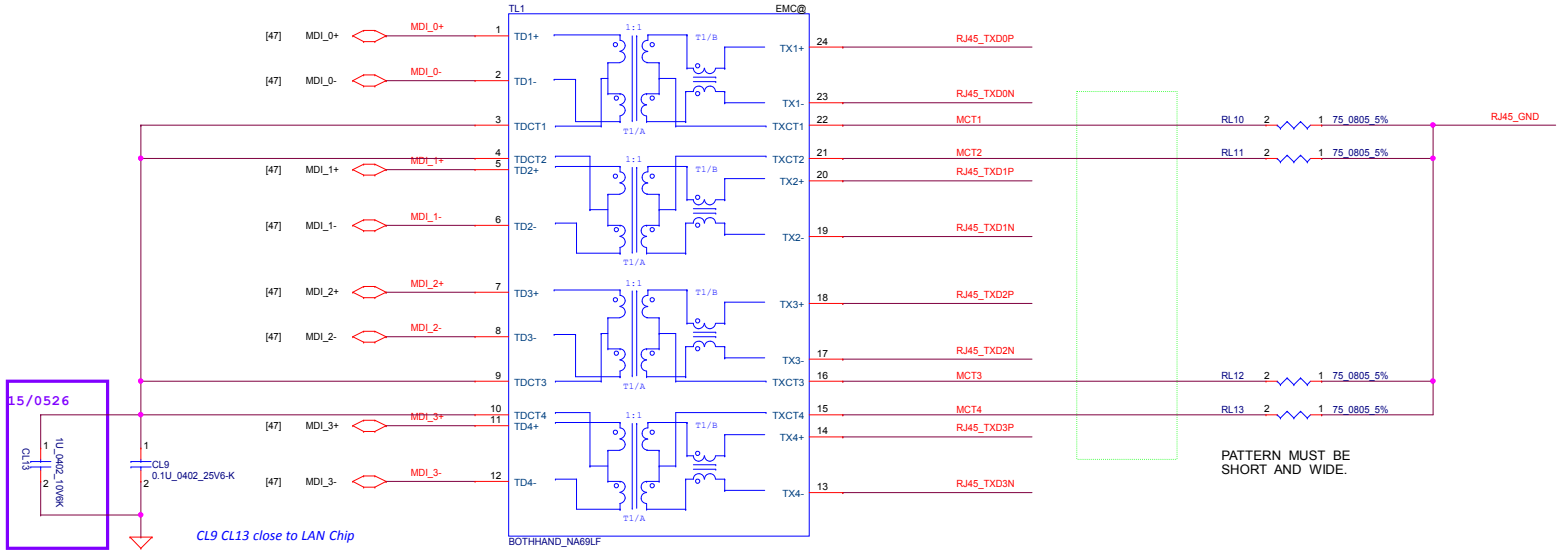
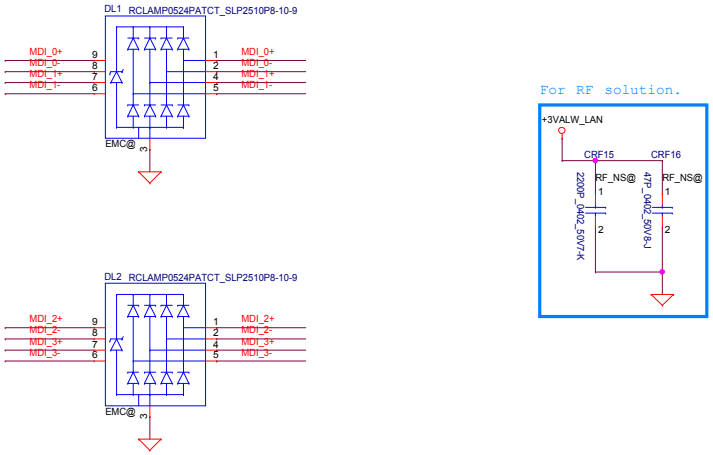
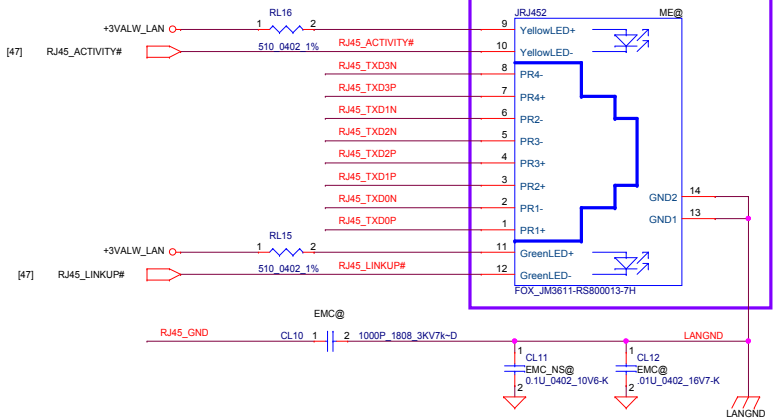


ME will change CONN on SDV phase.



For RF solution.

RJ-45 Conn.



20141231

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: RJ45 CONN

Size: Custom | Document Number: BE560 | Rev: 0.1

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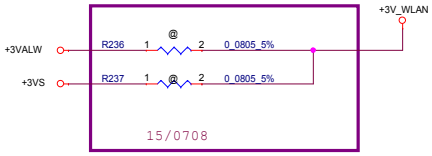
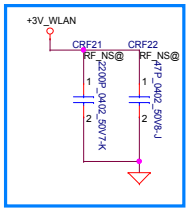
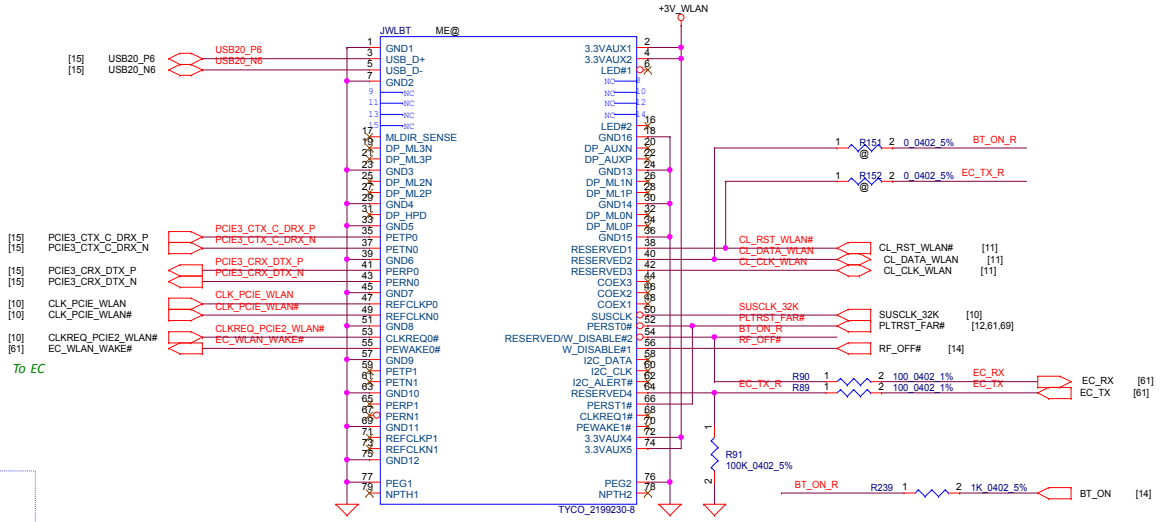
TYPE-A NGFF SLOT FOR WLAN
3.2H CONNECTOR

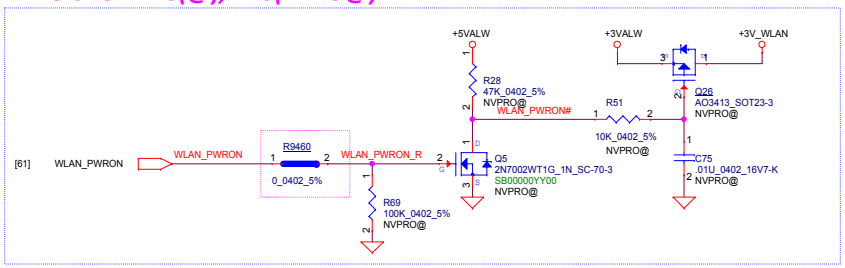


For RF solution.





VPRO SKU : R48(@), R70(VPRO@)



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: WWAN/WLAN NGFF CONN.

Size	Document Number	Rev
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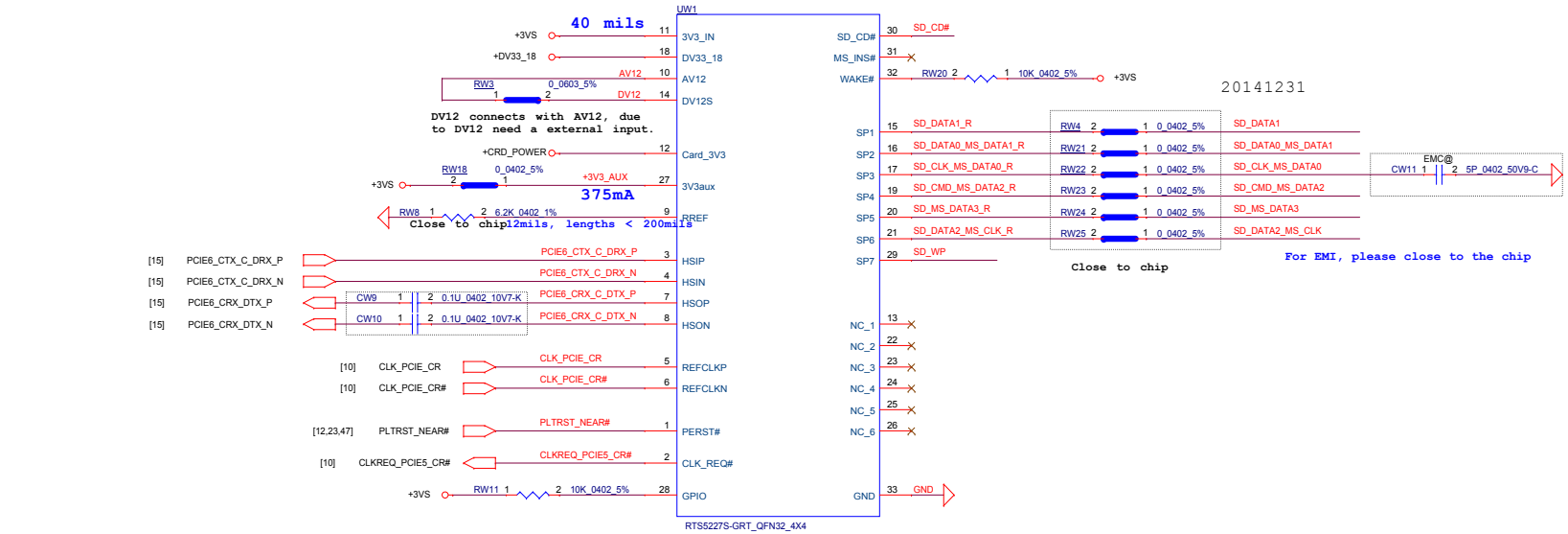

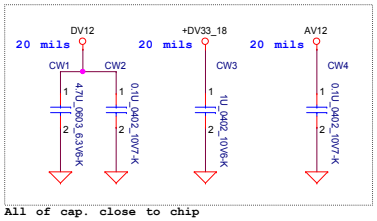

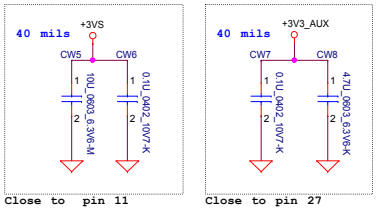

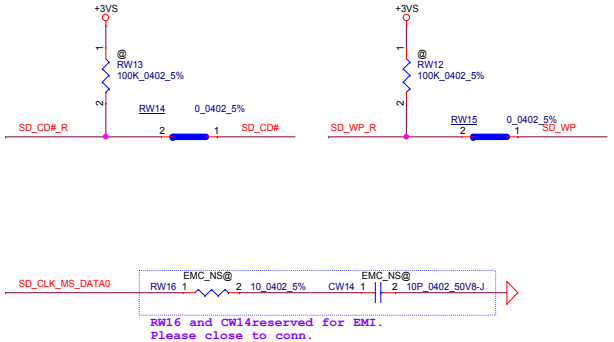

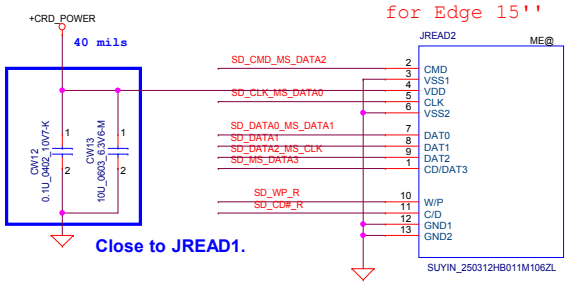

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **Card Reader**

Size	Document Number	Rev
Custom	BE560	0.1

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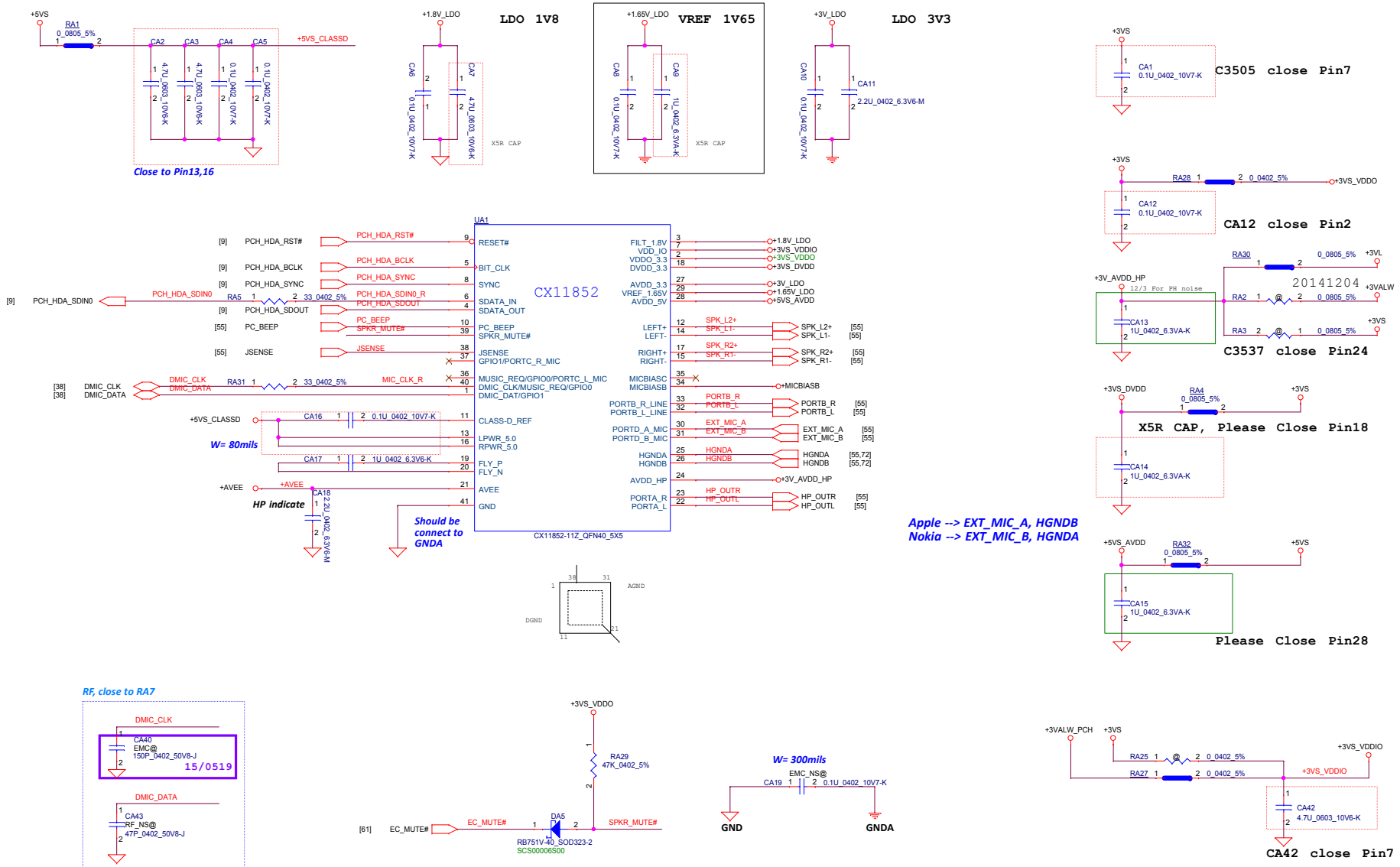

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Issued Date	2013/09/07	Deciphered Date	2014/09/07

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Title: **Audio Codec**

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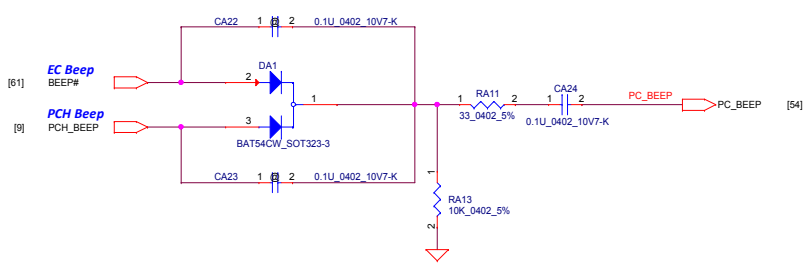
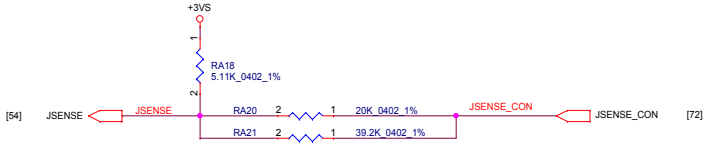
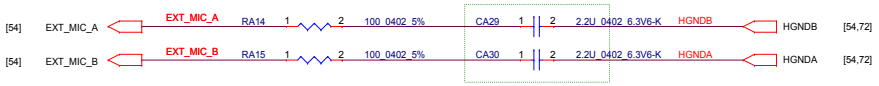
PC Beep





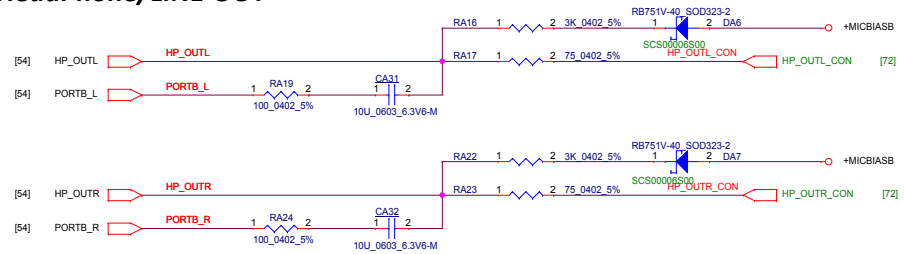
EXT. MIC/LINE IN

Apple --> EXT_MIC_A, HGNDB
Nokia --> EXT_MIC_B, HGNDA



Changed CA29 & CA30 from 1uF to 2.2uF/X5R
to meet Port-D(headset-Mic) THD+N <= -65 dB

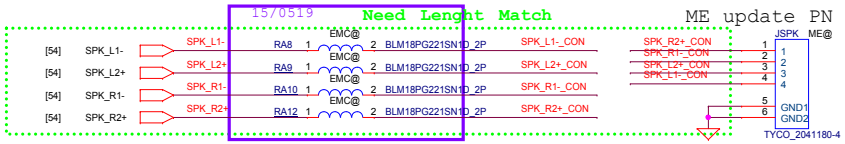
HeadPhone/LINE OUT

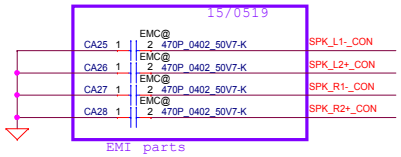


CA31, CA32 change to 4.7U for Quality requirement

Speaker OUT

SPK CONN.





Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **HP/MIC JACK/Speaker**

Size	Document Number	Rev
Custom	BE560	0.1

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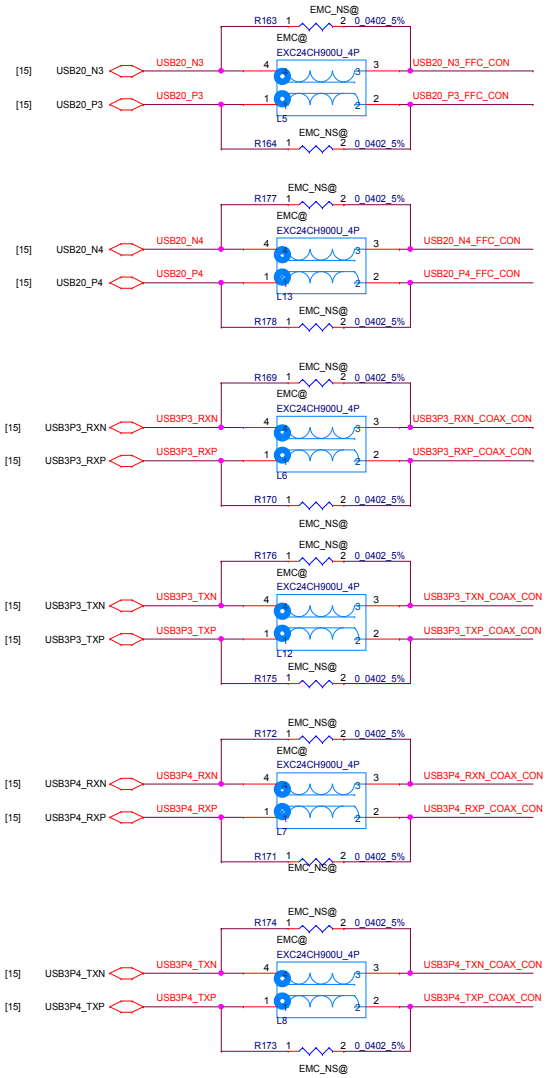
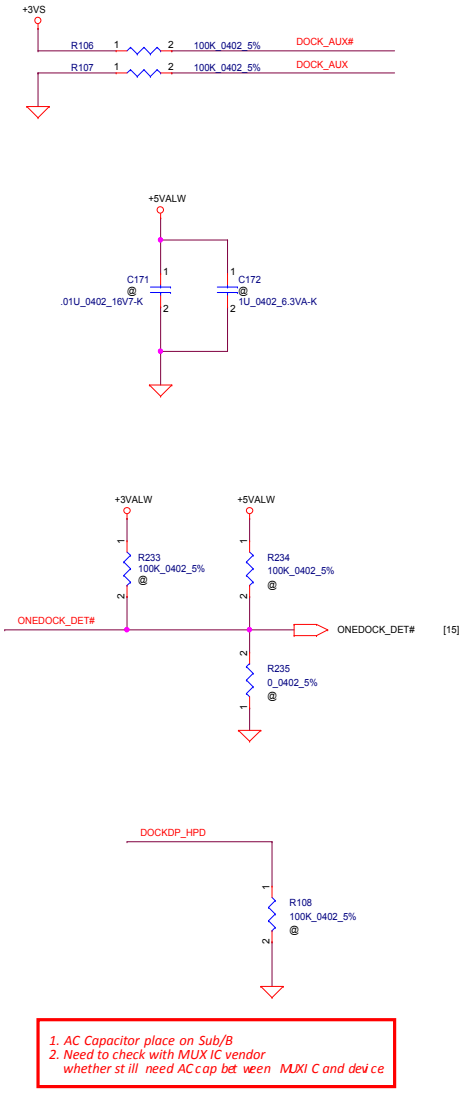
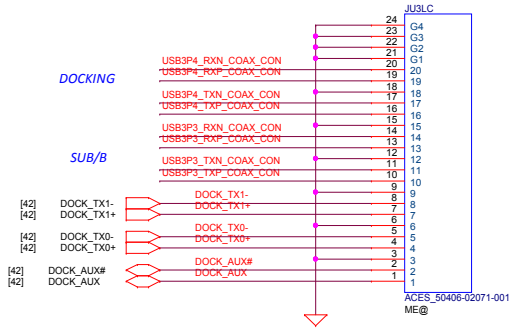


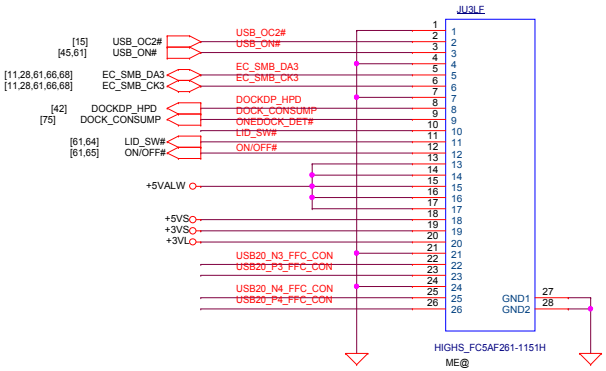


1. AC Capacitor place on Sub/B
2. Need to check with MUX IC vendor whether still need AC cap between MUXIC and device

CABLE



FFC



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **DOCKING/ DCIN CONN**

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Custom	BE560	0.1

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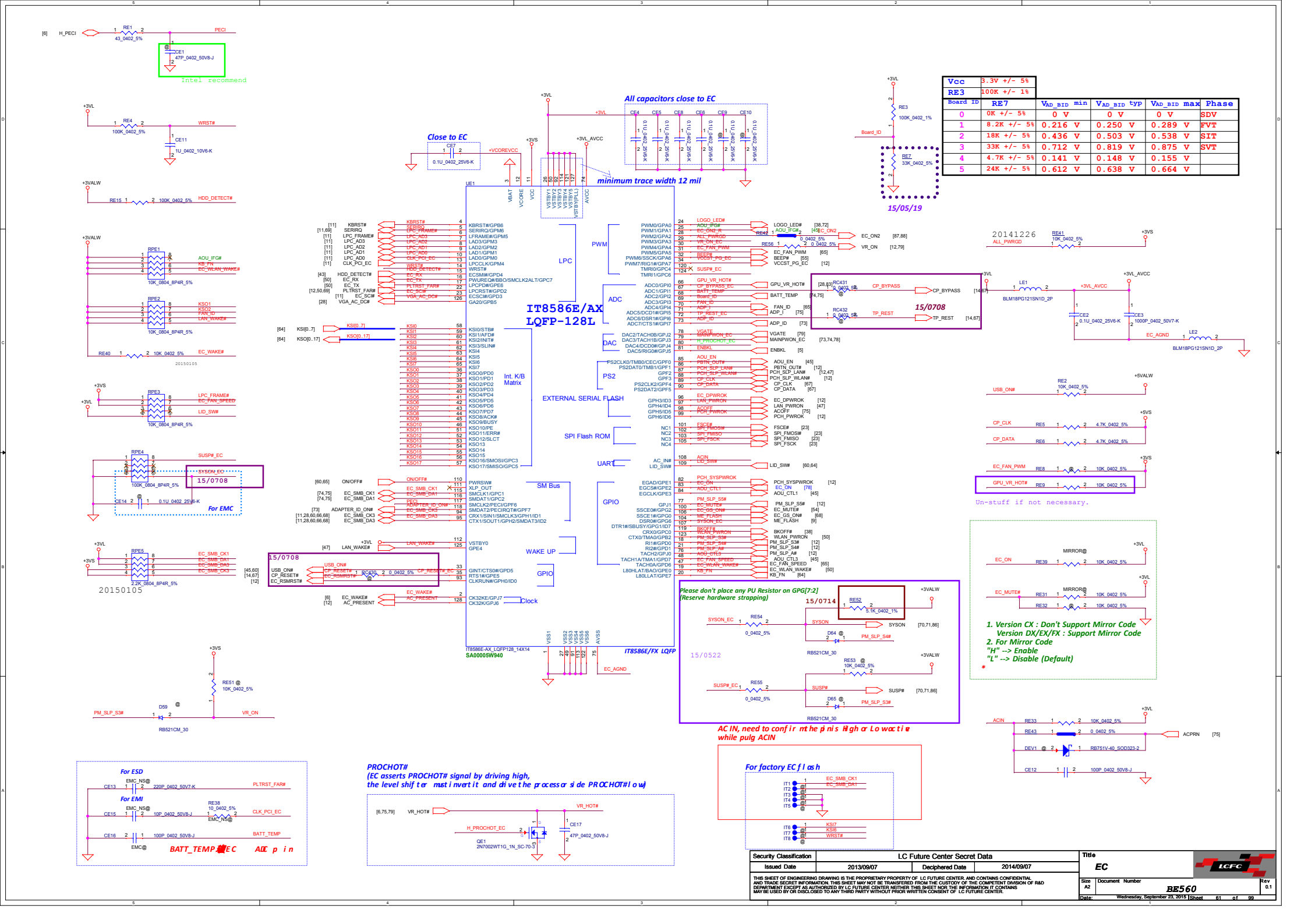
IT8586E/AX
LQFP-128L
All capacitors close to EC
Close to EC
minimum trace width 12 mil
15/05/19
Vcc 3.3V +/- 5%
RE3 100K +/- 1%
Board ID | RE7 | VAD_BID min | VAD_BID typ | VAD_BID max | Phase
0 | 0K +/- 5% | 0 V | 0 V | 0 V | SDV
1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V | FVT
2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V | SIT
3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V | SVT
4 | 4.7K +/- 5% | 0.141 V | 0.148 V | 0.155 V |
5 | 24K +/- 5% | 0.612 V | 0.638 V | 0.664 V |
15/0708
15/0714
15/0522
Un-stuff if not necessary.
1. Version CX : Don't Support Mirror Code
Version DX/EX/FX : Support Mirror Code
2. For Mirror Code
"H" --> Enable
"L" --> Disable (Default)
AC IN, need to confirm the pin is High or Low active while pulg ACIN
Please don't place any PU Resistor on GPG[7:2] (Reserve hardware strapping)
For ESD
For EMI
For EMC
For factory EC flash
PROCHOT# (EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the processor side PROCHOT# low)
BATT_TEMP pin
ADC pin
Intel recommend
20150105
20141226
IT8586E-AX_LQFP128_14X14
SA00005W940
IT8586E/FX LQFP
Security Classification | LC Future Center Secret Data
Issued Date | 2013/09/07 | Deciphered Date | 2014/09/07
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Title: EC
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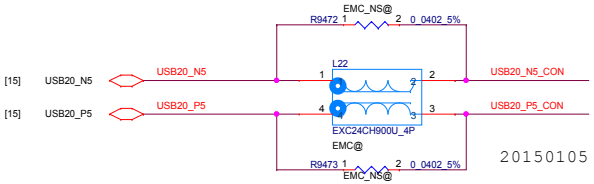
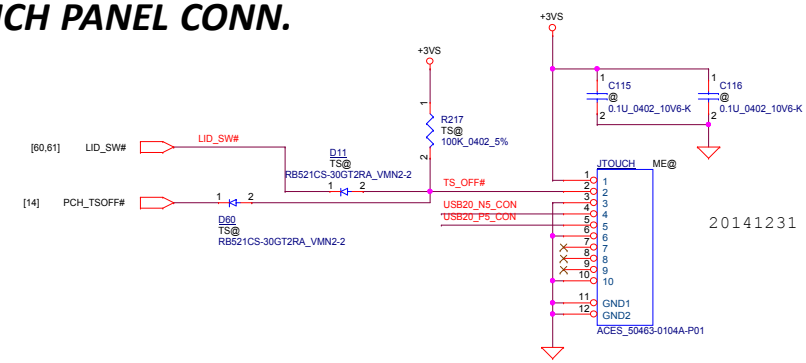
TOUCH PANEL CONN.

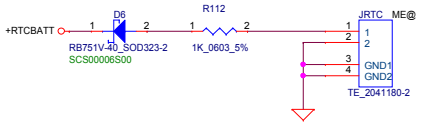


20150105

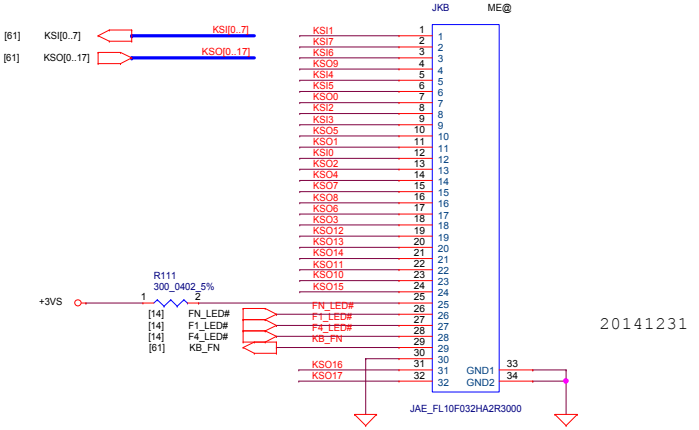


20141231

RTC CONN.



KB CONN



20141231

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: KB/RTC/TOUCH PAN CONN.

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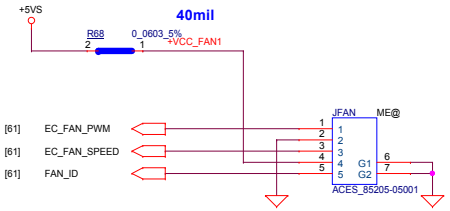
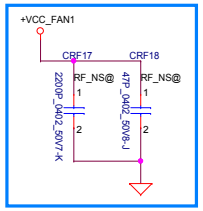
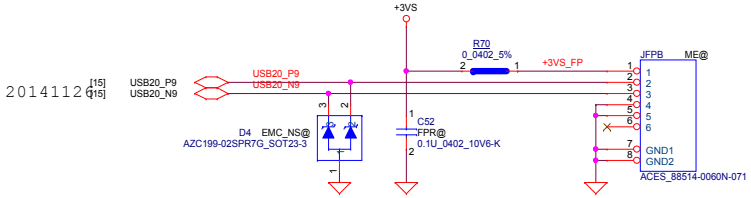
FAN CONN.



For RF solution.



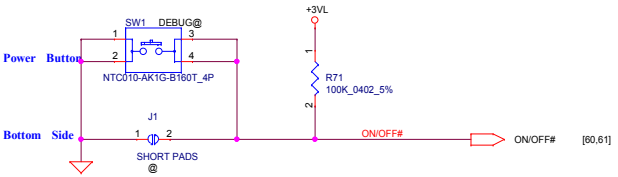
FingerPrint CONN.



PWR BTN/LID SW CONN.

For 14" on board
For 15" on Sub/B

ON/OFF Switch --> 簿Sub/B



Lid Switch --> 簿Sub/B

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Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: PBTN/LID/FP/FAN CONN.

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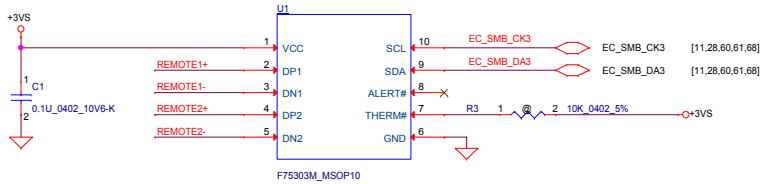
Thermal Sensor

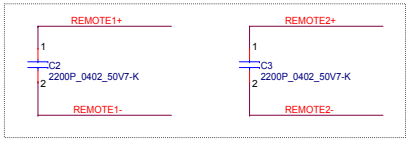
Thermal Sensor
placed near by VRAM



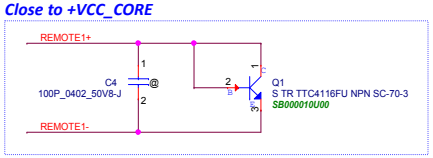
Address 1001_101xb

Internal pull up 1.2K to 1.5V
R for init i d ther mal shut do wn t e mp

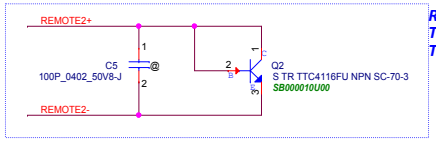
Close to U1



Close to +VCC_CORE



Close JDIMM1&JDIMM2



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

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Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: *Thermal Sensor*

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15/0525

+3VS

RC413
10K_0402_5%

[14,61] CP_BYPASS

+5VS

R63 4.7K_0402_5% TP_CLK2

R65 4.7K_0402_5% TP_DATA2

AMD TP_REST has PU

R67 100K_0402_5% CP_RESET#

TP_REST R64 0_0402_5% TP_RESET

R66 @ 0_0402_5% BYPASS_PAD

R105 0_0402_5%

Track point

+3VS

R60 4.7K_0402_5%

+5VS

R59 @ 4.7K_0402_5%

TP_DATA2
TP_RESET
TP_CLK2

JTP

20141231

GND1 GND2

JAE_FL10F012HA1R3000
ME@

Click Pad

+5VS

RL20 0_0603_5%

JCP ME@

[11,23,25,26] PM_SMB_CLK
[11,23,25,26] PM_SMB_DAT
[14,61] CP_RESET#
[61] CP_CLK
[61] CP_DATA
[14,61] TP_REST

PM_SMB_CLK
TP_DATA2
TP_CLK2
PM_SMB_DAT
CP_RESET#
CP_CLK
CP_DATA
TP_REST
BYPASS_PAD

R61 4.7K_0402_5% @

C44 @ 100P_0402_50V8J

C45 100P_0402_50V8J

GND1 GND2

ACES_50506-01201-AT1

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: CP/TPOINTCONN.

Size	Document Number	Rev
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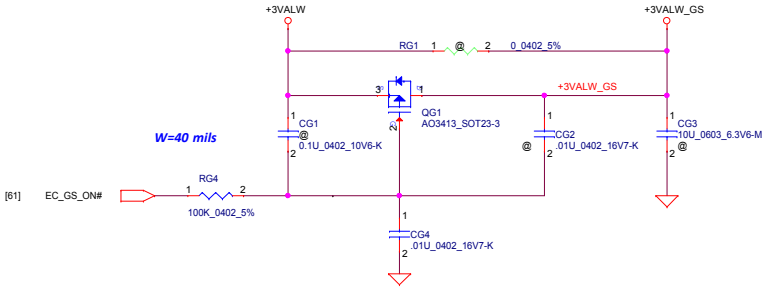
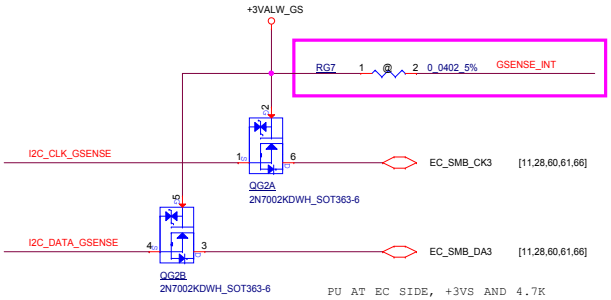


APS G-Sensor

TABLE

P/N	ADDR_SEL	Address
LIS3DH	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX023-1025	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)

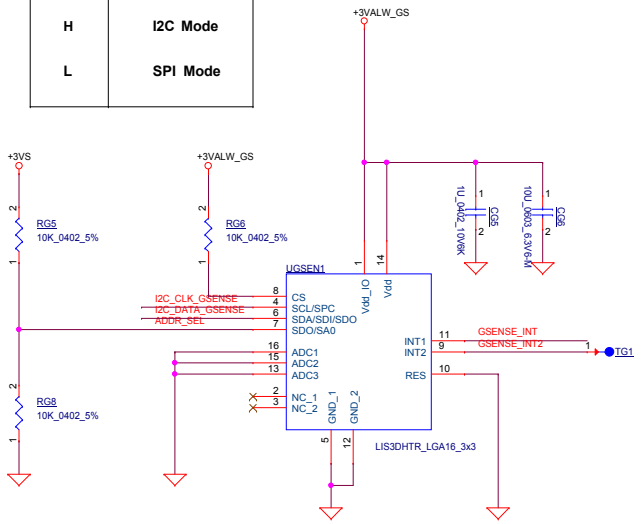


PU AT EC SIDE, +3VS AND 4.7K

20141204

TABLE

P/N	Mode Selection
H	I2C Mode
L	SPI Mode



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: G SENSOR

Size	Document Number	Rev
Custom	BE560	0.1

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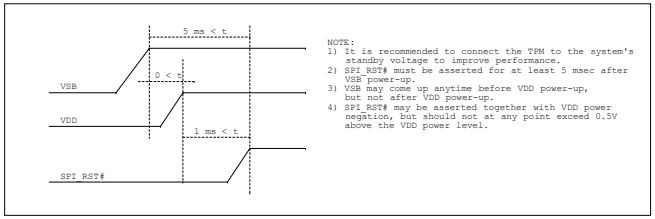
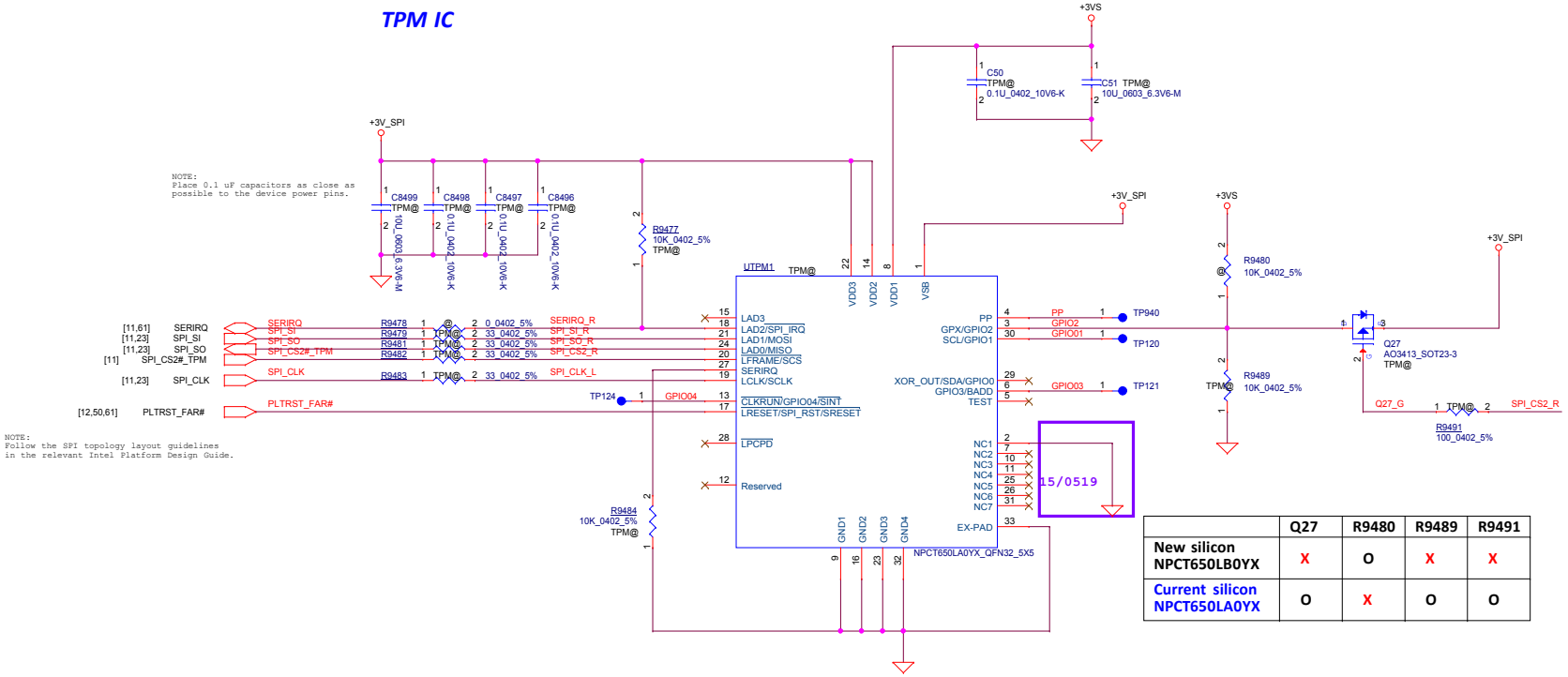


TPM IC



	Q27	R9480	R9489	R9491
New silicon NPCT650LB0YX	X	O	X	X
Current silicon NPCT650LA0YX	O	X	O	O

Security Classification	LC Future Center Secret Data		
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Title: TPM

Size	Document Number	Rev
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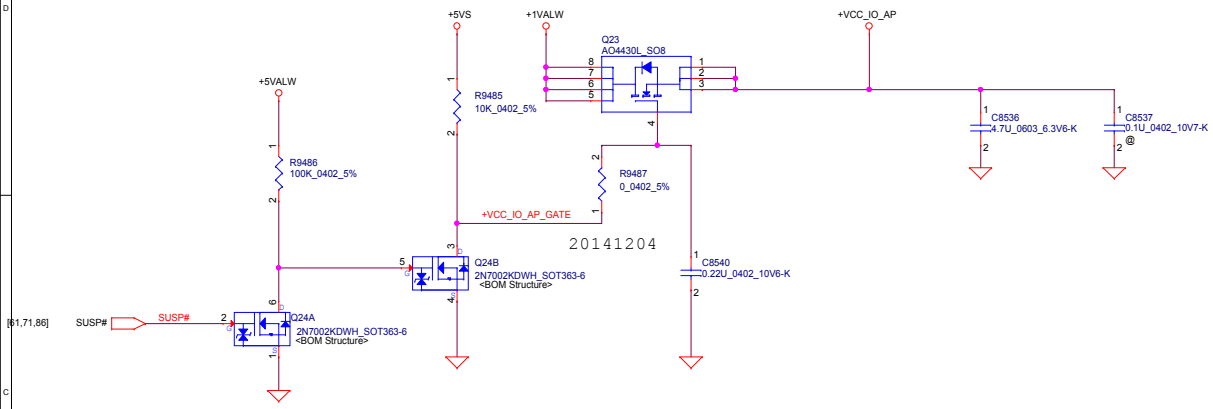
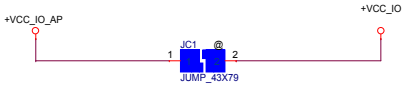
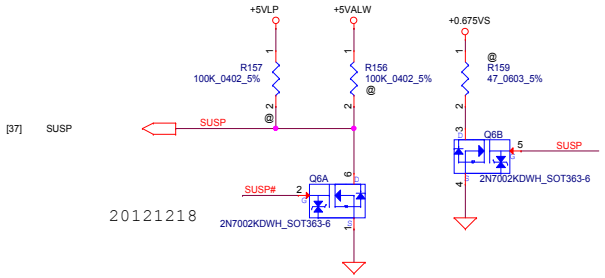
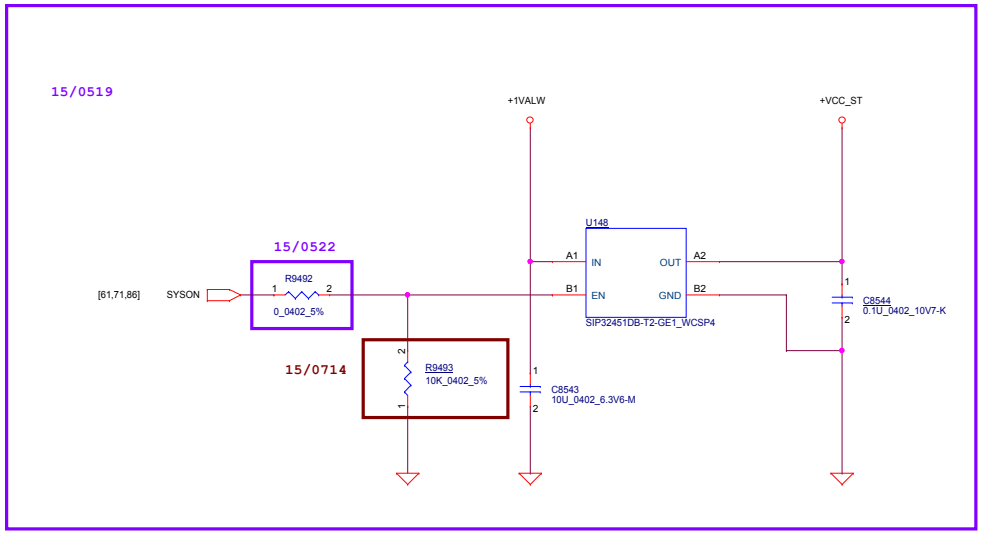
+1VALW to +VCC_IO_AP

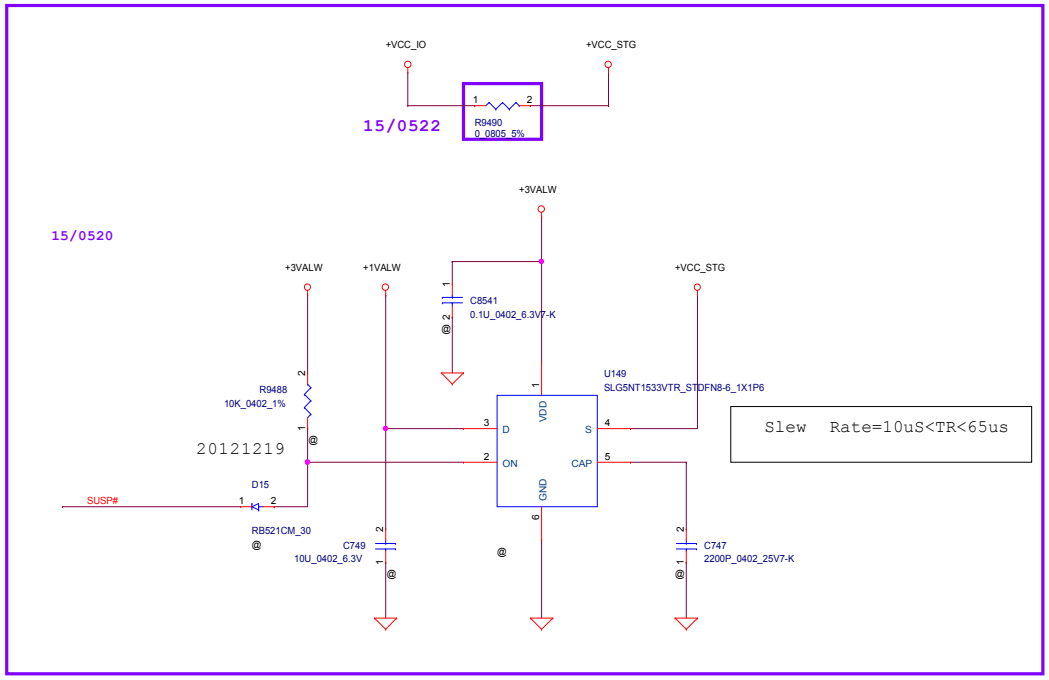
3A











Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: VCC_IO and VCC_ST LSW

Size: Custom | Document Number: BE560 | Rev: 0.1

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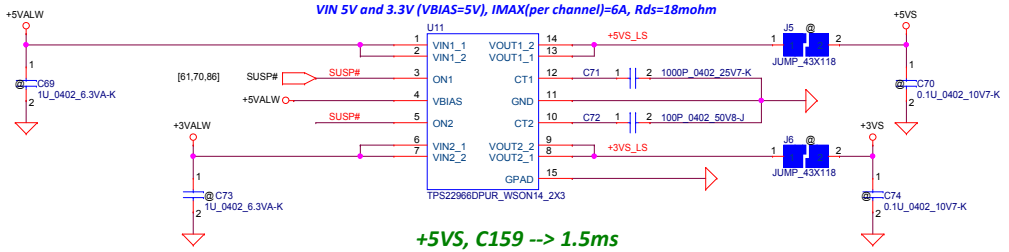
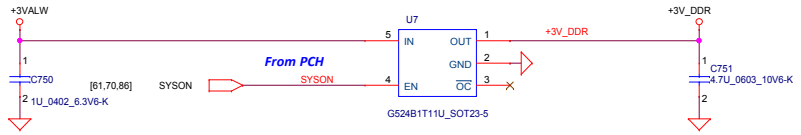
Load Switch
+5VALW To +5VS
+3VALW To +3VS



+3VALW to +3V_DDR



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: ***DC V TO VS/ V-PCH/VM***

Size	Document Number	Rev
Custom	***BE560***	0.1

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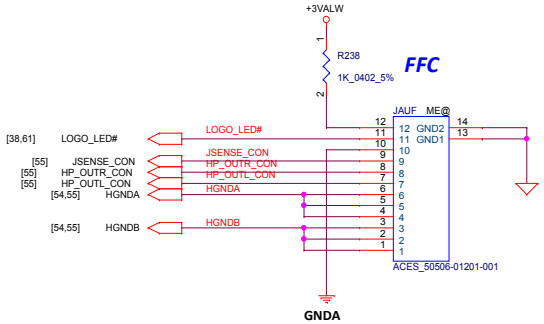
For Edge 15'' Audio board CONNECTOR



Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: **SUB-AUDIO JACK CONN.**

Size	Document Number	Rev
Custom	BE560	0.1

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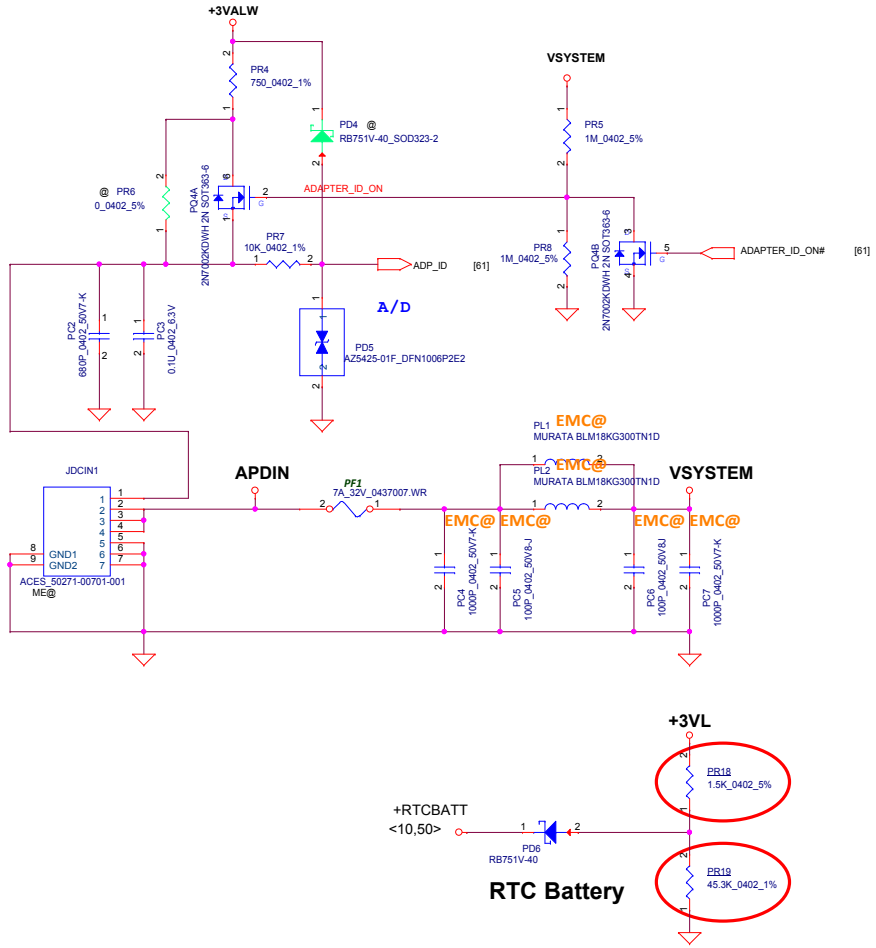

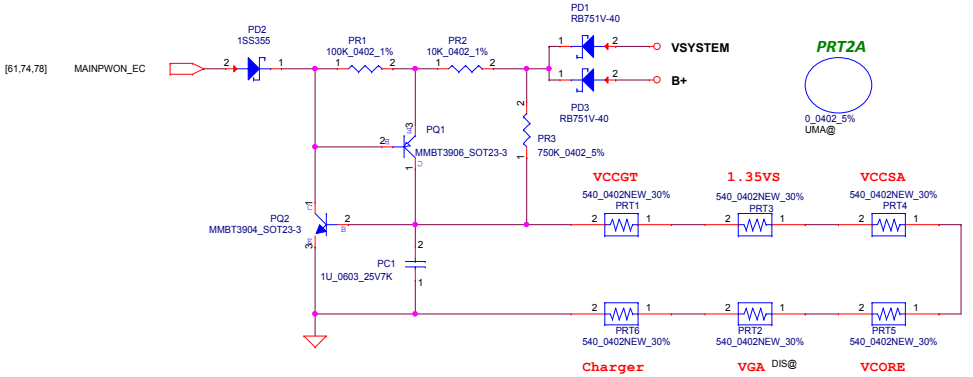

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: DCIN / Vin Detector

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

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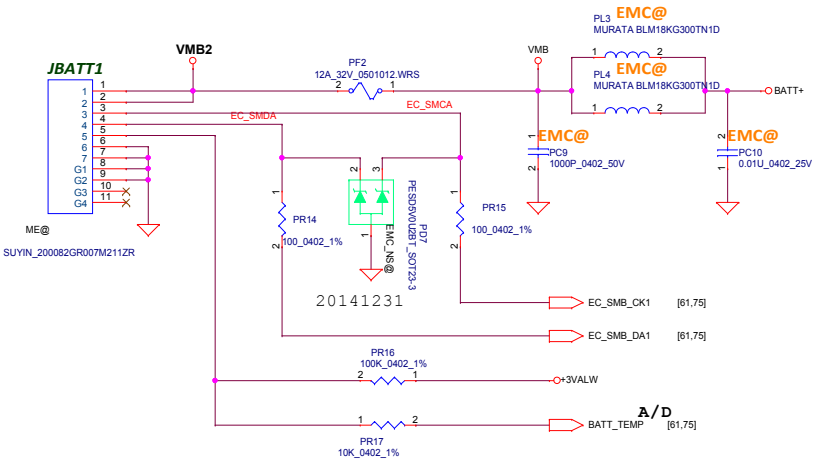
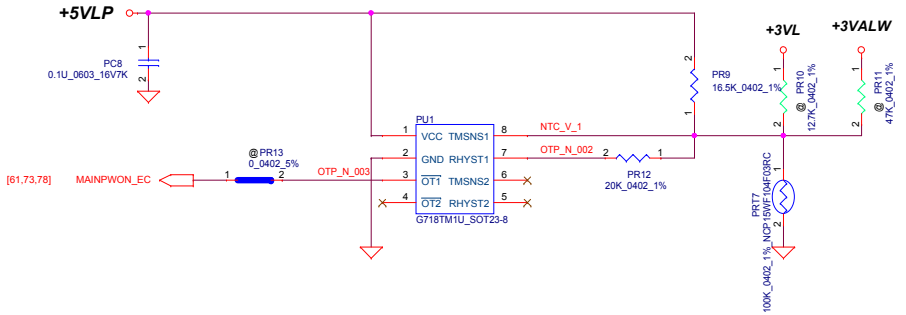


PRT7 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **BATTERY CONN/OTP**

Size	Document Number	Rev
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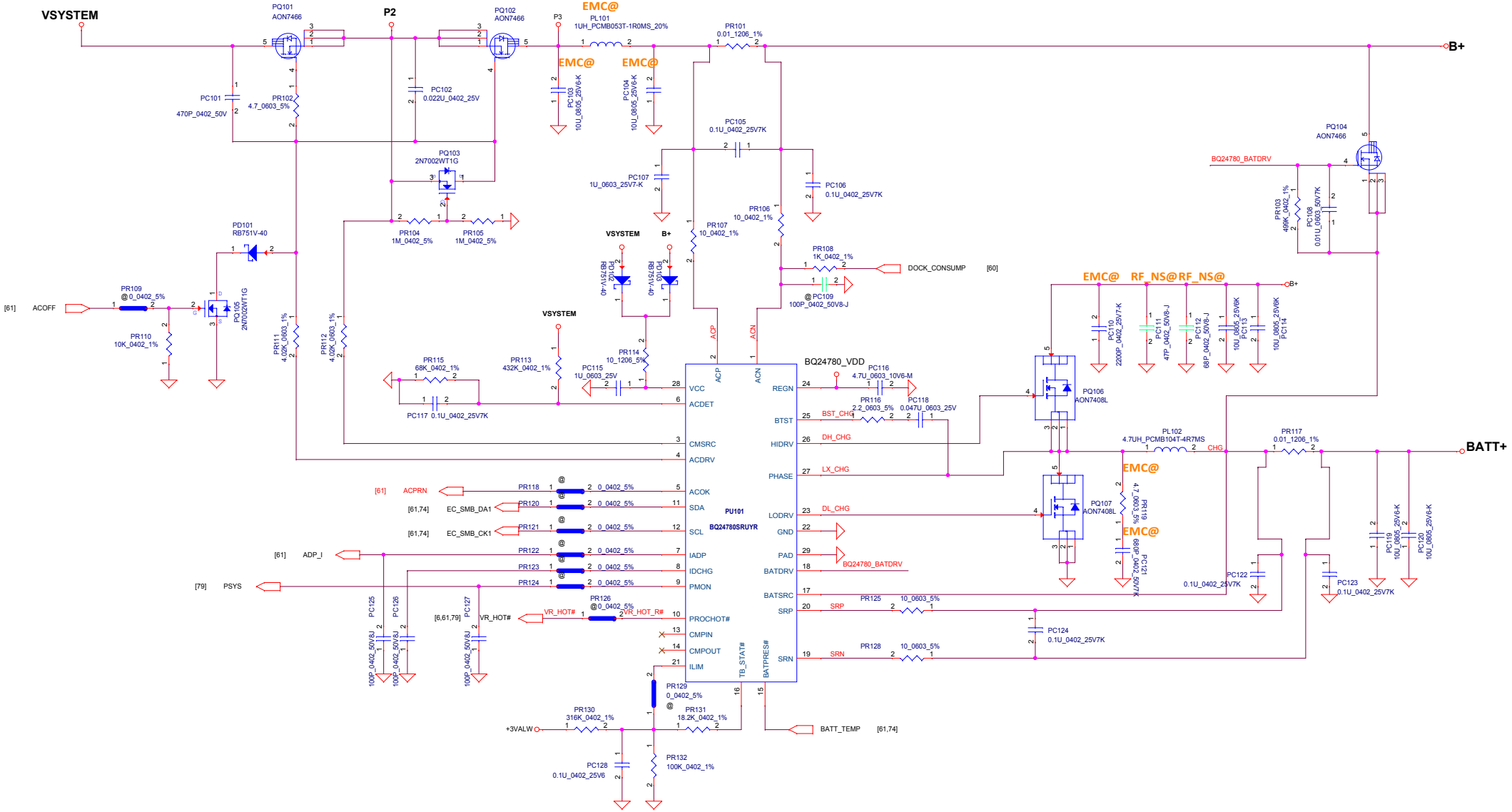

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Issued Date	2013/08/05	Deciphered Date	2014/12/31

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Title	CHARGER	
Size: Custom	Document Number: AIVL2 NM-A351	Rev: 0.1
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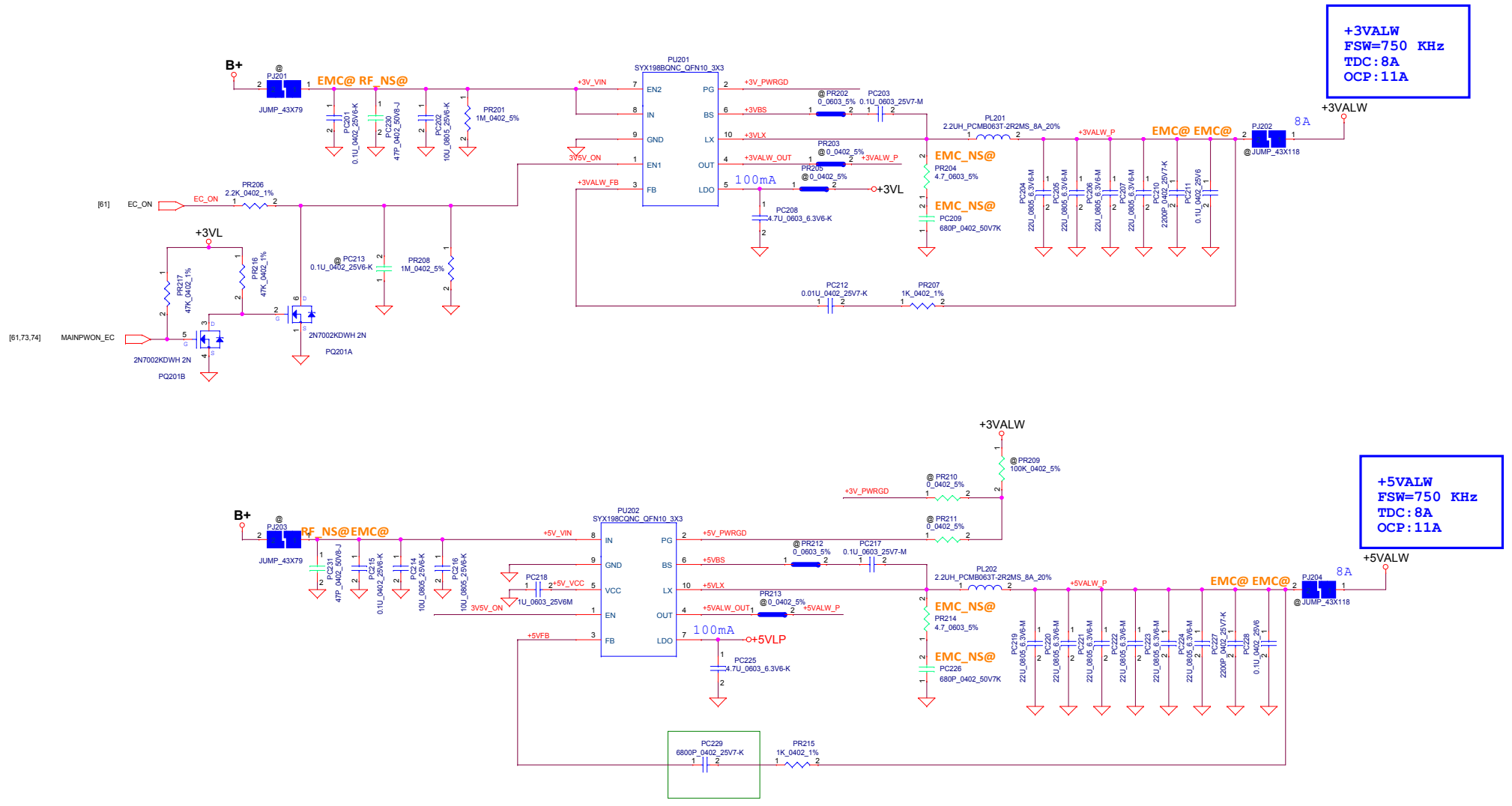
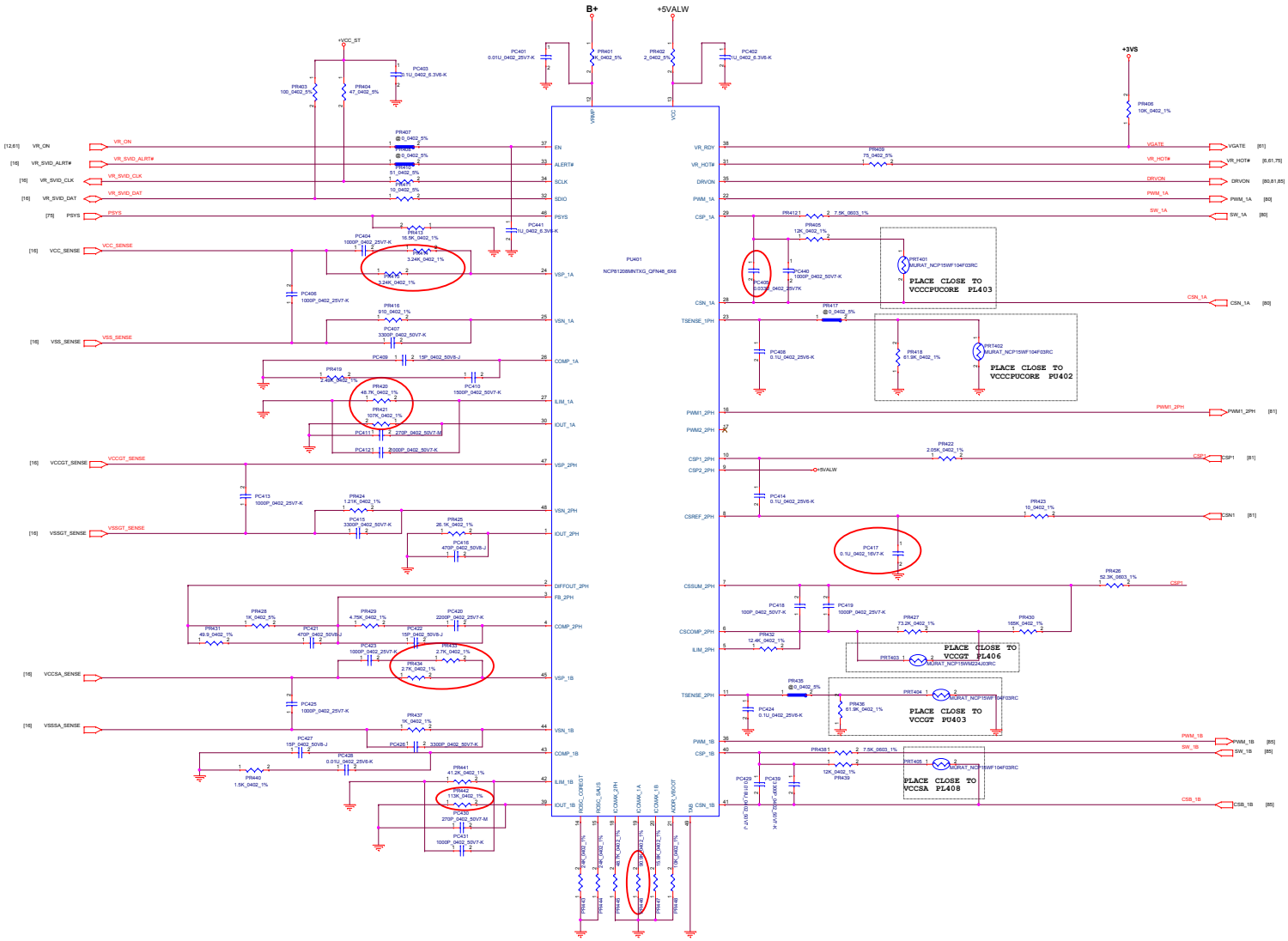


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

Date: Wednesday, September 23, 2015 | Sheet 78 of 99



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

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Title: MVP8

Size: V1 | Document Number: AIVL2 NM-A351 | Rev: 0.1

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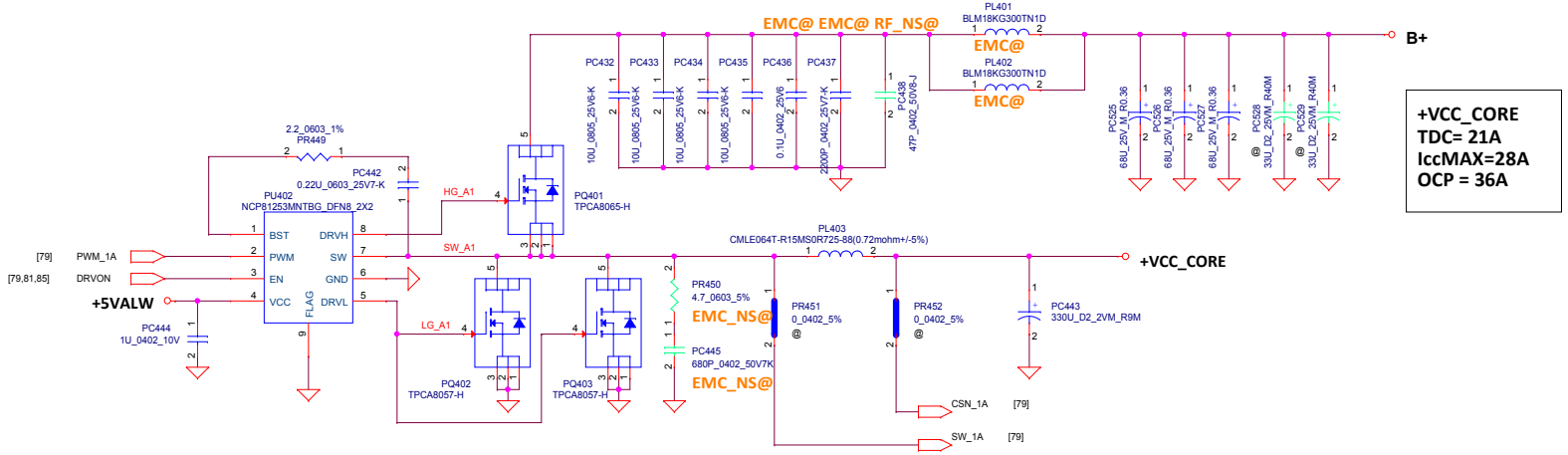

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_CORE

Size: Custom | Document Number: AIVL2 NM-A351 | Rev: 0.1

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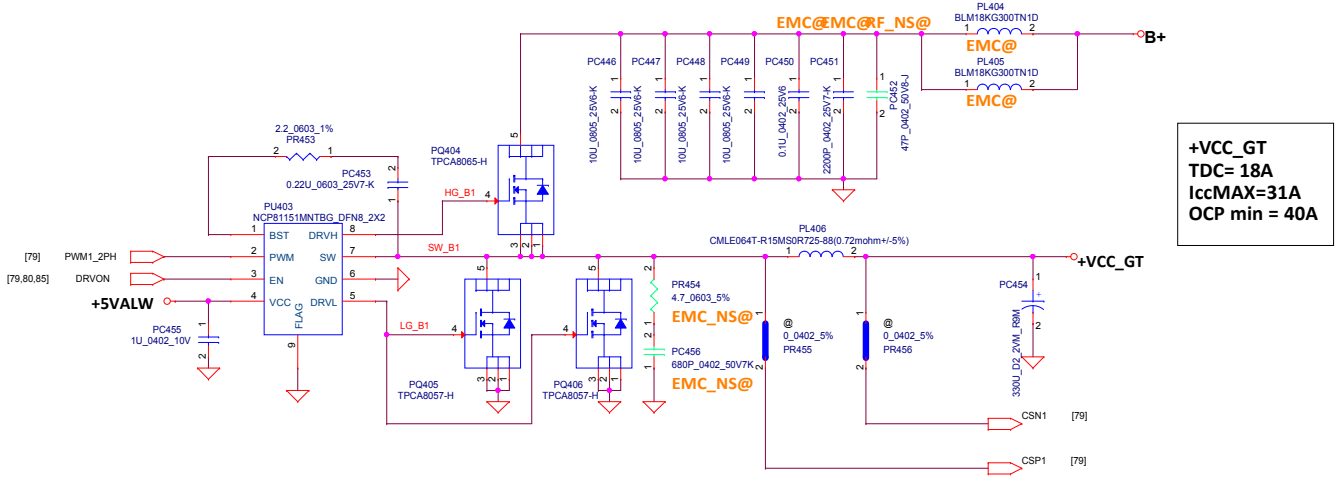

+VCC_GT
TDC= 18A
IccMAX=31A
OCP min = 40A

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +VCC_GT

Size: Custom | Document Number: AIVL2 NM-A351 | Rev: 0.1

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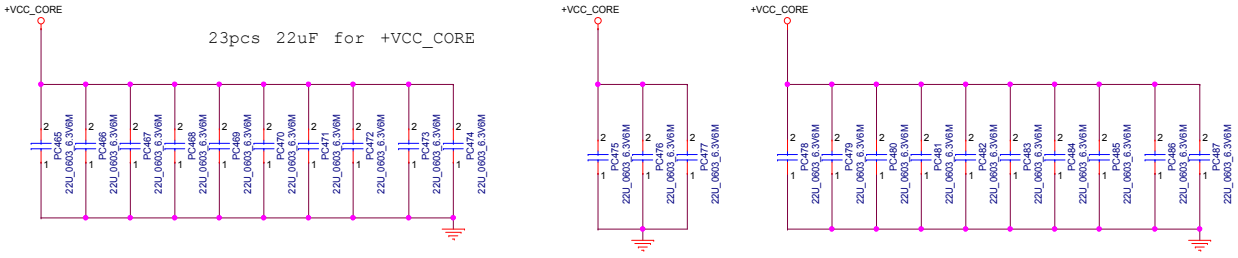
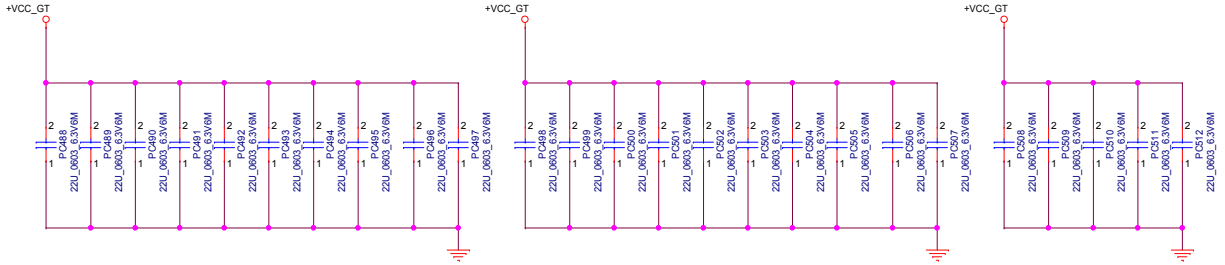
Based on PDDG rev 0.7 Table 5-1.

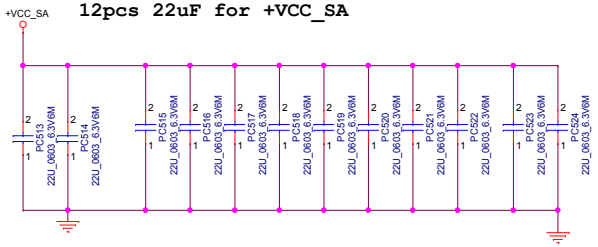
23pcs 22uF for +VCC_CORE



25pcs 22uF for +VCC_GT



12pcs 22uF for +VCC_SA



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: **PROCESSOR DECOUPLING**

Size	Document Number	Rev
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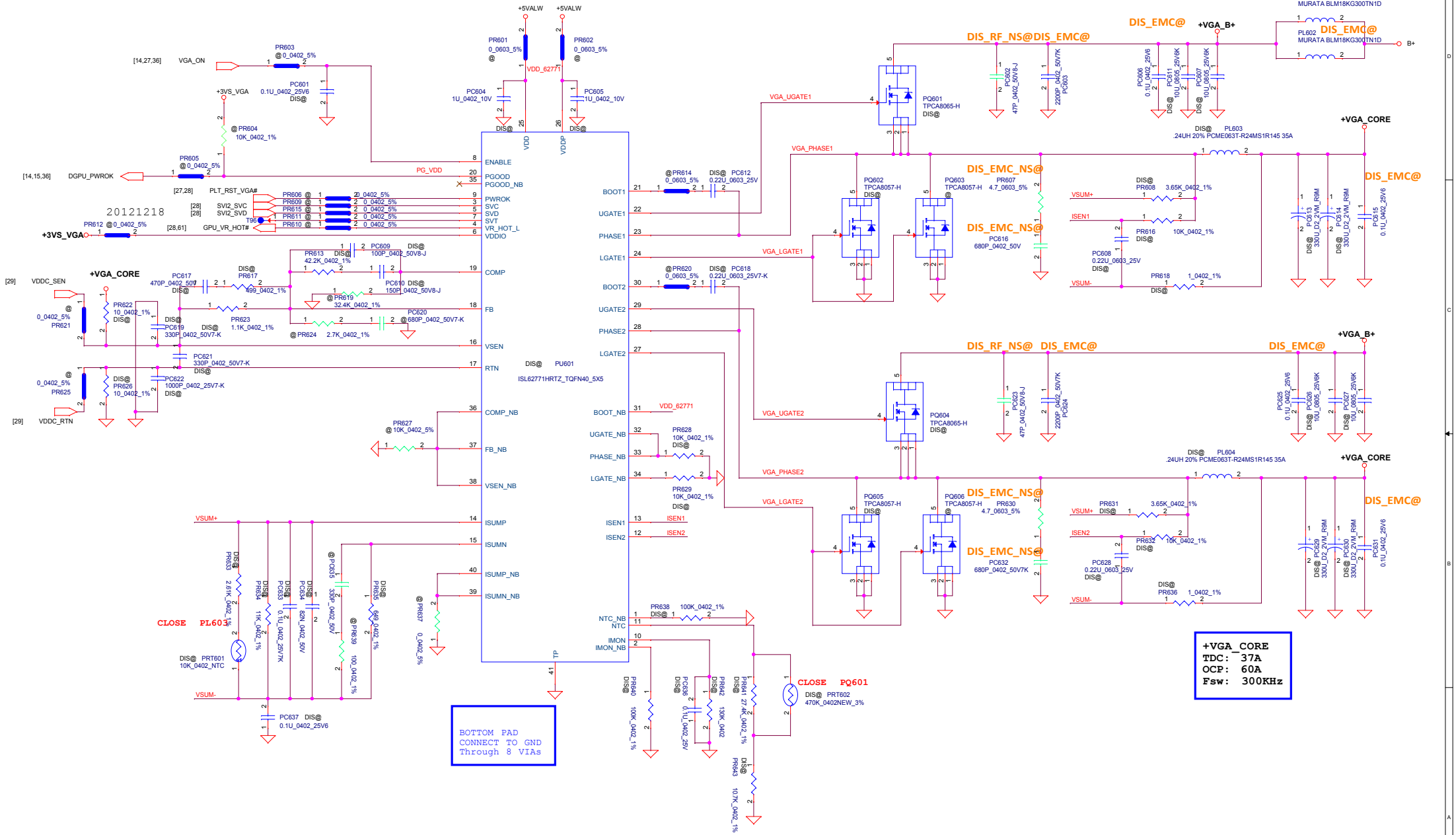
ISL62771 Schematic for FT3 solution



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+VGA_CORE		
Size Custom	Document Number	AIVL2 NM-A351	Rev 0.1
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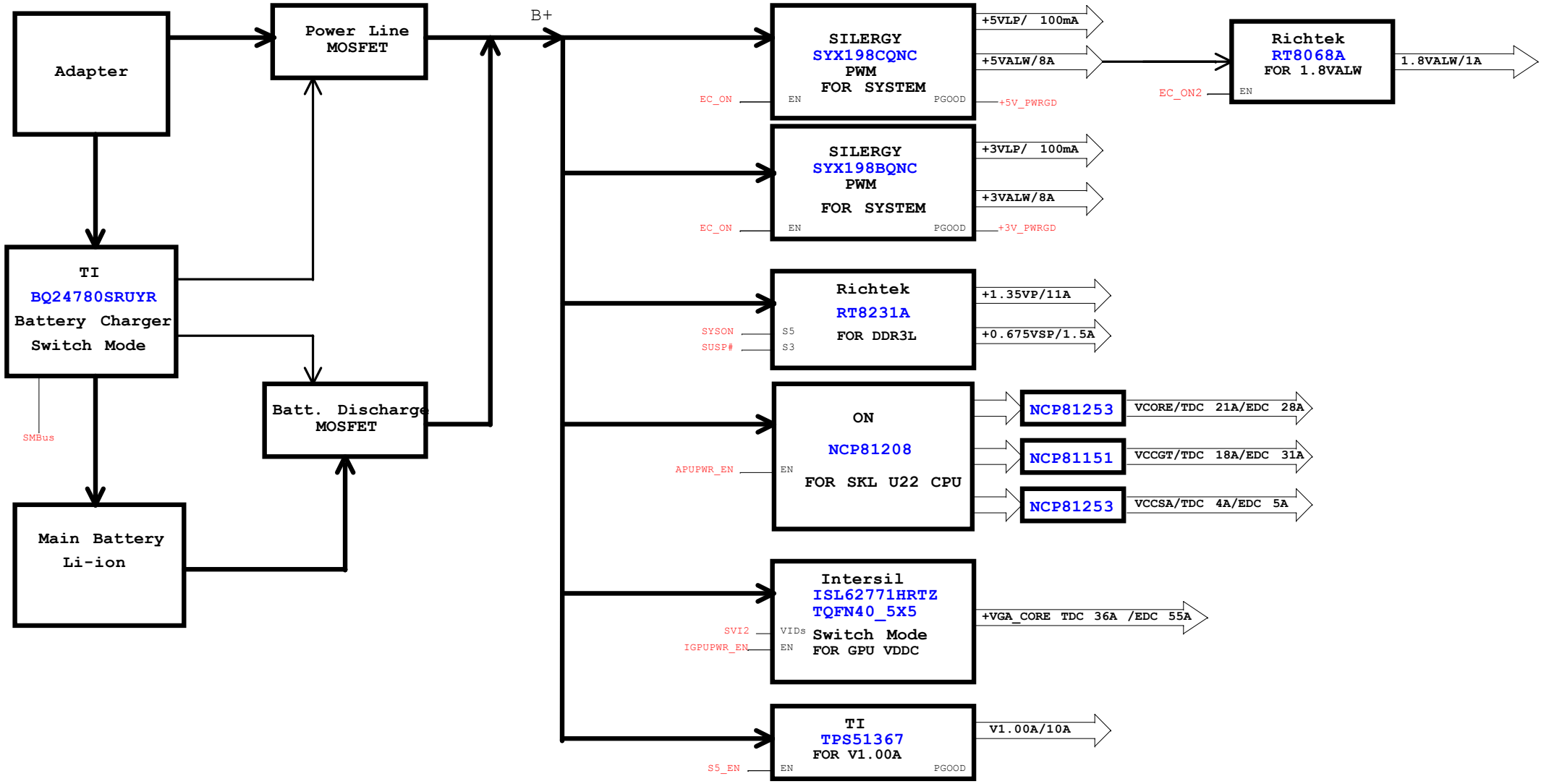
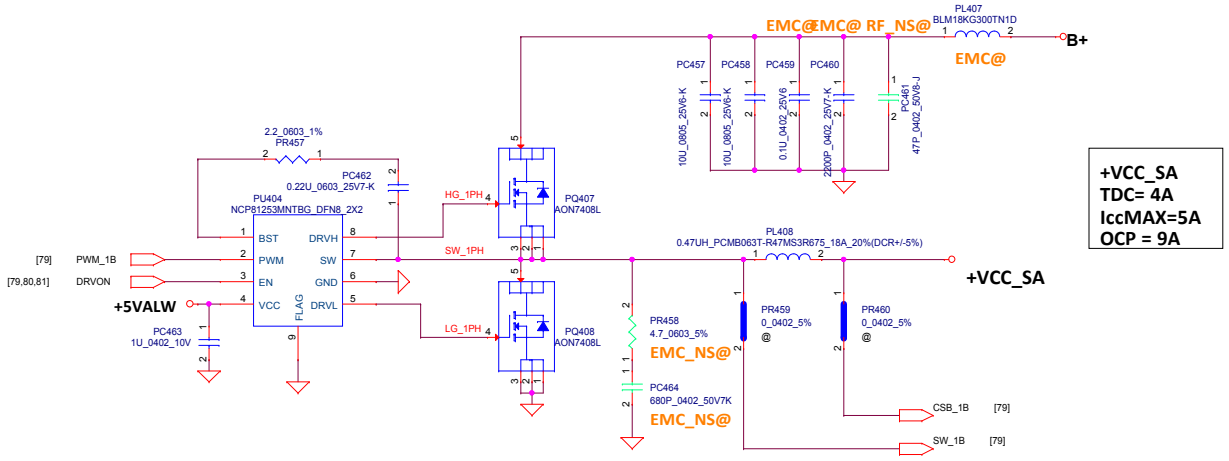


Title		
Block Diagram		
Size: Custom	Document Number: *AIVL2_NM-A351*	Rev: 0.1
Date: Wednesday, September 23, 2015	Sheet 84 of 99	



Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: VCCSA

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

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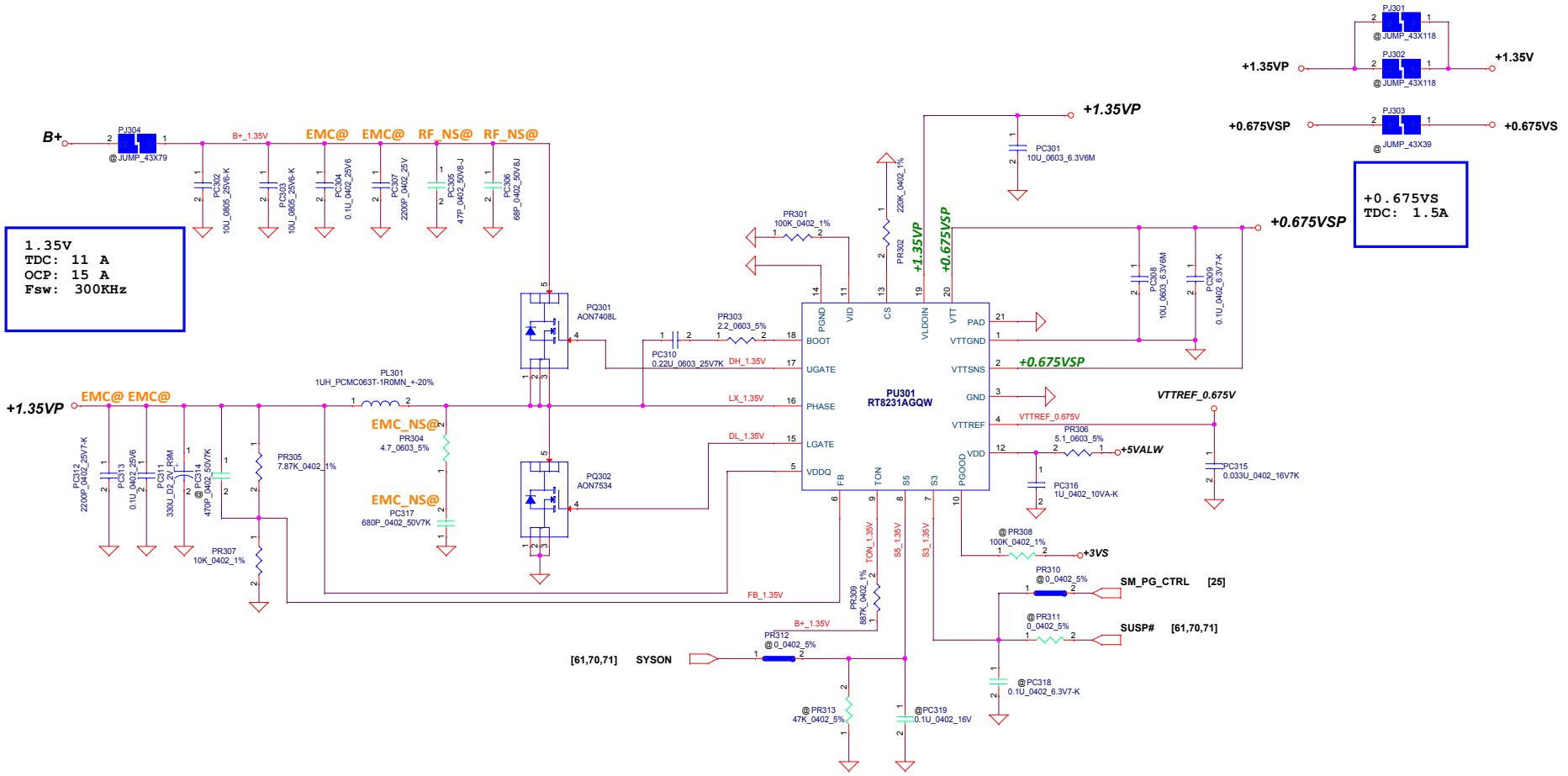
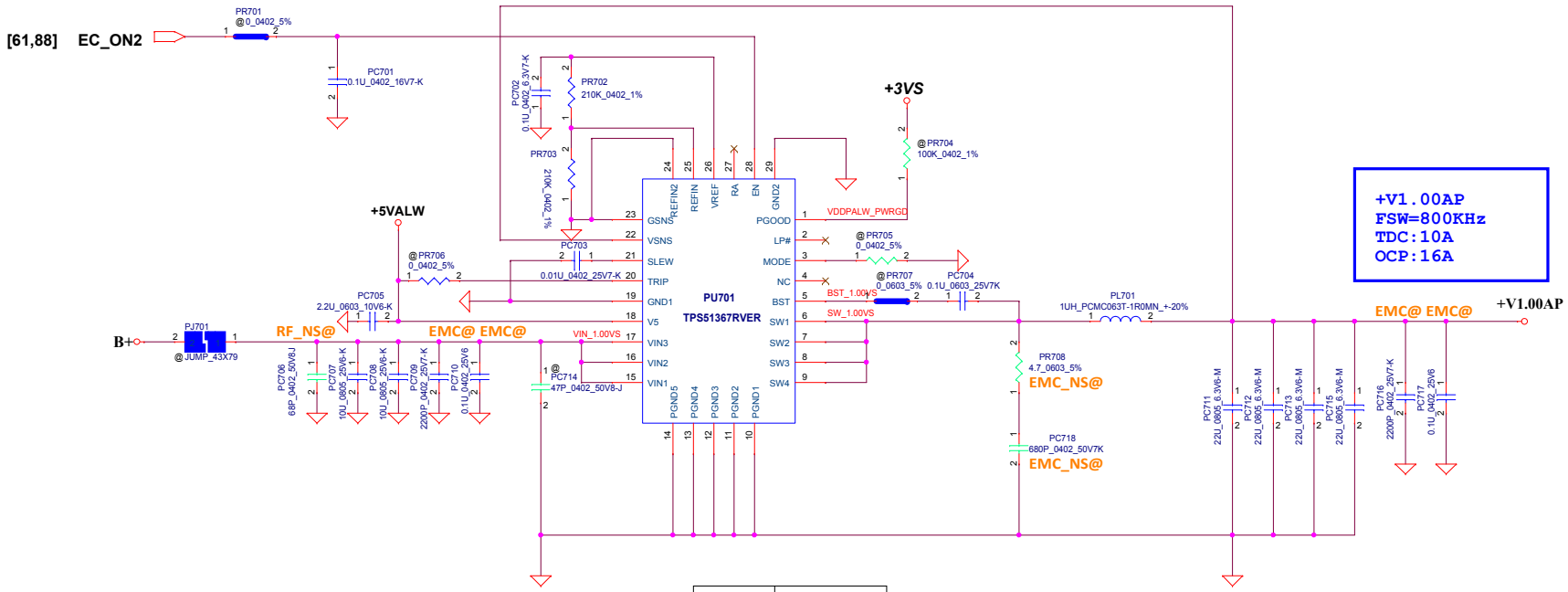


Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title	+1.35V/+0.675VS		
Size	Document Number		Rev
Custom	AIVL2 NM-A351		0.1
Date:	Wednesday, September 23, 2015	Sheet	86 of 99



Mode	Frequency
GND	400KHz
Float	800KHz

Title			
+V1.00A			
Size: Custom	Document Number: AIVL2 NM-A351		Rev: 0.1
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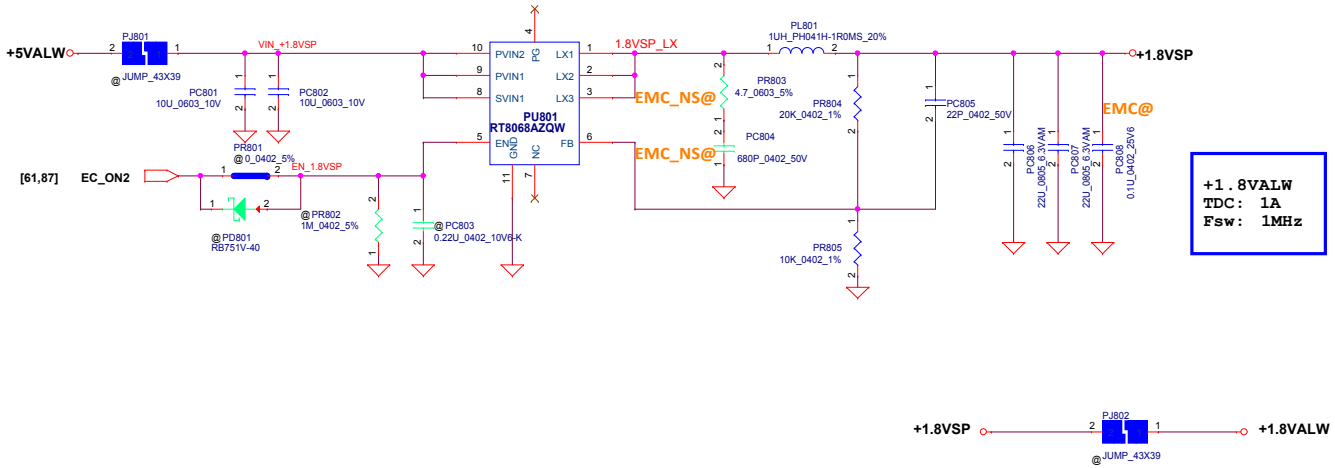

+1.8VALW
TDC: 1A
Fsw: 1MHz

Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/05	Deciphered Date	2014/12/31

Title: +1.8VS_VGA

Size	Document Number	Rev
Custom	AIVL2 NM-A351	0.1

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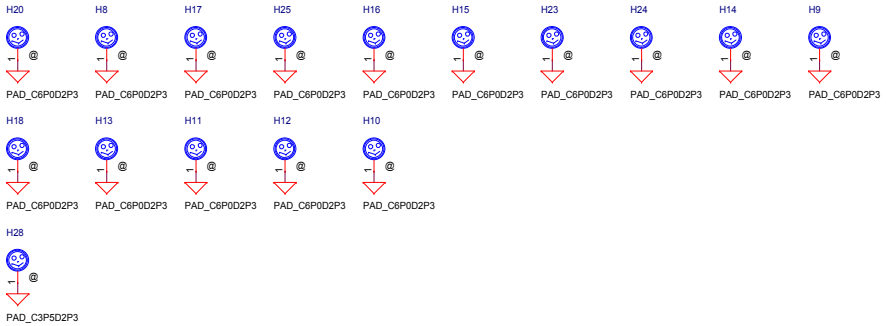
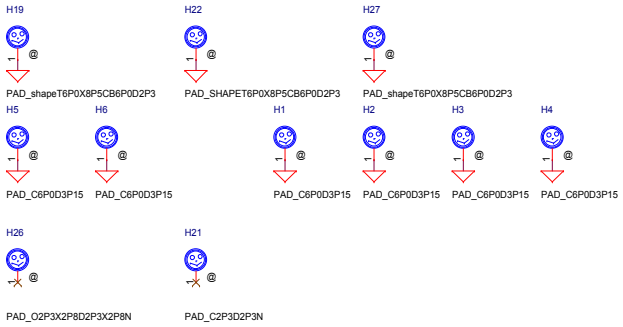
Screw Hole





Center Zero

PCB Fedical Mark PAD

Security Classification	LC Future Center Secret Data		
Issued Date	2013/09/07	Deciphered Date	2014/09/07

Title: XXXX

Size	Document Number	Rev
Custom	BE560	0.1

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