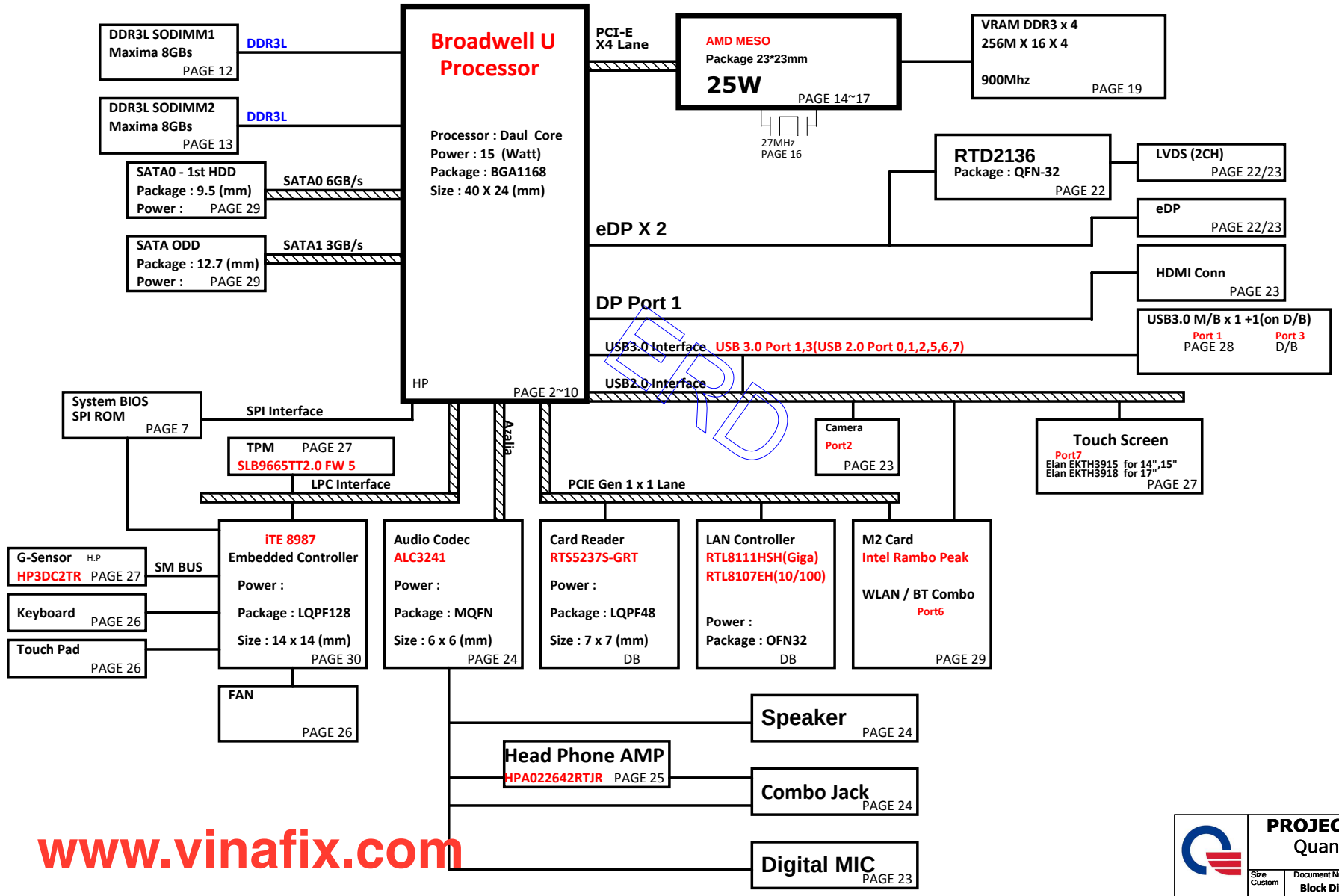
X11 DIS (14" / 15" / 17") Chocolate X11
Intel Cresent Bay ULT Platform Block Diagram



Note

VGA/CPU need check PN

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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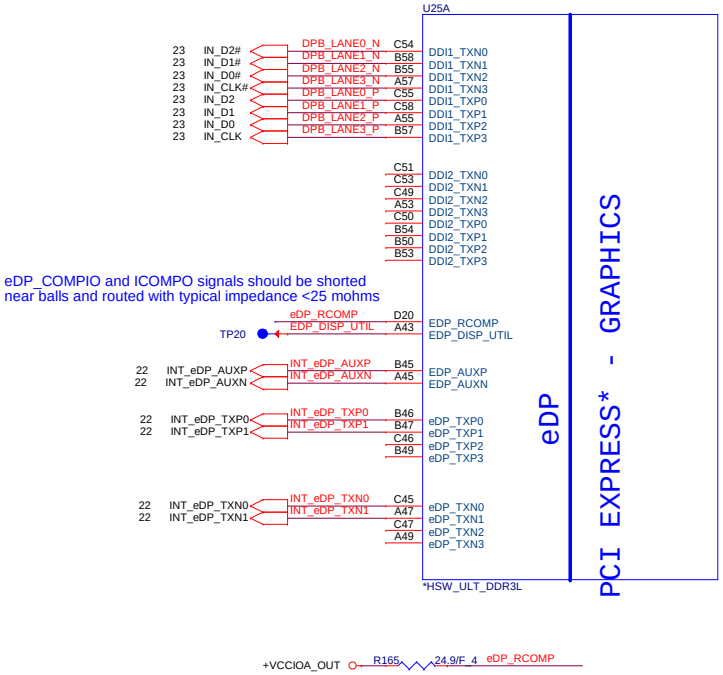
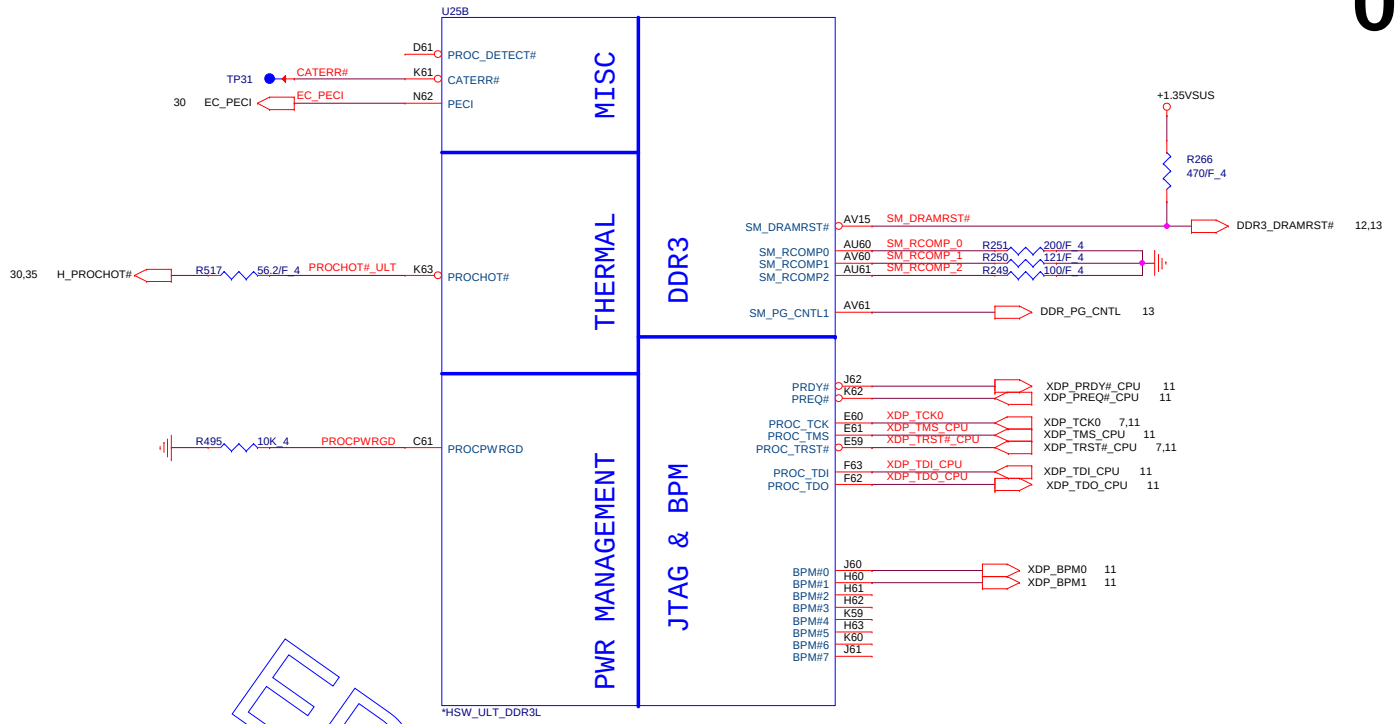
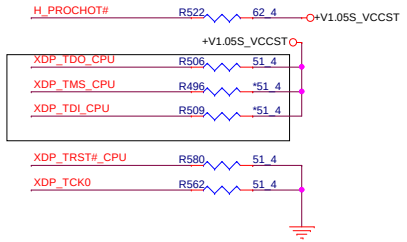


eDP_COMPIO and ICOMPO signals should be shorted
near balls and routed with typical impedance <25 mohms



Processor pull-up (CPU)



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Size	Document Number	Rev
Custom	ULT 1/9(eDP/DDI)	1A

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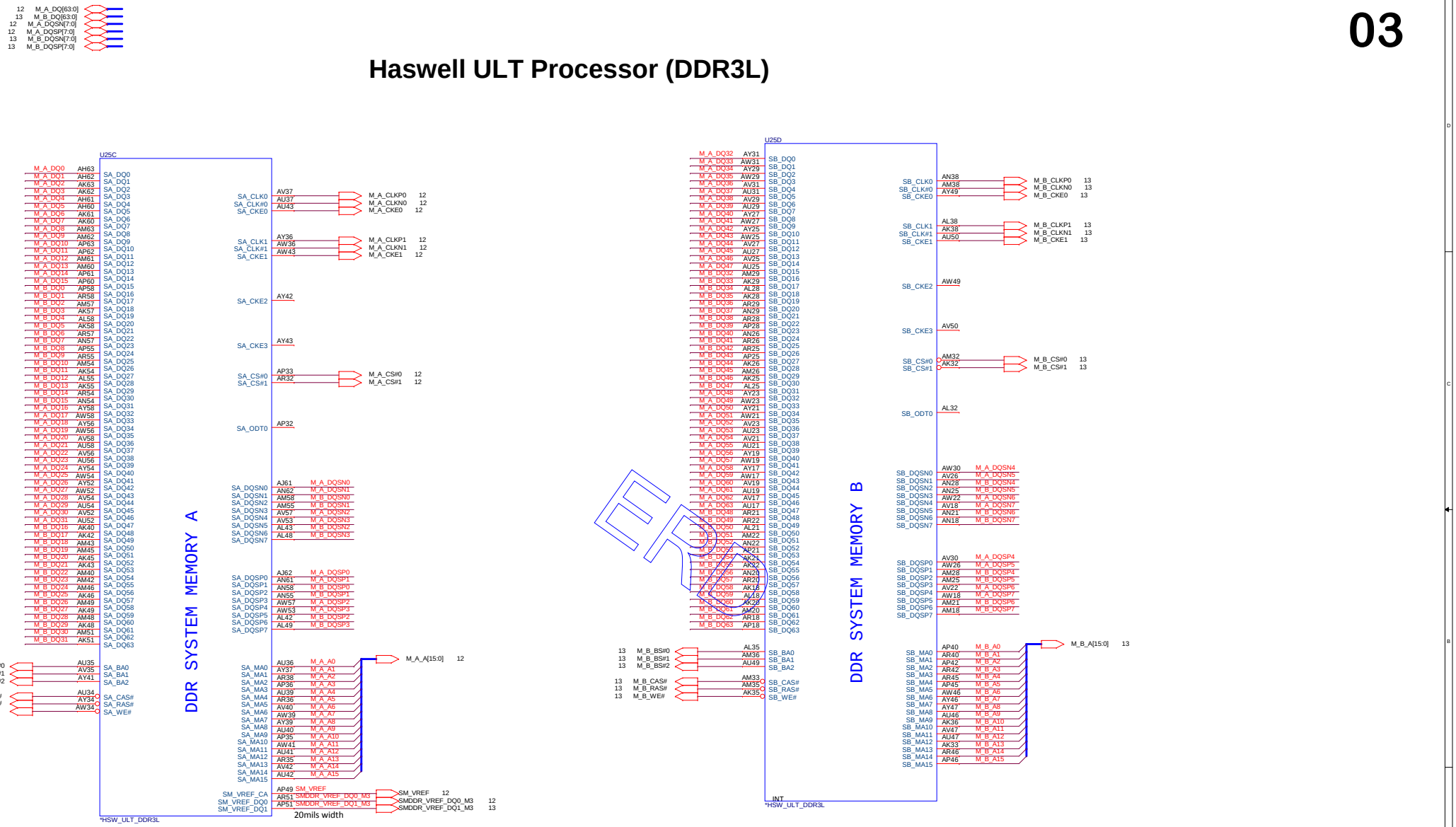
Haswell ULT Processor (DDR3L)



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Quanta Computer Inc.	
Size: Custom	Document Number: ULT 2/9 (DDR3 I/F)
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POWER

HSW ULT POWER

U25F — *HSW_ULT_DDR3L

32A — +VCC_CORE

1.4A — +1.35VSUS

Close to CPU

C738 10U/6.3V_6, C736 10U/6.3V_6, C744 10U/6.3V_6, C743 10U/6.3V_6, C737 10U/6.3V_6, C742 10U/6.3V_6

Direct tie to CPU VCC/VSS-Ball

C746 2.2U/6.3V_4, C739 2.2U/6.3V_4, C745 2.2U/6.3V_4, C740 2.2U/6.3V_4

C249 4.7U/6.3V_4

CFG0-19 need Reserve TP

U25E — *HSW_ULT_DDR3L

RESERVED

R537 49.9/F_4 CFG_RCOMP

R484 8.2K/F_4 TD_IREF

R584 49.9/F_4 PROC_OPI_RCOMP

Layout note: need routing together and ALERT need between CLK and DATA.

SVID ALERT

R533 75/F_4, R531 43_4, H_CPU_SVIDALRT#, VR_SVID_ALERT# 35, C718 *0.1U/16V_4

SVID CLK

VR_SVID_CLK, VR_SVID_CLK 35

SVID DATA

Place PU resistor close to VR

R521 130/F_4, H_CPU_SVIDDAT, VR_SVID_DATA 35

+V1.05S_VCCST

IO Thrm Protect

+3VPCU

For 65 degree, 1.8v limit, (SW)

R276 16.5K/F_4, C370 0.1U/16V_4, R280 3.3K/F_4

For 75 degree, 1.2v limit, (HW)

THRM_MOINTOR1 30, C375 0.1U/16V_4, THER_CPU, R162 100K_4_NTC

100- ±1% pull-up to VCC near processor.

R501 100/F_4 +VCC_CORE, R508 100/F_4

VCC_SENSE E63 — VCC_SENSE 35

VSS_SENSE E62 — VSS_SENSE 35

D2 MEK500V-40, HWPG 11,30,32,33,34, H_VCCST_PWRGD 11

R557 10K_4, C719 *10P/50V_4

+1.05V, +V1.05S_VCCST

C325 *1U/6.3V_4, C330 *22U/6.3V_6

R556 150/F_4, PWR_DEBUG, R555 *10K_4

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (MSR Privacy Bit Feature)	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	CFG3 R543 *1K_4
CFG4 (eDP enable)	Disabled	Enabled	CFG4 R542 1K_4

+VCCIOA_OUT 2
+VCCIO_OUT 6

+1.35VSUS 2,12,13,33
+1.05V 2,7,9,10,11,27,30,34,35,36
+VCC_CORE 35

PROJECT : X11
Quanta Computer Inc.

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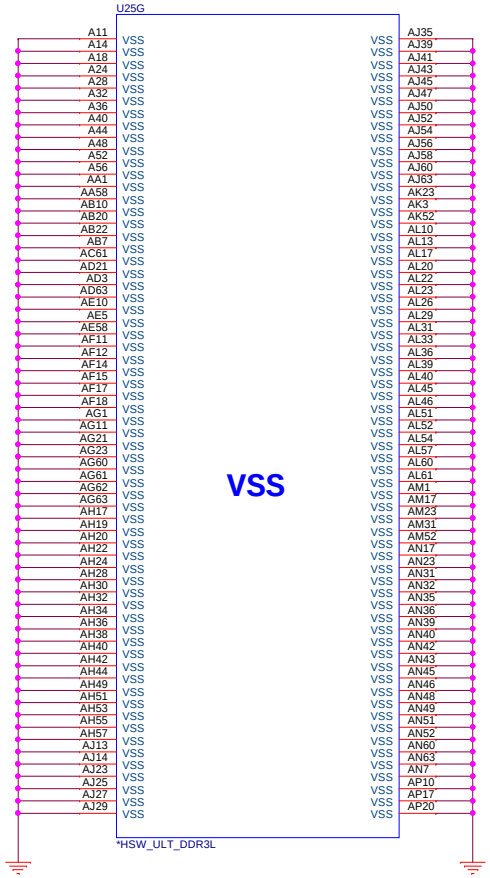

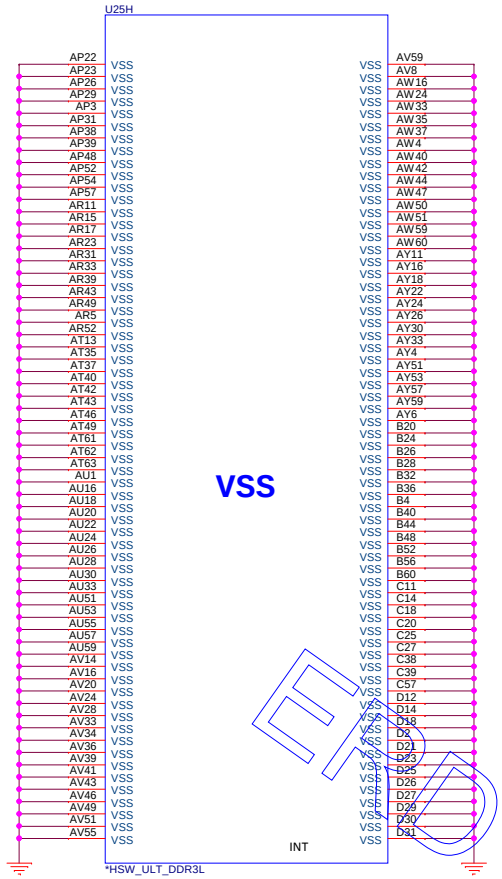

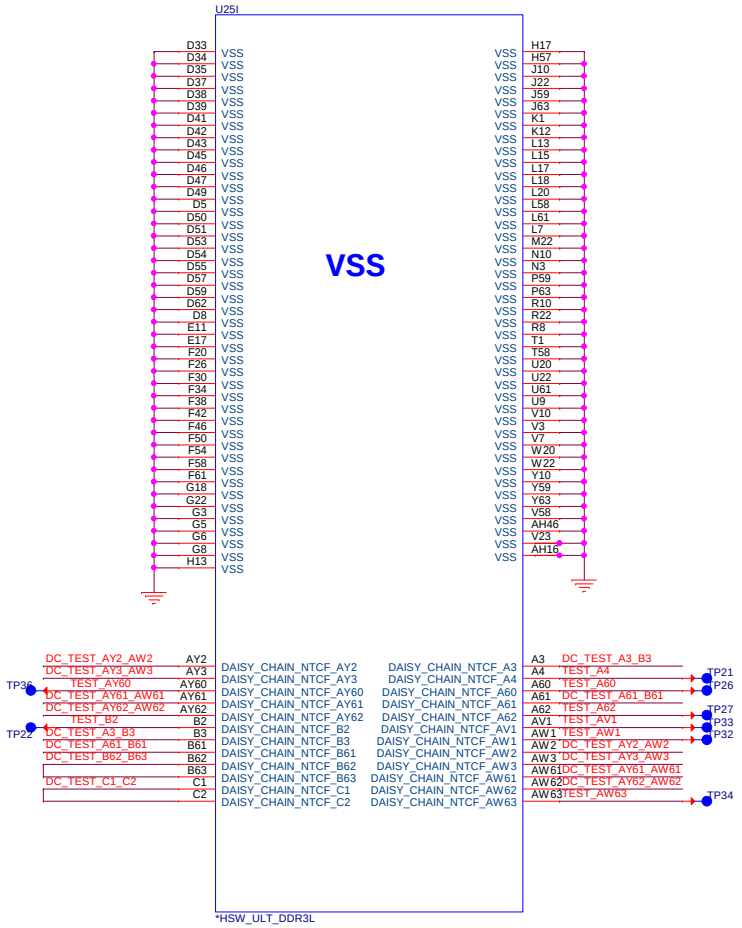

PROJECT : X11		
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Size: Custom	Document Number: ULT 4/9 (RSV,GND)	Rev: 1A
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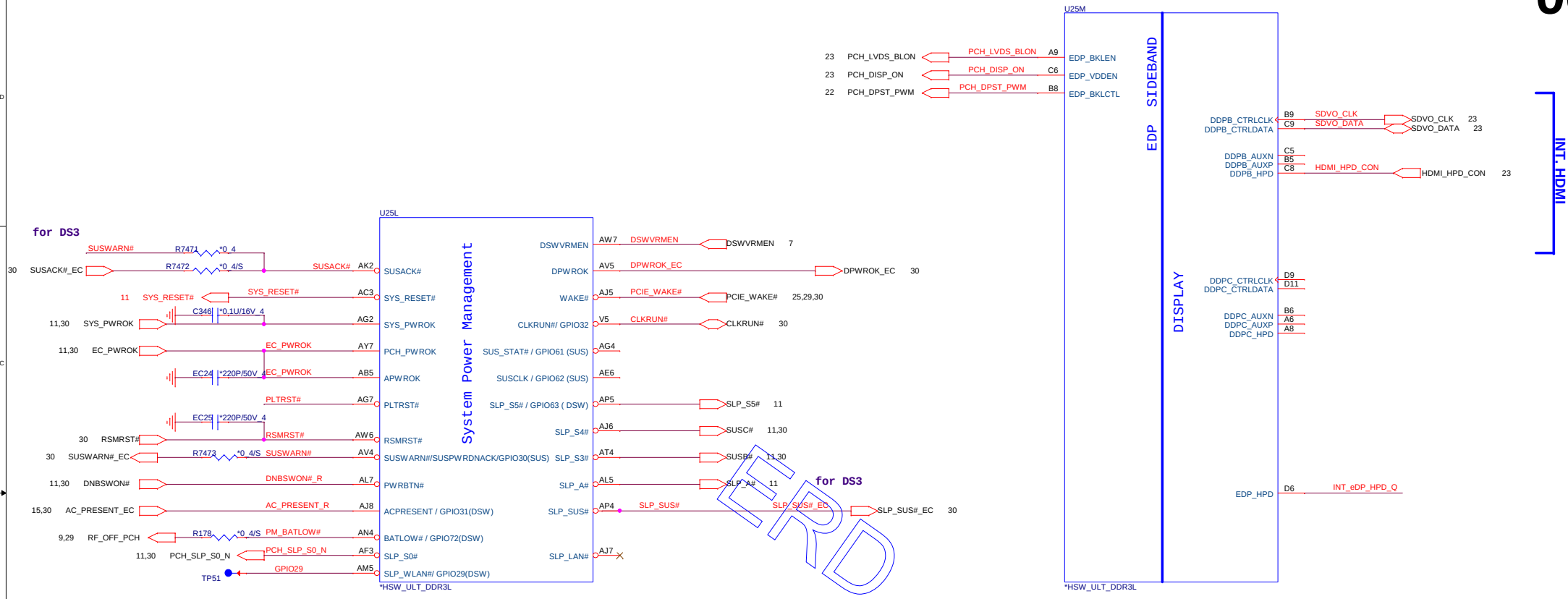
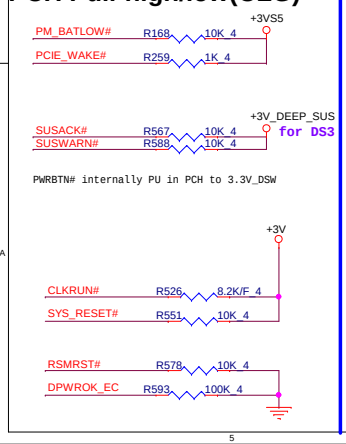
Lynx Point-LP Platform Controller Hub (LVDS,DDI)

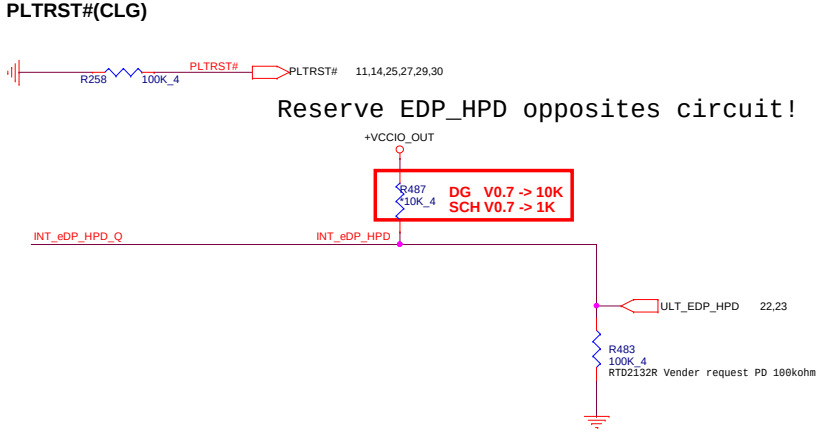
06



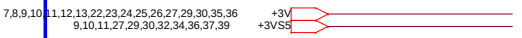
PCH Pull-high/low(CLG)



PLTRST#(CLG)



System PWR_OK(CLG)



PROJECT : X11

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 5/9(Power Manger)	1A

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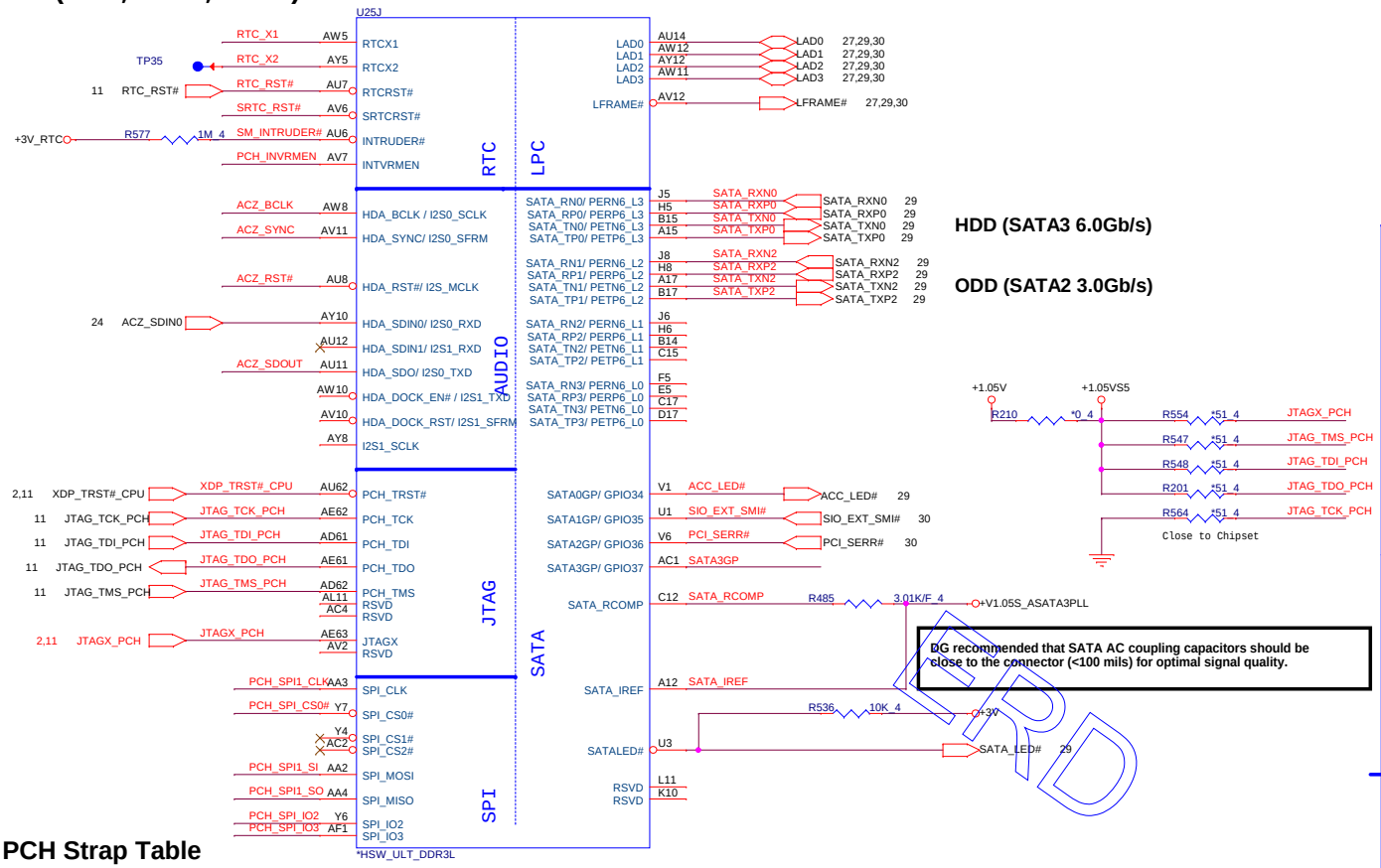
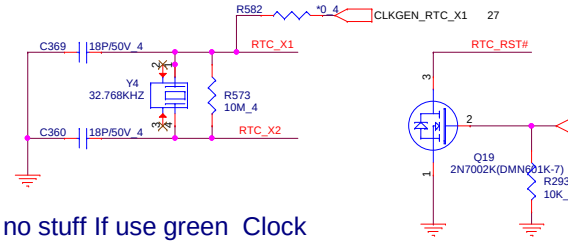
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)



PCH Strap Table

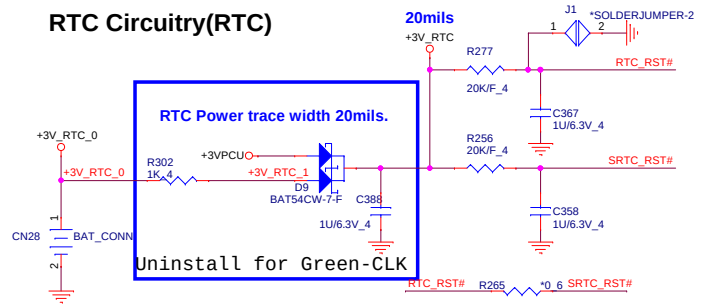
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R575 330K_4 PCH_INVRMEN
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridden	30 GPIO33_EC R581 1K_4 ACZ_SDOUT
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	GNT0# / Boot Location: 1 = LPC, 0 = SPI(Default)	
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality	
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC R576 330K_4 DSWVRMEN 6
				30 PCH_SPI_CS0#_R → PCH_SPI_CS0#_R 30 PCH_SPI1_CLK_R → PCH_SPI1_CLK_R 30 PCH_SPI1_SI_R → PCH_SPI1_SI_R 30 PCH_SPI1_SO_R → PCH_SPI1_SO_R

RTC Clock 32.768KHz

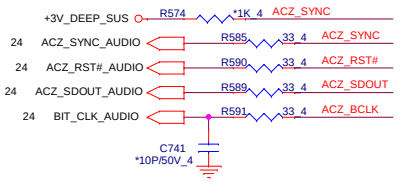


no stuff If use green Clock

RTC Circuitry(RTC)



HDA Bus(CLG)

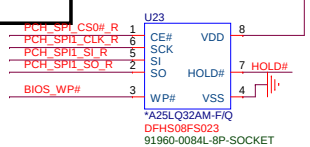


GPIO Pull UP

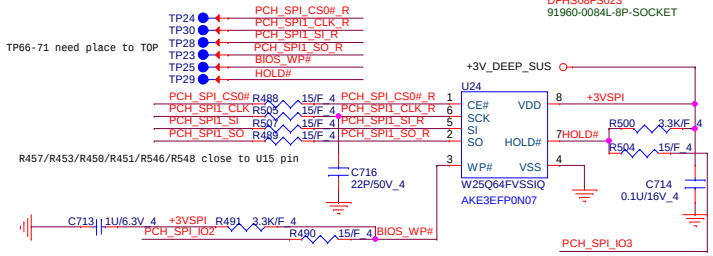
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket

U23&U24 footprint 要重疊



PCH SPI ROM(CLG)



+3V 6,8,9,10,11,12,13,22,23,24,25,26,27,29,30,35,36
+5V 23,24,25,26,29,36

+1.05V 2,4,9,10,11,27,30,34,35,36
+3VS5 6,9,10,11,27,29,30,32,34,36
+3VPCU 4,25,26,27,29,30,31,32
+3V_RTC 10,27
+V1.05S_ASATA3PLL 10

PROJECT : X11
Quanta Computer Inc.

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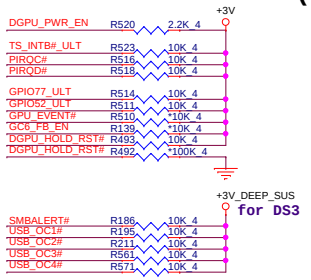
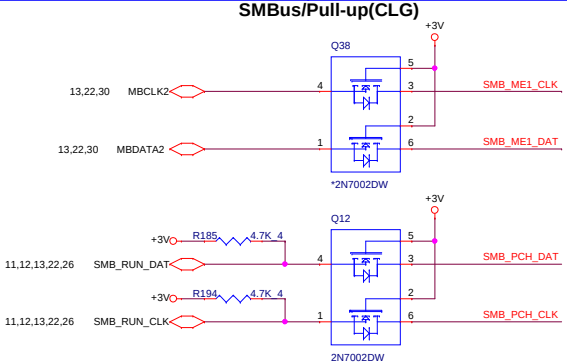
Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

08

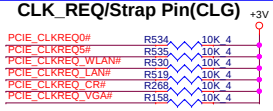
PCI/USBOC# Pull-up(CLG)

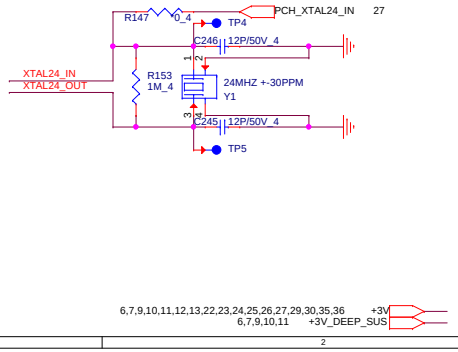


SMBus/Pull-up(CLG)

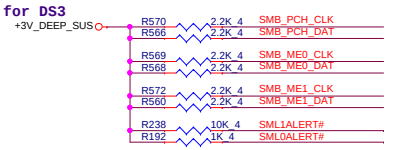


CLK_REQ/Strap Pin(CLG)





SMBus/Pull-up(CLG)



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Quanta Computer Inc.			
Size: Custom	Document Number: ULT 7/9 (PCIE/USB/CLK)		Rev: 1A
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Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)

09

U25O

GPIO8(SUS)
GPIO9(SUS)
GPIO10(SUS)
LAN_PHY_PWR_CTRL / GPIO12(DSW)
GPIO13(SUS)
GPIO14(SUS)
GPIO15(SUS)
GPIO16
GPIO17
GPIO24 (SUS)
GPIO25(DSW)
GPIO26(SUS)
GPIO27(DSW)
GPIO28(SUS)
DEVSLP0/ GPIO33
DEVSLP1/ GPIO38
DEVSLP2/ GPIO39
GPIO44(SUS)
GPIO45(SUS)
GPIO46(SUS)
GPIO47(SUS)
GPIO48
GPIO49
GPIO50
GPIO56(SUS)
GPIO57(SUS)
GPIO58(SUS)
GPIO59(SUS)
SDIO_POWER_EN/ GPIO70
HSIOPC/ GPIO71
BMBUSY# / GPIO76
SPKR/ GPIO81

GPIO

THRMTRIP#
RCIN# GPIO82
SERIRQ
PCH_OPI_RCOMP
RSVD
RSVD

CPU/MISC

GSPI0_CS/ GPIO83
GSPI0_CLK/ GPIO84
GSPI0_MISO/ GPIO85
GSPI0_MOSI/ GPIO86
GSPI1_CS/ GPIO87
GSPI1_CLK/ GPIO88
GSPI1_MISO/ GPIO89
GSPI1_MOSI/ GPIO90
UART0_RXD/ GPIO91
UART0_TXD/ GPIO92
UART0_RTS/ GPIO93
UART0_CTS/ GPIO94
UART1_RXD/ GPIO0
UART1_TXD/ GPIO1
UART1_RST/ GPIO2
UART1_CTS/ GPIO3
I2C0_SDA/ GPIO4
I2C0_SCL/ GPIO5
I2C1_SDA/ GPIO6
I2C1_SCL/ GPIO7
SDIO_CLK/ GPIO64
SDIO_CMD/ GPIO65
SDIO_D0/ GPIO66
SDIO_D1/ GPIO67
SDIO_D2/ GPIO68
SDIO_D3/ GPIO69

SERIAL IO

*HSW_ULT_DDR3L

30 SIO_EXT_SCI# — SIO_EXT_SCI# AU2
29 BT_OFF — BT_OFF AM3
6,29 RF_OFF_PCH — R177 *0_4 — RF_OFF_PCH_R AM2
LAN_DISABLE# AM7
GPIO13_ULT AT3
GPIO14_ULT AH4
AD6
29 ZERO_ODD_DP# — R553 *0_4 — ODD_PRSNT#_R Y1
15,30,37,39 DGPU_PWROK T3
BOARD_ID6 AD5
GPIO25_ULT AM4
BOARD_ID7 AN3
GPIO27 AN5
BOARD_ID8 AD7
DEVSLP0 P2
TP11 — DEVSLP1 L2
DEVSLP2 N5
GPIO44_ULT AK4
TP for DG
BOARD_ID4 AG5
GPIO46_ULT AG3
BOARD_ID5 AB6
TP12
BT_COMBO_EN# U4
27 ACCEL_INTA# — GPIO49_ULT Y3
GPIO50_ULT P3
BOARD_ID0 AG6
BOARD_ID1 AP1
BOARD_ID2 AL4
BOARD_ID3 AT5
GPIO70_ULT C4
36 MPHY_PWREN — MPHY_PWREN Y2
GPIO76_ULT P1
24 ACZ_SPKR — V2

D60 PCH_THRMTRIP# — PM_THRMTRIP# 30
V4 EC_RCIN# — EC_RCIN# 30
T4 SERIRQ — R529 10K_4 — +3V — SERIRQ 27,30
AW15 PCH_OPI_RCOMP — R583 49.9/F_4
AF20
AB21

R6 GSPI0_CS
L6 GSPI0_CLK
N6 GSPI0_MISO
L8
R7 GSPI1_CS
L5 GSPI1_CLK
N7 GSPI1_MISO
K2 GSPI1_MOSI
J1 UART0_RXD
K3 UART0_TXD
J2 UART0_RTS
G1 UART0_CTS
K4 UART1_RXD
G2 UART1_TXD
J3 UART1_RST
J4 UART1_CTS
F2 I2C0_SDA
F3 I2C0_SCL
G4 I2C1_SDA
F1 I2C1_SCL
E3 SDIO_CLK
F4 SDIO_CMD
D3
E4 SDIO_D1
C3 SDIO_D2
E2 SDIO_D3

RP2
GSPI1_CLK 10 — 1 GSPI0_CS
I2C1_SDA 9 — 2 GSPI1_CS
GSPI0_MISO 8 — 3 GSPI1_MISO
SDIO_CMD 7 — 4 UART0_TXD
6 — 5
10K_10P8R_6 — +3V

RP6
SDIO_D2 10 — 1 UART0_CTS
SDIO_D1 9 — 2 I2C0_SCL
SDIO_D3 8 — 3 I2C0_SDA
SDIO_CLK 7 — 4 I2C1_SCL
6 — 5
10K_10P8R_6 — +3V

RP5
UART1_TXD 10 — 1 GSPI0_CLK
UART0_RTS 9 — 2 UART1_RXD
UART0_RXD 8 — 3 GSPI1_MOSI
UART1_RST 7 — 4 UART1_CTS
6 — 5
10K_10P8R_6 — +3V

GPIO Pull-up/Pull-down(CLG)

+3V_DEEP_SUS

SIO_EXT_SCI# R282 10K_4
BT_OFF R180 10K_4
RF_OFF_PCH_R R172 10K_4
GPIO13_ULT R218 10K_4
GPIO14_ULT R183 10K_4
GPIO44_ULT R565 10K_4
GPIO46_ULT R541 10K_4

+3V

GPIO49_ULT R552 10K_4
GPIO50_ULT R524 10K_4
ODD_PRSNT#_R R546 10K_4
DGPU_PWROK R513 10K_4
DEVSLP0 R515 10K_4
DEVSLP2 R499 10K_4
BT_COMBO_EN# R512 *10K_4
GPIO70_ULT R486 10K_4
EC_RCIN# R269 10K_4
GPIO76_ULT R525 10K_4
MPHY_PWREN R544 100K_4
MPHY_PWREN R545 *10K_4

+3VS5

GPIO25_ULT R173 10K_4
LAN_DISABLE# R169 10K_4
GPIO27 R626 10K_4

GPIO12 LAN_DISABLE#
SUS -->Check list
+3V -->Datasheet

Close to EC

+V1.05S_VCCST
PM_THRMTRIP# R184 1K_4

Model	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X12) 01 Dual Rank (X12) 10 Meso-AMD (X11) 11 Reserve	00 14" 01 15" 10 17"	0 : UMA 1 : DIS

R174 *10K_4 BOARD_ID0 R539 10K_4 — +3V_DEEP_SUS
R205 10K_4 BOARD_ID1 R199 *10K_4
R558 10K_4 BOARD_ID2 R559 *10K_4
R248 10K_4 BOARD_ID3 R255 *10K_4
R175 *10K_4 BOARD_ID4 R540 10K_4
R167 10K_4 BOARD_ID5 R549 *10K_4
R161 10K_4 BOARD_ID6 R164 *10K_4
R204 10K_4 BOARD_ID7 R198 *10K_4
R160 10K_4 BOARD_ID8 R163 *10K_4

6,7,8,10,11,12,13,22,23,24,25,26,27,29,30,35,36 — +3V
6,10,11,27,29,30,32,34,36,37,39 — +3VS5

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 8/9 (GPIO/MISC)	1A

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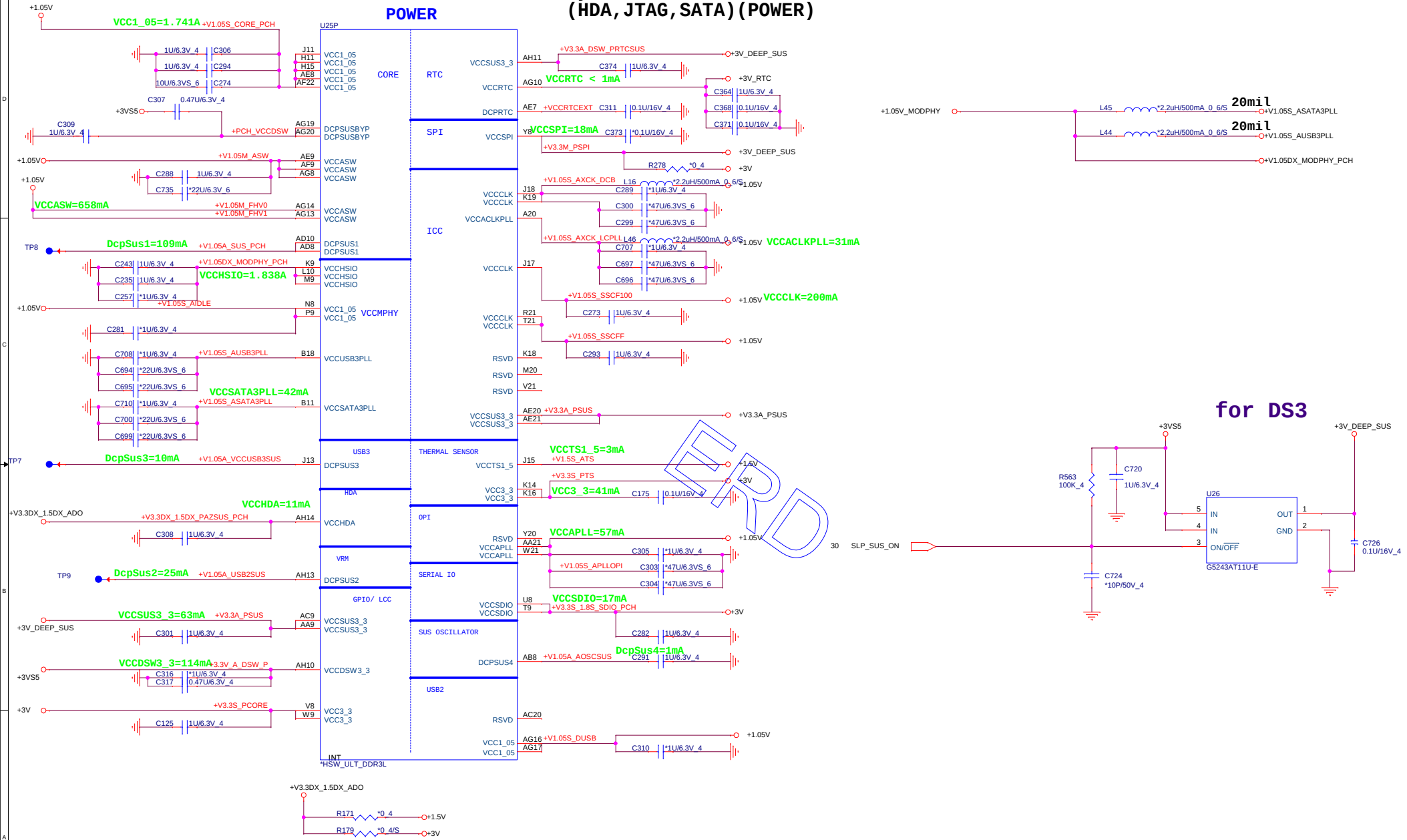
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)(POWER)

POWER



for DS3

6,7,8,9,11,12,13,22,23,24,25,26,27,29,30,35,36	+3V	8	+V1.05S_AUSB3PLL
23,24,25,26,29,36	+5V	7	+V1.05S_ASATA3PLL
		8	+V1.05S_AXCK_LCPLL
2,4,7,9,11,27,30,34,35,36	+1.05V	7,27	+3V_RTC
6,9,11,27,29,30,32,34,36,37,39	+3VS5	2,4,12,13,33	+1.35VSUS
13,25,28,32,33,34,35,36,37,39	+5VS5		

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 9/9(POWER-2)	1A

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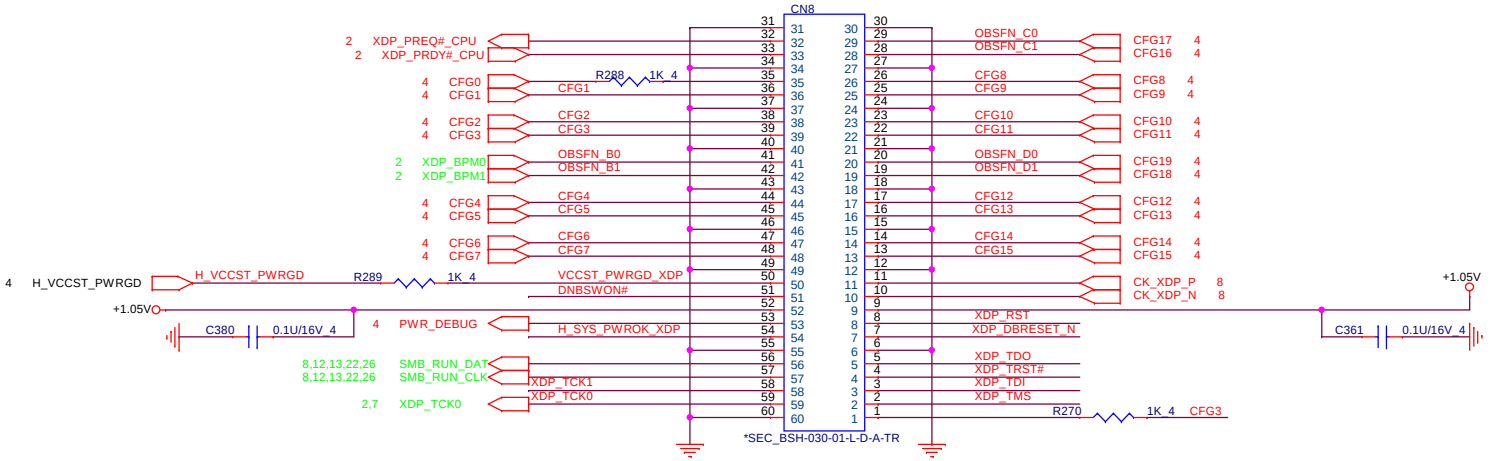
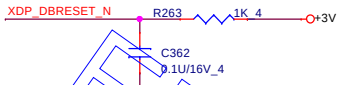
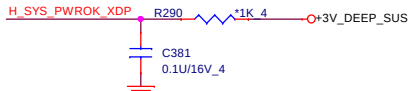
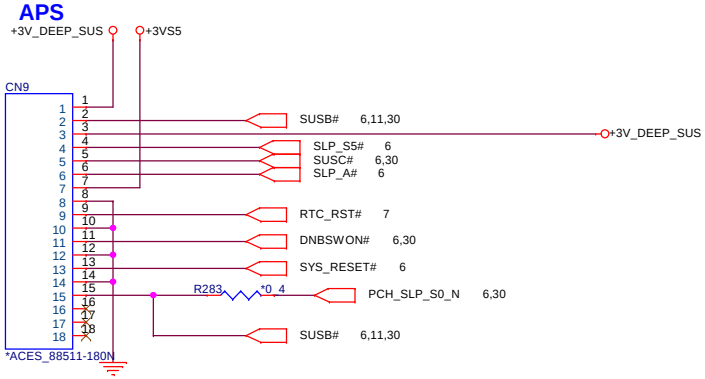
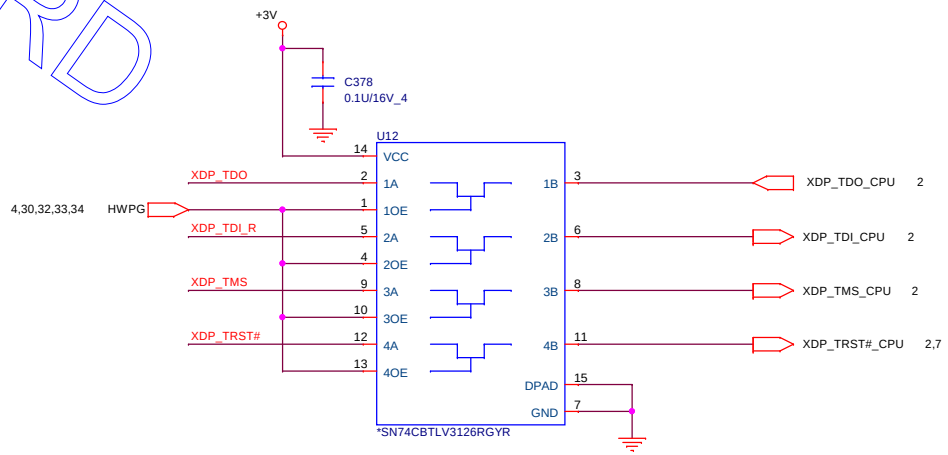


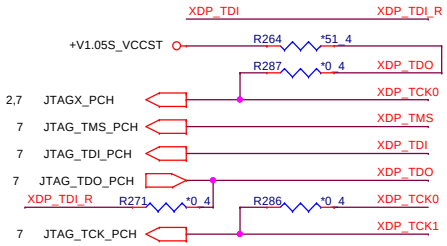




ERD







PROJECT : X11

Quanta Computer Inc.

ULT

Size	Document Number	Rev
	HSW XDP & APS	1A

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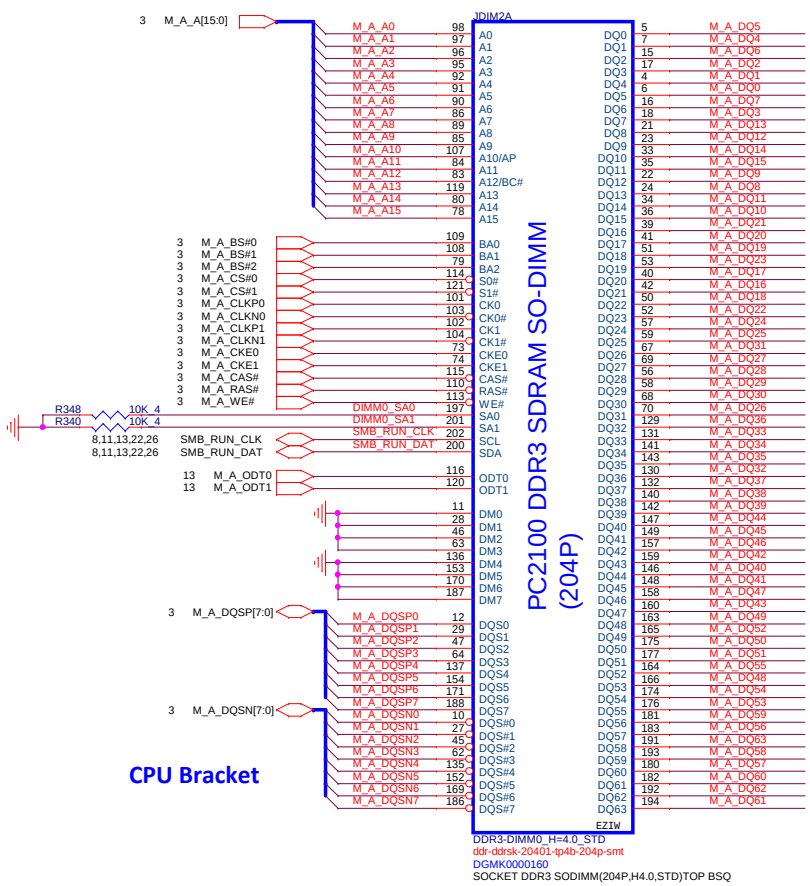
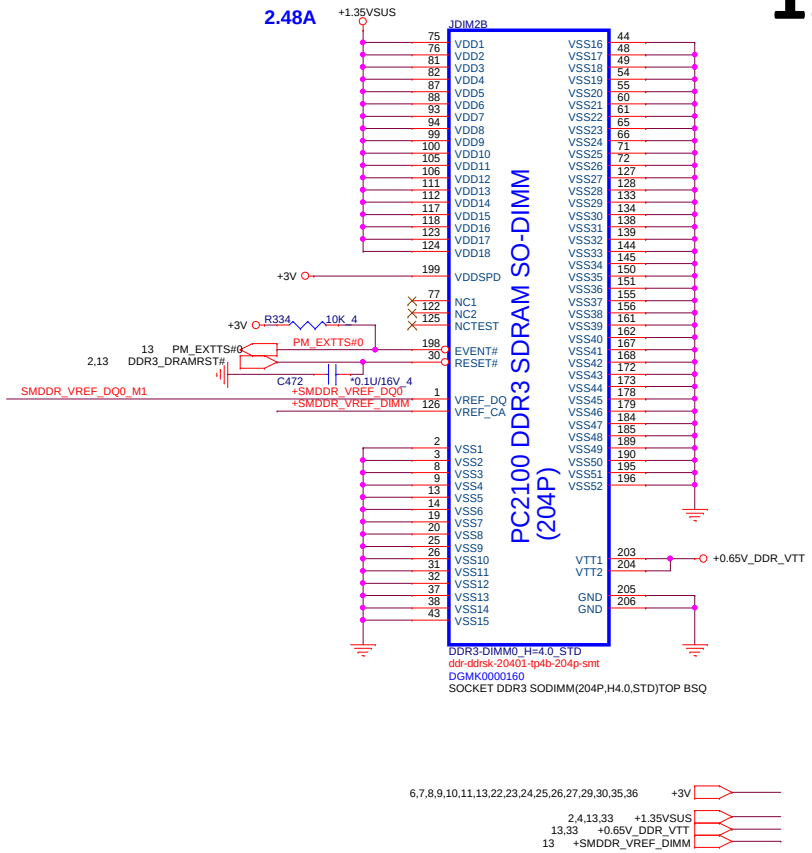
DIMM & Footprint 同Joshua提供



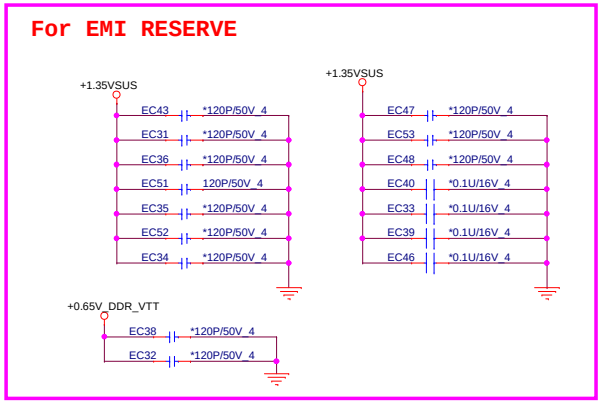
CPU Bracket

ERD

2.48A

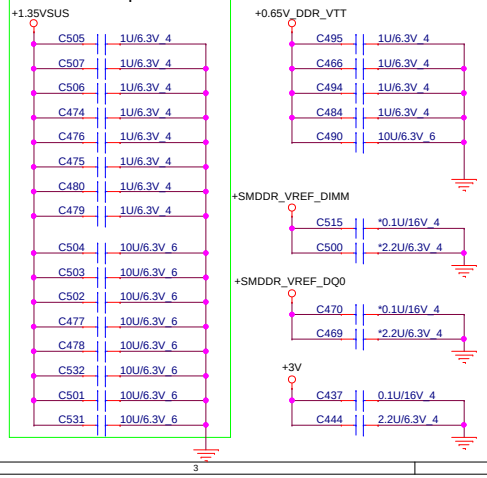


For EMI RESERVE

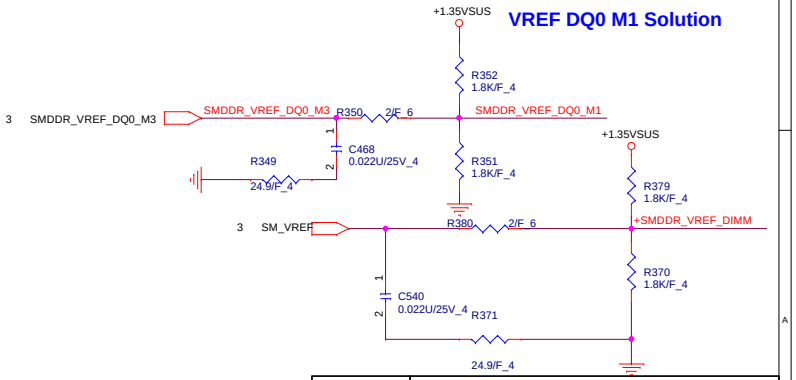


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution

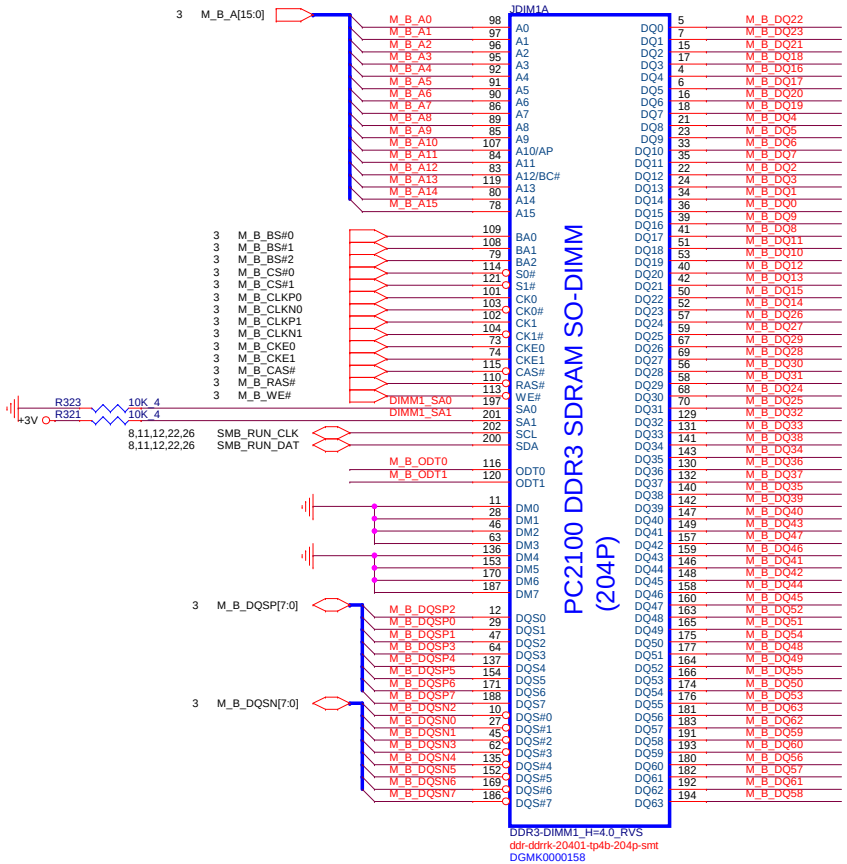


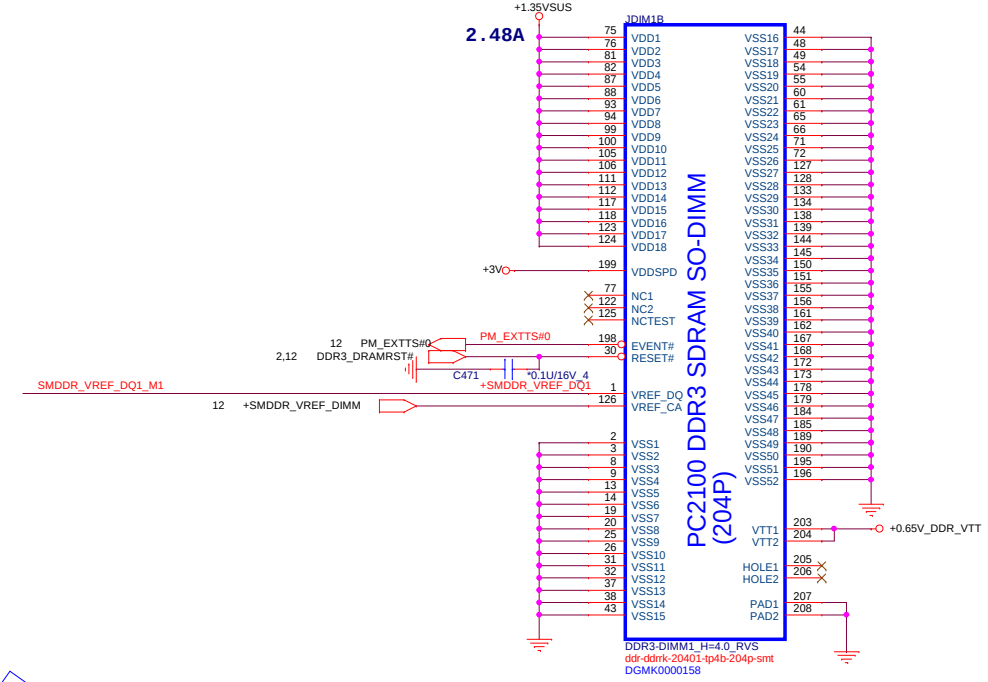
PROJECT : X11

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-STD(4.0H)	1A
Date: Monday, January 05, 2015	Sheet 12of 40	

DIMM & Footprint 同Joshua提供

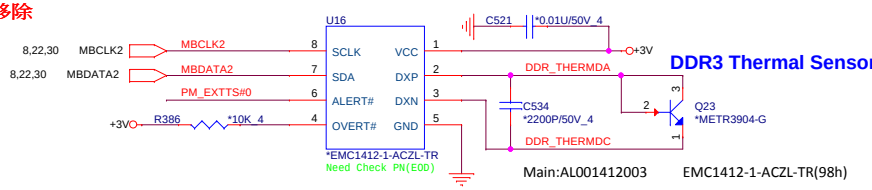




ERD

Local Thermal Sensor

MV可移除

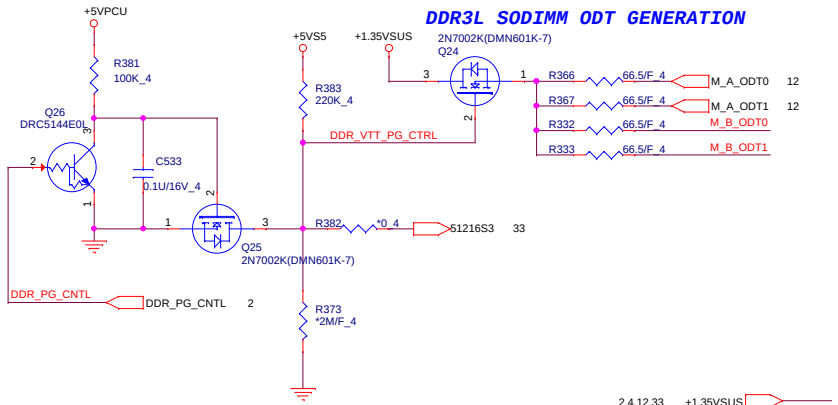


DDR3 Thermal Sensor

Main:AL001412003 EMC1412-1-ACZL-TR(98h)

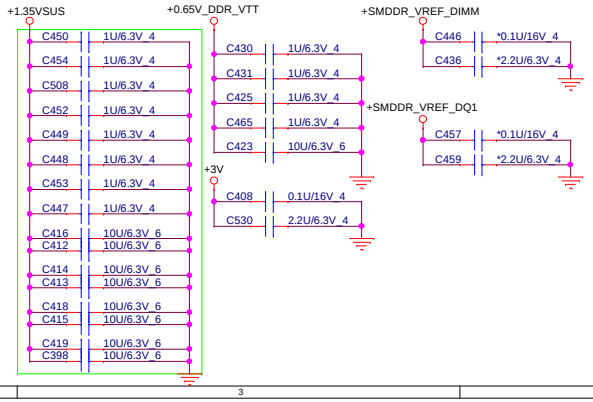
2nd:AL000431014 TMP431ADGKR(98h)

DDR3L SODIMM ODT GENERATION

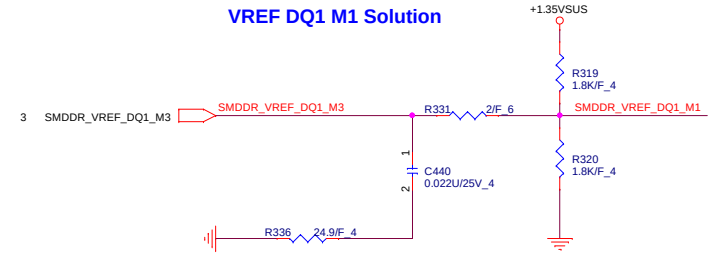


Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



VREF DQ1 M1 Solution



PROJECT : X11

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM1-RVS(4.0H)	1A

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Platform	Type HP	P/N
Carrizo$_{hp}$	Gen 3	CH4222K9B04 RD
Carrizo-L	Gen 1/Gen 2	CH4102K1B03

9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)

U4000A

PCI EXPRESS INTERFACE

PEG_TXP0 / PEG_TXN0 → AF30 / AE31 PCIE_RX0P / PCIE_RX0N
PEG_TXP1 / PEG_TXN1 → AE29 / AD28 PCIE_RX1P / PCIE_RX1N
PEG_TXP2 / PEG_TXN2 → AD30 / AC31 PCIE_RX2P / PCIE_RX2N
PEG_TXP3 / PEG_TXN3 → AC29 / AB28 PCIE_RX3P / PCIE_RX3N
AB30 / AA31 PCIE_RX4P / PCIE_RX4N
AA29 / Y28 PCIE_RX5P / PCIE_RX5N
Y30 / W31 PCIE_RX6P / PCIE_RX6N
W29 / V28 PCIE_RX7P / PCIE_RX7N
V30 / U31 NC#V30 / NC#U31
U29 / T28 NC#U29 / NC#T28
T30 / R31 NC#T30 / NC#R31
R29 / P28 NC#R29 / NC#P28
P30 / N31 NC#P30 / NC#N31
N29 / M28 NC#N29 / NC#M28
M30 / L31 NC#M30 / NC#L31
L29 / K30 NC#L29 / NC#K30

PCIE_TX0P / PCIE_TX0N AH30 / AG31 ← PEG_RXP0_C / PEG_RXN0_C (C4000 / C4001 0.22U/10V_4) → PEG_RXP0 / PEG_RXN0
PCIE_TX1P / PCIE_TX1N AG29 / AF28 ← PEG_RXP1_C / PEG_RXN1_C (C4002 / C4003 0.22U/10V_4) → PEG_RXP1 / PEG_RXN1
PCIE_TX2P / PCIE_TX2N AF27 / AF26 ← PEG_RXP2_C / PEG_RXN2_C (C4004 / C4005 0.22U/10V_4) → PEG_RXP2 / PEG_RXN2
PCIE_TX3P / PCIE_TX3N AD27 / AD26 ← PEG_RXP3_C / PEG_RXN3_C (C4006 / C4007 0.22U/10V_4) → PEG_RXP3 / PEG_RXN3
PCIE_TX4P / PCIE_TX4N AC25 / AB25
PCIE_TX5P / PCIE_TX5N Y23 / Y24
PCIE_TX6P / PCIE_TX6N AB27 / AB26
PCIE_TX7P / PCIE_TX7N Y27 / Y26
NC#W24 / NC#W23 W24 / W23
NC#V27 / NC#U26 V27 / U26
NC#U24 / NC#U23 U24 / U23
NC#T26 / NC#T27 T26 / T27
NC#T24 / NC#T23 T24 / T23
NC#P27 / NC#P26 P27 / P26
NC#P24 / NC#P23 P24 / P23
NC#M27 / NC#N26 M27 / N26

CLOCK
8 CLK_VGA_P / CLK_VGA_N → AK30 / AK32 PCIE_REFCLKP / PCIE_REFCLKN

CALIBRATION
PCIE_CALR_TX Y22 — SUN_PCIE_CALRP — R4000 1.69K/F_4 — +1.0V_VGA
PCIE_CALR_RX AA22 — SUN_PCIE_CALRN — R4002 1K/F_4

R4001 1K_4 TEST_PG → N10 TEST_PG
PEGX_RST# → AL27 PERSTB

Meso_S3

U4000G

DP POWER
AG15 AG16 AF16 AG17 AG18 AG19 AF14 NC_DP_VDDR#1..6 DP_VDDR
AG20 AG21 AF22 AG22 AD14 NC_DP_VDDC#1..4 DP_VDDC
AG14 AH14 AM14 AM16 AM18 AF23 AG23 AM20 AM22 AM24 AF19 AF20 AE14 NC_DP_VSSR#1..12 DP_VSSR
AF17 NC_UPHYAB_DP_CALR

NC/DP POWER
NC#AE11 NC#AF11 NC#AE13 NC#AF13 NC#AG8 NC#AG10
NC#AF6 NC#AF7 NC#AF8 NC#AF9
NC#AE1 NC#AE3 NC#AG1 NC#AG6 NC#AH5 NC#AF10 NC#AG9 NC#AH8 NC#AM6 NC#AM8 NC#AG7 NC#AG11
NC#AE10

Meso_S3

+1.8V_VGA — 1.8V (40mA) — C4008 10U/6.3VS_6 — C4009 1U/10V_4
+1.0V_VGA — 1.0V (32mA) — C4014 *10U/6.3VS_6 — C4015 1U/10V_4 — C4016 0.1U/16V_4

12/10:reserve for verify

+3V_VGA — R4003 1K/F_4
PLTRST# (2) / DGPU_HIN_RST# (1) → D4000 BAT54AW-L (3) → PEGX_RST#

+3V_VGA — C4021 *0.1U/16V_4
U4001 *MC74VHC1G08DFT2G
C4022 *0.1U/16V_4
6,11,25,27,29,30 PLTRST# → 2
8 DGPU_HOLD_RST# — R4004 *0_4/S — DGPU_HIN_RST# → 1
4 PEGX_RST# → PEGX_RST# 15
R4005 100K/F_4

15,17,39 +3V_VGA
15,17,27,37,39 +1.8V_VGA
17,39 +1.0V_VGA

ERD

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PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ S3 PCIE/DP power	1A

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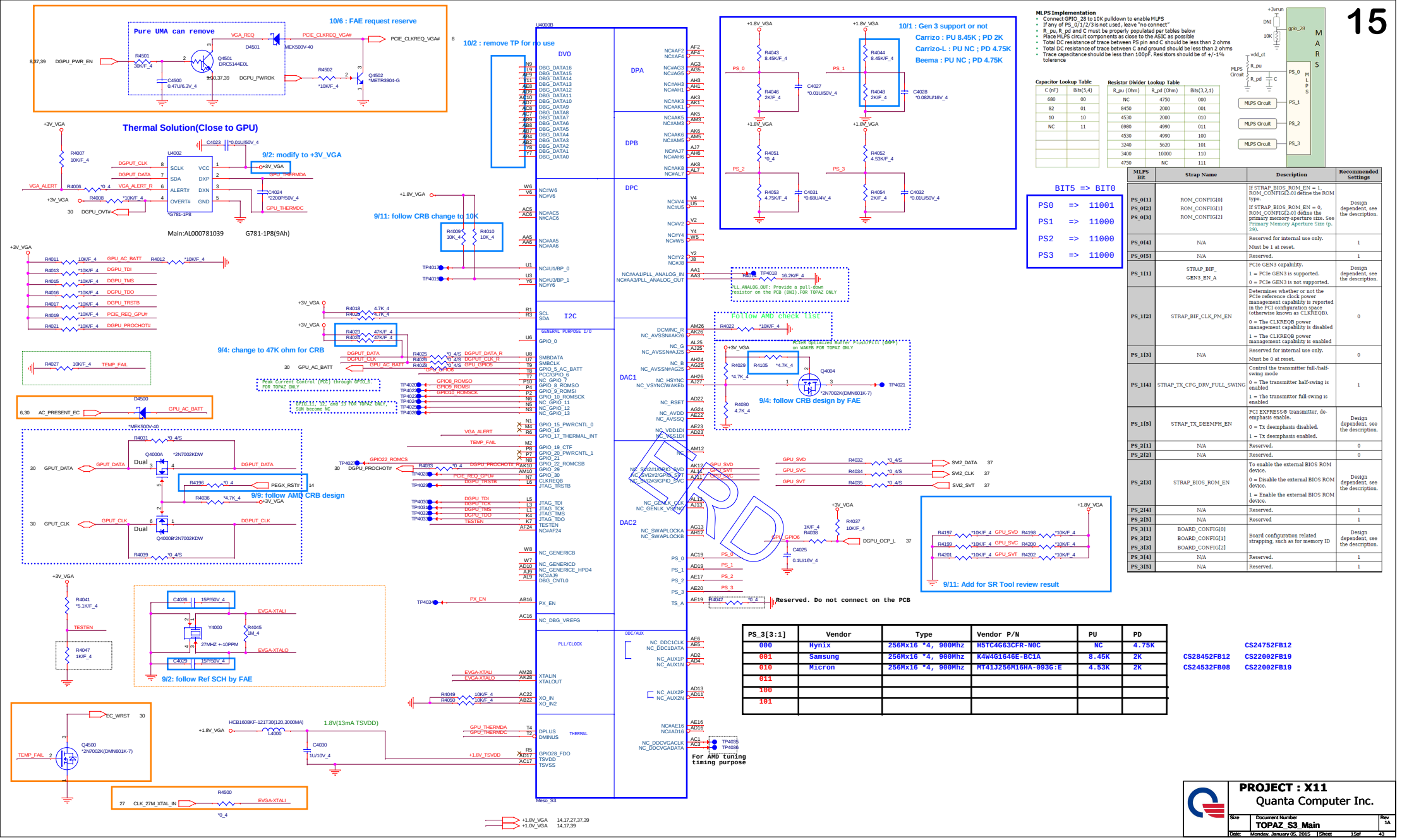

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 29).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved	1
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[2]	BOARD_CONFIG[1]		
PS_3[3]	BOARD_CONFIG[2]		
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1

PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD		
000	Hynix	256Mx16 *4, 900Mhz	H5TC4G63CFR-N0C	NC	4.75K		CS24752FB12
001	Samsung	256Mx16 *4, 900Mhz	K4W4G1646E-BC1A	8.45K	2K	CS28452FB12	CS22002FB19
010	Micron	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	4.53K	2K	CS24532FB08	CS22002FB19
011							
100							
101							

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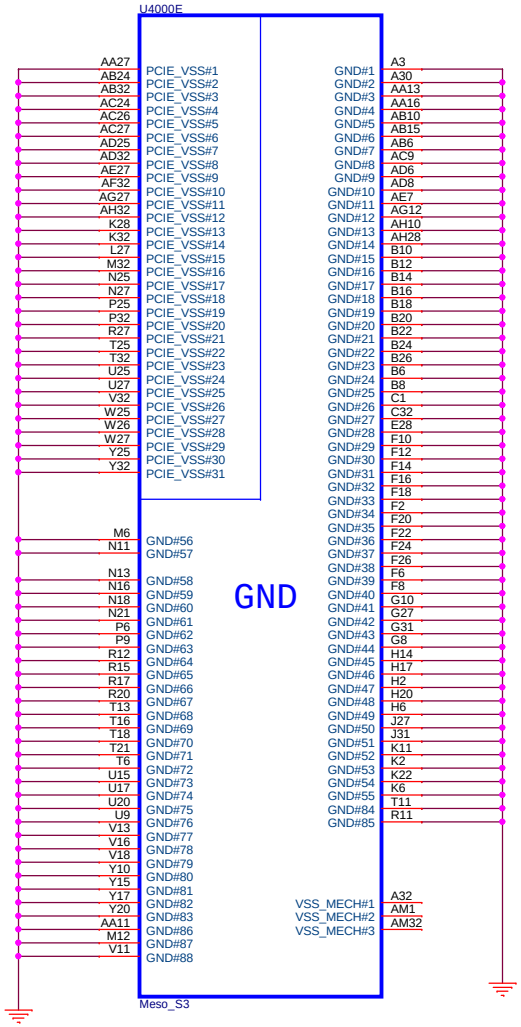
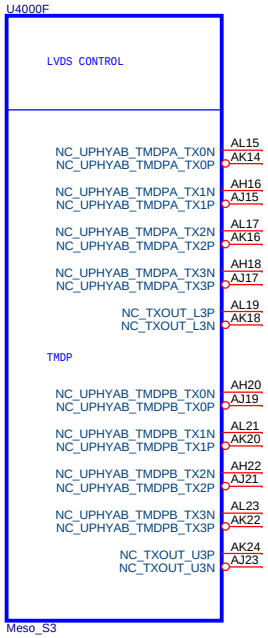
Quanta Computer Inc.
Size | Document Number: TOPAZ_S3_Main | Rev: 1A
Date: Monday, January 05, 2015 | Sheet 150f 43





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

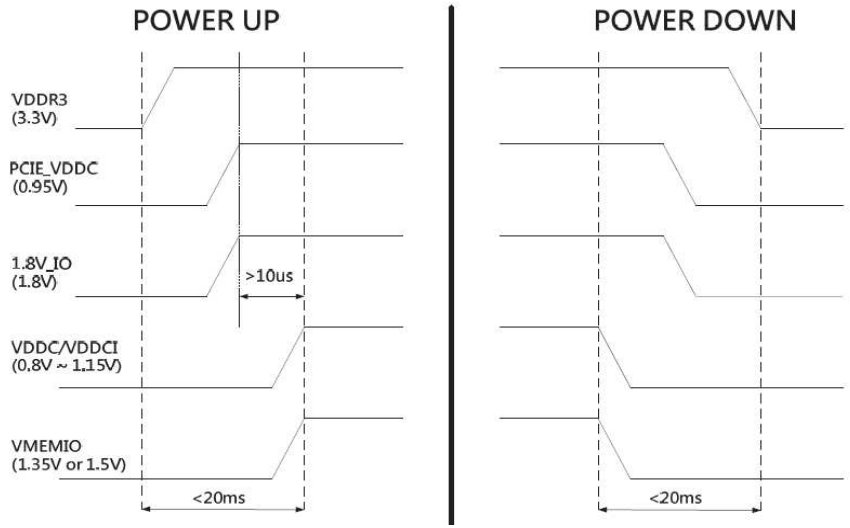
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE



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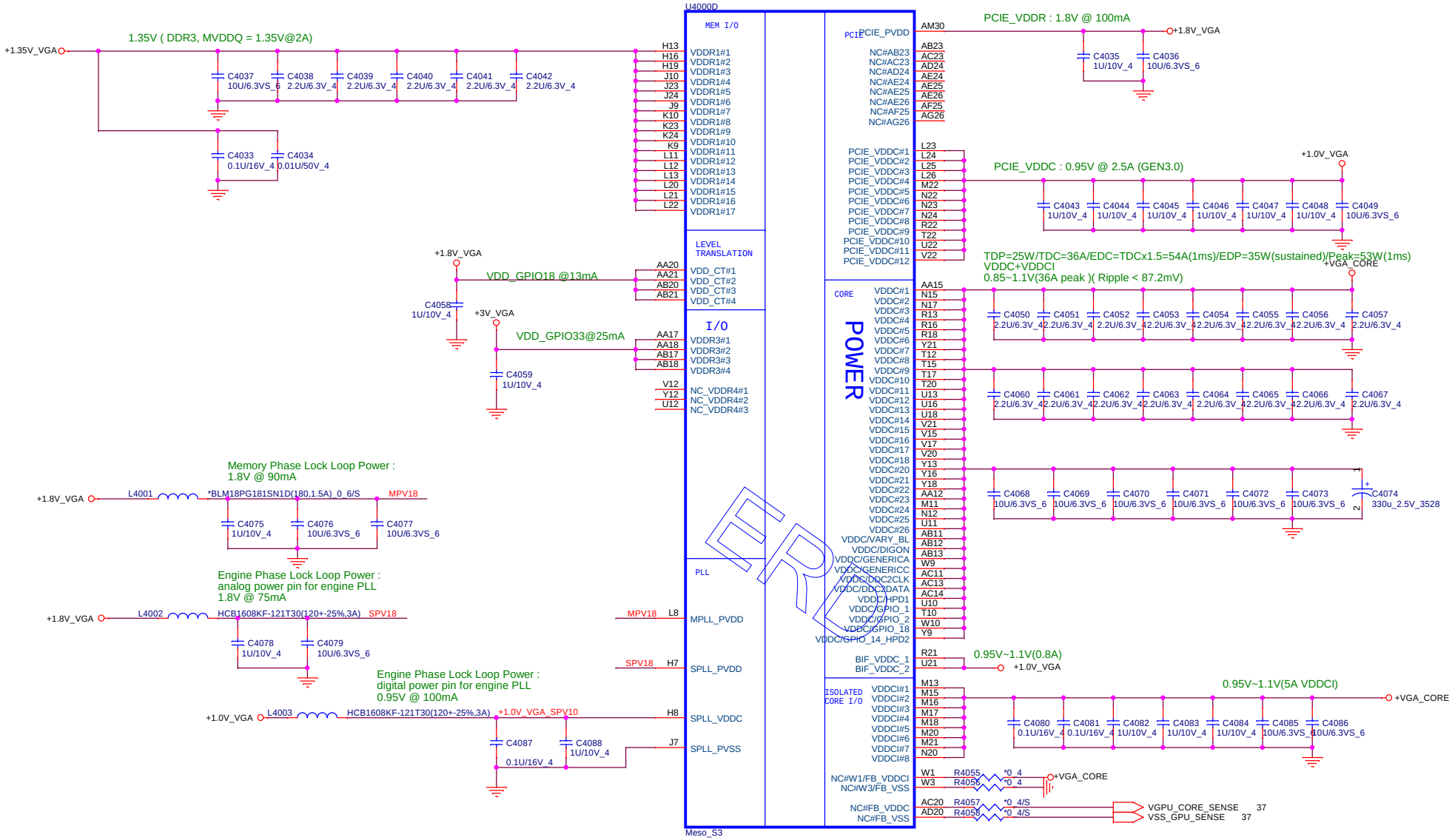
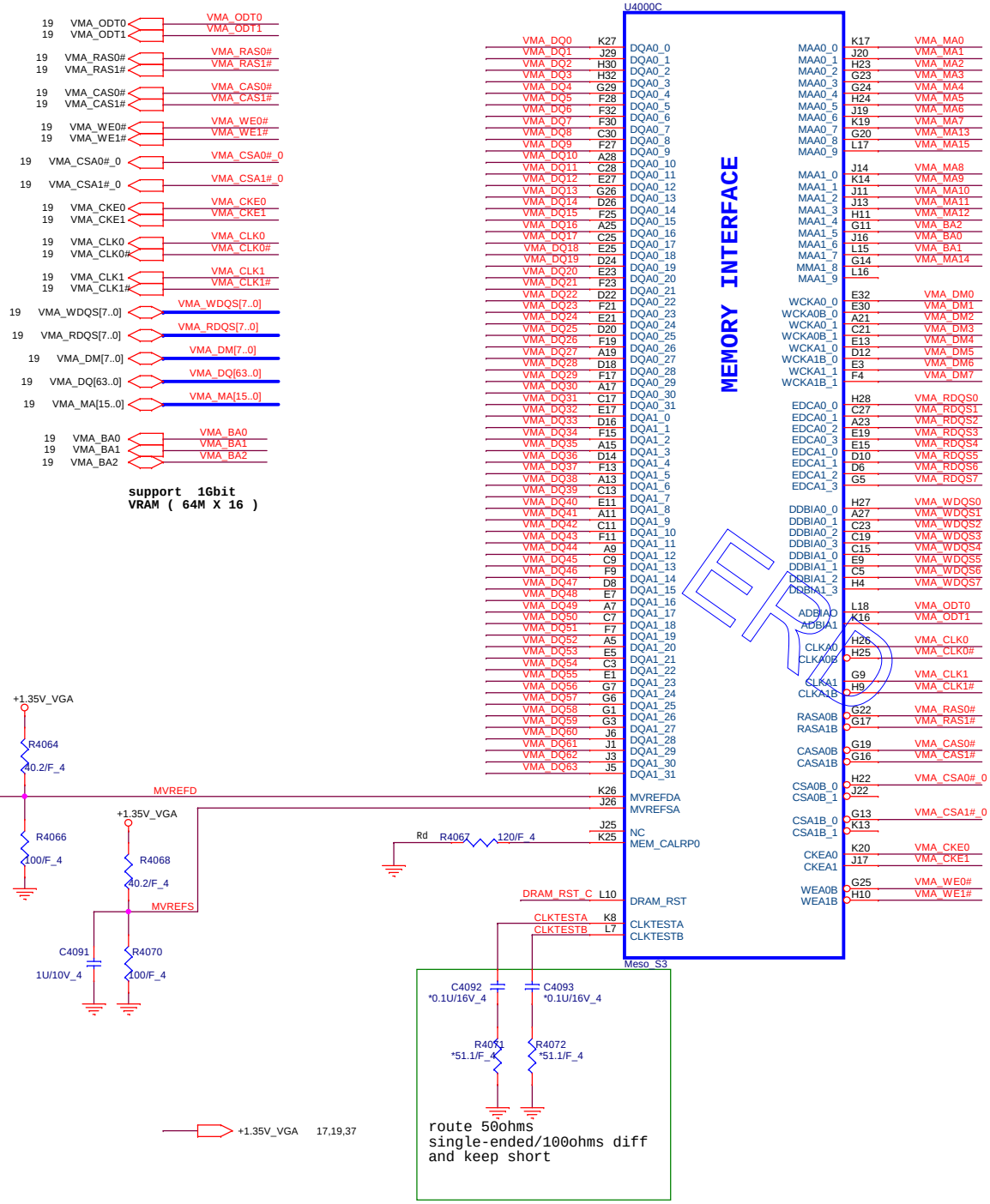
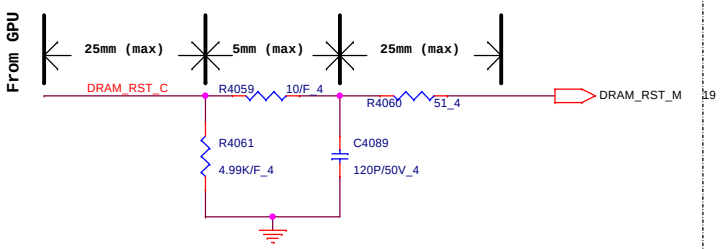
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A
Date: Monday, January 05, 2015	Sheet 16 of 43	



PROJECT : X11		
Quanta Computer Inc.		
Size	Document Number: TOPAZ S3 Power	Rev: 1A
Date: Monday, January 05, 2015	Sheet 17 of 43	



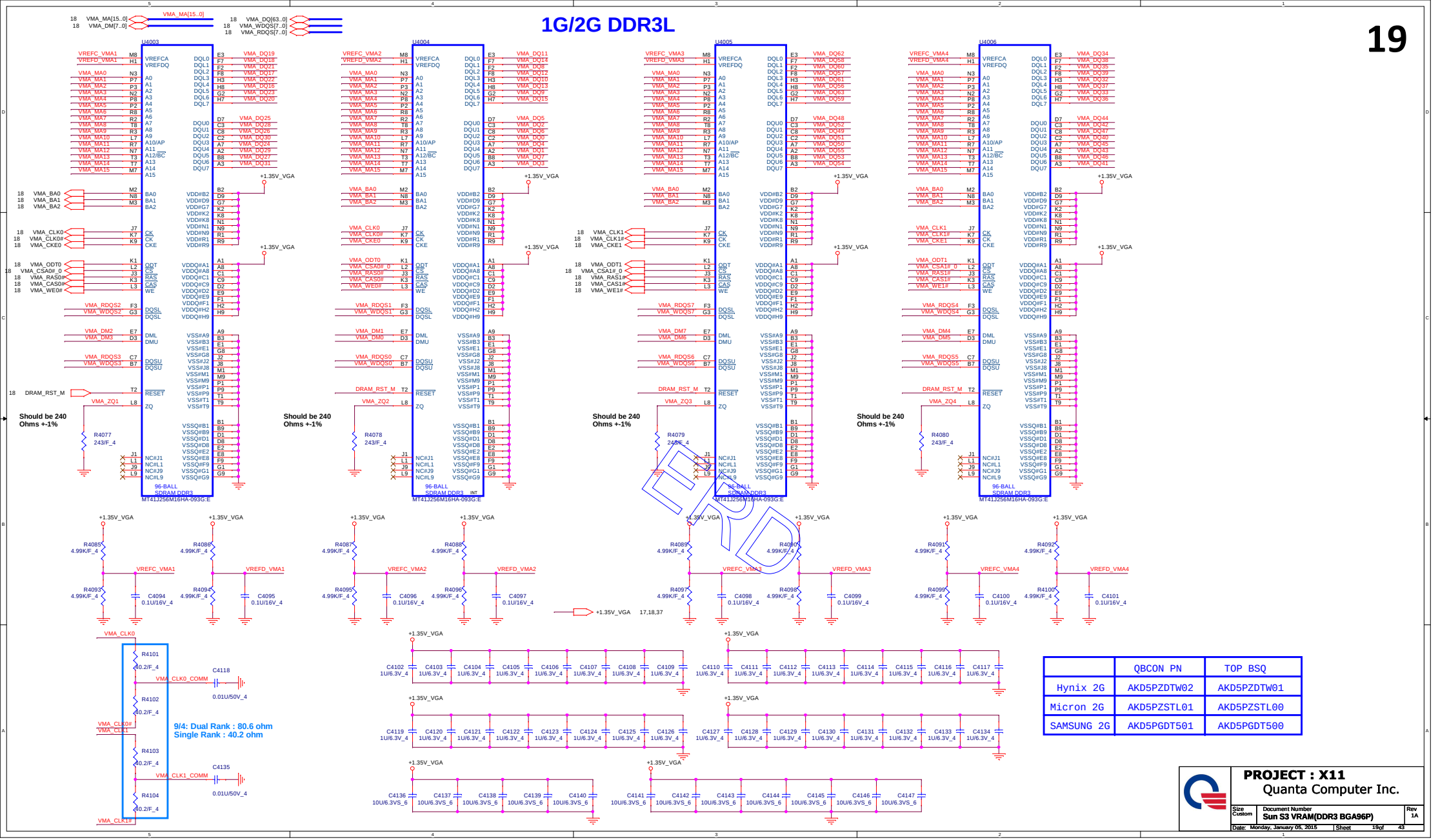


Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

PROJECT : X11 Quanta Computer Inc.		
Size	Document Number TPOAZ_S3_MEM_Interface	Rev 1A
Date: Monday, January 05, 2015	Sheet 18 of 43	

1G/2G DDR3L



	QBCON PN	TOP BSQ
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01
Micron 2G	AKD5PZSTL01	AKD5PZSTL00
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A

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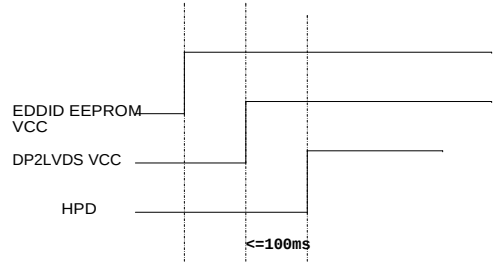
RTD2136 Dual Channel only

RTD2136S Power Up Sequence 22



Reserve for co layout EDP CON, EDP only please stuff

Pin 18: keep 80mil Trace

RTD2136R

IC底部需接GND

Reserve

Default(LVDS Only)

For eDP, close to U3

LVDS Only

L10: need use CV-4709MN00 for Vendor suggestion

keep 80 mil

USING 60R 2A

CLOSE TO Pin22

Close to Pin18

USING 60R 1A

Close to Pin5

Close to Pin17

Close to Pin11

Close to Pin43

SWR MODE	LDO MODE
Stuff L10	Stuff R59

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTD2136	1A

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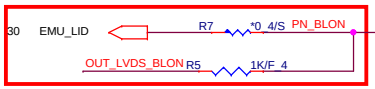
LID Switch



D1 MEK500V-40 BLON_CON C2 22P/50V_4 R6 100K/F_4

OUT_LVDS_BLON R4 100K/F_4

OUT_DPST_PWM R28 1K/F_4 VADJ1

C40 33P/50V_4

100mA

+VIN +VIN_BLIGHT

C71 0.1U/25V_4

C91 0.01U/50V_4

+VIN_BLIGHT

C101 *4.7U/25V_8 C98 0.1U/25V_4

C102 *4.7U/25V_8 C103 0.1U/25V_4 C97 0.1U/25V_4 C92 0.1U/25V_4 C72 0.1U/25V_4

22 EDIDDATA_2136 EDIDDATA
22 EDIDCLK_2136 EDIDCLK

+3V +3V_CAM

C26 *0.01U/50V_4 C34 *4.7U/6.3V_4

22 TXUCLKOUT- TXUCLKOUT-
22 TXUCLKOUT+ TXUCLKOUT+
22 TXUOUT0+ TXUOUT0+
22 TXUOUT0- TXUOUT0-
22 TXUOUT1+ TXUOUT1+
22 TXUOUT1- TXUOUT1-
22 TXUOUT2+ TXUOUT2+
22 TXUOUT2- TXUOUT2-

+3V R61 *4.7K_4 EDIDCLK
R62 *4.7K_4 EDIDDATA

For LVDS Only:

RF

C62 *10P/50V_4 C63 *10P/50V_4

LVDS Conn.

23

GS12401-1011-9H
lvds-50671-04041-001-40p-l

+3VLCD_CON

DFFC40FR063 CN2

C19 0.047U/25V_4 C18 0.047U/25V_4

+3V R14 *0_6/S

C17 1000P/50V_4

EDIDCLK_R
EDIDDATA_R
TXLOUT0-
TXLOUT0+
TXLOUT1-
TXLOUT1+
TXLOUT2-
TXLOUT2+
TXLCLKOUT-
TXLCLKOUT+
TXUOUT0-
TXUOUT0+
TXUOUT1-
TXUOUT1+
TXUOUT2-
TXUOUT2+
TXUCLKOUT-
TXUCLKOUT+

For LVDS Only: Stuff Rc
For EDP Only: Stuff Rd

6,22 ULT_EDP_HPD R8 0_4 ULT_EDP_HPD_R

Rc R9 *0_4
Rd

USBP2- R629 0_4 USBP2-_C
USBP2+ R630 0_4 USBP2+_C

*MCM2012B900GBE +3V_CAM

8 USBP2-
8 USBP2+
L2
USBP2-_C
USBP2+_C

24 DIGITAL_CLK
24 DIGITAL_D1

L3 120/300MA_S0_4

L1 120/300MA_S0_4

DIGITAL_CLK_L
VADJ1
BLON_CON

C13 *10P/50V_4 C12 *10P/50V_4

+VIN_BLIGHT

For LVDS
Close to LVDS connector

22 2136_DISP_ON

Power Switch Reserve

80 mil trace

R23 *0_8

R7468 *100K/F_4

C29 *4.7U/6.3V_4

+3VLCD_CON

+3V

For eDP
Close to LVDS connector

C37 1U/6.3V_4

U2
IN
IN
ON/OFF
OUT
GND
AP2821KTR-G1-E

L8 HCB1608KF-181T15_S0_6

C52 0.01U/50V_4 C49 0.1U/16V_4 C48 10U/6.3V_6

6 PCH_DISP_ON

R31 100K/F_4

R31 close to U2 for eDP,stuff

for eDP,stuff U2 & L8

for LVDS,stuff C29 & R23

+3VLCD_CON

ERD

For EDP Only: stuff Cap
For LVDS only stuff Resistor

22 TXLCLKOUT+ TXLCLKOUT+
22 TXLCLKOUT- TXLCLKOUT-
22 TXLOUT2+ TXLOUT2+
22 TXLOUT2- TXLOUT2-
22 INT_eDP_TXP1_R
22 TXLOUT0+_2136
22 TXLOUT0-_2136
22 INT_eDP_TXN1_R
22 INT_eDP_TXP0_R
22 TXLOUT1+_2136
22 TXLOUT1-_2136
22 INT_eDP_TXN0_R
22 INT_eDP_AUXN_R
22 EDIDDATA
22 EDIDCLK
22 INT_eDP_AUXP_R

R43 *0_4 R42 *0_4 C42 0.1U/16V_4 C41 0.1U/16V_4
R45 *0_4 R44 *0_4 C44 0.1U/16V_4 C43 0.1U/16V_4
R49 *0_4 R48 *0_4 C39 0.1U/16V_4 C38 0.1U/16V_4

TXLOUT0+ TXLOUT0-
TXLOUT1+ TXLOUT1-
EDIDDATA_R EDIDCLK_R

For LVDS Only close CN2

R37 *100K/F_4

Ra R38 *0_4 OUT_DPST_PWM

Rb R3 *0_4 OUT_LVDS_BLON

22 2136_DPST_PWM
22 2136_LVDS_BLON

For eDP, close to CN2

6 PCH_LVDS_BLON R101 0_4 OUT_LVDS_BLON
22 EDP_DPST_PWM R102 10/F_4 OUT_DPST_PWM

For EDP Only: Reserved

+3V R40 *100K_4 EDIDDATA_R
R39 *100K_4 EDIDCLK_R

+3V R58 *1K_4 OUT_DPST_PWM
R1 *1K_4 OUT_LVDS_BLON

EMI Solution

C_TX2_HDMI+ R247 220/F_4 C_TX2_HDMI-
C_TX1_HDMI+ R231 220/F_4 C_TX1_HDMI-
C_TX0_HDMI+ R234 220/F_4 C_TX0_HDMI-
C_TXC_HDMI+ R217 220/F_4 C_TXC_HDMI-

C_IN_CLK R219 0_4 C_TXC_HDMI+
C_IN_CLK# R215 0_4 C_TXC_HDMI-

HDMI SMBus Isolation

+3V R188 2.2K_4 Q14

6 SDVO_CLK HDMI_SCL_R HDMI_SCLK

6 SDVO_DATA HDMI_SDA_R HDMI_SDATA

+3V R187 2.2K_4

2N7002DW

Close to HDMI connector

DGPU_CL_HDMIP

Q40 2N7002K(DMN601K-7)

R253 470/F_4 C_TX2_HDMI+
R246 470/F_4 C_TX2_HDMI-
R232 470/F_4 C_TX1_HDMI+
R230 470/F_4 C_TX1_HDMI-
R241 470/F_4 C_TX0_HDMI+
R233 470/F_4 C_TX0_HDMI-
R222 470/F_4 C_IN_CLK
R214 470/F_4 C_IN_CLK#

+3V R273 100K/F_4 C372 0.1U/16V_4

Close to Q40

+3V R170 1M_4

6 HDMI_HPD_CON HDMI_HPD R176 20K/F_4

Q10 2N7002K(DMN601K-7)

2 IN_D2 IN_D2 C354 0.1U/16V_4 C_TX2_HDMI+
2 IN_D2# IN_D2# C349 0.1U/16V_4 C_TX2_HDMI-
2 IN_D1 IN_D1 C336 0.1U/16V_4 C_TX1_HDMI+
2 IN_D1# IN_D1# C331 0.1U/16V_4 C_TX1_HDMI-
2 IN_D0 IN_D0 C343 0.1U/16V_4 C_TX0_HDMI+
2 IN_D0# IN_D0# C339 0.1U/16V_4 C_TX0_HDMI-
2 IN_CLK IN_CLK C327 0.1U/16V_4 C_IN_CLK C_TXC_HDMI+
2 IN_CLK# IN_CLK# C324 0.1U/16V_4 C_IN_CLK# C_TXC_HDMI-

+5V_HDMIC D3 MEK500V-40 5V_HSMBCK R196 2.2K_4
D5 MEK500V-40 5V_HSMBDT R202 2.2K_4

C321 *10P/50V_4
C318 *10P/50V_4

HDMI_SCLK
HDMI_SDATA

+5V_HDMIC C313 *0.01U/50V_4

for EMI request

HDMI_HPD HDMI_DET_C

VC1 *TVM0G5R5M220R C298 220P/50V_4

CN24 SHELL1 HDMI CONN SHELL2

D2+ D2 Shield D2- D1+ D1 Shield D1- D0+SHELL2 D0 Shield D0- CK+ CK Shield CK- SHELL2 CE Remote NC DDC CLK DDC DATA GND +5V HP DET

+5V_HDMIC

+5V 40 mils F1 FUSE1A6V_POLY H=1.4mm(Max)

C314 0.1U/16V_4

VC2 *TVM0G5R5M220R

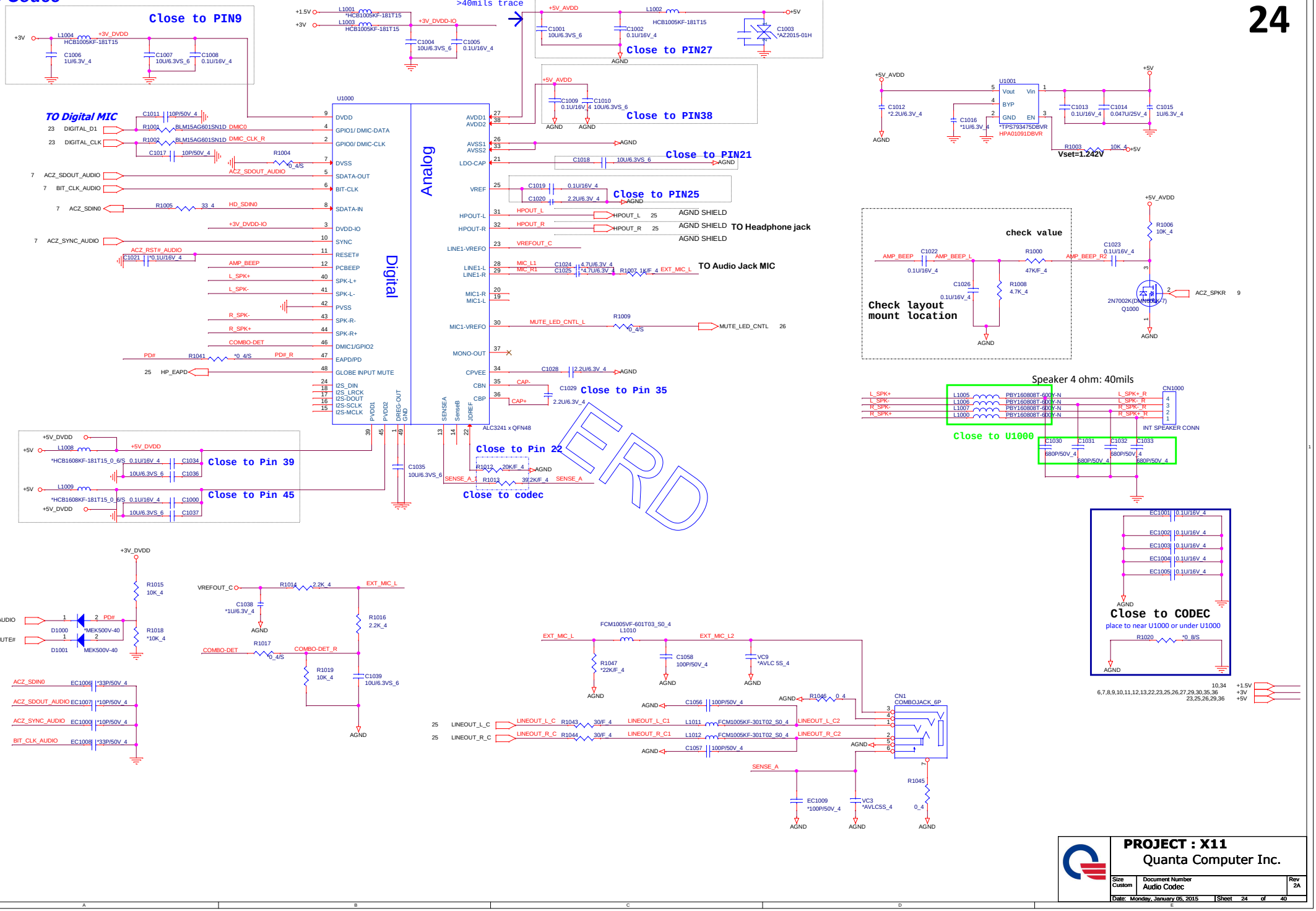
SSM14 spec is 40V 1A

13,25,28,32,33,34,35,36,37,39 +5VS5
6,7,8,9,10,11,12,13,22,24,25,26,27,29,30,35,36 +3V
4,7,25,26,27,29,30,31,32 +3VPCU
24,25,26,29,36 +5V
26,28,29,31,32,33,34,35,36,37,38,39 +VIN

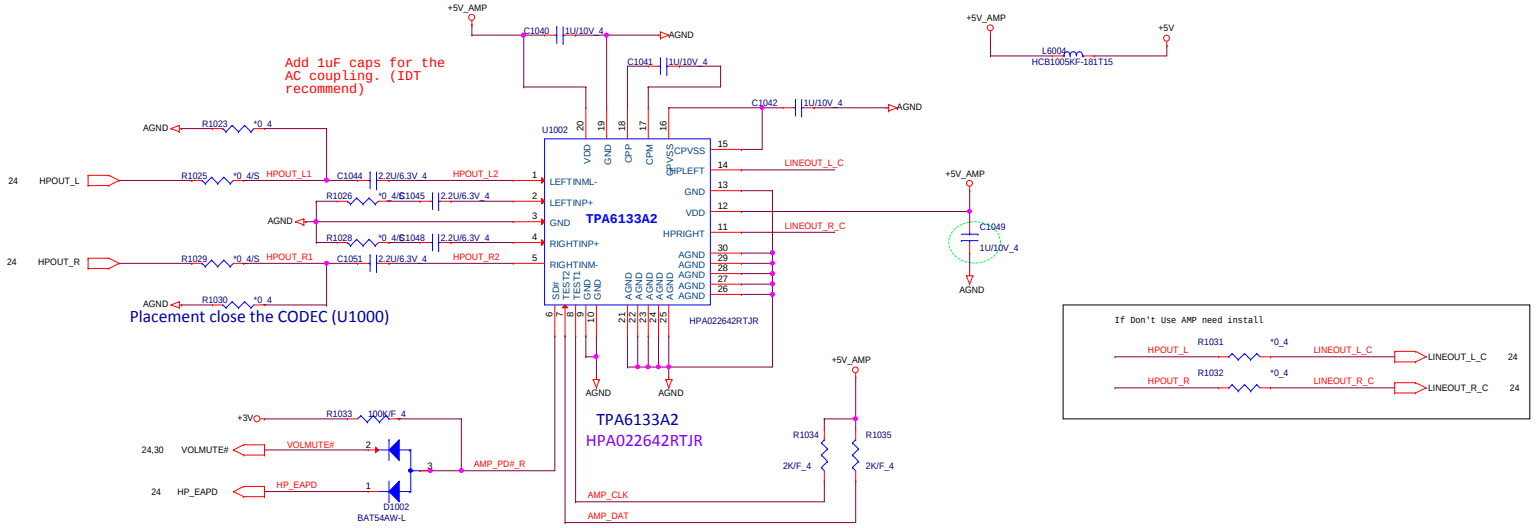
PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM/D-MIC	1A
Date: Monday, January 05, 2015	Sheet 23 of 40	

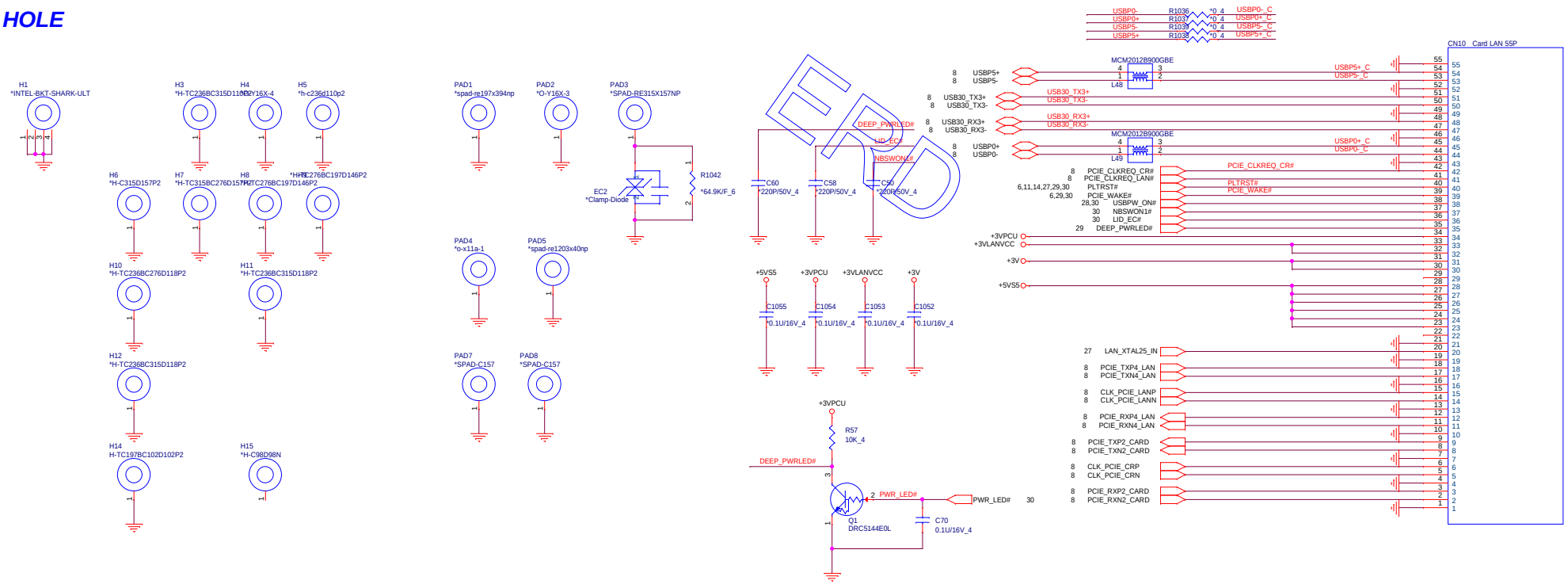
Audio Codec


Close to PIN9
>40mils trace
Close to PIN27
Close to PIN38
Close to PIN21
Close to PIN25
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
Close to Pin 35
Close to Pin 22
Close to Pin 39
Close to Pin 45
Close to codec
Close to U1000
Close to CODEC
place to near U1000 or under U1000
check value
Check layout mount location
Speaker 4 ohm: 40mils
INT SPEAKER CONN
Vset=1.242V
U1000
Digital
Analog
ALC3241 x QFN48
CN1 COMBOJACK_6P
CN1000
U1001
Q1000
PROJECT : X11
Quanta Computer Inc.
Audio Codec
Size Custom
Rev 2A
Date: Monday, January 05, 2015
Sheet 24 of 40

Head Phone out

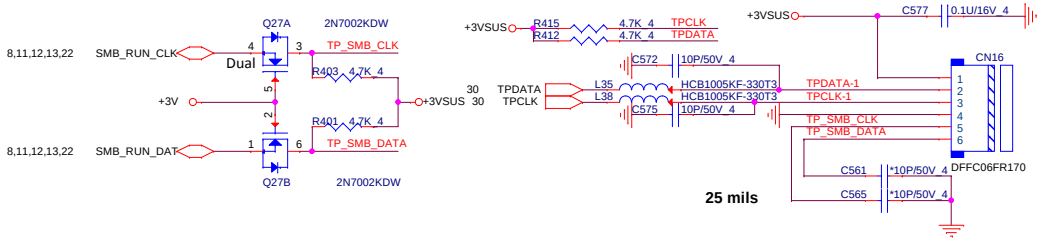


HOLE

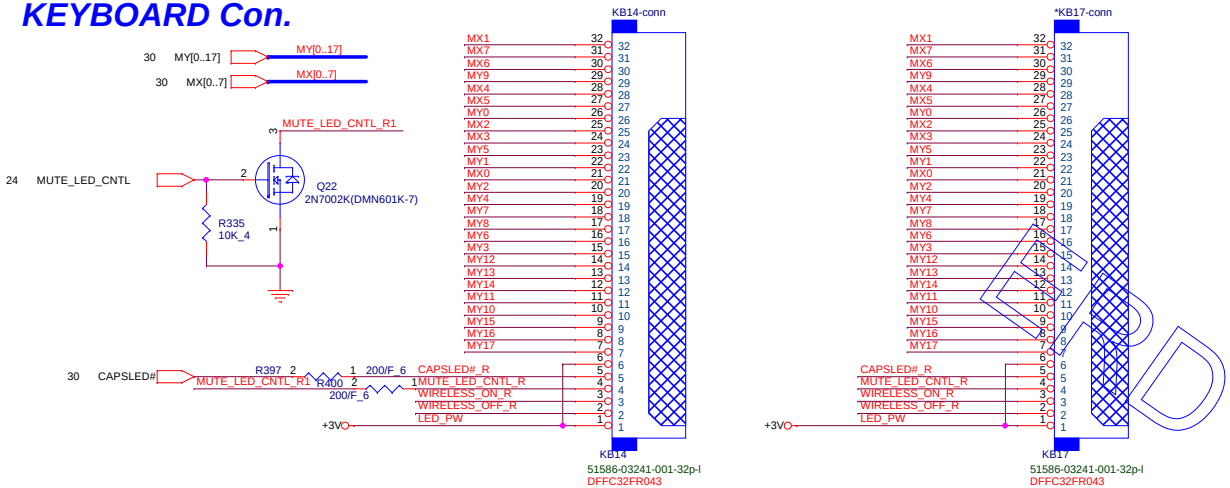


PROJECT : X11	Quanta Computer Inc.
Size C	Document Number: Card Reader
Rev 1A	
Date: Monday, January 05, 2015	Sheet 25 of 40

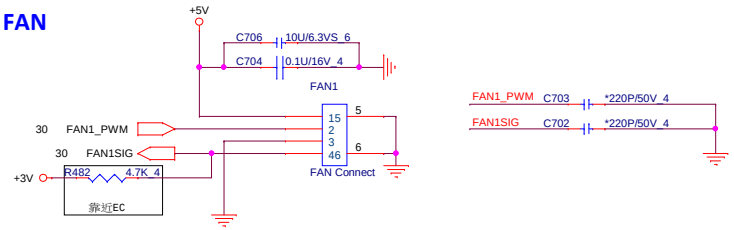
Touch Pad Connector



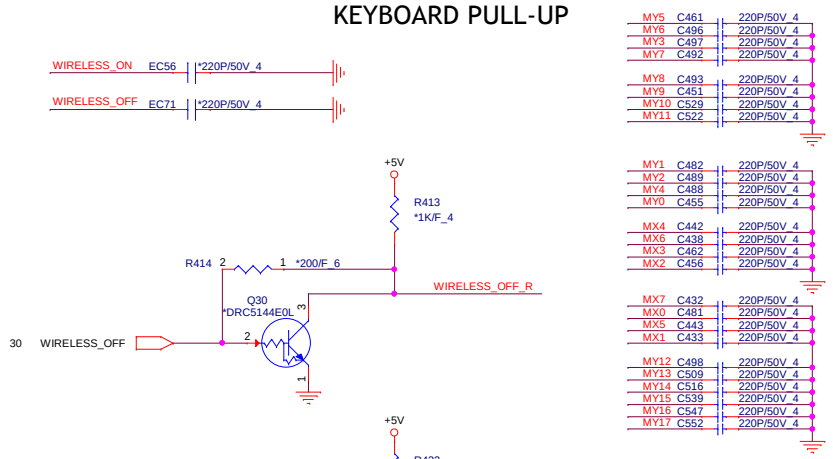
KEYBOARD Con.

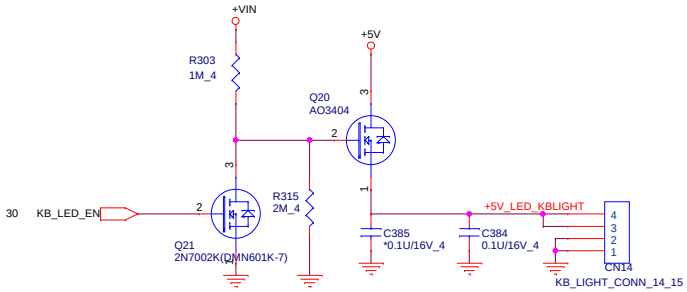


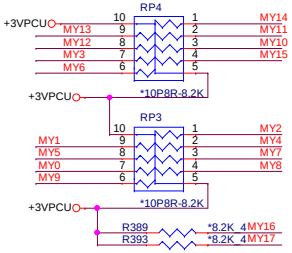
FAN

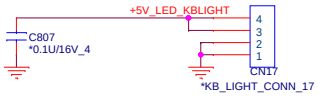


KEYBOARD PULL-UP









PROJECT : X11
Quanta Computer Inc.

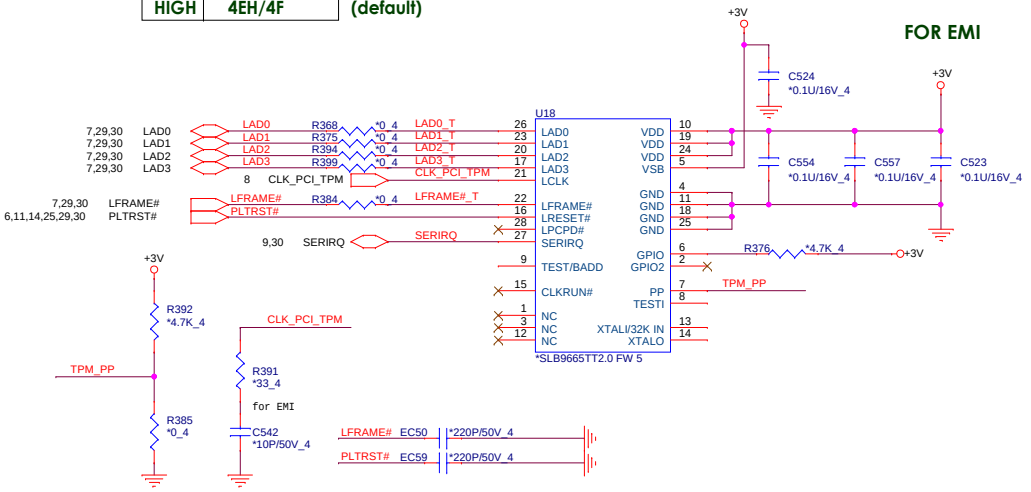
Size	Document Number	Rev
Custom	PB/TP/KB/FAN/EMI Cap	1A
Date: Monday, January 05, 2015	Sheet 26 of 40	

TPM (2.0)

Address

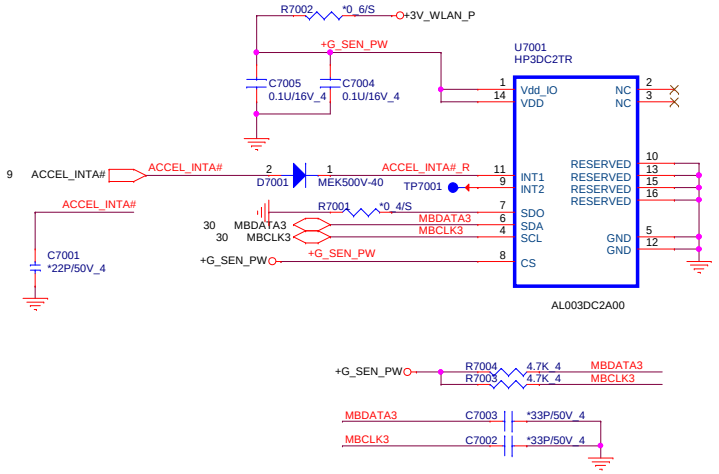
	BADD
HIGH	4EH/4F (default)

FOR EMI

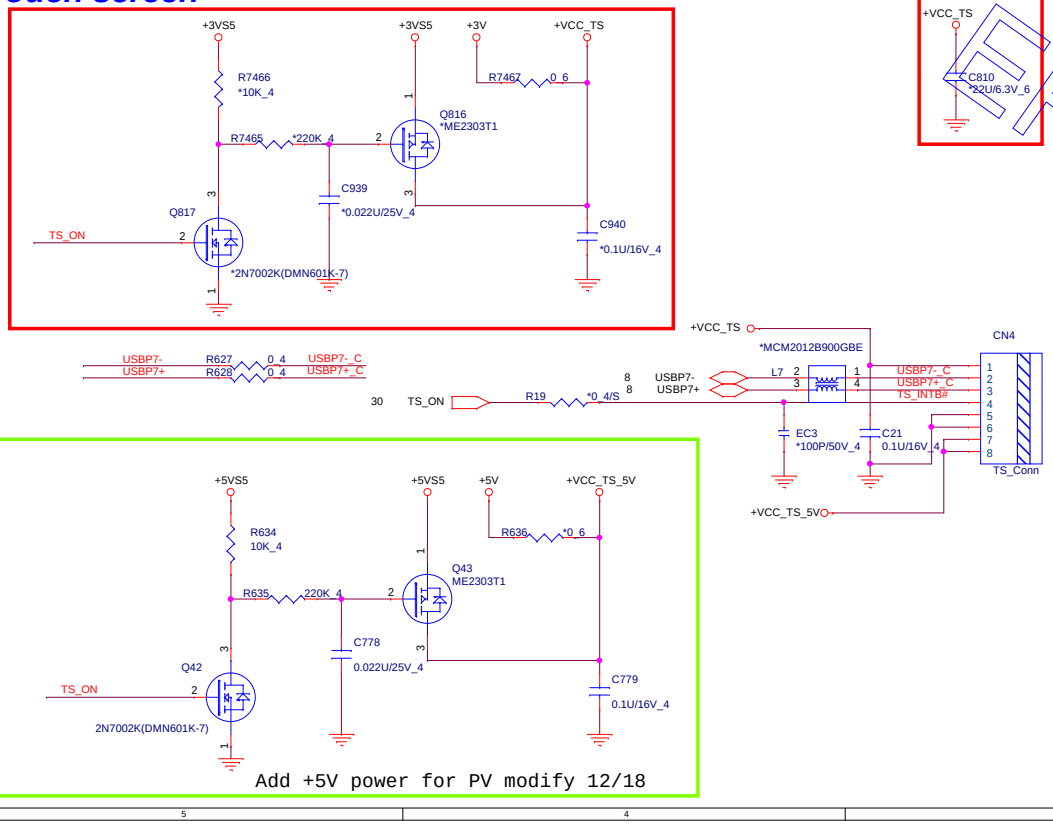


Accelerometer Sensor

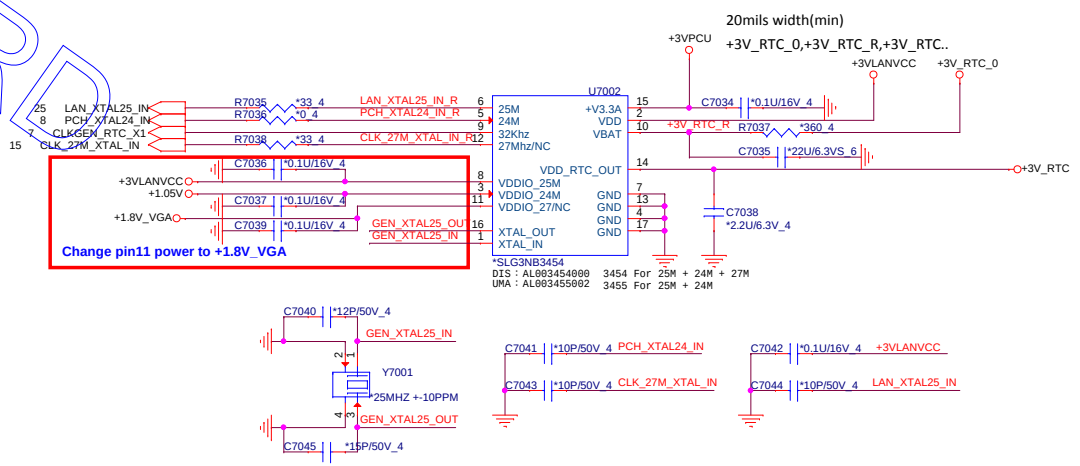
G-Sensor Power need check



Touch screen



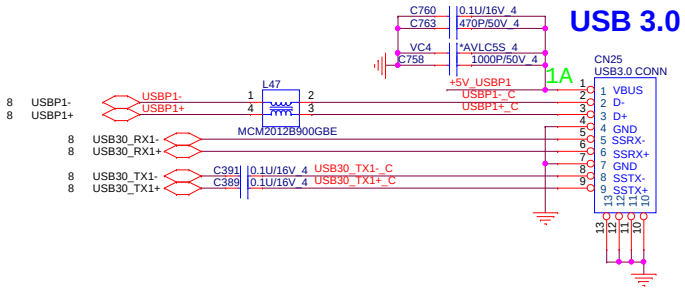
Green CLK Circuitry

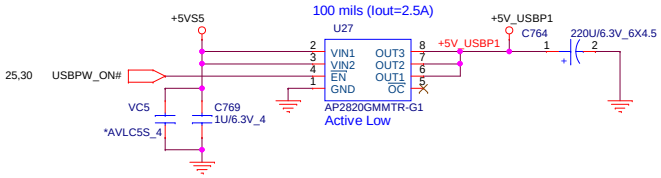


PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TPM/G-Sensor/G-CLK/TS/FP	1A
Date: Monday, January 05, 2015	Sheet 27of 40	

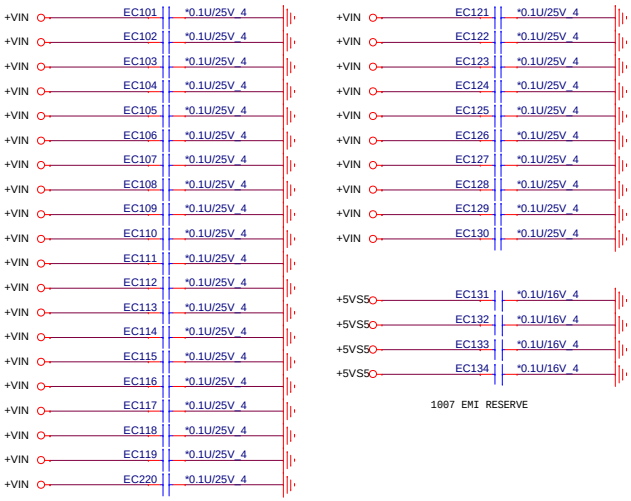
USB 2.0/3.0 Combo





ERD

EMI CAP

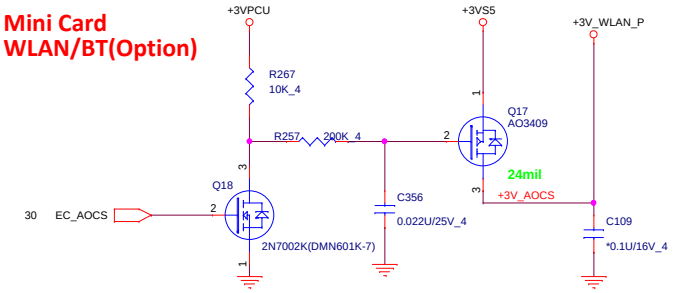


1007 EMI RESERVE

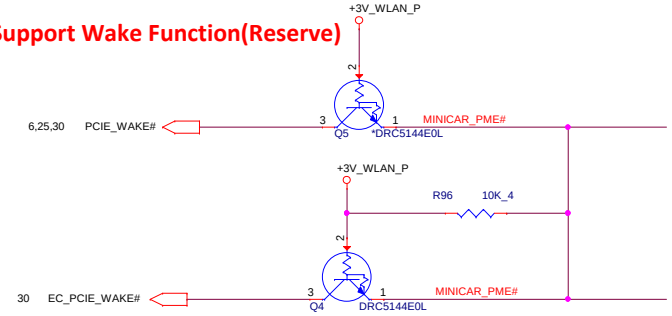
PROJECT : X11
Quanta Computer Inc.

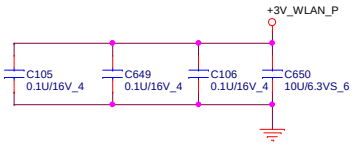
Size	Document Number	Rev
Custom	USB 3.0	1A
Date: Monday, January 05, 2015	Sheet 28 of 40	

Mini Card WLAN/BT(Option)

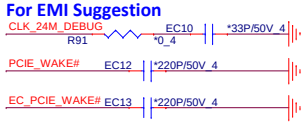


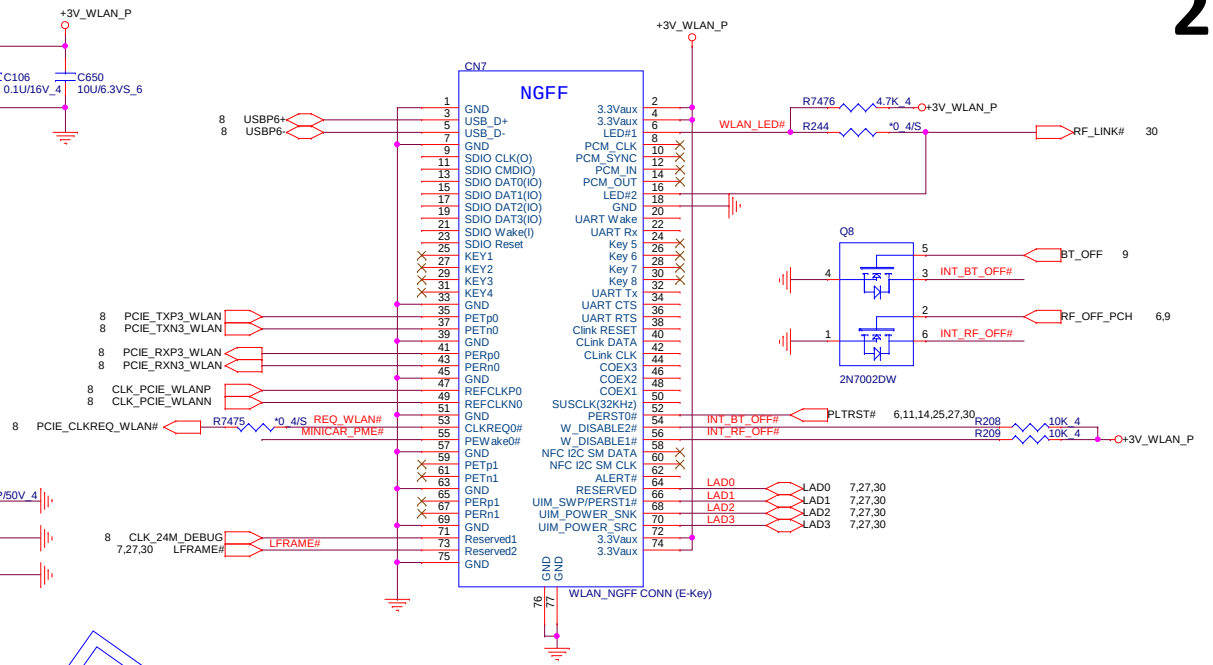
Support Wake Function(Reserve)





For EMI Suggestion

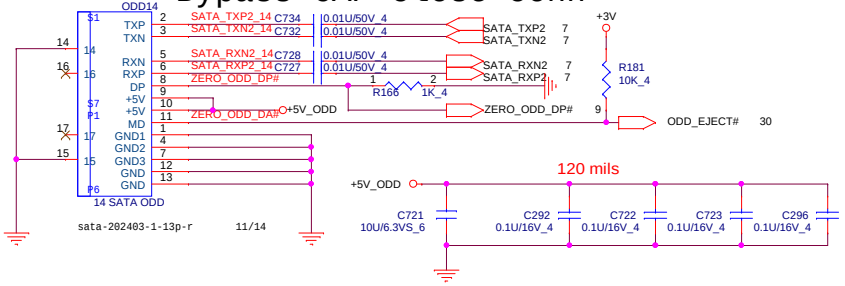




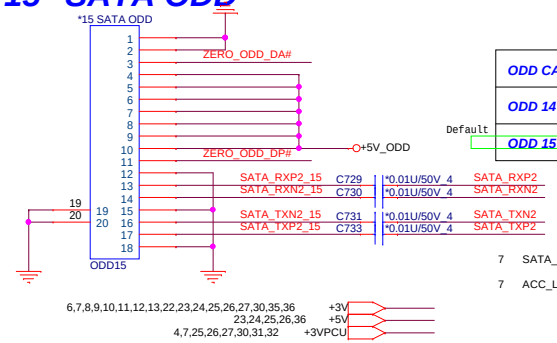
ERD

14" SATA ODD

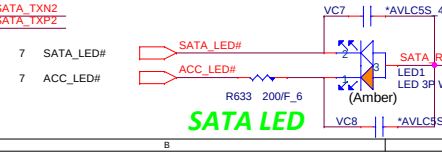
Bypass CAP close conn



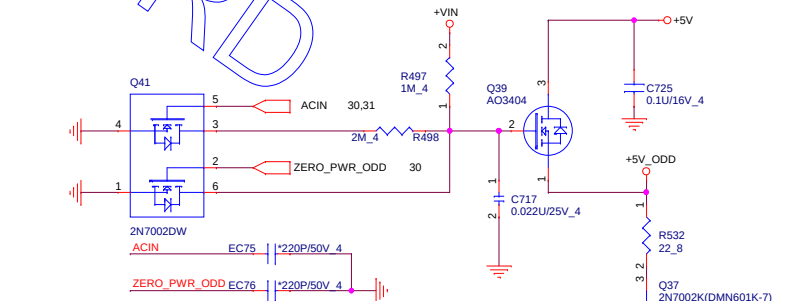
15" SATA ODD



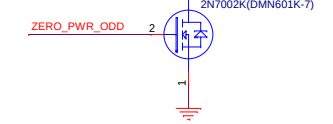
ODD CAP Setting	C727/C728/C732/C734	C729/C730/C731/C733
ODD 14"	O	X
Default ODD 15"/17"	X	O



SATA LED

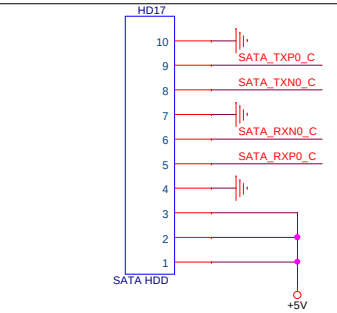


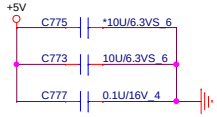
High : ODD power down
Low : ODD power on



PWR LED

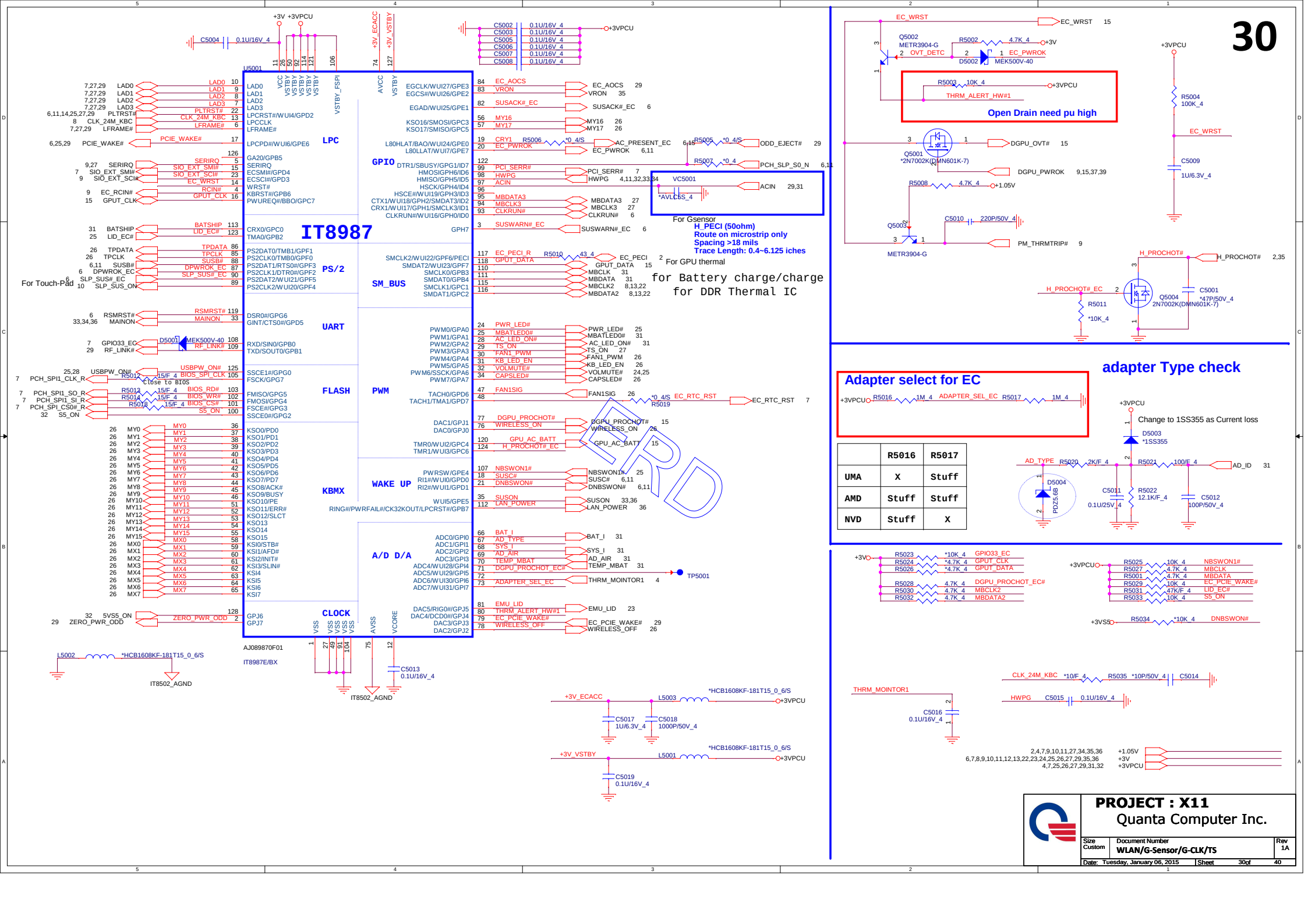
HDD





PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN/NGFF/MSATA	1A
Date: Monday, January 05, 2015	Sheet 29of 40	


30
IT8987
U5001
AJ089870F01
IT8987E/BX
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
for Battery charge/charge
for DDR Thermal IC
For Gsensor
For GPU thermal
For Touch-Pad
Open Drain need pu high
adapter Type check
Adapter select for EC
Change to 1SS355 as Current loss
PROJECT : X11
Quanta Computer Inc.
WLAN/G-Sensor/G-CLK/TS
Date: Tuesday, January 06, 2015
Sheet 30of 40

90W DC_JACK

AD_ID 30

CN20 DC-IN CONN

LED2 LED1

+VA_AC

PL6 *0_8/S

PL4 *0_8/S

PC78 1000P/50V_4

PC5 0.1U/25V_4

EC1 0.1U/25V_4

PQ33 EMB20P03V

IDEA_G

+VAD

PC236 0.1U/25V_4

PD9 P4SMAJ20A

Place this ZVS close to Diode away +VIN

PQ20 AP0203GMT-HF

PC237 2200P/50V_4

BATDIS_G

Do Not add test pad on BATDIS_G signal

PC238 0.1U/50V_6

+PRWSRC

PR211 RC1206-R010

PR228 *0_2/S

PR229 *0_2/S

+VIN

PD10 *P4SMAJ20A

Place this ZVS Far-Far away to +VIN

PQ39 FDMS7698

+BAT_DIS

PR225 4.02K/F_4

BQBATDRV

PC235 0.01U/50V_4

+BATCHG

PL5 *0_8/S

PL7 *0_8/S

BATT+

PC126 0.1U/25V_4

PC127 0.1U/25V_4

14"

2014/9/26 update again

BAT1 BBP28B3-B520A-9H

SMD SMC B_TEMP_MBAT

PR226 330_4

PR227 330_4

30 MBDATA

30 MBCLK

PR230 200K/J_4

+3VPCU

PC247 *100P/50V_4

PC248 *100P/50V_4

PD1 PDZ5.6B

PD2 PDZ5.6B

PR231 1K/F_4

TEMP_MBAT 30

PC242 0.01U/50V_4

PC243 0.01U/50V_4

Place this cap close to EC

For EMI

+PRWSRC

EC9 *1U/25V_4

EC6 *1U/25V_4

EC7 *1U/25V_4

EC8 *1U/25V_4

For ISN

+VIN

PQ36 EMB20N03V

PC12 4.7U/25V_8

PC244 2200P/50V_4

PC245 1000P/50V_4

PC246 0.1U/25V_4

EC15 EC16 EC11 EC14

10U/25V_8

100U/25V_8

+5VPCU

PR235 2.43K/F_6

PC249 1000P/50V_4

PQ41 DRC5144E0L

MBATLED0# 30

+VAD

PQ38 MMDT2907A

PR234 220K_4

PR237 220K_4

PR232 1M_4

PR238 1K_6

+VA

PR241 1M_4

PR233 4.02K/F_4

PC239 1U/25V_6

PC240 0.1U/25V_4

PC241 0.1U/25V_4

BQACP_N

BQACN_N

BQCMSRC

PR239 *0_4/S

PR240 *0_4/S

PV change

PU1 BQ24780RUYR

CMSRC ACDRV BQACDRV 4

BQVCC 28

BQACDET 6

ACDET=16.83V

PR242 10F_8

PC251 1U/25V_6

PD13 1N4448WS-7-F

PR243 *430K/F_4

PR244 430K/F_4

PR246 75K/F_4

PR247 71.5K/F_4

PC252 *1000P/50V_4

PR245 2.43K/F_6

PC253 1000P/50V_4

PQ42 DRC5144E0L

AC_LED_ON# 30

30 AD_AIR

PC254 0.1U/16V_4

PR251 12.4K/F_4

Place this cap close to EC

TP14 PROCHOT#

PR253 *0_4/S

PR254 *100K/F_4

PR268 *0_4/S

PR256 *100K/F_4

+3VPCU

PR248 *0_4/S

MBDATA BQDATA 11

MBCLK BQCLK 12

PR252 0_4/P

BQPROCHOT 10

BQBATPRES 15

BQTB_STAT 16

SDA SCL PROCHOT BATPRES TB_STAT

REGN6V

PR258 100K/F_4

29,30 ACIN

PR260 100K/F_4

ACIN 5

ACOK

BQIADP 7

30 SYS_I

PR261 10F_4

PC259 0.01U/50V_4

PC260 100P/50V_4

BQIBAT 8

IADP IDCHG

Place this cap close to EC

PR265 10F_4

30 BAT_I

PC262 0.01U/50V_4

PC263 100P/50V_4

Place this cap close to EC

VIDCHG = 8 or 16 × (VSRN – VSRP)

ILIM CMPIN CMPOUT PMON

PR263 *0_2/S

PR264 *0_4/S

PC261 100P/50V_4

20mV/W (default)

PR266 100K/F_4

PR267 43.2K/F_4

BQILIM

PV change

REGN HIDRV BQHIDRV 26

PD12 UDZ8V2B-7

PC250 2.2U/10V_6

BTST BQB_2

PR19 2.2_6

BQB_1

PC234 0.047U/25V_4

PHASE BQPHASE 27

PL8 3.3uH/6A(PCMC063T-3R3MN)

LODRV BQLODRV 23

GND 22

PAD 29

PQ37 EMB20N03V

PR14 2.2_6

PC255 2200P/50V_4

BATSRC BQBATSRC 17

PR255 10/F_6

PC256 0.1U/25V_4

PR257 10/F_6

PC257 0.1U/25V_4

SRP BQSRP 20

SRN BQSRN 19

PR259 10/F_6

PC258 0.1U/25V_4

BATDRV BQBATDRV 18

PAD 30 31 32 33 34 35

CSOP CSON

PR137 RC1206-R010

+BATCHG

PC124 PC128 PC130

10U/25V_8

0.1U/25V_4

PD8 RB501V-40

PR249 *0_2/S

PR250 *0_2/S

15"

BAT15 *BBP28B3-B520A-9H

2014/9/26 update again

17"

BAT17 *51483-00801-V01

+BATCHG

PR262 *470_8

30 BATSHIP

PQ43 *DMN601K-7

+3VPCU 4,7,25,26,27,29,30,32

+5VPCU 13,32

PROJECT : X11

Quanta Computer Inc.

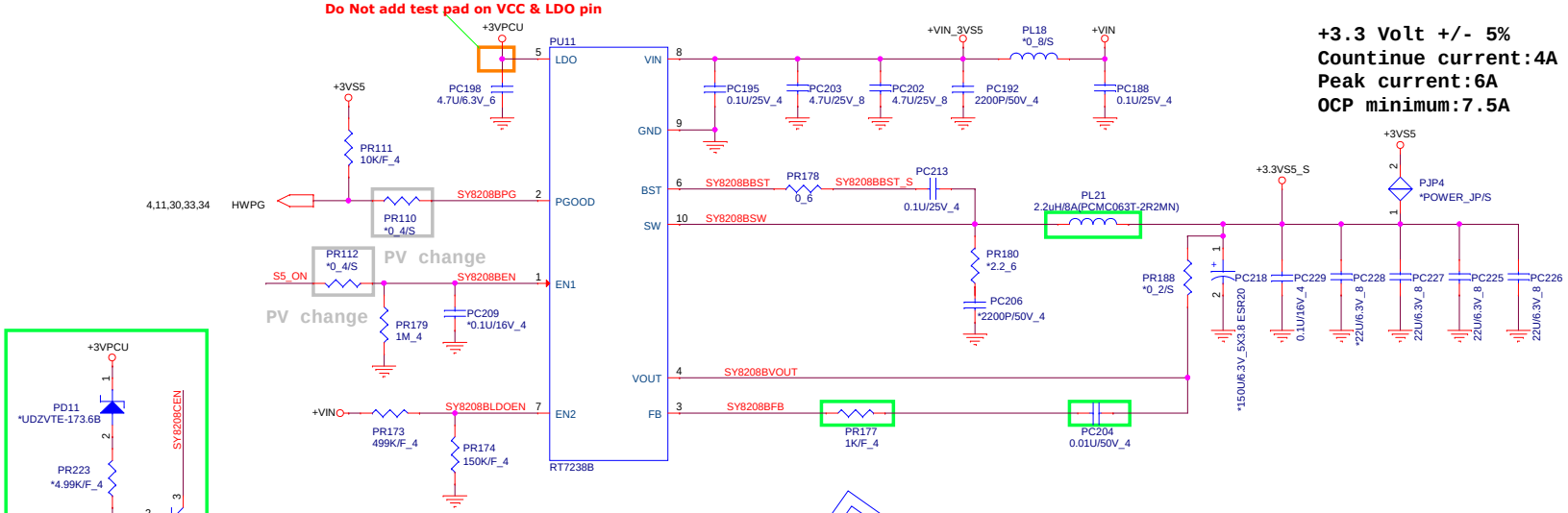
Size	Document Number	Rev
Custom	Charger (BQ24780)	1A

Date: Monday, January 05, 2015 Sheet 31 of 40

+3VS5 6,9,10,11,27,29,30,34,36,37,39
+5VS5 13,25,28,33,34,35,36,37,39

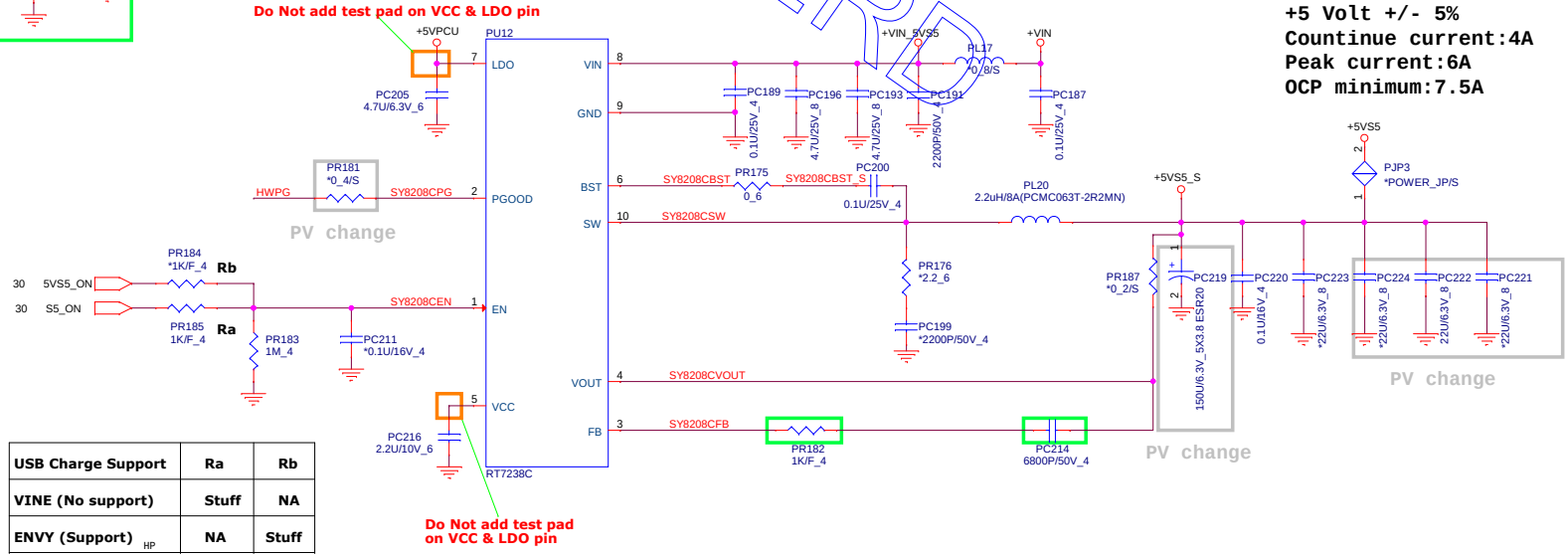
Do Not add test pad on VCC & LDO pin

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



Do Not add test pad on VCC & LDO pin

+5 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



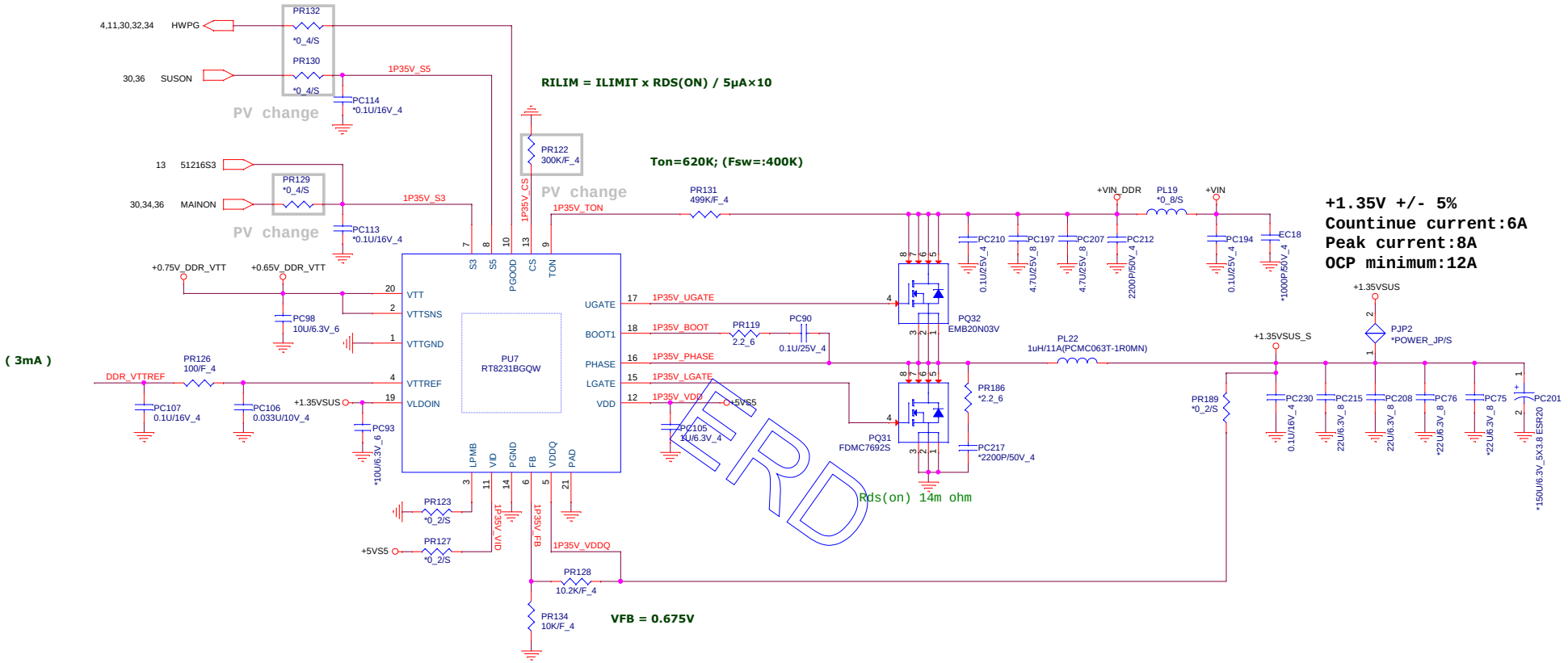
PV change

USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support) HP	NA	Stuff

Do Not add test pad on VCC & LDO pin

PROJECT : X11
Quanta Computer Inc.

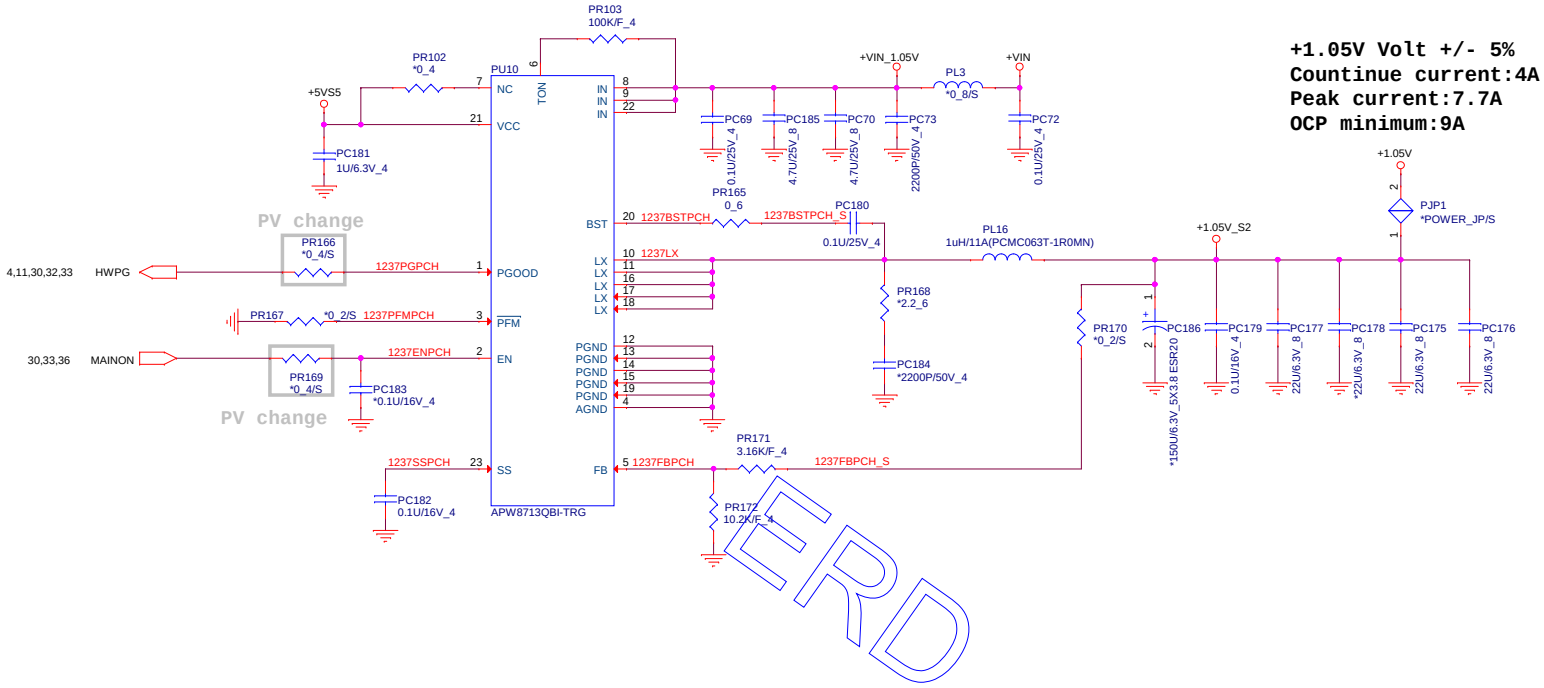
Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A
Date: Monday, January 05, 2015	Sheet 32 of 40	



+0.65V_DDR_VTT 12,13
+5VS5 13,25,28,32,34,35,36,37,39
+VIN 23,26,28,29,31,32,34,35,36,37,38,39
+1.35VSUS 2,4,12,13

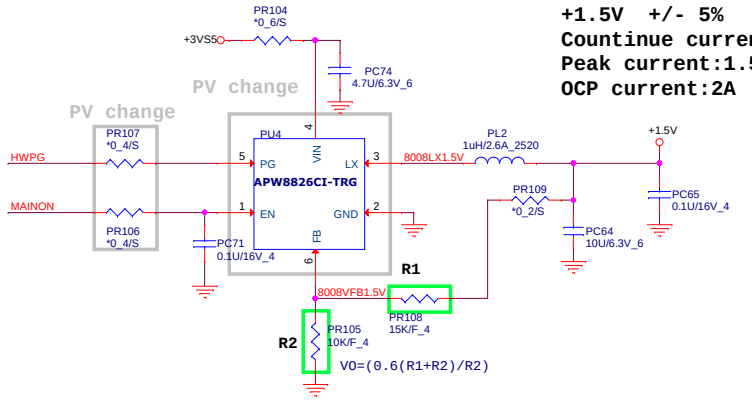
PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8231A)/1.8VS5	1A
Date: Monday, January 05, 2015	Sheet 33 of 40	



ERD

+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A



+1.5V +/- 5%
Countinue current:1.3A
Peak current:1.5A
OCP current:2A

+VIN	23,26,28,29,31,32,33,35,36,37,38,39
+3VS5	6,9,10,11,27,29,30,32,36,37,39
+5VS5	13,25,28,32,33,35,36,37,39

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Monday, January 05, 2015	Sheet 34 of 40	

+VIN 23,26,28,29,31,32,33,34,36,37,38,39
+VCC_CORE 4
+3V 6,7,8,9,10,11,12,13,22,23,24,25,26,27,29,30,36
+5VS5 13,25,28,32,33,34,36,37,39
+V1.05S_VCCST 2,4,7,9,10,11,27,30,34,36

POP Rb and no POP Ra for nex version.

Place this NTC close to inductor

Place this NTC close to MOSFET

For Acoustic

Boot Voltage Table	
R_boot	V_boot
30.1K	0V
49.9K	1.65V
69.8K	1.7V
90.9K	1.75V

PU3 NCP81101MNTXG

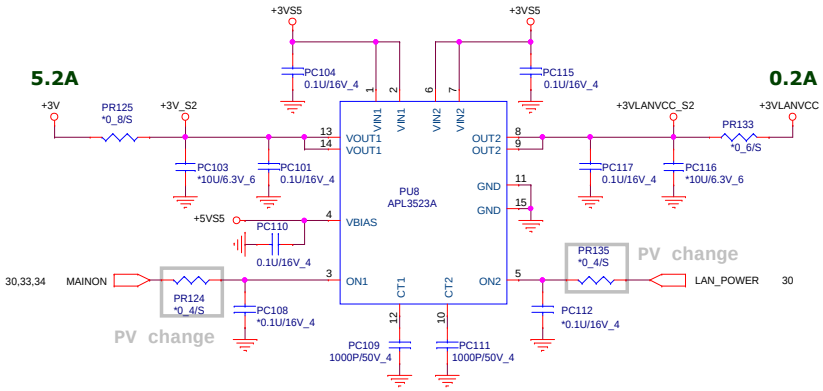
PV change

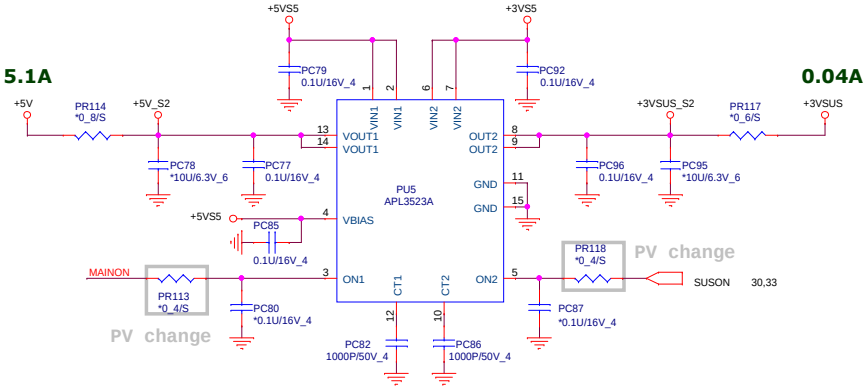
15W
Icc_Max=32A
I_TDC=14A
I_Dynamic=27A
V_Operate=1.6V~1.8V
DC_LL=2m
AC_LL=7m
AC_LL_VOS=9.4m
VBOOT=1.7V

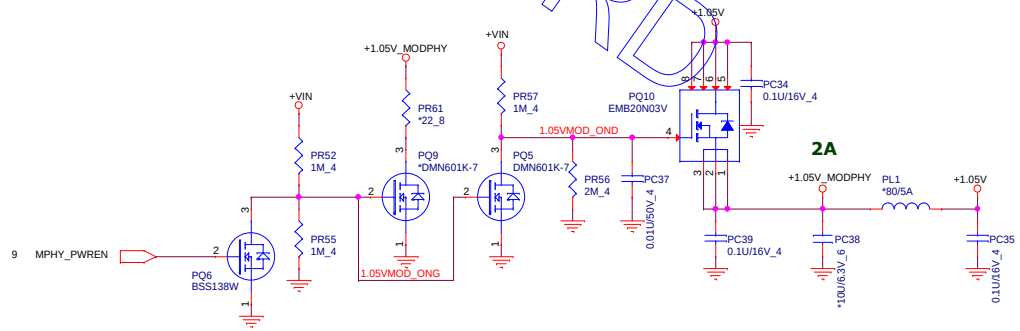
28W
Icc_Max=40A
I_TDC=19A
I_Dynamic=27A
V_Operate=1.6V~1.8V
DC_LL=2m
AC_LL=7m
AC_LL_VOS=9.4m
VBOOT=1.7V

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (NCP81101)ULT	1A
Date: Monday, January 05, 2015	Sheet 35 of 40	







6,7,8,9,10,11,12,13,22,23,24,25,26,27,29,30,35 +3V
23,24,25,26,29 +5V
23,26,28,29,31,32,33,34,35,37,38,39 +VIN
6,9,10,11,27,29,30,32,34,37,39 +3VS5
13,25,28,32,33,34,35,37,39 +5VS5
25,27 +3VLANVCC

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448)	1A
Date: Monday, January 05, 2015	Sheet 36 of 40	

+MVDDQ Volt +/- 5%
Countinue current:6A
OCP_TDC=12.6A
OCP_SPIKE=18A(1ms)
Vboot=0.9V
LL=0 V/A
external offset=0.45V

DCR=9mohm

PV change

VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

Vset1	109.5mV
Delta Vset1	309.9mV
Vset2	121.8mV
Delta Vset2	18.7mV

PUT COLSE TO MVDDQ HOT SPOT

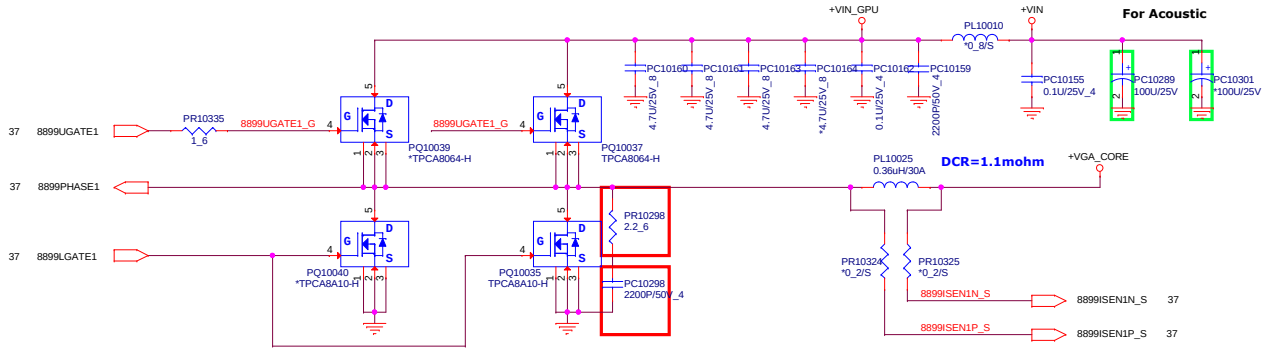
PUT COLSE TO VDDC HOT SPOT

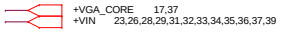
Vih=2V

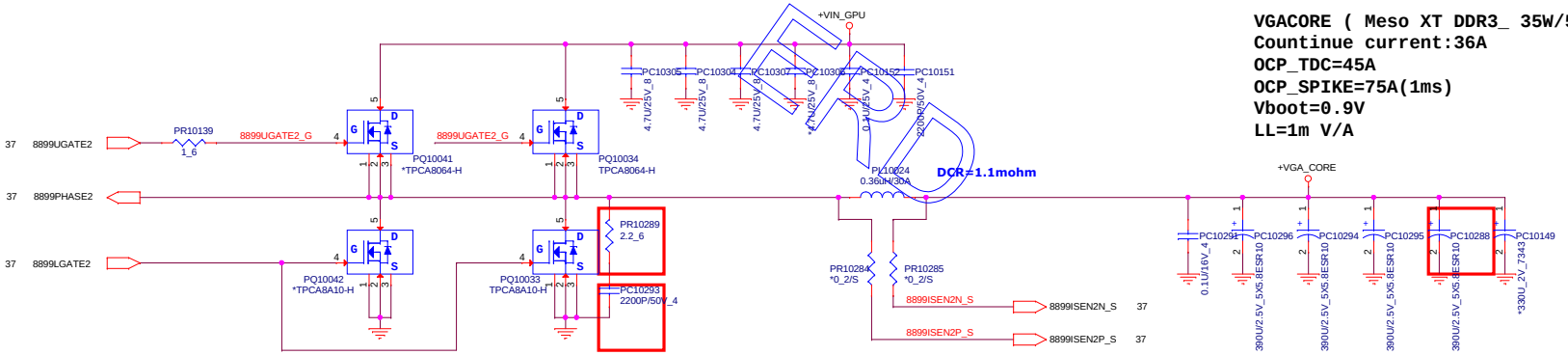
1.65V

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Vcore(RT8899A)	1A
Date: Monday, January 05, 2015	Sheet 37 of 43	

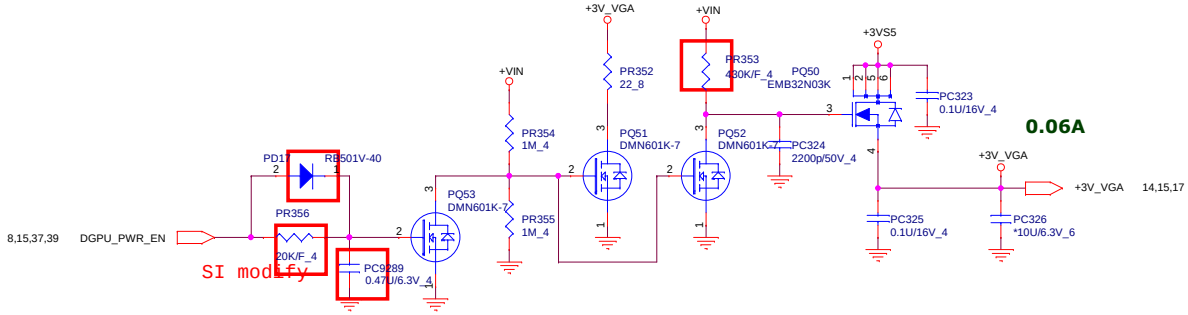




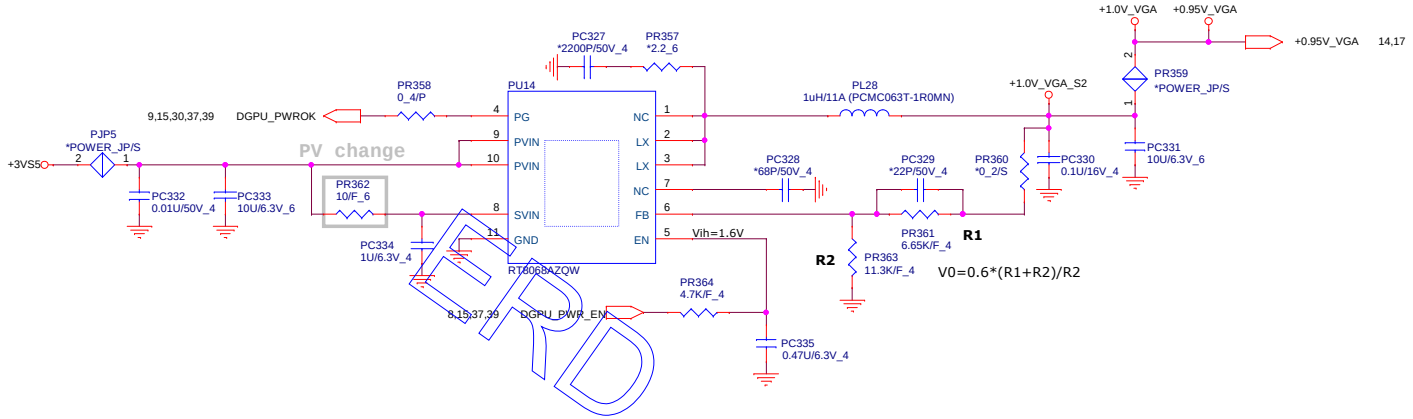


VGACORE (Meso XT DDR3_ 35W/53W(1ms))
Countinue current:36A
OCP_TDC=45A
OCP_SPIKE=75A(1ms)
Vboot=0.9V
LL=1m V/A

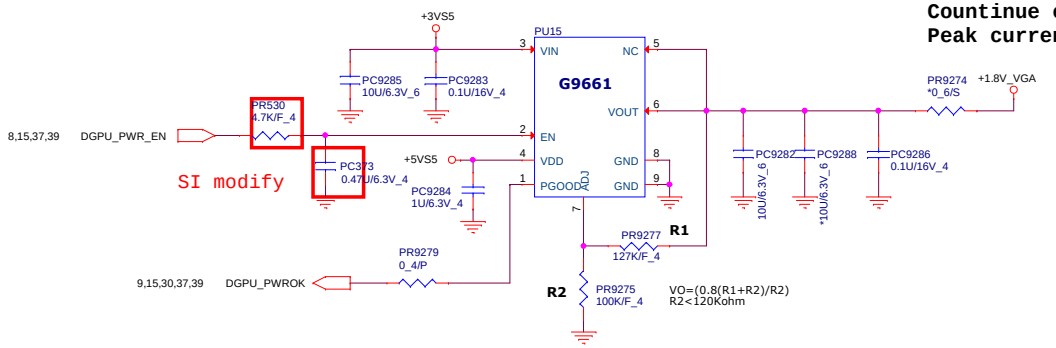
PROJECT : X11 Quanta Computer Inc.			
Size: Custom	Document Number: CPU Core2		Rev: 1A
Date: Monday, January 05, 2015	Sheet 38 of 43		

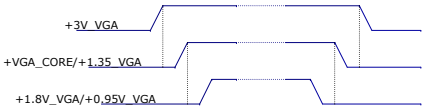


+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A[HP]



+1.8V_VGA +/- 5%
Countinue current:0.5A
Peak current:2A





PROJECT : X11 Quanta Computer Inc.		
Size: Custom	Document Number: **+VGA POWER**	Rev: 1A
Date: Monday, January 05, 2015	Sheet 39 of 9	

Battery Connector	Pavillion	ENVY
14"	-	-
15"	-	-
17"	-	-

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41、42、43 ,but keep below location
Page 41	PC161、PC162
Page 42	PC138、PC144、PC4、PC148
Page 43	PC84、PC102、PC88、PC97、PC40、PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151、PC160	NA
	PQ21、PQ23、PQ25、PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151、PC160	Stuff
	PQ21、PQ23、PQ25、PQ28	Stuff