PROJECT NAME : CAL51/CLA61/CAL71
PCB NO :

Dell / Compal Confidential

Schematic Document

AMD Raven
AMD R17M-M2-50 (23 X 23mm)+GDDR5 x4

2017-11-09 Rev: 1.00 (A00)

@ : Un-pop Component
R5_PC@/R7_PC@/R3_PC/R5_PR@/R7_PR@/R5_PR_R3@/R7_PR_R3@:APU PN
45@: HDMI LOGO
PCB@/: MB part number
4G_S@/4G_M@/4G_H@/2G_H@/2G_M@/2G_S:
VRAM Strap Pin:
Vram 2G:S2G_R3@ / H2G_R3@ /M2G_R3@
Vram 4G:S4G_R3@ / H4G_R3@ /M4G_R3@
DIS@: GPU only
M50_R3@:GPU R3 PN
UMA@/:UMA only
TI@/PARADE@/NRDSA@ : SATA
3234@ :Audio
EMI@/ESD@/RF@ : EMI, ESD ,RF Component
@EMI@/@ESD@/@RF@ : EMI, ESD,RF unpop
KBBL@:for KB backlight use
PTP@/NPTP@/TP_WAKE@:Touch pad
TYPEC@/NOTYPEC@:TYPEC

Typec@EMI@/Tyepc@ESD@: EMI/ESD typec component

CRT@:D-sub TPM@:TPM FFS@:free fall sensor
HDT@ /Debug use
MODS@:moderd standby

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Title: Cover Page

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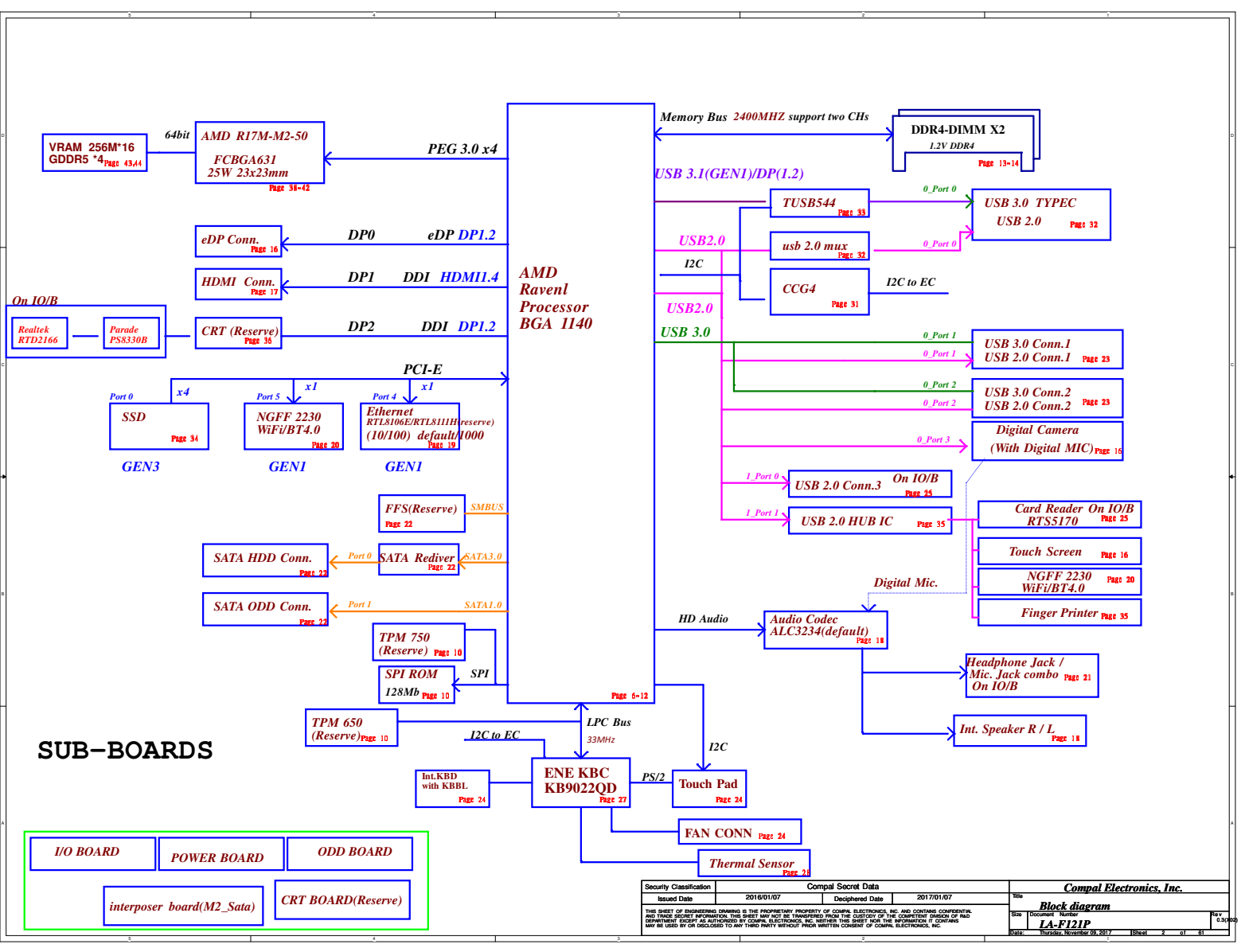
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SUB-BOARDS
I/O BOARD
POWER BOARD
ODD BOARD
interposer board(M2_Sata)
CRT BOARD(Reserve)
Security Classification
Compal Secret Data
Issued Date
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2017/01/07
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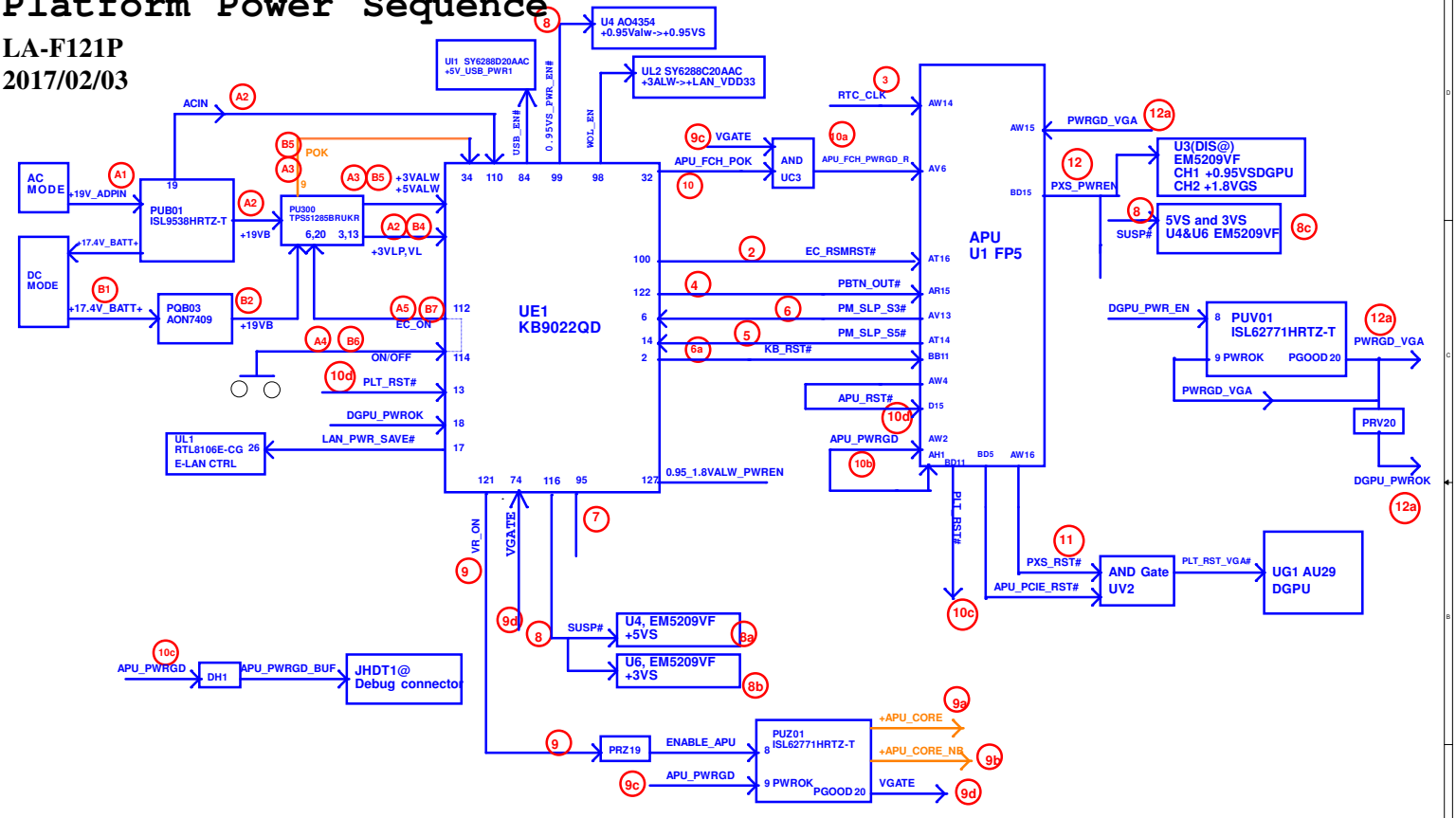
Platform Power Sequence

LA-F121P
2017/02/03



Compal Electronics, Inc.			
Title: Power Sequence diagram			
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Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x13
1	12K +/- 1%	0.347V	0.354V	0.360V	0x14 - 0x1E
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1F - 0x25
3	20K +/- 1%	0.541V	0.550V	0.559V	0x26 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3A
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3B - 0x45
6	43K +/- 1%	0.978V	0.992V	1.006V	0x46 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA4
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF
13	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC0 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD4
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD5 - 0xDD
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDE - 0xF0
19	NC	3.000V	3.300V	3.300V	0xF1 - 0xFF

BOARD ID Table

Board ID	
0	Raven EVT UMA
1	Raven EVT DIS
2	Raven DVT1 UMA
3	Raven DVT1 DIS
4	Raven DVT2 UMA
5	Raven DVT2 DIS
6	Raven Pilot UMA
7	Raven Pilot DIS
8	
9	
10	
11	
12	
13	
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15	
16	
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18	
19	

SMBUS Control Table

	SOURCE	BATT	Charger	DIMM	Thermal Sensor	FFS	CRT	
EC_SMB_CK1 EC_SMB_DA1	KB9022Q	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9022Q				V			
EC_I2C_TPCLK EC_I2C_TPDAT	KB9022Q							
APU_SCLK0 APU_SDATA0	APU			V		V	V	
APU_SCLK1 APU_SDATA1	APU							
APU_SIC APU_SID	APU				V			

PCI EXPRESS(GFX)		
Lane 1	PEG (AMD)M2-50	
Lane 2	PEG (AMD)M2-50	
Lane 3	PEG (AMD)M2-50	RV2 NA
Lane 4	PEG (AMD)M2-50	RV2 NA
Lane 5	RV2 NA	
Lane 6	RV2 NA	
Lane 7	RV2 NA	RV2 Sata only
Lane 8	RV2 NA	RV2 Sata only

	USB3.0	
	0_Port0	TYPE C
	0_Port1	USB3 connector 1
	0_Port2	USB3 connector 2
RV2 NA	0_Port3	progaming DP signal
	1_Port0	
RV2 NA	1_Port1	
	USB2.0	
	0_Port0	TYPE C
	0_Port1	USB connector 1
	0_Port2	USB connector 2
	0_Port3	Camera
ULT	1_Port0	USB connector 1(D/B)
	1_Port1	USB HUB
	PCI EXPRESS(GPP)	
	Lane 1	NVME SSD
	Lane 2	NVME SSD
RV2 NA	Lane 3	NVME SSD
RV2 NA	Lane 4	NVME SSD
	Lane 5	10/100 LAN(GIGA RESERVE)
	Lane 6	NGFF Card (WLAN)
RV2 Sata only	Lane 7	use sata interface
RV2 Sata only	Lane 8	use sata interface
	SATA	
	SATA0	HDD
	SATA1	ODD

CLOCK SIGNAL	
CLKOUT_PCIE0	dGPU
CLKOUT_PCIE1	10/100 LAN(GIGA RESERVE)
CLKOUT_PCIE2	NGFF Card (WLAN)
CLKOUT_PCIE3	NVME SSD

Symbol Note :

: means Digital Ground

: means Analog Ground

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+SDC_IN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A
+19VB	AC or DC for power circuit	N/A	N/A	N/A
+APU_VDDCORE	Core voltage for APU	ON	OFF	OFF
+APU_VDDSOC	VDDSOC voltage for APU	ON	OFF	OFF
+3VALW_APU	3V_always for APU	ON	ON	ON*
+0.8VALW_APU	0.8V_always for APU	ON	ON	ON*
+1.8V_ALW_APU	1.8V_always for APU	ON	ON	ON*
+0.8VS	0.8V_sustain for APU	ON	OFF	OFF
+VGA_CORE	VGA core power rail for GPU	ON	OFF	OFF
+1.35V_MEM_GFX	+1.35VS power rail for GPU and VRAM	ON	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF
+0.95VSDGPU	0.95V power rail for GPU	ON	OFF	OFF
+3.3V_VDD_PIC	3.3V power rail for PD chip	ON	OFF	ON*
+3VALW	System +3VALW always on power rail	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VS	System +3VS power rail	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF
+1.2V_DDR	DDR4/L-RS +1.2V power rail	ON	ON	OFF
+2.5V_MEM	DDR4/L-RS +2.5V power rail	ON	ON	OFF
+1.8VS	System +1.8VS power rail	ON	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON*
+5VS	System +5VS power rail	ON	OFF	OFF
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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Title: Notes List

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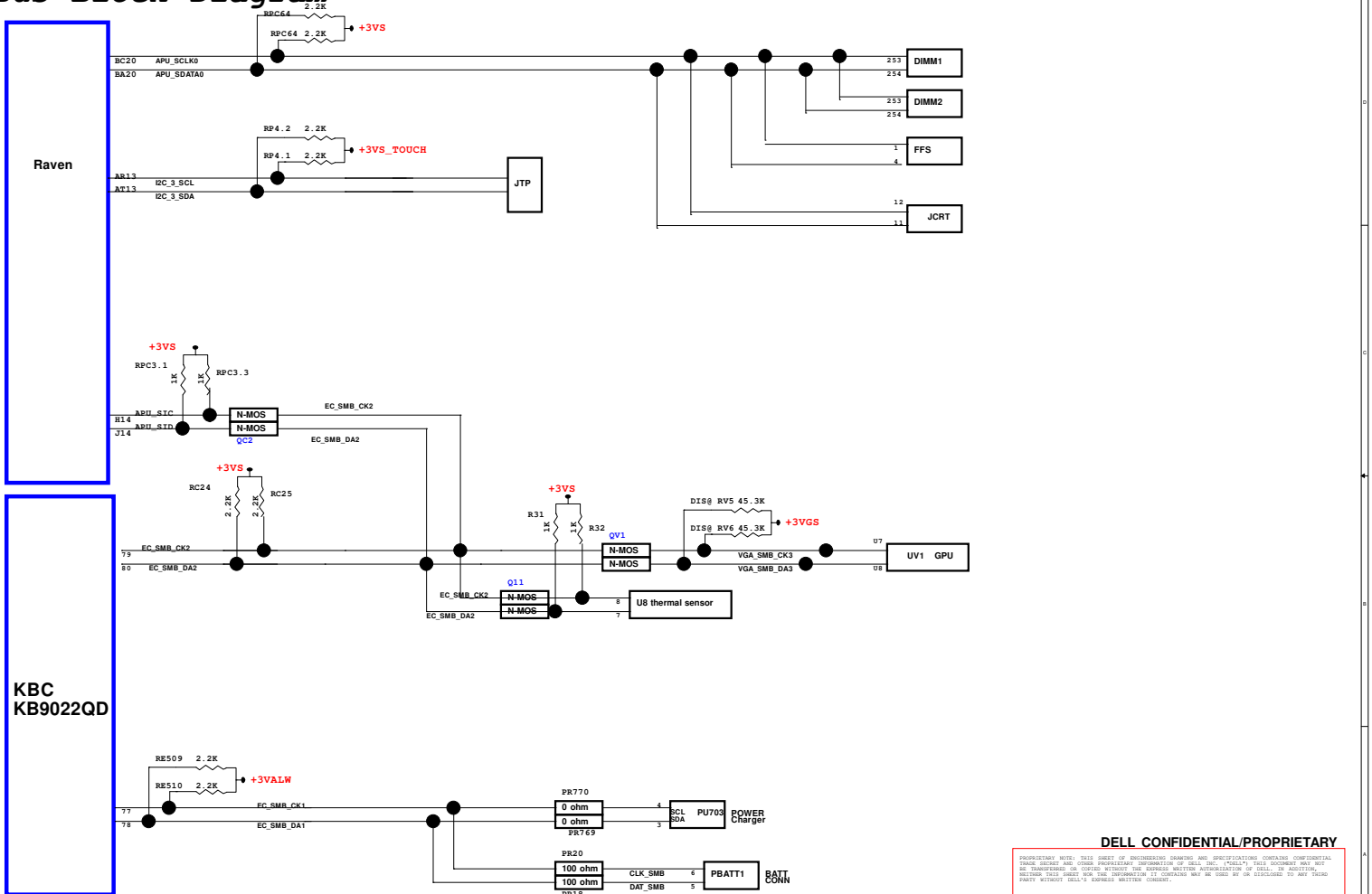
SMBus Block Diagram



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Title: SMBus block diagram			
Size:	Document Number: LA-F121P		Rev: 0.3(0.0)
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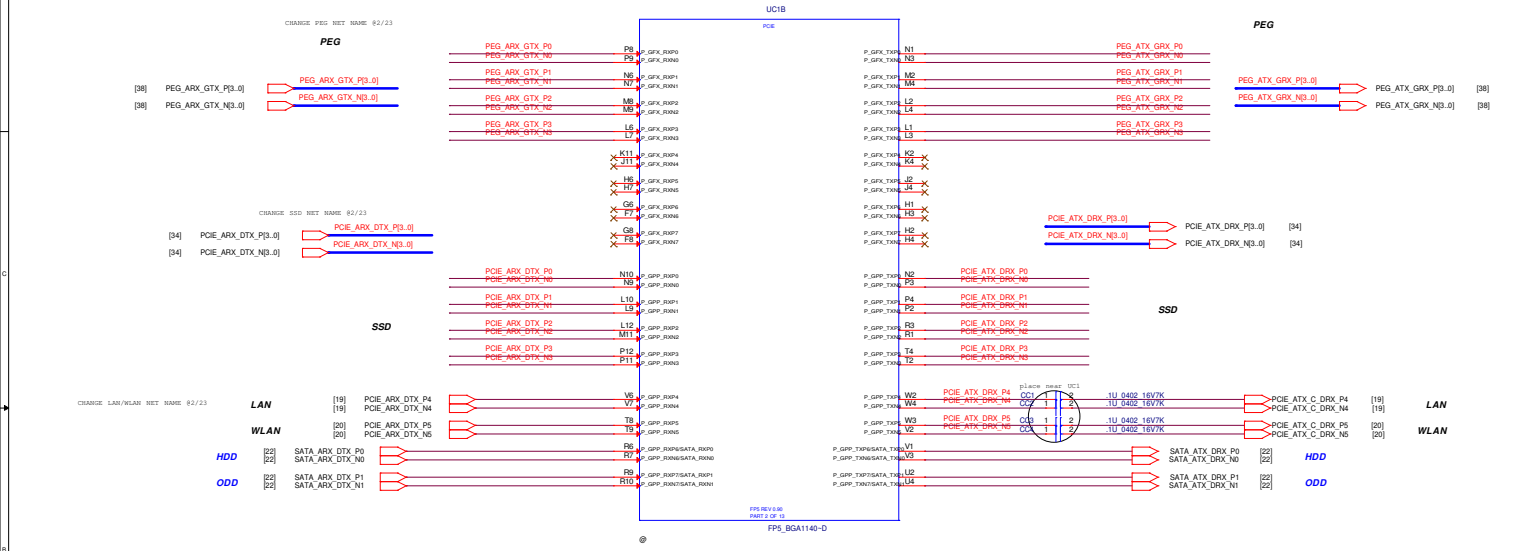
Main Func = CPU



UC1 SA0000BBJ0L
R3_PC@
S IC RAVEN3 ZM2300C4T2OFB 2G BGA 1140 APU

UC1 SA0000BBJ1L
R3_PR@
S IC RAVEN3 YM2200C4T2OFB 2.5G BGA 1140 APU

UC1 SA0000ASA2L
R7_PC@
S IC RAVEN7 ZM2000C4T4MF2 2G BGA 1140 APU

UC1 SA0000ASA3L
R7_PR@
S IC RAVEN7 YM2700C4T4MFB 2G BGA 1140 APU

UC1 SA0000ASA4L
R7_PR_R3@
S IC RAVEN7 YM2700C4T4MFB 2.2G BGA 1140 APU A31 !

UC1 SA0000A8R0L
R5_PC@
S IC RAVEN5 ZM1800C4T4MF2 1.8G BGA 1140 APU

UC1 SA0000A8R1L
R5_PR@
S IC RAVEN5 YM2500C4T4MFB 1.8G BGA 1140 APU

UC1 SA0000A8R2L
R5_PR_R3@
S IC RAVEN5 YM2500C4T4MFB 2G BGA 1140 APU A31 !

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Title: FP4 PCIE/UMI

Size	Document Number	Rev
Custom	LA-F121P	0.3(X02)

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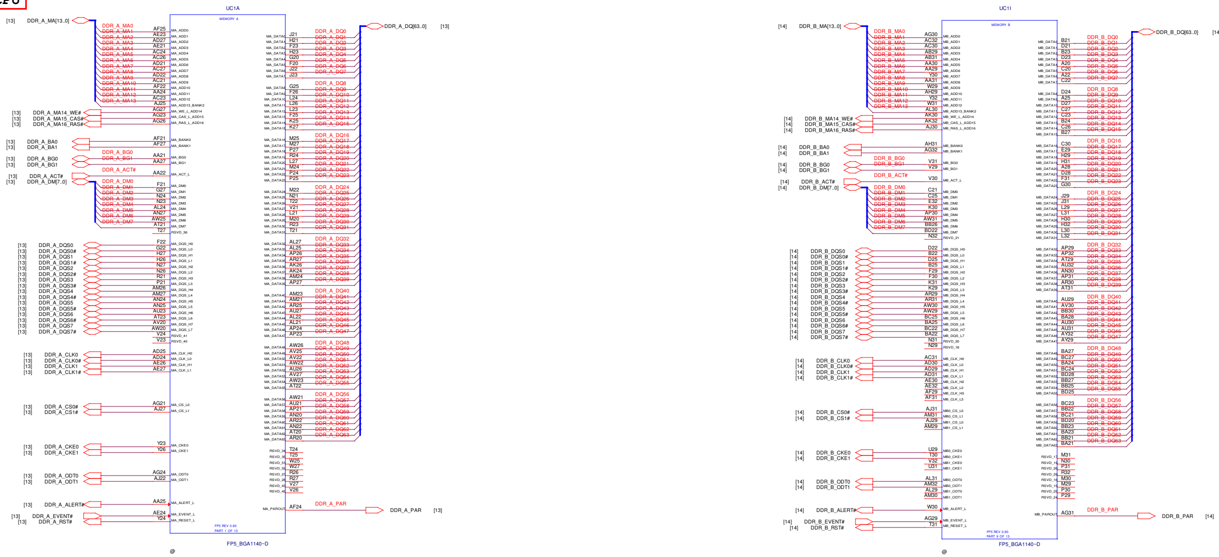
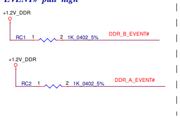


EVENT# pull high



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Title: FP4 DDR4 MEMORY I/F

Size: Custom | Document Number: LA-F121P | Rev: 0.3(X02)

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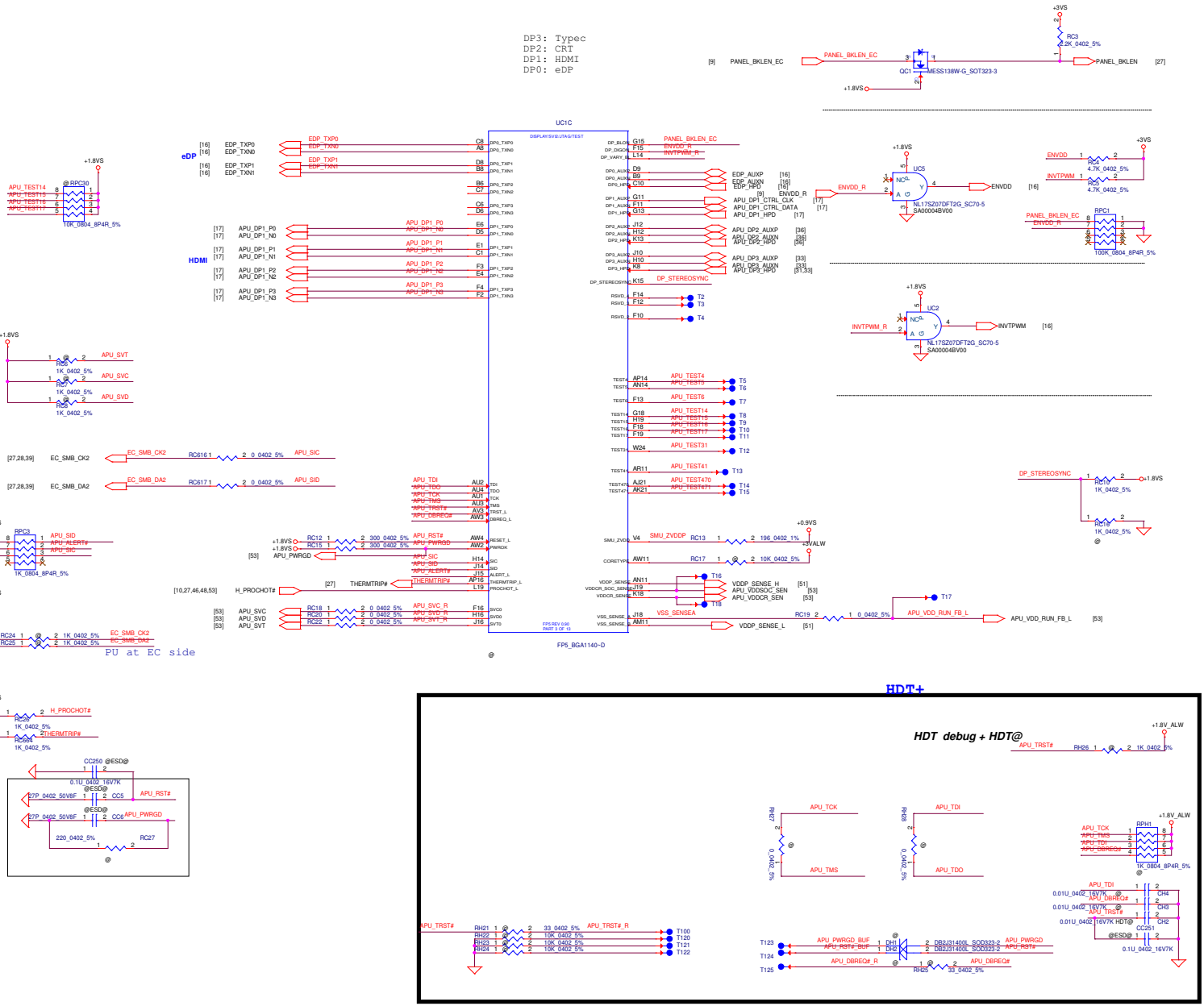
Main Func = CPU

DP3: Typec
DP2: CRT
DP1: HDMI
DP0: eDP



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Compal Electronics, Inc.

Title: FP4 DISP/MISC/HDT

Size	Document Number	Rev
Custom	LA-F121P	0.3(002)

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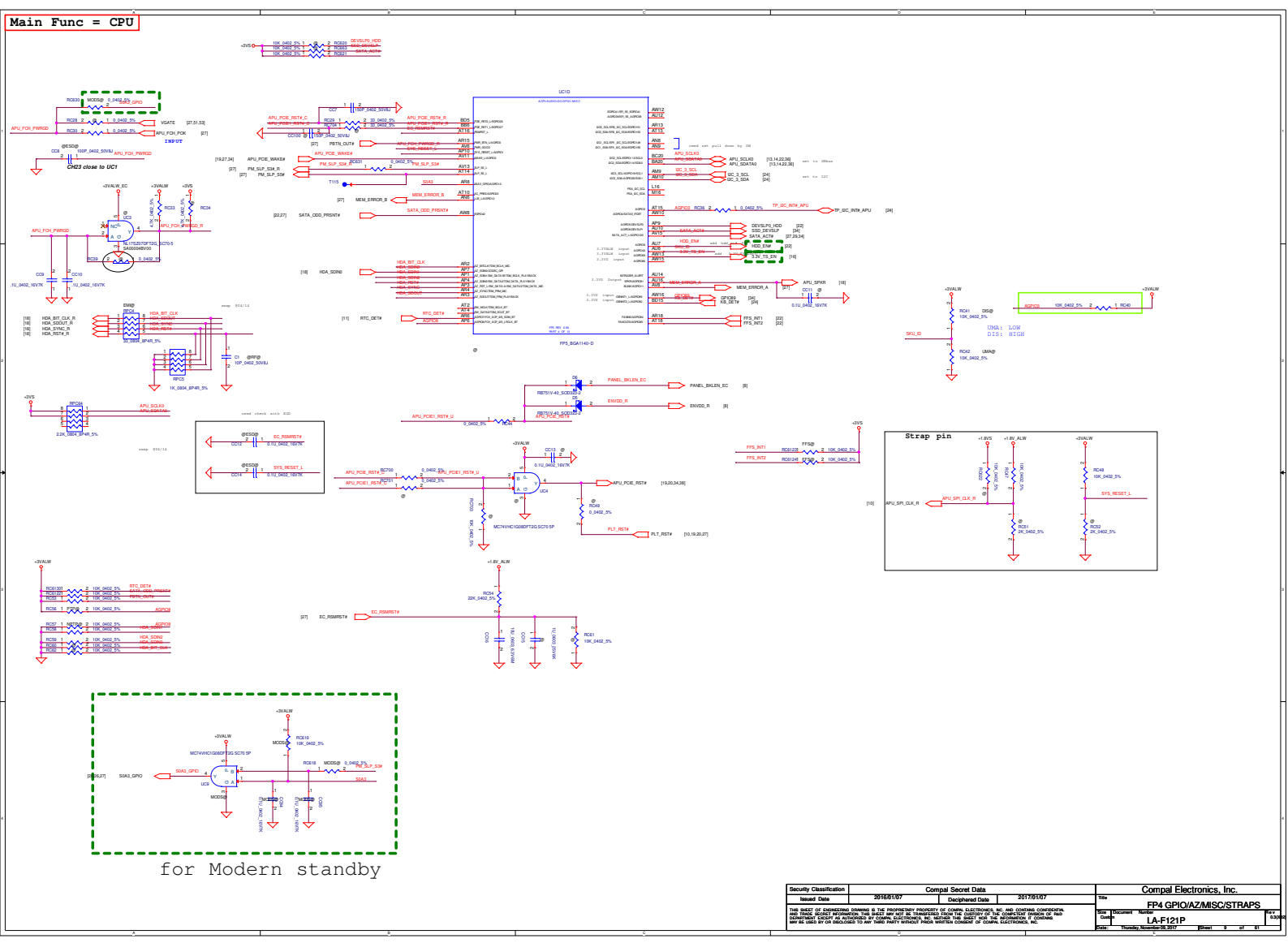

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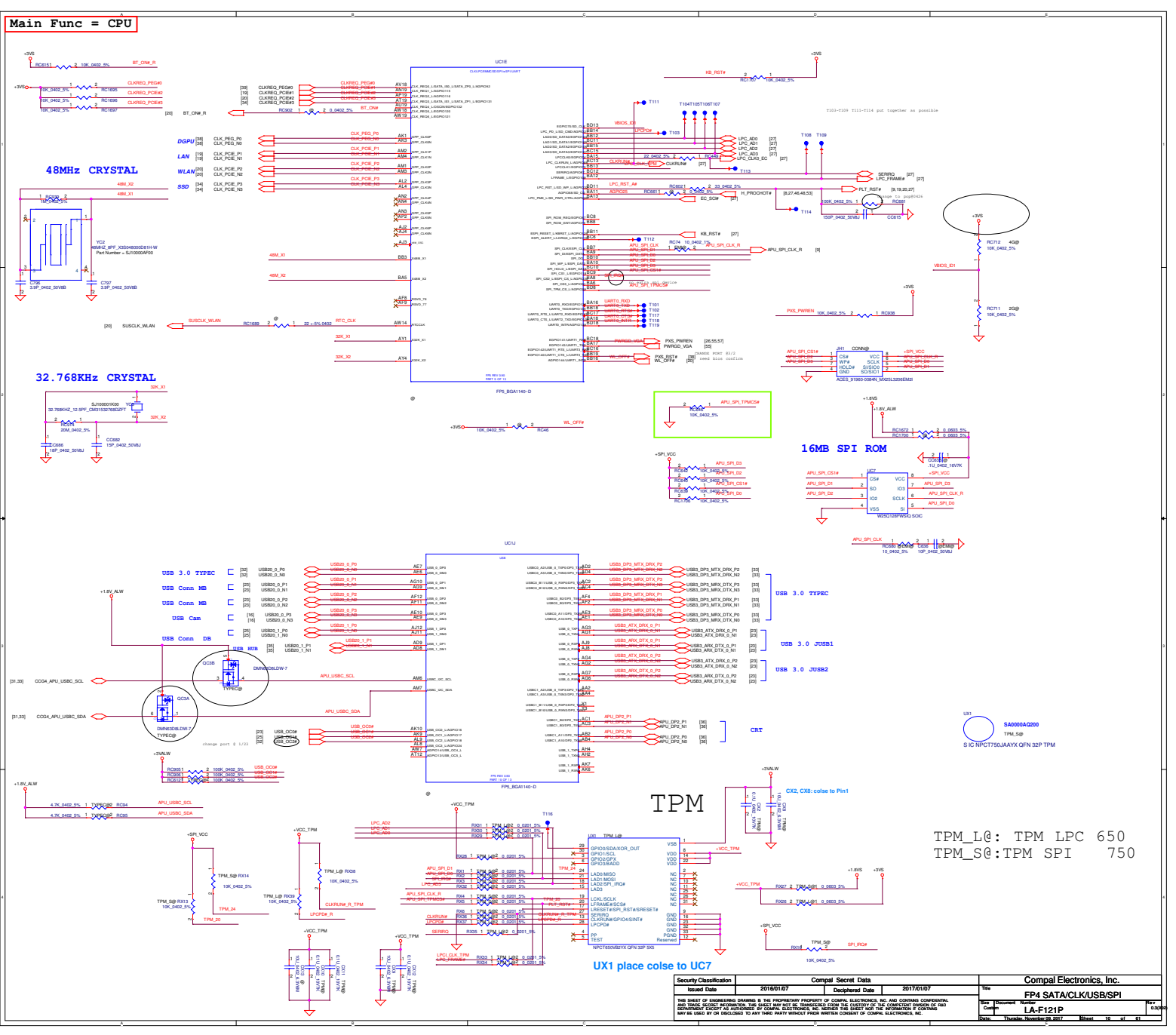

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Title	FP4 SATA/CLK/USB/SPI		
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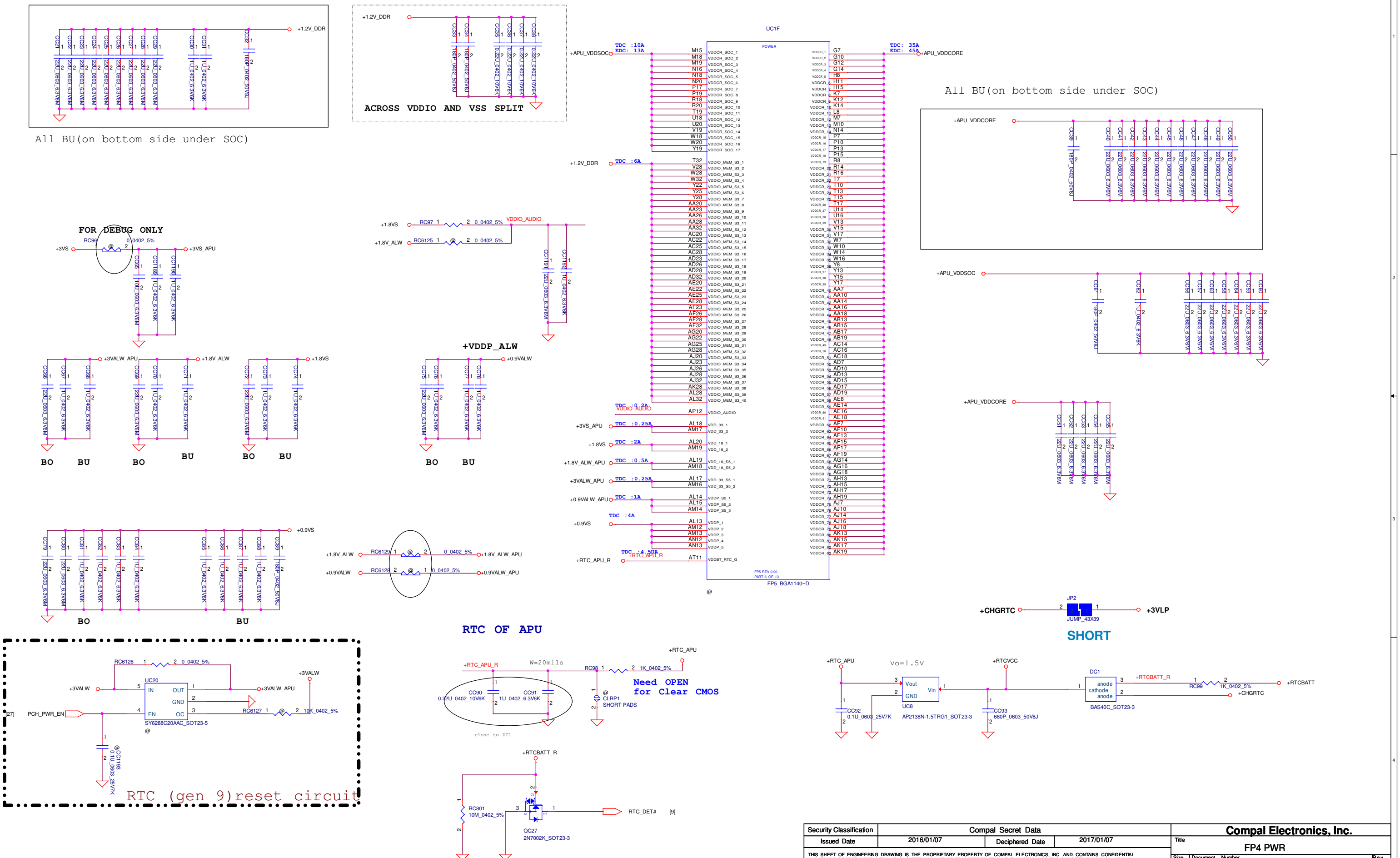

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Title: FP4 PWR

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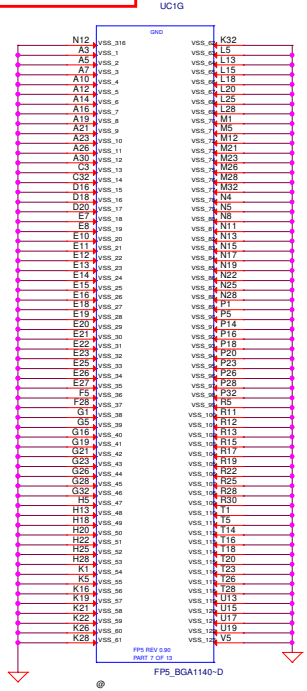

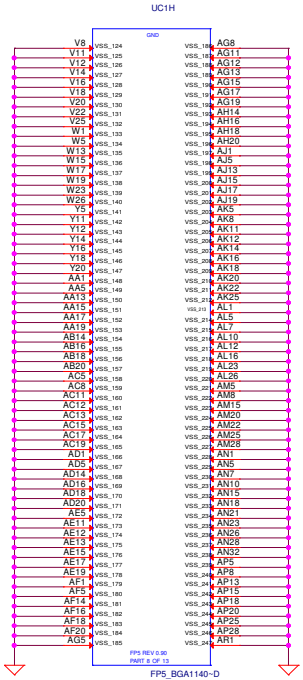

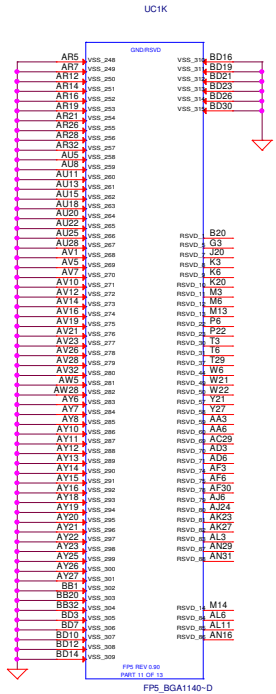

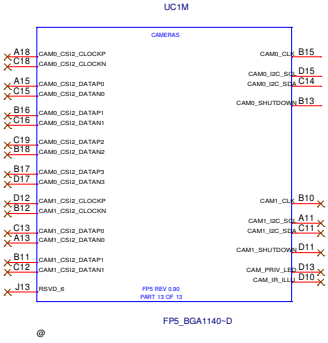

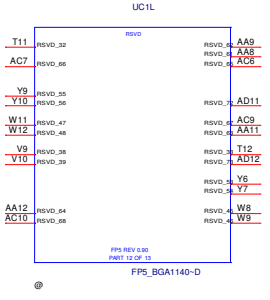

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Compal Electronics, Inc.

Title: FP4 GND

Size	Document Number	Rev
Custom	LA-F121P	0.3(X02)

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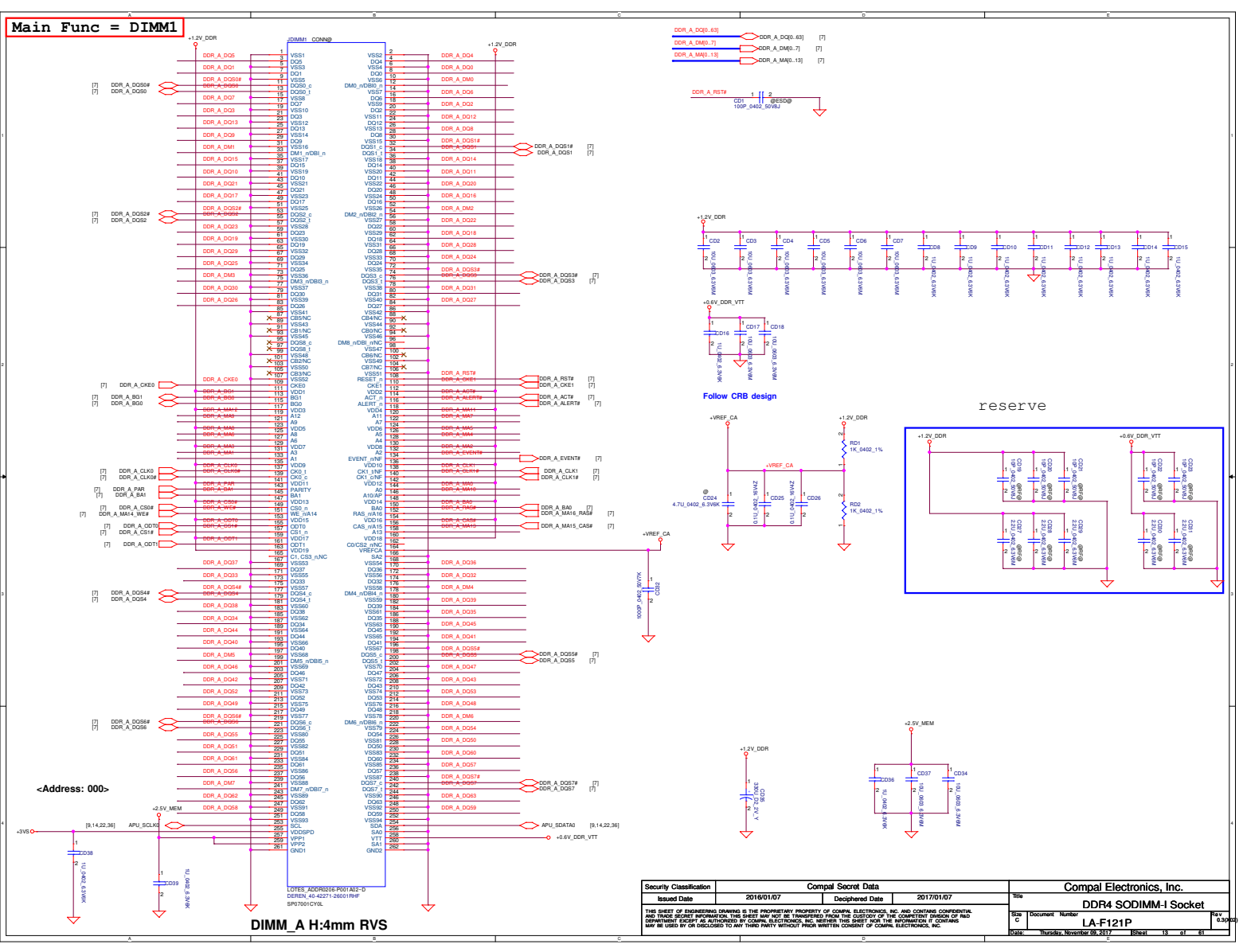

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Compal Electronics, Inc.			
Title	DDR4 SODIMM-I Socket		
Size C	Document Number LA-F121P		Rev 0.3(NOS)
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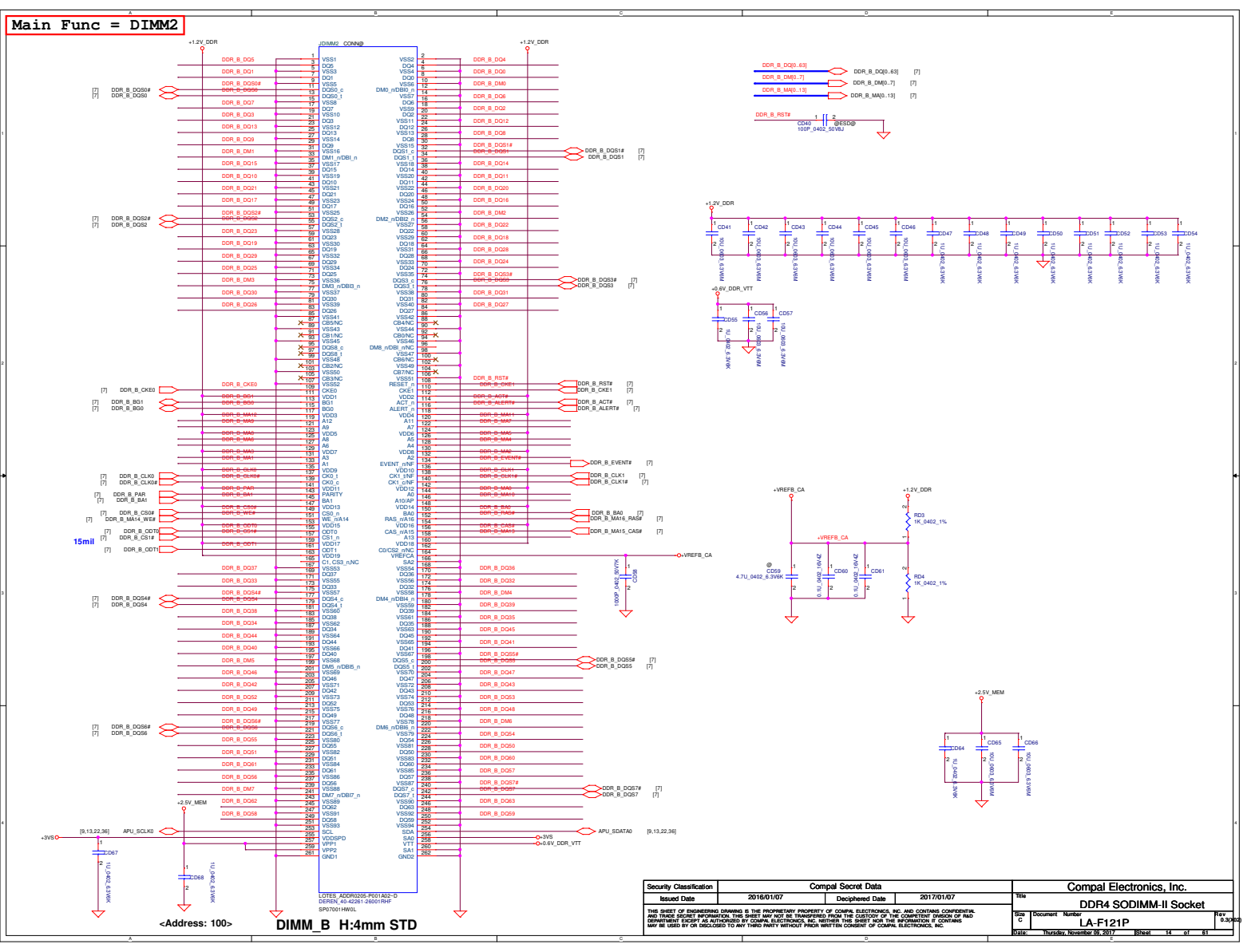
Main Func = DIMM2



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: DDR4 SODIMM-II Socket			
Size: C	Document Number: LA-F121P		Rev: 0.3(0G)
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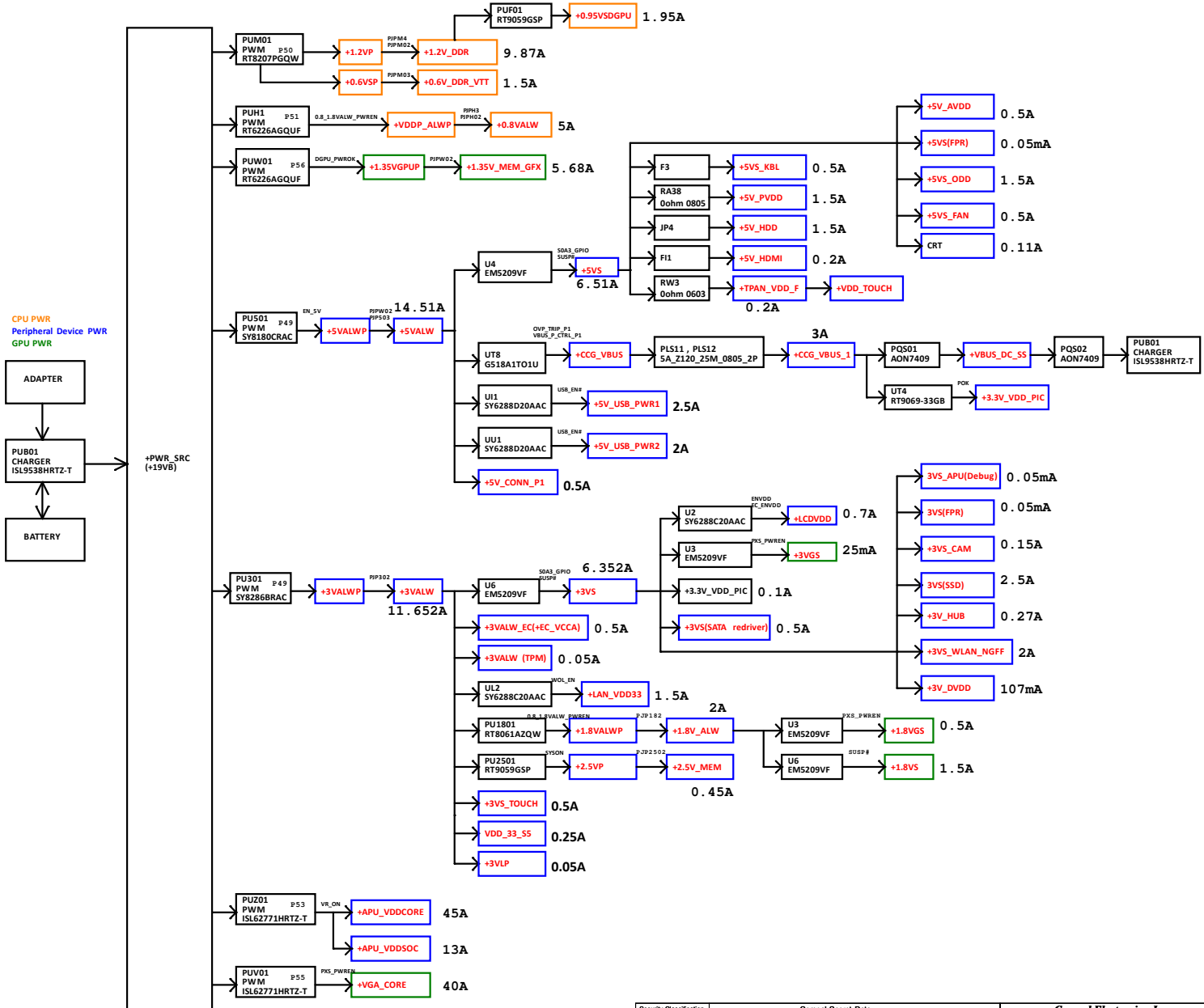

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: Green CLK			
Size:	Document Number: LA-F121P		Rev: 0.3(0G)
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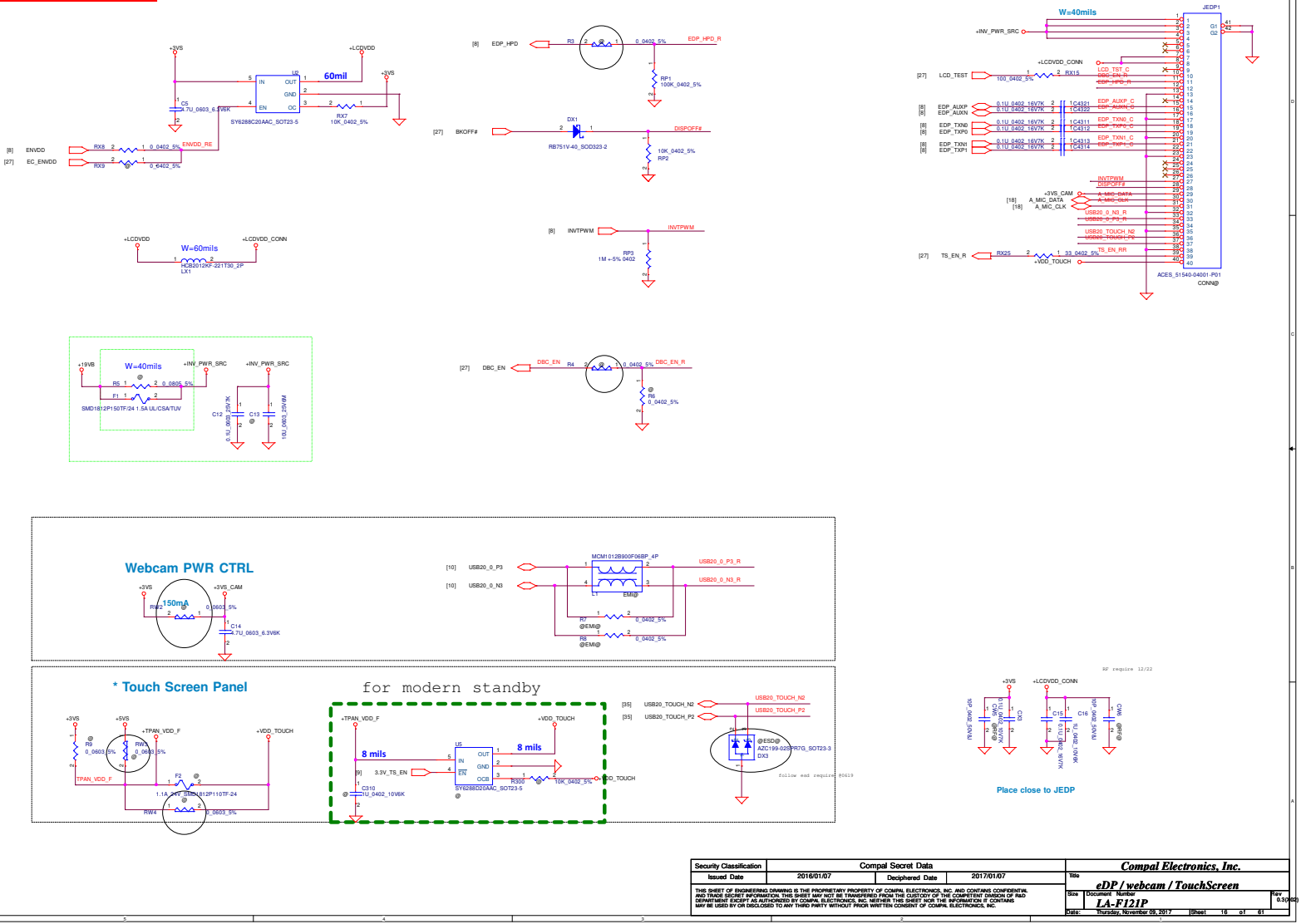

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Issued Date	2016/01/07	Deciphered Date	2017/01/07

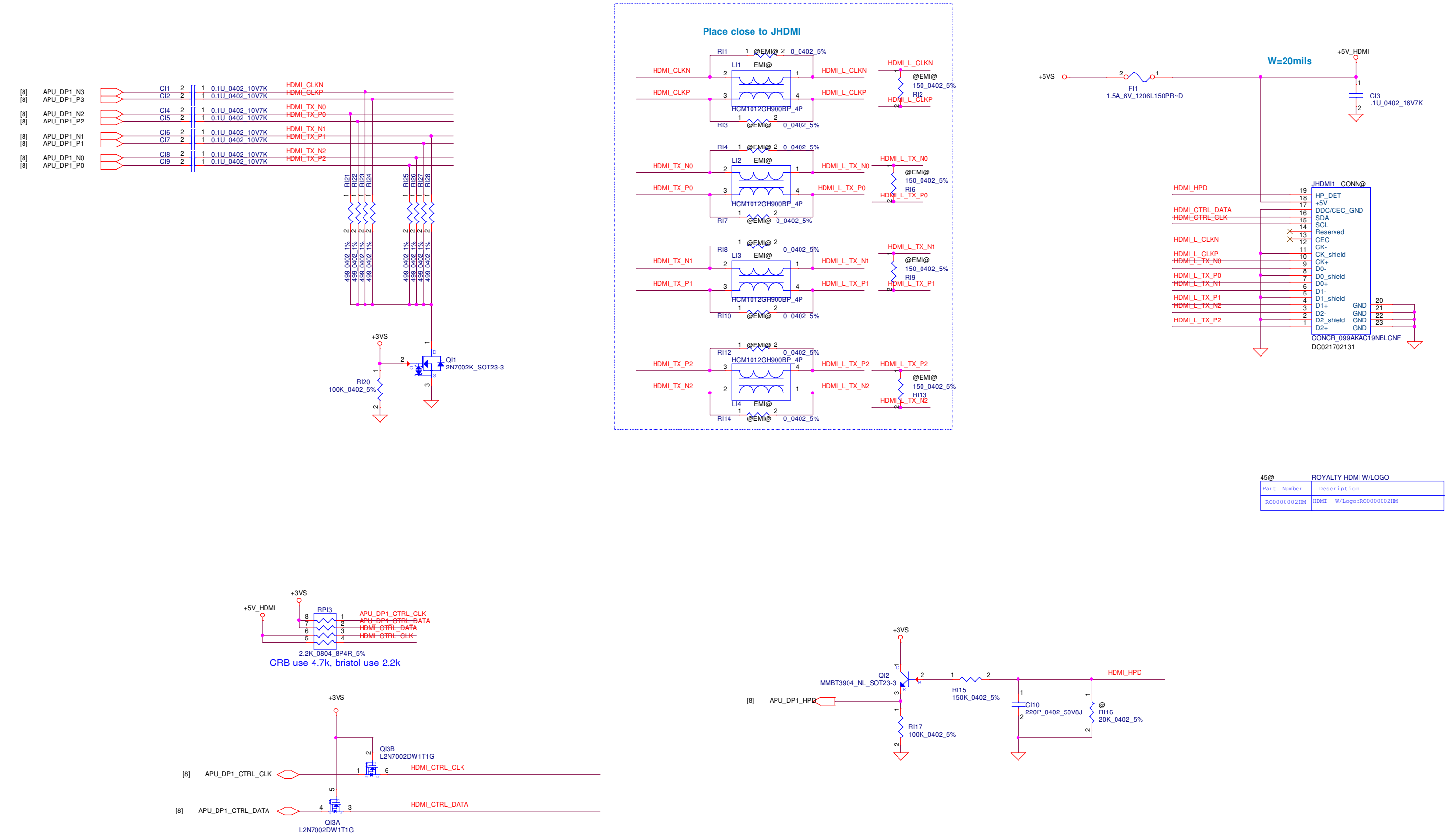
Compal Electronics, Inc.

Title: **eDP / webcam / TouchScreen**

Size	Document Number	Rev
	LA-F121P	0.3(0G)

Date: Thursday, November 09, 2017 | Sheet 16 of 61

Main Func = HDMI



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

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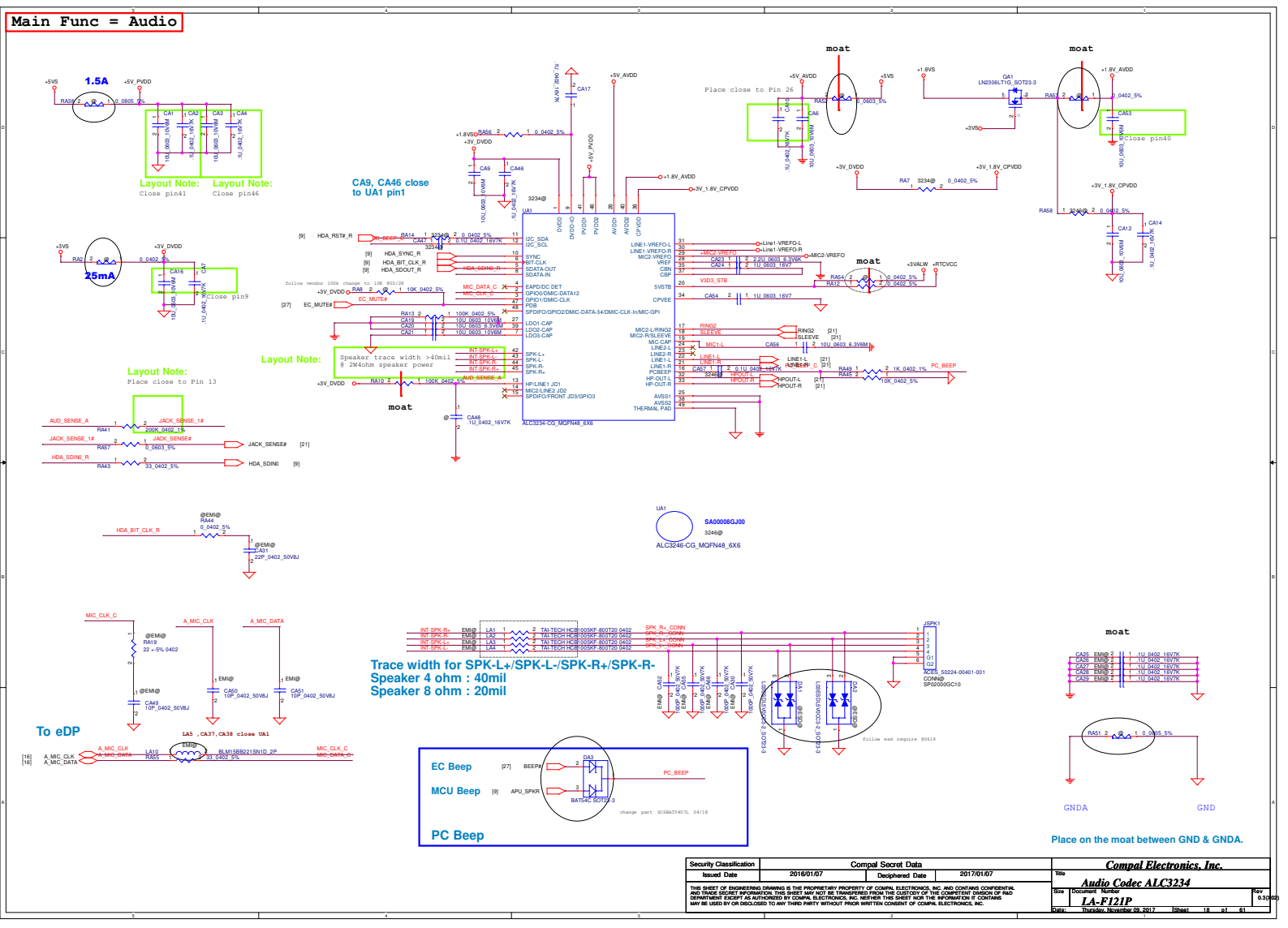
Compal Electronics, Inc.

Title: **HDMI**

Size | Document Number: **LA-F121P** | Rev 0.3(X02)

Date: Thursday, November 09, 2017 | Sheet 17 of 61

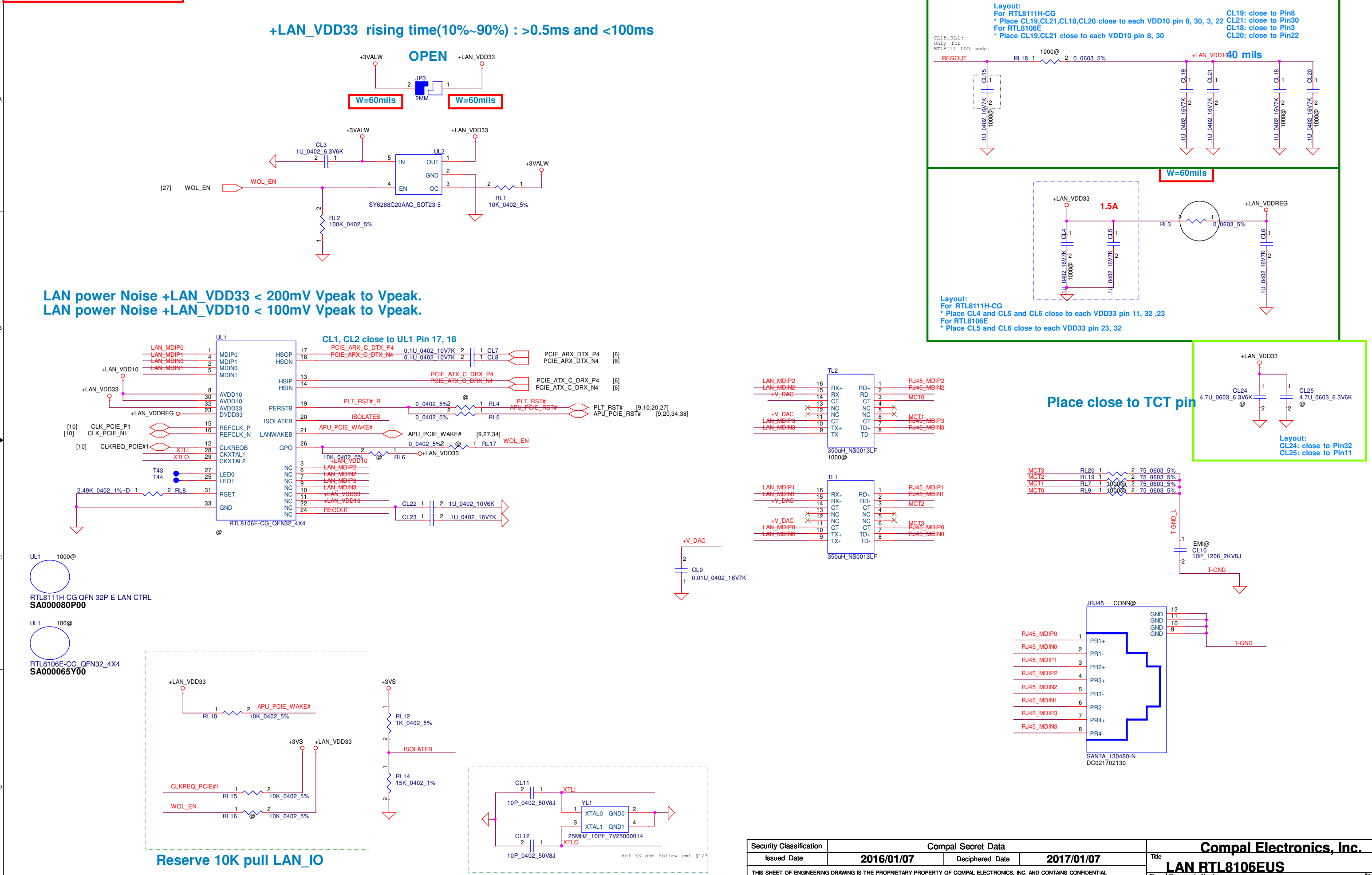
Main Func = Audio



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title: Audio Codec ALC3234			
Size	Document Number: LA-F121P		Rev: 0.3(0Q)
Date: Thursday, November 09, 2017	Sheet 18 of 61		

Main Func = LAN



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: **LAN RTL8106EUS**

Size: Custom | Document Number: **LA-F121P** | Rev: 0.3(X02)

Main Func = WLAN

CHANGE WLAN NET NAME @2/23

NGFF WL Con (A Key)

JWLAN1 CONN@

LCN_DAN05-67306-0100
SP070019F00

	77	MTG77	MTG76	76	
			GND	75	
	74	3.3VAUX	RESERVED	73	
	72	3.3VAUX	RESERVED	71	
	70	RESERVED	GND	69	
	68	RESERVED	RSRVD/PERN1	67	
	66	RESERVED	RSRVD/PERP1	65	
	64	RESERVED	GND	63	
	62	ALERT	RSRVD/PETN1	61	
	60	I2C_CLK	RSRVD/PETP1	59	
	58	I2C_DATA	GND	57	
WL_OFF#_R	56	W_DISABLE1#	PEWAKE0#	55	WLAN_WAKE# [27]
BT_ON#_R [10]	54	W_DISABLE2#	CLKEQ0#	53	CLKREQ_PCIE#2 [10]
PLT_RST#_RW	52	PERST0#	GND	51	
SUSCLK_WLAN [10]	50	SUSCLK	REFCLKN0	49	CLK_PCIE_N2 [10]
	48	COEX1	REFCLKP0	47	CLK_PCIE_P2 [10]
	46	COEX2	GND	45	
	44	COEX3	PERN0	43	PCIE_ARX_DTX_N5 [6]
	42	RESERVED	PERP0	41	PCIE_ARX_DTX_P5 [6]
	40	RESERVED	GND	39	
	38	RESERVED	PETN0	37	PCIE_ATX_C_DRX_N5 [6]
	36	UART_RTS	PETP0	35	PCIE_ATX_C_DRX_P5 [6]
	34	UART_CTS	GND	33	
	32	UART_TX	SDIO_RESET#	31	
	30	UART_RX	SDIO_WAKE#	29	
	28	UART_WAKE#	SDO_DAT3	27	
	26	GND	SDO_DAT2	25	
	24	LED2#	SDO_DAT1	23	
	22	PCM_OUT	SDO_DAT0	21	
	20	PCM_IN	SDIO_CMD	19	
	18	PCM_SYNC	SIDO_CLK	17	
	16	PCM_CLK			
	6	LED1#	GND	7	
	4	3.3VAUX	USB_D-	5	USB20_MINI1_N4 [35]
	2	3.3VAUX	USB_D+	3	USB20_MINI1_P4 [35]
			GND	1	

+3VS_WLAN_NGFF

EC_RX [27] RW7 1 2 0_0402_5% E51_RX1
EC_TX [27] RW6 1 2 0_0402_5% E51_TX1

100K_0402_5% 2 1 RW12

For EC to detect debug card insert.

MODS@ RW5 2 1 10_0402_5% S0A3_GPIO [9,26,27]

closed to pin 2, 4

+3VS_WLAN_NGFF

CW3 10U_0603_6.3V6M
CW4 0.1U_0402_10V7K-D
CW11 10P_0402_50V8J @RF@

+3VS_WLAN_NGFF

CW12 10U_0603_6.3V6M
CW13 0.1U_0402_10V7K-D
CW14 10P_0402_50V8J @RF@

+3VS_WLAN_NGFF

CW7 10P_0402_50V8J RF@
CW10 10P_0402_50V8J RF@
CW15 2.2U_0402_6.3V6M RF@
CW16 2.2U_0402_6.3V6M RF@

+3VS TO +3VS_WLAN_NGFF

+3VS — 1 RM1 2 0_1206_5% — +3VS_WLAN_NGFF

Prevent Backdriver from +3VS_WLAN_NGFF to +3VS

+3VS_WLAN_NGFF +3VS

RW8 10K_0402_5%~D

QW1 DII-DMN65D8LW-7~D

WL_OFF#_R — WL_OFF# [10]

+3VALW +3VS_WLAN_NGFF +3VALW

UW1 SY6288C20AAC_SOT23-5 (IN, OUT, GND, EN, OC)

[27] WLAN_EN

RW13 MODS@ 10K_0402_5%

RW14 100K_0402_5% MODS@

High Active

for modern standby

PLT_RST#_RW — 0_0402_5% RW10 — APU_PCIE_RST# — PLT_RST# [9,10,19,27] APU_PCIE_RST# [9,19,34,38]

0_0402_5% RW11

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

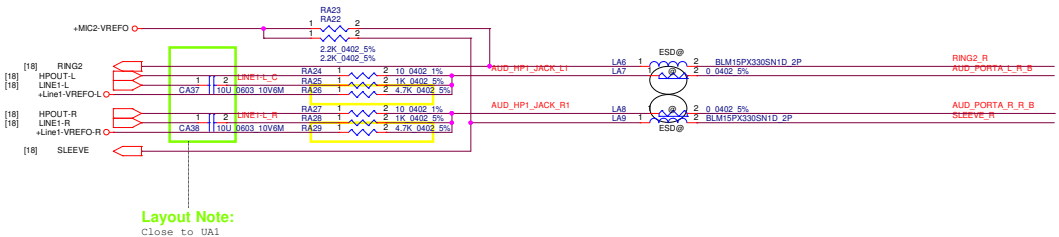
Compal Electronics, Inc.

Title: NGFF WLAN

Size: | Document Number: LA-F121P | Rev: 0.3(002)

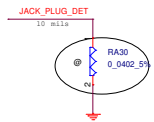
Date: Thursday, November 09, 2017 | Sheet 20 of 61

Main Func = Audio Jack

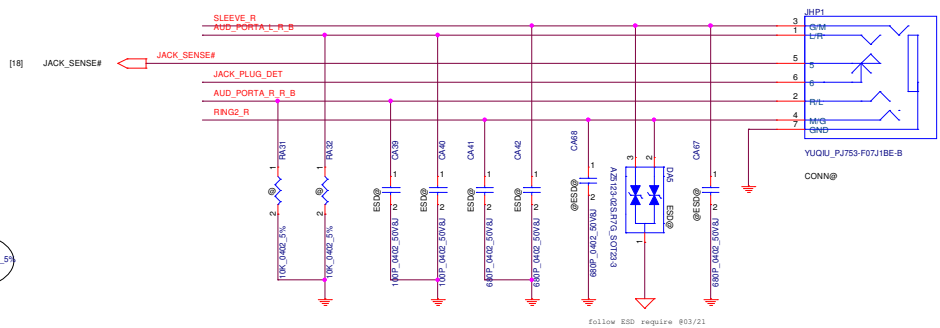


Layout Note:
Close to UA1

CLOSE TO JHP



Universal Jack
(Global Headset Jack + mic phone in + line in support)



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

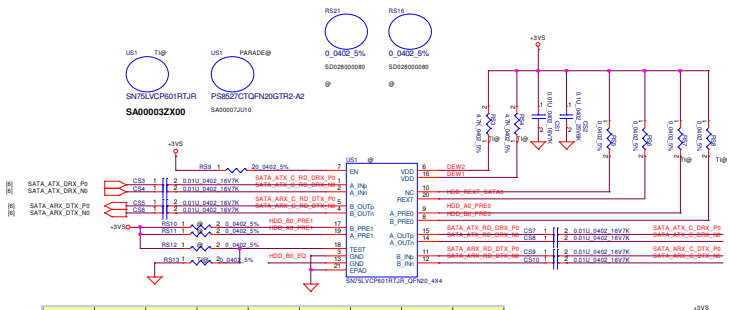
Compal Electronics, Inc.

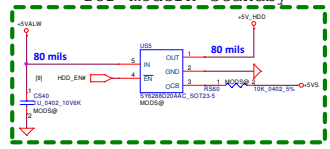
Title: **JACK**

Size | Document Number | Rev 0.3(X02)

Date: Thursday, November 09, 2017 | Sheet 21 of 61

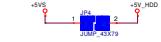
Main Func = HDD



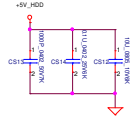


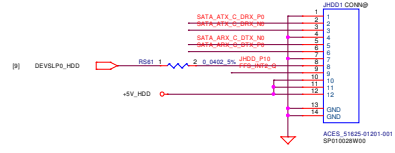
Vendor	RS18	RS22	RS23	RS27	RS28	RS33	RS34	RS37
TI	V	V	V	V	V	4.7k	4.7k	V
Parade	NC	NC	V	NC	NC	NC	NC	V

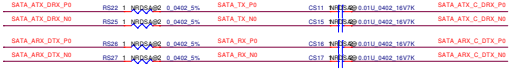
+5V_HDD Source
60 mils

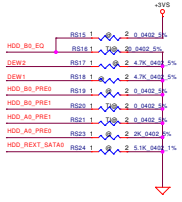


SHORT

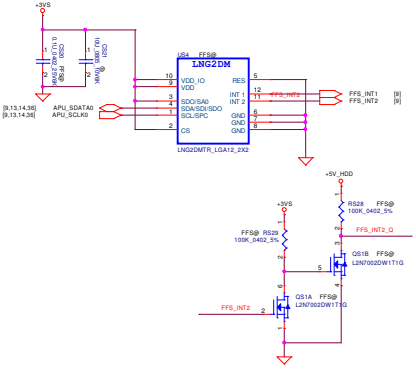






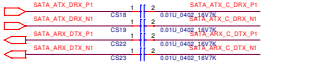


Main Func = FFS

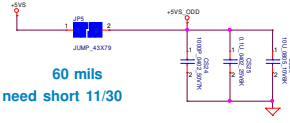


Main Func = ODD

APU TX
APU RX

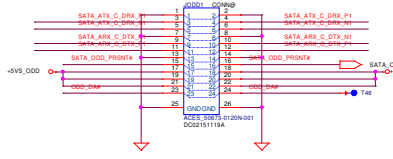


ODD Power Control



60 mils
need short 11/30

SATA ODD Connector (FFC Type)



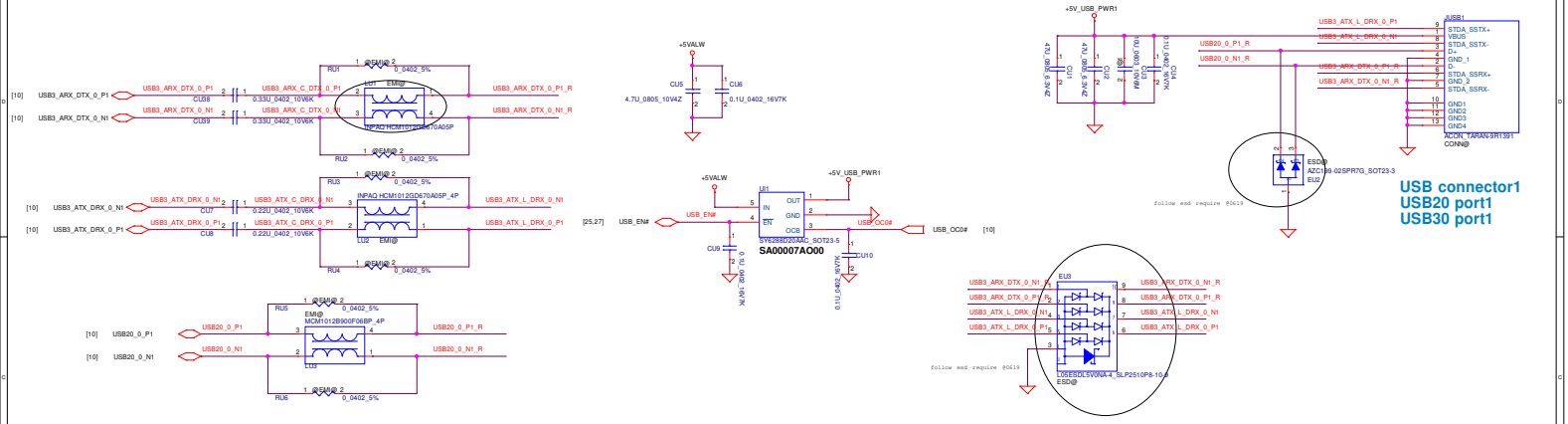
APU TX
APU RX

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title	HDD		
Size	Document Number	LA-F121P	Rev 0.3(0.0)
Date: Thursday, November 09, 2017	Sheet 22 of 61		

Main Func = USB3.0 Port1



Main Func = USB3.0 Port2

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

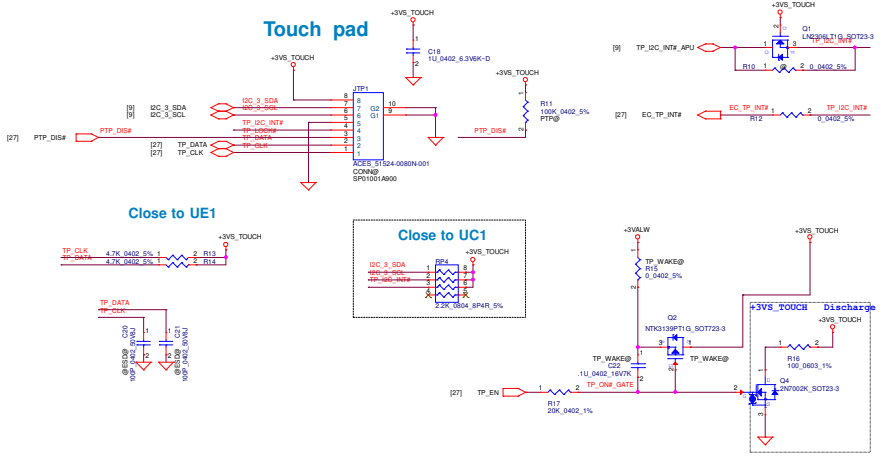
Compal Electronics, Inc.

Title: USB3.0

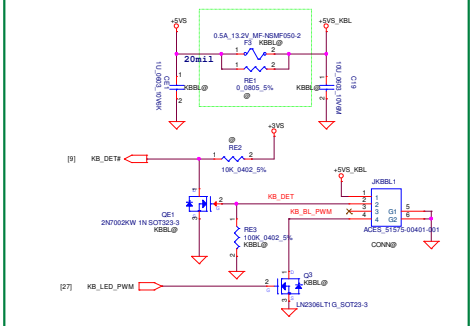
Size: | Document Number: LA-F121P | Rev: 0.3(0.0)

Date: Thursday, November 09, 2017 | Sheet 23 of 61

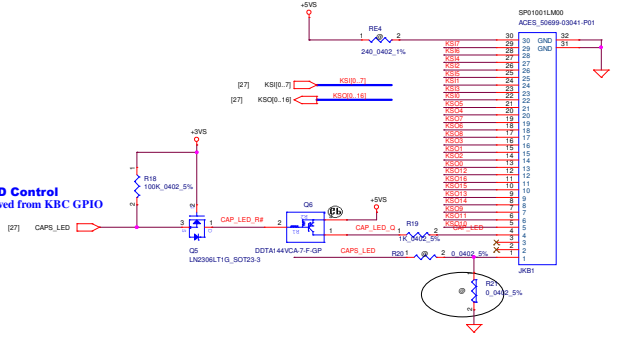
Main Func = Touch Pad



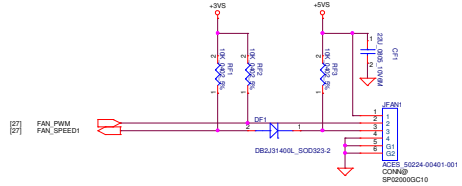
Main Func = KBBL



Main Func = KB



Main Func = FAN Control



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

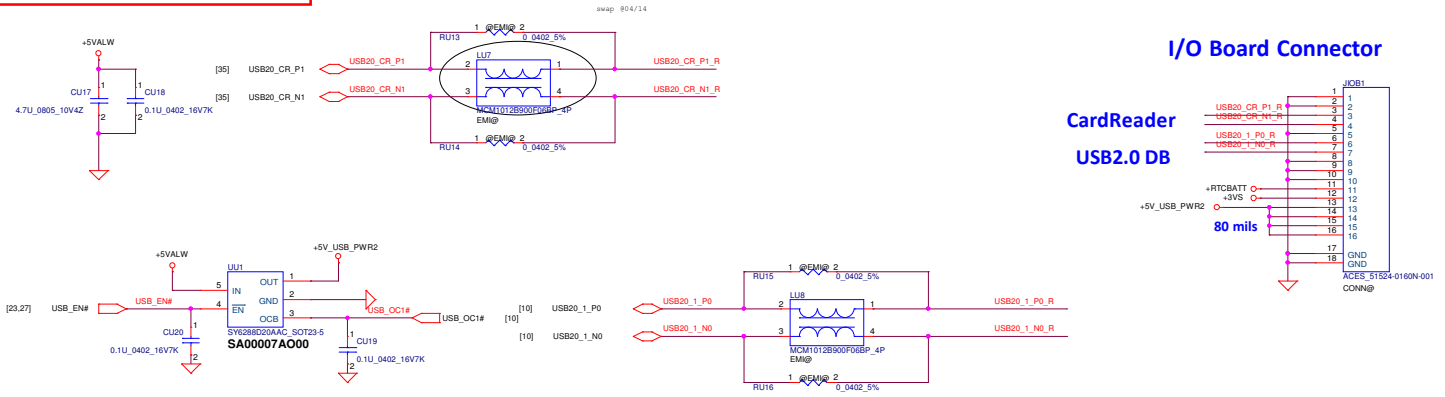
Compal Electronics, Inc.

Title: FAN / TP / PWR SW / KBBL

Size	Document Number	Rev
	LA-F121P	0.3(1002)

Date: Thursday, November 09, 2017 | Sheet 24 of 61

Main Func = IO Connector

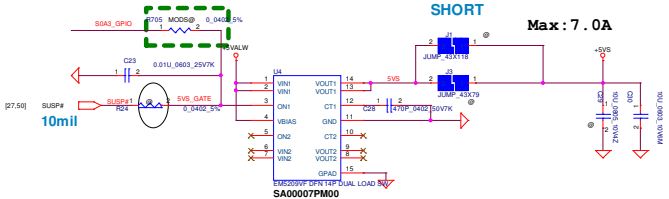


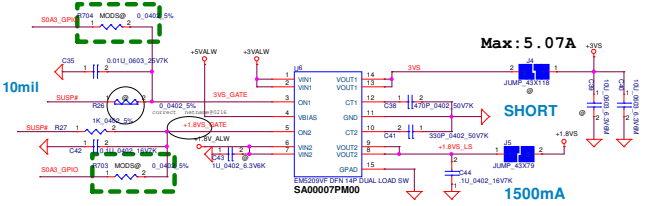
Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Title	IO-DB		
Size: Custom	Document Number: LA-F121P		Rev: 0.3(X02)
Date: Thursday, November 09, 2017	Sheet 25 of 61		

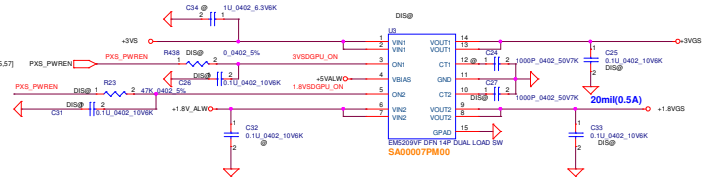
Main Func = DC Interface

+5VS and +3VS switch

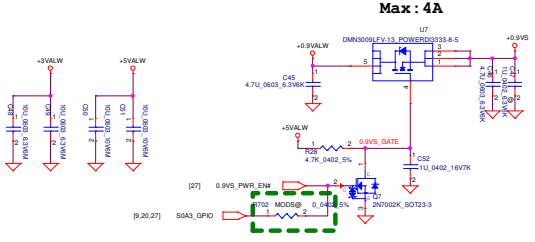




+3VS to +3VGS
+1.8V_ALW to +1.8VGS



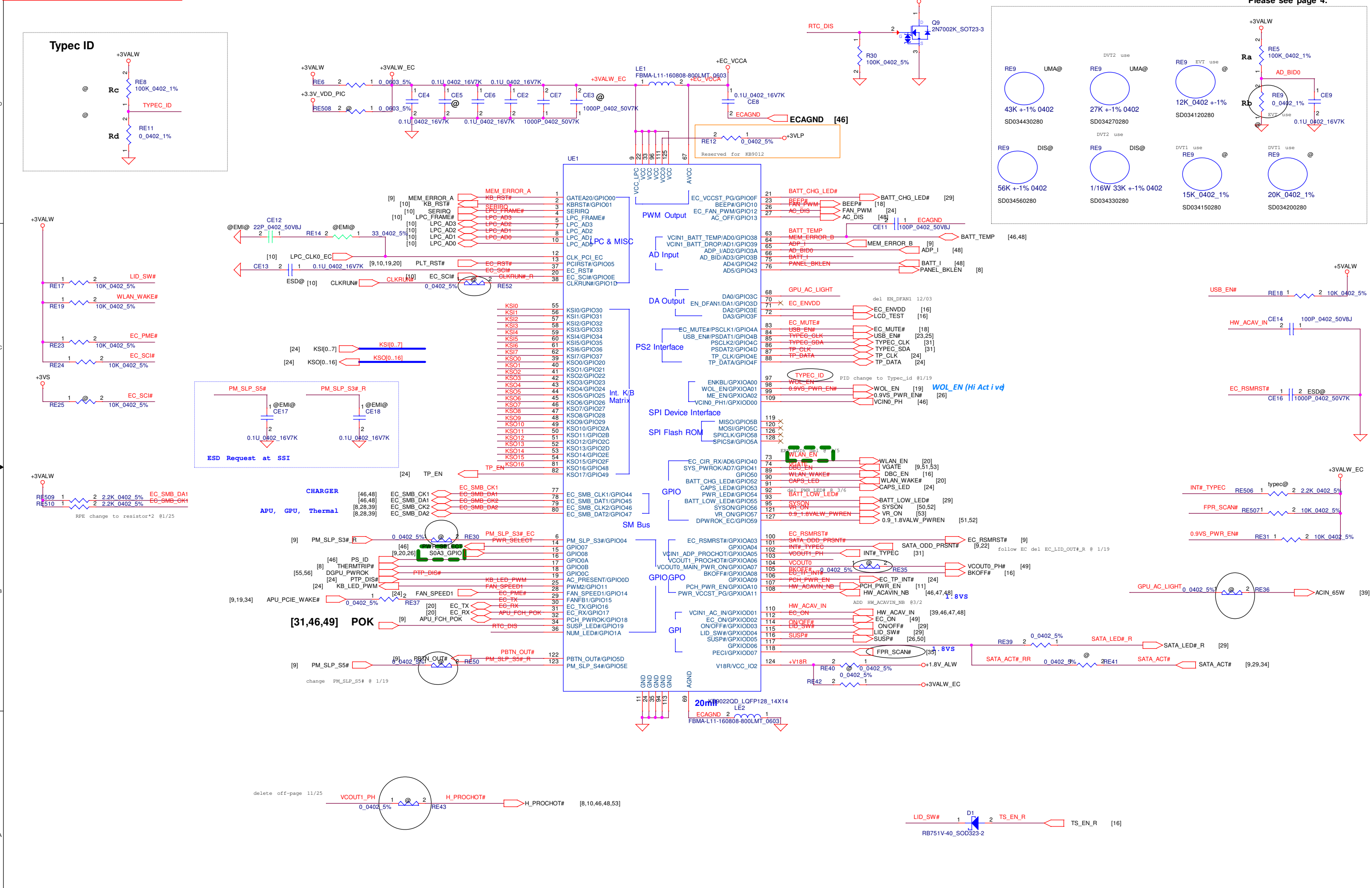
Max:4A



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title: DC/DC Interface			
Size	Document Number: LA-F121P		Rev: 0.3(0.02)
Date: Thursday, November 09, 2017	Sheet 26 of 61		

Main Func = KBC



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

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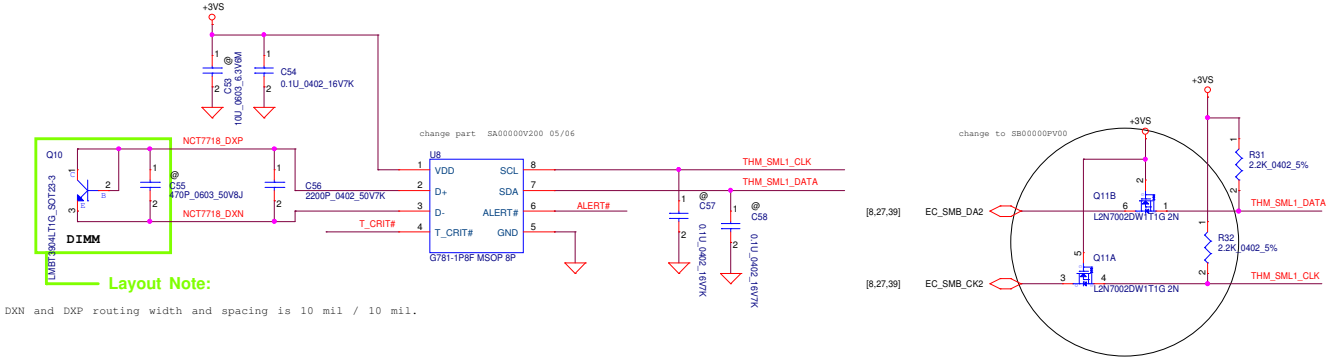
Compal Electronics, Inc.

Title: EC ENE-KB9012A4/KB9022QC

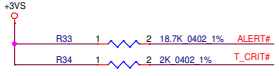
Size | Document Number: LA-F121P | Rev: 0.3(X02)

Main Func = Thermal Sensor



Layout Note:

DXN and DXP routing width and spacing is 10 mil / 10 mil.



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

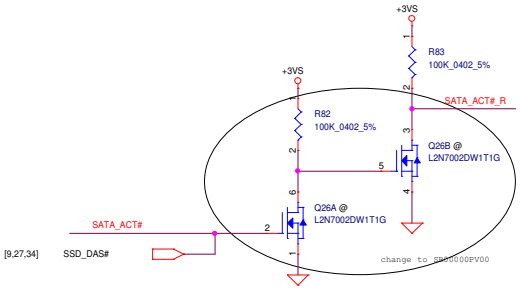
Compal Electronics, Inc.

Title: **Thermal Sensor**

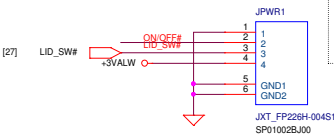
Size	Document Number	Rev
	LA-F121P	0.3(X02)

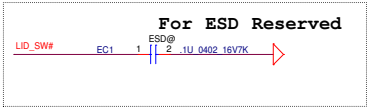
Date: Thursday, November 09, 2017 Sheet 28 of 61

Main Func = POWER BTN



Power button



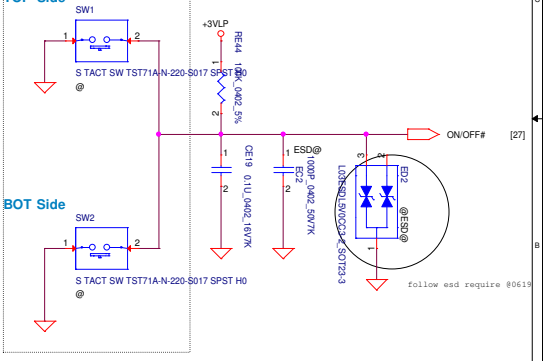


Pop only before MP

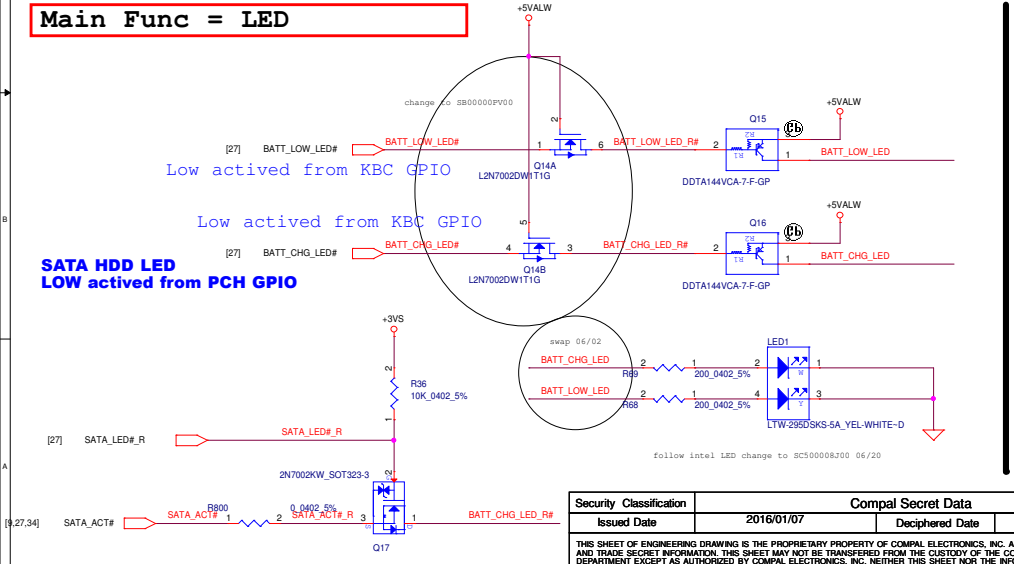
ON/OFF switch

TOP Side

BOT Side



Main Func = LED



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: LED/PWR-DB

Size: | Document Number: LA-F121P | Rev: 0.3(002)

Date: Thursday, November 09, 2017 | Sheet 29 of 61

Main Func = Screw Hole

ZZZ

Part Number	Description
DAZ21O00100	PCB CAL51 LA-F121P LS-F114P/F121P/F122P

PCB_R1@

ZZZ2

Part Number	Description
DAZ21O00102	PCB CAL51 LA-F121P LS-F114P/F121P/F122P TRIPOD A31 !

PCB_R3T@

ZZZ1

Part Number	Description
DAZ21O00101	PCB CAL51 LA-F121P LS-F114P/F121P/F122P GOLD A31 !

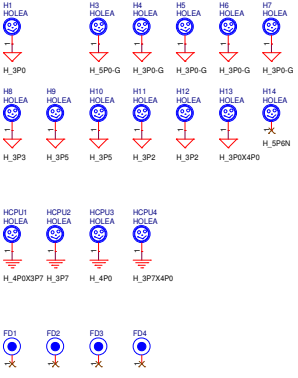
PCB_R3G@

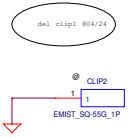
ZZZ3

Part Number	Description
DAZ21O00104	PCB CAL51 LA-F121P LS-F114P/F121P/F122P T-MAC A31 !

PCB_R3H@

Screw hole/FD





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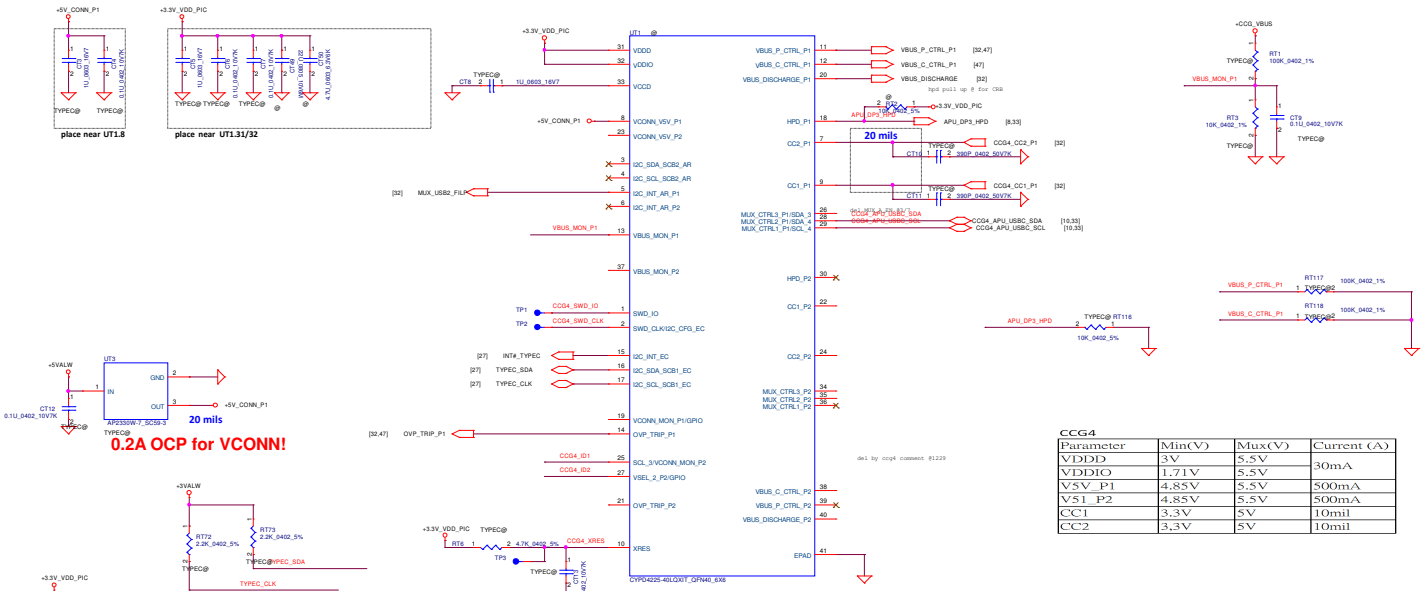
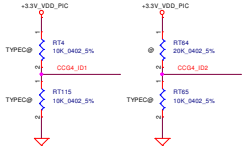
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.	
Title	Screw Hole
Size	Document Number: LA-F121P
Rev	0.3(X02)
Date: Thursday, November 09, 2017	Sheet 30 of 61



CCG4			
Parameter	Min(V)	Max(V)	Current (A)
VDDD	3V	5.5V	30mA
VDDIO	1.71V	5.5V	
V5V_P1	4.85V	5.5V	500mA
V51_P2	4.85V	5.5V	500mA
CC1	3.3V	5V	10mil
CC2	3.3V	5V	10mil

Loki AMD
CCG4 ID1: 4* VDD/8
CCG4 ID2: 0



Voltages for various platform on "CCG4_ID_1" pin and "CCG4_ID_2" pin

#	Platform	Voltage on CCG4_ID_1	Voltage on CCG4_ID_2
1	Single Port - Intel - DDM support - Armani 13" & 14"	L0	L7
2	Single Port - Intel - DDM support - Kyloren	L0	L6
3	Single Port - Intel - DDM support - Miyake	L0	L5
4	Single Port - Intel - DDM support - Loki 13"	L0	L4
5	Single Port - Intel - DDM support - Loki 15" & 17" (Motherboard is same)	L0	L3
6	Single Port - Intel - DDM support - StarLord KBL - R	L0	L2
7	Single Port - AMD - DDM not supported - Loki 15" & 17" (Motherboard is same)	L4	L0

Voltage level	Voltage value
L0	0V
L1	3.3V/8
L2	2 * 3.3V/8
L3	3 * 3.3V/8
L4	4 * 3.3V/8
L5	5 * 3.3V/8
L6	6 * 3.3V/8
L7	7 * 3.3V/8

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Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.			
Title: Cypress PD Control			
Size: Custom	Document Number: LA-F121P		Rev: 0.3(0.0)
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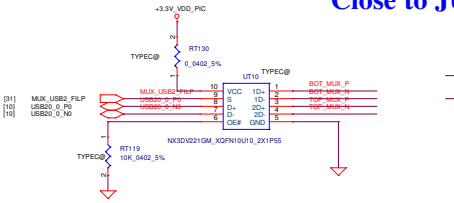
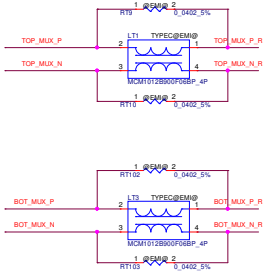
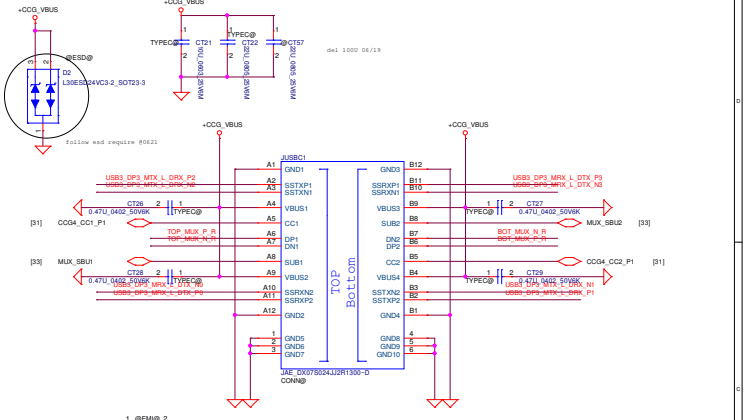
Main Func = USB2 Mux

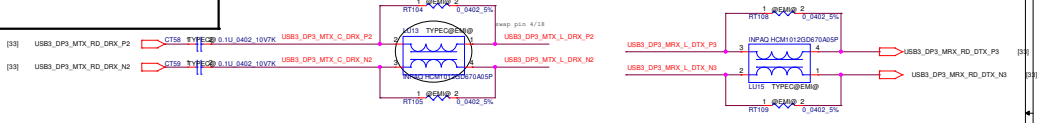
Close to JUSBC1 <500mil



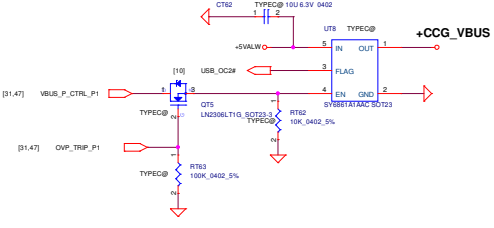
S	OE#	OUT PUT
Low	Low	1D+/1D-
High	Low	2D+/2D-

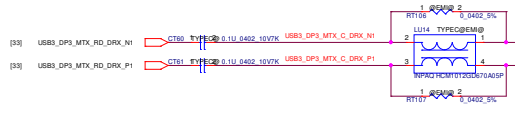


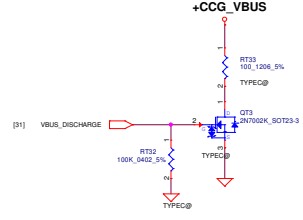


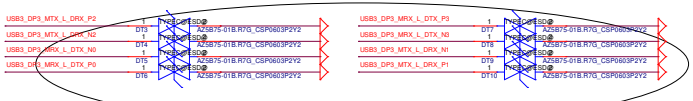


5V@3A









Type-C 5V Provide Path Control

Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: TYPE-C CONN

Size: C | Document Number: LA-F121P | Rev: 0.3(X02)

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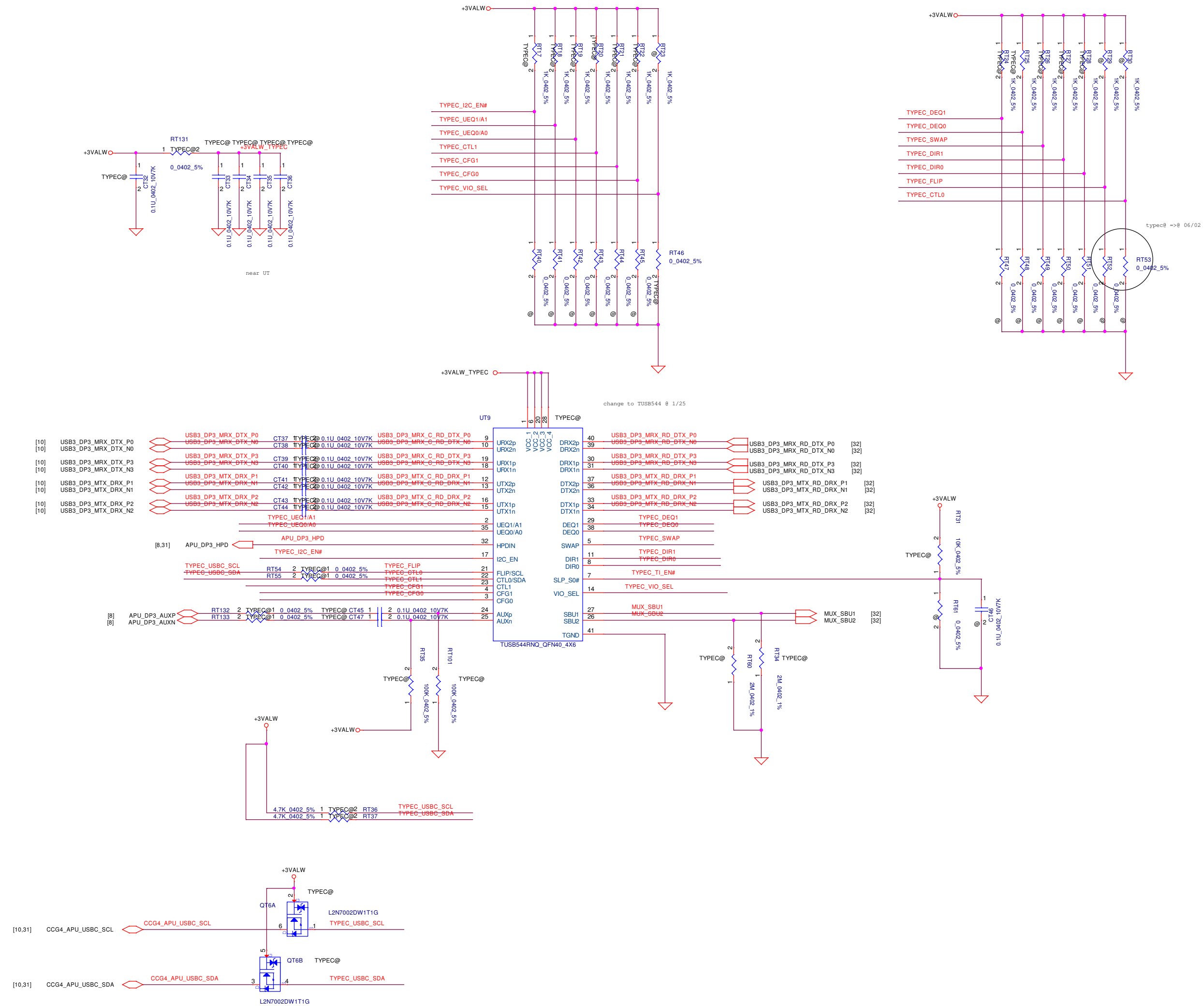
Main Func = TYPEC Re-driver



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Issued Date	2014/05/19	Deciphered Date	2015/12/31

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Compal Electronics, Inc.

Title: **TYPEC REDRIVER**

Size: Custom | Document Number: **LA-F121P** | Rev: 0.3(X02)

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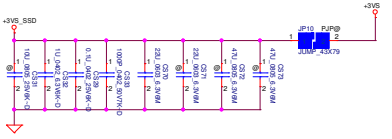
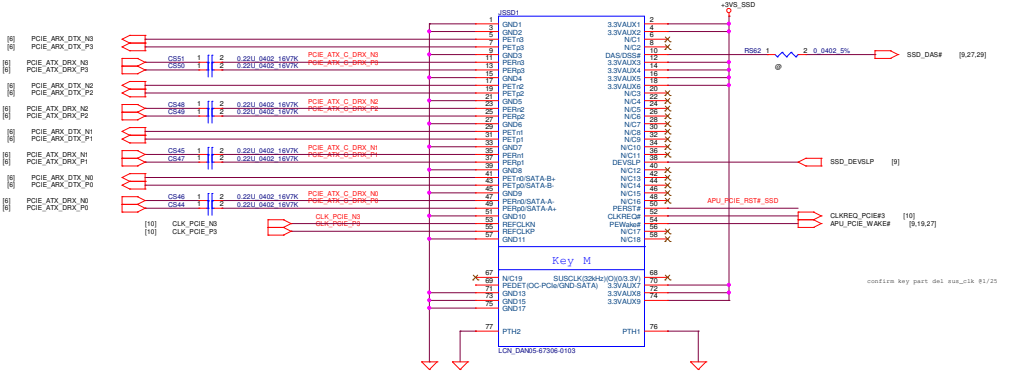
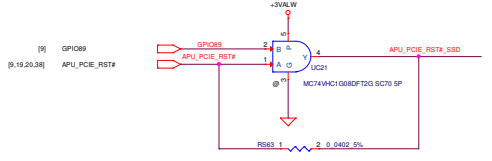
Main Func = SSD



NGFF Key M





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Issued Date	2014/05/19	Deciphered Date	2015/12/31

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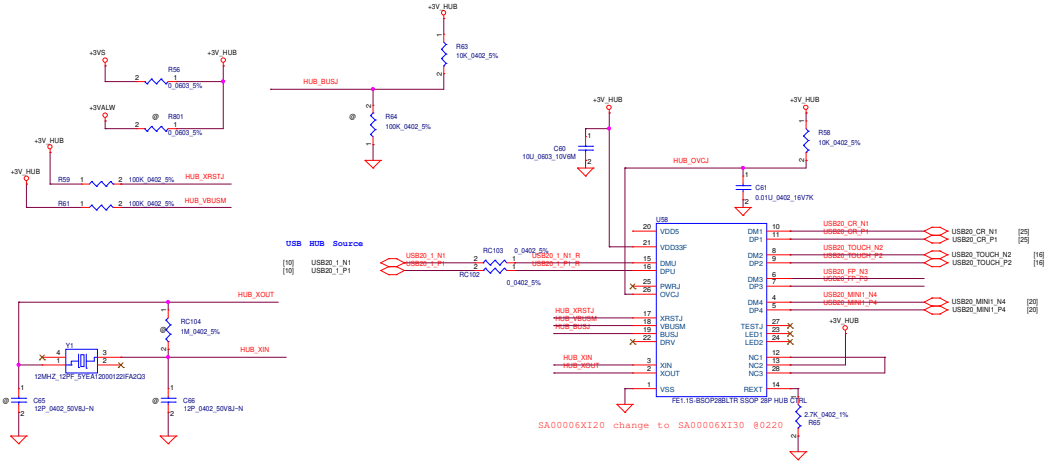
Compal Electronics, Inc.

Title: SSD

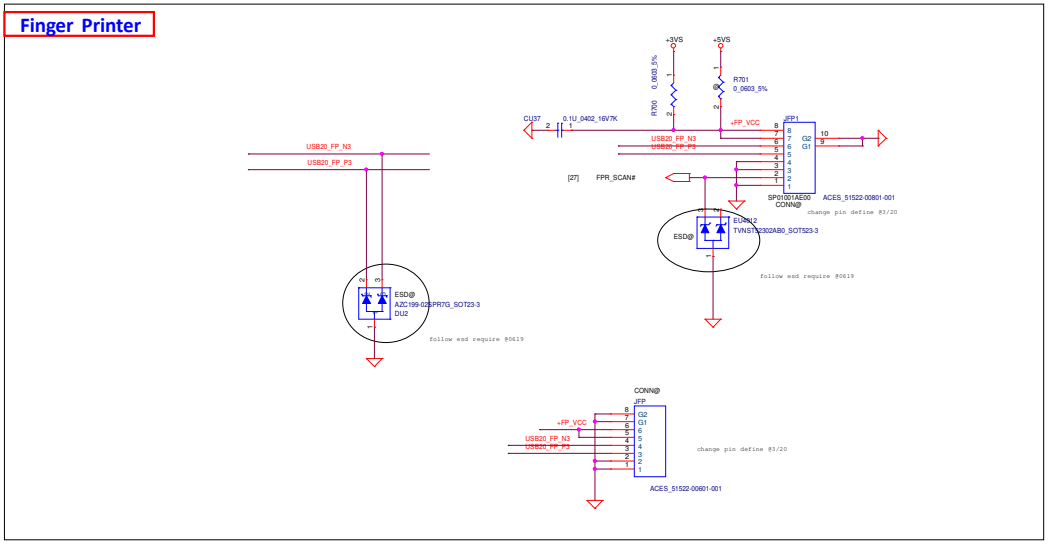
Size: C | Document Number: LA-F121P | Rev: 0.3(HG)

Date: Thursday, November 09, 2017 | Sheet 34 of 61

Main Func = USB HUB



Finger Printer



Security Classification	Compal Secret Data		
Issued Date	2014/05/19	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: USB HUB

Size: Custom | Document Number: LA-F121P | Rev: 0.3(X02)

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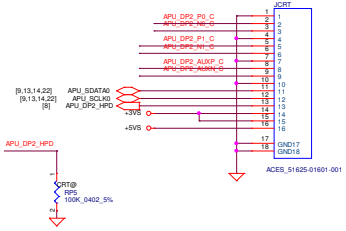
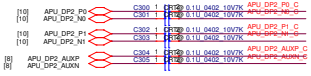
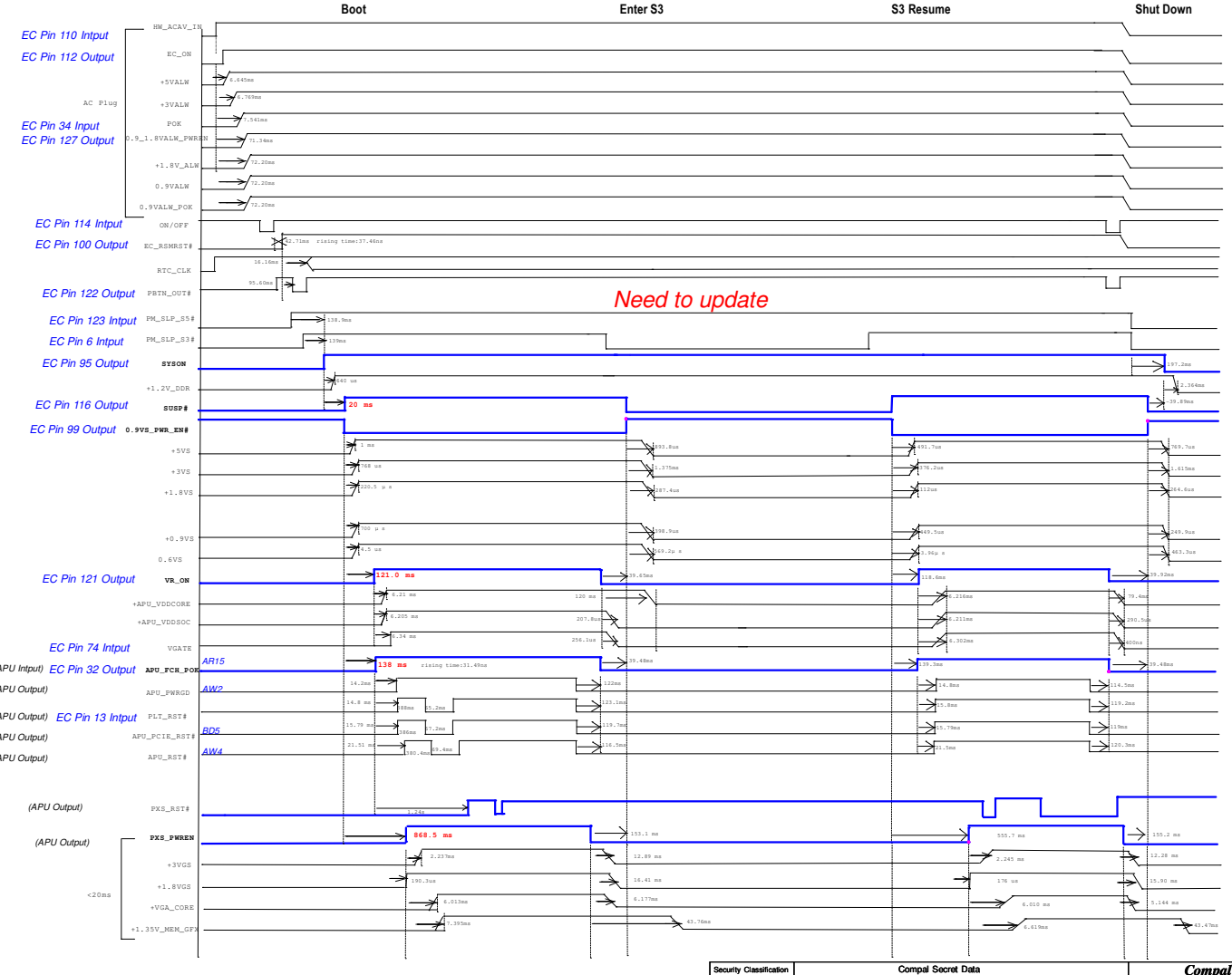
CRT





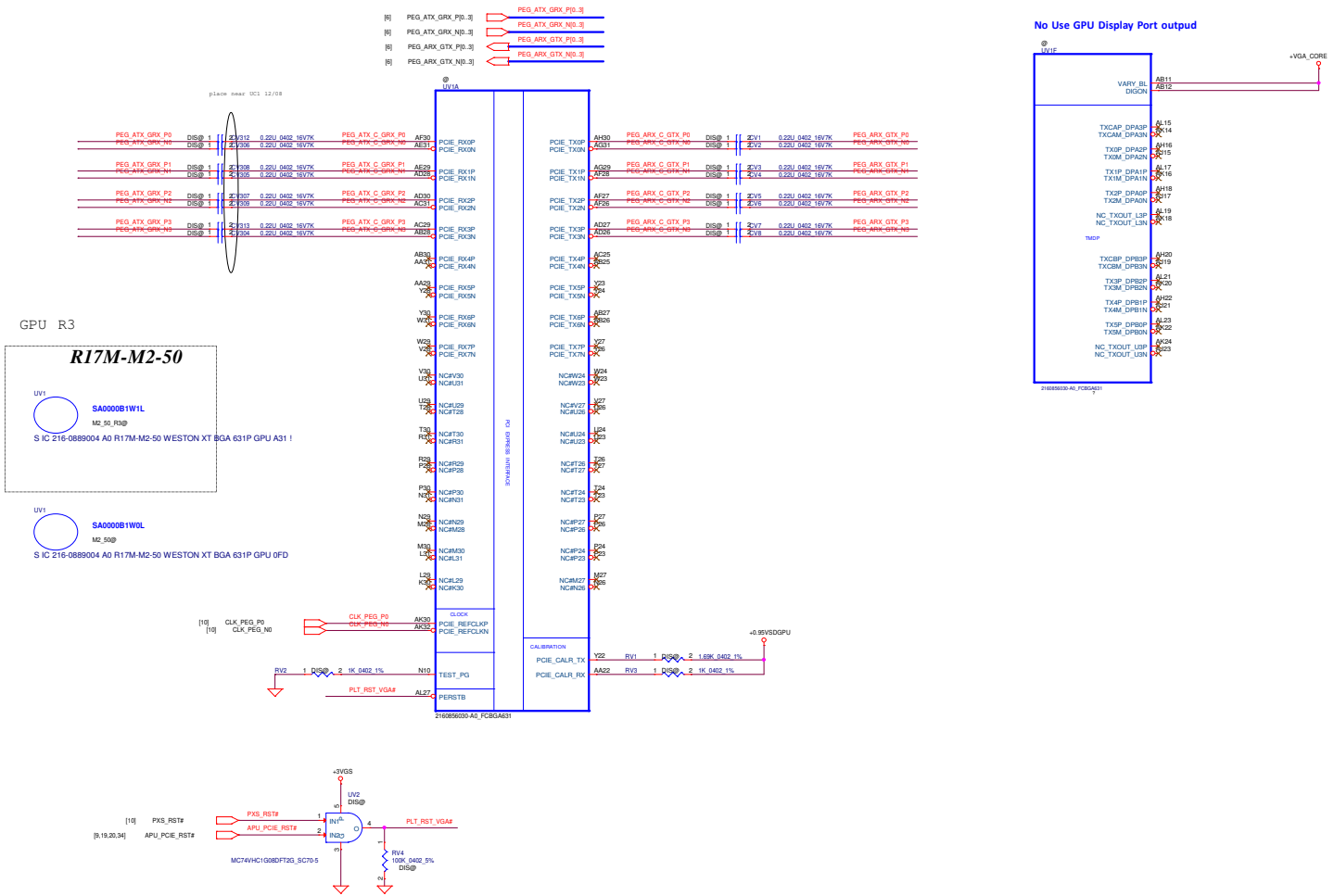
Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title: Reserve			
Size: Custom	Document Number: LA-F121P		Rev: 0.3(00)
Date:		Sheet 36 of 61	



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title	S5_MUX_CTRL		
Size	Document Number		Rev
	LA-F121P		0.3(302)
Date: Thursday, November 09, 2017	Sheet 37 of 81		



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

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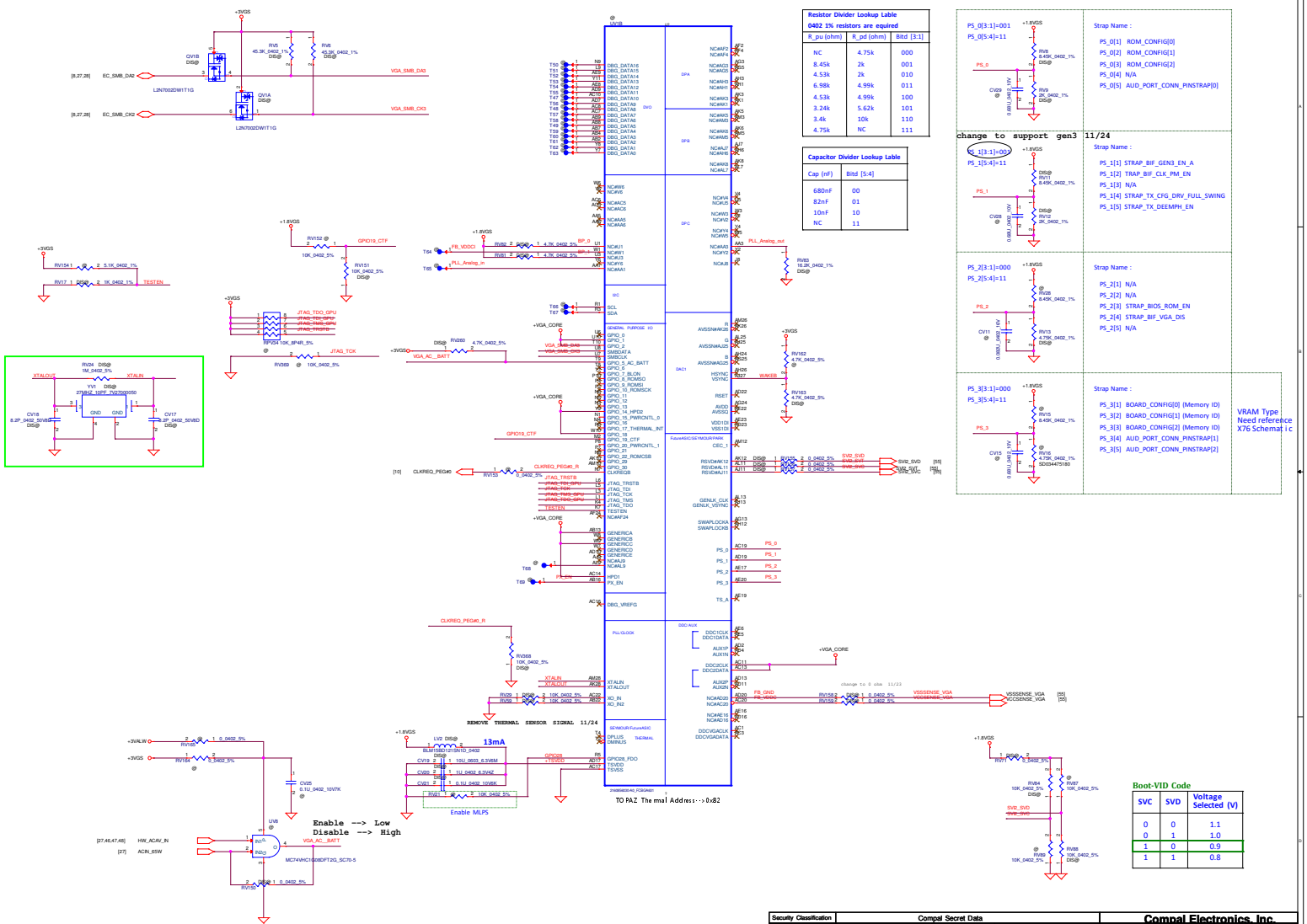
Compal Electronics, Inc.

Title: M30/M70_PCIE/DP

Size: Custom | Document Number: LA-F121P | Rev: 0.3(X02)

Date: Thursday, November 09, 2017 | Sheet 38 of 61


Resistor Divider Lookup Lable
0402 1% resistors are equired
R_pu (ohm) | R_pd (ohm) | Bitd [3:1]
NC | 4.75k | 000
8.45k | 2k | 001
4.53k | 2k | 010
6.98k | 4.99k | 011
4.53k | 4.99k | 100
3.24k | 5.62k | 101
3.4k | 10k | 110
4.75k | NC | 111
Capacitor Divider Lookup Lable
Cap (nF) | Bitd [5:4]
680nF | 00
82nF | 01
10nF | 10
NC | 11
change to support gen3 11/24
Strap Name :
PS_0[1] ROM_CONFIG[0]
PS_0[2] ROM_CONFIG[1]
PS_0[3] ROM_CONFIG[2]
PS_0[4] N/A
PS_0[5] AUD_PORT_CONN_PINSTRAP[0]
PS_1[1] STRAP_BIF_GEN3_EN_A
PS_1[2] TRAP_BIF_CLK_PM_EN
PS_1[3] N/A
PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
PS_1[5] STRAP_TX_DEEMPH_EN
PS_2[1] N/A
PS_2[2] N/A
PS_2[3] STRAP_BIOS_ROM_EN
PS_2[4] STRAP_BIF_VGA_DIS
PS_2[5] N/A
PS_3[1] BOARD_CONFIG[0] (Memory ID)
PS_3[2] BOARD_CONFIG[1] (Memory ID)
PS_3[3] BOARD_CONFIG[2] (Memory ID)
PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
PS_3[5] AUD_PORT_CONN_PINSTRAP[2]
VRAM Type
Need reference
X76 Schemat i c
REMOVE THERMAL SENSOR SIGNAL 11/24
13mA
Enable MLPS
TO PAZ Thermal Address---> 0x82
Enable --> Low
Disable --> High
Boot-VID Code
SVC | SVD | Voltage Selected (V)
0 | 0 | 1.1
0 | 1 | 1.0
1 | 0 | 0.9
1 | 1 | 0.8
Security Classification: Compal Secret Data
Issued Date: 2016/01/07 | Deciphered Date: 2017/01/07
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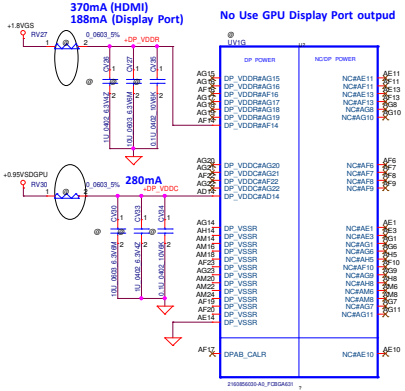
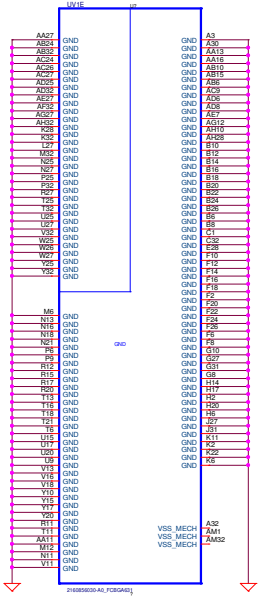
Compal Electronics, Inc.
Title: M30/M70_MSIC
Size: Custom | Document Number: LA-F121P | Rev: 0.3(X00)
Date: Thursday, November 09, 2017 | Sheet 39 of 61





Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.			
Title	M30/M70_Power/GND		
Size	Document Number		Rev
Custom	LA-F121P		0.3(X02)
Date:	Thursday, November 09, 2017	Sheet	40 of 61

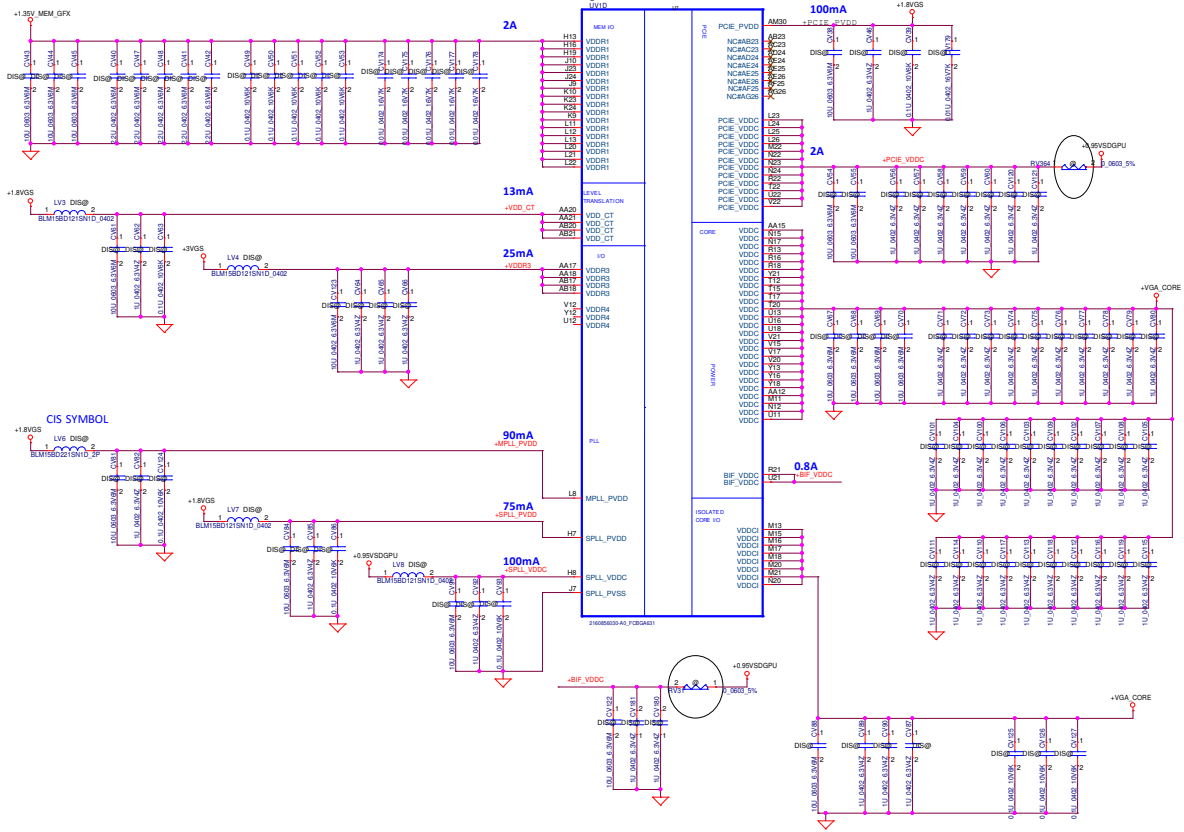
+VGA_CORE	10uF	1uF	0.1uF
VDDC VDDC and VDDCI TDC 28A	4	30	0
VDDCI	1	3	3

+0.95VSDGPU	10uF	1uF	0.1uF
PCIE_VDDC 2A	2	7	0
BIF_VDDC 0.8A	1	2	0
SPLL_VDDC 100mA	1	1	1

+1.35V_MEM_GFX	10uF	2.2uF	0.1uF	0.01uF
VDDR1 2A	3	5	5	5

+1.8VGS	10uF	1uF	0.1uF	0.01uF
PCIE_PVDD 100mA	1	1	1	1
MPLL_PVDD 90mA	1	1	1	0
SPLL_PVDD 75mA	1	1	1	0
VDD_CT 13mA	1	1	1	0
+DP_VDDR 40mA	1(@)	1(@)	1(@)	0
+DP_VDDC	1(@)	1(@)	1(@)	0

+3VGS	10uF	1uF	0.1uF
VDDR3 25mA	1	3	0



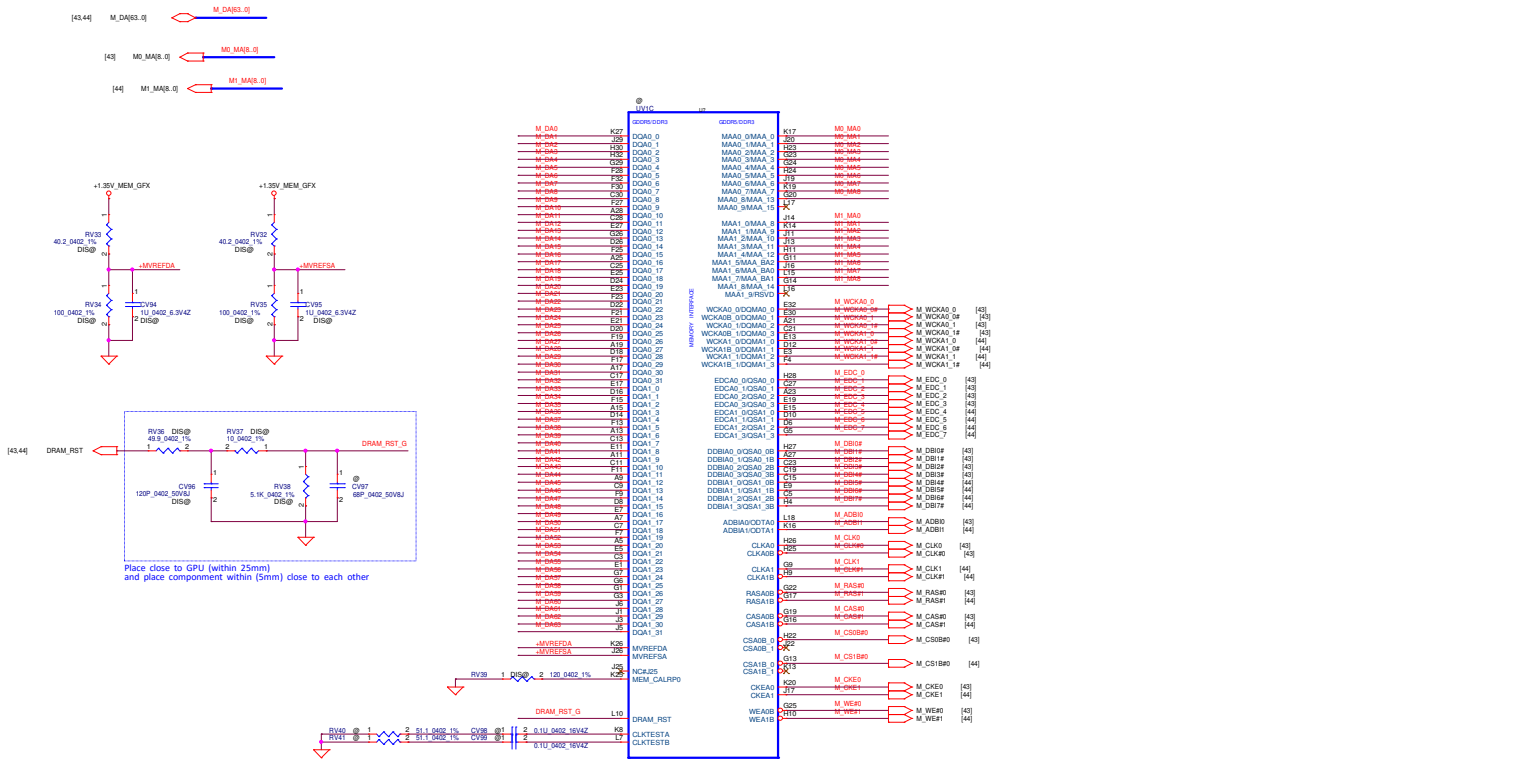
Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: M30/M70_Power

Size: Custom | Document Number: LA-F121P | Rev: 0.3(X00)

Date: Thursday, November 09, 2017 | Sheet 41 of 61



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

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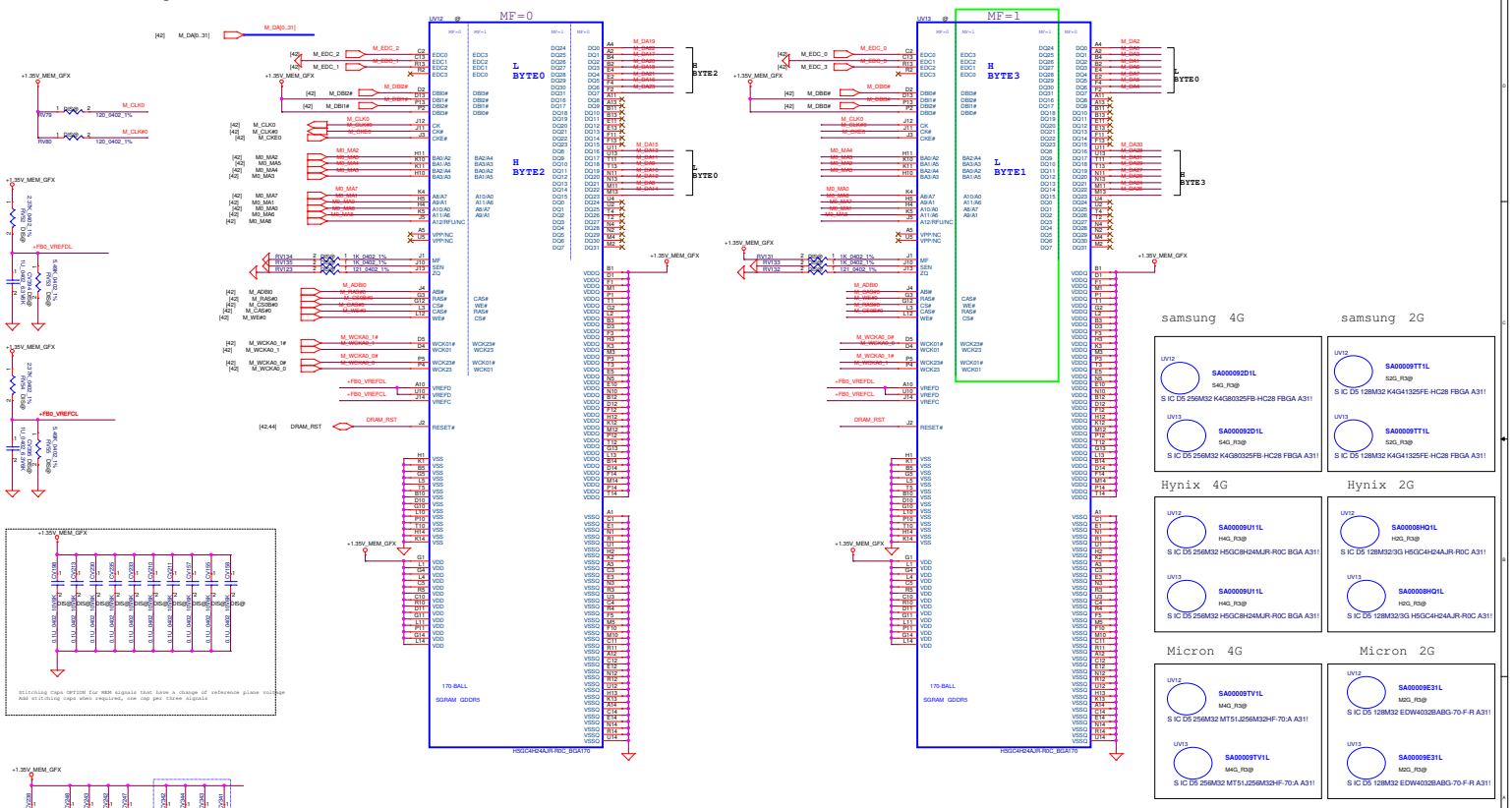
Compal Electronics, Inc.

Title: M30/M70_MEM

Size: Custom | Document Number: LA-F121P | Rev: 0.3(X02)

Date: Thursday, November 09, 2017 | Sheet 42 of 61

clamshell configuration



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

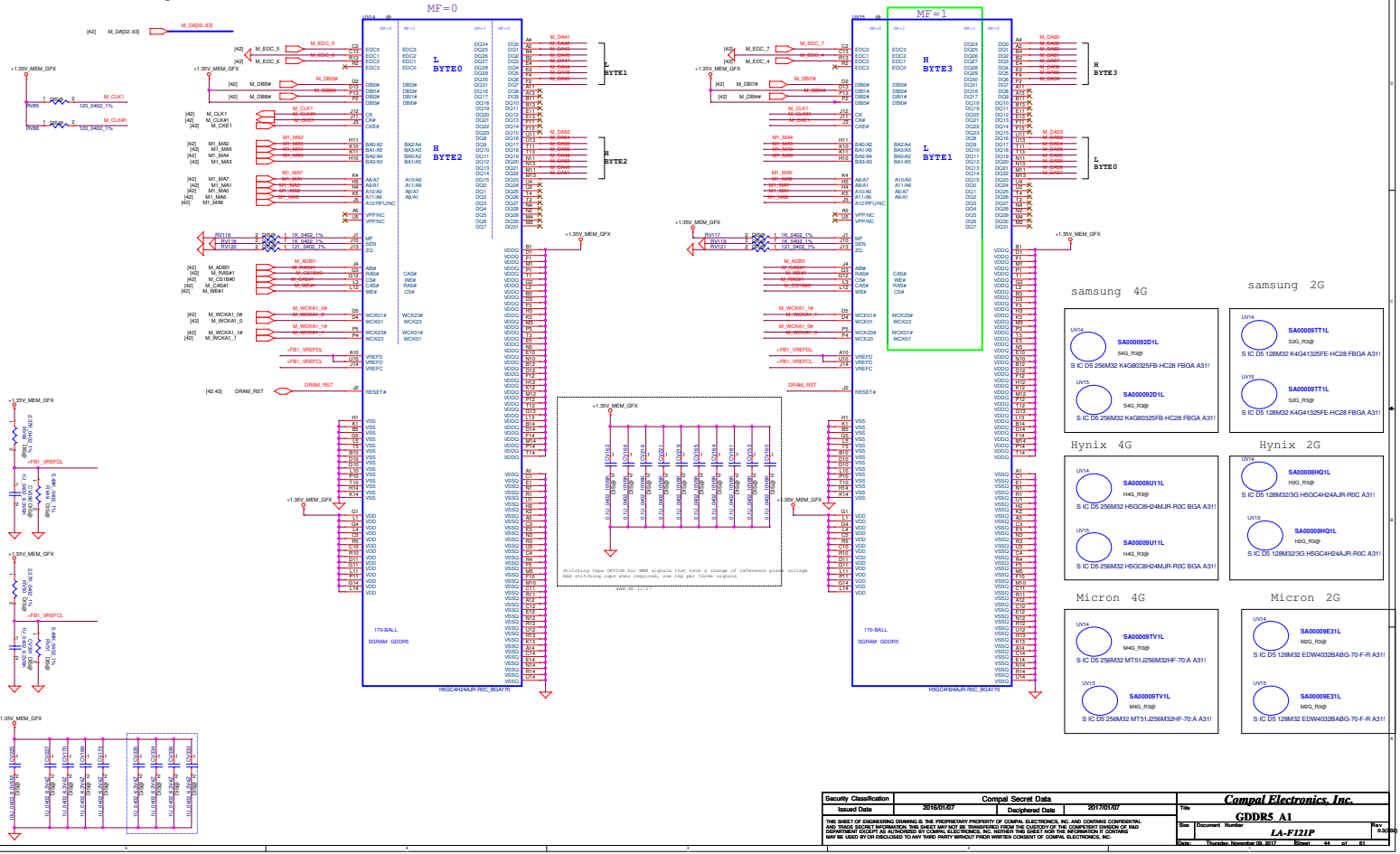
Compal Electronics, Inc.

Title: GDDR5 A0

Size: — Document Number: LA-F121P — Rev: 0.3(X00)

Date: Thursday, November 09, 2017 — Sheet 43 of 81

clamshell configuration



Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

Compal Electronics, Inc.

Title: **GDDR5 A1**

Size: — Document Number: **LA-F121P** — Rev: 0.3(SS)

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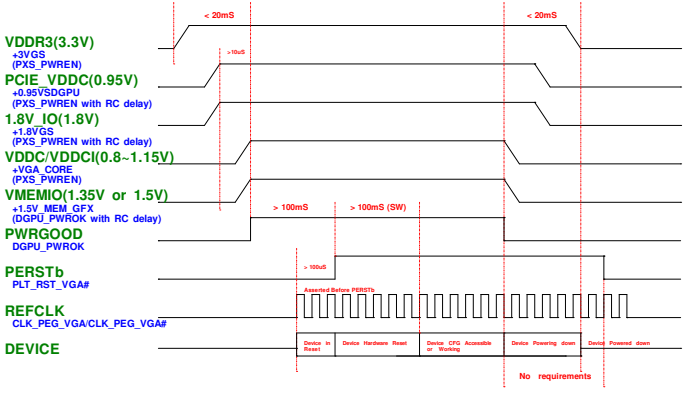
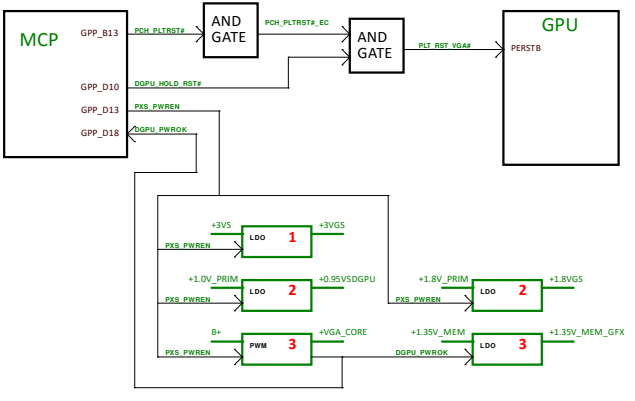
Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µ s
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress? idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/µ s).
5. VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.





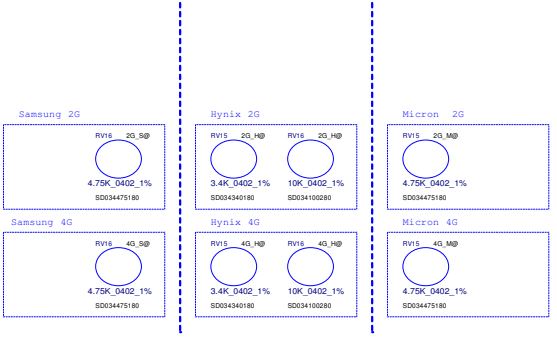


Table 3–21 Resistor Divider Lookup T.

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

For AMD R17M-M2-50 VRAM Only **2GB**

Memory ID	R3 P/N	Vendor	Configuratio n	Size
000	SA00009TT1L	SAMSUNG	S IC D5 128M32 K4G41325FE-HC28 FBGA A31!	2GB
110	SA00008HQ1L	Hynix	S IC D5 128M32/3G H5GC4H24AJR-R0C A31!	2GB
111	SA00009E31L	Micron	S IC D5 128M32 EDW4032BABG-70-F-R A31!	2GB

4GB

Memory ID	R3 P/N	Vendor	Configuratio	Size
000	SA000092D1L	SAMSUNG	S IC D5 256M32 K4G80325FB-HC28 FBGA A31!	4GB
110	SA00009U11L	Hynix	S IC D5 256M32 H5GC8H24MJR-R0C BGA A31!	4GB
111	SA00009TV1L	Micron	S IC D5 256M32 MT51J256M32HF-70:A A31!	4GB

Security Classification	Compal Secret Data		
Issued Date	2016/01/07	Deciphered Date	2017/01/07

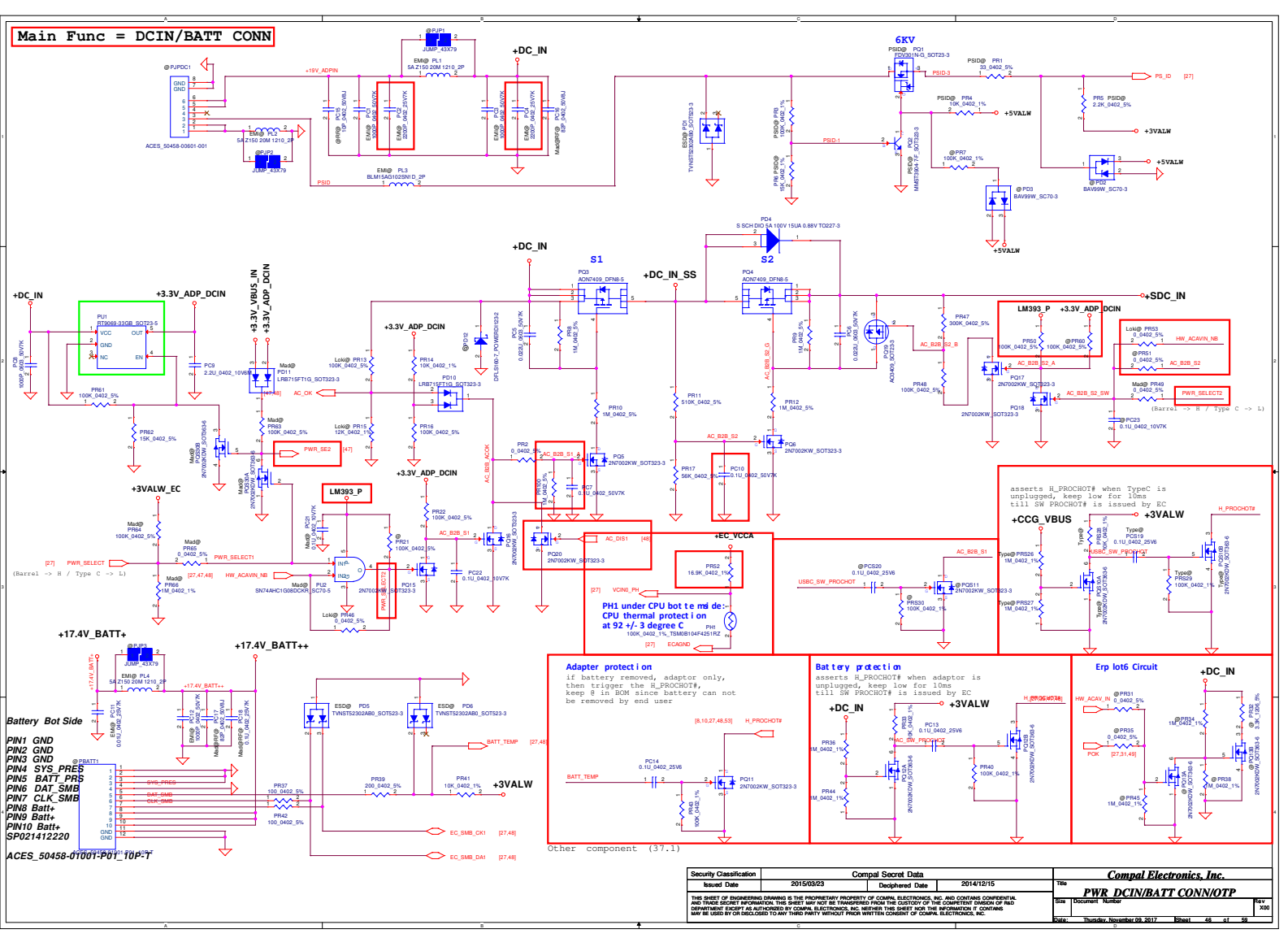
Compal Electronics, Inc.

Title: M30/M70_NOTE

Size: | Document Number: LA-F121P | Rev: 0.3

Date: Thursday, November 09, 2017 | Sheet 45 of 61

Main Func = DCIN/BATT CONN



Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

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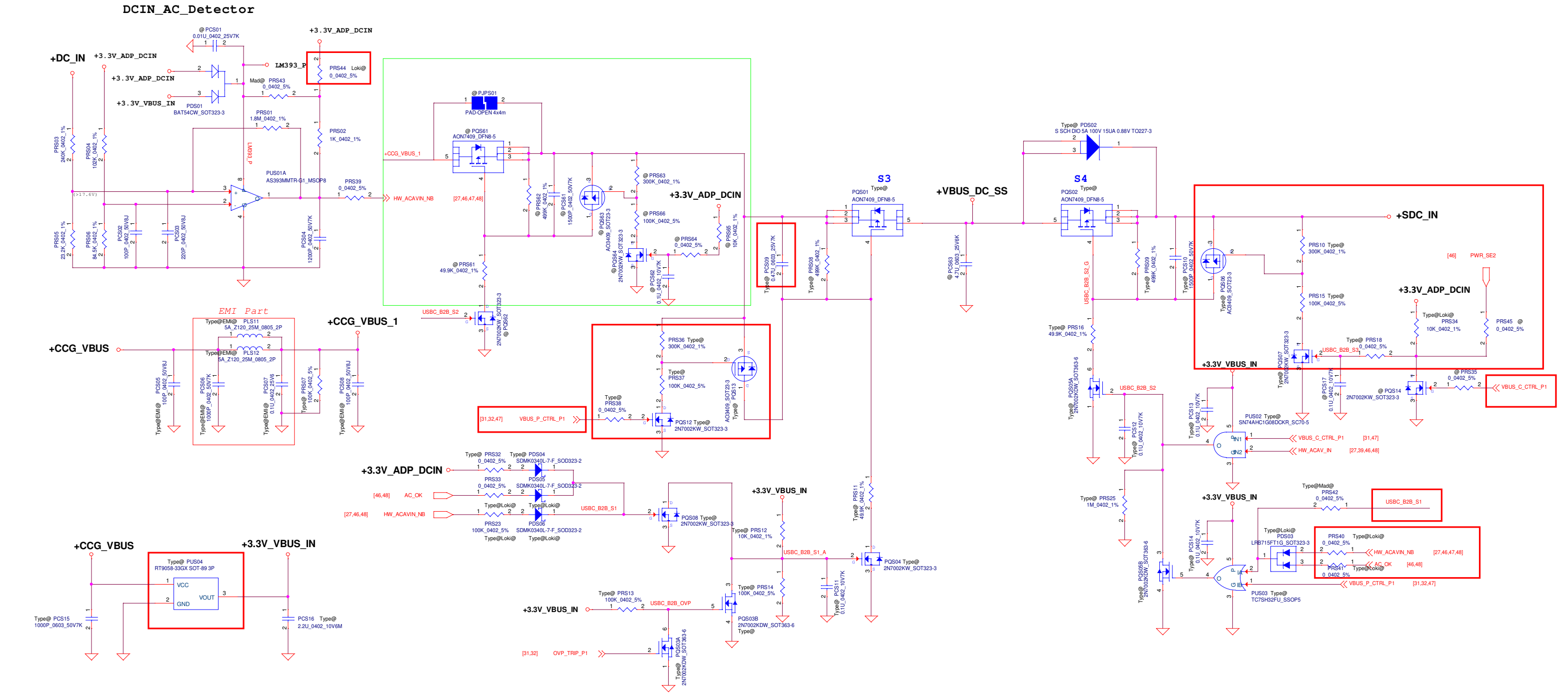
Compal Electronics, Inc.

Title: **PWR_DCIN/BATT CONN/OTP**

Size	Document Number	Rev
		X00

Date: Thursday, November 09, 2017 Sheet 46 of 59

Main Func = Type-C PD Selector



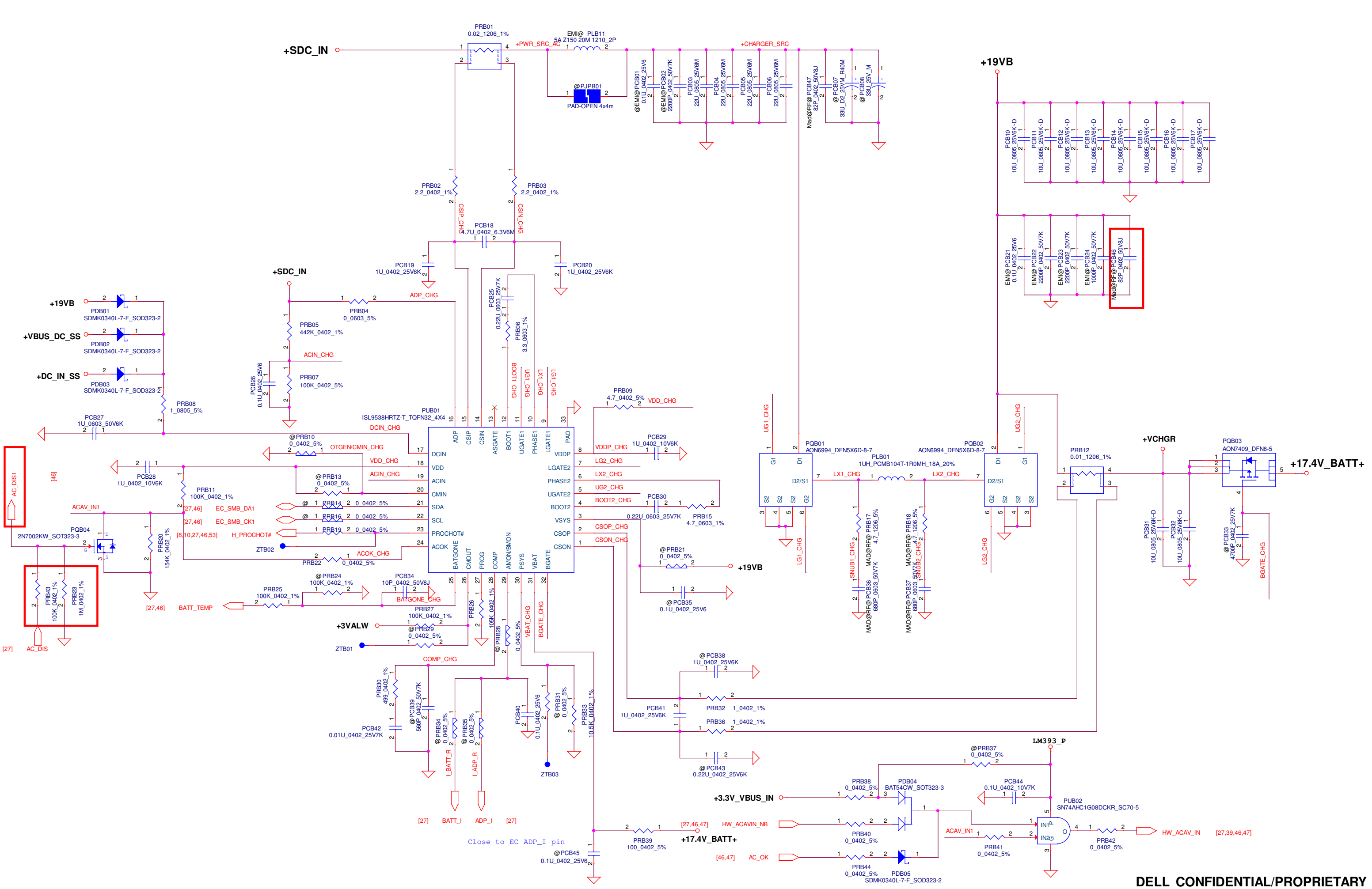
Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.

Title: **PWR_Type-C PD Selector**

Size | Document Number | Rev X00

Main Func = CHARGER



DELL CONFIDENTIAL/PROPRIETARY

Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

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Compal Electronics, Inc.

Title: *PWR_CHARGER*

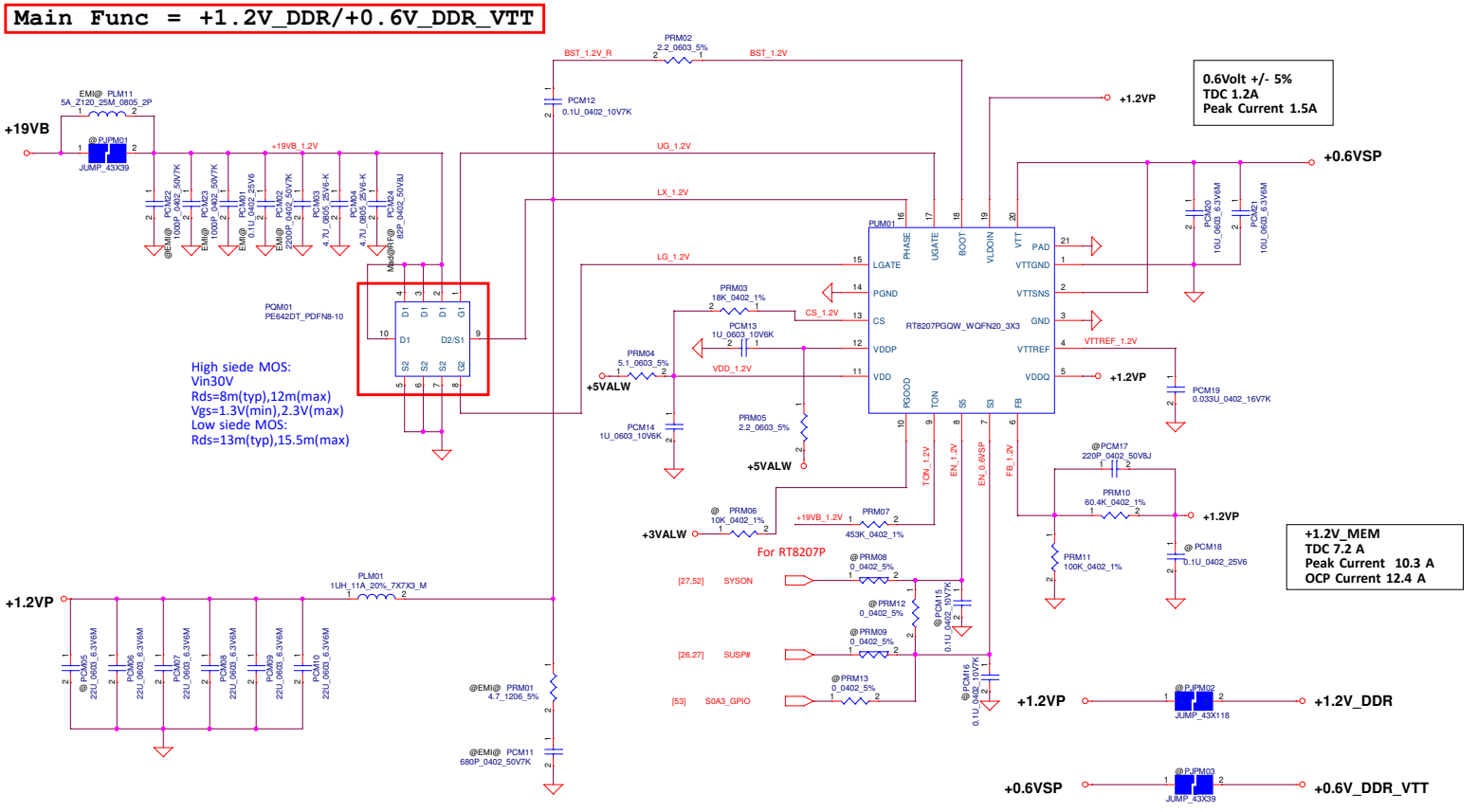
Size	Document Number	Rev
		X00

Date: Thursday, November 09, 2017 | Sheet 48 of 59

Main Func = 3.3VALWP/5VALWP

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2014/2/11	Deciphered Date	2014/2/11
Title	PWR_3.3VALWP/5VALWP		
Size	Document Number		Rev 0.(X00)
Date: Thursday, November 09, 2017	Sheet 49 of 59		

Main Func = +1.2V_DDR/+0.6V_DDR_VTT



Mode	S3	S5	+1.2V_MEN	+V_DDR_REF	+0.6V_P
S5	L	L	of f	off	of f
S3	L	H	on	on	of f
S0	H	H	on	on	on

Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

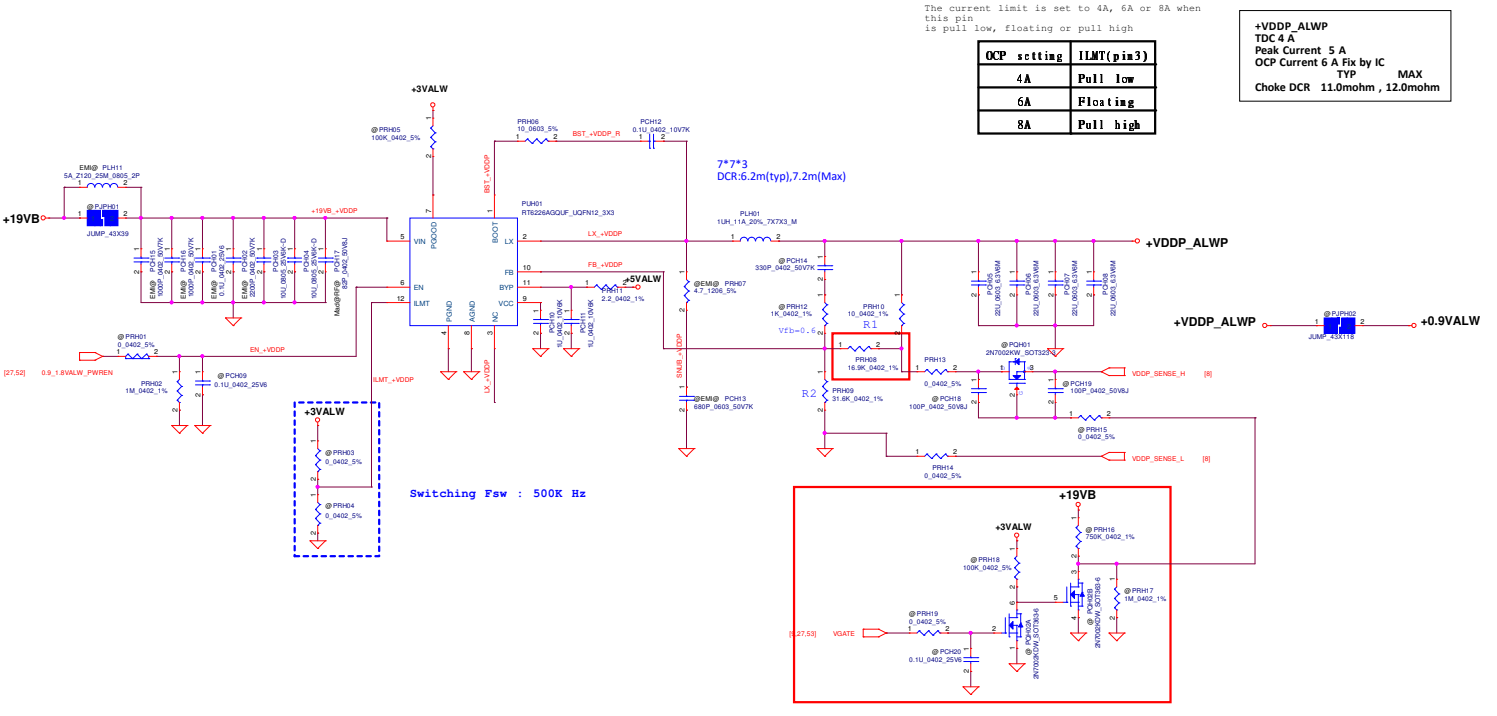
Compal Electronics, Inc.

Title: PWR_+1.2V_MEN/+0.6V_DDR_VTT

Size	Document Number	Rev
Custom		X00

Date: Thursday, November 09, 2017 Sheet 50 of 59

Main Func = +VDDP_ALWP



Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

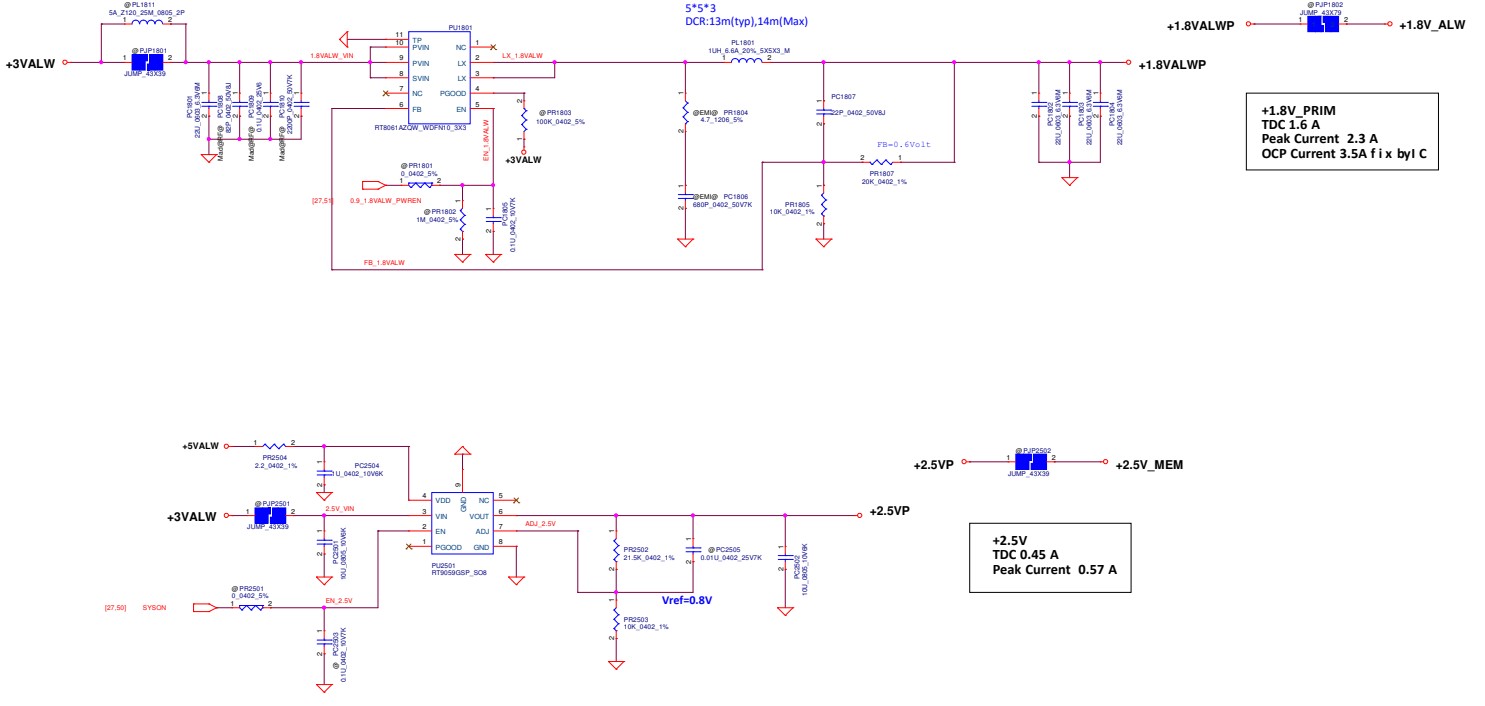
Compal Electronics, Inc.

Title: PWR +VDDP_ALWP

Size: C | Document Number: | Rev: X00

Date: Thursday, November 09, 2017 | Sheet 51 of 59

Main Func = +1.8VALWP / +2.5VP



Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

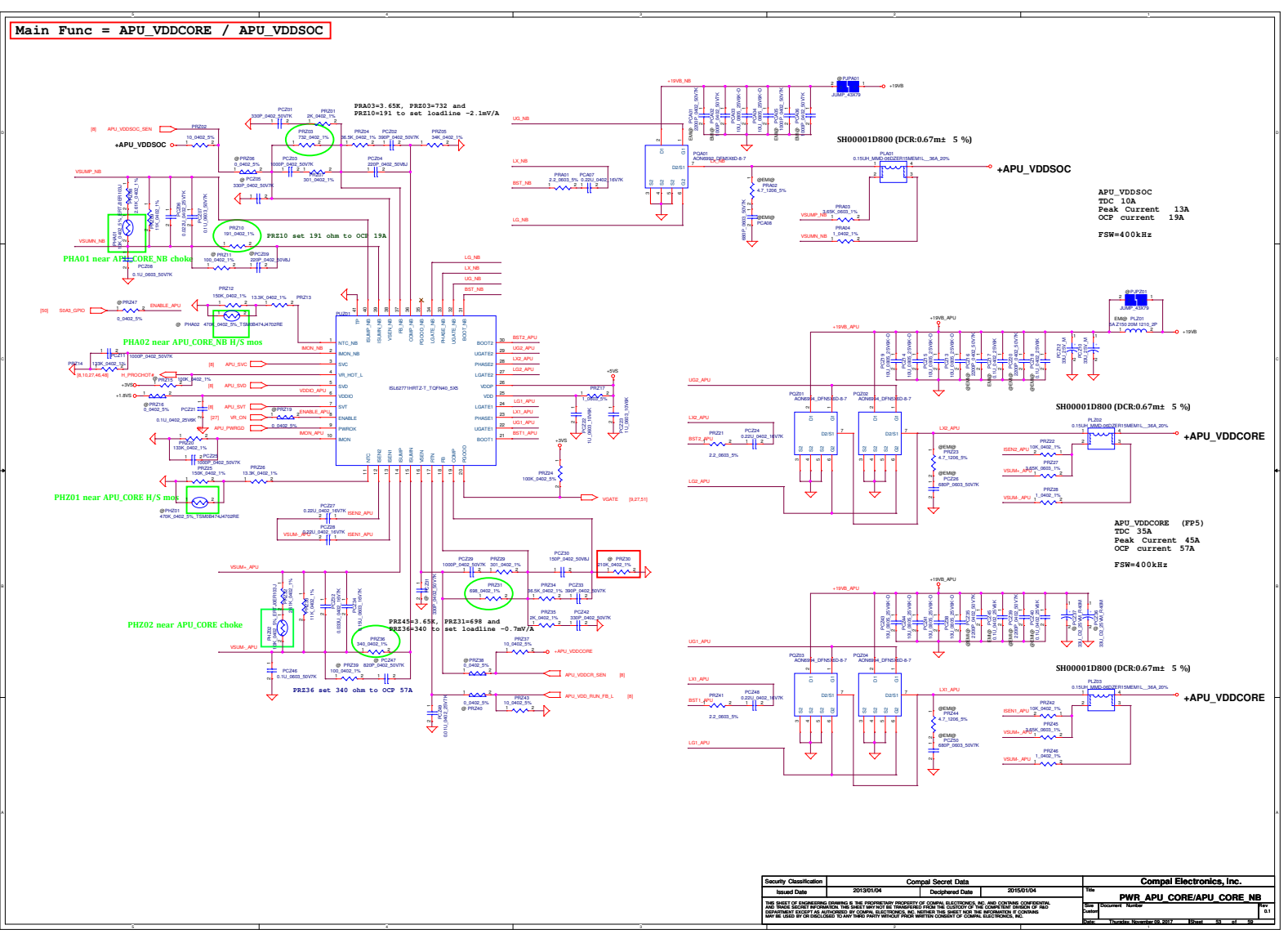
Compal Electronics, Inc.

Title: PWR +1.8V PRIM and +2.5V

Size	Document Number	Rev
C		X00

Date: Thursday, November 09, 2017 Sheet 52 of 59

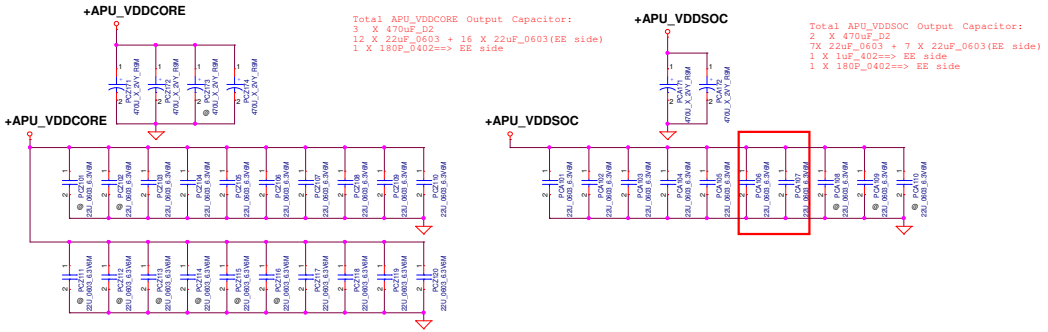
Main Func = APU_VDDCORE / APU_VDDSOC

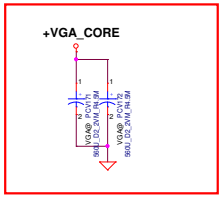


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/01/04	Deciphered Date	2015/01/04

Title	PWR_APU_CORE/APU_CORE_NB		
Size	Document Number		Rev
Custom			0.1
Date: Thursday, November 09, 2017		Sheet 53 of 59	

Main Func = APU/ VGA / APU_SOC MLCC

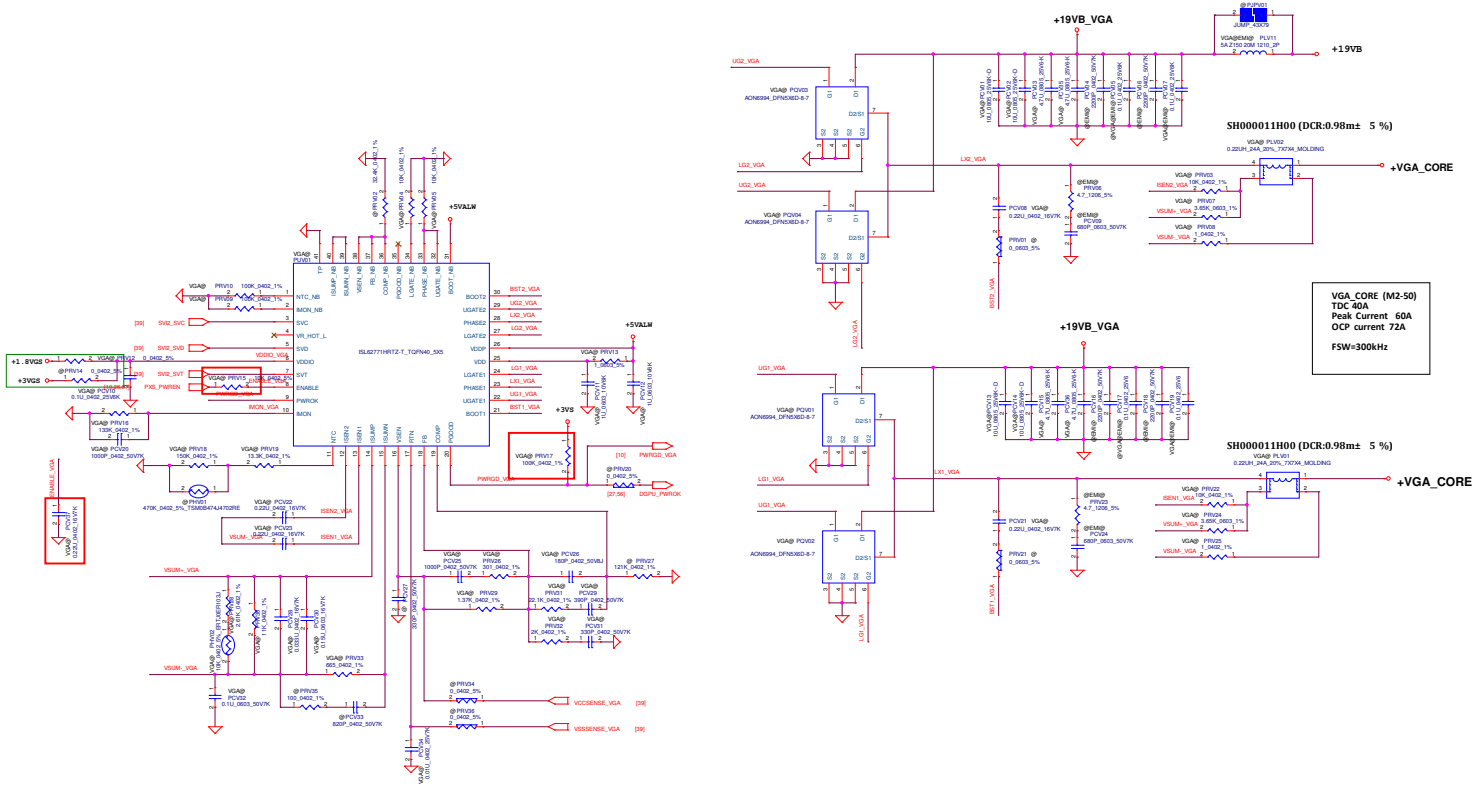




Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

Compal Electronics, Inc.	
Title	PWR_APU&VGA & NB MLCC
Size	Document Number / Rev X00
Date: Thursday, November 09, 2017	Sheet 54 of 59

Main Func = VGA CORE



Security Classification	Compal Secret Data		
Issued Date	2014/11/05	Deciphered Date	2014/12/15

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Compal Electronics, Inc.

Title: **PWR_VGA_CORE**

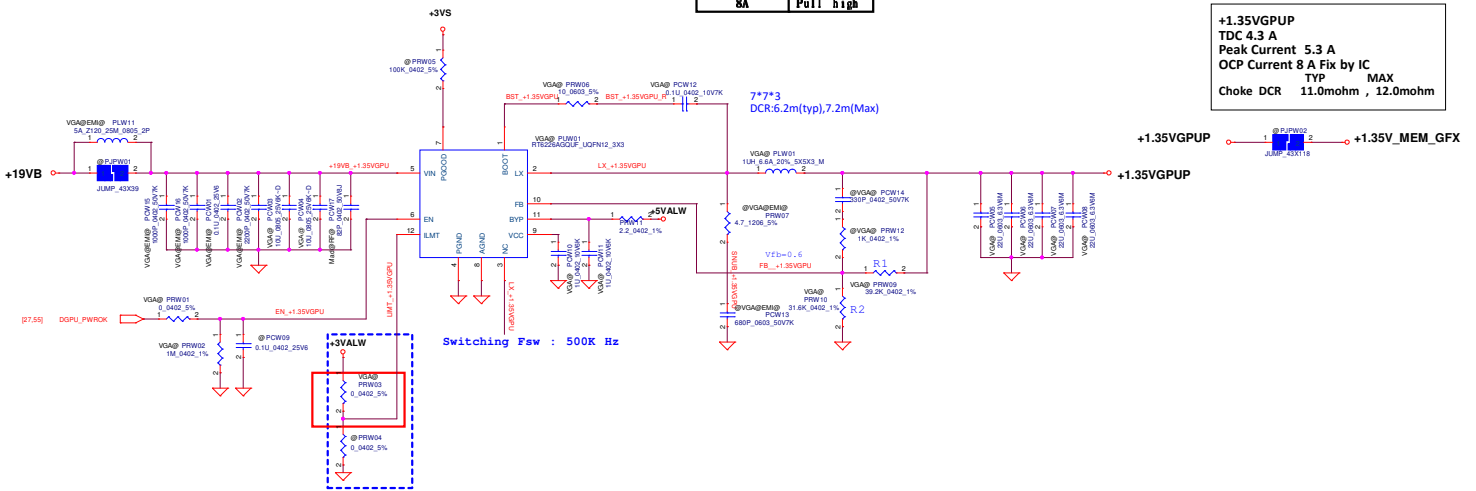
Size	Document Number	Rev
		X00

Date: Thursday, November 09, 2017 | Sheet 55 of 59

Main Func = +1.35VGPUP

OCP setting	ILMT(pin3)
4A	Pull low
6A	Floating
8A	Pull high

+1.35VGPUP
TDC 4.3 A
Peak Current 5.3 A
OCP Current 8 A Fix by IC
TYP MAX
Choke DCR 11.0mohm , 12.0mohm



Security Classification	Compal Secret Data		
Issued Date	2014/03/31	Deciphered Date	2015/04/30

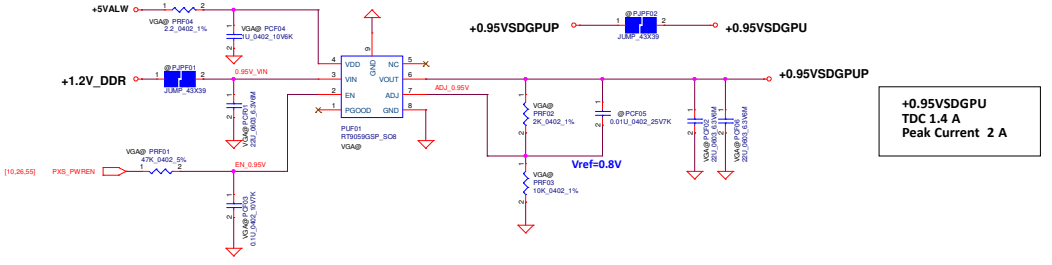
Compal Electronics, Inc.

Title: PWR +1.35VGPUP

Size	Document Number	Rev
		X00

Date: Thursday, November 09, 2017 Sheet 56 of 59

Main Func = +0.95VSDGPUP



Security Classification	Compal Secret Data		
Issued Date	2015/03/23	Deciphered Date	2014/12/15

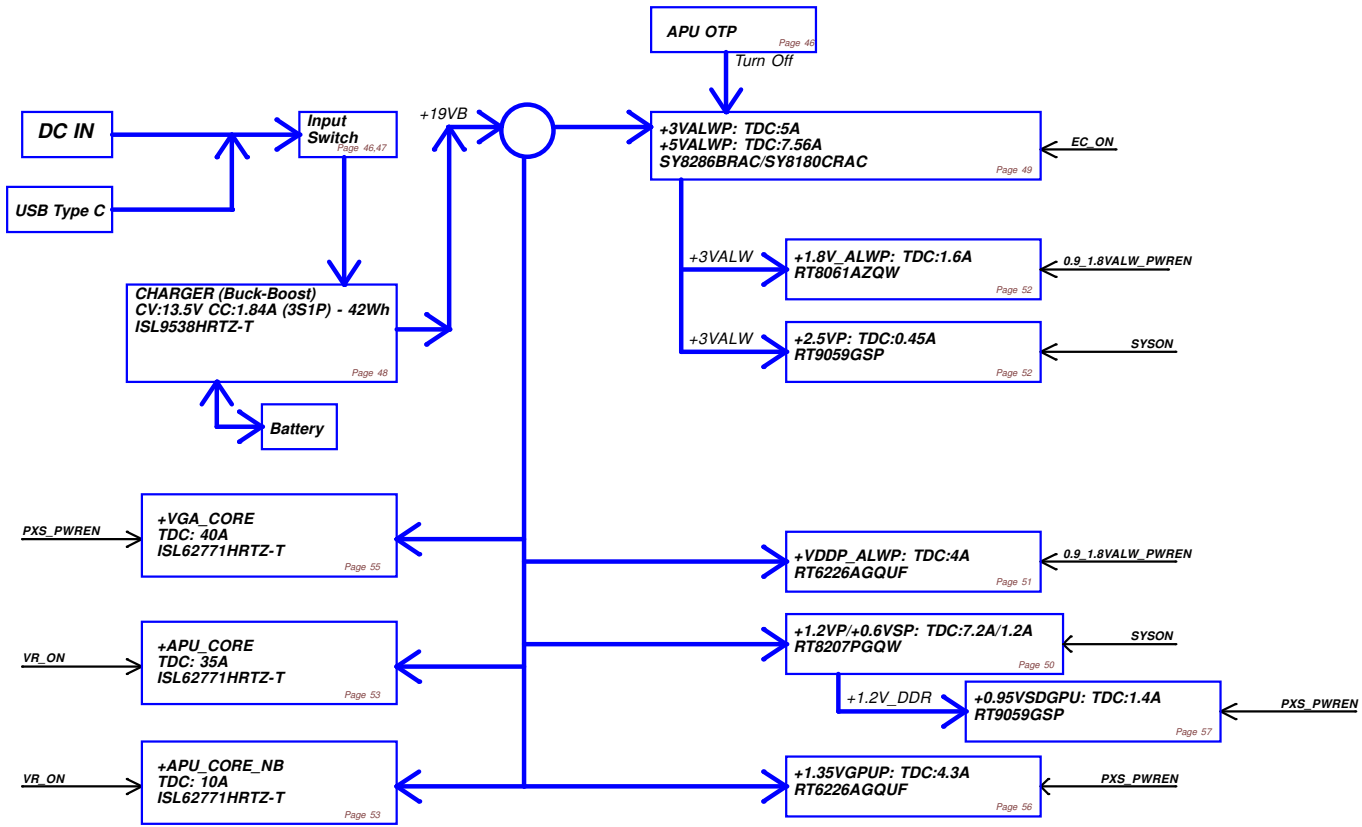
Compal Electronics, Inc.

Title: PWR +0.95VSDGPU

Size	Document Number	Rev
Custom		X00

Date: Thursday, November 09, 2017 Sheet 57 of 59

Power block



Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

Size: Document Number: Rev: 1.0

Date: Thursday, November 09, 2017 Sheet 58 of 59

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P46	PWR	20170704	COMPAL	EMI test result for change capacity	change PC2,PC4 from 0.1u to 2200p	0.2(X01)
2	P55	PWR	20170704	COMPAL	Request by EE for adjust DGPU sequence	change PRV15 from 0 to 10K and add PCV37 0.22u	0.2(X01)
3	P48	PWR	20170704	COMPAL	support FTRD 1.6 and LPS from EC request	change PRV15 from 0 to 10K and add PCV37 0.22u	0.2(X01)
4	P47	PWR	20170704	COMPAL	add fast close MOS	pop PQS06,PQS07,PQS13,PRS10,PRS15,PRS18,PRS36,PRS37,PRS38,PRS40.PRS41	0.2(X01)
5	P46	PWR	20170710	COMPAL	for LPS SW solution	add PQ20	0.2(X01)
6	P51	PWR	20170717	COMPAL	adjust output to 0.9V by EE request	change PRH08 from 10.7K to 15.8K	0.2(X01)
7	P46	PWR	20170917	COMPAL	follow Intel design	pop PR53 and unpop PR51	0.3(X02)
8	P46	PWR	20170917	COMPAL	follow Intel design	unpop PC23,PQS11,PRS30,PCS20 add PR100 1M	0.3(X02)
9	P54	PWR	20170918	COMPAL	for PSI_Dynamic test with AMD validation	pop PCA106,PCA107	0.3(X02)
10	P48	PWR	20170918	COMPAL	follow Intel design	unpop PCB46	0.3(X02)
11	P51	PWR	20170918	COMPAL	for VDDP_Static test with AMD validation	change PRH08 from 15.8K to 16.9K	0.3(X02)
12	P46	PWR	20170920	COMPAL	follow Intel design	change PC7,PC10 from 0.1U_10V to 0.1U_50V	0.3(X02)
13							

Compal Electronics, Inc.

Title: Changed-List PWR History

Size: | Document Number: | Rev: X00

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DVT1 change list

BOM change list

BOM Change							
Item		Date	Page	Part reference	Original CPN	New CPN	Change description	Reason
1		2017/6/2	33	RT52,RT53			bom structure from typec@ change to @	fix the typec i2c signal about DP out
2		2017/6/3	27	RE6			bom structure from notypec@ change to pop always	fix dead battery auto wakeup
3		2017/6/3	27	RE508			bom structure from typec@ change to @	fix dead battery auto wakeup
4		2017/6/19	27	RE9	SD034000080	SD034150280	0 ohm change to 15K	EC board id(UMA)
5		2017/6/19	27	RE9	SD034120280	SD034200280	12k change to 20K	EC board id(DSC)
6		2017/6/20	9	RC29,CC7,RC700			change to pop(PCIE_RESET_0)	fixed pcie rst singal
7		2017/6/20	9	RC704,CC100,RC701			change to unpop(PCIE_RESET_1)	pcie rst_1 signal code not ready
8		2017/7/6	10	C796	SE07156AD80	SE07147AC80	change part from 5.6P to 4.7P	fixed crystal accuracy
9		2017/7/6	10	C797	SE07156AD80	SE000011R00	change part from 5.6P to 3.9P	fixed crystal accuracy
10		2017/7/6	9	D5,D6		SCS000002Z00	add part (diode)	fix Panel will flash white screen when press power button (Bits333224)
11		2017/7/12	29	Q26		SB00000DH00	add part (dual mos) reserve	follow loki intel led design
12		2017/7/12	29	R82,R83		SD028100380	add part(100K) reserve	follow loki intel led design
13		2017/7/12	29,34	R800,RS62		SD028000080	add part(0 ohm)	follow loki intel led design
14		2017/7/12	23	CU38,CU39,CU40,CU41		SE00000P700	add part 0.33U	follow AMD require to add 0.33U Cap
15		2017/7/12	23	CU7,CU8,CU15,CU16	SE102104K00	SE095224K00	change part(0.1U to 0.22U)	follow AMD require to change to 0.22U Cap
16		2017/7/13	10	RC449	SD028330A80	SD028220A80	change part 33 ohm to 22 ohm	follow AMD SCL 1.04

GPIO change list

Signal for PCH				
Date	GPIO	Pin Definition		Reason
		R0.1(X00)	R0.2(X01)	
2017/6/3	AGPIO11	NC	MEM_ERROR_A	Memory error detection(Bits334733)
2017/7/4	AGPIO12	NC	MEM_ERROR_B	Memory error detection(Bits334733)
2017/7/4	EGPIO 70	NC	VBIOS_ID1	old GPIO SW no support
2017/7/10	AGPIO89	PXS_RST#	NC	fixed GPU Yellow bang
2017/7/10	AGPIO90	PXS_PWREN	KB_DET#	fixed GPU Yellow bang
2017/7/10	AGPIO86	PWRGD_VGA	NC	fixed GPU Yellow bang
2017/7/10	EGPIO 140	KB_DET#	PXS_RST#	fixed GPU Yellow bang
2017/7/10	EGPIO 141	NC	PXS_PWREN	fixed GPU Yellow bang
2017/7/10	EGPIO 143	NC	PWRGD_VGA	fixed GPU Yellow bang

KBC ENE 9022				
Date	GPIO	Pin Definition		Reason
		R0.1(X00)	R0.2(X01)	
2017/6/3	AGPIO0	NC	MEM_ERROR_A	Memory error detection(Bits334733)
2017/7/4	AGPIO39	NC	MEM_ERROR_B	Memory error detection(Bits334733)

Design change list

Design Change					
Item	Date	Page	Part reference	change description	Reason
Based on EVT					
1	2017/6/2	29		BATT_CHG_LED from R68.2 to R69.2 ,BATT_LOW_LED from R69.2 to R68.2	correct led color indication
2	2017/6/19	32		DT3~DT10 change footprint	meet DFB
3	2017/6/29	33		JUSBC1 change footprint	meet DFB
	2017/7/6	9		add D5,D6	fix Panel will flash white screen when press power button (Bits333224)
4	2017/7/11	36		JCRT from 20P coaxil to 16P ZIF	follow loki intel
5	2017/7/12	23		add RX cap footprint for usb compatible	follow AMD require
6	2017/7/12	29,34		add nvme led status circuit(reserve)	follow loki intel

DVT2 change list

BOM change list

BOM Change								
Item		Date	Page	Part reference	Original CPN	New CPN	Change description	Reason
1		2017/9/4	32	D2	SCA00001G00		unpop	follow ESD require
4		2017/9/4	27	RE9	SD034150280	SD034270280	15K change to 27K	EC board ID
5		2017/9/4	27	RE9	SD034200280	SD034330280	20K change to 33K	EC board ID
12		2017/9/4	11	RC801	SD028100580		add 10M	follow factory require for RTC detect
13		2017/9/4	11	QC27	SB00000EN00		add mos	follow factory require for RTC detect
14		2017/9/4	9	RC6130	SD028100280		add 10K	follow factory require for RTC detect
15		2017/9/8	18	CA50,CA51	SE071100J80		change to pop	follow EMI require
16		2017/9/18	33	RT132,RT133	SD028000080		add 0 ohm	follow SCL1.05

GPIO change list

Signal for PCH				
Date	GPIO	Pin Definition		Reason
		R0.2(X01)	R0.3(X02)	
	AGPIO7	NC	RTC_DET#	factory require
	AGPIO76	SPI_IRQ#	NC	PSP related GPIO
	AGPIO30	NC	SPI_IRQ#	PSP related GPIO
	EGPIO121	BT_ON#	NC	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.
	EGPIO120	NC	BT_ON#	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.

Design change list

Design Change					
Item	Date	Page	Part reference	change description	Reason
Based on DVT1					
1	2017/9/4	11	QC27,RC801,RC6130	add RTC coin battery detect circuit	for factory require
2	2017/9/4	27	RE9	UMA form 15K to 27K, DIS from 20K to 33K	EC board ID
3	2017/9/4	10,20	RC902	reserve (0 ohm)	BITS339503 DVT1-Loki-AMD:1810 WLAN/BT device lost after resume from S3/S4/CB/WB.
4	2017/9/12			I2C0 change to I2C3	BITS332966 ULV-Loki-AMD: Lost some items in Touchpad setting.
5	2017/9/18	33	RT132,RT133	add series resistor for APU_DP3_AUXP/APU_DP3_AUXN	follow SCL 1.05