Compal Confidential

DULU 330C (DLID4 / DLID5)

DIS M/B Schematic Document

Intel KabyLake U/KabyLake R Processor with DDR4

MX110 (23x23mm)

2018-03-09

LA-G201P

REV :1.0

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

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Title	Cover Page		
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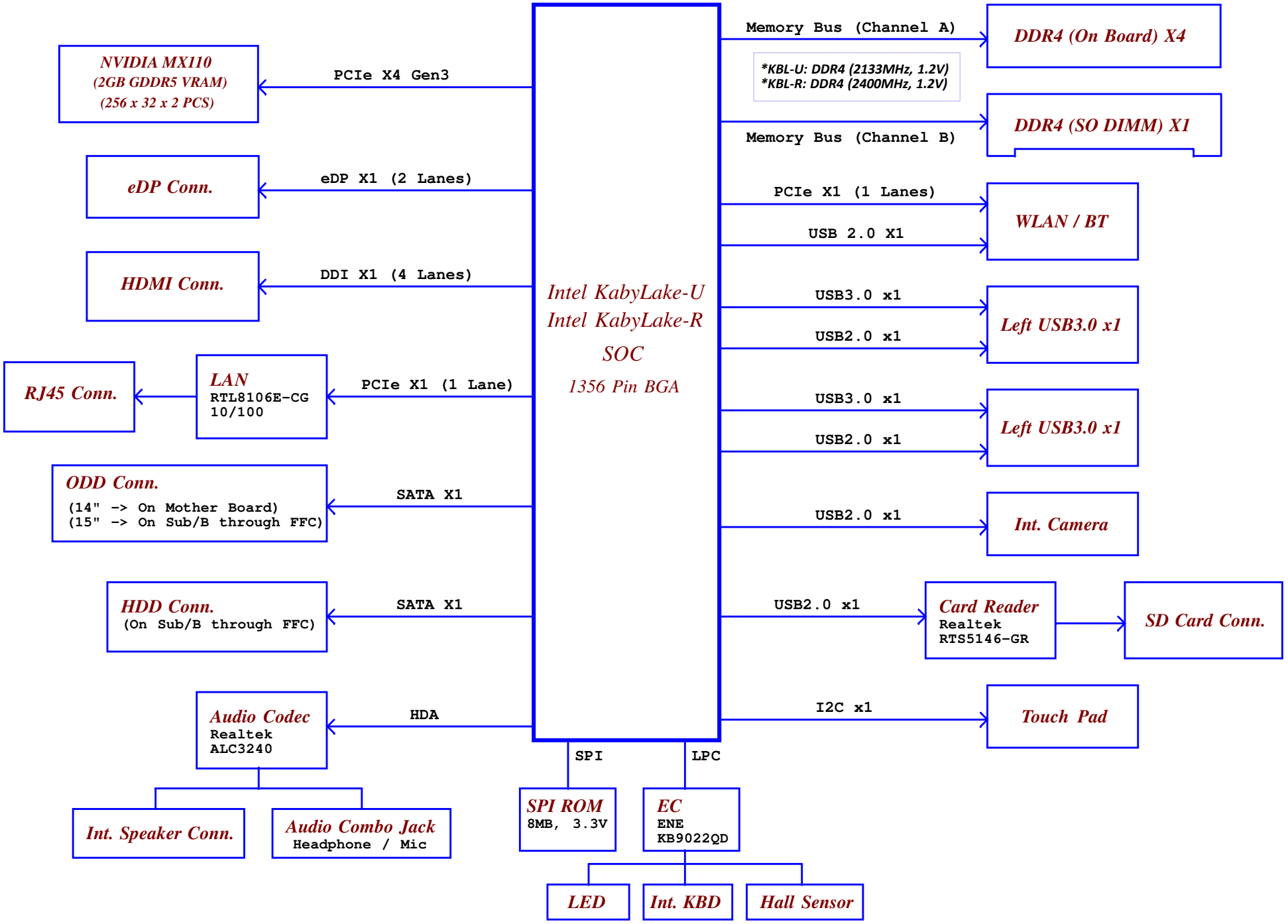

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: Block Diagram
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Voltage Rails

power plane / State	B+	+5VALW +3VALW	+1.2V	+5VS +3VS +1.35VS +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.6VS +1.0VALW
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
DIS Only Components	DIS@
UMA Only Components	UMA@
14" Only Components	14@
15" Only Components	15@
HDMI Logo	45@
GIGA LAN Reserved Items	8111GLDO@
Memory Down - SDP Package	SDP@
Memory Down - DDP Package	DDP@
GPU GC6 Components	GC6@
Un-Mount GPU GC6 Components	NOGC6@
GPU	N16S_R1@
	N16S_R3@
	N16V_R1@
	N16V_R3@
EMI Category	EMI@
ESD Category	ESD@
RF Category	RF@
EMI Un-Mount Items	@EMI@
ESD Un-Mount Items	@ESD@
RF Un-Mount Items	@RF@
Connectors	ME@
Test Point	TP@
Intel Debug Components	@DCI@
Un-Mount Components	@
CPU Components - U22 Only	U22@
CPU Components - U42 Only	U42@
EMI U22 Components	U22_EMI@
EMI U42 Components	U42_EMI@
CPU	i3_7020U_R1@
	i5_8250U_R1@
	i5_8250U_R3@
	i7_8550U_R1@
	i7_8550U_R3@
	i3_8130U_R1@

Item	BOM Structure
X4E	X4E_U22_14@
	X4E_U22_15@
	X4E_U42_14@
	X4E_U42_15@
On Board RAM (Hynix 4GB)	H4G_MD@
On Board RAM (Micron 4GB)	M4G_MD@
On Board RAM (Samsung 4GB)	S4G_MD@
On Board RAM X76 Resistors	X76RAM@
Realtek Card Reader	RTK_CR@
Genesys Card Reader	GNS_CR@
VRAM (Hynix 2GB)	H2G_VRAM@
	H2G@
	H2G_R1@
	H2G_R3@
VRAM (Hynix 4GB)	H4G_VRAM@
	H4G@
	H4G_R1@
	H4G_R3@
VRAM (Micron 2GB)	M2G_VRAM@
	M2G@
	M2G_R1@
	M2G_R3@
VRAM (Micron 4GB)	M4G_VRAM@
	M4G@
	M4G_R1@
	M4G_R3@
VRAM (Samsung 2GB)	S2G_VRAM@
	S2G@
	S2G_R1@
	S2G_R3@
VRAM (Samsung 4GB)	S4G_VRAM@
	S4G@
	S4G_R1@
	S4G_R3@

USB 2.0 Port Table

Port	External USB Port
1	
2	USB2/3 Port (MB-1)
3	USB2/3 Port (MB-2)
4	
5	Camera
6	Card Reader
7	NGFF WLAN+BT

USB 3.0 Port Table

Port	
1	
2	USB2/3 Port (MB-1)
3	USB2/3 Port (MB-2)
4	
5	
6	

SATA Port Table

Port	
0	HDD
1	ODD

PCIE Port Table

Lane	Port	
1	1	GPU
2		
3		
4		
5		LAN
6		NGFF WLAN+BT
7		
8		
9		
10		
11		
12		

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x 16h

EC SM Bus2 address

Device	Address
NCT7718W	1001 100x 98h

PCH SM Bus address

Device	Address
DDR_JDIMM1 Touch Pad	1010 000x A0h

GPU SM Bus address

Device	Address
Internal thermal sensor	1001 111x 9Eh

SMBUS Control Table

	SOURCE	VGA	BATT	CHARGER	NECP388	SODIMM	Thermal Sensor	DGPU			TP	PCH	G-SENSOR
SMB_EC_CK1 SMB_EC_DA1	NECP388 +3VALW	X	V +3VALW	V +19V_VIN	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	NECP388 +3VS	V +3VGS	X	X	V +3VS	X	V +3VS	X	X	X	X	V +3VS	X
SMB_EC_CK4 SMB_EC_DA4	NECP388 +3VALW	X	X	X	X	X	X	X	X	X	X	X	V +3VS
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	X	V +3VS	X	X	X	X	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	V +3VS	X	X	X
SML1CLK SML1DATA	PCH +3VALW	X	X	X	V +3VS	X	X	V +3VS	X	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

X4E

U42 — ZZZ X4E_U42@ — X4E U42 X4EABQ38L01

U22 — ZZZ X4E_U22@ — X4E U22 X4EABQ38L02

ON BOARD RAM * 4

ZZZ S4G_MD@ — X76 SAMSUNG 4GB MD X7677538LT3

ZZZ M4G_MD@ — X76 MICRON 4GB MD X7677538L14

ZZZ H4G_MD@ — X76 HYNIX 4GB MD X7677538L15

HDMI Logo

ZZZ 45@ — HDMI Logo RO0000003HM

CARD READER

*Main Source - Realtek
*Substitute - Genesys

PCB

ZZZ 14_DAZ@ — PCB DAZ29900201

ZZZ 15_DAZ@ — PCB DAZ23A00201

GDDR5 VRAM * 2

2GB

ZZZ H2G_VRAM@ — X76 HYNIX 2GB X7677538L06

ZZZ M2G_VRAM@ — X76 MICRON 2GB X7677538L05

ZZZ S2G_VRAM@ — X76 SAMSUNG 2GB X7677538L04

GPU

*N16V - MX110 (Device ID: 0x174E)
*N16S - MX130 (Device ID: 0x174D)

UV1 N16S_R1@ — N16S-GTR-S-A2 BGA 595P SA00009FP00

UV1 N16V_R1@ — N16V-GMR1-S-A2 BGA 595P SA00009IT00

UV1 N16S_R3@ — N16S-GTR-S-A2 BGA 595P SA00009FP30

UV1 N16V_R3@ — N16V-GMR1-S-A2 BGA 595P SA00009IT30

CPU

KBL U22 (= U22@)

UC1 i3_7020U_R1@ — QNZU H0 2.3G SA0000BLH10

UC1 i3_7020U_U22@ — SR3TK H0 2.3G SA0000BLH50

KBL U42 (= U42@)

UC1 i5_8250U_R1@ — SR3LA Y0 1.6G FCBGA SA0000AWB20

UC1 i7_8550U_R1@ — SR3LC Y0 1.8G FCBGA SA0000AWC20

UC1 i3_8130U_R1@ — QP8K Y0 2.2G SA0000BKN20

UC1 i5_8250U_R3@ — SR3LA Y0 1.6G FCBGA SA0000AWB50

UC1 i7_8550U_R3@ — SR3LC Y0 1.8G FCBGA SA0000AWC50

UC1 i3_8130U_R3@ — SR3W0 Y0 2.2G SA0000BKN30

UC1 i3_7020U_U42@ — SR3LD Y0 2.3G SA0000BLD60

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Issued Date	2018/03/09	Deciphered Date	2019/03/09

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Title: Notes List

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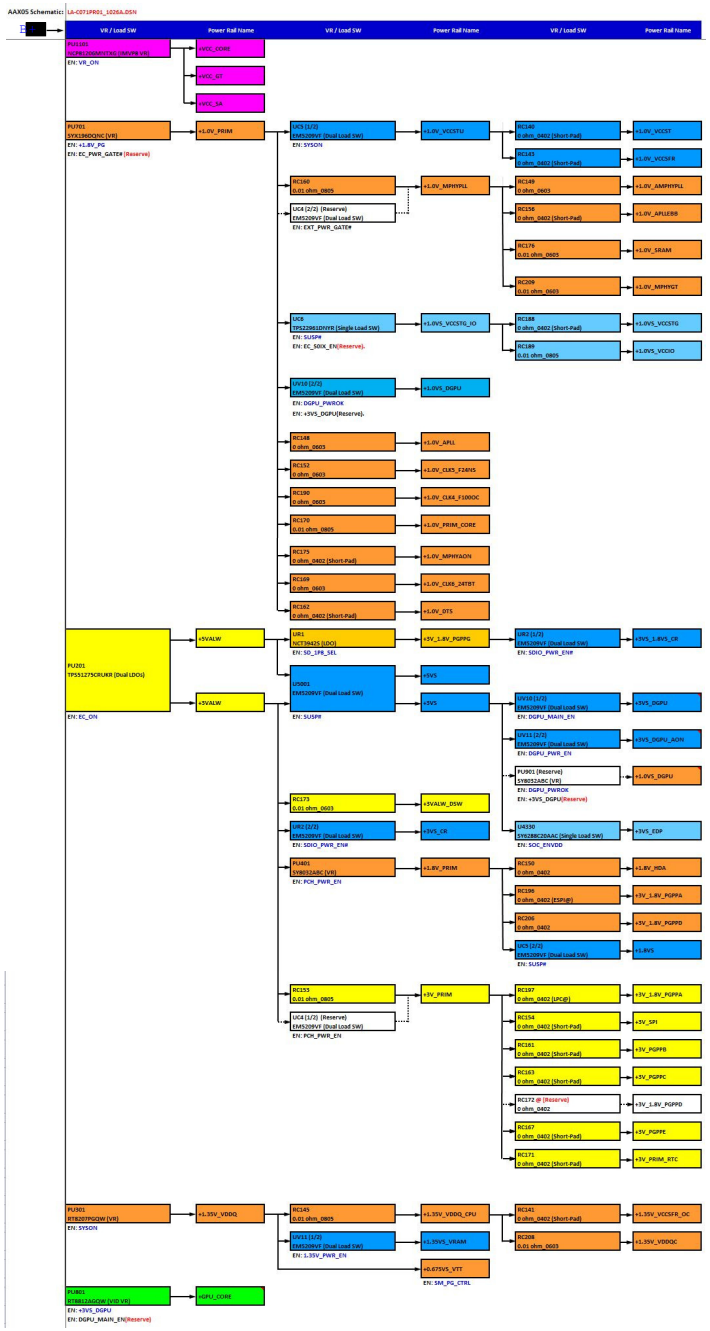
-PowerMap_KBL_DDR4_Volume_NON CS]



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Issued Date	2018/03/09	Deciphered Date	2019/03/09	Title	Power MAP
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Title: Power Sequence

Size	Document Number	Rev
		1.0

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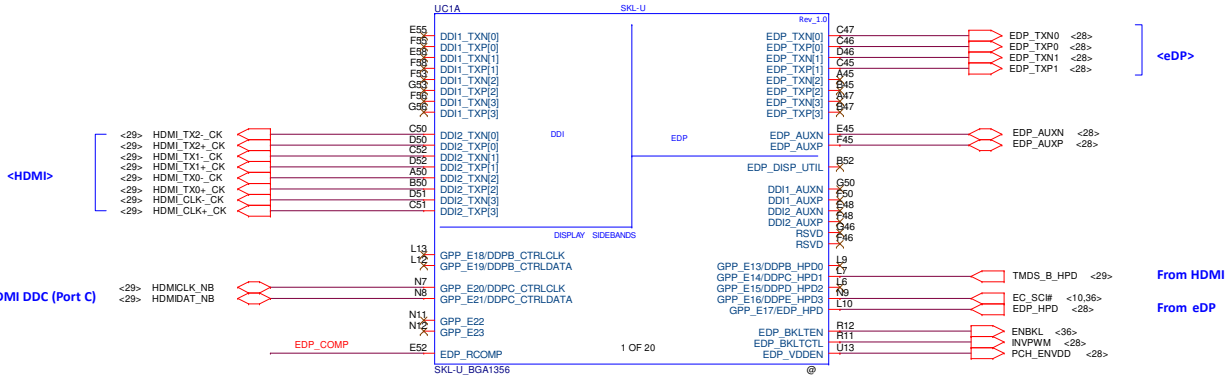


< Compensation PU For eDP >

+1.0VS_VCCIO

RC3 1 2 EDP_COMP 24.9_0402_1%

Trace width=20 mils, Spacing=25mil, Max length=100mils

+1.0V_VCCST

RC5 1 2 H_THERMTRIP# 1K_0402_5%

+1.0VS_VCCIO

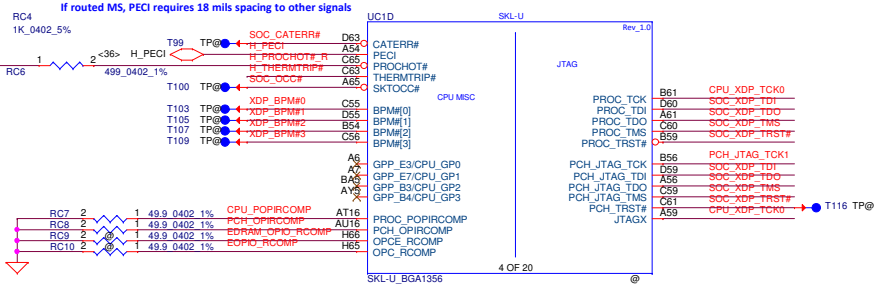
RC4 1K_0402_5%

If routed MS, PECI requires 18 mils spacing to other signals

<36> H_PROCHOT#

RC6 499_0402_1%

<36> H_PECI



< PU/PD for CMC Debug >

+1.0VS_VCCIO

SOC_XDP_TMS RC11 51_0402_5%

SOC_XDP_TDI RC12 51_0402_5%

SOC_XDP_TDO RC13 51_0402_5%

CPU_XDP_TCK0 RC14 51_0402_5%

PCH_JTAG_TCK1 RC15 51_0402_5%

SOC_XDP_TRST# RC23 51_0402_5%

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Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,EDP,MISC,CMC

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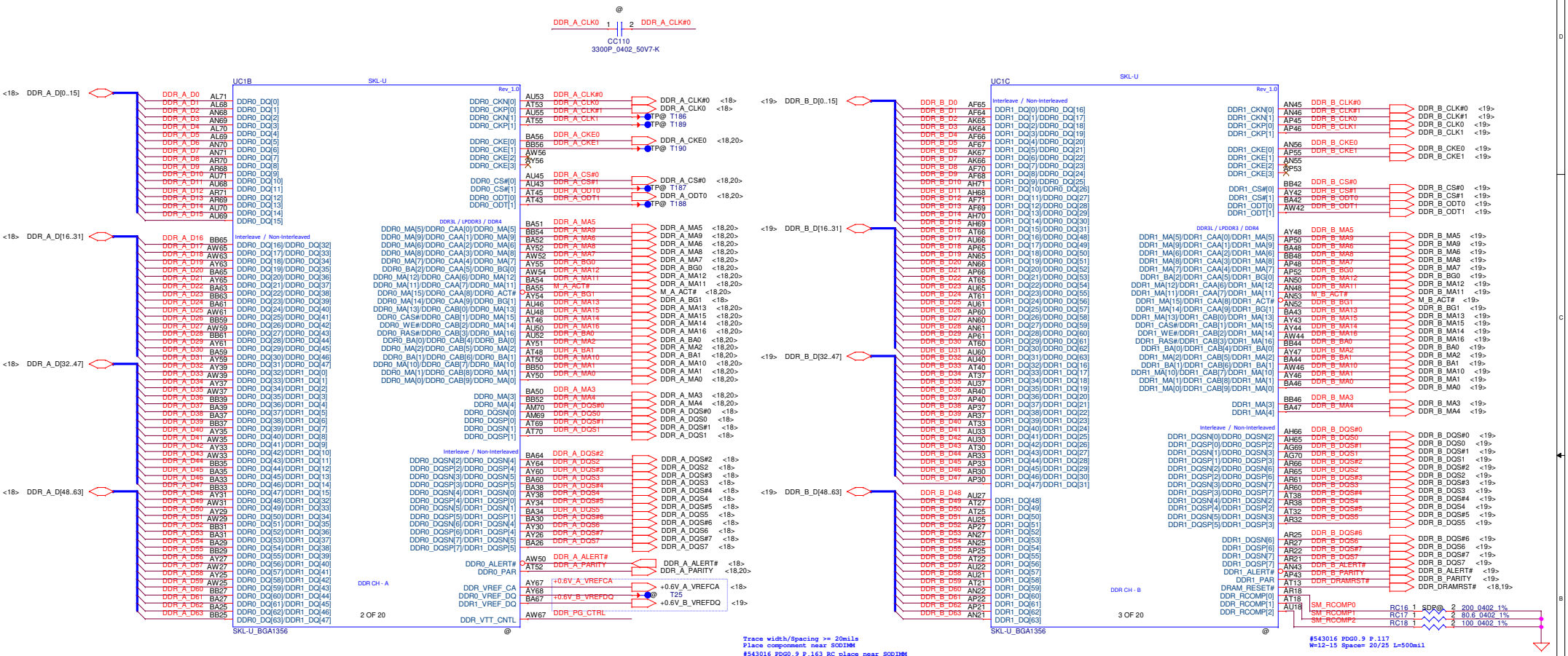
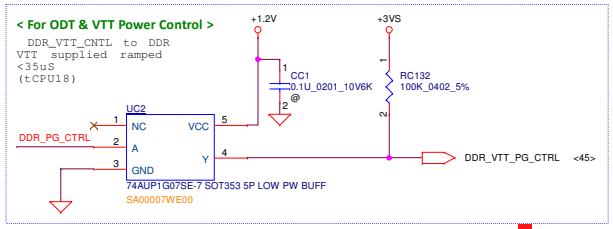
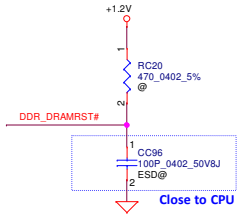
Interleaved Memory







Recommended By Intel Max

RC16
SD034121090
121_0402_1%
DDP@

www.laptoprepairsecrets.com

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Compal Electronics, Inc.	
Title	SKL-U(2/12)DDR3L
Size: Custom	Document Number: LA-G201P
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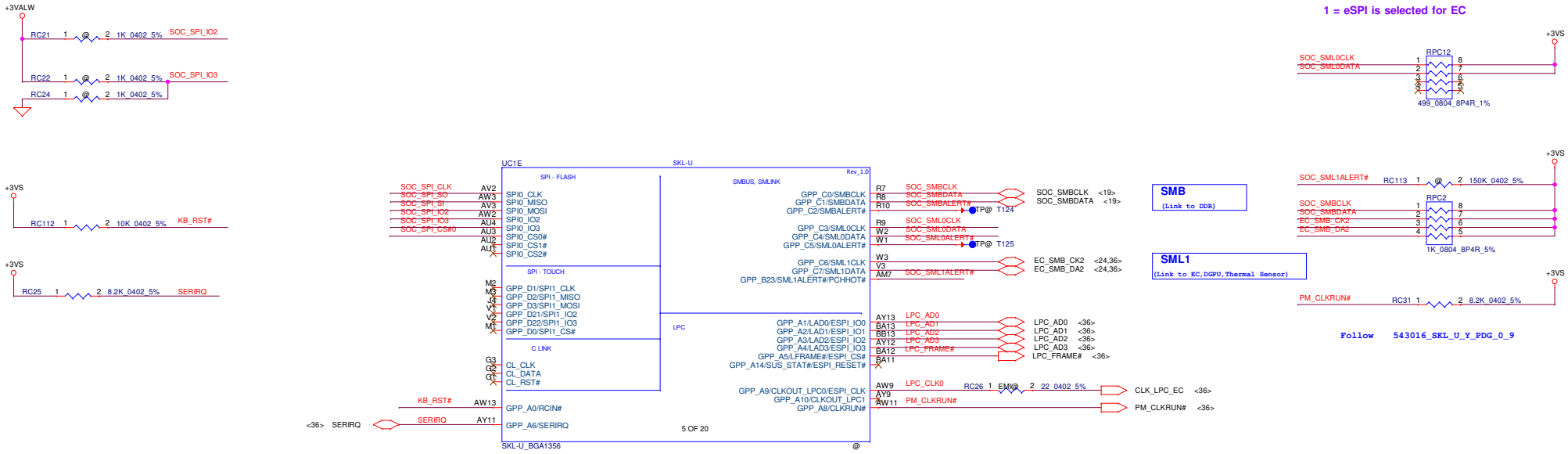
SML0ALERT# (Internal Pull Down):

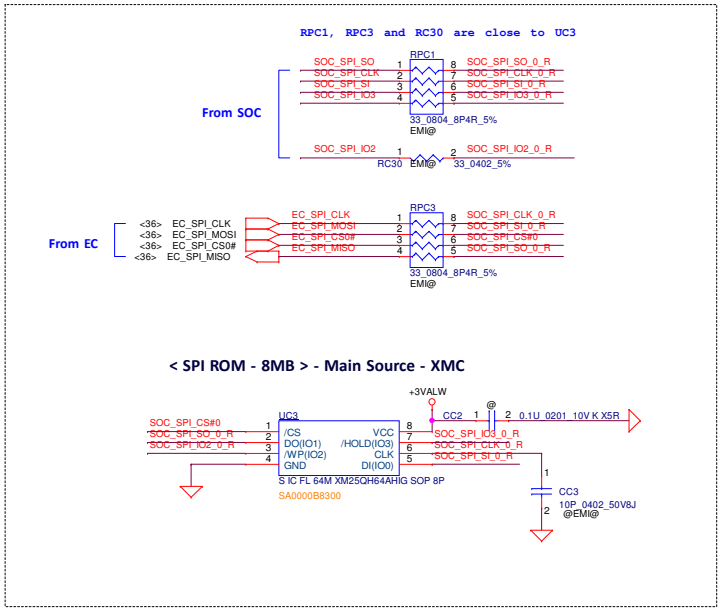
eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC



Follow 543016_SKL_U_Y_PDG_0_9



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Compal Electronics, Inc.

Title: SKL-U(3/12)SPI,SMB,LPC,ESPI

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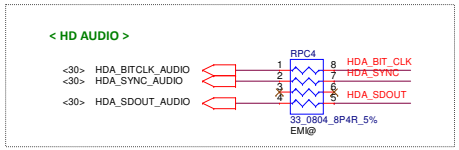
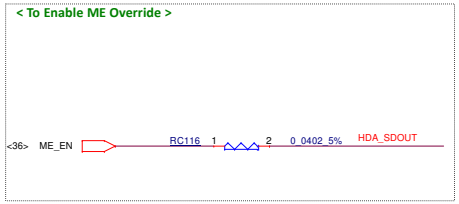
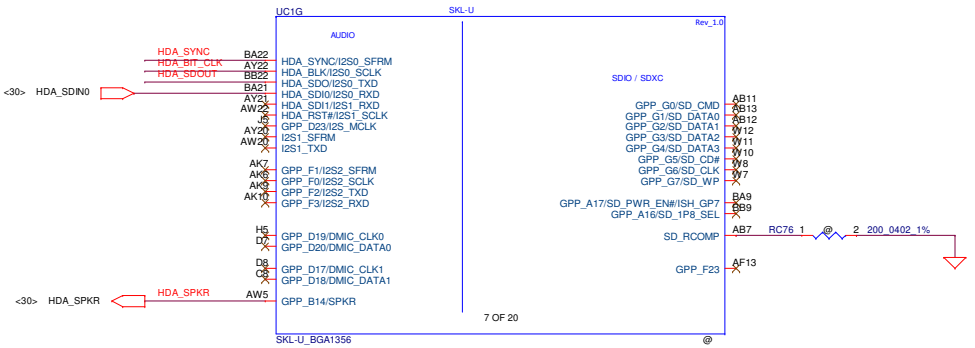
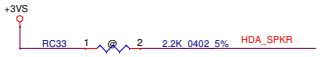






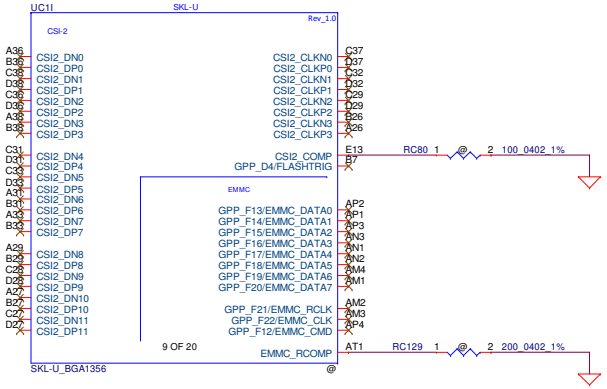


SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.



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Compal Electronics, Inc.		
Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2		
Size: Custom	Document Number: LA-G201P	Rev: 1.0
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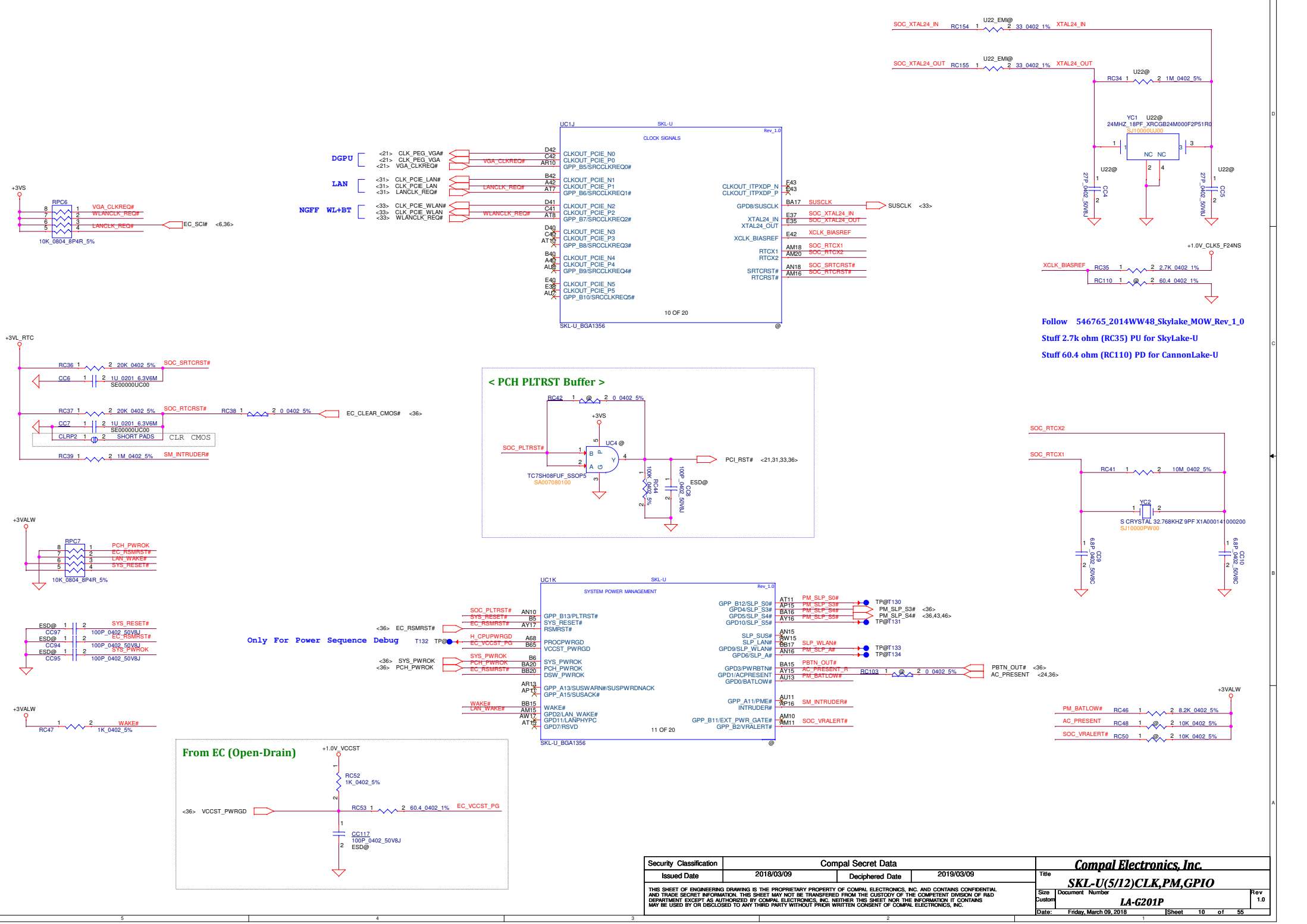

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: SKL-U(5/12)CLK,PM,GPIO

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GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode. ==> Default

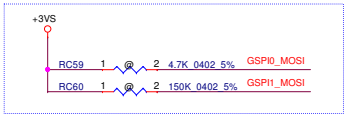
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This funct i oni s usef ul when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

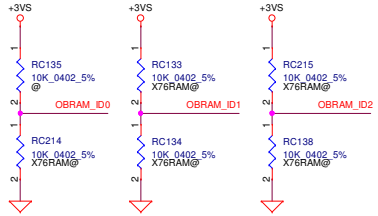
0 = SPI Mode ==> Default

1 = LPC Mode

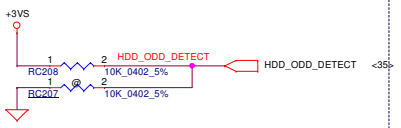


Capacity	Description	X76	PART NUMBER (R3)
4GB	WITHOUT ON-BOARD RAM	N/A	N/A
	SAMSUNG 2666MHz (K4A8G165WC-BCTD)	X7677538L13	SA0000B6F10
	HYNIX 2666MHz (H5AN8G6NCJR-VKC)	X7677538L15	SA0000BMN10
	MICRON 2666MHz (MT40A512M16LY-075:E)	X7677538L14	SA0000ARD30
	N/A	N/A	N/A
	N/A	N/A	N/A
	N/A	N/A	N/A
	N/A	N/A	N/A

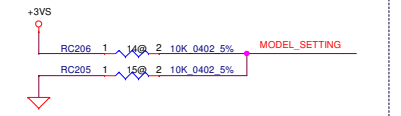
Capacity	Description	GPP_B19 OBRAM_ID0	GPP_B20 OBRAM_ID1	GPP_B21 OBRAM_ID2
4GB	WITHOUT ON-BOARD RAM	0	0	0
	SAMSUNG 2666MHz (K4A8G165WC-BCTD)	0	0	1
	HYNIX 2666MHz (H5AN8G6NCJR-VKC)	0	1	0
	MICRON 2666MHz (MT40A512M16LY-075:E)	0	1	1
	N/A	1	0	0
	N/A	1	0	1
	N/A	1	1	0
	N/A	1	1	1



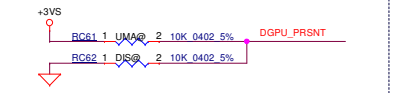
Function	HDD_ODD_DETECT (GPP_D11)
Mount ODD	0
Mount 2nd HDD	1



Function	MODEL_SETTING (GPP_D12)
15"	0
14"	1

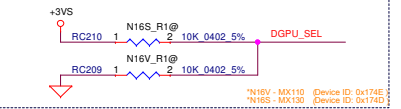


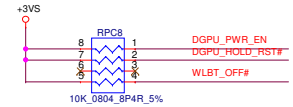
Function	DGPU_PRSNT (GPP_C15)
DIS	0
UMA Only	1

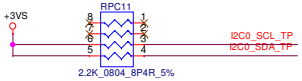


Function	DGPU_SEL (GPP_A20)
N16V-GMR1 (MX110)	0
N16S-GTR (MX130)	1

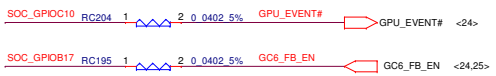
RC210 N16S_R3@ 10K_0402_5%
RC209 N16V_R3@ 10K_0402_5%



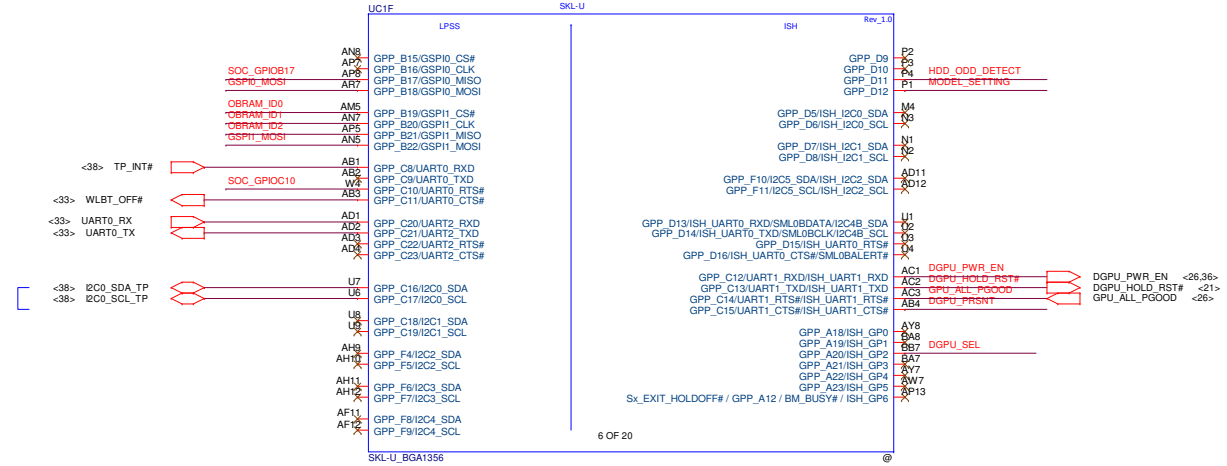




Touch PAD



TO DGPU



Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO,I2C,GSPI

Size	Document Number	Rev
Custom	LA-G201P	1.0

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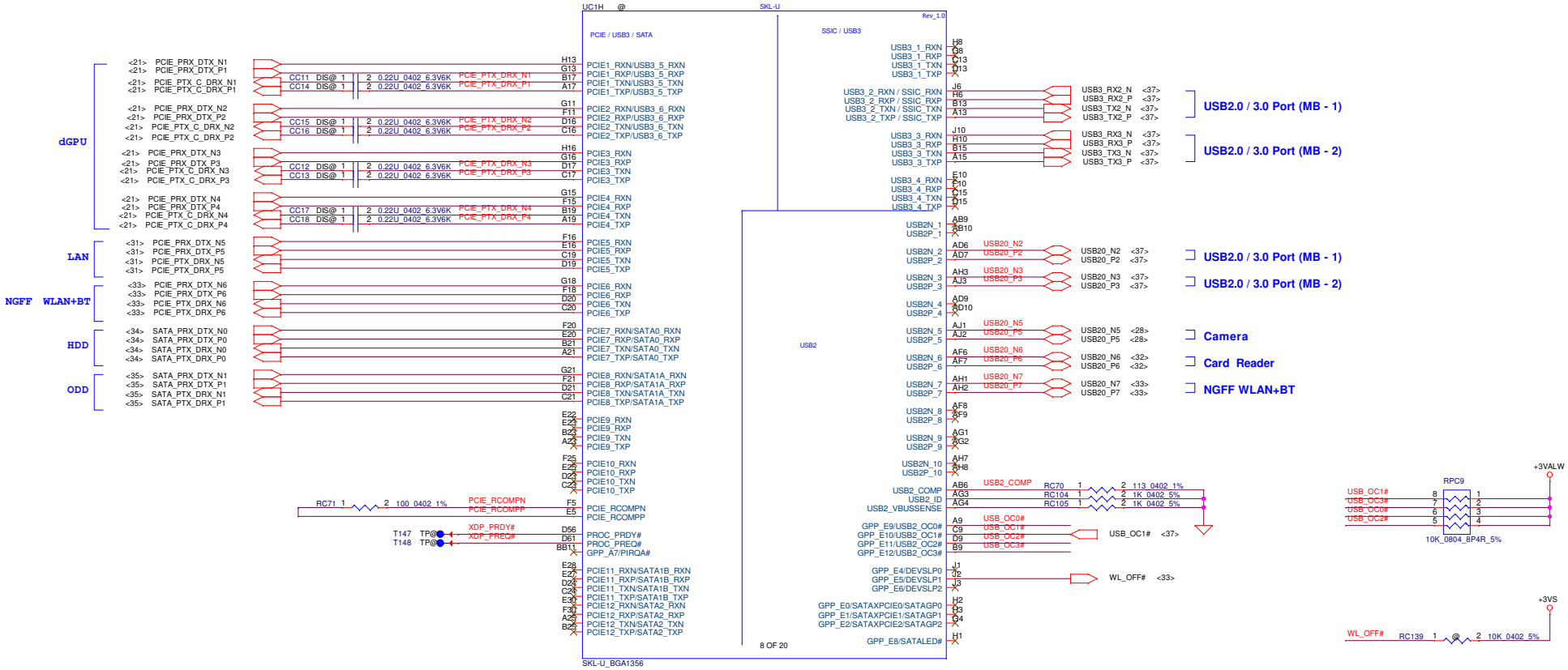

When PCIE8/SATA1A is used as SATA Port 1 (ODD), then PCIE11/SATA1B (M.2 SSD) cannot be used as SATA Port 1.

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: SKL-U(7/12)PCIE,USB,SATA

Size	Document Number	Rev
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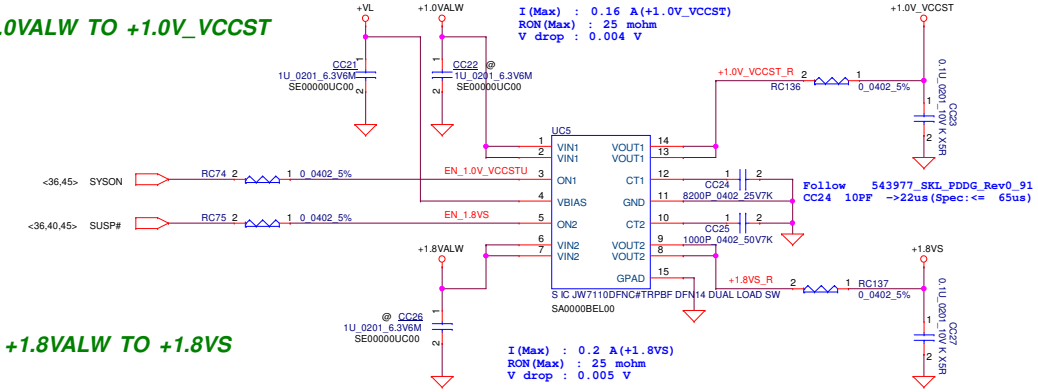
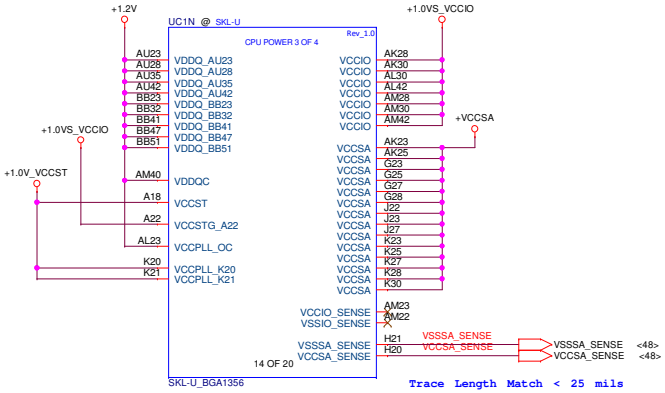
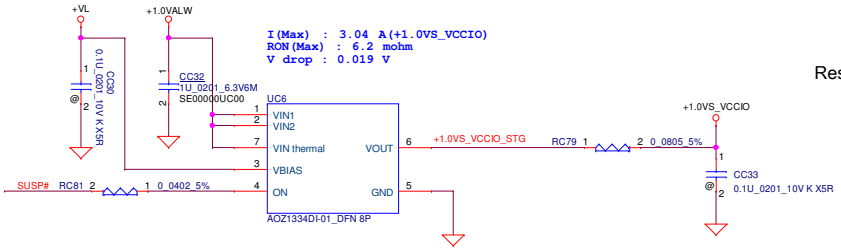
+1.0VALW TO +1.0V_VCCST



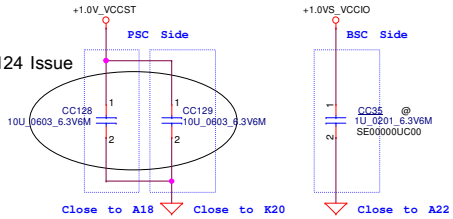
+1.8VALW TO +1.8VS

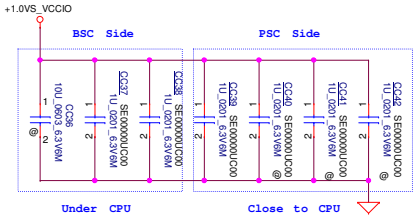


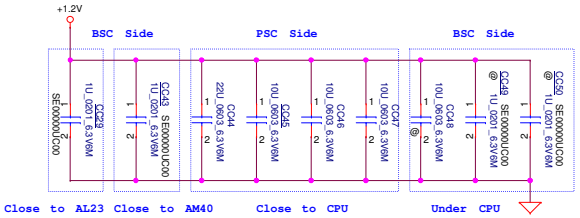
+1.0VALW TO +1.0VS_VCCIO



Reserved for BSoD 0x124 Issue

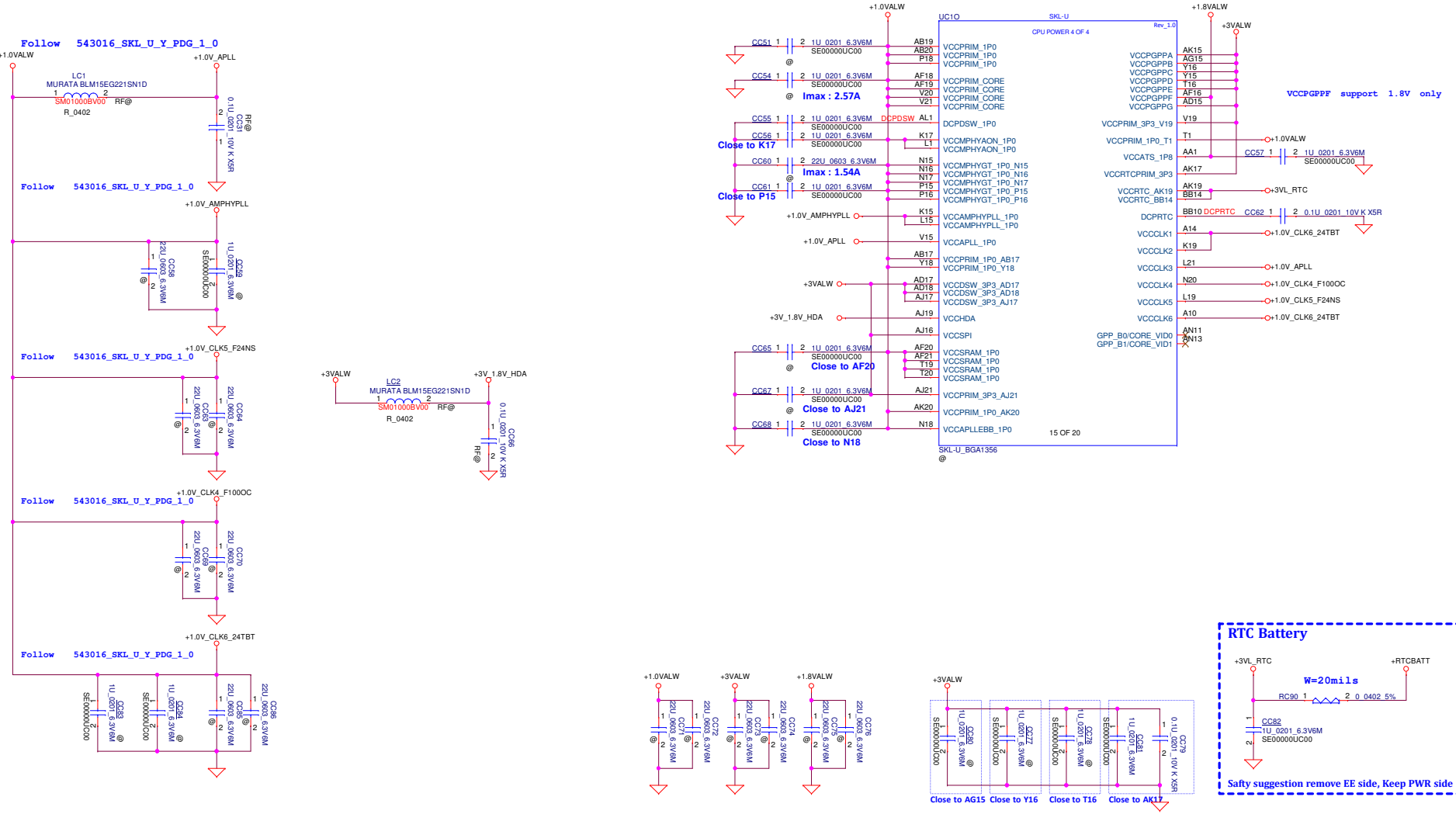






Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.			
Title	SKL-U(8/12)Power		
Size Custom	Document Number LA-G201P		Rev 1.0
Date: Friday, March 09, 2018	Sheet 13 of 55		



RTC Battery

Safty suggestion remove EE side, Keep PWR side

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.			
Title: SKL-U(9/12)Power			
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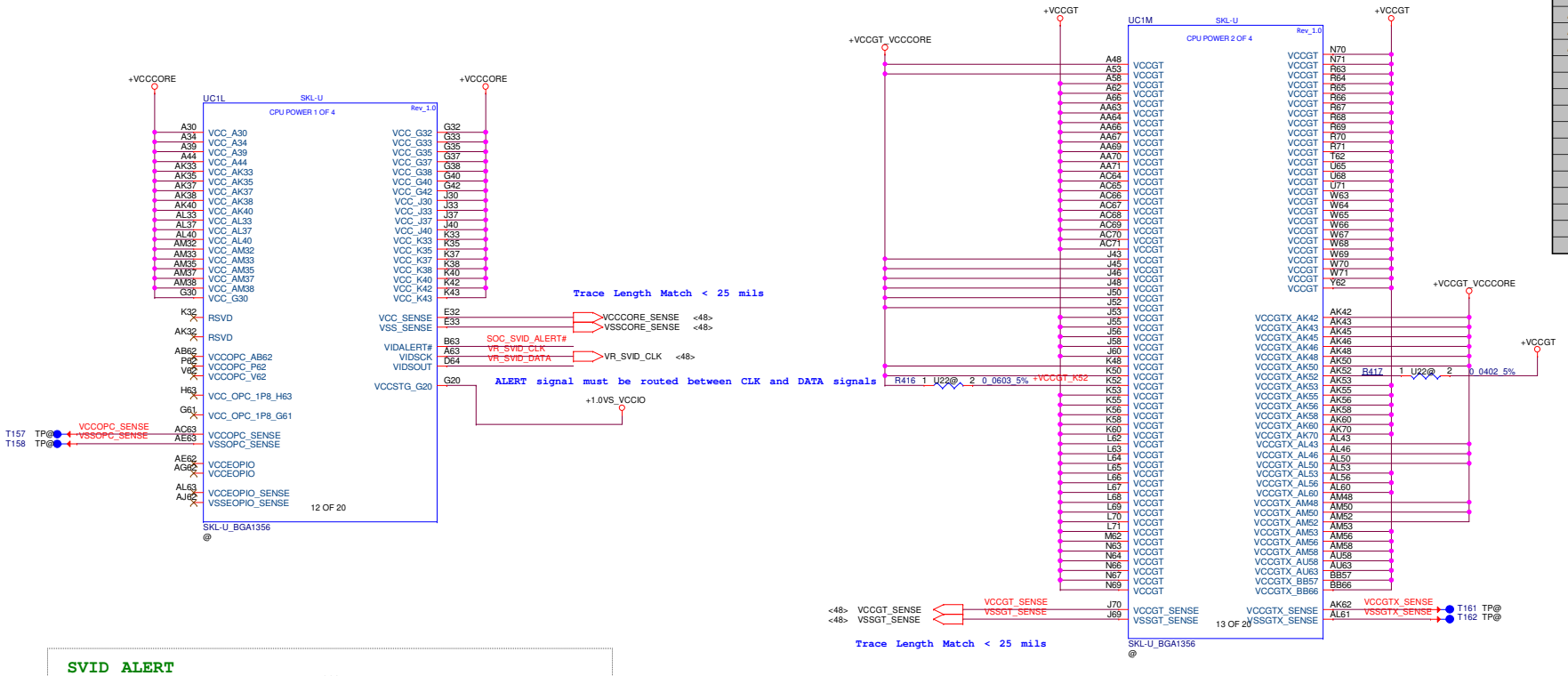
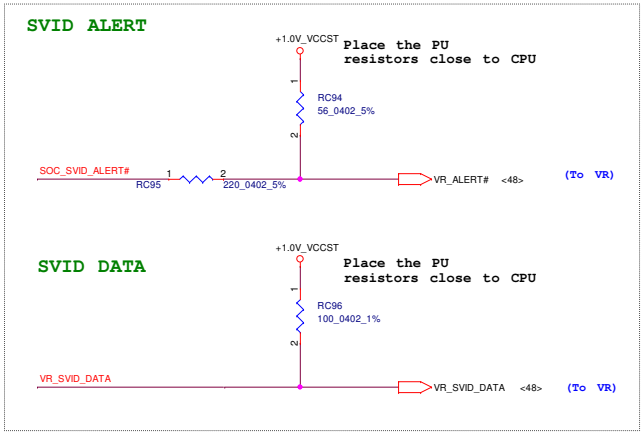
Ball #	Ball Names R-U42	Ball Names U22
C7	XTAL24_OUT	NC
E3	XTAL24_IN	NC
E35	NC	XTAL24_OUT
E37	NC	XTAL24_IN
AK42	VCCCORE	VccGTx
AK43		
AK45		
AK46		
AK48		
AK50		
AL43		
AL46		
AL50		
AM48		
AM50		
AM52		
J43		VCCGT
J45		
J46		
J48		
J50		
J52		
K48		
K50		
A48		
A53		
AK52	RSVD	VccGTx
K52	RSVD	VCCGT





Security Classification	Compal Secret Data	
Issued Date	2018/03/09	Deciphered Date 2019/03/09

Compal Electronics, Inc.

Title: SKL-U(10/12)Power,SVID

Size	Document Number	Rev
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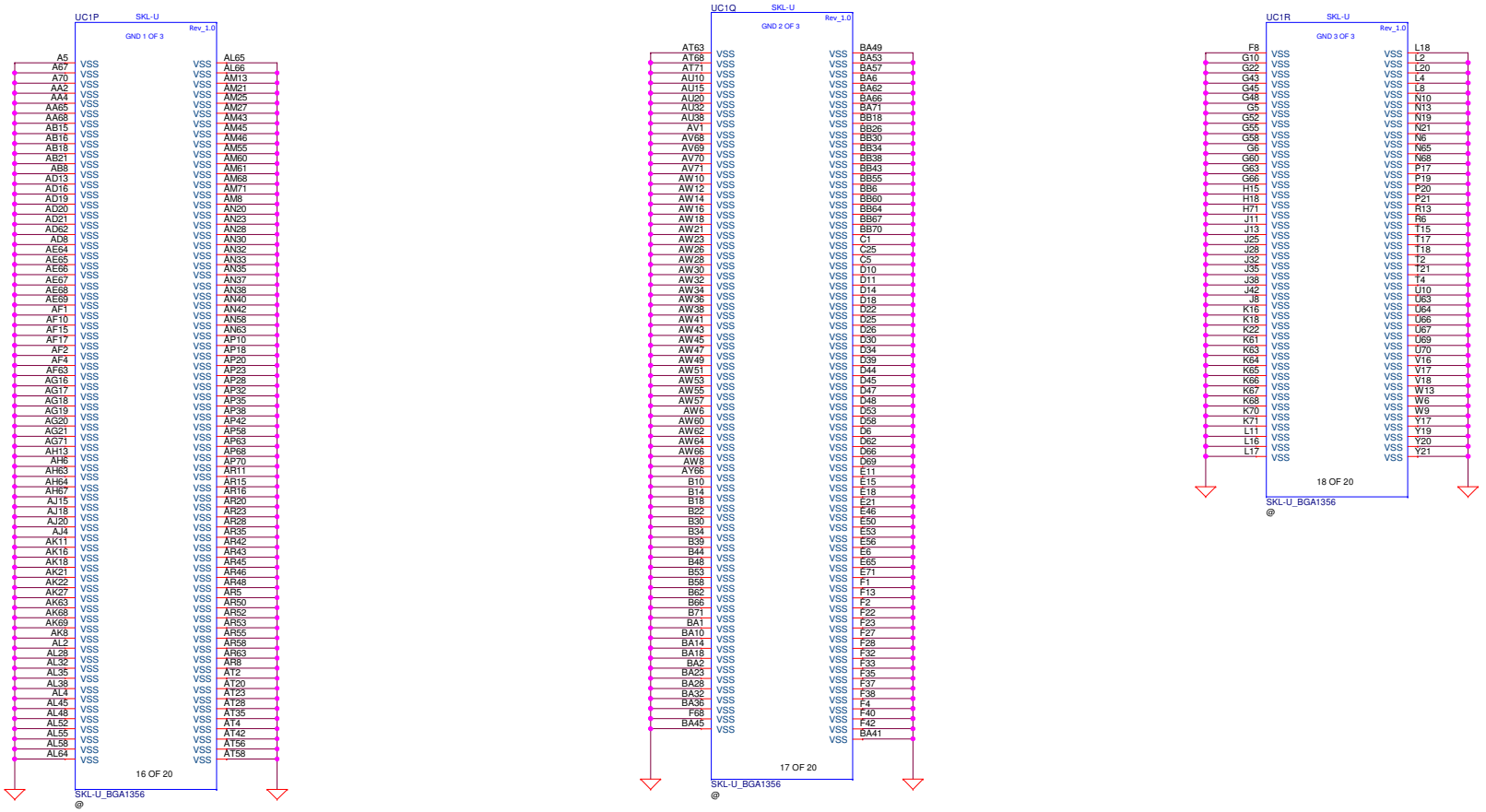

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: **SKL-U(11/12)GND**

Size	Document Number	Rev
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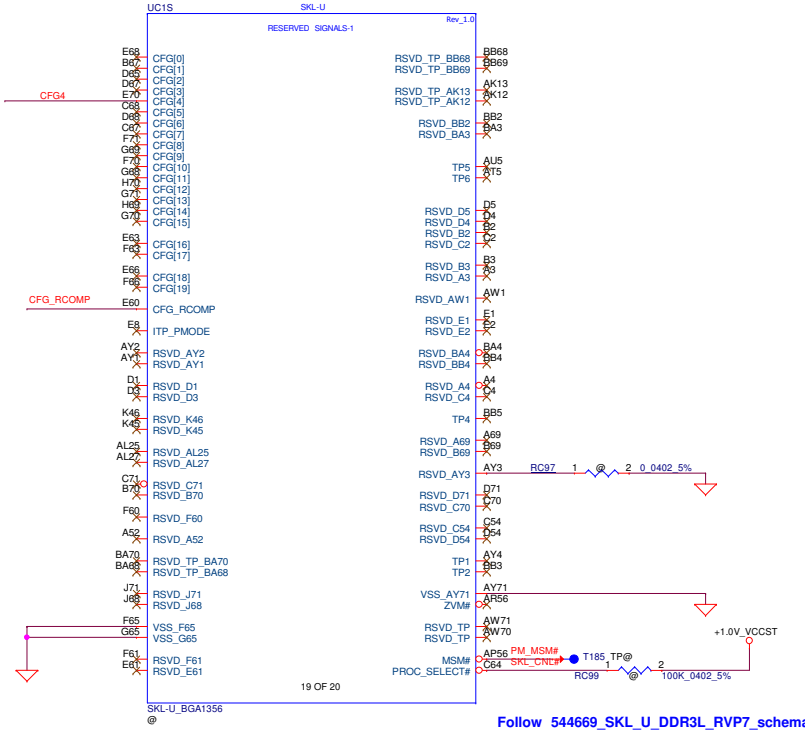
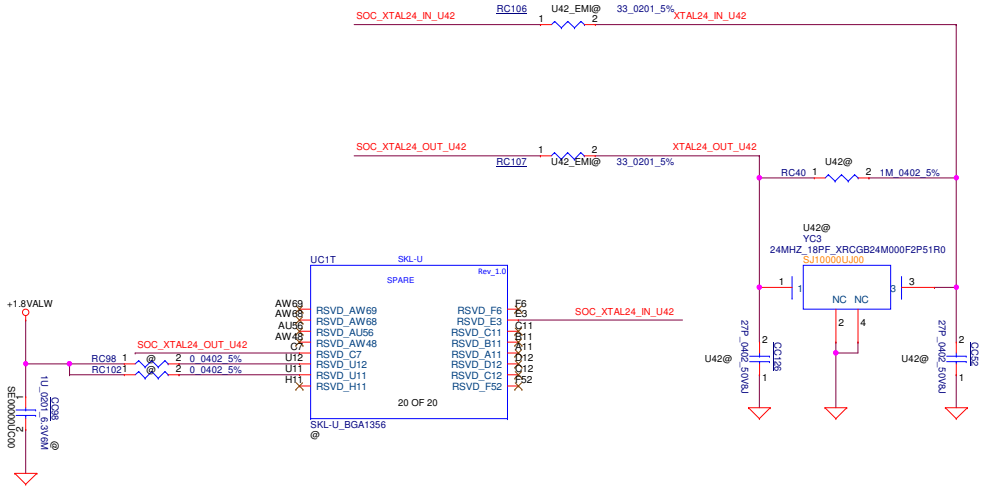
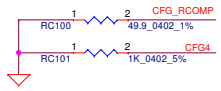




Follow 544669_SKL_U_DDR3L_RVP7_schematic_rev1.0

Stuff 100k(RC99) for CannonLake-U

Un-stuff 100k(RC99) for SkyLake-U



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.		
Title: SKL-U(12/12)CFG,RSVD		
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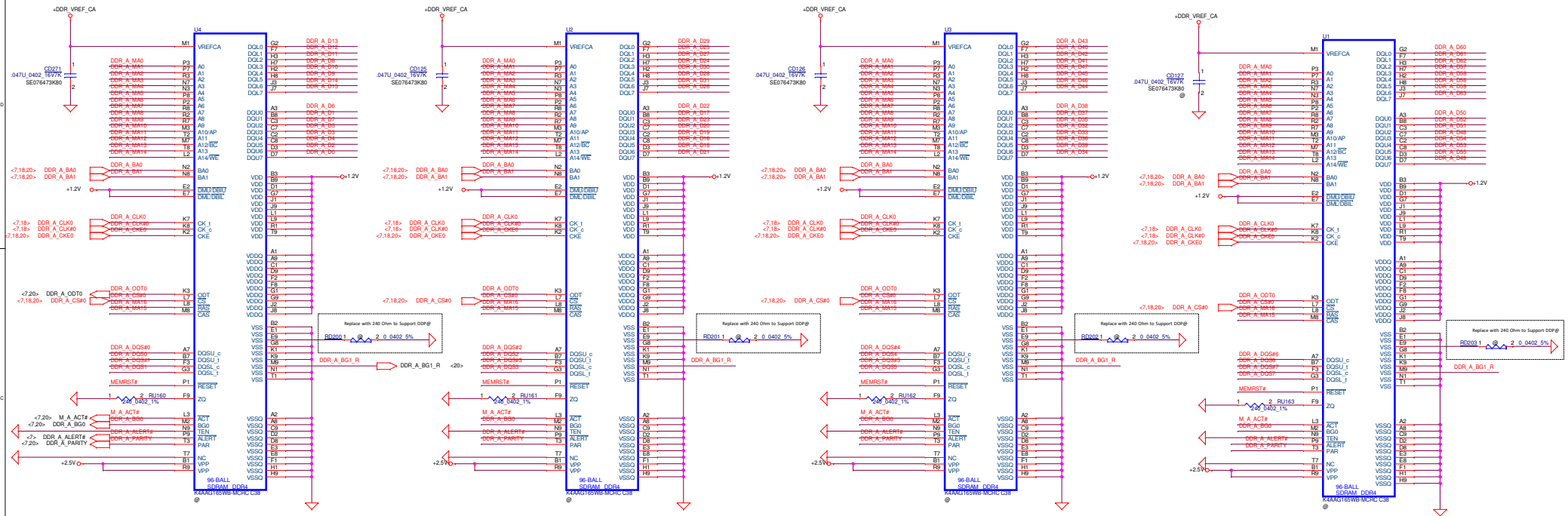
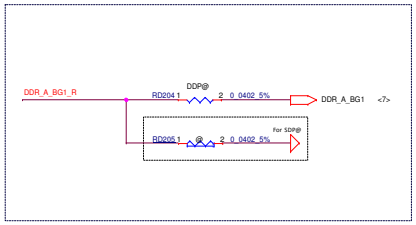
Interleaved Memory



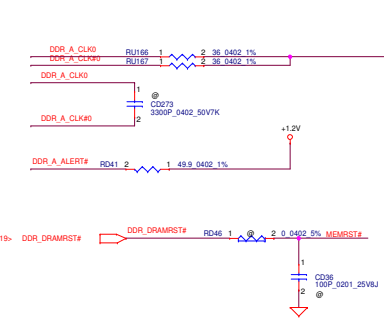
Co-lay for SDP / DDP Memory DIE

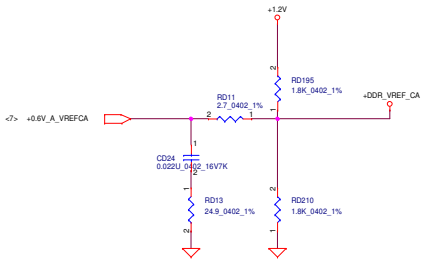


On Board RAM - Data Mapping

U4	DQ	U2	DQ	U3	DQ	U1	DQ
DQL0	D13	DQL0	D29	DQL0	D43	DQL0	D60
DQL1	D12	DQL1	D25	DQL1	D40	DQL1	D61
DQL2	D11	DQL2	D27	DQL2	D42	DQL2	D62
DQL3	D8	DQL3	D24	DQL3	D41	DQL3	D57
DQL4	D10	DQL4	D30	DQL4	D47	DQL4	D58
DQL5	D9	DQL5	D28	DQL5	D45	DQL5	D56
DQL6	D14	DQL6	D31	DQL6	D46	DQL6	D59
DQL7	D15	DQL7	D26	DQL7	D44	DQL7	D63
DQU0	D6	DQU0	D22	DQU0	D38	DQU0	D50
DQU1	D1	DQU1	D17	DQU1	D37	DQU1	D52
DQU2	D7	DQU2	D23	DQU2	D35	DQU2	D51
DQU3	D5	DQU3	D20	DQU3	D32	DQU3	D48
DQU4	D3	DQU4	D19	DQU4	D33	DQU4	D54
DQU5	D4	DQU5	D16	DQU5	D36	DQU5	D53
DQU6	D2	DQU6	D18	DQU6	D39	DQU6	D55
DQU7	D0	DQU7	D21	DQU7	D34	DQU7	D49

CLOCK TERMINATION





Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Title	DDR4 ON BOARD CHIPS		
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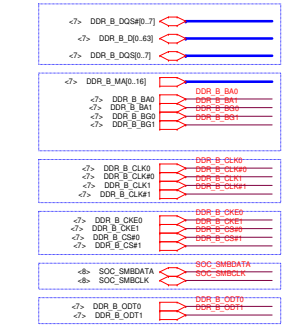
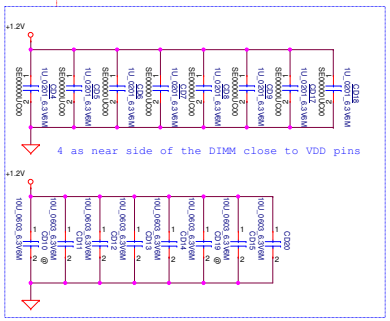
Reverse Type

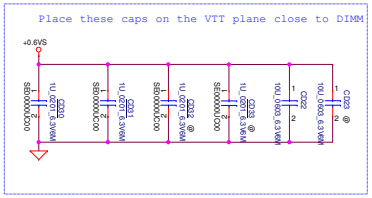
2-3A to 1 DIMMs/channel

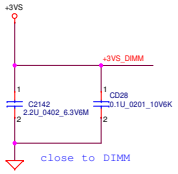


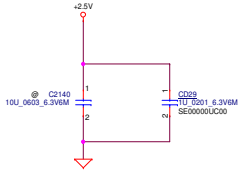
Layout Note:
Place near JDIMM1

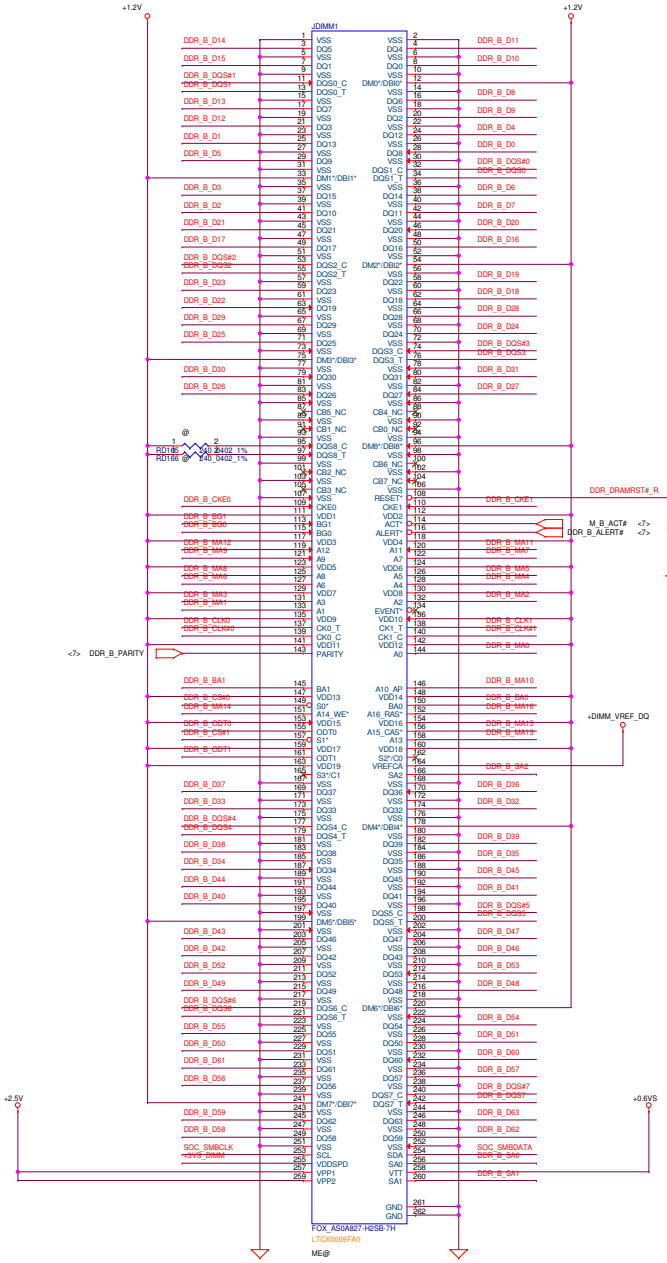
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

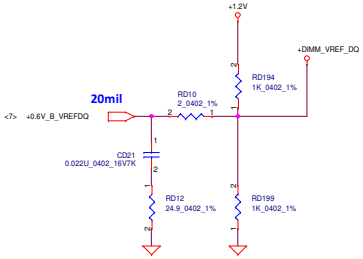


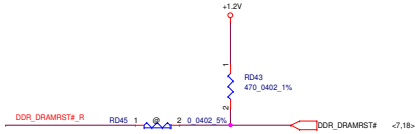




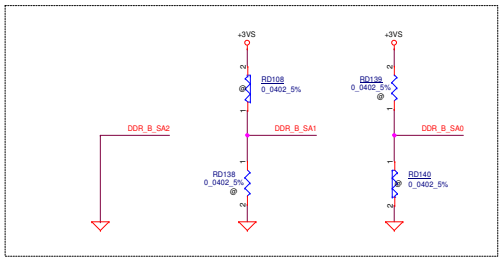








JDIMM1 ADDRESS (PLACE CLOSE TO DIMM)



Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: **DDR4 DIMM**

Size	Document Number	Rev
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<7,18> DDR_A_MA[0..16]

+1.2V

4 as near each on board RAM device as possible

CU89 220U_6.3V_M @

+2.5V

2 as near each on board RAM device as possible

+0.6VS

2 as near each on board RAM device as possible

+0.6VS

RP17 DDR_A_MA9 DDR_A_MA2 DDR_A_MA4 DDR_A_BA1 — <7,18> DDR_A_BA1 — 36_0804_8P4R_5%

RP18 DDR_A_MA10 DDR_A_MA3 DDR_A_MA12 DDR_A_BG0 — <7,18> DDR_A_BG0 — 36_0804_8P4R_5%

RP19 DDR_A_MA16 M_A_ACT# DDR_A_CS#0 DDR_A_MA15 — <7,18> M_A_ACT# <7,18> DDR_A_CS#0 — 36_0804_8P4R_5%

<18> DDR_A_BG1_R — DDR_A_BG1_R 1 DDR@ 2 RD211 36_0402_1%

RP20 DDR_A_CKE0 DDR_A_ODT0 DDR_A_MA14 — <7,18> DDR_A_CKE0 <7,18> DDR_A_ODT0 — 36_0804_8P4R_5%

RP21 DDR_A_MA13 DDR_A_MA8 DDR_A_PARITY DDR_A_MA11 — <7,18> DDR_A_PARITY — 36_0804_8P4R_5%

RP22 DDR_A_MA1 DDR_A_BA0 DDR_A_MA7 — <7,18> DDR_A_BA0 — 36_0804_8P4R_5%

RP24 DDR_A_MA5 DDR_A_MA6 DDR_A_MA0 — 36_0804_8P4R_5%

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Title	DDR4 MISC		
Size: Custom	Document Number: LA-D562P		Rev: 1.0
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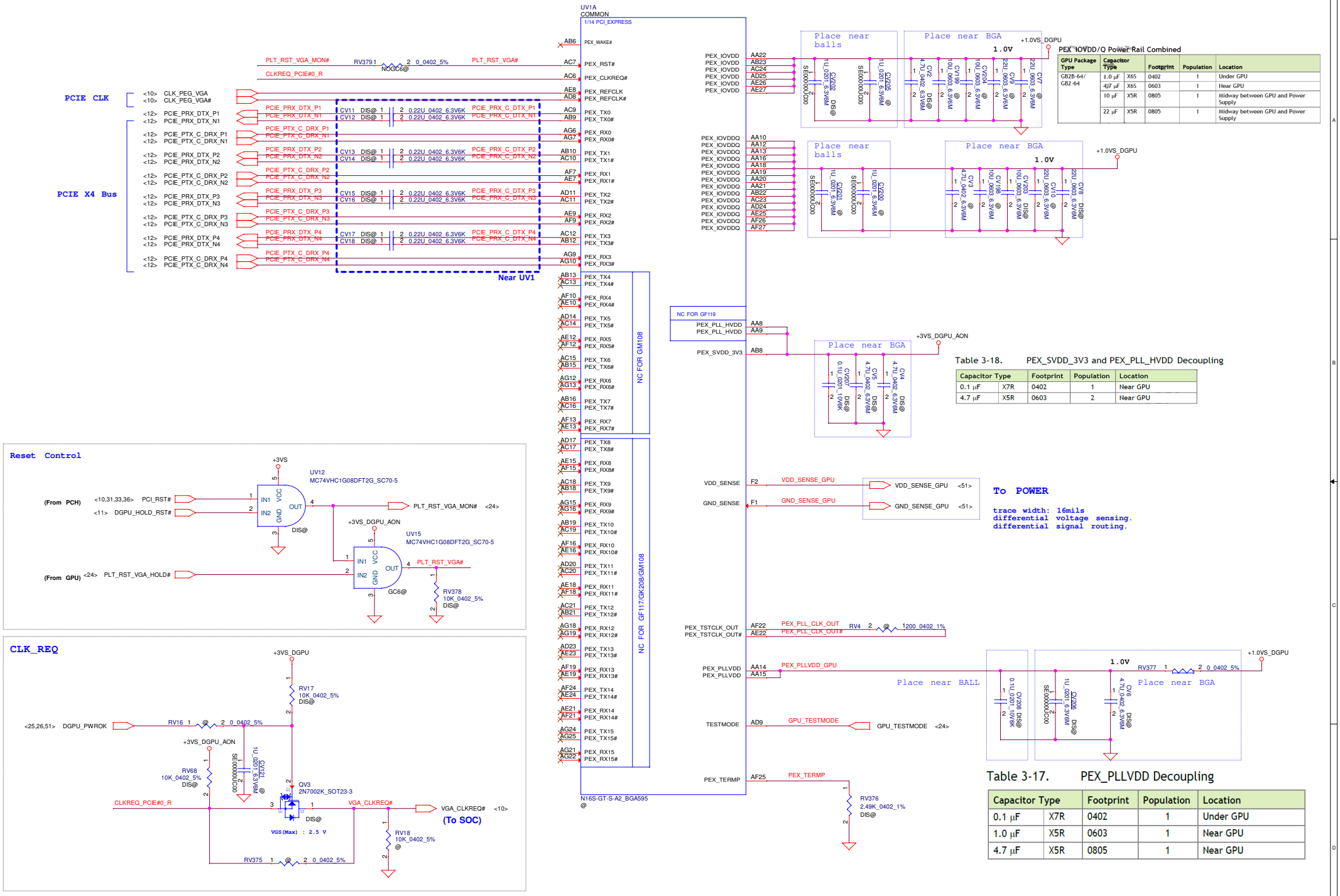

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64/ GB2-64	1.0 µF	X6S	0402	1	Under GPU
	4.7 µF	X6S	0603	1	Near GPU
	10 µF	X5R	0805	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	1	Midway between GPU and Power Supply

Capacitor Type	Footprint	Population	Location
0.1 µF	X7R	0402	1	Near GPU
4.7 µF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 µF	X7R	0402	1	Under GPU
1.0 µF	X5R	0603	1	Near GPU
4.7 µF	X5R	0805	1	Near GPU

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: **NV(1/5)-PCIE**

Size: | Document Number: **LA-G201P** | Rev: 1.0

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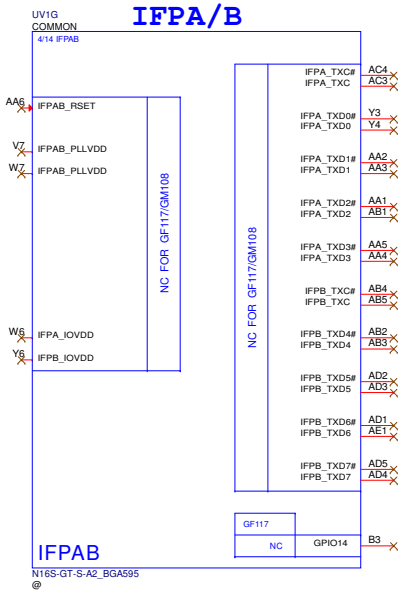
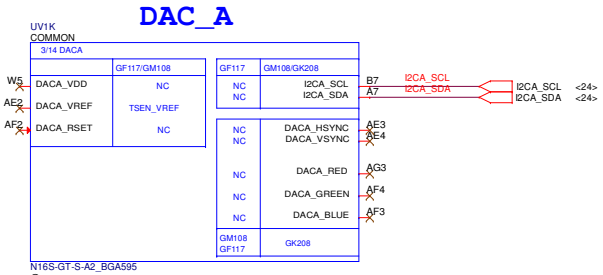
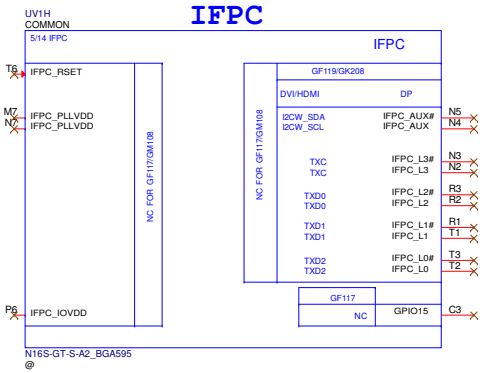
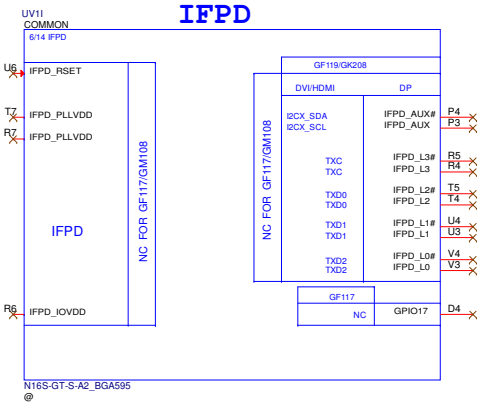
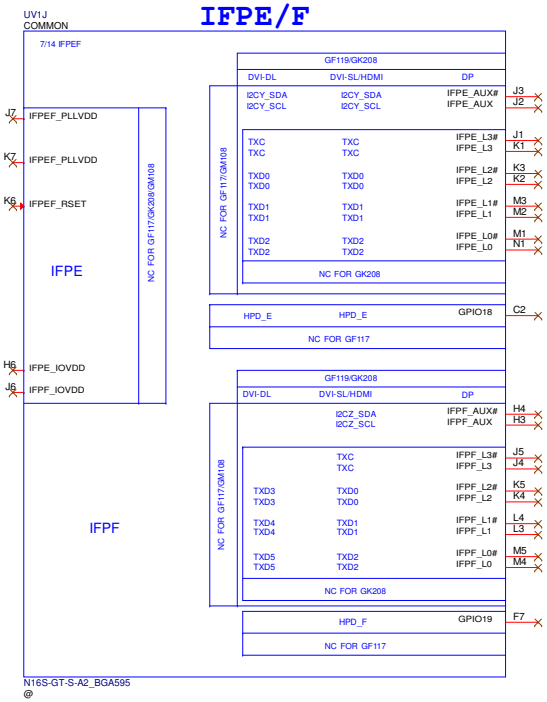
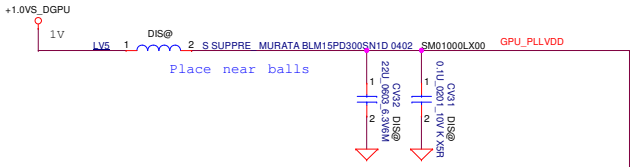












GPU Package	PLL Rail	Capacitor Type		Footprint	Population	Location
GB2-64, GB2B-64, GB4B-128	PLLVDD	0.1 µF	X7R	0402	1	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.05 Ω)		0402	1	Near GPU

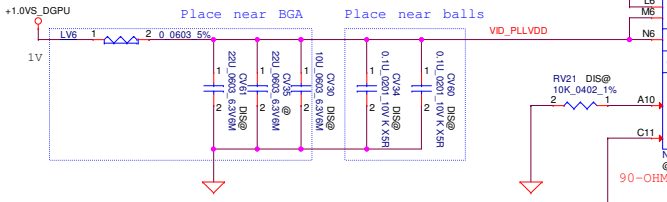
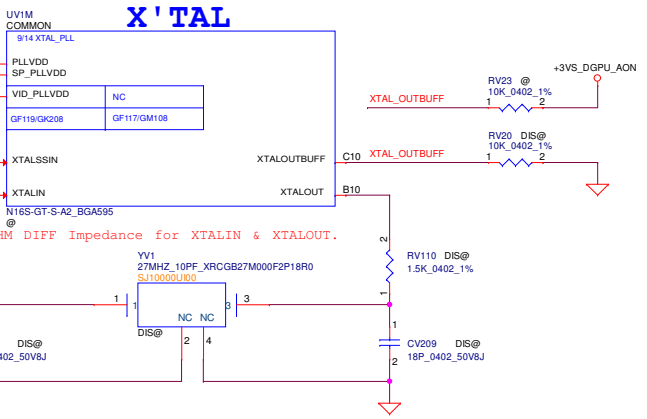


Table 3-33. SP_PLLVDD Power Rail Filtering [1]

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	SP_PLLVDD (+ VID_PLLVDD)[1]	0.1 µF	X7R	0402	1 per ball	Under GPU
		10 µF	X5R	0603	1	Near GPU
		47 µF	X5R	0805	1	Near GPU
		Bead Type				
		300 Ω (ESR=0.2 Ω)		0603	1	Near GPU

Note:
1. SP_PLLVDD and VID_PLLVDD power rails can be combined for customers who either do not use VGA display or uses VGA display with maximum resolution lower than 1024 x 768 with a 240 Hz refresh rate.



Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: NV(2/5)-IFP_ABCDEF_DAC_XTAL

Size	Document Number	Rev
	LA-G201P	1.0

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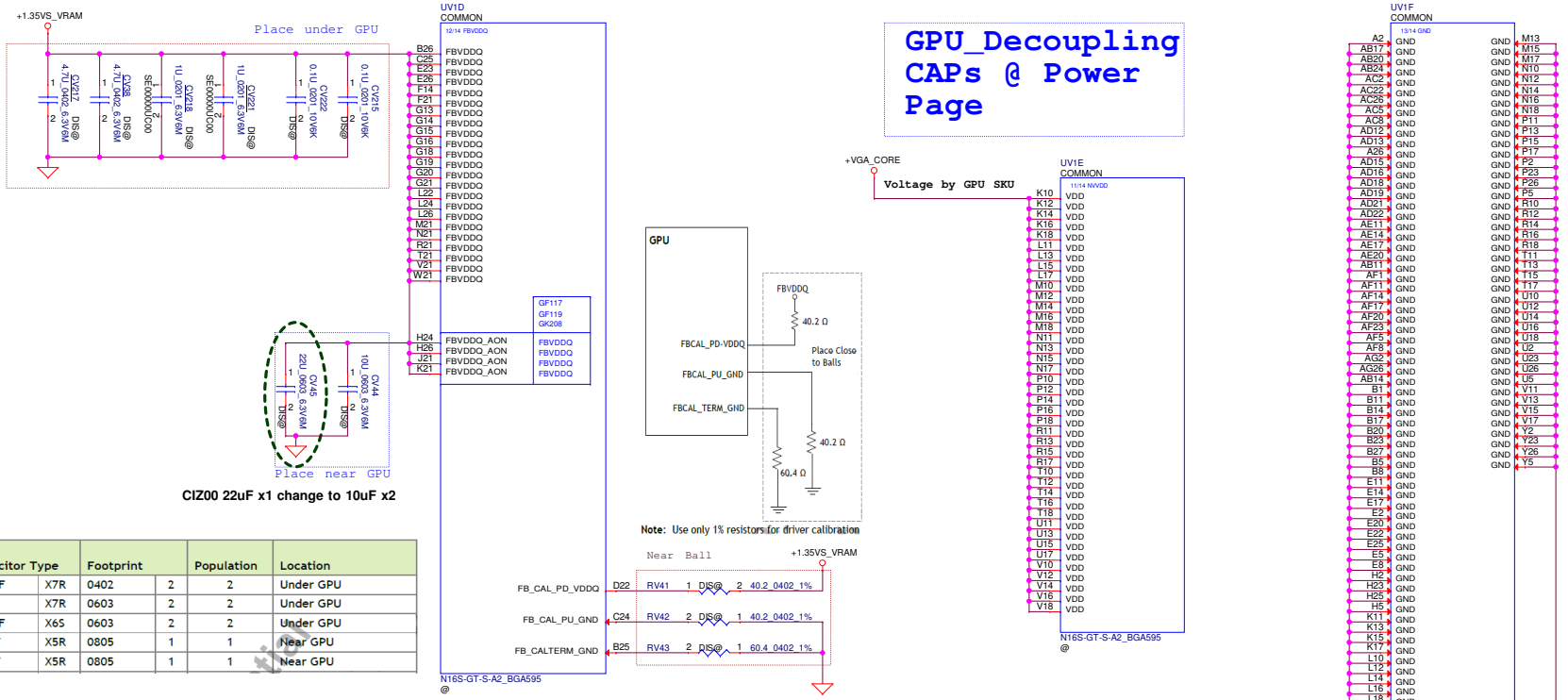
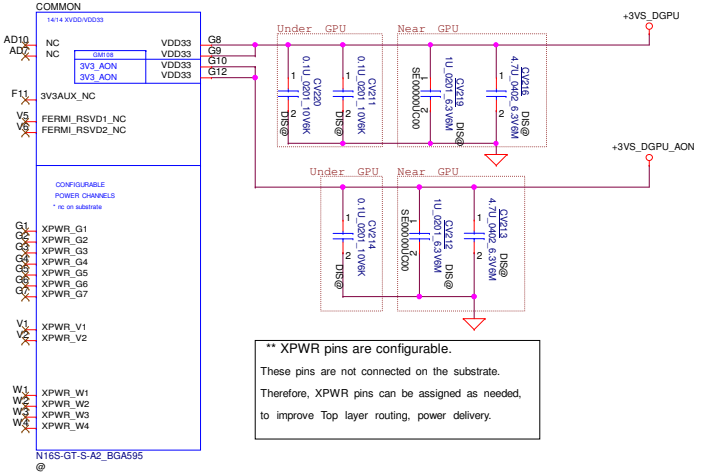
GPU_Decoupling CAPs @ Power Page



CIZ00 22uF x1 change to 10uF x2

GPU Package Type	Capacitor Type		Footprint		Population	Location
GB2B-64/ GB2-64 GDDR5	0.1 μF	X7R	0402	2	2	Under GPU
	1 μF	X7R	0603	2	2	Under GPU
	4.7 μF	X6S	0603	2	2	Under GPU
	10 μF	X5R	0805	1	1	Near GPU
	22 μF	X5R	0805	1	1	Near GPU



** XPWR pins are configurable.

These pins are not connected on the substrate.

Therefore, XPWR pins can be assigned as needed, to improve Top layer routing, power delivery.

GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2-64 GB2B-64 GB4B-128 GB3B-256	3V3_MAIN	0.1μF	X6S	0402	2	2	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU
GB2-64 GB2B-64 GB4B-128 GB3B-256	3V3_AON	0.1μF	X6S	0402	1	1	Under GPU
		1 μF	X5R	0603	1	1	Near GPU
		4.7 μF	X5R	0603	1	1	Near GPU

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

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Issued Date	2018/03/09	Deciphered Date	2019/03/09

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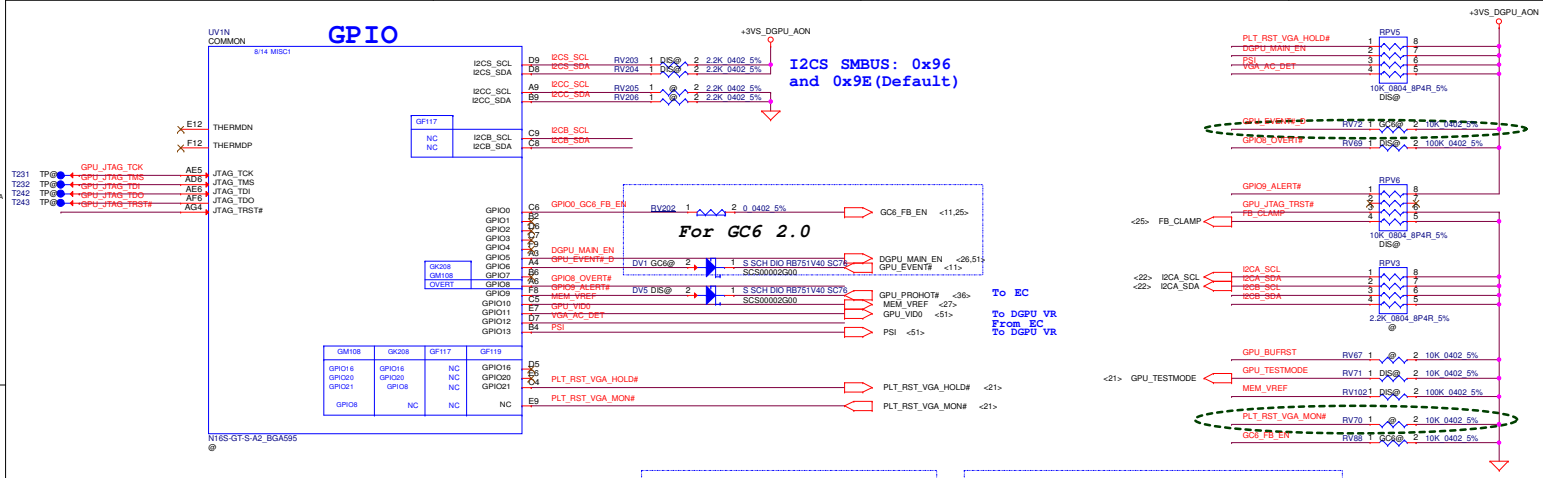
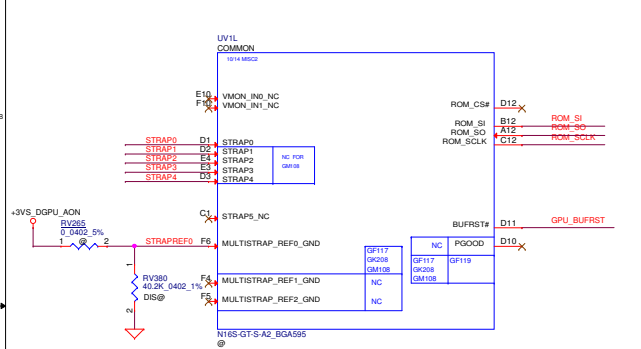
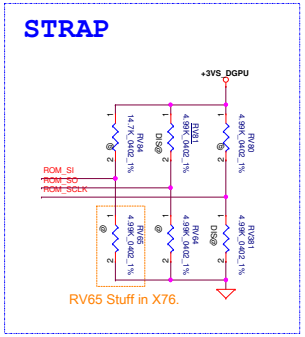
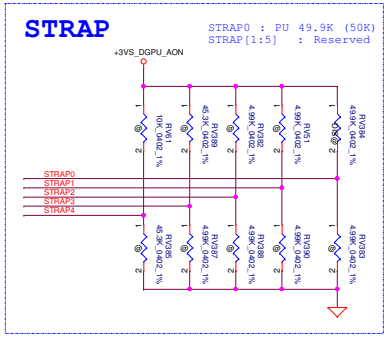


Table 12-2. GB2B-64 and GB4B-128 GPIO Description

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	GC6_FB_EN	O	FB Enable for GC6 2.0, Open Source	10 kΩ pull-down
GPIO1	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDDQ Boot voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100 kΩ pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	100 kΩ pull-down
GPIO4	LCD_BLEN	O	Panel Backlight Enable	100 kΩ pull-down
GPIO5	3V3_MAIN_EN	O	GPU power sequencing for GC6 2.0, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO6	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10 kΩ pull-up to 3V3_AON
GPIO7	3DVision	O	3D Vision L/R signal	100 kΩ pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset monitor	10 kΩ pull-up to 3V3_AON unless actively driven
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert, Open Drain	10 kΩ pull-up to 3V3_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100 kΩ pull-up to 3V3_AON
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AON to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	FRAME_LOCK#	I	Active Low Frame Lock, Open Drain	10 kΩ pull-up to 3V3_AON; Not available for GB2B-64
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control, Open Drain	10 kΩ pull-up to 3V3_AON
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON



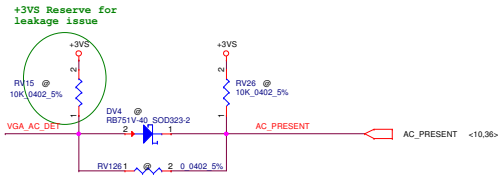




Item	N16P-GT	N16S-GT-B/S
Device ID	0X139A	0x1347
Package	GB4B-128	GB4B-128/GB2B-64
Internal P/N	GM107-750,28nm	GM108-755/655,28nm
ROM_SI	Refer to N16x_RAM_Straps table	Refer to N16x_RAM_Straps table
ROM_SO	0x0000, 4.99Kohm pull down	0x0000, 4.99Kohm pull down
ROM_SCLK	0x0 for Optimus, 4.99Kohm pull down	0x0 for Optimus, 4.99Kohm pull down
Strap0	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)	Reserved (Keep pull-up 3V3_AON and pull-down footprints and stuff 49.9kΩ pull-up)
Strap1	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)	Reserved (Keep pull-up and pull-down footprints and leave them no stuffed by default)
Strap2		
Strap3		
Strap4		
Open_VRG SKU	B	B
NVVDD Boot Voltage	0.9V	0.9V

Table 13. N16V-GMR1 and N16S-LG/-GMR/-GTR GDDR5 Recommended Memories

Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
	Samsung	K4G80325FB-HC28	B-die	0x0	3000	N/A	Substitution allowed with waiver²
	Samsung	K4G80325FB-HC25	B-die	0x0	3250	N/A	Substitution allowed with waiver²
	Hynix	H5GC8H24MJR-T2C	M-die	0x5	2500	N/A	Post production ready
	Hynix	H5GC8H24MJR-R0C	M-die	0x5	3000	N/A	Substitution allowed with waiver²
	Hynix	H5GQ8H24MJR-R4C	M-die	0x5	3000	N/A	Substitution allowed with waiver²
	Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
	Micron	MT51J256M32HF-70:A	A-die	0x1	3000	N/A	Substitution allowed with waiver²
	Micron	MT51J256M32HF-80:A	A-die	0x1	3000	N/A	Substitution allowed with waiver²



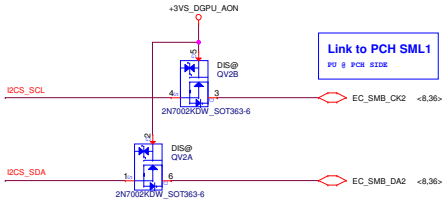
RAM_CFG	X76	CONFIG	ROM_SI		
0x0 4.99K(L)	X7677538L04	S2G@	RV65 4.99K +-1% 0402 SD034499180 S2G@	UV6 S2G_R1@ SA00009D10 / UV7 S2G_R1@ SA00009D10	K4G80325FB-HC28
				UV6 S2G_R3@ SA00009D30 / UV7 S2G_R3@ SA00009D30	K4G80325FB-HC28
0x1 10.0K(L)	X7677538L05	M2G@	RV65 10K +-1% 0402 SD034100280 M2G@	UV6 M2G_R1@ SA00009TV00 / UV7 M2G_R1@ SA00009TV00	MT51J256M32HF-70:A
				UV6 M2G_R3@ SA00009TV20 / UV7 M2G_R3@ SA00009TV20	MT51J256M32HF-70:A
0x5 30.1K(L)	X7677538L06	H2G@	RV65 30.1K +-1% 0402 SD034301280 H2G@	UV6 H2G_R1@ SA00009U100 / UV7 H2G_R1@ SA00009U100	H5GC8H24MJR-R0C
				UV6 H2G_R3@ SA00009U130 / UV7 H2G_R3@ SA00009U130	H5GC8H24MJR-R0C
0x6 34.8K(L)			RV65 34.8K +-1% 0402 SD034348280 @		RESERVED
0x7 45.3K(L)			RV65 45.3K +-1% 0402 SD034453280 @		RESERVED
0x4 24.9K(L)			RV65 24.9K +-1% 0402 SD034249280 @		RESERVED

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED 0	SOR2_EXPOSED 0	SOR1_EXPOSED 0	SOR0_EXPOSED 0
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL 0	PCIE_CFG 0	SMB_ALT_ADDR 0	VGA_DEVICE 0
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

RAM_CFG[3:0] (ROM_SI)	BAX40
0x0 4.99K(L)	S2G@
0x1 10.0K(L)	M2G@
0x2 15.0K(L)	
0x3 20.0K(L)	
0x4 24.9K(L)	
0x5 30.1K(L)	H2G@
0x6 34.8K(L)	
0x7 45.3K(L)	
0x8 4.99K(H)	
0x9 10.0K(H)	
0xA 15.0K(H)	
0xB 20.0K(H)	
0xC 24.9K(H)	
0xD 30.1K(H)	
0xE 34.8K(H)	
0xF 45.3K(H)	

Internal Thermal Sensor



10.2.1 Unconnected Signals (NC)

Do not route unused I²C signals on the PCB in order to protect the GPU from outside ESD risk. If unused traces are routed, the signals should be pulled down to ground with 1.8 kΩ resistors.

10.2.2 I²CS Slave Address

N16x GPUs use I²CS slave address 0x96h for NVIDIA internal testing. I²C address 0x96h must not be used by other I²C devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful I²CS Slave addresses can be used with SMB_ALT_ADDR strapping.

16.3.3 Internal Thermal Sensor Interface

The internal thermal sensor can be accessed through the I²CS interface as described in the I²C chapter. This interface is compliant with the System Management Bus (SMBus) Specification (Version 2.0). The interface supports PEC and SMBus Timeout as well as Read Byte and Read Byte with PEC. Writes to the internal thermal sensor registers through the I²CS interface by the system is not supported. The default port address to access the internal thermal sensor over the I²CS is 0x9E. Table 16-1 describes the byte-wise register accessible through the I²CS interface.

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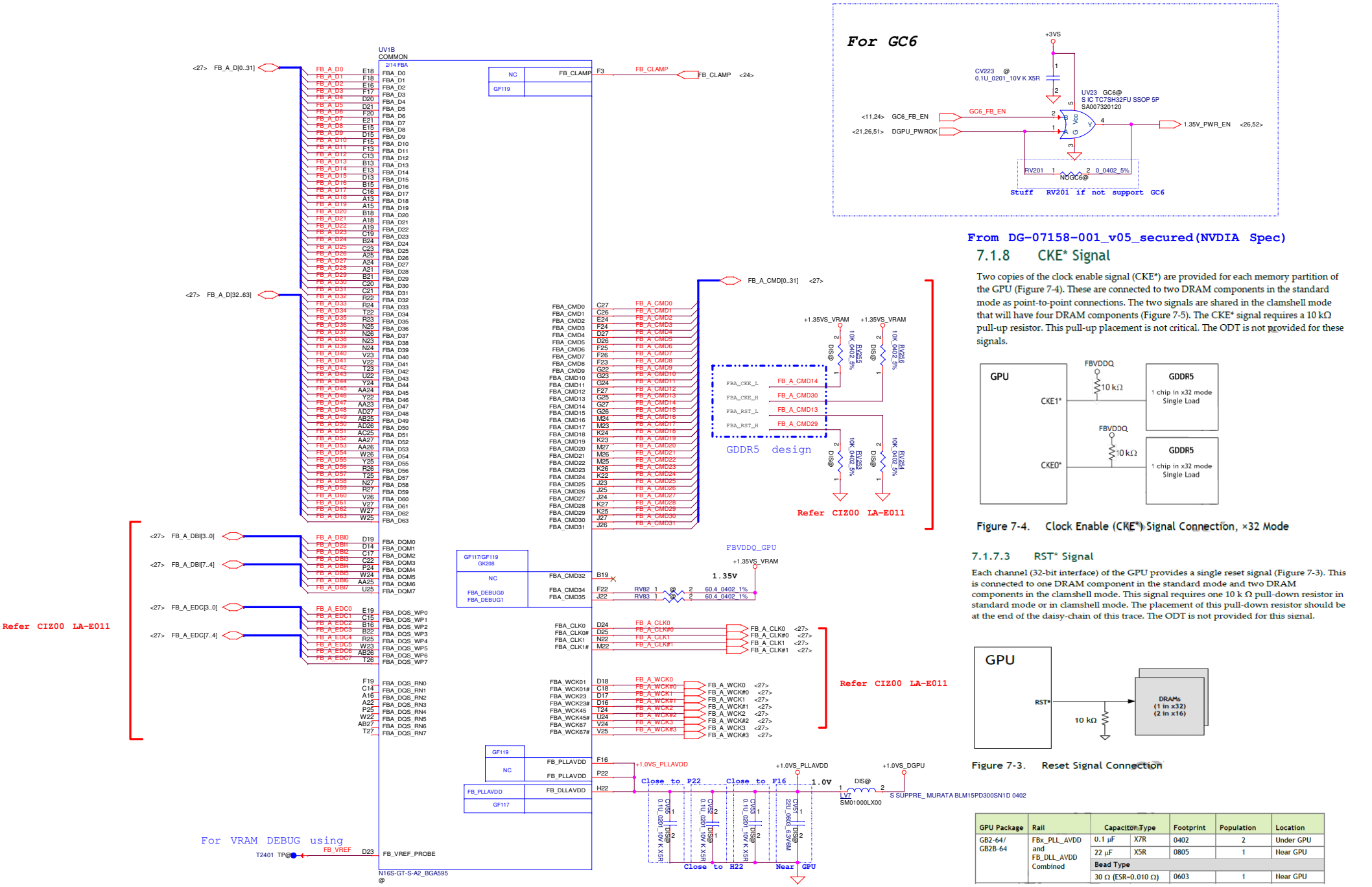

From DG-07158-001_v05_secured(NVDIA Spec)

7.1.8 CKE* Signal

Two copies of the clock enable signal (CKE*) are provided for each memory partition of the GPU (Figure 7-4). These are connected to two DRAM components in the standard mode as point-to-point connections. The two signals are shared in the clamshell mode that will have four DRAM components (Figure 7-5). The CKE* signal requires a 10 kΩ pull-up resistor. This pull-up placement is not critical. The ODT is not provided for these signals.

Figure 7-4. Clock Enable (CKE*) Signal Connection, ×32 Mode

7.1.7.3 RST* Signal

Each channel (32-bit interface) of the GPU provides a single reset signal (Figure 7-3). This is connected to one DRAM component in the standard mode and two DRAM components in the clamshell mode. This signal requires one 10 k Ω pull-down resistor in standard mode or in clamshell mode. The placement of this pull-down resistor should be at the end of the daisy-chain of this trace. The ODT is not provided for this signal.

Figure 7-3. Reset Signal Connection

GPU Package	Rail	Capacitor Type		Footprint	Population	Location
GB2-64/ GB2B-64	FBx_PLL_AVDD and FB_DLL_AVDD Combined	0.1 µF	X7R	0402	2	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

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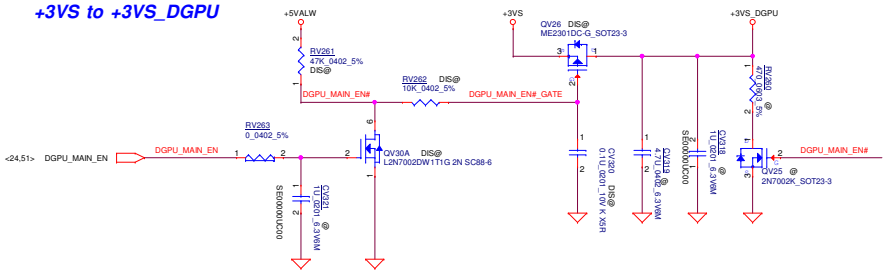
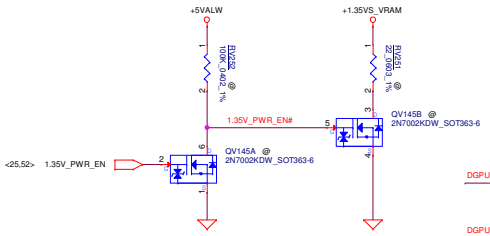
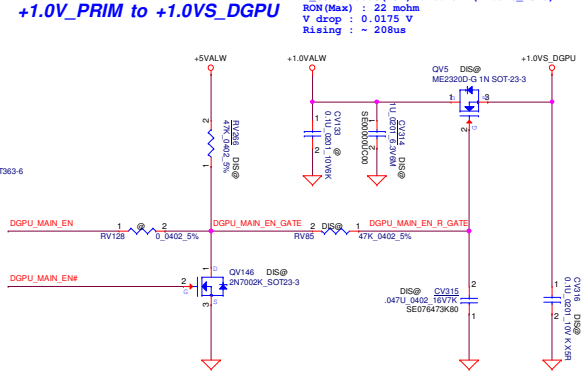
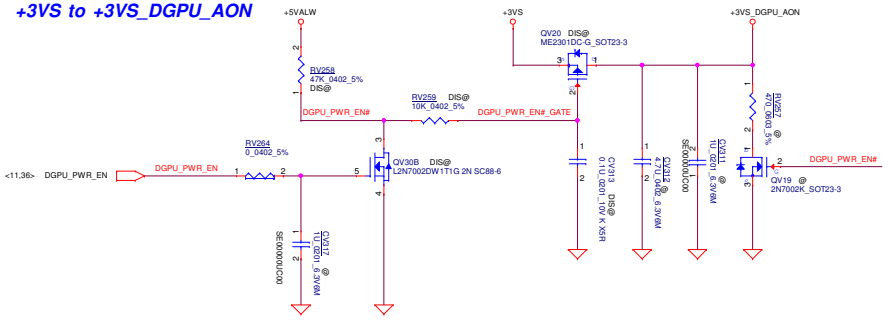
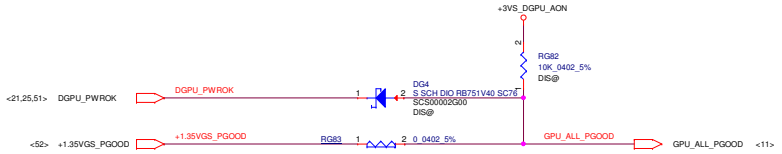










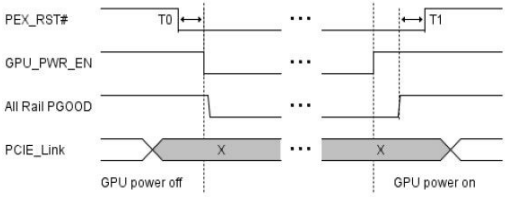
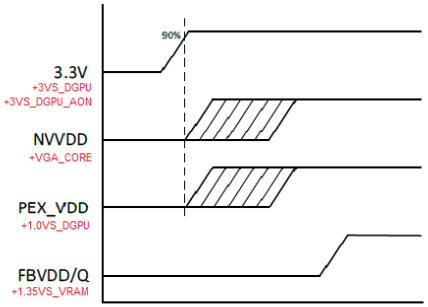


Figure 18-7. Optimus Entry/Exit Timing Diagram

Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

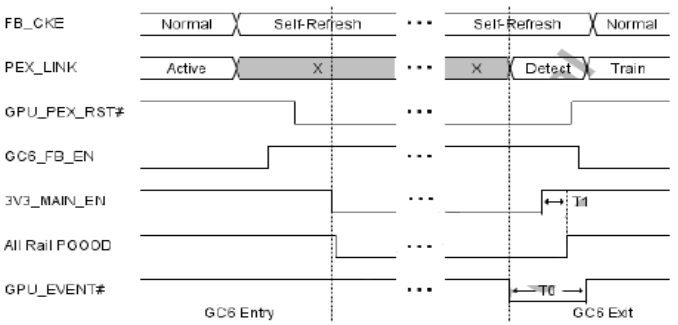


Note:
- 3.3V includes all rails powered at 3.3V; PEX_VDD includes all rails that are shared on 1.05V/1.0V
- The ramp time for any rail must be more than 40 µs and is recommended to be less than 2 ms.

Table 5. EDP-Continuous [3]

Products	VRAM Type	GPU Core	GPU FBIO		FB Total [1, 5]		1.05V Total [2]	3.3V Total
		–	1.5V [4]	1.35V [4]	1.5V [4]	1.35V [4]	1.05V [4]	3.3V [4]
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N16S-GMR	GDDR5	19.0	–	2.0	–	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N16S-GTR	GDDR5	26.5	–	2.0	–	4.2	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

Figure 18-12. GC6 2.0 Entry/Exit Sequence Timing Diagram



Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:
- ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in GC6 for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

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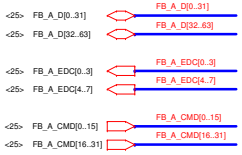
VRAM Memory Partition A

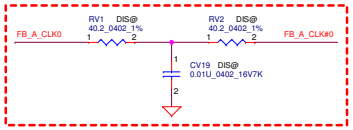
Table 7-4. GDDR5 Mode H Mapping

GB2-64, GB2B-64, GB4B-128	Channel 0 0..31	GB2-64, GB2B-64, GB4B-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*
GB2-64, GB2B-64, GB4B-128	Channel 0 & 1		
CMD32	Not used		
CMD33[1]	Not used		
CMD34	DEBUG0[2]		
CMD35	DEBUG1[2]		

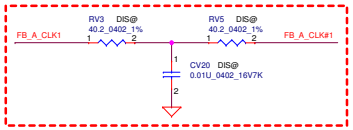
Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins not connected to VRAM, see section 7.1.13.

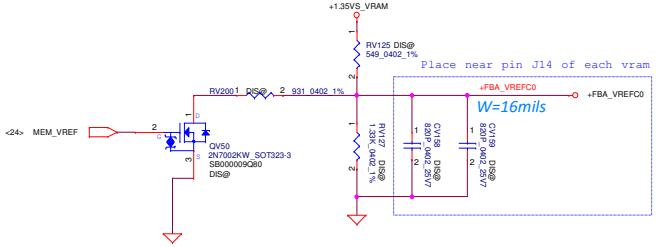


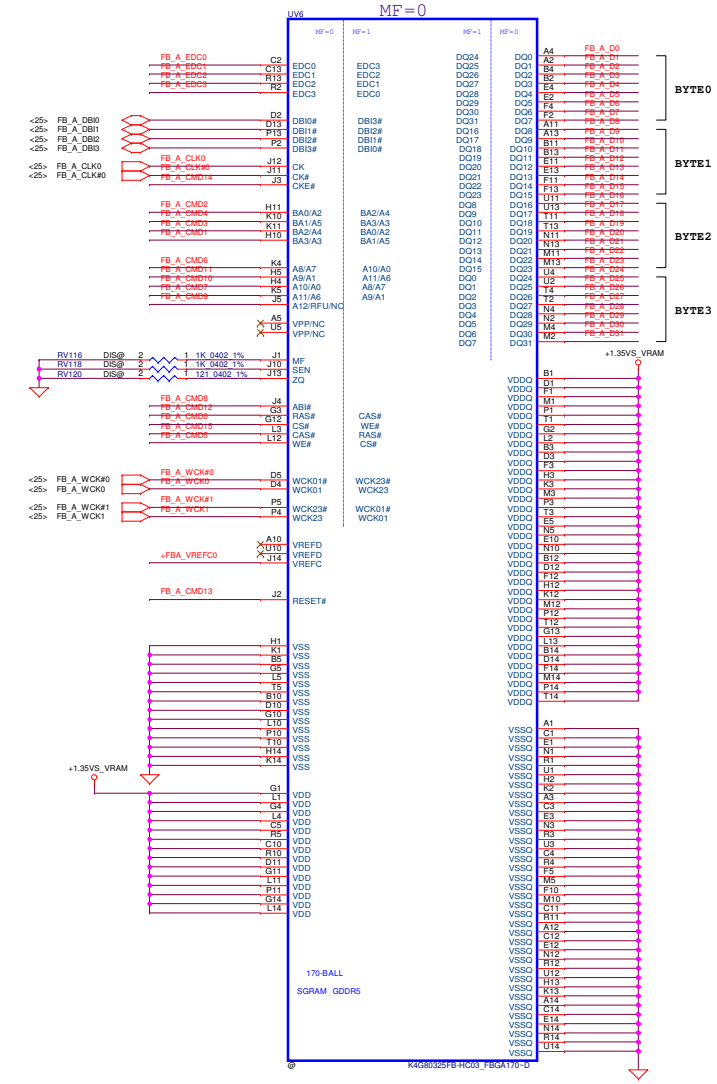
Near to UV6

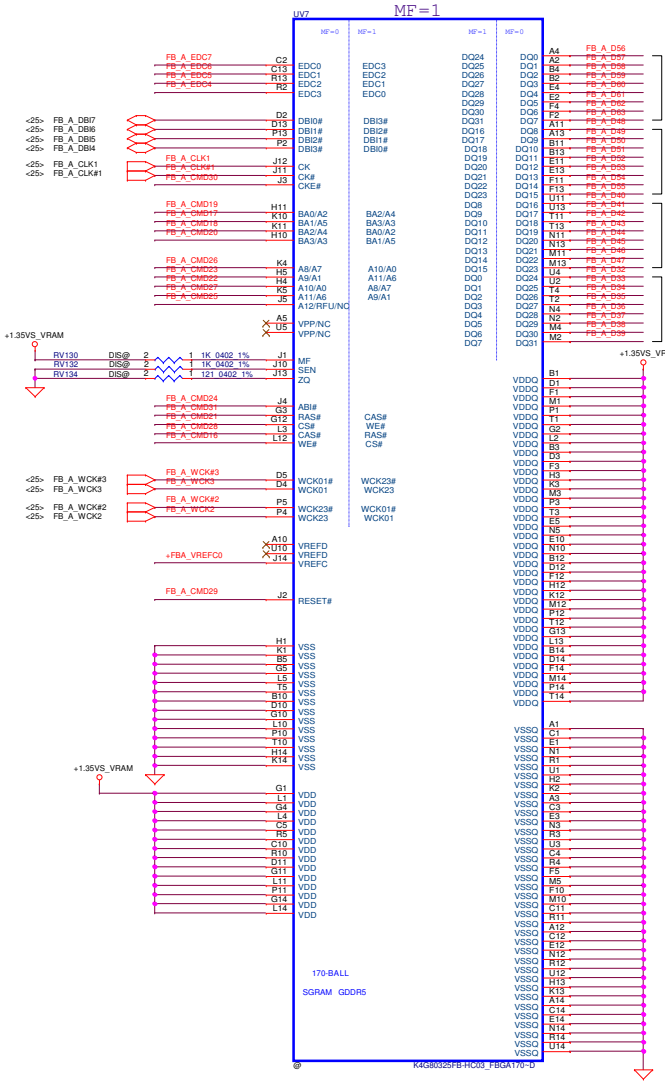


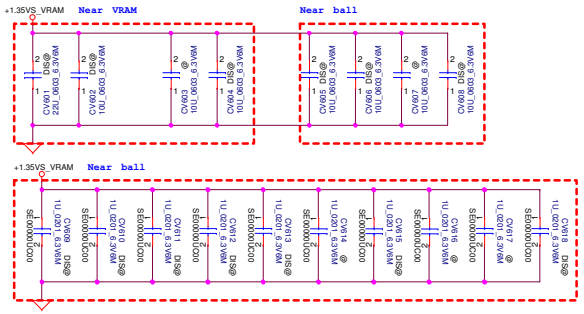
Near to UV7

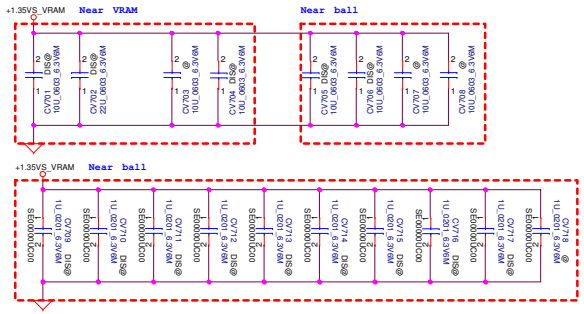












Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

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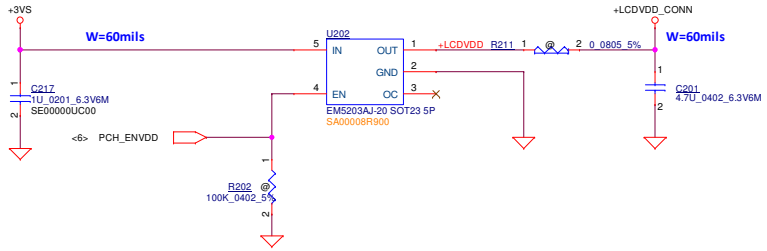
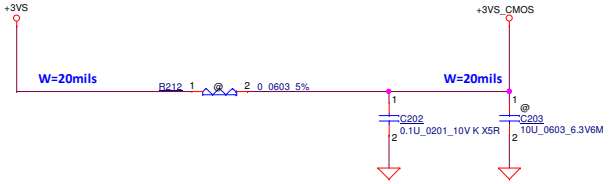
LCD POWER SWITCH



CAMERA POWER CIRCUIT



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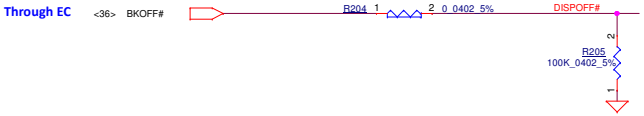
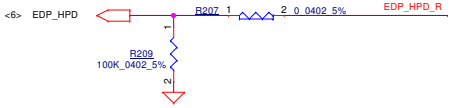
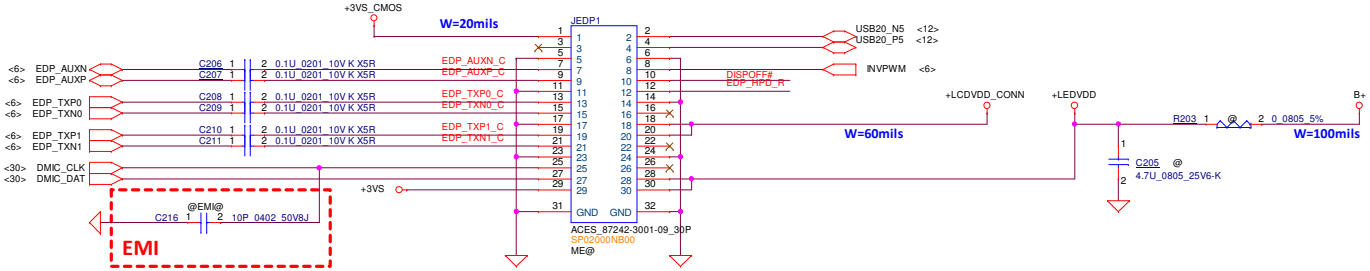


HOT PLUG DETECT



eDP CONNECTOR



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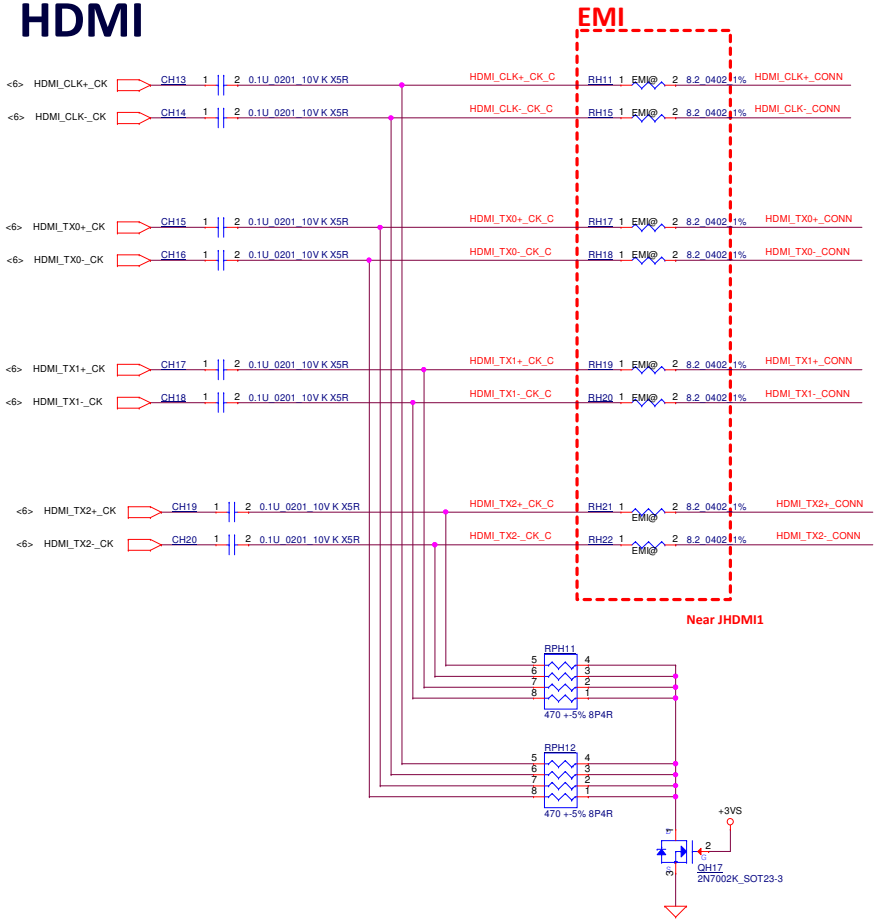
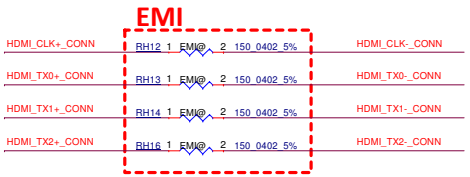
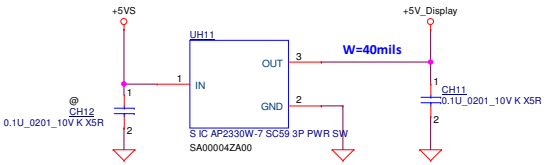
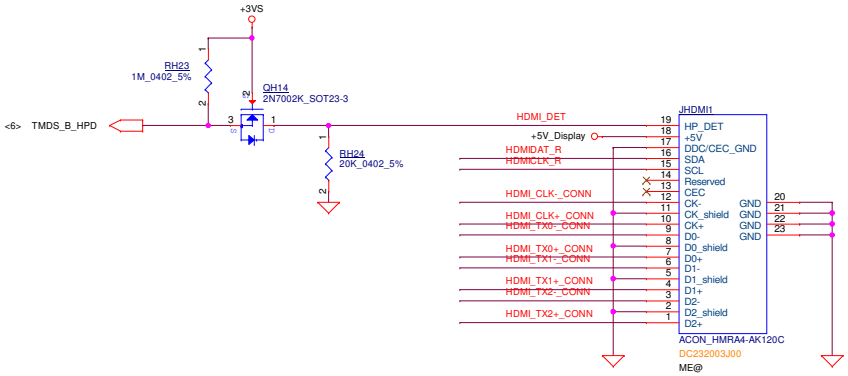
HDMI

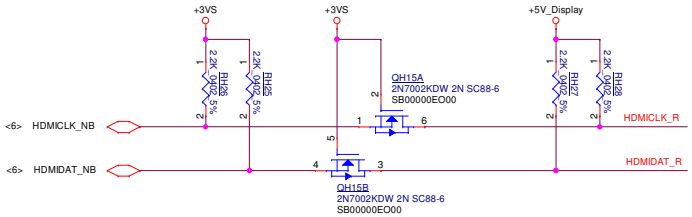


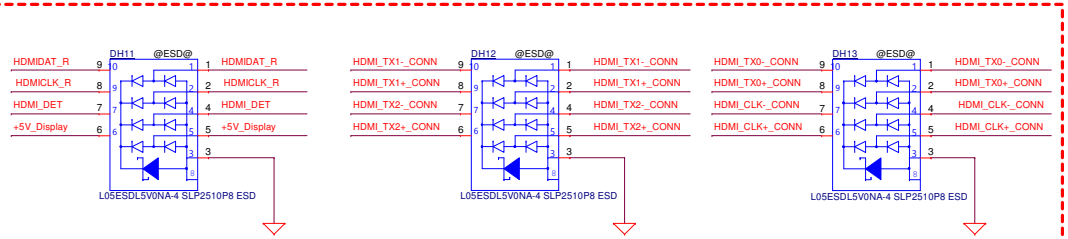


For HDMI









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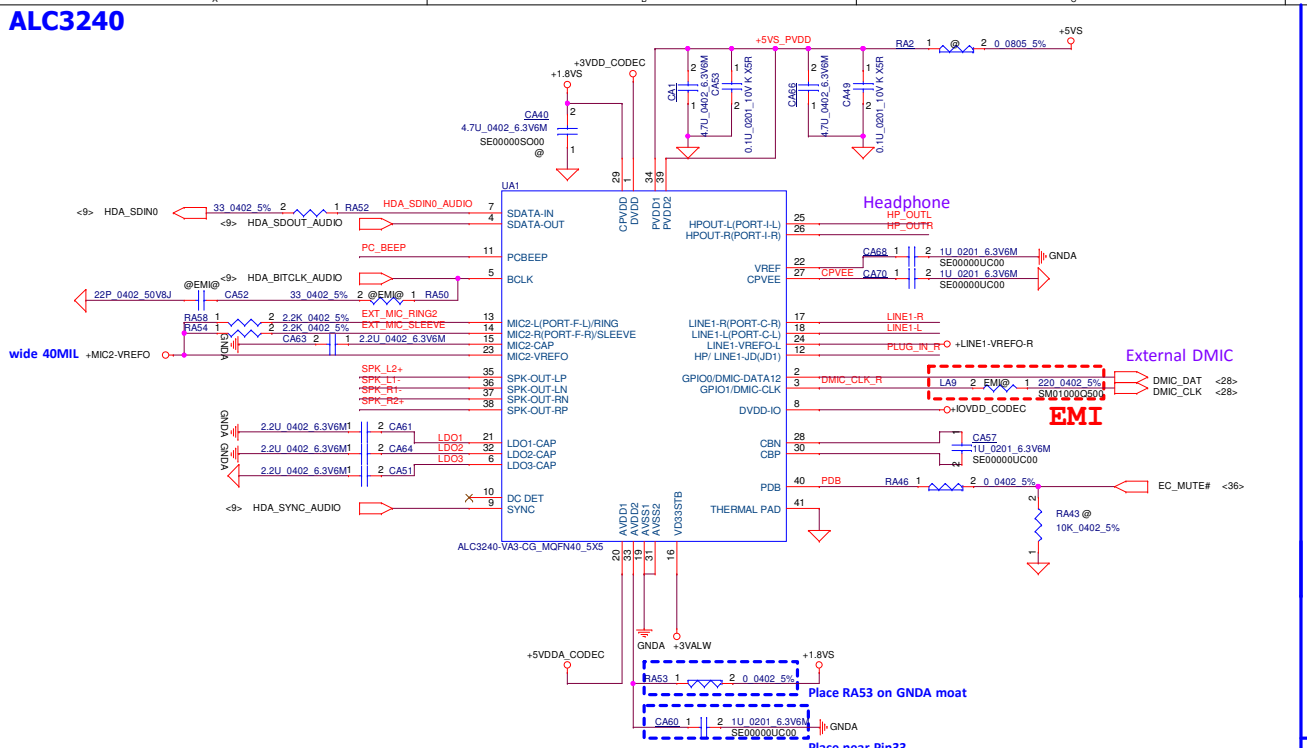
ALC3240



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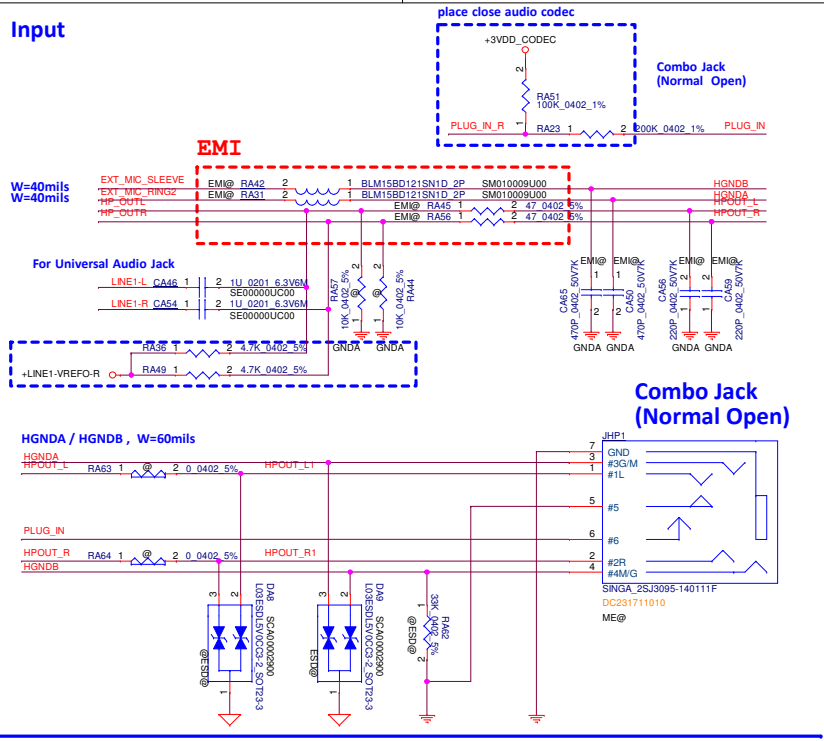

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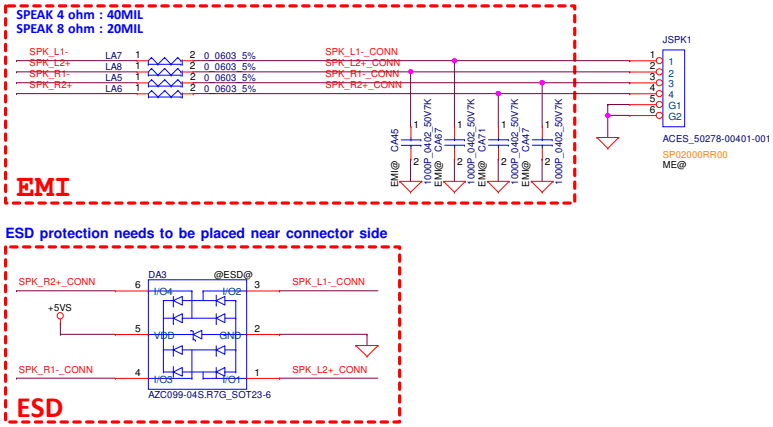
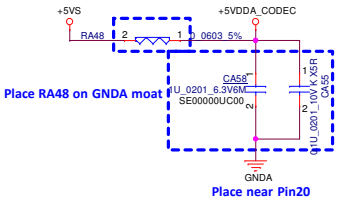


+5VS to +5VDDA_CODEC



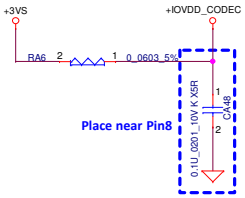
Each Platform Power Net Support List :

	+1.5VS	+1.8VS	+3VS	+5VS	+3VALW
	1.5V(S0)	1.8V(S0)	3.3V(S0)	5V(S0)	3.3V(S0~S5)
Intel Broadwell	V	X	V	V	V
Intel Skylake	X	V	V	V	V

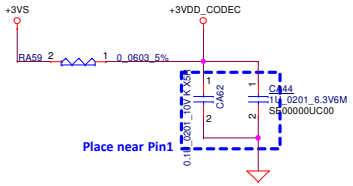
Each Platform HDA Link Voltage Support (Pin 8) :

	3.3V	1.5V
Intel Broadwell	V (default)	V
Intel Skylake	V (default)	V

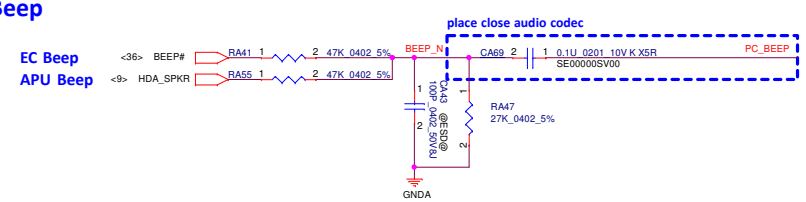
+3VS to +IOVDD_CODEC



+3VS to +3VDD_CODEC



PC Beep



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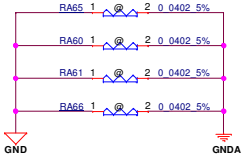

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Title	HD Audio Codec - ALC3240
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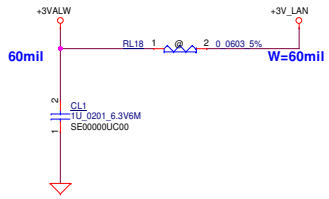
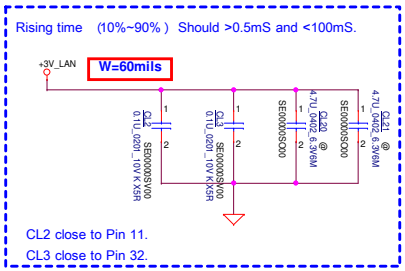
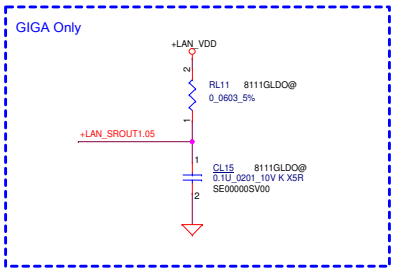
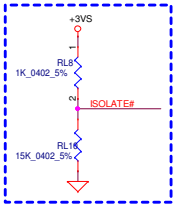
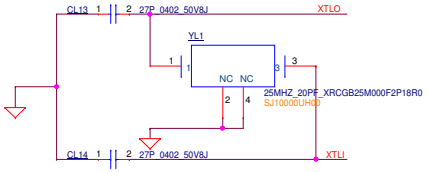
LAN

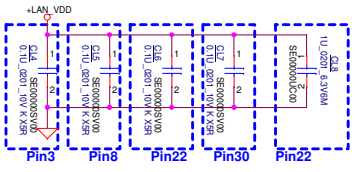




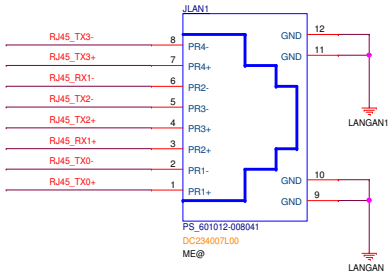


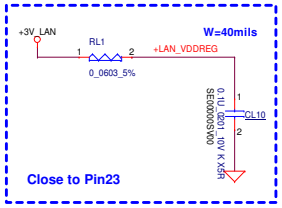


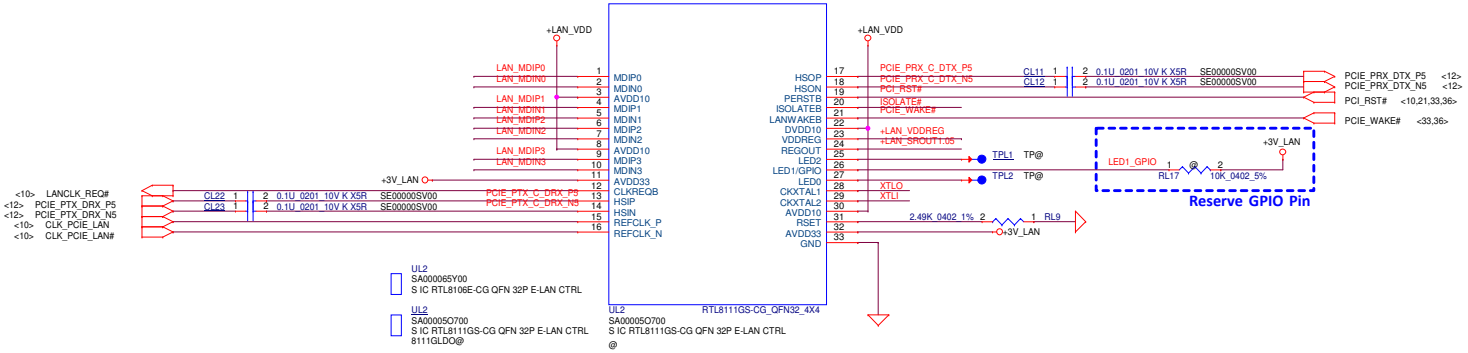




RJ-45 Connector







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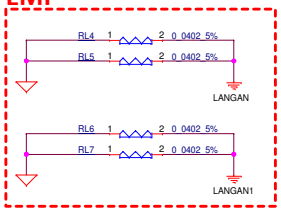

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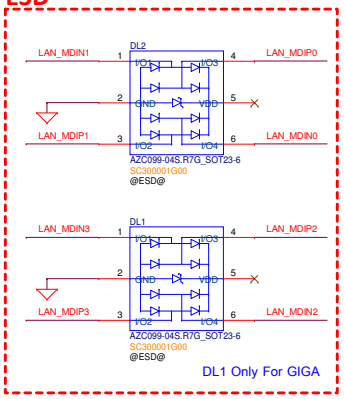

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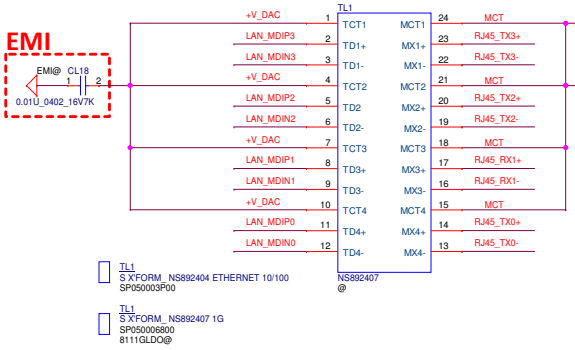

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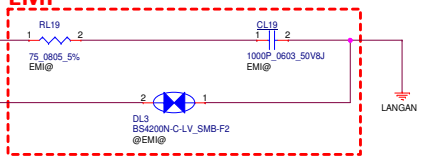

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Compal Electronics, Inc.

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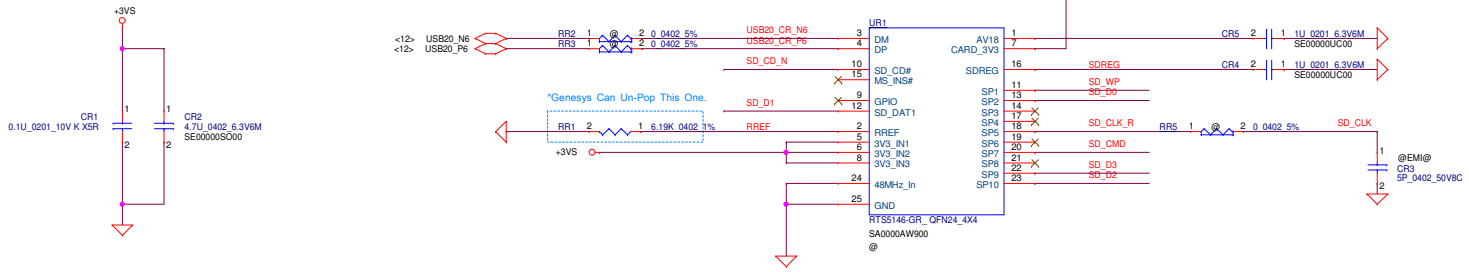
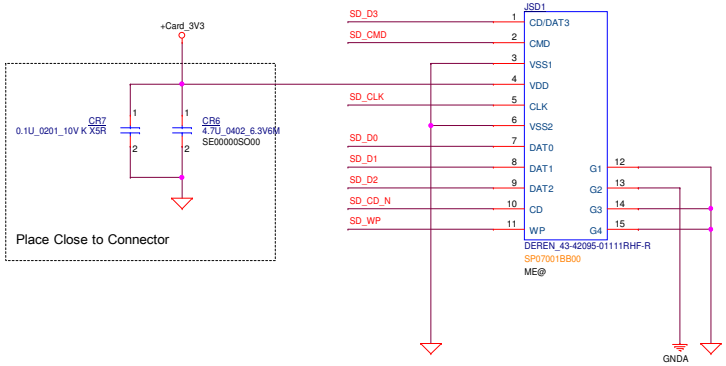
CARD READER

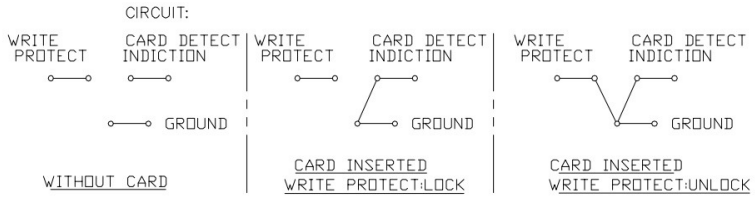
Card Reader IC

Main — UR1, S IC RTS5146-GR QFN 24P USB2.0 CARD READ, SA0000AW900

Second — UR1, S IC GL835-OGYL3 QFN 24P CARD READER, SA0000AVM10, GEN_CR@







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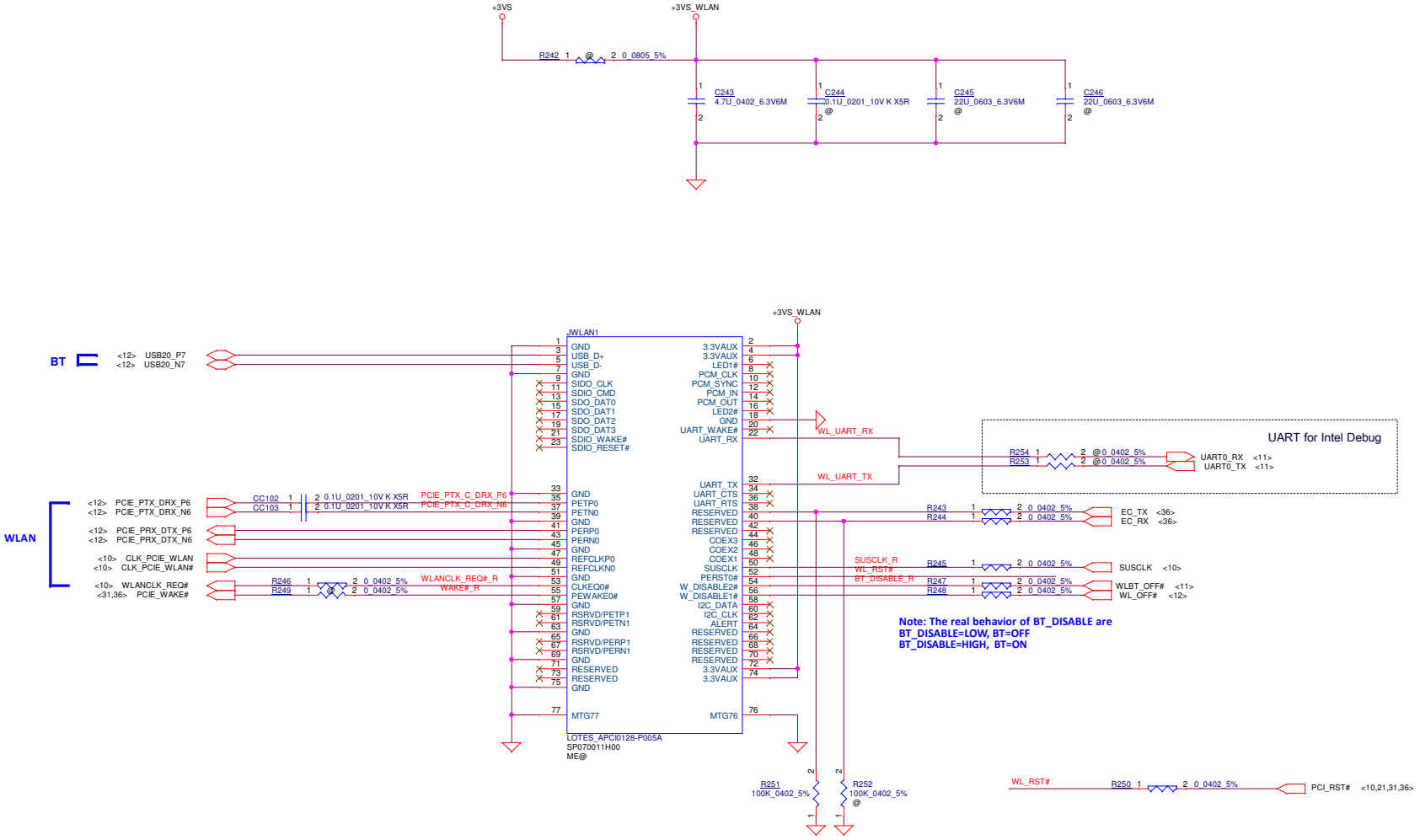
NGFF - WLAN / BT (E- KEY)



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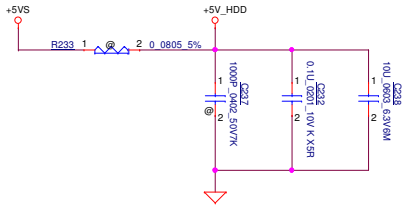
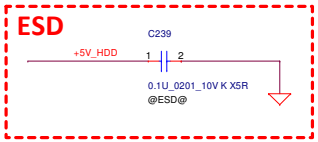
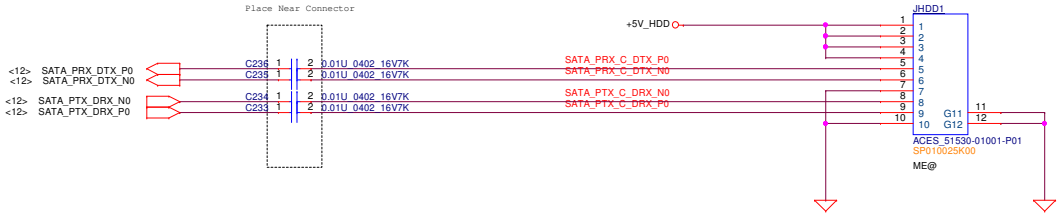
HDD FFC Connector to Sub Board







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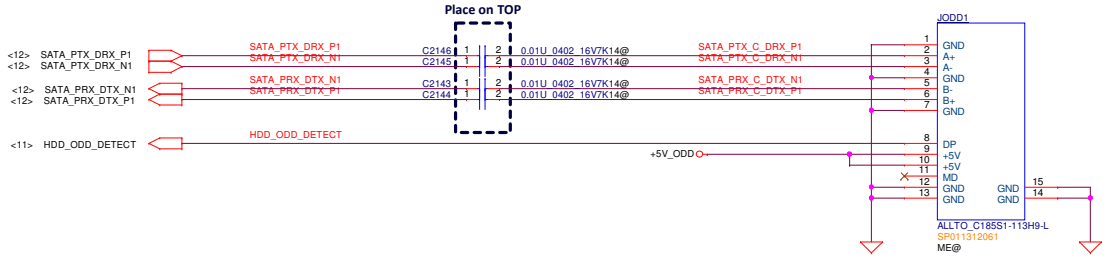
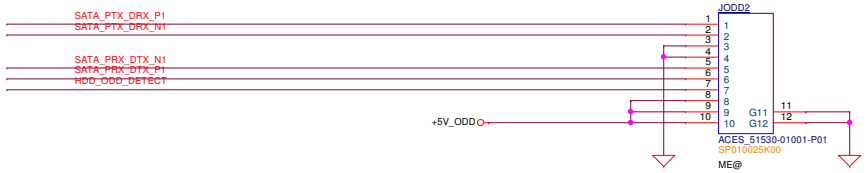
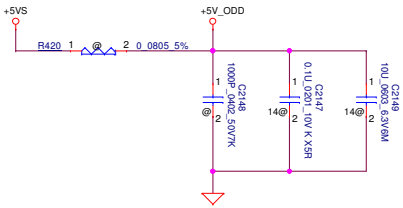
ODD Connector (14" Only)



ODD FFC Connector to Sub Board (15" Only)



ODD MISC.



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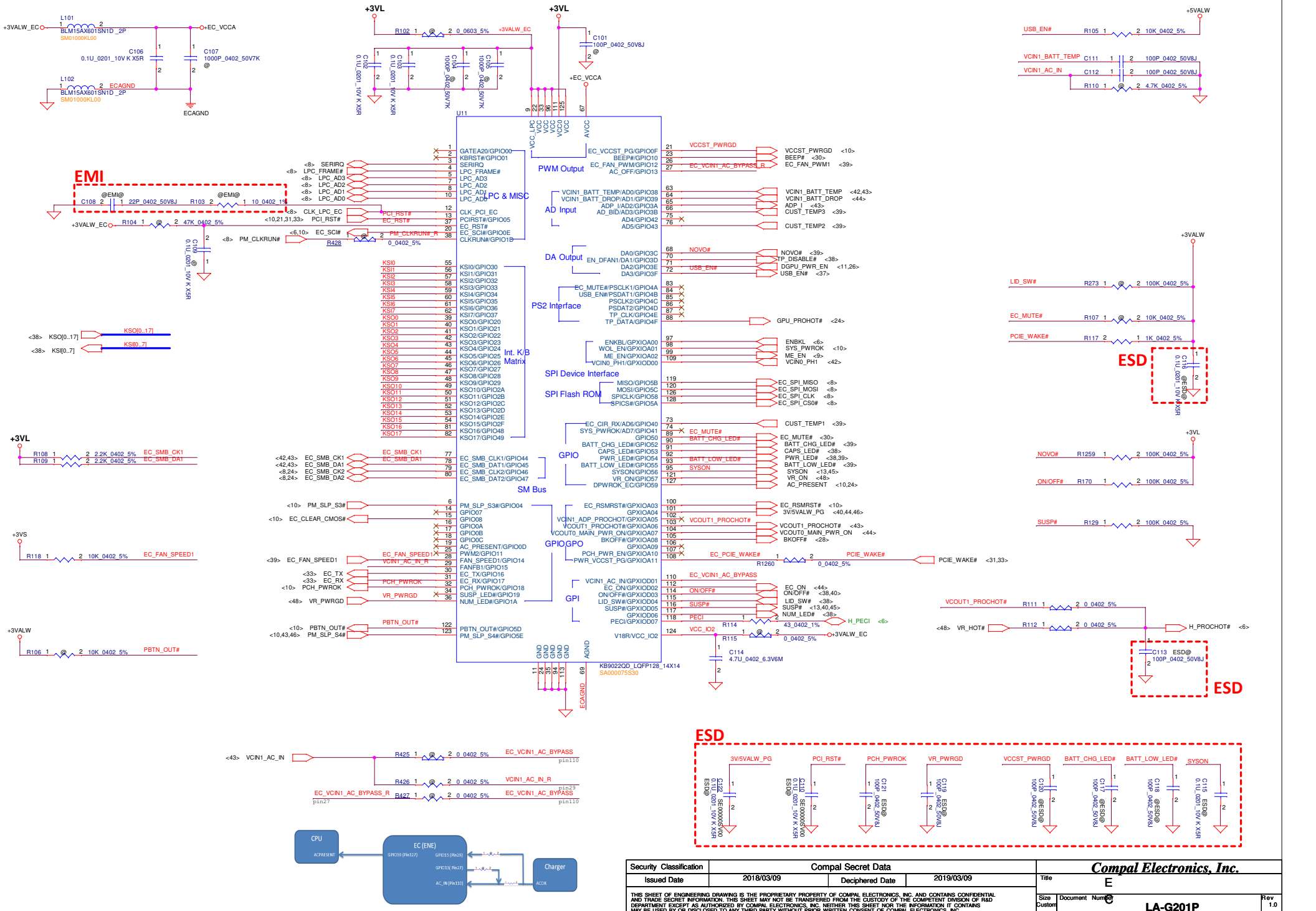

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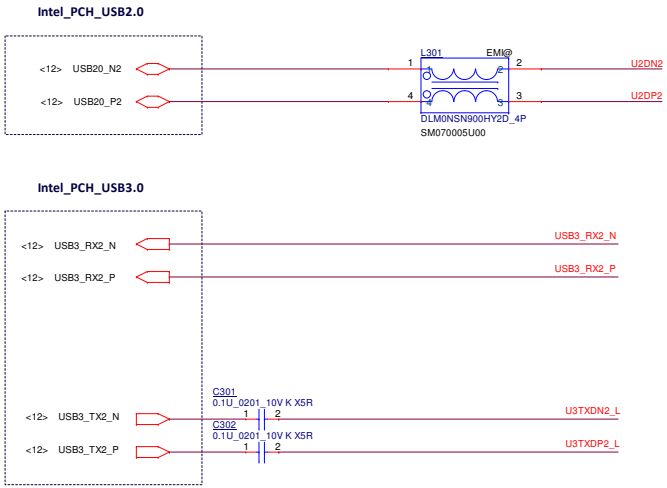
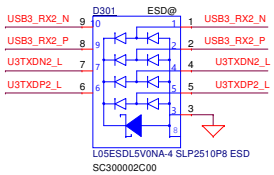
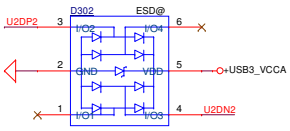
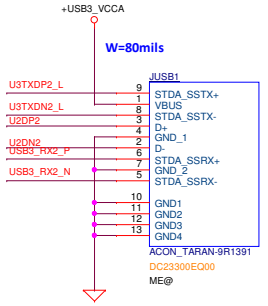
USB 3.0 (PORT 2)



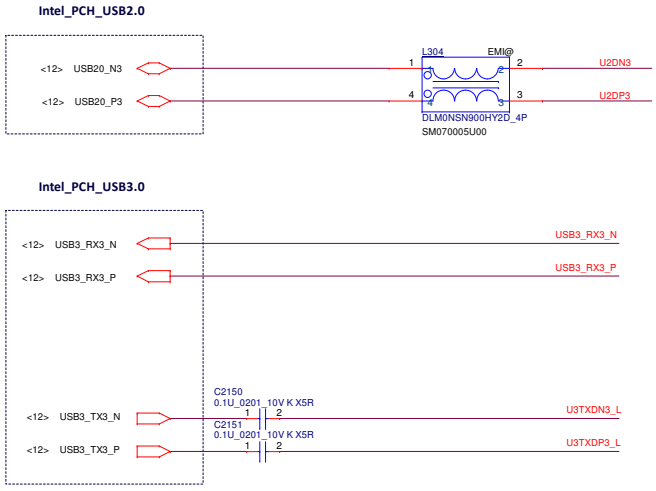
Place TX AC coupling Cap (C172,173). Close to connector



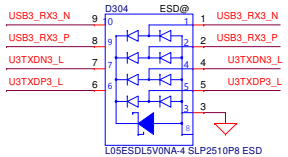


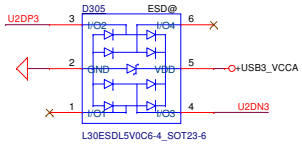


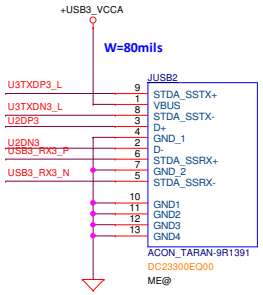
USB 3.0 (PORT 3)



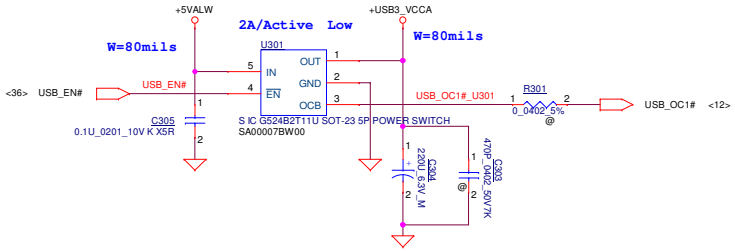
Place TX AC coupling Cap (C2150,2151). Close to connector







USB 3.0 MISC.



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Title	USB		
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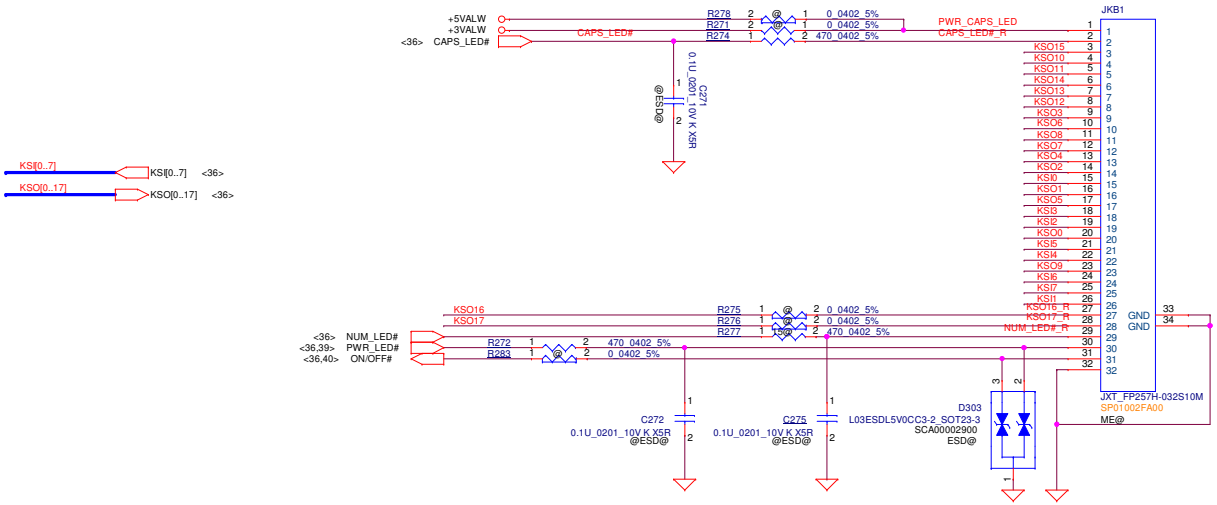
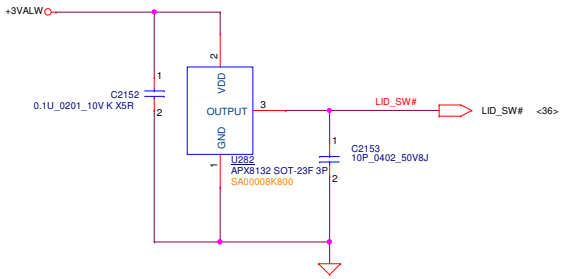
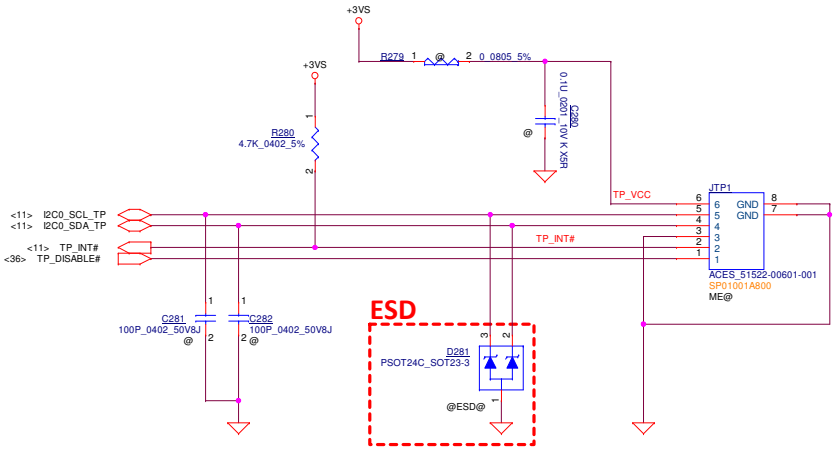
KEYBOARD



HALL SENSOR



TOUCH PAD



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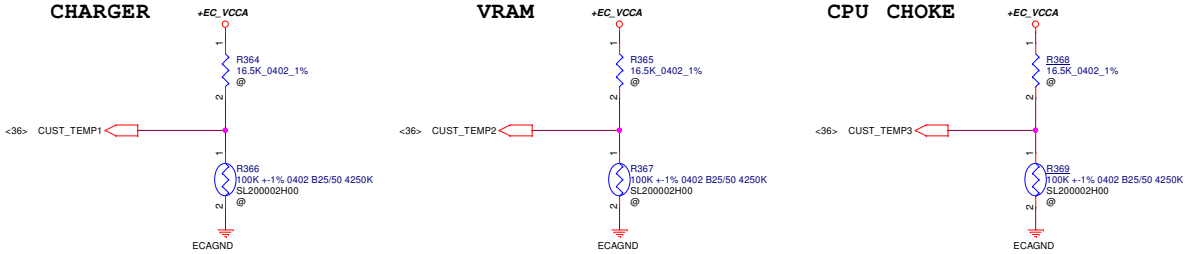
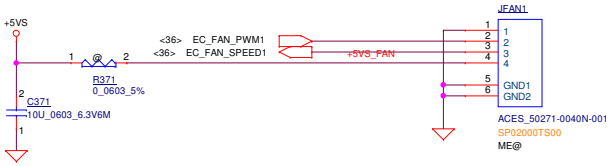
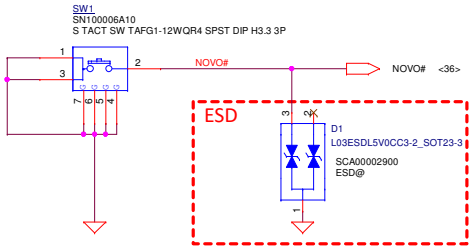
THERMISTOR



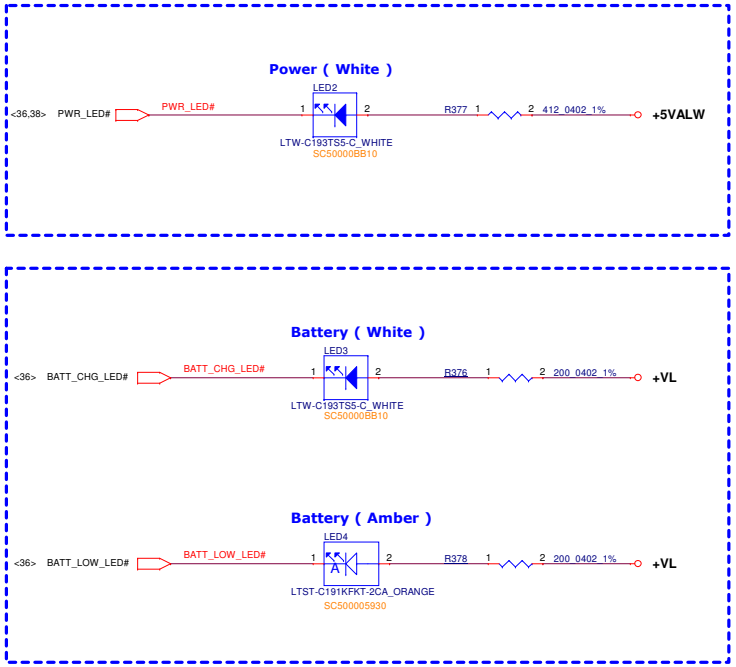
FAN



NOVO BUTTON



LED



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: FAN / Thermal / LED / NOVO

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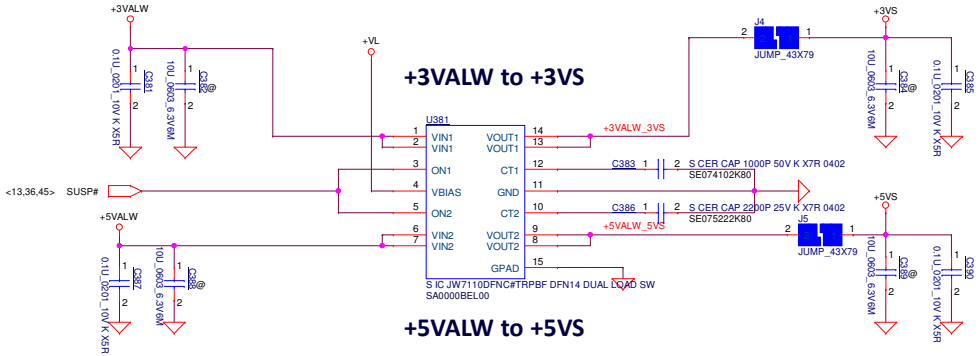
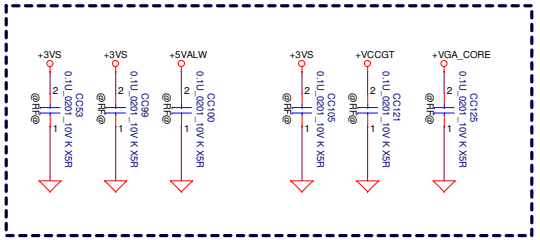
DC to DC

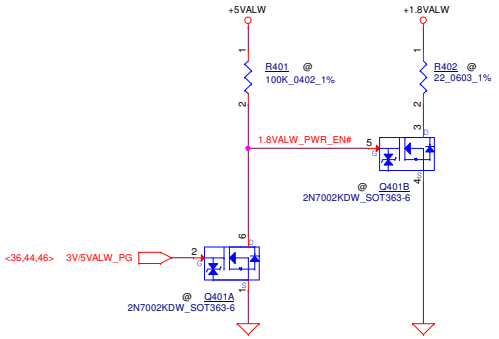


RF By-Pass / Cross Moat Caps



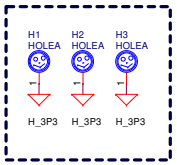
DISCHARGE CIRCUIT

For +1.8VALW Discharge

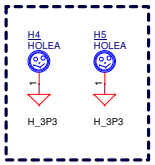


MISC.

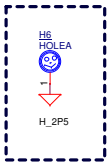
CPU



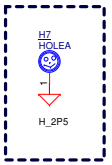
VGA



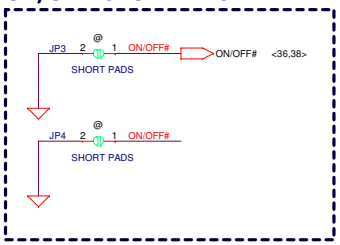
LAN



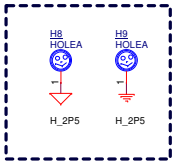
BATTERY



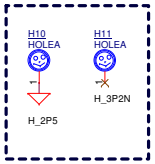
ON/OFF# SHORT PADS

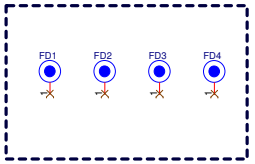


DC IN

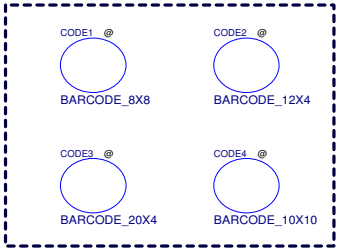


FAN

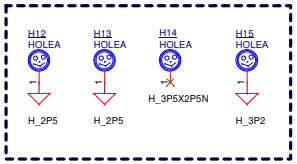




LASER BARCODE



MISC.



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Compal Electronics, Inc.

Title: DC to DC / Discharge / MISC

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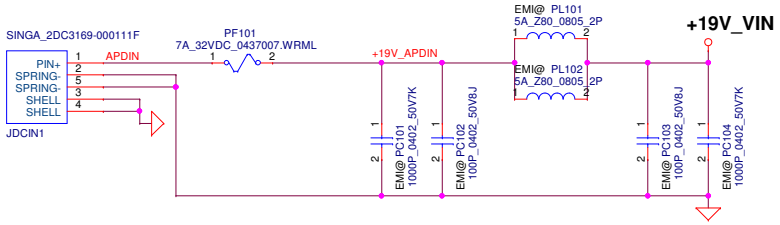

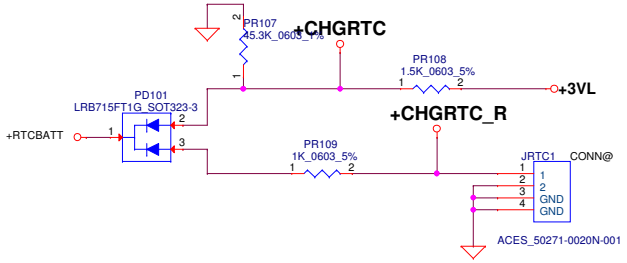

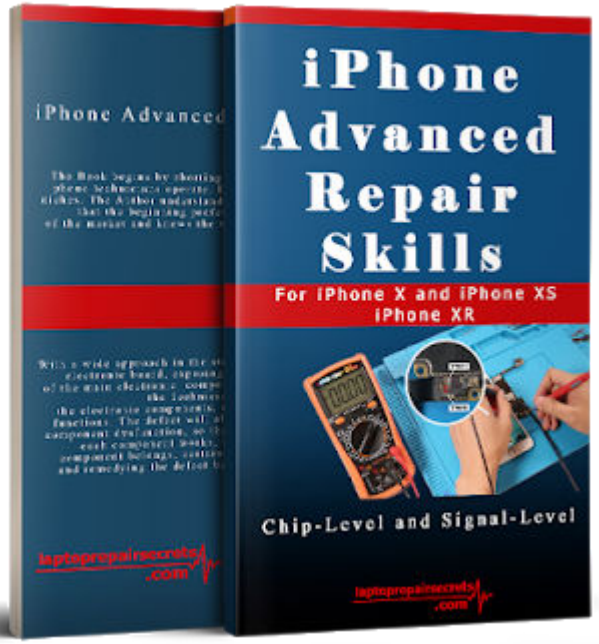

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **PWR- DCIN / Vin Detector**

Size	Document Number	Rev
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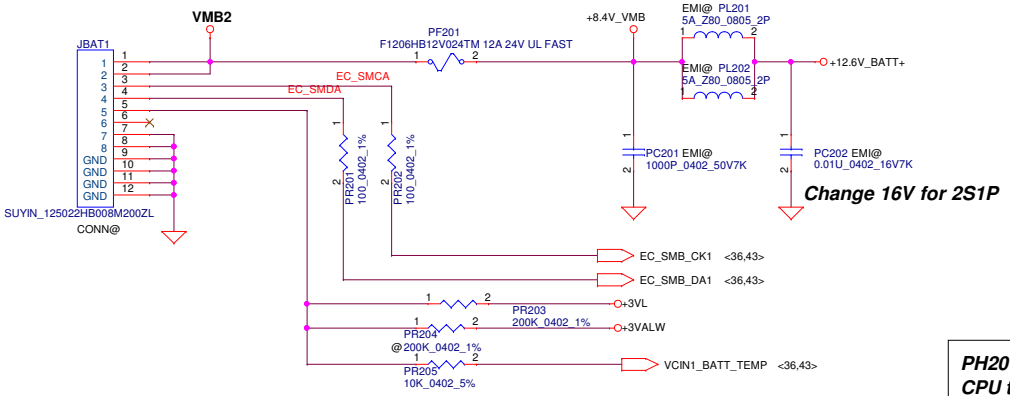
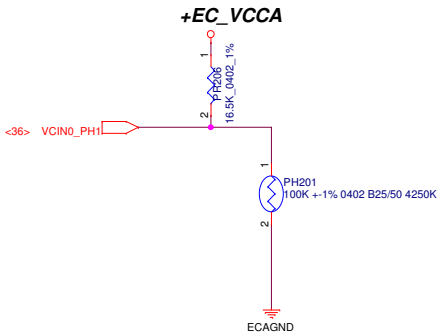


PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: **PWR- BATTERY CONN/OTP**

Size	Document Number	Rev
Custom	KBL	1.0

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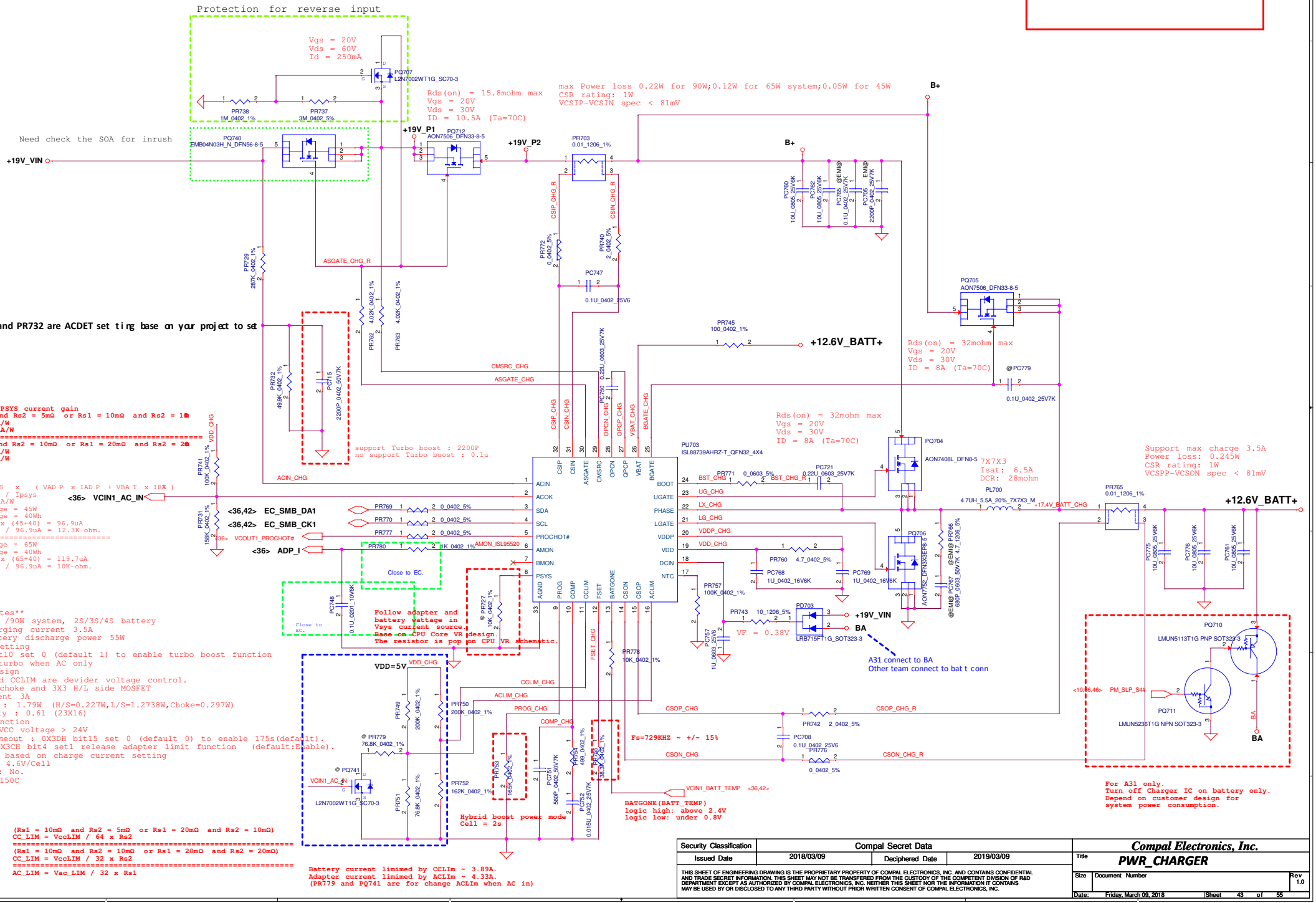
Module model information

ISL95520A_Hybrid_Boost_V2.mdd



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Compal Electronics, Inc.			
Title	PWR_CHARGER		
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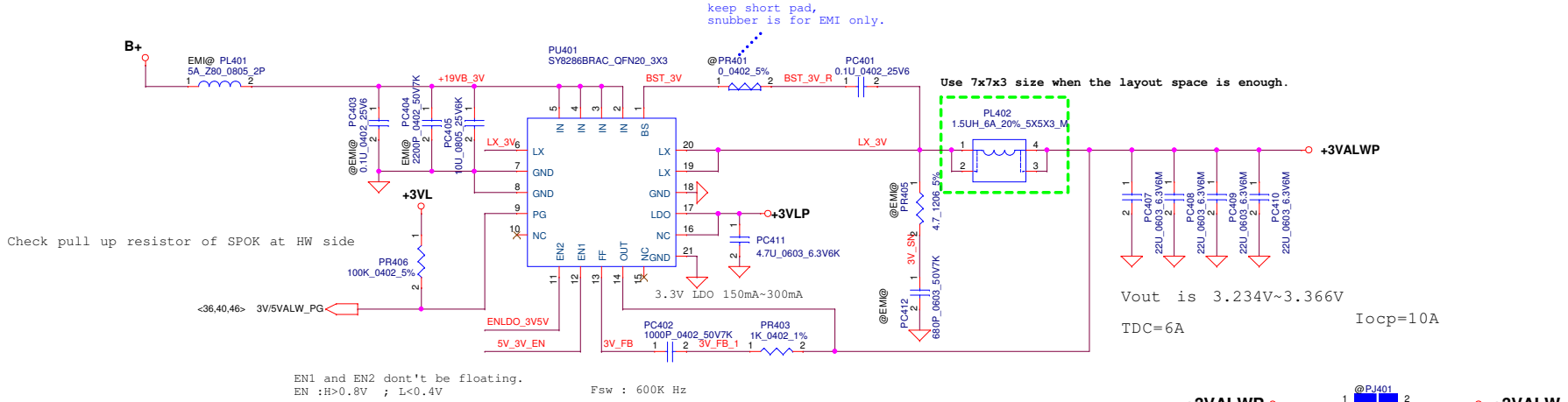
Module model information

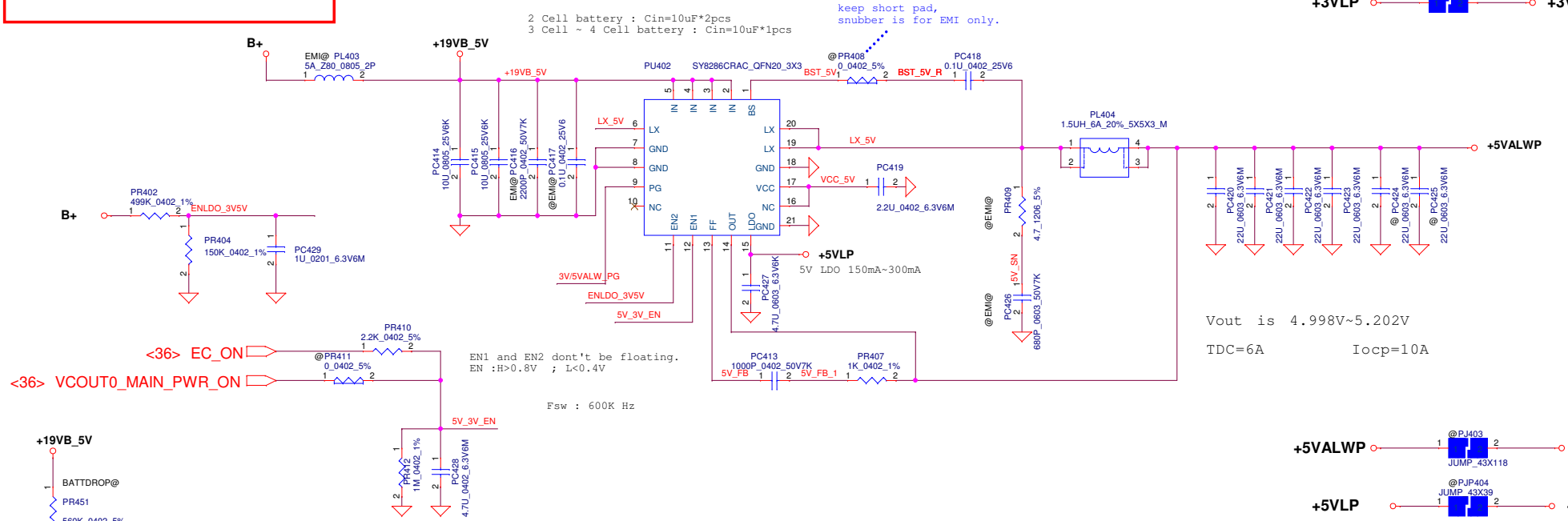
SY8286B_V3_single.mdd
SY8286B_V3_dual.mdd



+3VALWP — @PJ401 JUMP_43X118 — +3VALW

+3VLP — @PJP402 JUMP_43X39 — +3VL

Module model information
SY8286C_V3_single.mdd
SY8286C_V3_dual.mdd



+5VALWP — @PJ403 JUMP_43X118 — +5VALW

+5VLP — @PJP404 JUMP_43X39 — +VL

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: +3VALW/+5VALW

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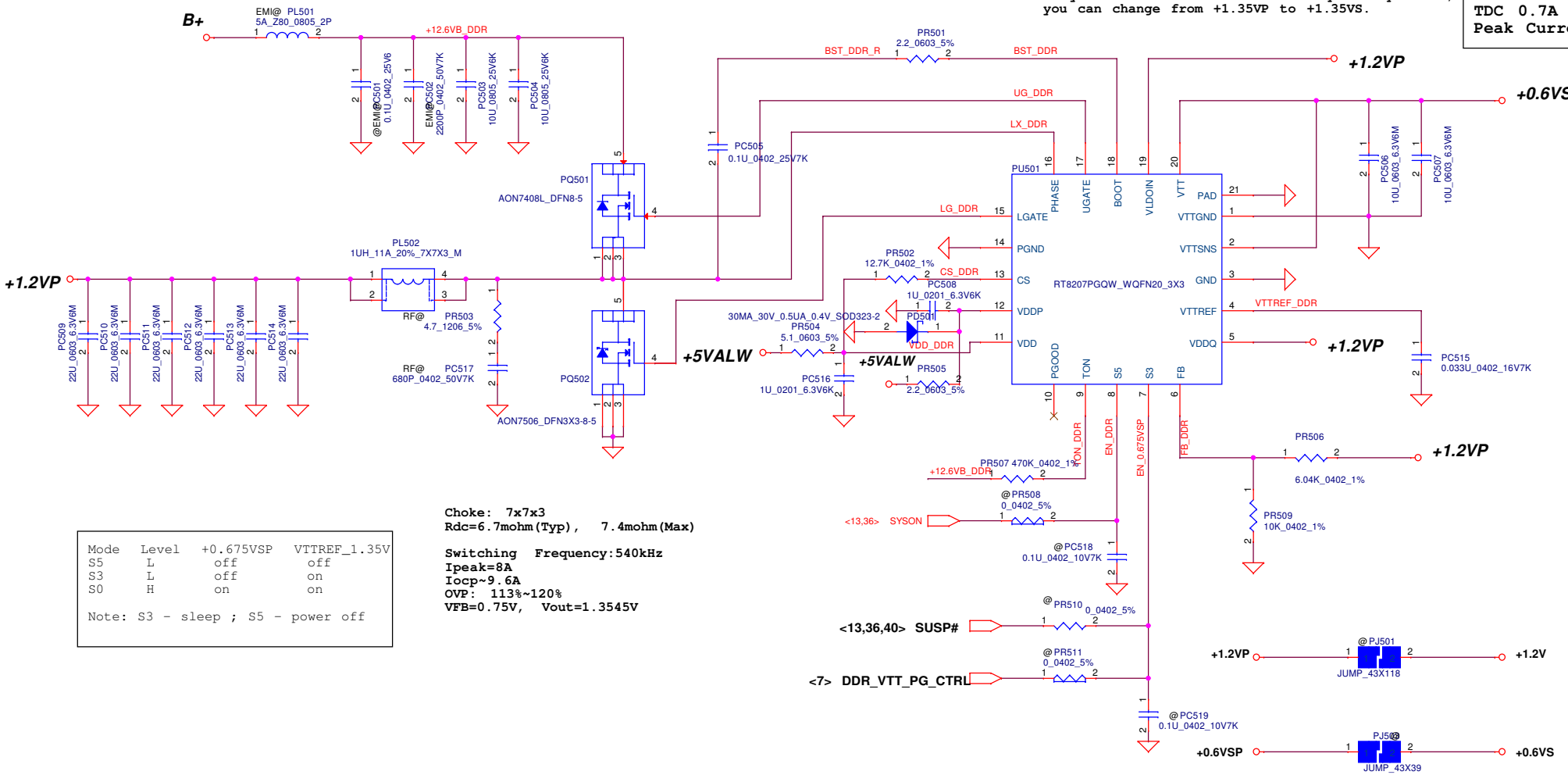
Module model information

RT8207P_single_V3.mdd For Single layer
RT8207P_dual_V3.mdd For Dual layer

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A



Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency:540kHz
Ipeak=8A
Iocp~9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number | Rev 1.0

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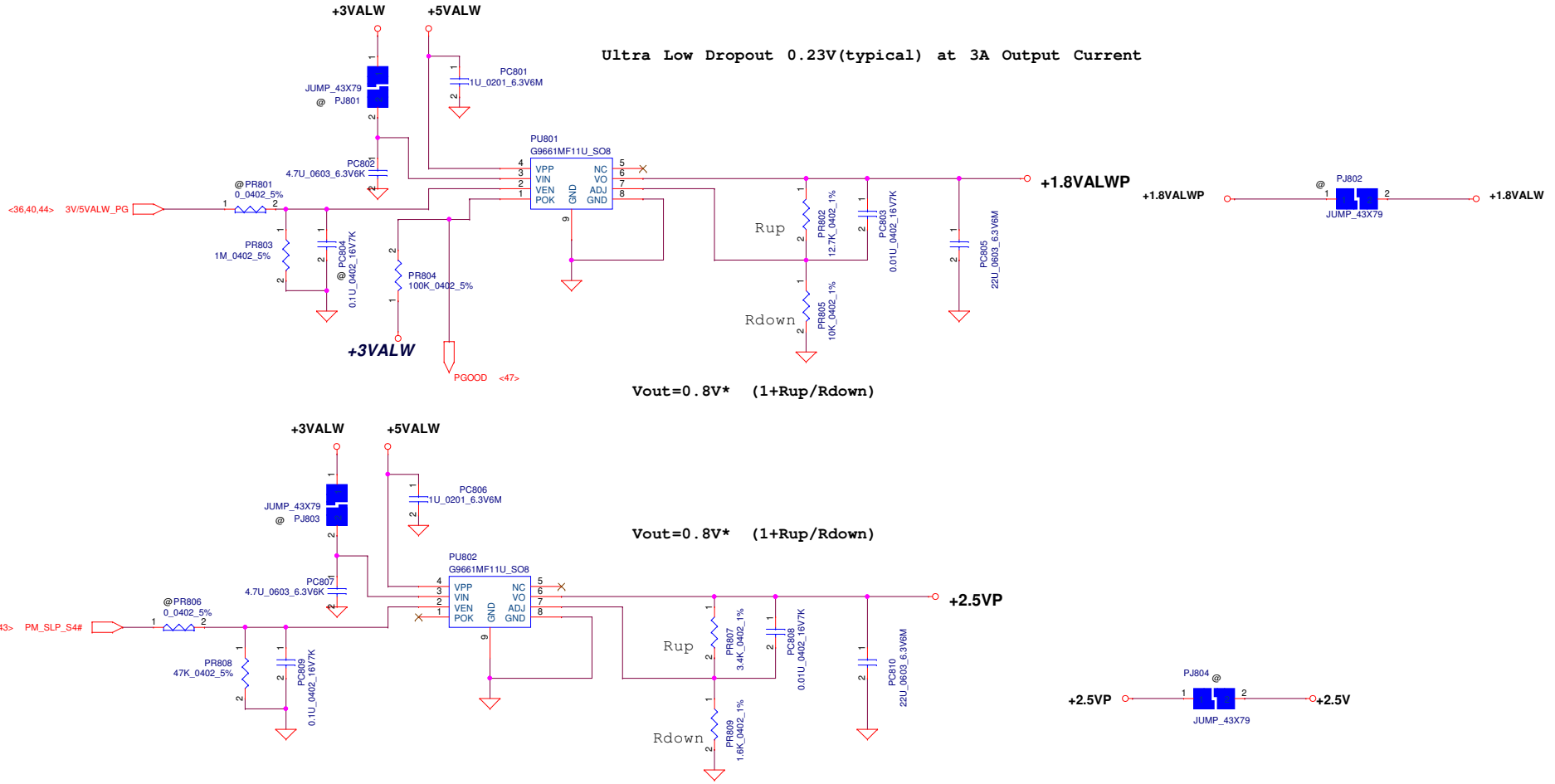
Module model information

APL5930_V2.mdd



Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: APL5930

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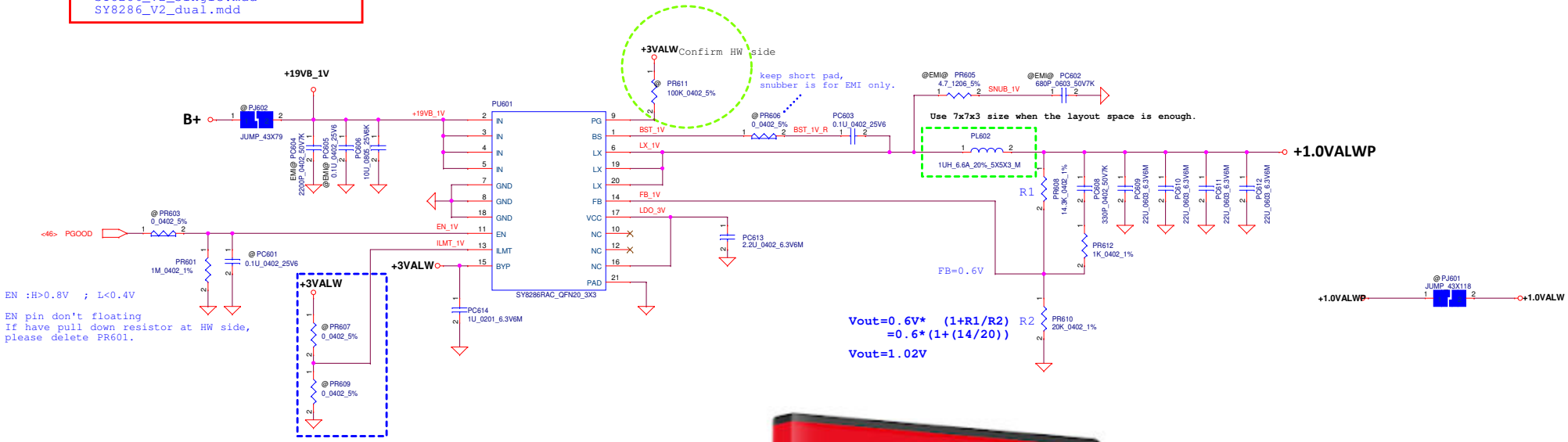
Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd



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Compal Electronics, Inc.

Title: SY8286

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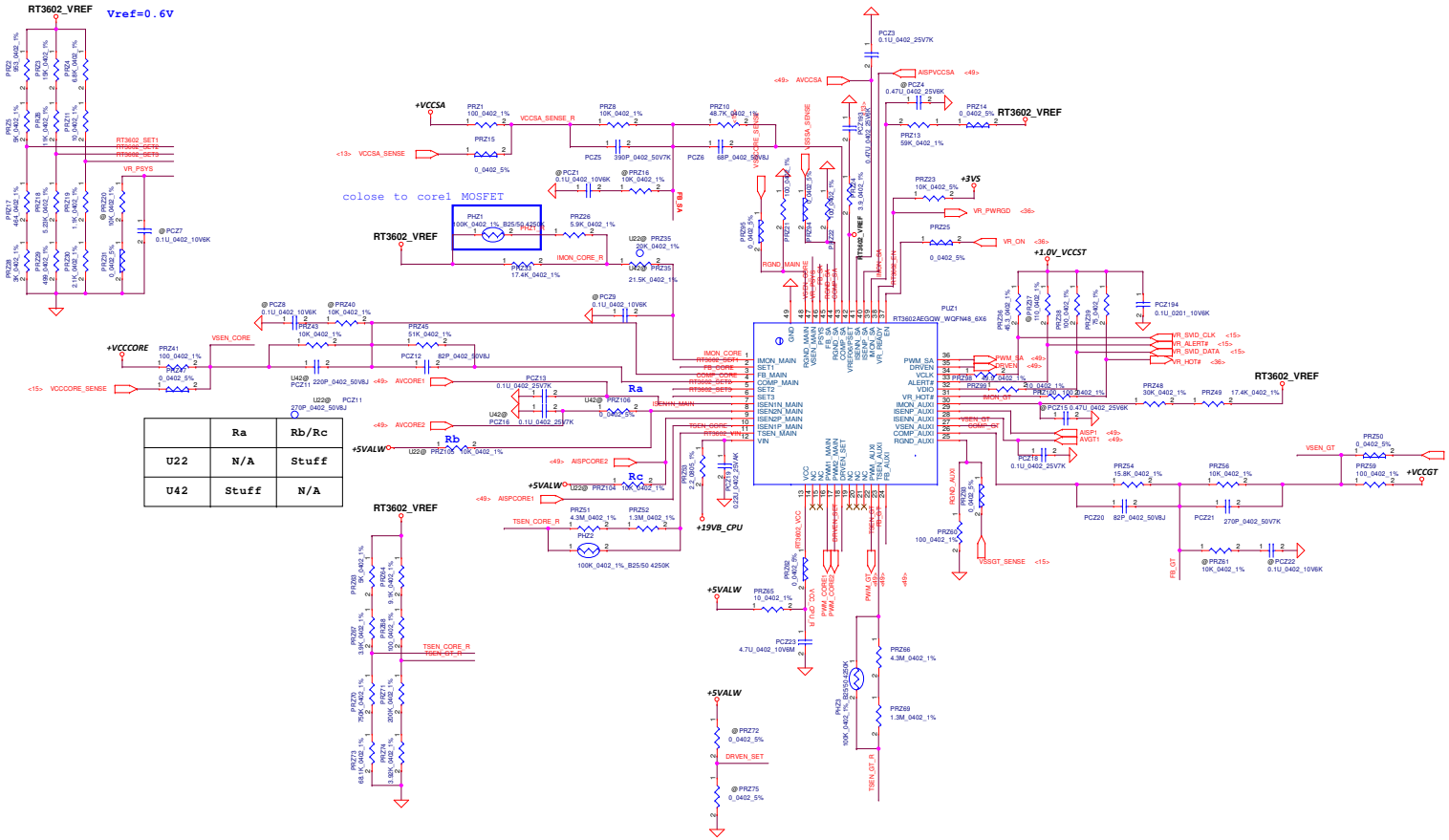

	Ra	Rb/Rc
U22	N/A	Stuff
U42	Stuff	N/A

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Issued Date	2018/03/09	Deciphered Date	2019/03/09
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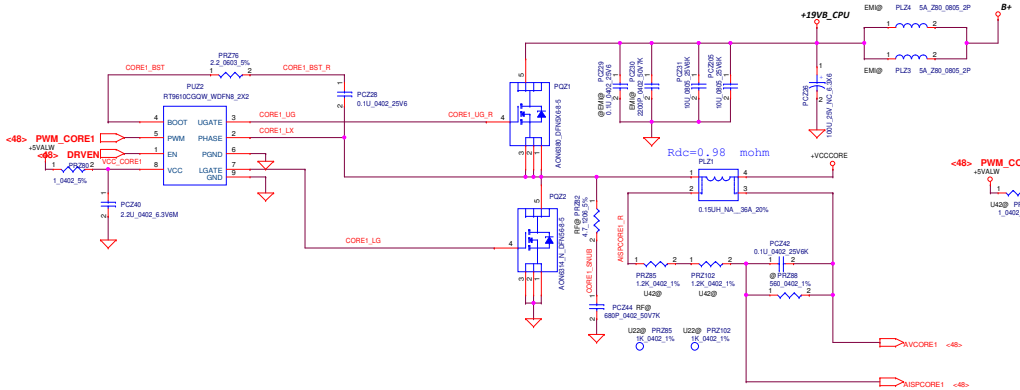
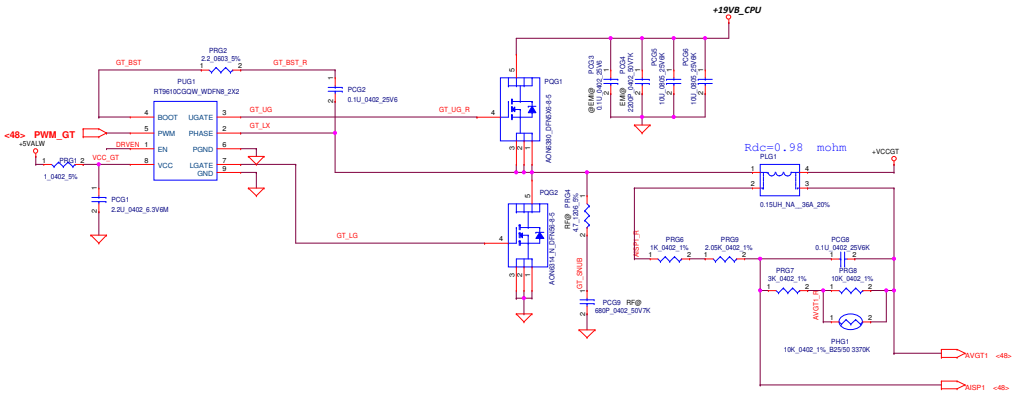
			Size: Document Number: Rev: 1.0
			Date: Friday, March 09, 2018 Sheet 48 of 55



H/S AON6280:
R DS(ON) (at V GS =10V) < 6.8m
R DS(ON) (at V GS =4.5V) < 10.5m

L/S AON6214:
R DS(ON) (at V GS =10V) < 2.8m?
R DS(ON) (at V GS =4.5V) < 3.5m?



VCC_CORE
FSW=450kHz
Choke=0.15uH
DCR=0.67 mohm +/- 5%

U22
LL=2.4 mohm
TDC=21A
ICCMAX=32A
OCP=40A

U42
LL=2.4 mohm
TDC=42A
ICCMAX=64A
OCP=70A

VCC_GT
FSW=450kHz
Choke=0.15uH
DCR=0.67 mohm +/- 5%

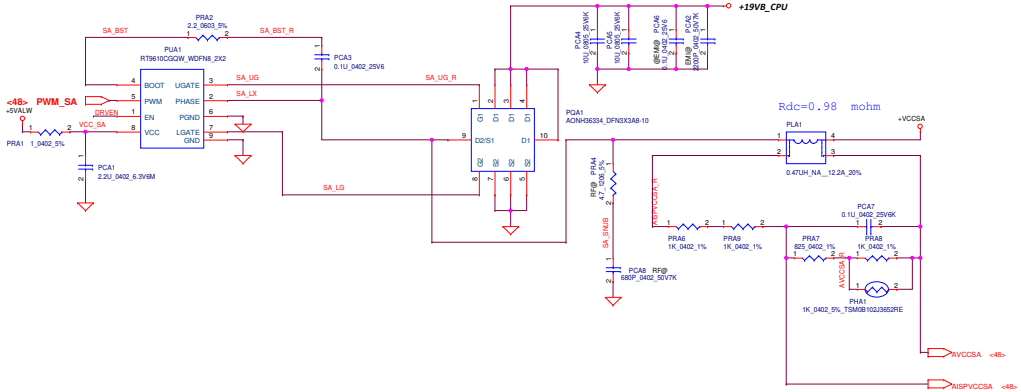
U22
LL=3.1 mohm
TDC=18A
ICCMAX=31A
OCP=39A

U42
LL=3.1 mohm
TDC=12A
ICCMAX=28A
OCP=39A

VCC_SA
FSW=600kHz
DCR=6.2 mohm +/- 5%

U22
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A

U42
LL=10.3 mohm
TDC=4A
ICCMAX=5A
OCP=10A



Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: *CPU Power stage*

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+VCCCORE

VCCCORE :
U22
22uF*28
1uF*35

U42
330uF*1
22uF*28
1uF*35

+VCCGT

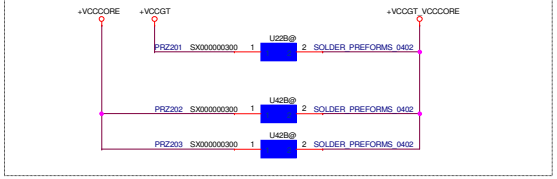
VCCGT :
U22 & U42
330uF*1
22uF*33
1uF*13

VCCSA :
U22 & U42
22uF*9
1uF*7

+VCCSA

+VCCGT_VCCCORE U42 co-lay

U22/U42 co-lay



Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: *PROCESSOR DECOUPLING*

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Module model information

RT8812A-1P_V2A.mdd for IC portion

RT8812A-1P_V2B.mdd for SW portion

PWM-VID Spec and component Values

PWM-VID Spec		Config A	Config B	Config C
Vmin		0.6V	0.6V	0.65V
Vmax		1.2V	1.2V	1.15V
Vboot		0.875V	0.9V	0.9V
Voltage step		6.25mV	6.25mV	25mV
N of Voltage level		96	96	20
Rrefadj	PR8	39K	20K	39K
Rref1	PR7	39K	20K	30K
Rboot	PR10	1.5K	2K	3K
Rref2=PR20+PR21	PR20	30K	18K	24K
	PR21	1.5K	0	3K
C	PC9	1.5nf	2.7nf	1.8nf

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) + 40 mV) / 10uA

I_ripple=(19-0.9)*0.9/
(304.89Khz*0.36u*19)=7.811A

Iocp=42A per phase
Ivalley=42A-7.811A/2=38.0945A

Choke: 0.22uH (Size:10*10*4)
Rdc=0.82 ± 5 %
Heat Rating Current=40A
Saturation Current=90A

C=3*330uF (9mohm)=990uF
Vripple=Iripple*ESR(min)=7.811A*3mohm=23.4mV

Different VGA Chip (different EDP-Peak Current) need select different solution

VGA Chip	N14P-GV	N14M-LP	N14P-LP
	Config B	Config B	Config B
Rated TDP Power at Tj=102C	18W	13W	18.9W
Boosted GPU Total at Tj=102C	25W	20W	23W
EDP-Continuous at Tj=102C	24A	22A	25A
EDP-Peak at Tj=102C	35A	35A	35A
Istep max (Evaluation)	15A	20A	14A
OCP Setting Current	42A	42A	42A
Rocset (PR12)	10.2K	10.2K	10.2K
Recommendation	1phase 2H2L	1phase 2H2L	1phase 2H2L
Polymer Cap (330uF)	6mohm * 2	6mohm * 2	6mohm * 2
Or OSCON (390uF)	10mohm * 3	10mohm * 3	10mohm * 3

Whether needs 3 OSCON capacitors depend on DC ripple test results!

OpenVReg Configurations

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.8V
1 phase with CCM	1.2V to 1.8V
Active phase with CCM	2.4V to 5.5V

Pull high on HW side

+VGA_CORE MX110
EDP-Continuous 18.8A
EDP-Peak 31A
OCP min 40A

+VGA_CORE MX130
EDP-Continuous 27.2A
EDP-Peak 53A
OCP min 65A

Under GPU Core GB2B-64 package

Remark:
1. Switching frequency setting: Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p) =304.89Khz
2. Soft-Start time (Internal) is 0.7ms (PC18 un-pop)
Tss=(Css*Vrefin)/Iss+2.3ms =0.01U*0.9V/5uA+2.3ms=4.1ms (PC18 pop)

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

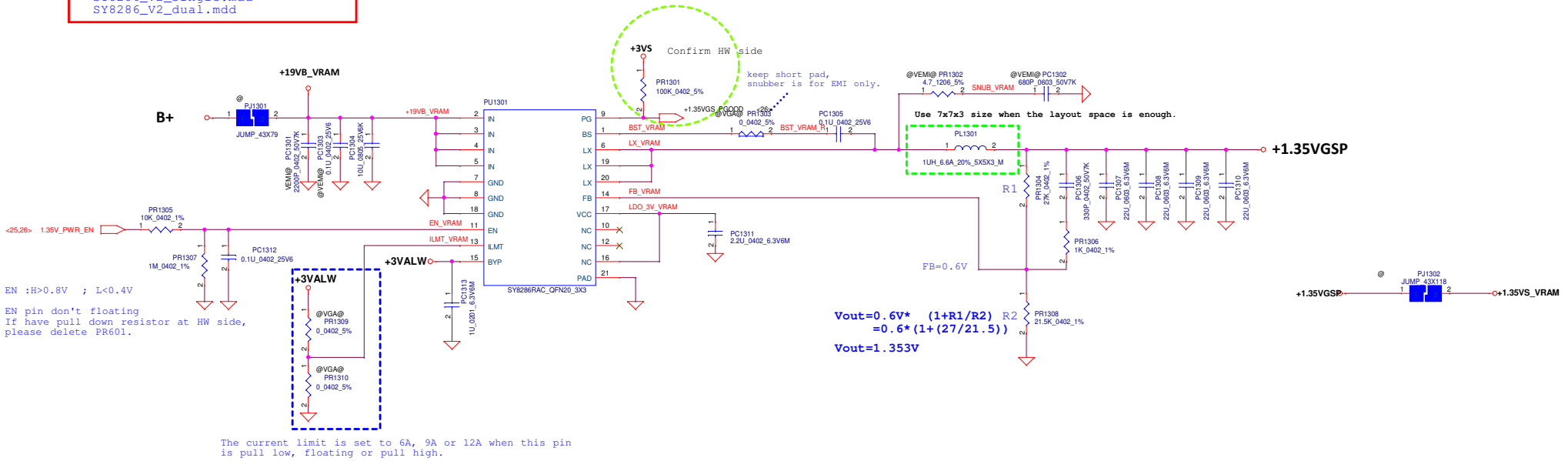
Title: VGA_CORE

Size: Custom | Document Number: VGA_CORE | Rev: 1.0

Date: Friday, March 09, 2018 | Sheet 51 of 55

Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd



EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

The current limit is set to 6A, 9A or 12A when this pin
is pull low, floating or pull high.

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: SY8286

Size	Document Number	Rev
C		1.0

Date: Friday, March 09, 2018 Sheet 52 of 55

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Down size for material shortage	P49	Change PRA6,PRA9,PRG6 from 1K +-1% 0603 to 1K +-1% 0402	2018.03.05	SVT
2	Down size for material shortage	P49	Change PRZ102,PRZ85 from 1.2K +-1% 0603 to 1.2K +-1% 0402	2018.03.05	SVT
3	Down size for material shortage(U42 SKU)	P49	Change PRZ103,PRZ87 from 1.2K +-1% 0603 to 1.2K +-1% 0402	2018.03.05	SVT
4	Down size for material shortage	P49	Change PRG9 from 2.05K +-1% 0603 to 2.05K +-1% 0402	2018.03.05	SVT
5	Down size for material shortage	P43	Change PR404 from 499K +-1% 0402 to 150K +-1% 0402 Change PC429 from 1U 16V K X5R 0402 to 1U 6.3V M X5R 0201	2018.03.05	SVT
6	Down size for material shortage	P50 P51	Change PC10,PC1313,PC30,PC31,PC32,PC33,PC614,PC801,PC806,PCZ117,PCZ151, PCZ166,PCZ167,PCZ170,PCZ179 from 1U 6.3V K X5R 0402 to 1U 6.3V M X5R 0201	2018.03.05	SVT
7	Down size for material shortage	P49	Change PCA1,PCG1,PCZ40,PCZ41 from 2.2U 16V K X5R 0402 to 2.2U 6.3V M X5R 0402	2018.03.05	SVT
8	Change size for common design	P44	Change PC401,PC418,PC603,PC1305 from 0.1U 10V K X5R 0201 to 0.1U 25V K X5R 0402	2018.03.05	SVT
9	Down size for material shortage	P48	Change PCZ23 from 4.7U 10V K X5R 0603 to S CER CAP 4.7U 10V M X5R 0402	2018.03.05	SVT
10	Down size for material shortage	P51	Change PC20,PC28,PC36,PC37,PC38,PC39,PC40 from 4.7U 6.3V K X5R 0603 to 4.7U 6.3V M X5R 0402	2018.03.05	SVT
11	Down size for material shortage	P45	Change PC505 from CAP .1U 25V K X7R 0603 to 0.1U 25V K X7R 0402	2018.03.05	SVT
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2018/03/09	Deciphered Date	2019/03/09

Compal Electronics, Inc.

Title: **PIR (PWR)**

Size: Custom | Document Number: Z_BDW | Rev: 1.0

Date: Friday, March 09, 2018 | Sheet 53 of 55

Version change list
(P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	ME Request	41	Add Screw Hole H15.	2017/12/13	EVT -> PVT
2	ME Request	41	Remove Screw Hole H16.	2017/12/15	EVT -> PVT
3	0 Ohm Reduction	31	Replace RA2 with R-Short.	2017/12/18	EVT -> PVT
4	0 Ohm Reduction	34	Replace R242 with R-Short.	2017/12/18	EVT -> PVT
5	0 Ohm Reduction	29	Replace R203, R211, R212 with R-Short.	2017/12/18	EVT -> PVT
6	Phase Out Un-Necessary X4E Level	3	Remove X4EABQ38L51 and X4EABQ38L52.	2017/12/19	EVT -> PVT
7	Update 14" PCB DA Part Number.	3	DA6001YG000 -> DA6001YG100	2017/12/19	EVT -> PVT
8	Cost Down Plan	36	C2147, C2149 -> 14" Only (BOM Structure Modify)	2017/12/20	EVT -> PVT
9	0 Ohm Reduction	36	Replace R420 with R-Short.	2017/12/20	EVT -> PVT
10	Cost Down Plan	20	Un-Pop CU206, CU204, CD41, CU198, CD210, CU213, CU212, CD46	2017/12/21	EVT -> PVT
11	Cost Down Plan	19	Un-Pop C2140, CD19, CD10, CD32, CD33, CD23	2017/12/21	EVT -> PVT
12	Cost Down Plan	18	Un-Pop CD127	2017/12/21	EVT -> PVT
13	Cost Down Plan	13	Replace CC45 with 10uF	2017/12/21	EVT -> PVT
14	0 Ohm Reduction	35	Replace R233 with R-Short.	2017/12/21	EVT -> PVT
15	0 Ohm Reduction	39	Replace R275, R276, R277, R279 with R-Short.	2017/12/21	EVT -> PVT
16	0 Ohm Reduction	10	Replace RC103 with R-Short.	2017/12/21	EVT -> PVT
17	0 Ohm Reduction	19	Replace RD108, RD140 with R-Short.	2017/12/21	EVT -> PVT
18	0 Ohm Reduction	39	Replace R283 with R-Short.	2017/12/21	EVT -> PVT
19	0 Ohm Reduction	37	Replace R425, R428, R102 with R-Short.	2017/12/21	EVT -> PVT
20	0 Ohm Reduction	32	Replace RL18 with R-Short.	2017/12/21	EVT -> PVT
21	0 Ohm Reduction	40	Replace R371 with R-Short.	2017/12/21	EVT -> PVT
22	Cost Down Plan	28	Un-Pop CV703, CV707, CV708, CV718 (DIS@)	2017/12/21	EVT -> PVT
23	Cost Down Plan	27	Un-Pop CV603, CV607, CV614, CV616, CV617 (DIS@)	2017/12/21	EVT -> PVT
24	Cost Down Plan	22	Un-Pop CV35 (DIS@)	2017/12/21	EVT -> PVT
25	Cost Down Plan	28	Replace CV701 with 10uF	2017/12/21	EVT -> PVT
26	Cost Down Plan	27	Replace CV602 with 10uF	2017/12/21	EVT -> PVT
27	Cost Down Plan	41	Un-Pop Q401, R401, R402	2017/12/21	EVT -> PVT
28	Cost Down Plan	13	Un-Pop CC40	2017/12/21	EVT -> PVT
29	Cost Down Plan	18	Replace RD200, RD201, RD202, RD203, RD205 with R-Short. (SDP@/DDP@)	2017/12/21	EVT -> PVT
30	Cost Down Plan	20	RD211 -> DDP Only (BOM Structure Modify)	2017/12/21	EVT -> PVT
31	VRAM EOL	27, 28	Remove VRAM UV8, UV9 (Replace with x32 DIE *2)	2017/12/22	EVT -> PVT

Compal Electronics, Inc.
Title: PIR (HW)
Size: Custom | Document Number: LA-G201P | Rev: 1.0
Date: Friday, March 09, 2018 | Sheet 54 of 55

Item	Reason for change	PG#	Modify List	Date	Phase
1	ME Request	38	Replace Touch Pad Connector Symbol (JTP1) - SP01001A800	2017/12/22	EVT -> PVT
2	VRAM EOL	24	Replace ROM_SI (RV65) BOM Structure with 256M*32	2017/12/25	EVT -> PVT
3	VRAM EOL	3	Replace 2GB VRAM X76 BOM Structure with @ (X7677538L01, L02, L03)	2017/12/25	EVT -> PVT
4	Layout Footprint Update	34, 35	Swap JHDD1, JODD2 Pin Define	2017/12/25	EVT -> PVT
5	VRAM EOL	27	Replace UV7 Data Lanes / EDC / DBI / RV130.2 - Pull High +1.35VS_VRAM	2017/12/26	EVT -> PVT
6	Fine Tune YL1 Crystal Capacitor Value	31	CL13 / CL14 : 10pF -> 27pF	2017/12/26	EVT -> PVT
7	Card Reader IC Controlled by X76	3, 32	Realtek -> X7677538LA1 , Genesys -> X7677538LA2.	2017/12/26	EVT -> PVT
8	EMI Cost Down Plan	30	Replace CA41, CA42 with R-Short (Location Changed to RA65, RA66)	2017/12/28	EVT -> PVT
9	Prevent +3VS_WLAN Drop	33	Reserve C245, C246	2017/12/29	EVT -> PVT
10	ME Request	34, 35	Replace JODD2, JHDD1 Symbol with SP010025K00	2017/12/31	EVT -> PVT
11	VRAM BOM Structure Update	3	Replace X7677538L04, L05, L06 BOM Structure with 2GB	2018/01/08	EVT -> PVT
12	Card Reader IC BOM Structure Update	32	Controlled by Main/Substitute, No X76 Anymore	2018/01/08	EVT -> PVT
13	VRAM BOM Structure Update	3	Delete X7677538L01, L02, L03 (EVT VRAM*4 - 2GB)	2018/01/08	EVT -> PVT
14	On Board RAM P/N Update	11	Replace On Board RAM P/N with R3	2018/01/08	EVT -> PVT
15	Cap P/N Update	40	Replace C383 470pF with 1nF (SE074102K80)	2018/01/08	EVT -> PVT
16	Cap P/N Update	40	Replace C386 220pF with 2.2nF (SE075222K80)	2018/01/08	EVT -> PVT
17	Dual Load Switch P/N Update	13, 40	Replace UC5, U381 SA00006U300 with SA00007PM00	2018/01/08	EVT -> PVT
18	Update CPU R3 Part Number	3	Add SA0000BKN30 (i3-8130U R3) and SA0000BLH50 (i3-7020U R3).	2018/02/22	PVT -> Pre-MP
19	Resistor Fine Tune - LED3 and LED4	39	Replace R376 and R378 with 200 Ohm. (SD034200080)	2018/02/22	PVT -> Pre-MP
20	Dual Load Switch P/N Update. (Source Priority Changes)	13, 40	Replace UC5, U381 - SA00007PM00 with SA0000BEL00.	2018/02/22	PVT -> Pre-MP
21	Keyboard Resistor Value Update	38	Replace R271 with 0 Ohm (@)	2018/02/22	PVT -> Pre-MP
22	Keyboard Resistor Value Update	38	Replace R278 with R-Short.	2018/02/22	PVT -> Pre-MP
23	Keyboard Resistor Value Update	38	Replace R272, R274, "R277 (15@)" with 470 Ohm.	2018/02/22	PVT -> Pre-MP
24	Co-Lay Remove	17	Remove LC99	2018/02/27	PVT -> Pre-MP
25	Replace BOM Structure	3	Replace SA0000BLH50 BOM Structure with i3_7020U_U22@.	2018/03/09	PVT -> Pre-MP
26	Add CPU	3	Add SA0000BLD60 (SR3LD) - i3_7020U_U42@	2018/03/09	PVT -> Pre-MP
27	Replace DA Part Number with DAZ P/N	3	Replace with DAZ29900201 (14_DAZ@) & DAZ29A00201 (15_DAZ@).	2018/03/09	PVT -> Pre-MP
28	ESD Request	36	Add C122 (0.1uF)	2018/03/09	PVT -> Pre-MP
29					
30					
31					