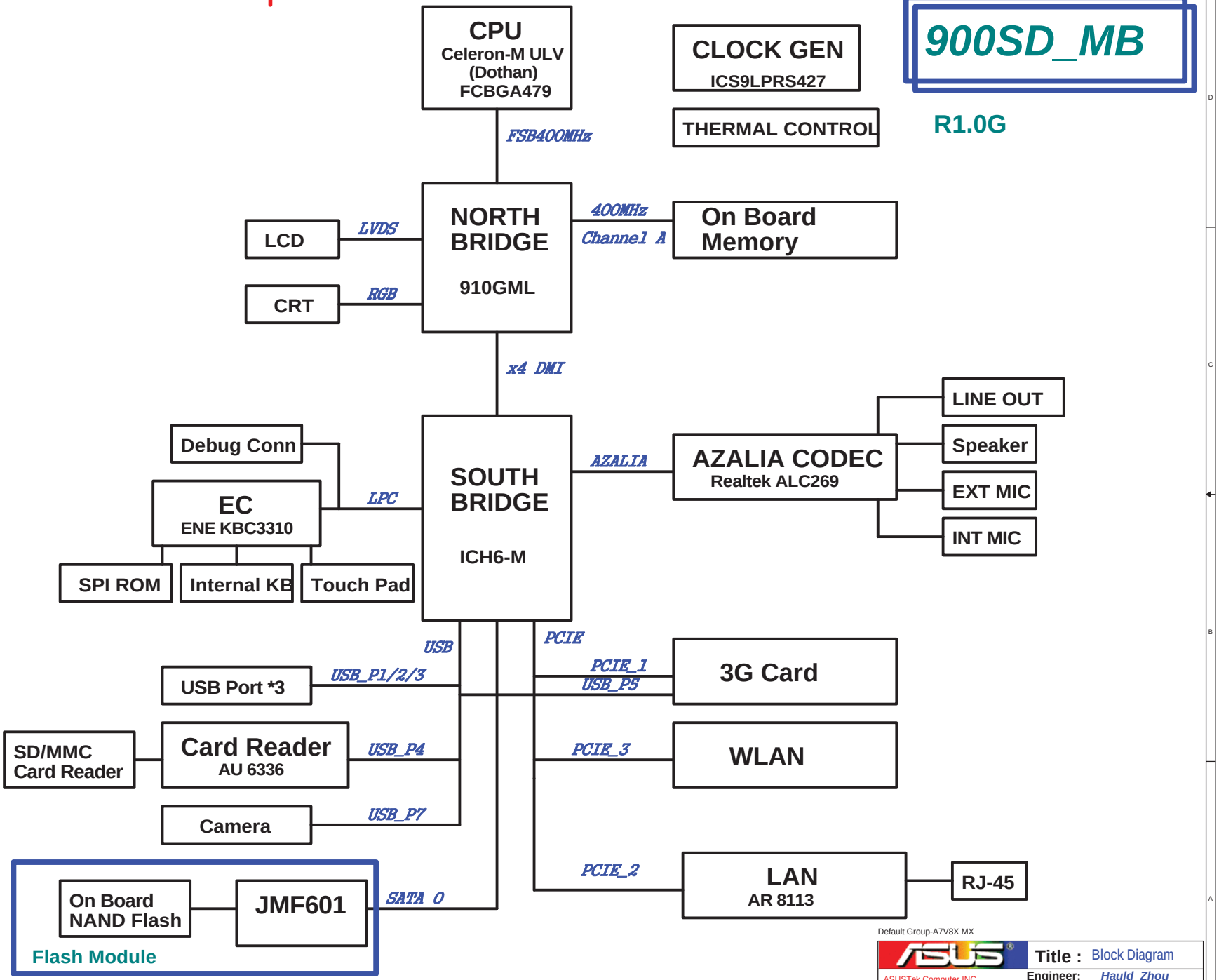


Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Block Diagram	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 1 of 51	

ICH6 GPIO SETTING

Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPI0/REQ6#	10K Pull +3V	I	fixed as Input only
E8	GPI1 / REQ5#	10K Pull +3V	I	fixed as Input only
D9	GPI2 / PIRQE#	10K Pull +3V	I	fixed as Input only
C7	GPI3 / PIRQF#	10K Pull +3V	I	fixed as Input only
C6	GPI4 / PIRQG#	10K Pull +3V	I	fixed as Input only
M3	GPI5 / PIRQH#	10K Pull +3V	I	fixed as Input only
AD19	GPI6 / BMBUSY#	NB BMBUSY#	I	Input
AE19	GPI7	NC	GPI	fixed as Input only
R1	GPI8	EC KBC_SCI#	GPI	fixed as Input only
C23	GPI9/OC4#	10K Pull +3V	I	Input
D23	GPI10/OC5#	10K Pull +3V	I	Input
W6	GPI11 / SMBALERT#	10K Pull +3V	I	Input
M2	GPI12	NC	GPI	fixed as Input only
R6	GPI13	EC EXTSMI#	GPI	fixed as Input only
C25	GPI14/OC6#	10K Pull +3V	I	Input
C24	GPI15 /OC7#	10K Pull +3V	I	Input
D8	GPO16/GTN6#	NC	O	Output
F6	GPO17 / GNT5#	NC	O	Output
AC21	GPO18 / STP_PCI#	Clock GEN STP_PCI#	O	Output
AB21	GPO19	WLAN_LED#	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	NC	GPO	
NA	GPIO22	NA	NA	NA
AD21	GPO23	NC	GPO	fixed as Output only
V3	GPIO24	3G	I/O	Output
P5	GPIO25	NC	I/O	Output

Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GPI26/SATA0GP	NC	GPI	(GPI)Input
R3	GPIO27	NC	I/O	Output
T3	GPIO28	NC	I/O	Output
AE18	GPI29 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GPI30 / SATA2GP	NC	GPI	(GPI)Input
AG18	GPI31 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPIO32 / CLKRUN#	10K Pull +3V	I/O	Input
AF20	GPIO33	NC	I/O	Output
AC18	GPIO34	NC	I/O	Output
NA	GPIO35	NA	NA	NA
NA	GPIO36	NA	NA	NA
NA	GPIO37	NA	NA	NA
NA	GPIO38	NA	NA	NA
NA	GPIO39	NA	NA	NA
F7	GPI40 / REQ4#	10K Pull +3V	I	Input
P4	GPI41 / LDRQ1#	NC	I	Input
NA	GPIO42	NA	NA	NA
NA	GPIO43	NA	NA	NA
NA	GPIO44	NA	NA	NA
NA	GPIO45	NA	NA	NA
NA	GPIO46	NA	NA	NA
NA	GPIO47	NA	NA	NA
E7	GPO48 /GNT4#	NC	O	Output
AC25	GPO49 / CPUPWRGD	CPU Power Ok	O	Output

fixed as Output only

Default Group-A7V8X MX

ASUSTek Computer INC.

Title : System Setting

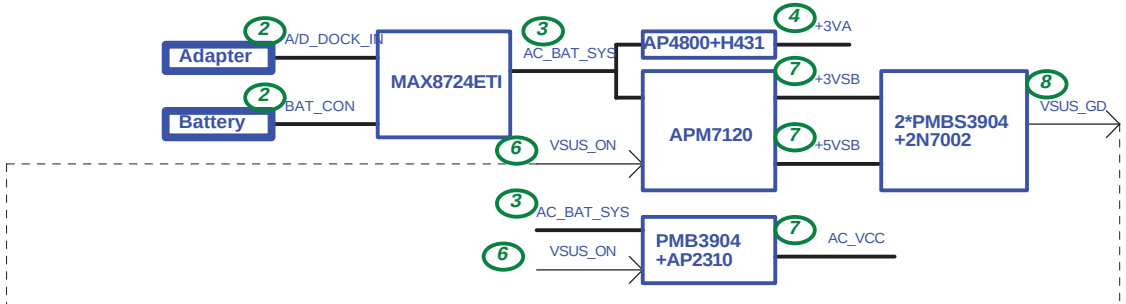
Engineer: Kell_Huang

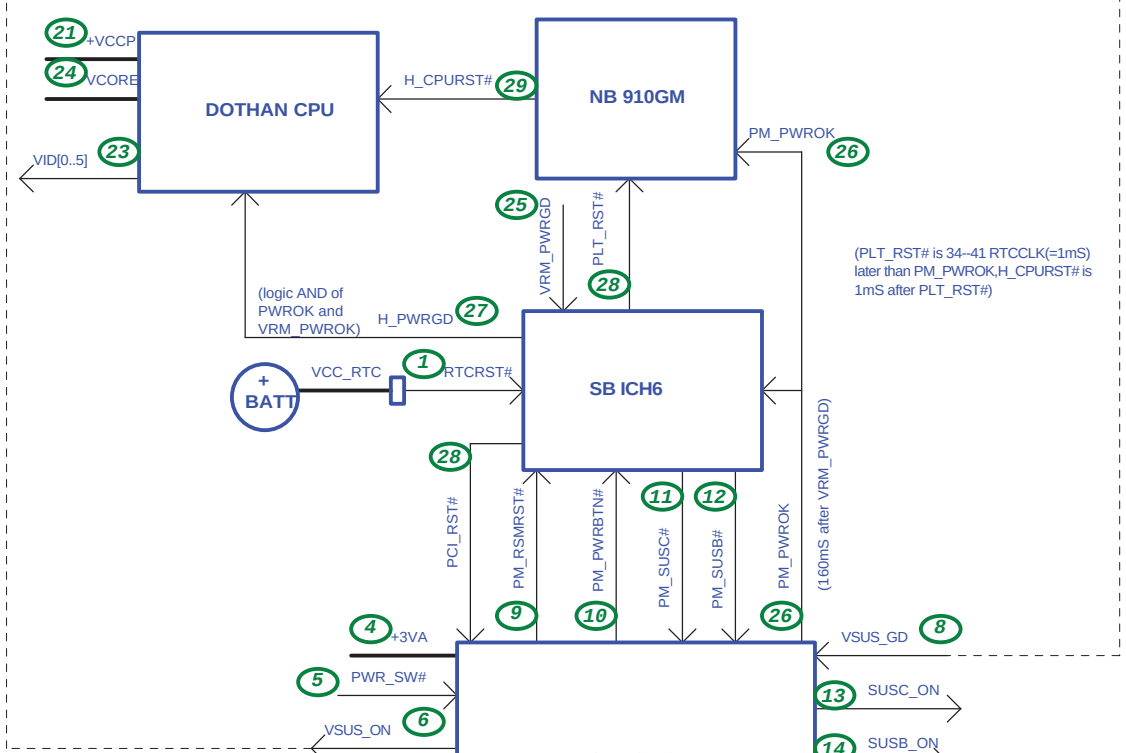
Size	Project Name	Rev
A3	900SD_MB	R1.0G

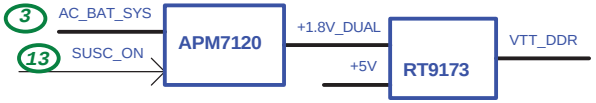
Date: Monday, November 10, 2008 Sheet 2 of 51

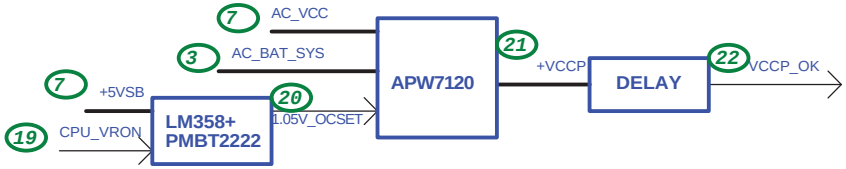
*This sequence is for Battery Plug-in and no Adapter,
if Adapter Plug-in,the sequence change to:
A/D_DOCK_IN--->AC_BAT_SYS--->+3VA--->VSUS_ON--->+3VSB & +5VSB
--->VSUS_GD--->PM_REMRST#--->PWR_SW#--->PM_PWRBTN--->PM_SUSC#--->PM_SUSB#

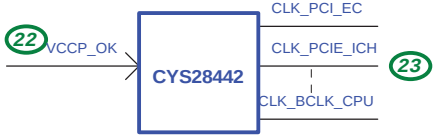
	Signal	S0/S1	S3	S4/S5	Power
Only Battery	VSUS_ON	H	H	L	VSB
Adapter In	VSUS_ON	H	H	H	VSB
	SUSB_ON	H	L	L	Main
	SUSC_ON	H	H	L	DUAL

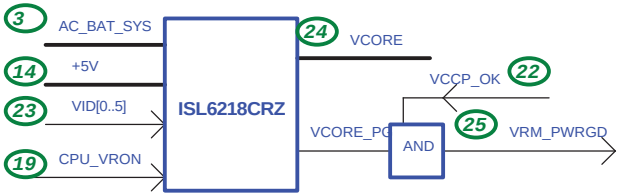












Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Power Sequence	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 3 of 51	

EC KB3310 GPIO SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
1	GA20	A20GATE	O	A20GATE
2	KBRST#	RC_IN#	O	KBRST#
6	GPIO04	CTRL_CAMER_PWR	I	Default : High
13	PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	N.C	O	Reserved
15	GPIO08	EXTSMI#	O	EXTSMI#, 10K Pull +3VSUS
16	GPIO0A	LID_EC#	I	LID_EC#, *
17	GPIO0B	LCD_CSB	O	LCD chip select
18	GPIO0C	LCD_SDA	I/O	LCD Data
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled,*
20	SCI#	KBC_SCI#	O	KBC_SCI#, 10K Pull +3VSUS
21	PWM1	BL_PWM_DA	O	LCD Light Switch
23	PWM2	LCD_SCL	O	LCD clock
25	GPIO11	PM_PWRBTN#	OD	Power Button to SB, *
26	FANPWM1	FAN0_PWM	O	CPU Fan(Unused)
27	FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	FANFB1	FAN0_TACH	I	CPU FanTach(Unused)
29	FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16	E51_TX	O	RS232 debug port
31	GPIO17	N.C	O	Reserved
32	GPIO18	PWR_SW#	I	power button, *
34	GPIO19	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A	CTRL_Mincard_PWR	O	Default : High
38	CLKRUN#	N.C	O	Reserved
39	KSO0	KSO0	O	For Keyboard interface
40	KSO1	KSO1	O	For Keyboard interface
41	KSO2	KSO2	O	For Keyboard interface
42	KSO3	KSO3	O	For Keyboard interface
43	KSO4	KSO4	O	For Keyboard interface
44	KSO5	KSO5	O	For Keyboard interface
45	KSO6	KSO6	O	For Keyboard interface
46	KSO7	KSO7	O	For Keyboard interface
47	KSO8	KSO8	O	For Keyboard interface
48	KSO9	KSO9	O	For Keyboard interface
49	KSO10	KSO10	O	For Keyboard interface
50	KSO11	KSO11	O	For Keyboard interface
51	KSO12	KSO12	O	For Keyboard interface
52	KSO13	KSO13	O	For Keyboard interface
53	KSO14	KSO14	O	For Keyboard interface
54	KSO15	KSO15	O	For Keyboard interface
55	KSI0	KSI0	I	For Keyboard interface
56	KSI1	KSI1	I	For Keyboard interface
57	KSI2	KSI2	I	For Keyboard interface
58	KSI3	KSI3	I	For Keyboard interface
59	KSI4	KSI4	I	For Keyboard interface
60	KSI5	KSI5	I	For Keyboard interface
61	KSI6	KSI6	I	For Keyboard interface
62	KSI7	KSI7	I	For Keyboard interface
63	AD0	P_PMON_10	I	Sense Power Loading
64	AD1	BAT_IN	I	sense Battery
65	AD2	N.C	I	Reserved
66	AD3	N.C	I	Reserved
68	GPO3C	DOC	O	Trigger Clock Gen
70	GPO3D	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E	CLK_PWRSAVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F	BAT_LL#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	PM_RSMRST#	O	10K Pull GND
75	GPIO42	N.C	O	Reserved
76	GPIO43	N.C	O	Reserved
77	SCL1	SMB0_CLK	I/OD	4.7K Pull +3VA_EC
78	SDA1	SMB0_DAT	I/OD	4.7K Pull +3VA_EC
79	SCL2	SMB1_CLK	I/OD	10K Pull +3VS
80	SDA2	SMB1_DAT	I/OD	10K Pull +3VS
81	KSO16	N.C	O	Reserved
82	KSO17	N.C	O	Reserved
83	PSCLK1	N.C	O	Reserved
84	PSDAT1	N.C	O	Reserved
85	PSCLK2	N.C	O	Reserved
86	PSDAT2	N.C	O	Reserved
87	PSCLK3	TP_CLK	I/OD	10K Pull +3VS
88	PSDAT3	TP_DAT	I/OD	10K Pull +3VS
89	GPIO50	BATSEL_3S	O	Battery series. Hi:3S, Lo:4S(Unused)
90	GPIO52	CHG_LED_UP#	O	charger LED
91	GPIO53	CTRL_L2_PWR	O	Default : High
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55	SCRL_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00	SPI_MODE#	O	"HW Strap for SPI Flash deExternal Pull Down 100K ohm to GND"
98	GPXOA01	SUSC_ON	O	
99	GPXOA02	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	ICH8_PWROK	O	
103	GPXOA06	N.C	O	Reserved
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPX0A10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0	BATSEL_2P#	O	Battery parallel. Hi:1P, Lo:2P~3P
110	GPXID1	N.C	O	Reserved
112	GPXID2	THRO_CPU	O	Active if Battery Temperature is
114	GPXID3	SUSB#	I	Pull Down 100K ohm to GND
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3VS
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	N.C	O	Reserved
121	GPIO57	INTERNET#	I	*
126	SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59	N.C	O	Reserved

EC KB3310 Other Pin SETTING

Pin No.	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	8.2K Pull +3VS
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA_EC	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA_EC	P	
24	GND	GND	P	
33	VCC	+3VA_EC	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 100K ohm to GND
67	AVCC	+3VACC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA_EC	P	
111	VCC	+3VA_EC	P	
113	GND	GND	P	
119	RD#	SPI_SO	I	
120	WR#	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R		Reserved 1uF to GND
125	VCC	+3VA_EC	P	
128	SPICS#	SPI_CE#	O	

Default Group-A7V8X MX

ASUSTek Computer INC.

Title : EC Pin Define

Engineer: Kell_Huang

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 4 of 51

CIRCUIT UPDATED HISTORY

Rev	Date	Description
900SD 1.0G	2008.10.15	Initial Release

Default Group-A7V8X MX

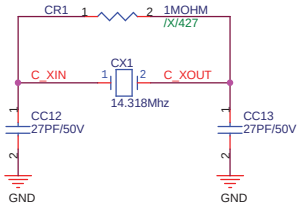
ASUSTek Computer INC.

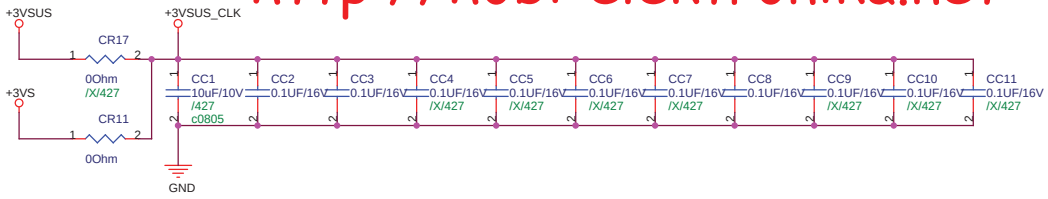
Title : History

Engineer: Hauld Zhou

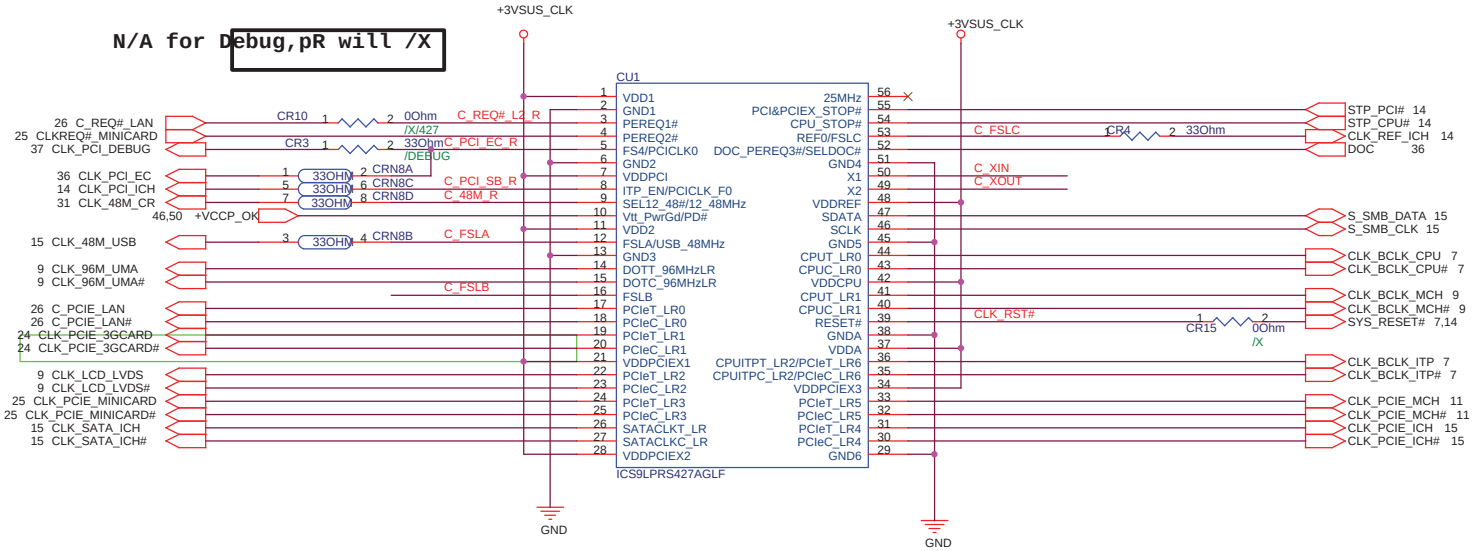
Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 5 of 51



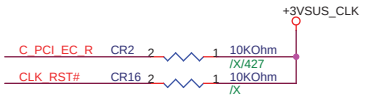


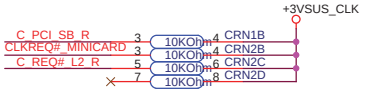
N/A for Debug,pR will /X

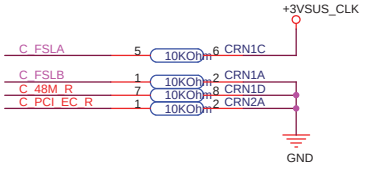


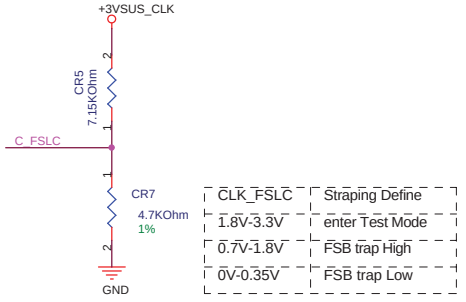
1:Disable
0:Enable

PEREQ1:PCIEx0 & PCIEx1
PEREQ2:PCIEx2 & PCIEx3 & SATA
PEREQ3:PCIEx4 & PCIEx5 & PCIEx6

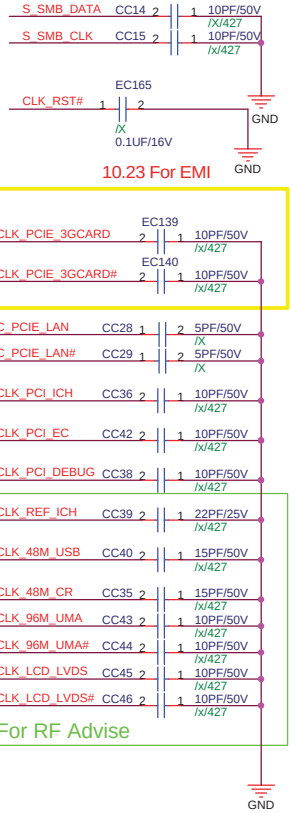








CLK_FSLC	Straping Define
1.8V-3.3V	enter Test Mode
0.7V-1.8V	FSB trap High
0V-0.35V	FSB trap Low



FSLC	FSLB	FSLA	CPU(MHZ)
0	0	1	133.33
1	0	1	100

Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Clock Gen_ICS9LPR427	
	Engineer: Hauld Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 6 of 51	

H_D#[63:0] 9
H_DINV#[3:0] 9
H_DSTBN#[3:0] 9
H_DSTBP#[3:0] 9

HC1 2 1 10PF/50V /X CLK_BCLK_CPU
HC2 2 1 10PF/50V /X CLK_BCLK_CPU#
GND

H_CPUSLP# HR1 1 2 0Ohm
HR2 1 2 0Ohm /X
N_CPUSLP# 9
S_CPUSLP# 14

U16A

H_D#15 C25 D[15]# D[47]# Y25 H_D#47
H_D#14 E23 D[14]# D[46]# AA26 H_D#46
H_D#13 B23 D[13]# D[45]# Y23 H_D#45
H_D#12 C26 D[12]# D[44]# V26 H_D#44
H_D#11 E24 D[11]# D[43]# U25 H_D#43
H_D#10 D24 D[10]# D[42]# V24 H_D#42
H_D#9 B24 D[9]# D[41]# U26 H_D#41
H_D#8 C20 D[8]# D[40]# AA23 H_D#40
H_D#7 B20 D[7]# D[39]# R23 H_D#39
H_D#6 A21 D[6]# D[38]# R26 H_D#38
H_D#5 B26 D[5]# D[37]# R24 H_D#37
H_D#4 A24 D[4]# D[36]# V23 H_D#36
H_D#3 B21 D[3]# D[35]# U23 H_D#35
H_D#2 A22 D[2]# D[34]# T25 H_D#34
H_D#1 A25 D[1]# D[33]# AA24 H_D#33
H_D#0 A19 D[0]# D[32]# Y26 H_D#32
H_DINV#0 D25 DINV[0]# DINV[2]# T24 H_DINV#2
H_DSTBN#0 C23 DSTBN[0]# DSTBN[2]# W25 H_DSTBN#2
H_DSTBP#0 C22 DSTBP[0]# DSTBP[2]# W24 H_DSTBP#2

H_D#31 K25 D[31]# D[63]# AF26 H_D#63
H_D#30 N25 D[30]# D[62]# AF22 H_D#62
H_D#29 H26 D[29]# D[61]# AF25 H_D#61
H_D#28 M25 D[28]# D[60]# AD21 H_D#60
H_D#27 N24 D[27]# D[59]# AE21 H_D#59
H_D#26 L26 D[26]# D[58]# AF20 H_D#58
H_D#25 J25 D[25]# D[57]# AD24 H_D#57
H_D#24 M23 D[24]# D[56]# AF23 H_D#56
H_D#23 J23 D[23]# D[55]# AE22 H_D#55
H_D#22 G24 D[22]# D[54]# AD23 H_D#54
H_D#21 F25 D[21]# D[53]# AC25 H_D#53
H_D#20 H24 D[20]# D[52]# AC22 H_D#52
H_D#19 M26 D[19]# D[51]# AC20 H_D#51
H_D#18 L23 D[18]# D[50]# AB24 H_D#50
H_D#17 G25 D[17]# D[49]# AC23 H_D#49
H_D#16 H23 D[16]# D[48]# AB25 H_D#48
H_DINV#1 J26 DINV[1]# DINV[3]# AD20 H_DINV#3
H_DSTBN#1 K24 DSTBN[1]# DSTBN[3]# AE24 H_DSTBN#3
H_DSTBP#1 L24 DSTBP[1]# DSTBP[3]# AE25 H_DSTBP#3

DATA GROUP 0 DATA GROUP 2 DATA GROUP 1 DATA GROUP 3

860555INT_FCBGA479
01G011920001PM

U16C

6 CLK_BCLK_CPU B15 BCLK[0]
6 CLK_BCLK_CPU# B14 BCLK[1]
H_ITP_CLK A16 ITP_CLK[0]
H_ITP_CLK# A15 ITP_CLK[1]
HOSTCLK

HR3 1 2 49.9Ohm 1%
HR5 1 2 49.9Ohm 1%
GND

14 H_A20M# C2 A20M#
14 H_FERR# D3 FERR#
14 H_IGNNE# A3 IGNNE#
14 H_DPSLP# B7 DPSLP#
H_CPUSLP# A6 SLP#
14 H_INTR D1 LINT0
14 H_NMI D4 LINT1
14 H_SMI# B4 SMI#
14 H_STPCLK# C6 STPCLK#
LEGACY CPU

+VCCP
HR9 200Ohm 1%
14 H_PWRGD E4 PWRGOOD
HC3 0.1UF/16V
GND

H4 VID[5]
G4 VID[4]
G3 VID[3]
F3 VID[2]
F2 VID[1]
E2 VID[0]

COMP[3] AB1 H_COMP3 HR4 1 2 54.9Ohm 1%
COMP[2] AB2 H_COMP2 HR6 1 2 27.4Ohm 1%
COMP[1] P26 H_COMP1 HR7 1 2 54.9Ohm 1%
COMP[0] P25 H_COMP0 HR8 1 2 27.4Ohm 1%
GND

BPM[3]# C9 H_BPM#3
BPM[2]# A9 H_BPM#2
BPM[1]# B8 H_BPM#1
BPM[0]# C8 H_BPM#0

GTLREF[3] AC1 H_GTLREF3 1 TPC26T T1
GTLREF[2] G1 H_GTLREF2 HR10 1 2 0Ohm /X H_DPRSTP# 14
GTLREF[1] E26 H_GTLREF1 1
GTLREF[0] AD26 H_GTLREF TPC26T T2

TEST1 C5 H_TEST1 HR11 1 2 1KOhm 1% /X
TEST2 F23 H_TEST2 HR12 1 2 1KOhm 1% /X
GND

+VCCP
HR13 1KOhm 1%
H_GTLREF
HR15 2KOhm 1%
HC4 0.1UF/16V
GND GND

+VCCP +VCCA T3 TPC26T 1 H_VCCA3 AC26 VCCA[3]
T177TPC26T 1 H_VCCA2 N1 VCCA[2]
T178TPC26T 1 H_VCCA1 B1 VCCA[1]
F26 VCCA[0]
MISC

HR14 56OHM /900/X
For Dothan 800

39 H_THERMDA B18 THERMDA
39 H_THERMDC A18 THERMDC
9,14 H_THERMTRIP# C17 THERMTRIP#
H_PROCHOT# B17 PROCHOT#

T170 TPC26T 1 PM_PSI# F1
T4 TPC26T 1 CPU_BSEL0 C16 RSVD5
T5 TPC26T 1 H_RSVD3 G3 RSVD4
T6 TPC26T 1 CPU_BSEL1 C14 RSVD3
T7 TPC26T 1 H_RSVD1 AF7 RSVD2
T8 TPC26T 1 H_RSVD0 B2 RSVD1
RSVD0

TCK A13 H_TCK
TDI C12 H_TDI
TDO A12 H_TDO
TMS C11 H_TMS
TRST# B13 H_TRST#

VCCSENSE AE7 H_VCCSENSE HR16 1 /X 2 54.9Ohm 1%
VSSSENSE AF6 H_VSSSENSE HR17 1 /X 2 54.9Ohm 1%
GND

U16 use 01G011920000PM

U16B

H_A#16 AA2 A[16]# ADS# N2 H_ADS# 9
H_A#15 Y3 A[15]# PRDY# A10 H_BPM#4
H_A#14 AA3 A[14]# PREQ# B10 H_BPM#5
H_A#13 U1 A[13]#
H_A#12 Y1 A[12]# BNR# L1 H_BNR# 9
H_A#11 Y4 A[11]# BPRI# J3 H_BPRI# 9
H_A#10 W2 A[10]#
H_A#9 T4 A[9]# DBR# A7 H_DBR# 1 TPC26T T9
H_A#8 W1 A[8]#
H_A#7 V2 A[7]# DEFER# L4 H_DEFER# 9
H_A#6 R3 A[6]# DRDY# H2 H_DRDY# 9
H_A#5 V3 A[5]# DBSY# M2 H_DBSY# 9
H_A#4 U4 A[4]#
H_A#3 P4 A[3]#
9 H_ADSTB#0 U3 ADSTB[0]#
H_REQ#4 T1 REQ[4]#
H_REQ#3 P1 REQ[3]#
H_REQ#2 T2 REQ[2]#
H_REQ#1 P3 REQ[1]#
H_REQ#0 R2 REQ[0]#
ADDRESS GROUP 0

H_A#[31:3] 9
H_REQ#[4:0] 9

CONTROL BR0# N4 H_BR0# 9
IERR# A4 H_IERR#
INIT# B5 H_INIT# 14
LOCK# J2 H_LOCK# 9
H_RS#[2:0] 9

H_A#31 AE1 A[31]#
H_A#30 AE1 A[30]#
H_A#29 AF3 A[29]#
H_A#28 AD6 A[28]#
H_A#27 AE2 A[27]#
H_A#26 AD5 A[26]#
H_A#25 AC6 A[25]#
H_A#24 AB4 A[24]#
H_A#23 AD2 A[23]#
H_A#22 AE4 A[22]#
H_A#21 AD3 A[21]#
H_A#20 AC3 A[20]#
H_A#19 AC7 A[19]#
H_A#18 AC4 A[18]#
H_A#17 AF4 A[17]#
9 H_ADSTB#1 AE5 ADSTB[1]#
ADDRESS GROUP 1

RESET# B11 H_CPURST# 9
RS[2]# L2 H_RS#2
RS[1]# K1 H_RS#1
RS[0]# H1 H_RS#0
TRDY# M3 H_TRDY# 9
HIT# K3 H_HIT# 9
HITM# K4 H_HITM# 9

9 H_DPWR# C19 DPWR#

860555INT_FCBGA479
01G011920001PM

+VCCP
HR28 54.9Ohm 1%

+VCCP
HR24 56OHM /X
HC7 0.1UF/16V /X
GND

+1.5VS HR18 0Ohm r0603_h24
+VCCA 120 mA
HC5 22UF/6.3V /X
HC6 0.1UF/16V
GND

Close to CPU

H_BPM#0 3 51OHM 4 HRN10B /XDP
H_BPM#1 1 51OHM 2 HRN10A /XDP
H_BPM#2 7 51OHM 8 HRN10D /XDP
H_BPM#3 5 51OHM 6 HRN10C /XDP
H_BPM#4 HR90 1 2 51Ohm /XDP

+VCCP
H_BPM#5 HR20 1 2 54.9Ohm 1%
H_TDO HR21 1 2 56OHM /XDP

H_TMS 1 56Ohm 2 HRN1A
H_TDI 3 56Ohm 4 HRN1B
H_TCK 5 56Ohm 6 HRN1C
H_TRST# 7 56Ohm 8 HRN1D
GND

+VCCP
HR91 62Ohm /XDP/X
H_PWRGD 1 2 XDP_PWRGD
TESTIN#

XDP

GND1 2 1 H_BPM#5
BPM3# 4 3 H_BPM#4
BPM2# 6 5 GND5
GND2 8 7 H_BPM#1
PWRGOOD 10 9 H_BPM#0
RESERVED 12 11
VTT 14 13 CLK_BCLK_ITP 6
GCLKp 16 15 CLK_BCLK_ITP# 6
GCLKn 18 17
GND3 20 19 H_CPURST#
SCL 22 21 SYS_RESET# 6,14
15,25 SMB_CLK SDA 24 23 H_TDO
15,25 SMB_DATA GND4 26 25 H_TRST#
NC 28 27
H_TCK TCK 30 29 H_TDI
31 H_TMS
BTOB_CON_31P
/XDP/X

BPM5# BPM4# GND5 BPM1# BPM0# GND6 BCLK0 BCKL1 GND7 RESET# DBR# TRST# GND8 TDI TMS

HR22 0Ohm /XDP

+VCCP
HR25 0Ohm /XDP
H_BPM#3
H_BPM#2

GND
Default Group-A7V8X MX

ASUSTek Computer INC.
Title : Dothan_HOST
Engineer: Kell_Huang
Size A3
Project Name 900SD_MB
Rev R1.0G
Date: Monday, November 10, 2008
Sheet 7 of 51

+VCCP 2.5 A

+VCORE

Celeron-M(Dothan) ULV max 7 A

U16D

VCC

860555INT_FCBGA479
01G011920001PM

+VCORE

HCE1 10UF/6.3V N/A c0805

HCE2 100U/2.5V /CAP/X

HCE3 10UF/6.3V /X c0603

HCE4 100U/2.5V /CAP/X

GND

900SD R1.0G

0.1U All X7R

HC23 0.1UF/16V /CAP/X

HC24 0.1UF/16V

HC26 0.1UF/16V /CAP/X

HC27 10UF/6.3V

HC28 10UF/6.3V /CAP/X

HC29 10UF/6.3V

HC20 0.1UF/16V

HC21 0.1UF/16V

HC22 0.1UF/16V /CAP/X

HC25 0.1UF/16V

HC10 10UF/6.3V /CAP/X

HC11 10UF/6.3V /CAP/X

HC12 10UF/6.3V

HC13 10UF/6.3V

HC14 10UF/6.3V /CAP/X

HC15 10UF/6.3V /CAP/X

HC16 10UF/6.3V /CAP/X

HC17 10UF/6.3V /CAP/X c0805

HC18 10UF/6.3V /CAP/X

U16E

GND

860555INT_FCBGA479
01G011920001PM

Default Group-A7V8X MX

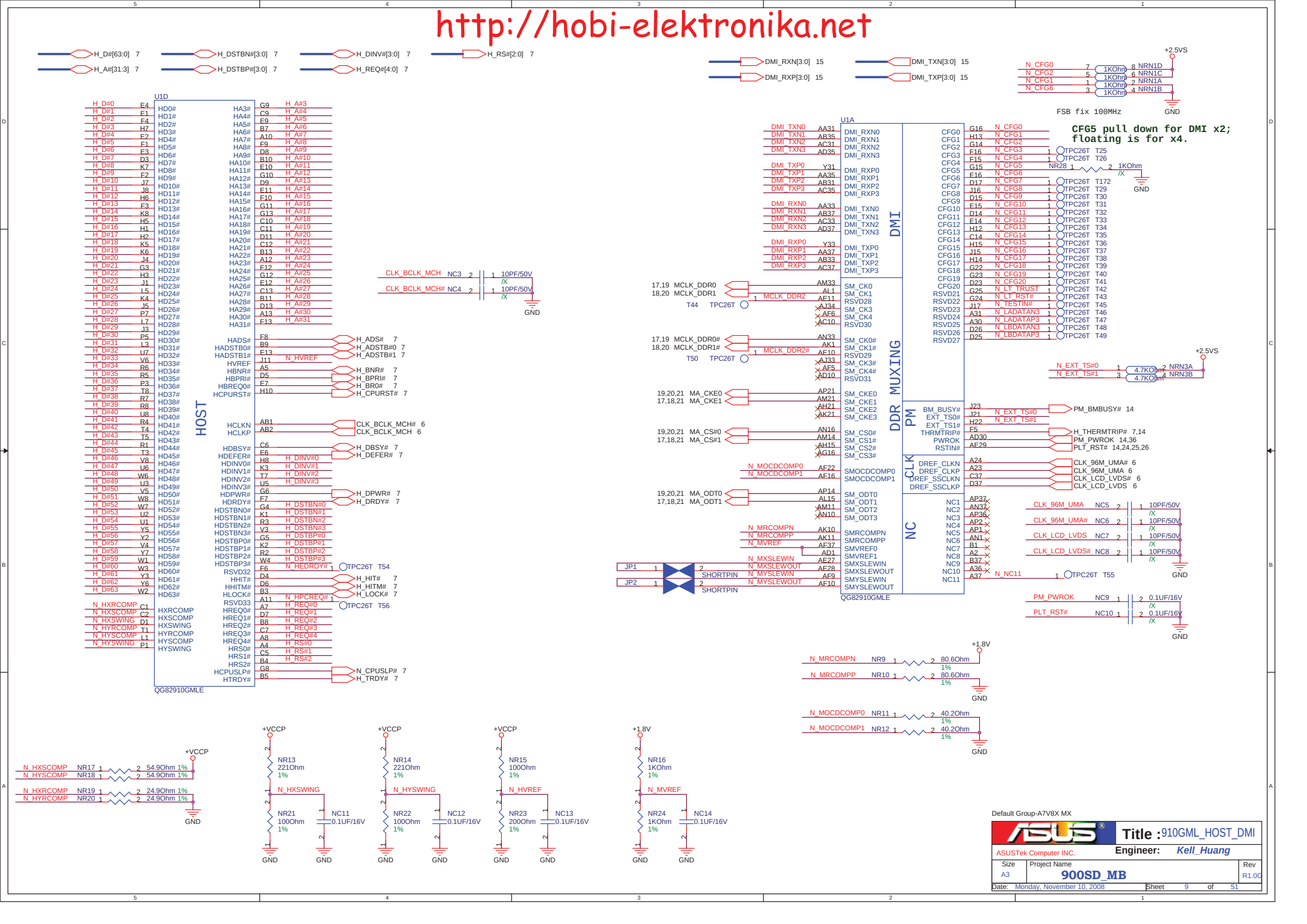
ASUSTek Computer INC.

Title : Dothan_PWR_GND

Engineer: Kell_Huang

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 8 of 51



MA_DQ[63:0] 17,18,19,20
MA_DQS[7:0] 17,18,19,20
MA_DQS#[7:0] 17,18,19,20
MA_DM[7:0] 17,18,19,20
MA_MA[13:0] 17,18,19,20,21
MA_BA[2:0] 17,18,19,20,21

U1B

DDR SYSTEM MEMORY A

MA_DQ0	AG35	SA_DQ0	SA_BS0	AK15	MA_BA0
MA_DQ1	AH35	SA_DQ1	SA_BS1	AK16	MA_BA1
MA_DQ2	AL35	SA_DQ2	SA_BS2	AL21	MA_BA2
MA_DQ3	AL37	SA_DQ3			
MA_DQ4	AH36	SA_DQ4	SA_DM0	AJ37	MA_DM0
MA_DQ5	AJ35	SA_DQ5	SA_DM1	AP35	MA_DM1
MA_DQ6	AK37	SA_DQ6	SA_DM2	AL29	MA_DM2
MA_DQ7	AL34	SA_DQ7	SA_DM3	AP24	MA_DM3
MA_DQ8	AM36	SA_DQ8	SA_DM4	AP9	MA_DM4
MA_DQ9	AN35	SA_DQ9	SA_DM5	AP4	MA_DM5
MA_DQ10	AP32	SA_DQ10	SA_DM6	AJ2	MA_DM6
MA_DQ11	AM31	SA_DQ11	SA_DM7	AD3	MA_DM7
MA_DQ12	AM34	SA_DQ12			
MA_DQ13	AM35	SA_DQ13	SA_DQS0	AK36	MA_DQS0
MA_DQ14	AL32	SA_DQ14	SA_DQS1	AP33	MA_DQS1
MA_DQ15	AM32	SA_DQ15	SA_DQS2	AN29	MA_DQS2
MA_DQ16	AN31	SA_DQ16	SA_DQS3	AP23	MA_DQS3
MA_DQ17	AP31	SA_DQ17	SA_DQS4	AM8	MA_DQS4
MA_DQ18	AN28	SA_DQ18	SA_DQS5	AM4	MA_DQS5
MA_DQ19	AP28	SA_DQ19	SA_DQS6	AJ1	MA_DQS6
MA_DQ20	AL30	SA_DQ20	SA_DQS7	AE5	MA_DQS7
MA_DQ21	AM30	SA_DQ21			
MA_DQ22	AM28	SA_DQ22	SA_DQS0#	AK35	MA_DQS#0
MA_DQ23	AL28	SA_DQ23	SA_DQS1#	AP34	MA_DQS#1
MA_DQ24	AP27	SA_DQ24	SA_DQS2#	AN30	MA_DQS#2
MA_DQ25	AM27	SA_DQ25	SA_DQS3#	AN23	MA_DQS#3
MA_DQ26	AM23	SA_DQ26	SA_DQS4#	AN8	MA_DQS#4
MA_DQ27	AM22	SA_DQ27	SA_DQS5#	AM5	MA_DQS#5
MA_DQ28	AL23	SA_DQ28	SA_DQS6#	AH1	MA_DQS#6
MA_DQ29	AM24	SA_DQ29	SA_DQS7#	AE4	MA_DQS#7
MA_DQ30	AN22	SA_DQ30			
MA_DQ31	AP22	SA_DQ31	SA_MA0	AL17	MA_MA0
MA_DQ32	AM9	SA_DQ32	SA_MA1	AP17	MA_MA1
MA_DQ33	AL9	SA_DQ33	SA_MA2	AP18	MA_MA2
MA_DQ34	AL6	SA_DQ34	SA_MA3	AM17	MA_MA3
MA_DQ35	AP7	SA_DQ35	SA_MA4	AN18	MA_MA4
MA_DQ36	AP11	SA_DQ36	SA_MA5	AM18	MA_MA5
MA_DQ37	AP10	SA_DQ37	SA_MA6	AL19	MA_MA6
MA_DQ38	AL7	SA_DQ38	SA_MA7	AP20	MA_MA7
MA_DQ39	AM7	SA_DQ39	SA_MA8	AM19	MA_MA8
MA_DQ40	AN5	SA_DQ40	SA_MA9	AL20	MA_MA9
MA_DQ41	AN6	SA_DQ41	SA_MA10	AM16	MA_MA10
MA_DQ42	AN3	SA_DQ42	SA_MA11	AN20	MA_MA11
MA_DQ43	AP3	SA_DQ43	SA_MA12	AM20	MA_MA12
MA_DQ44	AP6	SA_DQ44	SA_MA13	AM15	MA_MA13
MA_DQ45	AM6	SA_DQ45			
MA_DQ46	AL4	SA_DQ46	SA_CAS#	AN15	MA_CAS# 17,18,19,20,21
MA_DQ47	AM3	SA_DQ47	SA_RAS#	AP16	MA_RAS# 17,18,19,20,21
MA_DQ48	AK2	SA_DQ48	SA_RCVENIN#	AF29	MA_RCVENIN# 1 TPC26T T57
MA_DQ49	AK3	SA_DQ49	SA_RCVENOUT#	AF28	MA_RCVENOUT# 1 TPC26T T58
MA_DQ50	AG2	SA_DQ50	SA_WE#	AP15	MA_WE# 17,18,19,20,21
MA_DQ51	AG1	SA_DQ51			
MA_DQ52	AL3	SA_DQ52			
MA_DQ53	AM2	SA_DQ53			
MA_DQ54	AH3	SA_DQ54			
MA_DQ55	AG3	SA_DQ55			
MA_DQ56	AF3	SA_DQ56			
MA_DQ57	AE3	SA_DQ57			
MA_DQ58	AD6	SA_DQ58			
MA_DQ59	AC4	SA_DQ59			
MA_DQ60	AE2	SA_DQ60			
MA_DQ61	AF1	SA_DQ61			
MA_DQ62	AD4	SA_DQ62			
MA_DQ63	AD5	SA_DQ63			

QG82910GMLE

U1C

DDR SYSTEM MEMORY B

AE31	SB_DQ0	SB_BS0	AJ15	
AE32	SB_DQ1	SB_BS1	AG17	
AG32	SB_DQ2	SB_BS2	AG21	
AG36	SB_DQ3			
AE34	SB_DQ4	SB_DM0	AF32	
AE33	SB_DQ5	SB_DM1	AK34	
AE31	SB_DQ6	SB_DM2	AK27	
AE30	SB_DQ7	SB_DM3	AK24	
AH33	SB_DQ8	SB_DM4	AJ10	
AH32	SB_DQ9	SB_DM5	AK5	
AK31	SB_DQ10	SB_DM6	AE7	
AG30	SB_DQ11	SB_DM7	AB7	
AG34	SB_DQ12			
AG33	SB_DQ13	SB_DQS0	AF34	
AH31	SB_DQ14	SB_DQS1	AK32	
AJ31	SB_DQ15	SB_DQS2	AJ28	
AK30	SB_DQ16	SB_DQS3	AK23	
AJ30	SB_DQ17	SB_DQS4	AM10	
AH29	SB_DQ18	SB_DQS5	AH6	
AH28	SB_DQ19	SB_DQS6	AF8	
AK29	SB_DQ20	SB_DQS7	AB4	
AH30	SB_DQ21			
AH27	SB_DQ22	SB_DQS0#	AF35	
AG28	SB_DQ23	SB_DQS1#	AK33	
AF24	SB_DQ24	SB_DQS2#	AK28	
AG23	SB_DQ25	SB_DQS3#	AJ23	
AJ22	SB_DQ26	SB_DQS4#	AL10	
AK22	SB_DQ27	SB_DQS5#	AH7	
AH24	SB_DQ28	SB_DQS6#	AF7	
AH23	SB_DQ29	SB_DQS7#	AB5	
AG22	SB_DQ30			
AJ21	SB_DQ31	SB_MA0	AH17	
AG10	SB_DQ32	SB_MA1	AK17	
AG9	SB_DQ33	SB_MA2	AH18	
AG8	SB_DQ34	SB_MA3	AJ18	
AH8	SB_DQ35	SB_MA4	AK18	
AH11	SB_DQ36	SB_MA5	AJ19	
AH10	SB_DQ37	SB_MA6	AK19	
AJ9	SB_DQ38	SB_MA7	AH19	
AK9	SB_DQ39	SB_MA8	AJ20	
AJ7	SB_DQ40	SB_MA9	AH20	
AK6	SB_DQ41	SB_MA10	AJ16	
AJ4	SB_DQ42	SB_MA11	AG18	
AH5	SB_DQ43	SB_MA12	AG20	
AK8	SB_DQ44	SB_MA13	AG15	
AJ8	SB_DQ45			
AJ5	SB_DQ46	SB_CAS#	AH14	
AK4	SB_DQ47	SB_RAS#	AK14	
AG5	SB_DQ48	SB_RCVENIN#	AF15	
AG4	SB_DQ49	SB_RCVENOUT#	AF14	
AD8	SB_DQ50	SB_WE#	AH16	
AD9	SB_DQ51			
AH4	SB_DQ52			
AG6	SB_DQ53			
AE8	SB_DQ54			
AD7	SB_DQ55			
AC5	SB_DQ56			
AB8	SB_DQ57			
AB6	SB_DQ58			
AA8	SB_DQ59			
AC8	SB_DQ60			
AC7	SB_DQ61			
AA4	SB_DQ62			
AA5	SB_DQ63			

QG82910GMLE

Default Group-A7V8X MX

ASUSTek Computer INC.

Title : 910GML_DRAM

Engineer: Kell_Huang

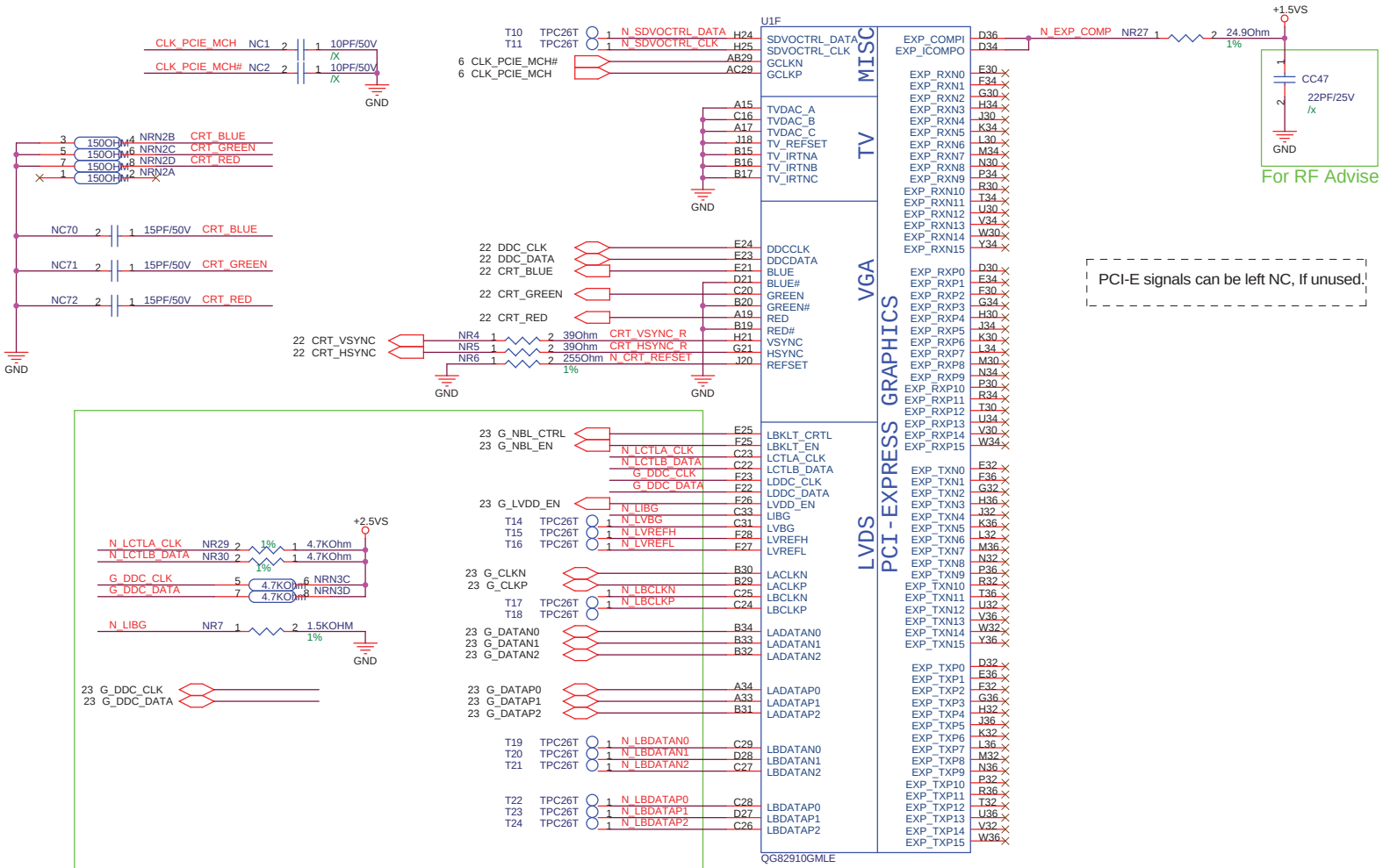
Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 10 of 51

SDVO SMbus have internal pull down

SDVOCRTL_DATA Int PD
0 : No SDVO device
1 : SDVO device present

U1 use 02G010007610



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : 910GML_VGA_LVDS	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 11 of 51	

U1 use 02G010007610

POWER

U1G
QG82910GMLE

+VCCP
+2.5VS
NR25
10Ohm
r0603_h24
ND1
BAT54CW
+1.5VS
+3VS
NR26
10Ohm
r0603_h24
ND2
BAT54CW

+1.5VS_DPLLB
40 mA
NL1
120Ohm/100Mhz
NC15 10uF/10V /CAP/X
NC16 0.1UF/16V
GND

+1.5VS_HOST_PLL
45 mA
NL2
120Ohm/100Mhz
NC17 0.1UF/16V
NC18 10uF/10V /CAP/X
GND

+1.5VS_DPLLA
40 mA
NL4
120Ohm/100Mhz
NC21 10uF/10V /CAP/X
NC22 0.1UF/16V
GND

+1.5VS_DRAM_PLL
45 mA
NL3
120Ohm/100Mhz
NC19 0.1UF/16V
NC20 10uF/10V /CAP/X
GND

+2.5VS_CRTDAC
68 mA
NR31
0Ohm
NC23 0.1UF/16V
NC24 22UF/6.3V /CAP/X
GND

+VCCP
1.05V 3700 mA
NC28 10uF/10V
NC29 10uF/10V /CAP/X
NC30 10uF/10V /CAP/X
NC31 0.1UF/16V
NC32 0.1UF/16V
NC33 0.1UF/16V
GND

+1.5VS
150 mA
NC34 10uF/10V /CAP/X
NC35 0.1UF/16V
GND

+2.5VS
2 mA
NC36 0.1UF/16V
GND

+VCCP
1.05V 640 mA
NC25 10uF/10V
NC26 10uF/10V /CAP/X
NC27 0.1UF/16V
GND

+VCCP_GMCH_CAP1
+VCCP_GMCH_CAP2
+VCCP_GMCH_CAP3
+VCCP_GMCH_CAP4
NC37 0.1UF/16V
NC38 0.1UF/16V
NC39 0.1UF/16V
NC40 0.1UF/16V
GND

+3VS_TV
+1.5VS_TV
GND

+1.8V_CAP3
+1.8V_CAP2
+1.8V_CAP1
+1.5VS
60 mA
NC53 10uF/10V /CAP/X
NC54 0.1UF/16V
GND
+2.5VS
10 mA
NC59 1UF/16V /CAP/X
NC60 0.1UF/16V
GND
+2.5VS
2 mA
NC55 0.1UF/16V
NC56 1UF/16V /CAP/X
GND
NC42 0.1UF/16V
NC43 0.1UF/16V
NC44 0.1UF/16V
GND

+1.8V
950 mA
NC45 10uF/10V
NC46 10uF/10V /CAP/X
NC47 0.1UF/16V
GND

+1.8V_CAP4
+1.8V_CAP5
+1.8V_CAP6
NC48 0.1UF/16V
NC49 0.1UF/16V
NC50 0.1UF/16V
GND
+2.5VS
60 mA
NC57 22UF/6.3V /CAP/X
NC58 0.1UF/16V
GND

+1.5VS
+1.5VS_DRAM
215 mA
NL8
120Ohm/100Mhz
NC64 10uF/10V
NC65 1UF/16V
NC66 0.1UF/16V
GND

+2.5VS
0.15 mA
NC41 0.1UF/16V
GND

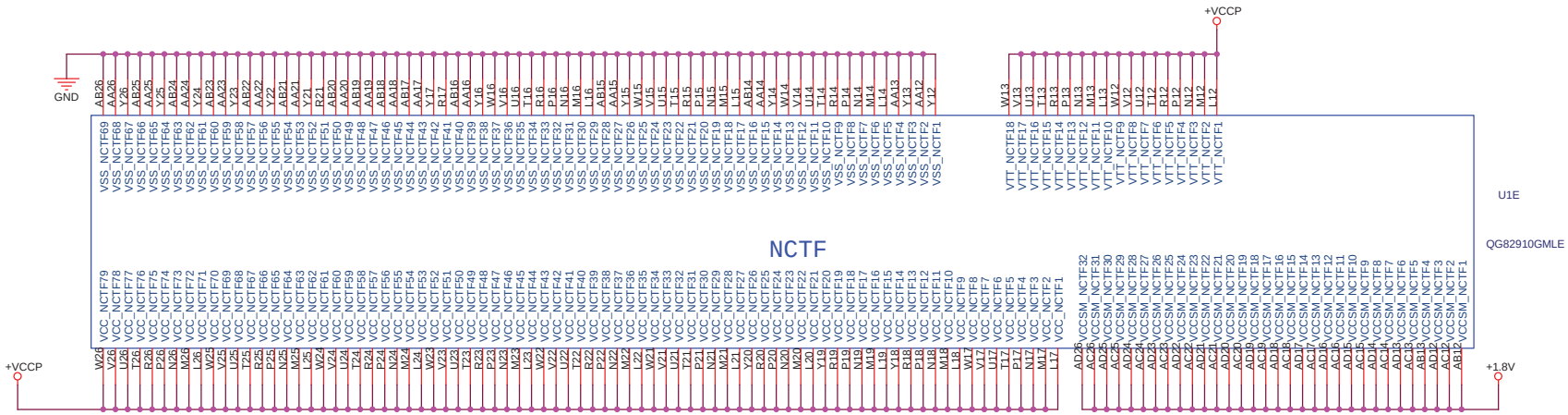
+1.5VS_NPCIE_PLL
NL6
120Ohm/100Mhz
NC51 0.1UF/16V
NC52 10uF/10V /CAP/X
GND
+1.5V_PCIE & +1.5V_PCIE_PLL total 1500 mA

+1.5VS
NC61 0.1UF/16V
NC62 10uF/10V /CAP/X
SC21 10uF/10V /CAP/X
GND

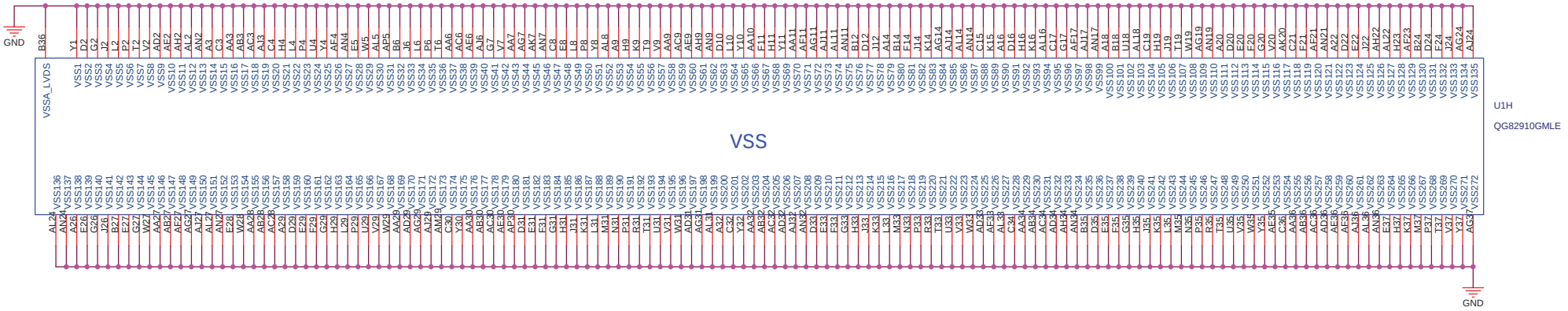
+3VS_TV
JP3
SHORTPIN
+1.5VS_TV
JP4
SHORTPIN
GND

Default Group-A7V8X MX

ASUSTek Computer INC.	Title : 910GML_PWR	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 12 of 51	

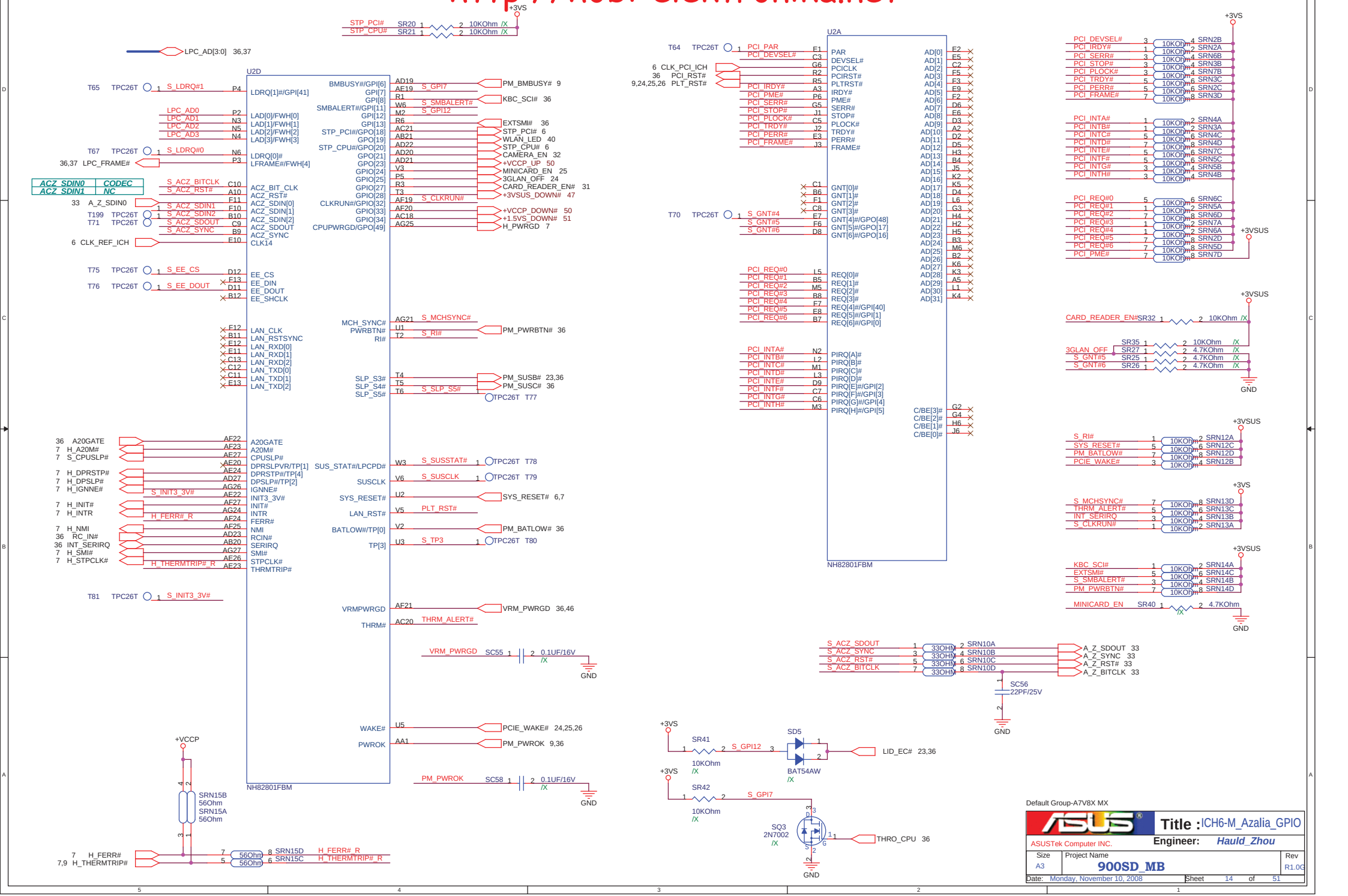


U1 use 02G010007612



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : 910GML_GND	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 13 of 51	



U2C

AD13 DD[15]
AG15 DD[14]
AE15 DD[13]
AC13 DD[12]
AB13 DD[11]
AB12 DD[10]
AE13 DD[9]
AE13 DD[8]
AB11 DD[7]
AD11 DD[6]
AC11 DD[5]
AE14 DD[4]
AD12 DD[3]
AF14 DD[2]
AE15 DD[1]
AD14 DD[0]

SATA[0]RXN AE3 S_SATA_RXN0 28
SATA[0]RXP AD3 S_SATA_RXP0 28
SATA[0]TXN AG2 S_SATA_TXN0 28
SATA[0]TXP AF2 S_SATA_TXP0 28
SATA[1]RXN/RESERVED AC5
SATA[1]RXP/RESERVED AD5
SATA[1]TXN/RESERVED AF4
SATA[1]TXP/RESERVED AG4
SATA[2]RXN AD7
SATA[2]RXP AC7
SATA[2]TXN AF6
SATA[2]TXP AG6
SATA[3]RXN/RESERVED AC9
SATA[3]RXP/RESERVED AD9
SATA[3]TXN/RESERVED AF8
SATA[3]TXP/RESERVED AG8

CLK_SATA_ICH# SC61 10PF/50V /X
CLK_SATA_ICH SC62 10PF/50V /X
GND

SATA_CLKN AC2 CLK_SATA_ICH# 6
SATA_CLKP AC1 CLK_SATA_ICH 6

+3VS
SR1 10KOhm 1% IDE_IORDY
AB15 DDACK#
AB14 DDREQ
AE16 DIOR#
AC14 DIOW#
AF16 IORDY

SATARBIAS# AG11 S_SATARBIAS
SATARBIAS AF11
SR44 24.9Ohm 1%
GND

AC16 DA[0]
AB17 DA[1]
AC17 DA[2]

SMBCLK Y4 S_SMB_CLK 6
SMBDATA W5 S_SMB_DATA 6

AD16 DCS1#
AE17 DCS3#

+3VS
SRN9D 10KOhm IDE_IRQ
AB16 IDEIRQ

LINKALERT# Y5 S_LINKALERT# SRN9C
SMLINK[0] W4 S_SMLINK0 SRN9B
SMLINK[1] U6 S_SMLINK1 SRN9A
10KOhm
+3VSUS

SATALED# AC19
SATA[0]GP/GPI[26] AF17 MEM_DET0 SIMCARD_IN# 24
SATA[1]GP/GPI[29] AE18 PCBA
SATA[2]GP/GPI[30] AF18 MEM_DET1
SATA[3]GP/GPI[31] AG18
INTRUDER# AA3 S_INTRUDER# SR7 1MOhm +VCC_RTC

RSMRST# Y3 PM_RSMRST# 36
RTCX1 Y1 RTC_X1
RTCX2 Y2 RTC_X2
RTCRST# AA2 RTCRST#
INTVRMEN AA5 S_INTVRMEN SR11 330KOhm +VCC_RTC
SPKR F8 SB_SPKR
SB_SPKR SR13 4.7KOhm /X +3VS

NH82801FBM

900SD 1.0G
+3VS
SR47 10KOhm 1% SIMCARD_IN#
SR48 10KOhm /X MEM_DET1
SR5 10KOhm /X MEM_DET0
SR45 10KOhm 1% PCBA
SR49 10KOhm 1%
SR6 10KOhm 1%
SR46 10KOhm /X
GND

SC9 15PF/50V RTC_X1
SX1 SIDE 32.768KHZ
SR15 10MOhm
SC11 15PF/50V RTC_X2
GND

PM_RSMRST# SC10 0.1UF/16V /X GND

S_SMB_CLK
S_SMB_DATA
SMB_CLK
SMB_DATA
4.7KOhm SRN8B SRN8A SRN8C SRN8D
+3VSUS +3VS

DMI_TXN[3:0] 9
DMI_TXP[3:0] 9
DMI_RXN[3:0] 9
DMI_RXP[3:0] 9

PCIE 1	WIMAX
PCIE 2	LAN
PCIE 3	WLAN
PCIE 4	NC

PCIE_RXN1 PCIE_RXP1 PCIE_TXN1 PCIE_TXP1
X_L1X1_RXN X_L1X1_RXP X_L1X1_TXN X_L1X1_TXP
PCIE_RXN3 PCIE_RXP3 PCIE_TXN3 PCIE_TXP3
C213 0.1UF/16V /WIMAX PCIE_TXN1_C
C214 0.1UF/16V /WIMAX PCIE_TXP1_C
SC1 0.1UF/16V PCIE_TXN2_C
SC2 0.1UF/16V PCIE_TXP2_C
SC3 0.1UF/16V PCIE_TXN3_C
SC4 0.1UF/16V PCIE_TXP3_C
GND

+1.5VS
SR4 24.9Ohm 1% S_DMI_COMP

CLK_PCIE_ICH SC5 10PF/50V /X
CLK_PCIE_ICH# SC6 10PF/50V /X
GND

6 CLK_PCIE_ICH#
6 CLK_PCIE_ICH

U2B

DMI_RXN0 DMI_RXP0 DMI_TXN0 DMI_TXP0 DMI_RXN1 DMI_RXP1 DMI_TXN1 DMI_TXP1 DMI_RXN2 DMI_RXP2 DMI_TXN2 DMI_TXP2 DMI_RXN3 DMI_RXP3 DMI_TXN3 DMI_TXP3
DMI[0]RXN DMI[0]RXP DMI[0]TXN DMI[0]TXP DMI[1]RXN DMI[1]RXP DMI[1]TXN DMI[1]TXP DMI[2]RXN DMI[2]RXP DMI[2]TXN DMI[2]TXP DMI[3]RXN DMI[3]RXP DMI[3]TXN DMI[3]TXP
PERn[1] PERp[1] PETn[1] PETp[1] PERn[2] PERp[2] PETn[2] PETp[2] PERn[3] PERp[3] PETn[3] PETp[3] PERn[4] PERp[4] PETn[4] PETp[4]
DMI_ZCOMP DMI_IRCOMP
AD25 DMI_CLKN
AC25 DMI_CLKP
NH82801FBM

USBP[0]N C21
USBP[0]P D21
USBP[1]N A20 U_USB1- 30
USBP[1]P B20 U_USB1+ 30
USBP[2]N D19 U_USB2- 30
USBP[2]P C19 U_USB2+ 30
USBP[3]N A18 U_USB3- 30
USBP[3]P B18 U_USB3+ 30
USBP[4]N E17 U_CARD- 31
USBP[4]P D17 U_CARD+ 31
USBP[5]N B16 U_3G- 24
USBP[5]P A16 U_3G+ 24
USBP[6]N C15
USBP[6]P D15
USBP[7]N A14 U_CAM- 32
USBP[7]P B14 U_CAM+ 32

OC[0]# C27 USB_OC#01 30
OC[1]# B27
OC[2]# B26 USB_OC#23 30
OC[3]# C26
OC[4]#/GPI[9] C23 USB_OC#4
OC[5]#/GPI[10] D23 USB_OC#5
OC[6]#/GPI[14] C25 USB_OC#6
OC[7]#/GPI[15] C24 USB_OC#7

USBRBIAS B22 S_USBRBIAS SR2 22.6Ohm 1%
USBRBIAS# A22
GND

+3VSUS
USB_OC#4 USB_OC#5 USB_OC#6 USB_OC#7
10KOhm SRN1A SRN1B SRN1C SRN1D

CLK48 A27 CLK_48M_USB 6

USB 0	NC
USB 1	USB Conn
USB 2	USB Conn
USB 3	USB Conn
USB 4	Card Reader
USB 5	3G
USB 6	NC
USB 7	Camera

+3VA
BAT WTOB_CON_2P
+VCC_BAT
SR12 1KOhm
SD1 BAT54CW
+VCC_BAT_R
GND

+VCC_RTC
SR9 100KOHM
SC7 1UF/16V
RTCRST# RC delay 18~25ms
SC8 1UF/16V
RTCRST#
CLRTC SGL_JUMP
Place Near Open Door
GND

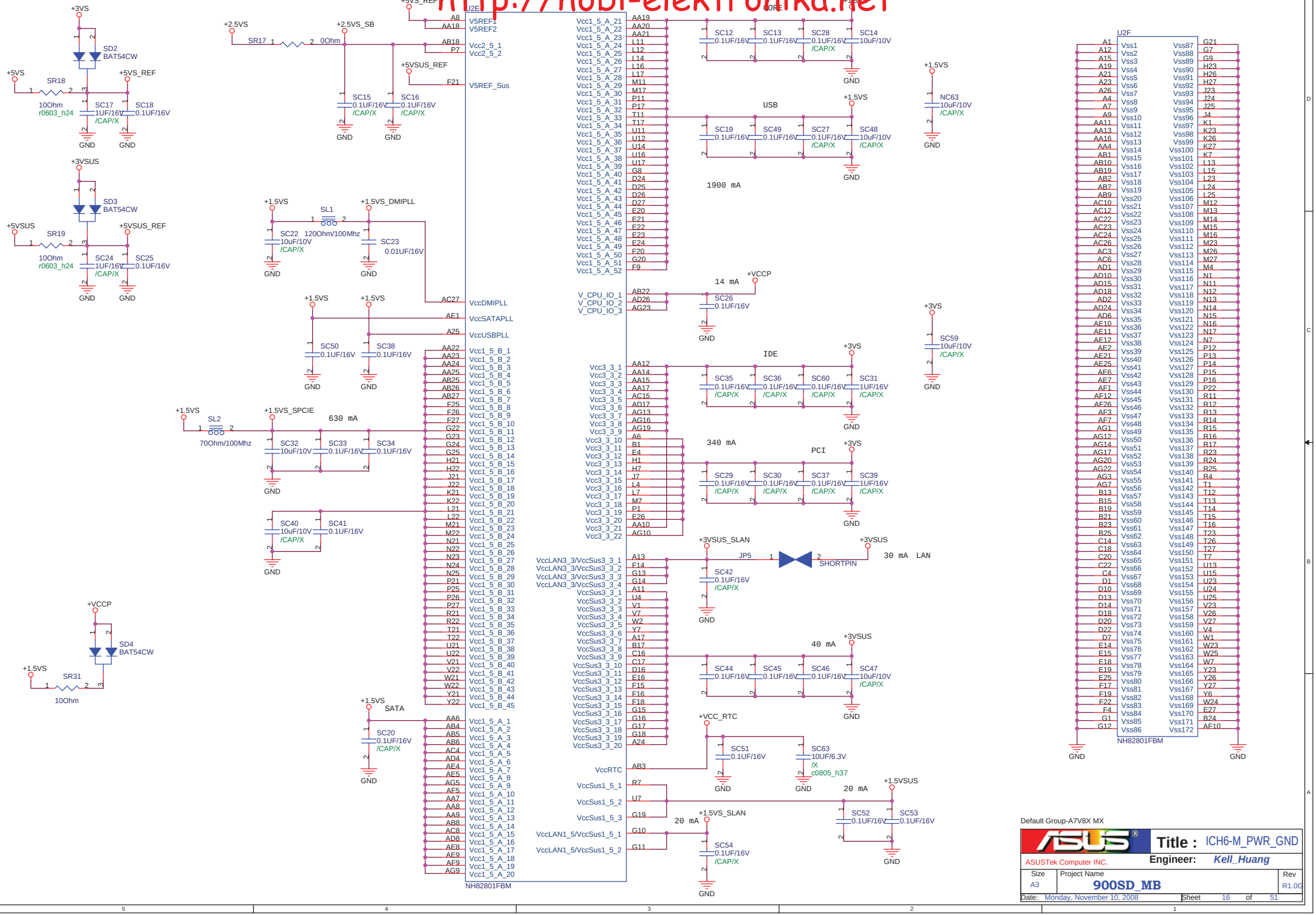
+5VS
S_SMB_CLK SQ1A SMB_CLK 7,25
UM6K1N
S_SMB_DATA SQ1B SMB_DATA 7,25
UM6K1N

Default Group-A7V8X MX

ASUSTek Computer INC.
Title : ICH6-M_USB_PCIE_IDE
Engineer: Hauld_Zhou

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 15 of 51



Default Group-A7V8X MX

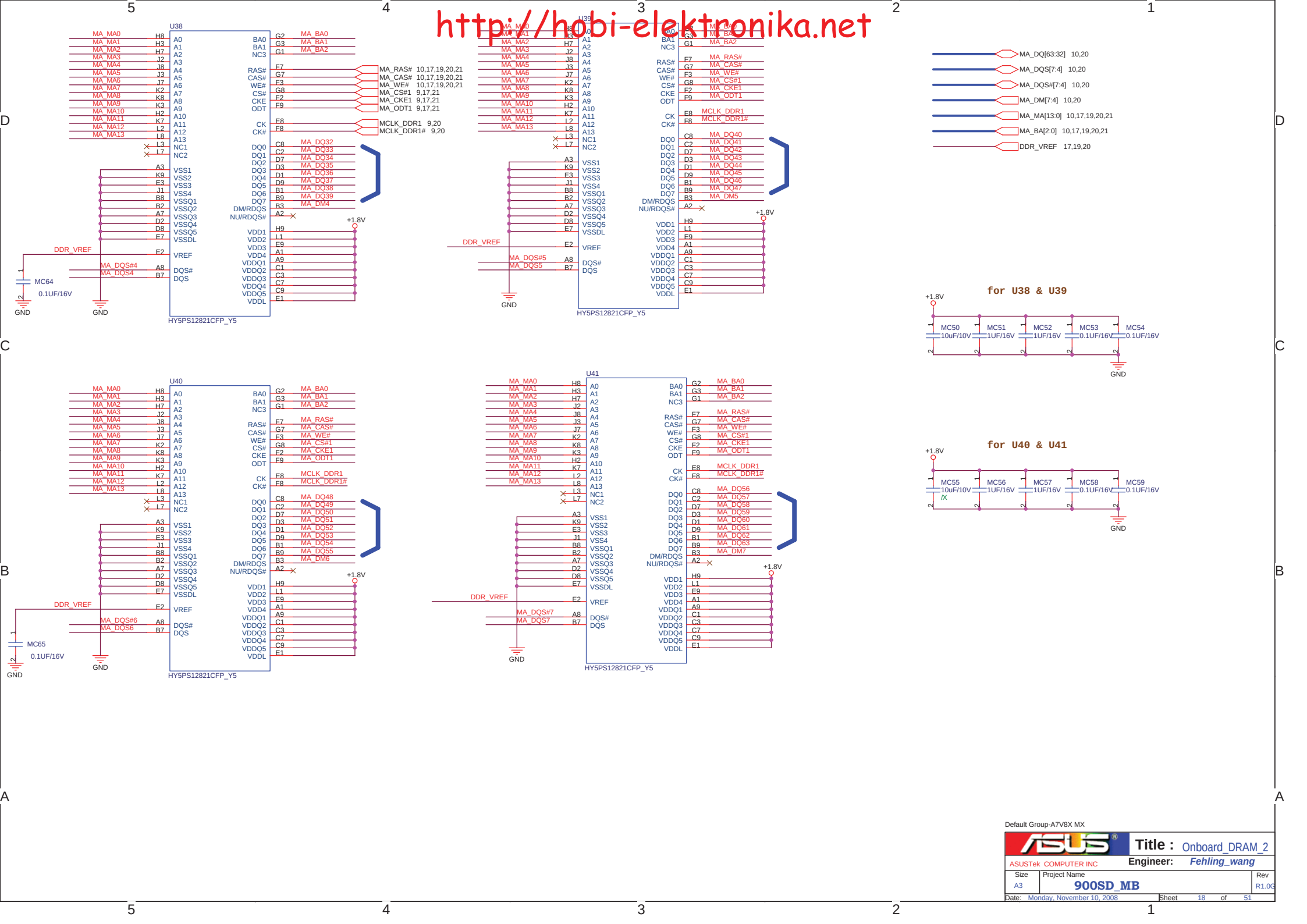
ASUSTek Computer INC.	Title : ICH6-M_PWR_GND	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 16 of 51	

for U34 & U35

for U36 & U37

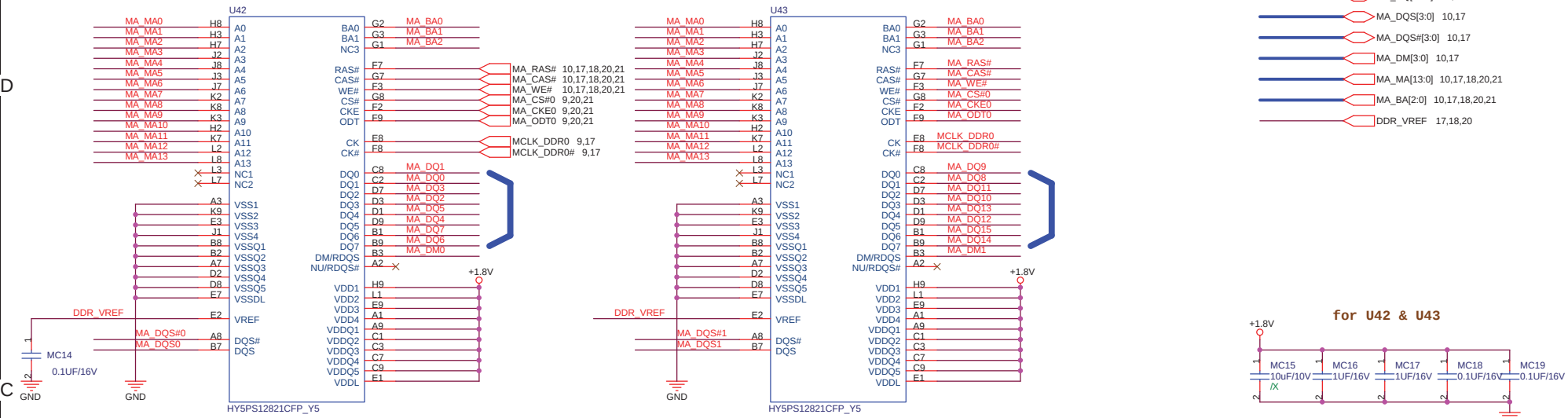
Default Group-A7V8X MX

ASUSTek COMPUTER INC	Title : Onboard_DRAM_1	
	Engineer: Fehling_wang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 17 of 51	

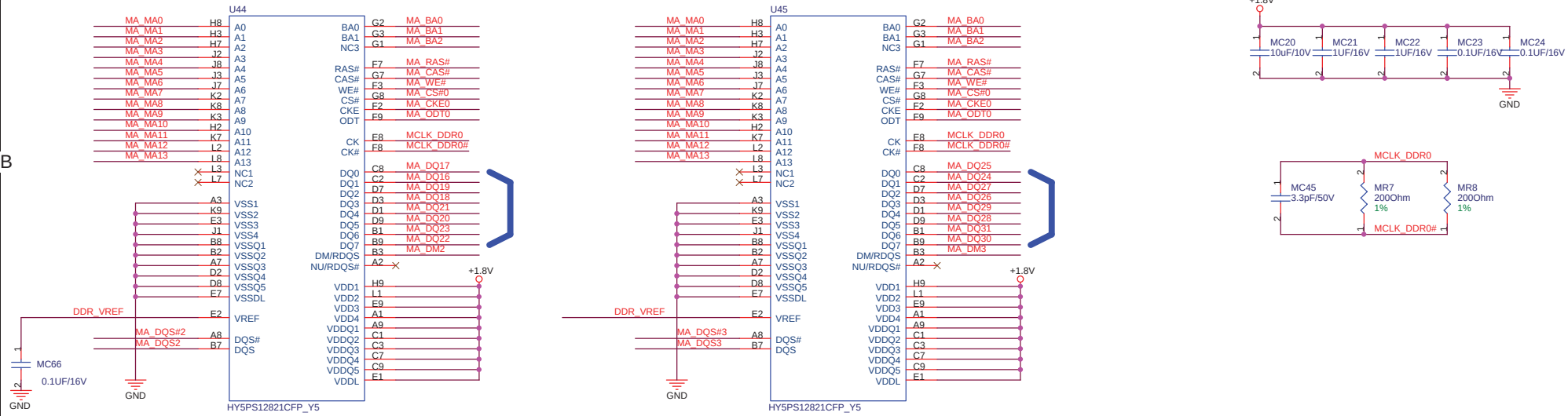


Default Group-A7V8X MX

ASUSTek COMPUTER INC	Title : Onboard_DRAM_2	
	Engineer: Fehling_wang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 18 of 51	



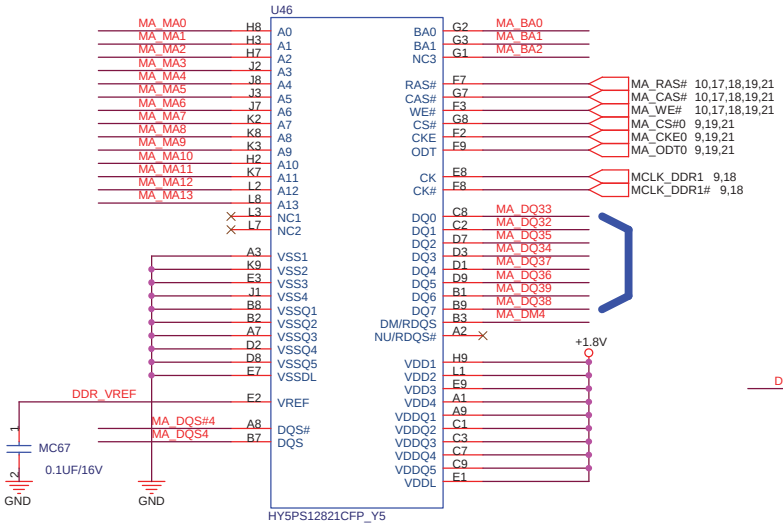
for U42 & U43

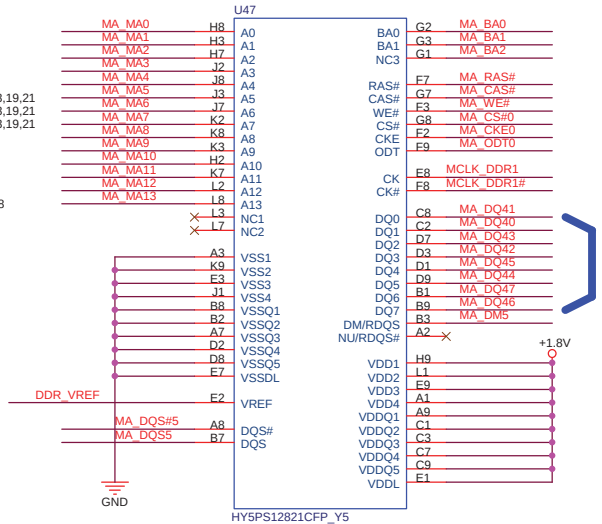


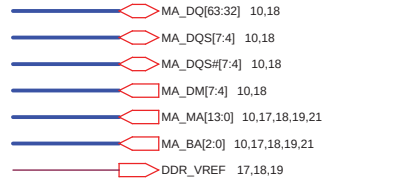
for U44 & U45

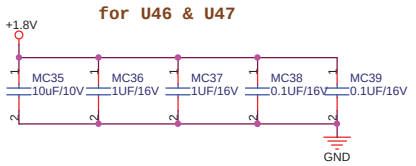
Default Group-A7V8X MX

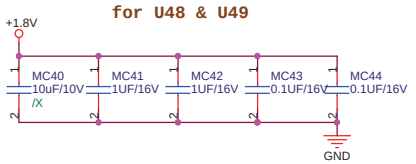
ASUSTek COMPUTER INC	Title : Onboard_DRAM_2	
	Engineer: Fehling_wang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 19 of 51	

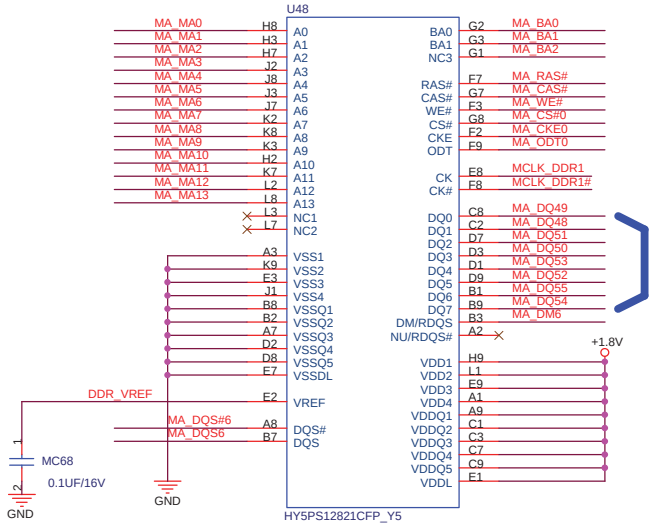


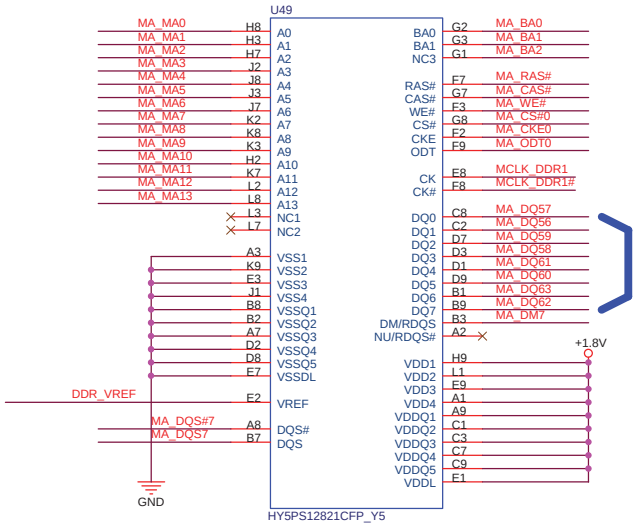


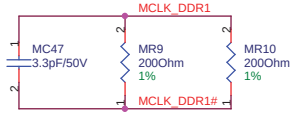


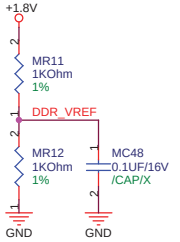






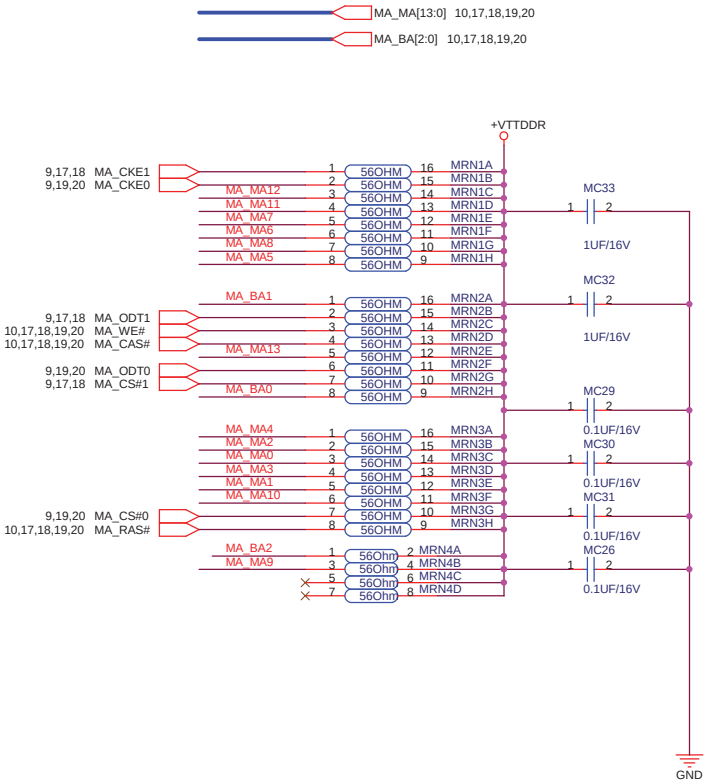






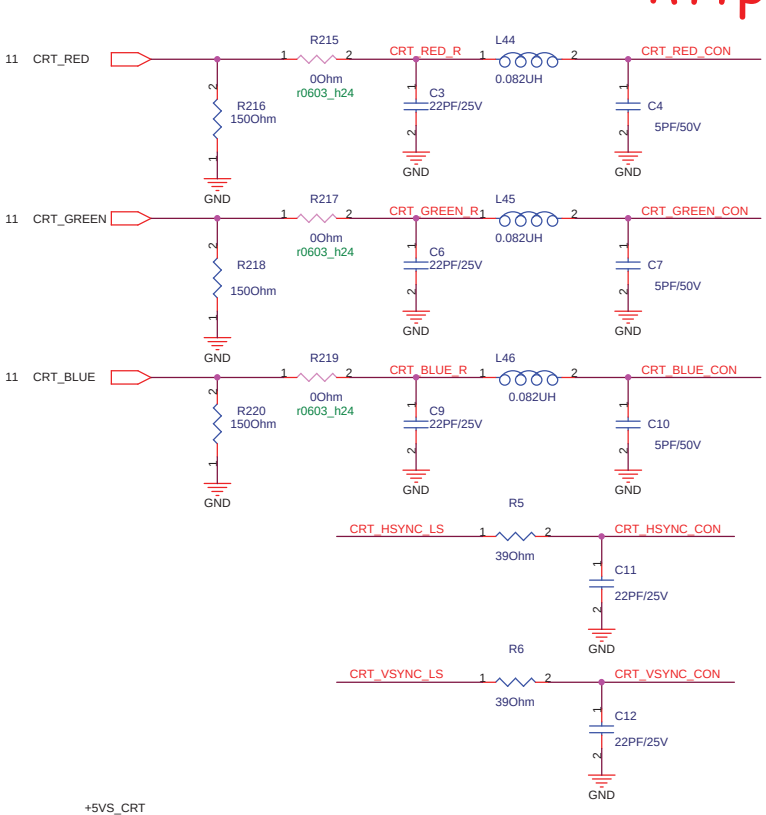
Default Group-A7V8X MX

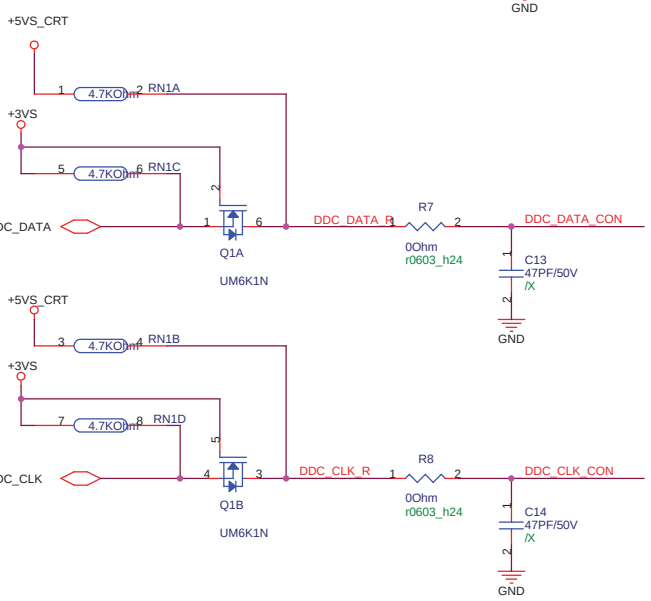
ASUSTek COMPUTER INC	Title : Onboard_DRAM_1	
	Engineer: Fehling_wang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 20 of 51	

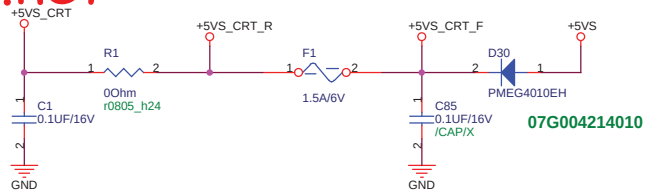


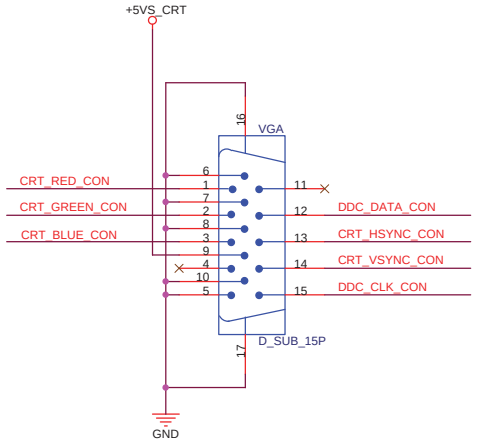
Default Group-A7V8X MX

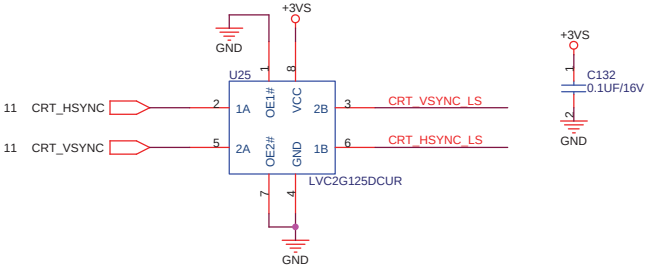
ASUSTek Computer INC.	Title : DDR2_Termination	
	Engineer: *Kell_Huang*	
Size: A3	Project Name: **900SD_MB**	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 21 of 51	

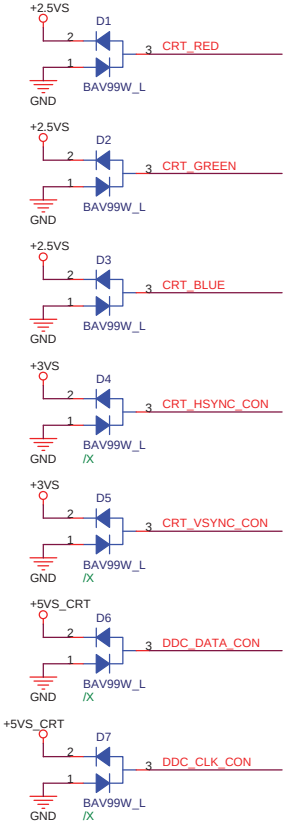








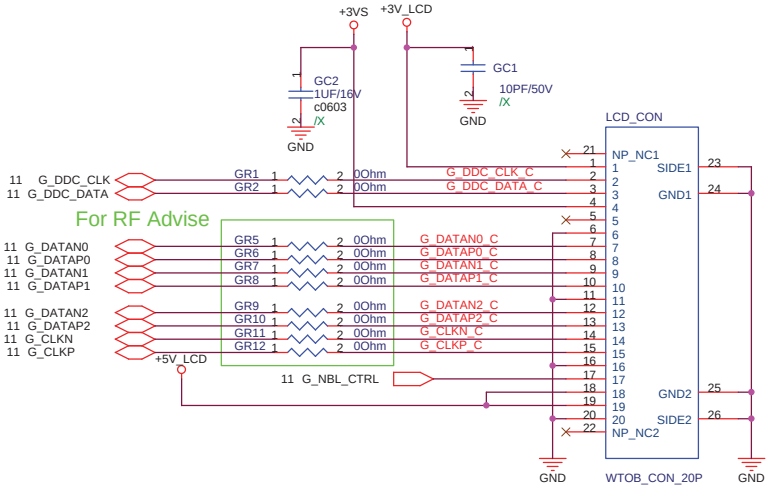


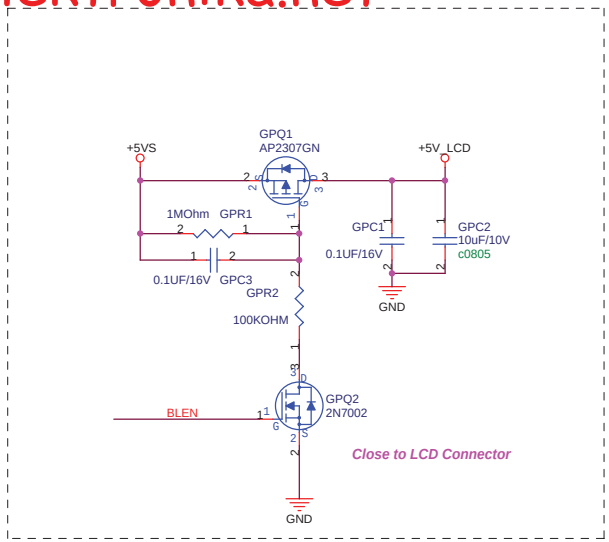


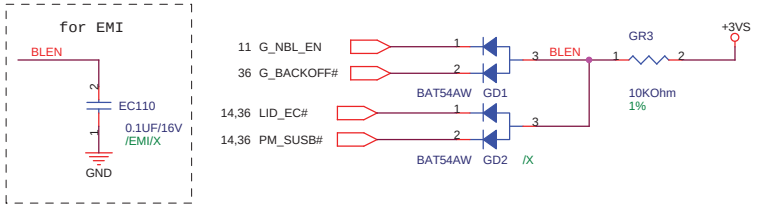
Default Group-A7V8X MX

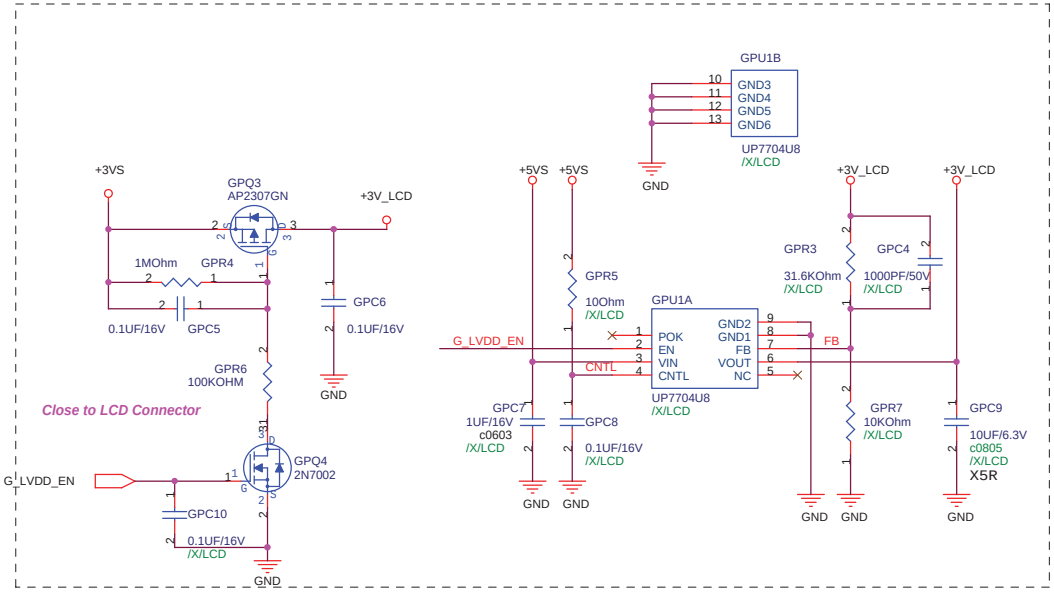
ASUSTek Computer INC.	Title : Onboard VGA	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 22 of 51	

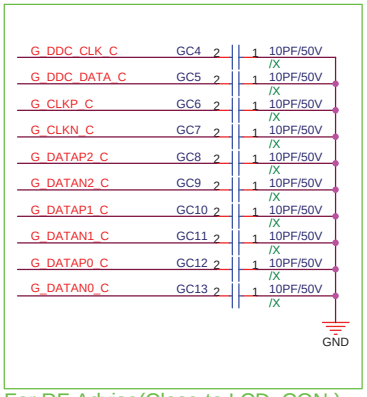
0.1 B Beta



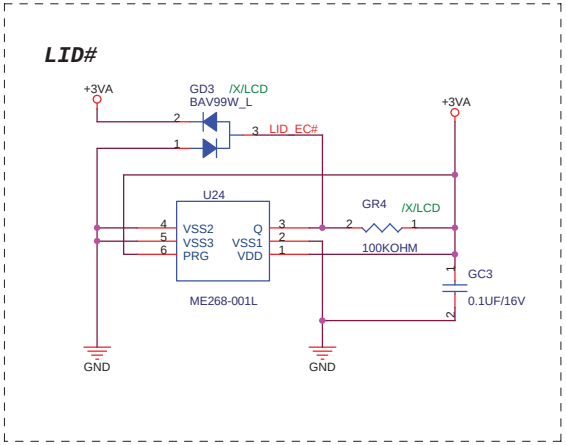






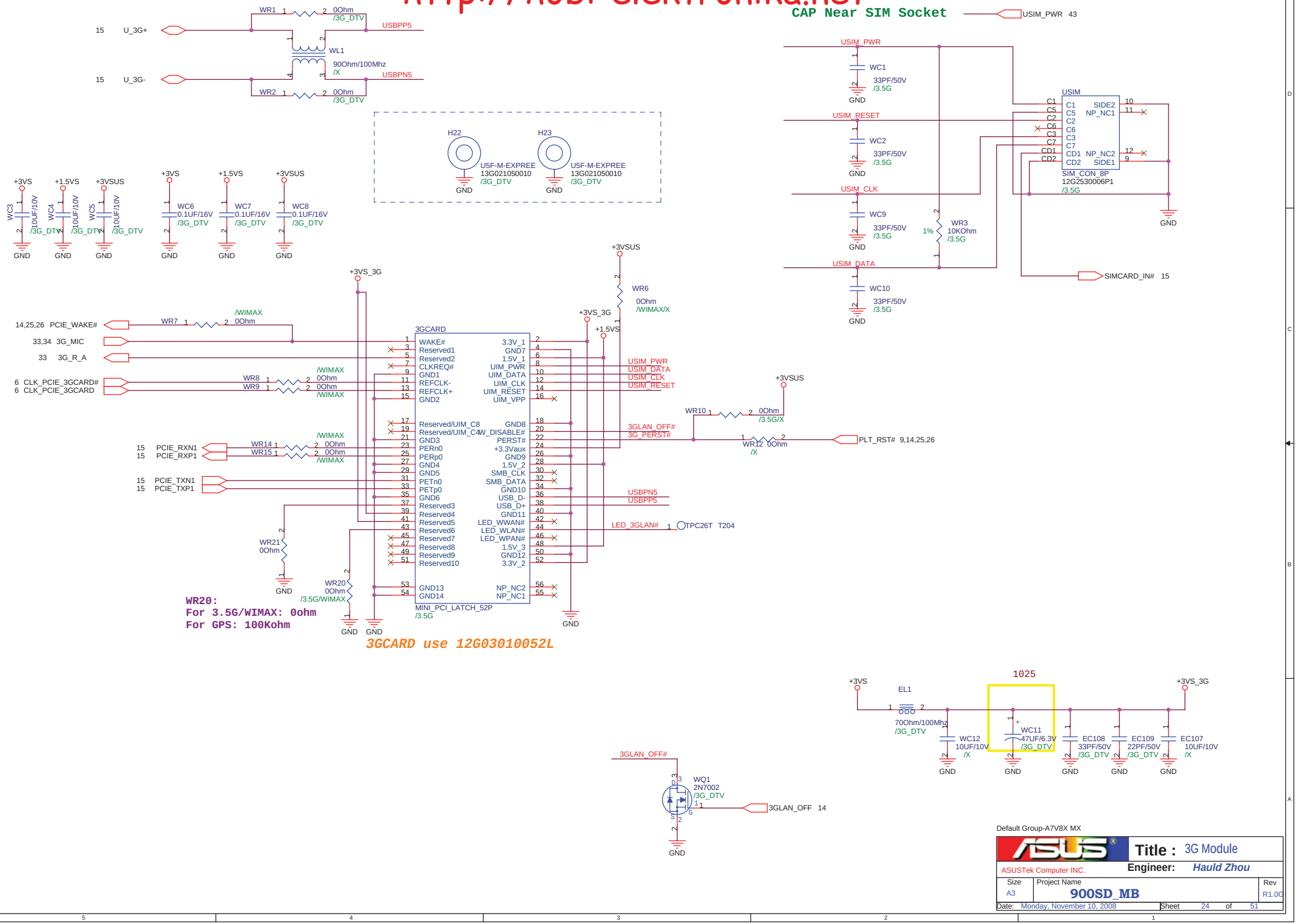


For RF Advise(Close to LCD_CON)



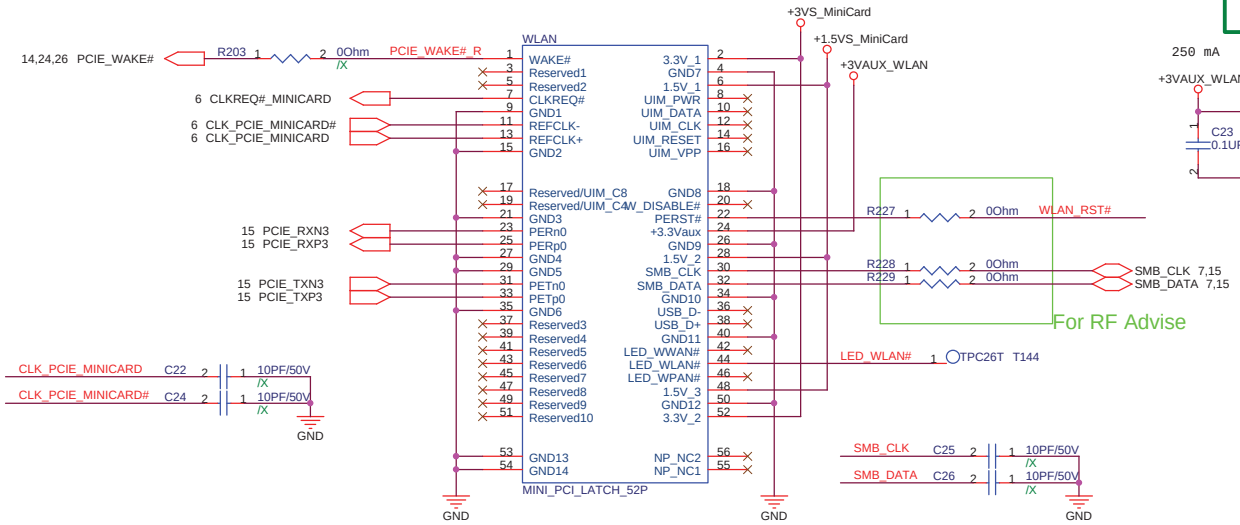
Default Group-A7V8X MX

ASUSTek Computer Inc.	Title : LCD-CON for 10inch	
	Engineer: SUSAN_SHI	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 23 of 51	

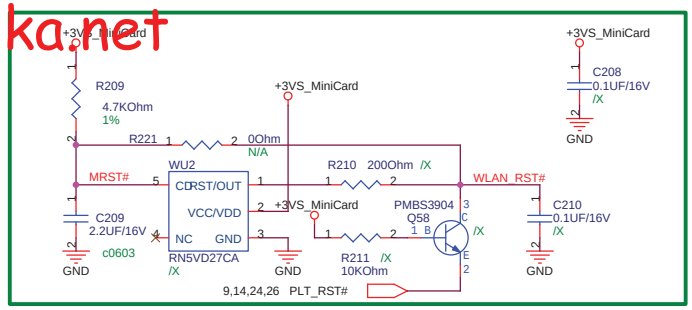


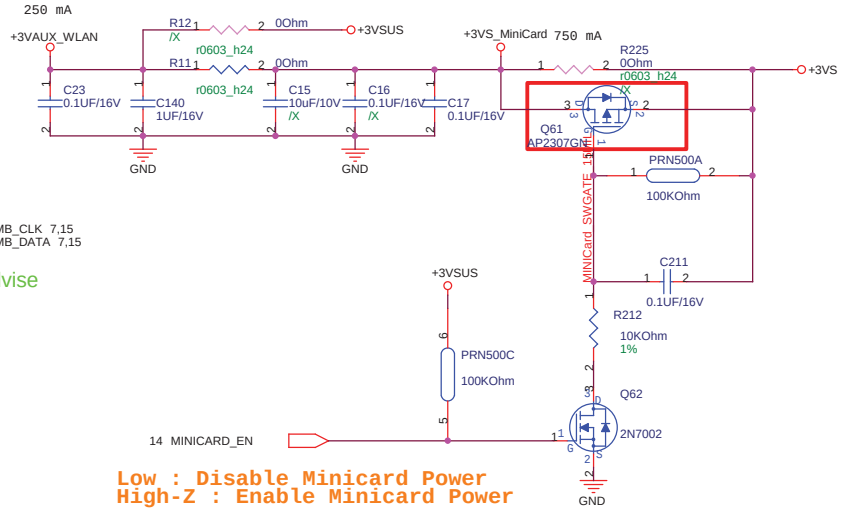
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : 3G Module	
	Engineer: Hauld Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 24 of 51	

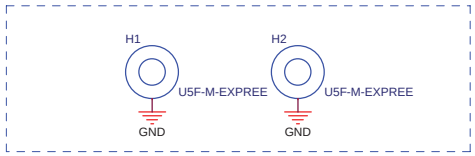


For RF Advise

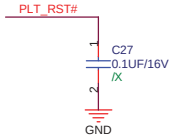


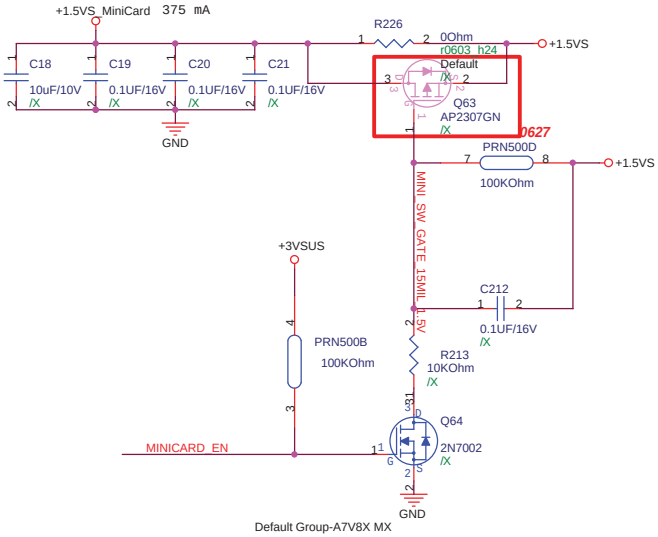


Low : Disable Minicard Power
High-Z : Enable Minicard Power



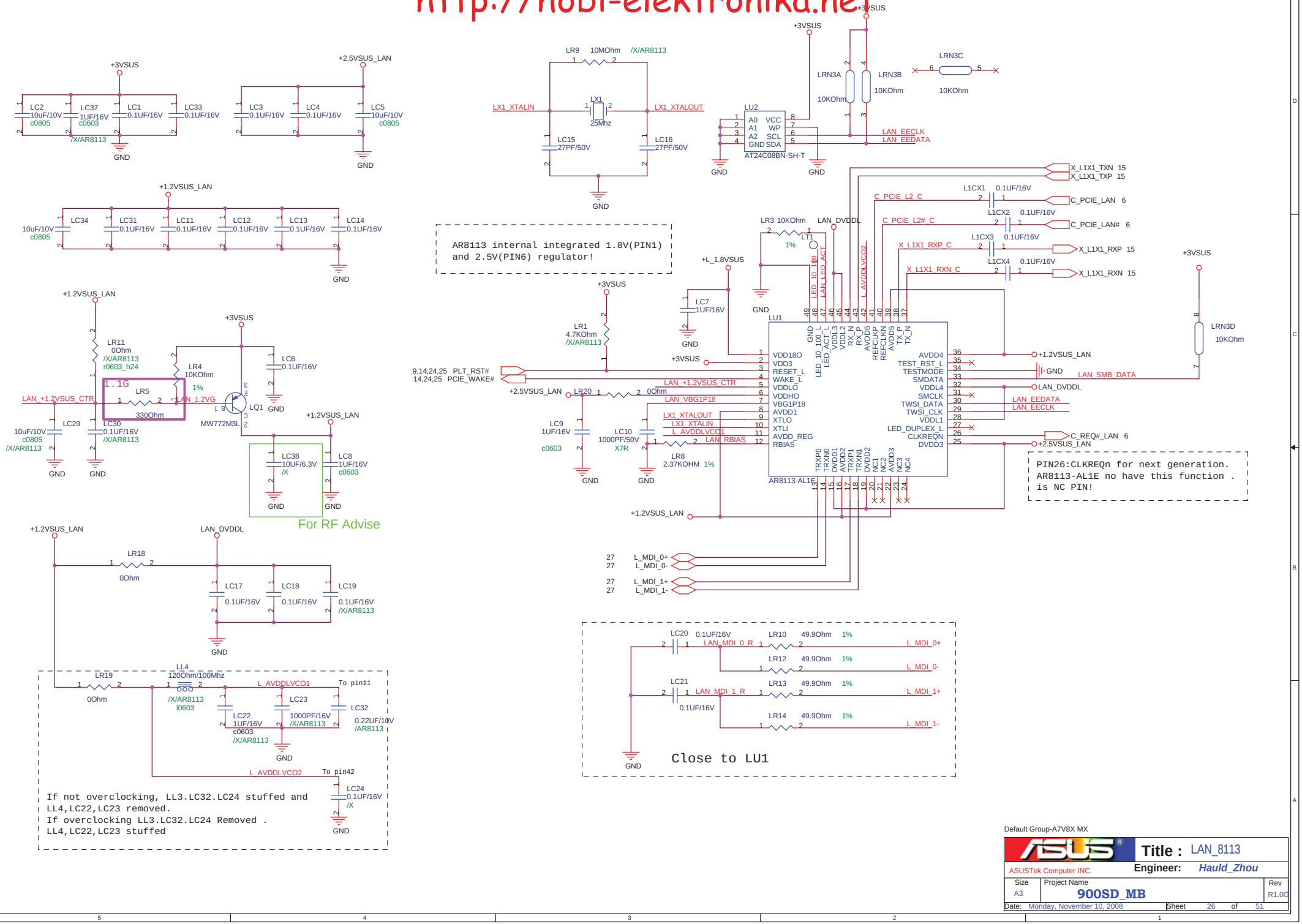
MINI CARD NUT(1.6mm) *2





Default Group-A7V8X MX

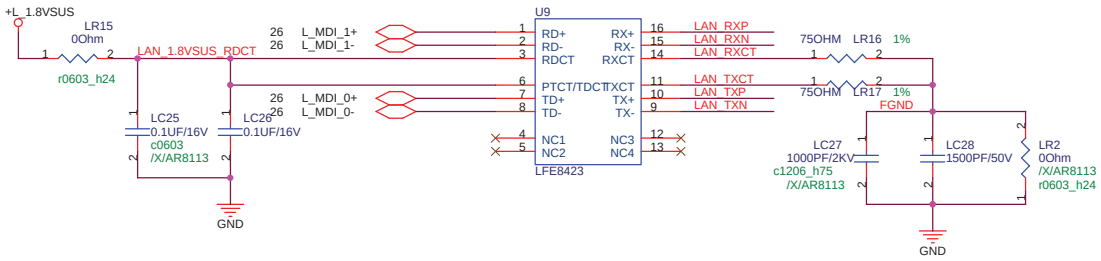
ASUSTek Computer INC.	Title : WLAN	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 25 of 51	

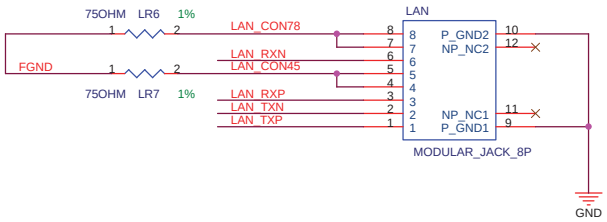


Default Group-A7V8X MX

ASUSTek Computer INC.	Title : LAN_8113	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 26 of 51	

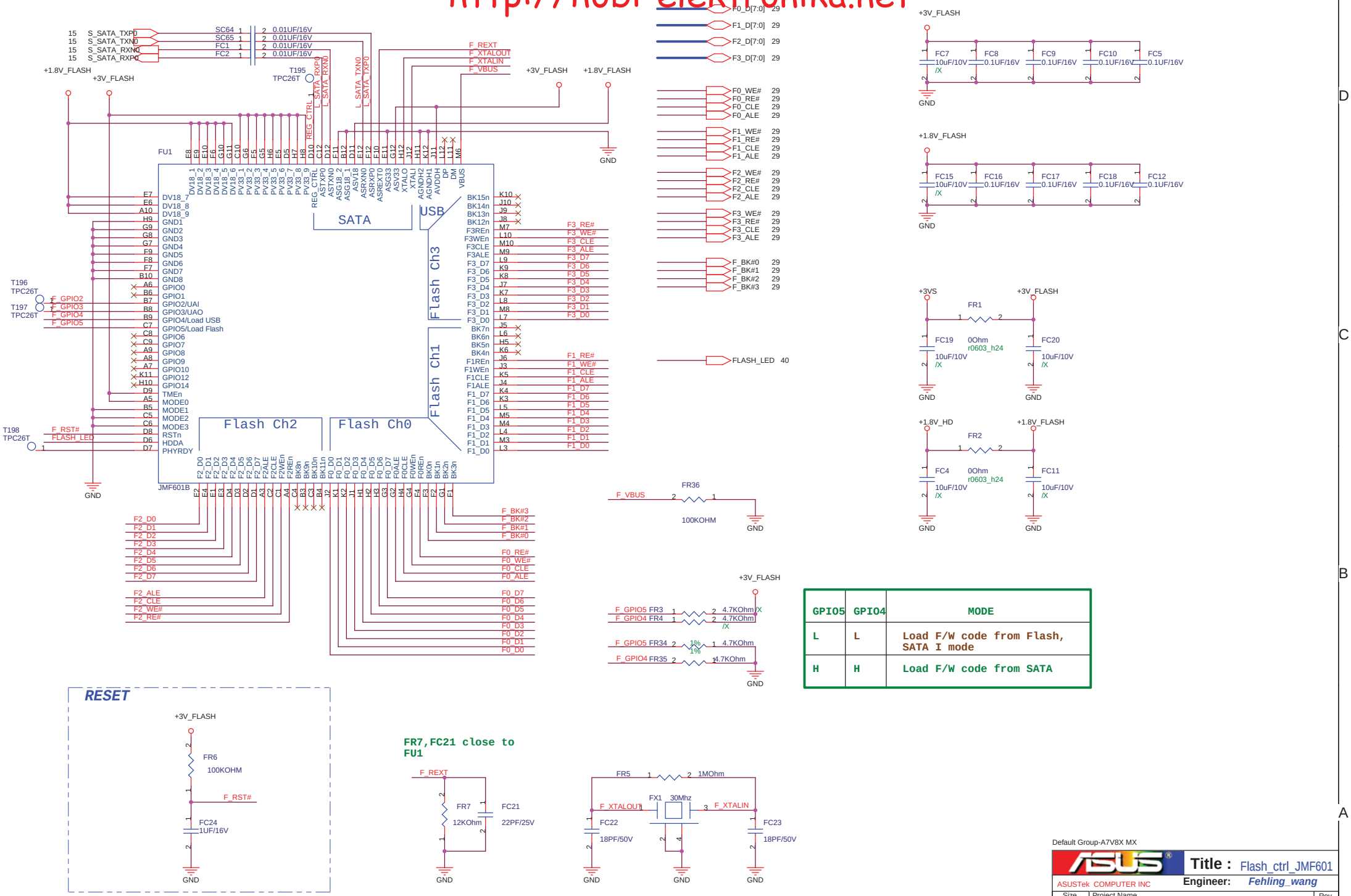
DELETE MODEM





Default Group-A7V8X MX

ASUSTek Computer INC.	Title : RJ45	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 27 of 51	



GPIO5	GPIO4	MODE
L	L	Load F/W code from Flash, SATA I mode
H	H	Load F/W code from SATA

FR7,FC21 close to FU1

Default Group-A7V8X MX

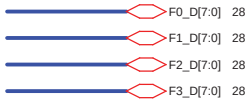
ASUSTek COMPUTER INC

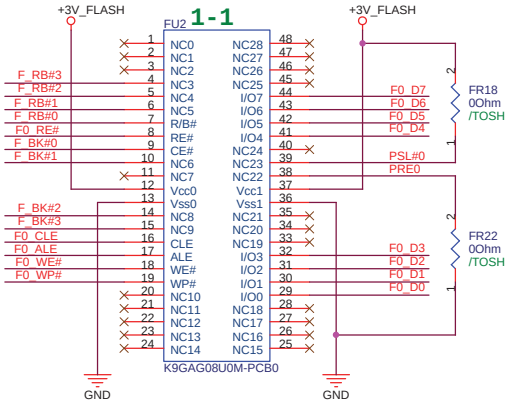
Title : Flash_ctrl_JMF601

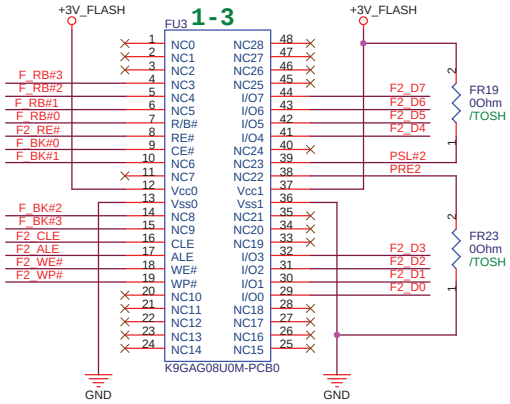
Engineer: Fehling_wang

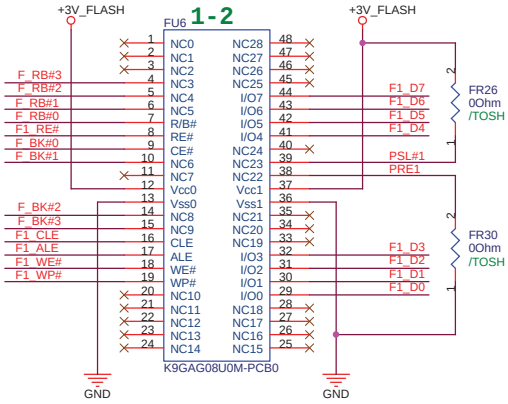
Size	Project Name	Rev
A3	900SD_MB	R1.0G

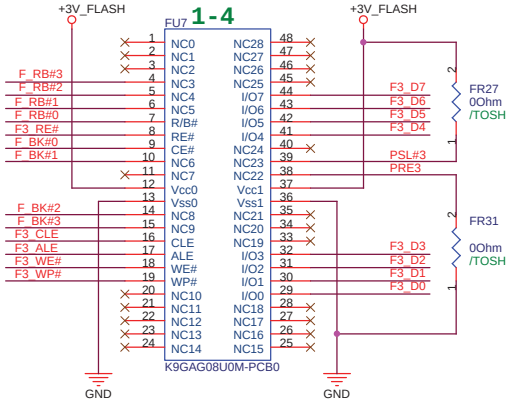
Date: Monday, November 10, 2008 Sheet 28 of 51

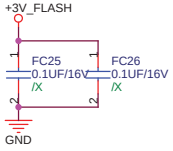


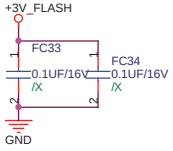


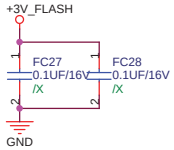


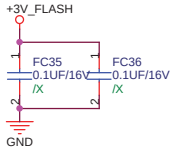






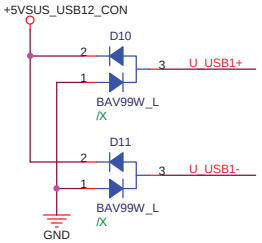


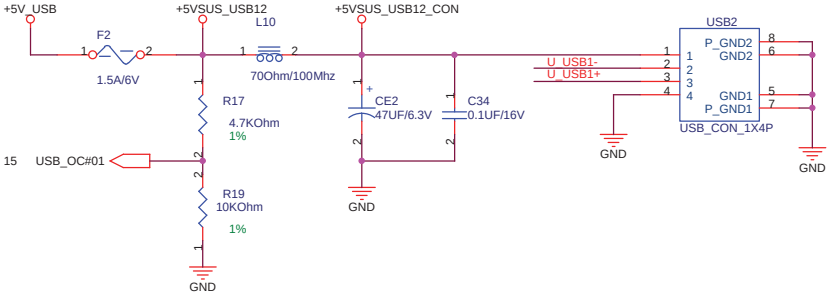


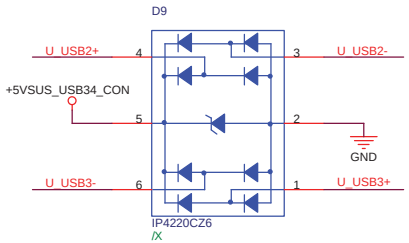


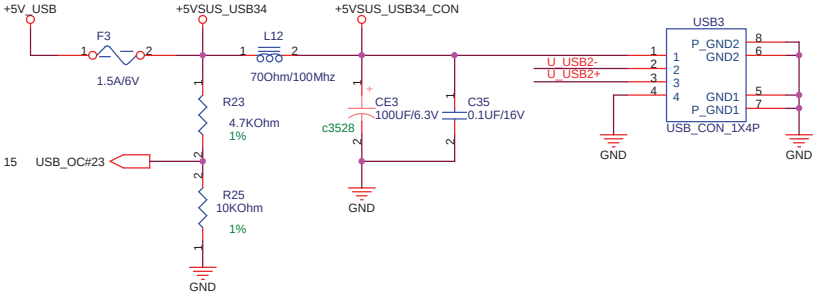
Default Group-A7V8X MX

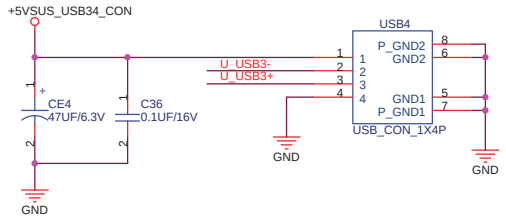
ASUSTek COMPUTER INC	Title: On Board NAND Flash	
	Engineer: Fehling_wang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 29 of 51	





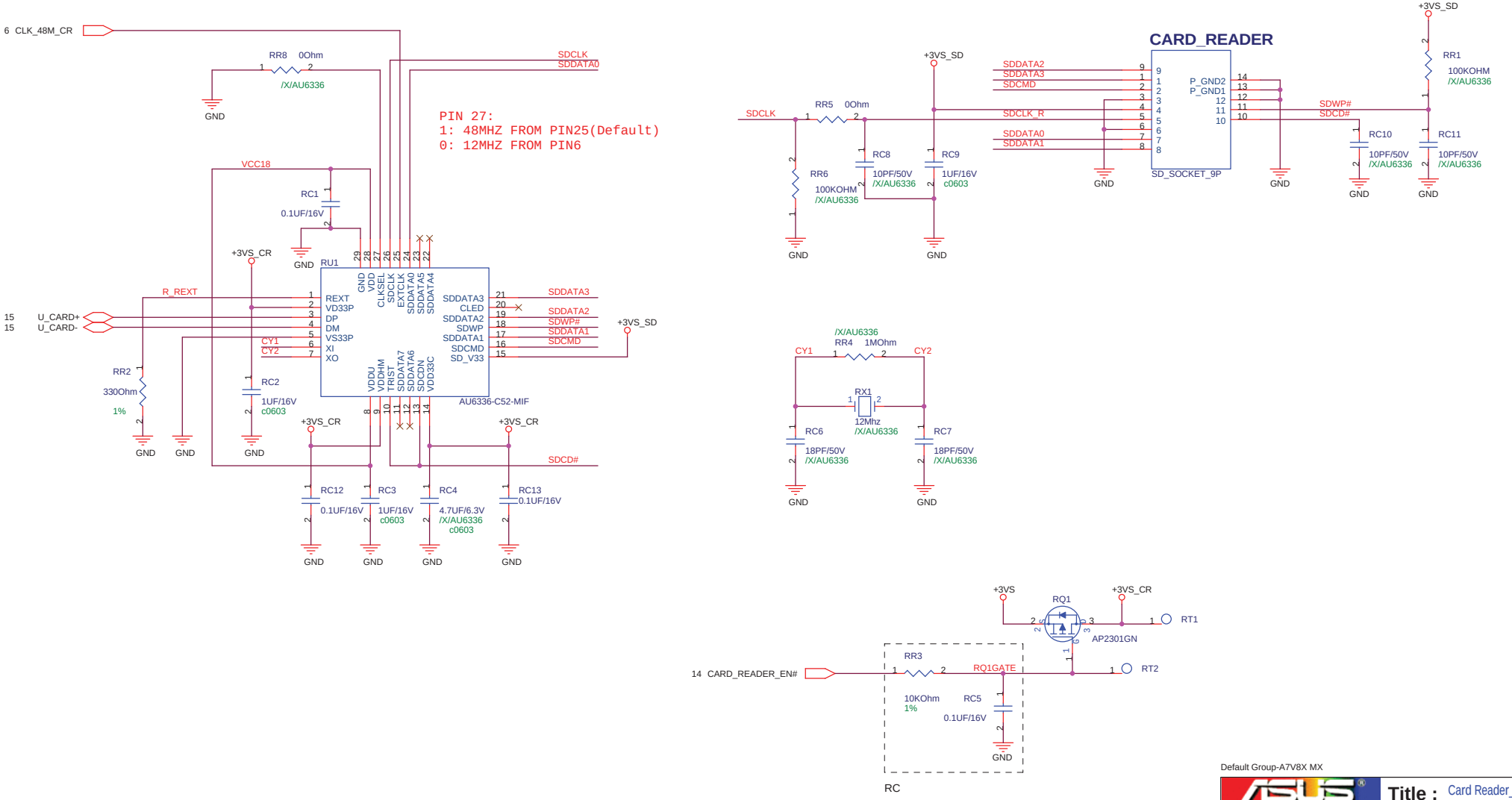






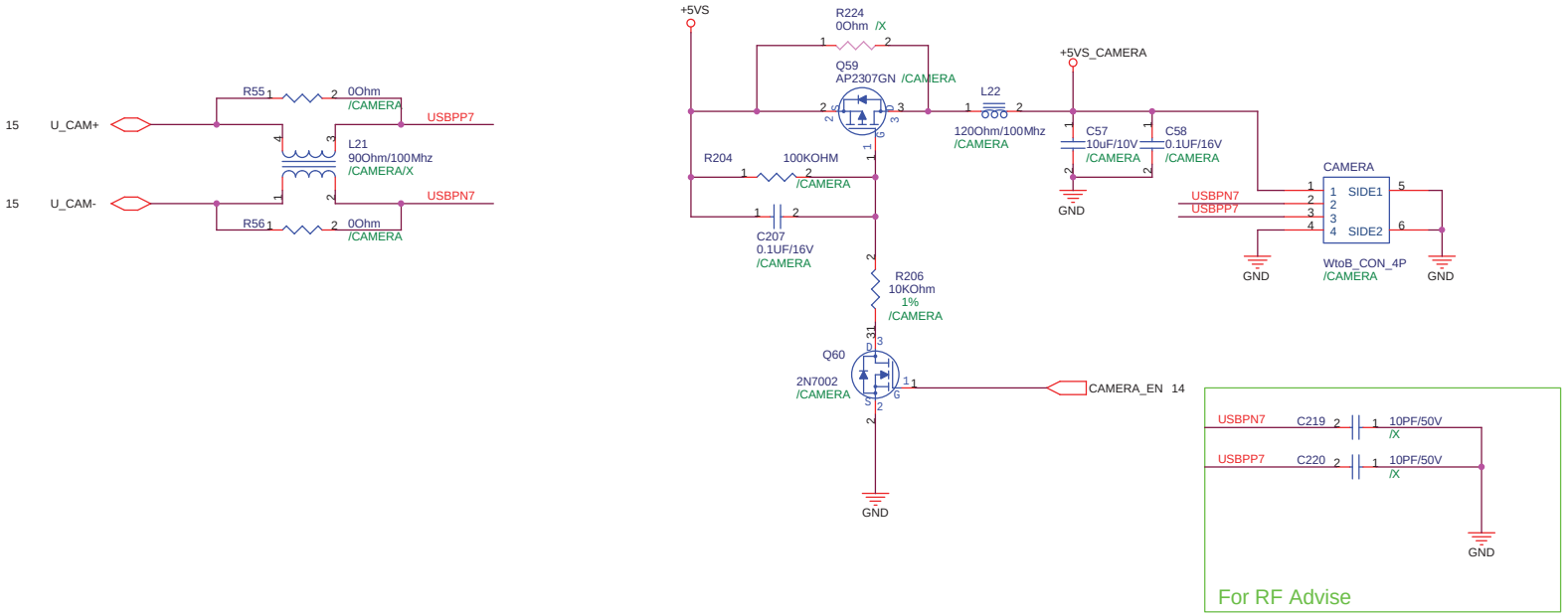
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : USB Port	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 30 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Card Reader_AU6336	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 31 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Camera Conn	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 32 of 51	

Vout=0.8*(1+(49.9K/10.2K))

900SD R1.0G

Place next to pin 38

Place next to pin 25

Place next to pin 46

Place next to pin 39

Place next to pin 27

Place next to pin 1

Place next to pin 9

Surges of PVDD >7V duration 0.1ms when class D amplifier is working may damage the amplifier, 10uF tantalum capacitors are required at PVDD1 and PVDD2 to uppress the surge.

A_PD#	speaker AMP.
H	power down
L	power up

R1.0G

R1.0G

Default Group-A7V8X MX

ASUSTek Computer INC.

Title : ALC269-1

Engineer: Jeff_Li

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 33 of 51

MIC1

Internal MIC

MIC
SIDE2 4 2 1 SIDE1 3
WTOB_CON_2P
GND
AL5 120Ohm/100Mhz l0603
A_MIC2_L_D
A_MIC2_L_C 35
AC8 100PF/50V /X/ALC269/EMI
Stereo MIC mount 100PF C
GND
For Layout

SPEAKER

A_SPK_L+ AC102 2200PF/50V /X/ALC269/EMI
A_SPK_R+ AC103 2200PF/50V /X/ALC269/EMI
A_SPK_L- AC104 2200PF/50V /X/ALC269/EMI
A_SPK_R- AC105 2200PF/50V /X/ALC269/EMI
GND GND

Demodulation Filter
Placement near
Audio Codec

33 A_SPK_L+_R AR108 0Ohm r0603_h24 A_SPK_L+
AC9 2200PF/50V c0402 /ALC269/EMI
AC11 2200PF/50V c0402 /ALC269/EMI
P_GND
AC10 1UF/16V /X/ALC269/EMI c0603
33 A_SPK_L-_R AR109 0Ohm r0603_h24 A_SPK_L-
33 A_SPK_R+_R AR110 0Ohm r0603_h24 A_SPK_R+
AC12 2200PF/50V c0402 /ALC269/EMI
AC14 2200PF/50V c0402 /ALC269/EMI
P_GND
AC13 1UF/16V /X/ALC269/EMI c0603
33 A_SPK_R-_R AR111 0Ohm r0603_h24 A_SPK_R-

SPEAKER
4 SIDE2 6
3
2
1 SIDE1 5
WtoB_CON_4P
GND

33 A_JD_MIC1
33 A_BIAS_MIC1_L
33 A_BIAS_MIC1_R
AR19 4.7KOhm 1%
AR20 4.7KOhm 1%
AC18 4.7UF/16V c0805 X5R
33 A_MIC1_R
33 A_MIC1_L
A_MIC1_R_C
A_MIC1_L_C
1KOhm AR21
AR22 1KOhm
AC19 4.7UF/16V c0805 X5R
4.7UF~10UF X5R or DIP
A_MIC1_R_R
A_MIC1_L_R
AL10 120Ohm/100Mhz l0603
AL11 120Ohm/100Mhz l0603
A_JD_MIC1_L
A_MIC1_R_L
A_MIC1_L_L

MIC_JACK
8 NP_NC2 10
7 NP_NC1 9
Shell
PHONE_JACK_6P

AC20 100PF/50V /ALC269/EMI
AC21 100PF/50V /ALC269/EMI
AC22 100PF/50V /ALC269/EMI
A_GND

HP

33 A_JD_HP
33 A_HP_R
33 A_HP_L
AR17 75Ohm r0603_h24
AR18 75Ohm r0603_h24
A_HP_R_R
A_HP_L_R
AL7 120Ohm/100Mhz l0603
AL8 120Ohm/100Mhz l0603
A_JD_HP_L
A_HP_R_L
A_HP_L_L

LINE_OUT
8 NP_NC2 10
7 NP_NC1 9
Shell
PHONE_JACK_6P

AC15 100PF/50V /ALC269/EMI
AC16 100PF/50V /ALC269/EMI
AC17 100PF/50V /ALC269/EMI
A_GND

24,33 3G_MIC
3G_MIC
AC110 1UF/16V /3.5G/X
AR106 100KOHM /3.5G/X
AR107 100KOHM /3.5G/X
AC109 1UF/16V /3.5G/X
AC111 1UF/16V /3.5G/X
A_MIC1_L_C
A_MIC1_R_C
R1.0G

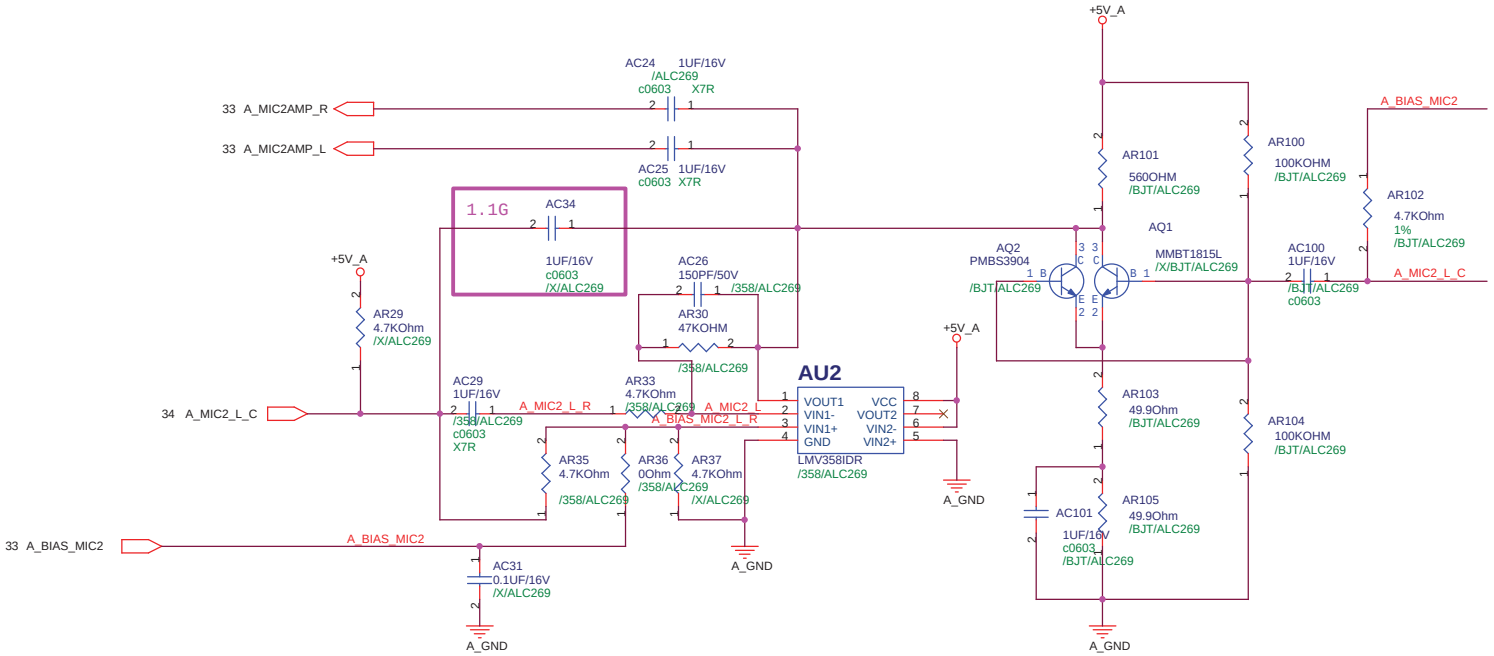
AR43 0Ohm /X/ALC269/EMI
AR44 0Ohm
AR6 0Ohm
P_GND
GND

AR23 0Ohm /X/ALC269/EMI
AR24 0Ohm
AR25 0Ohm
GND A_GND

AR24, AR25 can use
0.1UF 11G233310432320
for EMI

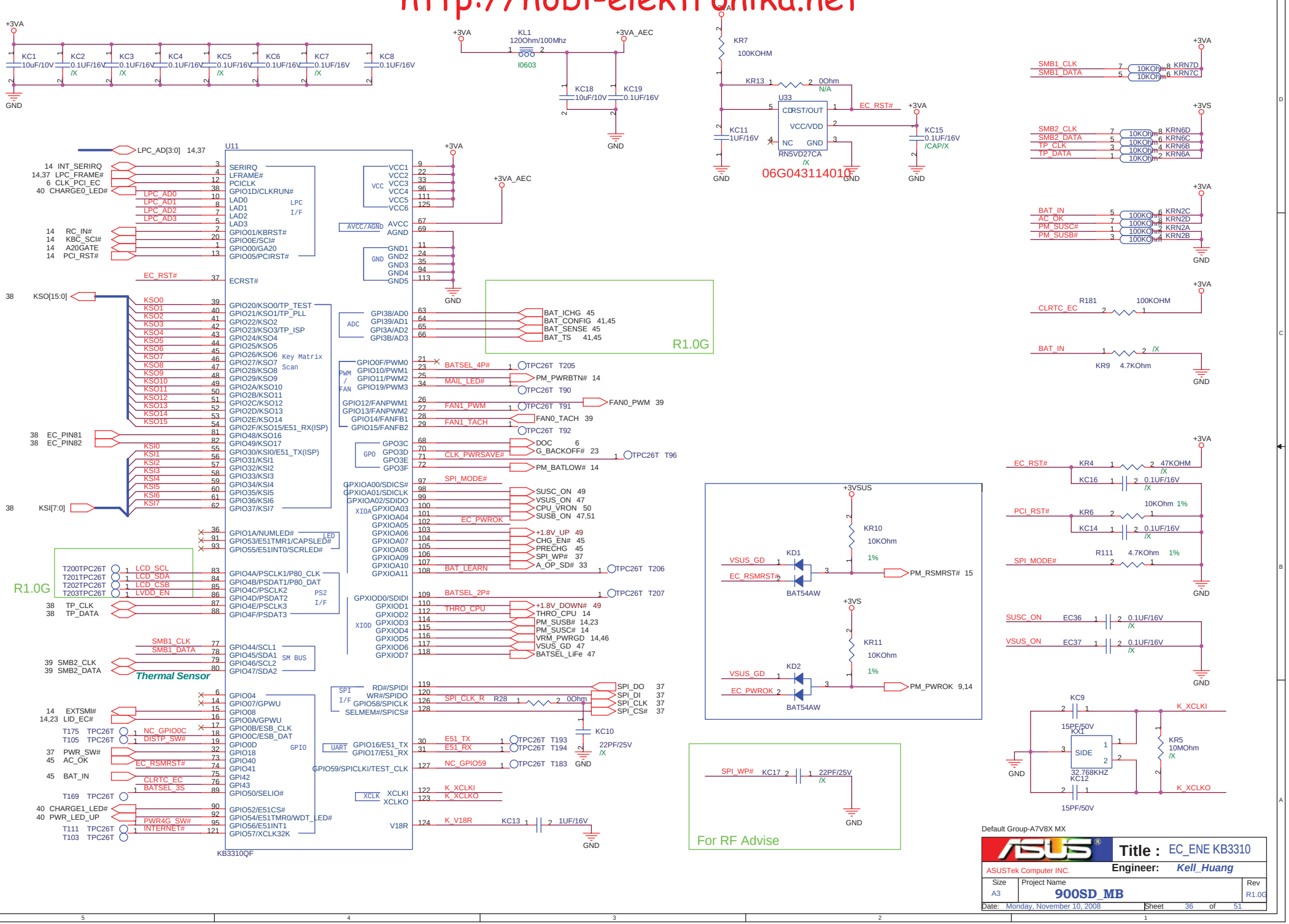
Default Group-A7V8X MX

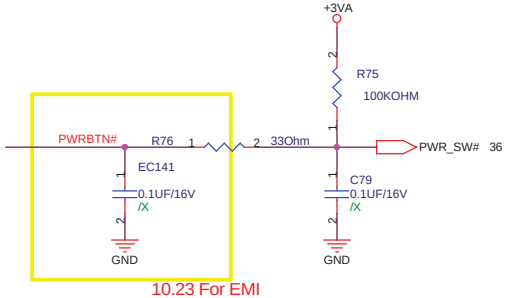
ASUSTek Computer INC.	Title : ALC269-2(IO)	
	Engineer: Jeff_Li	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 34 of 51	



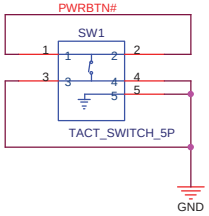
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : ALC269-3(MIC AMP)	
	Engineer: Jeff_Li	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 35 of 51	

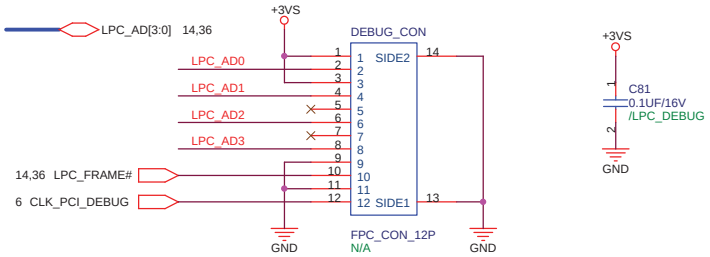


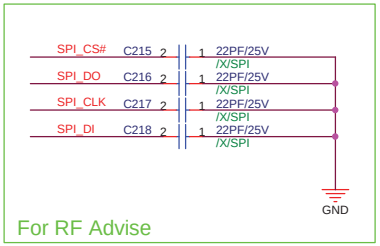


10.23 For EMI

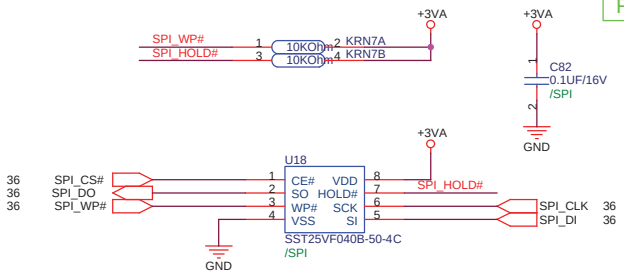


For Debug





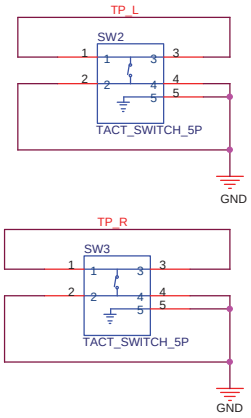
For RF Advise

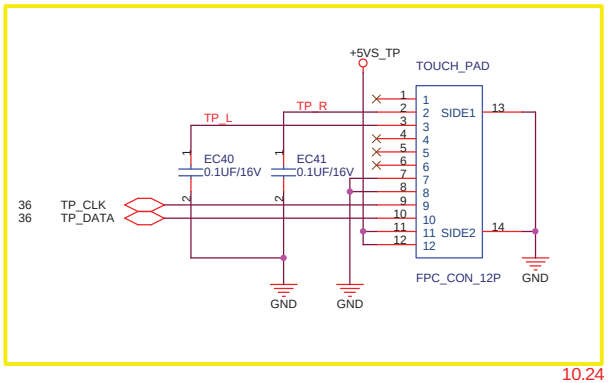


Default Group-A7V8X MX

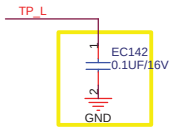
ASUSTek Computer INC.	Title : Switch_SPI ROM	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 37 of 51	

For Touch-Pad



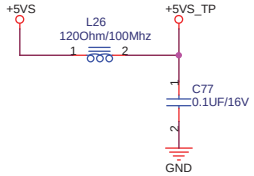


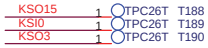
10.24

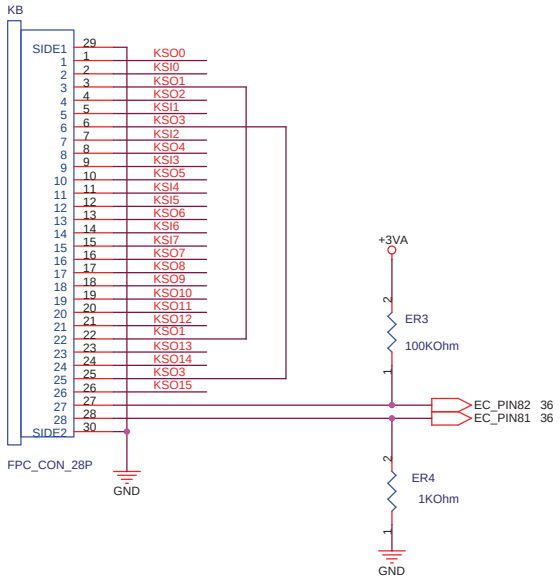


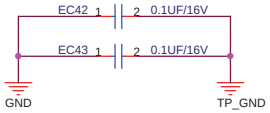
10.23 For EMI

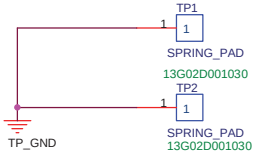
For Keyboard

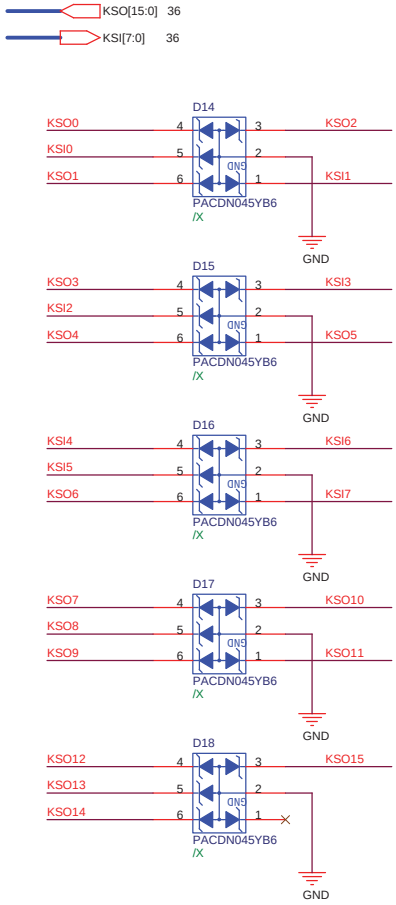


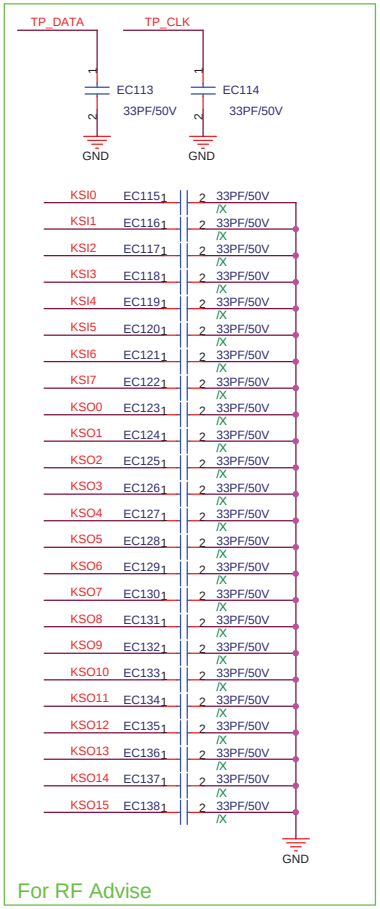








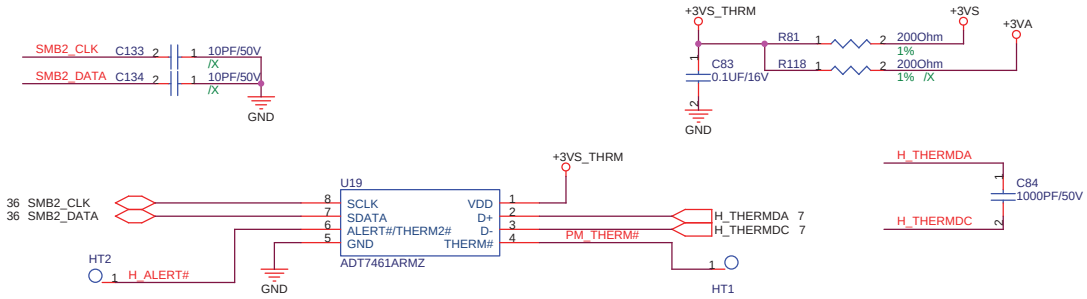




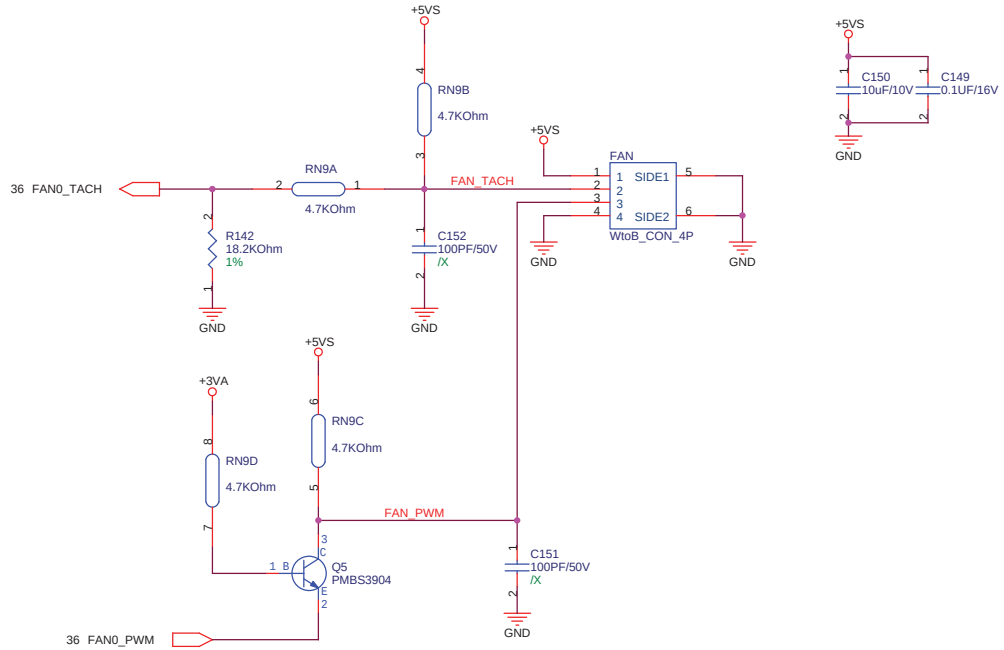
For RF Advise

Default Group-A7V8X MX

ASUSTek Computer INC.	Title : KB_Touch Pad	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 38 of 51	



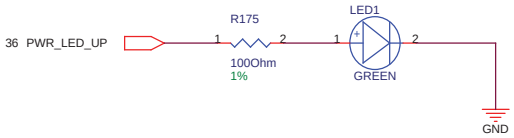
U19 use 06G023048021



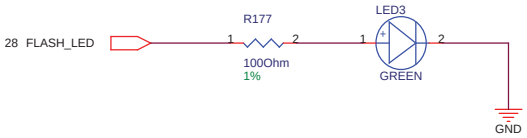
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Thermal Sensor_FAN	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 39 of 51	

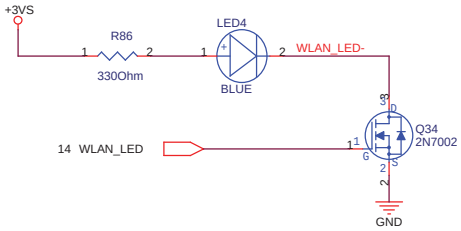
for POWER LED



for FLASH LED

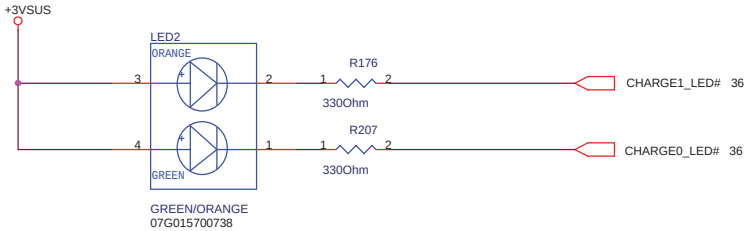


for WLAN LED



R1.0G

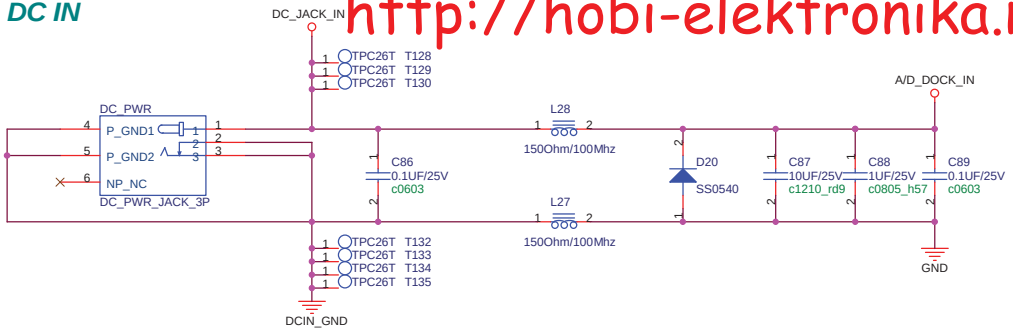
for CHARGE LED



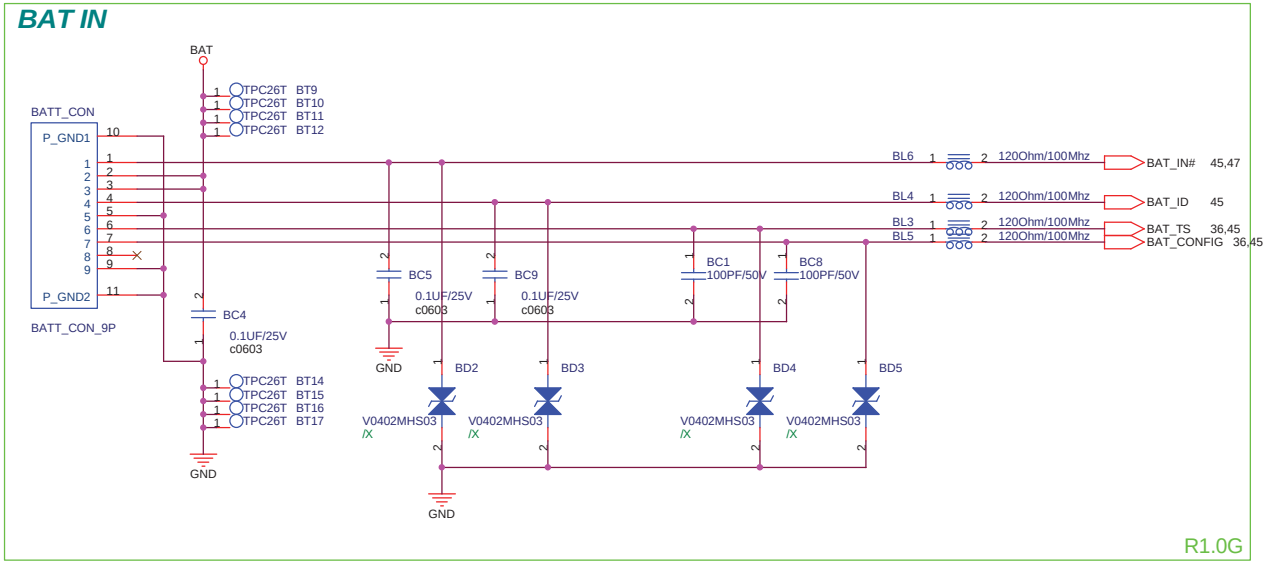
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : LED	
	Engineer: Hauld_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 40 of 51	

DC IN

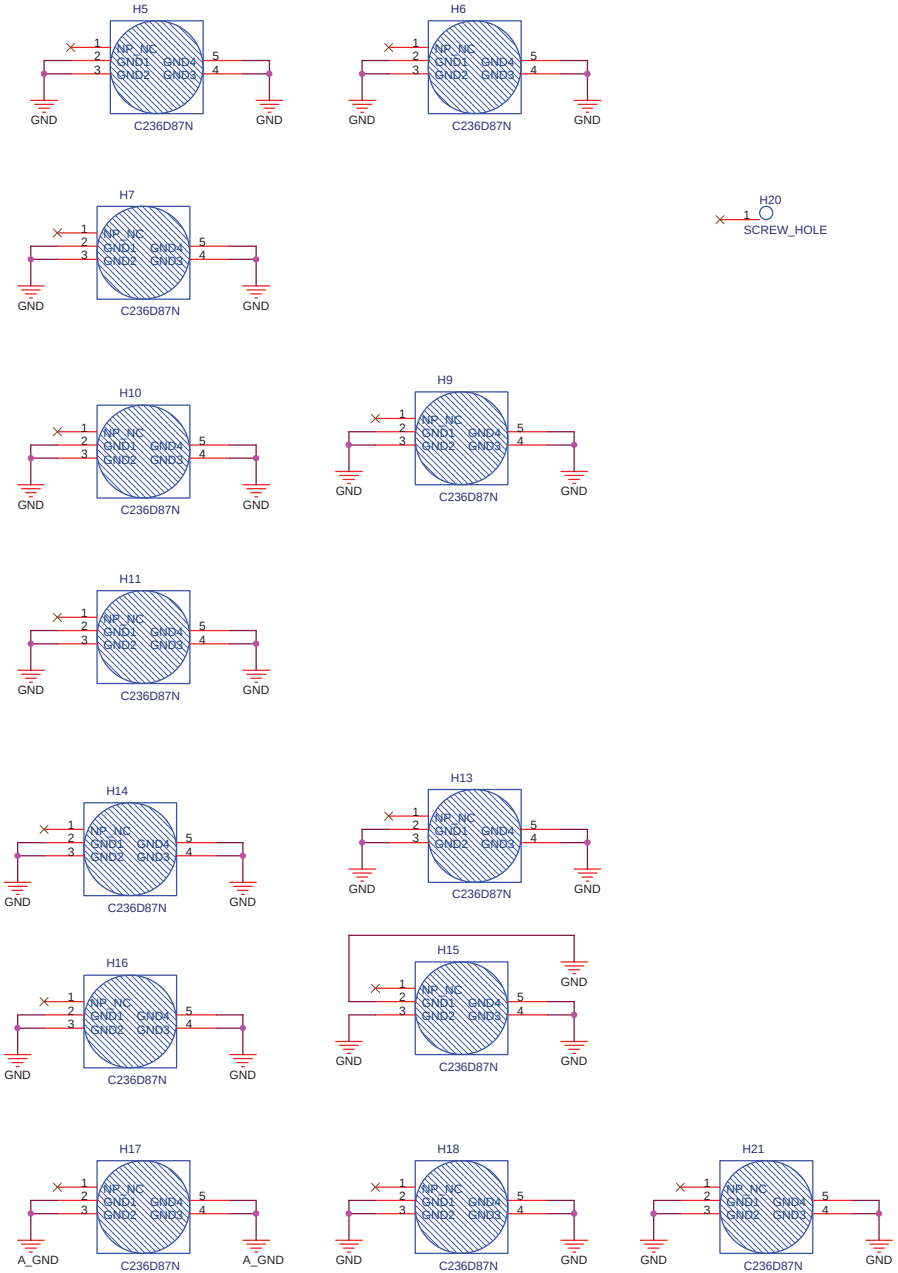


BAT IN



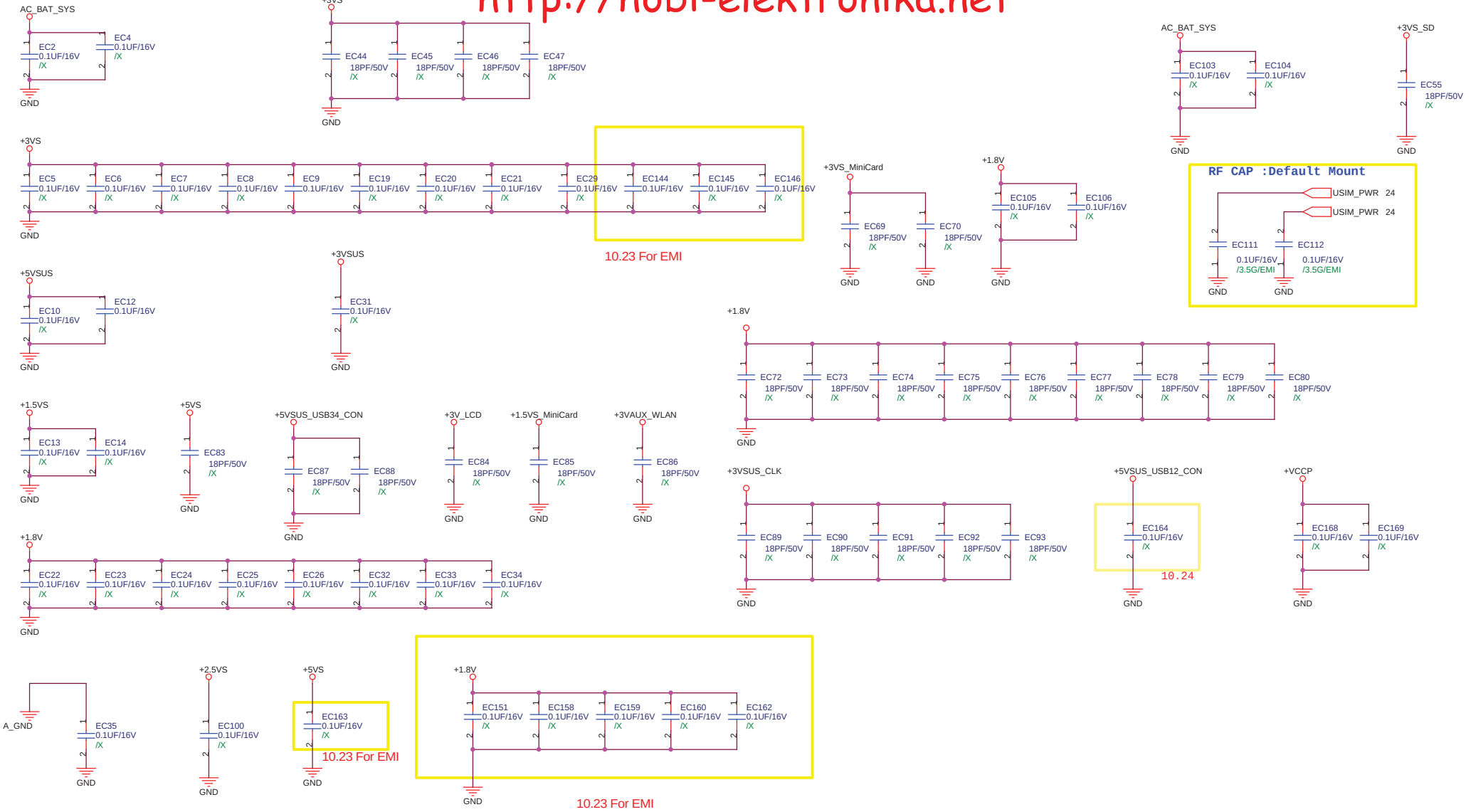
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : PWR Jack	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 41 of 51	



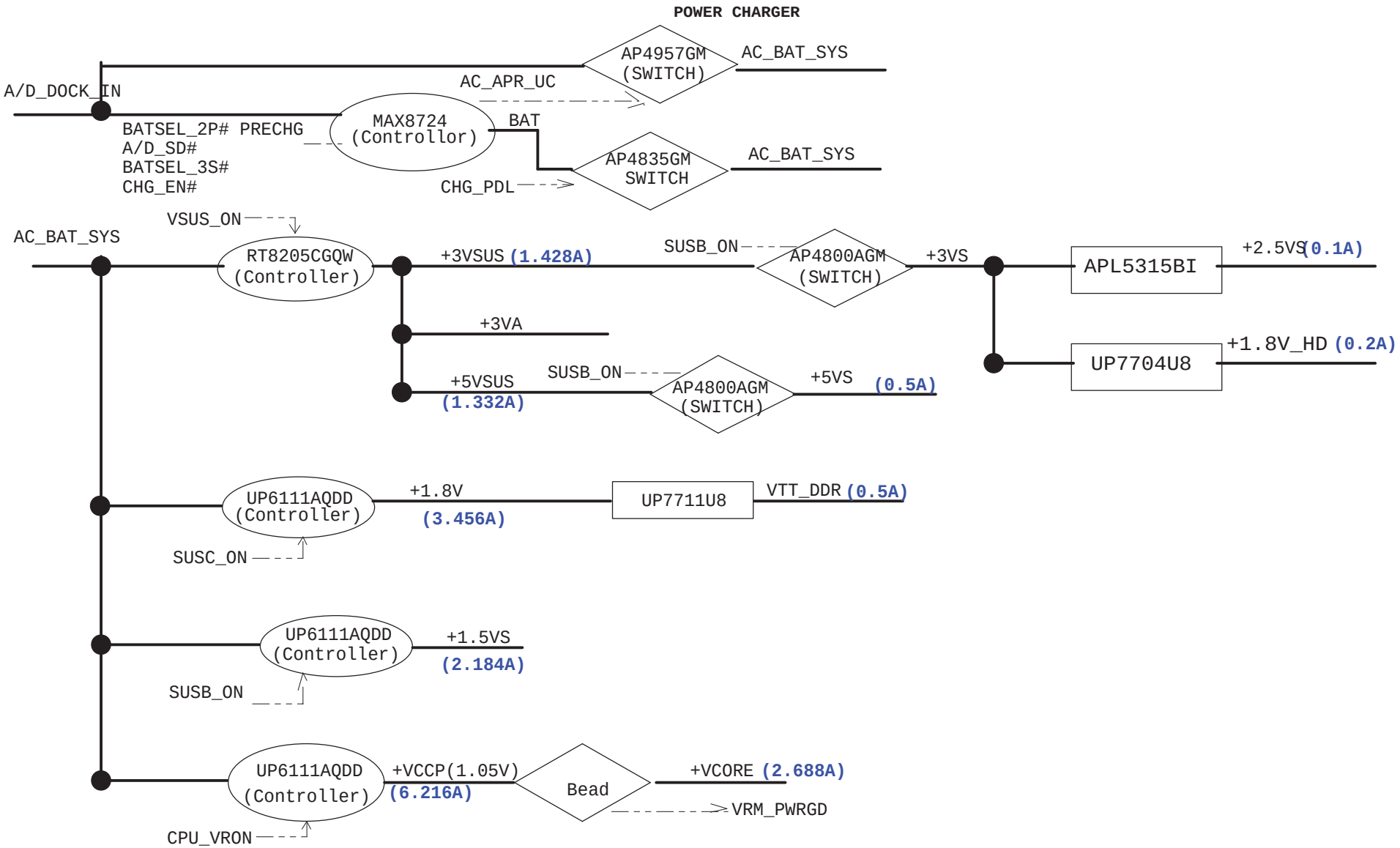
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Srew Hole	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 42 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : EMI	
	Engineer: Kell_Huang	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 43 of 51	



Default Group-A7V8X MX

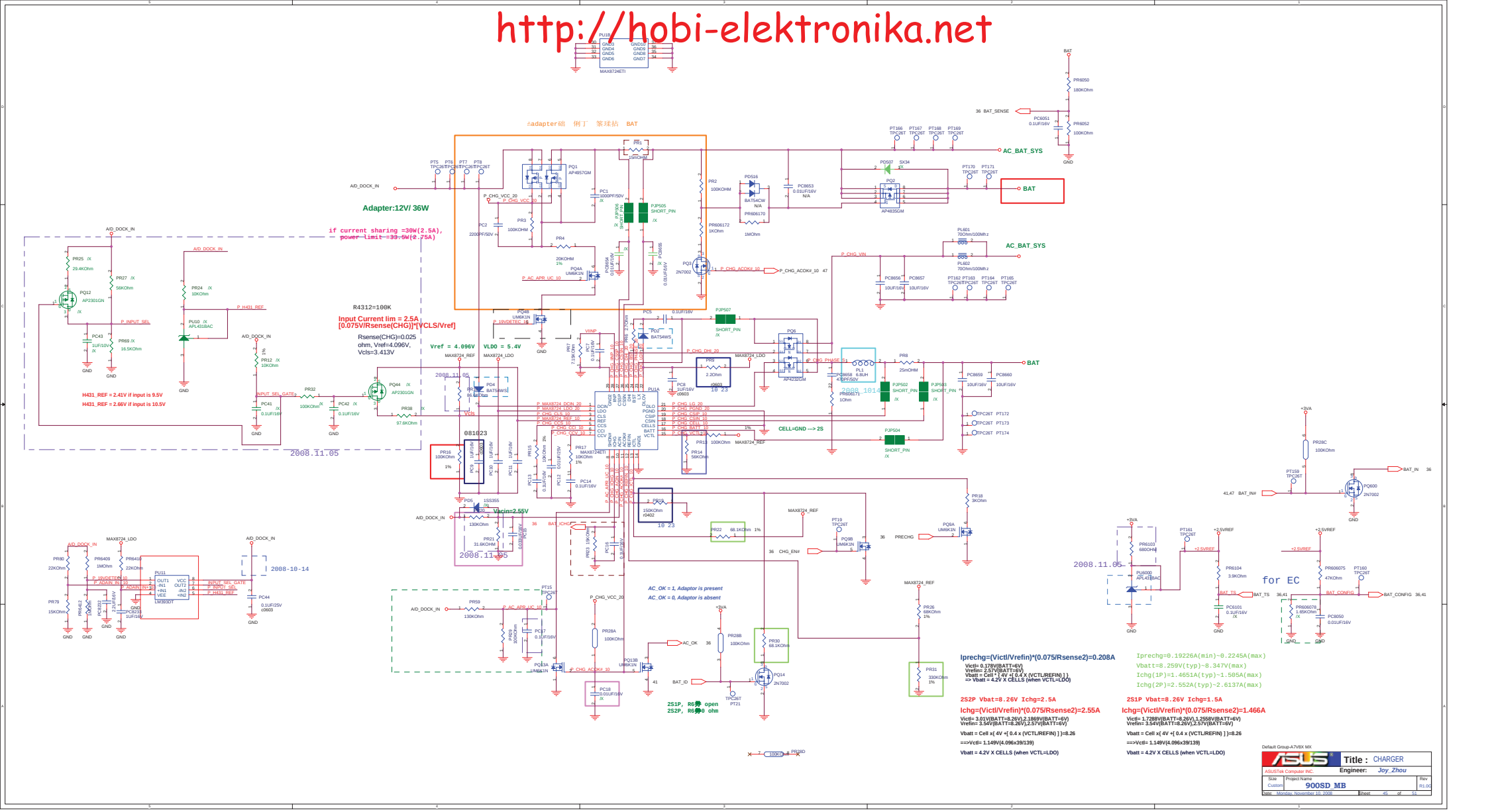
ASUSTek Computer INC.

Title : Power Flow

Engineer: Joy_Zhou

Size	Project Name	Rev
A3	900SD_MB	R1.0G

Date: Monday, November 10, 2008 Sheet 44 of 51



Iprechg=(Victl/Vrefin)*(0.075/Rsense2)=0.208A
Victl= 0.176V(BATT=6V)
Vrefin= 2.57V(BATT=6V)
Vbatt = Cell * [4V +[0.4 x (VCTL/REFIN)]]
=> Vbatt = 4.2V X CELLS (when VCTL=LDO)

Iprechg=0.19226A(min)~0.2245A(max)
Vbatt=8.259V(typ)~8.347V(max)
Ichg(1P)=1.4651A(typ)~1.505A(max)
Ichg(2P)=2.552A(typ)~2.6137A(max)

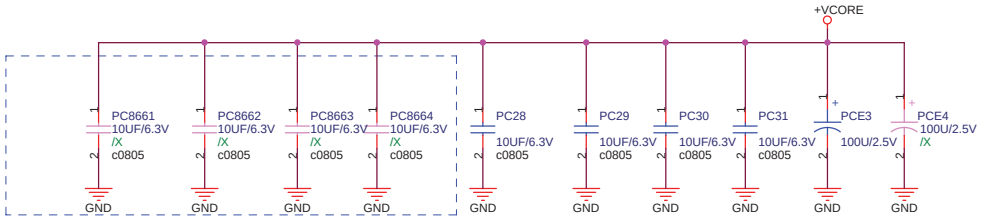
2S2P Vbat=8.26V Ichg=2.5A
Ichg=(Victl/Vrefin)*(0.075/Rsense2)=2.55A
Victl= 3.01V(BATT=8.26V),2.1869V(BATT=6V)
Vrefin= 3.54V(BATT=8.26V),2.57V(BATT=6V)
Vbatt = Cell x{ 4V +[0.4 x (VCTL/REFIN)] }=8.26
==>Vctl= 1.149V(4.096x39/139)
Vbatt = 4.2V X CELLS (when VCTL=LDO)

2S1P Vbat=8.26V Ichg=1.5A
Ichg=(Victl/Vrefin)*(0.075/Rsense2)=1.466A
Victl= 1.7288V(BATT=8.26V),1.2558V(BATT=6V)
Vrefin= 3.54V(BATT=8.26V),2.57V(BATT=6V)
Vbatt = Cell x{ 4V +[0.4 x (VCTL/REFIN)] }=8.26
==>Vctl= 1.149V(4.096x39/139)
Vbatt = 4.2V X CELLS (when VCTL=LDO)

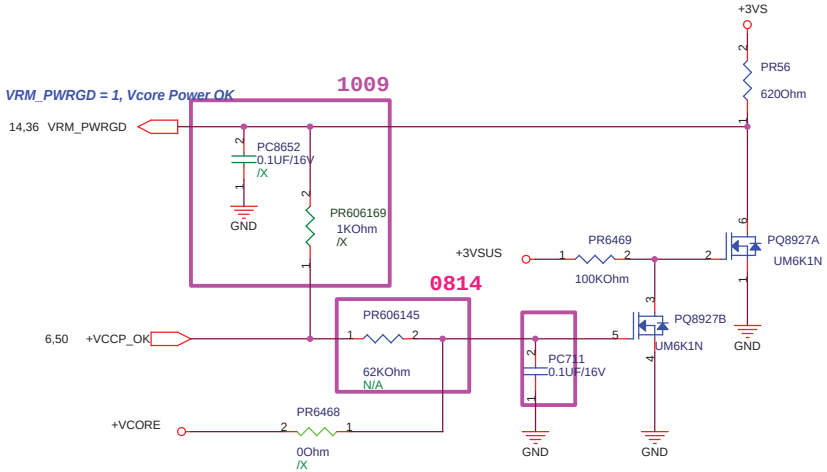
Default Group-A7V8X MX

ASUSTek Computer INC.	Title : CHARGER	
	Engineer: Joy_Zhou	
Size: Custom	Project Name: 90OSD_MB	Rev: R1.0C
Date: Monday, November 10, 2008	Sheet 45 of 51	

+Vcore / 7A

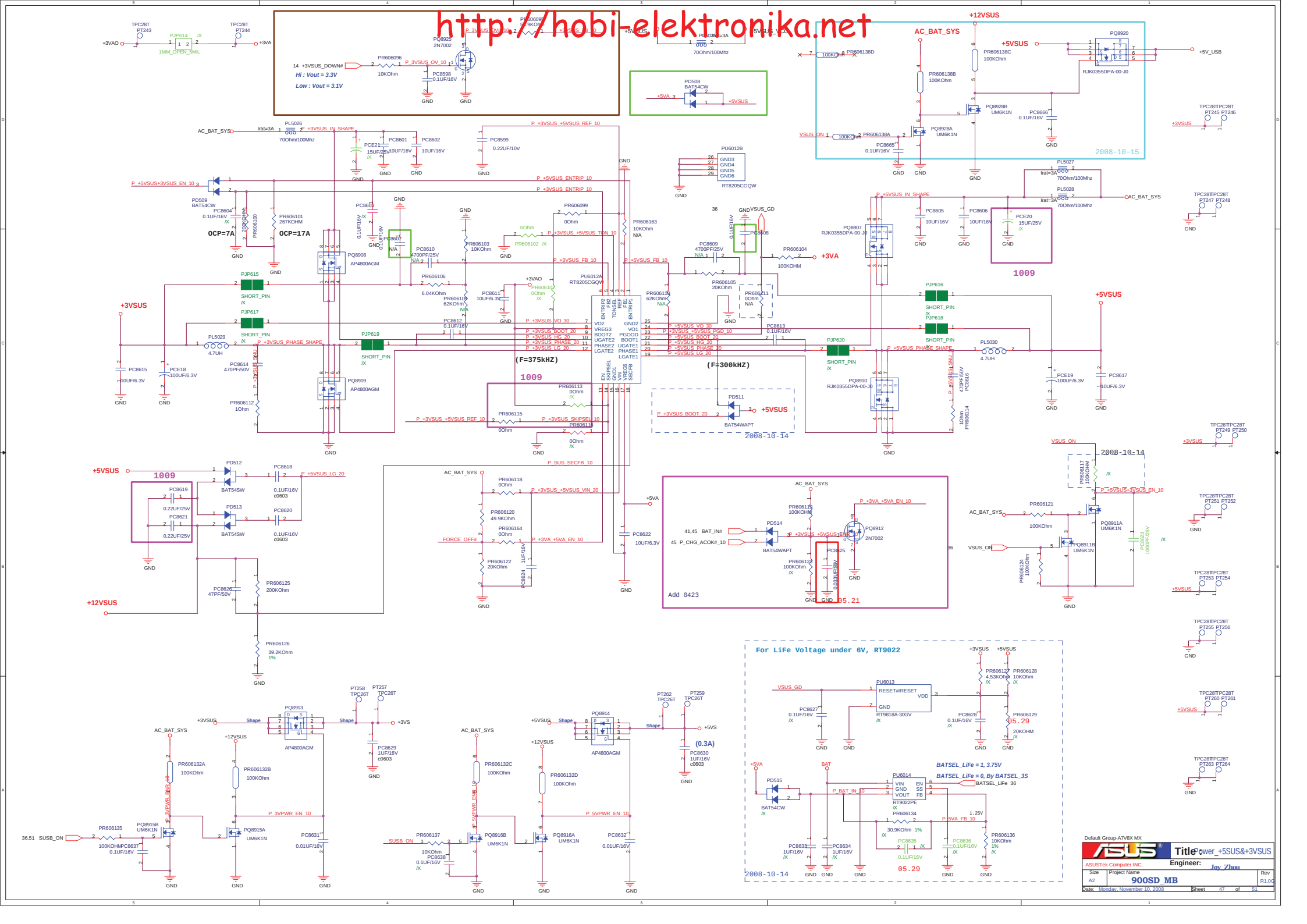


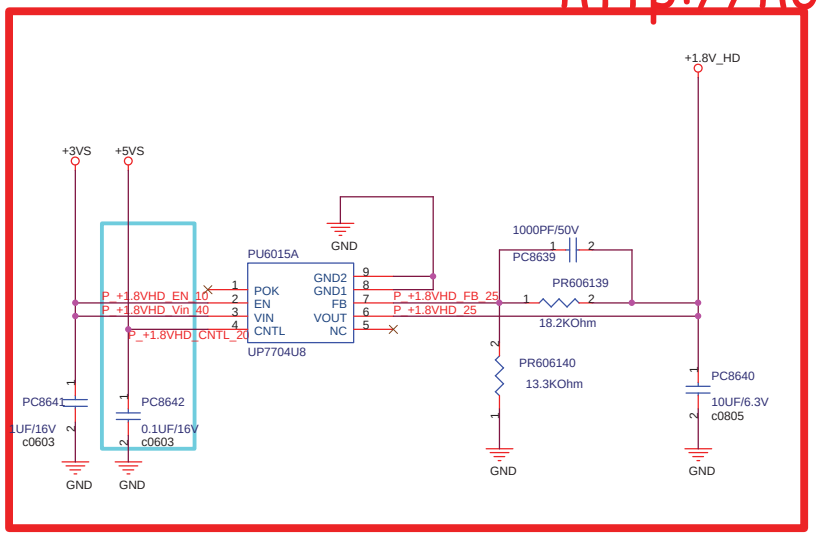
2008-10-15

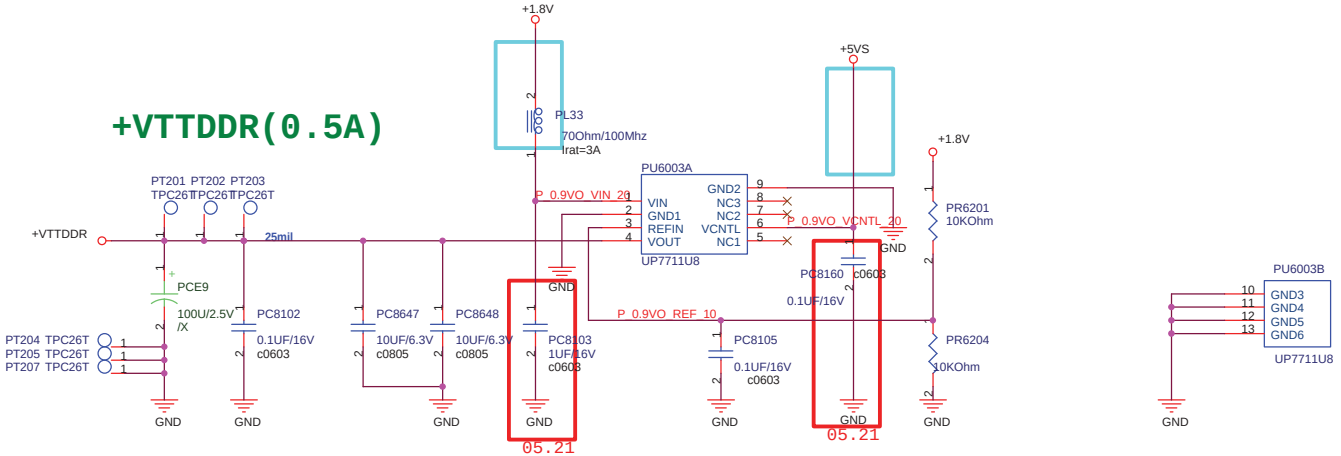


Default Group-A7V8X MX

ASUSTek Computer INC.	Title : Vcore	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 46 of 51	







Default Group-A7V8X MX

ASUSTek Computer INC.	Title : 1.8VHD_VTT_DDR	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
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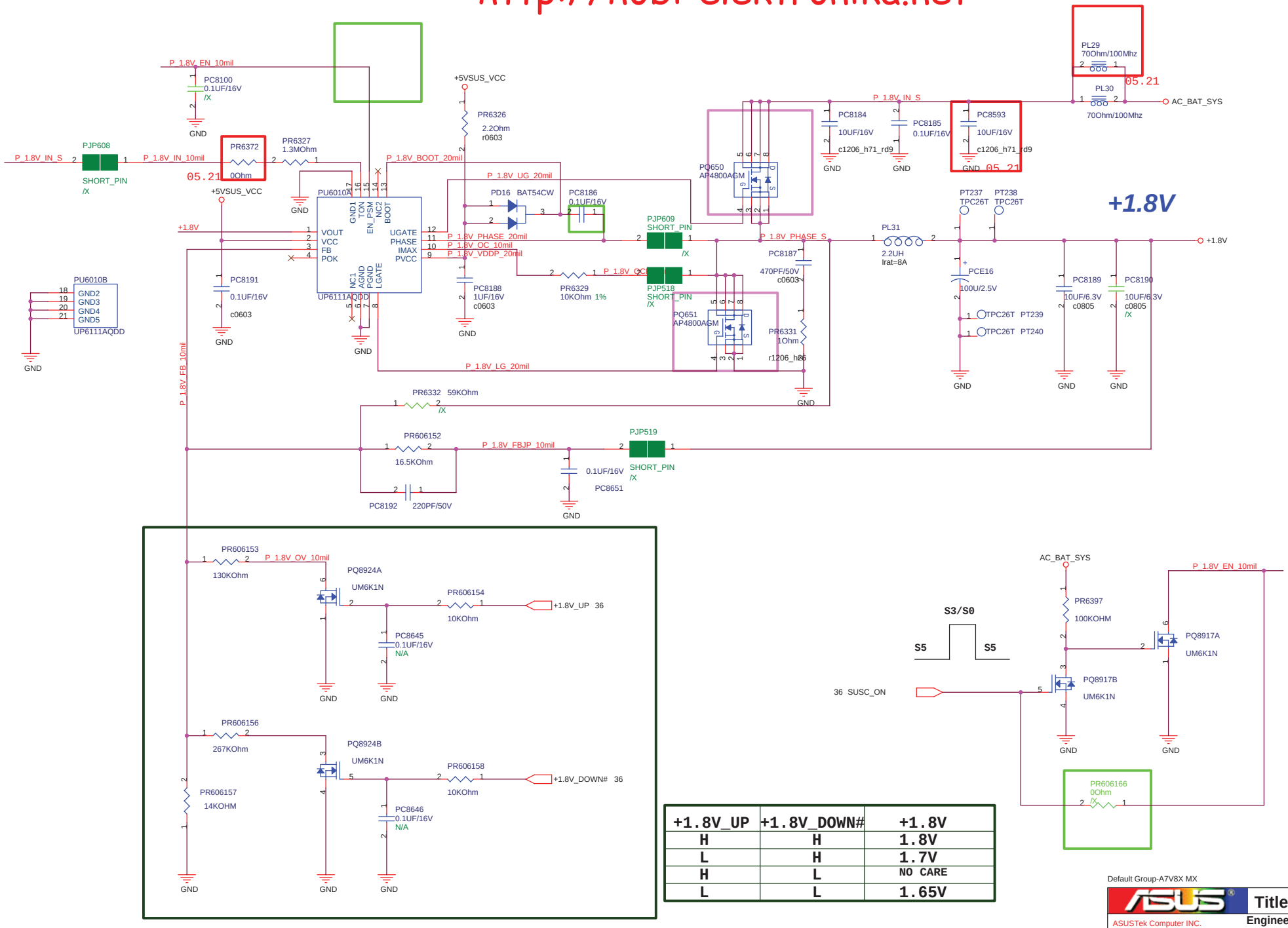
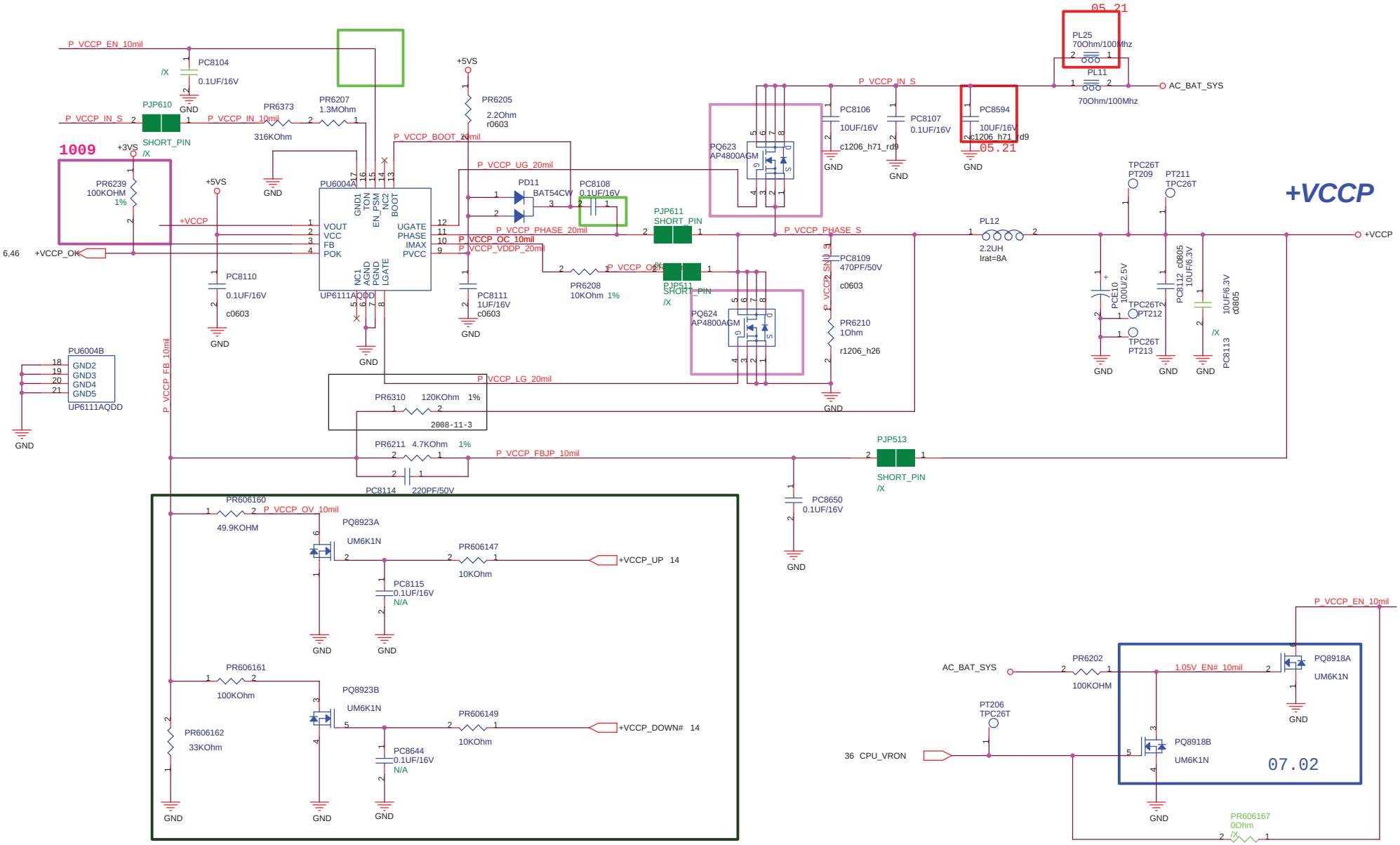


+1.8V_UP	+1.8V_DOWN#	+1.8V
H	H	1.8V
L	H	1.7V
H	L	NO CARE
L	L	1.65V

Default Group-A7V8X MX

ASUSTek Computer INC.	Title : +1.8V	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
Date: Monday, November 10, 2008	Sheet 49 of 51	



+VCCP_UP	+VCCP_DOWN#	+VCCP
H	H	0.96V
L	H	0.89V
H	L	NO CARE
L	L	0.85V

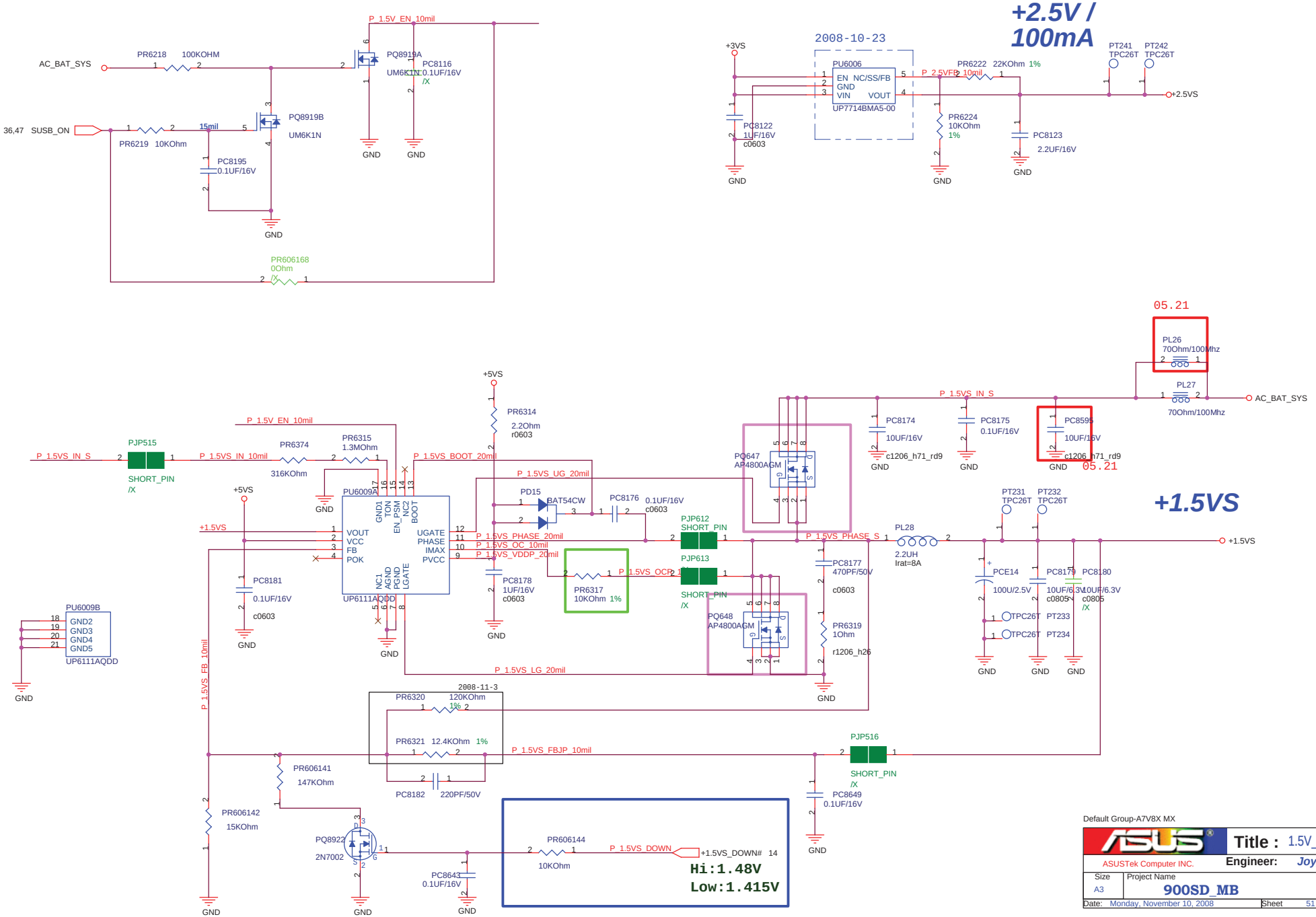
2008-11-3

0.955V
0.886V

0.852V

Default Group-A7V8X MX

ASUSTek Computer INC.	Title : VCCP	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0C
Date: Monday, November 10, 2008	Sheet 50 of 51	



Default Group-A7V8X MX

ASUSTek Computer INC.	Title : 1.5V_2.5V	
	Engineer: Joy_Zhou	
Size: A3	Project Name: 900SD_MB	Rev: R1.0G
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