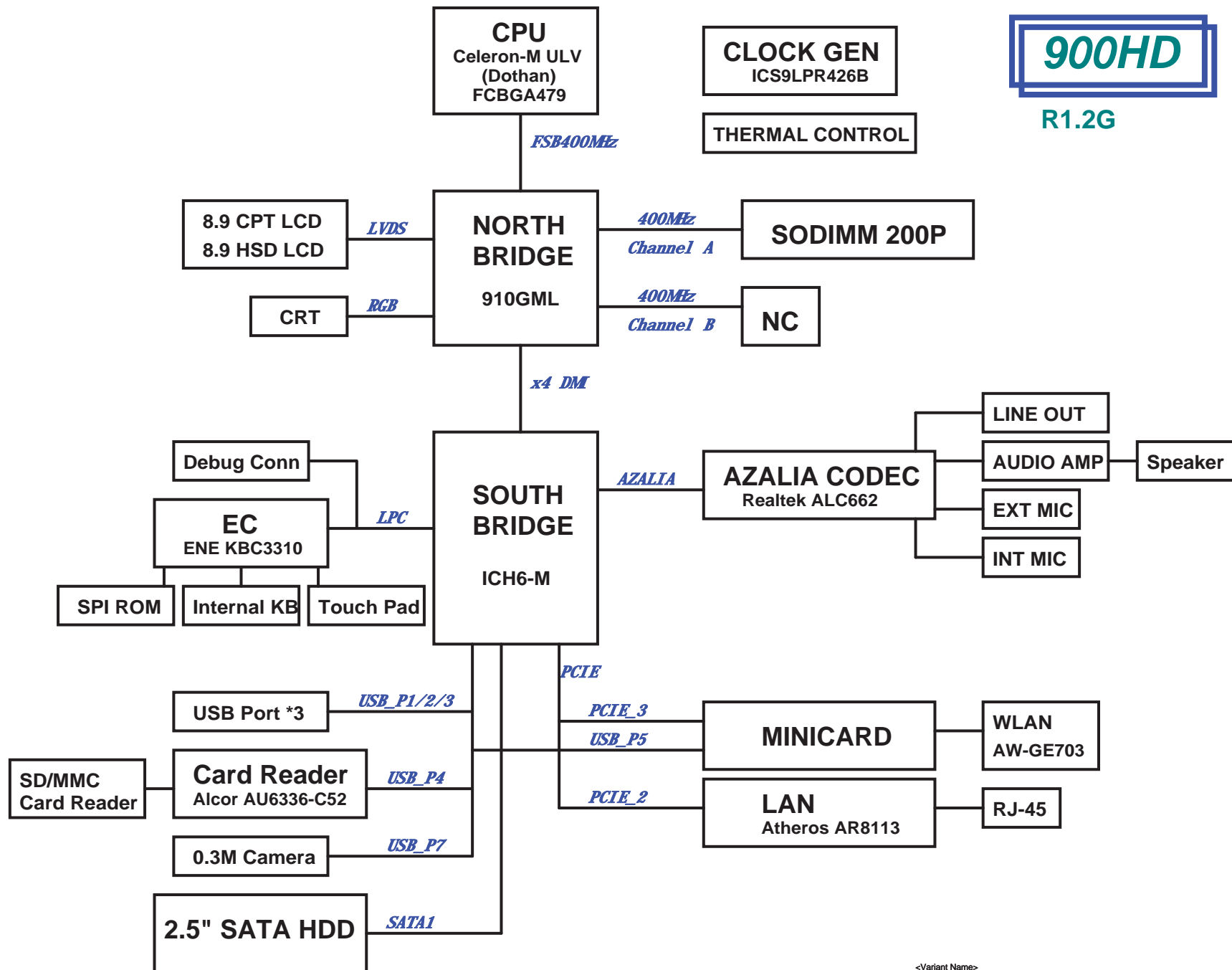


01_Block Diagram
 02_System Setting
 03_Power Sequence
 04_EC Pin Define
 05_History
 06_*
 07_Clock Gen_ICS9LPR426B
 08_Dothan_HOST
 09_Dothan_PWR_GND
 10_910GML_HOST_DMI
 11_910GML_DRAM
 12_910GML_VGA_LVDS_TV
 13_910GML_PWR
 14_910GML_GND
 15_ICH6-M_Azalia_GPIO_PCI_LAN
 16_ICH6-M_USB_PCIE_DMI_IDE_SATA
 17_ICH6-M_PWR_GND
 18_DDR2_SODIMM
 19_DDR2_Termination
 20_Onboard VGA
 21_LCD Conn
 22_Minicard
 23_LAN_Atheros AR8113
 24_RJ45
 25_SATA HDD
 26_G-Sensor
 27_USB Port
 28_Card Reader_Alcor AU6336-C52
 29_Camera Conn
 30_Codec_ALC662
 31_Audio_AMP_Jack
 32_EC_ENE KB3310
 33_Switch_SPI ROM_Debug Conn
 34_KB_Touch Pad
 35_Thermal Sensor_FAN
 36_LED
 37_Discharge
 38_PWR Jack
 39_Srew Hole
 40_EMI
 41_POWER FLOW
 42_CHARGER
 43_VCORE_VCCP(5.5A)
 44_POWER_3V_5V_VTT_DDR
 45_POWER_3VA_3VSB_5VSB
 46_POWER_1.5V_2.5V
 47_POWER_1.8V_DUAL




ICH6 GPIO SETTING

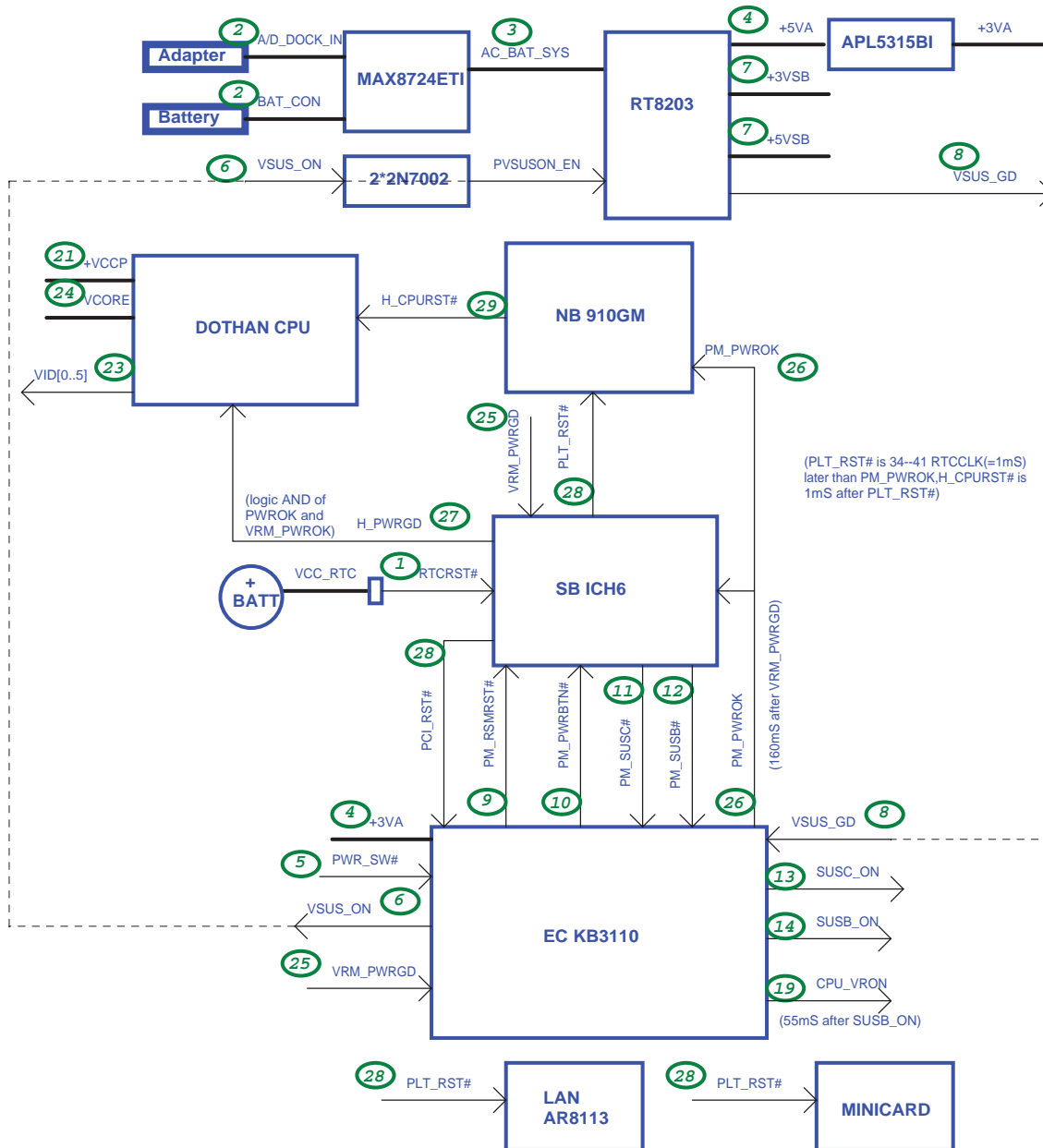
Pin	Pin Name	Connect to	Type	Input/Output Set
B7	GPIO/REQ6#	PCL_REQ#6	I	fixed as Input only 10K Pull +3V
E8	GPI1 / REQ5#	PCL_REQ#5	I	fixed as Input only 10K Pull +3V
D9	GPI2 / PIRQE#	PCL_INTE#(FALLINT1#)	I	fixed as Input only 10K Pull +3V
C7	GPI3 / PIRQF#	PCL_INTF#	I	fixed as Input only 10K Pull +3V
C6	GPI4 / PIRQG#	PCL_INTG#	I	fixed as Input only 10K Pull +3V
M3	GPI5 / PIRQH#	PCL_INTH#	I	fixed as Input only 10K Pull +3V
AD19	GPI6 / BMBUSY#	PM_BMBUSY#	I	Input
AE19	GPI7	THRO_CPU	GPI	fixed as Input only(Reserved)
R1	GPI8	KBC_SC#	GPI	fixed as Input only
C23	GPI9/OC4#	USB_OC#4	I	Input
D23	GPI10/OC5#	USB_OC#5	I	Input
W6	GPI11 / SMBALERT#	S_SMBALERT#	I	Input
M2	GPI12	LID_EC#	GPI	fixed as Input only
R6	GPI13	EXTSMI#	GPI	fixed as Input only
C25	GPI14/OC6#	USB_OC#6	I	Input
C24	GPI15 /OC7#	USB_OC#7	I	Input
D8	GPO16/GTN6#	S_GNT#6	O	Output
F6	GPO17 / GNT5#	S_GNT#5	O	Output
AC21	GPO18 / STP_PC#	STP_PC#	O	Clock GEN STP_PC#
AB21	GPO19	WLAN_LED	GPO	fixed as Output only
AD22	GPO20 / STP_CPU#	STP_CPU#	O	Output
AD20	GPO21	CAMERA_EN	GPO	fixed as Output only
NA	GPIO22	NC	NA	NA
AD21	GPO23	SPEAKER_EN#	GPO	fixed as Output only
V3	GPIO24	MINICARD_EN#	I/O	Output
P5	GPIO25	WLAN_ON#	I/O	Output

Pin	Pin Name	Connect to	Type	Input/Output Set
AF17	GPI26/SATA0GP	S_GPI26 LCD_ID1	GPI	(GPI)Input10K Pull down to GND
R3	GPIO27	CARD_READER_EN#	I/O	Output
T3	GPIO28	BT_EN	I/O	Output(Reserved)
AE18	GPI29 / SATA1GP	PCBVER0	GPI	(GPI)Input
AF18	GPI30 / SATA2GP	S_GPI30 LCD_ID2	GPI	(GPI)Input10K Pull down to GND
AG18	GPI31 / SATA3GP	PCBVER1	GPI	(GPI)Input
AF19	GPIO32 / CLKRUN#	S_CLKRUN#	I/O	Input 10K Pull +3V
AF20	GPIO33	PM_VCOREL1	I/O	Output
AC18	GPIO34	PM_VCOREL2	I/O	Output
NA	GPIO35	NA	NA	NA
NA	GPIO36	NA	NA	NA
NA	GPIO37	NA	NA	NA
NA	GPIO38	NA	NA	NA
NA	GPIO39	NA	NA	NA
F7	GPI40 / REQ4#	S_GNT#4	I	Input 10K Pull +3V
P4	GPI41 / LDRQ1#	S_LDRQ#1 (NC)	I	Input
NA	GPIO42	NA	NA	NA
NA	GPIO43	NA	NA	NA
NA	GPIO44	NA	NA	NA
NA	GPIO45	NA	NA	NA
NA	GPIO46	NA	NA	NA
NA	GPIO47	NA	NA	NA
E7	GPO48 / GNT4#	S_GNT#4 (NC)	O	Output
AC25	GPO49 / CPUPWRGD	H_PWRGD	O	Output

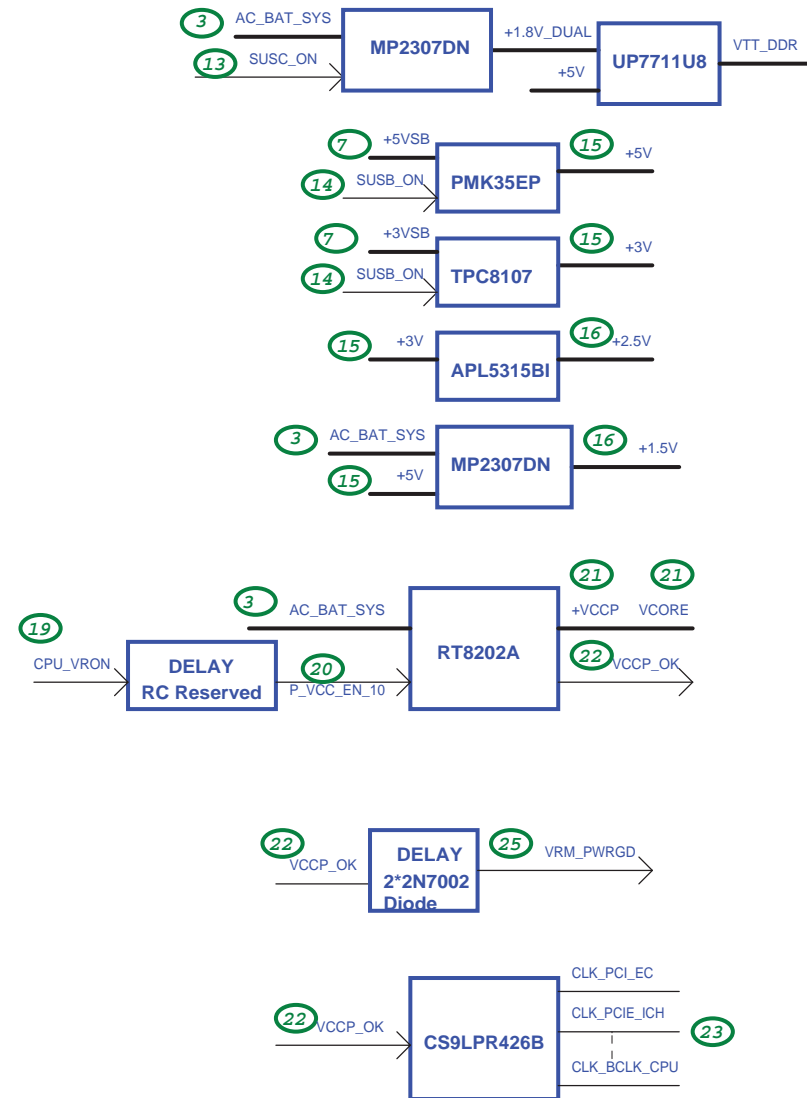
<Variant Name>

		Title : System Setting	
ASUSTek Computer INC.		Engineer: Brian_Liu	
Size A3	Project Name 900HD	Rev 1.2G	
Date: Wednesday, August 06, 2008		Sheet	2 of 47

*This sequence is for Battery Plug-in and no Adapter,
if Adapter Plug-in, the sequence change to:
A/D_DOCK_IN--->AC_BAT_SYS--->+3VA--->VSUS_ON--->+3VSB & +5VSB
--->VSUS_GD--->PM_REMRST#--->PWR_SW#--->PM_PWRBTN--->PM_SUSC#--->PM_SUSB#



	Signal	S0/S1	S3	S4/S5	Power
Only Battery	VSUS_ON	H	H	L	VSB
Adapter In	VSUS_ON	H	H	H	VSB
	SUSB_ON	H	L	L	Main
	SUSC_ON	H	H	L	DUAL



EC KB3310 GPIO SETTING

Pin	Pin Name	Signal Name	Type	NOTE
1	GPIO00/GA20	A20GATE	O	A20GATE
2	GPIO01/KBRST#	RC_IN#	O	KBRST#
6	GPIO04	EMAIL_SW#	I	Internal pull high
13	GPIO05/PCIRST#	PCI_RST#	I	PCI Reset
14	GPIO07	BAT_OTP	I	Battery over temperature
15	GPIO08	EXTSMI#	O/OD	EXTSMI#, 10K Pull up +3VSB
16	GPIO0A	LID_EC#	I	Internal pull high
17	GPIO0B/ESB_CLK	NC	O	
18	GPIO0C/ESB_DAT	NC	I/O	
19	GPIO0D	DISTP_SW#	I	Touch Pad Disabled,*
20	GPIO0E/SC#	KBC_SC#	O	KBC_SC#, 10K Pull +3VSB
21	GPIO0F/PWM0	BL_PWM_DA	O	
23	GPIO10/PWM1	BAT_CRITICAL	O	Battery critical capacity
25	GPIO11/PWM2	PM_PWRBTN#	OD	Power Button to SB, *
26	GPIO12/FANPWM1	FAN0_PWM	O	CPU Fan
27	GPIO13/FANPWM2	FAN1_PWM	O	VGA Fan(Unused)
28	GPIO14/FANFB1	FAN0_TACH	I	CPU FanTach
29	GPIO15/FANFB2	FAN1_TACH	I	VGA FanTach(Unused)
30	GPIO16/E51_TX	E51_TX	O	RS232 debug port
31	GPIO17/E51_RX	E51_RX	I	RS232 debug port
32	GPIO18	PWR_SW#	I	power button, *
34	GPIO19/PWM3	MAIL_LED#	O	Mail LED(Unused)
36	GPIO1A/NUMLED	NUM_LED#	O	EC H/W controls(Unused)
38	GPIO1D/CLKRUN#	N.C	O	Reserved
39	GPIO20/KSO0/TP_TEST	KSO0	O	For Keyboard interface
40	GPIO21/KSO1/TP_PLL	KSO1	O	For Keyboard interface
41	GPIO22/KSO2	KSO2	O	For Keyboard interface
42	GPIO23/KSO3	KSO3	O	For Keyboard interface
43	GPIO24/KSO4	KSO4	O	For Keyboard interface
44	GPIO25/KSO5	KSO5	O	For Keyboard interface
45	GPIO26/KSO6	KSO6	O	For Keyboard interface
46	GPIO27/KSO7	KSO7	O	For Keyboard interface
47	GPIO28/KSO8	KSO8	O	For Keyboard interface
48	GPIO29/KSO9	KSO9	O	For Keyboard interface
49	GPIO2A/KSO10	KSO10	O	For Keyboard interface
50	GPIO2B/KSO11	KSO11	O	For Keyboard interface
51	GPIO2C/KSO12	KSO12	O	For Keyboard interface
52	GPIO2D/KSO13	KSO13	O	For Keyboard interface
53	GPIO2E/KSO14	KSO14	O	For Keyboard interface
54	GPIO2F/KSO15	KSO15	O	For Keyboard interface
55	GPIO30/KSI0	KSI0	I	For Keyboard interface
56	GPIO31/KSI1	KSI1	I	For Keyboard interface
57	GPIO32/KSI2	KSI2	I	For Keyboard interface
58	GPIO33/KSI3	KSI3	I	For Keyboard interface
59	GPIO34/KSI4	KSI4	I	For Keyboard interface
60	GPIO35/KSI5	KSI5	I	For Keyboard interface
61	GPIO36/KSI6	KSI6	I	For Keyboard interface
62	GPIO37/KSI7	KSI7	I	For Keyboard interface
63	GPI38/AD0	BAT_I_CHG	I	Sense Power Loading(Rsv.)
64	GPI39/AD1	BAT_CONFIG	I	Battery configuration (Rsv.)
65	GPIO3A/AD2	BAT_SENT	I	Battery Voltage Sensor (Rsv.)
66	GPIO3B/AD3	BAT_TS	I	Battery Thermal Sensor
68	GPO3C/DA0	DOC	O	Trigger Clock Gen

Pin	Pin Name	Signal Name	Type	NOTE
70	GPO3D/DA1	LCD_BACKOFF#	O	LCD_BACKOFF#
71	GPO3E/DA2	CLK_PWRSAVE#	O	Active when BAT_IN=1 and AC_OK=0(Unused)
72	GPO3F/DA3	PM_BATLOW#	O	Battery Low Low
73	GPIO40	AC_OK	I	AC Adaptor Plug in
74	GPIO41	EC_RSMRST#	O	10K Pull GND
75	GPI42	BAT_IN	I	
76	GPI43	CLRTC_EC	I	
77	GPIO44/SCL1	SMB1_CLK	I/OD	4.7K Pull +3VA
78	GPIO45/SDA1	SMB1_DAT	I/OD	4.7K Pull +3VA
79	GPIO46/SCL2	SMB2_CLK	I/OD	10K Pull +3V
80	GPIO47/SDA2	SMB2_DAT	I/OD	10K Pull +3V
81	GPIO48/KSO16	KB pin 28	O	for KB type detection(Rsv.)
82	GPIO49/KSO17	KB pin 27	O	for KB type detection(Rsv.)
83	GPIO4A/PSCLK1	LCD_SCL	O	for AUO, default H at S0(Rsv.)
84	GPIO4B/PSDAT1	LCD_SDA	O	for AUO, default L at S0(Rsv.)
85	GPIO4C/PSCLK2	LCD_CSB	O	for AUO, default H at S0(Rsv.)
86	GPIO4D/PSDAT2	LCD_VSYNC	O	for AUO 7" Panel(Reserved)
87	GPIO4E/PSCLK3	TP_CLK	I/OD	10K Pull +3V
88	GPIO4F/PSDAT3	TP_DAT	I/OD	10K Pull +3V
89	GPIO50/SELIO#	BATSEL_3S	O	Battery series, H:3S, L:4S
90	GPIO52/E51_CS#	CHG_LED_UP#	O	charger LED
91	GPIO53/CAPLED	CAP_LED#	O	EC H/W controls
92	GPIO54	PWR_LED_UP	O	EC H/W blinking
93	GPIO55/SCRLED	SCRLED_LED#	O	EC H/W controls
95	GPIO56	PWR4G_SW#	I	*
97	GPXOA00/SDICS#	SPI_MODE#	O	*HW Strap for SPI Flash de External Pull Down 4.7K ohm to GND*
98	GPXOA01/SDICLK	SUSC_ON	O	
99	GPXOA02/SDIDO	VSUS_ON	O	
100	GPXOA03	CPU_VRON	O	
101	GPXOA04	SUSB_ON	O	
102	GPXOA05	EC_PWROK	O	
103	GPXOA06	PM_LEVELDOWN#	O	
104	GPXOA07	CHG_EN#	O	Battery charging enabled
105	GPXOA08	PRECHG	O	
106	GPXOA09	SPI_WP#	O	
107	GPXOA10	OP_SD#	O	Audio OP
108	GPXOA11	BAT_LEARN	O	
109	GPXID0/SDIDI	BATSEL_2P#	O	Battery parallel, Hi:1P, Lo:2P-3P
110	GPXID1	CPU_LEVELDOWN#	O	
112	GPXID2	THRO_CPU	O	Active if CPU Temperature is over spec
114	GPXID3	SUSB#	I	Pull Down 100K ohm to GND
115	GPXID4	SUSC#	I	Pull Down 100K ohm to GND
116	GPXID5	CPUPWR_GD	I	10K Pull +3V
117	GPXID6	VSUS_GD	I	Disabled **
118	GPXID7	BATSEL_Life	O	Reserved
121	GPI057	INTERNET#	I	*
126	GPIO57/SPICLK	SPI_CLK	O	SPI Clock
127	GPIO59/TEST_CLK	N.C	O	Reserved

EC KB3310 Other Pin SETTING


Pin	Pin Name	Signal Name	Type	NOTE
3	SERIRQ	INT_SERIRQ	I/OD	10K Pull +3V
4	LFRAME#	LPC_FRAME#	I	
5	LAD3	LPC_AD3	I/O	
7	LAD2	LPC_AD2	I/O	
8	LAD1	LPC_AD1	I/O	
9	VCC	+3VA	P	
10	LAD0	LPC_AD0	I/O	
11	GND	GND	P	
12	PCICLK	CLK_PCI_EC	I	
22	VCC	+3VA	P	
24	GND	GND	P	
33	VCC	+3VA	P	
35	GND	GND	P	
37	ECRST#	EC_RST#	I	Add 10K ohm to GND
67	AVCC	+3VA_AEC	P	
69	AGND	AGND	P	
94	GND	GND	P	
96	VCC	+3VA	P	
111	VCC	+3VA	P	
113	GND	GND	P	
119	RD#/SPIDI	SPI_SO	I	
120	WR#/SPIDO	SPI_SI	O	
112	XCLKI	32KXCLKI	I	
123	XCLKO	32KXCLKO	O	
124	V18R	K_V18R	P	Reserved 1uF to GND
125	VCC	+3VA	P	
128	SPICS#/SELMEM#	SPI_CE#	O	

<Variant Name>

		Title : EC Pin Define	
ASUSTek Computer INC.		Engineer: Brian_Liu	
Size A3	Project Name 900HD	Rev 1.2G	
Date: Wednesday, August 06, 2008	Sheet	4	of 47

Rev	Date	Description
1.0G	2007/02/26	S701L Schematic 1.0G Beginning
	2007/03/16	S701L 1.0G Gerber Out
1.1G	2007/03/24	S701L Schematic 1.1G Beginning
	2007/04/19	S701L 1.1G Gerber Out
1.0G	2007/04/24	<p>P701(S701L renamed) Schematic 1.0G Beginning</p> <ol style="list-style-type: none"> 1. PC8054, PR6075 /X to N/A 2. Attansic L2 change to Atheros L2(pin to pin) 3. LC1, LC33 /CAP/X to N/A 4. C87 change to X5R to cost down 5. L1, L2, L3 change to 56 NH, R5, R6 change to 75 Ohm to pass CRT EA measure 6. PR48 change to 22K Ohm, PC35 change to 4700PF to fix no VCORE issue 7. PR6074 change to 4.7K Ohm to fix +3VSB OCP issue 8. Clock Gen CY28442-2 change to ICS9LPR367 9. Phase in Power Level Reduce solution, mark "Taipei0508" 10. Card Reader Socket change to SD Socket 12G25100091E 11. Add System FAN circuit 12. Camera change to USB port 7, Minicard change to USB port 5 13. Use SB GPIO27 to Enable/Disable Card Reader UB6225P 14. Use SB GPIO28 to Enable/Disable Modem 15. Card Reader UB6225P share 48M clock from CLock Gen with SB USB part 16. Add D29 to fix LCD_CSB leakage current issue 17. LC29, LC30 change to 27PF to pass EA crystal measure 18. Change vaule of PR73, PR74, PC56 and add PC60 to adjust the power sequence timing between Stand By power and RSMRST# 19. Remove USB port 1 20. Add +5V generate +3V_LCD circuit 21. Remove +5V_CHG generate circuit 22. Use SB GPIO33, GPIO34 to controll the level of VCORE 23. U31 use APL5315BI-TRL to replace MAX8863TEUK(pin to pin, but reference voltage level different) 24. PR59 change to 130K Ohm for both 12V Adapter and 9.8V Adapter <p>P701 1.0G Gerber Out</p>
1.1G	2007/05/31	<p>P701 Schematic 1.1G Beginning</p> <ol style="list-style-type: none"> 1. Remove the 48M clock from CLock Gen to Card Reader UB6225P 2. Clock Gen ICS9LPR367 change to ICS9LPR426 3. Flash Connector increase SATA and USB interface 4. Add Onboard Flash(SM223 + NAND Flash x4) 5. BATT_CON pin 5 connect to GND 6. Q34 pin 1 connect to +3V to fix EC reset issue 7. Remove J1, J2 8. KB pin 28 connect to GND for P701-ISP_CARD 9. Use SB GPO23 to Enable/Disable Audio Amplifier 10. Use SB GPO21 to controll Camera Power 11. Use SB GPIO24 to controll Minicard Power 12. Use SB GPIO25 to Enable/Disable WLAN Ratio 13. Atheros L2 and Minicard SMBUS interface directly pull high 14. LCD_CON pin 20 connect to AC_BAT_SYS <p>P701 1.1G Gerber Out</p>


Rev	Date	Description
1.2G	2007/06/30 1 1	P701 Schematic 1.2G Beginning 1. Add R174 to short DASP pins of Master IDE device and SLave IDE device 2. Use SB GPIO27 to controll Card Reader UB6225P Power 3. PR606084.2 connect to +5V to fix LCD flash issue 4. Adjust SPEAKER pin define 5. Adjust CHARGE LED and WLAN LED lightness 6. Use SB GPI 26, 29, 30, 31 for PCB version 7. Change USB ESD diode for EMI request 8. Add Floating GND TP_GND and Spring TP1 & TP2 for EMI request 9. Change PM_VCOREL1, PM_VCOREL2 default level 10. Add PQ48 to controll +3V_PE to fix WLAN AW-GE780 can't detect issue 11. Power Charger part update circuit for new Adapter 12. Use SB GPI12 to detect LID signal level 13. Add H/W THERMTRIP circuit (page 36) 14. Add U40 to prevent system auto power on after clear CMOS 15. Use SB GPI7 for THRO_CPU 16. Power Charger part update circuit to prevent incorrect Adapter damage boards 17. Q1.1, Q2.1 change to +3V P701 1.2G Gerber Out
1.2G	2007/07/26 1 1	P701 Schematic 1.3G Beginning 1. Add R11 for 801
		902H CIRCUIT UPDATED HISTORY
1.0G	2008/04/28	Modify from P900 1.2G 1. Add 2.5" SATA HDD 2. Delete On board Flash/ MLC Flash Connector 3. Change Clock Gen. from CS9LPR426A to CS9LPR426B 4. Modify DDRI connector to reverse type 5. Reserved LVDS wire to board connector 6. Reserved HALL effect sensor 7. Change 3V/5V power solution 8. Change Charger solution and Battery Connector 9. Combine VCCP and VCORE power solution 10. Change Battery connector to support Life-battery
1.1G	2008/06/23	1. Change project name from 902H to 900HD 2. Add Panel EDID interface to NB 3. Change LAN controller from Atheros L2 to Atheros AR8113 4. Reserved G-sensor solution 5. Reserved USB port power switch to replace polyswitch 6. Change DC_PWR bead from 1812 size to 1206 size 7. Change VCCP/VCORE power regulation control from PM_LEVELDOWN# to CPU_LEVELDOWN# 8. Change 19V voltage protect circuit 9. Modify BOM for charger charging current change 10. Modify +3V power switch circuit Reserved external power good circuit for Life-battery use

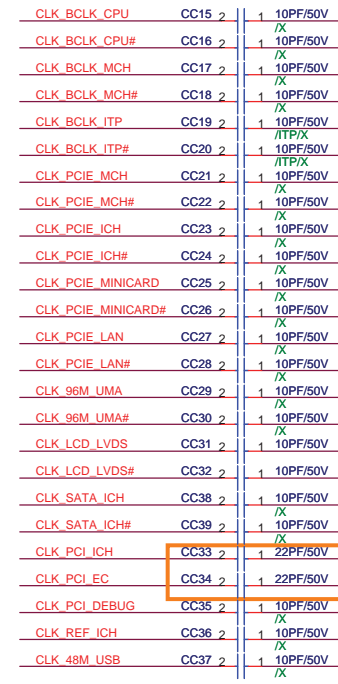
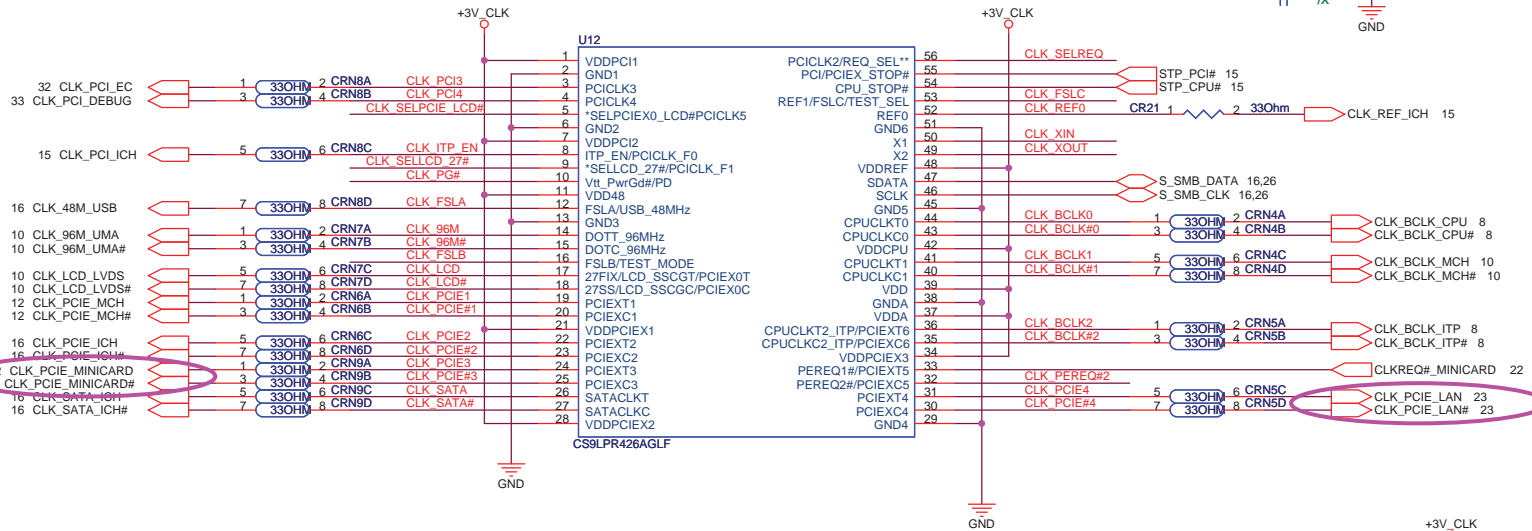
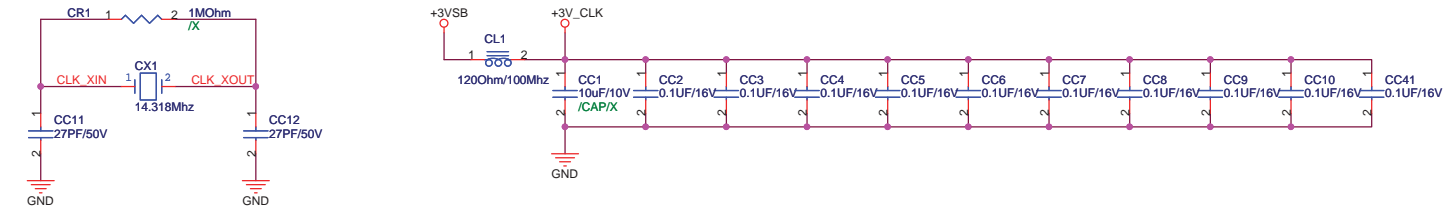
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ASUSTek Computer INC.		Engineer: <u>Brian_Liu</u>	
Size A3	Project Name 900HD		Rev 1.2G
Date: <u>Wednesday, August 06, 2008</u>		Sheet	<u>5</u> of <u>47</u>

900HD CIRCUIT UPDATED HISTORY

1.2G	2008/07/29	<ol style="list-style-type: none"> 1. Change Clock Gen. back to CS9LPR426AGLF 2. Reserved Reset signal and modify power switch of Minicard 3. Remove VGA 2nd source 12G10110015N 4. Change BOM mount LC52 5. Change Card Reader controller from ENE UB6225 to Alcor AU6336-C52-MIF 6. Reserved DC_PWR bead both 1812 size and 1206 size 7. Don't mount PD602 8. Change RT8202A to UP6111A 9. Change PU380; PU302; U31 from APL5315BI to G923 11. Change BOM of R69; R70; PR382; PR312 12. Reserved 0.1uF cap for +VCCP/ +3VSB/ +5VSB 13. Change +2.5V output cap from 10uF to 1uF 14. Swap L_DDC_CLK/L_DDC_DATA 15. Delete PM_RSMRST# pull down SRN9D 16. Add OD1, OD2, OR23, OR24, for PM_RSMRST# and PM_PWROK 17. Change HCE2 from 11G08D210728 100U/2V to 11G08D210790 100U/2.5V 18. Mount R240, R241 19. Don't mount C15, change R171 from 100K to 10K, mount C199 0.1uF 20. Change PR506 from 25.5K to 62K, let VCCP from 1.0497V down to 1.01V (+Vcore: 1.00V) 21. Change PR308 from 22K to 28.7K, let 1.5V down to 1.43V 22. Change PR404 from 47K to 100K, let 1.8V down to 1.72V 23. Modify TP1, TP2 symbol nb_emi_spring_156x108
1.2G	2008/07/31 2008/08/4	<ol style="list-style-type: none"> 24. Change PR307 from 4.22K to 4.7K; PR308 from 28.7K to 47K, let 1.5V down to high voltage at 1.43V and low voltage at 1.35V 25. Remove PD605 2nd source due to their height limit 26. Install PC1007 0.1uF 27. Install PC1008, PC1009 0.1uF

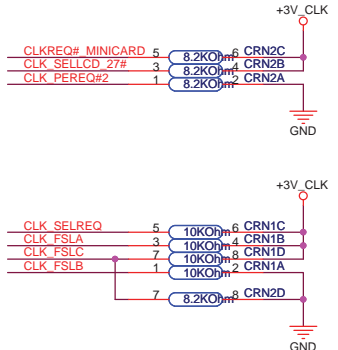
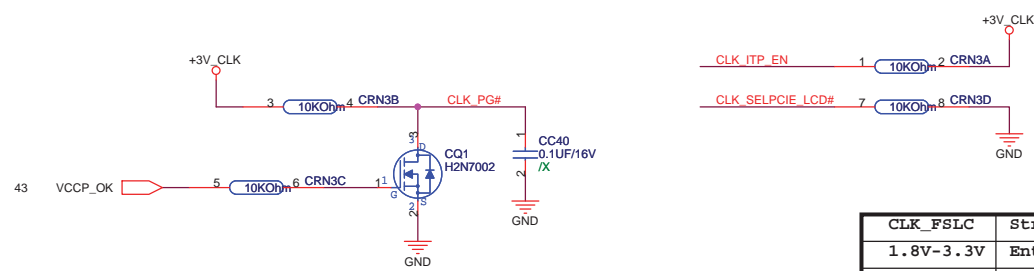
<Variant Name>

		Title : History2	
ASUSTek Computer INC.		Engineer: Brian_Liu	
Size A3	Project Name 900HD		Rev 1.2G
Date: Friday, August 08, 2008		Sheet	6 of 47



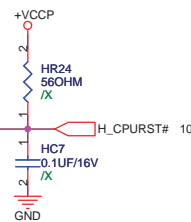
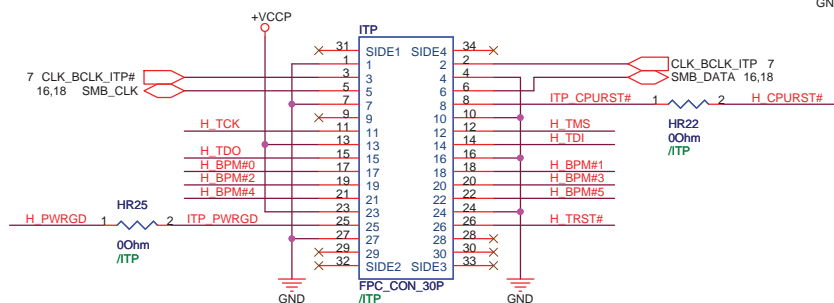
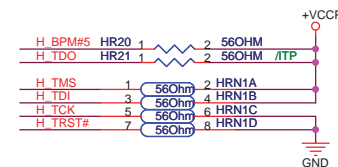
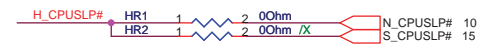
900HD與P900 R1.2G PCIE-Clock不同之處:
為了meet CLK_PCIE_MINICARD diff. pair <= 8"
所以與CLK_PCIE_LAN diff. pair對調

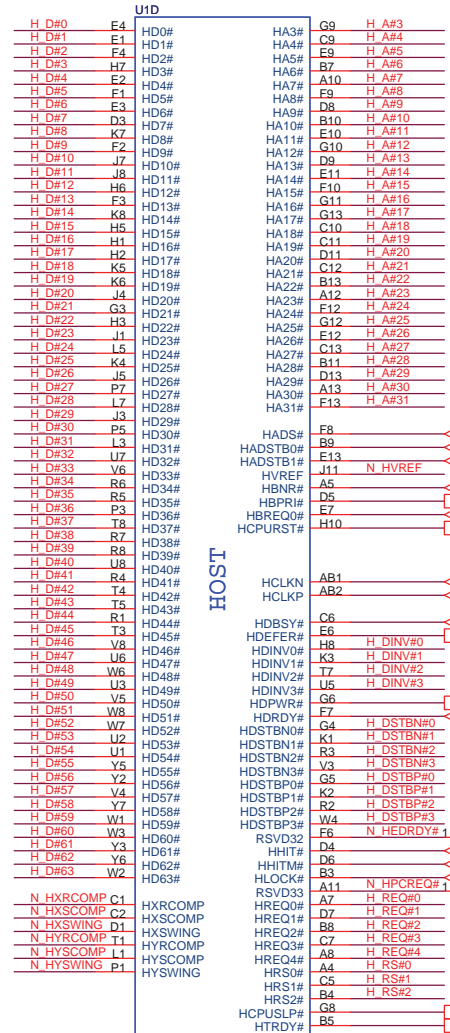
902H R1.0G與P900 R1.2G Clock Gen.不同之處:
426A: 5組PLL, 426B: 3組PLL
900HD R1.2G Clock Gen. 改回426A



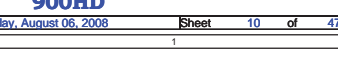
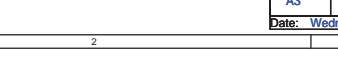
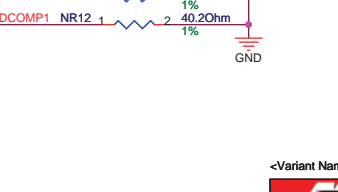
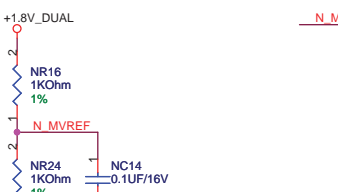
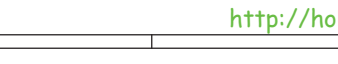
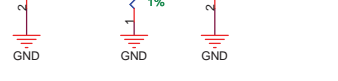
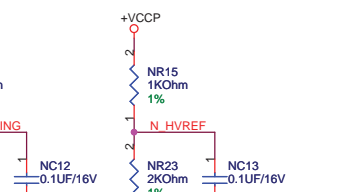
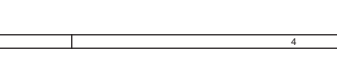
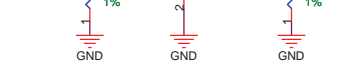
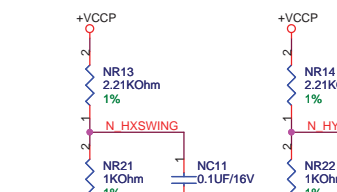
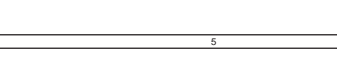
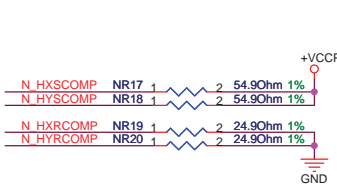
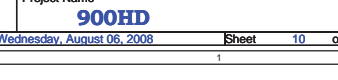
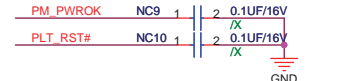
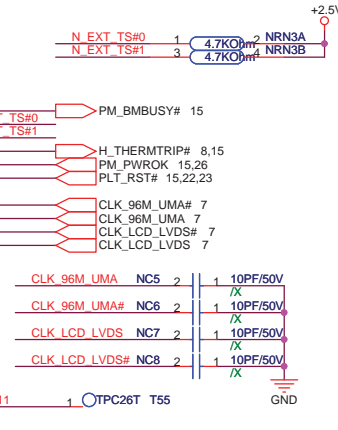
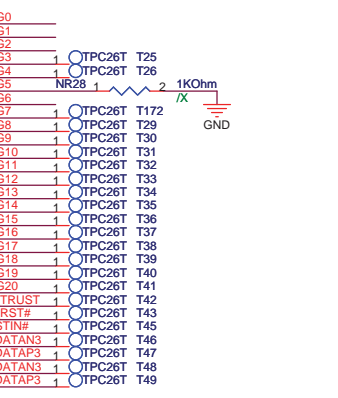
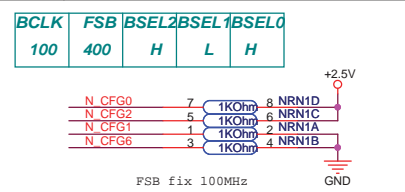
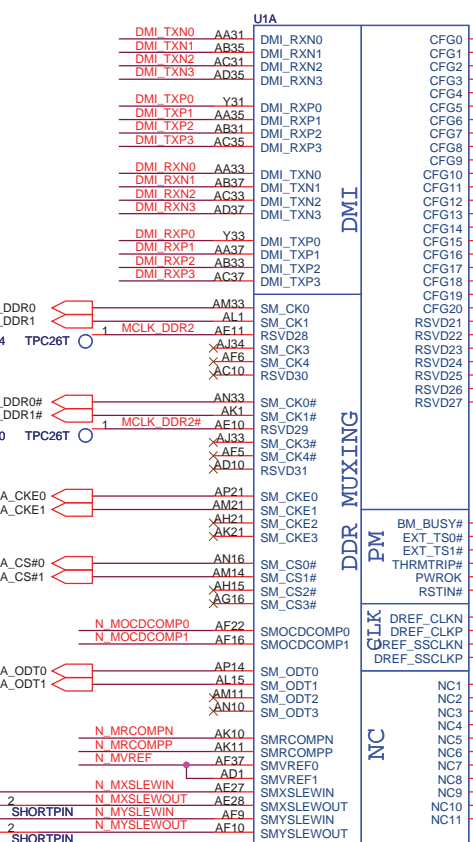
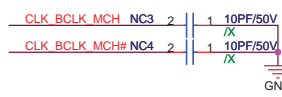
CLK_FSLC	Strapping Define
1.8V-3.3V	Enter Test Mode
0.7V-1.8V	FSB trap High
0V-0.35V	FSB trap Low

	100MHz	133MHz
FSLA	1	1
FSLB	0	0
FSLC	1	0





U1 use 02G010007612

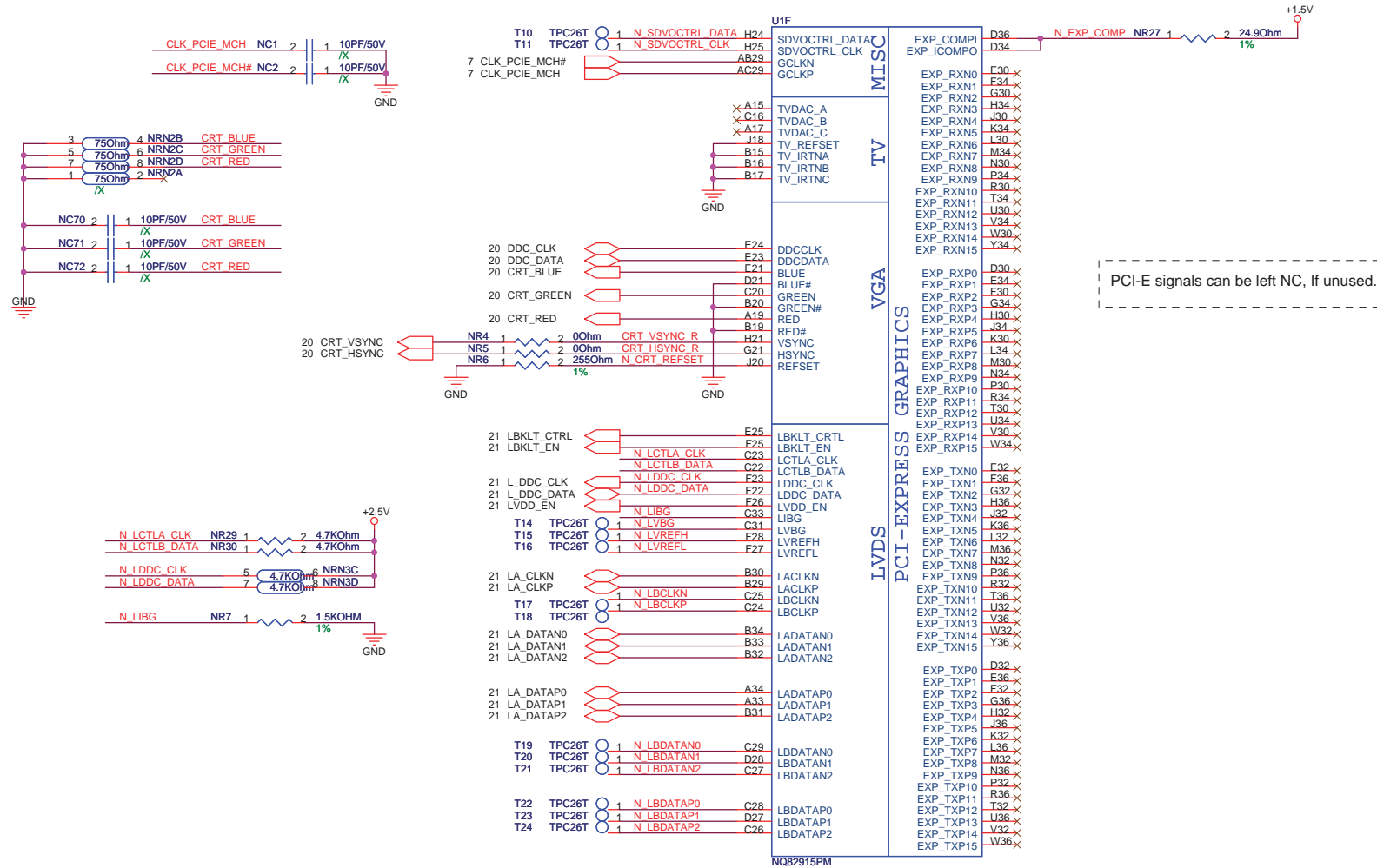




SDVO SMBus have internal pull down

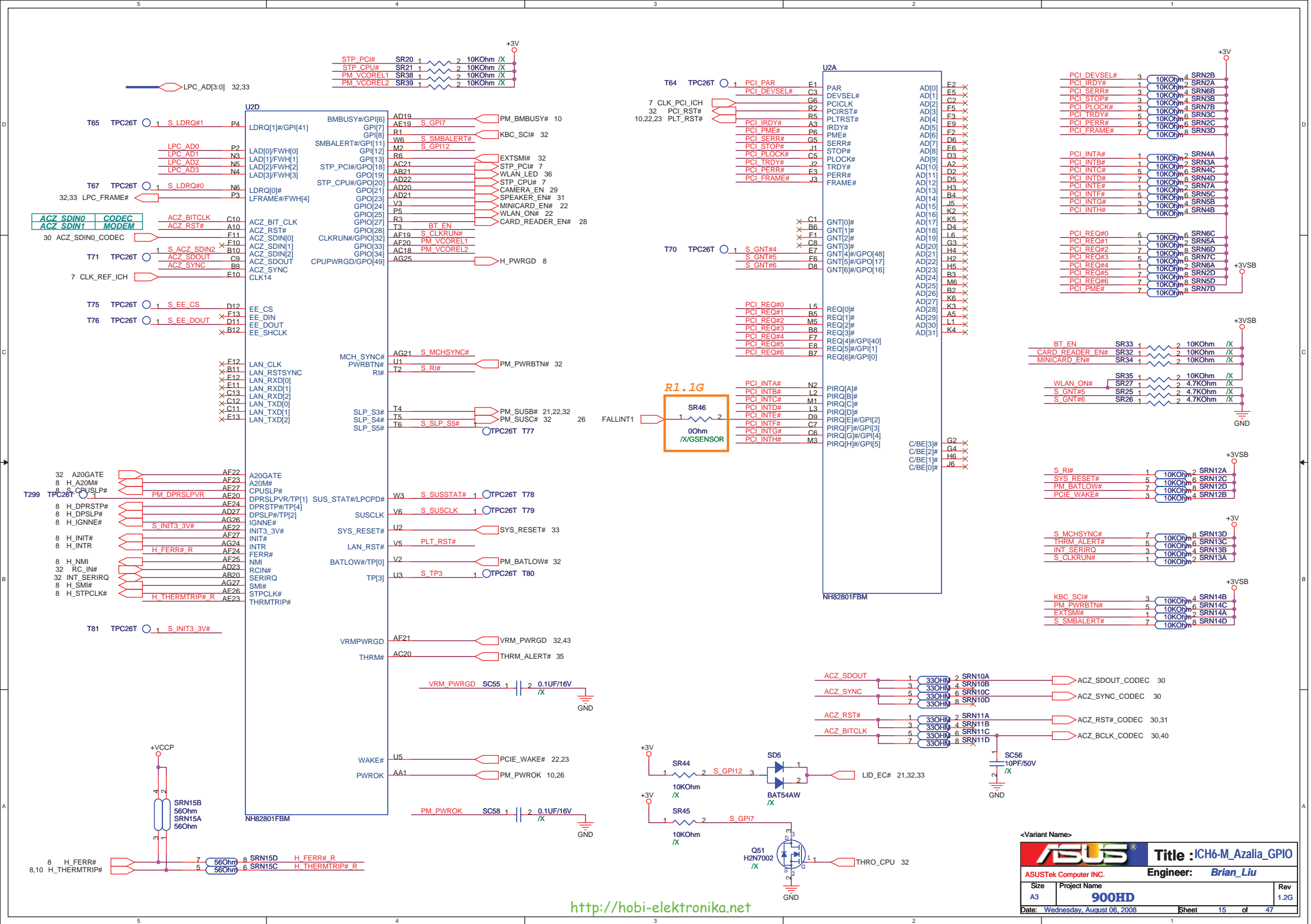
SDVOCRTL_DATA Int PD
0 : No SDVO device
1 : SDVO device present

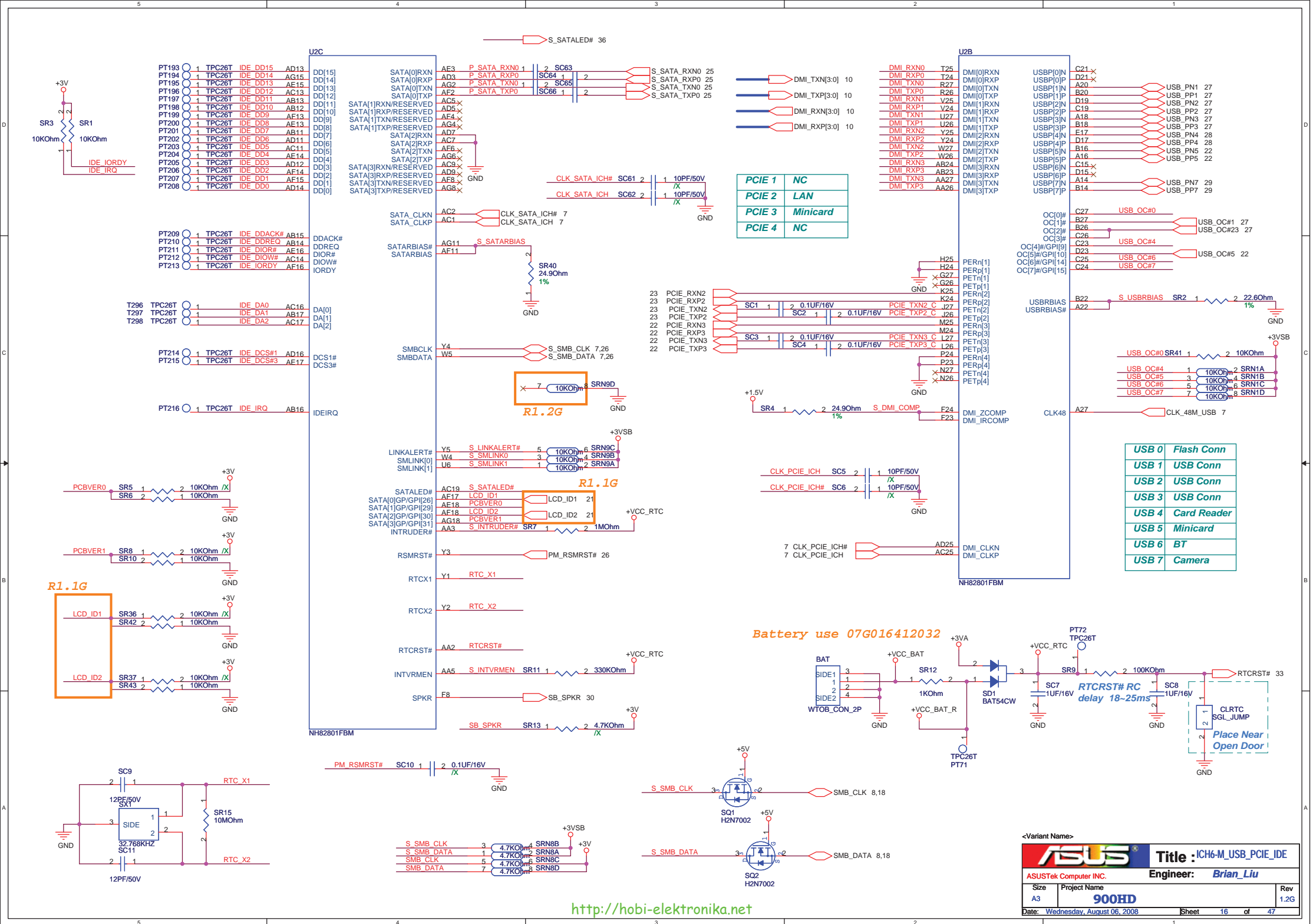
U1 use 02G010007612

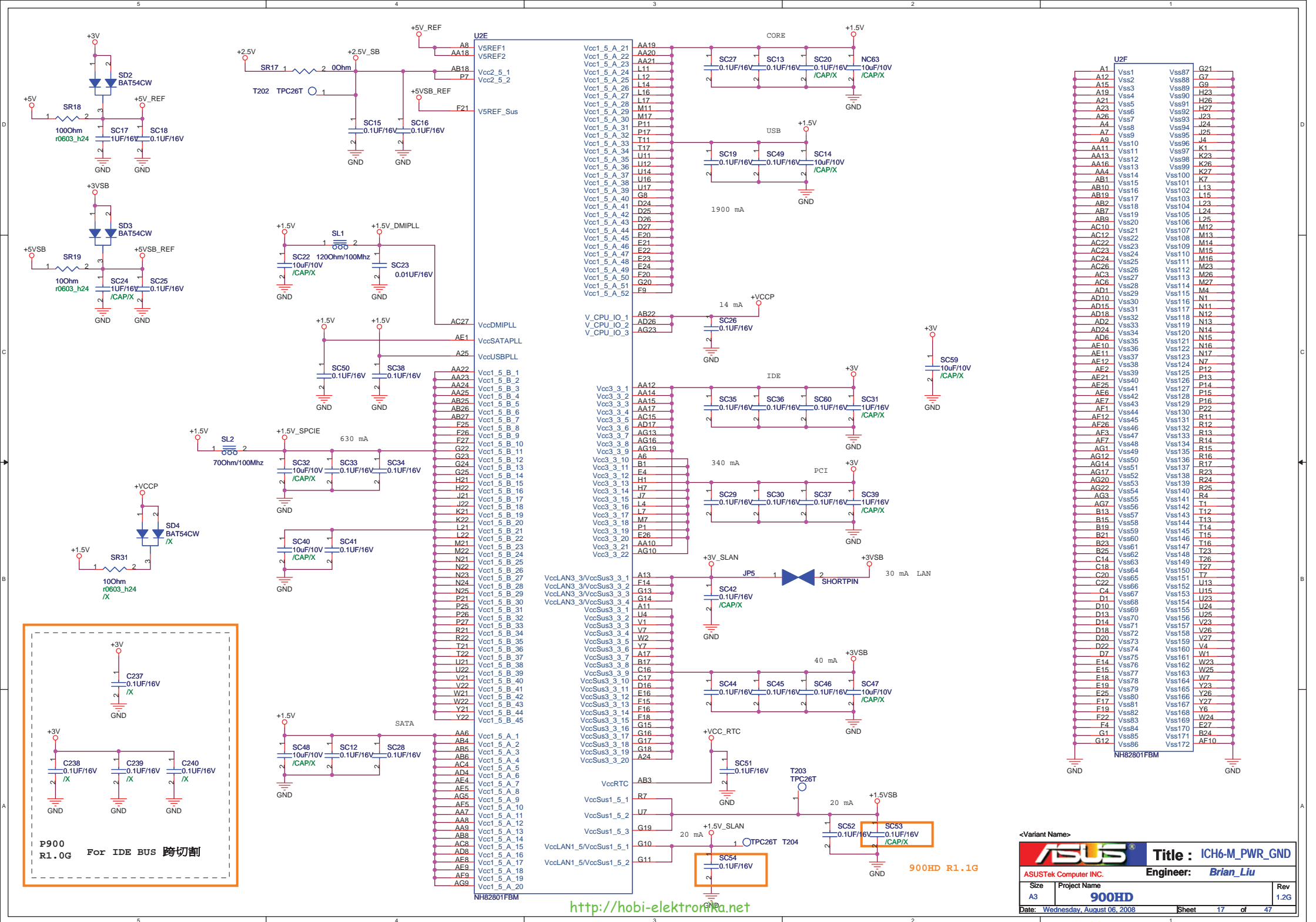


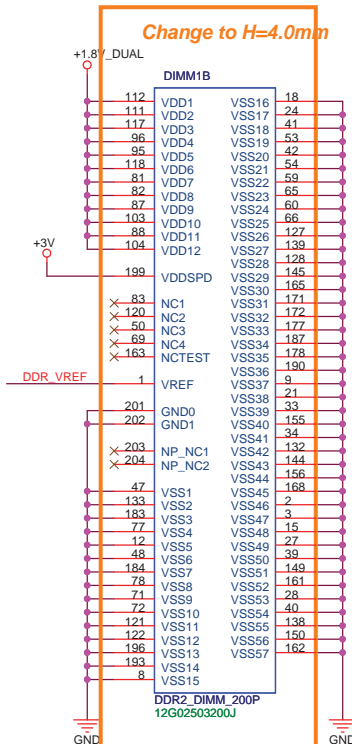
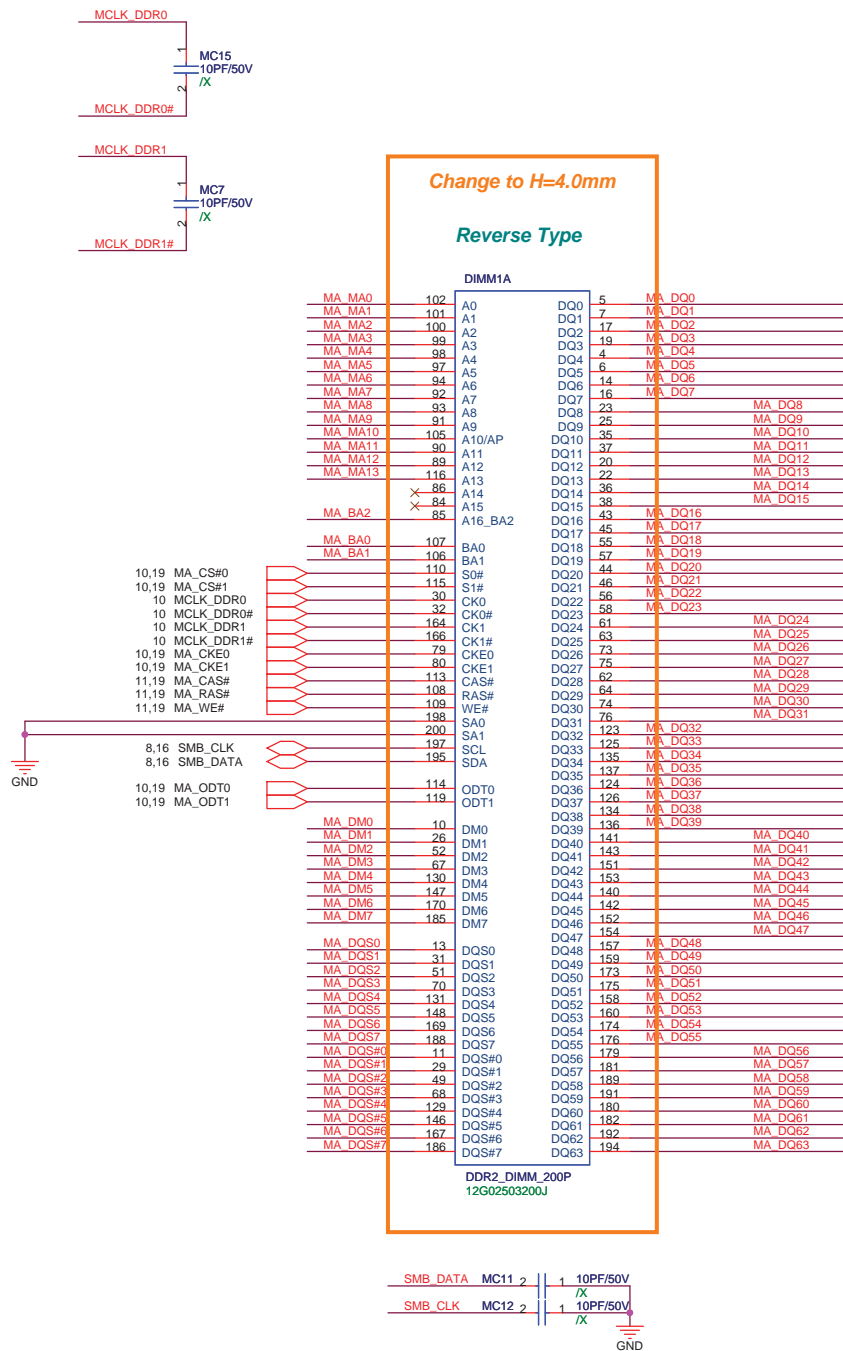
PCI-E signals can be left NC, if unused.

<Variant Name>

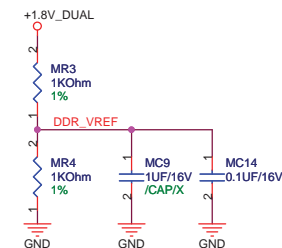
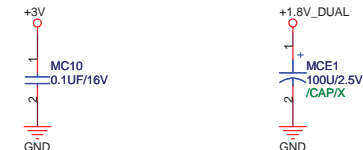
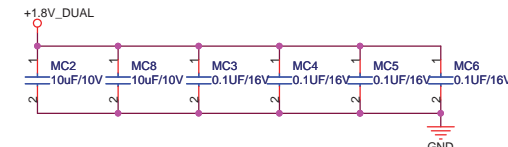






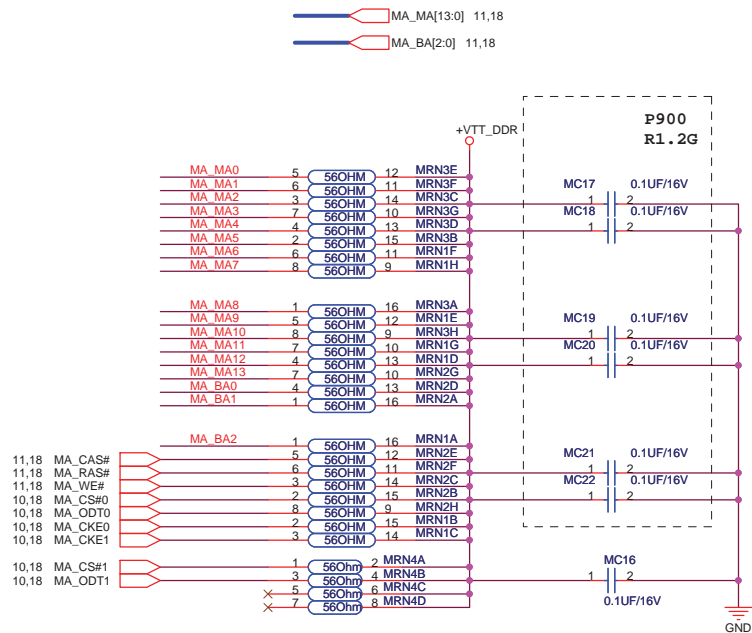


- MA_DQ[63:0] 11
- MA_DQS[7:0] 11
- MA_DQS#[7:0] 11
- MA_DM[7:0] 11
- MA_MA[13:0] 11,19
- MA_BA[2:0] 11,19

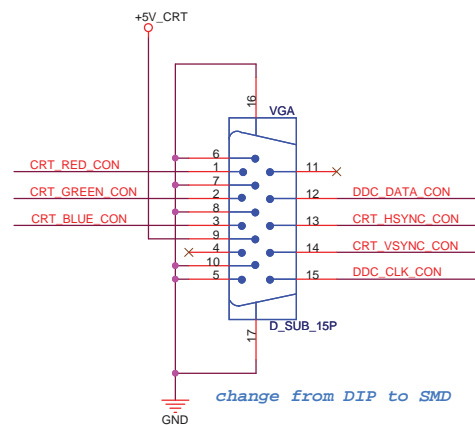
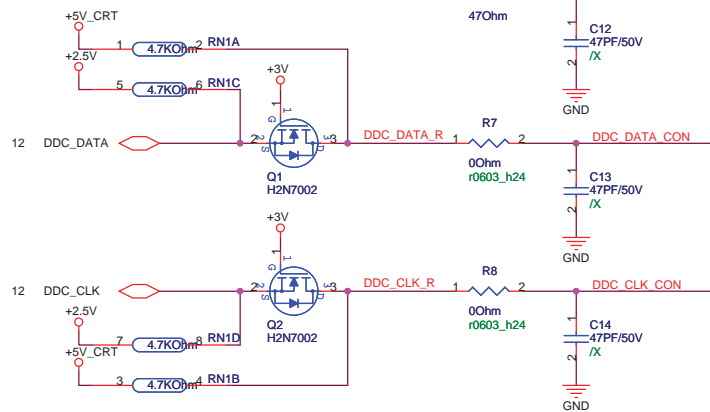
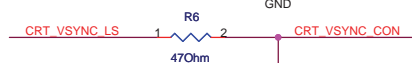
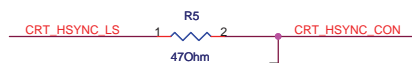
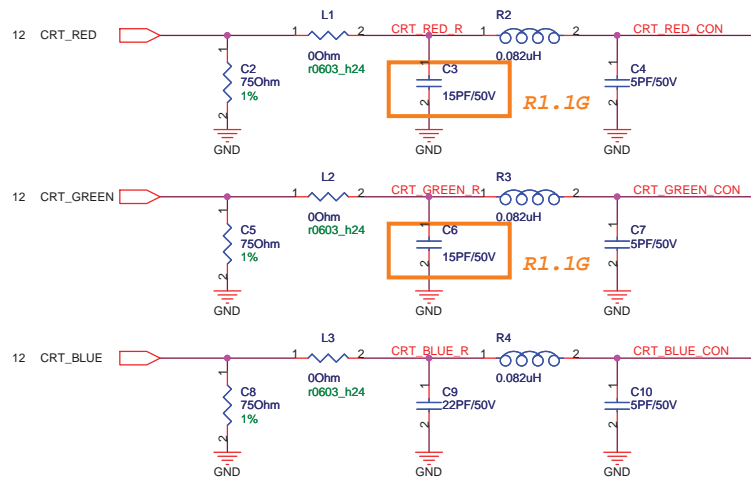


<Variant Name>

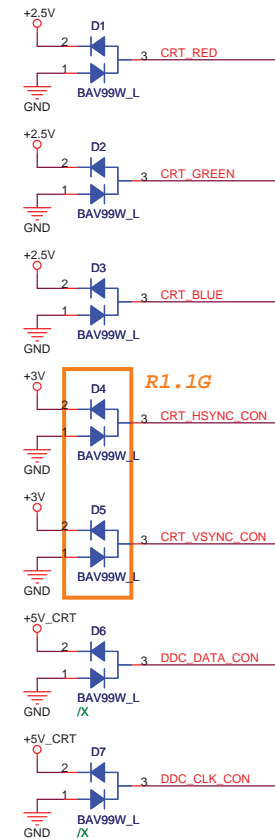
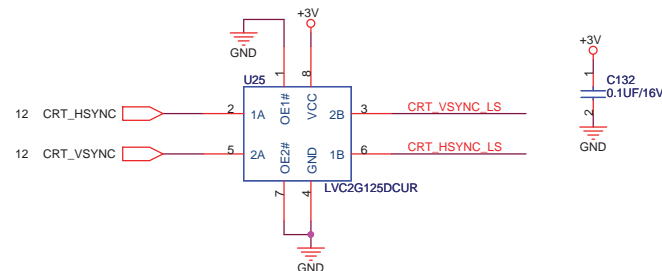
ASUS		Title : DDR2 SODIMM	
ASUSTek Computer INC.		Engineer: Brian_Liu	
Size	Project Name	Rev	
A3	900HD	1.2G	
Date: Wednesday, August 06, 2008	Sheet	18	of 47



<Variant Name>

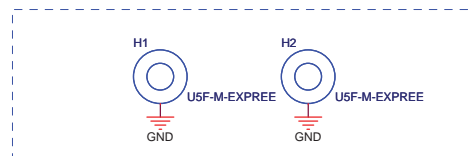
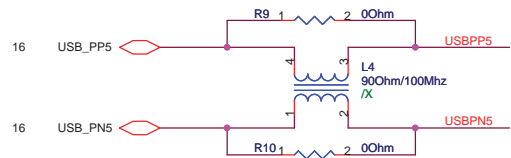


VGA use 12G10110015W

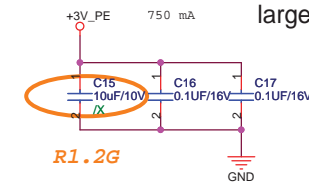


<Variant Name>

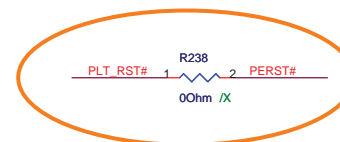
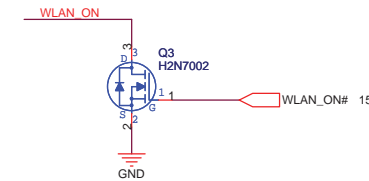
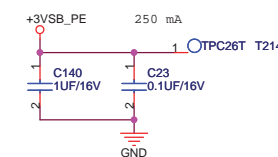
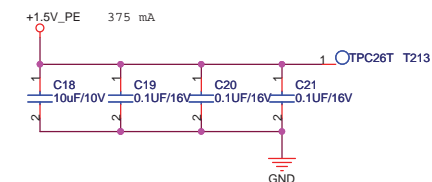
ASUS		Title : Onboard VGA	
ASUSTek Computer INC.		Engineer: Brian_Liu	
Size	Project Name	Rev	
A3	900HD	1.2G	
Date: Wednesday, August 06, 2008	Sheet	20	of 47



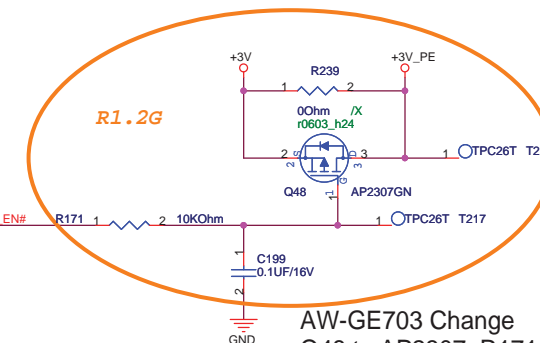
MINI CARD NUT(1.6mm) *2



R1.2G



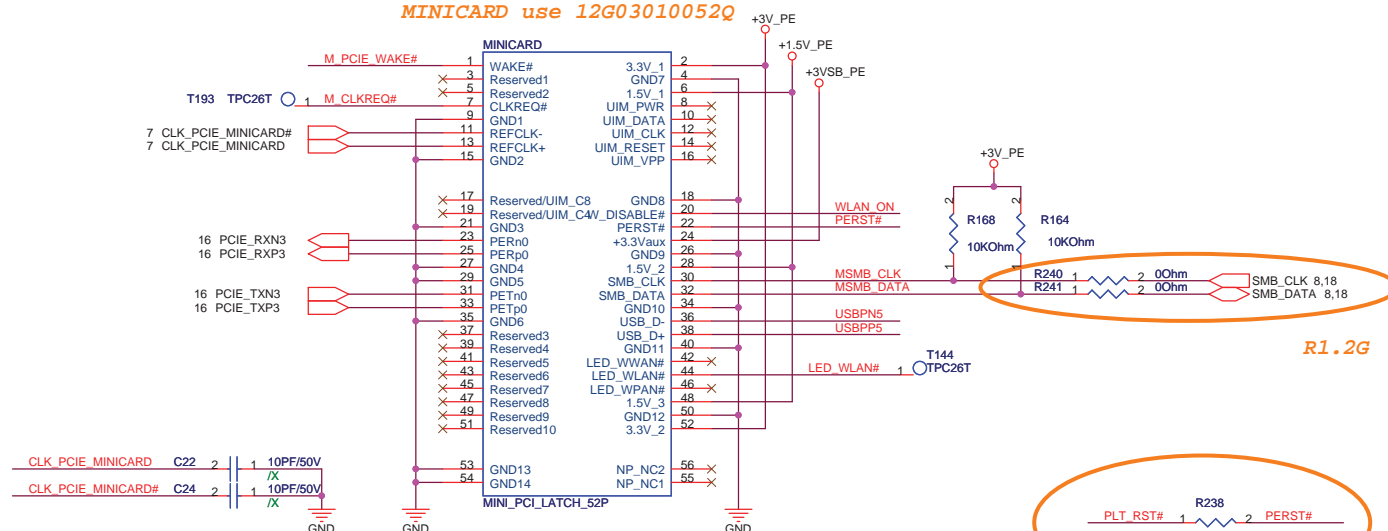
R1.2G



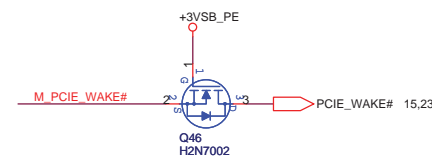
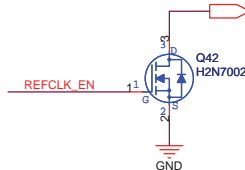
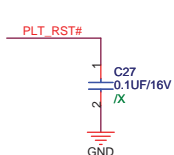
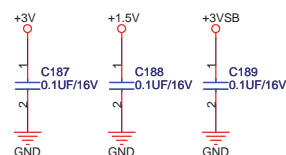
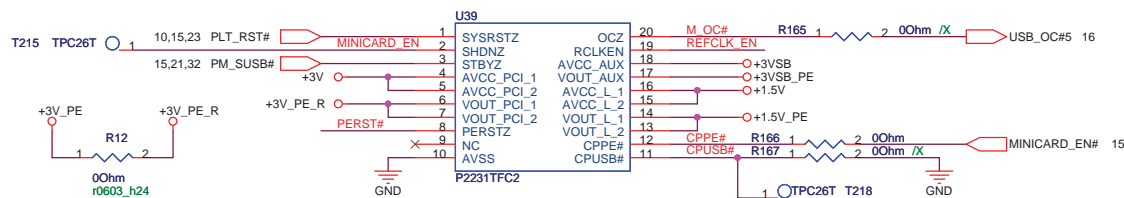
R1.2G

AW-GE703 Change Q48 to AP2307, R171 10K C199 0.1uF to solve too large inrush current

MINICARD use 12G03010052Q

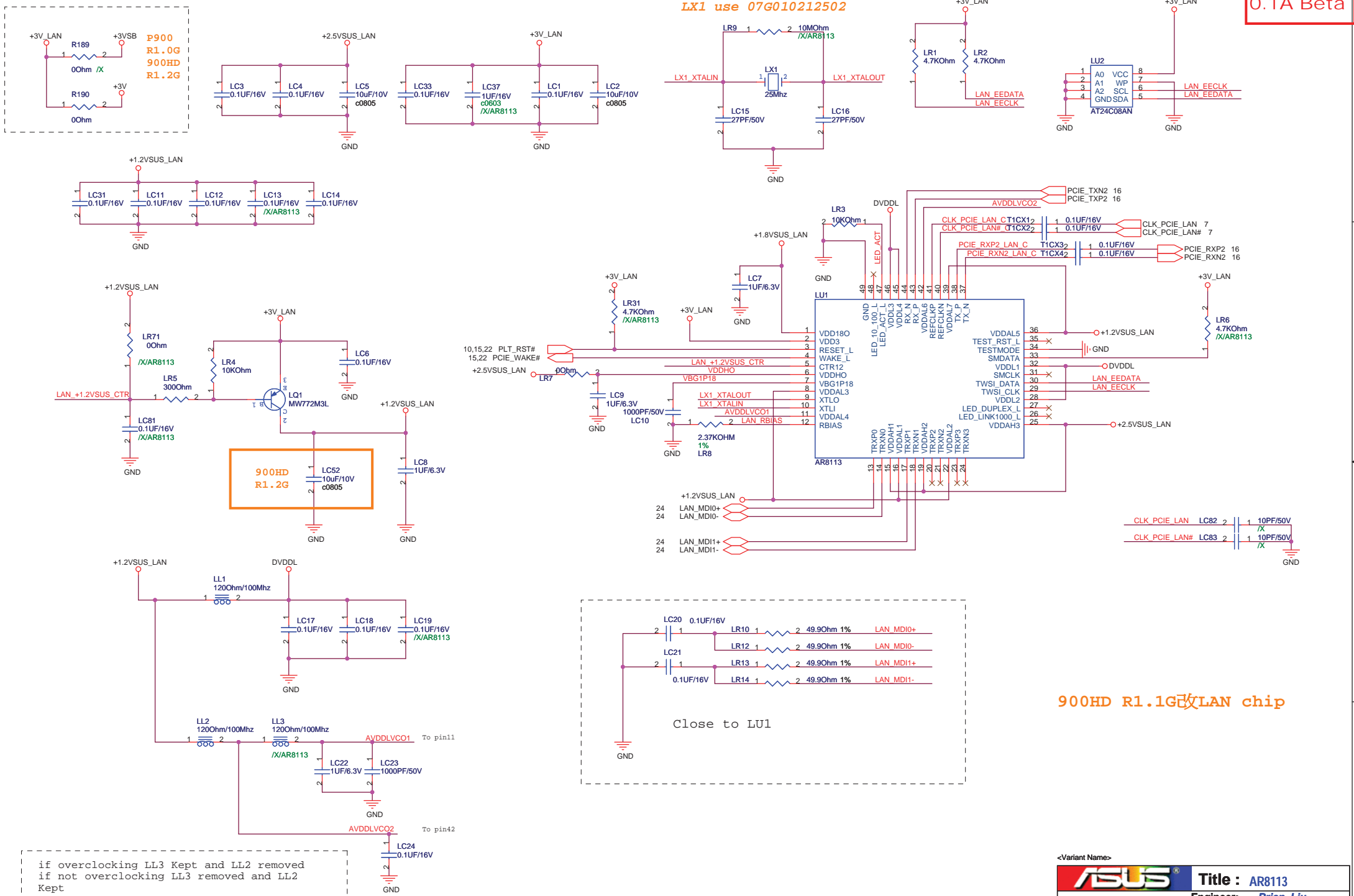


U39 use 06G030057011



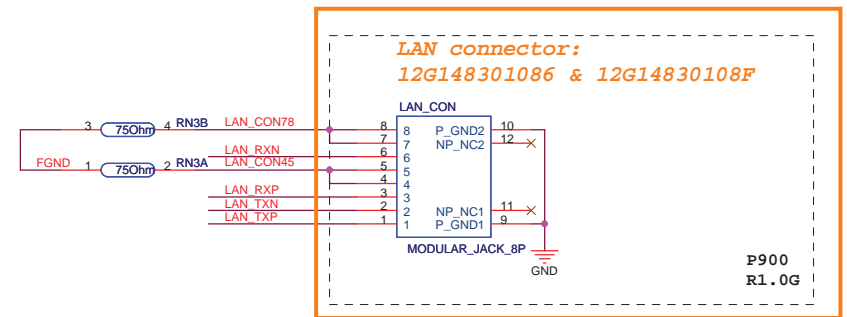
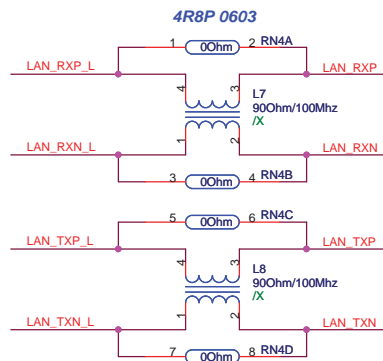
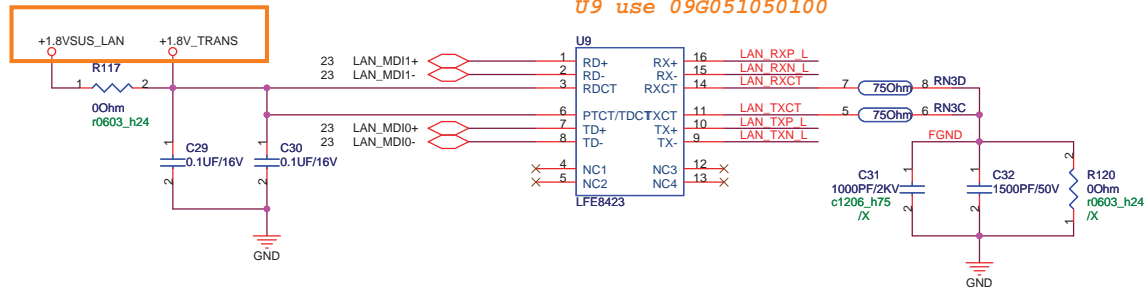
<Variant Name>

ASUS		Title : Minicard	
ASUSTek Computer INC.		Engineer: Brian_Liu	
Size	Project Name	90HD	
A3		Rev 1.2G	
Date: Friday, August 08, 2008		Sheet	22 of 47



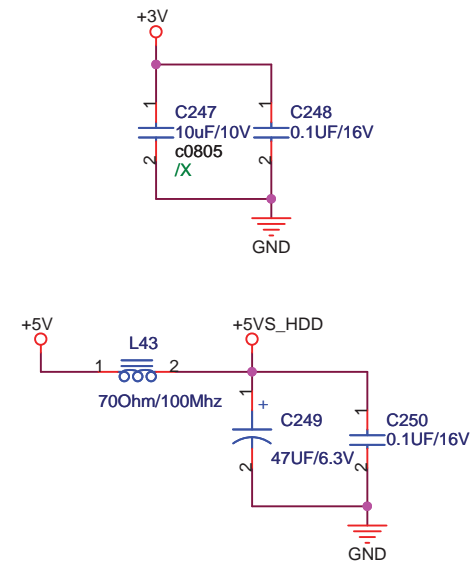
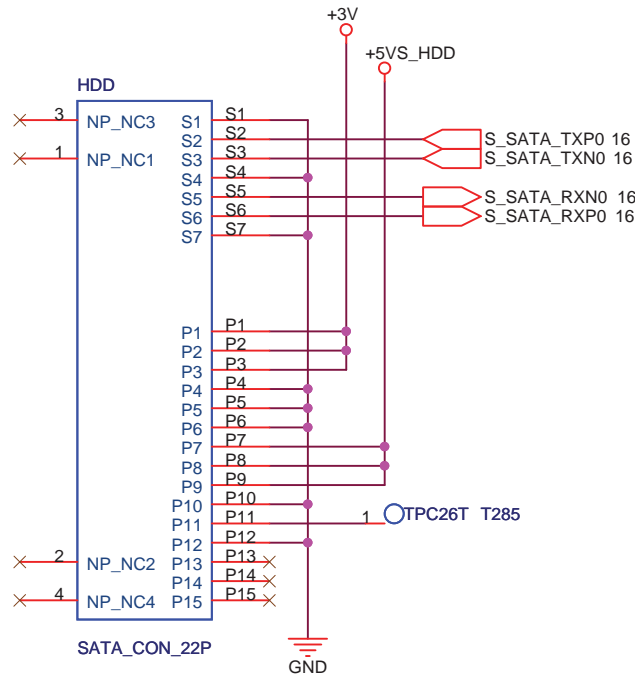
R1.1G

U9 use 09G051050100



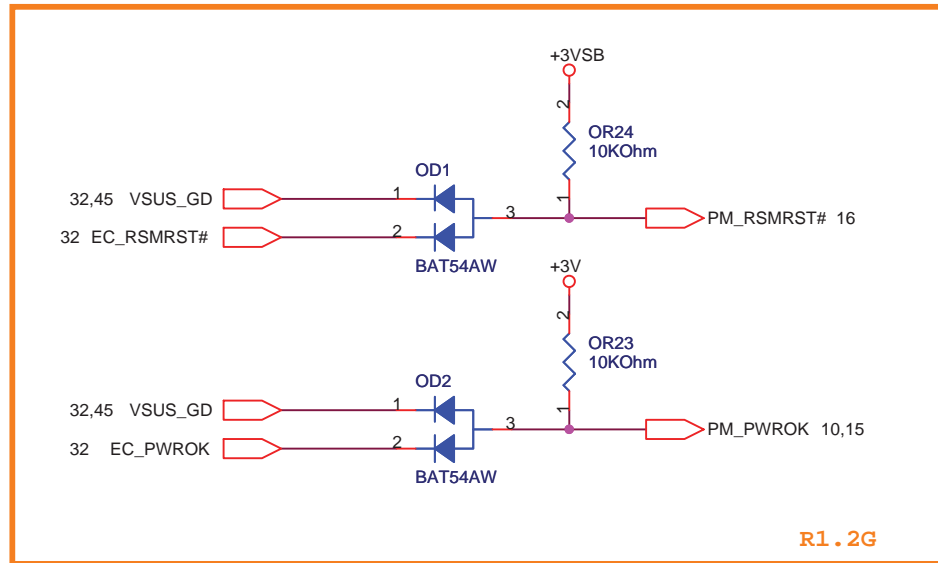
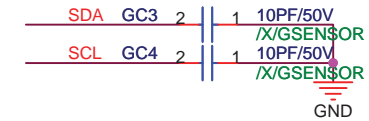
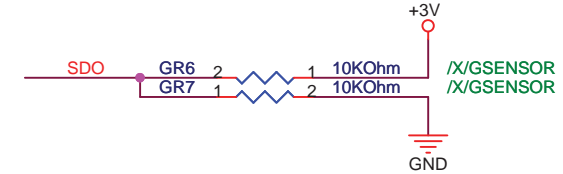
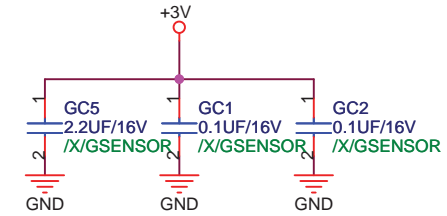
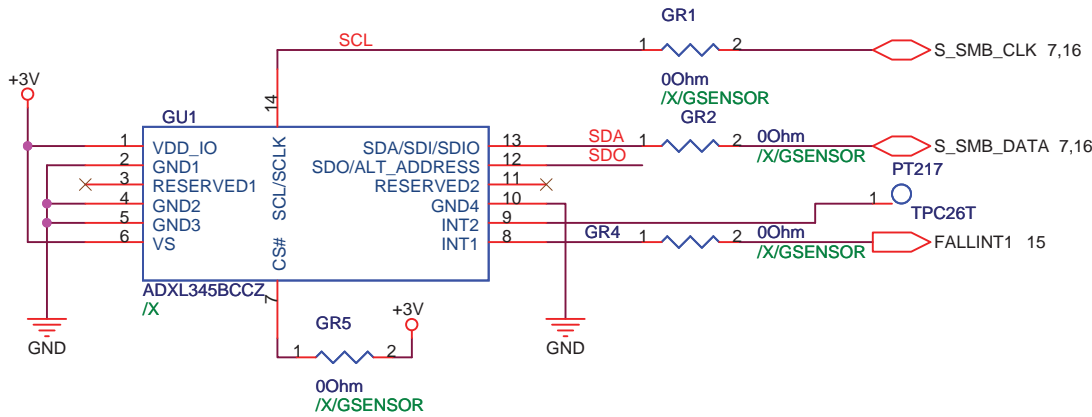
<Variant Name>

SATA HDD Connector



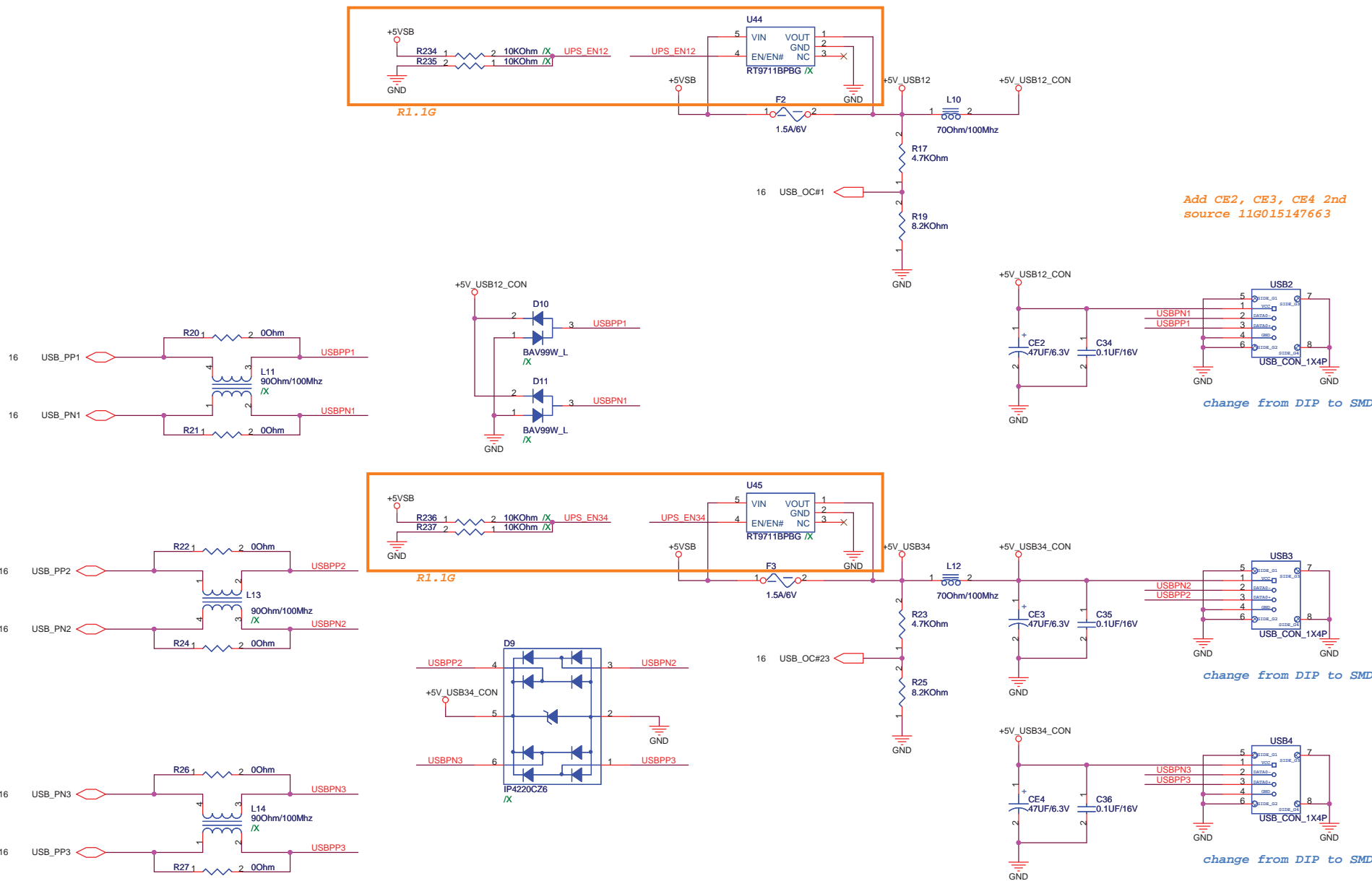
<Variant Name>

ASUS		Title : SATA HDD	
ASUSTek Computer INC.		Engineer: <i>Brian_Liu</i>	
Size A4	Project Name 900HD		Rev 1.2G
Date: Wednesday, August 06, 2008		Sheet	25 of 47



R1.2G

<Variant Name>



900HD R1.2G改Card Reader

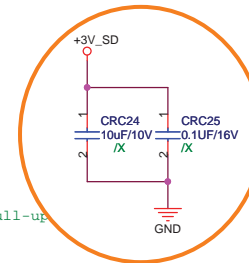
CLKSEL:
B52: Internal pull-down
C52: Internal pull-up

T86 TPC26T 1 CLK 48M READER

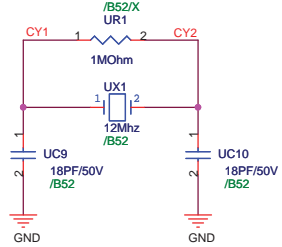
CLKSEL
0=12M
1=48M

UB SD CLK R
UB SD DATA0

Close to Chip

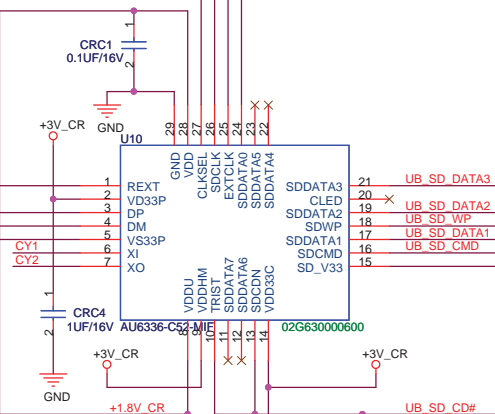


SDWP: Internal Pull-up
SDCDN: Internal Pull-up
SDWP = 1 Write protect
SDWP = 0 Write-able
SDCDN = 1 No card
SDCDN = 0 Card inserted



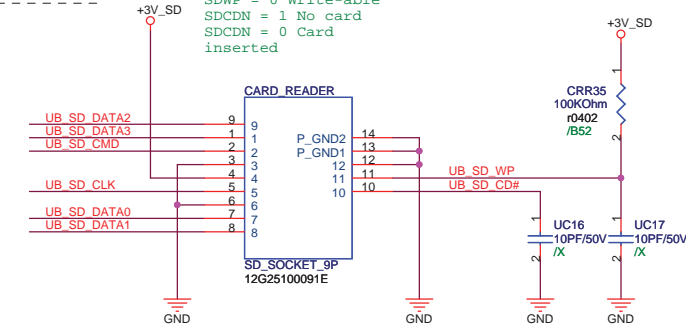
USB_PP4
USB_PN4

REXT CR

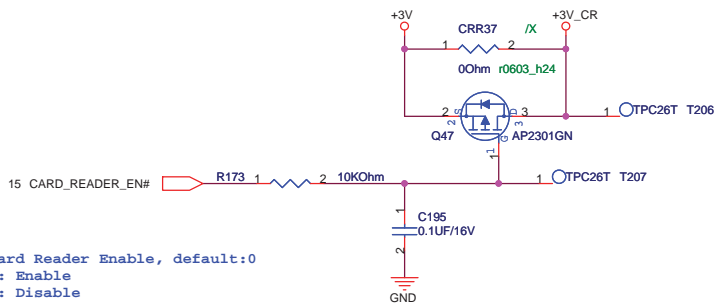


+3V_SD

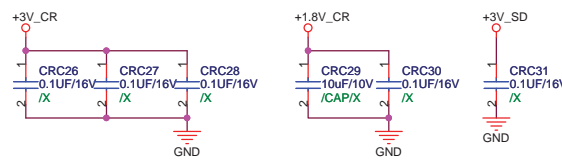
CRC15 close to CARD_READER

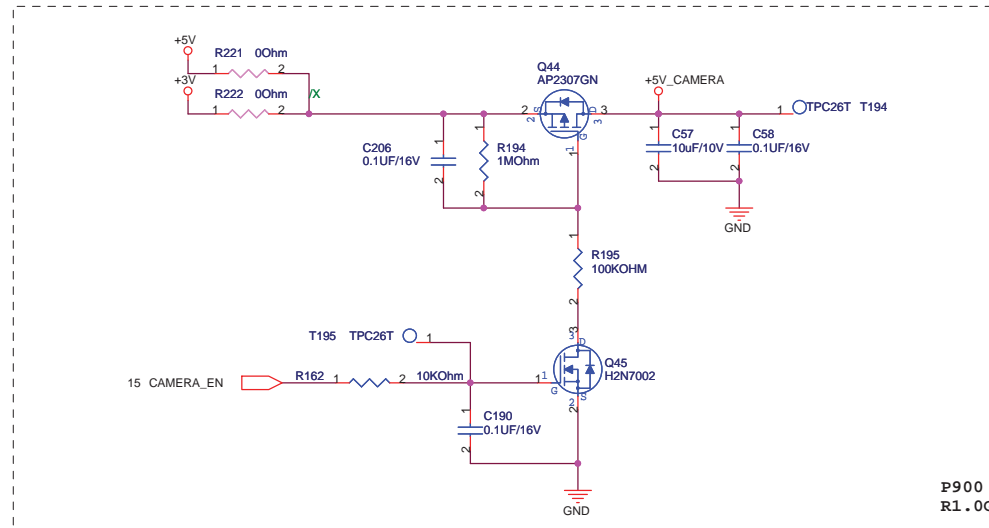
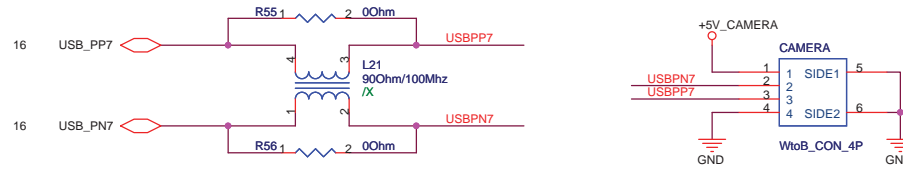


Card Insert: Pin.10 and Pin.12 are Shorted.
Card not Insert: Pin.10 and Pin.12 are Opened.
Write Protect: Pin.11 and Pin.12 are Opened.
Write Enable: Pin.11 and Pin.12 are Shorted.



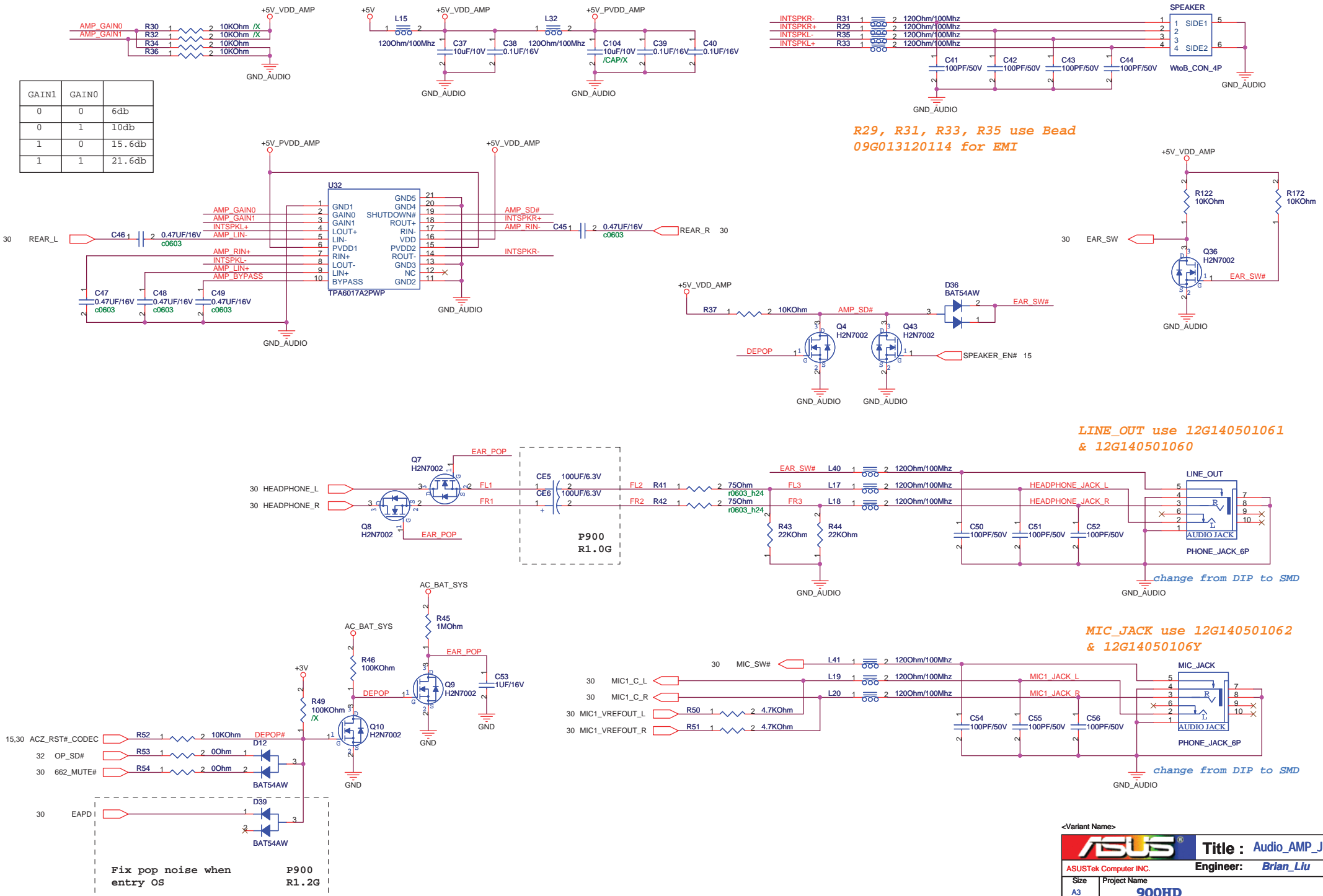
Card Reader Enable, default:0
0: Enable
1: Disable

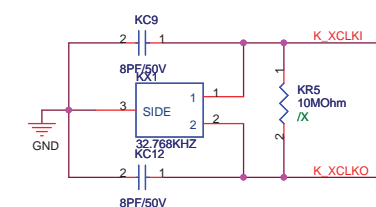
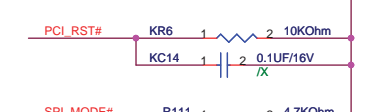
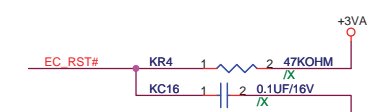
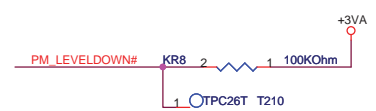
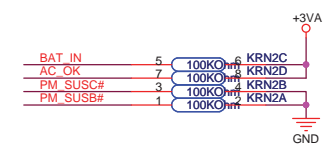
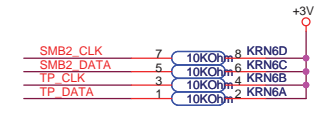
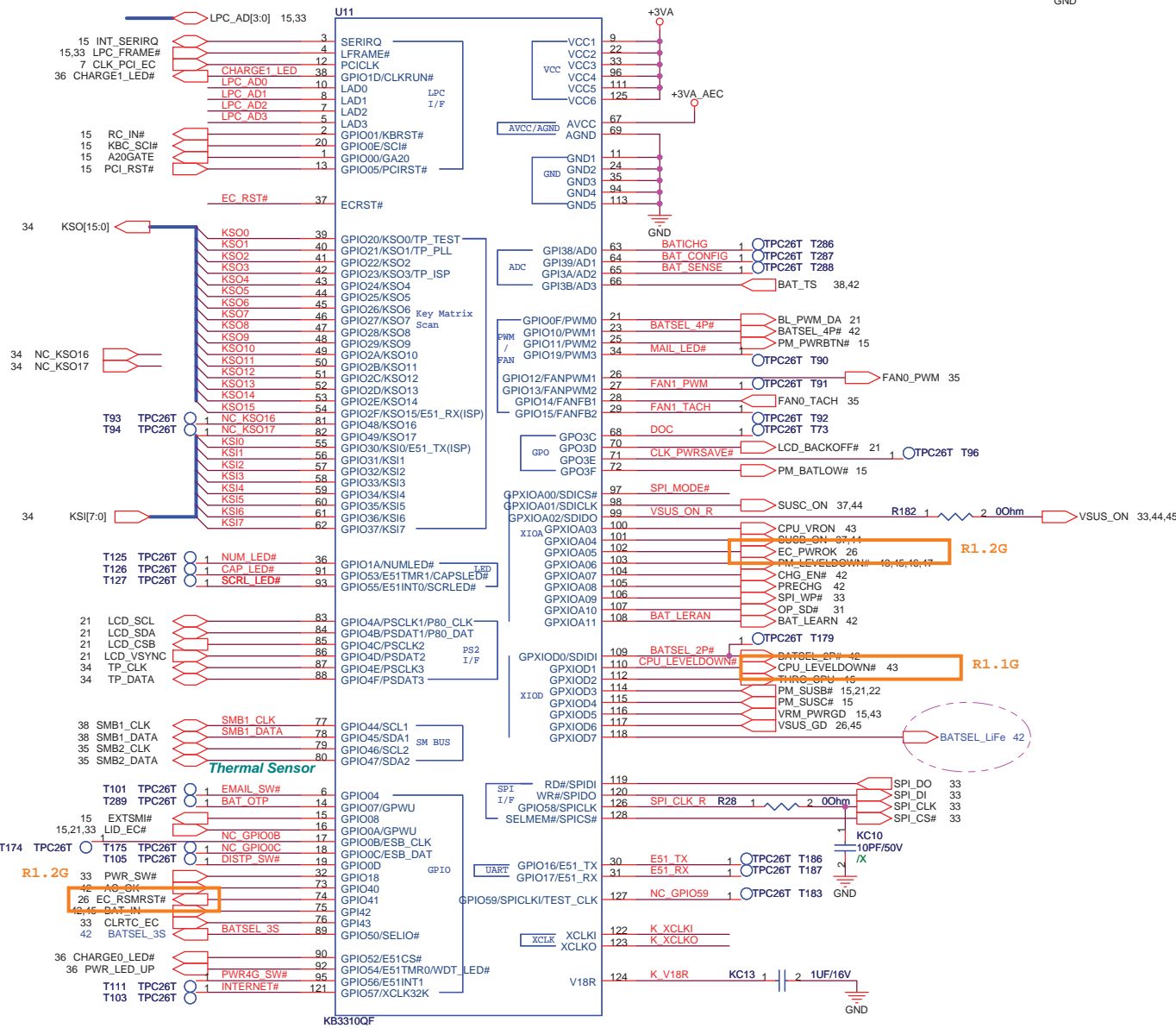




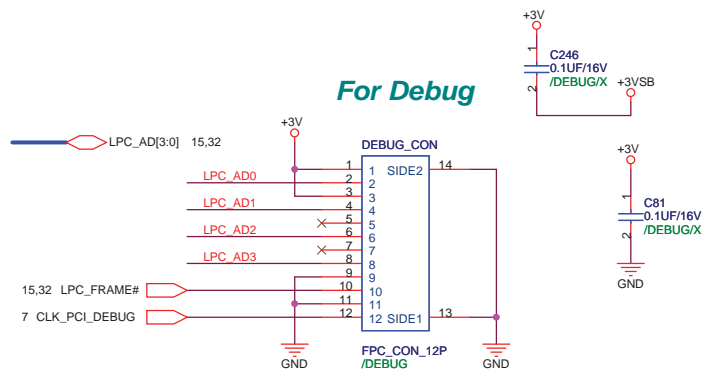
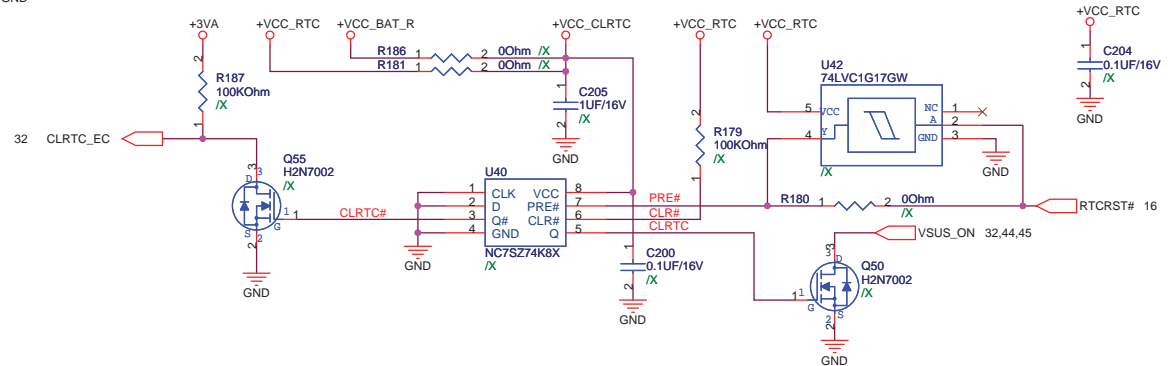
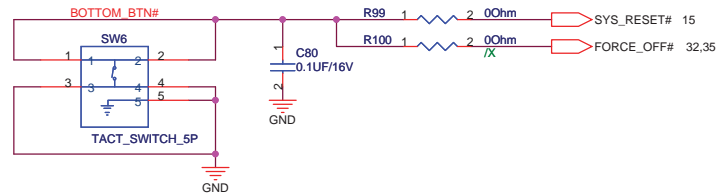
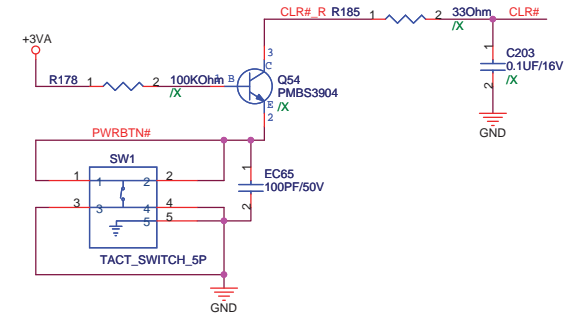
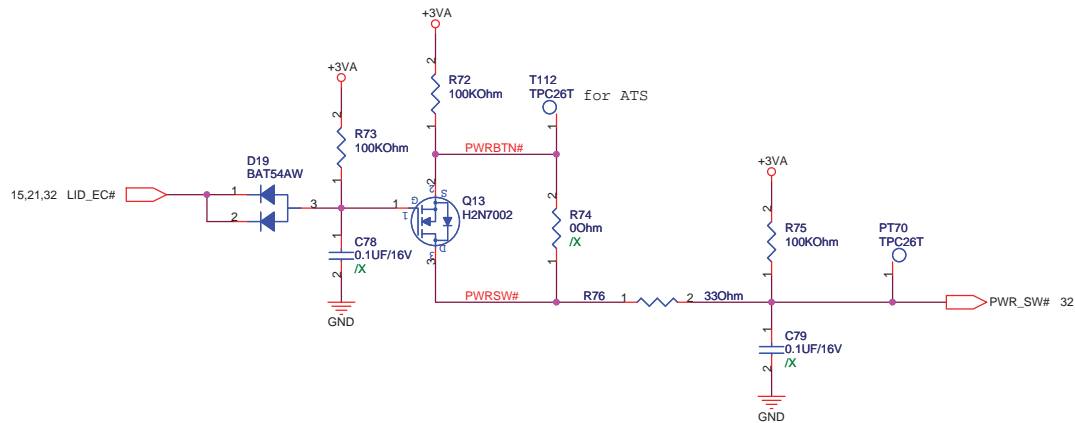
<Variant Name>

GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db

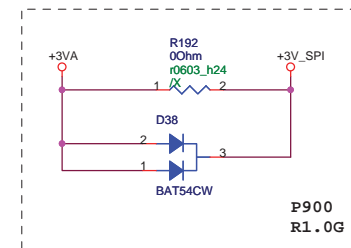
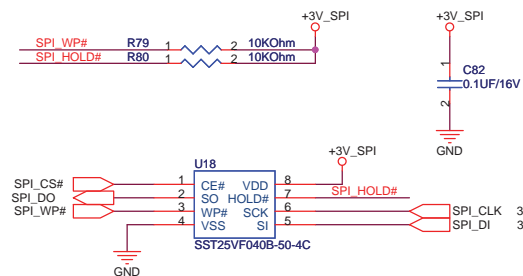




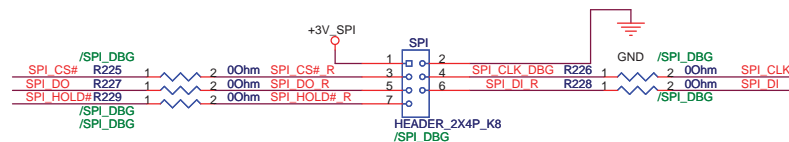
<Variant Name>



Debug Card cable use Z96 Touch Pad cable, P/N:
14G124110126, 14G124110120, 14G124110121
14G124110124, 14G124110125



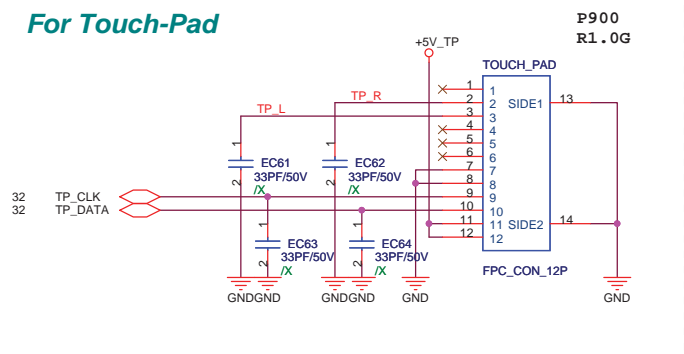
U18 use 05G001002900 & 05G00100F130 & 05G00100F131



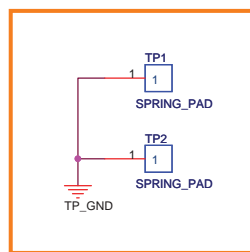
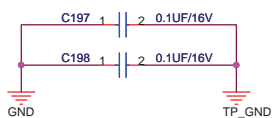
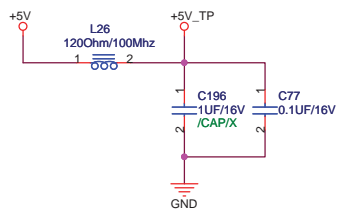
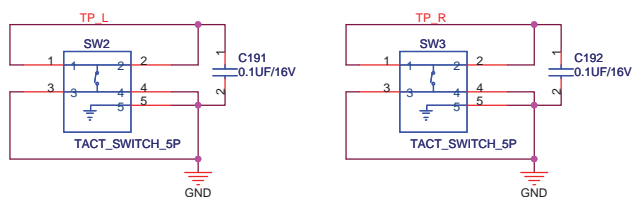
<Variant Name>		ASUS		Title : Switch_SPI ROM_Debug	
ASUSTek Computer INC.		Engineer: Brian_Liu			
Size	Project Name	900HD		Rev 1.2G	
A3					
Date: Wednesday, August 06, 2008		Sheet 33		of 47	

<http://hobi-elektronika.net>

For Touch-Pad

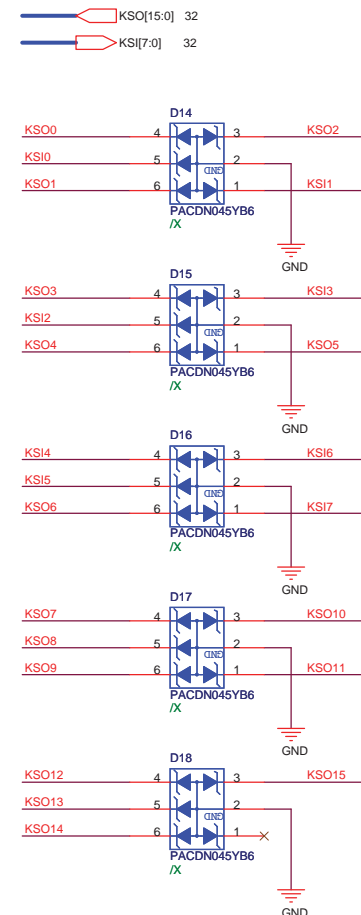
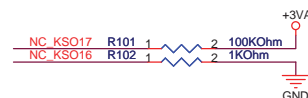
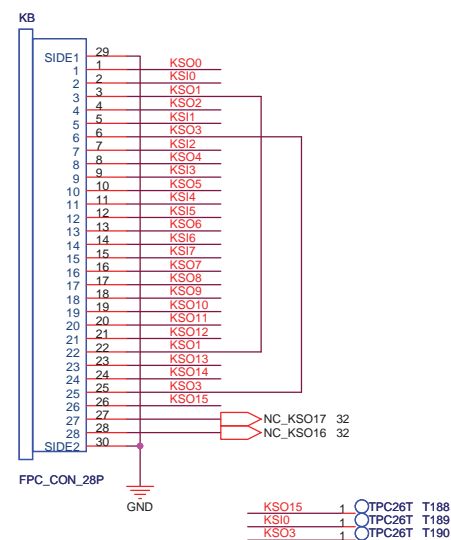


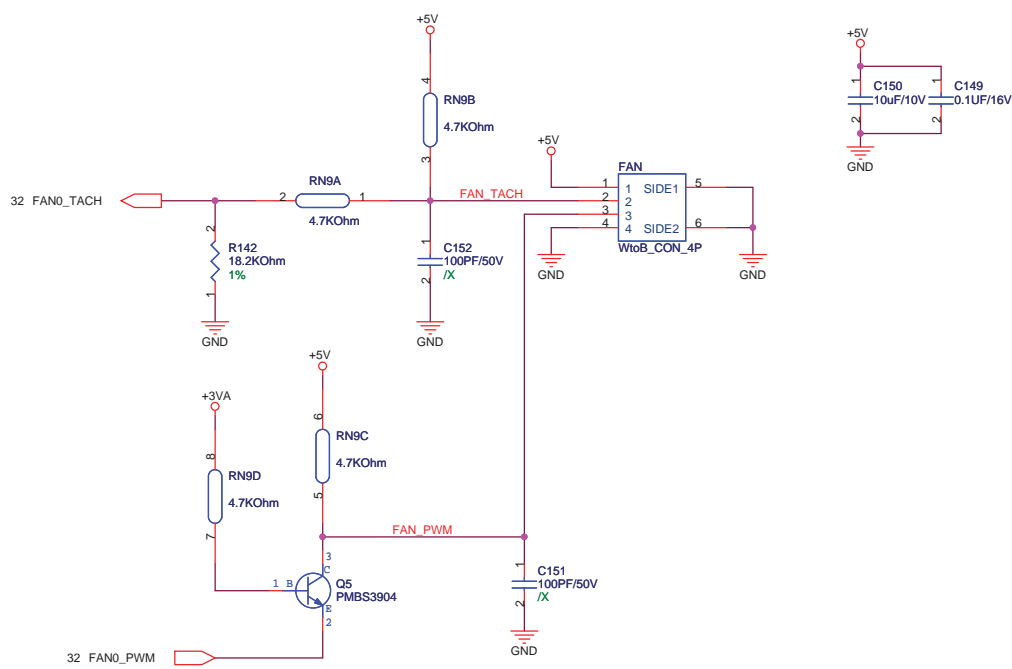
SW2, SW3 use 12G09103305N

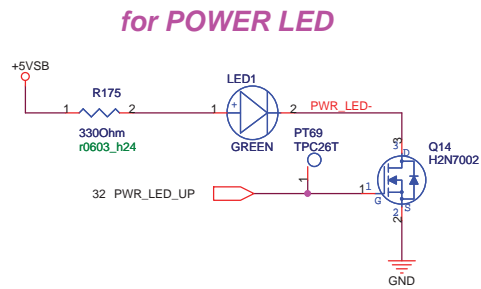


R1.2G
TP1, TP2 symbol modify to nb_emi_spring_156x108

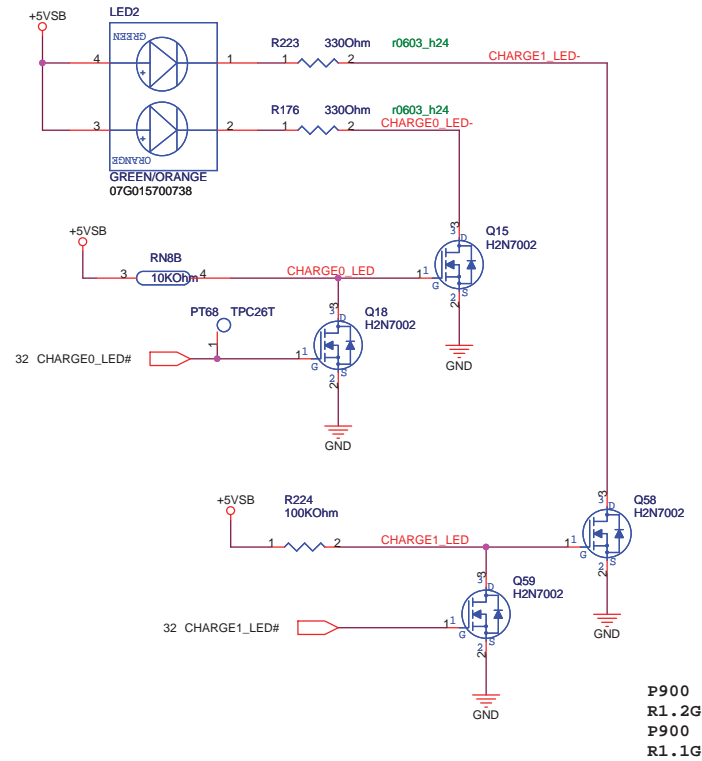
For Keyboard



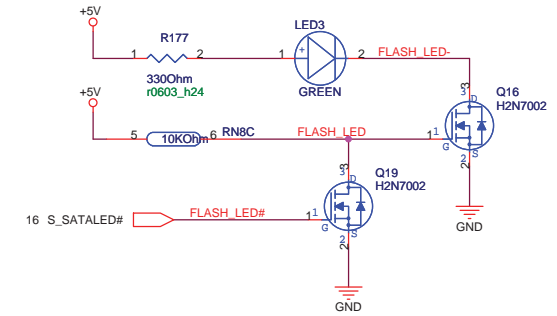




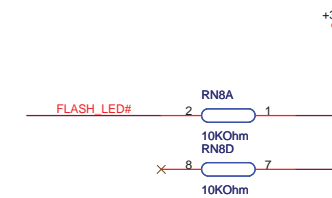
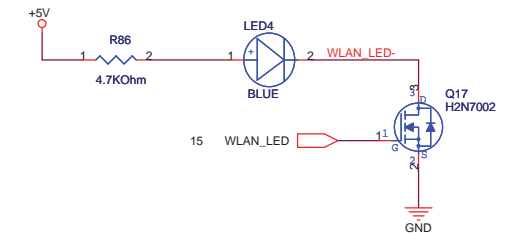
for CHARGE LED



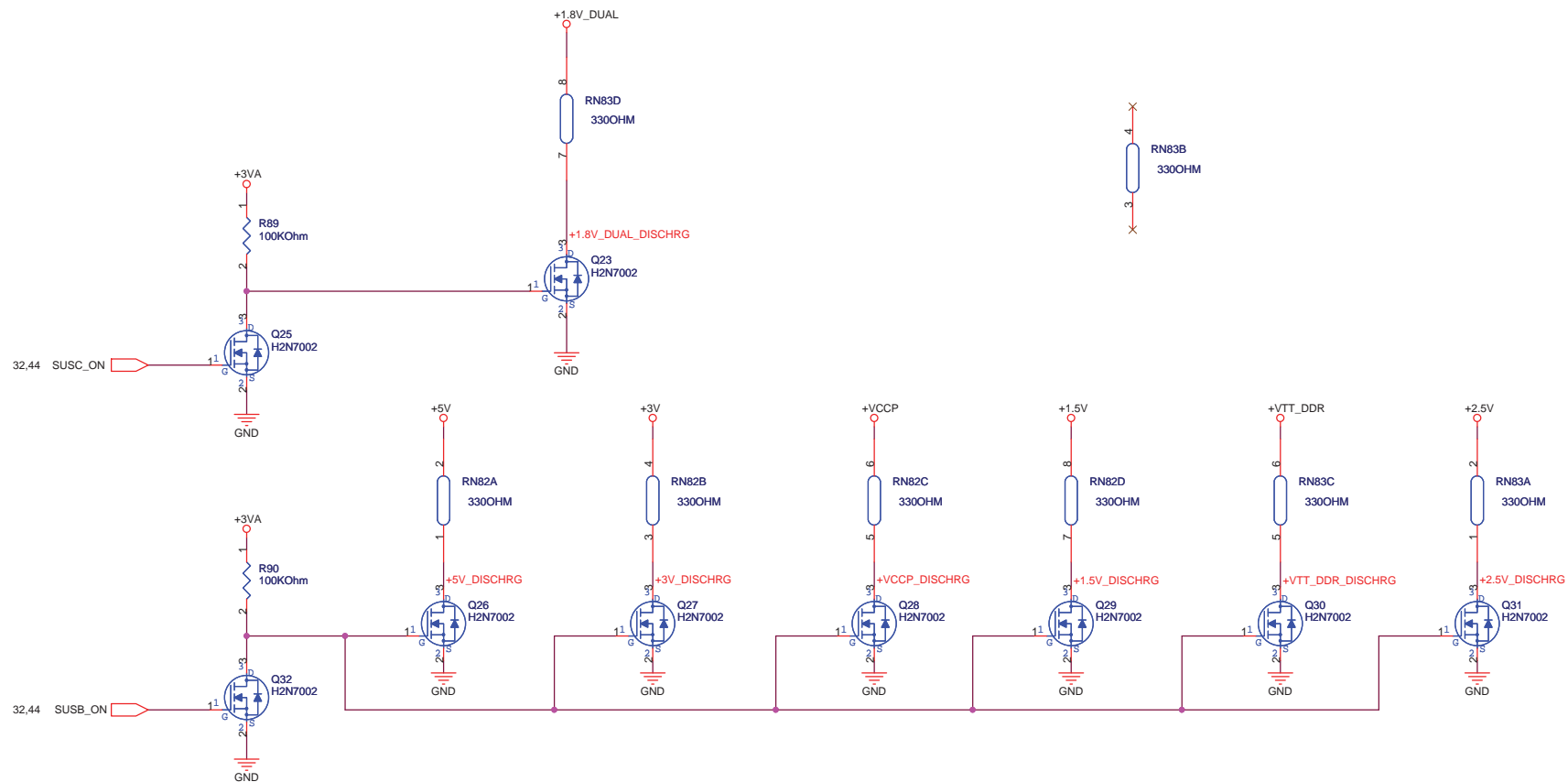
for SATA HDD LED



for WLAN LED



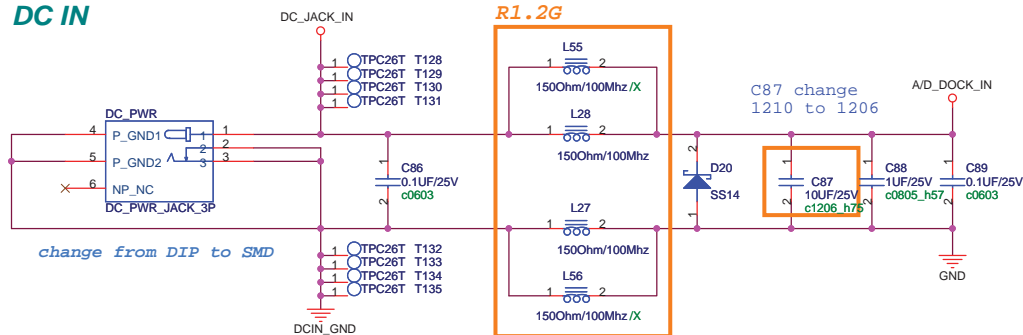
Delete THERMTRIP



<Variant Name>

ASUS		Title : Discharge	
ASUSTek Computer INC.		Engineer: Brian_Liu	
Size A3	Project Name 900HD		Rev 1.2G
Date: Wednesday, August 06, 2008		Sheet	37 of 47

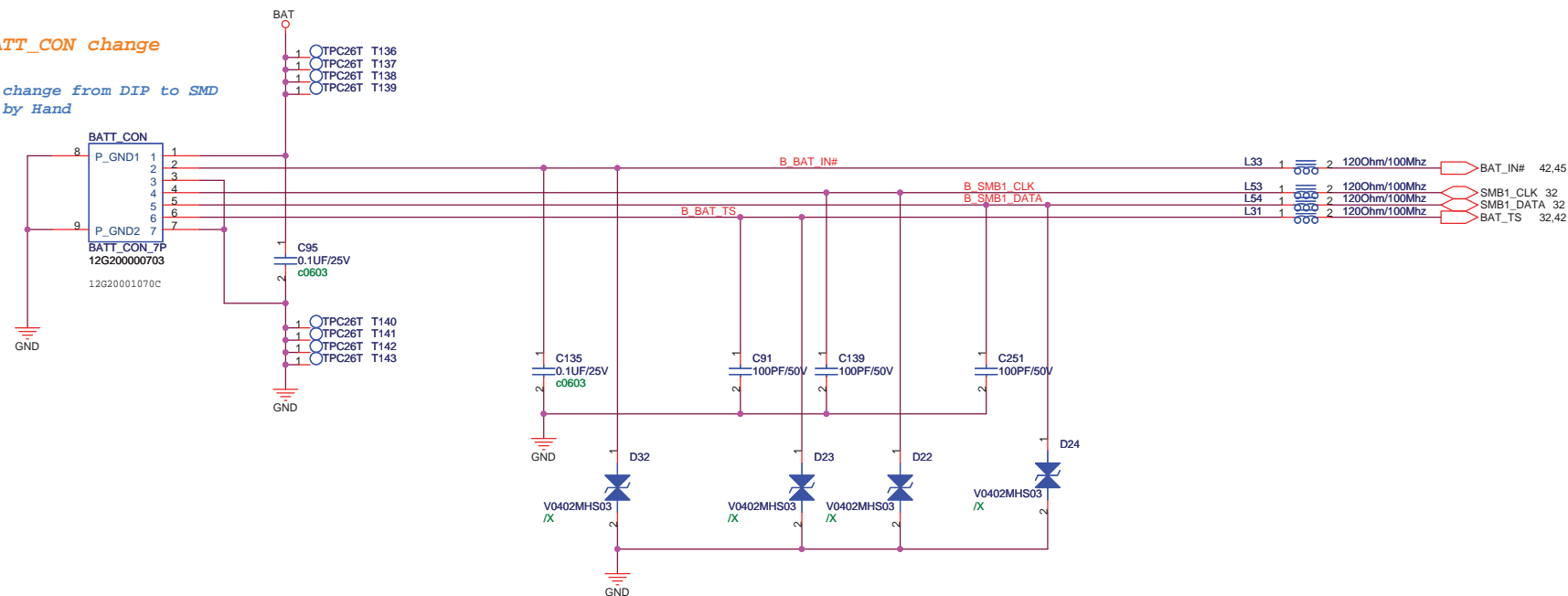
DC IN



BAT IN

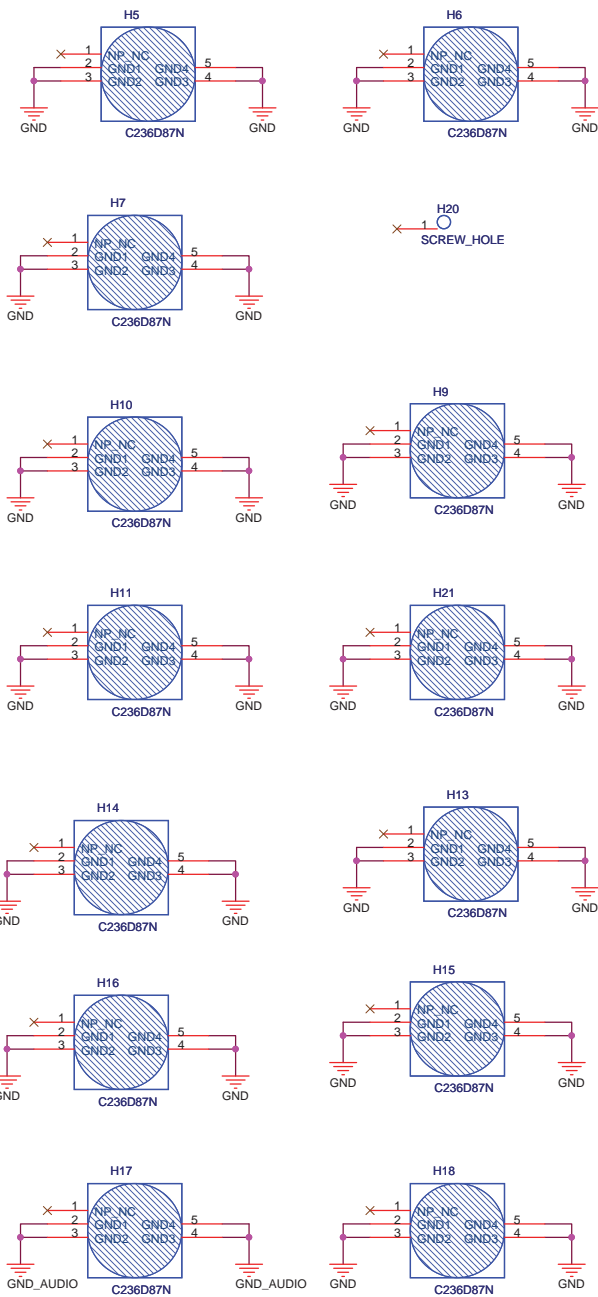
BATT_CON change

change from DIP to SMD
by Hand

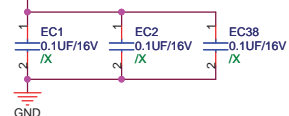


<Variant Name>

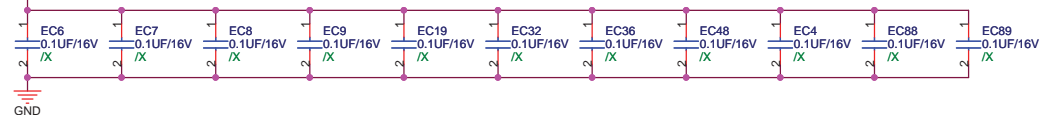
ASUS		Title : PWR Jack	
ASUSTek Computer INC.		Engineer: Brian_Liu	
Size	Project Name	Rev	
A3	900HD	1.2G	
Date: Wednesday, August 06, 2008		Sheet	38 of 47



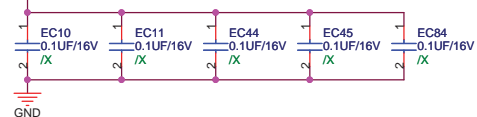
AC_BAT_SYS



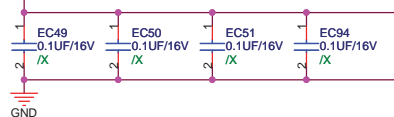
+3V



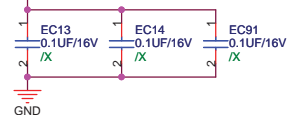
+5VSB



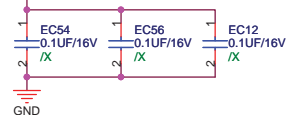
+3V



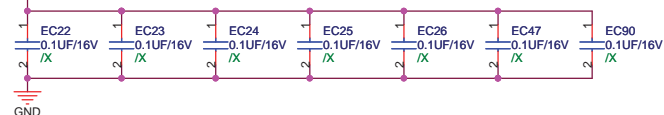
+1.5V



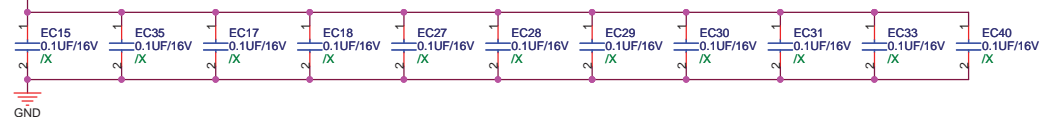
+5V



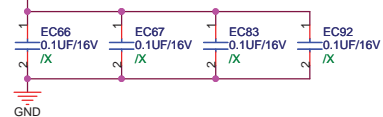
+1.8V_DUAL



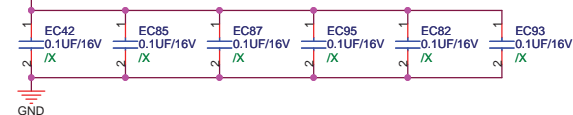
+3VSB



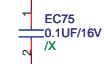
+3VSB



+VCCP



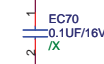
+VCCP



+VCCP



+VCCP



+VCCP



+VCCP



+VCCP



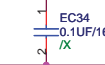
+3V



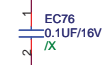
+3V



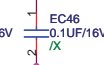
+3V



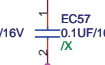
+3V



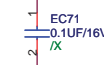
+3V



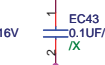
+3V



+3V



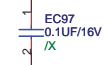
+3V



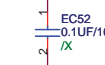
+5V



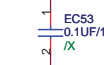
+5VSB



+1.8V_DUAL



+1.8V_DUAL



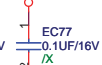
AC_BAT_SYS



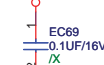
AC_BAT_SYS



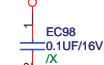
AC_BAT_SYS



AC_BAT_SYS

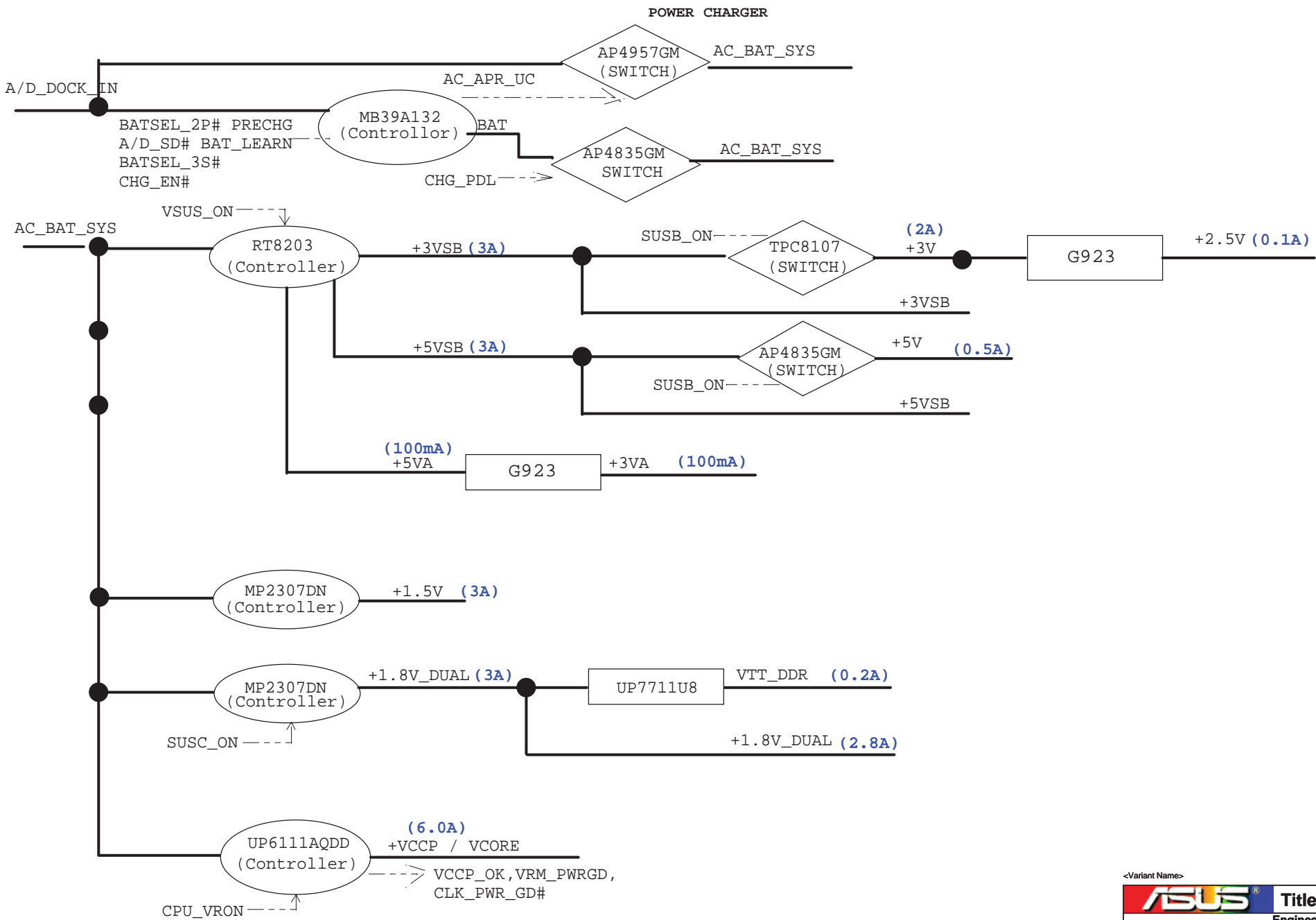


AC_BAT_SYS

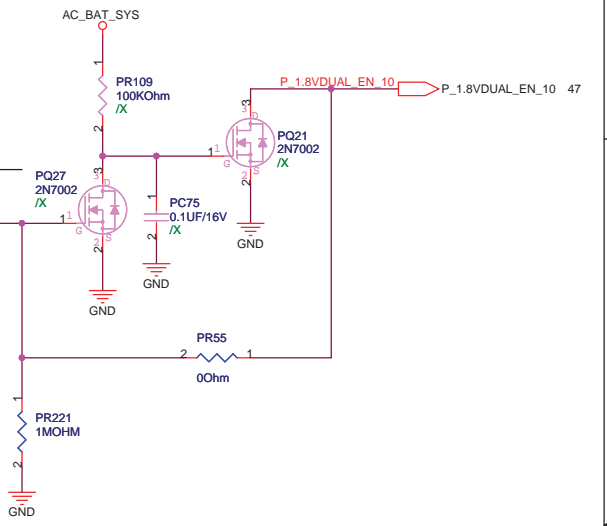
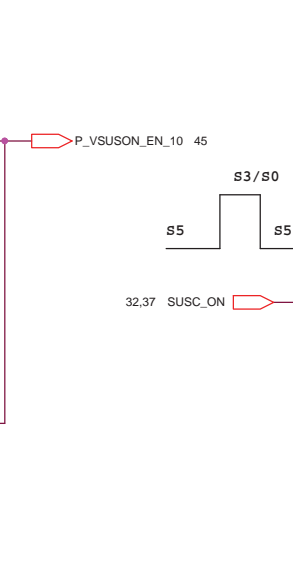
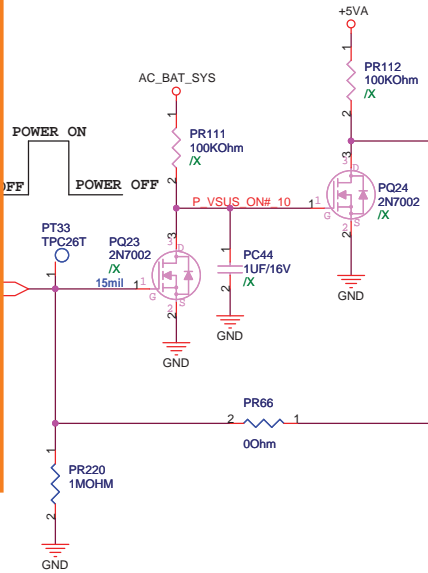
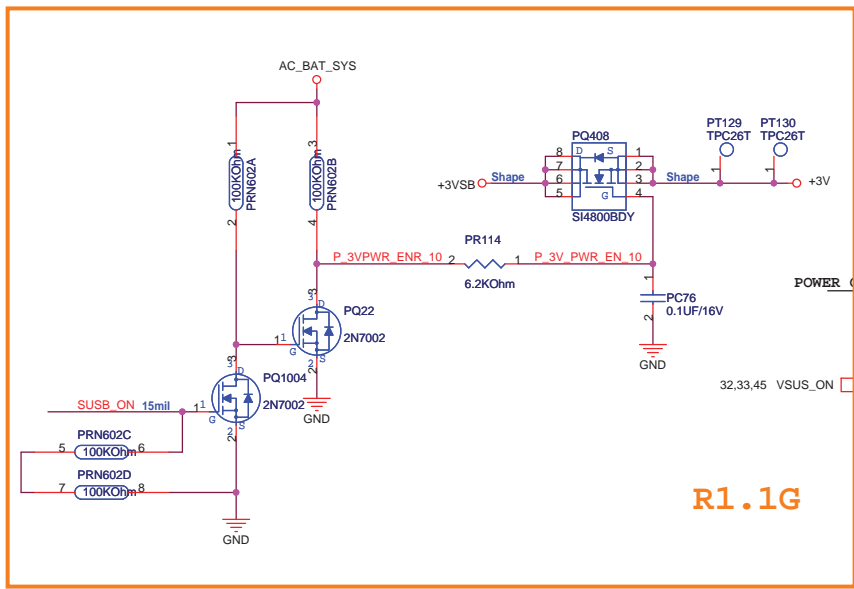


<Variant Name>

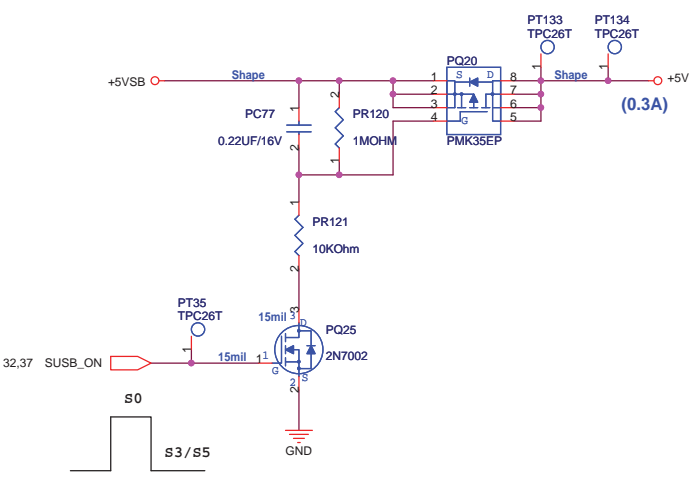
ASUS		Title : EMI	
ASUSTek Computer INC.		Engineer: Brian_Liu	
Size A3	Project Name 900HD		Rev 1.2G
Date: Wednesday, August 06, 2008		Sheet 40 of 47	



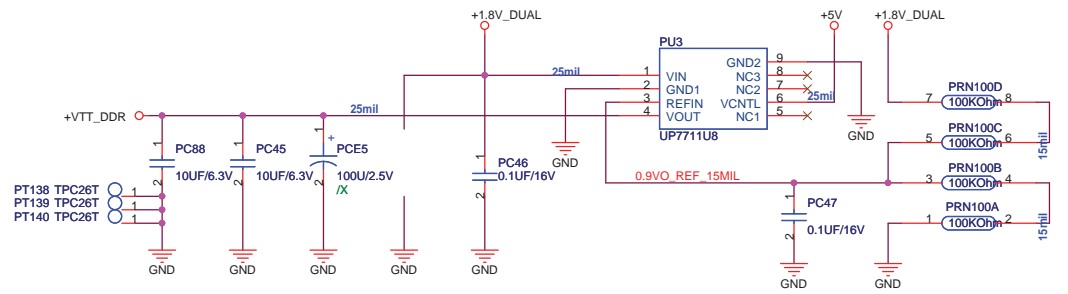




PC77更換-->0.22uF/16V



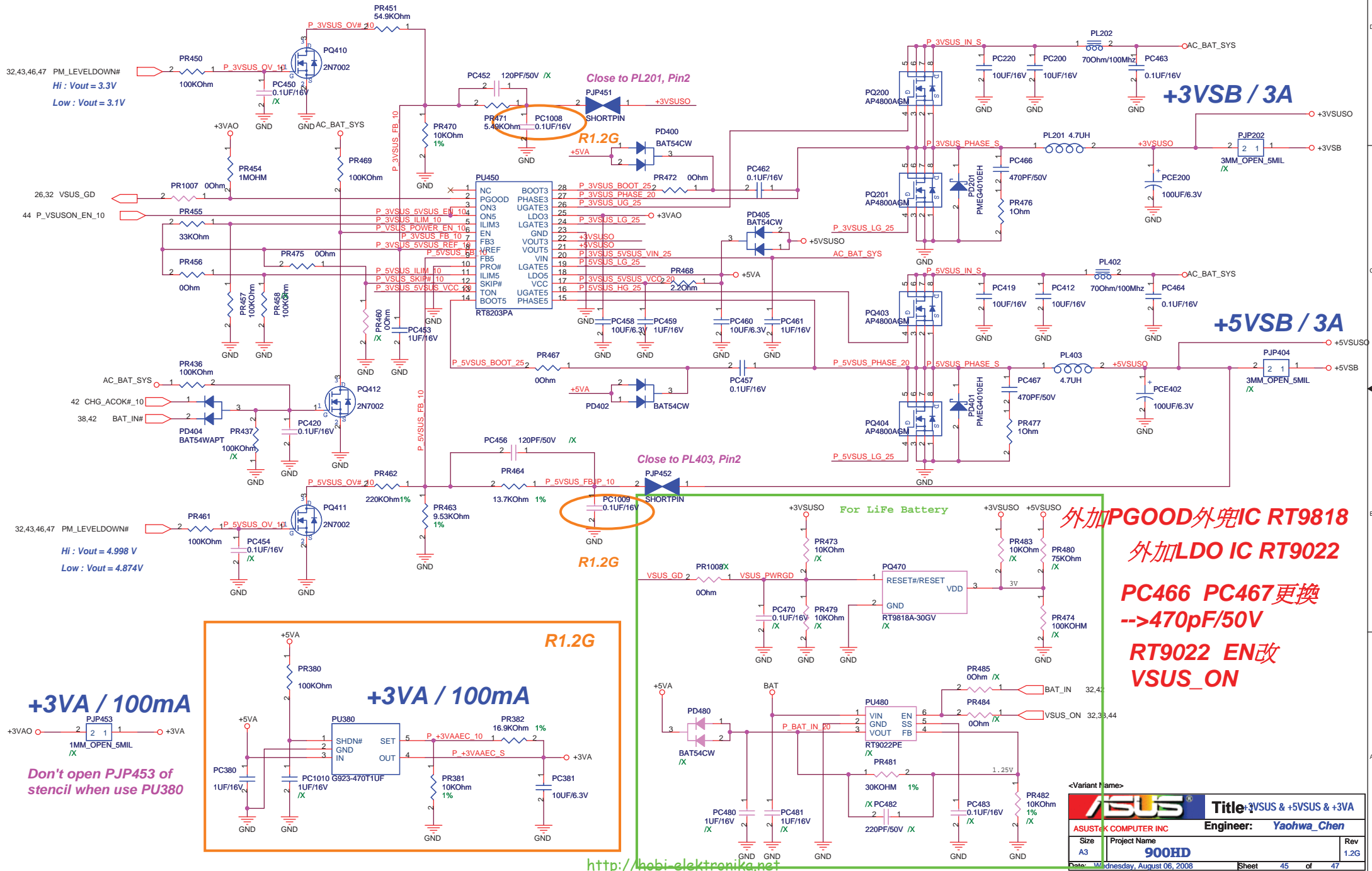
VTT_DDR (0.2A)



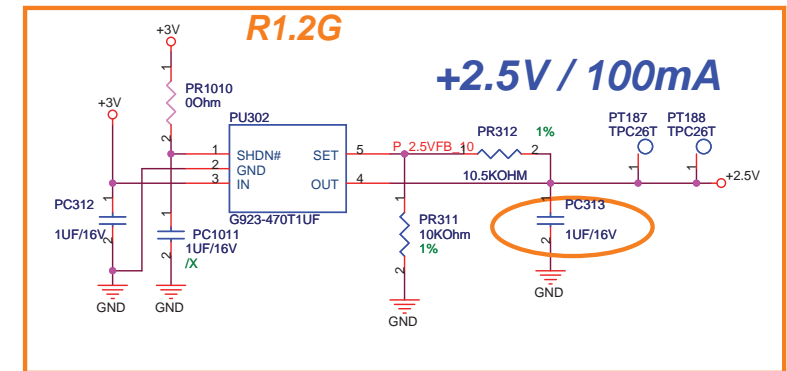
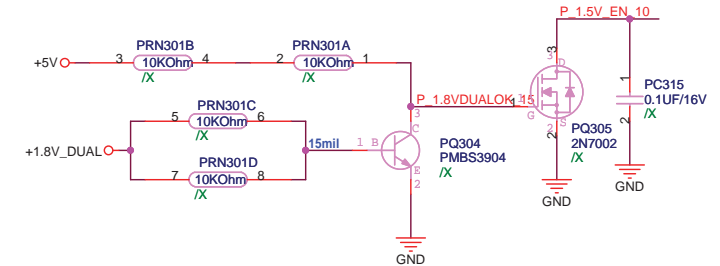
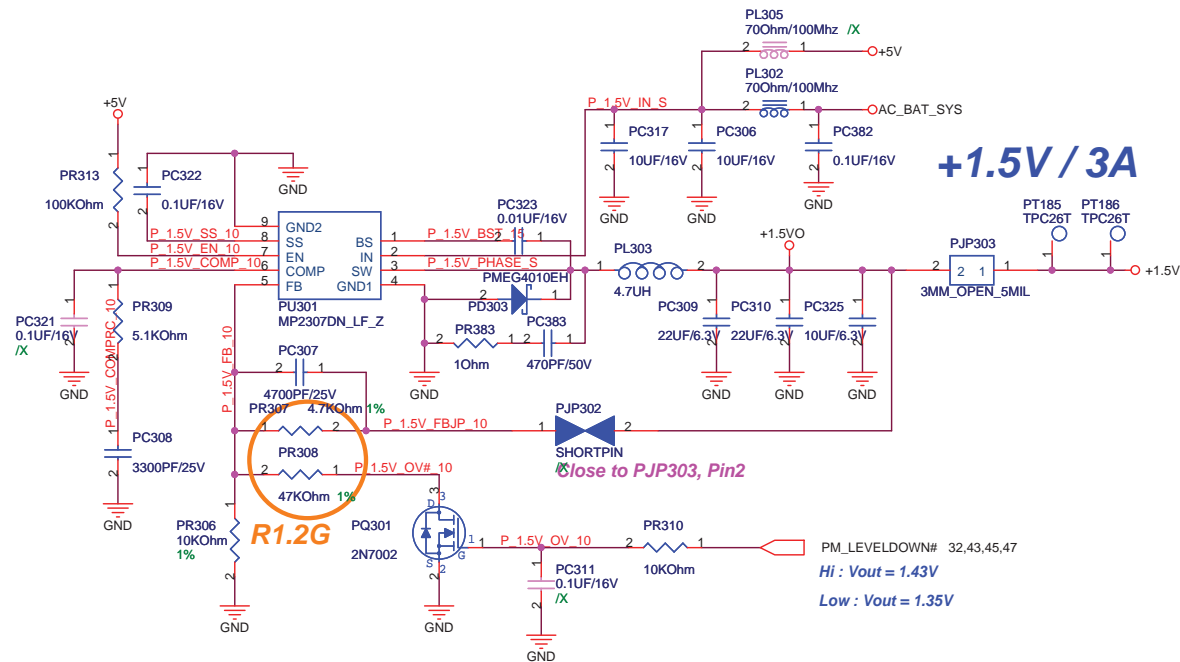
PR464: 13.7K Ohm
PR463: 9.53K Ohm
PR462: 220K Ohm
Hi: Vout = 4.998 V
Low: Vout = 4.874 V

PR464: 13.7K Ohm
PR463: 9.53K Ohm
PR462: 215K Ohm
Hi: Vout = 5.002 V
Low: Vout = 4.874 V

PR464: 13.7K Ohm
PR463: 9.53K Ohm
PR462: 210K Ohm
Hi: Vout = 5.004 V
Low: Vout = 4.874 V



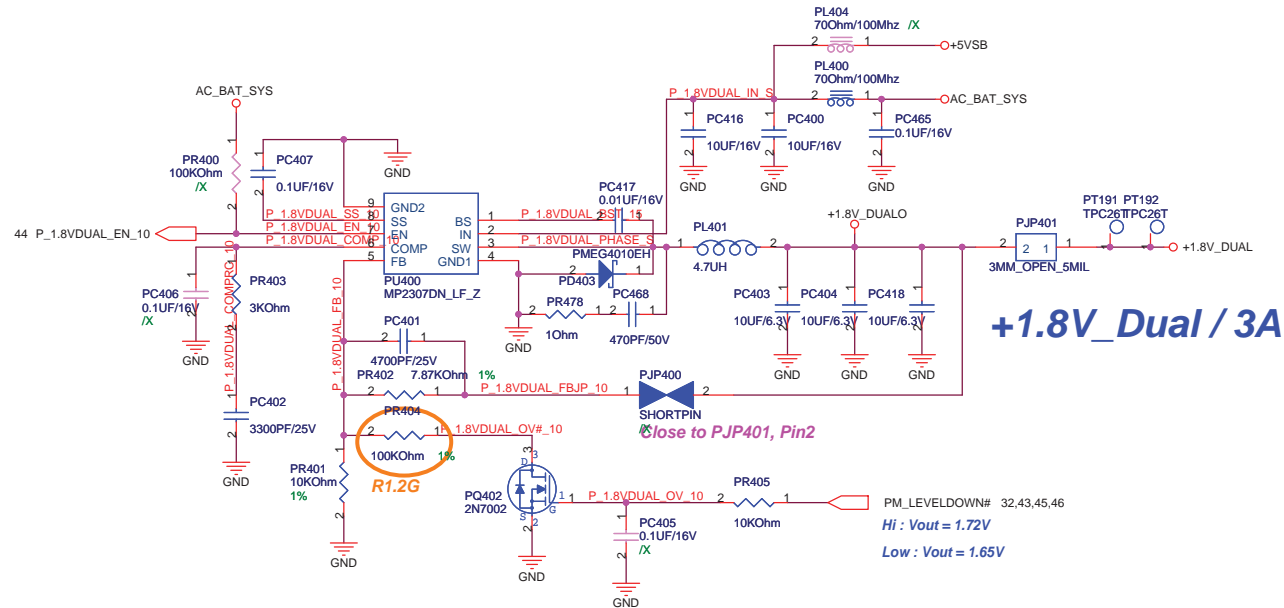
PC383更換-->470pF/50V



<Variant Name>

ASUS		Title : 1.05V_1.5V_2.5V	
ASUSTek Computer INC.		Engineer: Yaohwa Chen	
Size B	Project Name	900HD	Rev 1.2G
Date: Wednesday, August 06, 2008	Sheet 46	of 47	

補償値更換PC401-->4.7nF
PC468更換-->470pF/50V



<Variant Name>

ASUS		Title : 1.8V_DUAL_5VSB	
ASUSTek Computer INC.		Engineer: Yaohwa Chen	
Size	Project Name		Rev
A3	900HD		1.2G
Date: Wednesday, August 06, 2008		Sheet	47 of 47