Austin 13" Schematics Document

Ivy Bridge ULV
Panther Point

2013-02-26
REV : A00

DY : None Installed

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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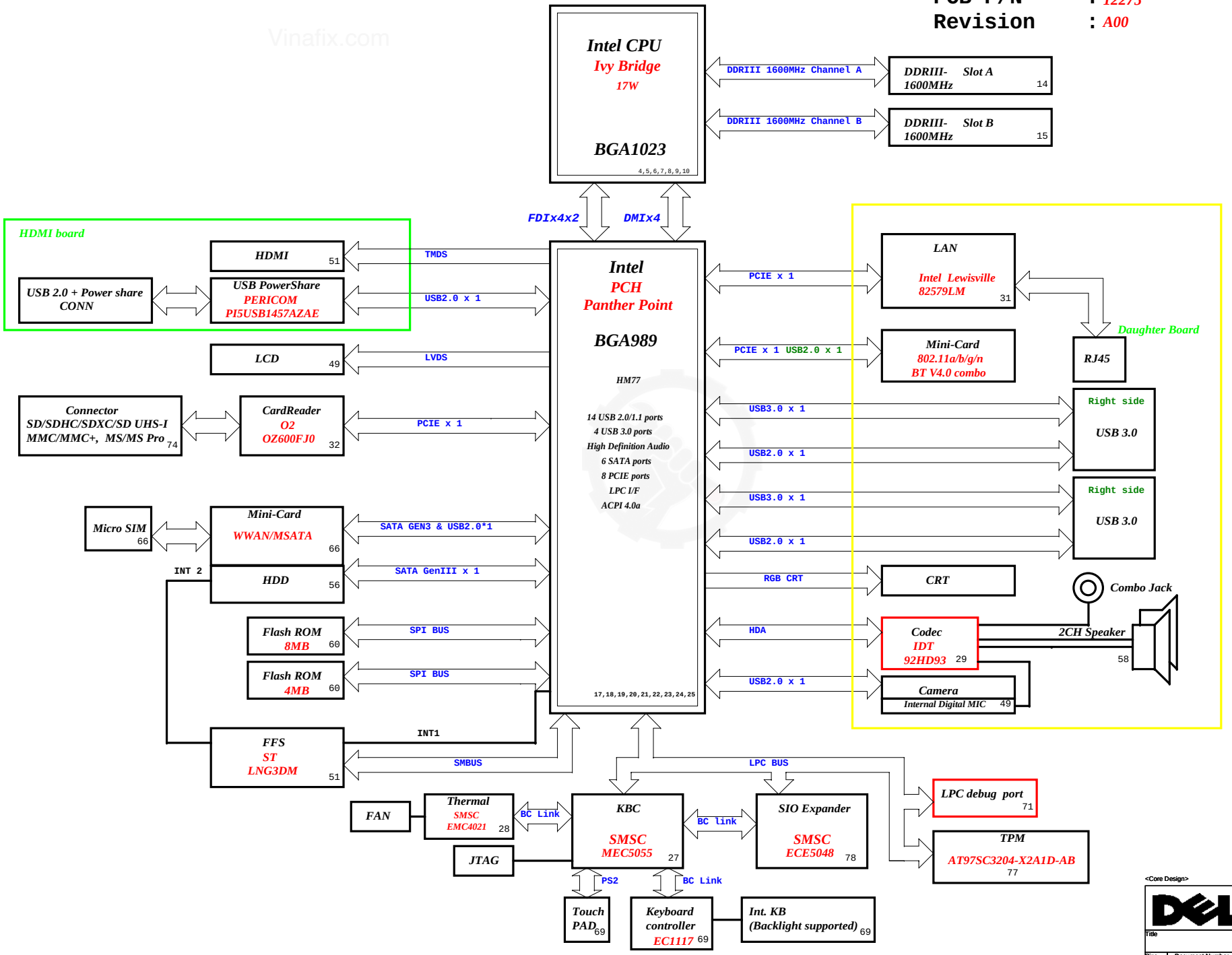
Austin 13 Block Diagram

Project Code : 91.4LA01.001
PCB P/N : 12275
Revision : A00



CHARGER ISL88731CHRTZ 40	
INPUTS	OUTPUTS
AD+	BT+

SYSTEM DC/DC TPS51125RGER 41	
INPUTS	OUTPUTS
DCBATOUT	5V_PWR_2 +3.3V_ALW2 +5V_ALW +3.3V_ALW +15V_ALW

CPU DC/DC VT1318+VT1323 42,43	
INPUTS	OUTPUTS
+5V_ALW	VCC_CORE

GFX DC/DC VT1318+VT1323 44	
INPUTS	OUTPUTS
+5V_ALW	VCC_GFXCORE

SYSTEM DC/DC VT386+RT8085	
INPUTS	OUTPUTS
+5V_ALW	+1.05V_RUN_VTT
+3.3V_ALW	+1.05V_M 45

SYSTEM DC/DC RT8207	
INPUTS	OUTPUTS
DCBATOUT	+1.35V_MEM +0.675_DDR_VTT +V_DDR_REF 46

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

SYSTEM DC/DC APL5930 47	
INPUTS	OUTPUTS
+3.3V_ALW	+1.5V_RUN

SYSTEM DC/DC SY8037 48	
INPUTS	OUTPUTS
+5V_ALW	+VCC_SA

INPUTS N.A	OUTPUTS

Switches	
INPUTS	OUTPUTS
+1.35V_MEM +5V_ALW +3.3V_ALW +1.05V_N +3.3V_ALW +3.3V_ALW +5V_ALW	+1.35V_CPU_VDDQ +5V_RUN +3.3V_RUN +1.05V_RUN +3.3V_M +3.3V_ALW_PCH +5V_ALW_PCH

PCB LAYER

L1:Top	L5:GND
L2:GND	L6:Bottom
L3:Signal	
L4:Signal	

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PCH Strapping

Name	Schematics Notes
SPKR	The signal has a weak internal pull-down. If the signal is sampled high, this indicates that the system is strapped to the "No Reboot" mode (Panther Point will disable the TCO Timer system reboot feature).
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
INTVRMEN	Integrated 1 V VRMs is enabled when high, External when low.
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
DF_TVS	DF_TVS needs to be pulled up to VccDFTERM power rail through 2.2 kOhms ±5% resistor.
HAD_DOCK_EN# /GPIO[33]	This signal controls the external Intel HD Audio docking isolation logic. This is an active-low-signal. When deasserted the external docking switch is in isolate mode. When asserted the external docking switch electrically connects the Intel HD Audio dock signals to the corresponding Panther Point signals. This signal can instead be used as GPIO33.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0) Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality

Sandy & Ivy Bridge Compatibility

Pin Name	Configuration	Schematic Notes
DDR3 VREF	**Sandy Bridge + Ivy Bridge**	DDR3 VREF, M1 and M3 function are required.
	Ivy Bridge	No change.
PROC_SELECT# & DF_TVS	**Sandy Bridge + Ivy Bridge**	Connect DF_TVS signal of the PCH to PROC_SELECT# of the processor through a 1K±5% series resistor. PROC_SELECT# also needs a 2.2K±5% pull up resistor to PCH VccDFTERM rail.
	Ivy Bridge	No change.
VCCIO_SEL	**Sandy Bridge + Ivy Bridge**	The POR for Ivy Bridge mobile parts is now 1.05 V. There is no longer a need for a separate VR for the processor at 1.0 V and the PCH at 1.05 V. A single VR may be shared for both.
	Ivy Bridge	No change.
VCCSA_VID[0:1]	**Sandy Bridge + Ivy Bridge**	VCCSA[0:1] are the select pin of VCCSA's power control.
	Ivy Bridge	No change.

Power Plane

Power Plane	Voltage	Actice Status	Description
+5V_RUN +3.3V_RUN +1.8V_RUN +1.5V_RUN +1.05V_RUN_VTT +1.05V_M +VCC_SA +VCC_CORE +VCC_GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 1.05V 0.75V~0.9V 0.3V to 1.3V 0 to 1.25V	S0	CPU Core Rail Graphics Core Rail
+1.35V_MEM +0.675V_DDR_VTT	1.5V 0.75V	S3	
BT+ DCBATOUT +15V_ALW +5V_ALW +3.3V_ALW	6V~14.1V 6V~14.1V 15V 5V 3.3V	All S states	AC Brick Mode only
+3.3V_LAN	3.3V	WOL_EN	Legacy WOL
+3.3V_ALW2	3.3V	DSW, Sx	ON for supporting Deep Sleep states
RTC_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

Processor Strapping

Chief River Schematic Checklist Rev.0_72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value	POP Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**1**	**1**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	**11:** 1x16 PCI Express **10:** 2 x8 - PCI Express **01:** Reserved **00:** 1x8, 2x4 PCI Express	**11**	**11**

USB Table

Pair	Device
0	**USB0(Left side-HDMI/B)**
1	**USB1(Right side-IO/B, for USB3.0)**
2	**USB2(Right side-IO/B, for USB3.0)**
3	**NC**
4	**WLAN**
5	**WWAN**
6	**NC**
7	**NC**
8	**NC**
9	**NC**
10	**NC**
11	**NC**
12	**CAMERA**
13	**NC**

PCIE Table

PCIE	
Lane	Device
1	**NC**
2	**WLAN**
3	**NC**
4	**NC**
5	**NC**
6	**Card Reader**
7	**Onboard LAN**
8	**NC**

SATA Table

SATA	
Pair	Device
0	**HDD1**
1	**mSATA**
2	**NC**
3	**NC**
4	**NC**
5	**NC**

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Title: *Table of Content*

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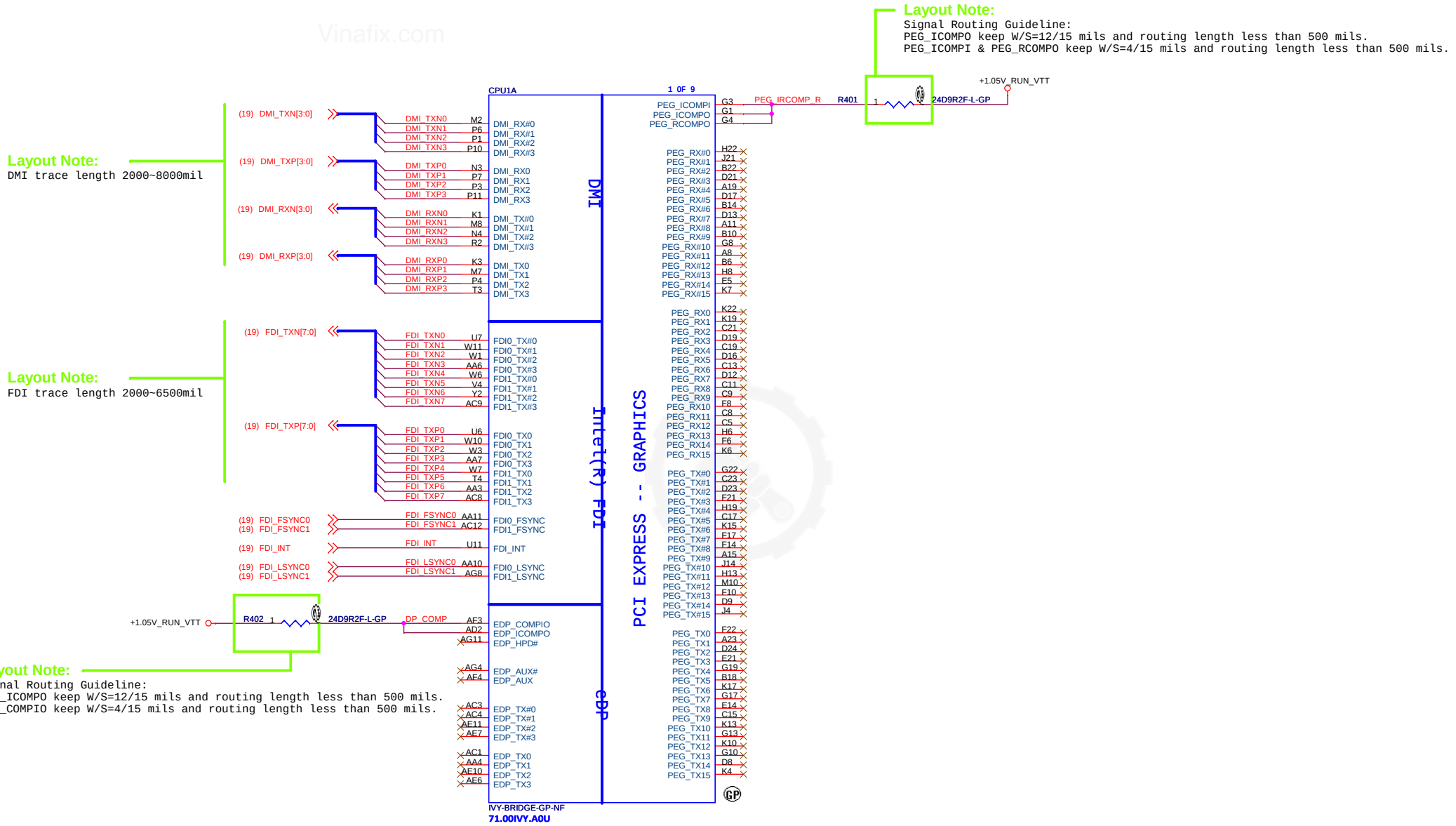
SSID = CPU



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Title: CPU(PCIE/DMI/FDI)

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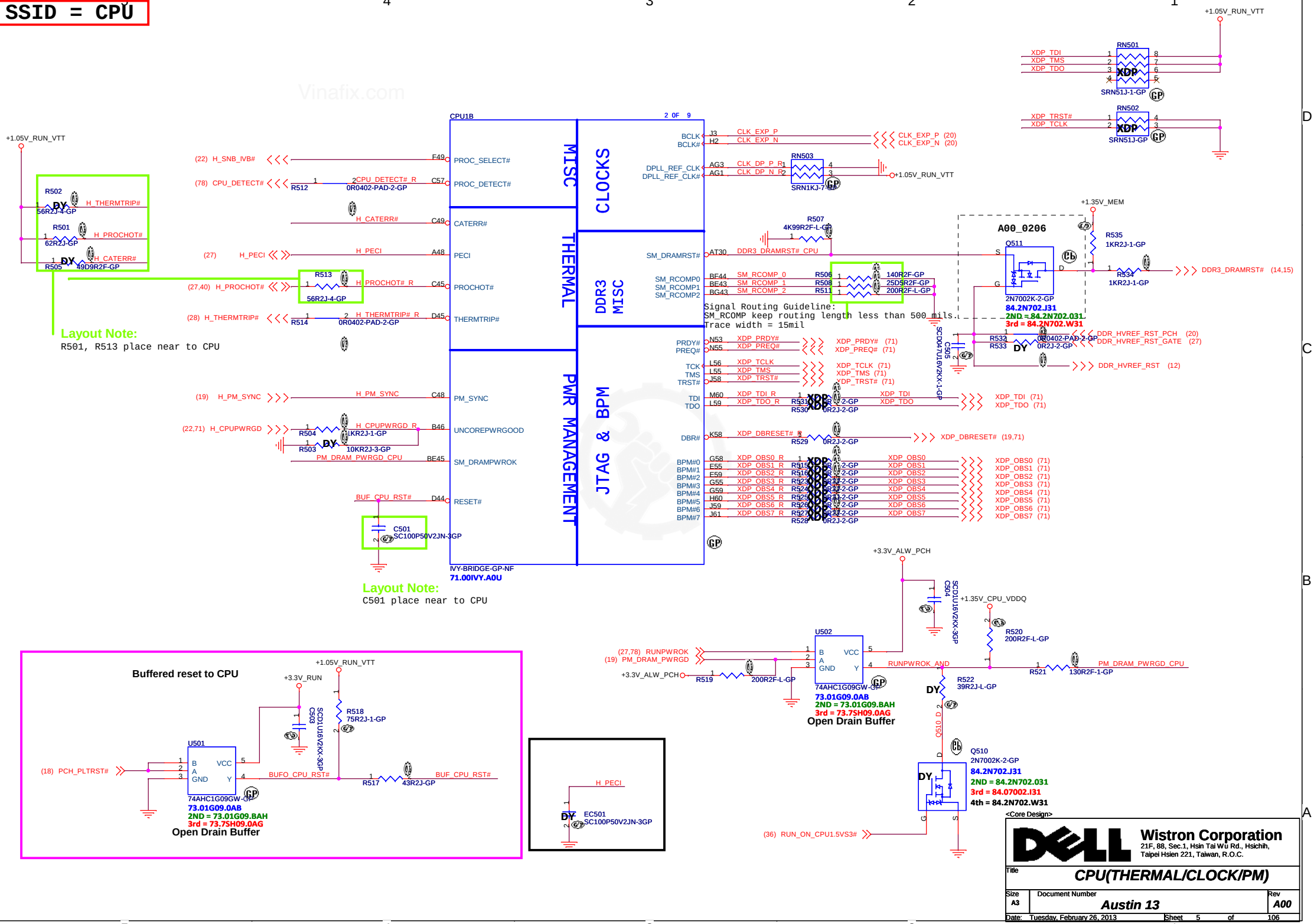
SSID = CPU


CPU1B
2 OF 9
MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM
IVY-BRIDGE-GP-NF
71.00IVY.A0U
Layout Note:
R501, R513 place near to CPU
Layout Note:
C501 place near to CPU
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.
Trace width = 15mil
A00_0206
Buffered reset to CPU
Open Drain Buffer
Open Drain Buffer
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CPU(THERMAL/CLOCK/PM)
Austin 13
A00
Tuesday, February 26, 2013
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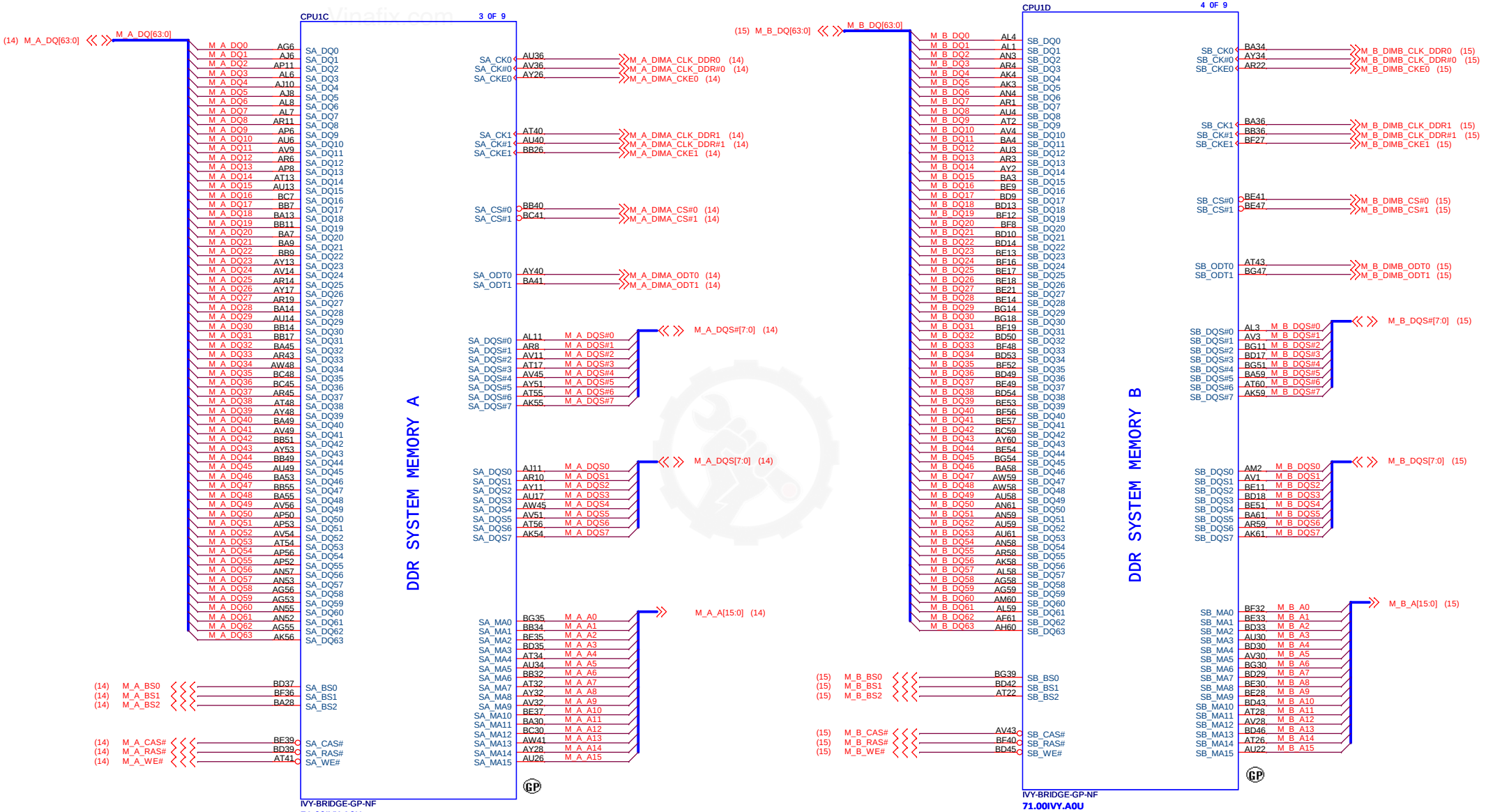
SSID = CPU



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Title: CPU (DDR)

Size	Document Number	Rev
A3	Austin 13	A00

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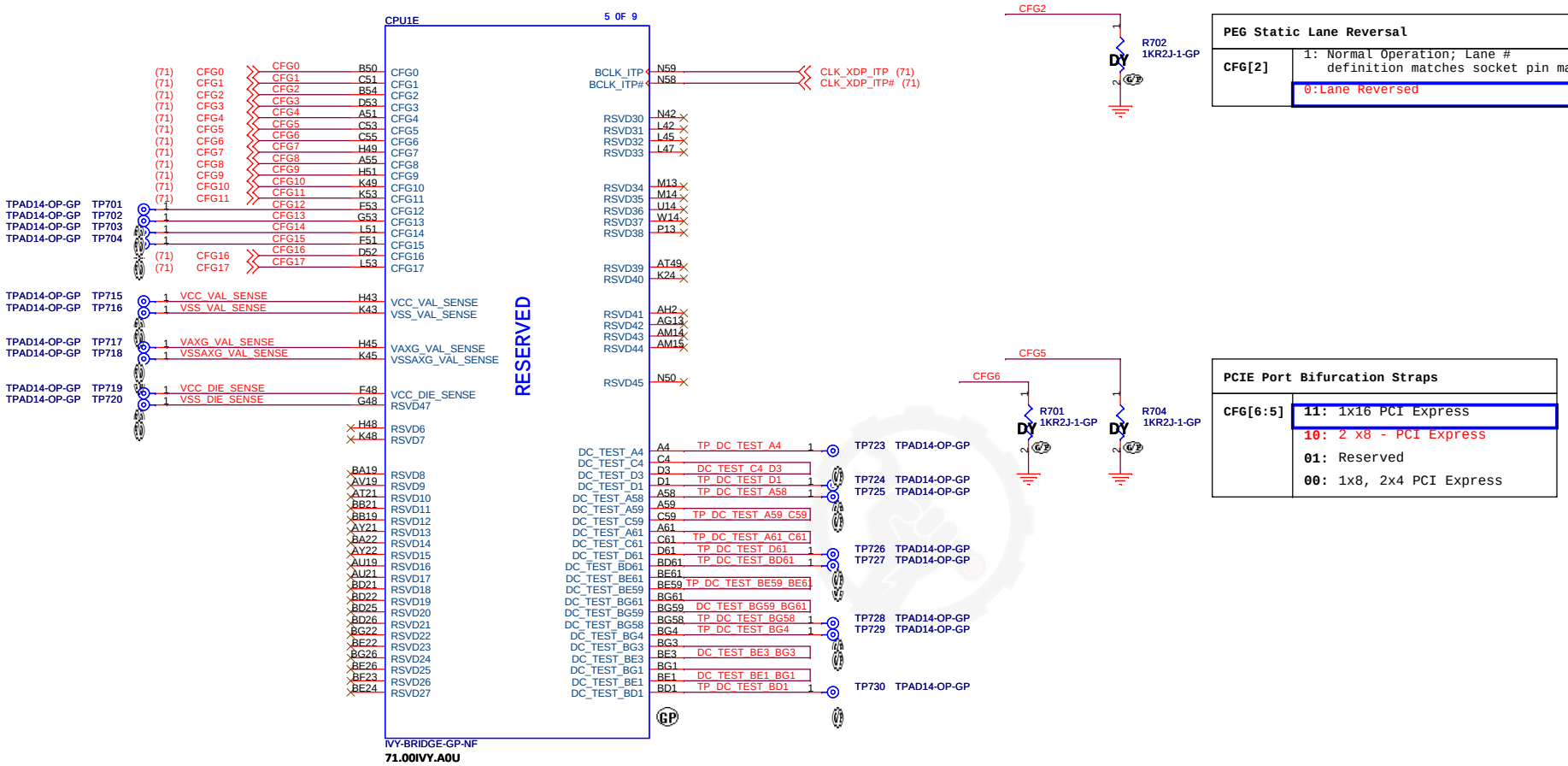
SSID = CPU



PEG Static Lane Reversal	
CFG[2]	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

PCIE Port Bifurcation Straps	
CFG[6:5]	**11:** 1x16 PCI Express
	10: 2 x8 - PCI Express
	01: Reserved
	00: 1x8, 2x4 PCI Express

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Title: CPU (RESERVED)

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SSID = CPU

POWER

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CPU1F

CORE SUPPLY

PEG IO AND DDR IO

QUIET RAILS

SVTID

SENSE LINES

IVY-BRIDGE-GP-NF

71.00IVY.A0U

VCC_CORE

33A

8.5A

+1.05V_RUN_VTT

22 uf x24
10 uf x7
2.2uf x2

22 uf x3
10 ufx9
1 uf x23

Added, cause the 1.05V far away CPU

Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(ULV)	0.3~1.52	33
VAXG(ULV)	0~1.52	33
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.9	4
VCCPLL	1.8	1.2

VCCIO Output Decoupling Recommendation:
330u x 2(Remove)
10u x 10(0603)
1u x 26(0402)

VCCPQ Output Decoupling Recommendation:
1u x 1(0402)

VCC Output Decoupling Recommendation:
1.9m ohm loadline design:(for SV)
470u x 4(Remove)
22u x 20(0805)
2.2u x 35(0402)

2.9m ohm loadline design:(for ULV/LV)
330u x 3(Remove)
22u x 12(0805)
2.2u x 16(0402)

VCCIO_SEL — BC22 — H_SNB_IVB#_PWRCTRL — TP801 TPAD14-OP-GP

VCCPQE1, VCCPQE2 — AM25, AN22 — +V1.05S_VCCPQE_R — R812 0R0402-PAD-2-GP — C826 SC1U6D3V2KX

VIDALERT# — A44 — H_CPU_SVIDALRT# — R803 43R2J1-GP

VIDSCLK — B43 — H_CPU_SVIDCLK

VIDSOUT — C44 — H_CPU_SVIDDAT

R805 75R2F-2-GP

R804 130R2F-1-GP

VR_SVID_ALERT# (42)
H_CPU_SVIDCLK (42)
H_CPU_SVIDDAT (42)

Layout Note:
R803, R804, R805 need close to CPU
Alert# signal must be routed between the Clock and Data lines to reduce the cross talk between them

Need place Pull Hi at IMVP page

VCC_SENSE — F43 — VCCSENSE
VSS_SENSE — G43 — VSSSENSE

R801 100R2F-L1-GP-U
R802 100R2F-L1-GP-U

VCCSENSE (42)
VSSSENSE (42)

Layout Note:
1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing

VCCIO_SENSE — AN16
VSS_SENSE_VCCIO — AN17

R807 10R2F-L-GP
R806 10R2F-L-GP

VCCIO_SENSE (45)
VSSIO_SENSE (45)

Layout Note:
1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing

<Core Design>

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Title: CPU (VCC_CORE)

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SSID = CPU

POWER

VCCAXG Output Decoupling Recommendation:
3.9m ohm loadline design:(for GT2)
470u x 2(remove)
22u x 5(0805)
10u x 6(0603)
1u x 11(0402)

4.6m ohm loadline design:(for GT1)
330u x 2(remove)
22u x 5(0805)
10u x 6(0603)
1u x 6(0402)

22 uf x17
1 uf x7

33A

VCC_GFXCORE

CPU1G

7 OF 9

GRAPHICS

VREF

SM_VREF

SA_DIMM_VREFDQ

SB_DIMM_VREFDQ

DDR3 - 1.5V RAILS

SENSE LINES

QUIET RAILS

1.8V RAIL

SENSE LINES

SA RAIL

VCCSA VID Lines

IVY-BRIDGE-GP-NF

71.00IVY.A0U

Layout Note:
+V_SM_VREF_CNT should have 10 mil trace width

+V_SM_VREF_CNT

+DIMM0_1_VREF_CPU

+DIMM0_1_CA_CPU

Voltage Rail	Voltage(V)	Iccmax(A)
VCC_CORE(ULV)	0.3~1.52	33
VAXG(ULV)	0~1.52	33
VCCIO	1.05	8.5
VDDQ	1.5	5
VCCSA	0.9	6
VCCPLL	1.8	1.2

5A

+1.35V_CPU_VDDQ

10 uf x8
1 uf x10

VDDQ Output Decoupling Recommendation:
330u x 1(Remove)
10u x 8(0603)
1u x 10(0402)

VCCDQ Output Decoupling Recommendation:
1u x 1(0402)

+1.35V_MEM

Layout Note:
For S3 reduction circuit's 1D5V return pass.

Layout Note:
1. PH/PL resisors place close CPU
2. SENSE signal recommend differential routing

R903 100R2F-L1-GP-U

R904 100R2F-L1-GP-U

VCC_AXG_SENSE

VSS_AXG_SENSE

+1.8V_RUN

1.2A

VCCPLL Output Decoupling Recommendation:
330u x 1(Remove)
1u x 2(0402)

+VCC_SA

6A

VCCSA Output Decoupling Recommendation:
330u x 1(Remove)
10u x 5(0603)
1u x 5(0402)

+V1.35S_VCCD_Q

R909 0R0402-PAD-2-GP

TP_VDDQ_SENSE

TP_VDDQ_VSS

TP901 TPAD14-OP-GP

TP902 TPAD14-OP-GP

VCCSA_SENSE

VCCSA_SEL0

VCCSA_SEL1

R911 1KR2J-1-GP

R910 1KR2J-1-GP

VCCSA Power Select		
Voltage(V)	VID[0]	VID[1]
0.9	0	0
0.85	0	1
0.775	1	0
0.75	1	1

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Title: CPU (VCC_GFXCORE)

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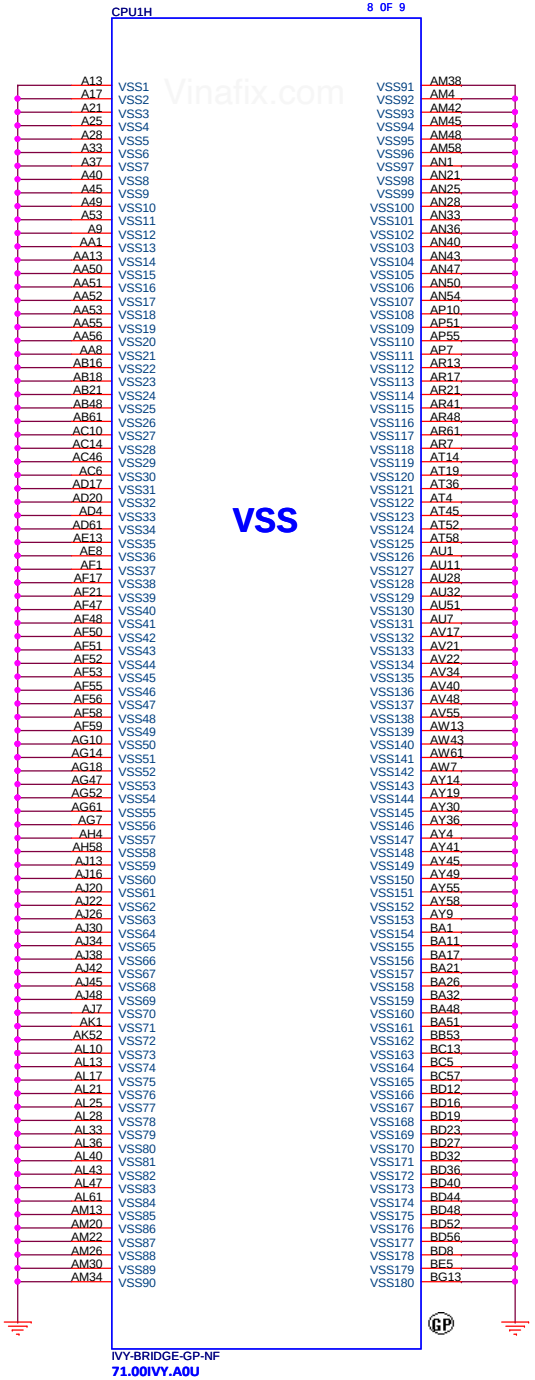
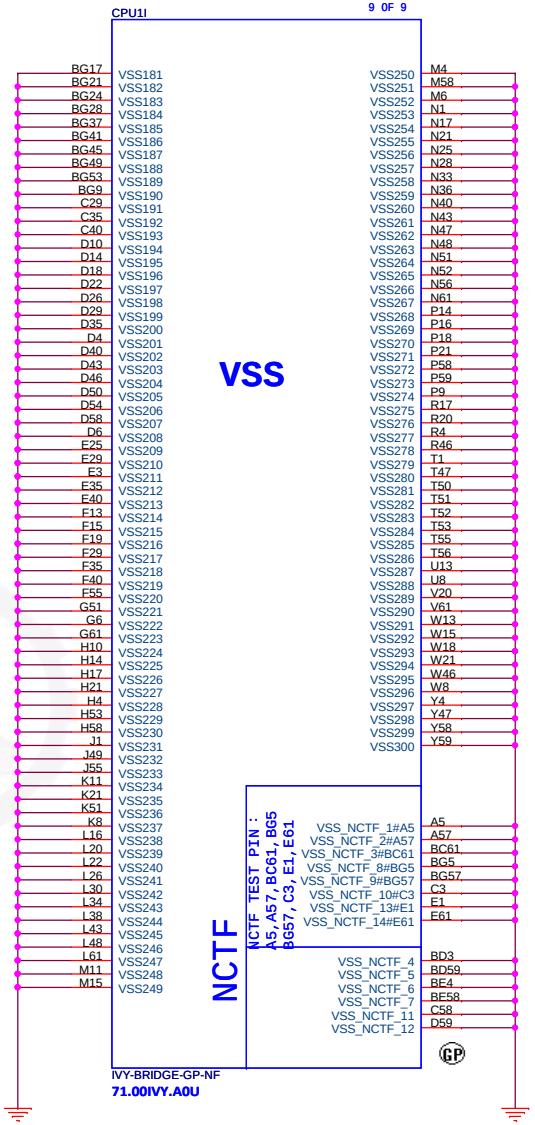
SSID = CPU





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Title: **CPU (VSS)**

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Title: *XDP*		
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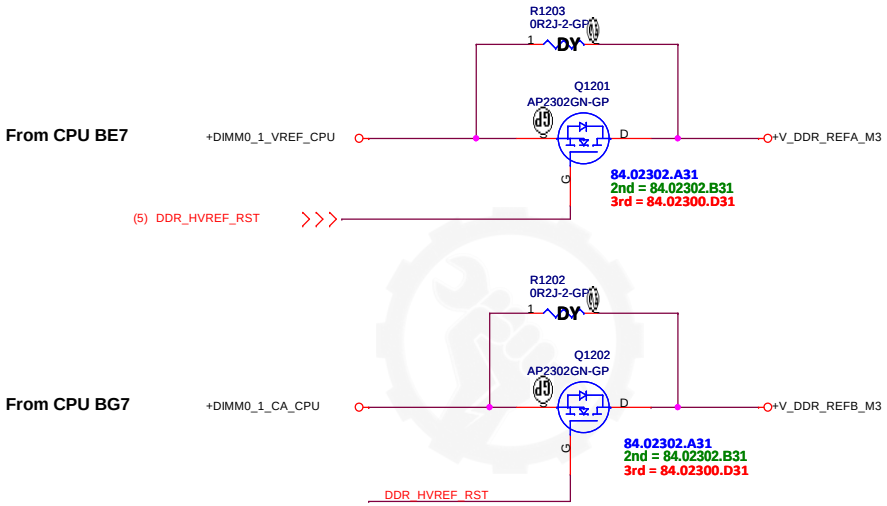
SSID = MEMORY



M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

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Title	DDRM1 & M3 solution	
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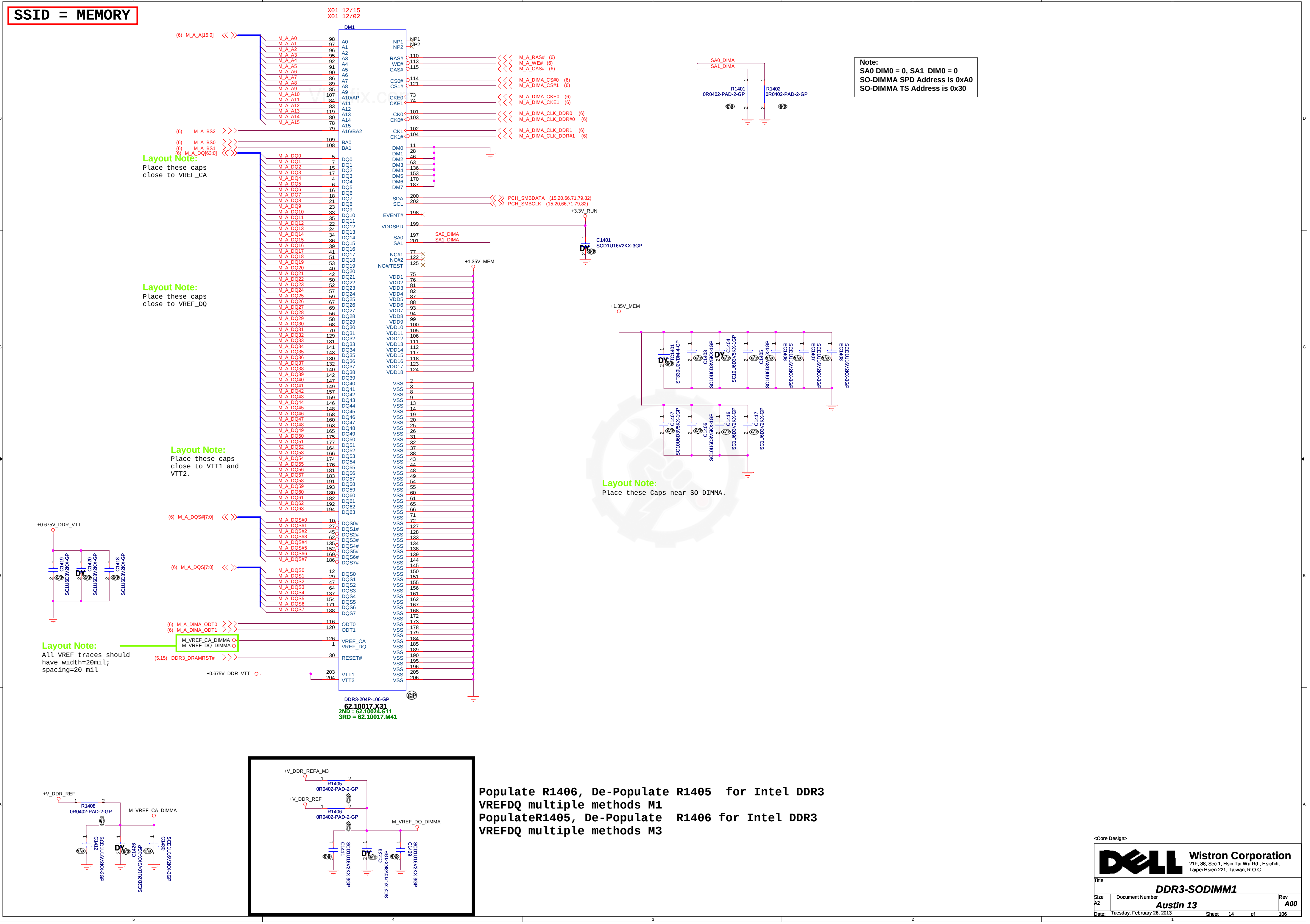

Populate R1406, De-Populate R1405 for Intel DDR3 VREFDQ multiple methods M1
PopulateR1405, De-Populate R1406 for Intel DDR3 VREFDQ multiple methods M3

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Title		
DDR3-SODIMM1		
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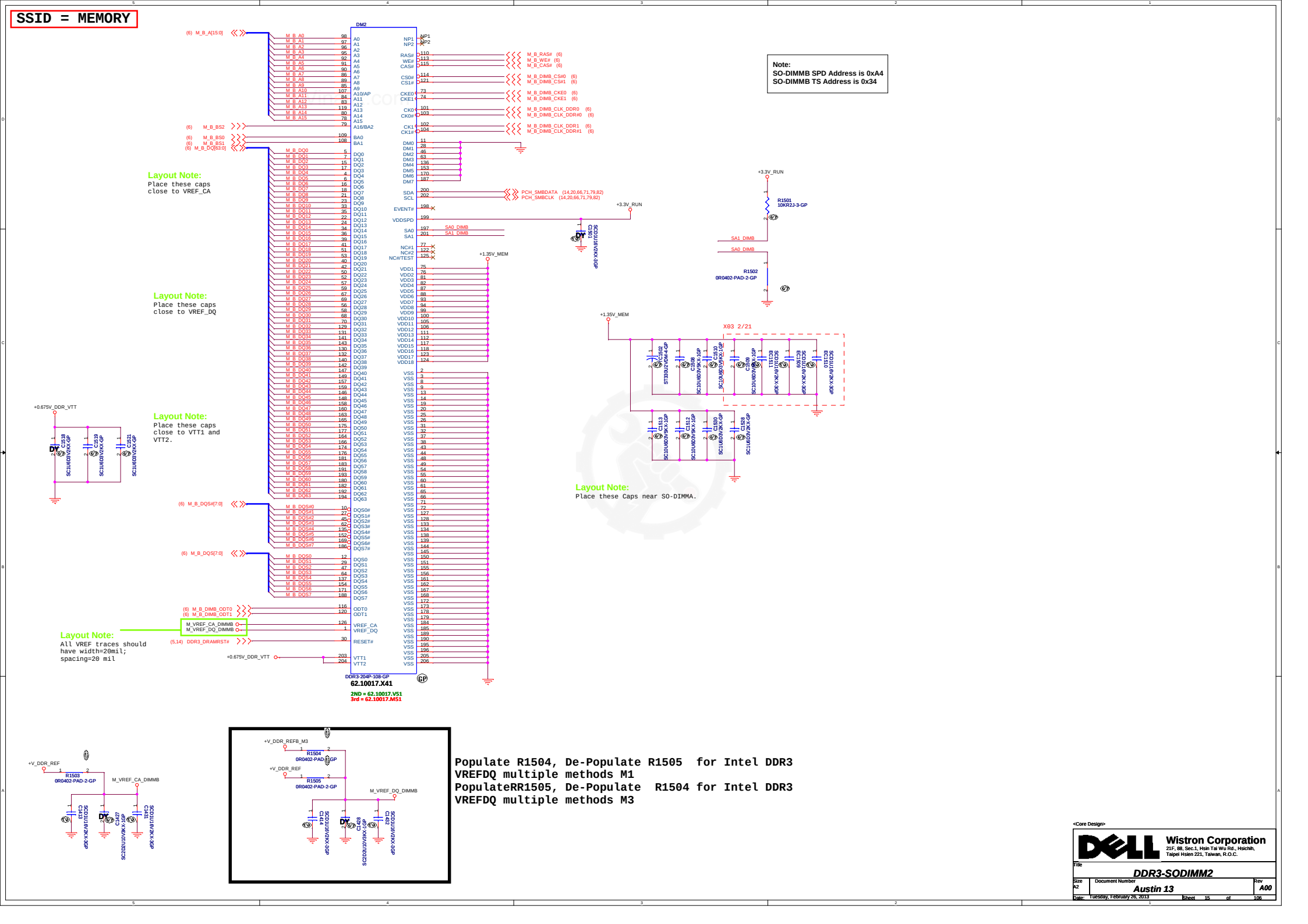
SSID = MEMORY



Populate R1504, De-Populate R1505 for Intel DDR3 VREFDQ multiple methods M1
PopulateRR1505, De-Populate R1504 for Intel DDR3 VREFDQ multiple methods M3

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Title	DDR3-SODIMM2
Size: A2	Document Number: Austin 13
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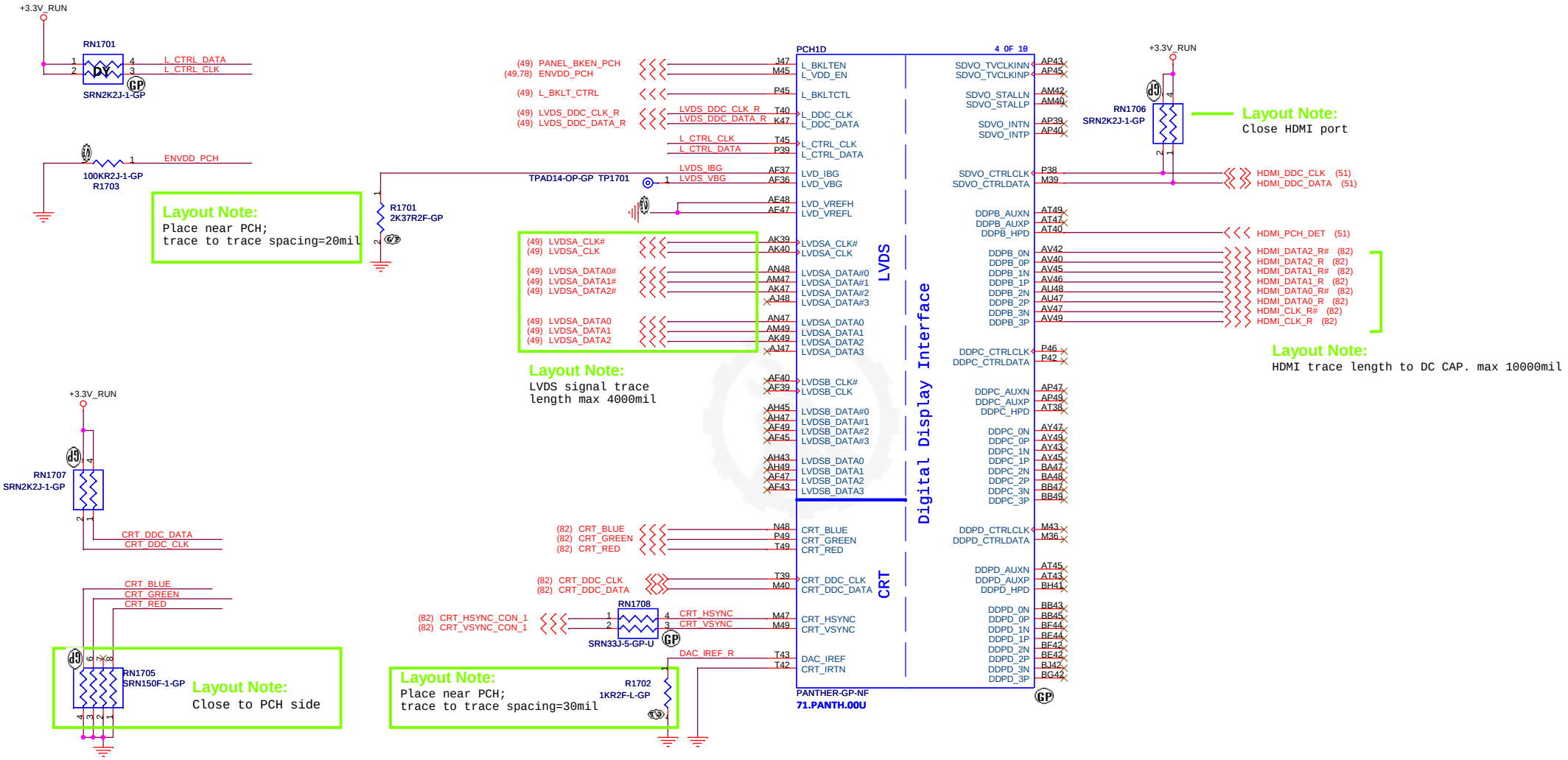
SSID = PCH



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Title	PCH (LVDS/CRT/DDI)	
Size A3	Document Number Austin 13	Rev A00
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SSID = PCH

USB3.0/2.0 Mapping Table

USB 3.0 Port	USB 2.0 port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

Layout Note:
Trace Length :
PCH ~~9000mil~~Cap~~1000mil~~CONN

USB Table

Pair	Device
0	USB0(Left side-HDMI/B)
1	USB1(Right side-IO/B, for USB3.0)
2	USB2(Right side-IO/B, for USB3.0)
3	NC
4	WLAN
5	WWAN
6	NC
7	NC
8	NC
9	NC
10	NC
11	NC
12	CAMERA
13	NC

1. USB Ext. port 9 (HS) External debug port use on Chief River platform.
2. 2011 July; Microsoft will support USB3.0 debug--> Port1 useable.

Boot Bios Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	Boot BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

A16 Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Layout Note:
1. USBRBIAS/# use 50ohm single-ended impedance spacing to other signal=15mil
2. Length < 500mil

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Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: Austin 13 | Rev: A00
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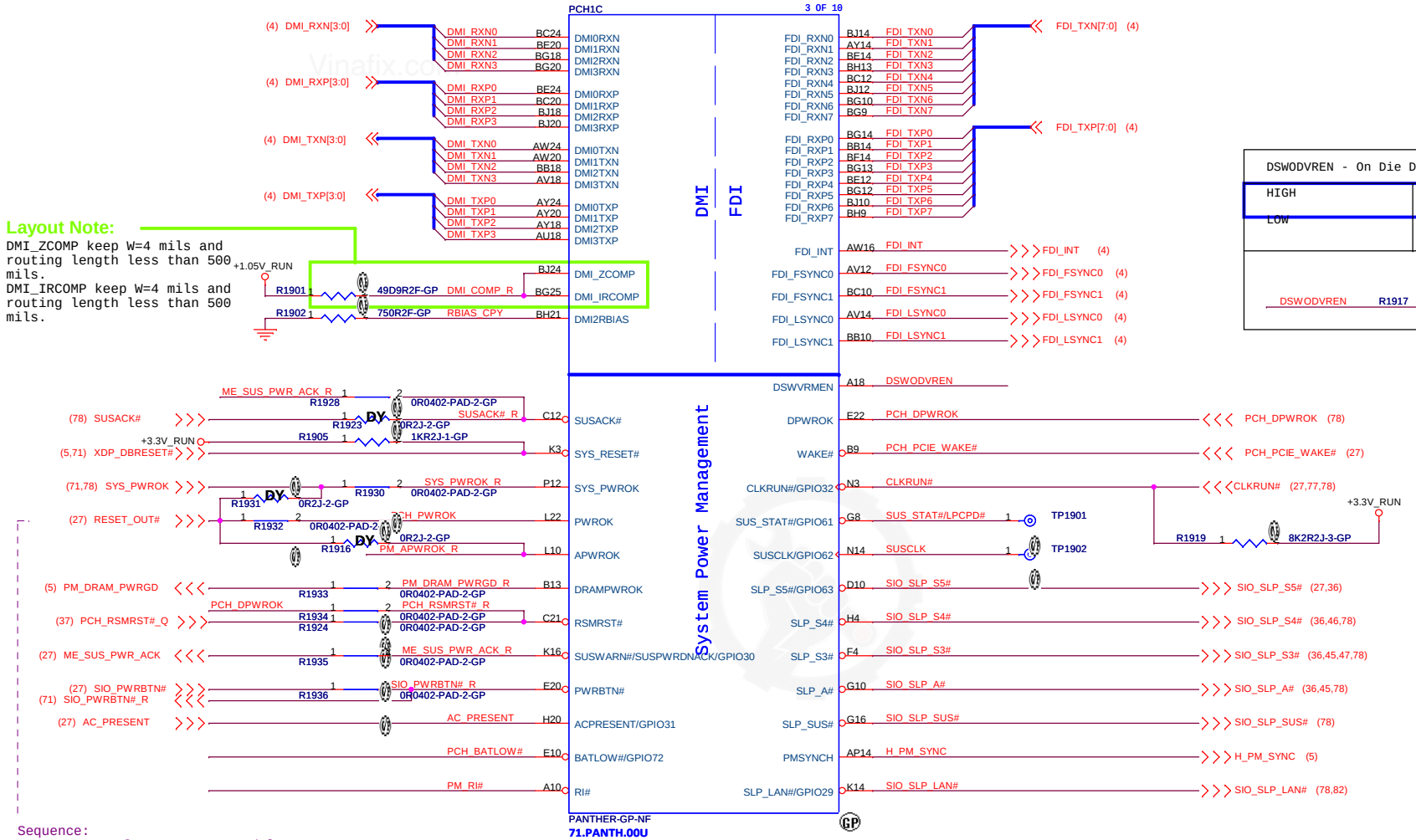
SSID = PCH



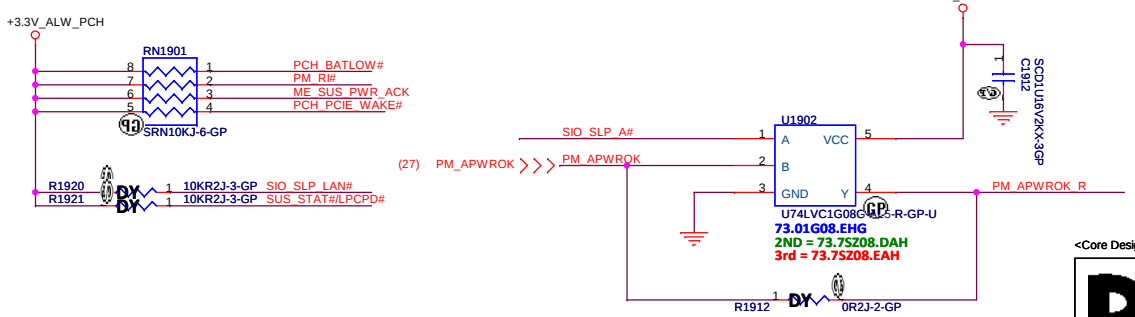
Layout Note:

DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

RTC_AUX_S5
DSWODVREN R1917 330KR2J-L1-GP

Sequence:
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms



<Core Design>

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Title: PCH (DM I/FDI/PM)

Size	Document Number	Rev
A3	Austin 13	A00

Date: Tuesday, February 26, 2013 Sheet 19 of 106

SSID = PCH

S5 power rail CLKREQ#:
PCIECLKRQ[0]#
PCIECLKRQ[7:3]#

S0 power rail CLKREQ#:
PCIECLKRQ[2:1]#

CRB : 1K
CEKLT: 10K

Layout Note:
Layout trace < 14000mil

Layout Note:
CLKOUT termination
place close to PCH <500mil

Layout Note:
1500mil < Layout trace < 10000mil

Can Place Far away PCH

<Core Design>

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Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A2 | Document Number: Austin 13 | Rev: A00

Date: Tuesday, February 26, 2013 | Sheet 20 of 106

SSID = PCH

Layout Note:
Place it at the open door location.

Integrated SUS 1V VRM Enable

INTVRMEN	Low = External VRs High = Internal VRs*

Layout Note:
Place it at the open door location.

Layout Note:
Place near PCH

Layout Note:
Place close together.
For RNxxxx later.

Layout Note:
HDA_SDO and HDA_BCLK must be
length matched to within 500 mils

Layout Note:
Place at the separated point

Layout Note:
HDD < 6000mil, mSATA < 6000mil, ODD < 12500mil

Layout Note:
Place close PCH(<500mil)

Flash Descriptor Security Overide/ Intel ME Debug Mode

HDA_SDOUT	Low = Default * High = Enable

No Reboot Strap

HDA_SPKR	Low = Default * High = No Reboot

PLL ODVR VOLTAGE

HDA_SYNC	Low = 1.8V High = 1.5V *

HDA_SYNC:
This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

PCH1A — 1 OF 10 — PANTHER-GP-NF — 71.PANTH.00U

BBS_BIT0 - BIOS BOOT STRAP BIT0

<Core Design>

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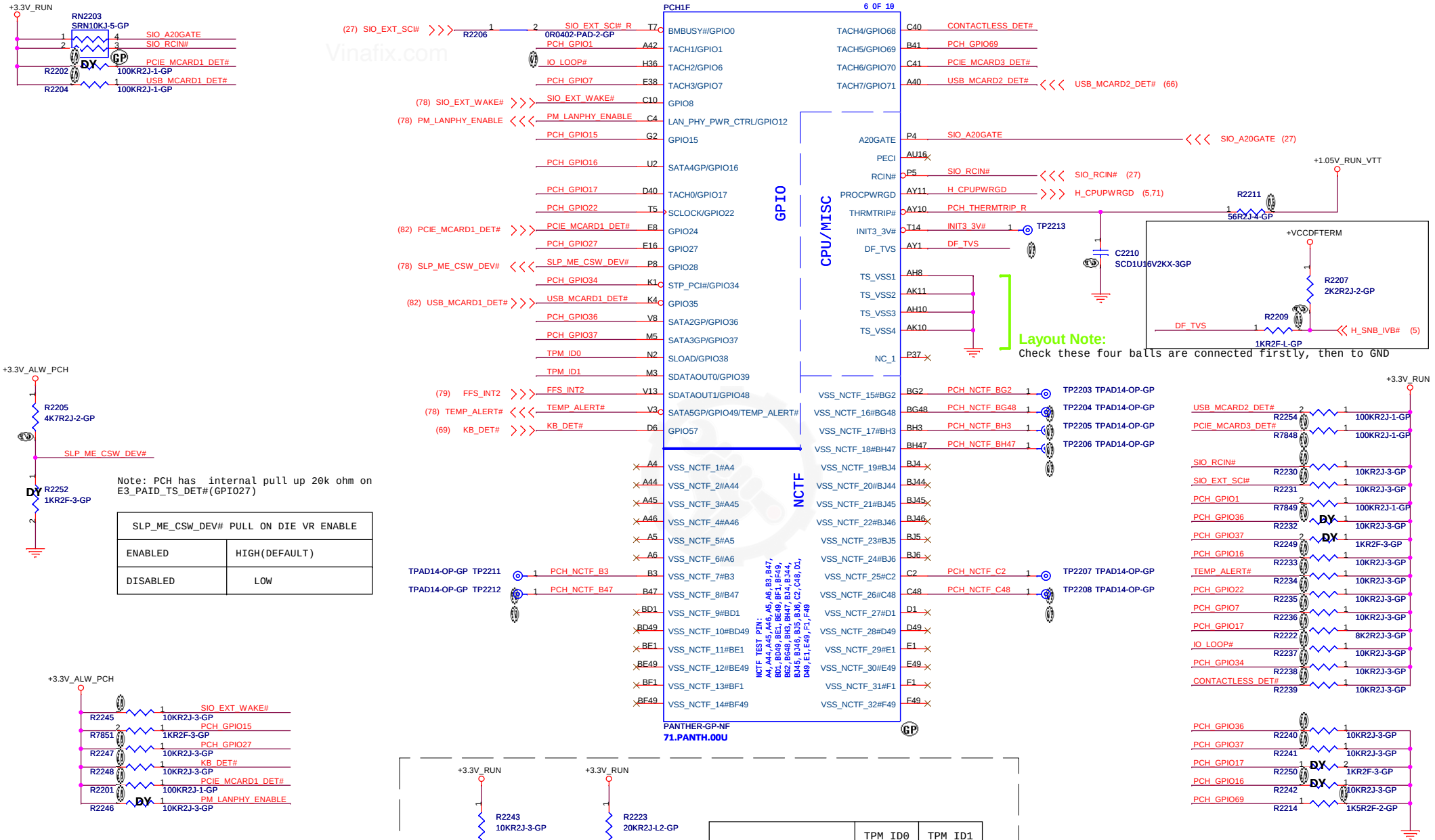
Title: PCH (SPI/RTC/LPC/SATA/IHDA)

Size	Document Number	Rev
A3	Austin 13	A00

Date: Tuesday, February 26, 2013 Sheet 21 of 106

SSID = PCH


PCH1F
6 OF 10
GPIO
CPU/MISC
NCTF
PANTHER-GP-NF
71.PANTH.00U
Layout Note:
Check these four balls are connected firstly, then to GND
Note: PCH has internal pull up 20k ohm on E3_PAID_TS_DET#(GPIO27)
SLP_ME_CSW_DEV# PULL ON DIE VR ENABLE
ENABLED HIGH(DEFAULT)
DISABLED LOW
TPM_ID0 TPM_ID1
No TPM, No China TPM 0 1
TPM 1 1
TBD
<Core Design>
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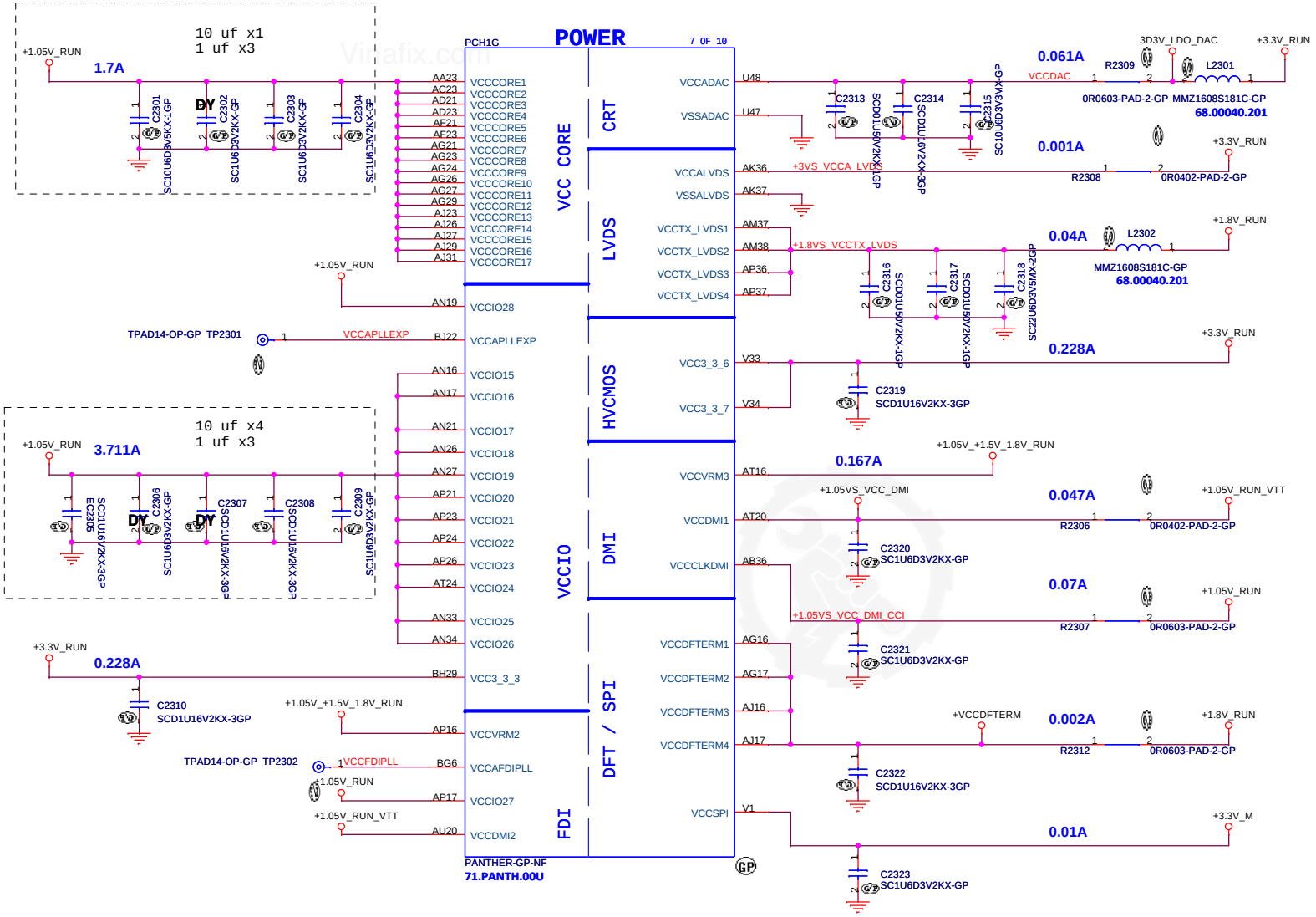
PCH (GPIO/CPU)
Austin 13
A00
Tuesday, February 26, 2013
Sheet 22 of 106

SSID = PCH



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

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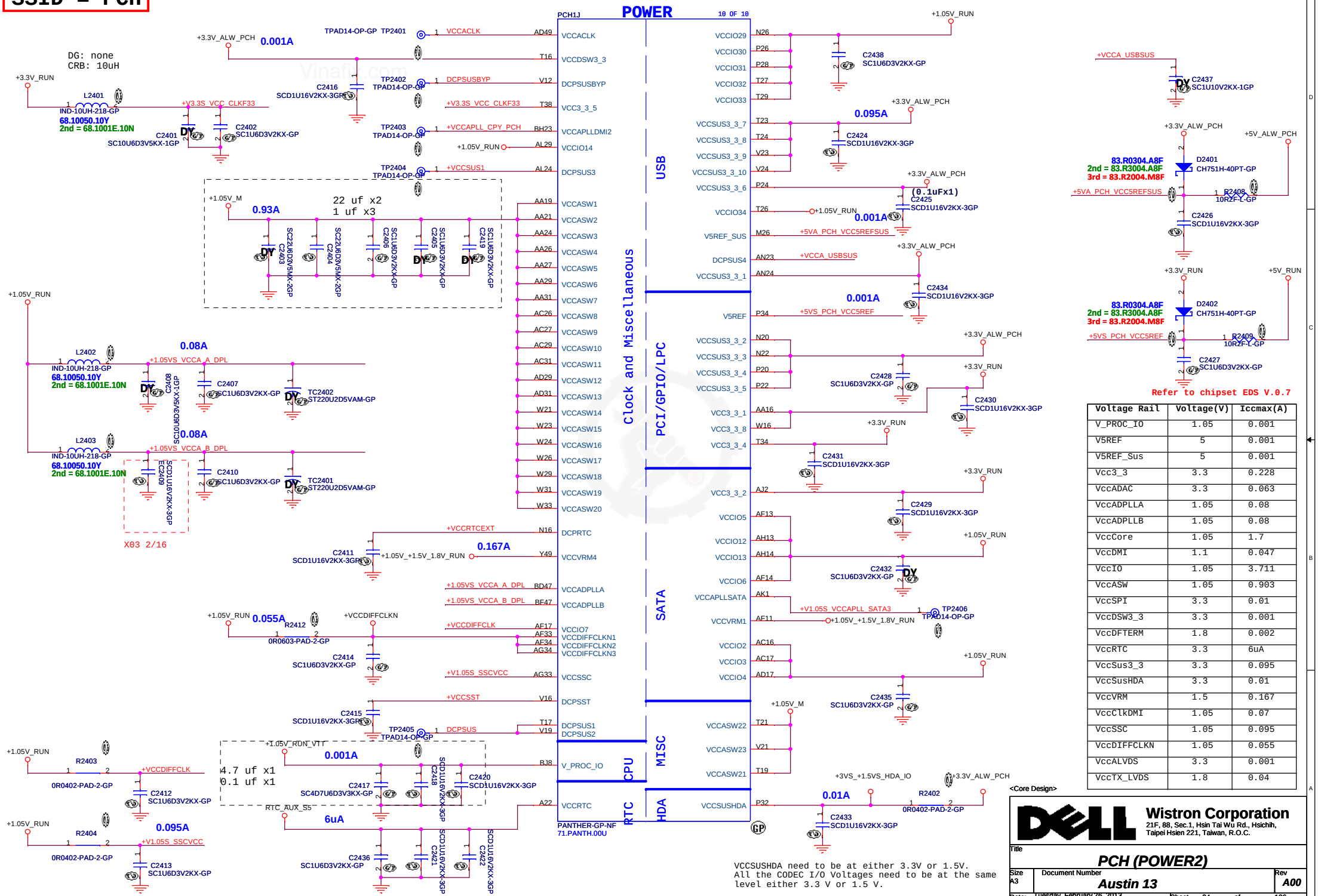
Title: PCH (POWER1)

Size: A3 | Document Number: Austin 13 | Rev: A00

Date: Tuesday, February 26, 2013 | Sheet 23 of 106

SSID = PCH



Voltage Rail	Voltage(V)	Iccmax(A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.1	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW3_3	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3	0.01
VccVRM	1.5	0.167
VccClkDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

VCCSUSHDA need to be at either 3.3V or 1.5V.
All the CODEC I/O Voltages need to be at the same level either 3.3 V or 1.5 V.

<Core Design>

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Title: PCH (POWER2)

Size	Document Number	Rev
A3	Austin 13	A00

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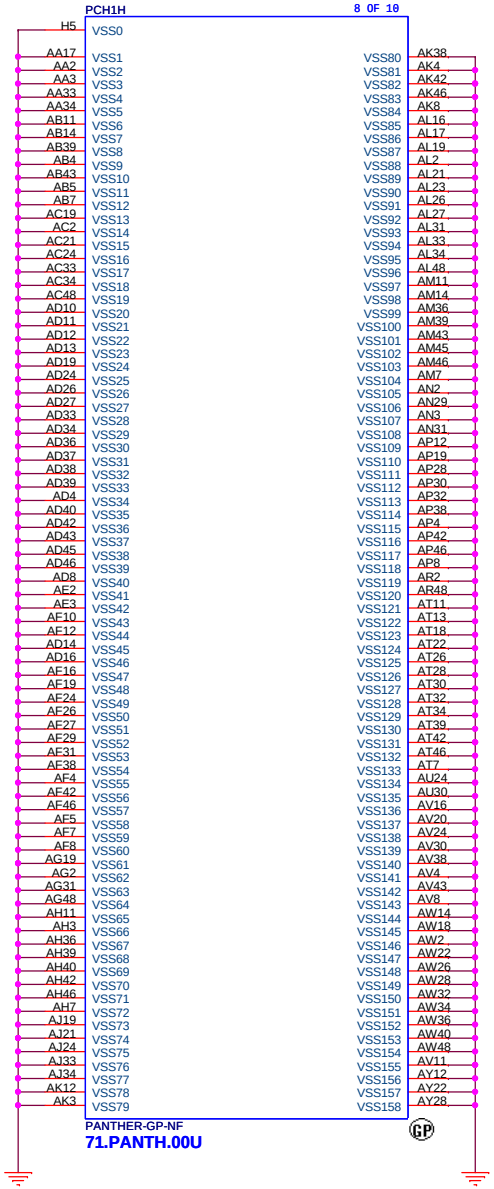
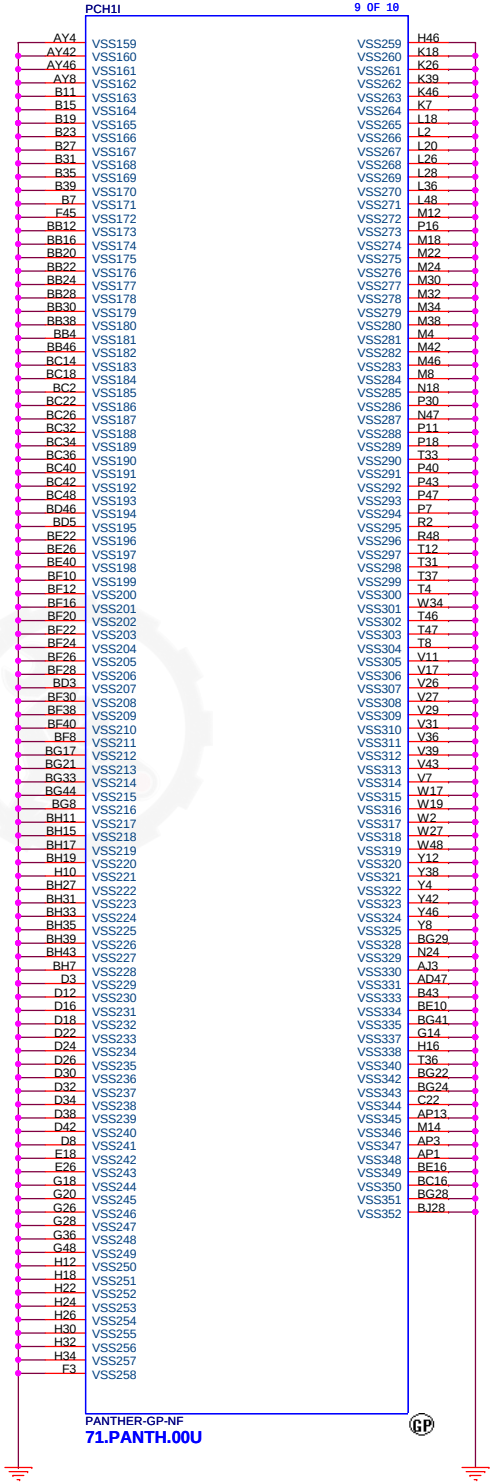
SSID = PCH





<Core Design>

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Title: **PCH (VSS)**

Size	Document Number	Rev
A3	Austin 13	A00

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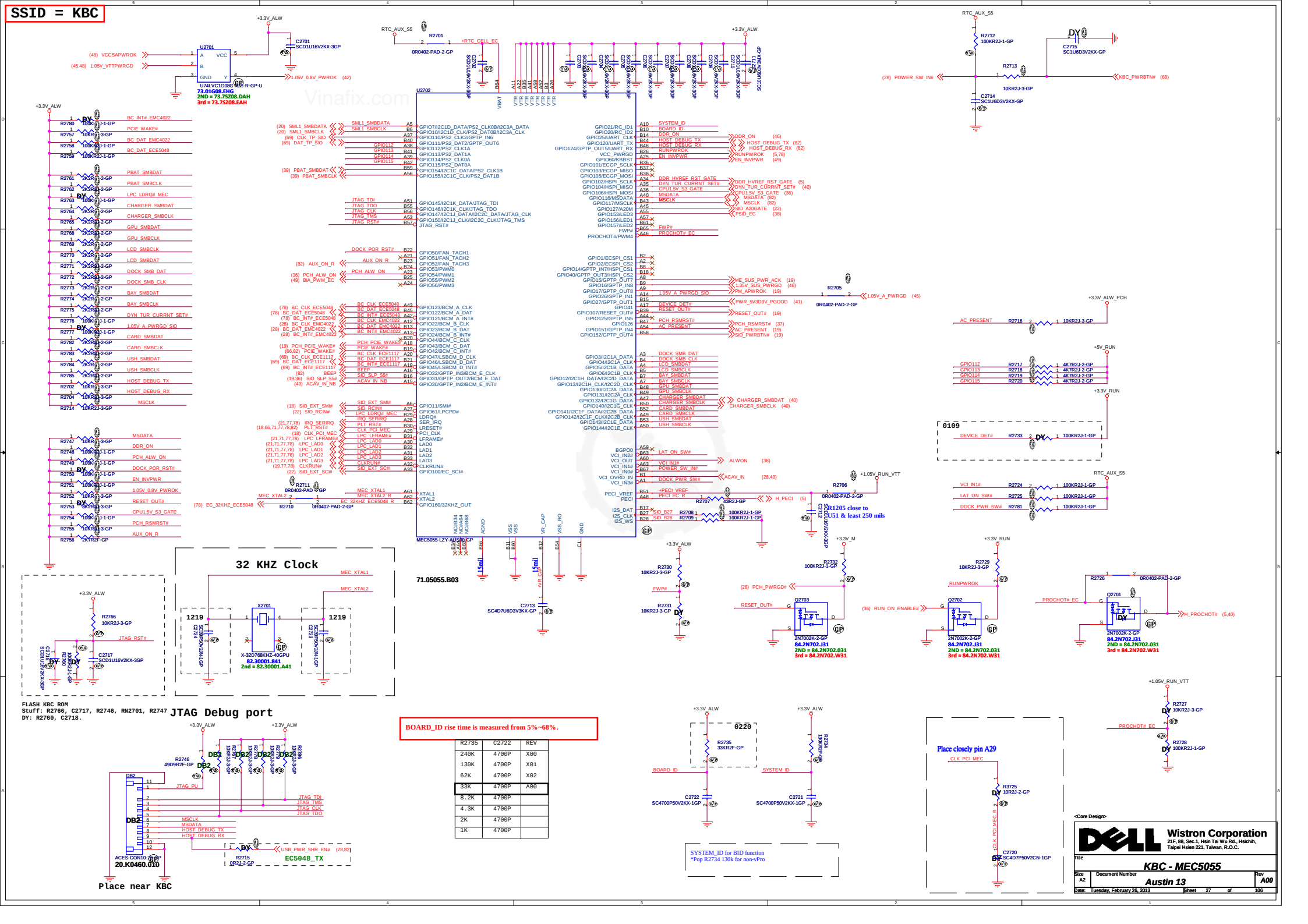
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***		
Size: A3	Document Number: ***Austin 13***	Rev: ***A00***
Date: Tuesday, February 26, 2013	Sheet 26 of 106	

SSID = KBC



Wistron Corporation
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Title: **KBC - MEC5055**

Size: A2 | Document Number: **Austin 13** | Rev: **A00**

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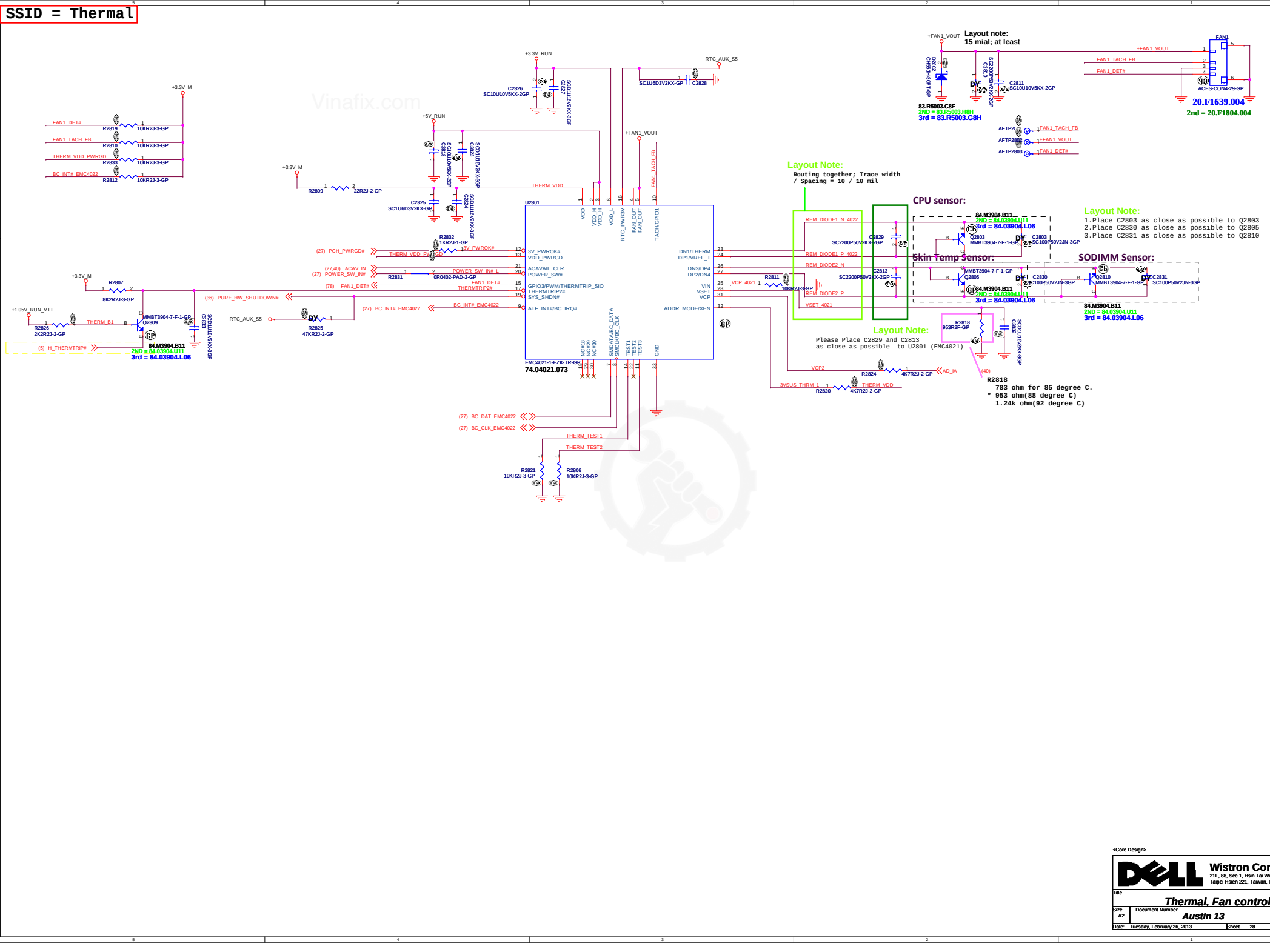
SSID = Thermal



<Core Design>

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Title: Thermal, Fan controller

Size	Document Number	Rev
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Date: Tuesday, February 26, 2013 Sheet 28 of 106

SSID = AUDIO

(Blanking)

<Core Design>

Wistron Corporation
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Title	Audio Codec 92HD94	
Size: A3	Document Number: Austin 13	Rev: A00
Date: Tuesday, February 26, 2013	Sheet 29 of 106	

(Blanking)

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<Core Design>

Wistron Corporation
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Title: *LAN Chip*		
Size: *A3*	Document Number: *Austin 13*	Rev: *A00*
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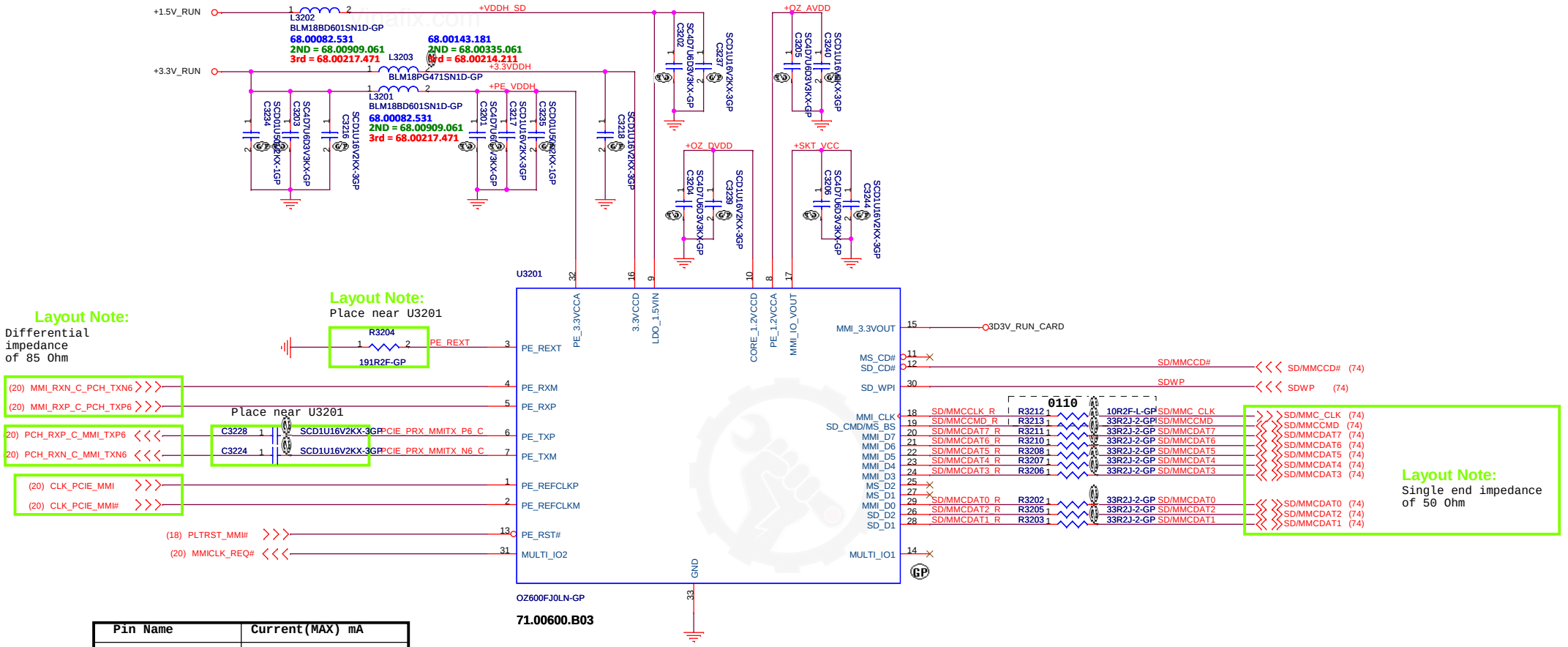
SSID = SDIO



Pin Name	Current(MAX) mA
3.3VCCD(pin16)	800 mA
PE_VCCA(pin32)	150 mA
LDO_1.5VIN(pin9)	150 mA
MMI_3.3VOUT(pin15)	SD3.0 spec is 800 mA
CORE_1.2VCCD(pin10)	100 mA
PE_1.2VCCA(pin8)	100 mA
MMI_IO_VOUT(pin17)	100 mA

<Core Design>

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Title: Card Reader

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Date: Tuesday, February 26, 2013 Sheet 32 of 106

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Austin 13* | Rev: *A00*

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(Blanking)

<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
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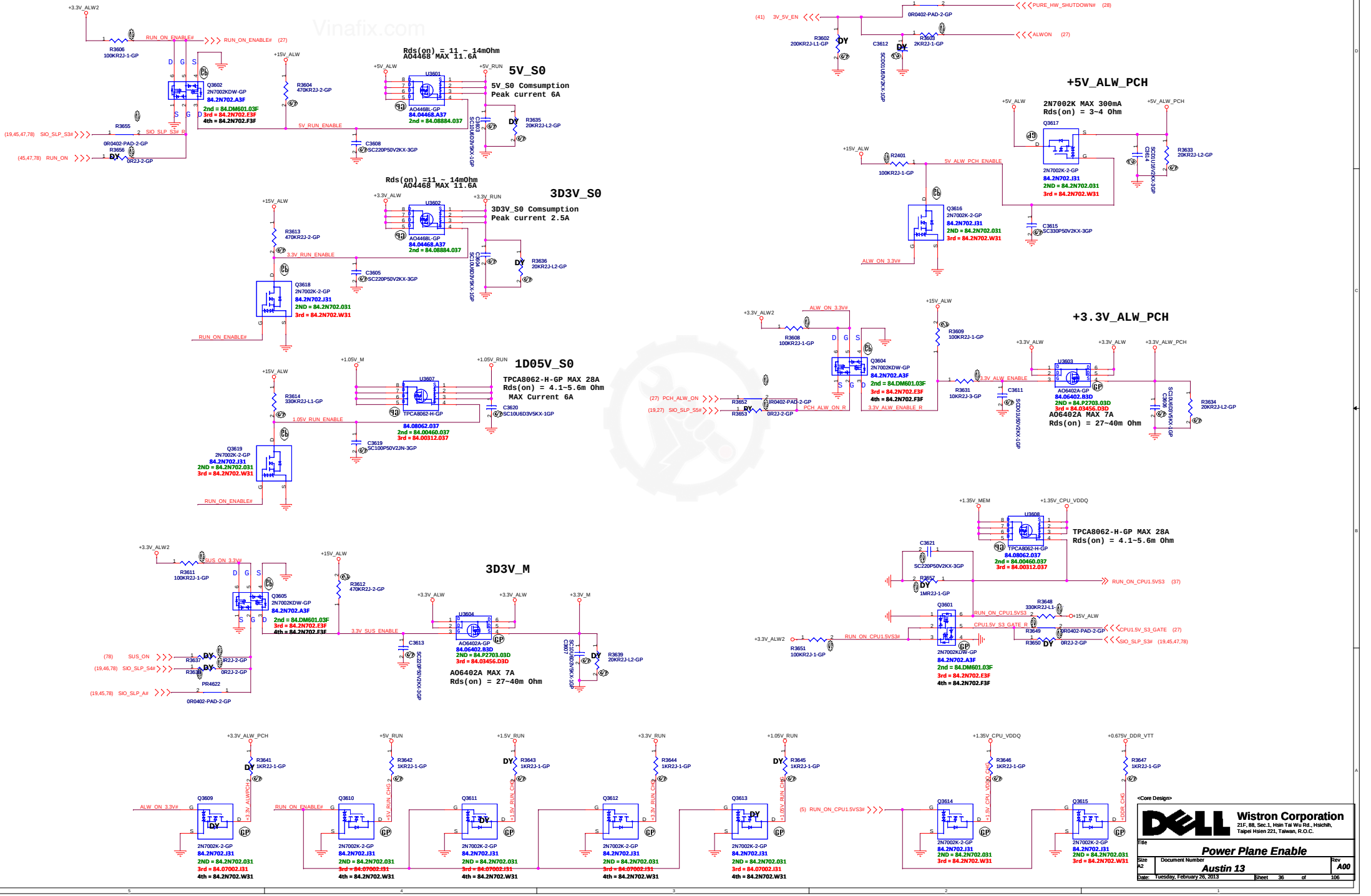
(Blanking)

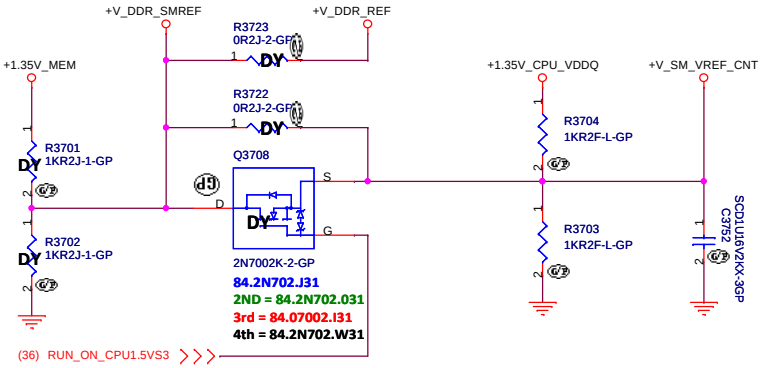
SSID = Reset.Suspend

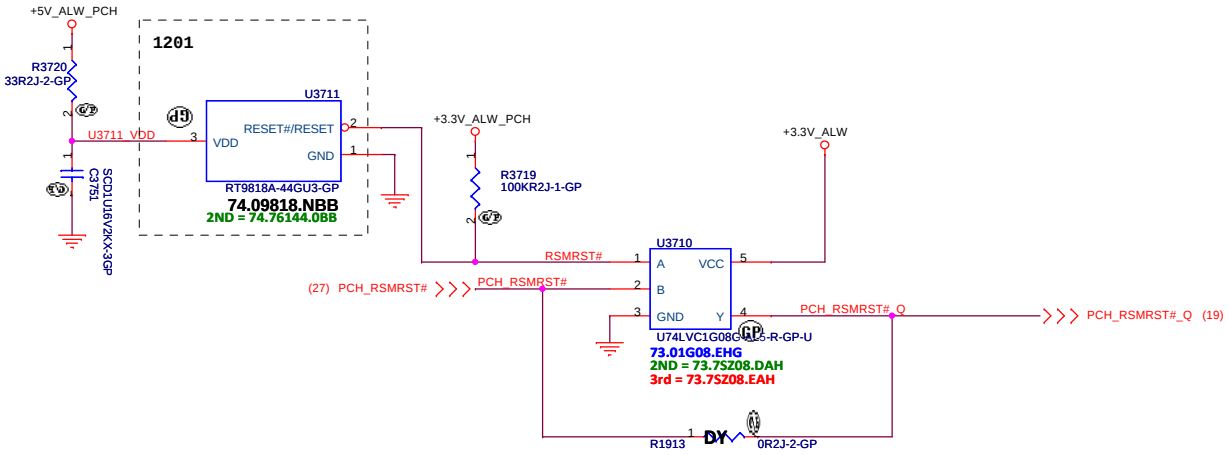
ROSA Run Power



SSID = Reset.Suspend

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation





<Core Design>

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Title	S3 Power Reduction	
Size A3	Document Number: Austin 13	Rev: A00
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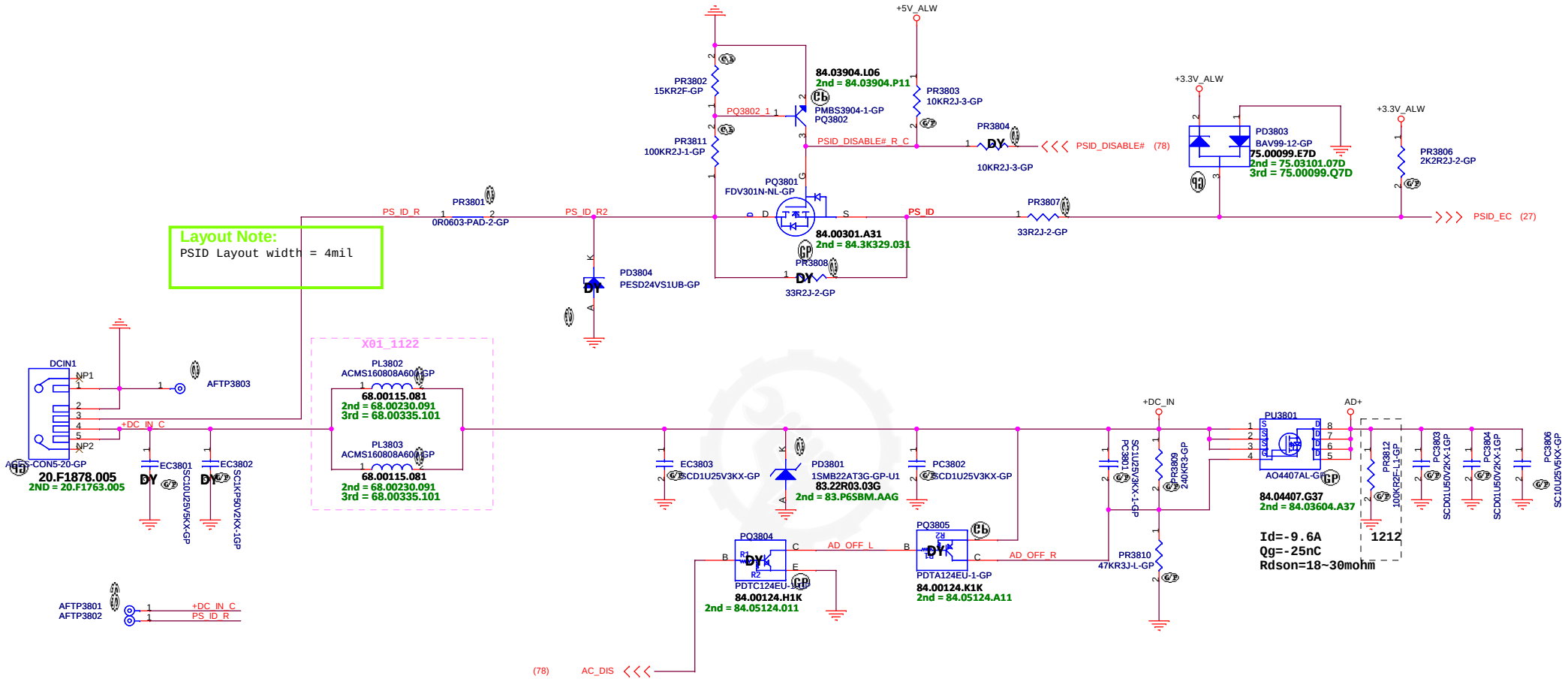
SSID = PWR.Support



<Core Design>

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Title: DCIN		
Size: A3	Document Number: Austin 13	Rev: A00
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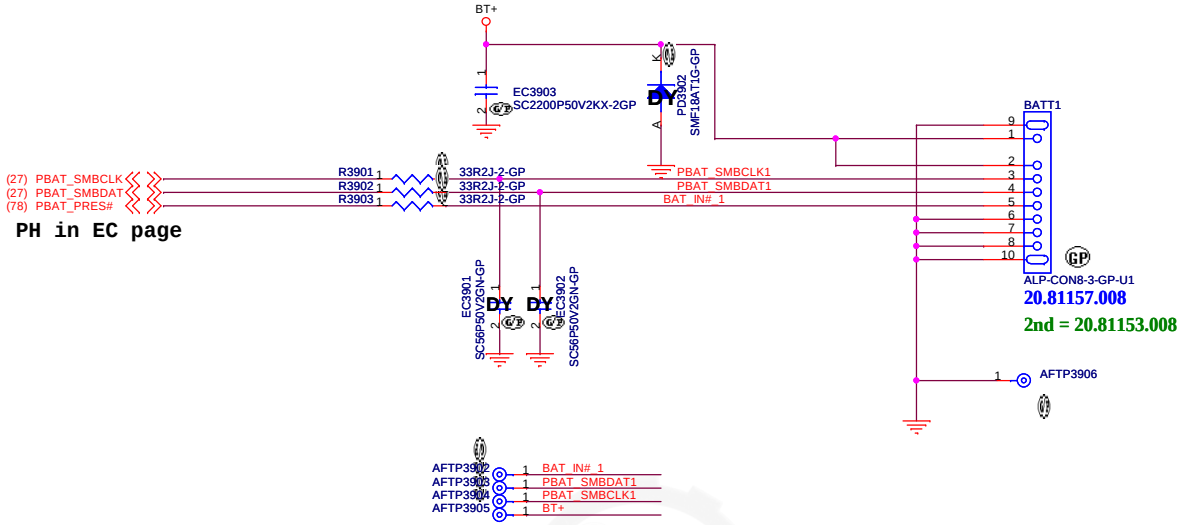
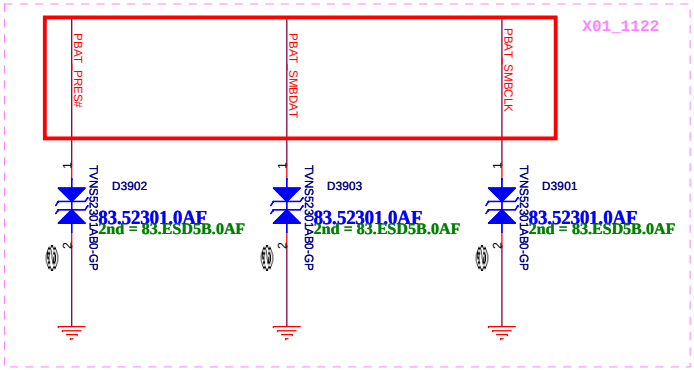
SSID = PWR.Support

Batt Connecter



Placement: Close to Batt Connector



<Core Design>

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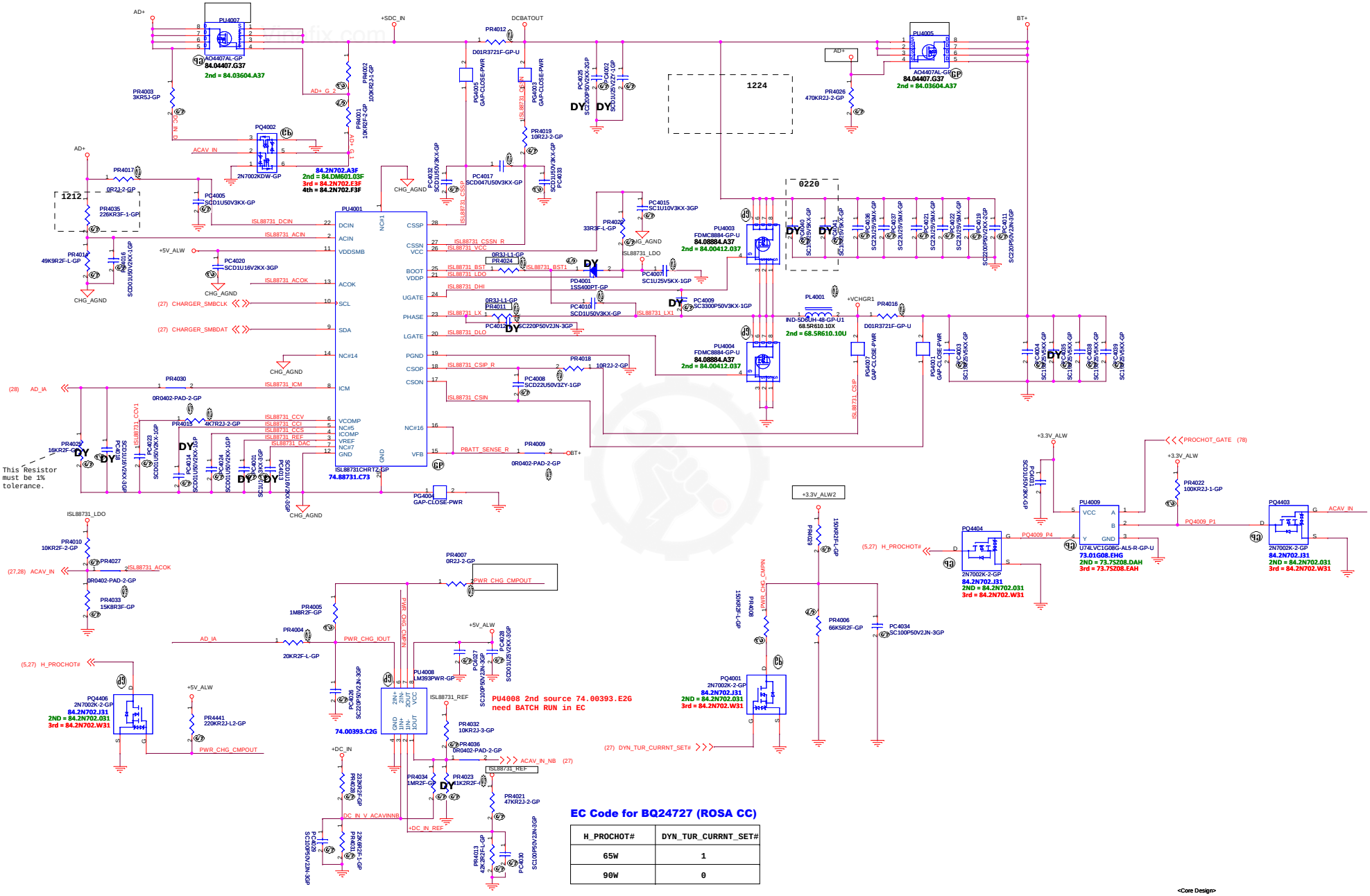
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

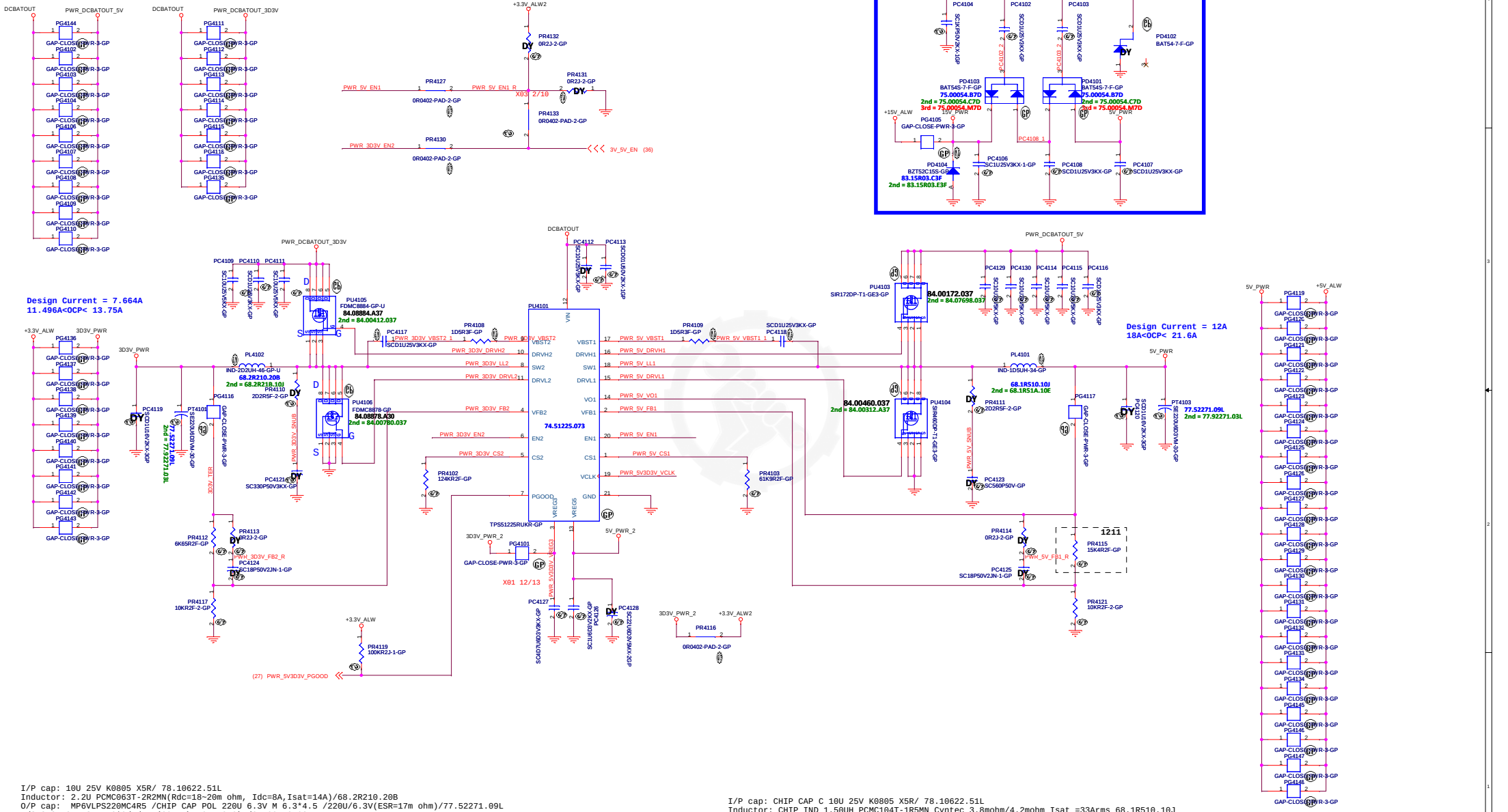
Size	Document Number	Rev
A3	Austin 13	A00

Date: Tuesday, February 26, 2013 Sheet 39 of 106

SSID = Charger



SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MN(Rdc=18~20m ohm, Idc=8A,Isat=14A)/68.2R210.20B
O/P cap: MP6VLPS220MC4R5 /CHIP CAP POL 220U 6.3V M 6.3*4.5 /220U/6.3V(ESR=17m ohm)/77.52271.09L
H/S:SIS412DN SIZE:3*3/Id=7A(30m ohm,Qg=12nC) /84.00412.037
L/S:SIS780DN/ POWERPAK 121Id=9.5A/ (14.5~17.5m ohm,Qg=11nC)/84.00780.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 1.50UH PCMC104T-1R5MN Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: MP6VLPS220MC4R5 /CHIP CAP POL 220U 6.3V M 6.3*4.5 /220U/6.3V(ESR=17m ohm)/77.52271.09L
H/S: FET MOS SIR172DP-T1-GE3 NC POWERPAK 8P/Id=12.9A(10.3~12.4m ohm,Qg=98nC)/84.00172.037
L/S: FET MOS SIR460DP-T1-GE3 NC SO8/Id=19.4A(4.9~6.1m ohm,Qg=16.8nC)/84.00460.037

<Core Design>

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Title: TPS51125 5V/3D3V

Size: A2 | Document Number: Austin 13 | Rev: A00

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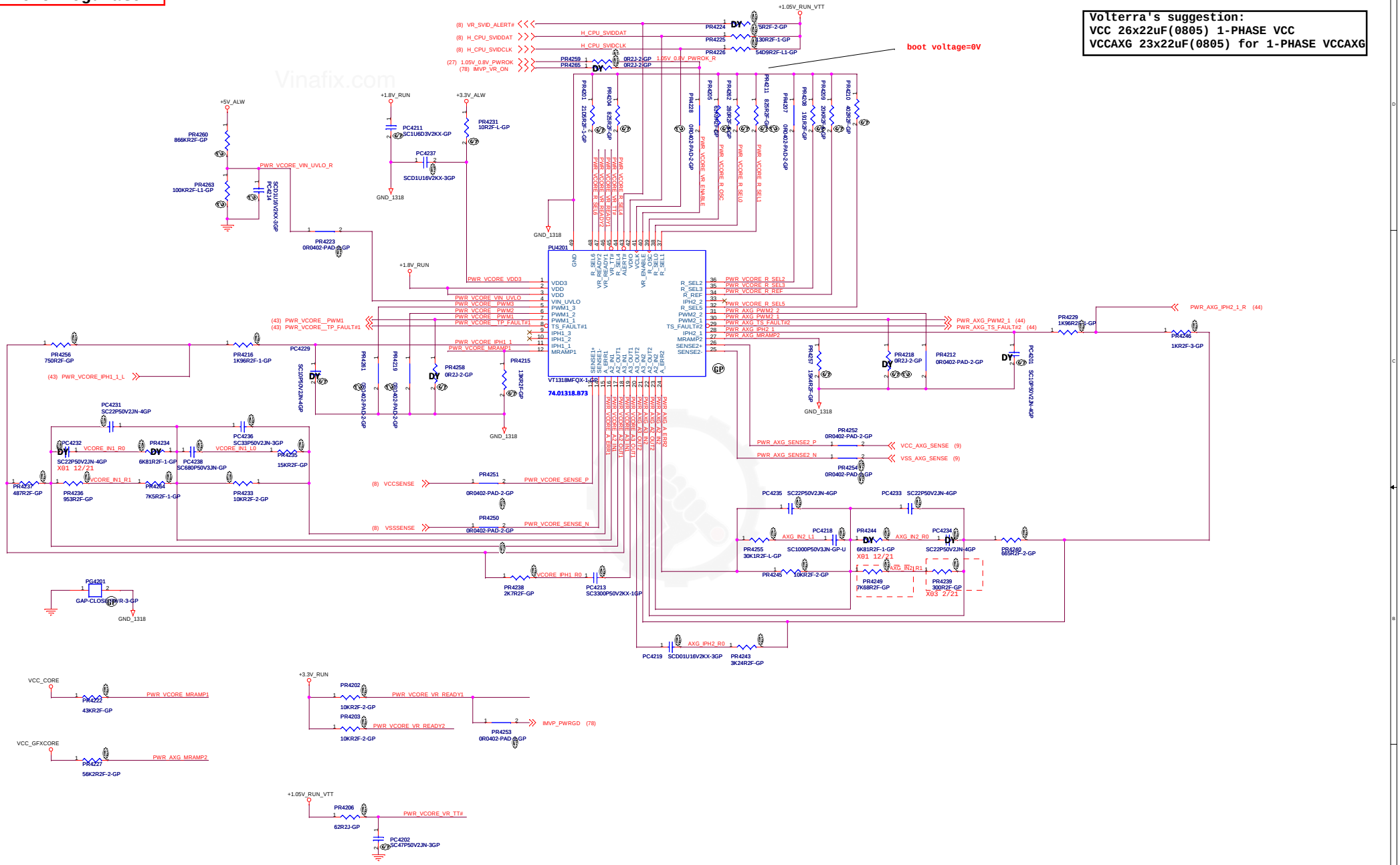
SSID = CPU.Regulator

Volterra's suggestion:
VCC 26x22uF(0805) 1-PHASE VCC
VCCAXG 23x22uF(0805) for 1-PHASE VCCAXG

boot voltage=0V



<Core Design>

DELL **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *VT1318+1323_CPU_CORE1+1(1/3)*

Size: A2 | Document Number: *Austin 13* | Rev: *A00*

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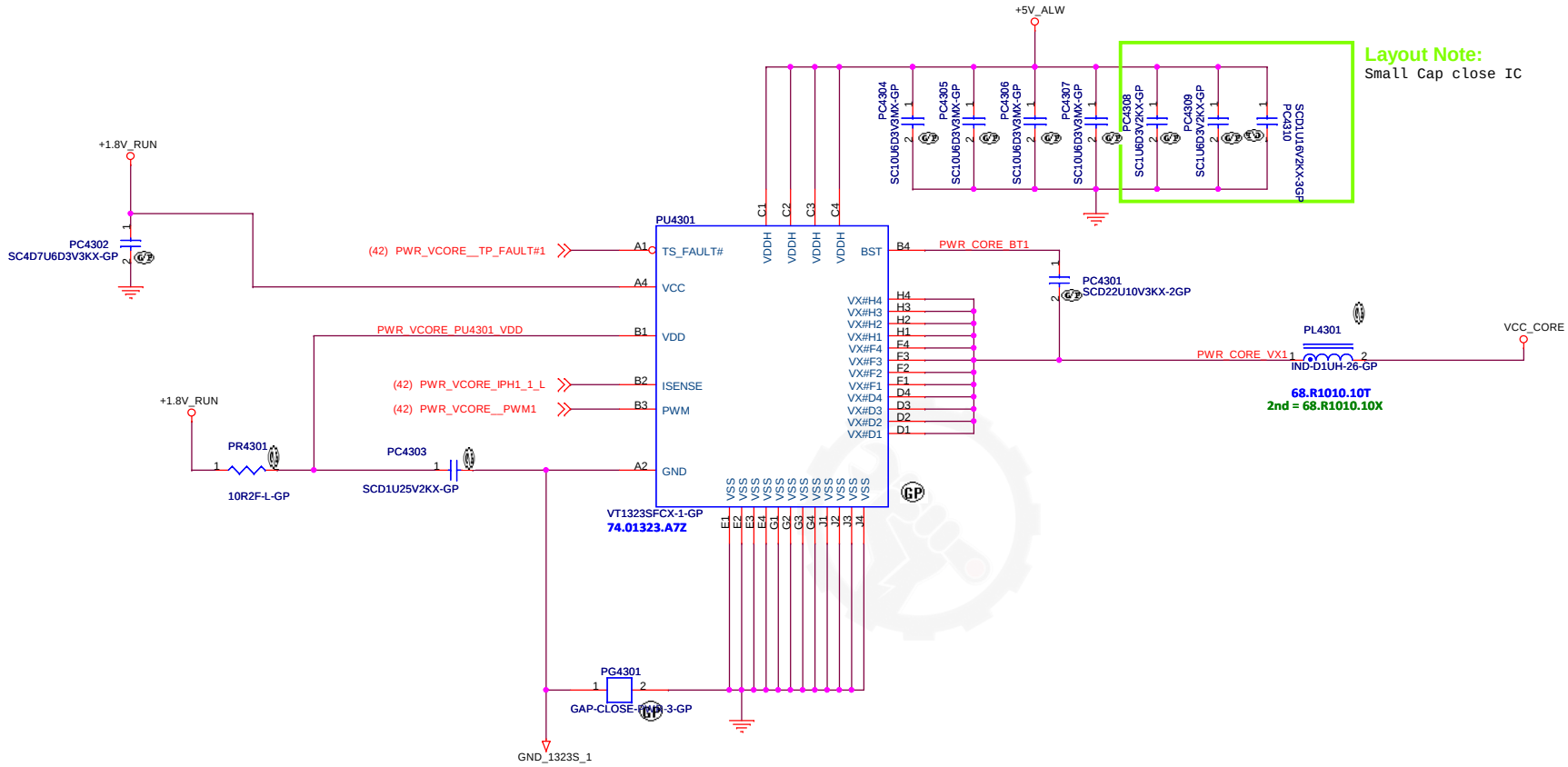
SSID = CPU.Regulator



<Core Design>

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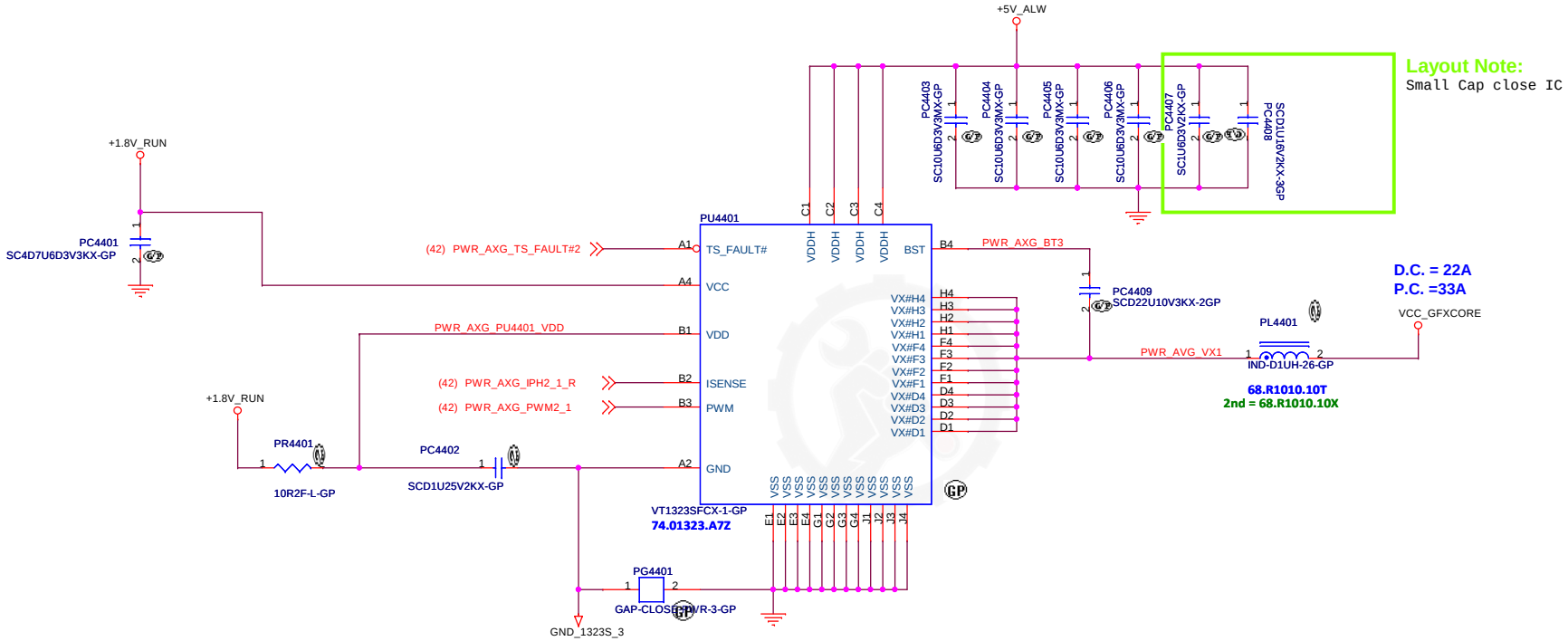
Title: VT1318+1326_CPU_CORE2+1(2/3)

Size	Document Number	Rev
A3	Austin 13	A00

Date: Tuesday, February 26, 2013 Sheet 43 of 106

SSID = CPU.Regulator



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	VT1318+1323_CPU_CORE1+1(3/3)	
Size A3	Document Number: Austin 13	Rev A00
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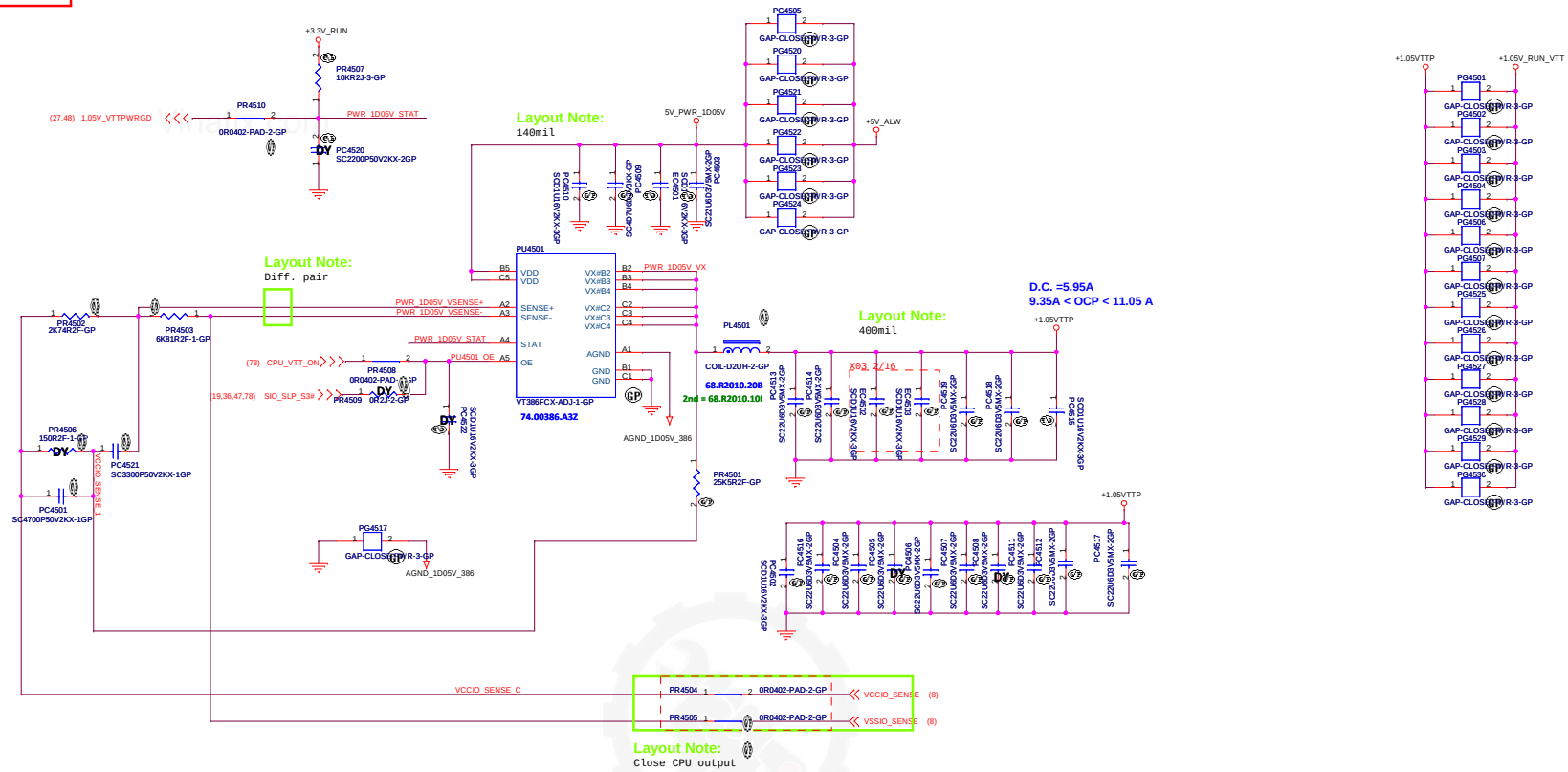
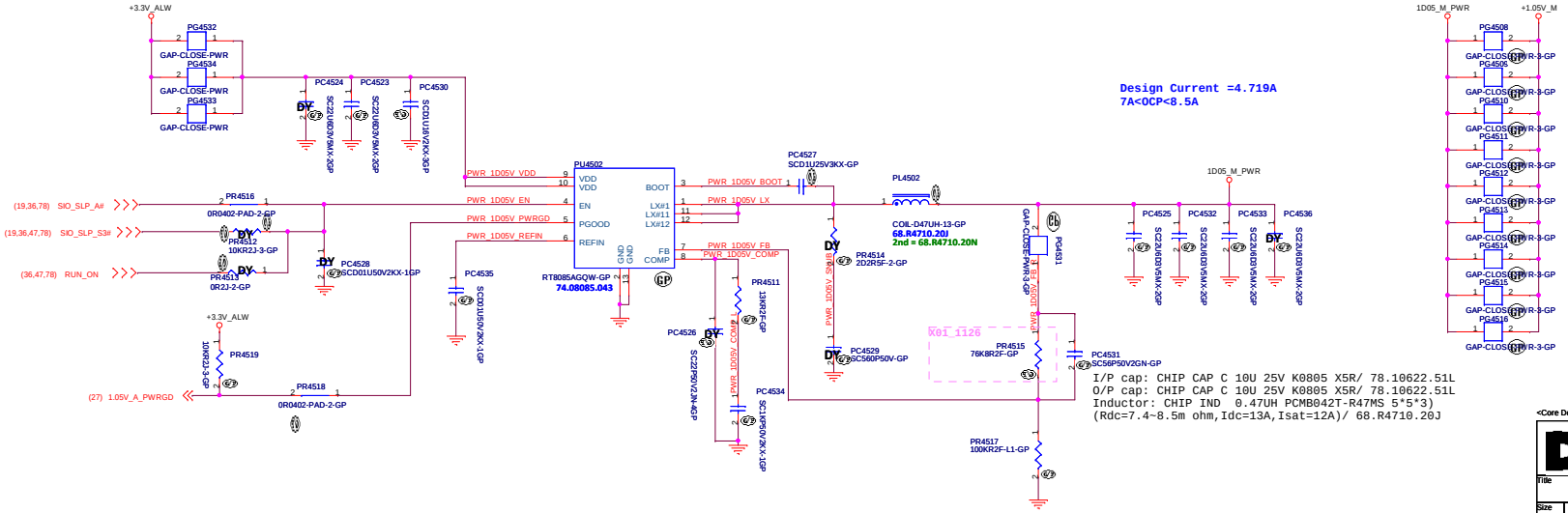
SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
O/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.20UH PCMB053T-R20MS(5*5*3)(Rdc=3.5~3.9m ohm,Idc=21A,Isat=14.5A)/68.R2010.20B



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
O/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.47UH PCMB042T-R47MS 5*5*3)
(Rdc=7.4~8.5m ohm,Idc=13A,Isat=12A)/ 68.R4710.20J

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D05V_PCH & VCCP_CPU

Size: A2 | Document Number: Austin 13 | Rev: A00

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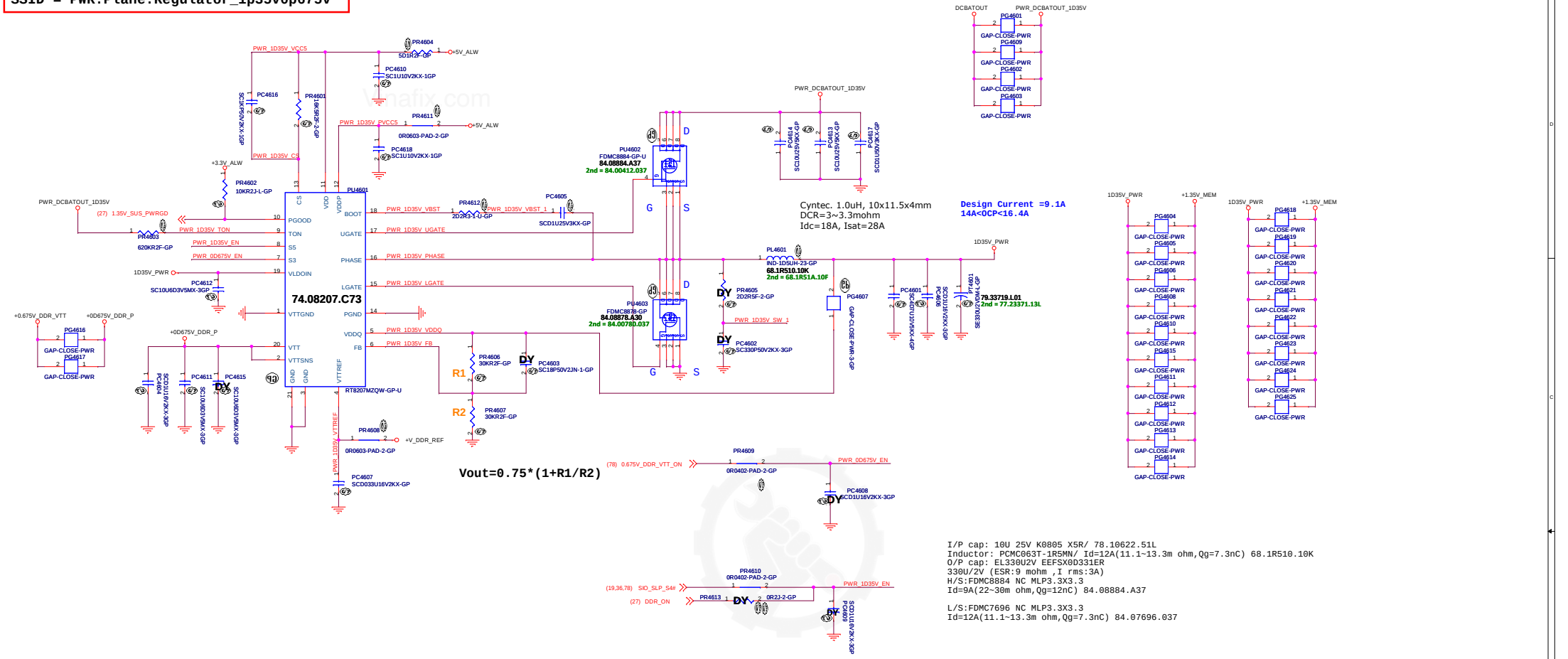
SSID = PWR.Plane.Regulator_1p35v0p675v



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: PCMC063T-1R5MN/ Id=12A(11.1~13.3m ohm,Qg=7.3nC) 68.1R510.10K
O/P cap: EL330U2V EEFSX0D331ER
330U/2V (ESR:9 mohm ,I rms:3A)
H/S:FDMC8884 NC MLP3.3X3.3
Id=9A(22~30m ohm,Qg=12nC) 84.08884.A37

L/S:FDMC7696 NC MLP3.3X3.3
Id=12A(11.1~13.3m ohm,Qg=7.3nC) 84.07696.037

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT385_1D5V_S3/RT9026_0D75V_S0

Size: A2 | Document Number: Austin 13 | Rev: A00

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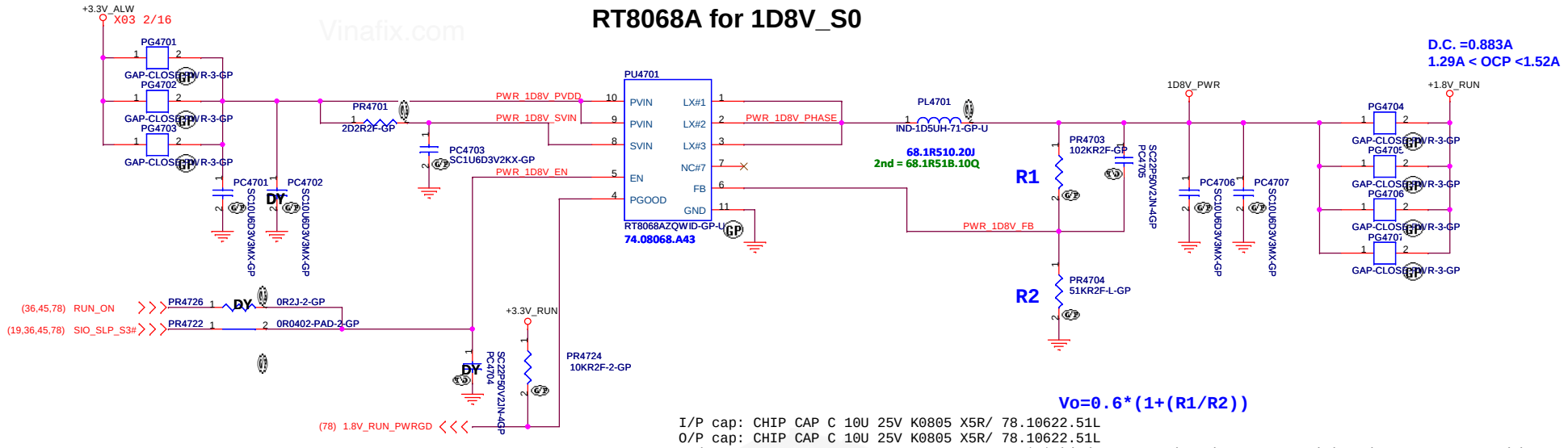
SSID = PWR.Plane.Regulator_1p8v

RT8068A for 1D8V_S0

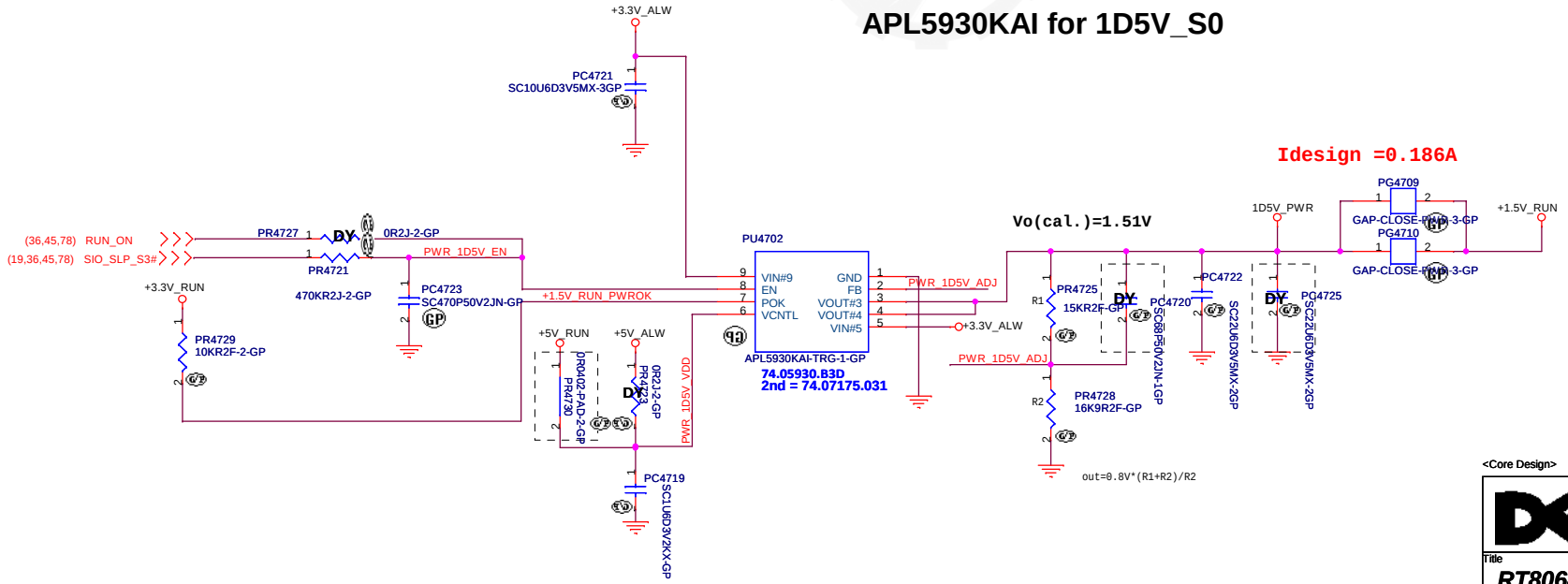


Vo=0.6*(1+(R1/R2))

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
O/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.5UH PCMB042T-1R5MS4*4*2)(Rdc=38~46m ohm,Idc=4A,Isat=6A)ohm,Idc=21A,Isat=14.5A)/
68.1R510.20J

SSID = PWR.Plane.Regulator_1p5v

APL5930KAI for 1D5V_S0



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8068A_1D8V_S0/APL5930_1D5V

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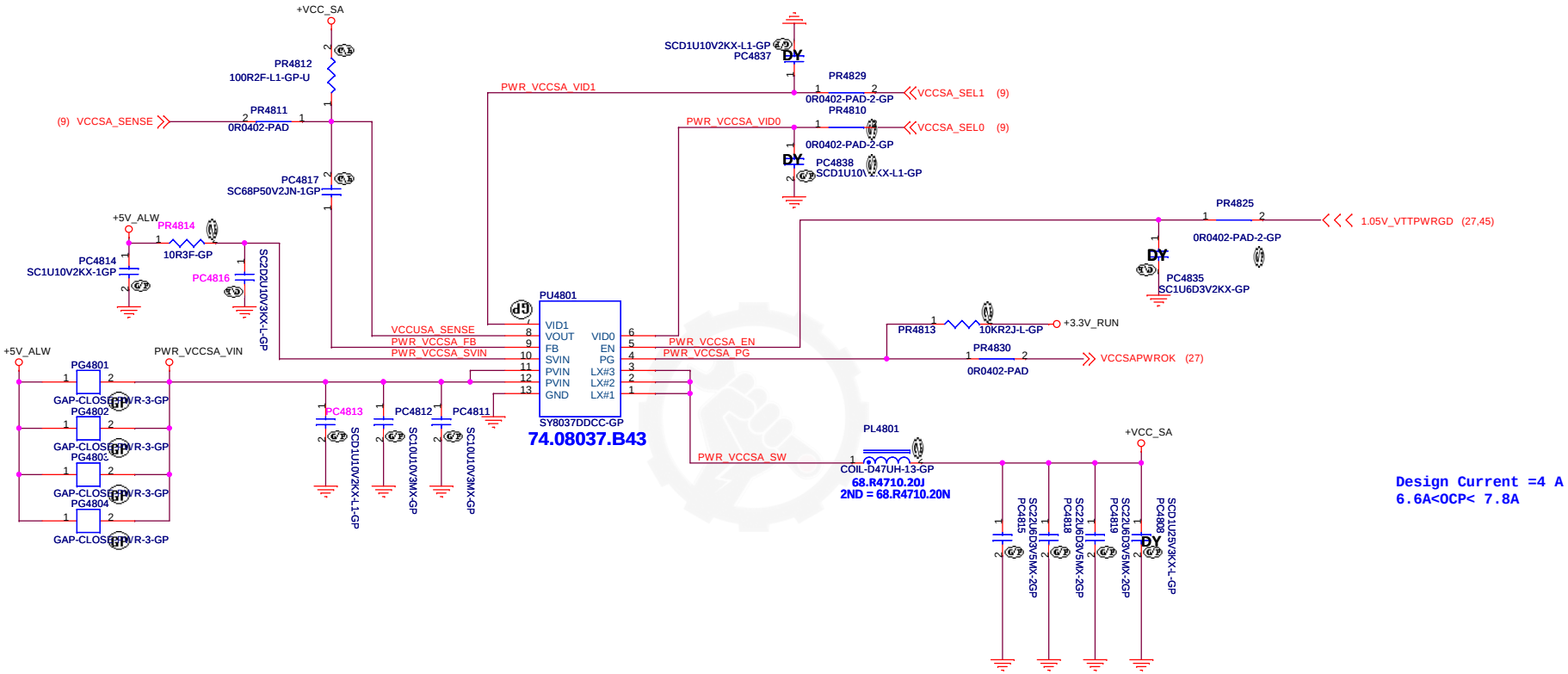
Date: Tuesday, February 26, 2013 Sheet 47 of 106

SSID = PWR.Plane.Regulator_vccsa



Design Current =4 A
6.6A<OCP< 7.8A

VID0	VID1	VCCSA ULV
L	L	0.9V
L	H	0.85V
H	L	0.775V
H	H	0.75V

<Core Design>

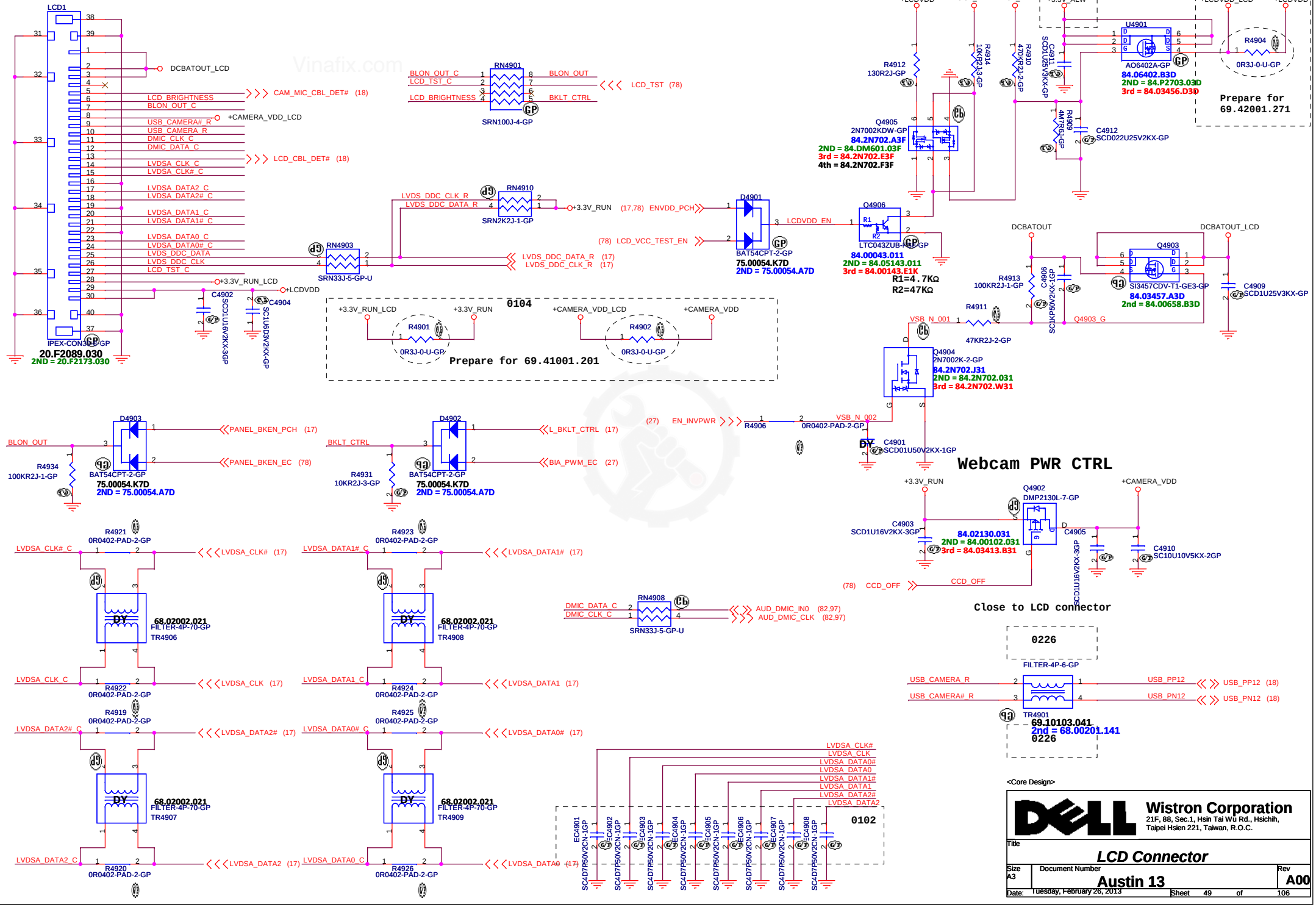
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SY8037DDCC_VCCSA

Size: A3 | Document Number: Austin 13 | Rev: A00

Date: Tuesday, February 26, 2013 | Sheet 48 of 106

SSID = VIDEO



<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	LCD Connector
Size A3	Document Number: Austin 13
Rev	A00
Date: Tuesday, February 26, 2013	Sheet 49 of 106

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<Core Design>

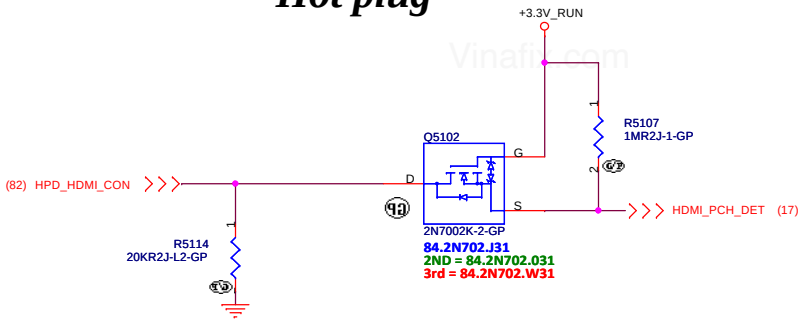
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT		
Size: A3	Document Number: Austin 13	Rev: A00
Date: Tuesday, February 26, 2013	Sheet 50 of 106	

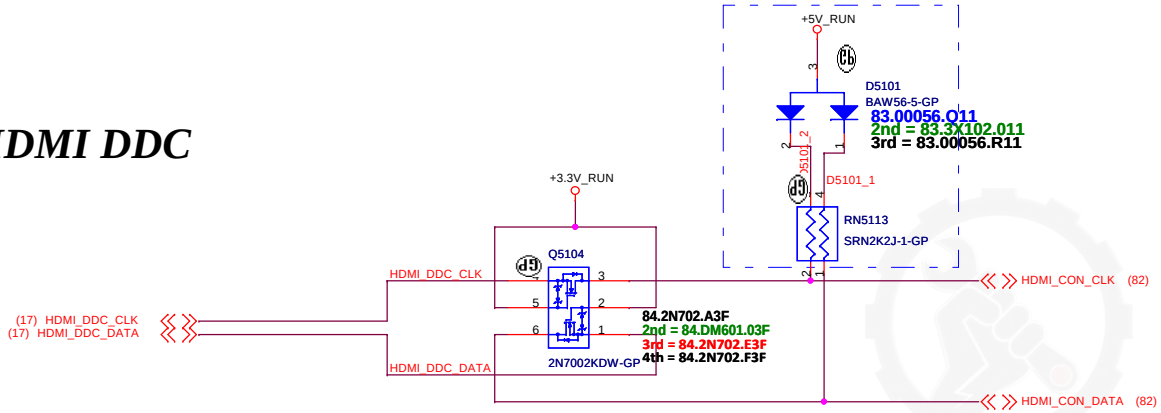
SSID = VIDEO

HDMI & HDMI CONNECTOR

Hot plug



HDMI DDC



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

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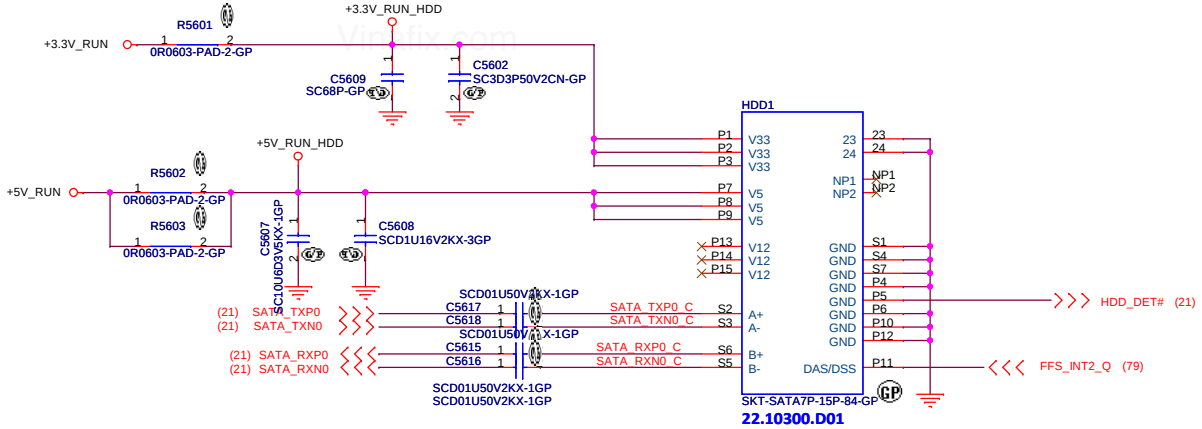
SSID = SATA

SATA HDD Connector



Pin name	Function
S1	Ground
S2	A+
S3	A-
S4	Ground
S5	B-
S6	B+
S7	Ground
P1	3.3V power
P2	3.3V power
P3	3.3V power
P4	Ground
P5	Ground
P6	Ground
P7	5V power
P8	5V power
P9	5V power
P10	Ground
P11	Reserved
P12	Ground
P13	12V power
P14	12V power
P15	12V power

Reserve for FFS INT pin

<Core Design>

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Title: ***HDD/ODD***

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Date: Tuesday, February 26, 2013 Sheet 56 of 106

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<Core Design>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ESATA		
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Date: Tuesday, February 26, 2013	Sheet 57 of 106	

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Magnetic/RJ45

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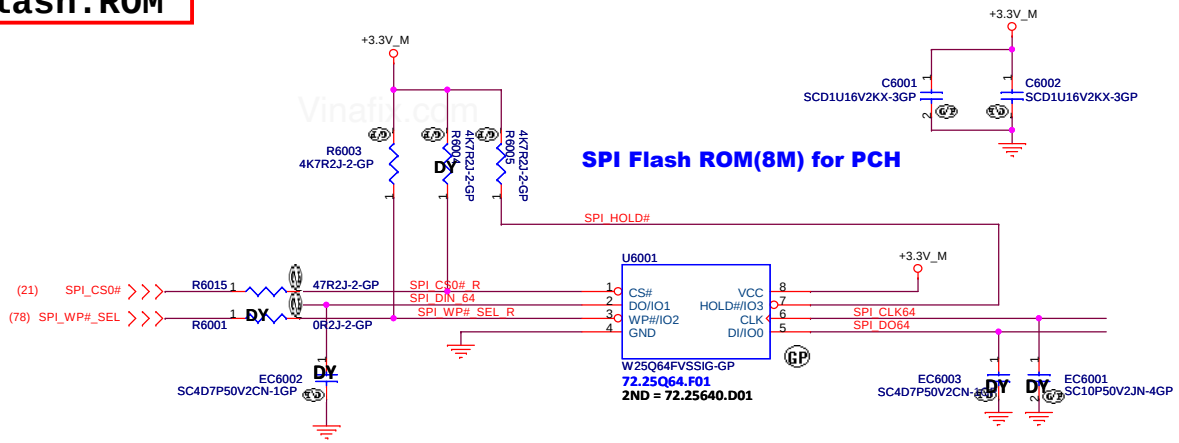
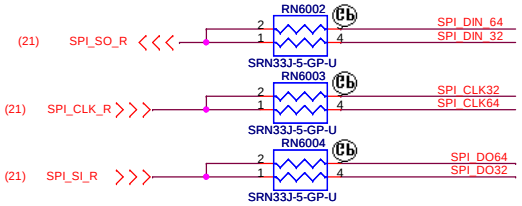
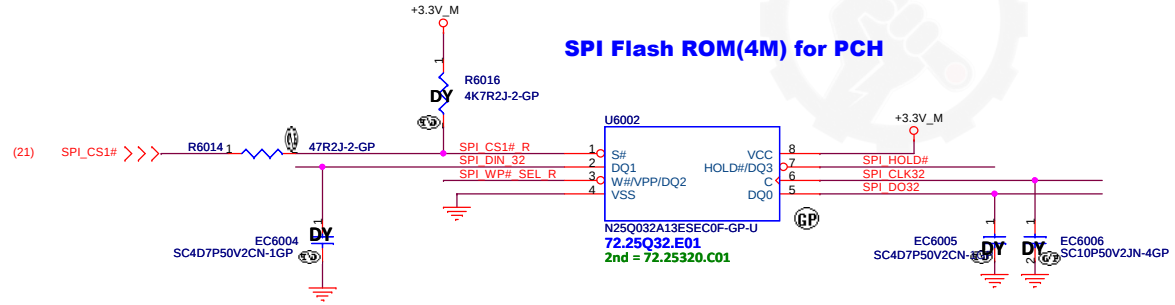
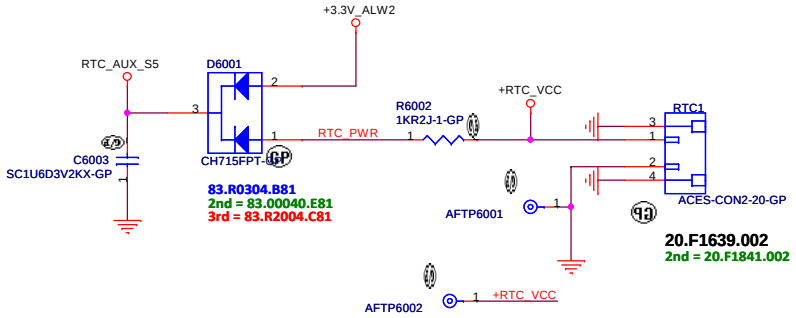
SSID = Flash.ROM







SSID = RBATT



<Core Design>

Wistron Corporation
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Title: Flash/RTC

Size: A3 | Document Number: Austin 13 | Rev: A00

Date: Tuesday, February 26, 2013 | Sheet 60 of 106

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

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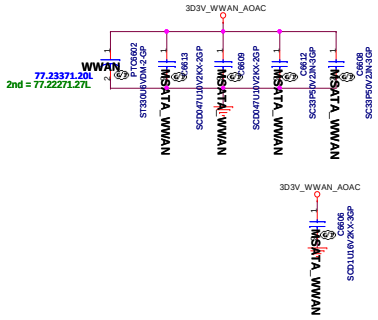
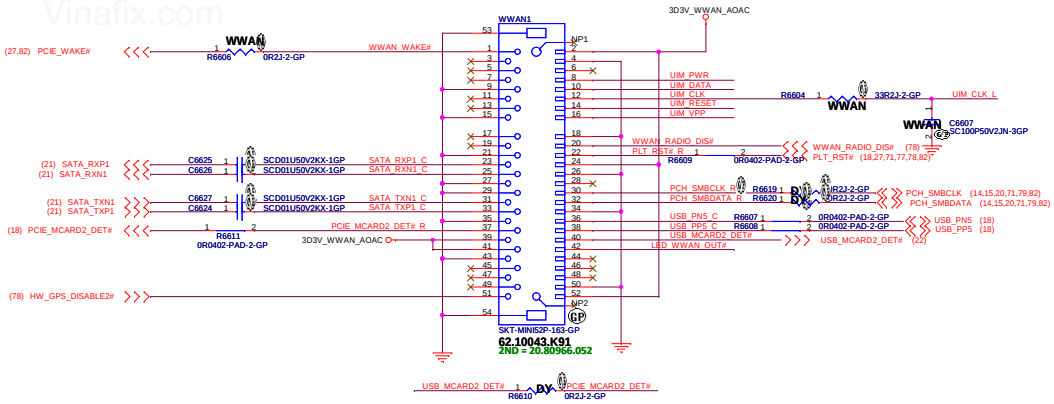
Mini Card Connector(WWAN)

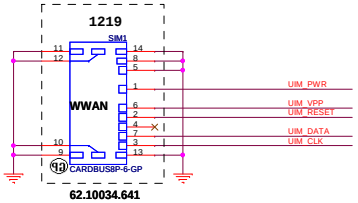
SSID = WWAN

Place near MINI Card CONN

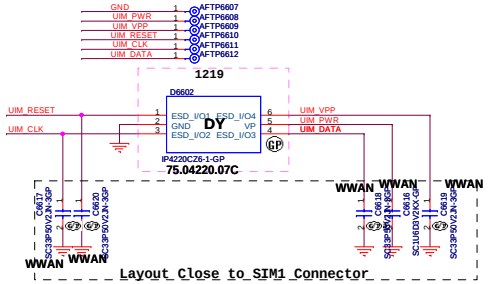


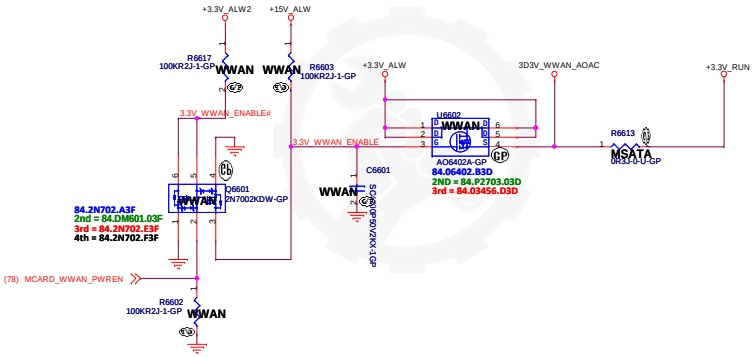


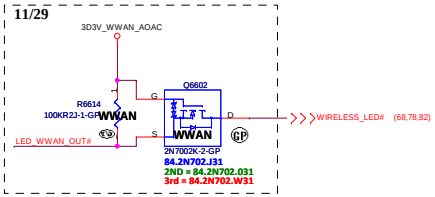
Micro SIM CARD	
Pin No.	NAME
C1	VCC
C2	RST
C3	CLK
C4	Reserved
C5	GND
C6	VPP
C7	I/O
C8	Reserved

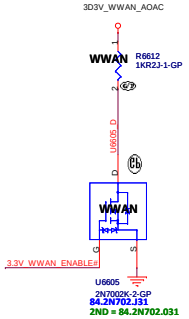


DATA and CLK need keep away at least 12mil









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WWAN CONN/SIM SOCKET

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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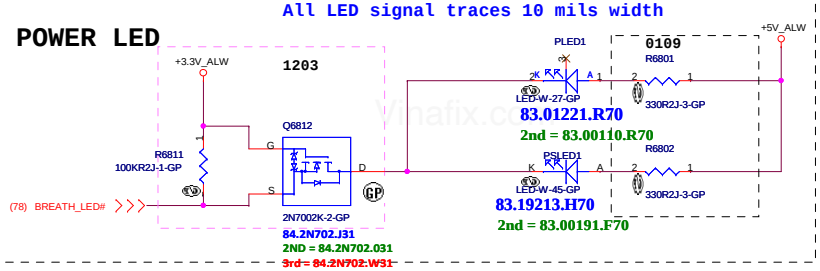
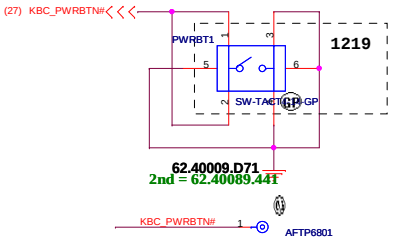
SSID = User.Interface

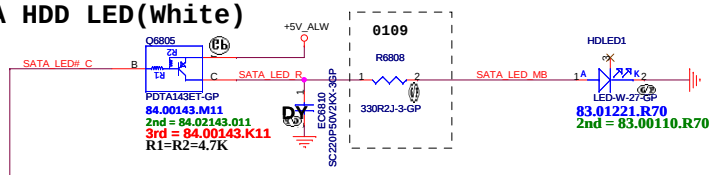
FRONT POWER LED

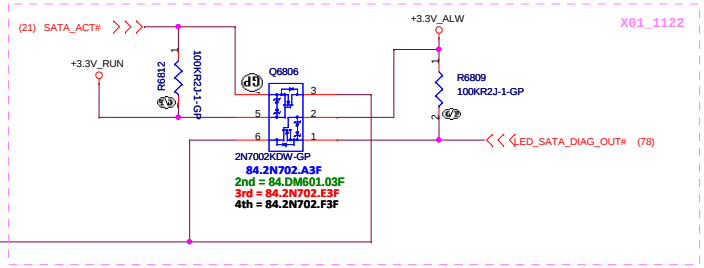
All LED signal traces 10 mils width





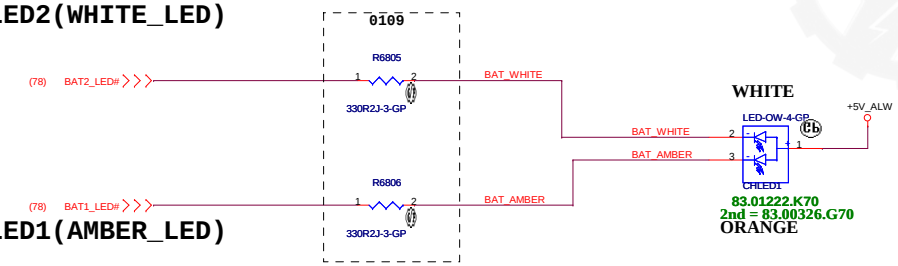
SATA HDD LED(White)



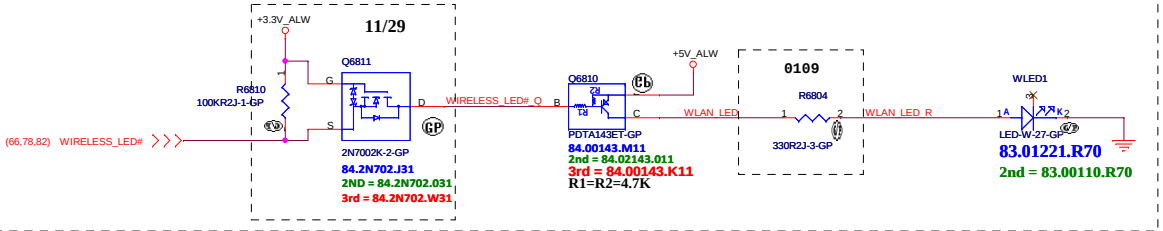


Battery LED2(WHITE_LED)

Battery LED1(AMBER_LED)



WLAN_LED



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bard/Power Button

Size: Custom | Document Number: Austin 13 | Rev: A00

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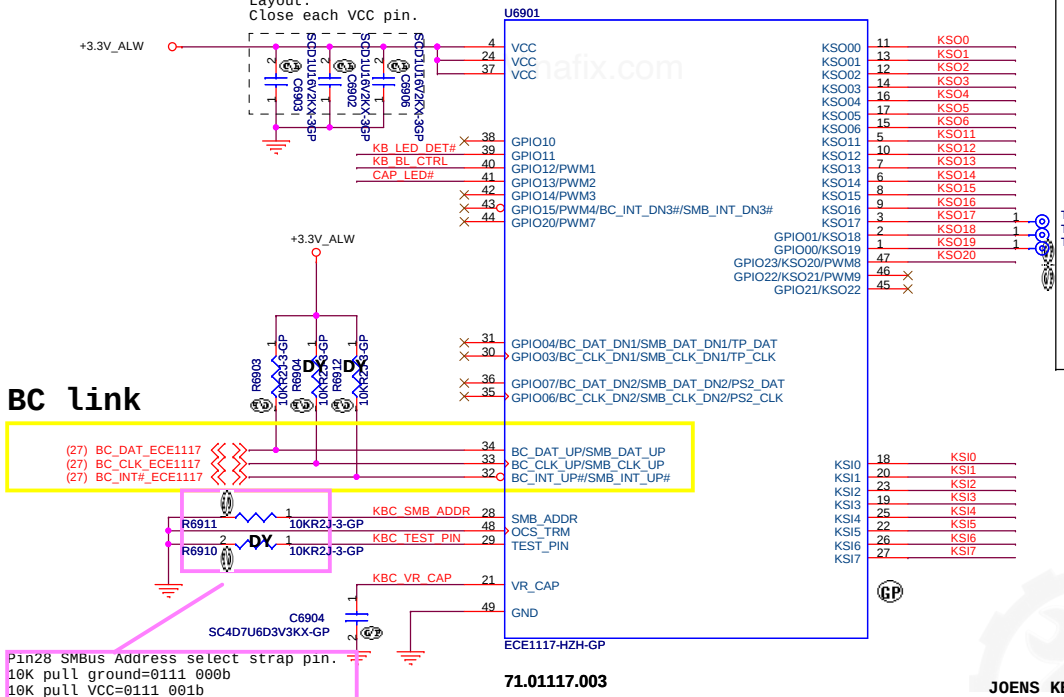
SSID = KBC

KBC SMSC ECE1117

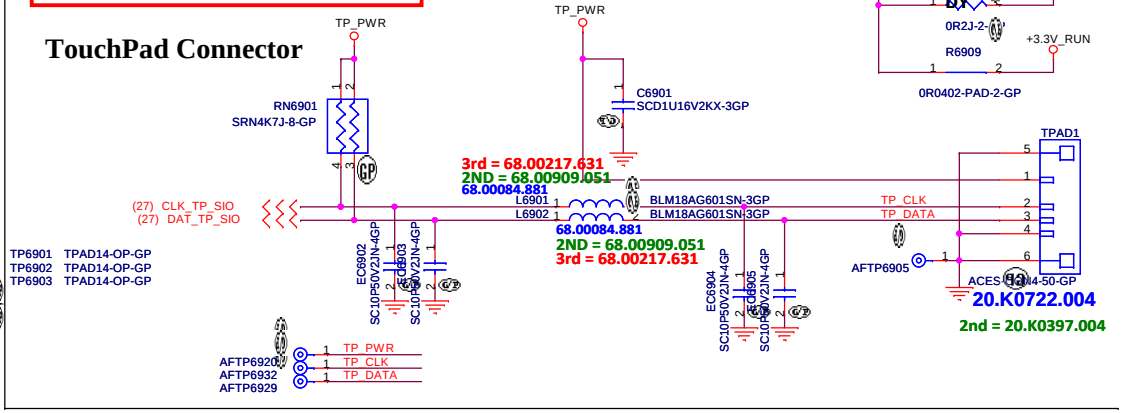


BC link

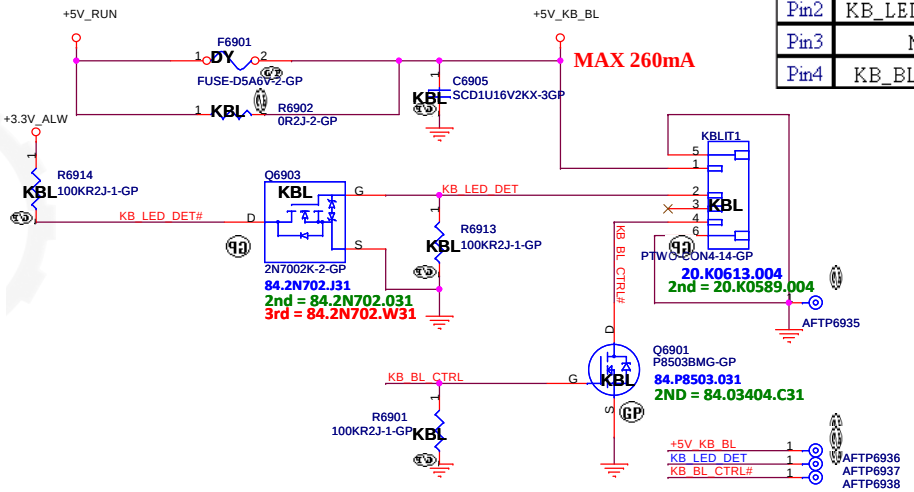
71.01117.003

SSID = Touch.Pad

TouchPad Connector

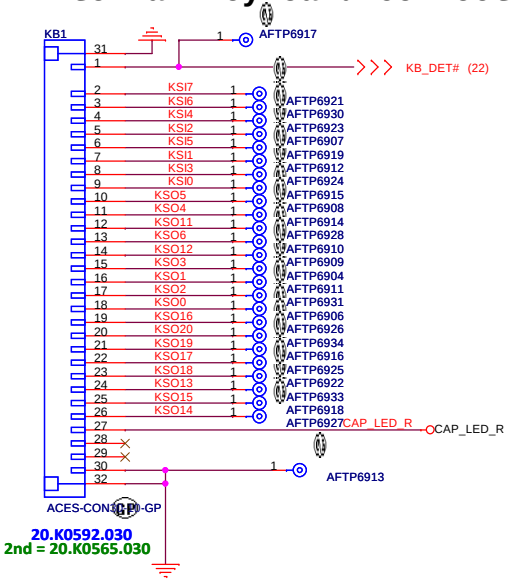


KB Backlight Connector



MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#

Internal KeyBoard Connector

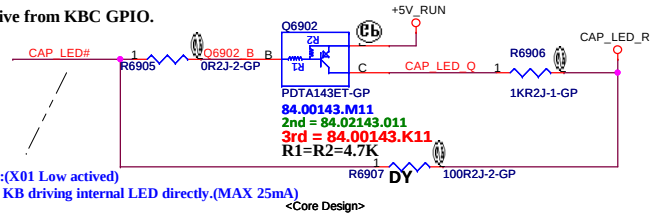


PIN No.	Description
1	Diag_Loop=GPIO_1(TPC)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND

JOENS KB

CAP LED CONTROL

High Active from KBC GPIO.



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size: A3 | Document Number: Austin 13 | Rev: A00

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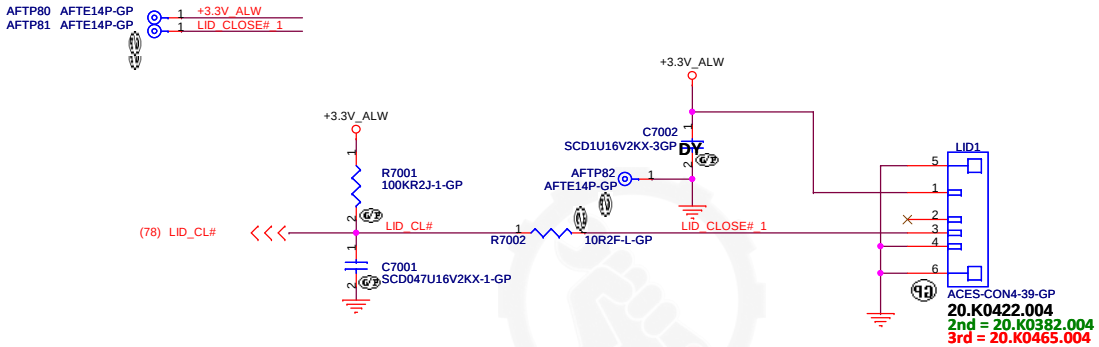
SSID = User.interface



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Hall Sensor

Size: A3 | Document Number: Austin 13 | Rev: A00

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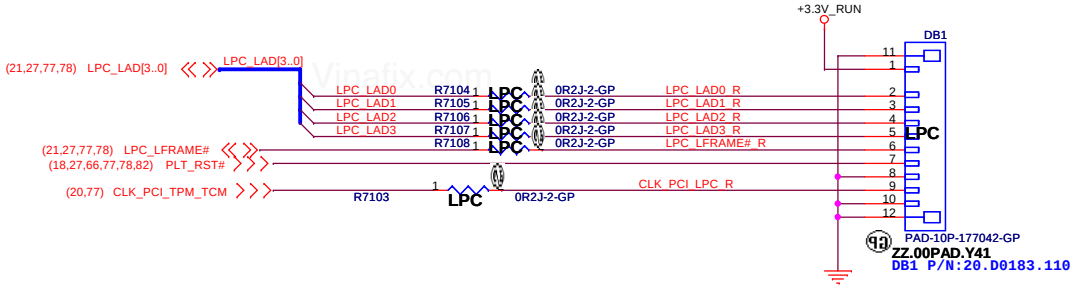
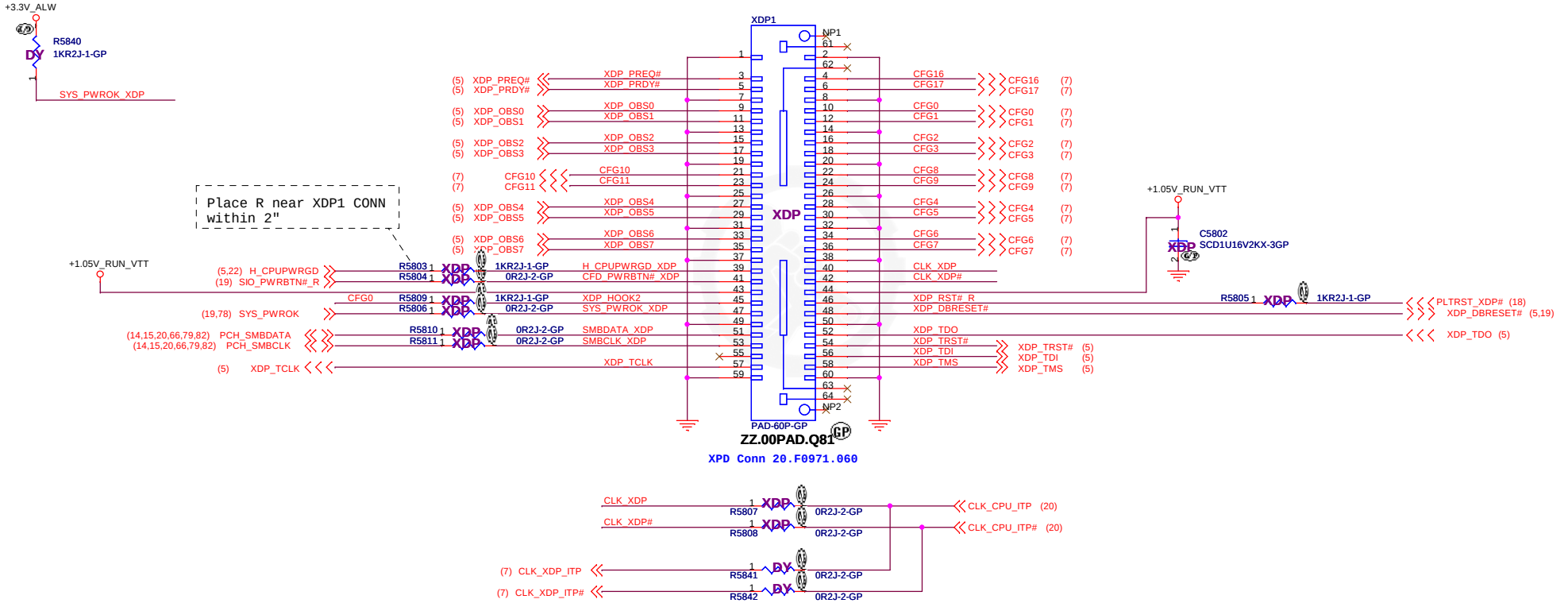
SSID = DEBUG PORT

Debug Connector



CPU XDP



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Dubug connector

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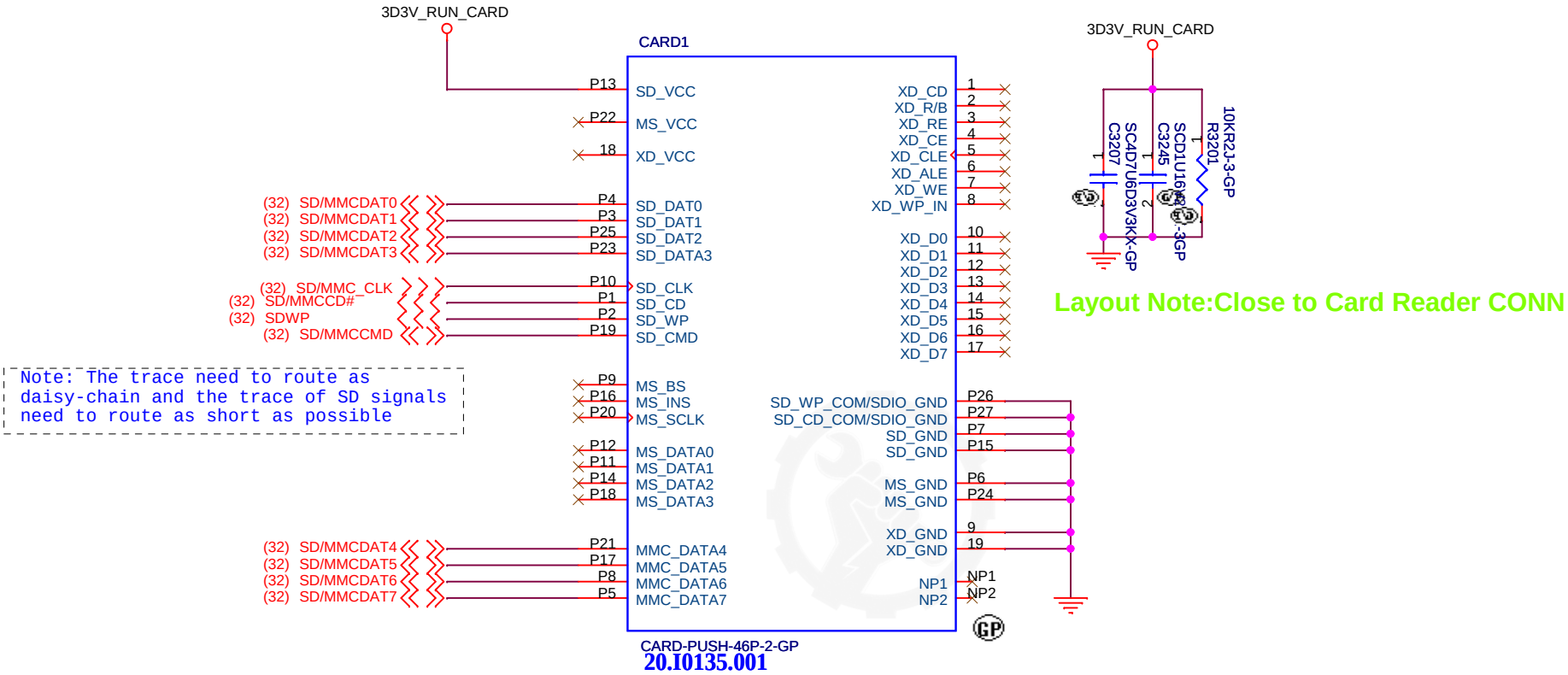
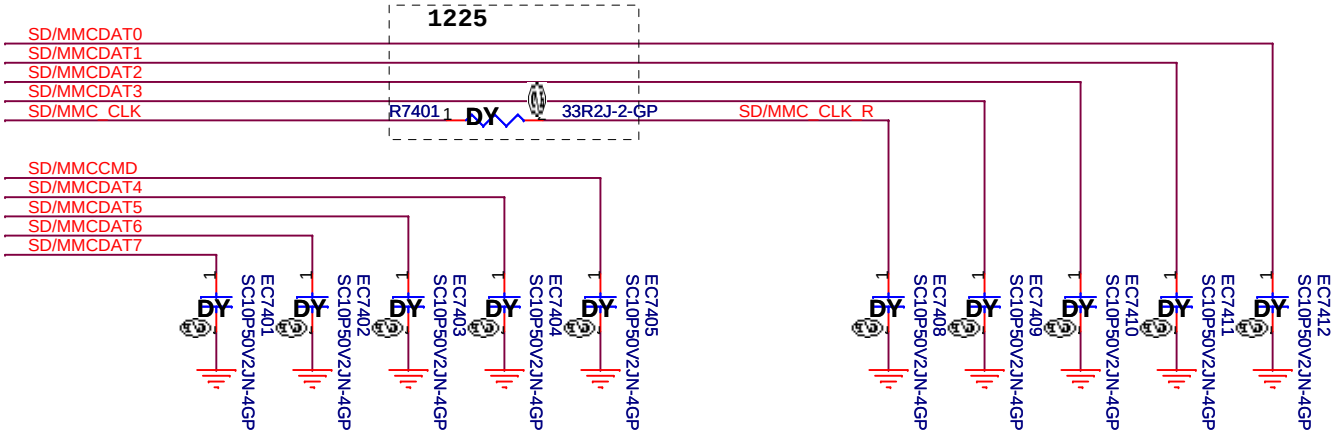
SD CONN

SD/MMC Card Connector



Note: The trace need to route as daisy-chain and the trace of SD signals need to route as short as possible

Layout Note:Close to Card Reader CONN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader CONN

Size	Document Number	Rev
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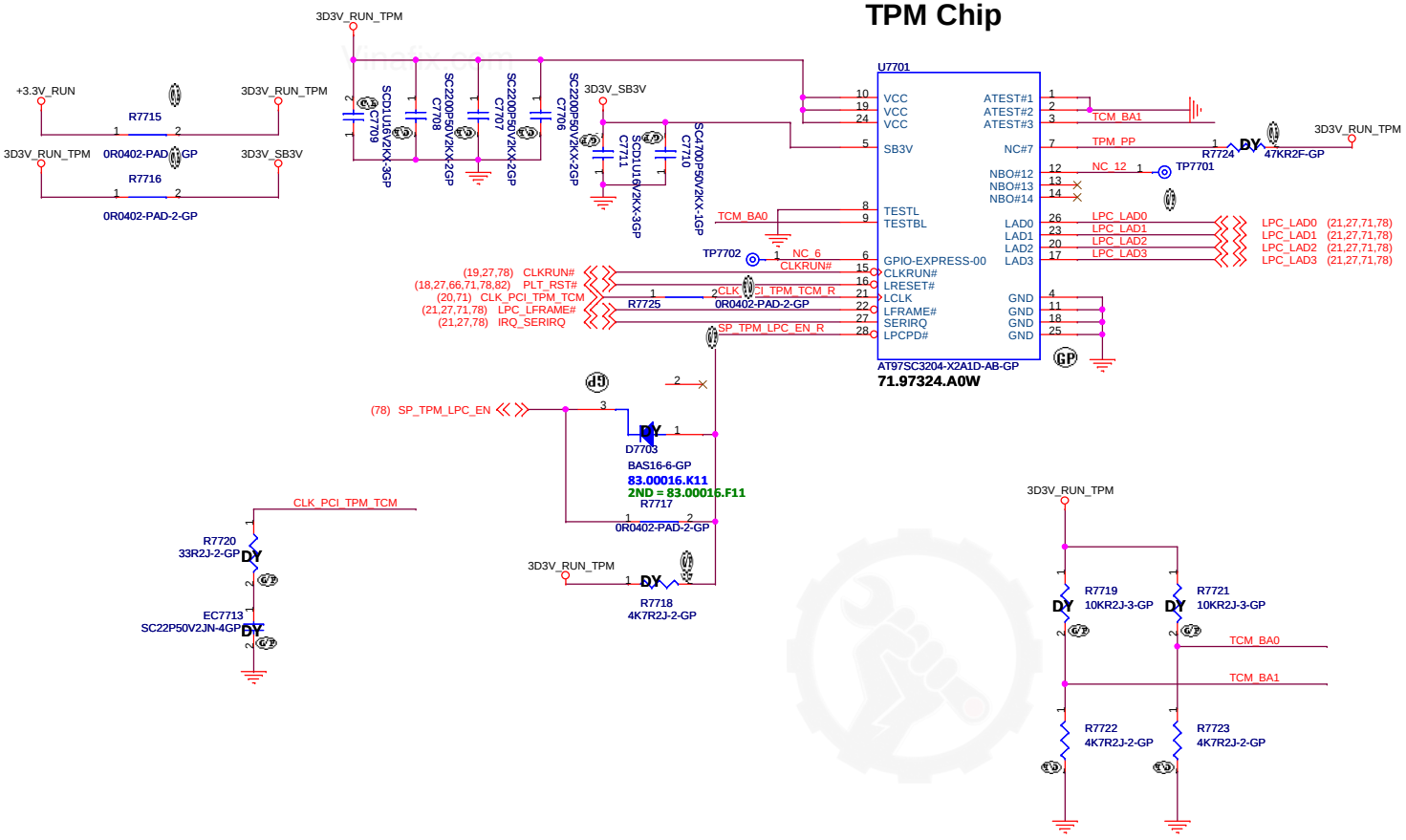
SSID = TPM

TPM Chip



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPM/TCM**

Size: Custom | Document Number: **Austin 13** | Rev: **A00**

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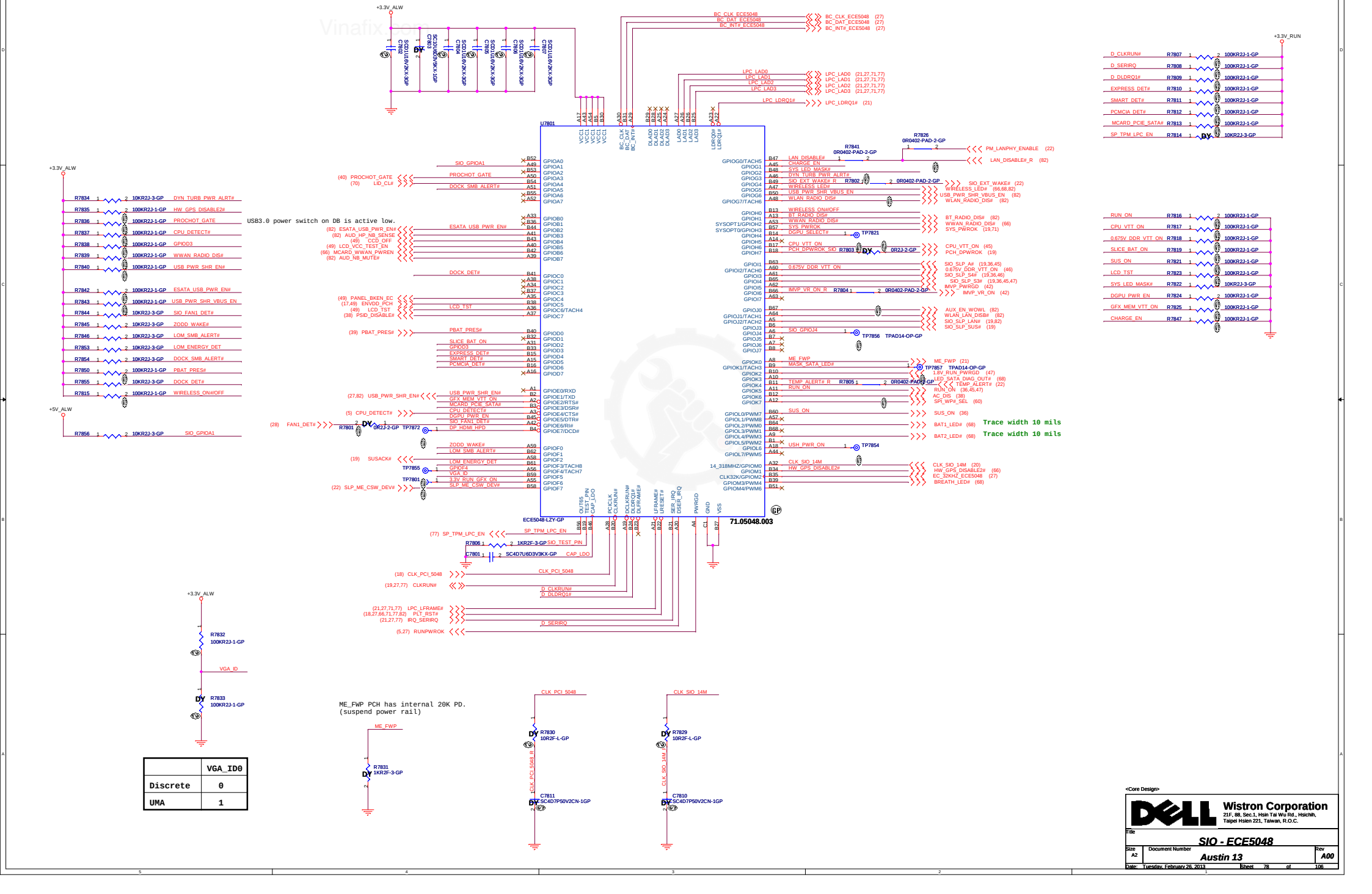
SSID = SIO



	VGA_ID0
Discrete	0
UMA	1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SIO - ECE5048

Size: A2 | Document Number: Austin 13 | Rev: A00

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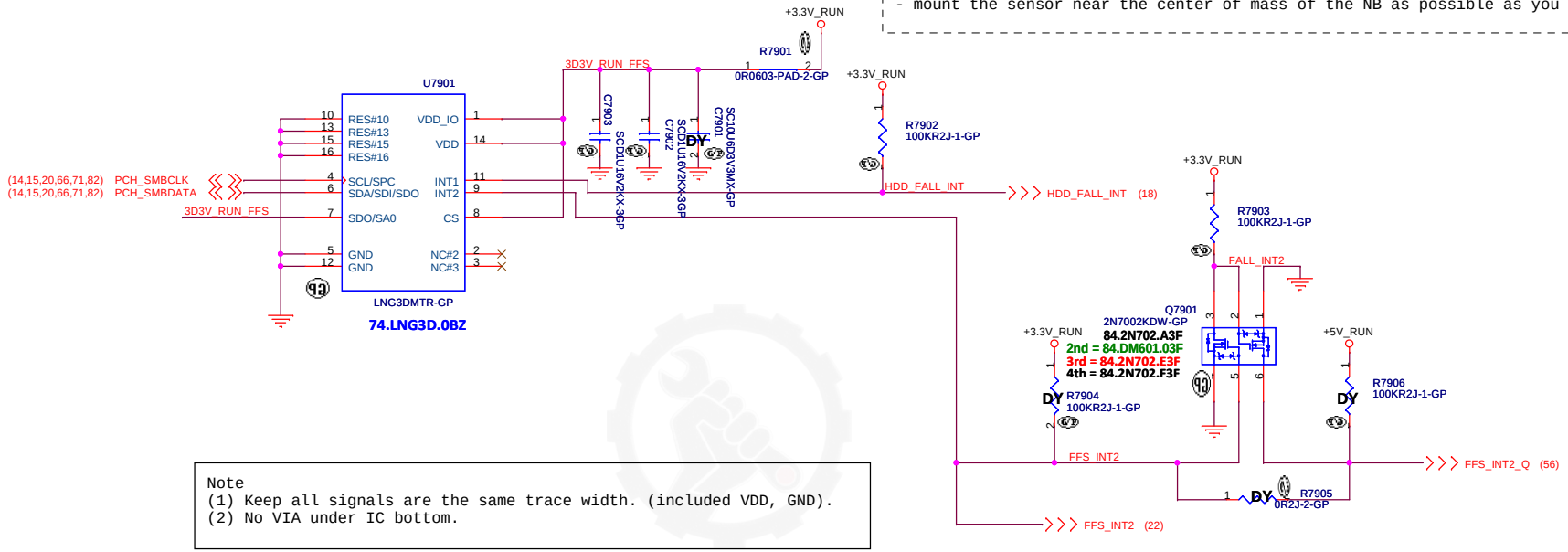
SSID = User.interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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Title	Free Fall Sensor	
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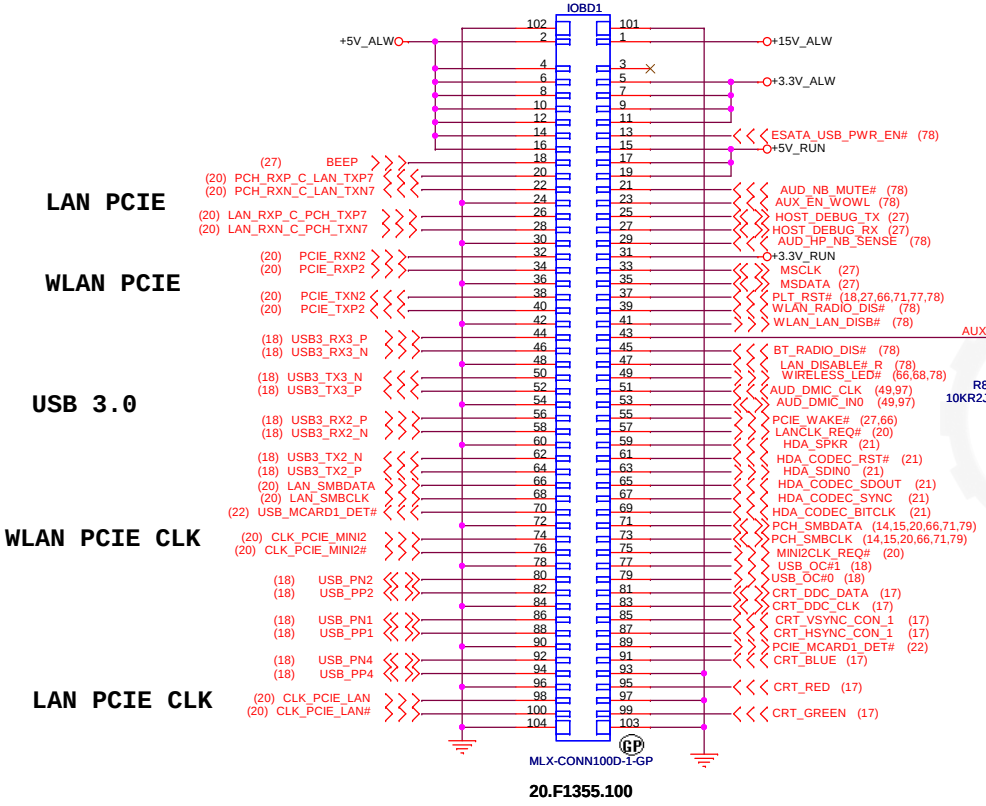
SSID = User.Interface

IO BD CONN



20.F1355.100

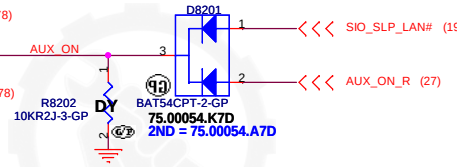
LAN PCIE

WLAN PCIE

USB 3.0

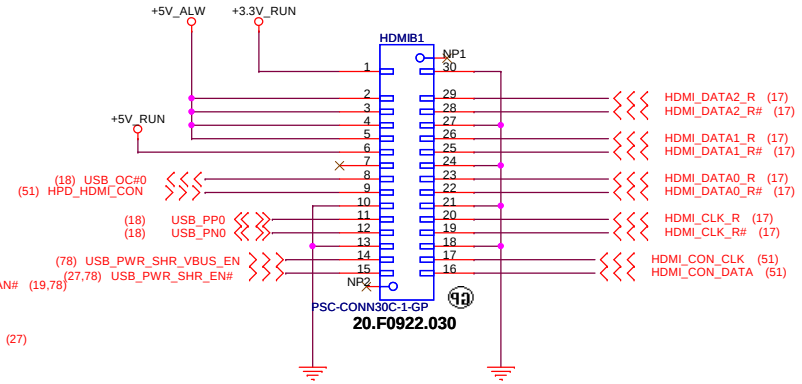
WLAN PCIE CLK

LAN PCIE CLK



CRT Bus

HDMI BD CONN



20.F0922.030

GND 18 pins
Power 17 pins

<Core Design>

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Title: IO Board Connector

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<Core Design>

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<Core Design>

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<Core Design>

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Title: *Reserved*

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<Core Design>

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Title: *Reverved*

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<Core Design>

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Title: *Reserved*

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<Core Design>

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H2 HOLE256R126-GP
H3 HOLE256R126-GP
H4 HOLE355X355R126-GP
H5 HT10X10BE10R32-L-5-GP
H6 HOLE197R166-1-GP
H7 HOLE256R126-GP
H8 HOLE197R166-1-GP
H9 HOLE197R166-1-GP
H10 HOLE256R126-GP
H11 HOLE197R166-1-GP
ZZ.00PAD.V71

H12 HOLE256R126-GP
H13 HOLE355X355R126-GP
H14 HOLE355X355R126-GP
H15 HOLE237R95-GP

H16 HOLE
H17 HOLE
H18 HOLE
H19 HOLE
H20 HOLE

H16,H17 GNDPADSR197_99-S
H18,H19,H20 GNDPADS79X119-NP

34.4T025.001
SPR1 SPRING-52-GP
34.4T025.001
SPR2 SPRING-52-GP DY
34.4H602.001
SPR3 SPRING-64-GP DY
SPR4 SPRING-9-GP
34.49U23.001

X01_1219
BOM need to stuff 34.49U23.001

EMI Request

AUD_DMIC_CLK
AUD_DMIC_IN0
R9701 47R2J-2-GP DY
R9702 47R2J-2-GP DY
AUD_DMIC_CLK
AUD_DMIC_IN0
EC9719 SCD1U16V2KX-3GP DY
EC9720 SCD1U16V2KX-3GP DY

EC9738 SCD1U16V2KX-3GP DY
+3.3V_RUN +5V_ALW
EC9740 SCD1U25V2KX-GP DY
+5V_ALW +DC_IN
EC9741 SCD1U25V2KX-GP DY
+5V_ALW DCBATOUT

(49,82) AUD_DMIC_CLK
(49,82) AUD_DMIC_IN0
(17,49) LVDS_DDC_DATA_R
(17,49) LVDS_DDC_CLK_R

RF Request

+1.35V_MEM: EC9727 EC9734 EC9749 EC9750 EC9751 EC9752 SCD1U16V2KX-3GP DY
+1.05V_RUN_VTT: EC9724 EC9725 EC9726 SCD1U16V2KX-3GP DY
+5V_RUN: EC9730 EC9731 EC9732 SCD1U16V2KX-3GP DY
+1.35V_MEM: EC9753 EC9754 EC9755 EC9756 SCD1U16V2KX-3GP DY
+1.05V_M: EC9757 EC9758 EC9759 EC9760 SCD1U16V2KX-3GP DY
EC9733 +3.3V_RUN +5V_RUN SCD1U16V2KX-3GP DY
+5V_ALW: EC9766 EC9767 EC9768 EC9769 EC9770 EC9771 EC9772 EC9773 EC9774 EC9775 EC9776 EC9777 EC9778 EC9779 EC9780 EC9728 EC9729 SCD1U16V2KX-3GP DY
+3.3V_ALW: EC9781 EC9782 EC9783 EC9784 EC9785 EC9786 EC9787 EC9735 SCD1U16V2KX-3GP DY
+1.05V_RUN_VTT: EC9761 EC9762 SCD1U16V2KX-3GP DY

<Core Design>

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Title: UNUSED PARTS/EMI Capacitors
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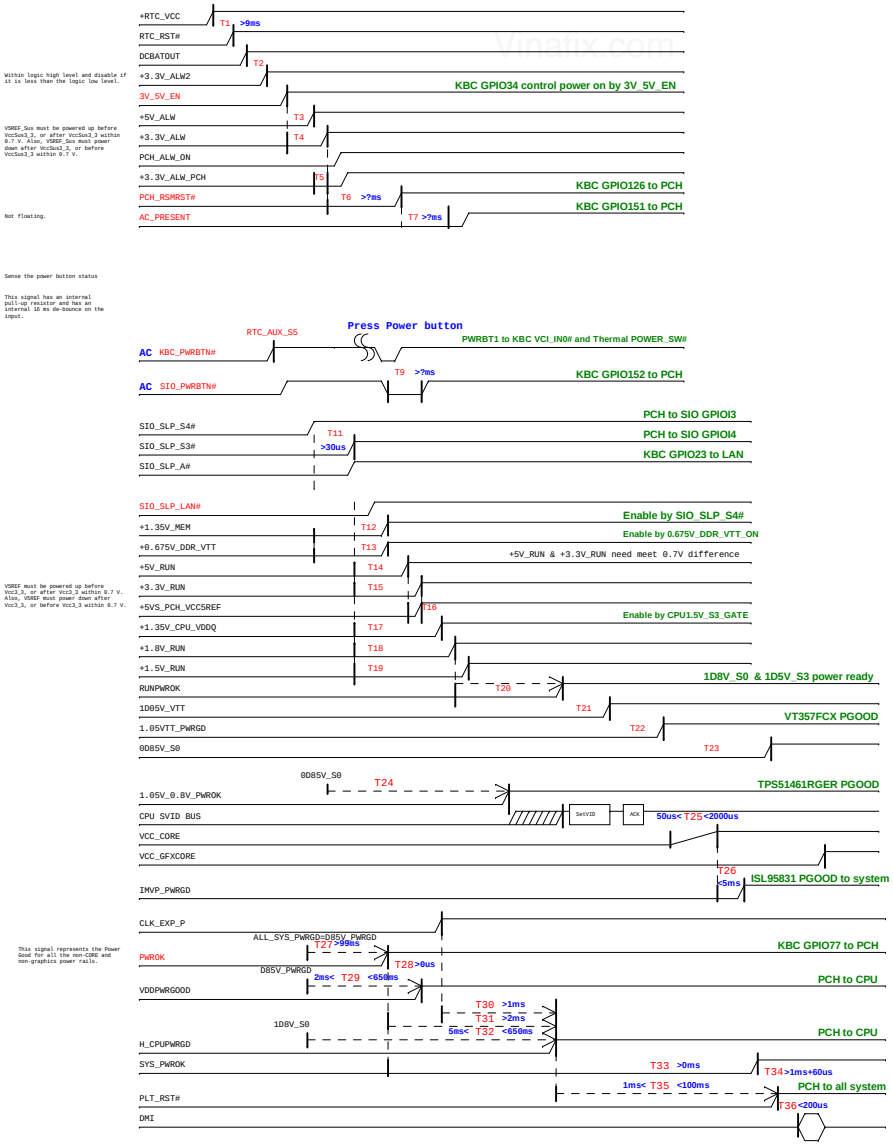
Cheif River Platform Power Sequence

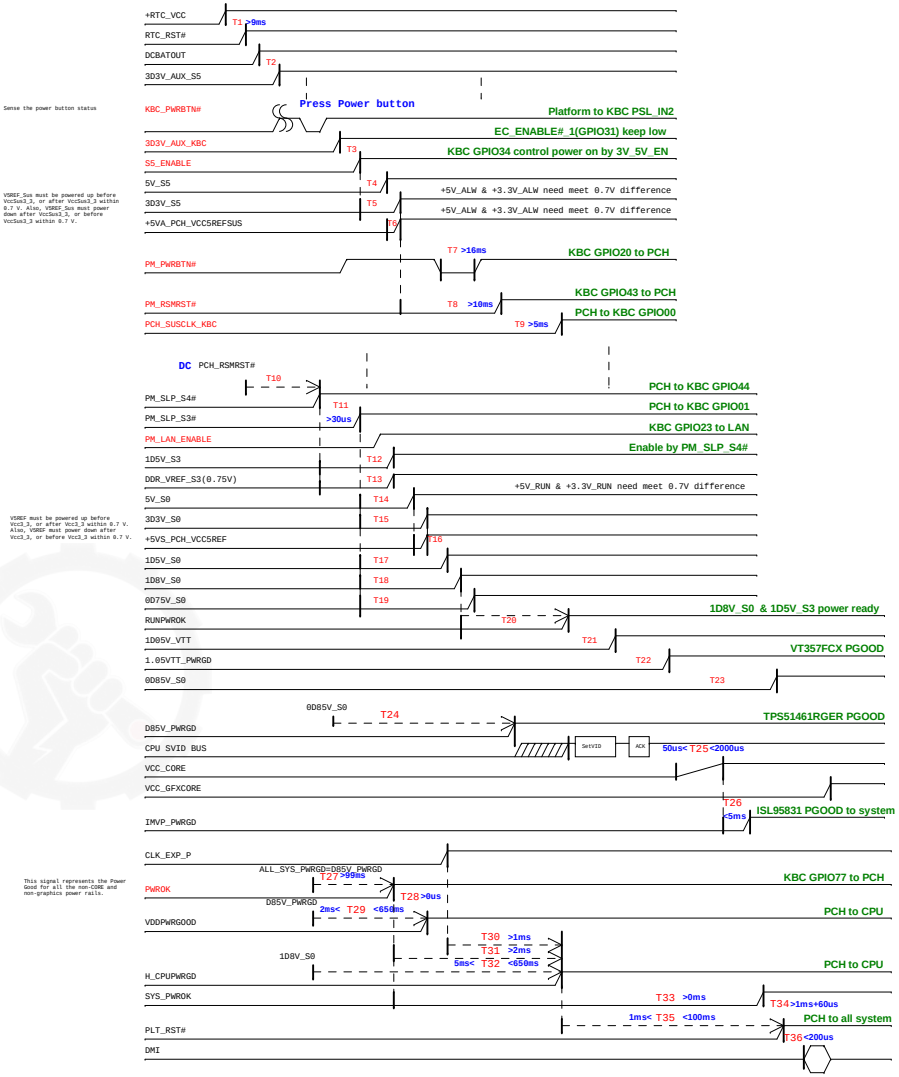
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



<Core Design>

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Title: Power Sequence

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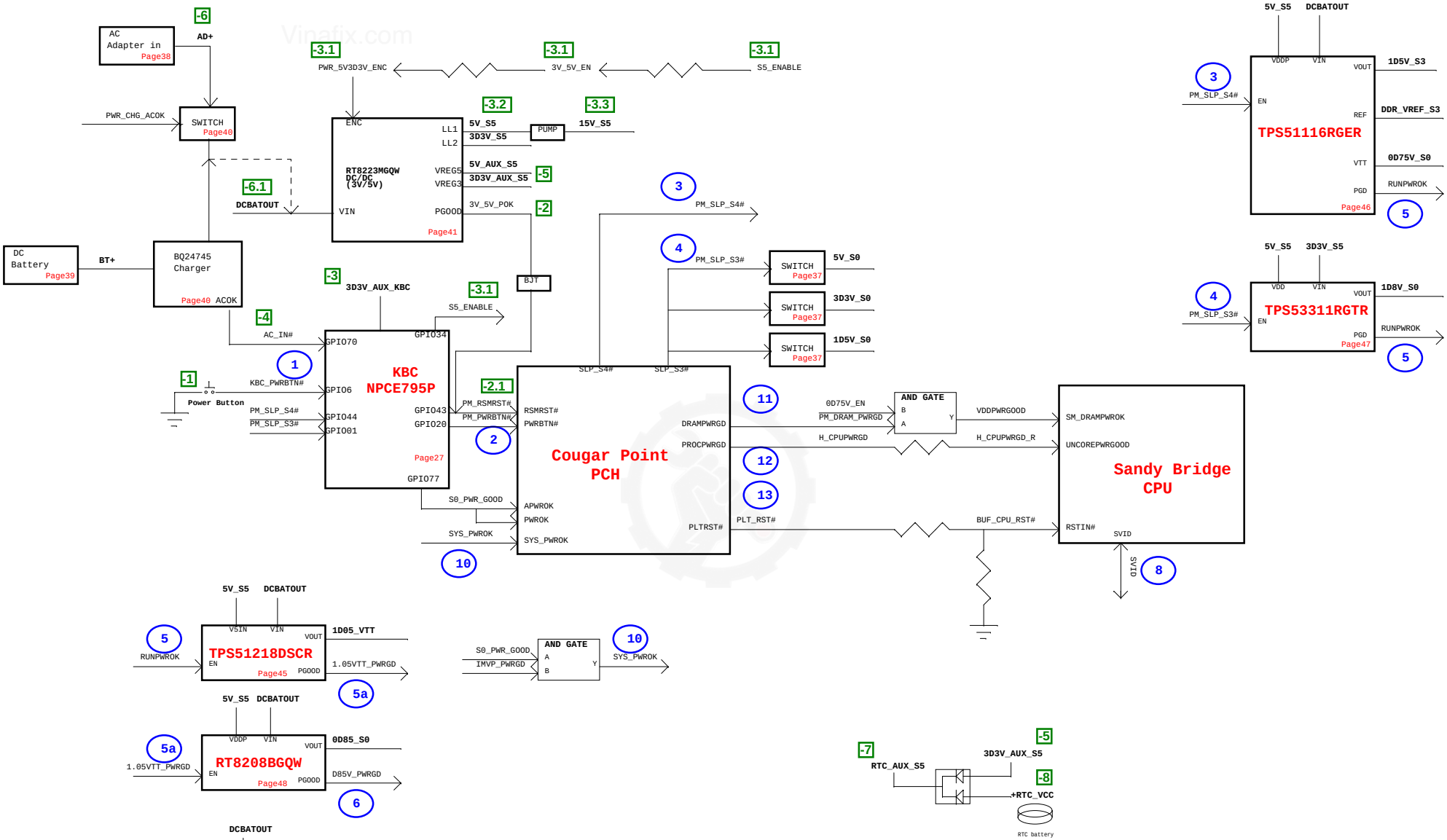
Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13

<Core Design>
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Title	Power Up Sequence Diagram	
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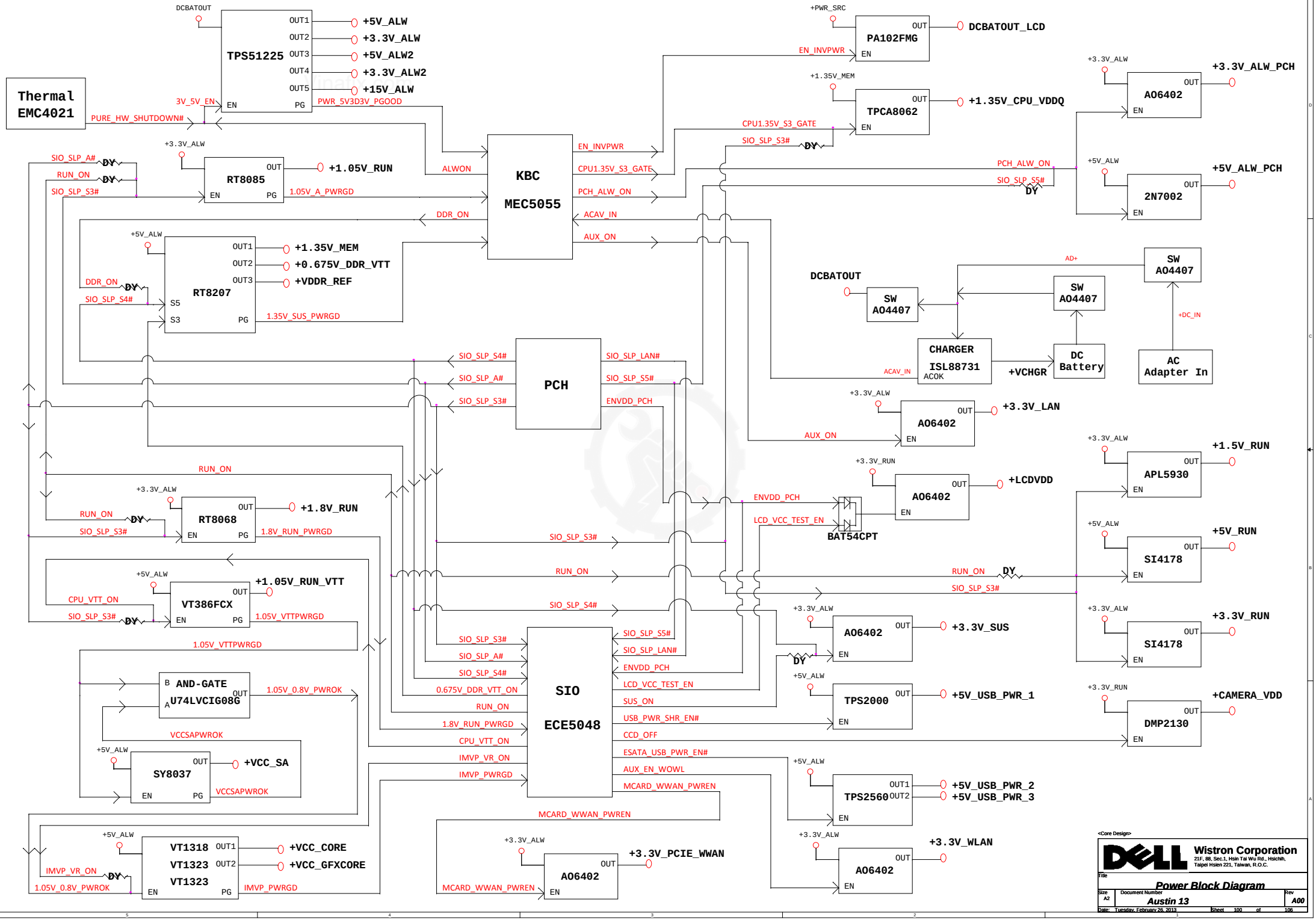
Thermal EMC4021
TPS51225
DCBATOUT
OUT1 +5V_ALW
OUT2 +3.3V_ALW
OUT3 +5V_ALW2
OUT4 +3.3V_ALW2
OUT5 +15V_ALW
3V_5V_EN
PWR_5V3D3V_PGOOD
PURE_HW_SHUTDOWN#
KBC MEC5055
RT8085 +1.05V_RUN
ALWON
1.05V_A_PWRGD
SIO_SLP_A#
RUN_ON
SIO_SLP_S3#
DDR_ON
RT8207 +1.35V_MEM +0.675V_DDR_VTT +VDDR_REF
SIO_SLP_S4#
1.35V_SUS_PWRGD
PCH
SIO_SLP_LAN#
SIO_SLP_S5#
ENVDD_PCH
RT8068 +1.8V_RUN
1.8V_RUN_PWRGD
VT386FCX +1.05V_RUN_VTT
CPU_VTT_ON
1.05V_VTTPWRGD
AND-GATE U74LVCIG08G
1.05V_0.8V_PWROK
SY8037 +VCC_SA
VCCSAPWROK
VT1318 VT1323 VT1323 +VCC_CORE +VCC_GFXCORE
IMVP_VR_ON
IMVP_PWRGD
SIO ECE5048
0.675V_DDR_VTT_ON
RUN_ON
1.8V_RUN_PWRGD
CPU_VTT_ON
IMVP_VR_ON
IMVP_PWRGD
LCD_VCC_TEST_EN
SUS_ON
USB_PWR_SHR_EN#
CCD_OFF
ESATA_USB_PWR_EN#
AUX_EN_WOWL
MCARD_WWAN_PWREN
EN_INVPWR
CPU1.35V_S3_GATE
PCH_ALW_ON
ACAV_IN
AUX_ON
PA102FMG DCBATOUT_LCD
TPCA8062 +1.35V_CPU_VDDQ
AO6402 +3.3V_ALW_PCH
2N7002 +5V_ALW_PCH
SW AO4407
CHARGER ISL88731 ACOK
DC Battery
AC Adapter In
+VCHGR
ACAV_IN
AD+
+DC_IN
AO6402 +3.3V_LAN
AO6402 +LCDVDD
BAT54CPT
APL5930 +1.5V_RUN
SI4178 +5V_RUN
SI4178 +3.3V_RUN
AO6402 +3.3V_SUS
TPS2000 +5V_USB_PWR_1
DMP2130 +CAMERA_VDD
TPS2560 +5V_USB_PWR_2 +5V_USB_PWR_3
AO6402 +3.3V_WLAN
AO6402 +3.3V_PCIE_WWAN
DY
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Power Block Diagram
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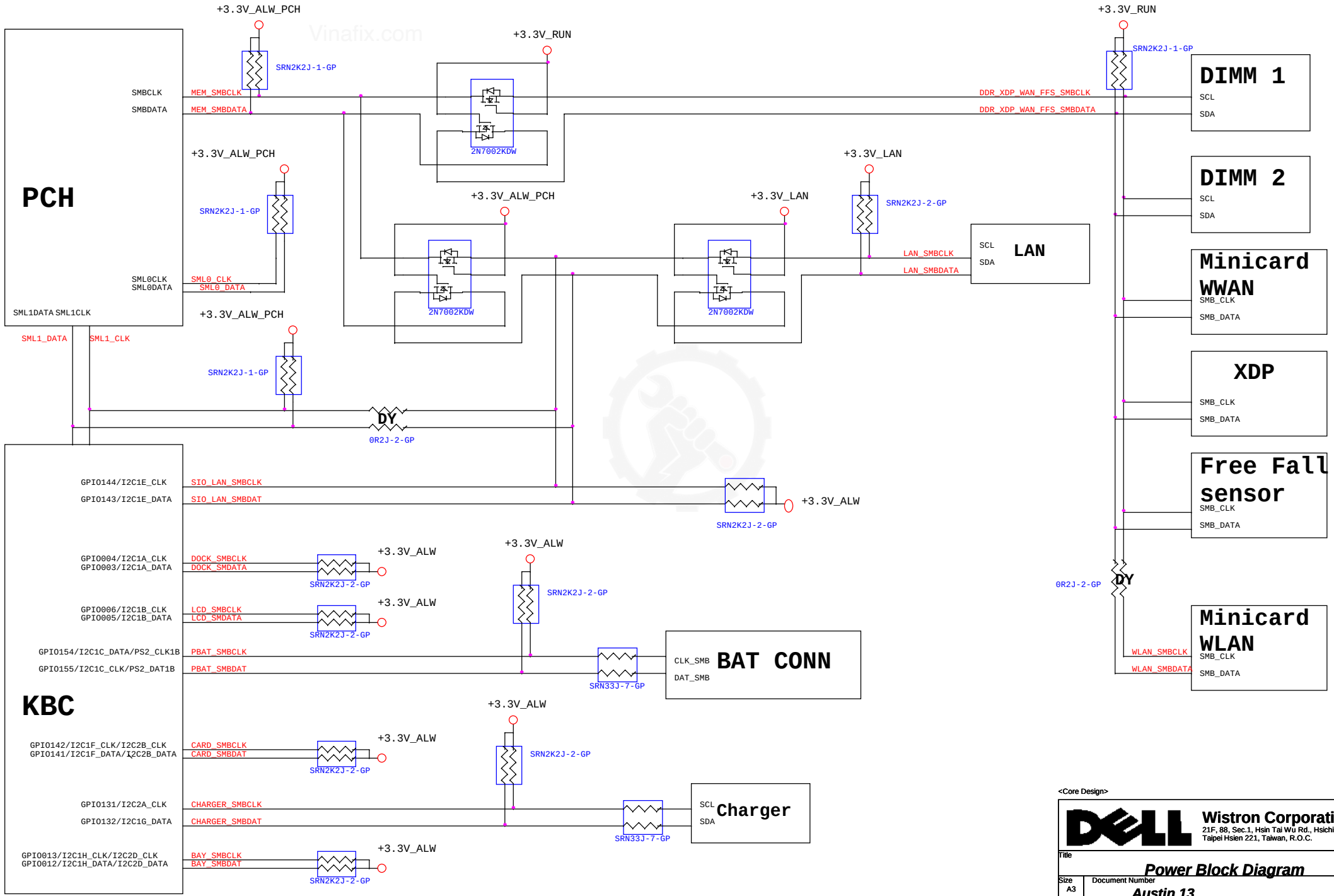
SMBus Block Diagram



<Core Design>

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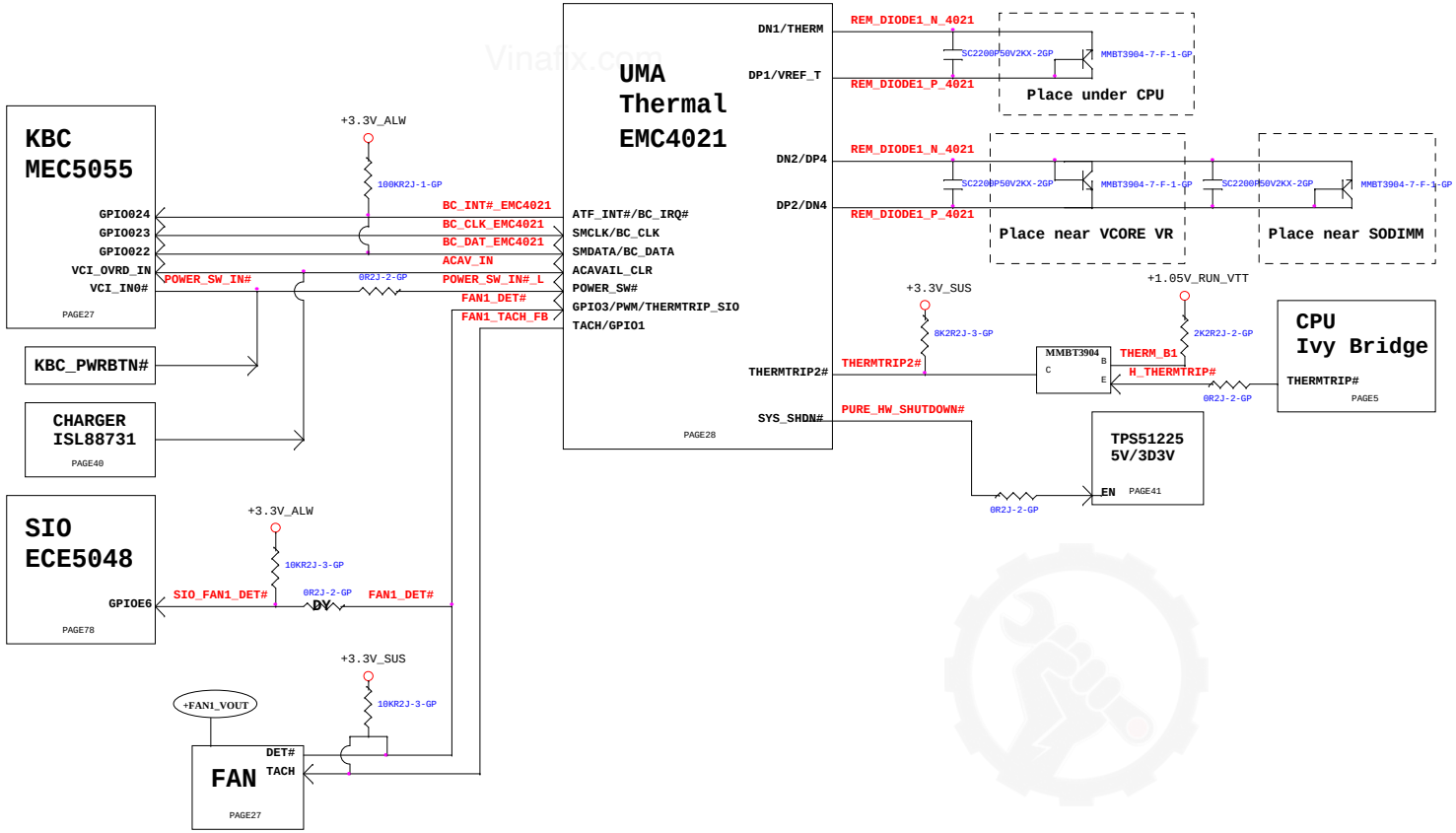
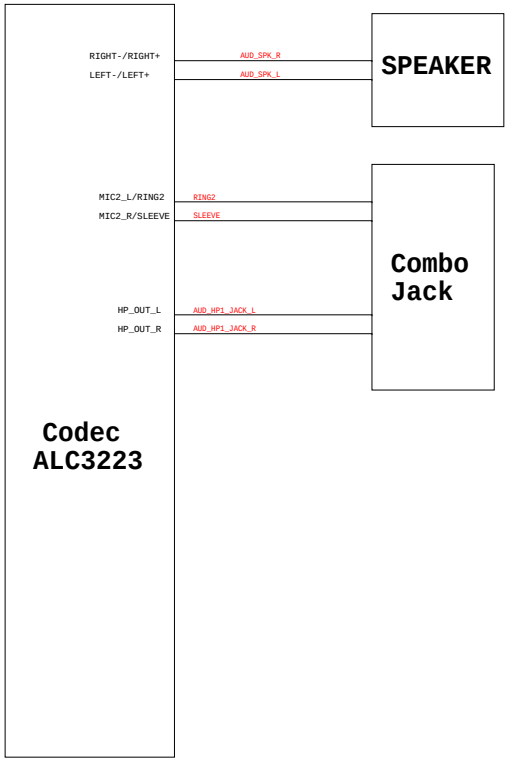
Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title: Power Block Diagram

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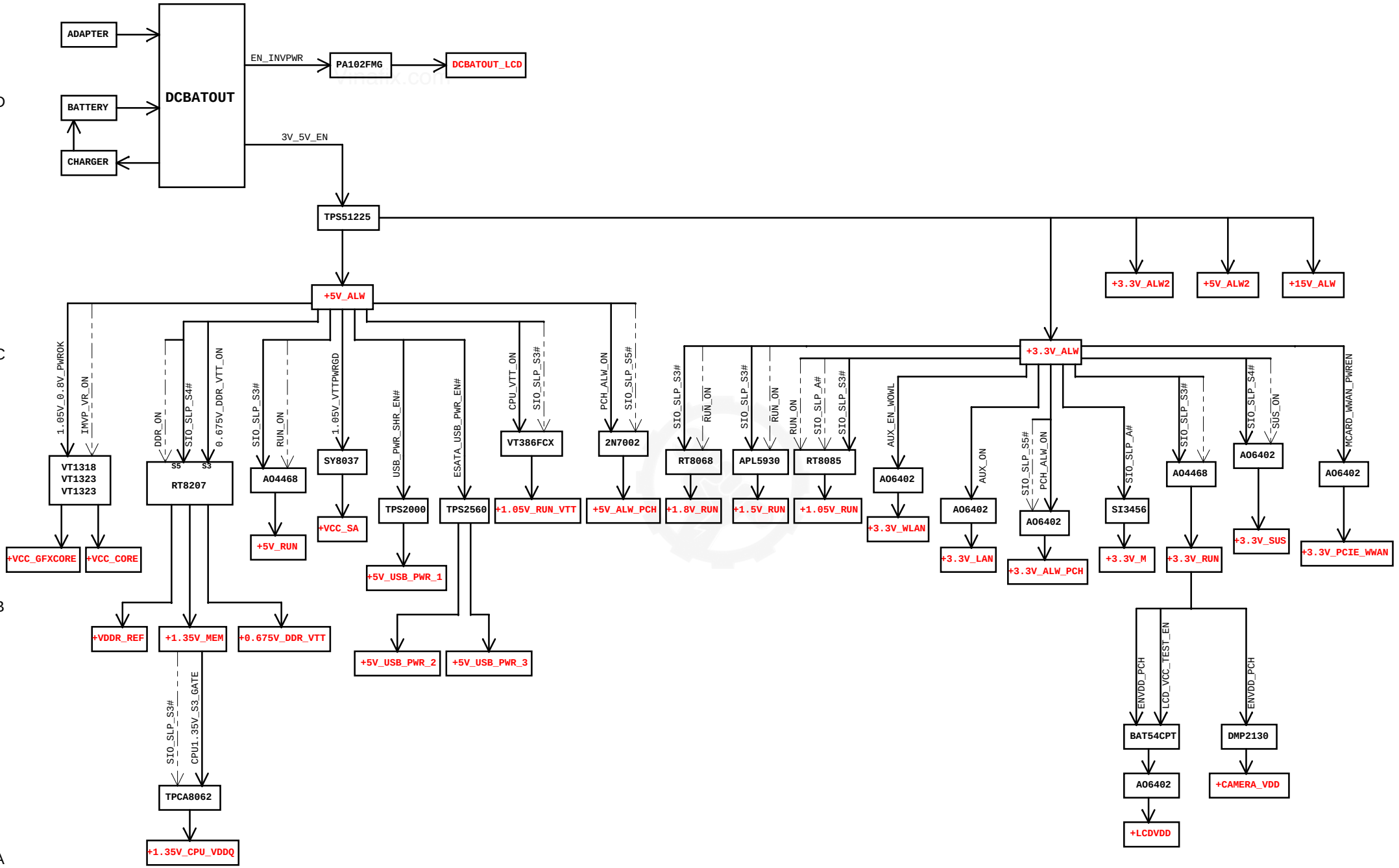

<Core Design>

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Title: Power Rail Diagram

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Version	Date	Page	Function	Change Item
X01	1126	45	Power	PR4515 84K5R2F-GP change to 76K8R2F-GP(64.76825.6DL) V change to 1.0608V
X01	1122	68	EE	Change Q6806 from 84.2N702.J31 to 84.2N702.A3F. And Delete D6804 by LED leackage
X01	1122	38	EE	Change PL3802 from 68.00084.771 to 68.00115.081. Add PL3803 becuz each 3A only. Sourcer : EOL concern, pls downsize to 3216
X01	1122	38	EMC	Change D3901,D3902,D3903 from 83.02025.0AF to 83.52301.0AF.
X01	1122	97	ME	Change SPR4 from 34.17S03.001 to 34.49U23.001. 34.17S03.001此料廠商告之已於09年設變爲34.49U23.001（兩顆料的差異只在於包裝方向不一樣）
X01	1126	66	EE	Re-connect SIM1 for correction.Delete R6605
X01	1129	66,68	EE	Delete R6603 imnstead of Q6602 for leackage Delete R6811 imnstead of Q6811 for leackage
X01	1129	49	EE	Change U4901.1 form +3.3V_RUN to +3.3V_ALW by Leackage
X01	1129	66	EE	Stuff R6612,U6605 for Discharge
X01	1201	37	EE	change U3711 form 74.00863.07B to 74.09818.NBB
X01	1203	68	EE	Add Q6812,R6811
X01	1205	68	EE	Change D6602 from 83.00005.BAE to 83.04220.0AE OBS REASON:For contract issue,replaced by 75.00005.07C Too expensive, pls change to 83.04220.0AE
X01	1211	41	Power	Change PR4115 form 64.15025.6DL to 64.15425.6DL for rise 5V to meet EA measurment
X01	1212	40	Power	Change PR4035 form 64.21535.55L to 64.22635.55L for remove ADP shutdown issue
X01	1212	38	Power	Change PC3805 to PR3812 form 78.10324.2FL to 64.10035.6DL for remove ADP shutdown issue
X01	1219	68	ME	Change PWRBT1 form 62.40076.001 to 62.40009.D71
X01	1219	97	ME	Change SPR4 form 34.17S03.001 to 34.49U23.001
X01	1219	66	ME	Change SIM1 form 62.10034.591 to 62.10034.641
X01	1219	66	EE	Change D6602 form 83.04220.0AE to 75.04220.07C (OBS REASON)
X01	1219	27	EE	Change C2723 and C2724 form 78.22034.1FL to 78.39034.1FL (Base on vendor recommend and Korbel also use 39pF)
X01	1219	27	EE	Change R2735 form 64.13035.6DL to 64.62025.6DL for upgrade PCB version
X01	1219	68	EE	Add AFTP6801
X01	1224	40	Power	Del pg4006 pg4002 pg4008 pg4009 for pu4005 modify high limit
X01	1225	74	EMI	Add R7401
X01	1228	21	EE	Change R2116,R2121,R2127,R2128,R2136 from 63.R0034.1DL to 63.22034.1DL for enhance LPC waveform
X01	0102	49	EMC	Add EC4901~EC4908 and stuff 78.4R774.1FL
X01	0102	47	Power	Add PU4702 2nd =74.07175.031
X01	0104	49	EE	Add R4901,R4902,R4904 prepare for 0603 fuse.
X01	0104	46,41	Power	PU4603, PU4106 84.07696.037 change to 84.08878.A30

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Title: Change History

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Version	Date	Page	Function	Change Item
X01	0109	27	EE	Dummy R2733 to prevent S5 leackage
X01	0109	68	EE	Change R6801 R6802 R6804 R6805 R6806 R6808 from 1.2K (63.12234.1DL) to 330R (63.33134.1DL) for Brightness Tunning
X01	0109	32	EE	Change R3212 from 33R(63.33034.1DL) to 10R(64.10R05.6DL) follow Korbel
X01	0117	66	EE	Change R6612 from 100R(63.10134.1DL) to 1K(63.10234.1DL) prevent De-rating issue.
A00	0206	5	EE	Change Q511 from 84.00138.03K to 84.2N702.J31
A00	0218		Power	0ohm change to pad. Charger :PR4030, PR4009, PR4036,PR4027, 5/3.3v : PR4127, PR4130, PR4116 CPU :PR4251, PR4250 1.05V_VTT : PR4510 , PR4508, 1.05V_M: PR4516, PR4518 1.35V : PR4610, PR4609, PR4608, PR4611 1.8V : PR4722 VCCSA : PR4825, PR4829, PR4810
A00	0220	71	EE	Change XDP1 form 20.F0971.060 to ZZ.00PAD.Q81 Change DB1 from 20.D0183.110 to ZZ.00PAD.Y41
A00	0220	27	EE	Change R2735 to 64.33025.6DL for XB
A00	0220		EE	Change to 0 ohm pad. R1928, R1934, R1936, R2309, R2705, R2701, R2831, R3610, R3655, PR4622, R3652, R3649, PR4730 R4921, R4922, R4923, R4924, R4919, R4920, R4925, R4926, R6609,
A00	0220	40	EE	Add PC4040,PC4041
A00	0226	49	EE	Delete R4903,R4908
A00	0226	78	EE	Chnage R7826,R7841 to SHORT PAD

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Title: Change History

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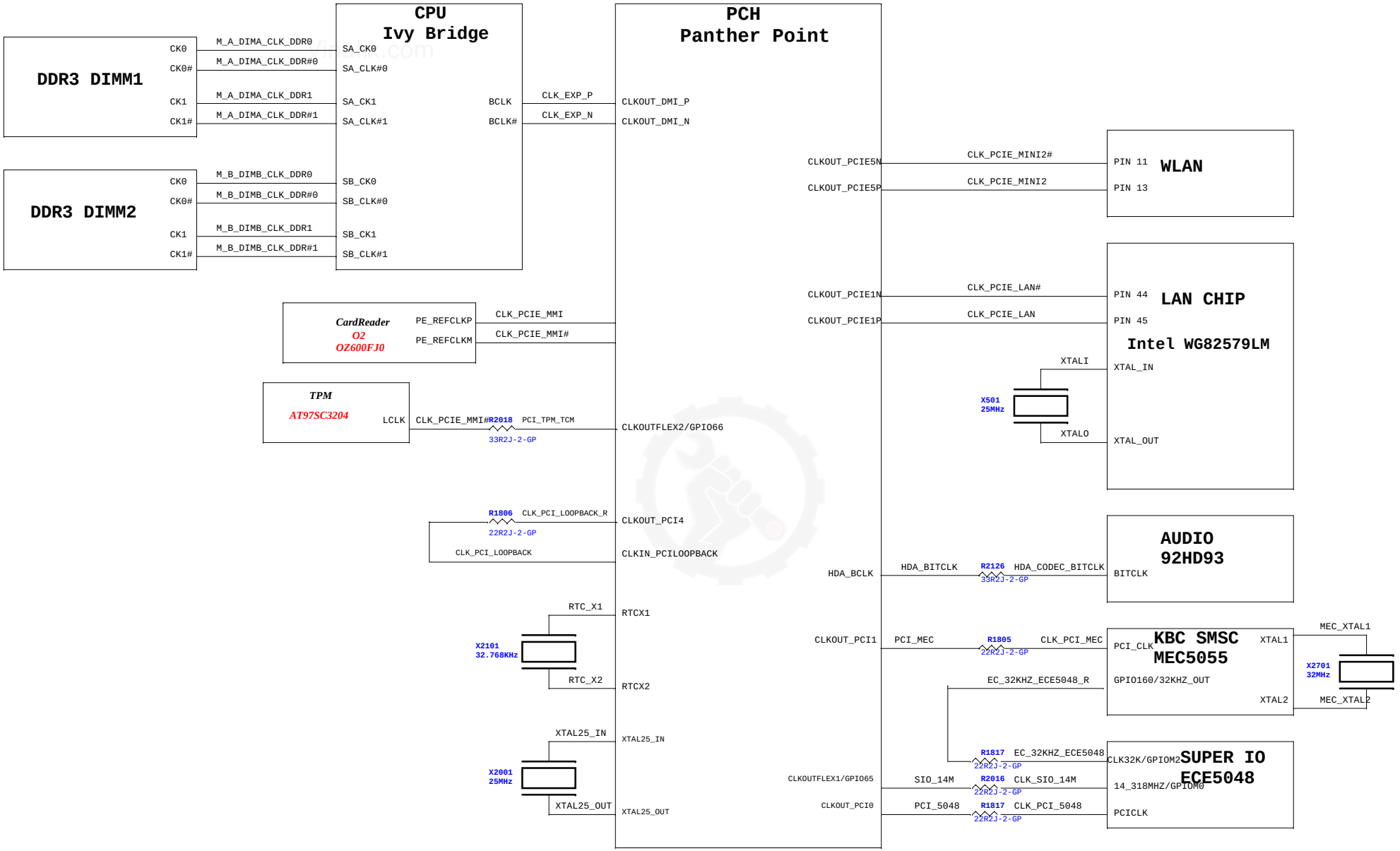
AUSTIN CLK Block Diagram



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Title: CLK Diagram

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