COMPAL CONFIDENTIAL

MODEL NAME : Goliad MLK 12 UMA

PCB NO : LA-A971P

BOM P/N : 4319RJ31LXX

GPIO MAP: 3.3b

Goliad MLK 12" UMA

Broadwell U Processor

2013-12-23

REV : 0.3 (X01)

@ : Nopop Component

EMC@ : EMI, ESD and RF Component

@EMC@ : EMI, ESD and RF Nopop Component

CXDP@ : XDP Component

CONN@ : Connector Component

VPRO@ : Vpro Component

NVPRO@ : Non-Vpro Component

Layout Dell logo

REV: X01
PWB: 89XM3
DATE: 1351-05

MB PCB

Part Number	Description
DA80003000	PCB 14A LA-A971P REV0 MB WITH DOCKING 2

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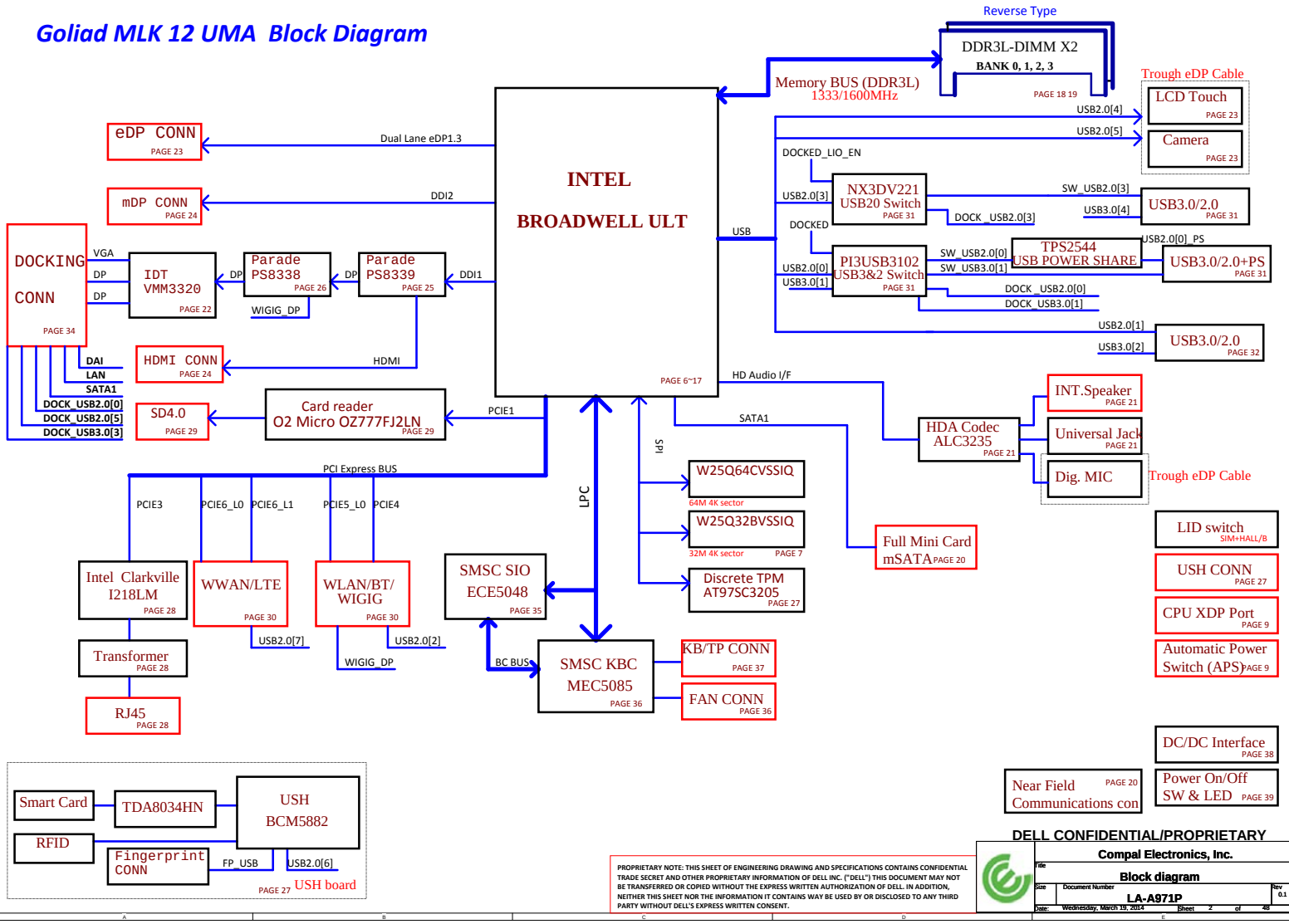
Title: Cover Sheet

Size: | Document Number: LA-A971P | Rev: 0.1

Date: Wednesday, March 19, 2014 | Sheet 1 of 48

Goliad MLK 12 UMA Block Diagram



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Title: Block diagram

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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

PM TABLE

State \ power plane	+5V_ALW +3.3V_ALW +3.3V_ALW_PCH +3.3V_RTC_LDO	+3.3V_SUS +1.35V_MEM	+5V_RUN +3.3V_RUN +0.675V_DDR_VTT +1.05V_RUN +VCC_CORE	+3.3V_M +1.05V_M	+3.3V_M +1.05V_M (M-OFF)
S0	ON	ON	ON	ON	ON
S3	ON	ON	OFF	ON	OFF
S5 S4/AC	ON	OFF	OFF	ON	OFF
S5 S4/AC doesn't exist	OFF	OFF	OFF	OFF	OFF

PCIE	USB3.0	SATA	DESTINATION
	USB3.0 1		JUSB1-->Rear left
	USB3.0 2		JUSB3-->Right
PCIE 1	USB3.0 3		MMI (CARD READER)
PCIE 2	USB3.0 4		JUSB2-->Rear Right
PCIE 3			LOM
PCIE 4			WLAN - JNGFF1
PCIE 5			WiGig - JNGFF1
PCIE 6		SATA 3	HCA & SATA Cache - JNGFF2
		SATA 2	SATA Cache - JNGFF2
		SATA 1	JMINI3
		SATA 0	JDOCK1

	USB PORT#	DESTINATION
BDW ULT	0	JUSB1 or DOCK1
	1	JUSB3
	2	WLAN + BT
	3	JUSB2 or DOCK2
	4	Touch Screen
	5	CAMERA
	6	USH
	7	WWAN

USH	0	BIO
	1	NA

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Title: Port assignment

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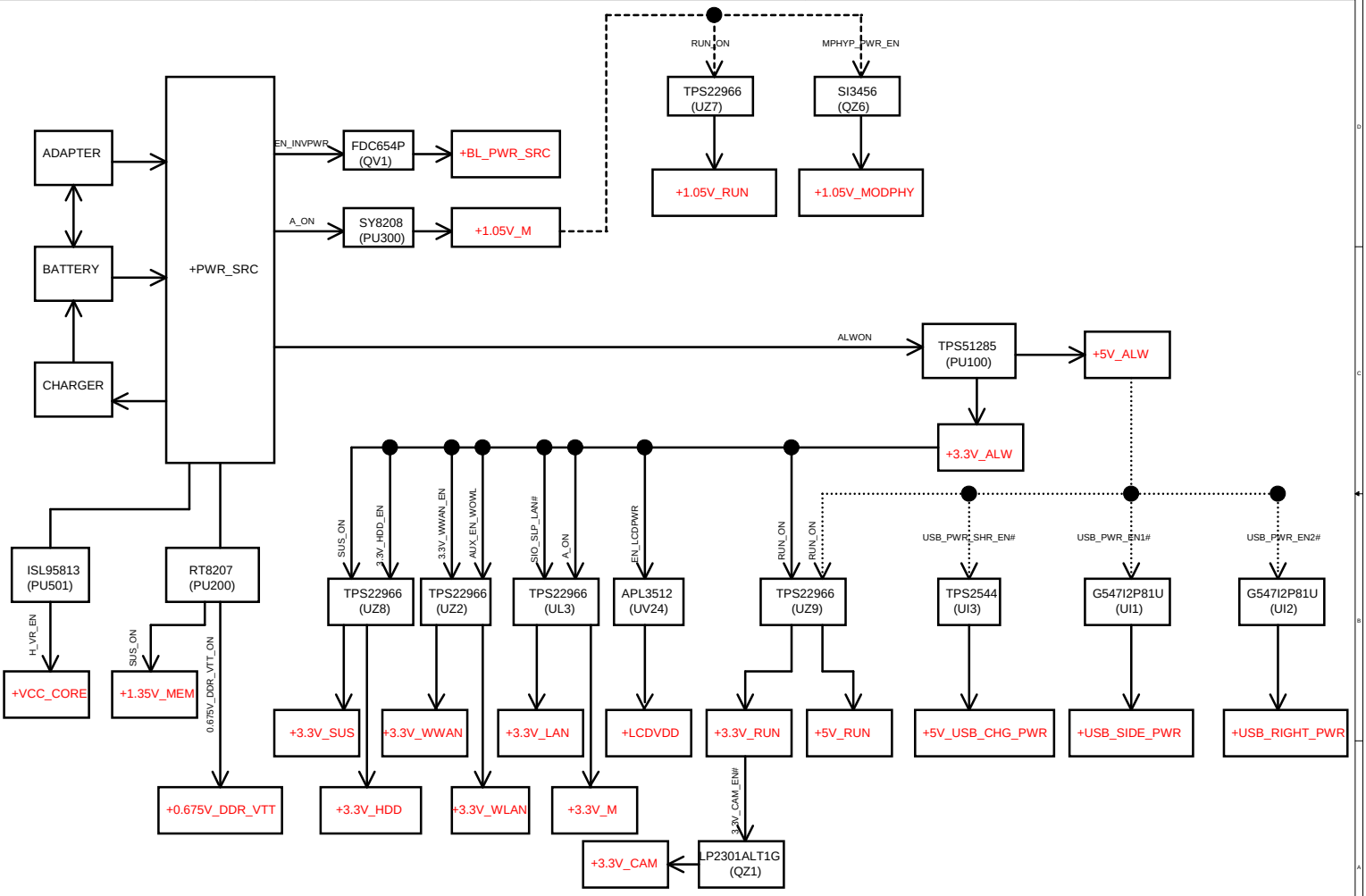

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Title: Power rails

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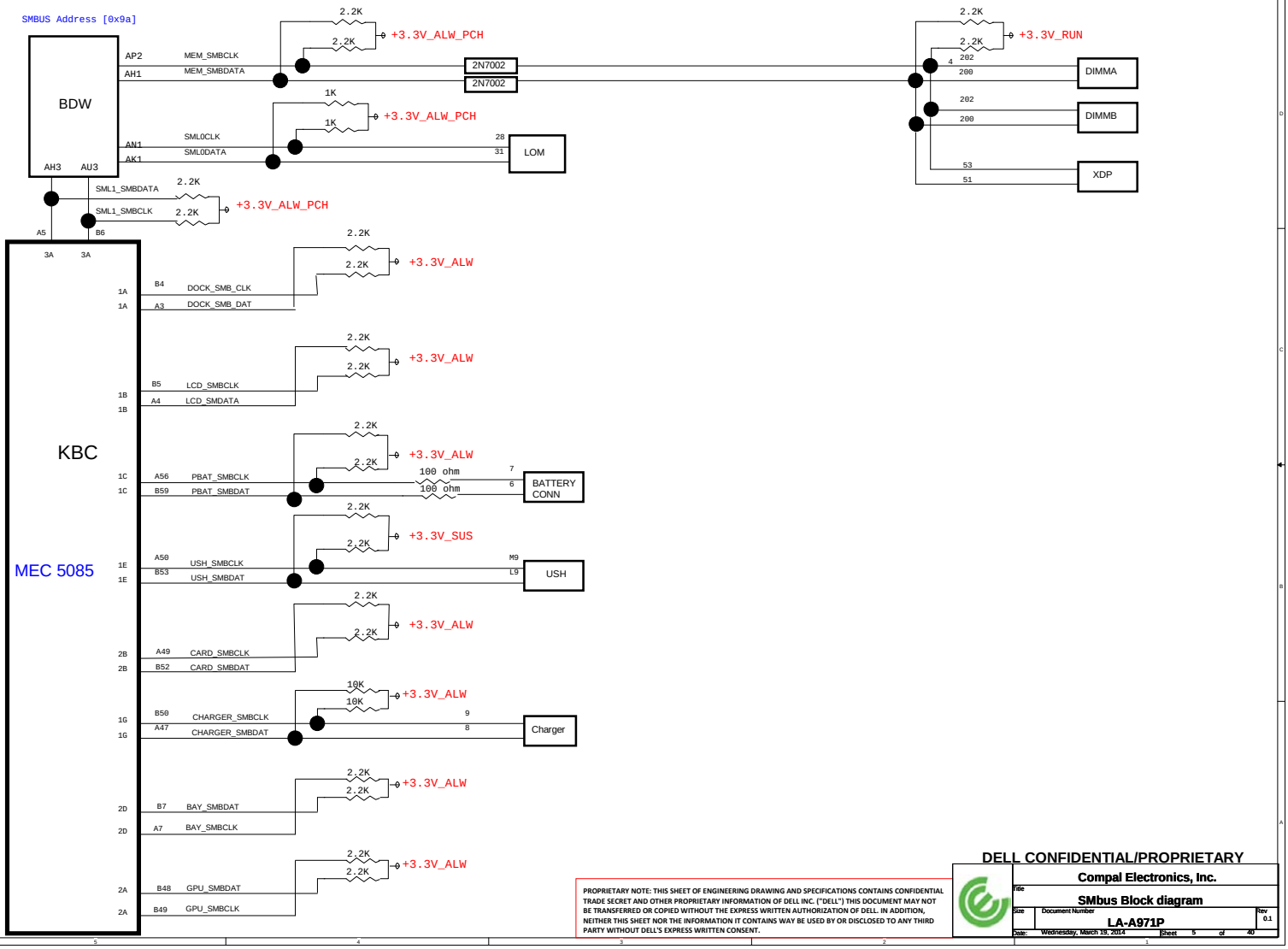

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Title: SMbus Block diagram

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UMA SATA port

SATA0	SATA1	PCB	SATA2/PCIE6 L1	SATA3/PCIE6 L0	
E-Dock	mSATA	G12 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G12 Entry	NA	NA	
E-Dock	mSATA	G14 DSC	M2 3042 SATA-Cache(no HCA)	M2 3030 WIGIG	SATA2/PCIE6_L1 contact to WWAN SATA3/PCIE6 L0 contact to WLAN
E-Dock	HDD	G14 UMA	M2 3042 2nd PCIe Lane for PCIe Cache	M2 3042 (HCA & SATA-Cache)	contact to WWAN
NA	mSATA	G14D_En	NA	M2 3030 WIGIG	contact to WLAN
NA	HDD	G14U_En	NA	NA	

Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

+3.3V_ALW_PCH

ME_FWP_EC — @RC301 0_0402_5% — ME_FWP

PT, ST pop RC2 & SW1; MP pop RC301.

RC2 1K_0402_5%

<36> ME_FWP_EC

SW1 — SSSCMFTQRS_5P

ME_FWP PCH has internal 20K PD.

FLASH DESCRIPTOR SECURITY OVERRIDE	
LOW = ENABLE (DEFAULT)	-->Pin1 & Pin3 short
HIGH = DISABLE (ME can update)	-->Pin2 & Pin3 short

+RTC_CELL — RC1 330K_0402_5% — PCH_INTVRMEN

INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

CC1 12P_0402_50V8J — PCH_RTCX1_R — @RC4 0_0402_5% — PCH_RTCX1

YC1 32.768KHZ_12.5PF_9H03220008 — RC7 10M_0402_5%

CC2 12P_0402_50V8J — PCH_RTCX2

RC9 1M_0402_5%

RC10 20K_0402_5%

RC8 20K_0402_5%

@CMOS1 SHORT PADS-D

CC3 1U_0402_6.3V6K

CC4 1U_0402_6.3V6K

CMOS place near DIMM

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

UC1E — BDW_ULT_DDR3L

RTC: RTCX1, RTCX2, INTRUDER, INTVRMEN, SRTCRST, RTCRST

<9> PCH_RTCRST#

INTRUDER# — PCH_INTVRMEN — SRTCRST# — PCH_RTCRST#

AUDIO: HDA_BCLK/I2S0_SCLK, HDA_SYNC/I2S0_SFRM, HDA_RST/I2S_MCLK, HDA_SDI0/I2S0_RXD, HDA_SDI1/I2S1_RXD, HDA_SDO/I2S0_TXD, HDA_DOCK_EN/I2S1_TXD, HDA_DOCK_RST/I2S1_SFRM, I2S1_SCLK

PCH_AZ_BITCLK — PCH_AZ_SYNC — PCH_AZ_RST# — PCH_AZ_CODEC_SDIN0

<21> PCH_AZ_CODEC_SDIN0

ME_FWP — RC11 1K_0402_5% — PCH_AZ_SDOUT

SATA: SATA_RN0/PERN6_L3, SATA_RP0/PERP6_L3, SATA_TN0/PETN6_L3, SATA_TP0/PETP6_L3

J5: H5, B15, A15

SATA_PRX_DKTX_N0_C <34> — SATA_PRX_DKTX_P0_C <34> — SATA_PTX_DKRX_N0_C <34> — SATA_PTX_DKRX_P0_C <34>

for DOCK

SATA_RN1/PERN6_L2, SATA_RP1/PERP6_L2, SATA_TN1/PETN6_L2, SATA_TP1/PETP6_L2

J8: H8, A17, B17

SATA_PRX_DTX_N1 <20> — SATA_PRX_DTX_P1 <20> — SATA_PTX_DRX_N1 <20> — SATA_PTX_DRX_P1 <20>

SATA HDD

SATA_RN2/PERN6_L1, SATA_RP2/PERP6_L1, SATA_TN2/PETN6_L1, SATA_TP2/PETP6_L1

J6: H6, B14, C15

PCIE_PRX_SATATX_N6_L1 <30> — PCIE_PRX_SATATX_P6_L1 <30> — PCIE_PTX_SATARX_N6_L1 <30> — PCIE_PTX_SATARX_P6_L1 <30>

for PCIe Cache (WWAN)

SATA_RN3/PERN6_L0, SATA_RP3/PERP6_L0, SATA_TN3/PETN6_L0, SATA_TP3/PETP6_L0

F5: E5, C17, D17

PCIE_PRX_SATATX_N6_L0 <30> — PCIE_PRX_SATATX_P6_L0 <30> — PCIE_PTX_SATARX_N6_L0 <30> — PCIE_PTX_SATARX_P6_L0 <30>

for SATA-CACHE (WWAN)

SATA0GP/GPIO34, SATA1GP/GPIO35, SATA2GP/GPIO36, SATA3GP/GPIO37

V1 MPCIE_RST# — V6 SATA2_PCIE6_L1 — AC1

HDD_DET# <20> — SATA2_PCIE6_L1 <12,35> — mCARD_PCIE#_SATA <36,7>

SATA_IREF — A12 — PCH_ASATA3PLL

RSVD — L11

RSVD — K10

SATA_RCOMP — C12 — SATA_COMP

SATA1ES — U3 — SATA_ACT#

SATA_ACT# <39>

JTAG: PCH_TRST, PCH_TCK, PCH_TDI, PCH_TDO, PCH_TMS, RSVD, RSVD, ITAGX, RSVD

<9> PCH_JTAG_TRST# — PCH_JTAG_TRST# AU62
<9> PCH_JTAG_TCK — PCH_JTAG_TCK AE62
<9> PCH_JTAG_TDI — PCH_JTAG_TDI AD61
<9> PCH_JTAG_TDO — PCH_JTAG_TDO AE61
<9> PCH_JTAG_TMS — PCH_JTAG_TMS AD62
PM_TEST_RST AL11
<9> PCH_JTAG_JTAGX — AC2 — AE63 — AV2

BDW-ULT-DDR3L_BGA1168
5 OF 19

+1.05V_M — RPC21 51_0804_8P4R_5% — PCH_JTAG_TDO, PCH_JTAG_TMS, PCH_JTAG_TDI

@RC18 1K_0402_1% — PCH_JTAG_JTAGX

@RC21 51_0402_5% — PCH_JTAG_TCK

+1.05V_M — @RC300 10K_0402_5%

@CC100 1U_0402_6.3V6K

+3.3V_RUN — RPC18 10K_8P4R_5%

MPCIE_RST# — HDD_DET#

<29,7> MMCLK_REQ# — <10> DGPU_PWROK

HDA for Codec

<21> PCH_AZ_CODEC_SDOUT — RC19 33_0402_5% — PCH_AZ_SDOUT
<21> PCH_AZ_CODEC_SYNC — RC20 33_0402_5% — PCH_AZ_SYNC
<21> PCH_AZ_CODEC_RST# — RC22 33_0402_5% — PCH_AZ_RST#
<21> PCH_AZ_CODEC_BITCLK — RC23 33_0402_5% — PCH_AZ_BITCLK

EMC@ CC2 27P_0402_50V8J

Reserve for EMI

SATA Impedance Compensation

+PCH_ASATA3PLL — SATA_COMP — 3.01K_0402_1% — RC17

CAD note:
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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Title: CPU (1/12)

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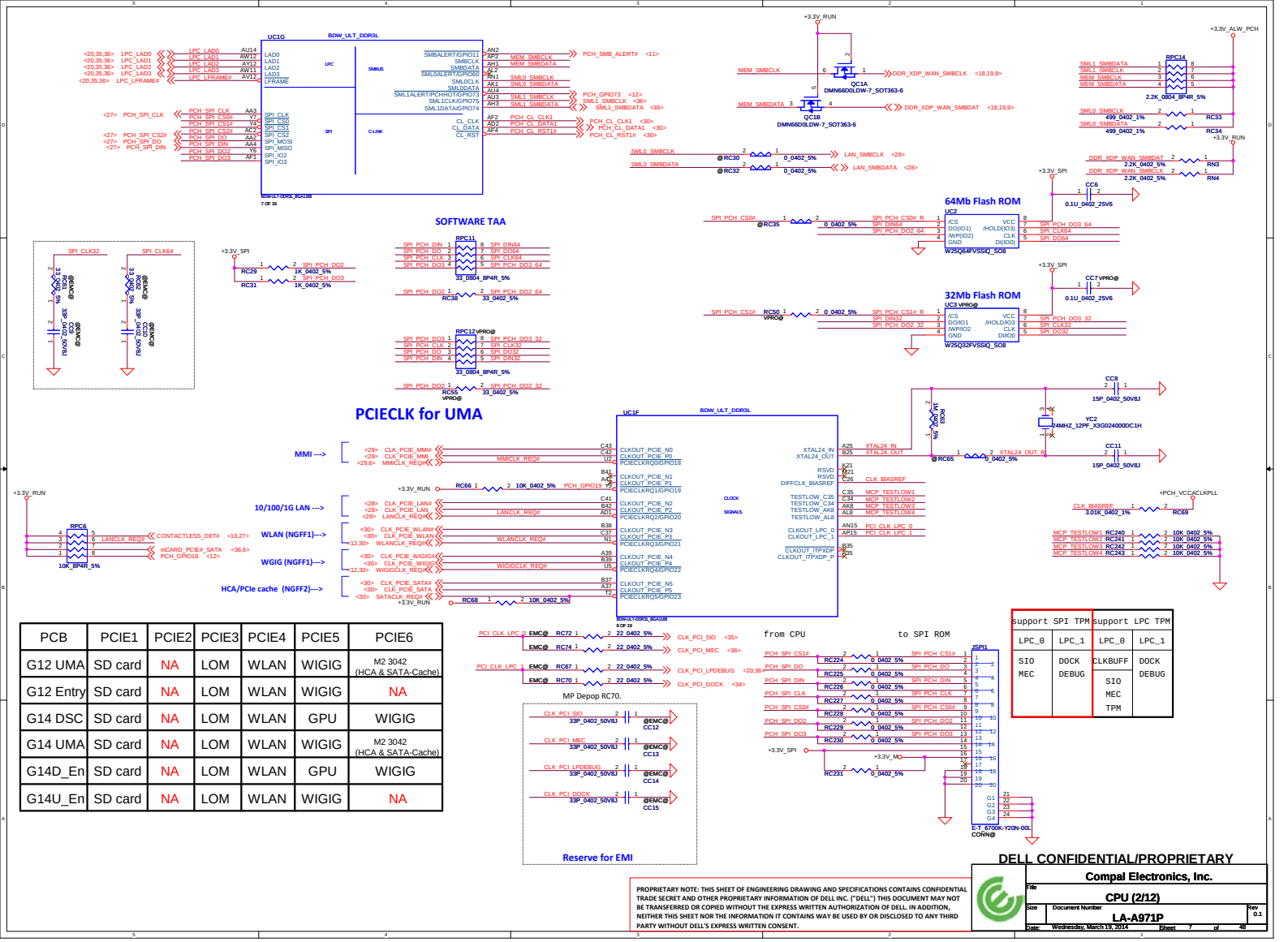

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA

Support SPI TPM		Support LPC TPM	
LPC_0	LPC_1	LPC_0	LPC_1
SIO	DOCK	CLKBUFF	DOCK
MEC	DEBUG	SIO	DEBUG
		MEC	
		TPM	

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Title: CPU (2/12)

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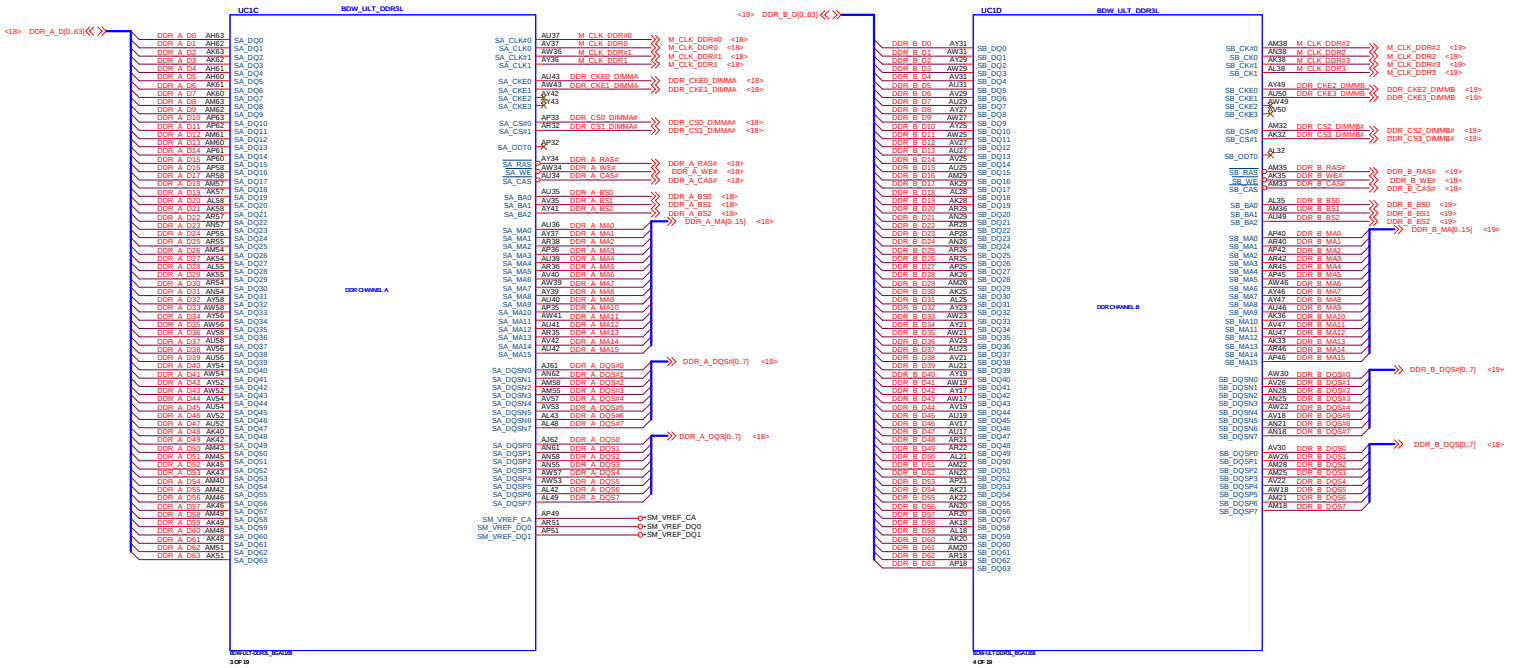

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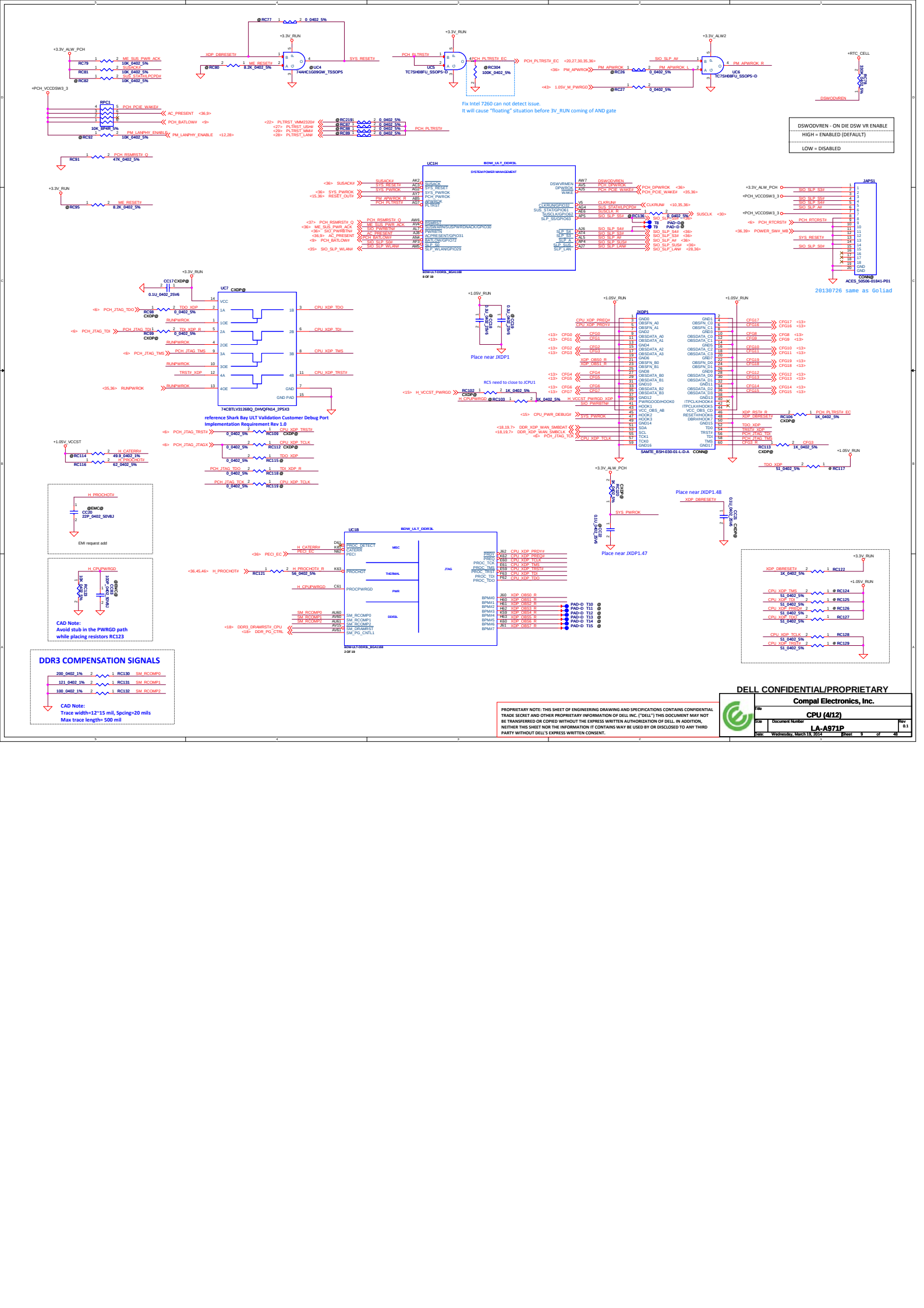
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED
Fix Intel 7260 can not detect issue.
It will cause "floating" situation before 3V_RUN coming of AND gate
20130726 same as Goliad
Place near JXDP1
Place near JXDP1.48
Place near JXDP1.47
reference Shark Bay ULT Validation Customer Debug Port
Implementation Requirement Rev 1.0
RCS need to close to JCPU1
74CBTLV3126BQ_DHVQFN14_2P5X3
SAMTE_BSH-030-01-L-D-A CONN@
ACES_50506-01841-P01
DDR3 COMPENSATION SIGNALS
200_0402_1% RC130 SM_RCOMP0
121_0402_1% RC131 SM_RCOMP1
100_0402_1% RC132 SM_RCOMP2
CAD Note:
Trace width=12~15 mil, Spcing=20 mils
Max trace length= 500 mil
CAD Note:
Avoid stub in the PWRGD path
while placing resistors RC123
EMI request add
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CPU (4/12)
LA-A971P
Wednesday, March 19, 2014
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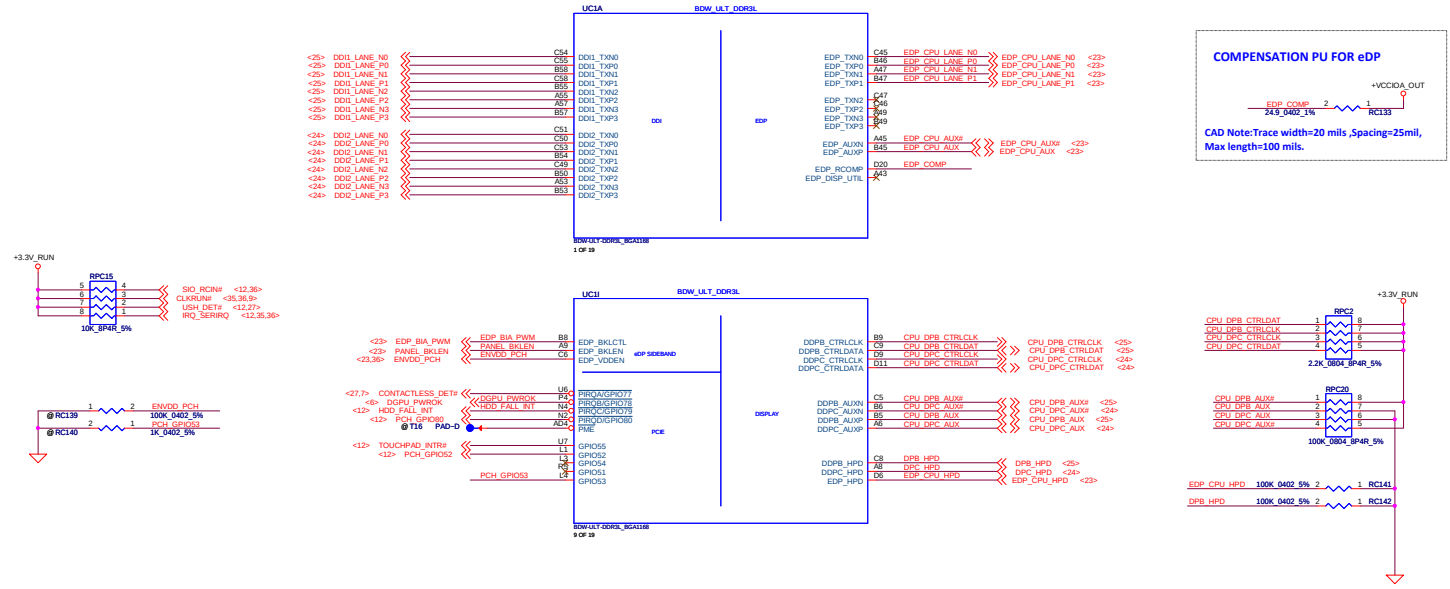

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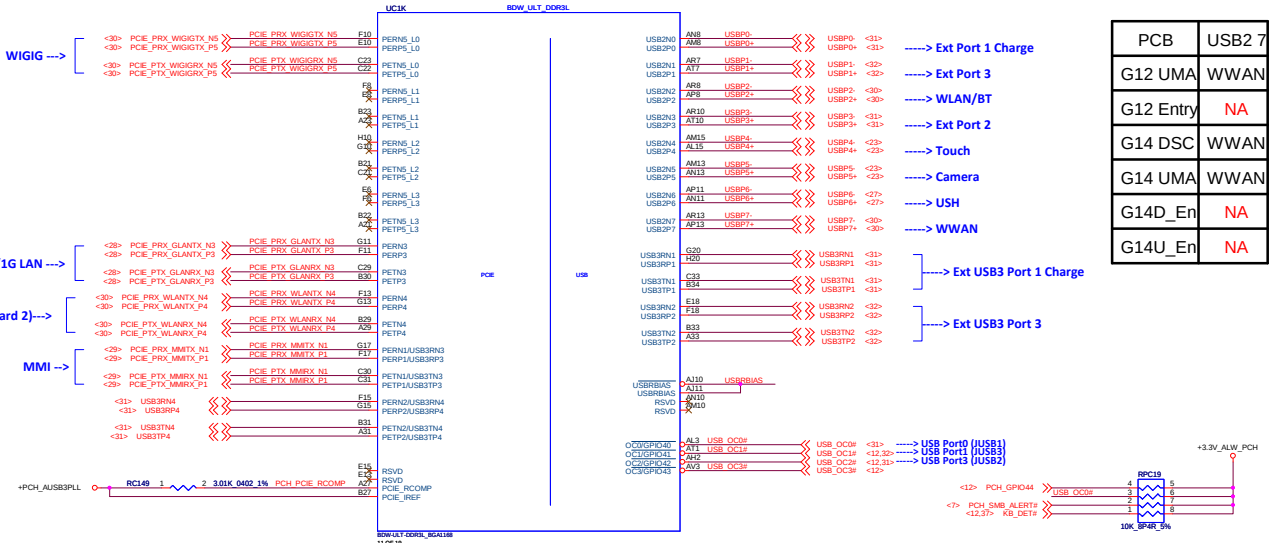
PCIE for UMA



PCB	USB2 7
G12 UMA	WWAN
G12 Entry	NA
G14 DSC	WWAN
G14 UMA	WWAN
G14D_En	NA
G14U_En	NA

PCB	PCIE1	PCIE2	PCIE3	PCIE4	PCIE5	PCIE6
G12 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G12 Entry	SD card	NA	LOM	WLAN	WIGIG	NA
G14 DSC	SD card	NA	LOM	WLAN	GPU	WIGIG
G14 UMA	SD card	NA	LOM	WLAN	WIGIG	M2 3042 (HCA & SATA-Cache)
G14D_En	SD card	NA	LOM	WLAN	GPU	WIGIG
G14U_En	SD card	NA	LOM	WLAN	WIGIG	NA

CAD NOTE:
Route single-end 50-ohms and max 500-mils length.
Avoid routing next to clock pins or under stitching capacitors.
Recommended minimum spacing to other signal traces is 15 mils.

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Title: CPU (6/12)

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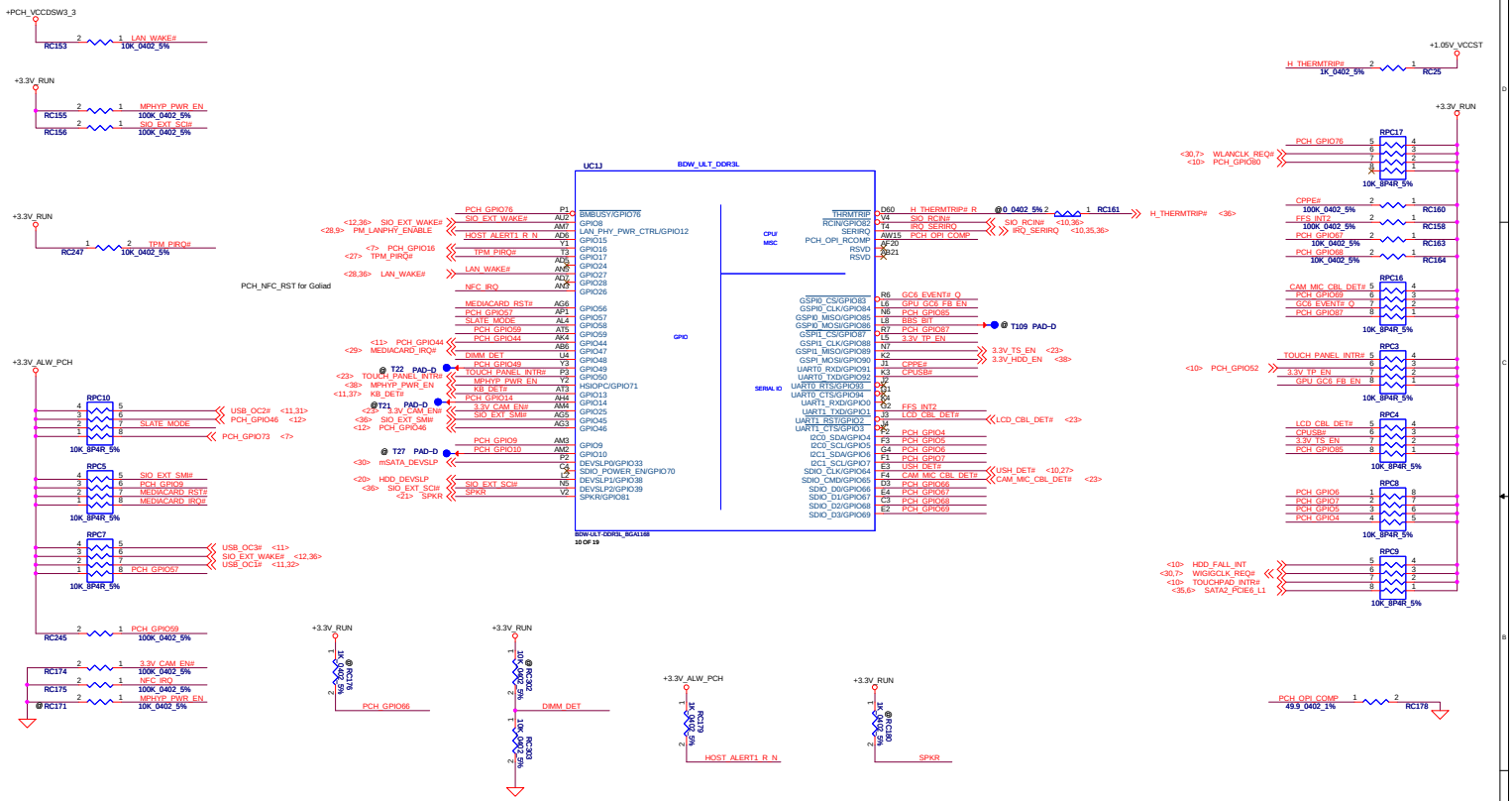

TOP-BLOCK SWAP OVERRIDE	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

TLS CONFIDENTIALITY	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

No Reboot on TCO Timer expiration	
HIGH	ENABLE
LOW(DEFAULT)	DISABLE

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Title: CPU (7/12)		
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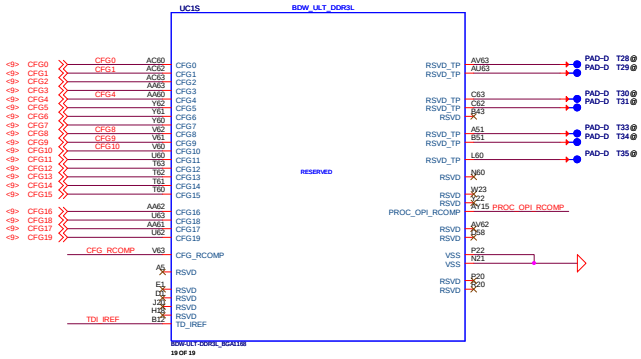
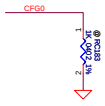
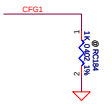
CFG STRAPS for CPU

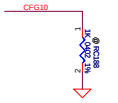


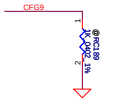


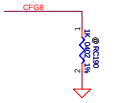
EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	1:(Default) Normal Operation; No stall 0:Lane Reversed

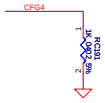


PCH/PCH LESS MODE SELECTION	
CFG1	1:(Default) Normal Operation 0:Lane Reversed









SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

	Display Port Presence Strap
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	0 : Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: CPU (8/12)

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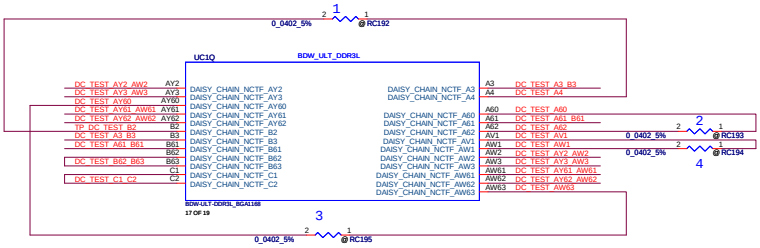


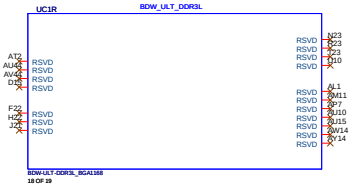
Package Daisy Chain:

1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4

2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60

3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63

4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



Compal Electronics, Inc.

Title: CPU (9/12)

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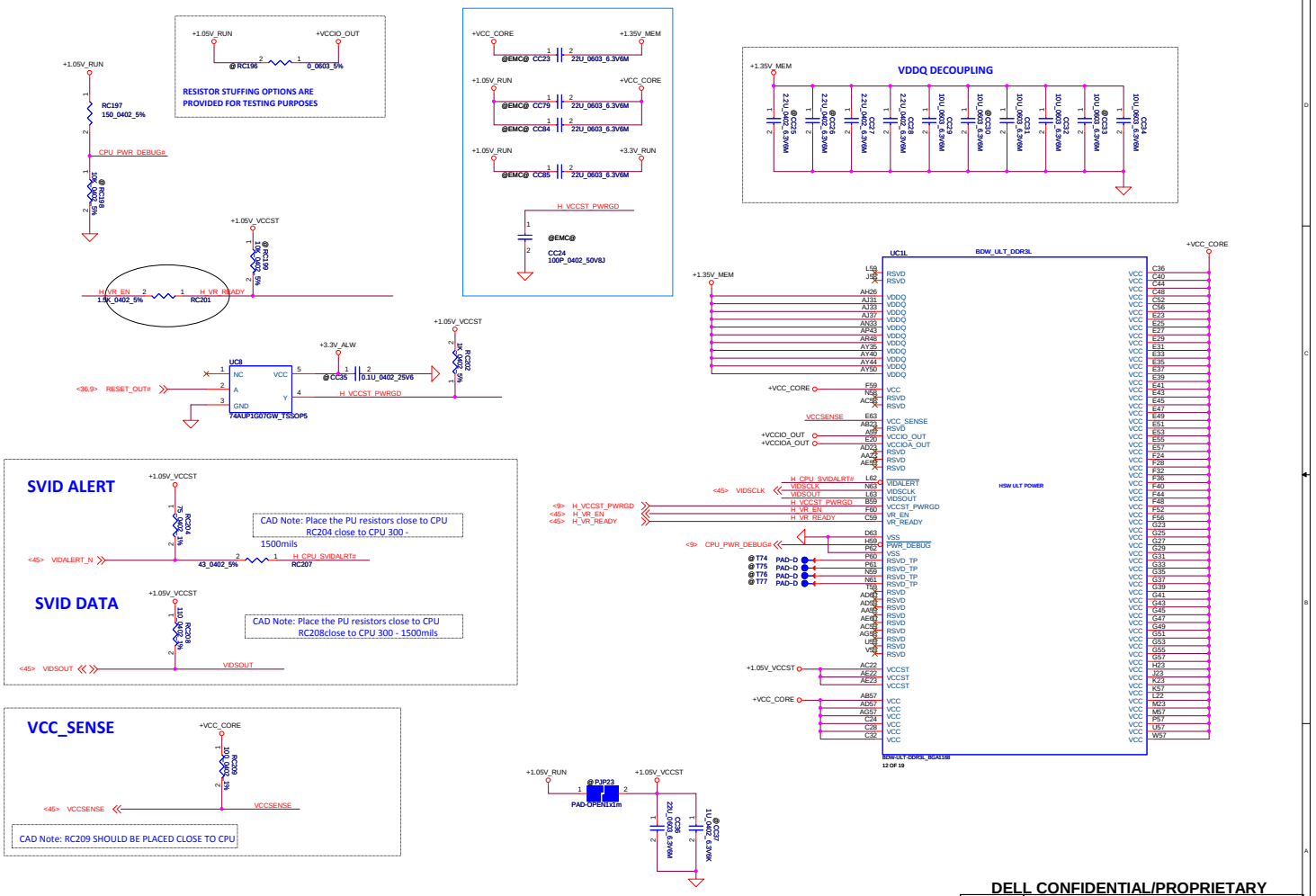
ESD Request



Compal Electronics, Inc.

Title: CPU (10/12)

Size: | Document Number: LA-A971P | Rev: 0.1

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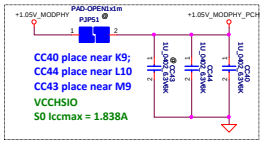

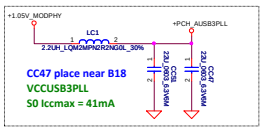

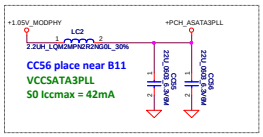

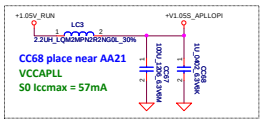

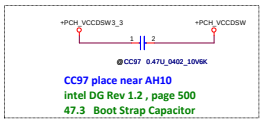

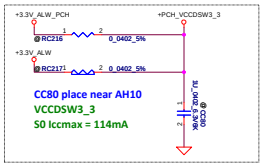

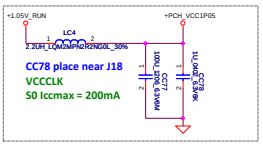

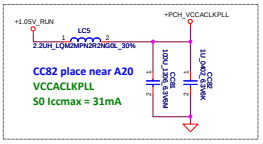

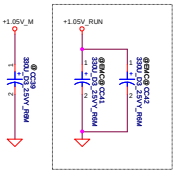

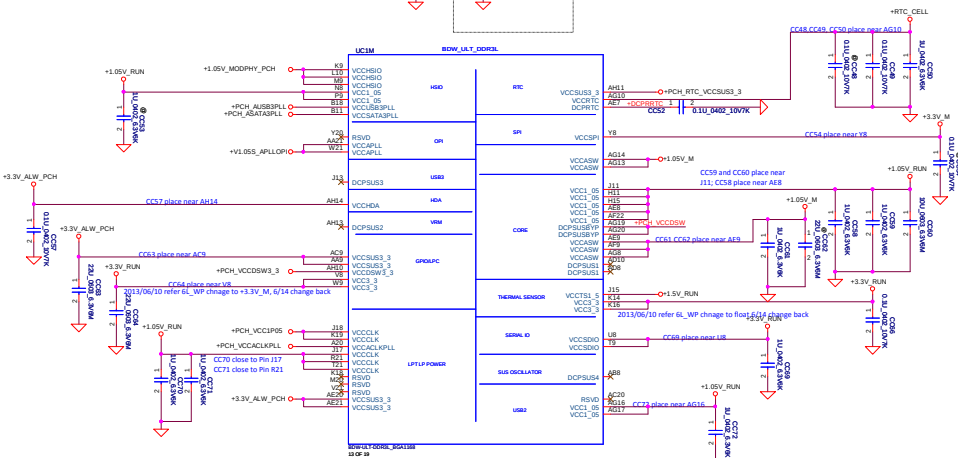

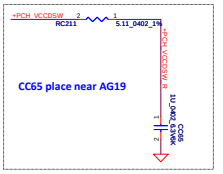

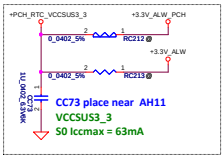

Voltage Rail	Voltage (V)	S0 Iccmax Current (A)[3]	Sx Iccmax Current (A)[3]	Deep Sx Iccmax (A)[3]	G3
VCC1_05 (Internal Suspend VR mode using INTVRMEN)	1.05	1.741	0	0	0
VCC1_05 (External Suspend VR mode using INTVRMEN)	1.05	1.432	0	0	
VCCAPLL	1.05	0.057	0	0	0
VCCSATA3PLL	1.05	0.042	0	0	0
VCCUSB3PLL	1.05	0.041	0	0	0
VCCACLKPLL	1.05	0.031	0	0	0
VCCCLK	1.05	0.200	0	0	0
VCCHSIO	1.05	1.038	0	0	0
VCCTS1_5	1.5	0.003	0	0	0
VCC3_3	3.3	0.041	0	0	0
VCCSDIO	3.3	0.017	0	0	0
VCCASW	1.05	0.638	0	0	0
VCCSRT	3.3	0.018	0	0	0
VCCHDA	3.3	0.011	<1 mA	0	0
VCCSUS3_3 (Internal Suspend VR mode using INTVRMEN)	3.3	0.063	0.024	0	0
VCCSUS3_3 (External Suspend VR mode using INTVRMEN)	3.3	0.062	0.005	0	0
DcpSus1[4]	1.05	0.109	0.014	0	0
DspSus2[4]	1.05	0.025	0.001	0	0
DspEus3[4]	1.05	0.010	0.003	0	0
DcpSus4[4]	1.05	0.001	0.001	0	0
VCCDSW3_3	3.3	0.114	0.004	0.002	0
VCCRTC	3.3	<1 mA	<1 mA	<1 mA	6 µA See notes 1, 2

Reminder below power rail need isolation for layout refer attach file for more detail that from Intel review feedback.

Power Rail Isolation

Voltage Supply	Interface/power rail isolation required	PCH Pins sharing power rail
V1.05s	Core	J11, H11, H15, AE8, AF22
	OPI	AA21, W21
	HSIO	K9, L10, N8, P9, B18, B11, M9
	USB2	AG15, AG17
	CLK(PLL	A20
	CLK(A)	R21, T21
	CLK(B)	J18, K19
	CLK(C)	J17
V3.3a	GPIO	AC9, AA9, AE20, AE21
	RTC	AH11
	HDA	AH14
V3.3s	GPIO	V8, W9
	SDIO	U8, T9
	Thermal Sensor	K14, K16

Compal Electronics, Inc.

Title: CPU (11/12)

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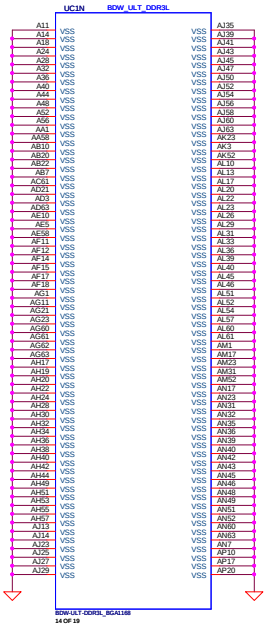

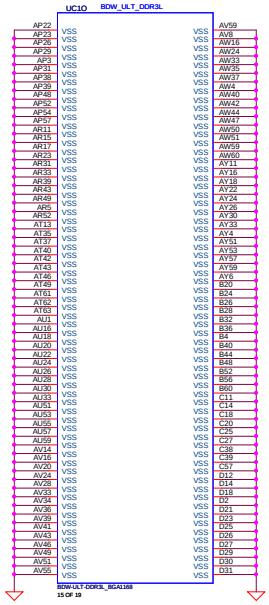

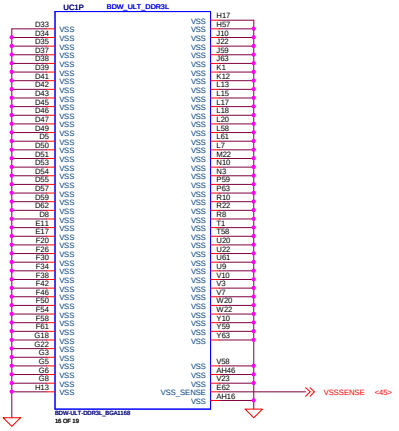

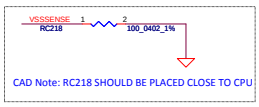

Compal Electronics, Inc.		
Title: CPU (12/12)		
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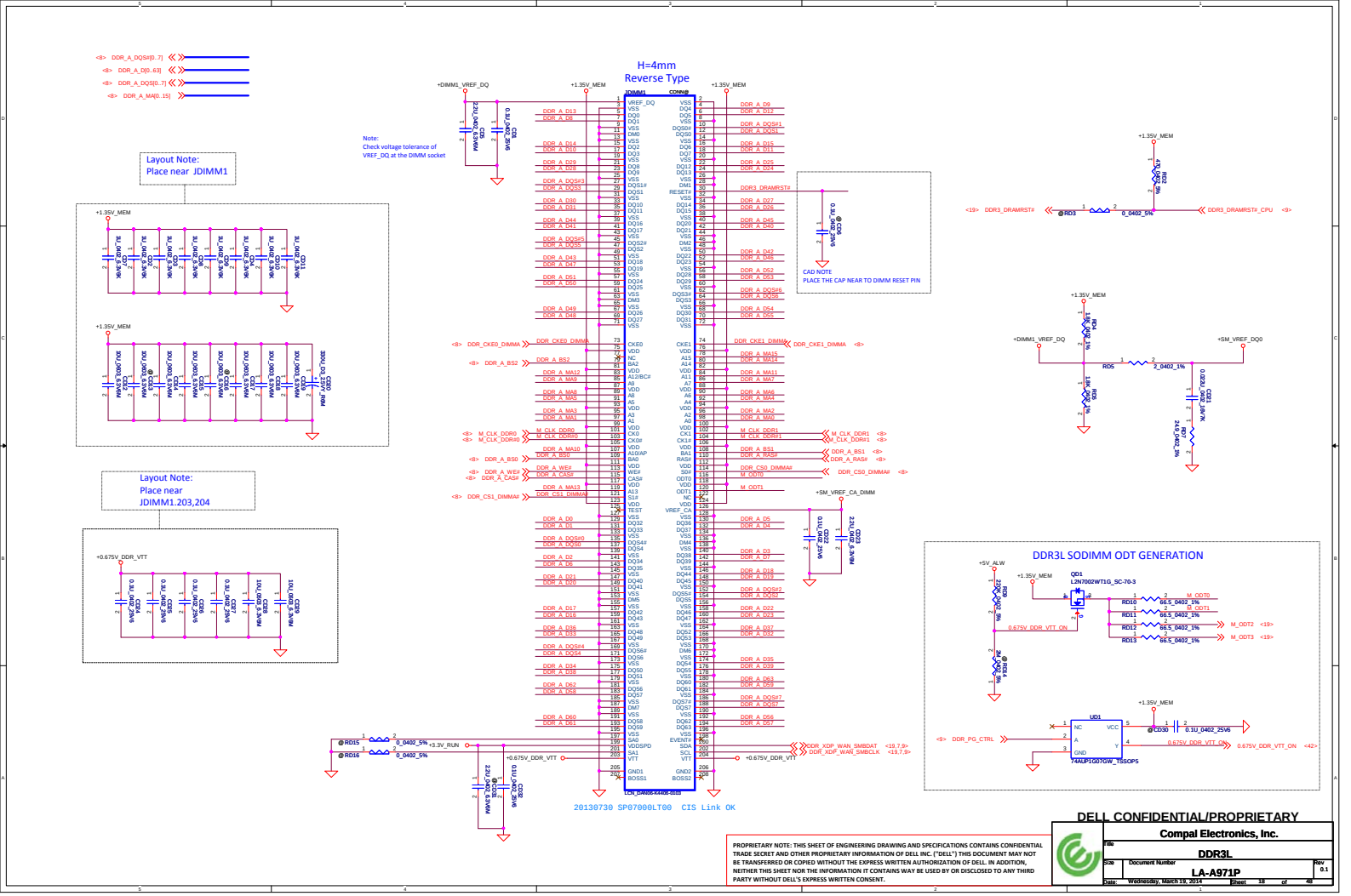

Compal Electronics, Inc.

Title: DDR3L

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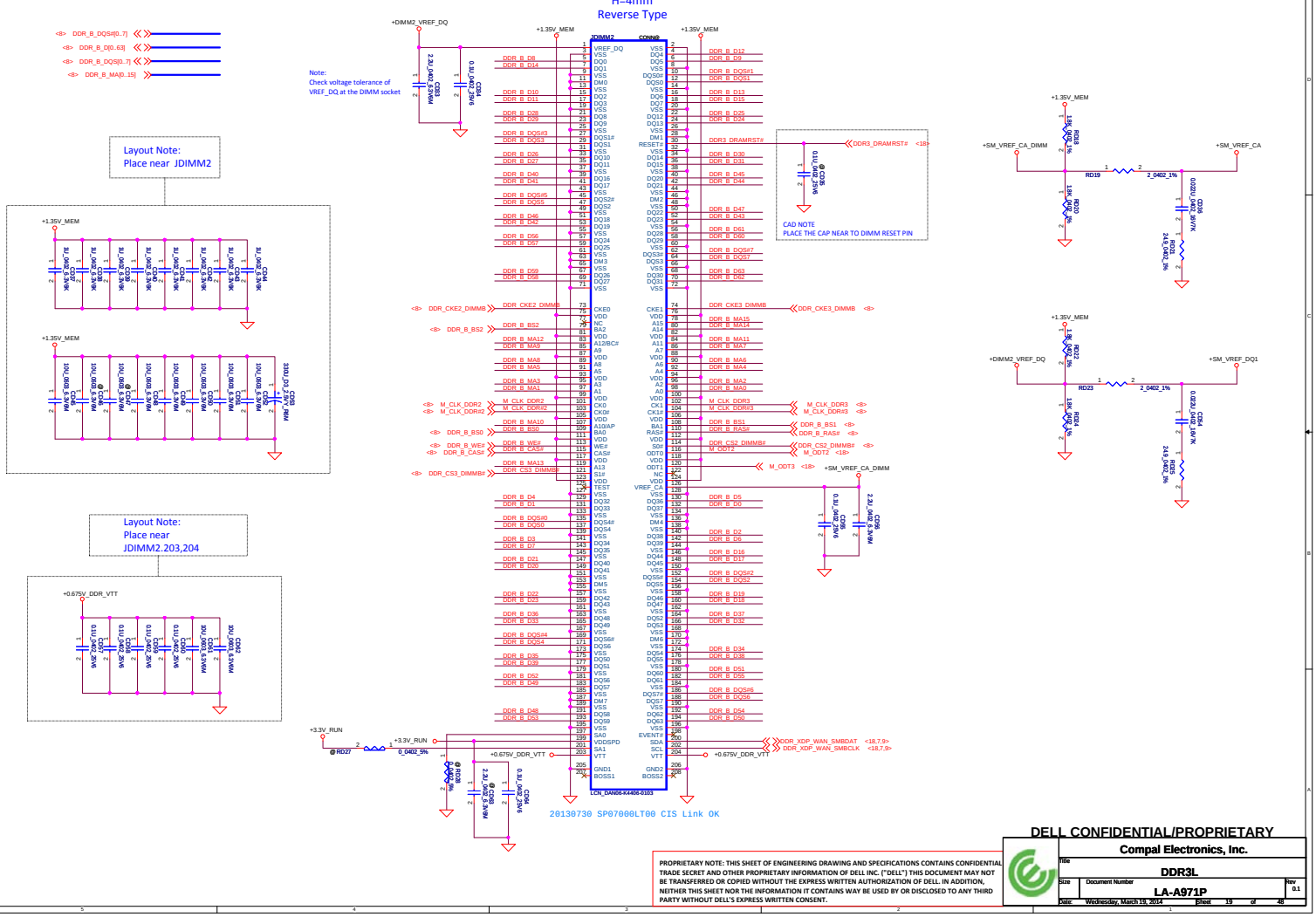

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Title	HDD CONN	
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1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

Internal Speakers Header

40 mils trace keep 20 mil spacing

CONN@ JSPK1 ACES_50279-0040N-001

20130806 CIS Link OK

Close to UA1

Close to UA1 pin6

BCLK: Audio serial data bus bit clock input/output

LRCK: Audio serial data bus word clock input/output

Verb table configures as 1 JD mode with internal 47K pull high to save external rBOM.

Place closely to Pin 13.

Add for solve pop noise and detect issue

Place closely to Pin 14 for DOCK only

Digital Mic (Goliad MLK no single Mic)

Realtek feedback
Prevent the Noise from Combo Jack while system entry into S3 / S4 /S5

Place CA29 close to Codec

Place CA12 & CA13 close to Audio Jack

EMI De-pop

Global Headset Combo Jack

HP-Out-Right

HP-Out-Left

Nokia-MIC

iPhone-MIC

Normal Open

CIS Link OK

Compal Electronics, Inc.

Title: Codec _ALC3235

Size: Document Number: LA-A971P Rev: 0.1

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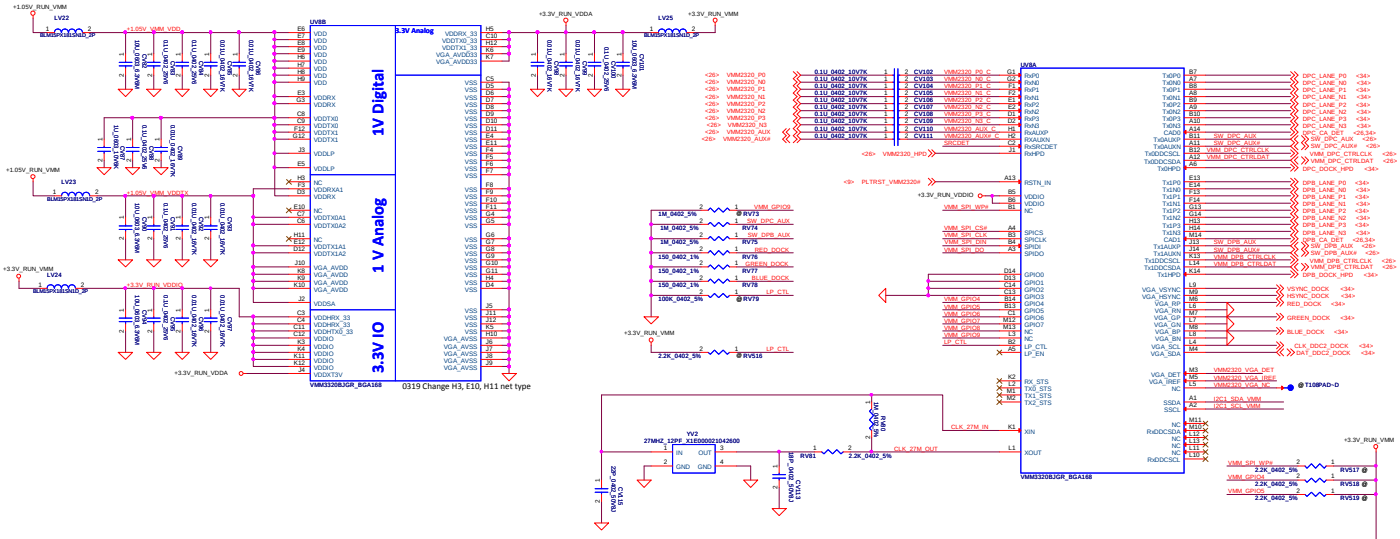
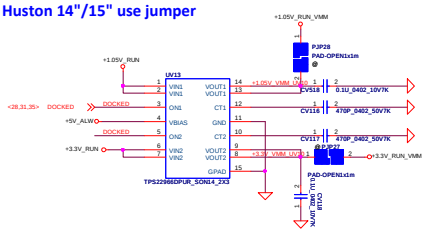
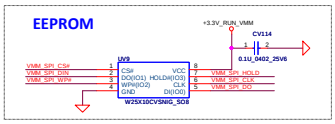
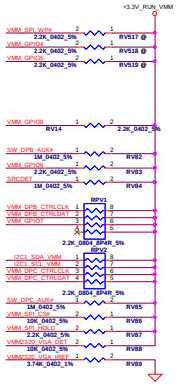


Goliad MLK should be use DOCKED to control TPS22966
Huston 14"/15" use jumper







Compal Electronics, Inc.

Title: DP 1.2 MST HUB

Size: | Document Number: LA-A971P | Rev: 0.1

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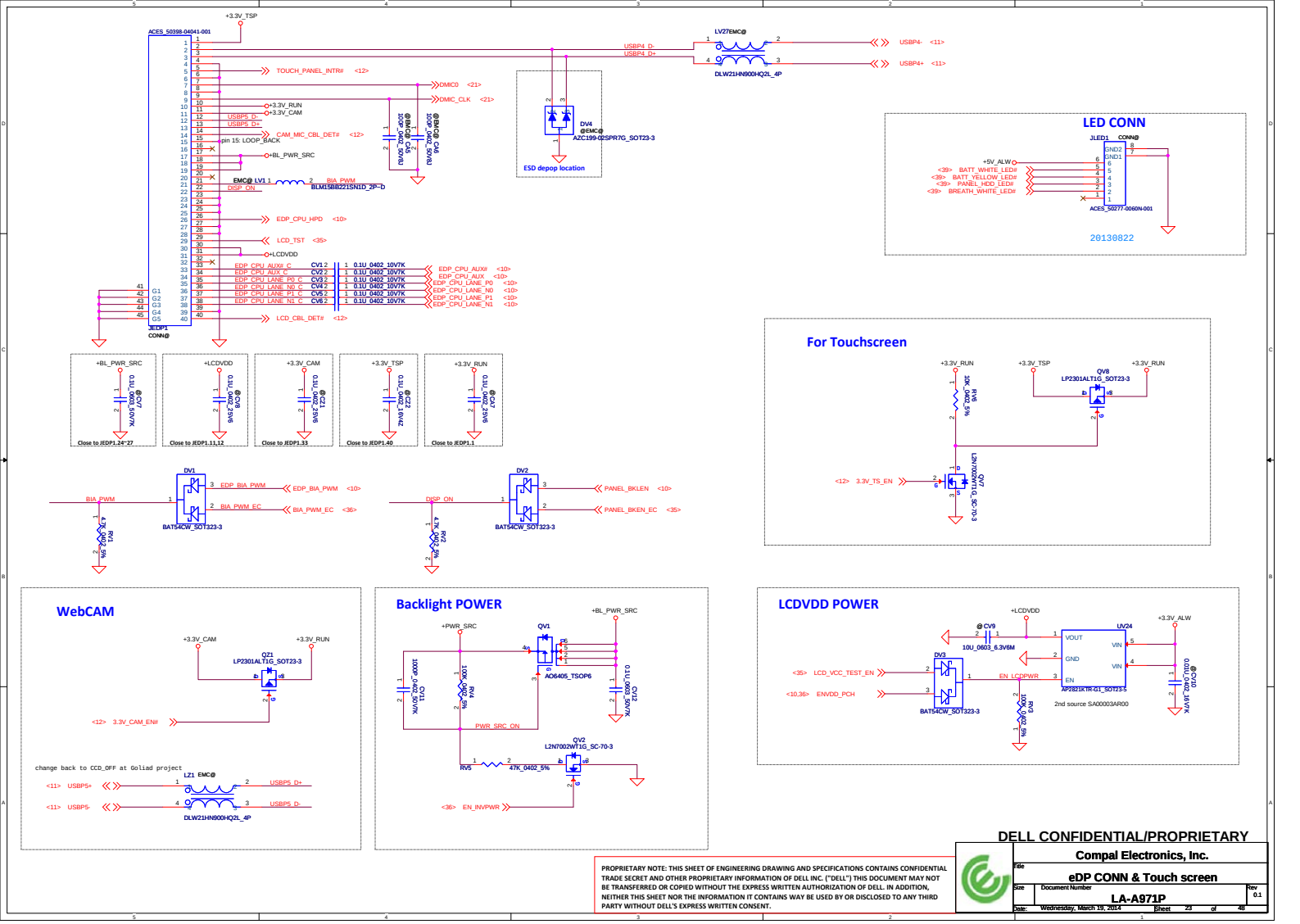

Compal Electronics, Inc.

Title: eDP CONN & Touch screen

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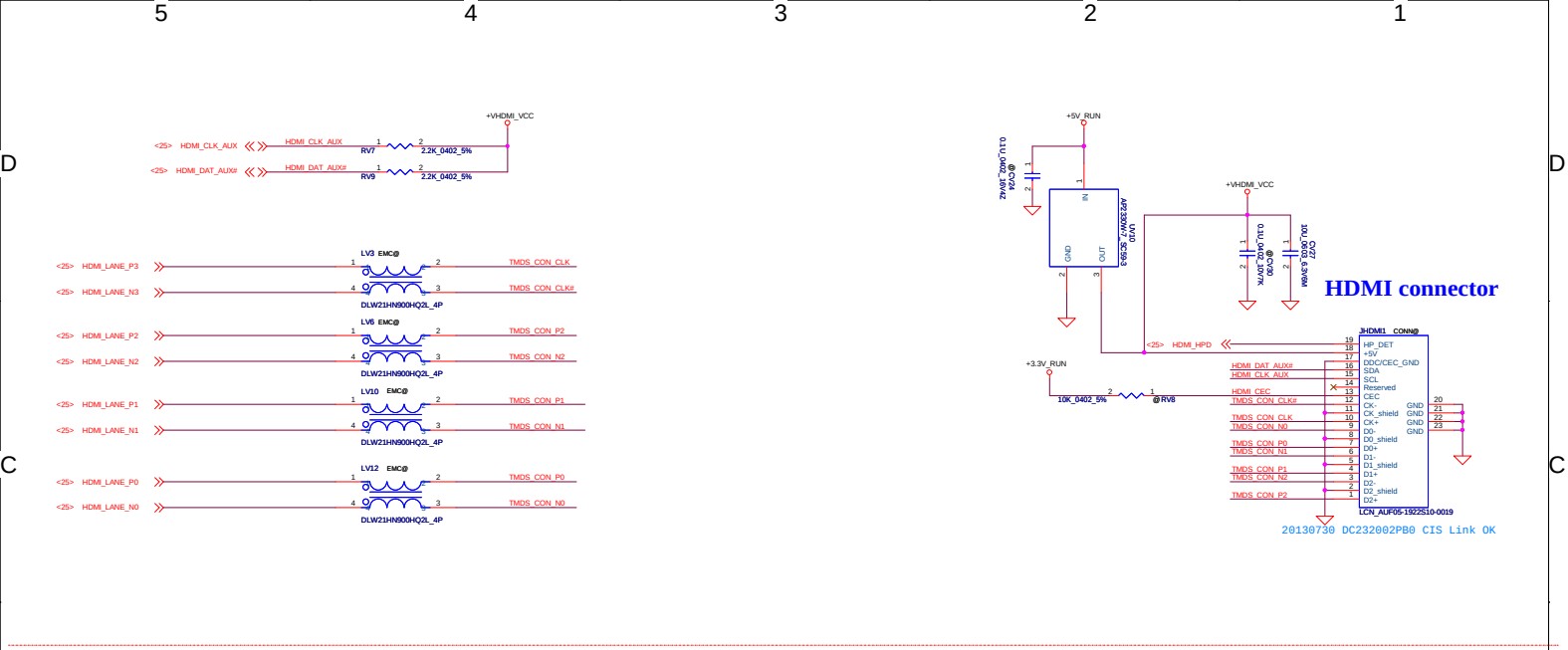

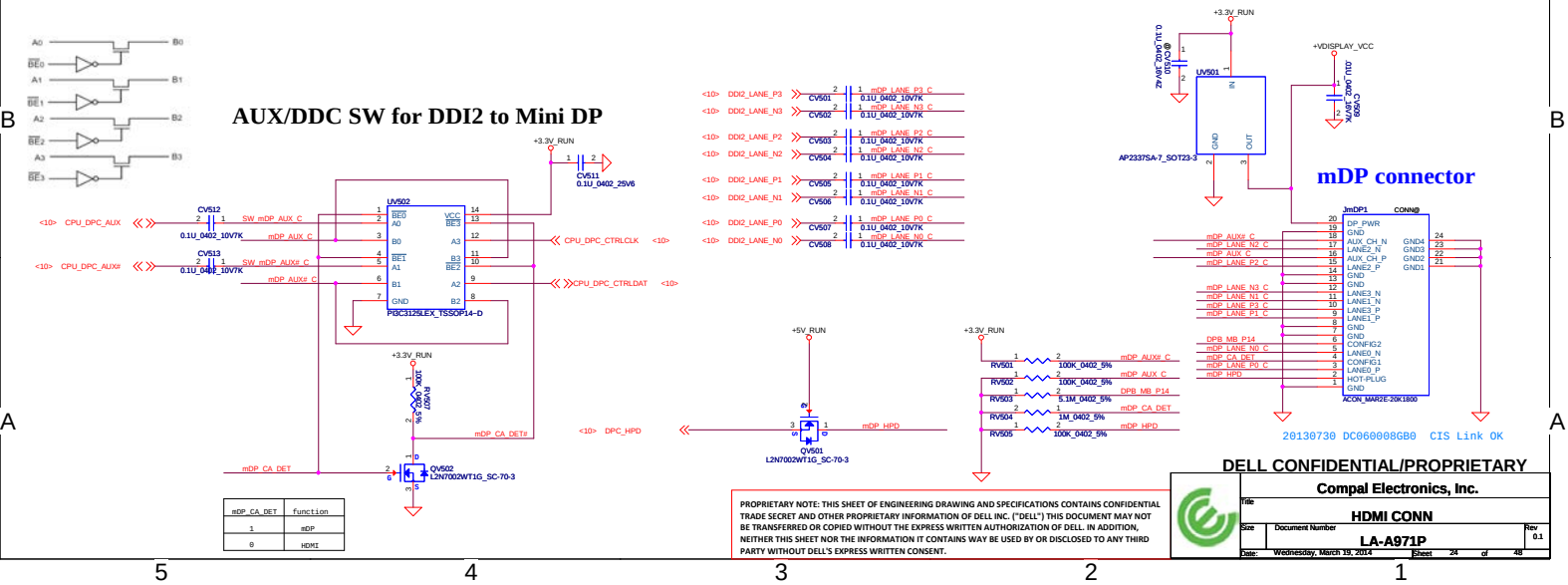

Compal Electronics, Inc.

Title: HDMI CONN

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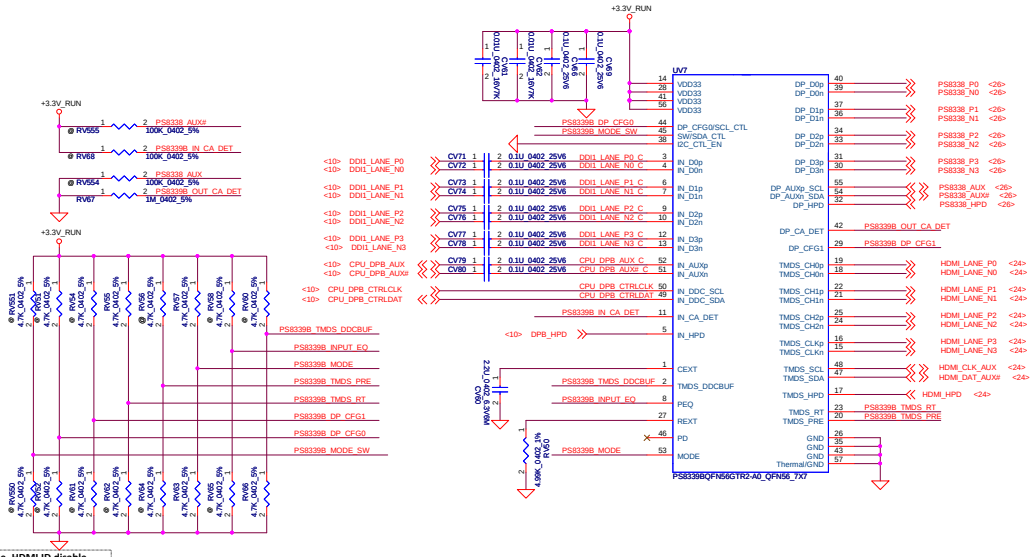
PCB	DP SWITCH
G12 UMA	PS8339+PS8338
G12 Entry	PS8339
G14 DSC	PS8339+PS8338
G14 UMA	PS8339
G14D_En	PS8339+PS8338
G14U_En	PS8339



MODE = L: Control Switching Mode, HDMI ID disable
= H: Automatic Switching Mode, HDMI ID disable
= M: Automatic Switching Mode, HDMI ID enable

TMDS_PRE = L: no pre-emphasis
= H: 1.5dB pre-emphasis
= M: 3.0dB pre-emphasis

TMDS_RT = L: Standard open drain driver
= H: Open drain driver with termination resistors

TMDS_DDCBUF = L: DDC pass through
= H: DDC active buffer
= M: DDC pass through with 40 kohm pull up resistor

PEQ = L: default, LEQ, compensate channel loss up to 12dB @ HBR2
= H: HEQ, compensate channel loss up to 15dB @ HBR2
= M: LLEQ, compensate channel loss up to 5dB @ HBR2

DP_CFG1 = L: default, auto test disable & input offset cancellation enable
= H: auto test enable & input offset cancellation enable
= M: auto test disable & input offset cancellation disable

DP_CFG0 = L: default, automatic EQ enable & AUX interception enable
= H: automatic EQ disable & AUX interception enable
= M: automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing

Compal Electronics, Inc.

Title: DP SW

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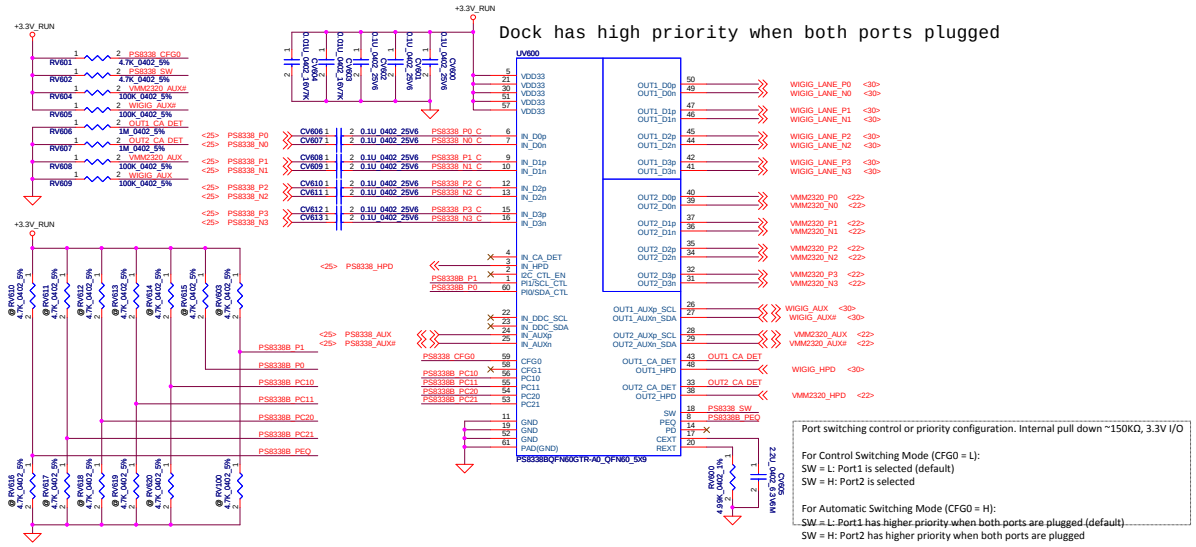
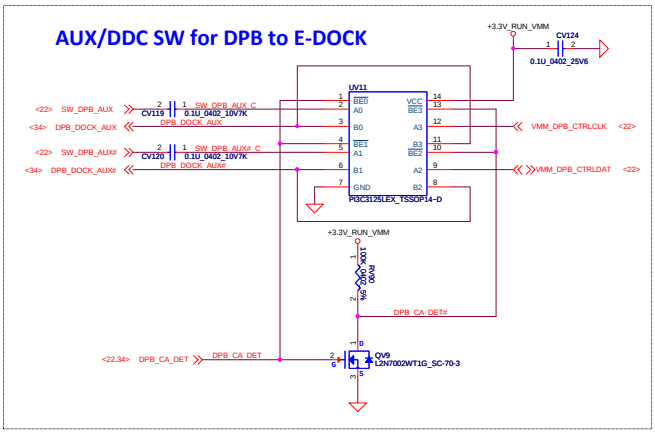
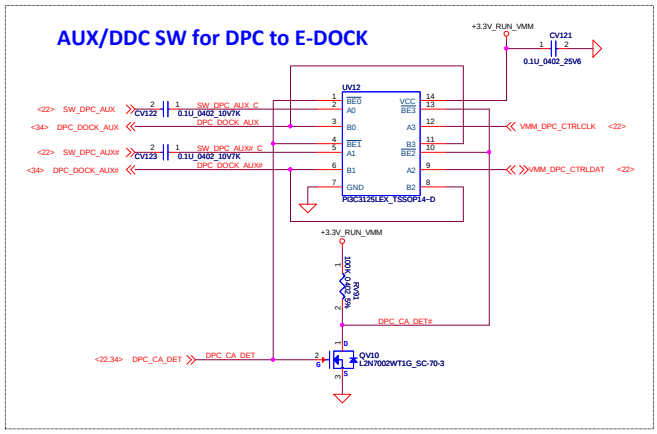
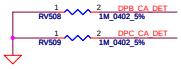
PCB	DP SWITCH
G12 UMA	PS8339+PS8338
G12 Entry	PS8339
G14 DSC	PS8339+PS8338
G14 UMA	PS8339
G14D_En	PS8339+PS8338
G14U_En	PS8339









Compal Electronics, Inc.

Title	DP SW	
Size	Document Number: LA-A971P	Rev: 0.1
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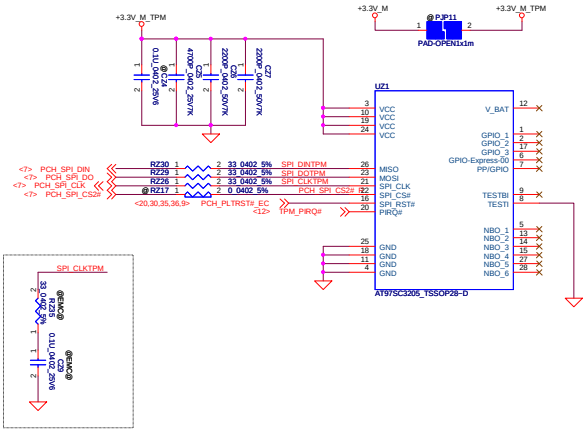
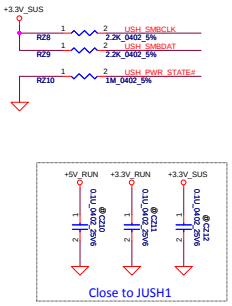
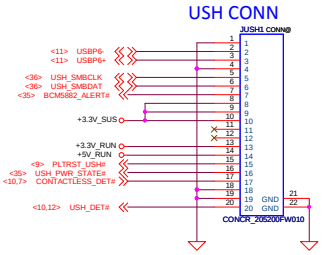




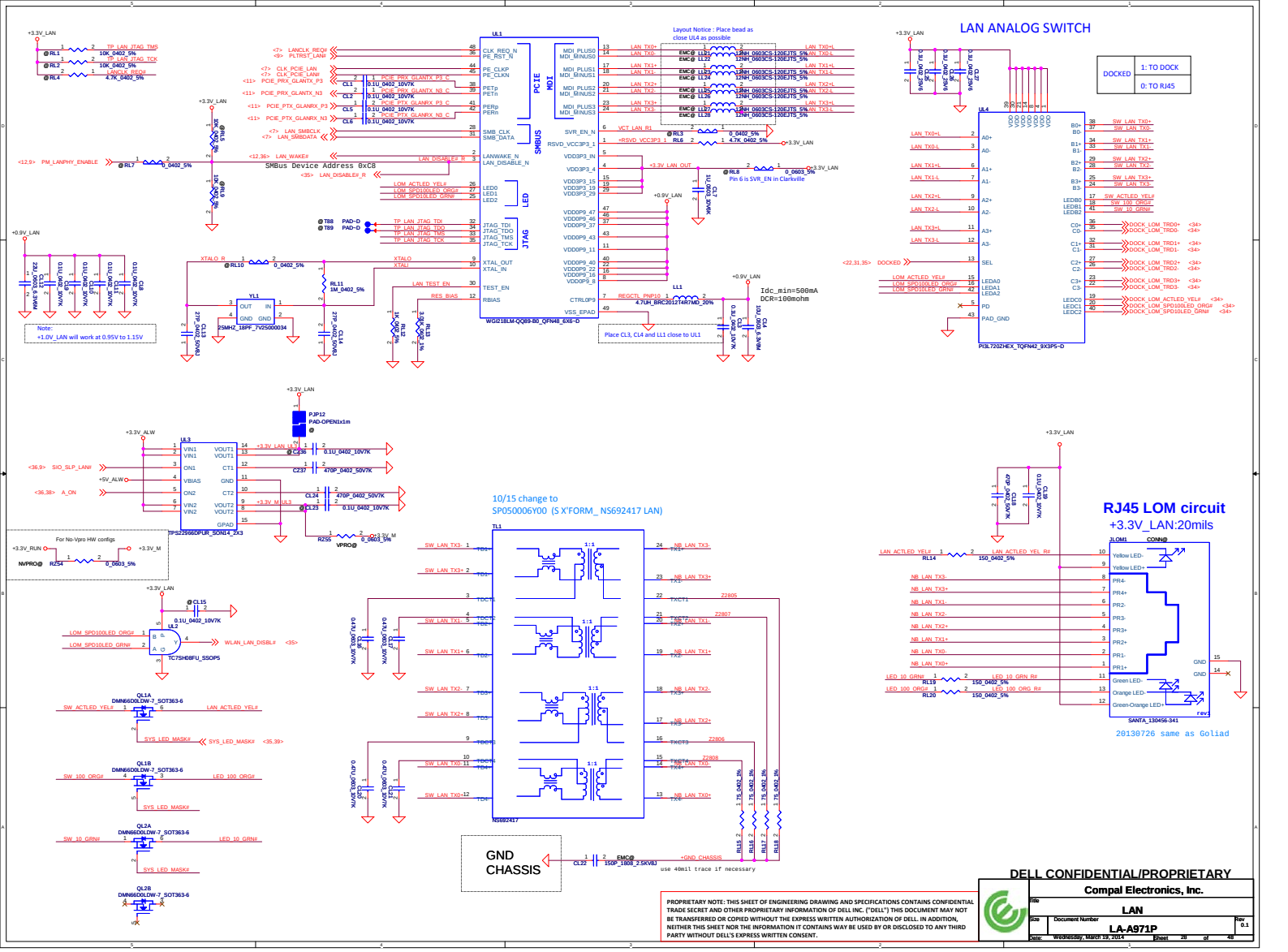


Compal Electronics, Inc.

Title: USH & TPM

Size | Document Number: LA-A971P | Rev: 0.1

Date: Wednesday, March 19, 2014 | Sheet 27 of 48



Compal Electronics, Inc.

Title: LAN

Size: — Document Number: LA-A971P — Rev: 0.1

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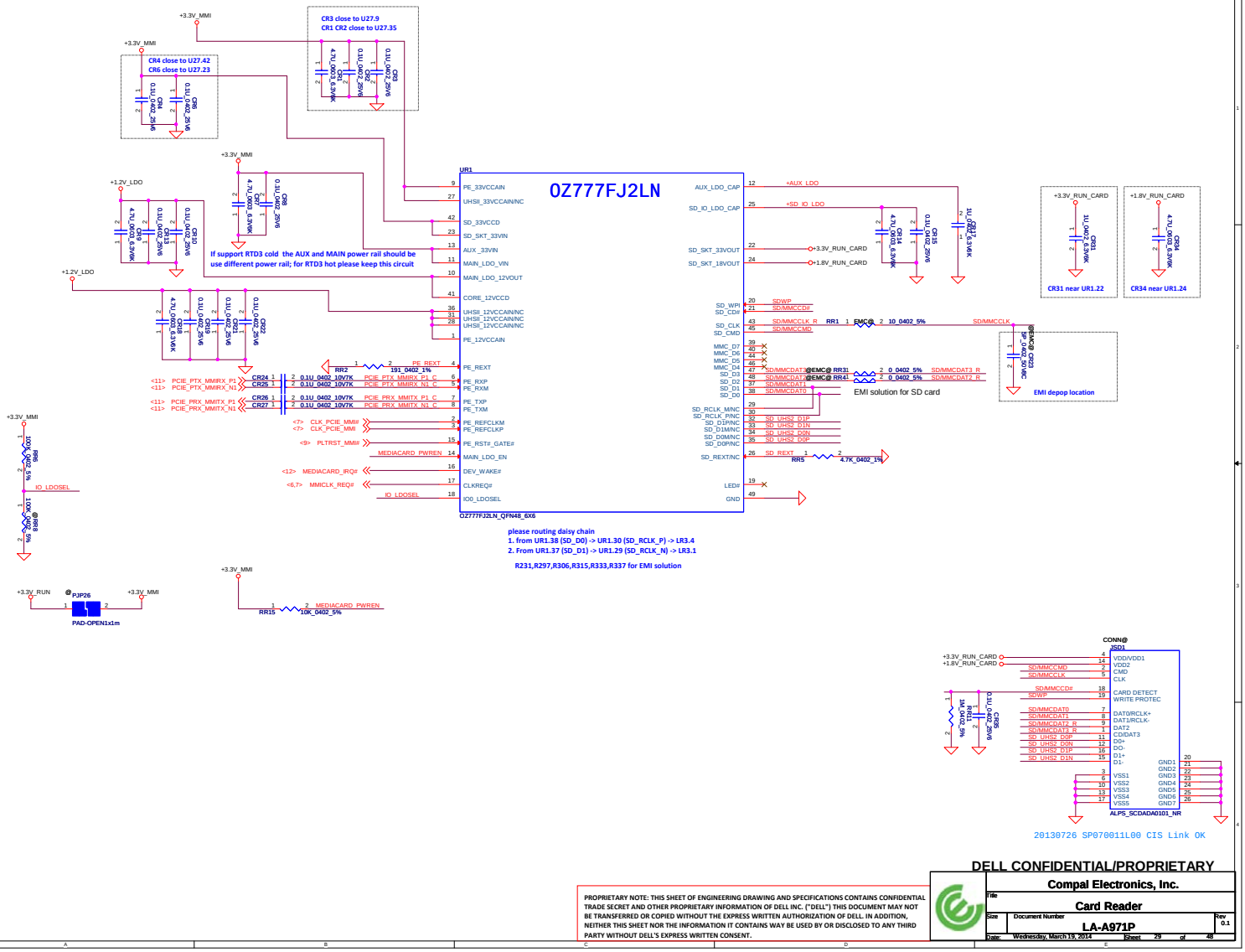

20130726 SP070011L00 CIS Link OK

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Compal Electronics, Inc.	
Title	Card Reader
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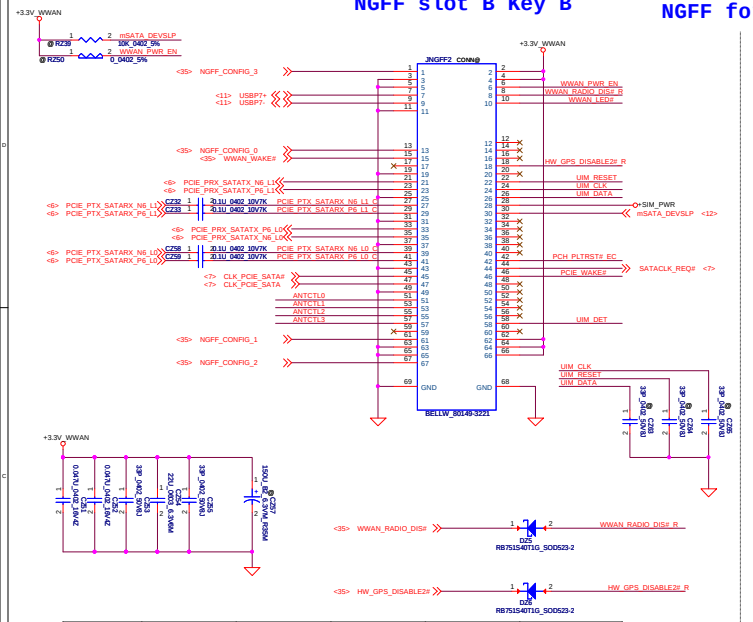
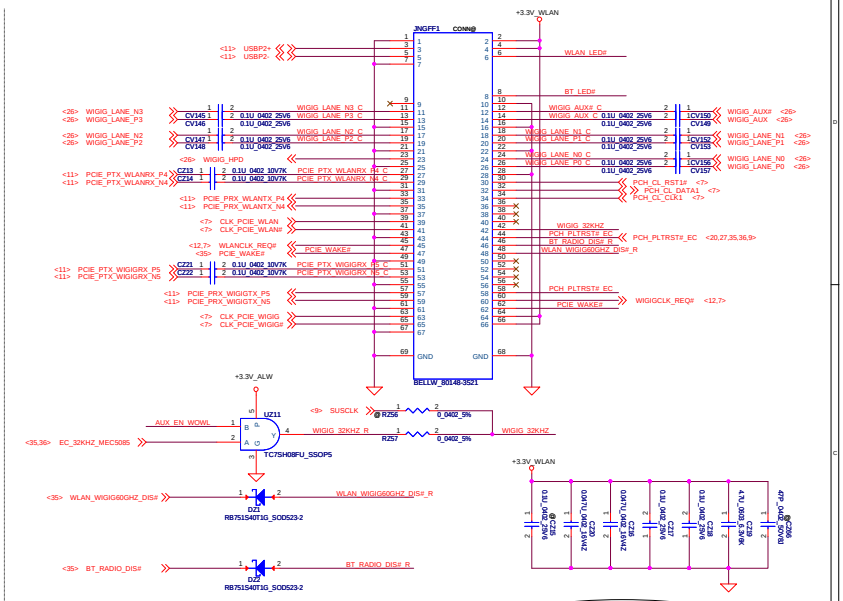
NGFF slot B Key B

NGFF for UMA

NGFF slot A Key A



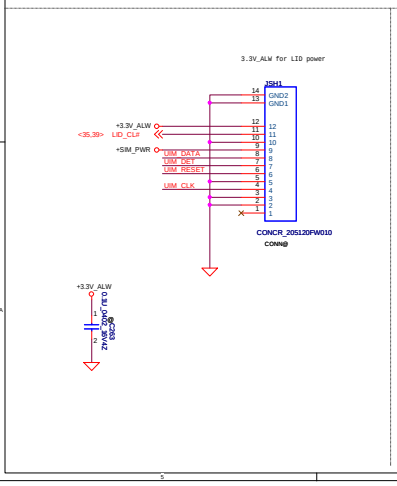


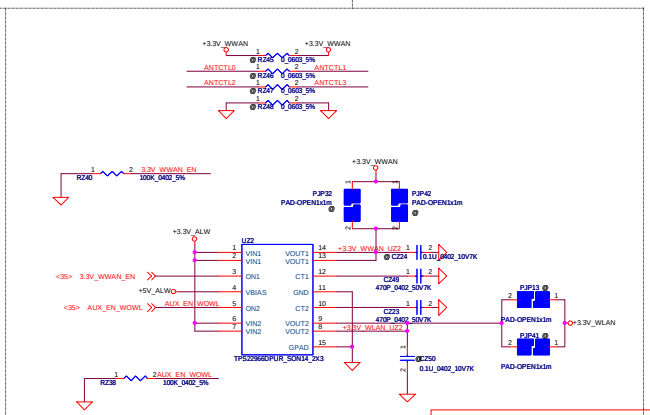
STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD-SATA
1	GND	HIGH	GND	GND	SSD-PCIE
8	HIGH	GND	GND	GND	WWAN
14	HIGH	GND	HIGH	HIGH	HCA-PCIE
15	HIGH	HIGH	HIGH	HIGH	NA

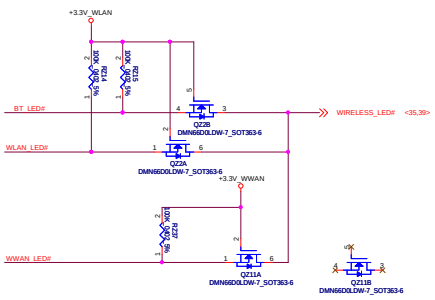
Power Rating TBD

PWR Rail	Voltage Tolerance	Primary Power		Aux Power
		Peak	Normal	Normal
+3.3V				

LED control circuit





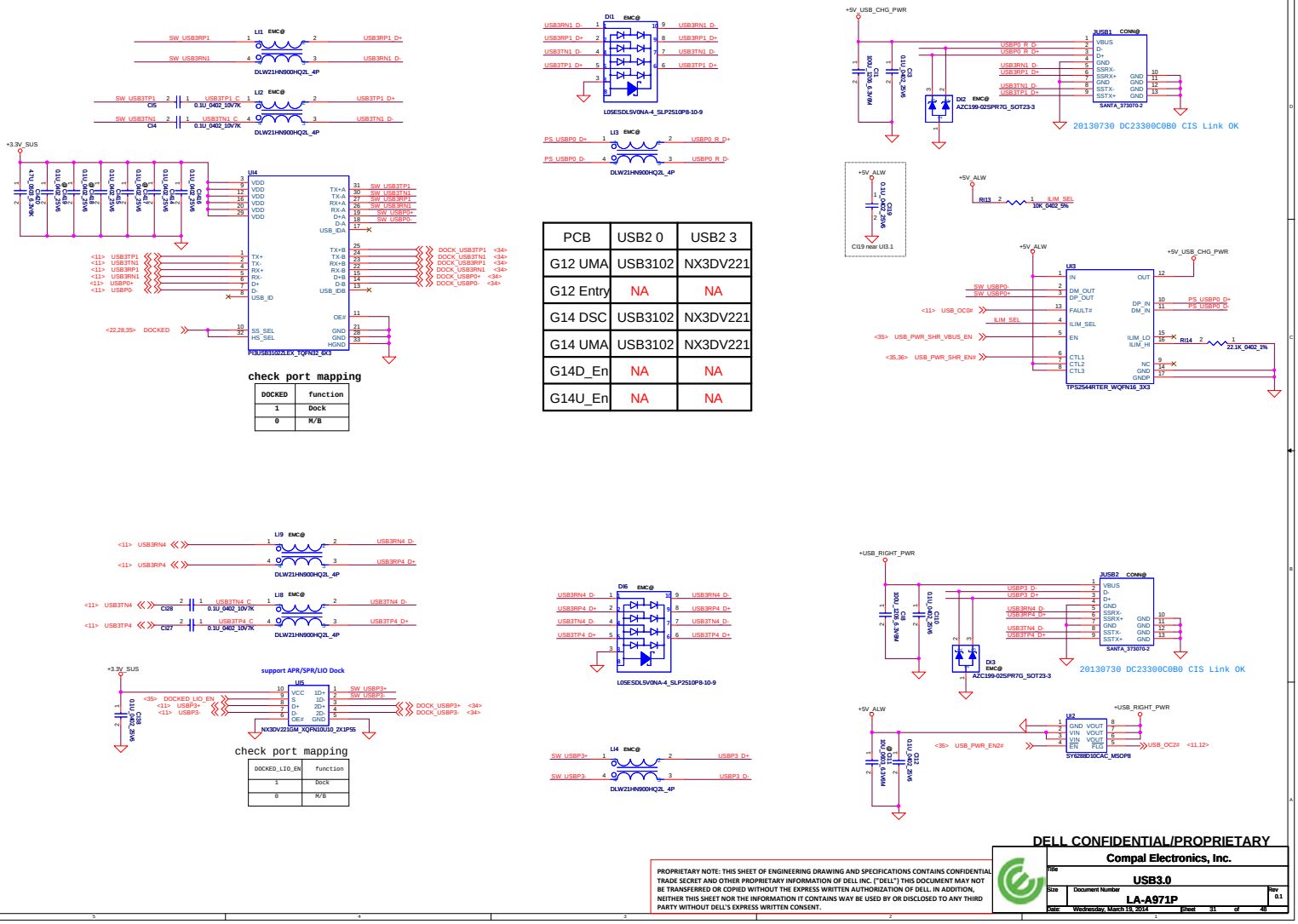


Compal Electronics, Inc.

Title: NGFF Card

Size: | Document Number: LA-A971P | Rev: 0.1

Date: Wednesday, March 19, 2014 | Sheet 30 of 40



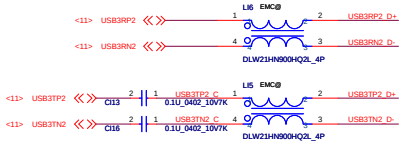
PCB	USB2 0	USB2 3
G12 UMA	USB3102	NX3DV221
G12 Entry	NA	NA
G14 DSC	USB3102	NX3DV221
G14 UMA	USB3102	NX3DV221
G14D_En	NA	NA
G14U_En	NA	NA

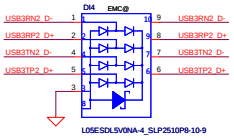
Compal Electronics, Inc.

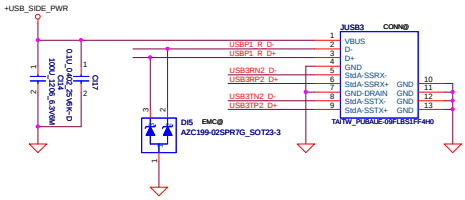
Title: USB3.0

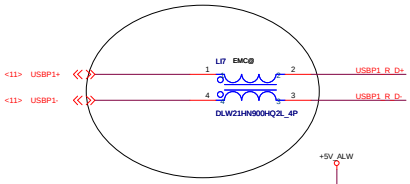
Size: | Document Number: LA-A971P | Rev: 0.1

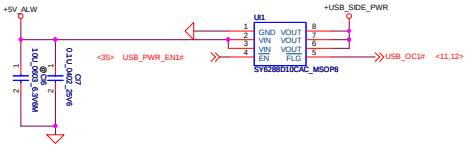
Date: Wednesday, March 19, 2014 | Sheet 31 of 48











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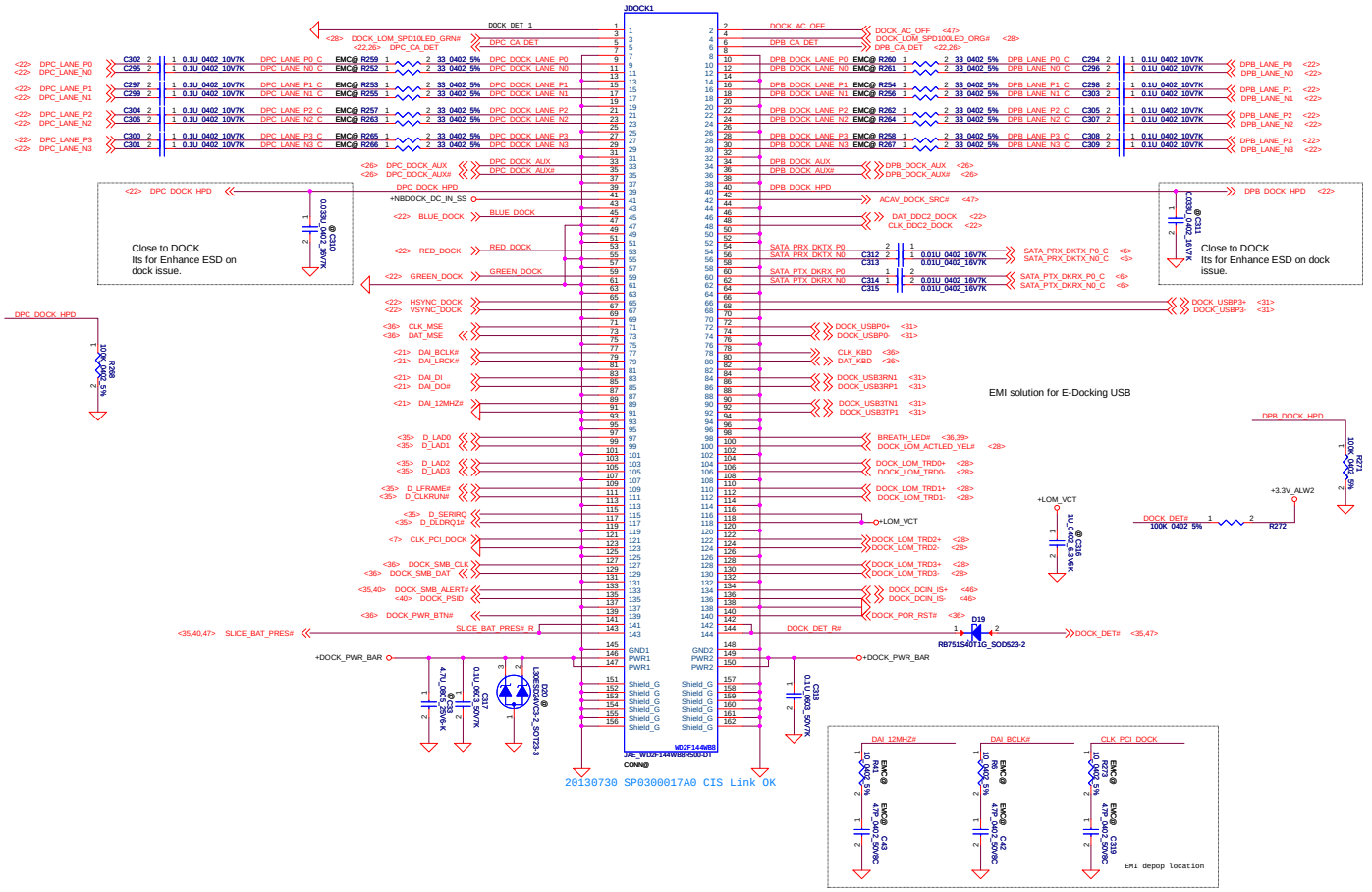
Compal Electronics, Inc.		
Title: USB SW		
Size	Document Number: LA-A971P	Rev: 0.1
Date: Wednesday, March 19, 2014	Sheet 32 of 48	

NFC on USH/B

DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: NFC		
Size	Document Number: LA-A971P	Rev: 0.1
Date: Wednesday, March 19, 2014	Sheet 33 of 48	



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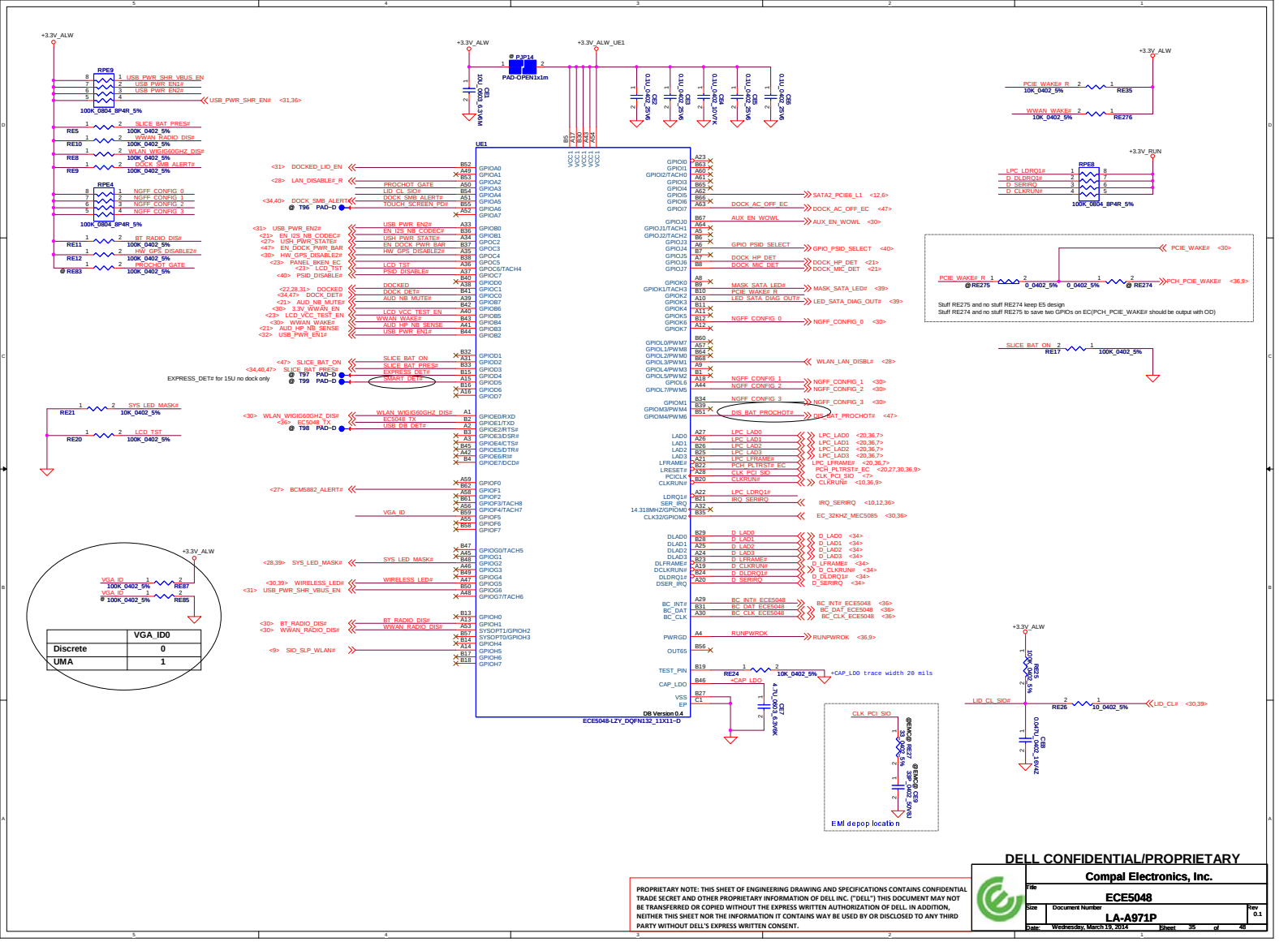
Compal Electronics, Inc.		
Title: E-Dock		
Size	Document Number: LA-A971P	Rev: 0.1
Date: Wednesday, March 19, 2014	Sheet 34 of 48	



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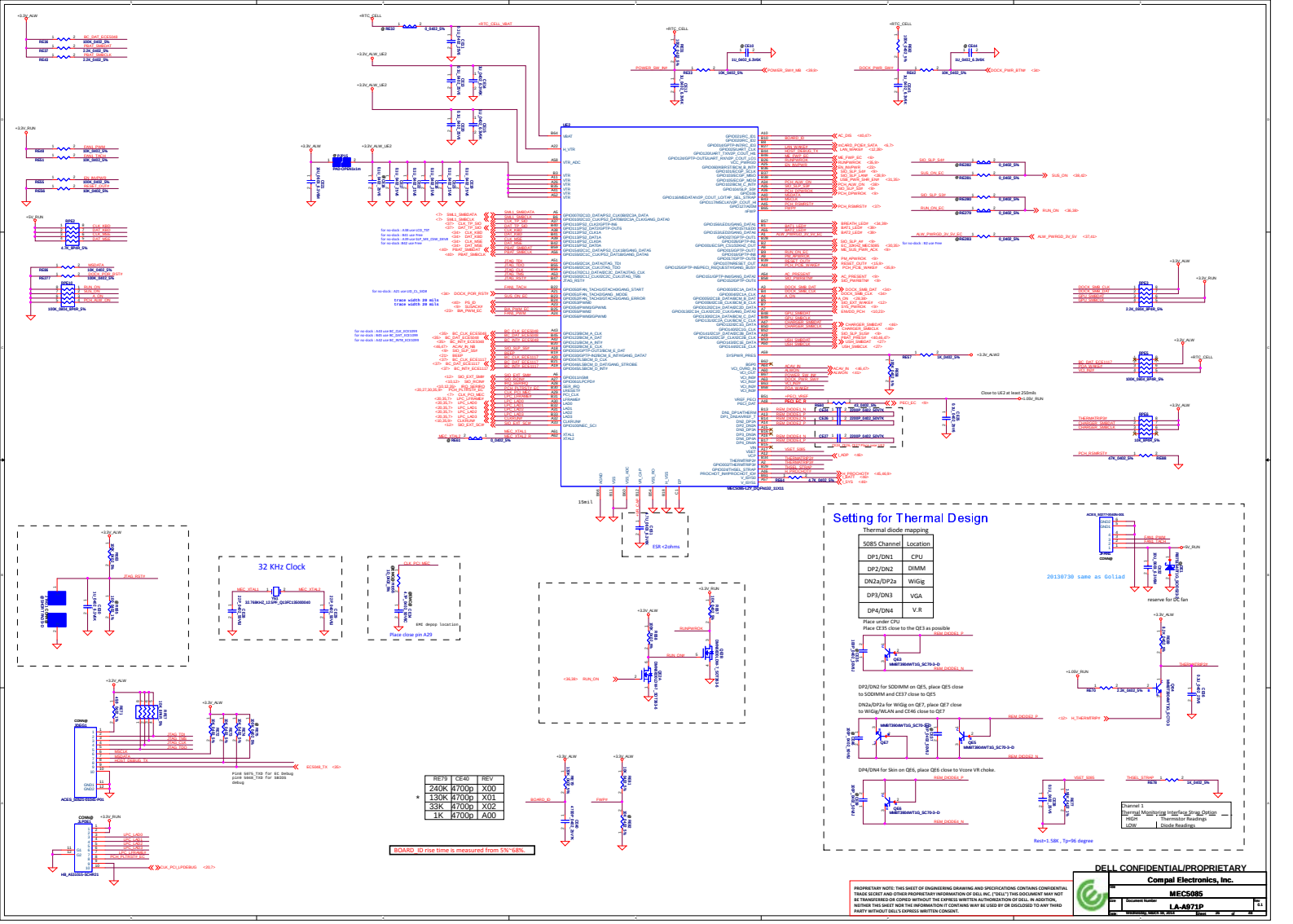
Compal Electronics, Inc.	
Title	ECE5048
Size	Document Number: LA-A971P
Rev	0.1
Date: Wednesday, March 19, 2014	Sheet 35 of 48



Setting for Thermal Design

Thermal diode mapping

5085 Channel	Location
DP1/DN1	CPU
DP2/DN2	DIMM
DN2a/DP2a	WiGig
DP3/DN3	VGA
DP4/DN4	V.R

Place under CPU
Place CE35 close to the QE3 as possible

DP2/DN2 for SDDIMM on QE5, place QE5 close to SDDIMM and CE37 close to QE5

DN2a/DP2a for WiGig on QE7, place QE7 close to WiGig/WLAN and CE46 close to QE7

DP4/DN4 for Skin on QE6, place QE6 close to Vcore VR choke.

RE'9	CE40	REV
240K	4700p	X00
130K	4700p	X01
33K	4700p	X02
1K	4700p	A00

BOARD_ID rise time is measured from 5%~68%.

Channel 1
Thermal Monitoring Interface Smsg Option

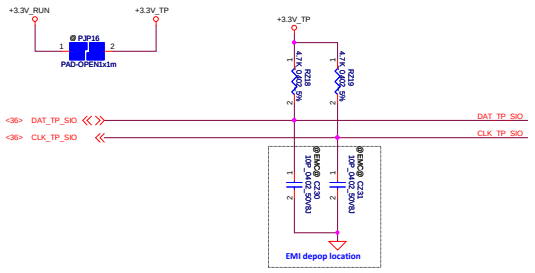
Thermistor Readings	Diode Readings
HIGH	
LOW	

Rest=1.58K , Tp=96 degree

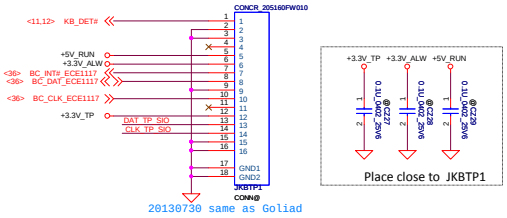
Compal Electronics, Inc.

Size	Document Number	Rev
	MEC5085	0.1
	LA-A971P	
Date:	Wednesday, March 06, 2013	Sheet 39 of 68

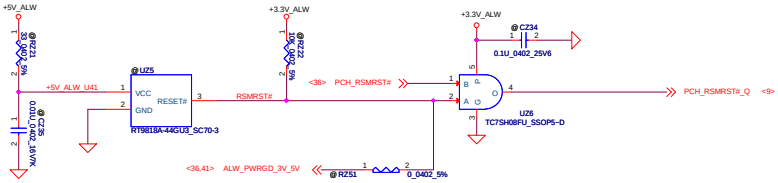
Touch Pad



Keyboard



RSMRST circuit



@IO FFC

Part Number	Description
DA30000GZ00	FPC 0VN LF-9591P REV0 M/B-IO/B

@eDP TS Cable

Part Number	Description
DC02C004S00	H-CONN SET 0VN MB-LCD-LED-CAM-TS

@eDP Cable

Part Number	Description
DC02C004T00	H-CONN SET 0VN MB-LCD-LED-CAM

@SATA Cable

Part Number	Description
DC02C004K00	H-CONN SET 0VN MB-HDD

@DC-IN Cable

Part Number	Description
DC30100MF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@RTC BATT

Part Number	Description
DC3010GMF00	CONN SET 0VN DCJACK-MB 2DW1003-038110F

@FAN

Part Number	Description
DC28A000B00	FAN SET DAQ20 DC5V AB7405HB-HB3 ADDA

@MEDIA Board FFC

Part Number	Description
NBX0001CW00	FFC 8P G P0.5 PAD0.3 50MM MB-MEDIA/B 0VN

@KBTP FFC

Part Number	Description
NBX0001CZ00	FFC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

@NFC Board FFC

Part Number	Description
NBX0001CZ00	FFC 15P G P.5 PAD.3 85MM MB-NFC MODU 0VN

@USH Board FFC

Part Number	Description
NBX0001CY00	FFC 20P G P0.5 PAD=0.3 75MM MB-USH/B 0VN

@FP FFC

Part Number	Description
NBX0001D100	FFC 6P G P0.5 PAD=0.3 75MM USH/B-FP 0VN

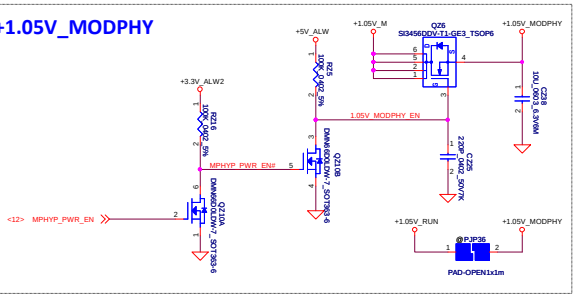
@Speak

Part Number	Description
PK230003Q0L	SPK PACK ZJX 2.0W 4 OHM FG

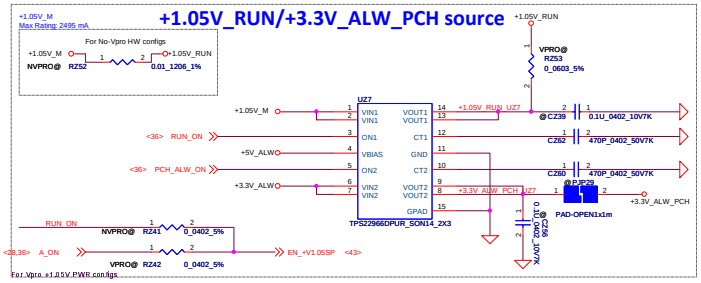
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.		
Title: Keyboard		
Size	Document Number: LA-A971P	Rev: 0.1
Date: Wednesday, March 19, 2014	Sheet 37 of 48	

+1.05V_MODPHY

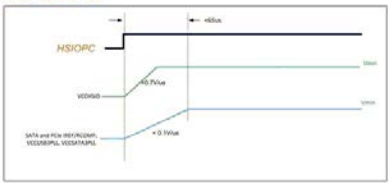


+1.05V_RUN/+3.3V_ALW_PCH source

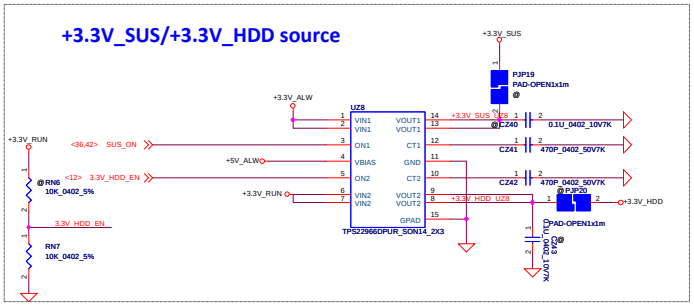


if support MODPHY off keep DSC solution
MODPHY timing spec 0.7V/us and <65us

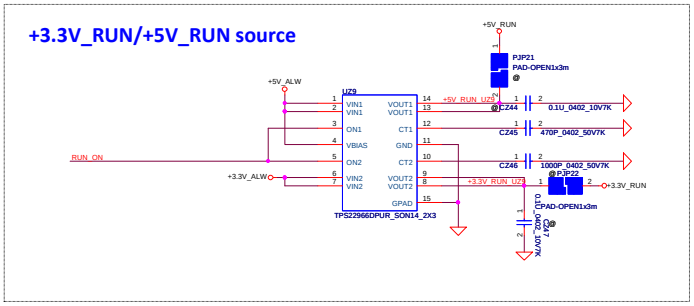
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



+3.3V_SUS/+3.3V_HDD source



+3.3V_RUN/+5V_RUN source



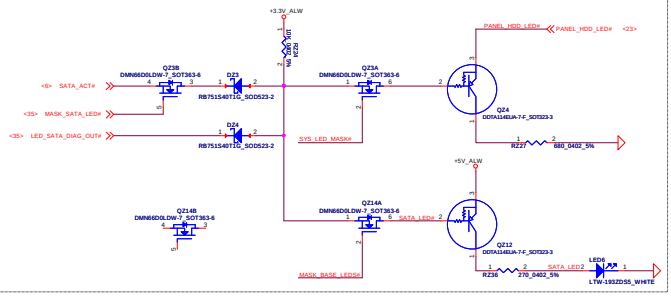
Compal Electronics, Inc.

Title: Power control

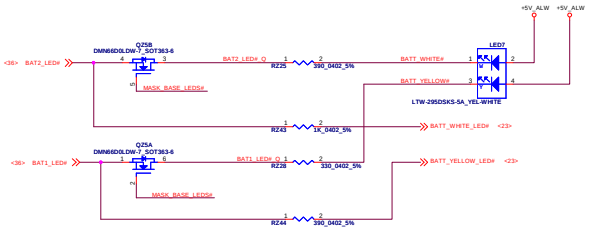
Size: | Document Number: LA-A971P | Rev: 0.1

Date: Wednesday, March 19, 2014 | Sheet 38 of 48

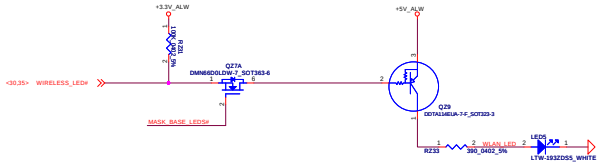
HDD LED solution for White LED



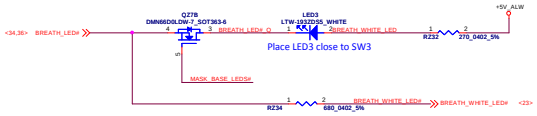
Battery LED

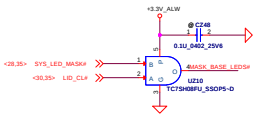


WLAN LED solution for White LED

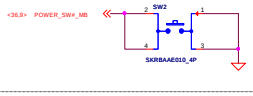


Breath LED





POWER & INSTANT ON SWITCH

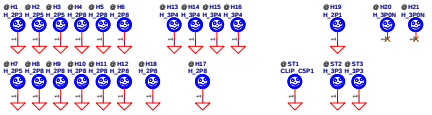


LED Circuit Control Table

	SYS_LED_MASK#	LID_CL#
Mask All LEDs (Sniffer Function)	0	X
Mask Base MB LEDs (Lid Closed)	1	0
Do not Mask LEDs (Lid Opened)	1	1

Fiducial Mark

FD1 FIDUCIAL MARK~D
FD2 FIDUCIAL MARK~D
FD3 FIDUCIAL MARK~D
FD4 FIDUCIAL MARK~D

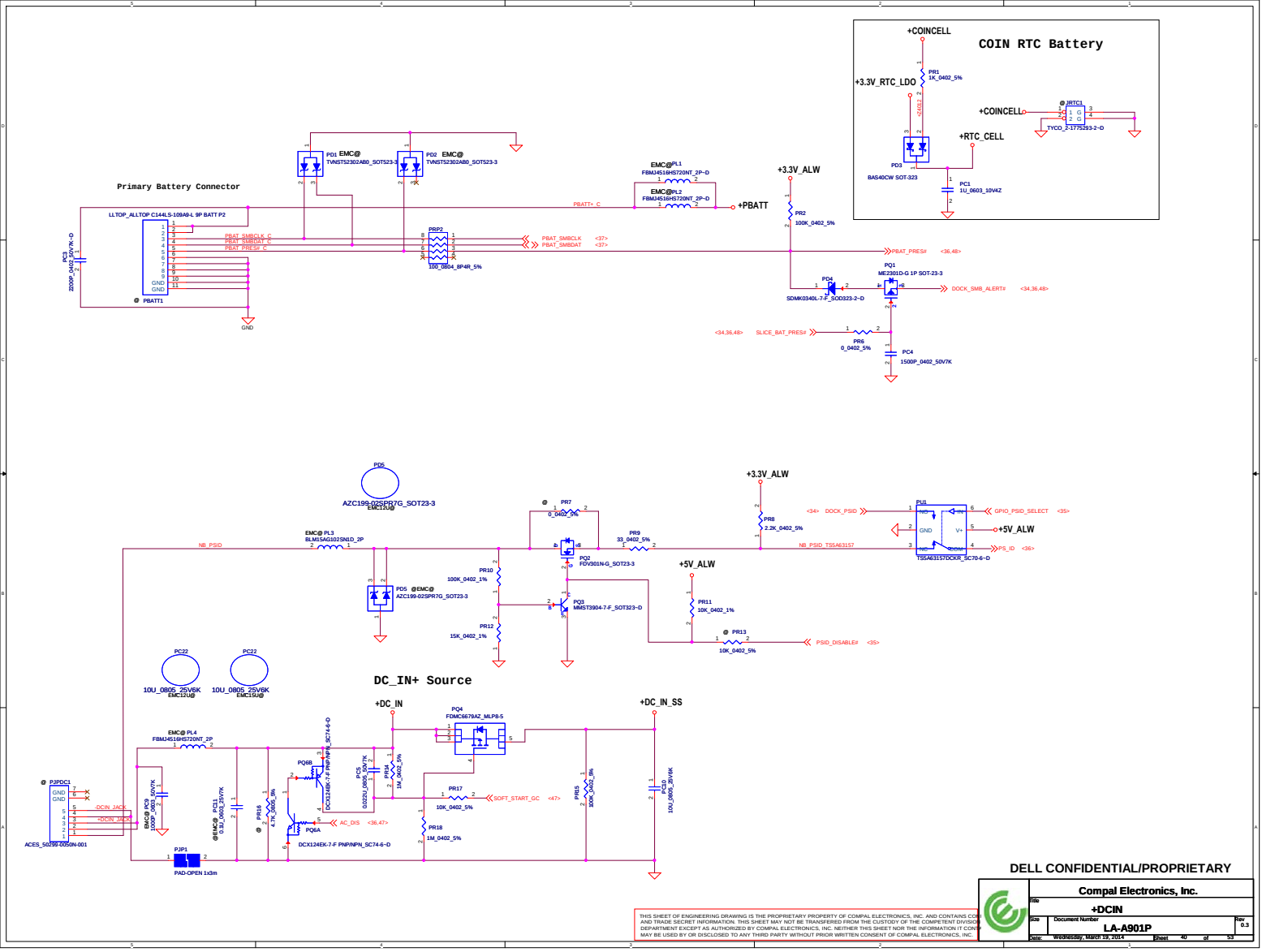


Compal Electronics, Inc.

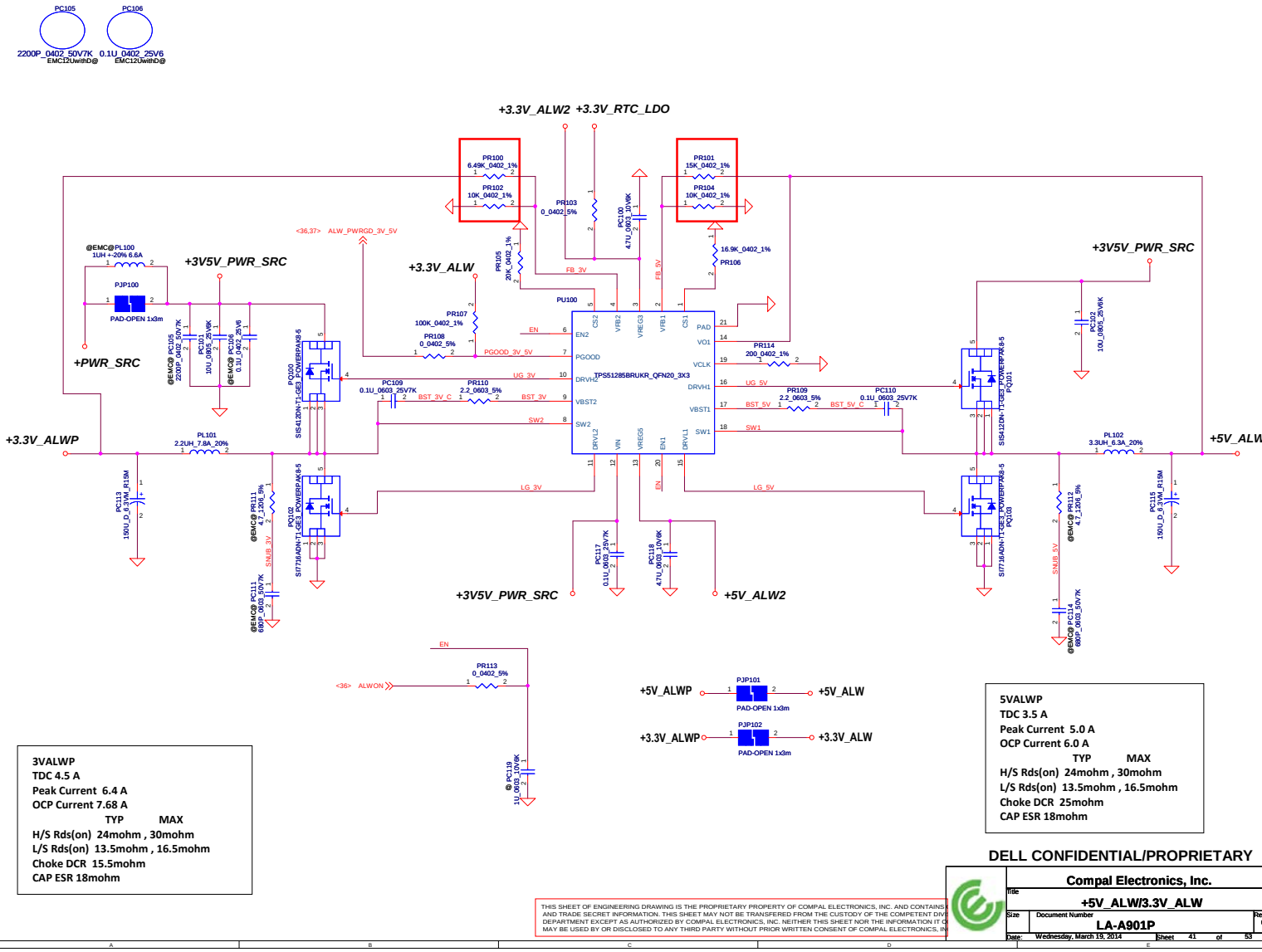
Title: PAD, LED

Size: | Document Number: LA-A971P | Rev: 0.1

Date: Wednesday, March 19, 2014 | Sheet 39 of 48



Compal Electronics, Inc.		
Title: +DCIN		
Size	Document Number: LA-A901P	Rev: 0.3
Date: Wednesday, March 19, 2014	Sheet 40 of 53	



3VALWP
TDC 4.5 A
Peak Current 6.4 A
OCP Current 7.68 A

	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	15.5mohm	
CAP ESR	18mohm	

5VALWP
TDC 3.5 A
Peak Current 5.0 A
OCP Current 6.0 A

	TYP	MAX
H/S Rds(on)	24mohm	30mohm
L/S Rds(on)	13.5mohm	16.5mohm
Choke DCR	25mohm	
CAP ESR	18mohm	

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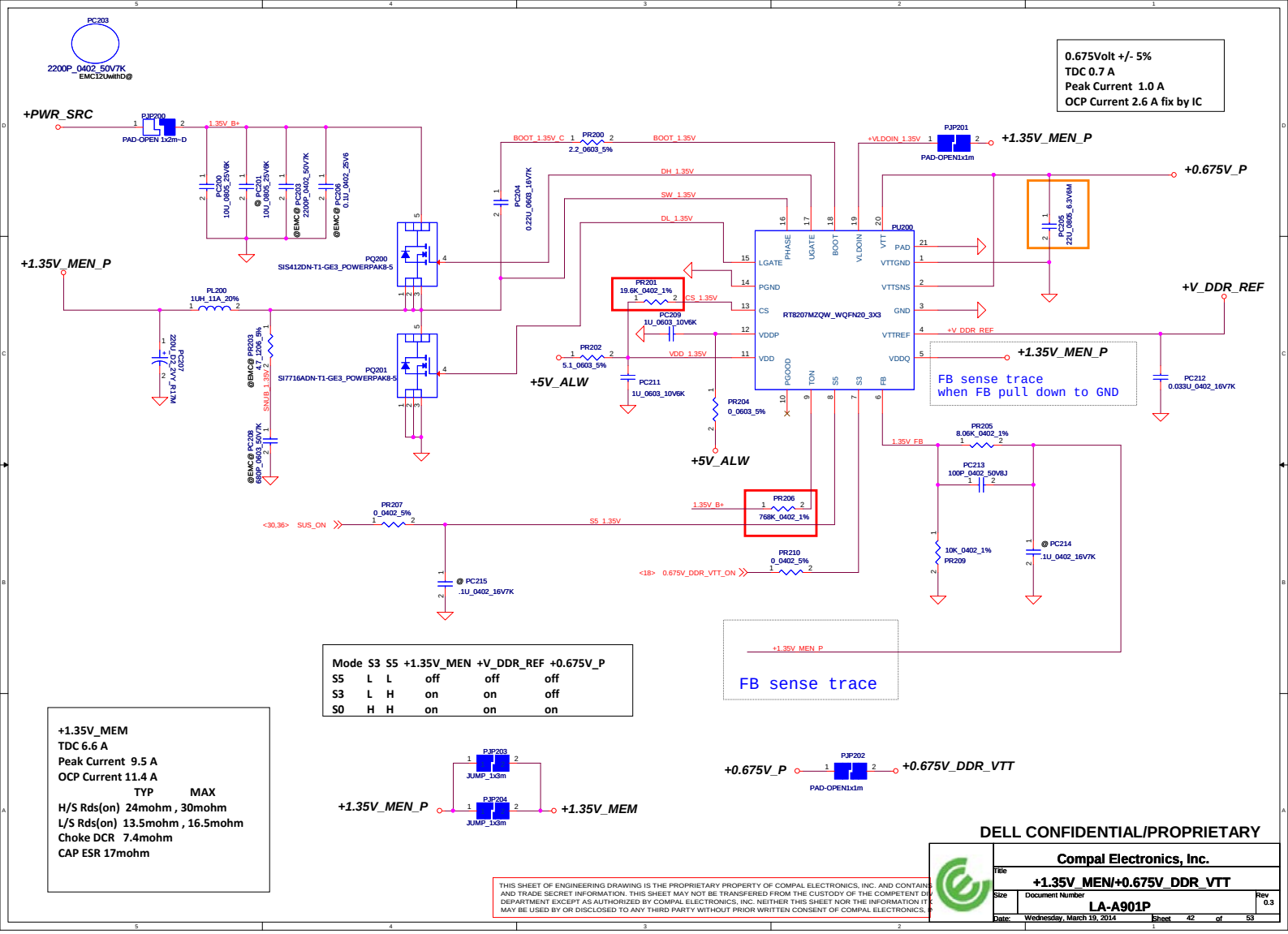
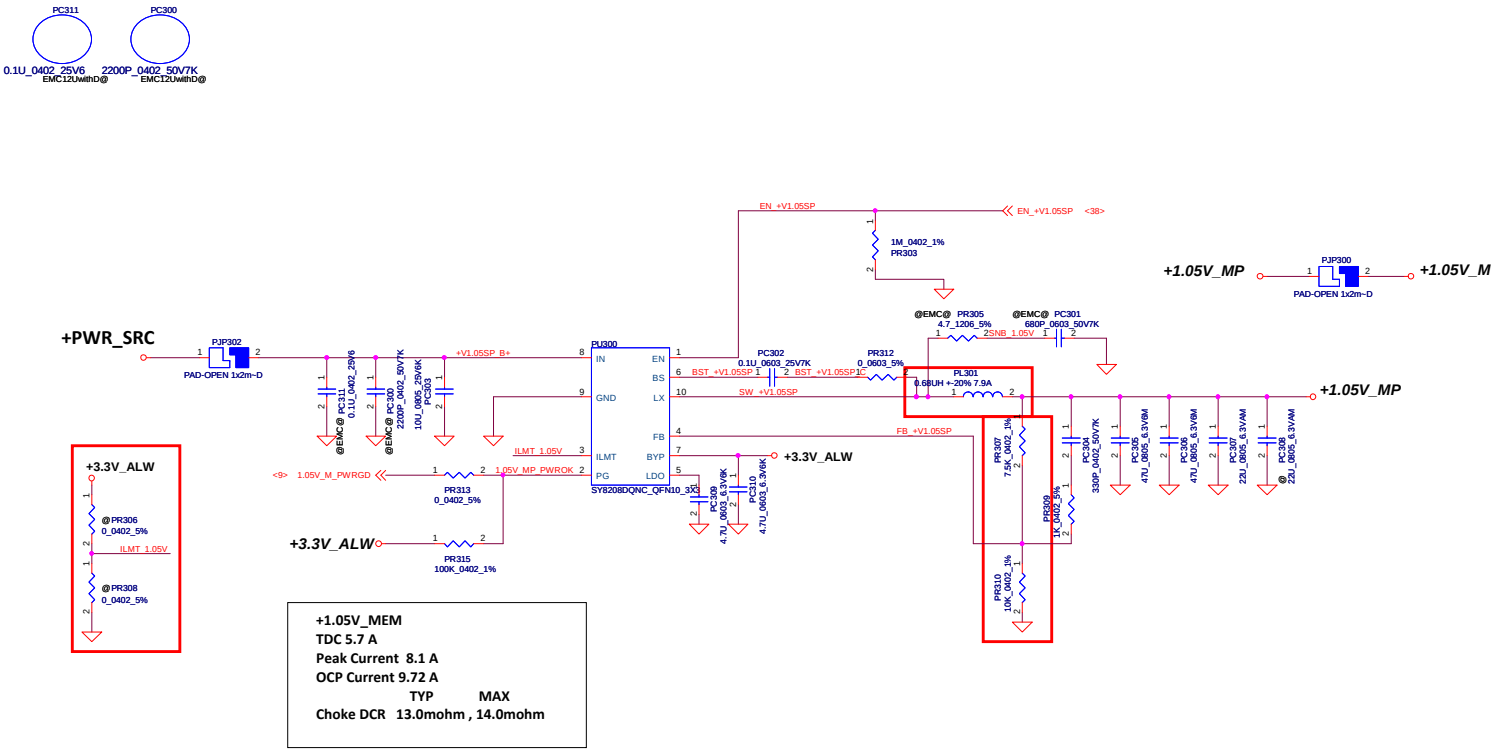
Compal Electronics, Inc.

Title	+5V_ALW/3.3V_ALW	
Size	Document Number	Rev
	LA-A901P	0.3
Date: Wednesday, March 19, 2014	Sheet 41 of 53	





Compal Electronics, Inc.	
Title	+1.05V_M
Size	Document Number: LA-A901P
Rev	0.3
Date:	Wednesday, March 19, 2014
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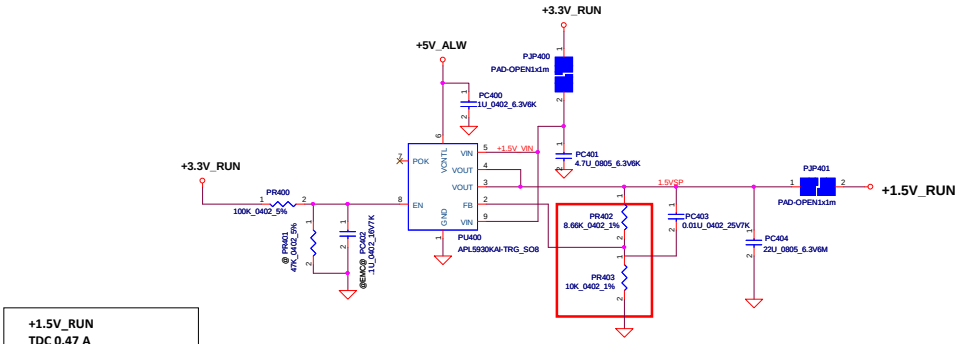

+1.5V_RUN
TDC 0.47 A
Peak Current 0.67 A

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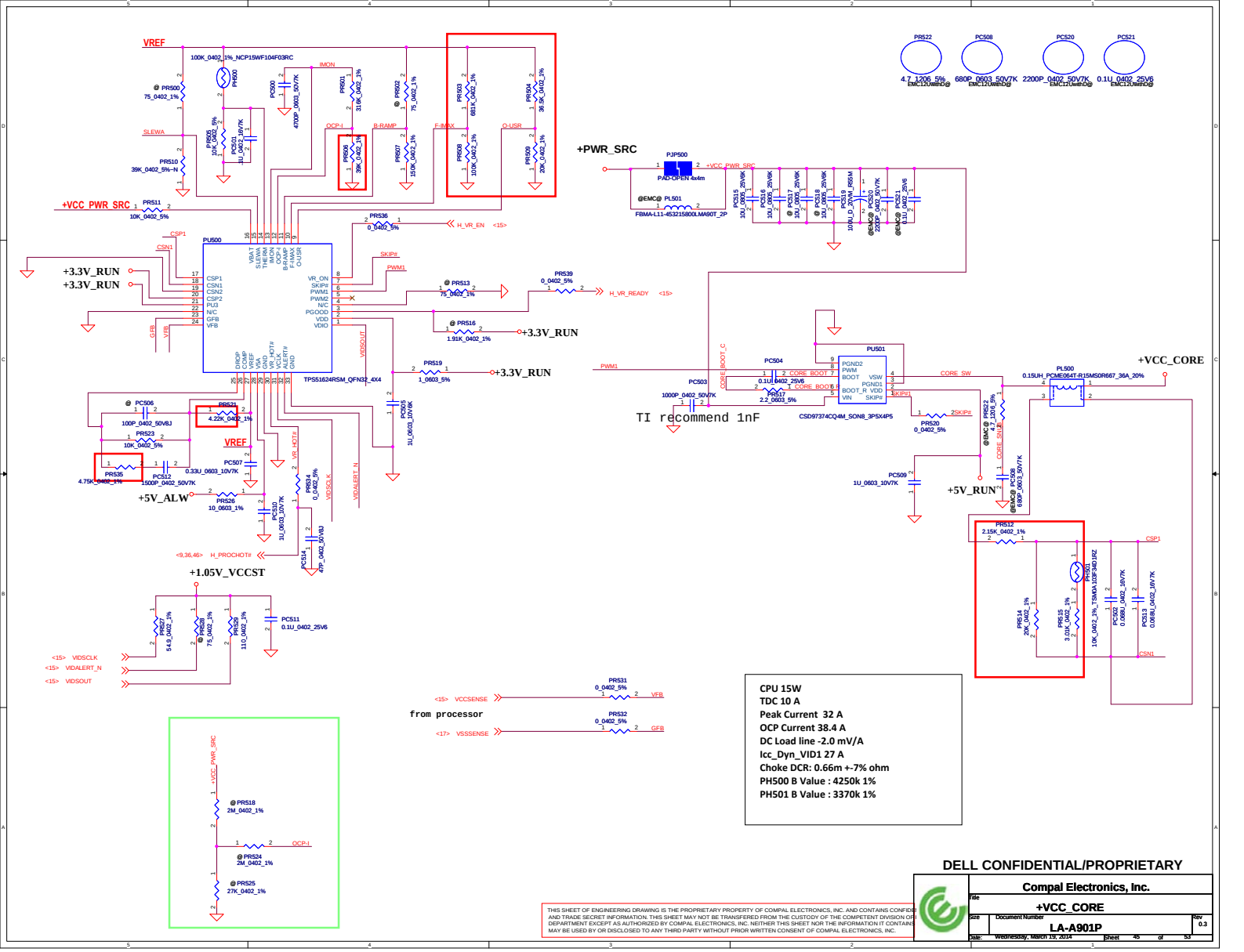
Compal Electronics, Inc.		
Title: +1.5V_RUN		
Size	Document Number: LA-A901P	Rev: 0.3
Date: Wednesday, March 19, 2014	Sheet 44 of 53	



CPU 15W
TDC 10 A
Peak Current 32 A
OCP Current 38.4 A
DC Load line -2.0 mV/A
Icc_Dyn_VID1 27 A
Choke DCR: 0.66m +-7% ohm
PH500 B Value : 4250k 1%
PH501 B Value : 3370k 1%

TI recommend 1nF

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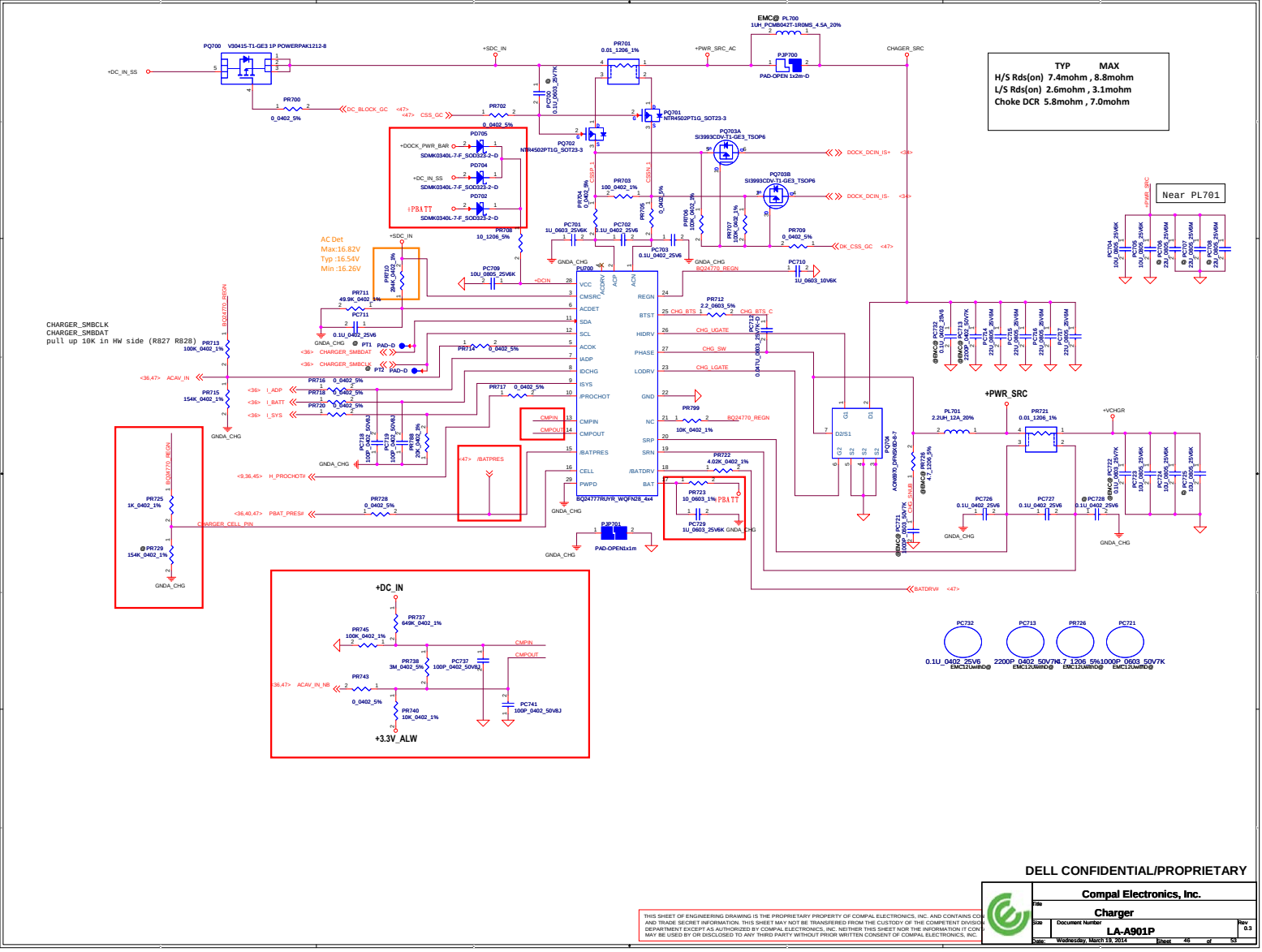
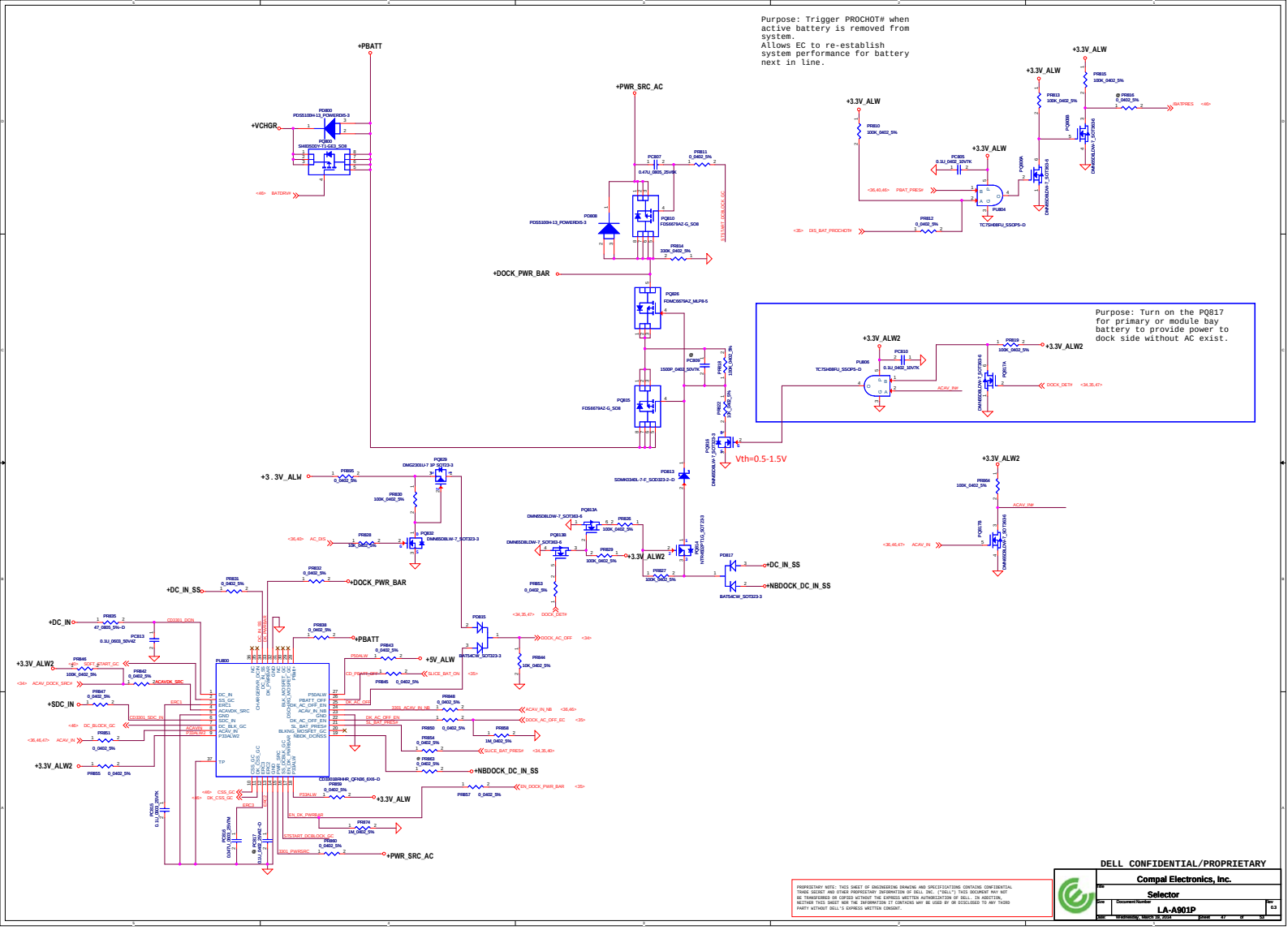
Compal Electronics, Inc.		
Title: +VCC_CORE		
Size	Document Number: LA-A901P	Rev: 0.3
Date: Wednesday, March 19, 2014	Sheet 45 of 53	



DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.			
Title: Charger			
Size	Document Number: LA-A901P		Rev: 0.3
Date: Wednesday, March 19, 2014	Sheet 46 of 53		



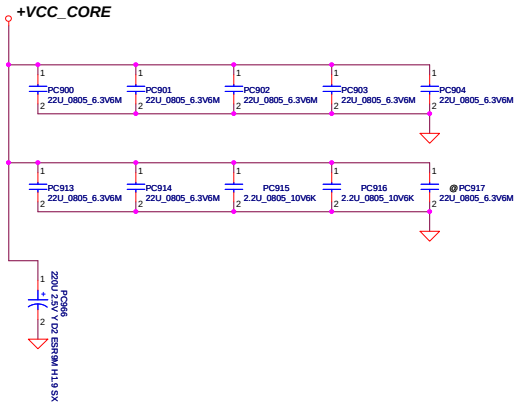
DELL CONFIDENTIAL/PROPRIETARY

Compal Electronics, Inc.

Title: Selector

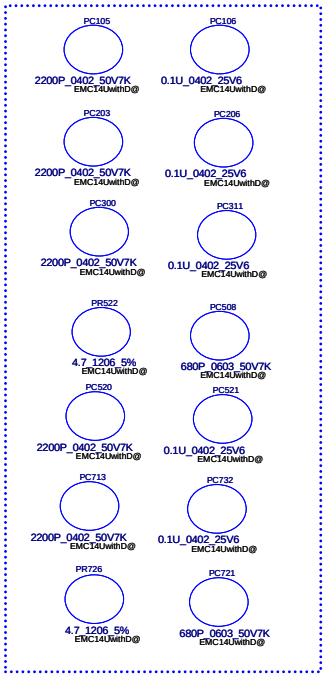
Size: | Document Number: LA-A901P | Rev: 0.3

Date: Wednesday, March 31, 2010 | Sheet 47 of 53



961

Based on _RF Cheng. Hill
鄭智仁(11257) for PT 20131107



Compal Electronics, Inc.		
Title: PROCESSOR DECOUPLING		
Size	Document Number: LA-A901P	Rev: 0.3
Date: Wednesday, March 19, 2014	Sheet 48 of 53	

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	47	Selector	10/8	Compal	Remove slice battery support circuit	Remove PC808, PC811, PC812 , PC814, PD806, PD807, PD811, PD814, PD819, PD821, PQ801, PQ807, PQ809, PQ811, PQ812, PQ818, PQ821, PQ828, PQ830, PQ831, PR802, PR804, PR808, PR813, PR815, PR816, PR817, PR821, PR823, PR825, PR834, PR836, PR837, PR839, PR849, PR852, PR861, PU805, PU807, PU808	X01
2	45	VCC_CORE	10/8	Compal	To prevent acoustic noise issue	Remove PC923, PC924, PC925, PC926, PC927, PC928, PC929, PC930, PC931, PC940, PC941, PC943, PC946, PC947, PC948 Add PC966	X01
3	42	1.35V_MEN	10/8	RICHTEK	To prevent IC damage	Add PR204	X01
4	46	Charger	10/8	Compal	Fine tune divider voltage	Change PR713, PR725 to 100k Change PR715, PR729 to 154k	X01
5	41,43,44	+1.05V_M +1.5V_RUN +3V/+5V	10/22	Compal	To improve the ability of anti-noise	Change PR307 to 7.5k Change PR310, PR102, PR104, PR403 to 10k Change PR100 to 6.49k Change PR101 to 15k Change PR402 to 8.66k	X01
6	46	Charger	10/25	Compal	Change /BATPRES pin control net from /BATPRES to PBAT_PRES#	Pop PR728 Depop PR816	X01
7	45	VCC_CORE	10/31	Compal	Fine tune IMON	Add PR518, PR524, PR525	X01
8	ALL	ALL	10/31	Compal	RF request	Add PC521, PC206, PC106, PC311, PC732 (0.1uF)	X01
9	ALL	ALL	10/31	Compal	RF request	Pop PR111,PC111,PR112,PC114,PR203,PC208,PR305,PC301,PR522,PC508, (4.7ohm, 680pF)	X01
10	46	Charger	10/31	Compal	To prevent VCP trigger PROCHOT#	PR703 change to 100ohm	X01

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	6	HW	2013/10/8	COMPAL	Follow intel reference circuit.	Add CC100, RC300 on CPU pin AC4, net name is PM_TEST_RST	0.2(X01)
2	27	HW	2013/10/8	COMPAL	Dell drop POA function.	Change JUSH1 from 26 pin to 20 pin, pin define follow E5	0.2(X01)
3	36	HW	2013/10/8	COMPAL	Dell drop POA function.	remove POA_WAKE# off page symbol remove POA_ON/OFF#,make UE2.B62 to be NC pin	0.2(X01)
4	22	HW	2013/10/9	COMPAL	IC version changed.	VMM2320 circuit change: 1. UV8 from VMM2320 change to VMM 2330 (SA00007G800) 2. UV8 pin J3, E5 to +1.05V_RUN 3. VMM_SPI_WP# reserved RV517, 2.2K resistor PU to +3.3V_RUN_VMM 4. VMM_GPIO4,reserved RV518, 2.2K resistor PU to +3.3V_RUN_VMM 5. VMM_GPIO5 reserved RV519, 2.2K resistor PU to +3.3V_RUN_VMM 6. UV8 pin B5, B6 change to +3.3V_RUN_VMM 7. LP_CTL reserved RV516, 2.2K resistor PU to +3.3V_RUN_VMM 8. Depop RV73	0.2(X01)
5	24	HW	2013/10/9	COMPAL	correct HDMI schematic error.	swap HDMI LANE0 & LANE2 BUS	0.2(X01)
6	23	HW	2013/10/9	COMPAL	Follow EMC suggestion	Change LI1,LI2,LI3,LI4,LI5,LI6,LI7,LI8,LI9,LV3,LV6,LV10,LV12,LV27 From SM070003K00 (S COM FI_ CHILISIN CMMI21T-900Y-N) To SM070003Y00 (S COM FI_ MURATA DLW21HN900HQ2L)	0.2(X01)
7	9	HW	2013/10/9	COMPAL	reserved for S3 within 2s , system shutdown issue debug.	add RC26, reserved RC27.	0.2(X01)
8	36	HW	2013/10/9	COMPAL	board ID change.	RE79 change to 130K	0.2(X01)
9	24	HW	2013/10/9	COMPAL	SATA ciruit issue	Swap mSATA P & N	0.2(X01)
10	36	HW	2013/10/14	COMPAL	follow intel latest design guide.	pop RE56 and change from 8.2K to 10K , it's RESET_OUT# pull down resistor	0.2(X01)
11	7	HW	2013/10/16	COMPAL	RF requirement.	add CC14, CC15 and move CC12, CC13 to behind the resistor (RC72)	0.2(X01)
12	20,23,31,32	HW	2013/10/17	COMPAL	follow ESD recommend list.	change all ESD diode CPN change DI2, DI3, DI5, DV4 from SCA00001100(S ZEN ROW PJDLC05C 3P C/A SOT23) to SC600001600(S DIO ROW AZC199-02S.R7G C/C SOT23 ESD) change DI1,DI6,DI4 from SC300002800(S DIO(BR) TVWDF1004AD0 DFN ESD) to SC300002C00(S DIO(BR) L05ESDL5V0NA-4 SLP2510P8 ESD) change DA1,DA2,DA3,DA6,DA7 from SCA00001L00(S ZEN ROW L30ESDL5V0C3-2 C/A SOT23 ESD) to SCA00002900(S ZEN ROW L03ESDL5V0CC3-2 C/A SOT-23 ESD)	0.2(X01)
13	38	HW	2013/10/17	COMPAL	power doesn't split VPRO & NPRO BOM.	add RZ41, RZ42, reserve it for VPRO & NVPRO option.	0.2(X01)
14	39	HW	2013/10/17	COMPAL	SSI design will cause LED behavior error.	QL1 Pin2,5 & QL2 Pin2 change from MASK_BASE_LEDS# to SYS_LED_MASK#	0.2(X01)

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15	20	HW	2013/10/17	COMPAL	To solve Line-on HDD dirty shut down issue.	UZ8 Pin2 change from +3.3V_ALW to 3.3V_RUN	0.2(X01)
16	28, 36, 38	HW	2013/10/17	COMPAL	follow Dell requirement.	Add back SUS_ON, change control pin from SUS_ON to SIO_SLP_S4# 1. UZ8.3 from SIO_SLP_S4# to SUS_ON 2. UE2.B23 → SUS_ON_EC , RPE10.2 → SUS_ON 3. add RE282, RE281, RE280, RE279 4. UE2.B9 → RUN_ON_EC	0.2(X01)
17	12	HW	2013/10/24	COMPAL	add GPIO pin for DIMM quantity detection.	add DIMM_DET on UC1.U4? to replace PCH_GPIO48 ,Reserve RC302 &RC303	0.2(X01)
18	6	HW	2013/10/24	COMPAL	debug usage.	add RC301	0.2(X01)
19	9	HW	2013/10/28	COMPAL	reserve it to prevent PCH_PLTRST# floating when power on	add RC304, 100K pull down, on PCH_PLTRST#_EC	0.2(X01)
20	6, 7, 22, 28	HW	2013/10/23	COMPAL	follow xtal vender suggest	1 CC1 &CC2 change from 18PF to 3PF 2 CC8 & CC11 change from 18PF to 15PF 3 CL13 & CL14 change from 33PF to 27PF 4 RV81 change from 0 ohm to 2.2K & CV113 change to 18PF	0.2(X01)
21	23	HW	2013/10/29	COMPAL	it's designed for E5 Goliad, E6 GMLK doesn't need.	remove RZ1	0.2(X01)
22	30	HW	2013/10/29	COMPAL	To solve WWAN can not detec issue.	Add RZ50, 100k pull up for WWAN_PWR_EN	0.2(X01)
23	12	HW	2013/10/29	COMPAL	To solve backdrive issue.	Change TPM_PIRQ# pull up (RC247) to +3.3V_RUN from +3.3V_ALW_PCH	0.2(X01)
24	30	HW	2013/10/30	COMPAL	Dell doesn't support MODPHY.	add PJP36, depop QZ6, QZ10, RZ16, RZ5, CZ25, CZ38	0.2(X01)
25	7	HW	2013/11/2	COMPAL	SMBUS Pull High	Add RN3&RN4 pull high to +3.3V_RUN for DDR_XDP_WAN_SMBDAT/SMBCLK	0.2(X01)
26	21	HW	2013/11/2	COMPAL	EMC request.	Add RA42, RA43.	0.2(X01)
27	21	HW	2013/11/05	COMPAL	follow vender suggestion. It's for 15KV ESD fail issue.	add CA12, CA13 change DA1, DA2, DA3, DA4 from GNDA to GND	0.2(X01)
28	12	HW	2013/11/05	COMPAL	GPIO 14 is sus power well, it has risk to cause back drive.	move TPM_PIRQ# from PCH_GPIO14 to PCH_GPIO17, add T21 on PCH_GPIO14	0.2(X01)
39	21	HW	2013/12/17	COMPAL	follow vender suggest to solve "Bo" noise	1.UA1 pin22 add RA45 0 ohm PU to +3.3V_RUN_AUDIO 2.UA1 pin21 add RA44 100k ohm to GND	0.3(X01)
40	22	HW	2013/12/17	COMPAL	follow vender suggest	1.RPC8 change from 2.2k to 10k 2.UC1.F2 &RPC8.3 change name from I2C0_SDA to PCH_GPIO4 3.UC1.F3 &RPC8.4 change name from I2C0_SCL to PCH_GPIO5 4.UC1.G4 &RPC8.1 change name from I2C1_SDA_VMM to PCH_GPIO6 5.UC1.F1 &RPC8.2 change name from I2C1_SCL_VMM to PCH_GPIO7 6.RPV2.1 connect to I2C1_SDA_VMM 8.RPV2.2 connect to I2C1_SCL_VMM 9.Depop RV516, CV116, CV117	0.3(X01)

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29	22	HW	2013/12/17	COMPAL	To solve CRT display jitter issue	1.LV23,LV25 change from BLM15AX102SN1D to BLM15PX181SN1D 2.CV90,CV101 change from 1uF to 10uF	0.3(X01)
30	22	HW	2013/12/17	COMPAL	Base on Pre-PT RSMRST EA result	1.POP RE88,UZ6,RE51 2. remove QZ12,RZ48,RZ49,RZ50	0.3(X01)
31	22	HW	2013/12/17	COMPAL	follow vender suggestion	1. change LV22 , LV24 From SM01000N400 S SUPPRE_ MURATA BLM15AX102SN1D 0402 To SM01000NO00 S SUPPRE_ MURATA BLM15PX181SN1D 0402 2. change CV82, CV94 from 1uF to 10uF 3. UV8 pin D3 from +1.05V_VMM_VDDTX to +1.05V_VMM_VDD. 4. UV8 Pin H3, E10, H11 change to NC 5. Change UV8 pin B5, B6 from +3.3V_RUN_VMM to +3.3V_RUN_VDDIO"	0.3(X01)
32	7	HW	2013/12/26	COMPAL	RF recommend	Change CC12, CC13, CC14, CC15 from 16pF to 33pF	0.3(X01)
33	7	HW	2013/12/27	COMPAL	Intel recommend	Change RC33, RC34 from 1k to 499 ohm	0.3(X01)