

## ZAS BLOCK DIAGRAM

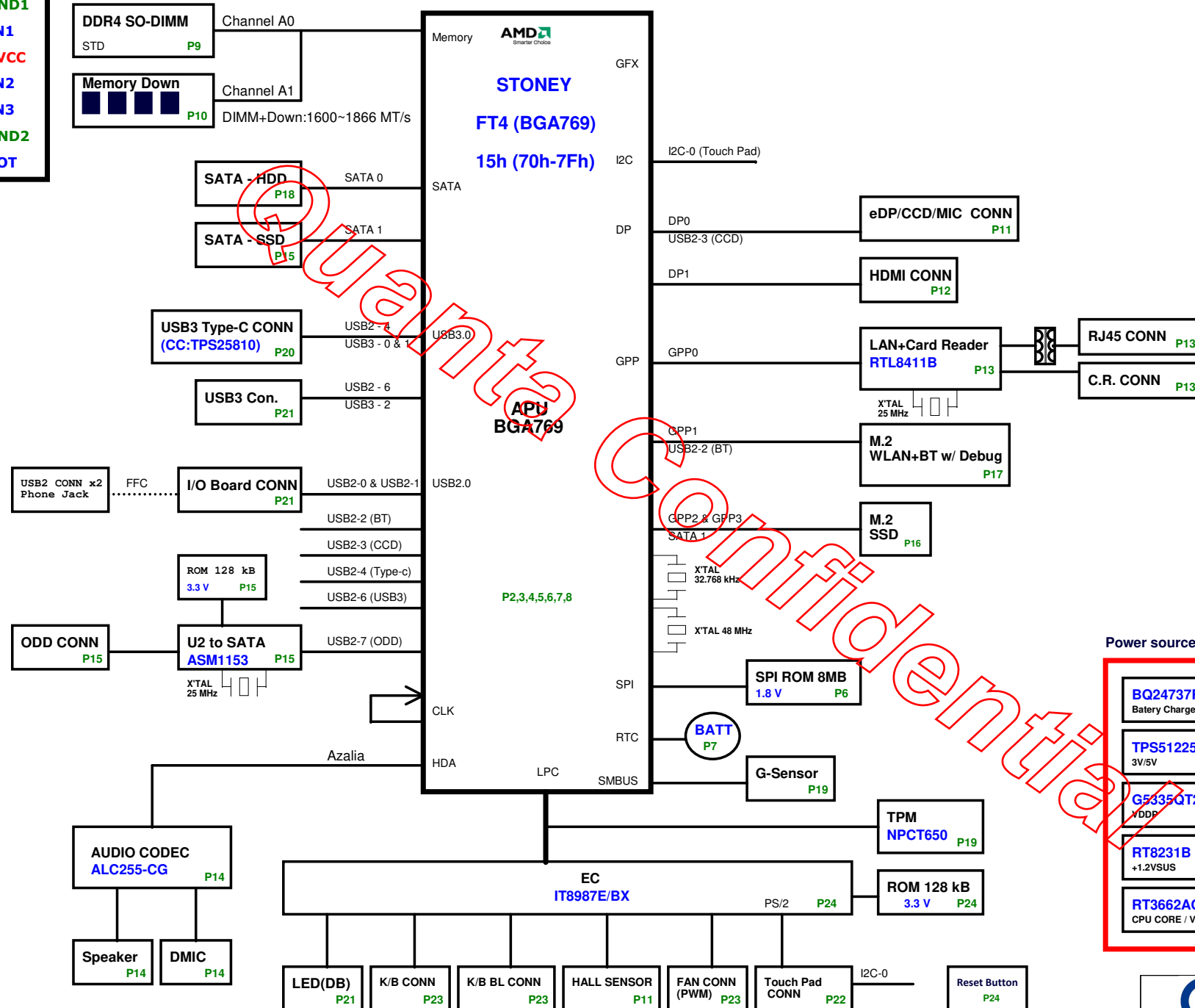
Vinafix

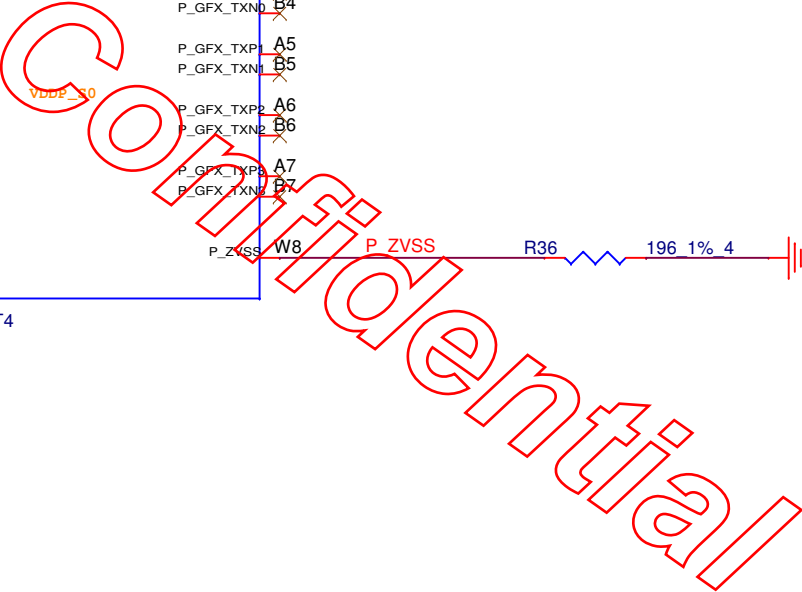
## Power source

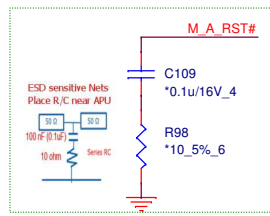
<b>BQ24737RGRR</b> Battery Charger P25	<b>M5671RE1U</b> 1.8V P31
<b>TPS51225R</b> 3V/5V P26	<b>G9336ADJTP1U</b> 0.775V P31
<b>G5335QT2U</b> VDDP P27	<b>G5719CTB1U</b> 1.5V P31
<b>RT8231B</b> +1.2VSUS P28	<b>TPS61087DRCR</b> 12V(PANEL) P33
<b>RT3662AC</b> CPU CORE / VDDNB P29, P30	

## PCB STACK UP

- LAYER 1 : TOP**  
**LAYER 2 : GND1**  
**LAYER 3 : IN1**  
**LAYER 4 : SVCC**  
**LAYER 5 : IN2**  
**LAYER 6 : IN3**  
**LAYER 7 : GND2**  
**LAYER 8 : BOT**







A0-DIMM

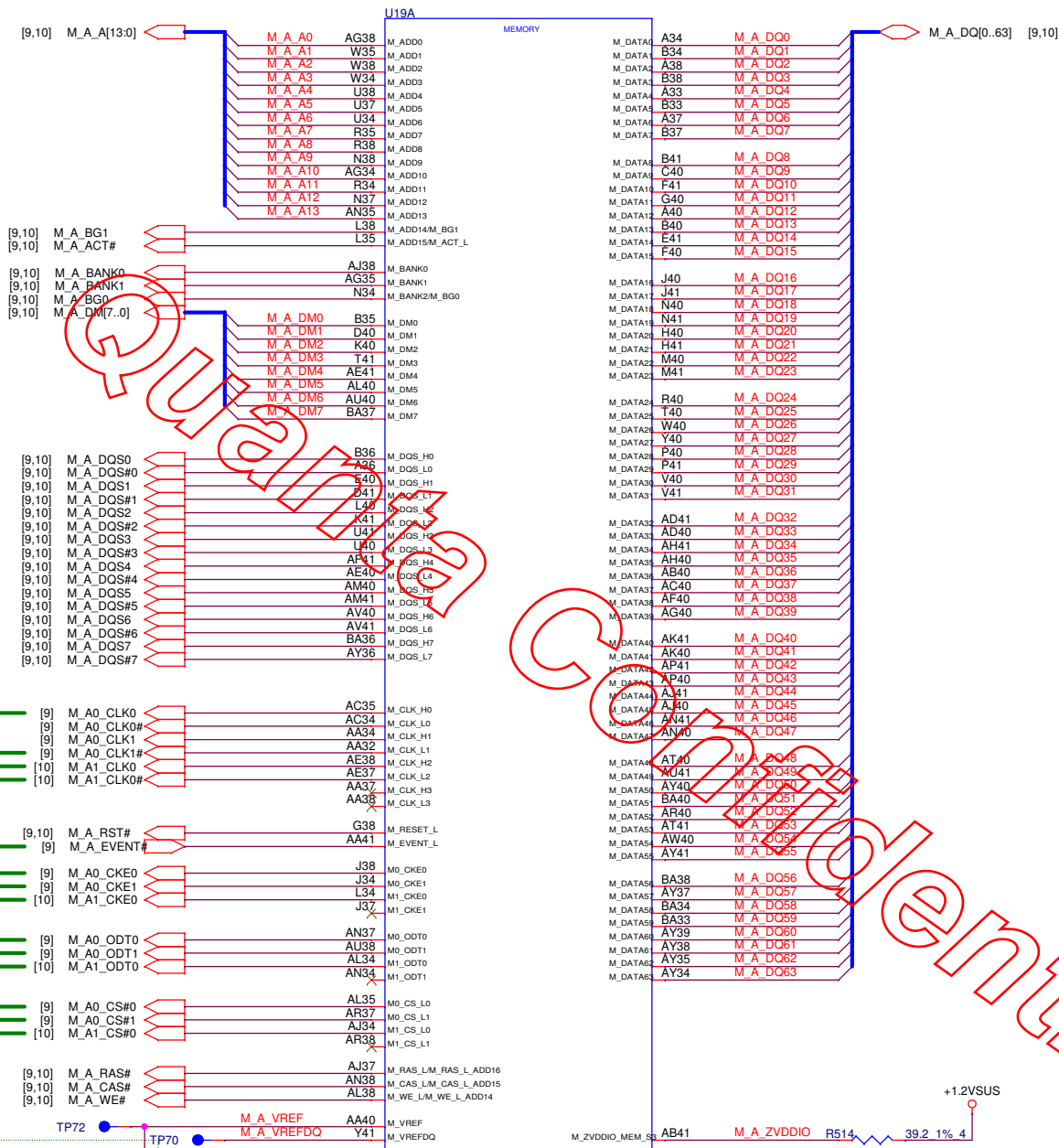
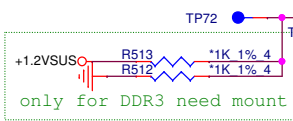
A1-ON BOARD

A0-DIMM

A0-DIMM  
A1-ON BOARD

A0-DIMM  
A1-ON BOARD

A0-DIMM  
A1-ON BOARD



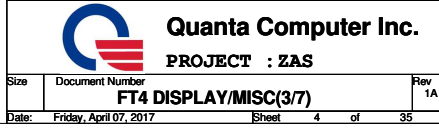
Quanta Computer Inc.  
PROJECT : ZAS

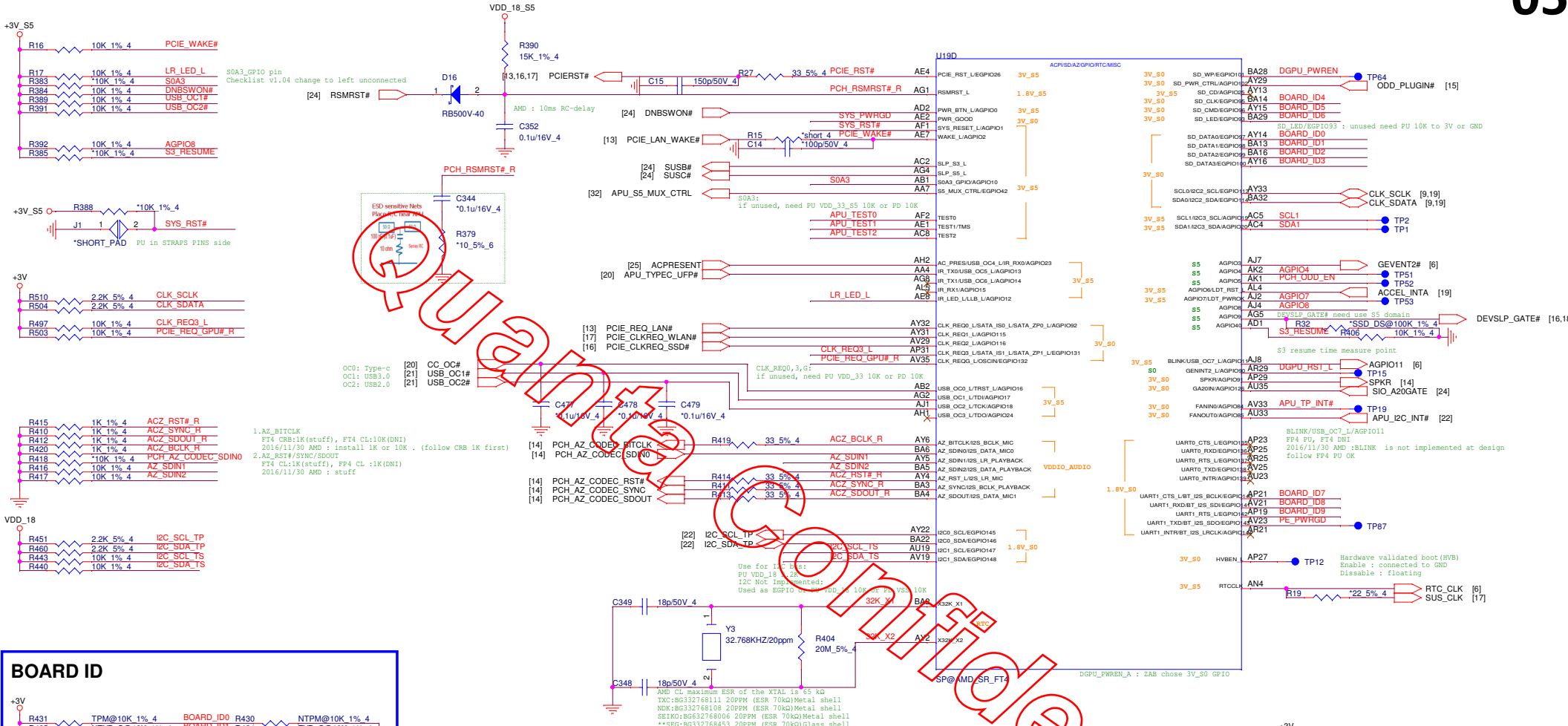
Size	Document Number	Rev
	FT4 DDR4 I/F(2/7)	1A
Date:	Friday, April 07, 2017	Sheet 3 of 35

## Serial VID

### SMBUS (Internal Thermal sensor)

## HDT(Hardware Debug Tool ) Connector





### BOARD ID

+3V

R431 TPM@10K 1% 4 BOARD ID0 R430 NTPM@10K 1% 4

R425 NTP C@10K 1% 4 BOARD ID1 TYP C@10K 1% 4

R429 NCS@10K 1% 4 BOARD ID2 GS@10K 1% 4

R427 EV@10K 1% 4 BOARD ID3 UMA@10K 1% 4

R437 SP@10K 1% 4 BOARD ID4 SP@10K 1% 4

R426 SP@10K 1% 4 BOARD ID5 SP@10K 1% 4

R4501 SP@10K 1% 4 BOARD ID6 SP@10K 1% 4

VDD\_18

R635 SSDS@10K 1% 4 BOARD ID7 R637 SSDP@10K 1% 4

R636 SP@10K 1% 4 BOARD ID8 R638 SP@10K 1% 4

R639 SP@10K 1% 4 BOARD ID9 R640 SP@10K 1% 4

GPIO	High	Low
BOARD_ID0	dTPM	iTPM
BOARD_ID1	non-Type C	Type C
BOARD_ID2	non-G sensor	G sensor
BOARD_ID3	GPU	UMA
BOARD_ID4	Memory ID	Memory ID
BOARD_ID5	Memory ID	Memory ID
BOARD_ID6	Memory ID	Memory ID
BOARD_ID7	SATA SSD	PCIe SSD
BOARD_ID8	Reserve	Reserve
BOARD_ID9	Reserve	Reserve

Reserve:Default PD

### Test mode setting (Follow AMD's suggestion)

+3V\_S5

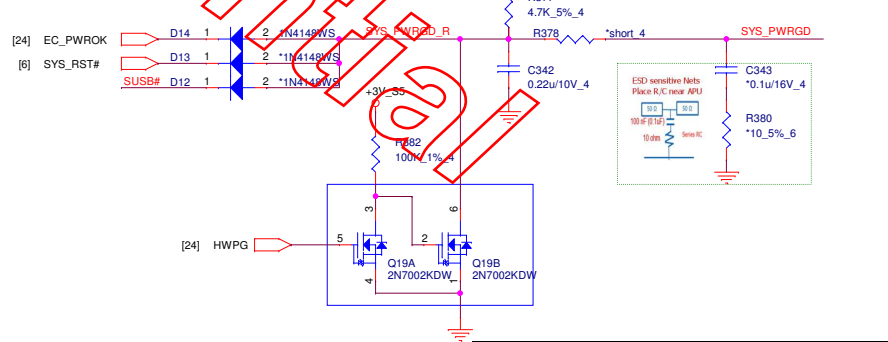
NC, no install by default

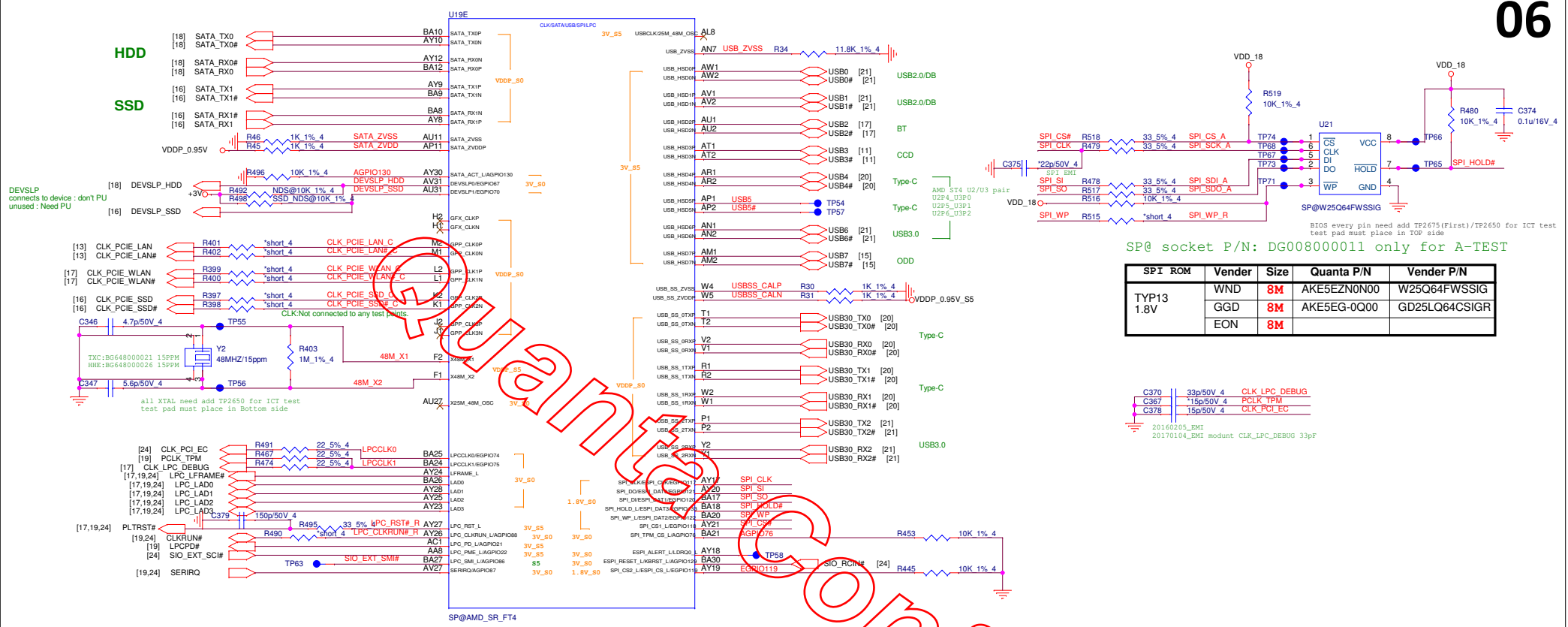
R387 APU\_TEST0 R408 15K 1% 4

R386 APU\_TEST1 R407 15K 1% 4

R25 APU\_TEST2 R29 15K 1% 4

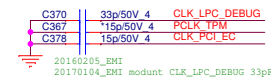
TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



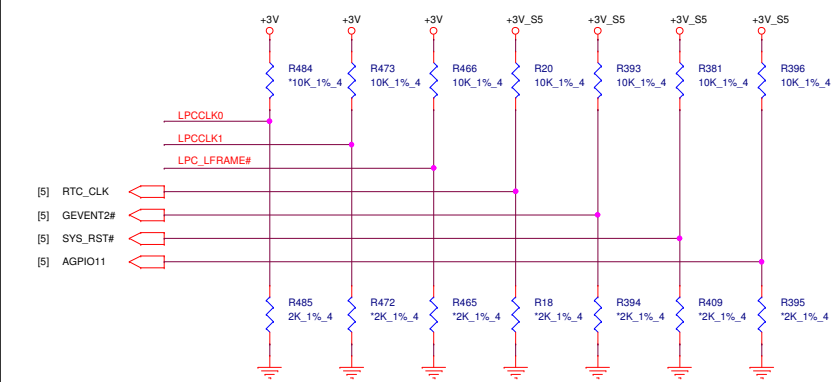


SP@ socket P/N: DG008000011 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
TYP13 1.8V	WND	8M	AKE5EZNN000	W25Q64FWSSIG
	GGD	8M	AKE5EG-0Q00	GD25LQ64CSIGR
	EON	8M		

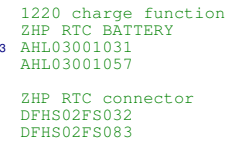
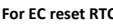
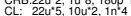
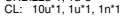
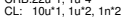


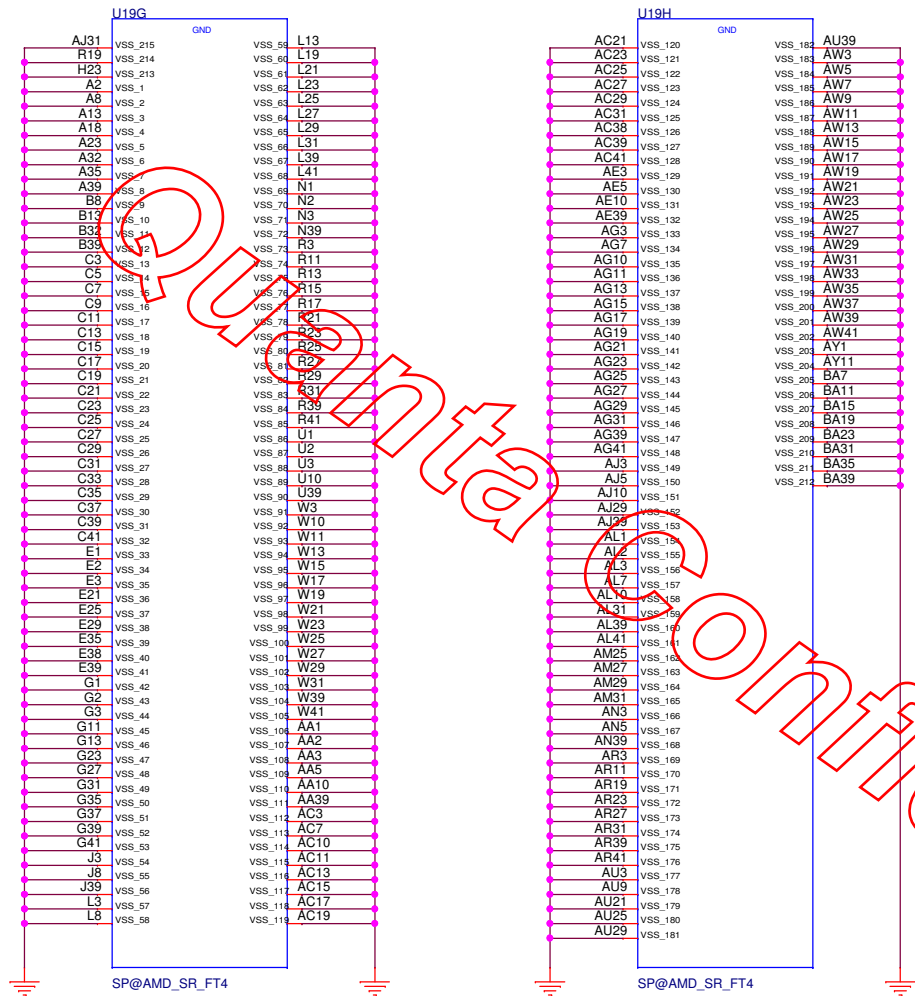
## STRAPS PINS



	LPC_CLK0	LPC_CLK1	LFRAME#	RTC_CLK	GEVENT2# (AGPIO3)	SYS_RST#	AGPIO11(BLINK)
PU	BOOT Fail Timer ENABLE	Use 48MHz crystal clock and generate both internal and external clocks	SPI ROM	Coin battery is on board.	1.8V SPI ROM	Enhanced Reset logic (for quicker S5 resume)	normal reset mode
PD	BOOT Fail Timer DISABLE	Use 100MHz PCIe clock as reference clock and generate internal clocks only	LPC ROM	Coin battery isn't on board.	3.3V SPI ROM	Default to traditional reset logic	short reset mode



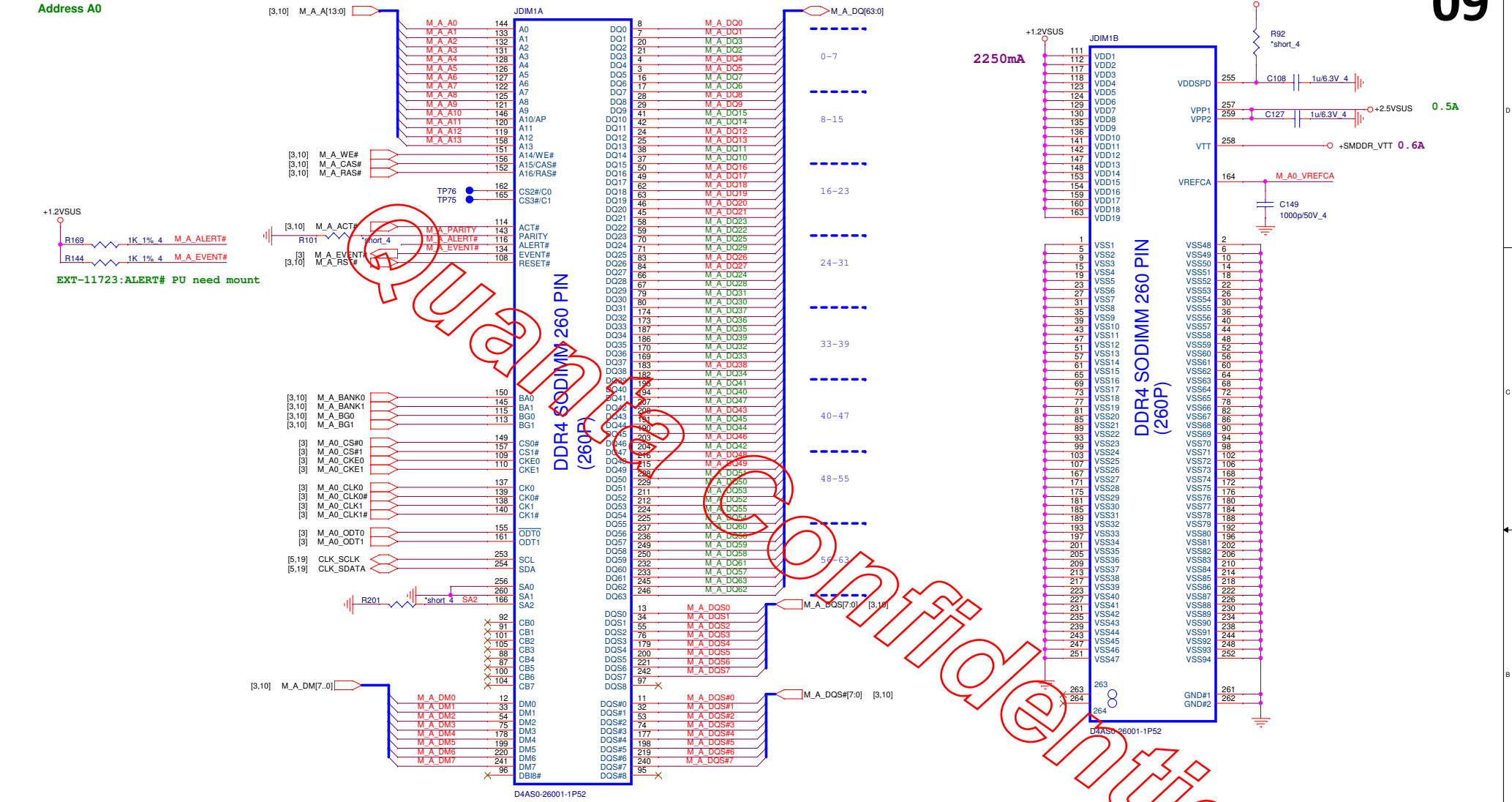




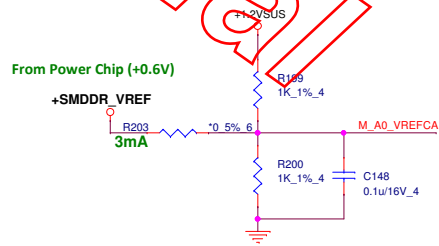
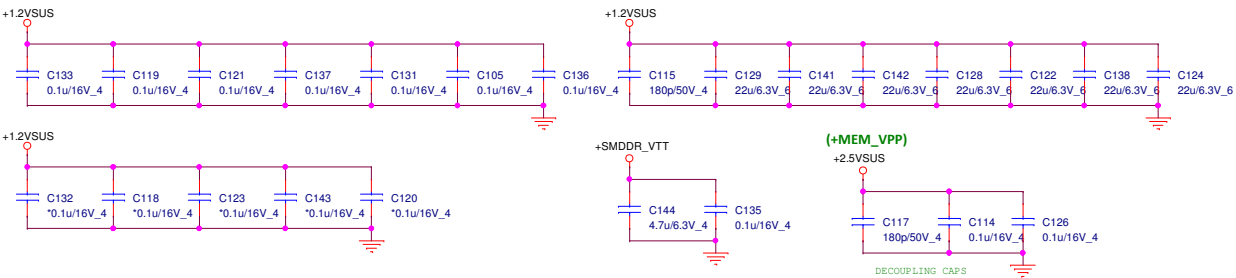



SODIMM (SDM)

Address A0



Place these Caps near So-Dimm A





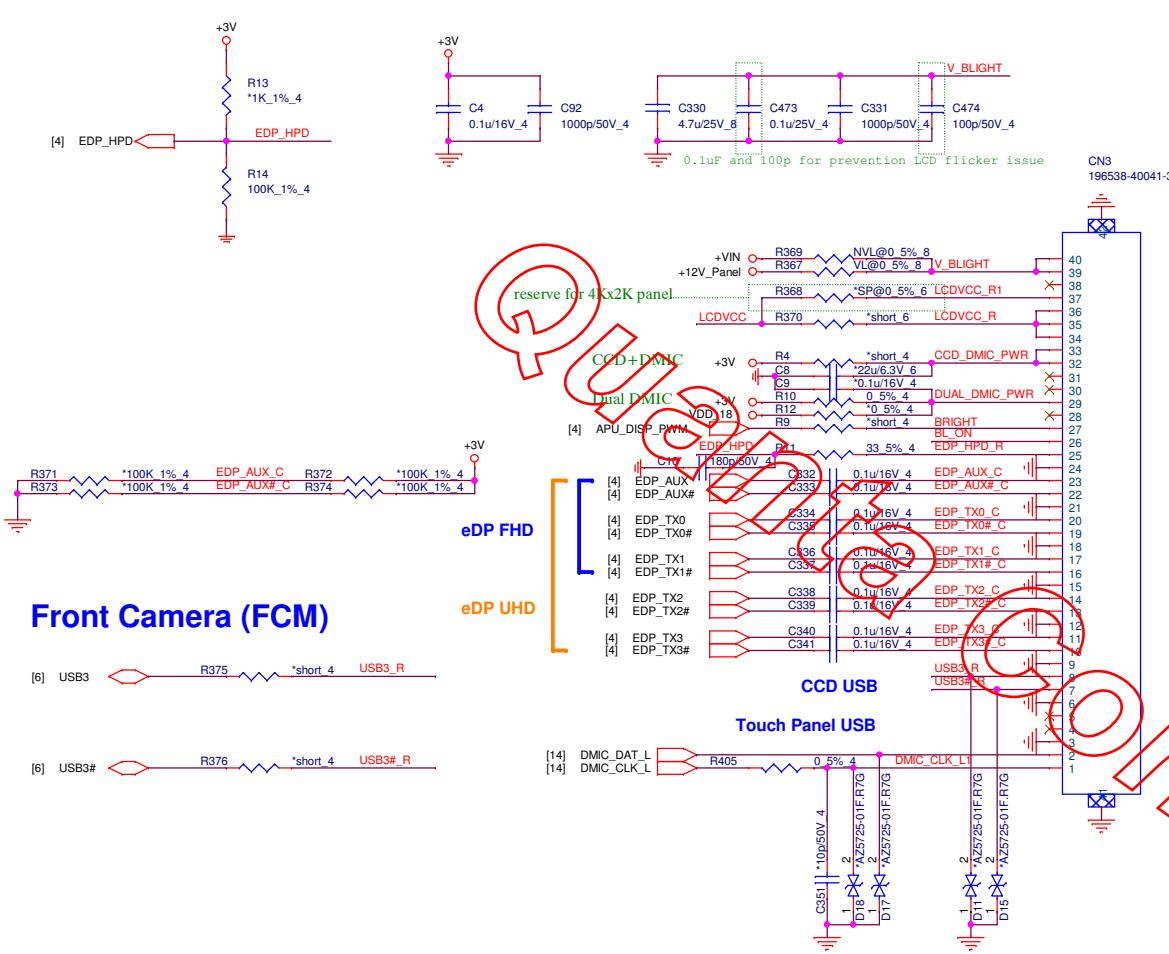
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**PROJECT : ZAS**

**DDR4 DIMM CHA0 (STD)**

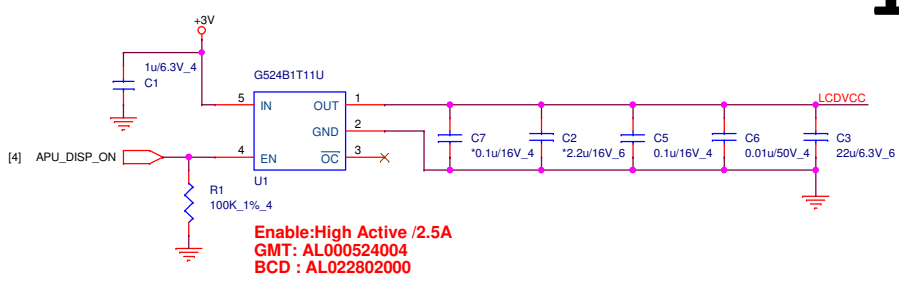
Size	Document Number	Rev
		1A
Date:	Friday, April 07, 2017	Sheet 9 of 35



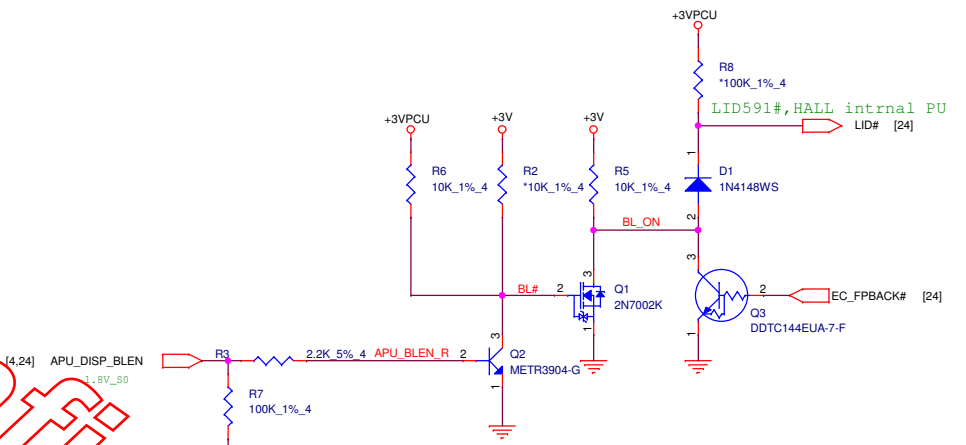


PIN30,31 TP power  
PIN28 TP Enable  
PIN4,5 TP USB

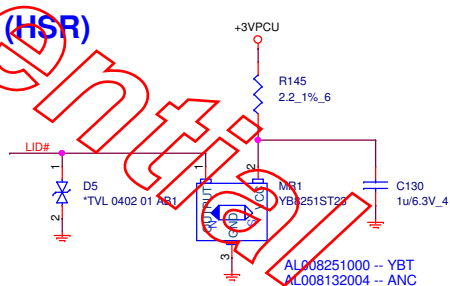
## LCD Power (LDS)



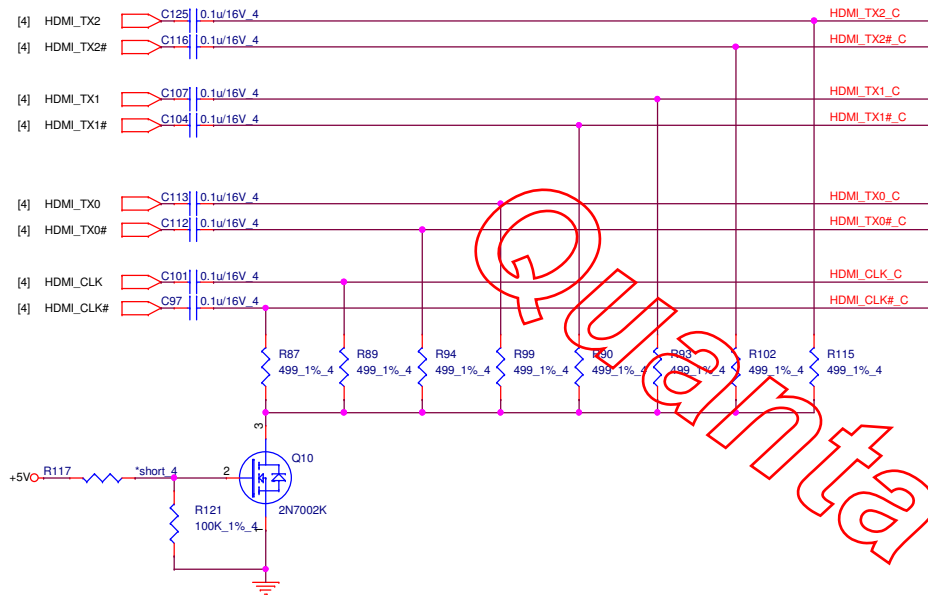
## Backlight Control (LDS)



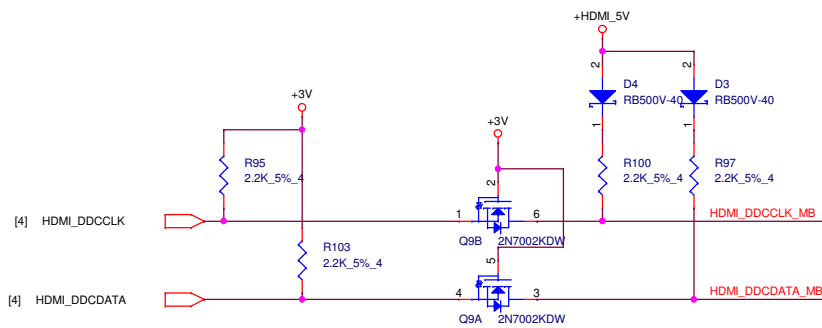
**Lid Switch (HSR)**



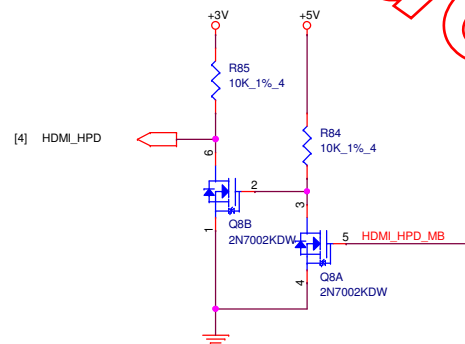
## HDMI(HDM)



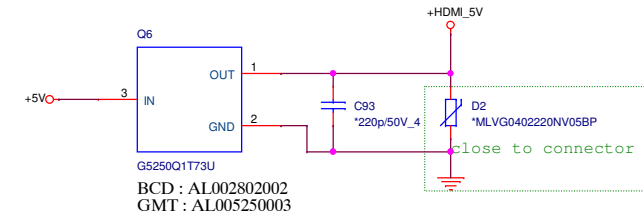
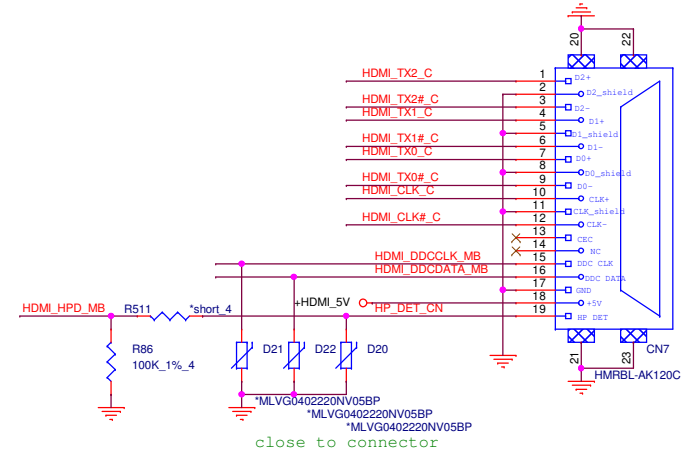
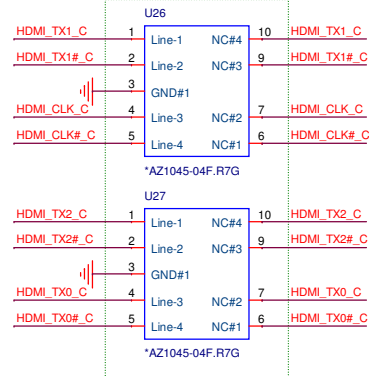
## HDMI DDC (HDM)



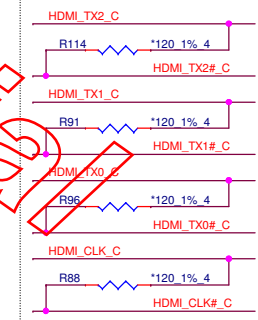
## HDMI-detect (HDM)



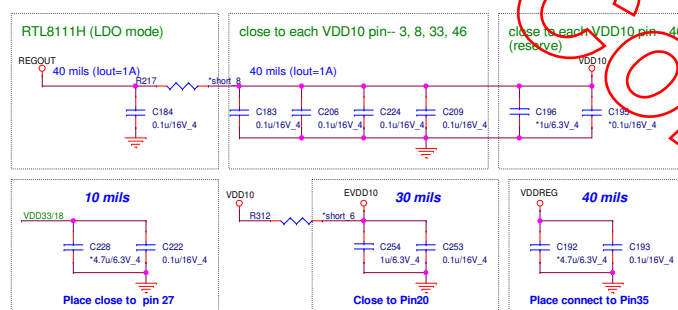
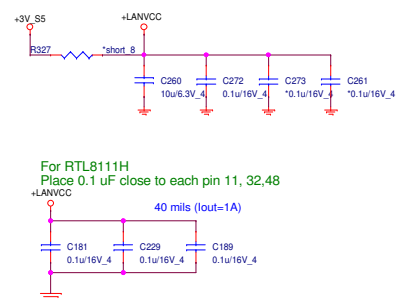
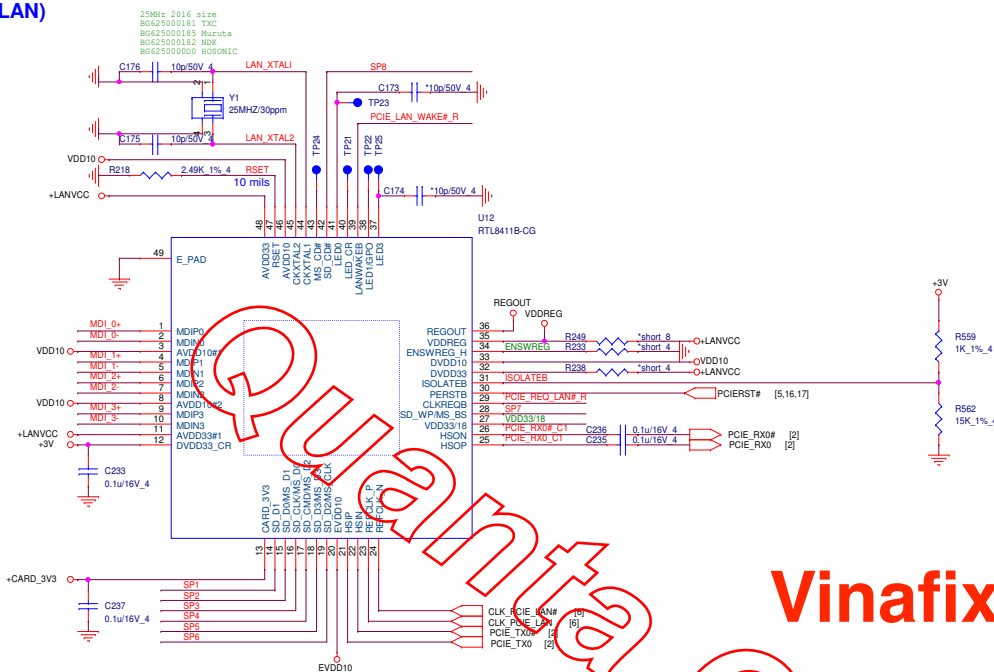
close to connector



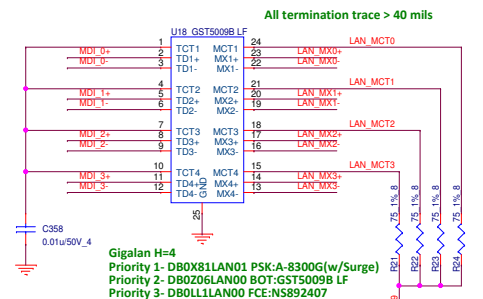
## EMI



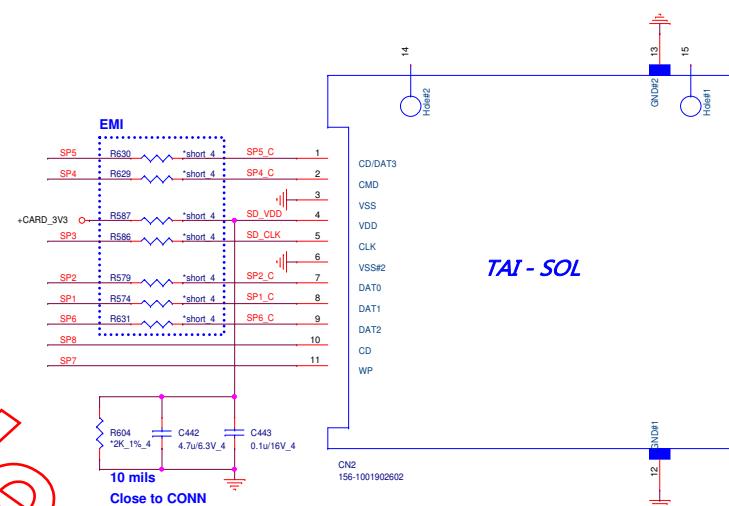
### LAN & Card reader Combo (LAN)



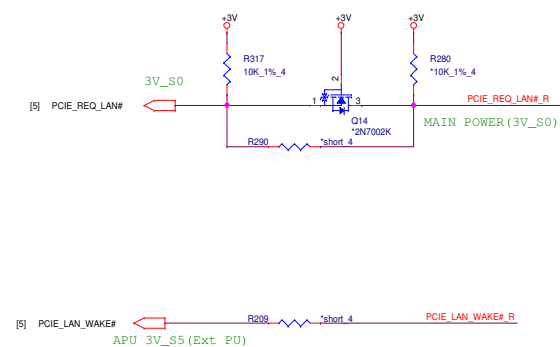
## Transformer



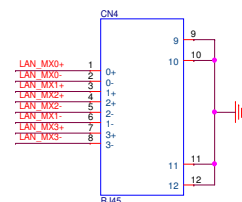
## Crad Reader Connector



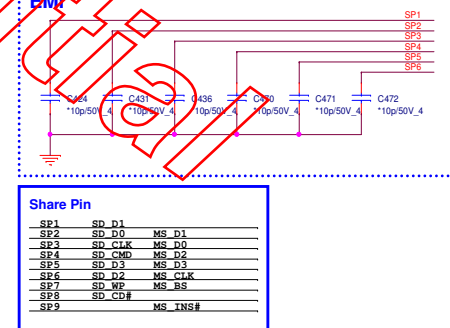
## Leakage circuit



## RJ45 Connector



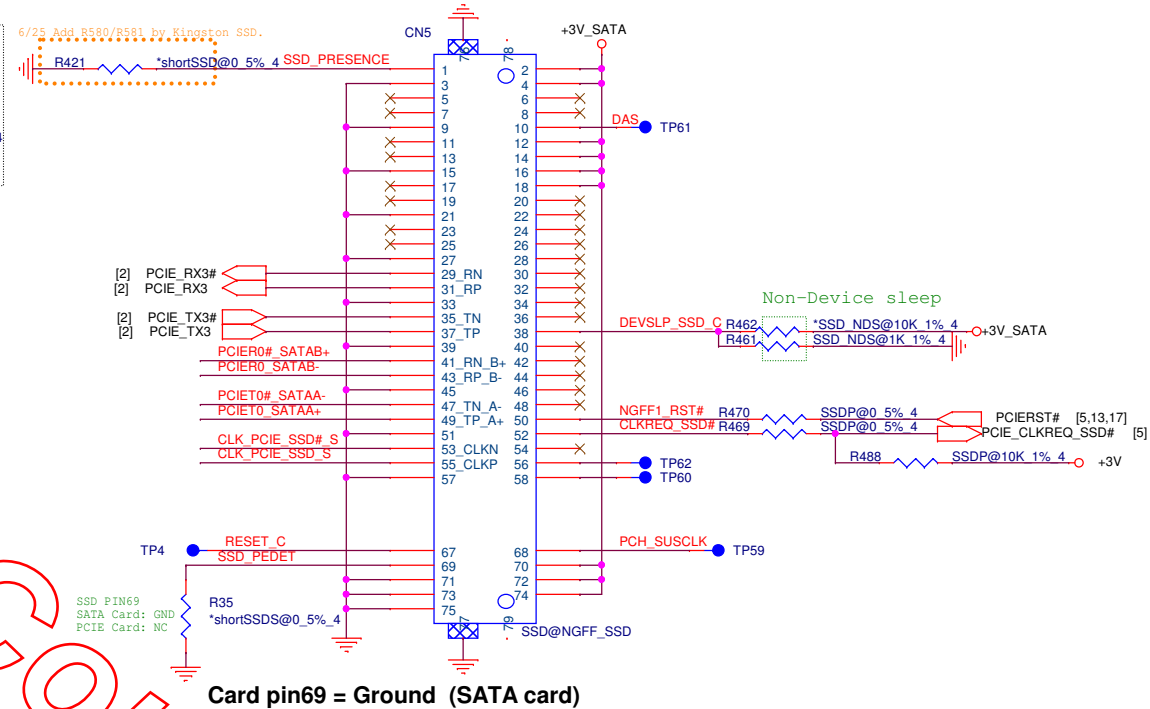
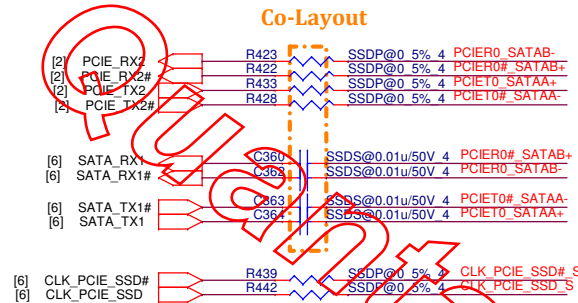
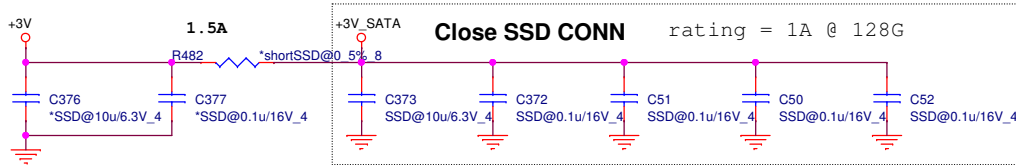
EM





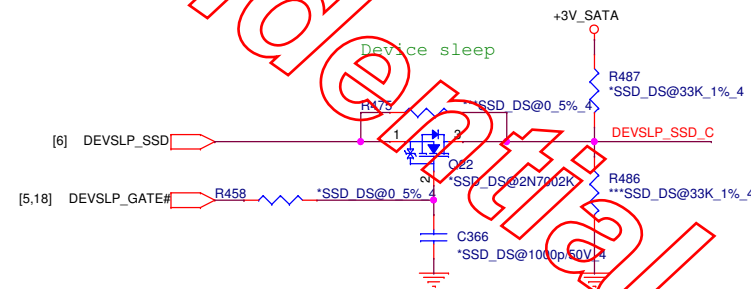






Card pin69 = Ground (SATA card)

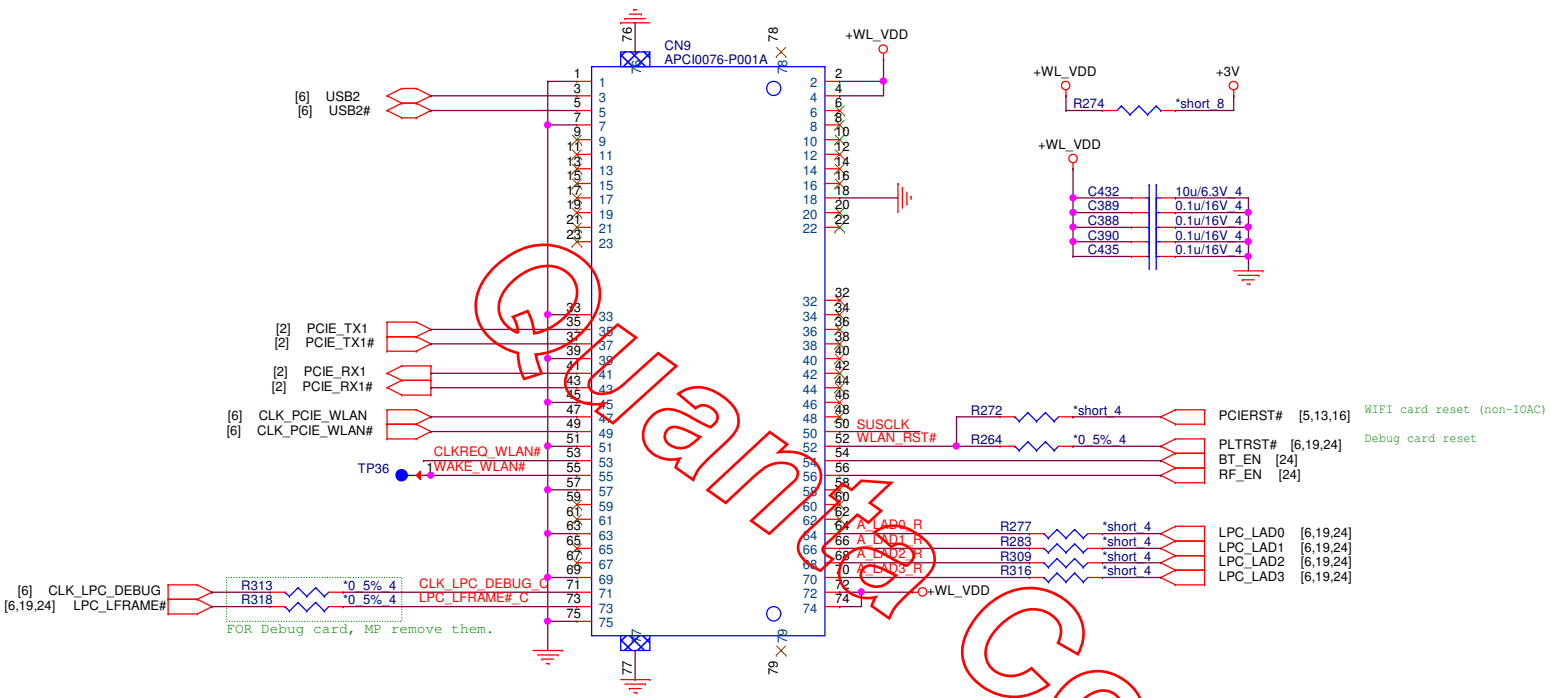
pin	Type	Description
1	PRESENCE	This pin is grounded on the SSD. May be used by host to determine if slot is empty or populated
10	DAS#	Device Activity Signal
21	WWAN/SSDIND_N	This pin connect to Ground
38	Device Sleep Signal	If system didn't support DEVSLP, set DEVSLP Sleep Signal pin power high and keep (from power on), device will ignore. If system support DEVSLP, set DEVSLP Sleep Signal pin power low (from power on) device, device will support DEVSLP function. Device Sleep Signal H: SSD enter sleep model. Device Sleep Signal L: SSD exit sleep model.
53	REFCLKN	no connect on SSD
55	REFCLKP	no connect on SSD
56	MFG1	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
58	MFG2	Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board
68	SUSCLK	no connect on SSD
69	IFDET	This pin connect to Ground



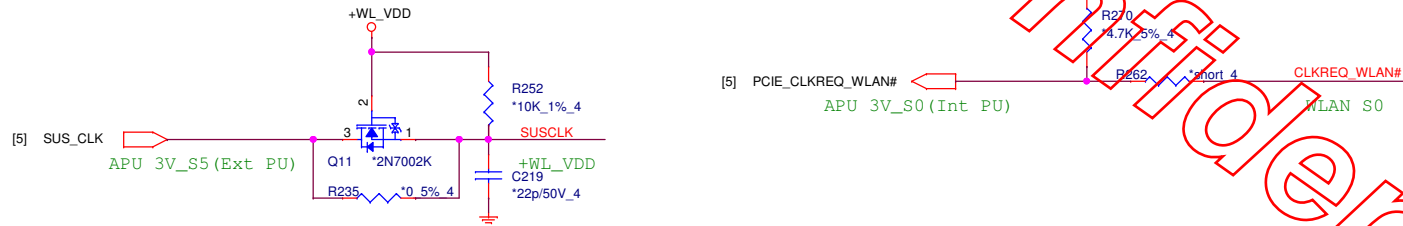
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Size	Document Number	Rev
	M.2 SSD	1A

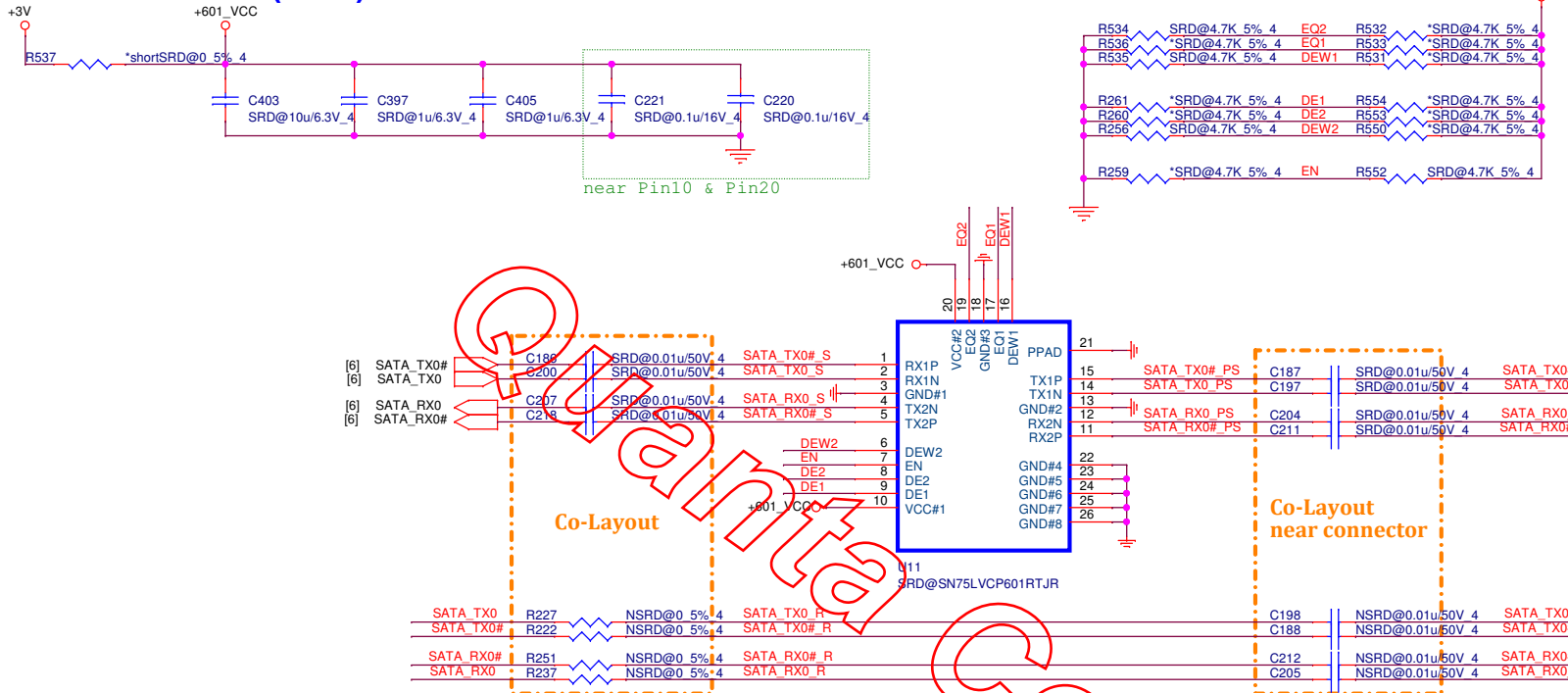
Date: Friday, April 07, 2017 Sheet 16 of 35



### Leakage circuit



## SATA Re-driver (HDD)

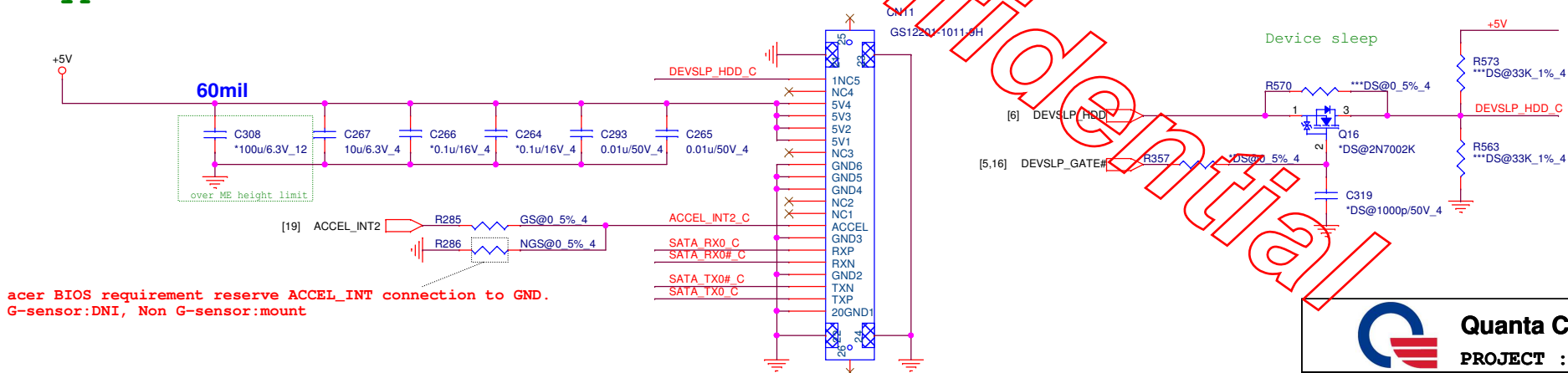


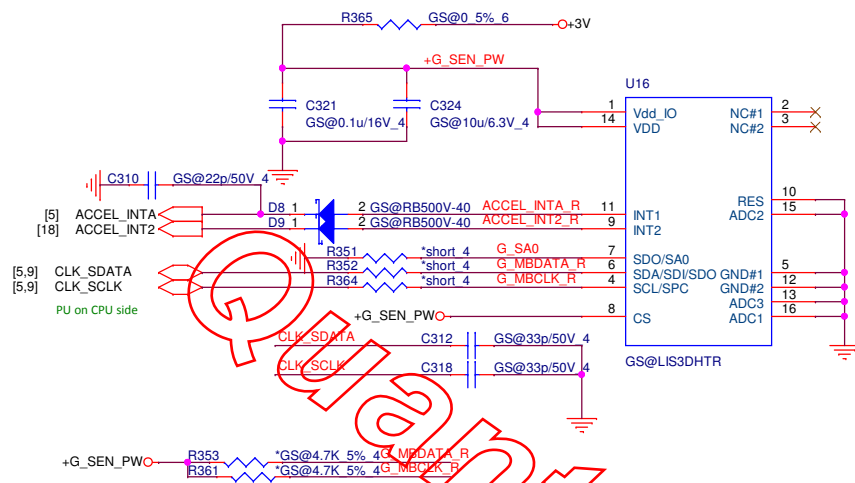
EQ2 H - 14dB X - 0dB L - 7dB	DE1 H - -2dB X - -4dB L - 0dB
EQ1 H - 14dB X - 0dB L - 7dB	DE2 H - -2dB X - -4dB L - 0dB
DEW1 H - Long Duration X - NC (Long) L - Short Duration	DEW2 H - Long Duration X - NC (Long) L - Short Duration
SW7 - EN H - Enabled L - Standby Mode	

18

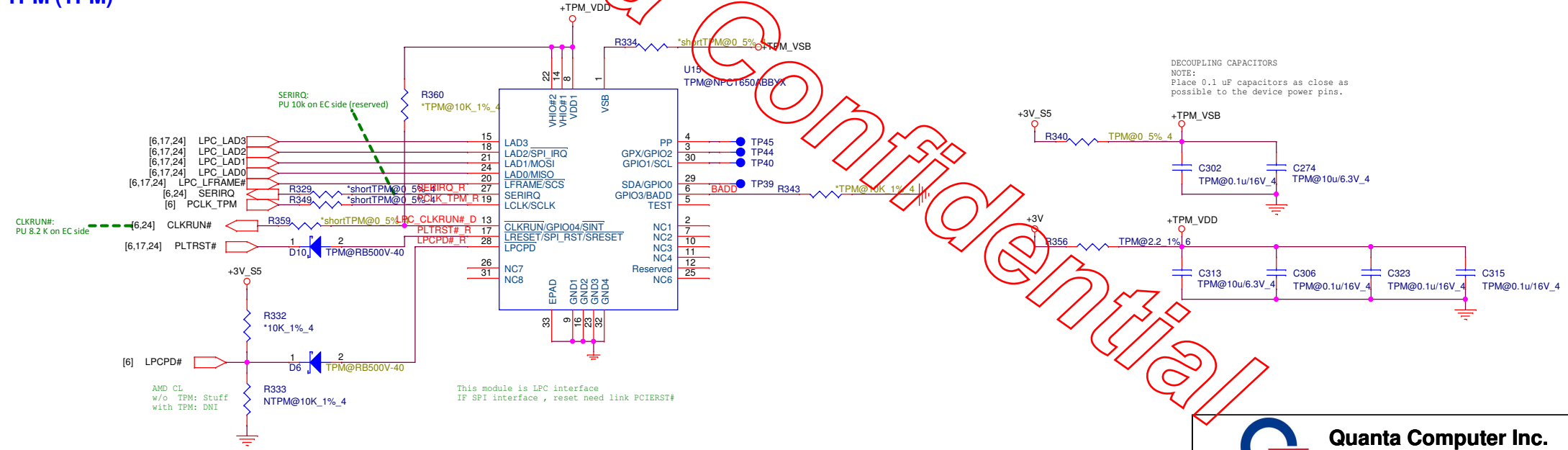
## 2.5" SATA HDD (HDD)

### Cable type connector






TPM (TPM)



DECOUPLING CAPACITORS  
NOTE:  
Place 0.1 uF capacitors as close as possible to the device power pins.

This module is LPC interface  
If SPI interface, reset need link PCIERST#

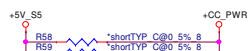


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**PROJECT : ZAS**

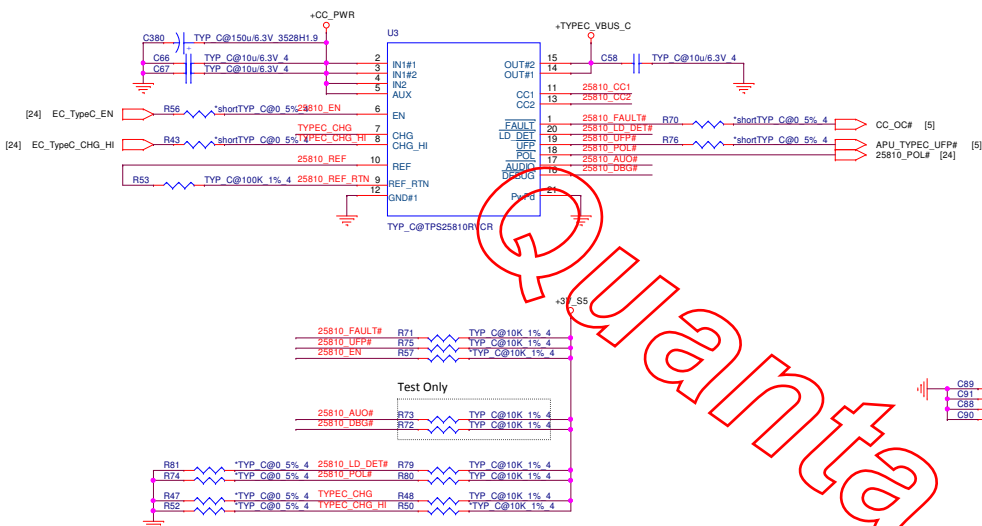
Size	Document Number	Rev
	<b>TPM (NPCT650)/G-sensor</b>	1A
Date:	Friday, April 07, 2017	Sheet 19 of 35

## USB Type C (UTC)



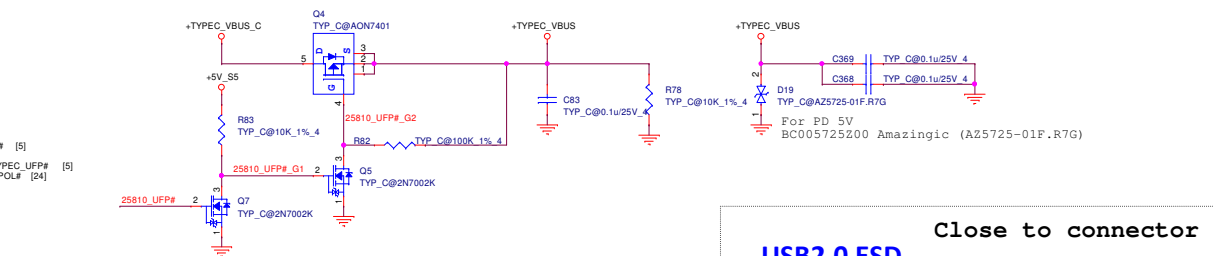
## Type-C CC

Vendor suggest input cap 120u



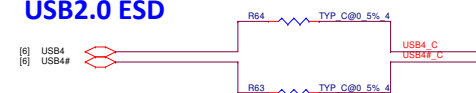
CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

TPS25810 Port	TPS25810 Response							
	CC1	CC2	OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

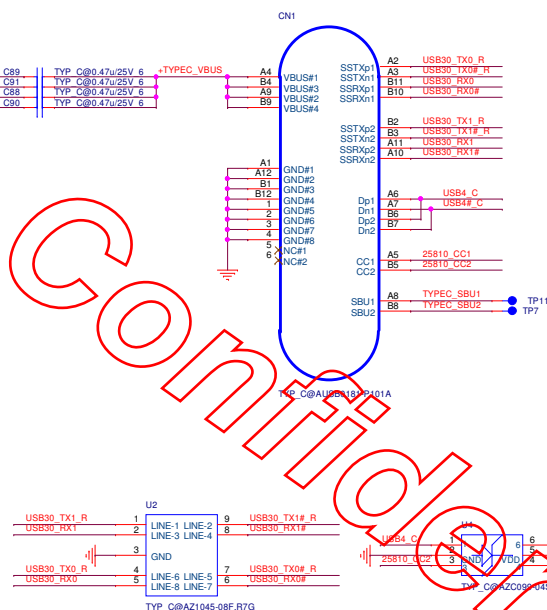
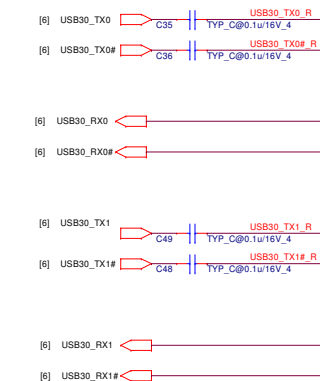


## USB2.0 ESD

Close to connector



## Type C1\_HSIO\_ESD



USE 5V TVS for U3  
 BC104508Z00 Amazingic  
 BC605S8QZ00 PANJIT  
 BC38109LZ00 INPAQ

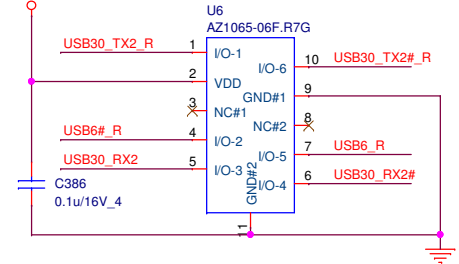
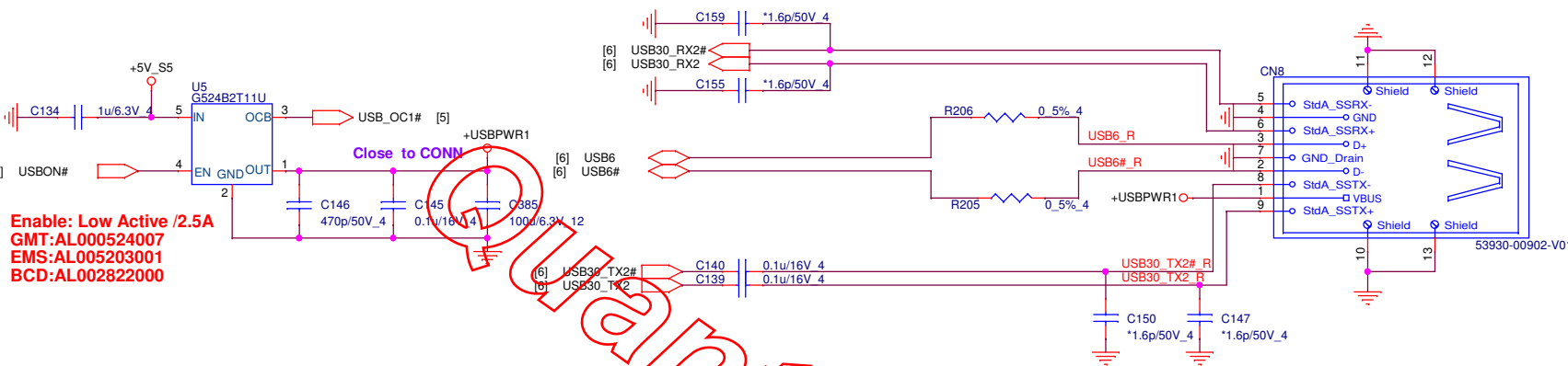
USE 4CH TVS for U2 CC  
 BC09904S200 Amazingic  
 BCSR05W201 PANJIT  
 BCST2304Z00 INPAQ



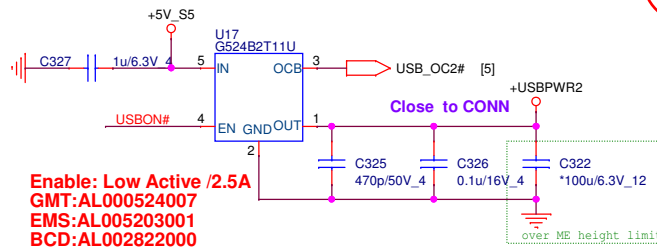
## USB 3.0 Connector (UB3)

USB 3.0 (5V) 6CH  
BC106506000 Amazing (10KV)  
BCD5326DZ00 willsemi (10KV)  
BC12010LZ00 INPAQ (8KV\_can't use)  
+USBPWR1

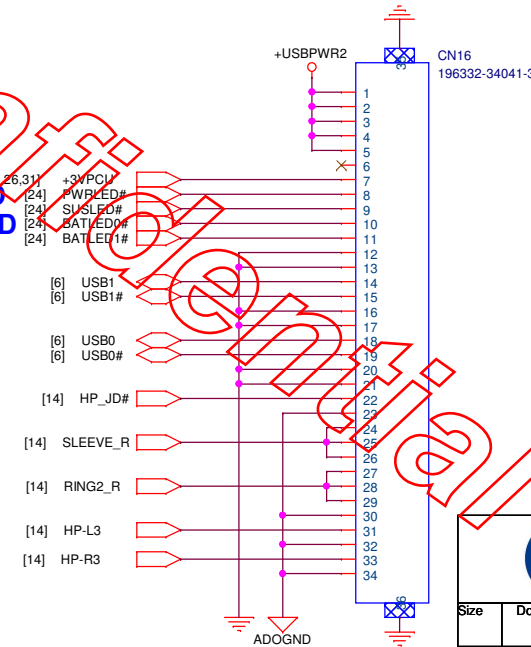
21



## DB USB2.0 (UB2)



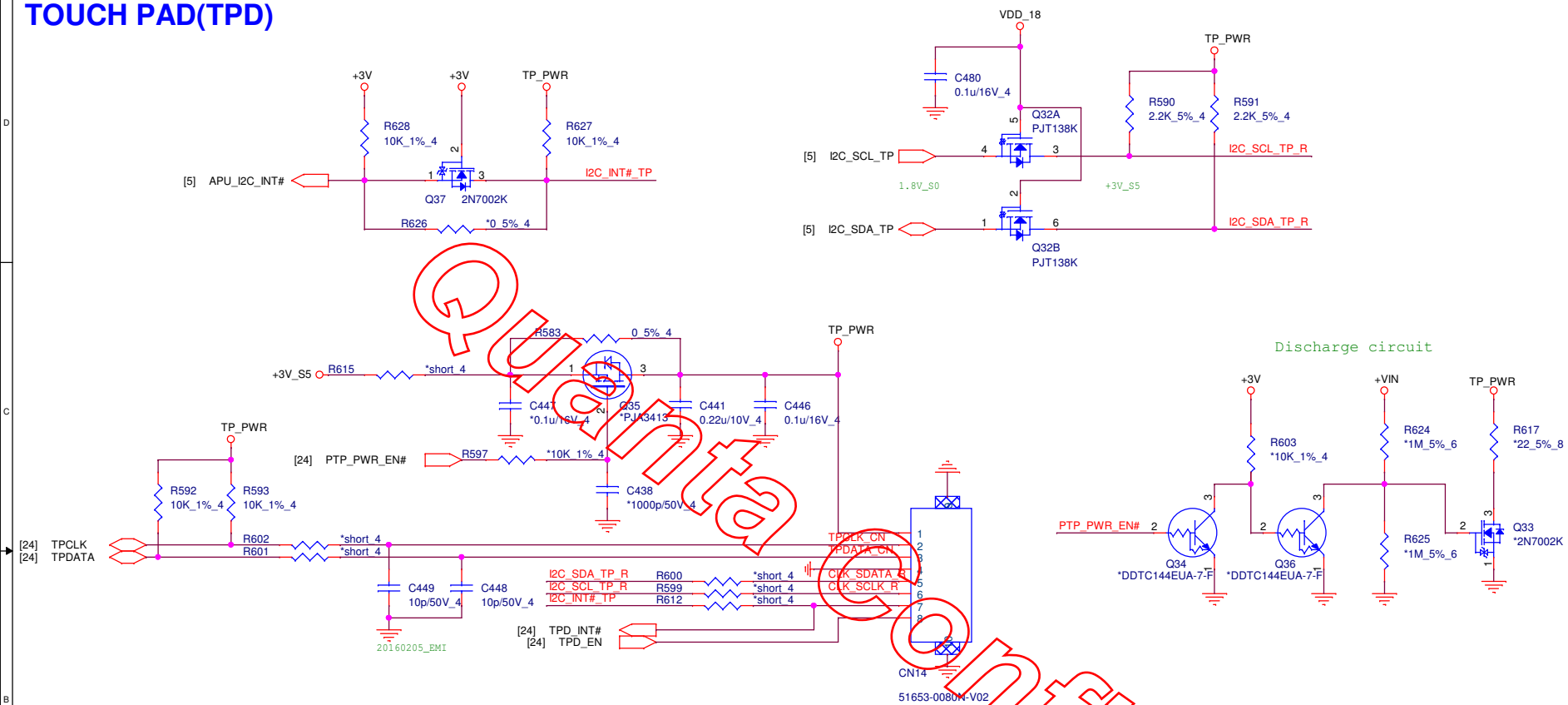
Power LED  
Battery LED



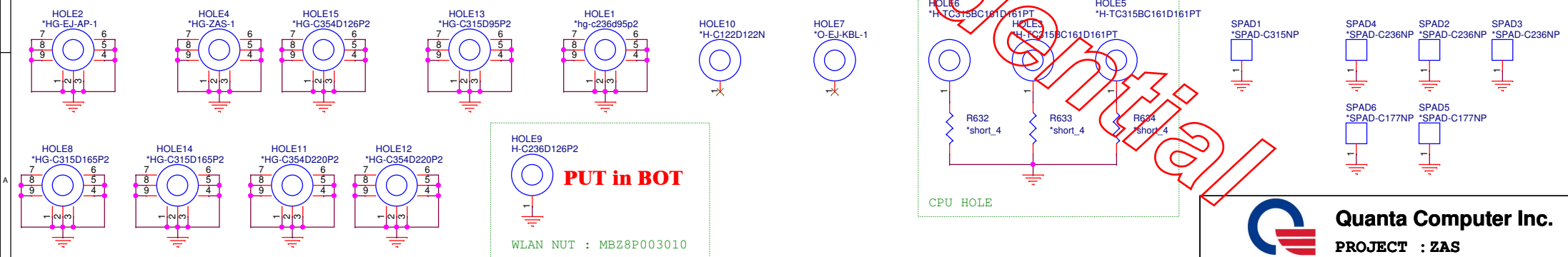
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Size	Document Number	Rev
	USB3/USB2 DB	1A
Date:	Friday, April 07, 2017	Sheet 21 of 35

## TOUCH PAD(TPD)



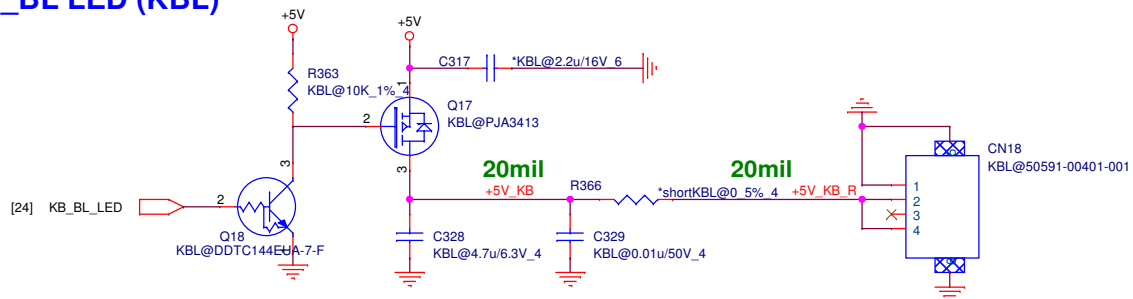
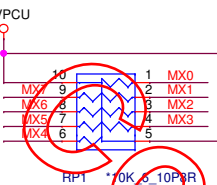
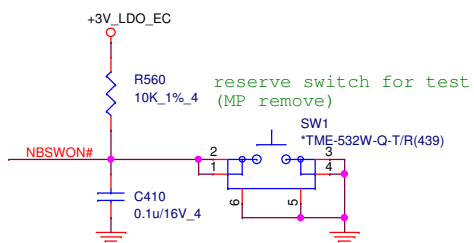
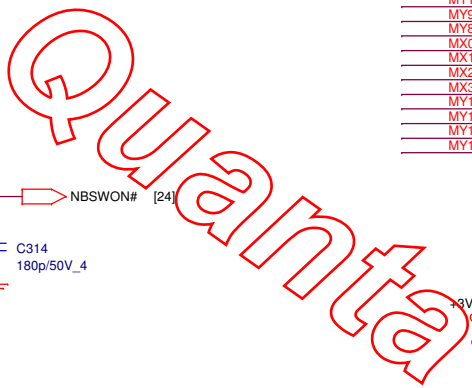
## HOLE(OTH)



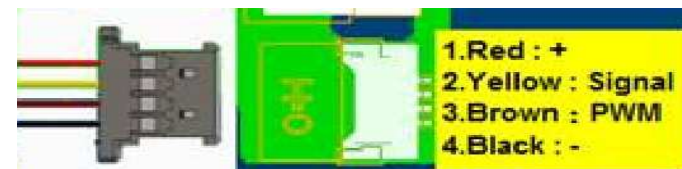
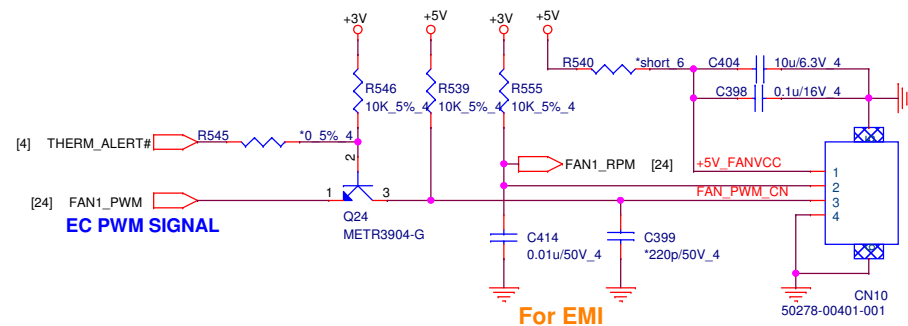
**Quanta Computer Inc.**  
PROJECT : ZAS

Size	Document Number	Rev
	Touch Pad/HOLE	1A
Date: Friday, April 07, 2017	Sheet 22 of 35	

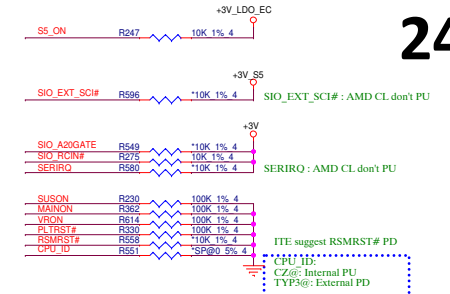
CN13



23



## Stich cap



The diagram shows the EC SMBus PU voltage divider circuit. It includes two voltage dividers: one for +3V\_LDO\_EC and another for +3V\_S5. The +3V\_S5 divider is connected to the CPU temperature sensor (Q28) and the CORE\_PWM\_PROCHOT# pin. The sensor is a 2N7002K MOSFET. The temperature sensor is connected to the CPU temperature sensor (Q28) and the CORE\_PWM\_PROCHOT# pin. The temperature sensor is connected to the CPU temperature sensor (Q28) and the CORE\_PWM\_PROCHOT# pin.

Change EC SMBus PU voltage from +3V\_GFX to +3V\_S5 due to it also connect to CPU(SIC/SID) and GPU.

EC need read CPU temperature even in UMA mode or GPU off mode

CORE\_PWM\_PROCHOT# [4.25,29]

[illegible]

(KBC)

3V

R544  
10K/F\_4

[31] HWPG\_0.775VS5

[31] HWPG\_1.8VS5

[29] VRM\_PWRIGD

[26] HWPG\_VCDR

[26] HWPG\_0.9VS5

[26] SYS\_HWPG

[24] HWPG\_1.5V

[26] HWPG\_2.5V

1 2

D26 1N4148WS

D27 1N4148WS

D25 1N4148WS

D28 1N4148WS

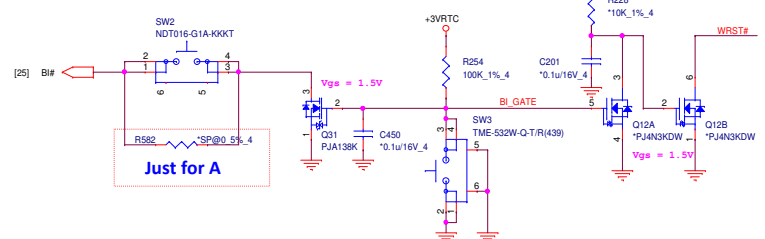
D28 1N4148WS

D29 1N4148WS

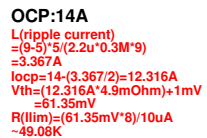
D24 1N4148WS

D23 1N4148WS

HWPG [5]

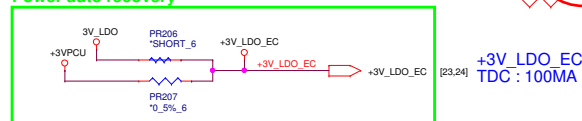




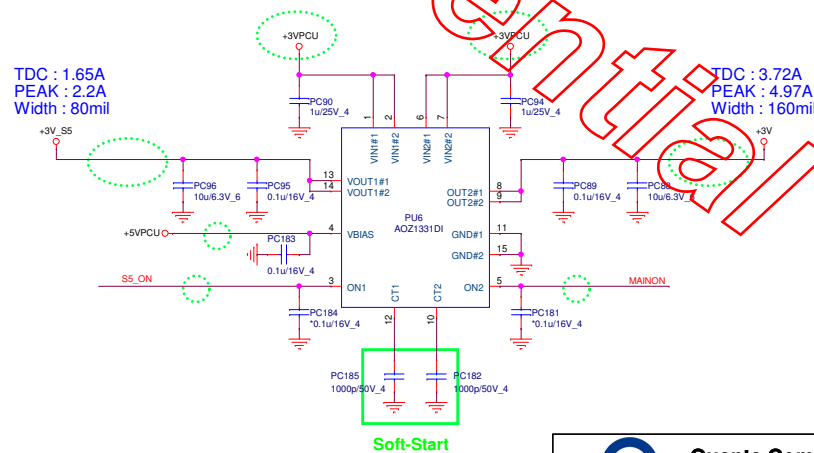


**Rds(on)=14.5m ohm**

**OCP:14A**  
 $L(\text{ripple current}) = (9 \cdot 3.3) \cdot 3.3 / (2 \cdot 2u \cdot 0.355M \cdot 9) \sim 2.676A$   
 $I_{ocp} = 14 - (2.676/2) = 13.162A$   
 $V_{th} = (12.662A \cdot 14.5m\Omega) + 1mV = 184.599mV$   
 $R(I_{lim}) = (184.599mV \cdot 8) / 10uA = 147.68K$



**For EC power auto recovery  
Don't change to short pad**





+VIN [11,15,22,25,26,28,30,31,32,33]  
 VDDP\_0.95V\_S5 [6,7,31]  
 VDDP\_0.95V [2,6,7,31]  
 +5VPCU [26,31]  
 +3V [4,5,6,7,9,11,12,13,14,15,16,17,18,19,22,23,24,26,28,29,31]

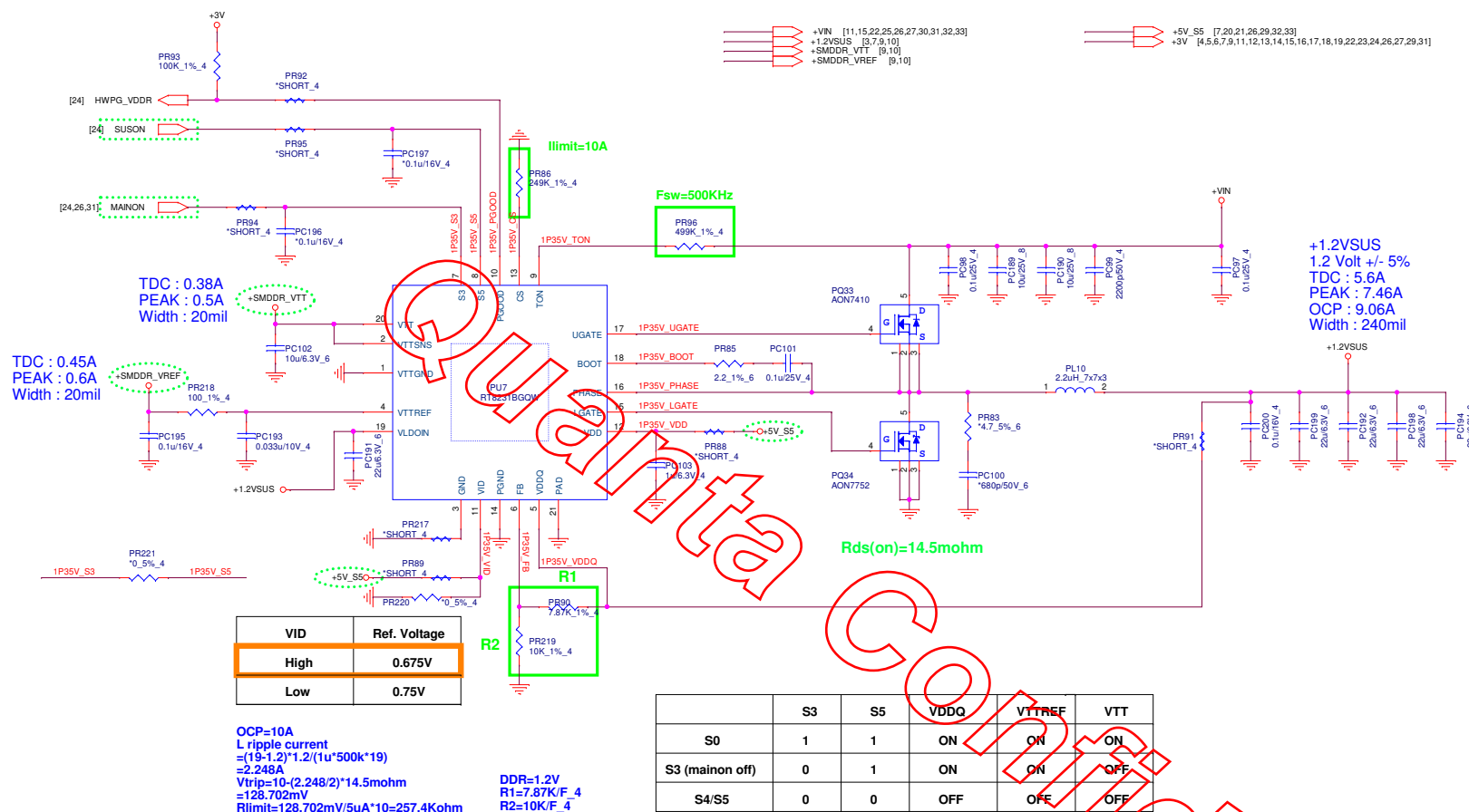
VDDP\_0.95V\_S5  
 0.95 Volt +/- 5%  
 TDC : 6.15A  
 PEAK : 8.2A  
 Width : 260mil

AMD requirements (depends on OPN)  
 Refer to datasheet...SR: 55366 / BR:53557 / SR FT4:55367  
 1.05V: 2.49K ohm, CS22492FB22  
 0.95V: 0 ohm, CS00002JB38

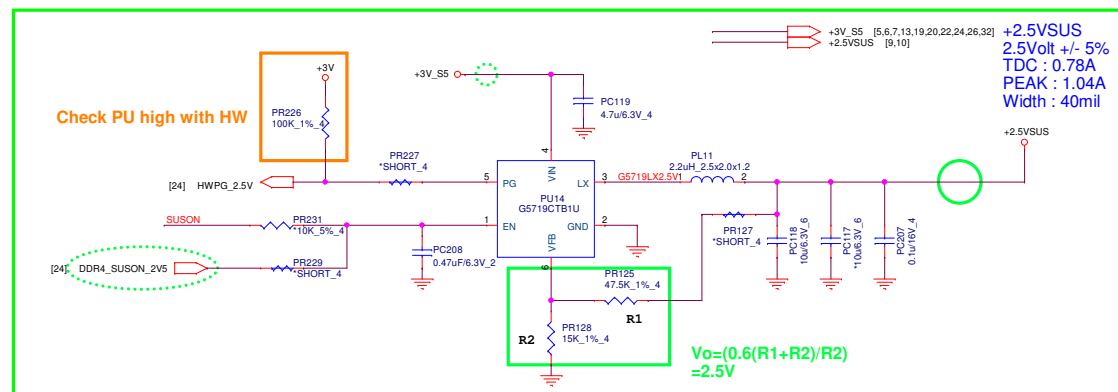
VDDP\_0.95V\_S5

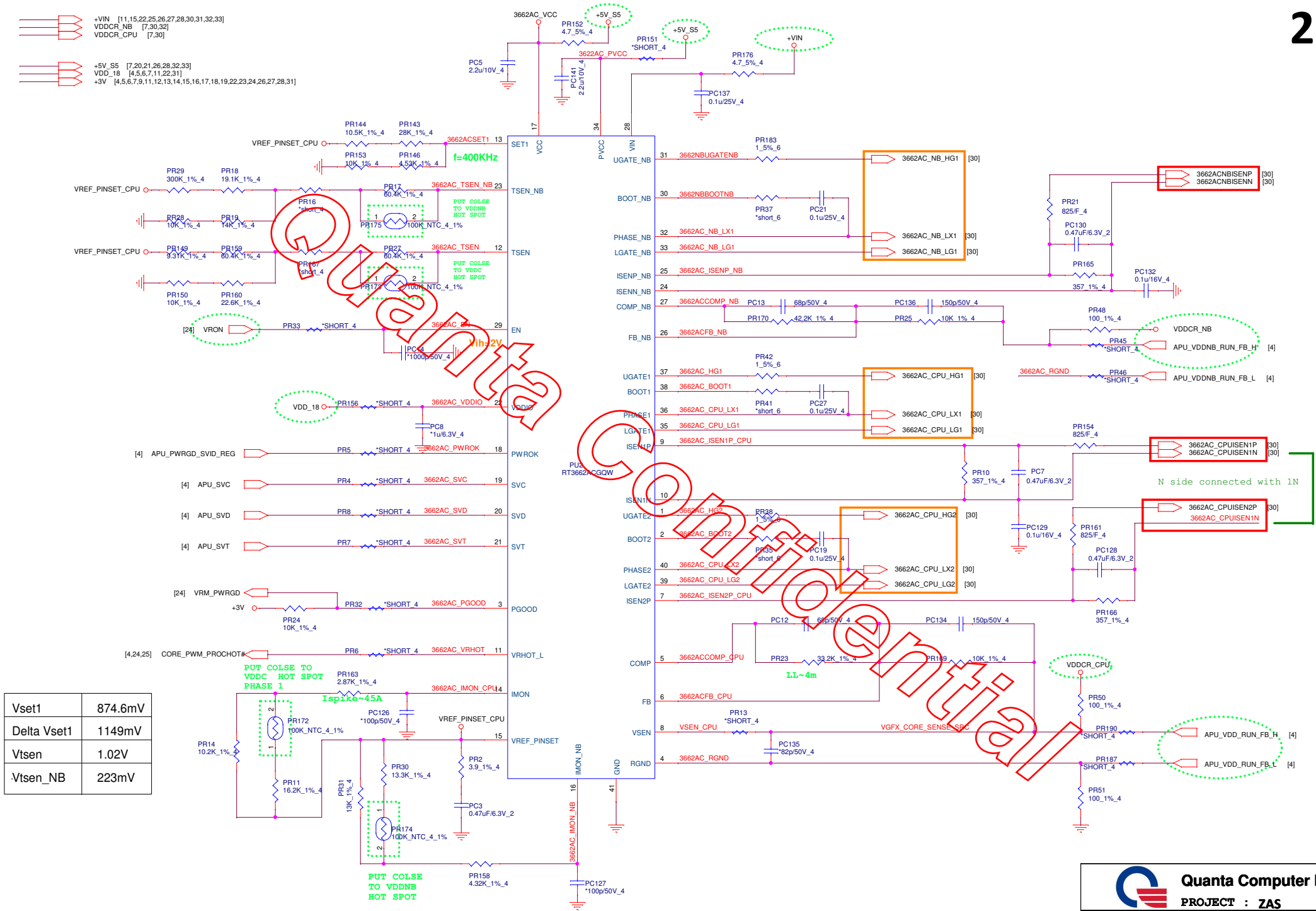
$$V_o = 0.8 * (R1 + R2) / R2 = 0.95V$$

+0.95V  
 TDC : 5.23A  
 PEAK : 7A  
 Width : 220mil

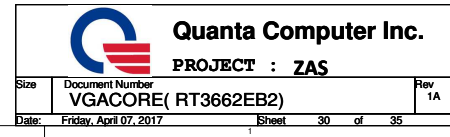
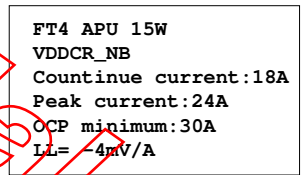
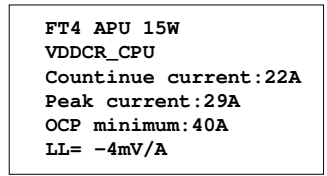


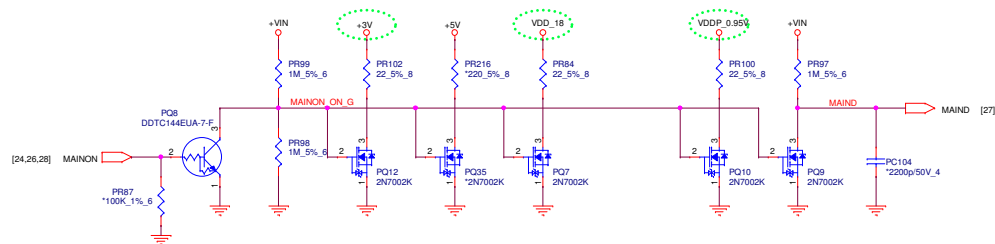
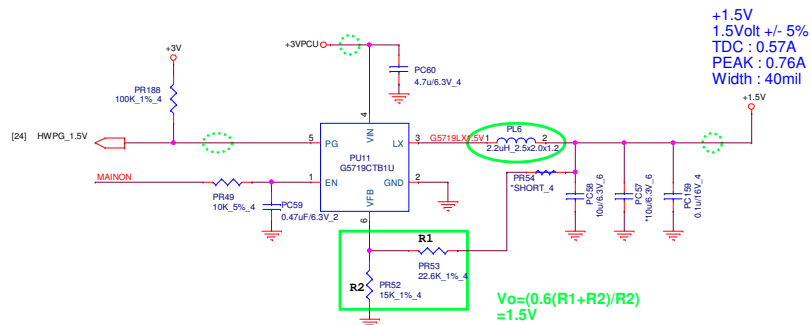
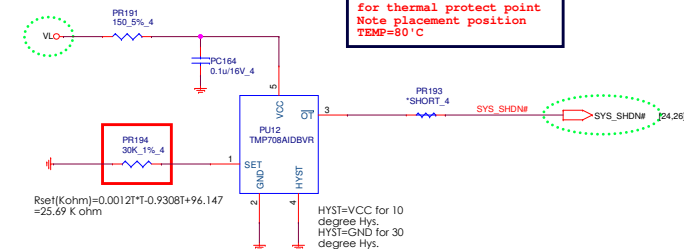
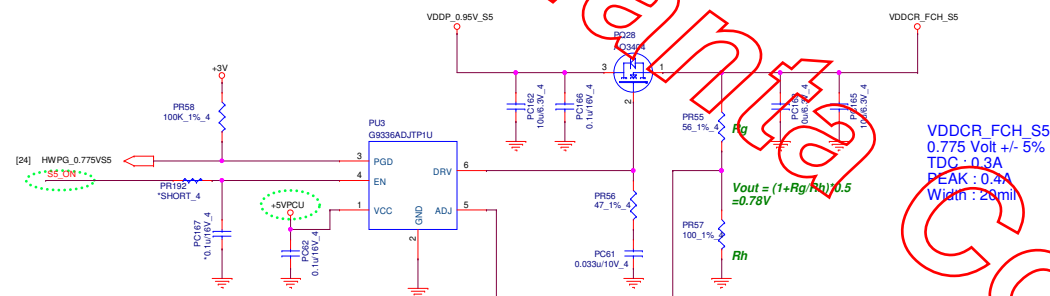
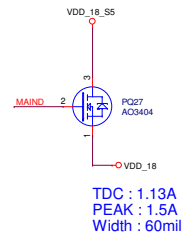
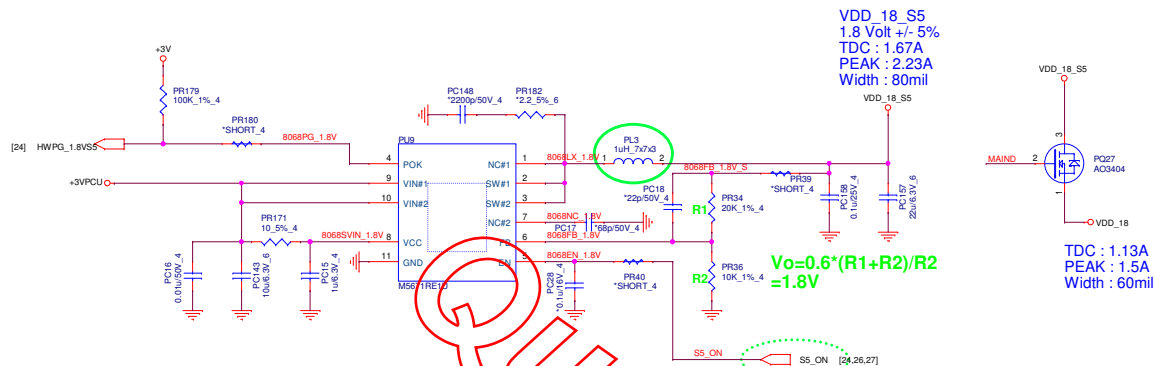
## +2.5VSUS Power Rail For DDR4



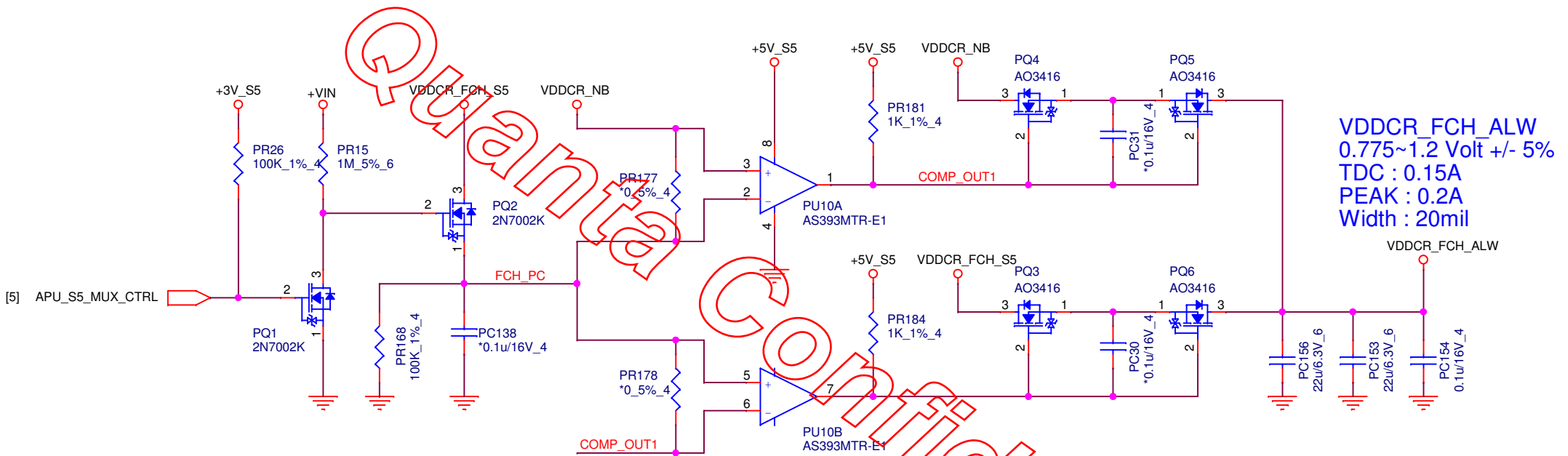


Vset1	874.6mV
Delta Vset1	1149mV
Vtsen	1.02V
Vtsen_NB	223mV






For Type 1 &amp; 3



VDDCR\_FCH\_ALW  
0.775~1.2 Volt +/- 5%  
TDC : 0.15A  
PEAK : 0.2A  
Width : 20mil

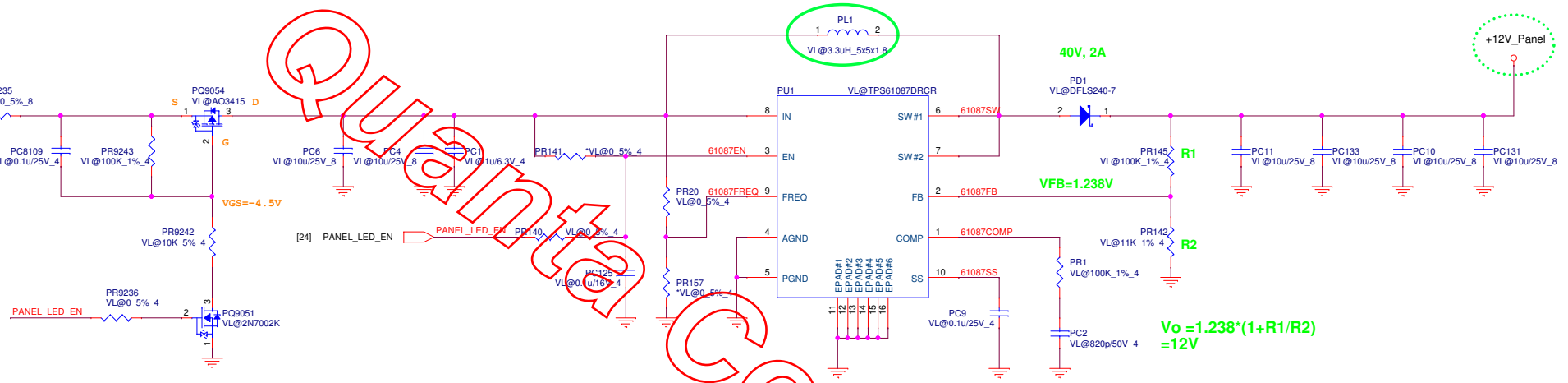
		
Quanta Computer Inc.		
PROJECT : ZAS		
Size	Document Number	Rev
	VDDCR_FCH_ALW	1A
Date:	Friday, April 07, 2017	Sheet 32 of 35



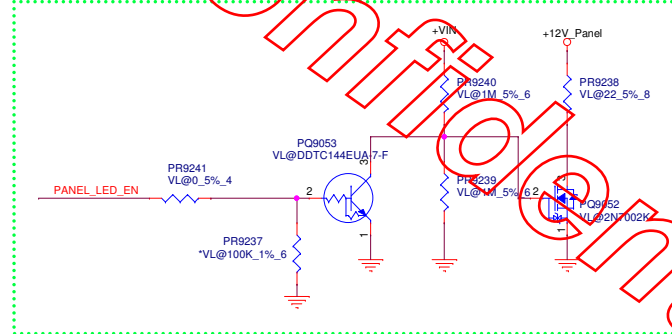
+5V\_S5 [7,20,21,26,28,29,32]  
+12V\_Panel [11]


Panel Spec (TFT-LCD 14")  
VLED : 6V~21V (Typ:12.5V)  
Power Consumption : 3W (MAX)

+12V\_Panel  
12.5 Volt +/- 5%  
PEAK : 0.35A  
Width : 20mil



#### BL Discharge Circuit



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<b>PROJECT :</b>			
Size	Document Number	Rev	
		1A	
Date:	Friday, April 07, 2017	Sheet	33 of 35

## Power Tree

