Vegas Schematic

KBL-R

2017/11/08

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

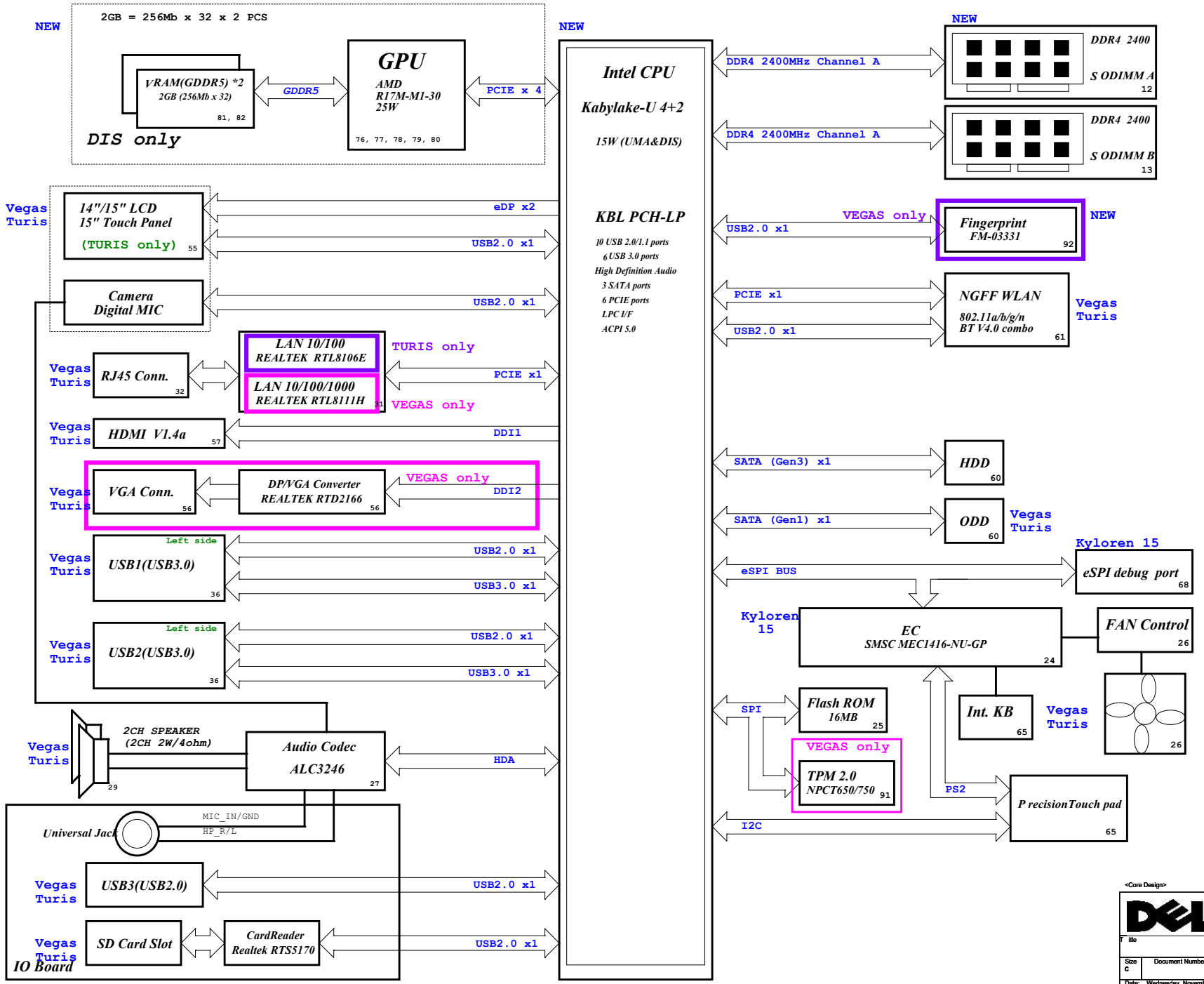
Title: Cover Page

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Wednesday, November 08, 2017 Sheet 1 of 105

Project code:
PCB P/N:17841-1
Revision: X02

Vegas/Turis MLK KBL-R Block Diagram



CHARGER
ISL88739 — 44

INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC
TPS51225RUKR-GP — 45

INPUTS	OUTPUTS
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5

CPU Core Power
NCP81208MNTXG — 46~50
NCP81382MNTXG x 2
NCP81382MNTXG (23e)
NCP81253MNTBG

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
DCBATOUT	+VCCGT
DCBATOUT	+VCCGT (23e)
DCBATOUT	+VCCSA

DDR4 SUS
RT8231AGQW-GP
APL5930KAI-TRG — 51

INPUTS	OUTPUTS
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3

CPU VCCPRIM_CORE 1V — 11

INPUTS	OUTPUTS
1D0V_S5	+VCCPRIM_CORE

CPU DCDC-V1D00A
AOZ2262QI-10-GP-U — 53

INPUTS	OUTPUTS
DCBATOUT	1D0V_S5

LDO-V1D8V
APL5930KAI-TRG — 54

INPUTS	OUTPUTS
3D3V_S5	1D8V_S5

5V/3V S0
TPS22966DPUR-GP — 40

INPUTS	OUTPUTS
5V_S5 3D3V_S5	5V_S0 3D3V_S0

EOPIO/EDRAM (23e)
TPS22961DNYT — 40

INPUTS	OUTPUTS
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR

3D3V VGA
AO3419L — 86

INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0

VGA_CORE
ISL62771HRTZ-GP-U — 85

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

1D5V_VGA_S0
Y8288RAC-GP — 86

INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0

<Core Design>

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Title: Block Diagram

Size	Document Number	Rev
C	Vegas SKL/KBL-U	A00

Date: Wednesday, November 08, 2017 | Sheet 2 of 105

Main Func = CPU

[PECI] and [PROCHOT#]
Impedance control: 50 ohm

[24] H_PECI
[24,44,46] H_PROCHOT#
[24,55] TOUCH_PANEL_INTR#
[24,65] INT_TP#

#544669 CRB Rev0.52

#543016 Rev0.7: Ra = 500 ohm / Rb = 1k ohm
#544669 Rev0.52:
Ra = 56 ohm (TO BE CHANGED TO 100 OHMS) / Rb = 62 ohm and 150 ohm

+VCCST_CPU
R419 1KR2J-1-GP
PCH_THERMTRIP

+VCCSTG = 1.0 V
+VCCSTG
R401 1KR2J-1-GP
Ra
R403 499R2F-2-GP
H_PROCHOT#

TPAD14-OP-GP TP401
TPAD14-OP-GP TP402
TPAD14-OP-GP TP405
TPAD14-OP-GP TP406
TPAD14-OP-GP TP407
TPAD14-OP-GP TP408
TPAD14-OP-GP TP404
INT_TP# R410 0R0402-PAD

H_CATERR# D63
H_PECI A54
H_PROCHOT#_R C65
PCH_THERMTRIP C63
SKTOCC# A65
XDP_BPM0 C55
XDP_BPM1 D55
XDP_BPM2 B54
XDP_BPM3 C56
TOUCH_PANEL_INTR# A6
TOUCHPAD_INTR# A7
GPP_B4/CPU_GP3 BA5
AY5

R412 49D9R2F-L1-GP
R413 49D9R2F-L1-GP
R414 49D9R2F-L1-GP
R415 49D9R2F-L1-GP
CPU_POPIRCOMP AT16
PCH_POPIRCOMP AU16
EDRAM_OPIO_RCOMP H66
EOPIO_RCOMP H65

CPU1D 4 OF 20
SKYLAKE_ULT
CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#
CPU MISC
BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]
GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3
PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP
SKYLAKE-U-GP

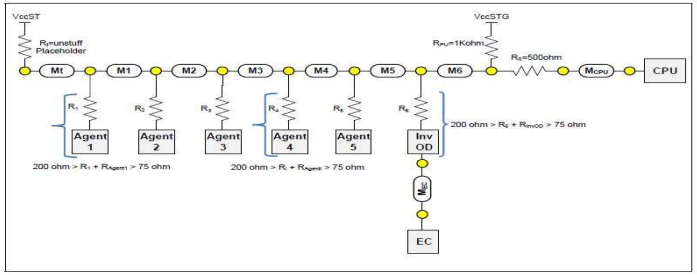
JTAG
PROC_TCK B61 XDP_TCLK
PROC_TDI D60 XDP_TDI
PROC_TDO A61 XDP_TDO_CPU
PROC_TMS C60 XDP_TMS
PROC_TRST# B59 XDP_TRST#
PCH_JTAG_TCK B56 PCH_JTAG_TCK
PCH_JTAG_TDI D59 PCH_JTAG_TDI
PCH_JTAG_TDO A56 PCH_JTAG_TDO
PCH_JTAG_TMS C59 PCH_JTAG_TMS
PCH_TRST# C61 XDP_TRST#
JTAGX A59 XDP_TCK_JTAGX

XDP_TRST# DY EC401 SC1KP50V2KX-L-1-GP

+VCCSTG = 1.0 V
+VCCSTG
XDP_TMS R421 DY 51R2J-2-GP
XDP_TDI R422 DY 51R2J-2-GP
XDP_TDO_CPU R423 DY 51R2J-2-GP
PCH_JTAG_TDI R408 51R2J-2-GP
0525 Follow KY15 & SF
PCH_JTAG_TDO R409 51R2J-2-GP
PCH_JTAG_TMS R416 51R2J-2-GP
XDP_TCK_JTAGX R417 DY 1KR2J-1-GP
XDP_TRST# R402 DY 51R2J-2-GP
XDP_TCLK R406 51R2J-2-GP
PCH_JTAG_TCK R407 DY 51R2J-2-GP

(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

<Core Design>

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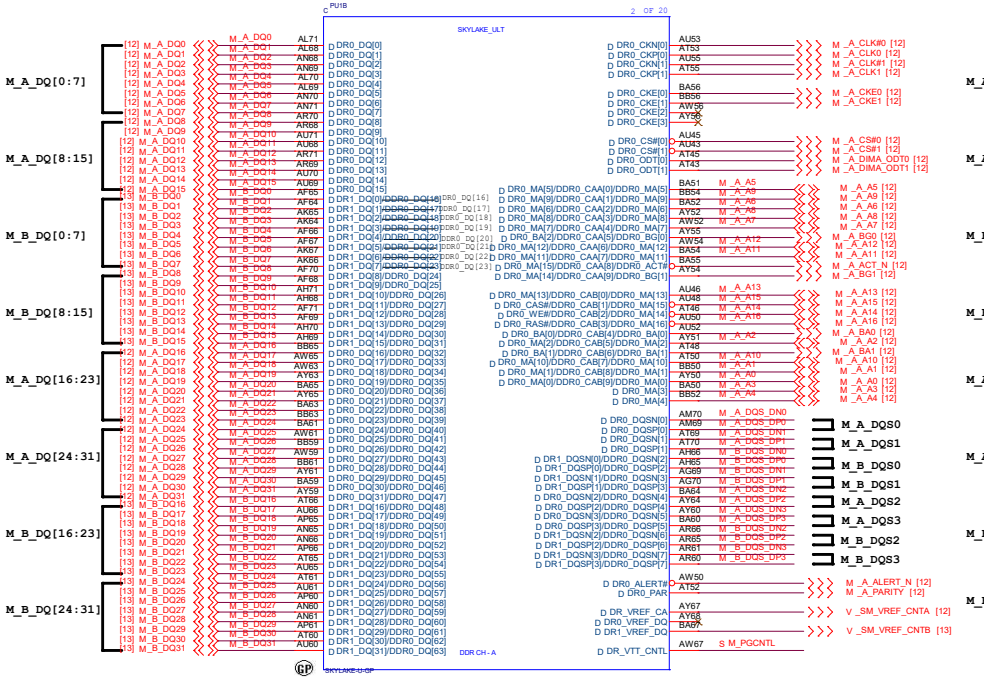
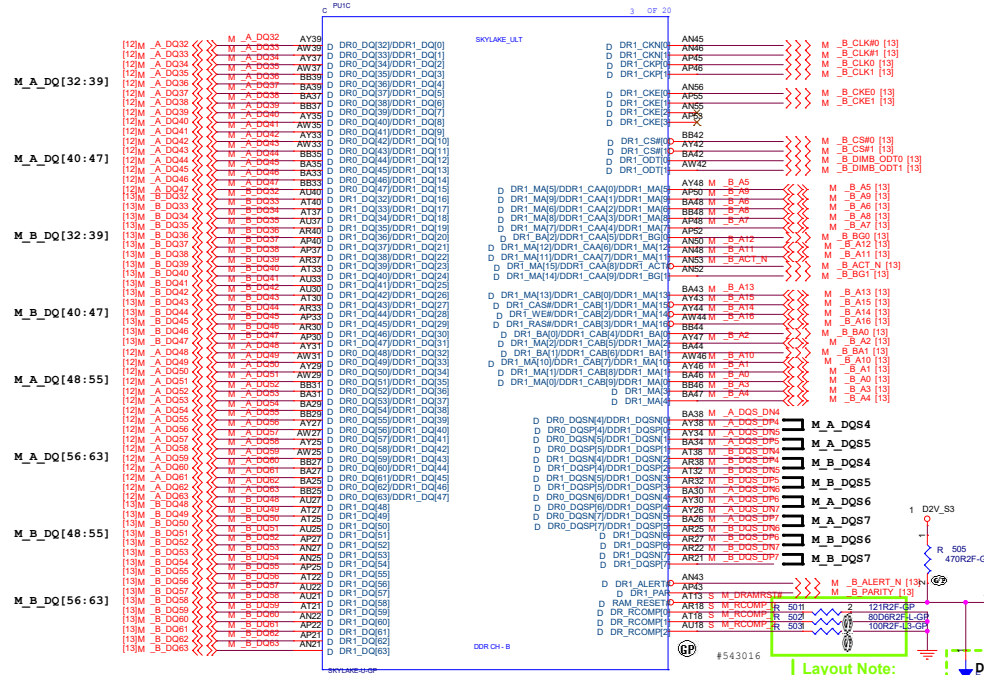
Title: CPU_(JTAG/CPU SIDE BAND)
Size: A3
Document Number: Vegas SKL/KBL-U
Rev: A00
Date: Wednesday, November 08, 2017
Sheet 4 of 105

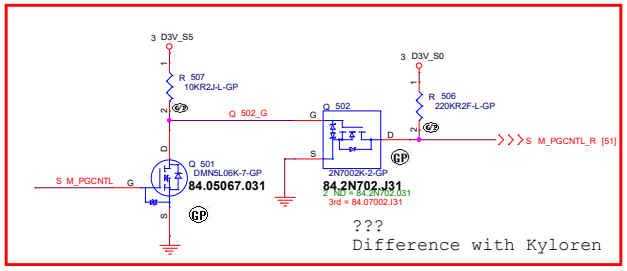
Main Func = CPU

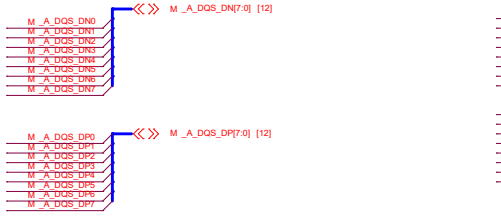
DDR4 ball type: Interleaved Type

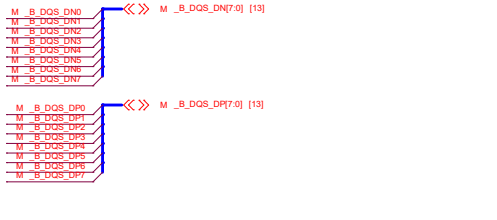




DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel.
Clock (CLK and CLK#) and Strobe (DQS and DQS#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.







PDG: DDR/ODT

4.17 SKL U and SKL Y System Memory ODT Signal Connectivity Details

Table 4-41. ODT Signals Connectivity table

Processor	Memory Type	Side	Signal	Rule	Notes
SKL-Y	LPDDR3 Memory Down	Processor	DDR0_ODT[0] DDR1_ODT[0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
SKL-U	LPDDR3 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' ODT. T-topology connection. Processor's ODT[1] not connected.	1,2
		DRAMs	One ODT per x32 DRAM PKG Two ODT per x64 DRAM PKG		
	DDR3L Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT . Processor's ODT[1] connected to DRAMs' Rank1 ODT. If Rank1 not used, Processor ODT[1] not connected.	3,4
		DRAMs	ODT[1:0]		
	DDR3L SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] connected to DIMMs ODT[1:0].	1,3
		DIMMs	ODT[1:0]		
	DDR3L Mixed Memory Down and SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's SODIMM Channel ODT[1:0] connected to DIMM. Processor's Memory Down channel - ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT. If rank1 not used, ODT[1] not connected.	3,4
		DIMM	ODT[1:0]		
		DRAMs	ODT[1:0]		
	DDR4 Memory Down	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used, Processor ODT[1] not connected.	
		DRAMs	ODT[1:0]		
	DDR4 SO-DIMM	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.	
		DIMMs	ODT[1:0]		

Notes:
1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files (RVP3 - SKL-Y LPDDR3, RVP5 - SKL-U LPDDR3).
2. LPDDR3 Rank1 ODT is always disabled by BIOS/MRC. ODT signal is controlling only Rank0 ODT.
3. DDR3L ODT input is held high (Active). RTT NOM is defined by BIOS as High-Z in both ranks, when a Rank receives write command it enables RTT WR (set by BIOS after power training). Otherwise ODT gets RTT NOM (High-Z)
4. These guidelines are related to DDR3L supported Memory down topologies only. 2R x16 DDP single side, 2R x16 SDP dual sided and 2Rx8 dual side.

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.
close to CPU

Layout Note:

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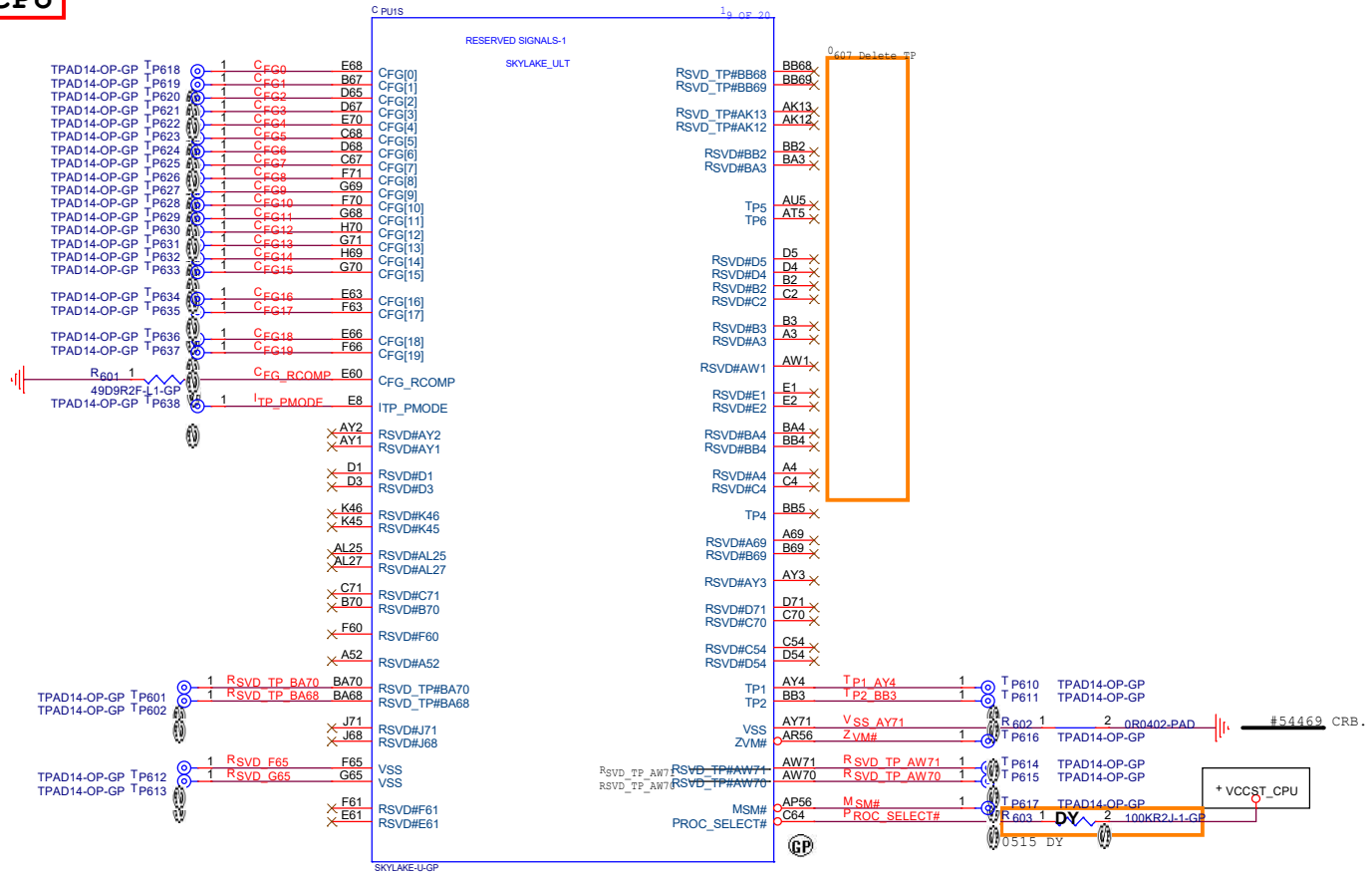
Title: CPU_(DDR)

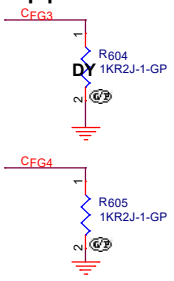
Size	Document Number	Rev
A 2	Vegas SKL/KBL-U	A 00

Date: Wednesday, November 08, 2017 Sheet 5 of 105

Main Func = CPU



PCH strap pin:



[BDW Only]PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

(#543016)

DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED An external Display Port device is connected to the Embedded Display Port.
	1 : DISABLED (Default) No Physical Display Port attached to Embedded DisplayPort*. No connect for disable.

CFG TERMINATIONS

#544669 Rev0.52 (CRB)

20140807 david

SKL(#543016):
Processor strap CFG[4] should be pulled low to enable embedded DisplayPort*

<Core Design>

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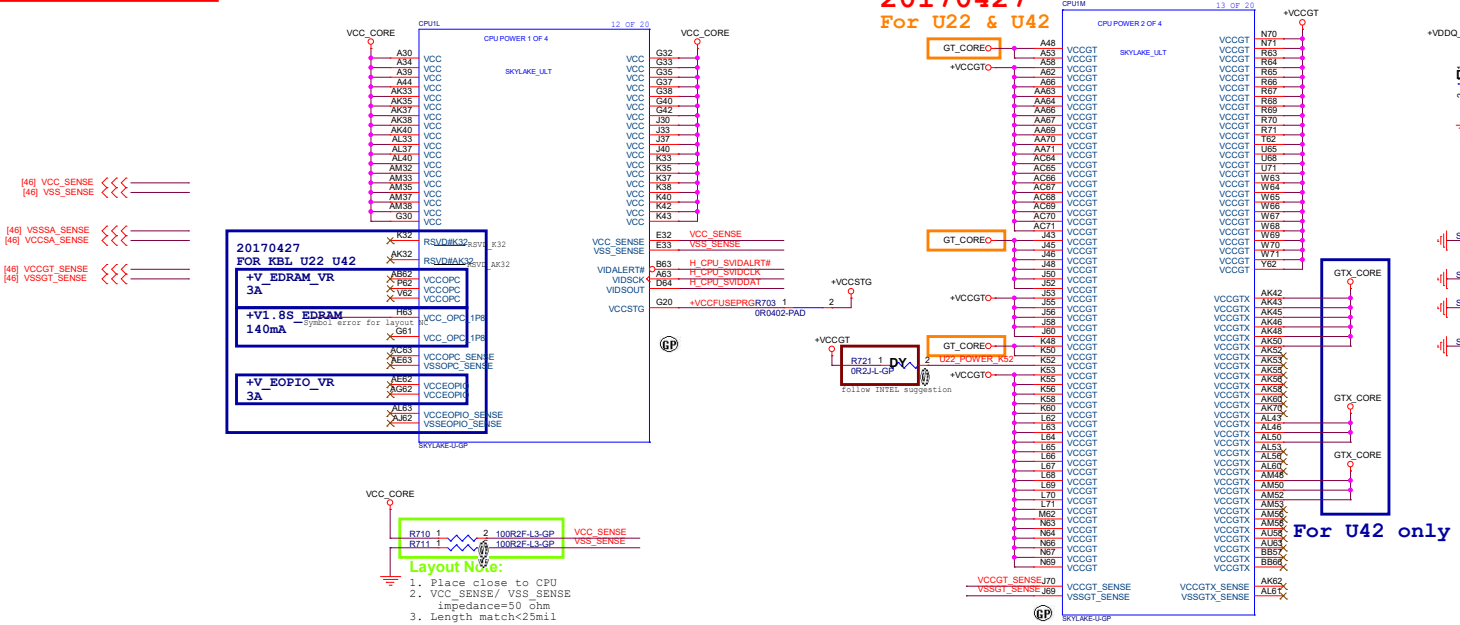
Title: CPU_(RESERVED)

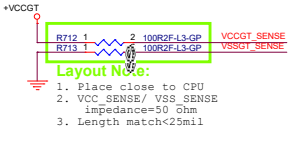
Size	Document Number	Rev
A 3	Vegas SKL/KBL-U	A00

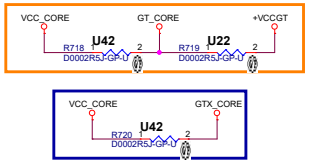
Date: Wednesday, November 08, 2017 Sheet 6 of 105

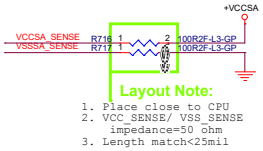
Main Func = CPU

20170427
For U22 & U42



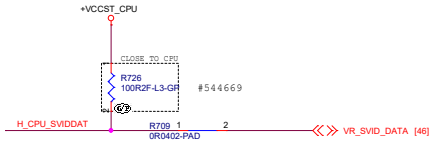




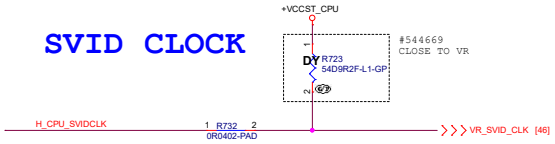


Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.

SVID DATA



SVID CLOCK



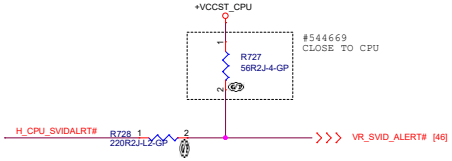
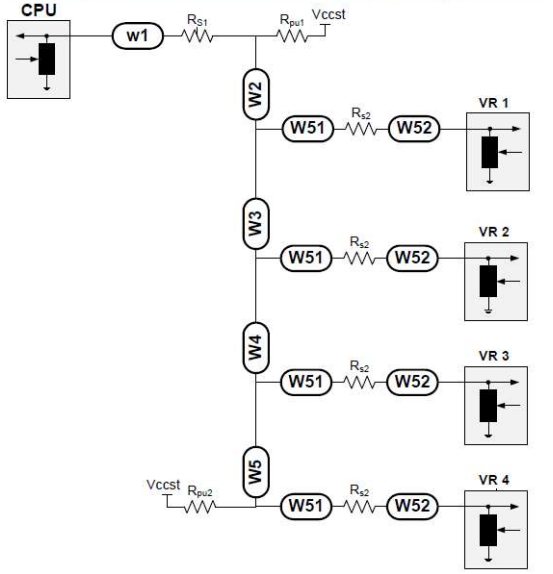


Figure 10-7. Routing Illustration for SVID Topology



SVID_543016:

Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W51 [inches]	W52 [inches]	R_{pu1} [Ω]	R_{pu2} [Ω]	R_{s1} [Ω]	R_{s2} [Ω]	VCC_{GT} [v]
VIDSOUT	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	100	100	0	10	1.0
VIDSCK							Empty	45	0	50	
VIDALERT #							56	Empty	220	0	

<Core Design>
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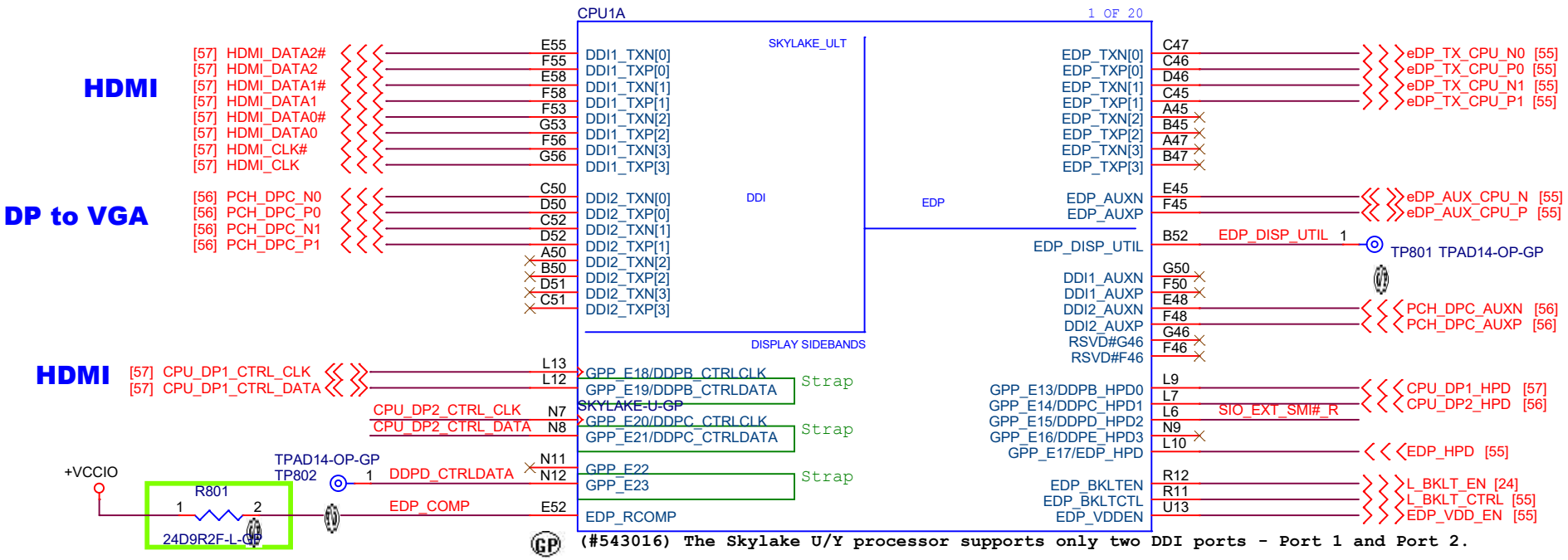
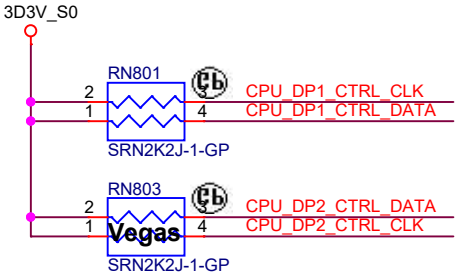
Title: CPU(VCC_CORE)
Size: A2 | Document Number: Turis/Vegas KBL-R | Rev: A00
Date: Wednesday, November 08, 2017 | Sheet 7 of 105

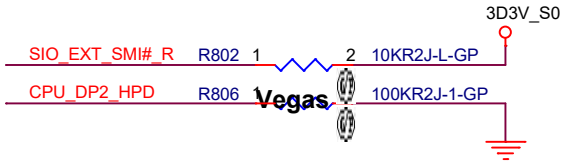
Main Func = CPU



(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 ±1% Ω resistor.





(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

These two signals have weak internal pull-down.

<Core Design>

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Title: **CPU_(DISPLAY)**

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Wednesday, November 08, 2017 Sheet 8 of 105

Main Func = CPU

CORE

VCC_CORE

U-line 23e 28W
IccMax current-10ms max = 34 A

PC1001 PC1002 PC1003 PC1004 PC1005 PC1006 PC1007 PC1008 PC1009 PC1010 PC1011 DY PC1012 PC1013 PC1014 DY PC1015

SC22U6D3V3MX-1-GP ×15

22U 0603 x 22

PC1016 PC1017 PC1018 PC1019 PC1020 PC1021 PC1022 PC1023 PC1024 DY PC1025 DY PC1026 PC1027 PC1028 PC1029 PC1030

SC22U6D3V3MX-1-GP ×15

PC1040 PC1066 PC1067 PC1068 PC1097 PC1099

U42 U42 U42 DY U42 U42

SC22U6D3V3MX-1-GP ×6

+VCCIO

+VCCIO(ICCMAX.=2.73A)

PC1035 PC1036 DY PC1037

SC22U6D3V3MX-1-GP ×3

1D0V_S5

PC1038 PC1039

20170810
New Common Part

SC22U6D3V3MX-1-DL-GP ×2

SLICED GT

+VCCGT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

22U 0603 x28

PC1031 PC1032 PC1033 PC1034 PC1041 PC1042 PC1043 PC1044 PC1069 PC1070 PC1071 DY PC1072 DY PC1073 PC1074 PC1075

SC22U6D3V3MX-1-GP ×15

PC1076 PC1077 PC1078 PC1079 DY PC1080 PC1081 PC1082 PC1083 PC1084 PC1085 PC1086 PC1087 PC1088 PC1089 PC1090 DY

SC22U6D3V3MX-1-GP ×15

PC1091 DY PC1092 DY PC1093 DY PC1094 DY PC1095 PC1096

SC22U6D3V3MX-1-GP ×6

PC1053 U42 PC1065 U42

SC22U6D3V3MX-1-GP ×2

KBL-R U42 / KBL U 22 Decoupling Requirements (Sheet 2 of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc_{PLL}		1x 1 uF 0402	Place as close to the package as possible.
Vcc_{PLL_OC}		1x 1 uF 0201	Do not route Vcc_{PLL}, Vcc_{PLL_OC}, Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{ST}		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

1D2V_S3

10U 0603 x 4

(#543016 PDG)

PC1055 PC1057 PC1058 PC1056 PC1059 PC1060 PC1061 PC1062 PC1063 PC1064

SC10U6D3V3MX-GP ×3

DY DY DY DY DY DY

SC4D7P50V2BN-GP ×4

SC22U6D3V3MX-1-GP ×3

VCCSA

+VCCSA

22U 0603 x 8

PC1045 PC1046 PC1047 PC1048 PC1049 PC1050 PC1051 PC1052 PC1054 PC1098

DY DY

SC22U6D3V3MX-1-GP ×10

Bulk Decoupling Example (KBL-R U42/KBL U22)

Bulk Decoupling Locations	Example - U 4+2	Example - U 2+2	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR)	1x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mO ESR)		Placed at backside side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220 uF (@4.5mO ESR)		Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{IO} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{SA} Power Plane at VR output	2x 47 uF 0805		Placed at primary side near to VR output
Vcc_{PLL} Power Plane at V1P0A VR output	1x 0.1uF 0402		Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

KBL-R U42 / KBL U 22 Decoupling Requirements (Sheet 1of 3)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	31x 1 uF 0402 or 0201		Refer to diagram in Note 4 below for placement recommendation of 0402 caps Refer to diagram in Note 5 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
		8x 10 uF 0402	
Vcc/Vcc_{GT}	5x 1 uF 0402 or 0201		Place as close to the package as possible
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
Vcc_{SA}	7x 10 uF 0402	3x 47 uF 0805 (6.3V)[1]	Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.

Note: Refer to latest revision of KBL- RU PDG for final specifications

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(Power CAP1)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 10 of 105

Main Func = CPU

PCH DERIVED RAILS

1D0V_S5 → +VCCPRIM_CORE
R1101 1 — 2 : 0R1206-PAD

+V1.00A_SIP
R1117 1 — 2 : 0R0603-PAD-2-GP-U
C1108 : SC22U6D3V3MX-1-GP

3D3V_S5_PCH → +V3.3A_SIP
R1110 1 — 2 : 0R0603-PAD-2-GP-U
C1104 : SC22U6D3V3MX-1-GP

1D8V_S5 → +V1.8A_SIP
R1139 1 — 2 : 0R0603-PAD-2-GP-U
C1106 : SC22U6D3V3MX-1-GP

UNSLICED GT

+VCCGT
1U 0402 x 6
C1136 DY : SC1U10V2KX-1GP
C1138 DY : SC1U10V2KX-1GP
C1147 DY : SC1U10V2KX-1GP
C1148 : SC1U10V2KX-1GP
C1149 DY : SC1U10V2KX-1GP
C1150 : SC1U10V2KX-1GP

VCCIO

+VCCIO
+VCCIO(ICCMAX.=2.73A)
C1151 DY : SC1U10V2KX-1GP
C1152 : SC1U10V2KX-1GP
C1153 : SC1U10V2KX-1GP
C1154 : SC1U10V2KX-1GP

+VCCMPHYGTAON_1P0(ICCMAX.=2.12A)

+VCCMPHYGTAON_1P0_LS_SIP
C1182 : SC22U6D3V3MX-1-GP
C1174 : SC1U10V2KX-1GP

+VCCMPHYGTAON_1P0_LS_SIP
C1173 : SC1U10V2KX-1GP
C1180 : SC1U10V2KX-1GP

+VCCMPHYGTAON_1P0_LS_SIP
C1184 : SC22U6D3V3MX-1-GP
C1172 : SC1U10V2KX-1GP

+VCCMPHYGTAON_1P0_LS_SIP
C1176 : SC10U6D3V3MX-GP
C1175 : SC1U10V2KX-1GP

Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

VCC_CORE
1U 0402 x 5
U-line 23e 28W
IccMax current-10ms max = 34 A
C1101 : SC1U10V2KX-1GP
C1102 : SC1U10V2KX-1GP
C1103 : SC1U10V2KX-1GP
C1116 : SC1U10V2KX-1GP
C1117 : SC1U10V2KX-1GP

+VCCPRIM_CORE
PC1105 : SC22U6D3V3MX-1-GP
PC1106 : SC22U6D3V3MX-1-GP

+V3.3A_SIP
C1183 : SC10U6D3V3MX-GP

<Core Design>

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Title	CPU_(Power CAP2)	
Size: Custom	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 11 of 105	

Main Func = DDR4 SODIMM

20170502 DM1
062.10011.00U1>
062.10011.01C1

DM1A 1 OF 4
DDR4-260P-65-GP
062.10011.01C1

DM1B 2 OF 4
DDR4-260P-65-GP

DM1C 3 OF 4
DDR4-260P-65-GP

DM1D 4 OF 4
DDR4-260P-65-GP

UN 0225

???跟sw確認
DDR4 SWAP 0212

for placement modify 2015/10/19

Layout note: closed to Dimm

<Core Design>

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Title: DDR4-SODIMM1
Size: Custom
Document Number: Vegas SKL/KBL-U
Rev: A00
Date: Wednesday, November 08, 2017
Sheet 12 of 106

Main Func = DDR4 SODIMM

20170502 DM1
062.10011.00T1>
062.10011.01B1

DM2A 1 OF 4
DDR4-260P-64-GP
062.10011.01B1

DM2C 3 OF 4
DDR4-260P-64-GP

DM2B 2 OF 4
DDR4-260P-64-GP

DM2D 4 OF 4
DDR4-260P-64-GP

跟sw確認 DDR4 SWAP 0212

Layout note: closed to Dimm
0921 Install

UN 0225

<Core Design>

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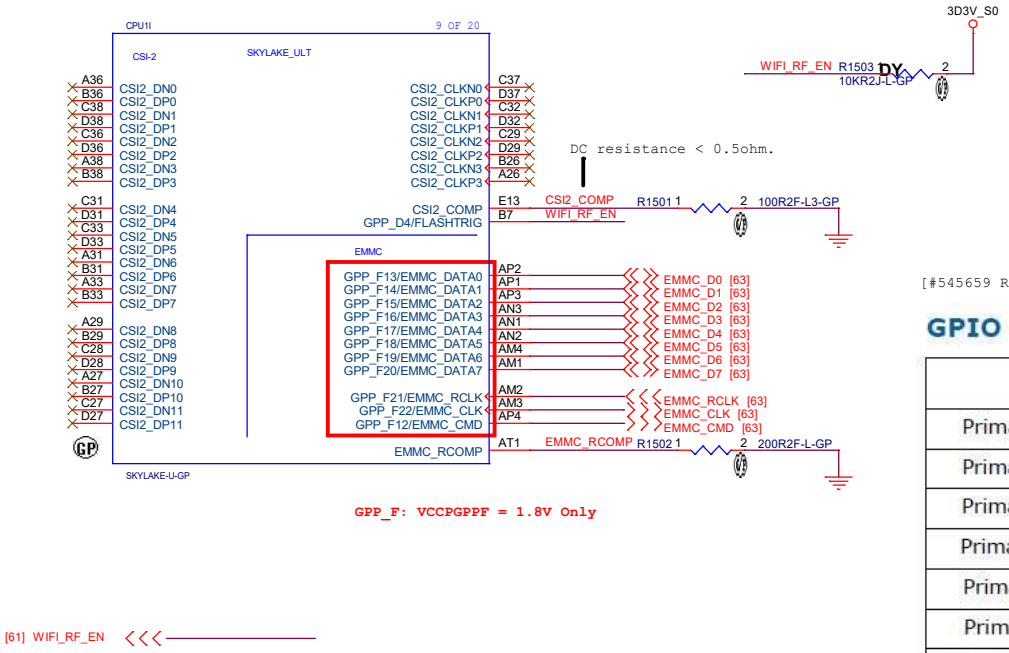
Title: DDR4-SODIMM1
Size: Custom
Document Number: Vegas SKL/KBL-U
Rev: A00
Date: Wednesday, November 08, 2017
Sheet 13 of 106

Main Func = PCH



GPP_F: VCCPGPPF = 1.8V Only

[61] WIFI_RF_EN

Table 8-1. Switchable Graphics GPIO Requirements

GPIO	Usage
DGPU_PWR_EN#	BIOS drives to turn on/off the discrete graphics power.
DGPU_PWROK	dGPU voltage regulator drives to indicate power status to the PCH. It enables clocks to dGPU.
DGPU_HOLD_RST#	Discrete Graphics Enable signal. BIOS controls and a PCH GPIO drives. It gates Platform Reset to enable Reset for the dGPU.
DGPU_PRSNT#	Used only by the CRB or if Graphic Cards requiring AC caps on the motherboard or add-in card is supported on the platform to indicate that a card is present.

[#545659 Rev0.7]

GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCPGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCPGPPB	1.8V or 3.3V
Primary Well Group C (GPP_C)	VCCPGPPC	1.8V or 3.3V
Primary Well Group D (GPP_D)	VCCPGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCPGPPE	1.8V or 3.3V
Primary Well Group F (GPP_F)	VCCPGPPF	1.8V
Primary Well Group G (GPP_G)	VCCPGPPG	1.8V or 3.3V
Deep Sleep Well Group (GPD)	VCCPDSW_3p3	3.3V

<Core Design>

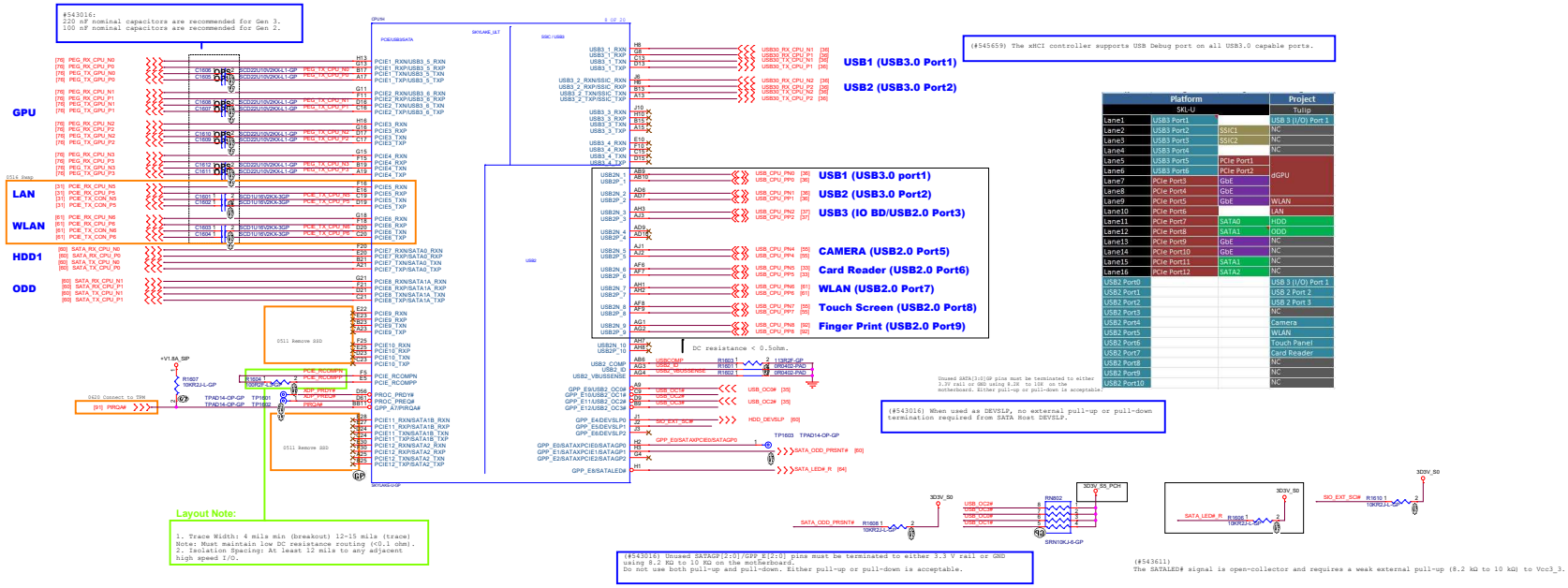
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(CS-2/EMMC)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 15 of 105

Main Func = PCH



Platform SKL-U	Project Tulip
Lane1 USB3 Port1	USB 3 (I/O) Port 1
Lane2 USB3 Port2 SSIC1	NC
Lane3 USB3 Port3 SSIC2	NC
Lane4 USB3 Port4	NC
Lane5 USB3 Port5 PCIe Port1	dGPU
Lane6 USB3 Port6 PCIe Port2	dGPU
Lane7 PCIe Port3 GbE	dGPU
Lane8 PCIe Port4 GbE	dGPU
Lane9 PCIe Port5 GbE	WLAN
Lane10 PCIe Port6	LAN
Lane11 PCIe Port7 SATA0	HDD
Lane12 PCIe Port8 SATA1	ODD
Lane13 PCIe Port9 GbE	NC
Lane14 PCIe Port10 GbE	NC
Lane15 PCIe Port11 SATA1	NC
Lane16 PCIe Port12 SATA2	NC
USB2 Port0	USB 3 (I/O) Port 1
USB2 Port1	USB 2 Port 2
USB2 Port2	USB 2 Port 3
USB2 Port3	NC
USB2 Port4	Camera
USB2 Port5	WLAN
USB2 Port6	Touch Panel
USB2 Port7	Card Reader
USB2 Port8	NC
USB2 Port9	NC
USB2 Port10	NC

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN	
5 (L0~L3)	GPU	
6 (L3)	HDD	SATA0
6 (L2)	ODD	SATA1
6 (L0~L1)	N/A	

USB 2.0 Table

Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3 (IOBD)
3	Finger Print
4	CAMERA
5	Card Reader
6	Touch Panel
7	WLAN

#545659 (SKL_PCH_U_Y_EDS Rev0.7)

Figure 3-1. HSIO Muxing on SKL PCH-LP (U Series)

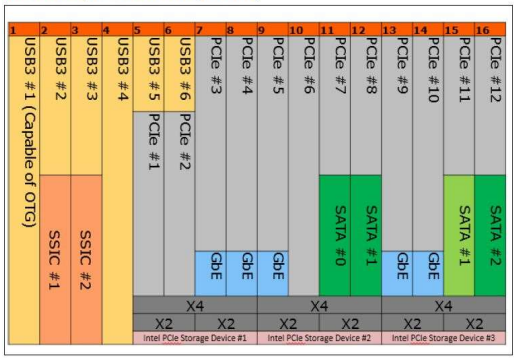


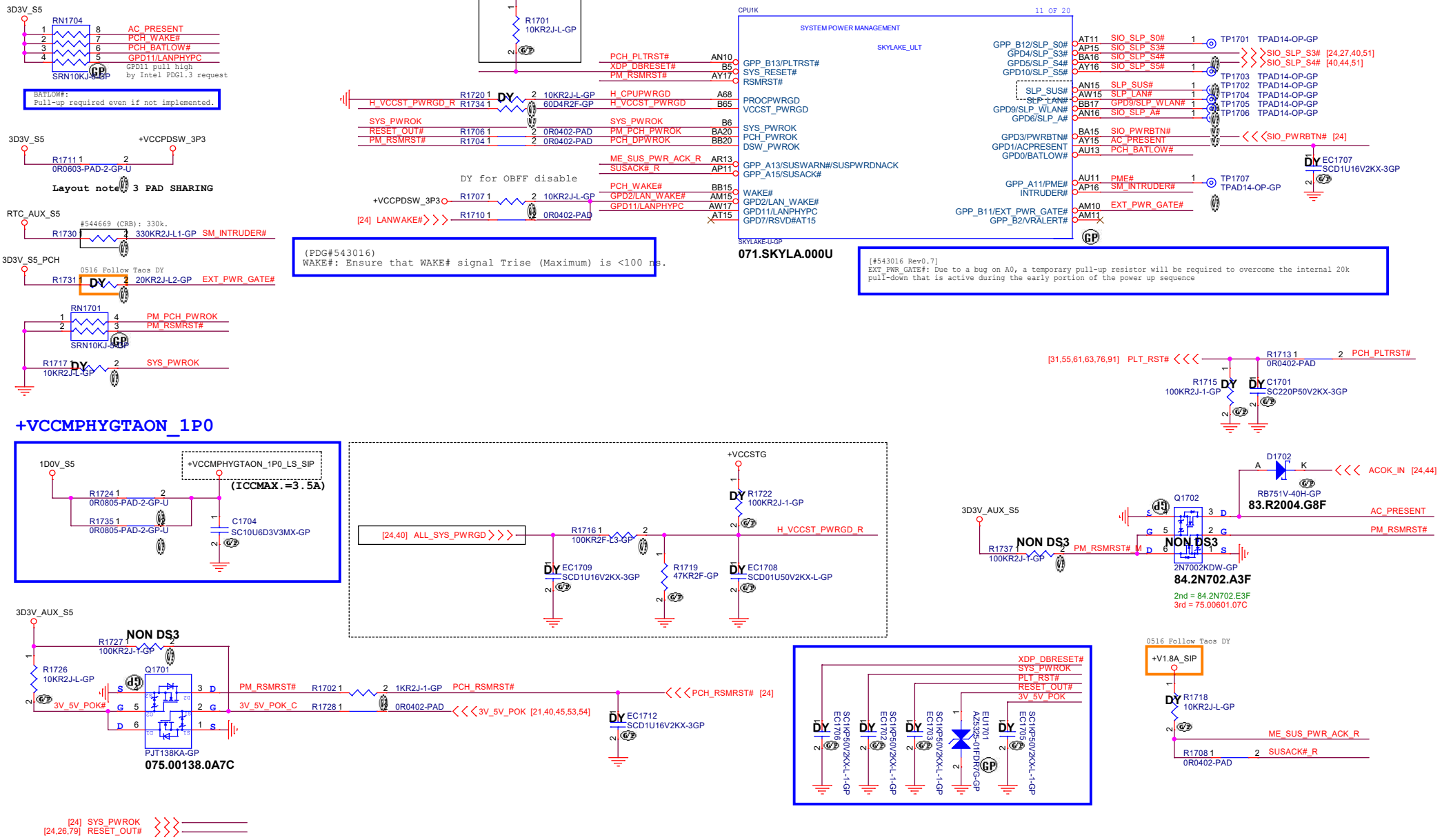
Table 24-2. PCI Express* Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s) x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

Table 24-3. PCI Express* Link Configurations Supported

SKL	PCIe Link Config	PCI Express* Lanes 1	2	3	4	5	6	7	8	9	10	11	12
U	1x4	Port1				Port5				Port9			
	2x2	Port1		Port3		Port5		Port7		Port9		Port11	
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8	Port9		Port11	Port12
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8	Port9	Port10	Port11	Port12
Y	1x4	Port1				Port5							
	2x2	Port1		Port3		Port5		Port7					
	1x2 + 2x1	Port1		Port3	Port4	Port5		Port7	Port8				
	4x1	Port1	Port2	Port3	Port4	Port5	Port6	Port7	Port8				
	1x2									Port9			
	2x1									Port9	Port10		

Main Func = PCH



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(POWER MANAGEMENT)

Size	Document Number	Rev
A3	Turis/Vegas KBL-R	A00

Date: Wednesday, November 08, 2017 Sheet 17 of 105

Main Func = PCH

PCH strap pin:

eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

This signal has a weak internal pull-down.

PCH strap pin:

BOOT HALT	
SPI0_MOSI	0 = ENABLED 1 = DISABLED WEAK INTERNAL PU

This signal has a weak internal pull-up.

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

eSPI

For eSPI

20170428

84.2N702.J31

2ND = 84.2N702.031
3rd = 84.07002.I31

82.30001.A41

84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

Layout: Place at the open door area.

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (LPC/SPI/SMBUS/CL/CLK)

Size	Document Number	Rev
Custom	Turis/Vegas KBL-R	A00

Date: Wednesday, November 08, 2017 Sheet 18 of 105

Main Func = PCH

PCH strap pin:

Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

[24,79,85] DGPU_PWROK

[27] HDA_CODEC_BITCLK

[27] HDA_CODEC_SDOUT

[27] HDA_CODEC_SYNC

[27] HDA_SDIN0

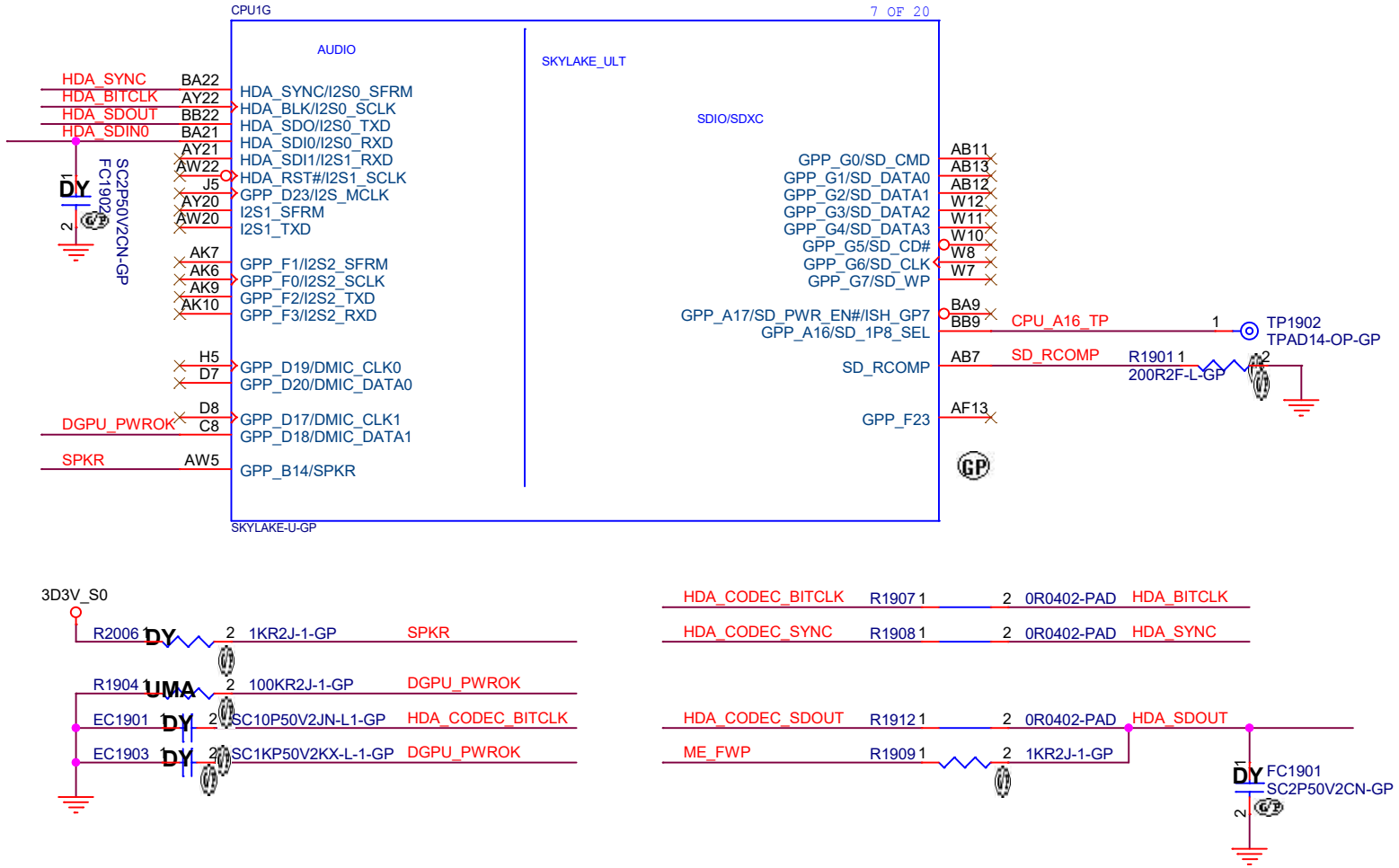
[24] ME_FWP

[27] SPKR

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



<Core Design>

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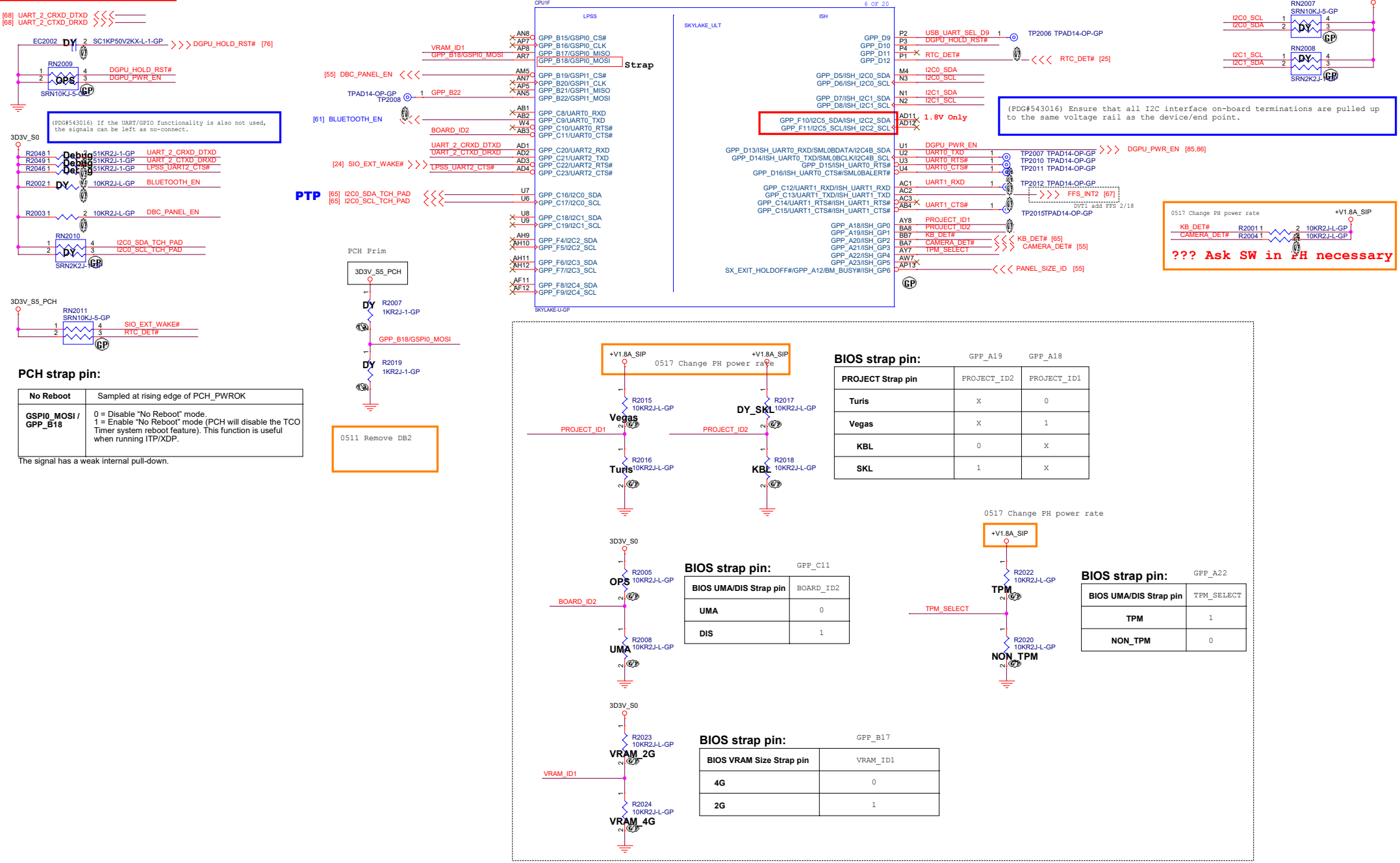
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU_(AUDIO/SDIO/SDXC)*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-U*	*A00*

Date: Wednesday, November 08, 2017 Sheet 19 of 105

Main Func = PCH



PCH strap pin:

No Reboot	Sampled at rising edge of PCH_PWROK
GSPI0_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.

BIOS strap pin:

GPP_A19 GPP_A18

PROJECT Strap pin	PROJECT_ID2	PROJECT_ID1
Turis	X	0
Vegas	X	1
KBL	0	X
SKL	1	X

BIOS strap pin:

GPP_C11

BIOS UMA/DIS Strap pin	BOARD_ID2
UMA	0
DIS	1

BIOS strap pin:

GPP_A22

BIOS UMA/DIS Strap pin	TPM_SELECT
TPM	1
NON_TPM	0

BIOS strap pin:

GPP_B17

BIOS VRAM Size Strap pin	VRAM_ID1
4G	0
2G	1

<Core Design>

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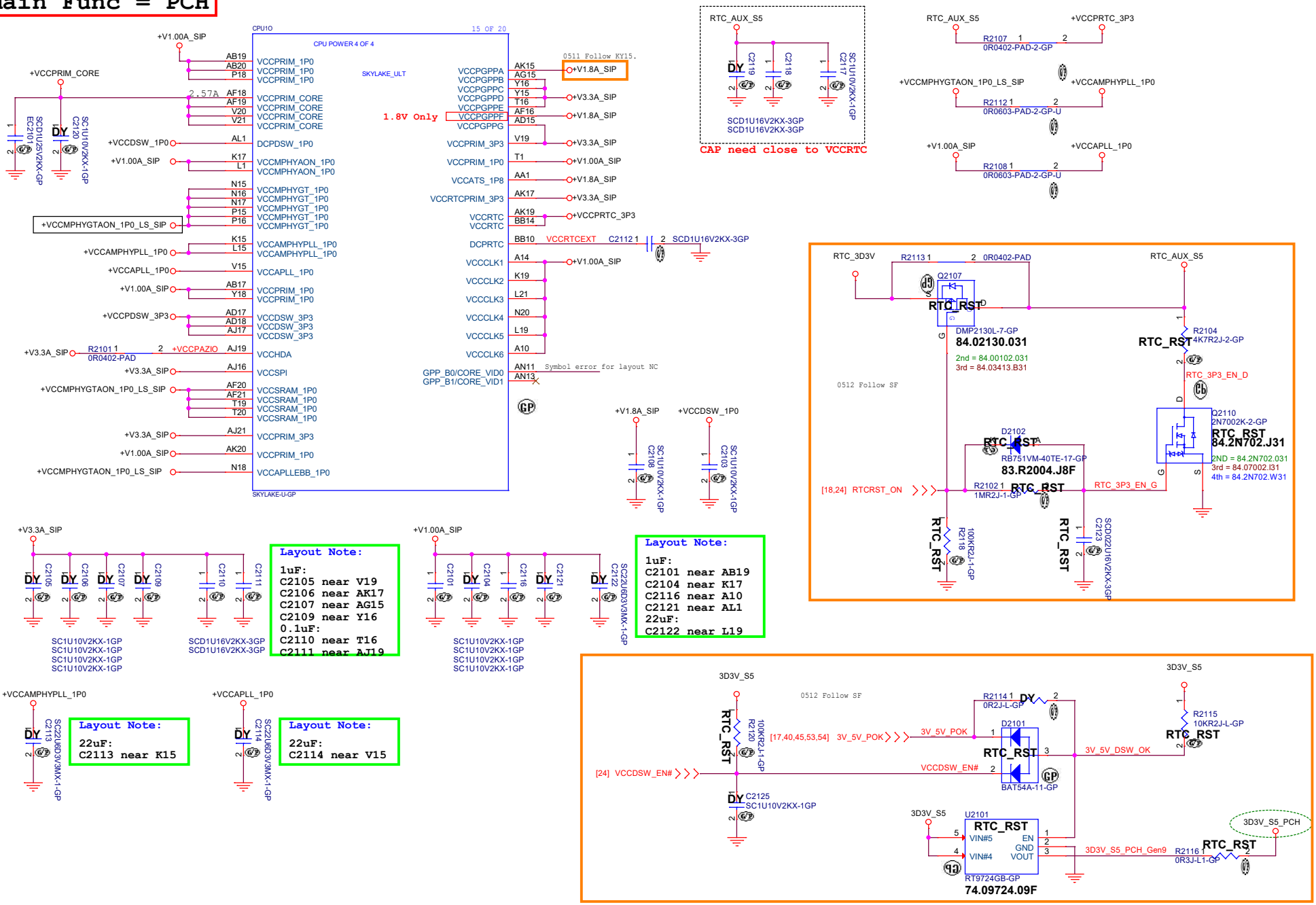
Title: CPU_(LPSS/ISH)

Size: Custom | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 20 of 105

Main Func = PCH



Layout Note:

1uF:
C2105 near V19
C2106 near AK17
C2107 near AG15
C2109 near Y16
0.1uF:
C2110 near T16
C2111 near AJ19

Layout Note:

1uF:
C2101 near AB19
C2104 near K17
C2116 near A10
C2121 near AL1
22uF:
C2122 near L19

Layout Note:

22uF:
C2113 near K15

Layout Note:

22uF:
C2114 near V15

<Core Design>

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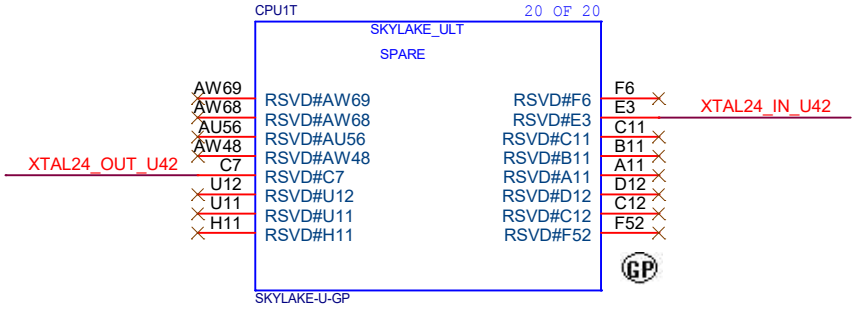
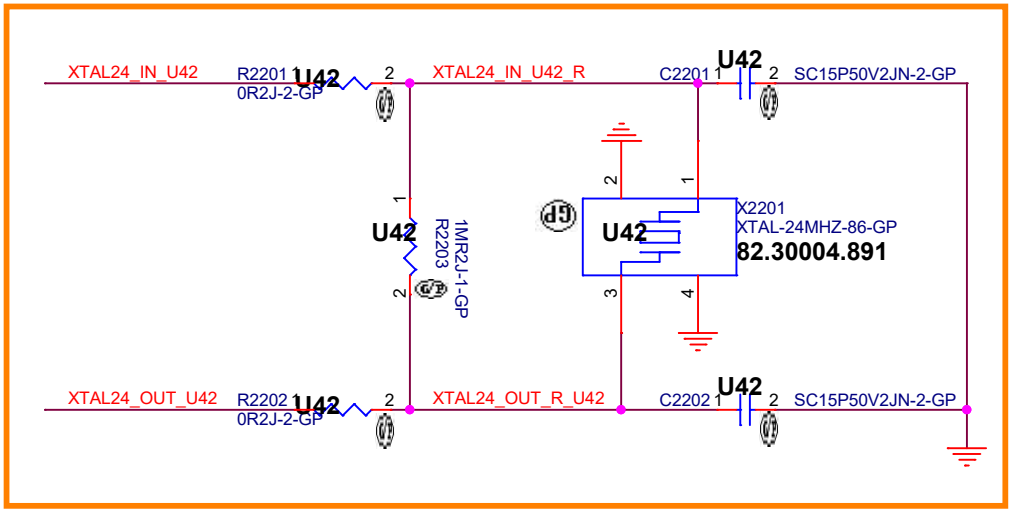
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU_(POWER1)	
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 21 of 105	





<Core Design>

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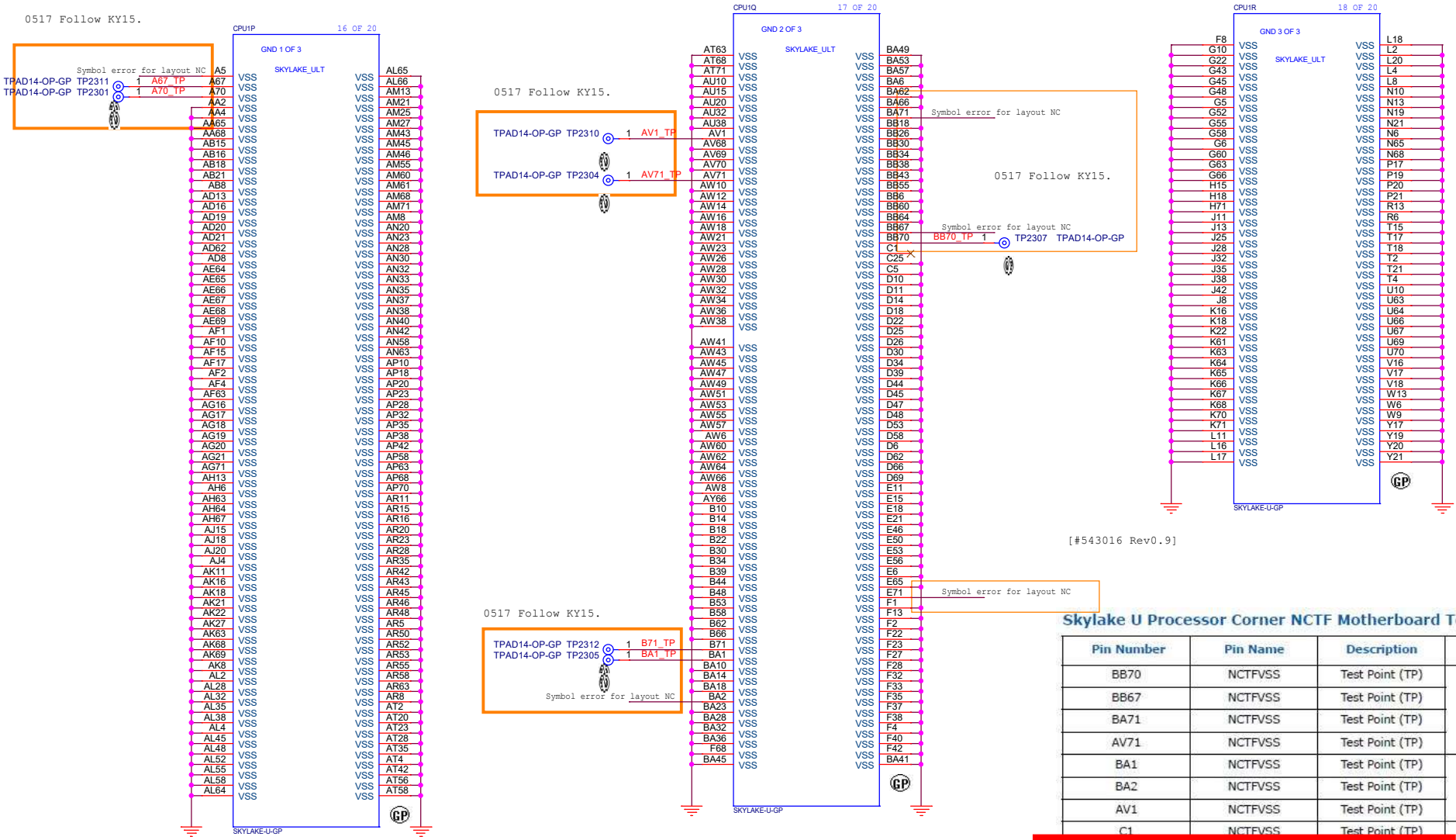
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU_(RSVD)***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

Date: Wednesday, November 08, 2017 Sheet 22 of 105

Main Func = PCH



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	
BA1	NCTFVSS	Test Point (TP)	Corner BB1
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	
C1	NCTFVSS	Test Point (TP)	Corner A1
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

Size: A3 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 23 of 105

Main Func = KBC

Layout Note:
Need very close to EC

ESPI

EC_GPIO47 High Active

Power Switch Logic(PSL)

??? Check function with Kevin

EC LCD test

Layout Note:
Connect GND and AGND planes via either OR resistor or connect directly.

Layout Note:
Need very close to EC

Q2412 and Q2413 merge
84.2N702.A3F
2nd = 84.2N702.E3F
3rd = 75.00601.07C

84.2N702.J31
2ND = 84.2N702.031
3rd = 84.07002.I31

83.R2004.G8F

082.30003.0221

071.01416.000G

20.K0691.006

#	Board_ID(GPIO155)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	X00	100.0K	10.0K	3
2	X01	100.0K	17.8K	2.801
3	X02	100.0K	27.0K	2.598
4	X03(reserve)	100.0K	37.4K	2.402
5	A00	100.0K	49.9K	2.201
6	A01	100.0K	64.9K	2.001
7	A02	100.0K	82.5K	1.808
8	A03	100.0K	107K	1.594
9	Reserve	100.0K	154K	1.299
10	Reserve	100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

#	MODEL_ID(GPIO153)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
1	Vegas KBL-R UMA	100.0K	10.0K	3
2		100.0K	17.8K	2.801
3	Turis KBL-R UMA	100.0K	27.0K	2.598
4		100.0K	37.4K	2.402
5		100.0K	49.9K	2.201
6		100.0K	64.9K	2.001
7	Vegas KBL-R DIS	100.0K	82.5K	1.808
8		100.0K	107K	1.594
9	Turis KBL-R DIS	100.0K	154K	1.299
10		100.0K	200K	1.1
11	Reserve	100.0K	TBD	0.9
12	Reserve	100.0K	TBD	0.7
13	Reserve	100.0K	TBD	0.5
14	Reserve	100.0K	TBD	0.3

<Core Design>

Wistron Corporation
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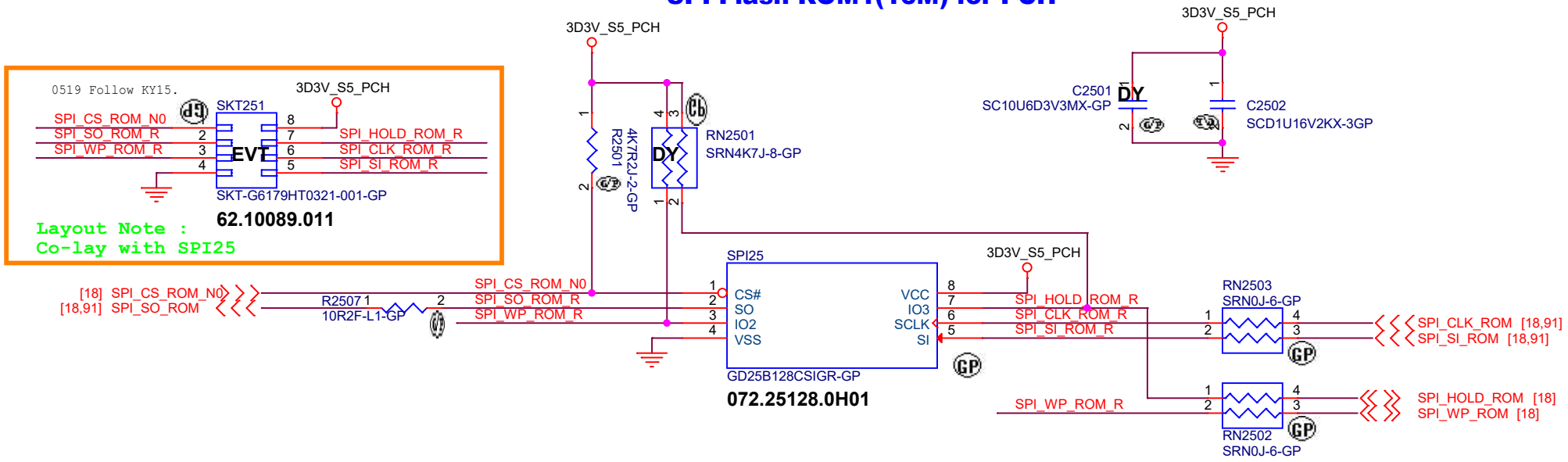
Taipei Hsien 221, Taiwan, R.O.C.

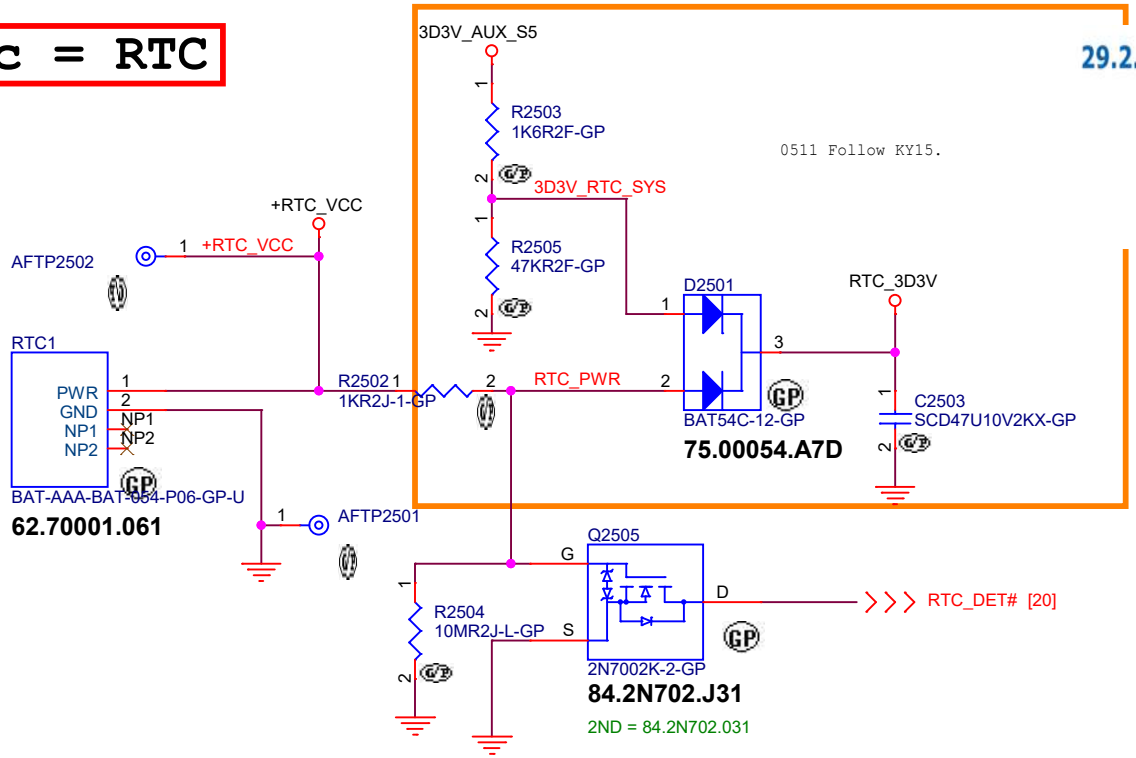
Title: KBC SMSC 1416
Size: Custom
Document Number: Turis/Vegas KBL-R
Rev: A00
Date: Friday, November 10, 2017
Sheet 24 of 105

Main Func = SPI Flash

SPI Flash ROM1(16M) for PCH



Main Func = RTC



29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.

<Core Design>

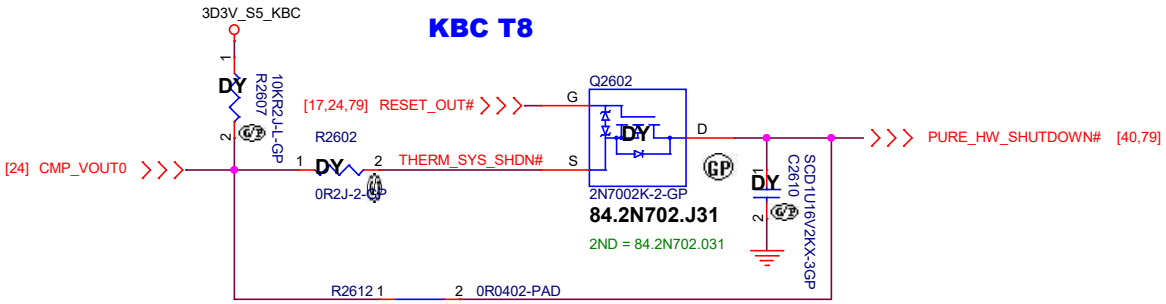
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

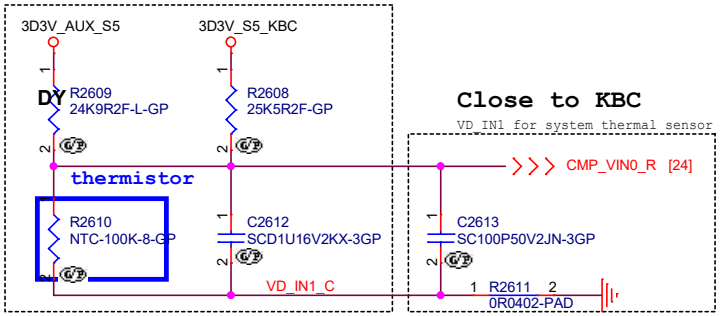
Title: Flash/RTC

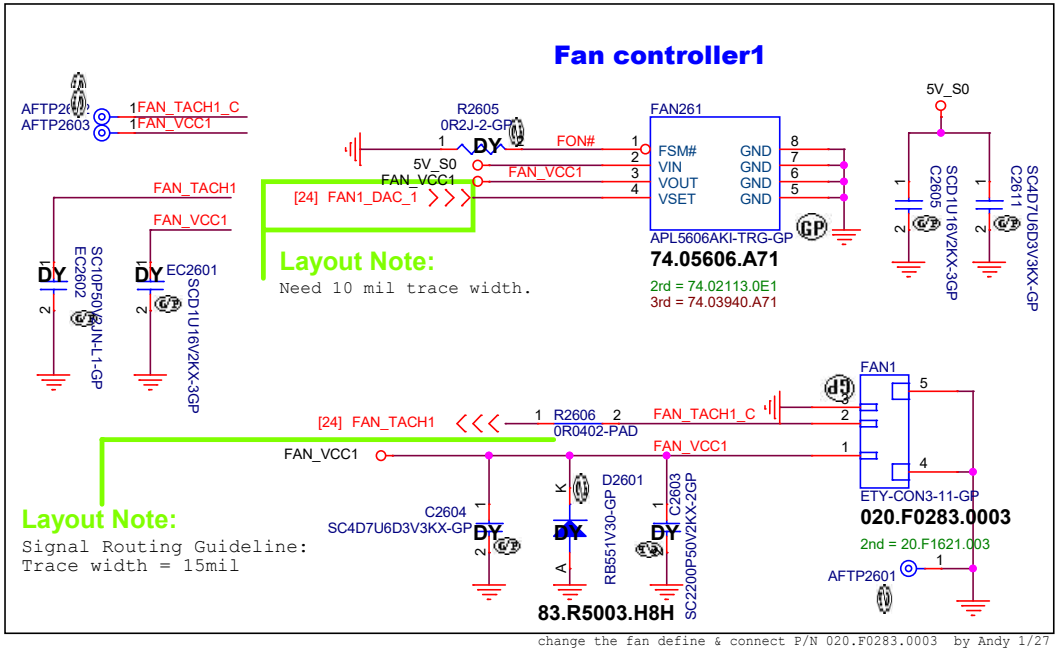
Size	Document Number	Rev
A4	Turis/Vegas KBL-R	A00

Date: Wednesday, November 08, 2017 Sheet 25 of 105

Main Func = Thermal Sensor







<Core Design>

Wistron Corporation
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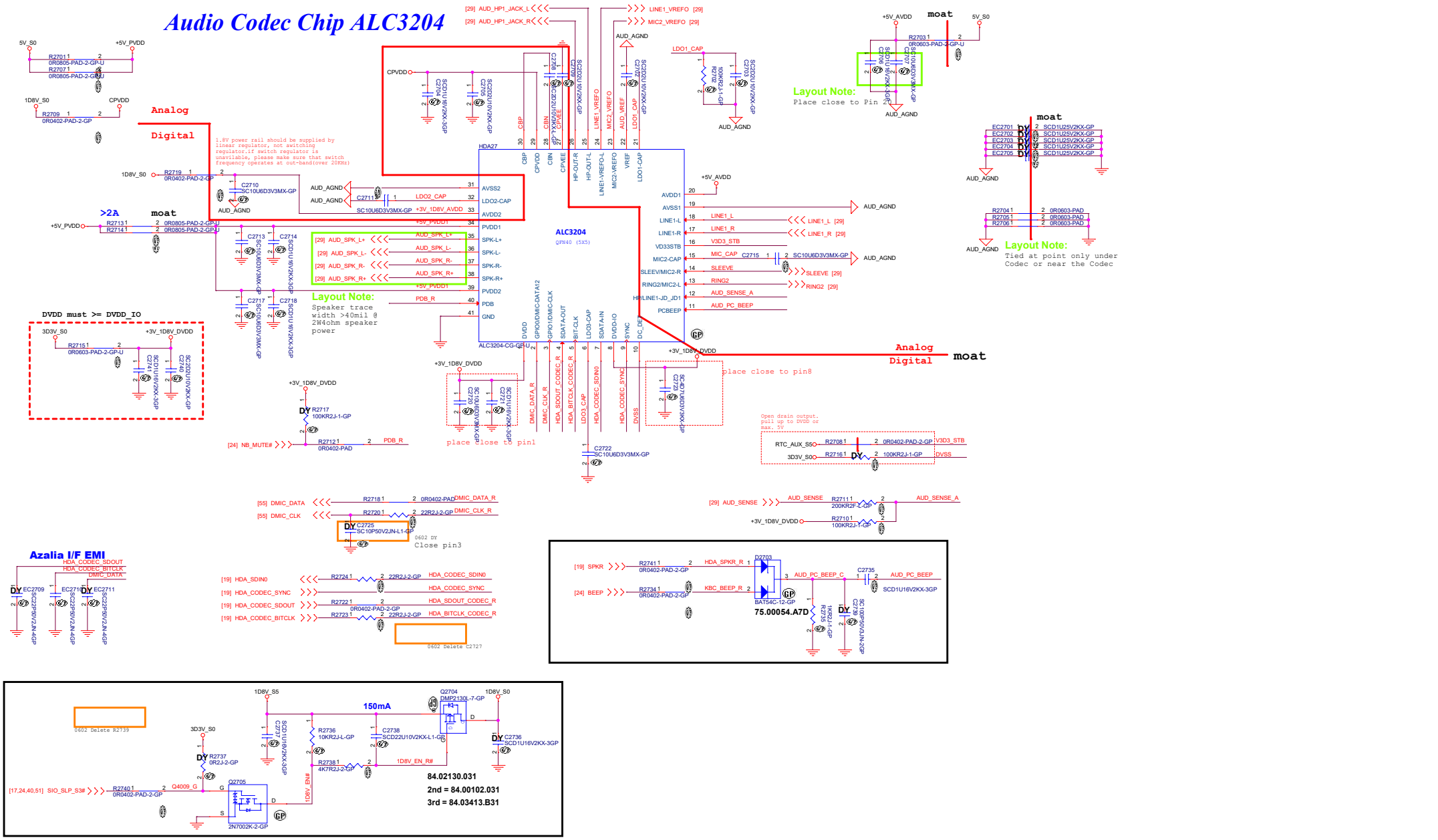
Taipei Hsien 221, Taiwan, R.O.C.

Title	THERMAL NCT7718W/Fan	
Size: Custom	Document Number: Turis/Vegas KBL-R	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 26 of 105	

Main Func = Audio

Audio Codec Chip ALC3204



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3204

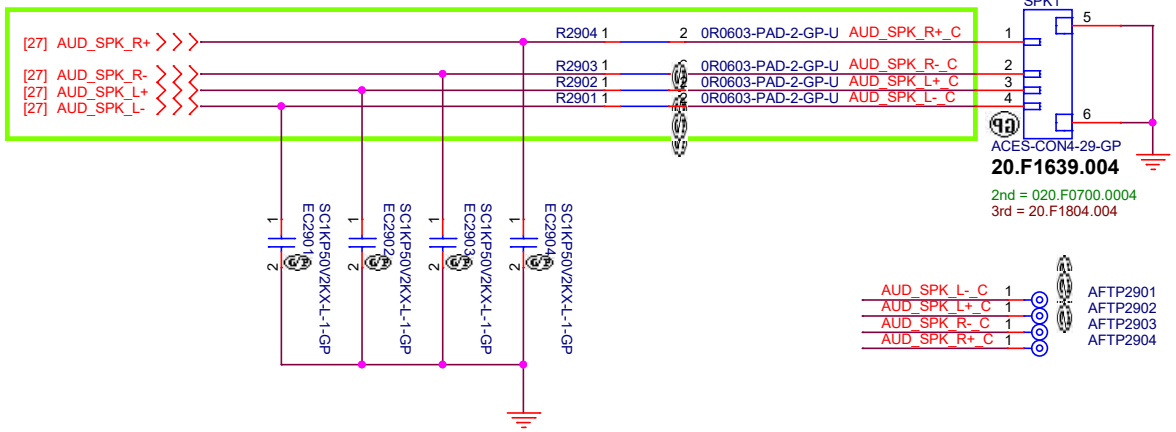
Size: A2 | Document Number: Turis/Vegas KBL-R | Rev: X00

Date: Wednesday, November 08, 2017 | Sheet 27 of 105

Main Func = Audio

Layout Note:

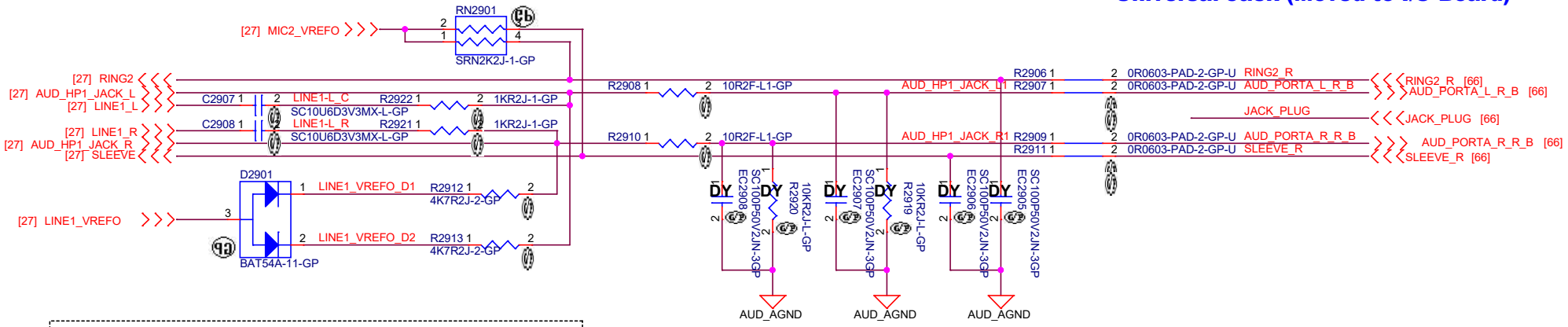
Speaker trace width >40mil @ 2W4ohm speaker power



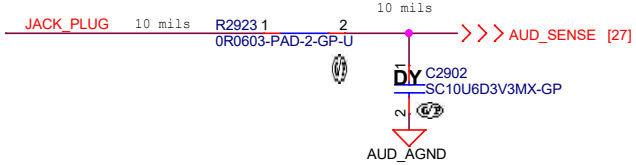
Speaker

CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Universal Jack (Moved to I/O Board)



Delay circuit
(JACK_PLUG_DET: on IO Board)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

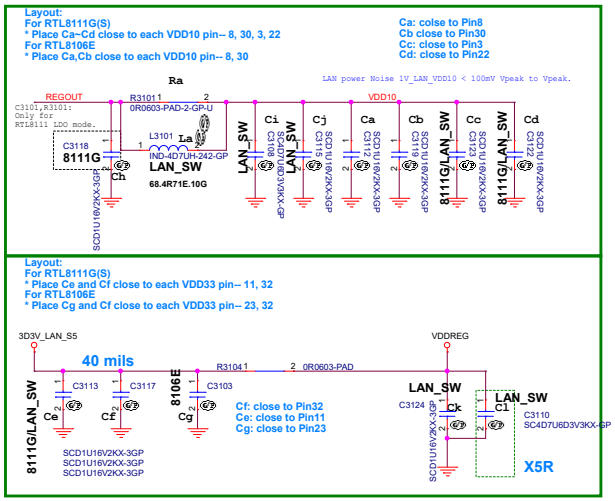
Title: *Audio IO*

Size: Custom | Document Number: Turis/Vegas KBL-R | Rev: A00

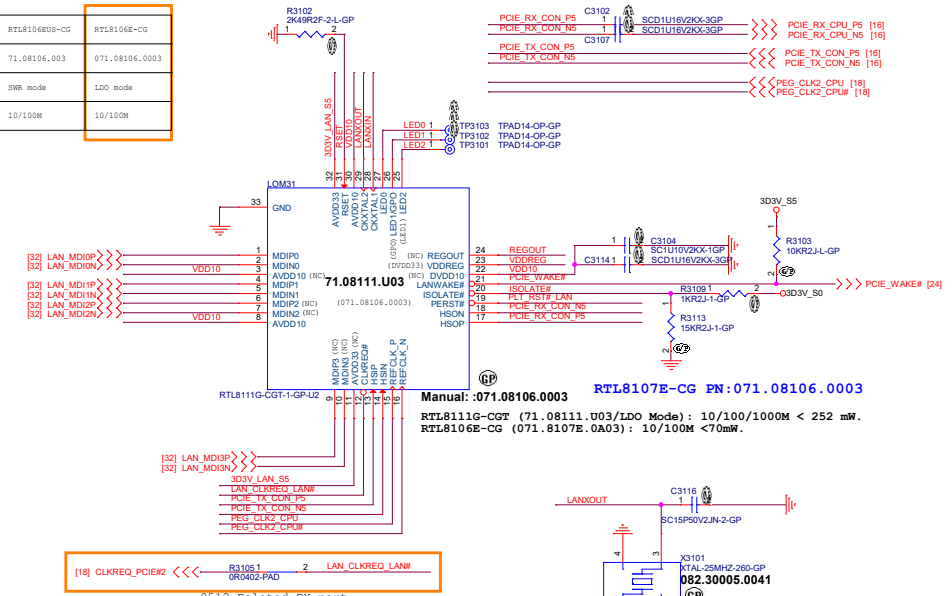
Date: Wednesday, November 08, 2017 | Sheet 29 of 105

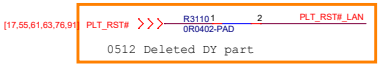
Main Func = LAN

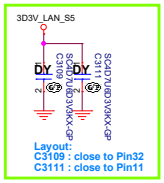
LAN CHIP (10/100/1000M & 10/100M co-lay)

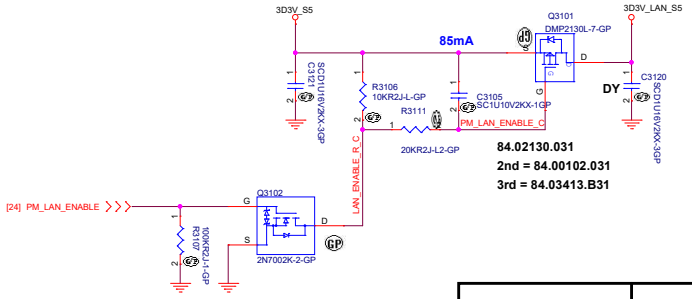


RTL8111GUS-CG	RTL8111G-CGT	RTL8106EUS-CG	RTL8106E-CG
71.08111.W03	71.08111.U03	71.08106.003	071.08106.0003
SWR mode	LDO mode	SWR mode	LDO mode
10/100/1000M	10/100/1000M	10/100M	10/100M









	BOM Option	1.0V Source	Ra	Ch	Cc	Cd	Ce	La	Ci	Cj	Ck	Cl	Cg
RTL8111G-CGT (71.08111.U03)	8111G	LDO	O	O	O	O	O	X	X	X	X	X	X
RTL8111GUS-CG (71.08111.W03) / RTL8106EUS-CG (71.08106.003)	LAN_SW	SWR	X	X	O	O	O	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	8106E	LDO	X	X	X	X	X	X	X	X	X	X	O

<Core Design>

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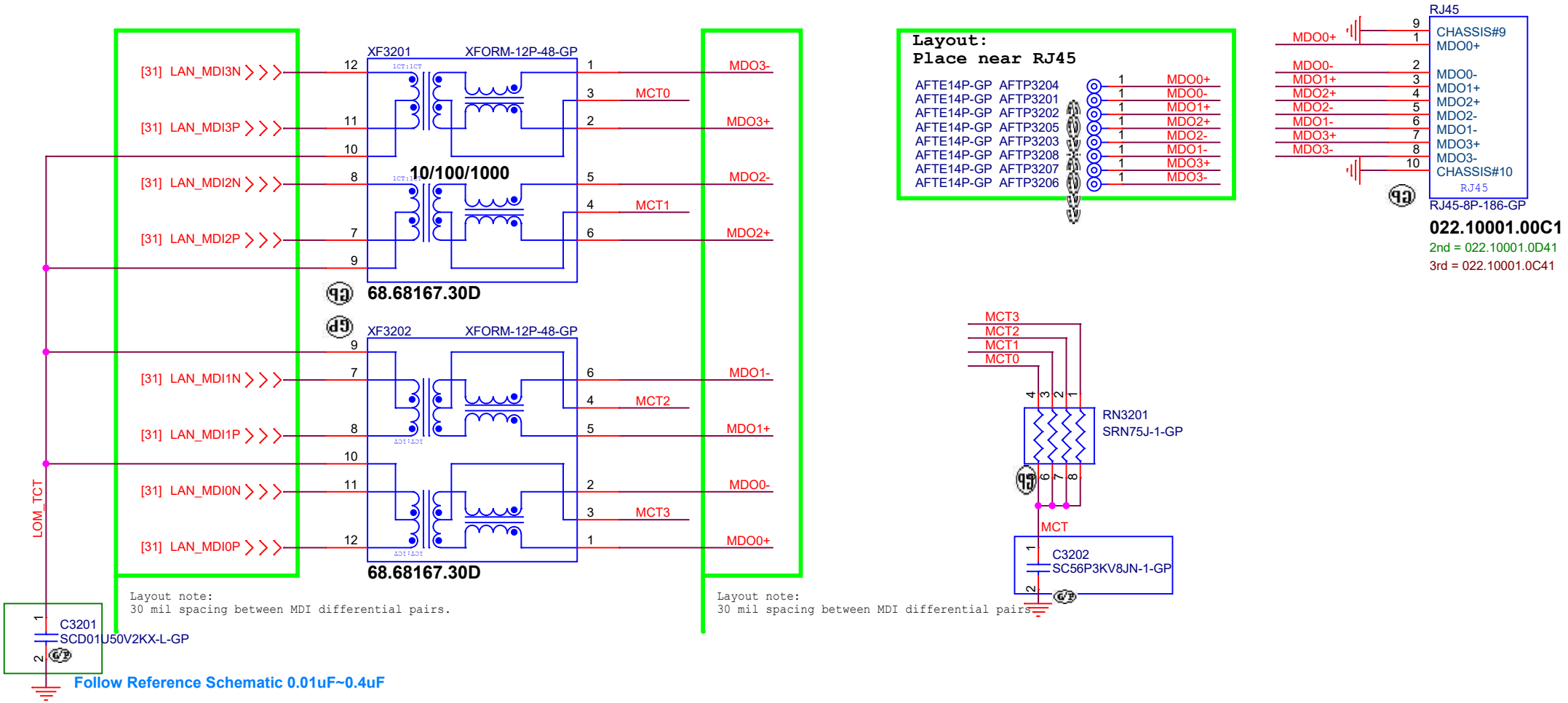
Title: LAN RTL8106

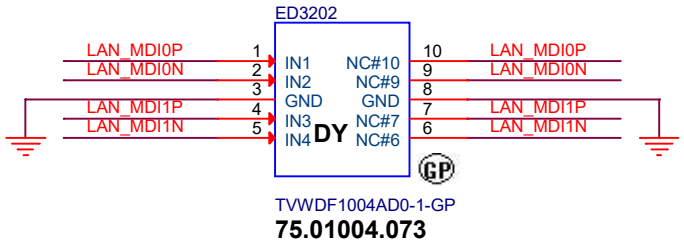
Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

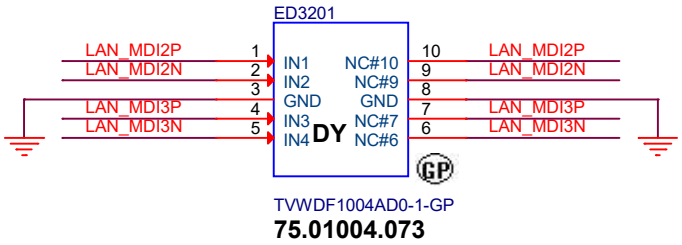
Date: Wednesday, November 08, 2017 | Sheet 31 of 105

Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)







<Core Design>

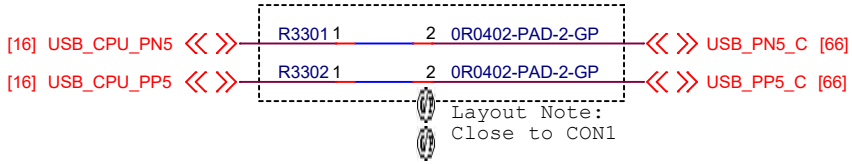
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **XFOM&RJ45**

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Wednesday, November 08, 2017 Sheet 32 of 105

Main Func = Card Reader



<Core Design>

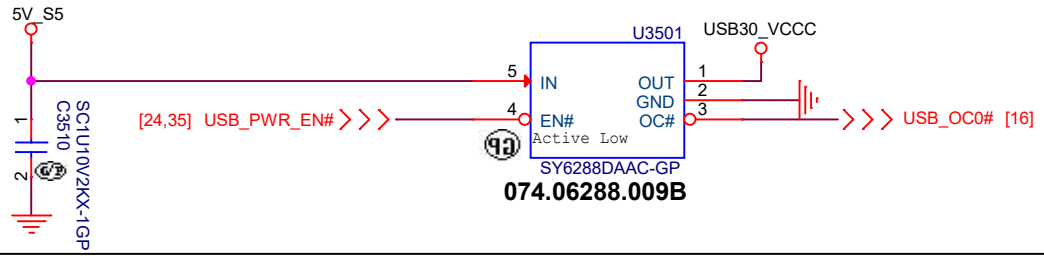
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5170

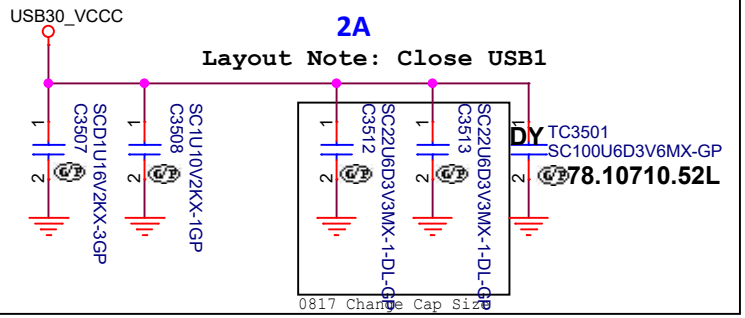
Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Wednesday, November 08, 2017 Sheet 33 of 105

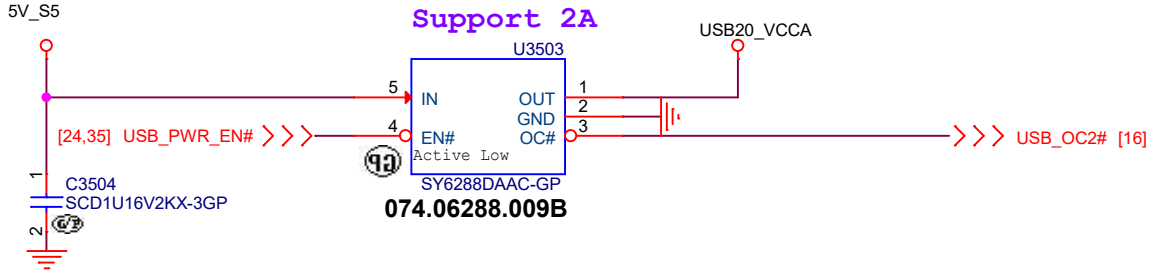
Main Func = USB3.0 Port1



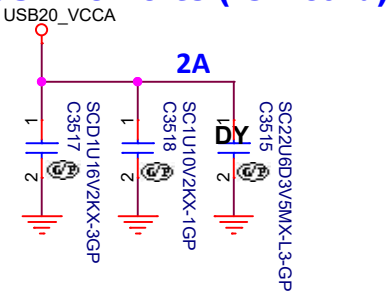
USB3.0 Port1



Main Func = USB2.0 Port3



USB2.0 Port3 (IO Board)

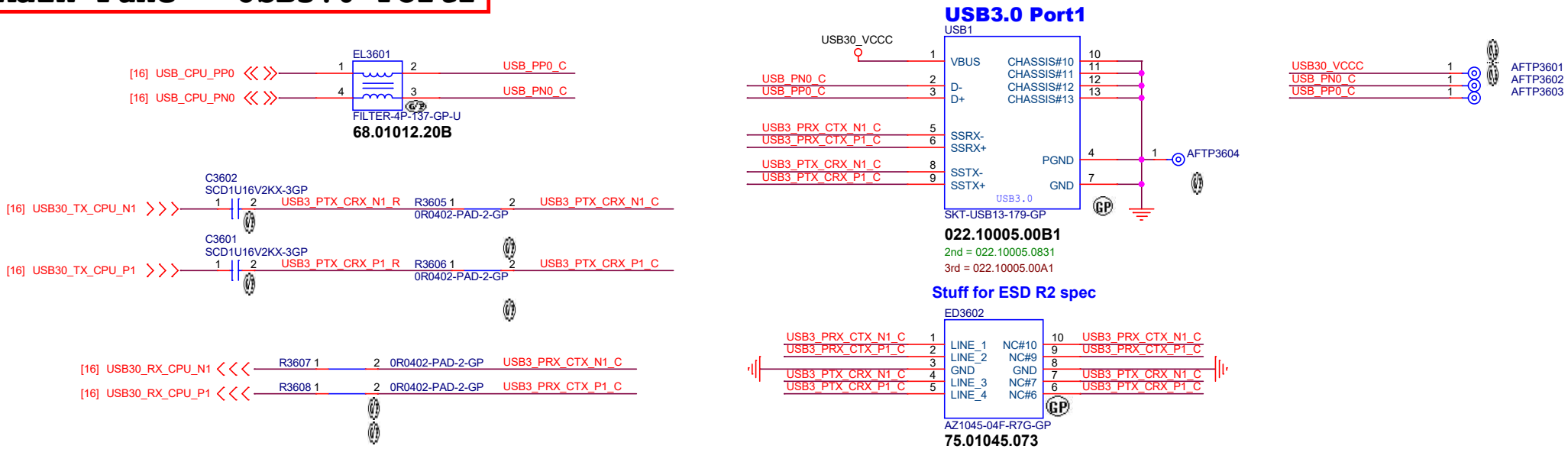


<Core Design>

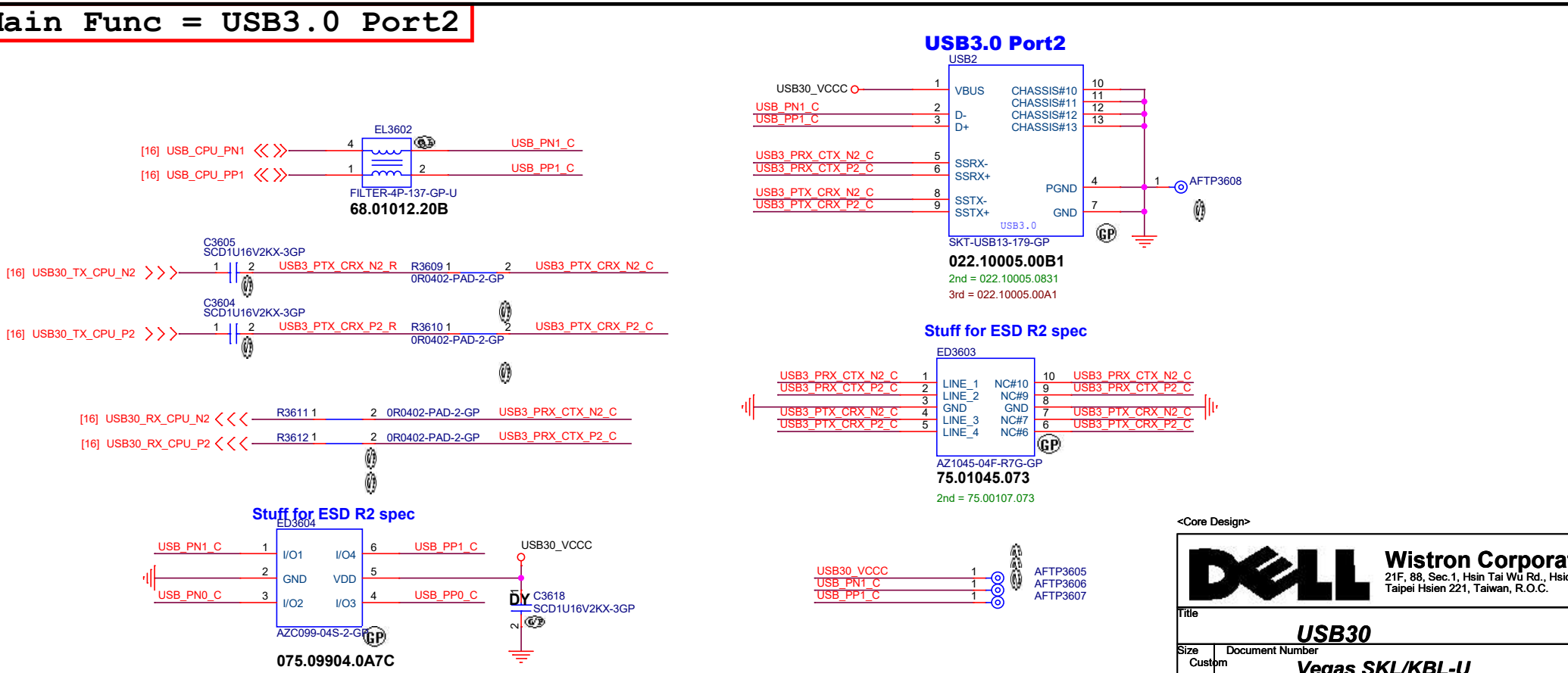
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB switch*		
Size	Document Number: *Turis/Vegas KBL-R*	Rev: *A00*
Date: Wednesday, November 08, 2017	Sheet 35 of 105	

Main Func = USB3.0 Port1



Main Func = USB3.0 Port2



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

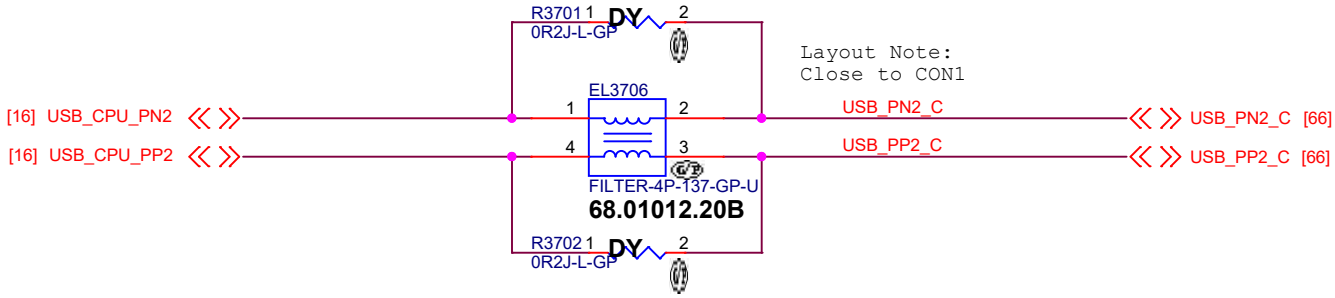
Title: USB30

Size	Document Number	Rev
Custom	Vegas SKL/KBL-U	A00

Date: Wednesday, November 08, 2017 Sheet 36 of 105

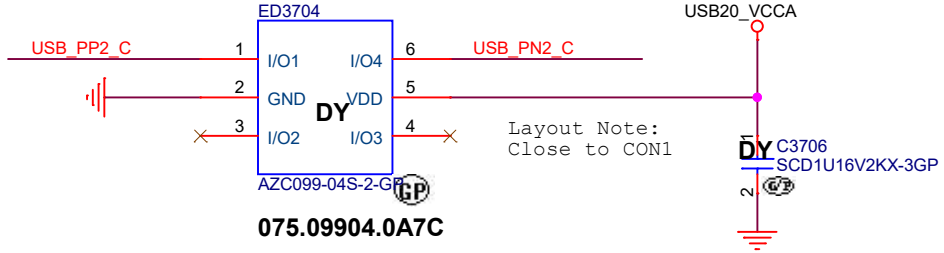
Main Func = USB2.0 Port3

USB port 3 (USB2.0 only) CMC



USB ESD Diode

Stuff for ESD R2 spec



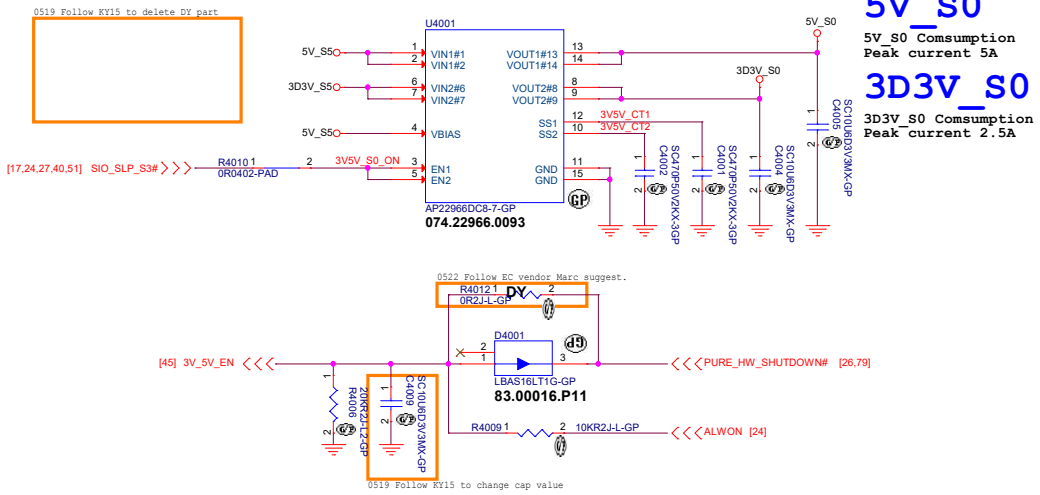
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *USB20*		
Size: A4	Document Number: *Turis/Vegas KBL-R*	Rev: *A00*
Date: Wednesday, November 08, 2017	Sheet 37 of 105	

Main Func = Power Plane & Sequence

ROSA Run Power



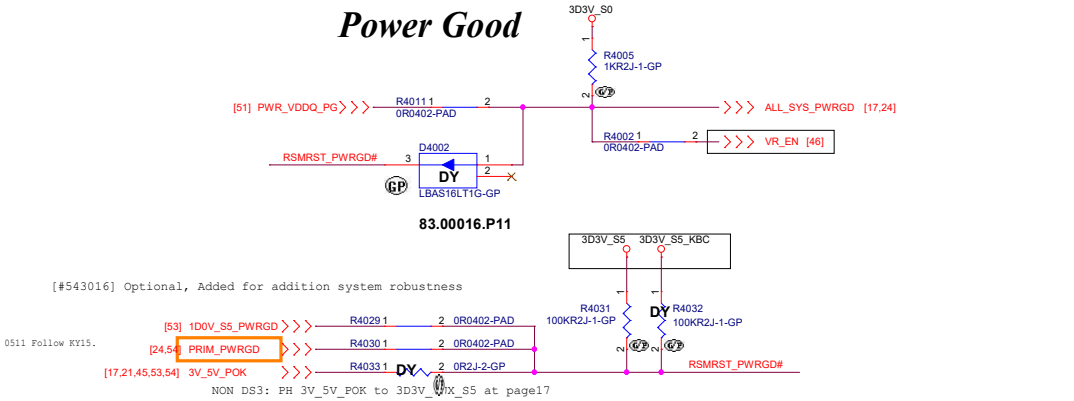
5V_S0

5V_S0 Comsumption
Peak current 5A

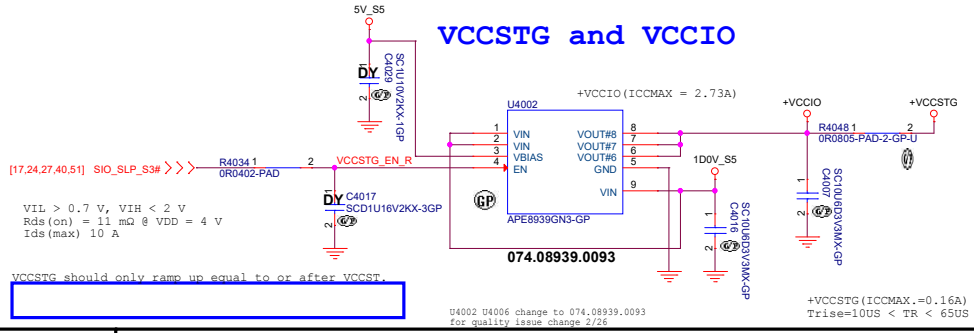
3D3V_S0

3D3V_S0 Comsumption
Peak current 2.5A

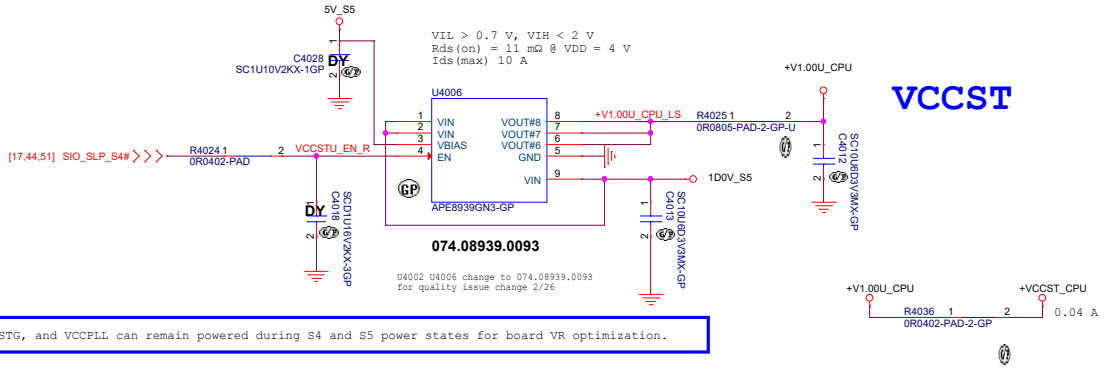
Power Good



VCCSTG and VCCIO



MANAGEMENT RAIL POWER GENERATION



VCCST

VCCST, VCCSTG, and VCCPLL can remain powered during S4 and S5 power states for board VR optimization.

EOPIO and EDRAM

20170428

V1.8S

20170428

<Core Design>

Wistron Corporation
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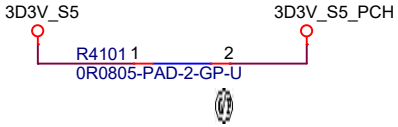
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
Custom	Vegas SKL/KBL-U	A00

Date: Wednesday, November 08, 2017 Sheet 40 of 105

Main Func = Power & Sequence



<Core Design>

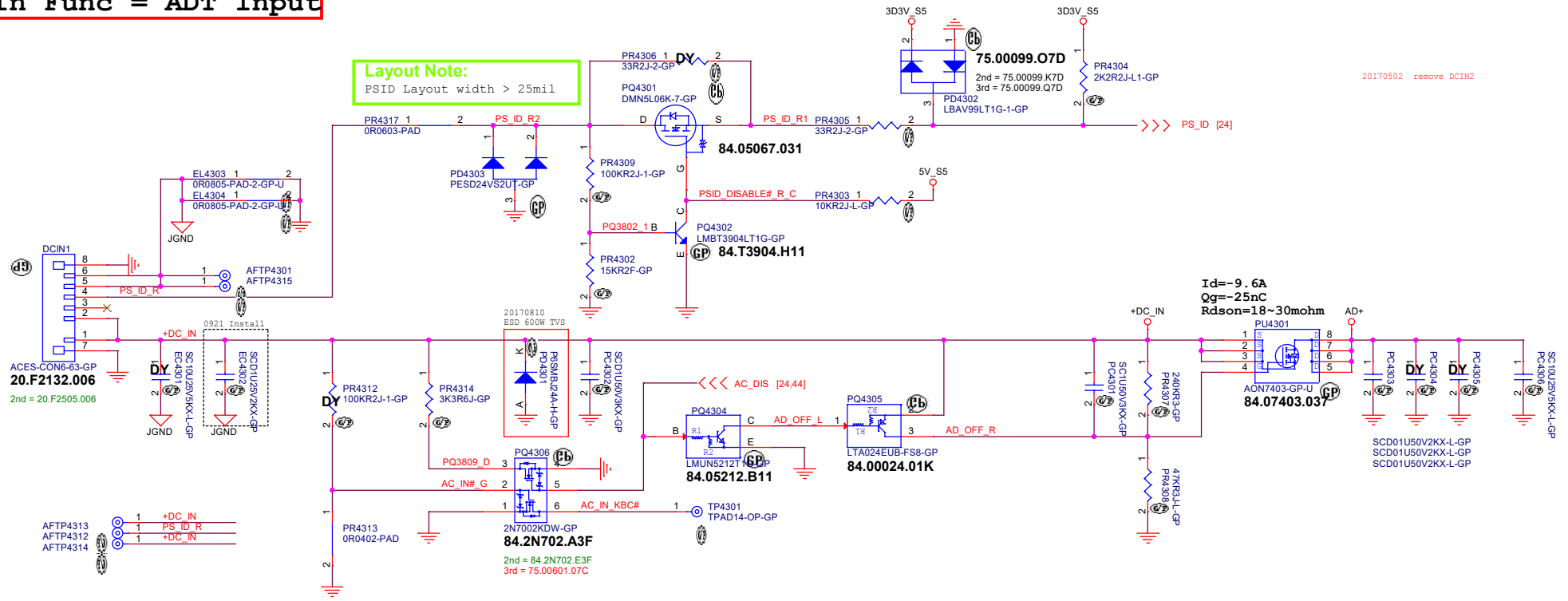
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Connected_Standby(1/2)+DS3***

Size	Document Number	Rev
A4	***Vegas SKL/KBL-U***	***A00***

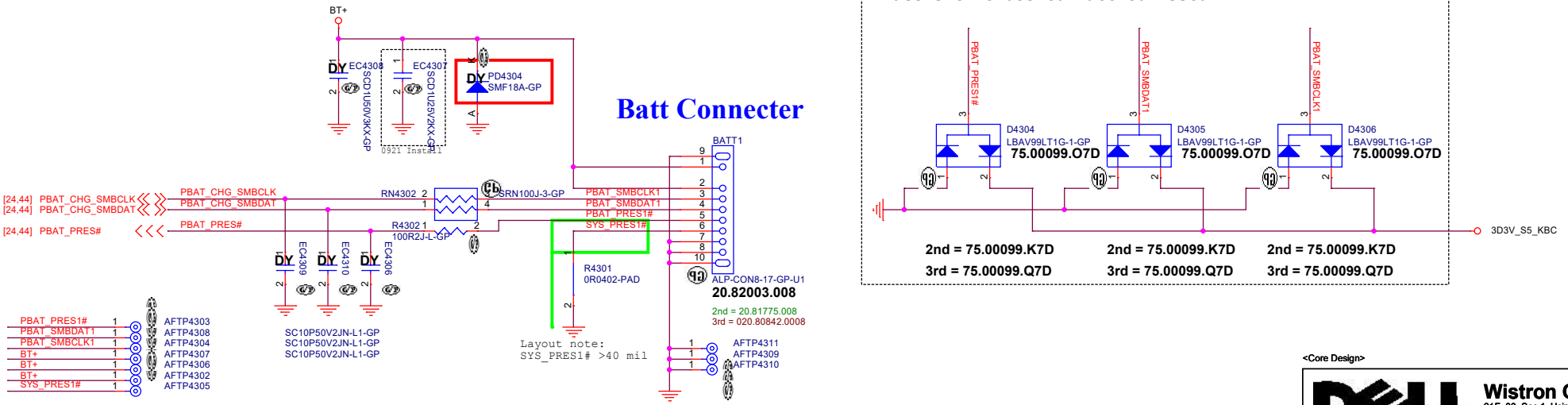
Date: Wednesday, November 08, 2017 Sheet 41 of 105

Main Func = ADT Input



Main Func = M-BAT Input

20170502 remove BATT2

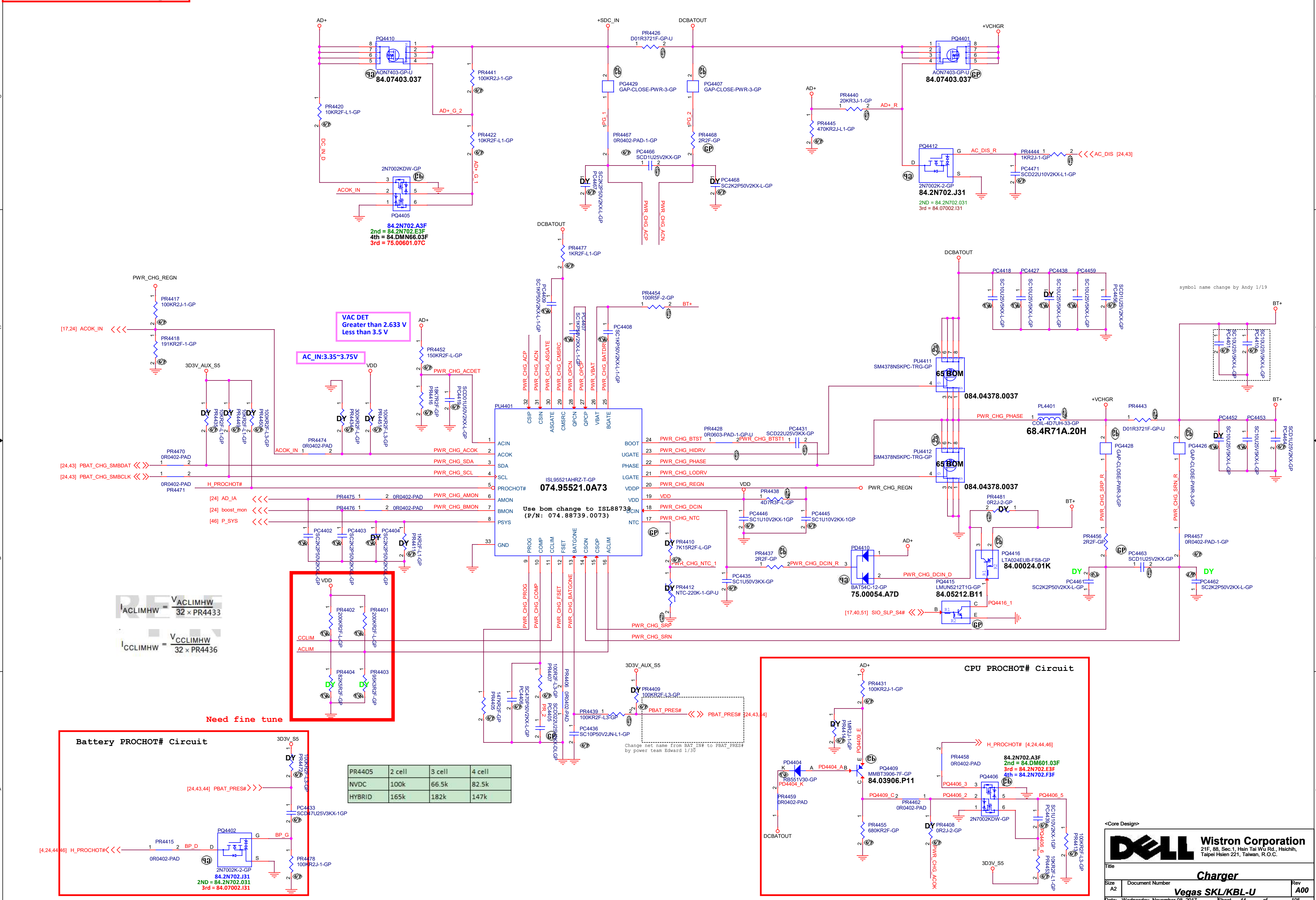


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN		
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 43 of 105	

Main Func = Charger



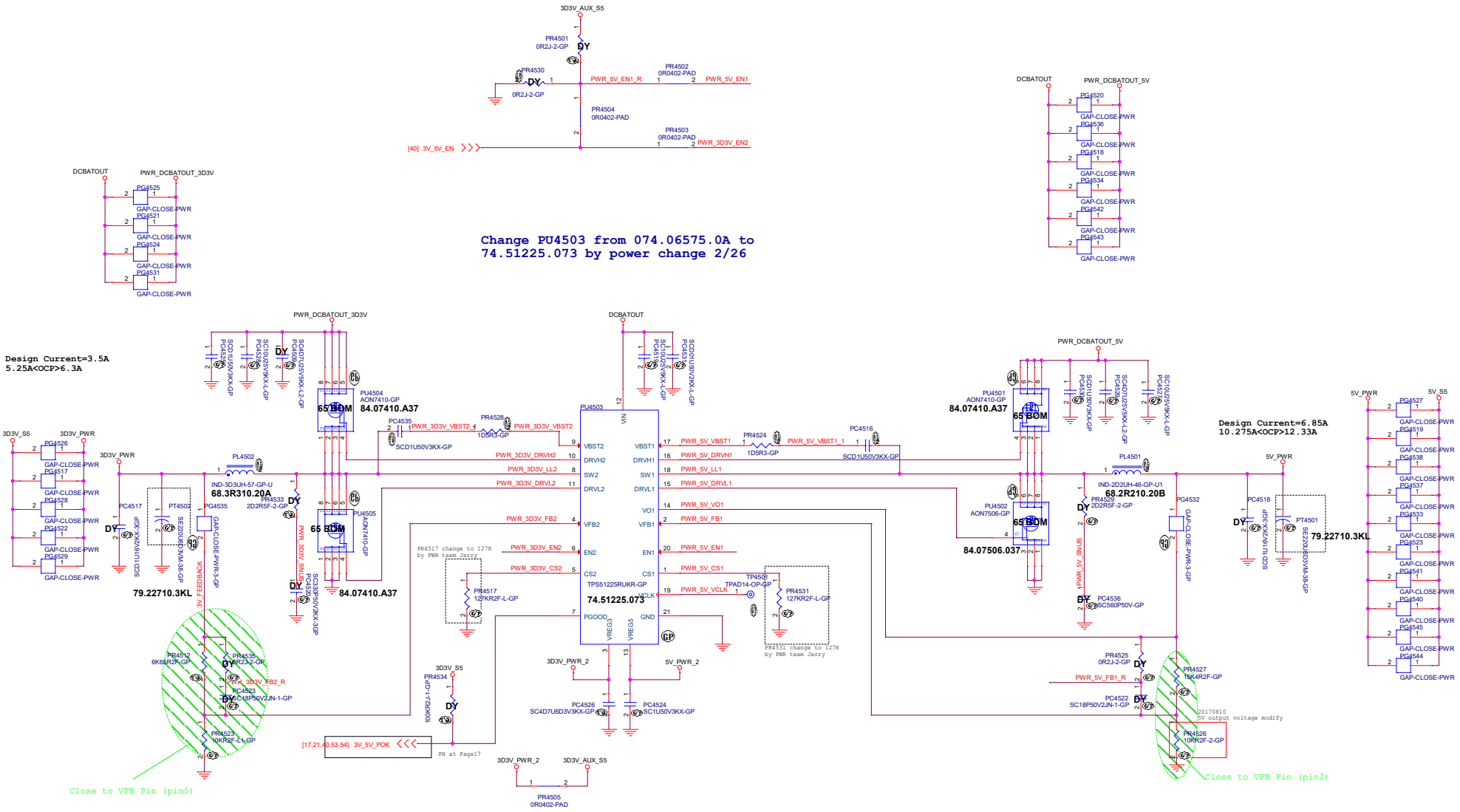
PR4405	2 cell	3 cell	4 cell
NVDC	100k	66.5k	82.5k
HYBRID	165k	182k	147k

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Charger		
Size: A2	Document Number: Vegas SKL/KBL-U		Rev: A00
Date: Wednesday, November 08, 2017	Sheet 44 of 105		

Main Func = 3D3V_5V



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P capCHIP CAP EL 220U 6.3V M6.3*4.4 /Chemi-con/ 18mOhm / 79.22710.3KL
H/S:SIS412 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC-3D3V&5V

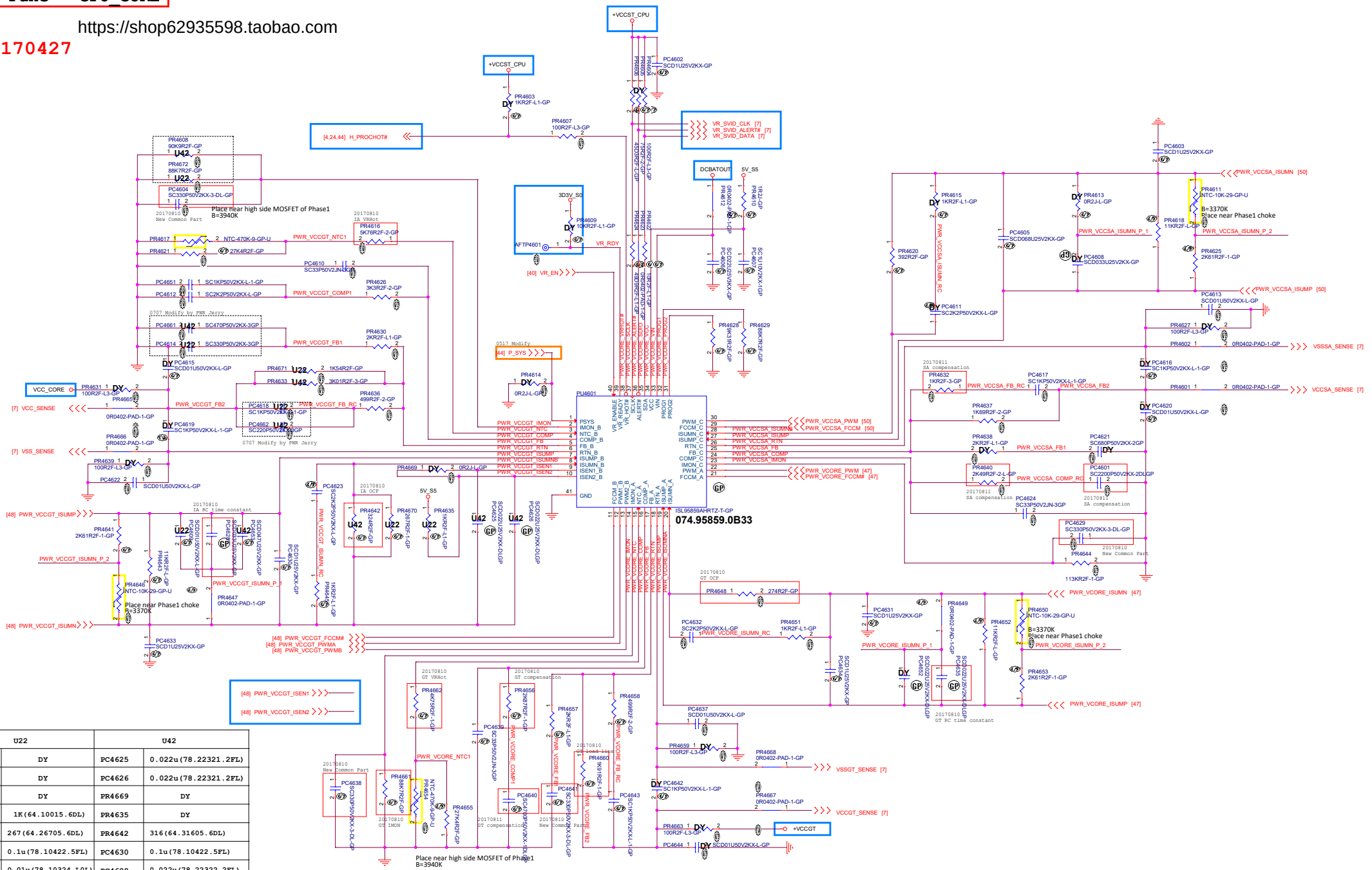
Size	Document Number	Rev
A2	Vegas SKL/KBL-U	A00

Date: Wednesday, November 08, 2017 Sheet 45 of 105

Main Func = CPU_CORE

https://shop62935598.taobao.com

20170427



U22		U42	
PC4625	DY	PC4625	0.022u(78.22321.2FL)
PC4626	DY	PC4626	0.022u(78.22321.2FL)
PR4669	DY	PR4669	DY
PR4635	1K(64.10015.6DL)	PR4635	DY
PR4670	267(64.26705.6DL)	PR4642	316(64.31605.6DL)
PC4630	0.1u(78.10422.5FL)	PC4630	0.1u(78.10422.5FL)
PC4609	0.01u(78.10324.L0L)	PC4628	0.022u(78.22322.2FL)
PC4653	DY	PC4653	47n(78.47322.2FL)
PR4671	1.54K(64.15415.6DL)	PR4633	3.01K(64.30115.6DL)
PR4672	88.7K(64.88725.6DL)	PR4608	90.9K(64.90925.6DL)
PC4614	330p(78.33124.2FL)	PC4661	470p(78.47124.2FL)
PC4618	1000p(78.10224.2FL)	PC4662	220p(78.22124.2FL)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

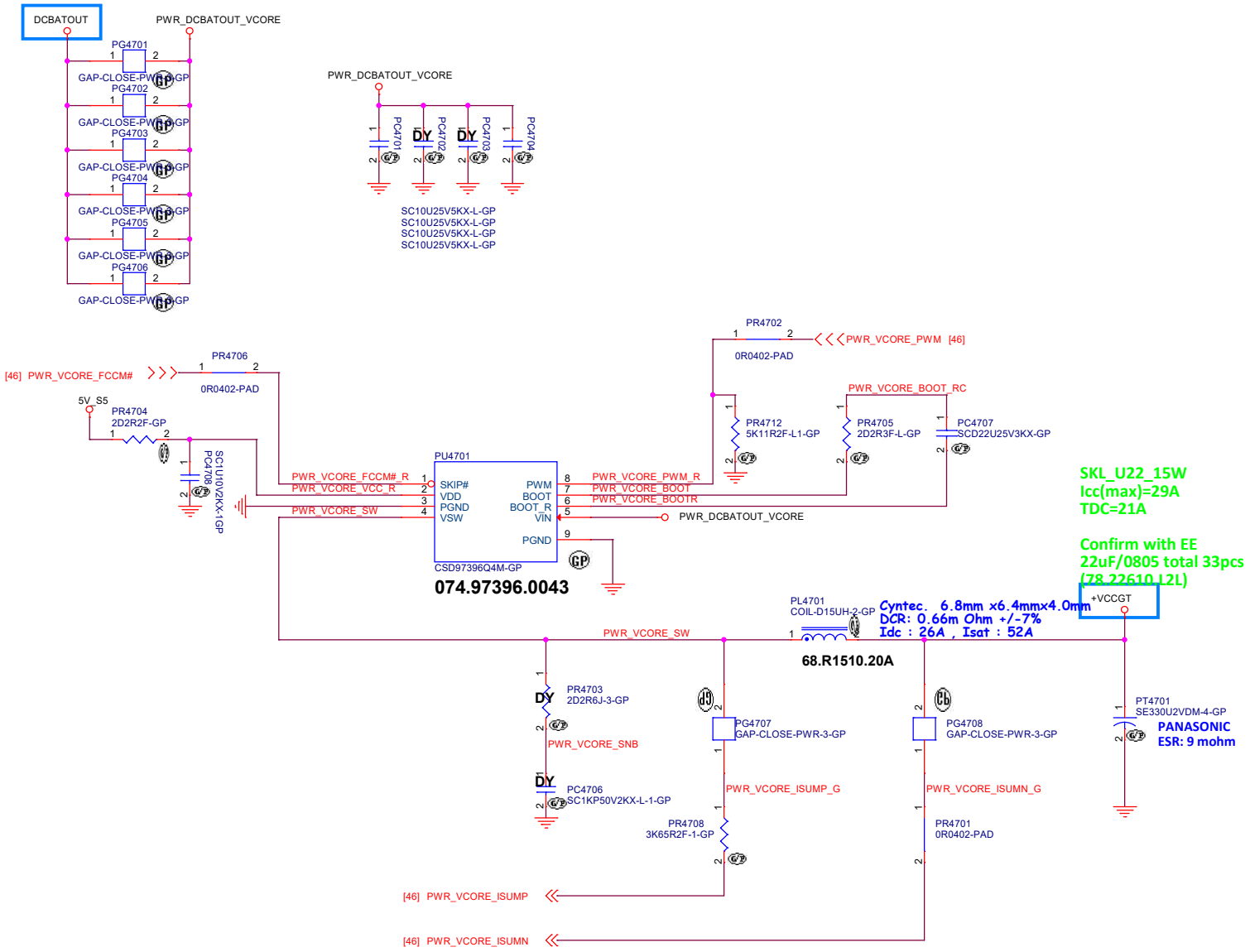
Title: NCP81208MN_CPU_VCORE(1/3)

Size: A2 | Document Number: Vegas SKL/KBL-R | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 46 of 105

Main Func = CPU_CORE

20170427



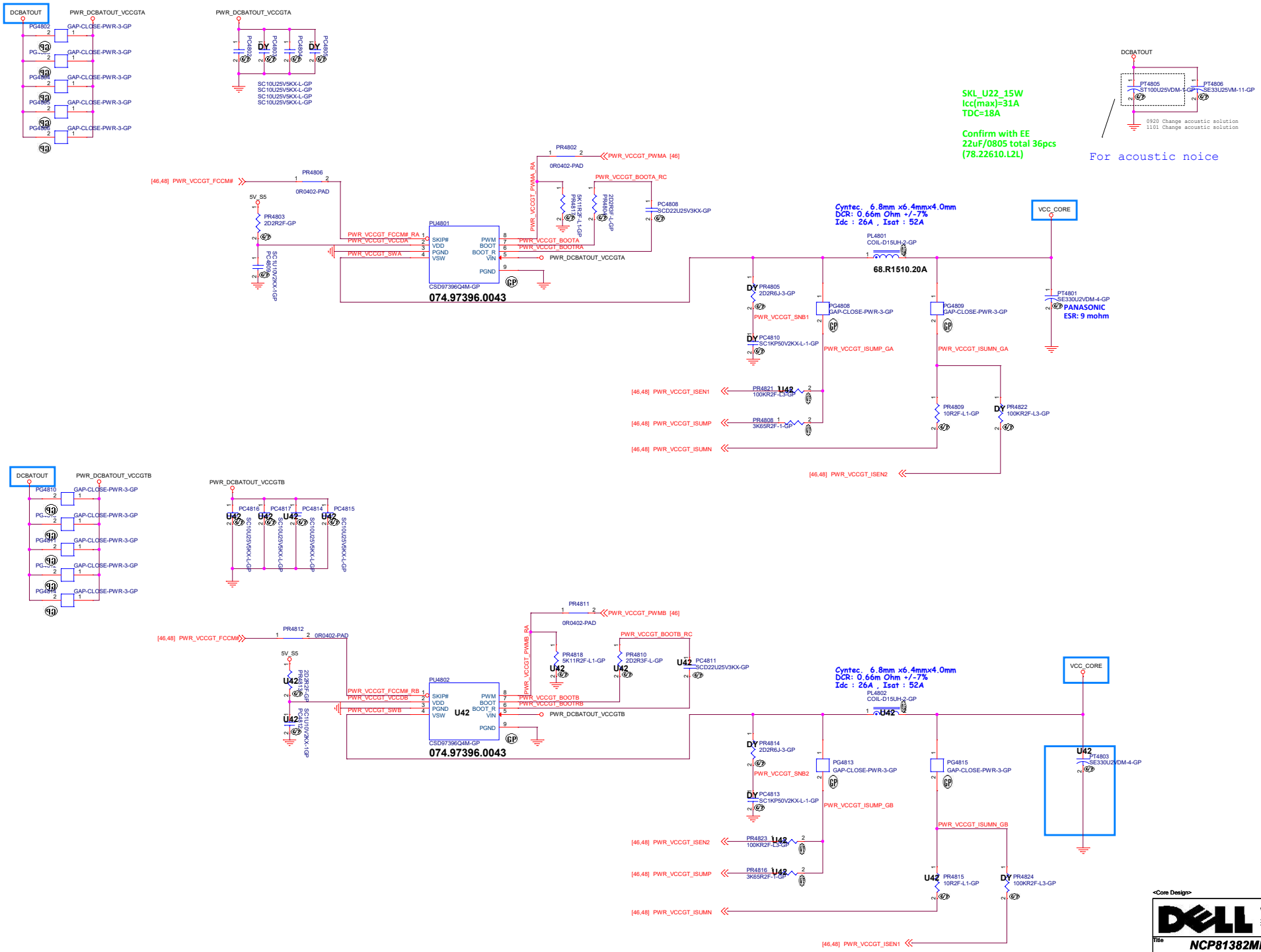
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81382MN_CPU_VCORE(2/3)	
Size: A3	Document Number: Vegas SKL/KBL-R	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 47 of 105	

Main Func = CPU_CORE

20170427



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

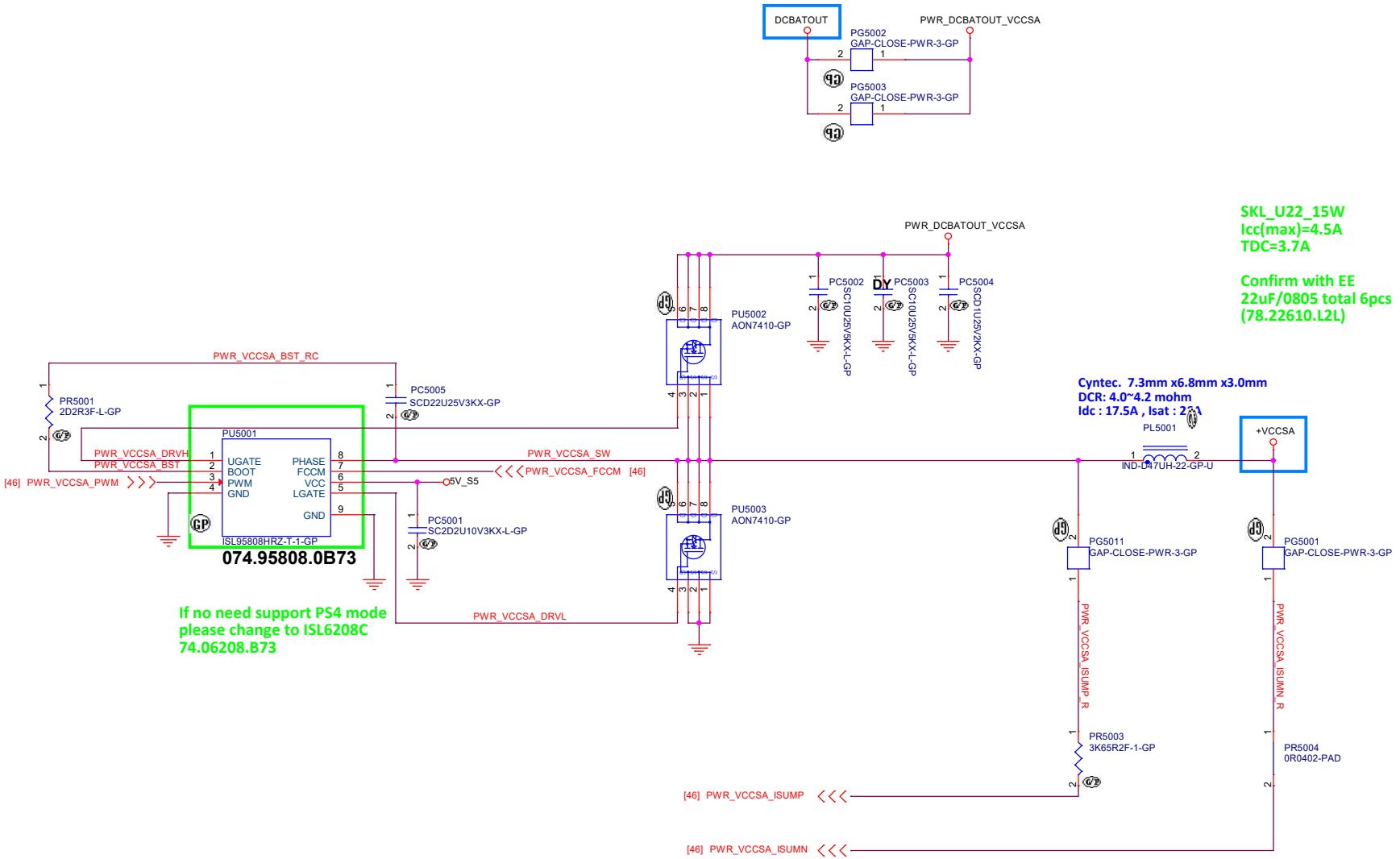
Title: NCP81382MN_CPU_VCCGT(3/3)

Size: A2 | Document Number: Vegas SKL/KBL-R | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 48 of 105

Main Func = CPU_CORE

20170427

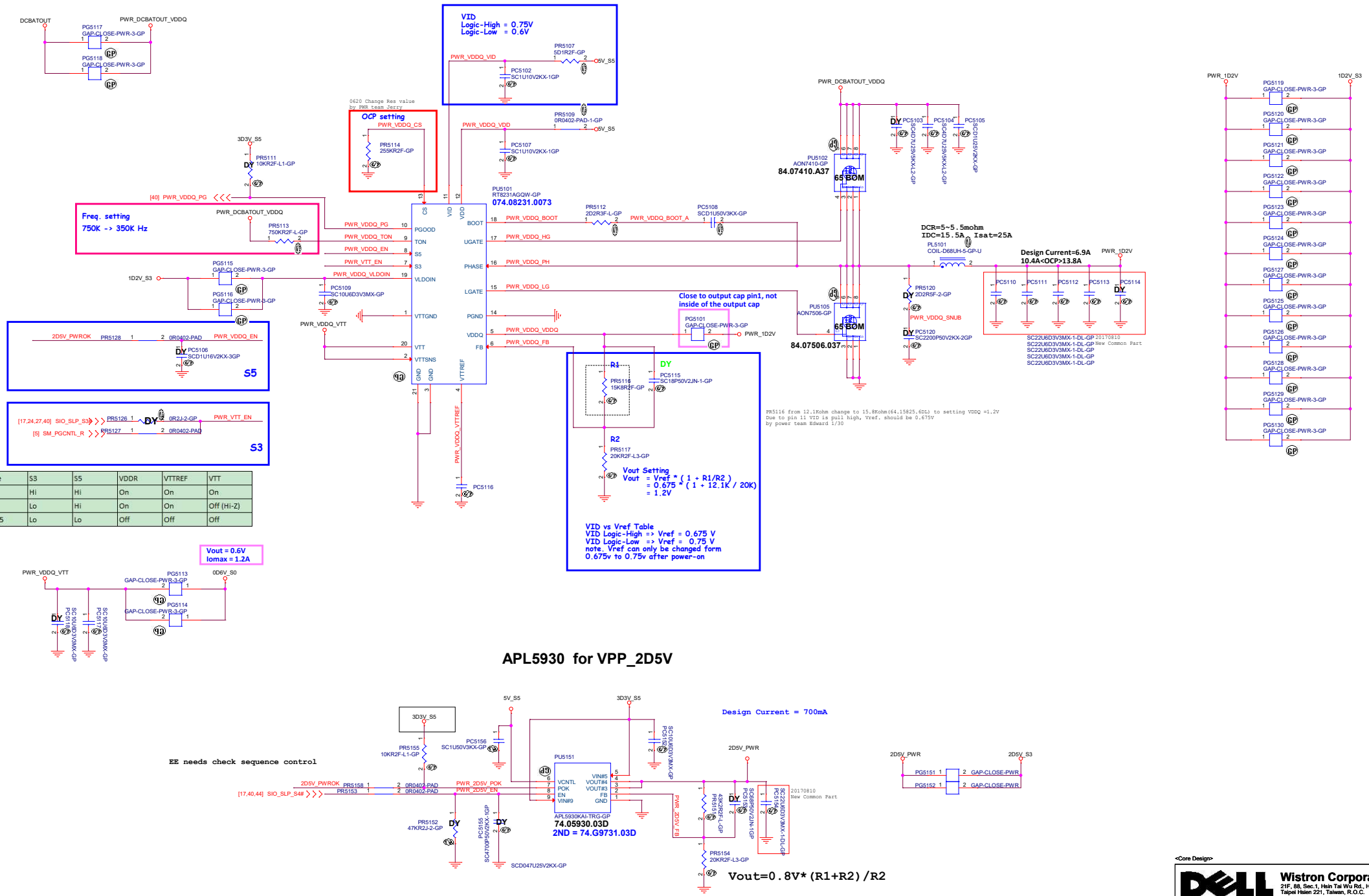


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	NCP81253MN_CPU_VCCSA	
Size: A3	Document Number: Vegas SKL/KBL-R	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 50 of 105	

SSID = PWR.Plane.Regulator_1p2v& 2D5V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Vout Setting
Vout = Vref * (1 + R1/R2)
= 0.675 * (1 + 12.1K / 20K)
= 1.2V

VID vs Vref Table
VID Logic-High => Vref = 0.675 V
VID Logic-Low => Vref = 0.75 V
note. Vref can only be changed form
0.675v to 0.75v after power-on

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

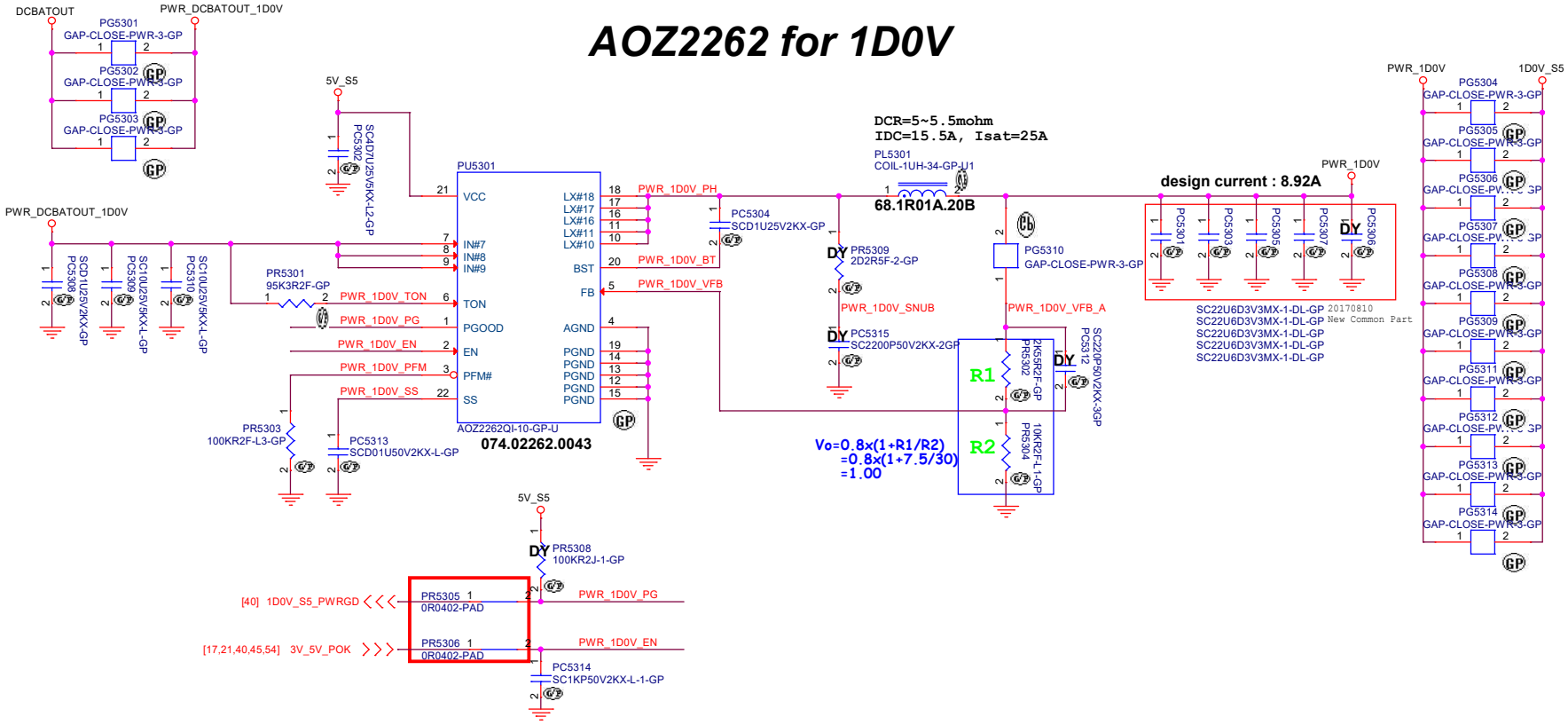
Title: RT8231_VDDQ/VTT

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 51 of 105

SSID = PWR.Plane.Regulator_1p0v

AOZ2262 for 1D0V



<Core Design>

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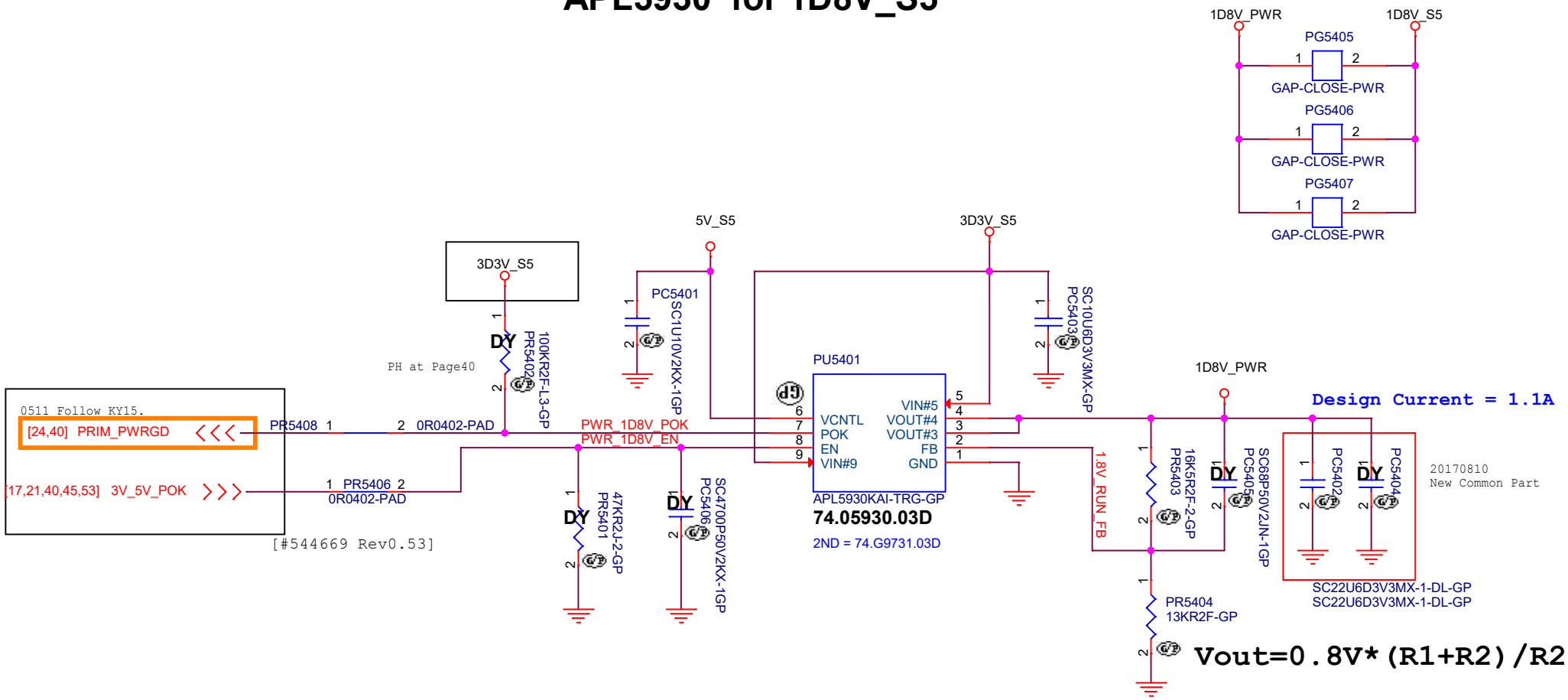
Taipei Hsien 221, Taiwan, R.O.C.

Title	AOZ2262QI_1D0V	
Size: Custom	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 53 of 105	

Main Func = 1D8V

APL5930 for 1D8V_S5

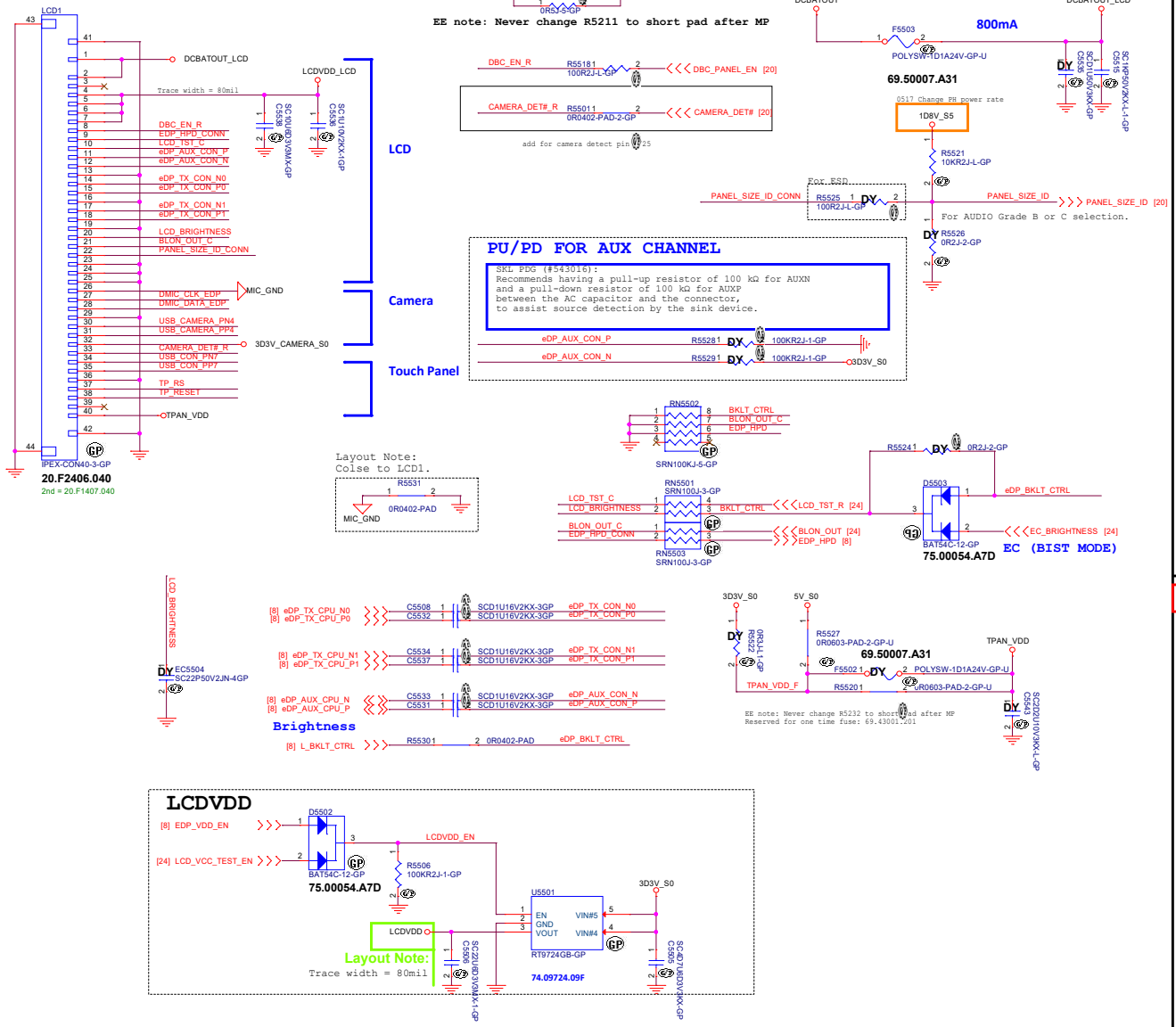


<Core Design>

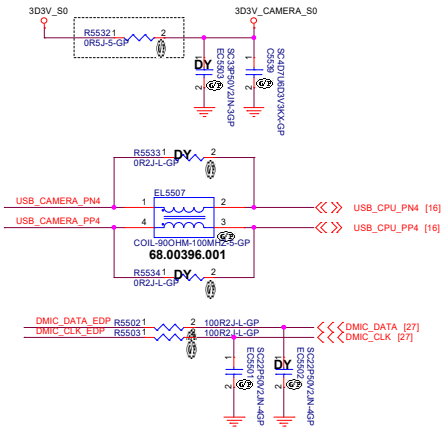
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *LDO-V1D5V&V1D8V*		
Size: A4	Document Number: *Vegas SKL/KBL-U*	Rev: *A00*
Date: Wednesday, November 08, 2017	Sheet 54 of 105	

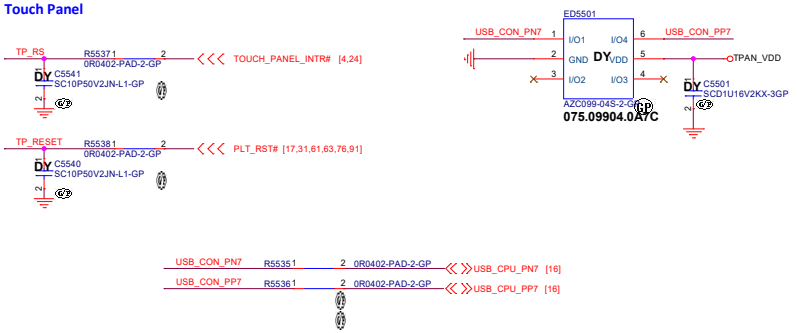
Main Func = LCD



Main Func = CAMERA



Main Func = Touch panel



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD&CAM&DMC&Touch
Size: Custom
Document Number: Vegas SKL/KBL-U
Rev: A00
Date: Wednesday, November 08, 2017
Sheet 55 of 105

Main Func = CRT

CRT Connector

VGA1

D-SUB-15-297-GP

020.20067.0015

2nd = 20.20975.015

For EMI R2 SPEC Reserved

83.05725.0A0

83.05725.0A0

83.05725.0A0

Layout note:
R5607, R5608, R5606 need to close U5601
Trace length not over 300 mil

Layout note:
C5611 & C5612 & C5613 & C5614 & C5618 & C5619 & L5601 & L5602 & L5603 need to close connect

U5601

RTD2166-CGT-GP

071.02166.0003

Layout note:
close to pin17

<Core Design>

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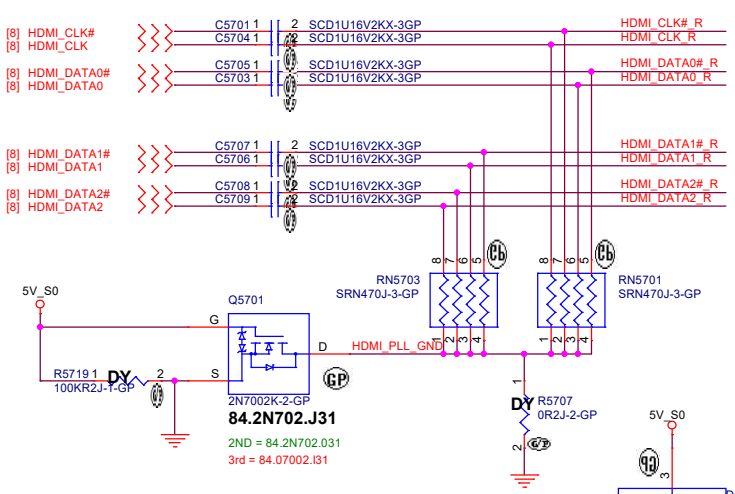
Taipei Hsien 221, Taiwan, R.O.C.

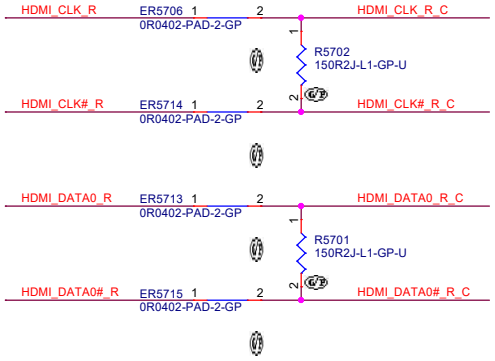
Title: CRT

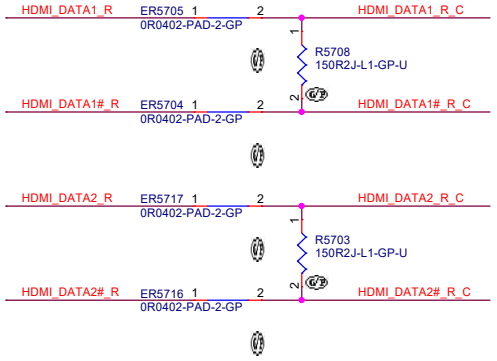
Size: Custom | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 56 of 105

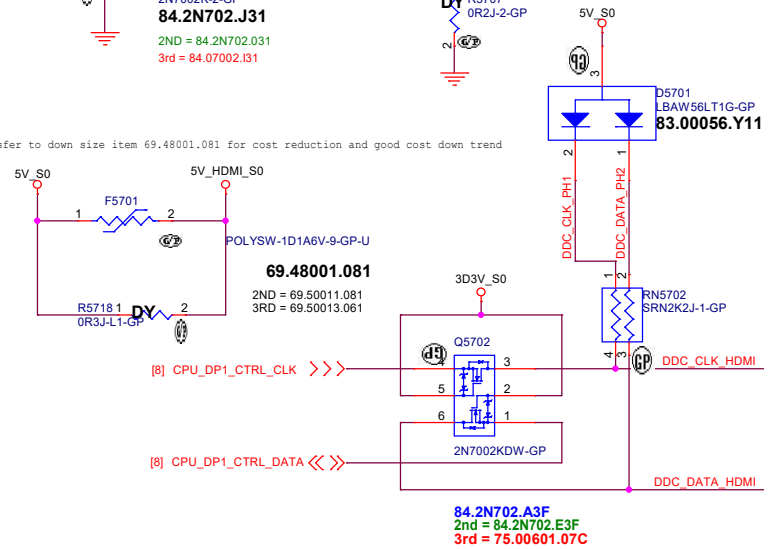
Main Func = HDMI



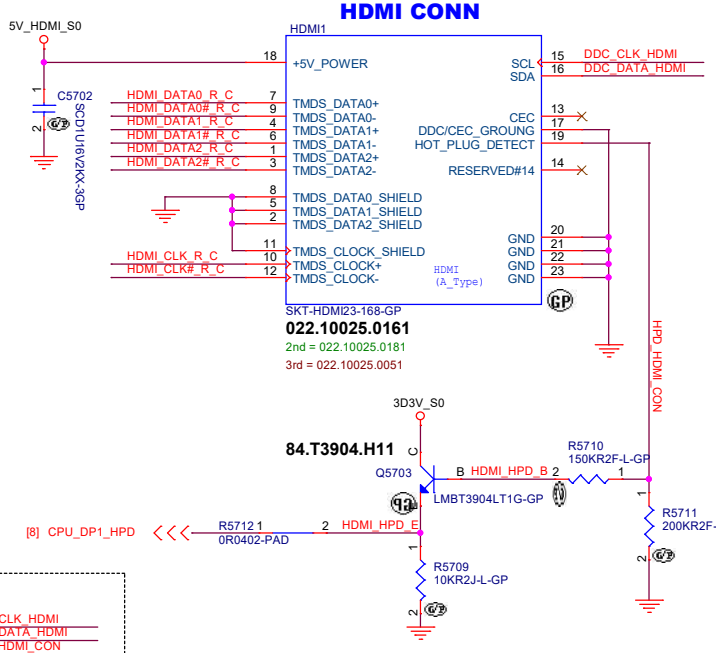




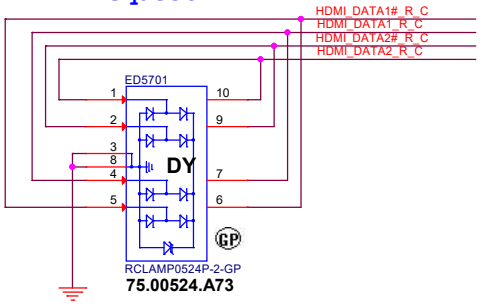
69.50007.691:
OBS REASON: Please transfer to down size item 69.48001.081 for cost reduction and good cost down trend

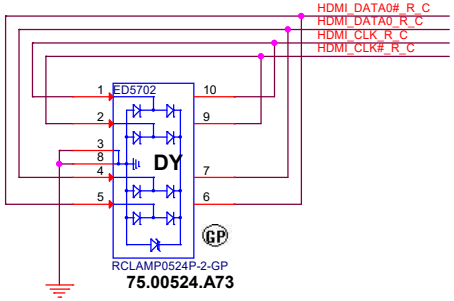


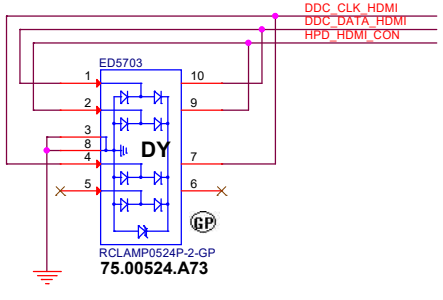
HDMI CONN



EMI Request:







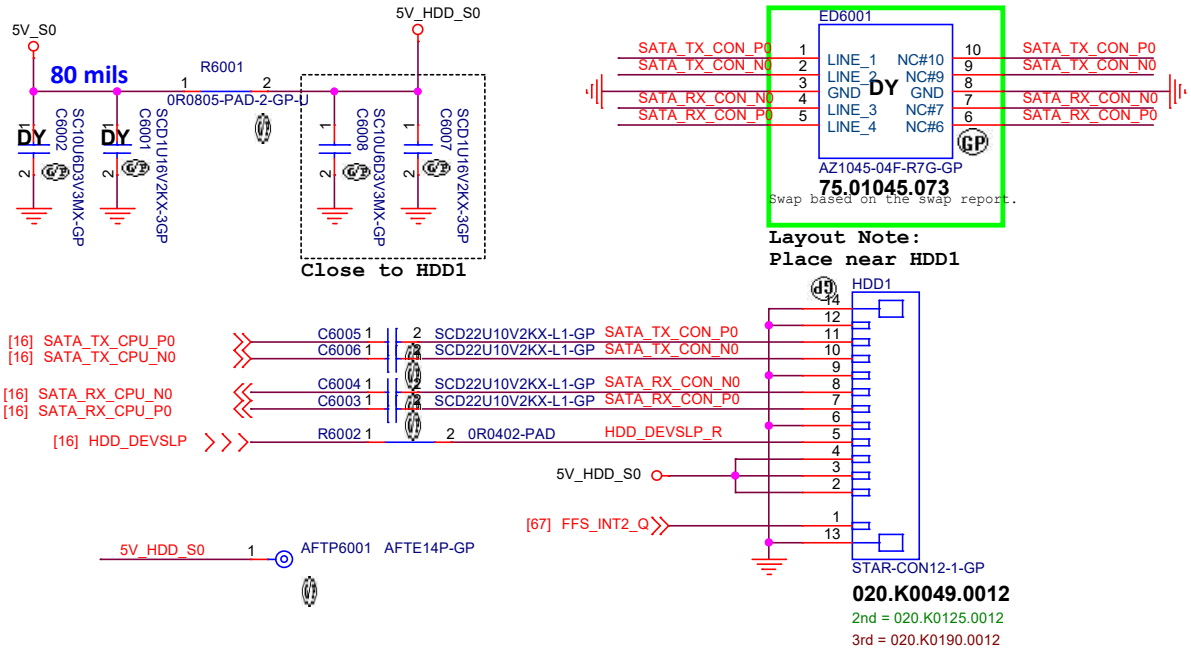
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI		
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 57 of 105	

Main Func = HDD

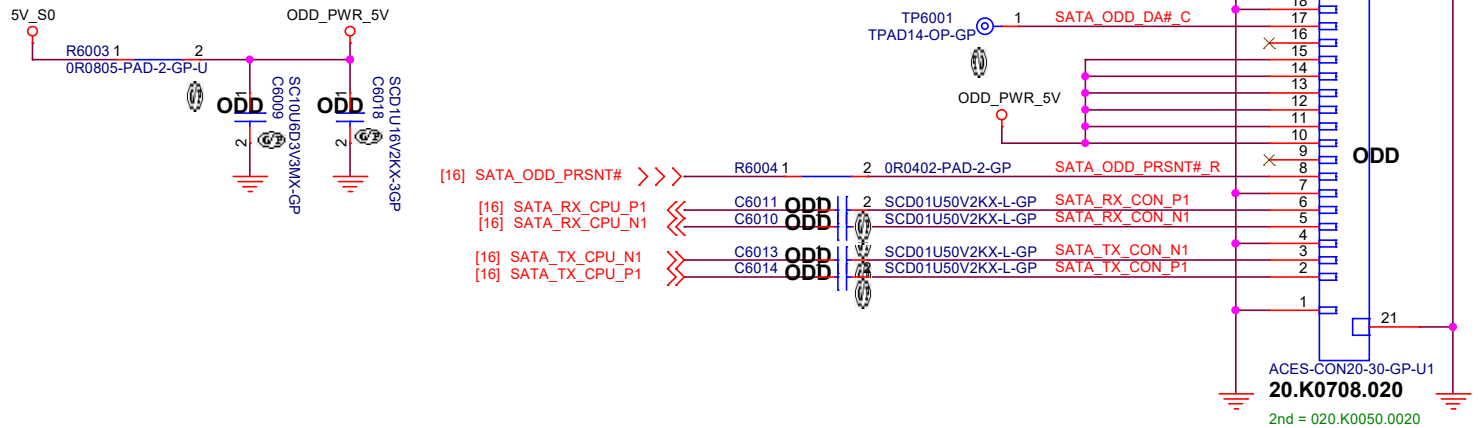
SATA HDD Connector



CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

ODD Connector



<Core Design>

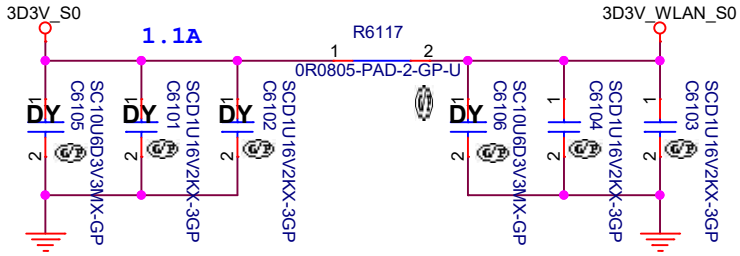
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

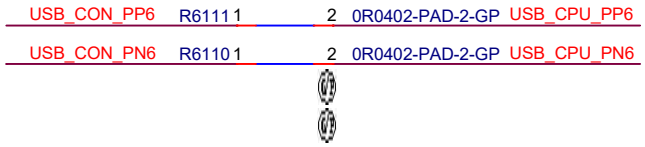
Title: INT IO (HDD/ODD)

Size: Custom | Document Number: Vegas SKL/KBL-U | Rev: A00

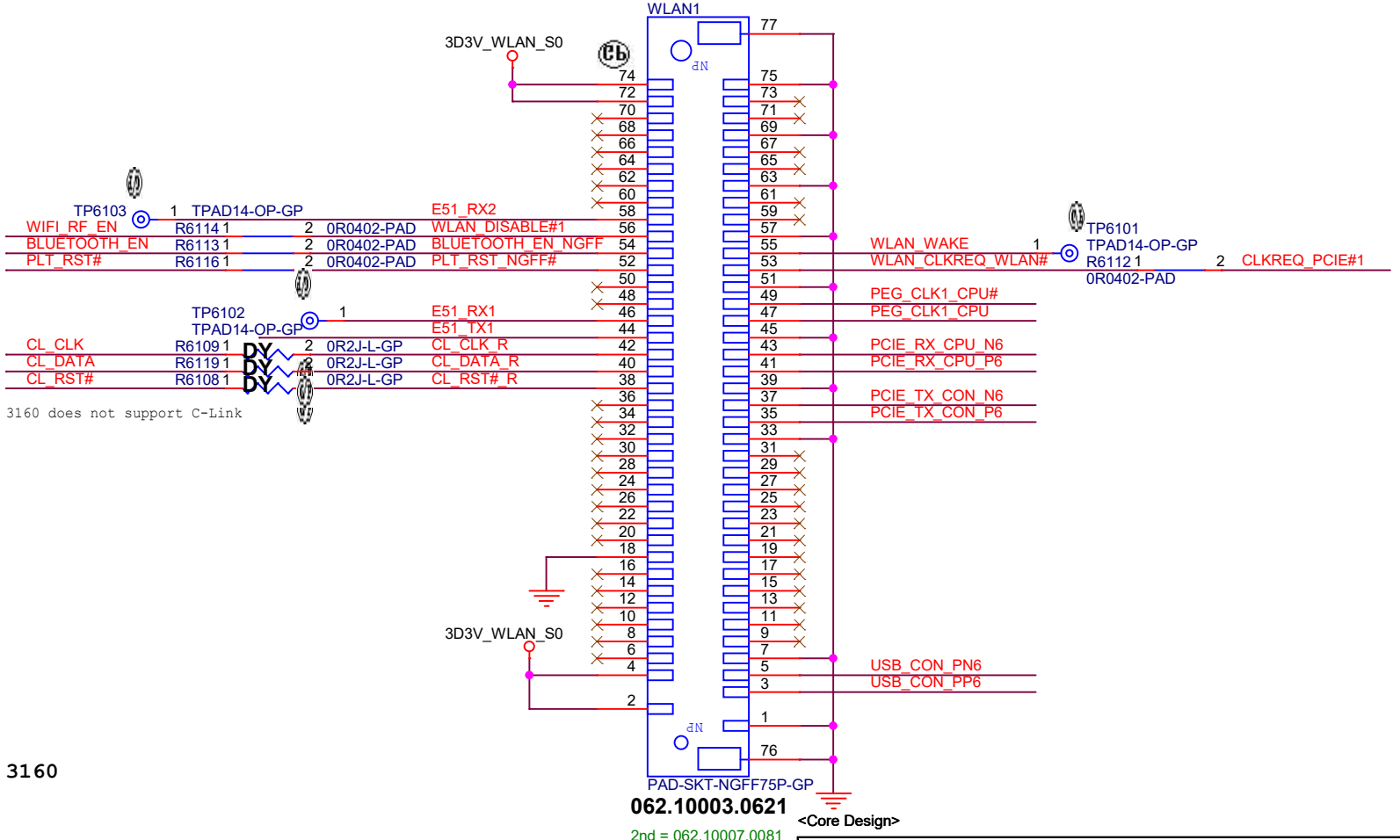
Date: Wednesday, November 08, 2017 | Sheet 60 of 105

Main Func = WLAN





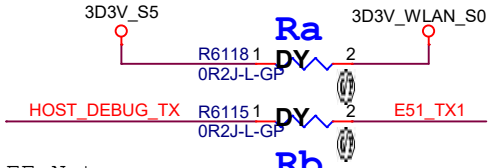
[18] PEG_CLK1_CPU#
[18] PEG_CLK1_CPU
[16] PCIE_RX_CPU_N6
[16] PCIE_RX_CPU_P6
[16] PCIE_TX_CON_N6
[16] PCIE_TX_CON_P6
[18] CLKREQ_PCIE#1
[15] WIFI_RF_EN
[20] BLUETOOTH_EN
[24,68] HOST_DEBUG_TX
[17,31,55,63,76,91] PLT_RST#
[18] CL_RST#
[18] CL_CLK
[18] CL_DATA
[16] USB_CPU_PN6
[16] USB_CPU_PP6



062.10003.0621 <Core Design>

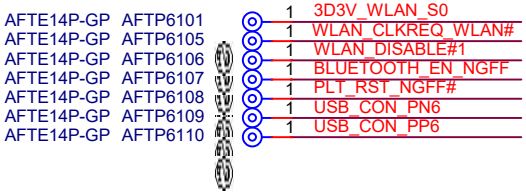
2nd = 062.10007.0081
3rd = 062.10007.0391

Reserved for NGFF Debug Card



EE Note:
For NFGG Debug Card:
Stuff Ra, Rb; DY Rc.
Note:pin 76 and pin 77 need contact to GND

Support: Intel Dual Band Wireless-AC 3160



Wistron Corporation
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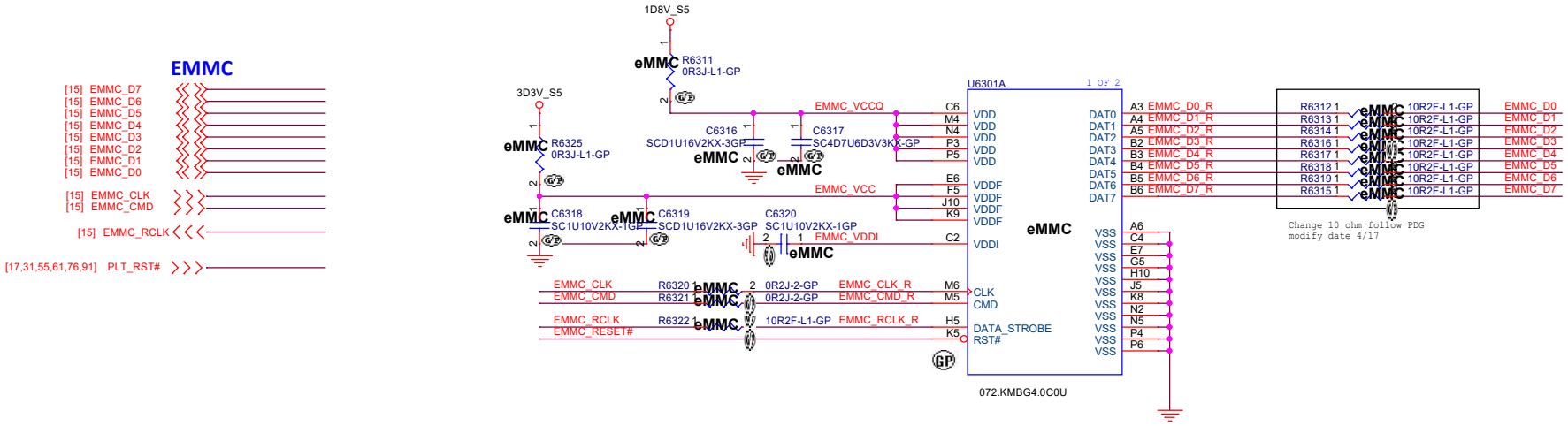
Taipei Hsien 221, Taiwan, R.O.C.

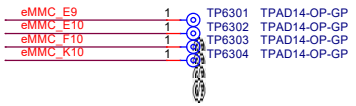
Title: **NGFF_WLAN CONN**

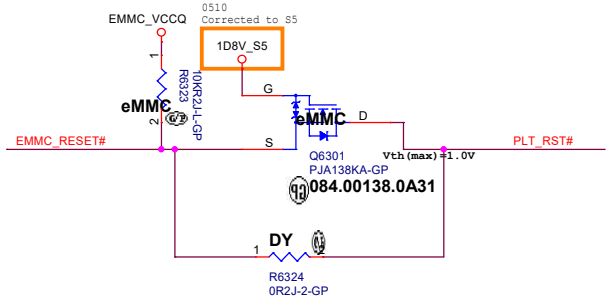
Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

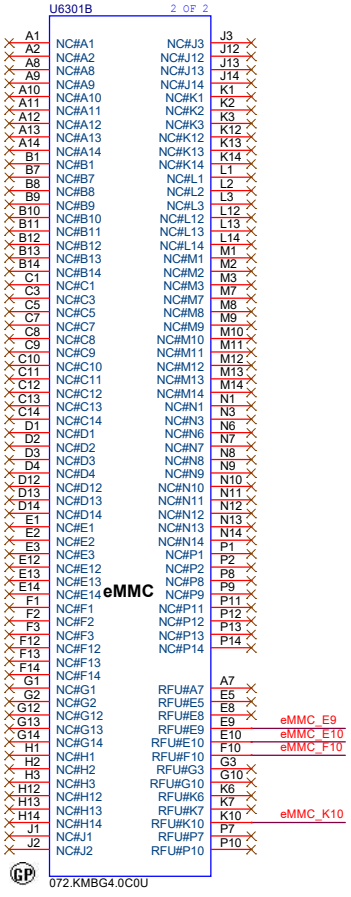
Date: Wednesday, November 08, 2017 Sheet 61 of 105

Main Func = eMMC









<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

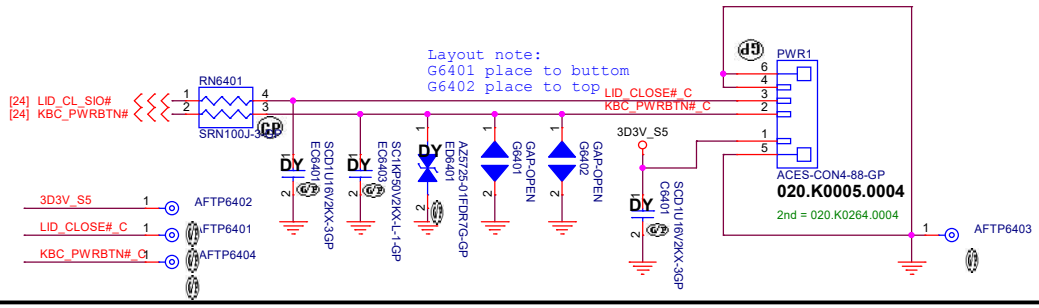
Title: eMMC

Size: A3 | Document Number: Vegas SKL/KBL-R | Rev: A00

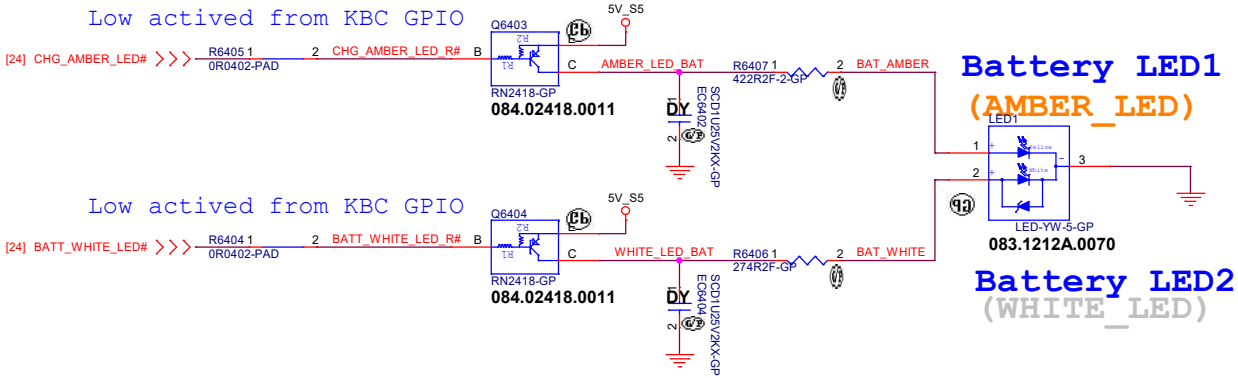
Date: Wednesday, November 08, 2017 | Sheet 63 of 105

Main Func = Power BTN

Power button

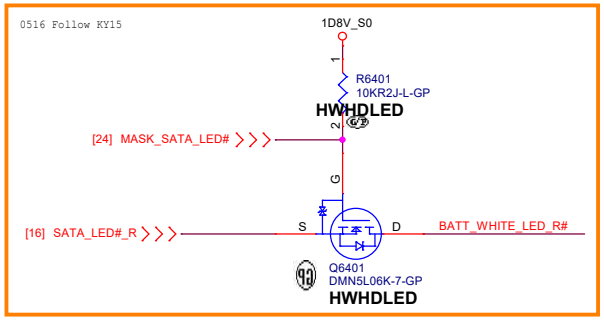


Main Func = Battery LED



Main Func = HDD LED

SATA HDD LED
LOW actived from PCH GPIO



<Core Design>

Wistron Corporation
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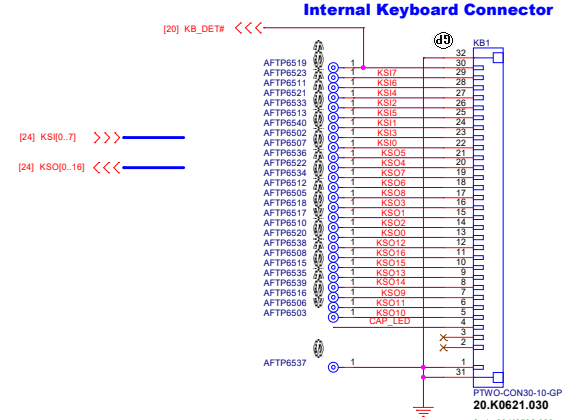
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED Board&Power Button	
Size A3	Document Number Vegas SKL/KBL-U	Rev A00
Date: Wednesday, November 08, 2017	Sheet 64 of 105	

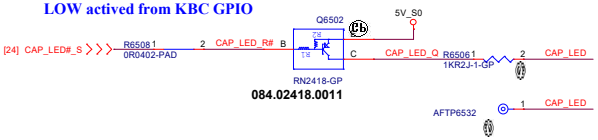
Main Func = KB

Internal Keyboard Connector



CAP LED Control

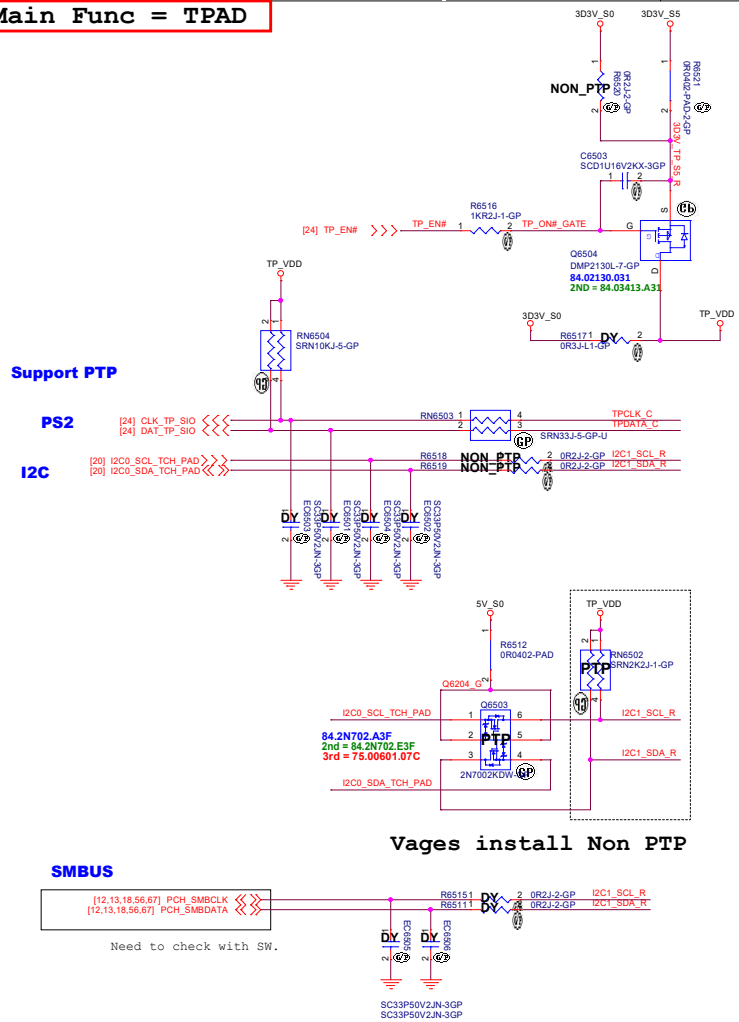
LOW actived from KBC GPIO

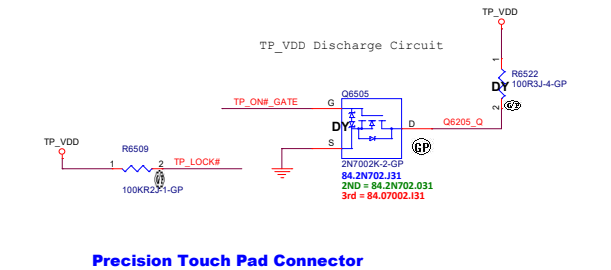


0502 Deleted KB2

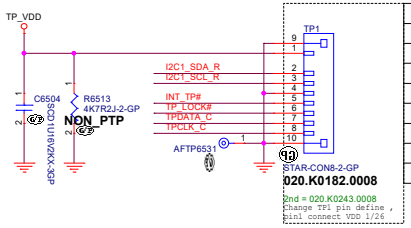
0524 Deleted KBBL1 block

Main Func = TPAD



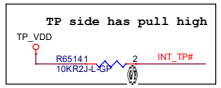


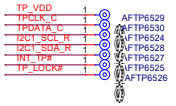
Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

Need to check if it is Active High or Active Low and check if there is PH on TPAD side.





[4,24] INT_TP#
[24] TP_LOCK#

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

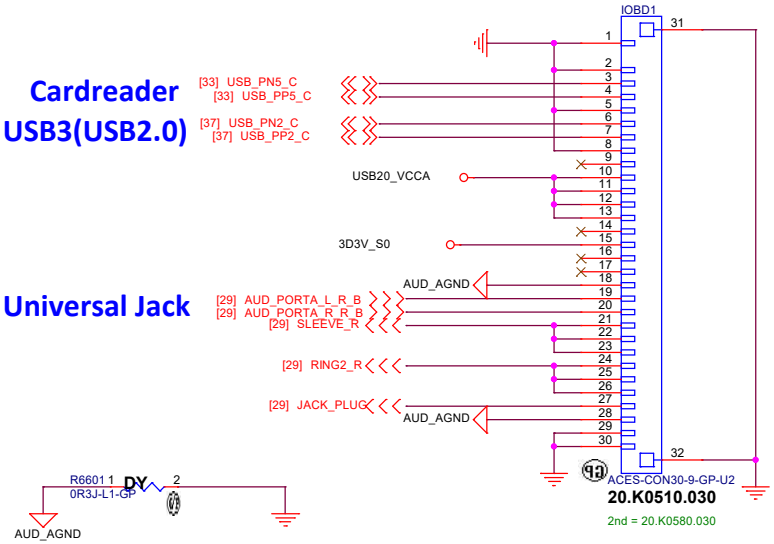
Title: Key Board&Touch Pad

Size: Custom | Document Number: Vegas SKL/KBL-U | Rev: A00

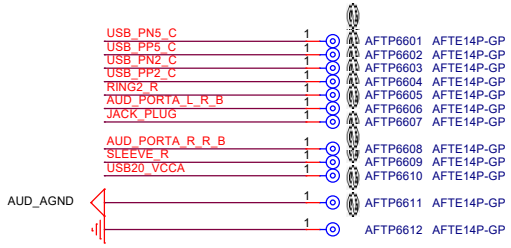
Date: Wednesday, November 08, 2017 | Sheet 65 of 105

Main Func = IO Connector

I/O Board Connector



Pitch: 1mm
Power: 6 pins
GND: 7 pins
AGND: 2 Pins



<Core Design>

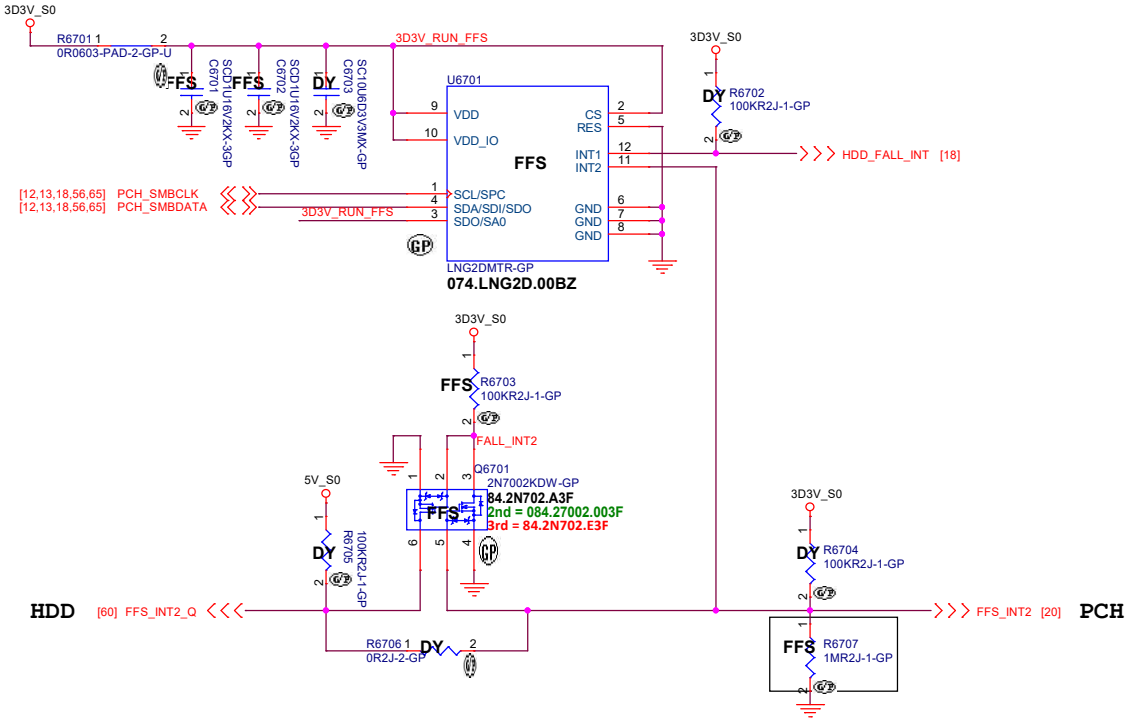
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A3
Document Number: Vegas SKL/KBL-U
Rev: A00
Date: Wednesday, November 08, 2017
Sheet 66 of 105

SSID = User.interface

Free Fall Sensor

DVT1 add FFS 2/18



2014.04.24 Venrer suggest,reserve to prevent error trigger

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

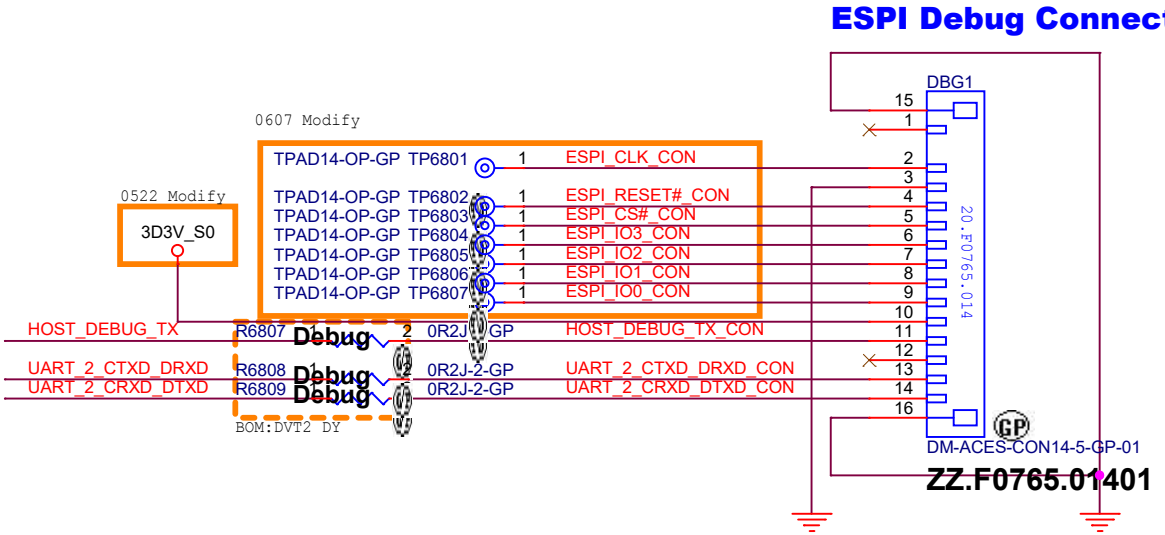
Title: Free Fall Sensor		
Size: A3	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 67 of 105	

Main Func = Debug

UART

[24,61] HOST_DEBUG_TX
[20] UART_2_CTXD_DRXD
[20] UART_2_CRXD_DTXD

ESPI Debug Connector



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Dubug connector*

Size	Document Number	Rev
A4	*Vegas SKL/KBL-R*	*A00*

Date: Friday, November 10, 2017 Sheet 68 of 105

Main Func = dGPU

20170502

GFX & GPP, 85Ω
GFX & GPP CLK, 85Ω

GPU1A 1 OF 7

[16] PEG_TX_GPU_P0
[16] PEG_TX_GPU_N0
[16] PEG_TX_GPU_P1
[16] PEG_TX_GPU_N1
[16] PEG_TX_GPU_P2
[16] PEG_TX_GPU_N2
[16] PEG_TX_GPU_P3
[16] PEG_TX_GPU_N3

PEG_TX_GPU_P0 AF30 PCIE_RX0P
PEG_TX_GPU_N0 AE31 PCIE_RX0N
PEG_TX_GPU_P1 AE29 PCIE_RX1P
PEG_TX_GPU_N1 AD28 PCIE_RX1N
PEG_TX_GPU_P2 AD30 PCIE_RX2P
PEG_TX_GPU_N2 AC31 PCIE_RX2N
PEG_TX_GPU_P3 AC29 PCIE_RX3P
PEG_TX_GPU_N3 AB28 PCIE_RX3N
AB30 PCIE_RX4P
AA31 PCIE_RX4N
AA29 PCIE_RX5P
Y28 PCIE_RX5N
Y30 PCIE_RX6P
W31 PCIE_RX6N
W29 PCIE_RX7P
V28 PCIE_RX7N
V30 NC#V30
U31 NC#U31
U29 NC#U29
T28 NC#T28
T30 NC#T30
R31 NC#R31
R29 NC#R29
P28 NC#P28
P30 NC#P30
N31 NC#N31
N29 NC#N29
M28 NC#M28
M30 NC#M30
L31 NC#L31
L29 NC#L29
K30 NC#K30

PCIE_TX0P AH30 PEG_RX_GPU_P0 C7601 OPS SCD22U10V2KX-L1-GP PEG_RX_CPU_P0 [16]
PCIE_TX0N AG31 PEG_RX_GPU_N0 C7602 OPS SCD22U10V2KX-L1-GP PEG_RX_CPU_N0 [16]
PCIE_TX1P AG29 PEG_RX_GPU_P1 C7603 OPS SCD22U10V2KX-L1-GP PEG_RX_CPU_P1 [16]
PCIE_TX1N AF28 PEG_RX_GPU_N1 C7604 OPS SCD22U10V2KX-L1-GP PEG_RX_CPU_N1 [16]
PCIE_TX2P AF27 PEG_RX_GPU_P2 C7605 OPS SCD22U10V2KX-L1-GP PEG_RX_CPU_P2 [16]
PCIE_TX2N AF26 PEG_RX_GPU_N2 C7606 OPS SCD22U10V2KX-L1-GP PEG_RX_CPU_N2 [16]
PCIE_TX3P AD27 PEG_RX_GPU_P3 C7607 OPS SCD22U10V2KX-L1-GP PEG_RX_CPU_P3 [16]
PCIE_TX3N AD26 PEG_RX_GPU_N3 C7608 OPS SCD22U10V2KX-L1-GP PEG_RX_CPU_N3 [16]
PCIE_TX4P AC25
PCIE_TX4N AB25
PCIE_TX5P Y23
PCIE_TX5N Y24
PCIE_TX6P AB27
PCIE_TX6N AB26
PCIE_TX7P Y27
PCIE_TX7N Y26
NC#W24 W24
NC#W23 W23
NC#V27 V27
NC#U26 U26
NC#U24 U24
NC#U23 U23
NC#T26 T26
NC#T27 T27
NC#T24 T24
NC#T23 T23
NC#P27 P27
NC#P26 P26
NC#P24 P24
NC#P23 P23
NC#M27 M27
NC#N26 N26

PCI EXPRESS INTERFACE

CLOCK
[18] PEG_CLK_CPU AK30 PCIE_REFCLKP
[18] PEG_CLK_CPU# AK32 PCIE_REFCLKN

TEST_PG
PWRGOOD_TEST N10

PERST#
VGA_RST# AL27

CALIBRATION
PCIE_CALR_TX Y22
PCIE_CALR_RX AA22

JET-XT-S3-GP
OPS

Table 3–5 PCI Express® Bus Interface

Pin Name	I/O	Description
PERSTb	I	Fundamental reset. 3.3-V tolerant pad. This signal must be asserted during any fundamental reset event, such as power up, warm boot, reset button pressed, CTL-ALT-DEL, Windows restart, or wake from D3.
PCIE_REFCLKP/N	I	PCI Express PLL differential reference clock (+/-). 100-MHz (± 300 ppm) input frequency; 0-V to 0.7-V single-ended swing.
PCIE_TX[7:0]P/N	O	PCI Express transmitter output data channel TX[7:0] (+/-). Differential serial data transmitted up to a 8.0-GT/s bit rate.
PCIE_RX[7:0]P/N	I	PCI Express receiver input data channel RX[7:0] (+/-). Differential serial data received up to a 8.0-GT/s bit rate.
PCIE_CALR_RX	I	Connect to PCIE_VDDC through a 1-kΩ (1% tolerance) resistor.
PCIE_CALR_TX	I	Connect to PCIE_VDDC through a 1.69-kΩ (1% tolerance) resistor.
CLKREQB	O	Reserved, do not connect on the PCB.

DGPU_HOLD_RST#	
H	dGPU mode
L	IGPU
H	IGPU with BACO

3D3V_VGA_S0
R7625 10KR2J-L-GP DY
R7623 1 0R0402-PAD 2
[20] DGPU_HOLD_RST#
R7601 1KR2F-L1-GP OPS
ATI_RST# R7621 1 0R0402-PAD 2
[17,31,55,61,63,91] PLT_RST#
D7601 BAW56-5-GP
C7609 SC47P50V2JN-3GP DY

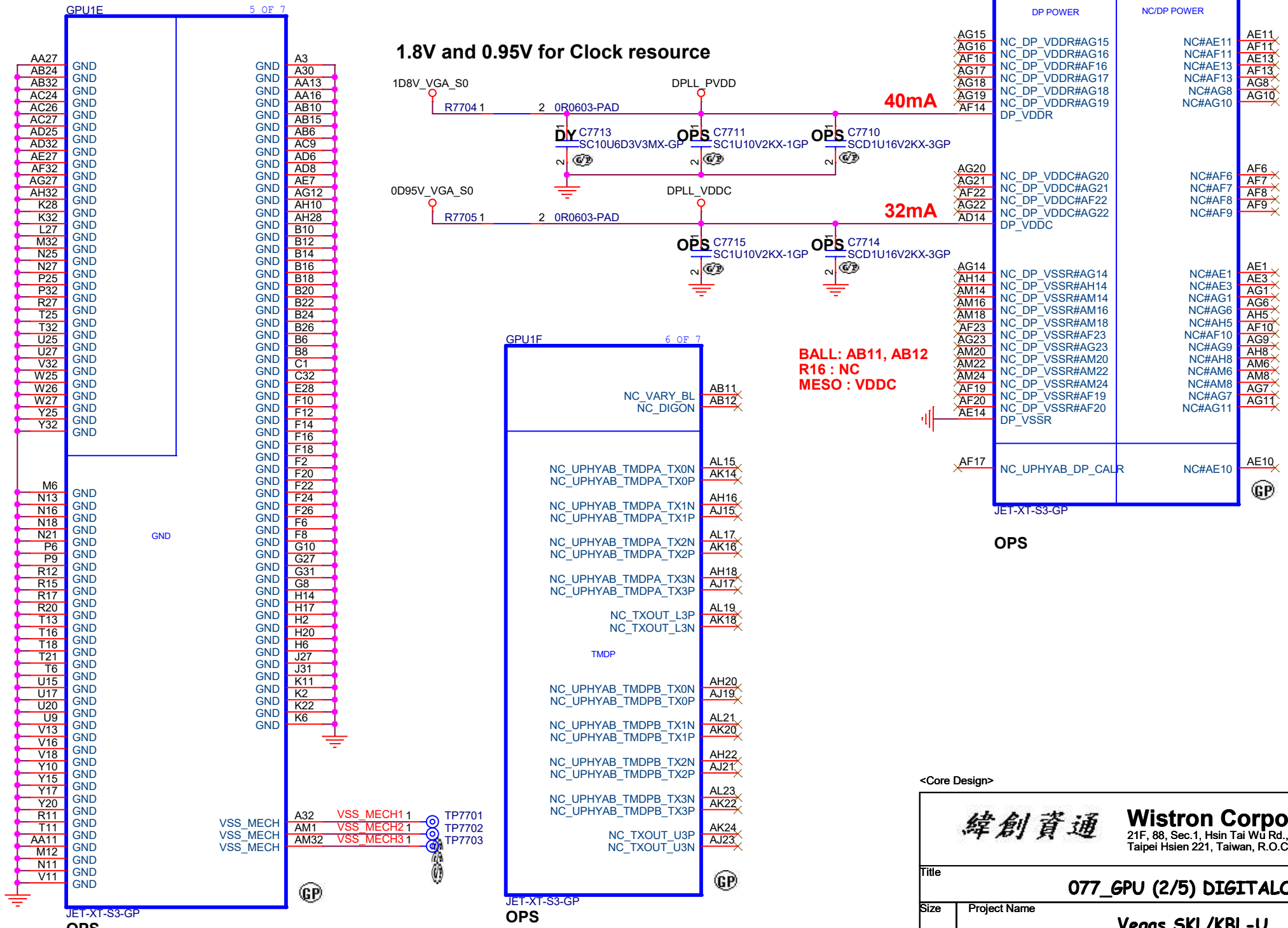
PCIE_CALR_TX 1K69R2F-2-GP OPS R7622 0D95V_VGA_S0
PCIE_CALR_RX R7618 1KR2F-L1-GP OPS

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 076_GPU(1/5) PEG
Size | Project Name: <Project Name> | Rev
Date: Wednesday, November 08, 2017 Sheet 76 of 105

Main Func = dGPU



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	077_GPU (2/5) DIGITALOUT	
Size	Project Name: Vegas SKL/KBL-U	Rev: X00
Date: Wednesday, November 08, 2017	Sheet 77 of 105	

Main Func = dGPU

[81] DQA0_0 … [81] DQA0_31

[81] DQA1_0 … [81] DQA1_31

[81] MAA0_0 … [81] MAA0_8

[81] MAA1_0 … [81] MAA1_8

[81] EDCA0_0 … [81] EDCA0_3

[81] EDCA1_0 … [81] EDCA1_3

[81] DDBIA0_0 … [81] DDBIA0_3

[81] DDBIA1_0 … [81] DDBIA1_3

[81] WCKA0_0
[81] WCKA0b_0
[81] WCKA0_1
[81] WCKA0b_1
[81] WCKA1_0
[81] WCKA1b_0
[81] WCKA1_1
[81] WCKA1b_1

[81] ADBIA0
[81] ADBIA1

[81] CSA0b_0
[81] CSA1b_0

[81] CKEA0
[81] CKEA1

[81] WEA0b
[81] WEA1b

[81] CASA0b
[81] CASA1b
[81] RASA0b
[81] RASA1b

[81] CLKA0
[81] CLKA0b
[81] CLKA1
[81] CLKA1b

Please MVREF drivers and Caps close to ASIC

DDR3/GDDR3 Memory Stuff Option(R16)

	GDDR5	GDDR3	DDR3
MVDDQ	1.5V	1D35V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

3.24

1D35V_VGA_S0

R7817 40D2R2F-GP (Ra) OPS — MVREFDA

R7818 100R2F-L3-GP (Rb) OPS — C7805 SC1U10V2KX-1GP OPS

1D35V_VGA_S0

R7810 40D2R2F-GP (Ra) OPS — MVREFSA

R7814 100R2F-L3-GP (Rb) OPS — C7801 SC1U10V2KX-1GP OPS

Place all these componets very close to GPU (within 25mm) and keep all components close to each other
This basic topology should be used for DRAM_RST for DDR3/GDDR5

1D35V_VGA_S0

DY R7802 2K2R2J-L1-GP

[81] DRAM_RST — R7804 49D9R2F-L1-GP OPS — DRAM_RST_R — R7803 10R2J-L-GP OPS — DRAM_RST_VGA1

C7802 SC100P50V2JN-3GP OPS

R7819 5K1R2F-2-GP OPS

DY C7803 SC68P50V2JN-1GP

???
Difference with AMD

0510
Follow AMD adding DY ca

GPU1C 3 OF 7

GDDR5/DDR3 — DQA0_0 … DQA0_31 (K27, J29, H30, H32, G29, F28, F32, F30, C30, F27, A28, C28, E27, G26, D26, F25, A25, C25, E25, D24, E23, F23, D22, F21, E21, D20, F19, A19, D18, F17, A17, C17, E17, D16, F15, A15, D14, F13, A13, C13, E11, A11, C11, F11, A9, C9, F9, D8, E7, A7, C7, F7, A5, E5, C3, E1, G7, G6, G1, G3, J6, J1, J3, J5)

DQA1_0 … DQA1_31 (K25, J25, H25, H23, G23, G24, H24, J19, K19, G20, L17, J14, K14, J11, J13, H11, G11, J16, L15, G14, L16, E32, E30, A21, C21, E13, D12, E3, F4, H28, C27, A23, E19, E15, D10, D6, G5, H27, A27, C23, C19, C15, E9, C5, H4, L18, K16, H26, H25, G9, H9, G22, G17, G19, G16, H22, J22, G13, K13, K20, J17, G25, H10)

MVREFDA K26 — MVREFDA
MVREFSA J26 — MVREFSA

NC#J25 — MEM_CALRP0 K25 — MEM_CALRP0

Jet Setting
R7809 1 OPS 120R2F-GP

DRAM_RST_VGA1 — L10 — DRAM_RST#

CLKTESTA K8 — CLKTESTA
CLKTESTB L7 — CLKTESTB

JET-XT-S3-GP
OPS

C7822 SCD1U16V2KX-3GP DY — C7821 SCD1U16V2KX-3GP DY

CLKTESTA_C — CLKTESTB_C

R7821 51D1R2F-GP DY — R7820 51D1R2F-GP DY

Debug only, for clock observation, if not needed, DNI

MEMORY INTERFACE

MAA0_0 … MAA0_9 (K17, J20, H23, G23, G24, H24, J19, K19, G20, L17)

MAA1_0 … MAA1_9 (J14, K14, J11, J13, H11, G11, J16, L15, G14, L16)

WCKA0_0 … WCKA1#_1 (E32, E30, A21, C21, E13, D12, E3, F4)

EDCA0_0 … EDCA1_3 (H28, C27, A23, E19, E15, D10, D6, G5)

DDBIA0_0 … DDBIA1_3 (H27, A27, C23, C19, C15, E9, C5, H4)

ADBIA0 L18 — ADBIA0
ADBIA1 K16 — ADBIA1

CLKA0 H26 — CLKA0
CLKA0# H25 — CLKA0b
CLKA1 G9 — CLKA1
CLKA1# H9 — CLKA1b

RASA0# G22 — RASA0b
RASA1# G17 — RASA1b
CASA0# G19 — CASA0b
CASA1# G16 — CASA1b

CSA0#_0 H22 — CSA0b_0
CSA0#_1 J22
CSA1#_0 G13 — CSA1b_0
CSA1#_1 K13

CKEA0 K20 — CKEA0
CKEA1 J17 — CKEA1

WEA0# G25 — WEA0b
WEA1# H10 — WEA1b

ADD
DM
DQS
Ctrl
CLK
CMD
Ctrl, CS
Ctrl
CMD

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **078_GPU (3/5) VRAM I/F**

Size | Project Name: **Vegas SKL/KBL-U** | Rev

Date: Wednesday, November 08, 2017 | Sheet 78 of 105

Main_Func = dGPU

#3 PS0 ~ PS3 Setting

PS_0	R_pu	R_pd	Bits[3:1]	Size of the Prima
	NC	4750	000	128 MB
	8450	2000	001	256 MB
	4530	2000	010	64 MB
	6980	4990	011	Reserved
	4530	4990	100	N/A
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

PS_1	R_pu	R_pd	Bits[3:1]	
	NC	4750	000	PCIe GEN3 is not supported ; The CLKREQB power management capability is disabled.
	8450	2000	001	PCIe GEN3 is supported ; The CLKREQB power management capability is disabled.
	4530	2000	010	PCIe GEN3 is not supported ; The CLKREQB power management capability is enabled.
	6980	4990	011	PCIe GEN3 is supported ; The CLKREQB power management capability is enabled.
	4530	4990	100	N/A
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

PS_2	R_pu	R_pd	Bits[3:1]	
	NC	4750	000	Disable the external BIOS ROM device.
	8450	2000	001	N/A
	4530	2000	010	N/A
	6980	4990	011	N/A
	4530	4990	100	Enable the external BIOS ROM device.
	3240	5620	101	N/A
	3400	10000	110	N/A
	4750	NC	111	N/A

AMD suggest Aperture Size = 256MB — 11001

GEN3 — 11000 — 680nF

11000 — 680nF

R7929 cgange to 2K ohm 1/21

If PS_1[2:0] => GEN_3 setting, need decide for AMD

Pre-PWROK METAL VID CODES

SVC	SVD	Output Voltage
0	0	1.1
0	1	1.0
AMD suggestion 1	0	0.9
1	1	0.8

MLPS Memory ID setting:

Board_config[2:0]		Memory Type	Configuration	Row x Col x Bank bits	Channel Size	Vendor PN	Wistron PN	SMT quantity	R_pu	R_pd
ID	[2:0]								R7932	R7933
0	000	Samsung - GDDR5	256M x 32 bits		2GB	K4G80325FB-HC28	N1MMH		NC	4750
1	001	Micron - GDDR5	256M x 32 bits		2GB	MT51J256M32HF-70:A	V15MH		8450	2000
2	010	SK Hynix - GDDR5	256M x 32 bits		2GB	H5GC8H24MJR-R0C	029XX		4530	2000
3	011									
4	100									
5	101									
6	110									
7	111									

	SVID	PWR Sequencing
R16	R7919 R7920	PR8611 PC8607 / PR8612 PC8612

MESO non-install

BALL: U10,T10,Y9,W10 R16: NC MESO : VDDC

BALL: AB13, W9, AC14 R16: NC MESO : VDDC

BALL: AC11,AC13 R16: NC MESO : VDDC

R16 : DY MESO : 上件

R16: DY MESO : 上件

PINs for debug

OPS

Table 8. Boot-VID Code

SVC	SVD	Voltage Selected (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

Cap Value (nF)	Bits [5:4]
680	00
82	01
10	10
NC	11

GPU thermal sensor

Layout Note: Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

84.2N702.J31

2ND = 84.2N702.031
3rd = 84.07002.I31

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: 079_GPU (4/5) GPIO/STRAP
Size: | Project Name: Vegas SKL/KBL-U | Rev:
Date: Wednesday, November 08, 2017 | Sheet 79 of 105

Main Func = dGPU

20170502

AMD schematic Review need
10uF x 1, 2.2uFx5, 0.1uF x1, 0.01uF x1

1A
1D35V_VGA_S0
C8001 OPS SC10U6D3V3MX-GP
C8007 DY SCD1U16V2KX-3GP
C8014 DY SCD01U50V2KX-L-GP
C8003 C8004 C8005 C8006 C8009 C8031 C8032 C8033 C8034 C8042
SC1U10V2KX-1GP

GPU1D
MEM I/O
H13 H16 H19 J10 J23 J24 J9 K10 K23 K24 K9 L11 L12 L13 L20 L21 L22
VDDR1
LEVEL TRANSLATION
13mA
1D8V_VGA_S0
C8017 SC1U10V2KX-1GP OPS
AA20 AA21 AB20 AB21
VDD_CT
I/O
25mA
AA17 AA18 AB17 AB18
VDDR3
3D3V_VGA_S0
C8024 SC1U10V2KX-1GP OPS
V12 Y12 U12
NC_VDDR4#V12 NC_VDDR4#Y12 NC_VDDR4#U12

4 OF 7
PCIE
PCIE_PVDD AM30
0.1A
1D8V_VGA_S0
DY C8008 SC1U10V2KX-1GP
OPS C8002 SC10U6D3V3MX-GP
NC#AB23 AC23 NC#AC23 AD24 NC#AD24 AE24 NC#AE24 AE25 NC#AE25 AE26 NC#AE26 AF25 NC#AF25 AG26 NC#AG26
PCIE_VDDC
L23 L24 L25 L26 M22 N22 N23 N24 R22 T22 U22 V22
2.5A
0D95V_VGA_S0
C8010 DY C8016 OPS SC10U6D3V3MX-GP
AMD schematic Review need 10uF x 2, 1uFx3, 0.1uF x2
C8011 C8012 C8013 C8015 C8057 OPS
SCD1U16V2KX-3GP
SC1U10V2KX-1GP

CORE
VDDC
AA15 N15 N17 R13 R16 R18 Y21 T12 T15 T17 T20 U13 U16 U18 V21 V15 V17 V20 Y13 Y16 Y18 AA12 M11 N12 U11
AMD ORB 10U x 6 2.2U x 16
LF145M 4.7U x 6 1U x 20
VGA_CORE
C8018 C8019 C8020 C8021 C8022 C8023 C8025 C8026 C8027 OPS
SC1U10V2KX-1GP
NC on JET
AB13 U10 W9 Y9 W10 T10 AC14 AB12 AB11 AC11 AC13
C8028 C8029 C8030 C8035 C8036 C8037 C8058 C8059 C8060 OPS

POWER
BIF_VDDC
R21 U21
1.4A
0D95V_VGA_S0
C8065 SC1U10V2KX-1GP OPS

ISOLATED CORE I/O
VDDCI
M13 M15 M16 M17 M18 M20 M21 N20
5A
AMD ORB 10U x 2 1U x 3 0.1U x2
LF145M 4.7U x 2 1U x 3 0.1U x 2
VGA_CORE
C8046 C8047 C8048 C8049 C8050 C8051 C8052 OPS
SCD1U16V2KX-3GP
SC1U10V2KX-1GP
SC4D7U6D3V3KX-GP

PLL
MPV18 90mA L8 MPLL_PVDD
SPV18 75mA H7 SPLL_PVDD
SPV10 100mA H8 SPLL_VDDC
J7 SPLL_PVSS

JET-XT-S3-GP

Memory phase lock loop power: Dedicated analogue power in for memory PLLs
1D8V_VGA_S0
L8001 OPS MMZ1005S241C-GP MPV18
C8043 SC10U6D3V3MX-GP OPS
C8044 SC10U6D3V3MX-GP OPS
C8045 SC1U10V2KX-1GP OPS

Engine phase loop power: Dedicated analogue power pin for engine PLL
1D8V_VGA_S0
L8002 OPS BLM15AG121SN-1GP SPV18
68.00084.921
C8053 SC10U6D3V3MX-GP OPS
C8054 SC1U10V2KX-1GP OPS

Engine phase loop power: Dedicated digital power pin for engine PLL
0D95V_VGA_S0
L8003 OPS BLM15AG121SN-1GP SPV10
68.00084.921
C8055 SC1U10V2KX-1GP OPS
C8056 SCD1U16V2KX-3GP OPS

VGA_CORE
C8038 C8039 C8040 C8041 C8063 C8064 OPS
SC10U6D3V3MX-GP

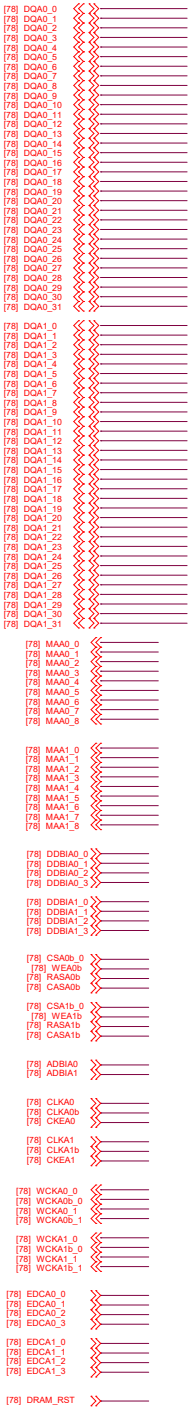
VGA_CORE
OPS C8066 SC22U6D3V3MX-1-GP
OPS C8061 SC1U10V2KX-1GP
OPS C8062 SC1U10V2KX-1GP

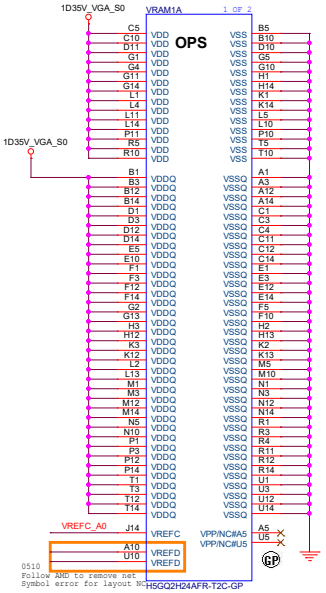
<Core Design>

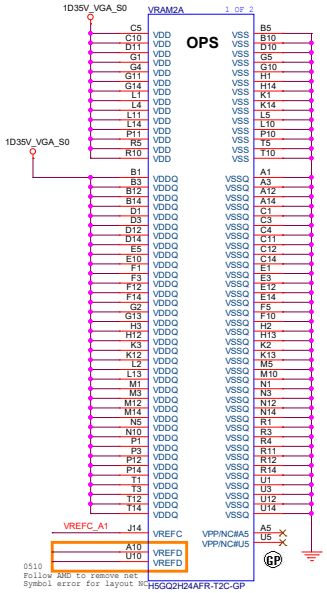
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

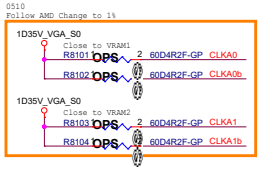
Title	080_GPU (5/5) PWR/GND	
Size	Project Name <Project Name>	Rev
Date: Wednesday, November 08, 2017	Sheet 80 of 105	

SSID = Vram (GDDR5)

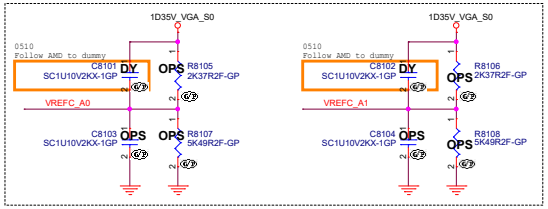


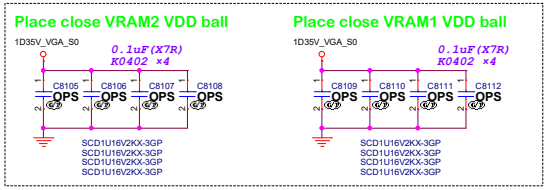


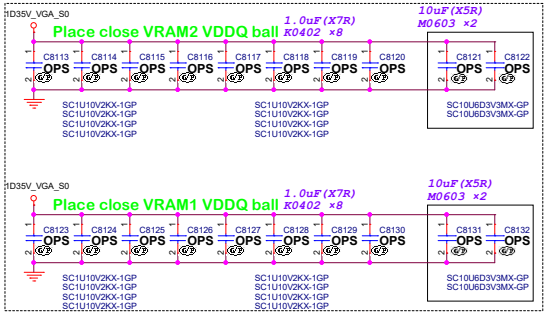




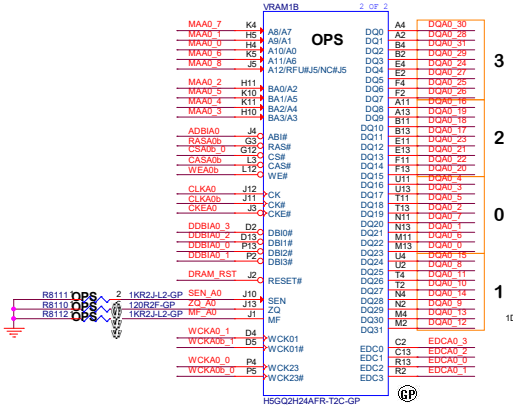
Frame Buffer Patition A-Lower Half



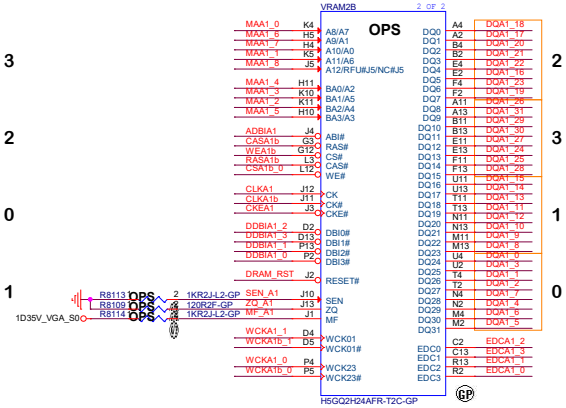




Normal(MF=0)



Mirrored(MF=1)



<Core Design>
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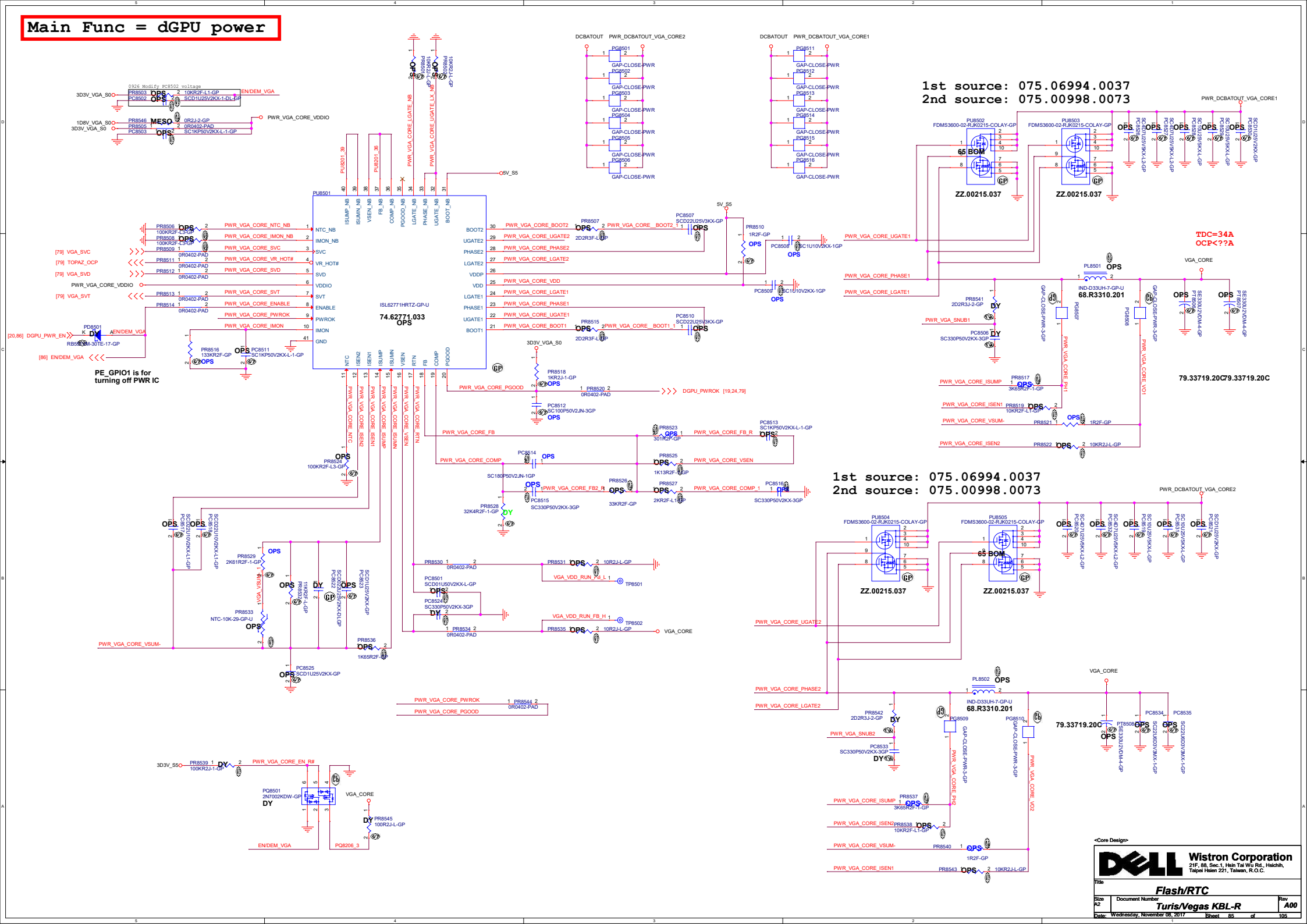
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: A2 | Document Number: Vegas SKL/KBL-R | Rev: A00

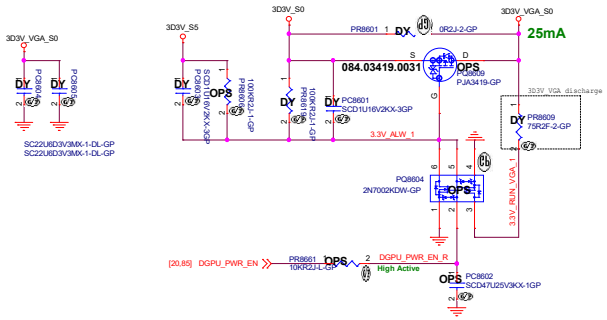
Date: Wednesday, November 08, 2017 | Sheet 81 of 105

Main Func = dGPU power



Main Func = dGPU

3D3V_S0 to 3D3V_VGA_S0 Transfer



GPU PWR Sequencing

3D3V_VGAS0

=> 0D95V_VGA_S0/1D8V_VGA_S0

=> 1D5V_VGA_S0

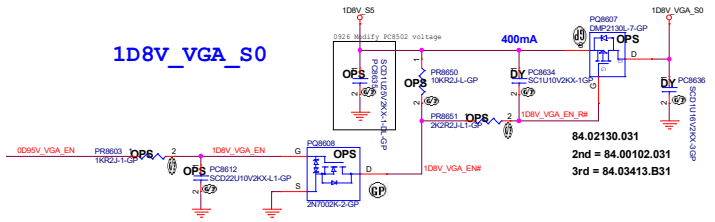
=> VGA_CORE

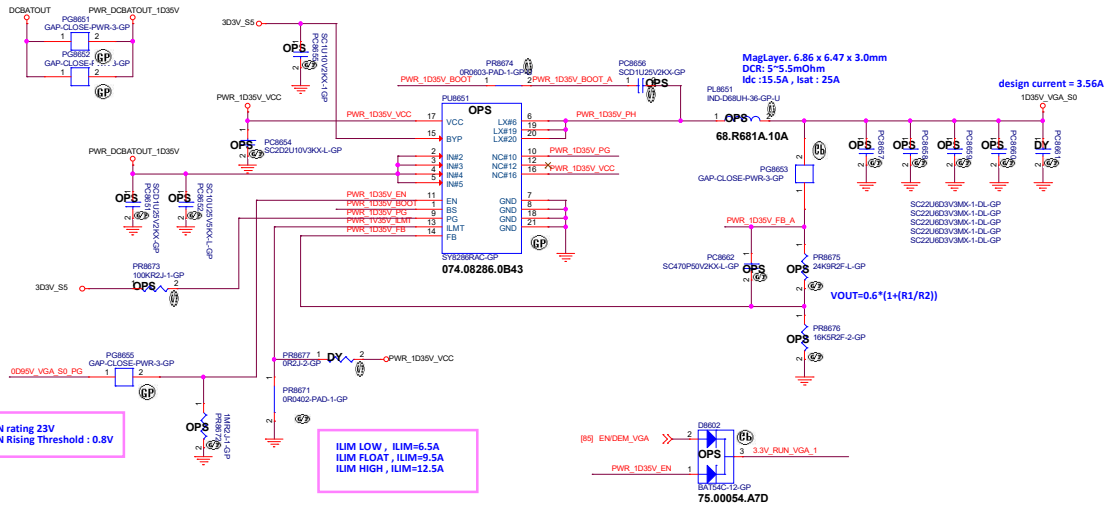
All the ASIC supplies must reach their respective nominal voltages withing 20ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.

It is recommended that the 3.3V rail ramp up first.

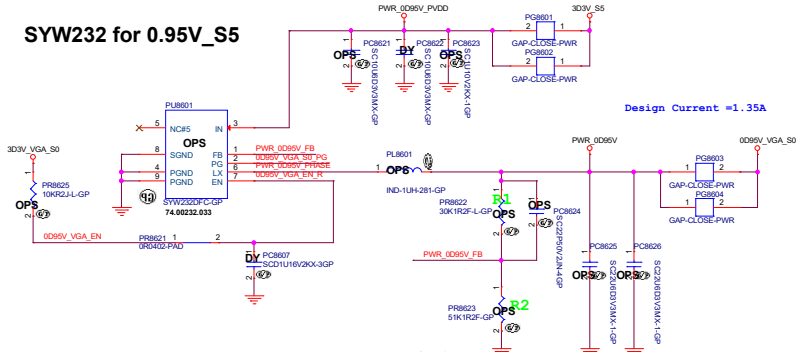
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.

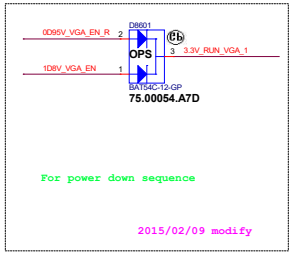
1D8V_VGA_S0

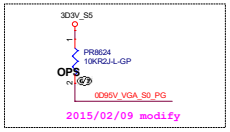




SYW232 for 0.95V_S5







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Title: **GPU Discrete Power**

Size: Custom | Document Number: **Vegas SKL/KBL-U** | Rev: **A00**

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Main Func = UnusedParts

H1 HOLE335R178-GP — ZZ.00PAD.7F1
H2 HOLE335R178-GP — ZZ.00PAD.7F1
H3 HOLE335R178-GP — ZZ.00PAD.7F1
H4 HOLE335R178-GP — ZZ.00PAD.7F1
H5 HOLE335R178-GP — ZZ.00PAD.7F1
H6 HOLE335R178-GP — ZZ.00PAD.7F1
H7 HOLE335R178-GP — ZZ.00PAD.7F1
H8 HOLE335R178-GP — ZZ.00PAD.7F1
H9 HOLE335R115-GP — ZZ.00PAD.D01
H10 HOLE335R115-GP — ZZ.00PAD.D01
H11 HT85B85X925R29-S-GP — ZZ.00PAD.D81
H12 HOLE335R115-GP — ZZ.00PAD.D01
H13 HOLE335R115-GP — ZZ.00PAD.D01
H14 HT85B85X925R29-S-GP — ZZ.00PAD.D81
H15 HOLE276R91-GP — ZZ.00PAD.CZ1
H16 HT85BE95R29-U-5-GP — ZZ.00PAD.D31
H17 HOLE384X421R115-GP — ZZ.SCREW.681

SPR1 SPRING-63-GP — Spring — 34.4Y806.001
SPR2 SPRING-63-GP — Spring — 34.4Y806.001
SPR3 SPRING-63-GP — Spring — 34.4Y806.001
SPR5 SPRING-63-GP — Spring — 34.4Y806.001
SPR4 SPRING-43-GP-U — Spring — 34.15J03.001

0502 Changed PN
HS1 STF237R128H128-3-GP — 34.4LO45.201
2nd = 34.4LO45.301

0512 Deleted HS2

DCBATOUT
0927 Change acoustic solution
1101 Change acoustic solution
DY PT8901 SE33U25VM-11-GP
OPS PT8902 ST100U25VDM-1-GP
For acoustic noice

Main Func = EMI & RF Capacitors

For RF solution DVT1 3/2

3D3V_S0 / 5V_S0 / +VCCGT
EC9702 EC9703 EC9704 EC9706 EC9707 EC9708
SC1U10V2KX-1GP
SCD1U25V2KX-GP

1D35V_VGA_S0
EC9727 EC9725 EC9726 EC9730 EC9728 EC9729 EC9731
SC1U10V2KX-1GP

AUD_AGND
EC9739 EC9744 EC9743 EC9745
SC1KP50V2KX-L-1-GP

VGA_CORE
EC9746 EC9750 EC9751 EC9752 EC9753
SCD1U25V2KX-GP

Mind the voltage rating of the caps.

DCBATOUT
EC9701 EC9702 EC9703 EC9704 EC9705 EC9706 EC9707 EC9708 EC9709 EC9710
SCD1U25V2KX-GP
SC1KP50V2KX-L-1-GP

0921 Uninstall
EC9712 EC9713 EC9715 EC9716 EC9717 EC9711 EC9714
SCD1U25V2KX-GP
SC1KP50V2KX-L-1-GP

1D2V_S3
0921 Uninstall
EC8901 EC8902 EC8903 EC8904 EC8905 EC8906 EC8907 EC8908 EC8909
EC8910 EC8911 EC8912 EC8913 EC8914 EC8915
SCD1U25V2KX-GP

3D3V_S5
0921 Install
EC8916 EC8917 EC8918 EC8919 EC8920 EC8921 EC8922 EC8923 EC8924 EC8925 EC8926 EC8927 EC8928
SCD1U25V2KX-GP

5V_S0
EC9718 EC9719 EC9720 EC9721 EC9722 EC9723 EC9724
SCD1U25V2KX-GP

3D3V_S0
EC9735 EC9736 EC9737 EC9738
SCD1U25V2KX-GP

5V_S5
EC9732 EC9733 EC9734
SCD1U25V2KX-GP

DCBATOUT
EC9741 EC9742 EC9747 EC9749 EC9740 EC9748
SCD1U25V2KX-GP
SC1KP50V2KX-L-1-GP

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Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Vegas SKL/KBL-U
Rev: A00
Date: Wednesday, November 08, 2017
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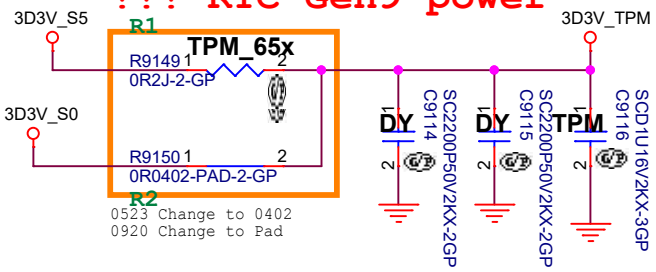
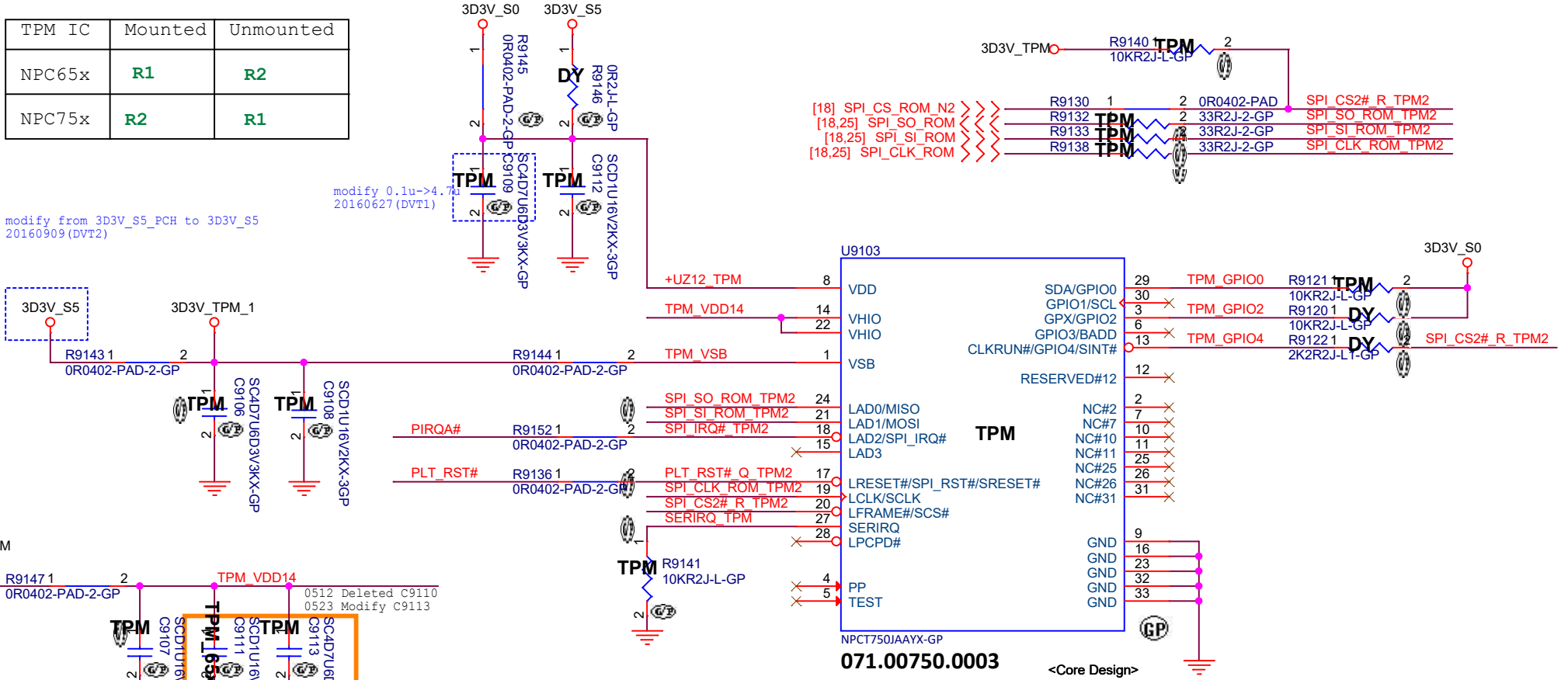
SSID = TPM

??? RTC Gen9 power



	NPCT650		NPCT750	
Pin define	Power Name	Power status	Power Name	Power status
Pin1	VSB	VALW	VSB	VALW
Pin8	VDD	VRUN	VHIO	VRUN (S0)
Pin14	VHIO	VSPI	NC	nc
Pin22	VHIO	VSPI	VHIO	VRUN (S0)

TPM IC	Mounted	Unmounted
NPC65x	R1	R2
NPC75x	R2	R1



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Title: **TPM**

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

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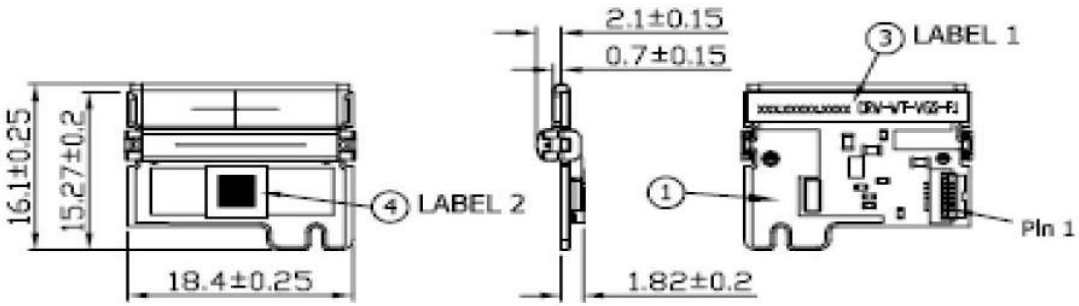
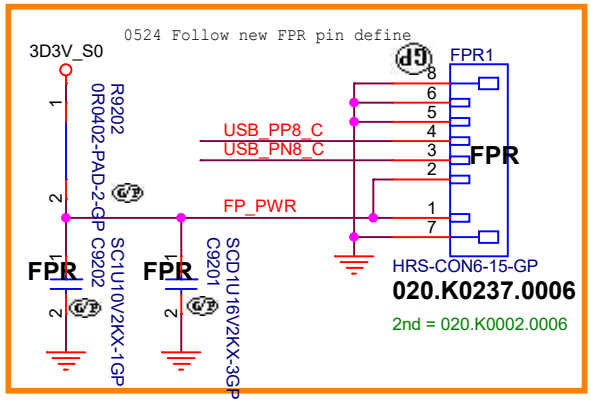
SSID = Finger Print

[16] USB_CPU_PN8 — R9203 1 — 2 0R0402-PAD-2-GP — USB_PN8_C

[16] USB_CPU_PP8 — R9204 1 — 2 0R0402-PAD-2-GP — USB_PP8_C

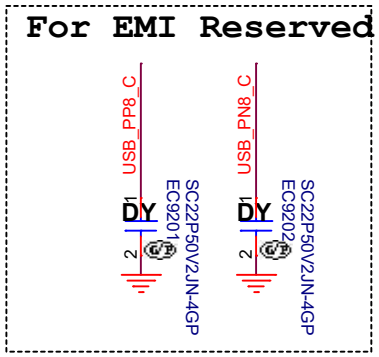




FingerPrint Pin Assignments.

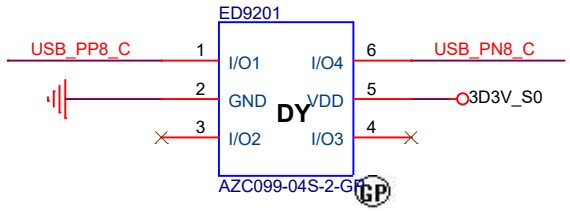
Pin 1 = 3.3Vin
Pin 2 = GND
Pin 3 = D-
Pin 4 = D+
Pin 5 = Reset_N
Pin 6 = GND

For EMI Reserved



Layout Note:

close to FPR1



075.09904.0A7C

AFTE14P-GP AFTP8902 — 1 FP_PWR
AFTE14P-GP AFTP8903 — 1 USB_PN8_C
AFTE14P-GP AFTP8904 — 1 USB_PP8_C

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Title: Finger Print		
Size: A4	Document Number: Vegas SKL/KBL-U	Rev: A00
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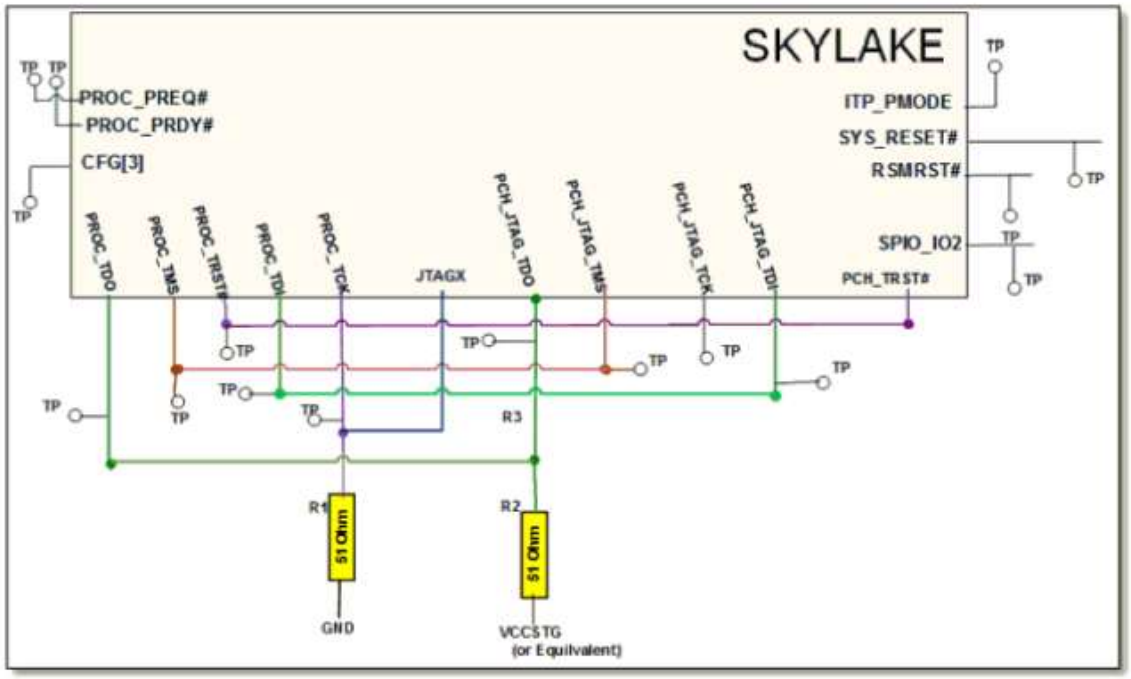
PCH_JTAG_TMS
XDP_TMS
test point

PCH_JTAG_TDI
XDP_TDI
test point

XDP_TCLK
XDP_TCK_JTAGX
test point

XDP_TDO_CPU
PCH_JTAG_TDO
test point



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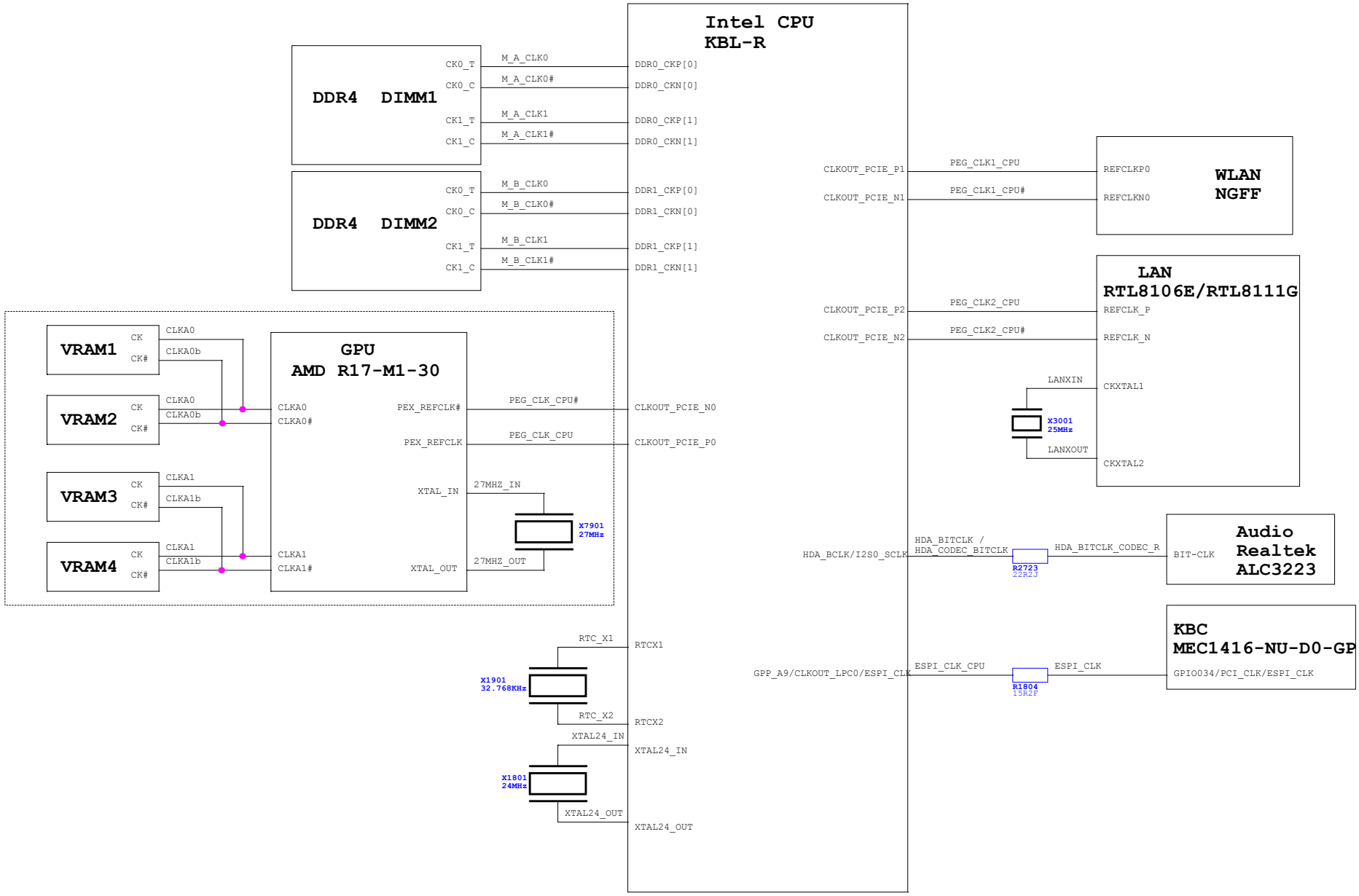
Title: ***Debug (XDP debug)***

Size	Document Number	Rev
A4	Vegas SKL/KBL-U	A00

Date: Wednesday, November 08, 2017 Sheet 99 of 105

CLK Block Diagram



<Core Design>

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Title: CLK Block Diagram

Size: A2 | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 100 of 105

Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

<Core Design>

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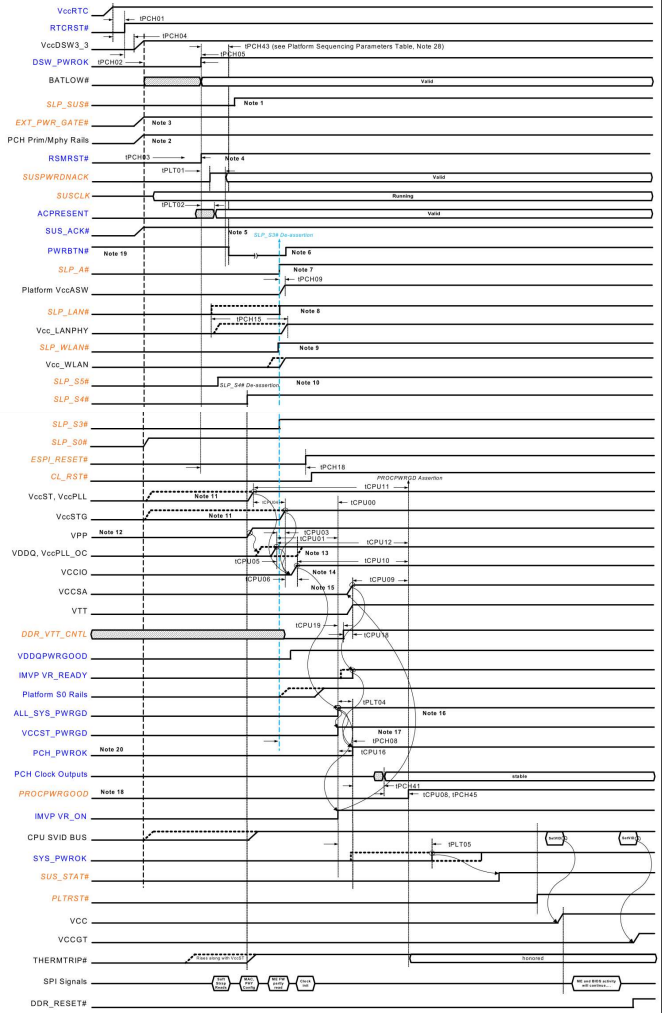
Title: ***Change History***

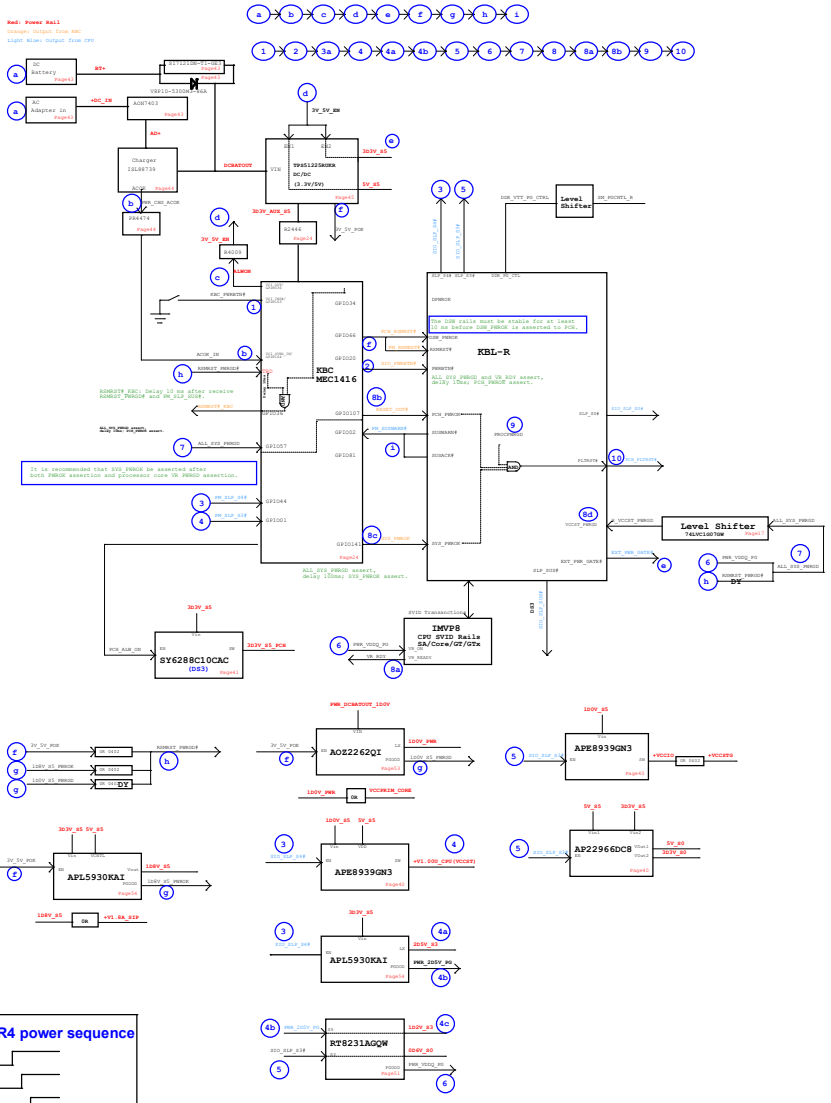
Size	Document Number	Rev
A3	*Vegas SKL/KBL-U*	*A00*

Date: Wednesday, November 08, 2017 Sheet 101 of 105

KBL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



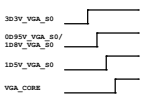
POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



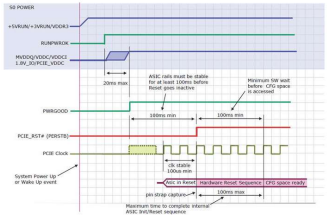
AMD GPU Power sequence

3D3V_VGAS0
=> 0D95V_VGA_S0/1D8V_VGA_S0
=> 1D5V_VGA_S0
=> VGA_CORE

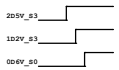
20ms
All the ASIC supplies must reach their respective nominal voltages within of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50mV/us.
It is recommended that the 3.3V rail ramp up first.
It is recommended that the 0.95V rail reach at least 90% of its normal value no later than 2ms from the start of VDDC ramping up.



POWER UP RESET SEQUENCE – COLD BOOT



For DDR4 power sequence



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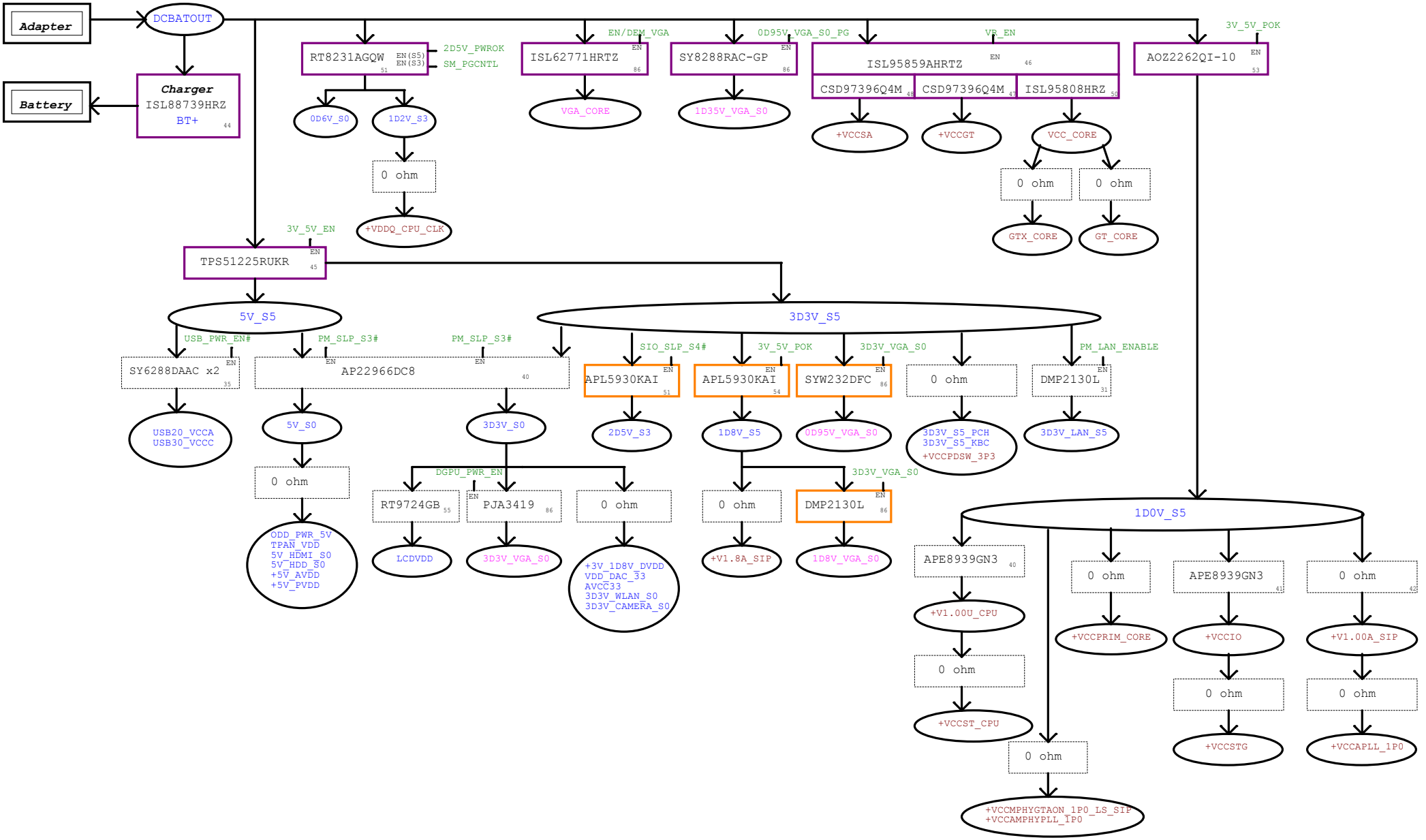
Power Sequence

Vegas SKL/KBL-U

Size: A3



Power Shape

Regulator | LDO | Switch

<Core Design>

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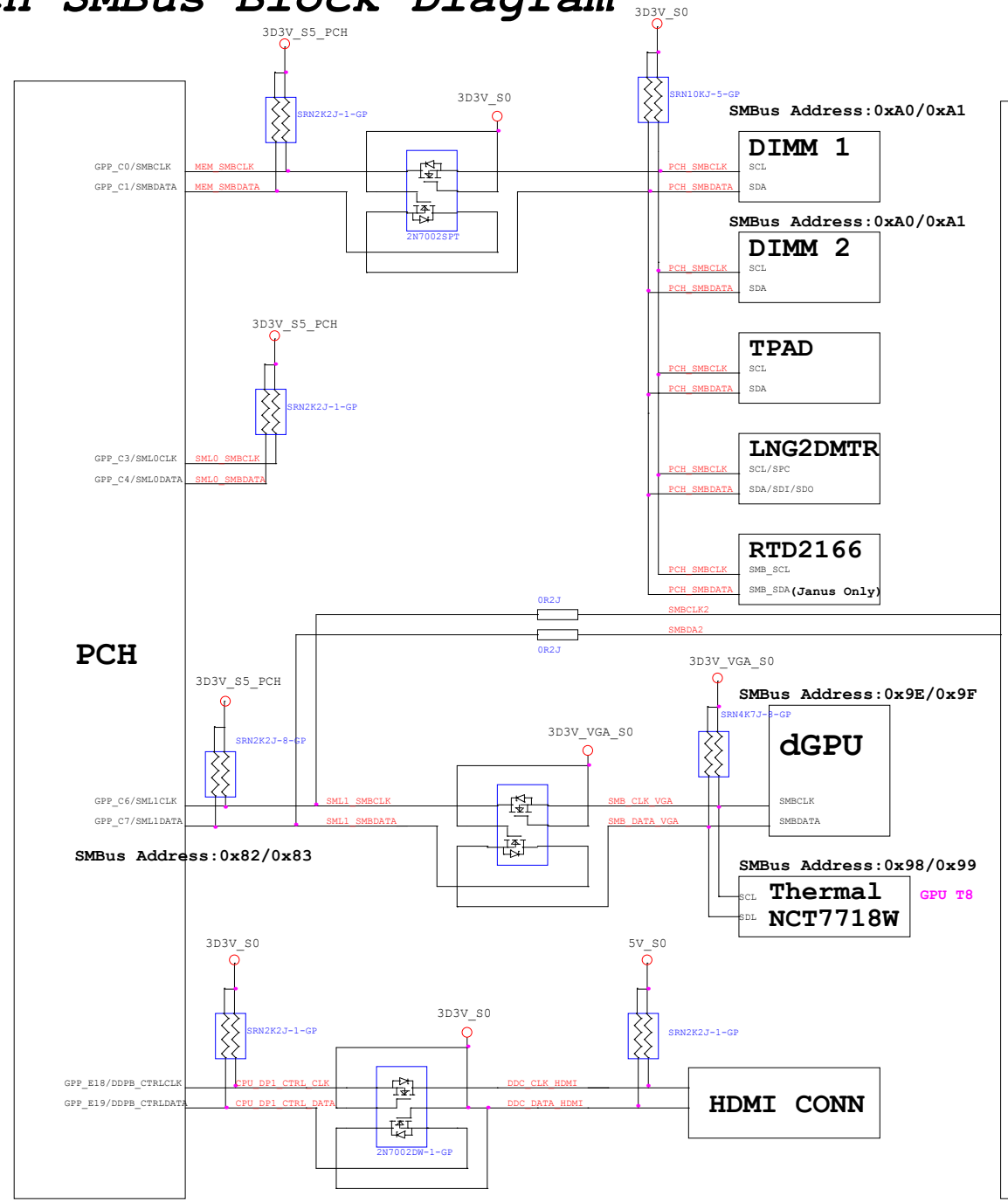
Title: Power Block Diagram

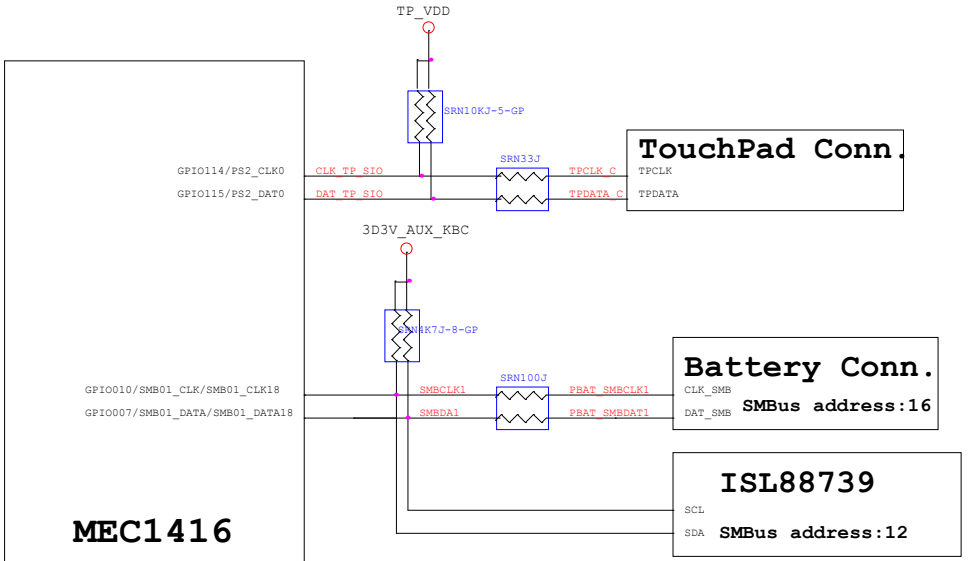
Size: Custom | Document Number: Vegas SKL/KBL-U | Rev: A00

Date: Wednesday, November 08, 2017 | Sheet 103 of 105

PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>

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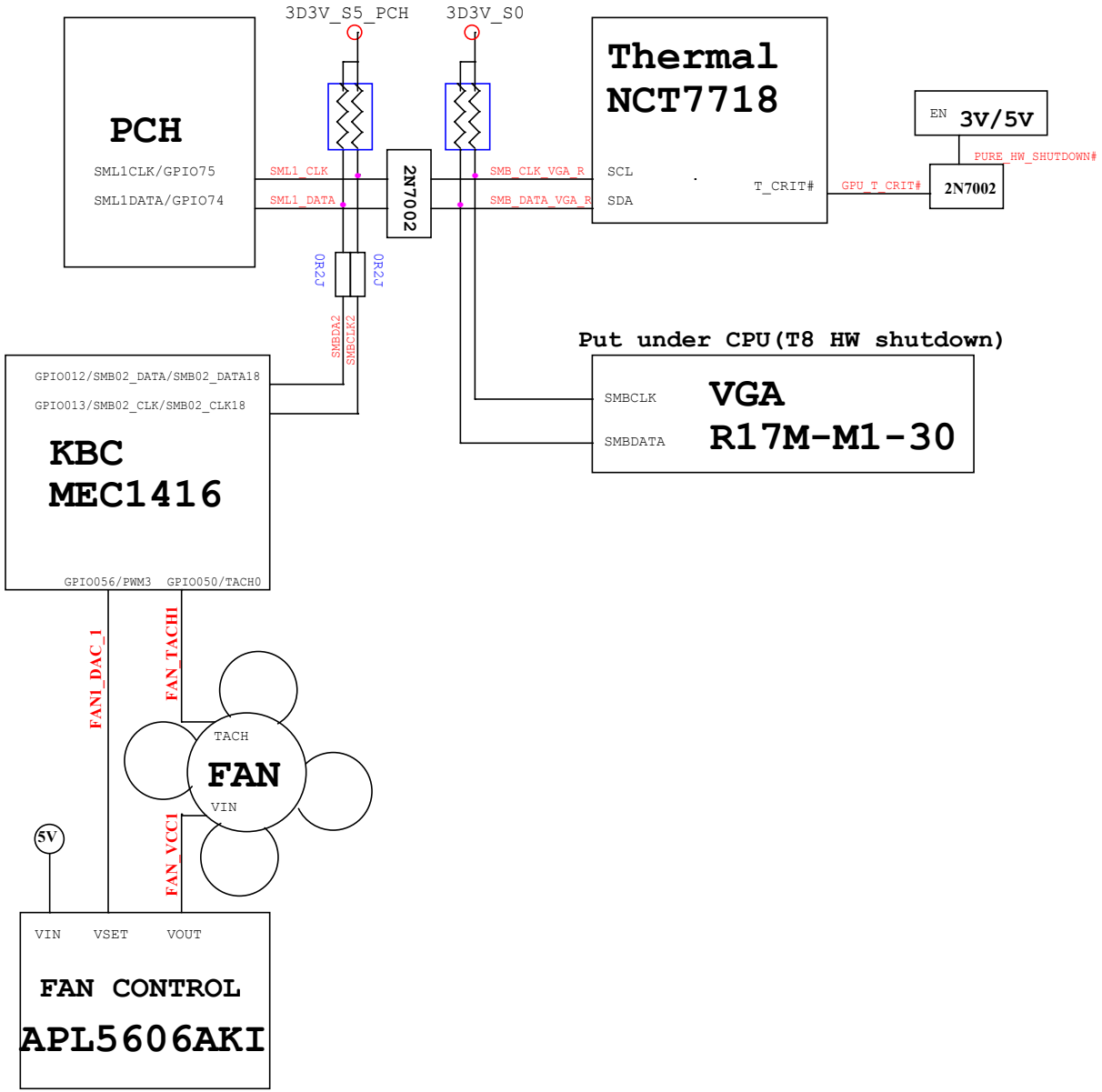
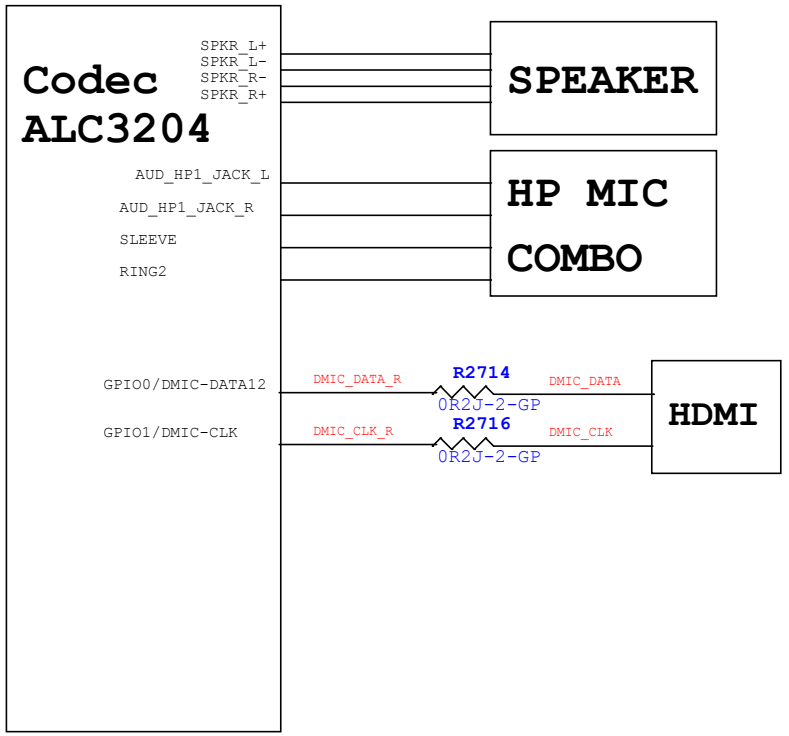
Taipei Hsien 221, Taiwan, R.O.C.

Title	SMBUS Block Diagram	
Size: Custom	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 104 of 105	

Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: Vegas SKL/KBL-U	Rev: A00
Date: Wednesday, November 08, 2017	Sheet 105 of 105	