Compal Confidential

B5W11 MB Schematic Document

LA-E061P

Rev: 1.0

2016.07.18

Security Classification	Compal Secret Data		
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HDMI Conn.

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eDP

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Fan Control page 31

Interleaved Memory

page 19

260pin DDR4-SO-DIMM X2

page 20

Memory BUS

Dual Channel

1.2V DDR4 1866/2133

eDP

DDI2

HDMI x 4 lanes

DDI

Intel Kabylake U

Kabylake U
Kabylake PCH-LP(MCP)
(KBL-U_2+2)

Processor

Dual Core + GT2

15W
1356pin BGA
page 07~18

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NGFF
WLAN
USB port 5

PCIe 1.0
2.5GT/s
port 6

LAN(GbE)

Flexible IO

USB 3.0
conn x1
USB port 1

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USB 2.0
conn x2
USB port2,3
Port3 on Sub/B

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CMOS
Camera
USB port 7

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Card Reader
RTS5170
SD only
USB port 8
on Sub/B

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USBx8 48MHz

HD Audio 3.3V 24MHz

PCIe 1.0
2.5GT/s
port 5

SATA3.0
6.0 Gb/s
port 7
(SATA0)

SATA3.0
6.0 Gb/s
port 8
(SATA1)

LAN(GbE)
Realtek 8111H
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RJ45 conn.

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SATA HDD
Conn.

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SATA CDROM
Conn.

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SPI

SPI ROM
64Mb page 9

HDA Codec
ALC233 page 25

Touch
Screen
I2C (PORT1)
USB port 6
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Int. Speaker
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Int. AMIC
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UAJ
on Sub/B
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LPC/eSPI BUS

CLK=24MHz

ENE
KB9022
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RTC CKT.
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Power On/Off CKT.
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DC/DC Interface CKT.
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Power Circuit DC/DC
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Sub Board

LS-D671
IO/B
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Int.KBD

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Touch Pad
PS2 (from EC) / I2C (from SOC)

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Title: Block Diagrams

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Board ID Table for AD channel

Vcc	3.3V +/- 5%
Ra	100K +/- 1%

Board ID	Rb	VBID min	VBID typ	VBID max	EC AD3	PCB Revision
0	0	0 V	0 V	0.300 V	0x00 - 0x13	0.1
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	0.1
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	

Power State

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Voltage Rails

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON

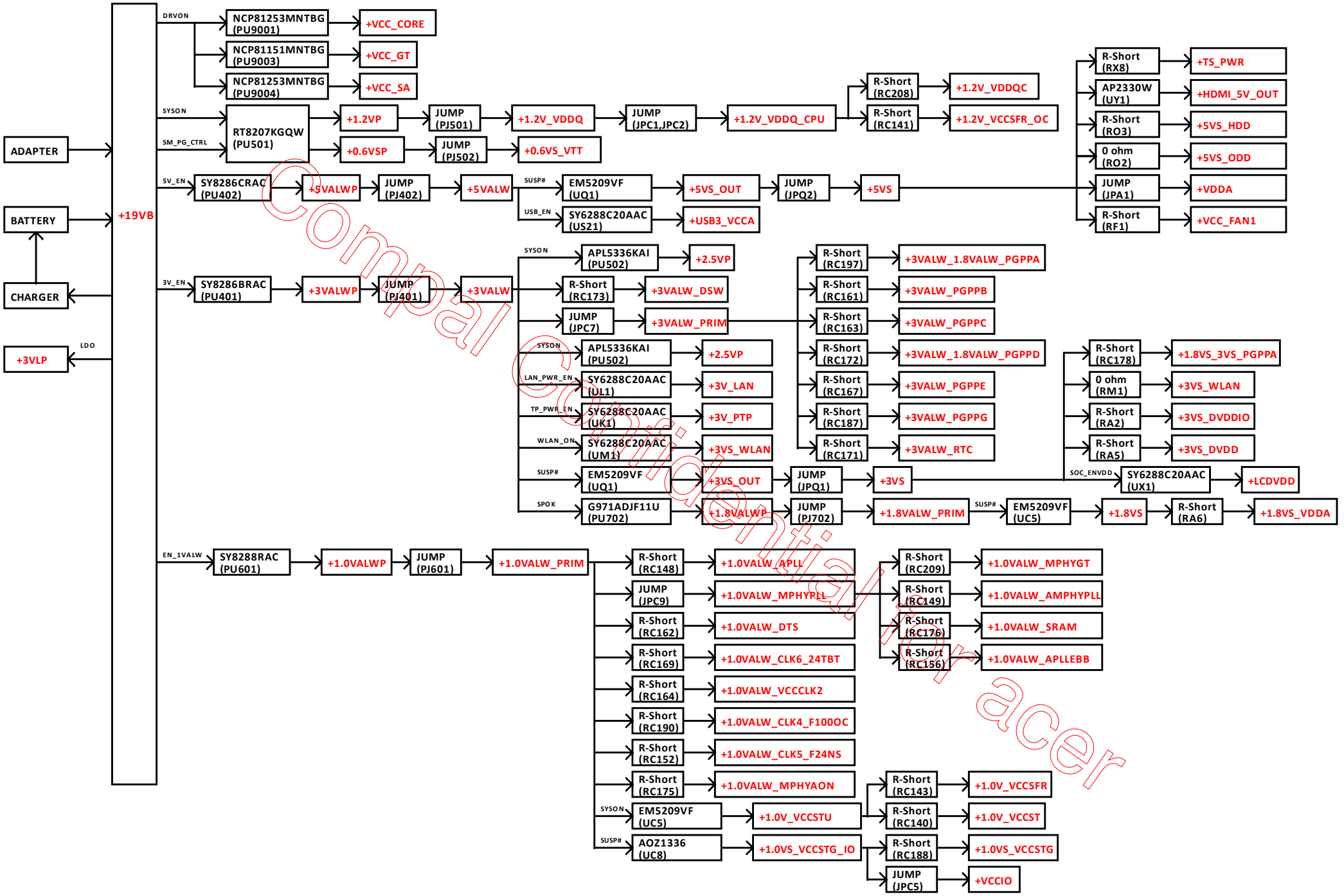
Note : ON*1 means power plane is ON only when WOL enable and RTC wake at BIOS setting, otherwise it is OFF.

BOM Structure Table

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@		
Connector	CONN@		
For Acer BYOC	BYOC@	SkyLake platform	SKL@
No Acer BYOC	NBYOC@	KabyLake platform	KBL@
CODEC(ALC255)	255@		
CODEC(ALC233)	233@		
LPC MODE for EC	LPC@		
ESPI MODE for EC	ESPI@		
For Intel CMC	CMC@		
EMI requirement	EMI@		
EMI requirement depop	@EMI@		
ESD requirement	ESD@		
ESD requirement depop	@ESD@	CPU Code	QKJW@
LAN(8111GUS)	8111GUS@		
LAN(8111H)	8111H@		
RF requirement	RF@		

43 level BOM table

43 Level	Description	BOM Structure
431A3EBOL01	SMT MB AE061 B5W11 QKJW HDMI	



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.		
Title: Power Rail		
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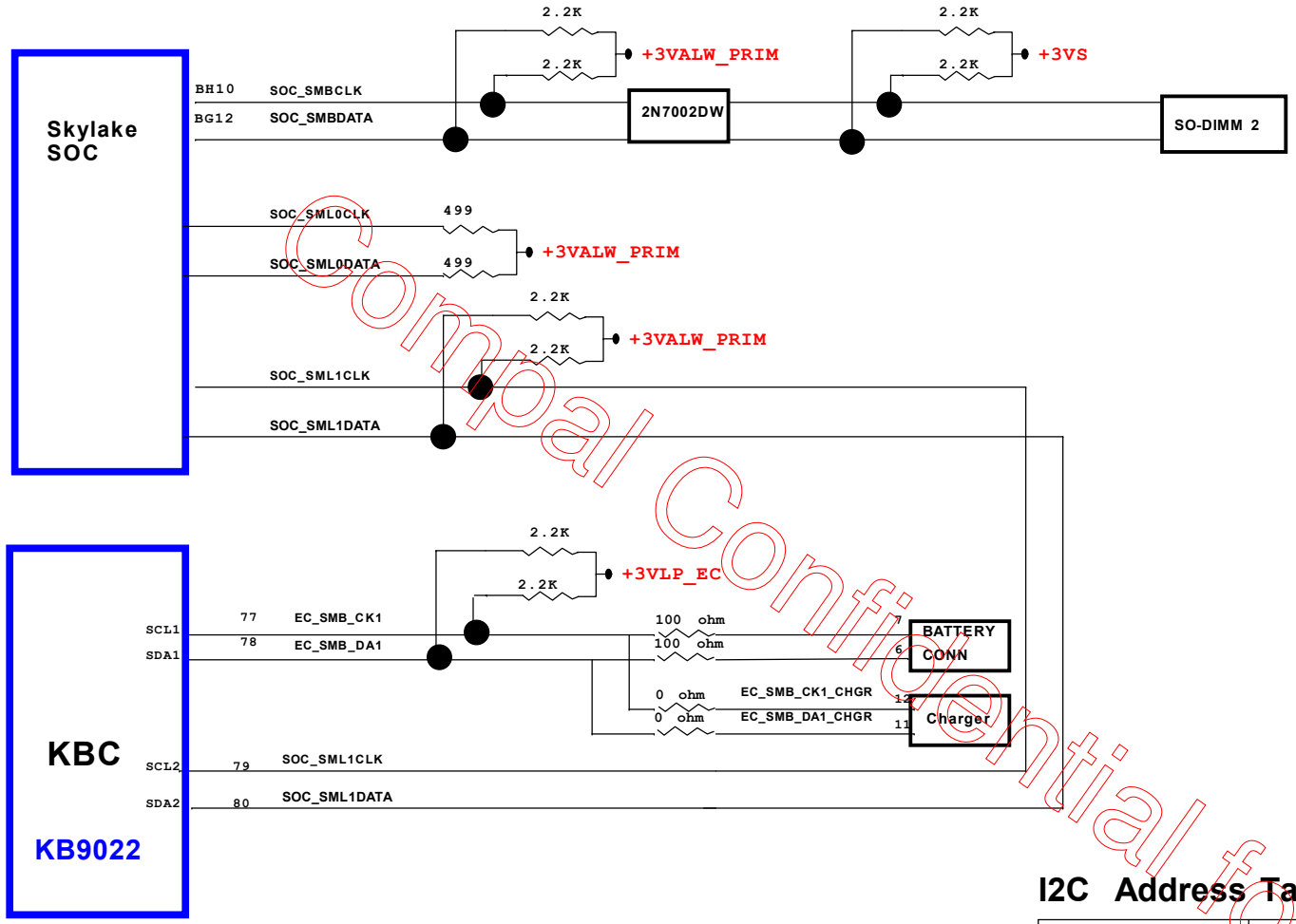

Need check

I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit) Write	Address(8bit) Read
I2C_0 (+3VS)	Reserved (Touch Panel)			
I2C_1 (+3VS)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x15		
SOC_SMBCLK +3VS	DIMM2	0xA4		
SOC_SML1CLK +3VALW_PRIM	PCH-LP (SOC)	0x90		
EC_SMB_CK1 +3VLP	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

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Title: SMBUS Routing Table

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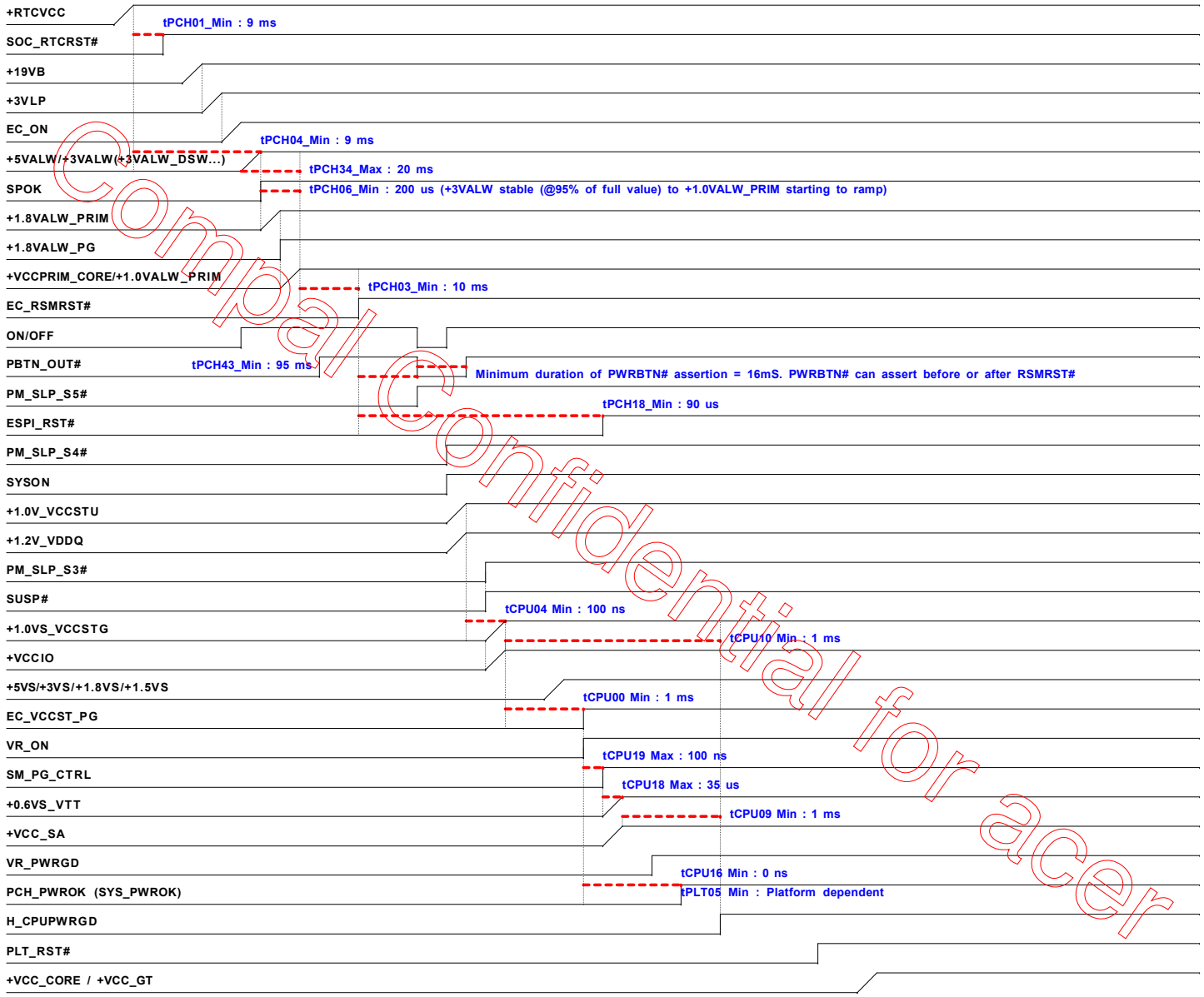
PWR Sequence_SKL-U2+2_DDR3L_Value_NON CS



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Title: Power Sequence			
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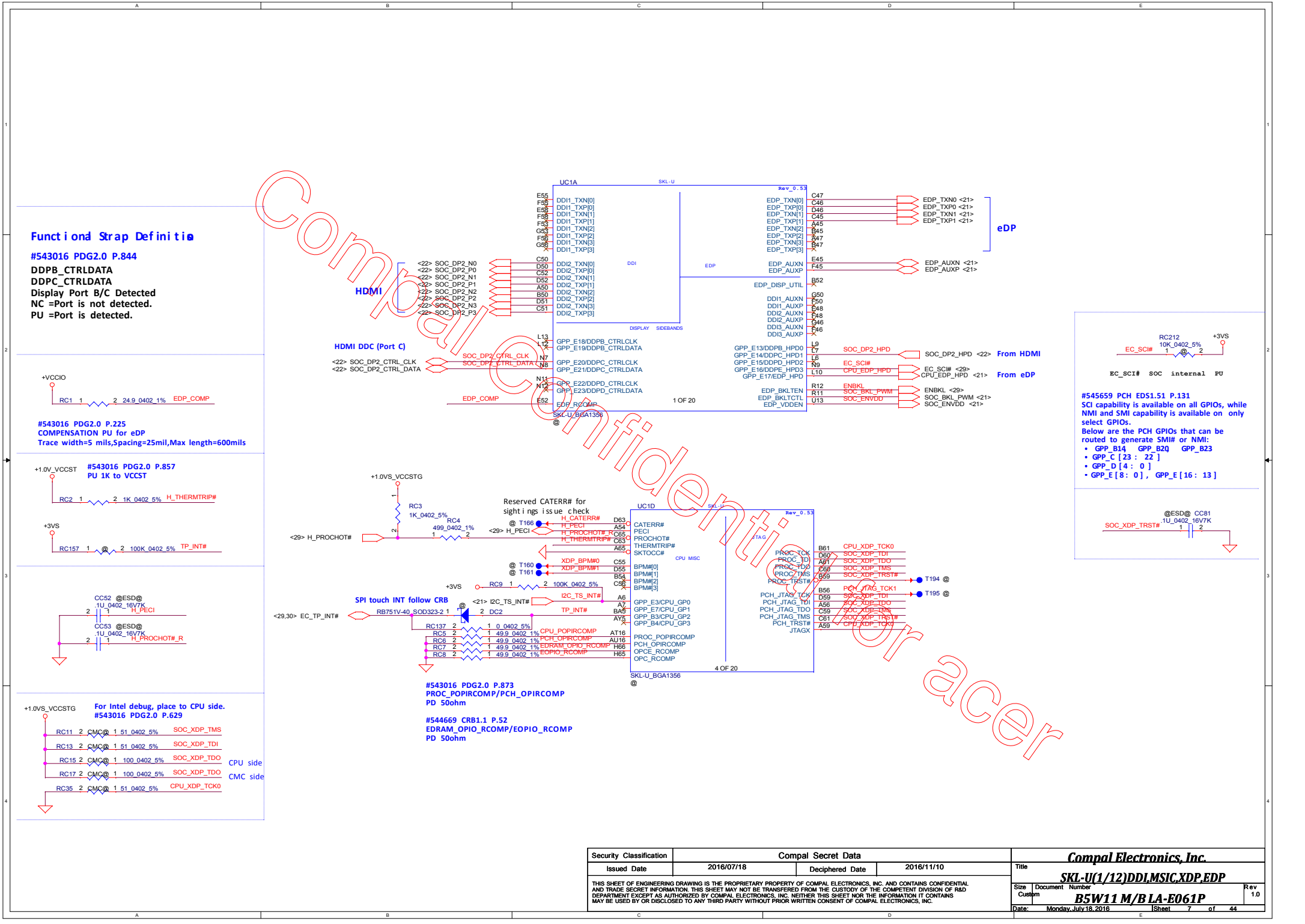

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Title: SKL-U(1/12)DDI,MSIC,XDP,EDP

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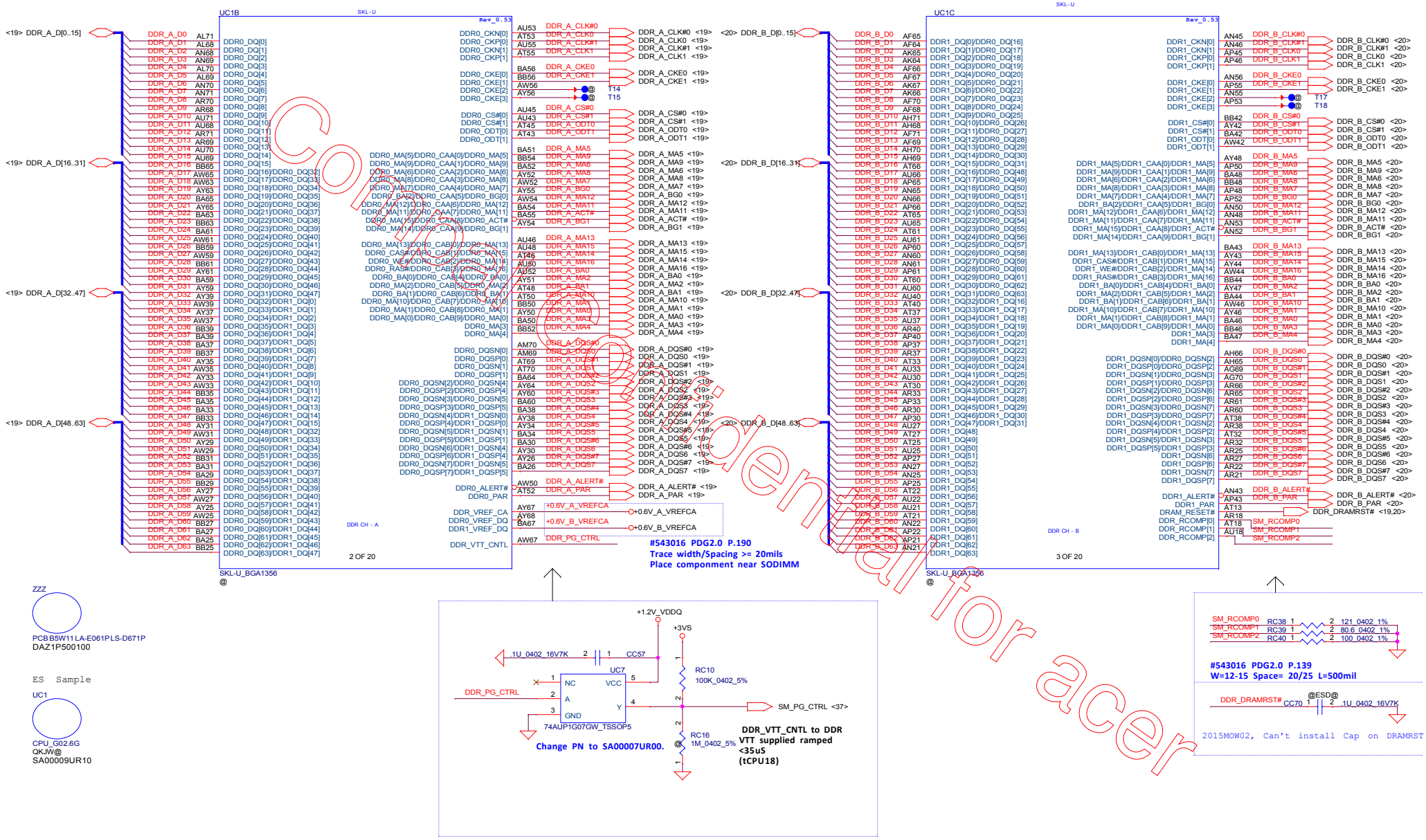
Interleaved Memory



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Compal Electronics, Inc.

Title: SKL-U(2/12)DDR4

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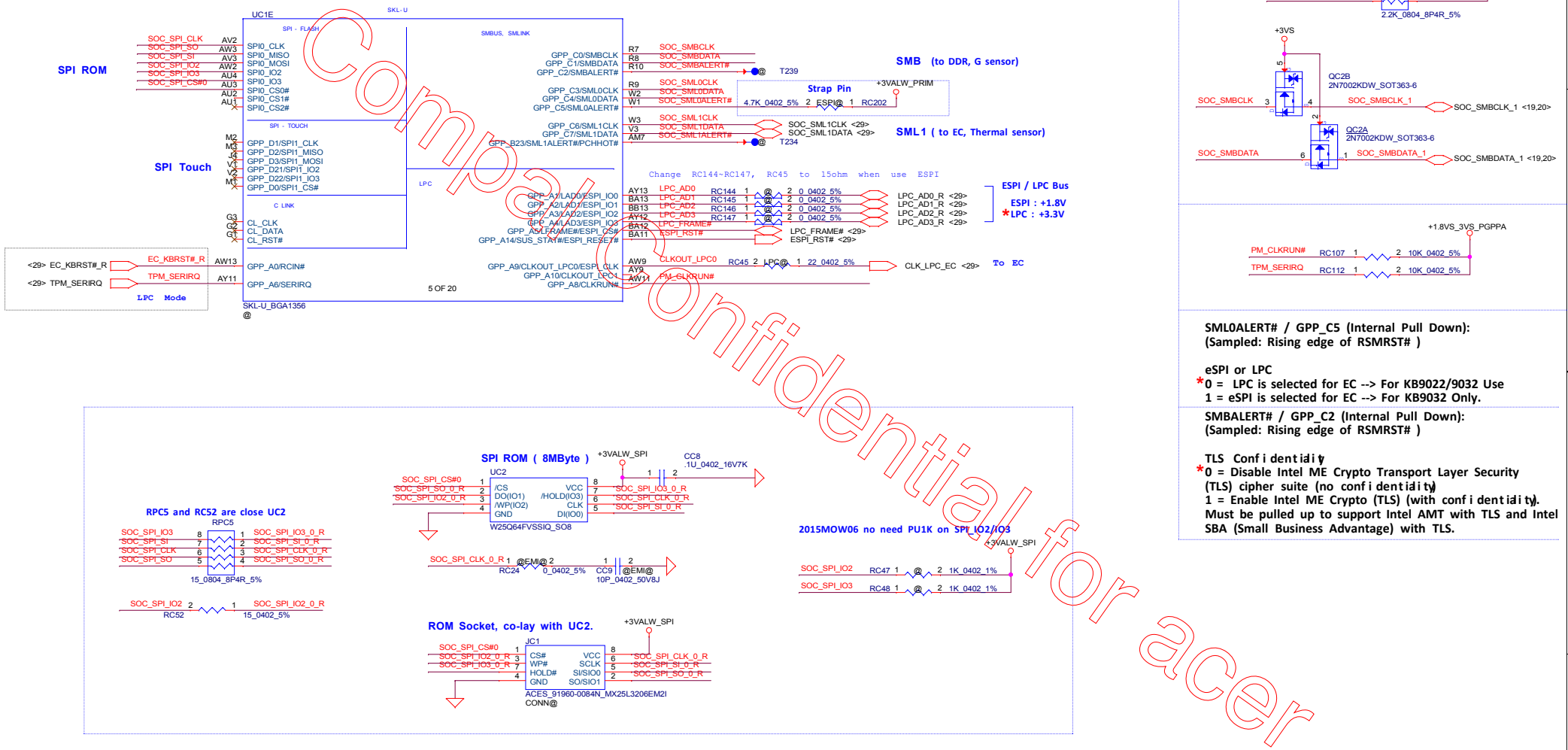

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Compal Electronics, Inc.			
Title: SKL-U(3/12)SPI,ESPI,SMB,LPC			
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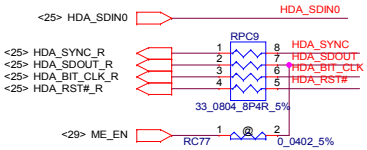
HDA for AUDIO



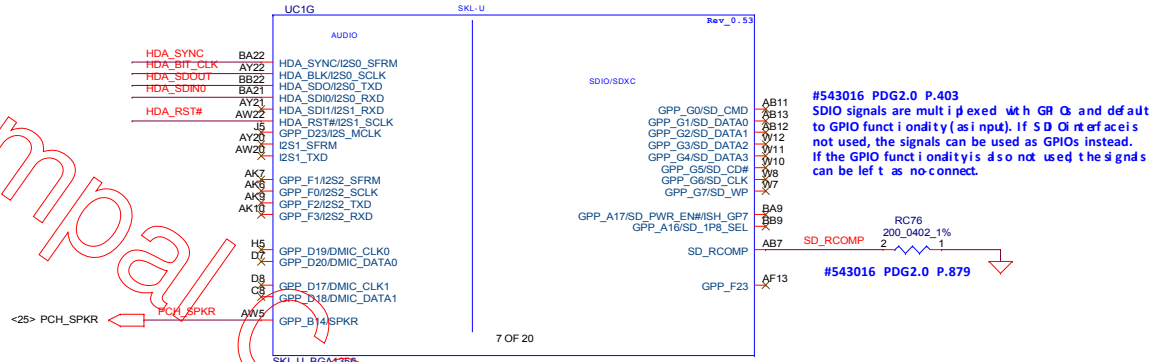
HDA_SDO / I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external

pull-up in manufacturing/debug environments ONLY.

SPKR / GPP_B14 (Internal Pull Down):
(Sampled:Rising edge of PCH_PWROK)

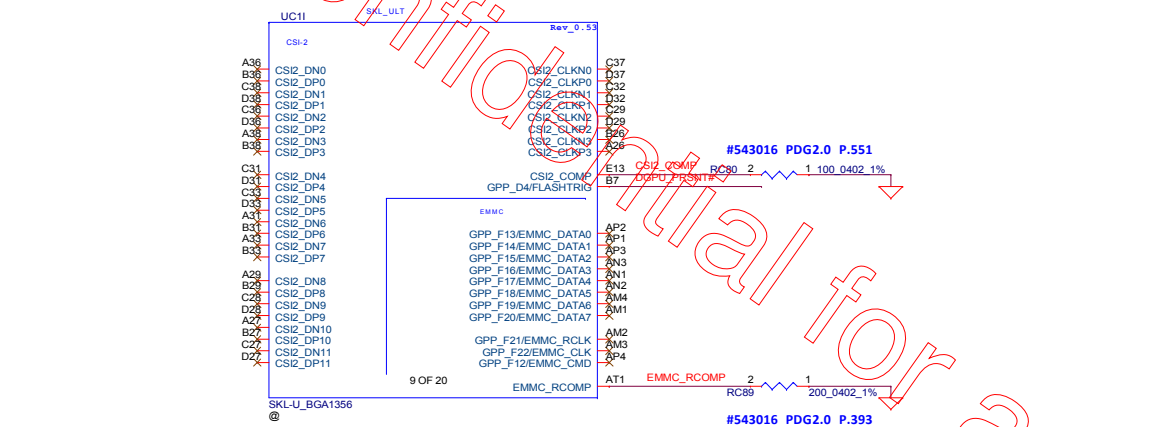
TOP Swap Override
*** 0 = Disable TOP Swap mode.**
1 = Enable TOP Swap Mode.

Intel HD Audio link capabilities
> Two SDI signals to support two external codecs.
> Drivers variable requency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
-- SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.



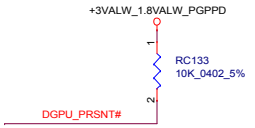
#543016 PDG2.0 P.403
SDIO signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDIO interface is not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used, the signals can be left as no-connect.

#543016 PDG2.0 P.879



#543016 PDG2.0 P.551

#543016 PDG2.0 P.393



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Compal Electronics, Inc.			
Title	SKL-U(4/12)HDA,EMMC,SDIO,CSI2		
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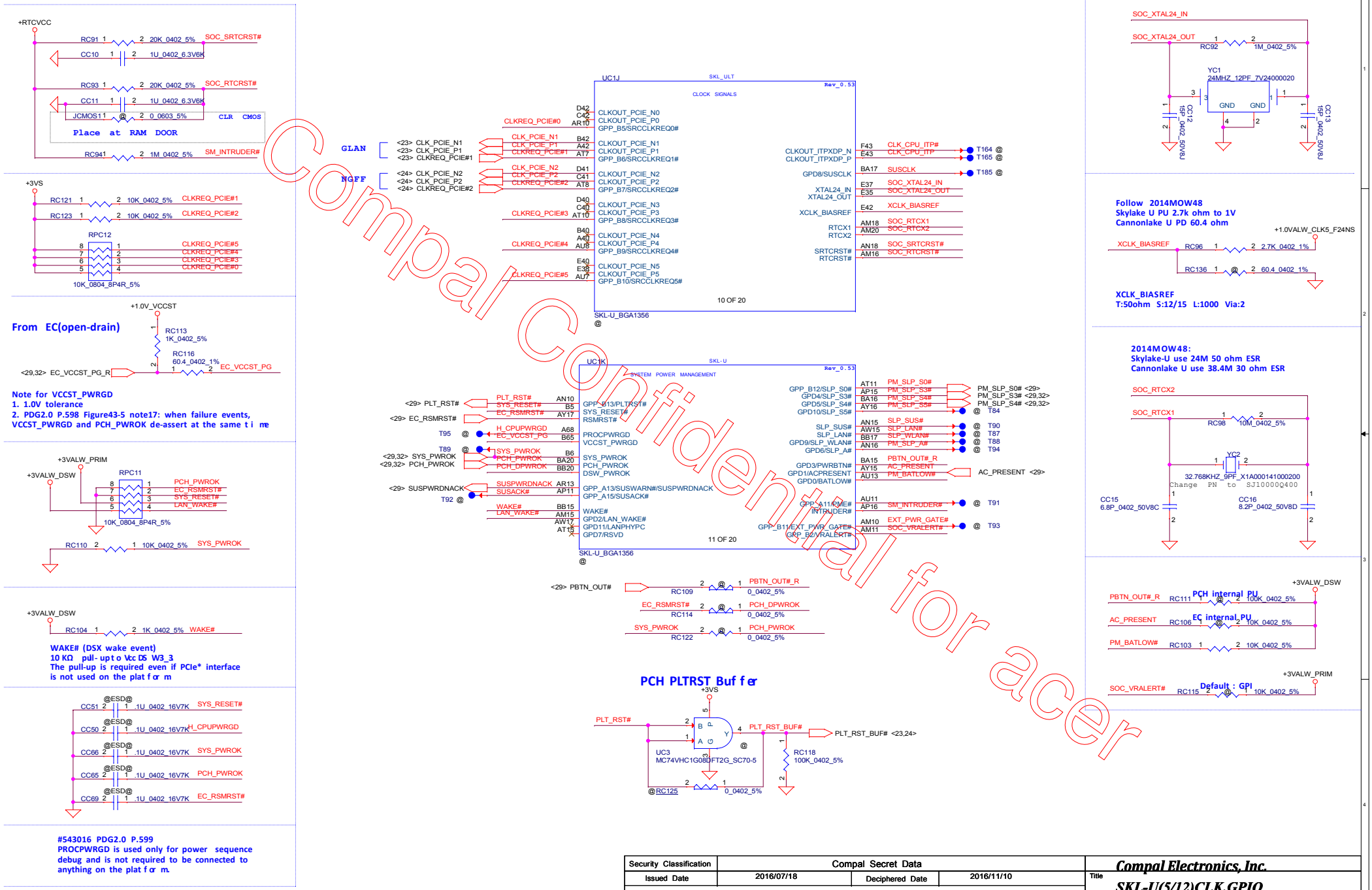

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Compal Electronics, Inc.			
Title	SKL-U(5/12)CLK,GPIO		
Size	Document Number		Rev
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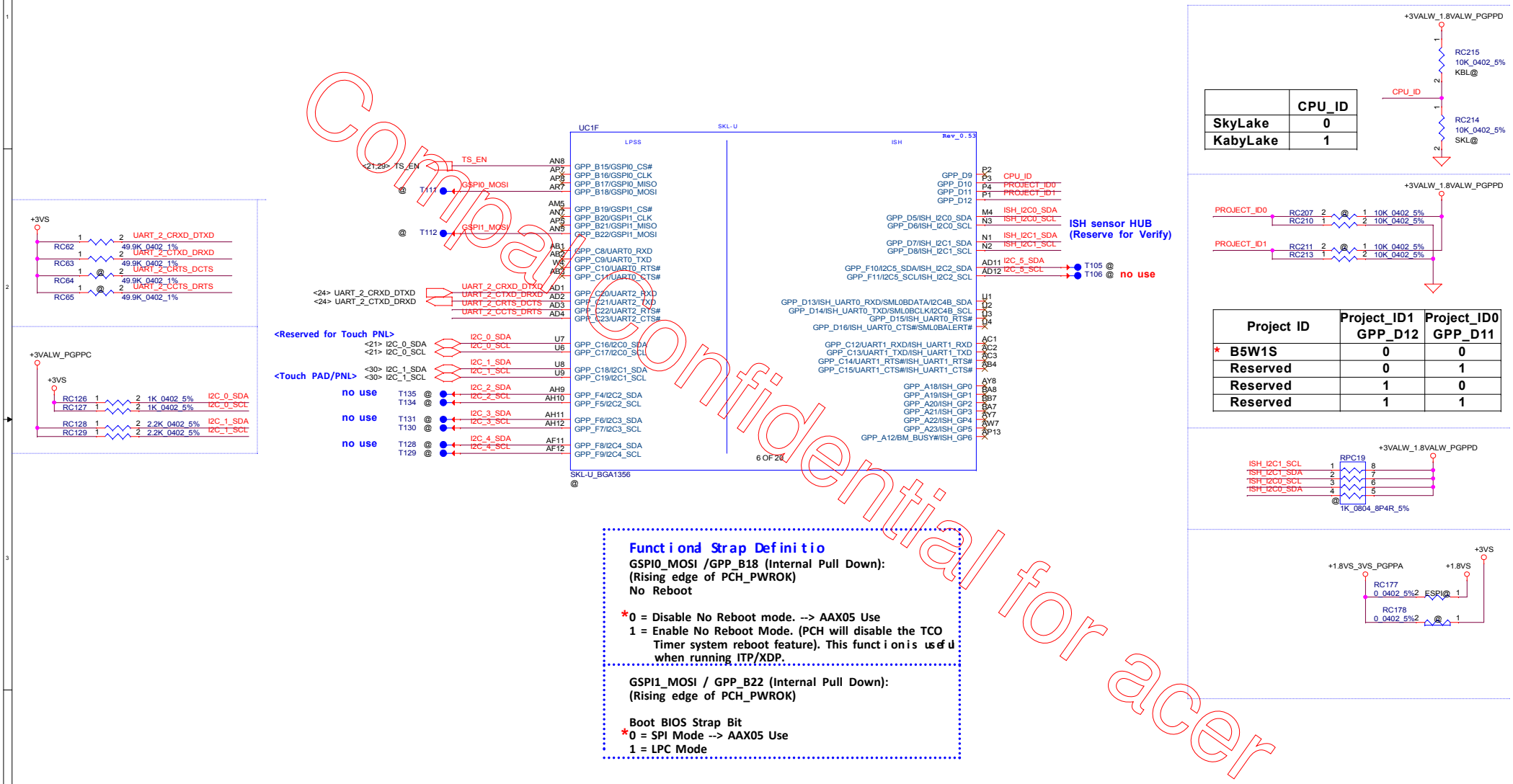

	CPU_ID
SkyLake	0
KabyLake	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* B5W1S	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

Functiond Strap Definitio

GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

*0 = Disable No Reboot mode. --> AAX05 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This functi onis usefu when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
*0 = SPI Mode --> AAX05 Use
1 = LPC Mode

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Title: SKL-U(6/12)GPIO

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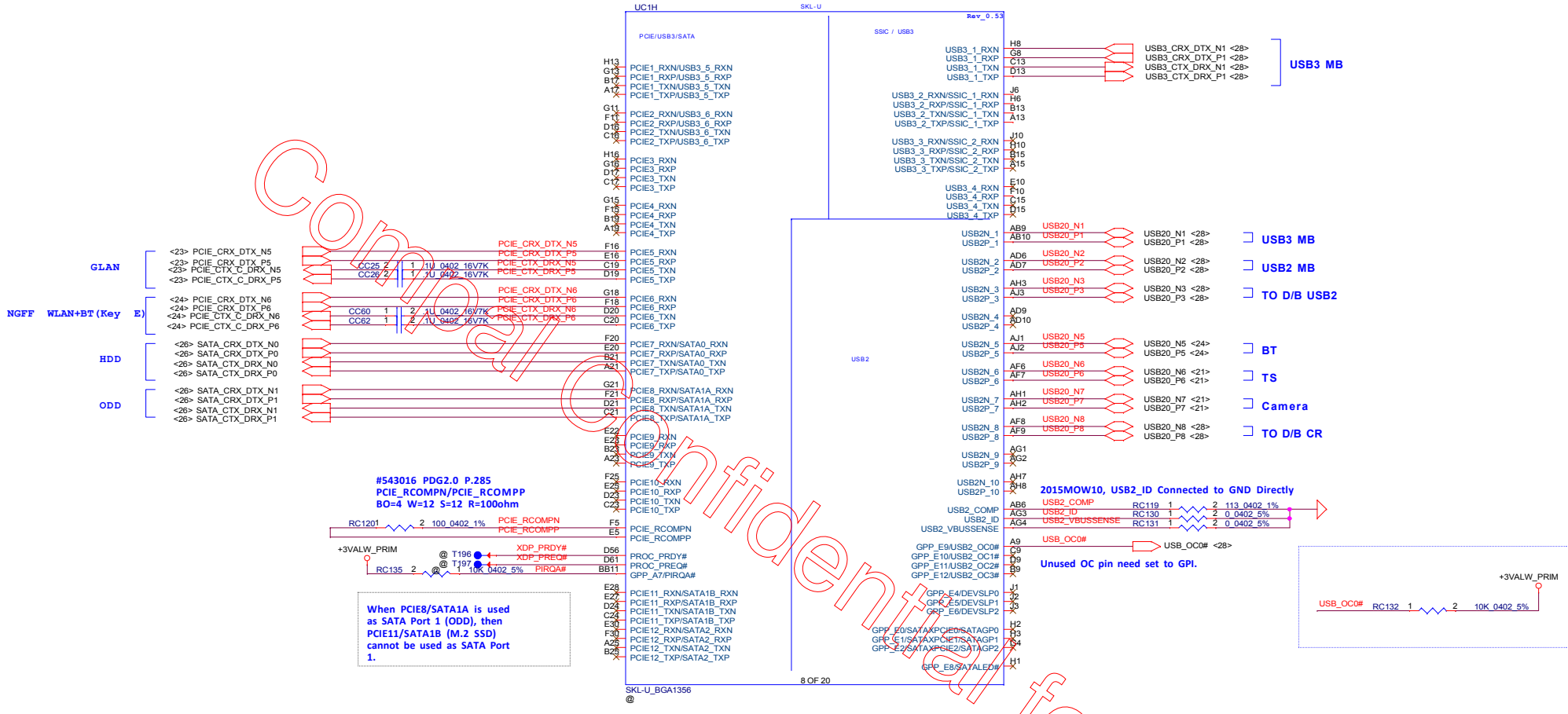

GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation

DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.

The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.

- When high, DEVSLP requests the SATA device to enter into the DEVSLP power state
- When low, DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state

SATA General Purpose (SATAGP[2:0]) Signals

- The processor provides three SATA general purpose input signals, SATAGP[2:0] for SKL U

These signals can be configured as interlock switch inputs corresponding to a given SATA port.

- When used as an interlock switch status indication, this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.

If mechanical presence switches will not be used on the platform, SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

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Title: SKL-U(7/12)PCIE,USB,SATA

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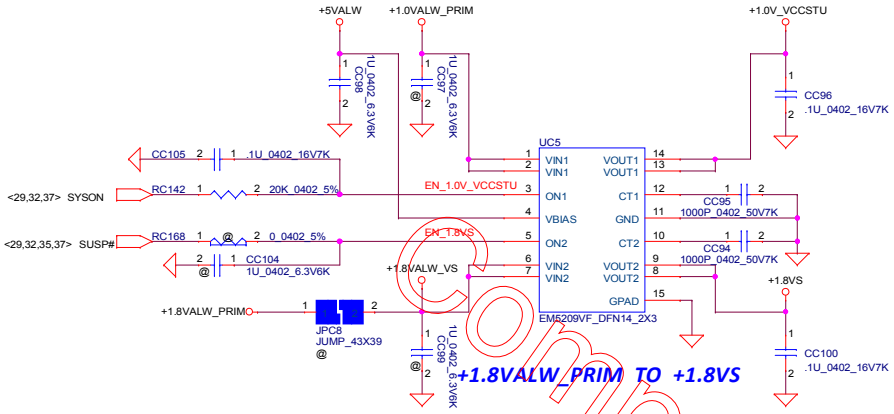
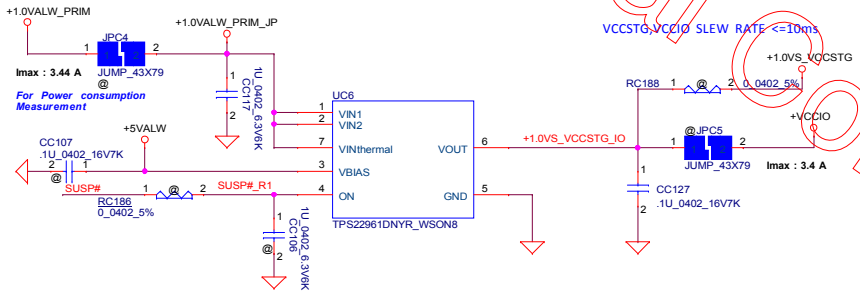
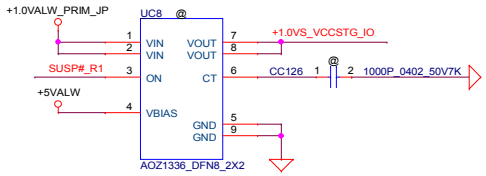
+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

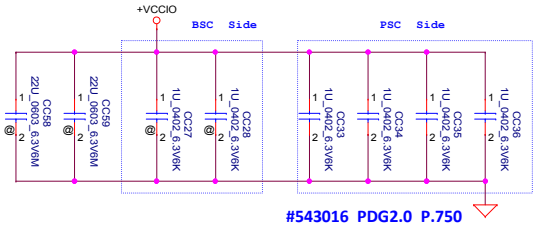


+1.8VALW_PRIM TO +1.8VS

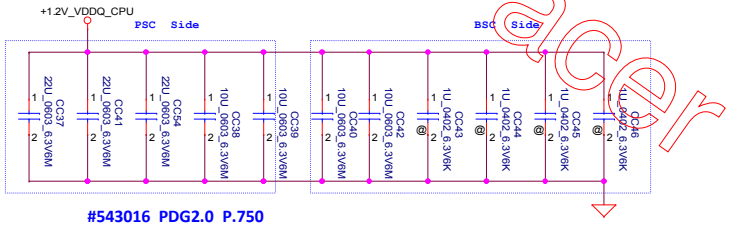
+1.0VALW_PRIM TO +1.0VS_VCCSTG



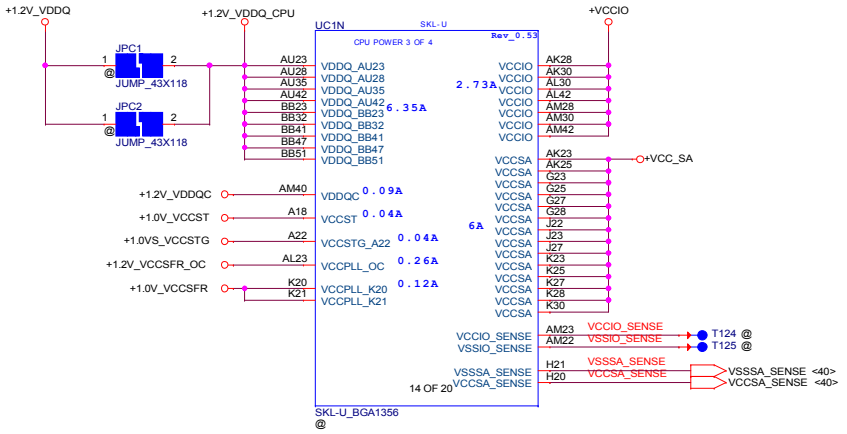


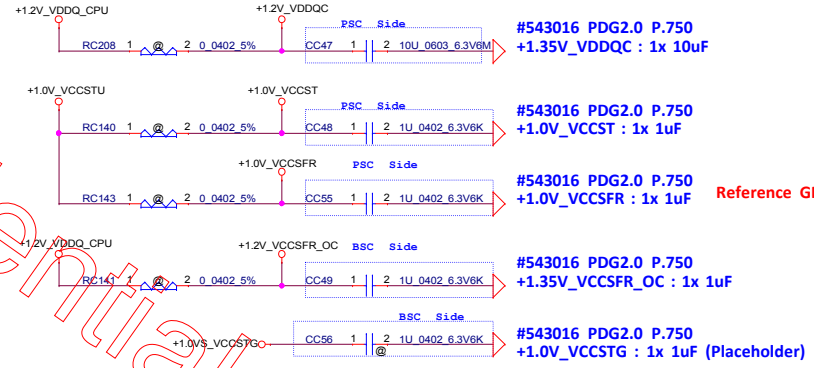


#543016 PDG2.0 P.750
+VCCIO : 4x 1uF 0402



#543016 PDG2.0 P.750
+1.35V_VDDQ_CPU :
4x 10uF 0402
3x 22uF 0603





#543016 PDG2.0 P.750
+1.35V_VDDQC : 1x 10uF

#543016 PDG2.0 P.750
+1.0V_VCCST : 1x 1uF

#543016 PDG2.0 P.750
+1.0V_VCCSFR : 1x 1uF

Reference GND as possible.

#543016 PDG2.0 P.750
+1.35V_VCCSFR_OC : 1x 1uF

#543016 PDG2.0 P.750
+1.0V_VCCSTG : 1x 1uF (Placeholder)

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Compal Electronics, Inc.			
Title: SKL-U(8/12)Power			
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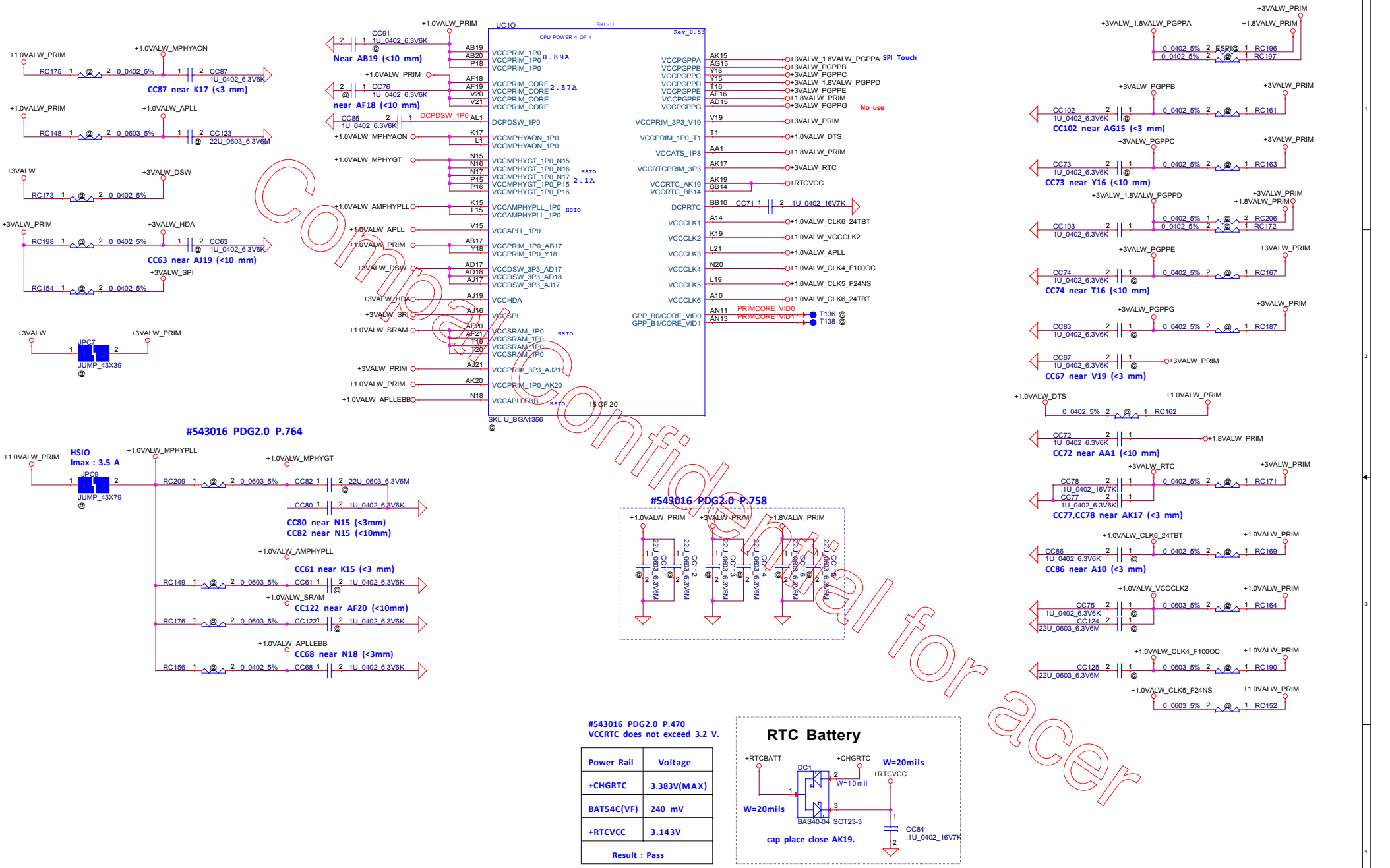

#543016 PDG2.0 P.470
VCCRTC does not exceed 3.2 V.

Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C(VF)	240 mV
+RTCVCC	3.143V
Result : Pass	

RTC Battery

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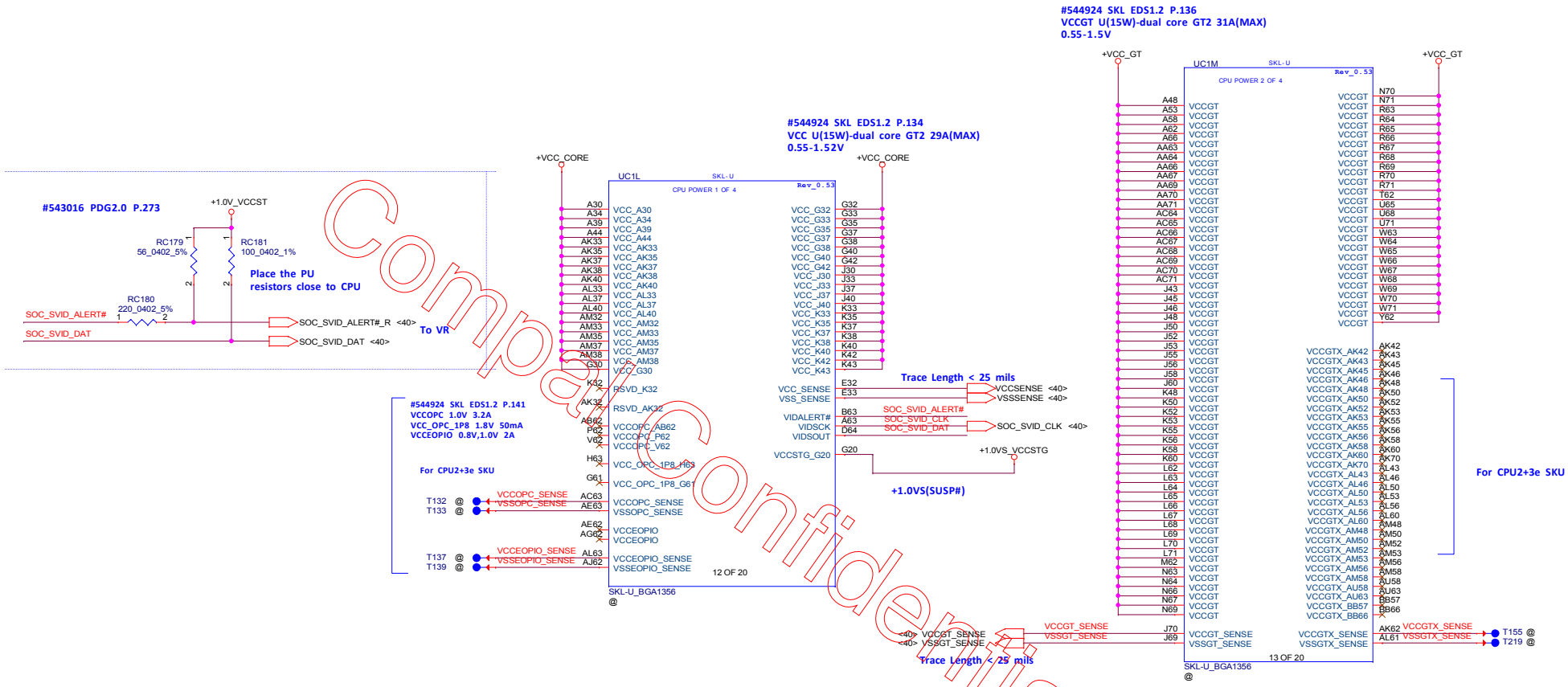


Processor Power Rails

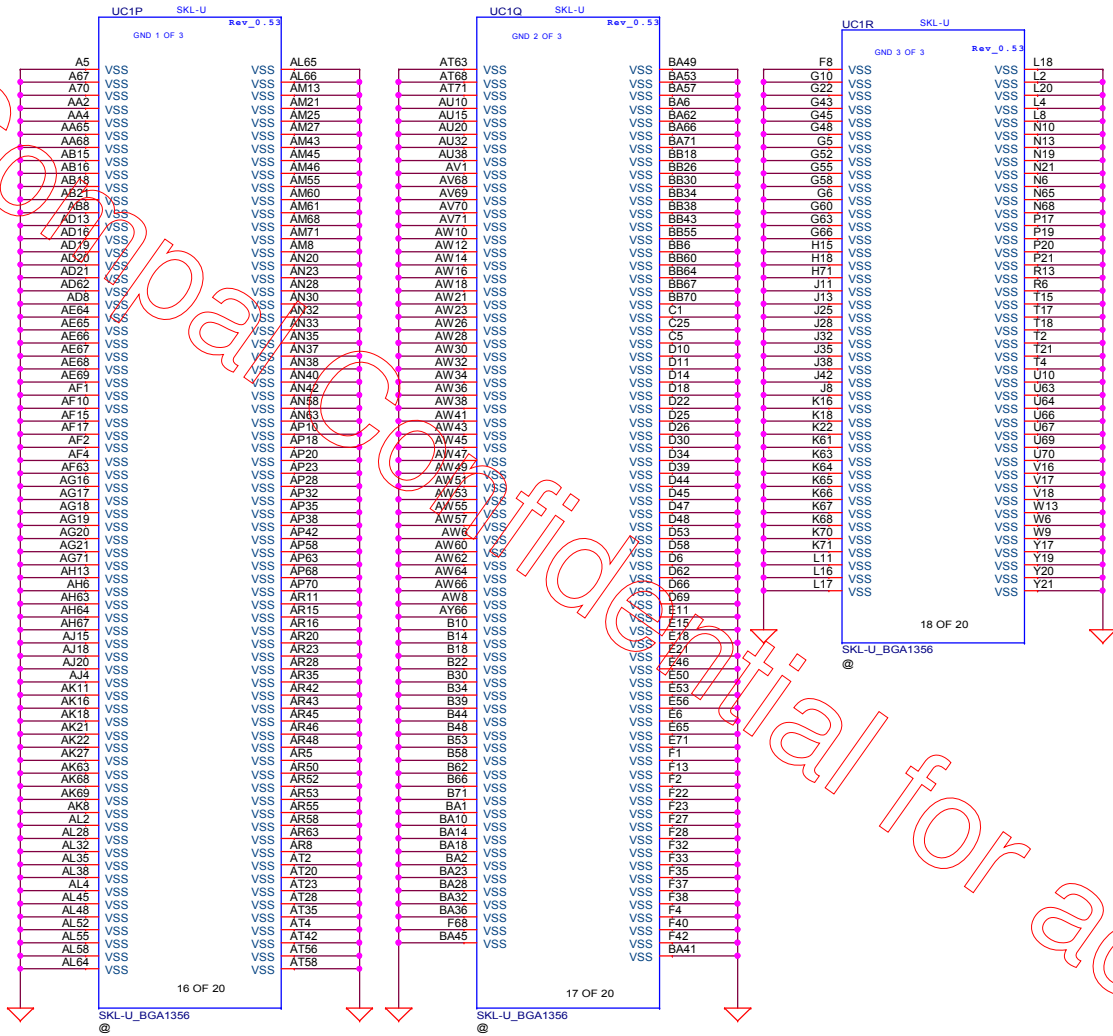
Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

Compal Electronics, Inc.

Title: SKL-U(10/12)Power,SVID

Size: Custom | Document Number: B5W11 M/B LA-E061P | Rev: 1.0

Date: Monday, July 18, 2016 | Sheet 16 of 44



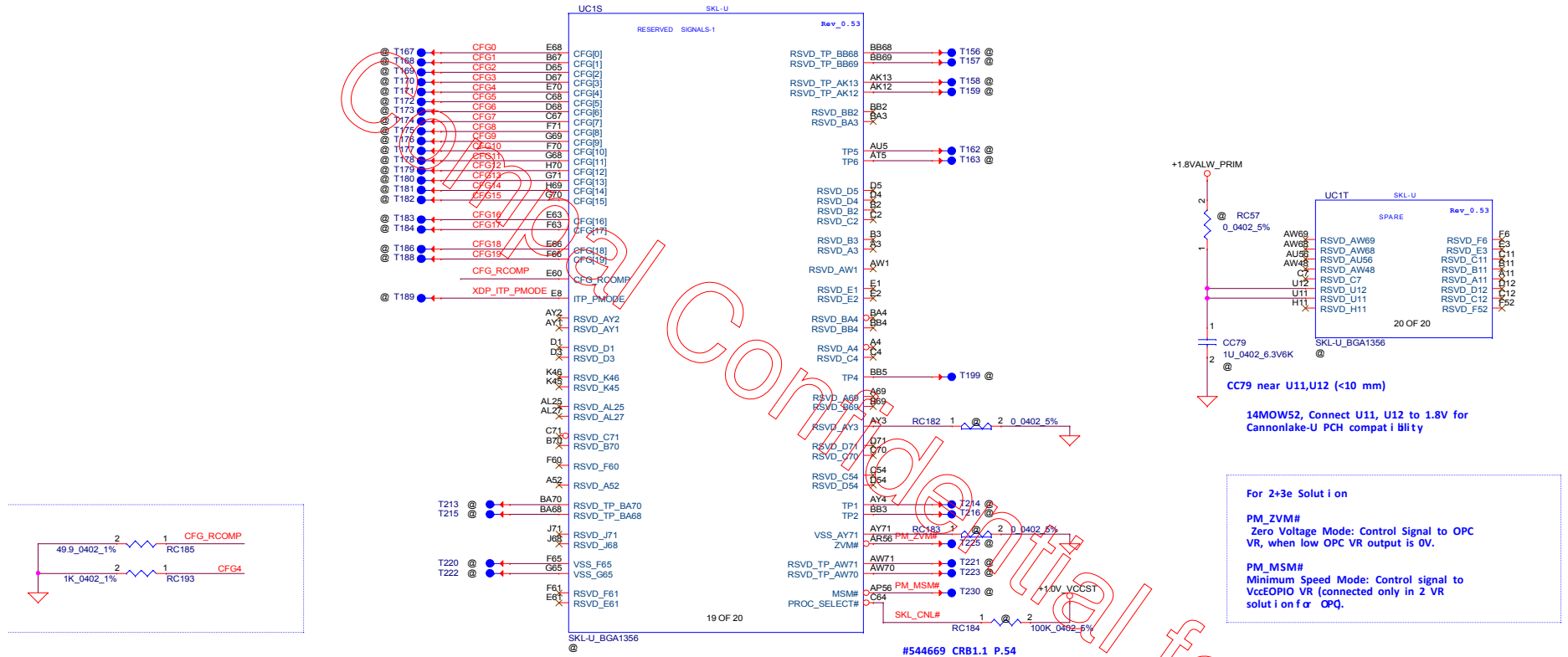
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: **SKL-U(11/12)GND**

Size	Document Number	Rev
Custom	B5W11 M/B LA-E061P	1.0

Date: Monday, July 18, 2016 Sheet 17 of 44



CC79 near U11,U12 (<10 mm)

14MOW52, Connect U11, U12 to 1.8V for Cannonlake-U PCH compatibility

For 2+3e Solution

PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.

PM_MSM#
Minimum Speed Mode: Control signal to VccEOPIO VR (connected only in 2 VR solution for OPC).

#544669 CRB1.1 P.54
#544924 SKL EDS1.2 P.125
PROC_SELECT#
This pin is for compatibility with future platforms. It should be unconnected for the processor.

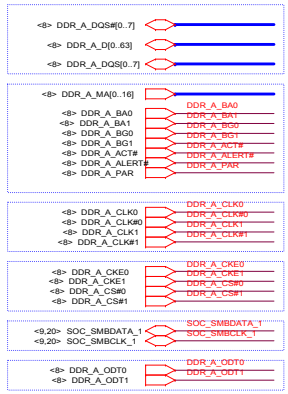
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: SKL-U(12/12)RSVD			
Size: Custom	Document Number: B5W11 M/B LA-E061P		Rev: 1.0
Date: Monday, July 18, 2016		Sheet 18 of 44	

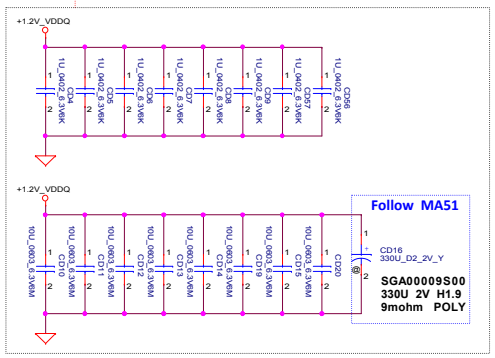
Reverse Type

2-3A to 1 DIMMs/channel

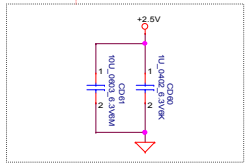


Layout Note:
Place near JDIMM1

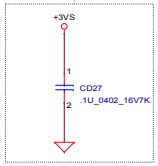
Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

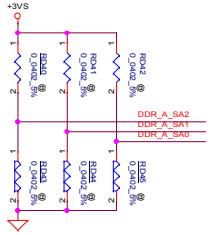


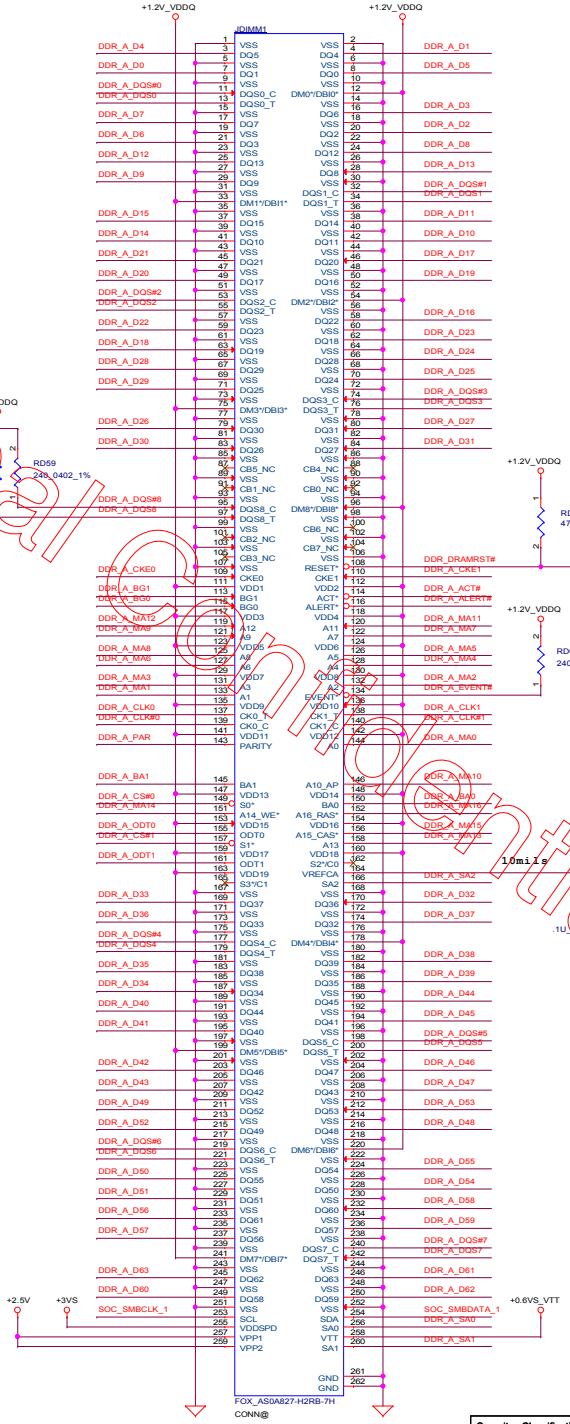
Layout Note:
Place near JDIMM1.257,259

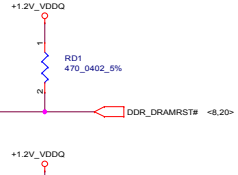


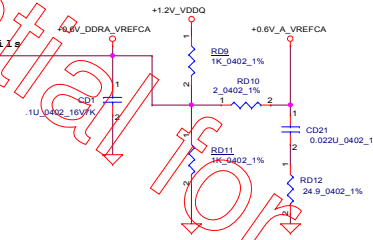
Layout Note:
Place near JDIMM1.255





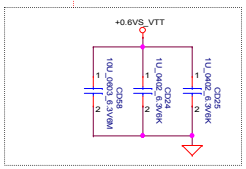






Place near to SO-DIMM connector.

Layout Note:
Place near JDIMM1.258



Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: **DDR4 DIMMA**

Size	Document Number	Rev
Custom	B5W11 M/B LA-E061P	1.0

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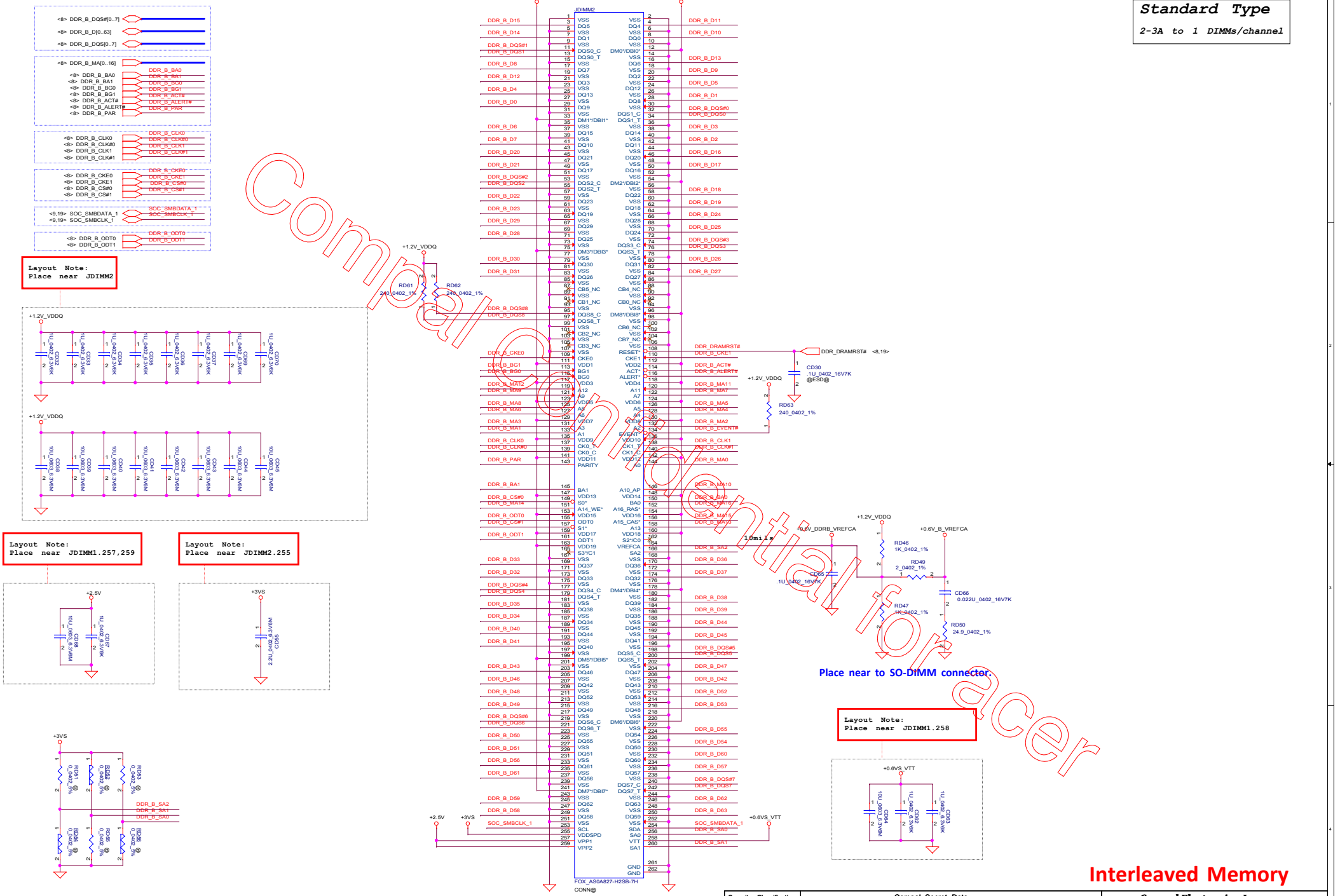
Standard Type

2-3A to 1 DIMMs/channel



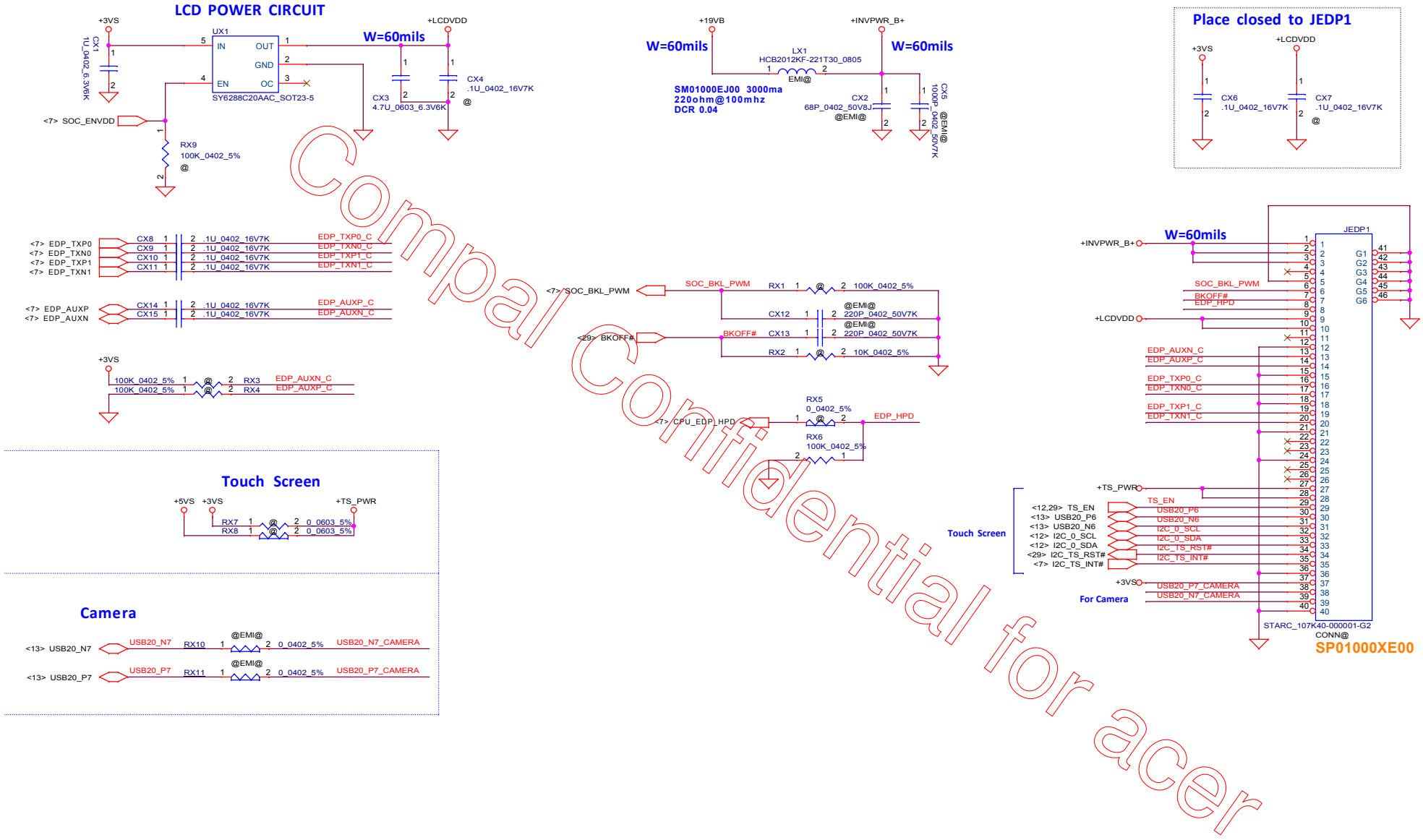
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: DDR4 DIMMB

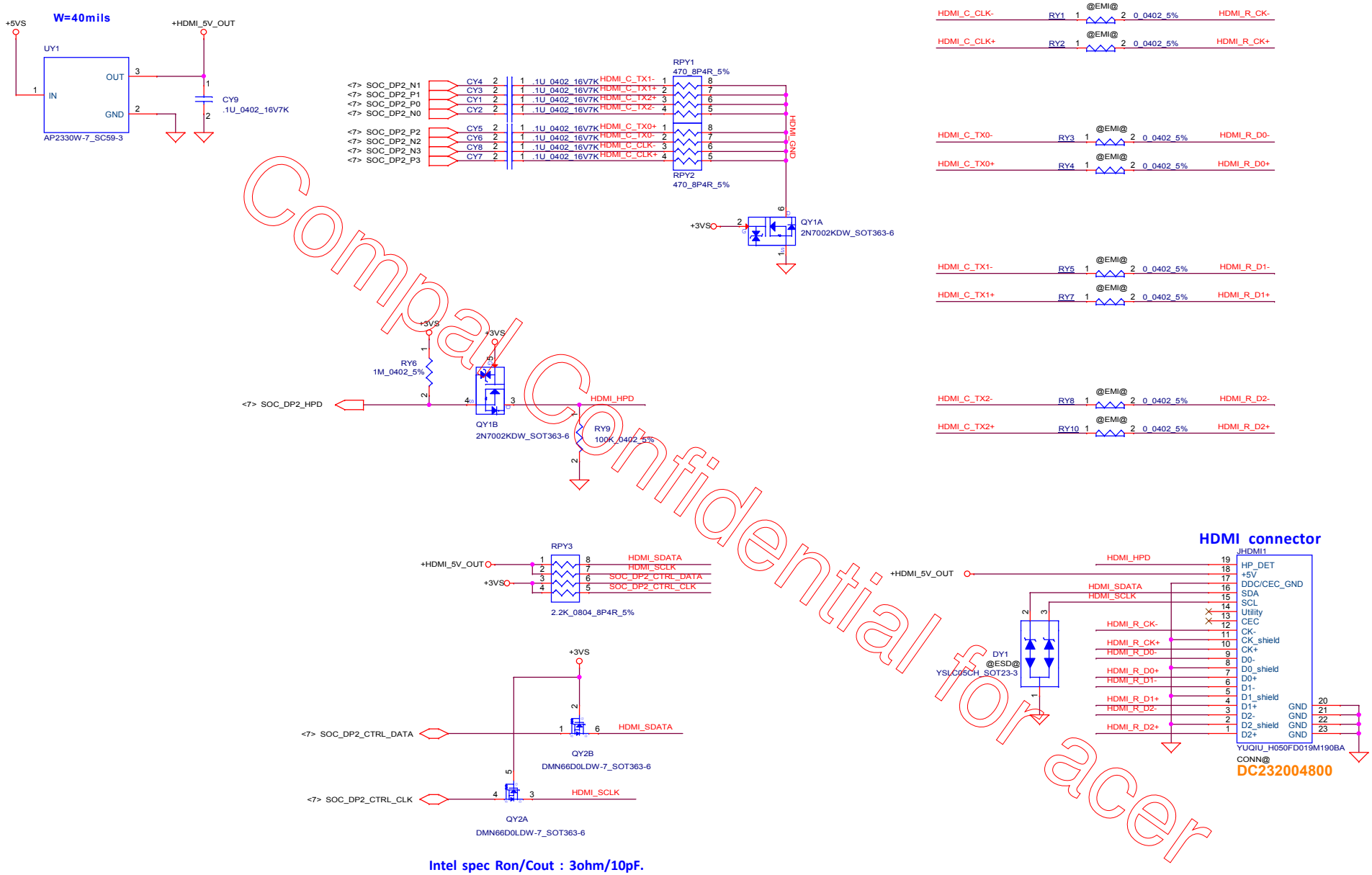
Size: Custom | Document Number: B5W11 M/B LA-E061P | Rev: 1.0

Date: Monday, July 18, 2016 | Sheet 20 of 44



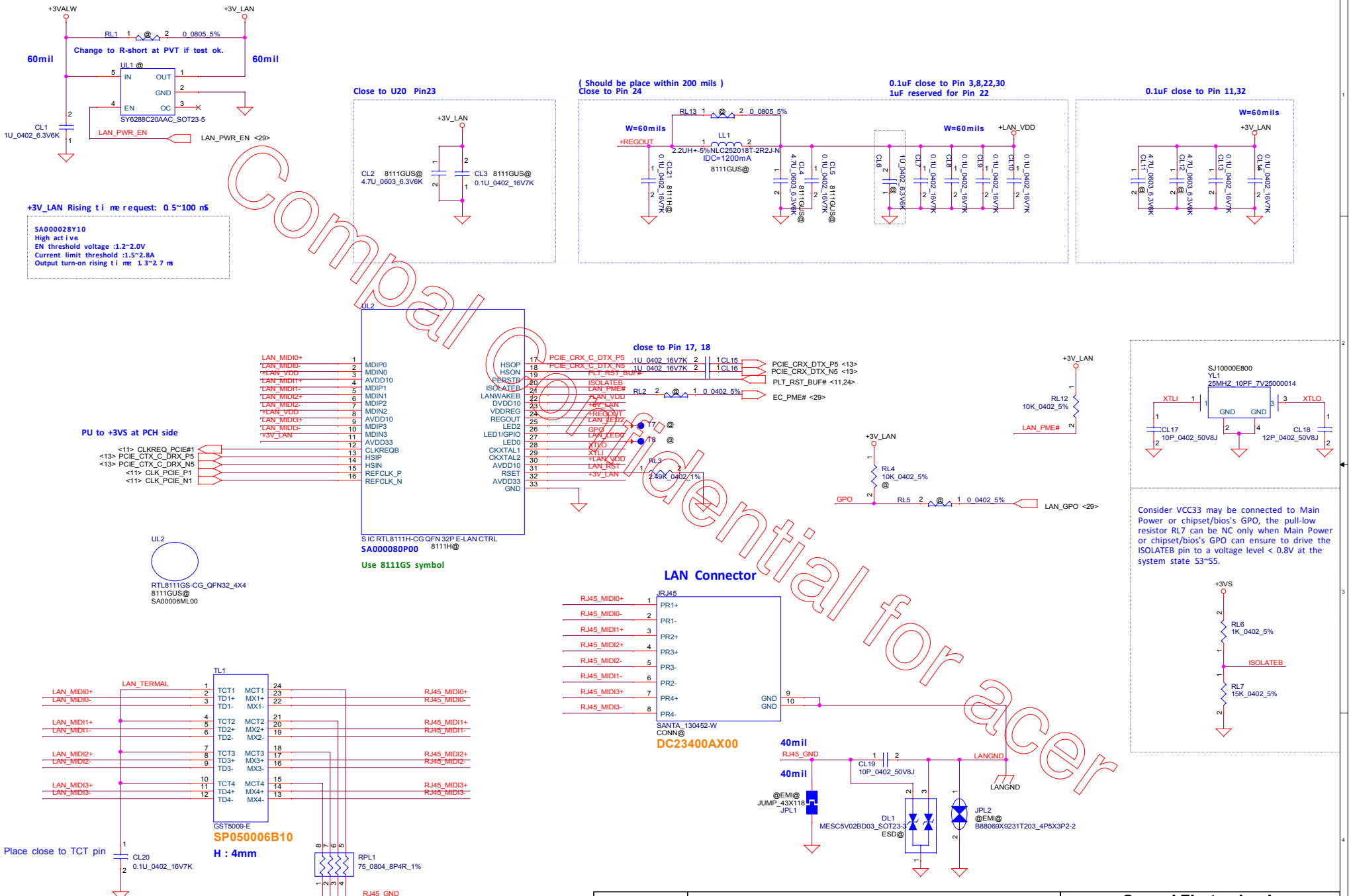
Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: eDP Connector			
Size: Custom	Document Number: B5W11 M/B LA-E061P		Rev: 1.0
Date: Monday, July 18, 2016	Sheet 21 of 44		



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: HDMI CONN.			
Size: Custom	Document Number: B5W11 M/B LA-E061P		Rev: 1.0
Date: Monday, July 18, 2016	Sheet 22 of 44		



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2014/10/28

Compal Electronics, Inc.

Title: LAN_RTL8111H

Size	Document Number	Rev
Custom	B5W11 M/B LA-E061P	1.0

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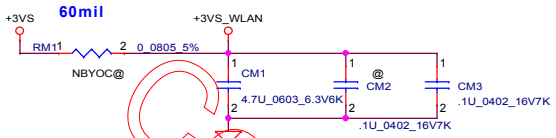
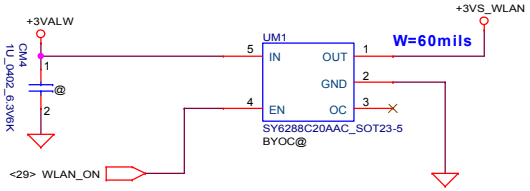
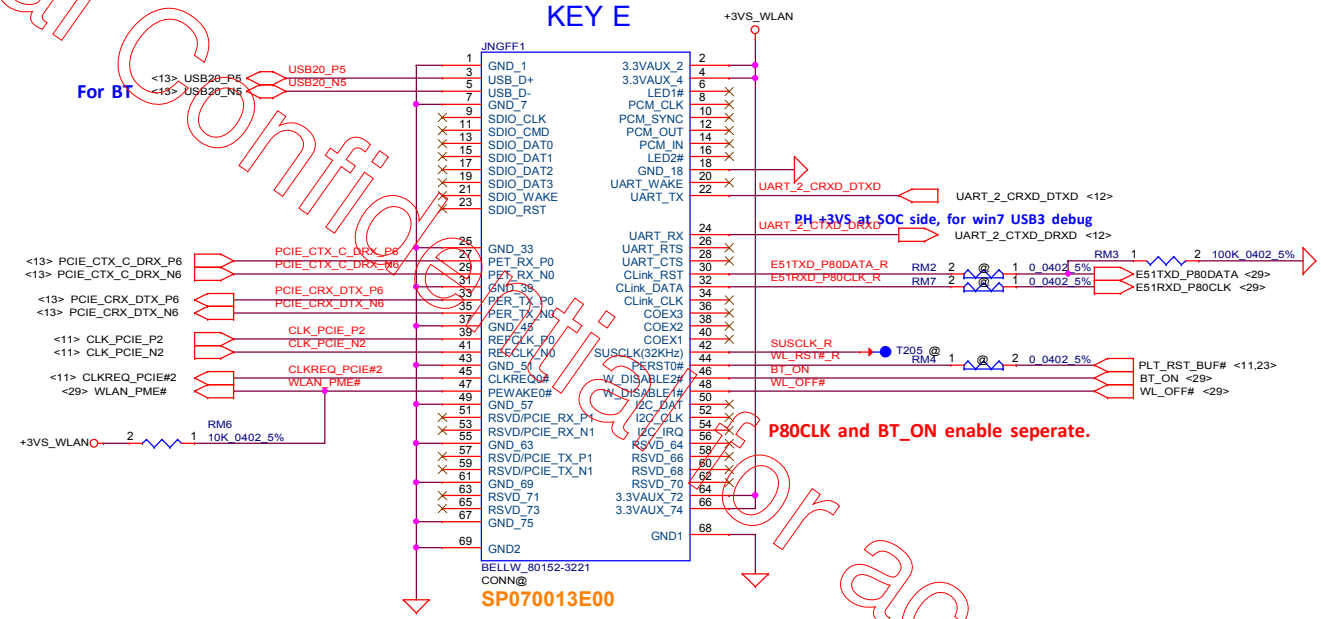
Wireless LAN





NGFF WL+BT (KEY E)

KEY E



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: M.2 Key E (WLAN)

Size	Document Number	Rev
Custom	B5W11 M/B LA-E061P	1.0

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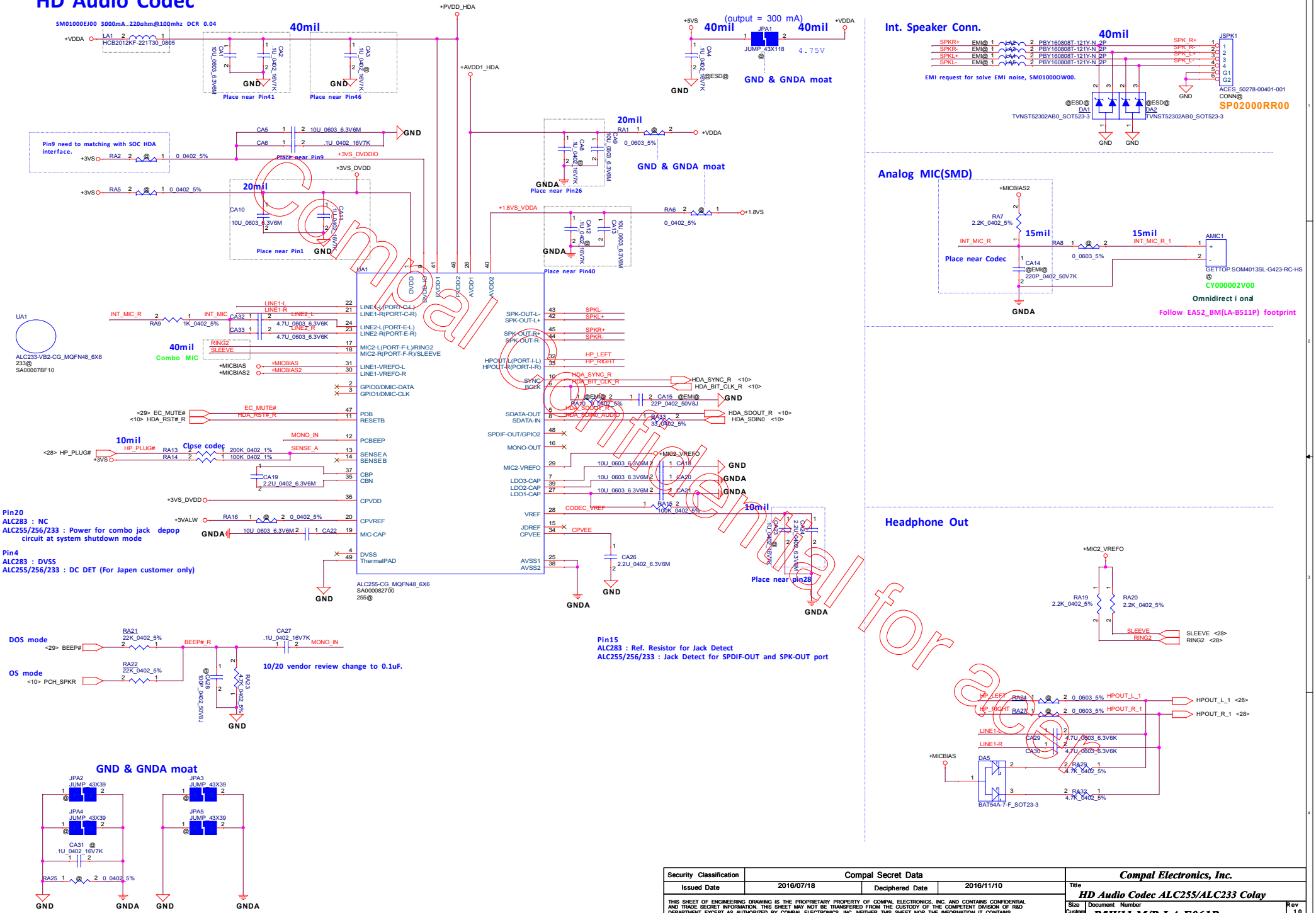
HD Audio Codec



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: HD Audio Codec ALC255/ALC233 Colay			
Size: Custom	Document Number: B5W11 M/B LA-E061P		Rev: 1.0
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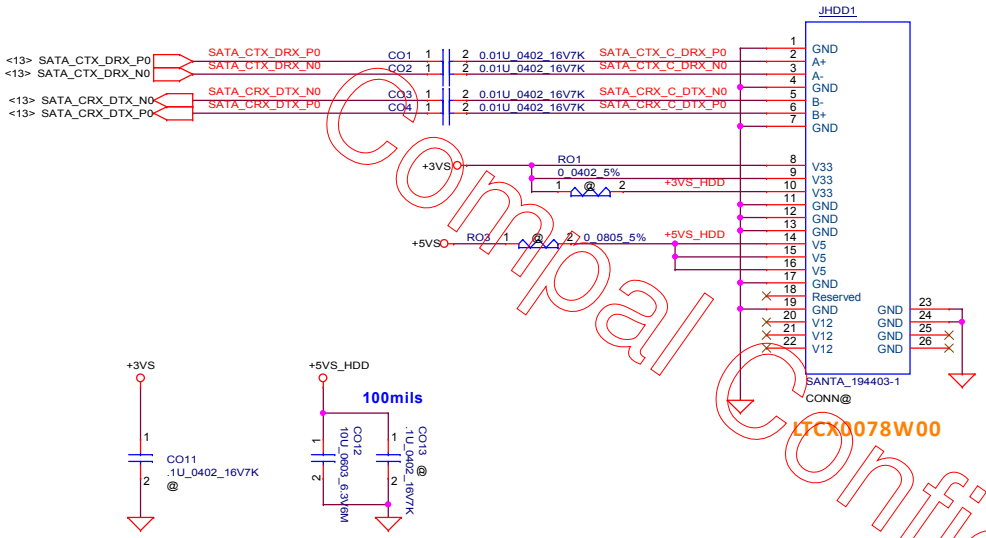
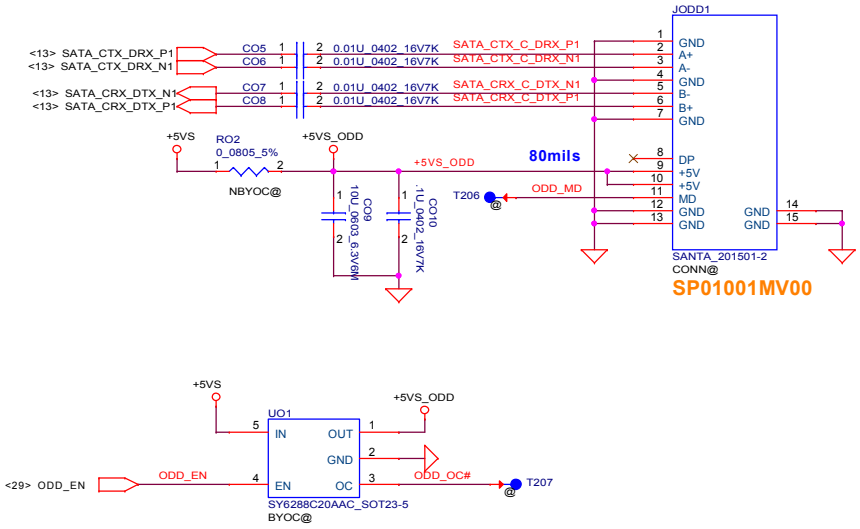
SATA HDD Conn.



SATA ODD Conn.



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: HDD/ODD/ HDD Re-Driver			
Size: Custom	Document Number: B5W11 M/B LA-E061P		Rev: 1.0
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SPACE

Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: **EMMC STORAGE**

Size	Document Number	Rev
Custom	B5W11 M/B LA-E061P	1.0

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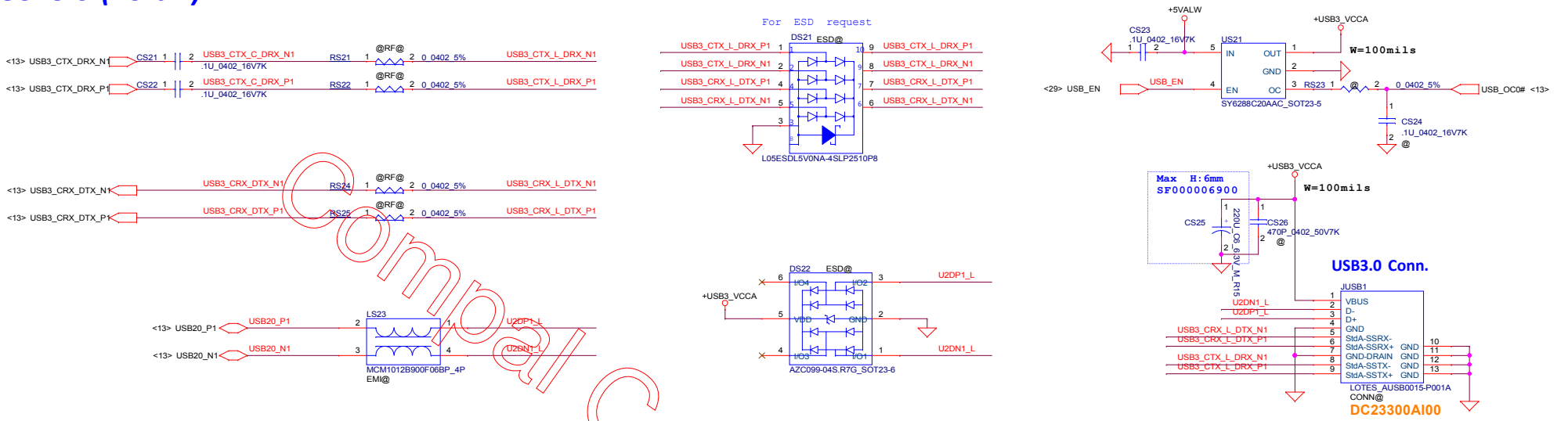
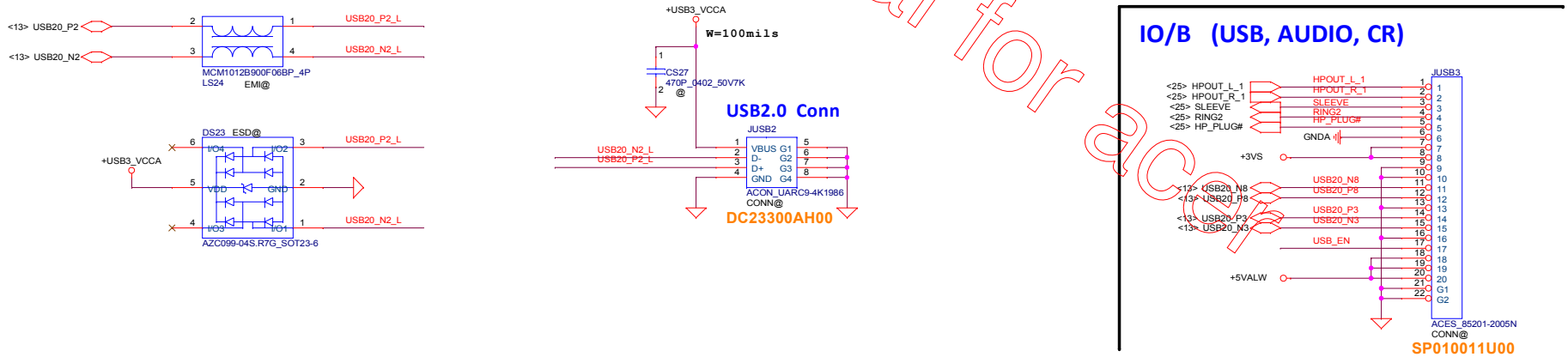
USB3.0 (Port 1)



USB2.0 (Port 2)



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title	USB Conn/IO_B		
Size	Document Number		Rev
Custom	B5W11 M/B LA-E061P		1.0
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PN:SM01000K500

CB9 1 2 1000P 0402 50V7K EC_RST#

+3VLP_EC
RB5 1 @ 2 47K_0402_5% EC_PME#
EC_PME# PU +3V_LAN at LAN side

+3VLP_EC
RB13 1 2 2.2K 0402 5% EC_SMB_CK1
RB14 1 2 2.2K 0402 5% EC_SMB_DA1

For turn off internal LPC module of KB9032

ESPI@ 1 2 47K_0402_5% ESPI_RST#
ESPI@ 1 2 47K_0402_5% PLT_RST#
CB5 1 2 100P_0402_50V8J @ESD@
CB6 1 2 100P_0402_50V8J AC_IN
@EMI@ 2 1 CB7 22P_0402_50V8J @EMI@ 1 2 RB10 33_0402_5% CLK_LPC_EC

RB12 0_0402_5% 1 @ 2 EC_KBRST#
<9> EC_KBRST#_R

For abnormal shutdown
SPOK
DB2 RB751V-40_SOD323-2 EC_RSMRST#
DB3 RB751V-40_SOD323-2 PCH_PWROK
DB4 RB751V-40_SOD323-2 EC_VCCST_PG_R

Board ID
+3VLP_EC
Ra RB1 100K_0402_1%
AD_BID
Rb RB4 15K_0402_1% CB4 .1U_0402_16V7K @

Analog Board ID definition, Please see page 3.

+3VLP @RB22 0_0805_5% +3VLP_EC
LB1 FBMA-L11-160808-800LMT_0603 +3VLP_ECA
CB1 .1U_0402_16V7K CB2 .1U_0402_16V7K
+3VALW_1.8VALW_PGPPA
RB3 0_0402_5% @ RB2 0_0402_5%
+3VCC_LPC
CB3 .1U_0402_16V7K
ECAGND ECAGND <34>

UB1

ESPI Bus Pin : 1-3,7,8,10,12,14
LPC Bus Pin : 3-5,7,8,10,12,13
Combine w/ SMI

<11> SUSPWRDNACK SUSPWRDNACK
<9> TPM_SERIRQ TPM_SERIRQ
<9> LPC_FRAME# LPC_FRAME#
<9> LPC_AD3_R LPC_AD3_R
<9> LPC_AD2_R LPC_AD2_R
<9> LPC_AD1_R LPC_AD1_R
<9> LPC_AD0_R LPC_AD0_R
<9> CLK_LPC_EC CLK_LPC_EC
<11> PLT_RST# PLT_RST#
<31> EC_RST# EC_RST#
<7> EC_SCI# EC_SCI#
<24> WLAN_ON WLAN_ON

GATEA20/GPIO00 KBRST#/GPIO01 SERIRQ LPC_FRAME# LPC_AD3 LPC_AD2 LPC_AD1 LPC_AD0 CLK_PCI_EC PCIRST#/GPIO05 EC_RST# EC_SCI#/GPIO0E CLKRUN#/GPIO1D
LPC & MISC

VCC_LPC VCC VCC VCC VCC AVCC
PWM Output
EC_VCCST_PG/GPIO0F BEEP#/GPIO10 EC_FAN_PWM/GPIO12 AC_OFF/GPIO13
EC_VCCST_PG_R BEEP# FAN_PWM1 I2C_TS_RST#
<11,32> <25> <31> <21>

AD Input
VCIN1_BATT_TEMP/AD0/GPIO38 VCIN1_BATT_DROP/AD1/GPIO39 ADP_I/AD2/GPIO3A AD_BID/AD3/GPIO3B AD4/GPIO42 AD5/GPIO43
BATT_TEMP VCIN1_BATT_DROP ADP_I AD_BID WLAN_PME# EC_PME#
<34> <34> <34,35> <24> <23>

DA Output
DA0/GPIO3C EN_DFAN1/DA1/GPIO3D DA2/GPIO3E DA3/GPIO3F
LAN_PWR_EN
<23>

PS2 Interface
EC_MUTE#/PSCLK1/GPIO4A USB_EN#/PSDAT1/GPIO4B PSCLK2/GPIO4C PSDAT2/GPIO4D TP_CLK/GPIO4E TP_DATA/GPIO4F
EC_MUTE# USB_EN PM_SLP_S0# TP_CLK TP_DATA
<25> <28> T85 @ <11> <30> <30>
PU at PTP side

<30> KSI[0..7]
<30> KSO[0..17]
Int. K/B Matrix
KSI0 KSI1 KSI2 KSI3 KSI4 KSI5 KSI6 KSI7
KSO0 KSO1 KSO2 KSO3 KSO4 KSO5 KSO6 KSO7 KSO8 KSO9 KSO10 KSO11 KSO12 KSO13 KSO14 KSO15 KSO16 KSO17
KSI0/GPIO30 KSI1/GPIO31 KSI2/GPIO32 KSI3/GPIO33 KSI4/GPIO34 KSI5/GPIO35 KSI6/GPIO36 KSI7/GPIO37
KSO0/GPIO20 KSO1/GPIO21 KSO2/GPIO22 KSO3/GPIO23 KSO4/GPIO24 KSO5/GPIO25 KSO6/GPIO26 KSO7/GPIO27 KSO8/GPIO28 KSO9/GPIO29 KSO10/GPIO2A KSO11/GPIO2B KSO12/GPIO2C KSO13/GPIO2D KSO14/GPIO2E KSO15/GPIO2F KSO16/GPIO48 KSO17/GPIO49

SPI Device Interface
SPI Flash ROM
ENKBL/GPXIOA00 WOL_EN/GPXIOA01 ME_EN/GPXIOA02 VCIN0_PH1/GPXIOD00
ENBKL TP_PWR_EN ME_EN VCIN0_PH
<7> <30> <10> <34>
MISO/GPIO5B MOSI/GPIO5C SPICLK/GPIO58 SPICS#/GPIO5A
BT_ON
<24>

GPIO
EC_CIR_RX/AD6/GPIO40 SYS_PWROK/AD7/GPIO41 GPIO50 BATT_CHG_LED#/GPIO52 CAPS_LED#/GPIO53 PWR_LED#/GPIO54 BATT_LOW_LED#/GPIO55 SYSON/GPIO56 VR_ON/GPIO57 DPWROK_EC/GPIO59
SYS_PWROK_R BATT_4S BATT_BLUE_LED# ODD_EN PWR_LED#_R BATT_AMB_LED# SYSON EC_TP_INT#
<35> <30> <26> <30> <30> <37> <7,30>

SM Bus
EC_SMB_CK1 EC_SMB_DA1 SOC_SML1CLK SOC_SML1DATA
EC_SMB_CLK1/GPIO44 EC_SMB_DAT1/GPIO45 EC_SMB_CLK2/GPIO46 EC_SMB_DAT2/GPIO47
<34,35> <34,35> <9> <9>
PU at CPU side

GPIO
PM_SLP_S3# ESPI_RST# SPOK TP_EN TS_EN WL_OFF# AC_PRESENT FAN_SPEED1 VR_ON E51TXD_P80DATA E51RXD_P80CLK PCH_PWROK PWR_SUSP_LED# VR_PWRGD
PM_SLP_S3#/GPIO04 GPIO07 GPIO08 GPIO0A GPIO0B GPIO0C AC_PRESENT/GPIO0D PWM2/GPIO11 FAN_SPEED1/GPIO14 FANFB1/GPIO15 EC_TX/GPIO16 EC_RX/GPIO17 PCH_PWROK/GPIO18 SUSP_LED#/GPIO19 NUM_LED#/GPIO1A
<11,32> <9> <36,39> <30> <12,21> <24> <11> <31> <32,40> <24> <24> <11,32> <30> <40>

GPIO,GPO
EC_RSMRST#/GPXIOA03 GPXIOA04 VCIN1_ADP_PROCHOT/GPXIOA05 VCOUT1_PROCHOT#/GPXIOA06 VCOUT0_MAIN_PWR_ON/GPXIOA07 BKOFF#/GPXIOA08 GPXIOA09 PCH_PWR_EN/GPXIOA10 PWR_VCCST_PG/GPXIOA11
EC_RSMRST# VCIN1_ADP_PROCHOT VCOUT1_PROCHOT# MAINPWON BKOFF# LAN_GPO 3V_EN_R
<11> <34> <34,36> <21> <23>

GPI
VCIN1_AC_IN/GPXIOD01 EC_ON/GPXIOD02 ON/OFF#/GPXIOD03 LID_SW#/GPXIOD04 SUSP#/GPXIOD05 GPXIOD06 PECI/GPXIOD07
AC_IN EC_ON ON/OFFBTN# LID_SW# SUSP# H_PECI_R
<35> <38> <30> <30> <14,32,35,37>
RB19 1 2 43_0402_1% H_PECI <7>

V18R/VCC_IO2
+3VLP_EC

PBTN_OUT#/GPIO5D PM_SLP_S4#/GPIO5E
PBTN_OUT# PM_SLP_S4#
<11> PBTN_OUT#
<11,32> PM_SLP_S4#

GND GND GND GND GND AGND
KB9022QD_LQFP128_14X14
20mil
ECAGND

CB8 1 2 100P_0402_50V8J BATT_TEMP
LB2 2 1 FBMA-L11-160808-800LMT_0603
PN:SM01000K500

CO-LAY with KB9032QA (SA000080J00)

+3VLP_EC
LID_SW# RB15 1 2 100K_0402_1%
I2C_TS_RST# RB6 2 1 100K_0402_5%

SYS_PWROK_R RB11 1 @ 2 0_0402_5% SYS_PWROK <11,32>

For Thermal Portect Shutdown
DB1 RB751V-40_SOD323-2
MAINPWON 1 2 3V_EN 3V_EN <36>
3V_EN_R RB16 1K_0402_5% RB17 1M_0402_5%

RB20 1 @ 2 0_0402_5% VR_HOT# VR_HOT# <40>
<7> H_PROCHOT# H_PROCHOT# RB21 1 @ 2 0_0402_5% VCOUT1_PROCHOT#

Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: **EC ENE KB9022**

Size: Custom | Document Number: **B5W11 M/B LA-E061P** | Rev: 1.0

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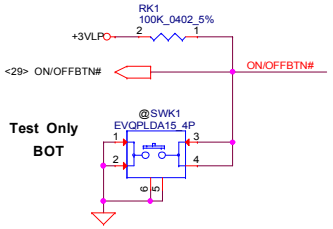
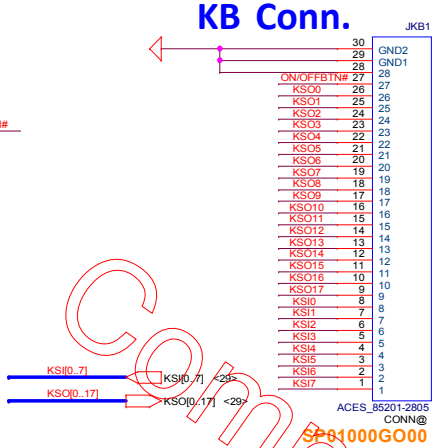
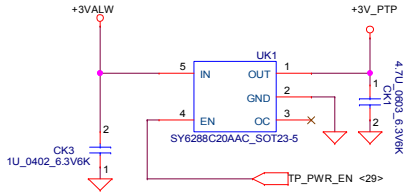
KB Conn.

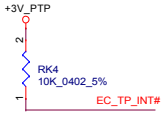
ON/OFF BTN

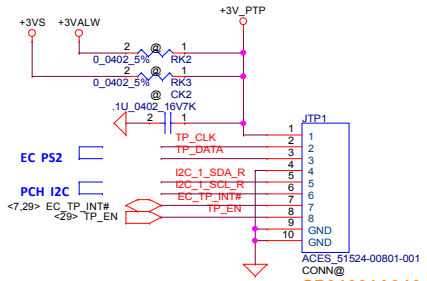


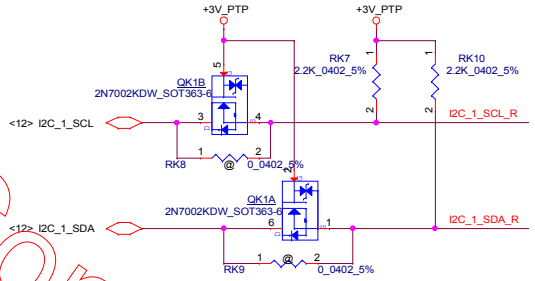


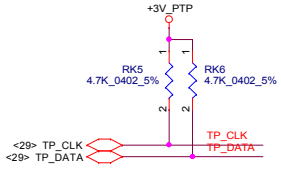
TP/B Conn.







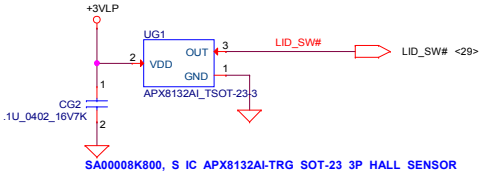




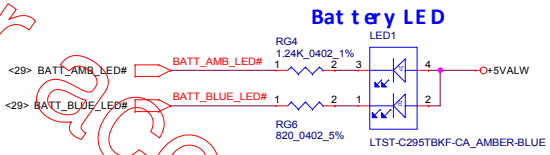
Lid Switch

(Hall Effect Switch)

Follow 2015

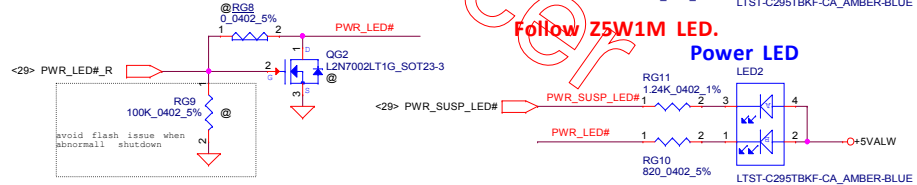


Bat t ery LE D



Follow Z5W1M LED.

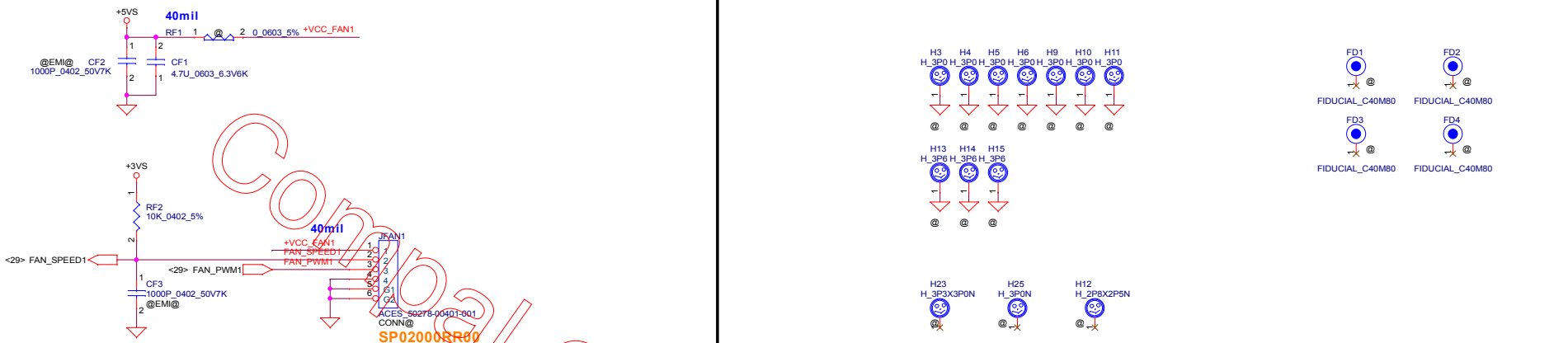
Power LED



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

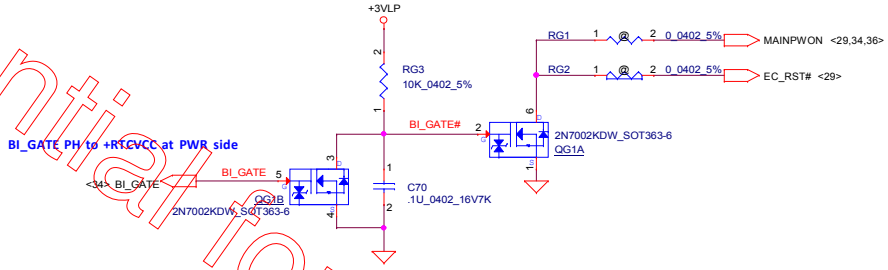
Compal Electronics, Inc.			
Title	KB & TP & TPM & LID SW & LED		
Size: Custom	Document Number: B5W11 M/B LA-E061P		Rev: 1.0
Date: Monday, July 18, 2016		Sheet 30 of 44	

FAN1 Conn

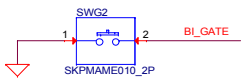


Screw Hole

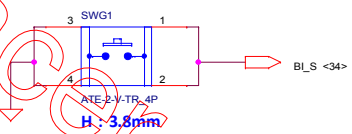
Reset Circuit



Reset Button



BI SW



H : 3.8mm

Release : Battery Of
Push : Battery ON

Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

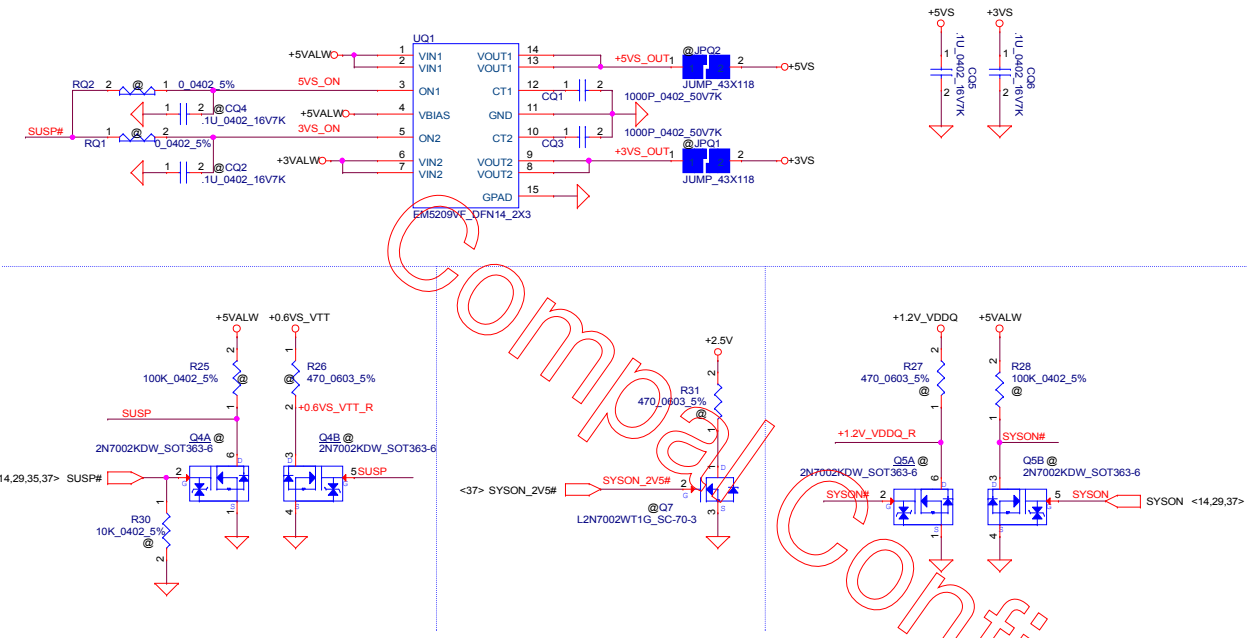
Compal Electronics, Inc.

Title: FAN & Screw Hole & Reset

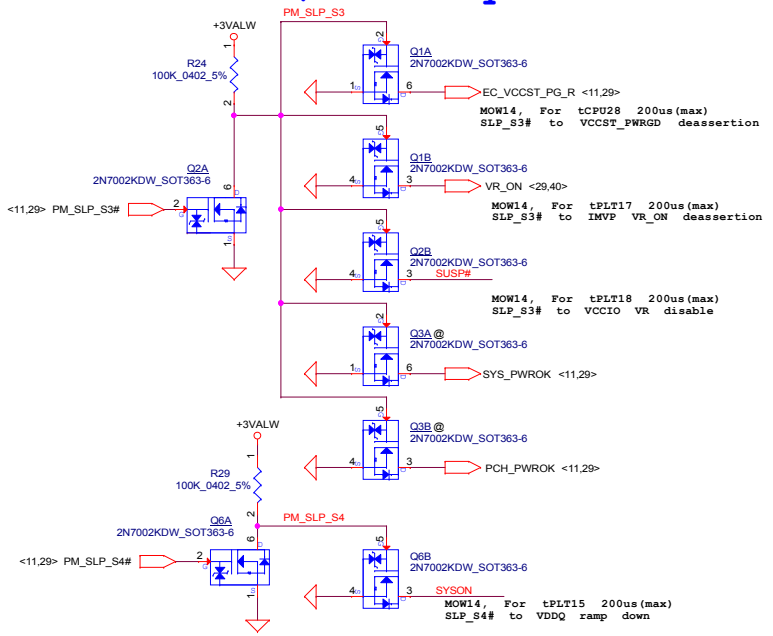
Size	Document Number	Rev
Custom	B5W11 M/B LA-E061P	1.0

Date: Monday, July 18, 2016 Sheet 31 of 44

DC Interface



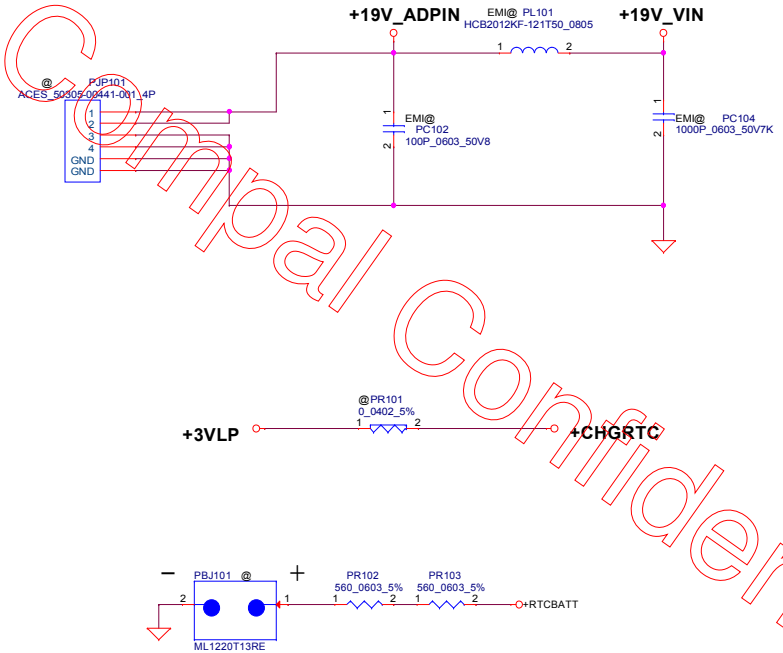
For Power ON/Off Sequence



Security Classification	Compal Secret Data		
Issued Date	2016/07/18	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title: DC Interface			
Size: Custom	Document Number: B5W11 M/B LA-E061P		Rev: 1.0
Date: Monday, July 18, 2016		Sheet 32 of 44	

schematic from A4WAS



Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2016/11/10

Compal Electronics, Inc.

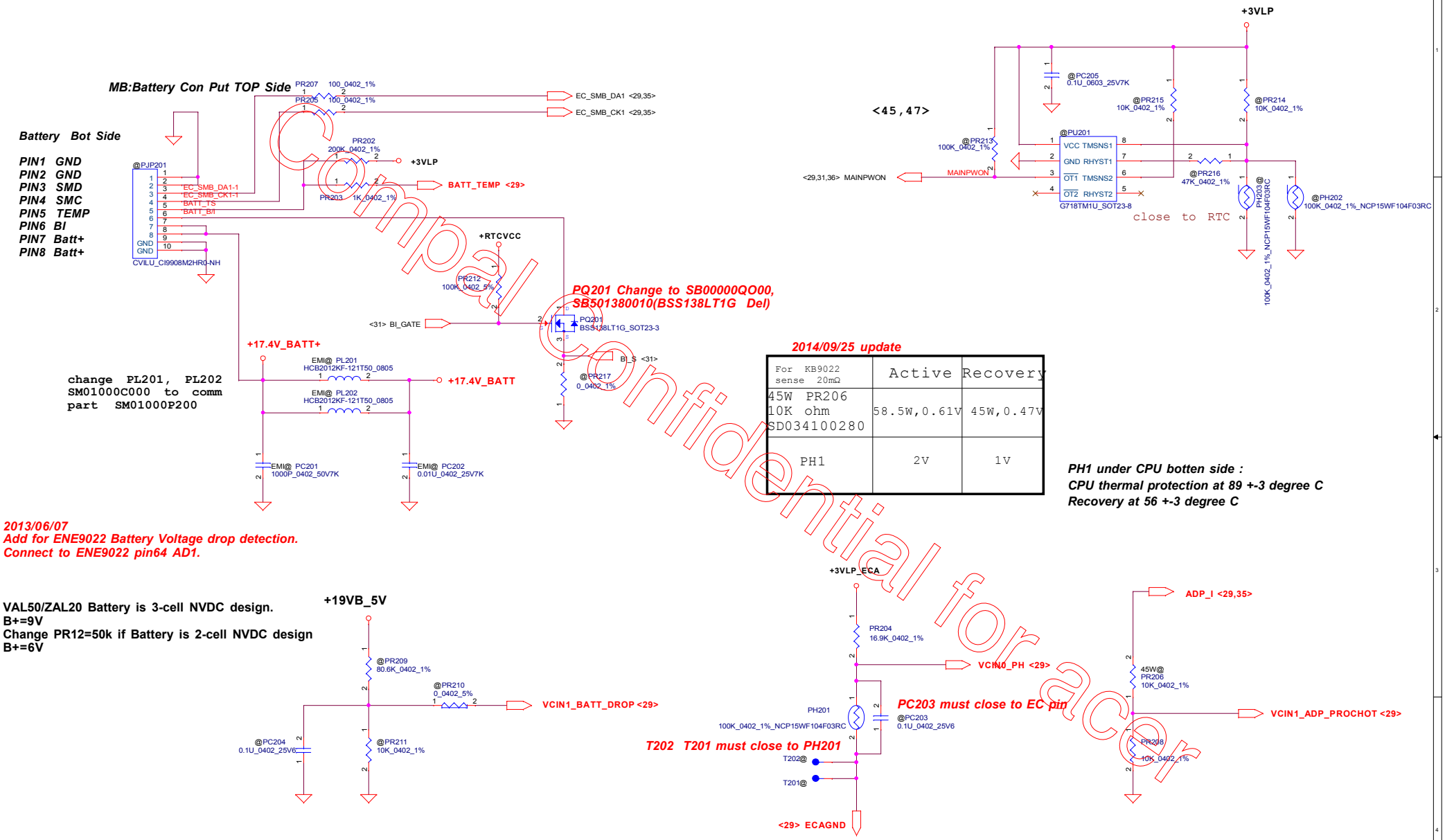
Title: PWR DCIN / Pre-charge

Size	Document Number	Rev
Custom	B5W1S M/B LA-D671P	0.2

Date: Monday, July 18, 2016 Sheet 33 of 44

2013/07/23
change PC5 and PC6 function field from 37.1 to 47.1

schematic from A4WAS



Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: B5W1S M/B LA-D671P | Rev: 0.2

Date: Monday, July 18, 2016 | Sheet 34 of 44

Protection for reverse input

schematic from module

Need check the SOA for inrush

Vgs = 20V
Vds = 60V
Id = 250mA

PQ301 2N7002KW_SOT323-3

PR301 1M_0402_5%

PR302 3M_0402_5%

+19V_VIN

PQ302 MDU1512RH_POWERDFN56-8-5

+19V_P1

PQ303 AON7506_DFN33-8-5

+19V_P2

PR303 0.02_1206_1%

@PJ301 JUMP_43X79

EMI@ PL301 1UH +-30% 2.8A

Isat: 4A
DCR: 27mohm

+19VB

+19VB_CHG

PC303 10U_0805_25V6K

PC304 10U_0805_25V6K

EMI@ PC305 2200P_0402_25V7K

@EMI@ PC306 0.1U_0402_25V6

PQ304 AON7506_DFN33-8-5

PC307 0.01U_0402_50V7K

BQ24725A_BATDRV

BQ24725A_BATDRV_1

PR305 4.12K_0603_1%

PC301 2200P_0402_50V7K

PR304 @ 0_0402_5%

PC302 0.1U_0402_25V6

BQ24725A_ACDRV_1

PC308 0.1U_0402_25V6

PC309 0.1U_0402_25V6

PC310 0.1U_0402_25V6

+19V_VIN

VF = 0.5V

PD301 BAS40CW_SOT323-3

PC311 0.047U_0402_25V7K

PR306 10_1206_1%

VF = 0.37V

PD302 RB751V-40_SOD323-2

PR307 2.2_0603_5%

Rds(on) = 30mohm max
Vgs = 20V
Vds = 30V
ID = 7A (Ta=70C)

PQ305 AON7506_DFN33-8-5

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VSRP-VSRN spec < 81.28mV

5*5*3

+17.4V_BATT

DH_CHG

@PR308 0_0603_5%

PC312 1U_0603_25V6K

PC313 1U_0603_25V6K

PL302 3.3UH_PCMB053T-3R3MS_5A_20%

PR311 0.01_1206_1%

BQ24725A_LX

CHG

PR309 4.12K_0603_1%

PR310 4.12K_0603_1%

PU301 BQ24735RGRR_QFN20_3P5X3P5

PAD
ACN
ACP
CMSRC
ACDRV
ACOK
VCC
PHASE
HIDRV
BTST
REGN
LODRV
GND
SRP
SRN
BATDRV
ACDET
IOUT
SDA
SCL
ILIM

BQ24725A_CMSRC

BQ24725A_ACDRV

DL_CHG

PR313 10_0603_1%

PR314 6.8_0603_1%

CSOP1

CSON1

PC319 0.1U_0603_16V7K

PC306 AON7506_DFN33-8-5

PR312 47_1206_5% @EMI@

PC318 680P_0402_50V7K @EMI@

PC316 0.1U_0402_25V6

PC317 0.1U_0402_25V6

PC314 10U_0805_25V6K

PC315 10U_0805_25V6K

PC324 10U_0805_25V6K

+3VLP

PR315 100K_0402_1%

<29> AC_IN

BQ24725A_ACDET

BQ24725A_IOUT

BQ24725A_ILIM

PR324 316K_0402_1%

PR317 100K_0402_1%

PC320 0.01U_0402_25V7K

PR318 422K_0402_1%

PC321 2200P_0402_50V7K

PR319 66.5K_0402_1%

PC322 100P_0402_50V8J

EC_SMB_CK1 <29,34>

EC_SMB_DA1 <29,34>

PR320 0_0402_5%

ADP_I <29,34>

PC323 @ 100P_0402_50V8J

Close EC chip

For 4S per cell 4.35V battery

PR321 2M_0402_1%

PR322 @ 0_0402_5%

PQ307 LTC015EUBFSSTL_UMT3F

PR323 100K_0402_1%

<29> BATT_4S

PQ308 2N7002KW_SOT323-3

<14,29,32,37> SUSP#

Vin Dectector

	Min.	Typ	Max.
L-->H	17.16V	17.63V	18.12V
H-->L	16.76V	17.22V	17.70V

VILIM = 20*ILIM*Rsr
ILIM = 3.3*100/(100+316)/20/0.01
= 3.966 A

Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2014/05/24

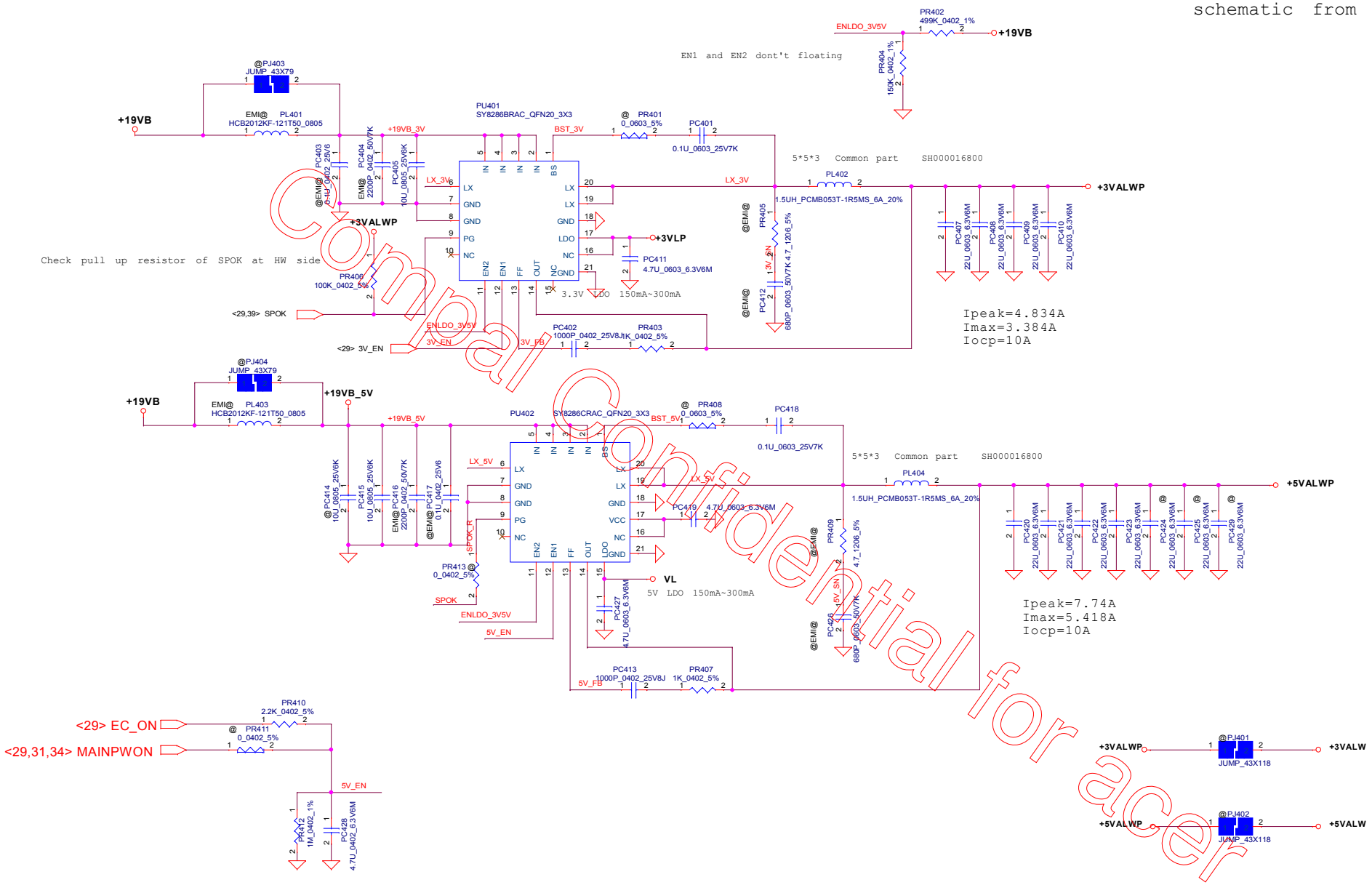
Compal Electronics, Inc.

Title: **CHARGER**

Size | Document Number: Common Circuit | Rev: 0.2

Date: Monday, July 18, 2016 | Sheet 35 of 44

schematic from A4WAS



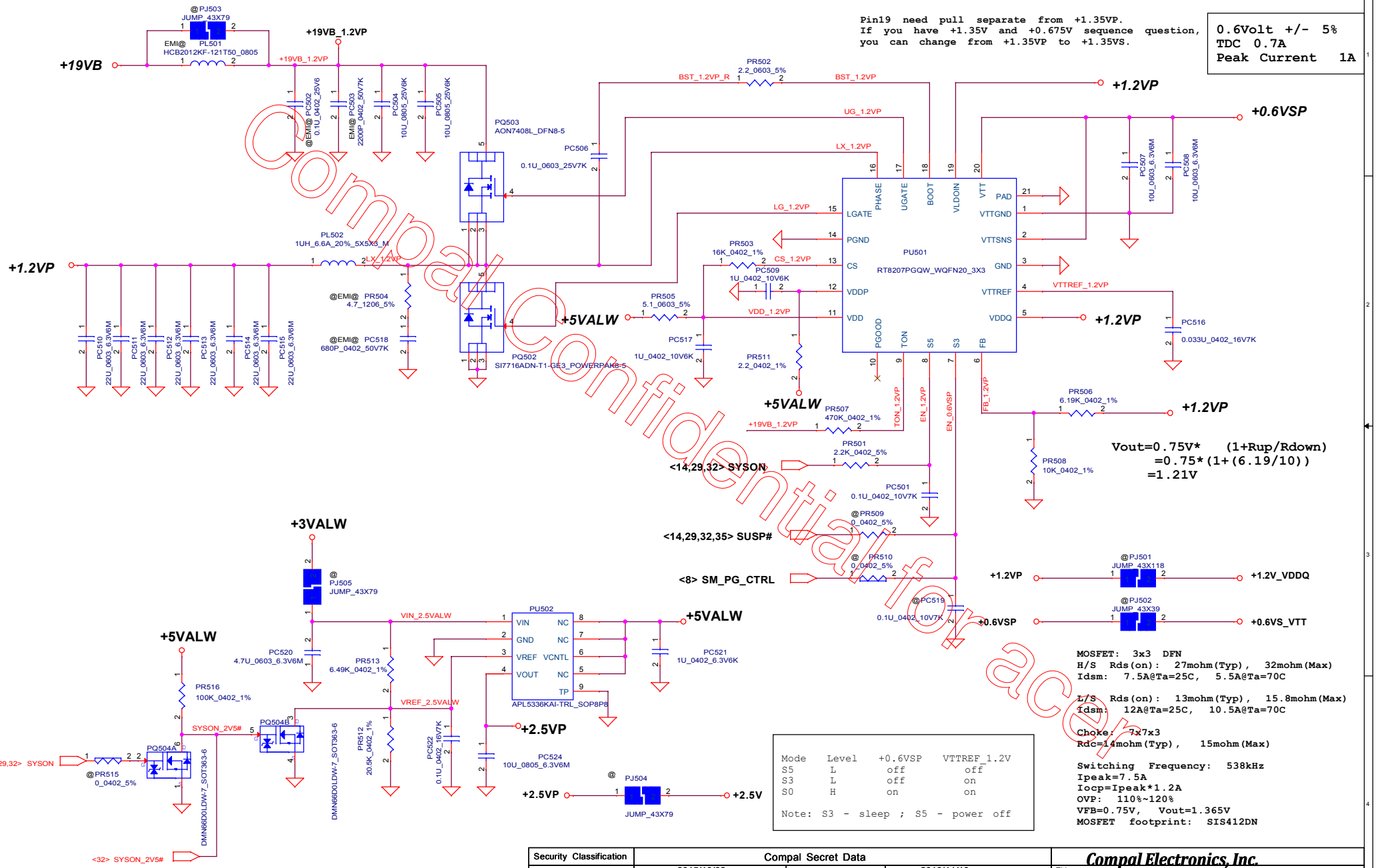
Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2016/11/10

Compal Electronics, Inc.			
Title	PWR-3.3VALWP/5VALWP		
Size Custom	Document Number B5W1S M/B LA-D671P		Rev 0.2
Date: Monday, July 18, 2016	Sheet 36 of 44		

schematic from A4WAS
IC change RT8207K

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A



Vout=0.75V* (1+Rup/Rdown)
=0.75*(1+(6.19/10))
=1.21V

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 32mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 13mohm(Typ), 15.8mohm(Max)
Idsm: 12A@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3
Rdc=14mohm(Typ), 15mohm(Max)

Switching Frequency: 538kHz
Ipeak=7.5A
Iocp=Ipeak*1.2A
OVP: 110%~120%
VFB=0.75V, Vout=1.365V
MOSFET footprint: SIS412DN

Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2016/11/10

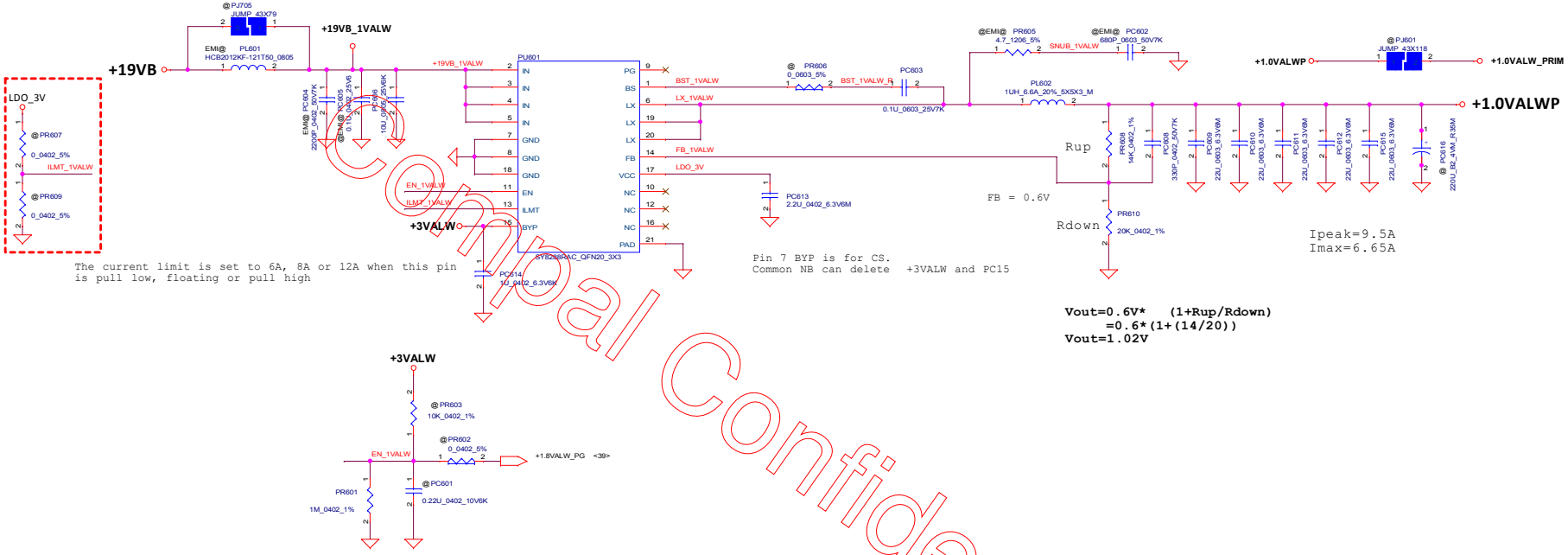
Compal Electronics, Inc.

Title: RT8207P

Size: Custom | Document Number: B5W1S M/B LA-D671P | Rev: 0.2

Date: Monday, July 18, 2016 | Sheet 37 of 44

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702



Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2016/11/10

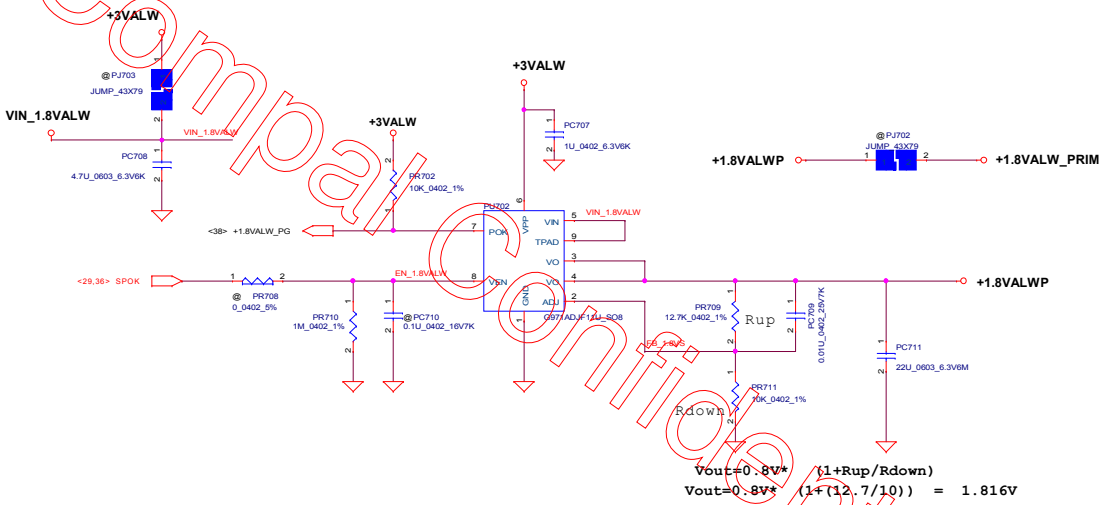
Compal Electronics, Inc.

Title: VCCP

Size	Document Number	Rev
C	B5W1S M/B LA-D671P	0.2

Date: Monday, July 18, 2016 Sheet 38 of 44

schematic from A4WAS
IC change to G971



Vout=0.8V* (1+Rup/Rdown)

Vout=0.8V* (1+(12.7/10)) = 1.816V

Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2016/11/10

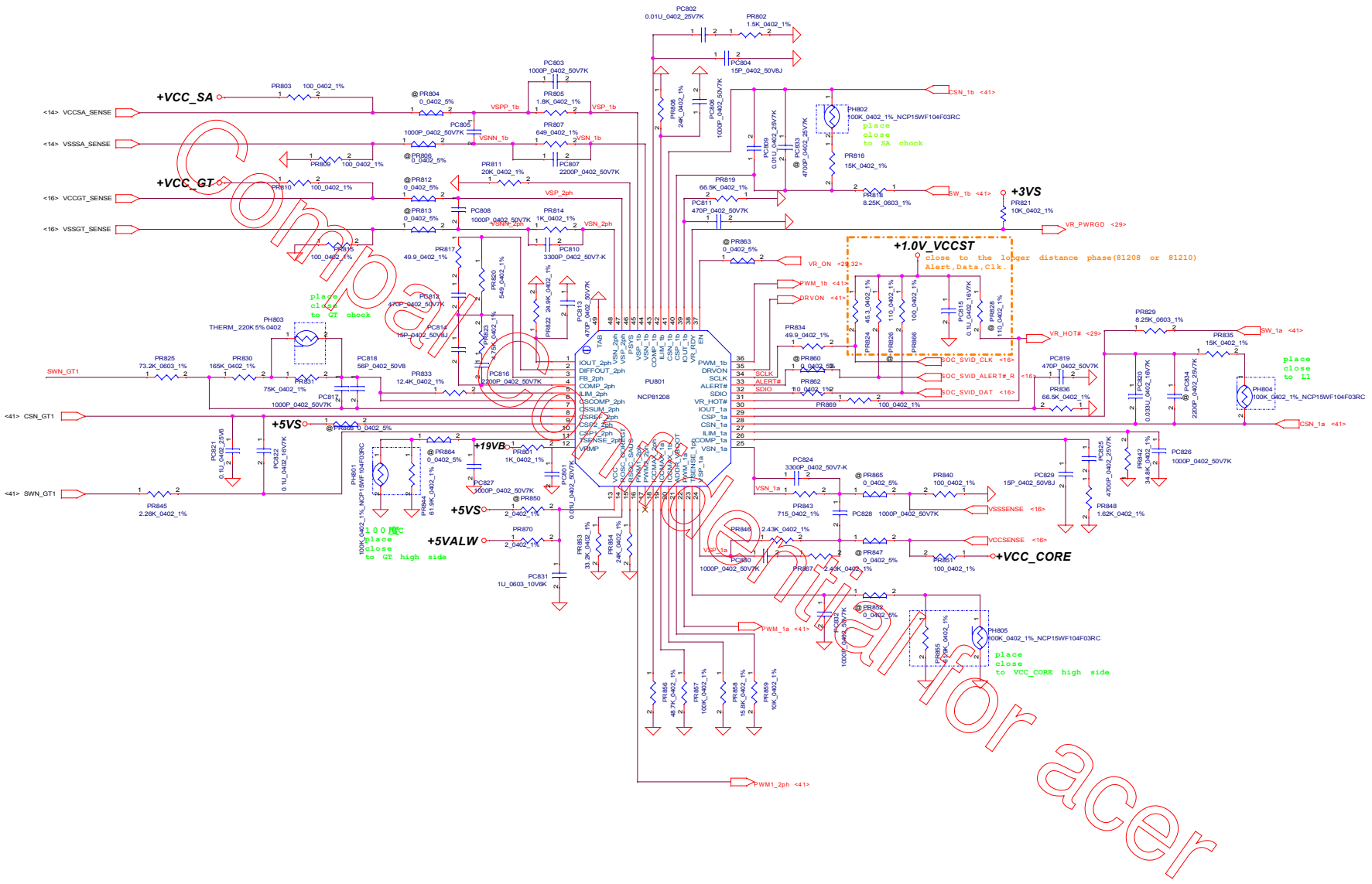
Compal Electronics, Inc.

Title: SY8032

Size: C | Document Number: B5W1S M/B LA-D671P | Rev: 0.2

Date: Monday, July 18, 2016 | Sheet 39 of 44

schematic from A4WAS



Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2016/11/10

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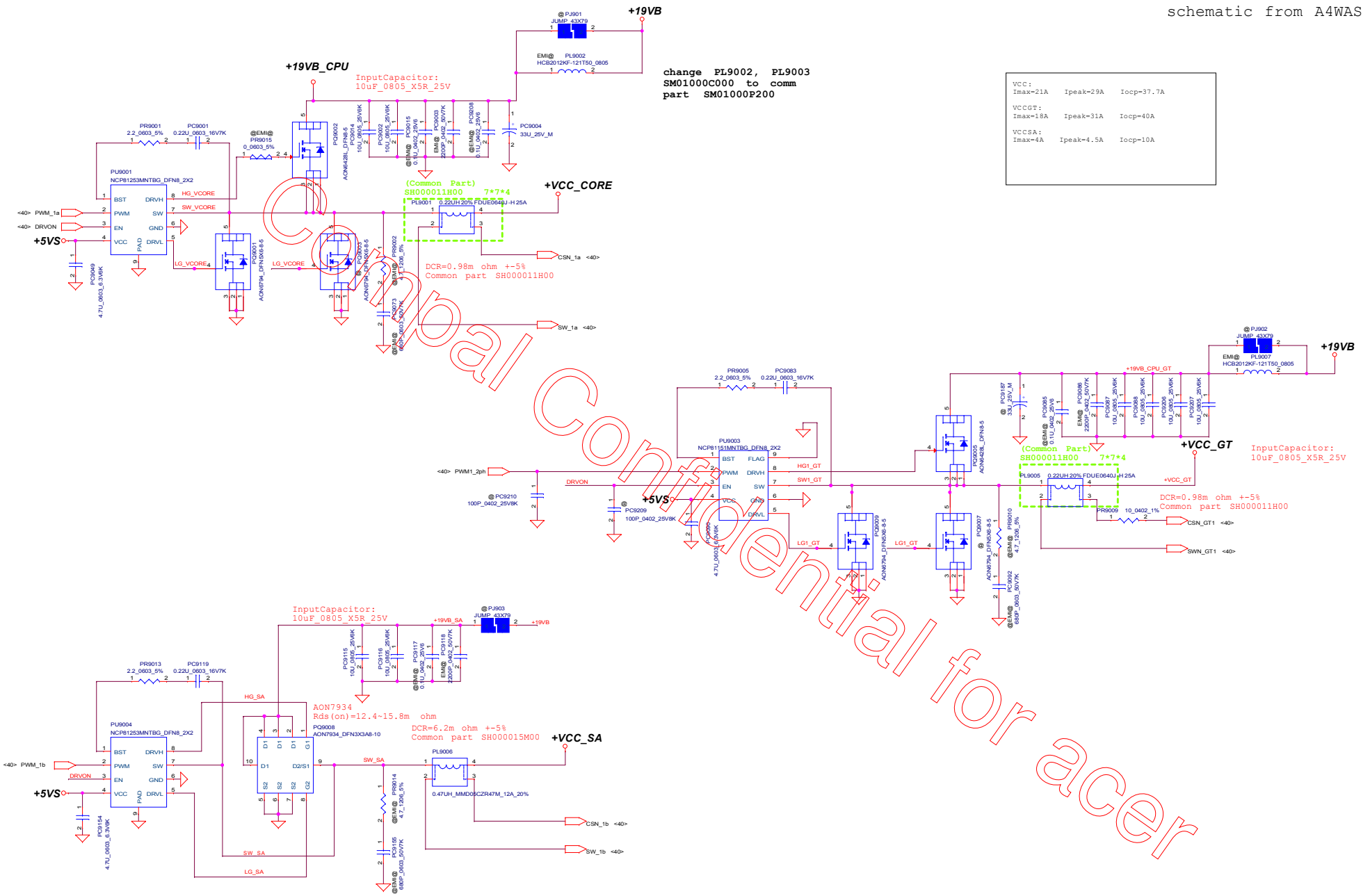
Compal Electronics, Inc.

Title: **IMVP8, NCP81206**

Size: C | Document Number: **B5W1S M/B LA-D671P** | Rev: 0.2

Date: Monday, July 18, 2016 | Sheet 40 of 44

schematic from A4WAS



Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2016/11/10

Compal Electronics, Inc.

Title: **Power Train**

Size	Document Number	Rev
C	B5W1S M/B LA-D671P	0.2

Date: Monday, July 18, 2016 Sheet 41 of 44

schematic from A4WAS

543016_543016_SKL_PDG_UY_1_0_pub
VCORE Output Capacitor:

22uF_0603*25
1uF_0201*35
220uF *1

UNPOP
22_0603_8PCS
330uF_R9_1PCS

Security Classification	Compal Secret Data		
Issued Date	2015/10/02	Deciphered Date	2016/11/10

Compal Electronics, Inc.
Title: Power Train
Size: C | Document Number: B5W1S M/B LA-D671P | Rev: 0.2
Date: Monday, July 18, 2016 | Sheet 42 of 44

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	CPU transient	modify transient set		P40	PR857 change to 100K ohm PR842 change to 34.8K ohm PR836 change to 66.5k ohm PR843 change to 715 ohm	4/12	DVT
02	BOM change	reduce BOM quantity			PR515, PR804, PR806, PR812, PR813. PR865. PR847. PR860, PR863, PR852, PR864, PR9015 change to R-Short	7/6	PVT
03	sequence	add RC to adjuct			PR501 change to 2.2K from R-short POP PC501to 0.1U		

Compal Electronics, Inc.
Title: PIR
Size: Custom | Document Number: B5W1S M/B LA-D671P | Rev: 0.2
Date: Monday, July 18, 2016 | Sheet 43 of 44

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
1	14,32	Load SW	4/15	For load SW output stable.	1. Add CC127, CQ5, CQ6.	DVT	0.2
2	29	EC	4/15	Update Board ID.	1. Change RB4 from 0 ohm to 12k ohm.	DVT	0.2
3	30	LED	4/15	Follow B5W1S LED brightness test.	1. Change RG4,RG11 to 1.24k ohm. 2. Change RG6,RG10 to 820 ohm.	DVT	0.2
4	20	Ripple	5/13	Improve +0.6VS DDR4 ripple quality.	1. Change CD64 from non-pop to pop.	DVT	0.2
5	14	Ripple	5/13	Improve +VCCIO & +1.0VS_VCCSTG ripple	1. Pop UC6. 2. Depop UC8 & CC126.	DVT	0.2
6		Standard part	5/18	Follow standard part.	Change Q1, Q2, Q6, QC2, QG1, QK1, QY1 from SB00000DH00 (S TR DMN66D0LDW-7 2N SOT363-6) to SB00000EO00 (S TR 2N7002KDW 2N SOT-363-6 PANJIT)	DVT	0.2
7	25	ESD diode	5/26	No spacing to add test point for ATE.	Change DA1,DA2 from reserve MESC5V02BD03_SOT23-3 to TVNST52302AB0_SOT523	DVT	0.2
8	23	Crystal cap	5/27	Fine tune 25MHz crystal to minimum frequency shif t.	Chagne CL17 from 12P_0402_50V8J to 10P_0402_50V8J	DVT	0.2
1		NPI test	7/6	For NPI test only.	1. Change RC125, RD43, RD44, RD45, RD52, RD54, RD56, RX10, RX11, RY1~RY5, RY7, RY8, RY10, RS21, RS22, RS24, RS25, RG8 from 0_0402 resistor to R-short 2. Change RL1, RL13, RB22 from 0_0805 to R-short	PVT	1.0
2	29	Board ID	7/6	Change board ID for PCB Rev1.0	Change RB4 from 12K_0402 to 15K_0402.	PVT	1.0
3	30	NPI test	7/14	For NPI test only.	Change SWK1 from pop to non-pop.	PVT	1.0
4	32	NPI test	7/15	To reduce +2.5V powe falling t i me	Reserve R31 & Q7 discharge circuit.	PVT	1.0