1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
<REV>	<ECN>	<ECO_DESCRIPTION>	<ECODATE>

SCHEM,MLB,VENUS,X425G

EVT 01/12/2015

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00383	1	SCHEM,MLB,VENUS,X425G	SCH	CRITICAL	
820-00163	1	PCBF,MLB,VENUS,X425G	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Mon Jan 12 16:34:40 2015

DRAWING TITLE: <PART_DESCRIPTION>
Apple Inc.
DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 1 OF 119
SHEET: 1 OF 97

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00042	COMMON PARTS,MLB,VENUS,X425G	X425_COMMON
985-00050	DEV BOM,MLB,VENUS,X425G	X425_DEVEL:ENG
639-00682	PCBA,MLB,VENUS,CTO,16GHYN,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:HYNIX_1600,FB_4G_HYNIX
639-00703	PCBA,MLB,VENUS,CTO,16GMIC,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:MICRON_1600,FB_4G_MICRON
639-00739	PCBA,MLB,VENUS,CTO,16GHYN,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:HYNIX_1600,FB_4G_MICRON
639-00740	PCBA,MLB,VENUS,CTO,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:CTO,RAM:MICRON_1600,FB_4G_HYNIX
639-00798	PCBA,MLB,VENUS,BEST,16GHYN,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:HYNIX_1600,FB_4G_HYNIX
639-00799	PCBA,MLB,VENUS,BEST,16GMIC,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:MICRON_1600,FB_4G_MICRON
639-00800	PCBA,MLB,VENUS,BEST,16GHYN,VR-4GMIC,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:HYNIX_1600,FB_4G_MICRON
639-00801	PCBA,MLB,VENUS,BEST,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,CPU_CRW:BEST,RAM:MICRON_1600,FB_4G_HYNIX
639-00803	PCBA,MLB,VENUS,NOCPU,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,GFX_BOM,RAM:MICRON_1600,FB_4G_HYNIX
639-00974	PCBA,MLB,NOGPU,CTO,16GMIC,VR-4GHYN,X425G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:MICRON_1600,FB_4G_HYNIX

X425 BOM Groups

BOM GROUP	BOM OPTIONS
X425_COMMON	ALTERNATE,COMMON,X425_COMMON1,X425_COMMON2,X425_PROGPARTS,ACAPS:A2
X425_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CPUPEG:X8X4X4,S2_PWR:S0,SMC_SUSACK:YES
X425_COMMON2	EDP:YES,XDP,SSD_PWR_EN:GPIO,CAM_WAKE:NO,SAMCONN,APCLKRQ:ISOL,CRW_SPRT,WLAN_SW:SIL
X425_PVT	BKLT:PROD,SENSOR_NONPROD:N
X425_PROGPARTS	SMC_PROG:BASE,BOOTROM_PROG:EVT,TBTROM:PROG,DPMUXMCU:PROG
X425_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,SENSOR_NONPROD:Y,SENSOR_NONPROD_R,BKLT:ENG,DBGLED,DPMUX_DEBUG,GPU_ROM:YES,SENSOR_GPU_NONPROD:Y
X425_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
X425_DEVEL:PVT	XDP_DEBUG
GFX_BOM	VENUS:XTA
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00058	1	CRW,SR1ZX,PRQ,C0,2.5,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:BEST
337S00059	1	CRW,SR1ZY,PRQ,C0,2.8,47W,4+3E,1.2,6M,BGA	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,QENV,LPT-M,HM87,C2,SR199,PRQ,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC,FCBGA288	U2800	CRITICAL	
338S1264	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S00032	32	IC,SDRAM,DDR3L-1600,4GBIT,78B FBGA		CRITICAL	HYNIX_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA		CRITICAL	MICRON_1600
337S00116	1	IC,GPU,VENUS XTAA1,QS,29X29MM,FCBGA962	U8400	CRITICAL	VENUS:XTA
333S00027	4	IC,GDDR5,4GBIT,6GBPS,1.5V,25NM,BGA170	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_HYNIX
333S0766	4	IC,GDDR5,4GBIT,6GBPS,128MX32,25NM,170BGA	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_MICRON

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:HYNIX_1600	HYNIX_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:MICRON_1600	MICRON_1600,RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L

COMMON/DEVEL BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00042	1	COMMON PARTS,MLB,VENUS,X425G	BASE	CRITICAL	BASE_BOM
985-00050	1	DEV,MLB,VENUS,X425G	DEVEL	CRITICAL	DEVEL_BOM

SYNC_MASTER=CLEAN_X305 SYNC_DATE=05/30/2014

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 2 OF 119

SHEET: 2 OF 97

Programmables - All builds

335S0915	1	IC,SERIAL SPI FLASH ROM,4MBIT,50MHZ,USON	U2890	CRITICAL	TBTROM:BLANK
341S00166	1	T29,FALCON RIDGE(V27.1)PROTO0,X425G	U2890	CRITICAL	TBTROM:PROG
335S0724	1	1MBIT SERIAL FLASH 2X3X0.6MM UFDFPN8 PKG	U9101	CRITICAL	GPUROM:BLANK
341S3565	1	IC,EDP MUX-95C,(RENESAS) V3.2.8,DVB,D2	U9600	CRITICAL	DPMUXMCU:PROG
337S4313	1	IC,MCU,H8S/2113,9X9MM,TLP-145V	U9600	CRITICAL	DPMUXMCU:BLANK

SMC

338S1214	1	IC,SMC-B1,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BLANK
341S00157	1	IC,SMC-B1,EXT (V2.25A9) PROTO 0,X425G	U5000	CRITICAL	SMC_PROG:BASE

EFI ROM

335S00007	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:WIN
335S00006	1	IC,SERIAL FLASH,64MB,3V,WSON,6X5MM	U6100	CRITICAL	BOOTROM_BLANK:MAC
341S00239	1	IC,EFI ROM (V0145) EVT,X425	U6100	CRITICAL	BOOTROM_PROG:EVT

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1053	376S0604		ALL	Diodes alt to Fairchild
128S0311	128S0329		ALL	NEC alt to Sanyo
138S0739	138S0706		ALL	Samsung alt to Murata
197S0481	197S0480		ALL	Epson Alt to NDK
197S0478	197S0479		ALL	NDK Alt to Epson
371S0713	371S0558		ALL	DDS alt to ST
152S0461	152S1645		ALL	Cyntec alt to Vishay
376S1080	376S0820		ALL	Diodes alt to On Semi
155S0667	155S00008		ALL	Panasonic alt to TDK
376S00074	376S0855		ALL	Toshiba alt to Diodes
376S1129	376S0855		ALL	NXP alt to Diodes
376S1089	376S1128		ALL	NXP alt to Diodes
128S0371	128S0376		ALL	Kemet alt to Sanyo
138S0803	138S0639		ALL	Samsung alt to Murata
138S0843	138S0674		ALL	Samsung alt to Murata
138S0846	138S0811		ALL	Samsung alt to Murata
127S0164	127S0162		ALL	Rohm alt to Vishay
138S0732	138S0715		ALL	Rohm alt to Vishay
128S0364	128S0264		ALL	Kemet alt to Sanyo
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000
311S0649	311S0541		ALL	ON alt to Toshiba
376S00014	376S0761		ALL	Toshiba alt to Vishay
740S00003	740S0135		ALL	AEM alt to Tyco
740S00004	740S0134		ALL	AEM alt to Littlefuse
107S00029	107S00030		ALL	TFT alt to Cyntec
128S0398	128S0220		ALL	Kemet alt to Sanyo
128S0386	128S0284		ALL	Kemet alt to Sanyo
311S00008	311S0271		ALL	Diodes alt to NXP
128S0393	128S0334		ALL	Kemet alt to Sanyo
311S00007	311S0426		ALL	Diodes alt to NXP
371S00017	371S0749		ALL	Diodes alt to Onsemi
107S00033	107S00034		ALL	TFT alt to Cyntec
107S0240	107S0255		ALL	TFT alt to Cyntec
107S0248	107S0250		ALL	TFT alt to Cyntec
107S00031	107S00032		ALL	TFT alt to Cyntec
107S0249	107S0251		ALL	TFT alt to Cyntec
107S00037	107S00038		ALL	TFT alt to Cyntec
107S00015	107S00011		ALL	TFT alt to Cyntec
128S00008	128S0380		ALL	NEC alt to Sanyo
311S00060	311S0273		ALL	Diodes alt to NXP
353S00133	353S2741		ALL	ON Semi alt to TI
353S00394	353S2162		ALL	ON Semi alt to TI
376S00086	376S0761		ALL	Diodes alt to Vishay
112S00001	112S0254		ALL	Yageo alt to Cyntec
353S00095	353S3328		ALL	Pericom alt to TI
128S0397	128S0325		ALL	Kemet alt to Sanyo
311S00004	311S0370		ALL	ON Semi alt to NXP

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: BOM Configuration

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

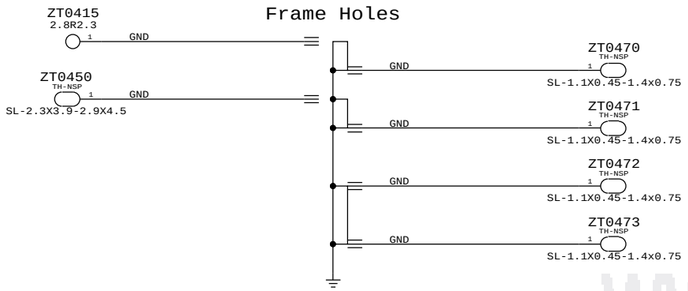
REVISION: <E4LABEL>

BRANCH: <BRANCH>

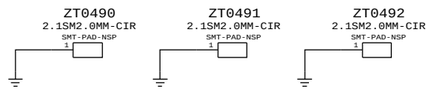
PAGE: 3 OF 119

SHEET: 3 OF 97

Frame Holes



SMT GND TEST PONTS



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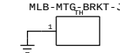


X305G THERMAL MODULE STANDOFF

APN 860-3690
SH0424
STDOFF-4.5OD1.9H-SM-1

APN 817-0688
SH0446
STDOFF-4.9OD2.38H-SM-2

APN 817-0741
SH0445
STDOFF-4.9OD2.38H-SM-SL-2.6X2NP-2

GPU BOSS APN 860-4772

SH0430
4.5OD1.85ID-1.95H

SH0427
4.5OD1.85ID-1.95H

SH0428
4.5OD1.85ID-1.95H

GPU BOSS APN 817-4517

SH0421
4.5OD1.85ID-1.95H-1

FAN BOSS APN 860-3428

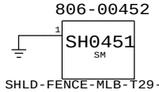
SH0425
STDOFF-4.5OD1.8H-SM-1

SH0423
STDOFF-4.5OD1.8H-SM-1

APN 806-9391

SHLD-MLB-USB-J45

806-00452



SHLD-FENCE-MLB-T29-X305

CPU BOSS APN 860-2931

SH0429
5.00D1.85ID-2.35H

SH0420
5.00D1.85ID-2.35H

SH0422
5.0OD1.85ID-2.35H

SH0426
5.00D1.85ID-2.35H

PD parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	

Thermal Module gaskets APN 875-9290

OMIT
CG0400
6.0OD3.9H-SM

OMIT
CG0402
6.0OD3.9H-SM

OMIT
CG0401
6.0OD3.9H-SM

OMIT
CG0403
6.0OD3.9H-SM

X305G POGO PINS

APN 870-2451

SH0431
POGO-2.3OD-5.5H-X304

SH0432
POGO-2.3OD-5.5H-X304

SH0433
POGO-2.3OD-5.5H-X304

SH0434
POGO-2.3OD-5.5H-X304

SH0435
POGO-2.3OD-5.5H-X304

SH0437
POGO-2.3OD-5.5H-X304

X305G STANDOFF

APN 860-1448

SH0440
2.9OD1.2ID-1.35H-SM

SH0441
2.9OD1.2ID-1.35H-SM

SH0444
2.9OD1.2ID-1.35H-SM

SH0460
2.9OD1.2ID-1.35H-SM

SH0461
2.9OD1.2ID-1.35H-SM

SH0463
2.9OD1.2ID-1.35H-SM

SH0464
2.9OD1.2ID-1.35H-SM

SH0442
2.9OD1.2ID-1.35H-SM

SH0443
2.9OD1.2ID-1.35H-SM

SH0462
2.9OD1.2ID-1.35H-SM

SH0465
2.9OD1.2ID-1.35H-SM

SH0466
2.9OD1.2ID-1.35H-SM

SH0467
2.9OD1.2ID-1.35H-SM

RIO FLEX BRACKET BOSS (860-00166)

SH0480
3.5OD1.85ID-2.0H

SH0481
3.5OD1.85ID-2.0H

IPD FLEX BRACKET BOSS (860-00166)

SH0482
3.5OD1.85ID-2.0H

SH0483
3.5OD1.85ID-2.0H

SYNC_MASTER=CLEAN_X305G
SYNC_DATE=08/08/2014

PAGE TITLE
PD Parts

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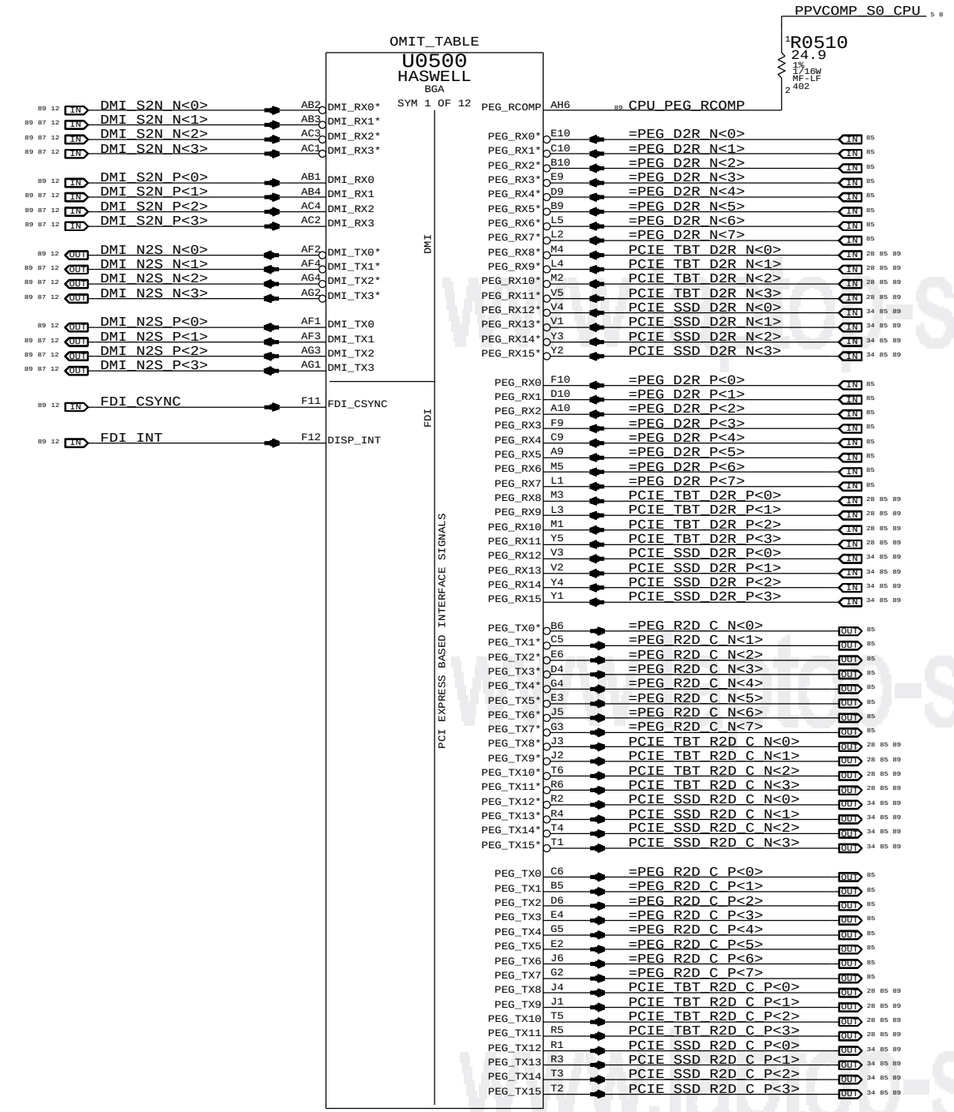
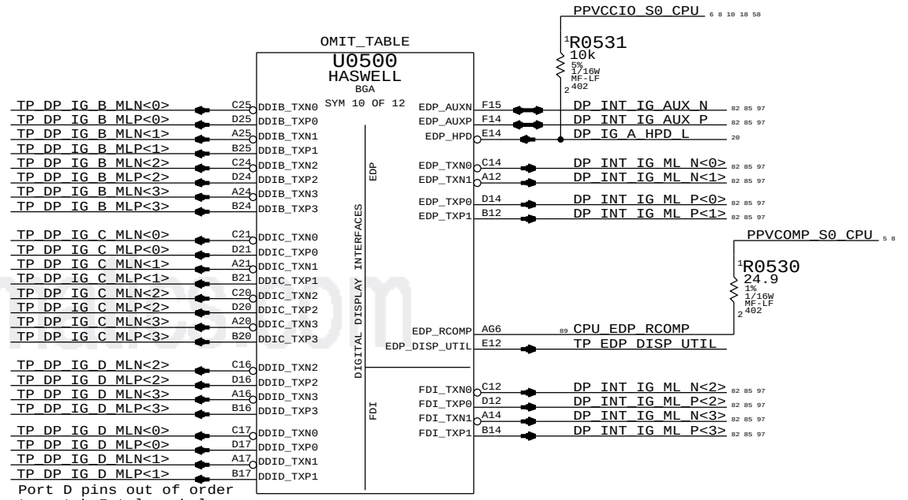
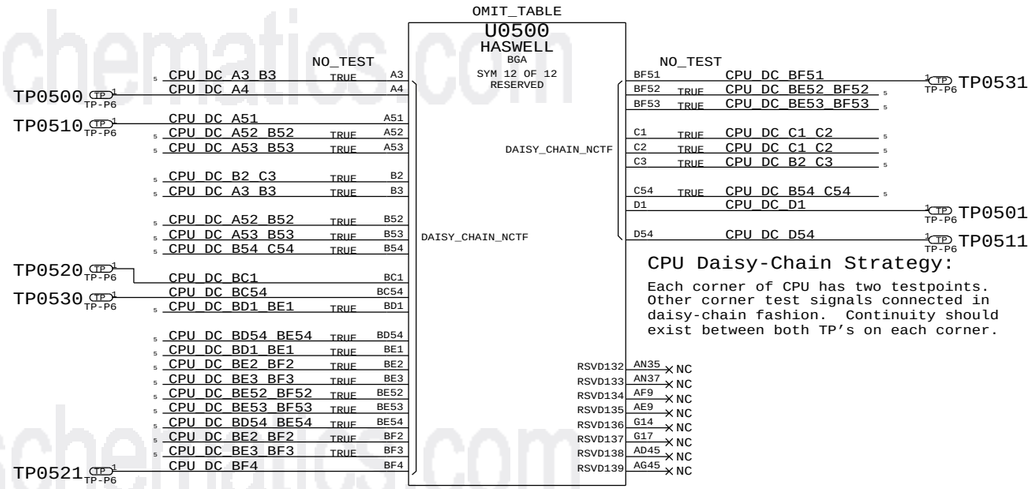
PAGE 4 OF 119
SHEET 4 OF 97







SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

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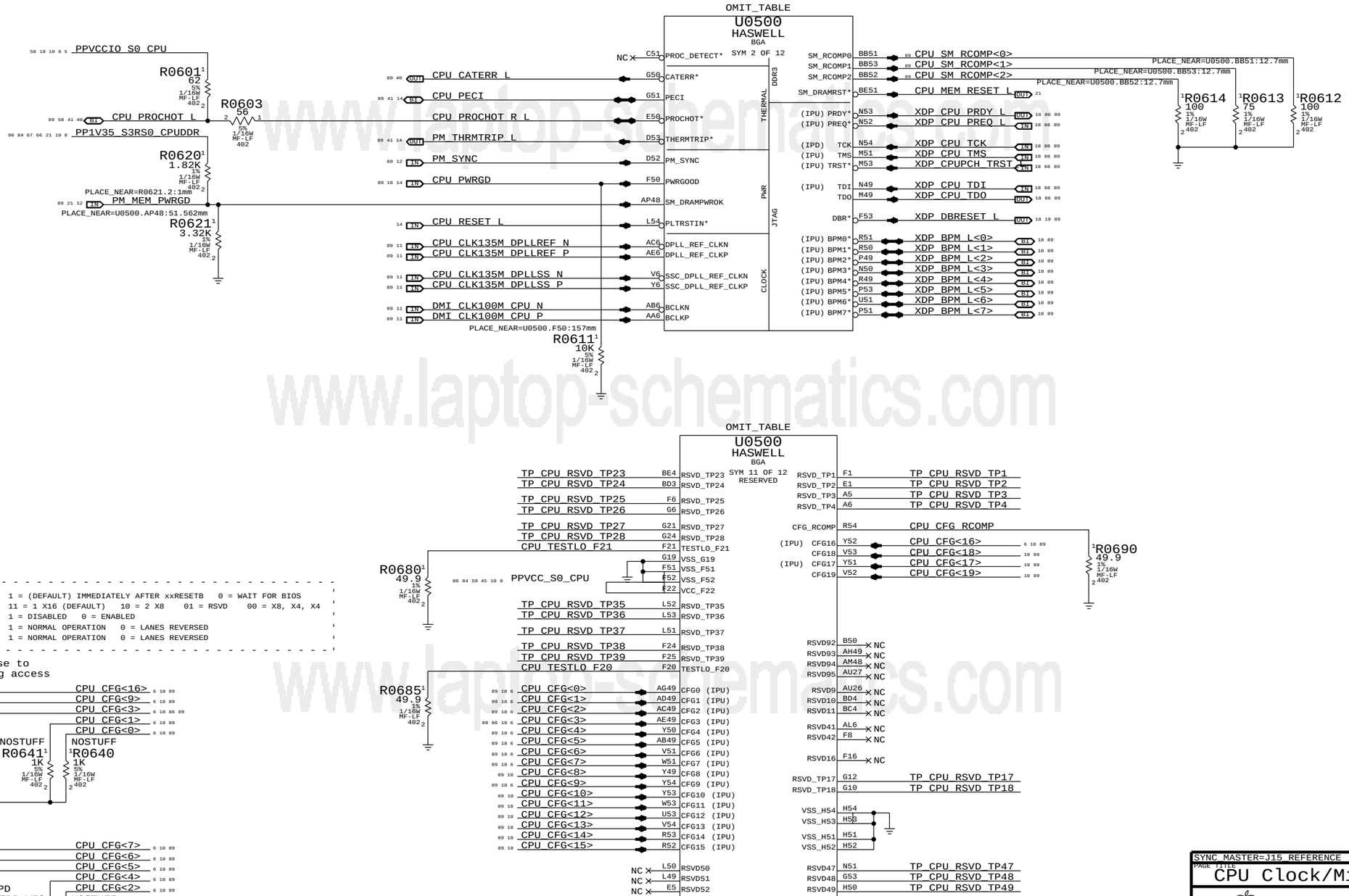
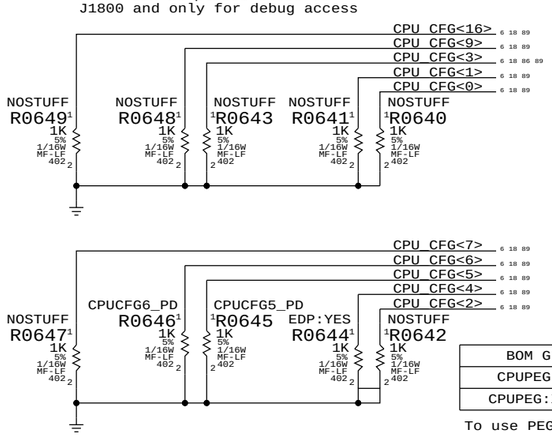
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 5 OF 119
SHEET 5 OF 97



CFG [7] :PEG DEFER TRAINING — 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION — 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE — 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: CPU Clock/Misc/JTAG/CFG

Apple Inc.

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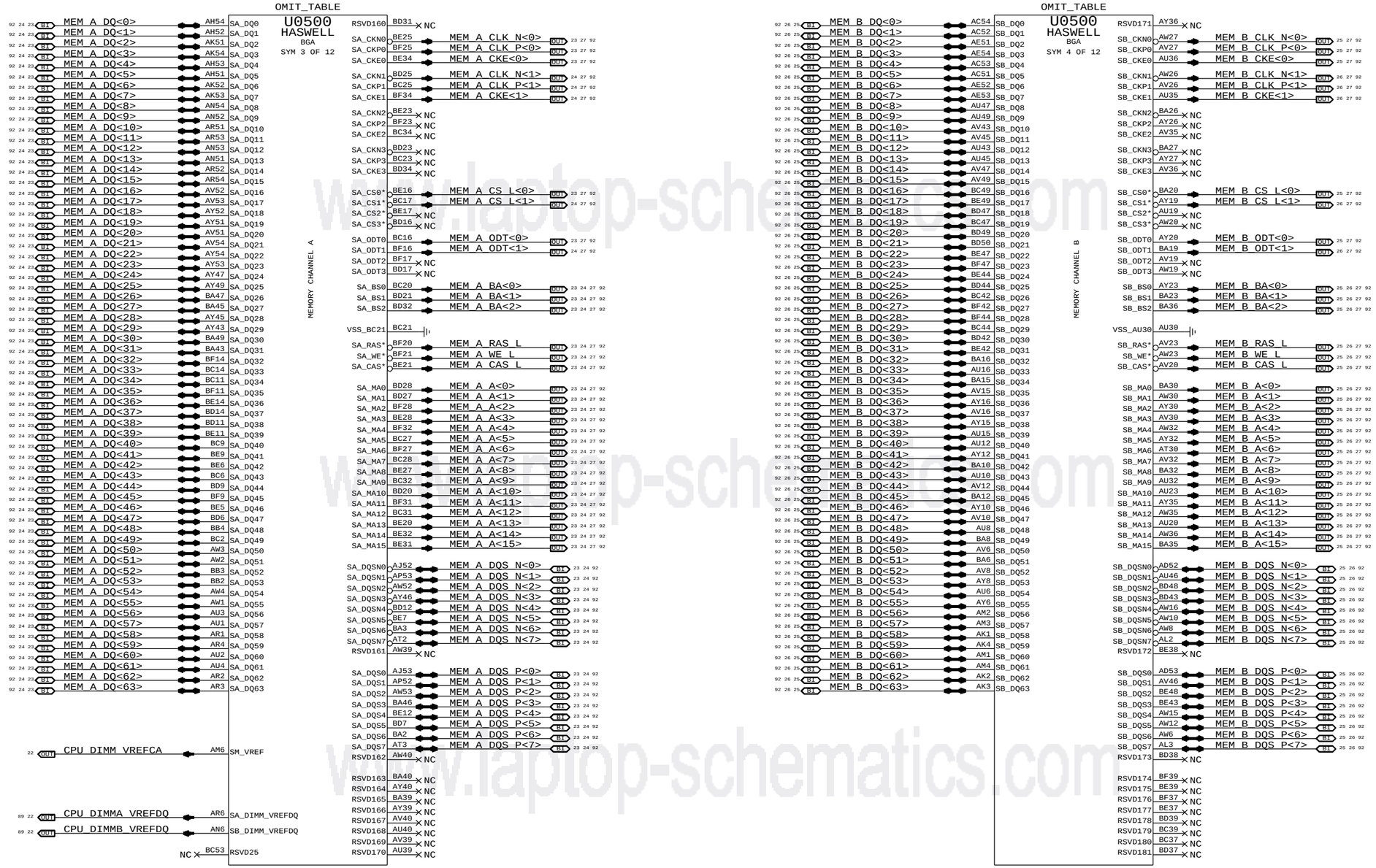
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 6 OF 119
SHEET: 6 OF 97



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PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

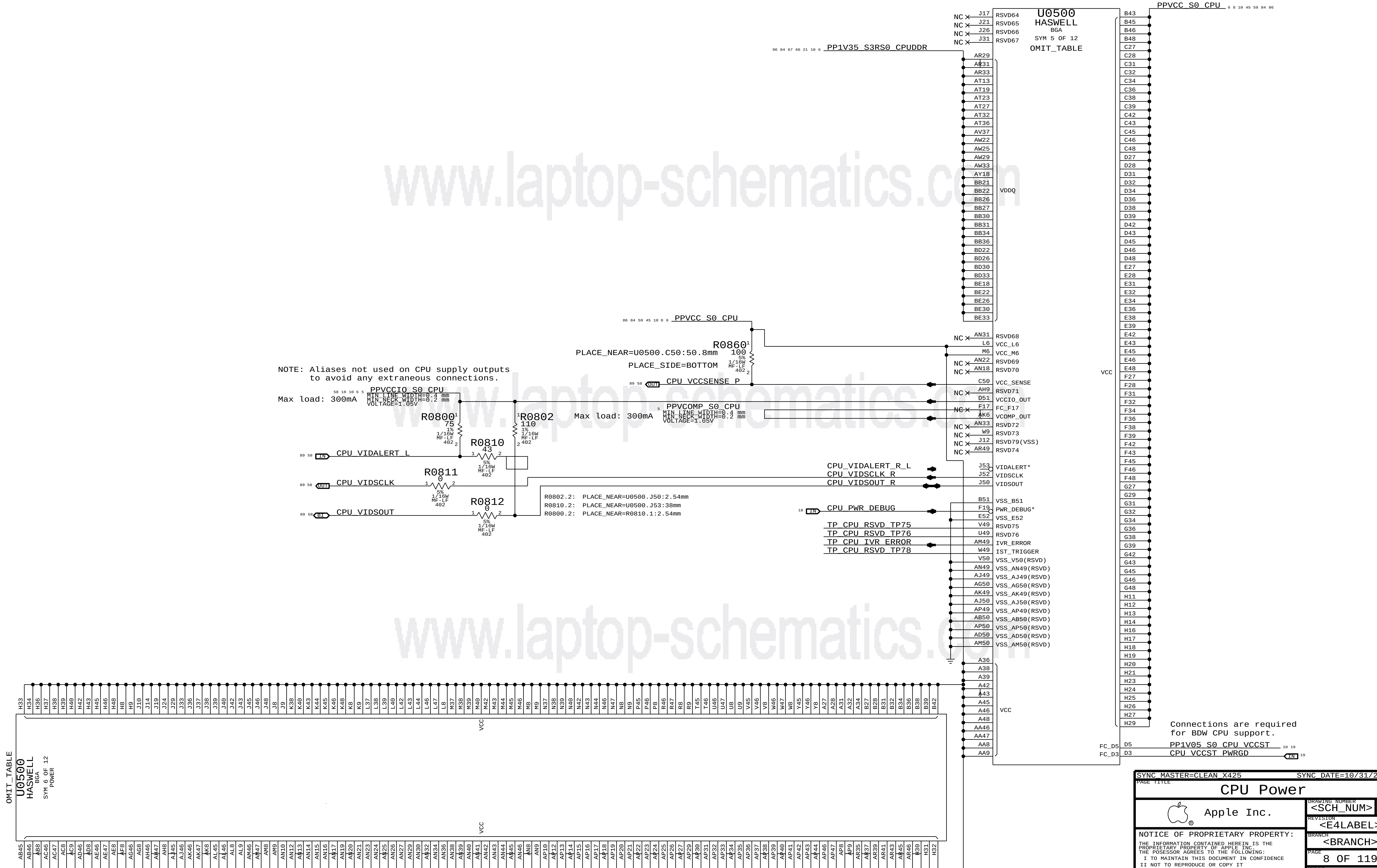
DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 7 OF 119

SHEET 7 OF 97



SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/31/2014

PAGE TITLE

CPU Power

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

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U0500
HASWELL
BGA
SYM 7 OF 12
GROUND

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OMIT_TABLE

U0500
HASWELL
BGA
SYM 8 OF 12
GROUND

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OMIT_TABLE

U0500
HASWELL
BGA
SYM 9 OF 12

VSS: G20, G23, G25, G26, G30, G33, G37, G40, G44, G49, G52, G54, G7, G8, G9, H44, H49, H7, J44, J49, J51, J54, J7, K1, K2, K3, K4, K5, K6, K7, L48, L7, L9, M48, M50, M52, M54, M7, N48, N7, P1, P2, P3, P4, P48, P5, P50, P52, P54, P6, P7, R48, R7, T48, U1, U2, U3, U4, U48, U5, U50, U52, U54, U6, U7, V48, V7, V9, W48, W50, W52, W54, W7, Y48, Y7, Y9

VSS_AR22(RSVD): AR22
VSS_AB48(RSVD): AB48
VSS_P9(RSVD): P9
VSS_G18(RSVD): G18

VSS_NCTF: A49, A50, A8, B4, BA1, BA54, BB1, BB54, BD2, BD53, BF49, BF5, BF50, BF6, C53, D2, E54, F54, G1

VSS_SENSE: D50

CPU_VCCSENSE_N (OUT) 58 89

R0960
100
5%
1/16W
MF-LF
402
PLACE_NEAR=U0500.D50:50.8mm
PLACE_SIDE=BOTTOM

VSS: BC10, BC12, BC15, BC18, BC22, BC26, BC3, BC30, BC33, BC36, BC38, BC41, BC43, BC46, BC48, BC5, BC50, BC52, BC7, BD10, BD15, BD18, BD36, BD41, BD46, BD5, BD51, BE10, BE15, BE36, BE41, BE46, BF10, BF12, BF15, BF18, BF22, BF26, BF30, BF33, BF36, BF38, BF41, BF43, BF46, BF48, BF7, C11, C15, C19, C22, C26, C30, C33, C37, C4, C40, C44, C49, C52, C8, D11, D15, D19, D22, D26, D30, D33, D37, D40, D44, D49, D8, E11, E15, E16, E17, E19, E20, E21, E22, E24, E25, E26, E30, E33, E37, E40, E44, E49, E51, E53, E8, F2, F26, F3, F30, F33, F37, F4, F40, F44, F49, F5, G11, G13, G16

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE: CPU Ground

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 9 OF 119
SHEET: 9 OF 97

CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

86 84 59 45 8 6 PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402
C1001 1UF 10% 10V X6S-CERM 0402
C1002 1UF 10% 10V X6S-CERM 0402
C1003 1UF 10% 10V X6S-CERM 0402
C1004 1UF 10% 10V X6S-CERM 0402
C1005 1UF 10% 10V X6S-CERM 0402
C1006 1UF 10% 10V X6S-CERM 0402
C1007 1UF 10% 10V X6S-CERM 0402
C1008 1UF 10% 10V X6S-CERM 0402
C1009 1UF 10% 10V X6S-CERM 0402
C1010 1UF 10% 10V X6S-CERM 0402
C1011 1UF 10% 10V X6S-CERM 0402
C1012 1UF 10% 10V X6S-CERM 0402
C1013 1UF 10% 10V X6S-CERM 0402
C1014 1UF 10% 10V X6S-CERM 0402
C1015 1UF 10% 10V X6S-CERM 0402
C1016 1UF 10% 10V X6S-CERM 0402
C1017 1UF 10% 10V X6S-CERM 0402
C1018 1UF 10% 10V X6S-CERM 0402
C1019 1UF 10% 10V X6S-CERM 0402

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side

ACAPS:A2
CAPS for Acoustic Control (C109A to C102D)

C1020 20UF 20% 2.5V X6S-CERM 0402
C1021 20UF 20% 2.5V X6S-CERM 0402
C1022 20UF 20% 2.5V X6S-CERM 0402
C1023 20UF 20% 2.5V X6S-CERM 0402

NO STUFF NO STUFF NO STUFF NO STUFF NO STUFF ACAPS:A1 ACAPS:A1 ACAPS:A2 ACAPS:A1 ACAPS:A1 ACAPS:A1 NO STUFF ACAPS:A1 NO STUFF NO STUFF ACAPS:A2

CRITICAL C109A 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C109B 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C109C 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C109D 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C109E 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C109F 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C101A 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C101B 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C101C 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C101D 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C101E 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C101F 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C102A 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C102B 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C102C 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C102D 20UF 20% 2.5V X6S-CERM 0402

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

ACAPS:A2

NO STUFF NO STUFF

CRITICAL C1024 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1025 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1026 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1027 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1028 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1029 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1030 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1031 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1032 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1033 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1034 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1035 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1036 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1037 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1038 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1039 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1040 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1041 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1042 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1043 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1044 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1045 20UF 20% 2.5V X6S-CERM 0402

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

ACAPS:A1 ACAPS:A2 ACAPS:A1 ACAPS:A1 ACAPS:A2 ACAPS:A2 ACAPS:A1 ACAPS:A2 NO STUFF ACAPS:A2 ACAPS:A2 ACAPS:A1 ACAPS:A1

CRITICAL C1046 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1047 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1048 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1049 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1050 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1051 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1052 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1053 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1054 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1055 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1056 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1057 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1058 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1059 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1060 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1061 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1062 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1063 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1064 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1065 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1066 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C1067 20UF 20% 2.5V X6S-CERM 0402

NO STUFF NO STUFF NO STUFF

PLACEMENT_NOTE (C1068-C1076:
Place near inductors on bottom side.

CAPS for Acoustic Control (C102E to C103F)
ACAPS:A2 NO STUFF NO STUFF ACAPS:A2 NO STUFF NO STUFF ACAPS:A2

CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1069 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1070 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1071 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1072 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1073 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1074 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1075 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1076 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1077 330UF-9MOHM 20% 2.5V POLY-TANT D1ST-1
CRITICAL C102E 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C102F 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C103A 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C103B 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C103C 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C103D 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C103E 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C103F 20UF 20% 2.5V X6S-CERM 0402
CRITICAL C108D 12PF 5% 50V NP0-C0G 0201
CRITICAL C108E 12PF 5% 50V NP0-C0G 0201
CRITICAL C107A 3.0PF +/-0.1PF 25V NP0-C0G 0201

FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 3x 270uF, 8x 10uF 0603, 10x 1uF 0402

67 66 23 8 6 96 84 PP1V35_S3RS0_CPUDDR

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402
C1081 1UF 10% 10V X6S-CERM 0402
C1082 1UF 10% 10V X6S-CERM 0402
C1083 1UF 10% 10V X6S-CERM 0402
C1084 1UF 10% 10V X6S-CERM 0402
C1085 1UF 10% 10V X6S-CERM 0402
C1086 1UF 10% 10V X6S-CERM 0402
C1087 1UF 10% 10V X6S-CERM 0402
C1088 1UF 10% 10V X6S-CERM 0402
C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S 0402
C1091 10UF 20% 4V X6S 0402
C1092 10UF 20% 4V X6S 0402
C1093 10UF 20% 4V X6S 0402
C1094 10UF 20% 4V X6S 0402
C1095 10UF 20% 4V X6S 0402
C1096 10UF 20% 4V X6S 0402
C1097 10UF 20% 4V X6S 0402
CRITICAL C108B 12PF 5% 50V NP0-C0G 0201
CRITICAL C108C 12PF 5% 50V NP0-C0G 0201
CRITICAL C107B 3.0PF +/-0.1PF 25V NP0-C0G 0201

FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C1099 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C108A 270UF 20% 2V TANT CASE-B2-SM
(Z = 2mm, place on tall side next to CPU & under heat pipe)

C1098, C1099 and C108A use B size caps due to EG board placement constraints.

CPU VCCIO Decoupling

Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

58 18 8 6 5 PPVCCIO_S0_CPU

C1079 0.01UF 10% 16V X7R-CERM 0402

CPU VCCST Decoupling

Intel recommendation: 1x 0.1uF 0402, 1x 4.7uF 0805
Apple Implementation: 1x 0.1uF 0201, 1x 4.7uF 0402

86 84 67 62 41 18 17 15 14 PP1V05_S0

BDW_SPRT R1080 0 5% 1/10W MF-LF 603

PP1V05_S0_CPU_VCCST
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

PLACE_NEAR=U0500.D5:25.4mm
PLACE_NEAR=U0500.D5:12.7mm

BDW_SPRT C106A 0.1UF 10% 6.3V CERM-X5R 0201
BDW_SPRT C106B 4.7UF 20% 6.3V X5R 402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC_MASTER=CLEAN_X305G SYNC_DATE=08/11/2014
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 10 OF 119
SHEET: 10 OF 97

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(1 OF 11)

SYSCLK_CLK32K_RTC — B5 RTCX1; NC — B4 RTCX2

RTC:
- PCH_SRTCRST_L — B9 SRTCRST*
- PCH_INTRUDER_L — A8 INTRUDER*
- PCH_INTVRMEN_L — G10 INTVRMEN
- RTC_RESET_L — D9 RTCRST*

AZALIA:
- HDA_BIT_CLK — R1110 33 — HDA_BIT_CLK_R — B25 HDA_BCLK
- HDA_SYNC — R1111 33 — HDA_SYNC_R — A22 HDA_SYNC (IPD-boot)
- PCH_SPKR — AL10 SPKR (IPD-PLTRST#)
- HDA_RST_L — R1112 33 — HDA_RST_R_L — C24 HDA_RST*
- HDA_SDIN0 — L22 HDA_SDI0 (IPD)
- NC_HDA_SDIN1 — K22 HDA_SDI1 (IPD)
- NC_HDA_SDIN2 — G22 HDA_SDI2 (IPD)
- NC_HDA_SDIN3 — F22 HDA_SDI3 (IPD)
- HDA_SDOUT — R1113 33 — HDA_SDOUT_R — A24 HDA_SDO (IPD-boot)

PLACE_NEAR=U1100.B25:1.27mm
PLACE_NEAR=U1100.A22:1.27mm
PLACE_NEAR=U1100.C24:1.27mm
PLACE_NEAR=U1100.A24:1.27mm

- DP_TBT_SEL — B17 DOCKEN*/GPIO33 (IPD-DOCKEN#2)
- ENET_MEDIA_SENSE_RDIV — C22 HDA_DOCK_RST*/GPIO13

JTAG:
- XDP_PCH_TCK — AB3 JTAG_TCK (IPD)
- XDP_PCH_TMS — AD1 JTAG_TMS (IPU)
- XDP_PCH_TDI — AE2 JTAG_TDI (IPU)
- XDP_PCH_TDO — AD3 JTAG_TDO

NC — F8 TP25; NC — C26 TP22; NC — AB6 TP20

SATA:
- SATA_RXN0 BC8 — NC_SATA_A_D2RN
- SATA_RXP0 BE8 — NC_SATA_A_D2RP
- SATA_TXN0 AW8 — NC_SATA_A_R2D_CN
- SATA_TXP0 AY8 — NC_SATA_A_R2D_CP
- SATA_RXN1 BC10 — NC_SATA_B_D2RN
- SATA_RXP1 BE10 — NC_SATA_B_D2RP
- SATA_TXN1 AV10 — NC_SATA_B_R2D_CN
- SATA_TXP1 AW10 — NC_SATA_B_R2D_CP
- SATA_RXN2 BB9 — NC_SATA_ODD_D2RN
- SATA_RXP2 BD9 — NC_SATA_ODD_D2RP
- SATA_TXN2 AY13 — NC_SATA_ODD_R2D_CN
- SATA_TXP2 AW13 — NC_SATA_ODD_R2D_CP
- SATA_RXN3 BC12 — NC_SATA_D_D2RN
- SATA_RXP3 BE12 — NC_SATA_D_D2RP
- SATA_TXN3 AR13 — NC_SATA_D_R2D_CN
- SATA_TXP3 AT13 — NC_SATA_D_R2D_CP
- SATA_RXN4/PERN1 BD13 — TP_PCIE_ENET_D2RN
- SATA_RXP4/PERP1 BB13 — TP_PCIE_ENET_D2RP
- SATA_TXN4/PETN1 AV15 — TP_PCIE_ENET_R2D_CN
- SATA_TXP4/PETP1 AW15 — TP_PCIE_ENET_R2D_CP
- SATA_RXN5/PERN2 BC14 — NC_SATA_F_D2RN
- SATA_RXP5/PERP2 BE14 — NC_SATA_F_D2RP
- SATA_TXN5/PETN2 AP15 — NC_SATA_F_R2D_CN
- SATA_TXP5/PETP2 AR15 — NC_SATA_F_R2D_CP
- SATA_RCOMP AY5 — PCH_SATA_RCOMP
- SATALED* AP3 — PCH_SATALED_L
- SATA0GP/GPIO21 AT1 — XDP_DC0_DP_AUXCH_ISOL_L
- SATA1GP/GPIO19 (IPU-PLTRST#) AU2 — XDP_DC1_SATARDRVR_EN
- SATA_IREF BD4

TP9 BA2 — NC; TP8 BB2 — NC

SATA Port assignments:

Primary HDD/SSD (SATA only)

Secondary HDD/SSD (SATA only)

Reserved: ODD

Unused

PCIe:
Reserved: Ethernet
(if not combo w/SD Card)

PP1V5_S0 — R1130 7.5K 1% 1/20W MF 201 — PCH_SATA_RCOMP
PLACE_NEAR=U1100.AY5:2.54mm

Unused

NOTE: ENET pair only used if SD Card Reader is USB3.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(2 OF 11)

CLOCKS:
- PCIE_CLK100M_SSD_N — Y43 CLKOUT_PCIE_N0
- PCIE_CLK100M_SSD_P — Y45 CLKOUT_PCIE_P0
- SSD_CLKREQ_L — AB1 PCIECLKRQ0*/GPIO73
- NC_PCIE_CLK100M_ENETSDN — AA44 CLKOUT_PCIE_N1
- NC_PCIE_CLK100M_ENETSDP — AA42 CLKOUT_PCIE_P1
- XDP_DD2_ENETSD_CLKREQ_L — AF1 PCIECLKRQ1*/GPIO18
- PCIE_CLK100M_AP_N — AB43 CLKOUT_PCIE_N2
- PCIE_CLK100M_AP_P — AB45 CLKOUT_PCIE_P2
- XDP_DD3_AP_CLKREQ_L — AF3 PCIECLKRQ2*/GPIO20/SMI*
- PCIE_CLK100M_CAMERA_N — AD43 CLKOUT_PCIE_N3
- PCIE_CLK100M_CAMERA_P — AD45 CLKOUT_PCIE_P3
- CAMERA_CLKREQ_L — T3 PCIECLKRQ3*/GPIO25
- PEG_CLK100M_N — AF43 CLKOUT_PCIE_N4
- PEG_CLK100M_P — AF45 CLKOUT_PCIE_P4
- TBT_CLKREQ_L — V3 PCIECLKRQ4*/GPIO26
- NC_PCIE_CLK100M_PE5N — AE44 CLKOUT_PCIE_N5
- NC_PCIE_CLK100M_PE5P — AE42 CLKOUT_PCIE_P5
- PCH_CLKRQ5_L_GPIO44 — AA2 PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
- NC_PCIE_CLK100M_SWN — AB40 CLKOUT_PCIE_N6
- NC_PCIE_CLK100M_SWP — AB39 CLKOUT_PCIE_P6
- PEG_CLKREQ_L — AE4 PCIECLKRQ6*/GPIO45
- PCIE_CLK100M_TBT_N — AJ44 CLKOUT_PCIE_N7
- PCIE_CLK100M_TBT_P — AJ42 CLKOUT_PCIE_P7
- PCH_CLKRQ7_L_GPIO46 — Y3 PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
- NC_ITPXDP_CLK100MN — AH43 CLKOUT_ITPXDP_N
- NC_ITPXDP_CLK100MP — AH45 CLKOUT_ITPXDP_P
- LPC_CLK33M_SMC_R — D44 CLKOUT_33MHZ0 (IPD-PWROK)
- NC_LPC_CLK33M_LPCPLUS_R — E44 CLKOUT_33MHZ1 (IPD-PWROK)
- LPC_CLK33M_DPMUX_UC_R — B42 CLKOUT_33MHZ2 (IPD-PWROK)
- NC_PCI_CLK33M_OUT3 — F41 CLKOUT_33MHZ3 (IPD-PWROK)
- PCH_CLK33M_PCIOUT — A40 CLKOUT_33MHZ4 (IPD-PWROK)

- CLKOUT_PEG_A_N AB35 — NC_PCIE_CLK100M_ENETN
- CLKOUT_PEG_A_P AB36 — NC_PCIE_CLK100M_ENETP
- PEG_A_CLKRQ*/GPIO47 AF6 — ENET_CLKREQ_L
- CLKOUT_PEG_B_N Y39 — NC_PCIE_CLK100M_PEGBN
- CLKOUT_PEG_B_P Y38 — NC_PCIE_CLK100M_PEGBP
- PEG_B_CLKRQ*/GPIO56 U4 — PCH_PEGCLKRQB_L_GPIO56
- CLKOUT_DMI_N AF39 — DMI_CLK100M_CPU_N
- CLKOUT_DMI_P AF40 — DMI_CLK100M_CPU_P
- CLKOUT_DP_N AJ40 — CPU_CLK135M_DPLLSS_N
- CLKOUT_DP_P AJ39 — CPU_CLK135M_DPLLSS_P
- CLKOUT_DPNS_N AF35 — CPU_CLK135M_DPLLREF_N
- CLKOUT_DPNS_P AF36 — CPU_CLK135M_DPLLREF_P
- CLKIN_DMI_N AY24 — PCIE_CLK100M_PCH_N
- CLKIN_DMI_P AW24 — PCIE_CLK100M_PCH_P
- CLKIN_GND_N AR24 — PCH_CLKIN_GNDN
- CLKIN_GND_P AT24 — PCH_CLKIN_GNDP
- CLKIN_DOT96_N H33 — PCH_CLK96M_DOT_N
- CLKIN_DOT96_P G33 — PCH_CLK96M_DOT_P
- CLKIN_SATA_N BE6 — PCH_CLK100M_SATA_N
- CLKIN_SATA_P BC6 — PCH_CLK100M_SATA_P
- REFCLK14IN F45 — PCH_CLK14P3M_REFCLK
- CLKIN_33MHZLOOPBACK D17 — PCH_CLK33M_PCIIN
- XTAL25_IN AM43 — SYSCLK_CLK25M_SB_R
- XTAL25_OUT AL44 — NC

Unused clock terminations for FCIM Mode

R1196 10K — PCIE_CLK100M_PCH_N
R1195 10K — PCIE_CLK100M_PCH_P
R1171 10K — PCH_CLKIN_GNDN
R1170 10K — PCH_CLKIN_GNDP
R1192 10K — PCH_CLK96M_DOT_N
R1191 10K — PCH_CLK96M_DOT_P
R1194 10K — PCH_CLK100M_SATA_N
R1193 10K — PCH_CLK100M_SATA_P
R1197 10K — PCH_CLK14P3M_REFCLK

R1172 340 1% 1/16W MF-LF 402 — SYSCLK_CLK25M_SB
1.5V -> 1.1V
R1173 1K 1% 1/20W MF 201

- (IPD-PWROK) CLKOUTFLEX0/GPIO64 C40 — NC_PCH_GPIO64_CLKOUTFLEX0
- (IPD-PWROK) CLKOUTFLEX1/GPIO65 F38 — NC_PCH_GPIO65_CLKOUTFLEX1
- (IPD-PWROK) CLKOUTFLEX2/GPIO66 F36 — NC_PCH_GPIO66_CLKOUTFLEX2
- (IPD-PWROK) CLKOUTFLEX3/GPIO67 F39 — NC_PCH_GPIO67_CLKOUTFLEX3
- ICLK_IREF AM45 — PP1V5_S0

TP19 AD39 — NC; TP18 AD38 — NC

- DIFFCLK_BIASREF AN44 — PCH_DIFFCLK_BIASREF
PLACE_NEAR=U1100.AN44:2.54mm

R1190 7.5K 1% 1/20W MF 201 — PP1V5_S0

NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.

PPVRTC_G3H — R1100 330K, R1101 1M, R1102 20K, R1103 20K

- PCH_SRTCRST_L
- PCH_INTRUDER_L
- PCH_INTVRMEN_L
- RTC_RESET_L

C1102 1UF 10V X5R 402; C1103 1UF 10V X5R 402

PP3V3_SUS; PP3V3_S0

- R1177 4.7K — PCH_SPKR
- R1176 10K — DP_TBT_SEL
- R1178 4.7K — PCH_SATALED_L
- R1134 10K — DP_AUXCH_ISOL_L
- R1133 10K — XDP_DC1_SATARDRVR_EN
- R1143 10K — SSD_CLKREQ_L
- R1142 10K — XDP_DD2_ENETSD_CLKREQ_L
- R1169 10K — AP_CLKREQ_L
- R1144 10K — CAMERA_CLKREQ_L
- R1145 10K — TBT_CLKREQ_L
- R1147 10K — PCH_CLKRQ5_L_GPIO44
- R1114 10K — PEG_CLKREQ_L
- R1115 10K — PCH_CLKRQ7_L_GPIO46
- R1146 10K — ENET_CLKREQ_L
- R1148 10K — PCH_PEGCLKRQB_L_GPIO56
- R1179 10K — ENET_MEDIA_SENSE_RDIV

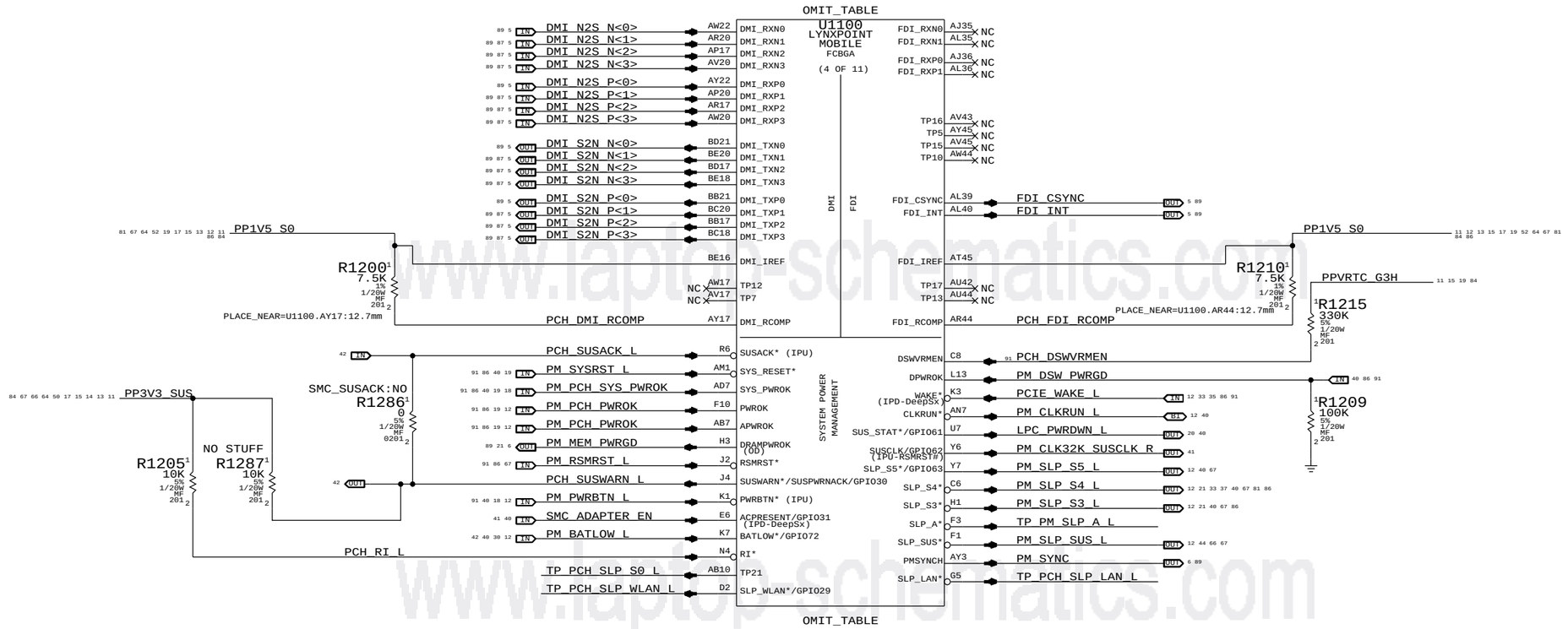
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.

SYNC_MASTER=J15_REFERENCE
SYNC_DATE=12/18/2012

PAGE TITLE: PCH RTC/HDA/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 11 OF 119
SHEET: 11 OF 97


OMIT_TABLE
U1100
LYNXPOINT MOBILE
FCBGA
(4 OF 11)
DMI_RXN0 AW22
DMI_RXN1 AR20
DMI_RXN2 AP17
DMI_RXN3 AV20
DMI_RXP0 AY22
DMI_RXP1 AP20
DMI_RXP2 AR17
DMI_RXP3 AW20
DMI_TXN0 BD21
DMI_TXN1 BE20
DMI_TXN2 BD17
DMI_TXN3 BE18
DMI_TXP0 BB21
DMI_TXP1 BC20
DMI_TXP2 BB17
DMI_TXP3 BC18
DMI_IREF BE16
TP12 AW17
TP7 AV17
DMI_RCOMP AY17
DMI
FDI
FDI_RXN0 AJ35
FDI_RXN1 AL35
FDI_RXP0 AJ36
FDI_RXP1 AL36
TP16 AV43
TP5 AY45
TP15 AV45
TP10 AW44
FDI_CSYNC AL39
FDI_INT AL40
FDI_IREF AT45
TP17 AU42
TP13 AU44
FDI_RCOMP AR44
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>
DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
FDI_CSYNC
FDI_INT
PP1V5_S0
R1200 1 7.5K 1% 1/20W MF 201 2
PLACE_NEAR=U1100.AY17:12.7mm
PCH_DMI_RCOMP
R1210 1 7.5K 1% 1/20W MF 201 2
PLACE_NEAR=U1100.AR44:12.7mm
PCH_FDI_RCOMP
PPVRTC_G3H
R1215 330K 5% 1/20W MF 201
R1209 100K 5% 1/20W MF 201
SYSTEM POWER MANAGEMENT
PCH_SUSACK_L
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_PCH_PWROK
PM_MEM_PWRGD
PM_RSMRST_L
PCH_SUSWARN_L
PM_PWRBTN_L
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_RI_L
TP_PCH_SLP_S0_L
TP_PCH_SLP_WLAN_L
SUSACK* (IPU) R6
SYS_RESET* AM1
SYS_PWROK AD7
PWROK F10
APWROK AB7
DRAMPWROK (OD) H3
RSMRST* J2
SUSWARN*/SUSPWRNACK/GPIO30 J4
PWRBTN* (IPU) K1
ACPRESENT/GPIO31 (IPD-DeepSx) E6
BATLOW*/GPIO72 K7
RI* N4
TP21 AB10
SLP_WLAN*/GPIO29 D2
DSWVRMEN C8
DPWROK L13
WAKE* (IPD-DeepSx) K3
CLKRUN* AN7
SUS_STAT*/GPIO61 U7
SUSCLK/GPIO62 (IPU-RSMRST#) Y6
SLP_S5*/GPIO63 Y7
SLP_S4* C6
SLP_S3* H1
SLP_A* F3
SLP_SUS* F1
PMSYNCH AY3
SLP_LAN* G5
PCH_DSWVRMEN
PM_DSW_PWRGD
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
PM_SLP_SUS_L
PM_SYNC
TP_PCH_SLP_LAN_L
PP3V3_SUS
SMC_SUSACK:NO
R1286 0 5% 1/20W MF 0201
NO STUFF
R1205 10K 5% 1/20W MF 201
R1287 10K 5% 1/20W MF 201
PCH_RI_L
OMIT_TABLE
U1100
LYNXPOINT MOBILE
FCBGA
(5 OF 11)
VGA_BLUE T45
VGA_GREEN U44
VGA_RED V45
VGA_DDC_CLK M43
VGA_DDC_DATA M45
VGA_HSYNC N42
VGA_VSYNC N44
DAC_IREF U40
VGA_IRTN U39
CRT
DISPLAY
EDP
EDP_BKLTCTL N36
EDP_BKLTEN K36
EDP_VDDEN G36
DDPB_CTRLCLK R40
DDPB_CTRLDATA (IPD-PLTRST#) R39
DDPC_CTRLCLK R35
DDPC_CTRLDATA (IPD-PLTRST#) R36
DDPD_CTRLCLK N40
DDPD_CTRLDATA (IPD-PLTRST#) N38
DDPB_AUXN H45
DDPC_AUXN K43
DDPD_AUXN J42
DDPB_AUXP H43
DDPC_AUXP K45
DDPD_AUXP J44
DDPB_HPD K40
DDPC_HPD K38
DDPD_HPD H39
NC_EDP_IG_BKL_PWM
EDP_IG_BKL_ON
EDP_IG_PANEL_PWR
DPA_IG_DDC_CLK
DPA_IG_DDC_DATA
DPB_IG_DDC_CLK
DPB_IG_DDC_DATA
TP_DP_IG_D_DDC_CLK
TP_DP_IG_D_DDC_DATA
DPA_IG_AUX_CH_N
DPB_IG_AUX_CH_N
NC_DP_IG_D_AUXCHN
DPA_IG_AUX_CH_P
DPB_IG_AUX_CH_P
NC_DP_IG_D_AUXCHP
DP_TBTSNK0_HPD_IG
DP_TBTSNK1_HPD_IG
DP_TBT_IG_D_HPD
VGA DAC Disabled per SB
DG v1.0 (Table 12-18).
PP3V3_S0
R1260 10K
R1261 10K
R1262 10K
R1263 10K
PCI_INTA_L
PCI_INTB_L
PCI_INTC_L
PCI_INTD_L
PIRQA* H20
PIRQB* L20
PIRQC* K17
PIRQD* M20
PCI
GPIO50 A12
GPIO52 B13
GPIO54 C12
GPIO51 C10
GPIO53 A10
GPIO55 AL6
(IPU-PWROK&PCIRST#)
ENET_LOW_PWR_PCH
AUD_IPHS_SWITCH_EN_PCH
BT_PWRRST_L
TP_PCH_STRP_BBS1
TP_PCH_STRP_ESI_L
PCH_STRP_TOPBLK_SWP_L
PIRQE*/GPIO2 G17
PIRQF*/GPIO3 F17
PIRQG*/GPIO4 L15
PIRQH*/GPIO5 M15
(IPU) PME* AD10
PLTRST* Y11
SDCONN_OC_L
AUD_IP_PERIPHERAL_DET
TBT_PWR_REQ_L
AUD_I2C_INT_L
NC_PCI_PME_L
PLT_RESET_L
PP3V3_S5
PP3V3_S0
R1239 3.0K PM_PWRBTN_L
R1240 10K PM_BATLOW_L
R1291 10K PM_CLKRUN_L
R1216 10K ENET_LOW_PWR_PCH
R1217 100K AUD_IPHS_SWITCH_EN_PCH
R1218 10K BT_PWRRST_L
R1230 10K SDCONN_OC_L
NO STUFF Redundant to pull-up on audio page
R1214 100K AUD_IP_PERIPHERAL_DET
R1231 10K TBT_PWR_REQ_L
NO STUFF Redundant to pull-up on audio page
R1233 10K AUD_I2C_INT_L
R1225 1K PCIE_WAKE_L
R1224 100K PM_SLP_S3_L
R1221 100K PM_SLP_S4_L
R1222 100K PM_SLP_S5_L
R1223 100K PM_SLP_SUS_L
R1281 100K EDP_IG_BKL_ON
R1284 100K EDP_IG_PANEL_PWR
5% 1/20W MF 201
SYNC_MASTER=J15_REFERENCE
SYNC_DATE=12/18/2012
PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 12 OF 119
SHEET 12 OF 97
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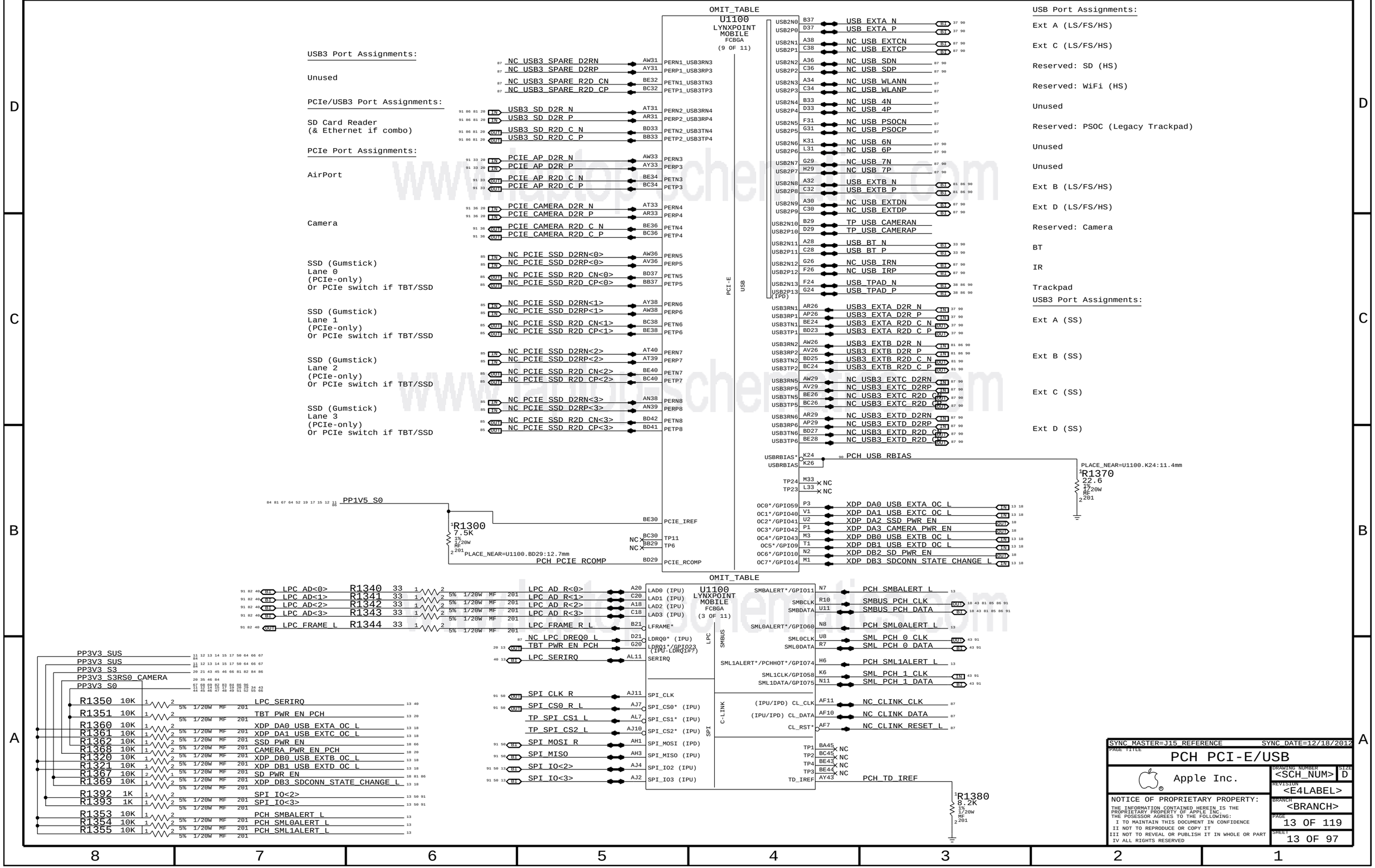
USB3 Port Assignments:
Unused
PCIe/USB3 Port Assignments:
SD Card Reader
(& Ethernet if combo)
PCIe Port Assignments:
AirPort
Camera
SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD
SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD
NC_USB3_SPARE_D2RN
NC_USB3_SPARE_D2RP
NC_USB3_SPARE_R2D_CN
NC_USB3_SPARE_R2D_CP
USB3_SD_D2R_N
USB3_SD_D2R_P
USB3_SD_R2D_C_N
USB3_SD_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_CAMERA_D2R_N
PCIE_CAMERA_D2R_P
PCIE_CAMERA_R2D_C_N
PCIE_CAMERA_R2D_C_P
NC_PCIE_SSD_D2RN<0>
NC_PCIE_SSD_D2RP<0>
NC_PCIE_SSD_R2D_CN<0>
NC_PCIE_SSD_R2D_CP<0>
NC_PCIE_SSD_D2RN<1>
NC_PCIE_SSD_D2RP<1>
NC_PCIE_SSD_R2D_CN<1>
NC_PCIE_SSD_R2D_CP<1>
NC_PCIE_SSD_D2RN<2>
NC_PCIE_SSD_D2RP<2>
NC_PCIE_SSD_R2D_CN<2>
NC_PCIE_SSD_R2D_CP<2>
NC_PCIE_SSD_D2RN<3>
NC_PCIE_SSD_D2RP<3>
NC_PCIE_SSD_R2D_CN<3>
NC_PCIE_SSD_R2D_CP<3>
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(9 OF 11)
PCI-E
USB
AW31 PERN1_USB3RN3
AY31 PERP1_USB3RP3
BE32 PETN1_USB3TN3
BC32 PETP1_USB3TP3
AT31 PERN2_USB3RN4
AR31 PERP2_USB3RP4
BD33 PETN2_USB3TN4
BB33 PETP2_USB3TP4
AW33 PERN3
AY33 PERP3
BE34 PETN3
BC34 PETP3
AT33 PERN4
AR33 PERP4
BE36 PETN4
BC36 PETP4
AW36 PERN5
AV36 PERP5
BD37 PETN5
BB37 PETP5
AY38 PERN6
AW38 PERP6
BC38 PETN6
BE38 PETP6
AT40 PERN7
AT39 PERP7
BE40 PETN7
BC40 PETP7
AN38 PERN8
AN39 PERP8
BD42 PETN8
BD41 PETP8
BE30 PCIE_IREF
BC30 TP11
BB29 TP6
BD29 PCIE_RCOMP
PP1V5_S0
R1300
7.5K
1% 1/20W MF 201
PLACE_NEAR=U1100.BD29:12.7mm
PCH PCIE RCOMP
USB Port Assignments:
Ext A (LS/FS/HS)
Ext C (LS/FS/HS)
Reserved: SD (HS)
Reserved: WiFi (HS)
Unused
Reserved: PSOC (Legacy Trackpad)
Unused
Unused
Ext B (LS/FS/HS)
Ext D (LS/FS/HS)
Reserved: Camera
BT
IR
Trackpad
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
Ext C (SS)
Ext D (SS)
USB2N0 B37 USB_EXTA_N
USB2P0 D37 USB_EXTA_P
USB2N1 A38 NC_USB_EXTCN
USB2P1 C38 NC_USB_EXTCP
USB2N2 A36 NC_USB_SDN
USB2P2 C36 NC_USB_SDP
USB2N3 A34 NC_USB_WLANN
USB2P3 C34 NC_USB_WLANP
USB2N4 B33 NC_USB_4N
USB2P4 D33 NC_USB_4P
USB2N5 F31 NC_USB_PSOCN
USB2P5 G31 NC_USB_PSOCP
USB2N6 K31 NC_USB_6N
USB2P6 L31 NC_USB_6P
USB2N7 G29 NC_USB_7N
USB2P7 H29 NC_USB_7P
USB2N8 A32 USB_EXTB_N
USB2P8 C32 USB_EXTB_P
USB2N9 A30 NC_USB_EXTDN
USB2P9 C30 NC_USB_EXTDP
USB2N10 B29 TP_USB_CAMERAN
USB2P10 D29 TP_USB_CAMERAP
USB2N11 A28 USB_BT_N
USB2P11 C28 USB_BT_P
USB2N12 G26 NC_USB_IRN
USB2P12 F26 NC_USB_IRP
USB2N13 F24 USB_TPAD_N
USB2P13 G24 USB_TPAD_P
(IPD)
USB3RN1 AR26 USB3_EXTA_D2R_N
USB3RP1 AP26 USB3_EXTA_D2R_P
USB3TN1 BE24 USB3_EXTA_R2D_C_N
USB3TP1 BD23 USB3_EXTA_R2D_C_P
USB3RN2 AW26 USB3_EXTB_D2R_N
USB3RP2 AV26 USB3_EXTB_D2R_P
USB3TN2 BD25 USB3_EXTB_R2D_C_N
USB3TP2 BC24 USB3_EXTB_R2D_C_P
USB3RN5 AW29 NC_USB3_EXTC_D2RN
USB3RP5 AV29 NC_USB3_EXTC_D2RP
USB3TN5 BE26 NC_USB3_EXTC_R2D_CN
USB3TP5 BC26 NC_USB3_EXTC_R2D_CP
USB3RN6 AR29 NC_USB3_EXTD_D2RN
USB3RP6 AP29 NC_USB3_EXTD_D2RP
USB3TN6 BD27 NC_USB3_EXTD_R2D_CN
USB3TP6 BE28 NC_USB3_EXTD_R2D_CP
USBRBIAS* K24
USBRBIAS K26
PCH_USB_RBIAS
PLACE_NEAR=U1100.K24:11.4mm
R1370
22.6
1% 1/20W MF 201
TP24 M33 NC
TP23 L33 NC
OC0*/GPIO59 P3 XDP_DA0_USB_EXTA_OC_L
OC1*/GPIO40 V1 XDP_DA1_USB_EXTC_OC_L
OC2*/GPIO41 U2 XDP_DA2_SSD_PWR_EN
OC3*/GPIO42 P1 XDP_DA3_CAMERA_PWR_EN
OC4*/GPIO43 M3 XDP_DB0_USB_EXTB_OC_L
OC5*/GPIO9 T1 XDP_DB1_USB_EXTD_OC_L
OC6*/GPIO16 N2 XDP_DB2_SD_PWR_EN
OC7*/GPIO14 M1 XDP_DB3_SDCONN_STATE_CHANGE_L
OMIT_TABLE
U1100
LYNXPOINT
MOBILE
FCBGA
(3 OF 11)
LPC
SMBUS
C-LINK
SPI
LAD0 (IPU) A20 LPC_AD_R<0>
LAD1 (IPU) C20 LPC_AD_R<1>
LAD2 (IPU) A18 LPC_AD_R<2>
LAD3 (IPU) C18 LPC_AD_R<3>
LFRAME* B21 LPC_FRAME_R_L
LDRQ0* (IPU) D21 NC_LPC_DREQ0_L
LDRQ1*/GPIO23 (IPU-LDRQ1#7) G20 TBT_PWR_EN_PCH
SERIRQ AL11 LPC_SERIRQ
SPI_CLK AJ11 SPI_CLK_R
SPI_CS0* (IPU) AJ7 SPI_CS0_R_L
SPI_CS1* (IPU) AL7 TP_SPI_CS1_L
SPI_CS2* (IPU) AJ10 TP_SPI_CS2_L
SPI_MOSI (IPD) AH1 SPI_MOSI_R
SPI_MISO (IPU) AH3 SPI_MISO
SPI_IO2 (IPU) AJ4 SPI_IO<2>
SPI_IO3 (IPU) AJ2 SPI_IO<3>
SMBALERT*/GPIO11 N7 PCH_SMBALERT_L
SMBCLK R10 SMBUS_PCH_CLK
SMBDATA U11 SMBUS_PCH_DATA
SML0ALERT*/GPIO60 N8 PCH_SML0ALERT_L
SML0CLK U8 SML_PCH_0_CLK
SML0DATA R7 SML_PCH_0_DATA
SML1ALERT*/PCHHOT*/GPIO74 H6 PCH_SML1ALERT_L
SML1CLK/GPIO58 K6 SML_PCH_1_CLK
SML1DATA/GPIO75 N11 SML_PCH_1_DATA
(IPU/IPD) CL_CLK AF11 NC_CLINK_CLK
(IPU/IPD) CL_DATA AF10 NC_CLINK_DATA
CL_RST* AF7 NC_CLINK_RESET_L
TP1 BA45 NC
TP2 BC45 NC
TP4 BE43 NC
TP3 BE44 NC
TD_IREF AY43 PCH_TD_IREF
R1380
9.2K
1% 1/20W MF 201
LPC_AD<0> R1340 33
LPC_AD<1> R1341 33
LPC_AD<2> R1342 33
LPC_AD<3> R1343 33
LPC_FRAME_L R1344 33
5% 1/20W MF 201
PP3V3_SUS
PP3V3_SUS
PP3V3_S3
PP3V3_S3RS0_CAMERA
PP3V3_S0
R1350 10K LPC_SERIRQ
R1351 10K TBT_PWR_EN_PCH
R1360 10K XDP_DA0_USB_EXTA_OC_L
R1361 10K XDP_DA1_USB_EXTC_OC_L
R1362 10K SSD_PWR_EN
R1368 10K CAMERA_PWR_EN_PCH
R1320 10K XDP_DB0_USB_EXTB_OC_L
R1321 10K XDP_DB1_USB_EXTD_OC_L
R1367 10K SD_PWR_EN
R1369 10K XDP_DB3_SDCONN_STATE_CHANGE_L
R1392 1K SPI_IO<2>
R1393 1K SPI_IO<3>
R1353 10K PCH_SMBALERT_L
R1354 10K PCH_SML0ALERT_L
R1355 10K PCH_SML1ALERT_L
SYNC_MASTER=J15_REFERENCE
SYNC_DATE=12/18/2012
PAGE TITLE
PCH PCI-E/USB
Apple Inc.
DRAWING NUMBER
<SCH_NUM>
SIZE
D
REVISION
<E4LABEL>
BRANCH
<BRANCH>
PAGE
13 OF 119
SHEET
13 OF 97
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Pull-up/down on chipset support page (depends on TBT controller)
Falcon Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
(6 OF 11)

TBT_CIO_PLUG_EVENT_L	AT8	BMBUSY*/GPIO0	
FW_PME_L	F13	TACH1/GPIO1	
DPMUX_UC_IRQ	A14	TACH2/GPIO6	
SMC_RUNTIME_SCI_L	G15	TACH3/GPIO7	
XDP_FC0_HDD_PWR_EN	Y1	GPIO8 (IPU-RSMRST#)	
WOL_EN	K13	LAN_PHY_PWR_CTRL/GPIO12	
MEM_VDD_SEL_1V5_L	AB11	GPIO15	
XDP_DD0_SSD_PCIE_SEL_L	AN2	SATA4GP/GPIO16 (IPU-Boot/SATA4GP?)	
LPCPLUS_GPIO	C14	TACH0/GPIO17	
JTAG_TBT_TMS_PCH	BB4	SCLOCK/GPIO22	
TBT_GO2SX_BIDIR	Y10	GPIO24	
SMC_WAKE_SCI_L	R11	GPIO27 (IPU-DeepSx)	
ISOLATE_CPU_MEM_L	AD11	GPIO28	
TBT_POC_RESET_L	AN6	GPIO34	
XDP_FC1_GPU_GOOD	AP1	GPIO35/NMI*	
XDP_DC2_ODD_PWR_EN_L	AT3	SATA2GP/GPIO36 (IPD-PLTRST#)	
XDP_DC3_JTAG_ISP_TCK	AK1	SATA3GP/GPIO37 (IPD-PLTRST#)	
JTAG_ISP_TDO	AT7	SLOAD/GPIO38	
JTAG_ISP_TDI	AM3	SDATAOUT0/GPIO39	
FW_PWR_EN_PCH	AN4	SDATAOUT1/GPIO48	
XDP_DD1_MLB_RAMCFG1	AK3	SATA5GP/GPIO49 (IPU-Boot/SATA5GP?)	
SPIROM_USE_MLB	U12	GPIO57	
MLB_RAMCFG3	C16	TACH4/GPIO68	
MLB_RAMCFG2	D13	TACH5/GPIO69	
SD_SEL_PCIE_L_USB_H	G13	TACH6/GPIO70 (IPU-Boot?)	
MLB_RAMCFG0	H15	TACH7/GPIO71 (IPU-Boot?)	
	BE41		
	BE5		
VSS	C45		
	A5		

CPU/MISC

	AN10	TP14	PCH_A20GATE
	AY1	(IPD) PECI	PCH_PECI
	AT6	RCIN*	PCH_RCIN_L
	AV3	PROCPWRGD	PCH_PROCPWRGD
	AV1	THRMTRIP*	PM_THRMTRIP_L_R
	AU4	PLTRST_PROC*	CPU_RESET_L
VSS	N10		
	A2		
	A41		
	A43		
	A44		
	B1		
	B2		
	B44		
	B45		
	BA1		
	BC1		
	BD1		
VSS	BD2		
	BD44		
	BD45		
	BE2		
	BE3		
	D1		
	E1		
	E45		
	A4		

PP1V05_S0
BDW_SPRT
R1457 1K 5% 1/16W MF-LF 402

R1470 43 5% 1/20W MF 201 — NO STUFF — CPU_PECI
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L
CRW_SPRT

PP3V3_S0
R1475 10K 5% 1/20W MF 201 — RAMCFG0:H
R1474 10K 5% 1/20W MF 201 — RAMCFG1:H
R1473 10K 5% 1/20W MF 201 — RAMCFG2:H
R1472 10K 5% 1/20W MF 201 — RAMCFG3:H

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MF,1A MAX,0.0 OHM,5%,0201,BLACK	R1456		BDW_SPRT

PP3V3_S5
PP3V3_SUS
PP3V3_S0

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K	FW_PME_L	
R1411	20K	DPMUX_UC_IRQ	
R1496	10K	SMC_RUNTIME_SCI_L	
R1494	10K	WOL_EN	
R1489	10K	MEM_VDD_SEL_1V5_L	
R1495	100K	XDP_DD0_SSD_PCIE_SEL_L	
R1490	100K	LPCPLUS_GPIO	
R1412	10K	JTAG_TBT_TMS_PCH	
R1492	10K	TBT_GO2SX_BIDIR	
R1491	10K	SMC_WAKE_SCI_L	
R1498	10K	XDP_DC2_ODD_PWR_EN_L	
R1413	10K	JTAG_ISP_TCK	
R1486	10K	JTAG_ISP_TDO	
R1499	10K	JTAG_ISP_TDI	
R1484	10K	FW_PWR_EN_PCH	
R1493	100K	SPIROM_USE_MLB	

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K	PCH_A20GATE	
R1455	10K	PCH_RCIN_L	

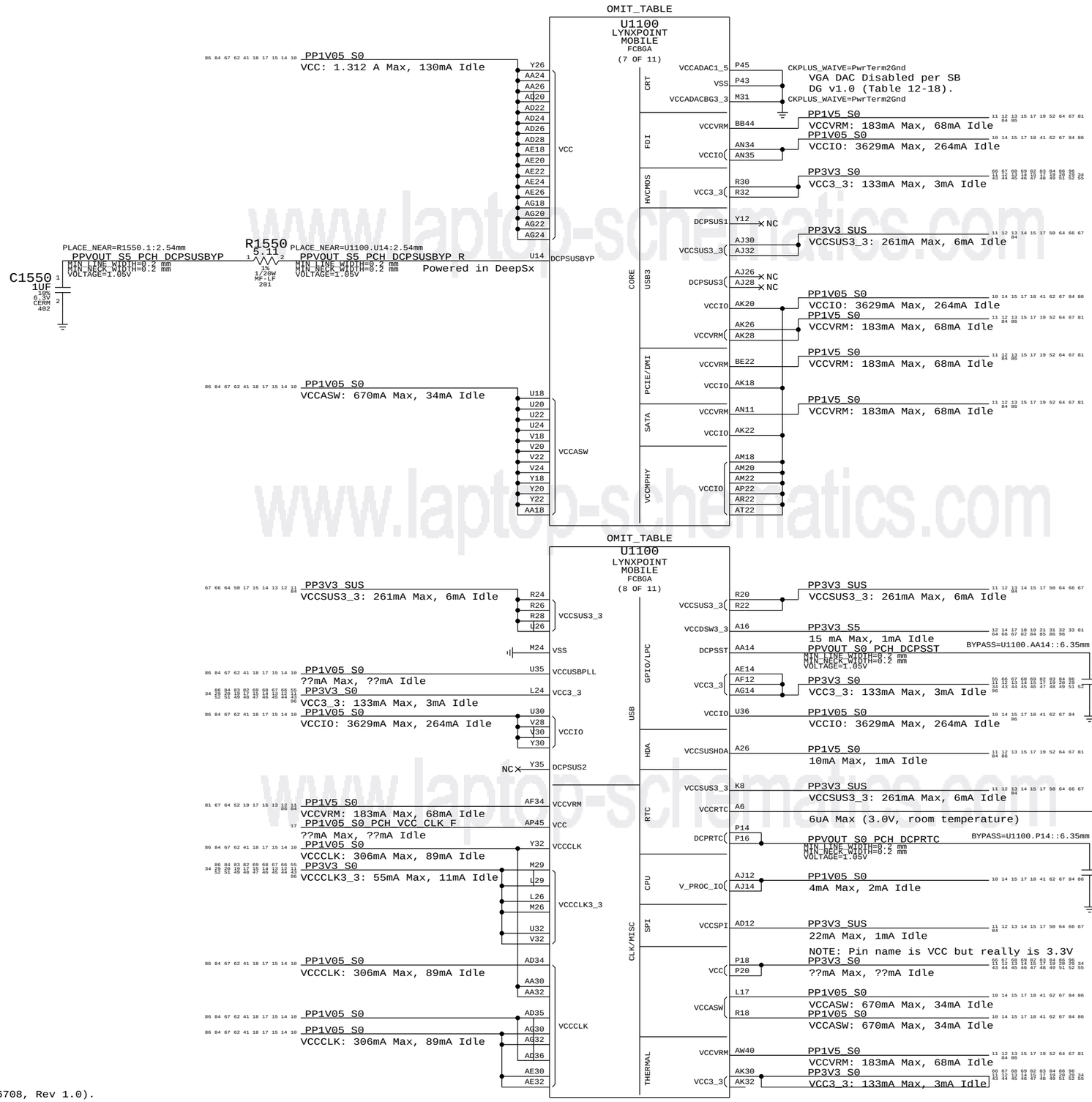
All: 5% 1/20W MF 201

SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/31/2014

PAGE TITLE: PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 14 OF 119
SHEET: 14 OF 97



Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE

PCH Power

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 15 OF 119

SHEET 15 OF 97

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(10 OF 11)
VSS

AL34			K39
AL38			L2
AL8			L44
AM14			M17
AM24			M22
AM26			N12
AM28			N35
AM30			N39
AM32			N6
AM16			P22
AN36			P24
AN40			P26
AN42			P28
AN8			P30
AP13			P32
AP24			R12
AP31			R14
AP43			R16
AR2			R2
AK16			R34
AT10			R38
AT15		VSS	R44
AT17	VSS		R8
AT20			T43
AT26			U10
AT29			U16
AT36			U28
AT38			U34
D42			U38
AV13			U42
AV22			U6
AV24			V14
AV31			V16
AV33			V25
BB25			V43
AV40			W2
AV6			W44
AW2			Y14
F43			Y15
AY10			Y24
AY15			Y28
AY20			Y34
AY26			Y36
AY29			Y40
AY7			Y8
B11			
B15			

OMIT_TABLE

U1100
LYNXPOINT
MOBILE
FCBGA
(11 OF 11)
VSS

AA16			B19
AA20			B23
AA22			B27
AA28			B31
AA4			B35
AB12			B39
AB34			B7
AB38			BA40
AB8			BD11
AC2			BD15
AC44			BD19
AD14			AY36
AD16			AT43
AD18			BD31
AD30			BD35
AD32			BD39
AD40			BD7
AD6			D25
AD8			AV7
AE16			F15
AE28			F20
AF38			F29
AF8	VSS	VSS	F33
AG16			BC16
AG2			D4
AG26			G2
AG28			G38
AG44			G44
AJ16			G8
AJ18			H10
AJ20			H13
AJ22			H17
AJ24			H21
AJ34			H24
AJ38			H26
AJ6			H31
AJ8			H36
AK14			H40
AK24			H7
AK43			K10
AK45			K15
AL12			K20
AL2			K25
BC22			K33
BB42			BC28

SYNC_MASTER=J15_REFERENCE SYNC_DATE=12/18/2012

PAGE TITLE
PCH Grounds

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 16 OF 119
SHEET 16 OF 97

PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
PP3V3_S5

C1700 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.A16::6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
PP3V3_SUS

C1702 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AD12::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
PP3V3_SUS

C1704 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.R20::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND USB PWR)
PP3V3_SUS

C1706 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.R26::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
PP3V3_SUS

C1708 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.K8::6.35mm

PCH VCCCLK3_3 BYPASS
(PCH 3.3V CLK PWR)
PP3V3_S0

C1720 1.0UF 10% 6.3V X6S 0402
C1721 1.0UF 10% 6.3V X6S 0402
C1722 1.0UF 10% 6.3V X6S 0402
C1723 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.L26::6.35mm
BYPASS=U1100.L29::6.35mm
BYPASS=U1100.M29::6.35mm
BYPASS=U1100.U32::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V HVCMOS PWR)
PP3V3_S0

C1726 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.R30::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
PP3V3_S0

C1728 0.01UF 10% 16V X7R-CERM 0402
BYPASS=U1100.AE14::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V USB2 PWR)
PP3V3_S0

C1730 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.L24::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
PP3V3_S0

C1732 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.AK30::6.35mm

PCH VCC BYPASS
(PCH 3.3V FUSE PWR)
PP3V3_S0

C1734 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.P18::6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
PP1V05_S0
670mA Max, 34mA Idle

C1750 22UF 20% 6.3V X5R-CERM-1 603
C1751 1.0UF 10% 6.3V X6S 0402
C1752 1.0UF 10% 6.3V X6S 0402
CRITICAL
C1753 12PF 5% NP0-C0G 0201 25V
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
PLACE_NEAR=U1100.V20:2.54mm
Not documented in EDS!

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
PP1V05_S0

C1755 10UF 20% 16V X6S-CERM 0603
C1756 1.0UF 10% 6.3V X6S 0402
C1757 1.0UF 10% 6.3V X6S 0402
C1758 1.0UF 10% 6.3V X6S 0402
CRITICAL
C1759 12PF 5% NP0-C0G 0201 25V
BYPASS=U1100.AG18::12.7mm
BYPASS=U1100.AG22::6.35mm
BYPASS=U1100.AD20::6.35mm
BYPASS=U1100.AE18::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V PCIe/DMI/SATA/USB3 PWR)
PP1V05_S0

C1760 10UF 20% 16V X6S-CERM 0603
C1761 1.0UF 10% 6.3V X6S 0402
C1762 1.0UF 10% 6.3V X6S 0402
C1763 1.0UF 10% 6.3V X6S 0402
C1764 1.0UF 10% 6.3V X6S 0402
CRITICAL
C1765 12PF 5% NP0-C0G 0201 25V
BYPASS=U1100.AK18::12.7mm
BYPASS=U1100.AK22::6.35mm
BYPASS=U1100.AK20::6.35mm
BYPASS=U1100.AM18::6.35mm

PCH VCCUSBPLL BYPASS
(PCH 1.05V USB2 PLL PWR)
PP1V05_S0

C1770 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.U35::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V FDI PWR)
PP1V05_S0

C1772 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AN34::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
PP1V05_S0

C1774 0.1UF 10% 25V X7R-CERM 0402
CRITICAL
C1775 12PF 5% NP0-C0G 0201 25V
BYPASS=U1100.U30::6.35mm

PCH V_PROC_IO BYPASS
(PCH 1.05V CPU I/F PWR)
PP1V05_S0

C1785 1.0UF 10% 6.3V X6S 0402
C1786 0.1UF 10% 25V X7R-CERM 0402
C1787 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.AJ12::12.7mm
BYPASS=U1100.AJ12::6.35mm
BYPASS=U1100.AJ12::6.35mm

PP1V05_S0
22mA Max, 22mA Idle
R1790 1 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_CLK_R
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

CRITICAL
OMIT_TABLE
L1790 4.7UH-170MA-0.321OHM 0603
PCH CLK VCC BYPASS
(PCH 1.05V CLK PLL PWR)
PP1V05_S0_PCH_VCC_CLK_F
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.075 MM
VOLTAGE=1.05V
NO STUFF
C1790 10UF 20% 16V X6S-CERM 0603
C1791 1UF 10% 10V X6S-CERM 0402
BYPASS=U1100.AP45::12.7mm
BYPASS=U1100.AP45::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC100 PWR)
PP1V05_S0

C1776 1.0UF 10% 6.3V X6S 0402
C1777 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AE30::6.35mm
BYPASS=U1100.AG30::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK PWR)
PP1V05_S0

C1778 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AD35::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V DIFFCLK135 PWR)
PP1V05_S0

C1780 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AD34::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V SSC PWR)
PP1V05_S0

C1782 1.0UF 10% 6.3V X6S 0402
BYPASS=U1100.AA30::6.35mm

PCH VCCSUSHDA BYPASS
(PCH 3.3V/1.5V HDA PWR)
PP1V5_S0

C1710 0.1UF 10% 25V X7R-CERM 0402
BYPASS=U1100.A26::6.35mm

PCH VCCVRM BYPASS
(PCH 1.5V VCCVRM PWR)
PP1V5_S0
183mA Max, 68mA Idle
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0
PP1V5_S0

C1740 10UF 10% 16V X6S-CERM 0603
BYPASS=U1100.AF34::12.7mm

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE
PCH DECOUPLING

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 17 OF 119
SHEET 17 OF 97

Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout. Use with 921-0133 Adapter Flex to support chipset debug.

PP1V05_S0 → R1830 150 5% 1/16W MF-LF 402

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
SMBUS_PCH_DATA	SDA	TDO	XDP_PCH_TDO
SMBUS_PCH_CLK	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

518S0847

XDP_CPU_PRESENT_L

CPU_PWRGD → R1800 1K → XDP (PLACE_NEAR=U0500.F50:2.54mm)
PM_PWRBTN_L → R1802 0 → XDP (PLACE_NEAR=U5000.J3:2.54mm)
PM_PCH_SYS_PWROK → R1804 0 → XDP
XDP_CPU_TCK

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

PP1V05_S0 → R1820 51 5% 1/20W MF 201 → XDP_CPU_TDO
R1823 51 → XDP_CPU_TCK
R1824 51 → XDP_CPUPCH_TRST_L
PLACE_NEAR=U0500.M49:28mm / M54:28mm / M53:28mm

TDI and TMS are terminated in CPU.

R1805 1K → XDP_PLT_RESET_L (PLACE_NEAR=U0500.A67:2.54mm)

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS

CRITICAL Q1840 DMN5L06VK-7 SOT563 VER 5 → XDP_CPU_TDO (PLACE_NEAR=J1800.51:28mm)
CRITICAL Q1840 DMN5L06VK-7 SOT563 VER 5 → XDP_CPUPCH_TRST_L (PLACE_NEAR=J1800.53:28mm, MAKE_BASE=TRUE)
CRITICAL Q1842 DMN5L06VK-7 SOT563 VER 5 → XDP_CPU_TDI (PLACE_NEAR=J1800.55:28mm)
CRITICAL Q1842 DMN5L06VK-7 SOT563 VER 5 → XDP_CPU_TMS (PLACE_NEAR=J1800.57:28mm)

PCH/XDP Signals

	OMIT (All 10 R's)	Non-XDP Signals
XDP_DA0_USB_EXTA_OC_L	R1890 SHORT	USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895 SHORT	SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893 SHORT	CAMERA_PWR_EN_PCH
XDP_DB0_USB_EXTB_OC_L	R1894 SHORT	USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896 SHORT	SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897 SHORT	SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872 SHORT	DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN	MAKE_BASE=TRUE	XDP_DC1_SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L	MAKE_BASE=TRUE	XDP_DC2_ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875 SHORT	JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876 SHORT	SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1	MAKE_BASE=TRUE	XDP_DD1_MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L	MAKE_BASE=TRUE	XDP_DD2_ENETSD_CLKREQ
XDP_DD3_AP_CLKREQ_L	R1879 SHORT	AP_CLKREQ_L

(all: NONE NONE NONE 201)

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813

CPU JTAG Isolation

PP5V_S0
PP3V3_S5
C1845 0.1UF 10% 16V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC, NC, NC)
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

PP1V05_SUS

R1860 51 → XDP_PCH_TDO
R1861 51 → XDP_PCH_TDI
R1862 51 → XDP_PCH_TMS
R1866 51 → XDP_PCH_TCK
(PLACE_NEAR=U1100.AD3:28mm / AE2:28mm / AD1:28mm / AB3:28mm)

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: CPU & PCH XDP

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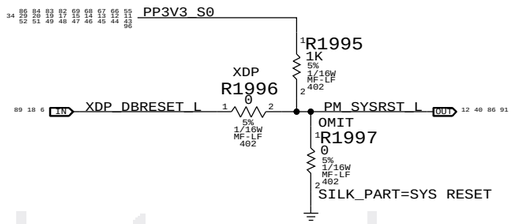
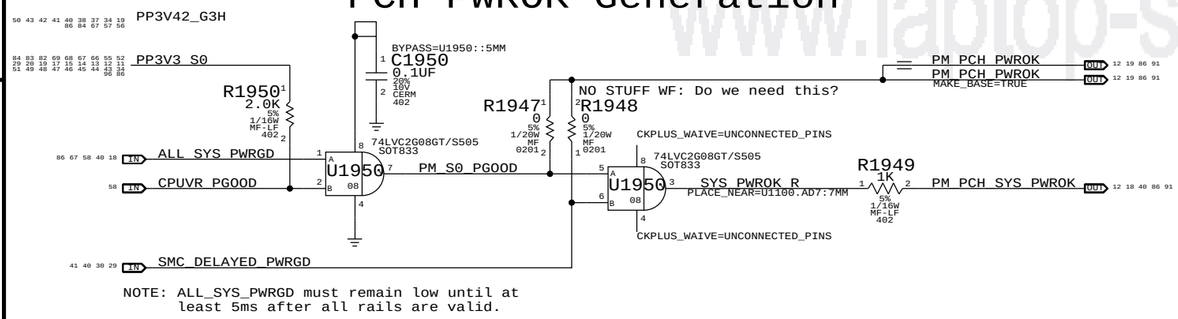
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 18 OF 119
SHEET: 18 OF 97

PCH Reset Button

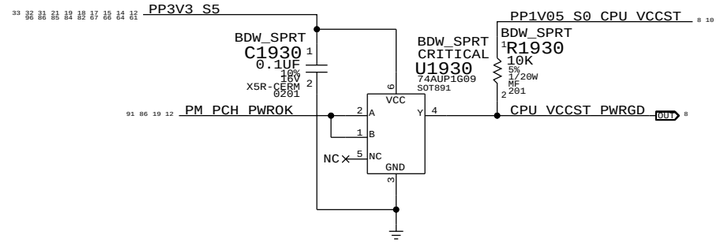


PCH PWROK Generation

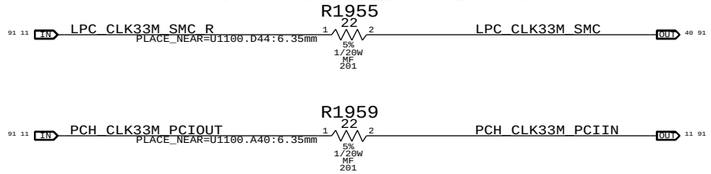


NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

VCCST (1.05V S0) PWRGD



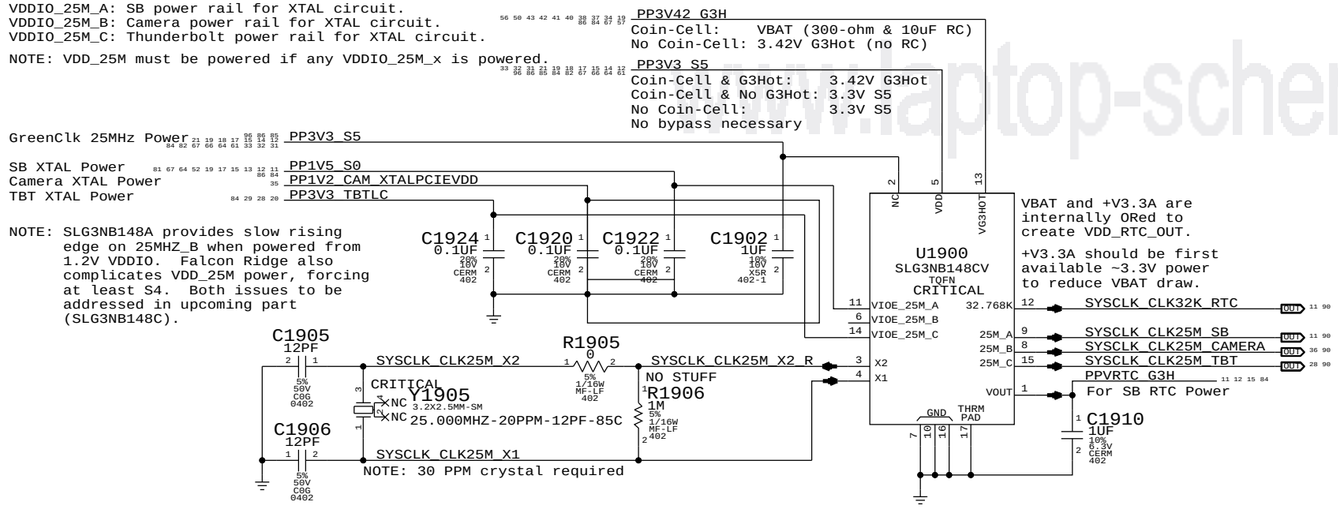
PCH 33MHz Clocks



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

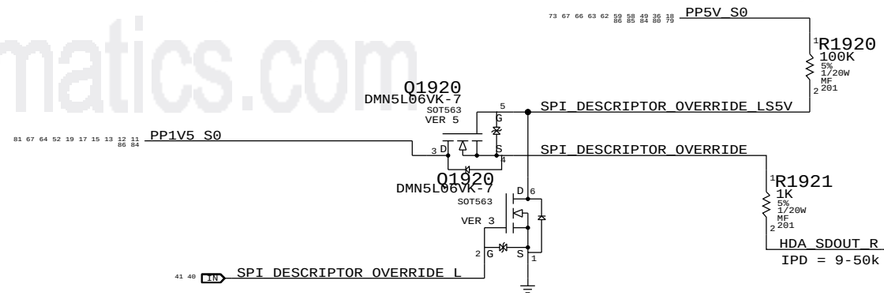


NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Falcon Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).

NOTE: 30 PPM crystal required

PCH ME Disable Strap

PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



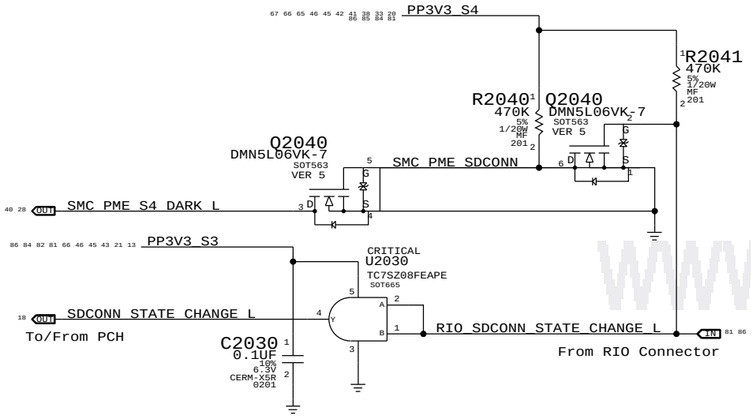
SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/31/2014

PAGE TITLE: Chipset Support

Apple Inc.

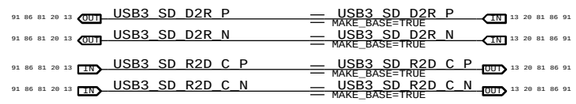
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 19 OF 119
SHEET: 19 OF 97

RIO SD Card Reader Support



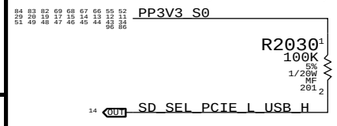
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



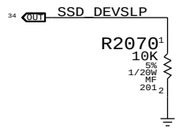
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe

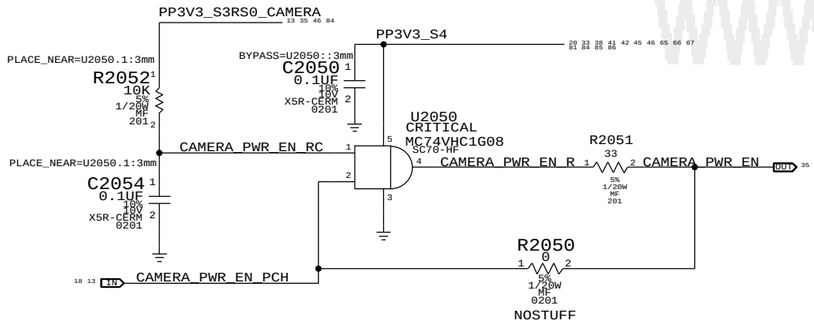


GS3 Connector Support

DEVSLP not supported on LPT-H

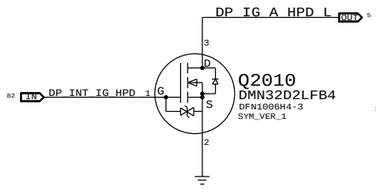


Camera power-up sequencing Support



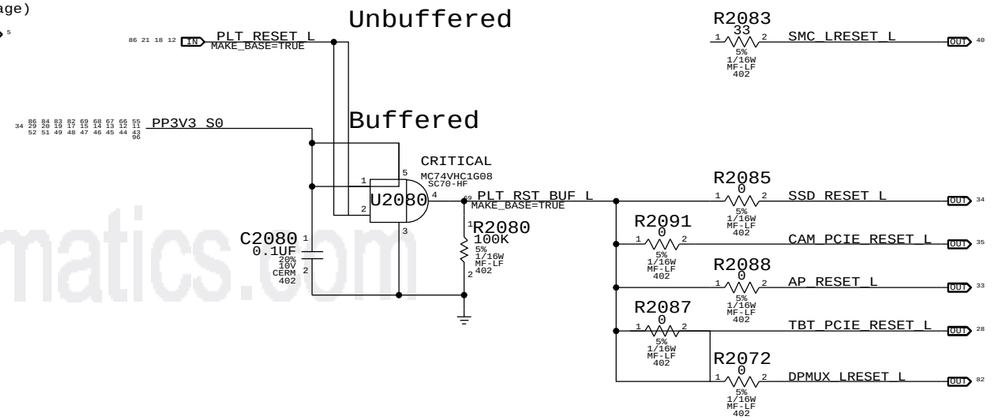
LCD HPD Inverter

(Pull-Up on CPU Page)



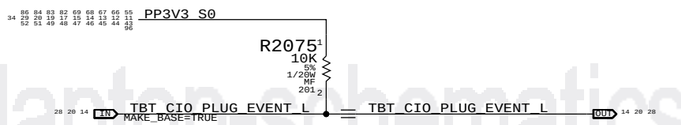
HDMI HPD pull-down

Platform Reset Connections



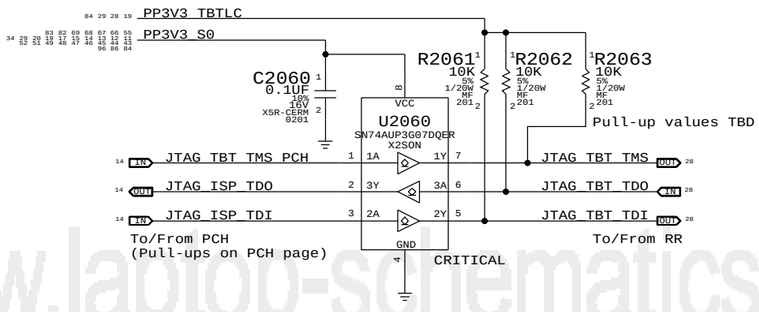
Falcon Ridge Support

RR output is open-drain, no isolation necessary

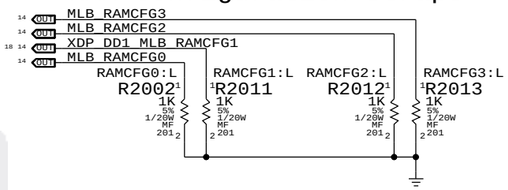


Falcon Ridge JTAG Isolation

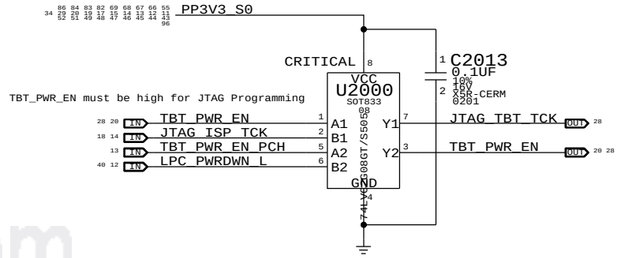
TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V



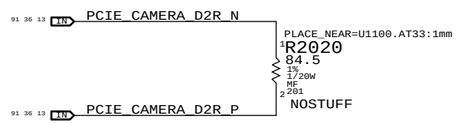
RAM Configuration Straps



GPIO Glitch Prevention

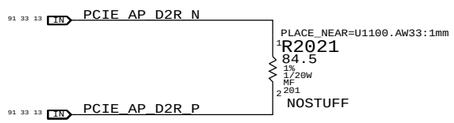


Camera PCIE D2R test points



PCH 33MHz Clock for DPMUX

AP PCIE D2R test points



SYNC_MASTER=J15_REFERENCE SYNC_DATE=01/14/2013

PAGE TITLE

Project Chipset Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

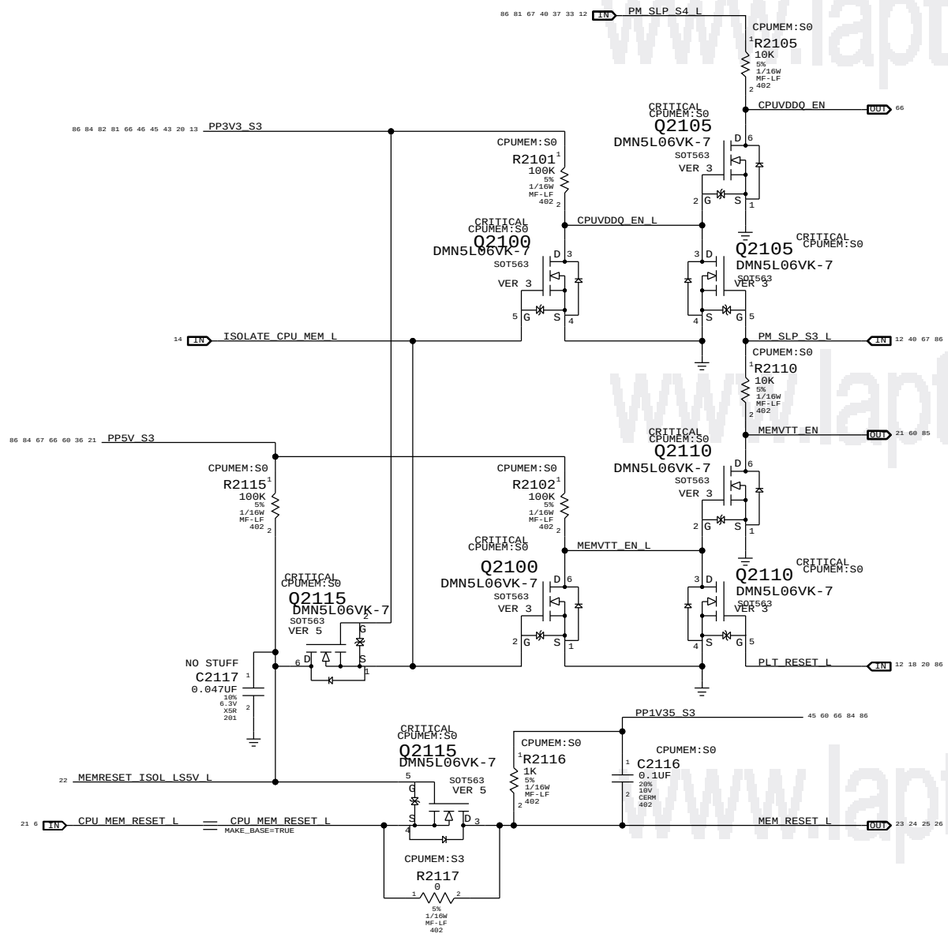
PAGE 20 OF 119

SHEET 20 OF 97

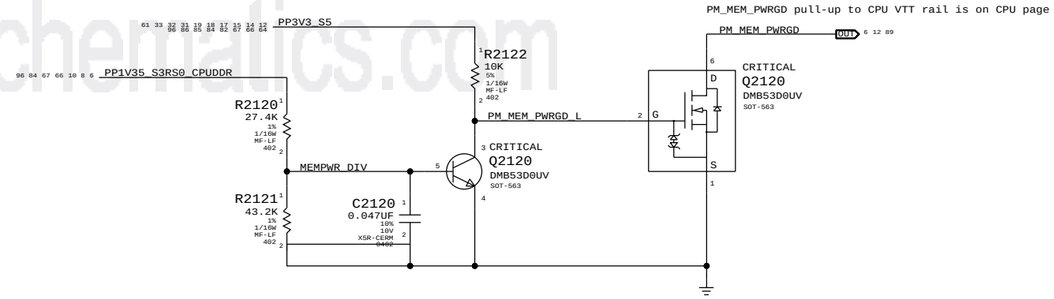
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

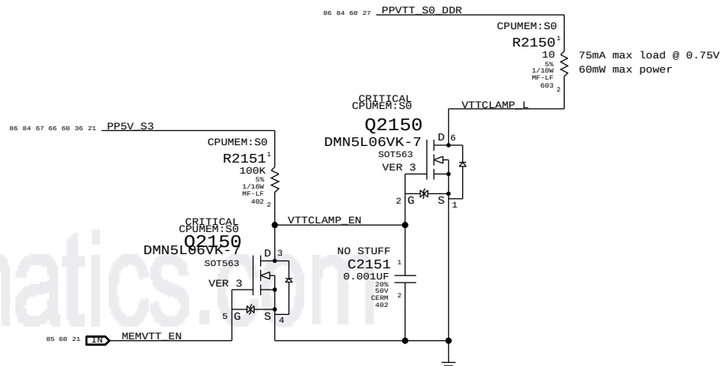


MEM S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
S3	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC_MASTER=CLEAN_MAXWELL SYNC_DATE=07/02/2014

PAGE TITLE: CPU Memory S3 Support

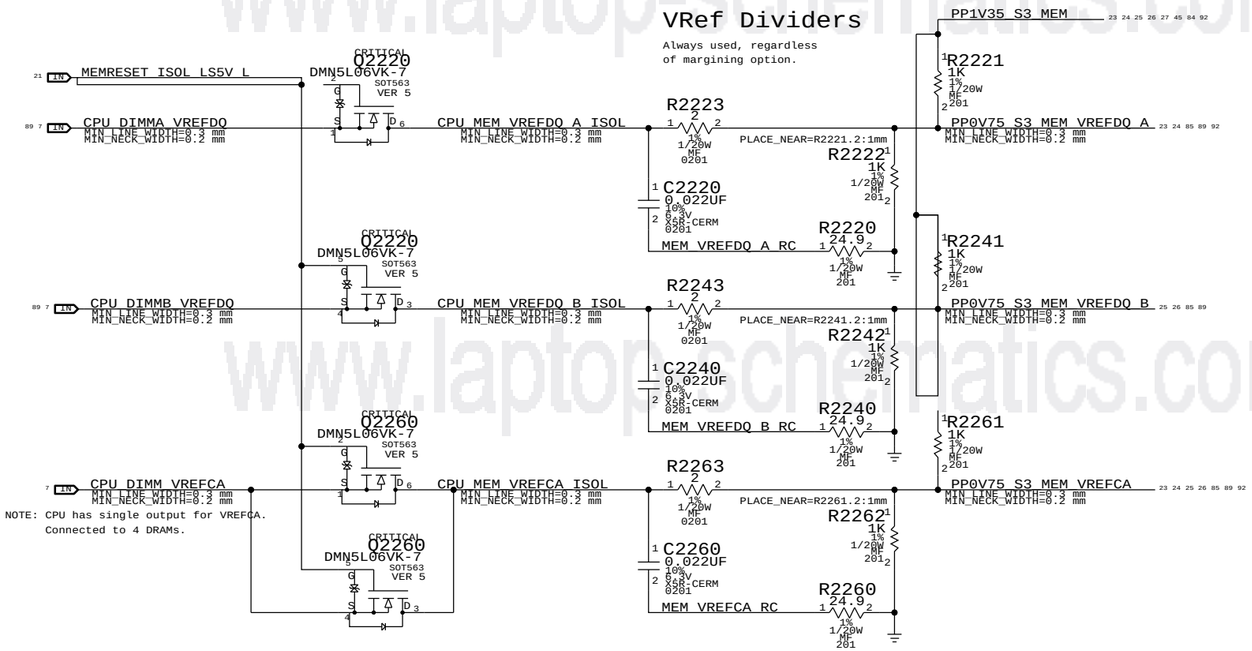
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 21 OF 119
SHEET: 21 OF 97

CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

NOTE: CPU has single output for VREFCA.
Connected to 4 DRAMs.



SYNC_MASTER=CLEAN_X425 SYNC_DATE=08/11/2014

PAGE TITLE: DDR3 VREF MARGINING

Apple Inc.

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REVISION: <E4LABEL>

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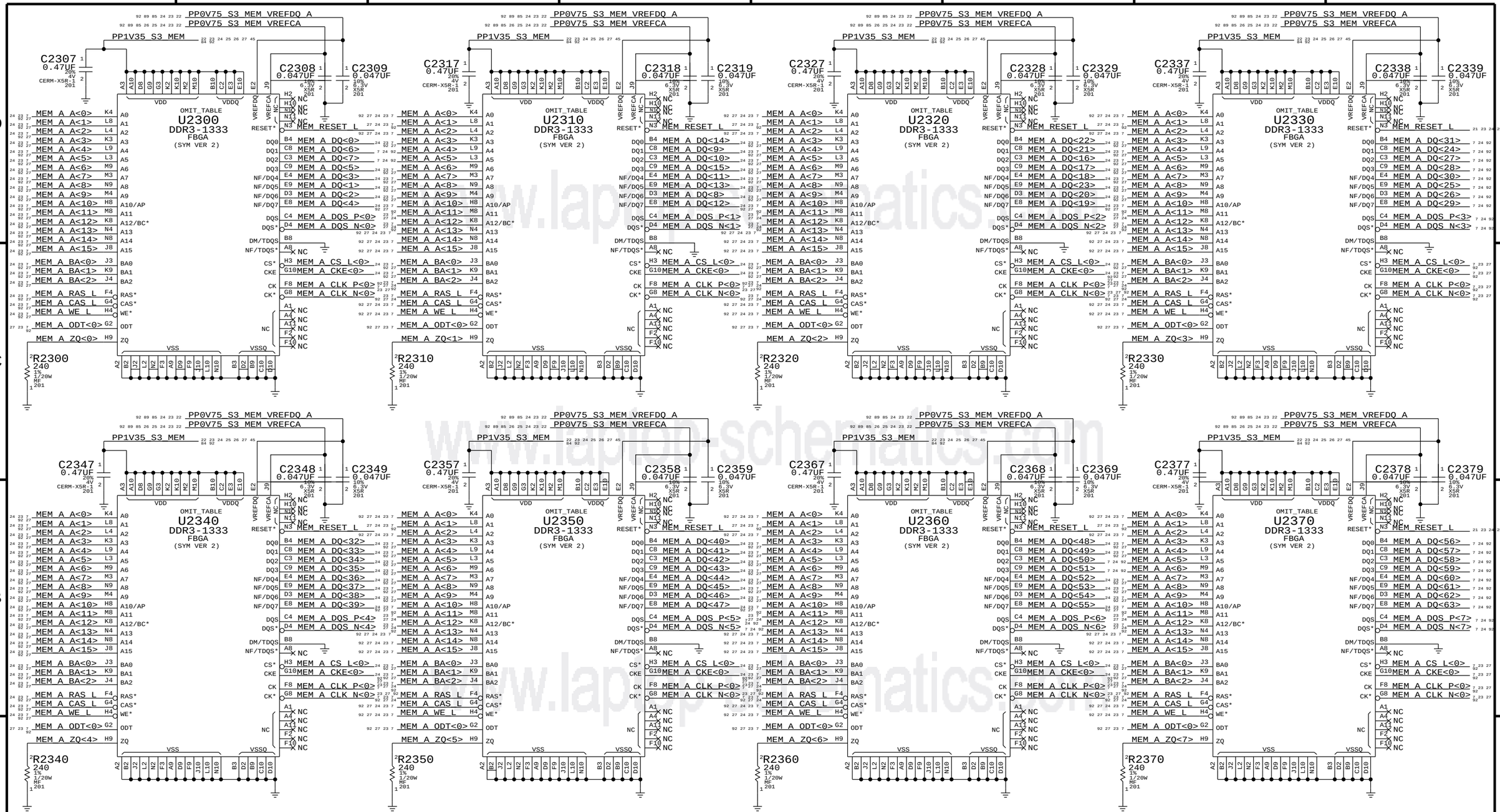
PAGE: 22 OF 119

SHEET: 22 OF 97



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 23 OF 119
SHEET 23 OF 97

PP0V75_S3_MEM_VREFDQ_A
PP0V75_S3_MEM_VREFCA
PP1V35_S3_MEM

C2407 0.47UF 20% 4V CERM-X5R-1 201
C2408 0.047UF 10% 6.3V X5R 201
C2409 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2400
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<8> H9
MEM_RESET_L
MEM_DQ<6>
MEM_DQ<0>
MEM_DQ<5>
MEM_DQ<7>
MEM_DQ<4>
MEM_DQ<2>
MEM_DQ<1>
MEM_DQ<3>
MEM_DQS_P<0>
MEM_DQS_N<0>
MEM_CS_L<1>
MEM_CKE<1>
MEM_CLK_P<1>
MEM_CLK_N<1>

R2400 240 1% 1/20W MF 201

C2417 0.47UF 20% 4V CERM-X5R-1 201
C2418 0.047UF 10% 6.3V X5R 201
C2419 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2410
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<9> H9
MEM_RESET_L
MEM_DQ<9>
MEM_DQ<14>
MEM_DQ<15>
MEM_DQ<10>
MEM_DQ<12>
MEM_DQ<8>
MEM_DQ<13>
MEM_DQ<11>
MEM_DQS_P<1>
MEM_DQS_N<1>
MEM_CS_L<1>
MEM_CKE<1>
MEM_CLK_P<1>
MEM_CLK_N<1>

R2410 240 1% 1/20W MF 201

C2427 0.47UF 20% 4V CERM-X5R-1 201
C2428 0.047UF 10% 6.3V X5R 201
C2429 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2420
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<10> H9
MEM_RESET_L
MEM_DQ<21>
MEM_DQ<22>
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MEM_DQ<19>
MEM_DQ<20>
MEM_DQ<23>
MEM_DQ<18>
MEM_DQS_P<2>
MEM_DQS_N<2>
MEM_CS_L<1>
MEM_CKE<1>
MEM_CLK_P<1>
MEM_CLK_N<1>

R2420 240 1% 1/20W MF 201

C2437 0.47UF 20% 4V CERM-X5R-1 201
C2438 0.047UF 10% 6.3V X5R 201
C2439 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2430
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<11> H9
MEM_RESET_L
MEM_DQ<24>
MEM_DQ<31>
MEM_DQ<28>
MEM_DQ<27>
MEM_DQ<29>
MEM_DQ<26>
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MEM_DQ<30>
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MEM_DQS_N<3>
MEM_CS_L<1>
MEM_CKE<1>
MEM_CLK_P<1>
MEM_CLK_N<1>

R2430 240 1% 1/20W MF 201

C2447 0.47UF 20% 4V CERM-X5R-1 201
C2448 0.047UF 10% 6.3V X5R 201
C2449 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2440
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
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MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<12> H9
MEM_RESET_L
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MEM_DQ<37>
MEM_DQ<36>
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MEM_DQS_N<4>
MEM_CS_L<1>
MEM_CKE<1>
MEM_CLK_P<1>
MEM_CLK_N<1>

R2440 240 1% 1/20W MF 201

C2457 0.47UF 20% 4V CERM-X5R-1 201
C2458 0.047UF 10% 6.3V X5R 201
C2459 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2450
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<13> H9
MEM_RESET_L
MEM_DQ<41>
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MEM_DQS_P<5>
MEM_DQS_N<5>
MEM_CS_L<1>
MEM_CKE<1>
MEM_CLK_P<1>
MEM_CLK_N<1>

R2450 240 1% 1/20W MF 201

C2467 0.47UF 20% 4V CERM-X5R-1 201
C2468 0.047UF 10% 6.3V X5R 201
C2469 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2460
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<14> H9
MEM_RESET_L
MEM_DQ<49>
MEM_DQ<48>
MEM_DQ<51>
MEM_DQ<50>
MEM_DQ<55>
MEM_DQ<54>
MEM_DQ<53>
MEM_DQ<52>
MEM_DQS_P<6>
MEM_DQS_N<6>
MEM_CS_L<1>
MEM_CKE<1>
MEM_CLK_P<1>
MEM_CLK_N<1>

R2460 240 1% 1/20W MF 201

C2477 0.47UF 20% 4V CERM-X5R-1 201
C2478 0.047UF 10% 6.3V X5R 201
C2479 0.047UF 10% 6.3V X5R 201

OMIT_TABLE
U2470
DDR3-1333
FBGA
(SYM VER 2)

MEM_A_A<0> K4
MEM_A_A<1> L8
MEM_A_A<2> L4
MEM_A_A<4> K3
MEM_A_A<3> L9
MEM_A_A<6> L3
MEM_A_A<5> M9
MEM_A_A<8> M3
MEM_A_A<7> N9
MEM_A_A<9> M4
MEM_A_A<10> H8
MEM_A_A<11> M8
MEM_A_A<12> K8
MEM_A_A<13> N4
MEM_A_A<14> N8
MEM_A_A<15> J8
MEM_BA<1> J3
MEM_BA<0> K9
MEM_BA<2> J4
MEM_RAS_L F4
MEM_CAS_L G4
MEM_WE_L H4
MEM_ODT<1> G2
MEM_ZQ<15> H9
MEM_RESET_L
MEM_DQ<57>
MEM_DQ<56>
MEM_DQ<59>
MEM_DQ<58>
MEM_DQ<63>
MEM_DQ<62>
MEM_DQ<61>
MEM_DQ<60>
MEM_DQS_P<7>
MEM_DQS_N<7>
MEM_CS_L<1>
MEM_CKE<1>
MEM_CLK_P<1>
MEM_CLK_N<1>

R2470 240 1% 1/20W MF 201

SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

PP1V35_S3_MEM

C2400 2.2UF 20% 10V X5R-CERM 402
C2401 2.2UF 20% 10V X5R-CERM 402
C2410 2.2UF 20% 10V X5R-CERM 402
C2411 2.2UF 20% 10V X5R-CERM 402
C2420 2.2UF 20% 10V X5R-CERM 402
C2421 2.2UF 20% 10V X5R-CERM 402
C2430 2.2UF 20% 10V X5R-CERM 402
C2431 2.2UF 20% 10V X5R-CERM 402
C2403 0.1UF 10% 6.3V CERM-X5R 0201
C2404 0.1UF 10% 6.3V CERM-X5R 0201
C2405 0.1UF 10% 6.3V CERM-X5R 0201
C2413 0.1UF 10% 6.3V CERM-X5R 0201
C2414 0.1UF 10% 6.3V CERM-X5R 0201
C2415 0.1UF 10% 6.3V CERM-X5R 0201
C2423 0.1UF 10% 6.3V CERM-X5R 0201
C2424 0.1UF 10% 6.3V CERM-X5R 0201
C2425 0.1UF 10% 6.3V CERM-X5R 0201
C2433 0.1UF 10% 6.3V CERM-X5R 0201
C2434 0.1UF 10% 6.3V CERM-X5R 0201
C2435 0.1UF 10% 6.3V CERM-X5R 0201

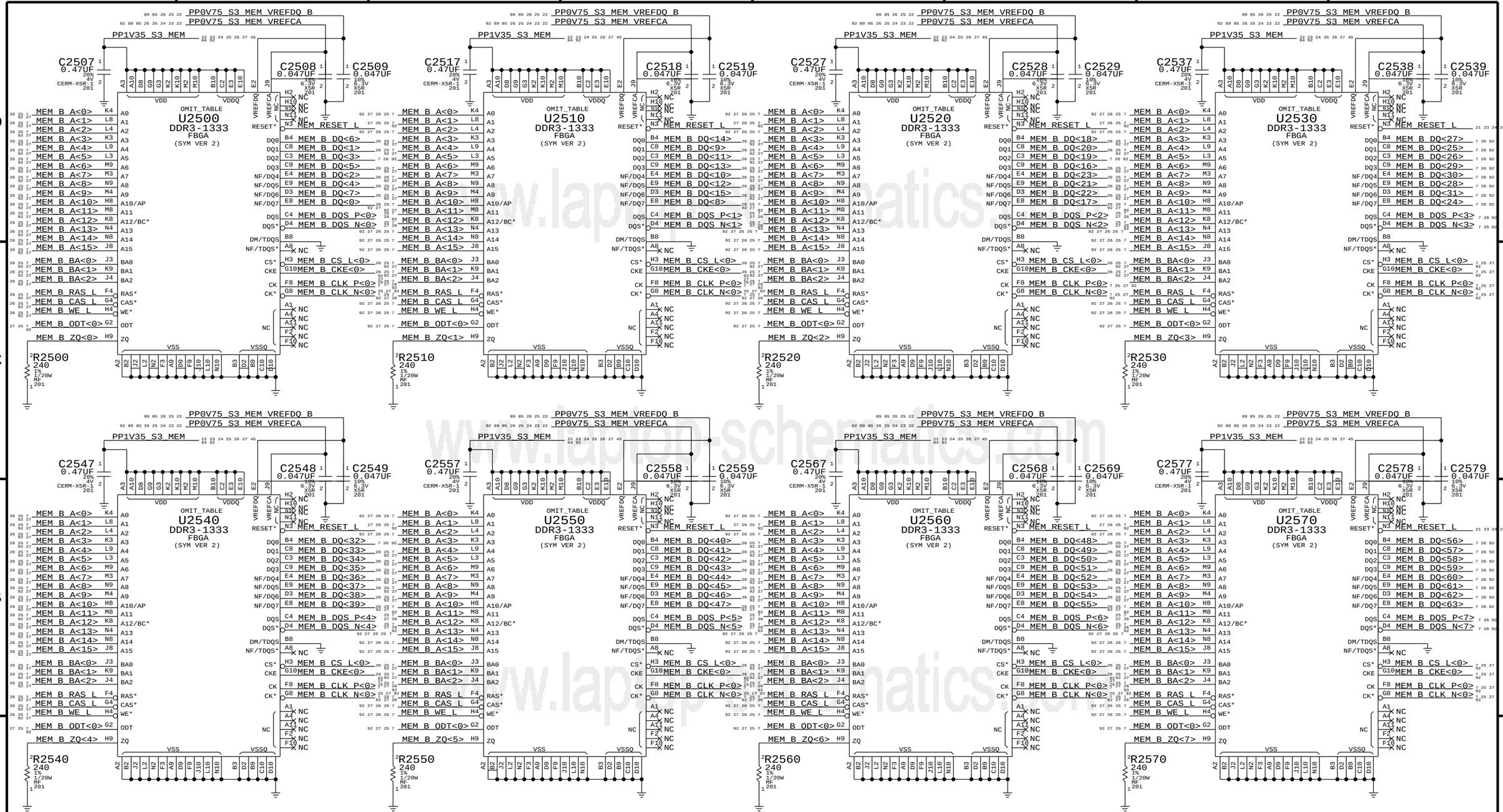
C2440 2.2UF 20% 10V X5R-CERM 402
C2441 2.2UF 20% 10V X5R-CERM 402
C2450 2.2UF 20% 10V X5R-CERM 402
C2451 2.2UF 20% 10V X5R-CERM 402
C2460 2.2UF 20% 10V X5R-CERM 402
C2461 2.2UF 20% 10V X5R-CERM 402
C2470 2.2UF 20% 10V X5R-CERM 402
C2471 2.2UF 20% 10V X5R-CERM 402
C2443 0.1UF 10% 6.3V CERM-X5R 0201
C2444 0.1UF 10% 6.3V CERM-X5R 0201
C2445 0.1UF 10% 6.3V CERM-X5R 0201
C2453 0.1UF 10% 6.3V CERM-X5R 0201
C2454 0.1UF 10% 6.3V CERM-X5R 0201
C2455 0.1UF 10% 6.3V CERM-X5R 0201
C2463 0.1UF 10% 6.3V CERM-X5R 0201
C2464 0.1UF 10% 6.3V CERM-X5R 0201
C2465 0.1UF 10% 6.3V CERM-X5R 0201
C2473 0.1UF 10% 6.3V CERM-X5R 0201
C2474 0.1UF 10% 6.3V CERM-X5R 0201
C2475 0.1UF 10% 6.3V CERM-X5R 0201

SYNC_MASTER=J15_MLB
SYNC_DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank A (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 24 OF 119
SHEET 24 OF 97



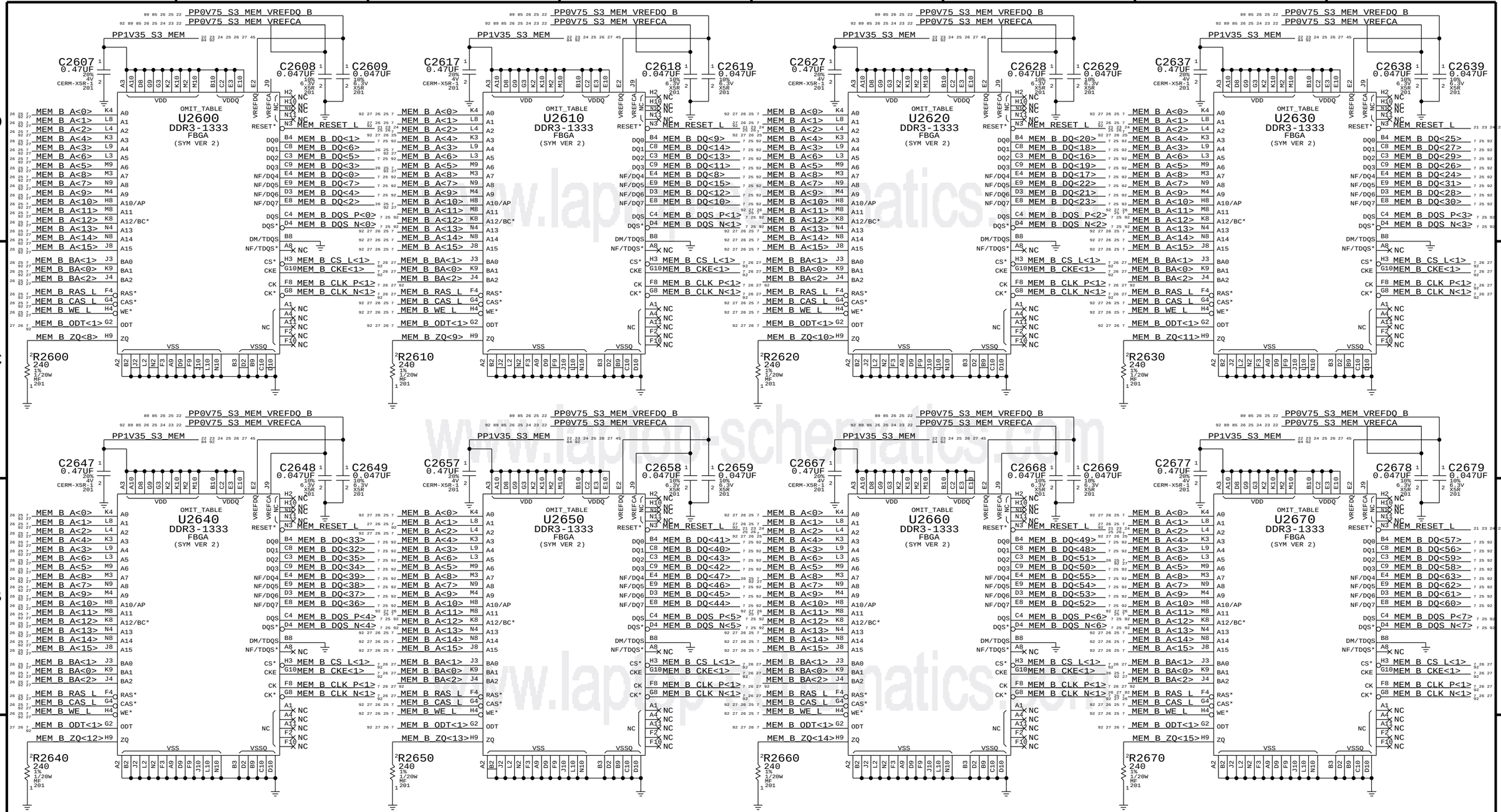
SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank B (1 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 25 OF 119
SHEET 25 OF 97



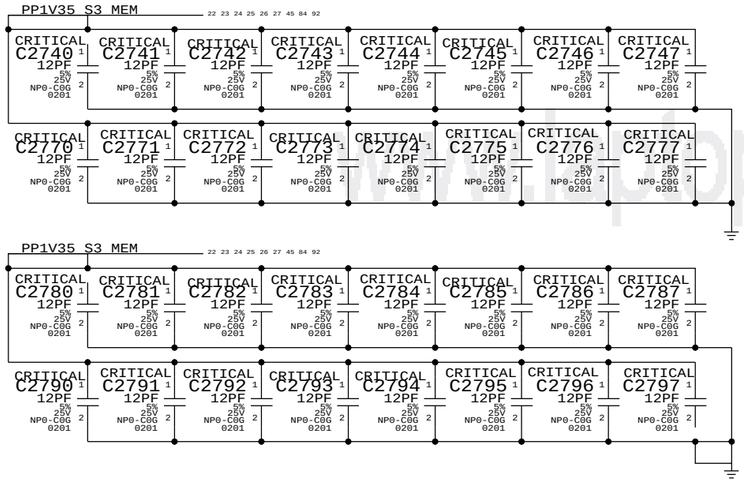
SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE
DDR3 SDRAM Bank B (2 OF 2)

Apple Inc.

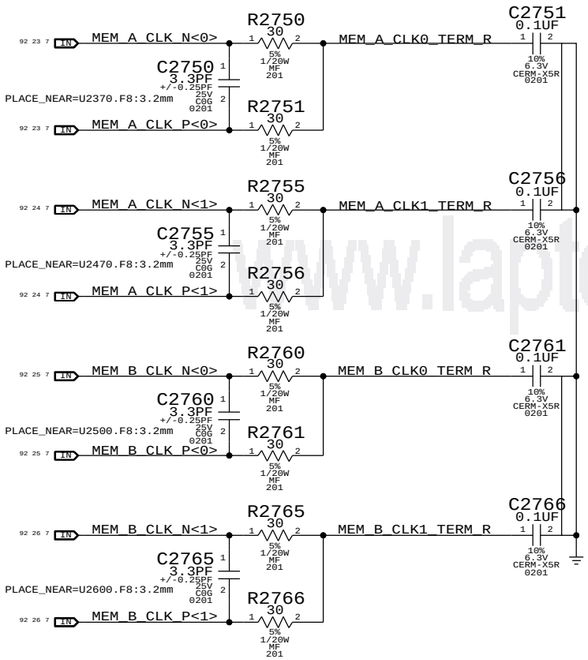
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 26 OF 119
SHEET 26 OF 97

FOR DESENSE IMPROVEMENT
PLACE ONE AT EACH DDR3L MEMORY MODULE.



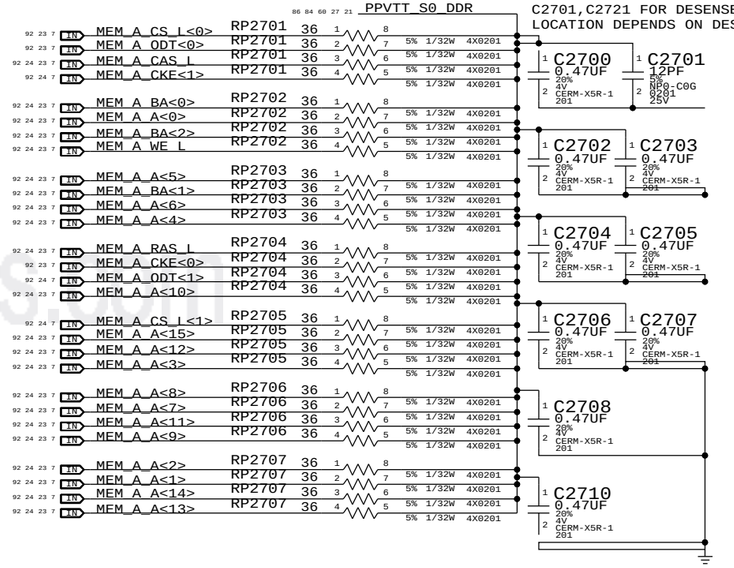
MEM Clock Termination

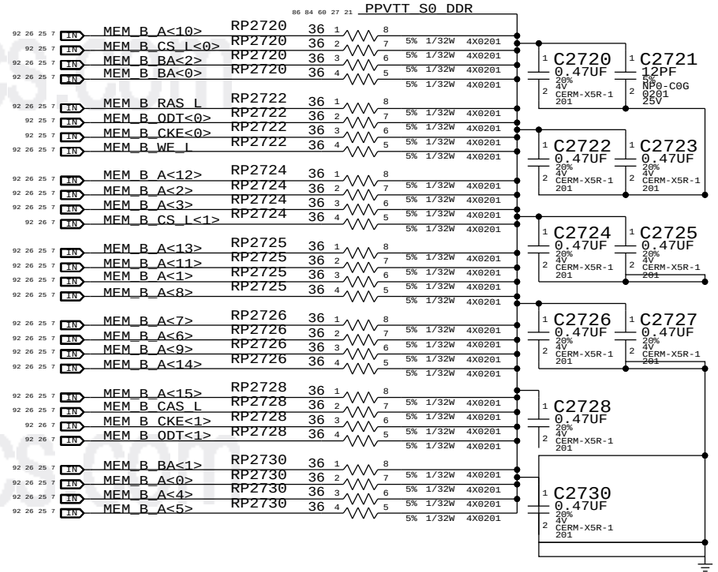
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

C2701,C2721 FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM



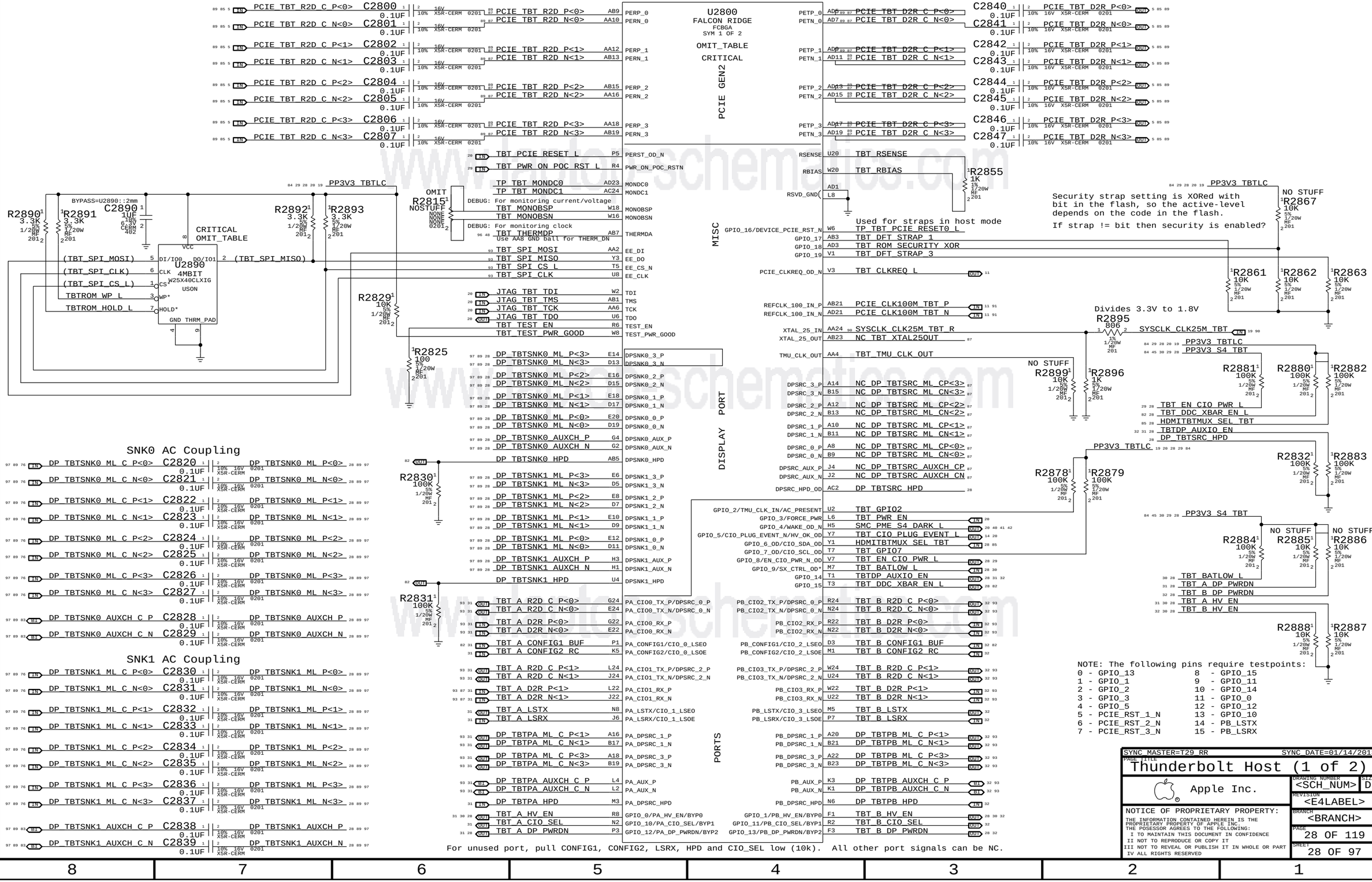


SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE: DDR3 Termination

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 27 OF 119
SHEET: 27 OF 97


U2800
FALCON RIDGE
FCBGA
SYM 1 OF 2
OMIT_TABLE
CRITICAL
PCIE GEN2
MISC
DISPLAY PORTS
U2890
4MBIT
W25X40CLXIG
USON
CRITICAL
OMIT_TABLE
BYPASS=U2890::2mm
PP3V3_TBTLC
SNK0 AC Coupling
SNK1 AC Coupling
Used for straps in host mode
Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.
If strap != bit then security is enabled?
Divides 3.3V to 1.8V
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=T29_RR
SYNC_DATE=01/14/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER <SCH_NUM>
SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 28 OF 119
SHEET 28 OF 97
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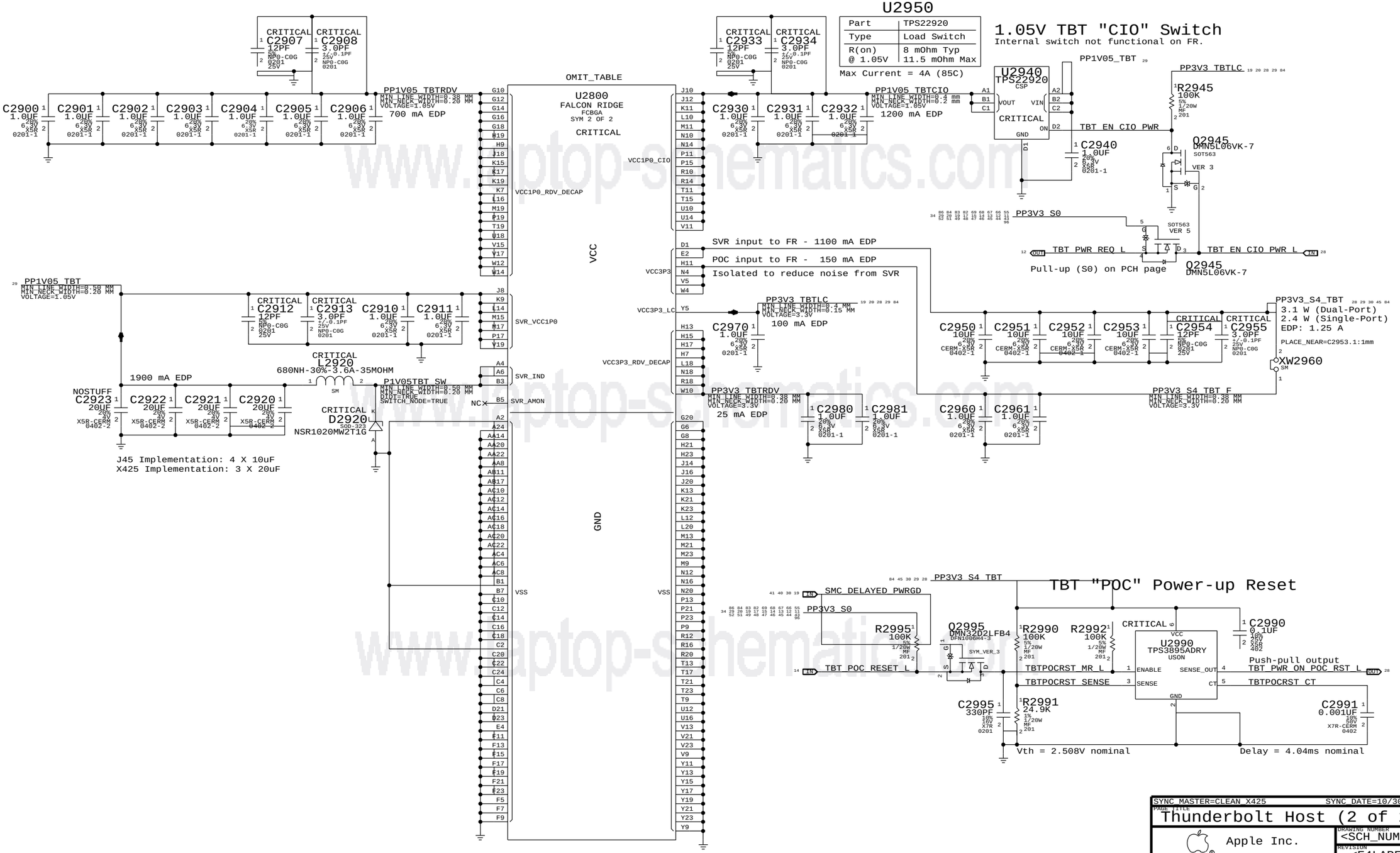

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator

C3080 USING 0603 PAKAGE IS FOR DFM TO PROTECT Q3080 (CSP)

CRITICAL
Q3080
SI8409DB
BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPBUS_G3H
8-13V Input
Changes required
for 2S.

R3080 470K 5% 1/10W MF-LF 402
C3080 0.1UF 10% 50V X7R 603-1
TBTBST_PWREN_DIV_L
R3081 330K 5% 1/10W MF-LF 402
TBTBST_PWREN_L

Q3005 DMN5L06VK-7 SOT563 VER 3
TBT_A_HV_EN
Q3005 DMN5L06VK-7 SOT563 VER 3
TBT_B_HV_EN

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here,
add property on another page.

R3091 200K 1% 1/10W MF-LF 402 <R1>
C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL
L3095
3.3UH-6.5A
PIMB063T-SM
TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
U3090
LT3957
QFN
VIN
SW
SNS1
SNS2
EN/UVLO
INTVCC
VC
RT
SS
SYNC
FBX
SGND
GND

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
TBTBST_FBX

C3085 2.2UF 20% 10V CER-X6S 0402
C3086 2.2UF 20% 10V CER-X6S 0402
C3087 68PF 5% 50V CERM 0402
R3093 49.9K 1% 1/10W MF-LF 402
R3092 73.2K 1% 1/10W MF-LF 402 <R2>
C3092 2.2UF 20% 10V CER-X6S 0402
C3093 0.0033UF 10% 50V X7R-CERM 0402
R3094 26.7K 1% 1/10W MF-LF 402
C3094 0.33UF 10% 6.3V X6S-CERM 0402

GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to
GND inside package,
no XW necessary.

R3089 0 5% 1/20W MF 0201
TBTBST_SNS1
TBTBST_SNS2
R3097 10 5% 1/10W MF-LF 402
TBTBST_VSNS
R3095 137K 1% 1/10W MF-LF 402 <Ra>
C3088 10PF 5% 50V CERM 0402
R3096 15.8K 1% 1/10W MF-LF 402 <Rb>
C3089 100PF 5% 25V CERM 402
NO STUFF

CRITICAL
D3095
PDS540XF
PWRDI5

NOTE: Change R3097 to XW3095 at PVT

PP15V_TBT
Vout = 15.47V
Max Current = 2A?
Freq = 480KHz

C3095 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L
C3096 10UF 20% 25V X5R-CERM 0603
NO STUFF
C3097 10UF 10% 25V X7R-CERM 1206
C3099 0.001UF 10% 50V X7R-CERM 0402
C3098 10UF 20% 25V X5R-CERM 0603

Vout = 1.6V * (1 + Ra / Rb)

PLACE_SIDE=BOTTOM
PLACE_SIDE=TOP

NOTE: MIRROR C3096 and C3098

Q3088 DMN5L06VK-7 SOT563 VER 3
Max Vgs: 10V
TBTBST_SHDN_DIV
R3088 330K 5% 1/10W MF-LF 402
R3087 330K 5% 1/10W MF-LF 402
Q3088 DMN5L06VK-7 SOT563 VER 3
SMC_DELAYED_PWRGD

BATLOW# Isolation

Q3000 DMN32D2LFB4 DFN1006H4-3 SYM_VER_3
PP3V3_S4_TBT
Pull-up on RR page
PM_BATLOW_L
TBT_BATLOW_L
TBT_BATLOW_L
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE
Thunderbolt Mobile Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 30 OF 119
SHEET 30 OF 97

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
PP15V_TBT
15.75V Max
CRITICAL C3287 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3280 22UF 20% 6.3V X5R-CERM 603
C3281 0.1UF 10% 16V X5R-CERM 0201
C3215 4.7UF 10% 25V X5R-CERM 0603
C3210 0.1UF 10% 16V X5R 402
CRITICAL U3210 CD3211A1RGP QFN
V3P3
VHV
ENHVU
EN
HV_EN
S0
FAULT
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
V3P3OUT
OUT
C3285 0.1UF 10% 16V X5R-CERM 0201
C3286 10UF 20% 6.3V CERM-X5R 0402
C3211 0.1UF 10% 25V X5R 402
PP3V3_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3RHV_S4_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
S4_PWR_EN
TBT_A_HV_EN
PM_SLP_S3_R_L
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
TBTHV:P15V
12V: See below
R3210 22.6K 1% 1/20W MF 201
R3211 22.6K 1% 1/20W MF 201
R3212 36.5K 1% 1/20W MF 201 <RV3P3>
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R3213 22.6K 1% 1/20W MF 201 <RHVS3>
R3214 22.6K 1% 1/20W MF 201 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

PP3V3_S4_TBTAPWR
C3220 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3220 CBTL05024 HVQFN24-COMBO
SIGNAL_MODEL=TBT_MUX
VDD
GND_THMPAD
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
GND_VOID=TRUE (Both C's)
C3277 0.47UF 20% 4V 201 CERM-X5R-1
C3276 0.47UF 20% 4V 201 CERM-X5R-1
TBT_A_D2R_C_N<1>
TBT_A_D2R_C_P<1>
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C3230 0.1UF 10% 16V X5R-CERM 0201
C3231 0.1UF 10% 16V X5R-CERM 0201
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C3232 0.22UF 20% 6.3V X5R 0201
C3233 0.22UF 20% 6.3V X5R 0201
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_CIO_SEL
TBTDP_AUXIO_EN
DP_PD
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
TBT_A_HPD
TBT_A_LSX_ML_P<1>
TBT_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)

Thunderbolt Connector A

CRITICAL L3200 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTAPWR_F
C3200 0.01UF 20% 16V X7R-CERM 0402
C3201 0.01UF 10% 16V X7R-CERM 0402
TBTACONN_20_RC
R3201 12 5% 1/20W MF 201
CRITICAL C3203 12PF 5% 25V NP0-C0G 0201
CRITICAL C3204 3.0PF +/-0.1PF 25V NP0-C0G 0201
TBTACONN_1_C
C3205 0.01UF 10% 16V X5R-CERM 0201
GND_VOID=TRUE (0-18.9V)
TBTACONN_7_C
C3206 0.01UF 10% 25V X5R-CERM 0201
CRITICAL J3200 MDP-J44 F-RT-TH
SHIELD PINS
PORT B
514-0876
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
GND0
TBT Dir
DP Dir
TBT: RX_0
TBT: TX_0
TBT: TX_1
TBT: Unused
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
C3278 0.22UF 20% 6.3V X5R 0201
C3279 0.22UF 20% 6.3V X5R 0201
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
C3274 0.47UF 20% 4V 201 CERM-X5R-1
C3275 0.47UF 20% 4V 201 CERM-X5R-1
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
R3294 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3295 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3279 470K 5% 1/20W MF 201
R3278 470K 5% 1/20W MF 201
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
C3270 0.22UF 20% 6.3V X5R 0201
C3271 0.22UF 20% 6.3V X5R 0201
R3270 470K 5% 1/20W MF 201
R3271 470K 5% 1/20W MF 201
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
C3272 0.22UF 20% 6.3V X5R 0201
C3273 0.22UF 20% 6.3V X5R 0201
R3272 470K 5% 1/20W MF 201
R3273 470K 5% 1/20W MF 201
470k R's for ESD protection on AC-coupled signals.
R3252 1M 5% 1/20W MF 201
R3251 1M 5% 1/20W MF 201
C3294 330PF 10% 16V X7R 0201
C3295 330PF 10% 16V X7R 0201
R3241 100K 5% 1/20W MF 201
C3202 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014
PAGE TITLE: Thunderbolt Connector A
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 32 OF 119
SHEET: 31 OF 97

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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

PP3V3_S5
PP15V_TBT
15.75V Max
CRITICAL C3387 100UF 20% 6.3V POLY TANT CASE-B2-SM
C3380 22UF 20% 6.3V X5R-CERM 0603
C3381 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3310 CD3211A1RGP QFN
C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 16V X5R 402
C3385 0.1UF 10% 16V X5R-CERM 0201
C3386 10UF 20% 6.3V CERM-X5R 0402
C3311 0.1UF 10% 25V X5R 402
PP3V3_S4_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
PP3V3RHV_S4_TBTBPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V
S4_PWR_EN
TBT_B_HV_EN
PM_SLP_S3_R_L
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V R3310 22.6K 1% 1/20W MF 201
TBTHV:P15V R3311 22.6K 1% 1/20W MF 201
R3312 36.5K 1% 1/20W MF 201 <RV3P3>
TBTHV:P15V R3313 22.6K 1% 1/20W MF 201 <RHVS3>
TBTHV:P15V R3314 22.6K 1% 1/20W MF 201 <RHVS0>
12V: See below
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B

PP3V3_S4_TBTBPWR
C3320 0.1UF 10% 16V X5R-CERM 0201
SIGNAL_MODEL=TBT_MUX
CRITICAL U3320 CBTL05024 HVQFN24-COMBO
GND_VOID=TRUE (Both C's)
C3377 0.47UF 20% 4V 201 CERM-X5R-1
C3376 0.47UF 20% 4V 201 CERM-X5R-1
C3330 0.1UF 10% 16V X5R-CERM 0201
C3331 0.1UF 10% 16V X5R-CERM 0201
C3332 0.22UF 20% 6.3V X5R 0201
C3333 0.22UF 20% 6.3V X5R 0201
TBT_B_D2R_N<1>
TBT_B_D2R_P<1>
TBT_B_D2R_C_N<1>
TBT_B_D2R_C_P<1>
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
DP_TBTPB_AUXCH_N
DP_TBTPB_AUXCH_P
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_HPD
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
TBT_B_D2R1_AUXDDC_N
TBT_B_D2R1_AUXDDC_P
TBT: RX_1
TBT_B_CONFIG1_RC
TBT_B_HPD
TBT: LSX_A_R2P/P2R (P/N)

CRITICAL L3300 FERR-120-OHM-3A 0603
C3300 0.01UF 20% 16V X7R-CERM 0402
C3301 0.01UF 10% 16V X7R-CERM 0402
PP3V3RHV_S4_TBTBPWR_F
TBTBCONN_20_RC
R3301 12 5% 1/20W MF 201
CRITICAL C3303 12PF 5% 25V NP0-C0G 0201
CRITICAL C3304 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL J3200 MDP-J44 F-RT-TH
SHIELD PINS
PORT A
514-0876
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
TBTBCONN_1_C
TBTBCONN_7_C
C3305 0.01UF 10% 16V X5R-CERM 0201
C3306 0.01UF 10% 25V X5R-CERM 0201
(0-18.9V)
DP_Dir TBT_Dir
TBT: TX_0
TBT: TX_1
C3370 0.22UF 20% 6.3V X5R 0201
C3371 0.22UF 20% 6.3V X5R 0201
C3372 0.22UF 20% 6.3V X5R 0201
C3373 0.22UF 20% 6.3V X5R 0201
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
470k R's for ESD protection on AC-coupled signals.

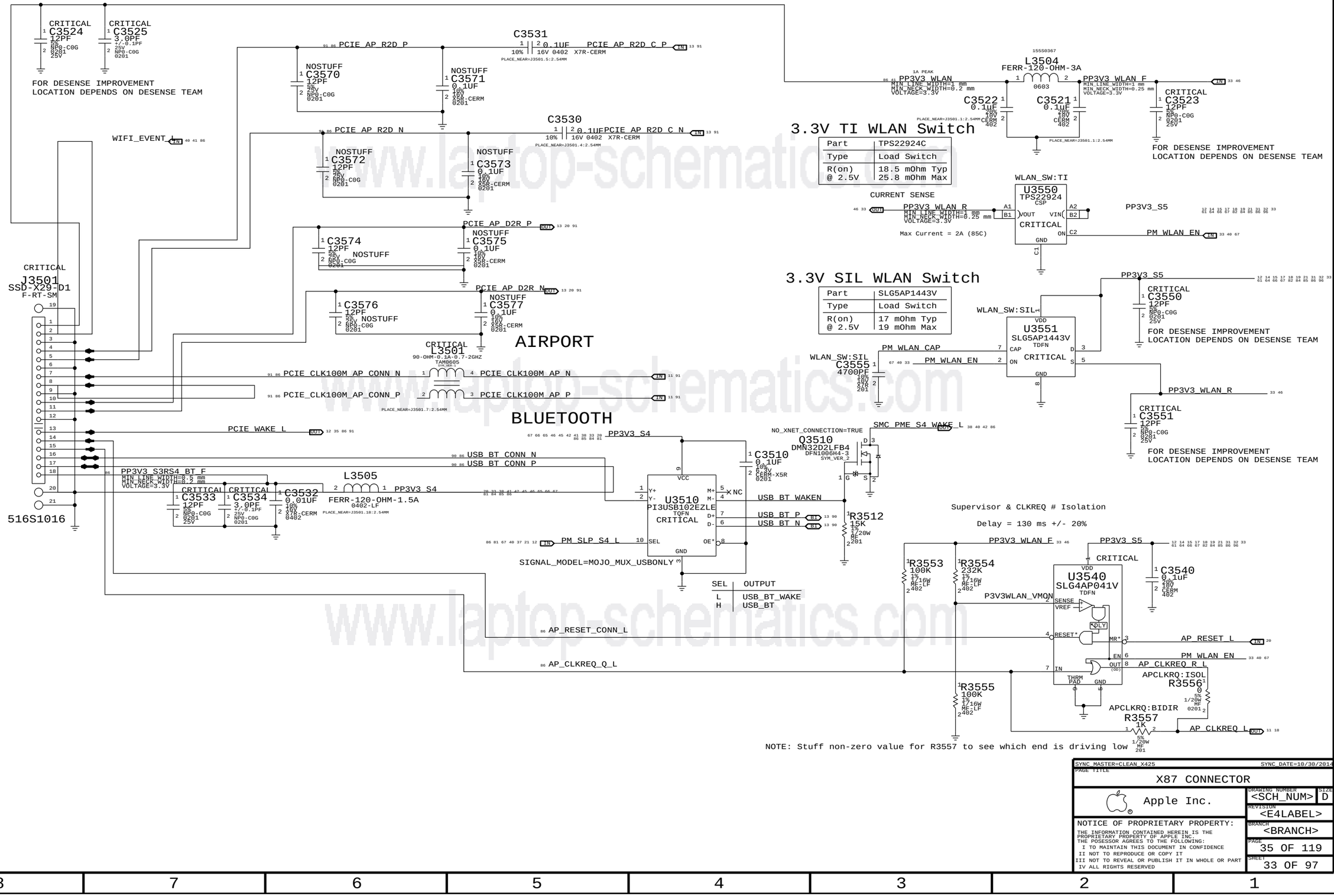
C3374 0.47UF 20% 4V 201 CERM-X5R-1
C3375 0.47UF 20% 4V 201 CERM-X5R-1
C3378 0.22UF 20% 6.3V X5R 0201
C3379 0.22UF 20% 6.3V X5R 0201
C3394 330PF 10% 16V X7R 0201
C3395 330PF 10% 16V X7R 0201
C3302 0.01UF 10% 16V X5R-CERM 0201
R3394 1K 5% 1/20W MF 201
R3395 1K 5% 1/20W MF 201
R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
R3341 100K 5% 1/20W MF 201
GND_VOID=TRUE
NO_XNET_CONNECTION=TRUE
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
DP_TBTPB_ML_P<3>
DP_TBTPB_ML_N<3>
TBT: Unused
TBT: RX_0
TBT: RX_1
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
TBT_B_CONFIG2_RC
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 33 OF 119
SHEET: 32 OF 97



SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE: X87 CONNECTOR

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DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 35 OF 119

SHEET: 33 OF 97

FOR DESENSE IMPROVEMENT

C3722 12PF 5% 50V C0G 0201 — PLACE_NEAR=J3700.3:2mm
C3723 12PF 5% 50V C0G 0201 — PLACE_NEAR=J3700.4:2mm
C3724 12PF 5% 50V C0G 0201 — PLACE_NEAR=J3700.5:2mm

PLACE_NEAR=J3700.1:3mm
CRITICAL
L3700 FERR-26-OHM-6A 0603
PP3V3_S0SW_SSD (86 84 45 34) → PP3V3_S0SW_SSD_FLT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.15mm
VOLTAGE=3.3V

C3701 0.1UF 10% 10V X5R-CERM 0201 — PLACE_NEAR=L3700.1:1mm
C3702 0.1UF 10% 10V X5R-CERM 0201 — PLACE_NEAR=L3700.1:1mm

514S0449
CRITICAL
J3700 SSD-GS3
F-RT-SM

NOSTUFF
R3700 100K 1% 1/20W MF 201

PP3V3_S0 (86 84 83 82 69 68 67 66 55 52 51 49 48 47 46 45 44 43 96 → 34)

GND_VOID
NO_TEST=TRUE

1	GND_VOID		
2	SMC_OOB1_R2D_CONN_L	52	SMC_OOB1_R2D_CONN_L
3	SMC_OOB1_D2R_CONN_L	51	SMC_OOB1_D2R_CONN_L
4		50	SSD_PCIE_SEL_L (OUT 18)
5		49	SSD_DEVSLP (IN 20)
6	PP3V3_S0	48	SMC_PWRFAIL_WARN_L (IN 40)
7	SSD_RESET_CONN_L	47	SSD_PWR_FET_EN (IN 34 66)
8	NC_SSD_MFG_RSVD	46	
9		45	PCIE_SSD_D2R_N<3> (OUT 5 85 89)
10	PCIE_SSD_R2D_N<3>	44	PCIE_SSD_D2R_P<3> (OUT 5 85 89)
11	PCIE_SSD_R2D_P<3>	43	
12		42	PCIE_SSD_D2R_N<2> (OUT 5 85 89)
13	PCIE_SSD_R2D_N<2>	41	PCIE_SSD_D2R_P<2> (OUT 5 85 89)
14	PCIE_SSD_R2D_P<2>	40	
15		39	
16	PCIE_SSD_R2D_N<1>	38	PCIE_SSD_D2R_N<1> (OUT 5 85 89)
17	PCIE_SSD_R2D_P<1>	37	PCIE_SSD_D2R_P<1> (OUT 5 85 89)
18		36	
19	PCIE_SSD_R2D_N<0>	35	PCIE_SSD_D2R_N<0> (OUT 5 85 89)
20	PCIE_SSD_R2D_P<0>	34	PCIE_SSD_D2R_P<0> (OUT 5 85 89)
21		33	
22	SSD_CLKREQ_CONN_L	32	
23		31	PCIE_CLK100M_SSD_N (IN 11 91)
24		30	PCIE_CLK100M_SSD_P (IN 11 91)
25		29	
26		59	
27		60	
28		61	
54		62	
55		63	
56			
57			
58			

Gumstick3 Connector

PCIE_SSD_R2D_C_N<3> (89 85 5 IN) C3710 0.22UF 20% 6.3V X6S-CERM 0201 2 GND_VOID=TRUE
PCIE_SSD_R2D_C_P<3> C3711 0.22UF
PCIE_SSD_R2D_C_N<2> C3712 0.22UF
PCIE_SSD_R2D_C_P<2> C3713 0.22UF
PCIE_SSD_R2D_C_N<1> C3714 0.22UF
PCIE_SSD_R2D_C_P<1> C3715 0.22UF
PCIE_SSD_R2D_C_N<0> C3716 0.22UF
PCIE_SSD_R2D_C_P<0> C3717 0.22UF

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

OOB Isolation

PP3V3_S0SW_SSD (86 84 45 34)

C3718 0.1UF 10% 10V X5R-CERM 0201 — BYPASS=U3710::5 mm
CRITICAL 74LVC1G08 SOT891 U3710 08
SMC_OOB1_R2D_L (IN 40)
NC

PP3V3_S0 (86 84 83 82 59 58 67 66 55 52 51 49 48 47 46 45 44 43 96 → 34)

C3719 0.1UF 10% 10V X5R-CERM 0201 — BYPASS=U3711::5 mm
CRITICAL 74LVC1G08 SOT891 U3711 08
SMC_OOB1_D2R_L (OUT 40)
NC

R3701 100K 1% 1/20W MF 201

Supervisor & CLKREQ# Isolation

Delay = ~55ms

PP3V3_S0SW_SSD (34 45 84 86)
PP3V42_G3H (19 37 38 40 41 42 43 50 56 57 67 84 86)

R3740 100K 1% 1/20W MF 201
R3741 232K 1% 1/20W MF 201
R3742 100K 1% 1/20W MF 201

CRITICAL
U3740 SLG4AP016V TDFN
APN 343S0511

C3740 0.1UF 10% 6.3V CERM-X5R 0201

P3V3SSD_VMON
SENSE 0.7V
DLY
RESET* → SSD_RESET_L (IN 20)
MR*
EN ← SSD_PWR_FET_EN (IN 34 66)
OUT (OD) → SSD_CLKREQ_L (OUT 11)
IN
THRM PAD
GND

SSD_PWR_FET_EN (66 34) = SSD_PWR_FET_EN (34 66)
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_X425 SYNC_DATE=08/15/2014

PAGE TITLE: SSD Connector

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DRAWING NUMBER	<SCH_NUM>
SIZE	D
REVISION	<E4LABEL>
BRANCH	<BRANCH>
PAGE	37 OF 119
SHEET	34 OF 97

U3900 BCM15700 FBGA SYM 3 OF 3 CRITICAL OMIT_TABLE

U3900 BCM15700 FBGA SYM 2 OF 3 CRITICAL OMIT_TABLE

U3900 BCM15700 FBGA SYM 1 OF 3 CRITICAL OMIT_TABLE

L3902 1.0UH-1.6A-55MOHM 1008 P1V35 CAM SRVLXD PHASE

L3901 1.0UH-1.6A-55MOHM 1008 P1V2 CAM SRVLXC PHASE

L3903 220-OHM-1.4A 0603

L3904 220-OHM-1.4A 0603

L3906 22NH 0402

PP1V35 CAM

PP1V35 DDR CLK

PP0V675 CAM VREF

PP1V2 CAM PCIE VDD FLT

PP1V2 CAM PVDD FLT

PP1V8 CAM

PP1V2 CAM

PP1V2 CAM XTALPCIEVDD

PP1V35 CAM SRVLXD PHASE

P1V2 CAM SRVLXC PHASE

GND CAM PVSSD

GND CAM PVSSC

(=PP3V3_S3RS0_CAMERA)

PP3V3_S3RS0_CAMERA

I2C CAM SMBDBG CLK

I2C CAM SMBDBG DAT

I2C CAM SCK

I2C CAM SDA

CAM RAMCFG2

CAM RAMCFG1

CAM RAMCFG0

CAM GPIO3

CAM UARTCTS

CAM UARTRXD

CAM UARTRTS

CAM UARTTXD

CAM TEST OUT

CAM TEST MODE

CAM XTAL FREQ

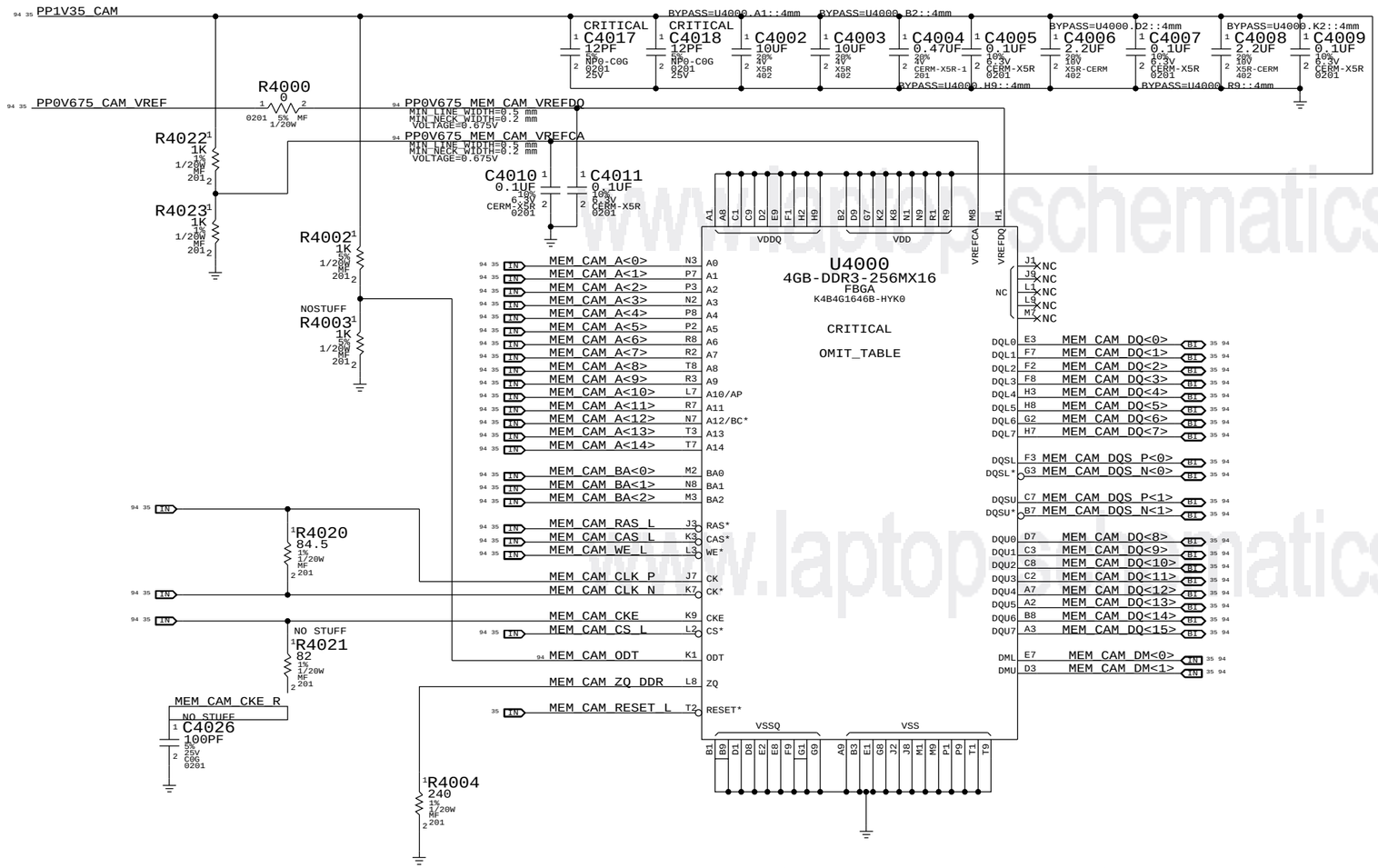
CAM XTAL SEL

PU on PCH page

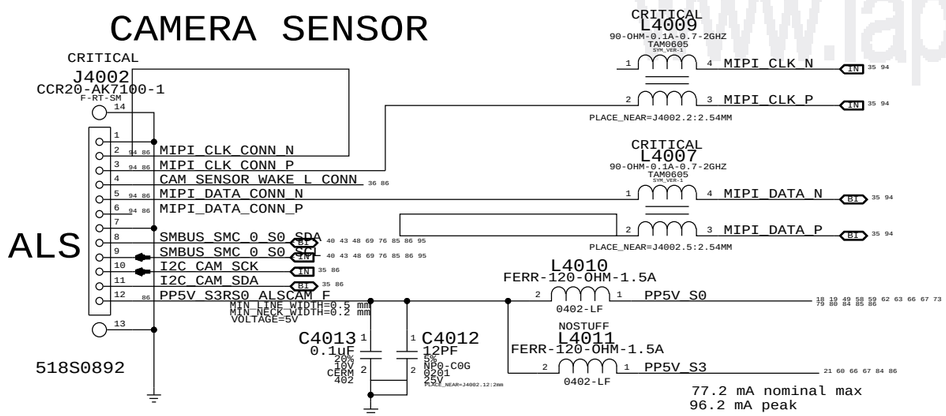
PU = 25MHz

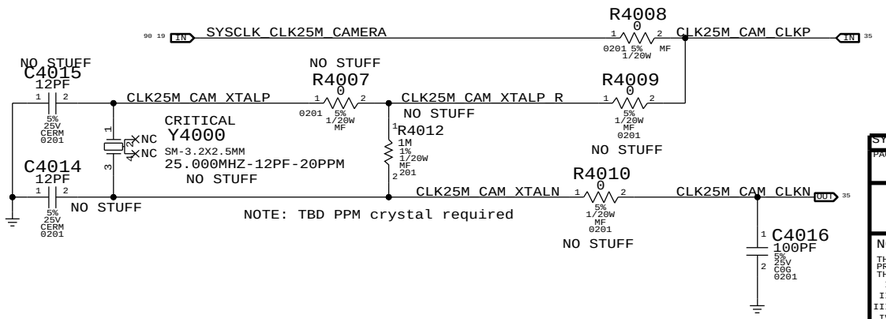
PU = 1.35V

SYNC_MASTER=CLEAN_X42S	SYNC_DATE=10/30/2014
PAGE TITLE	Camera 1 of 2
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 39 OF 119
	SHEET 35 OF 97



CAMERA SENSOR





remove DRAM SPD Straps

DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE: Camera 2 of 2

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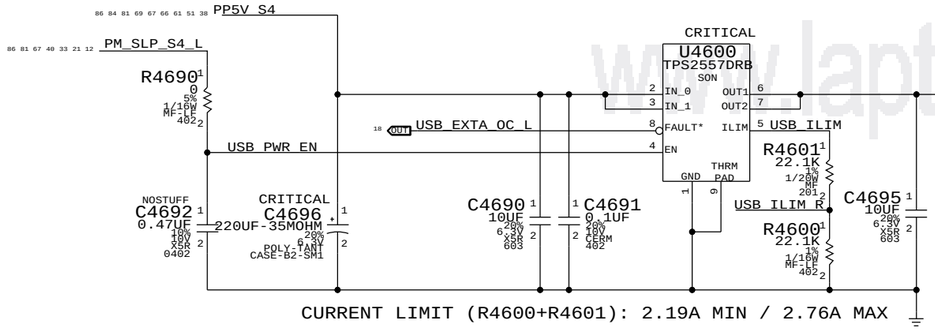
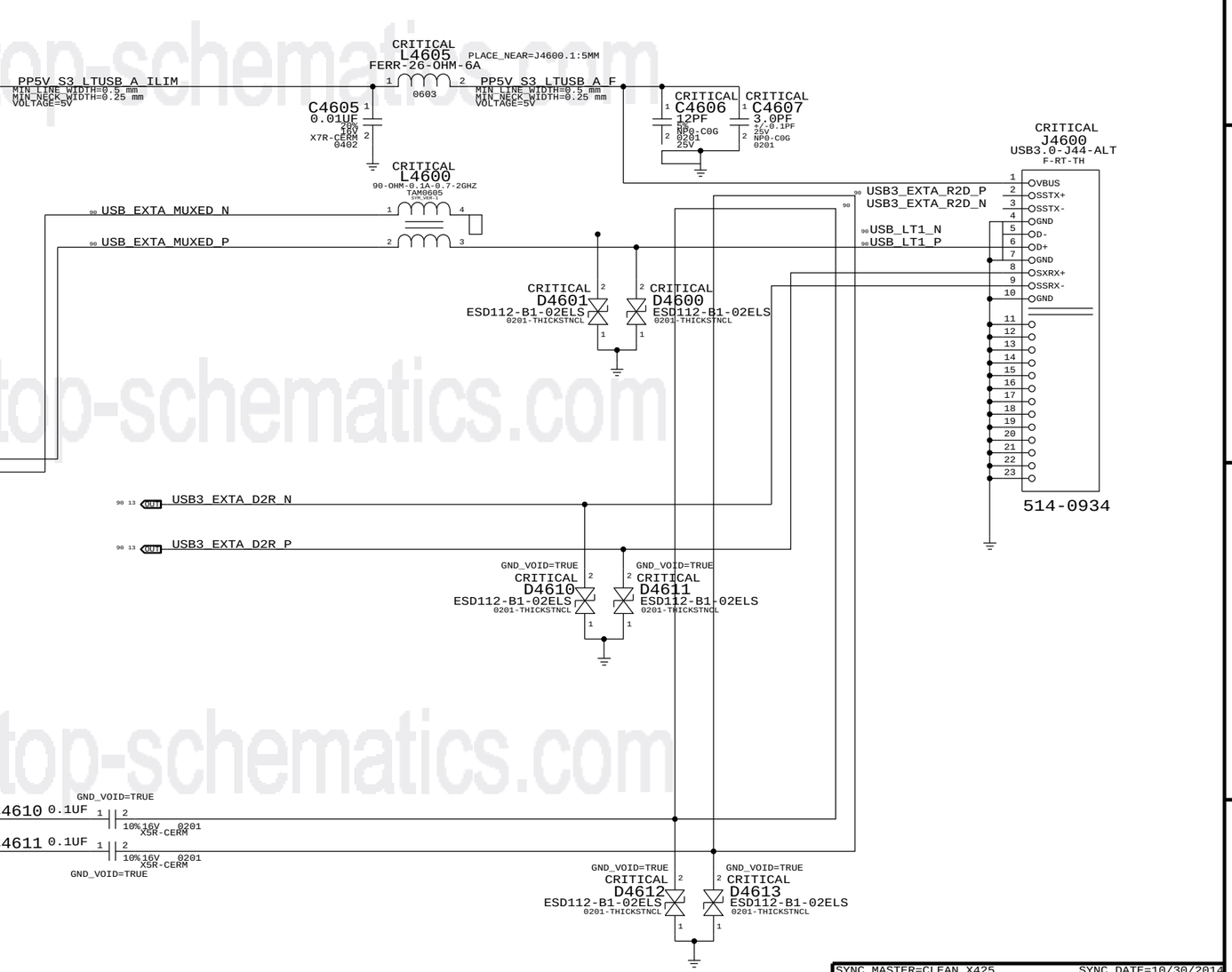
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 40 OF 119
SHEET: 36 OF 97

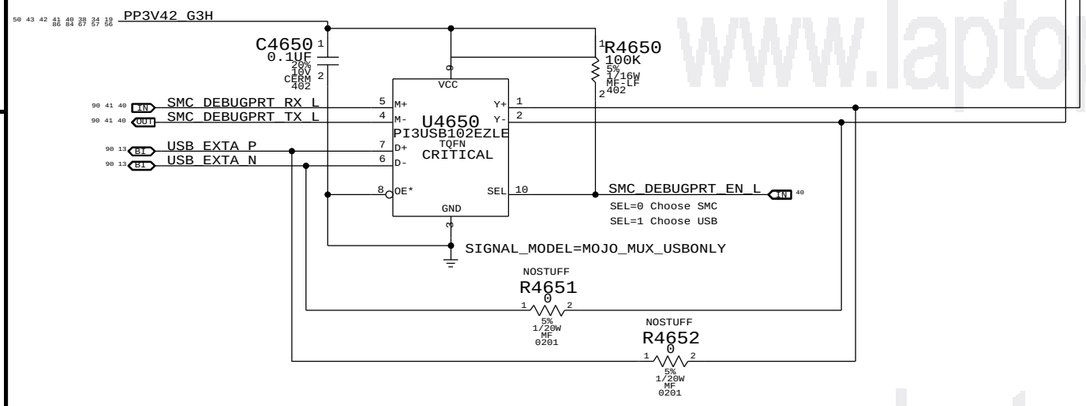
USB Port Power Switch

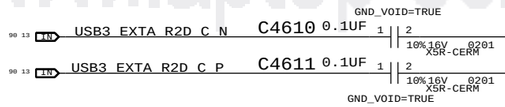


Left USB Port A



USB/SMC Debug Mux





SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 46 OF 119
SHEET: 37 OF 97

IPD CONNECTOR

CRITICAL
J4801
DF40CG1.5-48DS-0.4V
F-ST-SM

XW4801
SM
PLACE_NEAR=J4801:3MM

CRITICAL
F4809
2.5A-16V-0.10HM
1812

PPVIN_S4_TPAD
PPVIN_S4_TPAD_FUSE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=28V

CRITICAL
C4805 12PF 10% 100V CERM 0402
C4808 1.0UF 10% 35V CERM-X5R 0402
C4806 0.1UF 10% 35V CER-X5R 0201
C4807 0.1UF 10% 35V CER-X5R 0201
PLACE_NEAR=J4801.7:5mm

GND_ACTUATOR
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

NOSTUFF
R4891 0 5% 1/16W MF-LF 402

SMBUS_SMC_2_S3_SDA	19	20	SMC_ACTUATOR_EN_R_L
SMBUS_SMC_2_S3_SCL	21	22	TPAD_VBUS_EN
TPAD_NC3	23	24	TPAD_ACTUATOR_THRMTRIP_L
SMC_PME_S4_WAKE_L	25	26	PP5V_S4_TPAD_F
PP3V3_S4	27	28	SMC_LID
	29	30	
	31	32	
TPAD_SPI_INT_L	35	36	USB_TPAD_P
TPAD_SPI_BUS_EN	37	38	USB_TPAD_N
	39	40	
TPAD_SPI_SCLK	41	42	I2C_IOXP_SCL
TPAD_SPI_MISO	43	44	IOXP2_INT_L
TPAD_SPI_CS_L	45	46	I2C_IOXP_SDA
TPAD_SPI_MOSI	47	48	TPAD_NC4
	51	52	

NOSTUFF
R4890 0 5% 1/16W MF-LF 402

APN 516S1035
CONNECT WITH 516S1037

PP3V3_S4
NOSTUFF
R4893 100K 5% 1/20W MF 201
R4808 0 1/20W MF 0201
SMC_ACTUATOR_EN_L
L4803 FERR-120-OHM-1.5A 0402-LF
PP5V_S4_TPAD_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
C4801 100PF 5% 25V C0G 0201
C4803 0.1UF 10% 10V CERM 402
C4804 12PF 5% 25V NP0-C0G 0201 CRITICAL

Keyboard Connector

518S0752
CRITICAL
J4813
F-RT-SM
FF14A-30C-R11DL-B-3H

PP3V3_S4
PP3V42_G3H
C4811 12PF 5% 25V NP0-C0G 0201 CRITICAL
C4812 12PF 5% 25V NP0-C0G 0201 CRITICAL

WS_KBD1	30	29
WS_KBD2	28	27
WS_KBD3	26	25
WS_KBD4	24	23
WS_KBD5	22	21
WS_KBD6	20	19
WS_KBD7	18	17
WS_KBD8	16	15
WS_KBD9	14	13
WS_KBD10	12	11
WS_KBD11	10	9
WS_KBD12	8	7
WS_KBD13	6	5
WS_KBD14	4	3
WS_KBD15_CAP	2	1
WS_KBD16_NUM		
WS_KBD17		
WS_KBD18		
WS_KBD19		
WS_KBD20		
WS_KBD21		
WS_KBD22		
WS_KBD23		
WS_KBD_ONOFF_L		
WS_LEFT_SHIFT_KBD		
WS_LEFT_OPTION_KBD		
WS_CONTROL_KBD		

WS_KBD15_C
R4814 113 1% 1/10W MF-LF 402
WS_KBD16N
R4815 0 5% 1/10W MF-LF 402
R4810 1K 5% 1/10W MF-LF 402
SMC_ONOFF_L
PLACE_NEAR=J4813.5:5MM
C4810 0.1UF 20% 10V CERM 402

PART WILL NOT WORK WITH BOOST.

SMC Manual Reset & Isolation

LEFT SHIFT, OPTION & CONTROL KEYS COMBINED WITH POWER BUTTON CAUSE SMC RESET# ASSERTION.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).

PP3V42_G3H
BYPASS=U4850.10:5:5 mm
C4850 0.1UF 10% 10V X7R-CERM 0402
VDD

U4850
SLG4AP4103
TQFN

PP3V3_S4	4 OE (IPD)		
WS_LEFT_SHIFT_KBD	1 IN_1 (IPD)	OUT_1 9	WS_LEFT_SHIFT_KEY
WS_LEFT_OPTION_KBD	2 IN_2 (IPD)	OUT_2 8	WS_LEFT_OPTION_KEY
WS_CONTROL_KBD	3 IN_3 (IPD)	OUT_3 7	WS_CONTROL_KEY
		OUT_ALL# 6	Pull-up in U5110. SMC_TPAD_RST_L
	GND 5	THRM PAD 11	

IO EXPANDER / KEYBOARD INTERFACE

PP3V3_S4
R4831 10K 5% 1/20W MF 201
R4830 100K 5% 1/20W MF 201
CRITICAL
C4833 12PF 5% 25V NP0-C0G 0201
C4830 1UF 10% 6.3V CERM 402
BYPASS=U4830.B4:E2:5MM
BYPASS=U4830.B3:E2:2MM
C4831 0.1UF 10% 6.3V CERM-X5R 0201
C4832 0.1UF 10% 6.3V CERM-X5R 0201

U4830
PCAL6416A
VFBGA

IOXP2_INT_L	A3	INT*	
	B5	ADDR	
I2C_IOXP_SCL	A5	SCL	
I2C_IOXP_SDA	A4	SDA	
IOXP2_RESET_L	A2	RESET*	
	B3	VCCI	
	B4	VCCP	
	E2	GND	
	A1	P0_0	WS_KBD5
	C3	P0_1	WS_KBD6
	B1	P0_2	WS_KBD7
	C1	P0_3	WS_KBD9
	C2	P0_4	WS_KBD12
	D1	P0_5	WS_KBD8
	E1	P0_6	WS_KBD17
	D2	P0_7	WS_KBD18
	E3	P1_0	WS_KBD19
	E4	P1_1	WS_KBD10
	D3	P1_2	WS_KBD14
	E5	P1_3	WS_KBD13
	D4	P1_4	WS_KBD11
	D5	P1_5	
	C5	P1_6	WS_CONTROL_KEY
	C4	P1_7	WS_LEFT_OPTION_KEY
			WS_LEFT_SHIFT_KEY

NOSTUFF
C4834 0.01UF 10% 16V X5R-CERM 0201

311S0597
(Write: 0x42 Read: 0x43)

PP3V3_S4
R4802 R4801 R4852 R4853 R4854 R4855 R4856 R4857
10K 5% 1/20W MF 201

PP3V3_S4
R4858 R4859 R4860 R4861 R4862
10K 5% 1/20W MF 201

PP3V3_S4
R4821 10K 5% 1/20W MF 201
R4820 100K 5% 1/20W MF 201
BYPASS=U4820.B4:E2:5MM
BYPASS=U4820.B3:E2:2MM
C4820 1UF 10% 6.3V CERM 402
C4821 0.1UF 10% 6.3V CERM-X5R 0201
C4822 0.1UF 10% 6.3V CERM-X5R 0201
R4822 2.0K 5% 1/20W MF 201
R4823 2.0K 5% 1/20W MF 201

U4820
PCAL6416A
VFBGA

IOXP1_INT_L	A3	INT*	
	B5	ADDR	
I2C_IOXP_SCL	A5	SCL	
I2C_IOXP_SDA	A4	SDA	
IOXP1_RESET_L	A2	RESET*	
	B3	VCCI	
	B4	VCCP	
	E2	GND	
	A1	P0_0	WS_KBD23
	C3	P0_1	WS_KBD2
	B1	P0_2	WS_KBD1
	C1	P0_3	WS_KBD3
	C2	P0_4	WS_KBD4
	D1	P0_5	WS_KBD20
	E1	P0_6	WS_KBD22
	D2	P0_7	WS_KBD21
	E3	P1_0	TP_IOXP1_0
	E4	P1_1	TP_IOXP1_1
	D3	P1_2	TP_IOXP1_2
	E5	P1_3	TP_IOXP1_3
	D4	P1_4	TP_IOXP1_4
	D5	P1_5	IOXP1_DEBUG
	C5	P1_6	WS_KBD16N
	C4	P1_7	IOXP1_LED_DRV

NOSTUFF
C4824 0.01UF 10% 16V X5R-CERM 0201

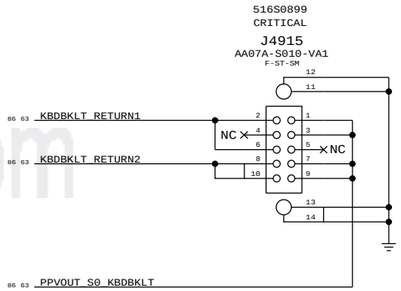
NOSTUFF
R4824 0 5% 1/20W MF 0201
SMC_ONOFF_L

Q4840
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2
WS_KBD15_C
R4840 100K 1% 1/16W MF-LF 402

311S0597
(Write: 0x40 Read: 0x41)

SYNC_MASTER=CLEAN_X425G	SYNC_DATE=09/10/2014
PAGE TITLE	KEYBOARD/TRACKPAD (1 OF 2)
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 48 OF 119
	SHEET 38 OF 97

Keyboard Backlight Connector



SYNC_MASTER=CLEAN_MAXWELL SYNC_DATE=07/02/2014

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

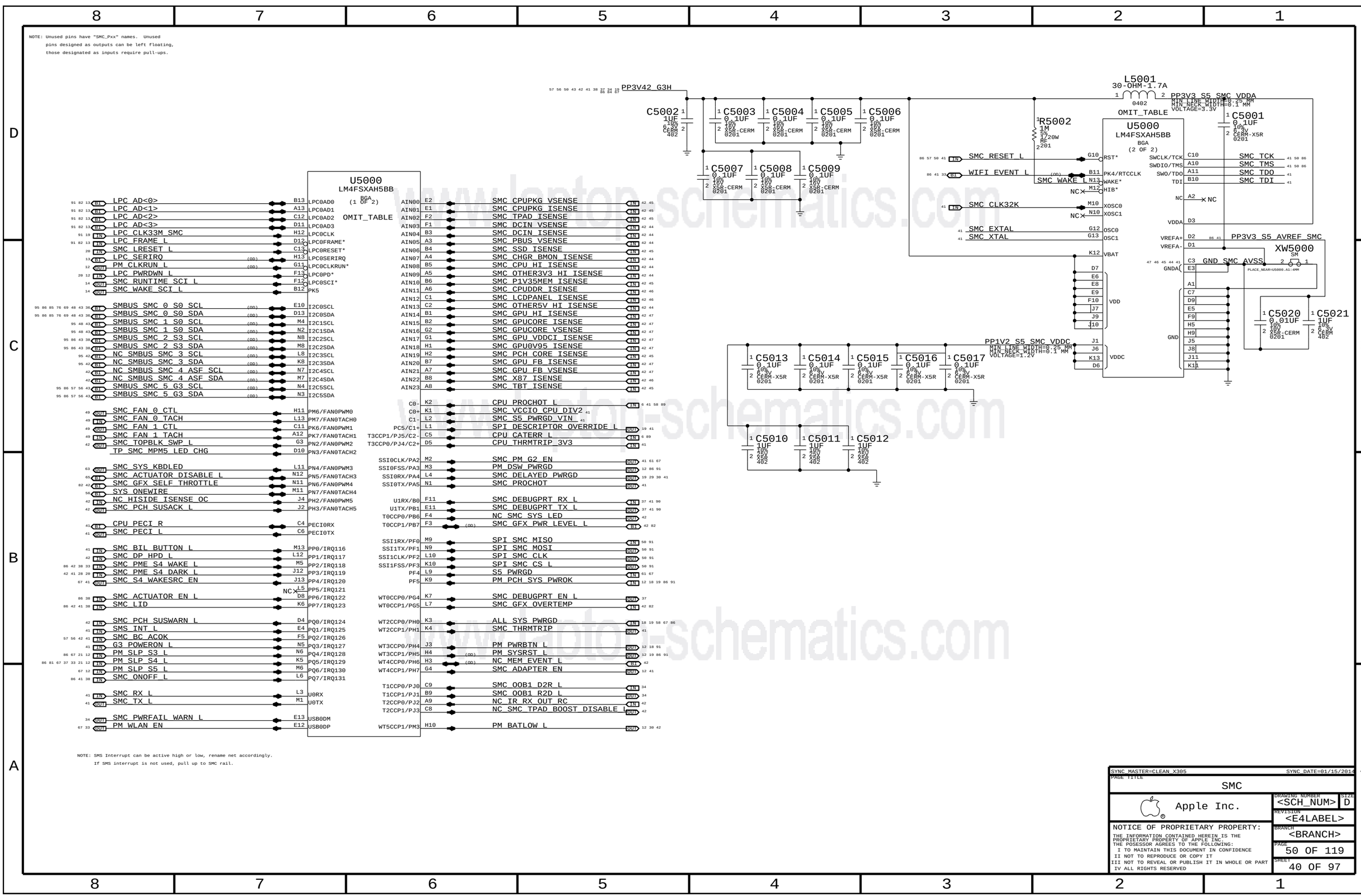
REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 49 OF 119

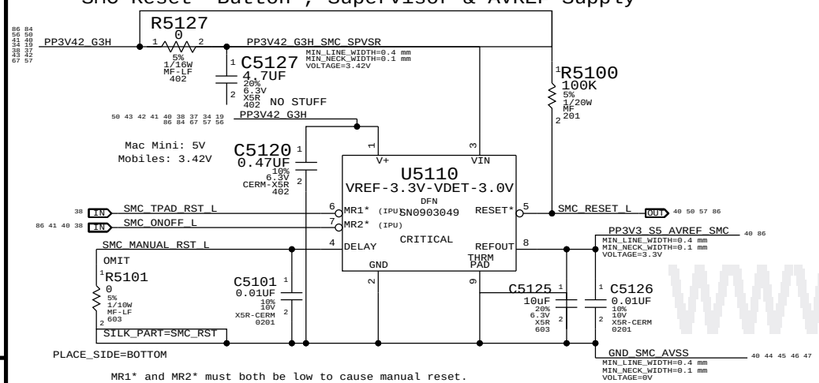
SHEET 39 OF 97

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SYNC_MASTER=CLEAN_X305	SYNC_DATE=01/15/2014
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 50 OF 119
	SHEET 40 OF 97

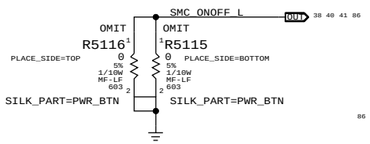
SMC Reset "Button", Supervisor & AVREF Supply



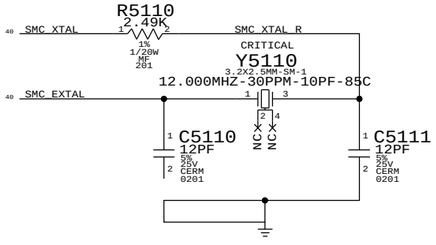
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

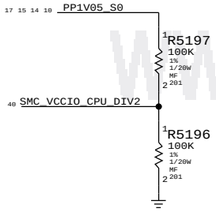
Debug Power "Buttons"



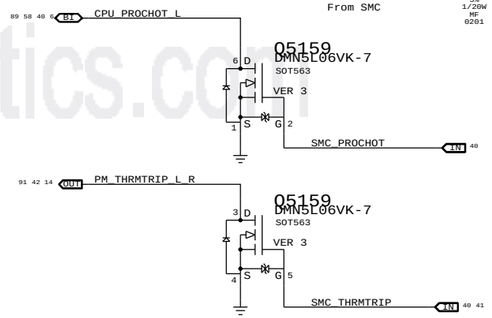
SMC Crystal Circuit

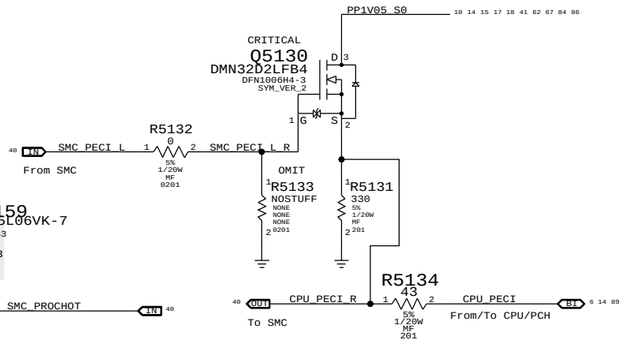


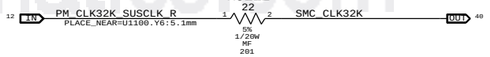
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ

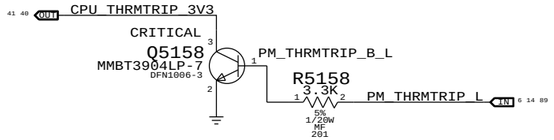


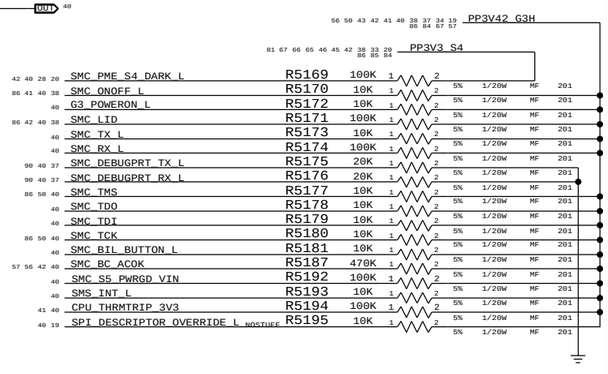
SMC12 PECI SUPPORT

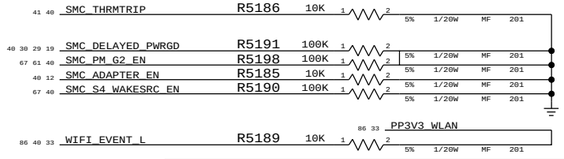












SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE
SMC Shared Support

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 51 OF 119
SHEET 41 OF 97

SMC_BC_ACOK
NC_HISIDE_ISENSE_OC
SMC_CPUPKG_VSENSE
SMC_CPUPKG_ISENSE
SMC_TPAD_ISENSE
SMC_DCIN_VSENSE
SMC_DCIN_ISENSE
SMC_PBUS_VSENSE
SMC_SSD_ISENSE
SMC_CHGR_BMON_ISENSE
SMC_CPU_HI_ISENSE
SMC_OTHER3V3_HI_ISENSE
SMC_P1V35MEM_ISENSE
SMC_CPUDDR_ISENSE
SMC_LCDPANEL_ISENSE
SMC_OTHER5V_HI_ISENSE
SMC_GPU_HI_ISENSE
SMC_GPUCORE_ISENSE
SMC_GPUCORE_VSENSE
SMC_GPU_VDDCI_ISENSE
SMC_GPU0V95_ISENSE
SMC_PCH_CORE_ISENSE
SMC_GPU_FB_ISENSE
SMC_GPU_FB_VSENSE
SMC_X87_ISENSE
SMC_TBT_ISENSE
NC_SMBUS_SMC_4_ASF_SCL
NC_SMBUS_SMC_4_ASF_SDA
NC_SMBUS_SMC_3_SCL
NC_SMBUS_SMC_3_SDA
NC_SMC_TPAD_BOOST_DISABLE_L
SMC_PME_S4_DARK_L

NC_SMC_SYS_LED
NC_MEM_EVENT_L
NC_IR_RX_OUT_RC
SMC_GFX_SELF_THROTTLE
SMC_GFX_PWR_LEVEL_L

GPU HI ISENSE

PM_THRMTRIP_L_R

SMC_SUSACK:YES
R5230 0 5% 1/20W MF 201
SMC_PCH_SUSWARN_L → PCH_SUSWARN_L
R5231 0 5% 1/20W MF 201
SMC_PCH_SUSACK_L → PCH_SUSACK_L
SMC_SUSACK:YES

Q5260 DMN32D2LFB4 (CRITICAL)
SMC_GFX_OVERTEMP

Spare S4 IRQ

PP3V3_S4
R5259 100K 5% 1/20W MF 201
SMC_DP_HPD_L

PP3V3_S4
R5282 100K 5% 1/20W MF 201
SMC_PME_S4_WAKE_L (MAKE_BASE=TRUE)

Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99
SM
NC, NC, NC, NC
PP3V42_G3H
SMC_LID_R
R5250 0 5% 1/20W MF 0201
SMC_LID
C5250 0.001UF 10% 50V X7R-CERM 0402

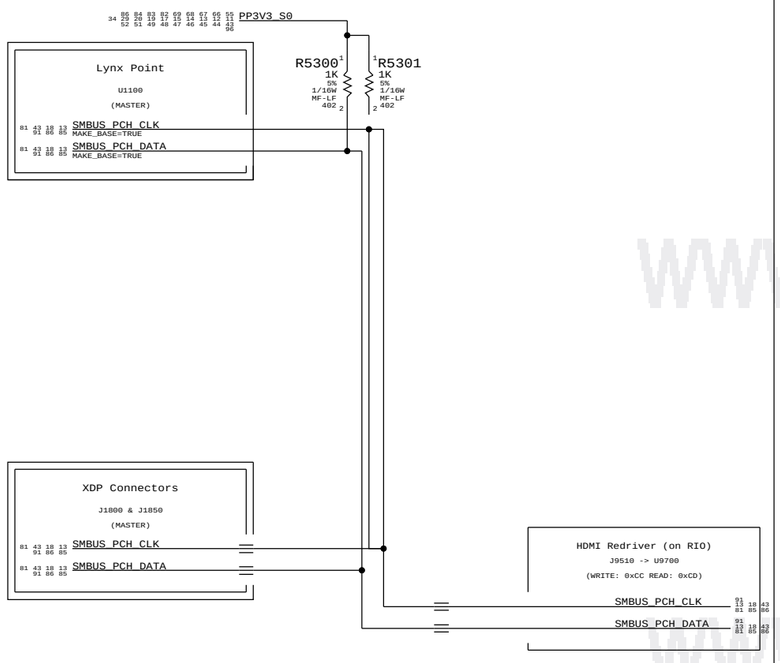
R5283 1K 5% 1/20W MF 201
SMC_TOPBLK_SWP_L → PCH_STRP_TOPBLK_SWP_L

PM_BATLOW_L

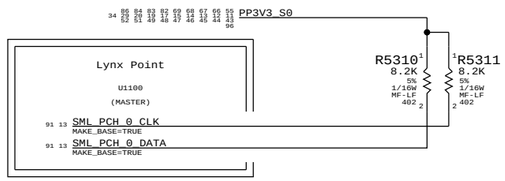
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	

PAGE TITLE: SMC Project Support
Apple Inc.
DRAWING NUMBER: <SCH_NUM>
SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 52 OF 119
SHEET: 42 OF 97

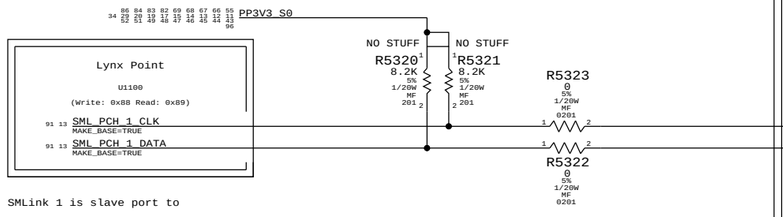
PCH SMBus "0" Connections



PCH "SMLink 0" Connections



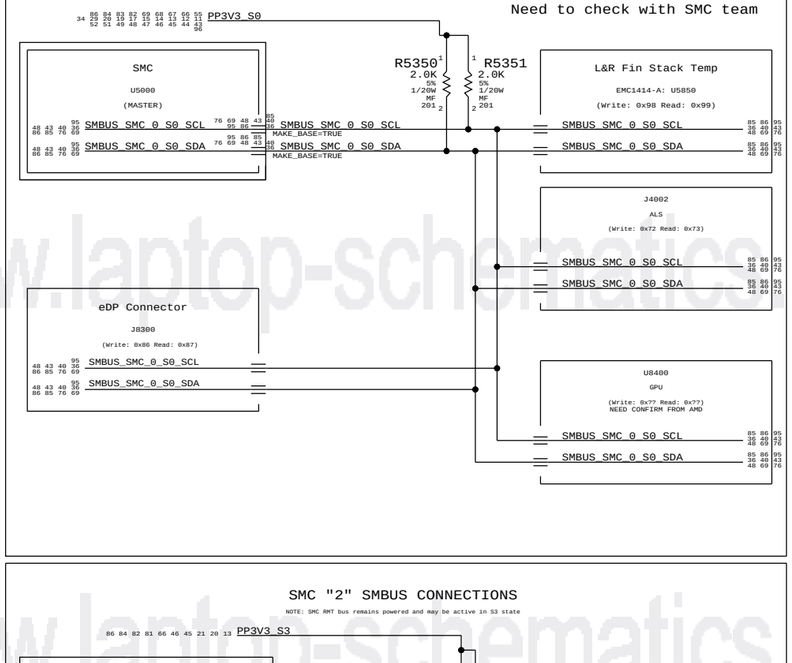
PCH "SMLink 1" Connections



SMLink 1 is slave port to
access PCH & CPU via PECI.

SMC "0" SMBus Connections

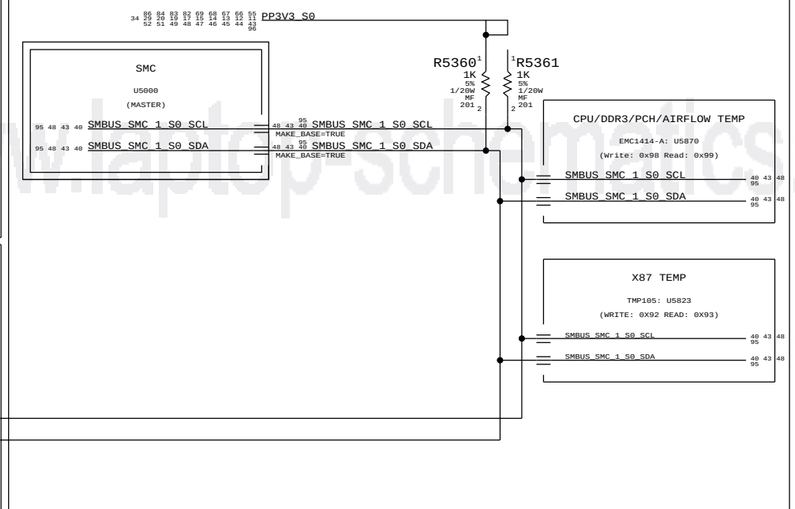
Need to check with SMC team



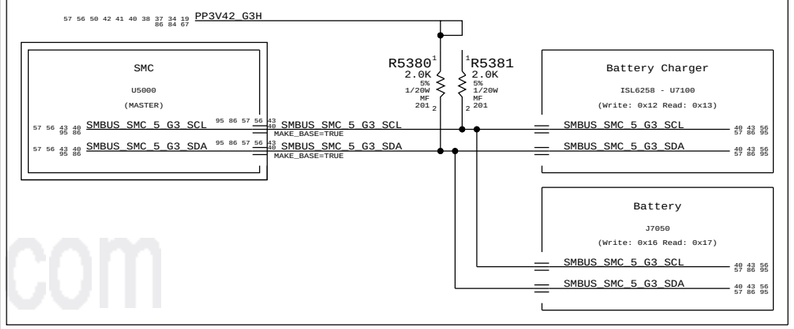
SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state

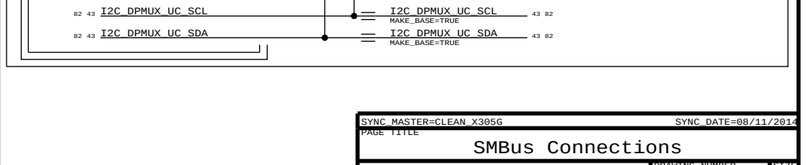
SMC "1" SMBUS CONNECTIONS



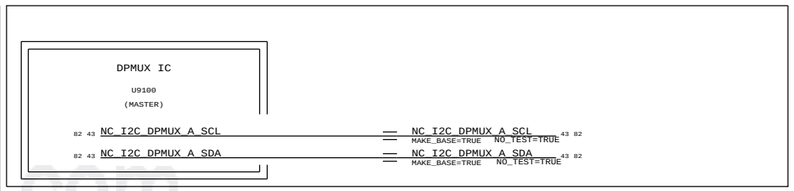
SMC "5" SMBUS CONNECTIONS

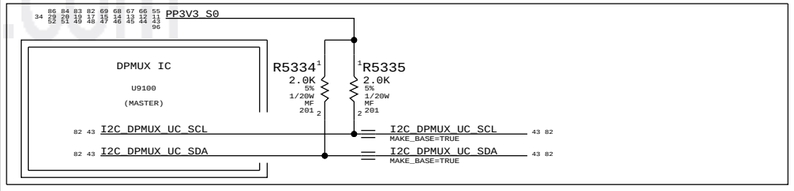


SMC "4" SMBUS CONNECTIONS



SMC "3" SMBUS CONNECTIONS





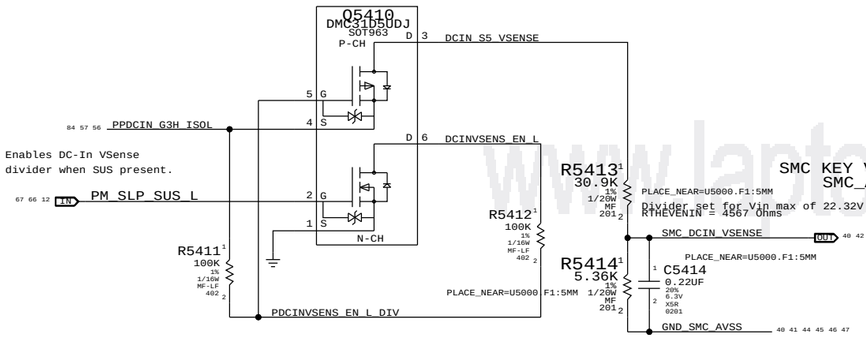
SYNC_MASTER=CLEAN_X305G SYNC_DATE=08/11/2014

PAGE TITLE: SMBus Connections

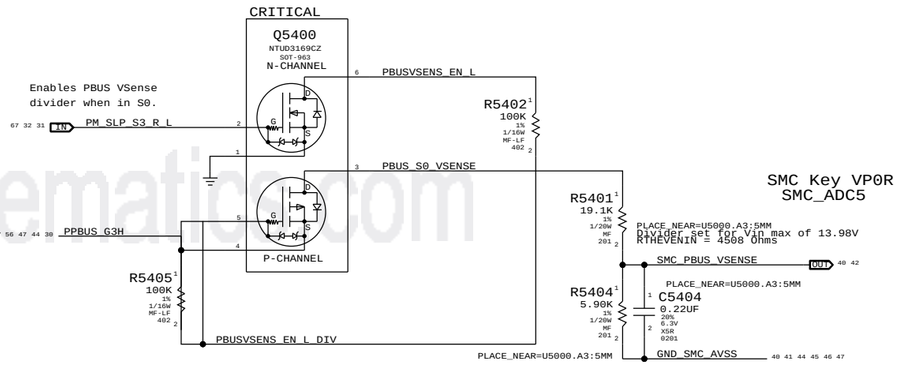
Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 53 OF 119
SHEET: 43 OF 97

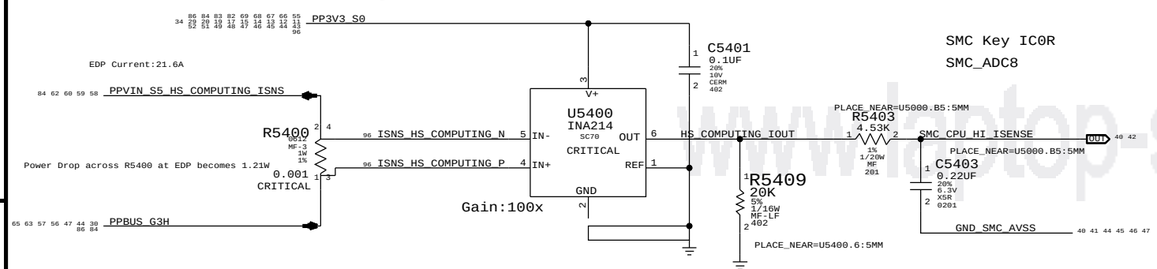
DC-In Voltage Sense Enable & Filter



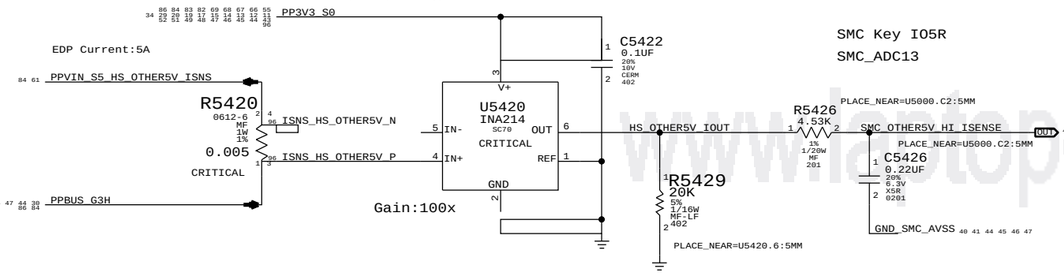
PBUS Voltage Sense Enable & Filter



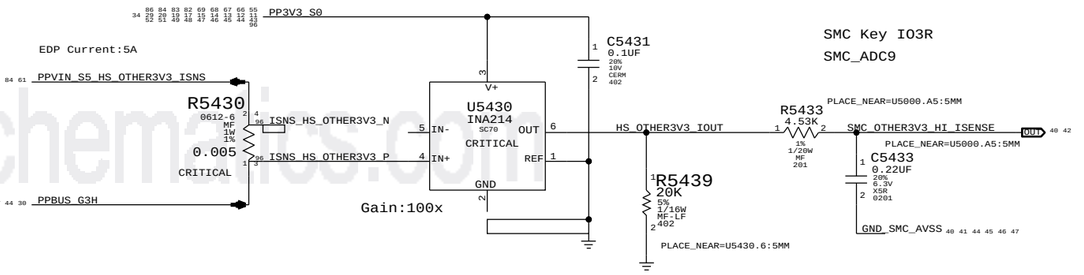
COMPUTING High Side Current Sense / Filter



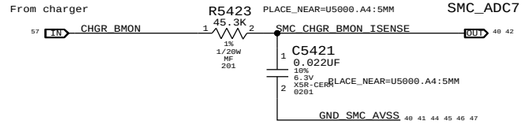
OTHERS (5V) High Side Current Sense / Filter



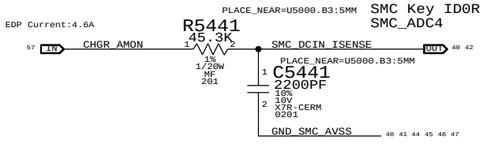
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: High Side Voltage and Current Sensing

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

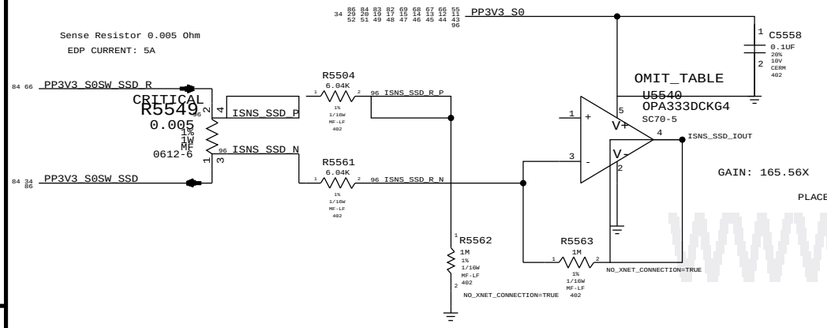
REVISION: <E4LABEL>

BRANCH: <BRANCH>

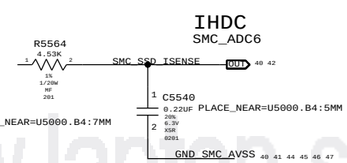
PAGE: 54 OF 119

SHEET: 44 OF 97

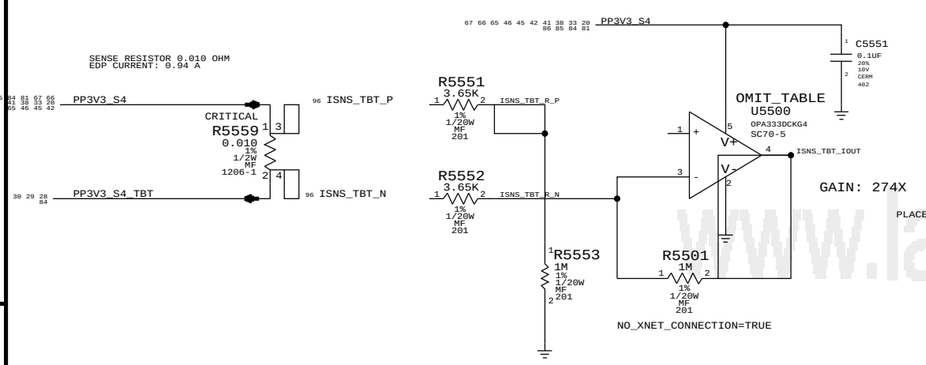
SSD CURRENT SENSE



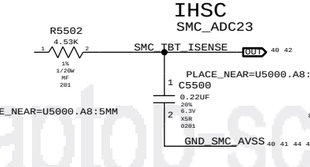
IHDC
SMC_ADC6



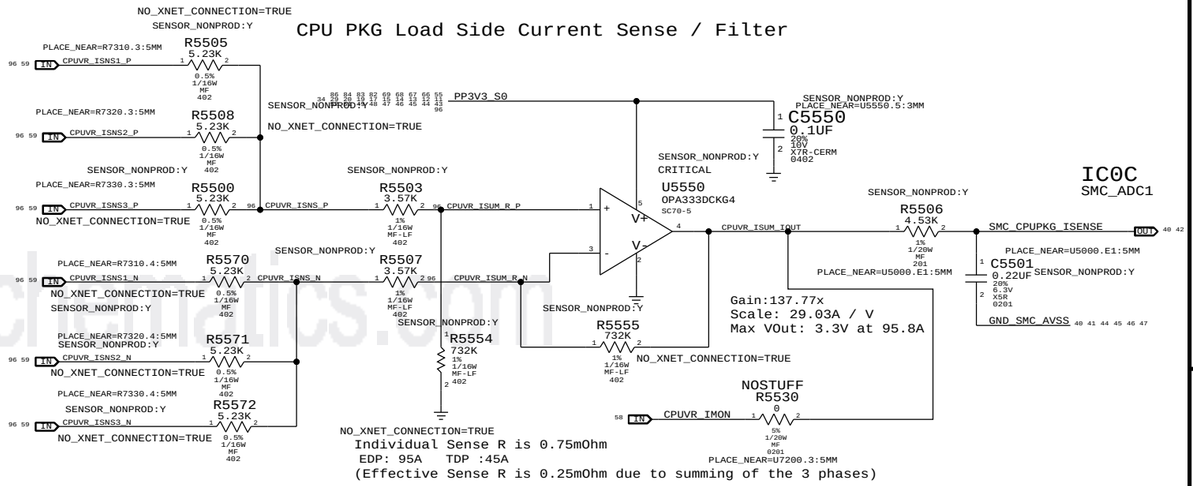
TBT Router CURRENT SENSE



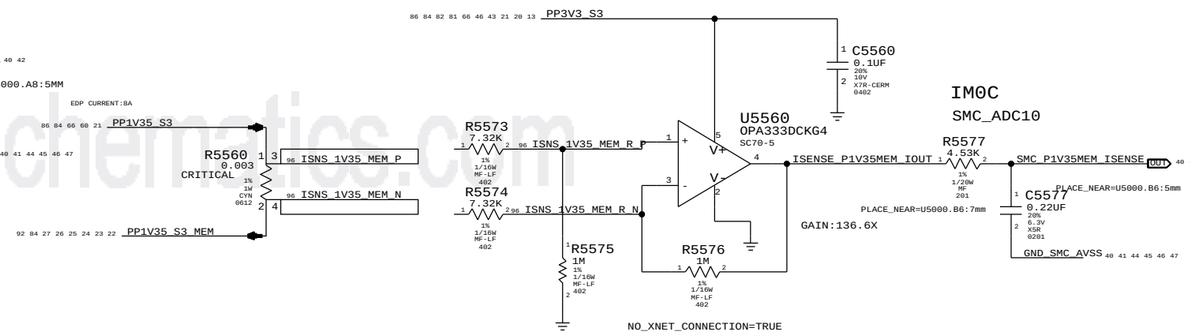
IHSC
SMC_ADC23



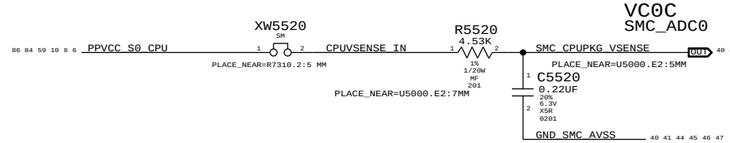
CPU PKG Load Side Current Sense / Filter



DDR3L 1.35V DRAM ONLY CURRENT SENSE / FILTER

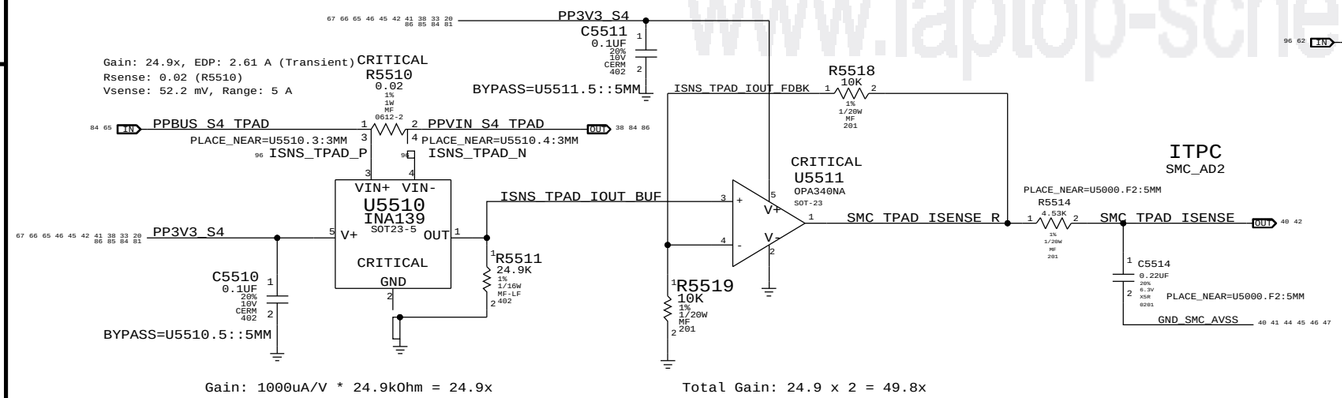


CPU Vcore Voltage Sense / Filter



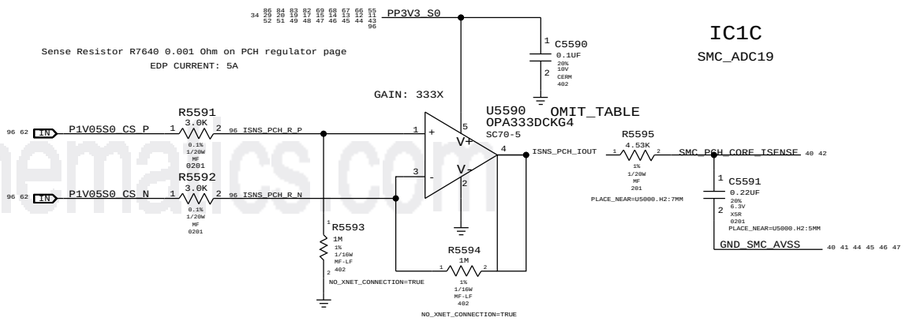
VC0C
SMC_ADC0

TRACKPAD CURRENT SENSE



ITPC
SMC_AD2

PCH CORE CURRENT SENSE



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00107	3	IC,OPAMP,NCS333QS3,SC70-5	U5500,U5540,U5590	CRITICAL	

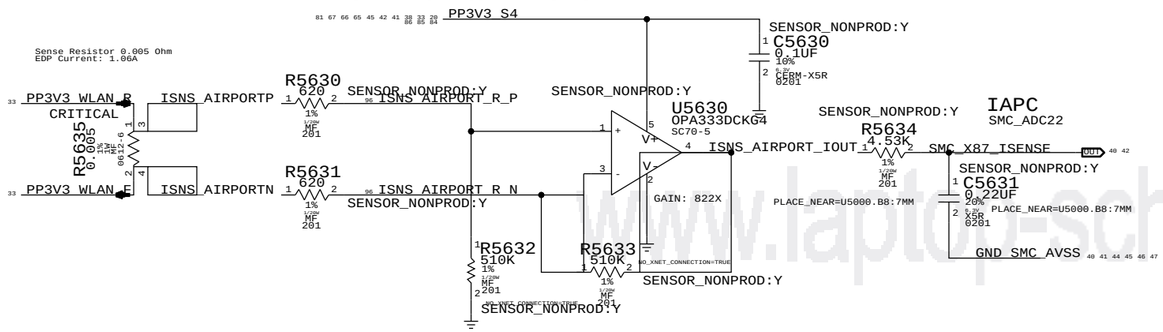
SYNC_MASTER=CLEAN_X425G SYNC_DATE=09/10/2014

PAGE TITLE
Load Side Voltage and Current Sensing

Apple Inc.

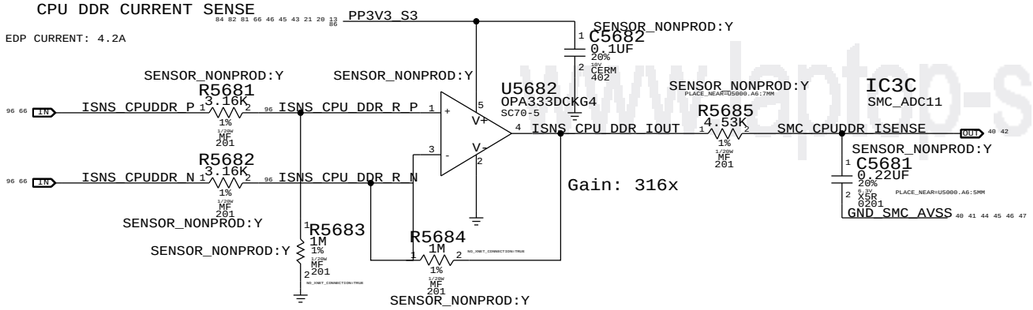
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 55 OF 119
SHEET 45 OF 97

X87 AIRPORT CURRENT SENSE



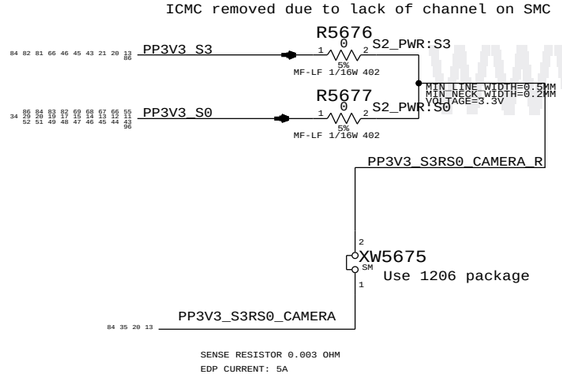
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF	C5601,C5631,C5600,C5681,C5671		SENSOR_NONPROD:N

CPU DDR CURRENT SENSE



S2 CAMERA CONTROLLER CURRENT SENSE

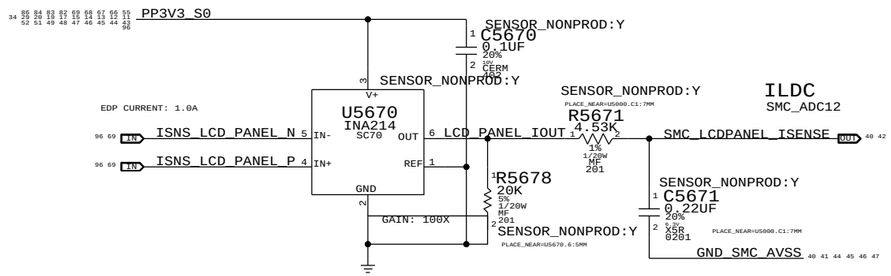
ICMC removed due to lack of channel on SMC



SENSE RESISTOR 0.003 OHM

EDP CURRENT: 5A

LCD PANEL CURRENT SENSE



SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/14/2014

PAGE TITLE

Debug Sensors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

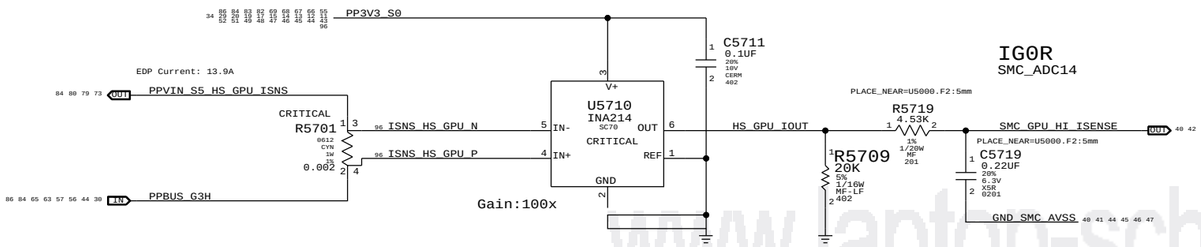
REVISION <E4LABEL>

BRANCH <BRANCH>

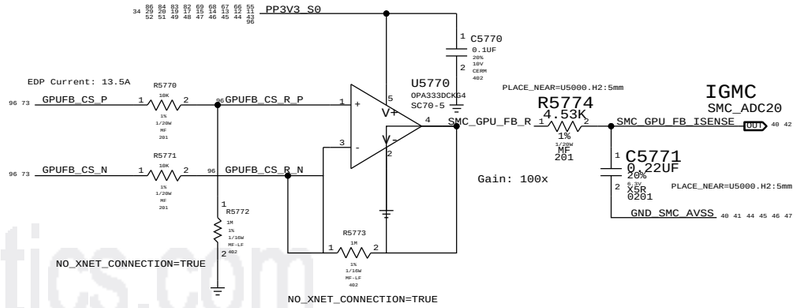
PAGE 56 OF 119

SHEET 46 OF 97

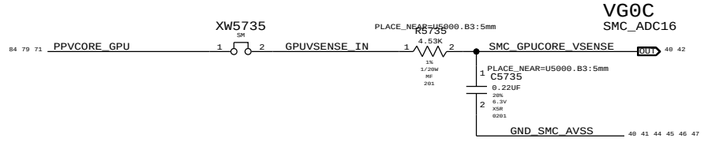
GRAPHICS High Side Current Sense



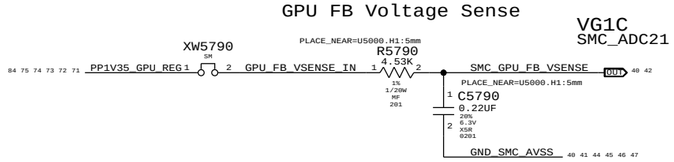
GPU FB Current Sense



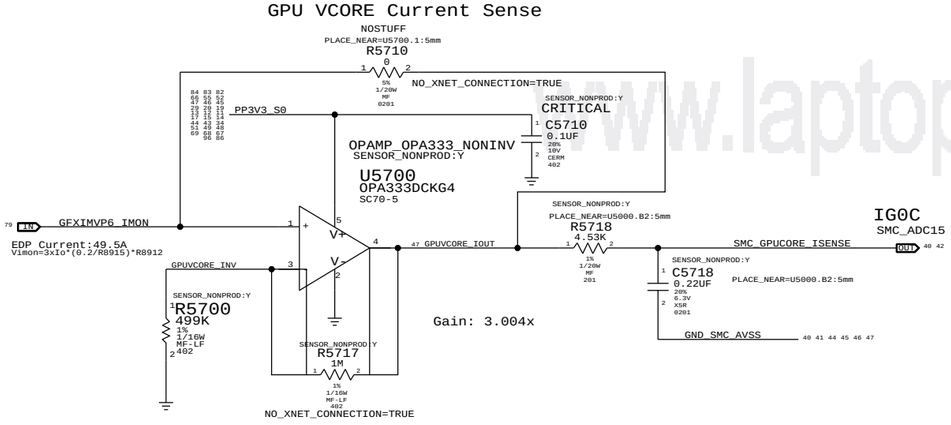
GPU VCORE Voltage Sense



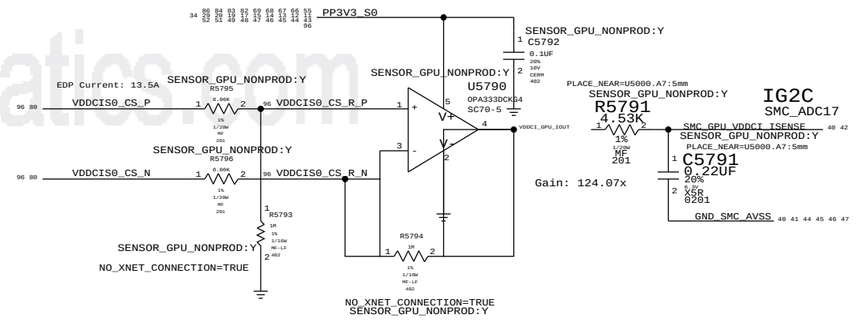
GPU FB Voltage Sense



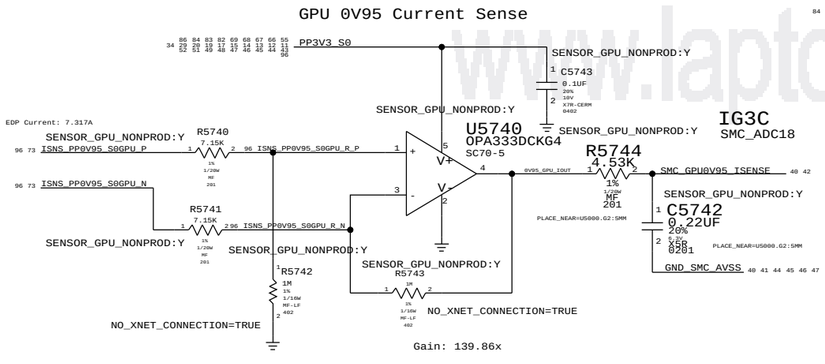
GPU VCORE Current Sense



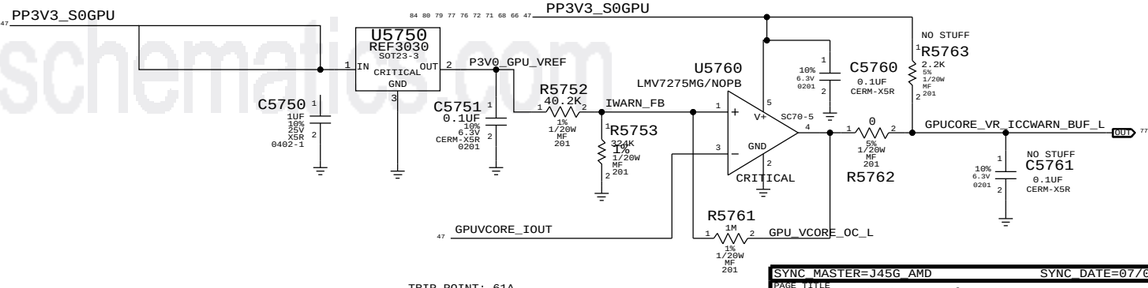
VDDCI Current Sense



GPU 0V95 Current Sense

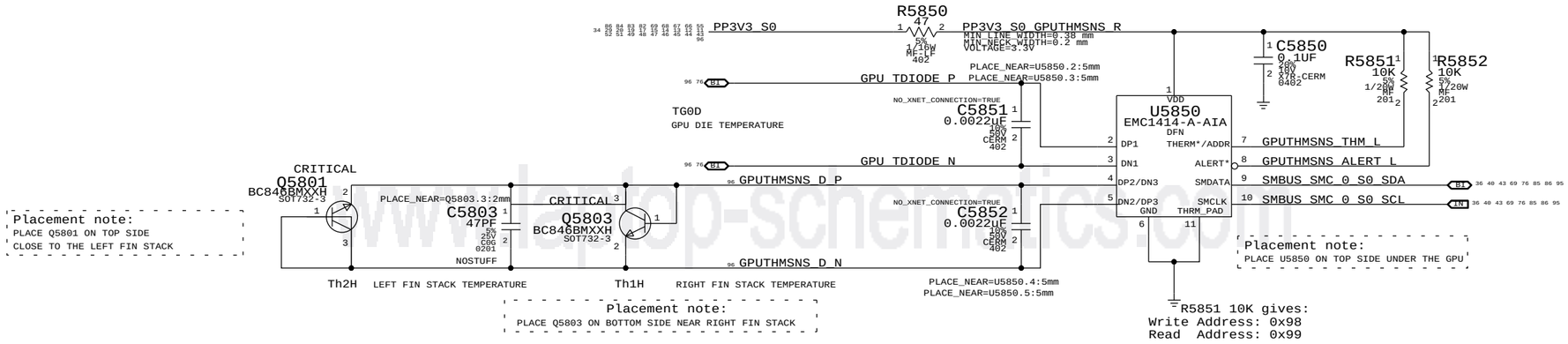


GPU VR OCP

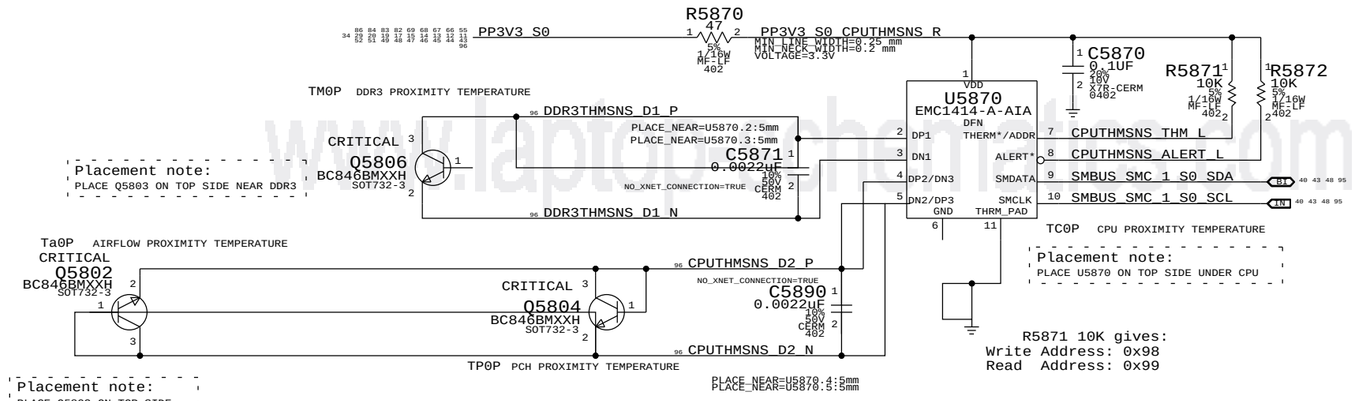


SYNC_MASTER=J45G_AMD	SYNC_DATE=07/01/2014
PAGE TITLE	GPU V/I Sensors
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 57 OF 119
	SHEET 47 OF 97

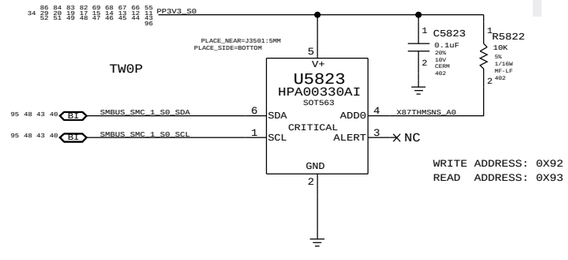
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK



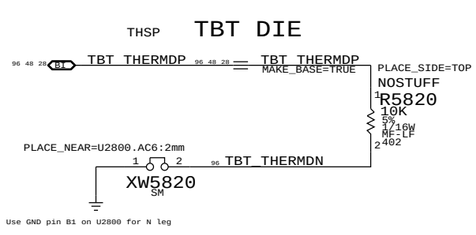
DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



X87 PROXIMITY



TBT DIE



SYNC_MASTER=CHANG J45 SYNC_DATE=11/26/2012

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

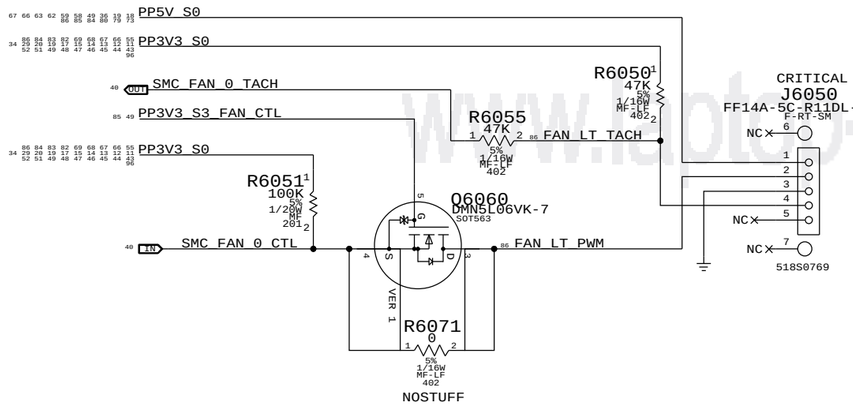
REVISION: <E4LABEL>

BRANCH: <BRANCH>

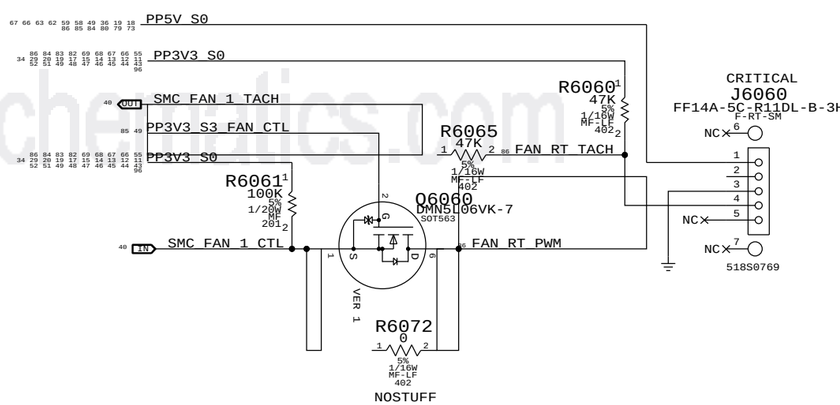
PAGE: 58 OF 119

SHEET: 48 OF 97

Left Fan



Right Fan



SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

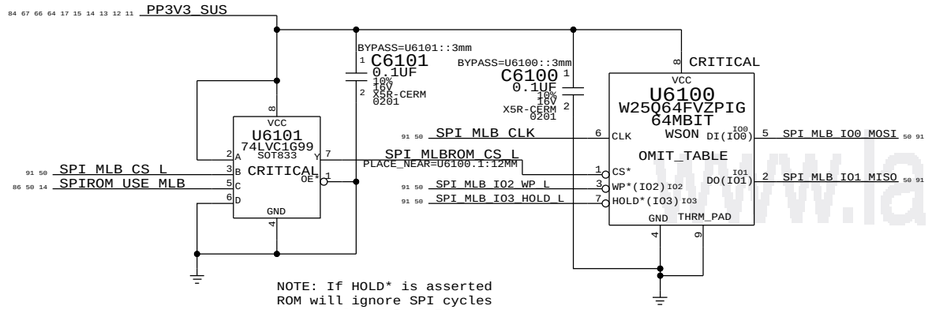
BRANCH: <BRANCH>

PAGE: 60 OF 119

SHEET: 49 OF 97

SPI ROM

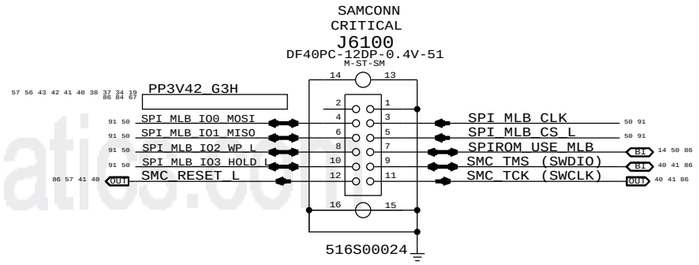
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

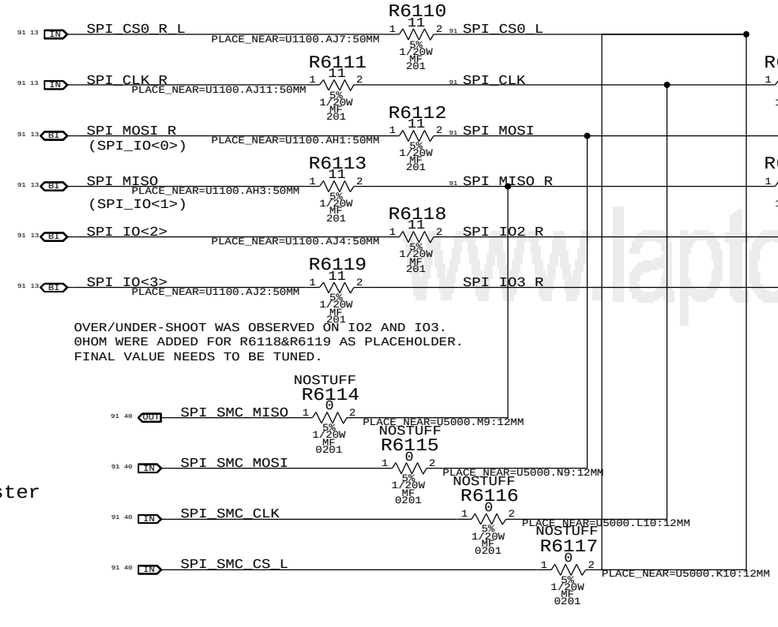
SPI+SWD SAM Connector

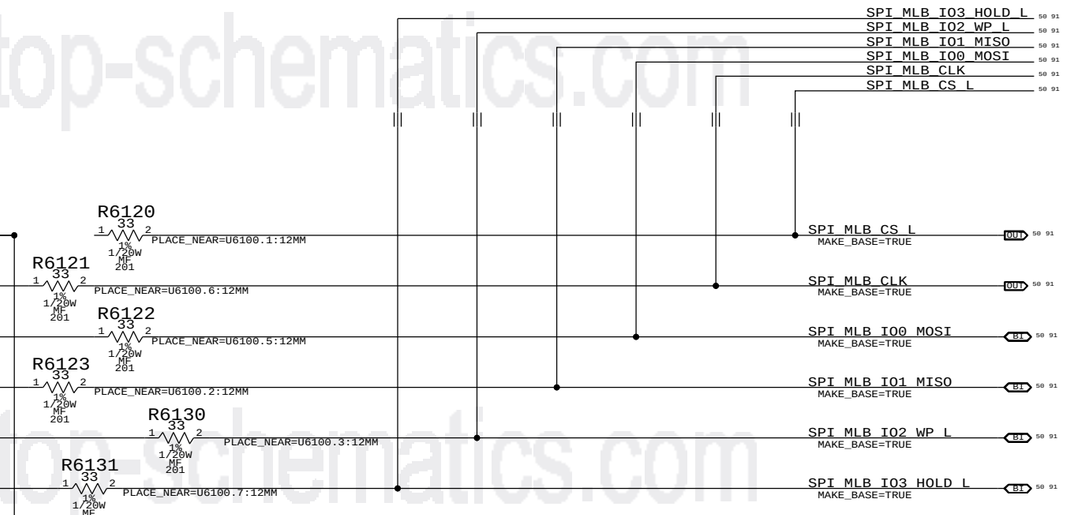


SPI Bus Series Termination

PCH Master

SMC12 Master





Sam Card ROM Slave

SPI ROM Slave

SYNC_MASTER=CLEAN_X425 SYNC_DATE=08/15/2014

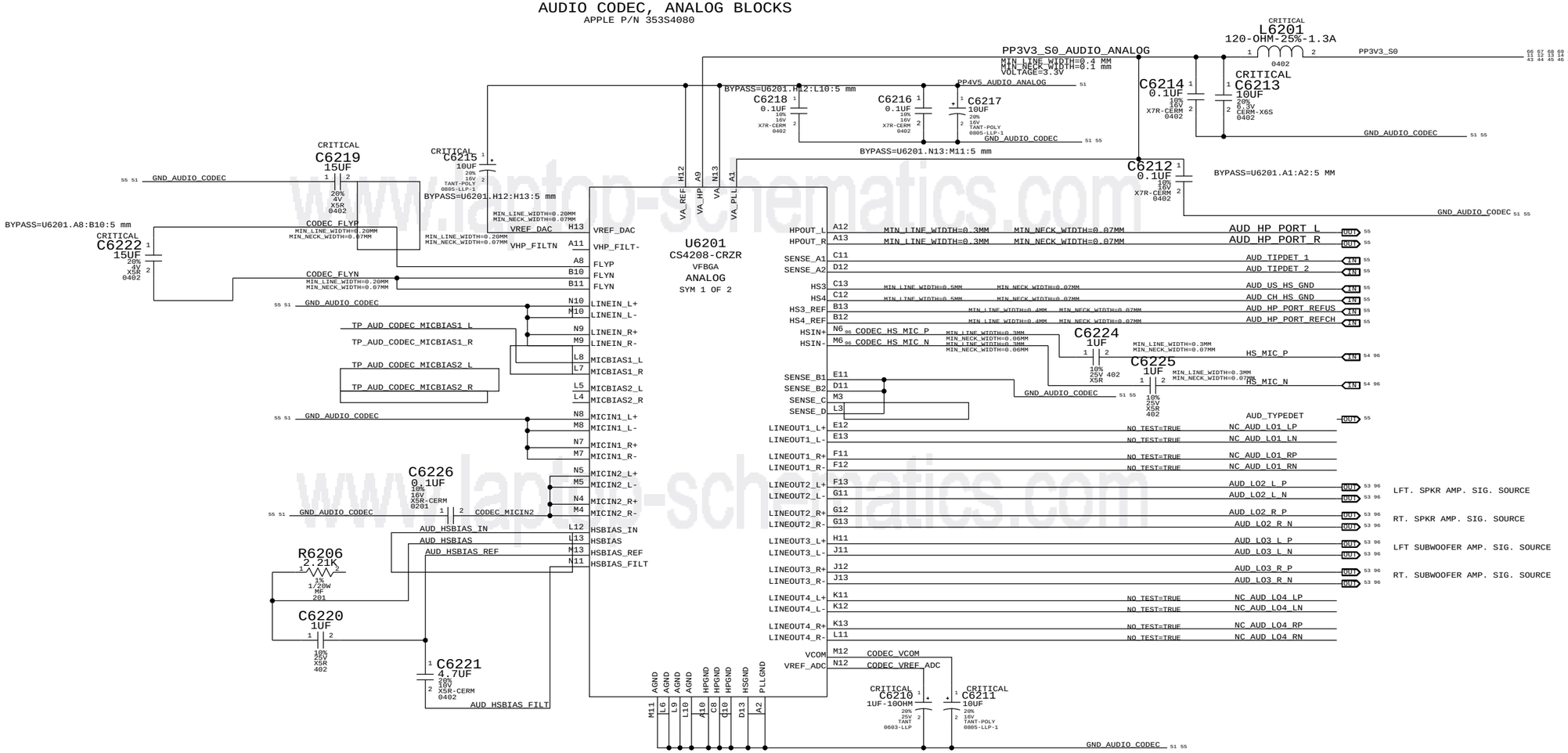
PAGE TITLE
SPI Debug Connector

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 61 OF 119
SHEET 50 OF 97

AUDIO CODEC, ANALOG BLOCKS

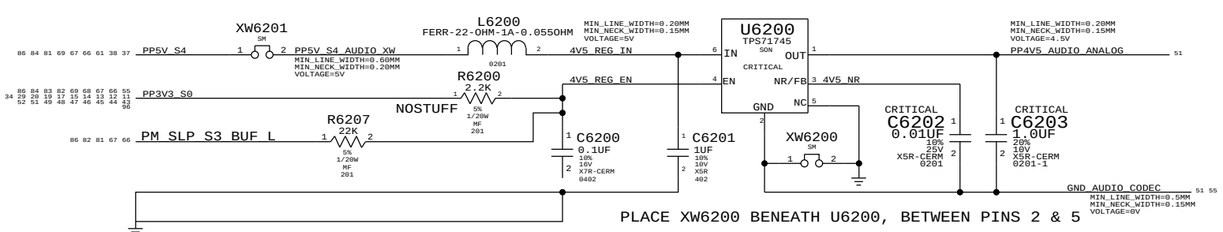
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456

PLACE XW6201 NEAR 5V SOURCE

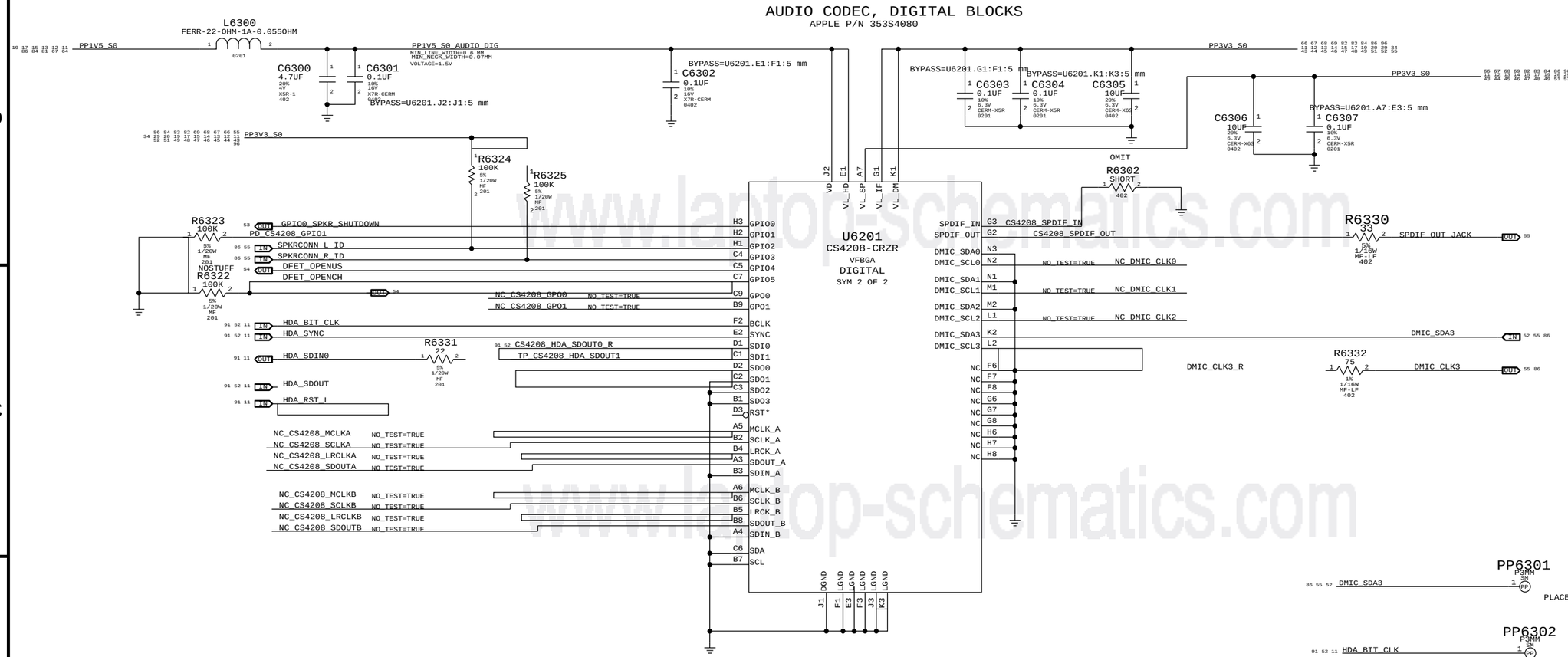


PLACE XW6200 BENEATH U6200, BETWEEN PINS 2 & 5

SYNC_MASTER=J0E_J45	SYNC_DATE=07/30/2013
PAGE TITLE	AUDIO:CODEC, ANALOG
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 62 OF 119
	SHEET 51 OF 97

AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

PAGE TITLE: AUDIO:CODEC, DIGITAL

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

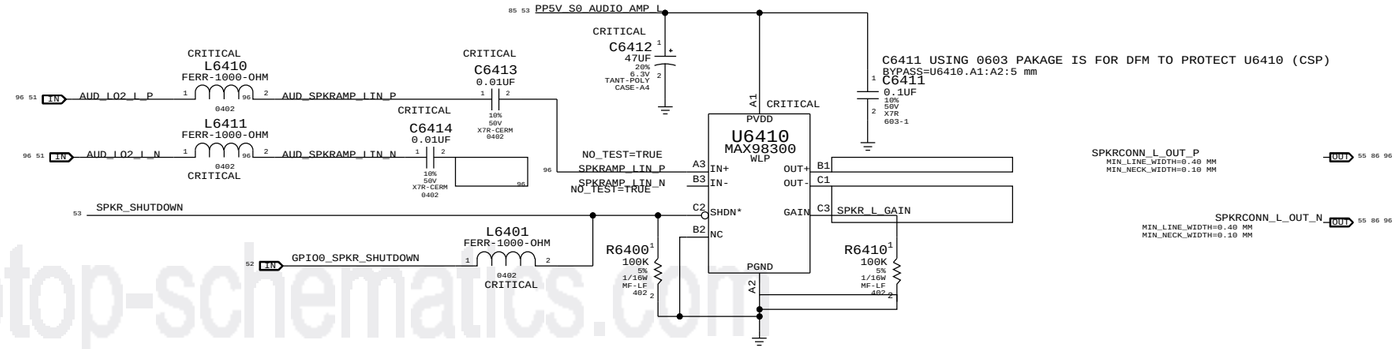
REVISION: <E4LABEL>

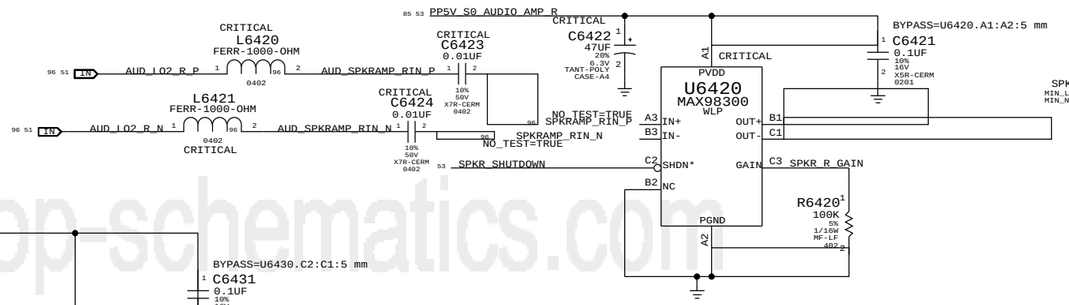
BRANCH: <BRANCH>

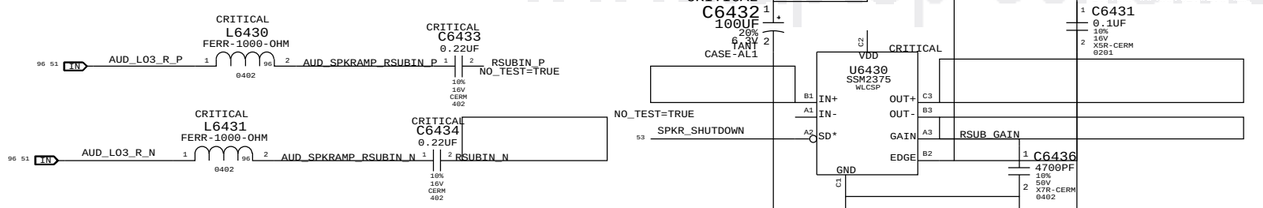
PAGE: 63 OF 119

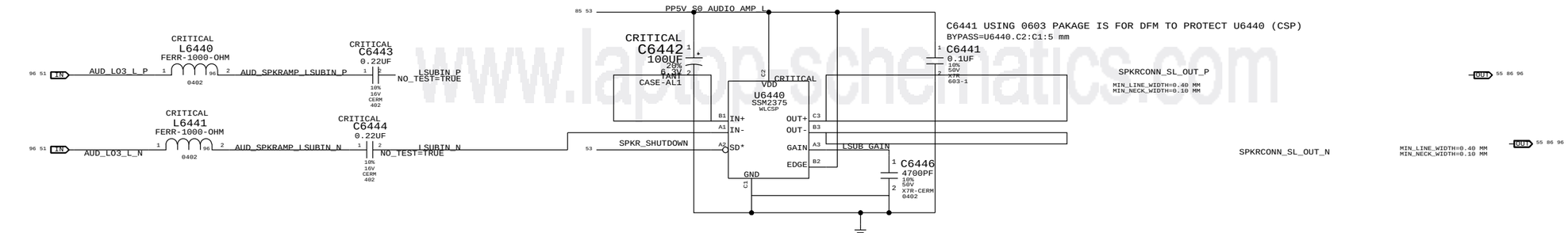
SHEET: 52 OF 97

4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ







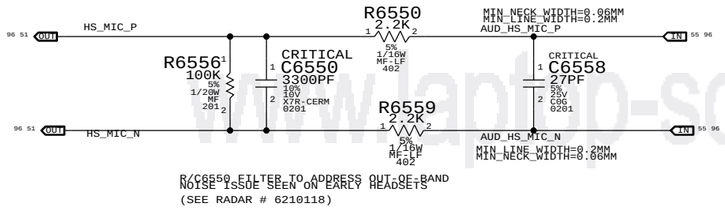


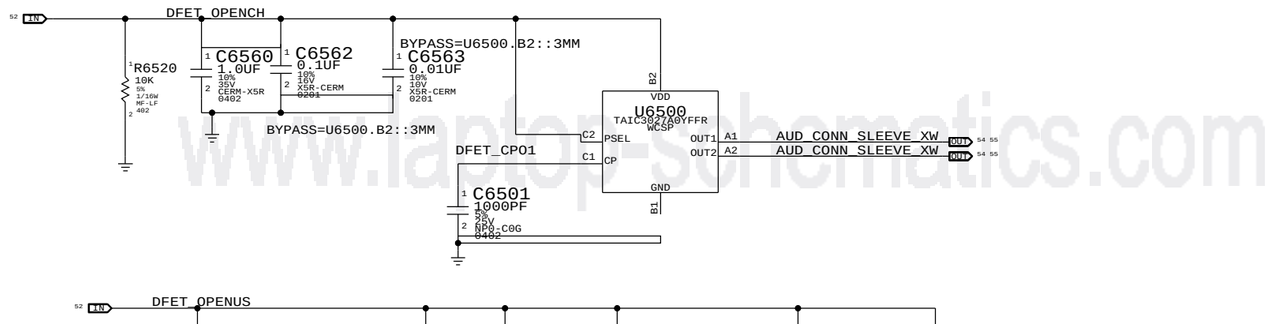
SYNC_MASTER=JOE_J45 SYNC_DATE=07/30/2013

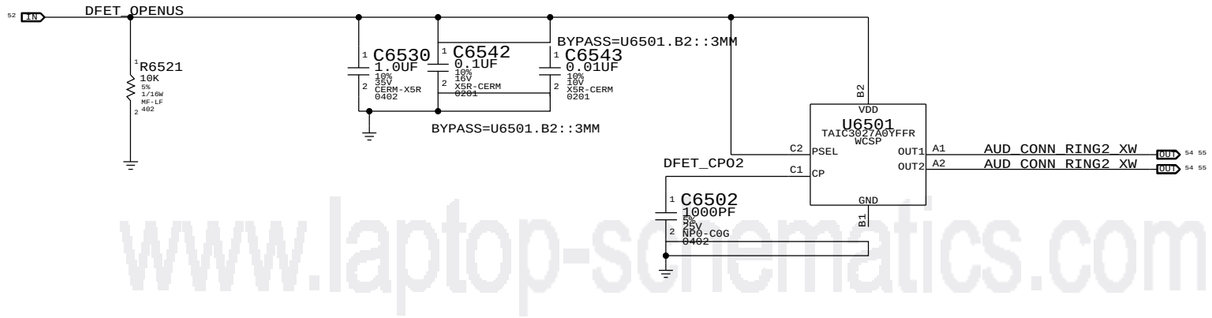
PAGE TITLE
AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 64 OF 119
SHEET 53 OF 97







SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 65 OF 119

SHEET: 54 OF 97

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

PP3V3_S0
DMIC_SDA3
DMIC_CLK3
OMIT
R6680
SHORT
402
DMIC_SDA2

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

J6602
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_L_OUT_P
SPKRCONN_L_OUT_N
SPKRCONN_L_ID
SPKRCONN_SL_OUT_P
SPKRCONN_SL_OUT_N

J6603
78171-6006
M-RT-SM
CRITICAL

SPKRCONN_R_OUT_P
SPKRCONN_R_OUT_N
SPKRCONN_R_ID
SPKRCONN_SR_OUT_P
SPKRCONN_SR_OUT_N

L6611 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFCH
AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.3:2.54mm
XW6600 SM
L6612 120-OHM-25%-1.3A 0402 CRITICAL
AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
AUD_CH_HS_GND
XW6601 SM
AUD_HS_MIC_P

L6613 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_REFUS
AUD_CONN_RING2
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.5:2.54mm
XW6602 SM
L6614 120-OHM-25%-1.3A 0402 CRITICAL
AUD_CONN_RING2_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
AUD_US_HS_GND
XW6603 SM
AUD_HS_MIC_N

L6604 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_L
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
R6602 2.2K 5% 1/20W MF 201
L6608 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_2
AUD_CONN_TIPDET_2
GND_AUDIO_CODEC
R6603 2.2K 5% 1/20W MF 201
L6607 FERR-470-OHM 0201 CRITICAL
AUD_TIPDET_1
AUD_CONN_TIPDET_1
L6605 120-OHM-25%-1.3A 0402 CRITICAL
AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
L6606 FERR-470-OHM 0201 CRITICAL
AUD_TYPEDET
AUD_CONN_TYPEDET
SPDIF_OUT_JACK
PP3V3_S0

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

MIC
AUDIO GND
2RTN
DET2
DET1
1RTN
R.AUDIO
AUDIO GND
AUDIO
NC
VIN
VDD
GND
OPERATING VOLTAGE 3.3
POF
SHELL PINS

R6601 10K 5% 1/16W MF-LF 402
C6602 100PF 5% 25V C0G 0201
C6600 1UF 10% 10V X5R 402-1
C6601 0.1UF 10% 16V CERM-X5R 0201
DZ6601 ESDALC5-1BM2 SOD882 CRITICAL
DZ6607 ESDALC5-1BM2 SOD882 CRITICAL
C6603 100PF 5% 25V C0G 0201
C6604 100PF 5% 25V C0G 0201
DZ6602 ESDALC5-1BM2 SOD882 CRITICAL
C6605 100PF 5% 25V C0G 0201
DZ6603 ESDALC5-1BM2 SOD882 CRITICAL
C6606 100PF 5% 25V C0G 0201
DZ6605 ESDALC5-1BM2 SOD882 CRITICAL
DZ6606 ESDALC5-1BM2 SOD882 CRITICAL
C6607 100PF 5% 25V C0G 0201
C6608 100PF 5% 25V C0G 0201
DZ6604 ESDALC5-1BM2 SOD882 CRITICAL

SYNC_MASTER=CLEAN_X305 SYNC_DATE=06/24/2014

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 66 OF 119
SHEET 55 OF 97

MagSafe DC Power Jack

CRITICAL
J7000
WTB-PWR-M82
M-RT-SM
518S0508

86 PP20V_DCIN_FUSE
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=20V

CRITICAL
F7005
6AMP-32V-0.0095OHM
0603

PPDCIN_G3H
57 84 86

NOSTUFF
C7005
0.01UF
20%
50V
CERM
0603

TP_TDM_ONEWIRE_MPM

PP3V42_G3H
84 86 42 43 58 59 56 57 67

C7008
0.1UF
20%
10V
CERM
402
PLACEMENT_NOTE=PLACE NEAR U7100 and U7001

CRITICAL
U7001
TC7SZ08FEAPE
SOT665

SMC_BC_ACOK_VCC
SMC_BC_ACOK
IN 40 41 42 57

C7000
0.1UF
20%
10V
CERM
402

U7000
MAX9940
SC70-5
CRITICAL
VCC
EXT
INT
NC
GND

R7029
2.0K
5%
1/16W
MF-LF
402

86 ADAPTER_SENSE
SYS_ONEWIRE
BI 40

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

R7012
22.1K
1%
1/20W
MF
201

Input impedance of 22.1K meets sparkitecture requirements for D2 design only

Q7010
SI5419DU
POWERPAK

R7010
100K
5%
1/20W
MF
201

C7012
0.047UF
10%
25V
X7R
0402

R7011
10K
5%
1/20W
MF
201

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

DCIN_ISOL_GATE_R
DCIN_ISOL_GATE
84 57 44 PPDCIN_G3H_ISOL

D7010
CDZ6.8B
SM
6.8V Zener

R7020
47
1%
1/3W
MF
805

PP20V_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=20V

CRITICAL
D7005
BAT30CWFILM
SOT-323

R7005
10
5%
1/8W
MF-LF
805

86 84 65 63 57 47 44 30 PPBUS_G3H
PPBUS_G3H_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=20V

APN:353S3733
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

P3V42G3H_BOOST
DIDT=TRUE

C7094
0.22UF
10%
16V
CERM
402

CRITICAL
L7095
10UH-20%-0.85A-0.46OHM
2520

U7090
LT3470AEDFD
DFN
VIN
BOOST
SW
BIAS
SHDN*
NC
FB
THRM
GND
PAD
CRITICAL

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

PP3V42_G3H
39 54 37 38 40 41 42 43 50 56 57 67 84 86

Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)

NOTE: R7097 can be replaced by SHORT at PVT

R7097
0
5%
1/16W
MF-LF
402

P3V42G3H_SHDN_L

R7001
0
5%
1/20W
MF
0201

NOTE: MIRROR C7092 and C7096

NOSTUFF
C7090 4.7UF 10% 35V X5R-CERM 0603
C7091 4.7UF 10% 35V X5R-CERM 0603
C7092 4.7UF 10% 35V X5R-CERM 0603
C7093 4.7UF 10% 35V X5R-CERM 0603
C7096 4.7UF 10% 35V X5R-CERM 0603
C7097 4.7UF 10% 35V X5R-CERM 0603

NOTE: MIRROR C7093 and C7097

OMIT
C7001
NOSTUFF
NONE
NONE
NONE
402

NOSTUFF
R7002
49.9K
1%
1/20W
MF
201

C7099
10UF
20%
6.3V
CERM-X6S
0402

C7098
10UF
20%
6.3V
CERM-X6S
0402

P3V42G3H_BIAS
<Ra>
R7095
348K
1%
1/20W
MF
201

C7095
22PF
5%
50V
C0G
0201

P3V42G3H_FB
<Rb>
R7096
200K
1%
1/20W
MF
201

Vout = 1.25V * (1 + Ra / Rb)

BATTERY CONNECTOR

518-0376
CRITICAL
J7050
BAT-J5
F-ST-TH
VER 1

12 POS 1
13 POS 2
14 POS 3
15 POS 4
16 SCL 5
17 SDA 6
18 SYS_DETECT 7
19 NEG 8
20 NEG 9
21 NEG 10
22 NEG 11

NC
NC

86 57 PPVBAT_G3H_CONN
SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA
86 SYS_DETECT_L
40 43 57 86 95
40 43 57 86 95

C7050
0.1UF
10%
25V
X7R-CERM
0402

C7060
1UF
10%
16V
CER-X6S
0402

CRITICAL
D7050
RCLAMP2402B
SC-75

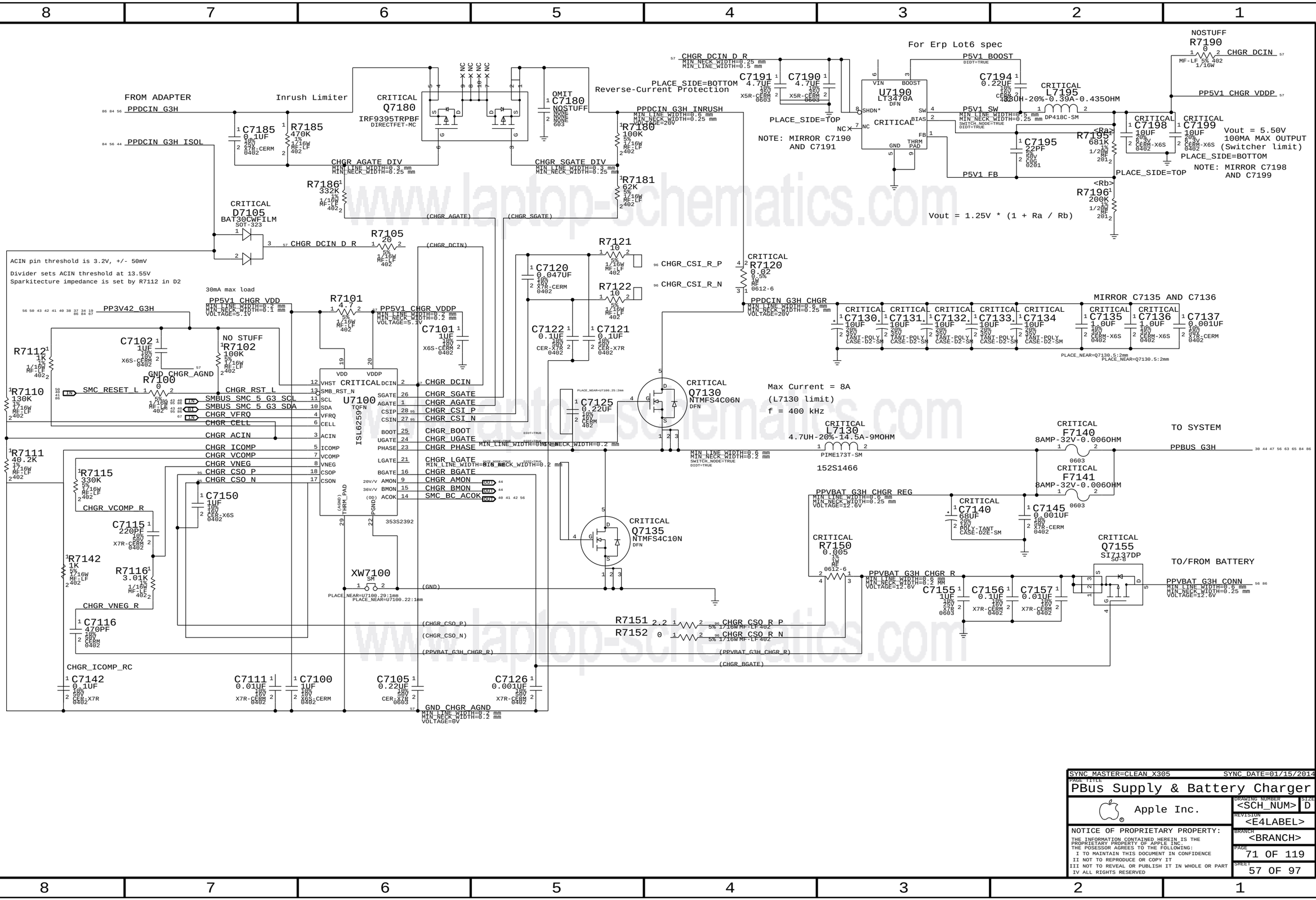
R7050
10K
5%
1/16W
MF-LF
402

SYNC_MASTER=CLEAN X425
SYNC_DATE=11/04/2014

PAGE TITLE
DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 70 OF 119
SHEET 56 OF 97

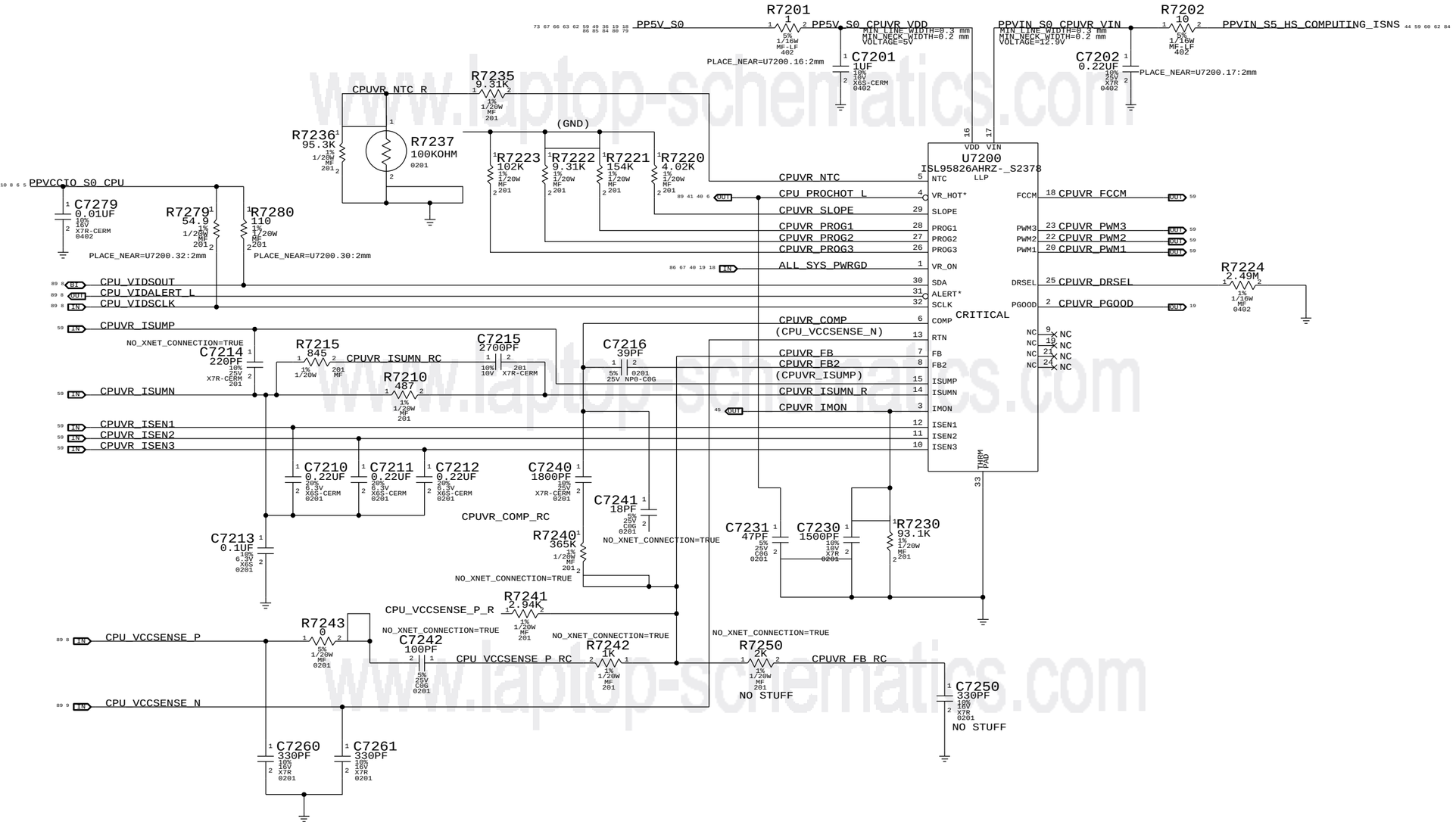


SYNC_MASTER=CLEAN_X305 SYNC_DATE=01/15/2014

PAGE TITLE
PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 71 OF 119
SHEET 57 OF 97



SYNC_MASTER=CLEAN_X425 SYNC_DATE=01/09/2015

PAGE TITLE: CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 72 OF 119

SHEET: 58 OF 97

FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM

PPVIN_S5_HS_COMPUTING_ISNS

PP5V_S0

PHASE 1

R7311 0 5% 1/10W MF-LF 402
CPUVR_BOOT1_RC — CPUVR_BOOT1
C7311 0.22UF 10% 16V CERM 402
CPUVR_PHASE1_K
C7310 1UF 10% 16V X6S-CERM 0402

U7310 FDMF6808N PQFN CRITICAL
353S3836

BOOT, DISB*, GH, GL, PHASE, PWM, ZCD_EN*, THWN*, VCIN, VDRV, VIN, VSWH, CGND, PGND

CPUVR_PWM1
CPUVR_FCCM

C7340 CRITICAL 12PF 5% 50V NP0-C0G 0201
C7341 CRITICAL 3.0PF +/-0.1PF 25V NP0-C0G 0201

C7313 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7314 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7315 NOSTUFF 10UF 20% 16V X6S-CERM 0603
C7316 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7317 1UF 10% 16V X6S-CERM 0402
C7318 THESE TWO CAPS ARE FOR EMC 0.001UF 10% 50V X7R-CERM 0402
C7319 0.001UF 10% 50V X7R-CERM 0402

R7310 CRITICAL 0.00075 1% 1W MF 0612-1

L7310 CRITICAL 0.36UH-20%-36A-0.001080HM
PIMS103T-SM 152S1538
CPUVR_PHASE1 — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH1 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.8V

R7312 NOSTUFF 2.2 5% 1/10W MF-LF 603
CPUVR_PH1_SNUB — DIDT=TRUE, NOSTUFF — C7312 0.001UF 10% 50V X7R-CERM 0402

CPUVR_ISNS1_P — CPUVR_ISNS1_N
R7314 3.9 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN
R7315 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R7316 10K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R7317 10K 1% 1/20W MF 201 — CPUVR_ISNS2_N — NO_XNET_CONNECTION=TRUE
R7318 10K 1% 1/20W MF 201 — CPUVR_ISNS3_N — NO_XNET_CONNECTION=TRUE
CPUVR_ISEN1
CPUVR_ISUMP

Additonal Input Bulk Caps

C7370 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7371 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7372 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7373 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7374 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7375 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7376 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7377 CRITICAL 15UF 20% 16V TANT SM
C7378 CRITICAL 15UF 20% 16V TANT SM
C7379 CRITICAL 15UF 20% 16V TANT SM
C7380 CRITICAL 15UF 20% 16V TANT SM

PP5V_S0

PHASE 2

R7321 0 5% 1/10W MF-LF 402
CPUVR_BOOT2_RC — CPUVR_BOOT2
C7321 0.22UF 10% 16V CERM 402
CPUVR_PHASE2_K
C7320 1UF 10% 16V X6S-CERM 0402

U7320 FDMF6808N PQFN CRITICAL
353S3836

CPUVR_PWM2
CPUVR_FCCM

C7323 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7324 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7325 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7326 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7327 1UF 10% 16V X6S-CERM 0402
C7328 THESE TWO CAPS ARE FOR EMC 0.001UF 10% 50V X7R-CERM 0402
C7329 0.001UF 10% 50V X7R-CERM 0402

R7320 CRITICAL 0.00075 1% 1W MF 0612-1

L7320 CRITICAL 0.36UH-20%-36A-0.001080HM
PIMS103T-SM 152S1538
CPUVR_PHASE2 — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH2 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.8V

R7322 NOSTUFF 2.2 5% 1/10W MF-LF 603
CPUVR_PH2_SNUB — DIDT=TRUE, NOSTUFF — C7322 0.001UF 10% 50V X7R-CERM 0402

CPUVR_ISNS2_P — CPUVR_ISNS2_N
R7324 3.9 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN
R7325 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R7326 10K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R7327 10K 1% 1/20W MF 201 — CPUVR_ISNS1_N — NO_XNET_CONNECTION=TRUE
R7328 10K 1% 1/20W MF 201 — CPUVR_ISNS3_N — NO_XNET_CONNECTION=TRUE
CPUVR_ISEN2
CPUVR_ISUMP

PP5V_S0

PHASE 3

R7331 0 5% 1/10W MF-LF 402
CPUVR_BOOT3_RC — CPUVR_BOOT3
C7331 0.22UF 10% 16V CERM 402
CPUVR_PHASE3_K
C7330 1UF 10% 16V X6S-CERM 0402

U7330 FDMF6808N PQFN CRITICAL
353S3836

CPUVR_PWM3
CPUVR_FCCM

C7333 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7334 CRITICAL 68UF 20% 16V POLY-TANT CASE-D2E-SM
C7335 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7336 NOSTUFF CRITICAL 10UF 20% 16V X6S-CERM 0603
C7337 1UF 10% 16V X6S-CERM 0402
C7338 THESE TWO CAPS ARE FOR EMC 0.001UF 10% 50V X7R-CERM 0402
C7339 0.001UF 10% 50V X7R-CERM 0402

R7330 CRITICAL 0.00075 1% 1W MF 0612-1

L7330 CRITICAL 0.36UH-20%-36A-0.001080HM
PIMS103T-SM 152S1538
CPUVR_PHASE3 — MIN_LINE_WIDTH=1.5 MM, MIN_NECK_WIDTH=0.2 MM, DIDT=TRUE, SWITCH_NODE=TRUE
PPVCC_S0_CPU_PH3 — MIN_LINE_WIDTH=0.6 MM, MIN_NECK_WIDTH=0.25 MM, VOLTAGE=1.8V

R7332 NOSTUFF 2.2 5% 1/10W MF-LF 603
CPUVR_PH3_SNUB — DIDT=TRUE, NOSTUFF — C7332 0.001UF 10% 50V X7R-CERM 0402

CPUVR_ISNS3_P — CPUVR_ISNS3_N
R7334 3.9 1% 1/20W MF 201
NO_XNET_CONNECTION=TRUE
CPUVR_ISUMN
R7335 1K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R7336 10K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R7337 10K 1% 1/20W MF 201 — CPUVR_ISNS1_N — NO_XNET_CONNECTION=TRUE
R7338 10K 1% 1/20W MF 201 — CPUVR_ISNS2_N — NO_XNET_CONNECTION=TRUE
CPUVR_ISEN3
CPUVR_ISUMP

PPVCC_S0_CPU

Vout = 1.85V max
95A max output
f = 450 kHz

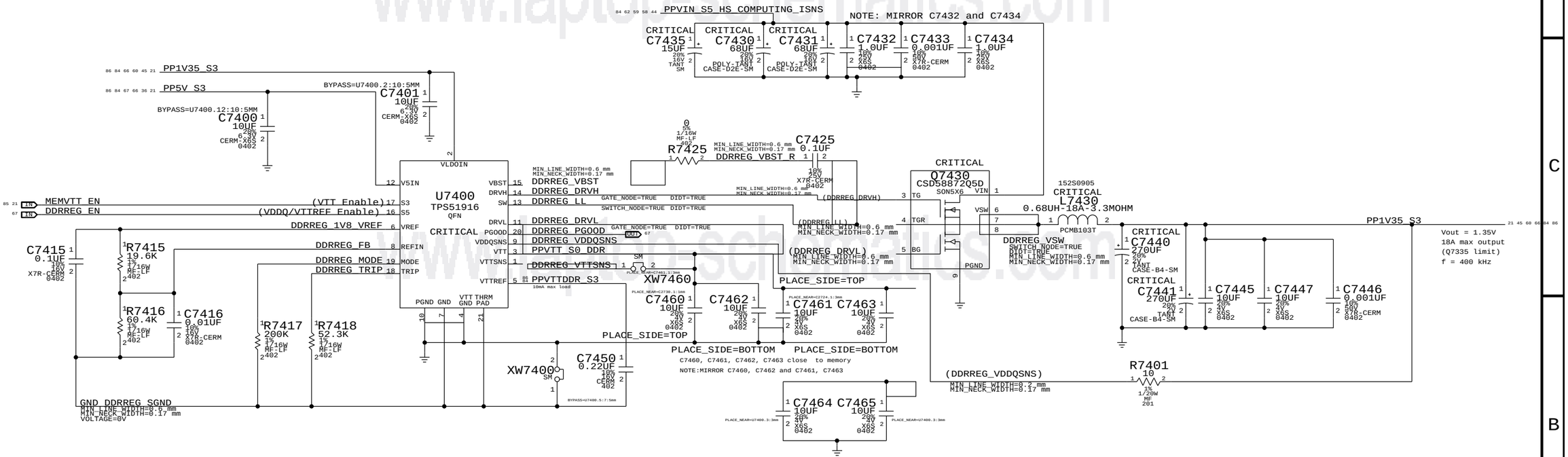
SYNC_MASTER=CLEAN_X425 SYNC_DATE=01/09/2015

PAGE TITLE: CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 73 OF 119
SHEET: 59 OF 97

DDR3L (1V35 S3) REGULATOR



SYNC_MASTER=CLEAN X305 SYNC_DATE=01/15/2014

PAGE TITLE: 1.35V DDR3L SUPPLY

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 74 OF 119

SHEET: 60 OF 97

NOTE: MIRROR C7540 and C7541

NOTE: MIRROR C7581 and C7586

PPVIN_S5_HS_OTHER5V_ISNS

PPVIN_S5_HS_OTHER3V3_ISNS

PP5V_S4

PP5V_S5
VOUT = 5V
100MA MAX OUTPUT

PP3V3_S5
VOUT = 3.3V
10A MAX OUTPUT
F = 400 KHZ

VOUT = 5.0V
11A MAX OUTPUT
F = 400 KHZ

P5V_S4_VBST

P3V3S5_VBST

P5V_S4_VSW

P5V_S4_SNUBR

P5V_S4_CSP1_R

P5V_S4_VFB1_R

P5V_S4_COMP1_R

P3V3S5_CSP2_R

P3V3S5_COMP2_R

P3V3S5_VFB2_R

P3V3S5_SNUBR

P5V_S4_VBST_R

P5V_S4_DRVH

P5V_S4_LL

P5V_S4_DRVL

P5V_S4_CSP1

P5V_S4_CSN1

P5V_S4_VFB1

P5V_S4_COMP1

P5V_S4_EN

P5V_S4_PGOOD

P3V3S5_VBST_R

P3V3S5_DRVH

P3V3S5_LL

P3V3S5_DRVL

P3V3S5_CSP2

P3V3S5_CSN2

P3V3S5_RF

P3V3S5_VFB2

P3V3S5_COMP2

P3V3S5_EN

S5_PWRGD

SMC_PM_G2_EN

P5VP3V3_VREG3

P5VP3V3_VREF2

P5VP3V3_SKIPSEL

SKIP_5V3V3:INAUDIBLE

SKIP_5V3V3:AUDIBLE

GND_5V3V3_AGND
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V

GND

THRM_PAD

CRITICAL
U7501
TPS51980
QFN

CRITICAL
Q7520
CSD58872Q5D
VIN SON5X6

CRITICAL
Q7560
NTMFD4951NF
DFN8

152S0754
CRITICAL
L7560
1.0UH-22A
PCMC063T-SM

CRITICAL
L7520
2.2UH-20%-13A-9MOHM
PCMB103T-SM

NO STUFF
CRITICAL
C7555
150UF-0.035OHM
20%
6.3V
POLY-TANT
CASE-B2-SM

NO STUFF
R7599
10
5%
1/10W
MF-LF
603

NO STUFF
C7599
0.0033UF
10%
50V
X7R-CERM
0402

NO STUFF
R7598
10
5%
1/10W
MF-LF
603

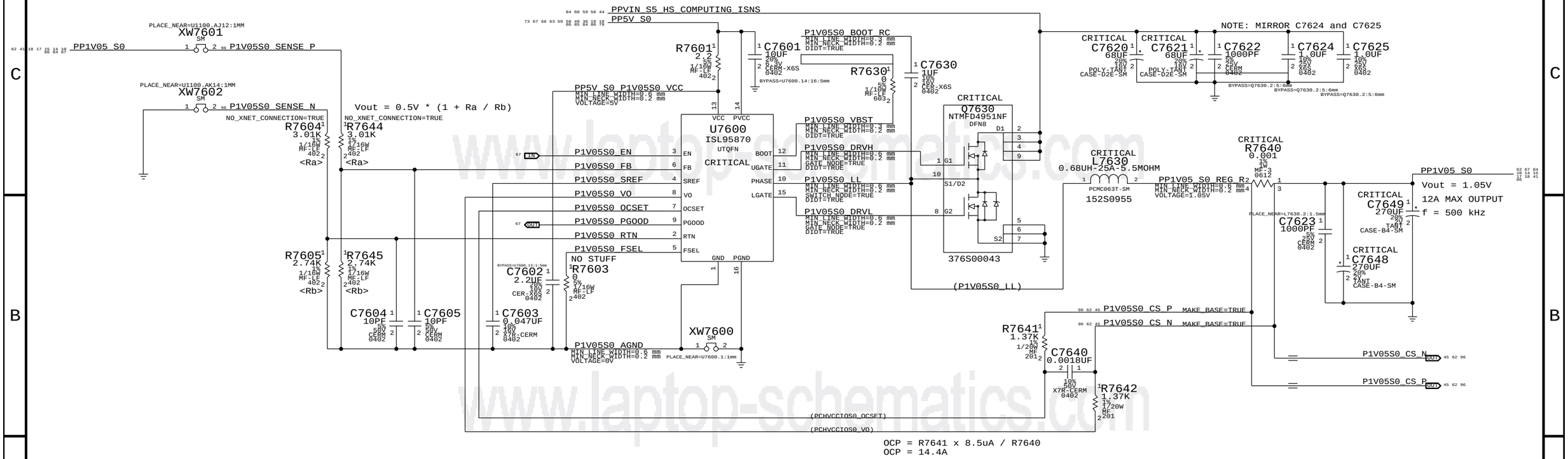
NO STUFF
C7598
0.001UF
10%
50V
X7R-CERM
0402

NOTE: Change R7522 to XW7522 at PVT

NOTE: Change R7562 to XW7562 at PVT

SYNC_MASTER=CLEAN_X425	SYNC_DATE=11/04/2014
PAGE TITLE	5V / 3.3V Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 75 OF 119
	SHEET 61 OF 97

1V05 S0 REGULATOR



SYNC_MASTER=CLEAN_X305_PEG	SYNC_DATE=02/18/2014
PAGE TITLE	1V05V POWER SUPPLY
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 76 OF 119
	SHEET 62 OF 97

Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

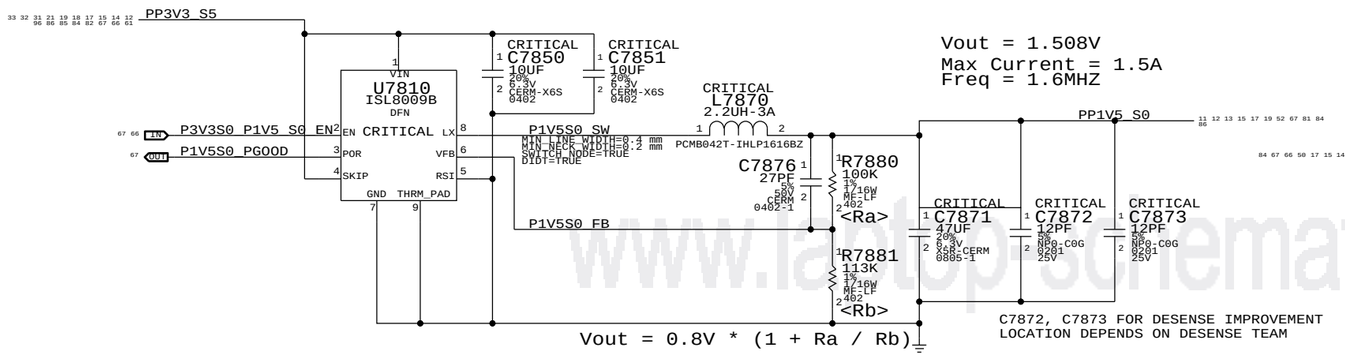
BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7723,R7724		BKLT:PROD

PPBUS_G3H
CRITICAL F7700 3AMP-32V 0603
PPBUS_S0_LCDBKLT_FUSED MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=12.6V
CRITICAL R7700 0.025 1% 1W MF 0612-1
PPBUS_SW_LCDBKLT_PWR MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=12.6V
CRITICAL Q7706 FDC638APZ_SBMS001 SSOT6-HF
PPBUS_SW_BKL MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=12.6V
C7710 4.7UF 10% 25V X5R-CERM 0603
C7711 4.7UF 10% 25V X5R-CERM 0603
C7712 0.1UF 10% 25V X5R 402
152S1527
CRITICAL L7710 22UH-20%-2.4A-0.105OHM DEM8030C-SM
PPBUS_S0_LCDBKLT_PWR_SW MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=45V SWITCH_NODE=TRUE DIDT=TRUE
PLACE_NEAR=L7710.2:3MM
CRITICAL D7701 POWERDI-123 DFLS2100
PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE
CRITICAL C7715 2.2UF 20% 100V X7R 1210-1
CRITICAL C7716 2.2UF 20% 100V X7R 1210-1
CRITICAL C7718 2.2UF 20% 100V X7R 1210-1
CRITICAL C7719 2.2UF 20% 100V X7R 1210-1
C7717 1000PF 10% 100V X7R-CERM 0603
PPVOUT_S0_LCDBKLT MIN_LINE_WIDTH=0.8 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=55V
PLACE_NEAR=D7701.K:3MM PLACE_NEAR=D7701.K:3MM PLACE_NEAR=D7701.K:3MM PLACE_NEAR=D7701.K:5MM PLACE_NEAR=D7701.K:5MM
C7730 12PF 2% 100V CERM 0402
C7731 12PF 2% 100V CERM 0402
NOSTUFF C7701 0.001UF 10% 50V X7R 402
C7700 1000PF 10% 16V X7R-1 0201
R7701 80.6K 1% 1/20W MF 201
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
LCDBKLT_EN_L
PP5V_S0
R7743 0 5% 1/16W MF-LF 402
R7744 0 5% 1/16W MF-LF 402
VOLTAGE=5V MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM
PP5V_S0_BKLT_VDDA
PP5V_S0_BKLT_VDDD
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=5V
R7702 63.4K 1% 1/16W MF-LF 402
C7740 1UF 10% 16V X5R 402-2
C7741 1UF 10% 16V X5R 402-2
GND_BKLT_SGND
R7740 1M 5% 1/20W MF 201
U7701 QFN LP8548B1SQ_-03
VDDD VDDA
BKLT_SD
(PPBUS_S0_BKLT_PWR_R)
(PPBUS_S0_BKLT_PWR_F)
BKLT_SENSE_OUT
SD VSENSE_N VSENSE_P SENSE_OUT ISET_KEYB KEYB1 KEYB2 SW2 FB2 SW SW FB GD
BKL_SW MIN_LINE_WIDTH=2 mm MIN_NECK_WIDTH=0.25 mm DIDT=TRUE
BKL_FB
BKLT_ISET_KEYB
BKLT_KEYB1
BKLT_KEYB2
R7742 0 5% 1/20W MF 0201
LCD_BKLT_EN
BKLT_EN_R
NO STUFF C7742 33PF 5% 25V NPO-C0G 0201
GND_BKLT_SGND
R7747 0 5% 1/20W MF 0201
SMC_SYS_KBDLED
BKLT_PWM_KEYB
NO STUFF C7747 33PF 5% 25V NPO-C0G 0201
GND_BKLT_SGND
CRITICAL 353S4159
GND_SW GND_SW GND_SW2 GNDD GNDA THERM PAD
R7741 31.6K 1% 1/20W MF 201
PPVOUT_BKLT_FB2 MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=48V
XW7700 SM
KBDBKLT_SW MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE
GND_BKLT_SGND MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0V
BKLT:ENG R7723 10.2 1% 1/16W MF 402
KBDBKLT_RETURN1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
BKLT:ENG R7724 10.2 1% 1/16W MF 402
KBDBKLT_RETURN2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
PP5V_S0
R7760 1.8K 5% 1/20W MF 201
R7761 1.8K 5% 1/20W MF 201
I2C_BKLT_SCL
I2C_BKLT_SDA
R7758 0 5% 1/20W MF 0201 BKLT_SCL
R7757 0 5% 1/20W MF 0201 BKLT_SDA
PP5V_S0
R7783 0 5% 1/16W MF-LF 402
152S1701 CRITICAL L7720 10UH-20%-1.4A-0.17OHM PST041H-CDH46D14-SM
PP5V_S0_KBDLED_R
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=5V
C7720 2.2UF 10% 25V X5R-CERM 603
C7721 2.2UF 10% 25V X5R-CERM 603
C7722 0.1UF 10% 16V X5R-CERM 0201
C7720, C7721 SHOULD BE PLACED MIRRORED
371S0572 CRITICAL D7720 SOD-123 RB160M-60G
XW7720 SM
PLACE_NEAR=D7720.K:2MM
C7726 1.0UF 10% 50V X7R 0805
C7727 1.0UF 10% 50V X7R 0805
C7728 12PF 2% 100V CERM 0402
C7729 12PF 2% 100V CERM 0402
PPVOUT_S0_KBDBKLT MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=48V
C7723 1.0UF 10% 50V X7R 0805
C7724 1.0UF 10% 50V X7R 0805
C7725 0.001UF 10% 100V X7R-CERM 0402
C7723, C7724 SHOULD BE PLACED MIRRORED
CRITICAL Q7701 SI7812DN PWRPK-1212-8
BKL_FET_CNTL_R MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE
R7703 0 5% 1/16W MF-LF 402
BKL_FET_CNTL MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE
R7708 18.2K 1% 1/16W MF-LF 402
R7709 150K 1% 1/16W MF-LF 402
R7780 0 5% 1/20W MF 0201 LCD_BKLT_PWM LCD_BKLT_PWM_R

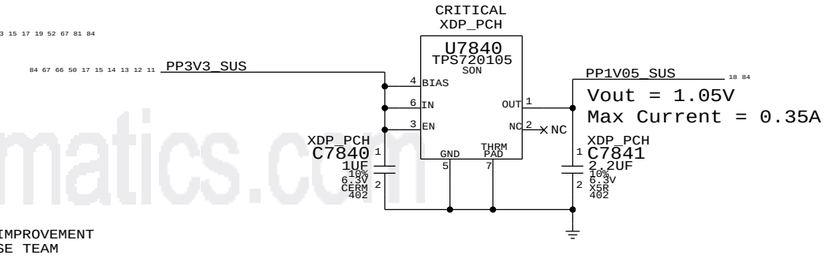
SYNC_MASTER=CLEAN_X425 SYNC_DATE=10/30/2014
PAGE TITLE: LCD/KBD Backlight Driver
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 77 OF 119
SHEET: 63 OF 97

1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC_MASTER=CLEAN X305 SYNC_DATE=01/15/2014

PAGE TITLE: Misc Power Supplies

Apple Inc.

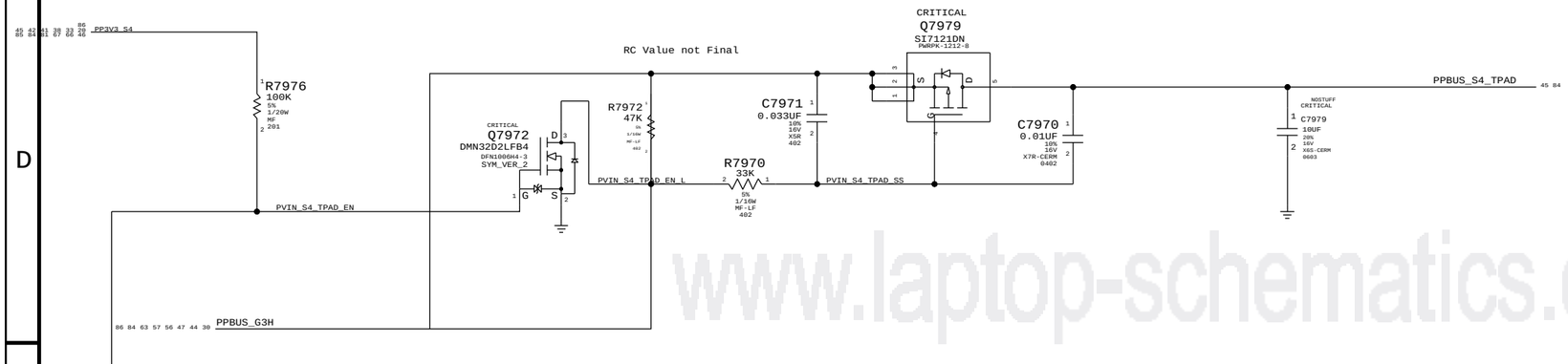
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 78 OF 119

SHEET: 64 OF 97



PBUS ONLY CONTROL INPUTS

SYSTEM STATE	SMC_ACTUATOR_DISABLE_L	TPAD_ACTUATOR_THRMTRIP_L	T101 POWER
G3H, S5	X	X	0 V
S4, S3, S0	Hi-Z	Hi-Z	PBUS
S4, S3, S0	0 V	X	0 V
S4, S3, S0	X	0 V	0 V

SYNC_MASTER=CLEAN_MAXWELL SYNC_DATE=07/02/2014

PAGE TITLE

X249 POWER SUPPLY

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D

REVISION <E4LABEL>

BRANCH <BRANCH>

PAGE 79 OF 119

SHEET 65 OF 97

3.3V S4 FET

376S0945
CRITICAL
Q8000
SIA413DJ
SC70-6L

EDP is per J45 Power Budget rev5

PP3V3_S5 → R8002 220K → P3V3S4_EN_L → C8009 0.033UF (10% 16V X5R 402) → R8000 47K (5% 1/16W MF-LF 402) → P3V3S3_S4 → C8000 0.01UF (10% 16V X7R-CERM 0402) → PP3V3_S4

Q8002
DMN5L06VK-7
SOT563
VER 1

S4_PWR_EN

3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET

CRITICAL
Q8010
SIA413DJ
SC70-6L

PP3V3_S5 → R8012 47K (5% 1/16W MF-LF 402) → P3V3S3_EN_L → C8011 0.033UF (10% 16V X5R 402) → R8010 39K (5% 1/16W MF-LF 402) → P3V3S3_SS → C8010 0.01UF (10% 16V X7R-CERM 0402) → PP3V3_S3

CRITICAL
C8012 12PF (5% NP0-C0G 0201 25V) FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM

Q8012
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

P3V3S3_EN

SSD_PWR_EN:GPIO → R8073 0 (0201 1/20W 5% MF) → SSD_PWR_EN_L → R8074 0 (0201 1/20W 5% MF) → PM_SLP_S3_BUF_L

3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

5V S3 FET

CRITICAL
Q8050
SIA427DJ
SC70-6L

PP5V_S4 → R8052 200K (5% 1/16W MF-LF 402) → P5VS3_EN_L → C8051 0.033UF (10% 16V X5R 402) → R8050 5.1K (5% 1/16W MF-LF 402) → P5VS3_SS → C8050 0.01UF (10% 16V X7R-CERM 0402) → PP5V_S3

Q8052
DMN5L06VK-7
SOT563
VER 1

P5VS3_EN

5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET

PP5V_S5 → C8001 0.1UF (20% 16V CERM 402) → U8001 SLG5AP1438V TDFN CRITICAL (VDD, CAP, ON, GND, D, S)

P1V35CPU_SLEW_CTL
CPUVDDQ_EN
C8002 0.018UF (10% 16V X7R 402)

Slew rate :
0.8V/ms = 19.75nF

PP1V35_S3

1.35V S3/S0 FET	
Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

SENSOR_NONPROD_R
R8005 0.002 (1% 1W CYN 0612)

PP1V35_S3RS0_FET → PP1V35_S3RS0_CPUDDR
ISNS_CPUDDR_N
ISNS_CPUDDR_P

3.3V SUS FET

CRITICAL
Q8020
SIA413DJ
SC70-6L

PP3V3_S5 → R8022 100K (5% 1/16W MF-LF 402) → P3V3SUS_EN → C8021 0.033UF (10% 16V X5R 402) → R8020 12K (5% 1/16W MF-LF 402) → P3V3SUS_SS → C8020 0.01UF (10% 16V X7R-CERM 0402) → PP3V3_SUS

Q8002
DMN5L06VK-7
SOT563
VER 1

PM_SLP_SUS_L

3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

3.3V S0 SSD FET

PLACE_NEAR=R5549.2:6mm

CRITICAL
Q8070
SI7615DN
PWRPK-1212-8

PP3V3_S5 → R8072 47K (5% 1/16W MF-LF 402) → P3V3_SSD_EN_L → C8071 0.033UF (10% 16V X5R 402) → R8070 33K (5% 1/16W MF-LF 402) → P3V3_SSD_SS → C8070 0.01UF (10% 16V X7R-CERM 0402) → PP3V3_S0SW_SSD_R

Q8072
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

SSD_PWR_FET_EN

3.3V S0 SSD FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET

CRITICAL
Q8060
SI7615DN
PWRPK-1212-8

PP5V_S4 → R8062 270K (5% 1/16W MF-LF 402) → P5V0S0_EN_L → C8061 0.12UF (10% 10.0V X5R 402) → R8060 6.2K (5% 1/16W MF-LF 402) → P5V0S0_SS → C8060 0.47UF (10% 10V X5R 0402) → PP5V_S0

Q8052
DMN5L06VK-7
SOT563
VER 1

P5VS0_EN

5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

GPU_3.3V S0 Switch

Max Current = 0.11A
APN 353S3979

U8090
TPS22904
CSP
CRITICAL
VIN, VOUT, ON, GND, A1, A2, B1, B2

PP3V3_S5 → C8090 1UF (10% 6.3V X5R 402)
P3V3_S0GPU_EN
PP3V3_S0GPU
NOSTUFF C8091 0.1UF (10% 16V X5R 402)

U8090	
Part	TPS22904
Type	Load Switch
R(on) @ 3.6V	66 mOhm Typ 90 mOhm Max
Current	0.5A Max

3.3V S0 Switch

APN 353S2741

U8030
TPS22924
CSP
CRITICAL
VIN, VOUT, ON, GND, A1, A2, B1, B2, C1, C2

PP3V3_S5 → C8030 1UF (10% 10V X5R 603)
P3V3S0_P1V5_S0_EN
PP3V3_S0
Max Current = 2A

C8030 USING 0603 PAKAGE IS FOR DFM TO PROTECT U8030 (CSP)

U8030	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=J45_IG
SYNC_DATE=07/01/2014
PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 80 OF 119
SHEET: 66 OF 97

Power State Debug LEDs
(For development only)

PP3V3_S5 → R8194 0 (5% 1/16W MF-LF 402) — PP3V3_S5_DBGLED: PLACE_SIDE=BOTTOM, MIN_NECK_WIDTH=0.2 MM, MIN_LINE_WIDTH=0.25 MM, VOLTAGE=3.3V

DBGLED_S5	DBGLED_S4	DBGLED_S3	DBGLED_S0
R8190 20K (5% 1/20W MF 201)	R8191 20K	R8192 20K	R8193 20K
D8190	D8191	D8192	D8193
GREEN-56MCD-2MA-2.65V LTQH9G-SM, PLACE_SIDE=BOTTOM, SILK_PART=S5_ON	GREEN-56MCD-2MA-2.65V LTQH9G-SM, PLACE_SIDE=BOTTOM, SILK_PART=S4_ON	GREEN-56MCD-2MA-2.65V LTQH9G-SM, PLACE_SIDE=BOTTOM, SILK_PART=S3_ON	GREEN-56MCD-2MA-2.65V LTQH9G-SM, PLACE_SIDE=BOTTOM, SILK_PART=S0_ON
DBGLED_S5_D	DBGLED_S4_D	DBGLED_S3_D	DBGLED_S0_D
Q8190 DMN5L06VK-7 SOT563	Q8190 DMN5L06VK-7 SOT563	Q8191 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2	

S4_PWR_EN; PM_SLP_S4_L; PM_SLP_S3_BUF_L; VER 1

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

S4 Power Enable

PP3V3_S5 → C8170 0.1uF (20% 10V CERM 402) → PM_SLP_S5_L (PM_SLP_S5_L:100K pull down on PCH page)

SMC_S4_WAKESRC_EN → U8170 74LVC1G32 SOT891 (MAKE_BASE=TRUE) → S4_PWR_EN

S4_PWR_EN → D8174 SOD-523 BAT54XV2T1 → R8174 43K (5% 1/16W MF-LF 402) → P5VS4_EN (MAKE_BASE=TRUE)

P5VS4_EN_D → R8175 240 (5% 1/16W MF-LF 402); C8174 2.2UF (10% 6.3V X5R 402)

S4_PWR_EN (OUT) ×3

S3 ENABLE

PM_SLP_S4_L (IN) — PM_SLP_S4_L:100K pull down in PCH page

R8111 5.1K	R8112 0	R8113 0	R8114 3.3K (1/20W MF 201)
			PLACE_NEAR=J4801.22:10MM
C8110 0.47UF	C8112 0.47UF	C8113 0.47UF	C8114 0.47UF
	NO STUFF	NO STUFF	NO STUFF

(10% 6.3V CERM-X5R 402)

TPAD_VBUS_EN (OUT 38 86)

P5VS3_EN — P5VS3_EN (MAKE_BASE=TRUE) (OUT 66 67)

P3V3S3_EN — P3V3S3_EN (MAKE_BASE=TRUE) (OUT 66 67)

DDRREG_EN — DDRREG_EN (MAKE_BASE=TRUE) (OUT 60 67)

S0 ENABLE

PP3V3_S5 → C8180 0.1uF (20% 10V CERM 402) → U8180 MC74VHC1G08 SC70-HF

(PM_SLP_S3_BUF_L) → NO STUFF R8180 100K (5% 1/16W MF-LF 402) → D8185 SOD-523 BAT54XV2T1

D8185 → R8185 130K (PLACE_NEAR=U7600.3:6mm) → C8185 0.82UF (PLACE_NEAR=U7600.3:6mm)

R8178 100 (PM_SLP_S3_L → PM_SLP_S3_R_L, MAKE_BASE=TRUE)

PM_SLP_S3_L:100K pull down in PCH page

P1V05_EN_D → R8138 820 (PLACE_NEAR=R8138.1:6mm)

R8186 20K	R8187 0	
C8186 0.68UF	C8187 0.68UF	NO STUFF

PM_SLP_S3_BUF_L (OUT 51 66 67 81 82 86) — PLACE_NEAR=Q8052.5:6mm

P5VS0_EN — P5VS0_EN (MAKE_BASE=TRUE) (OUT 66 67)

P3V3S0_P1V5_S0_EN — P3V3S0_P1V5_S0_EN (MAKE_BASE=TRUE) (OUT 64 66 67)

P1V05S0_EN — P1V05S0_EN (MAKE_BASE=TRUE) (OUT 62 67)

PM_SLP_S3_R_L (OUT 31 32 44 67) ×2

PLACE_NEAR=R8185.2:6mm; PLACE_NEAR=Q8052.5:6mm

CPUVCORE ENABLE

ALL_SYS_PWRGD — ALL_SYS_PWRGD (MAKE_BASE=TRUE) (OUT 18 19 40 58 67 86)

3.3V SUS Enable

PM_SLP_SUS_L — PM_SLP_SUS_L (MAKE_BASE=TRUE) (OUT 12 44 66 67) ×2

PM_SLP_SUS_L: 100K pull down on PCH page

S0 Rail PGOOD (BJT Version)

PP5V_S0 → R8151 54.9K (1% 1/16W MF-LF 402) → VMON_5V_DIV (5.0V Divider:1.07V)

PP3V3_S5 → R8156 150K (1% 1/16W MF-LF 402) → S0PGD_C

ALL_SYS_PWRGD

R8153 1K → VMON_Q2_BASE	R8154 1K → VMON_Q3_BASE	R8155 1K → VMON_Q4_BASE

PP1V35_S3RS0_CPUDDR → R8154; PP3V3_S0 → R8158 15.0K (1% 1/16W MF-LF 402) → VMON_3V3_DIV (3V3 Divider:1.07V) → R8159 7.15K

Q8150 ASMCC0179 DFN2015H4-8 353S2809 (Q1 Q2 Q3 Q4 CRITICAL; NC; NC)

S0PGD_BJT_GND_R → R8157 100

Vbe 0.7V max @2mA
Vce(sat) 0.1V max @1mA
Q1 Vth 0.7~1V @Id 250uA

3.3V SUS Detect

PP3V3_S5 → C8130 0.1uF (20% 10V CERM 402)

PP3V3_SUS → R8133 100K (5% 1/16W MF-LF 402)

U8130 TPS3808G33DBVRG4 SOT23-6 (CRITICAL; VDD; SENSE; RESET*; CT; MR*; GND)

PM_RSMRST_L → PM_RSMRST_L goes to U1100.C21

SUS_PGOOD_CT → C8131 0.001UF (NO STUFF, 20% 50V CERM 402)

TP_SUS_PGOOD_MR_L

S5 Rail Enables & PGOOD

PP3V42_G3H (PLACE_NEAR=U7501.20:7mm) → R8141 100K (5% 1/16W MF-LF 402) → S5_PWRGD (MAKE_BASE=TRUE)

S5_PWRGD-->SMC
SMC-->PM_DSW_PWRGD

SMC_PM_G2_EN (MAKE_BASE=TRUE) → R8140 100 → P3V3S5_EN (MAKE_BASE=TRUE)

SMC_PM_G2_EN → NO STUFF C8142 0.0033UF (10% 50V X7R-CERM 0402) (PLACE_NEAR=U7501.21:7mm)

S0 Rail PGOOD Circuitry
(ISL Version in development)

Thresholds:
VDD: 2.734V-3.010V
V2MON: 0.815V-3.009V
V3MON: 0.572V-0.630V
V4MON: 0.572V-0.630V

keep R8171 DDRCPU 1.35V only

PP3V3_S0 → R8195 10 (5% 1/16W MF-LF 402) → C8162 0.1UF (20% 10V X7R-CERM 0402) (PLACE_NEAR=U8160.2:4mm)

PP3V3_S0_VMON_P2 → C8160 0.1UF (20% 10V X7R-CERM 0402) (PLACE_NEAR=U8160.2:5mm)

PP3V3_S0_VMON_P7 → NOSTUFF R8197 100K → C8161 0.1UF (20% 10V X7R-CERM 0402) (PLACE_NEAR=U8160.7:6mm)

PP3V3_S0 → R8196 10 (5% 1/16W MF-LF 402) → C8163 0.1UF (20% 10V X7R-CERM 0402) (PLACE_NEAR=U8160.2:7mm)

PP1V35_S3RS0_CPUDDR; PP1V05_S0

R8160 6.04K; R8170 10K; R8172 6.04K (S0PGOOD_ISL) — PSV_VMON divider 3.16V @4.5V

R8161 15.0K; R8171 12.4K; R8173 15.0K (S0PGOOD_ISL) — 1V35_VMON divider 0.710V @1.31V; 1V05_VMON divider 0.710V @1.02V

U8160 ISL88042IRTEZ TDFN (CRITICAL; VDD; V2MON; V3MON; V4MON; GND; THRM_PAD; RST*; VMON_MR)

P1V5S0_PGOOD from U7810

P1V5S0_PGOOD → R8168 100 → PP1V5_S0

P1V05S0_PGOOD → R8169 100 → PP1V5_S0

R8167 10K → PM_SLP_S3_BUF_L

S0PGOOD_ISL → R8162 330 → ALL_SYS_PWRGD_R → ALL_SYS_PWRGD

1V5 S0 "PGOOD" Delay

PP3V3_S5 → R8136 23.7K (1% 1/16W MF-LF 402) → PM_1V5_PGD_L

C8134 2.2UF (10% 6.3V X5R 402)

DELAY_1V5S0_PGD → R8137 100 (5% 1/16W MF-LF 402) → ALL_SYS_PWRGD (OUT 18 19 40 58 67 86)

CRITICAL Q8151 DMB53D0UV SOT-563 (Vgs:0.7V~1.0V)

PM_1V5_PGD_L_R → R8139 2.0K (1% 1/16W MF-LF 402) → PM_1V5_PGD_DIV

R8135 54.9K; R8134 61.9K (1% 1/16W MF-LF 402)

CRITICAL Q8151 DMB53D0UV SOT-563 (VBEon: 0.58~0.7V; 1V5 Divider:0.75~0.85V)

PM_SLP_S3_R_L

CHGR VFRQ Generation

VFRQ High: Variable Frequency
VFRQ Low: Fix Frequency

PP3V42_G3H → R8131 100K (5% 1/16W MF-LF 402) → CHGR_VFRQ (OUT 57)

Unused PGOOD signals

Q8131 DMN32D2LFB4 DFN1006H4-3 SYM_VER_2

DDRREG_PGOOD (IN 60)

P5VS4_PGOOD (IN 61)

PP5V_S3 → R8120 470K (5% 1/20W MF 201) → PP5V_S4 → R8165 470K (5% 1/16W MF-LF 402)

WLAN Enable Generation

"WLAN" = ("S4" && "AP_PWR_EN" && ("AC" || "S0"))
NOTE: S4 term is guaranteed by S4 pull-up on open-drain AP_PWR_EN signal.

PP3V3_S4 → R8125 330K (5% 1/20W MF 201) → PM_WLAN_EN (MAKE_BASE=TRUE) (OUT 33 40 67)

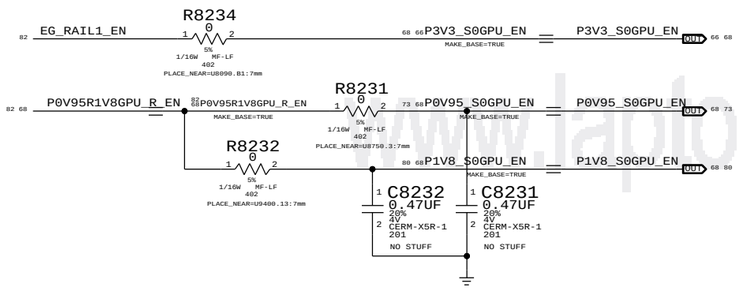
PM_WLAN_EN (IN 67)

SYNC_MASTER=J45_IG	SYNC_DATE=07/01/2014
PAGE TITLE	Power Control 1/ENABLE
Apple Inc.	DRAWING NUMBER <SCH_NUM> D; REVISION <E4LABEL>; BRANCH <BRANCH>; PAGE 81 OF 119; SHEET 67 OF 97

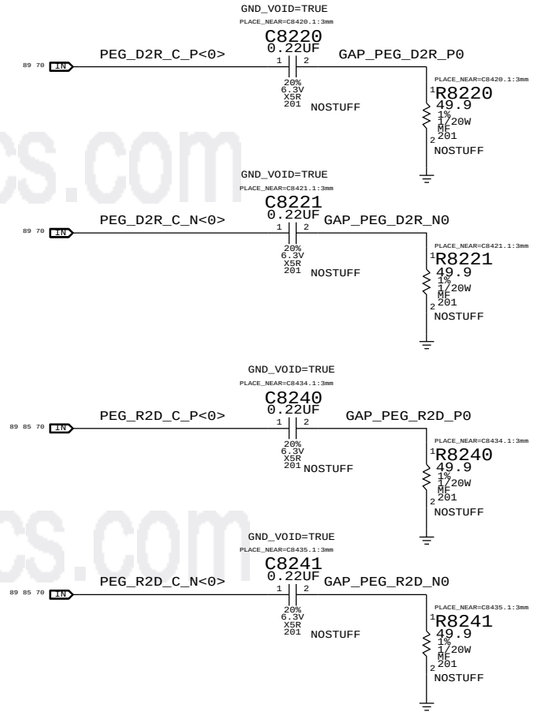
GPU Rails Power UP Sequencing

Venus GPU requires rails to come up in the following order:

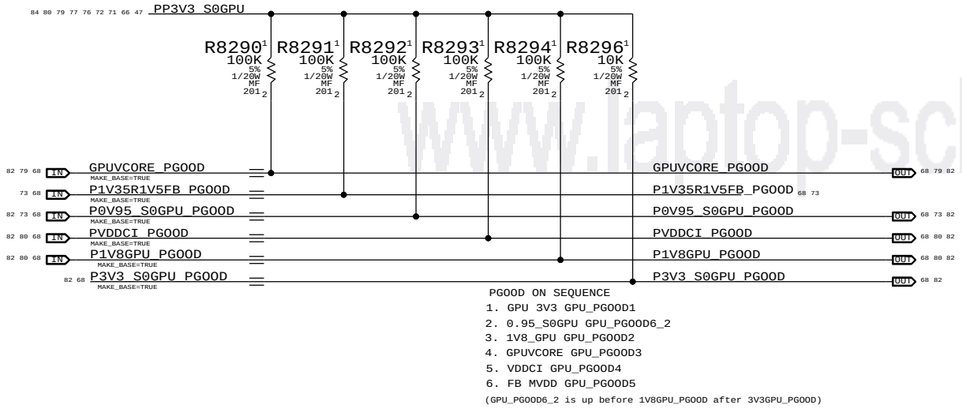
1) GPU_3.3V
2) GPU_0V95 (BIF_VDDC) & GPU_1V8 (VDD_CT)
3) GPUVCore
4) VDDCI
5) FB VRAM MVDD



PCIE TEST STRUCTURES (FOR LAB USE)
Pending Layout. Can add more.



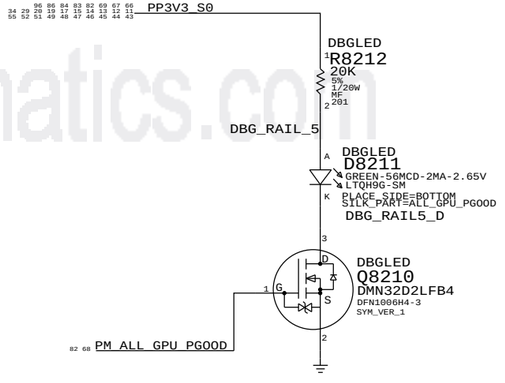
EXT GPU PWRGD Pullup



PGOOD ON SEQUENCE
1. GPU 3V3 GPU_PGOOD1
2. 0.95_S0GPU GPU_PGOOD6_2
3. 1V8_GPU GPU_PGOOD2
4. GPUVCORE GPU_PGOOD3
5. VDDCI GPU_PGOOD4
6. FB MVDD GPU_PGOOD5

(GPU_PGOOD6_2 is up before 1V8GPU_PGOOD after 3V3GPU_PGOOD)

Power State Debug LEDs
(For development only)



SYNC_MASTER=MARY_X425G SYNC_DATE=09/11/2014

PAGE TITLE: Power Sequencing EG/PGOOD

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 82 OF 119
SHEET: 68 OF 97

LCD PANEL INTERFACE (eDP)

5V TCON Switch

TCON 5V 2A

U8300
SLG5AP1443V
TDFN
CRITICAL

Part	SLG5AP1443V
Type	Load Switch
R(on) @100mA	17 mOhm Typ 19 mOhm Max
Current	2.5 A Max

3.3V_EDP ON/OFF CONTROL

3.3V TCON Switch

TCON 3V3 <30mA

U8310
TPS22904
CSP
CRITICAL

Part	TPS22904(353S3979)
Type	Load Switch
R(on) @ 3.6V	66 mOhm Typ 90 mOhm Max
Current	0.5A Max

LCD Panel HPD & AUX strapping

C8305 is placeholder for 3pF cap

SYNC_MASTER=MARY X425G	SYNC_DATE=12/11/2014
PAGE TITLE	eDP Display Connector
Apple Inc.	DRAWING NUMBER <SCH_NUM> D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 83 OF 119
	SHEET 69 OF 97

Page Notes

Power aliases required by this page:

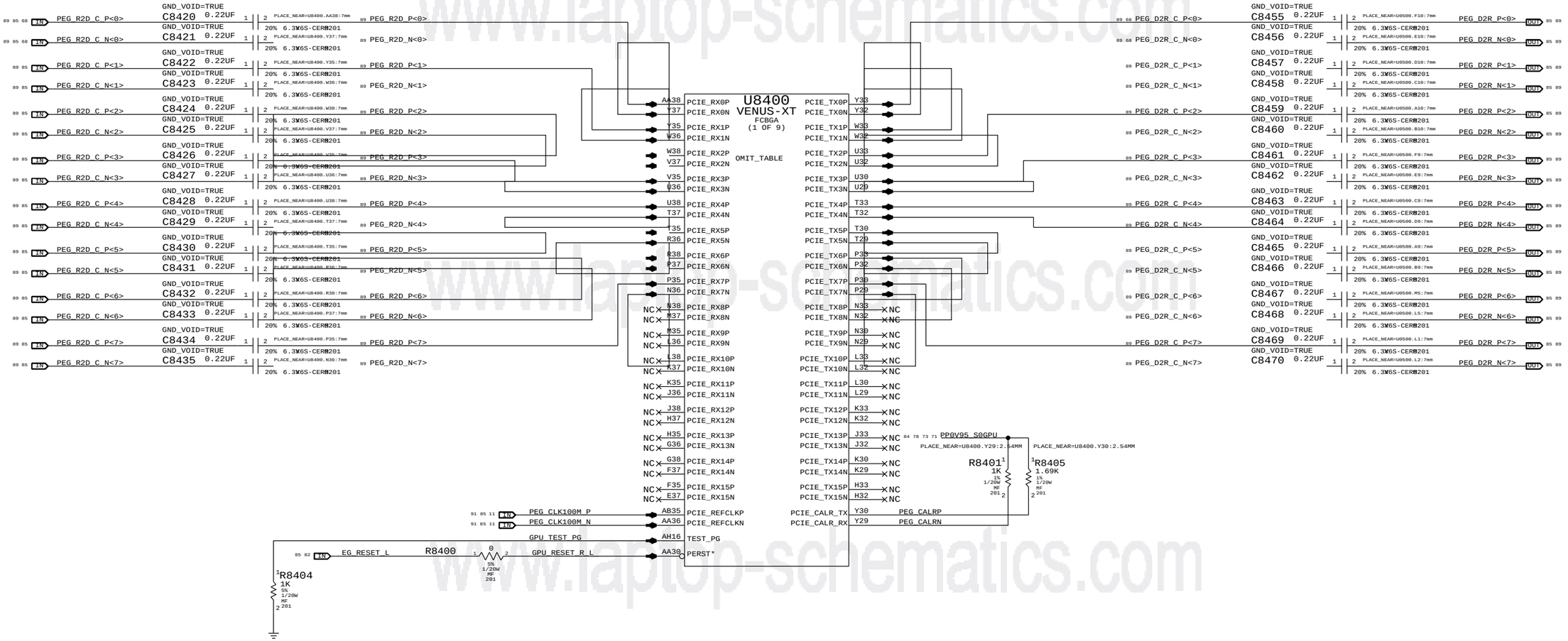
- +PPVS5_GPU_PCIE

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



SYNC_MASTER=MARY_X425G	SYNC_DATE=08/22/2014
PAGE TITLE	Venus PCI-E
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 84 OF 119
	SHEET 70 OF 97

Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V5R1V35_GPU_FB_VDDR1
- =PP1V8_GPU_VDD_CT
- =PP1V8_GPU_PLL
- =PP3V3_GPU_VDDR3
- =PP3V3_GPU_VDDR4
- =PP1V8_GPU_MEM_PLL
- =PP1V8_GPU_PLL
- =PP1V8_GPU_PCIE_VDDR
- =PP1V8_GPU_PCIE_VDDC

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

U8400 VENUS-XT FCBGA (7 OF 9)

OMIT_TABLE

PP1V35_GPU_REG — 2000mA

C8504 12PF 5% NP0-C0G 0201 25V (CRITICAL)
C8517 3.0PF +/-0.1PF 25V NP0-C0G 0201 (CRITICAL)
C8500 10UF 20% 6.3V CERM-X6S 0402
C8501 10UF 20% 6.3V CERM-X6S 0402
C8502 10UF 20% 6.3V CERM-X6S 0402

C8505 2.2UF 20% 4V X6S-CERM 0201
C8506 2.2UF 20% 4V X6S-CERM 0201
C8507 2.2UF 20% 4V X6S-CERM 0201
C8508 2.2UF 20% 4V X6S-CERM 0201
C8509 2.2UF 20% 4V X6S-CERM 0201
C8510 0.01UF 10% 10V X7R-CERM 0201
C8511 0.01UF 10% 10V X7R-CERM 0201
C8512 0.01UF 10% 10V X7R-CERM 0201
C8513 0.01UF 10% 10V X7R-CERM 0201
C8514 0.01UF 10% 10V X7R-CERM 0201

C8520 0.1UF 10% 6.3V X7R 0201
C8521 0.1UF 10% 6.3V X7R 0201
C8522 0.1UF 10% 6.3V X7R 0201
C8523 0.1UF 10% 6.3V X7R 0201
C8524 0.1UF 10% 6.3V X7R 0201

AC7, AD11, AF7, AG10, AJ7, AK8, AL9, G11, G14, G17, G20, G23, G26, G29, H10, J7, J9, K11, K13, K8, L12, L16, L21, L23, L26, L7, M11, N11, P7, R11, U11, U7, Y11, Y7 → VDDR1

PP1V8_GPUIFPX — 250mA
L8520 120OHM-25%-1.8A-0.06DCR (CRITICAL) 0402
PLACE_NEAR=L8520.1:2.54MM
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
C8515 0.1UF 10% 6.3V X7R 0201
C8525 10UF 20% 6.3V CERM-X6S 0402
C8528 1.0UF 20% 4V X6S 0201
C8529 0.1UF 10% 6.3V X7R 0201
PLACE_NEAR=U8400.AF26:2.54MM
PLACE_NEAR=U8400.AG26:2.54MM

AF26, AF27, AG26, AG27 → VDD_CT

PP3V3_S0GPU — 60mA
L8551 120OHM-25%-1.8A-0.06DCR (CRITICAL) 0402
PLACE_NEAR=L8551.1:2.54MM
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
C8516 0.1UF 10% 6.3V X7R 0201
C8533 1UF 20% 6.3V X6S-CERM 0201
C8534 1UF 20% 6.3V X6S-CERM 0201
C8535 0.1UF 10% 6.3V X7R 0201
PLACE_NEAR=U8400.AF23:2.54MM
PLACE_NEAR=U8400.AG23:2.54MM

AF23, AF24, AG23, AG24 → VDDR3

AD12, AF11, AF12, AF13, AF15, AG11, AG13, AG15 → VDDR4

PP1V8_GPUIFPX — 300mA
C85C0 10UF 20% 6.3V CERM-X6S 0402
C85C1 1.0UF 20% 4V X6S 0201
C85C2 0.1UF 10% 6.3V X7R 0201
PLACE_NEAR=U8400.AF12:2.54MM
PLACE_NEAR=U8400.AG13:2.54MM

PP1V8_GPUIFPX — 150mA
L8531 220-OHM-1A 0402 150mohm DCR (CRITICAL)
PLACE_NEAR=L8531.1:2.54MM
C8518 0.1UF 10% 6.3V X7R 0201
C8537 10UF 20% 6.3V CERM-X6S 0402
C8538 1.0UF 20% 4V X6S 0201
C8540 0.1UF 10% 6.3V X7R 0201
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
PLACE_NEAR=U8400.H7:2.54MM
PLACE_NEAR=U8400.H8:2.54MM

H7, H8 → MPLL_PVDD

AM10 → SPLL_PVDD
AN9 → SPLL_VDDC
GND_SPLL_PVSS → AN10 → SPLL_PVSS

PP1V8_GPUIFPX
L8532 120OHM-25%-1.8A-0.06DCR (CRITICAL) 0402
PLACE_NEAR=L8532.1:2.54MM
C8519 0.1UF 10% 6.3V X7R 0201
XW8542
PP1V8_GPU_PLL — 75mA
C8542 10UF 20% 6.3V CERM-X6S 0402
C8543 1.0UF 20% 4V X6S 0201
C8544 0.1UF 10% 6.3V X7R 0201
PLACE_NEAR=U8400.AM10:2.54MM
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

VSNS_GPU_VDDC_P → AF28 → FB_VDDC
VSNS_GPU_VDDI_P → AG28 → FB_VDDCI
GPU_GND_SENSE → AH29 → FB_GND

V28, W29 → NC_BIF_VDDC
AA31, AA32, AA33, AA34, W30 → NC_PCIE_VDDR

PP0V95_S0GPU
L8530 120OHM-25%-1.8A-0.06DCR (CRITICAL) 0402
PLACE_NEAR=L8530.1:2.54MM
C8503 0.1UF 10% 6.3V X7R 0201
PP0V95_GPU_PLL — 150mA
C8530 10UF 20% 6.3V CERM-X6S 0402
C8531 1.0UF 20% 4V X6S 0201
C8532 0.1UF 10% 6.3V X7R 0201
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.95V
PLACE_NEAR=U8400.AN9:2.54MM

PP1V8_GPUIFPX — 200mA
C8545 10UF 20% 6.3V CERM-X6S 0402
C8547 1.0UF 20% 4V X6S 0201
C8548 1.0UF 20% 4V X6S 0201
PLACE_NEAR=U8400.AB37:2.54MM

Y31, AB37 → PCIE_PVDD

PP0V95_S0GPU — 2500mA
C8559 12PF 5% NP0-C0G 0201 25V (CRITICAL)
C855A 3.0PF +/-0.1PF 25V NP0-C0G 0201 (CRITICAL)
C8550 10UF 20% 6.3V CERM-X6S 0402
C8551 10UF 20% 6.3V CERM-X6S 0402
C8552 1.0UF 20% 4V X6S 0201
C8553 1.0UF 20% 4V X6S 0201
C8554 1.0UF 20% 4V X6S 0201
C8555 1.0UF 20% 4V X6S 0201
C8556 1.0UF 20% 4V X6S 0201
C8557 1.0UF 20% 4V X6S 0201
C8558 1.0UF 20% 4V X6S 0201

G30, G31, H29, H30, J29, J30, L28, M28, N28, R28, T28, U28 → PCIE_VDDC

AA15, AA17, AA20, AA22, AA24, AA27, AB16, AB18, AB21, AB23, AB26, AB28, AC17, AC20, AC22, AC24, AC27, AD18, AD21, AD23, AD26, AF17, AF20, AF22, AG16, AG18, AH22, AH27, AH28, M26, N24, N27, R18, R21, R23, R26, T17, T20, T22, T24, T27, U16, U18, U21, U23, U26, V17, V20, V22, V24, V27, Y16, Y18, Y21, Y23, Y26, Y28 → VDDC

PPVCORE_GPU — 52A (63A?)

C8560 2.2UF 20% 4V X6S-CERM 0201
C8561 2.2UF 20% 4V X6S-CERM 0201
C8562 2.2UF 20% 4V X6S-CERM 0201
C8563 2.2UF 20% 4V X6S-CERM 0201
C8564 2.2UF 20% 4V X6S-CERM 0201
C8565 2.2UF 20% 4V X6S-CERM 0201
C8566 2.2UF 20% 4V X6S-CERM 0201
C8567 2.2UF 20% 4V X6S-CERM 0201

C8570 2.2UF 20% 4V X6S-CERM 0201
C8571 2.2UF 20% 4V X6S-CERM 0201
C8572 2.2UF 20% 4V X6S-CERM 0201
C8573 2.2UF 20% 4V X6S-CERM 0201
C8574 2.2UF 20% 4V X6S-CERM 0201
C8575 2.2UF 20% 4V X6S-CERM 0201
C8576 2.2UF 20% 4V X6S-CERM 0201
C8577 2.2UF 20% 4V X6S-CERM 0201

C8590 10UF 20% 6.3V CERM-X6S 0402
C8591 10UF 20% 6.3V CERM-X6S 0402
C8592 10UF 20% 6.3V CERM-X6S 0402
C8593 10UF 20% 6.3V CERM-X6S 0402
C8594 10UF 20% 6.3V CERM-X6S 0402
C8595 10UF 20% 6.3V CERM-X6S 0402
C8596 10UF 20% 6.3V CERM-X6S 0402
C8597 12PF 5% NP0-C0G 0201 25V (CRITICAL)
C8598 3.0PF +/-0.1PF 25V NP0-C0G 0201 (CRITICAL)

BIF_VDDC — 1200mA — PP0V95_S0GPU

PPVCORE_GPU
R8510 (NOSTUFF) 100 1% 1/20W MF 201 — PLACE_NEAR=U8400.AF28:2.54MM
VSNS_GPU_VDDC_P
R8510/1/2 only stuffed for GPU VR measurement

GPU_GND_SENSE — VOLTAGE=0.0V — MIN_LINE_WIDTH=0.3MM — MIN_NECK_WIDTH=0.2MM
XW8510 (NO_XNET_CONNECTION=TRUE) → VSNS_GPU_VDDC_N → OUT
XW8512 → VSNS_GPU_VDDI_N → OUT (NO_XNET_CONNECTION=TRUE)
R8511 (NOSTUFF) 100 1% 1/20W MF 201 — PLACE_NEAR=U8400.AH29:2.54MM

PPVDDCI_S0_ISENSE
R8512 (NOSTUFF) 100 1% 1/20W MF 201 — PLACE_NEAR=U8400.AG28:2.54MM
VSNS_GPU_VDDI_P

PPVDDCI_S0_ISENSE — 7A@0.9V

AA13, AB13, AC12, AC15, AD13, AD16, M15, M16, M18, M23, N13, N15, N17, N20, N22, R12, R13, R16, T12, T15, V15, Y13 → VDDCI

C85A0 0.1UF 10% 6.3V X7R 0201
C85A1 0.1UF 10% 6.3V X7R 0201
C85A2 0.1UF 10% 6.3V X7R 0201
C85A7 1.0UF 20% 4V X6S 0201
C85A8 1.0UF 20% 4V X6S 0201
C85A9 1.0UF 20% 4V X6S 0201
C85A3 12PF 5% NP0-C0G 0201 25V (CRITICAL)
C85A4 3.0PF +/-0.1PF 25V NP0-C0G 0201 (CRITICAL)
C85B0 10UF 20% 6.3V CERM-X6S 0402

SYNC_MASTER=MARY_X425G — SYNC_DATE=09/22/2014

PAGE TITLE: Venus CORE/FB POWER

Apple Inc.

DRAWING NUMBER: <SCH_NUM> — SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 85 OF 119
SHEET: 71 OF 97

Page Notes

Power aliases required by this page:

- =PP1V5R1V3S_FB_CAL
- =PP1V5R1V3S_FB_REF

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

U8400
VENUS-XT
FCBGA
(4 OF 9)

OMIT_TABLE

FB_A0_DQ<0>	C37	DQA0_0	
FB_A0_DQ<1>	C35	DQA0_1	
FB_A0_DQ<2>	A35	DQA0_2	
FB_A0_DQ<3>	E34	DQA0_3	
FB_A0_DQ<4>	G32	DQA0_4	
FB_A0_DQ<5>	D33	DQA0_5	
FB_A0_DQ<6>	F32	DQA0_6	
FB_A0_DQ<7>	E32	DQA0_7	
FB_A0_DQ<8>	D31	DQA0_8	
FB_A0_DQ<9>	F30	DQA0_9	
FB_A0_DQ<10>	C30	DQA0_10	
FB_A0_DQ<11>	A30	DQA0_11	
FB_A0_DQ<12>	F28	DQA0_12	
FB_A0_DQ<13>	C28	DQA0_13	
FB_A0_DQ<14>	A28	DQA0_14	
FB_A0_DQ<15>	E28	DQA0_15	
FB_A0_DQ<16>	D27	DQA0_16	
FB_A0_DQ<17>	F26	DQA0_17	
FB_A0_DQ<18>	C26	DQA0_18	
FB_A0_DQ<19>	A26	DQA0_19	
FB_A0_DQ<20>	F24	DQA0_20	
FB_A0_DQ<21>	C24	DQA0_21	
FB_A0_DQ<22>	A24	DQA0_22	
FB_A0_DQ<23>	E24	DQA0_23	
FB_A0_DQ<24>	C22	DQA0_24	
FB_A0_DQ<25>	A22	DQA0_25	
FB_A0_DQ<26>	F22	DQA0_26	
FB_A0_DQ<27>	D21	DQA0_27	
FB_A0_DQ<28>	A20	DQA0_28	
FB_A0_DQ<29>	F20	DQA0_29	
FB_A0_DQ<30>	D19	DQA0_30	
FB_A0_DQ<31>	E18	DQA0_31	
FB_A1_DQ<0>	C18	DQA1_0	
FB_A1_DQ<1>	A18	DQA1_1	
FB_A1_DQ<2>	F18	DQA1_2	
FB_A1_DQ<3>	D17	DQA1_3	
FB_A1_DQ<4>	A16	DQA1_4	
FB_A1_DQ<5>	F16	DQA1_5	
FB_A1_DQ<6>	D15	DQA1_6	
FB_A1_DQ<7>	E14	DQA1_7	
FB_A1_DQ<8>	F14	DQA1_8	
FB_A1_DQ<9>	D13	DQA1_9	
FB_A1_DQ<10>	F12	DQA1_10	
FB_A1_DQ<11>	A12	DQA1_11	
FB_A1_DQ<12>	D11	DQA1_12	
FB_A1_DQ<13>	F10	DQA1_13	
FB_A1_DQ<14>	A10	DQA1_14	
FB_A1_DQ<15>	C10	DQA1_15	
FB_A1_DQ<16>	G13	DQA1_16	
FB_A1_DQ<17>	H13	DQA1_17	
FB_A1_DQ<18>	J13	DQA1_18	
FB_A1_DQ<19>	H11	DQA1_19	
FB_A1_DQ<20>	G10	DQA1_20	
FB_A1_DQ<21>	G8	DQA1_21	
FB_A1_DQ<22>	K9	DQA1_22	
FB_A1_DQ<23>	K10	DQA1_23	
FB_A1_DQ<24>	G9	DQA1_24	
FB_A1_DQ<25>	A8	DQA1_25	
FB_A1_DQ<26>	C8	DQA1_26	
FB_A1_DQ<27>	E8	DQA1_27	
FB_A1_DQ<28>	A6	DQA1_28	
FB_A1_DQ<29>	C6	DQA1_29	
FB_A1_DQ<30>	E6	DQA1_30	
FB_A1_DQ<31>	A5	DQA1_31	
FB_A_VREFD	L18	MVREFDA	
FB_A_VREFS	L20	MVREFSA	
NC	L27	NC_MEM_CALRN0	
NC	N12	NC_MEM_CALRN1	
NC	AG12	NC_MEM_CALRN2	
FB_CALRP0	M27	MEM_CALRP0	
NC	M12	NC_MEM_CALRP1	
NC	AH12	NC_MEM_CALRP2	

NOSTUFF R8613 120 1% 1/20W MF 201 PLACE_NEAR=U8400.M27:2.54MM

MAA0_0	G24	FB_A0_A<0>	OUT
MAA0_1	J23	FB_A0_A<1>	OUT
MAA0_2	H24	FB_A0_A<2>	OUT
MAA0_3	J24	FB_A0_A<3>	OUT
MAA0_4	H26	FB_A0_A<4>	OUT
MAA0_5	J26	FB_A0_A<5>	OUT
MAA0_6	H21	FB_A0_A<6>	OUT
MAA0_7	G21	FB_A0_A<7>	OUT
MAA1_0	H19	FB_A1_A<0>	OUT
MAA1_1	H20	FB_A1_A<1>	OUT
MAA1_2	L13	FB_A1_A<2>	OUT
MAA1_3	G16	FB_A1_A<3>	OUT
MAA1_4	J16	FB_A1_A<4>	OUT
MAA1_5	H16	FB_A1_A<5>	OUT
MAA1_6	J17	FB_A1_A<6>	OUT
MAA1_7	H17	FB_A1_A<7>	OUT
WCKA0_0	A32	FB_A0_WCLK_P<0>	B
WCKA0_0*	C32	FB_A0_WCLK_N<0>	B
WCKA0_1	D23	FB_A0_WCLK_P<1>	B
WCKA0_1*	E22	FB_A0_WCLK_N<1>	B
WCKA1_0	C14	FB_A1_WCLK_P<0>	B
WCKA1_0*	A14	FB_A1_WCLK_N<0>	B
WCKA1_1	E10	FB_A1_WCLK_P<1>	B
WCKA1_1*	D9	FB_A1_WCLK_N<1>	B
EDCA0_0	C34	FB_A0_EDC<0>	IN
EDCA0_1	D29	FB_A0_EDC<1>	IN
EDCA0_2	D25	FB_A0_EDC<2>	IN
EDCA0_3	E20	FB_A0_EDC<3>	IN
EDCA1_0	E16	FB_A1_EDC<0>	IN
EDCA1_1	E12	FB_A1_EDC<1>	IN
EDCA1_2	J10	FB_A1_EDC<2>	IN
EDCA1_3	D7	FB_A1_EDC<3>	IN
DDBIA0_0	A34	FB_A0_DBI_L<0>	B
DDBIA0_1	E30	FB_A0_DBI_L<1>	B
DDBIA0_2	E26	FB_A0_DBI_L<2>	B
DDBIA0_3	C20	FB_A0_DBI_L<3>	B
DDBIA1_0	C16	FB_A1_DBI_L<0>	B
DDBIA1_1	C12	FB_A1_DBI_L<1>	B
DDBIA1_2	J11	FB_A1_DBI_L<2>	B
DDBIA1_3	F8	FB_A1_DBI_L<3>	B
ADBIA0	J21	FB_A0_ABI_L	B
ADBIA1	G19	FB_A1_ABI_L	B
CLKA0	H27	FB_A0_CLK_P	OUT
CLKA0*	G27	FB_A0_CLK_N	OUT
CLKA1	J14	FB_A1_CLK_P	OUT
CLKA1*	H14	FB_A1_CLK_N	OUT
RASA0*	K23	FB_A0_RAS_L	OUT
RASA1*	K19	FB_A1_RAS_L	OUT
CASA0*	K20	FB_A0_CAS_L	OUT
CASA1*	K17	FB_A1_CAS_L	OUT
CSA0_0*	K24	FB_A0_CS_L	OUT
CSA0_1*	K27	NC	
CSA1_0*	M13	FB_A1_CS_L	OUT
CSA1_1*	K16	NC	
CKEA0	K21	FB_A0_CKE_L	OUT
CKEA1	J20	FB_A1_CKE_L	OUT
WEA0*	K26	FB_A0_WE_L	OUT
WEA1*	L15	FB_A1_WE_L	OUT
MAA0_8	H23	FB_A0_A<8>	OUT
MAA0_9	M21	NC_FB_A0_A<9>	87
MAA1_8	J19	FB_A1_A<8>	OUT
MAA1_9	M20	NC_FB_A1_A<9>	87

DQB0_0	C5	FB_B0_DQ<0>	B
DQB0_1	C3	FB_B0_DQ<1>	B
DQB0_2	E3	FB_B0_DQ<2>	B
DQB0_3	E1	FB_B0_DQ<3>	B
DQB0_4	F1	FB_B0_DQ<4>	B
DQB0_5	F3	FB_B0_DQ<5>	B
DQB0_6	F5	FB_B0_DQ<6>	B
DQB0_7	G4	FB_B0_DQ<7>	B
DQB0_8	H5	FB_B0_DQ<8>	B
DQB0_9	H6	FB_B0_DQ<9>	B
DQB0_10	J4	FB_B0_DQ<10>	B
DQB0_11	K6	FB_B0_DQ<11>	B
DQB0_12	K5	FB_B0_DQ<12>	B
DQB0_13	L4	FB_B0_DQ<13>	B
DQB0_14	M6	FB_B0_DQ<14>	B
DQB0_15	M1	FB_B0_DQ<15>	B
DQB0_16	M3	FB_B0_DQ<16>	B
DQB0_17	M5	FB_B0_DQ<17>	B
DQB0_18	N4	FB_B0_DQ<18>	B
DQB0_19	P6	FB_B0_DQ<19>	B
DQB0_20	P5	FB_B0_DQ<20>	B
DQB0_21	R4	FB_B0_DQ<21>	B
DQB0_22	T6	FB_B0_DQ<22>	B
DQB0_23	T1	FB_B0_DQ<23>	B
DQB0_24	U4	FB_B0_DQ<24>	B
DQB0_25	V6	FB_B0_DQ<25>	B
DQB0_26	V1	FB_B0_DQ<26>	B
DQB0_27	V3	FB_B0_DQ<27>	B
DQB0_28	Y6	FB_B0_DQ<28>	B
DQB0_29	Y1	FB_B0_DQ<29>	B
DQB0_30	Y3	FB_B0_DQ<30>	B
DQB0_31	Y5	FB_B0_DQ<31>	B
DQB1_0	AA4	FB_B1_DQ<0>	B
DQB1_1	AB6	FB_B1_DQ<1>	B
DQB1_2	AB1	FB_B1_DQ<2>	B
DQB1_3	AB3	FB_B1_DQ<3>	B
DQB1_4	AD6	FB_B1_DQ<4>	B
DQB1_5	AD1	FB_B1_DQ<5>	B
DQB1_6	AD3	FB_B1_DQ<6>	B
DQB1_7	AD5	FB_B1_DQ<7>	B
DQB1_8	AF1	FB_B1_DQ<8>	B
DQB1_9	AF3	FB_B1_DQ<9>	B
DQB1_10	AF6	FB_B1_DQ<10>	B
DQB1_11	AG4	FB_B1_DQ<11>	B
DQB1_12	AH5	FB_B1_DQ<12>	B
DQB1_13	AH6	FB_B1_DQ<13>	B
DQB1_14	AJ4	FB_B1_DQ<14>	B
DQB1_15	AK3	FB_B1_DQ<15>	B
DQB1_16	AF8	FB_B1_DQ<16>	B
DQB1_17	AF9	FB_B1_DQ<17>	B
DQB1_18	AG8	FB_B1_DQ<18>	B
DQB1_19	AG7	FB_B1_DQ<19>	B
DQB1_20	AK9	FB_B1_DQ<20>	B
DQB1_21	AL7	FB_B1_DQ<21>	B
DQB1_22	AM8	FB_B1_DQ<22>	B
DQB1_23	AM7	FB_B1_DQ<23>	B
DQB1_24	AK1	FB_B1_DQ<24>	B
DQB1_25	AL4	FB_B1_DQ<25>	B
DQB1_26	AM6	FB_B1_DQ<26>	B
DQB1_27	AM1	FB_B1_DQ<27>	B
DQB1_28	AN4	FB_B1_DQ<28>	B
DQB1_29	AP3	FB_B1_DQ<29>	B
DQB1_30	AP1	FB_B1_DQ<30>	B
DQB1_31	AP5	FB_B1_DQ<31>	B
FB_B_VREFD	Y12	MVREFDB	
FB_B_VREFS	AA12	MVREFSB	
GPU_TEST_EN	AD28	TESTEN	
GPU_CLK_TEST_P	AK10	CLKTESTA	
GPU_CLK_TEST_N	AL10	CLKTESTB	

PP3V3_S0GPU

NOSTUFF R8665 10K 5% 1/20W MF 201

NOSTUFF C8651 0.1UF 10% 6.3V XSR 201

NOSTUFF C8652 0.1UF 10% 6.3V XSR 201

R8650 10K 5% 1/20W MF 201

GPU_CLK_TEST_RC_P — NOSTUFF R8651 51.1 1% 1/20W MF 201

GPU_CLK_TEST_RC_N — NOSTUFF R8652 51.1 1% 1/20W MF 201

U8400
VENUS-XT
FCBGA
(5 OF 9)

OMIT_TABLE

MAB0_0	P8	FB_B0_A<0>	OUT
MAB0_1	T9	FB_B0_A<1>	OUT
MAB0_2	P9	FB_B0_A<2>	OUT
MAB0_3	N7	FB_B0_A<3>	OUT
MAB0_4	N8	FB_B0_A<4>	OUT
MAB0_5	N9	FB_B0_A<5>	OUT
MAB0_6	U9	FB_B0_A<6>	OUT
MAB0_7	U8	FB_B0_A<7>	OUT
MAB1_0	Y9	FB_B1_A<0>	OUT
MAB1_1	W9	FB_B1_A<1>	OUT
MAB1_2	AC8	FB_B1_A<2>	OUT
MAB1_3	AC9	FB_B1_A<3>	OUT
MAB1_4	AA7	FB_B1_A<4>	OUT
MAB1_5	AA8	FB_B1_A<5>	OUT
MAB1_6	Y8	FB_B1_A<6>	OUT
MAB1_7	AA9	FB_B1_A<7>	OUT
WCKB0_0	H3	FB_B0_WCLK_P<0>	B
WCKB0_0*	H1	FB_B0_WCLK_N<0>	B
WCKB0_1	T3	FB_B0_WCLK_P<1>	B
WCKB0_1*	T5	FB_B0_WCLK_N<1>	B
WCKB1_0	AE4	FB_B1_WCLK_P<0>	B
WCKB1_0*	AF5	FB_B1_WCLK_N<0>	B
WCKB1_1	AK6	FB_B1_WCLK_P<1>	B
WCKB1_1*	AK5	FB_B1_WCLK_N<1>	B
EDCB0_0	F6	FB_B0_EDC<0>	IN
EDCB0_1	K3	FB_B0_EDC<1>	IN
EDCB0_2	P3	FB_B0_EDC<2>	IN
EDCB0_3	V5	FB_B0_EDC<3>	IN
EDCB1_0	AB5	FB_B1_EDC<0>	IN
EDCB1_1	AH1	FB_B1_EDC<1>	IN
EDCB1_2	AJ9	FB_B1_EDC<2>	IN
EDCB1_3	AM5	FB_B1_EDC<3>	IN
DDBIB0_0	G7	FB_B0_DBI_L<0>	B
DDBIB0_1	K1	FB_B0_DBI_L<1>	B
DDBIB0_2	P1	FB_B0_DBI_L<2>	B
DDBIB0_3	W4	FB_B0_DBI_L<3>	B
DDBIB1_0	AC4	FB_B1_DBI_L<0>	B
DDBIB1_1	AH3	FB_B1_DBI_L<1>	B
DDBIB1_2	AJ8	FB_B1_DBI_L<2>	B
DDBIB1_3	AM3	FB_B1_DBI_L<3>	B
ADBIB0	T7	FB_B0_ABI_L	B
ADBIB1	W7	FB_B1_ABI_L	B
CLKB0	L9	FB_B0_CLK_P	OUT
CLKB0*	L8	FB_B0_CLK_N	OUT
CLKB1	AD8	FB_B1_CLK_P	OUT
CLKB1*	AD7	FB_B1_CLK_N	OUT
RASB0*	T10	FB_B0_RAS_L	OUT
RASB1*	Y10	FB_B1_RAS_L	OUT
CASB0*	W10	FB_B0_CAS_L	OUT
CASB1*	AA10	FB_B1_CAS_L	OUT
CSB0_0*	P10	FB_B0_CS_L	OUT
CSB0_1*	L10	NC	
CSB1_0*	AD10	FB_B1_CS_L	OUT
CSB1_1*	AC10	NC	
CKEB0	U10	FB_B0_CKE_L	OUT
CKEB1	AA11	FB_B1_CKE_L	OUT
WEB0*	N10	FB_B0_WE_L	OUT
WEB1*	AB11	FB_B1_WE_L	OUT
MAB0_8	T8	FB_B0_A<8>	OUT
MAB0_9	U12	NC_FB_B0_A<9>	87
MAB1_8	W8	FB_B1_A<8>	OUT
MAB1_9	V12	NC_FB_B1_A<9>	87
DRAM_RST	AH11	GPU_FB_RESET_L	

PLACE_NEAR=U8400.AH11:5MM

R8661 10 1% 1/20W MF 201 — PLACE_NEAR=U8400.AH11:5MM

R8660 4.99K 1% 1/20W MF 201

C8660 120PF 5% 50V C0G-CERM 0402 — PLACE_NEAR=R8661.2:5MM

R8662 51 1% 1/20W MF 201 — PLACE_NEAR=R8661.2:5MM

FB_RESET_RC_L — FB_RESET_L — OUT 74 75

PP1V35_GPU_REG

PLACE_NEAR=U8400.L18:2.54MM — NOSTUFF R8600 40.2 1% 1/20W MF 201

FB_A_VREFD — NOSTUFF R8601 100 1% 1/20W MF 201 — PLACE_NEAR=U8400.L18:2.54MM

NOSTUFF C8600 1.0UF 20% 6.3V XSR 0201 — PLACE_NEAR=U8400.L18:2.54MM

PP1V35_GPU_REG

PLACE_NEAR=U8400.L20:2.54MM — NOSTUFF R8602 40.2 1% 1/20W MF 201

FB_A_VREFS — NOSTUFF R8603 100 1% 1/20W MF 201 — PLACE_NEAR=U8400.L20:2.54MM

NOSTUFF C8601 1.0UF 20% 6.3V XSR 0201 — PLACE_NEAR=U8400.L20:2.54MM

PP1V35_GPU_REG

PLACE_NEAR=U8400.Y12:2.54MM — NOSTUFF R8604 40.2 1% 1/20W MF 201

FB_B_VREFD — NOSTUFF R8605 100 1% 1/20W MF 201 — PLACE_NEAR=U8400.Y12:2.54MM

NOSTUFF C8602 1.0UF 20% 6.3V XSR 0201 — PLACE_NEAR=U8400.Y12:2.54MM

PP1V35_GPU_REG

PLACE_NEAR=U8400.AA12:2.54MM — NOSTUFF R8606 40.2 1% 1/20W MF 201

FB_B_VREFS — NOSTUFF R8607 100 1% 1/20W MF 201 — PLACE_NEAR=U8400.AA12:2.54MM

NOSTUFF C8603 1.0UF 20% 6.3V XSR 0201 — PLACE_NEAR=U8400.AA12:2.54MM

SYNC_MASTER=J45G_AMD — SYNC_DATE=06/30/2014

PAGE TITLE: Venus FRAME BUFFER I/F

Apple Inc.

DRAWING NUMBER: <SCH_NUM> — SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 86 OF 119

SHEET: 72 OF 97

GPU FB SUPPLY

VOUT = 1.5V / 1.35V
12A MAX OUTPUT
F = 500 KHZ

MIRROR C8702 AND C8708

U8700
ISL95870AH
UTQFN
CRITICAL

Q8710
SIZ710DT
APN 152S00140
POWERPAK-6X3.7
L8710 CRITICAL
0.68UH-20%-14A

GPIO 21 --> VID1

VID1	VID0	FBVDD
0	0	1.5V
1	0	1.35V

GPU 0.95V/BIF_VDDC SUPPLY

VOUT = 0.95V
5.2A MAX OUTPUT
F = 500 KHZ

MIRROR C8750 AND C8758

U8750
ISL95870
UTQFN
CRITICAL

Q8760
CSD58873Q3D
Q3D

L8760
1.0UH-20%-8.6A
PIME053T-SM

Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=ADITYA_X425G	SYNC_DATE=09/16/2014
PAGE TITLE	0V95 GPU / 1V35 FB Power Supply
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 87 OF 119
	SHEET 73 OF 97

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Page Notes

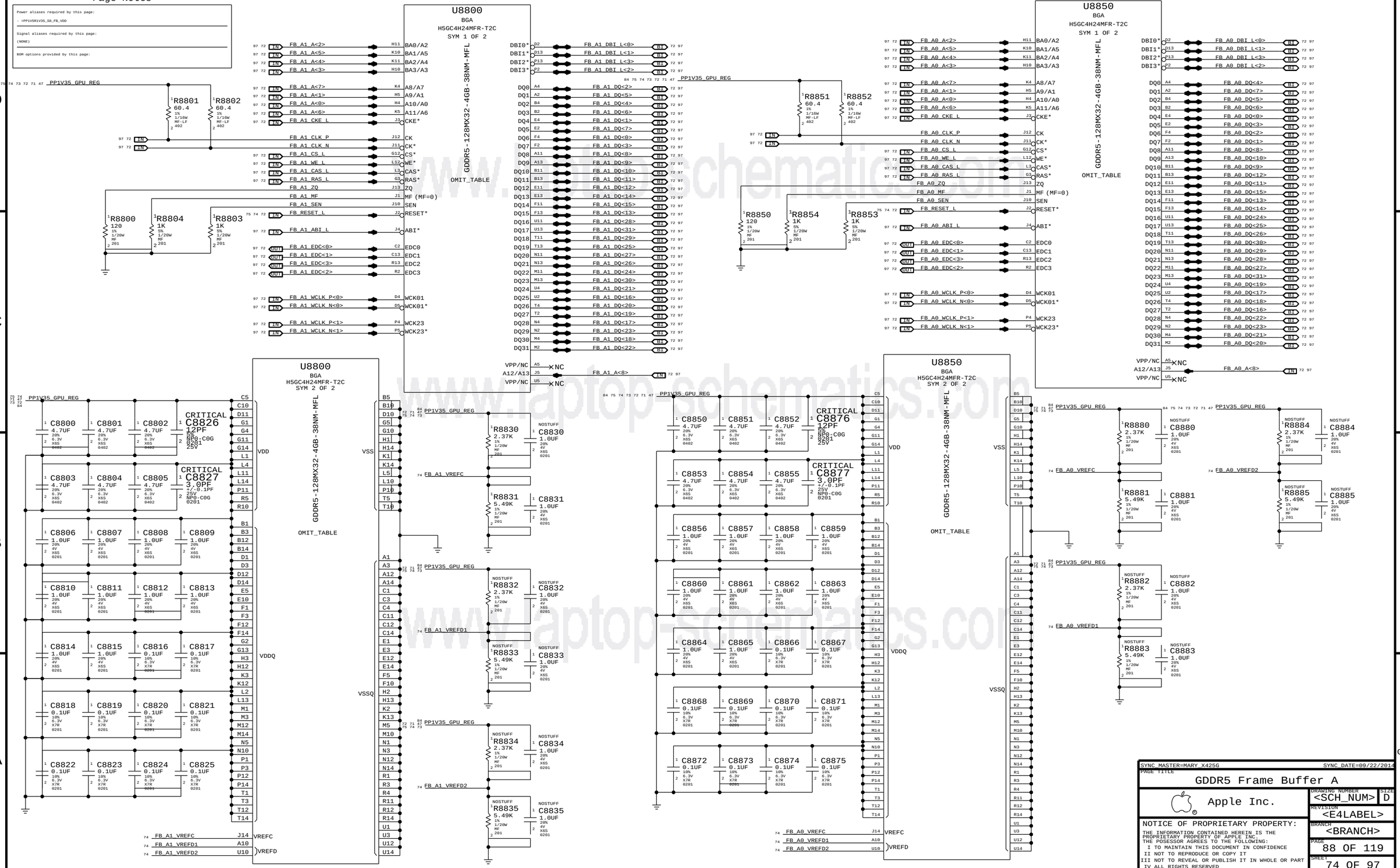
Power aliases required by this page:

- =PP1VSR1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:



SYNC_MASTER=MARY_X425G SYNC_DATE=09/22/2014

PAGE TITLE: GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 88 OF 119

SHEET: 74 OF 97

Page Notes

Power aliases required by this page:

- =PP1VSR1V35_S0_FB_VDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

PP1V35_GPU_REG

R8901 60.4 1% 1/16W MF-LF 402
R8902 60.4 1% 1/16W MF-LF 402
R8951 60.4 1% 1/16W MF-LF 402
R8952 60.4 1% 1/16W MF-LF 402

R8900 120 1% 1/20W MF 201
R8904 1K 5% 1/20W MF 201
R8903 1K 5% 1/20W MF 201
R8950 120 1% 1/20W MF 201
R8954 1K 5% 1/20W MF 201
R8953 1K 5% 1/20W MF 201

U8900

BGA
H5GC4H24MFR-T2C
SYM 1 OF 2

GDDR5-128MX32-4GB-38NM-MFL

OMIT_TABLE

FB_B1_A<2>	H11	BA0/A2	
FB_B1_A<5>	K10	BA1/A5	
FB_B1_A<4>	K11	BA2/A4	
FB_B1_A<3>	H10	BA3/A3	
FB_B1_A<7>	K4	A8/A7	
FB_B1_A<1>	H5	A9/A1	
FB_B1_A<0>	H4	A10/A0	
FB_B1_A<6>	K5	A11/A6	
FB_B1_CKE_L	J3	CKE*	
FB_B1_CLK_P	J12	CK	
FB_B1_CLK_N	J11	CK*	
FB_B1_CS_L	G12	CS*	
FB_B1_WE_L	L12	WE*	
FB_B1_CAS_L	L3	CAS*	
FB_B1_RAS_L	G3	RAS*	
FB_B1_ZQ	J13	ZQ	
FB_B1_MF	J1	MF (MF=0)	
FB_B1_SEN	J10	SEN	
FB_RESET_L	J2	RESET*	
FB_B1_ABI_L	J4	ABI*	
FB_B1_EDC<0>	C2	EDC0	
FB_B1_EDC<1>	C13	EDC1	
FB_B1_EDC<3>	R13	EDC2	
FB_B1_EDC<2>	R2	EDC3	
FB_B1_WCLK_P<0>	D4	WCK01	
FB_B1_WCLK_N<0>	D5	WCK01*	
FB_B1_WCLK_P<1>	P4	WCK23	
FB_B1_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_B1_DBI_L<0>	
DBI1*	D13	FB_B1_DBI_L<1>	
DBI2*	P13	FB_B1_DBI_L<3>	
DBI3*	P2	FB_B1_DBI_L<2>	
DQ0	A4	FB_B1_DQ<3>	
DQ1	A2	FB_B1_DQ<4>	
DQ2	B4	FB_B1_DQ<6>	
DQ3	B2	FB_B1_DQ<1>	
DQ4	E4	FB_B1_DQ<2>	
DQ5	E2	FB_B1_DQ<0>	
DQ6	F4	FB_B1_DQ<5>	
DQ7	F2	FB_B1_DQ<7>	
DQ8	A11	FB_B1_DQ<10>	
DQ9	A13	FB_B1_DQ<9>	
DQ10	B11	FB_B1_DQ<8>	
DQ11	B13	FB_B1_DQ<13>	
DQ12	E11	FB_B1_DQ<11>	
DQ13	E13	FB_B1_DQ<15>	
DQ14	F11	FB_B1_DQ<12>	
DQ15	F13	FB_B1_DQ<14>	
DQ16	U11	FB_B1_DQ<30>	
DQ17	U13	FB_B1_DQ<31>	
DQ18	T11	FB_B1_DQ<28>	
DQ19	T13	FB_B1_DQ<29>	
DQ20	N11	FB_B1_DQ<26>	
DQ21	N13	FB_B1_DQ<27>	
DQ22	M11	FB_B1_DQ<25>	
DQ23	M13	FB_B1_DQ<24>	
DQ24	U4	FB_B1_DQ<23>	
DQ25	U2	FB_B1_DQ<22>	
DQ26	T4	FB_B1_DQ<20>	
DQ27	T2	FB_B1_DQ<21>	
DQ28	N4	FB_B1_DQ<19>	
DQ29	N2	FB_B1_DQ<18>	
DQ30	M4	FB_B1_DQ<17>	
DQ31	M2	FB_B1_DQ<16>	
VPP/NC	A5	NC	
A12/A13	J5	NC	
VPP/NC	U5	NC	

FB_B1_A<8>

U8950

BGA
H5GC4H24MFR-T2C
SYM 1 OF 2

GDDR5-128MX32-4GB-38NM-MFL

OMIT_TABLE

FB_B0_A<2>	H11	BA0/A2	
FB_B0_A<5>	K10	BA1/A5	
FB_B0_A<4>	K11	BA2/A4	
FB_B0_A<3>	H10	BA3/A3	
FB_B0_A<7>	K4	A8/A7	
FB_B0_A<1>	H5	A9/A1	
FB_B0_A<0>	H4	A10/A0	
FB_B0_A<6>	K5	A11/A6	
FB_B0_CKE_L	J3	CKE*	
FB_B0_CLK_P	J12	CK	
FB_B0_CLK_N	J11	CK*	
FB_B0_CS_L	G12	CS*	
FB_B0_WE_L	L12	WE*	
FB_B0_CAS_L	L3	CAS*	
FB_B0_RAS_L	G3	RAS*	
FB_B0_ZQ	J13	ZQ	
FB_B0_MF	J1	MF (MF=0)	
FB_B0_SEN	J10	SEN	
FB_RESET_L	J2	RESET*	
FB_B0_ABI_L	J4	ABI*	
FB_B0_EDC<1>	C2	EDC0	
FB_B0_EDC<0>	C13	EDC1	
FB_B0_EDC<2>	R13	EDC2	
FB_B0_EDC<3>	R2	EDC3	
FB_B0_WCLK_P<0>	D4	WCK01	
FB_B0_WCLK_N<0>	D5	WCK01*	
FB_B0_WCLK_P<1>	P4	WCK23	
FB_B0_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_B0_DBI_L<1>	
DBI1*	D13	FB_B0_DBI_L<0>	
DBI2*	P13	FB_B0_DBI_L<2>	
DBI3*	P2	FB_B0_DBI_L<3>	
DQ0	A4	FB_B0_DQ<8>	
DQ1	A2	FB_B0_DQ<9>	
DQ2	B4	FB_B0_DQ<10>	
DQ3	B2	FB_B0_DQ<11>	
DQ4	E4	FB_B0_DQ<14>	
DQ5	E2	FB_B0_DQ<13>	
DQ6	F4	FB_B0_DQ<15>	
DQ7	F2	FB_B0_DQ<12>	
DQ8	A11	FB_B0_DQ<0>	
DQ9	A13	FB_B0_DQ<5>	
DQ10	B11	FB_B0_DQ<1>	
DQ11	B13	FB_B0_DQ<4>	
DQ12	E11	FB_B0_DQ<6>	
DQ13	E13	FB_B0_DQ<7>	
DQ14	F11	FB_B0_DQ<2>	
DQ15	F13	FB_B0_DQ<3>	
DQ16	U11	FB_B0_DQ<21>	
DQ17	U13	FB_B0_DQ<23>	
DQ18	T11	FB_B0_DQ<18>	
DQ19	T13	FB_B0_DQ<22>	
DQ20	N11	FB_B0_DQ<20>	
DQ21	N13	FB_B0_DQ<16>	
DQ22	M11	FB_B0_DQ<17>	
DQ23	M13	FB_B0_DQ<19>	
DQ24	U4	FB_B0_DQ<31>	
DQ25	U2	FB_B0_DQ<29>	
DQ26	T4	FB_B0_DQ<30>	
DQ27	T2	FB_B0_DQ<26>	
DQ28	N4	FB_B0_DQ<27>	
DQ29	N2	FB_B0_DQ<24>	
DQ30	M4	FB_B0_DQ<28>	
DQ31	M2	FB_B0_DQ<25>	
VPP/NC	A5	NC	
A12/A13	J5	NC	
VPP/NC	U5	NC	

FB_B0_A<8>

U8900

BGA
H5GC4H24MFR-T2C
SYM 2 OF 2

GDDR5-128MX32-4GB-38NM-MFL

OMIT_TABLE

PP1V35_GPU_REG

C8900 4.7UF 20% 6.3V X6S 0402
C8901 4.7UF 20% 6.3V X6S 0402
C8902 4.7UF 20% 6.3V X6S 0402
CRITICAL C8926 12PF 5% 50V NP0-C0G 0201
C8903 4.7UF 20% 6.3V X6S 0402
C8904 4.7UF 20% 6.3V X6S 0402
C8905 4.7UF 20% 6.3V X6S 0402
CRITICAL C8927 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8906 1.0UF 20% 4V X6S 0201
C8907 1.0UF 20% 4V X6S 0201
C8908 1.0UF 20% 4V X6S 0201
C8909 1.0UF 20% 4V X6S 0201
C8910 1.0UF 20% 4V X6S 0201
C8911 1.0UF 20% 4V X6S 0201
C8912 1.0UF 20% 4V X6S 0201
C8913 1.0UF 20% 4V X6S 0201
C8914 1.0UF 20% 4V X6S 0201
C8915 1.0UF 20% 4V X6S 0201
C8916 0.1UF 10% 6.3V X7R 0201
C8917 0.1UF 10% 6.3V X7R 0201
C8918 0.1UF 10% 6.3V X7R 0201
C8919 0.1UF 10% 6.3V X7R 0201
C8920 0.1UF 10% 6.3V X7R 0201
C8921 0.1UF 10% 6.3V X7R 0201
C8922 0.1UF 10% 6.3V X7R 0201
C8923 0.1UF 10% 6.3V X7R 0201
C8924 0.1UF 10% 6.3V X7R 0201
C8925 0.1UF 10% 6.3V X7R 0201

VDD
VDDQ

FB_B1_VREFC → VREFC
FB_B1_VREFD1 → VREFD
FB_B1_VREFD2 → VREFD

VSS
VSSQ

PP1V35_GPU_REG

R8930 2.37K 1% 1/20W MF 201
C8930 1.0UF 20% 4V X6S 0201
FB_B1_VREFC
R8931 5.49K 1% 1/20W MF 201
C8931 1.0UF 20% 4V X6S 0201

PP1V35_GPU_REG

NOSTUFF R8932 2.37K 1% 1/20W MF 201
NOSTUFF C8932 1.0UF 20% 4V X6S 0201
FB_B1_VREFD1
NOSTUFF R8933 5.49K 1% 1/20W MF 201
NOSTUFF C8933 1.0UF 20% 4V X6S 0201

PP1V35_GPU_REG

NOSTUFF R8934 2.37K 1% 1/20W MF 201
NOSTUFF C8934 1.0UF 20% 4V X6S 0201
FB_B1_VREFD2
NOSTUFF R8935 5.49K 1% 1/20W MF 201
NOSTUFF C8935 1.0UF 20% 4V X6S 0201

U8950

BGA
H5GC4H24MFR-T2C
SYM 2 OF 2

GDDR5-128MX32-4GB-38NM-MFL

OMIT_TABLE

PP1V35_GPU_REG

C8950 4.7UF 20% 6.3V X6S 0402
C8951 4.7UF 20% 6.3V X6S 0402
C8952 4.7UF 20% 6.3V X6S 0402
CRITICAL C8976 12PF 5% 50V NP0-C0G 0201
C8953 4.7UF 20% 6.3V X6S 0402
C8954 4.7UF 20% 6.3V X6S 0402
C8955 4.7UF 20% 6.3V X6S 0402
CRITICAL C8977 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8956 1.0UF 20% 4V X6S 0201
C8957 1.0UF 20% 4V X6S 0201
C8958 1.0UF 20% 4V X6S 0201
C8959 1.0UF 20% 4V X6S 0201
C8960 1.0UF 20% 4V X6S 0201
C8961 1.0UF 20% 4V X6S 0201
C8962 1.0UF 20% 4V X6S 0201
C8963 1.0UF 20% 4V X6S 0201
C8964 1.0UF 20% 4V X6S 0201
C8965 1.0UF 20% 4V X6S 0201
C8966 0.1UF 10% 6.3V X7R 0201
C8967 0.1UF 10% 6.3V X7R 0201
C8968 0.1UF 10% 6.3V X7R 0201
C8969 0.1UF 10% 6.3V X7R 0201
C8970 0.1UF 10% 6.3V X7R 0201
C8971 0.1UF 10% 6.3V X7R 0201
C8972 0.1UF 10% 6.3V X7R 0201
C8973 0.1UF 10% 6.3V X7R 0201
C8974 0.1UF 10% 6.3V X7R 0201
C8975 0.1UF 10% 6.3V X7R 0201

VDD
VDDQ

FB_B0_VREFC → VREFC
FB_B0_VREFD1 → VREFD
FB_B0_VREFD2 → VREFD

VSS
VSSQ

PP1V35_GPU_REG

R8980 2.37K 1% 1/20W MF 201
NOSTUFF C8980 1.0UF 20% 4V X6S 0201
FB_B0_VREFC
R8981 5.49K 1% 1/20W MF 201
C8981 1.0UF 20% 4V X6S 0201

PP1V35_GPU_REG

NOSTUFF R8982 2.37K 1% 1/20W MF 201
NOSTUFF C8982 1.0UF 20% 4V X6S 0201
FB_B0_VREFD1
R8983 5.49K 1% 1/20W MF 201
NOSTUFF C8983 1.0UF 20% 4V X6S 0201

PP1V35_GPU_REG

NOSTUFF R8984 2.37K 1% 1/20W MF 201
NOSTUFF C8984 1.0UF 20% 4V X6S 0201
FB_B0_VREFD2
NOSTUFF R8985 5.49K 1% 1/20W MF 201
NOSTUFF C8985 1.0UF 20% 4V X6S 0201

SYNC_MASTER=MARY_X425G	SYNC_DATE=09/22/2014
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER <SCH_NUM> SIZE D
	REVISION <E4LABEL>
	BRANCH <BRANCH>
	PAGE 89 OF 119
	SHEET 75 OF 97

GPU Int Temp Sense can not be read through SMBUS

CRITICAL
Q9010
DMN5L06VK-7
SOT563
VER 5

SMBUS "0"
SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

PP3V3_S0GPU

R9020 4.7K 5% 1/20W MF 201
R9021 4.7K 5% 1/20W MF 201

CRITICAL
Q9010
DMN5L06VK-7
SOT563
VER 5

CRITICAL
L9002
120OHM-25%-1.8A-0.06DCR
0402

PP1V8_GPUIFPX
PP1V8_GPUIFPX_TSVDD
8mA
(GND_GPU_TSVSS)
GND_GPU_TSVSS

XW9001 SM

C9015 0.1UF 10% 6.3V X7R 0201
C9007 10UF 20% 6.3V CERM-X6S 0402
C9008 1.0UF 20% 4V X6S 0201
C9009 0.1UF 10% 6.3V X7R 0201

PLACE_NEAR=L9002.1:2.54MM
PLACE_NEAR=U8400.AJ32:2.54MM
PLACE_NEAR=U8400.AJ32:2.54MM

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

R9035 10K 5% 1/20W MF 201

R9002 499 1% 1/20W MF 201
R9003 249 1% 1/20W MF 201
C9000 0.1UF 10% 6.3V X7R 0201

PLACE_NEAR=U8400.AH13:2.54MM
PLACE_NEAR=U8400.AH13:2.54MM

CRITICAL
Y9000
2.50X2.00MM-SM
27MHZ-30PPM-12PF-40OHM
C9080 15PF 5% 50V C0G 0201
C9081 15PF 5% 50V C0G 0201
R9082 1M 5% 1/20W MF 201

R9023 1K 5% 1/20W MF 201 NOSTUFF
R9024 1K 5% 1/20W MF 201 NOSTUFF

U8400
VENUS-XT
FCBGA
(2 OF 9)

OMIT_TABLE

NC_DVPCNTL_M<0>	AR8	DVPCNTL_MVP_0
NC_DVPCNTL_M<1>	AU8	DVPCNTL_MVP_1
NC_DVPCNTL<0>	AP8	DVPCNTL_0
NC_DVPCNTL<1>	AW8	DVPCNTL_1
NC_DVPCNTL<2>	AR3	DVPCNTL_2
NC_DVPCLK	AR1	DVPCLK
TP_DVPDATA<0>	AU1	DVPDATA_0
TP_DVPDATA<1>	AU3	DVPDATA_1
TP_DVPDATA<2>	AW3	DVPDATA_2
TP_DVPDATA<3>	AP6	DVPDATA_3
TP_DVPDATA<4>	AW5	DVPDATA_4
TP_DVPDATA<5>	AU5	DVPDATA_5
NC_DVPDATA<6>	AR6	DVPDATA_6
NC_DVPDATA<7>	AW6	DVPDATA_7
NC_DVPDATA<8>	AU6	DVPDATA_8
NC_DVPDATA<9>	AT7	DVPDATA_9
NC_DVPDATA<10>	AV7	DVPDATA_10
NC_DVPDATA<11>	AN7	DVPDATA_11
NC_DVPDATA<12>	AV9	DVPDATA_12
NC_DVPDATA<13>	AT9	DVPDATA_13
NC_DVPDATA<14>	AR10	DVPDATA_14
NC_DVPDATA<15>	AW10	DVPDATA_15
NC_DVPDATA<16>	AU10	DVPDATA_16
NC_DVPDATA<17>	AP10	DVPDATA_17
NC_DVPDATA<18>	AV11	DVPDATA_18
NC_DVPDATA<19>	AT11	DVPDATA_19
NC_DVPDATA<20>	AR12	DVPDATA_20
NC_DVPDATA<21>	AW12	DVPDATA_21
NC_DVPDATA<22>	AU12	DVPDATA_22
NC_DVPDATA<23>	AP12	DVPDATA_23
	AJ21	SWAPLOCKA
	AK21	SWAPLOCKB
	AK26	SCL
	AJ26	SDA
GFX_VDDCI_ALTV	AH20	GPIO_0
NC_GPU_GPIO_1	AH18	GPIO_1
NC_GPU_GPIO_2	AN16	GPIO_2
GPU_SMB_CLK	AJ23	SMBCLK
GPU_SMB_DAT	AH23	SMBDATA
GPU_GFX_PWR_LEVEL_R_L	AH17	GPIO_5_AC_BATT
GFXIMVP_VR_ICCMAX_WARN_L	AJ17	GPIO_6
EG_BKLT_EN	AK17	GPIO_7_BLON
GPU_ROM_SO	AJ13	GPIO_8_ROMSO
GPU_ROM_SI	AH15	GPIO_9_ROMSI
GPU_ROM_SCLK	AJ16	GPIO_10_ROMSCK
GPU_VCORE_VID4	AK16	GPIO_11
GPU_VCORE_VID5	AL16	GPIO_12
GPU_VCORE_VID0	AM16	GPIO_13
DP_TBTSNK1_HPD_EG	AM14	GPIO_14_HPD2
GPU_VCORE_VID1	AM13	GPIO_15_PWRCNTL_0
GPU_VCORE_VID2	AK14	GPIO_16
GFX_SELF_THROTTLE_R	AG30	GPIO_17_THERMAL_INT
HDMI_EG_HPD	AN14	GPIO_18_HPD3
GPU_GFX_OVERTEMP_R	AM17	GPIO_19_CTF
GPU_VCORE_VID3	AL13	GPIO_20_PWRCNTL_1
FBVDD_ALTV0	AJ14	GPIO_21
GPU_ROM_CS_L	AK13	GPIO_22_ROMCS*
GPU_MLPS_EN_L	AK32	GPIO_28_FDO
GPU_VCORE_PSI_L	AG32	GPIO_29
GFXIMVP_DPSLP_EN_R	AG33	GPIO_30
GPU_JTAG_TRST_L	AM23	JTAG_TRST*
GPU_JTAG_TDI	AN23	JTAG_TDI
GPU_JTAG_TCK	AK23	JTAG_TCK
GPU_JTAG_TMS	AL24	JTAG_TMS
GPU_JTAG_TDO	AM24	JTAG_TDO
NC_GPU_GENERICA	AJ19	GENERICA
NC_GPU_GENERICB	AK19	GENERICB
NC_DP_EXTB_CA_DET_EG	AJ20	GENERICC
NC_DP_EXTA_CA_DET_EG	AK20	GENERICD
NC_GPU_GPIO_33	AJ24	GENERICE_HPD4
DP_INT_EG_HPD	AH26	GENERICF_HPD5
NC_GPU_GPIO_35	AH24	GENERICG_HPD6
DP_TBTSNK0_HPD_EG	AK24	HPD1
	AH13	VREFG
GPU_27M_XTAL_IN	AV33	XTALIN
GPU_27M_XTAL_OUT	AU34	XTALOUT
PD_GPU_CLK27M	AW34	XO_IN
PD_GPU_CLK100M	AW35	XO_IN2
GPU_TDIODE_P	AF29	DPLUS
GPU_TDIODE_N	AG29	DMINUS
	AL31	TS_A
	AJ32	TSVDD
	AJ33	TSVSS

TXCAP_DPA3P	AU24	DP_TBTSNK0_ML_C_P<3>
TXCAM_DPA3N	AV23	DP_TBTSNK0_ML_C_N<3>
TX0P_DPA2P	AT25	DP_TBTSNK0_ML_C_P<2>
TX0M_DPA2N	AR24	DP_TBTSNK0_ML_C_N<2>
TX1P_DPA1P	AU26	DP_TBTSNK0_ML_C_P<1>
TX1M_DPA1N	AV25	DP_TBTSNK0_ML_C_N<1>
TX2P_DPA0P	AT27	DP_TBTSNK0_ML_C_P<0>
TX2M_DPA0N	AR26	DP_TBTSNK0_ML_C_N<0>
TXCBP_DPB3P	AR30	NC
TXCBM_DPB3N	AT29	NC
TX3P_DPB2P	AV31	NC
TX3M_DPB2N	AU30	NC
TX4P_DPB1P	AR32	NC
TX4M_DPB1N	AT31	NC
TX5P_DPB0P	AT33	NC
TX5M_DPB0N	AU32	NC
TXCCP_DPC3P	AU14	DP_TBTSNK1_ML_C_P<3>
TXCCM_DPC3N	AV13	DP_TBTSNK1_ML_C_N<3>
TX0P_DPC2P	AT15	DP_TBTSNK1_ML_C_P<2>
TX0M_DPC2N	AR14	DP_TBTSNK1_ML_C_N<2>
TX1P_DPC1P	AU16	DP_TBTSNK1_ML_C_P<1>
TX1M_DPC1N	AV15	DP_TBTSNK1_ML_C_N<1>
TX2P_DPC0P	AT17	DP_TBTSNK1_ML_C_P<0>
TX2M_DPC0N	AR16	DP_TBTSNK1_ML_C_N<0>
TXCDP_DPD3P	AU20	NC
TXCDM_DPD3N	AT19	NC
TX3P_DPD2P	AT21	NC
TX3M_DPD2N	AR20	NC
TX4P_DPD1P	AU22	NC
TX4M_DPD1N	AV21	NC
TX5P_DPD0P	AT23	NC
TX5M_DPD0N	AR22	NC
R	AD39	NC
G	AE36	NC
B	AF37	NC
HSYNC	AC36	GPU_AUD_1
VSYNC	AC38	GPU_AUD_0
RSET	AB34	GPU_RSET
AVDD	AD34	PP1V8_GPUIFPX
AVSSQ	AE34	
VDD1DI	AC33	
VSS1DI	AC34	
AVSSN0	AE38	
AVSSN1	AD35	
AVSSN2	AD37	
GENLK_CLK	AD29	NC
GENLK_VSYNC	AC29	NC
CEC_1	AC30	NC
CLKREQ*	AN13	TP_CLKREQ_L
NC_TSVSSQ	AF33	NC
NC_XTAL_PVSS	AF31	NC
NC_XTAL_PVDD	AF30	NC
DDC1CLK	AM26	DPA_EG_DDC_CLK
DDC1DATA	AN26	DPA_EG_DDC_DATA
AUX1P	AM27	DP_TBTSNK0_EG_AUXCH_P
AUX1N	AL27	DP_TBTSNK0_EG_AUXCH_N
DDC2CLK	AM19	DPB_EG_DDC_CLK
DDC2DATA	AL19	DPB_EG_DDC_DATA
AUX2P	AN20	DP_TBTSNK1_EG_AUXCH_P
AUX2N	AM20	DP_TBTSNK1_EG_AUXCH_N
DDCCLK_AUX3P	AL30	NC
DDCDATA_AUX3N	AM30	NC
DDCCLK_AUX4P	AL29	NC
DDCDATA_AUX4N	AM29	NC
DDCCLK_AUX5P	AN21	HDMI_EG_DDC_CLK_Q
DDCDATA_AUX5N	AM21	HDMI_EG_DDC_DATA_Q
DDCVGACLK	AJ30	NC
DDCVGADATA	AJ31	NC
DDCCLK_AUX6P	AK30	DP_INT_EG_AUX_P
DDCDATA_AUX6N	AK29	DP_INT_EG_AUX_N

Straps for audio on DP and HDMI
PP3V3_S0GPU
R9004 10K 5% 1/20W MF 201
R9005 10K 5% 1/20W MF 201
R9050 499 1% 1/20W MF 201

R9006 10K 5% 1/20W MF 201

U8400
VENUS-XT
FCBGA
(3 OF 9)

OMIT_TABLE

VARY_BL	AK27	GPU_LCD_BLK_PWM
DIGON	AJ27	EG_LCD_PWR_EN
TXCLK_UP_DPF3P	AK35	DP_INT_EG_ML_P<3>
TXCLK_UN_DPF3N	AL36	DP_INT_EG_ML_N<3>
TXOUT_U0P_DPF2P	AJ38	DP_INT_EG_ML_P<2>
TXOUT_U0N_DPF2N	AK37	DP_INT_EG_ML_N<2>
TXOUT_U1P_DPF1P	AH35	DP_INT_EG_ML_P<1>
TXOUT_U1N_DPF1N	AJ36	DP_INT_EG_ML_N<1>
TXOUT_U2P_DPF0P	AG38	DP_INT_EG_ML_P<0>
TXOUT_U2N_DPF0N	AH37	DP_INT_EG_ML_N<0>
TXOUT_U3P	AF35	NC
TXOUT_U3N	AG36	NC
TXCLK_LP_DPE3P	AP34	HDMI_EG_CLK_P
TXCLK_LN_DPE3N	AR34	HDMI_EG_CLK_N
TXOUT_L0P_DPE2P	AW37	HDMI_EG_DATA_P<0>
TXOUT_L0N_DPE2N	AU35	HDMI_EG_DATA_N<0>
TXOUT_L1P_DPE1P	AR37	HDMI_EG_DATA_P<1>
TXOUT_L1N_DPE1N	AU39	HDMI_EG_DATA_N<1>
TXOUT_L2P_DPE0P	AP35	HDMI_EG_DATA_P<2>
TXOUT_L2N_DPE0N	AR35	HDMI_EG_DATA_N<2>
TXOUT_L3P	AN36	NC
TXOUT_L3N	AP37	NC

PP3V3_S0GPU
R9025 4.7K 1% 1/20W MF 201
R9026 4.7K 1% 1/20W MF 201

CRITICAL
Q9000
DMN5L06VK-7
SOT563
VER 5

CRITICAL
Q9000
DMN5L06VK-7
SOT563
VER 5

DDC 3.3V level isolation

Page Notes

Power aliases required by this page:
- +PP3V3_GPU_I2C
- +PP1V8_GPU_VREFG
- +PP1V8_GPU_DPLL
- +PP1V8_GPU_DPLL
- +PP1V8_GPU_TS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=MARY_X425G SYNC_DATE=09/22/2014
PAGE TITLE
Venus HDMI/DP/GPIO

Apple Inc.

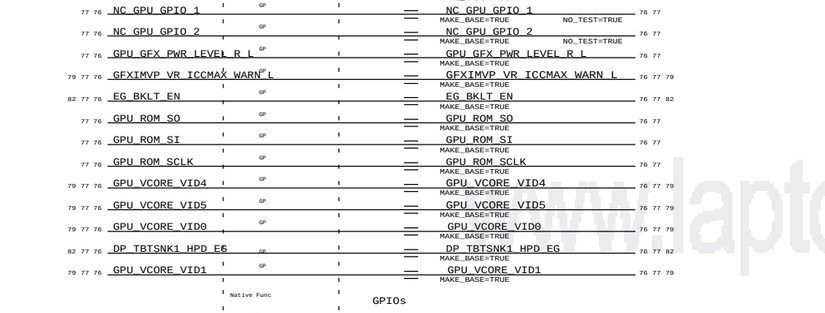
DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 90 OF 119
SHEET 76 OF 97

GPU GPIO TABLE

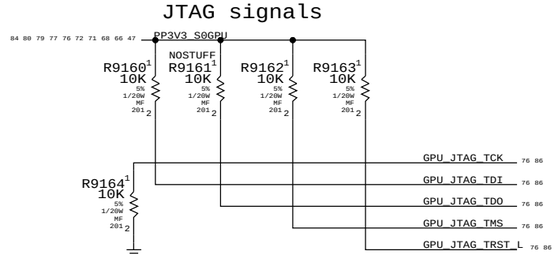
		Native Func				
80 77 76	GFX_VDDCI_ALTV	GP	GFX_VDDCI_ALTV	MAKE_BASE=TRUE		76 77 80
77 76	NC_GPU_GPIO_1	GP	NC_GPU_GPIO_1	MAKE_BASE=TRUE	NO_TEST=TRUE	76 77
77 76	NC_GPU_GPIO_2	GP	NC_GPU_GPIO_2	MAKE_BASE=TRUE	NO_TEST=TRUE	76 77
77 76	GPU_GFX_PWR_LEVEL_R_L	GP	GPU_GFX_PWR_LEVEL_R_L	MAKE_BASE=TRUE		76 77
79 77 76	GFXIMVP_VR_ICCMAX_WARN_L	GP	GFXIMVP_VR_ICCMAX_WARN_L	MAKE_BASE=TRUE		76 77 79
82 77 76	EG_BKLT_EN	GP	EG_BKLT_EN	MAKE_BASE=TRUE		76 77 82
77 76	GPU_ROM_SO	GP	GPU_ROM_SO	MAKE_BASE=TRUE		76 77
77 76	GPU_ROM_SI	GP	GPU_ROM_SI	MAKE_BASE=TRUE		76 77
77 76	GPU_ROM_SCLK	GP	GPU_ROM_SCLK	MAKE_BASE=TRUE		76 77
79 77 76	GPU_VCORE_VID4	GP	GPU_VCORE_VID4	MAKE_BASE=TRUE		76 77 79
79 77 76	GPU_VCORE_VID5	GP	GPU_VCORE_VID5	MAKE_BASE=TRUE		76 77 79
79 77 76	GPU_VCORE_VID0	GP	GPU_VCORE_VID0	MAKE_BASE=TRUE		76 77 79
82 77 76	DP_TBTSNK1_HPD_EG	GP	DP_TBTSNK1_HPD_EG	MAKE_BASE=TRUE		76 77 82
79 77 76	GPU_VCORE_VID1	GP	GPU_VCORE_VID1	MAKE_BASE=TRUE		76 77 79

		Native Func				
79 77 76	GPU_VCORE_VID2	GP	GPU_VCORE_VID2	MAKE_BASE=TRUE		76 77 79
77 76	GFX_SELF_THROTTLE_R	GP	GFX_SELF_THROTTLE_R	MAKE_BASE=TRUE		76 77
82 77 76	HDMI_EG_HPD	GP	HDMI_EG_HPD	MAKE_BASE=TRUE		76 77 82
77 76	GPU_GFX_OVERTEMP_R	GP	GPU_GFX_OVERTEMP_R	MAKE_BASE=TRUE		76 77
79 77 76	GPU_VCORE_VID3	GP	GPU_VCORE_VID3	MAKE_BASE=TRUE		76 77 79
77 76 73	FBVDD_ALTVO	GP	FBVDD_ALTVO	MAKE_BASE=TRUE		73 76 77
77 76	GPU_ROM_CS_L	GP	GPU_ROM_CS_L	MAKE_BASE=TRUE		76 77
77 76	TP_CLKREQ_L	GP	TP_CLKREQ_L	MAKE_BASE=TRUE		76 77
77 76	NC_GPU_GENERICA	GP	NC_GPU_GENERICA	MAKE_BASE=TRUE	NO_TEST=TRUE	76 77
77 76	NC_GPU_GENERICB	GP	NC_GPU_GENERICB	MAKE_BASE=TRUE	NO_TEST=TRUE	76 77
77 76	GPU_VCORE_PSI_L	GP	GPU_VCORE_PSI_L	MAKE_BASE=TRUE		76 77
79 77 76	GFXIMVP_DPSLP_EN_R	GP	GFXIMVP_DPSLP_EN_R	MAKE_BASE=TRUE		76 77 79
77 76	NC_DP_EXTB_CA_DET_EG	GP	NC_DP_EXTB_CA_DET_EG	MAKE_BASE=TRUE	NO_TEST=TRUE	76 77
77 76	NC_DP_EXTA_CA_DET_EG	GP	NC_DP_EXTA_CA_DET_EG	MAKE_BASE=TRUE	NO_TEST=TRUE	76 77
77 76	NC_GPU_GPIO_33	GP	NC_GPU_GPIO_33	MAKE_BASE=TRUE	NO_TEST=TRUE	76 77
82 77 76	DP_INT_EG_HPD	GP	DP_INT_EG_HPD	MAKE_BASE=TRUE		76 77 82
77 76	NC_GPU_GPIO_35	GP	NC_GPU_GPIO_35	MAKE_BASE=TRUE	NO_TEST=TRUE	76 77
82 77 76	DP_TBTSNK0_HPD_EG	GP	DP_TBTSNK0_HPD_EG	MAKE_BASE=TRUE		76 77 82

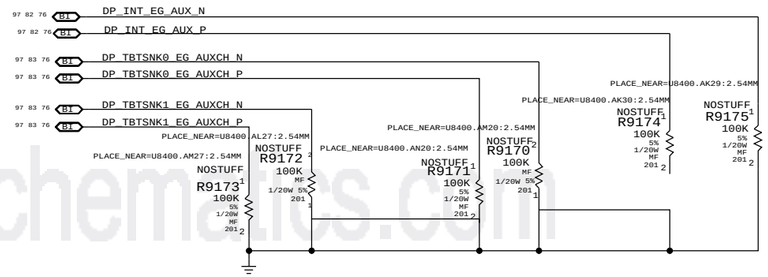
GPU ROM



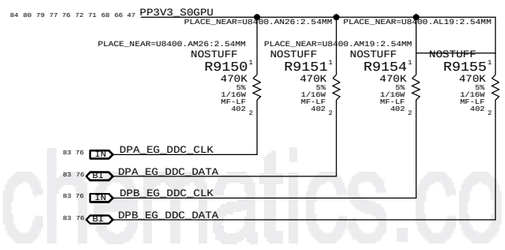
JTAG signals



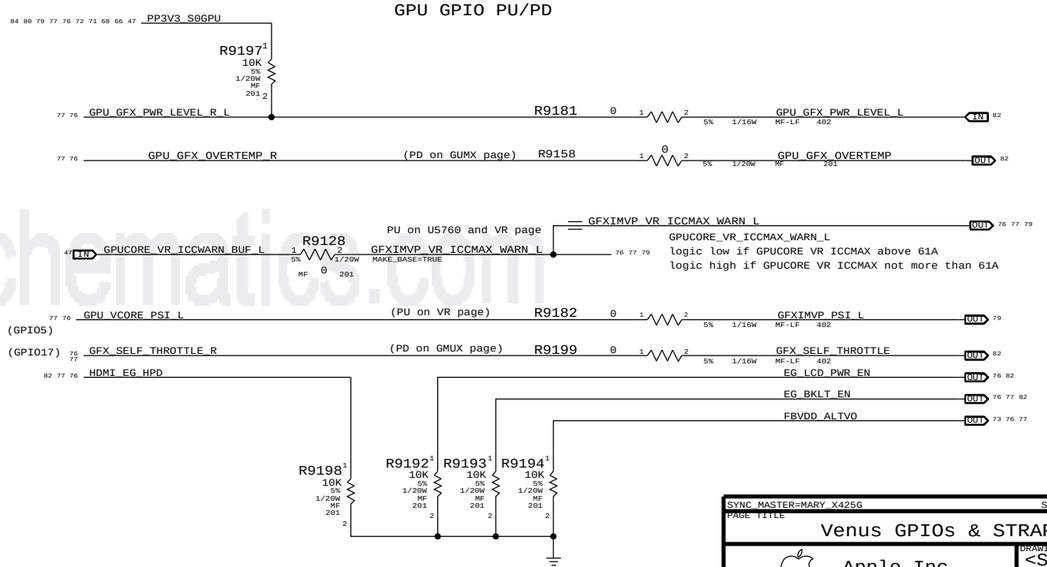
AMD AUX PD



DDC PULL UP



GPU GPIO PU/PD



SYNC_MASTER=MARY_X425G SYNC_DATE=11/07/2014

PAGE TITLE: Venus GPIOs & STRAPs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 91 OF 119
SHEET: 77 OF 97

Page Notes

Power aliases required by this page:

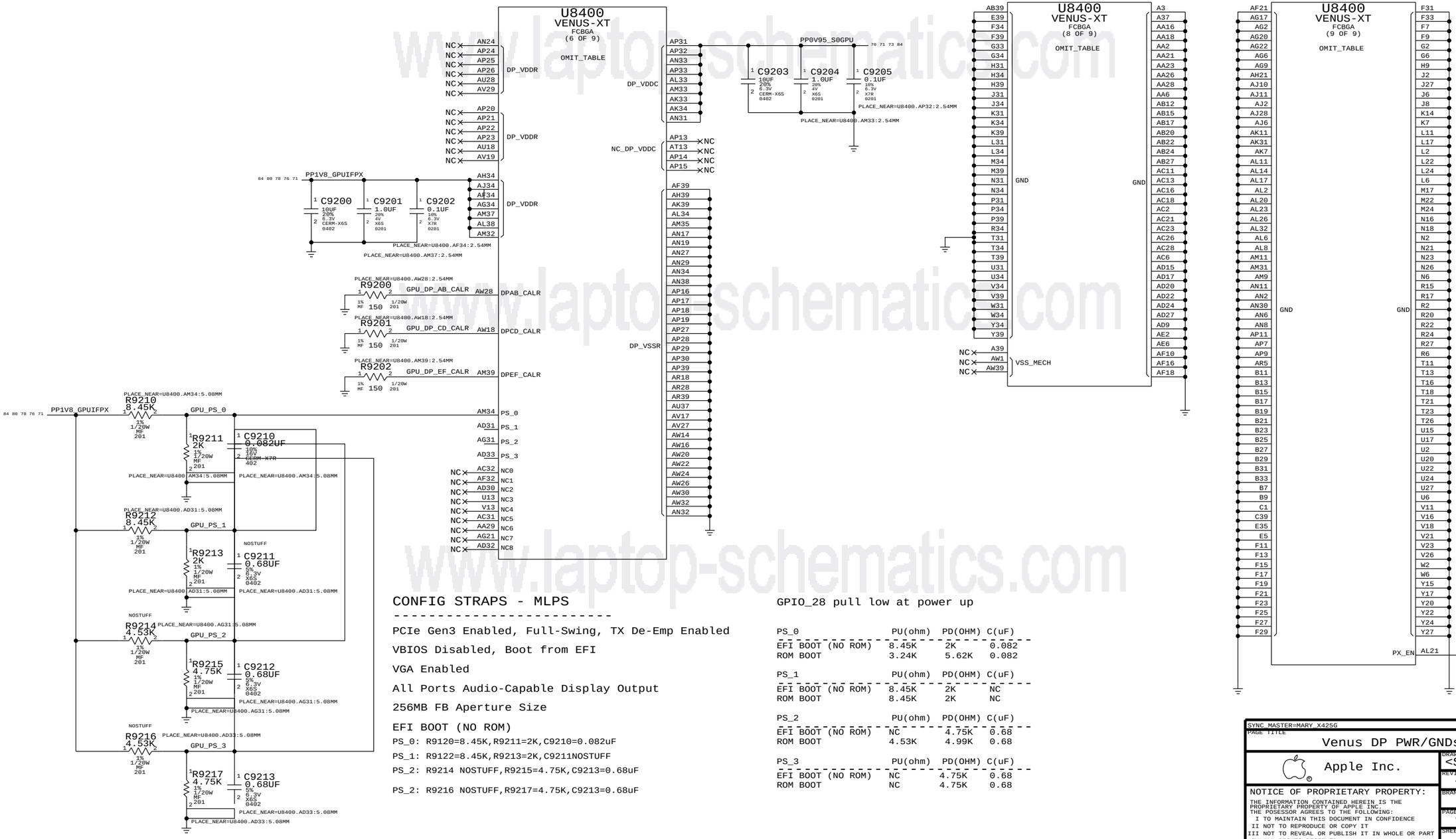
- =PP1V8_GPU_DP_AB
- =PP1V8_GPU_DP_CD
- =PP1V8_GPU_DP_EF
- =PP1V0_GPU_DP_AB
- =PP1V0_GPU_DP_CD
- =PP1V0_GPU_DP_EF

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



CONFIG STRAPS - MLPS

PCIe Gen3 Enabled, Full-Swing, TX De-Emp Enabled

VBIOS Disabled, Boot from EFI

VGA Enabled

All Ports Audio-Capable Display Output

256MB FB Aperture Size

EFI BOOT (NO ROM)

PS_0: R9120=8.45K,R9211=2K,C9210=0.082uF

PS_1: R9122=8.45K,R9213=2K,C9211NOSTUFF

PS_2: R9214 NOSTUFF,R9215=4.75K,C9213=0.68uF

PS_2: R9216 NOSTUFF,R9217=4.75K,C9213=0.68uF

GPIO_28 pull low at power up

PS_0	PU(ohm)	PD(OHM)	C(uF)
EFI BOOT (NO ROM)	8.45K	2K	0.082
ROM BOOT	3.24K	5.62K	0.082

PS_1	PU(ohm)	PD(OHM)	C(uF)
EFI BOOT (NO ROM)	8.45K	2K	NC
ROM BOOT	8.45K	2K	NC

PS_2	PU(ohm)	PD(OHM)	C(uF)
EFI BOOT (NO ROM)	NC	4.75K	0.68
ROM BOOT	4.53K	4.99K	0.68

PS_3	PU(ohm)	PD(OHM)	C(uF)
EFI BOOT (NO ROM)	NC	4.75K	0.68
ROM BOOT	NC	4.75K	0.68

SYNC_MASTER=MARY_X425G SYNC_DATE=09/22/2014

PAGE TITLE: Venus DP PWR/GNDs

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 92 OF 119

SHEET: 78 OF 97

PPVIN_S5_HS_GPU_ISNS

PP5V_S0

PLACE_NEAR=U9300.25:1mm
C9302 1UF 10% 25V X6S-CERM 0402
R9300 10 5% 1/20W MF 201
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=12.8V
PPVIN_S0_GFXIMVP_R

R9301 1 5% 1/20W MF 201
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=5V
PP5V_S0_GFXIMVP_VDD

PLACE_NEAR=U9300.16:1mm
C9301 1UF 10% 25V X6S-CERM 0402

PLACE_NEAR=U9300.17:1mm
C9300 0.22UF 10% 25V X7R 0402

(GND_GFXIMVP_AGND)

R9340 147K 1% 1/20W MF 201
R9318 30.1K 1% 1/20W MF 201

U9300 ISL62882C TQFN
VDD VCCP VIN
16 25 17

Line Width & DIDT on all DIDT nets

GFXIMVP_RBIAS	3	RBIAS 353S3679	
GFXIMVP_NTC	5	NTC	
GPUVCORE_PGOOD (OUT)	1	PGOOD	
GFXIMVP_VR_TT_L	4	VR_TT*	
	40	CLK_EN*	
GPU_VCORE_VID0	31	VID0	
GPU_VCORE_VID1	32	VID1	
GPU_VCORE_VID2	33	VID2	
GPU_VCORE_VID3	34	VID3	
GPU_VCORE_VID4	35	VID4	
GPU_VCORE_VID5	36	VID5	
GFXIMVP6_VID6	37	VID6	
GFXIMVP_PSI_L	2	PSI*	
GFXIMVP_DPSLP_EN	39	DPRSLPVR	
GPUVCORE_EN (IN)	38	VR_ON	
GFXIMVP_VW	6	VW	
GFXIMVP_COMP	7	COMP	
GFXIMVP_FB2	9	FB2	
GFXIMVP_FB	8	FB	
GPUVCORE_SENSE_P	12	VSEN	
GPUVCORE_SENSE_N	13	RTN	
GFXIMVP6_IMON (OUT)	18	IMON	
	41	THRM PAD	
	10	ISEN2	
	19	BOOT1	
	20	UGATE1	
	21	PHASE1	
	23	LGATE1A	
	24	LGATE1B	
	22	VSSP1	
	11	ISEN1	
	15	ISUM+	
	14	ISUM-	
	30	BOOT2	
	29	UGATE2	
	28	PHASE2	
	26	LGATE2	
	27	VSSP2	

GFXIMVP_BOOT2 GATE_NODE=TRUE
GFXIMVP_UGATE2 SWITCH_NODE=TRUE
GFXIMVP_PHASE2
GFXIMVP_LGATE2 GATE_NODE=TRUE
GFXIMVP_VSSP2 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
GFXIMVP_ISEN2
GFXIMVP_BOOT1 GATE_NODE=TRUE
GFXIMVP_UGATE1 SWITCH_NODE=TRUE
GFXIMVP_PHASE1 GATE_NODE=TRUE
GFXIMVP_LGATE1 MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V
NC
GFXIMVP_VSSP1
GFXIMVP_ISEN1
GFXIMVP_ISUMP
GFXIMVP_ISUMN_R

C9316 560PF 10% 16V X7R-CERM 0201 GFXIMVP_COMP_R
C9317 100PF 5% 50V C0G 0201
R9313 249K 1% 1/20W MF 201
R9314 5.11K 1% 1/20W MF 201
C9319 1000PF 10% 16V X7R-1 0201
NOSTUFF C9318 22PF 5% 50V NP0-C0G-CERM 0201
R9316 301 1% 1/20W MF 201 GFXIMVP_FB_SNS_R
R9315 3.09K 1% 1/20W MF 201
C9340 470PF 10% 16V X5R-X7R-CERM 0201
NO_XNET_CONNECTION=TRUE
NO_XNET_CONNECTION=TRUE

PLACE_NEAR=U9300.37:5mm
R9319 10K 5% 1/20W MF 201

XW9315 VSNS_GPU_VDDC_P
XW9314 VSNS_GPU_VDDC_N
NOSTUFF R9317 49.9 1% 1/20W MF 201 GFXIMVP_FB_GND_R
NOSTUFF C9341 5600PF 10% 10V CERM 201

C9315 1000PF 10% 16V X7R-1 0201 NO_XNET_CONNECTION=TRUE
C9314 1000PF 10% 16V X7R-1 0201 NO_XNET_CONNECTION=TRUE
R9312 10K 1% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
C9313 0.1UF 10% 0.3V X6S 0201 NO_XNET_CONNECTION=TRUE

GND_GFXIMVP_AGND
MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

XW9300 SM PLACE_NEAR=U9300.41:1mm

NOSTUFF C9312 0.1UF 10% 6.3V X6S 0201
R9310 1.54K 1% 1/20W MF 201
NOSTUFF R9311 1.15K 1% 1/20W MF 201
C9310 5600PF 10% 10V CERM 201
C9311 0.1UF 10% 6.3V X6S 0201
GFXIMVP_ISUMP_C
GFXIMVP_ISUMN

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM DIDT=TRUE
GFXIMVP_BOOT2_R
C9330 0.22UF 10% 16V CERM 402
R9330 0 5% 1/10W MF-LF 603

Q9330 IRF6802SDTRPBF DIRECTFET-SA
CRITICAL L9330 0.2UH-20%-28A-0.0011OHM MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.05V PILA63T-SM
NCNC
Q9331 649135PBF DIRECTFET_S3C 376S1011
PLACE_NEAR=Q9331.3:1mm XW9330 SM

R9398 0.00075 1% 1W MF 0612-1
PPVCORE_S0_GFX_PH2
GFXIMVP_ISNS2_P
NO_XNET_CONNECTION
GFXIMVP_ISNS2_N
R9331 10K 1% 1/20W MF 201
R9333 1K 1% 1/20W MF 201
R9334 1.00 1% 1/20W MF-LF 0201
GFXIMVP_ISUMN
GFXIMVP_ISUMP
R9332 10K 1% 1/20W MF 201
C9331 0.22UF 20% 6.3V X6S-CERM 0201
GFXIMVP_ISNS1_N

~30.5A max per phase
PPVCORE_GPU
CRITICAL C9361 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9362 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9363 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9364 330UF-6MOHM 20% 2.0V POLY-TANT D15T-ECGLT-COMBO

CRITICAL C9325 33UF 20% 16V POLY-TANT CASED12-SM
CRITICAL C9320 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C9321 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C9322 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C9326 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C9329 33UF 20% 16V POLY-TANT CASED12-SM
CRITICAL C9332 12PF 5% 25V NP0-C0G 0201
CRITICAL C9333 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9328 2.2UF 20% 6.3V X6S-CERM 0402
C9327 2.2UF 20% 6.3V X6S-CERM 0402
C9323 2.2UF 20% 6.3V X6S-CERM 0402
C9324 2.2UF 20% 6.3V X6S-CERM 0402

MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM DIDT=TRUE
GFXIMVP_BOOT1_R
C9365 0.22UF 10% 16V CERM 402
R9360 0 5% 1/10W MF-LF 603

Q9330 IRF6802SDTRPBF DIRECTFET-SA
CRITICAL L9360 0.2UH-20%-28A-0.0011OHM MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.05V PILA63T-SM
NCNC
Q9361 649135PBF DIRECTFET_S3C 376S1011
PLACE_NEAR=Q9361.3:1mm XW9331 SM

R9399 0.00075 1% 1W MF 0612-1
PPVCORE_S0_GFX_PH1
GFXIMVP_ISNS1_P
NO_XNET_CONNECTION
GFXIMVP_ISNS1_N
R9361 10K 1% 1/20W MF 201
R9363 1K 1% 1/20W MF 201
R9364 1.00 1% 1/20W MF-LF 0201
GFXIMVP_ISUMN
GFXIMVP_ISUMP
C9366 0.22UF 20% 6.3V X6S-CERM 0201
R9362 10K 1% 1/20W MF 201
GFXIMVP_ISNS2_N

VIMON = Imon* R9312
Imon = 3* Idroop. Idroop = 2*Rsns*Io/(N*Ri)

VIMON = 1.46104uA/A * Io * 14.6104mV/A*Io
1A will generate 14.6104mV and 891.23mV for 61A

GPU_VCORE_VID0 GPU_VCORE_VID1 GPU_VCORE_VID2 GPU_VCORE_VID3 GPU_VCORE_VID4 GPU_VCORE_VID5
MAKE_BASE=TRUE

PP3V3_S0GPU

NOSTUFF R9387 2.2K 5% 1/20W MF 201
NOSTUFF R9384 2.2K 5% 1/20W MF 201
R9382 2.2K 5% 1/20W MF 201
NOSTUFF R9395 2.2K 5% 1/20W MF 201
R9391 2.2K 5% 1/20W MF 201
R9378 2.2K 5% 1/20W MF 201

Default Vcore set to 0.85V.
0.85V is set by setting VID0-VID5 as 001011

R9388 2.2K 5% 1/20W MF 201
R9385 2.2K 5% 1/20W MF 201
NOSTUFF R9383 2.2K 5% 1/20W MF 201
R9396 2.2K 5% 1/20W MF 201
NOSTUFF R9392 2.2K 5% 1/20W MF 201
NOSTUFF R9379 2.2K 5% 1/20W MF 201

Stuff option for GPIO control
R9375 = GFXIMVP_VR_TT_L GPIO13
R9377 = DPSLP Control GPIO 30

R9375 0 5% 1/20W MF 201 GFXIMVP_VR_ICCMAX_WARN GFXIMVP_VR_TT_L
NOSTUFF R9377 0 5% 1/20W MF 201 GFXIMVP_DPSLP_EN_R GFXIMVP_DPSLP_EN

PP3V3_S0GPU
R9370 10K 1% 1/20W MF 201
R9371 10K 5% 1/20W MF 201
NOSTUFF R9374 100K 5% 1/20W MF 201
GFXIMVP_VR_TT_L
GFXIMVP_PSI_L
GFXIMVP_DPSLP_EN
NOSTUFF R9372 100K 5% 1/20W MF 201
R9373 100K 5% 1/20W MF 201

Do not config
PSI_L = HIGH & DPSLP_EN = HIGH

SYNC_MASTER=ADITYA_X425G SYNC_DATE=09/15/2014
PAGE TITLE: GFX IMVP VCore Regulator
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 93 OF 119
SHEET: 79 OF 97

GPU VDDCI REGULATOR

VOUT = 0.9V
7A MAX OUTPUT
F = 500 KHZ

VSNS_GPU_VDDI_P
VSNS_GPU_VDDI_N
GPU_VDDCI_SENSE_XW_N
GPU_VDDCI_SENSE_XW_P
XW9470 SM PLACE_NEAR=U8400.AH28:5mm
XW9471 SM PLACE_NEAR=U8400.AG28:5mm
NO_XNET_CONNECTION=TRUE

PP5V_S0
PP5V_VDDCI_VCC
PP5V_VDDCI_PVCC
R9405 10 5% 1/20W MF 201
R9406 2.2 5% 1/20W MF 201
VOLTAGE=5V MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.4 MM
C9403 1UF 10% 10V CERM 0402
C9404 2.2UF 10% 6.3V X6S-CERM 0402
AGND_GPU_VDDCI

REG_BOOT_GPU_VDDCI_RC
R9407 2.2 5% 1/16W MF-LF 402
C9405 0.1UF 10% 16V X7R-CERM 0402

PPVIN_S5_HS_GPU_ISNS
CRITICAL C9402 68UF 20% 16V POLY-TANT CASE-D2E-SM
CRITICAL C9406 12PF 5% 50V NP0-C0G 0201
CRITICAL C9407 3.0PF +/-0.1PF 25V NP0-C0G 0201
EMC C9409 2.2UF 20% 6.3V X6S-CERM 0402
EMC C9410 2.2UF 20% 6.3V X6S-CERM 0402
C9408 1000PF 5% 25V CERM 0402

U9450 ISL95870AH UTQFN
VCC PVCC
PVDDCI_GPU_EN
REG_GPU_VDDCI_FB
REG_GPU_VDDCI_SREF
REG_GPU_VDDCI_VO
REG_GPU_VDDCI_OCSET
PVDDCI_PGOOD
REG_GPU_VDDCI_RTN
REG_GPU_VDDCI_FSEL
REG_GPU_VDDCI_SET0
REG_GPU_VDDCI_SET1
VID0
VID1
GND PGND
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm
DIDT=TRUE

APN376S1005
CRITICAL Q9410 CSD58873Q3D Q3D
REG_UGATE_VDDCI_R
REG_UGATE_VDDCI
REG_PHASE_GPU_VDDCI
REG_LGATE_GPU_VDDCI
R9408 1 5% 1/16W MF-LF 402
DIDT=TRUE GATE_NODE=TRUE MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm
DIDT=TRUE SWITCH_NODE=TRUE MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm

APN152S1822 CRITICAL L9410 1.0UH-20%-15A-0.00660HM PIME063T-SM
VR_PHASE_GPU_VDDCI
VRVDDCI_R
CRITICAL R9400 0.003 1% 1W CYN 0612
PPVDDCI_S0_ISENSE
NOSTUFF C9411 0.001UF 10% 50V X7R-CERM 0402
REG_SNUBBER_GPU_VDDCI
NOSTUFF R9409 2.2 5% 1/10W MF-LF 603

Note:
Regulator requires a minimum load to prevent noise in the audio frequencies

C9413 1000PF 5% 25V CERM 0402
R9412 200 5% 1/16W MF-LF 402
CRITICAL C9417 10UF 20% 10V X6S-CERM 0603
CRITICAL C9418 10UF 20% 10V X6S-CERM 0603
CRITICAL C9414 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9415 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9416 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9419 270UF 20% 2V TANT CASE-B2-SM
CRITICAL C9431 270UF 20% 2V TANT CASE-B2-SM

<Ra> R9470 2.8K 0.1% 1/20W MF 0201
<Ra> R9471 2.8K 0.1% 1/20W MF 0201
<Rb> R9472 4.02K 0.1% 1/20W MF 0201
<Rb> R9473 4.02K 0.1% 1/20W MF 0201
C9470 10PF 5% 50V NP0-C0G 0201
C9485 10PF 5% 50V NP0-C0G 0201
C9490 0.033UF 10% 16V X5R 402
R9474 17.4K 0.1% 1/20W MF 0201
R9475 34.8K 0.1% 1/20W MF 0201-1
NOSTUFF R9476 0 5% 1/20W MF 0201
R9477 0 5% 1/20W MF 0201
R9478 249K 0.1% 1/20W MF 0201
REG_GPU_VDDCI_SET1_R
XW9473 SM PLACE_NEAR=U9450.3:1mm
AGND_GPU_VDDCI
MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm VOLTAGE=0V

Vout = 0.5 * (1 + Ra / Rb)

PP3V3_S0GPU
R9484 0 5% 1/20W MF 0201
NOSTUFF R9485 0 5% 1/20W MF 0201
R9483 10K 5% 1/20W MF 201
R9481 10K 5% 1/20W MF 201
GFX_VDDCI_ALTV
GFX_VDDCI_ALTV0
GFX_VDDCI_ALTV1

VID1	VID0	GPU VDDCI
1	1	0.85V
1	0	0.9V --> DEFAULT

REG_GPU_VDDCI_OCSET_R
REG_GPU_VDDCI_VO_R
XW9480 SM
XW9481 SM
VDDCIS0_CS_P
VDDCIS0_CS_N
R9410 3.92K 1% 1/20W MF 201
C9412 0.0022UF 10% 50V CERM 402
PLACE_NEAR=R9410.2:3mm
R9411 3.92K 1% 1/20W MF 201
REG_GPU_VDDCI_OCSET
REG_GPU_VDDCI_VO

1.8V S0 GPU Regulator

PPVIN_S5_HS_GPU_ISNS
CRITICAL C9432 12PF 5% 50V NP0-C0G 0201
CRITICAL C9433 3.0PF +/-0.1PF 25V NP0-C0G 0201
CRITICAL C9420 33UF 20% 16V POLY-TANT CASED12-SM
CRITICAL C9421 2.2UF 20% 25V X6S-CERM 0402
CRITICAL C9422 2.2UF 20% 25V X6S-CERM 0402

U9400 TPS62130ARGT QFN
CRITICAL 353S4283
AVIN DEF EN FSW VOS FB SW PG SS/TR PVIN PGND AGND THRM PAD
R9420 10 5% 1/20W MF 201
PPVIN_S0GPU_1V8_RC
P1V8_S0GPU_EN
REG_VOS_PVDDR
REG_FB_PVDDR
P1V8GPU_PGOOD
REG_SSTR_PVDDR
C9423 0.1UF 10% 16V X5R 0402
C9424 4700PF 10% 16V X7R 201
AGND_PVDDR
MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm VOLTAGE=0V
MIN_NECK_WIDTH=0.2 mm MIN_LINE_WIDTH=0.6 mm VOLTAGE=8.4V

APN152S00137 CRITICAL L9400 1.5UH-20%-2.61A-0.0680HM PIFE32251B-SM
REG_PHASE_PVDDR
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM SWITCH_NODE=TRUE DIDT=TRUE
PP1V8_GPUIFPX
R9421 10 5% 1/20W MF 201
R9422 105K 0.1% 1/20W MF 0201-1
<Ra>
R9423 82.5K 0.1% 1/20W MF 0201-1
<Rb>
XW9420 SM
Vout = 0.8V * (Ra + Rb) / Rb

Output voltage: 1.818 V
Max peak current: 1.5A
Switching freq: 1250 kHz

CRITICAL C9425 47UF 20% 2V POLY-TANT 0805
CRITICAL C9426 47UF 20% 2V POLY-TANT 0805
CRITICAL C9427 47UF 20% 2V POLY-TANT 0805
CRITICAL C9428 47UF 20% 2V POLY-TANT 0805
CRITICAL C9429 47UF 20% 2V POLY-TANT 0805
CRITICAL C9430 47UF 20% 2V POLY-TANT 0805

SYNC_MASTER=ADITYA X425G SYNC_DATE=09/16/2014
PAGE TITLE: VREG GPU VDDCI
Apple Inc.
DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 94 OF 119
SHEET: 80 OF 97

Wire-to-Board (Micro-coax) Connector

CRITICAL

J9500
20525-130E-01
F-RT-SM

NO_XNET_CONNECTION=TRUE
BP9501
BEAD-PROBE
SM
TP

NO_XNET_CONNECTION=TRUE
BP9502
BEAD-PROBE
SM
TP

NO_XNET_CONNECTION=TRUE
BP9505
BEAD-PROBE
SM
TP

NO_XNET_CONNECTION=TRUE
BP9506
BEAD-PROBE
SM
TP

NO_XNET_CONNECTION=TRUE
BP9503
BEAD-PROBE
SM
TP

NO_XNET_CONNECTION=TRUE
BP9504
BEAD-PROBE
SM
TP

90 13	IN	USB3_EXTB_R2D_C_P	C9501 0.1UF 10% 16V X5R-CERM 0201	GND_VOID=TRUE	90 86 13 BI USB_EXTB_P
90 13	IN	USB3_EXTB_R2D_C_N	C9502 0.1UF 10% 16V X5R-CERM 0201	GND_VOID=TRUE	90 86 13 BI USB_EXTB_N
				GND_VOID=TRUE	90 86 USB3_EXTB_R2D_P
				GND_VOID=TRUE	90 86 USB3_EXTB_R2D_N
90 86 13	OUT	USB3_EXTB_D2R_P		GND_VOID=TRUE	
90 86 13	OUT	USB3_EXTB_D2R_N		GND_VOID=TRUE	
				GND_VOID=TRUE	97 86 76 IN HDMI_EG_DATA_P<0>
				GND_VOID=TRUE	97 86 76 IN HDMI_EG_DATA_N<0>
				GND_VOID=TRUE	97 86 76 IN HDMI_EG_DATA_P<1>
				GND_VOID=TRUE	97 86 76 IN HDMI_EG_DATA_N<1>
				GND_VOID=TRUE	97 86 76 IN HDMI_EG_DATA_P<2>
				GND_VOID=TRUE	97 86 76 IN HDMI_EG_DATA_N<2>
					97 86 76 IN HDMI_EG_CLK_P
					97 86 76 IN HDMI_EG_CLK_N
				GND_VOID=TRUE	91 86 20 13 OUT USB3_SD_D2R_P
				GND_VOID=TRUE	91 86 20 13 OUT USB3_SD_D2R_N
				GND_VOID=TRUE	91 86 20 13 IN USB3_SD_R2D_C_P
				GND_VOID=TRUE	91 86 20 13 IN USB3_SD_R2D_C_N

Board-to-Board (Flex) Connector

CRITICAL

J9510
DF40HC-3.0-40DS-0.4V-51
F-ST-SM

86 84 81 69 67 66 61 51 38 37	PP5V_S4		PP5V_S4		37 38 51 61 66 67 69 81 84 86
84 82 81 66 46 45 43 21 20 13 86	PP3V3_S3		PP3V3_S3		13 20 21 43 45 46 66 81 82 84 86
84 67 64 52 19 17 15 13 12 11 86	PP1V5_S0				
86 20	OUT RIO_SDCONN_STATE_CHANGE_L		HDMI_EG_DDC_DATA	BI	76
86 18 13	IN SD_PWR_EN		HDMI_EG_DDC_CLK	IN	76
86 18	OUT USB_EXTB_OC_L		PM_SLP_S4_L	IN	12 21 33 37 40 67 86
86 82 20	OUT HDMI_HPD		PM_SLP_S3_BUF_L	IN	51 66 67 82 86
			SMBUS_PCH_DATA	BI	13 18 43 85 86 91
			SMBUS_PCH_CLK	IN	13 18 43 85 86 91
			PP3V3_S4		20 33 38 41 42 45 46 65 66 67 84 85 86

C9510 0.1uF 20% 10V CERM 402

C9511 0.1uF 20% 10V CERM 402

C9512 12PF 5% NPO-C0G 0201 25V
PLACE_NEAR=J9510.1:3mm

C9513 12PF 5% NPO-C0G 0201 25V
PLACE_NEAR=J9510.21:3mm

C9512&C9513 FOR DESENSE IMPROVEMENT
LOCATION DEPENDS ON DESENSE TEAM

516S00052

518S0829

SYNC_MASTER=CLEAN_MAXWELL SYNC_DATE=07/01/2014

PAGE TITLE
RIO Connectors

Apple Inc.

DRAWING NUMBER <SCH_NUM> SIZE D
REVISION <E4LABEL>
BRANCH <BRANCH>
PAGE 95 OF 119
SHEET 81 OF 97

U9600 R4F2113NLG TLP-145V SYM 1 OF 3

OMIT_TABLE

TP_DPMUX_UC_P10	B12	P10/WUE0*	
TP_DPMUX_UC_P11	A13	P11/WUE1*	
TP_DPMUX_UC_P12	A12	P12/WUE2*	
TP_DPMUX_UC_P13	B13	P13/WUE3*	
TP_DPMUX_UC_P14	D11	P14/WUE4*	
TP_DPMUX_UC_P15	C13	P15/WUE5*	
TP_DPMUX_UC_P16	C12	P16/WUE6*	
TP_DPMUX_UC_P17	D10	P17/WUE7*	
EG_RAIL1_EN	D13	P20	
P0V95R1V8GPU_R_EN	E11	P21	
EG_RAIL3_EN	D12	P22	
EG_RAIL4_EN	F11	P23	
EG_RAIL5_EN	E13	P24	
PEG_CLKREQ_L	E12	P25	
EG_RESET_L	F13	P26	
TP_FB_CLAMP	E10	P27	
LPC_AD<0>	A9	P30/LAD0	
LPC_AD<1>	D9	P31/LAD1	
LPC_AD<2>	C8	P32/LAD2	
LPC_AD<3>	B7	P33/LAD3	
LPC_FRAME_L	A8	P34/LFRAM*	
DPMUX_LRESET_L	D8	P35/LRESET*	
LPC_CLK33M_DPMUX_UC	D7	P36/LCLK	
TP_DPMUX_UC_P37	D6	P37/SERIRQ	
TP_DPMUX_UC_P40	D4	P40/TMI0/TCMCYI0	
TP_DPMUX_UC_P41	A5	P41/TMO0/TCMCKI0/TCMMCI0	
TP_DPMUX_UC_P42	B4	P42/TCMCYI1	
LCD_FSS	A1	P43/TMI1/TCMCKI1/TCMMCI1	
LCD_MUX_SEL	C2	P44/TMO1/PWMU2B/TCMCYI2	
TP_DPMUX_UC_P45	B2	P45/PWMU3B/TCMCKI2/TCMMCI2	
TP_DPMUX_UC_P46	C1	P46/PWMU4B	
TP_DPMUX_UC_P47	C3	P47/PWMU5B	
DPMUX_UC_TX	G2	P50/FTXD	
DPMUX_UC_RX	F3	P51/FRXD	
TP_DPMUX_UC_P52	E4	P52/SCL0	

P60/KIN0*	L13	DP_EXTA_MUX_EN	OUT
P61/KIN1*	K12	DP_EXTA_MUX_SEL_EG	OUT
P62/KIN2*	K11	TP_DPMUX_UC_P62	
P63/KIN3*	J12	GMUX_SLP_S3_BUF_L	
P64/KIN4*	K13	DP_EXTB_MUX_EN	OUT
P65/KIN5*	J10	DP_EXTB_MUX_SEL_EG	OUT
P66/KIN6*	J11	TP_DPMUX_UC_P66	
P67/IRQ7*/KIN7*	H12	TP_DPMUX_UC_P67	
P70/AN0	N10	NC	
P71/AN1	M11	NC	
P72/AN2	L10	NC	
P73/AN3	N11	NC	
P74/AN4	N12	NC	
P75/AN5	M13	NC	
P76/AN6	N13	NC	
P77/AN7	L12	NC	
P80/PME*	A7	TP_DPMUX_UC_P80	
P81/GA20	B6	TP_DPMUX_UC_P81	
P82/CLKRUN*	C7	TP_DPMUX_UC_P82	
P83/LPCPD*	D5	TP_DPMUX_UC_P83	
P84/IRQ3*/TXD1	A6	DPMUX_UC_TX	OUT
P85/IRQ4*/RXD1	B5	DPMUX_UC_RX	IN
P86/IRQ5*/SCK1	C6	TP_LCD_IRQ	
P90/IRQ2*	J4	GPU_GFX_OVERTEMP	IN
P91/IRQ1*	G3	TP_DP_TBTPB_HPD_BUF	
P92/IRQ0*	H2	DP_TBTSNK0_HPD	IN
P93/IRQ12*	G1	DP_TBTSNK1_HPD	IN
P94/IRQ13*	H4	GFX_SELF_THROTTLE	IN
P95/IRQ14*	G4	SMC_GFX_PWR_LEVEL_L	IN
P96/EXCL	F4	TP_DPMUX_UC_P96	
P97/SDA0/IRQ15*	F1	TBT_DDC_XBAR_EN_L	IN

U9600 R4F2113NLG TLP-145V SYM 2 OF 3

OMIT_TABLE

I2C_DPMUX_UC_SDA	N3	PA0/KIN8*/SDA1	
I2C_DPMUX_UC_SCL	N1	PA1/KIN9*/SCL1	
DPMUX_UC_IRQ	M3	PA2/KIN10*/PS2AC	
	M2	PA3/KIN11*/PS2AD	NC
	N2	PA4/KIN12*/PS2BC	NC
	L1	PA5/KIN13*/PS2BD	NC
SMC_GFX_OVERTEMP	K3	PA6/KIN14*/PS2CC	
TP_FB_CLAMP_TOGGLE_REQ_L	L2	PA7/KIN15*/PS2CD	
TP_DPA_EG_HPD	B8	PB0/LSMI*	
TP_DPB_EG_HPD	C9	PB1/LSCI	
DP_TBTSNK0_HPD_EG	B9	PB2/RI*/PWMU0B	
DP_TBTSNK1_HPD_EG	A10	PB3/DCD*/PWMU1B	
SMC_GFX_SELF_THROTTLE	C10	PB4/DSR*/FSIDO	
GPU_GFX_PWR_LEVEL_L	B10	PB5/DTR*/FSIDI	
HDMI_EG_HPD	C11	PB6/CTS*/FSICK	
TP_INT_EG_HPD	A11	PB7/RTS*/FSISS	
LCD_PWR_EN	G11	PC0/TIOCA0/WUE8*	
LCD_BKLT_EN	G13	PC1/TIOCB0/WUE9*	
TP_DPMUX_UC_PC2	F12	PC2/TIOCC0/TCLKA/WUE10*	
TP_DPMUX_UC_PC3	H13	PC3/TIOCD0/TCLKB/WUE11*	
LCD_MUX_EN	G10	PC4/TIOCA1/WUE12*	
TP_LCD_MUX_REQ	G12	PC5/TIOCB1/TCLKC/WUE13*	
LCD_BKLT_PWM	H11	PC6/TIOCA2/WUE14*	
DP_DDC_MUX_CROSSBAR_L	J13	PC7/TIOCB2/TCLKD/WUE15*	
TP_DPA_IG_HPD	M10	PD0/AN8	
TP_DPB_IG_HPD	N9	PD1/AN9	
DP_TBTSNK0_HPD_IG	K10	PD2/AN10	
DP_TBTSNK1_HPD_IG	L8	PD3/AN11	
TP_DP_EXTA_CA_DET_IG	M9	PD4/SSO	
TP_DP_EXTB_CA_DET_IG	N8	PD5/SSI	
TP_HDMI_IG_HPD	K9	PD6/SSCK	
DP_INT_IG_HPD	L7	PD7/SCS	

PE0/EXEXCL	K1	DPMUX_UC_CLK32K	
PE1/ETCK	J3	DPMUX_UC_TCK	
PE2/ETDI	K2	DPMUX_UC_TDI	
PE3/ETDO	J1	DPMUX_UC_TDO	
PE4/ETMS	K4	DPMUX_UC_TMS	
PE5/ETRST*	H3	DPMUX_UC_TRST_L	
PF0/IRQ8*/PWMU0A	K5	EG_LCD_PWR_EN	IN
PF1/IRQ9*/PWMU1A	N5	EG_BKLT_EN	IN
PF2/IRQ10*/TMOY	M6	PM_ALL_GPU_PGOOD	IN
PF3/IRQ11*/TMOX	L5	P0V95_S0GPU_PGOOD	IN
PF4/PWMU2A/EXDSR	M5	PVDDCI_PGOOD	IN
PF5/PWMU3A/EXDTR	N4	GPUVCORE_PGOOD	IN
PF6/PWMU4A/EXCTS	L4	P1V8GPU_PGOOD	IN
PF7/PWMU5A/EXRTS	M4	P3V3_S0GPU_PGOOD	IN
PG0/EXIRQ8*/TMIX/SDAA	M8	NC_I2C_DPMUX_A_SDA	BI
PG1/EXIRQ9*/TMIY/SCLA	N7	NC_I2C_DPMUX_A_SCL	OUT
PG2/EXIRQ10*/SDAB	K8	NC	
PG3/EXIRQ11*/SCLB	K7	NC	
PG4/EXIRQ12*/SDAC	K6	NC	
PG5/EXIRQ13*/SCLC	N6	DPMUX_LRESET_L	IN
PG6/EXIRQ14*/SDAD	M7	HDMI_HPD	IN
PG7/EXIRQ15*/SCLD	L6	LCD_HPD	IN
PH0/IRQ6*	E2	EDP_IG_PANEL_PWR	IN
PH1/EXIRQ7*	F2	EDP_IG_BKL_ON	IN
PECI	A4	DPMUX_UC_PECI	
PEVREF	B3	DPMUX_UC_PEVREF	

U9600 R4F2113NLG TLP-145V SYM 3 OF 3

OMIT_TABLE

TP_DPMUX_UC_XTAL	A3	XTAL	
DPMUX_UC_EXTAL	A2	EXTAL	
DPMUX_UC_RESET_L	D3	RES*	
DPMUX_UC_MD1	D1	MD1	
DPMUX_UC_MD2	H1	MD2	
DPMUX_UC_NMI	E3	NMI	
	E5	NC	NC
	C4	MDCKN	

	M12	AVCC	
	B1	VCC	
	M1	VCC	
	H10	VCC	
	E1	VCL	
	L11	AVREF	
	J2	VBAT	
	D2	VSS	
	L3	VSS	
	F10	VSS	
	C5	VSS	
	B11	VSS	
	L9	AVSS	

U9650 CBTL06142EEE TFBGA CRITICAL

DP_INT_IG_ML_P<0>	B4	DIN1_0+	
DP_INT_IG_ML_N<0>	A4	DIN1_0-	
DP_INT_IG_ML_P<1>	B5	DIN1_1+	
DP_INT_IG_ML_N<1>	A5	DIN1_1-	
DP_INT_IG_ML_P<2>	B6	DIN1_2+	
DP_INT_IG_ML_N<2>	A6	DIN1_2-	
DP_INT_IG_ML_P<3>	A8	DIN1_3+	
DP_INT_IG_ML_N<3>	A9	DIN1_3-	
DP_INT_IG_AUX_P	H9	DAUX1+	
DP_INT_IG_AUX_N	J9	DAUX1-	
	H8	DDC_CLK1	NC
	J8	DDC_DAT1	NC
	J2	HPD_1	NC
DP_INT_EG_ML_P<0>	B8	DIN2_0+	
DP_INT_EG_ML_N<0>	B9	DIN2_0-	
DP_INT_EG_ML_P<1>	D8	DIN2_1+	
DP_INT_EG_ML_N<1>	D9	DIN2_1-	
DP_INT_EG_ML_P<2>	E8	DIN2_2+	
DP_INT_EG_ML_N<2>	E9	DIN2_2-	
DP_INT_EG_ML_P<3>	F8	DIN2_3+	
DP_INT_EG_ML_N<3>	F9	DIN2_3-	
DP_INT_EG_AUX_P	H6	DAUX2+	
DP_INT_EG_AUX_N	J6	DAUX2-	
	H5	DDC_CLK2	NC
	J5	DDC_DAT2	NC
	H3	HPD_2	NC
LCD_MUX_SEL	A1	GPU_SEL	
LCD_MUX_EN	B7	XSD*	
	C2	DDC_AUX_SEL	
	B3 C8 G8 H4 H7 G2	GND	
DP_INT_ML_C_P<0>	B2	DOUT_0+	OUT
DP_INT_ML_C_N<0>	B1	DOUT_0-	OUT
DP_INT_ML_C_P<1>	D2	DOUT_1+	OUT
DP_INT_ML_C_N<1>	D1	DOUT_1-	OUT
DP_INT_ML_C_P<2>	E2	DOUT_2+	OUT
DP_INT_ML_C_N<2>	E1	DOUT_2-	OUT
DP_INT_ML_C_P<3>	F2	DOUT_3+	OUT
DP_INT_ML_C_N<3>	F1	DOUT_3-	OUT
DP_INT_AUXCH_C_P	H2	AUX+	BI
DP_INT_AUXCH_C_N	H1	AUX-	BI
DPMUX_HPD_PD	J1	HPDIN	

J9600 1909782 M-RT-SM

PP3V3_S0_DPMUX_UC_R	1	
DPMUX_UC_TX	2	
DPMUX_UC_RX	3	
DPMUX_UC_RESET_L	4	
	5	
DPMUX_UC_MD1	6	
	7	
	8	

DPMUX_DEBUG

DPMUX UC DEBUG HEADER

DP 2:1 ANALOG MUX

DPMUX UC PULL-DOWNS

DPMUX UC PULL-UPS

PU on PCH Page

CONNECT I2C TO LCD BKLT IC

PU OFFPAGE

CA_DET ISOLATION-Will delete

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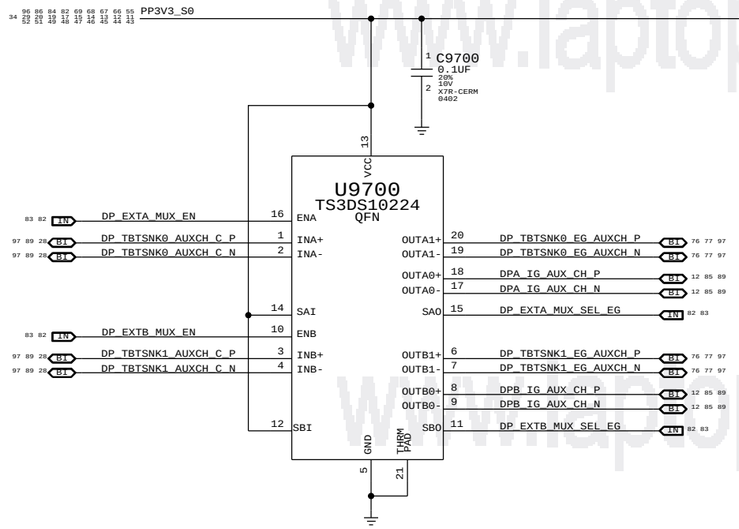
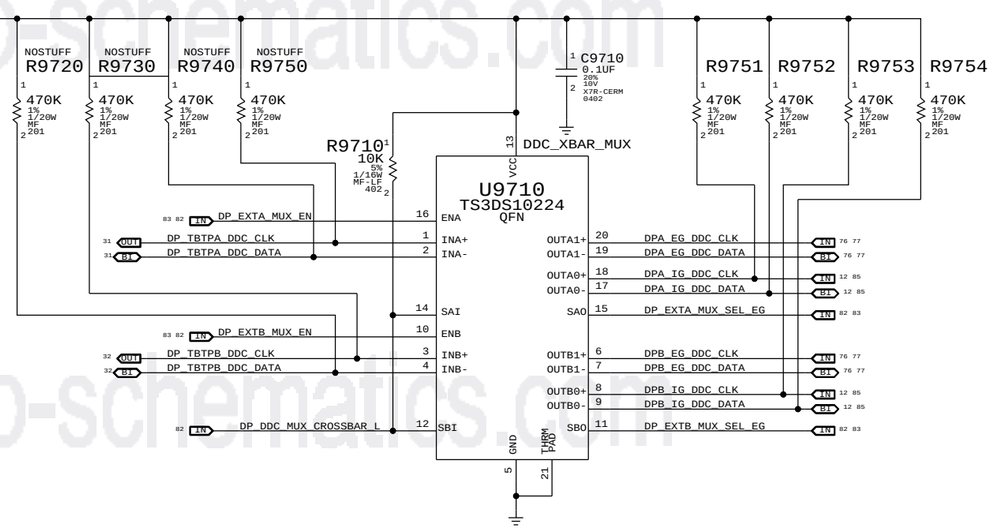
SYNC_MASTER=MARY_X425G		SYNC_DATE=09/22/2014	
PAGE TITLE	eDP Mux		
Apple Inc.		DRAWING NUMBER	<SCH_NUM>
		SIZE	D
		REVISION	<E4LABEL>
		BRANCH	<BRANCH>
		PAGE	96 OF 119
		SHEET	82 OF 97

DP A & DP B AUX MUX



DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC_MASTER=MARY_X425G SYNC_DATE=10/15/2014

PAGE TITLE: eDP Muxed Graphics Support

Apple Inc.

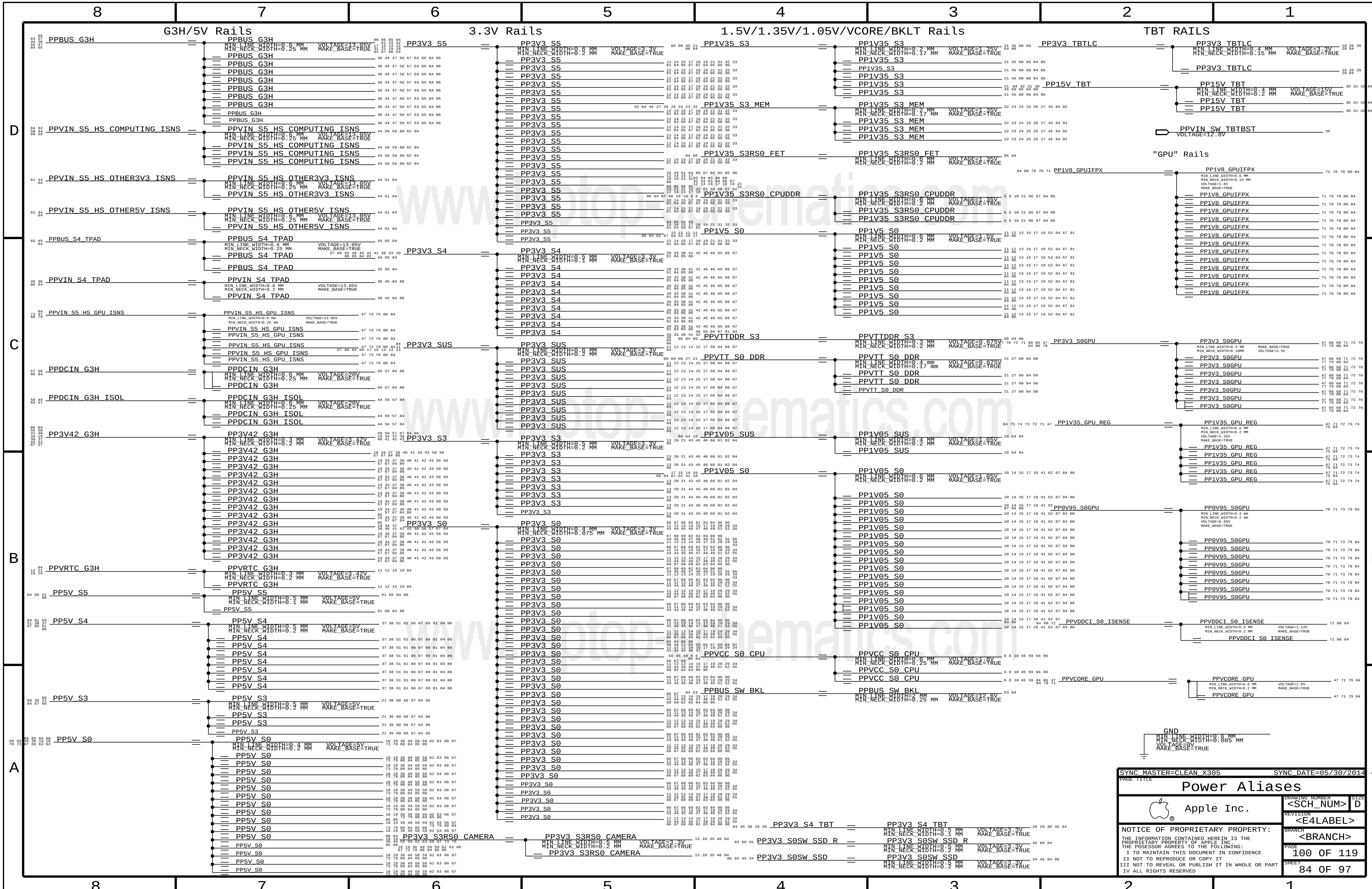
DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 97 OF 119

SHEET: 83 OF 97



Display Aliases

EDP_IG_PANEL_PWR	MAKE_BASE=TRUE	EDP_IG_PANEL_PWR	
EDP_IG_BKL_ON	MAKE_BASE=TRUE	EDP_IG_BKL_ON	
DP_INT_IG_ML_P<3..0>	MAKE_BASE=TRUE	TP_DP_IG_A_MLP<3..0>	
DP_INT_IG_ML_N<3..0>	MAKE_BASE=TRUE	TP_DP_IG_A_MLN<3..0>	
DP_INT_IG_AUX_P	MAKE_BASE=TRUE	DP_INT_IG_AUX_P	
DP_INT_IG_AUX_N	MAKE_BASE=TRUE	DP_INT_IG_AUX_N	
DPA_IG_AUX_CH_P	MAKE_BASE=TRUE	DPA_IG_AUX_CH_P	
DPA_IG_AUX_CH_N	MAKE_BASE=TRUE	DPA_IG_AUX_CH_N	
DPB_IG_AUX_CH_P	MAKE_BASE=TRUE	DPB_IG_AUX_CH_P	
DPB_IG_AUX_CH_N	MAKE_BASE=TRUE	DPB_IG_AUX_CH_N	
DPA_IG_DDC_CLK	MAKE_BASE=TRUE	DPA_IG_DDC_CLK	
DPA_IG_DDC_DATA	MAKE_BASE=TRUE	DPA_IG_DDC_DATA	
DPB_IG_DDC_CLK	MAKE_BASE=TRUE	DPB_IG_DDC_CLK	
DPB_IG_DDC_DATA	MAKE_BASE=TRUE	DPB_IG_DDC_DATA	
DP_TBTSNK0_HPD_IG	MAKE_BASE=TRUE	DP_TBTSNK0_HPD_IG	
DP_TBTSNK1_HPD_IG	MAKE_BASE=TRUE	DP_TBTSNK1_HPD_IG	
DPMUX_UC_RX	MAKE_BASE=TRUE	DPMUX_UC_RX	
DPMUX_UC_TX	MAKE_BASE=TRUE	DPMUX_UC_TX	
EG_RESET_L	MAKE_BASE=TRUE	EG_RESET_L	
PEG_CLKREQ_L	MAKE_BASE=TRUE	PEG_CLKREQ_L	
DP_AUXCH_ISOL_L	MAKE_BASE=TRUE	DP_AUXCH_ISOL_L	

LCD_FSS	MAKE_BASE=TRUE	LCD_FSS	
PEG_CLK100M_N	MAKE_BASE=TRUE	PEG_CLK100M_N	
PEG_CLK100M_P	MAKE_BASE=TRUE	PEG_CLK100M_P	
VSNS_GPU_VDDC_P	MAKE_BASE=TRUE	VSNS_GPU_VDDC_P	
VSNS_GPU_VDDI_P	MAKE_BASE=TRUE	VSNS_GPU_VDDI_P	

CPU signals

MEMVTT_EN	MAKE_BASE=TRUE	MEMVTT_EN

J9510 RIO FLEX CONN

SMBUS_PCH_DATA		SMBUS_PCH_DATA
SMBUS_PCH_CLK		SMBUS_PCH_CLK

SSD Signals Through PEG

PCIE_SSD_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<15..12>
PCIE_SSD_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<15..12>
PCIE_SSD_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<15..12>
PCIE_SSD_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<15..12>

Thunderbolt Signals Through PEG

PCIE_TBT_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<11..8>
PCIE_TBT_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<11..8>
PCIE_TBT_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<11..8>
PCIE_TBT_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<11..8>

GUP PEG Lanes

PEG_D2R_P<7..0>	MAKE_BASE=TRUE	=PEG_D2R_P<7..0>
PEG_D2R_N<7..0>	MAKE_BASE=TRUE	=PEG_D2R_N<7..0>
PEG_R2D_C_P<7..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<7..0>
PEG_R2D_C_N<7..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<7..0>

Unused PCH PCIE Lanes

	MAKE_BASE	NO_TEST	
NC_PCIE_SSD_D2RP<3..0>	TRUE	TRUE	=PCIE_SSD_D2R_P<3..0>
NC_PCIE_SSD_D2RN<3..0>	TRUE	TRUE	=PCIE_SSD_D2R_N<3..0>
NC_PCIE_SSD_R2D_CP<3..0>	TRUE	TRUE	=PCIE_SSD_R2D_C_P<3..0>
NC_PCIE_SSD_R2D_CN<3..0>	TRUE	TRUE	=PCIE_SSD_R2D_C_N<3..0>

Unused TPAD SPI

PP3V3_S4

TPAD_SPI_BUS_EN	MAKE_BASE=TRUE	TPAD_SPI_BUS_EN
TPAD_SPI_CS_L	TRUE	TPAD_SPI_CS_L
TPAD_SPI_INT_L	TRUE	TPAD_SPI_INT_L
TPAD_SPI_MISO	TRUE	TPAD_SPI_MISO
TPAD_SPI_MOSI	TRUE	TPAD_SPI_MOSI
TPAD_SPI_SCLK	TRUE	TPAD_SPI_SCLK

RA294 100K 1% 1/20W MF 201 (pin 2 → pin 1)
RA295 100K 1% 1/20W MF 201 (pin 2 → pin 1)
RA296 100K 1% 1/20W MF 201 (pin 2 → pin 1)
RA297 100K 1% 1/20W MF 201 (pin 2 → pin 1)
RA298 100K 1% 1/20W MF 201 (pin 2 → pin 1)
RA299 100K 1% 1/20W MF 201 (pin 2 → pin 1)

PP0V75_S3_MEM_VREFDQ_A	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A	
PP0V75_S3_MEM_VREFDQ_B	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B	
PP0V75_S3_MEM_VREFCA	0.675V	TRUE	PP0V75_S3_MEM_VREFCA	
PP0V75_S3_MEM_VREFCA				
PP0V75_S3_MEM_VREFCA				

EDP CABLE

I2C_BKLT_SCL	MAKE_BASE=TRUE	I2C_BKLT_SCL
I2C_BKLT_SDA	MAKE_BASE=TRUE	I2C_BKLT_SDA
SMBUS_SMC_0_S0_SCL		SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA		SMBUS_SMC_0_S0_SDA

PP3V3_S3_FAN_CTL — MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=3.3V, MAKE_BASE=TRUE

RA201 0 5% 1/20W MF 0201 (PP3V3_S5)
RA202 0 5% 1/20W MF 0201 NOSTUFF (PP3V3_S4)

Unused signals

- BT_PWRRST_L
- MEM_VDD_SEL_1V5_L
- FW_PWR_EN_PCH
- WOL_EN
- FW_PME_L
- DP_TBT_SEL
- ENET_MEDIA_SENSE_RDIV
- AUD_IPHS_SWITCH_EN_PCH
- AUD_IP_PERIPHERAL_DET
- AUD_I2C_INT_L
- TBT_GO2SX_BIDIR
- DPMUX_UC_IRQ
- PEG_CLKREQ_L
- ENET_CLKREQ_L
- ENET_LOW_PWR_PCH
- HDMITBTMUX_SEL_TBT
- SDCONN_OC_L
- LPCPLUS_GPIO (148)

PP5V_S0

XWA202 SM — PP5V_S0_AUDIO_AMP_L — MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=5V
XWA203 SM — PP5V_S0_AUDIO_AMP_R — MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=5V

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 102 OF 119
SHEET: 85 OF 97

Functional Test Points

J3501 - airport

FUNC_TEST

TRUE	AP_CLKREQ_Q_L	33
TRUE	AP_RESET_CONN_L	33
TRUE	PCIE_AP_D2R_PI_N	91
TRUE	PCIE_AP_D2R_PI_P	91
TRUE	PCIE_AP_R2D_N	33 91
TRUE	PCIE_AP_R2D_P	33 91
TRUE	PCIE_CLK100M_AP_CONN_N	33 91
TRUE	PCIE_CLK100M_AP_CONN_P	33 91
TRUE	PCIE_WAKE_L	12 33 35 91
TRUE	PP3V3_S3RS4_BT_F	33
TRUE	PP3V3_WLAN	33 41
TRUE	USB_BT_CONN_N	33 90
TRUE	USB_BT_CONN_P	33 90
TRUE	WIFI_EVENT_L	33 40 41
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	36 94
TRUE	MIPI_CLK_CONN_P	36 94
TRUE	CAM_SENSOR_WAKE_L_CONN	36
TRUE	MIPI_DATA_CONN_N	36 94
TRUE	MIPI_DATA_CONN_P	36 94
TRUE	SMBUS_SMC_0_S0_SDA	36 40 43 48 69 76 85 86 95
TRUE	SMBUS_SMC_0_S0_SCL	36 40 43 48 69 76 85 86 95
TRUE	I2C_CAM_SCK	35 36
TRUE	I2C_CAM_SDA	35 36
TRUE	PP5V_S3RS0_ALSCAM_F	36
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_EG_CLK_N	76 81 97
TRUE	HDMI_EG_CLK_P	76 81 97
TRUE	HDMI_EG_DATA_N<0>	76 81 97
TRUE	HDMI_EG_DATA_N<1>	76 81 97
TRUE	HDMI_EG_DATA_N<2>	76 81 97
TRUE	HDMI_EG_DATA_P<0>	76 81 97
TRUE	HDMI_EG_DATA_P<1>	76 81 97
TRUE	HDMI_EG_DATA_P<2>	76 81 97
TRUE	USB3_SD_D2R_N	13 20 81 91
TRUE	USB3_SD_D2R_P	13 20 81 91
TRUE	USB3_SD_R2D_C_N	13 20 81 91
TRUE	USB3_SD_R2D_C_P	13 20 81 91
TRUE	USB3_EXTB_D2R_N	13 81 90
TRUE	USB3_EXTB_D2R_P	13 81 90
TRUE	USB3_EXTB_R2D_N	81 90
TRUE	USB3_EXTB_R2D_P	81 90
TRUE	USB_EXTB_N	13 81 90
TRUE	USB_EXTB_P	13 81 90
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 81
TRUE	HDMI_DDC_CLK	
TRUE	HDMI_DDC_DATA	
TRUE	HDMI_HPD	20 81 82
TRUE	SMBUS_PCH_CLK	13 18 43 81 85 91
TRUE	SMBUS_PCH_DATA	13 18 43 81 85 91
TRUE	PM_SLP_S3_BUF_L	51 66 67 81 82
TRUE	PM_SLP_S4_L	12 21 33 37 40 67 81
TRUE	PP3V3_S3	3X 13 20 21 43 45 46 66 81 82 84 86
TRUE	PP3V3_S4	20 33 38 41 42 45 46 65 66 67 81 84 85 86
TRUE	PP5V_S4	5X 37 38 51 61 66 67 69 81 84 86
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 81
TRUE	USB_EXTB_OC_L	18 81
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	19 34 37 38 40 41 42 43 50 56 57 67 84 86
TRUE	SMC_LID_R	42
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	49
TRUE	FAN_LT_TACH	49
TRUE	PP5V_S0	3X 18 19 36 49 58 59 62 63 66 67 73 79 80 84 85 86
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	49
TRUE	FAN_RT_TACH	49
TRUE	PP5V_S0	3X 18 19 36 49 58 59 62 63 66 67 73 79 80 84 85 86
TRUE	GND	5X

J6100 - spi

FUNC_TEST

TRUE	PP3V42_G3H	19 34 37 38 40 41 42 43 50 56 57 67 84 86
TRUE	SMC_RESET_L	40 41 50 57
TRUE	SMC_TCK	40 41 50
TRUE	SMC_TMS	40 41 50
TRUE	SPIROM_USE_MLB	14 50
TRUE	GND	2X

J4801 - ipd flex

TRUE	USB_TPAD_N	13 38 90
TRUE	USB_TPAD_P	13 38 90
TRUE	IOXP2_INT_L	38
TRUE	I2C_IOXP_SCL	38
TRUE	I2C_IOXP_SDA	38
TRUE	SMC_PME_S4_WAKE_L	33 38 40 42
TRUE	TPAD_ACTUATOR_THRMTRIP_L	38 65
TRUE	TPAD_VBUS_EN	38 67
TRUE	SMBUS_SMC_2_S3_SCL	38 40 43 95
TRUE	SMBUS_SMC_2_S3_SDA	38 40 43 95
TRUE	SMC_LID	38 40 41 42
TRUE	SMC_ACTUATOR_EN_L	38 40
TRUE	PPVIN_S4_TPAD	4X 38 45 84
TRUE	GND_ACTUATOR	4X 38
TRUE	PP3V3_S4	20 33 38 41 42 45 46 65 66 67 81 84 85 86
TRUE	PP5V_S4	37 38 51 61 66 67 69 81 84 86
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	20 33 38 41 42 45 46 65 66 67 81 84 85 86
TRUE	PP3V42_G3H	19 34 37 38 40 41 42 43 50 56 57 67 84 86
TRUE	WS_CONTROL_KBD	38
TRUE	WS_KBD1	38
TRUE	WS_KBD10	38
TRUE	WS_KBD11	38
TRUE	WS_KBD12	38
TRUE	WS_KBD13	38
TRUE	WS_KBD14	38
TRUE	WS_KBD15_CAP	38
TRUE	WS_KBD16_NUM	38
TRUE	WS_KBD17	38
TRUE	WS_KBD18	38
TRUE	WS_KBD19	38
TRUE	WS_KBD2	38
TRUE	WS_KBD20	38
TRUE	WS_KBD21	38
TRUE	WS_KBD22	38
TRUE	WS_KBD23	38
TRUE	WS_KBD3	38
TRUE	WS_KBD4	38
TRUE	WS_KBD5	38
TRUE	WS_KBD6	38
TRUE	WS_KBD7	38
TRUE	WS_KBD8	38
TRUE	WS_KBD9	38
TRUE	WS_KBD_ONOFF_L	38
TRUE	WS_LEFT_OPTION_KBD	38
TRUE	WS_LEFT_SHIFT_KBD	38
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 39 63
TRUE	KBDBKLT_RETURN2	2X 39 63
TRUE	PPVOUT_S0_KBDBKLT	39 63
TRUE	GND	4X

J6601 - mic

TRUE	DMIC_CLK3	52 55
TRUE	PP3V3_S0	66 67 68 69 82 83 84 86 96 11 12 13 14 15 17 19 20 29 34 43 44 45 46 47 48 49 51 52 55
TRUE	DMIC_SDA2	55
TRUE	DMIC_SDA3	52 55
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	52 55
TRUE	SPKRCONN_L_OUT_N	53 55 96
TRUE	SPKRCONN_L_OUT_P	53 55 96
TRUE	SPKRCONN_SL_OUT_N	53 55 96
TRUE	SPKRCONN_SL_OUT_P	53 55 96
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	52 55
TRUE	SPKRCONN_R_OUT_N	53 55 96
TRUE	SPKRCONN_R_OUT_P	53 55 96
TRUE	SPKRCONN_SR_OUT_N	53 55 96
TRUE	SPKRCONN_SR_OUT_P	53 55 96
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	56
TRUE	PP20V_DCIN_FUSE	2X 56
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 56 57
TRUE	SMBUS_SMC_5_G3_SCL	40 43 56 57 95
TRUE	SMBUS_SMC_5_G3_SDA	40 43 56 57 95
TRUE	SYS_DETECT_L	56
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	69 97
TRUE	DP_INT_AUX_P	69 97
TRUE	DP_INT_ML_N<0>	69 97
TRUE	DP_INT_ML_N<1>	69 97
TRUE	DP_INT_ML_N<2>	69 97
TRUE	DP_INT_ML_N<3>	69 97
TRUE	DP_INT_ML_P<0>	69 97
TRUE	DP_INT_ML_P<1>	69 97
TRUE	DP_INT_ML_P<2>	69 97
TRUE	DP_INT_ML_P<3>	69 97
TRUE	LCD_FSS	69 82 85
TRUE	LCD_HPD_CONN	69
TRUE	LCD_BKLT_PWM_R	63 69
TRUE	SMBUS_SMC_0_S0_SDA	36 40 43 48 69 76 85 86 95
TRUE	SMBUS_SMC_0_S0_SCL	36 40 43 48 69 76 85 86 95
TRUE	I2C_BKLT_SDA	63 69 85
TRUE	I2C_BKLT_SCL	63 69 85
TRUE	PP5VR3V3_SW_LCD	3X 69
TRUE	PPVOUT_S0_LCDBKLT	63 69
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 40 67
TRUE	PPVTT_S0_DDR	21 27 60 84
TRUE	PP3V3_S0	66 67 68 69 82 83 84 86 96 11 12 13 14 15 17 19 20 29 34 43 44 45 46 47 48 49 51 52 55
TRUE	PP3V3_S3	13 20 21 43 45 46 66 81 82 84 86
TRUE	PP3V3_S5	12 14 15 17 18 19 21 31 32 33 61 64 66 67 82 84 86 96
TRUE	PP3V3_S5_AVREF_SMC	40 41
TRUE	PP3V42_G3H	19 34 37 38 40 41 42 43 50 56 57 67 84 86
TRUE	PP5V_S0	18 19 36 49 58 59 62 63 66 67 73 79 80 84 85 86
TRUE	PP5V_S3	21 36 60 66 67 84
TRUE	PP5V_S5	61 66 84
TRUE	PPBUS_G3H	30 44 47 56 57 63 65 84
TRUE	PPDCIN_G3H	56 57 84
TRUE	PPVCC_S0_CPU	6 8 10 45 59 84
TRUE	PPVTTDDR_S3	60 84
TRUE	PP3V3_S0SW_SSD	34 45 84
TRUE	PP1V5_S0	11 12 13 15 17 19 52 64 67 81 84
TRUE	PP1V35_S3	21 45 60 66 84

XDP

FUNC_TEST

TRUE	XDP_CPU_TCK	6 18 89
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 89
TRUE	XDP_CPU_TDO	6 18 89
TRUE	XDP_CPUPCH_TRST_L	6 18 89
TRUE	XDP_CPU_TMS	6 18 89
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 89
TRUE	XDP_CPU_PRDY_L	6 18 89
TRUE	PM_RSMRST_L	12 67 91
TRUE	PM_PCH_PWROK	12 19 91
TRUE	PM_SYSRST_L	12 19 40 91
TRUE	CPU_CFG<3>	6 18 89
TRUE	PP1V05_S0	10 14 15 17 18 41 62 67 84
TRUE	GND	2X GND

Power Sequence

FUNC_TEST

TRUE	SMC_ONOFF_L	38 40 41
TRUE	PM_DSW_PWRGD	12 40 91
TRUE	ALL_SYS_PWRGD	18 19 40 58 67
TRUE	PM_PCH_SYS_PWROK	12 18 19 40 91
TRUE	PLT_RESET_L	12 18 20 21
TRUE	LCD_PWR_EN	69 82
TRUE	LCD_BKLT_EN	63 82

GPU_VENUS JTAG

FUNC_TEST

TRUE	GPU_JTAG_TCK	76 77
TRUE	GPU_JTAG_TDI	76 77
TRUE	GPU_JTAG_TDO	76 77
TRUE	GPU_JTAG_TMS	76 77
TRUE	GPU_JTAG_TRST_L	76 77
TRUE	GPU_PWRGOOD	

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: Functional Test Points

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 104 OF 119

SHEET: 86 OF 97

NC NO_TESTs

PCH

		NO_TEST	MAKE_BASE	
87 13	NC_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN 13 87
87 13	NC_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP 13 87
87 13	NC_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN 13 87
87 13	NC_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP 13 87
90 87 13	NC_USB3_EXTC_D2RN	TRUE	TRUE	NC_USB3_EXTC_D2RN 13 87 90
90 87 13	NC_USB3_EXTC_D2RP	TRUE	TRUE	NC_USB3_EXTC_D2RP 13 87 90
90 87 13	NC_USB3_EXTC_R2D_CN	TRUE	TRUE	NC_USB3_EXTC_R2D_CN 13 87 90
90 87 13	NC_USB3_EXTC_R2D_CP	TRUE	TRUE	NC_USB3_EXTC_R2D_CP 13 87 90
90 87 13	NC_USB3_EXTD_D2RN	TRUE	TRUE	NC_USB3_EXTD_D2RN 13 87 90
90 87 13	NC_USB3_EXTD_D2RP	TRUE	TRUE	NC_USB3_EXTD_D2RP 13 87 90
90 87 13	NC_USB3_EXTD_R2D_CN	TRUE	TRUE	NC_USB3_EXTD_R2D_CN 13 87 90
90 87 13	NC_USB3_EXTD_R2D_CP	TRUE	TRUE	NC_USB3_EXTD_R2D_CP 13 87 90
87	NC_PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN 87
87	NC_PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP 87
87	NC_PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN 87
87	NC_PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP 87
90 87 11	NC_SATA_A_D2RN	TRUE	TRUE	NC_SATA_A_D2RN 11 87 90
90 87 11	NC_SATA_A_D2RP	TRUE	TRUE	NC_SATA_A_D2RP 11 87 90
90 87 11	NC_SATA_A_R2D_CN	TRUE	TRUE	NC_SATA_A_R2D_CN 11 87 90
90 87 11	NC_SATA_A_R2D_CP	TRUE	TRUE	NC_SATA_A_R2D_CP 11 87 90
90 87 11	NC_SATA_B_D2RN	TRUE	TRUE	NC_SATA_B_D2RN 11 87 90
90 87 11	NC_SATA_B_D2RP	TRUE	TRUE	NC_SATA_B_D2RP 11 87 90
90 87 11	NC_SATA_B_R2D_CN	TRUE	TRUE	NC_SATA_B_R2D_CN 11 87 90
90 87 11	NC_SATA_B_R2D_CP	TRUE	TRUE	NC_SATA_B_R2D_CP 11 87 90
87 11	NC_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN 11 87
87 11	NC_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP 11 87
87 11	NC_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN 11 87
87 11	NC_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP 11 87
87 11	NC_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN 11 87
87 11	NC_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP 11 87
87 11	NC_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN 11 87
87 11	NC_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP 11 87
87 11	NC_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN 11 87
87 11	NC_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP 11 87
87 11	NC_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN 11 87
87 11	NC_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP 11 87
90 87 13	NC_USB_EXTCN	TRUE	TRUE	NC_USB_EXTCN 13 87 90
90 87 13	NC_USB_EXTCP	TRUE	TRUE	NC_USB_EXTCP 13 87 90
90 87 13	NC_USB_SDN	TRUE	TRUE	NC_USB_SDN 13 87 90
90 87 13	NC_USB_SDP	TRUE	TRUE	NC_USB_SDP 13 87 90
87 13	NC_USB_WLANN	TRUE	TRUE	NC_USB_WLANN 13 87
87 13	NC_USB_WLANP	TRUE	TRUE	NC_USB_WLANP 13 87
90 87 13	NC_USB_6N	TRUE	TRUE	NC_USB_6N 13 87 90
90 87 13	NC_USB_6P	TRUE	TRUE	NC_USB_6P 13 87 90
90 87 13	NC_USB_7N	TRUE	TRUE	NC_USB_7N 13 87 90
90 87 13	NC_USB_7P	TRUE	TRUE	NC_USB_7P 13 87 90
90 87 13	NC_USB_EXTDN	TRUE	TRUE	NC_USB_EXTDN 13 87 90
90 87 13	NC_USB_EXTDP	TRUE	TRUE	NC_USB_EXTDP 13 87 90
87 13	NC_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN 13 87
87 13	NC_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP 13 87
90 87 13	NC_USB_IRN	TRUE	TRUE	NC_USB_IRN 13 87 90
90 87 13	NC_USB_IRP	TRUE	TRUE	NC_USB_IRP 13 87 90
89 87 11	NC_ITPXDP_CLK100MN	TRUE	TRUE	NC_ITPXDP_CLK100MN 11 87 89
89 87 11	NC_ITPXDP_CLK100MP	TRUE	TRUE	NC_ITPXDP_CLK100MP 11 87 89
87 12	NC_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L 12 87
87 11	NC_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3 11 87
87 11	NC_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1 11 87
87 11	NC_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2 11 87
87 11	NC_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3 11 87
87 13	NC_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L 13 87
87 13	NC_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK 13 87
87 13	NC_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA 13 87
87 13	NC_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L 13 87
91 87 11	NC_LPC_CLK33M_LPCPLUS_R	TRUE	TRUE	NC_LPC_CLK33M_LPCPLUS_R 11 87 91
87 12	NC_EDP_IG_BKL_PWM	TRUE	TRUE	NC_EDP_IG_BKL_PWM 12 87
90 87	NC_USB_SMCP	TRUE	TRUE	NC_USB_SMCP 87 90
90 87	NC_USB_SMCN	TRUE	TRUE	NC_USB_SMCN 87 90
87	NC_SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2 87

Thunderbolt

		NO_TEST	MAKE_BASE	
87 28	NC_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT 28 87
	TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0> 28
	TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0> 28
28 87	NC_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP 28 87
28 87	NC_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN 28 87
87 12	NC_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN 12 87
87 12	NC_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP 12 87
87 11	NC_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N 11 87
87 11	NC_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P 11 87
87 11	NC_PCIE_CLK100M_ENETSDN	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN 11 87
87 11	NC_PCIE_CLK100M_ENETSDP	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP 11 87
87 11	NC_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN 11 87
87 11	NC_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP 11 87
87 11	NC_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN 11 87
87 11	NC_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP 11 87
87 11	NC_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN 11 87
87 11	NC_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP 11 87
87 11	NC_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0 11 87
87 11	NC_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1 11 87
87 11	NC_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2 11 87
87 11	NC_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3 11 87
87 13	NC_USB_4N	TRUE	TRUE	NC_USB_4N 13 87
87 13	NC_USB_4P	TRUE	TRUE	NC_USB_4P 13 87
	TP_DVPCNTL_M<1..0>	TRUE	TRUE	NC_DVPCNTL_M<1..0> 76
	TP_DVPCNTL<2..0>	TRUE	TRUE	NC_DVPCNTL<2..0> 76
87 76	NC_DVPCLK	TRUE	TRUE	NC_DVPCLK 76 87
	TP_NC_DVPDATA<23..6>	TRUE	TRUE	NC_DVPDATA<23..6> 76
87 72	NC_FB_B0_A<9>	TRUE	TRUE	NC_FB_B0_A<9> 72 87
87 72	NC_FB_B1_A<9>	TRUE	TRUE	NC_FB_B1_A<9> 72 87
87 72	NC_FB_A0_A<9>	TRUE	TRUE	NC_FB_A0_A<9> 72 87
87 72	NC_FB_A1_A<9>	TRUE	TRUE	NC_FB_A1_A<9> 72 87
	PCIE_TBT_R2D_P<3..0>	TRUE		28 89
	PCIE_TBT_R2D_N<3..0>	TRUE		28 89
	PCIE_TBT_D2R_C_P<3..0>	TRUE		28 89
	PCIE_TBT_D2R_C_N<3..0>	TRUE		28 89
	DMI_S2N_P<3..1>	TRUE		5 12 89
	DMI_S2N_N<3..1>	TRUE		5 12 89
	DMI_N2S_P<3..1>	TRUE		5 12 89
	DMI_N2S_N<3..1>	TRUE		5 12 89

PLACEABLE BEAD-PROBES FOR TBT

93 31 28	TBT_A_D2R_P<1>	1	SM BEAD-PROBE	BPA531 NO_XNET_CONNECTION=TRUE
93 31 28	TBT_A_D2R_N<1>	1	SM BEAD-PROBE	BPA532 NO_XNET_CONNECTION=TRUE

SYNC_MASTER=J15_MLB SYNC_DATE=10/31/2012

PAGE TITLE: NC & No Test

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 105 OF 119

SHEET: 87 OF 97

X425G BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.092 MM	0.092 MM		0.120 MM	0.120 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.155 MM	0.155 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: PCB Rule Definitions

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 110 OF 119

SHEET: 88 OF 97

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	*	=4X_DIELECTRIC	?
PEG3_TXRX	*	=8X_DIELECTRIC	?
PEG3_2OTHER	*	=5X_DIELECTRIC	?
PEG3_2CLK	*	=8X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG3_2SAME	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG3_TXRX	TOP,BOTTOM	=12X_DIELECTRIC	?
PEG3_2OTHER	TOP,BOTTOM	=8X_DIELECTRIC	?
PEG3_2CLK	TOP,BOTTOM	=12X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG3_*	=SAME	*	PEG3_2SAME
PEG3_R2D	PEG3_D2R	*	PEG3_TXRX
PEG3_*	*	*	PEG3_2OTHER
PEG3_*	CLK_*	*	PEG3_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_P<3:0>	5 12 87
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N_N<3:0>	5 12 87
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_P<3:0>	5 12 87
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S_N<3:0>	5 12 87
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 86
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MP	11 87
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	NC_ITPXDP_CLK100MN	11 87
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 86
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 86
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 86
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 86
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPUPCH_TRST_L	6 18 86
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
XDP_DBRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 86
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 86
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 40
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 41
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 40 41 58
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTL	PM_THRMTRIP_L	6 14 41
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 58
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 58
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 58
CPU_MEM_VREF		MEM_12MTL	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		MEM_12MTL	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A	22 23 24 85 92
CPU_MEM_VREF		CPU_VREF	PP0V75_S3_MEM_VREFDQ_B	22 25 26 85
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 85 89 92
CPU_MEM_VREF		MEM_PWR	PP0V75_S3_MEM_VREFCA	22 23 24 25 26 85 89 92
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG_D2R_C_P<7..0>	68 70
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG_D2R_C_N<7..0>	68 70
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG_D2R_P<7..0>	70 85
PCIE_D2R_GPU	PEG_80D	PEG3_D2R	PEG_D2R_N<7..0>	70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG_R2D_C_P<7..0>	68 70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG_R2D_C_N<7..0>	68 70 85
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG_R2D_P<7..0>	70
PCIE_R2D_GPU	PEG_80D	PEG3_R2D	PEG_R2D_N<7..0>	70
PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_P<3..0>	5 34 85
PCIE_D2R_SSD	CPU_85D	PEG3_D2R	PCIE_SSD_D2R_N<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_P<3..0>	5 34 85
PCIE_R2D_SSD	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_C_N<3..0>	5 34 85
	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_P<3..0>	34
	CPU_85D	PEG3_R2D	PCIE_SSD_R2D_N<3..0>	34
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	5 28 85
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	5 28 85
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 87
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 87
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 87
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 87
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	5 28 85
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	5 28 85

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P	12 83 85
DP_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N	12 83 85

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	28 76 97
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	28 76 97
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28 97
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	28 76 97
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	28 76 97
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28 97
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28 97
TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28 97
TBTSNK_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28 97
	DP_85D		DP_TBTSNK0_AUXCH_C_P	28 83 97
	DP_85D		DP_TBTSNK0_AUXCH_C_N	28 83 97
TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_P	28 97
TBTSNK_AUXCH	DP_85D		DP_TBTSNK1_AUXCH_N	28 97
	DP_85D		DP_TBTSNK1_AUXCH_C_P	28 83 97
	DP_85D		DP_TBTSNK1_AUXCH_C_N	28 83 97

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: CPU Constraints

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 111 OF 119
SHEET: 89 OF 97

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	11 87
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	11 87
I27	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	11 87
I27	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	11 87
I29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	11 87
I29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	11 87
I30	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	11 87
I30	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	11 87
I213 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
	USB_85D	USB	USB_EXTA_P	13 37
	USB_85D	USB	USB_EXTA_N	13 37
I24	USB_85D	USB	USB_EXTA_MUXED_P	37
I24	USB_85D	USB	USB_EXTA_MUXED_N	37
I24	USB_85D	USB	USB_LT1_P	37
I24	USB_85D	USB	USB_LT1_N	37
	USB_85D	USB	NC_USB_EXTCP	13 87
	USB_85D	USB	NC_USB_EXTCN	13 87
I23	USB_85D	USB	NC_USB_SDP	13 87
I23	USB_85D	USB	NC_USB_SDN	13 87
I27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	37 40 41
I27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	37 40 41
	USB_85D	USB	NC_USB_SMCP	87
	USB_85D	USB	NC_USB_SMCN	87
I28	USB_85D	USB	NC_USB_6P	13 87
I28	USB_85D	USB	NC_USB_6N	13 87
I28	USB_85D	USB	NC_USB_7P	13 87
I28	USB_85D	USB	NC_USB_7N	13 87
	USB_85D	USB	USB_EXTB_P	13 81 86
	USB_85D	USB	USB_EXTB_N	13 81 86
I26	USB_85D	USB	NC_USB_EXTDP	13 87
I25	USB_85D	USB	NC_USB_EXTDN	13 87
	USB_85D	USB	USB_BT_P	13 33
	USB_85D	USB	USB_BT_N	13 33
	USB_85D	USB	USB_BT_CONN_P	33 86
	USB_85D	USB	USB_BT_CONN_N	33 86
I28	USB_85D	USB	NC_USB_IRP	13 87
I28	USB_85D	USB	NC_USB_IRN	13 87
I28	USB_85D	USB	USB_TPAD_P	13 38 86
I28	USB_85D	USB	USB_TPAD_N	13 38 86
I302	USB_85D	USB	USB_TPAD_R_P	
I30	USB_85D	USB	USB_TPAD_R_N	
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
I22 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 37
I23 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 37
I26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
I26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
I23 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	37
I22 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	37
I26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 37
I26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 37
I22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 81 86
I22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 81 86
I26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
I26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
I22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	81 86
I22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	81 86
I26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 81
I26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 81
I20 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	13 87
I20 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	13 87
I20	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	13 87
I20	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	13 87
I25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	13 87
I25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	13 87
I20	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	13 87
I20	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	13 87

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I250 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
I255 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
I255	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
I255 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 36
I253 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
I250	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: PCH Constraints 1

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 112 OF 119
SHEET: 90 OF 97

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?
SPI3X	*	=3x_DIELECTRIC	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 40 82
	LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 40 82
	SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 18 43 81 85 86
	SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 18 43 81 85 86
	SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 43
	SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 43
	SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 43
	SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 43
	HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 52
		HDA_45S	HDA	HDA_BIT_CLK_R	11
	HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 52
		HDA_45S	HDA	HDA_SYNC_R	11
		HDA_45S	HDA	HDA_RST_R_L	11
	HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 52
	HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 52
	HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	52
	HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 52
		HDA_45S	HDA	HDA_SDOUT_R	11 19
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	13 20 81 86
	USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	13 20 81 86
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	13 20 81 86
	USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	13 20 81 86
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	33 86
	PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	33 86
		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 33
1804		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 33
		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	
1805		PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 20 33
	PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 20 33
1276		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	86
1276		PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	86
1825	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	35 36
1824	PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	35 36
1827		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 36
1826		PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 36
1830	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 20 36
1829	PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 20 36
1831		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	35 36
1832		PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	35 36
		CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
	PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 40
1503		CLK_LPC_45S	CLK_LPC	NC_LPC_CLK33M_LPCPLUS_R	11 87
1540	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
1255	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
1256	PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
1253	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
1254	PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
1257	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
1258	PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
1251	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
1252	PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
1260	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
1259	PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_P	
	PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SD_N	
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 33
	PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 33
1808		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	33 86
1809		PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	33 86
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 36
	PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 36
1833		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	35 36
1834		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	35 36
1261	PCIE_CLK100M_FW	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 34
1262		CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 34
1837	PCIE_CLK100M_GPU	CLK_PCIE_85D	CLK_PCIE	PEG_CLK100M_P	11 70 85
1838		CLK_PCIE_85D	CLK_PCIE	PEG_CLK100M_N	11 70 85

PCH Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1315	PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
1314	PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
1316	PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
1318	PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
1309	PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 67 86
1307	PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 40 86
1312	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 86 91
1317	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 86 91
1320	PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 40 86
1310	PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 40 86
1308	PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 40
1306	PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 41 42
1326	PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 33 35 86
1324	PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
1336	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_CLK	
1335	SPI_MLB	SPI_45S	SPI	SPI_CLK	50
1345	SPI_MLB	SPI_45S	SPI	SPI_CLK_R	13 50
1338	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_CLK	50
1339	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_CLK	40 50
1340	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_CS_L	
1344	SPI_MLB	SPI_45S	SPI	SPI_CS0_L	50
1343	SPI_MLB	SPI_45S	SPI	SPI_CS0_R_L	13 50
1342	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_CS_L	50
1341	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_CS_L	40 50
1330	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_IO1_MISO	
1331	SPI_MLB	SPI_45S	SPI	SPI_MISO	13 50
1346	SPI_MLB	SPI_45S	SPI	SPI_MISO_R	50
1347	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_IO1_MISO	50
1348	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_MISO	40 50
1350	SPI_MLB	SPI_45S	SPI3X	SPI_ALT_IO0_MOSI	
1329	SPI_MLB	SPI_45S	SPI	SPI_MOSI	50
1328	SPI_MLB	SPI_45S	SPI	SPI_MOSI_R	13 50
1327	SPI_MLB	SPI_45S	SPI3X	SPI_MLB_IO0_MOSI	50
1326	SPI_MLB	SPI_45S	SPI3X	SPI_SMC_MOSI	40 50
1333	SPI_MLB_IO2	SPI_45S	SPI3X	SPI_IO<2>	13 50
1332	SPI_MLB_IO2	SPI_45S	SPI3X	SPI_MLB_IO2_WP_L	50
1334	SPI_MLB_IO2	SPI_45S	SPI3X	SPI_ALT_IO2_WP_L	
1335	SPI_MLB_IO3	SPI_45S	SPI3X	SPI_IO<3>	13 50
1337	SPI_MLB_IO3	SPI_45S	SPI3X	SPI_MLB_IO3_HOLD_L	50
1336	SPI_MLB_IO3	SPI_45S	SPI3X	SPI_ALT_IO3_HOLD_L	
1344	SPI_TPAD	SPI_45S	SPI	TPAD_SPI_SCLK	38 85
1343	SPI_TPAD_CS	SPI_45S	SPI	TPAD_SPI_CS_L	38 85
1342	SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MISO	38 85
1341	SPI_TPAD	SPI_45S	SPI	TPAD_SPI_MOSI	38 85

SYNC_MASTER=CLEAN_X305_PEG SYNC_DATE=02/18/2014

PAGE TITLE: PCH Constraints 2

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 113 OF 119

SHEET: 91 OF 97

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 25 26
		MEM_PWR	PP0V75_S3_MEM_VREFDQ_A 22 23 24 85 89
		MEM_PWR	PP0V75_S3_MEM_VREFCA 22 23 24 25 26 85 89
		MEM_PWR	PP1V35_S3_MEM 22 23 24 25 26 27 45 84

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Memory Constraints

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 114 OF 119
SHEET: 92 OF 97

DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0> 28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0> 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1> 28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1> 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3> 28 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3> 31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0> 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0> 28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0> 28 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1> 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1> 28 31 87
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1> 28 31 87
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P 31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N 28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N 31
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0> 28 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0> 32
TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1> 28 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1> 32
DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3> 28 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3> 32
DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0> 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0> 28 32
TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1> 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1> 28 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P 32
TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N 28 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P 32
TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N 32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK 28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI 28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO 28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L 28

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Thunderbolt Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 115 OF 119

SHEET: 93 OF 97

MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	PHYSICAL (NET_TYPE)	SPACING (NET_TYPE)	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE
161	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L
162		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT
163	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L
164	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0>
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1>
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2>
165	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0>
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0>
166	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1>
167	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1>
168	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0>
169	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1>
147	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0>
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0>
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8>
132	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P
133	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N
134		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P
135		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N
136	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P
137	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N
138		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P
139		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N
140			S2_MEM_PWR	PP1V35_CAM
140			S2_MEM_PWR	PP0V675_CAM_VREF
140			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA
140			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Camera Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 116 OF 119

SHEET: 94 OF 97

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	38 40 43 86
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	38 40 43 86
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	40 43 48
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	40 43 48
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	36 40 43 48 69 76 85 86
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	36 40 43 48 69 76 85 86
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	40 43 56 57 86
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	40 43 56 57 86
SMBUS_SMC_3_SCL	SMB_45S	SMB	NC_SMBUS_SMC_3_SCL	40 42
SMBUS_SMC_3_SDA	SMB_45S	SMB	NC_SMBUS_SMC_3_SDA	40 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	1TO1_DIFFPAIR		CHGR_CSI_P	57
	1TO1_DIFFPAIR		CHGR_CSI_N	57
	1TO1_DIFFPAIR		CHGR_CSO_P	57
	1TO1_DIFFPAIR		CHGR_CSO_N	57

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: SMC Constraints

Apple Inc.

DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 117 OF 119

SHEET: 95 OF 97

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	*			0.09 MM	100 MIL		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_GPUVR	*	Y	0.300 MM	0.200 MM	3.000 MM	0.400 MM	0.200 MM

AMD Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUFB_CS_P	47 73
	THERM_1TO1_45S	THERM	GPUFB_CS_N	47 73
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPU_TDIODE_P	48 76
	THERM_1TO1_45S	THERM	GPU_TDIODE_N	48 76
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPU_VDDCISENSE_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPU_VDDCISENSE_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPU_VDDCI_SENSE_XW_P	80
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPU_VDDCI_SENSE_XW_N	80
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPUVCORE_SENSE_P	79
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPUVCORE_SENSE_N	79
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PP0V95_S0GPU_R_P	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PP0V95_S0GPU_R_N	47
SENSE_DIFFPAIR	THERM_1TO1_45S	SENSE	VSNS_GPU_0V95_XW_P	73
	THERM_1TO1_45S	SENSE	VSNS_GPU_0V95_XW_N	73
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VDDCIS0_CS_R_P	47
	SENSE_1TO1_45S	SENSE	VDDCIS0_CS_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GPUFB_CS_R_P	47
	SENSE_1TO1_45S	SENSE	GPUFB_CS_R_N	47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VSNS_GPU_VDDC_P	71 79 85
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VSNS_GPU_VDDC_N	71 79
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VSNS_GPU_VDDI_P	71 80 85
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VSNS_GPU_VDDI_N	71 80
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V8_GPU_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V8_GPU_R_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V8_GPU_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V8_GPU_N	
SENSE_DIFFPAIR	THERM_1TO1_45S	SENSE	VSNS_GPU_FB_XW_P	73
	THERM_1TO1_45S	SENSE	VSNS_GPU_FB_XW_N	73

X425G Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P	46 66
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N	46 66
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P	46
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N	46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N	48
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	46 69 96
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	46 69 96
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N	48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	FINTHMSNS_D_N	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N	45
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P	45
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P	46
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N	46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	63
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_N	46 69 96
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCD_PANEL_P	46 69 96
	SENSE_1TO1_45S	SENSE	ISNS_PCH_R_P	45
	SENSE_1TO1_45S	SENSE	ISNS_PCH_R_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_P	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_TPAD_N	45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	44
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P	45
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N	45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N	

			DIFFERENTIAL_PAIR		
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1	CPUVR_ISNS1_P	45 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1	CPUVR_ISNS1_N	45 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2	CPUVR_ISNS2_P	45 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2	CPUVR_ISNS2_N	45 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3	CPUVR_ISNS3_P	45 59
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3	CPUVR_ISNS3_N	45 59

SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P	45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N	45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	79 96
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	79 96
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_P	79 96
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GFXIMVP_ISNS1_N	79 96
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N	45
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P	45
	AUDIODIFF	AUDIO	ISNS_TBT_R_N	45
	AUDIODIFF	AUDIO	ISNS_TBT_R_P	45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P	45
	THERM_1TO1_45S	THERM	ISNS_SSD_N	45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P	45
	THERM_1TO1_45S	THERM	ISNS_SSD_R_N	45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P	45 62
	THERM_1TO1_45S	THERM	P1V05S0_CS_N	45 62

			DIFFERENTIAL_PAIR		
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE	P1V05S0_SENSE_P	62
	THERM_1TO1_45S	THERM	P1V05S0_SENSE	P1V05S0_SENSE_N	62
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMDP		28 48
	THERM_1TO1_45S	THERM	TBT_THERMDN		48
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P		57
	AUDIODIFF	AUDIO	CHGR_CSI_R_N		57
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P		57
	AUDIODIFF	AUDIO	CHGR_CSO_R_N		57
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GFXIMVP_ISNS2_P		79
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	GFXIMVP_ISNS2_N		79
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GPU_P		47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_GPU_N		47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PP0V95_S0GPU_P		47 73
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_PP0V95_S0GPU_N		47 73
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VDDCIS0_CS_P		47 80
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	VDDCIS0_CS_N		47 80
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_P		48
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_N		48

X425G Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N	53
	AUDIODIFF	AUDIO	RSUBIN_P	53
	AUDIODIFF	AUDIO	RSUBIN_N	53
	AUDIODIFF	AUDIO	LSUBIN_P	53
	AUDIODIFF	AUDIO	LSUBIN_N	53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	51 53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_P	53
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N	53
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	53 55 86
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N	
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N	51
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P	
	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N	
	DIFFPAIR	AUDIO	AUD_HS_MIC_P	54 55
	DIFFPAIR	AUDIO	AUD_HS_MIC_N	54 55
	DIFFPAIR	AUDIO	HS_MIC_P	51 54
	DIFFPAIR	AUDIO	HS_MIC_N	51 54
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P	
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N	
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P	51 53
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N	51 53

SB_POWER	PP3V3_S5		66 67 82 84 85 86 12 14 15 17 18 19 21 31 32 33
SB_POWER	PP3V3_S0		66 67 68 69 82 83 84 86 11 12 13 14 15 17 18 20
SB_POWER	PP1V35_S3RS0_CPUDDR		43 44 45 46 47 48 49 51 52 55 6 8 10 21 66 67 84
GND	GND		

SYNC_MASTER=SIDLE_J45 SYNC_DATE=12/10/2012

PAGE TITLE: Project Specific Constraints

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DRAWING NUMBER: <SCH_NUM> SIZE: D

REVISION: <E4LABEL>

BRANCH: <BRANCH>

PAGE: 118 OF 119

SHEET: 96 OF 97

GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=7x_DIELECTRIC	?

GDDR5_CMD spacing can be relaxed to 2x per AMD recommendation for x32_4.5G config.

Breakout Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR5_*	*	BGA	GDDR5_BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_BGA	*	=1.3x_DIELECTRIC	?

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P	72 74
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N	72 74
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P	72 74
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N	72 74
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_A<8..0>	72 74
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_A<8..0>	72 74
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_ABI_L	72 74
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_ABI_L	72 74
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_RAS_L	72 74
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_RAS_L	72 74
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CAS_L	72 74
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CAS_L	72 74
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_WE_L	72 74
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_WE_L	72 74
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CKE_L	72 74
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CKE_L	72 74
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CS_L	72 74
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CS_L	72 74
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>	72 74
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>	72 74
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>	72 74
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>	72 74
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>	72 74
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>	72 74
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>	72 74
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>	72 74
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>	72 74
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>	72 74
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>	72 74
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>	72 74
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>	72 74
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>	72 74
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>	72 74
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>	72 74
FB_A0_WCLK0	GDDR5_80D	GDDR5_CLK	FB_A0_WCLK_P<0>	72 74
FB_A0_WCLK0	GDDR5_80D	GDDR5_CLK	FB_A0_WCLK_N<0>	72 74
FB_A0_WCLK1	GDDR5_80D	GDDR5_CLK	FB_A0_WCLK_P<1>	72 74
FB_A0_WCLK1	GDDR5_80D	GDDR5_CLK	FB_A0_WCLK_N<1>	72 74
FB_A1_WCLK0	GDDR5_80D	GDDR5_CLK	FB_A1_WCLK_P<0>	72 74
FB_A1_WCLK0	GDDR5_80D	GDDR5_CLK	FB_A1_WCLK_N<0>	72 74
FB_A1_WCLK1	GDDR5_80D	GDDR5_CLK	FB_A1_WCLK_P<1>	72 74
FB_A1_WCLK1	GDDR5_80D	GDDR5_CLK	FB_A1_WCLK_N<1>	72 74
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>	72 74
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>	72 74
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>	72 74
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>	72 74
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>	72 74
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>	72 74
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>	72 74
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>	72 74
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_RESET_L	
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_RESET_L	

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P	72 75
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N	72 75
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P	72 75
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N	72 75
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>	72 75
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>	72 75
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L	72 75
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L	72 75
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L	72 75
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L	72 75
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L	72 75
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L	72 75
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L	72 75
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L	72 75
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L	72 75
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L	72 75
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L	72 75
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L	72 75
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>	72 75
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>	72 75
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>	72 75
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>	72 75
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>	72 75
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>	72 75
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>	72 75
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>	72 75
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>	72 75
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>	72 75
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>	72 75
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>	72 75
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>	72 75
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>	72 75
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>	72 75
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>	72 75
FB_B0_WCLK0	GDDR5_80D	GDDR5_CLK	FB_B0_WCLK_P<0>	72 75
FB_B0_WCLK0	GDDR5_80D	GDDR5_CLK	FB_B0_WCLK_N<0>	72 75
FB_B0_WCLK1	GDDR5_80D	GDDR5_CLK	FB_B0_WCLK_P<1>	72 75
FB_B0_WCLK1	GDDR5_80D	GDDR5_CLK	FB_B0_WCLK_N<1>	72 75
FB_B1_WCLK0	GDDR5_80D	GDDR5_CLK	FB_B1_WCLK_P<0>	72 75
FB_B1_WCLK0	GDDR5_80D	GDDR5_CLK	FB_B1_WCLK_N<0>	72 75
FB_B1_WCLK1	GDDR5_80D	GDDR5_CLK	FB_B1_WCLK_P<1>	72 75
FB_B1_WCLK1	GDDR5_80D	GDDR5_CLK	FB_B1_WCLK_N<1>	72 75
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>	72 75
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>	72 75
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>	72 75
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>	72 75
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>	72 75
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>	72 75
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>	72 75
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>	72 75
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L	
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L	

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	69 82
	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	69 82
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	69
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	69
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	69 86
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	69 86
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	69 82
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	69 82
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P	69 86
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_N	69 86
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	76 77 82
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	76 77 82
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	76 82
	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	76 82
	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P	5 82 85
	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N	5 82 85
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3..0>	5 82 85
	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3..0>	5 82 85
DP_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_P	76 77 83
DP_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_N	76 77 83
DP_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_P	76 77 83
DP_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_N	76 77 83
TBTSNK_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	28 89
TBTSNK_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	28 89
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	28 83 89
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	28 83 89
TBTSNK_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	28 89
TBTSNK_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	28 89
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	28 83 89
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	28 83 89
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28 89
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28 89
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	28 76 89
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	28 76 89
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28 89
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28 89
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	28 76 89
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	28 76 89

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	1:1_DIFFPAIR		GPU_CLK_TEST_RC_P	72
	1:1_DIFFPAIR		GPU_CLK_TEST_RC_N	72
GPU_CLK_TEST	1:1_DIFFPAIR		GPU_CLK_TEST_P	72
GPU_CLK_TEST	1:1_DIFFPAIR		GPU_CLK_TEST_N	72
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_P<2..0>	76 81 86
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_N<2..0>	76 81 86
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_P	76 81 86
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_N	76 81 86

SYNC_MASTER=J45G_AMD SYNC_DATE=07/01/2014

PAGE TITLE: GPU (AMD VENUS) Constraints

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DRAWING NUMBER: <SCH_NUM> SIZE: D
REVISION: <E4LABEL>
BRANCH: <BRANCH>
PAGE: 119 OF 119
SHEET: 97 OF 97