Colossus 15/17
DIS_OPT Schematic
IVY Bridge (rPGA989)
Intel PCH (Panther Point)

REV:-1
2012-01-05.

DY:No stuff
DIS_OPT:DISCRTE OPTIMUS installed
DY_35W:No stuff on 35W CPU
DY_45W:No stuff on 45W CPU
CR_Balen17:Stuff for 17"
CR_Goya:Stuff for 15"

<Core Design>

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Title: Cover Page

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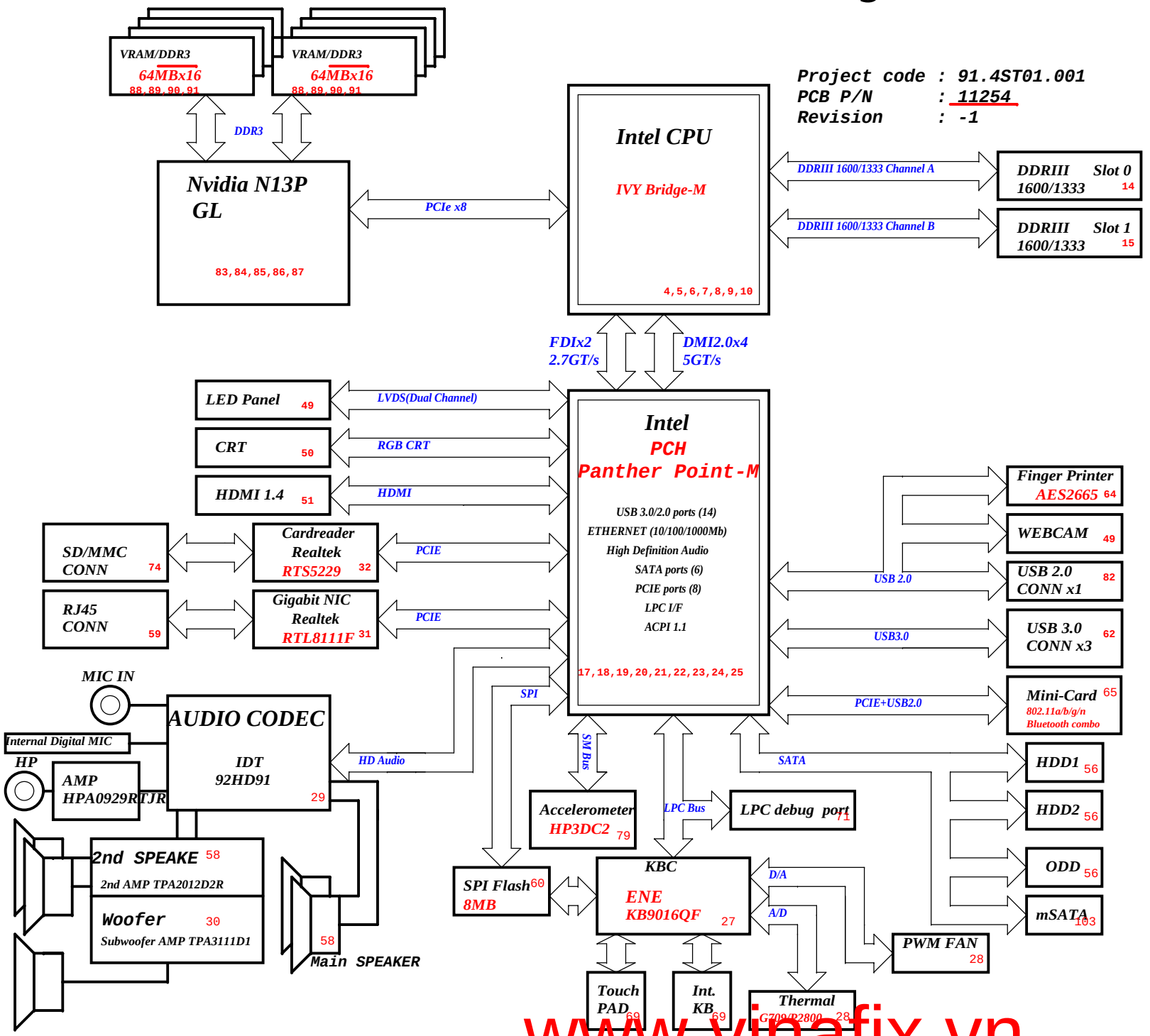
COLOSSUS Block Diagram



SYSTEM DC/DC TPS51461 48	
INPUTS	OUTPUTS
5V_S5	VCCSA=0D85V_S0

CPU DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT(5V_S5)	VCC_CORE

SYSTEM DC/DC SN1003055RUWR 45	
INPUTS	OUTPUTS
5V_S5/3D3V_S5	1D05V_S0

SYSTEM DC/DC RT8223M_5V/3D3V 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC RT8207MZ 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC VT1323 42~44	
INPUTS	OUTPUTS
DCBATOUT(5V_S5)	VCC_GFXCORE

VGA NCP3218G 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER BQ24738 40	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC RT8068A 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC VT385FCX 93	
INPUTS	OUTPUTS
3D3V_S0 1D5V_S0 1D5V_S3	3D3V_VGA_S0 1D5V_VGA_S0 1V05_VGA_S0

Switches 36	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER (DISCRETE)

L1:Top	L5:Vcc
L2:GND	L6:Signa
L3:Signal	L7:GND
L4:Signal	L8::Bottom

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Title: Block Diagram

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PCH Strapping

Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	**0**
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	**11**
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	**1**

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_S0 VCCSA_0D85V 0D75V_S0 VCC_CORE VCC_GFXCORE 3D3V_VGA_S0 1D5V_VGA_S0 1D05V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 3.3V 1D5V 1D05V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SMBus ADDRESSES

I²C / SMBus Addresses Device	Ref Des	Chief River CRV Address / Hex / Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

PCIe Routing

LANE1	N/A
LANE2	17"Card Reader
LANE3	15"Card Reader
LANE4	Mini Card1(WLAN)
LANE5	N/A
LANE6	Intel GBE LAN / LAN
LANE7	N/A
LANE8	N/A

USB2.0 Table

Pair	Device
0	USB 3.0 I/O CONN. 1
1	N/A
2	USB 3.0 I/O CONN. 2
3	USB 3.0 I/O CONN. 3
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 I/O CONN.
10	Camera
11	FREE
12	FREE
13	FREE

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1
2	FREE
3	I/O CONN. 2
4	I/O CONN. 3

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	HDD2
3	N/A
4	ODD
5	N/A

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Title: Table of Content

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CPU(1/7)

IVY BRIDGE PROCESSOR (DMI,DP,PEG,FDI)

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

DP Compensation, within 500mil

NOTE: EDP_HPD
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns.
If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.
This signal can be left as no connect if entire eDP interface is disabled.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

PEG Compensation

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

633996-302

2ND = 62.10055.321

3RD = 62.10055.551

Hand control CPU1 P/N

1st 633996-302
2nd 633996-501
3rd 633996-301

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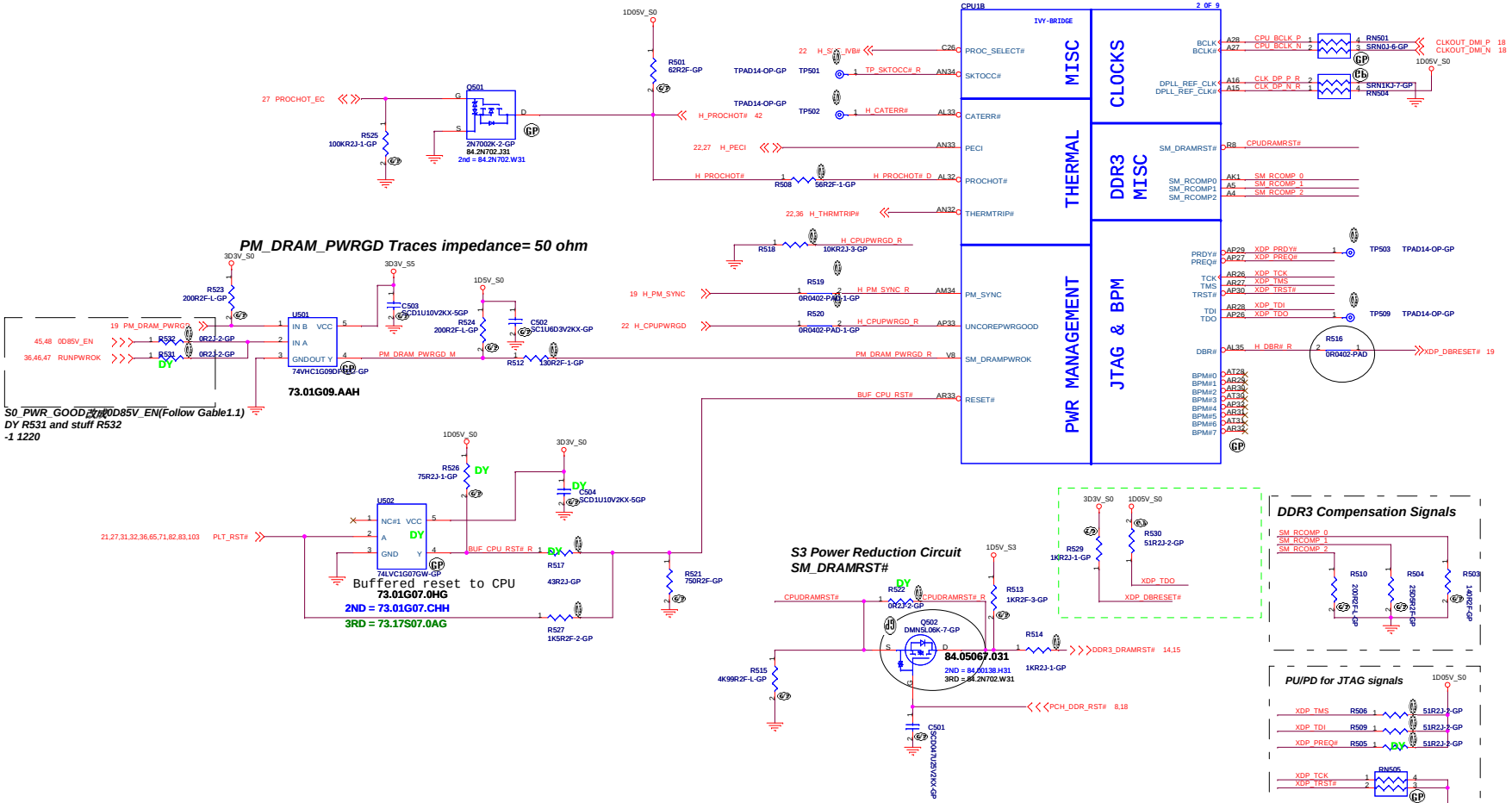
Title: CPU(1/7): DMI/PEG/FDI
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 4 of 103

CPU(2/7)

IVY BRIDGE PROCESSOR (CLK,MISC,JTAG)



<Core Design>

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Title: CPU(2/7): CLK/MISC/JTAG

Size: A2 | Document Number: Colossus | Rev: 1

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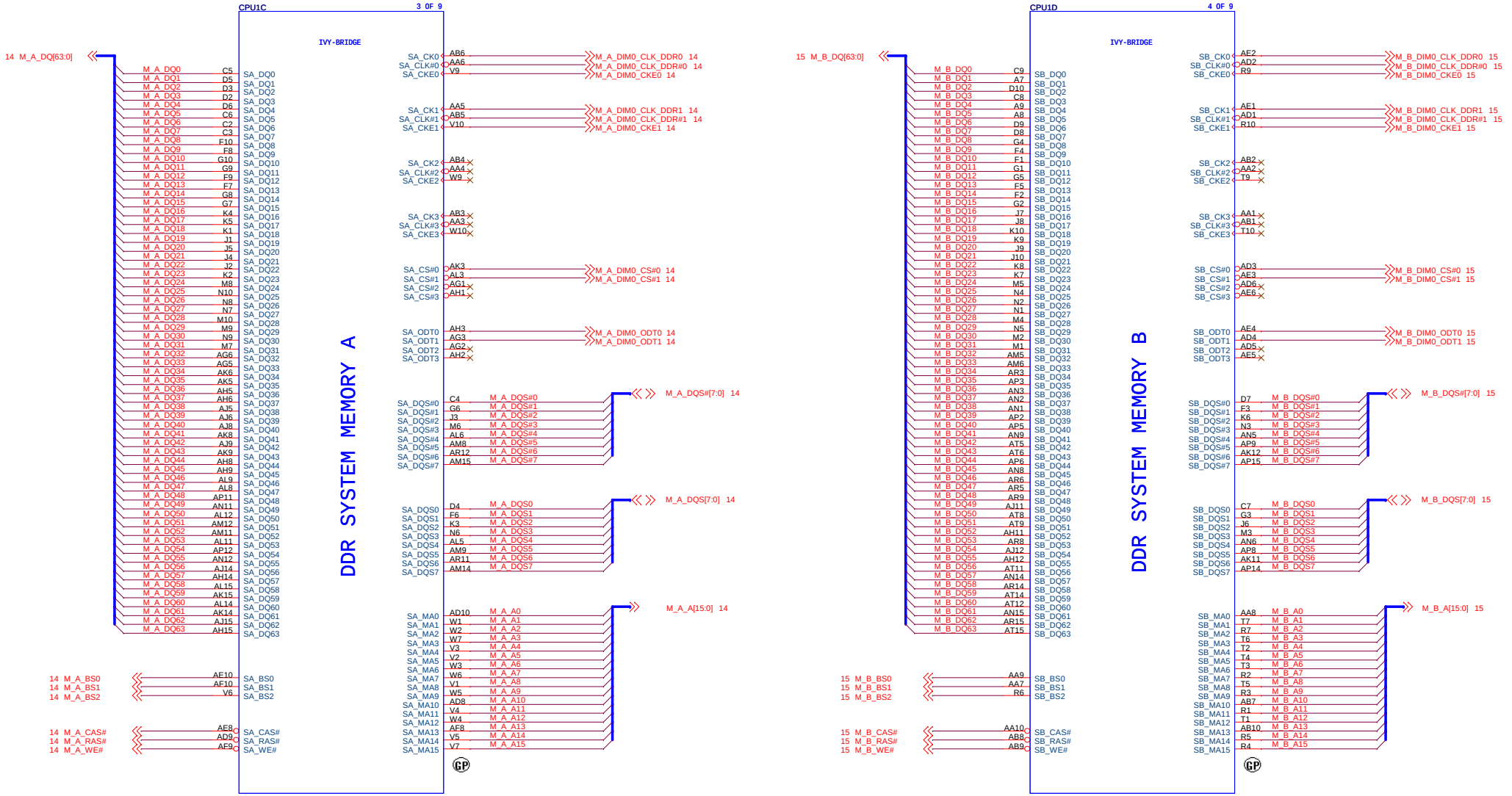
CPU(3/7)

IVY BRIDGE PROCESSOR (DDR3)



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CPU(4/7)

IVY BRIDGE PROCESSOR (POWER)

POWER

CPU1F

6 OF 9

IVY-BRIDGE

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

PROCESSOR CORE POWER

53A

VCC_CORE

Place Bottom

Place Top

PROCESSOR UNCORE POWER

8.5A

1D05V_S0

Power 78.22610.51L

Differential Sense feedback

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CPU(5/7)
IVY BRIDGE PROCESSOR (GRAPHICS POWER)

M3 - Processor Generated SO-DIMM VREF_DQ

33A

VCC_GFXCORE

470U*2 22U*6

Under Socket and Closed to CPU

C820 C821 C822 C823 C824 C825 SC22U6D3V5MX-2GP

VCC_GFXCORE

22U*6

Closed to CPU Socket

C826 C827 C828 C829 C830 C831 SC22U6D3V5MX-2GP

Power 78.22610_51L

C837 C836 C835 C834 C833 SC10U6D3V5KX-1GP

C832 SC22U6D3V5MX-2GP

1.5A

1D8V_S0

C819 C816 SC10U6D3V5KX-1GP

C817 SC1U10V2KX-1GP

C818 SC1U10V2KX-1GP

CPU1G

IVY-BRIDGE

7 OF 9

POWER

SENSE LINES

VAXG_SENSE AK35 → VCC_AXG_SENSE 42

VSSAXG_SENSE AK34 → VSS_AXG_SENSE 42

VREF

SM_VREF AL1 ← +V_SM_VREF_CNT

CAD Note: +V_SM_VREF should have 10 mil trace width

B4:VREF_DQ CHA
D1:VREF_DQ CHB

SA_DIMM_VREFDQ B4 → DDR_VREF_S3_B4

SB_DIMM_VREFDQ D1 → DDR_VREF_S3_D1

R815 1KR2F-3-GP DY

R816 1KR2F-3-GP DY

C801 DY SCD1U16V2ZY-2GP

C802 DY SCD2U10V2ZY-1GP

GRAPHICS

DDR3 -1.5V RAILS

12~16A

330U*1 10U*6

1D5V_S0

VDDQ1 AE7
VDDQ2 AE4
VDDQ3 AE1
VDDQ4 AC7
VDDQ5 AC4
VDDQ6 AC1
VDDQ7 Y7
VDDQ8 Y4
VDDQ9 Y1
VDDQ10 U7
VDDQ11 U4
VDDQ12 U1
VDDQ13 P7
VDDQ14 P4
VDDQ15 P1

C803 C804 SC4D7U6D3V3KX-GP

C805 C806 SC10U6D3V5KX-1GP

C807 DY SC10U6D3V5KX-1GP

C808 DY SC10U10V5KX-2GP

TC801 ST330U2D5VDM-9GP

77.23371.13L
2nd = 79.33719.L01

SA RAIL

6A

0D85V_S0

VCCSA1 M27
VCCSA2 M26
VCCSA3 L26
VCCSA4 J26
VCCSA5 J25
VCCSA6 J24
VCCSA7 H26
VCCSA8 H25

C813 C814 SC10U6D3V5KX-1GP

C815 SC10U6D3V5KX-1GP

0D85V_S0

R801 DY 100R2J-2-GP

VCCSA_SENSE H23 → VCCUSA_SENSE

VCCUSA_SENSE 48

1.8V RAIL

VCCPLL1 B6
VCCPLL2 A6
VCCPLL3 A2

MISC

VCCSA_VID0 C22
VCCSA_VID1 C24

H_FC_C22
VCCSA_SEL

H_FC_C22 48
VCCSA_SEL 48

VCCIO_SEL A19 ← H_VCCP_SEL

RN801 SRN1KJ-11-GP-U

R817 0R2J-2-GP DY

H_SNB_IVB#_PWRCTRL

TP801 TPAD14-OP-GP

R818 0R2J-2-GP DY

SNB: No Connect
IVB: VSS

H_VCCP_SEL	Voltage
1	1.05V
0	1.0V

DDR_VREF_S3

R808 0R2J-2-GP DY

R809 0R2J-2-GP DY

14 M_VREF_DQ_DIMM0

15 M_VREF_DQ_DIMM1

84.05067.031

2ND = 84.00138.H31
3RD = 84.2N702.W31

Q802 DMN5L06K-7-GP

R810 0R2J-2-GP DY

PCH_DDR_RST#

0R2J-2-GP R812

0R2J-2-GP R813

M_VREF_DQ_DIMM0_R

M_VREF_DQ_DIMM1_R

DDR_VREF_S3_B4

DDR_VREF_S3_D1

3RD = 84.2N702.W31
2ND = 84.00138.H31
84.05067.031

Q803 DMN5L06K-7-GP

R814 0R2J-2-GP DY

5,18 PCH_DDR_RST#

-1 1221

S3 Power Reduction Circuit Processor VREF_DQ Implementation

DDR_VREF_S3

R807 0R2J-2-GP

R811 DY 0R2J-2-GP

14 M_VREF_DQ_DIMM0

R805 DY 0R2J-2-GP

+V_SM_VREF

Q801 DMN5L06K-7-GP

84.05067.031

2ND = 84.00138.H31
3RD = 84.2N702.W31

+V_SM_VREF_CNT

R803 100KR2J-1-GP

R802 DY 0R2J-2-GP

5,18 PCH_DDR_RST#

19,27,36,46,47,92 PM_SLP_S3#

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Title: CPU(5/7): GFX/PWR

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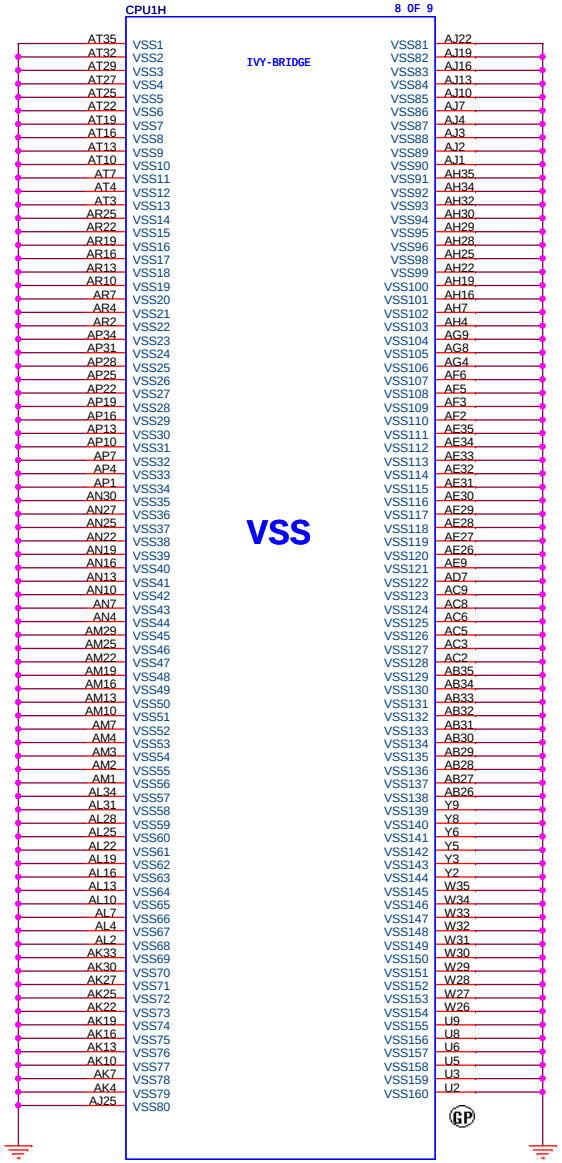
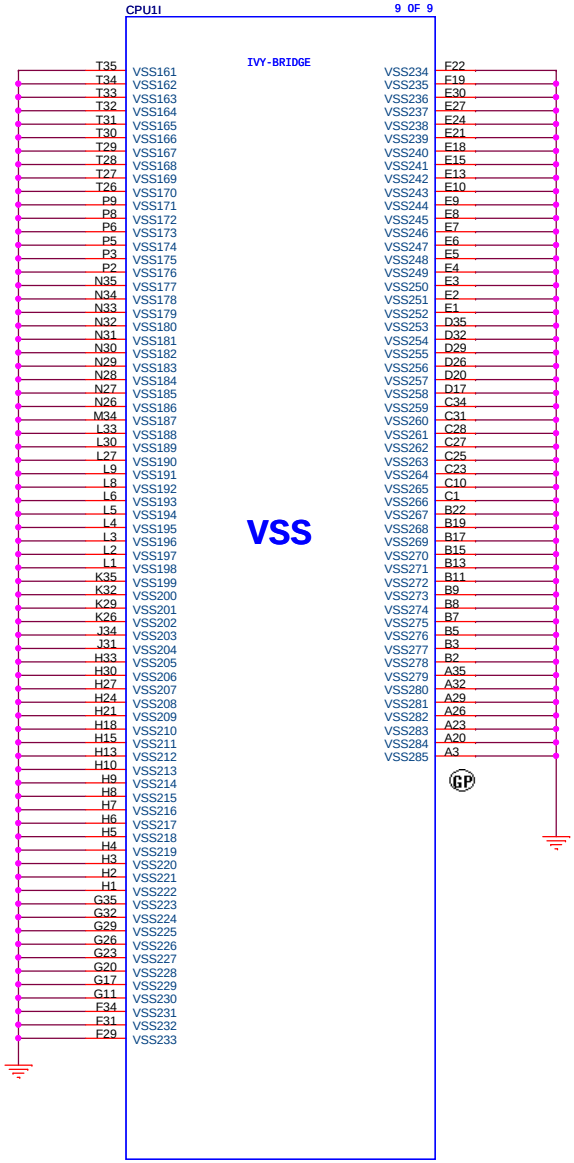
CPU(6/7)

IVY BRIDGE PROCESSOR (GND)





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Title: **CPU (6/7):GND**

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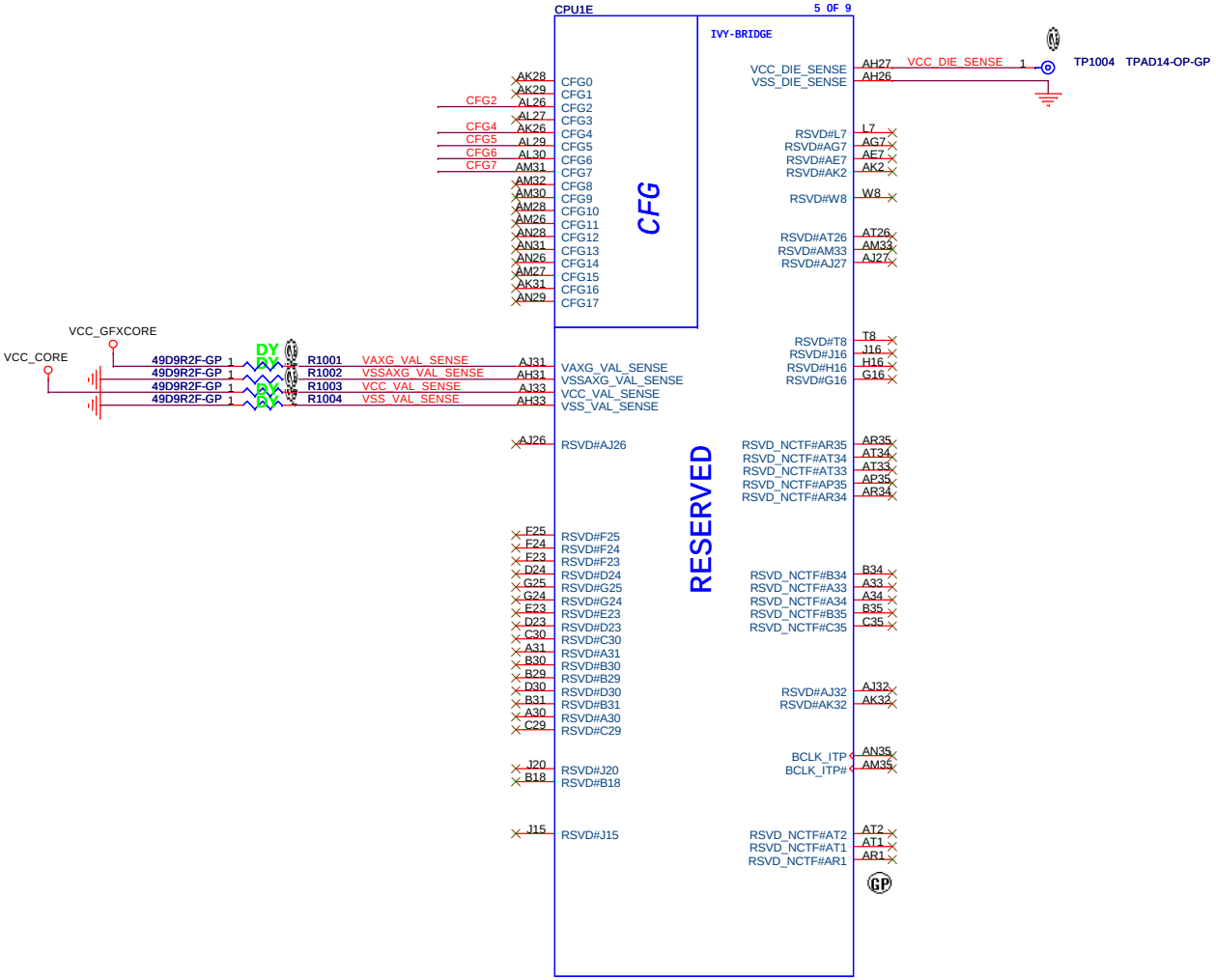
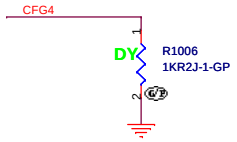
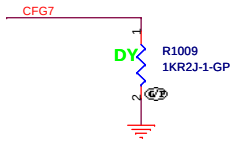
CPU(7/7)

IVY BRIDGE PROCESSOR (RESERVED)

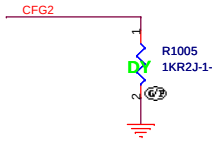




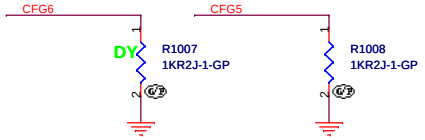
Display Port Presence Strap	0:Enable eDP
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



PEG Static Lane Reversal	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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Title: **CPU(7/7): CFG/RSVD/DDR3_VRE**

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Title: CPU XDP

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A3	Colossus	1

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Title: Reserved

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<Core Design>

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Title
AOAC

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A3	**Colossus**	1

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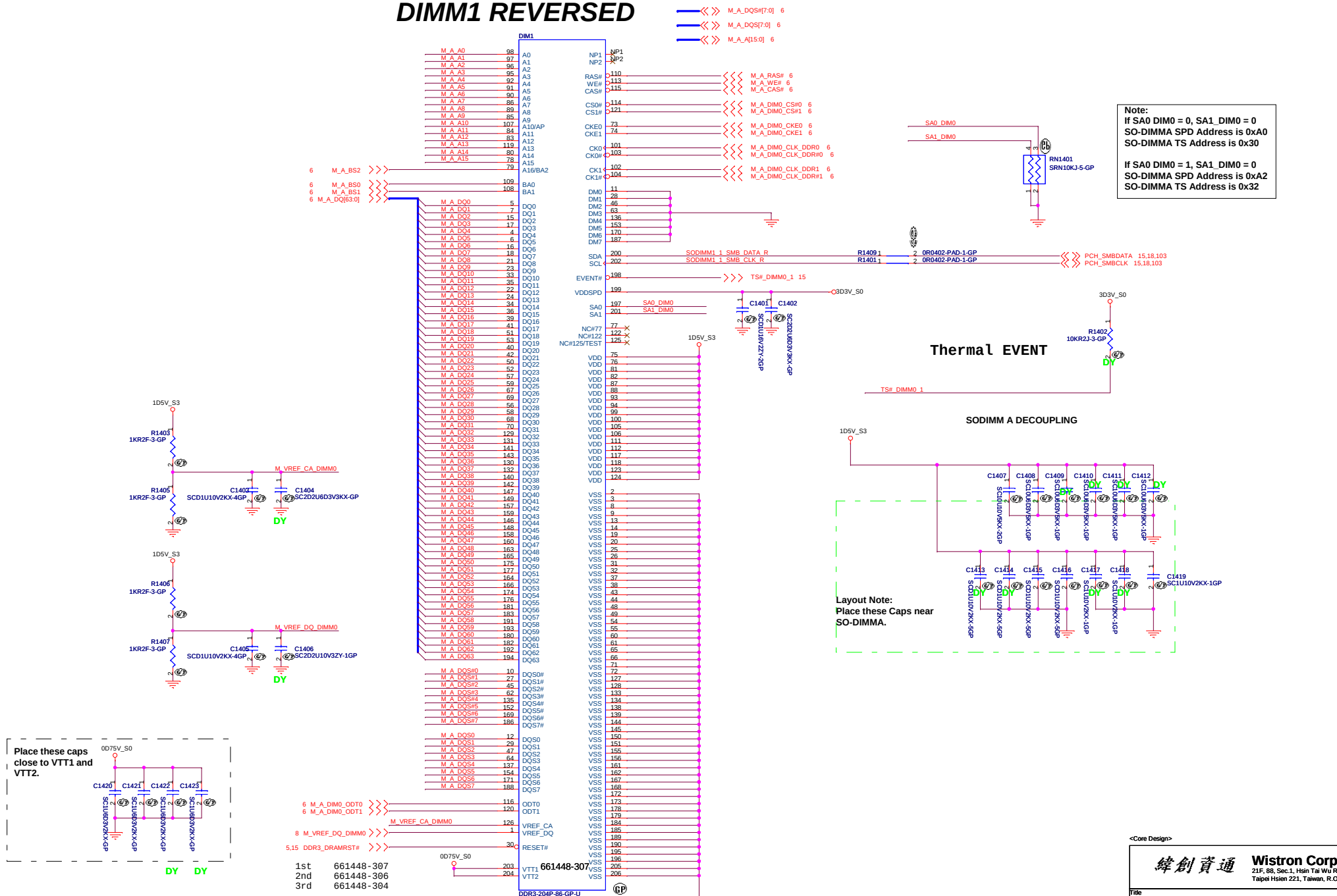
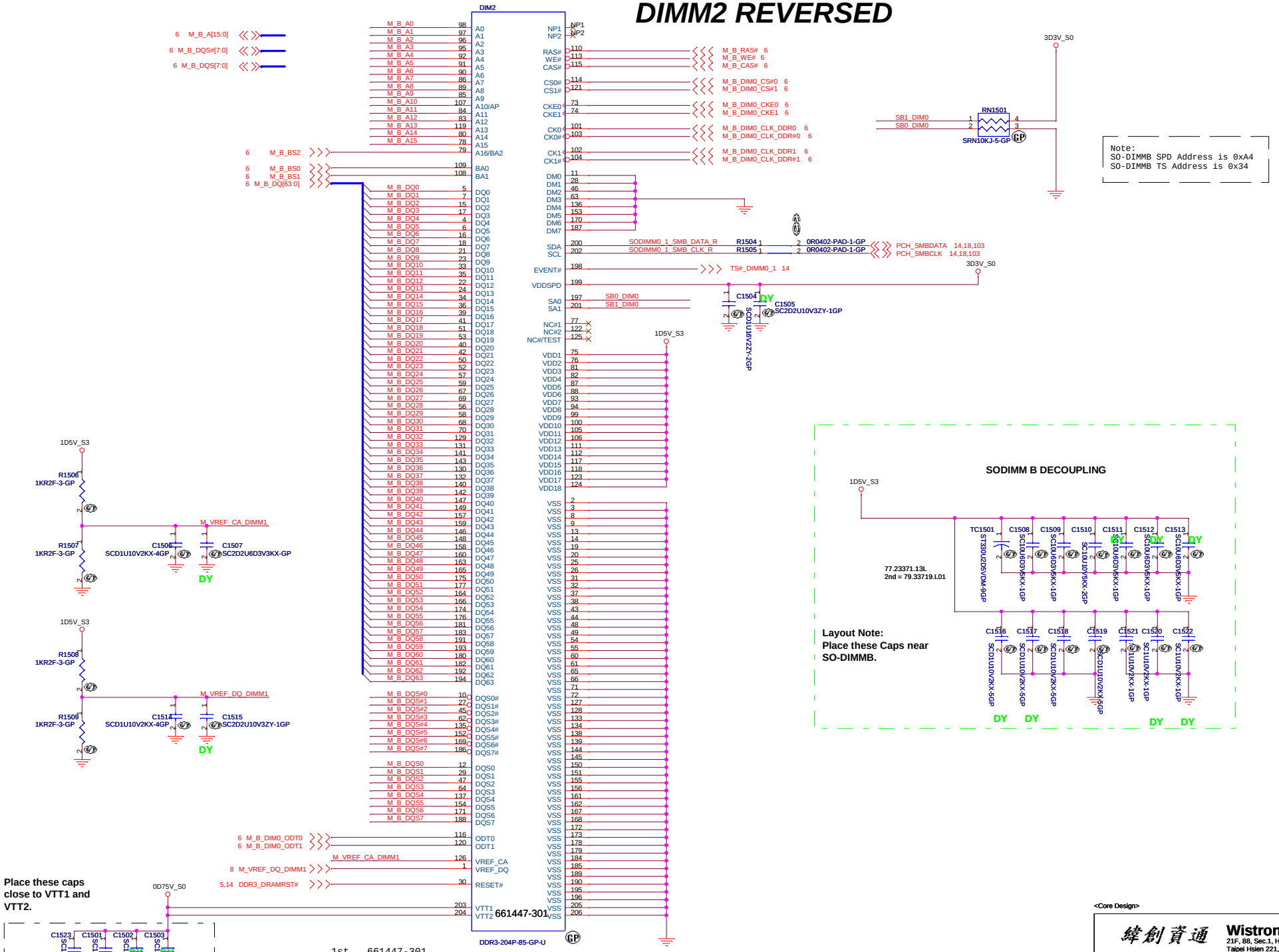
DIMM1 REVERSED



DIMM2 REVERSED



1st 661447-301
2nd 661447-306
3rd 661447-304

010412 Update connetor HP P/N, hanle control but not change library

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3 SO-DIMM2

Size: Custom | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 15 of 103

(Blanking)

<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 16 of 103

PCH(1/9)

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs

PCH1A — 1 OF 10 — PANTHER-GP-NF

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23, SERIRQ
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13
SATA: SATA 6G — SATA0RXN/RXP/TXN/TXP, SATA1RXN/RXP/TXN/TXP, SATA2RXN/RXP/TXN/TXP, SATA3RXN/RXP/TXN/TXP, SATA4RXN/RXP/TXN/TXP, SATA5RXN/RXP/TXN/TXP, SATAICOMPO, SATAICOMPI, SATA3RCOMPO, SATA3COMPI, SATA3RBIAS, SATALED#, SATA0GP/GPIO21, SATA1GP/GPIO19
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

HDD1 / mSATA / HDD2 / ODD

RTC Battery

RTC1 — ACES-CON2-18-GP — 20.F1637.002 — 2ND = 20.F1864.002
U1701 — TM715FPT-GP — 83.R0304.B81 — 2ND = 83.R2004.C81
C1705 SC1U10V3ZY-6GP

NO REBOOT STRAP

No Reboot Strap R1722	
HDA_SPKR	Low = Default High = No Reboot

LAYOUT NOTE:

JTAG_TMS TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDI TERMINATIONS NEED TO BE PLACED NEAR PCH
JTAG_TDO TERMINATIONS NEED TO BE PLACED NEAR XDP
JTAG_TCK TERMINATIONS NEED TO BE PLACED NEAR PCH

<Core Design>

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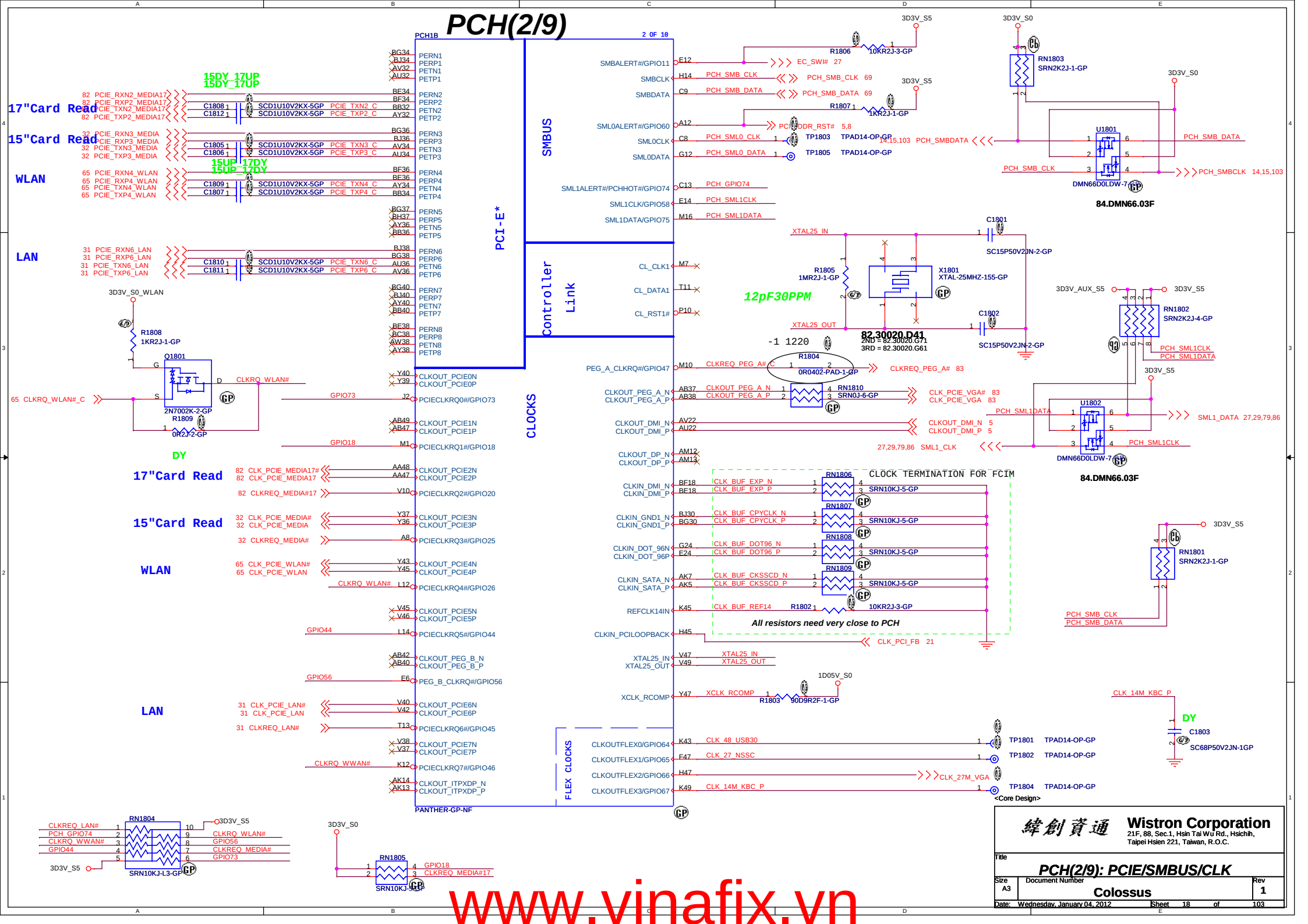
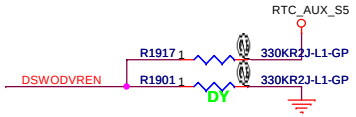
Title: PCH(1/9): HDA/JTAG/SATA
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 17 of 103

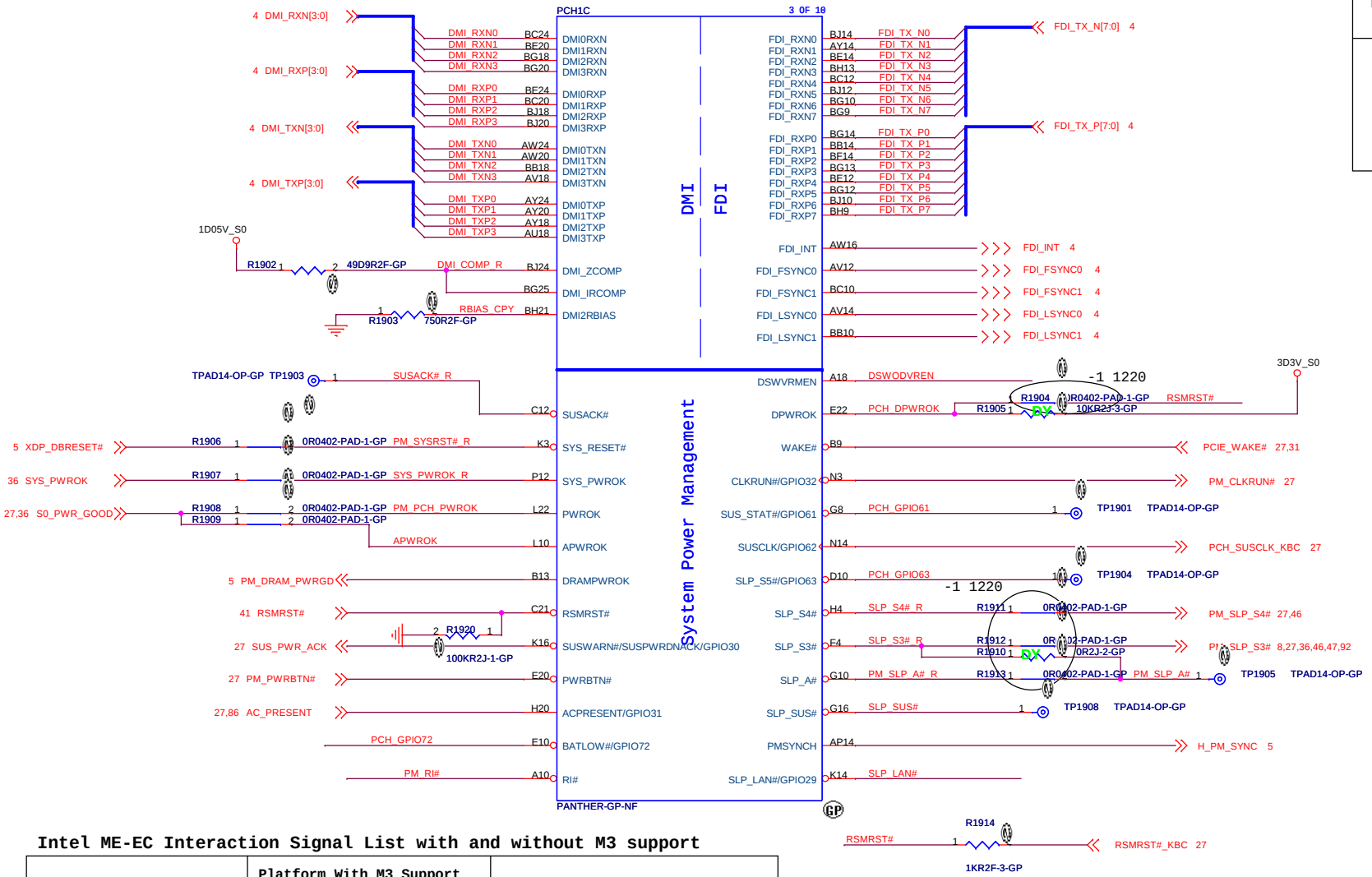
PCH(2/9)



PCH(3/9)

DSWODVREN - On Die DSW VR Enable	
HIGH (R1917 STUFFED, R1901 UNSTUFFED	Enabled (DEFAULT)
LOW (R1917 UNSTUFFED, R1901 STUFFED	Disabled





Intel ME-EC Interaction Signal List with and without M3 support

Signal Name	Platform With M3 Support (e.g., Intel AMT)	Platform Without M3 Support
SUSPWRDNACK(GPIO30)	Required	Required
ACPRESENT(GPIO31)	Required	Required
SLP_A#	Required	(Tie to SLP_S3#) Note: If SLP_S3# is not routed from PCH to EC, then SLP_A# becomes required from Intel ME-EC prespecrive.

<Core Design>

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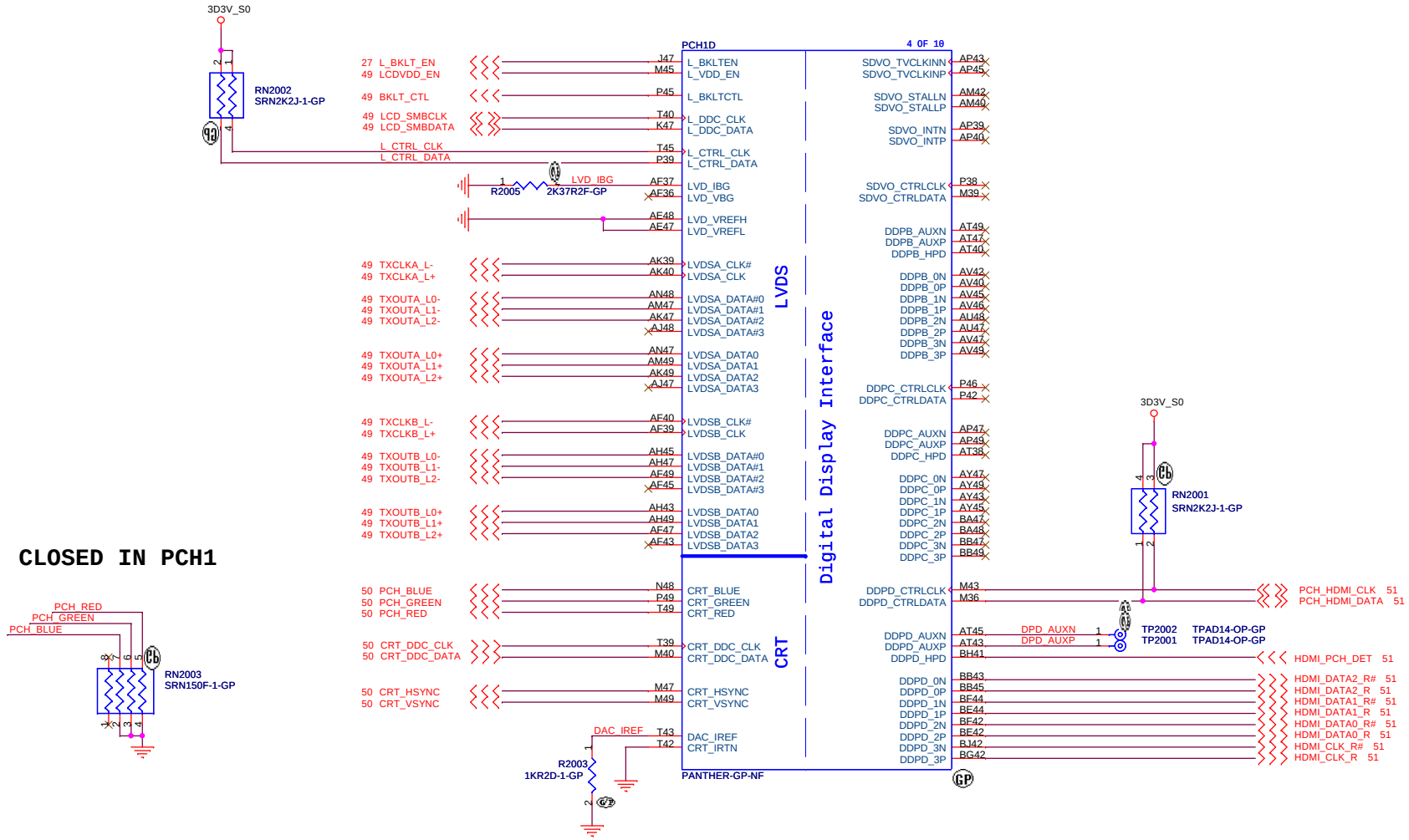
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH(3/9): DMI/FDI/PM

Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 19 of 103

PCH(4/9)



CLOSED IN PCH1

<Core Design>

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Title: **PCH(4/9): LVDS/CRT/DDI**

Size	Document Number	Rev
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Date: Wednesday, January 04, 2012 Sheet 20 of 103

PCH(5/9)

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

USB3.0 Table

USB	
Pair	Device
1	I/O CONN. 1 LEFT_DOWN
2	FREE
3	I/O CONN. 2 LEFT_UP
4	I/O CONN. 3 RIGHT_UP

USB2.0 Table

USB	
Pair	Device
0	USB 3.0 I/O CONN.
1	N/A
2	USB 3.0 I/O CONN.
3	USB 3.0 I/O CONN.
4	FREE
5	BT WLAN combo
6	FREE
7	FREE
8	Fingerprint
9	USB 2.0 CONN(Debug)
10	Camera
11	FREE
12	FREE
13	FREE

USB 3.0 Conn. 1
USB 3.0 Conn. 2
USB 3.0 Conn. 3 (UB1)
BT WLAN combo
Fingerprint
USB 2.0 Conn. 1 (UB1)
Camera
(UB2)
(UB2)

USB 3.0/2.0 Port Pairing

USB 3.0 Port	USB 2.0 Port
Port 1	Port 0
Port 2	Port 1
Port 3	Port 2
Port 4	Port 3

AND GATE

73.01G08.L04
2ND = 73.7SZ08.EAH
3RD = 73.7SZ08.DAH

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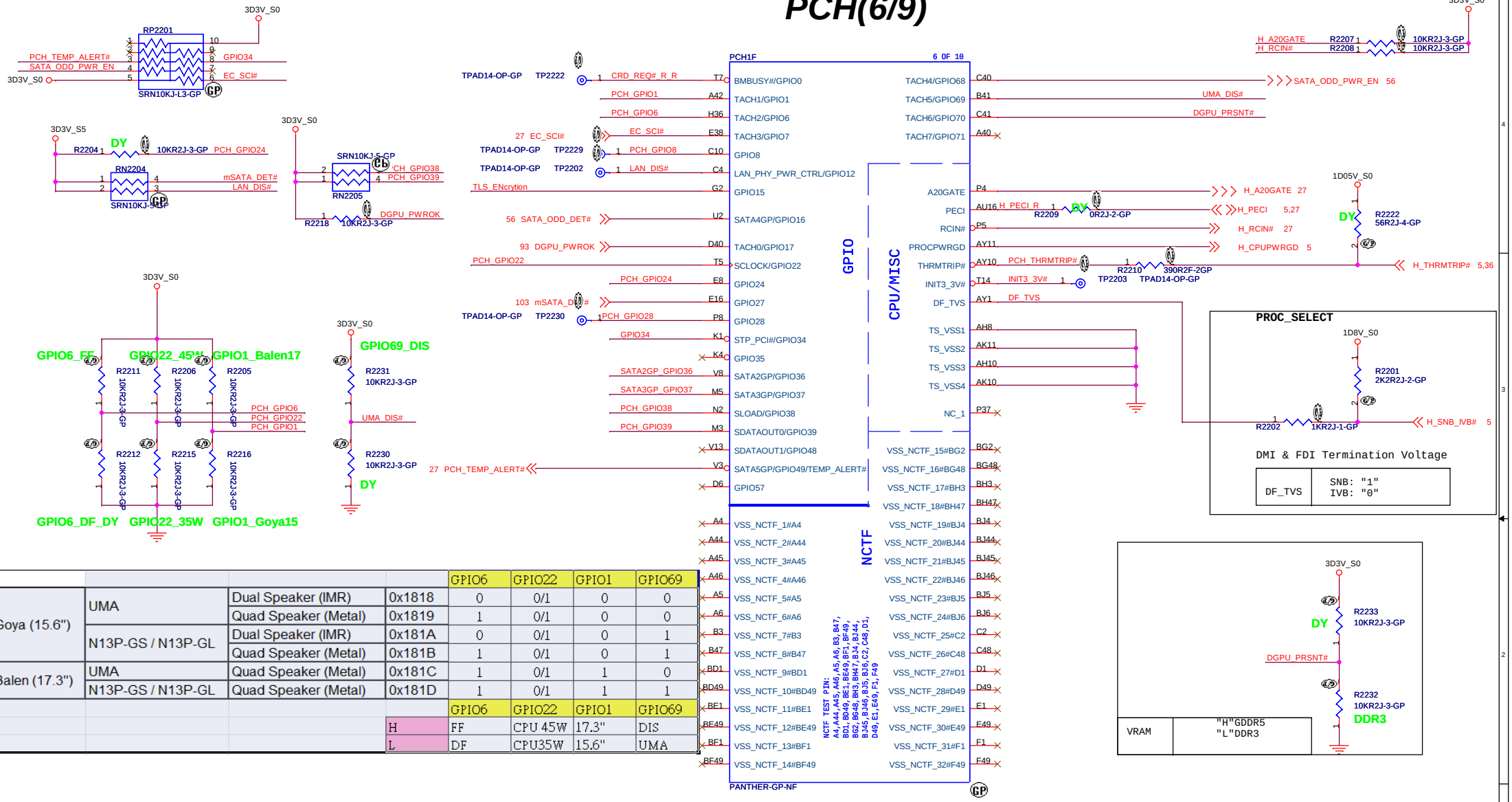
Title: PCH(5/9): PCI/USB/NVM
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 21 of 103

PCH(6/9)



PROC_SELECT

DMI & FDI Termination Voltage

DF_TVS	SNB: "1" IVB: "0"

VRAM	"H"GDDR5 "L"DDR3

				GPIO6	GPIO22	GPIO1	GPIO69
Goya (15.6")	UMA	Dual Speaker (IMR)	0x1818	0	0/1	0	0
		Quad Speaker (Metal)	0x1819	1	0/1	0	0
	N13P-GS / N13P-GL	Dual Speaker (IMR)	0x181A	0	0/1	0	1
		Quad Speaker (Metal)	0x181B	1	0/1	0	1
Balen (17.3")	UMA	Quad Speaker (Metal)	0x181C	1	0/1	1	0
	N13P-GS / N13P-GL	Quad Speaker (Metal)	0x181D	1	0/1	1	1

	GPIO6	GPIO22	GPIO1	GPIO69
H	FF	CPU 45W	17.3"	DIS
L	DF	CPU35W	15.6"	UMA

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

<Core Design>
緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

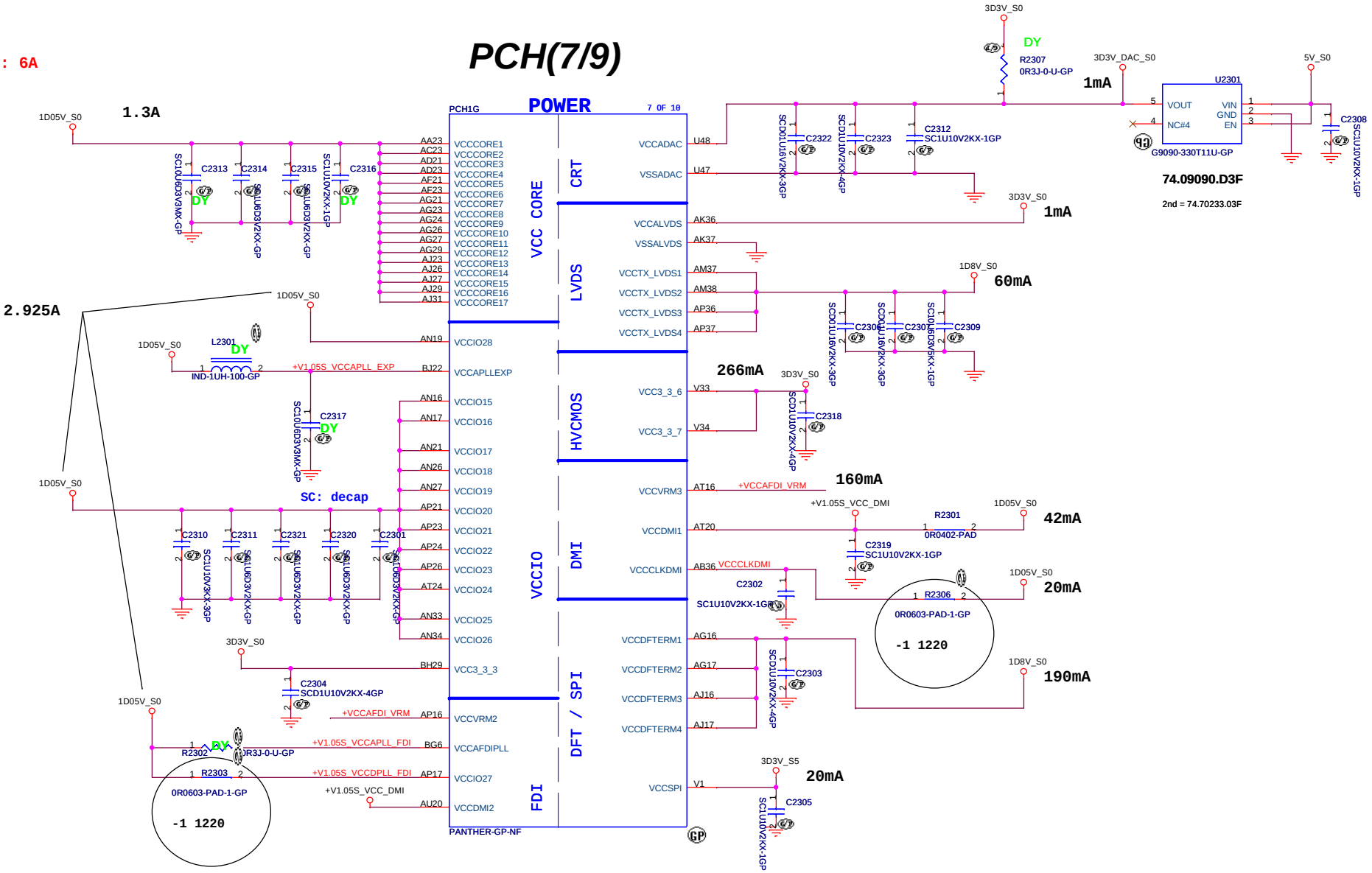
Title: PCH(6/9): GPIO/NTCF/RSVD

Size: A3 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 22 of 103

VCC_PCH: 6A

PCH(7/9)



<Core Design>

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Title: PCH(7/9): PWR1

Size	Document Number	Rev
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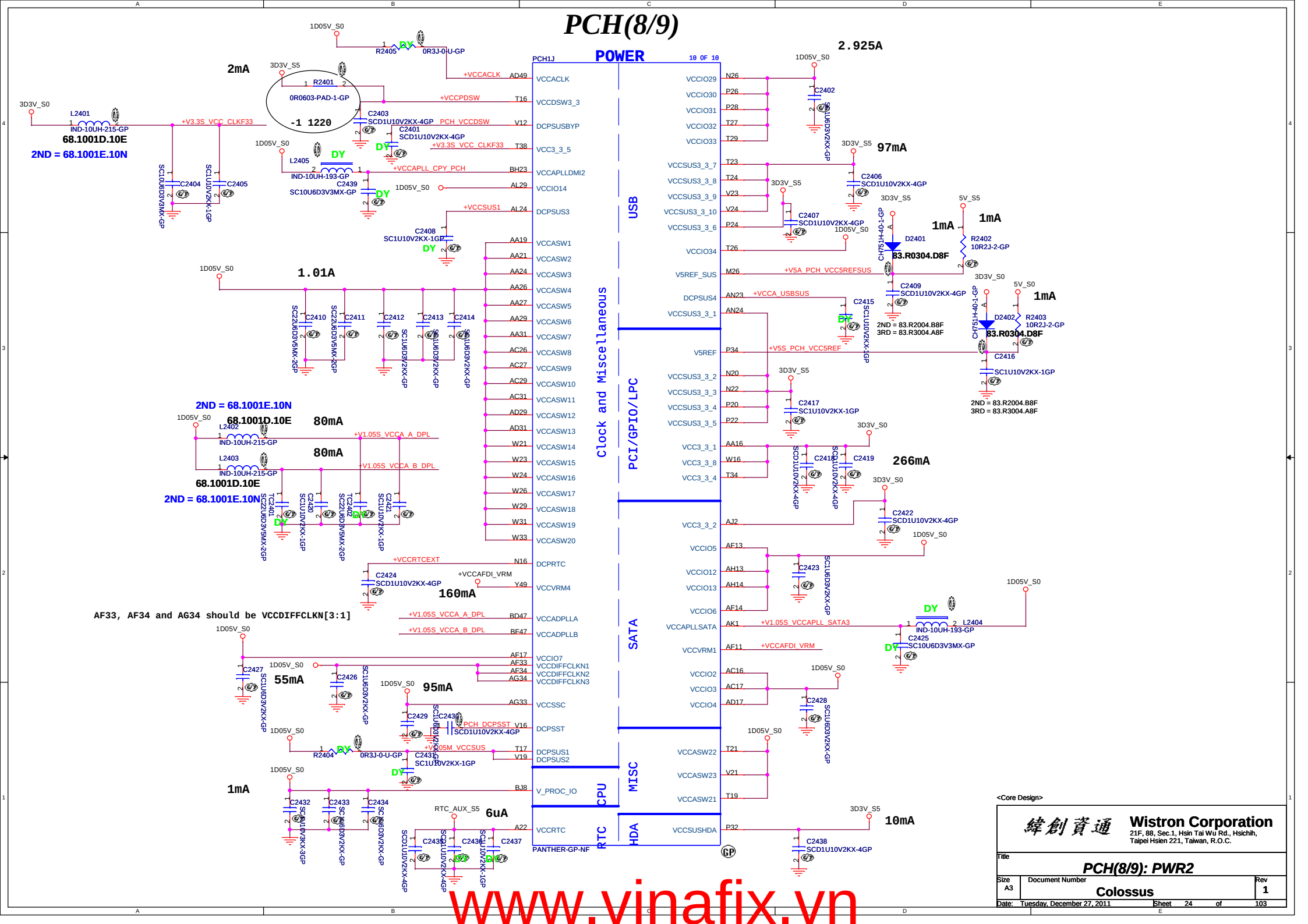
PCH(8/9)



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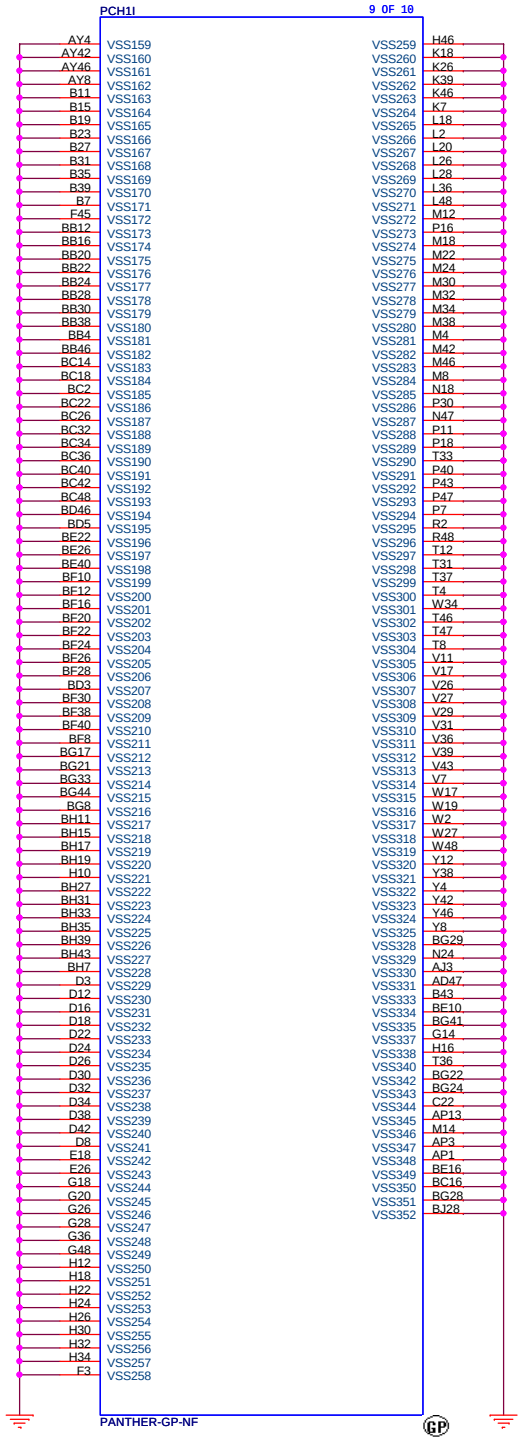
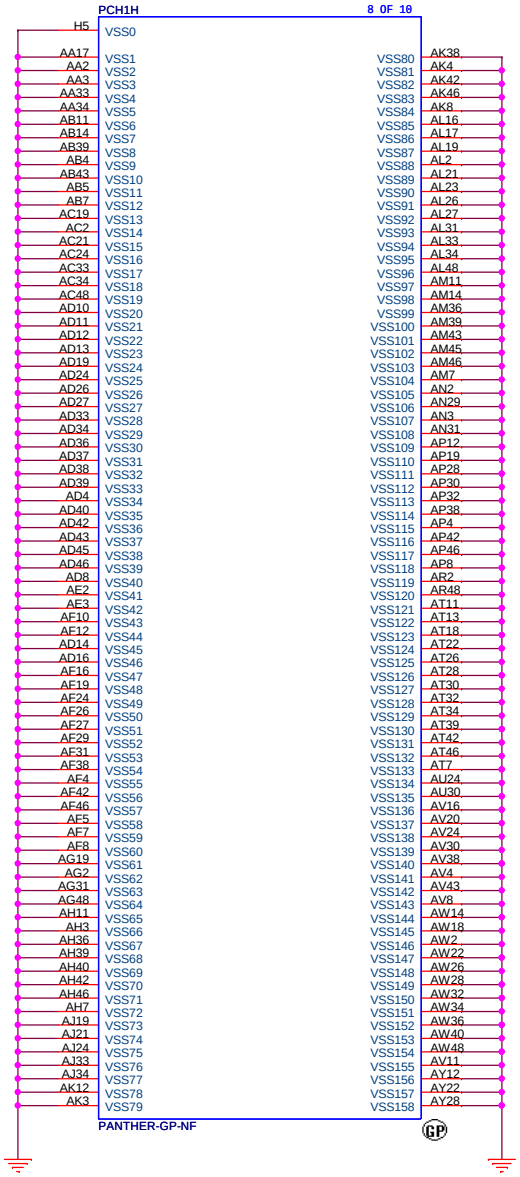
Title	PCH(8/9): PWR2	
Size: A3	Document Number: Colossus	Rev: 1
Date: Tuesday, December 27, 2011	Sheet 24 of 103	

<Core Design>

PCH(9/9)





<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***PCH(9/9): GND***

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A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 25 of 103

(Blanking)

<Core Design>

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Title: PCH XDP

Size	Document Number	Rev
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SSID = KBC

U2701

KB9016QF-A3-GP

71.09016.B0G

20110608 for vendor debug

PCB VERSION

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K	10.0K	3.0V
SB	100.0K	20.0K	2.75V
SC	100.0K	33.0K	2.48V
SD	100.0K	47.0K	2.24V
-	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V

01/05/12 PCB_1

83.00355.F1F

MODEL ID

Model_ID	Model_ID (SI2)	Model_ID (SI2)	Pull-Low Register	Pull-High Register	Typical Voltage
Goya(15.6")	UMA	UMA (35W)	100.0 K	10.0 K	3.000 V
	UMA	UMA (45W)	100.0 K	20.0 K	2.750 V
Goya(15.6")	DIS	DIS GL (35W)	100.0 K	33.0 K	2.481 V
	DIS	DIS GL (45W)	100.0 K	47.0 K	2.245 V
Balen(17.3")	UMA	UMA (35W)	100.0 K	64.9 K	2.001 V
Balen(17.3")	DIS	DIS GL (35W)	100.0 K	76.8 K	1.867 V
Balen(17.3")		DIS GL (45W)	100.0 K	100.0 K	1.650 V
Balen(17.3")	eserved for project u	DIS GT (35W)	100.0 K	143.0 K	1.358 V
Balen(17.3")	eserved for project u	DIS GT (45W)	100.0 K	174.0 K	1.204 V
Balen(17.3")	eserved for project u	UMA (45W)	100.0 K	215.0 K	1.048 V
Goya(15.6")	eserved for project u	DIS GT (35W)	100.0 K	237.0 K	0.979 V
Goya(15.6")	eserved for project u	DIS GT (45W)	100.0 K	261.0 K	0.914 V

Prevent BIOS data loss solution

Q2701 MMBT3906-4-GP
84.T3906.A11
2nd = 84.03906.F11

GPIO06-->PWRBTN

HP Limit Signal Detect

D2701 BAV99PT-GP-U

83.00099.K11
2ND = 83.00099.M11
3RD = 83.00099.T11

HP AIRLINE COMBO

EC GPIO standard PH/PL

RN2701 SRN4K7J-8-GP

RN2713 pull-Low 10K Resistor to DY on BLUETOOTH_EN.

GPIO70-->PWR_CHG_ACOK# OW active

For EC power consumption reserver

3RD = 84.2N702.W31
2ND = 84.07002.I31
84.2N702.J31
Q2703 2N7002K-2-GP

<Core Design>
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Title: EC CONTROLLER

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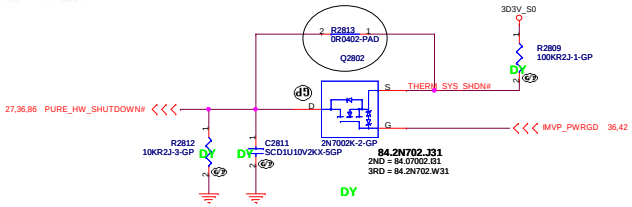
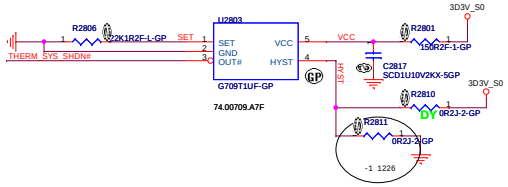
$R_{SET}(k\Omega) = 0.0012T^2 - 0.9308T + 96.147$

where T is the trip temperature in Centigrade. R_{SET} is the set- point resistance.



90 C



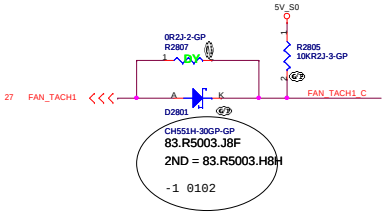
Global Mixed-mode Technology Inc.

G709/G710

Pin Description

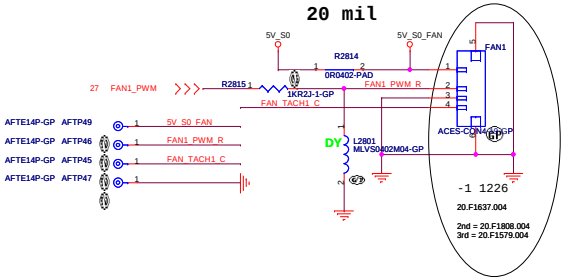
PIN		NAME	FUNCTION
G709	G710		
1	1	SET	Temperature Set Point, Connect an external 1% resistor from SET to GND to set trip point.
2	2	GND	Ground
3	3	$\overline{OT}$	Open-Drain Active Low Output.
4	4	HYST	Hysterisis Selection. Hysterisis is 10°C for HYST = V_{CC}, 2°C for HYST = GND.
	5	N.C.	Not Connected.
5	6	VCC	Power-Supply Input.

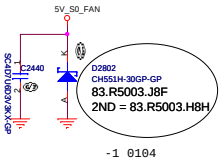
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
HYST Input Threshold	V_{IH}		0.7 x V_{CC}	---	---	V
	V_{IL}		---	---	0.3 x V_{CC}	V



FOR PWM FAN

20 mil





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/FAN

Size: A2 | Document Number: Colossus | Rev: 1

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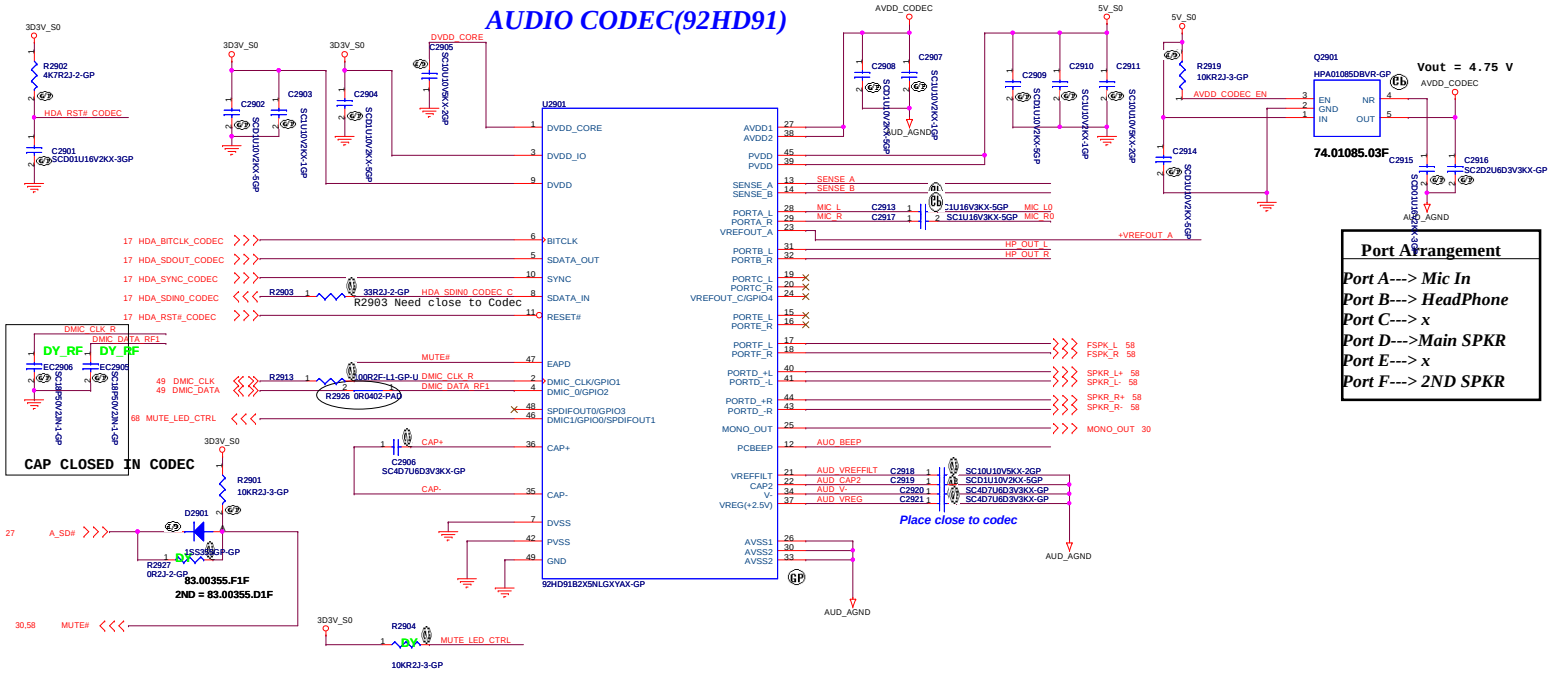
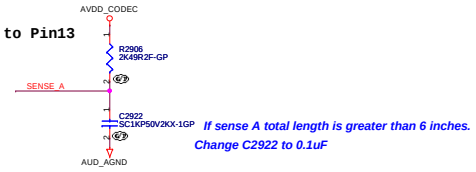
AUDIO CODEC(92HD91)



SENSE Detect

Headphone Trace = 15mil

Close to Pin13



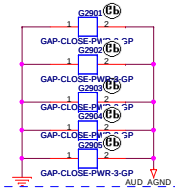
If sense A total length is greater than 6 inches.
Change C2922 to 0.1uF

Close to Pin14

Digital GND & AUD_AGND

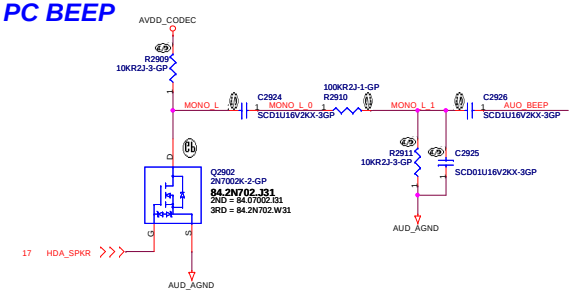
Tie Analog GND and Digital GND under codec by a single point

0818 IDT request
Place under U2901



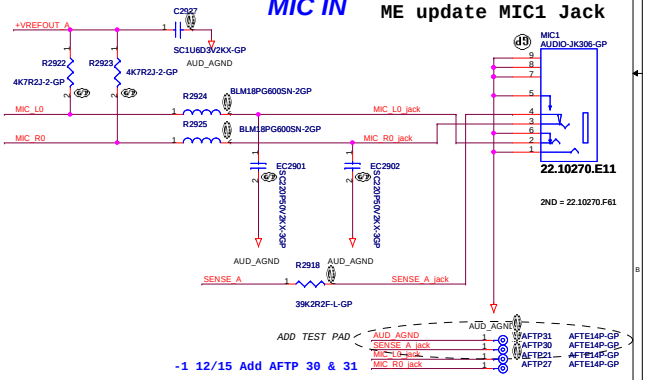
audio ground must be connect to digital ground with an 80 mil copper bridge located directly under codec to prevent ESD latch up.

PC BEEP



MIC IN

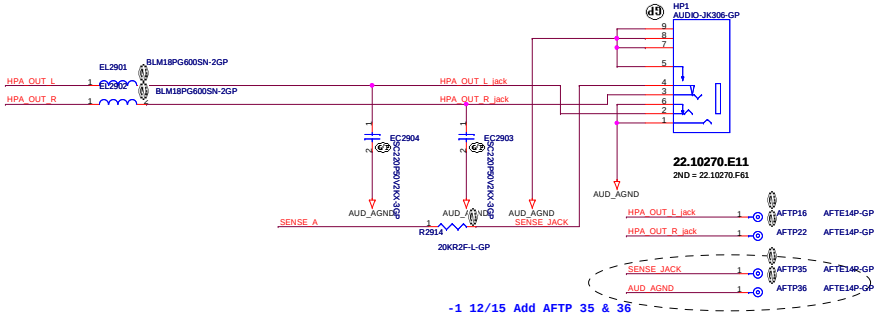
ME update MIC1 Jack



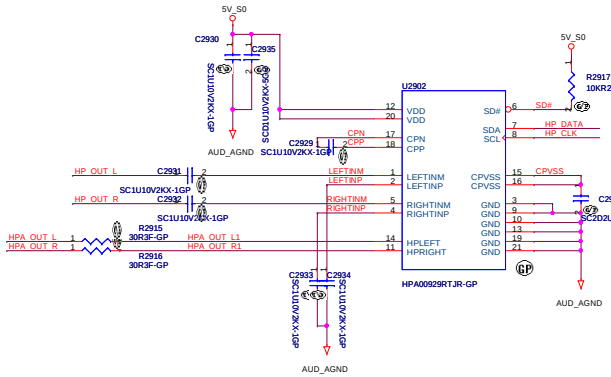
-1 12/15 Add AFTP 30 & 31

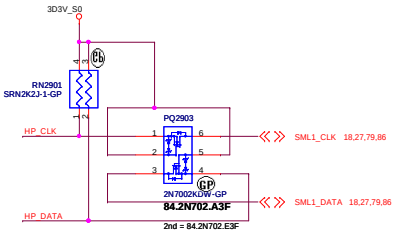
HeadPhone

ME update HP1 Jack



-1 12/15 Add AFTP 35 & 36





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Audio Codec 92HD91/HeadphoneAMP

Size	Document Number	Rev
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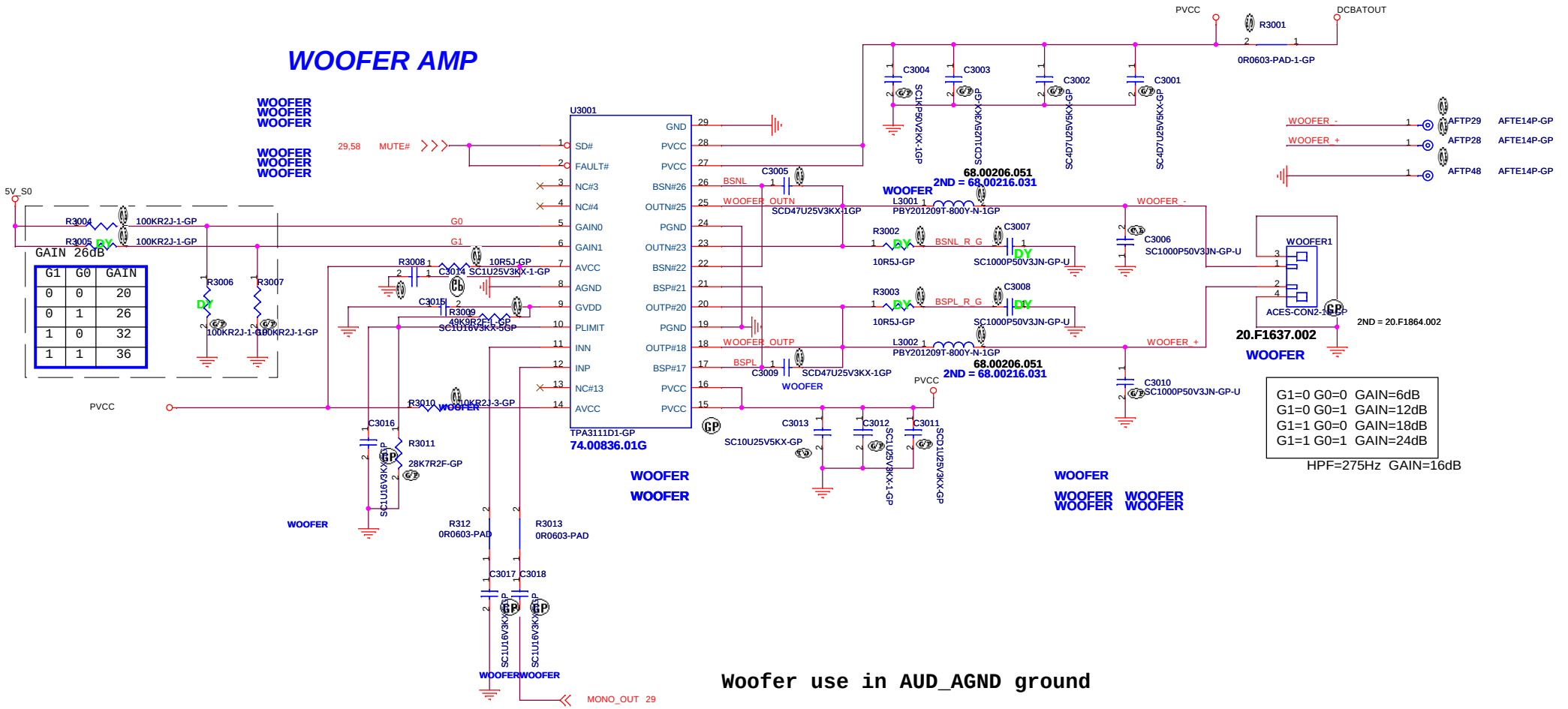
WOOFER AMP



Woofer use in AUD_AGND ground

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP SPK/WOOFER***

Size	Document Number	Rev
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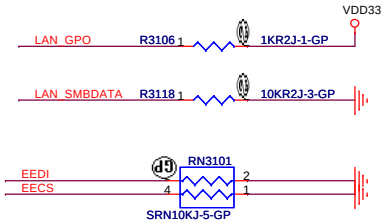
Date: Wednesday, January 04, 2012 Sheet 30 of 103

LAN CHIP-RTL8111F

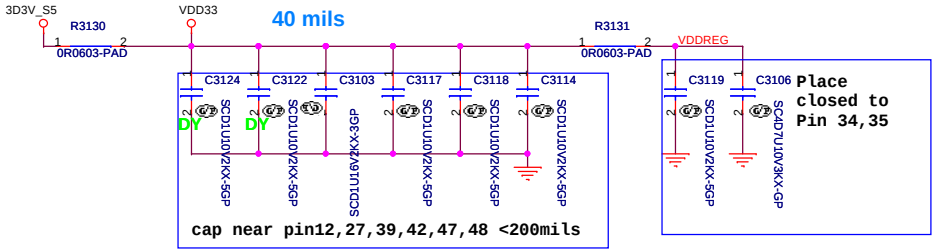
USE EFuse No ASF

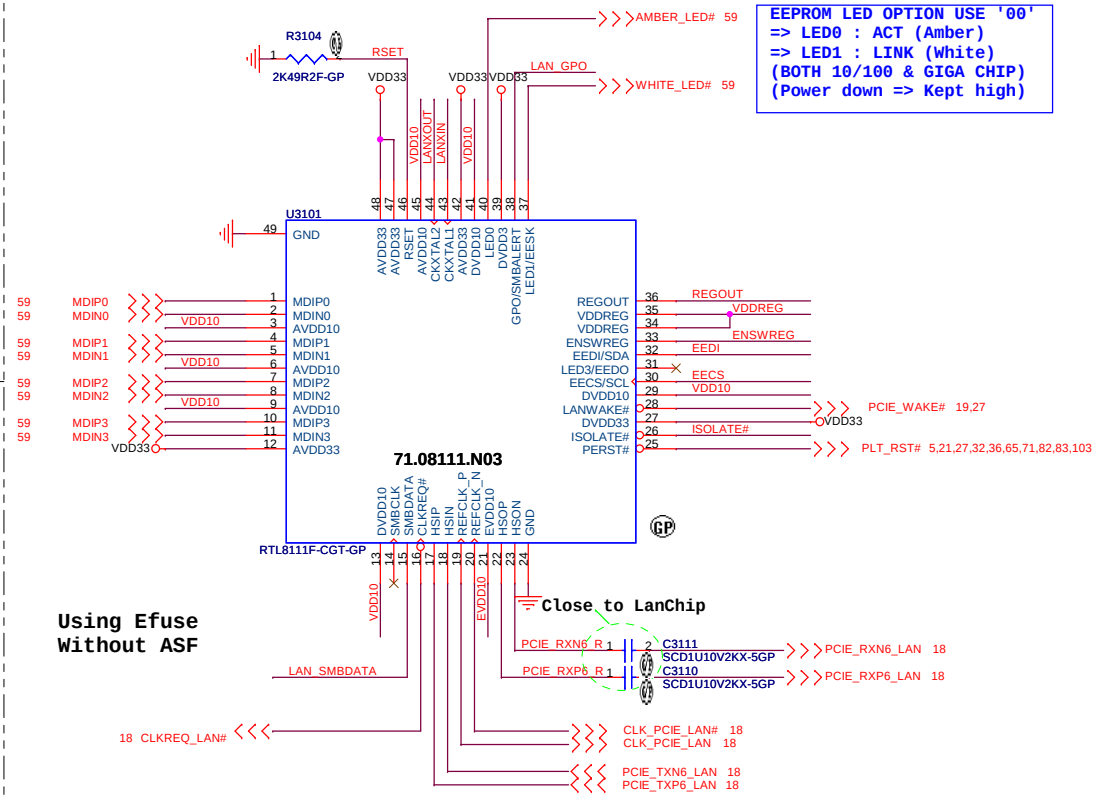


Avoid Leakage

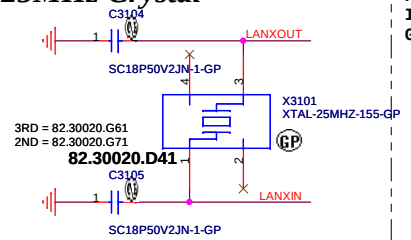
LanChip Power

+3.3V_LAN_S5 Rising time (10%~90%)
Spec >1mS and <100mS



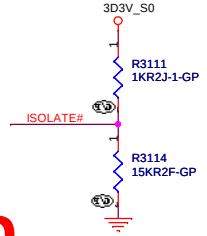


25MHz Crystal

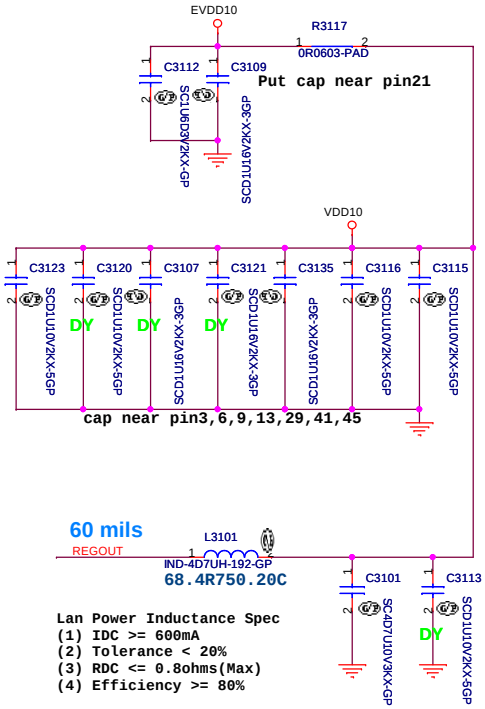


KBC Reserved Pin
Isolate# => Low , Isolate LanChip
GPO => EFuse Strap Pin

Isolate Strap Pin

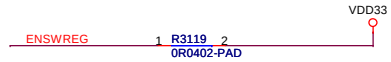


Regout power plane(1D05V)



Put 4D7U L + 22U cap near pin36 <200mils
(2nd = 78.22610.81L)

Regout Switch



ENSWREG (REGOUT 1D05V)
PH = Enable
PL = Disable

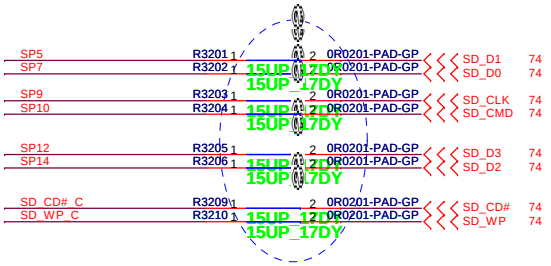
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN_RTL8111F
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 31 of 103

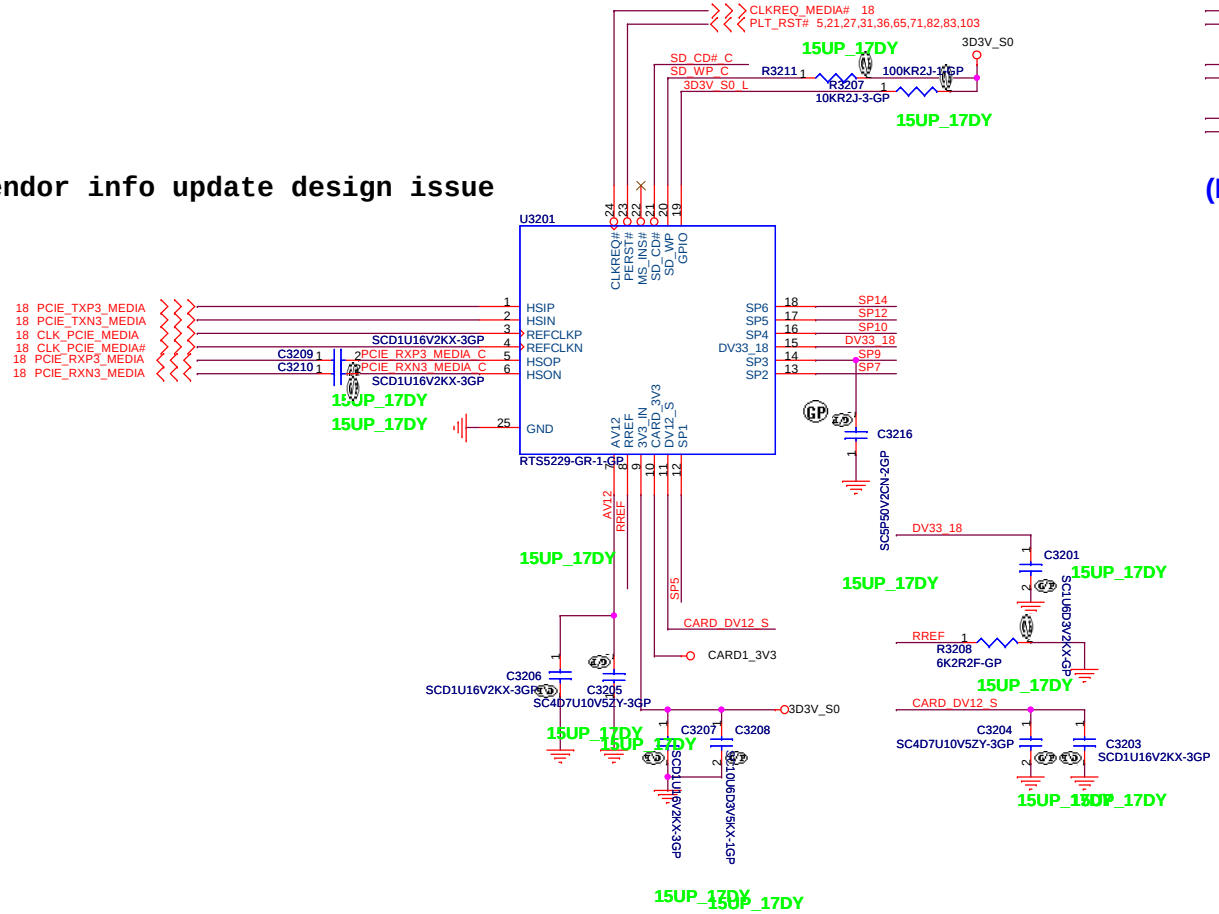
RTS5229

-1 12/15 0201 0 Ohm change to short pad



Vendor info update design issue

(RTS5229)U3201 closed near



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5229

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 32 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title 1394

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 33 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 34 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 35 of 103

Power Sequence

R3614
CRB 1K

28,42 IMVP_PWRGD — R3614 0R0201-PAD-GP — SYS_PWROK — SYS_PWROK 19

19,27 S0_PWR_GOOD — D3603 BAS16-6-GP

C3612 SCD01U50V2KX-1GP DY

83.00016.K11
2ND = 83.00016.F11

R3623 0R0402-PAD

5,46,47 RUNPWROK
8,19,27,46,47,92 PM_SLP_S3#

U3608 74LVC1G08GW-1-GP (B, A, GND, VCC, Y) — 3D3V_S5

PWR_1D05V_1V_EN 45

73.01G08.L04
2ND = 73.7SZ08.DAH

DY

ANNIE Run Power

Run power follow TOP-1

DCBATOUT

R3619 330KR2J-L1-GP

RUN_ENABLE — R3622 0R0402-PAD

D3602 MMPZ5239BPT-GP
83.9R103.D3F
2ND = 83.9R103.F3F

R3618 470R2J-2-GP

RUN_PWR_ON_G

C3615 SCD01U50V2KX-1GP
78.10324.2FL

3D3V_AUX_S5 — R3612 100KR2J-1-GP

8,19,27,46,47,92 PM_SLP_S3# — Q3603 DMN66D0LDW-7-GP
84.DMN66.03F

PS_S3CNTRL

0D75V_S0 — R3621 22R2J-2-GP — Q3604 DMN66D0LDW-7-GP
84.DMN66.03F

R3620 220R2F-GP — 1D5V_S0

5V_S0 — C3607 SCD1U25V2KX-GP DY — U3604 QM3004M3-GP — 5V_S5

C3608 SCD1U25V2KX-GP DY

84.30043.037
2nd = 84.02657.037

3D3V_S0 — C3616 SCD1U25V2KX-GP DY — U3607 QM3004M3-GP — 3D3V_S5

C3609 SCD1U25V2KX-GP DY

84.30043.037
2nd = 84.02657.037

1D5V_S0 — C3611 SCD1U25V2KX-GP DY — U3605 TPCA8062-H-GP — 1D5V_S3

C3610 SCD1U25V2KX-GP DY

84.08062.037
2ND = 84.00460.037

-1 0103 check Power list

5V_S0 — C3613 SCD1U10V2KX-5GP

5V_S5 — C3614 SCD1U10V2KX-5GP

5V_S0 — R3624 1KR2J-1-GP — Q3605 2N7002K-2-GP

PS_S3CNTRL

1D5V_S0

MAX Current 3000 mA
Design Current 2100 mA

Total= 11.39A

H_THRMTRIP# 5,22

MMBT2222ALT1G-GP Q3601
84.02222.X11
2ND = 84.02222.V11

H_PWRGD_R — C3602 SCD1U10V2KX-5GP

5,21,27,31,32,65,71,82,83,103 PLT_RST# — R3616 4K7R2J-2-GP

R3632 2K2R2J-2-GP

83.R0304.D8F
2ND = 83.R2004.B8F
3RD = 83.R3004.A8F

41 3V_5V_EN — D3601 CH751H-40-1-GP

R3603 2KR2F-3-GP — PURE_HW_SHUTDOWN# 27,28,86

S5_ENABLE 27

R3602 200KR2J-L1-GP DY

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 36 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

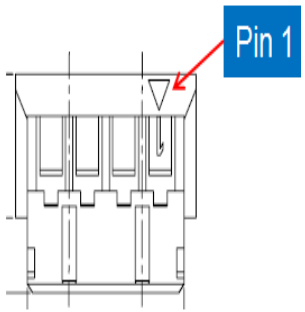
Title: ADAPTER

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 37 of 103

Adaptor in to generate DCBATOUT

Pin	Description	Wire color
Pin 1	White LED	White
Pin 2	Amber LED	Yellow
Pin 3	ID	Brown
Pin 4	GND	Black
Pin 5	GND	Black
Pin 6	GND	Black
Pin 7	-	
Pin 8	+VA	Red
Pin 9	+VA	Red
Pin 10	+VA	Red



-1 1222 PR3802 to save 100mW when battery full.

AC Present = White
Standby = White pulsing
Charging = Amber
***LED's are off if no AC jack pluged in**

-1 1222 PR3802 to save 100mW when battery full.

<Core Design>

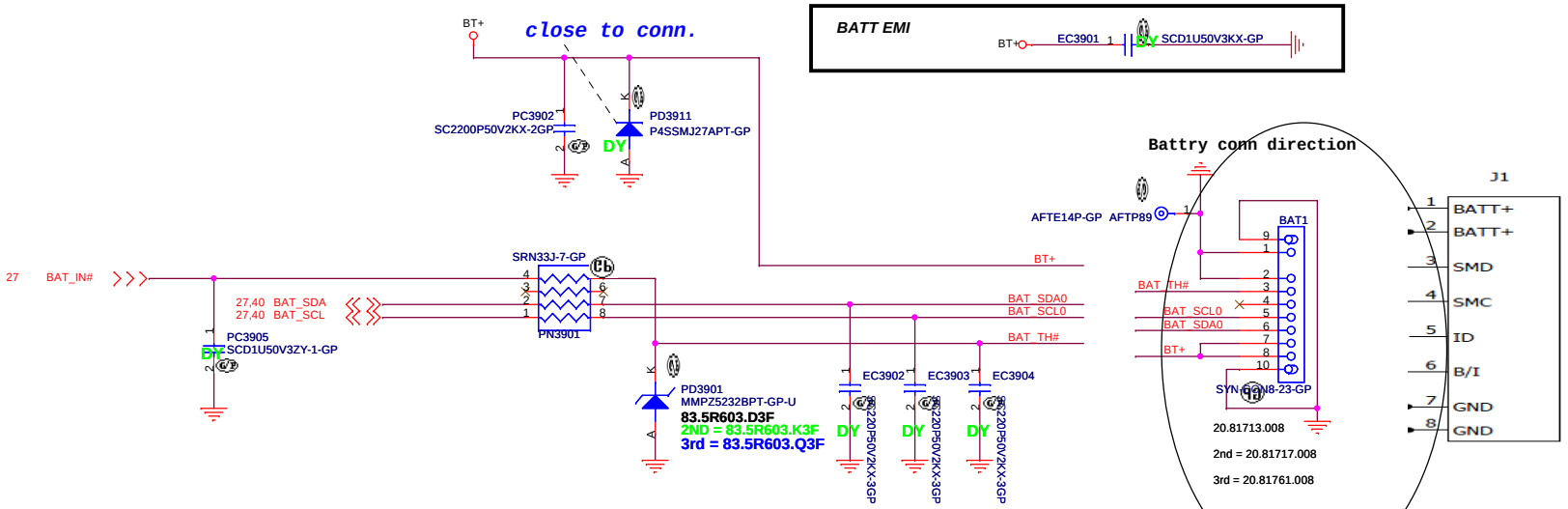
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

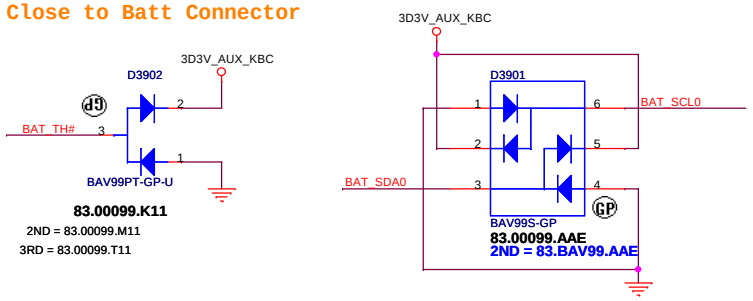
Title: DCIN JACK

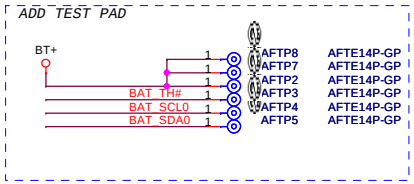
Size: A4 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 38 of 103

BATT Connector



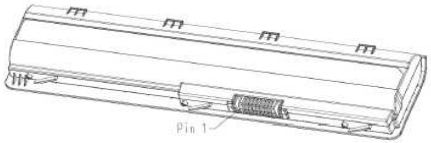




3. Interface

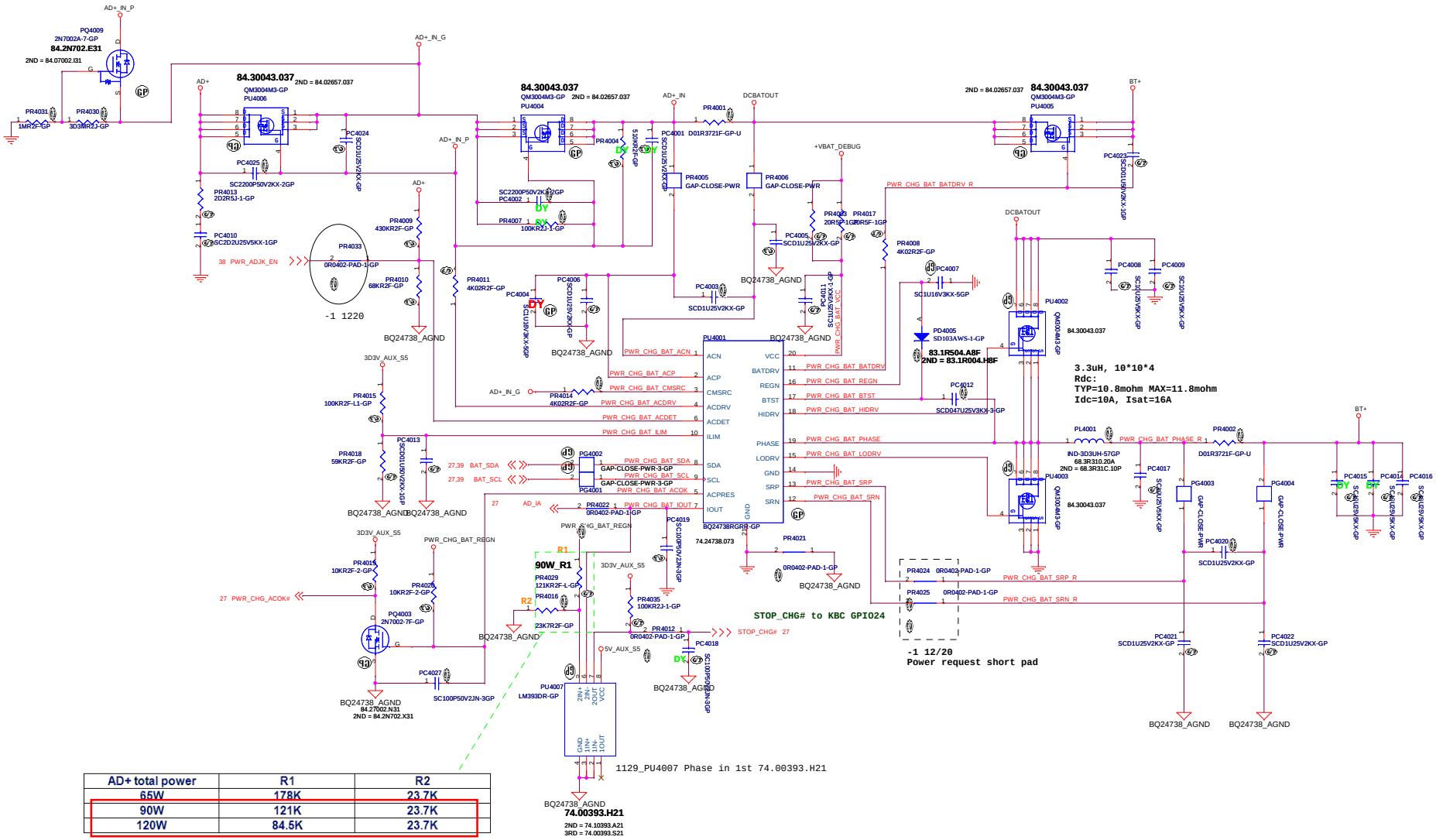
Connector ; 8pin
(Alltop C19029-10803-B, Foxconn BR0208C-B61H5-4H, Octek BTK-08ABEB)

Pin No.	Symbol	Description
1	BATT+	Batt+, Battery Positive Terminal
2	BATT+	Batt+, Battery Positive Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	ID	Open
6	B/I	Connect to thermistor (103AT2 equivalent)
7	GND	Batt-, Battery Negative Terminal
8	GND	Batt-, Battery Negative Terminal



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 39 of 103



AD+ total power	R1	R2
65W	178K	23.7K
90W	121K	23.7K
120W	84.5K	23.7K

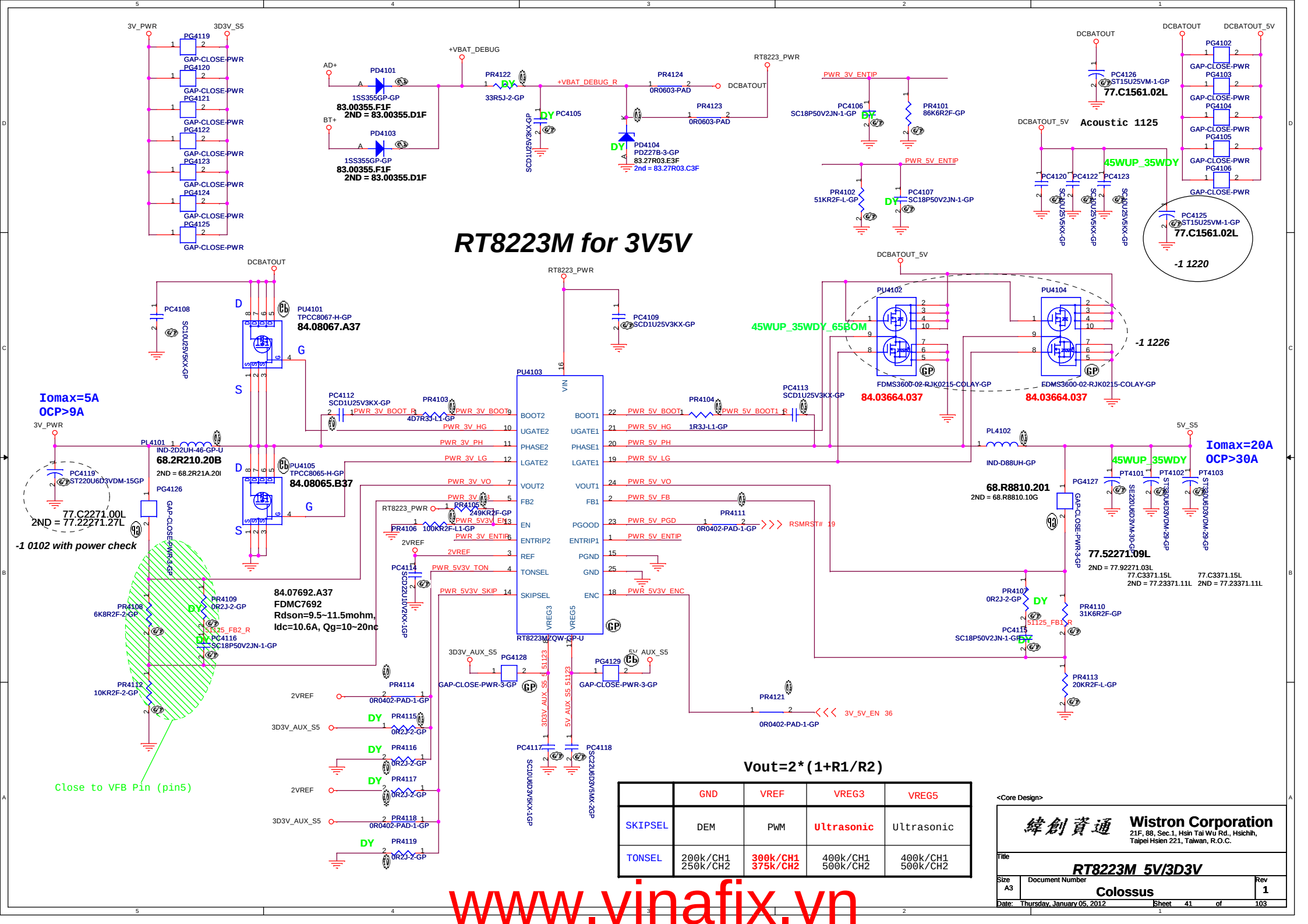
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Charger_BQ24738

Size: A2 | Document Number: Colossus | Rev: 1

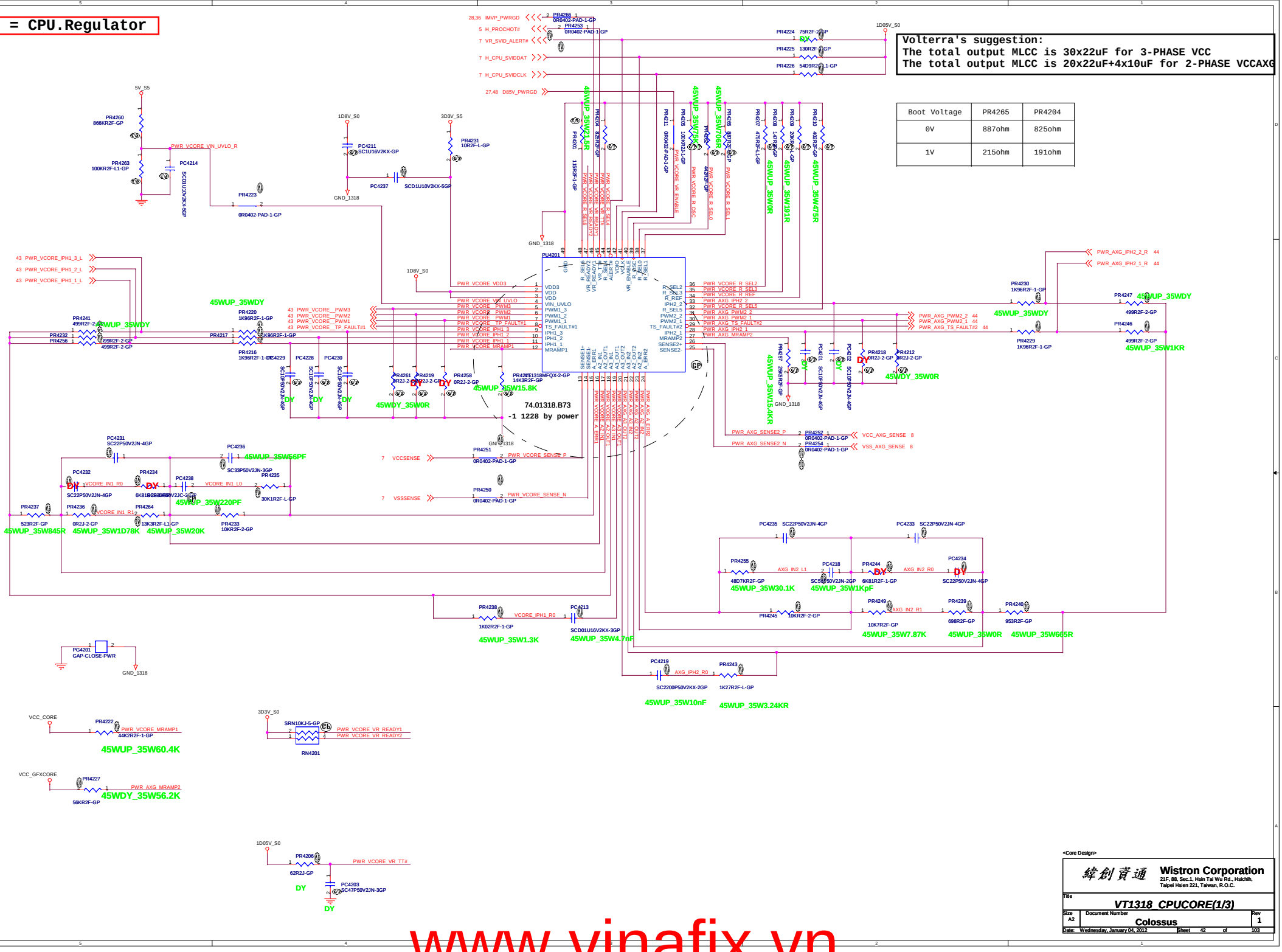
Date: Thursday, January 05, 2012 | Sheet 40 of 103


RT8223M for 3V5V
Iomax=5A
OCP>9A
Iomax=20A
OCP>30A
Vout=2*(1+R1/R2)
SKIPSEL | GND | VREF | VREG3 | VREG5
TONSEL | 200k/CH1 250k/CH2 | 300k/CH1 375k/CH2 | 400k/CH1 500k/CH2 | 400k/CH1 500k/CH2
Close to VFB Pin (pin5)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
RT8223M 5V/3D3V
Colossus
Thursday, January 05, 2012
www.vinafix.vn

SSID = CPU.Regulator

Volterra's suggestion:
The total output MLCC is 30x22uF for 3-PHASE VCC
The total output MLCC is 20x22uF+4x10uF for 2-PHASE VCCAXG

Boot Voltage	PR4265	PR4204
0V	887ohm	825ohm
1V	215ohm	191ohm



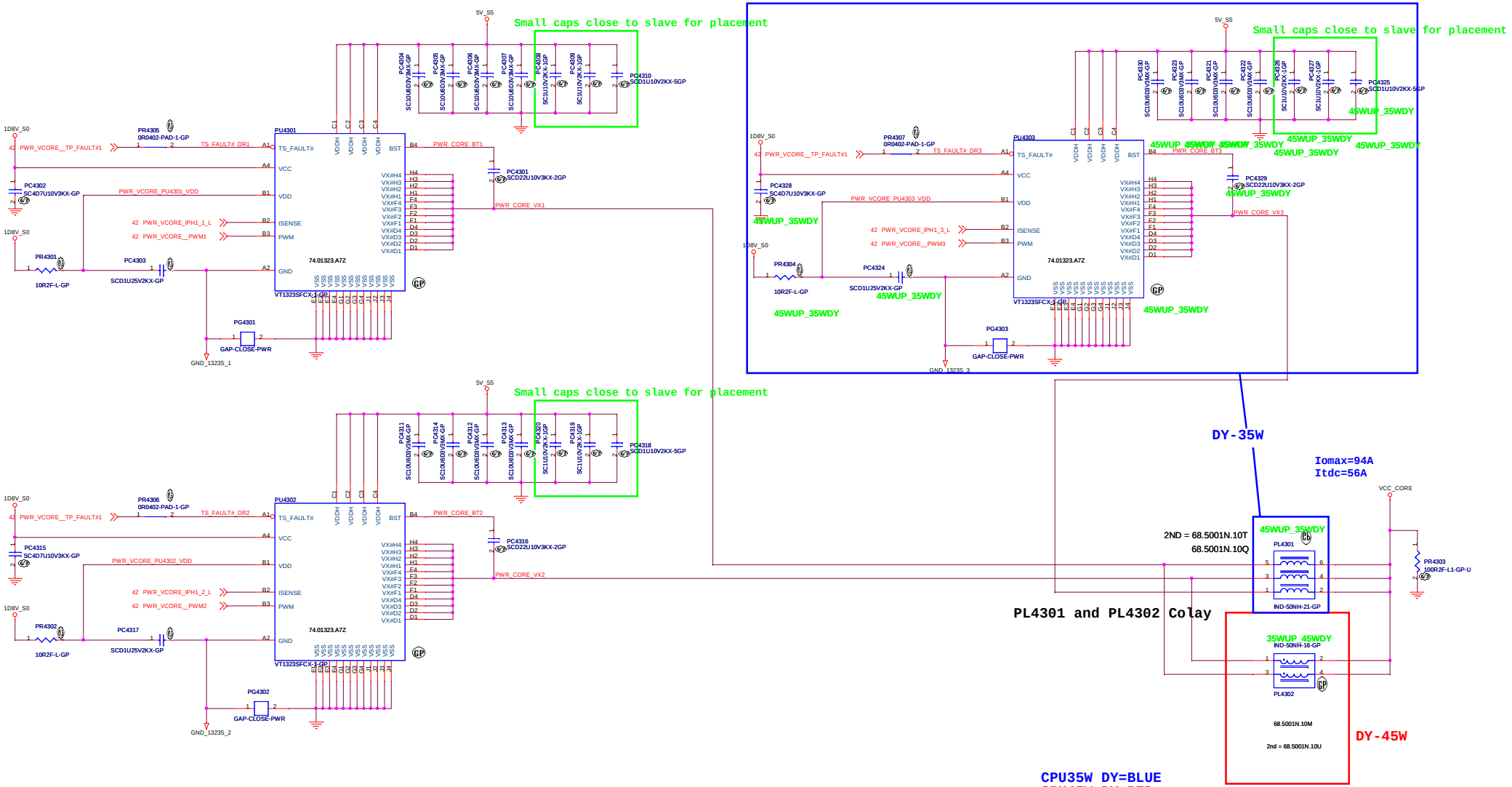
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1318_CPUCORE(1/3)

Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 42 of 103



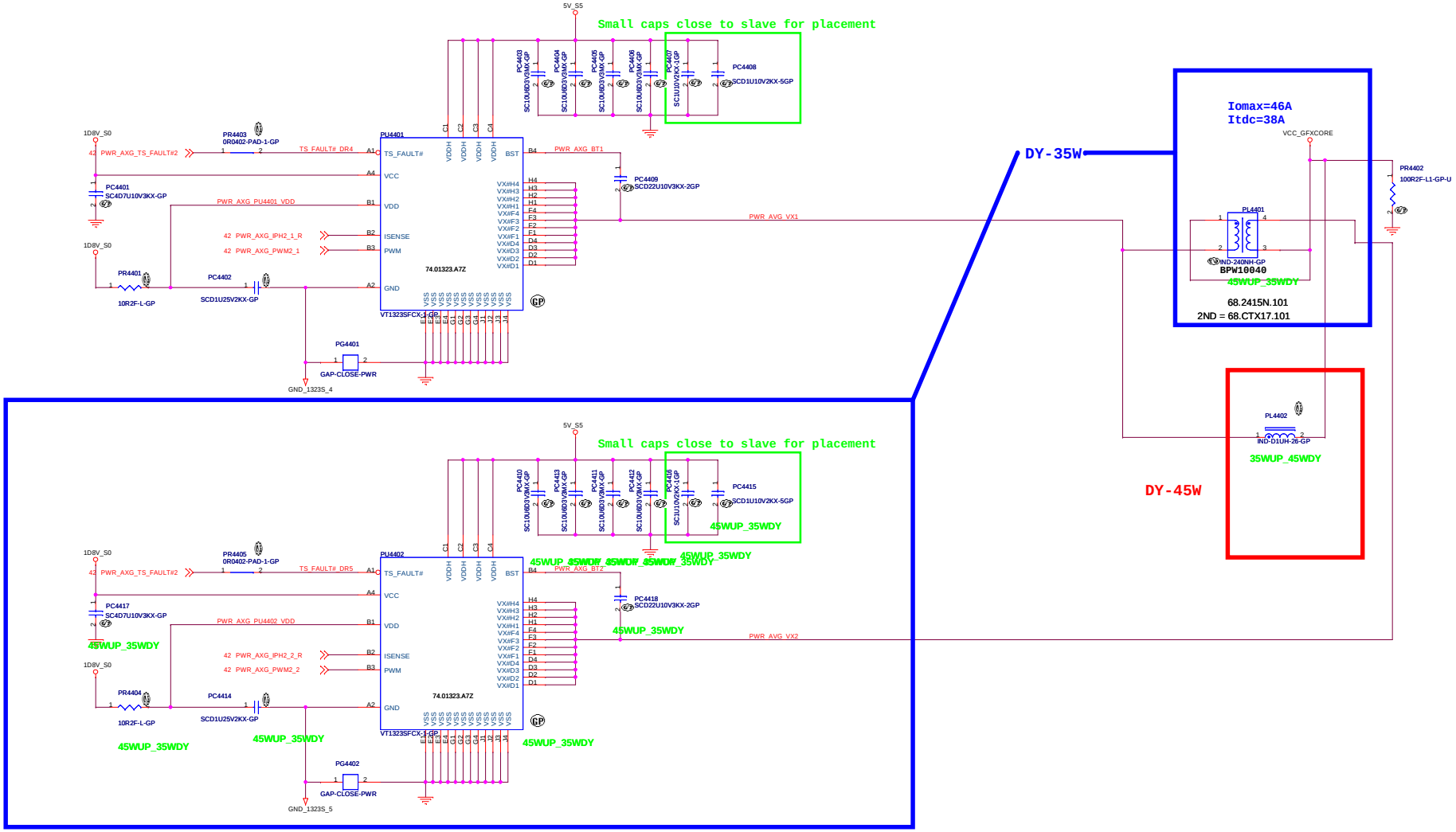
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1323_CPUCORE(2/3)

Size: A2 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 43 of 103



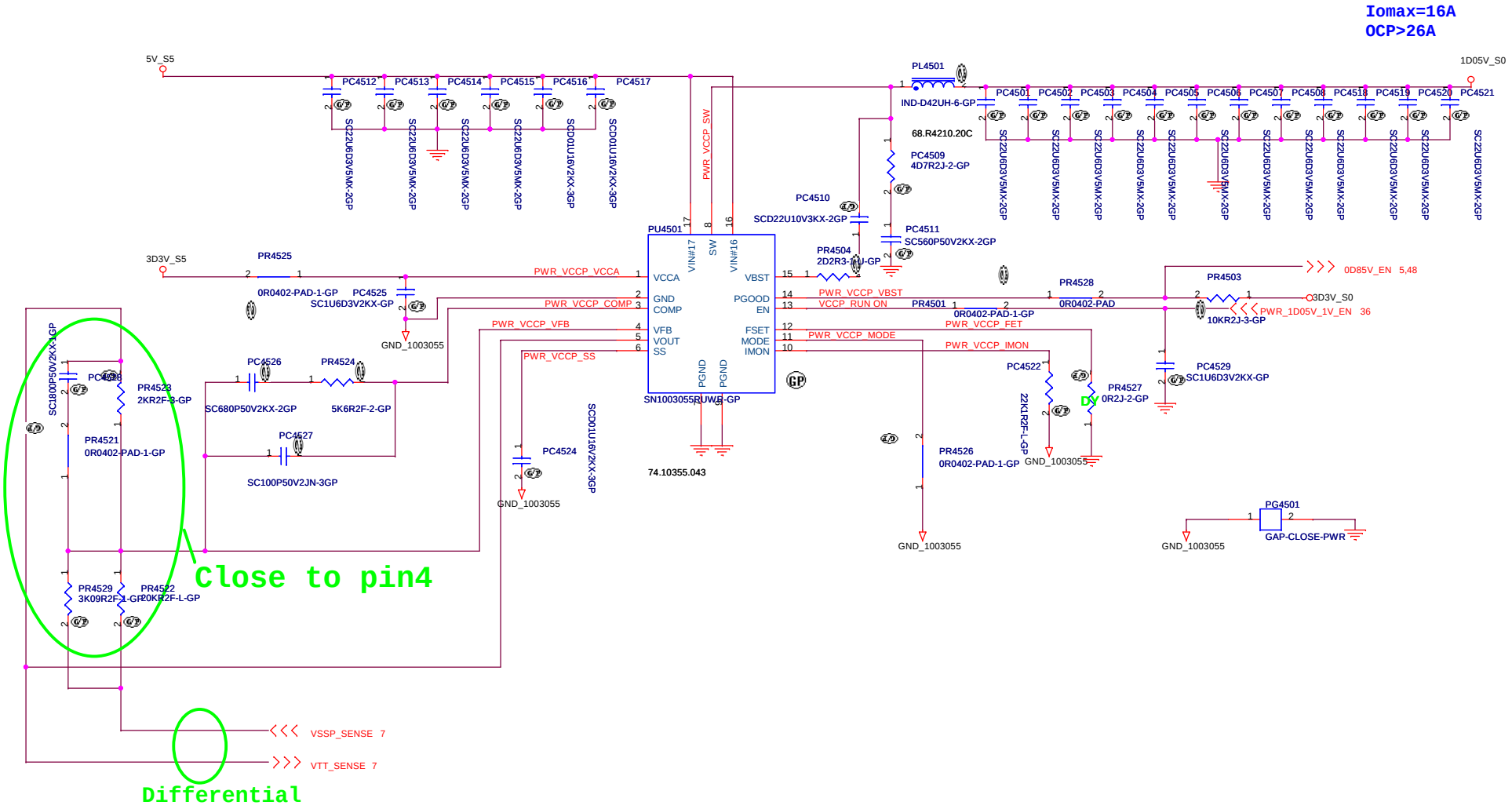
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1323_CPUCORE(3/3)

Size	Document Number	Rev
A2	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 44 of 103



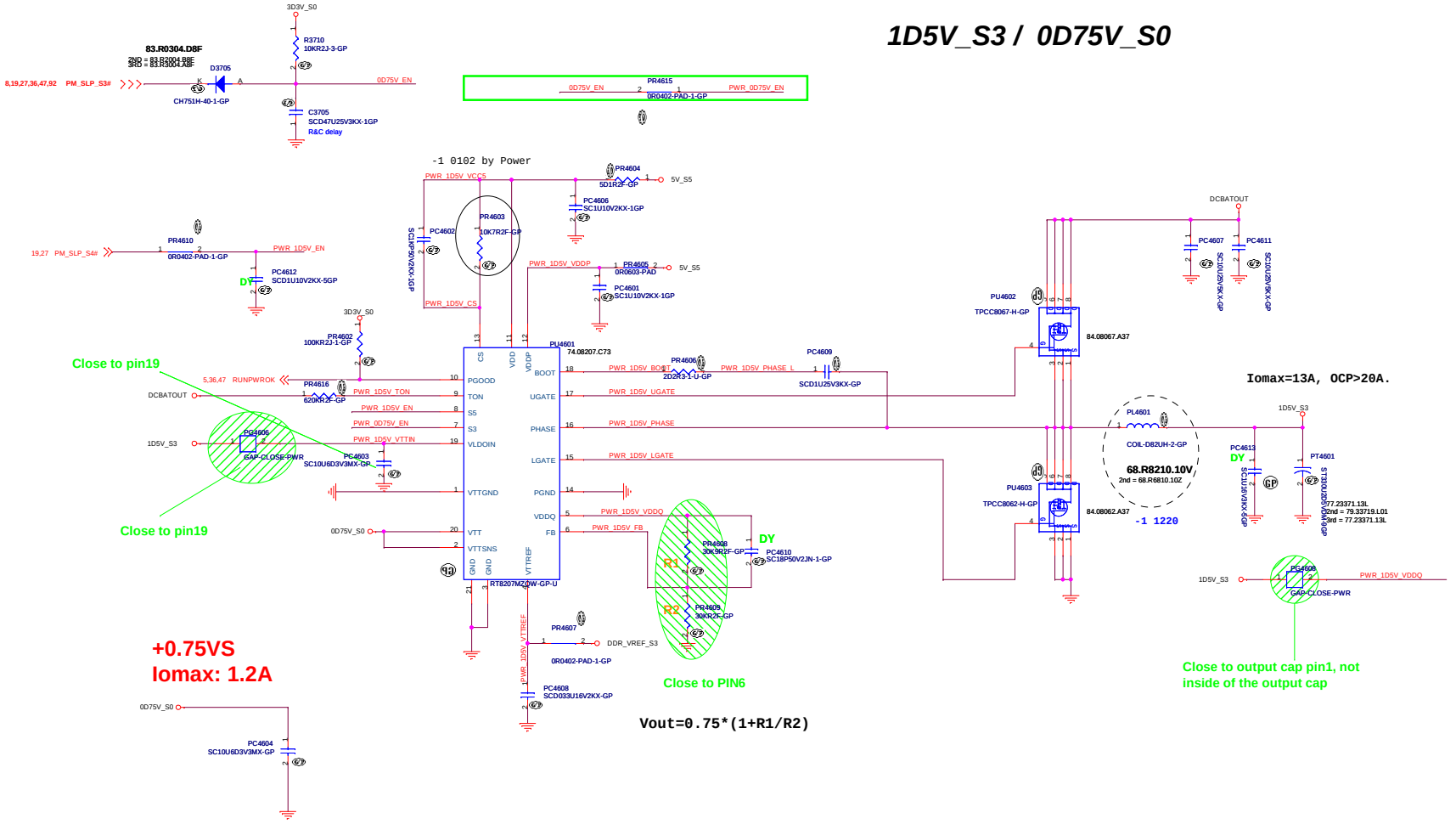
<variant_name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SN1003055RUWR		
Size: A3	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 45 of 103	

SSID = PWR.Plane.Regulator_1p5v0p75v

⑤

1D5V_S3 / 0D75V_S0



<Core Design>

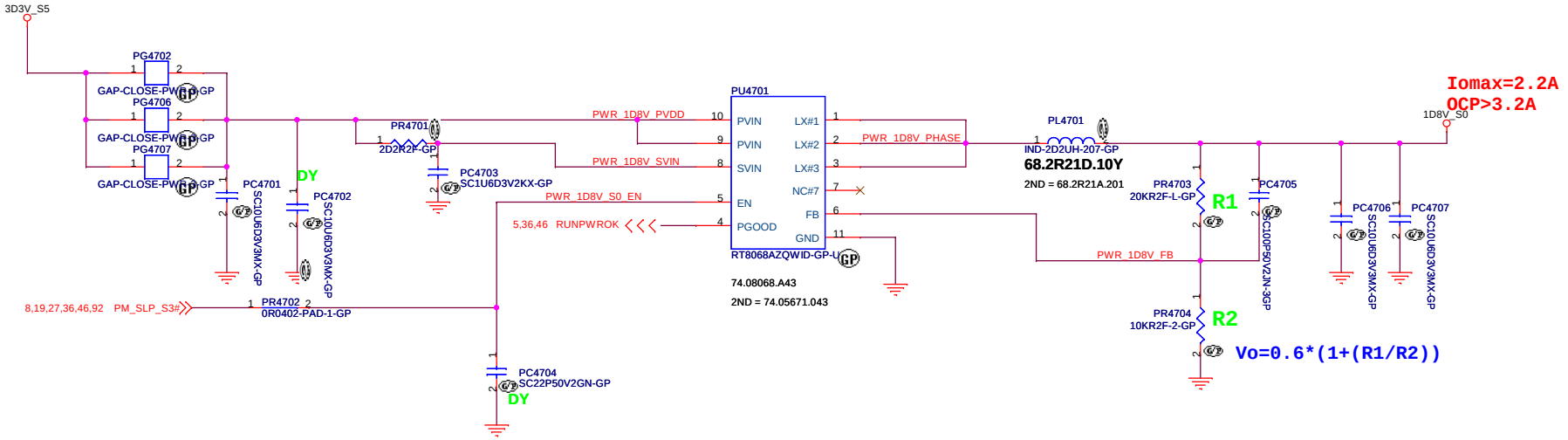
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8207MZ_1D5V & 0D75V

Size: A2 | Document Number: Colossus | Rev: 1

Date: Thursday, January 05, 2012 | Sheet 46 of 103

RT8068A for 1D8V_S0

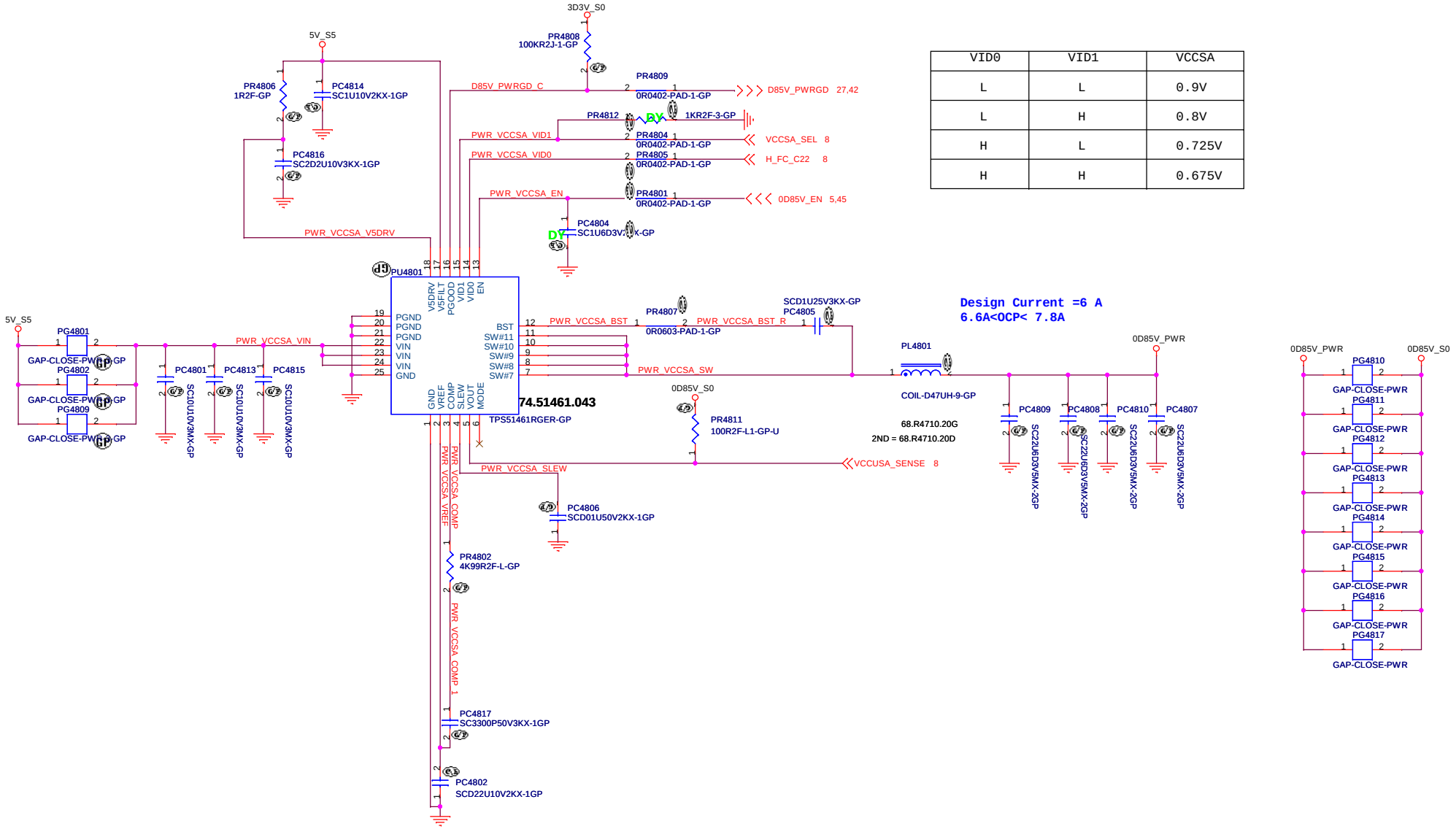


<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***RT8068A_1D8V***	
Size: A3	Document Number: **Colossus**	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 47 of 103	

TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51461 VCCSA

Size: A3 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 48 of 103

LVDS CONNECTOR
AUO B156HB01 V0

D_MIC by EMI

LVDS Impedance:90 ohm

3D3V_S0
RN9401
SRN2K2J-1-GP
LCD_SMBCLK
LCD_SMBDATA

EL4901
DMIC_DATA_C
SBY100505T-601Y-N-GP
DMIC_DATA 29
EC4908
SC22P50V2JN-4GP

EL4902
DMIC_CLK_C
SBY100505T-601Y-N-GP
DMIC_CLK 29
EC4909
SC22P50V2JN-4GP

DCBATOUT_LCD
DCBATOUT
F4901
POLYSW-1D1A24V-GP-U
C4907
SCD1U50V3KX-GP

FUSE
Main:69.50007.A41
Second:69.50007.A31
69.50007.A31
2nd = 69.50007.A41

WEBCAM
21 USB_PP10
21 USB_PN10
R4905 0R0402-PAD
R4906 0R0402-PAD
USB_CAMERA
USB_CAMERA#
-1 12/20 Delete TR4901

LCDVDD
U4902
G5285T11U-GP
Layout 40 mil
OUT
GND
EN
IN#4
IN#5
74.05285.07F
2ND = 74.09724.09F
20 LCDVDD_EN
R4907
100KR2J-1-GP
C4903
SC4D7U6D3V3KX-GP
3D3V_S0
C4906
SC4D7U6D3V3KX-GP

27 BLON_OUT
R4901
1KR2J-1-GP
BLON_OUT_C
R4904
100KR2J-1-GP
C4904
SC100P50V2JN-3GP

LVDS1
IPEX-CONN40-2R-GP-U
20.F1093.040
2ND = 20.F1289.040

DCBATOUT_LCD
SC1U6D3V2KX-GP
C4905 C4902
C4901 SC1U6D3V2KX-GP
SCD1U10V2KX-5GP
5V_S0_LOGO_BL
LCDVDD
3D3V_S0

WEBCAM
-1 12/22
USB_CAMERA
USB_CAMERA#
DMIC_DATA_RF2
DMIC_CLK_RF2
LCD_BRIGHTNESS
BLON_OUT_C
ER4901
ER4902
R4903
0R0402-PAD
0R0402-PAD
1KR2J-1-GP
DMIC_DATA_C
DMIC_CLK_C
DMIC
BKLT_CTL 20
LCD_SMBCLK 20
LCD_SMBDATA 20

TXOUTA_L0- 20
TXOUTA_L0+ 20
TXOUTA_L1- 20
TXOUTA_L1+ 20
TXOUTA_L2- 20
TXOUTA_L2+ 20
TXCLKA_L- 20
TXCLKA_L+ 20
TXOUTB_L0- 20
TXOUTB_L0+ 20
TXOUTB_L1- 20
TXOUTB_L1+ 20
TXOUTB_L2- 20
TXOUTB_L2+ 20
TXCLKB_L- 20
TXCLKB_L+ 20

DCBATOUT_LCD
EC4902 EC4901
EC4904 EC4903
EC4906 EC4905
EC4910 EC4907
SC5D6P50V2CN-1GP
LCDVDD
3D3V_S0
DMIC_DATA_RF2
DMIC_CLK_RF2

CAP CLOSED IN LVDS1

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector
Size: A3
Document Number: Colossus
Rev: 1
Date: Wednesday, January 04, 2012
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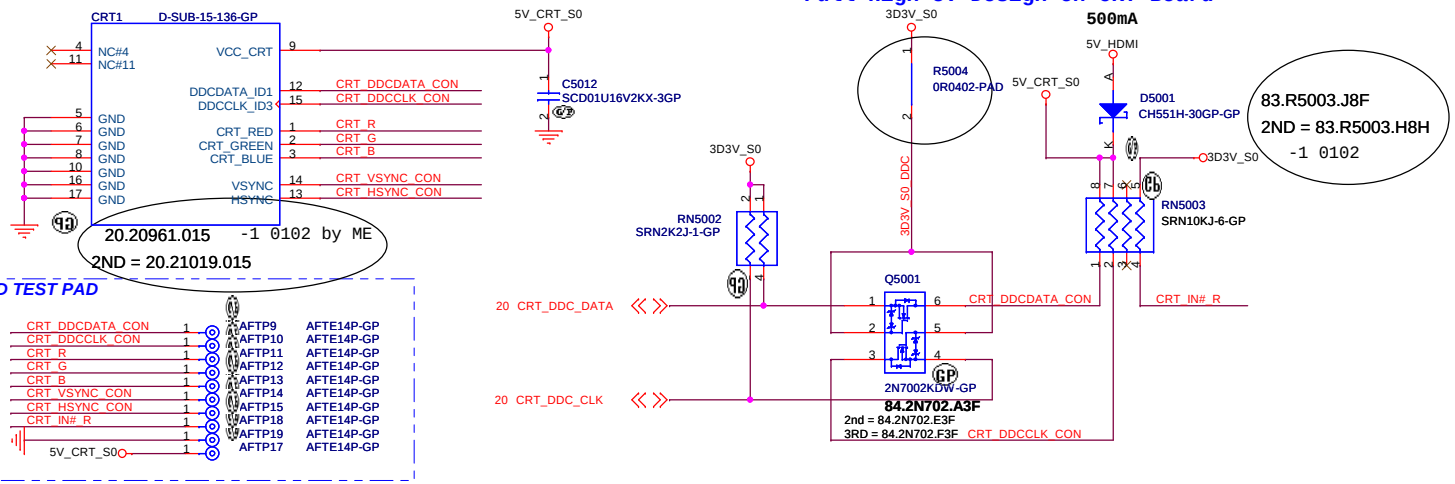
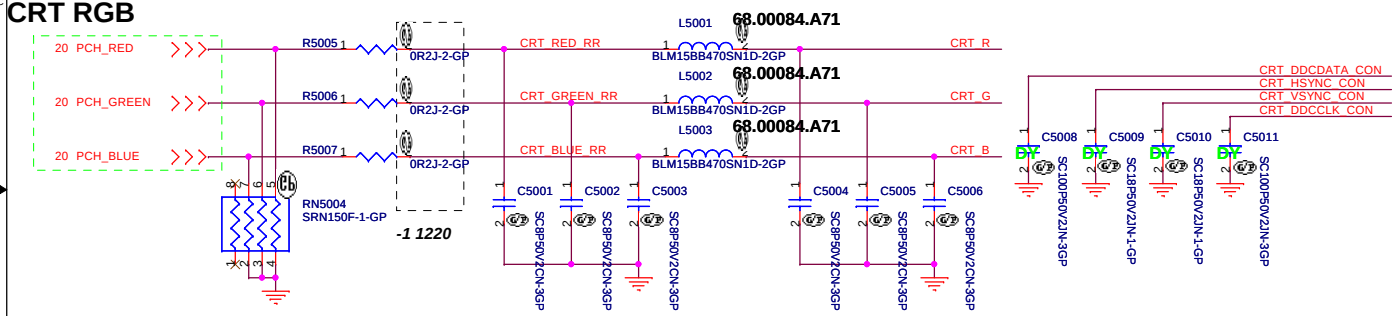
CRT Connector

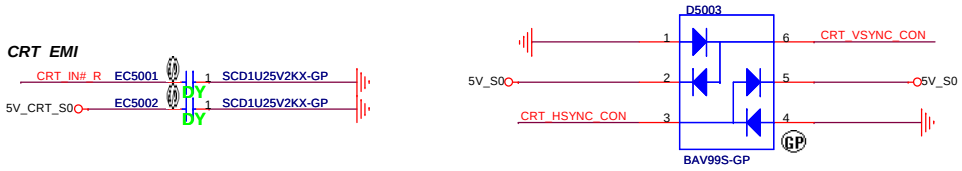


CRT DDCDATA & DDCCLK level shift

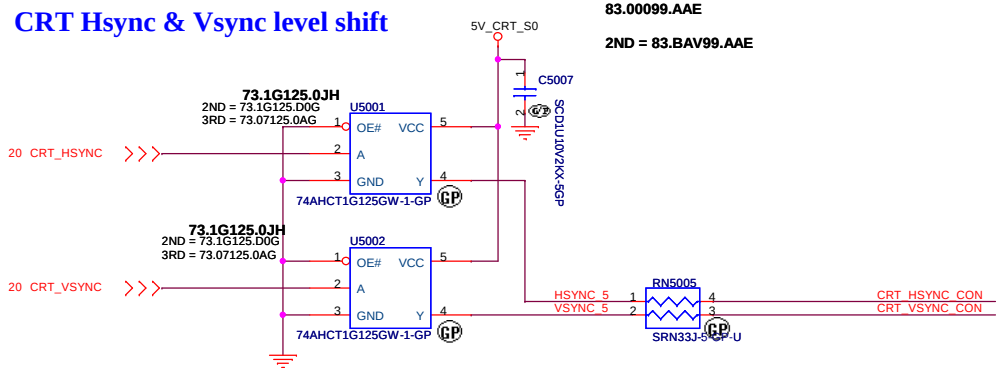
Pull High 5V Design on CRT Board

CRT RGB





CRT Hsync & Vsync level shift



<Core Design>

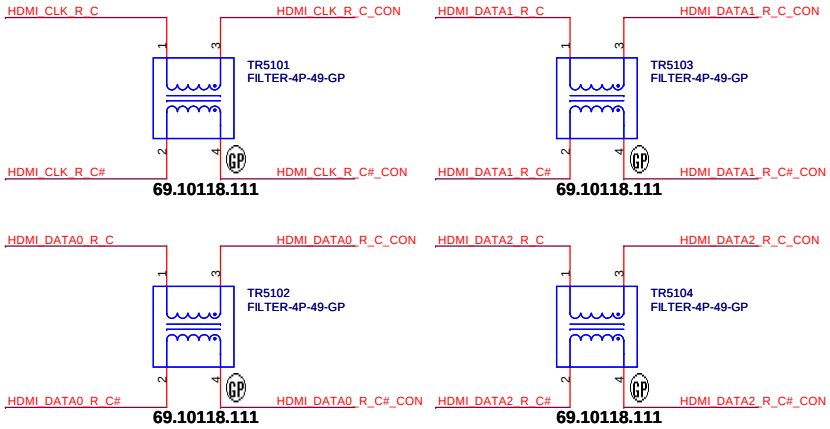
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT_CONN**

Size	Document Number	Rev
A3	Colossus	1

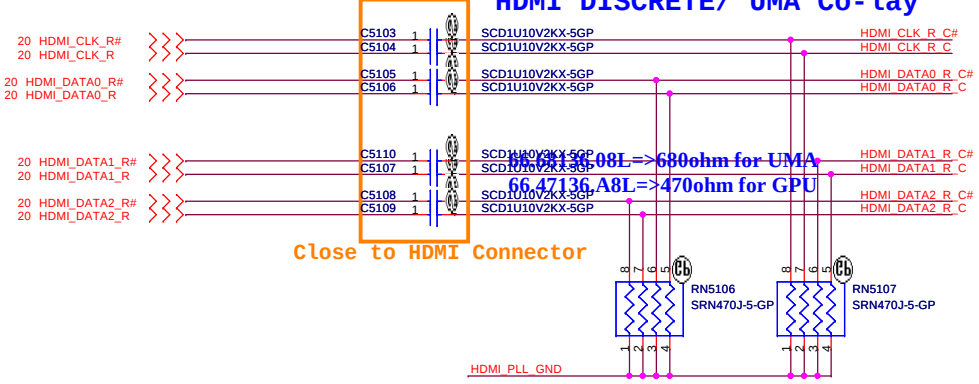
Date: Wednesday, January 04, 2012 Sheet 50 of 103

HDMI Level Shifter & CONNECTOR



Close to GPU

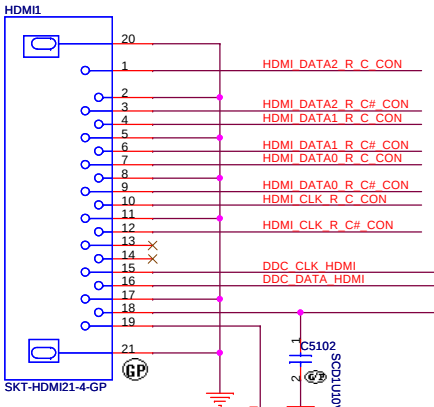
HDMI DISCRETE/ UMA Co-lay

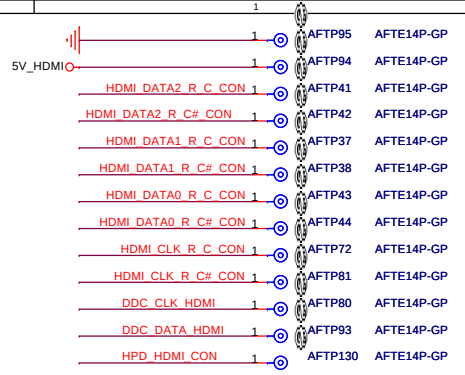


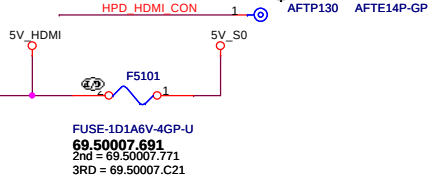
RC-051J08L=>680ohm for UMA
66.47136.A8L=>470ohm for GPU

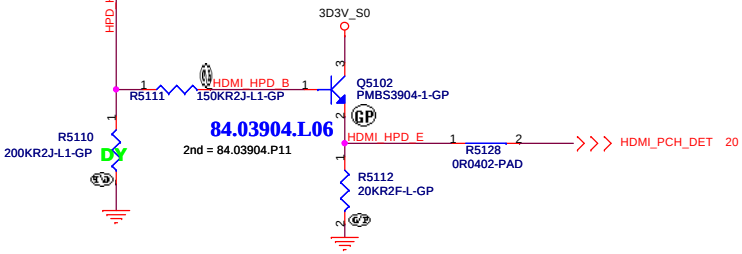
Close to HDMI Connector

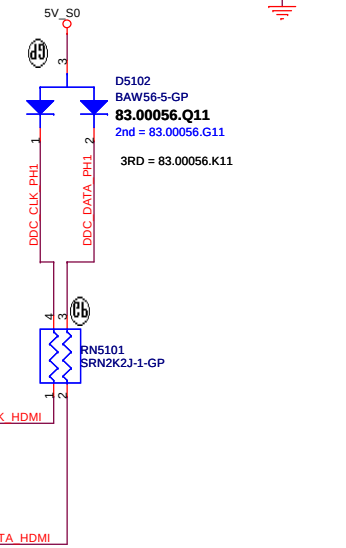
HDMI CONN

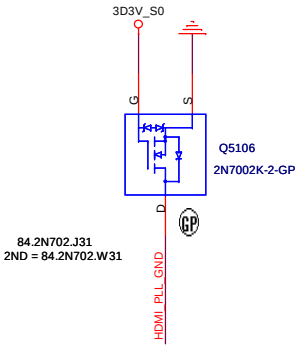












Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

緯創資通 Wistron Corporation
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Title: HDMI Level Shifter/Conn
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 51 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Display Port*

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 52 of 103

(Blanking)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
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Date: Monday, December 26, 2011 Sheet 53 of 103

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 54 of 103

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
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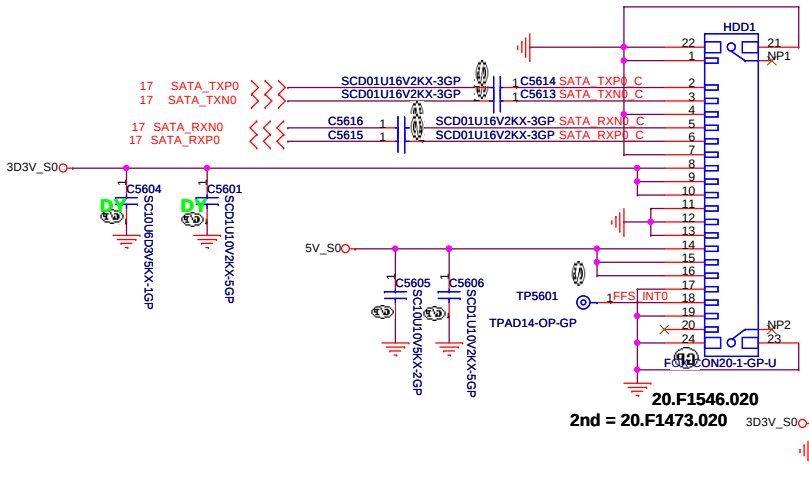
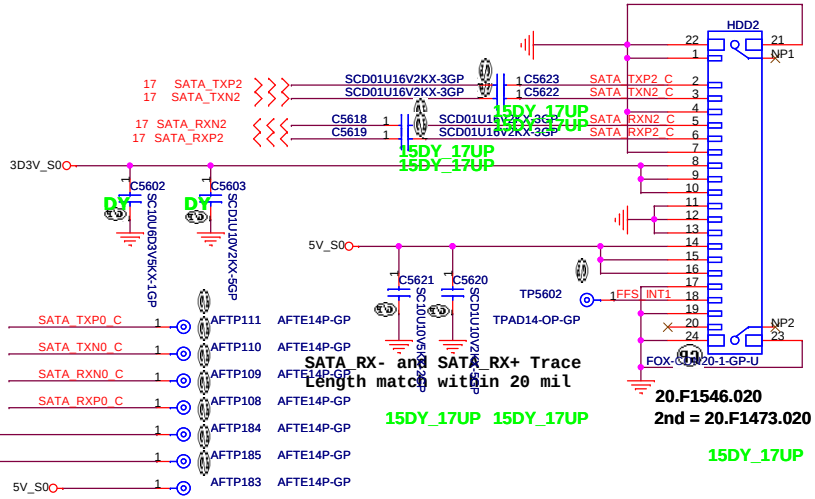
Date: Monday, December 26, 2011 Sheet 55 of 103

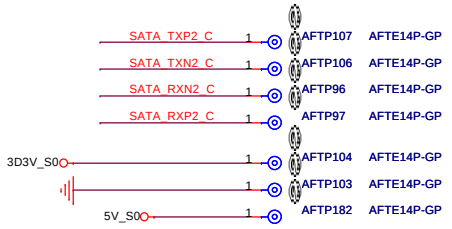
SATA HDD1 Connector

CHECK HDD conn model pin define_ME wire

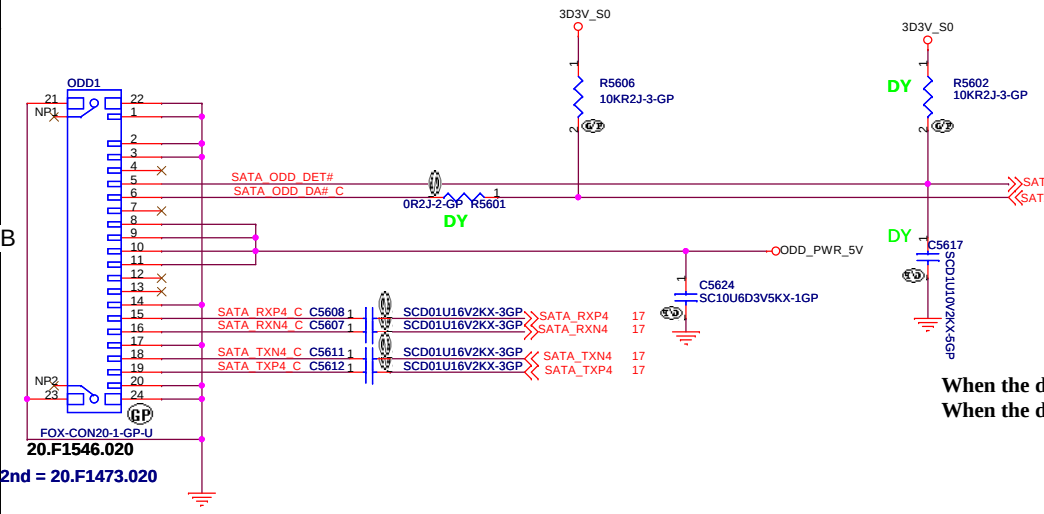


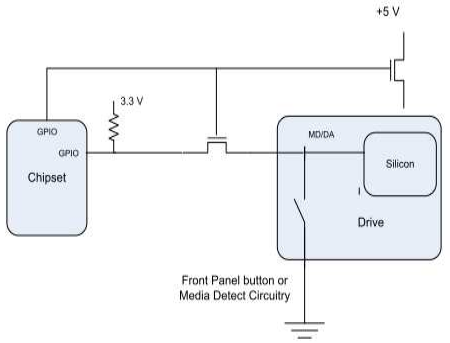
SATA HDD2 Connector





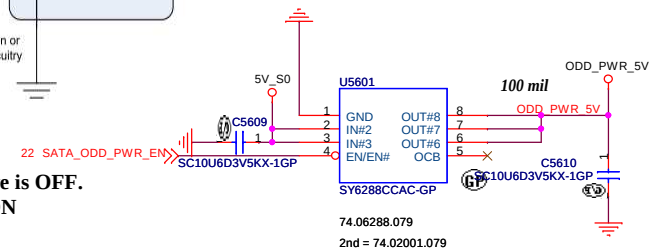
ODD Connector



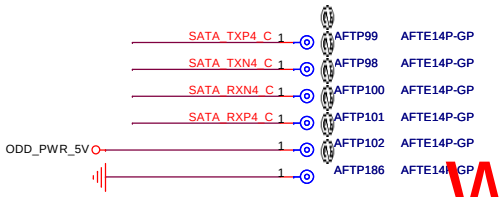


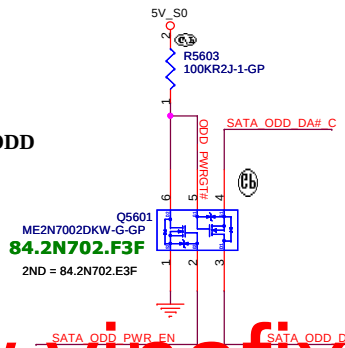
When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

SATA Zero Power ODD



SUPPORT ZERO SATA ODD





<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 56 of 103

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<Core Design>

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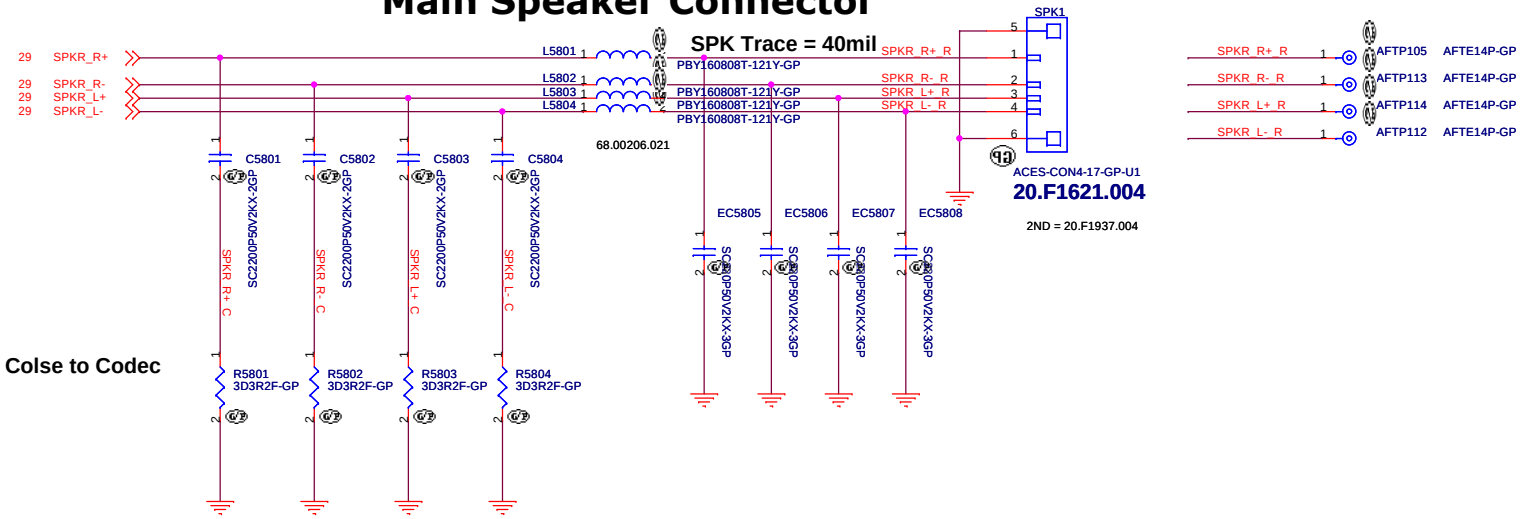
Taipei Hsien 221, Taiwan, R.O.C.

Title: ESATA

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 57 of 103

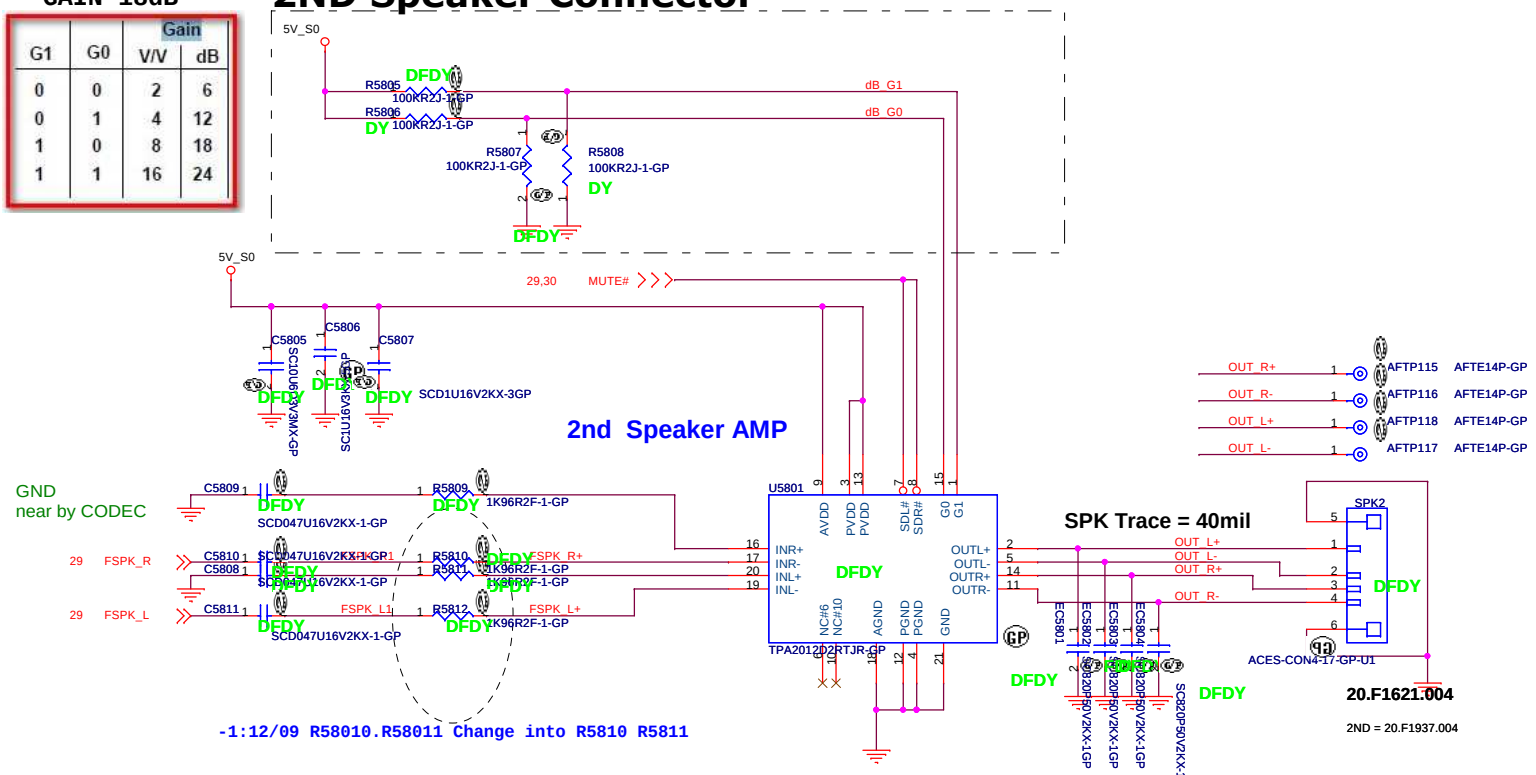
Main Speaker Connector



2ND Speaker Connector

GAIN 18dB

Gain			
G1	G0	V/V	dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24



-1:12/09 R58010.R58011 Change into R5810 R5811

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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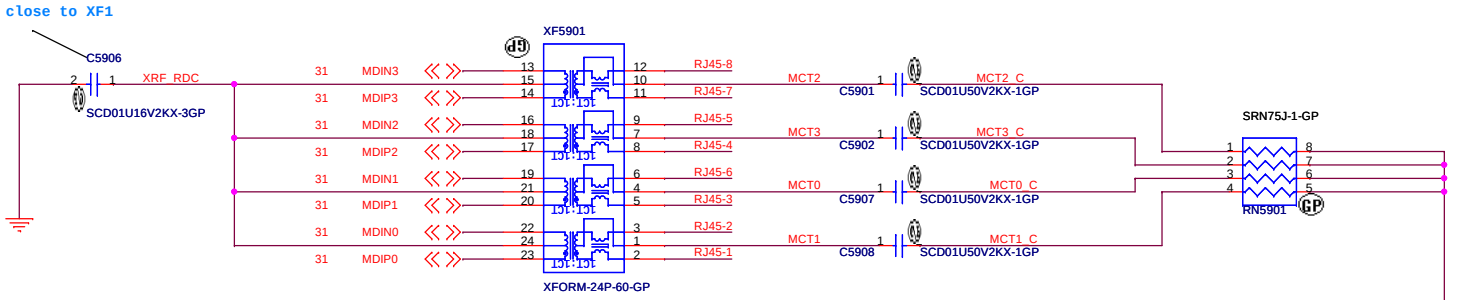
Title: **SPEAKER CONN**

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 58 of 103

White LED for connectivity and Amber LED for activity located on RJ-45 connector

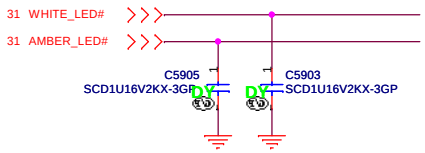
close to XF1



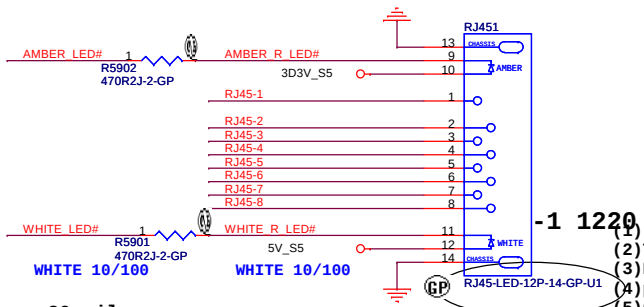
68.IH160.30A

2ND = 68.89246.301

AMBER = LAN ACK



RJ451



WHITE 10/100 **WHITE 10/100**

20 mils

-1 1220

(1)route on bottom as differential pairs.
(2)Tx+/Tx- are pairs. Rx+/Rx- are pairs.
(3)No vias, No 90 degree bends.
(4)pairs must be equal lengths.
(5)6mil trace width,12mil separation.
(6)36mil between pairs and any other trace.
(7)Must not cross ground moat,
except RJ-45 moat.

<Core Design>

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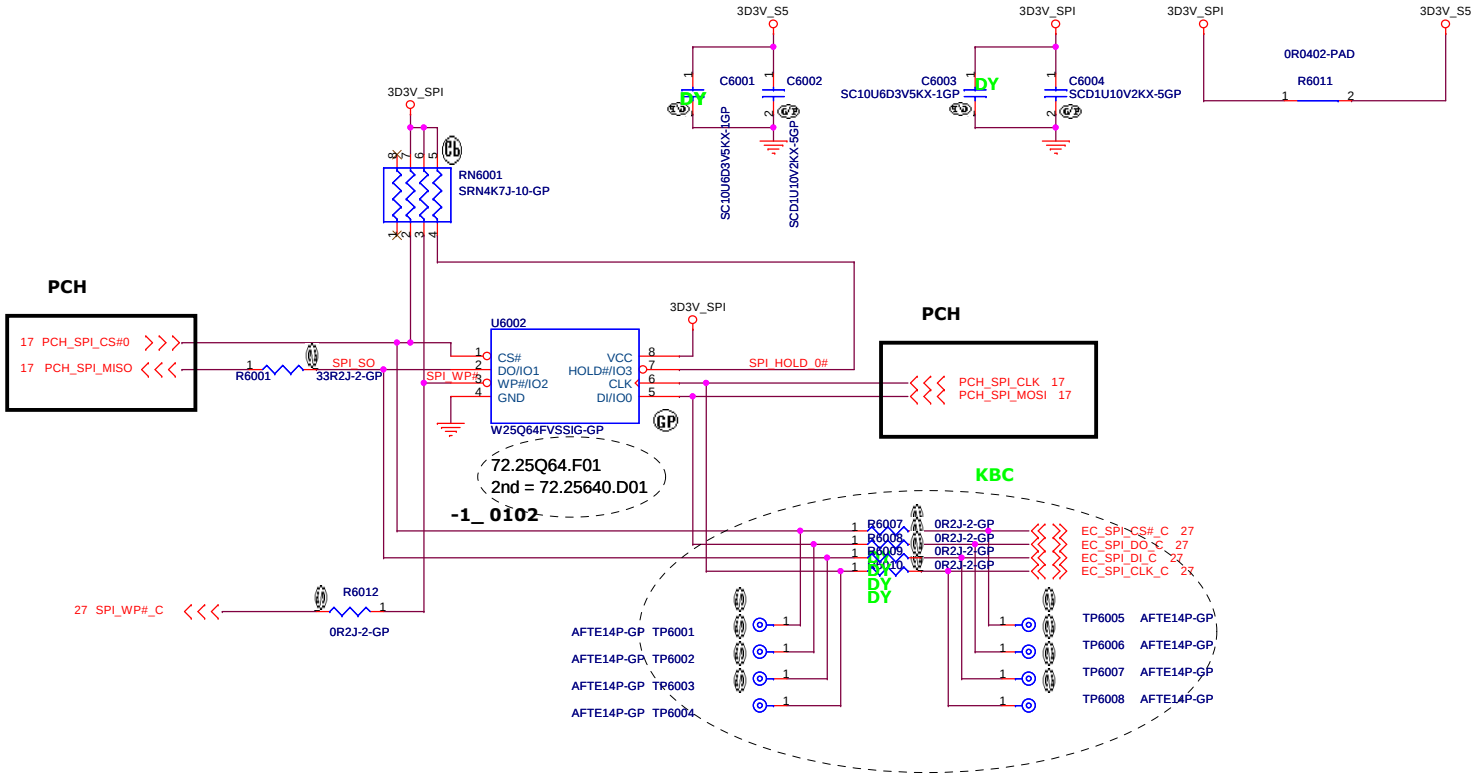
Title: ***RJ45+Transformer***

Size	Document Number	Rev
A3	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 59 of 103

SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH & KBC



Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

-1 1223 Reversed TP6001~TP6008 / R6007~R6010 is DY
1, 測試點請使用14mil, 測試之間距離75mil以上。
2，測試點必須在Top層.

<Core Design>

緯創資通 Wistron Corporation
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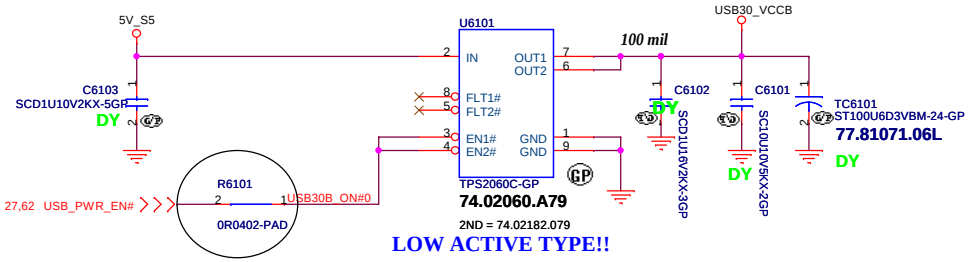
Title		
Flash		
Size: A3	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 60 of 103	

RESERVED USB 2.0/3.0 BD

SSID = USB

Power switcher Low active

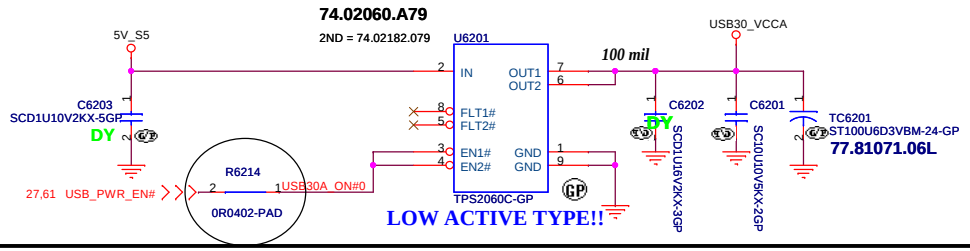


LOW ACTIVE TYPE!!

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***USB Power SW_USB IO***
Size A3 / Document Number	**Colossus** / Rev **1**
Date: Wednesday, January 04, 2012	Sheet 61 of 103

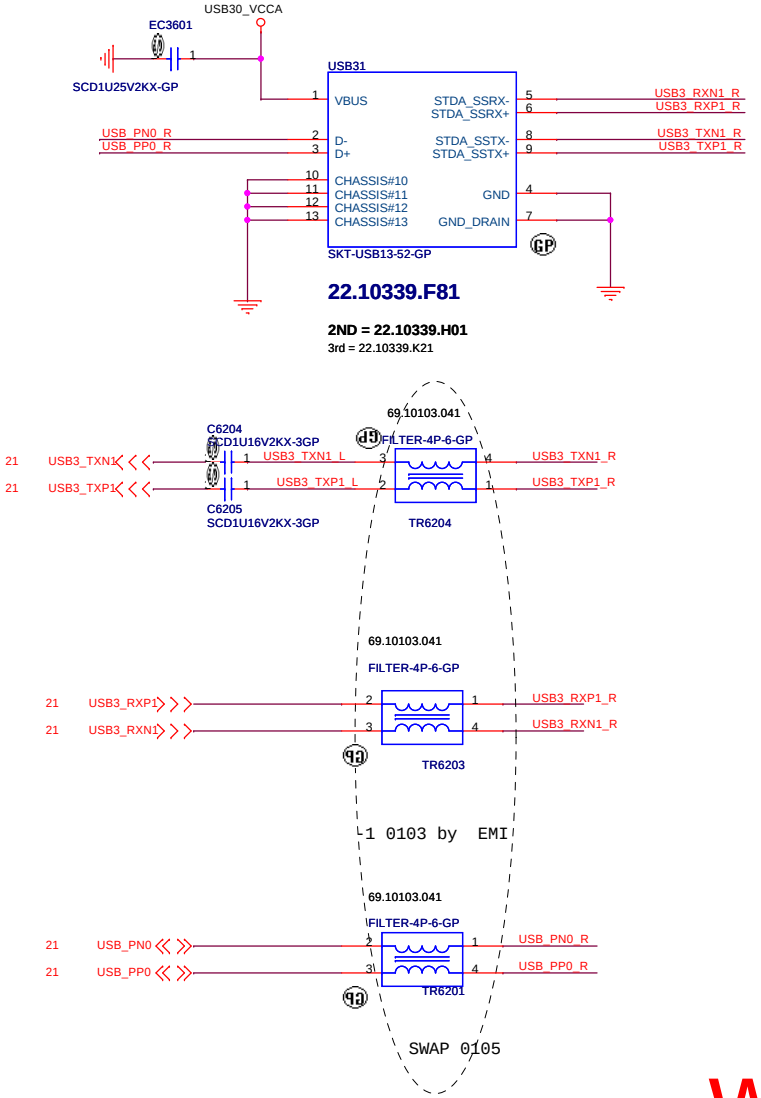
Power switcher Low active



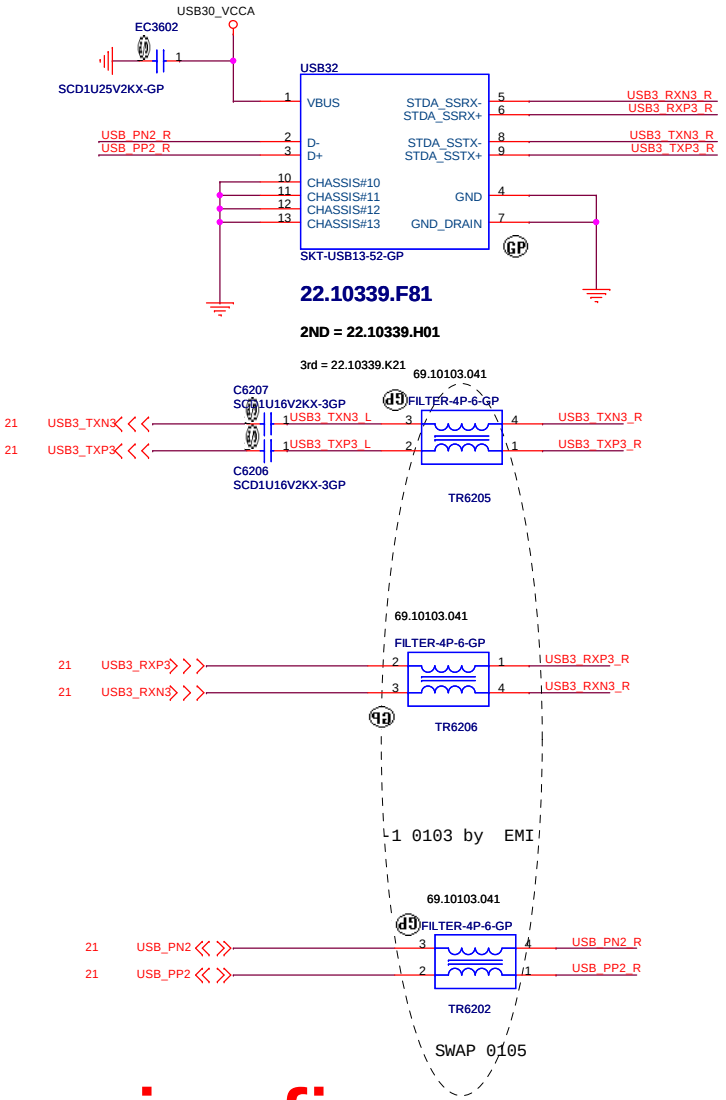
USB 3.0 Connector Pin definition

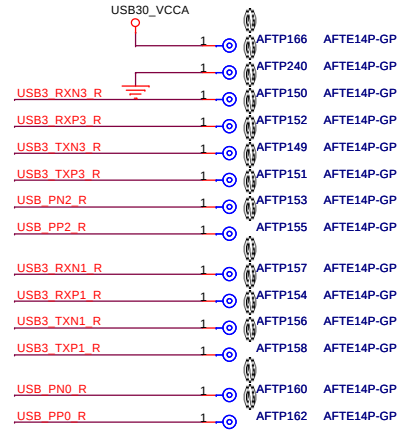
1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

USB3_1

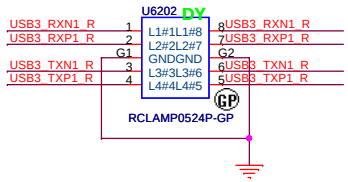


USB3_2

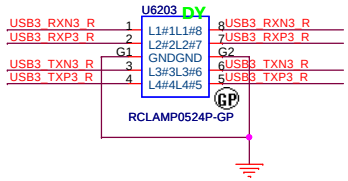




Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



Ultra Low Capacitance TVS Arrays (Pin5.6.7.8 No Internal Connection)



<Core Design>

緯創資通 **Wistron Corporation**
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Title: **USB3.0**

Size	Document Number	Rev
A3	Colossus	1

Date: Thursday, January 05, 2012 Sheet 62 of 103

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<Variant Name>

緯創資通 Wistron Corporation
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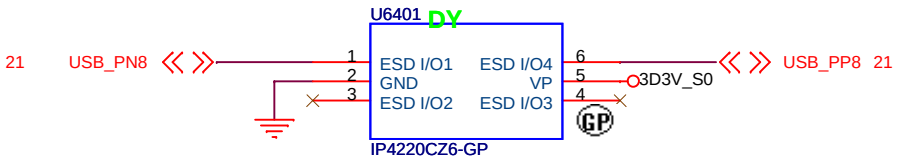
Taipei Hsien 221, Taiwan, R.O.C.

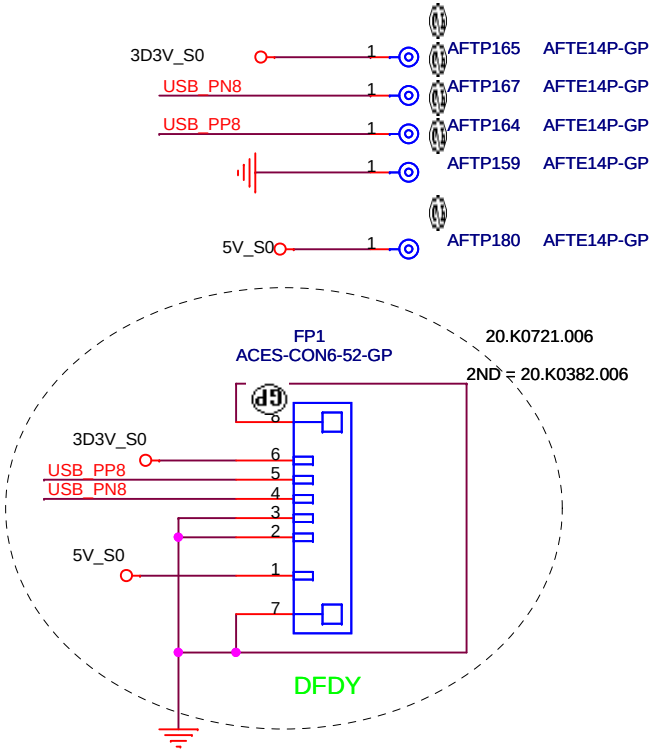
Title: *Resered(Bluetooth)*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 63 of 103

Finger Printer





-1 12/23 FP1 change source

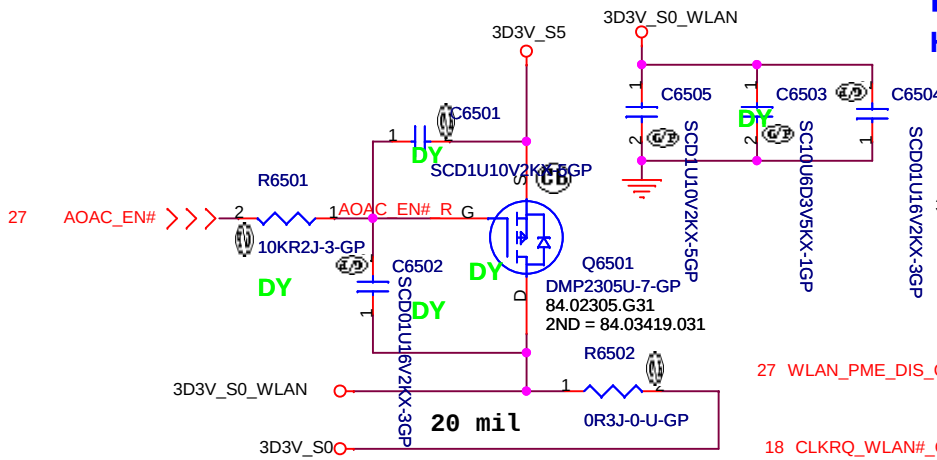
<Core Design>

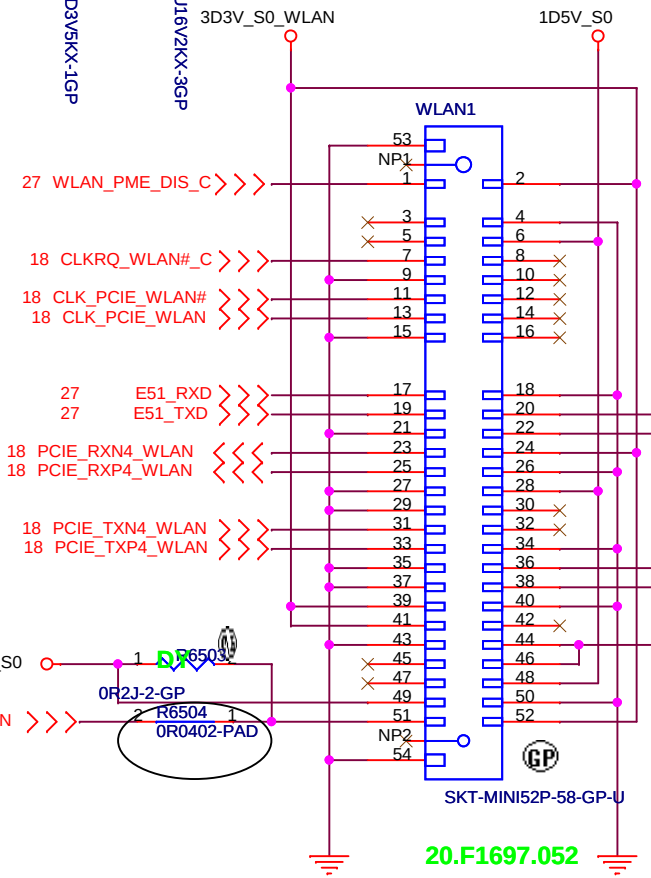
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Finger Print Conn*		
Size: A4	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 64 of 103	

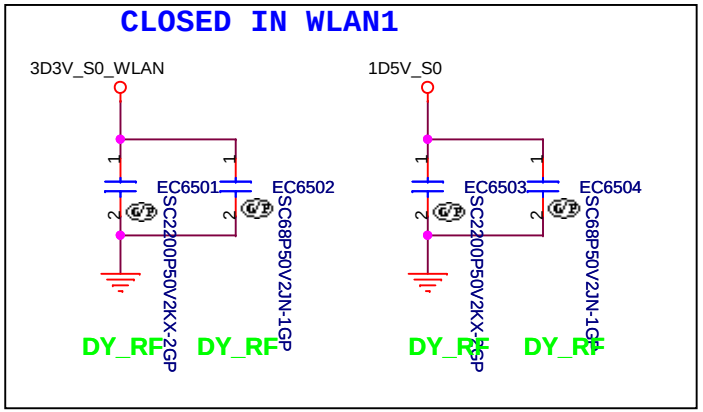
SSID = Wireless

Mini-Card--WLAN

Half minicard







51	BT_ DISABLE_L (low active to disable Bluetooth)

Pin	Active	Function
5	High(3V)	GPIO/BT_WAKE
20	High(3V)	WIFI_Enable
47	Reserved	BT_PRISEL(coexistence)
51	Reserved	BTCX_STAT(coexistence)

1-1 1226 del TR6501

<Core Design>

677869-FM8

1st	677869-FM8
2nd	677869-AM8
3rd	677869-BM8
4th	677869-LM8

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINICARD(WLAN+Bluetooth)/CONN

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 65 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 66 of 103

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<Core Design>

緯創資通 Wistron Corporation
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Title: *Reserved*

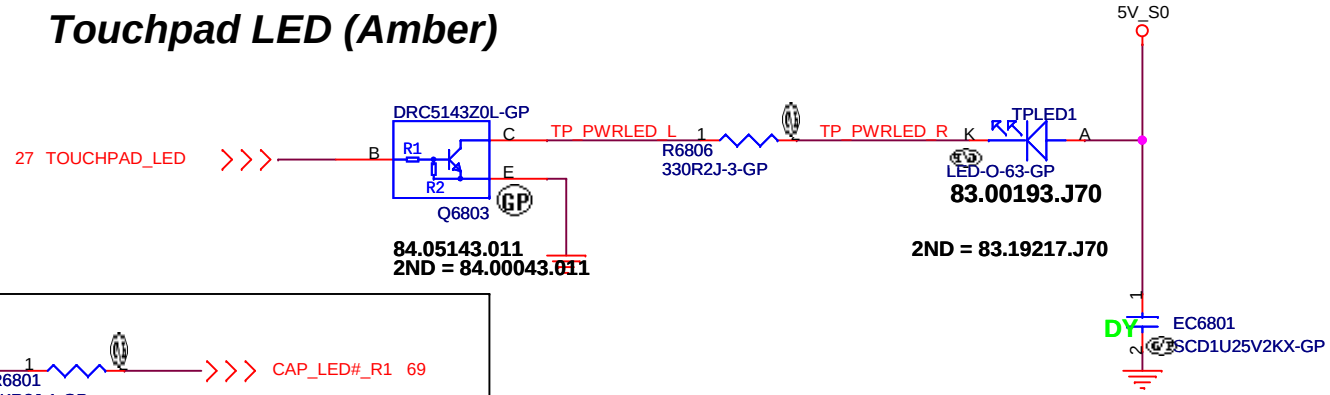
Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 67 of 103

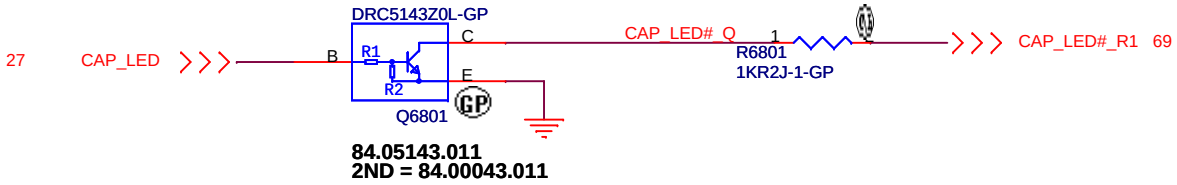
SSID = User.Interface

On Keyboard LEDs

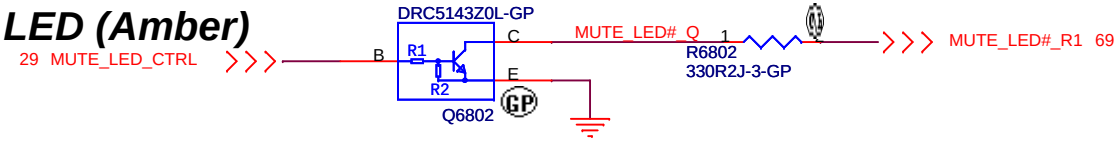
Touchpad LED (Amber)



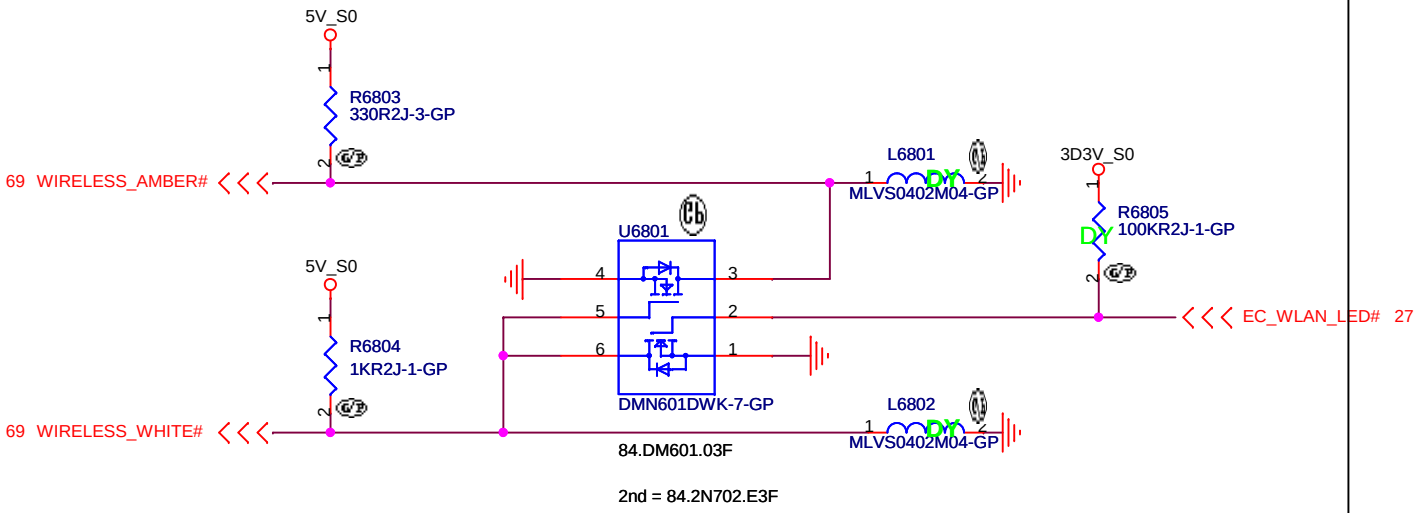
Cap locks LED (White)



Mute LED (Amber)



Wireless LED (White-On, Amber-Off)



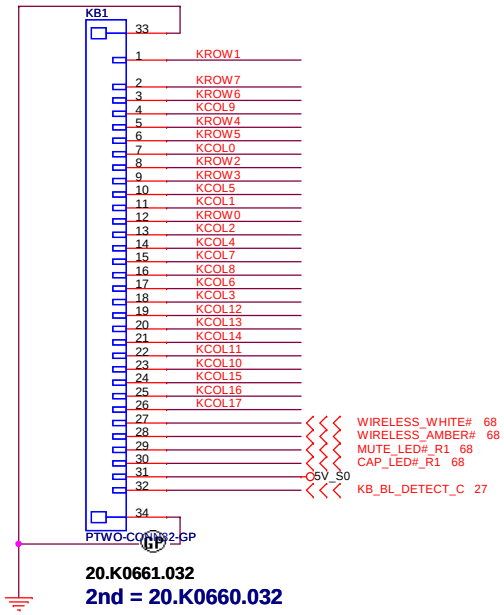
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LED Bard/Power Button	
Size A4	Document Number Colossus	Rev 1
Date: Wednesday, January 04, 2012	Sheet 68 of 103	

SSID = KBC

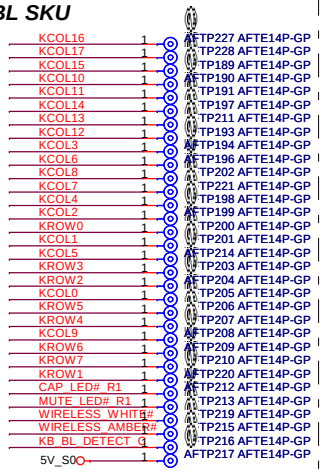
Internal KeyBoard Connector



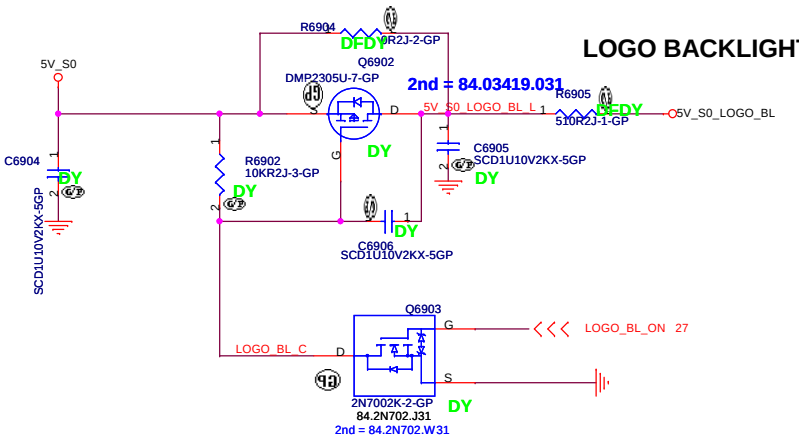
20.K0661.032
2nd = 20.K0660.032
3rd = 20.K0676.032

KROW[0..7] 27
KCOL[0..17] 27

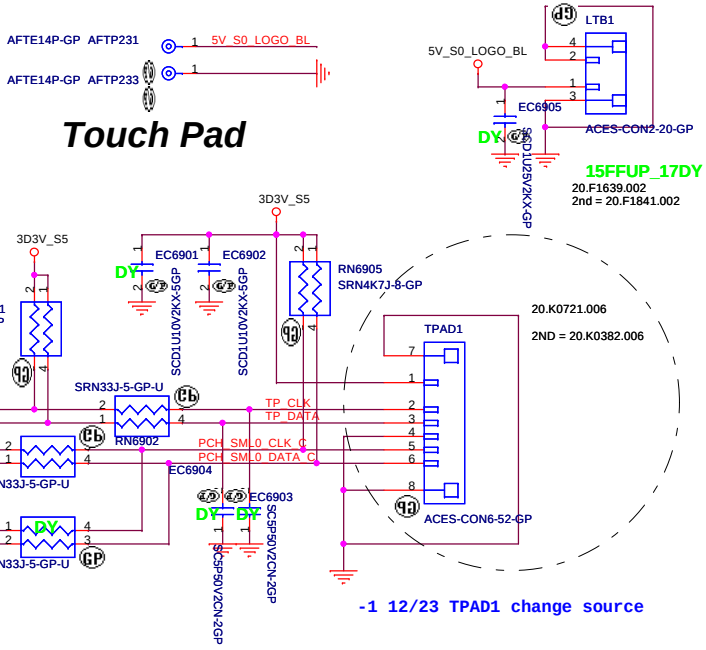
KB_BL_DETECT
HIGH = BL SKU
LOW = NON-BL SKU



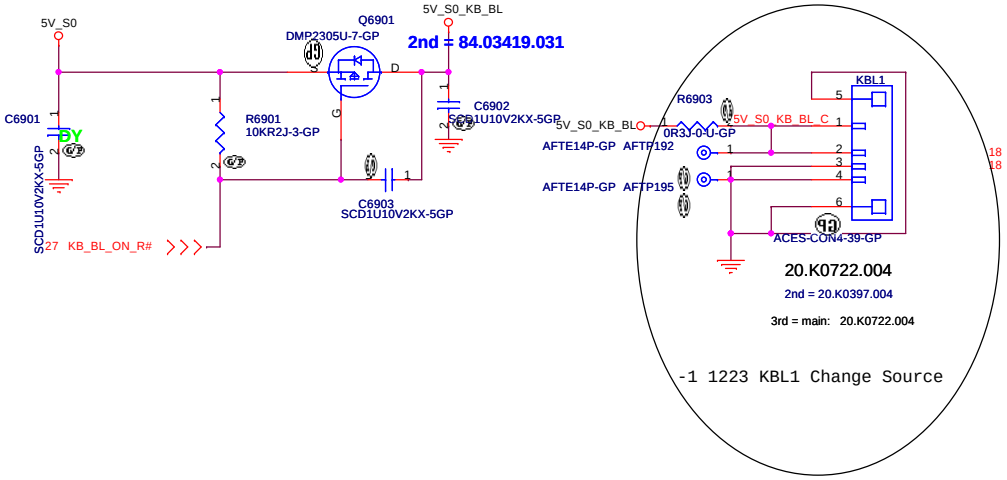
A Cover Logo Backlight

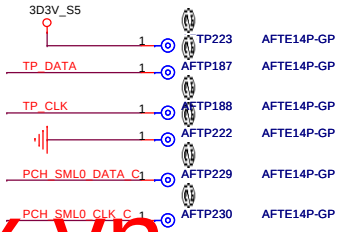


Touch Pad



Internal KeyBoard Backlight Connector





<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: Key Board/Touch Pad
Size: A3 | Document Number: Colossus | Rev: 1
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(Hall sensor at Power BD)

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Hall Sensor

Size	Document Number	Rev
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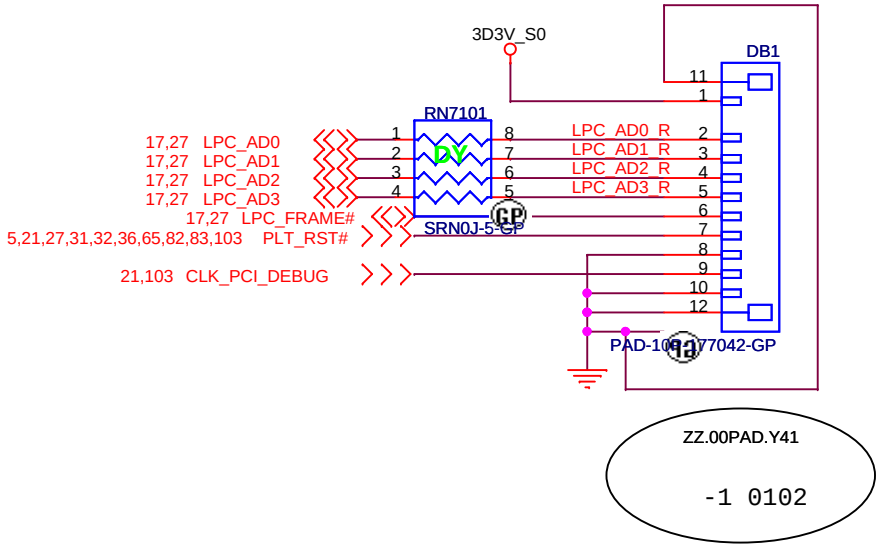
DEBUG BD for Factory Test



<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 71 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 72 of 103

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<Core Design>

緯創資通 Wistron Corporation
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Title: *Reserved*

Size	Document Number	Rev
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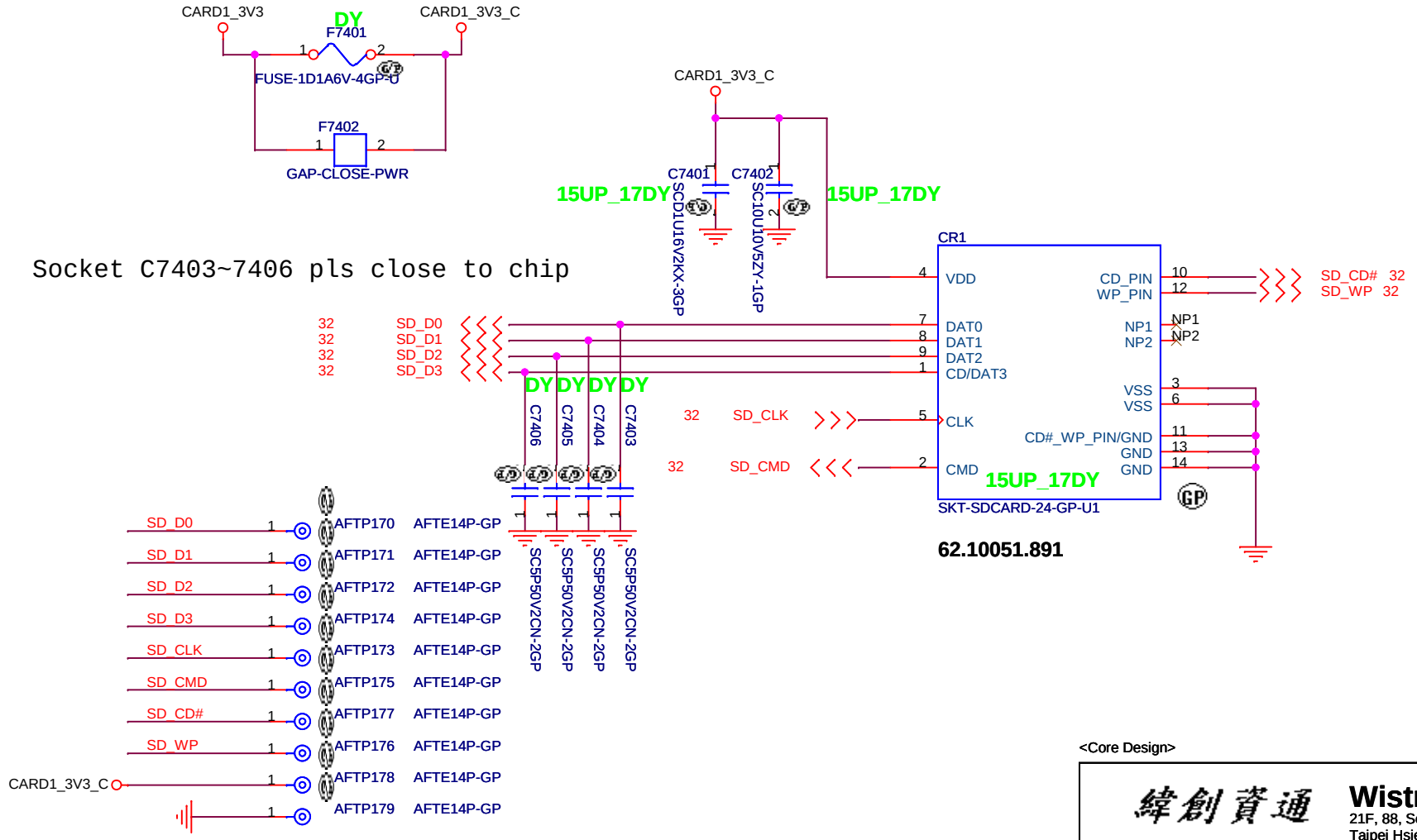
2 IN1 CARD-READER (SD/MMC)



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 74 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Express Card*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 75 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 76 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPM

Size: A3 | Document Number: Colossus | Rev: 1

Date: Monday, December 26, 2011 | Sheet 77 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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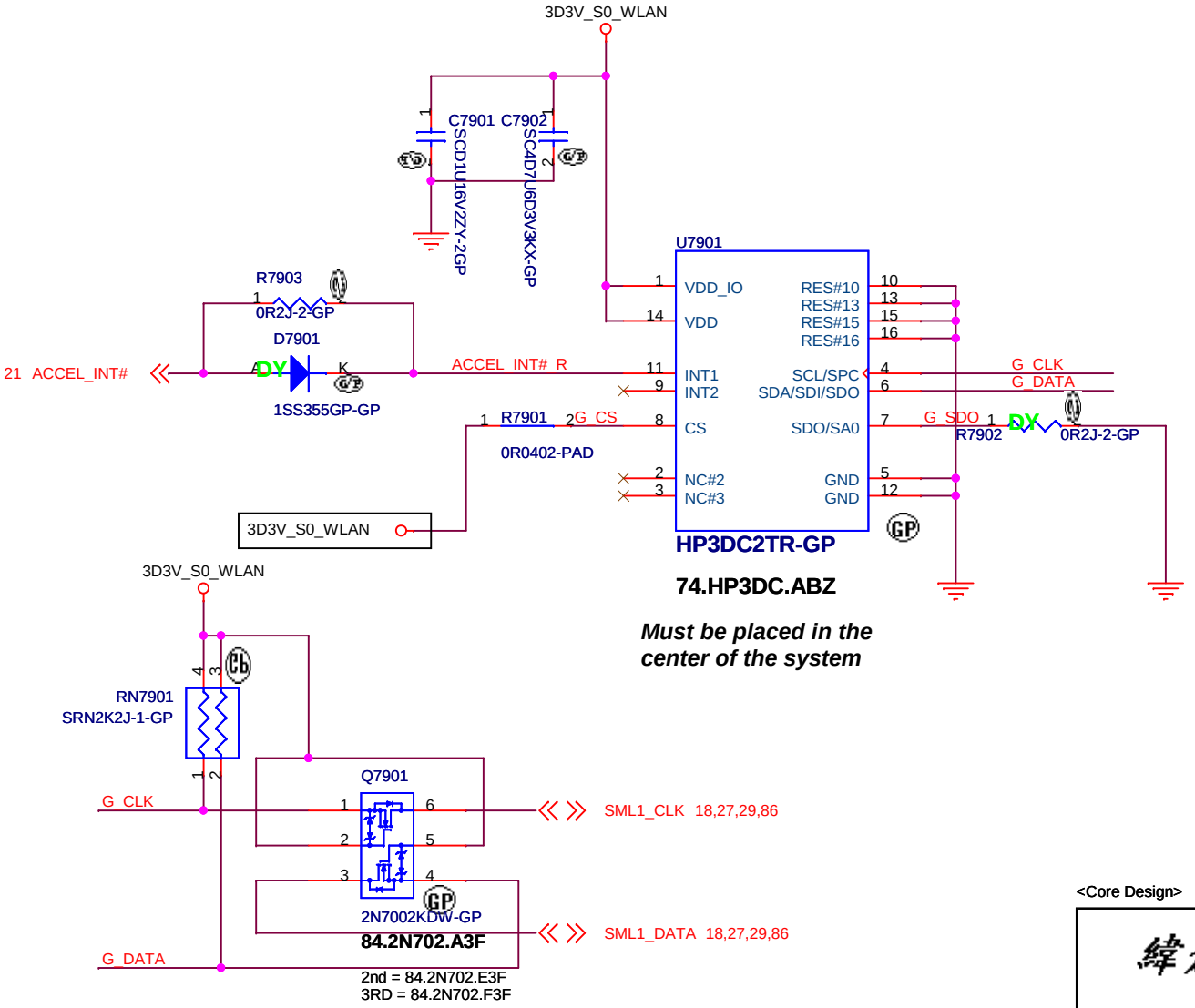
ACCELEROMETER



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ACCELEROMETER

Size	Document Number	Rev
A4	Colossus	1

Date: Wednesday, January 04, 2012 Sheet 79 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

Date: Monday, December 26, 2011 Sheet 80 of 103

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<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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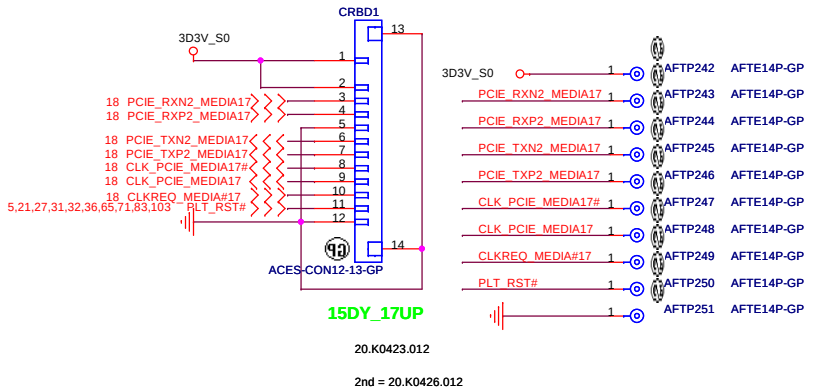
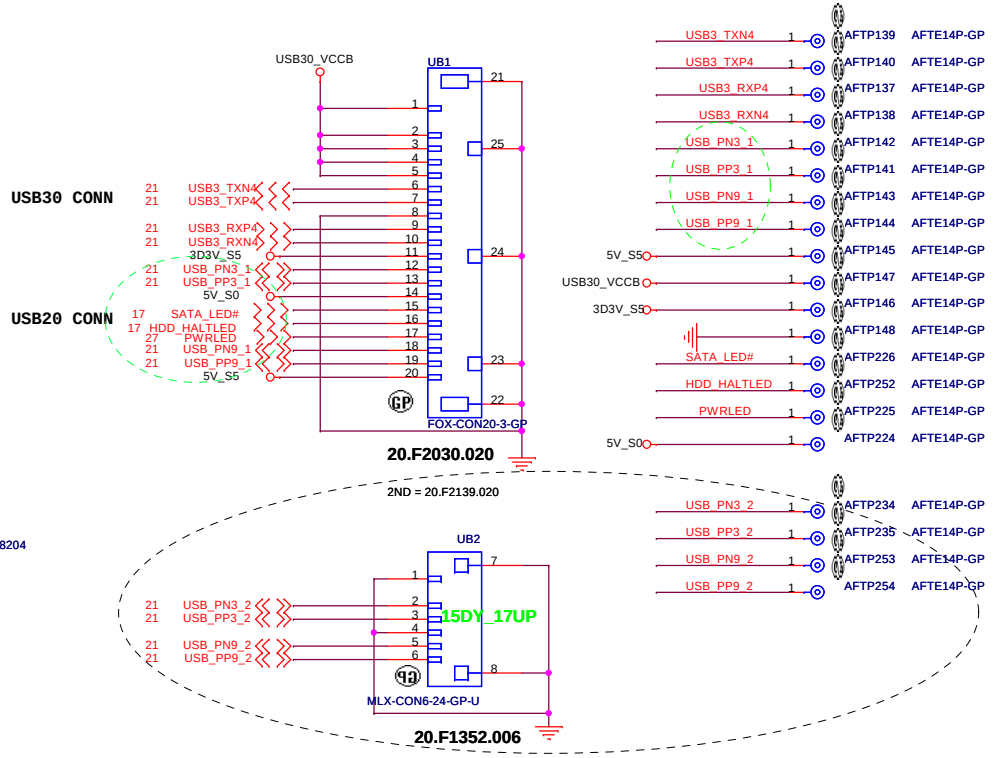
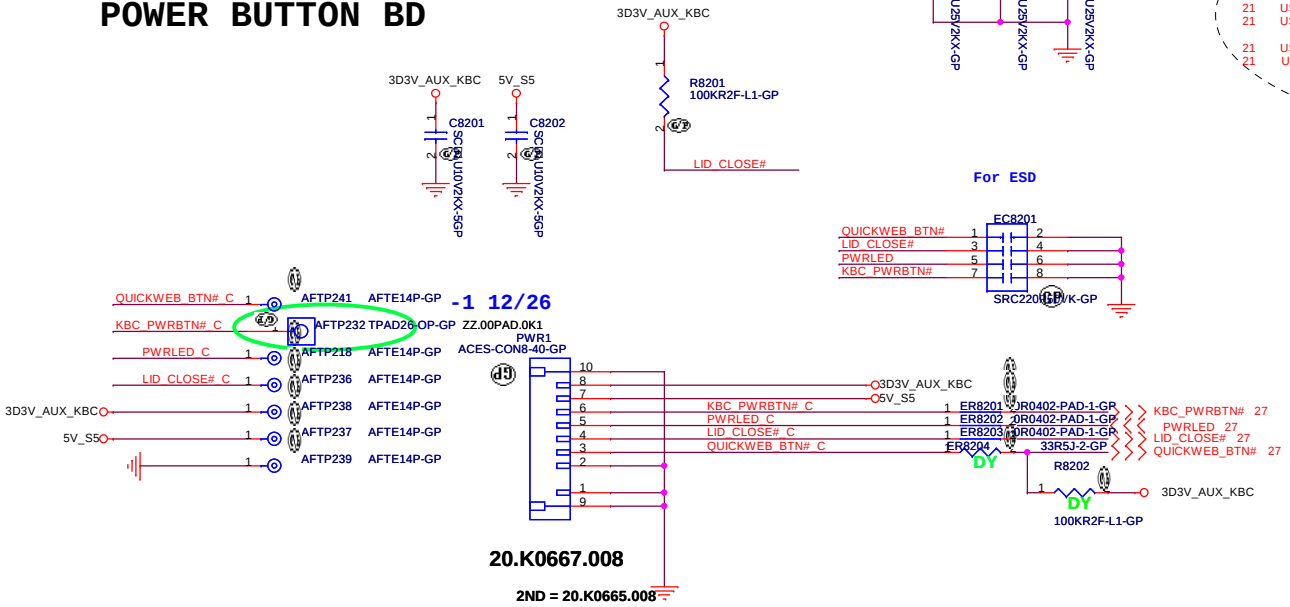
Card Reader BD 15"=DY 17"=PHASE IN



USB BD(USB3.0*1+USB2.0*1)



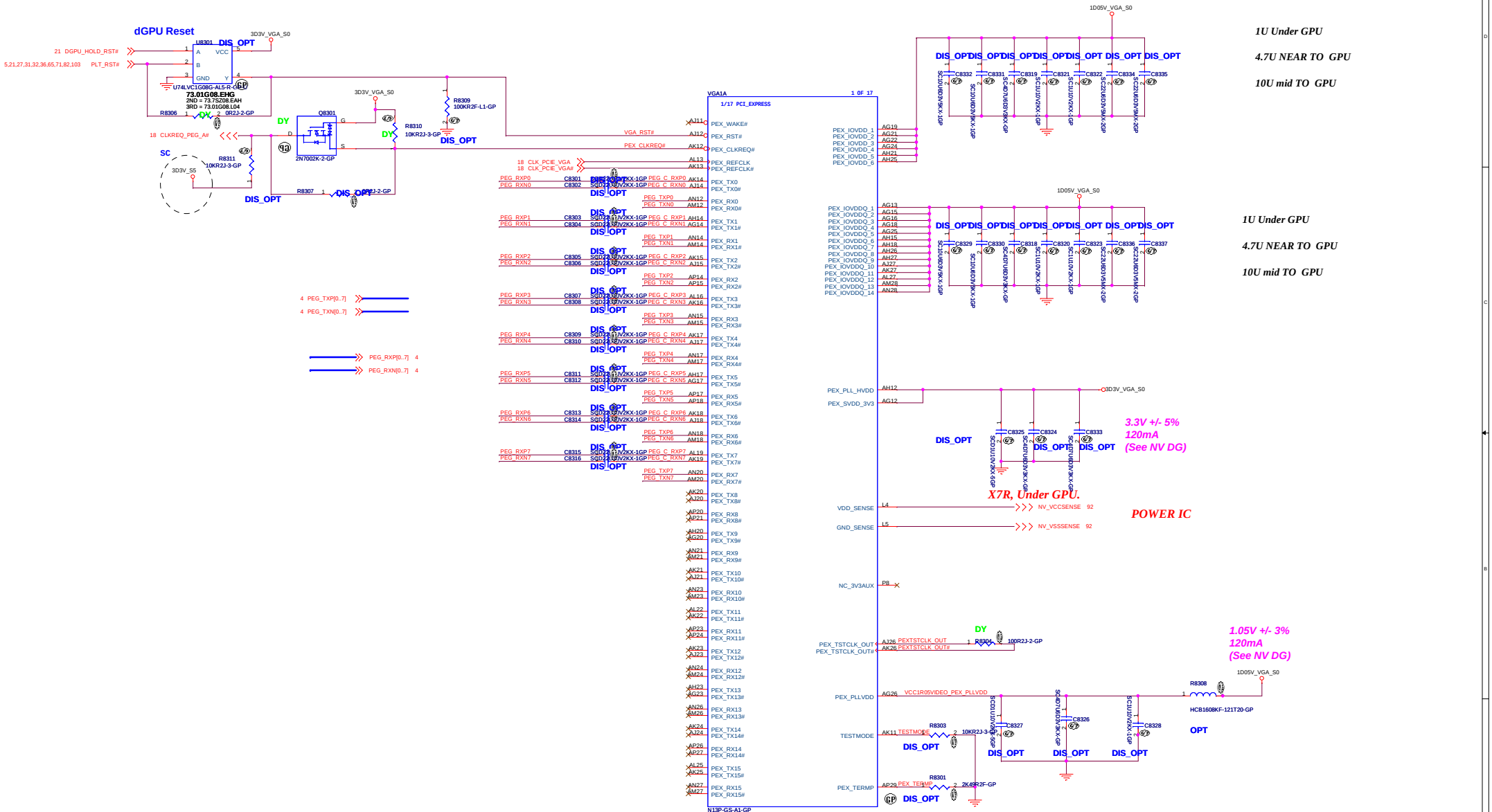
POWER BUTTON BD



TOUCHPAD BD PAGE 69

<Core Design>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector
Size: A3 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 82 of 103



<Variant Name>

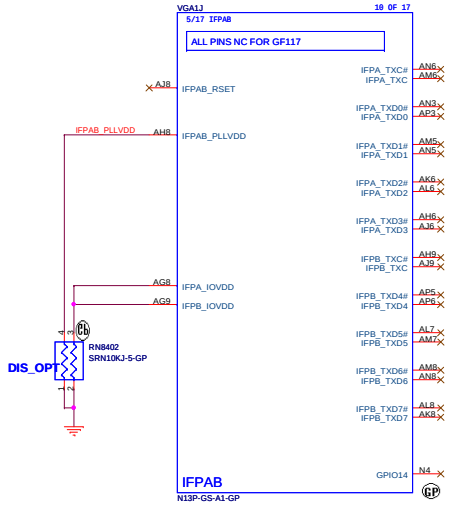
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

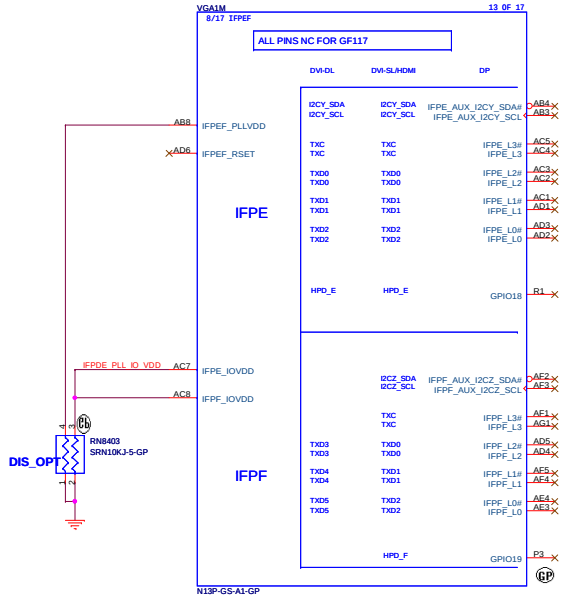
Size: A2 | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 83 of 103

LVDS Interface



71.0N13P.00U DIS_OPT



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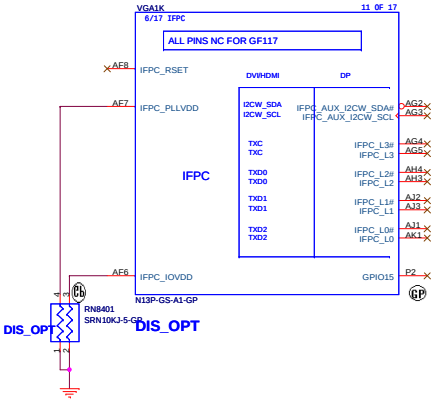

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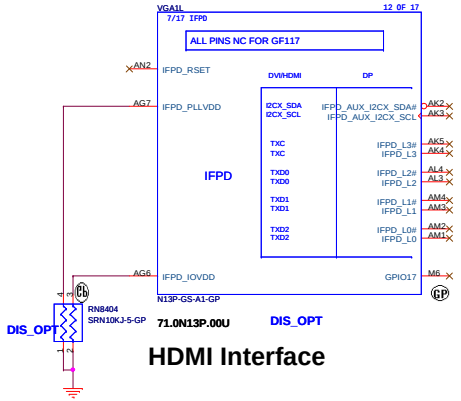

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HDMI Interface

<Variant Name>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)

Size: A2 | Document Number: Colossus | Rev: 1

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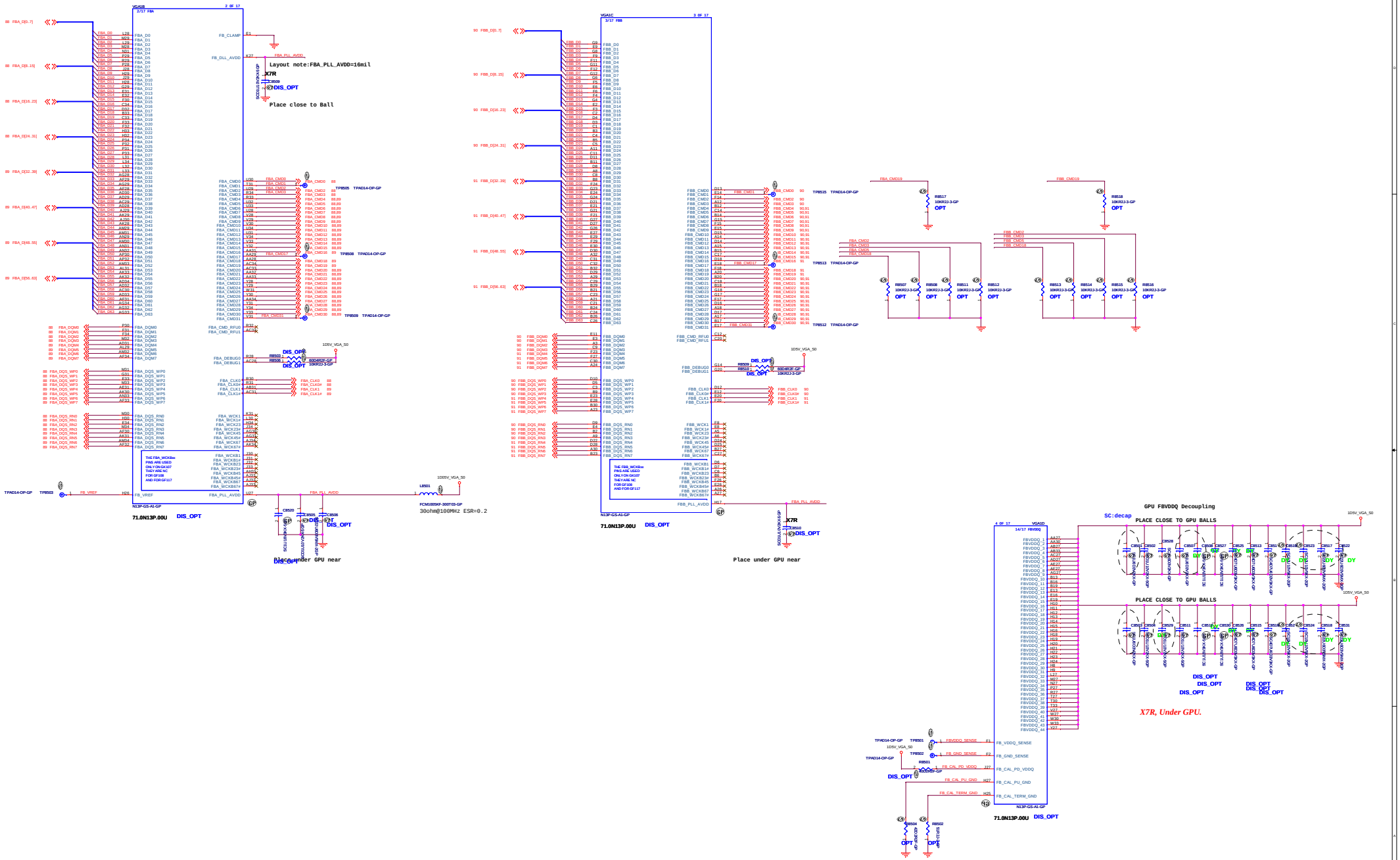

<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title: GPU_DP/LVDS/CRT/GPIO(3/5)
Size: A2 | Document Number: Colossus | Rev: 1
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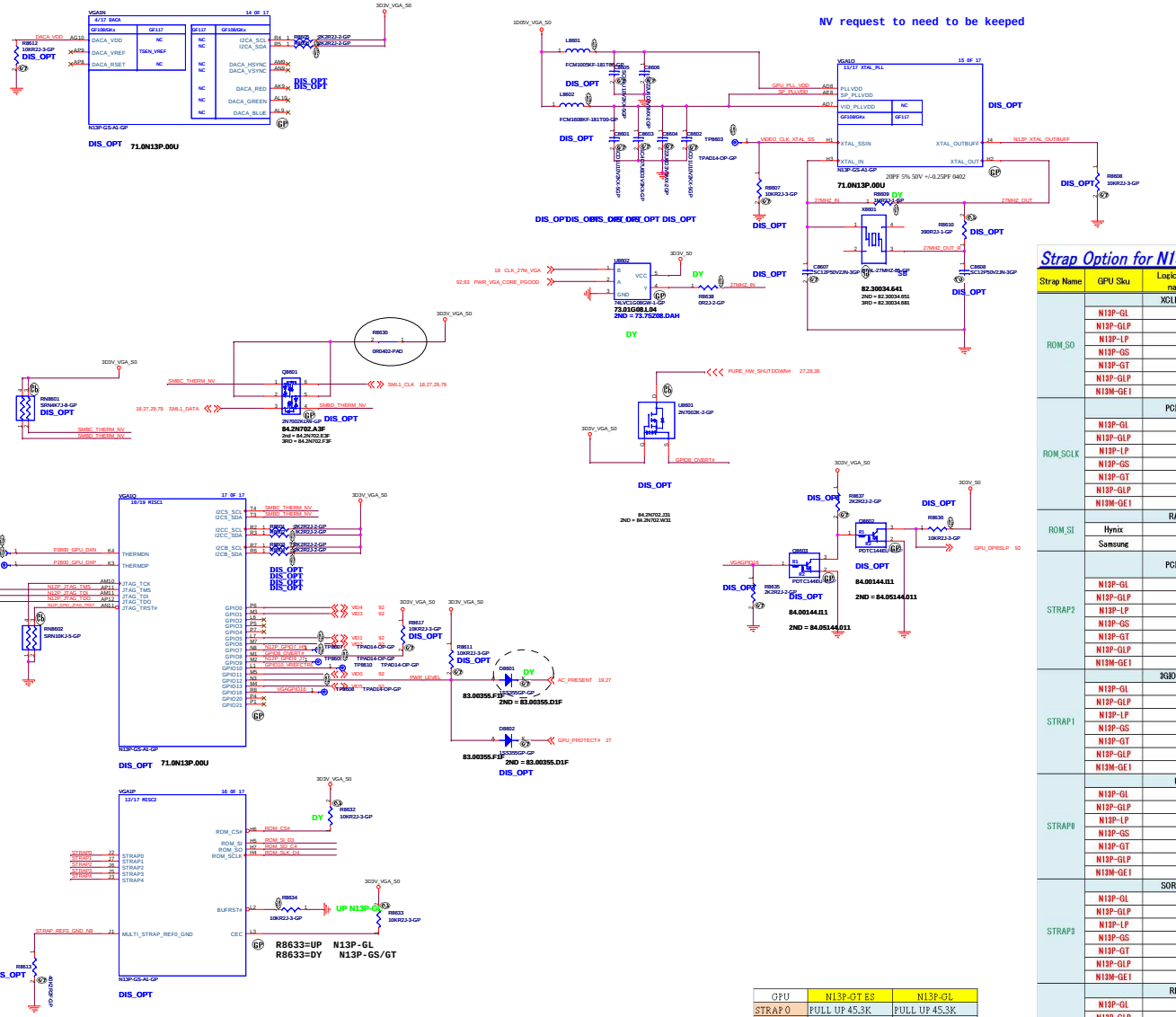

01/04/12 N13P-GL

Strap Option for N13P-GL/LP/GS/GT

Strap Name	GPU Sku	Logical strapping name bit#3	Logical strapping name bit#2	Logical strapping name bit#1	Logical strapping name bit#0	Set your BOM according to this column	Comment from NVIDIA
		XCLK_417/FB[1]	FB_0_BAR_SIZE/FB[0]	SMB_ALT_ADDR	VGA_DEVICE		
ROM_SO	N13P-GL	0	0	0	1	PULL DOWN 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13P-LP	1	0	0	1	PULL UP 10K	
	N13P-GS	1	0	0	1	PULL UP 10K	
	N13P-GT	1	0	0	1	PULL UP 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13M-GE1	0	1	0	1	PULL DOWN 30.1K	
		PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM		
ROM_SCLK	N13P-GL	0	0	1	0	PULL DOWN 15K	
	N13P-GLP	0	0	1	0	PULL DOWN 15K	
	N13P-LP	1	0	0	0	PULL UP 4.99K	
	N13P-GS	1	0	0	0	PULL UP 4.99K	
	N13P-GT	1	0	0	0	PULL UP 4.99K	
	N13P-GLP	0	0	1	0	PULL DOWN 15K	
	N13M-GE1	1	0	0	0	PULL UP 4.99K	
		RAMCFG[3]	RAMCFG[2]	RAMCFG[2]	RAMCFG[0]		
ROM_SI	Hynix	X	X	X	X	This is depends on what Vram you will use. Please check latest RVL.	
	Samsung	X	X	X	X		
		PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]		
STRAP2	N13P-GL	1	0	0	1	PULL UP 10K	N13P-GL DID => 0x0DE9
	N13P-GLP	1	0	0	0	PULL UP 4.99K	N13P-GLP DID => 0x0DE8
	N13P-LP	0	0	1	1	PULL DOWN 20K	N13P-LP DID => 0x0FD2
	N13P-GS	0	0	1	0	PULL DOWN 15K	N13P-GS QS DID =>0x0FD2
	N13P-GT	0	0	0	1	PULL DOWN 10K	N13P-GT QS DID =>0x0FD1
	N13P-GLP	1	0	0	0	PULL UP 4.99K	N13P-GLP DID => 0x0DE8
	N13M-GE1	1	0	0	0	PULL UP 4.99K	N13M-GE1 DID => 0x1058
		3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]		
STRAP1	N13P-GL	0	1	1	1	PULL DOWN 45.3K	
	N13P-GLP	0	1	1	1	PULL DOWN 45.3K	
	N13P-LP	0	1	1	0	PULL DOWN 34.8K	
	N13P-GS	0	1	1	0	PULL DOWN 34.8K	
	N13P-GT	0	1	1	0	PULL DOWN 34.8K	
	N13P-GLP	0	1	1	1	PULL DOWN 45.3K	
	N13M-GE1	0	1	1	0	PULL DOWN 34.8K	
		USER[3]	USER[2]	USER[1]	USER[0]		
STRAP0	N13P-GL	1	1	1	1	PULL UP 45.3K	
	N13P-GLP	1	1	1	1	PULL UP 45.3K	
	N13P-LP	1	1	1	1	PULL UP 45.3K	
	N13P-GS	1	1	1	1	PULL UP 45.3K	
	N13P-GT	1	1	1	1	PULL UP 45.3K	
	N13P-GLP	1	1	1	1	PULL UP 45.3K	
	N13M-GE1	1	1	1	1	PULL UP 45.3K	
		SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED		
STRAP3	N13P-GL	0	0	0	0	PULL DOWN 4.99K	No display for Optimus sku
	N13P-GLP	0	0	0	0	PULL DOWN 4.99K	
	N13P-LP	0	0	0	0	PULL DOWN 4.99K	
	N13P-GS	0	0	0	0	PULL DOWN 4.99K	
	N13P-GT	0	0	0	0	PULL DOWN 4.99K	
	N13P-GLP	0	0	0	0	PULL DOWN 4.99K	
	N13M-GE1	0	0	0	0	PULL DOWN 4.99K	
		RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V		
STRAP4	N13P-GL	0	0	0	1	PULL DOWN 10K	
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13P-LP	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GS	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GT	0	1	1	1	PULL DOWN 45.3K	For GEN2 only system, pull down 20K
	N13P-GLP	0	0	0	1	PULL DOWN 10K	
	N13M-GE1	0	0	0	1	PULL DOWN 10K	

GPU	N13P-GT ES	N13P-GL
STRAP 0	PULL UP 45.3K	PULL UP 45.3K
STRAP 1	PULL DOWN 34.8K	PULL DOWN 45.3K
STRAP 2	PULL UP 20K	PULL UP 10K
STRAP 3	PULL DOWN 4.99K	PULL DOWN 4.99K
STRAP 4	PULL DOWN 10K	PULL DOWN 10K
ROM_SO	PULL UP 10K	PULL DOWN ~~30.1K~~ 10KR by NV
ROM_SCLK	PULL UP 4.99K	PULL DOWN 15K

V-RAM	ROM_SI
64M*16 DDR3 Samsung	PULL DOWN 20K
64M*16 DDR3 Hynix	PULL DOWN 15K
128M*16 DDR3 Samsung	PULL DOWN 45.3K
128M*16 DDR3 Hynix	PULL DOWN 34.8K
64M*16 GDDR5 Samsung	PULL DOWN 45.3K
64M*16 GDDR5 Hynix	PULL DOWN 34.8K
128M*16 GDDR5 Samsung	PULL DOWN 30.1K
128M*16 GDDR5 Hynix	PULL DOWN 24.9K

Part Reference	Part Number	Value	PCB Footprint
R8621(DIS_ROM SI)	64.20025.6DL	20KR2F-L-GP	R402H16
R8621	64.15025.6DL	15KR2F-GP	R402H16
R8621	64.34825.6DL	34K8R2F-L-GP	R402H16
R8621	64.45325.6DL	45K3R2F-L-GP	R402H16
R8621	64.30125.6DL	30K1R2F-L-GP	R402H16
R8621	64.24925.6DL	24K9R2F-L-GP	R402H16

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GPU_POWER(4/5)

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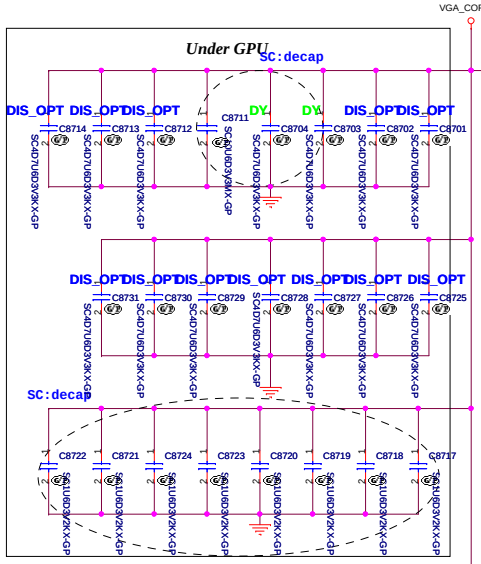
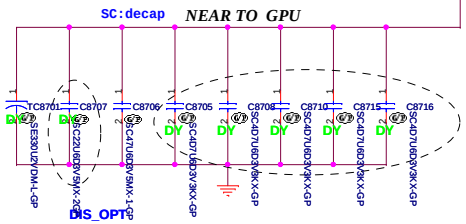
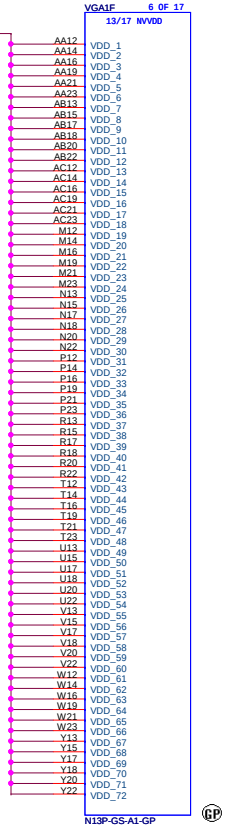
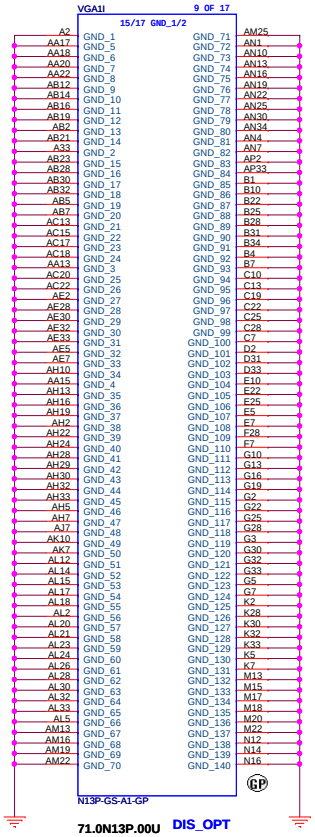
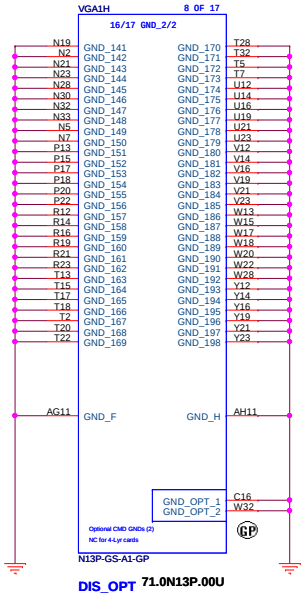
EDP 60A (TDP 55W)

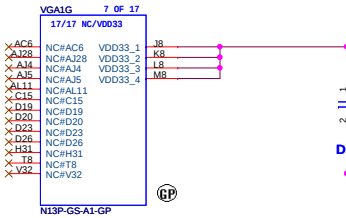


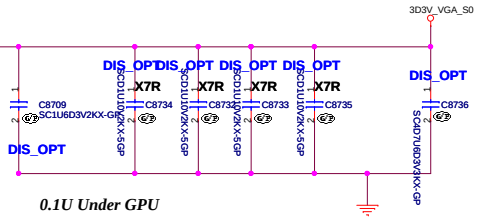












<Variant Name>

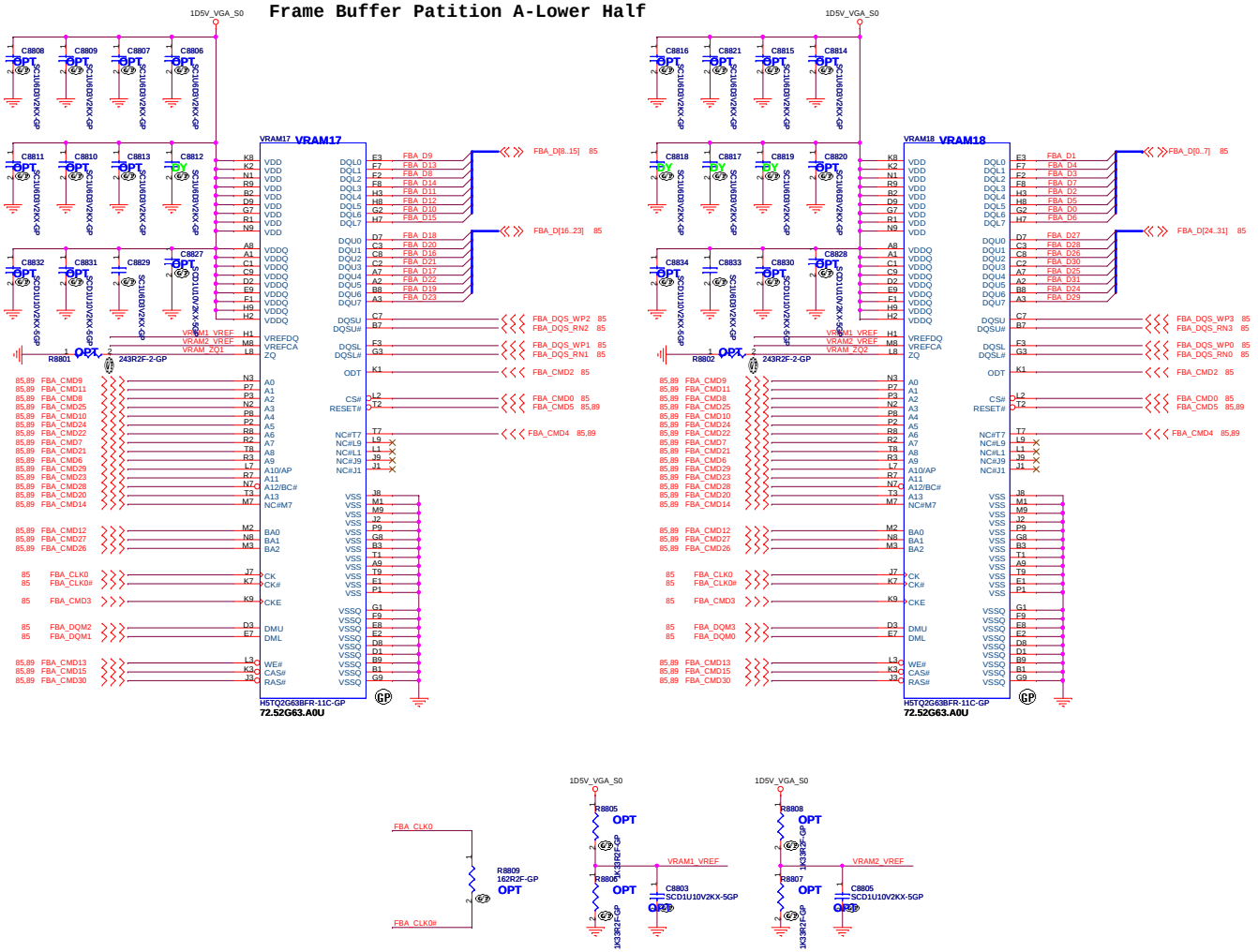
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_DPPWR/GND(5/5)

Size: Custo | Document Number: Colossus | Rev: 1

Date: Wednesday, January 04, 2012 | Sheet 87 of 103

Frame Buffer Patition A-Lower Half



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

Size: A2 | Document Number: Colossus | Rev: 1

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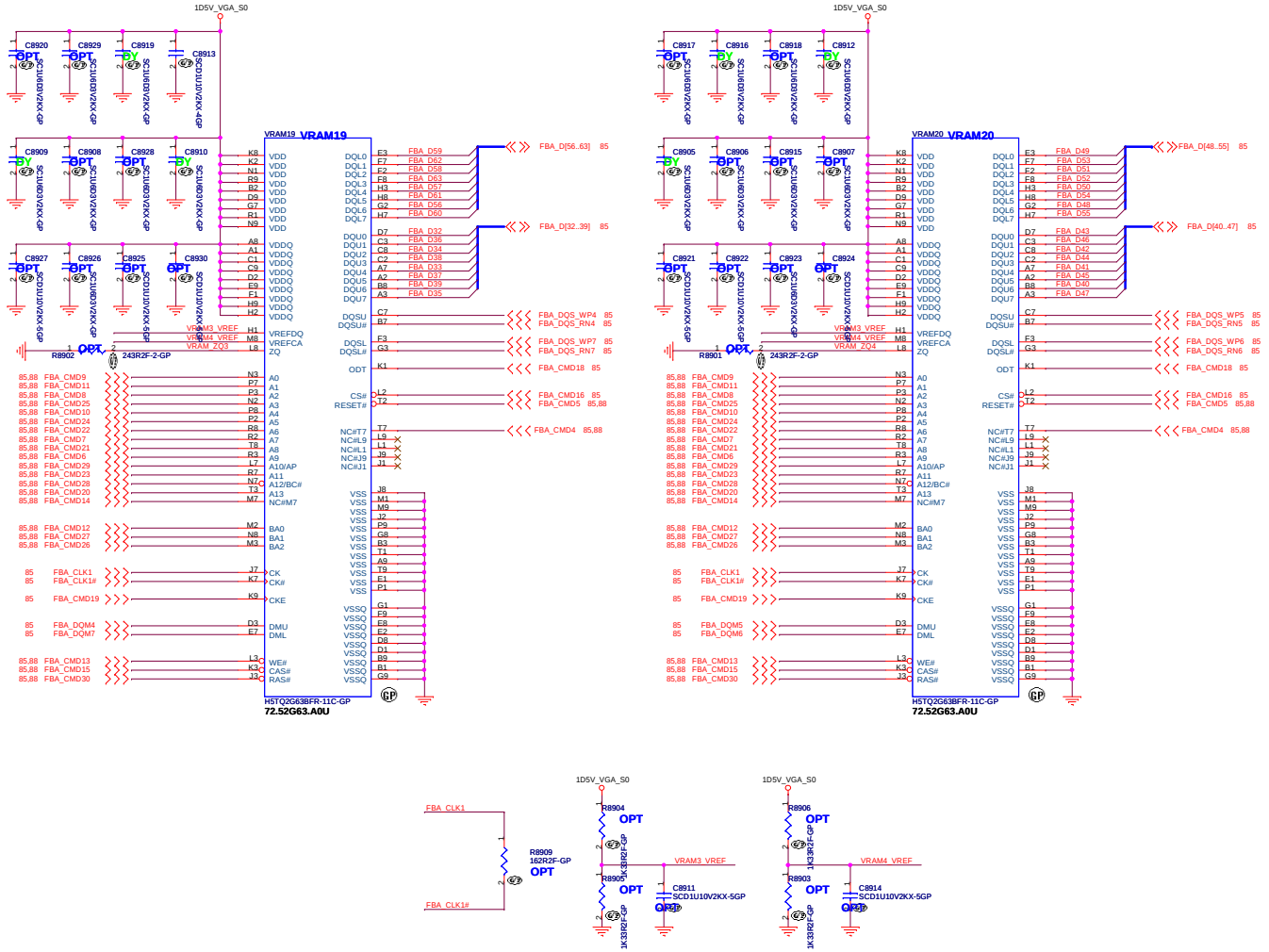
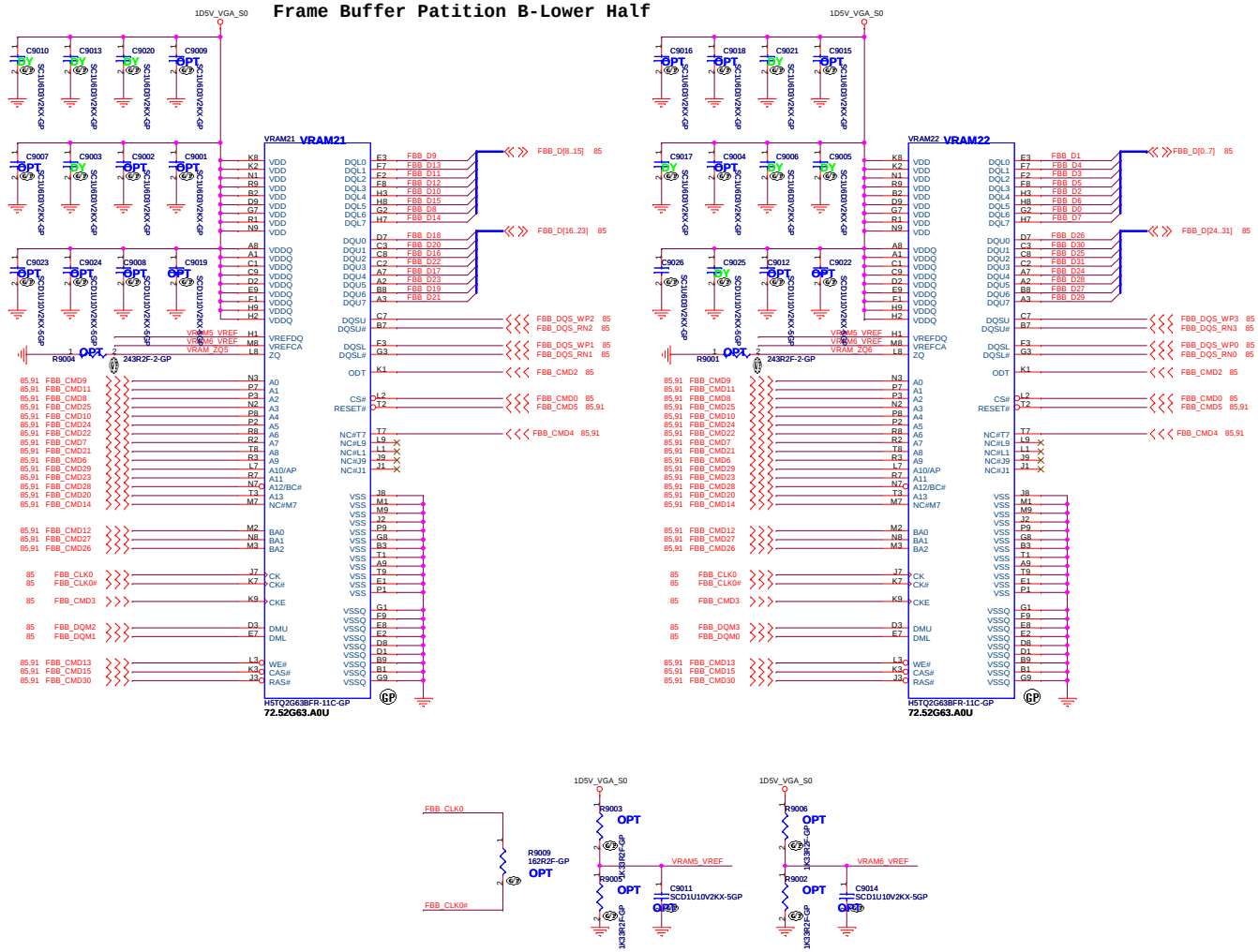
Frame Buffer Patition A-Upper Half



<Variant Name>	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GPU-VRAM3,4 (2/4)	
Size: A2	Document Number: Colossus	Rev: 1
Date: Wednesday, January 04, 2012	Sheet 89 of 103	

Frame Buffer Patition B-Lower Half



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A2 | Document Number: Colossus | Rev: 1

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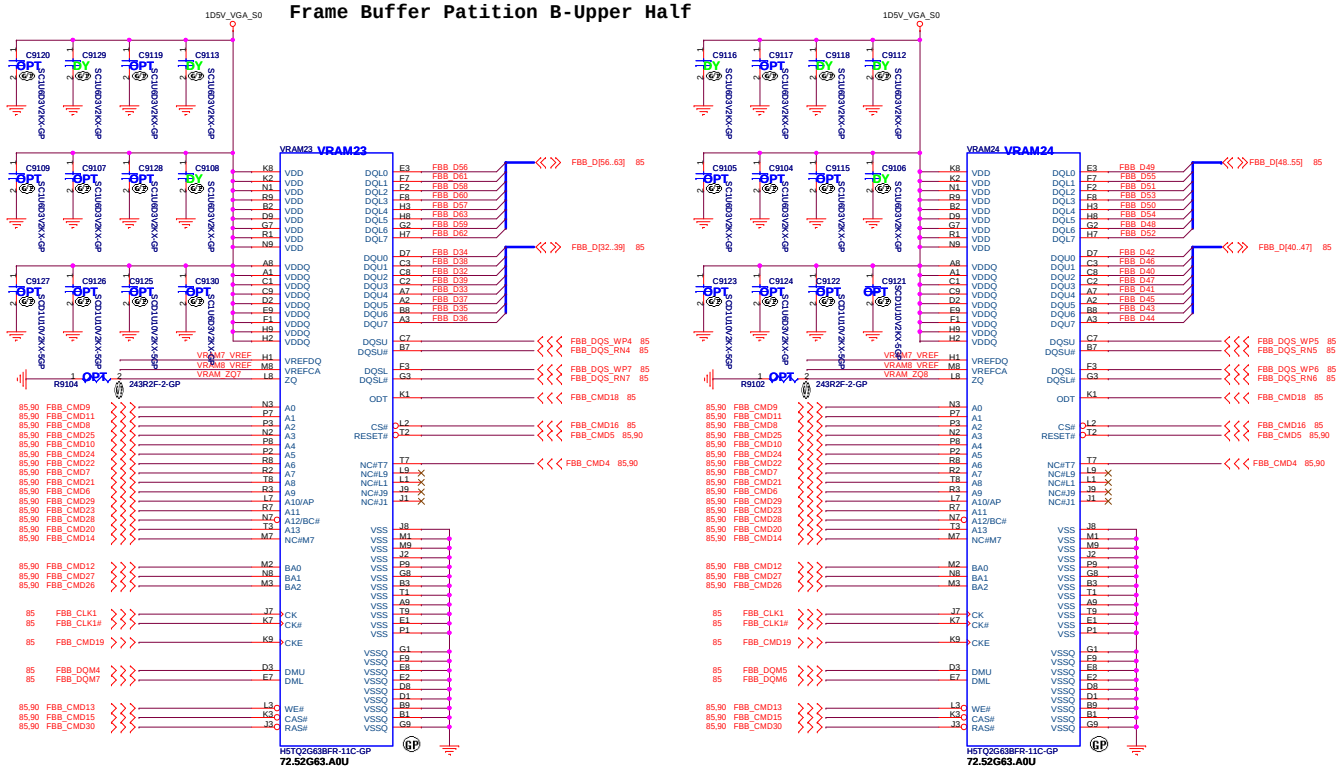
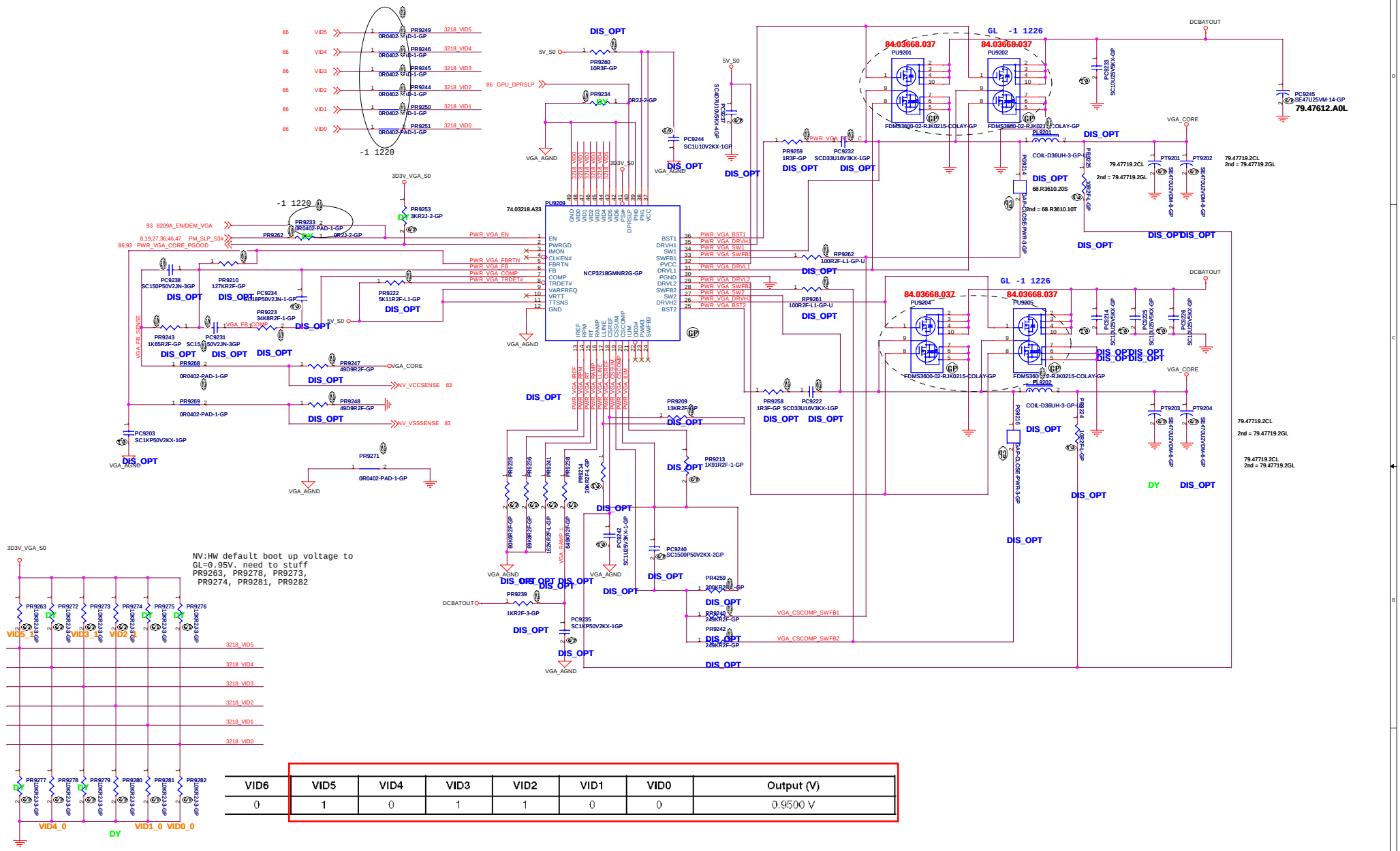
Frame Buffer Patition B-Upper Half





VID6	VID5	VID4	VID3	VID2	VID1	VID0	Output (V)
0	1	0	1	1	0	0	0.9500 V

<Core Design>
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Taipei Hsien 221, Taiwan, R.O.C.

Title: NCP3218 VGACORE25W

Size: A2 | Document Number: Colossus | Rev: 1

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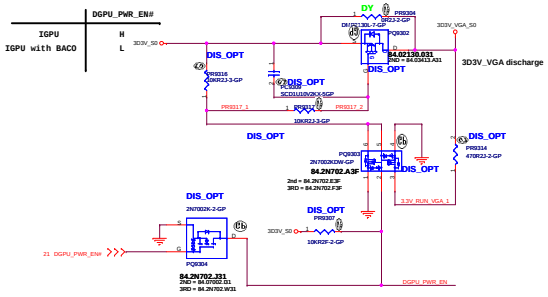
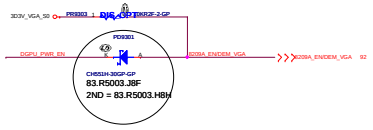
VGA chip sequence: 3V_VGA_S0>VGA_CORE>1D5V_VGA>1D05V_VGA

3V_VGA_S0 → VGA_CORE → 1.5V_VGA_S0





1D5V_VGA_S0
Design current = 9A

100mils or Copper Shape

400mils or Copper Shape

Design Current = 9A

Close to PL9331

Close to output MLCC

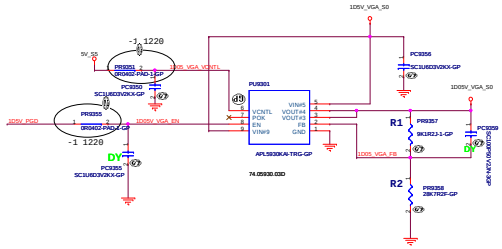
Diff pair

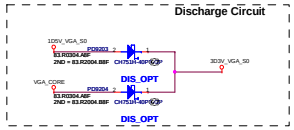
VSENSE-TRACE
ROUTED DIFFERENTIALLY
PARALLEL TO VSENSE+

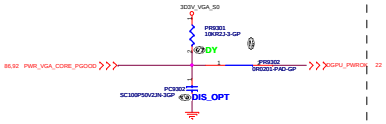
1D05V_VGA

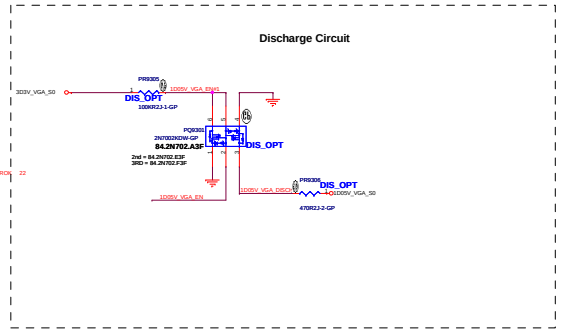
3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D5V_VGA_S0 should ramp up
so 1D05V_VGA_S0 EN have to fine tune RC delay after VGA_Core

1D05V_VGA_S0
Design current = 3.8A









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Title: DISCRETE VGA POWER
Size: A1 | Document Number: Colossus | Rev: 1
Date: Wednesday, January 04, 2012 | Sheet 88 of 103

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<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

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(Blanking)

<Core Design>

緯創資通 Wistron Corporation
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Title: *Reserved*

Size	Document Number	Rev
A3	Colossus	1

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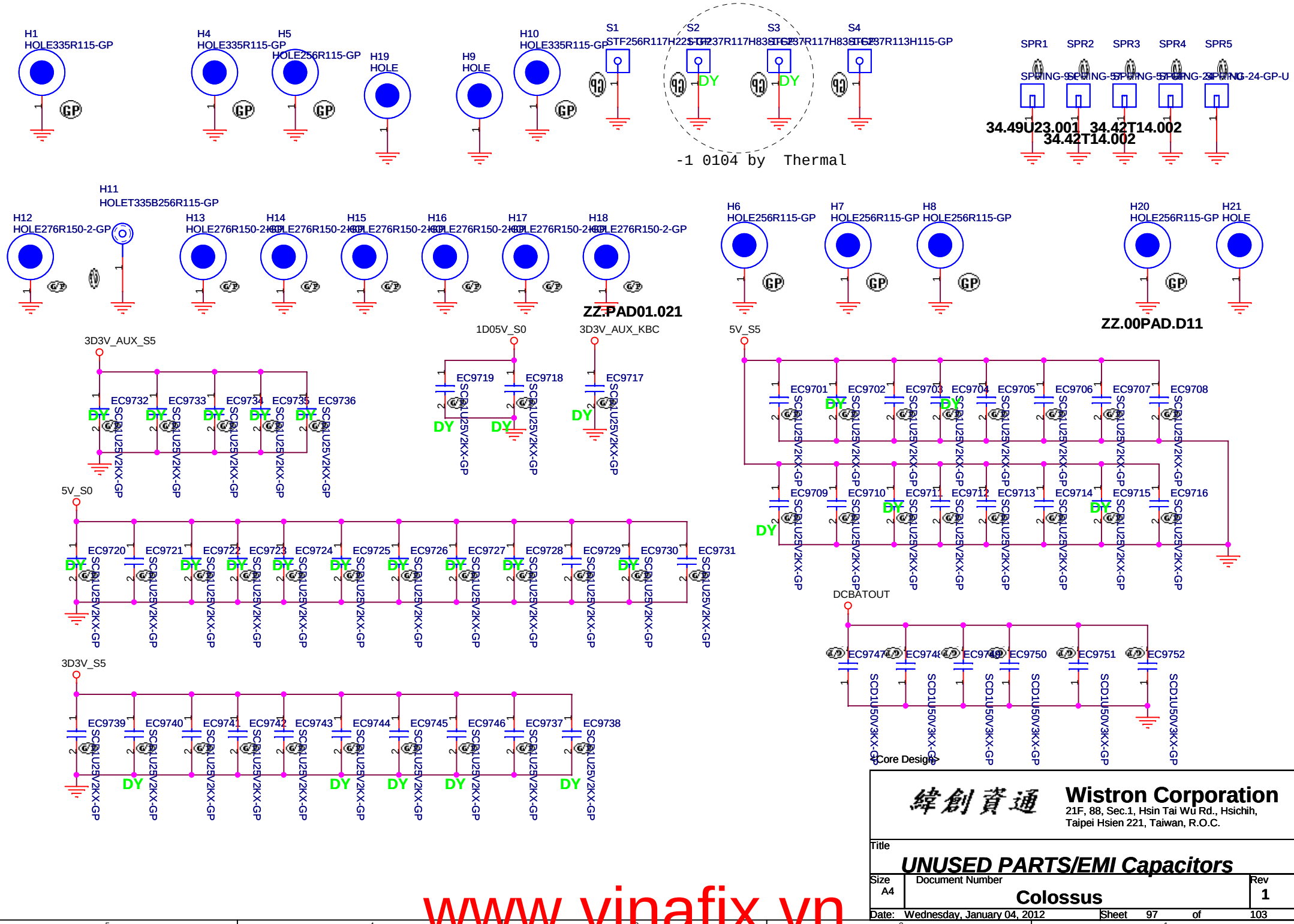

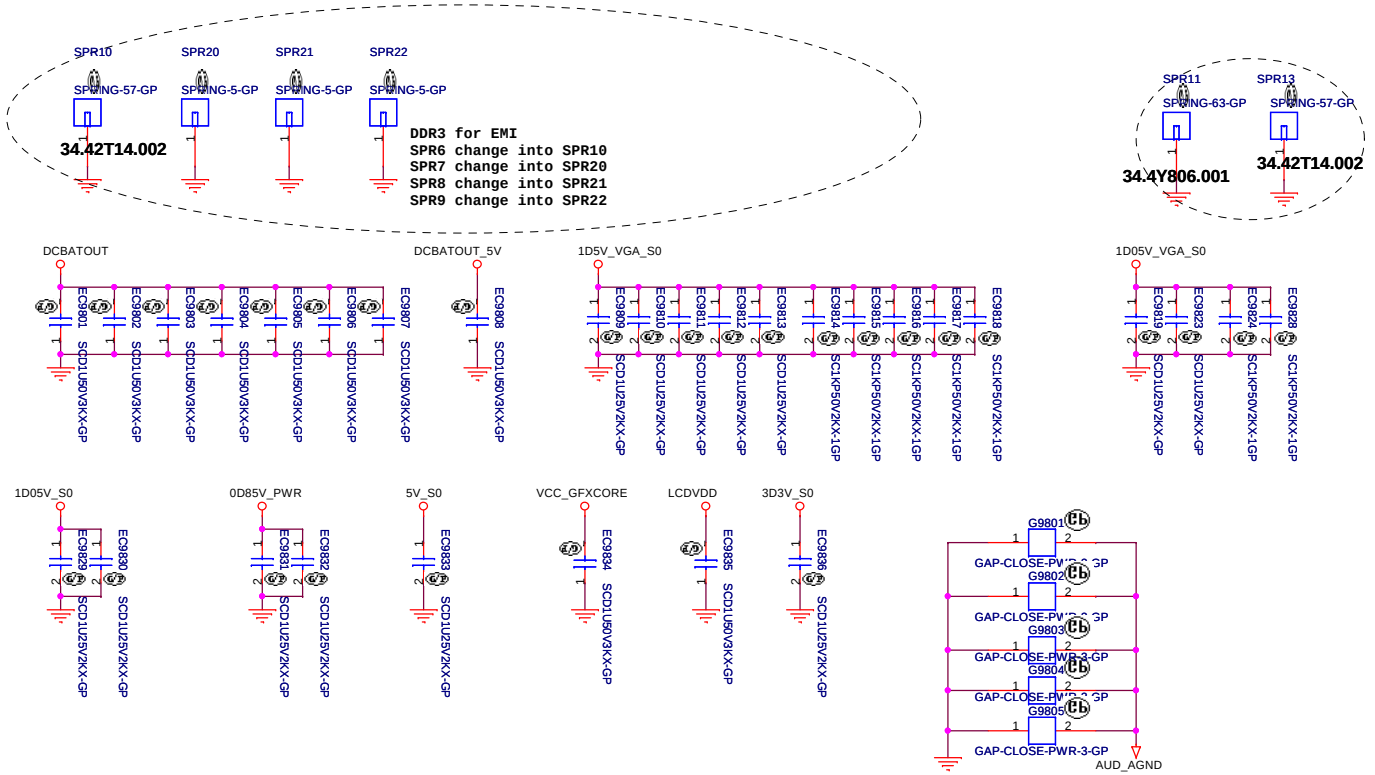

<Core Design>

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Title: ***Change History***

Size	Document Number	Rev
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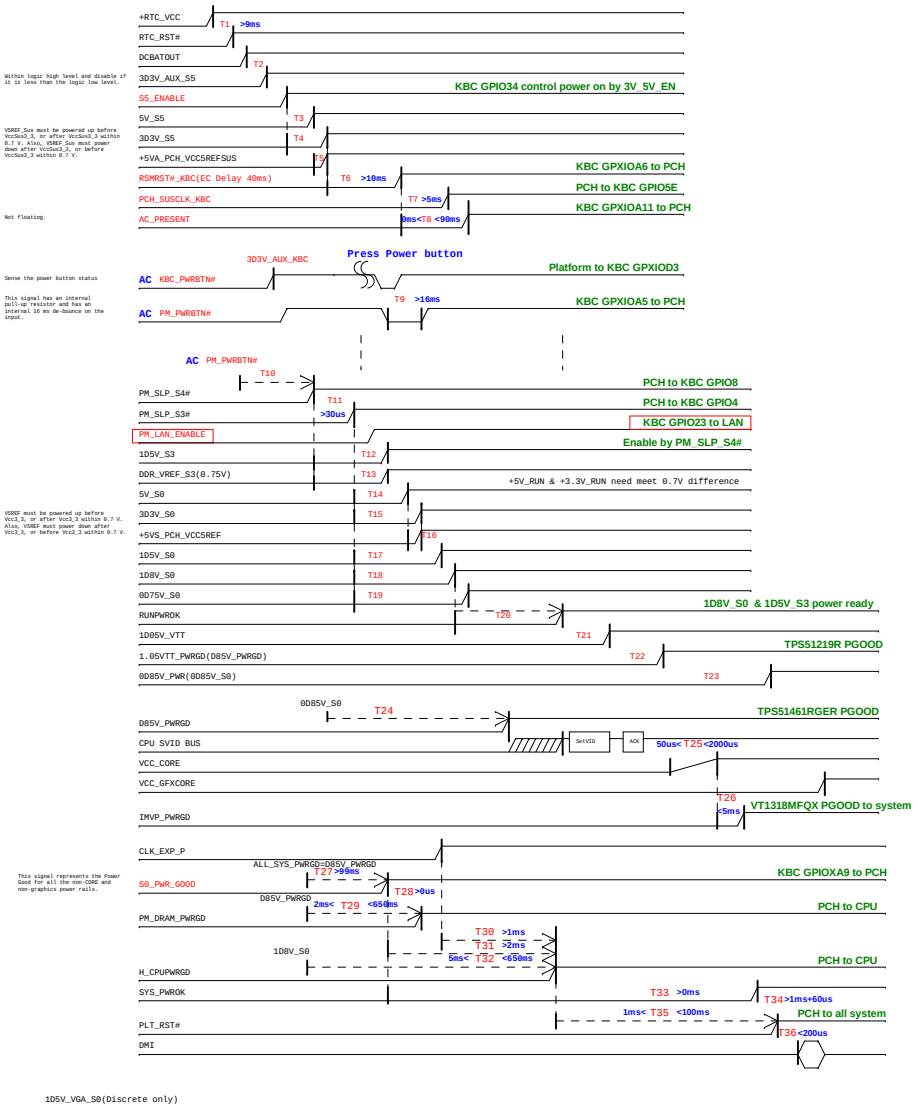
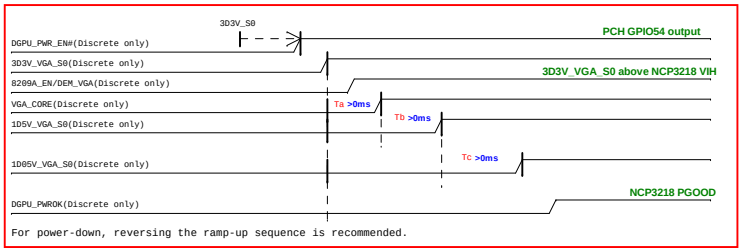
Chief River Platform Power Sequence

(AC mode)

red word: KBC GPIO



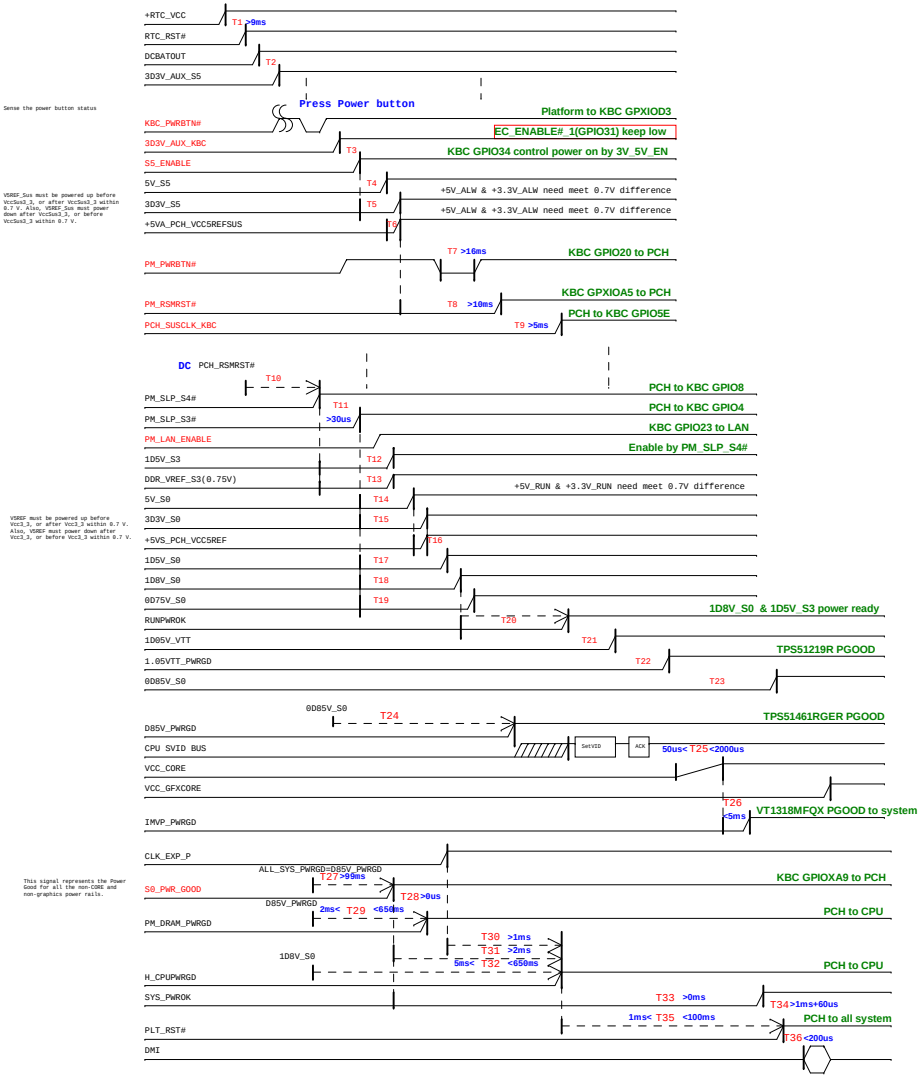
N13P Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

red word: KBC GPIO



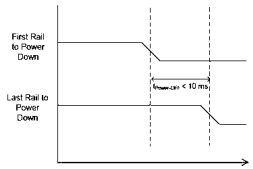


Figure 18. Recommended Power Off Sequencing Order

<Core Design>

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Title: Power Sequence

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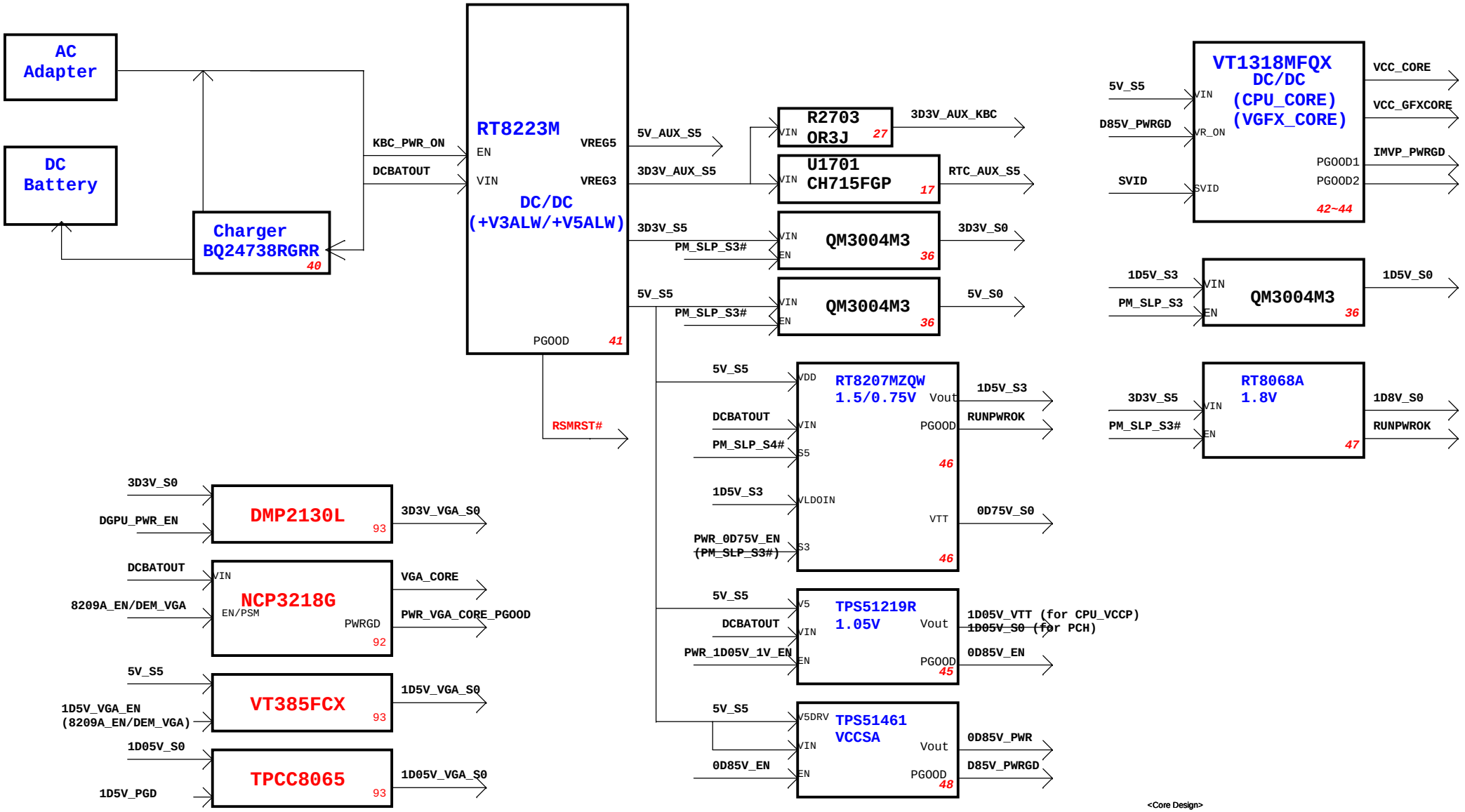
COLOSUSS POWER BLOCK DIAGRAM



<Core Design>

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Title: Power Block Diagram

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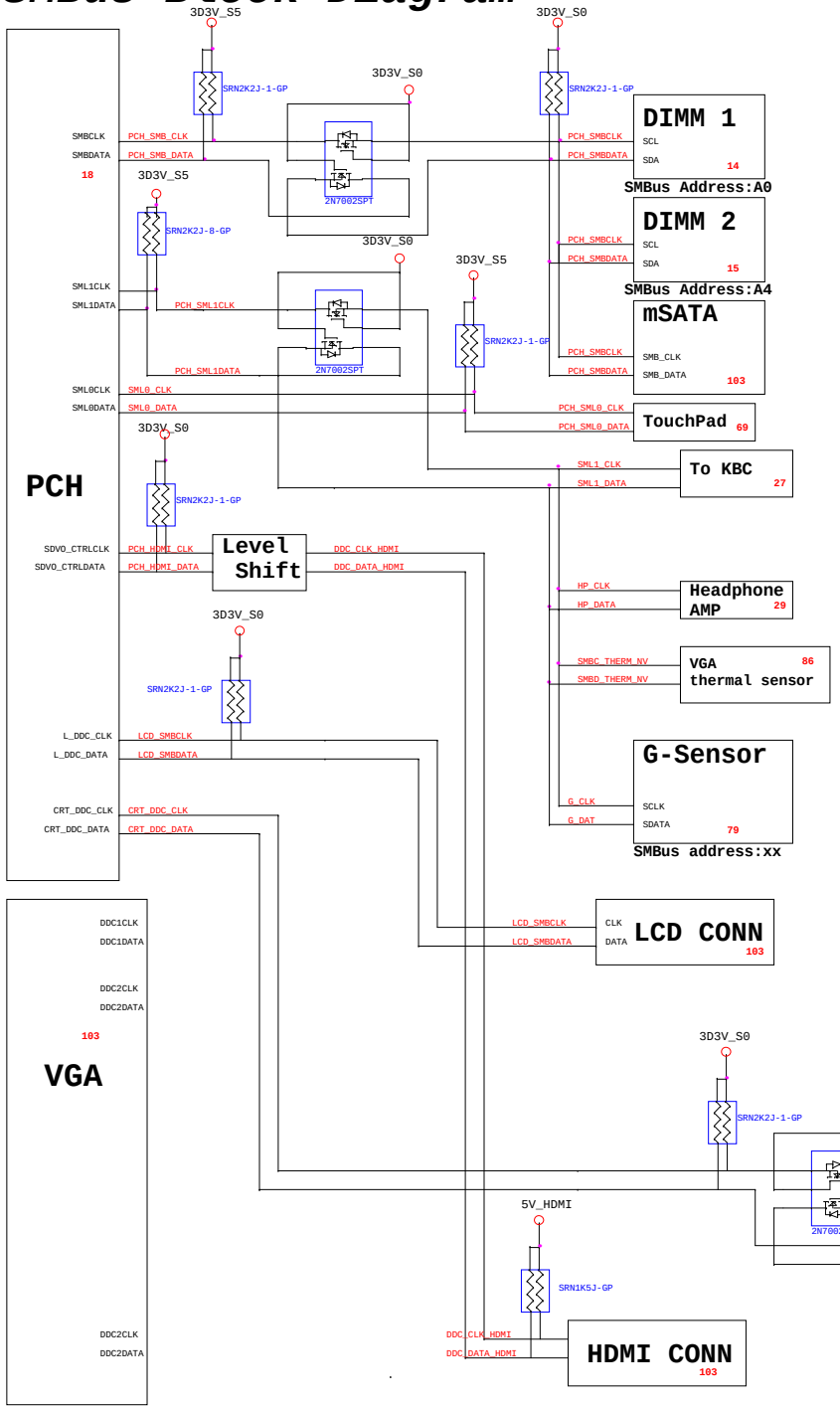
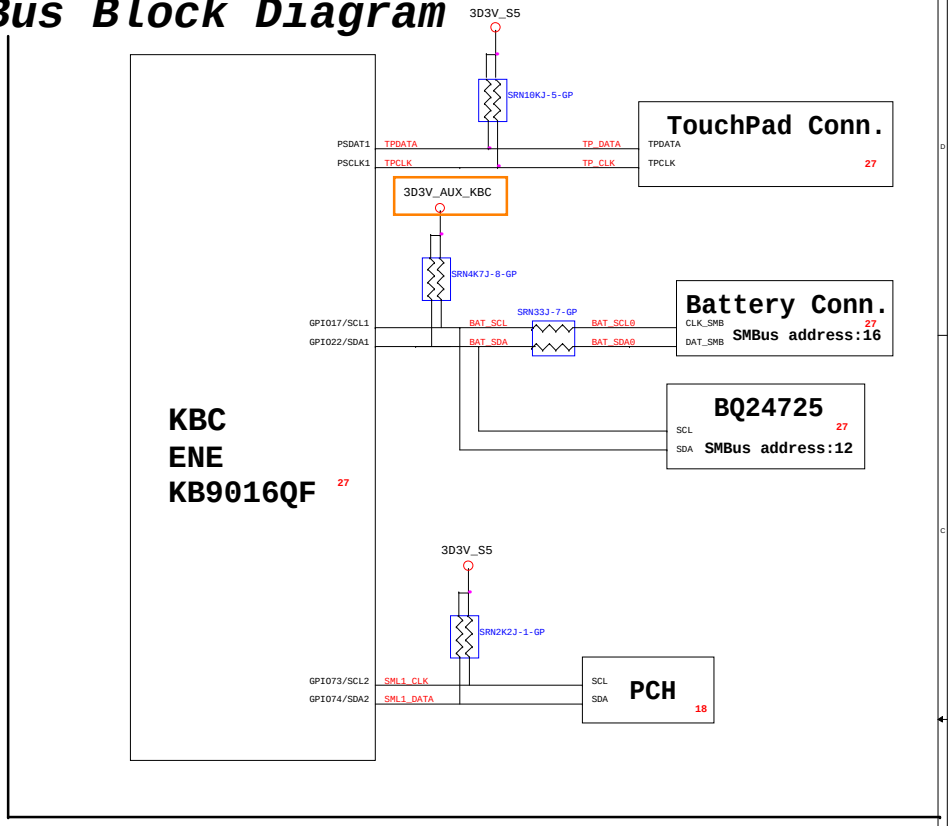
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

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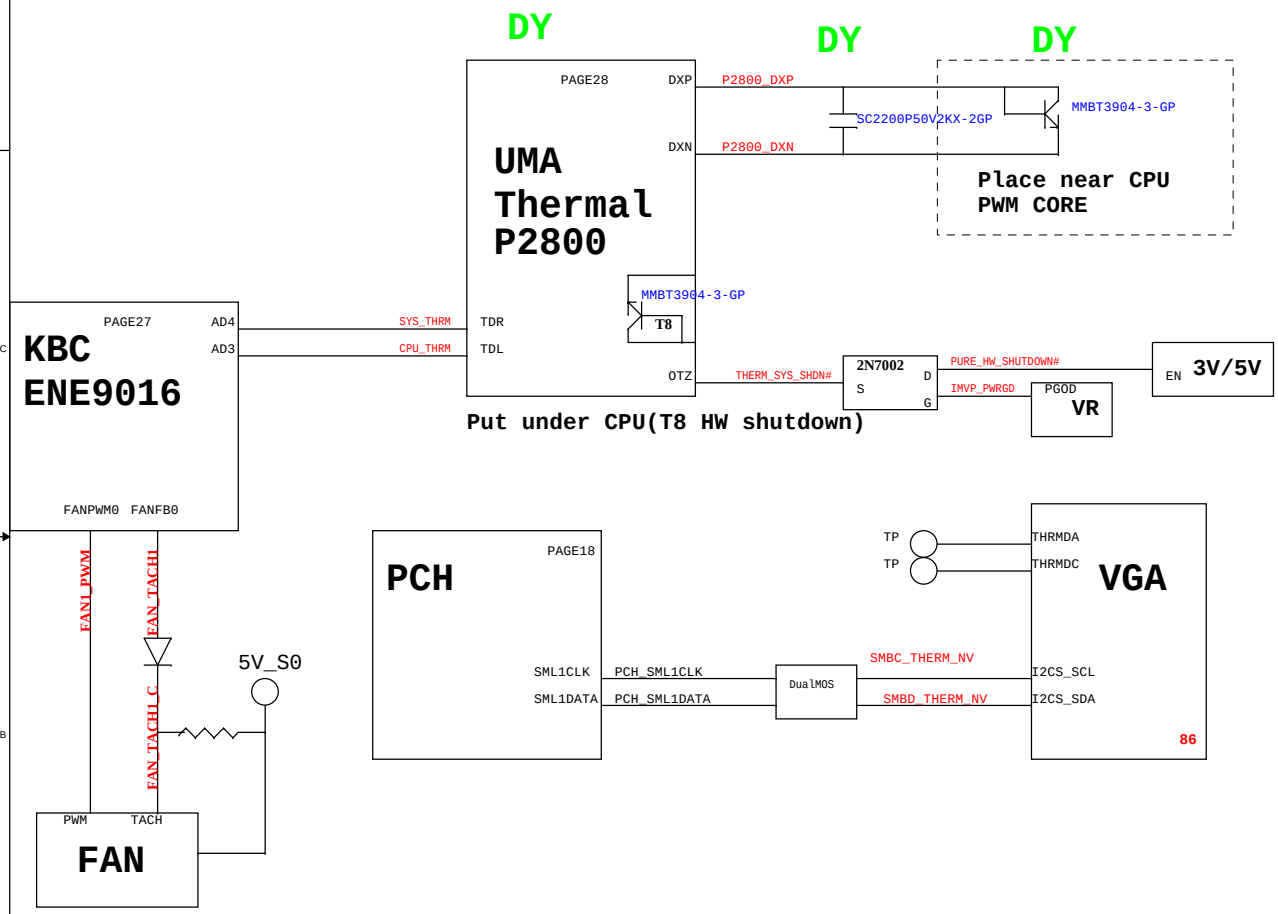
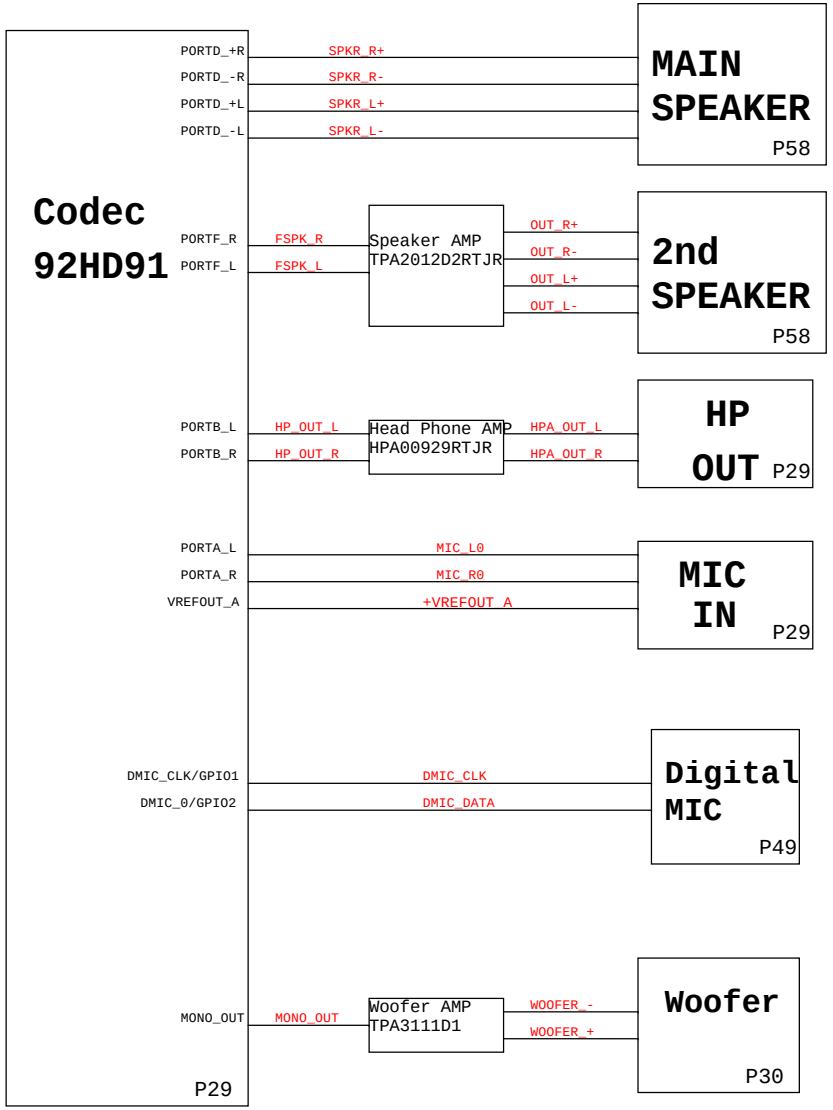
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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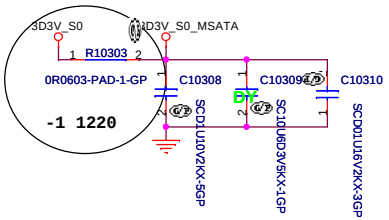
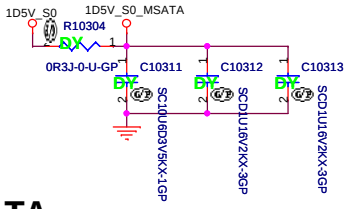
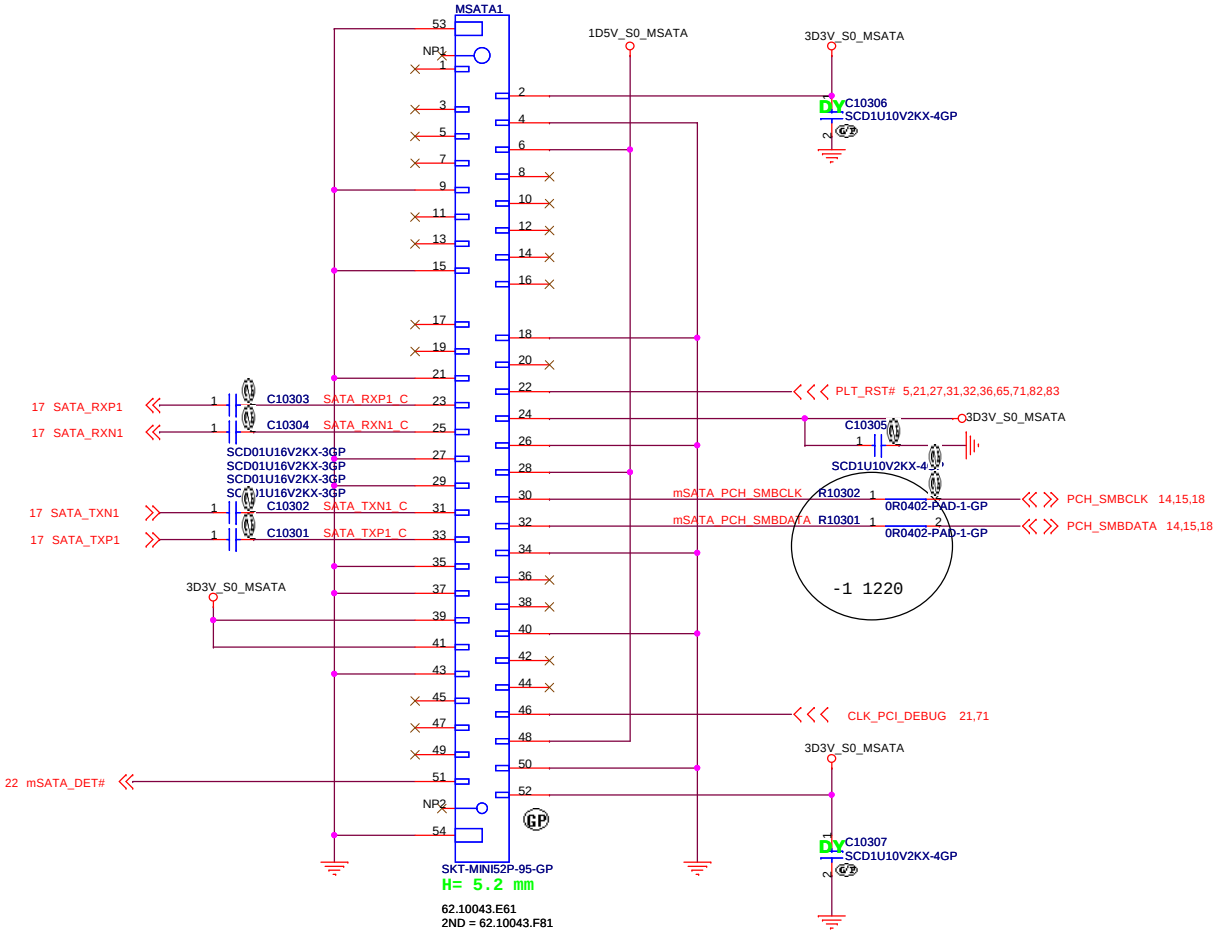




mSATA



677867-FM5

Pin #	Name	Description		Pin #	Name	Description
1	Reserved	NC		2	V33	3.3V power
3	Reserved	NC		4	GND	Return Current Path
5	Reserved	NC		6	V15	1.5V power (Unused)
7	Reserved	NC		8	Reserved	NC
9	GND	Return Current Path		10	Reserved	NC
11	Reserved	NC		12	Reserved	NC
13	Reserved	NC		14	Reserved	NC
15	GND	Return Current Path		16	Reserved	NC
		Key				
17	Reserved	NC		18	GND	Return Current Path
19	Reserved	NC		20	Reserved	NC
21	GND	Return Current Path		22	Reserved	NC
23	B+	Differential Signal Pair B (Device Tx)		24	V33	3.3V power
25	B-			26	GND	Return Current Path
27	GND	Return Current Path		28	V15	1.5V power (Unused)
29	GND	Return Current Path		30	Reserved	NC
31	A-	Differential Signal Pair A (Device Rx)		32	Reserved	NC
33	A+			34	GND	Return Current Path
35	GND	Return Current Path		36	Reserved	NC
37	GND	Return Current Path		38	Reserved	NC
39	V33	3.3V power		40	GND	Return Current Path
41	V33	3.3V power		42	Reserved	NC
43	GND	Return Current Path		44	Reserved	NC
45	Vendor	No connect at Host side		46	Reserved	NC
47	Vendor	No connect at Host side		48	V15	1.5V power (Unused)
49	DAS/DSS*1	Drive Activity Signal		50	GND	Return Current Path
51	Presense*2	Device Presense		52	V33	3.3V power

Note: *1: DAS/DSS signal is not use for this drive. (DAS Signal output is optional)

*2: Presense pin is Connected to GND by device side. (220Ω Pull Down)

1st	677867-FM5
2nd	677867-AM5
3rd	677867-BM5
4th	677867-LM5

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: mSATA

Size: A3 | Document Number: Colossus | Rev: 1

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