H61H2-M17 Rev : 1.0

ECS CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
P61G V1.0	2011/04/07	RED_PCB P/N : 15-Y97-011001 (GE1) / 15-Y97-011000 (CHUANYI) BOM P/N : 81-605-Y97100 EC35 change to EC-cap 1000U-6.3DL EC1, EC4 from 100uF change to 220uF Del RT1, RT3, R137, R180 (Not need compensation of temperature). For 5VSB Inrush Current : R102 from 100k change to 33k. Select TACH0_GPIO17 to decide COM .
H61H2-M12 VA	2011/05/04	Black_PCB P/N : 15-EC7-010010 BOM P/N : 81-605-EC7000/81-605-EC7001(10/100 ; GiGA) PCB Size change to 225*170 mm Del DVI Vcore 減少一相 VIN 電容減少一顆 LAN change to Atheros 8152/8151/8161 Codec change to VT1705CE. USB Power use fuse & Jumper.
H61H2-M12 V1.0	2011/07/12	Black_PCB P/N : 15-EC7-011000/15-EC7-011001 BOM P/N : 89-206-EC7100 / 89-206-EC7101 (10_100 / GIGA) Page 17, Power VCC_DDC change to VCC. PCB Size change to 225*170 mm
H61H2-M17 V1.0	2012/04/16	PAGE 9,10,11:Change CPU VRM solution to Richtek. PAGE 14&22:Add USB*2. PAGE 17&21:Add HDMI. PAGE 26:Change to Giga LAN AR8151-B default.

NOTE:
Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_2_1.pdf,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip

RD : Leon Tang
LAYOUT : Run Ouyang
EMI : Light Wang

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Title	Cover Page	
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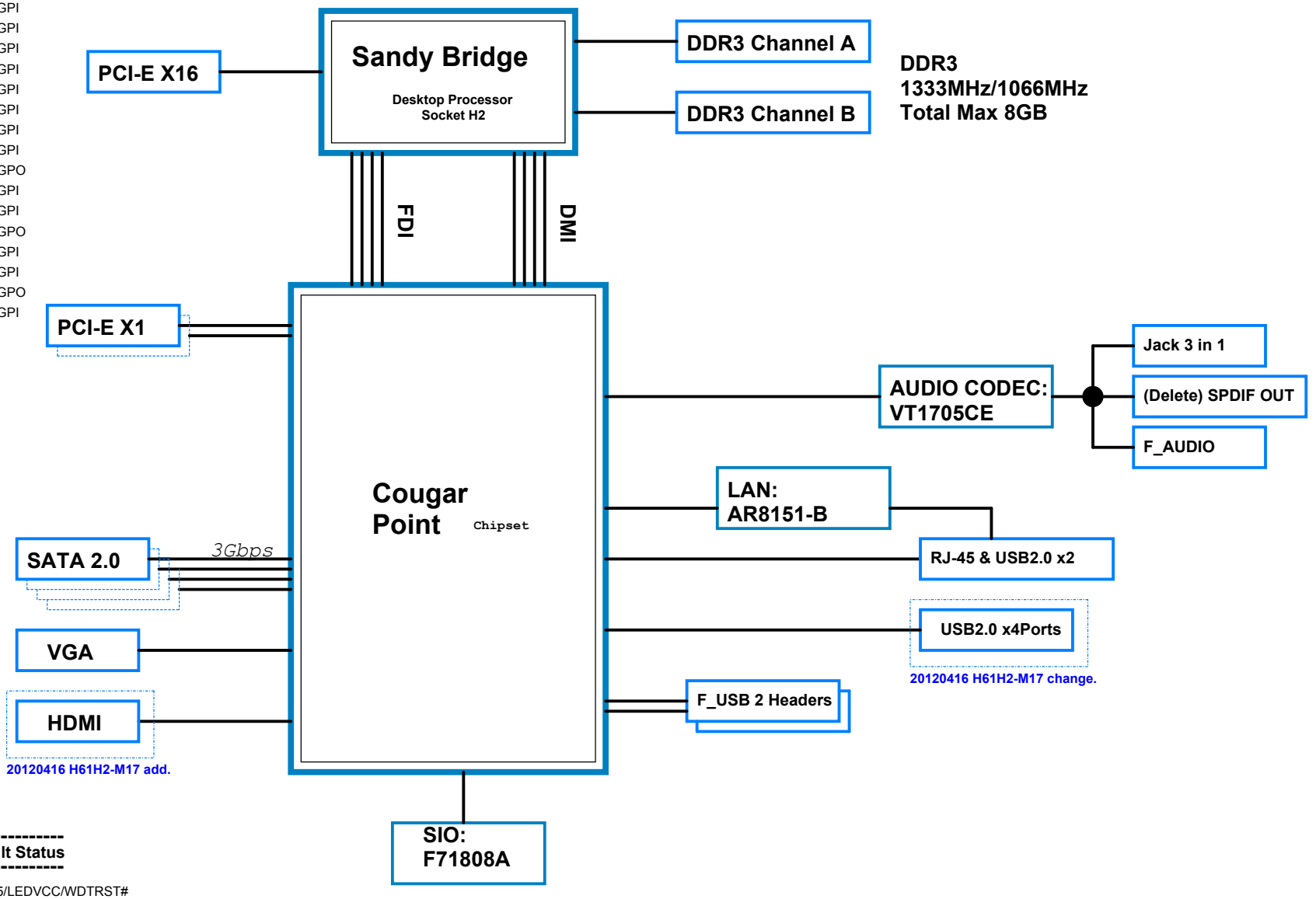
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI
GPIO15	3VSB	Down Voltage for DIMM	GPO
GPIO48	VCC3	Down Voltage for DIMM	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
PIN23	5VSB	Power LED	GPIO25/LEDVCC/WDTRST#
PIN22	5VSB	Power LED	GPIO24/LEDVSB
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

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Title: Block Diagram

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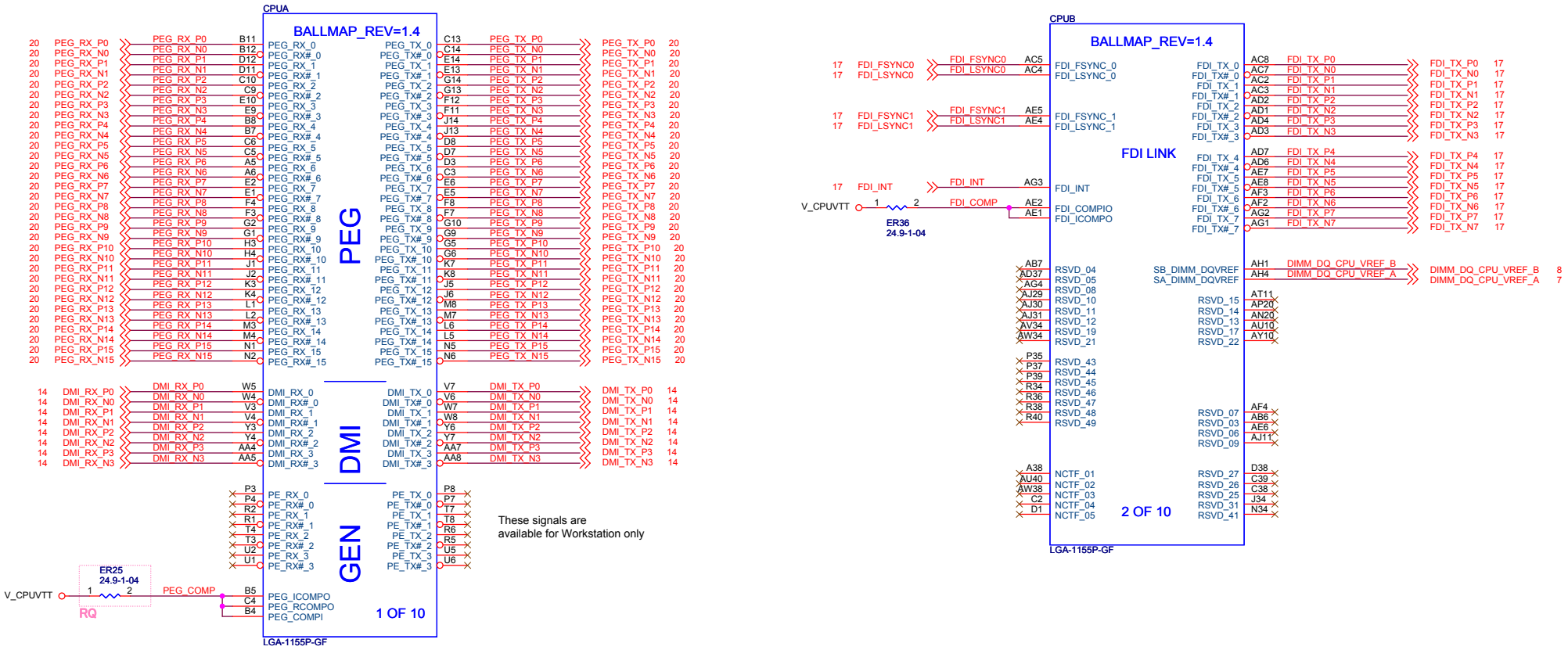


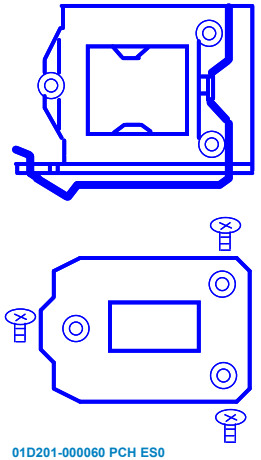
SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4MIL TRACE TO RQ.
1 ROUTE B5 TO RQ. 1 AS A SEPERATE 12MIL TRACE.

1228'10 Jayson :
Part number modified

11-018-115124 SOCKET.CPU..LGA 1155P SMD..G/F...
BLACK.ACA-ZIF-096-P02....LEAD-FREE(RoHS/HF).LOTES

20-800-005711 SUBASSY.STEEL....LGA 1155/1156P.....W/BACK
PLATE,CAP.ACA-ZIF-082-P32....LEAD-FREE(RoHS/HF).LOTES

CPU(104)
CPU_SUBASSY_STEEL



01D201-000060 PCH ES0

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Title	CPU - DMI/FDI/PEG		
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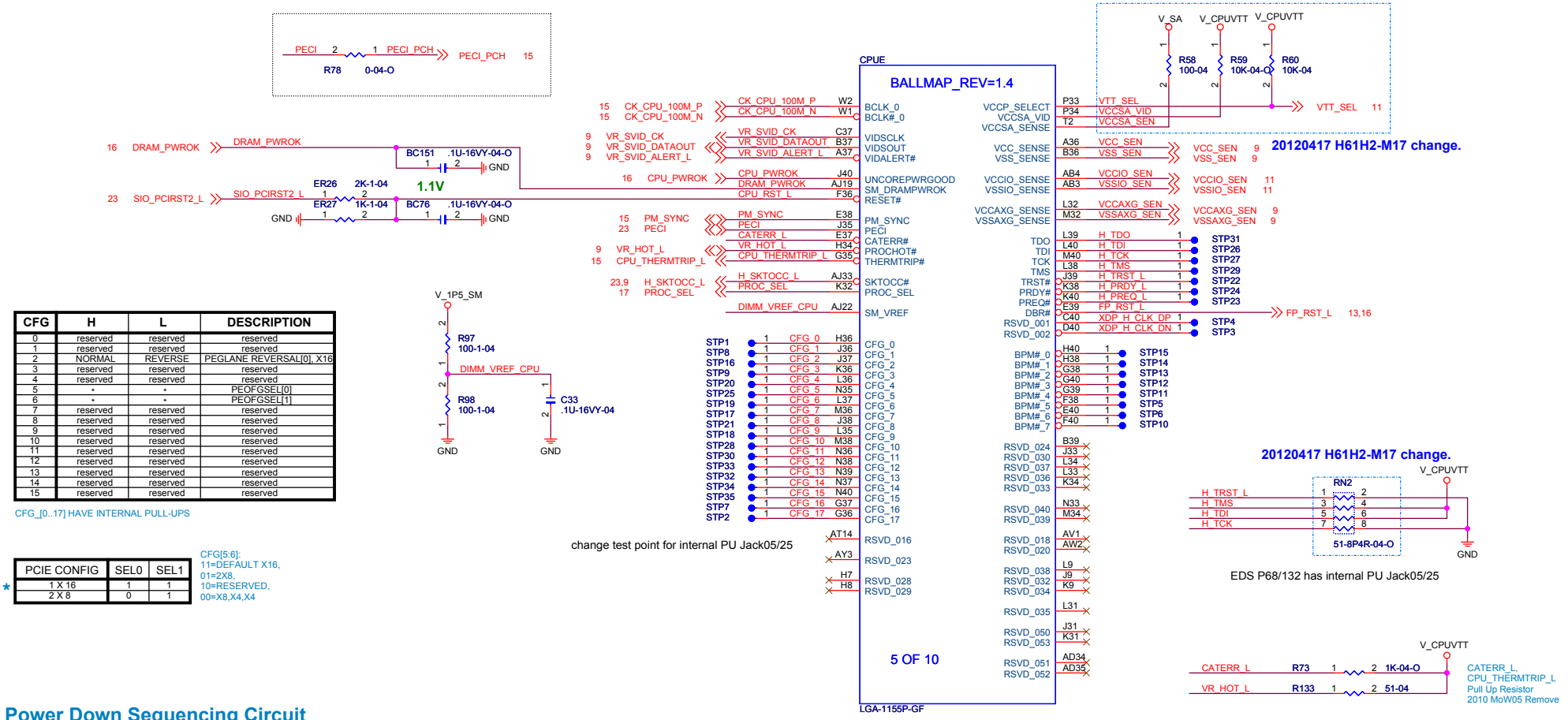


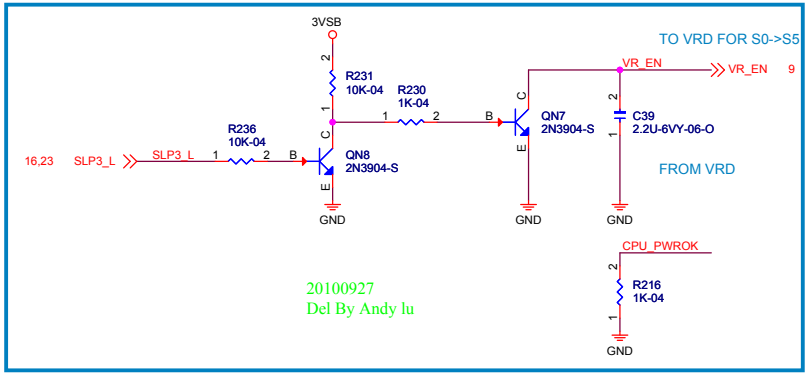
CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:
11=DEFAULT X16,
01=2X8,
10=RESERVED,
00=X8,X4,X4

Power Down Sequencing Circuit



Elitegroup Computer Systems		
Title: CPU - MISC		
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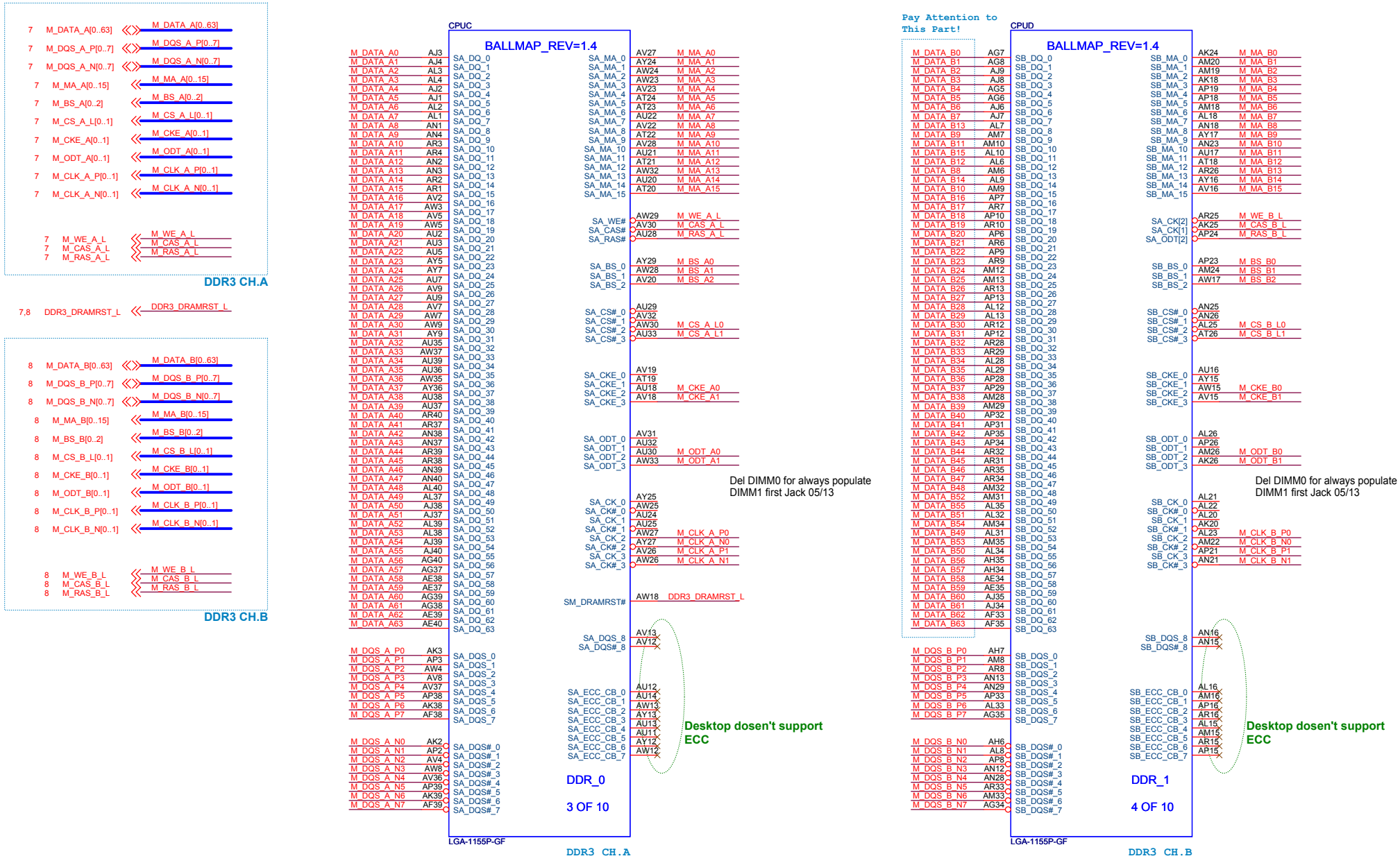

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Title: CPU - DDR3

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MAX 112A

1.05V/1.00V
MAX 8.5A

1.5V
MAX 4.5A

MAX 35A

0.925V/0.85V
MAX 8.8A

1.8V
MAX 1A

MC34/MC107 move to Vaxg path as vendor 08/04

20101021
Add By Andy lu

20100929
Change By Andy lu

20101014
Add By Andy lu

20101014
Add By Andy lu

20101014
Add By Andy lu

20100929
Change By Andy lu

Title	CPU - PWR
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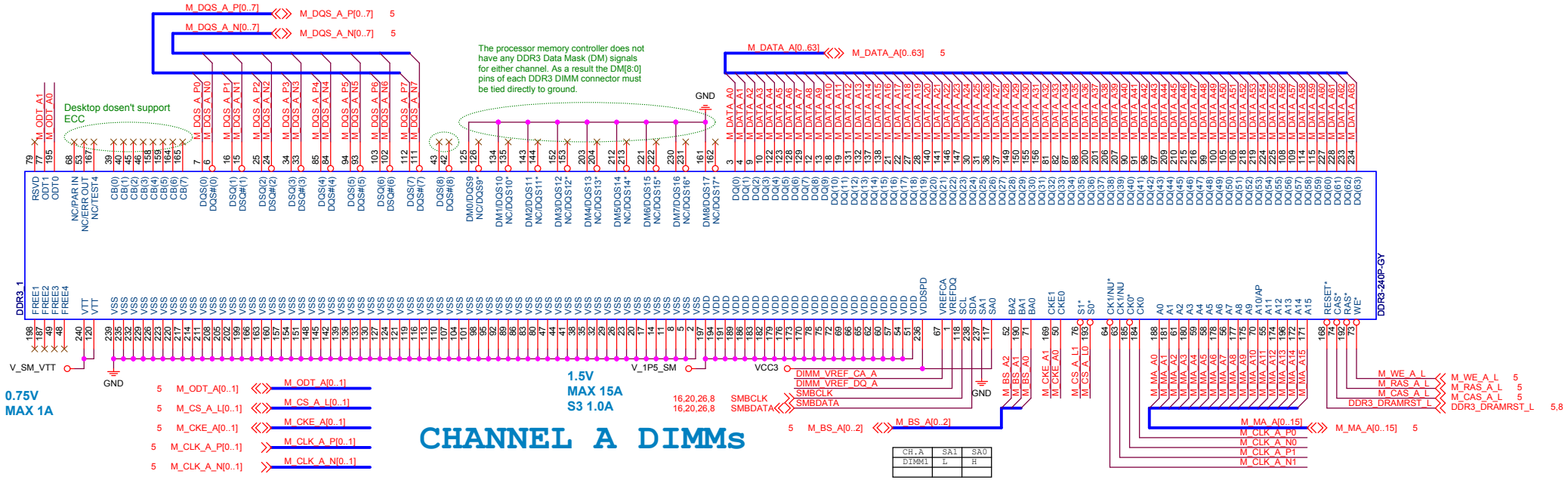
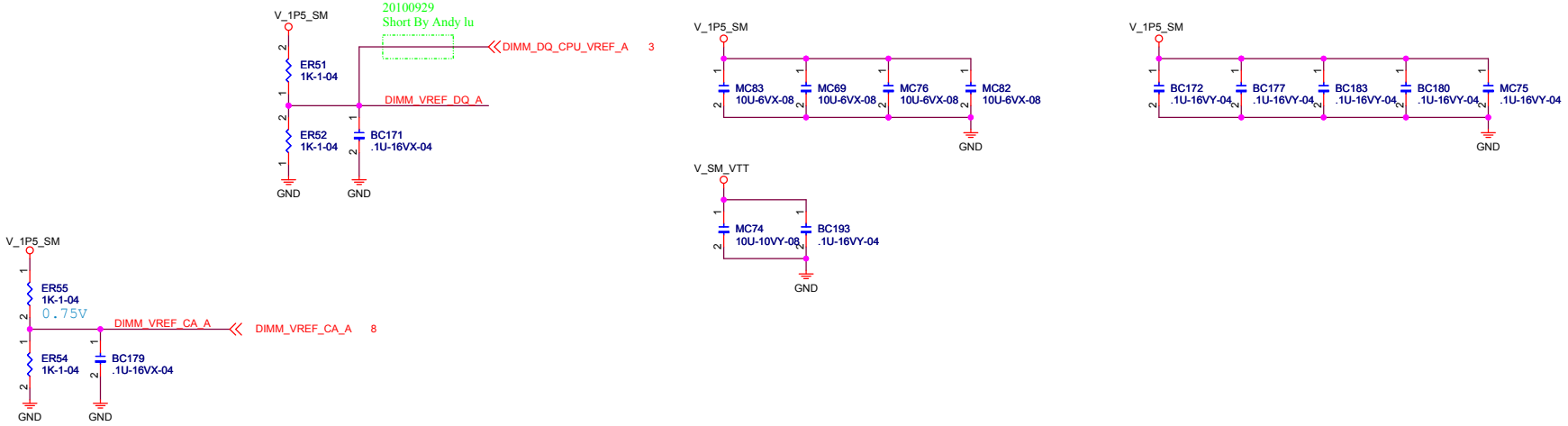


CHANNEL A DIMMs

CH.A	SA1	SA0
DIMM1	L	H



Del DIMM1 for always populate DIMM2 first Jack 05/13

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Title: DDR3 - CH_A_DIMM1

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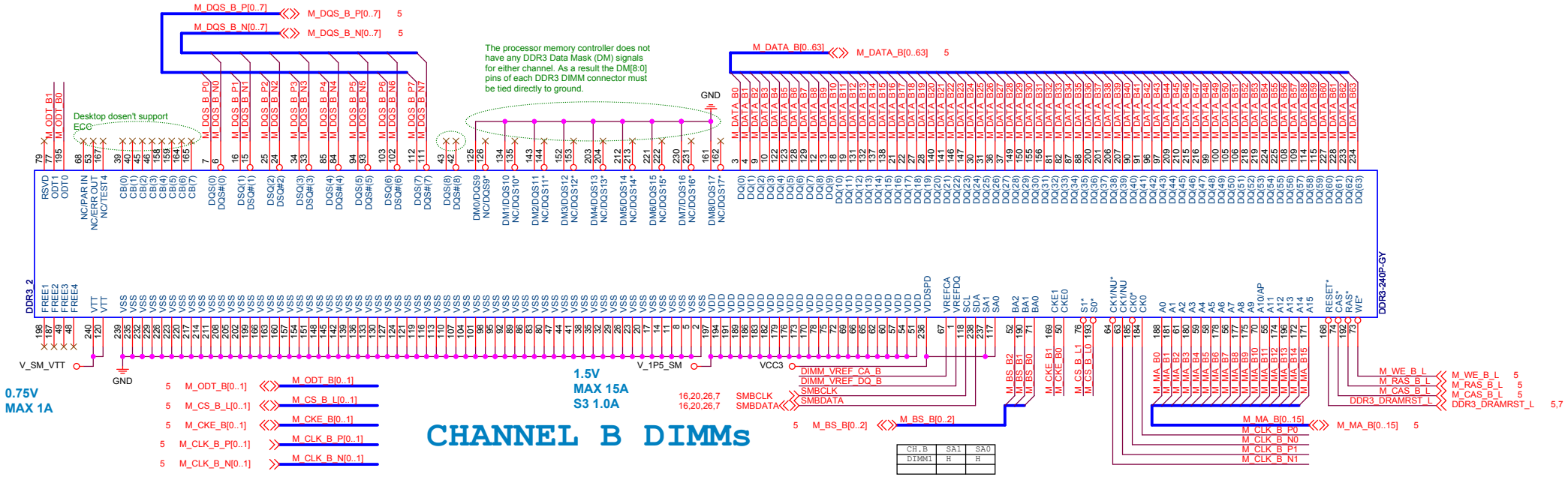
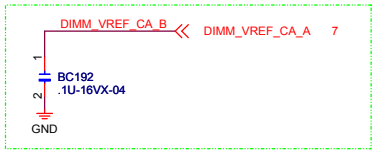
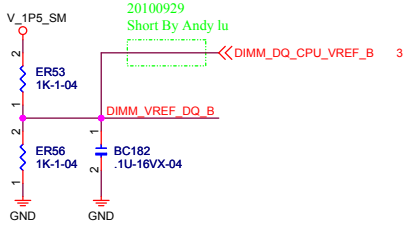
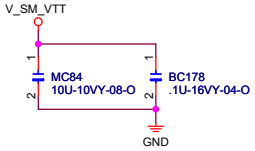


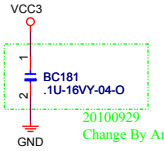
20100929
Change By Andy lu



20100929
Short By Andy lu







20100929
Change By Andy lu

Del DIMM3 for always populate DIMM4 first Jack 05/13

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Title	DDR3 - CH_B_DIMM3	
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20120417 H61H2-M17 change CPU VRM solution to Richtek.

External Connection

VCC, VCORE, V_CPUVTT, 5VSB, VCC3 → VCC, VCORE, V_CPUVTT, 5VSB, VCC3

12V_4P, VIN → VIN, 12V_4P

4 VR_EN → VR_EN
4 VR_SVID_ALERT_L → ALERT
4 VR_SVID_DATAOUT → VDIO
4 VR_SVID_CK → VCLK
4 VR_HOT_L → AU1_VRHOT
10 AU1_PWM[1..3] → AU1_PWM[1..3]

10 AU1_ISEN1P → AU1_ISEN1P
10 AU1_ISEN1N → AU1_ISEN1N

10 AU1_ISEN2P → AU1_ISEN2P
10 AU1_ISEN2N → AU1_ISEN2N

10 AU1_ISEN3P → AU1_ISEN3P
10 AU1_ISEN3N → AU1_ISEN3N

4 VCC_SEN → VCC_SEN
4 VSS_SEN → VSS_SEN

16 VR_READY → VR_READY

10 AU1_PWMA → AU1_PWMA

10 AU1_ISENAP → AU1_ISENAP
10 AU1_ISENAN → AU1_ISENAN

4 VCCAXG_SEN → VCCAXG_SEN
4 VSSAXG_SEN → VSSAXG_SEN

23,4 H_SKTOCC_L → H_SKTOCC_N

Sa

RT8859M (RT8859MZQWS)

GND

PWM

VRHOT 46 ← AU1_VRHOT
VBOOT 22 ← AU1_VBOOT
VBOOTA 23 ← AU1_VBOOTA
TMPMAX 24 ← AU1_TMPMAX
ICCMAX 25 ← AU1_ICCMAX
ICCMAXA 26 ← AU1_ICCMAXA
QRSET 55 ← AU1_QRSET
QRSETA 36 ← AU1_QRSETA
IMONA 28 → AU1_IMONA
IMONFBA 27 ← AU1_IMONFBA
RSET 9 → AU1_RSET
COMP 10 → AU1_COMP
FB 11 ← AU1_FB
DVD 48 ← AU1_DVD

TSEN 45 ← AU1_TSEN
TSENA 44 ← AU1_TSENA
IMON 15 → AU1_IMON
IMONFB 16 ← AU1_IMONFB
IBIAS 21 ← AU1_IBIAS
OFS 14 ← AU1_OFS
NC4/DVIDA 56 ← AU1_DVIDA
VCLK 18 ← VCLK
VDIO 19 ↔ VDIO
ALERT# 20 → ALERT#
ADD 17
RGNDA 31
RGND 12

PWM1 53 → AU1_PWM1
PWM2 54 → AU1_PWM2
PWM3 52 → AU1_PWM3
ISEN1P 4 ← AU1_ISEN1P
ISEN1N 3 ← AU1_ISEN1N
NC1/DVID 13 ← AU1_DVID
ISEN2P 1 ← AU1_ISEN2P
ISEN2N 2 ← AU1_ISEN2N
NC2/SR_ADDF 29 ← AU1_SR_ADDF
ISEN3P 5 ← AU1_ISEN3P
ISEN3N 6 ← AU1_ISEN3N
NC3/OFSA 30 ← AU1_OFSA
ISEN4P 8
ISEN4N 7
PWM4 51
DEL Phase4

DVDA 33 ← AU1_DVDA
COMPA 32 ← AU1_COMPA
FBA 39 ← AU1_FBA
VRA_RDY 40 ← VRA_RDY
VR_RDY 41 → VR_READY
VCC 42
OCSETA 43 ← AU1_OCSETA
OCSET 49 ← AU1_OCSET
TONSETA 50 ← AU1_TONSETA
TONSET 34 ← AU1_TONSET
ISENAN 35 ← AU1_ISENAN
ISENAP 37 ← AU1_ISENAP
PWMA 38 ← AU1_PWMA
EN 57 ← VR_EN
PAD 47

Sb

AU1_DVIDA — R281 0-04 — MC1081 1U-16VX-06-O
AU1_DVID — R282 0-04 — MC1091 1U-16VX-06-O
AU1_OFSA — R283 100K-1-04-O, R284 1K-04 — BC2801 .1U-16VX-04-O
AU1_SR_ADDF — R285 100K-1-04-O, R286 1K-04 — BC2811 .1U-16VX-04-O

Sc

AU1_OFS — R287 1.58K-1-04, ER94 499-1-04 — BC2331 .1U-16VX-04

Sd

ATX12V — ATX-PW-4P2R — 12V_4P — BC26 .01U-25VX-04

12V_4P — R256 2.2-04 — BC279 1U-16VX-06

12V_4P — DEL L1 — 08-413-604322 Idc=22A DCR=1.9m ohm — EC11 270U-16D-OS — MC10 10U-16V-08 — MC13 10U-16V-08 — VIN — MC49 10U-16V-08

reserve as Vendor 10/11

reserve as Vendor 10/11

	RT8859A	RT8859M
Sa	RT8859A	RT8859M
Sb	X	V
Sc	402-1-04 change 1K for OV	499-1-04
Sd	RT9619	RT9612

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Title: DC/DC VCORE/VAXG RT8859M

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External Connection

VCC — VCC
VCORE — VCORE
12V_4P — 12V_4P
VCC3 — VCC3
VIN — VIN

9 AU1_PWM[1..3] — AU1_PWM[1..3]
9 AU1_ISEN1P — AU1_ISEN1P
9 AU1_ISEN1N — AU1_ISEN1N
9 AU1_ISEN2P — AU1_ISEN2P
9 AU1_ISEN2N — AU1_ISEN2N
9 AU1_ISEN3P — AU1_ISEN3P
9 AU1_ISEN3N — AU1_ISEN3N
9 AU1_PWMA — AU1_PWMA
9 AU1_ISENAP — AU1_ISENAP
9 AU1_ISENAN — AU1_ISENAN

20120417 H61H2-M17 change CPU VRM solution to Richtek.

R48 2.2-06, BC52 .1U-16VY-04
PWM3
RT9612: BOOT, UGATE, PWM, PHASE, NC, PGND, VCC, LGATE
AU1_PWM1, HG1, PHASE1, LG1
R41 2.2-06, 12V_4P, BC47 .1U-16VY-04
RT9612BZS
02-415-612791 銅製程cost down
Sd

R61 2.2-06, BC53 .1U-16VY-04
PWM4
RT9612
AU1_PWM2, HG2, PHASE2, LG2
R94 2.2-06, 12V_4P, BC45 .1U-16VY-04
RT9612BZS

R35 2.2-06, BC54 .1U-16VY-04
PWM5
RT9612
AU1_PWM3, HG3, PHASE3, LG3
R36 2.2-06, 12V_4P, BC46 .1U-16VY-04
RT9612BZS

R89 2.2-06, BC40 .1U-16VY-04
PWM6
RT9612
AU1_PWMA, UG_GT, PHASE_GT, LG_GT
R34 2.2-06, 12V_4P, BC51 .1U-16VY-04
RT9612BZS

VIN
R57 0-06, HG1 — HG1_R
MF6 MN252-9MS
PHASE1
MF8 MN252-6MS
LG1
L6 PIND-0.3UD
R66 1-06, BC60 .01U-25VX-04
SP7 SHORT PAD, SP8 SHORT PAD
ER97 6.8K-1-04, MC70 .1U-16VY-04
AU1_ISEN1P, AU1_ISEN1N
VCORE
EC16 820U-2.5D6-OS, EC17 820U-2.5D6-OS, EC18 820U-2.5D6-OS, EC19 820U-2.5D6-OS

VIN
R32 0-06, HG2 — HG2_R
MF2 MN252-9MS
PHASE2
MF4 MN252-6MS
LG2
L5 PIND-0.3UD
R51 1-06, BC48 .01U-25VX-04
SP4 SHORT PAD, SP6 SHORT PAD
ER95 6.8K-1-04, MC59 .1U-16VY-04
AU1_ISEN2P, AU1_ISEN2N

VIN
R31 0-06, HG3 — HG3_R
MF1 MN252-9MS
PHASE3
MF5 MN252-6MS
LG3
L4 PIND-0.3UD
R52 1-06, BC49 .01U-25VX-04
SP5 SHORT PAD, SP10 SHORT PAD
ER96 6.8K-1-04, MC63 .1U-16VY-04
AU1_ISEN3P, AU1_ISEN3N

VIN
R72 0-06, UG_GT — UG_GT_R
MF9 MN252-9MS
EC3 270U-16D-OS, MC3 10U-16V-08
PHASE_GT
MF10 MN252-6MS
LG_GT
L7 PIND-0.6UD
R76 1-06, BC81 .01U-25VX-04
SP11 SHORT PAD, SP3 SHORT PAD
ER98 6.8K-1-04, MC90 .1U-16VY-04
AU1_ISENAP, AU1_ISENAN
VAXG
EC24 820U-2.5D6-OS, EC25 820U-2.5D6-OS

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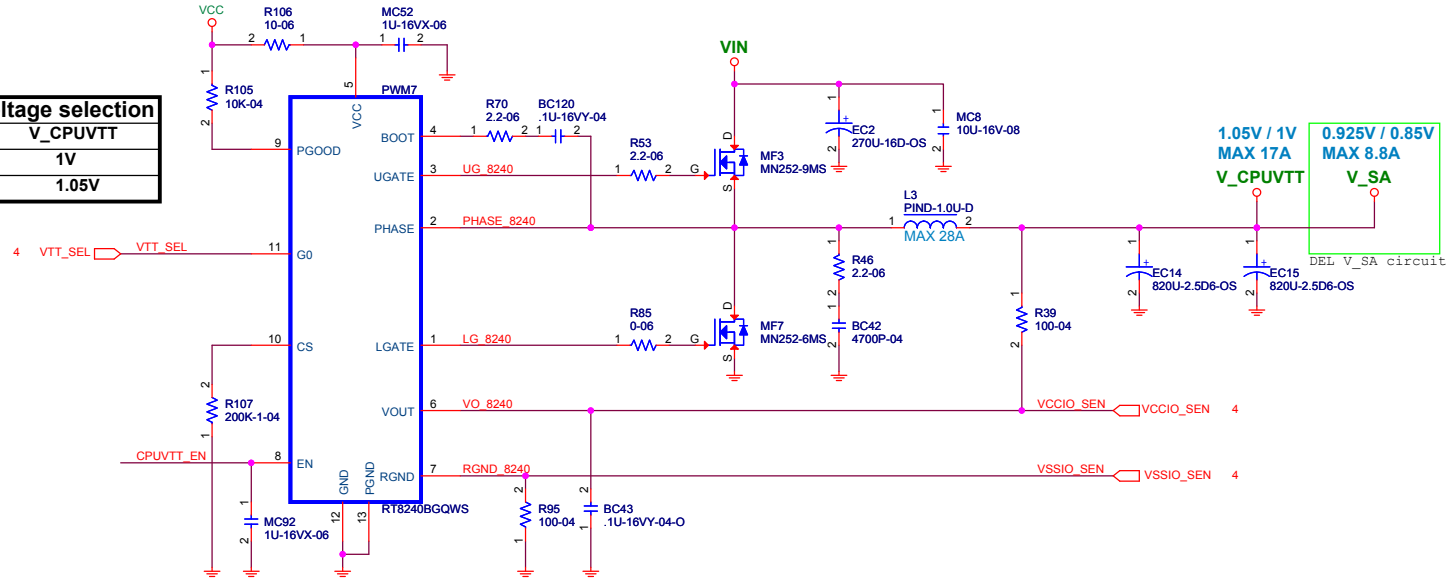
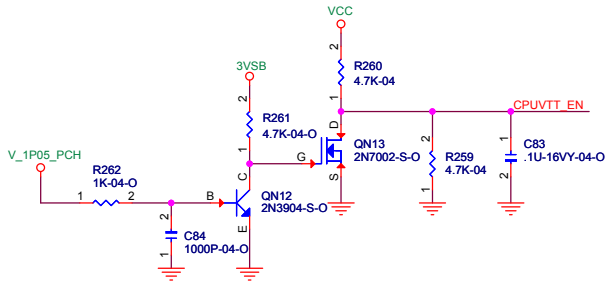
20120417 H61H2-M17 change CPU VRM solution to Richtek.

External Connection

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V





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Title: DC/DC V_CPUVTT/V_SA RT8240B

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20100924
Change By Andy lu
From 3VSB to 5VSB

20100924
Add By Andy lu
For Fintek SIO

reserve for LG_DIMM refer to VCC Jack 06/22

DIMM_5VDUAL

1207'10 Jayson :
Add By Jayson
for Down Voltage of DIMM

Idc=22A
DCR=1.9m ohm

20100929
Change By Andy lu

1.5V@TDC 20A, MAX 25A

DDR3

V_1P5_SM

0211'11 Jayson:
Change to 14.3K.

0211'11 Jayson:
Change to EC_Cap 1000U

locset=(40uA*Rocset-0.4V)/Rlowmos_dson=38.2A
Vgs=10V Rdson=4.5 mOHM

Rvdimm

Refer to page28

201001203
Change By Andy lu
EC33 Del

For Non-AMT

6.2A V_1P05_PCH
2.5A V_1P05_ME

20100929
Change By Andy lu

GP_V1.05:default OD ==>1.05V
Low==>1.1V

0.75V@1A

V_SM_VTT

20120417
H61H2-M17
change.

3VSB_IO

Vo=Vin*Rb/(Rt+Rb)-0.7
3VSB IO Max=25mA

1210'10 Jayson :
3VSB_IO 先線路預留不上
,SIO有內轉power.

VCCNS_REF

201001020
Change By Andy lu

1.6A
V_1P8_SFR

3VSB

0211'11 Jayson :
From 105 change to 102 ohm
let 3VSB up to 3.45V

Vo=1.25(1+Rb/Rt)

USB3.0 W/S3 ADJ1085-S 02-349-085810 (TO-252)
USB3.0 W/O S3 ADJ1086-S 02-347-086760 (SOT-223)

Elitegroup Computer Systems

Title: DC/DC VDIMM/DDR_VTT/5VDUAL

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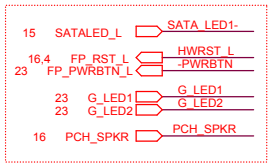
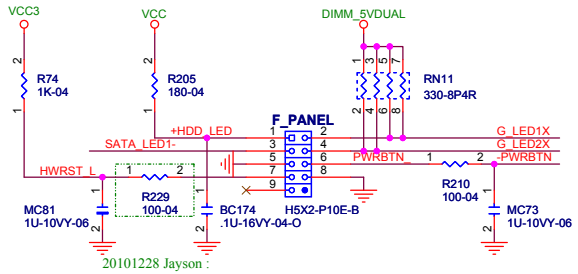
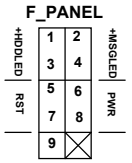
External Connection

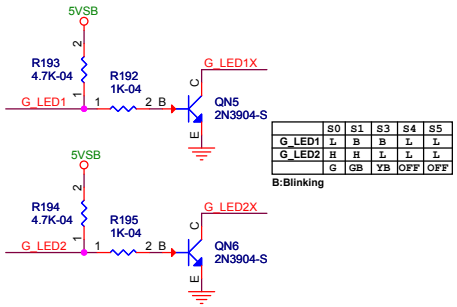


FRONT PANEL



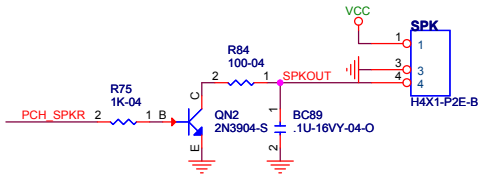
20101228 Jayson :
change to 100 ohm



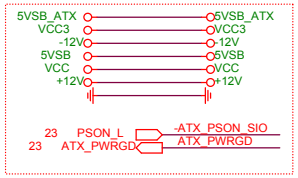


	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
	G	GB	YB	OFF	OFF

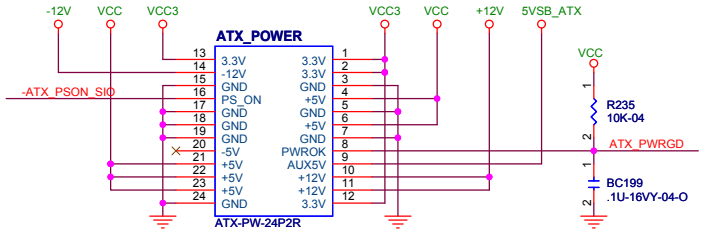
B:Blinking



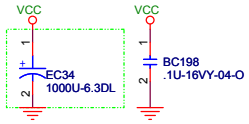
External Connection



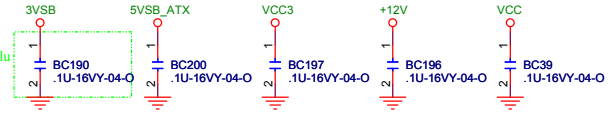
POWER CONNECTOR



20101029
Add By Andy lu

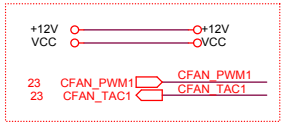


20100929
Change By Andy lu

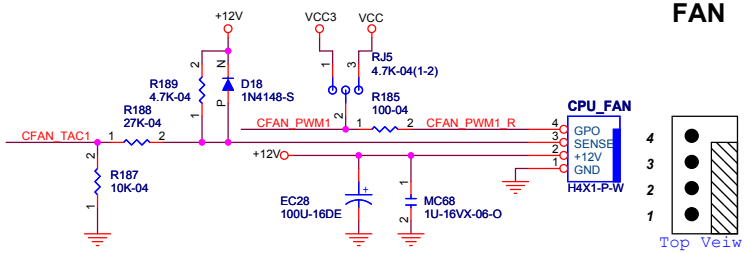


For EMI.

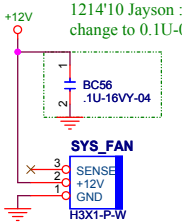
External Connection

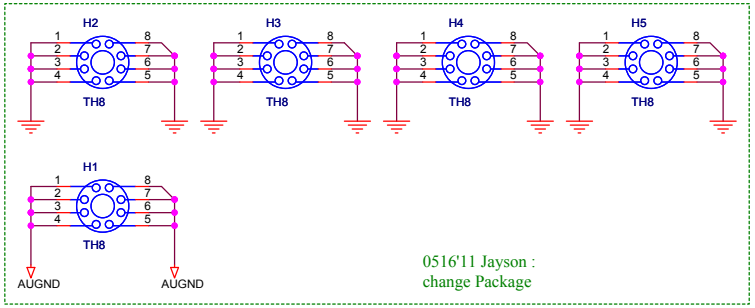


FAN

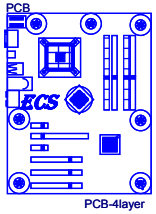


1214'10 Jayson :
change to 0.1U-04

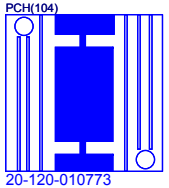




0516'11 Jayson :
change Package



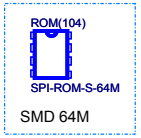
PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM



20-120-010773

5 series PN:20-120-010851

0214'11 Jayson :
PCH Heat Sink change to smaller.



20120417 H61H2-M17 change for WIN8.

Elitegroup Computer Systems

Title	Front Panel,FAN,PowerConn,GND,104	
Size: Custom	Document Number: H61H2-M17	Rev: 1.0
Date: Wednesday, May 02, 2012	Sheet 13 of 29	

For H61:USB Port 6/7/12/13 is disabled....From 440377 file

PCHA

DEVSEL_L, PCI_33M_FB, PCILPCAID_RST_L, IRDY_L, PCH_PME_L, SERR_L, STOP_L, PLOCK_L, TRDY_L, PERR_L, FRAME_L

15 PCI_33M_FB — STP40 — STP39

20100910
Add By Andy lu
For Test Point

GNT0_L, GNT1_L, GNT2_L, GNT3_L

TP9 TP11 TP10

07/21

REQ0_L, REQ1_L, REQ2_L, REQ3_L

20100910
Del By Andy lu
For PCI Slots

PCHINTA_L, PCHINTB_L, PCHINTC_L, PCHINTD_L, PCHINTE_L, PCHINTF_L, PCHINTG_L, PCHINTH_L

PAR, DEVSEL#, CLKIN_PCILOOPBACK, PCIRST#, IRDY#, PME#, SERR#, STOP#, PLOCK#, TRDY#, PERR#, FRAME#

GNT0#, GNT1#_GPIO51, GNT2#_GPIO53, GNT3#_GPIO55

REQ0#, REQ1#_GPIO50, REQ2#_GPIO52, REQ3#_GPIO54

PIRQA#, PIRQB#, PIRQC#, PIRQD#, PIRQE#_GPIO2, PIRQF#_GPIO3, PIRQG#_GPIO4, PIRQH#_GPIO5

AD0–AD31, C_BE0#, C_BE1#, C_BE2#, C_BE3#

1 OF 12

U1CPT

01-201-082013

PCHB

PCIEx1_A: PEX1A_RX_N1, PEX1A_RX_P1, PEX1A_TX_N1, PEX1A_TX_P1

20100910
Del By Andy lu
For PCI Bridge

PCI bridge

20100921
Del By Andy lu
For USB3.0

USB3.0

20100909
Add By Andy lu

PCIEx1_B: PEX1B_RX_N4, PEX1B_RX_P4, PEX1B_TX_N4, PEX1B_TX_P4

LAN: LAN_RX_N6, LAN_RX_P6, LAN_TX_N6, LAN_TX_P6

LAN_TX_N6 BC140 1 2 .1U-16VX-04
LAN_TX_P6 BC139 1 2 .1U-16VX-04

For H61:PCIE 7/8 is disable....From intel Jasmine

DMI_TX_N0–N3, DMI_TX_P0–P3, DMI_RX_N0–N3, DMI_RX_P0–P3

V_1P05_PCH — R191 1 2 49.9-1-04 — DMI_COMP

CKG_DMI_N, CKG_DMI_P

DMI0RXN, DMI0RXP, DMI0TXN, DMI0TXP, DMI1RXN, DMI1RXP, DMI1TXN, DMI1TXP, DMI2RXN, DMI2RXP, DMI2TXN, DMI2TXP, DMI3RXN, DMI3RXP, DMI3TXN, DMI3TXP, DMI_IRCOMP, DMI_ZCOMP, CLKIN_DMI_N, CLKIN_DMI_P, PERN1, PERP1, PETN1, PETP1, PERN2, PERP2, PETN2, PETP2, PERN3, PERP3, PETN3, PETP3, PERN4, PERP4, PETN4, PETP4, PERN5, PERP5, PETN5, PETP5, PERN6, PERP6, PETN6, PETP6, PERN7, PERP7, PETN7, PETP7, PERN8, PERP8, PETN8, PETP8

2 OF 12

U1CPT

USBP0N–USBP13P

USB_N0–USB_N11, USB_P0–USB_P11

F_USB2

F_USB1

USBx4

20120416 H61H2-M17 add.

USB_N8–USB_N11, USB_P8–USB_P11

USBLAN

OC0#_GPIO59, OC1#_GPIO40, OC2#_GPIO41, OC3#_GPIO42, OC4#_GPIO43, OC5#_GPIO9, OC6#_GPIO10, OC7#_GPIO14

USB_OC_L0–L7

R204 3VSB 10K-04

07/21

USBRBIAS# / USBRBIAS — ER49 22.6-1-04 — GND

CLKIN_DOT_96N, CLKIN_DOT_96P — CKG_DOT96_N, CKG_DOT96_P

DMI2RBIAS — ER50 750-1-04 — GND

VCC3

RN5: SERR_L, REQ1_L, REQ2_L, PERR_L

RN4: IRDY_L, STOP_L, FRAME_L, REQ3_L

RN6: PLOCK_L, REQ0_L, TRDY_L, DEVSEL_L

RN7: PCHINTH_L, PCHINTF_L, PCHINTE_L, PCHINTG_L

RN8: PCHINTA_L, PCHINTC_L, PCHINTD_L, PCHINTB_L

8.2K-8P4R-04

20120417 H61H2-M17 change.

R161 1K-04-O — GNT0_L — GND

GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ESI Strap (Server Only),
DON'T Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode,
When Sampled Low.

GNT[0..3]# / GPIO19
have been internal pull high to VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
* SPI	1	1

20100929
Change By Andy lu

Stuff for Integrated Clock Mode

Stuff for Integrated Clock Mode

RN13: CKG_DMI_N, CKG_DMI_P, CKG_DOT96_N, CKG_DOT96_P — 10K-8P4R-04 — GND

Elitegroup Computer Systems

Title: PCH - DMI / PCI / PE / USB

Size: Custom | Document Number: H61H2-M17 | Rev: 1.0

Date: Wednesday, May 02, 2012 | Sheet 14 of 29

For H61:SATA port2/3 is disable....From 440377 file

ONLY SATA PORT0 & PORT1 SUPPORT SATA3.0, ALSO SUPPORT SATA2.0, SATA1.0.

20100923 Add By Andy lu For LPC Debug

20100929 Short By Andy lu

PDG 0.7 33 Ω ± 5% for Single-End (except PCI Clocks)

Layout Note: PCI Clock Max 15000MILS

IN

PCHH

U1CPT

8 of 12

20100921 Del By Andy lu For USB3.0

20100910 Del By Andy lu For PCI Bridge

20100909 Add By Andy lu

20101207 Add By Jayson for Down Voltage

MOBILE ONLY, NOT FOR DESKTOP.

CPU

Jack 08/10

LAN

PCIEx1_B

PCIEx1_A

PCIEx16

PCHC

3 OF 12

20100916 Change By Andy lu From Ports 2,3 to Ports0,1

20120417 H61H2-M17 change.

Default GPI set to Pull Up: Reserve for BOM Detect.

GPIO36_TCM_PST_L, GPIO37_TCM: TCM Header In Eanble TCM, Disable TPM.

GPIO16, GPIO49: Reserve for TPM.

1210'10 Jayson: Del KBRST_L & A20GATE (Pull-High)

20100923 Add By Andy lu For LPC Debug

Detect USB3.0 control IC

STITCHING CAPS.

Stuff for Integrated Clock Mode

CKa

Clock Mode	CLK GEN. IDT CV184 Circuit.	CKa
Integrated Clock Mode	X	V
Buffer Through Mode	V	X

Stuff for Integrated Clock Mode

SATA

1207'10 : By Jayson added

Elitegroup Computer Systems

Title: PCH - SATA / CLK

Size: Custom | Document Number: H61H2-M17 | Rev: 1.0

Date: Wednesday, May 02, 2012 | Sheet 15 of 29

23 LPC_AD[0..3] LAD[0..3]

1207'10 :
By Jayson added

PCHD

STP48 1 LPC_DRQ1_L BA20
23 LPC_AD0 LPC_AD0 BK15
23 LPC_AD1 LPC_AD1 BJ17
23 LPC_AD2 LPC_AD2 BJ20
23 LPC_AD3 LPC_AD3 BG20
STP43 LPC_DRQ0_L BK17
23 LPC_FRAME_L LPC_FRAME_L BG17

24 HDA_BITCLK HDA_BITCLK BU22
24 HDA_RST_L HDA_SDIN0 BC22 BD22
BF22 BK22 BJ22 BT23
24 HDA_SDOUT HDA_SYNC BP23

22 SPI_MOSI SPI_MISO AU53 AT55
22 SPI_MISO SPI_CS_L0 AT57
22 SPI_CS_L0 SPI_CLK AR54
22 SPI_CLK SPI_CS_L1 AR56

PCH_RTCX1 BR39
PCH_RTCX2 BN39
RTCRST_L BT41
SRTCRST_L BN37
INTRUDER_L BM38
PWRGD BJ38
RSMRST_L BK38
INTVRMEN BN41
DPWROK BT37
DSWODVREN BR42

SMBALERT_L BN49
20,26,7,8 SMBCLK BT47
20,26,7,8 SMBDATA BR49
SMLK0ALERT_L BU49
SMLK0_LAN_CLK BT51
SMLK0_LAN_DATA BM50
SMLK1ALERT_L BR46
23 SMLK1_SIO_CLK SMLK1_SIO_CLK BJ46
23 SMLK1_SIO_DATA SMLK1_SIO_DATA BK46

LDRQ1#_GPIO23 FWH0_LAD0 FWH1_LAD1 FWH2_LAD2 FWH3_LAD3 LDRQ0# FWH4_LFRAME#
HDA_BCLK HDA_RST# HDA_SDIN0 HDA_SDIN1 HDA_SDIN2 HDA_SDIN3 HDA_SDO HDA_SYNC
SPI_MOSI SPI_MISO SPI_CS0# SPI_CLK SPI_CS1#
RTCX1 RTCX2 RTCRST# SRTCRST# INTRUDER# PWROK RSMRST# INTVRMEN DPWROK DSWVRMEN
SMBALERT#_GPIO11 SMBCLK SMBDATA SML0ALERT#_GPIO60 SML0CLK SML0DATA SML1ALERT#_PCHHOT#_GPIO74 SML1CLK_GPIO58 SML1DATA_GPIO75

BMBUSY#_GPIO0 CLKRUN#_GPIO32 HDA_DOCK_EN#_GPIO33 STP_PCI#_GPIO34 GPIO35
GPIO8 LAN_PHY_PWR_CTRL_GPIO12 HDA_DOCK_RST#_GPIO13 GPIO15 GPIO24_MEM_LED GPIO28 SLP_LAN#_GPIO29 PCIECLKRQ2#_GPIO20 PCIECLKRQ5#_GPIO44 PCIECLKRQ6#_GPIO45 PCIECLKRQ7#_GPIO46 GPIO57 SYS_PWROK RI# PLTRST# WAKE# SLP_A# SLP_S3# SLP_S4#
SLP_S5#_GPIO63 SUS_STAT#_GPIO61 SUSCLK_GPIO62 BATLOW#_GPIO72 SUSACK# SUSWARN#/SUSPWRDNACK/GPIO30 DRAMPWROK
GPIO27 GPIO31 SLP_SUS# PWRBTN#
SYS_RESET# SPKR
PROCPWRGD
TP12 JTAG_TCK JTAG_TDI JTAG_TDO JTAG_TMS

AW55 FP_AUD_DETECT → FP_AUD_DETECT 25
BC56 CLKRUN_L → TP24
BC25 HDA_DOCK_EN_L 1 → STP49
BL56 PCH_PU_GP34 1 → TP22
BJ57 TP_GPIO35 1 → STP71
BP51 IGC_EN_L
BK50 LAN_DISABLE_L 1 → STP61
BA25 LPC_PME_L ↔ LPC_PME_L 23
BM55 TLS_EN ↔ GPIO15 12
BP53 PCH_SKTOCC_L 1 → STP65
BJ55 ON_DIE_PLL_EN 1 → TP25
BH49 SLP_LAN_L 1 → STP62
AV43 PCH_GP20_PU
BL54 PCH_GP44
AV44 PCH_GP45
BP55 PCH_GP46 1 → TP17
BT53 GP57_5V_DETECT 1 → TP16
BJ53 PCH_SYSPWROK ↔ VR_READY ↔ VR_READY 9
BJ48 RI_L ↔ RI_L 21
BK48 PCH_PLTRST_L ↔ PCH_PLTRST_L 23
BC44 PCIE_WAKE_L ↔ PCIE_WAKE_L 20,26
BC41 SLPAMT_L 1 → STP51
BM53 SLP3_L ↔ SLP3_L 23,4
BN52 SLP4_L ↔ SLP4_L 23
BH50 SLP5_L 1 → STP67
BN54 LPCPD_L
BA47 SUSCLK 1 → STP57
AV46 GPIO72_BOMDET5 1 → STP66
BP45 SUSACK_L 1 → TP14
BU46 PCH_GP30
BG46 DRAM_PWROK → DRAM_PWROK 4
BJ43 PCH_GP27
BG43 PCH_GP31
BD43 SLP_SUS_L 1 → STP53
BT43 SIO_PWRBTN_L ↔ SIO_PWRBTN_L 23
BE52 SYS_RST_L ↔ FP_RST_L 13,4
BE56 PCH_SPKR ↔ PCH_SPKR 13
D53 CPU_PWROK → CPU_PWROK 4
BC49 PCH_JTAG_RST_R 1 → STP69
BA43 PCH_JTAG_TCK_R 1 → STP56
BC52 PCH_JTAG_TDI 1 → TP28
BF47 PCH_JTAG_TDO 1 → STP68
BC50 PCH_JTAG_TMS 1 → STP64

4 OF 12
U1CPT

20101207
Add By Jayson
GPIO15 for Down Voltage

20100929
Short By Andy lu

1231'10 Jayson :
Del TPM reserve LPC

PWRGD 1 C38 .1U-16VY-04-O 2 GND

VBAT_IO
DSWODVREN R203 1 2 390K-04
INTRUDER_L R201 1 2 1M-04

3VSB
SMLK0_LAN_DATA RN9 2 1 2.2K-8P4R-04
SMLK0_LAN_CLK 4 3
SMLK1_SIO_CLK 6 5
SMLK1_SIO_DATA 8 7
PCH_GP30 RN12 2 1 8.2K-8P4R-04
PCH_GP27 4 3
PCH_GP31 6 5
PCH_GP45 8 7
RI_L RN10 2 1 2.2K-8P4R-04
SMBCLK 4 3
SMBDATA 6 5
LPCPD_L 8 7

20120417
H61H2-M17
change.

SMBALERT_L R218 1 2 10K-04
SMLK0ALERT_L R209 1 2 2.2K-04
SMLK1ALERT_L R208 1 2 10K-04
LPC_PME_L R186 1 2 10K-04
PCIE_WAKE_L R223 1 2 1K-04
RSMRST_L R198 2 1 680-04
BC1701 2 .1U-16VY-04-O
GND

V_1P5_SM
DRAM_PWROK ER48 1 2 200-1-04

VCC3
SPI_CS_L1 R228 1 2 10K-04
PCH_GP20_PU R224 1 2 10K-04
R225 1 2 10K-04-O
PCH_GP45 R207 1 2 10K-04-O
GND

PCH_RTCX1
PCH_RTCX2
R206 10M-04
Y1 X-32.768K
BC175 18P-04
BC176 18P-04
GND

CASE 1 2 INTRUDER_L H2X1-B

CLR_CMOS
Width 20 mils
VBAT_IO
VBAT_IO_S
D11 BAT54C-S
R104 1K-04
3VSB_IO
CLR_CMOS H3XT-R
+VBAT
BT SK-CR2032-D
R108 20K-04
MC45 1U-10VY-06
ER37 20K-1-04
RTCRST_L
SRTCRST_L
MC47 1U-10VY-06
BC113 1U-10VY-06

Buffer Through Mode /
Integrated Clock Mode
have been changed to F/W Strap.
Default: Integrated Clock Mode
Doc. Cougar Point Platform Controller Hub
(PCH) Family EDS Update V0.7.1

IGC_EN_L R219 1 2 1K-04 GND

Integrated Clock:

IGC_EN_L (internal PU)	
H	Buffer Through Mode
* L	Integrated Clock Mode

3VSB
PCH_GP44 R220 1 2 10K-04
R221 1 2 10K-04-O GND

JTAG CLK FILTER:

PCH_GP44	
* H	Enable
L	Bypass

In Sugar Bay Q series Platform,
Enable TLS for vPro.

TLS_EN

TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
* L	Disable TLS

PCH_GP46

DFX TEST MODE Rings Oscillator:

PCH_GP46 (internal PU)	
* H	Enable
L	Bypass

PCH_SPKR

No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
* L	Disable

ON_DIE_PLL_EN

On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
* H	Enable
L	Disable

VBAT_IO
INTVRMEN R202 1 2 390K-04

Integrated 1.05V SUS VRM:

INTVRMEN	
* H	Enable
L	Disable

HDA_SYNC

On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
* L	1.8V

When Deep Sleep not implemented:

1.PCH_GP30, PCH_GP27 need to be Pull Up.
2.VCCDSW3_3 should to be connected to +3VSB.
3.SLP_SUS_L, SUSACK_L left unconnected.
4.SUSWARN_L may be used as GPIO30.(Reference to 1.)

RSMRST_L DPWROK
For platform not supporting deep sleep connect directly to RSMRST#.

20100929
Short By Andy lu

3VSB
R90 1K-04
ME_UNLOCK 1 2 ME_UN_PU HDA_SDOUT H2X1-B

ME Enable/Disable

	ME_UNLOCK
1-2	UNLOCK
Float	LOCK

Elitegroup Computer Systems

Title: PCH - MISC, Strap Function

Size	Document Number	Rev
Custom	H61H2-M17	1.0

Date: Wednesday, May 02, 2012 Sheet 16 of 29

0504'11 Jayson :
DEL DVI

20120416
H61H2-M17
add.

STP38
STP36

0504'11 Jayson :
DEL DVI

20120416 H61H2-M17 add.

PCHF

DDPD_HDP_F

DDPB_AUXP
DDPB_AUXN
DDPC_AUXP
DDPC_AUXN
DDPD_AUXP
DDPD_AUXN

DDPB_0P
DDPB_0N
DDPB_1P
DDPB_1N
DDPB_2P
DDPB_2N
DDPB_3P
DDPB_3N
DDPC_0P
DDPC_0N
DDPC_1P
DDPC_1N
DDPC_2P
DDPC_2N
DDPC_3P
DDPC_3N
DDPD_0P
DDPD_0N
DDPD_1P
DDPD_1N
DDPD_2P
DDPD_2N
DDPD_3P
DDPD_3N

DDPD_TX2
DDPD_TX2-
DDPD_TX1
DDPD_TX1-
DDPD_TX0
DDPD_TX0-
DDPD_TXC
DDPD_TXC-

SDVO_INTP
SDVO_INTN
SDVO_STALLP
SDVO_STALLN
SDVO_TVCLKINP
SDVO_TVCLKINN

CRT_HSYNC
CRT_VSYNC
C_HSYNC R172 2 1 33-04 VGA_HSYNC
C_VSYNC R164 2 1 33-04 VGA_VSYNC

Add damping 2010/7/27

CRT_RED
CRT_GREEN
CRT_BLUE
AN6 VGA_RED R170 2 1 150-1-04
AN2 VGA_GREEN R165 2 1 150-1-04
AM1 VGA_BLUE R166 2 1 150-1-04

CRT_IRTN
AM6
GND

CRT_DDC_DATA
CRT_DDC_CLK
DAC_IREF
AW1 VGA_DDC_DATA
AW3 VGA_DDC_CLK
AT3 DACREFSET ER40 2 1 1K-1-04
GND

TP6 Y18 PCH_TP6 STP47
TP7 Y17 PCH_TP7 STP44
TP8 AB18 PCH_TP8 STP46
TP9 AB17 PCH_TP9 STP42

DDPC_CTRLCLK
DDPC_CTRLDATA
AL12 DDPC_CTRLCLK STP41
AL14 DDPC_CTRLDATA STP45

20120416 H61H2-M17 add.

DDPD_CTRLCLK
DDPD_CTRLDATA
AL9 DDPD_CTRLCLK
AL8 DDPD_CTRLDATA
DDPD_CTRLCLK 21
DDPD_CTRLDATA 21

SDVO_CTRLCLK
SDVO_CTRLDATA
AL15
AL17

0504'11 Jayson :
DEL DVI

6 of 12

U1CPT

091222 Update!
Terminating unused DC NAND interface:

If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.

Note:

VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

4 PROC_SEL PROC_SEL R215 1 2 4.7K-04 NVR_CLE

PCHE

M48 RESERVED_29
R47 DF_TVS
Y41 RESERVED_6
M50 RESERVED_4
M49 RESERVED_3
U43 RESERVED_2
J57 RESERVED_1

RESERVED_22 AB50
RESERVED_21 Y50
RESERVED_14 AB48
RESERVED_13 AB44
RESERVED_12 U49
RESERVED_11 R44
RESERVED_10 U50
RESERVED_9 U46
RESERVED_8 U44
RESERVED_7 H50
RESERVED_20 K46
RESERVED_19 L56
RESERVED_18 J55
RESERVED_17 F53
RESERVED_16 H52
RESERVED_15 E52

RESERVED_28 K50
RESERVED_27 K49
RESERVED_26 AB46
RESERVED_25 G56

RESERVED_24 Y44
RESERVED_23 L53

RESERVED_5 R50

5 OF 12

U1CPT

100120 Update!
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip:

Renamed NV_WE#_CK[0:1], NV_RE#_WRB[0:1], NV_RCOMP, NV_RB#, NV_DQ9 / NV_IO[0:15], NV_DQS[0:1], NV_CE#[0:3], and NV_ALE to Reserved(RSVD).
Renamed NV_CLE to DF_TVS.

PCHG

H31 TP21 FDI_RXN0 C42 FDI_TX_N0 FDI_TX_N0 3
J31 TP25 FDI_RXP0 B43 FDI_TX_P0 FDI_TX_P0 3
C29 TP29 FDI_RXN1 F45 FDI_TX_N1 FDI_TX_N1 3
E29 TP33 FDI_RXP1 F43 FDI_TX_P1 FDI_TX_P1 3
H41 FDI_RXN2 H41 FDI_TX_N2 FDI_TX_N2 3
J27 J41 FDI_TX_P2 FDI_TX_P2 3
L27 TP22 FDI_RXP2 C46 FDI_TX_N3 FDI_TX_N3 3
F28 TP26 FDI_RXN3 D47 FDI_TX_P3 FDI_TX_P3 3
E27 TP30 FDI_RXP3 B45 FDI_TX_N4 FDI_TX_N4 3
TP34 FDI_RXN4 A46 FDI_TX_P4 FDI_TX_P4 3
FDI_RXP4 B47 FDI_TX_N5 FDI_TX_N5 3
J25 FDI_RXN5 C49 FDI_TX_P5 FDI_TX_P5 3
L25 TP23 FDI_RXP5 J43 FDI_TX_N6 FDI_TX_N6 3
C26 TP27 FDI_RXN6 H43 FDI_TX_P6 FDI_TX_P6 3
B27 TP31 FDI_RXP6 M43 FDI_TX_N7 FDI_TX_N7 3
TP35 FDI_RXN7 P43 FDI_TX_P7 FDI_TX_P7 3
FDI_RXP7

L22 TP24 FDI_FSYNC0 B51 FDI_FSYNC0 FDI_FSYNC0 3
J22 TP28 FDI_LSYNC0 E49 FDI_LSYNC0 FDI_LSYNC0 3
B25 TP32 FDI_FSYNC1 C52 FDI_FSYNC1 FDI_FSYNC1 3
D25 TP36 FDI_LSYNC1 D51 FDI_LSYNC1 FDI_LSYNC1 3

FDI_INT H46 FDI_INT FDI_INT 3

7 OF 12

U1CPT

0712'11 Jayson :
Change to VCC

VCC3
VCC
R9 2.2K-04
Q2 2N7002-S
R12 6.8K-04
VGA_DDC_CLK
DDCCLK

0712'11 Jayson :
Change to VCC

VCC3
VCC
R8 2.2K-04
Q1 2N7002-S
R17 6.8K-04
VGA_DDC_DATA
DDCDATA

ESD

0712'11 Jayson :
Change to VCC

VCC
U2
DDCDATA
DDCCLK
VGA_HSYNC
VGA_VSYNC
ESD-6P
BC10 .1U-16VY-04

0712'11 Jayson :
Change to VCC

VCC
U1
RED
GREEN
BLUE
ESD-6P
BC18 .1U-16VY-04

VGA

VGA_RED FB2 FB80-06-B RED
VGA_GREEN FB3 FB80-06-B GREEN
VGA_BLUE FB4 FB80-06-B BLUE

ER10 150-1-04
ER11 150-1-04
ER12 150-1-04
BC22 22P-04-O
BC23 22P-04-O
BC24 22P-04-O
BC17 10P-04-O
BC16 10P-04-O
BC15 10P-04-O

CONN-15P3R-VGA

DDCDATA
VGA_HSYNC
VGA_VSYNC
DDCCLK

BC11 47P-04-O
BC19 10P-04-O
BC20 10P-04-O
BC9 47P-04-O

Close to Connector

20100929
Change By Andy lu

Close to Connector

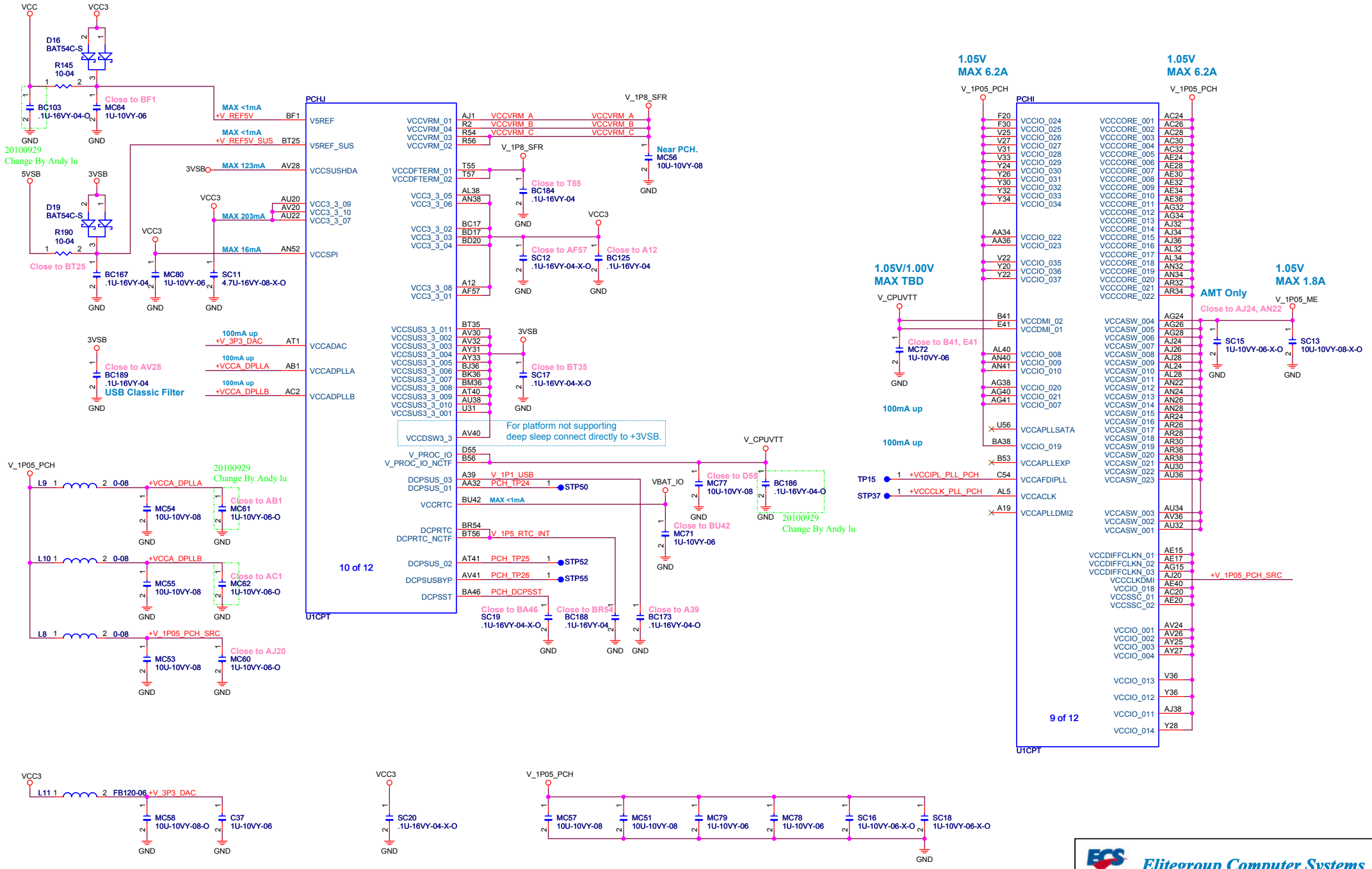
20100929
Change By Andy lu

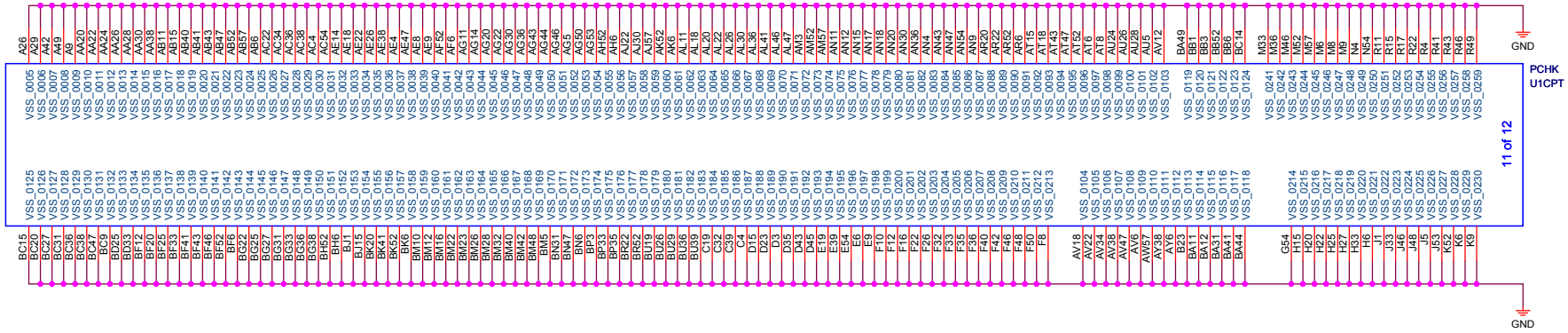
Elitegroup Computer Systems

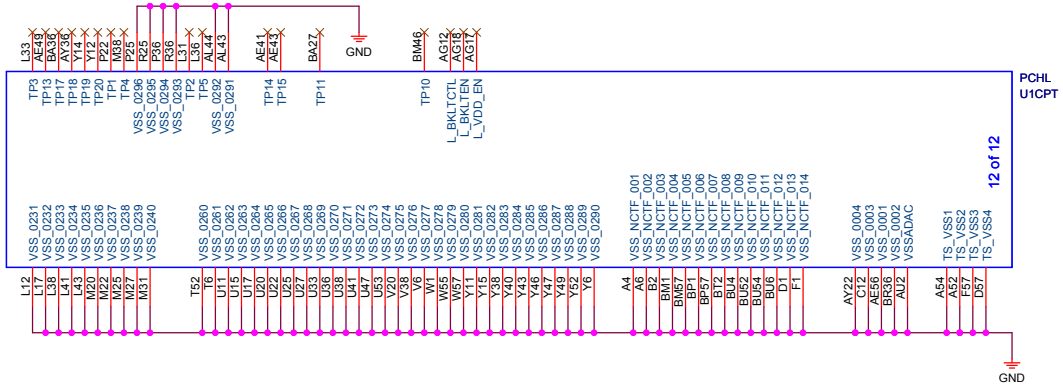
Title: PCH - DP/VGA/FDI

Size: Custom
Document Number: H61H2-M17
Rev: 1.0

Date: Wednesday, May 02, 2012
Sheet 17 of 29

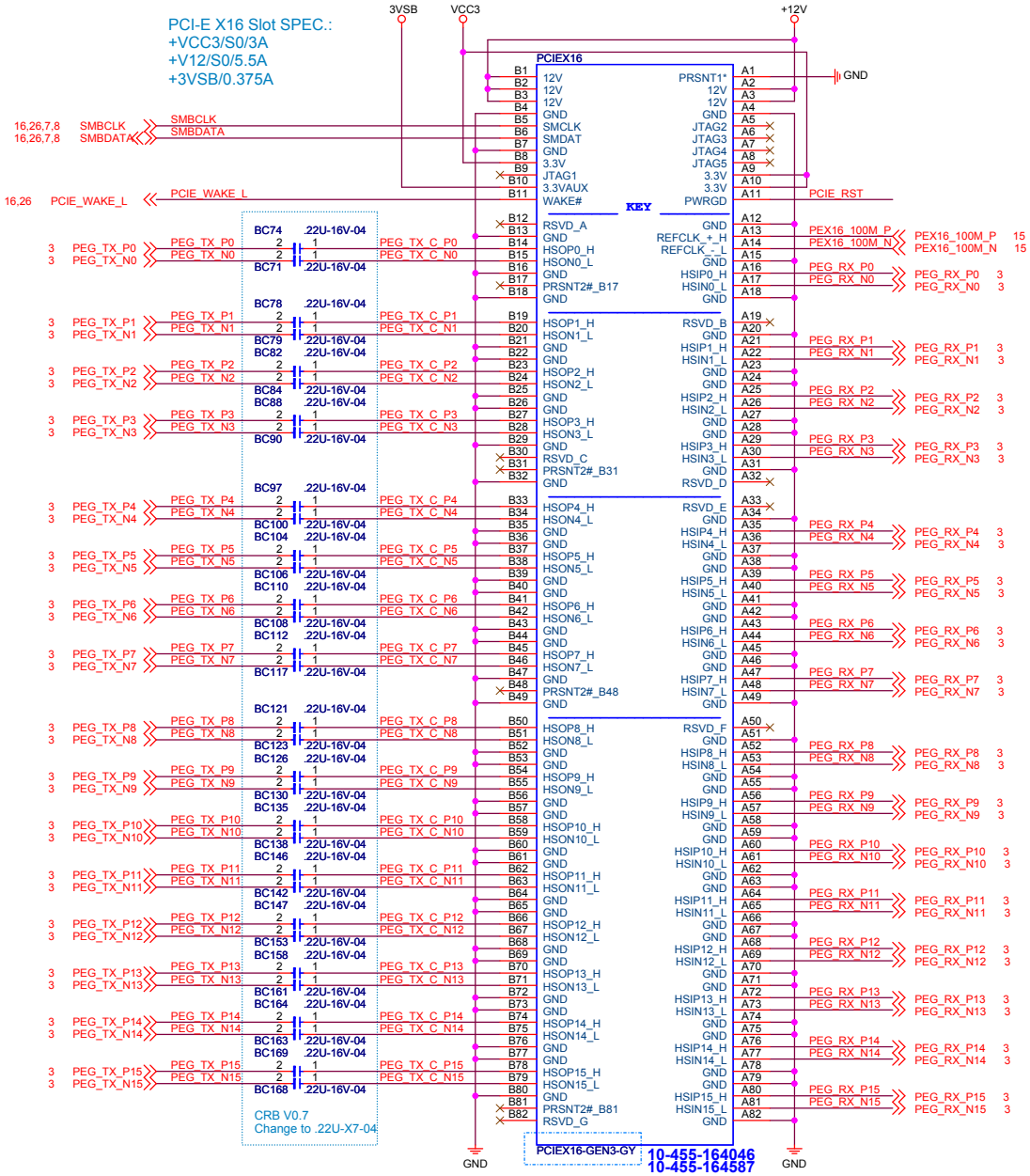

PCHJ
U1CPT
10 of 12
PCHI
9 of 12
1.05V
MAX 6.2A
1.05V/1.00V
MAX TBD
1.05V
MAX 1.8A
AMT Only
USB Classic Filter
For platform not supporting
deep sleep connect directly to +3VSB.
20100929
Change By Andy lu
Elitegroup Computer Systems
PCH - PWR
H61H2-M17
Wednesday, May 02, 2012





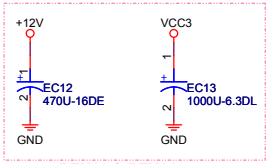
Elitegroup Computer Systems		
Title: PCH - GND		
Size: Custom	Document Number: H61H2-M17	Rev: 1.0
Date: Wednesday, May 02, 2012	Sheet 19 of 29	

PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A

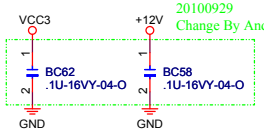


10-455-164046
10-455-164587

20120417 H61H2-M17 change.

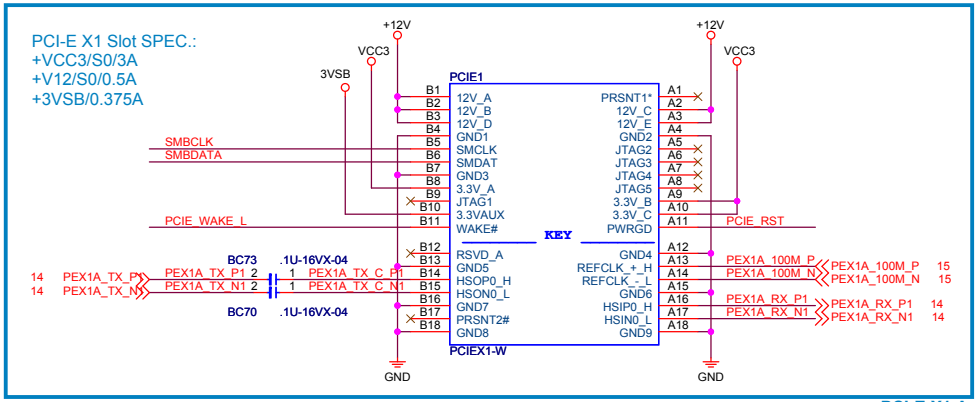


Between PEX16 & PEX1A



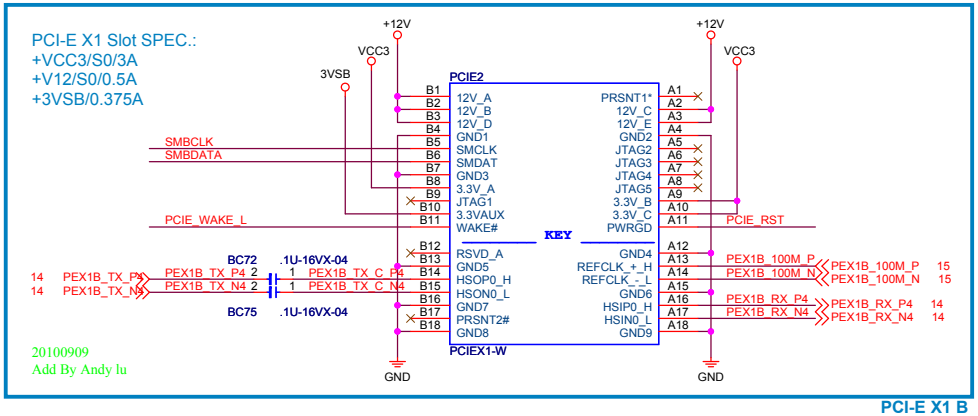
20100929
Change By Andy lu

PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A



PCI-E X1 A

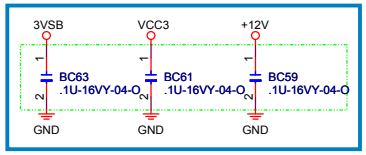
PCI-E X1 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/0.5A
+3VSB/0.375A



20100909
Add By Andy lu

PCI-E X1 B

20100929
Change By Andy lu



PCI-E X1 A Decoupling Cap.

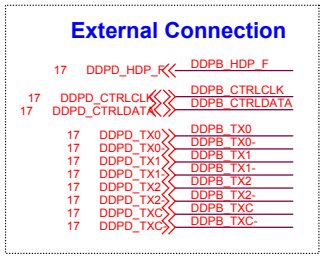
Elitegroup Computer Systems

Title: Slot - PCI-EX16/PCI-EX1

Size	Document Number	Rev
Custom	H61H2-M17	1.0

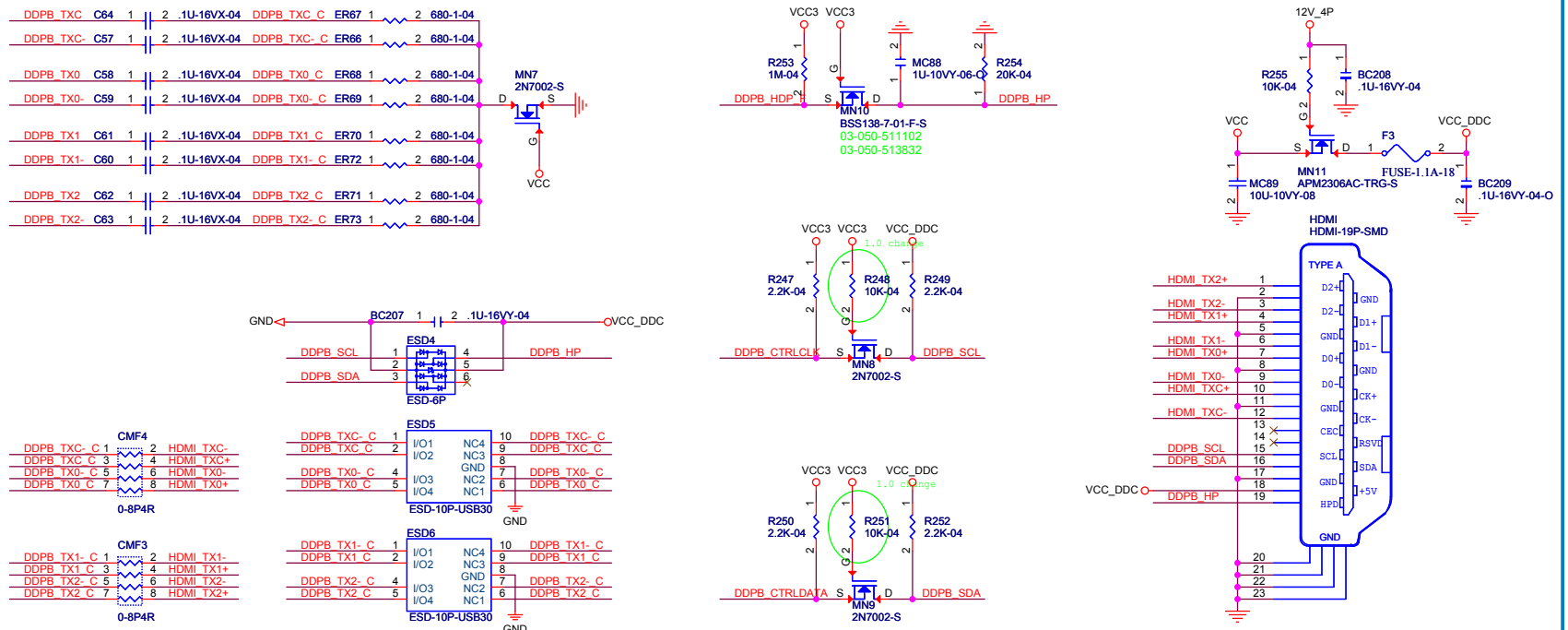
Date: Wednesday, May 02, 2012 Sheet 20 of 29

External Connection



HDMI

20120416 H61H2-M17 add HDMI circuit.



DVI

0504'11 Jayson : DEL DVI

0504'11 Jayson : DEL DVI

0504'11 Jayson : DEL Fuse & Diode

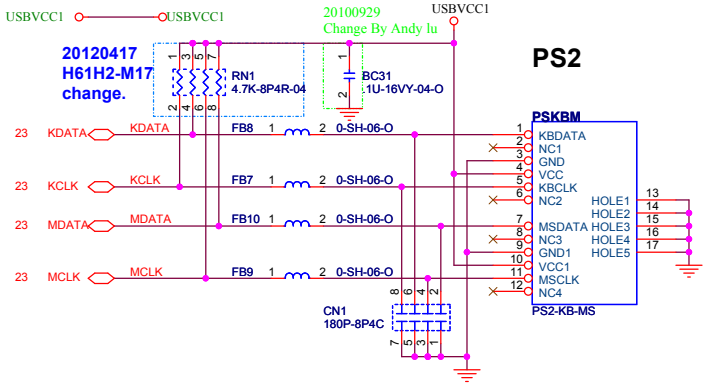
0504'11 Jayson : DEL DVI

0504'11 Jayson : DEL DVI

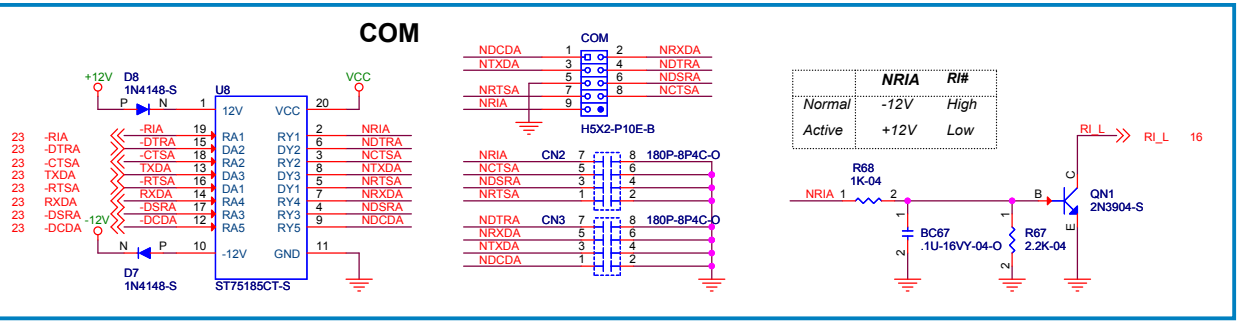
0504'11 Jayson : DEL DVI Connector

1202'10 Jayson : Del HDMI

PS2



COM



Elitegroup Computer Systems		
Title: HDMI / COM / PS2		
Size: Custom	Document Number: H61H2-M17	Rev: 1.0
Date: Wednesday, May 02, 2012	Sheet 21 of 29	

3VSB — 3VSB
USBVCC1 — USBVCC1
USBVCC1 — USBVCC1
USBPWR1 — USBPWR1
VCC — VCC
DIMM_5VDUAL — DIMM_5VDUAL

USB

USB_P0+ / USB_P0- / USB_P1+ / USB_P1- / USB_P2+ / USB_P2- / USB_P3+ / USB_P3- / USB_P4+ / USB_P4- / USB_P5+ / USB_P5- / USB_P6+ / USB_P6- / USB_P8+ / USB_P8- / USB_P9+ / USB_P9-

20120416 H61H2-M17 add.

SATA

SATA_RX_N[2..5] / SATA_RX_P[2..5] / SATA_TX_N[2..5] / SATA_TX_P[2..5]

SPI

SPI_MOSI / SPI_MISO / SPI_CS0_N / SPI_CLK

USBX4

20120416 H61H2-M17 add.

USB: VCC, DATA0-, DATA0+, GND, DATA1-, DATA1+, VCC, DATA2-, DATA2+, GND, DATA3-, DATA3+, VCC, HOLE1, HOLE2, HOLE3, HOLE4, HOLE5, HOLE6

USBR8-, USBR8+, USBR4-, USBR4+, USBR9-, USBR9+, USBR5-, USBR5+ — USBX4 — AUGND2

20100929 Change By Andy lu

BC29 .1U-16VY-04, U3, ESD-6P

USB_R4+, USB_R4-, USB_R5+, USB_R5- ↔ USBR4+, USBR4-, USBR5+, USBR5-

20120416 H61H2-M17 add.

BC206 .1U-16VY-04, U16, ESD-6P

USB_R8+, USB_R8-, USB_R9+, USB_R9- ↔ USBR8+, USBR8-, USBR9+, USBR9-

F_USB1

0504'11 Jayson : From USBPWR2 change to USBPWR1

F_USB1: USBPWR1, USBF2-, USBF2+, USBF3-, USBF3+, H5X2-P9E-W

BC165 .1U-16VY-04, U12, ESD-6P

USBF2-, USBF3+, USBF3, USBF2+

20100929 Change By Andy lu

USB_F2+, USB_F2-, USB_F3+, USB_F3- ↔ USBF2+, USBF2-, USBF3+, USBF3-

F_USB2

F_USB2: USBPWR1, USBF0-, USBF0+, USBF1-, USBF1+, H5X2-P9E-W

BC132 .1U-16VY-04, U14, ESD-6P

USBF0-, USBF1+, USBF1-, USBF0+

20100929 Change By Andy lu

USB_F0+, USB_F0-, USB_F1+, USB_F1- ↔ USBF0+, USBF0-, USBF1+, USBF1-

0504'11 Jayson : From SW_Power change to Jumper.

USBPWR_F / R	
1-2	VCC *
2-3	DIMM_5VDUAL

VCC — BC116 .1U-16VY-04-O

USB x4 & PS/2 & USBLAN F_USB1&2

VCC, DIMM_5VDUAL, VCC_DUAL_R1, USBPWR_R1, H3X1-WH

Default(1-2) — USBPWR_R1(1-2) — JP-WH-2P

VCC, DIMM_5VDUAL, VCC_DUAL_F1, USBPWR_F1, H3X1-WH

Default(1-2) — USBPWR_F1(1-2) — JP-WH-2P

0504'11 Jayson : ADD Jumper.

Power of USB

USBVCC1 — R28 0-08 — VCC_DUAL_R1 — F1 FUSE-2A-18

160 mils

20120416 H61H2-M17 change.

EC5 470U-6.3DE, BC27 .1U-16VY-04, AUGND2

USBPWR1 — R102 0-08 — VCC_DUAL_F1 — F2 FUSE-1.1A-18

80 mils

EC26 220U-16DE, BC115 .1U-16VY-04

0504'11 Jayson : EC28 From 100U change to 220U.

0504'11 Jayson : From SW_Power change to Jumper.

SATA

Layout Note: SATA2.0 4.5/7.5/15 in 90 Ω ±17.5%

SATA2 — SATA-7P2R-W

SATA_TX_P2_C C54 .01U-25VX-04 SATA_TX_P2
SATA_TX_N2_C C50 .01U-25VX-04 SATA_TX_N2
SATA_RX_N2_C C46 .01U-25VX-04 SATA_RX_N2
SATA_RX_P2_C C41 .01U-25VX-04 SATA_RX_P2

SATA1 — SATA-7P2R-W

SATA_TX_P3_C C53 .01U-25VX-04 SATA_TX_P3
SATA_TX_N3_C C49 .01U-25VX-04 SATA_TX_N3
SATA_RX_N3_C C45 .01U-25VX-04 SATA_RX_N3
SATA_RX_P3_C C40 .01U-25VX-04 SATA_RX_P3

SATA3 — SATA-7P2R-W

SATA_TX_P4_C C56 .01U-25VX-04 SATA_TX_P4
SATA_TX_N4_C C52 .01U-25VX-04 SATA_TX_N4
SATA_RX_N4_C C47 .01U-25VX-04 SATA_RX_N4
SATA_RX_P4_C C42 .01U-25VX-04 SATA_RX_P4

SATA4 — SATA-7P2R-W

SATA_TX_P5_C C55 .01U-25VX-04 SATA_TX_P5
SATA_TX_N5_C C51 .01U-25VX-04 SATA_TX_N5
SATA_RX_N5_C C44 .01U-25VX-04 SATA_RX_N5
SATA_RX_P5_C C43 .01U-25VX-04 SATA_RX_P5

SPI

3VSB — D20 BAT54C-S — 3VSB_SPI

BC194 .1U-16VY-04

SMD TYPE

SMD TYPE socket: 11-127-008120

ROM: CE#, SO, WP#, GND, VCC, HOLD#, SCK, SI — SPI-ROM-SOCKET

SPI_CS, SPI_MOS_OO, SPI_WP_L ↔ SPI_DC, SPI_CLKK, SPI_MOS_II

SPI_DEBUG — H4X2-B

FOR DEBUG USE

若上SMD SPI ROM, MP or A5後不上ROM Socket.

3VSB_SPI

SPI_DC R233 1K-04

SPI_WP_L R234 10K-04

20120417 H61H2-M17 change.

RN15: SPI_MOSI, SPI_CLK, SPI_MISO, SPI_CS0_N ↔ SPI_MOS_II, SPI_CLKK, SPI_MOS_OO, SPI_CSS — 33-8P4R-04

Elitegroup Computer Systems

Title: USB/SATA/SPI

Size: Custom | Document Number: H61H2-M17 | Rev: 1.0

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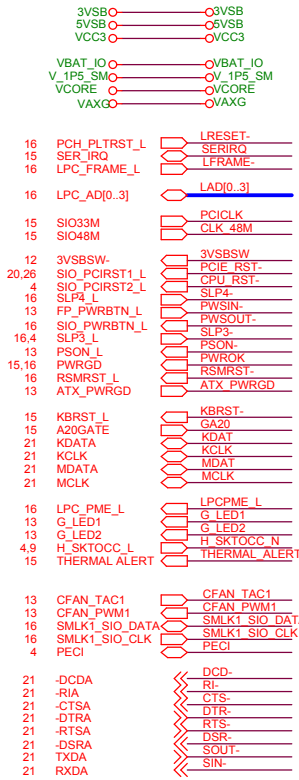
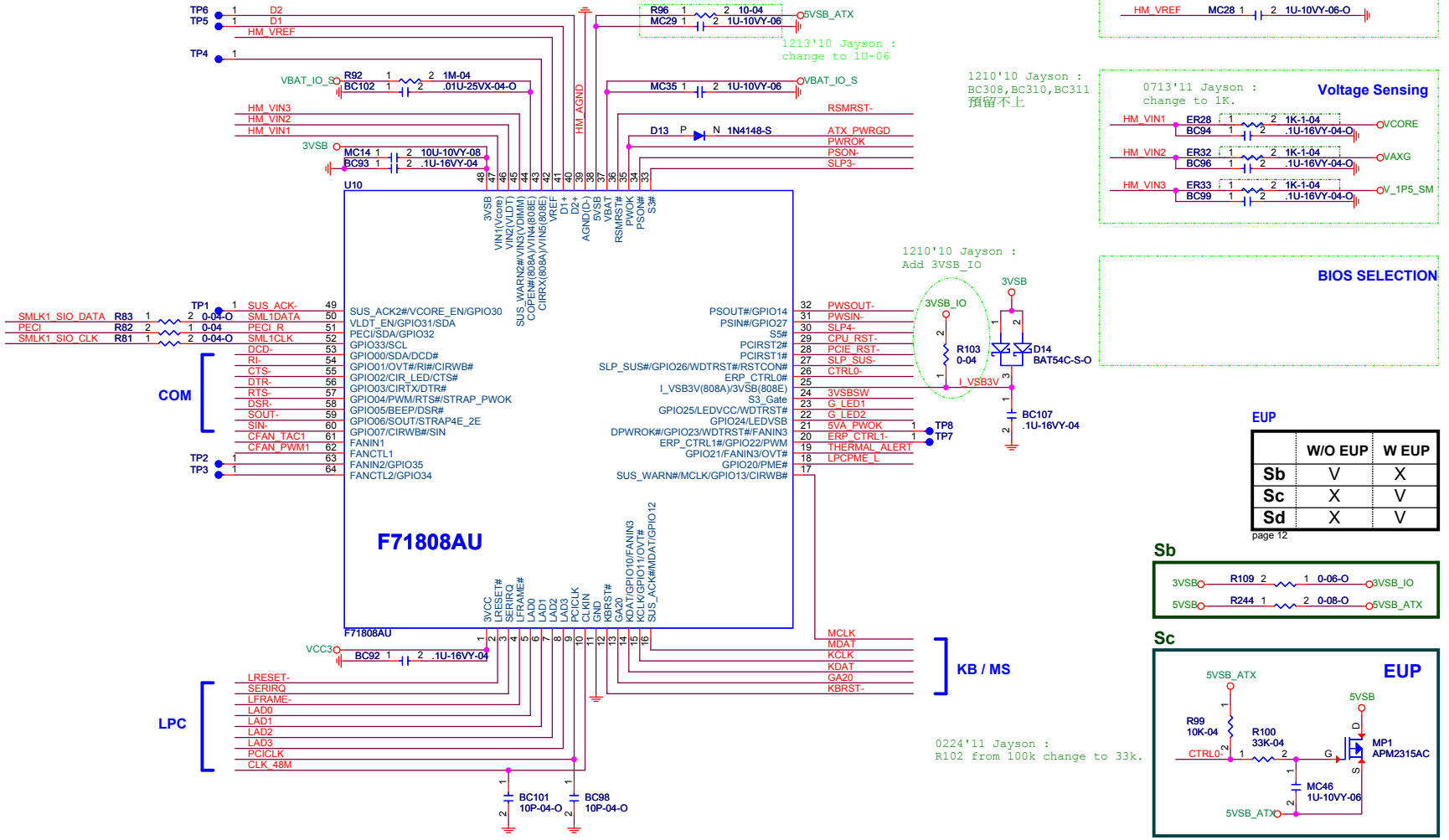
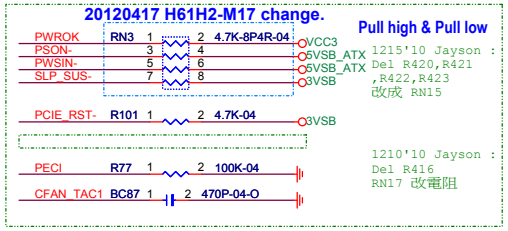
External Connection

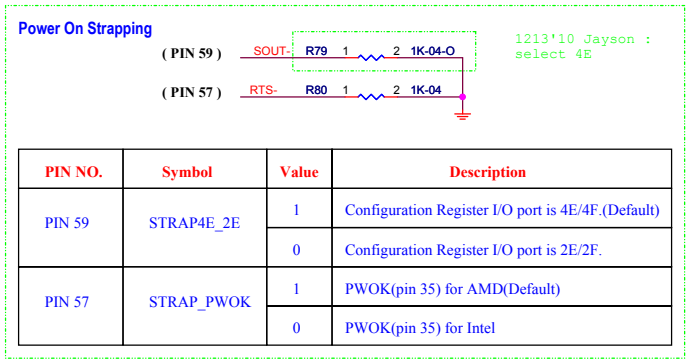




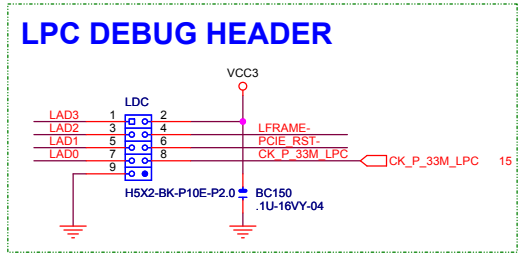
	W/O EUP	W EUP
Sb	V	X
Sc	X	V
Sd	X	V

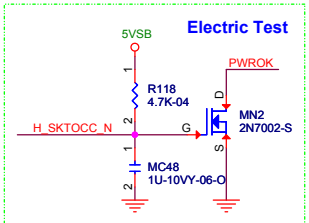
page 12





PIN NO.	Symbol	Value	Description
PIN 59	STRAP4E_2E	1	Configuration Register I/O port is 4E/4F.(Default)
		0	Configuration Register I/O port is 2E/2F.
PIN 57	STRAP_PWOK	1	PWOK(pin 35) for AMD(Default)
		0	PWOK(pin 35) for Intel





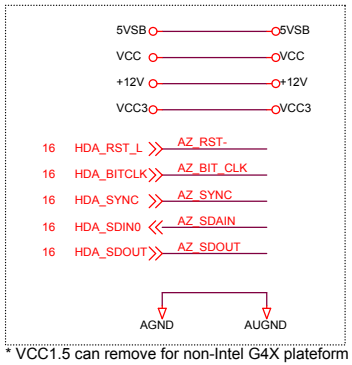
Elitegroup Computer Systems

Title: SIO-F71808A

Size: Custom | Document Number: H61H2-M17 | Rev: 1.0

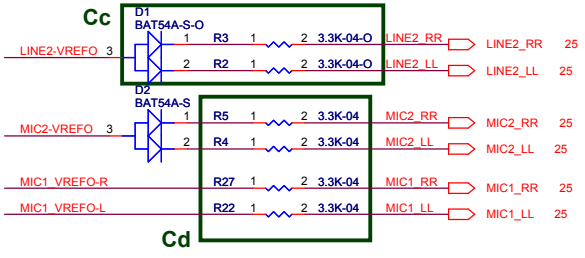
Date: Wednesday, May 02, 2012 | Sheet 23 of 29

External Connection

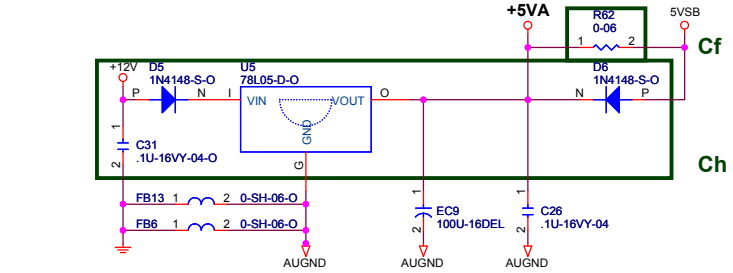


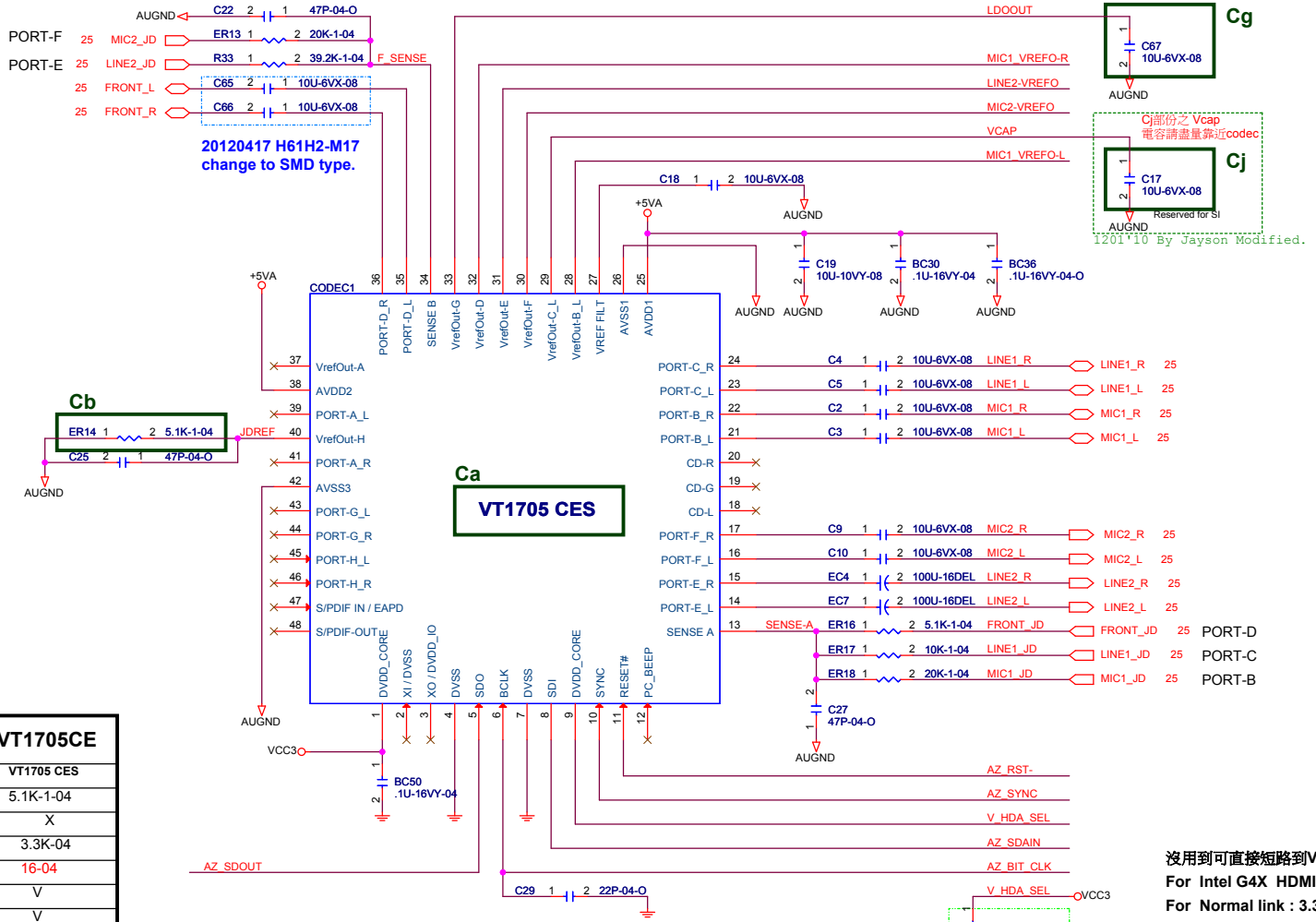
* VCC1.5 can remove for non-Intel G4X plateform

MIC Bias



20120417 H61H2-M17
change to SMD type.





20100929
Change By Andy lu

BOM Difference

Location	ALC662	VT1705CD	VT1705CE
Ca	ALC662-VC-GRS	VT1705CD	VT1705 CES
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	16-04	16-04
Cf	X	X	V
Cg	X	V	V
Ch	V	V	X
Cj	X	X	V
Ck	75-04	33-04	33-04

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

沒用到可直接短路到VCC3
For Intel G4X HDMI support : 1.5V (pin1-2)
For Normal link : 3.3V (pin2-3)

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Title: AUDIO VT1705/ALC662 (CHIP)

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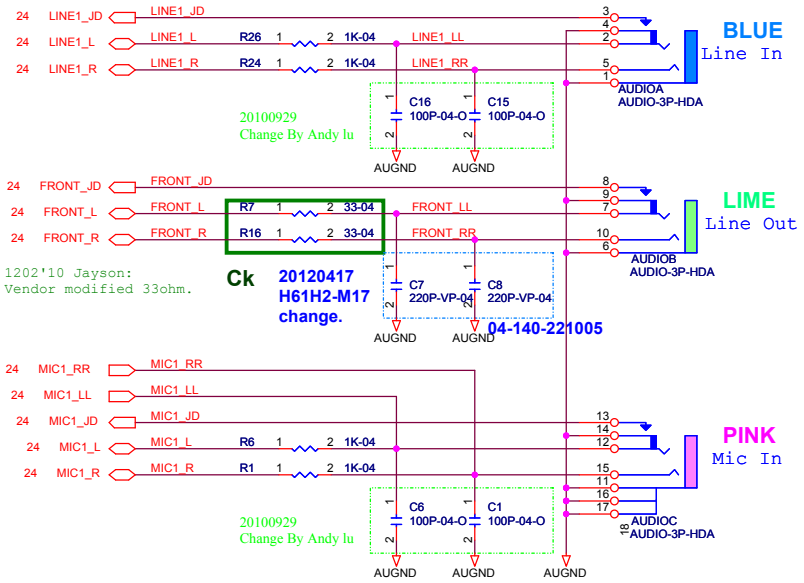
External Connection

16 FP_AUD_DETECT ⟵ HDPANEL_DETECT

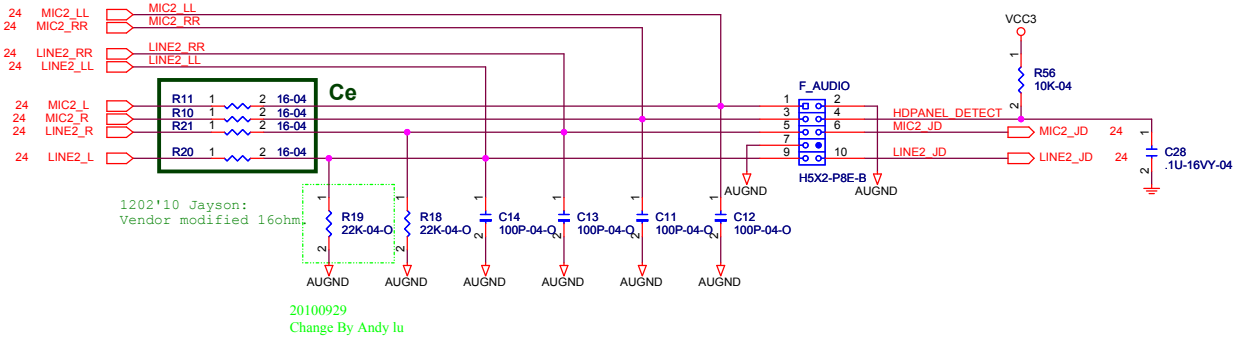
* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

REAR-AUDIO

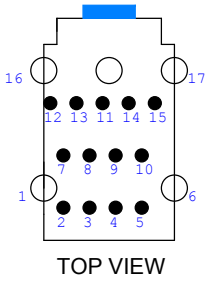
Non re-tasking for rear panel



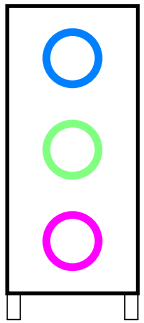
FRONT-AUDIO



1203'10 Jayson: Del SPDIF-OUT



TOP VIEW



FRONT VIEW

Elitegroup Computer Systems

Title	AUDIO VT1705/ALC662 (PANEL)	
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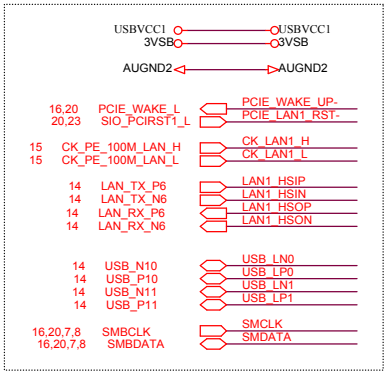
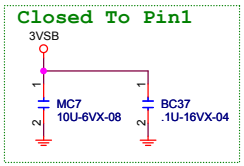
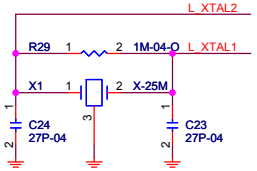
新手提醒: LAN_HSOP/N請接到SB的PCIE RX端　LAN_HSIP/N請接到SB的PCIE TX端　LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

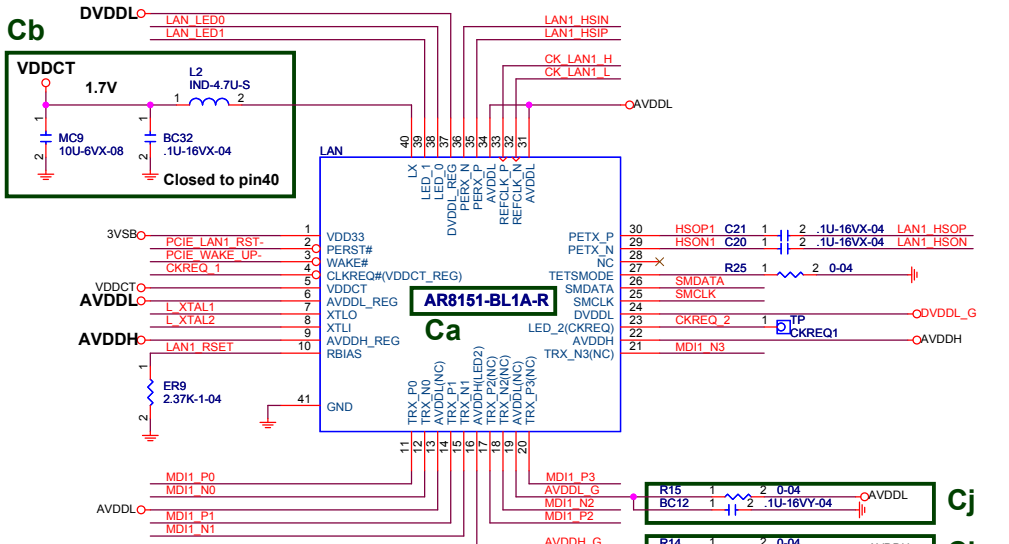
20120427 H61H2-M17 change to Giga LAN AR8151-B default.

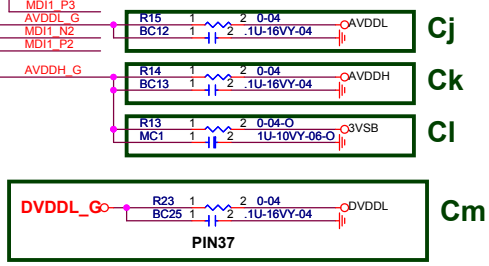
External Connection

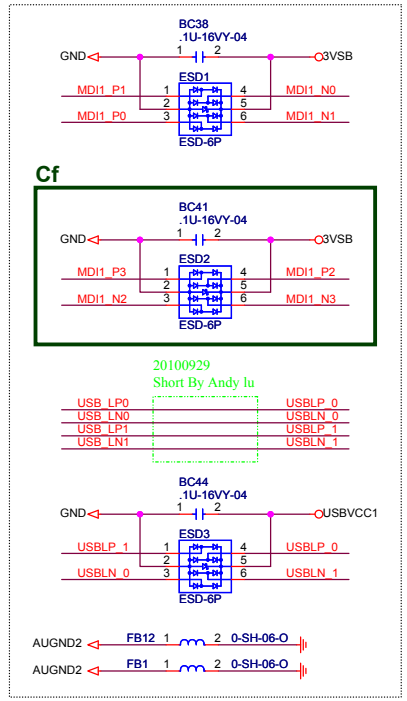




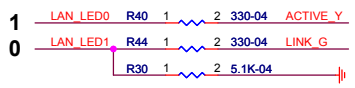








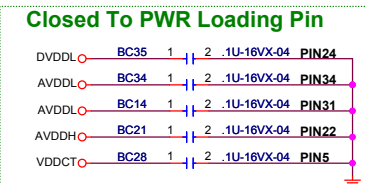
HW Strapping
LED0 : 0 -> OC disable
1 -> OC enable
LED1 : 0 -> VDDCT_REG enable
1 -> VDDCT_REG disable



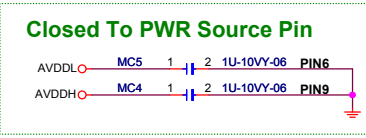
BOM Difference

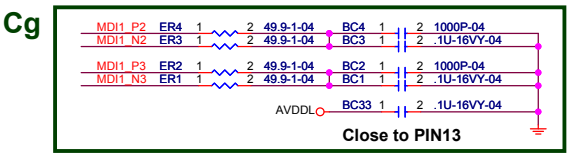
	AR8151-B 1000M	AR8152-B 10/100M	AR8161-B 1000M
Ca	AR8151-BL1A-R	AR8152-BL1A-R	AR8161-B
Cb	V	X	X
Cc	USBX2-LAN-1000	USBX2-LAN-100	USBX2-LAN-1000
Cd	X	V	X
Ce	0-04	.01U-25VX-04	0-04
Cf	V	X	V
Cg	V	X	X
Ch	X	V	X
Ci	V	V	X
Cj	V	X	V
Ck	V	X	X
Cl	X	X	V
Cm	V	V	X
Cn	V	V	X

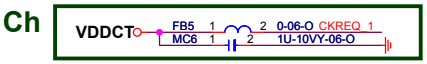
Closed To PWR Loading Pin



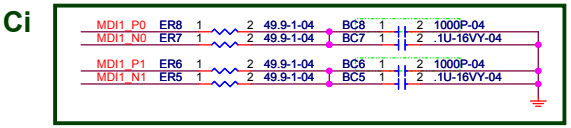
Closed To PWR Source Pin

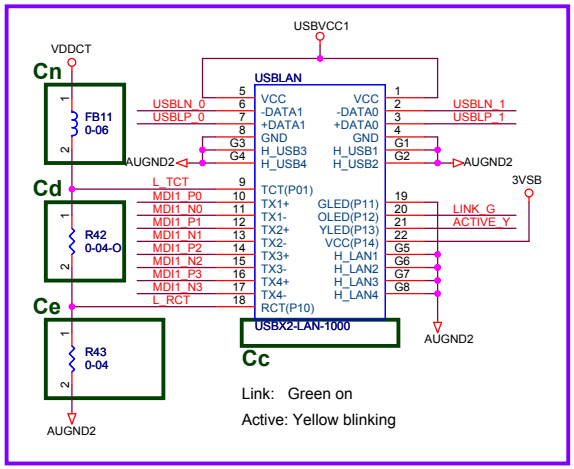






20100929
Change By Andy lu





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Title	AR8151-B / AR8152-B
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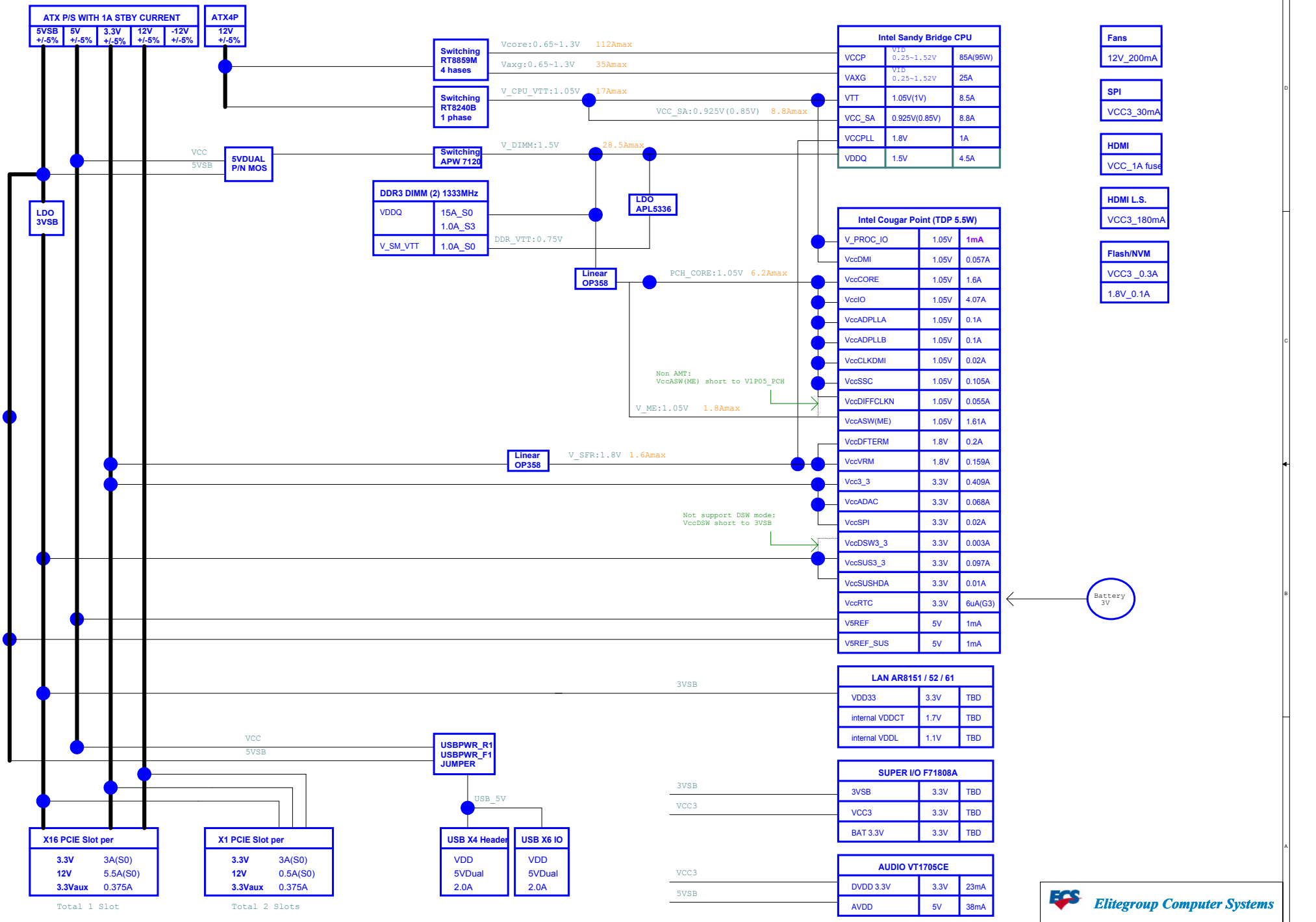
ATX P/S WITH 1A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
-12V +/-5%
ATX4P
12V +/-5%
Switching RT8859M 4 hases
Vcore:0.65~1.3V 112Amax
Vaxg:0.65~1.3V 35Amax
Switching RT8240B 1 phase
V_CPU_VTT:1.05V 17Amax
VCC_SA:0.925V(0.85V) 8.8Amax
Intel Sandy Bridge CPU
VCCP VID 0.25~1.52V 85A(95W)
VAXG VID 0.25~1.52V 25A
VTT 1.05V(1V) 8.5A
VCC_SA 0.925V(0.85V) 8.8A
VCCPLL 1.8V 1A
VDDQ 1.5V 4.5A
Fans
12V_200mA
SPI
VCC3_30mA
HDMI
VCC_1A fuse
HDMI L.S.
VCC3_180mA
Flash/NVM
VCC3 _0.3A
1.8V_0.1A
VCC
5VSB
5VDUAL P/N MOS
Switching APW 7120
V_DIMM:1.5V 28.5Amax
LDO 3VSB
DDR3 DIMM (2) 1333MHz
VDDQ 15A_S0 1.0A_S3
V_SM_VTT 1.0A_S0
LDO APL5336
DDR_VTT:0.75V
Linear OP358
PCH_CORE:1.05V 6.2Amax
Intel Cougar Point (TDP 5.5W)
V_PROC_IO 1.05V 1mA
VccDMI 1.05V 0.057A
VccCORE 1.05V 1.6A
VccIO 1.05V 4.07A
VccADPLLA 1.05V 0.1A
VccADPLLB 1.05V 0.1A
VccCLKDMI 1.05V 0.02A
VccSSC 1.05V 0.105A
VccDIFFCLKN 1.05V 0.055A
VccASW(ME) 1.05V 1.61A
VccDFTERM 1.8V 0.2A
VccVRM 1.8V 0.159A
Vcc3_3 3.3V 0.409A
VccADAC 3.3V 0.068A
VccSPI 3.3V 0.02A
VccDSW3_3 3.3V 0.003A
VccSUS3_3 3.3V 0.097A
VccSUSHDA 3.3V 0.01A
VccRTC 3.3V 6uA(G3)
V5REF 5V 1mA
V5REF_SUS 5V 1mA
Non AMT:
VccASW(ME) short to V1P05_PCH
V_ME:1.05V 1.8Amax
Linear OP358
V_SFR:1.8V 1.6Amax
Not support DSW mode:
VccDSW short to 3VSB
Battery 3V
3VSB
LAN AR8151 / 52 / 61
VDD33 3.3V TBD
internal VDDCT 1.7V TBD
internal VDDL 1.1V TBD
VCC
5VSB
USBPWR_R1
USBPWR_F1
JUMPER
USB_5V
3VSB
VCC3
SUPER I/O F71808A
3VSB 3.3V TBD
VCC3 3.3V TBD
BAT 3.3V 3.3V TBD
VCC3
5VSB
AUDIO VT1705CE
DVDD 3.3V 3.3V 23mA
AVDD 5V 38mA
X16 PCIE Slot per
3.3V 3A(S0)
12V 5.5A(S0)
3.3Vaux 0.375A
Total 1 Slot
X1 PCIE Slot per
3.3V 3A(S0)
12V 0.5A(S0)
3.3Vaux 0.375A
Total 2 Slots
USB X4 Header
VDD 5VDual 2.0A
USB X6 IO
VDD 5VDual 2.0A
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Power Delivery
Size C
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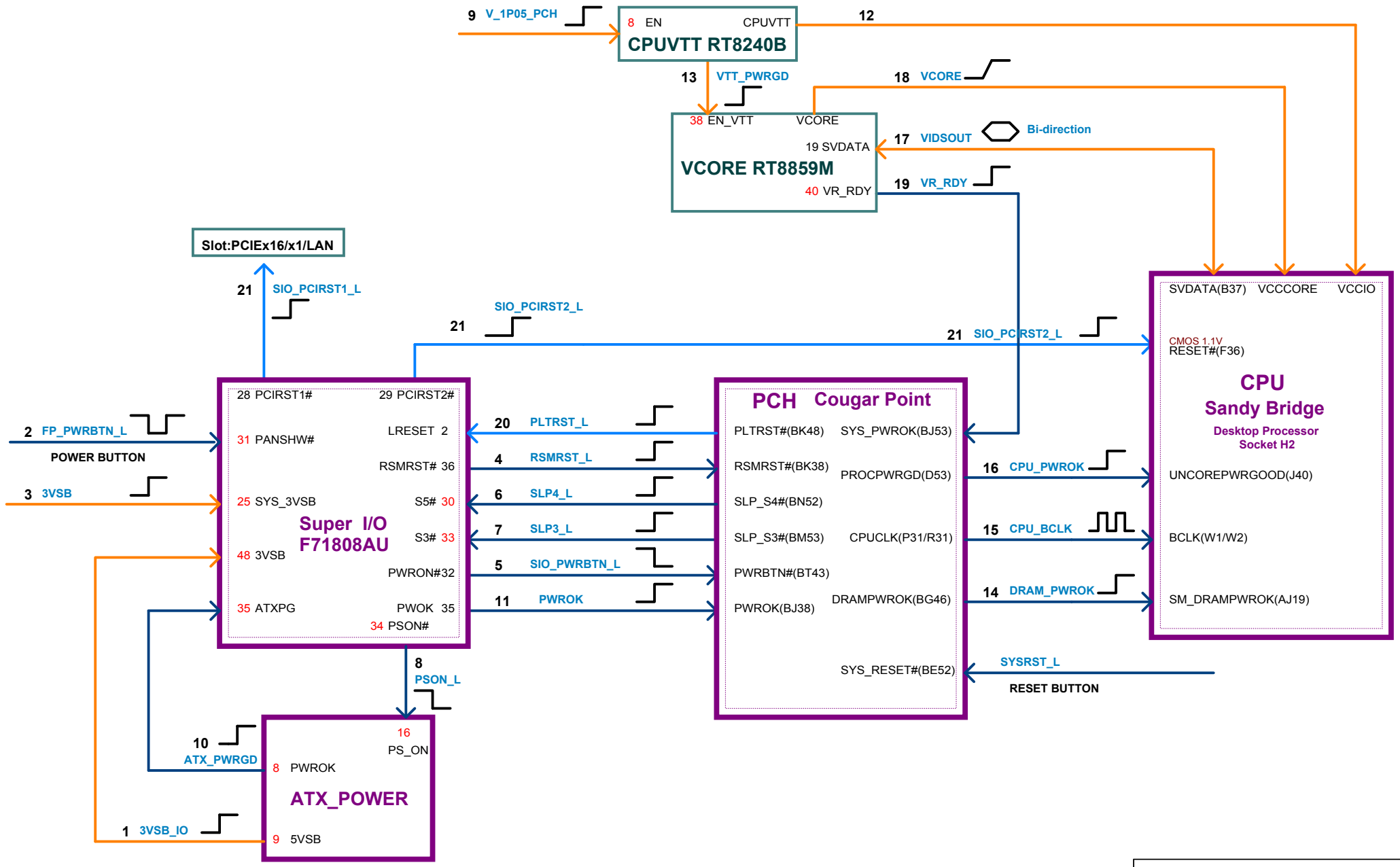

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Title: PWR Sequence / RST Diagram

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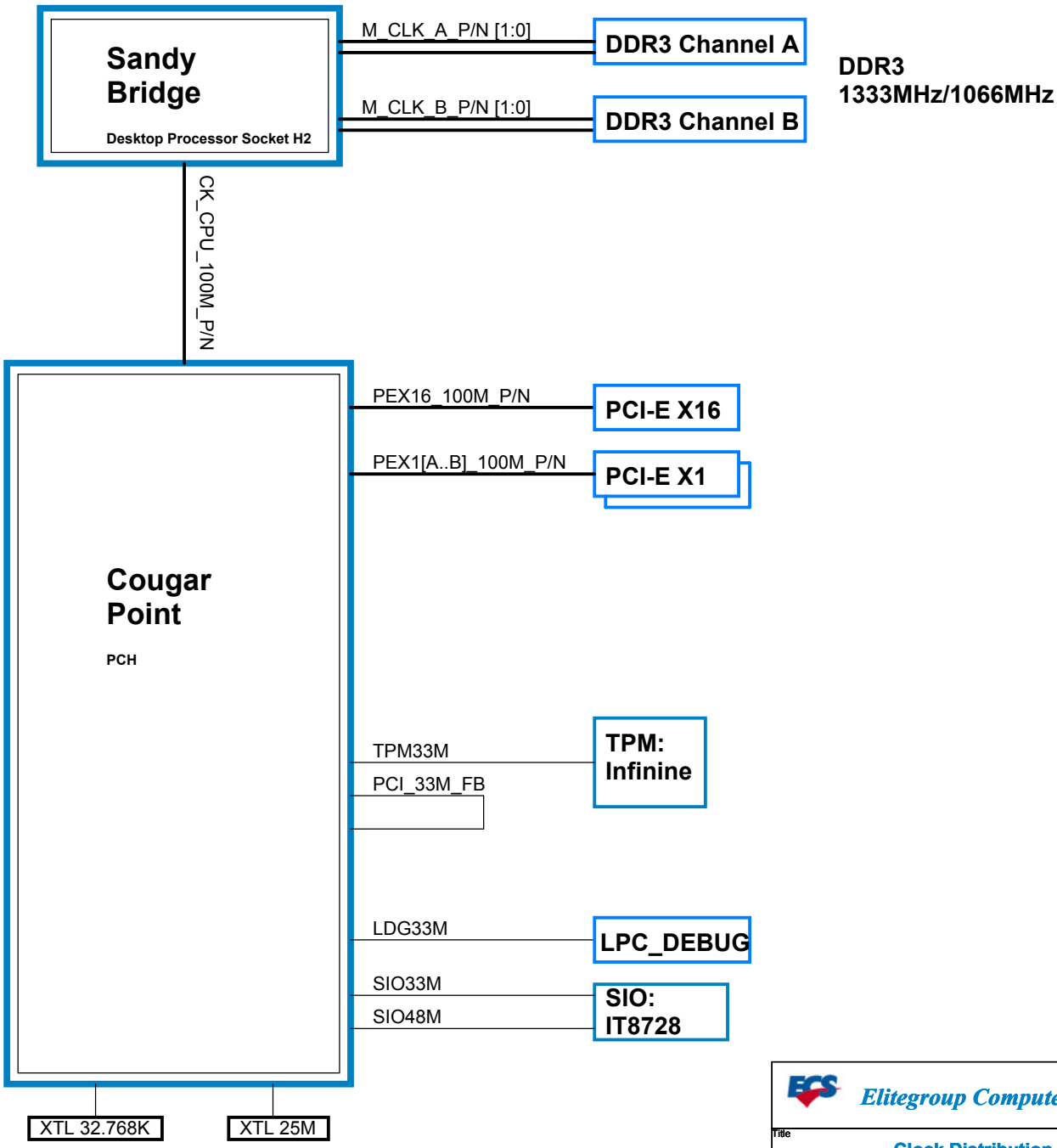
NOTE:

Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.
Please refer to
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
Page.13 PCH - SATA, SATA CONN for CLK IN PD
Page.14 PCH - MISC, F/W Strap
Page.15 PCH - CLK IO, CKG - CV184 for Option

1129'10 By Jayson modified



1129'10 By Jayson Del CK505

Elitegroup Computer Systems

Title: Clock Distribution

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