Model Name : CILL1 (Lenovo)
CILL2 (NEC)
File Name : LA-C422P

Compal Confidential

Lin-2 M/B Schematics Document

Intel Kabylake U Processor with DDR4

Rev. 1.0

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Issued Date	2016/03/21	Deciphered Date	2017/03/01

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Title: Cover Page		
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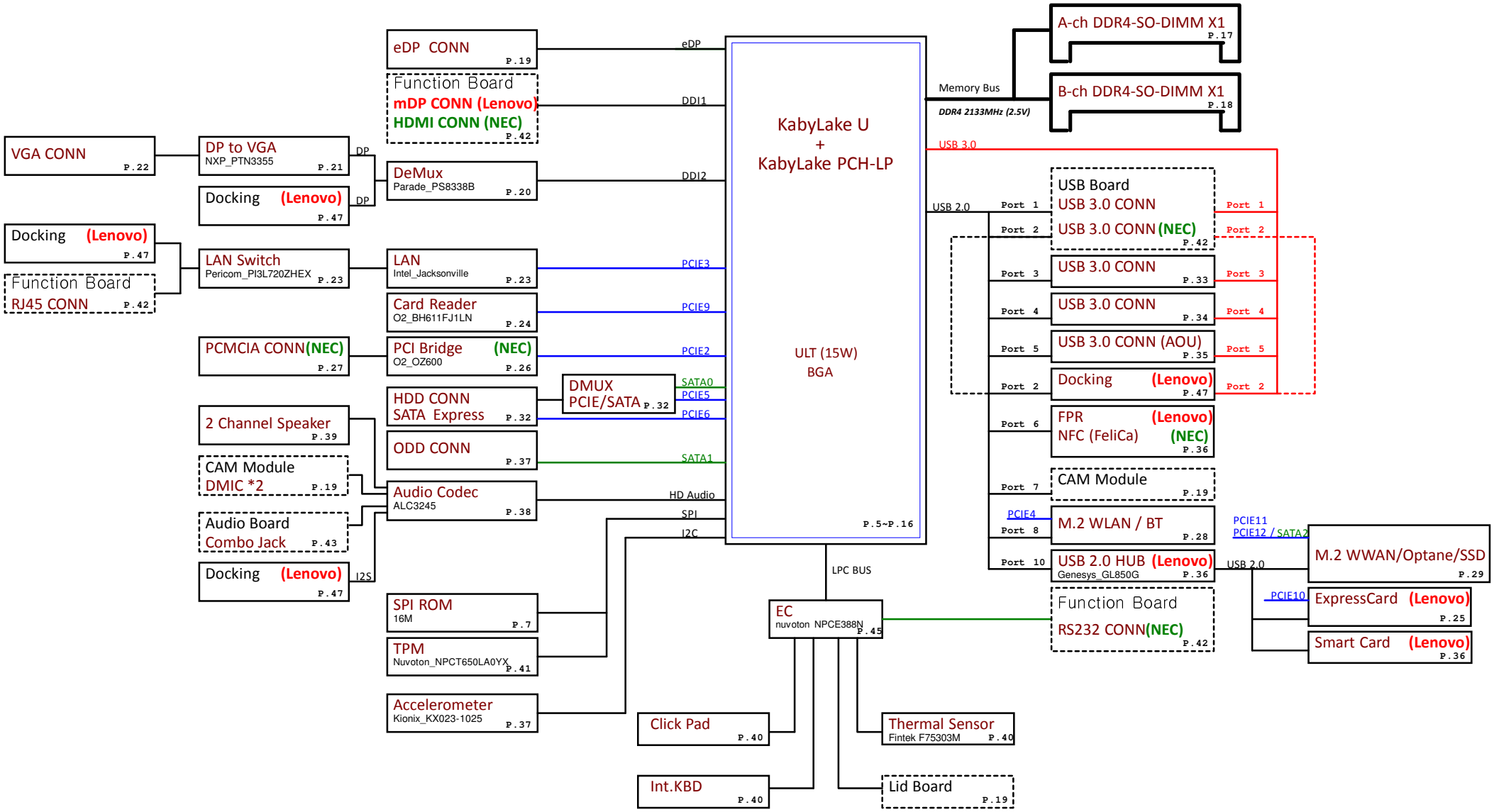
Date: Tuesday, November 15, 2016	Sheet 1 of 58	



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Title: Block Diagram

Size	Document Number	Rev
Custom	LA-C422P	1.0

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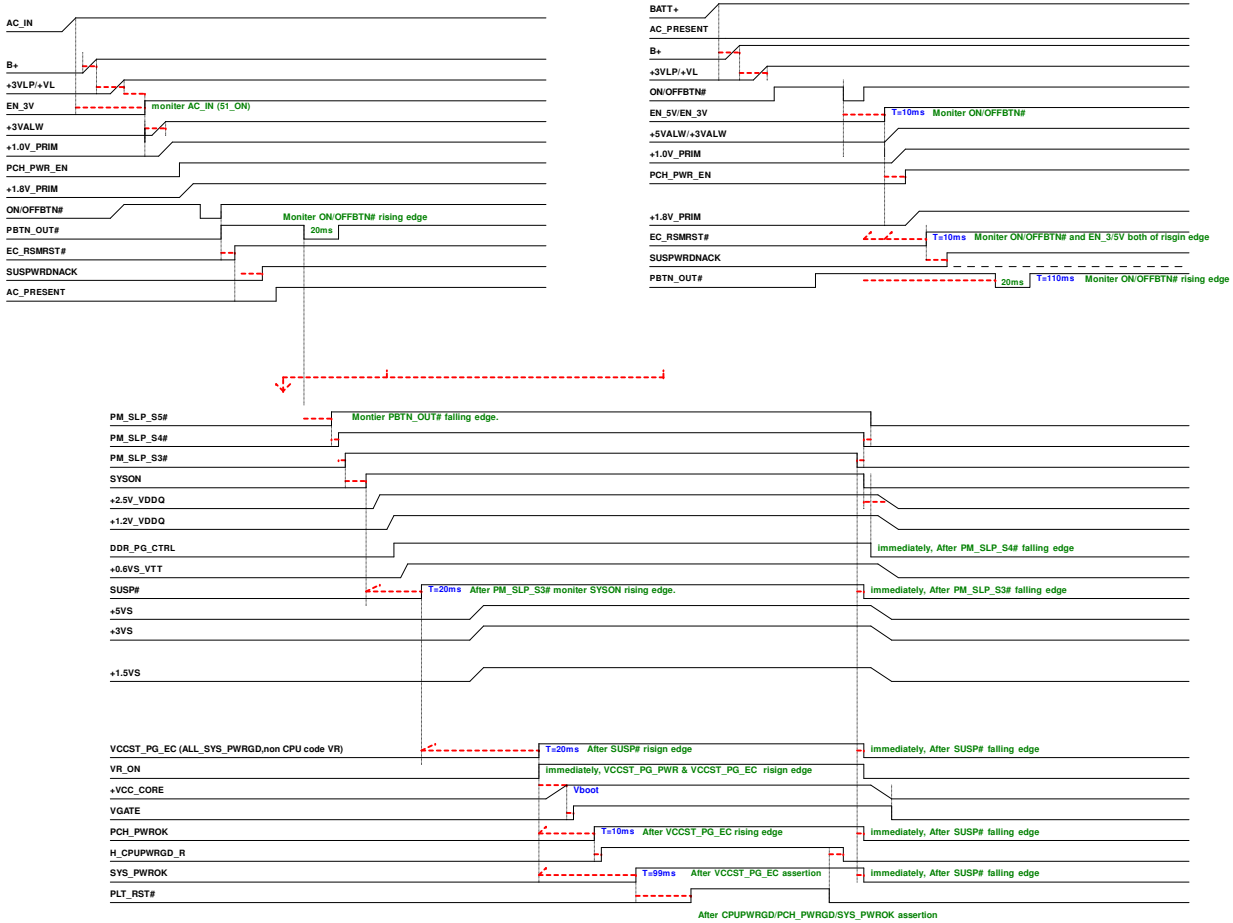
[CILL1 PWR Sequence_KBL-U_DDR4_Non-Deep Sx]

[AC Mode]



[DC Mode]

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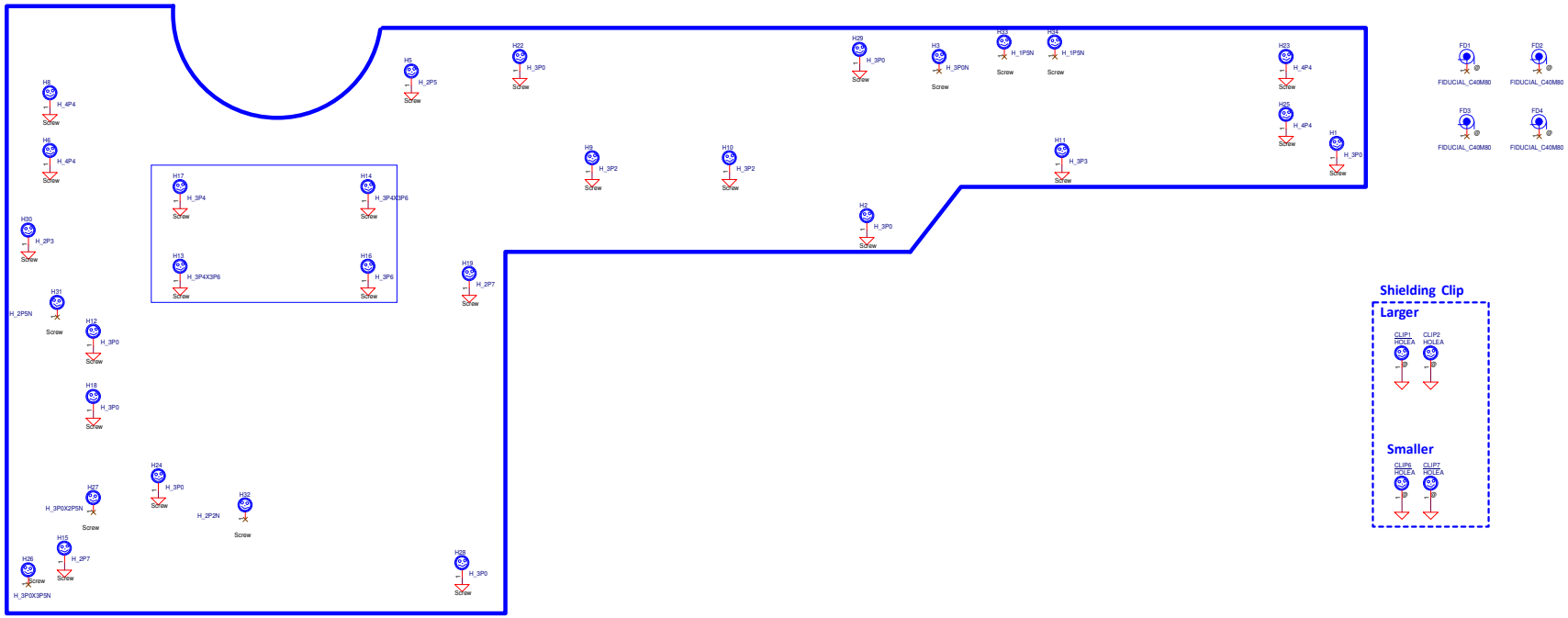
			Size: D; Document Number: LA-C422P; Rev: 1.0
			Date: Tuesday, November 15, 2016; Sheet 3 of 58



PCB

ZZZ
PCB
DAZ1SS00100

CPU

U1
CPU13@
SA0000ADM30
FJ8067702739934 SR34A H0 2.2G

U1
CPU19@
SA0000ADL40
FJ8067702739933 SR349 H0 1.8G

X4E

ZZZ1
EMC_LNV
Lenovo@

U1
CPU14@
SA0000A3BG0
FJ8067702739738 SR2ZW H0 2.4G

ZZZ2
EMC_NEC
NECPremium@

U1
CPU15@
SA0000A37G0
FJ8067702739739 SR2ZU H0 2.5G

ZZZ3
EMC_NEC
NECBase@

U1
CPU16@
SA0000ADC00
FJ8067702739633 SR340 H0 2.6G

U1
CPU17@
SA0000A3AE0
FJ8067702739740 SR2ZV H0 2.7G

U1
CPU18@
SA0000ADP30
FJ8067702739628 SR33Z H0 2.8G

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5
+3VL_RTC	RTC power	ON	ON	ON	ON
+3VLP	+19VB to +3VLP power rail	ON	ON	ON	ON
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+1.8V_PRIM	System +1.8V power rail	ON	ON	ON	ON*
+1.0V_PRIM	System +1.0V power rail	ON	ON	ON	ON*
+1.0V_MPHYPLL	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF
+2.5V	DDR4 +2.5V power rail	ON	ON	ON	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+1.0VS_VCCIO	+1.0VS IO power rail	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VS	System +3VS power rail	ON	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

SIT BOM Structure Table

BTO Item	BOM Structure	Remark
vPRO	M3@	vPRO sku
non vPRO	NOM3@	non vPRO sku
FPR/Docking	Lenovo@	LNV
USB Hub/WWAN/ Express/Smart card	LNVHUB@	LNV Premium-U
PCMCIA/NFC	NEC@	NEC
TPM_Infineon	TPMi@	LNV NEC
TPM_ST	TPMs@	LNV NEC
APS_Kionix	APSk@	LNV NEC
APS_ST	APSs@	NA
Premiun-U	Premium@	Premiun-U Sku
ESD requirement	ESD@	LNV NEC
ESD reserve	@ESD@	NA
EMI requirement	EMI@	LNV NEC
EMI reserve	@EMI@	NA
RF requirement	RF@	LNV NEC
RF reserve	@RF@	NA
XDP	XDP@	LNV NEC

I/O mapping

	Define.	LIN-2	
1	USB3#1	USB3#1_Rear	
2	USB3#2	USB3#2_Docking (LNV) USB3#2_Right-1 (NEC)	
3	USB3#3	USB3#3_Right-2	
4	USB3#4	USB3#4_Right-3	
5	USB3#5/PCIE#1	USB3#5_Left	
6	USB3#6/PCIE#2	PCIE2_PCMCIA Bridge (NEC)	
7	PCIE#3/Gbe	PCIE#3_GBE	
8	PCIE#4/Gbe	PCIE#4_WLAN	
9	PCIE#5/Gbe	PCIE#5_L0	M.2 2280 SSD
10	PCIE#6	PCIE#5_L1	
11	PCIE#7/SATA#0	SATA#0_HDD	
12	PCIE#8/SATA#1	SATA#1_ODD	
13	PCIE#9/Gbe	PCIE#5_Card Reader	
14	PCIE#10/Gbe	PCIE#6_Express Card	
15	PCIE#11/SATA#1	PCIE#11_L1	
16	PCIE#12/SATA#2	PCIE#11_L0/SATA#2	Optane/ 2242 SSD

USB 2.0

	LIN
1	USB3_Rear
2	USB3_Docking (LNV) USB3_Right-1 (NEC)
3	USB3_Right-2
4	USB3_Right-3
5	USB3_Left
6	FPR (LNV)
7	CAM
8	BT
9	X
10	USB 2.0 HUB (LNV)

USB 2.0 HUB (LNV)

	LIN
1	WWAN (LNV)
2	Express Card (LNV)
3	Smart Card (LNV)
4	X

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H
Charger	0001 011X b	12H

EC SM Bus2 address

Device	Address	HEX
Thermal Sensor Fintek F75303M	1001_101xb	9AH
Thermal Sensor ON-semi ADM1032	0100_110xb	4CH
CPU Intel KBL-U		
APS Kionix KX023-1025	0011_110xb	3Ch/3Dh
APS ST LIS3DHTR	0011_100xb	30h/31h

(LNV)

PCH SM Bus address

Device	Address	HEX
DDR DIMM1	1001 000Xb	A0H/A1H
DDR DIMM2	1001 001Xb	A3H/A4H
Synaptics Inter Touch Click Pad	TBD	TBD

PCH SM Link0 address

Device	Address	HEX
LAN Intel WGI219		C8H

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Title: Notes_List

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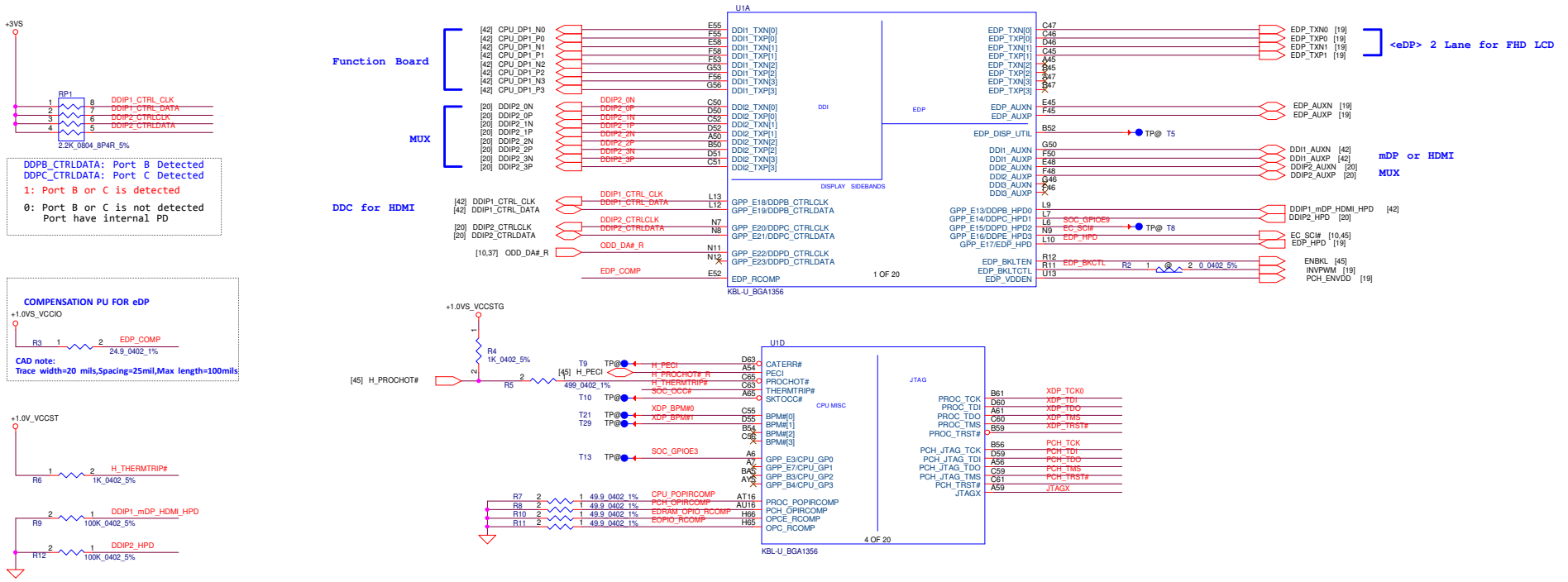

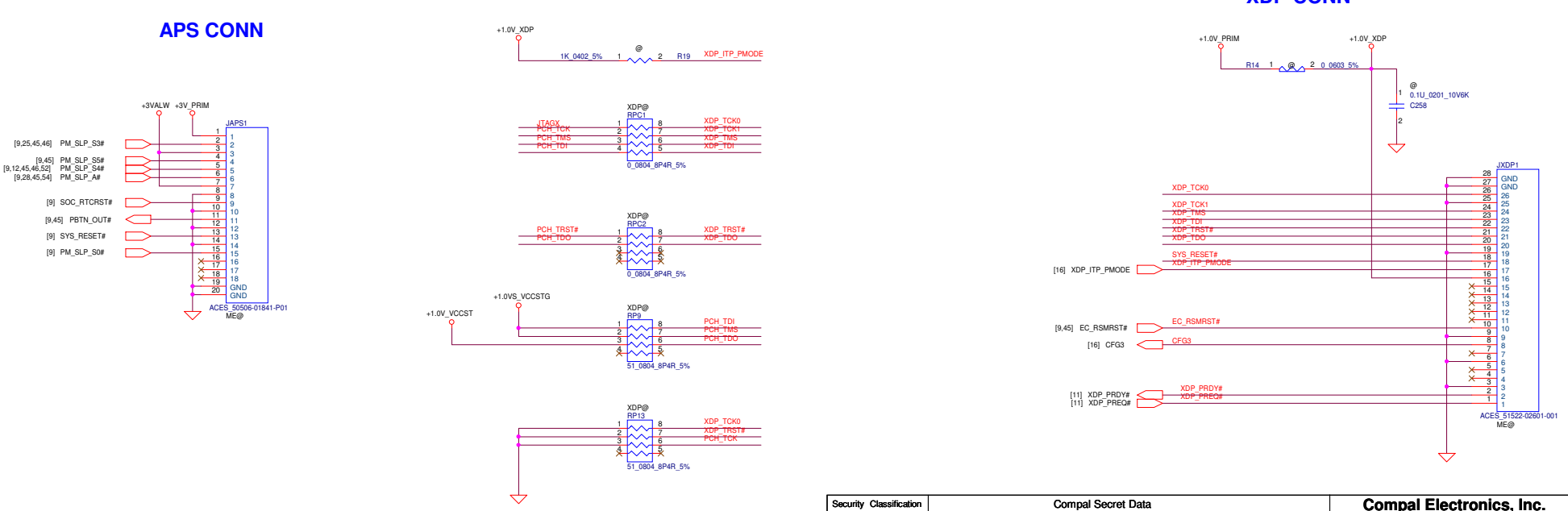

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Title: **KBL ULT(1/12) DDI,MSIC,XDP**

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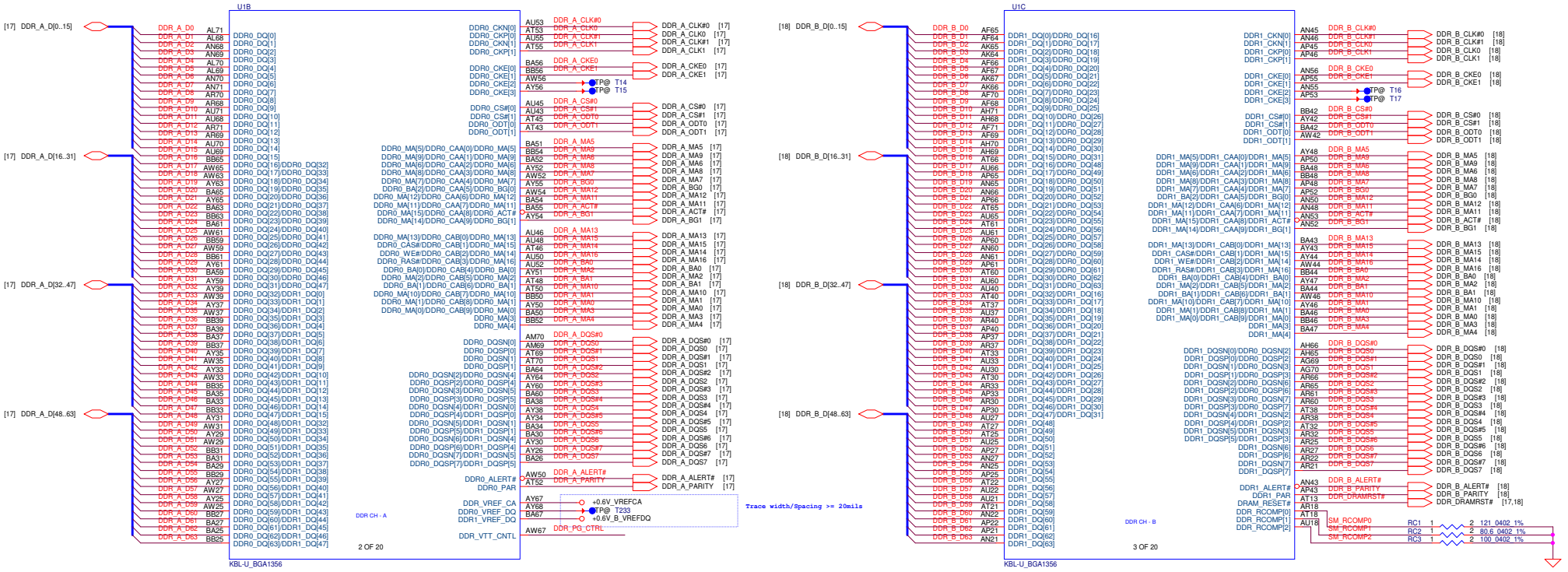
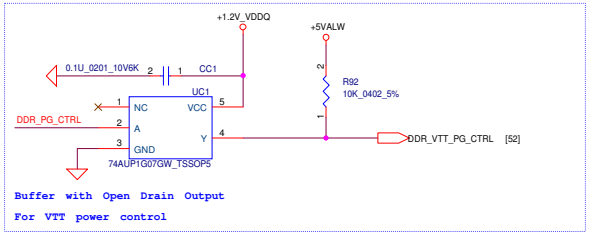
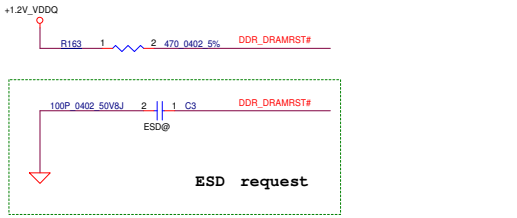
Interleaved Memory

LIN-2







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Title: **KBL ULT(2/12) DDR4**

Size	Document Number	Rev
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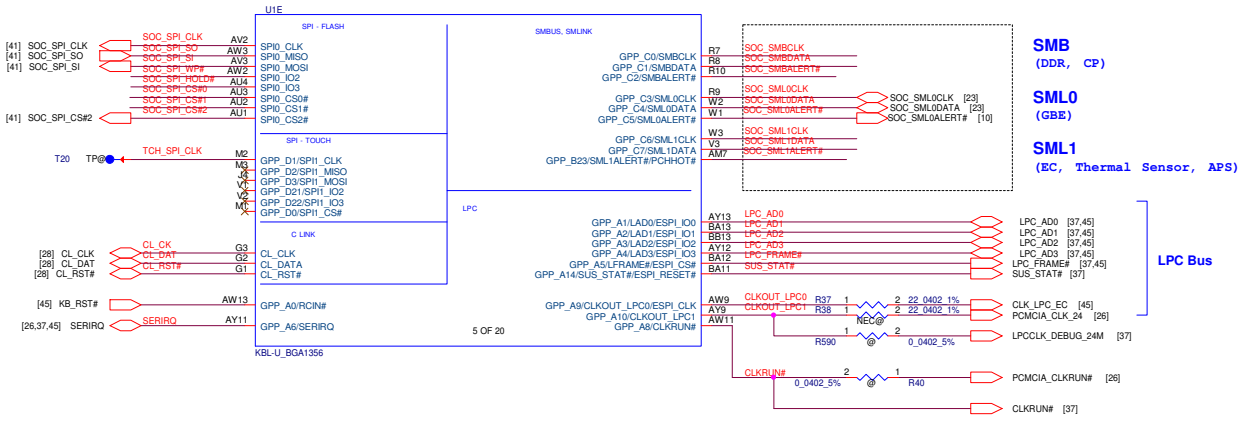
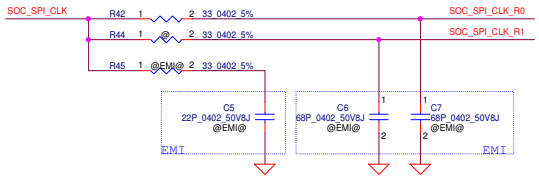
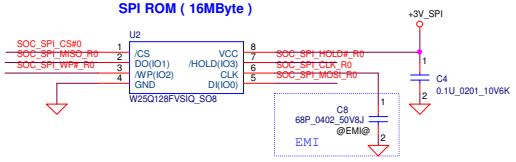
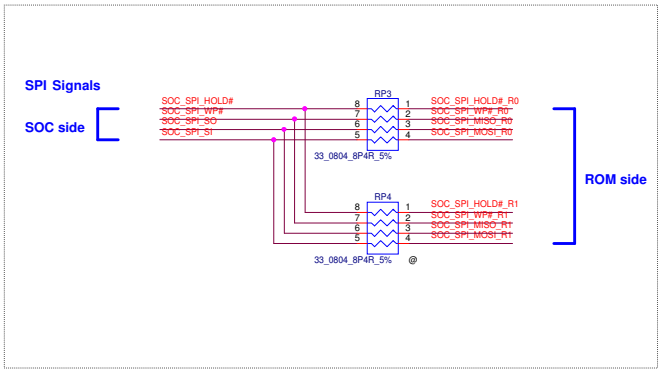
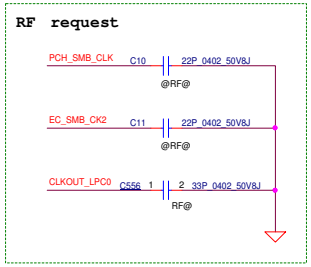


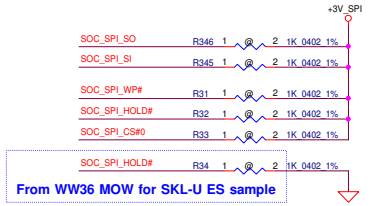


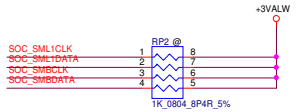


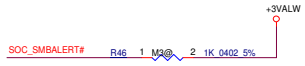
SPI ROM	Vendor	16MB	8MB	4MB
1st	Winbond	SA00005VV10	SA000039A30	SA00003K820
2nd				





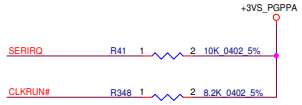


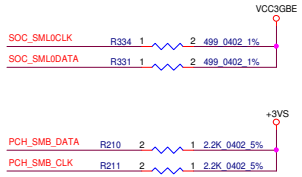




SMBALERT# / GPP_C2

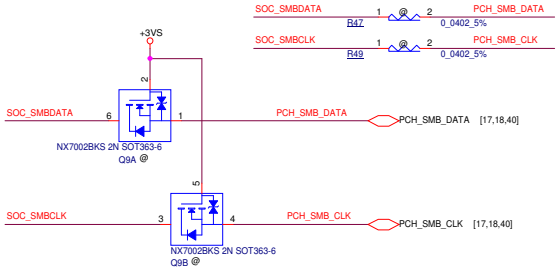
TLS	CONFIDENTIALITY
H	ENABLE
L	DISABLE





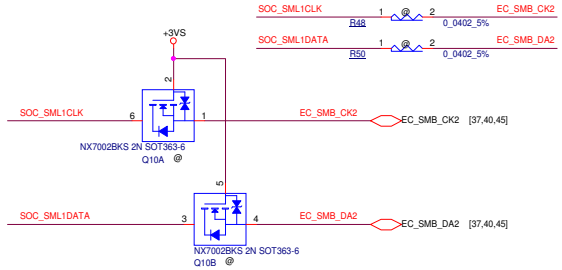
SOC_SMB (+3VALW)

PCH_SMB (+3VS)
DIMM1/DIMM2/ClickPad



SOC_SML1 (+3VALW)

EC_SMB (+3VS)
EC, Thermal Sensor, APS



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Title: KBL ULT(3/12) SPI,ESPI,SMB

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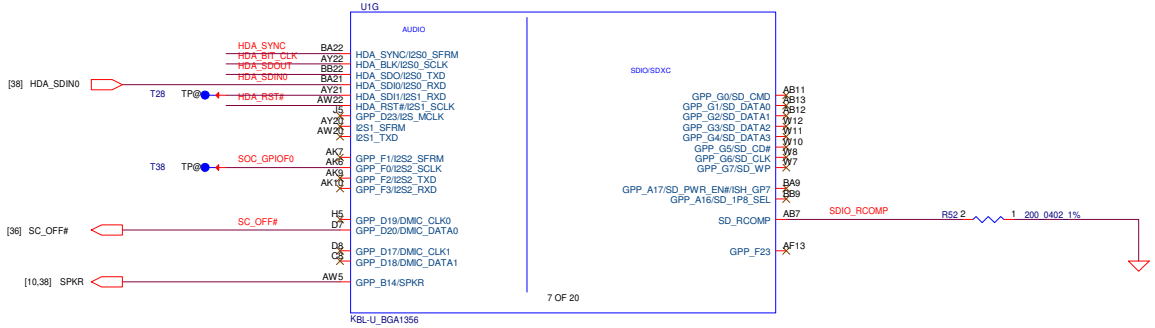

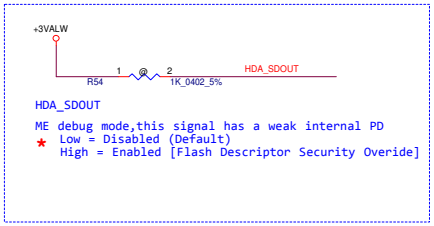

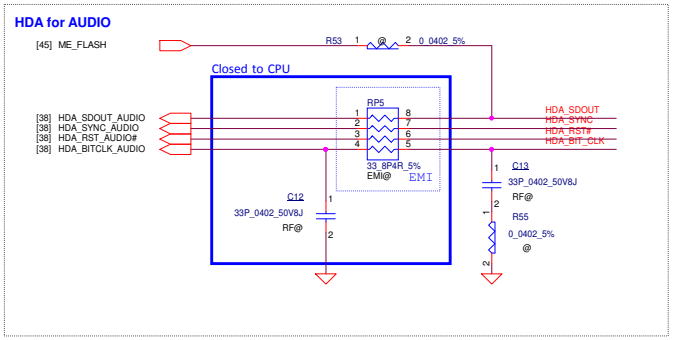

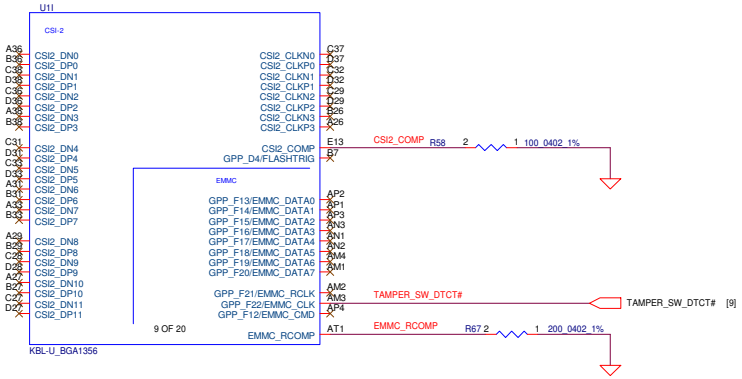

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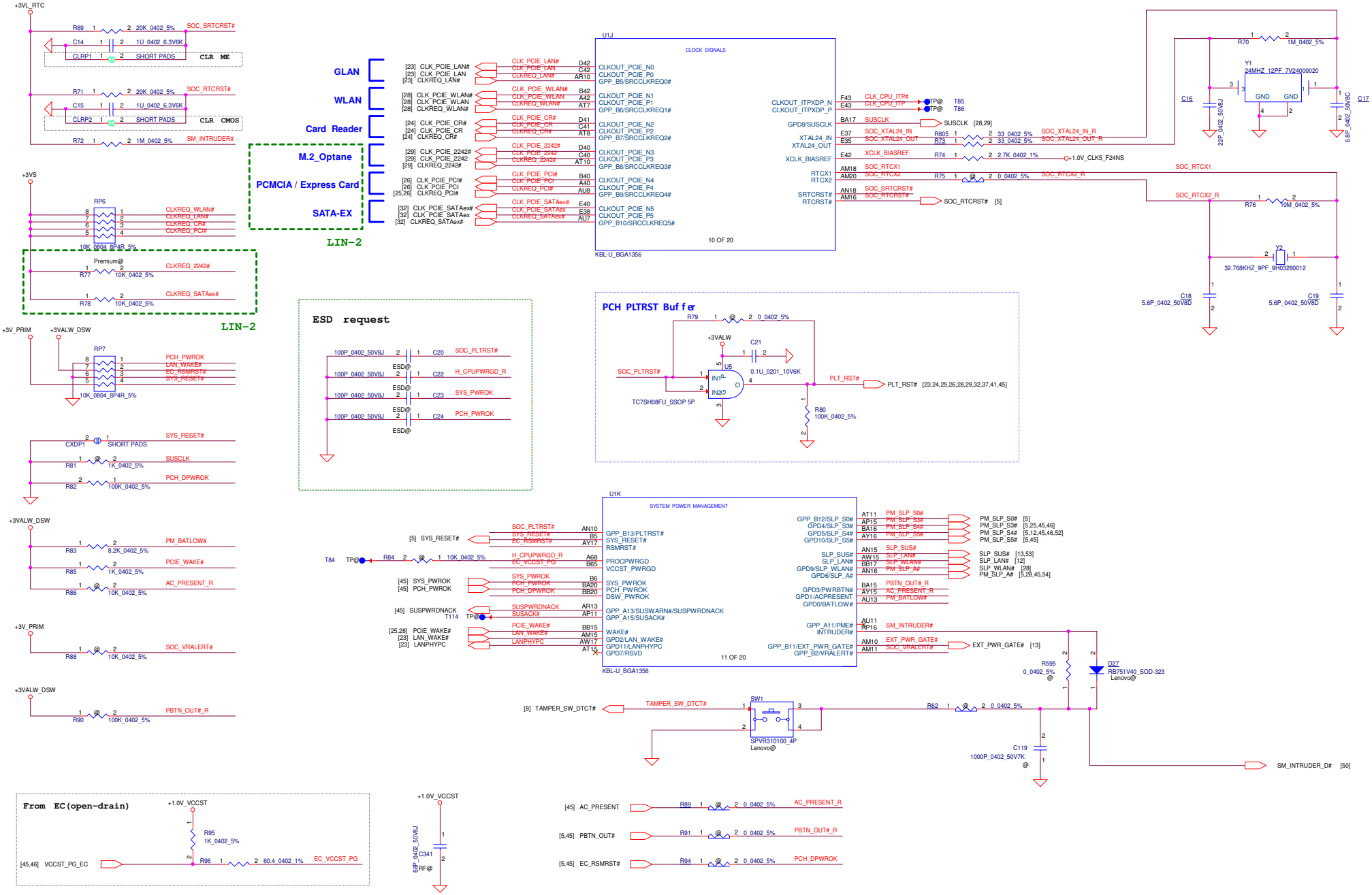
Title: **KBL ULT(4/12) HDA,EMMC,SDIO**

Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 8 of 58



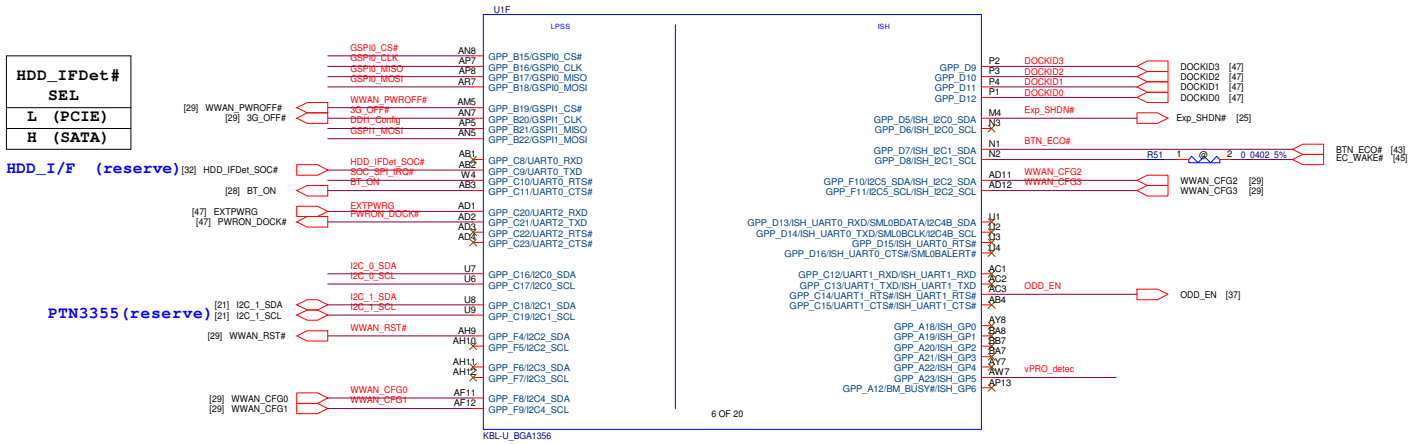
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

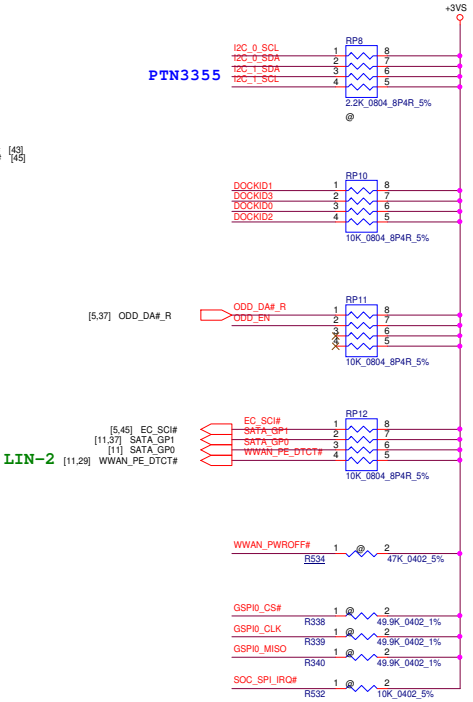
Compal Electronics, Inc.

Title: **KBL ULT(5/12) CLK,GPIO**

Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 9 of 58





Dock_ID3	Dock_ID2	Dock_ID1	Dock_ID0	Product
0	0	0	1	(RESERVE for NO DOCK)
0	0	1	0	GIDORAH
0	0	1	1	GODZILLA
0	1	0	0	MOTHRA

Functional Strap Definitions

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode.

1 = Enable TOP Swap Mode.

GSPI0_MOSI (Internal Pull Down):

No Reboot

0 = Disable No Reboot mode.

1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI (Internal Pull Down):

Boot BIOS Strap Bit

0 = SPI Mode

1 = LPC Mode

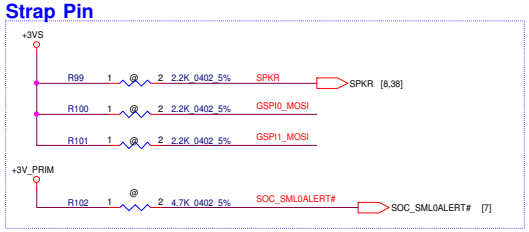
SML0ALERT# (Internal Pull Down):

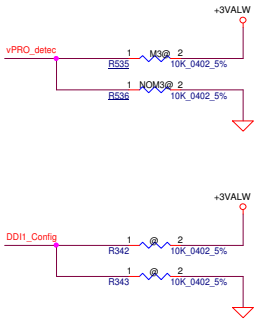
eSPI or LPC

0 = LPC is selected for EC --> For KB9022/9032 Use

1 = eSPI is selected for EC --> For KB9032 Only.

Strap Pin





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Compal Electronics, Inc.

Title: **KBL ULT(6/12) GPIO,LPIO**

Size	Document Number	Rev
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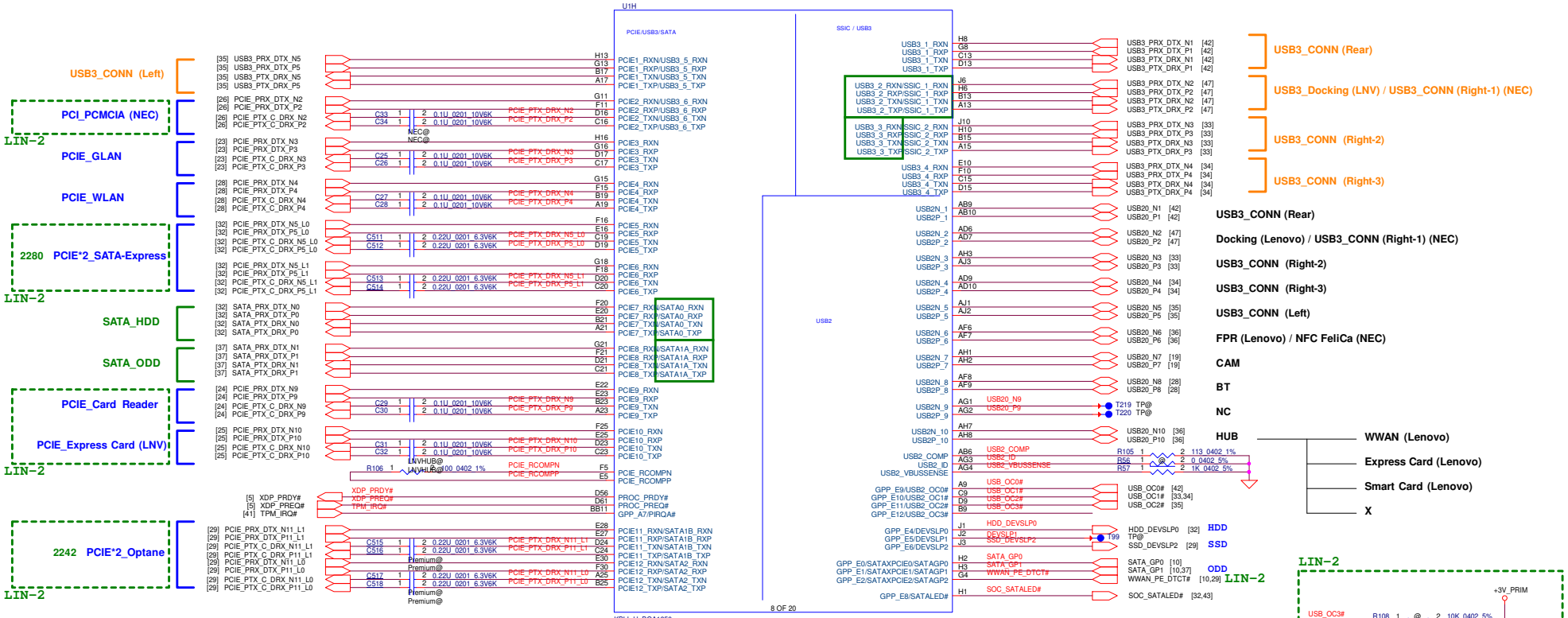
Date: Tuesday, November 15, 2016 | Sheet 10 of 58



WWAN_PE_DTCT#	
L	PCIE
H	SATA

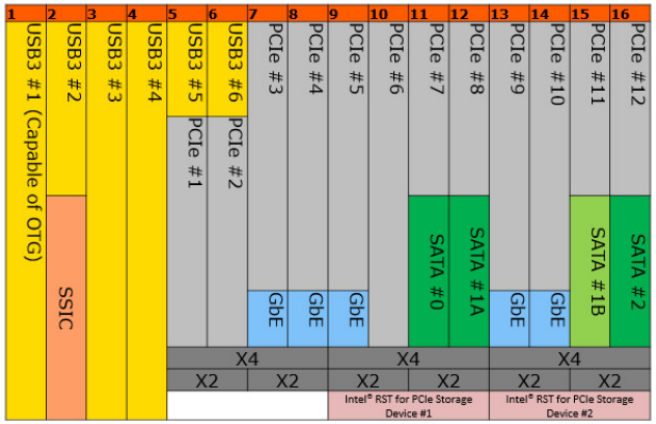


Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

GPIO	DEVICE CONTROL
USB_OC0#	USB3#1 ,2
USB_OC1#	USB3#3 ,4
USB_OC2#	USB3#5
USB_OC3#	NA
DEVSLP0	HDD
DEVSLP1	X
DEVSLP2	SSD
SATA_GP0	NA
SATA_GP1	ODD
SATA_GP2	WWAN_PE_DTCT#

Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

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Title: KBL ULT(7/12) PCIE,USB

Size	Document Number	Rev
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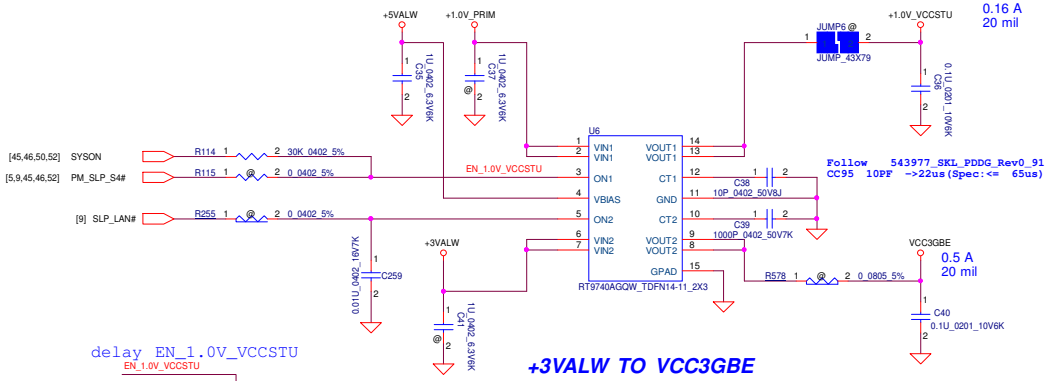
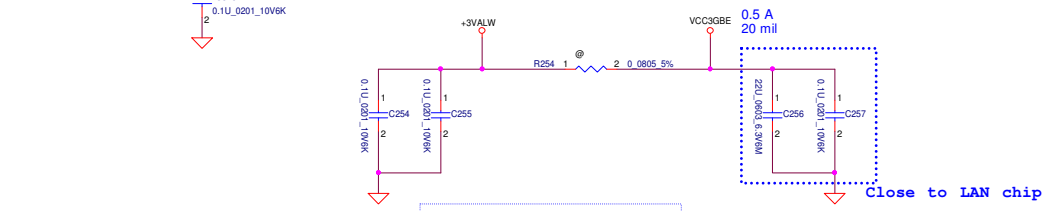
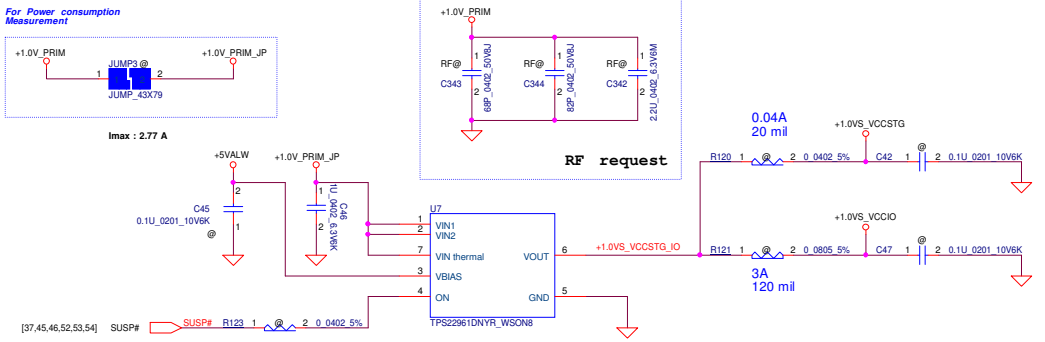
+1.0V_PRIM TO +1.0V_VCCSTU

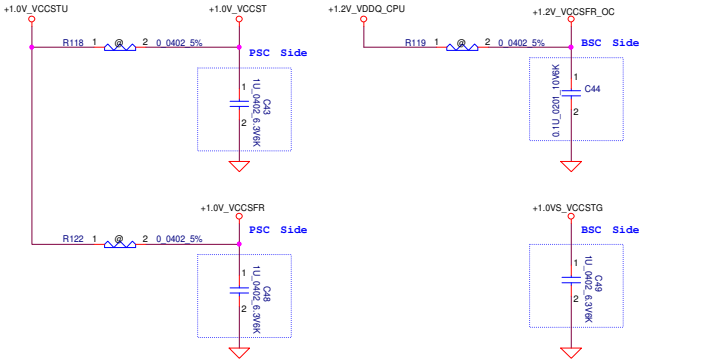


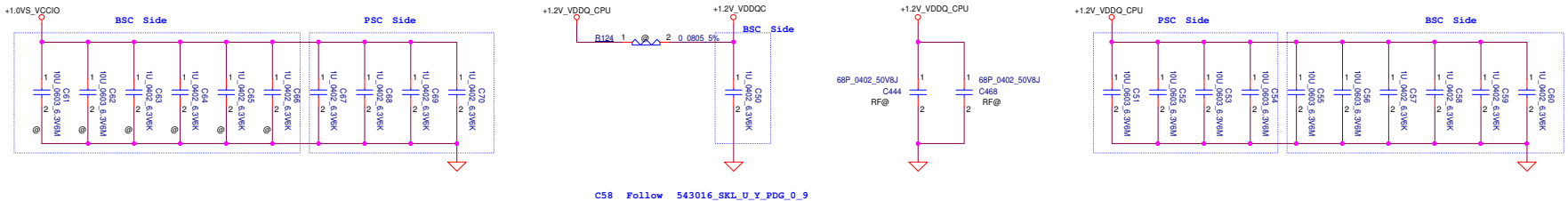
+3VALW TO VCC3GBE

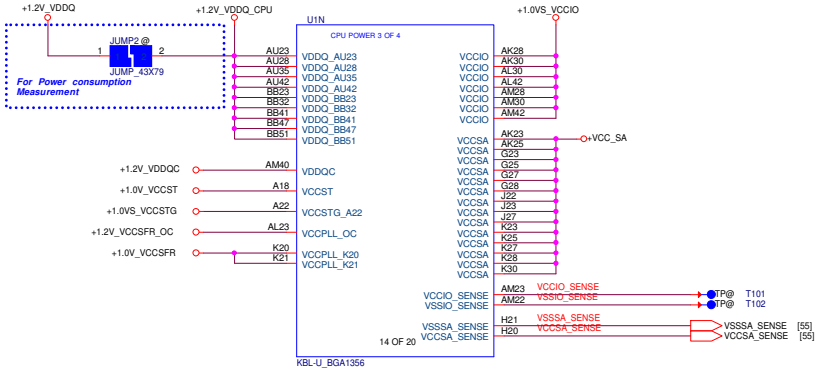


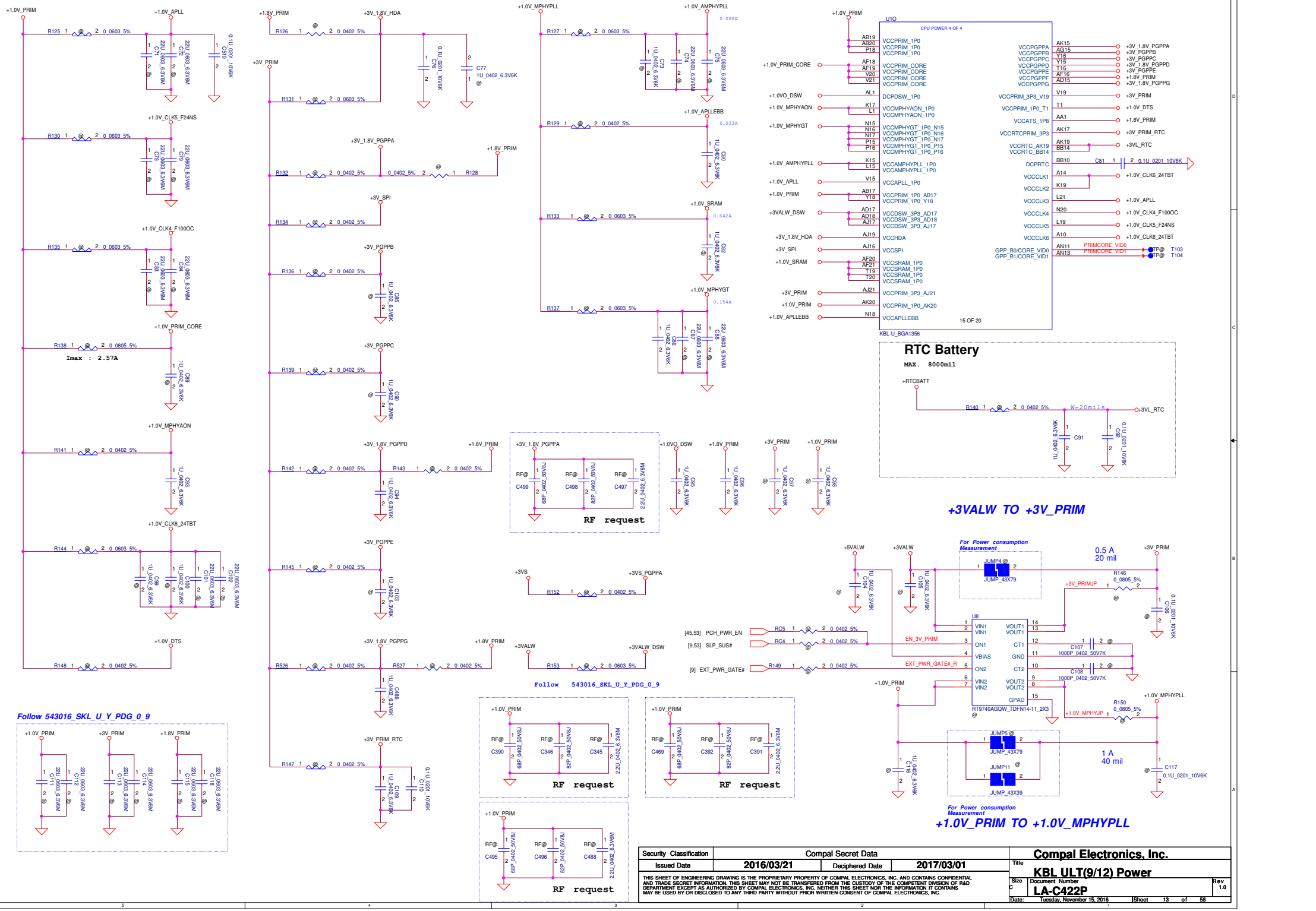


+1.0V_PRIM to +1.0VS_VCCSTG / +1.0VS_VCCIO









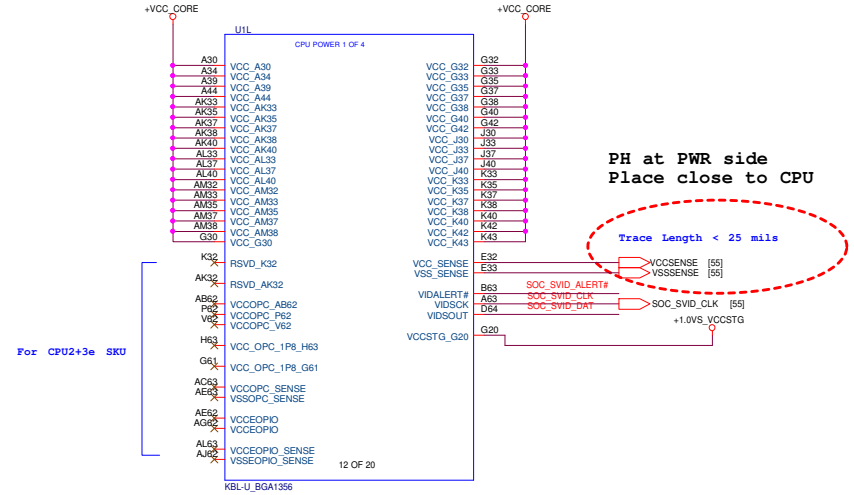
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

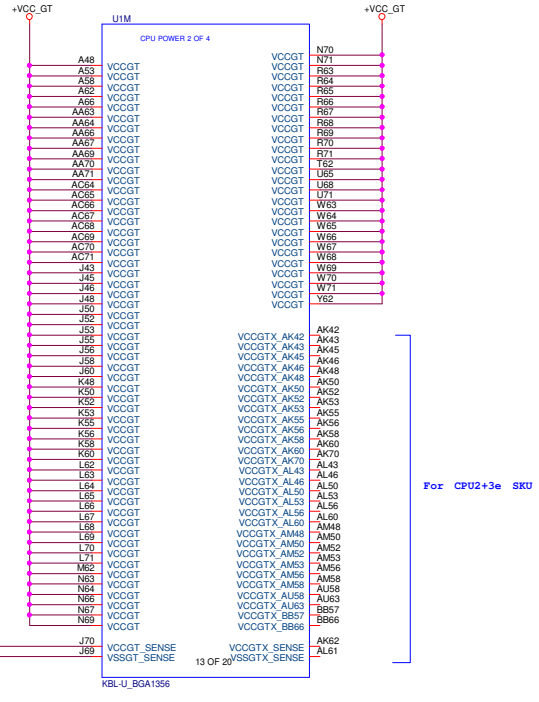
Compal Electronics, Inc.

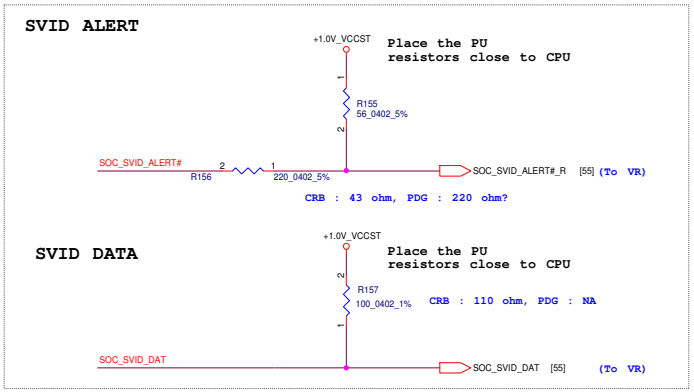
Title: **KBL ULT(9/12) Power**

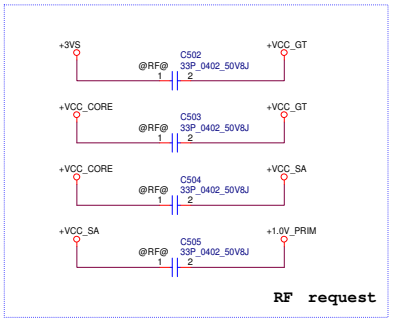
Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 13 of 58









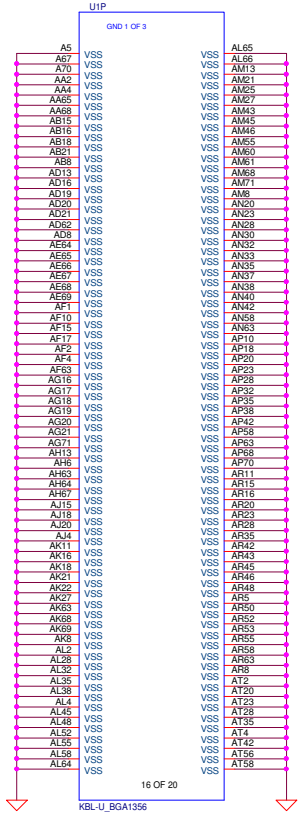
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

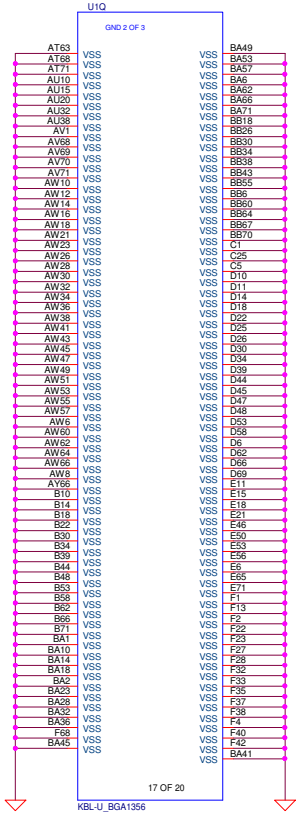
Compal Electronics, Inc.

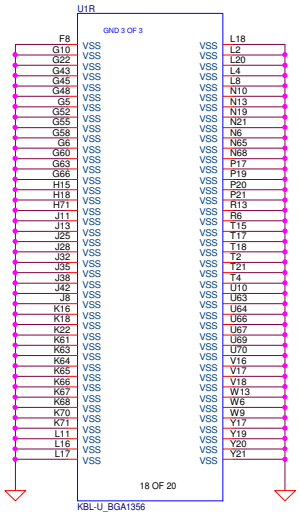
Title: KBL ULT(10/12) Power

Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 14 of 58





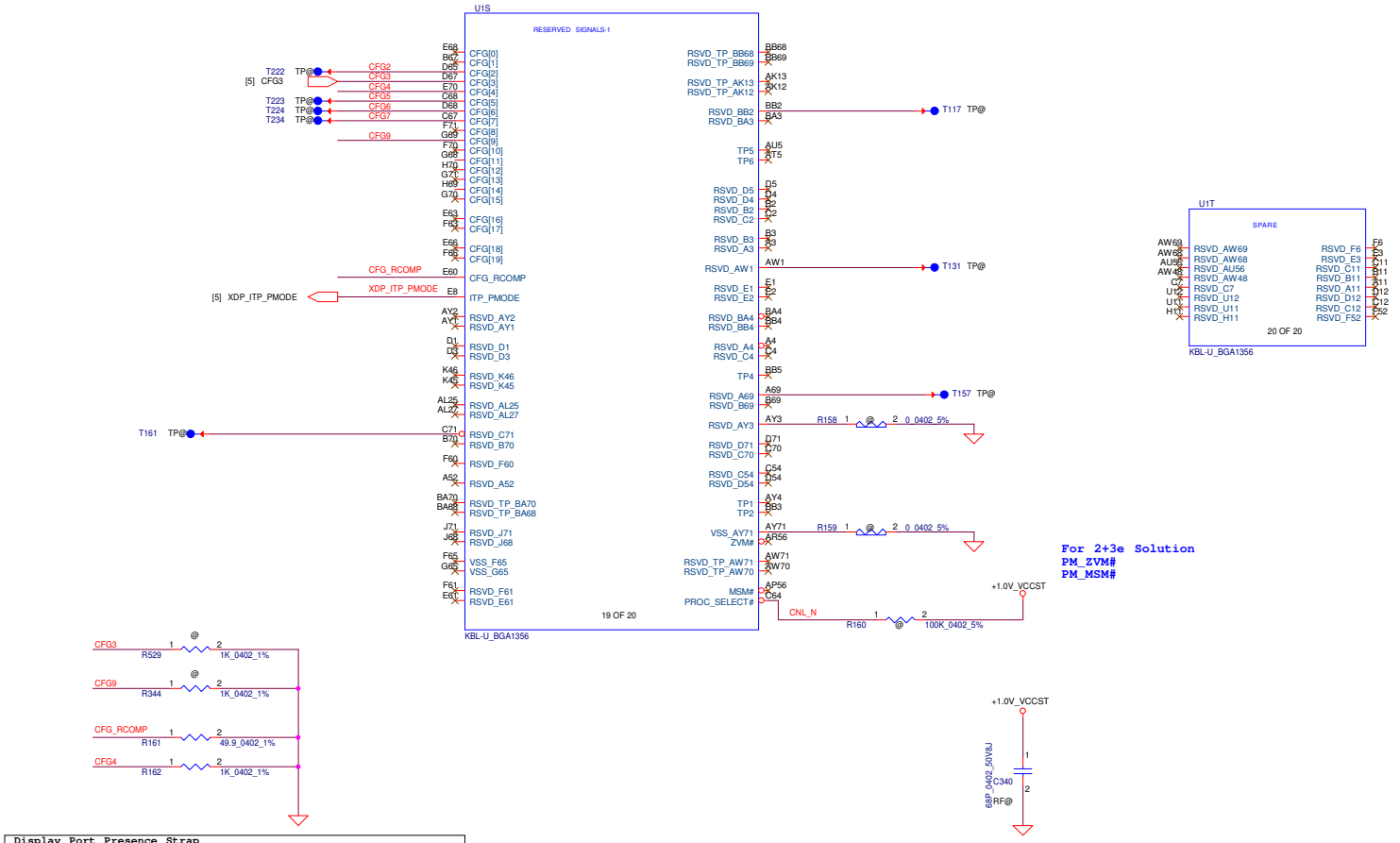


Compal Electronics, Inc.

Title: **KBL ULT(11/12) GND**

Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 15 of 58



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Compal Electronics, Inc.

Title: KBL ULT(12/12) RSVD

Size: C | Document Number: LA-C422P | Rev: 1.0

Date: Tuesday, November 15, 2016 | Sheet 16 of 58

Interleaved Memory

LIN-2

Reverse Type

2-3A to 1 DIMMs/channel

D/DQ Signals link to CPU

CMD Signals from CPU

Clock Signals from CPU

CTL Signals from CPU

SMBUS Signals link to CPU

ODT Signals to CH A

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note:
Place near JDIMM1.203,204

Layout Note:
Place near JDIMM1

Layout Note:
Place near JDIMM1

Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM1

JDIMM1

DEREN_40-42275-26002RHF

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

DIMM1 Side

CPU Side

Place near to SO-DIMM connector.

Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **DDR4 DIMMA**

Size	Document Number	Rev
Custom	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 17 of 58

Interleaved Memory

LIN-2

Reverse Type

2-3A to 1 DIMMs/channel

D/DQ Signals link to CPU

CMD Signals from CPU

Clock Signals from CPU

CTL Signals from CPU

SMBUS Signals link to CPU

ODT Signals to CH B

Layout Note:
Place near JDIMM2

Layout Note:
Place near JDIMM2

Layout Note:
Place near JDIMM2

Layout Note:
Place near JDIMM1

Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2

CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

DIMM2 Side

CPU Side

Place near to SO-DIMM connector.

Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: DDR4_DIMMB

Size: Custom | Document Number: LA-C422P | Rev: 1.0

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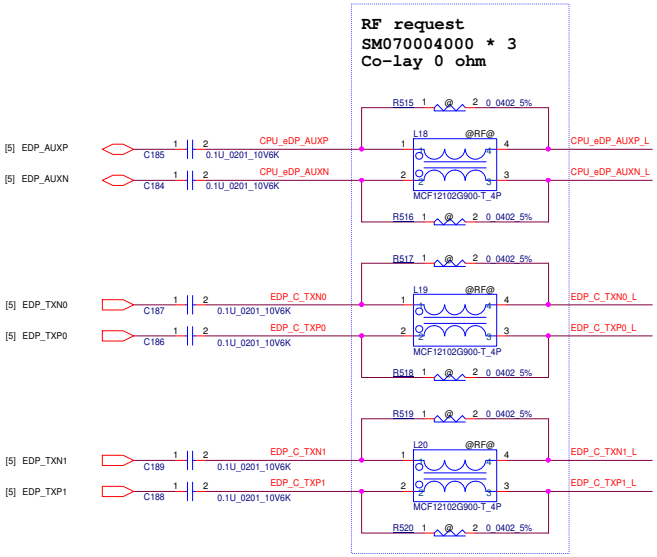
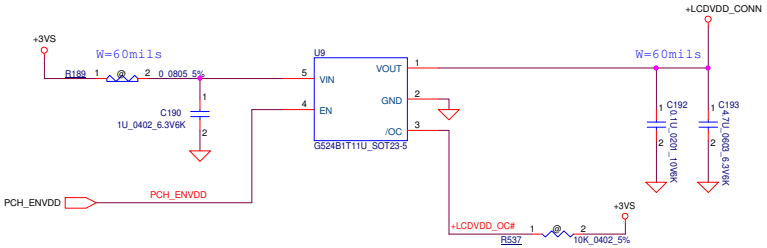
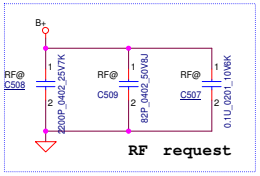
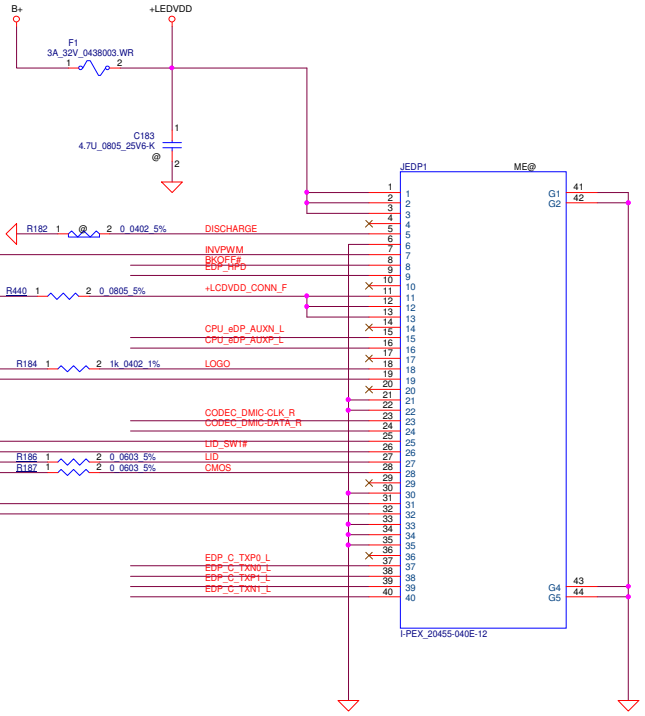
eDP + Camera / MIC / Lid



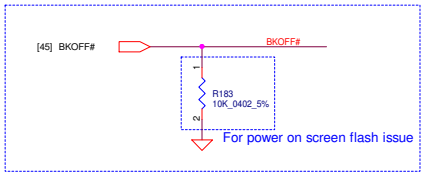


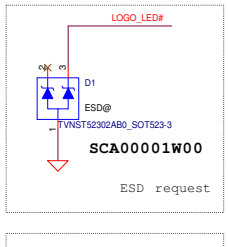


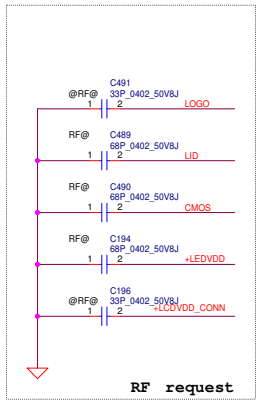


CAM/MIC/LID Module pin define

NO	Signal
1	VCC3M
2	LID_SWITCH
3	GND
4	MIC_CLK
5	MIC_DATA
6	MIC_DET#
7	GND
8	USB_D+
9	USB_D-
10	VCC3B







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Issued Date	2016/03/21	Deciphered Date	2017/03/01

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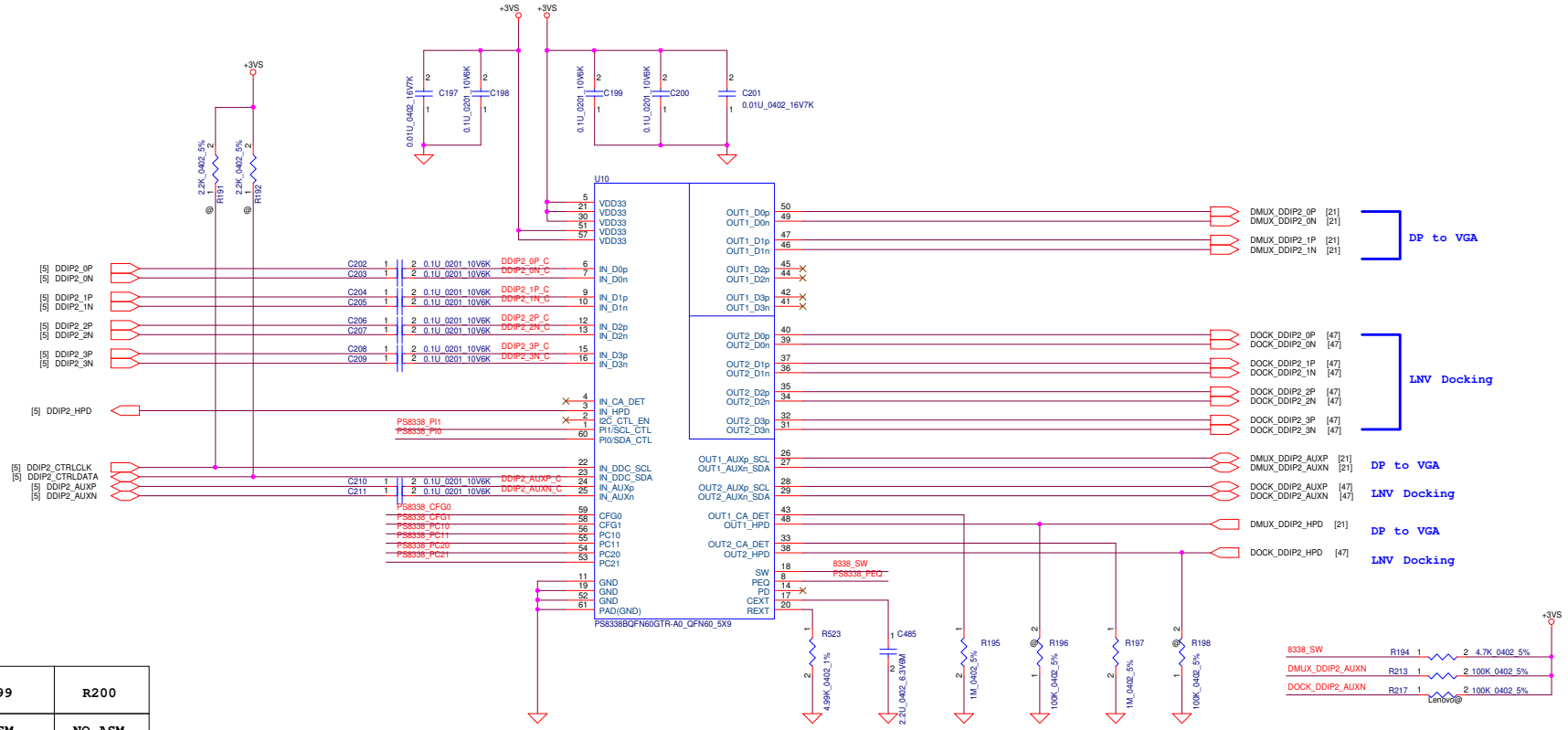
Compal Electronics, Inc.

Title: **eDP CONN**

Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 19 of 58



PEQ (INT PD)	R199	R200
HEQ 14.5dB	ASM	NO_ASM
LLEQ 8.5dB	ASM	ASM
LEQ 11.5dB	NO_ASM	NO_ASM

	PC10 (INT PD)		PC20 (INT PD)	
	R201	R202	R205	R206
AUX interception DIS Output 800mV & 0dB	ASM	NO_ASM	ASM	NO_ASM
AUX interception DIS Output 400mV & 0dB	ASM	ASM	ASM	ASM
AUX interception EN	NO_ASM	NO_ASM	NO_ASM	NO_ASM

	PC11 (INT PD)		PC21 (INT PD)	
	R203	R204	R207	R208
Swing +20%	ASM	NO_ASM	ASM	NO_ASM
Swing -16.7%	ASM	ASM	ASM	ASM
Swing default	NO_ASM	NO_ASM	NO_ASM	NO_ASM

TABLE : Automatic Switching Mode (CFG0 = H)

SW	
L	Port 1 has higher priority when both ports are plugged
H	Port 2 has higher priority when both ports are plugged

PI1 (INT PD)	R524	R525
Auto test EN & Offset cancellation EN	ASM	NO_ASM
Auto test DIS & Offset cancellation DIS	ASM	ASM
Auto test DIS & Offset cancellation EN	NO_ASM	NO_ASM

PI0 (INT PD)	R209
Auto EQ DIS	ASM
Auto EQ EN	NO_ASM

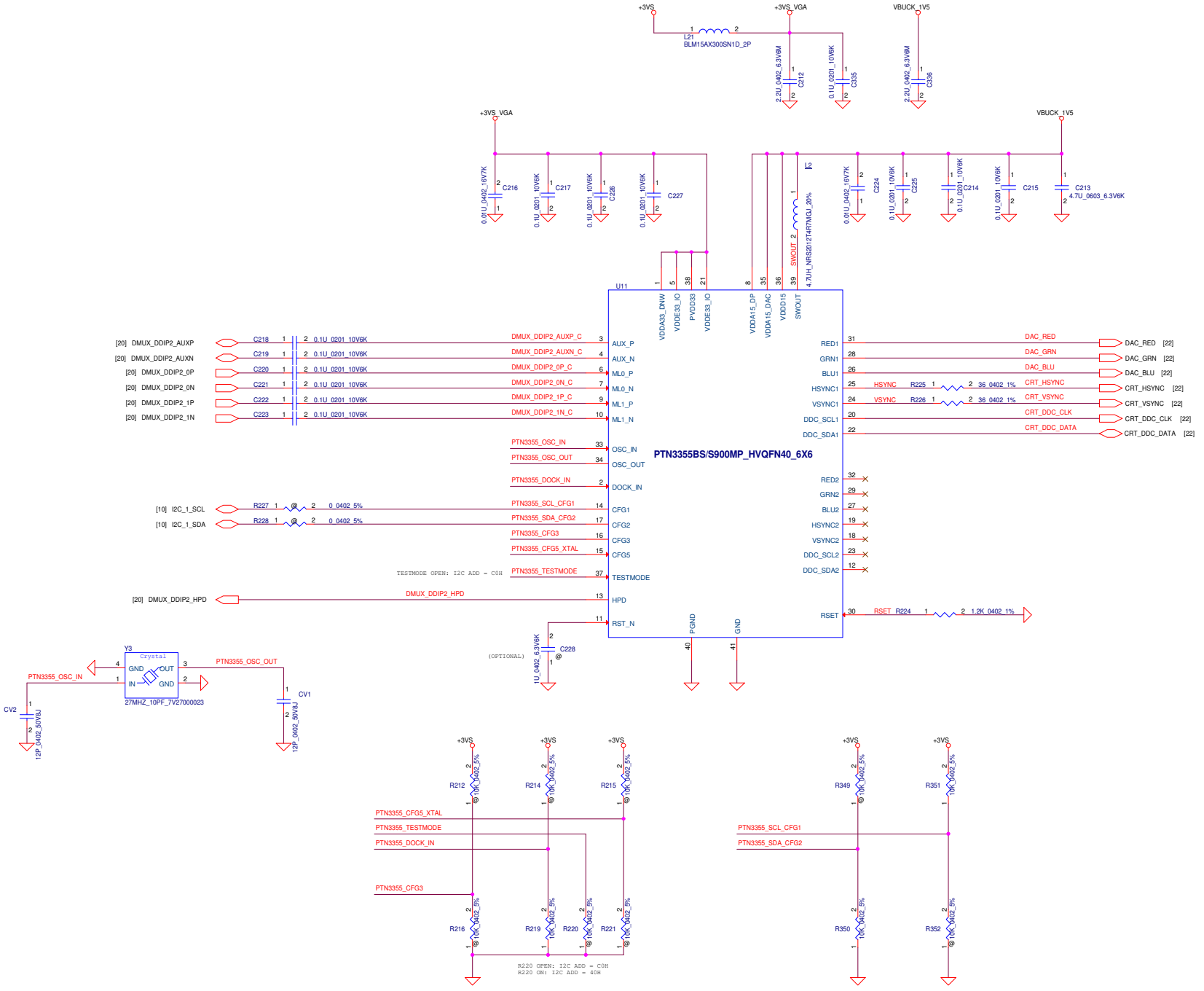
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: DP Mux_PS8338B

Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 20 of 58



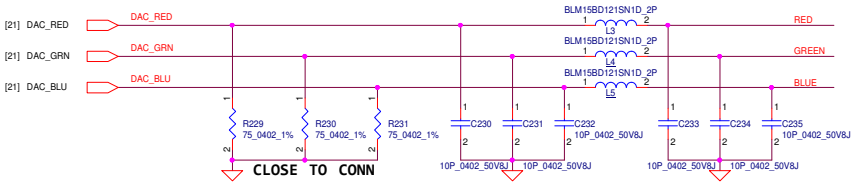
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

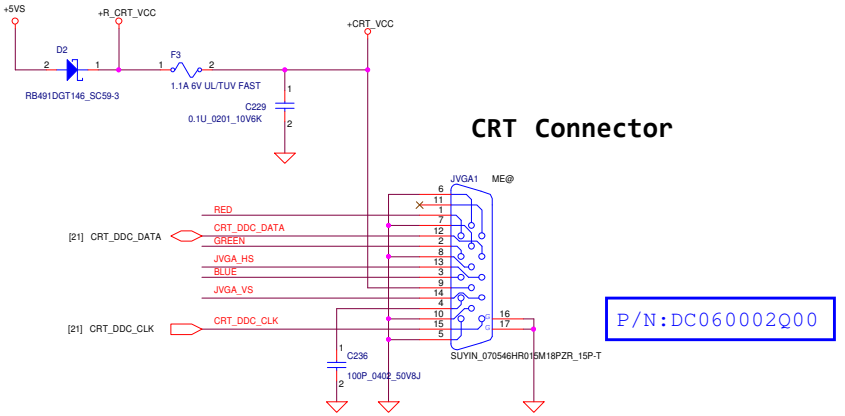
Compal Electronics, Inc.

Title: **DP to VGA_PTN3355**

Size	Document Number	Rev
C	LA-C422P	1.0

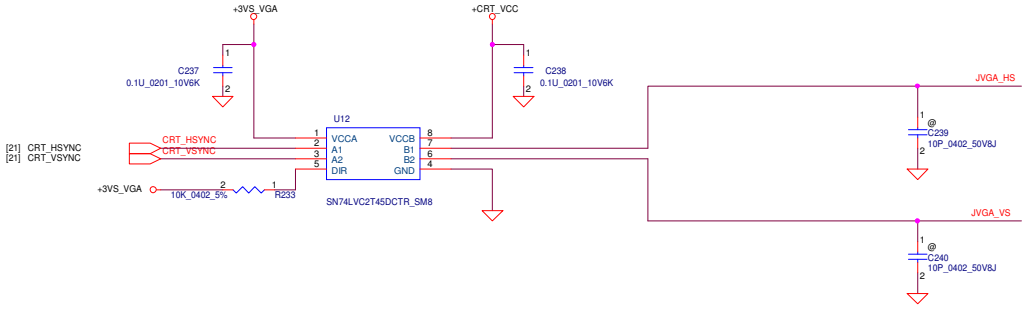
Date: Tuesday, November 15, 2016 | Sheet 21 of 58

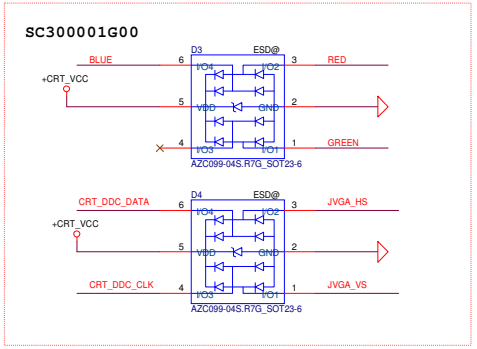


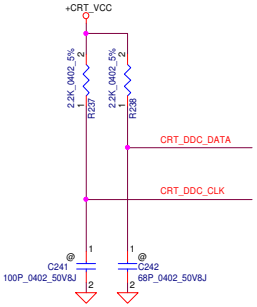


CRT Connector

P/N:DC060002Q00







Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **VGA CONN**

Size	Document Number	Rev
C	LA-C422P	1.0

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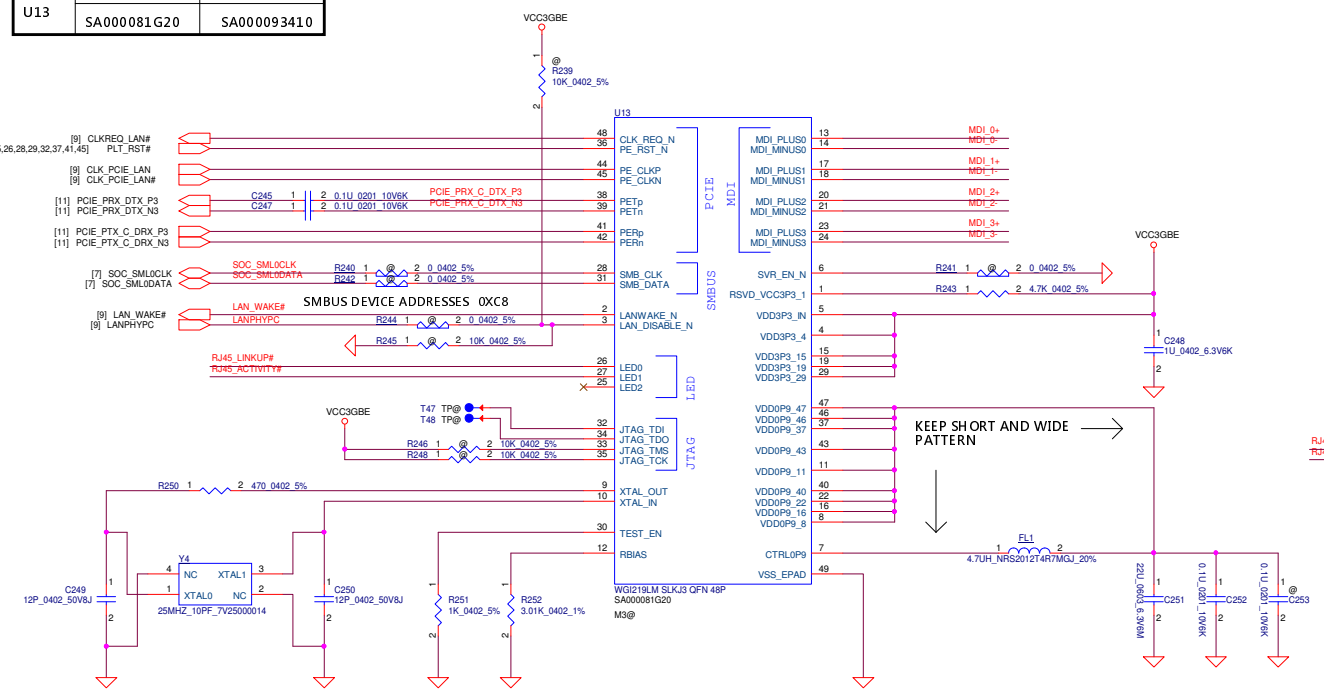
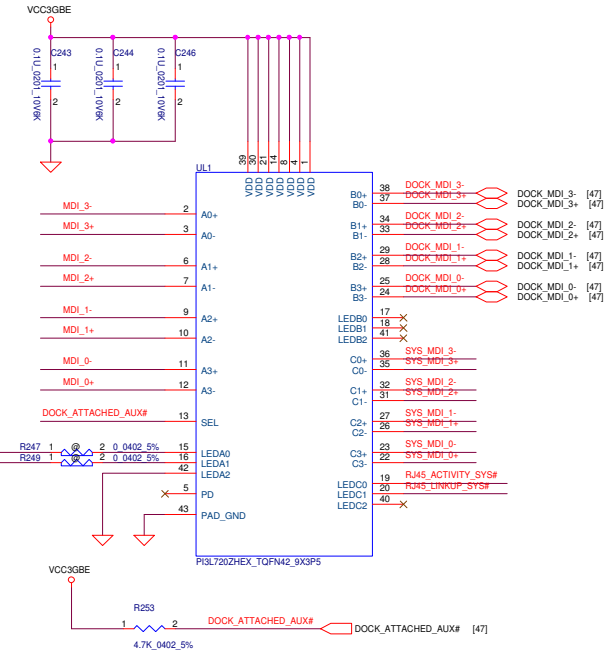
LAN SWITCH

TABLE

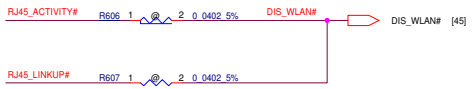
vPRO	Yes	No
U13	Jacksonville-LM	Jacksonville-V
	SA000081G20	SA000093410

The PHY SMBus address is 0xC8
and default MAC SMBus address is 0xE0.





PD (internal PD)	SEL	Function
L	L	Ax to Bx (Docking)
L	H	Ax to Cx (Sys)
H	X	Hi-Z



To Sub Board

SYS_MDI_3- SYS_MDI_3- [42]
SYS_MDI_3+ SYS_MDI_3+ [42]
SYS_MDI_2- SYS_MDI_2- [42]
SYS_MDI_2+ SYS_MDI_2+ [42]
SYS_MDI_1- SYS_MDI_1- [42]
SYS_MDI_1+ SYS_MDI_1+ [42]
SYS_MDI_0- SYS_MDI_0- [42]
SYS_MDI_0+ SYS_MDI_0+ [42]
RJ45_ACTIVITY_SYS# RJ45_ACTIVITY_SYS# [42]
RJ45_LINKUP_SYS# RJ45_LINKUP_SYS# [42]

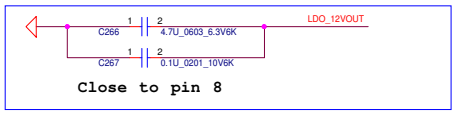
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

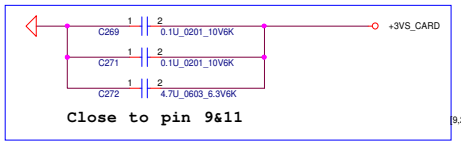
Compal Electronics, Inc.

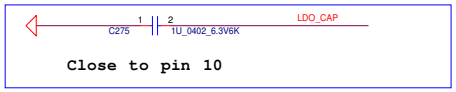
Title: **Intel GBE_JACKSONVILLE-LM**

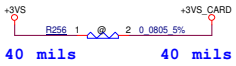
Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 23 of 58

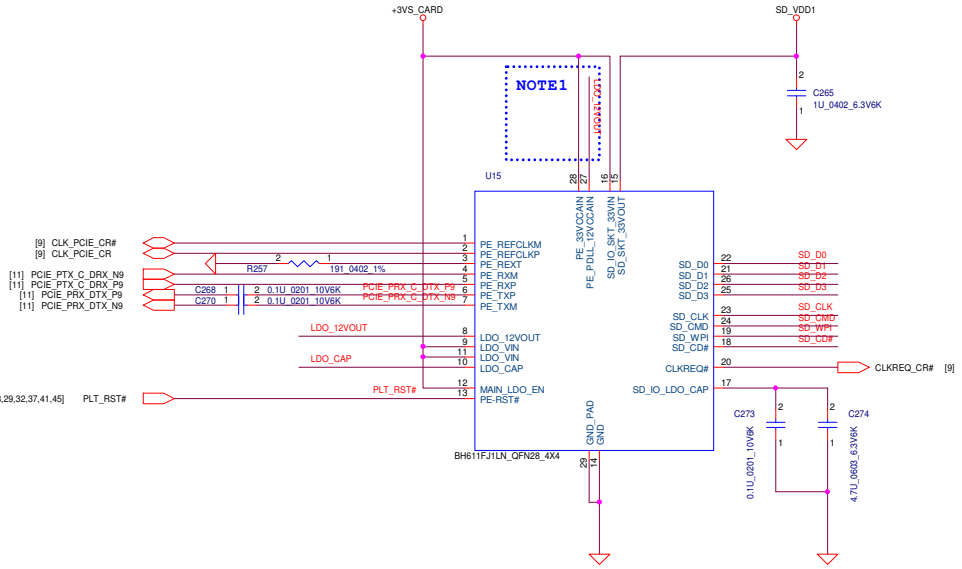


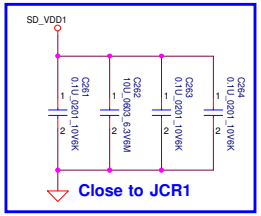


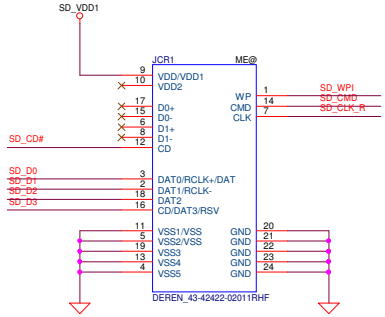




NOTE1
CONNECT THE POWER PIN WITH WIRE MORE THAN 50MIL, THE CAPACITOR SHOULD BE PLACED ON THE WIRE.



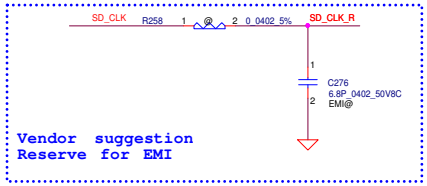




Normal open type

CIRCUIT DIAGRAM FOR CARD SWITCH

	W/P CONTACT		C/D CONTACT
	WRITE PROTECT POSITION	WRITE ENABLE POSITION	
CARD UNINSERTION	OPEN	OPEN	OPEN
CARD HALF INSERTION	CLOSE	CLOSE	OPEN
CARD INSERTION	OPEN	CLOSE	CLOSE



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.	
Title	Card Reader_BH611FJ1LN
Size C	Document Number LA-C422P
Rev	1.0
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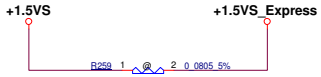
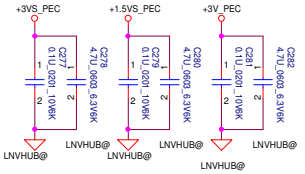
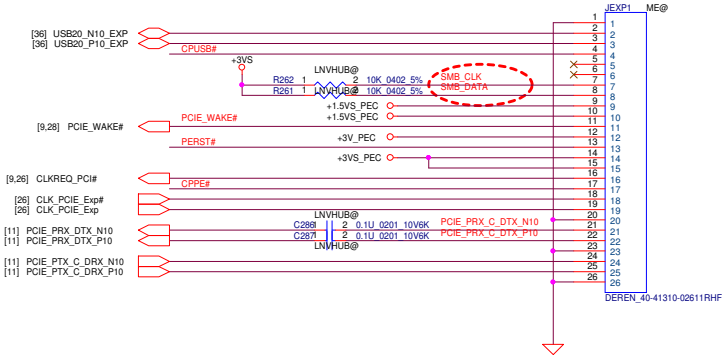
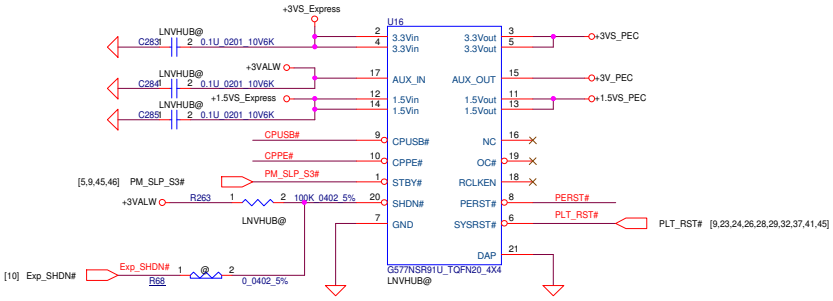
Express Card Slot









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Title	Express Card (L)		
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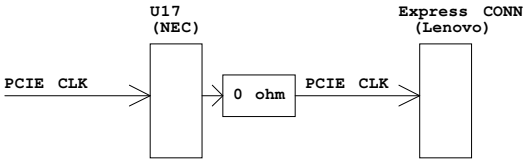

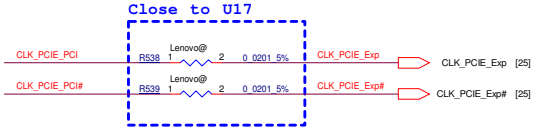

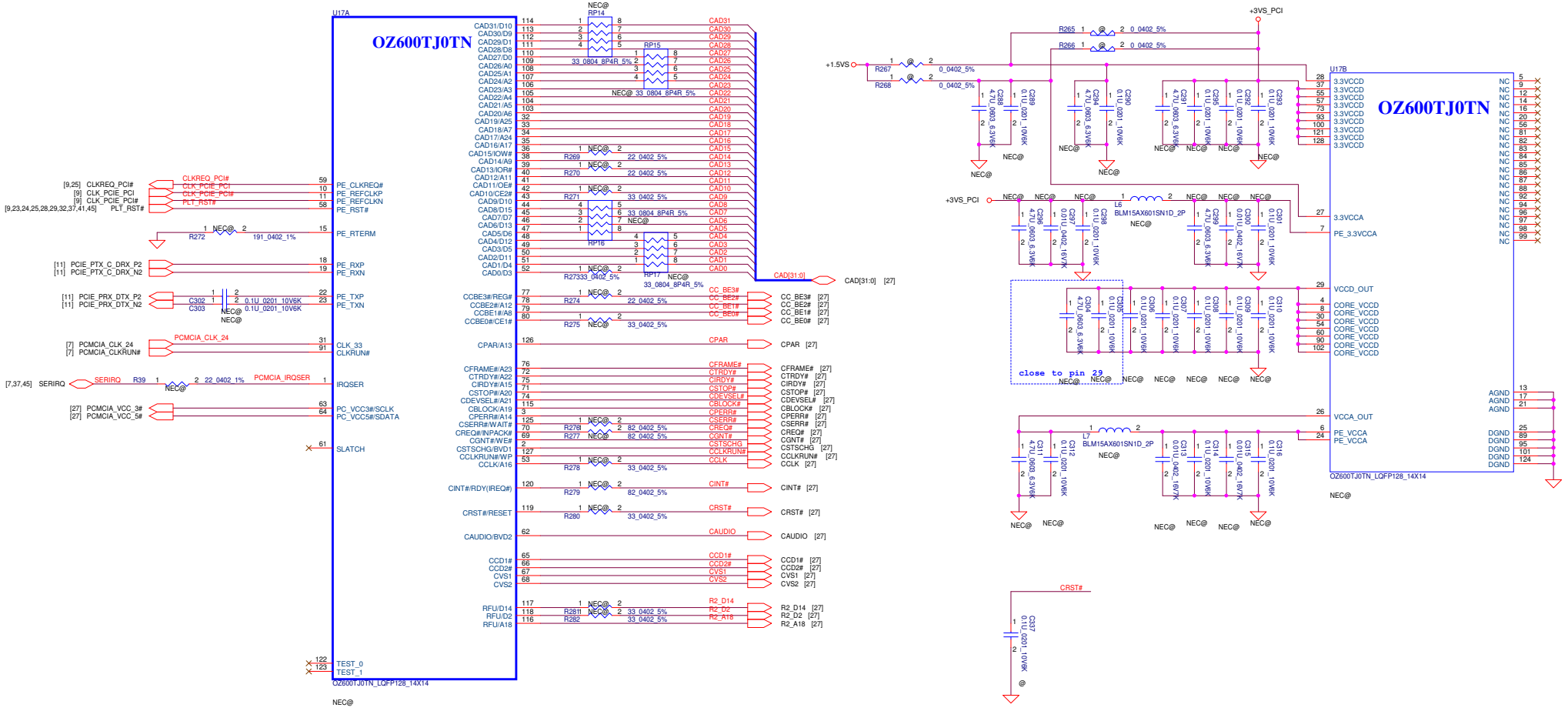

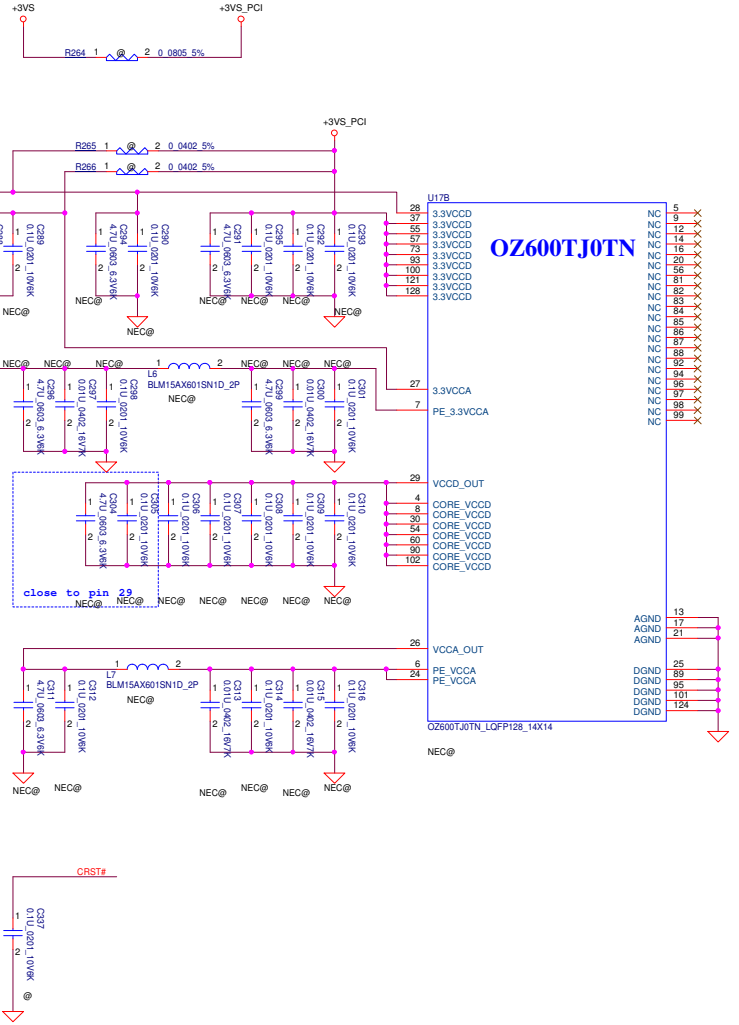

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Issued Date	2016/03/21	Deciphered Date	2017/03/01

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Title	PCI Bridge (N)
Size	C
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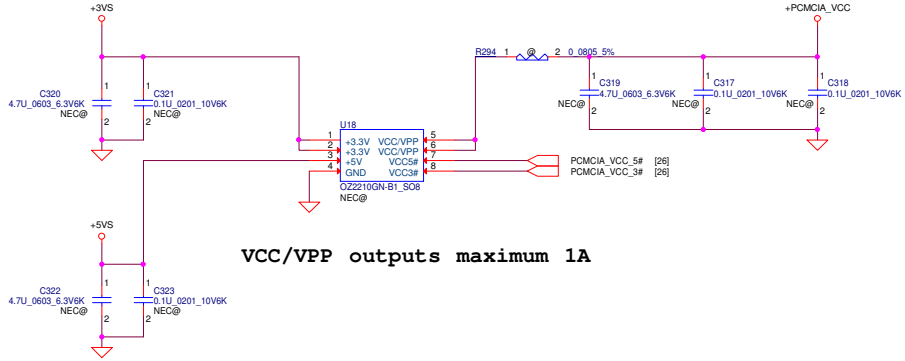

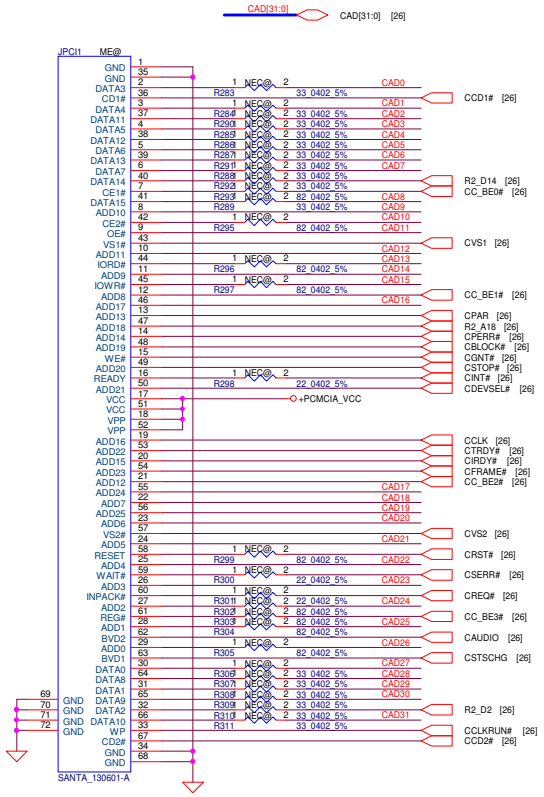

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Title	PCMCIA CONN (N)		
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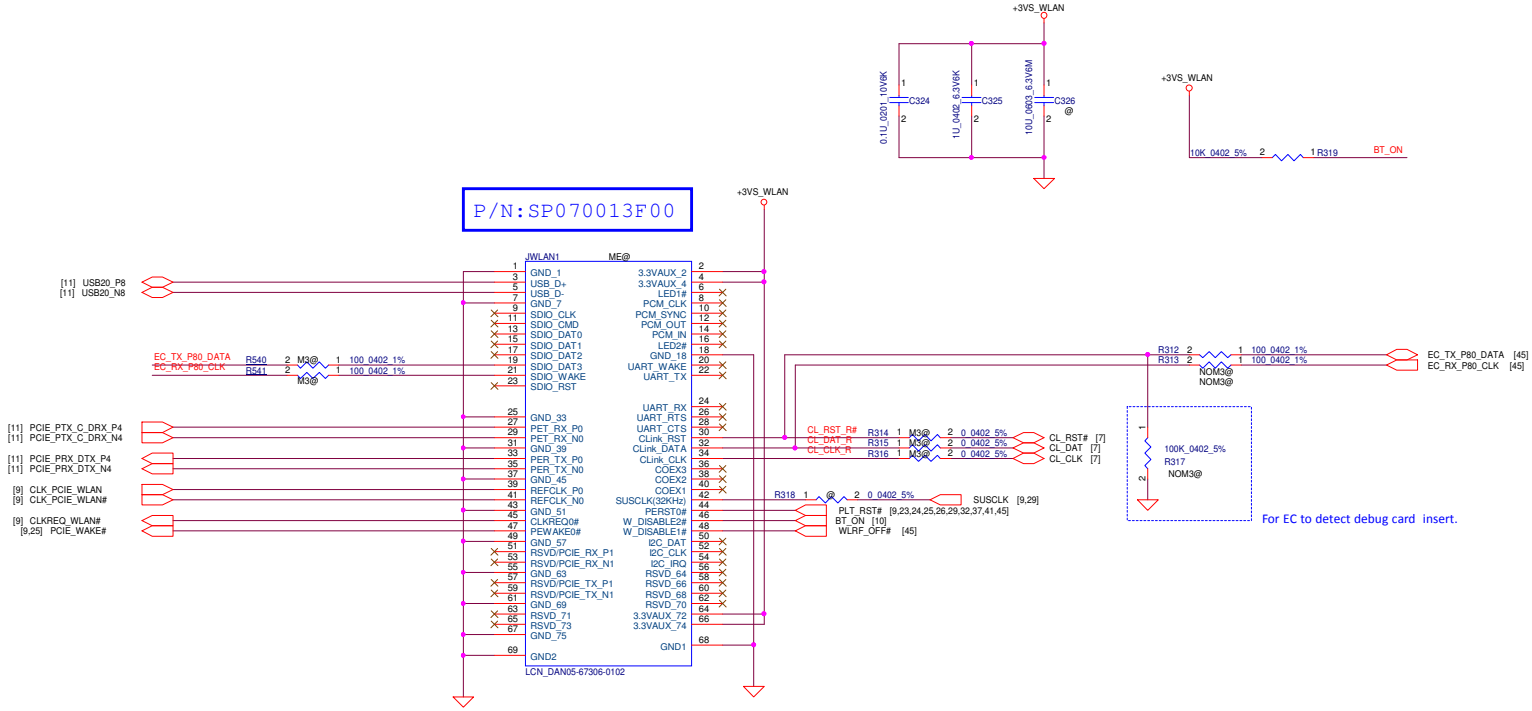
M.2 WLAN/BT



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **WLAN/BT**

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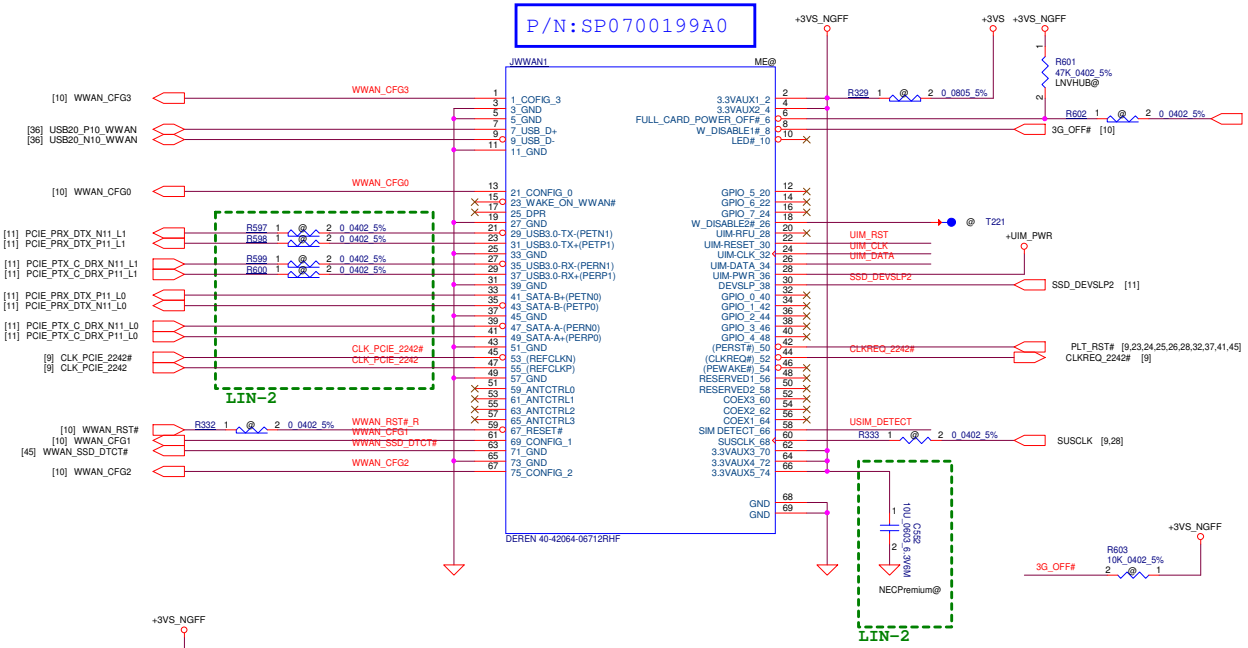
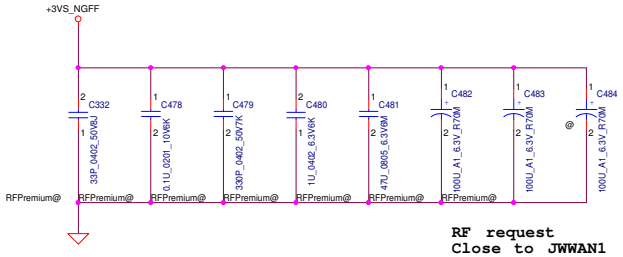
M.2 WWAN LTE

P/N:SP0700199A0





RF request
Close to JWWAN1

CFG0	CFG3	CACHE_DTCT (OE)	CFG1	WWAN_PE_DTCT# (B)
0	0	1 SSD	1	0 PCIE
			0	1 SATA
0	1	0 WWAN	X	NA
1	0			
1	1	0 NA		

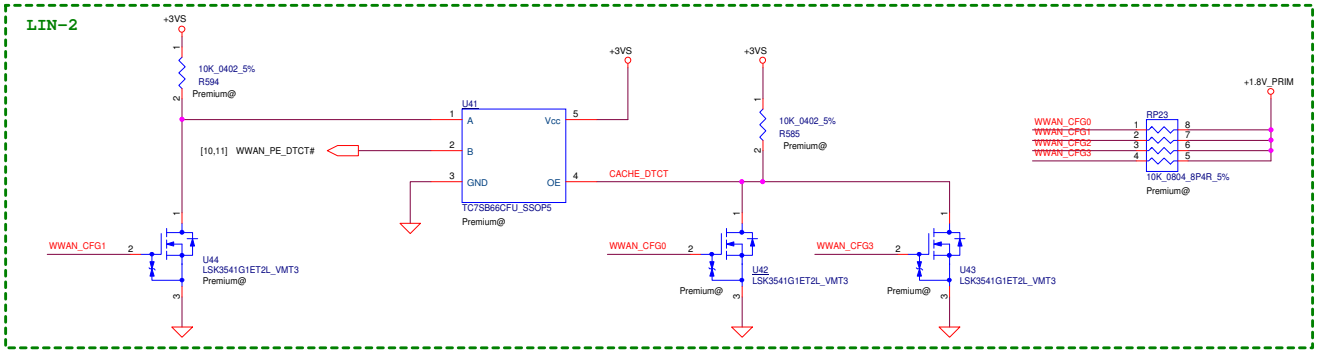
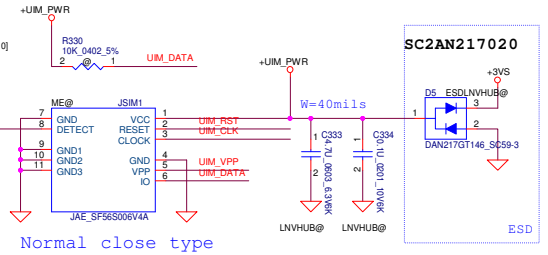
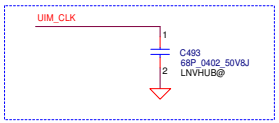


TABLE.1 CIRCUIT

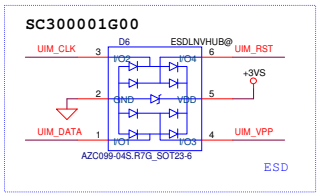
	WITHOUT CARD	CARD MATED
DETECTION SWITCH	④ ⑤ GND	④ ⑤ GND



Normal close type



Close to JSIM1 to avoid UIM_CLK over/under shoot



M.2 Revision 0.7a ,Version 1.0

M.2 Socket 2 Pin out	Config_0 (pin 21)	Config_3 (pin 1)	Config_2 (pin 75)	Config_1 (pin 69)
SATA	L	L	L	L
PCIE	L	L	L	NC
WWAN-USB	L	NC	States 4, 5, 6, 7	
WWAN-SSIC	NC	L	States 8, 9, 10, 11	

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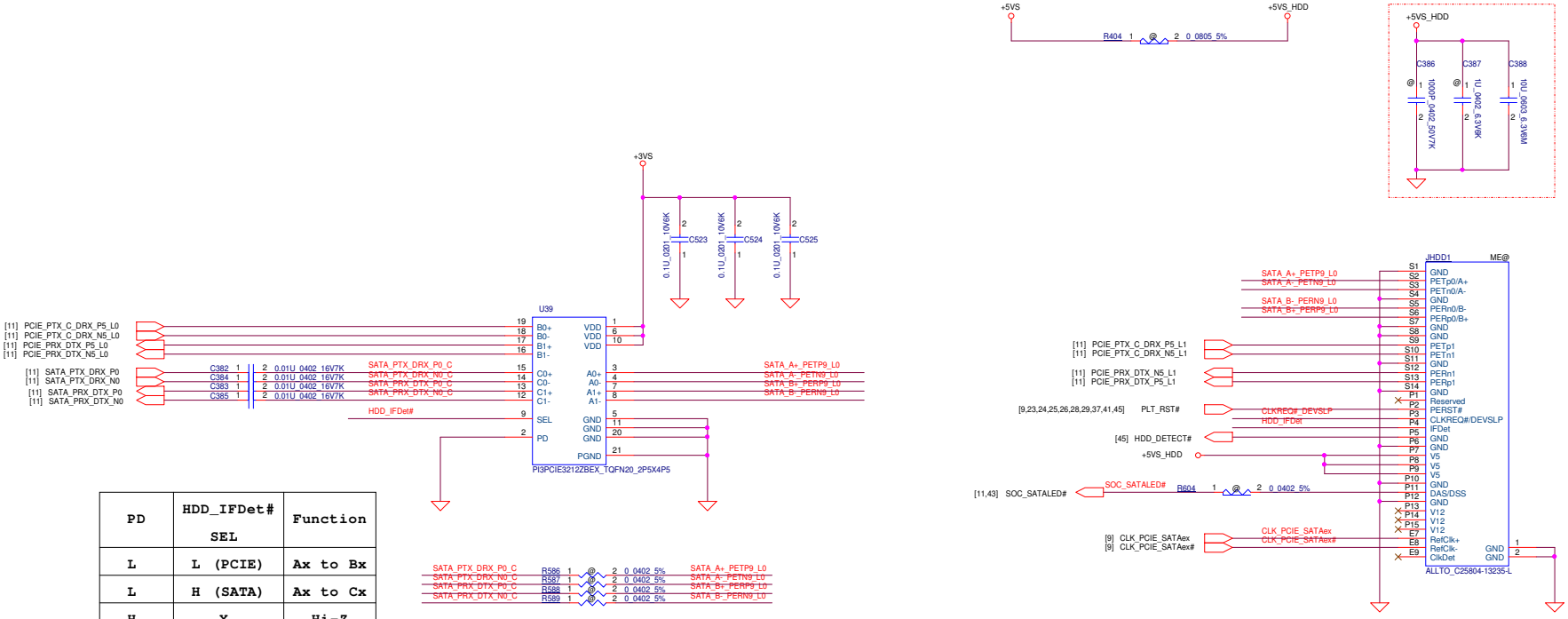
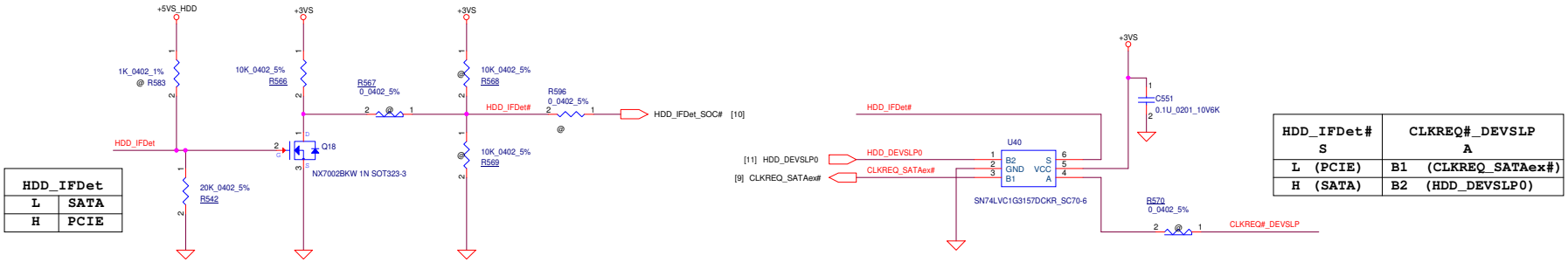
HDD CONN

LIN-2



PD	HDD_IFDet# SEL	Function
L	L (PCIE)	Ax to Bx
L	H (SATA)	Ax to Cx
H	X	Hi-Z



HDD_IFDet#S	CLKREQ#_DEVSLPA
L (PCIE)	B1 (CLKREQ_SATAex#)
H (SATA)	B2 (HDD_DEVSLP0)

Compal Electronics, Inc.

Title: BLANK

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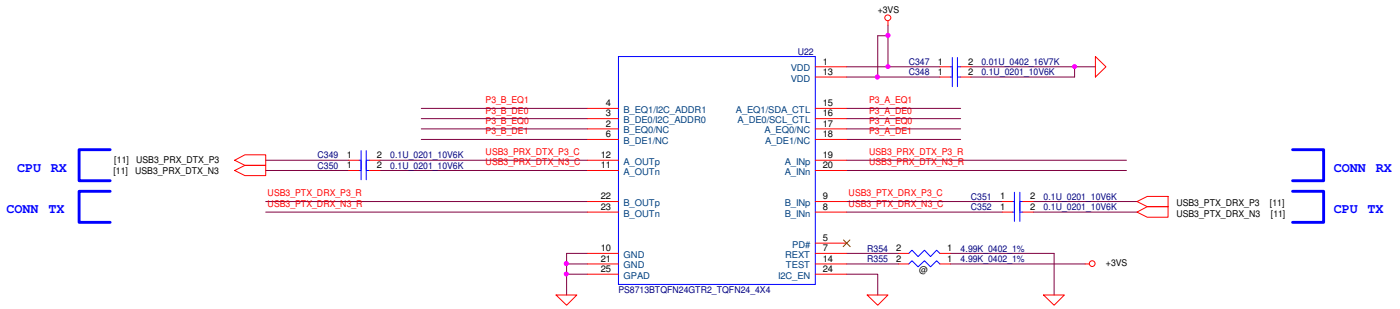
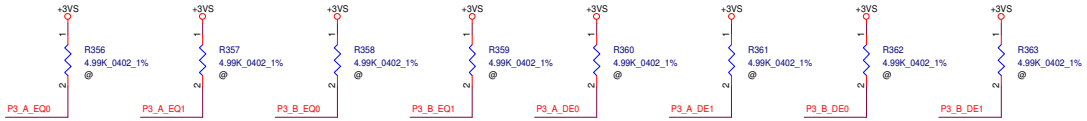
USB3 (Right-2)





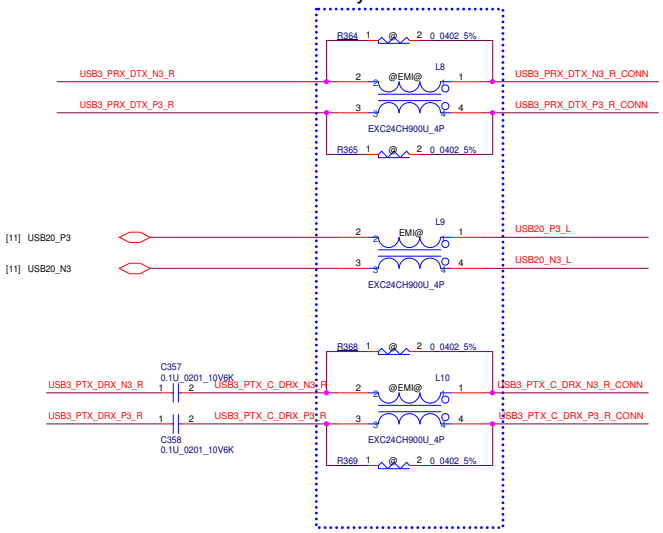
PIN13

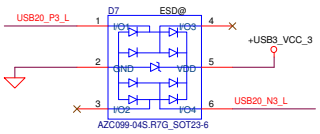
	A_EQ1/B_EQ1 (Internal pull Low)	A_EQ0/B_EQ0 (Internal pull Low)
reserved	Low	Low
program EQ for channel loss up to 7dB	Low	High
program EQ for channel loss up to 14.5dB	High	Low
program EQ for channel loss up to 11.5dB	High	High

	A_DE1/B_DE1 (Internal pull Low)	A_DE0/B_DE0 (Internal pull Low)
3.5dB de-emphasis	Low	Low
No de-emphasis	Low	High
2.7dB de-emphasis	High	Low
5dB with boost output swing	High	High

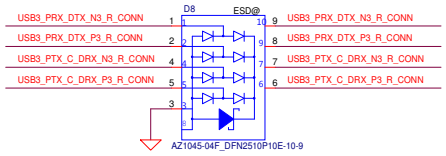
	TEST (Internal pull Low)
Normal operation (default)	Low
Test mode enable	High

PN: SM070004300 x 3
Co-lay with 0 ohm





SC300001G00



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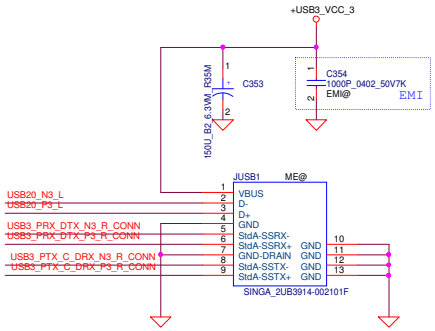

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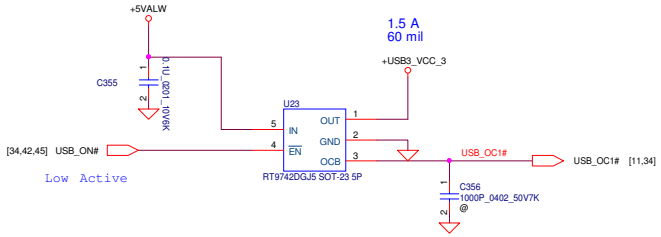

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Compal Electronics, Inc.

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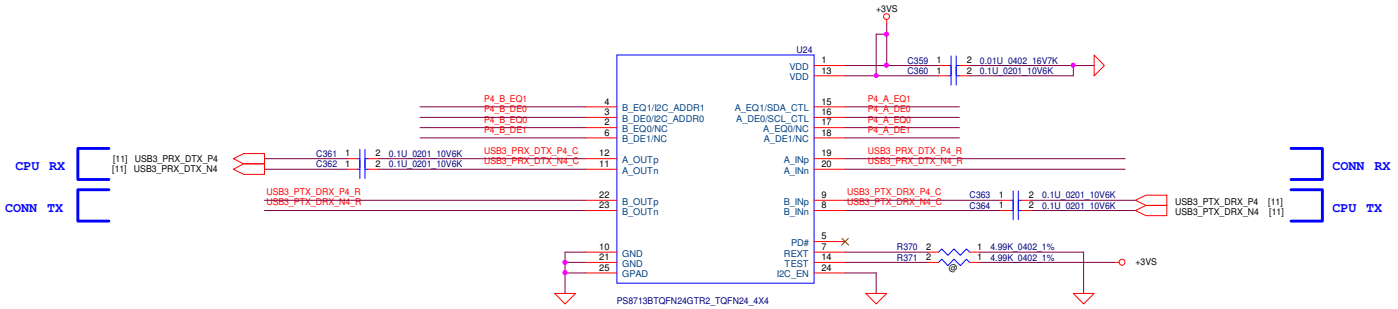
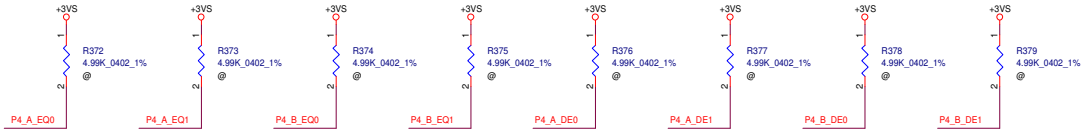
USB3 (Right-3)





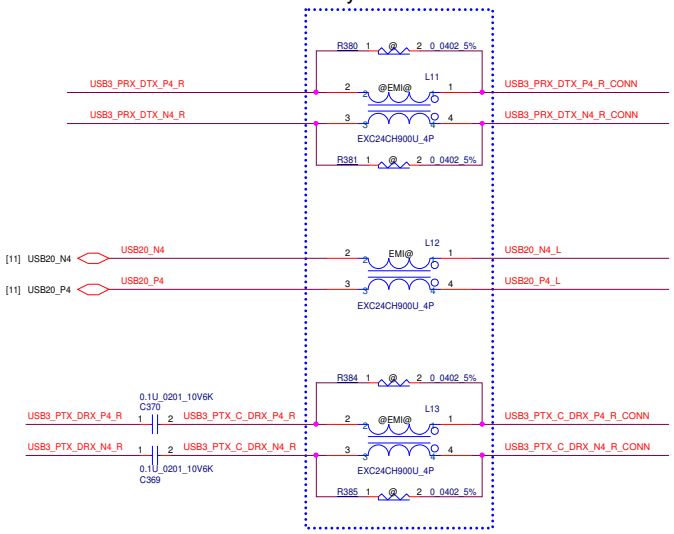
PIN13

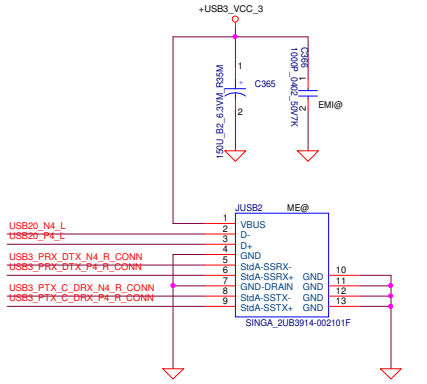
	A_EQ1/B_EQ1 (Internal pull Low)	A_EQ0/B_EQ0 (Internal pull Low)
reserved	Low	Low
program EQ for channel loss up to 7dB	Low	High
program EQ for channel loss up to 14.5dB	High	Low
program EQ for channel loss up to 11.5dB	High	High

	A_DE1/B_DE1 (Internal pull Low)	A_DE0/B_DE0 (Internal pull Low)
3.5dB de-emphasis	Low	Low
No de-emphasis	Low	High
2.7dB de-emphasis	High	Low
5dB with boost output swing	High	High

	TEST (Internal pull Low)
Normal operation (default)	Low
Test mode enable	High

PN: SM070004300 x 3
Co-lay with 0 ohm





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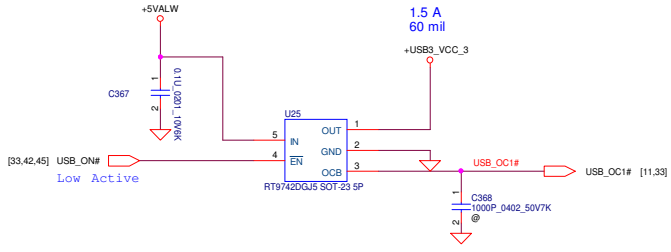

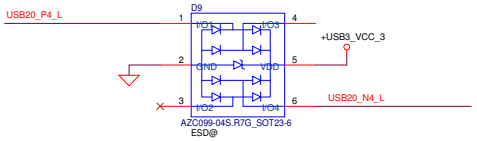

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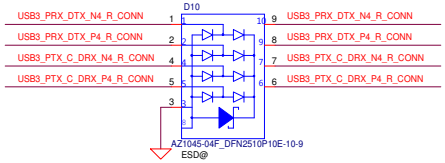

SC300001Y00

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Title: **USB 3.0 Redriver/Right**

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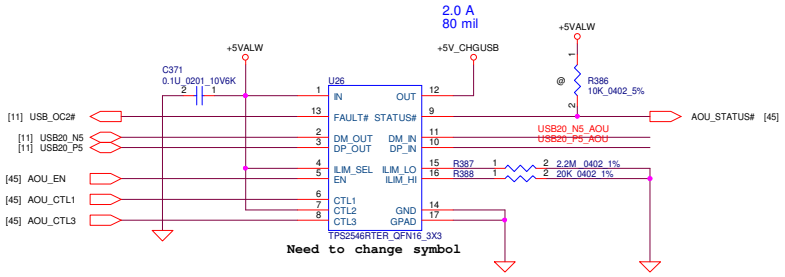
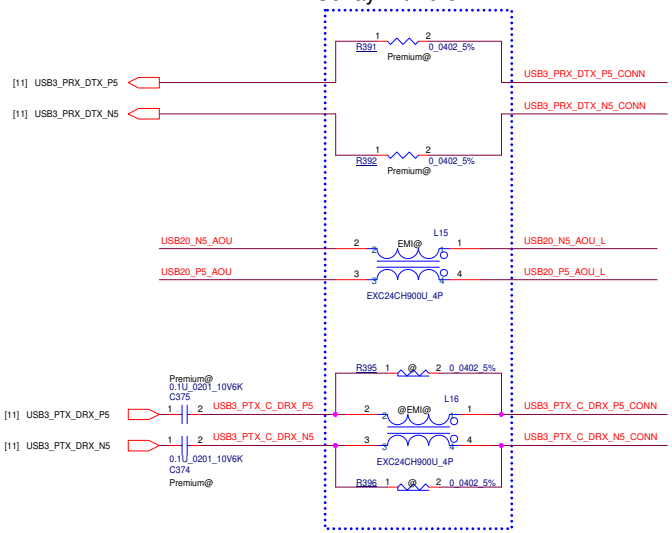
USB3 (Left) / AOU

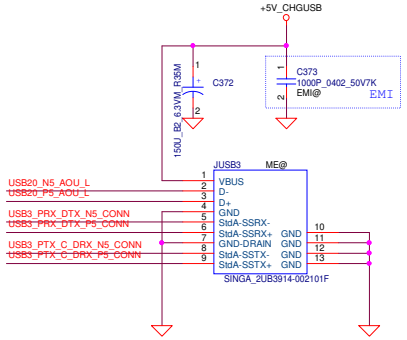


				AOU_EN	CTL1	CTL2	CTL3	ILIM_SEL
AOU : eanble/ Charge in off mode : disable	S0	AC/DC	CDP	1	1	1	1	1
	S3	AC/DC	DCP	1	0	1	1	1
	S4/S5	AC	DCP	1	0	1	1	1
	S4/S5	DC	OFF	0	0*	1*	1*	1*
AOU : eanble/ Charge In off mode : enable	S0	AC/DC	CDP	1	1	1	1	1
	S3	AC/DC	DCP	1	0	1	1	1
	S4/S5	AC	DCP	1	0	1	1	1
	S4/S5	DC	DCP	1	0	1	1	1
AOU : disable/ Charge in off mode : disable	S0	AC/DC	SDP	1	1*	1	0	1
	S3	AC/DC	SDP	1	1*	1	0	1
	S4/S5	AC	OFF	0	0*	1*	0*	1*
	S4/S5	DC	OFF	0	0*	0*	0*	0*

* Don't care

PN: SM070004300 x 3
Co-lay with 0 ohm





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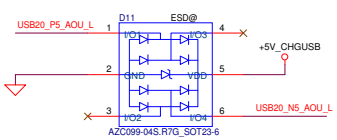

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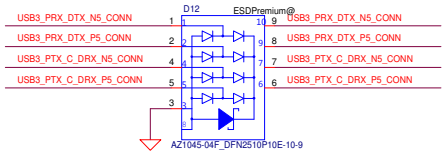

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Compal Electronics, Inc.

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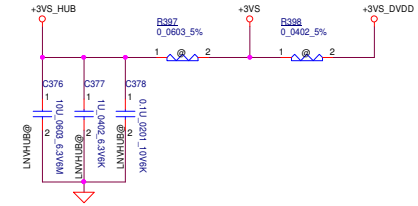
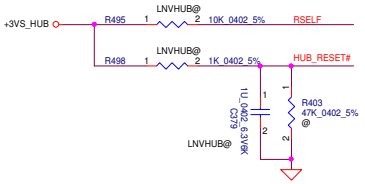
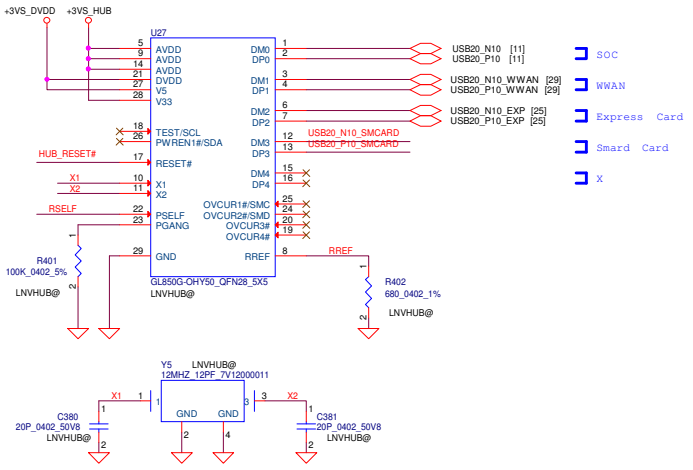
USB20 HUB

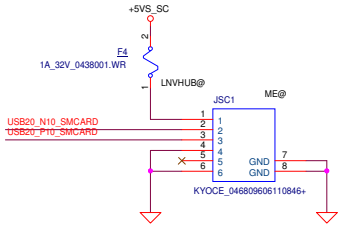




Pin 18 TEST:
0 : Switch mode.
1 : Chip will be put in test mode.
NC : Normal hub operation.



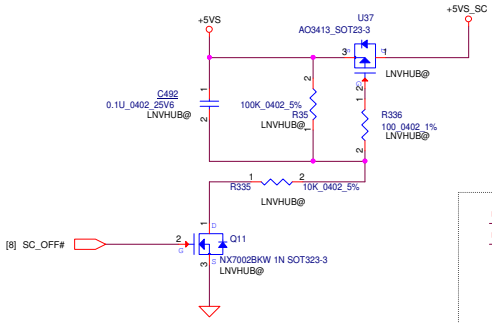
Smart Card

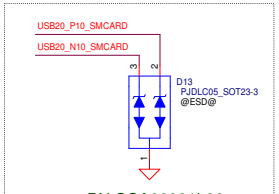


Smart Card define

NO	Signal
1	VCC (5V)
2	D-
3	D+
4	GND
5	N.C.
6	GND

0.1 A
20 mil





PN:SCA00001L00
ESD

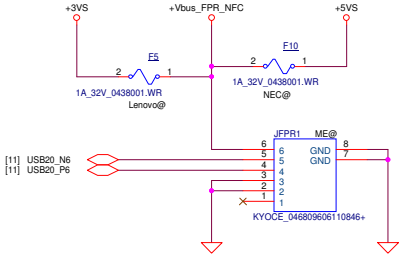
FPR/NFC USB I/F

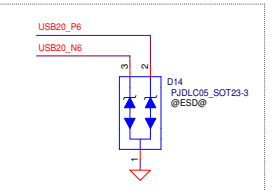
NFC (Felica)

NO	Signal
1	Vbus
2	D-
3	D+
4	GND
5	NC
6	NC

FPR pin define

NO	Signal
1	VCC3
2	D-
3	D+
4	GND
5	GND
6	NC





PN:SCA00001L00
ESD

Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

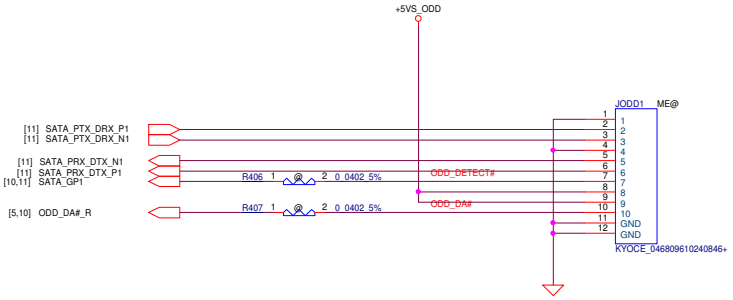
Compal Electronics, Inc.

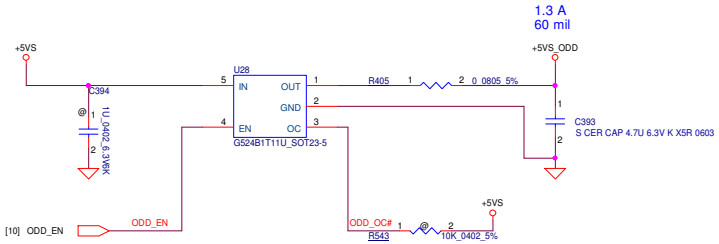
Title: **USB HUB/FPR/SmartCard (L)**

Size	Document Number	Rev
C	LA-C422P	1.0

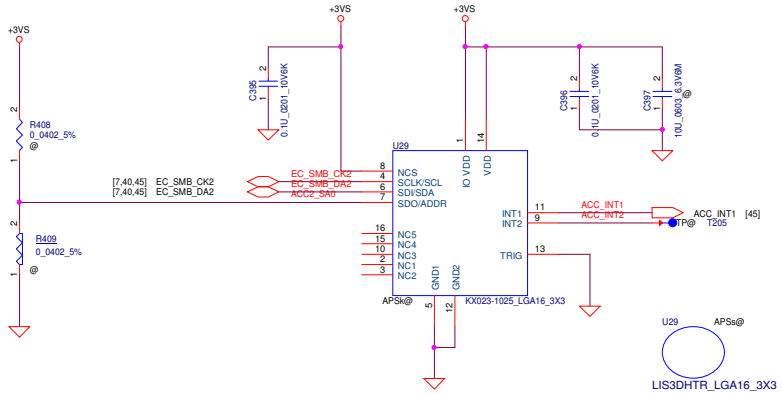
Date: Tuesday, November 15, 2016 | Sheet 36 of 58

ODD CONN





APS G-Sensor



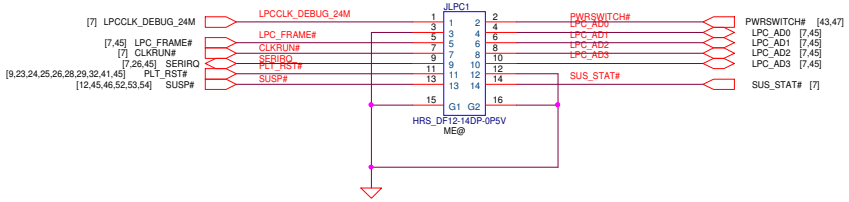
Kionix KX023-1025

SDO/ADDR	Address R/W
VDD	3Fh/3Eh
VSS	3Dh/3Ch

ST LIS3DHTR

SDO/ADDR	Address R/W
VDD	33h/32h
VSS	31h/30h

LPC Debug Port



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: ODD/APS/LPC Debug port

Size	Document Number	Rev
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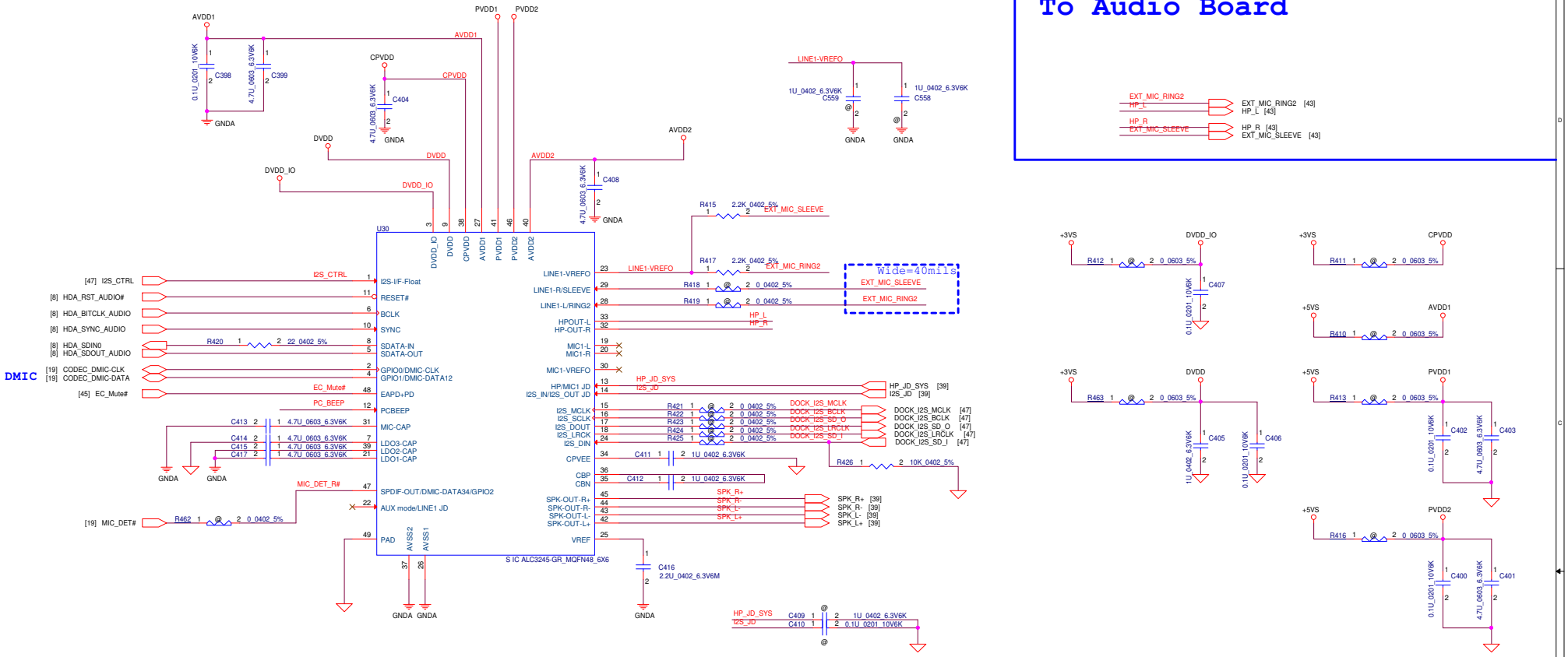
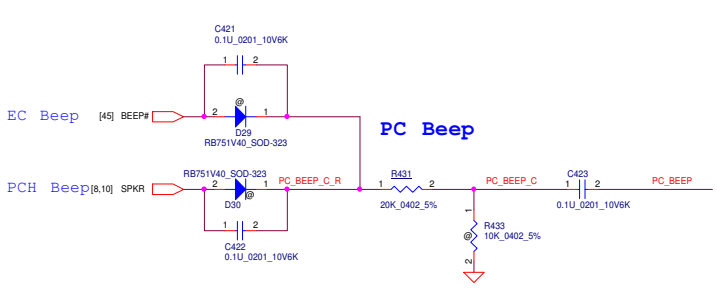
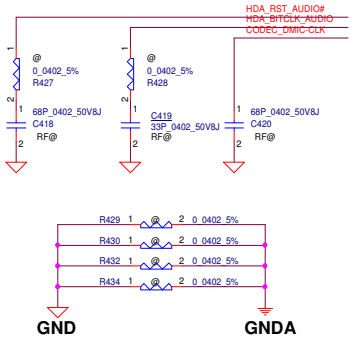
To Audio Board

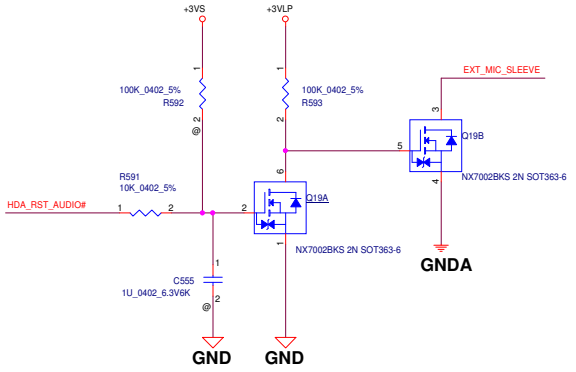
EXT_MIC_RING2 HP_L → EXT_MIC_RING2 [43] HP_L [43]

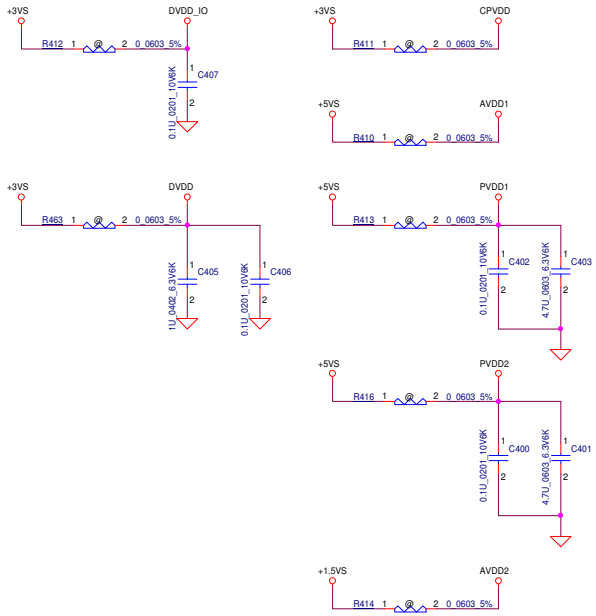
HP_R EXT_MIC_SLEEVE → HP_R [43] EXT_MIC_SLEEVE [43]











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Issued Date	2016/03/21	Deciphered Date	2017/03/01

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Title: Audio Codec-ALC3245

Size: C | Document Number: LA-C422P | Rev: 1.0

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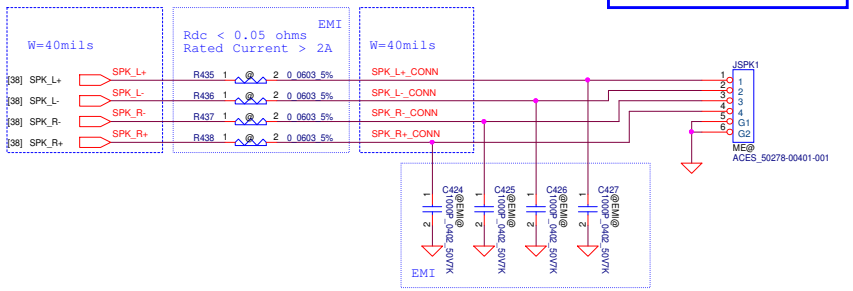
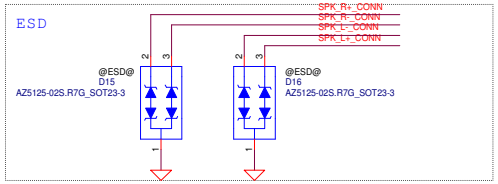
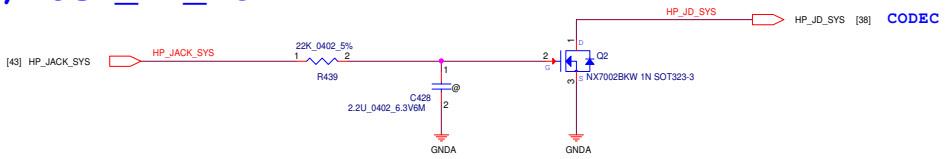
SPK CONN

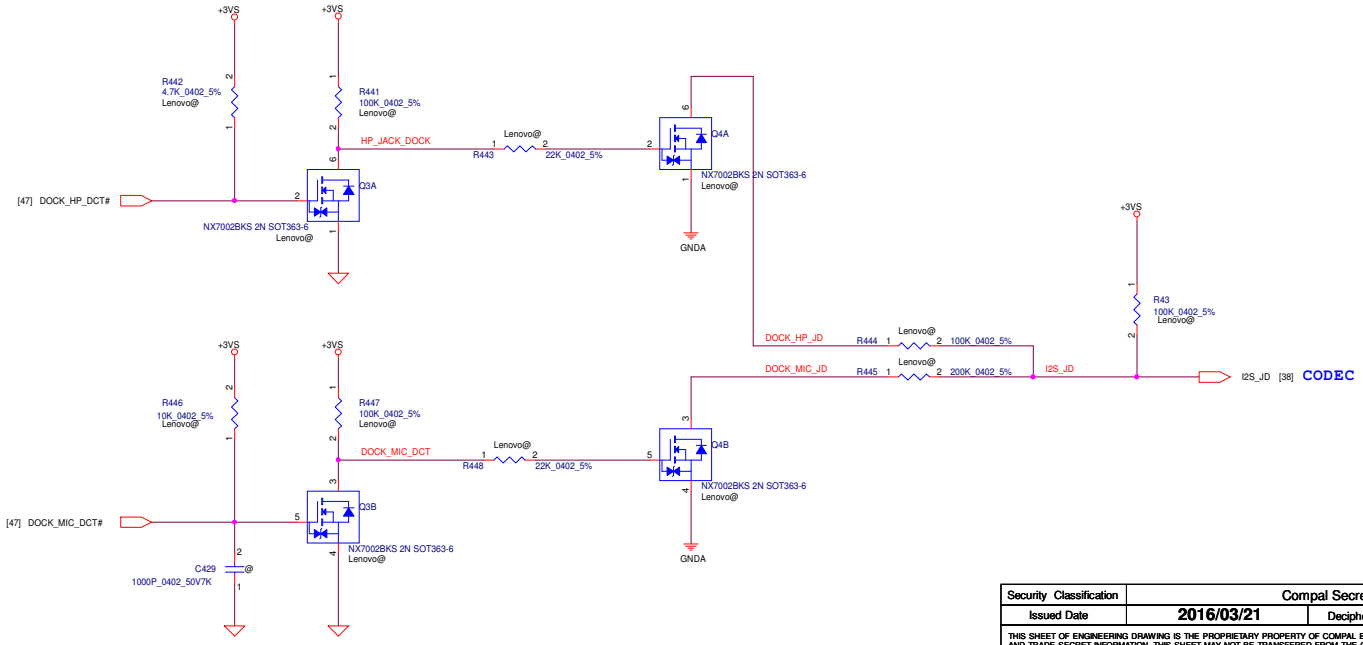
P/N:SP02000RR00





Sys/Dock_HP_DCT





Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **Audio SPK/HP_DCT**

Size	Document Number	Rev
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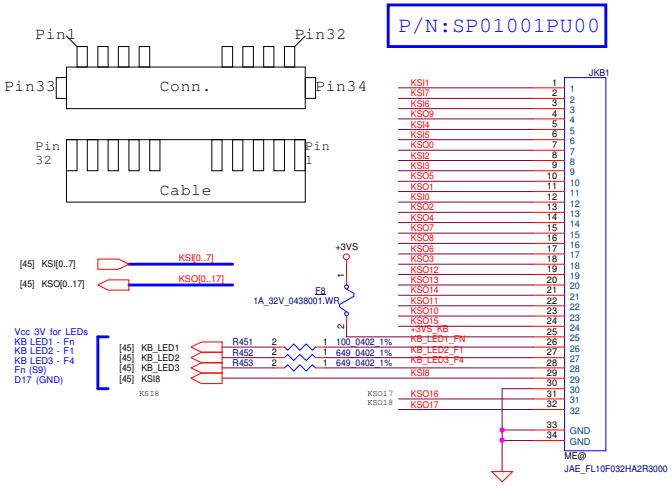
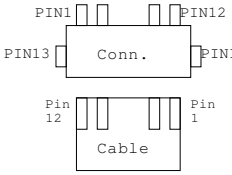
Int KB CONN

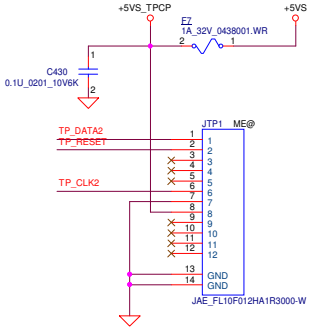
P/N:SP01001PU00

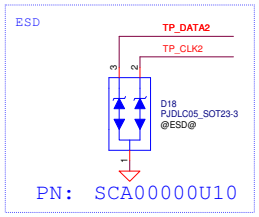


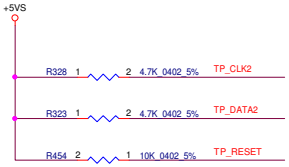
Track Point

P/N:SP01001RZ00





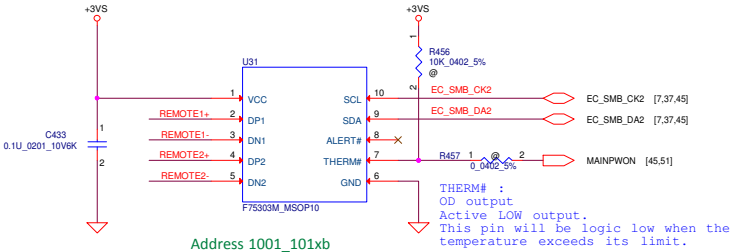




Track Point pin define

NO	Signal
1	IPD DATA
2	IPD RST
3	NC
4	NC
5	NC
6	IPD CLK
7	GND
8	VCC5
9	NC
10	NC
11	NC
12	NC

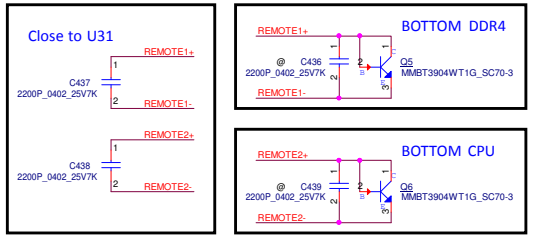
Fintek Thermal Sensor



THERM# :
OD output
Active LOW output.
This pin will be logic low when the temperature exceeds its limit.

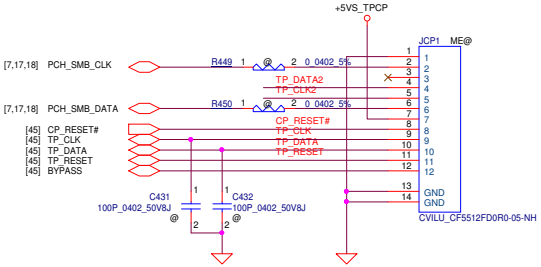
Address 1001_101xb
2nd source
SA000029210-->EMC1403-2-AIZL-TR

REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"



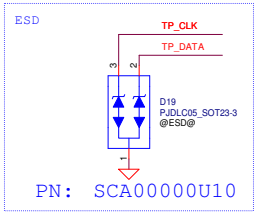
Click PAD

PN:SP01001Z200



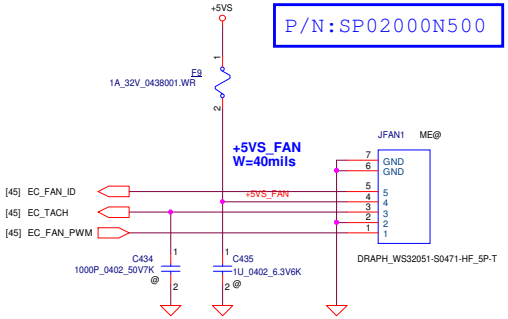
Click PAD pin define

NO	Signal
1	GND
2	SMB CLK
3	NC
4	DATA-TP
5	CLK-TP
6	SMB-DATA
7	VDD
8	RESET
9	CLK
10	DATA
11	TP4RST
12	BYPASS



FAN CONN

P/N:SP02000N500



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.			
Title	KB/TP/CP/Thermal/Fan		
Size	Document Number		Rev
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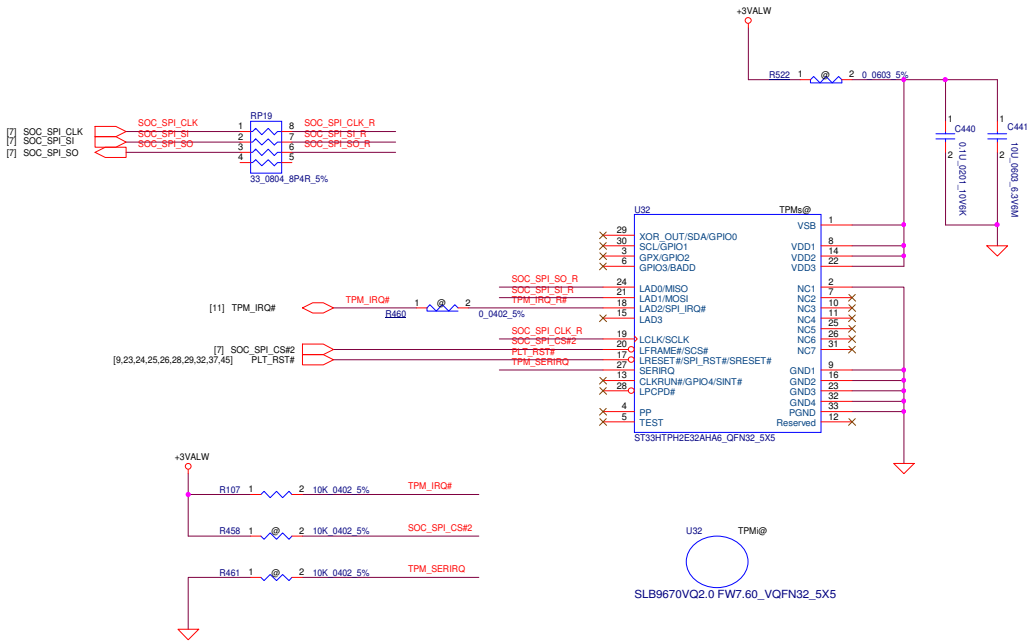
TPM



TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW7.60 SA00009N210	ST ST33HTPH2E32AHA6 SA00009SO10
1	VDD	VDD	NC
2	GND	GND	GND
3	GPIO	NC	NC
4	GPIO	NC	NC
5	NC	NC	NC
6	VNC/GPIO	GPIO	NC
7	GPIO/VDD	PP	PP
8	VDD	VDD	NC
9	GND	GND	NC
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	VNC/GPIO	NC	NC
14	VDD	NC	NC
15	NC	NC	NC
16	GND	NC	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#
19	SPI_CLK	SCLK	SCLK
20	SPI_CS#	CS#	SCS#
21	MOSI	MOSI	MOSI
22	VDD	VDD	VDD
23	GND	GND	GND
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	VNC/GPIO	NC	NC
30	VNC/GPIO	NC	NC
31	VNC	NC	NC
32	GND	GND	NC

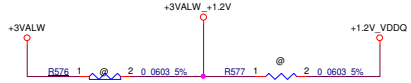
Compal Electronics, Inc.

Title: TPM

Size: C | Document Number: LA-C422P | Rev: 1.0

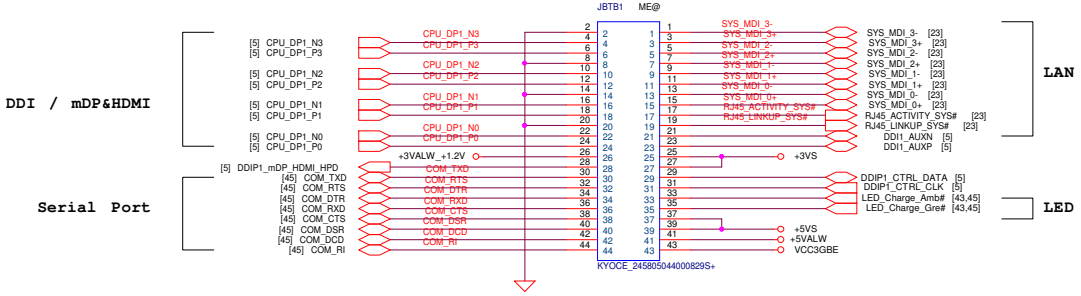
Date: Tuesday, November 15, 2016 | Sheet 41 of 58

Function Board

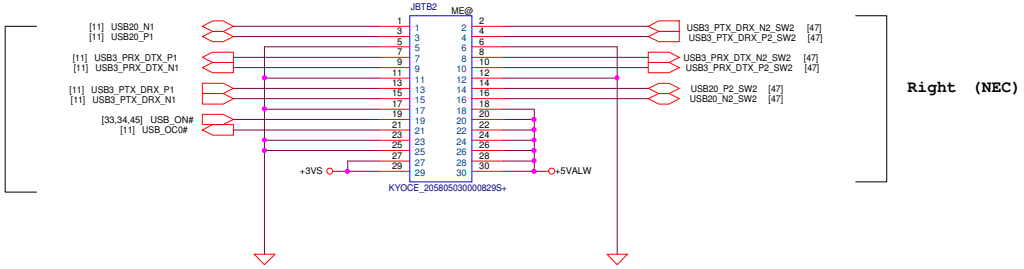


For Charge LED

Reserve For HDMI Redriver



USB Board



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **Sub Board_Function/USB**

Size	Document Number	Rev
C	LA-C422P	1.0

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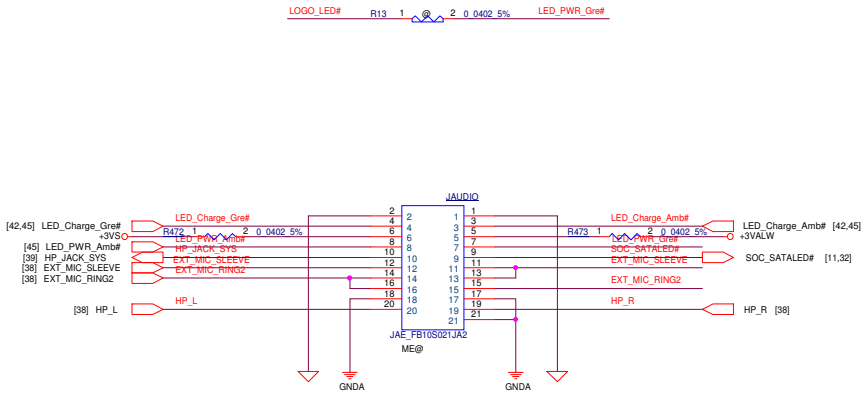
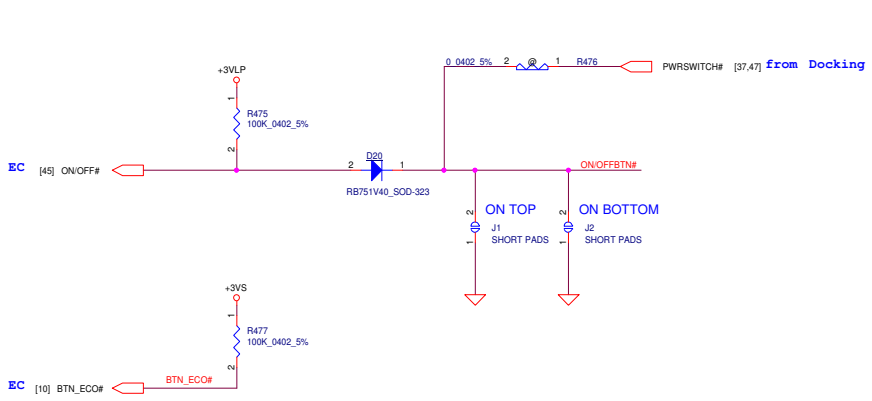
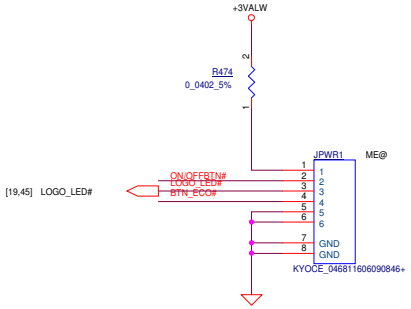
Audio Board



POWER BOARD





Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.			
Title: Sub Board_Audio/PWR			
Size: C	Document Number: LA-C422P		Rev: 1.0
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Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **BLANK**

Size	Document Number	Rev
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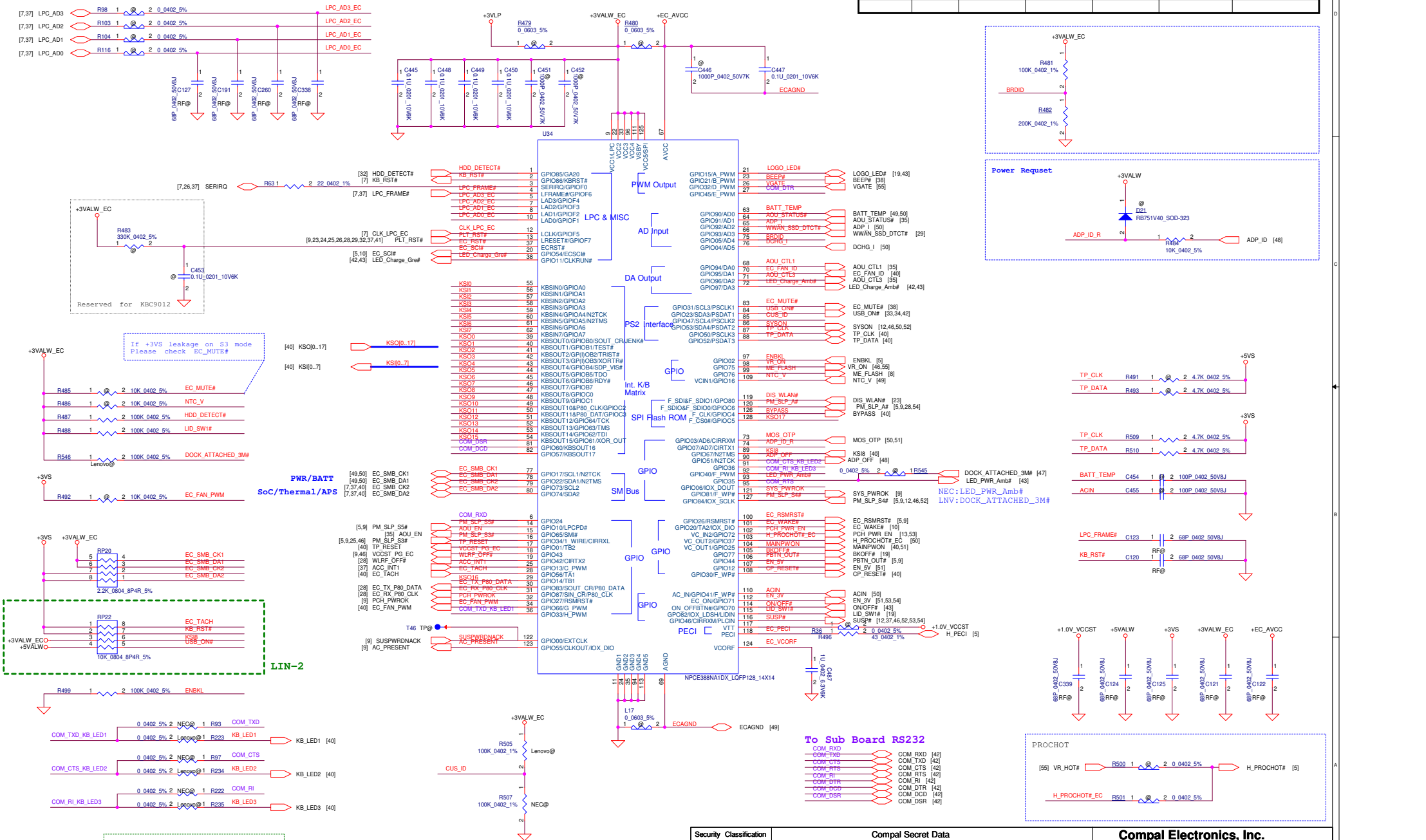
EC NPCE388N

Vcc	3.3V +/- 5%
R481	100K +/- 1%

PCB Ver.	Board ID	R482	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD
0.1	SDV	0K +/- 5%		0.000V	0.300V	0x00 - 0x0B
0.2	FVT	12K +/- 5%	0.347V	0.354V	0.360V	0x0C - 0x1C
0.3	SIT	15K +/- 5%	0.423V	0.430V	0.438V	0x1D - 0x26
1.0	SVT	200K +/- 1%	2.185V	2.200V	2.215V	0xA5 - 0xAF



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

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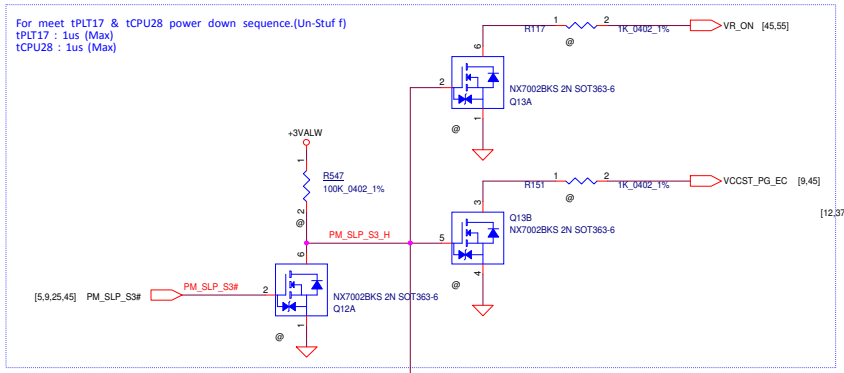
Compal Electronics, Inc.

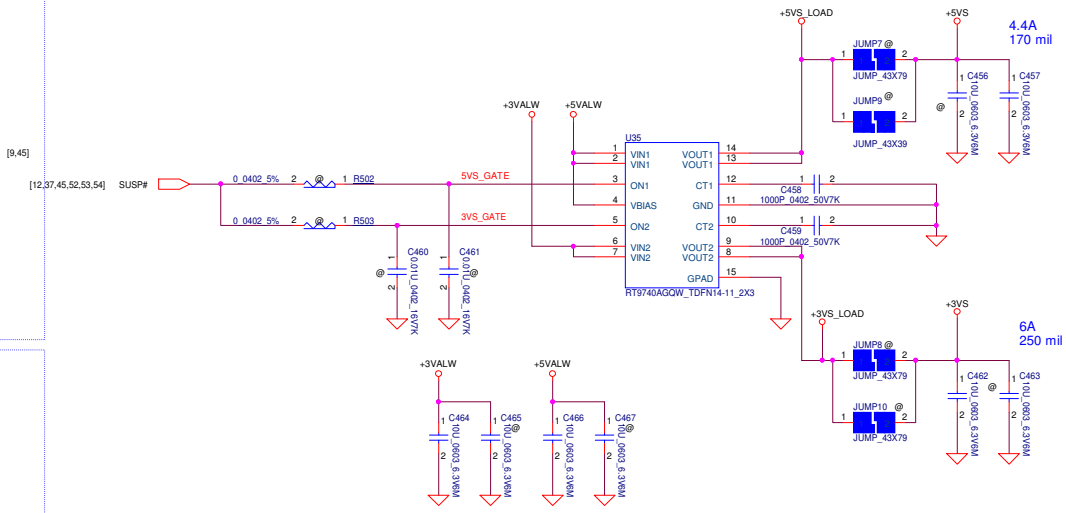
Title: EC_NPCE388N

Size: C | Document Number: LA-C422P | Rev: 1.0

Date: Tuesday, November 15, 2016 | Sheet 45 of 58

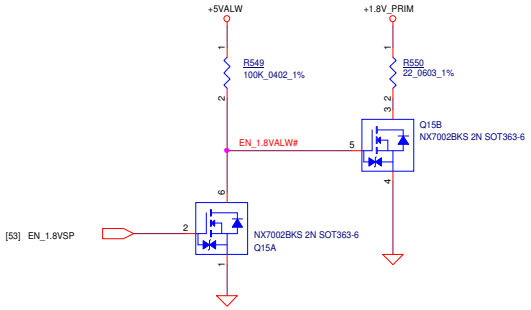


+5VALW TO +5VS



+3VALW TO +3VS

For +1.8V_PRIM Discharge



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

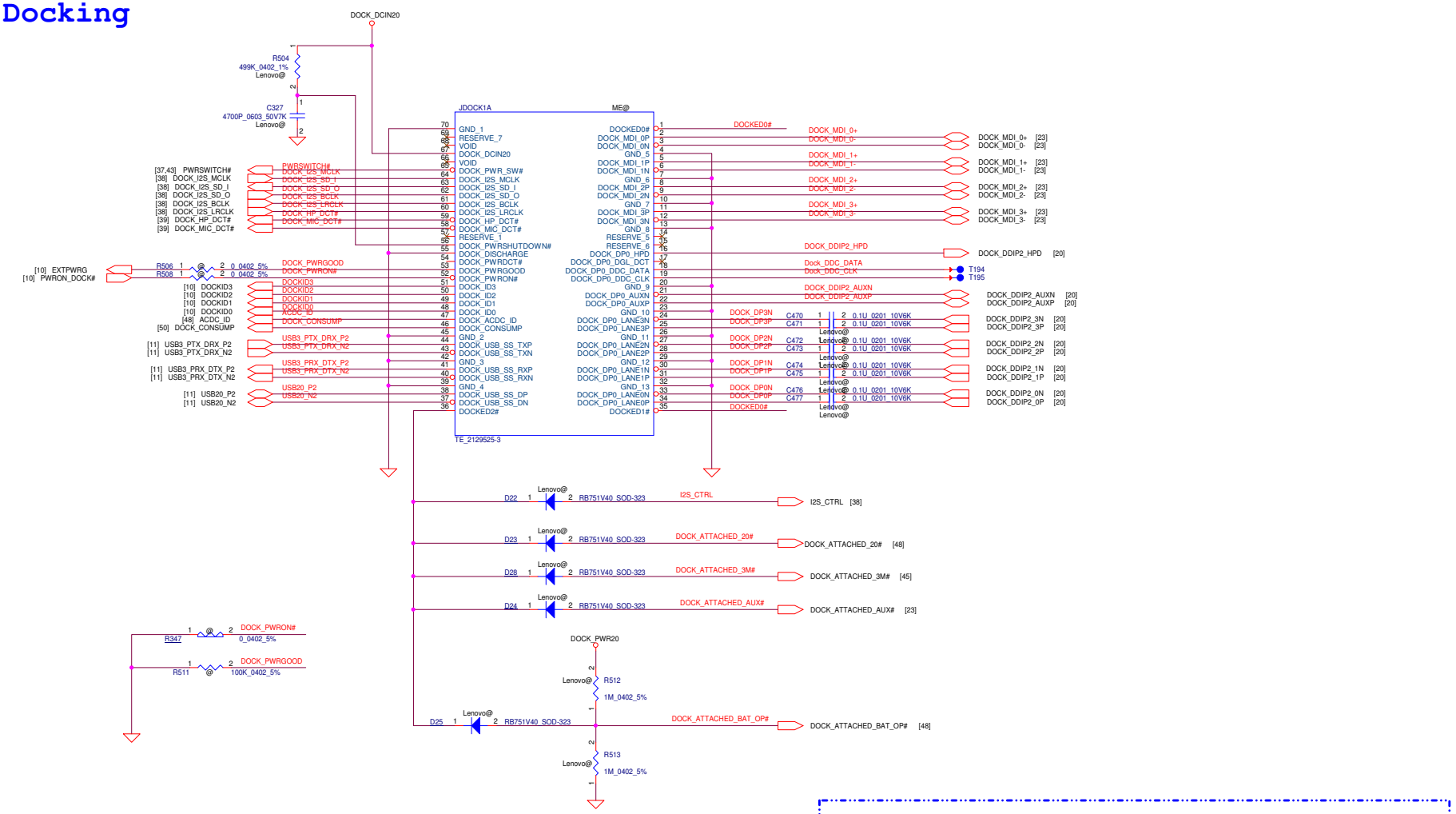
Compal Electronics, Inc.

Title: **DC/DC INTERFACE**

Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 46 of 58

Lenovo Docking



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **Docking CONN**

Size	Document Number	Rev
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Lenovo & NEC dif f er ent :

	Lenovo	NEC
PQ101	V	@
PR111	@	V
PR108	V	@
PJP101	V	@
PQ103	@	V
PR104	@	V
PR105	@	V
PR106	@	V
PR109	@	V
PQ104	@	V
PR129	@	V
PR130	@	V
PR132	@	V

	Lenovo	NEC
PQ102	V	@
PR131	V	@
PR133	V	@
PR134	V	@
PQ108	V	@
PC102	V	@
PR102	V	@
PR103	V	@
PC103	@	@
PR107	@	@
PC115	@	@
PC116	@	@
PQ109	@	V

	Lenovo	NEC
PQ110	@	V
PR135	@	V
PR136	@	V
PR137	@	V
PR138	@	V
PR141	@	V
PR142	@	V
PC117	@	V
PF102	V	@
PR144	V	@
PR145	V	@

ADP_ID

AC Adapter	45W	65W
R(ohm)	118	287
ADP_ID(V)	0.449	0.913
Detection -Voltage(V)	<=0.663, >0.234	<=1.134 >0.693

NEC: un-Mount
Lenovo: Mount

DOCK_PWR20
PQ102 Lenovo@ AO4407A_SO8
DOCK_PWR20_IN
Lenovo@ PF102
6A_24V_F1206HI6000V024TM
Lenovo@ PR102 200K_0402_5%
Lenovo@ PR131 100_0402_5%
PR103 Lenovo@ 100K_0402_5%
Lenovo@ PR133 100K_0402_5%
Lenovo@ PR134 100K_0402_5%
PC102 Lenovo@ 0.1U_0402_25V6
PQ108B Lenovo@ 2N7002KDW-2N_SOT363-6
Lenovo@ PR144 100K_0402_5%
PQ108A Lenovo@ 2N7002KDW-2N_SOT363-6
DOCK_ATTACHED_20# [47]
Lenovo@ PR145 100K_0402_5%

PJP101 @Lenovo@
PAD-OPEN 4x4m

ADPIN

@ JDCIN1
CVILU_CI0805M1HRA-NH
PF101
6A_24V_F1206HI6000V024TM

PQ103 NEC@ AON7401_DFN8-5
PR104 NEC@ 200K_0402_1%
PC103 @NEC@ 5600P_0402_25V7K
PR130 NEC@ 100_0402_5%
NEC@ PR105 200K_0402_1%
PR106 NEC@ 150K_0402_1%
PR107 @NEC@ 0_0402_5%
PQ104A NEC@ 2N7002KDW-2N_SOT363-6
ADP_OFF [45]
NEC@ PR129 0_0402_1%
@NEC@ PC115 .1U_0402_16V7K
NEC@ PR132 100K_0402_1%
NEC@ PQ104B 2N7002KDW-2N_SOT363-6
NEC@ PR109 200K_0402_1%

NEC: Mount
Lenovo: un-Mount

VIN
PL101 EMI@ BLM41PG600SN1L_2P
PC104 EMI@ 1000P_0402_50V7K
PC105 EMI@ 100P_0402_50V8J
PC106 EMI@ 100P_0402_50V8J
PC107 EMI@ 1000P_0402_50V7K

NEC: Mount
Lenovo: un-Mount
PR111 NEC@ 0_0402_1%

NEC: un-Mount
Lenovo: Mount
PQ101 Lenovo@ 2N7002KW_SOT323-3
DOCK_ATTACHED_BAT_OP# [47]

+3VALW
PR101 750_0402_1%
ADP_ID [45]
@PD101 ESD5Z3.3T1G_SOD523-2
PC101 .1U_0402_16V7K
PC108 @ 680P_0603_50V7K

NEC: un-Mount
Lenovo: Mount
PR108 Lenovo@ 0_0402_1%
ACDC_ID [47]

NEC@ PQ109 AO3413_SOT23-3
NEC@ PR141 215_0603_1%
NEC@ PR135 215_0603_1%
NEC@ PR142 215_0603_1%
ADP_ID
@NEC@ PC116 0.1U_0402_10V6K
NEC@ PR136 100K_0402_5%
NEC@ PR137 10K_0402_5%
NEC@ PR138 150K_0402_1%
NEC@ PQ110
ADP_OFF
NEC@ PC117 .1U_0402_16V7K
2N7002KW_SOT323-3

NEC: Mount
Lenovo: un-Mount

+CHGRTC
+3VLP
PR115 1K_0603_5%
@PR117 10K_0603_5%
PD103
+RTCBATT
S SCH DIO BAS40CW SOT-323
1K_0402_5% PR120
JRTC1 @
ACES_50273-0020N-001

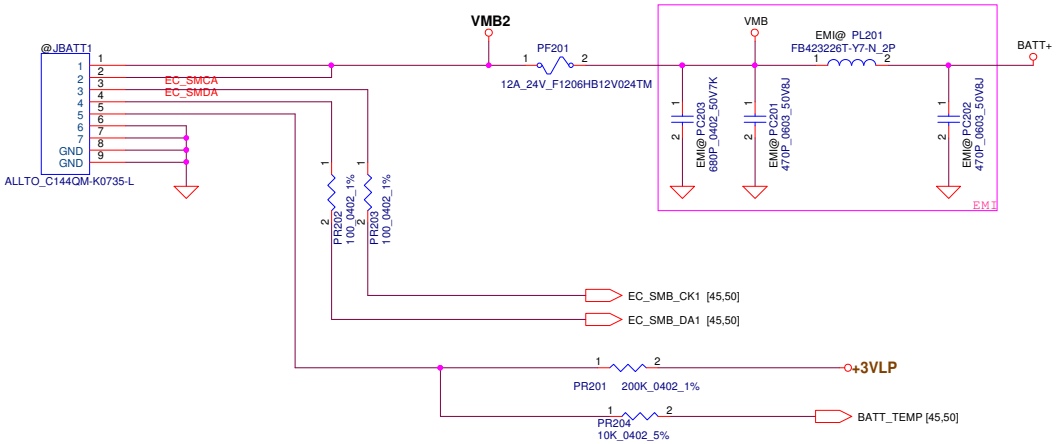
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **PWR-DCIN / Vin Detector**

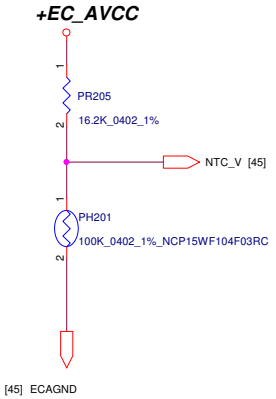
Size	Document Number	Rev
Custom	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 48 of 58



PH201 under CPU botten side :

CPU thermal protection at 93 degree C



PH201:	Temp.	Rman.	Rnor.	Rmin. (Kohm)
	93	7.3419	7.0792	6.8253

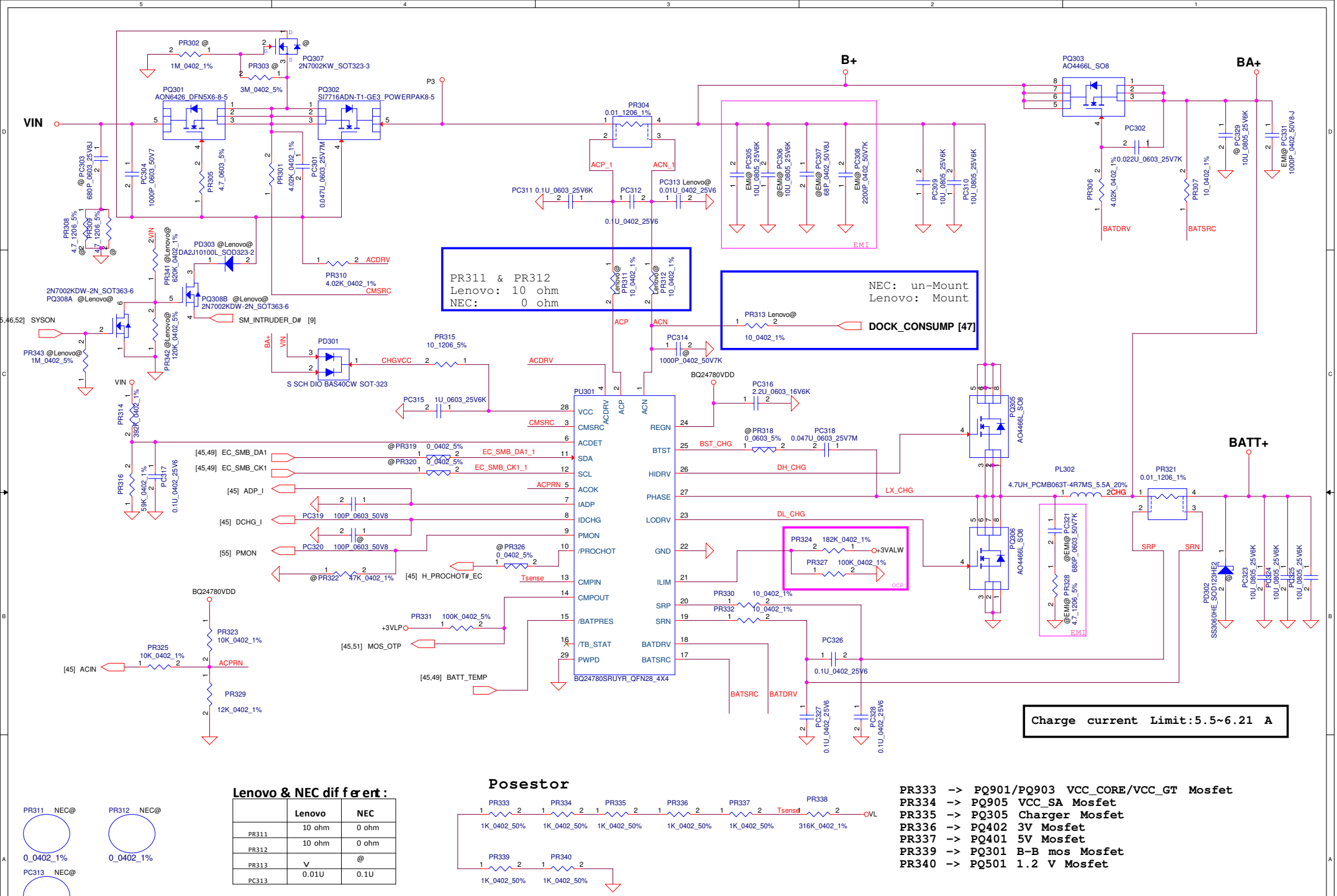
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **PWR-BATTERY CONN/OTP**

Size: Custom | Document Number: **LA-C422P** | Rev: 1.0

Date: Tuesday, November 15, 2016 | Sheet 49 of 58



Lenovo & NEC different:

	Lenovo	NEC
PR311	10 ohm	0 ohm
PR312	10 ohm	0 ohm
PR313	V	@
PC313	0.01U	0.1U

PR311 NEC@ 0_0402_1%

PR312 NEC@ 0_0402_1%

PC313 NEC@ 0.1U_0402_25V6

Posestor

PR333 1K_0402_50% — PR334 1K_0402_50% — PR335 1K_0402_50% — PR336 1K_0402_50% — PR337 1K_0402_50% — PR338 316K_0402_1% — VL

PR339 1K_0402_50% — PR340 1K_0402_50%

PR333 -> PQ901/PQ903 VCC_CORE/VCC_GT Mosfet
PR334 -> PQ905 VCC_SA Mosfet
PR335 -> PQ305 Charger Mosfet
PR336 -> PQ402 3V Mosfet
PR337 -> PQ401 5V Mosfet
PR339 -> PQ301 B-B mos Mosfet
PR340 -> PQ501 1.2 V Mosfet

Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: PWR-CHARGER

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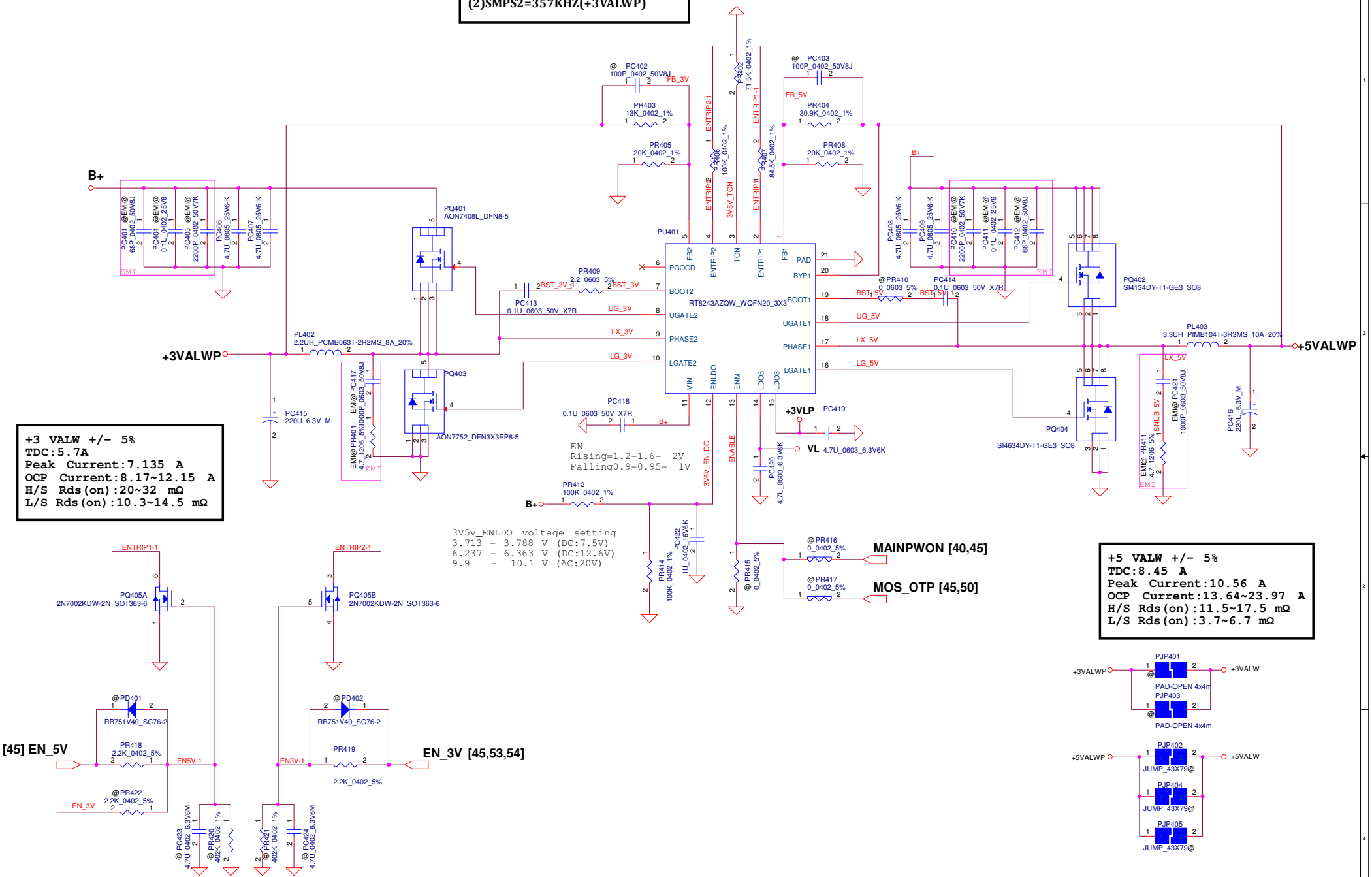
TON (1)SMPS1=305KHZ (+5VALWP)
(2)SMPS2=357KHZ(+3VALWP)



+3 VALW +/- 5%
TDC:5.7A
Peak Current:7.135 A
OCP Current:8.17~12.15 A
H/S Rds(on):20~32 mΩ
L/S Rds(on):10.3~14.5 mΩ

+5 VALW +/- 5%
TDC:8.45 A
Peak Current:10.56 A
OCP Current:13.64~23.97 A
H/S Rds(on):11.5~17.5 mΩ
L/S Rds(on):3.7~6.7 mΩ

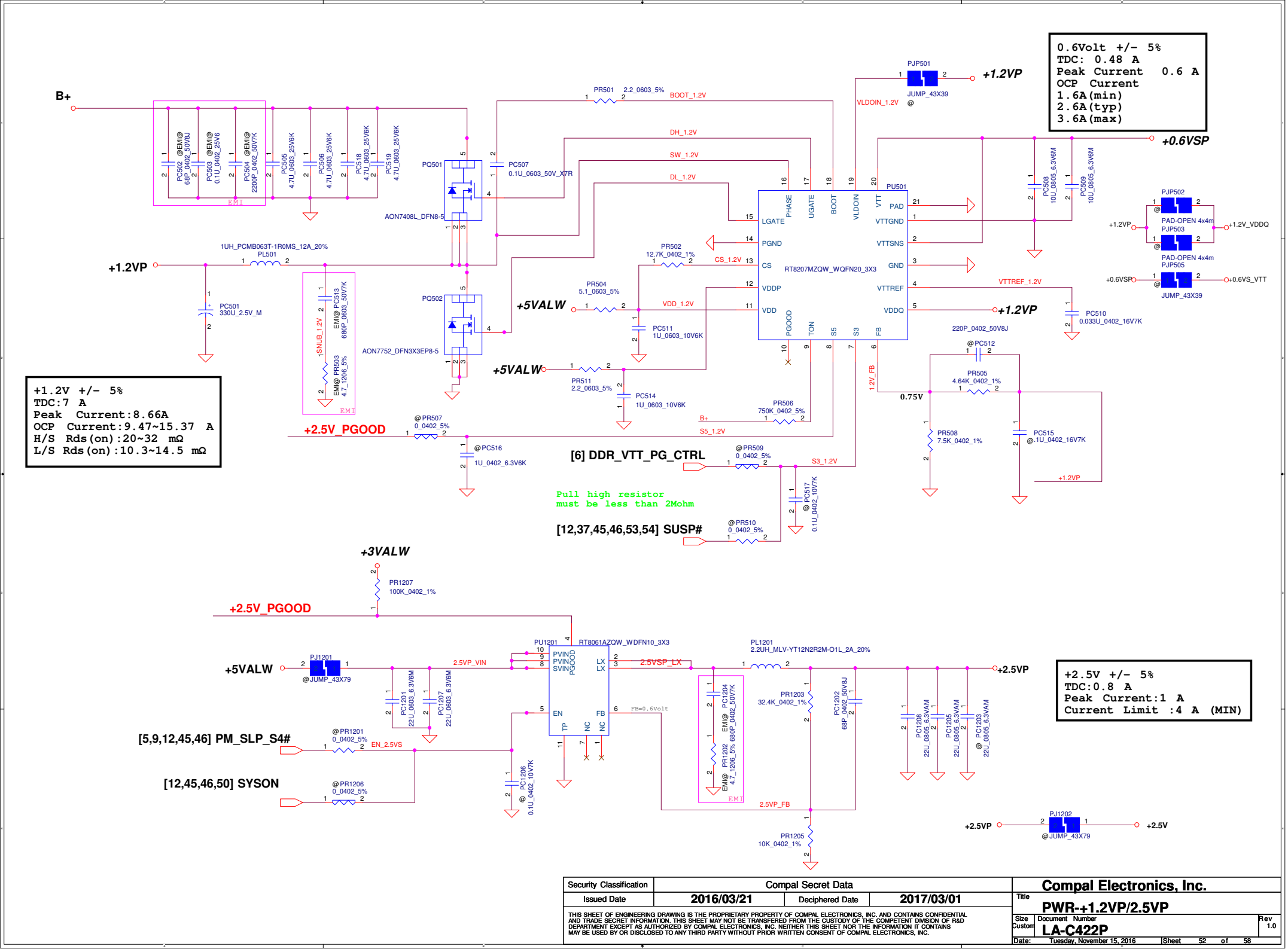
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: PWR-3VALWP/5VALWP

Size: Custom | Document Number: LA-C422P | Rev: 1.0

Date: Tuesday, November 15, 2016 | Sheet 51 of 58


B+
+1.2VP
+5VALW
+3VALW
+0.6VSP
+2.5V_PGOOD
0.6Volt +/- 5%
TDC: 0.48 A
Peak Current 0.6 A
OCP Current
1.6A(min)
2.6A(typ)
3.6A(max)
+1.2V +/- 5%
TDC:7 A
Peak Current:8.66A
OCP Current:9.47~15.37 A
H/S Rds(on):20~32 mΩ
L/S Rds(on):10.3~14.5 mΩ
RT8207MZQW_WQFN20_3X3
RT8061AZQW_WDFN10_3X3
AON7408L_DFN8-5
AON7752_DFN3X3EP8-5
1UH_PCMB063T-1R0MS_12A_20%
[6] DDR_VTT_PG_CTRL
Pull high resistor
must be less than 2Mohm
[12,37,45,46,53,54] SUSP#
[5,9,12,45,46] PM_SLP_S4#
[12,45,46,50] SYSON
+2.5V +/- 5%
TDC:0.8 A
Peak Current:1 A
Current Limit :4 A (MIN)
Compal Secret Data
2016/03/21
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PWR-+1.2VP/2.5VP
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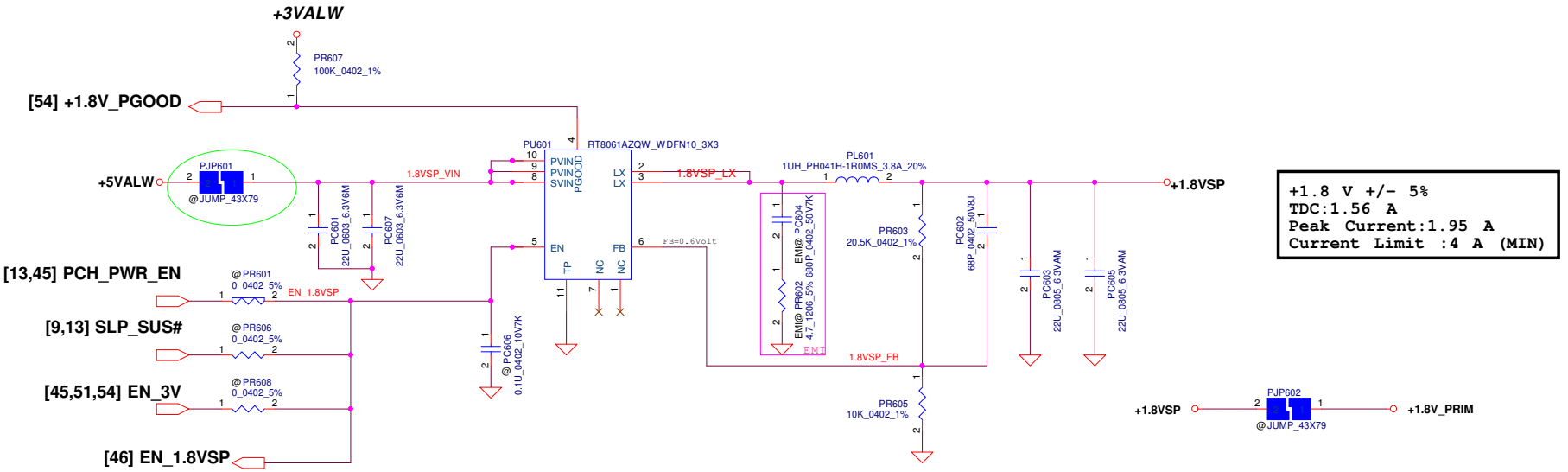
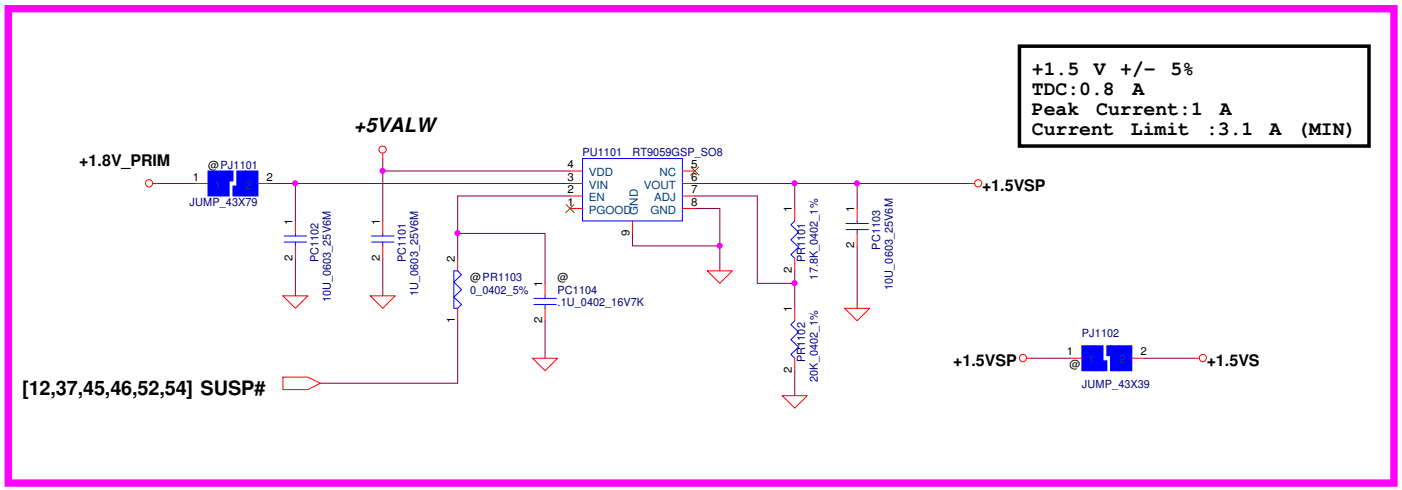




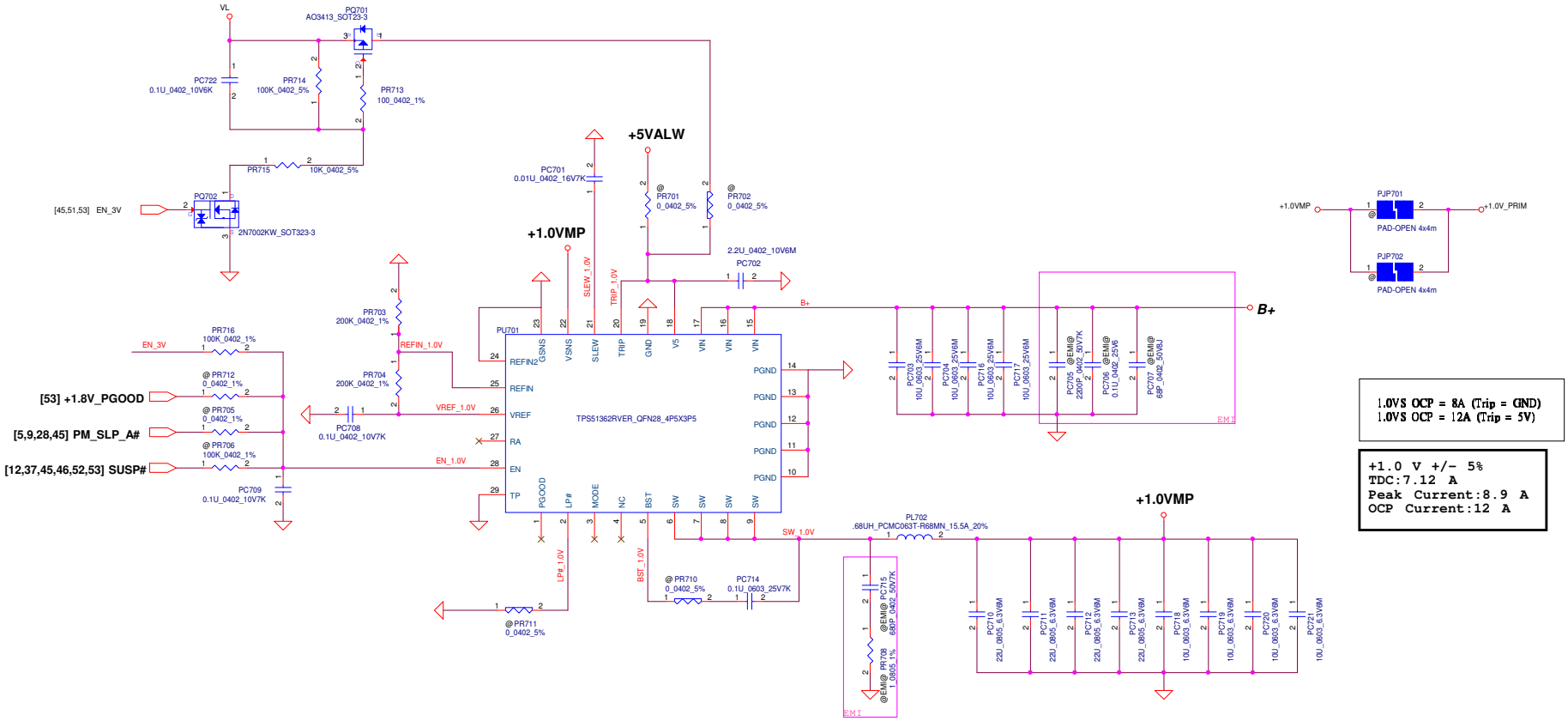
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **PWR-+1.8V/1.5VS**

Size	Document Number	Rev
Custom	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 53 of 58



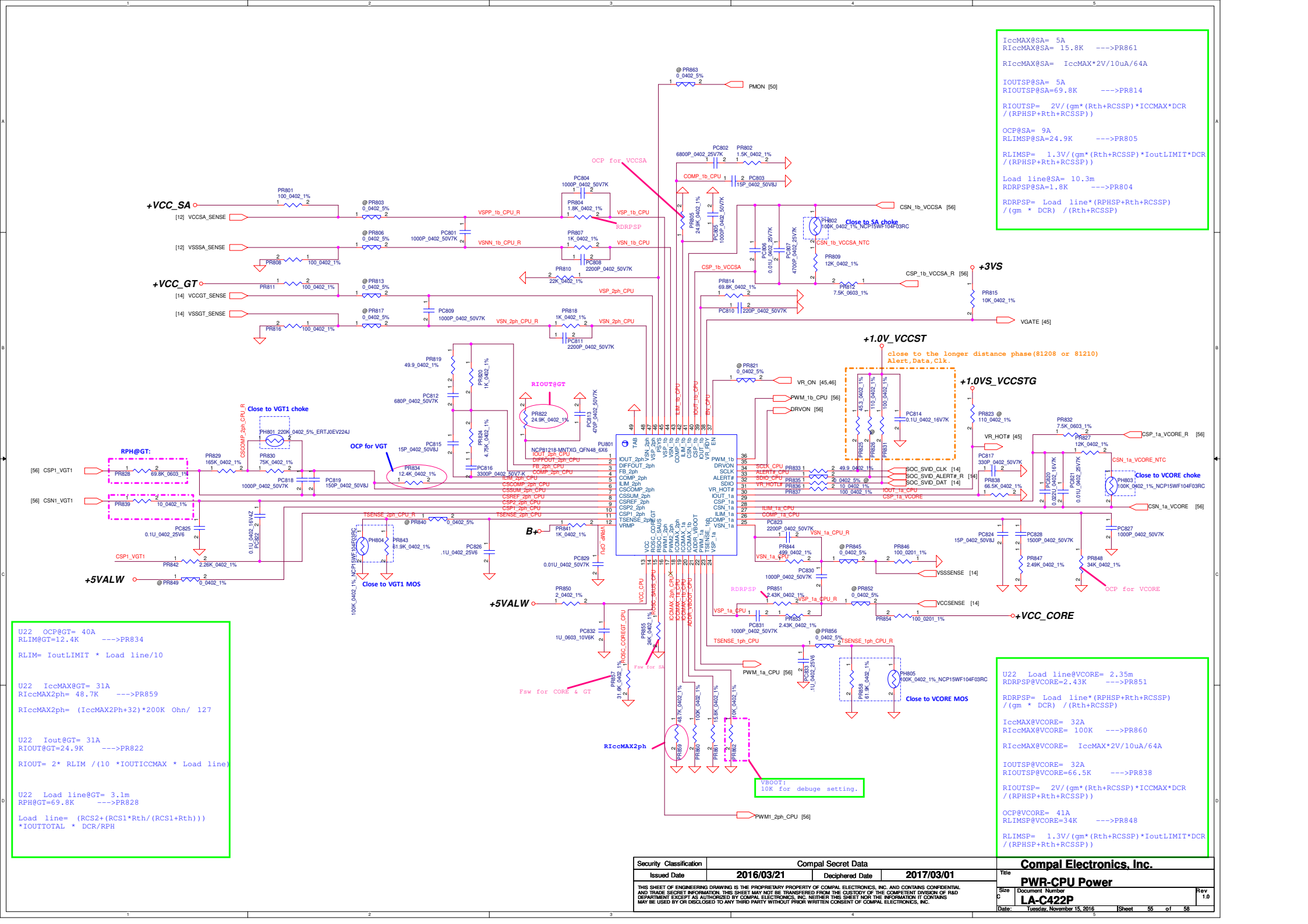
Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **PWR- +1.0VMP**

Size	Document Number	Rev
C	LA-C422P	1.0

Date: Tuesday, November 15, 2016 | Sheet 54 of 58


IccMAX@SA= 5A
RIccMAX@SA= 15.8K ---->PR861
RIccMAX@SA= IccMAX*2V/10uA/64A
IOUTSP@SA= 5A
RIOUTSP@SA=69.8K ---->PR814
RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR /(RPHSP+Rth+RCSSP))
OCP@SA= 9A
RLIMSP@SA=24.9K ---->PR805
RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR /(RPHSP+Rth+RCSSP))
Load line@SA= 10.3m
RDRPSP@SA=1.8K ---->PR804
RDRPSP= Load line*(RPHSP+Rth+RCSSP) /(gm * DCR) /(Rth+RCSSP)
+VCC_SA
+VCC_GT
+3VS
+1.0V_VCCST
close to the longer distance phase(81208 or 81210) Alert,Data,Clk.
+1.0VS_VCCSTG
OCP for VCCSA
RDRPSP
Close to SA choke
Close to VGT1 choke
Close to VGT1 MOS
Close to VCORE choke
Close to VCORE MOS
RPH@GT:
OCP for VGT
RIOUT@GT
RIccMAX2ph
B+
+5VALW
+VCC_CORE
OCP for VCORE
Fsw for CORE & GT
Fsw for SA
U22 OCP@GT= 40A
RLIM@GT=12.4K ---->PR834
RLIM= IoutLIMIT * Load line/10
U22 IccMAX@GT= 31A
RIccMAX2ph= 48.7K ---->PR859
RIccMAX2ph= (IccMAX2Ph+32)*200K Ohn/ 127
U22 Iout@GT= 31A
RIOUT@GT=24.9K ---->PR822
RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)
U22 Load line@GT= 3.1m
RPH@GT=69.8K ---->PR828
Load line= (RCS2+(RCS1*Rth/(RCS1+Rth))) *IOUTTOTAL * DCR/RPH
VBOOT: 10K for debuge setting.
U22 Load line@VCORE= 2.35m
RDRPSP@VCORE=2.43K ---->PR851
RDRPSP= Load line*(RPHSP+Rth+RCSSP) /(gm * DCR) /(Rth+RCSSP)
IccMAX@VCORE= 32A
RIccMAX@VCORE= 100K ---->PR860
RIccMAX@VCORE= IccMAX*2V/10uA/64A
IOUTSP@VCORE= 32A
RIOUTSP@VCORE=66.5K ---->PR838
RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR /(RPHSP+Rth+RCSSP))
OCP@VCORE= 41A
RLIMSP@VCORE=34K ---->PR848
RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR /(RPHSP+Rth+RCSSP))
PMON [50]
CSN_1b_VCCSA [56]
CSP_1b_VCCSA_R [56]
VGATE [45]
VR_ON [45,46]
PWM_1b_CPU [56]
DRVON [56]
VR_HOT# [45]
SOC_SVID_CLK [14]
SOC_SVID_ALERT#_R [14]
SOC_SVID_DAT [14]
CSP_1a_VCORE_R [56]
CSN_1a_VCORE [56]
VSSSENSE [14]
VCCSENSE [14]
PWM1_1a_CPU [56]
PWM1_2ph_CPU [56]
[12] VCCSA_SENSE
[12] VSSSA_SENSE
[14] VCCGT_SENSE
[14] VSSGT_SENSE
[56] CSP1_VGT1
[56] CSN1_VGT1
NCP81218-MNTXG_QFN48_6X6
Security Classification
Compal Secret Data
Issued Date
2016/03/21
Deciphered Date
2017/03/01
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Title
PWR-CPU Power
Size C
Document Number LA-C422P
Rev 1.0
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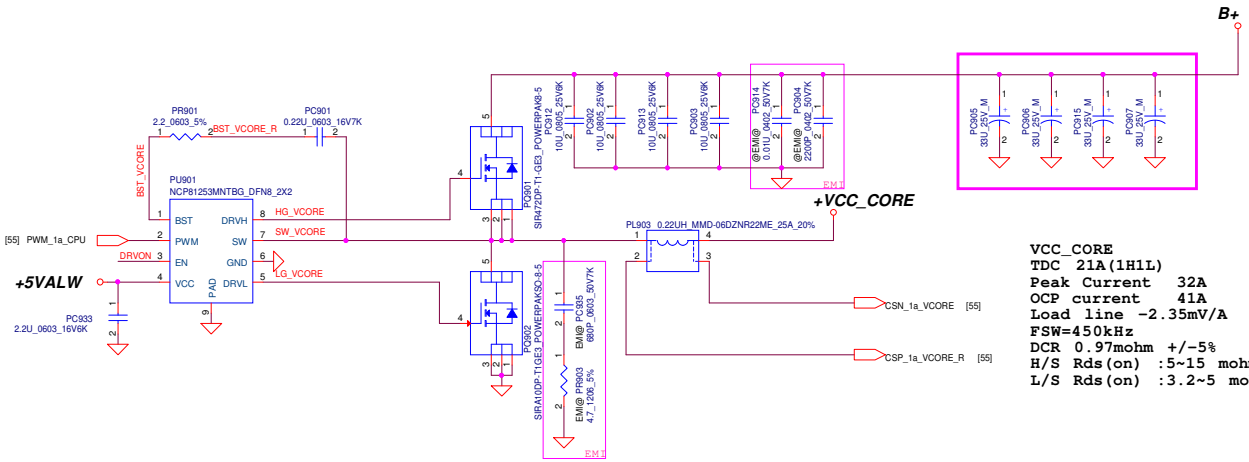
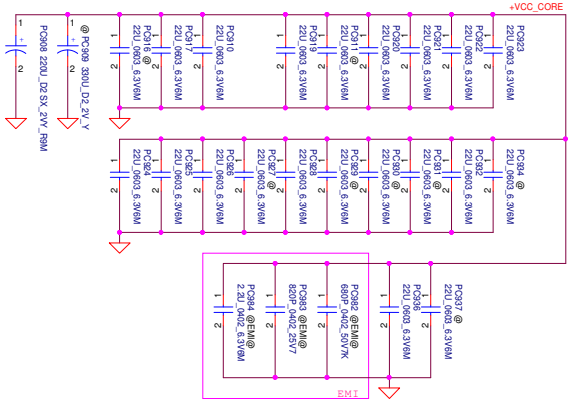
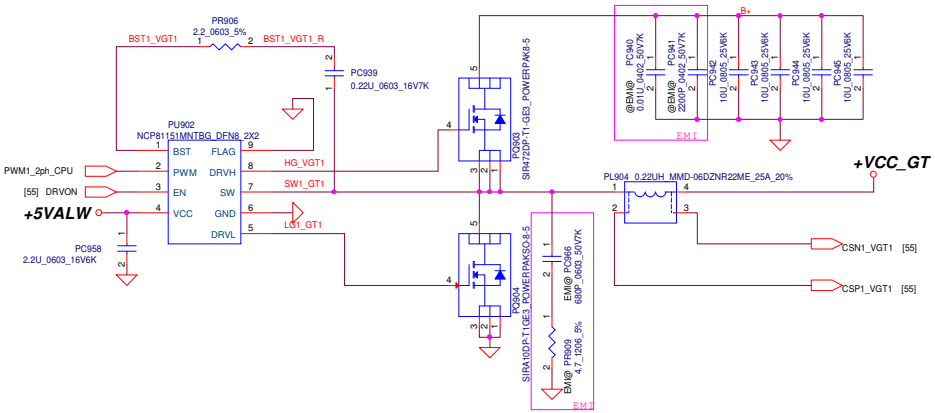


VCC_CORE
TDC 21A(1H1L)
Peak Current 32A
OCP current 41A
Load line -2.35mV/A
FSW=450kHz
DCR 0.97mohm +/-5%
H/S Rds(on) :5~15 mohm
L/S Rds(on) :3.2~5 mohm

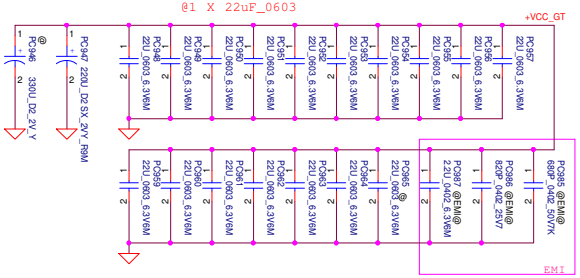
Total VCORE Output Capacitor:
20 X 22uF_0603_X5R + 330U/R9 *2
@3 X 22uF_0603_X5R

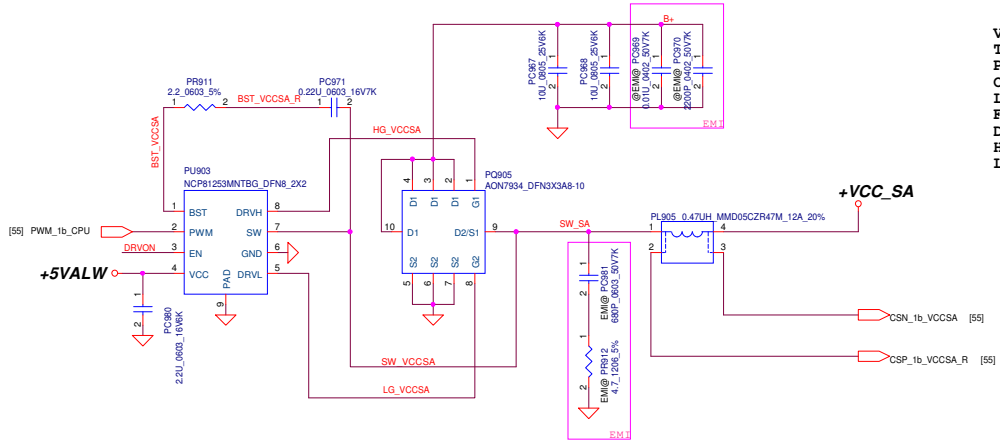




VCCGT(1 phase)
TDC 18A(1H1L)
Peak Current 31A
OCP current 40A
Load line -3.1mV/A (KBL U-22)
FSW=450kHz
DCR 0.97mohm +/-5%
H/S Rds(on) :5~15 mohm
L/S Rds(on) :3.2~5 mohm

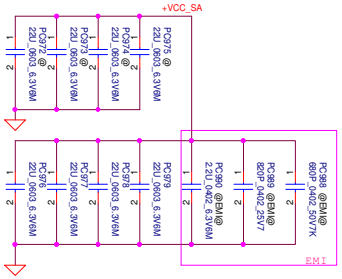
Total VGT Output Capacitor:
16 X 22uF_0603 + 2 X 330uF_9m
@1 X 22uF_0603





VCCSA
TDC NA(1H1L)
Peak Current 5A
OCP current 8A
Load line -10.3mV/A
FSW=450kHz
DCR 6.2 mohm +/-5%
H/S Rds(on) :10.2~19.2 mohm
L/S Rds(on) :7.7~14 mohm

Total VCSA Output Capacitor:
8X 22uF_0603



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: PWR-CPU Power Stages

Size	Document Number	Rev
C	LA-C422P	1.0

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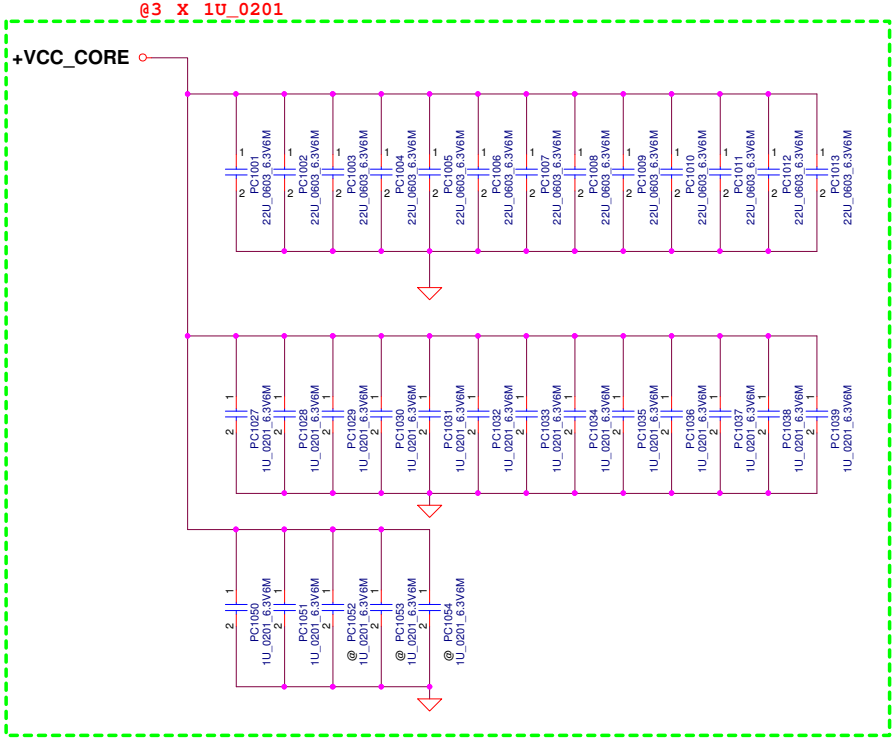
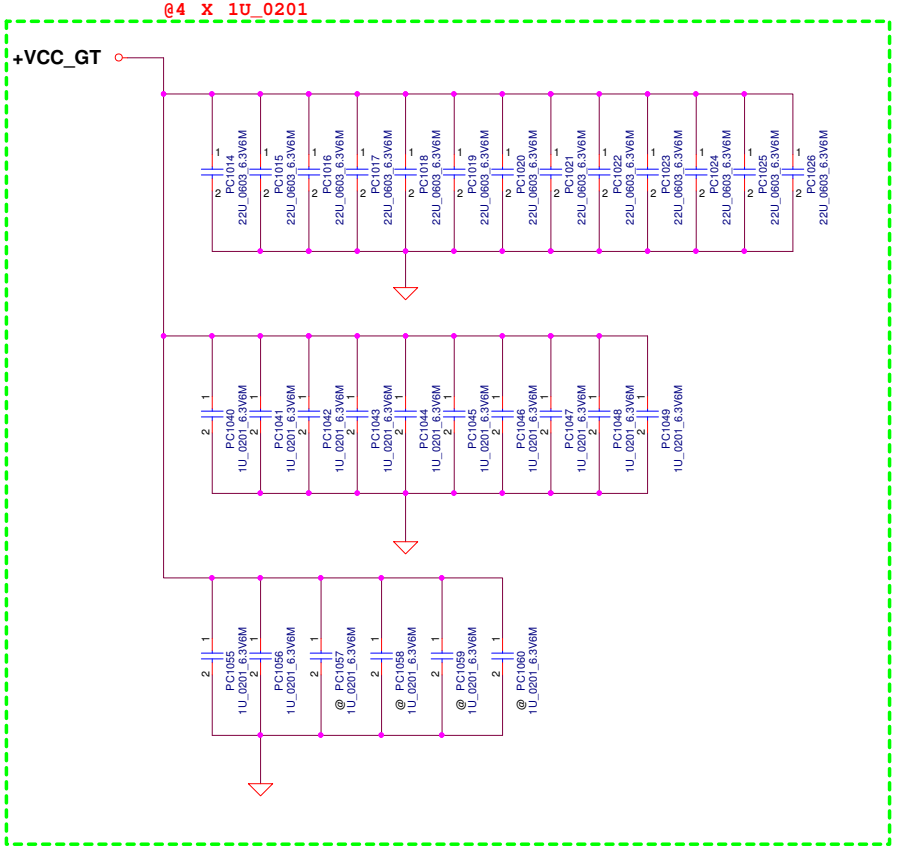
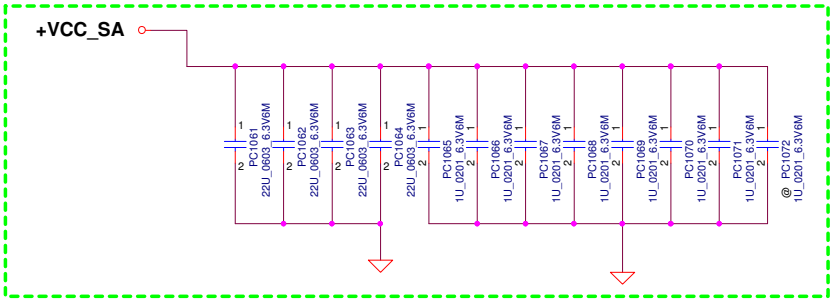
VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 13 pcs +1U_0201*35 pcs
@3 X 1U_0201



VCC_GT Place on CPU Back Side @ V09
22U_0603 * 13 pcs +1U_0201*12 pcs
@4 X 1U_0201



VCC_SA Place on CPU Back Side
22U_0603 * 4 pcs + 1U_0201*7
@ 1U_0201



Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: PWR-CPU BACK SIDE MLCC

Size: Custom | Document Number: LA-C422P | Rev: 1.0

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2016/03/21	Deciphered Date	2017/03/01

Compal Electronics, Inc.

Title: **PWR-PIR**

Size	Document Number	Rev
Custom	LA-C422P	1.0

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