EVT

AMD S1G2 PROCESSOR
638-Pin uFCPGA 638
CPU REV 11
5,6,7,8

DDRII 800MT/S
UNBUFFERED DDR2 NEAR SODIMM 9,10
200-PIN DDR2 SODIMM

DDRII 800MT/S
UNBUFFERED DDR2 FAR SODIMM 9,10
200-PIN DDR2 SODIMM

EXTERNAL CLOCK GENERATOR
CS9LPRS472 16

HT3 2600Mhz
5.2GT/s
16x16
OUT
IN

ATI NB - RS780M
HyperTransport LINK3 CPU I/F
DX10 IGP
LVDS/TVOUT/TMDS
1 X16 PCIE GFX I/F
1 X4 A-Link II-E I/F WITH SB
6 X1 PCIE GPP I/F
11,12,13,14,15

X16 PEIE I/F
ATI VGA - M82S
22,23,24,25,26,28,29
667M
GDDRIII 27
667M
GDDRIII 27

CRT
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TMDS

CRT
VGA CON 40

LVDS
LVDS CON 40

TMDS
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PCIE I/F

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A-LINK II
PCIE1.1
1X4 Lanes
2.5Gbps/L

ATI SB - SB700
USB 2.0 (12 PORTS)
SATA II (6 PORTS)
ATA 66/100/133
SMBus 2.0
SPI I/F
LPC I/F
ACPI 2.0
INT RTC
HW MONITOR
PCI/PCI BDGE
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SATA H.D.D. CONN. 37
UP TO SATAII
SATA 1.5/2.5/3Gbps
SATA O.D.D. CONN. 37

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KBD MOUSE 39
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Option Orange for MS13321 & MS12241
Option Green for MS13331 & MS12251
Option below for Cross File Circuit

HDMI
LVDS
ATI NB - RS780M
ATI VGA - M82S
GDDRIII X2
VGA

CPU&RS780 HT VLDT POWER 47
RS780 CORE POWER 44
CPU CORE POWER 47
SB700 & PCIE POWER 44
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M82S & GDDR III POWER 45
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Title: BLOCK DIAGRAM
Size: Custom
Document Number: MS-13331
Rev: 0B
Date: Tuesday, December 11, 2007
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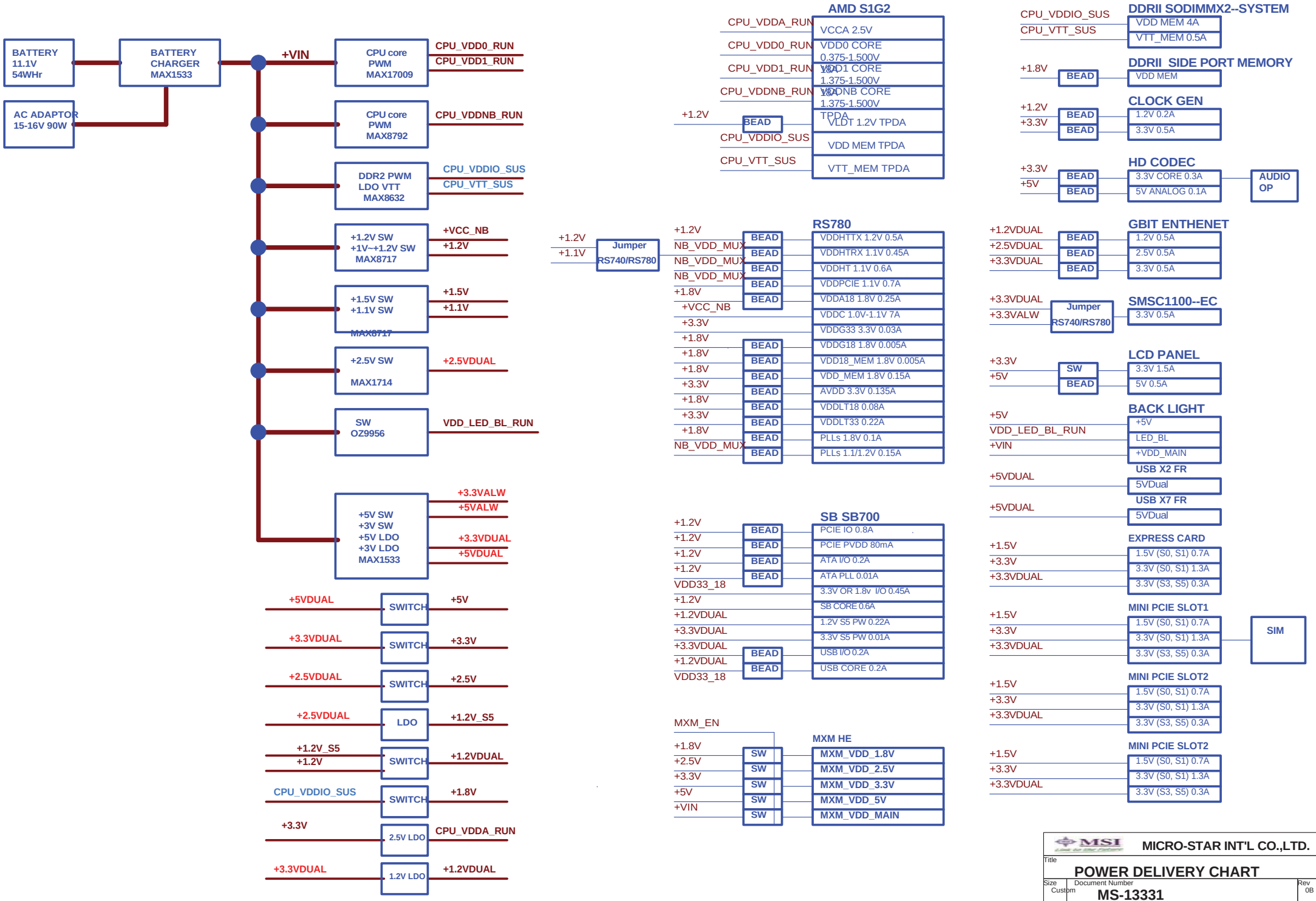
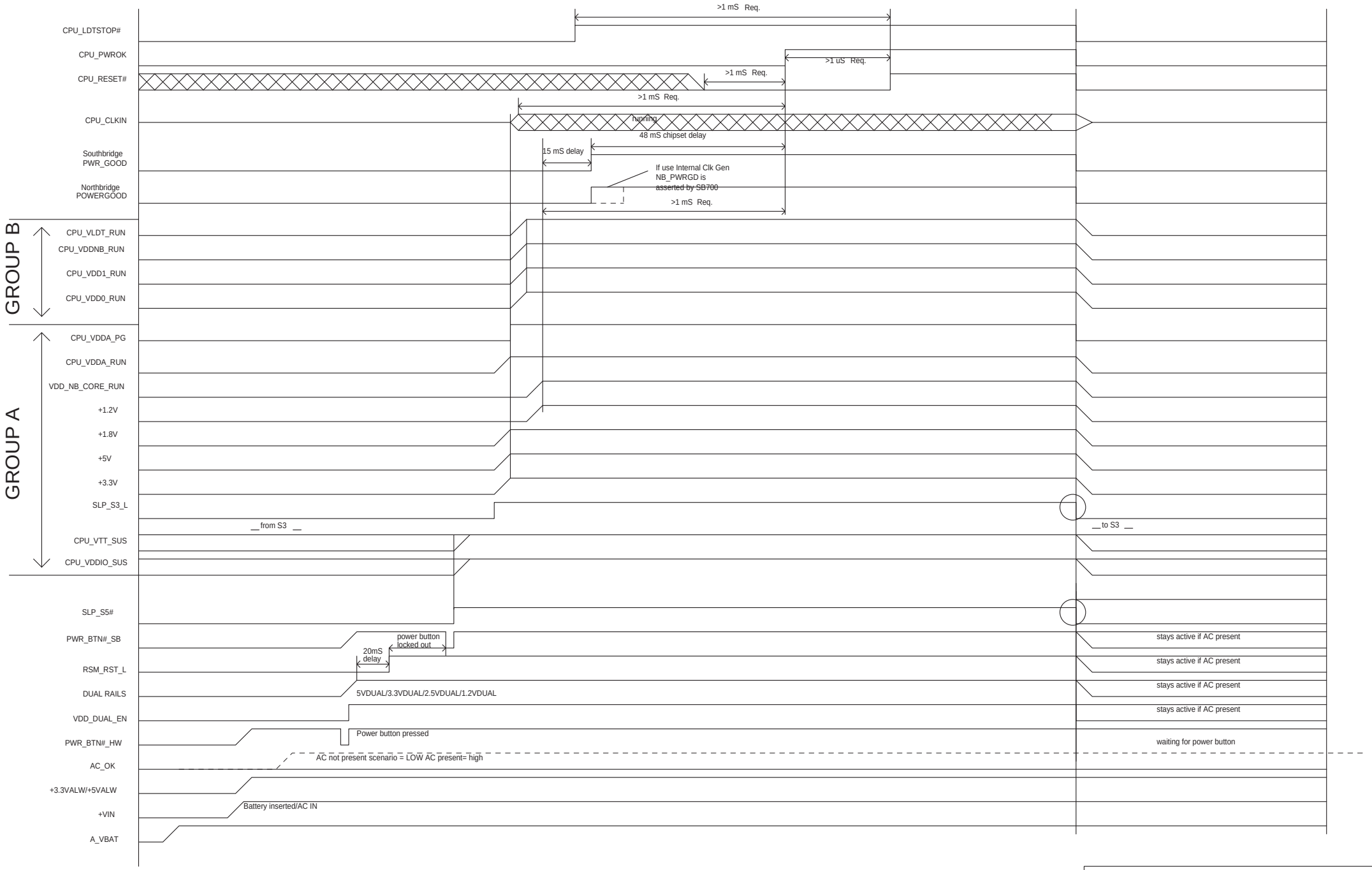


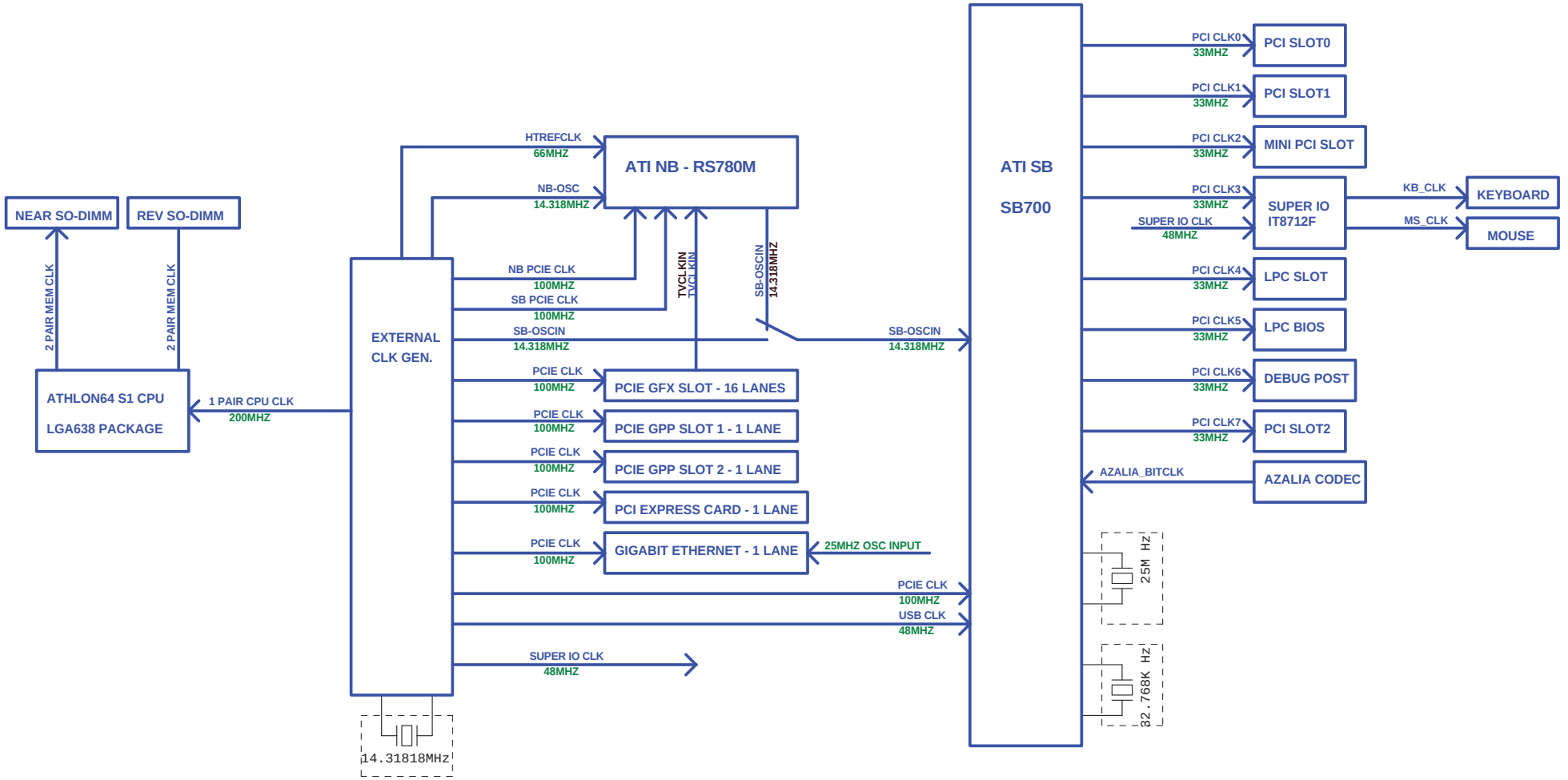


MICRO-STAR INT'L CO.,LTD.

Title: POWER SEQUENCE CHART

Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 3 of 55



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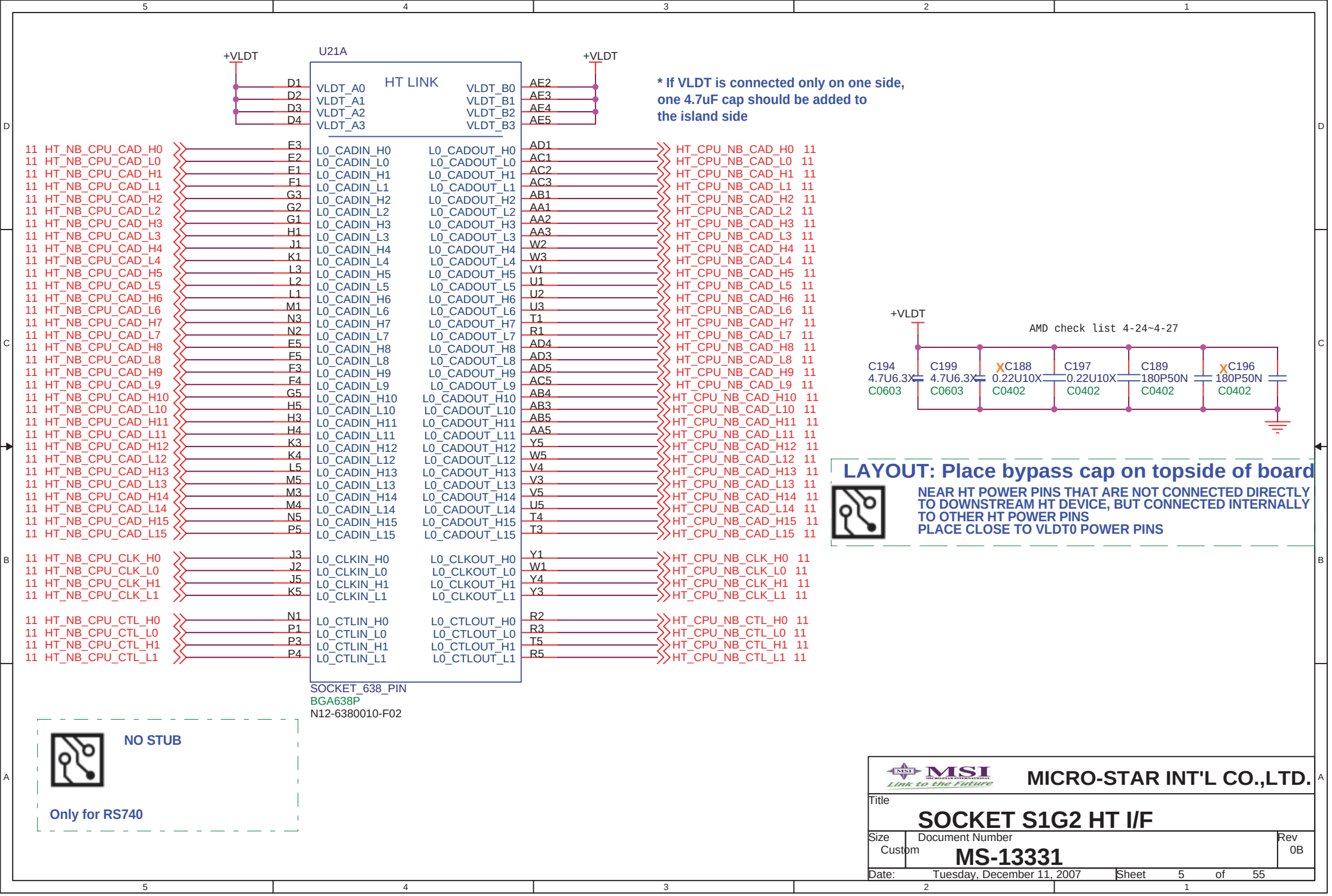
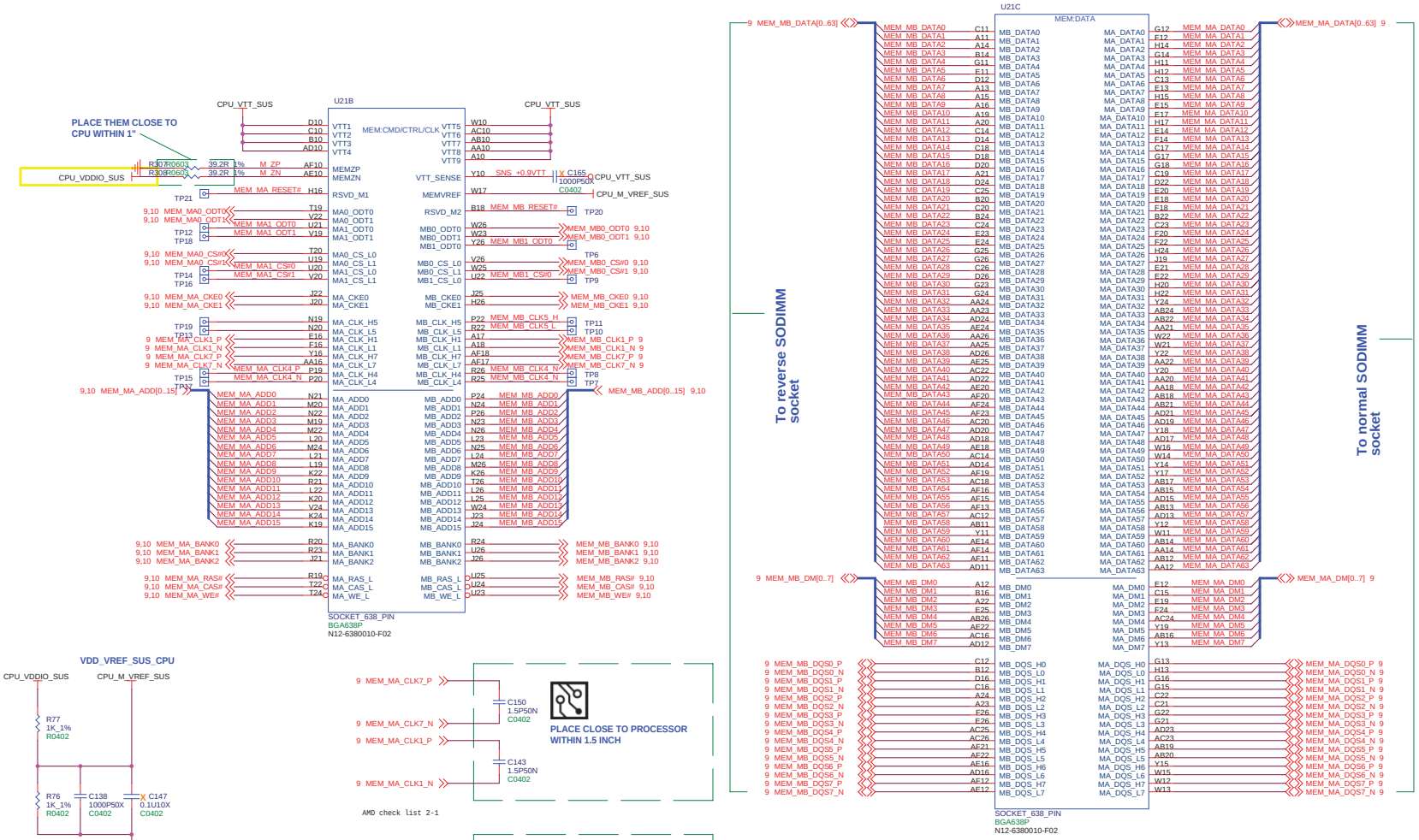
Title: CLOCK DISTRIBUTION

Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 4 of 55



Processor Memory Interface



CPU_VDDA_2.5_RUN

maximun 40 ohm

VDDA 2.5V ==> Max Current 250mA

AMD check list 4-22

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"

If unused, the ALERT_L pin is left unconnected

place them to CPU within 1.5"

PWM

PWM

PWM

route as differential as short as possible testpoint under package

Cap close to thermal sensor

Close to CPU socket

CPU_PWRGD Pull up to 1.8VRun

SOCKET_638_PIN
BGA638P
N12-6380010-F02

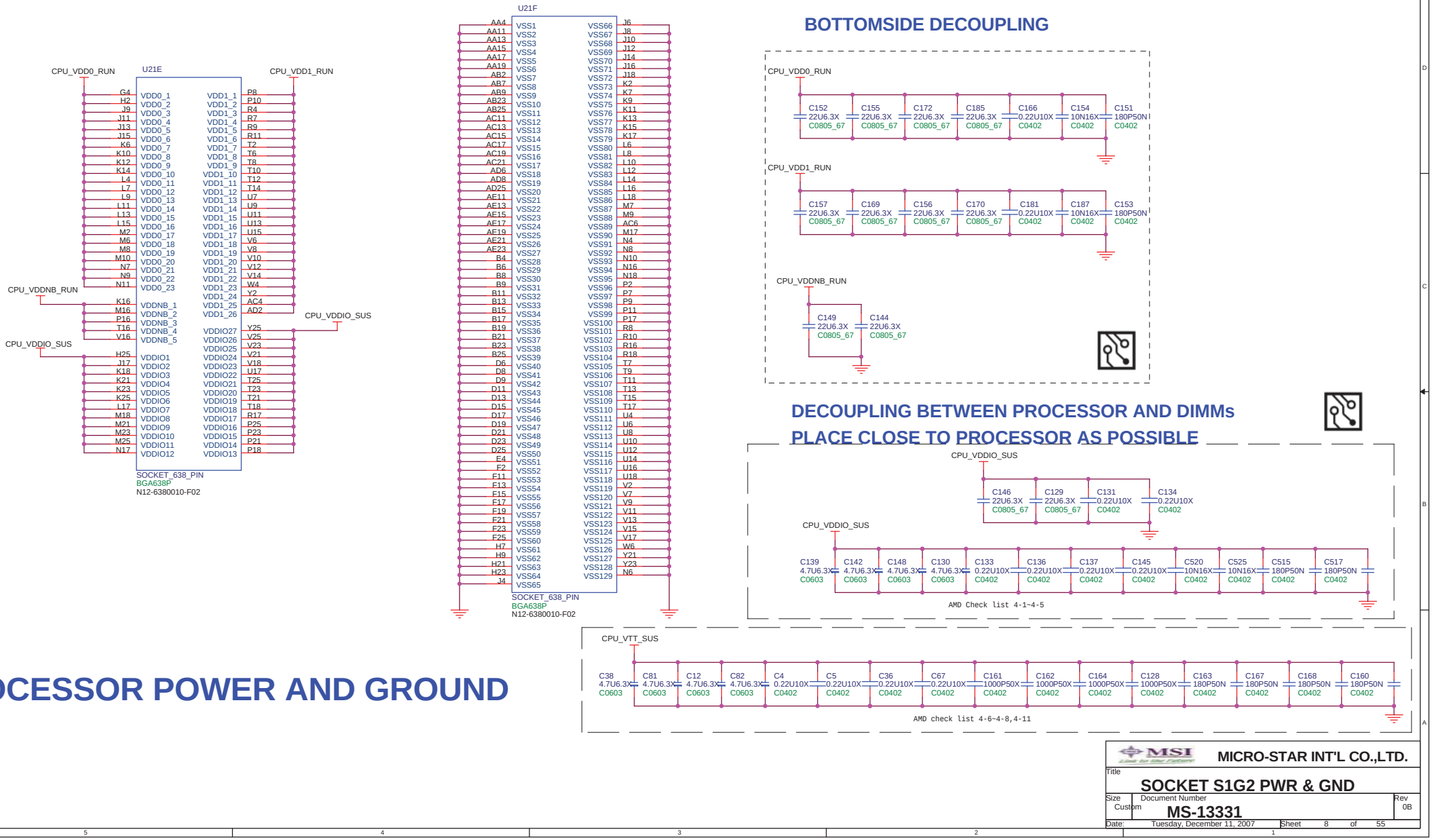
LM86CIMMXNOPB_MSOP8-RH
MSOP8_T

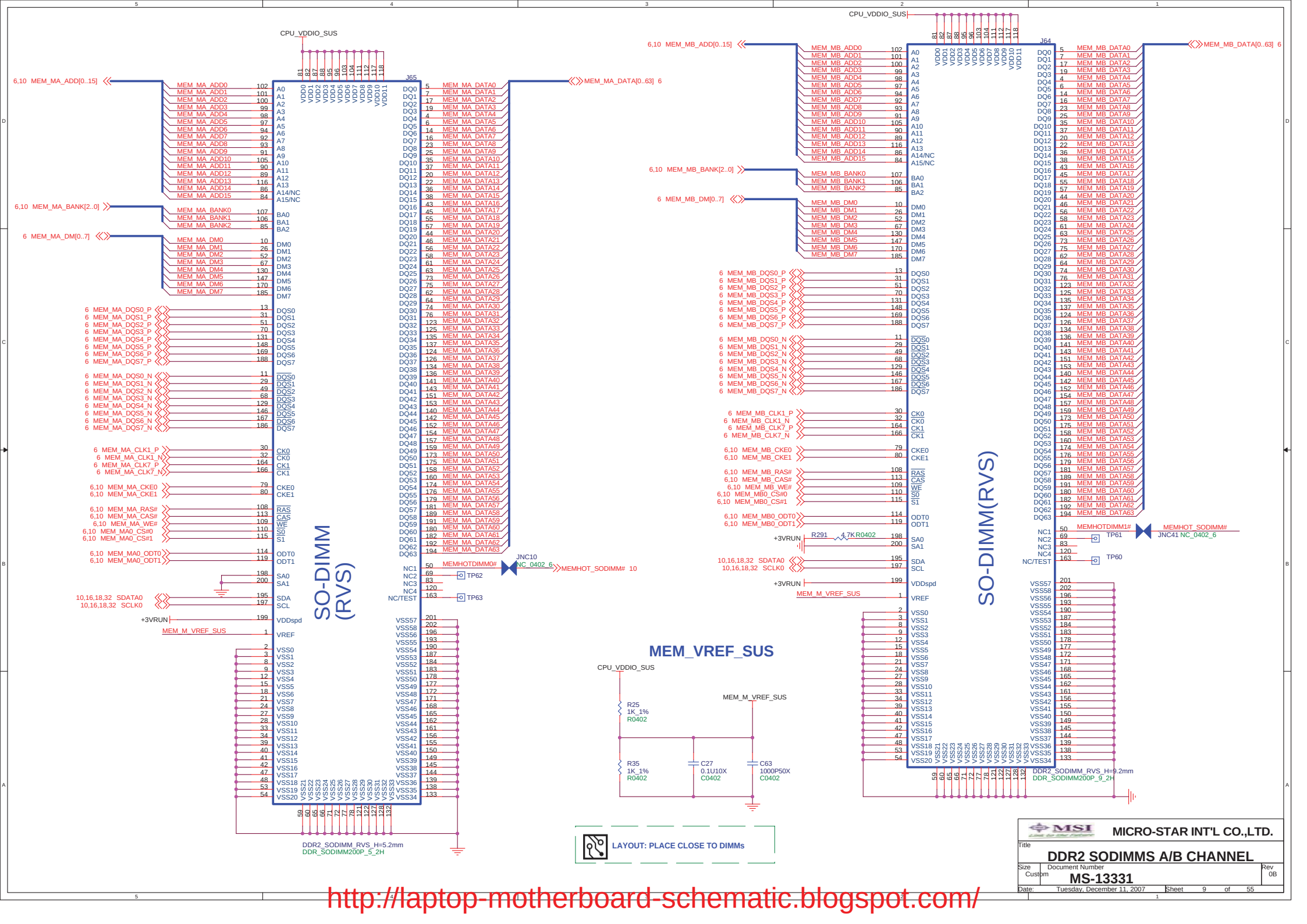
MICRO-STAR INT'L CO.,LTD.

Title: SOCKET S1G2 CTRL

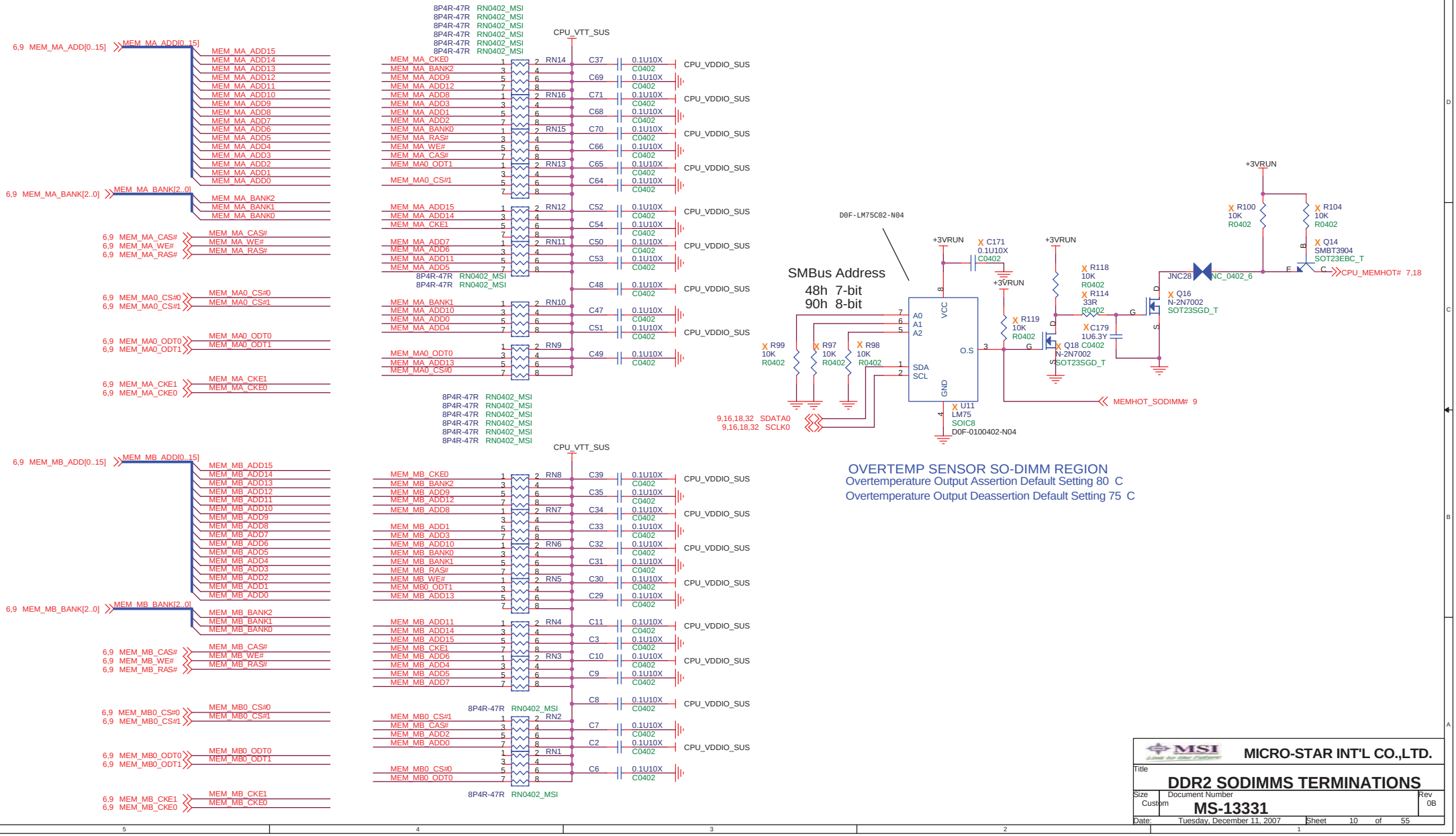
Size: Custom | Document Number: MS-13331 | Rev: 0B

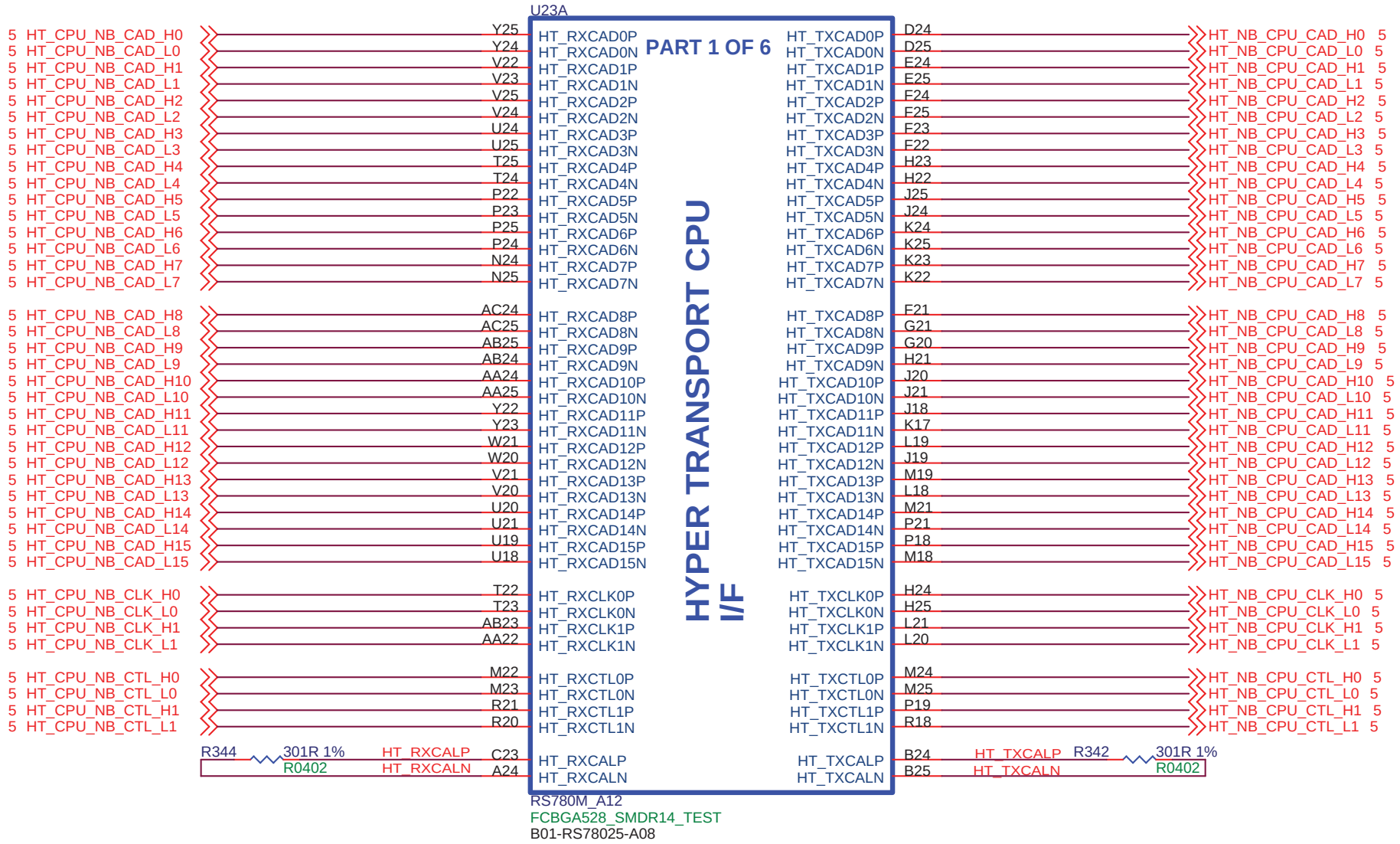
Date: Tuesday, December 11, 2007 | Sheet 7 of 55





MICRO-STAR INT'L CO.,LTD.	
Title	DDR2 SODIMMS A/B CHANNEL
Size: Custom	Document Number: MS-13331
Rev	0B
Date: Tuesday, December 11, 2007	Sheet 9 of 55





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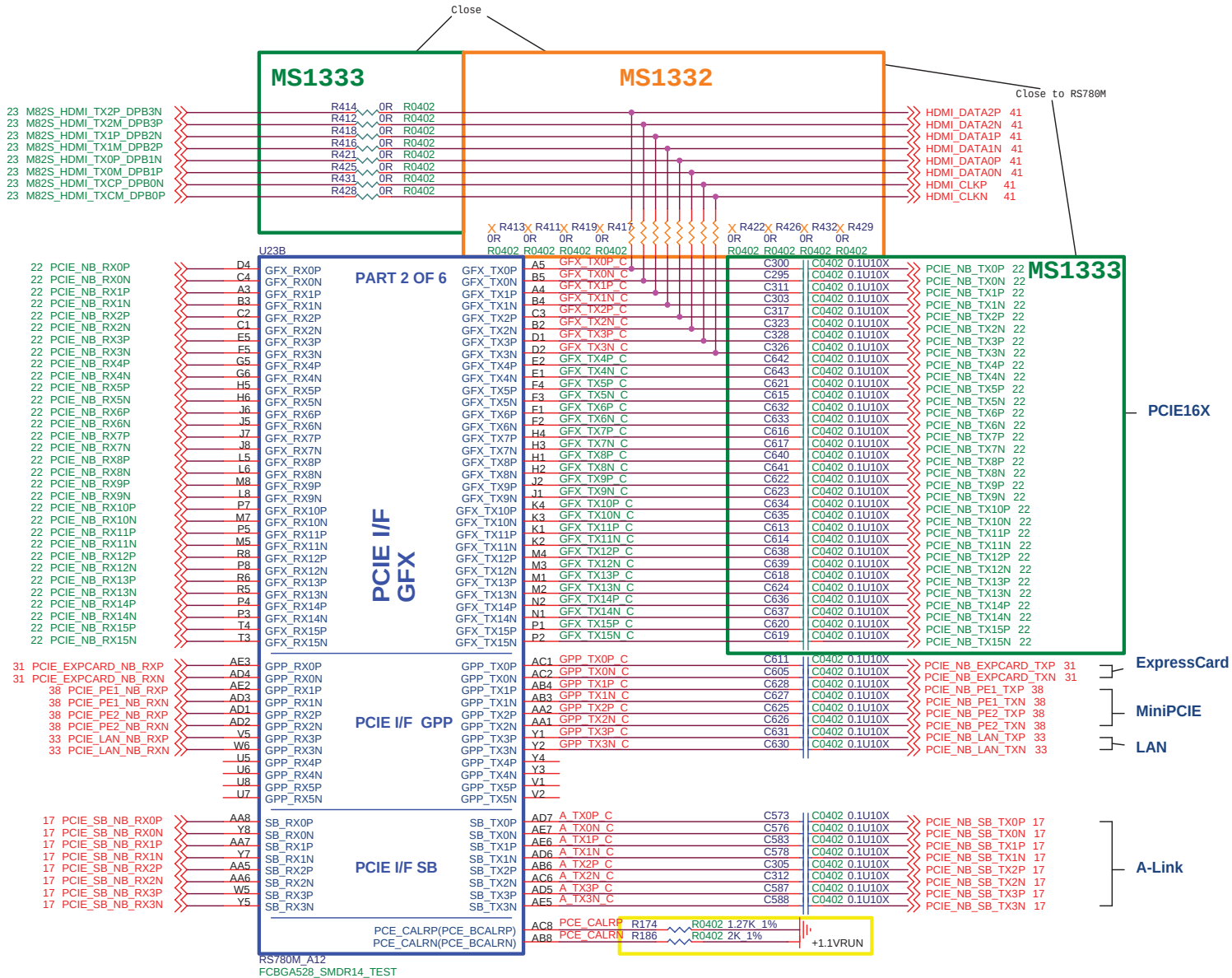
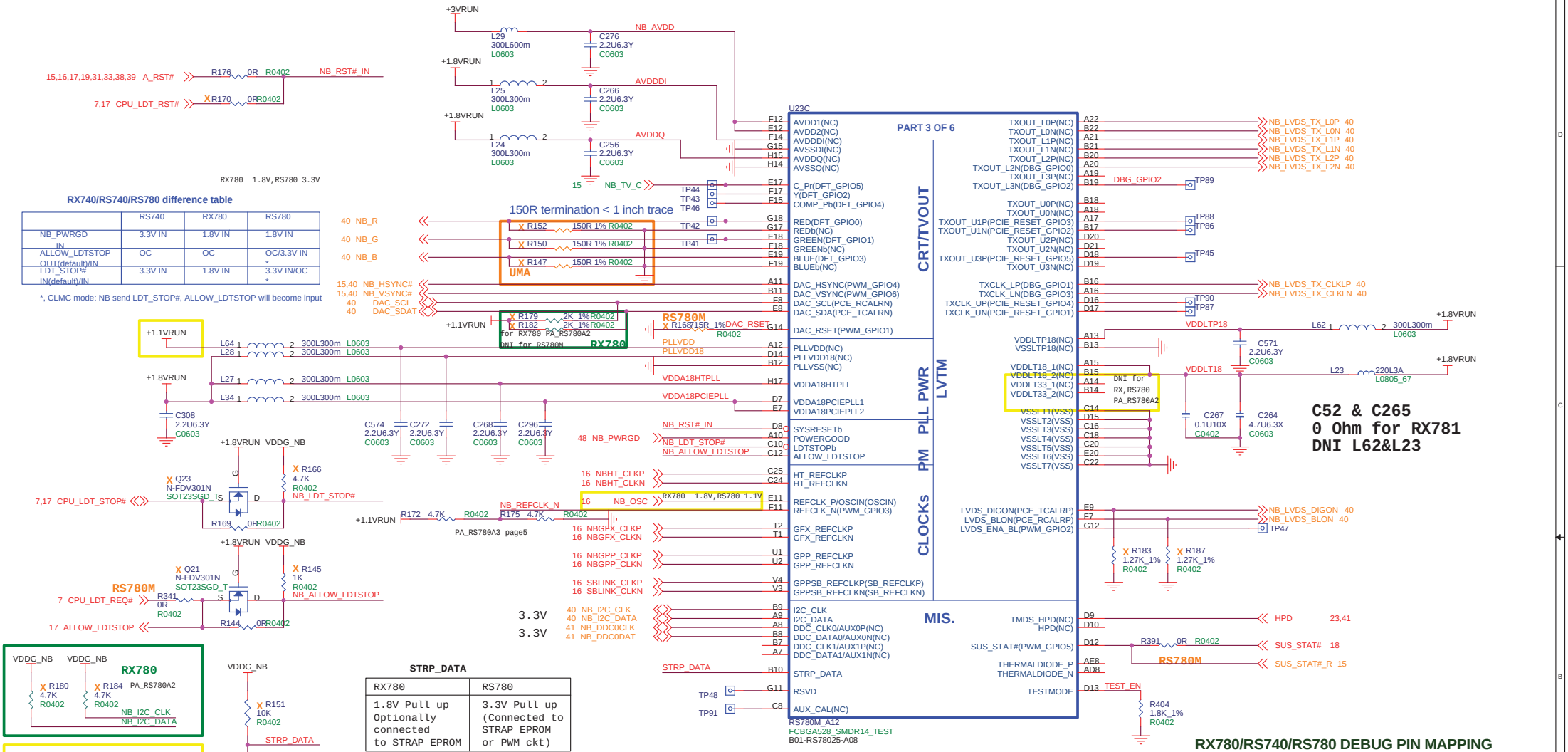
Title: RX/RS780 HT LINK I/F

Size	Document Number	Rev
A	MS-13331	0B

Date: Tuesday, December 11, 2007 Sheet 11 of 55



MICRO-STAR INT'L CO.,LTD.	
Title	RX/RS780 PCI-E LINK&GPP
Size B	Document Number MS-13331 Rev 0B
Date: Tuesday, December 11, 2007	Sheet 12 of 55



	RS740	RX780	RS780
NB_PWRGD IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP OUT(default)/IN	OC	OC	OC/3.3V IN *
LDT_STOP# IN(default)/IN	3.3V IN	1.8V IN	3.3V IN/OC *

*, CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

STRP_DATA	
RX780	RS780
1.8V Pull up Optionally connected to STRAP EPROM	3.3V Pull up (Connected to STRAP EPROM or PWM ckt)

PA_RS780A3 PU = Optionally connected to STRAP EPROM

Adobe Acrobat Professional - [PA_RS780A3.pdf]

RS740/RX780/RS780 Northbridge Clock Input Table:

NB CLOCKS	RS740	RX780	RS780		
HT_REFCLKP	66Mhz (SE)	100Mhz (DIFF)	100Mhz (DIFF)		
HT_REFCLKN	NC	100Mhz (DIFF)	100Mhz (DIFF)		
REFCLK_P	14Mhz (SE 3.3V)	14Mhz (SE 1.8V)	14Mhz (SE 1.1V)	or	100Mhz (DIFF)
REFCLK_N	NC	NC	Vref(.55V)		100Mhz (DIFF)
GFX_REFCLK	100Mhz (DIFF)	100Mhz (DIFF)	100Mhz DIFF (In/Out)*		
GPP_REFCLK	NC	100Mhz (DIFF)	100Mhz DIFF (Out)		
GPPSB_REFCLK	100Mhz (DIFF)	100Mhz (DIFF)	100Mhz (DIFF)		

"" RS780 can be used as clock buffer to output two PCIE reference clocks. By default chip will configure in input mode, the BIOS can program it to output mode.*

RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	AUX_CAL
	COMB_Pb(DFT_GPIO4)	X	X
	C_Pr(DFT_GPIO5)	X	X

MICRO-STAR INT'L CO.,LTD.

Title: RX/RS780 SYSTEM I/F

Size: Custom | Document Number: MS-13331 | Rev: 0B

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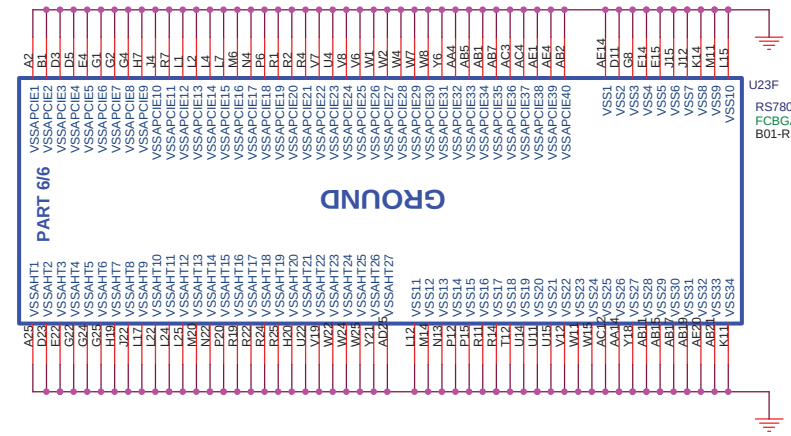
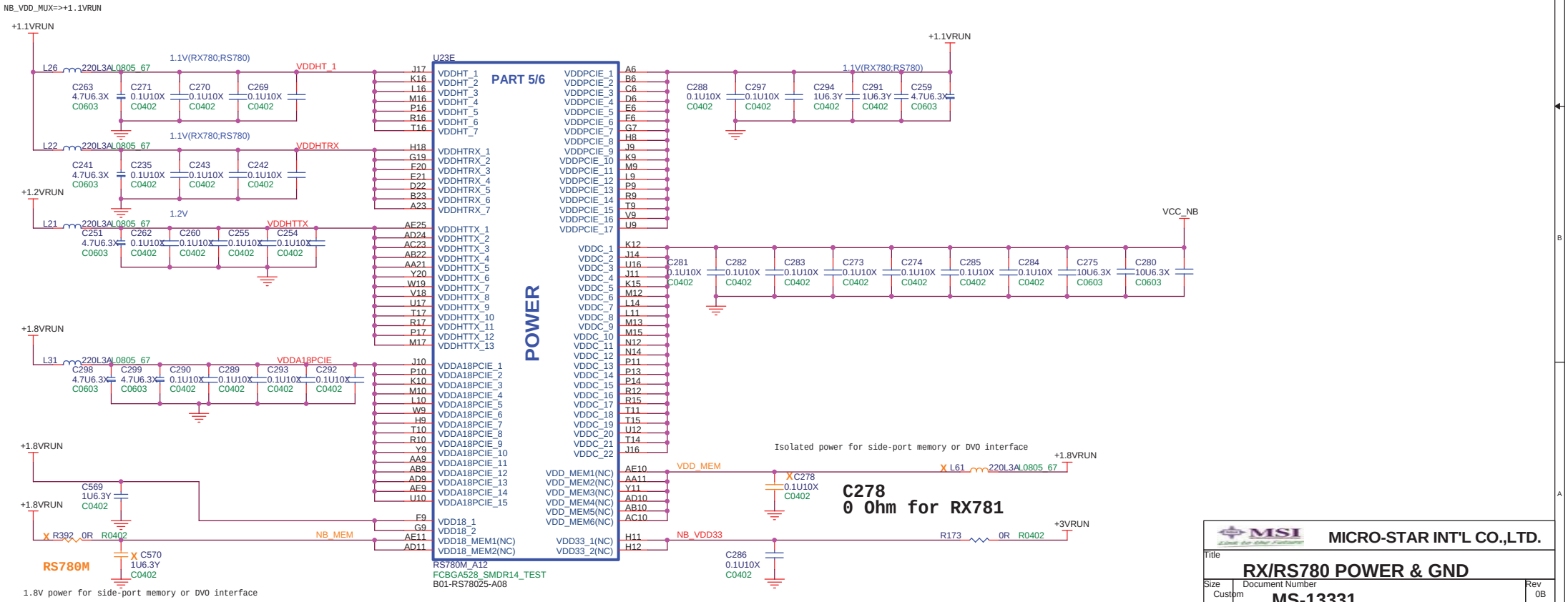
RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVDD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDDG18	+1.8V	+1.8V	+1.8V	PLLVDD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDDG33	+3.3V	NC	+3.3V	VDDLT18	+1.8V	NC	+1.8V
IOPLLVDD18	+1.8V	NC	+1.8V	VDDLT33	+3.3V	NC	NC





MICRO-STAR INT'L CO.,LTD.

Title: RX/RS780 POWER & GND

Size: Custom | Document Number: MS-13331 | Rev: 0B

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U23D

PAR 4 OF 6

SBD_MEM/DVO_I/F

AB12	MEM_A0(NC)	MEM_DQ0/DVO_VSYNC(NC)	AA18
AE16	MEM_A1(NC)	MEM_DQ1/DVO_HSYNC(NC)	AA20
V11	MEM_A2(NC)	MEM_DQ2/DVO_DE(NC)	AA19
AE15	MEM_A3(NC)	MEM_DQ3/DVO_D0(NC)	Y19
AA12	MEM_A4(NC)	MEM_DQ4(NC)	V17
AB16	MEM_A5(NC)	MEM_DQ5/DVO_D1(NC)	AA17
AB14	MEM_A6(NC)	MEM_DQ6/DVO_D2(NC)	AA15
AD14	MEM_A7(NC)	MEM_DQ7/DVO_D4(NC)	Y15
AD13	MEM_A8(NC)	MEM_DQ8/DVO_D3(NC)	AC20
AD15	MEM_A9(NC)	MEM_DQ9/DVO_D5(NC)	AD19
AC16	MEM_A10(NC)	MEM_DQ10/DVO_D6(NC)	AE22
AE13	MEM_A11(NC)	MEM_DQ11/DVO_D7(NC)	AC18
AC14	MEM_A12(NC)	MEM_DQ12(NC)	AB20
Y14	MEM_A13(NC)	MEM_DQ13/DVO_D9(NC)	AD22
		MEM_DQ14/DVO_D10(NC)	AC22
AD16	MEM_BA0(NC)	MEM_DQ15/DVO_D11(NC)	AD21
AE17	MEM_BA1(NC)		
AD17	MEM_BA2(NC)	MEM_DQS0P/DVO_IDCKP(NC)	Y17
		MEM_DQS0N/DVO_IDCKN(NC)	W18
W12	MEM_RASb(NC)	MEM_DQS1P(NC)	AD20
Y12	MEM_CASb(NC)	MEM_DQS1N(NC)	AE21
AD18	MEM_WEb(NC)		
AB13	MEM_CSb(NC)	MEM_DM0(NC)	W17
AB18	MEM_CKE(NC)	MEM_DM1/DVO_D8(NC)	AE19
V14	MEM_ODT(NC)		
		IOPLLVDD18(NC)	AE23
V15	MEM_CKP(NC)	IOPLLVDD(NC)	AE24
W14	MEM_CKN(NC)		
		IOPLLVSS(NC)	AD23
AE12	MEM_COMPP(NC)		
AD12	MEM_COMPN(NC)	MEM_VREF(NC)	AE18

RS780M_A12
FCBGA528_SMDR14_TEST
B01-RS78025-A08

please make a provision for tying to their power rails

IOPLLVDD18 — R362 0R0402 — +1.8VRUN
IOPLLVDD — R351 0R0402 — +1.1VRUN
MEM_VREF — R367 0R0402 — +1.8VRUN
R484 0R0402

C484
0 Ohm for RX781

Check the Orange in this page MS1332 whether DNI or Common

RS780M

13 SUS_STAT#_R — D11 BAS40WS DIODE_SOD323 (A / C) — A_RST# — 13,16,17,19,31,33,38,39

RS780M

13,40 NB_VSYNC# — R407 3K R0402 — +3VRUN
R502 3K R0402
13 NB_TV_C — R158 1K R0402
PA_RX7X0A1

RX780

RS740/RX780/RS780: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

STRAP_DEBUG_BUS_GPIO_ENABLEb

```
Enables the Test Debug Bus using GPIO.
1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)
PIN: RX780-->NB_TV_C (pin DFT_GPIO5) ; RS780--> VSYNC# (pin VSYNC)
```

RX740: DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

```
These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011
```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins:RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0] (configurable thru register settings only)

```
1-1-1-1-1-1 Mode L default
1-1-1-1-1-1 Mode L
2-0-2-0-2-0 Mode C2
2-0-2-0-1-1 Mode K
2-0-1-1-1-1 Mode E
1-1-1-1-1-1 Mode L
4-0-0-0-1-1 Mode C
4-0-0-0-2-0 Mode B
```

Adobe Acrobat Professional - [PA_RS780A3.pdf]

RS740/RX780/RS780 Straps:

STRAP Name	RS740	RX780	RS780	Comments
Load EPROM Straps	DFT_GPIO1	DFT_GPIO1	SUS_STAT#	Load Straps from EPROM connected through Strap and I2C_Clk pins
Strap_Debug_Bus_EN#	DFT_GPIO5	DFT_GPIO5	VSYNC	Enables debug bus over Memory I/O pins or/and GPIOs
GPPSB_LINK_Config	DFT_GPIO[4:2]	DFT_GPIO[4:2]	Register settings only	Configures A-Link and GPP
Srap_Debug_Bus_PCIE_EN#	Not applicable	DFT_GPIO0	Register settings only	Enable Debug bus over x16 PCIE interface
SidePort_EN#	DFT_GPIO0	Not applicable	HSYNC	Enables side port

Adobe Acrobat Professional - [42221_rs780m_ds_nda_0.02.pdf]

Pin Name	Type	Power Domain	Ground Domain	Functional Description
SUS_STAT#	I	VDD33	VSS	Suspend Status. SUS_STAT# from the south bridge is connected to the pin to gate the sideport memory I/Os while power is ramping up and the POWERGOOD signal to the RS780M is still low.

RS740/RX780/RS780: STRAP_SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1 : Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS780: pin HSYNC
RX780: Not Applicable
```

R406 3KR0402 — +3VRUN
13,40 NB_HSYNC# — R405 3KR0402

Adobe Acrobat Professional - [42221_rs780m_ds_nda_0.02.pdf]

Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
DAC_HSYNC	A-O	VDD33	VSS	50kΩ programmable: PU/PD/none	Display Horizontal Sync
DAC_VSYNC	A-O	VDD33	VSS	50kΩ programmable: PU/PD/none	Display Vertical Sync

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
Enables Test debug bus over PCIE bus
(Applicable to RX780 & RS780 Only)
1. Disable (can be enabled thru nbcfg register)
0 : Enable
RX780: pin DFT_GPIO0
RS780: configurable thru register setting only
```

DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

```
RX780: Enables the Test Debug Bus using PCIE bus
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable

RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
1.  Disable (RS740)  Enable (RS780)
0 : Enable (RS740)   Disable(RS780)
```

Adobe Acrobat Professional - [42223_rx780_ds_nda_0.02.pdf]

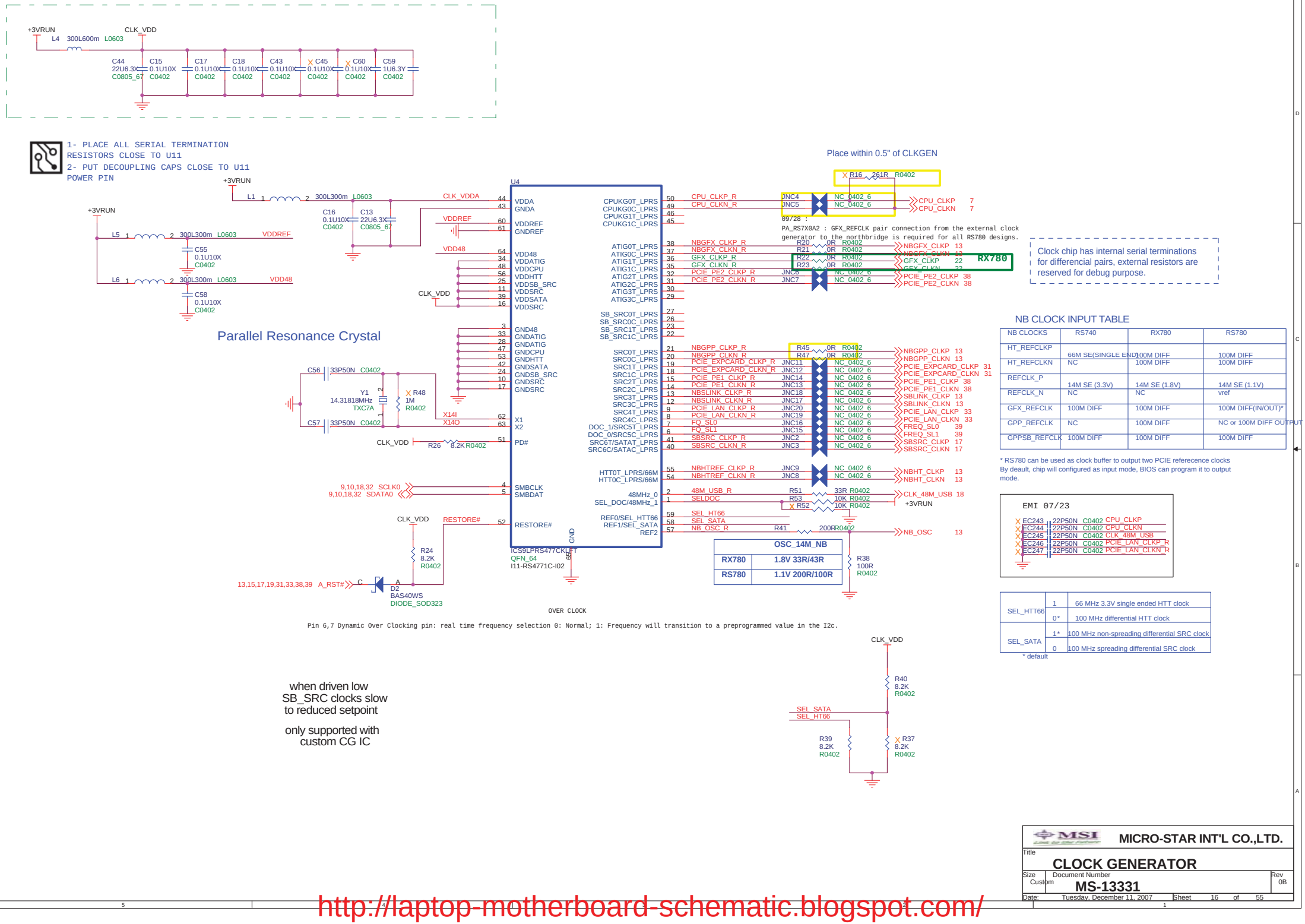
Pin Name	Type	Power Domain	Ground Domain	Integrated Termination	Functional Description
DFT_GPIO[5:0]	I/O	VDD18	VSS	Pull Up	Outputs for DFT TESTMODE. The pins cannot be used for general GPIO functions.

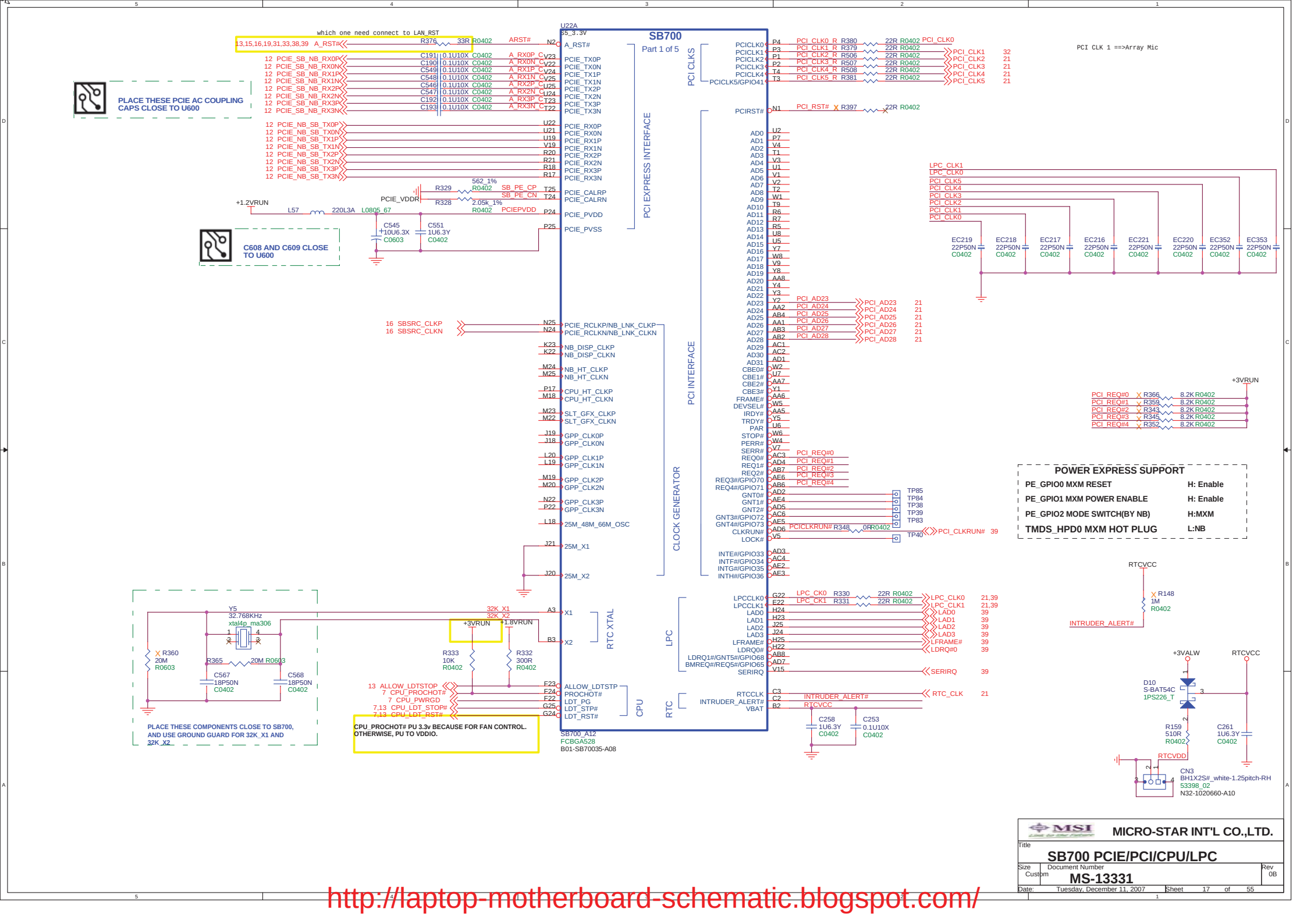
MSI MICRO-STAR INT'L CO.,LTD.

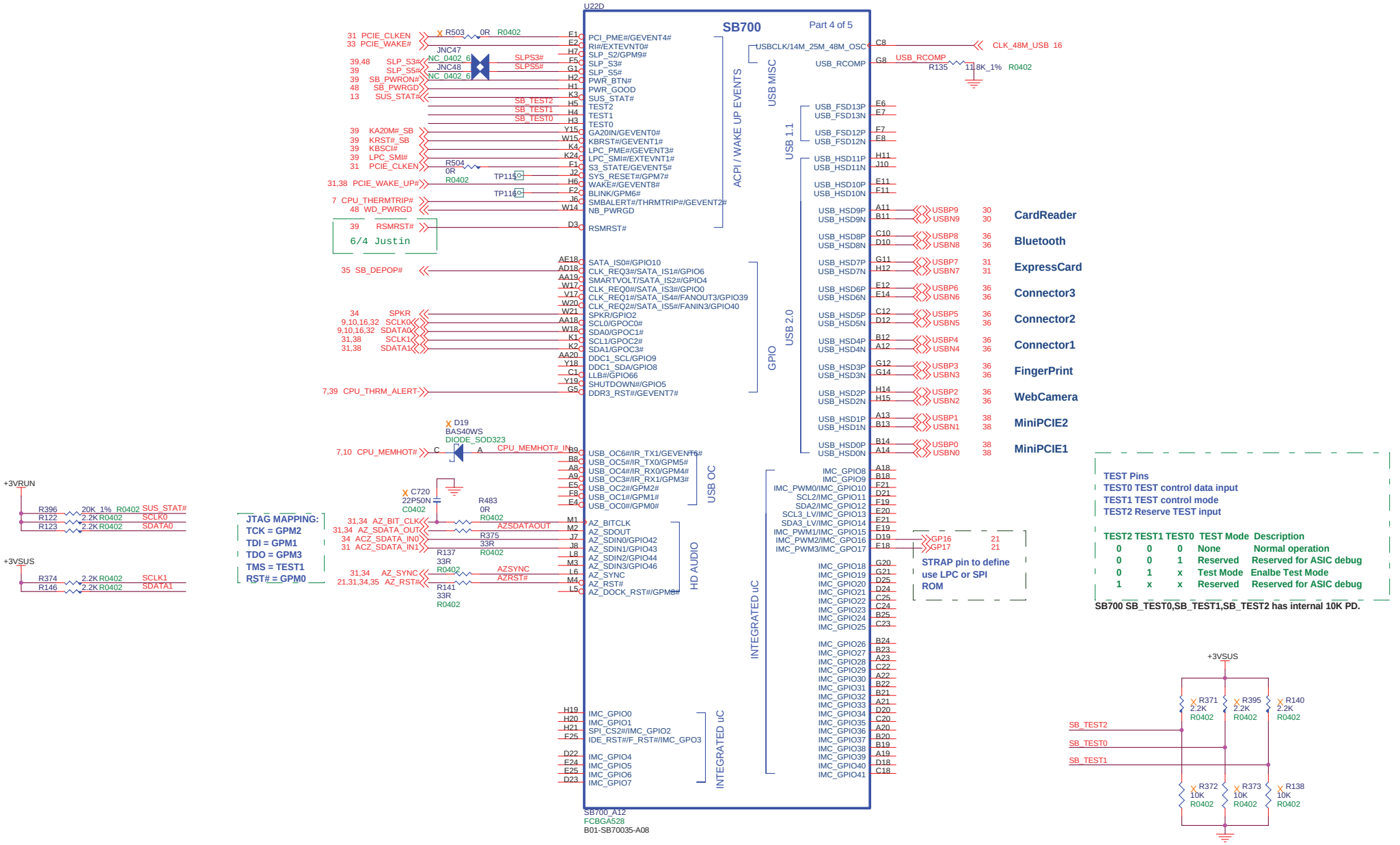
Title: RX/RS780-DVO

Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 15 of 55




SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
RTC XTAL
LPC
CPU
RTC
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO U600
C608 AND C609 CLOSE TO U600
PLACE THESE COMPONENTS CLOSE TO SB700, AND USE GROUND GUARD FOR 32K_X1 AND 32K_X2
CPU_PROCHOT# PU 3.3v BECAUSE FOR FAN CONTROL. OTHERWISE, PU TO VDDIO.
POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH(BY NB) H:MXM
TMDS_HPD0 MXM HOT PLUG L:NB
MICRO-STAR INT'L CO.,LTD.
SB700 PCIE/PCI/CPU/LPC
MS-13331
Tuesday, December 11, 2007
http://laptop-motherboard-schematic.blogspot.com/

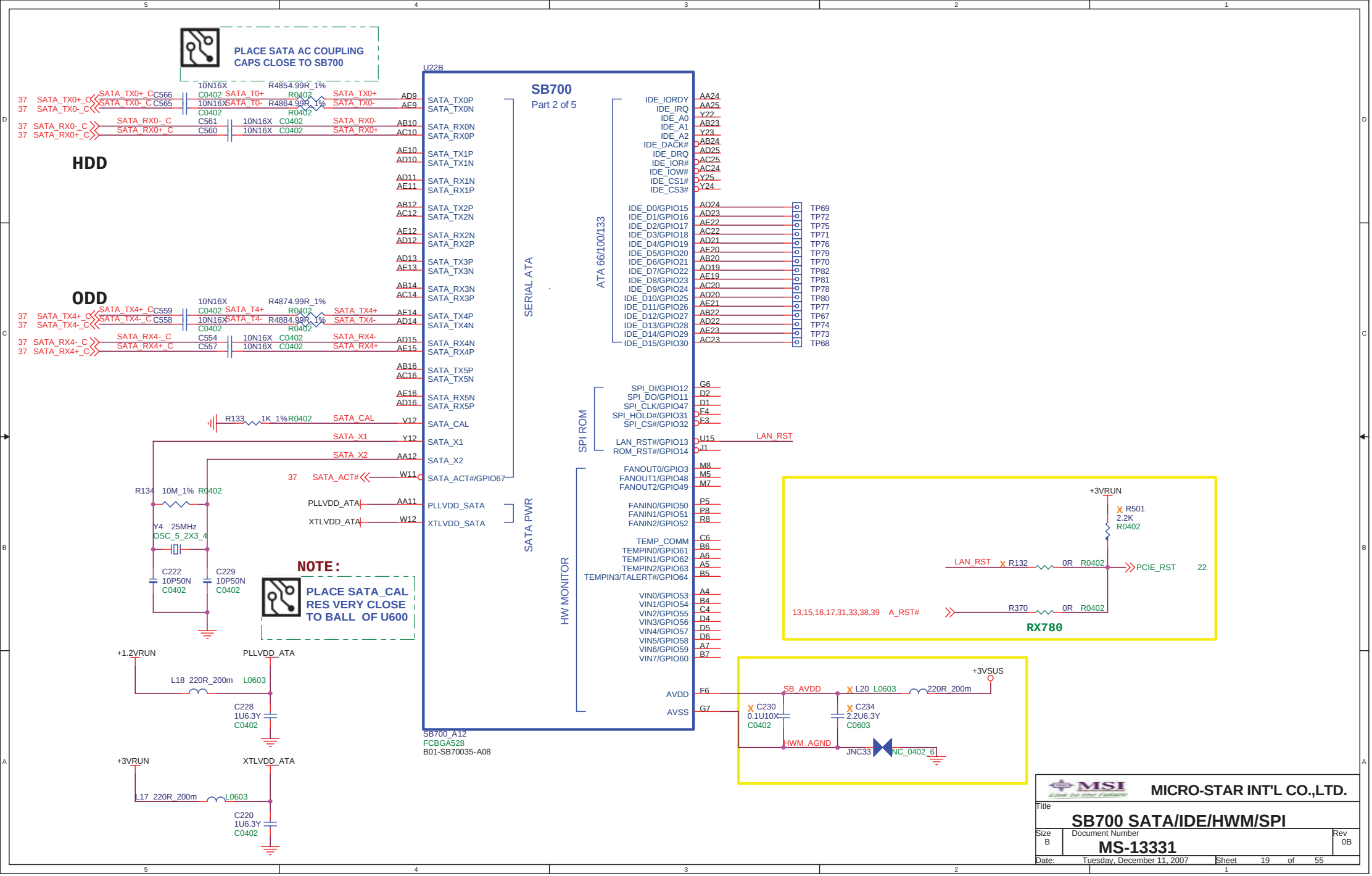


MICRO-STAR INT'L CO.,LTD.

Title: SB700 ACPI/GPIO/USB/AUDIO

Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 18 of 55



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

For SB700_A12

VDD33_18
+1.8V : FLASH MEMORY MODE(DEFAULT)
+3.3V : IDE MODE

Please make a provision for tying to +3.3V_S0

SB700
Part 3 of 5
POWER

U22C
SB700_A12
FCBGA528
B01-SB70035-A08

U22E
SB700
GROUND
Part 5 of 5
SB700_A12
FCBGA528
B01-SB70035-A08

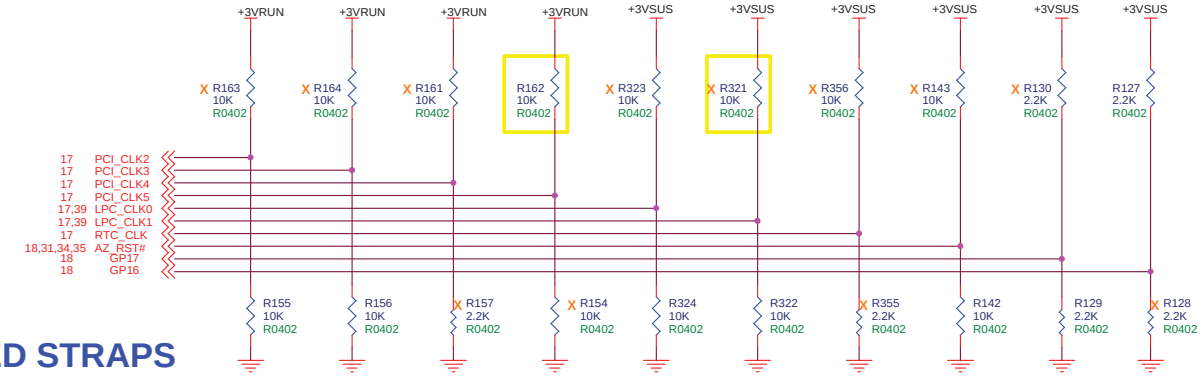
MICRO-STAR INT'L CO.,LTD.

Title: SB700 POWER & GND

Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 20 of 55

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

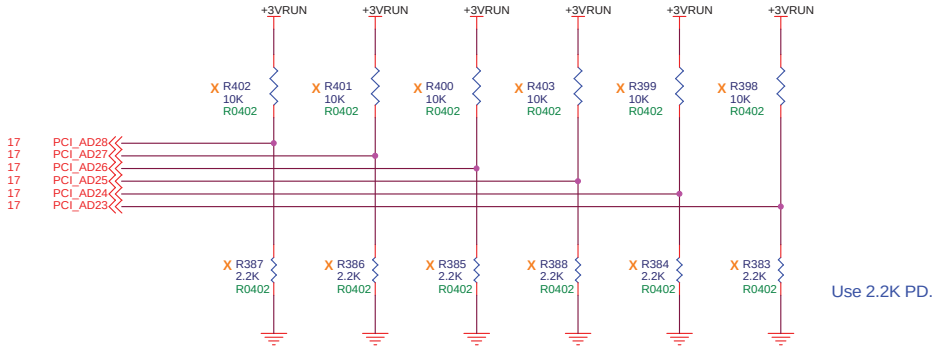


REQUIRED STRAPS

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST	GP17 GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	EC ENABLED	CLKGEN ENABLED	INTERNAL RTC DEFAULT	ENABLE PCI MEM BOOT	H,H = Reserved L,H = LPC ROM (DEFAULT) H,L = SPI ROM L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			EC DISABLED DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI MEM BOOT DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

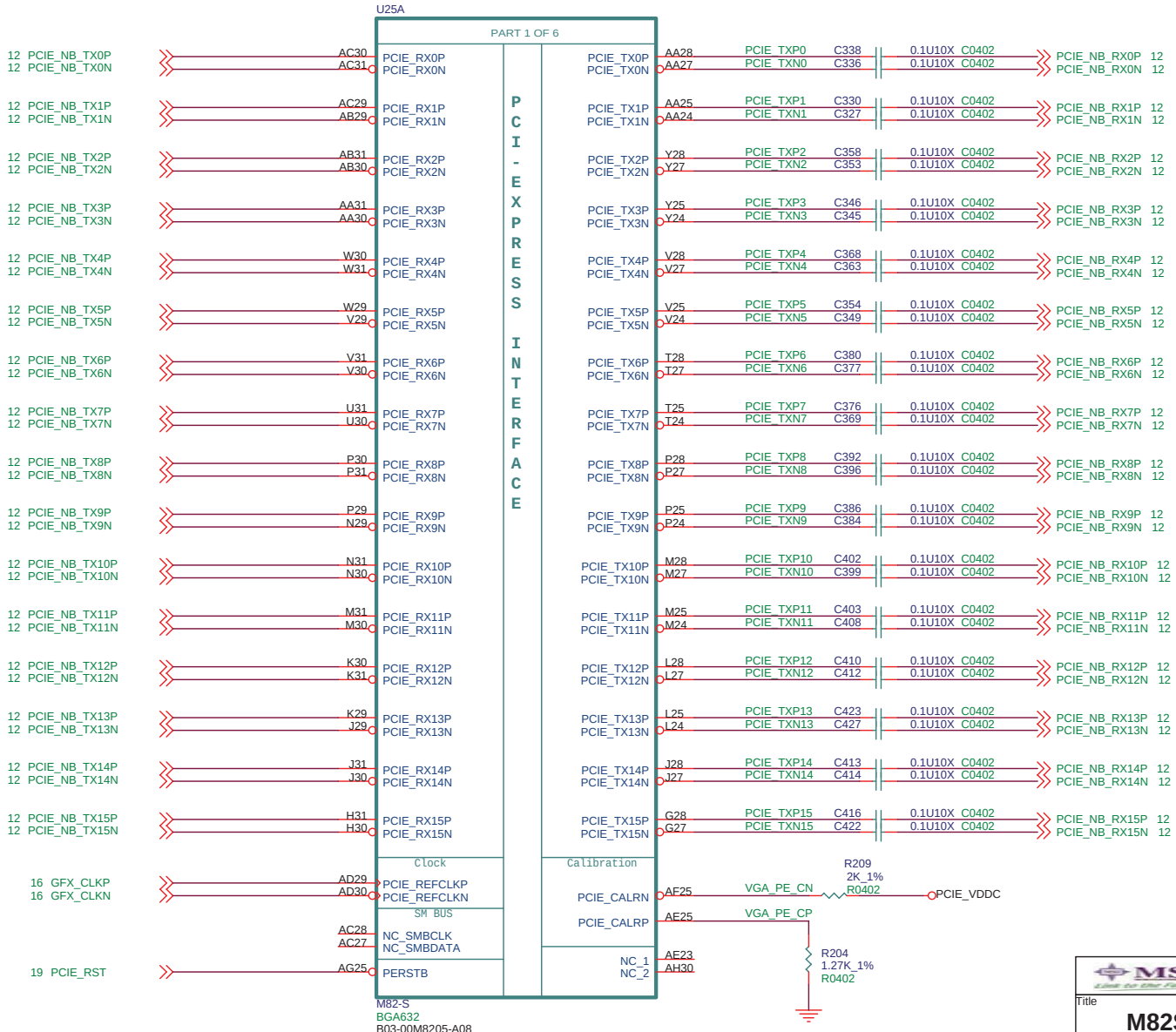
MICRO-STAR INT'L CO.,LTD.

Title: SB700 STRAPS

Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 21 of 55

MS1333



MICRO-STAR INT'L CO.,LTD.

Title: M82S PCI-E LINK

Size: B | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 22 of 55

MS1333

DVALID
1.)Transport stream data valid input or general purpose I/O
Note: Can be left unconnected if not used.
2.)This signals is also used for video capture and as an initialization pin strap.
3.)Internal use only. Other logic must not affect this signal during RESET.

PSYNC VGA_DIS(Internal pulldown)
VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space).
0 – VGA Controller capacity enabled
1 – The device will not be recognized as the system's VGA controller

THE PINS WITH TEST POINTS ARE REQUIRED TO BE ACCESSIBLE FOR DEBUG AND BOUNDRY SCAN PURPOSES USING TEST POINT VIAS IF UNUSED OR COMPONENT PADS

ENSURE DEBUG_ACCESS STRAP IS ALSO ACCESSIBLE SEE CONFIG STRAPPING PAGE

ACCESS TO ATI DEBUG PORT IS MANDATORY ON INITIAL PROTOTYPE DESIGNS

GPIO_17_THERMAL_INT
Thermal monitor interrupt.
GPIO_17_THERMAL_INT is used for ASIC temperature control. It is connected to the ALERTb signal of the thermal monitor which measures the temperature of the ASIC. If the ASIC temperature falls outside a defined range, the ALERTb signal is asserted. Low level on GPIO_17_THERMAL_INT causes M74/M72 to generate an interrupt (the polarity of this interrupt is programmable – the default is active low). Software can then activate the implemented temperature control scheme.

Power Control signals control the core voltage regulator.
At Reset, these signals will be inputs with weak internal pull-down resistors.
VBIOS can define these signals to be either 3.3V outputs or open drain outputs.
The output state (high/low) of these signals is programmable for each PowerPlay state.

Back Bias (BB) control:
When GPIO_21_BB_EN = 0V then back bias is disabled on the PCB (ie BPP=VDDC and BBN=VSS).
When GIO_21_BB_EN = 3.3V then back bias is enabled on the PCB.
Can function as a GPIO if not required for BB control.

GPIO_22_ROMCSB
BIOS_ROM_EN
Enable external BIOS ROM device
0 - Disable external BIOS ROM device
1 - Enable external BIOS ROM device

GPIO_23_CLKREQB DRIVES LOW DURING RESET

VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = .6V)

PLACE VREF DIVIDER AND CAP CLOSE TO ASIC

U25B
PART 2 OF 6
M82-S
BGA632
B03-00M8205-A08

HDMI

CRT

WITH M8x ASIC INSTALL M8x STRAP RESISTORS AND DO NOT INSTALL M7x STRAP RESISTORS

IF HOT PLUG DETECT IS NOT REQUIRED REMOVE ALL THIS LOGIC EXCEPT FOR 100K PULL DOWN

OPTIONAL 0 OHM STRAPS TO GROUND FOR RB,GB,BB AND R2B,G2B,B2B SEE DAC1_RGB AND DAC2_RGB SHEETS

PLACE OR RESISTORS CLOSE TO ASIC

Close to M82S
Cap close to thermal sensor
M82S

3.3V TO 5V LEVEL SHIFT LOGIC REQUIRED
IF DDC1,DDC2 USED ON M8x OR DDC1,DDC2,DDC3 USED ON M7x
DDC3,DDC4 ARE 5V TOLERANT ON M8x

CRT	3.3V	
LVDS	3.3V	
HDMI	5V	

MICRO-STAR INT'L CO.,LTD.

Title: M82S I/O
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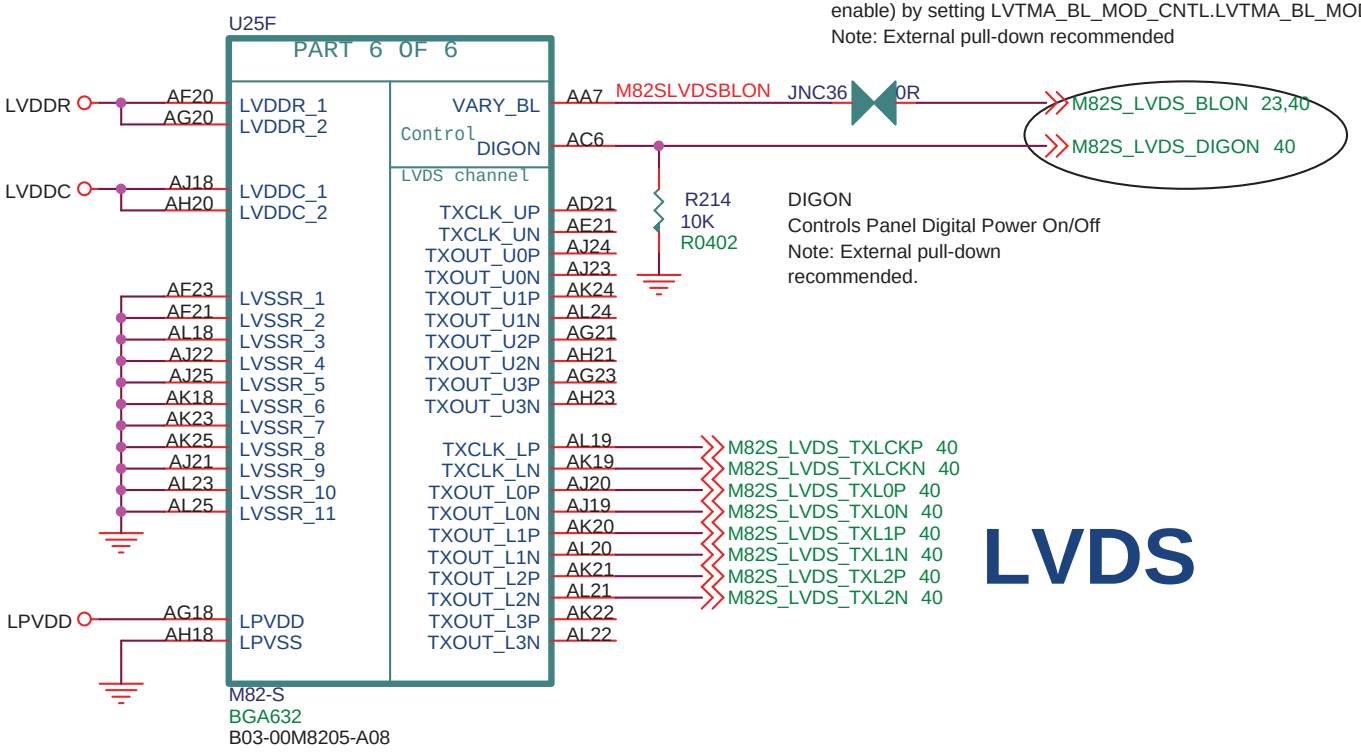
MS1333

VARY_BL
LCD PWM (Pulse Width Modulated) output to adjust LCD brightness. Active high.
LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_LEVEL can be used to control the backlight level by means of pulse width modulation.
Alternatively, VARY_BL can be used to control backlight on/off (backlight enable) by setting LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_EN = 0.
Note: External pull-down recommended



DIGON
Controls Panel Digital Power On/Off
Note: External pull-down recommended.

LVDS

MICRO-STAR INT'L CO.,LTD.		
Title: M82S LVDS		
Size: Custom	Document Number: MS-13331	Rev: 0B
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MS1333

U25E

Part 5 of 6

PCI-Express GND

PCIE_VSS_1 … PCIE_VSS_32

VSS_1 … VSS_102

CORE GND

M82-S
BGA632
B03-00M8205-A08

U25D

PART 4 OF 6

VDDR1_1 … VDDR1_18

VDD_CT_1 … VDD_CT_8

VDDR3_1 … VDDR3_4

VDDR4_1, VDDR4_2

VDDR5_1, VDDR5_2

RSVD_1 … RSVD_4

VDDRH_1, VDDRH_2

VSSRH_1, VSSRH_2

BBN_1, BBN_2

BBP_1, BBP_2

I/O Internal

Memory I/O

Memory Clock I/O

Back Bias

POWER

PCI-Express

Core

PCIE_VDDR_1 … PCIE_VDDR_8

PCIE_VDDC_1 … PCIE_VDDC_12

VDDC_1 … VDDC_33

VDDCI_1 … VDDCI_4

M82S_PCIE_VDDR

PCIE_VDDC

M82S_VDD_CORE

M82S_VDDCI

M82-S
BGA632
B03-00M8205-A08

1.8VGA

3.3V_DELAY

(3.3V @ 50MA VDDR3)

+VDDR4

+VDDR5

VDD_CT

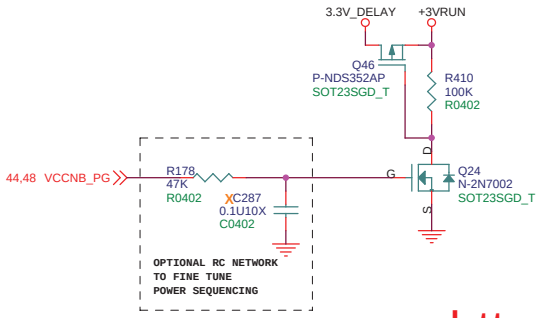
VDD_MEM_CLK0

VDD_MEM_CLK1

-BBN
VSS-1.0V to VSS

+BBP
VDDC to VDDC+1.0V

VDDC>VDDR1>PCIE_VDDC>VDDR3



Back Bias Pins
Back bias is a new feature which will require additional engineering verification and characterization. Prototype designs need to provide the option
to disable/by-pass this feature.

+BBP
Back Bias Enabled: (GPIO_21_BB_EN = 3.3V): 1.5V or 1.8V
Back Bias Disabled: (GPIO_21_BB_EN = 0V): VDDC
Connect to VBBP back bias regulator / generator.
If back bias is not used, connect directly to VDDC.

-BBN
Back Bias Enabled: (GPIO_21_BB_EN = 3.3V): -0.55V or -0.85V
Back Bias Disabled: (GPIO_21_BB_EN = 0V): VSS
Connect to VBBN back bias regulator / generator.
If back bias is not used connect directly to VSS.

VDD_CT (External TMDS enabled External TMDS enabled 120mA)
Level translation between core and I/O, excluding memory receivers.
VDD_CT must remain powered whenever the ASIC is powered.

VDDR4
DVOA_MSB_VMODE register bit; '1' - 3.3V(default); '0' - 1.8V

VDDR5
DVOA_LSB_VMODE register bit; '1' -3.3V(default); '0' - 1.8V

VDDRH
Dedicated power pins for memory clock pads for each channel.
Should have the same voltage level as VDDR1.

MICRO-STAR INT'L CO.,LTD.

Title: M82S PWR&GND

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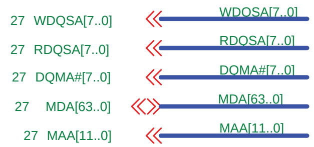
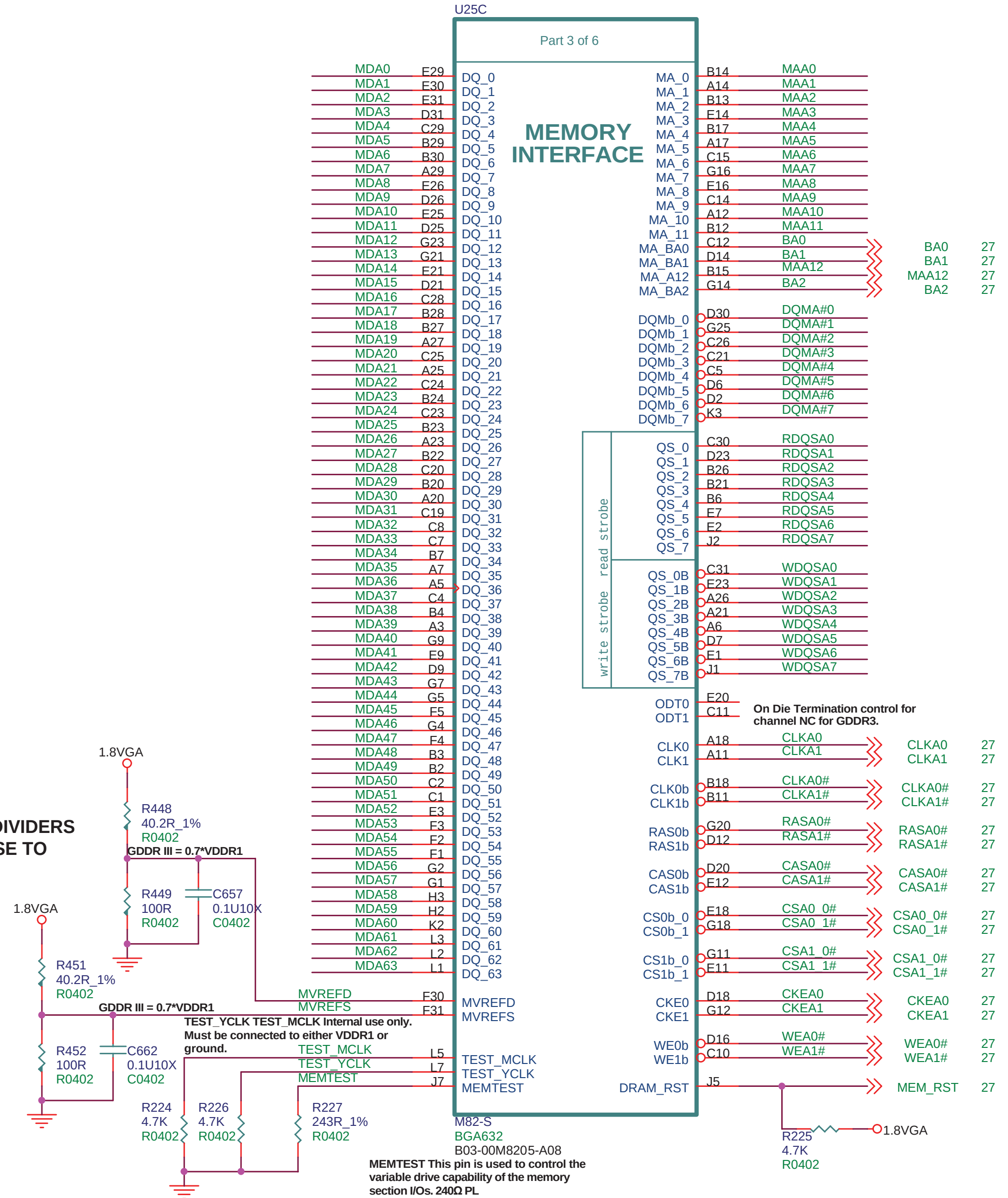


PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R


U25C
Part 3 of 6
MEMORY INTERFACE
MDA0 E29 DQ_0
MDA1 E30 DQ_1
MDA2 E31 DQ_2
MDA3 D31 DQ_3
MDA4 C29 DQ_4
MDA5 B29 DQ_5
MDA6 B30 DQ_6
MDA7 A29 DQ_7
MDA8 E26 DQ_8
MDA9 D26 DQ_9
MDA10 E25 DQ_10
MDA11 D25 DQ_11
MDA12 G23 DQ_12
MDA13 G21 DQ_13
MDA14 E21 DQ_14
MDA15 D21 DQ_15
MDA16 C28 DQ_16
MDA17 B28 DQ_17
MDA18 B27 DQ_18
MDA19 A27 DQ_19
MDA20 C25 DQ_20
MDA21 A25 DQ_21
MDA22 C24 DQ_22
MDA23 B24 DQ_23
MDA24 C23 DQ_24
MDA25 B23 DQ_25
MDA26 A23 DQ_26
MDA27 B22 DQ_27
MDA28 C20 DQ_28
MDA29 B20 DQ_29
MDA30 A20 DQ_30
MDA31 C19 DQ_31
MDA32 C8 DQ_32
MDA33 C7 DQ_33
MDA34 B7 DQ_34
MDA35 A7 DQ_35
MDA36 A5 DQ_36
MDA37 C4 DQ_37
MDA38 B4 DQ_38
MDA39 A3 DQ_39
MDA40 G9 DQ_40
MDA41 E9 DQ_41
MDA42 D9 DQ_42
MDA43 G7 DQ_43
MDA44 G5 DQ_44
MDA45 F5 DQ_45
MDA46 G4 DQ_46
MDA47 F4 DQ_47
MDA48 B3 DQ_48
MDA49 B2 DQ_49
MDA50 C2 DQ_50
MDA51 C1 DQ_51
MDA52 E3 DQ_52
MDA53 F3 DQ_53
MDA54 F2 DQ_54
MDA55 F1 DQ_55
MDA56 G2 DQ_56
MDA57 G1 DQ_57
MDA58 H3 DQ_58
MDA59 H2 DQ_59
MDA60 K2 DQ_60
MDA61 L3 DQ_61
MDA62 L2 DQ_62
MDA63 L1 DQ_63
MVREFD F30 MVREFD
MVREFS F31 MVREFS
TEST_MCLK L5 TEST_MCLK
TEST_YCLK L7 TEST_YCLK
MEMTEST J7 MEMTEST
MA_0 B14 MAA0
MA_1 A14 MAA1
MA_2 B13 MAA2
MA_3 E14 MAA3
MA_4 B17 MAA4
MA_5 A17 MAA5
MA_6 C15 MAA6
MA_7 G16 MAA7
MA_8 E16 MAA8
MA_9 C14 MAA9
MA_10 A12 MAA10
MA_11 B12 MAA11
MA_BA0 C12 BA0 BA0 27
MA_BA1 D14 BA1 BA1 27
MA_A12 B15 MAA12 MAA12 27
MA_BA2 G14 BA2 BA2 27
DQMb_0 D30 DQMA#0
DQMb_1 G25 DQMA#1
DQMb_2 C26 DQMA#2
DQMb_3 C21 DQMA#3
DQMb_4 C5 DQMA#4
DQMb_5 D6 DQMA#5
DQMb_6 D2 DQMA#6
DQMb_7 K3 DQMA#7
read strobe
QS_0 C30 RDQSA0
QS_1 D23 RDQSA1
QS_2 B26 RDQSA2
QS_3 B21 RDQSA3
QS_4 B6 RDQSA4
QS_5 E7 RDQSA5
QS_6 E2 RDQSA6
QS_7 J2 RDQSA7
write strobe
QS_0B C31 WDQSA0
QS_1B E23 WDQSA1
QS_2B A26 WDQSA2
QS_3B A21 WDQSA3
QS_4B A6 WDQSA4
QS_5B D7 WDQSA5
QS_6B E1 WDQSA6
QS_7B J1 WDQSA7
ODT0 E20
ODT1 C11
On Die Termination control for channel NC for GDDR3.
CLK0 A18 CLKA0 CLKA0 27
CLK1 A11 CLKA1 CLKA1 27
CLK0b B18 CLKA0# CLKA0# 27
CLK1b B11 CLKA1# CLKA1# 27
RAS0b G20 RASA0# RASA0# 27
RAS1b D12 RASA1# RASA1# 27
CAS0b D20 CASA0# CASA0# 27
CAS1b E12 CASA1# CASA1# 27
CS0b_0 E18 CSA0_0# CSA0_0# 27
CS0b_1 G18 CSA0_1# CSA0_1# 27
CS1b_0 G11 CSA1_0# CSA1_0# 27
CS1b_1 E11 CSA1_1# CSA1_1# 27
CKE0 D18 CKEA0 CKEA0 27
CKE1 G12 CKEA1 CKEA1 27
WE0b D16 WEA0# WEA0# 27
WE1b C10 WEA1# WEA1# 27
DRAM_RST J5 MEM_RST 27
R225 4.7K R0402 1.8VGA
M82-S
BGA632
B03-00M8205-A08
1.8VGA
R448 40.2R_1% R0402
GDDR III = 0.7*VDDR1
R449 100R R0402
C657 0.1U10X C0402
1.8VGA
R451 40.2R_1% R0402
GDDR III = 0.7*VDDR1
R452 100R R0402
C662 0.1U10X C0402
TEST_YCLK TEST_MCLK Internal use only. Must be connected to either VDDR1 or ground.
R224 4.7K R0402
R226 4.7K R0402
R227 243R_1% R0402
MEMTEST This pin is used to control the variable drive capability of the memory section I/Os. 240Ω PL

FOR DUAL RANK CONNECTIONS USE THE CSxB_1 CHIP SELECT PINS

MSI	MICRO-STAR INT'L CO.,LTD.	
Title	M82S MEMORY	
Size B	Document Number MS-13331	Rev 0B
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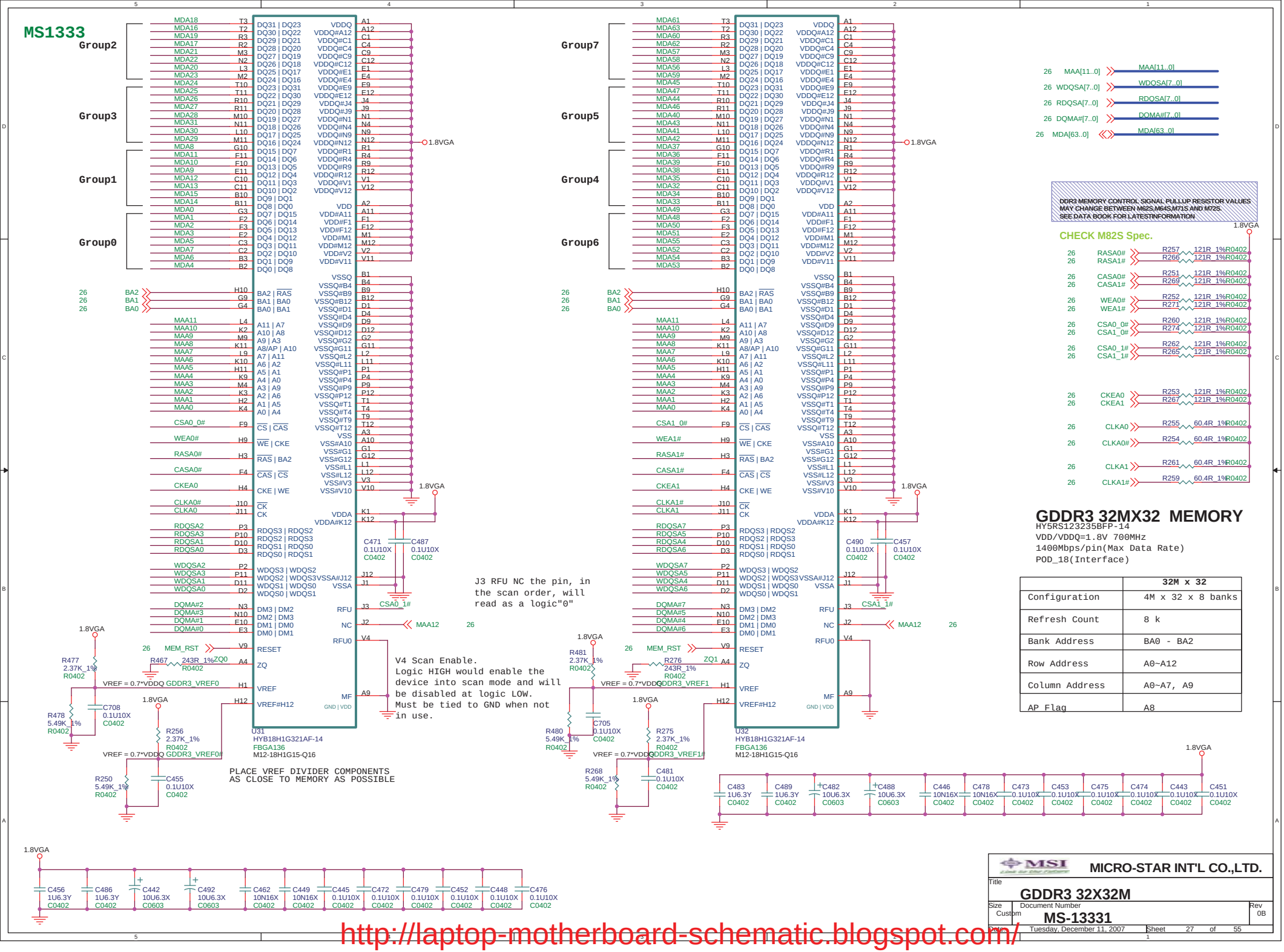

GDDR3 32MX32 MEMORY

HY5RS123235BFP-14
VDD/VDDQ=1.8V 700MHz
1400Mbps/pin(Max Data Rate)
POD_18(Interface)

	32M x 32
Configuration	4M x 32 x 8 banks
Refresh Count	8 k
Bank Address	BA0 - BA2
Row Address	A0~A12
Column Address	A0~A7, A9
AP Flag	A8

MICRO-STAR INT'L CO.,LTD.

Title: GDDR3 32X32M

Size: Custom | Document Number: MS-13331 | Rev: 0B

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MS1333

1.8VGA → L33 300L300m L0603 → LVDDR (3.3V @ 250MA LVDDR)
C306 10U6.3X C0603, C313 1U6.3Y C0402, C321 0.1U10X C0402

X R192 0R R0603

1.8VGA → L35 60L1_1000m L1206_113 → LVDDC (1.8V @ 100MA LVDDC) (1.8V @ 400MA LVDDC,LVDDR)
C320 10U6.3X C0603, C334 0.1U10X C0402, C337 0.1U10X C0402

1.8VGA → L32 220R_200m L0603 → LPVDD (1.8V @ 20MA LPVDD)
C302 10U6.3X C0603, C319 1U6.3Y C0402, C329 0.1U10X C0402 *

1.8VGA → L37 220R_200m L0603 → DPLL_PVDD (1.8V @ 40MA DPLL_PVDD)
C309 10U6.3X C0603, C315 1U6.3Y C0402, C332 0.1U10X C0402 *

1.8VGA → L39 220R_200m L0603 → PCIE_PVDD (1.8V @ 40MA PCIE_PVDD)
C324 10U6.3X C0603, C331 1U6.3Y C0402, C335 0.1U10X C0402 *

3.3V_DELAY → L38 220R_200m L0603 → A2VDD (3.3V @ 135MA A2VDD)
C304 10U6.3X C0603, C318 0.1U10X C0402, C339 1000P50X C0402

1.8VGA → L67 220R_200m L0603 → A2VDDQ (1.8V @ 2MA A2VDDQ)
C590 10U6.3X C0603, C597 1U6.3Y C0402, C602 0.1U10X C0402 *

1.8VGA → L68 220R_200m L0603 → VDDDI (1.8V @ 100MA VDD1DI,VDD2DI)
C592 10U6.3X C0603, C599 0.1U10X C0402, C608 1000P50X C0402 *

1.8VGA → L69 220R_200m L0603 → M82S_AVDD (1.8V @ 65MA AVDD)
C593 10U6.3X C0603, C598 0.1U10X C0402, C606 1000P50X C0402

+1.1VRUN → L70 220R_200m L0603 → DPA_VDDR (1.8V @ 100MA EACH SINGLE LINK) (1.1V @ 200MA EACH SINGLE LINK)
C594 10U6.3X C0603, C600 1U6.3Y C0402, C609 0.1U10X C0402

+1.1VRUN → L66 220R_200m L0603 → DPB_VDDR
C591 10U6.3X C0603, C596 1U6.3Y C0402, C603 0.1U10X C0402

1.8VGA → L71 220R_200m L0603 → DPA_PVDD (1.8V @ 20MA TPVDD EACH SINGLE LINK)
C595 10U6.3X C0603, C601 0.1U10X C0402, C610 1000P50X C0402 *

1.8VGA → L42 220R_200m L0603 → VDD_CT (VDD_CT 1.8V @ 110MA (VDD_CT)
C411 10U6.3X C0603, C407 0.1U10X C0402, C401 1000P50X C0402

1.8VGA → L30 60L1_1000m L1206_113 → M82S_PCIE_VDDR (1.8V @ 400MA PCIE_VDDR)
C307 10U6.3X C0603, C314 1U6.3Y C0402, C322 0.1U10X C0402

PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

1.8VGA → L73 220R_200m L0603 → VDD_MEM_CLK0 (1.8V @ MA VDDRHA_1 INCLUDED IN VDDR1)
C682 10U6.3X C0603, C683 1U6.3Y C0402, C684 0.1U10X C0402

1.8VGA → L44 220R_200m L0603 → VDD_MEM_CLK1 (1.8V @ MA VDDRHA_2 INCLUDED IN VDDR1)
C431 10U6.3X C0603, C437 1U6.3Y C0402, C436 0.1U10X C0402

FOR M7x
INSTALL LVDDR TO +3.3V AND
LVDDC TO 1.8V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M8x
INSTALL LVDDR AND LVDDC TO +1.8V
WITH THE ONE LVDDC FILTER
DO NOT INSTALL LVDDR FILTER
INSTALL STRAP RESISTOR

FOR M8x
INSTALL DPA_VDDR TO +1.1V AND
DPB_VDDR TO +1.1V
WITH SEPARATE FILTERS
DO NOT INSTALL STRAP RESISTOR
FOR M7x
INSTALL DPA_VDDR AND DPB_VDDR TO +1.8V
WITH THE ONE DPA_VDDR FILTER
DO NOT INSTALL DPB_VDDR FILTER
INSTALL STRAP RESISTOR

* PLACE ALL DECOUPLING CAPS CLOSE TO THE ASIC AND RUN DEDICATED TRACES FROM ASIC PINS TO JOIN THE GROUND PLANE WITH ONE VIA AT THE CAP

+1.1VRUN → L63 220L3A L0805_67 → PCIE_VDDC (PCIE_VDDC 1.1V @ 1A)
C575 10U6.3X C0603, C584 1U6.3Y C0402, C359 0.1U10X C0402
C398 1U6.3Y C0402, C370 1U6.3Y C0402, C387 1U6.3Y C0402

L36 220R_200m L0603 → DPLL_VDDC (DPLL_VDDC 1.1V @ 100 MA)
C310 10U6.3X C0603, C316 1U6.3Y C0402 *

M82S_VDD_CORE → L45 300L300m L0603 → MPVDD (.95V-1.1V @ 230MA MPVDD)
C435 10U6.3X C0603, C438 1U6.3Y C0402, C439 0.1U10X C0402 *

THE OPTIMAL +BBP OFFSET VOLTAGE (POWERPLAY VDDC MINUS 1.5V OR 1.8V RAIL) IS YET TO BE DETERMINED

THE OPTIMAL -BBN OFFSET VOLTAGE (0V MINUS -.6V TO -.9V) IS YET TO BE DETERMINED BUT MAX1673 DIVIDER RESISTORS MUST BE ADJUSTED FOR THE SAME OFFSET AS +BBP

BB_ENA = 0V FOR BACK BIASING DISABLED
MAX1673 SHUTDOWN
-BBN = 0V VIA MAX1673 INTERNAL 1 OHM TO GROUND
N FET A = OFF, P FET B = OFF, N FET C = ON
+BBP = VDD_CORE

1.8VGA → L80 220R_200m L0603 → DPB_PVDD
C724 0.1U10X C0402, C725 1000P50X C0402

23 BB_ENA

M82S_VDD_CORE (+1.8V 0R +1.1V @ 1A MAX)
+5VRUN
1.8VGA
X Q28 N-SI2304DS SOT23SGD_T
X Q29 P-SI2301DS SOT23SGD_T
X R216 100K R0402
FET C 1.7A
FET B 1.8A
M82S_VDD_CORE
R213 0R R0402
X PQ28 N-2N7002 SOT23SGD_T
X R203 10K R0402
+BBP
X C366 1U6.3Y C0402

+3VRUN
X U16 MAX1673ESA SOIC8
LIN/SKIP# IN
CAP+ GND
CAP- FB
SHDN# OUT
X C333 2.2U6.3Y C0603 BB_ENA
X C325 10U6.3X C0603
X R194 100K R0402
X R200 17.4K_1% R0402
-BBN
X C343 10U6.3X C0603
X C342 10U6.3X C0603
R206 0R R0402

-BB_VGA= -(+3VRUN) * R2138 / R2134

BB_ENA = +3.3V FOR BACK BIASING ENABLED
MAX1673 ENABLED
-BBN = -.85V
N FET A = ON, P FET B = ON, N FET C = OFF
+BBP = +1.8V

MICRO-STAR INT'L CO.,LTD.

Title: M82S_PWR_&_FILTER
Size: Custom | Document Number: MS-13331 | Rev: 0B
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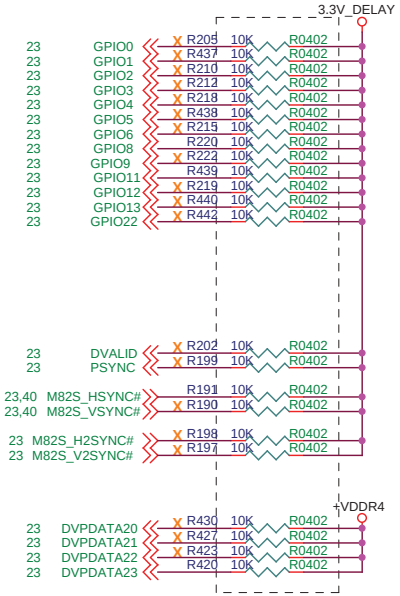
MS1333

CHECK M82S Spec. and Reference Schematic and ATi FAE



Only populate the required straps, see table and databook

GPIO22=0 GPIO_9 GPIO_[13:11]= CONFIG[3:0]
a) If BIOS_ROM_EN = 1, then Config[3:0] defines the ROM type. See "ROM Configurations"
b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. (Config 3 = don't care).

R440 R219 R439

Size of the primary memory apertures	CONFIG[3:0]
128MB	x000
256MB	x001
64MB	x010
32MB	x011
512MB	x100
1GB	x101
2GB	x110
4GB	x111

DVPDATA23 R420	DVPDATA22 R423	DVPDATA21 R427	MEM_TYPE
0	0	0	Hynix 16MX32
0	0	1	
0	1	0	
0	1	1	
1	0	0	QIMONDA 32MX32
1	0	1	SANGSUNG 32MX32
1	1	0	
1	1	1	

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED
(DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO	NA	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	M82S_VSYNC#	IGNORE VIP DEVICE STRAPS = LOW	0	0
BIF_VGA DIS	PSYNC	VGA ENABLED = LOW	0	0
BIF_HDMI_EN	M82S_HSYNC#	HDMI ENABLE = HIGHT (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE

GPIO2 GPIO3 DVALID H2SYNC V2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GENERICC GPIO21_BB_EN GPIO_28_TDO

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

COMPONENTS SHOWN ARE EXAMPLES ONLY AND NOT NECESSARILY QUALIFIED

MICRO-STAR INT'L CO.,LTD.

Title: M82S CONGIF STARP

Size: B | Document Number: MS-13331 | Rev: 0B

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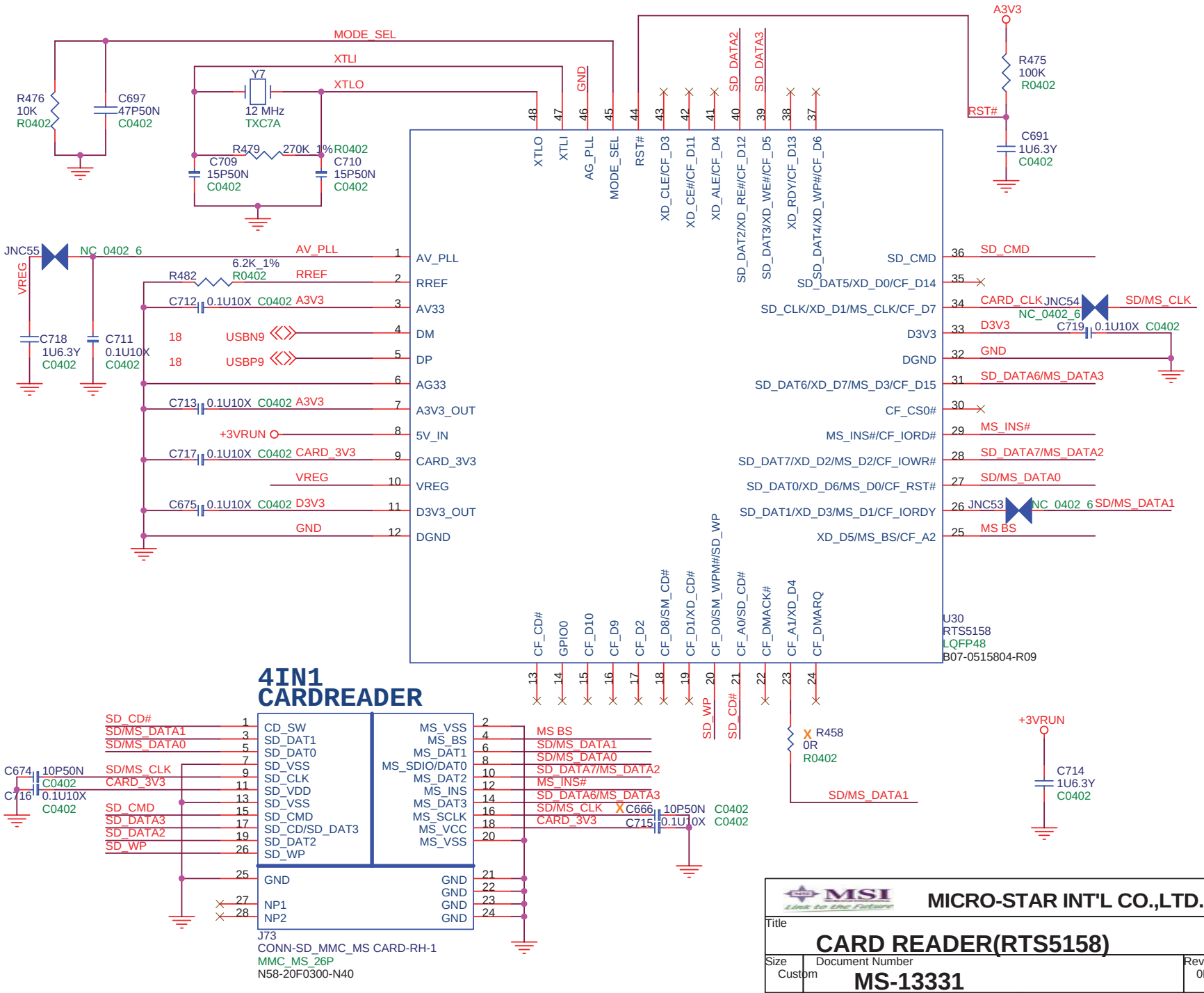
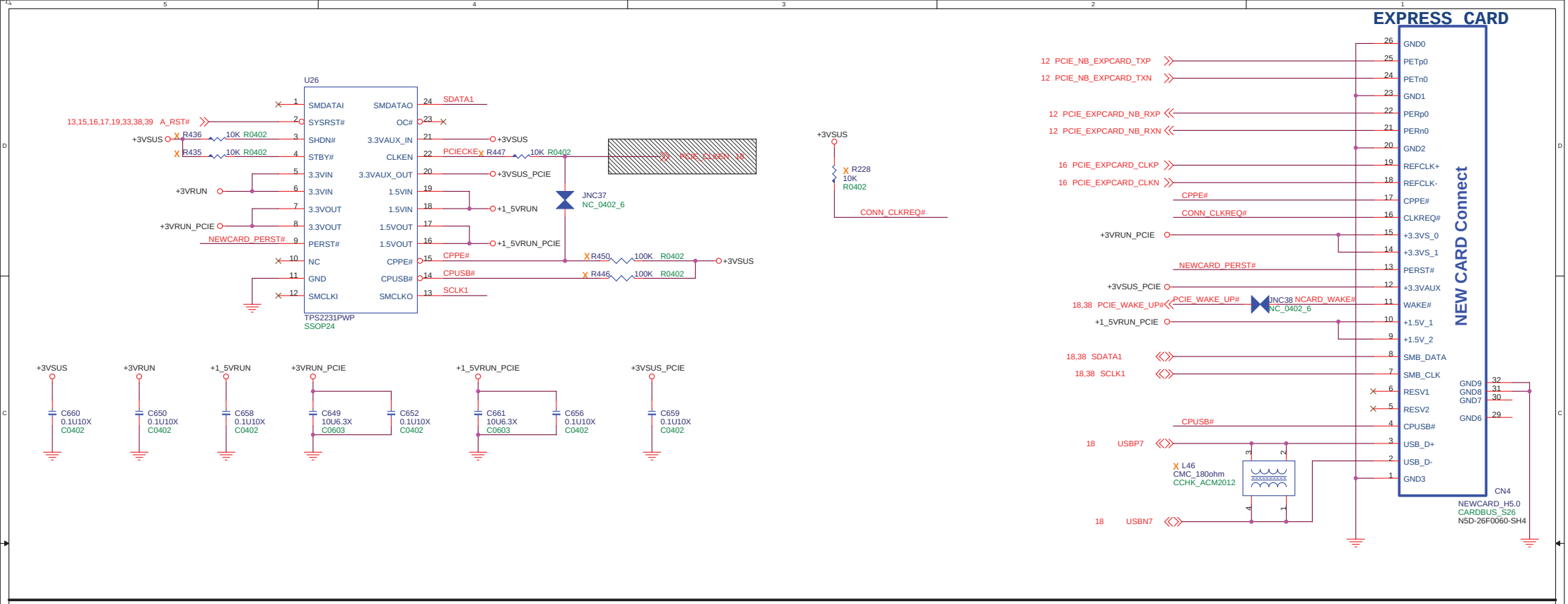


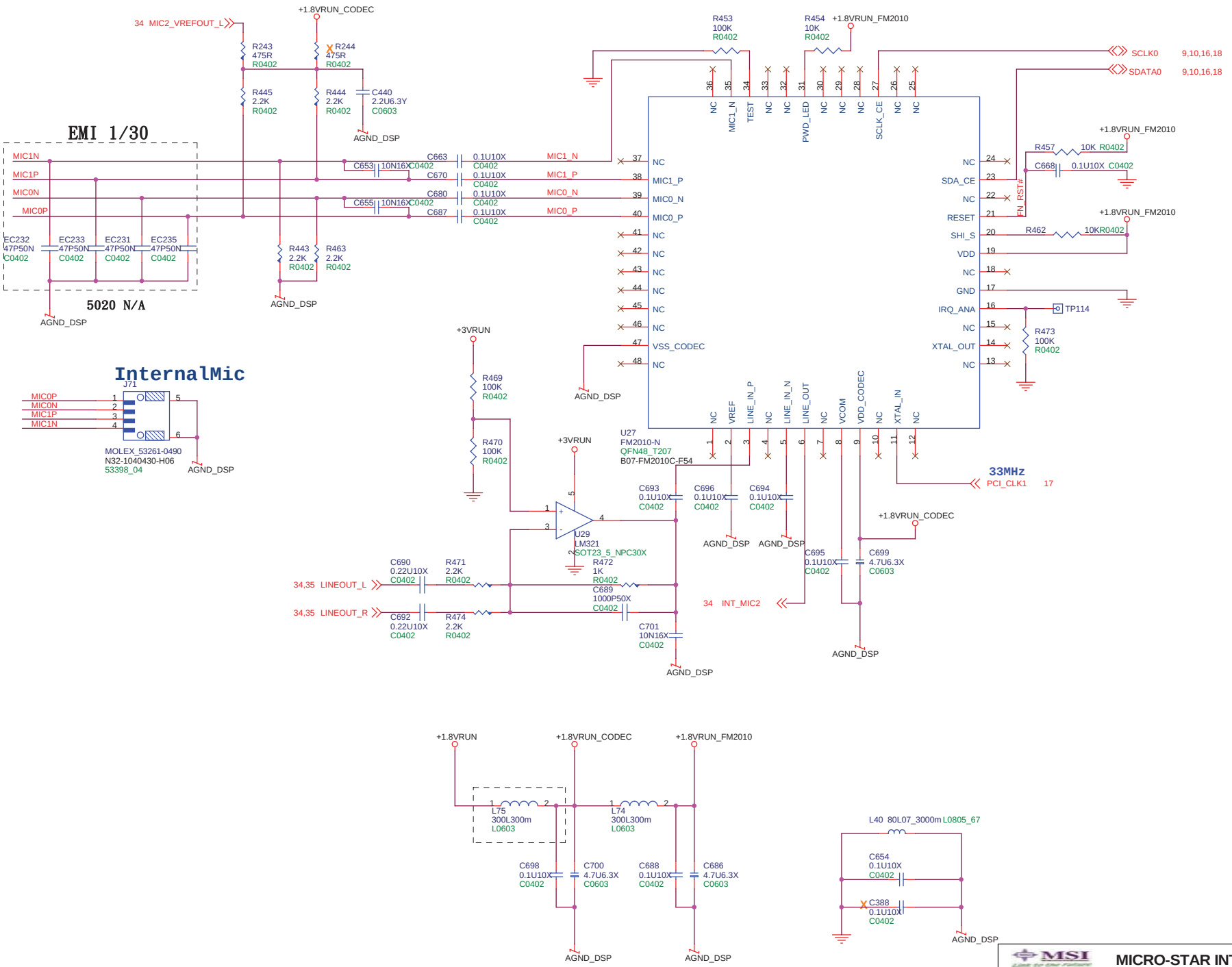


MICRO-STAR INT'L CO.,LTD.

Title: NEW CARD & MDC

Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 31 of 55



Company	MICRO-STAR INT'L CO.,LTD.
Title	Array Mic FM2010
Size	Custom
Document Number	MS-13331
Rev	0B
Date	Tuesday, December 11, 2007
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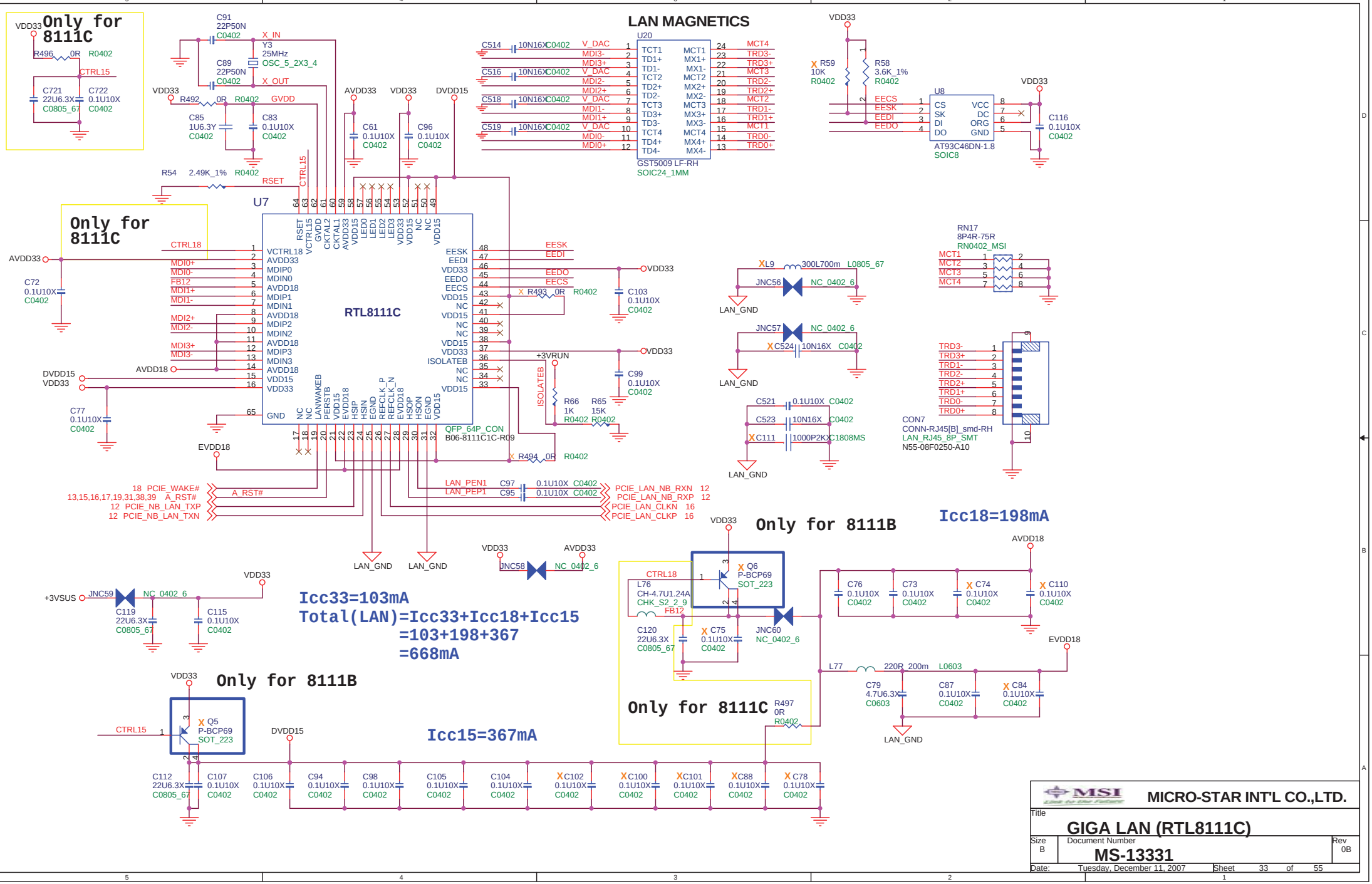
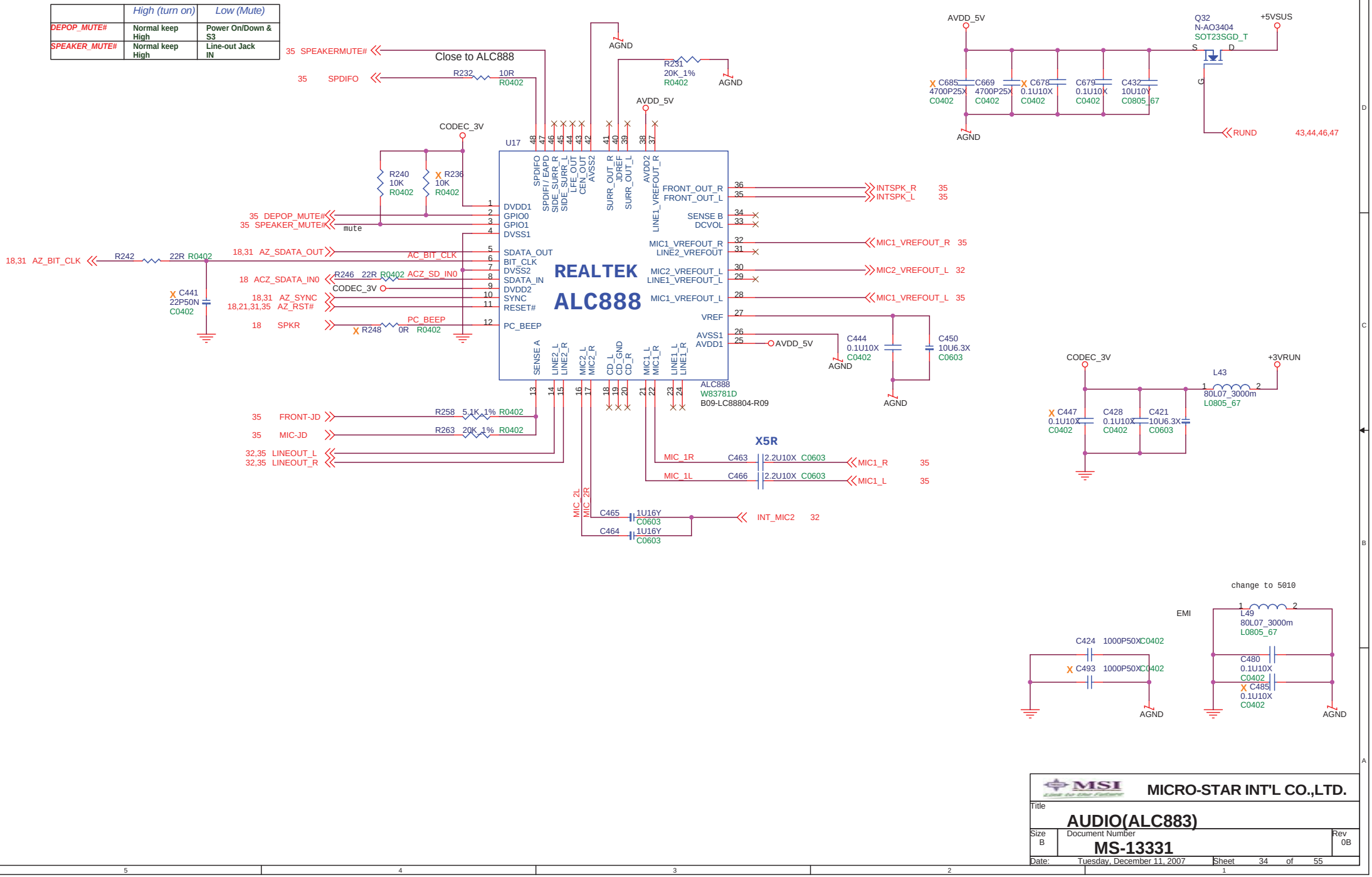


	High (turn on)	Low (Mute)
DEPOP_MUTE#	Normal keep High	Power On/Down & S3
SPEAKER_MUTE#	Normal keep High	Line-out Jack IN

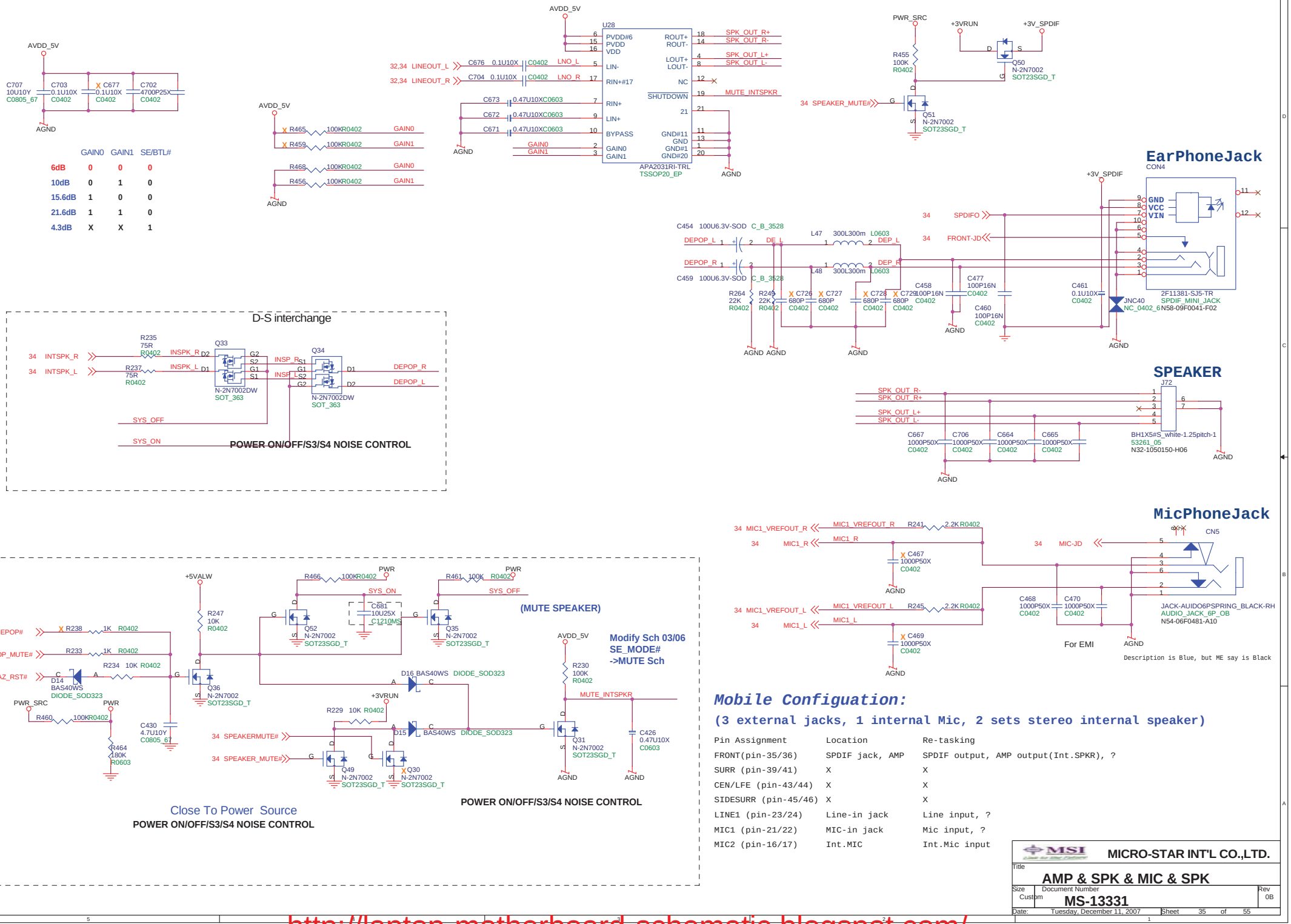


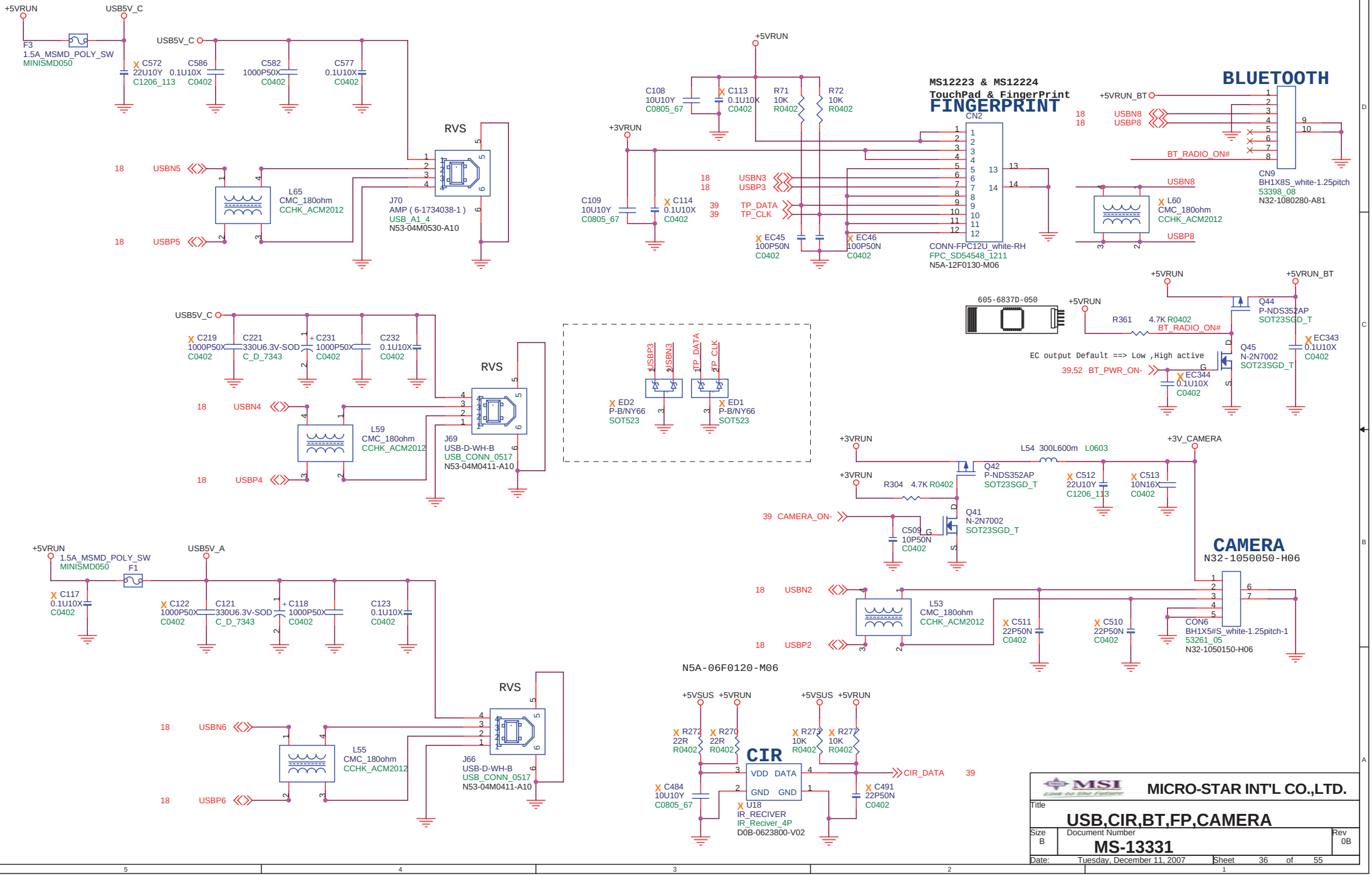
MICRO-STAR INT'L CO.,LTD.

Title: AUDIO(ALC883)

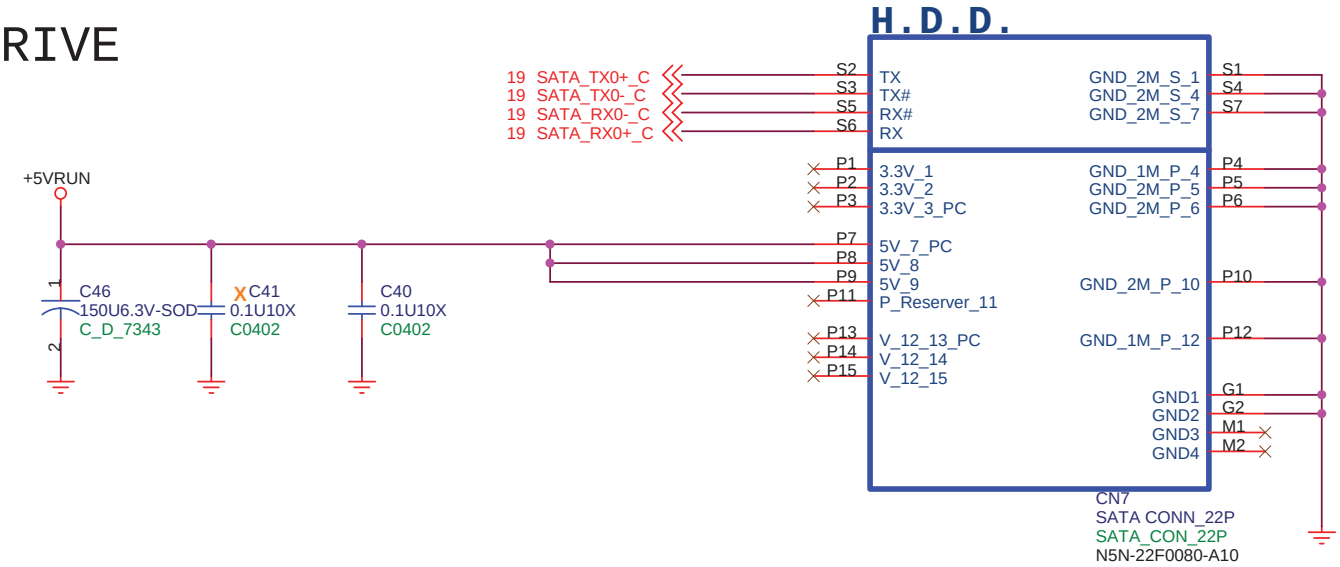
Size: B | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 34 of 55



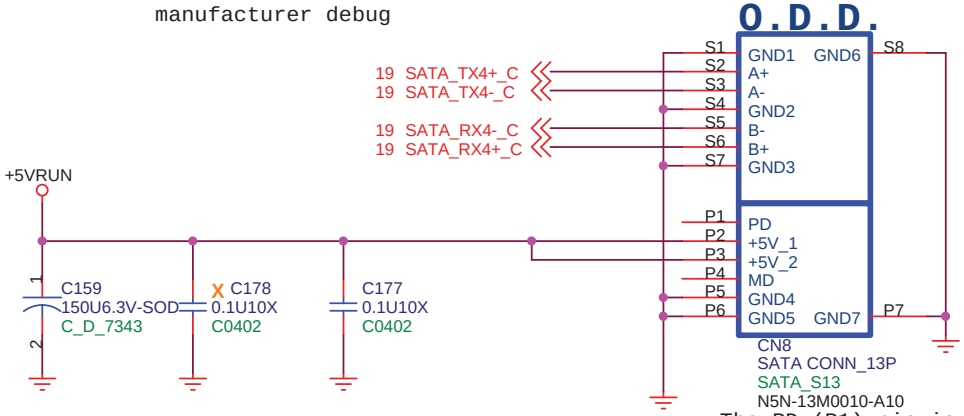


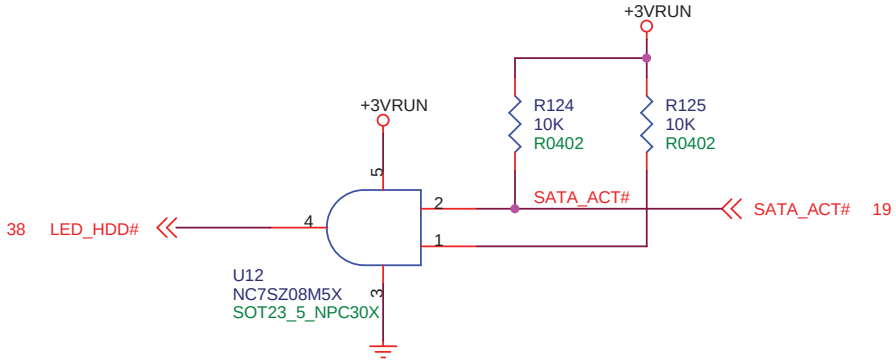
2.5"HD DRIVE



PN & FOOTPRINT N/A

The MD (P4) pin is for ODD manufacturer debug





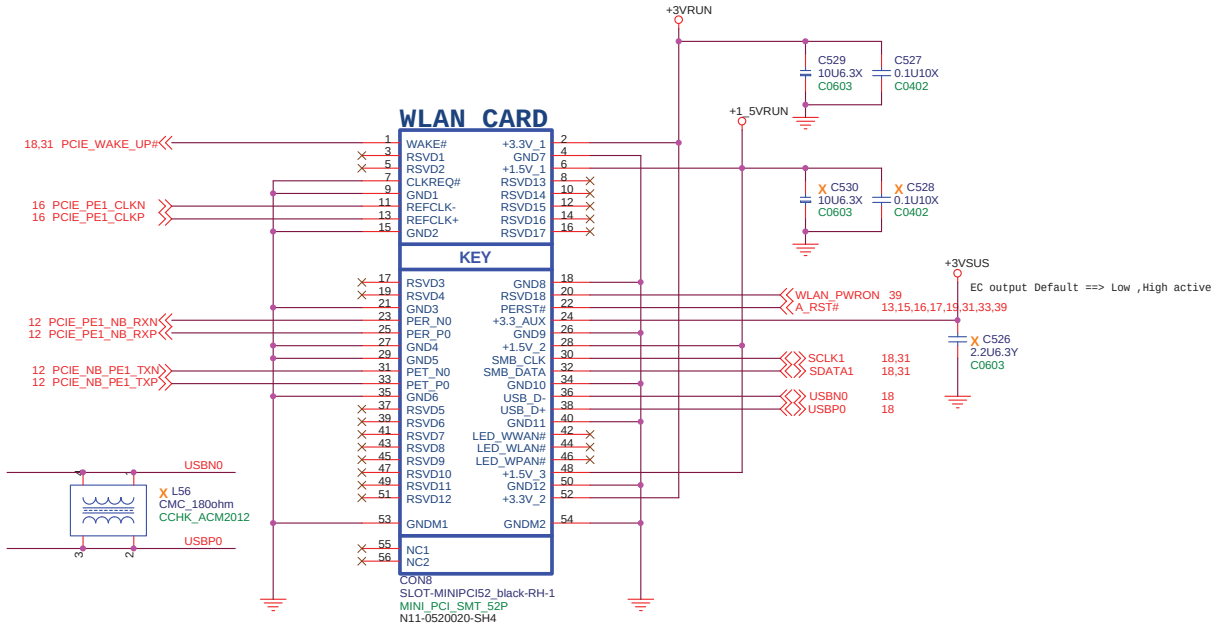
The PD (P1) pin is for host GIO to detect if the ODD is present or not. In the drive, the pin is “pull-low”. So when host side detects this pin as high,then no device; when host side detect this pin as low, then the device present.

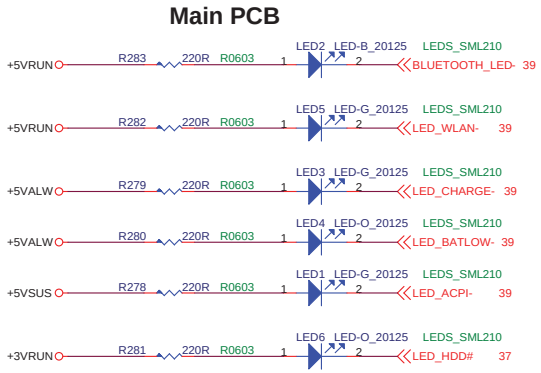
MICRO-STAR INT'L CO.,LTD.

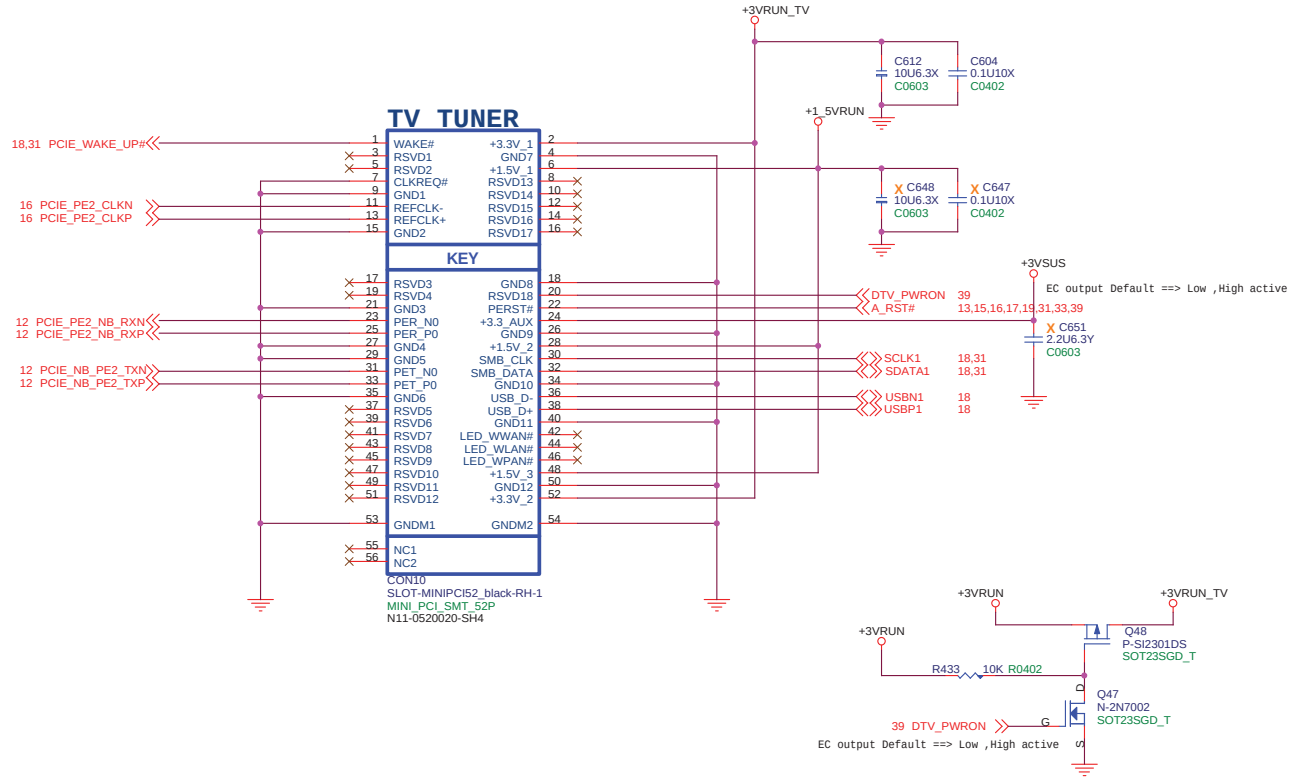
Title: SATA HDD/PATA CDROM CONN

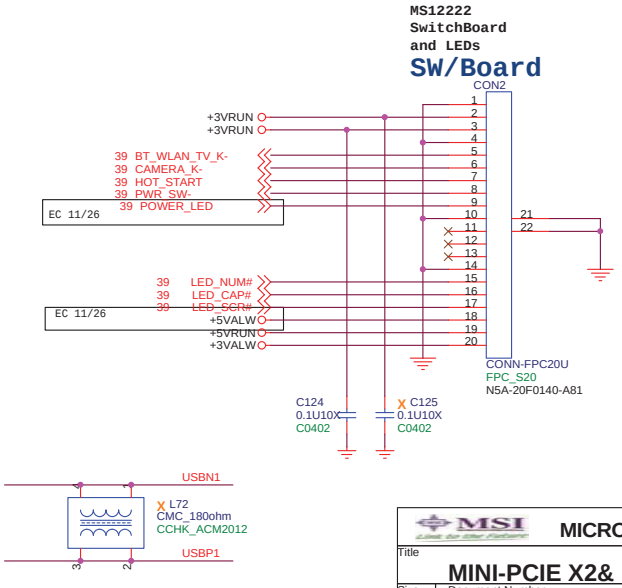
Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 37 of 55







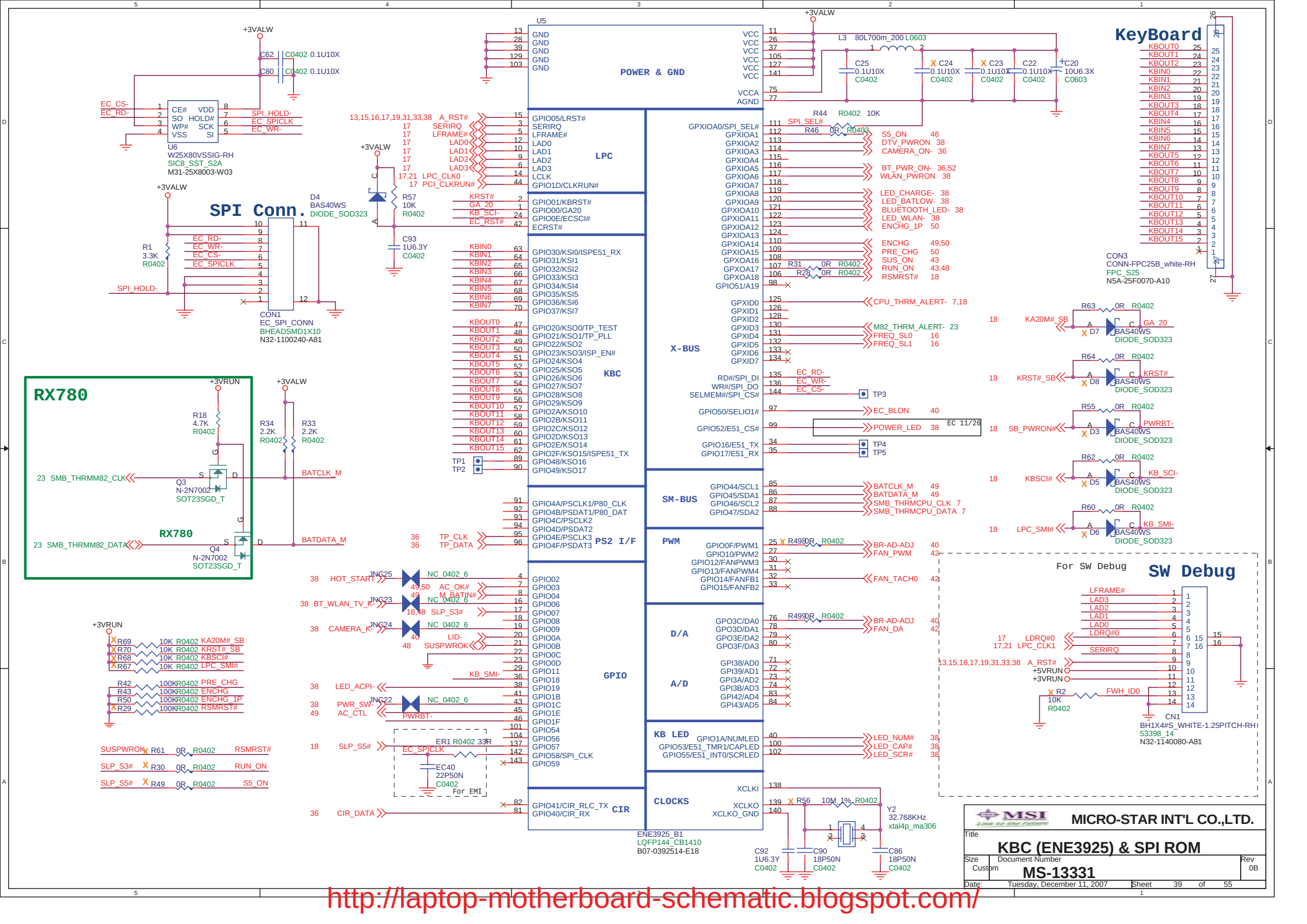


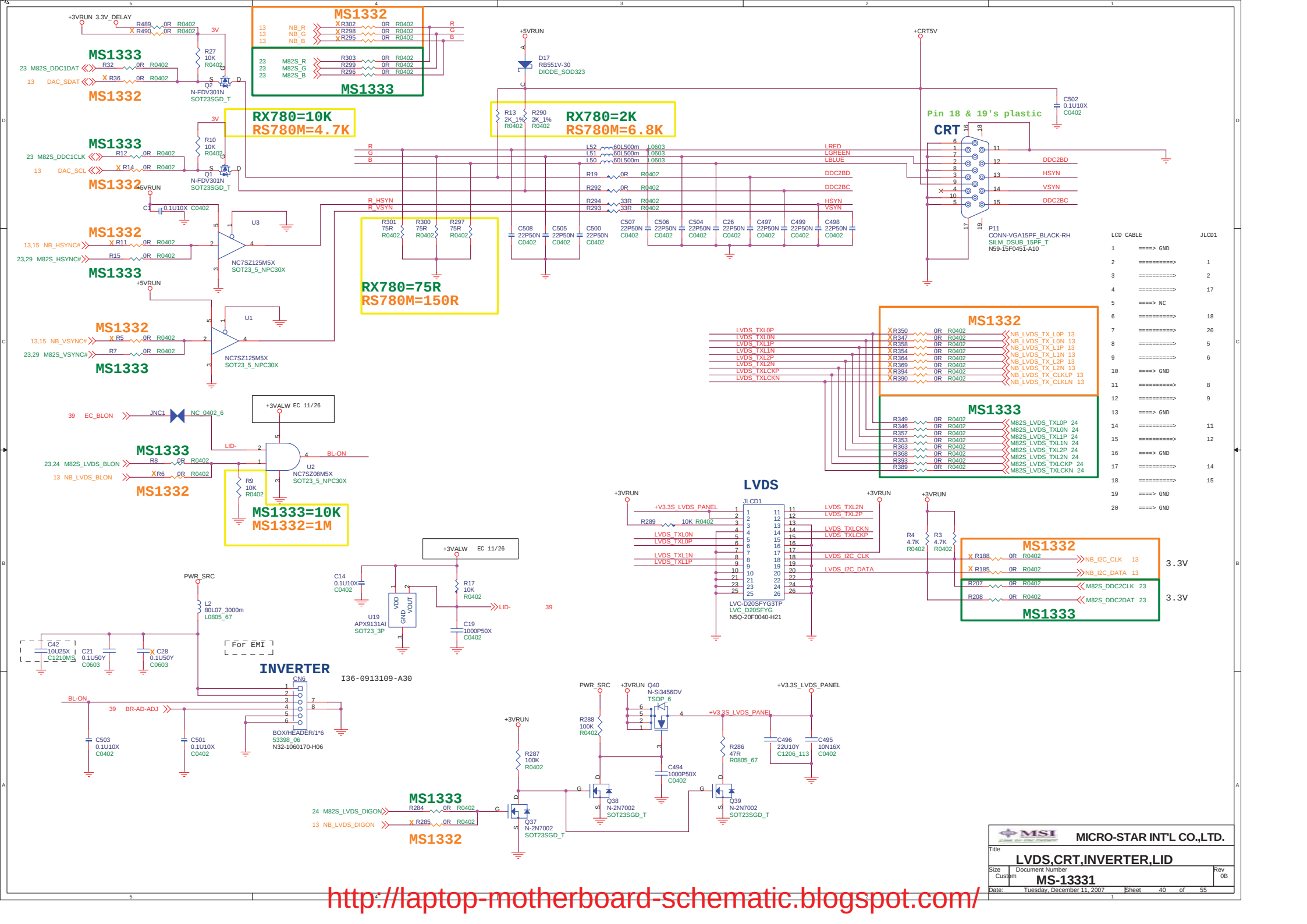
MICRO-STAR INT'L CO.,LTD.

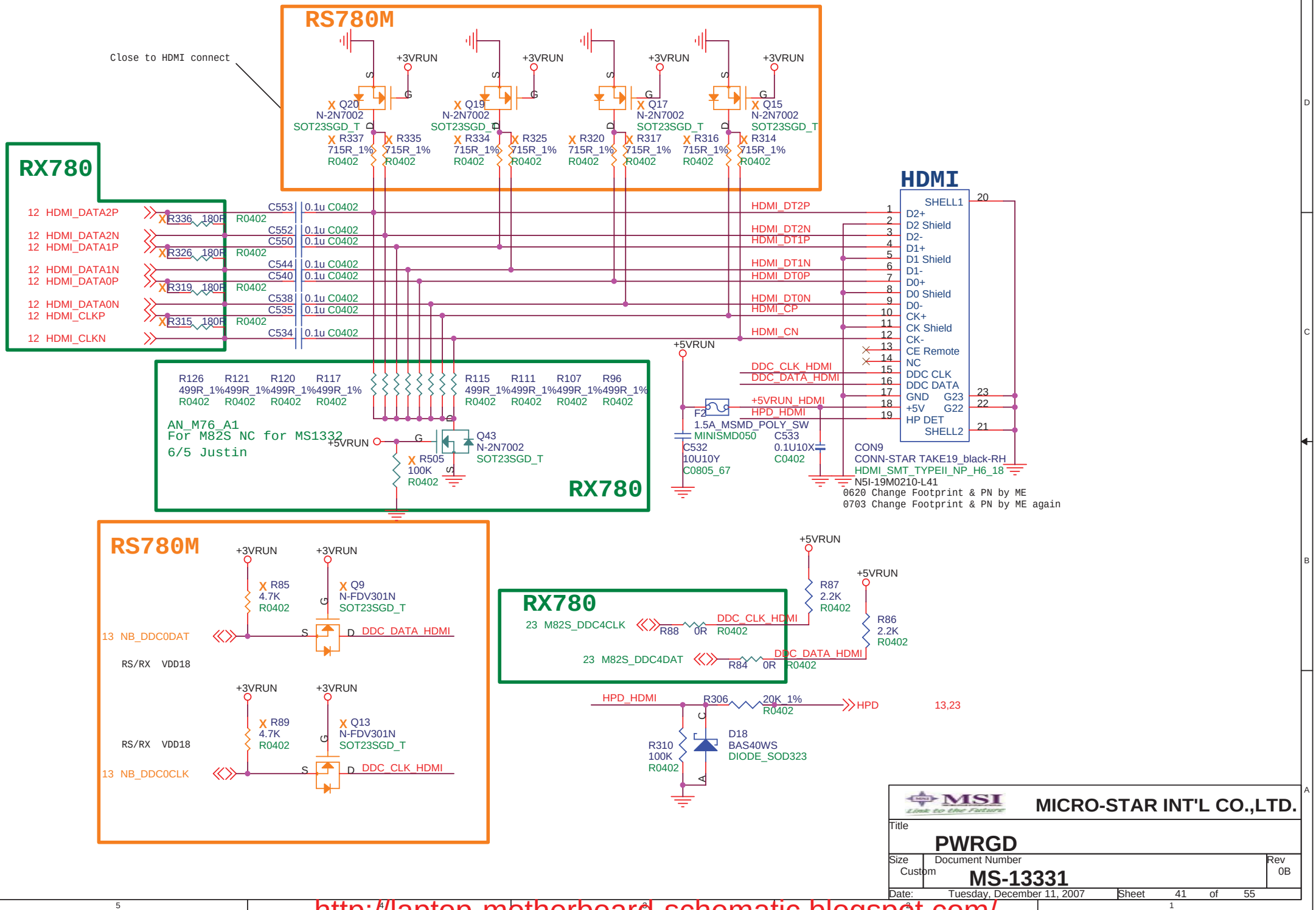
Title: MINI-PCIE X2& LED &SW

Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 38 of 55


KeyBoard
SPI Conn.
RX780
SW Debug
For SW Debug
POWER & GND
LPC
KBC
PS2 I/F
GPIO
X-BUS
SM-BUS
PWM
D/A
A/D
KB LED
CLOCKS
CIR
MICRO-STAR INT'L CO.,LTD.
KBC (ENE3925) & SPI ROM
MS-13331
Tuesday, December 11, 2007
http://laptop-motherboard-schematic.blogspot.com/


MS1332
MS1333
RX780=10K
RS780M=4.7K
RX780=2K
RS780M=6.8K
RX780=75R
RS780M=150R
MS1333=10K
MS1332=1M
Pin 18 & 19's plastic
CRT
LVDS
INVERTER
I36-0913109-A30
MICRO-STAR INT'L CO.,LTD.
LVDS,CRT,INVERTER,LID
MS-13331
Tuesday, December 11, 2007
http://laptop-motherboard-schematic.blogspot.com/

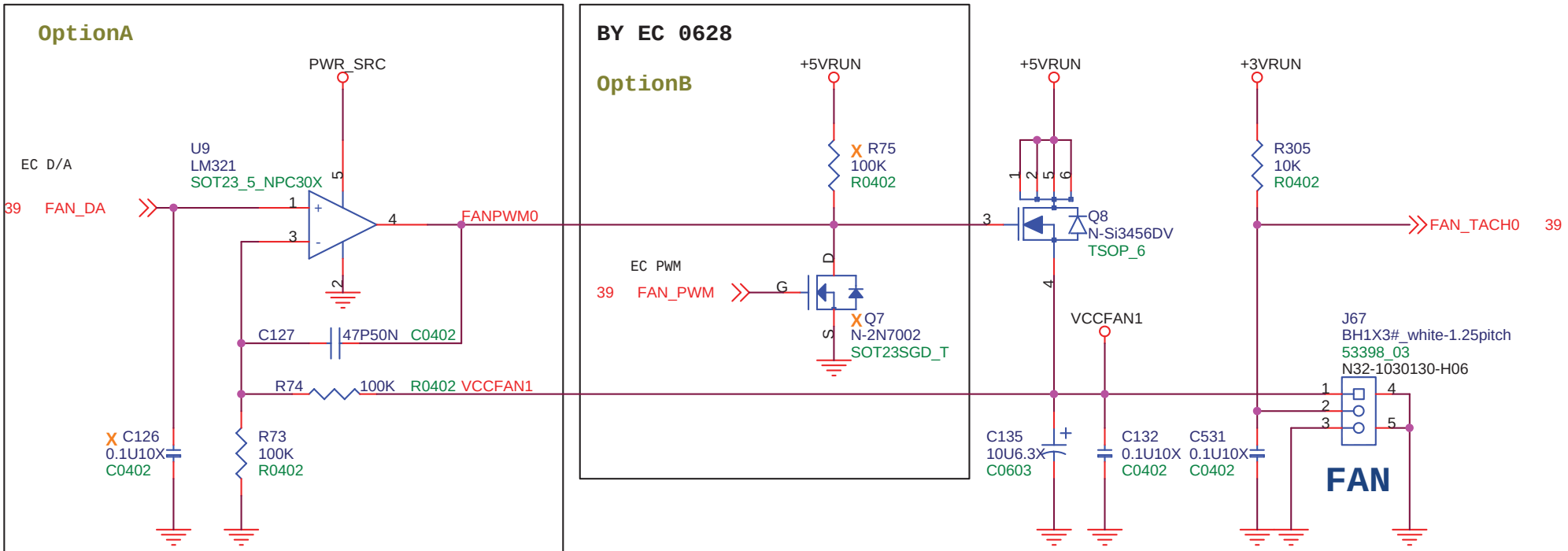


MICRO-STAR INT'L CO.,LTD.

Title: PWRGD

Size: Custom | Document Number: MS-13331 | Rev: 0B

Date: Tuesday, December 11, 2007 | Sheet 41 of 55

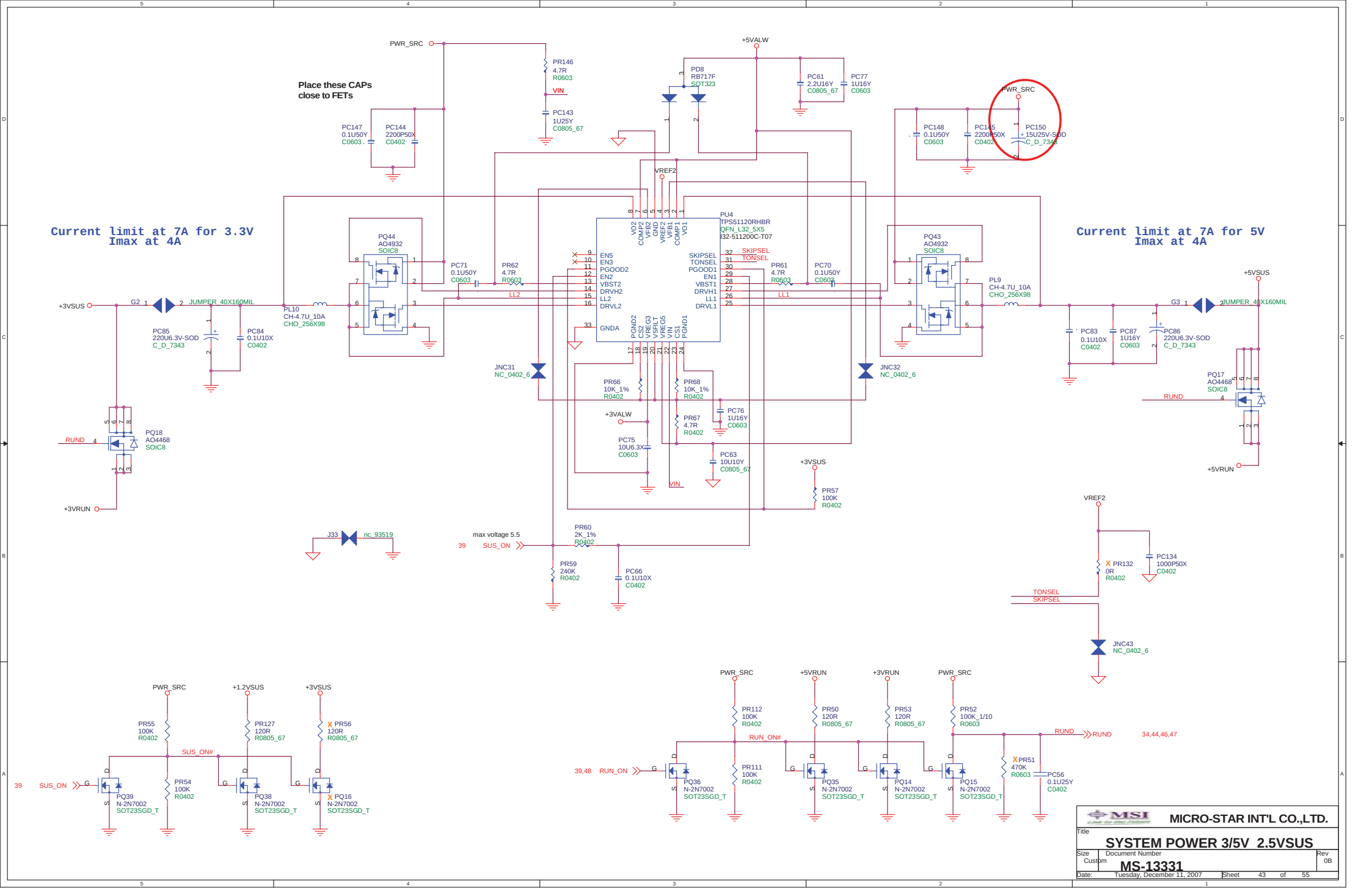


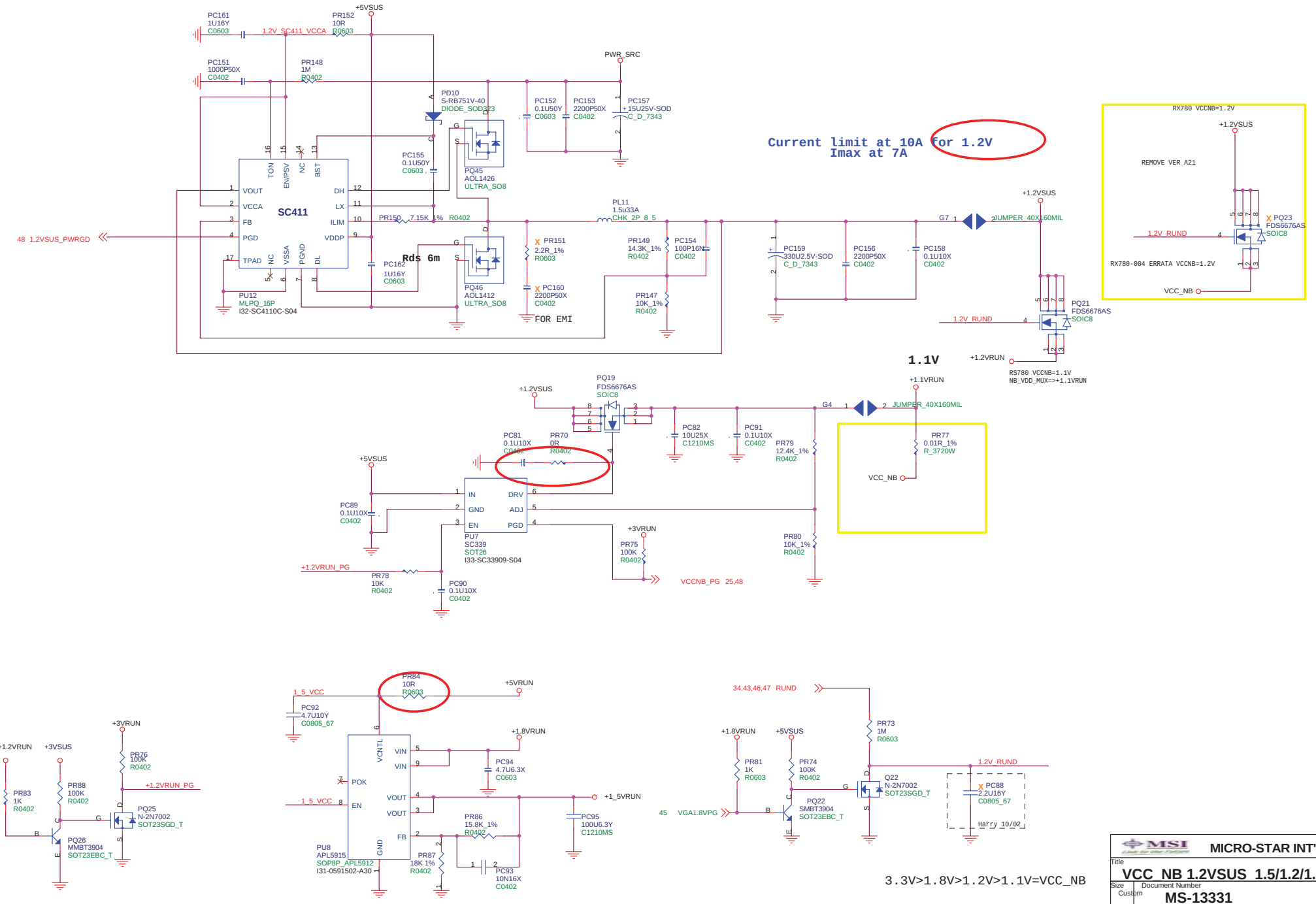
MICRO-STAR INT'L CO.,LTD.

Title: FAN

Size	Document Number	Rev
A	MS-13331	0B

Date: Tuesday, December 11, 2007 Sheet 42 of 55





MSI	MICRO-STAR INT'L CO.,LTD.
Title	VCC_NB 1.2VSUS 1.5/1.2/1.1VRUN
Size: Custom	Document Number: MS-13331
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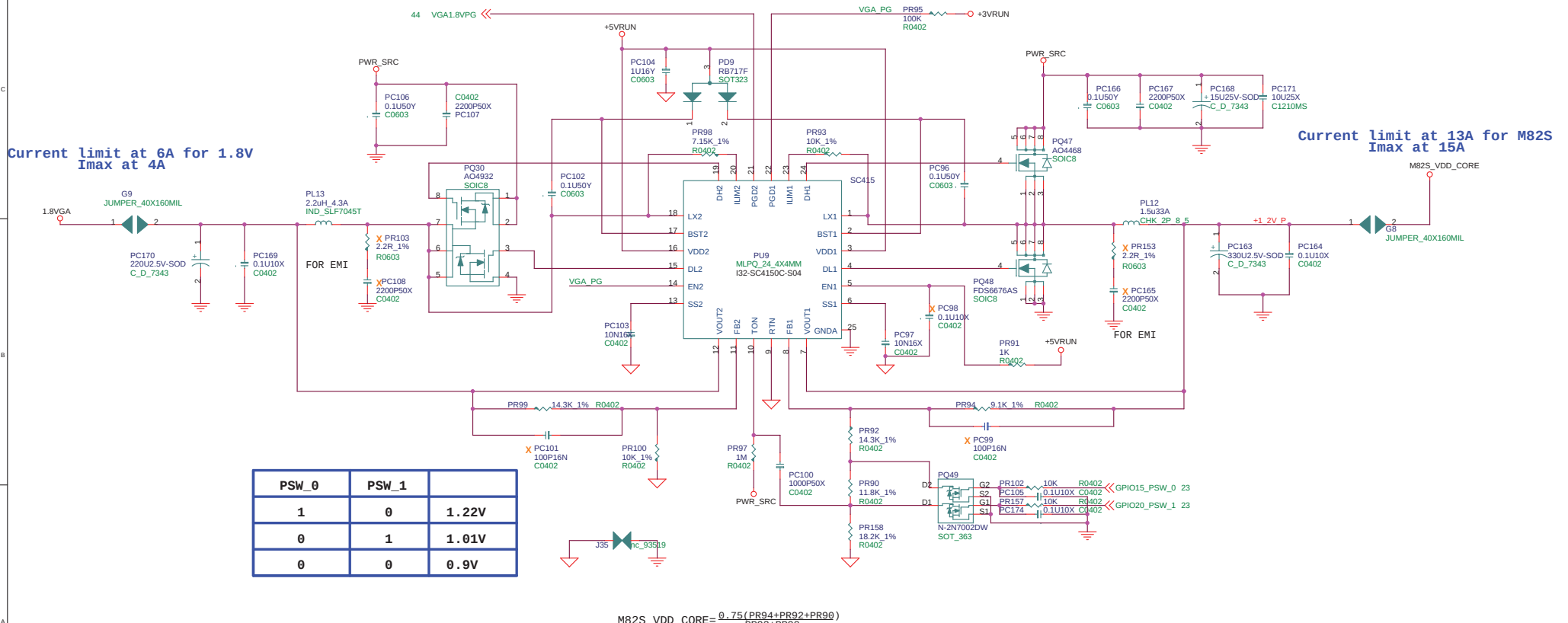
Date: Tuesday, December 11, 2007	Sheet 44 of 55

RX780

M82S_VDDC>1.8VRUN>1.2VRUN>1.1VRUN



PSW_0	PSW_1	
1	0	1.22V
0	1	1.01V
0	0	0.9V

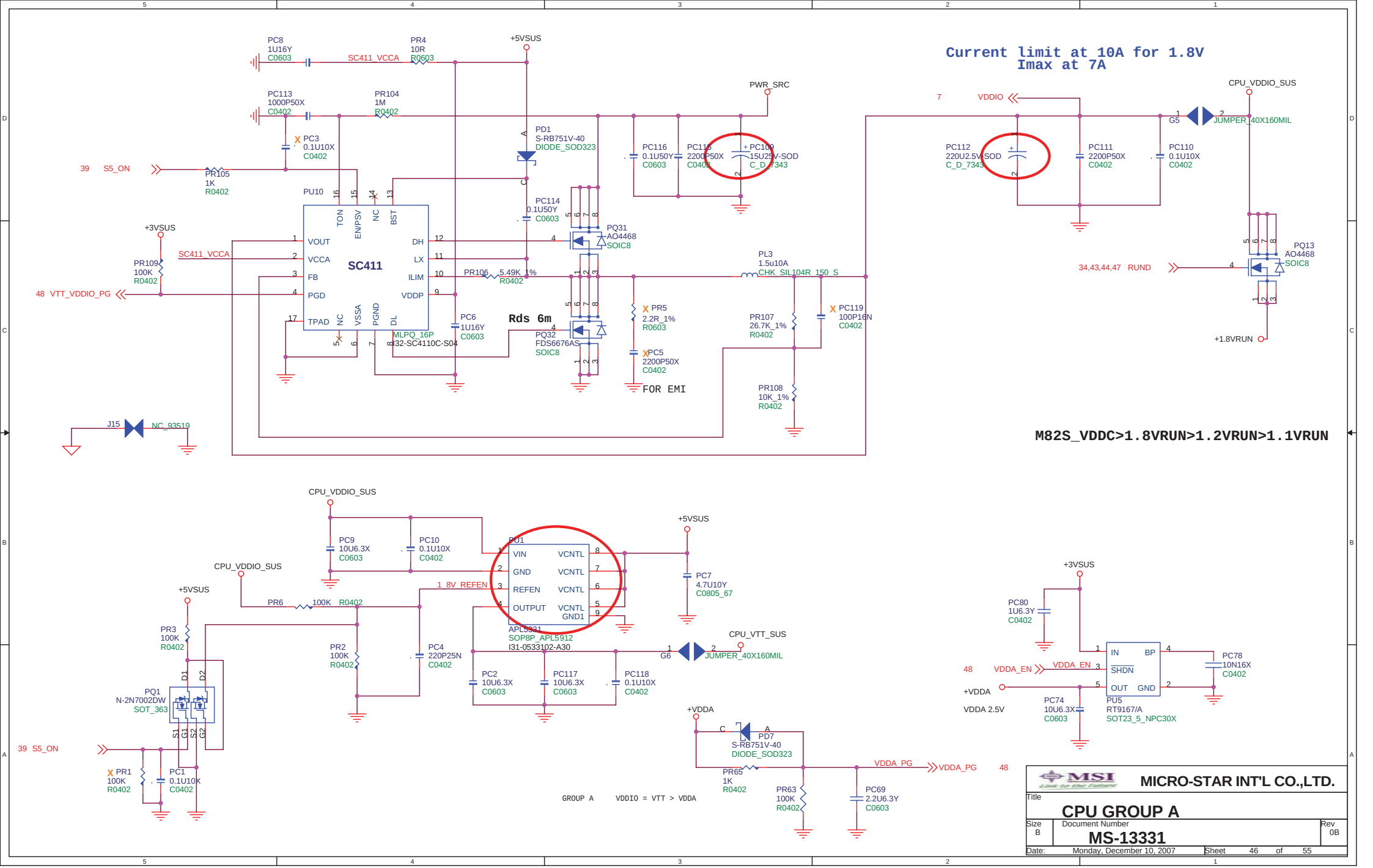
$$M82S\_VDD\_CORE=\frac{0.75(PR94+PR92+PR90)}{PR92+PR90}$$

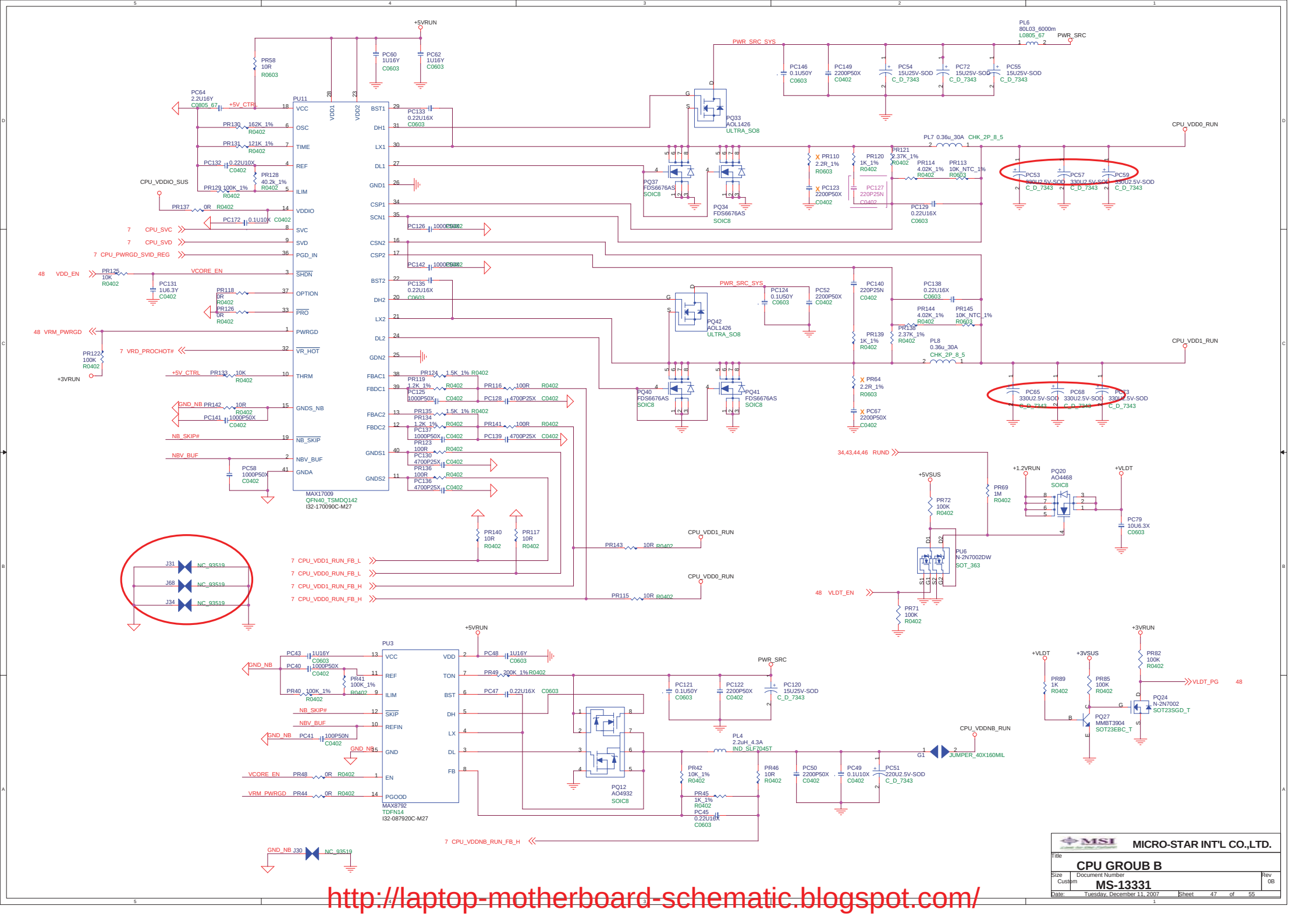
MICRO-STAR INT'L CO.,LTD.

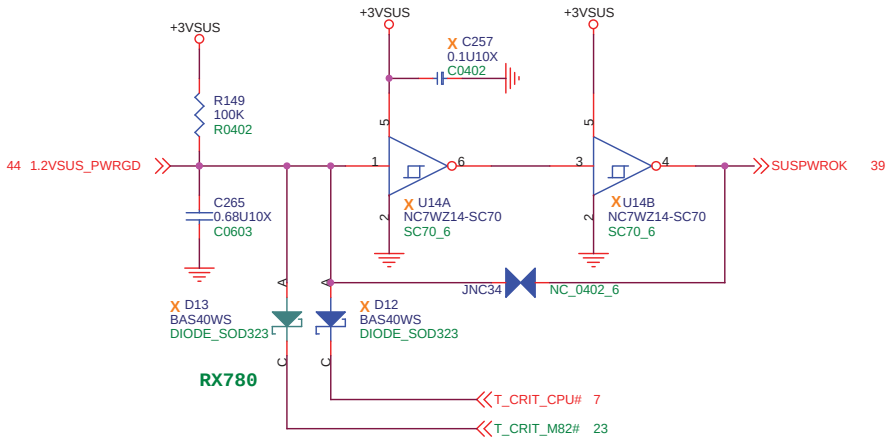
Title: VGA POWER

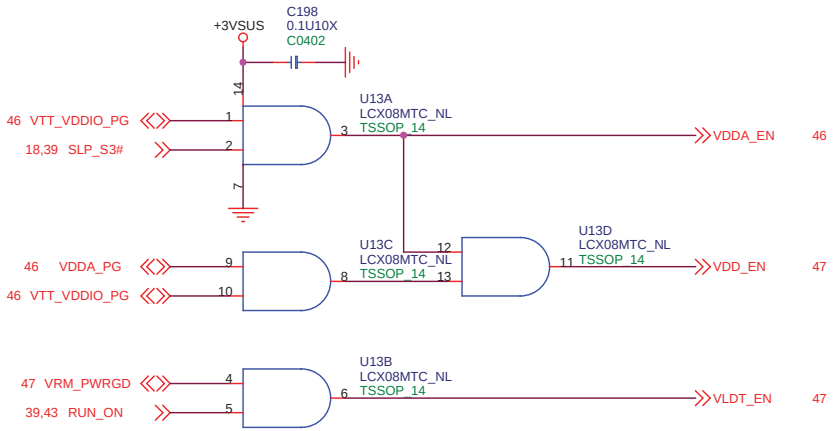
Size: Custom | Document Number: MS-13331 | Rev: 0B

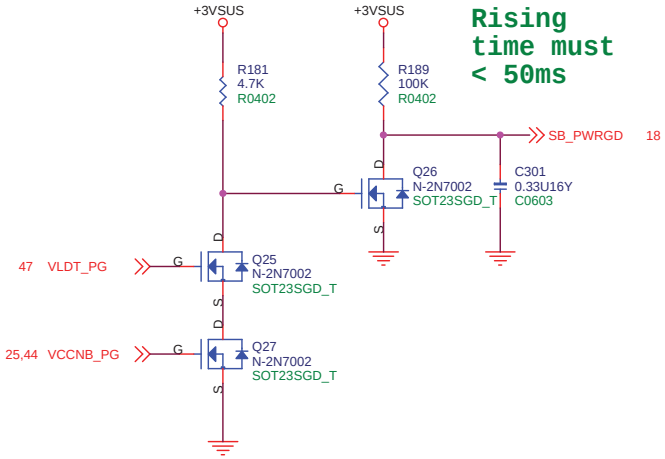
Date: Tuesday, December 11, 2007 | Sheet 45 of 55

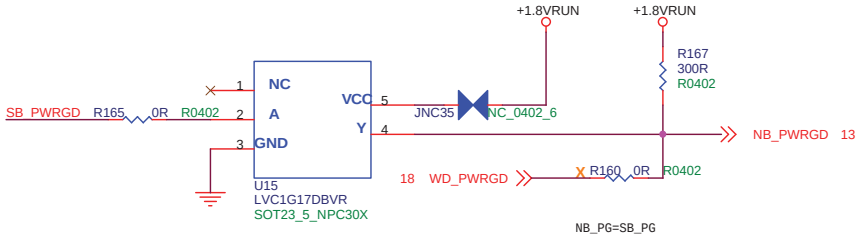




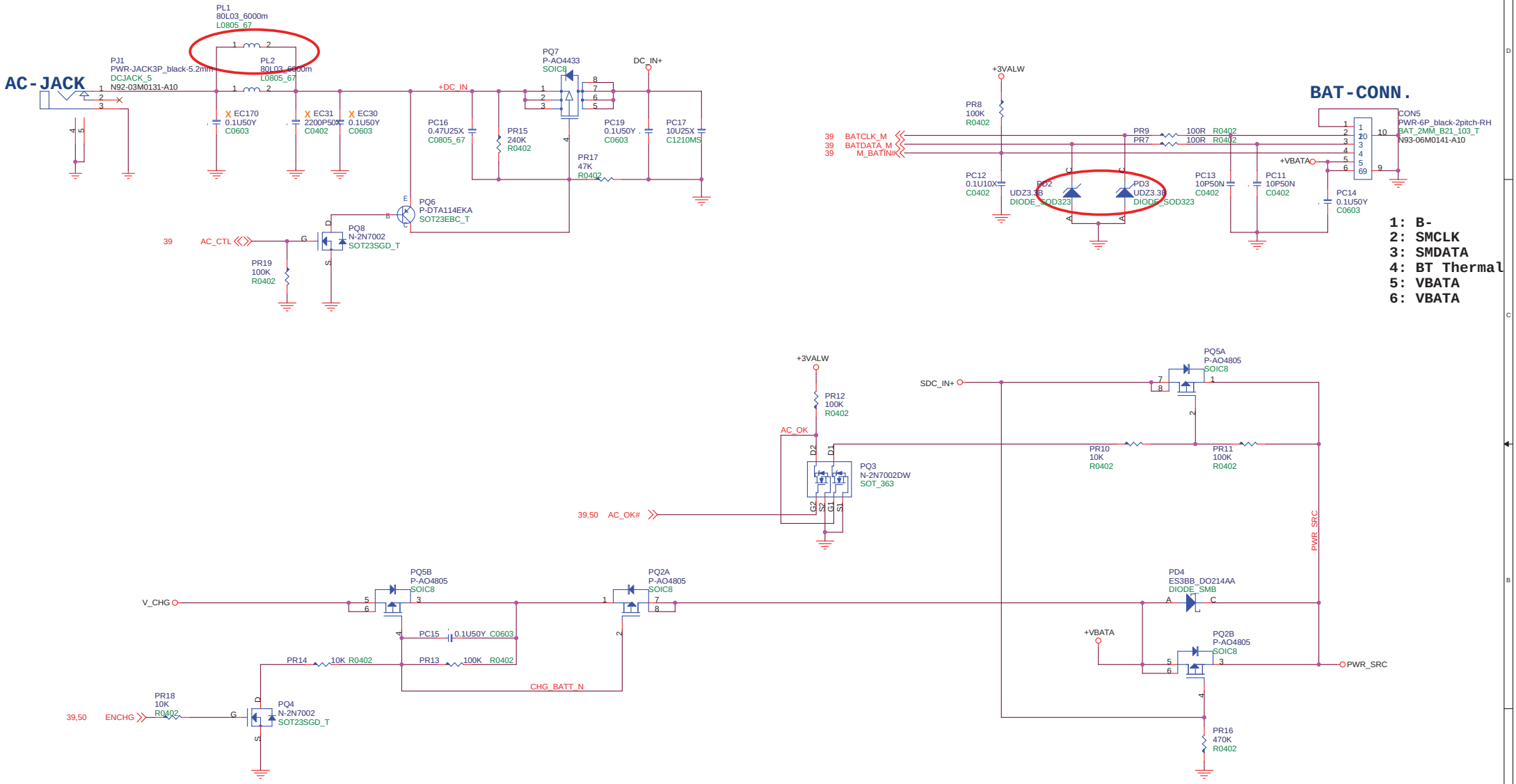








MICRO-STAR INT'L CO.,LTD.		
Title: PWRGD		
Size: B	Document Number: MS-13331	Rev: 0B
Date: Tuesday, December 11, 2007	Sheet 48 of 55	



MICRO-STAR INT'L CO.,LTD.

Title: **Battery Select**

Size: Custom | Document Number: **MS-13331** | Rev: 0B

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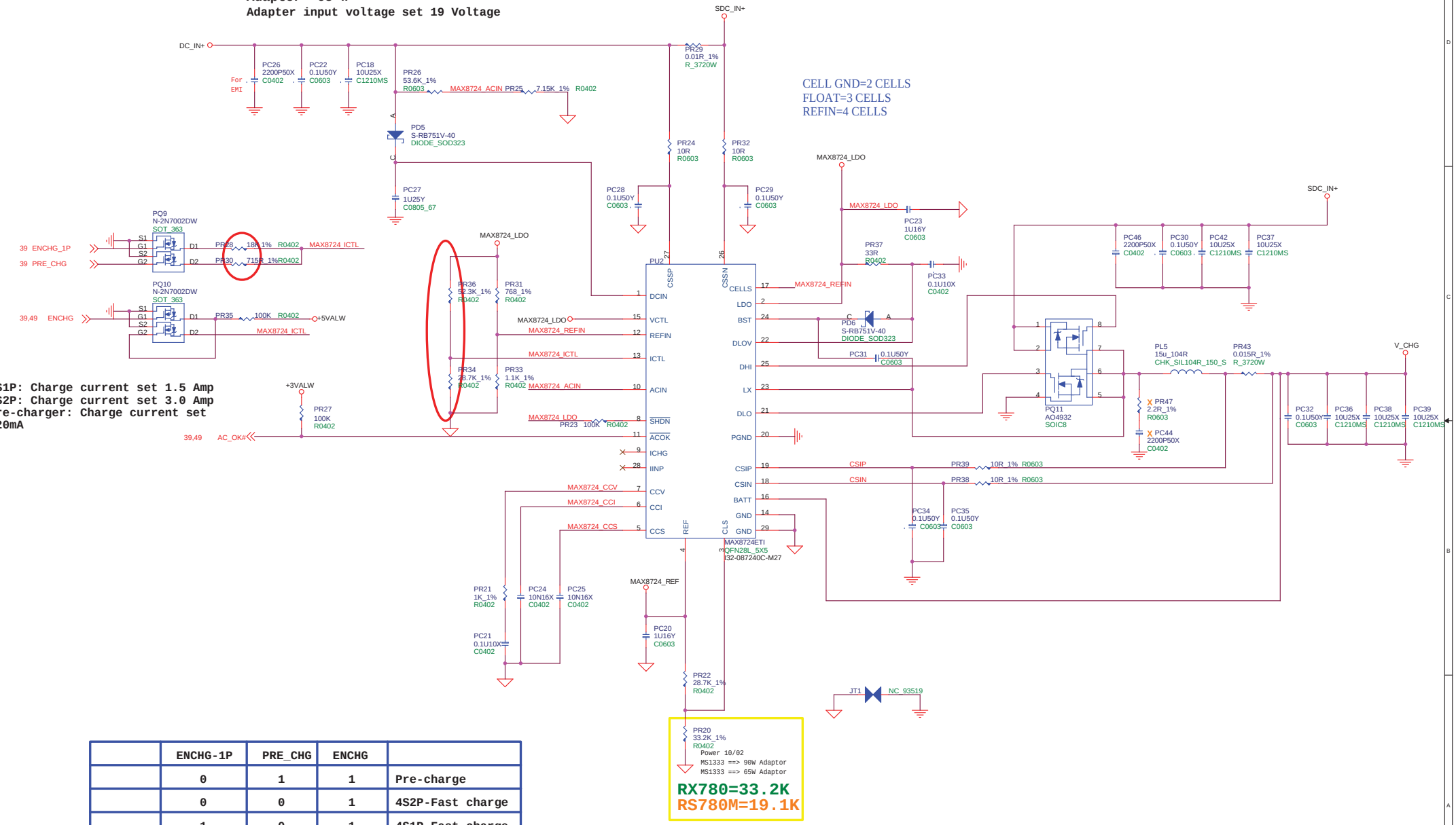
Adapter= 65 W
Adapter input voltage set 19 Voltage



4S1P: Charge current set 1.5 Amp
4S2P: Charge current set 3.0 Amp
Pre-charger: Charge current set 220mA

	ENCHG-1P	PRE_CHG	ENCHG	
	0	1	1	Pre-charge
	0	0	1	4S2P-Fast charge
	1	0	1	4S1P-Fast charge
	X	X	0	STOP CHARGE

MICRO-STAR INT'L CO.,LTD.

Title: M_Battery Charger

Size: Custom | Document Number: MS-13331 | Rev: 0B

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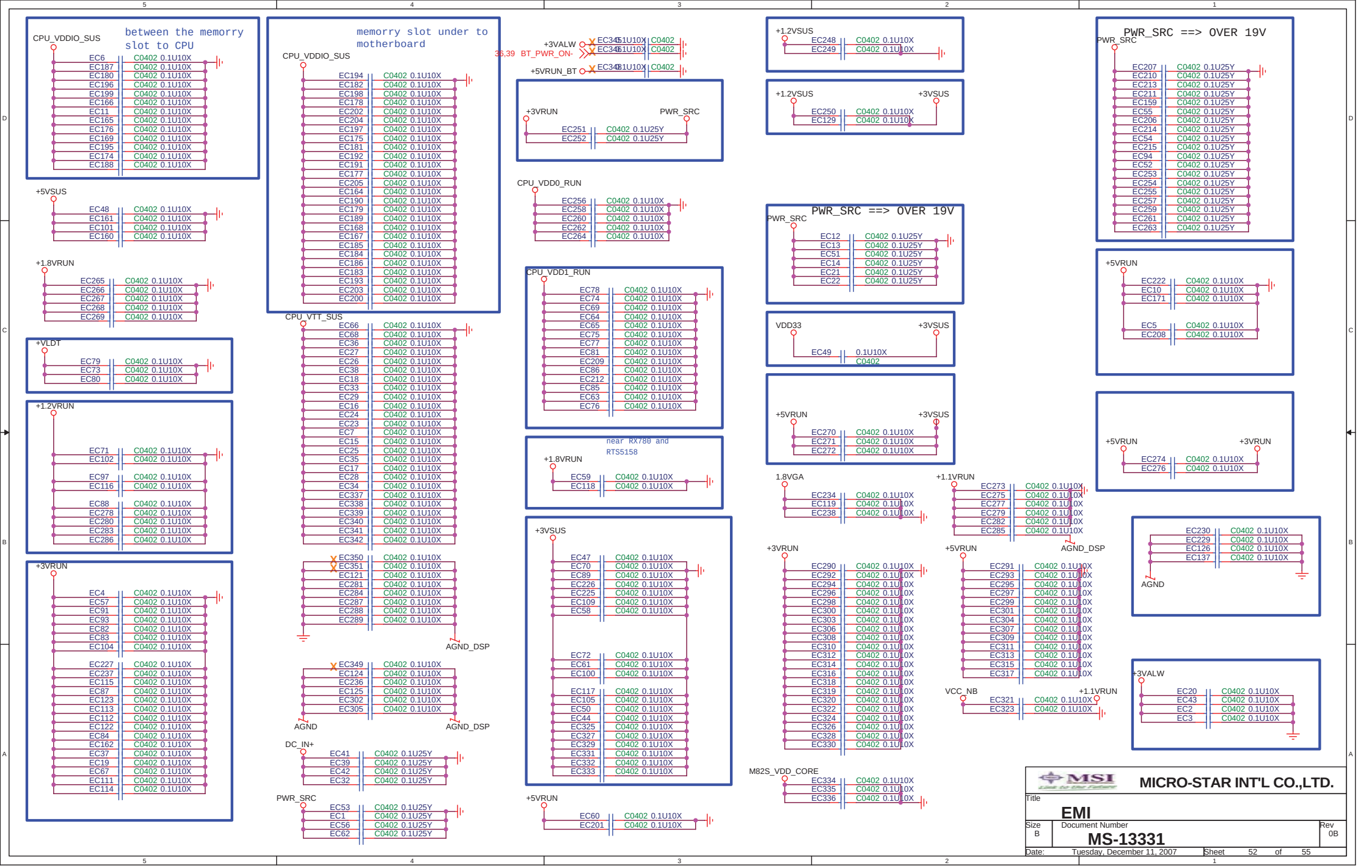

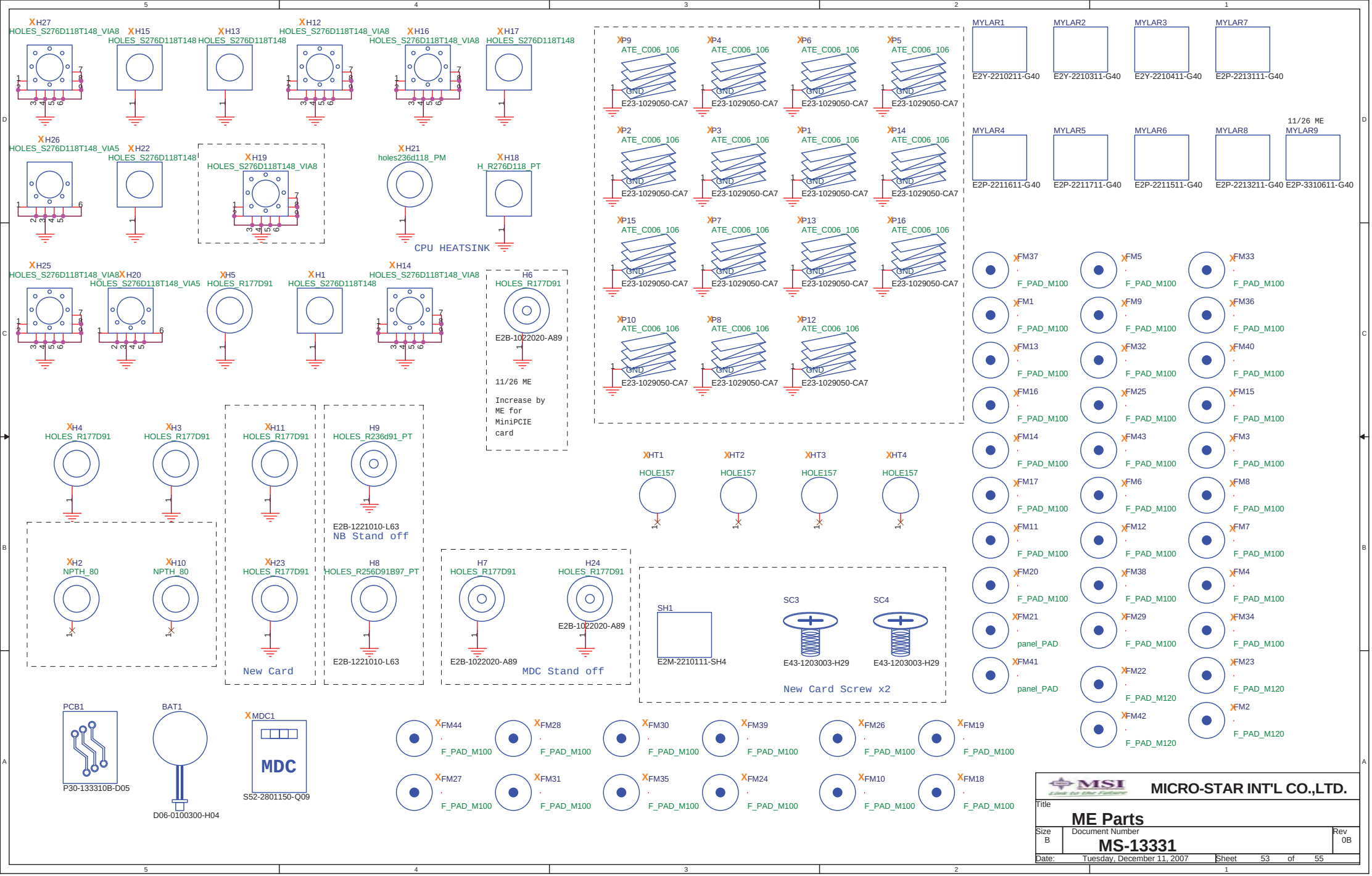

B10 version schematic change form A20.003

11/23: Excange TX and RX for HDMI interface -- P12
11/23: Correct Q12 pins with nets -- P7
11/23: Change DDC_CLK0 to A8 DDC_DATA0 to B8 -- P13
11/23: DNI R151 -- P13
11/23: Change the value of R344 R342 to 301 Ohm -- P11
11/23: DNI R170 and Increase R176 -- P13
11/23: Install L24 L25 L29 C256 C266 C276 -- P13
11/23: DNI R179 R182 -- P13
11/23: Install L64, L28, C574 C272 -- P13
11/23: DNI R145, Install R341 & R332 -- P13 & P17
11/23: Install R172 & R175 -- P13
11/23: Change the value of R38 to 100 Ohm R41 to 200 Ohm -- P16
11/23: Move 0 Ohm form R171 to R177 -- P13
11/23: Install L62, L23, C571, C264, C267 -- P13
11/23: DNI R183, R187 -- P16
11/23: Install R173 C286 -- P14
11/23: Install R406 -- P15
11/23: Change the schematic of VGA power -- P45
11/23: DNI R285 and R437 by ATi Roger-- P29
11/23: DNI R440, Install R439&R420 for 256MB 2X(32X32) GDDRIII seeting -- P29
11/23: Remove C287 for match power sequence -- P25
11/23: Change the value of C697 to 47p -- P30
11/23: Change R86&R87 form 6.8K to 2.2K -- P41
11/23: EC request to connect KBC U5.22 to GND -- P39
11/23: Remove D21 and connect U3's power to +5VRUN -- P40
11/23: Change the value of R167 from 4.7K to 300R -- P48

11/23: HDMI I2C signal pull high level from +1.8VRUN change to +3.3VRUN for RS780 (AWT3.2) -- P41
11/23: SB +1.2VSUS change to +1.2VRUN : R131 install and R136 N/C for SB700_A12 (AN_RS780E1) -- P20

11/26: Reserve C278 (P14) C571&C264 (P13) R7 (P15) to GND for RX781
11/26: Change NB&SB PN to ver A12, GDDRIII to 32X32
11/26: Increase R588 -- P23

RS780M:

11/23: Power
PR66 14.3K_1%-->10K_1%
PR68 14.3K_1%-->10K_1%
PR79 11.8K_1%-->12.4K_1%
PC154 100P_NC ' 100P_麗上件 -
PR98 10K_1%-->7.15K
PR93 7.15K'10K
PR106 7.15K_1%'5.49K_1%
PC128 4700P '1000P
PC139 4700P '1000P
PR49 100K_1% 200K_1%
PR30 1.4K_1% ' 715_1%
VGA Power change

11/30: Power
PR120 1K_1%_NC'1K_1% 上件 -
PR139 1K_1%_NC'1K_1% 上件 -
PC127 220P_NC '220P 上件
PC140 220P_NC '220P 上件
PC128 1000P'4700P
PC139 1000P'4700P

11/23: Change DDC_CLK0 to A8 DDC_DATA0 to B8 -- P13
11/23: Install L24 L25 L29 C256 C266 C276 -- P13
11/23: DNI R170 and Increase R176 -- P13
11/23: DNI R179 R182 -- P13
11/23: Install L64, L28, C574 C272 -- P13
11/23: Install R172 & R175 -- P13
11/23: Move 0 Ohm form R171 to R177 -- P13
11/23: DNI R151 -- P13
11/23: Install L62, L23, C571, C264, C267 -- P13

11/26: Reserve C278 (P14) C571&C264 (P13) R7 (P15) to GND for RX781

Need to change NB SB GDDR3 ClkGen LAN's PN

Size	<Title>		
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