MODEL NAME : *BCV00/ BCV10*

PCB NO : *LA-D991P*

BOM P/N :

Dell/Compal Confidential

Schematic Document

SKYLAKE-H

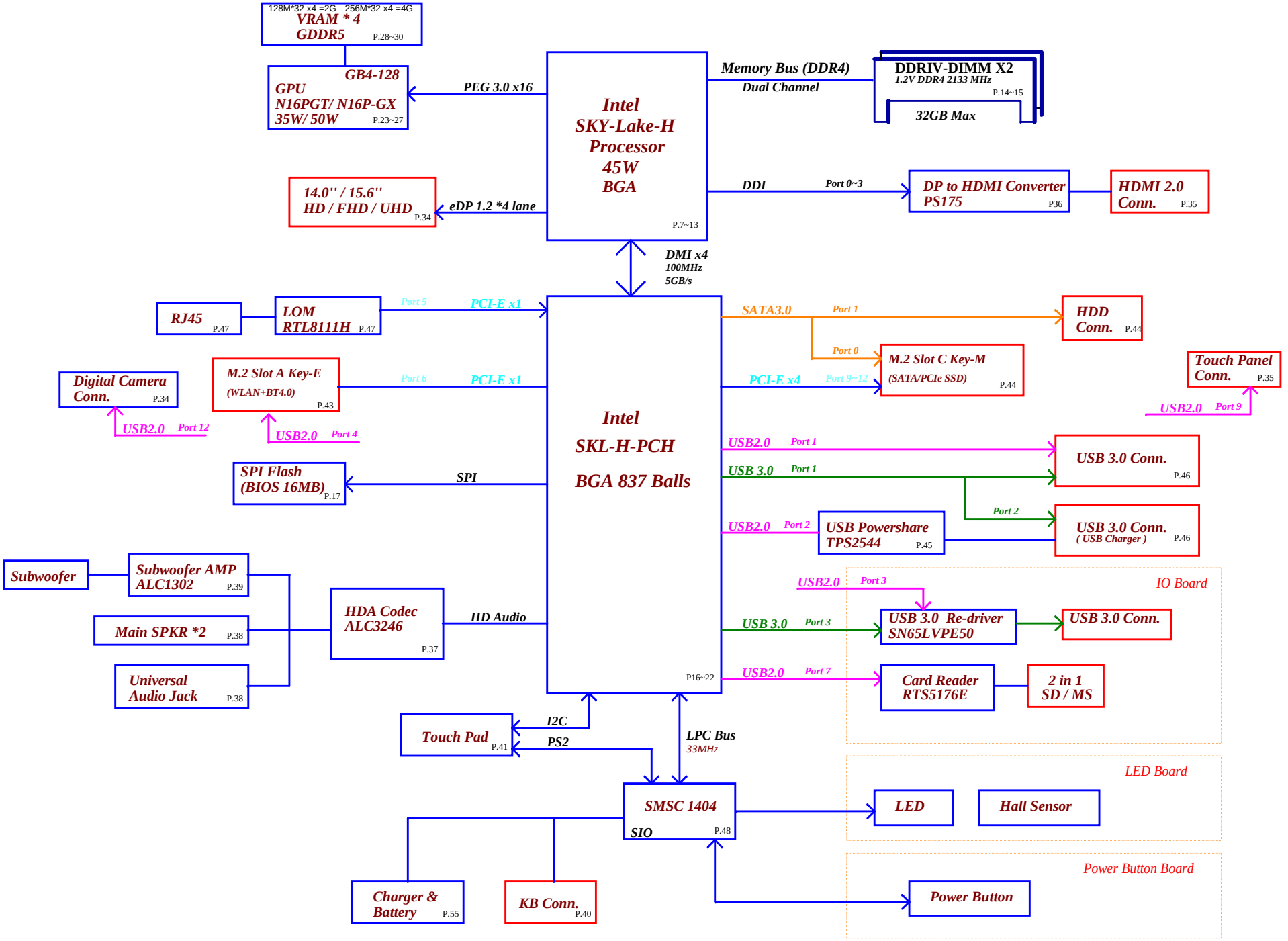
2016-06-25

Rev: 1.0 (A00)

@ : Nopop Component
CONN@ : Connector Component
R1@ / R3@ : R1/R3 CPN for CPU, GPU, PCB
EMC@ : Pop of EMI parts
M2G@ : Micron GDDR5 2G for GPU
H2G@ : Hynix GDDR5 2G for GPU
S4G@ : Samsung GDDR5 4G for GPU
M4G@ : Micron GDDR5 4G for GPU
BreakDown@ : For measure power consumption
14GT@ : 14" GPU N16P-GT
15GX@ : 15" GPU N16P-GX

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2011/08/25

Compal Electronics, Inc.			
Title: Cover Page			
Size	Document Number		Rev 0.1(A00)
Date: Thursday, August 18, 2016	Sheet 1 of 70		



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2011/08/25

Compal Electronics, Inc.

Title: **Block diagram**

Size	Document Number	Rev
		0.1(X00)

Date: Thursday, August 18, 2016 Sheet 2 of 70

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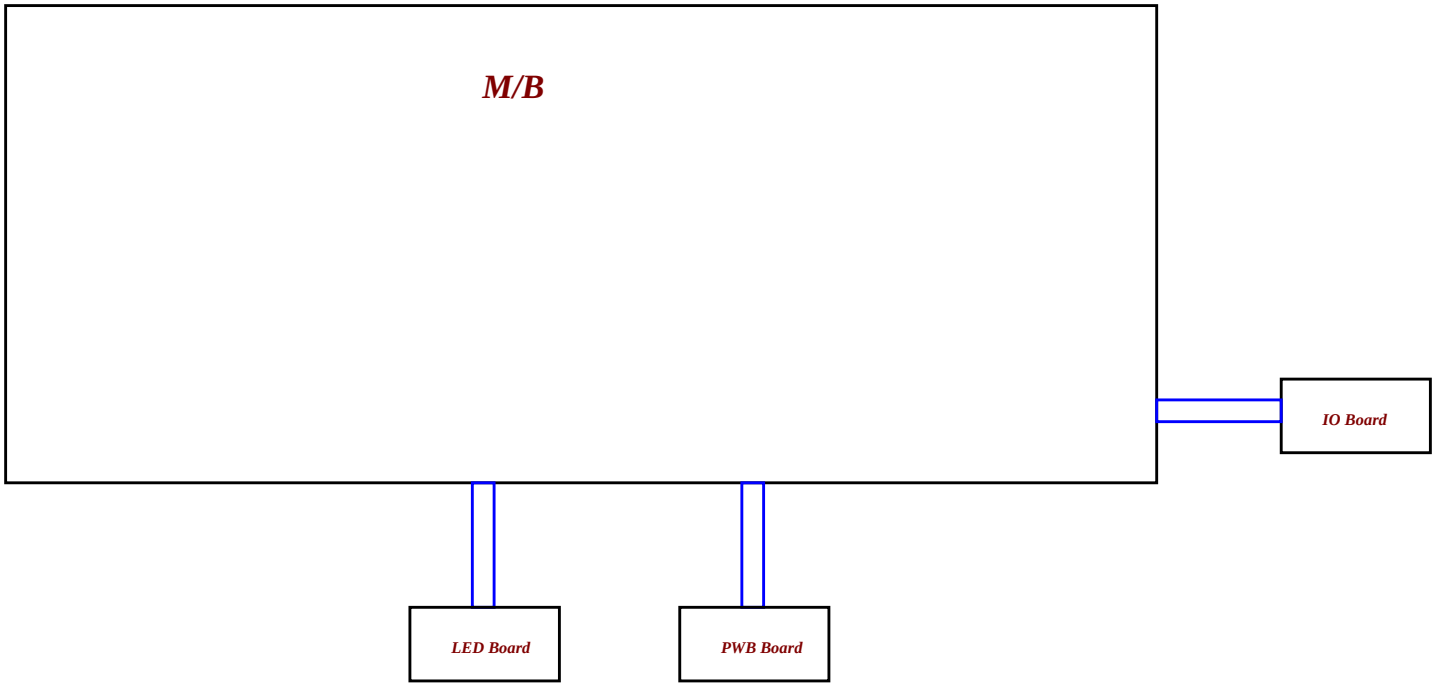
Project Code :
File Name :



Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **DB block diagram**

Size | Document Number | Rev 0.1(X00)

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Board ID	Resistor
X00	10K
X01	13.7K
X02	17.8K
X03	
A00	22.1K

USB3	DESTINATION
1	USB Conn 1
2	USB Conn 2
3	USB Conn 3 (IO Board)
4	None
5	None
6	None

USB 2.0	DESTINATION
1	USB Conn 1
2	USB Conn 2
3	USB Conn 3 (IO Board)
4	NGFF1- WLAN
5	None
6	None
7	Card Reader
8	None
9	Touch screen
10	None
11	None
12	CAMERA

DDI	DESTINATION
1	Converter
2	Converter
3	Converter

LPC	DESTINATION
LPC0	MEC1404
LPC1	DEBUG PORT

PCI EXPRESS	DESTINATION
Lane 1	None
Lane 2	None
Lane 3	None
Lane 4	None
Lane 5	LAN
Lane 6	WLAN
Lane 7	None
Lane 8	None
Lane 9	SSD
Lane 10	SSD
Lane 11	SSD
Lane 12	SSD
Lane 13	None
Lane 14	None
Lane 15	None
Lane 16	None

SATA	DESTINATION
0A	SSD
1A	SSD
N/A	N/A
N/A	N/A
0B	None
1B	HDD
2	None
3	None

CLKOUT_PCIE	DESTINATION	CLKOUT_PCIE	DESTINATION
0	None	10	None
1	None	11	None
2	LAN	12	GPU
3	NGFF-1 WLAN	13	None
4	None	14	None
5	None	15	None
6	NGFF-2 SSD		
7	None		
8	None		
9	None		

Symbol Note :

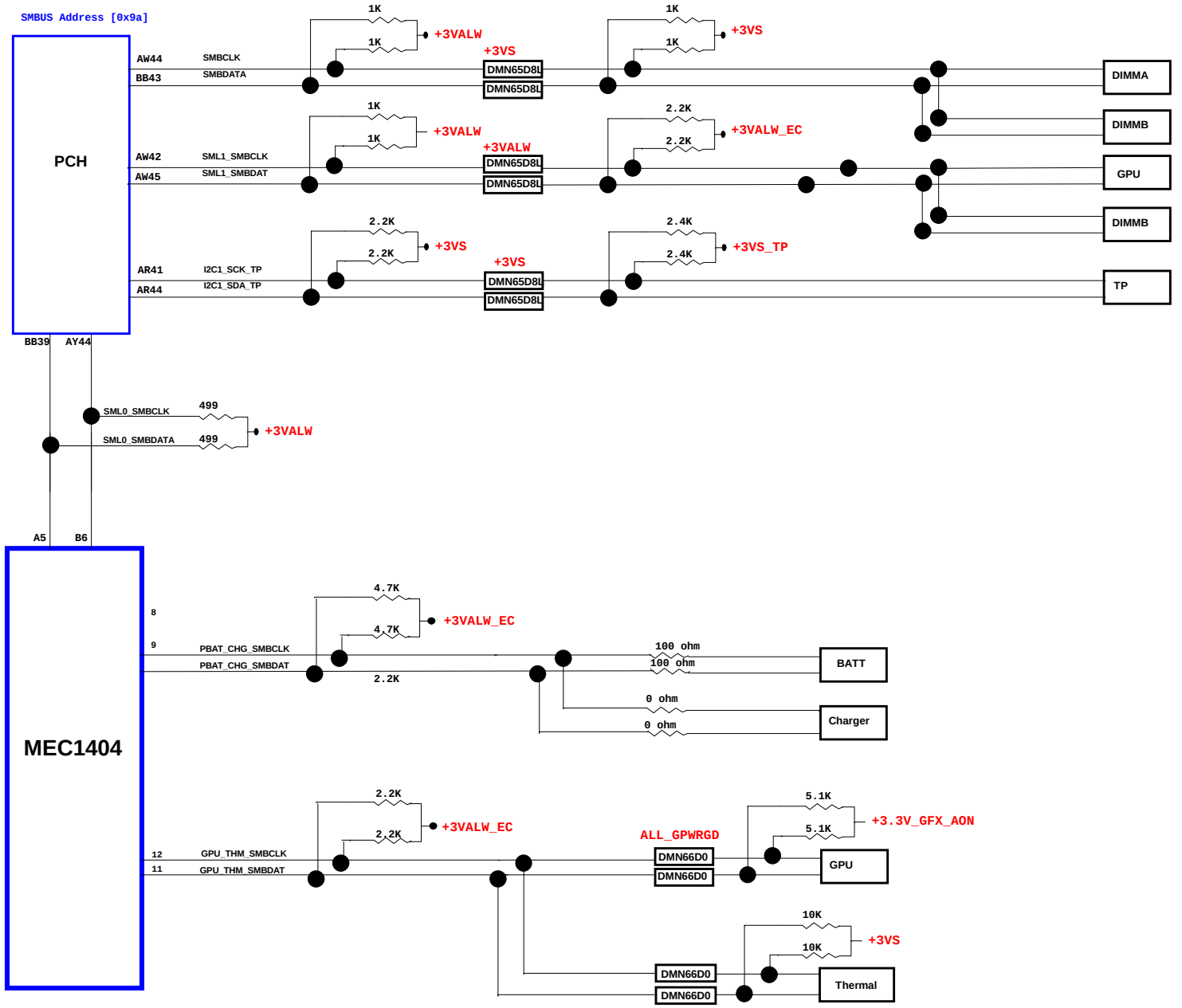
: means Digital Ground : means Analog Ground

Compal Electronics, Inc.

Title: Notes List

Size | Document Number: LA-D991P | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 4 of 70



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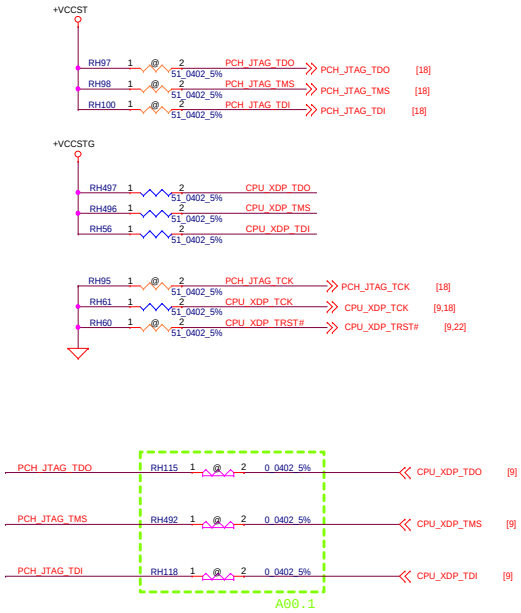
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/15

Title: *SMBus Block Diagram*

Size	Document Number	Rev
C		0.1(X00)

Date: Thursday, August 18, 2016 Sheet 5 of 70



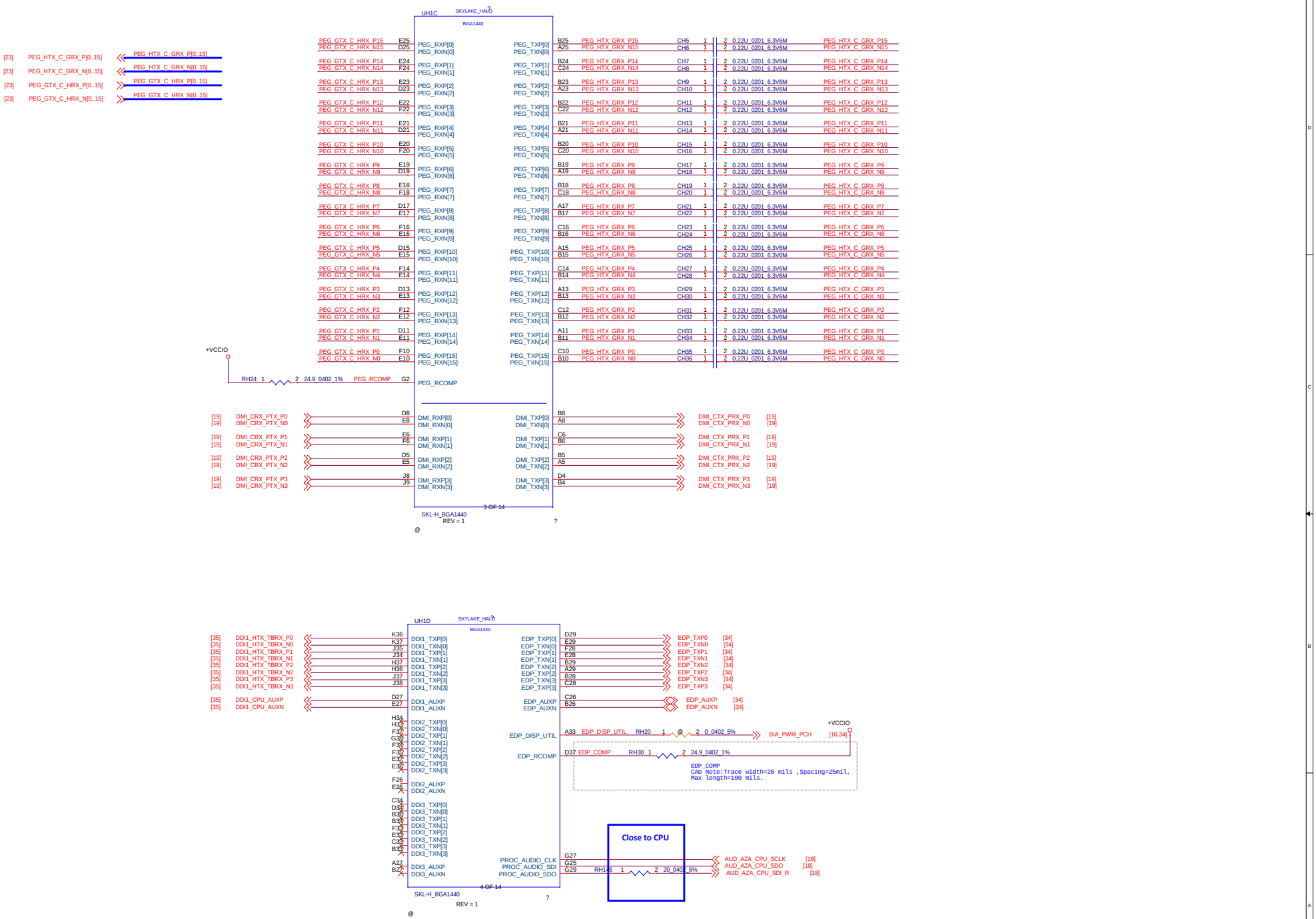
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **XDP CONN**

Size	Document Number	Rev
		0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 6 of 70



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

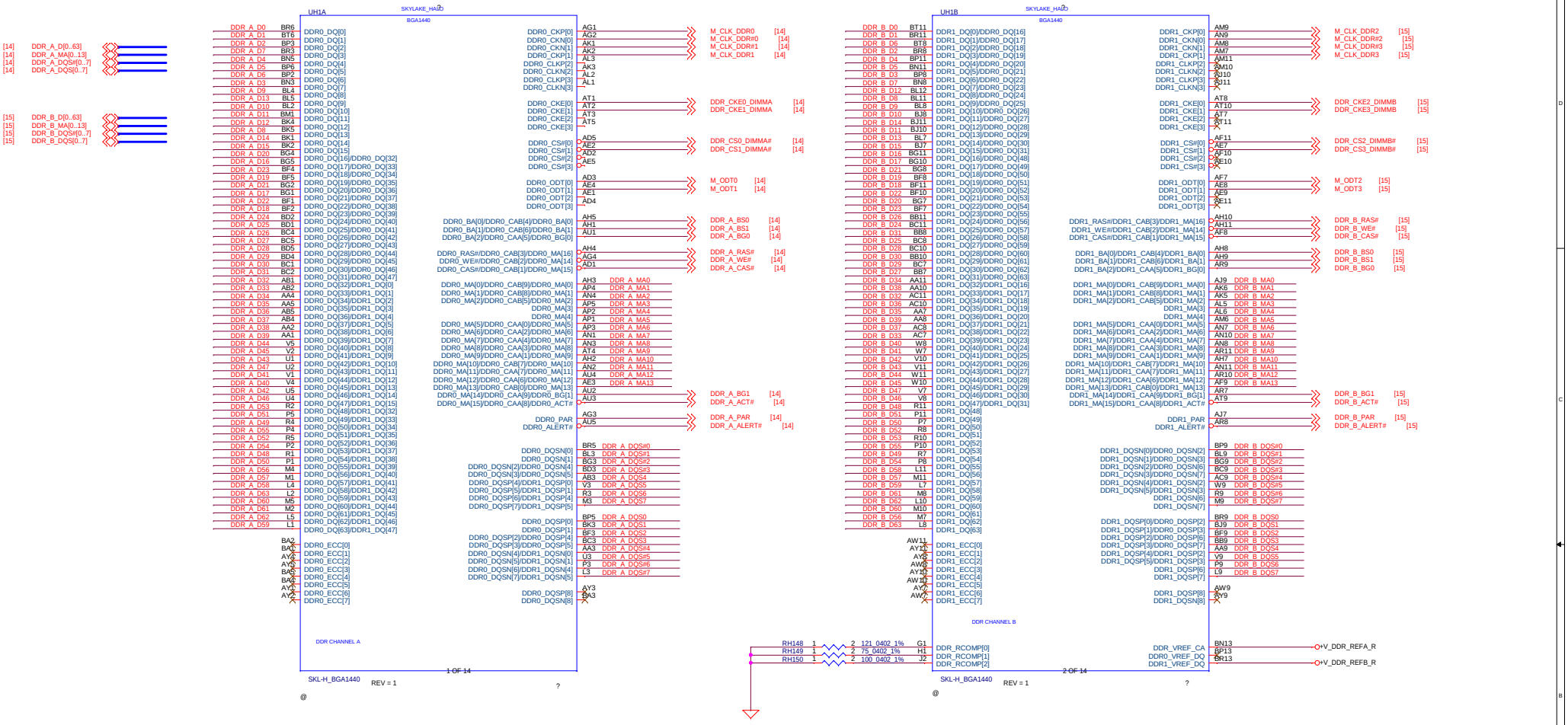
Compal Electronics, Inc.

Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
C		0.1(X00)

Date: Thursday, August 18, 2016 Sheet 7 of 70

Interleave



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(3/7) DDRIII**

Size	Document Number	Rev
C		0.1(000)

Date: Thursday, August 18, 2016 | Sheet 8 of 70

CFG Straps for Processor

Stall reset sequence after CPU PLL lock until de-asserted	
CFG0	* 1 = (Default) Normal Operation; No stall. 0 = Stall.

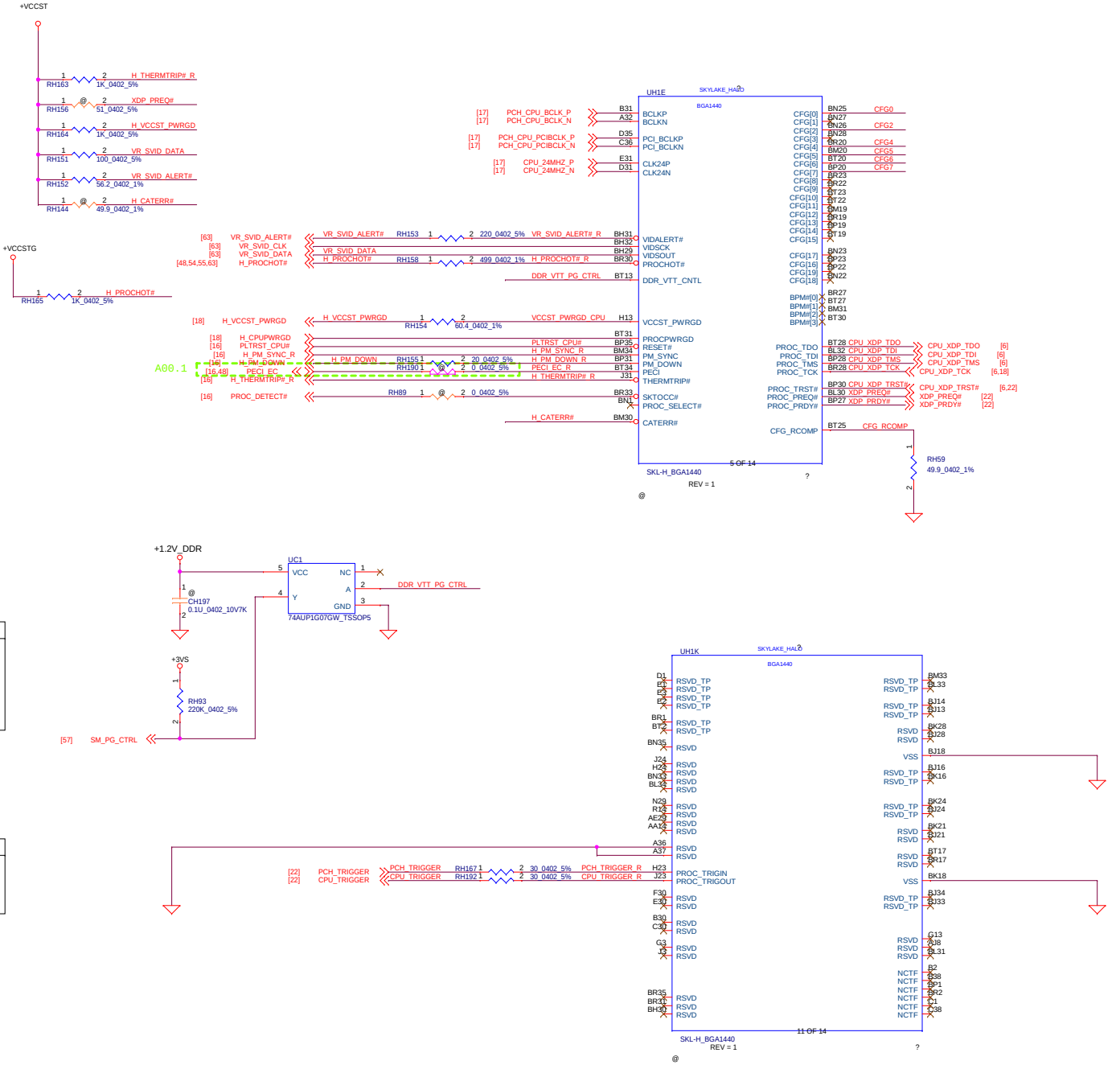
PCI EXPRESS STATIC LANE REVERSAL FOR ALL PEG PORTS	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Enable because PS175(DP to HDMI Converter

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



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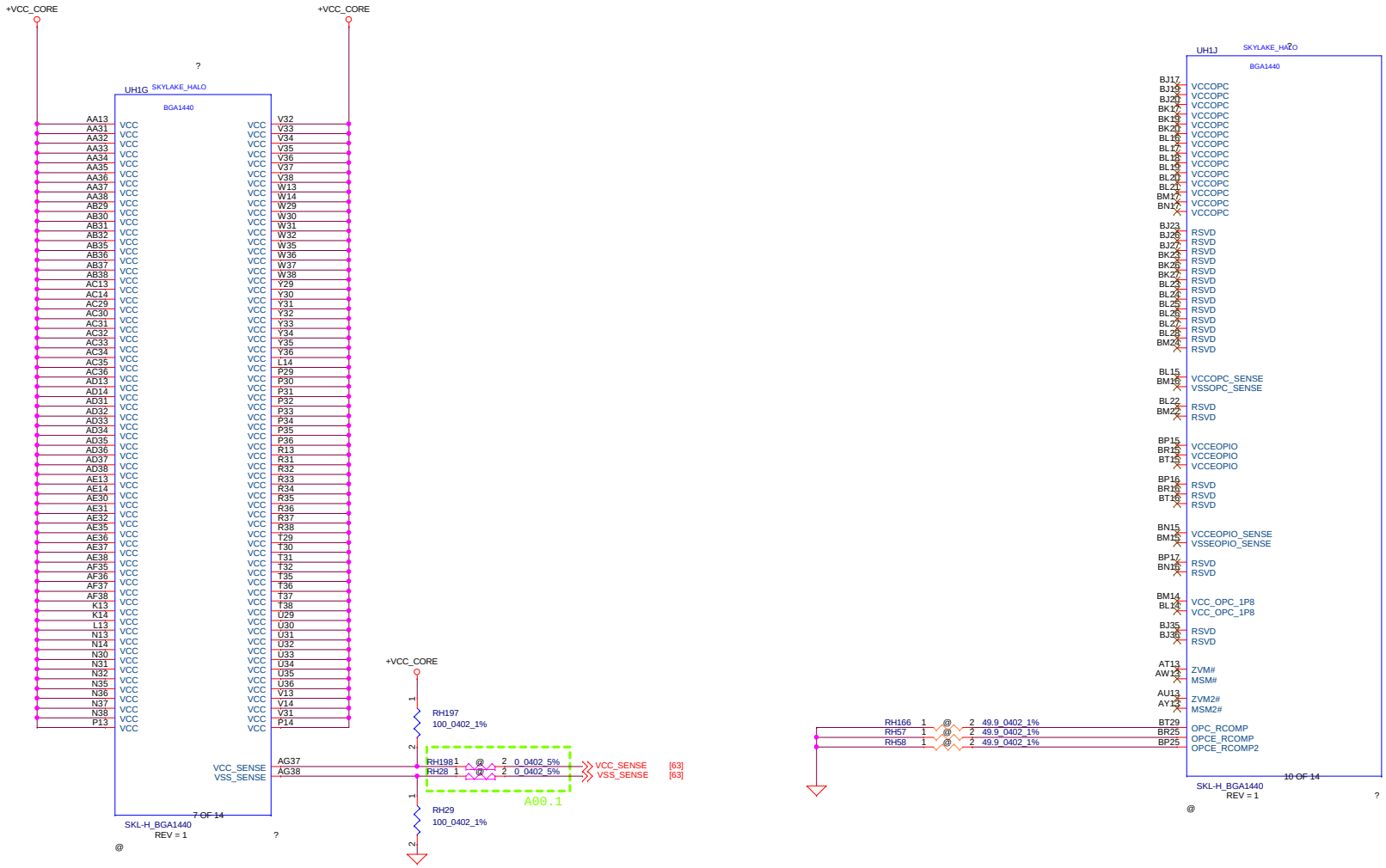
Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

Size	Document Number	Rev
C		0.1(X00)

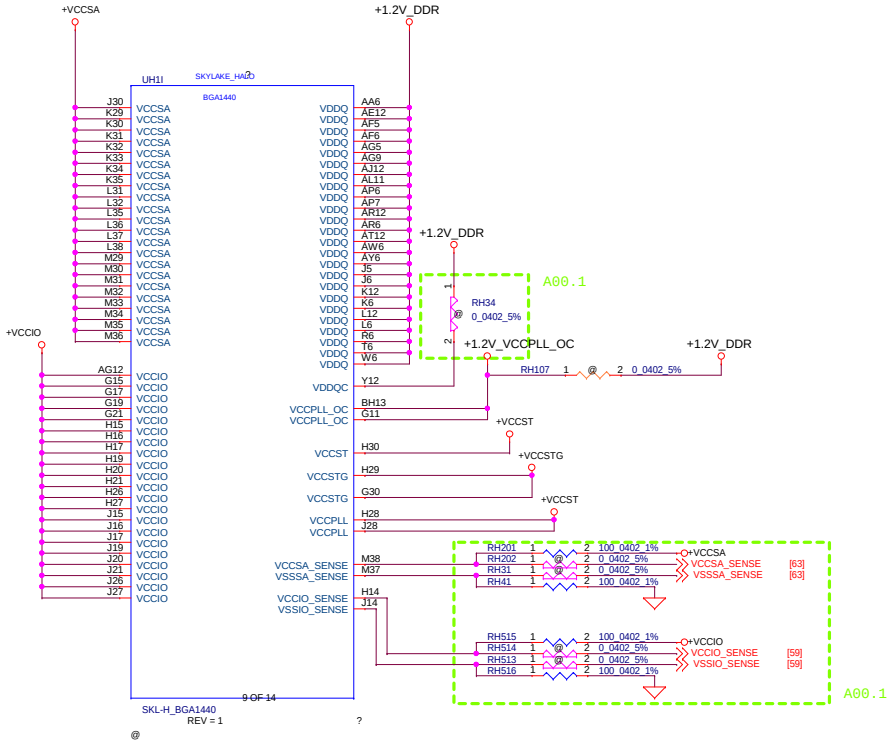
Date: Thursday, August 18, 2016 Sheet 9 of 70

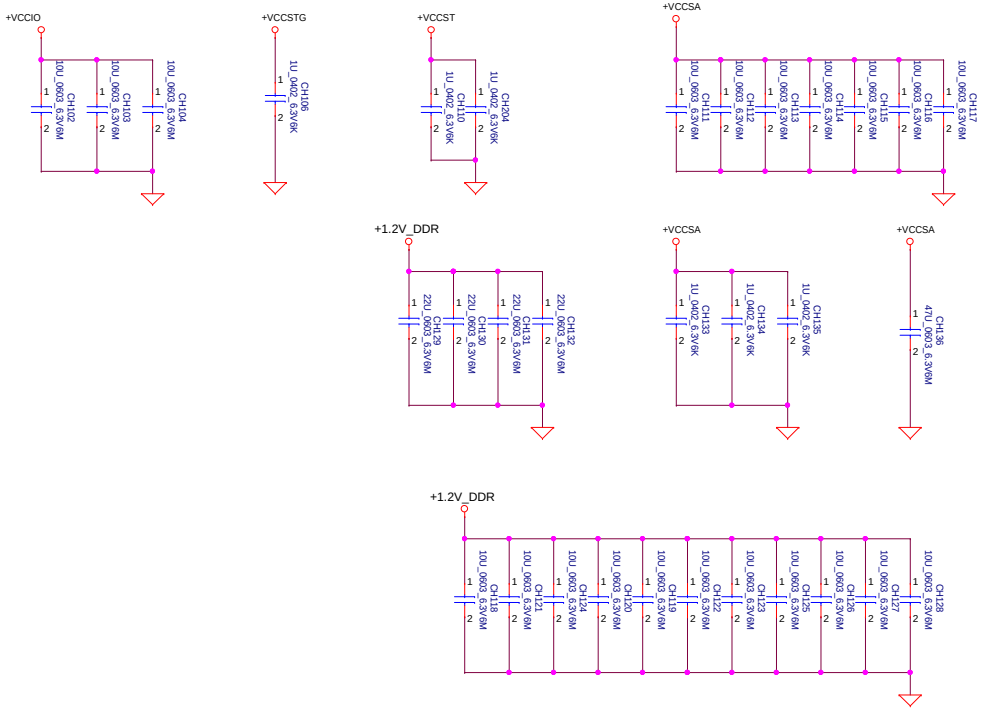


Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title: **PROCESSOR(5/7) PWR,BYPASS**

Size: Custom	Document Number	Rev: 0.1(X00)
Date: Thursday, August 18, 2016	Sheet 10 of 70	





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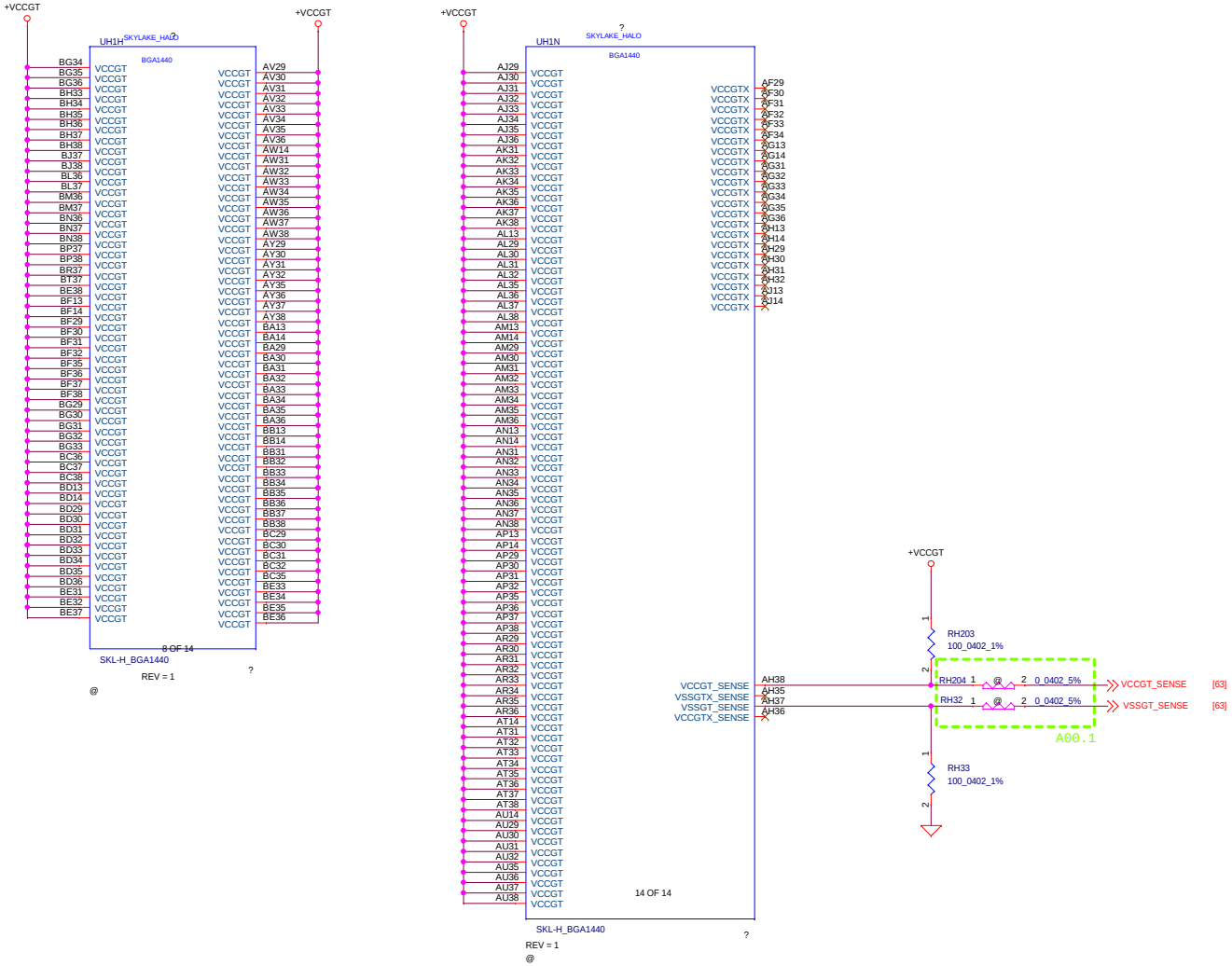
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PROCESSOR(6/7) PWR**

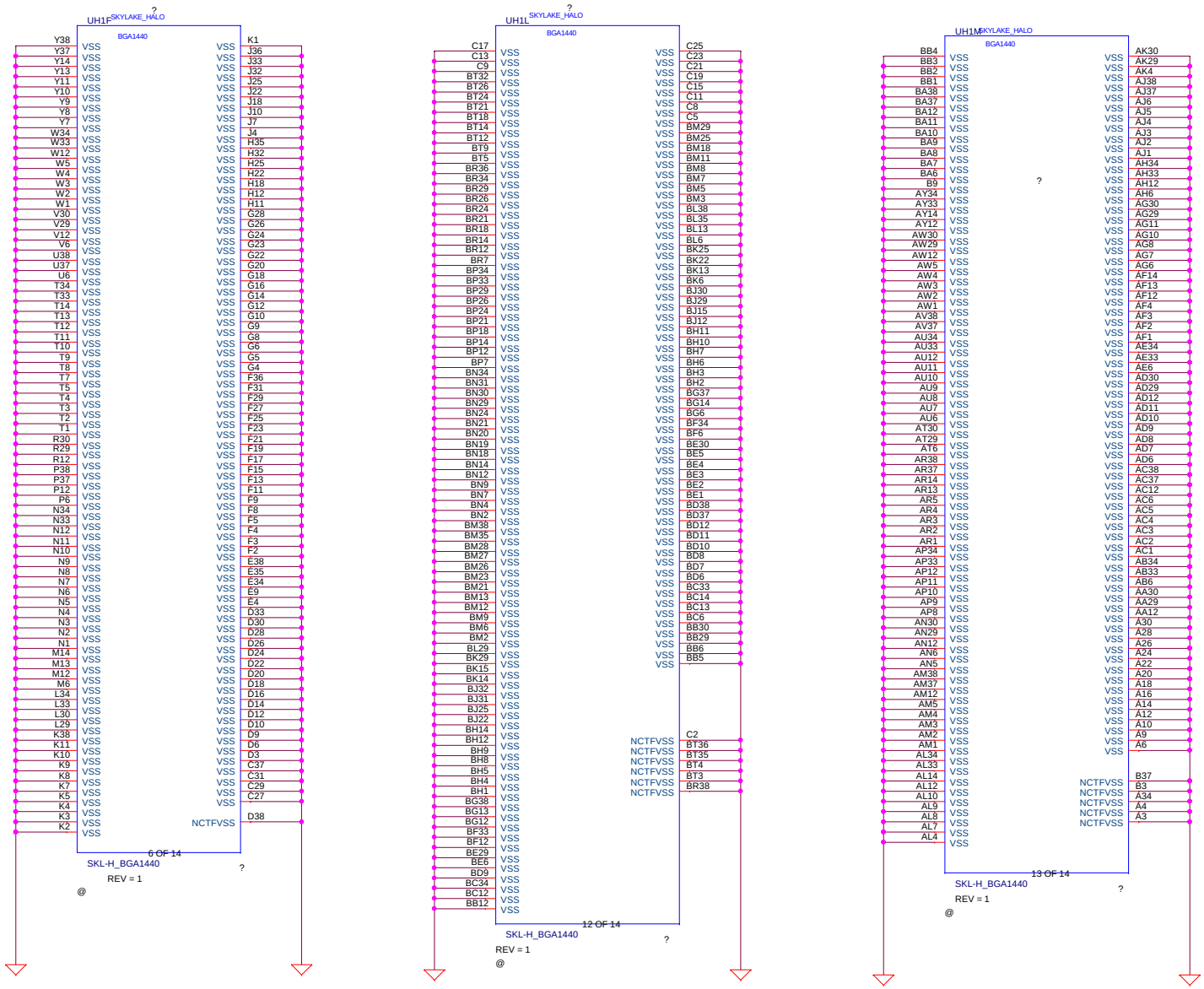
Size	Document Number	Rev
Custom		0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 11 of 70



Security Classification	Compal Secret Data	*Compal Electronics, Inc.*	
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title	*PROCESSOR(2/7) PM,XDP,CLK*		
Size: Custom	Document Number		Rev: 0.1(X00)
Date: Thursday, August 18, 2016	Sheet 12 of 70		



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

Size: Custom | Document Number | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 13 of 70

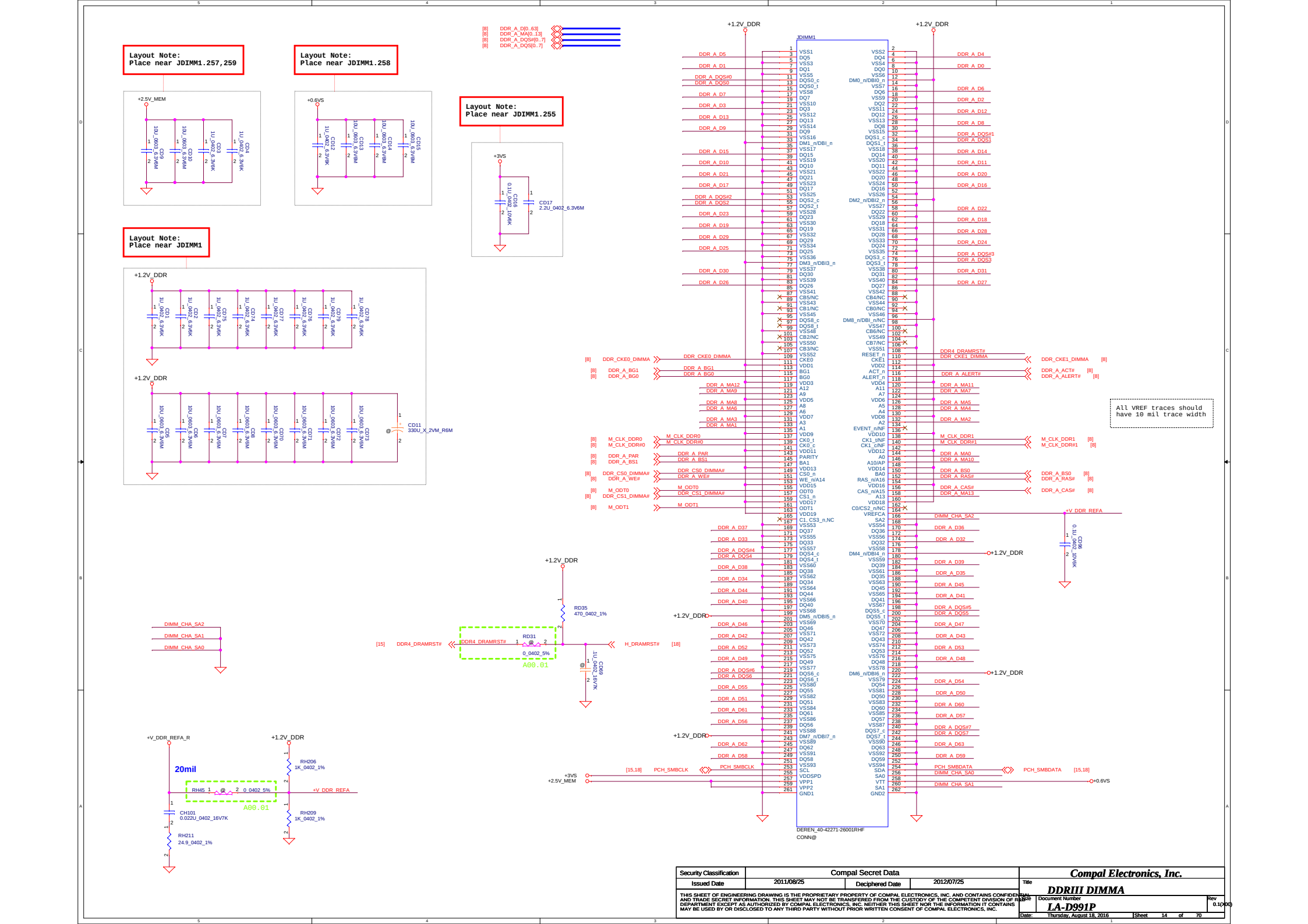
Layout Note:
Place near JDIMM1.257,259

Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM1.255

Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: DDRIII DIMMA			
Size	Document Number: LA-D991P		Rev: 0.1(DD)
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Layout Note:
Place near JDIMM1.258

Layout Note:
Place near JDIMM2.257,259

Layout Note:
Place near JDIMM2.255

Layout Note:
Place near JDIMMB

[8] DDR_B_D[0..63]
[8] DDR_B_MA[0..13]
[8] DDR_B_DQS#[0..7]
[8] DDR_B_DQS[0..7]

+0.6VS
CD32 1U_0402_6.3V6K
CD90 10U_0603_6.3V6M
CD89 10U_0603_6.3V6M
CD88 10U_0603_6.3V6M

+2.5V_MEM
CD30 1U_0402_6.3V6K
CD31 1U_0402_6.3V6K
CD91 10U_0603_6.3V6M
CD27 10U_0603_6.3V6M
CD28 10U_0603_6.3V6M

+3VS
CD34 0.1U_0402_16V7K
CD35 2.2U_0402_6.3V6M

+1.2V_DDR
CD19 1U_0402_6.3V6K
CD20 1U_0402_6.3V6K
CD21 1U_0402_6.3V6K
CD22 1U_0402_6.3V6K
CD83 1U_0402_6.3V6K
CD81 1U_0402_6.3V6K
CD80 1U_0402_6.3V6K
CD82 1U_0402_6.3V6K

+1.2V_DDR
CD23 10U_0603_6.3V6M
CD24 10U_0603_6.3V6M
CD25 10U_0603_6.3V6M
CD26 10U_0603_6.3V6M
CD87 10U_0603_6.3V6M
CD85 10U_0603_6.3V6M
CD84 10U_0603_6.3V6M
CD86 10U_0603_6.3V6M
CD33 330U_2.5V_M

JDIMM2
JP3

+1.2V_DDR
DDR_B_D5 DDR_B_D1 DDR_B_DQS#0 DDR_B_DQS0 DDR_B_D7 DDR_B_D3 DDR_B_D13 DDR_B_D9 DDR_B_D15 DDR_B_D10 DDR_B_D21 DDR_B_D17 DDR_B_DQS#2 DDR_B_DQS2 DDR_B_D23 DDR_B_D19 DDR_B_D29 DDR_B_D25
DDR_B_D30 DDR_B_D26
[8] DDR_CKE2_DIMMB DDR_CKE2_DIMMB
[8] DDR_B_BG1 DDR_B_BG0
DDR_B_MA12 DDR_B_MA9 DDR_B_MA8 DDR_B_MA6 DDR_B_MA3 DDR_B_MA1
[8] M_CLK_DDR2 [8] M_CLK_DDR#2
DDR_B_PAR [8] DDR_B_BS1
[8] DDR_CS2_DIMMB# [8] DDR_B_WE#
[8] M_ODT2 [8] DDR_CS3_DIMMB#
[8] M_ODT3
DDR_B_D37 DDR_B_D33 DDR_B_DQS#4 DDR_B_DQS4 DDR_B_D38 DDR_B_D34 DDR_B_D44 DDR_B_D40
+1.2V_DDR
DDR_B_D46 DDR_B_D42 DDR_B_D52 DDR_B_D49 DDR_B_DQS#6 DDR_B_DQS6 DDR_B_D55 DDR_B_D51 DDR_B_D61 DDR_B_D56
+1.2V_DDR
DDR_B_D62 DDR_B_D58
[14,18] PCH_SMBCLK PCH_SMBCLK
+3VS +2.5V_MEM
BELLW_SD-80886-1021
CONN@

+1.2V_DDR
DDR_B_D4 DDR_B_D0 DDR_B_D6 DDR_B_D2 DDR_B_D12 DDR_B_D8 DDR_B_DQS#1 DDR_B_DQS1 DDR_B_D14 DDR_B_D11 DDR_B_D20 DDR_B_D16
DDR_B_D22 DDR_B_D18 DDR_B_D28 DDR_B_D24
DDR_B_DQS#3 DDR_B_DQS3 DDR_B_D31 DDR_B_D27
DDR4_DRAMRST# [14] DDR_CKE3_DIMMB DDR_CKE3_DIMMB [8]
DDR_B_ACT# [8] DDR_B_ALERT# DDR_B_ALERT# [8]
DDR_B_MA11 DDR_B_MA7 DDR_B_MA5 DDR_B_MA4 DDR_B_MA2
M_CLK_DDR3 M_CLK_DDR#3 [8] M_CLK_DDR3 [8] M_CLK_DDR#3 [8]
DDR_B_MA0 DDR_B_MA10
DDR_B_BS0 [8] DDR_B_RAS# DDR_B_BS0 [8] DDR_B_RAS# [8]
DDR_B_CAS# DDR_B_MA13 DDR_B_CAS# [8]
+V_DDR_REFB
DIMM_CHB_SA2
CD208 0.1U_0402_10V6K
DDR_B_D36 DDR_B_D32
+1.2V_DDR
DDR_B_D39 DDR_B_D35 DDR_B_D45 DDR_B_D41 DDR_B_DQS#5 DDR_B_DQS5 DDR_B_D47 DDR_B_D43 DDR_B_D53 DDR_B_D48
+1.2V_DDR
DDR_B_D54 DDR_B_D50 DDR_B_D60 DDR_B_D57 DDR_B_DQS#7 DDR_B_DQS7 DDR_B_D63 DDR_B_D59
PCH_SMBDATA PCH_SMBDATA [14,18]
DIMM_CHB_SA0
DIMM_CHB_SA1
+0.6VS

All VREF traces should have 10 mil trace width

+3VS
DIMM_CHB_SA1
DIMM_CHB_SA2
DIMM_CHB_SA0

+V_DDR_REFB_R
+1.2V_DDR
RH207 1K_0402_1%
20mil
RH46 1 @ 2 0_0402_5%
+V_DDR_REFB
A00.01
CH100 0.022U_0402_16V7K
RH210 1K_0402_1%
RH212 24.9_0402_1%

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Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: DDRIII DIMMB

Size: Document Number: LA-D991P Rev: 0.1(DD)

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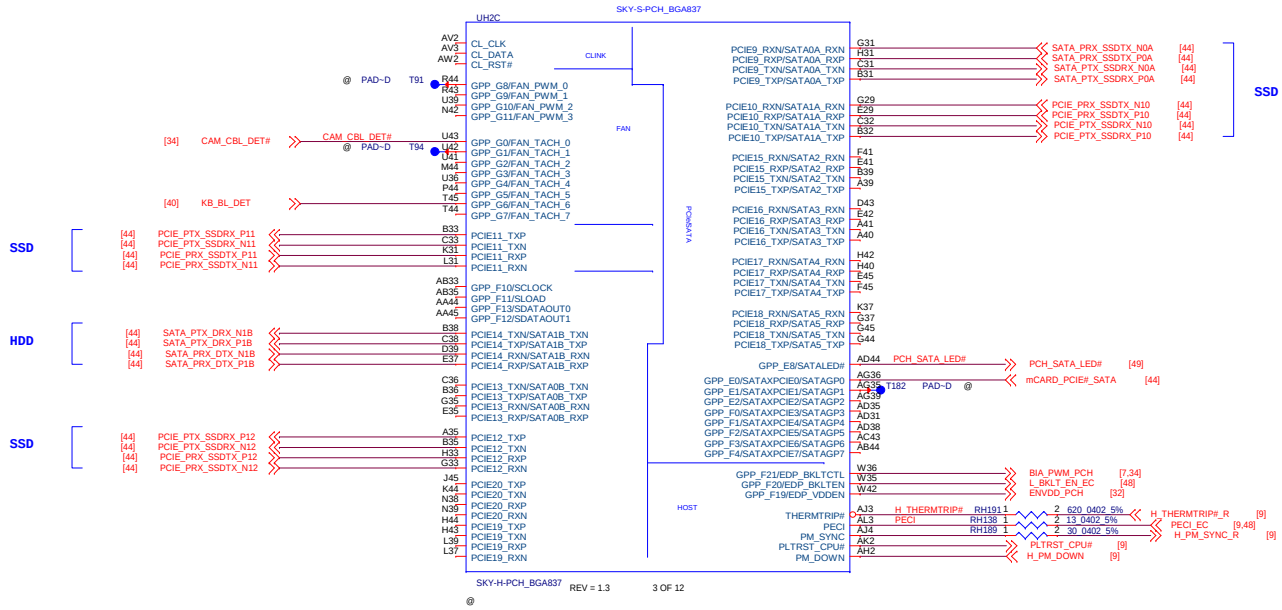

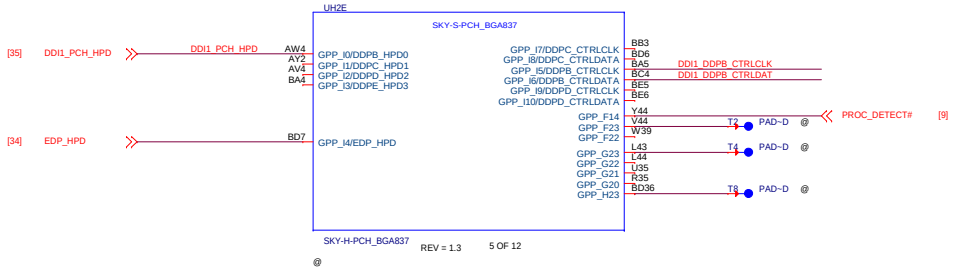

PCH Strap PIN

DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-kΩ ±5% resistor	No Connect

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Issued Date	2011/08/25	Deciphered Date	2012/07/25

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Title: PCH (1/8) SATA,HDA

Size | Document Number: LA-C361P | Rev: 0.1(XXX)

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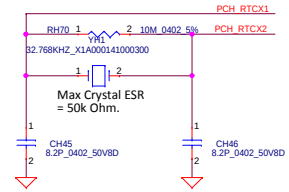
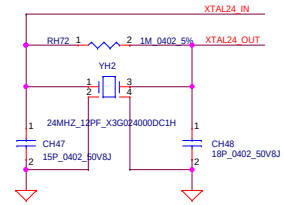
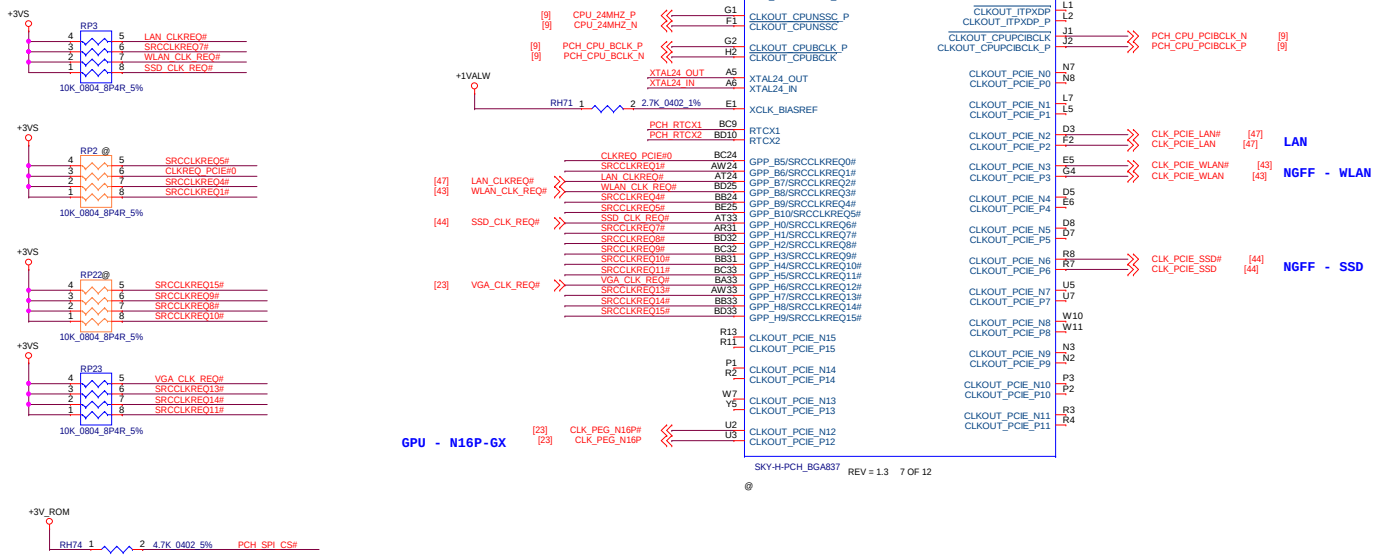
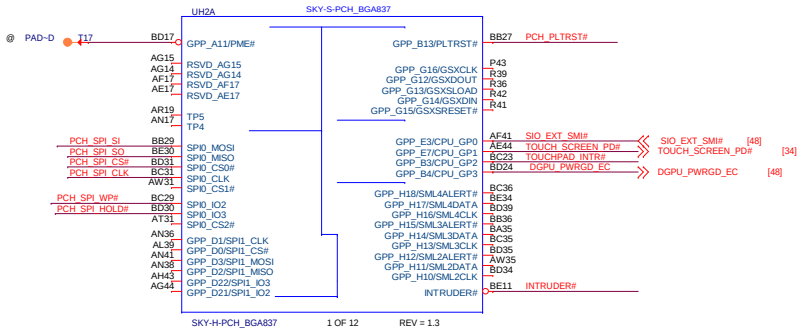
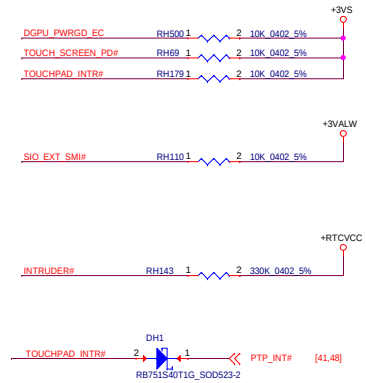
RTC CRYSTAL



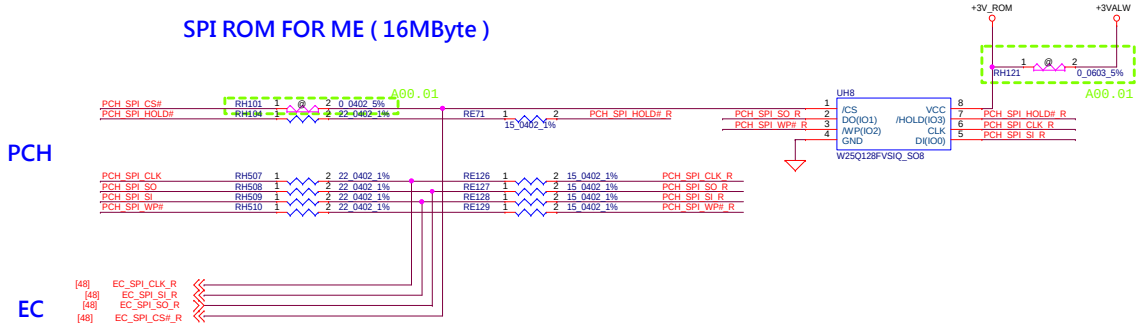


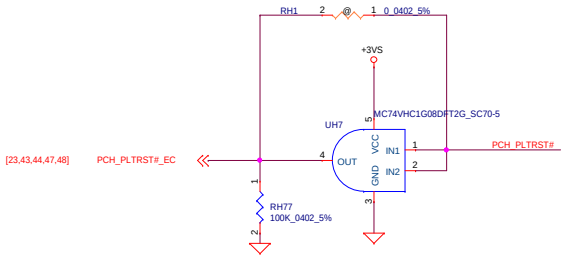






SPI ROM FOR ME (16MByte)





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: PCH (2/8) SMBUS, CLK, SPI, LPC

Size	Document Number	Rev
	LA-D991P	0.1(XXX)

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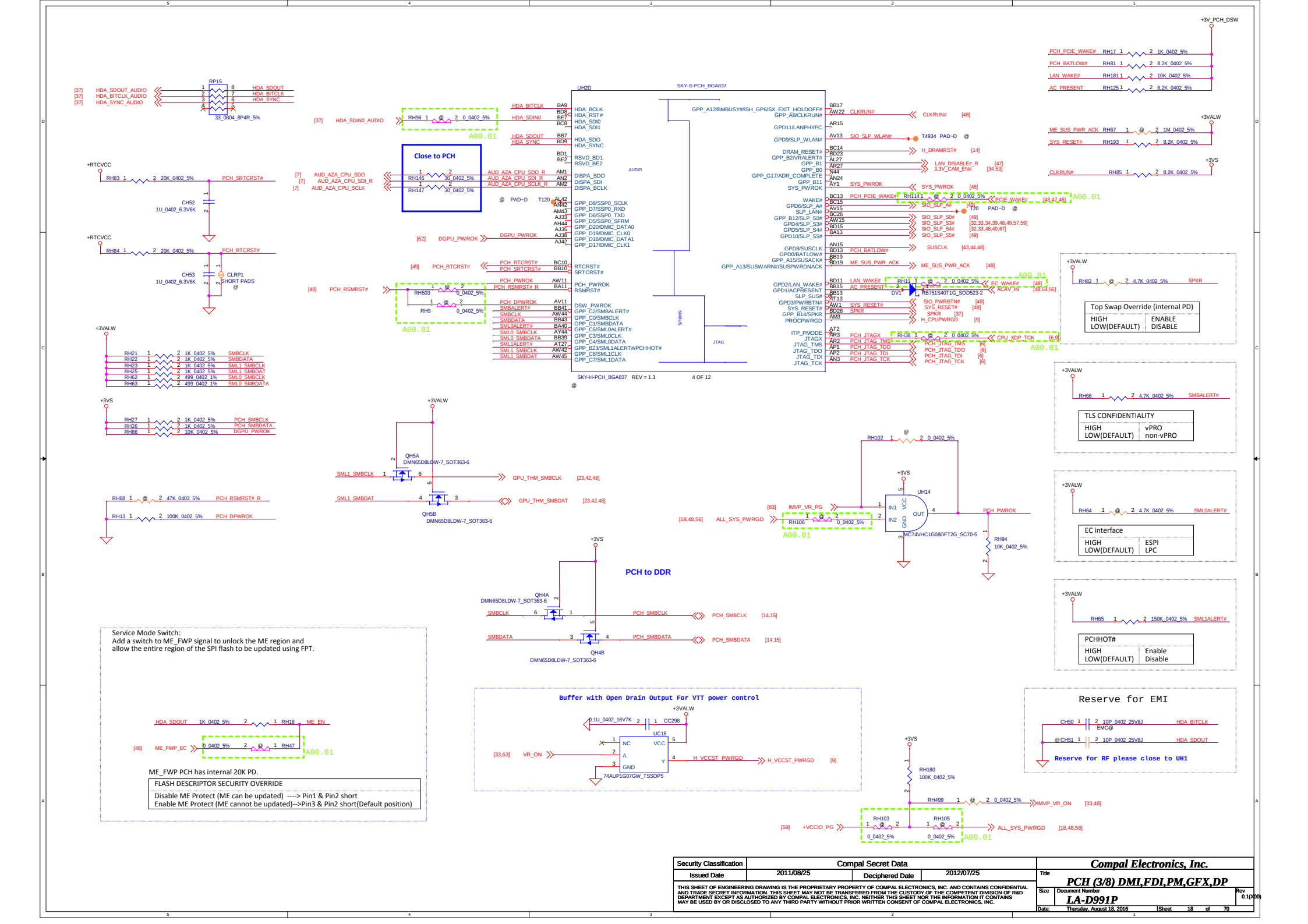
Close to PCH
PCH to DDR
Service Mode Switch:
Add a switch to ME_FWP signal to unlock the ME region and
allow the entire region of the SPI flash to be updated using FPT.
ME_FWP PCH has internal 20K PD.
FLASH DESCRIPTOR SECURITY OVERRIDE
Disable ME Protect (ME can be updated) ----> Pin1 & Pin2 short
Enable ME Protect (ME cannot be updated)-->Pin3 & Pin2 short(Default position)
Buffer with Open Drain Output For VTT power control
Top Swap Override (internal PD)
HIGH ENABLE
LOW(DEFAULT) DISABLE
TLS CONFIDENTIALITY
HIGH vPRO
LOW(DEFAULT) non-vPRO
EC interface
HIGH ESPI
LOW(DEFAULT) LPC
PCHHOT#
HIGH Enable
LOW(DEFAULT) Disable
Reserve for EMI
Reserve for RF please close to UH1
Security Classification Compal Secret Data
Issued Date 2011/08/25 Deciphered Date 2012/07/25
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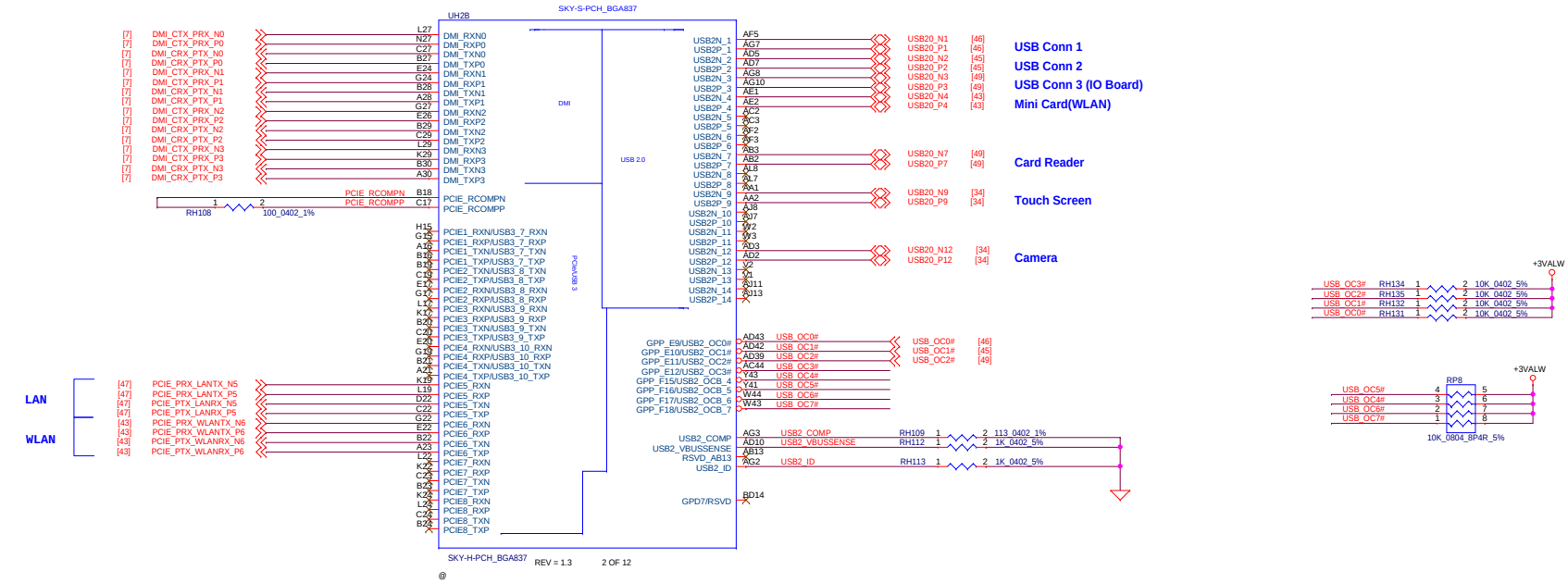
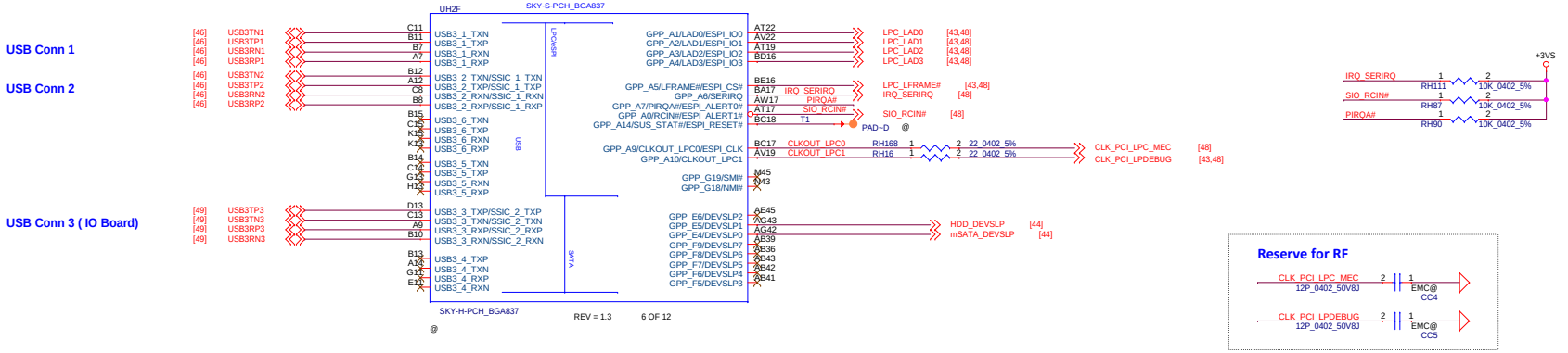
Size Document Number LA-D991P Rev 0.1(000)
Date: Thursday, August 18, 2016 Sheet 18 of 70





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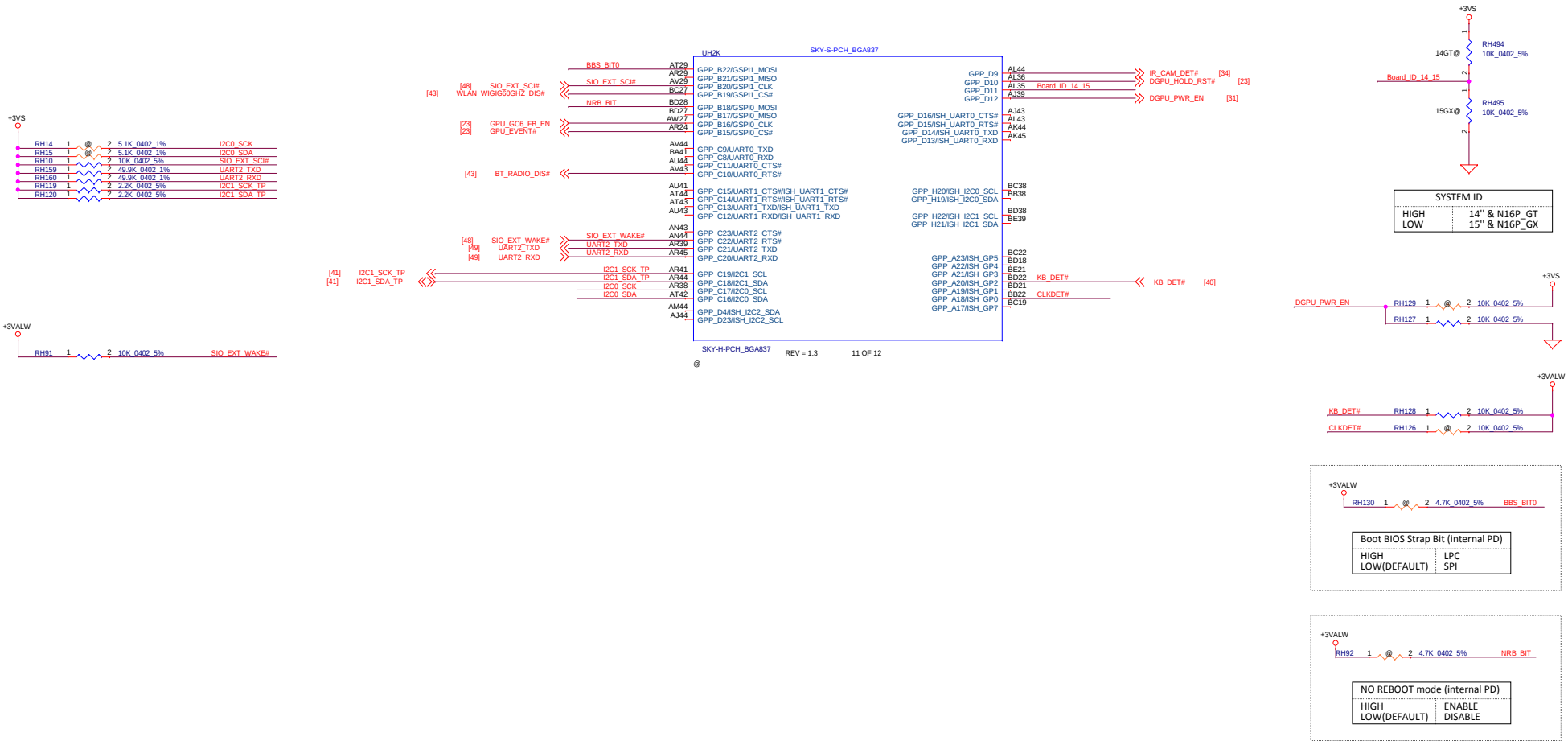
Compal Electronics, Inc.

Title: **PCH (4/8) PCI, USB**

Size	Document Number	Rev
	LA-D991P	0.1(XXX)

Date: Thursday, August 18, 2016 | Sheet 19 of 70



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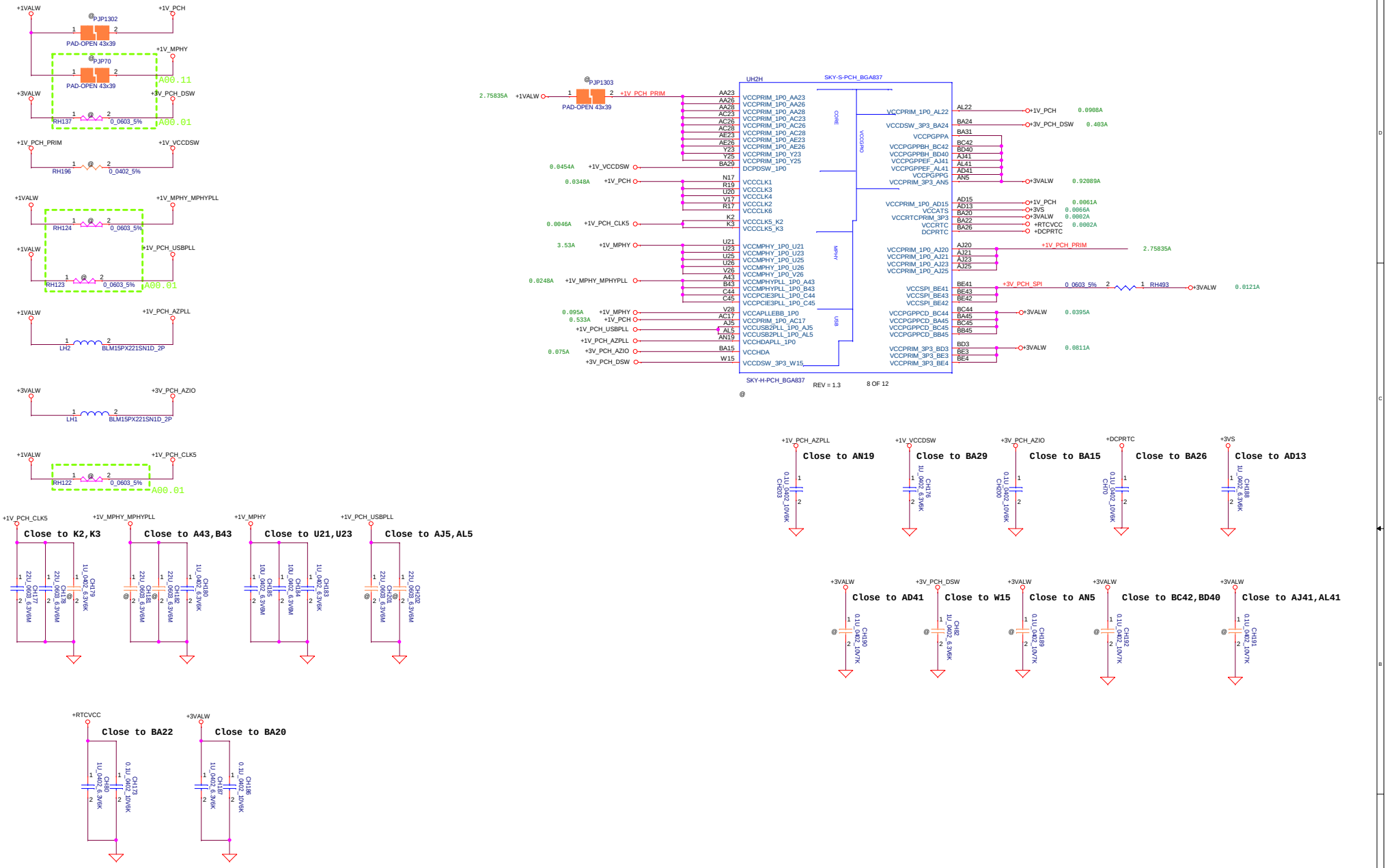
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (5/8) GPIO, CPU, MISC**

Size	Document Number	Rev
	LA-D991P	0.1(XXX)

Date: Thursday, August 18, 2016 Sheet 20 of 70



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (6/8) PWR**

Size	Document Number	Rev
	LA-D991P	0.1(XXX)

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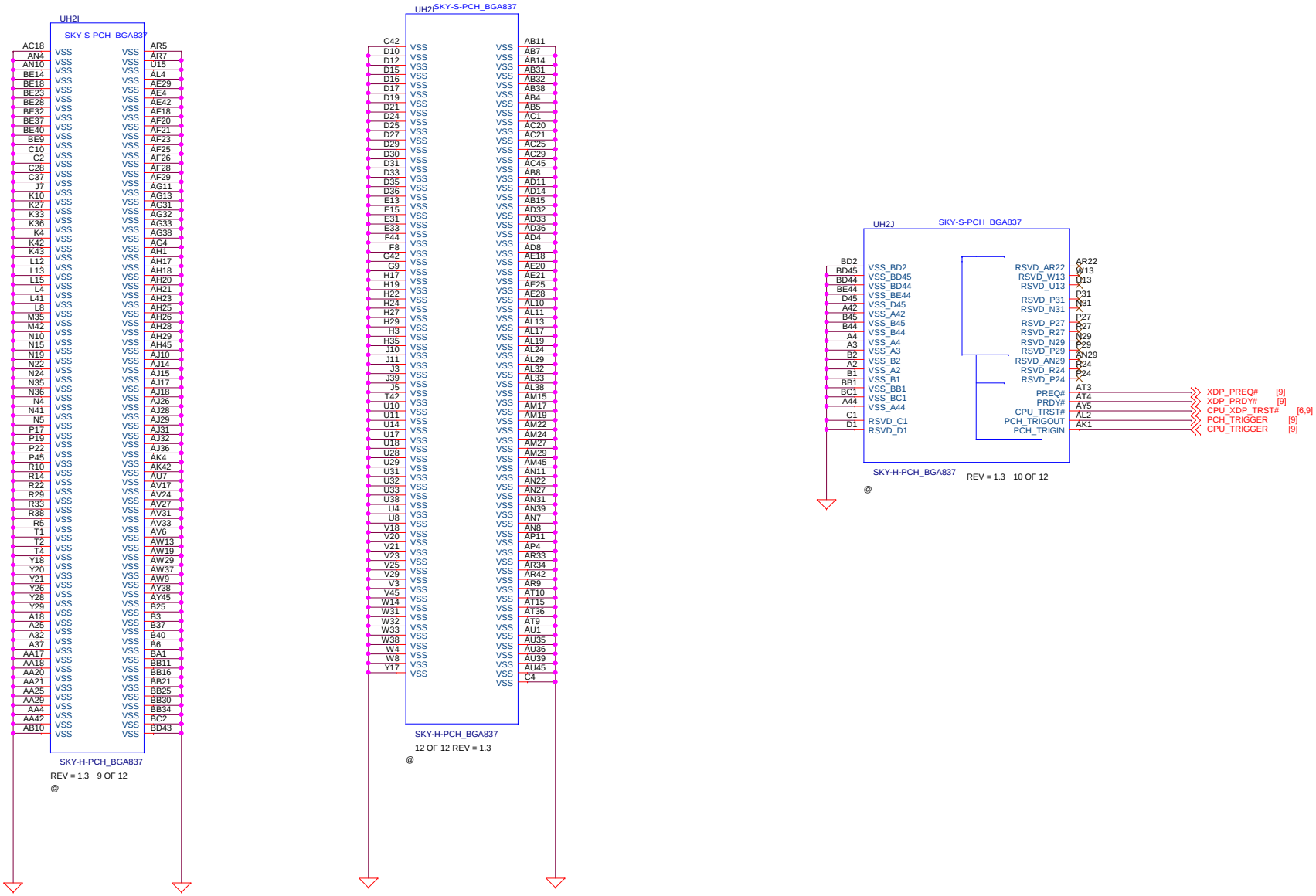

Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PCH (8/8) VSS**

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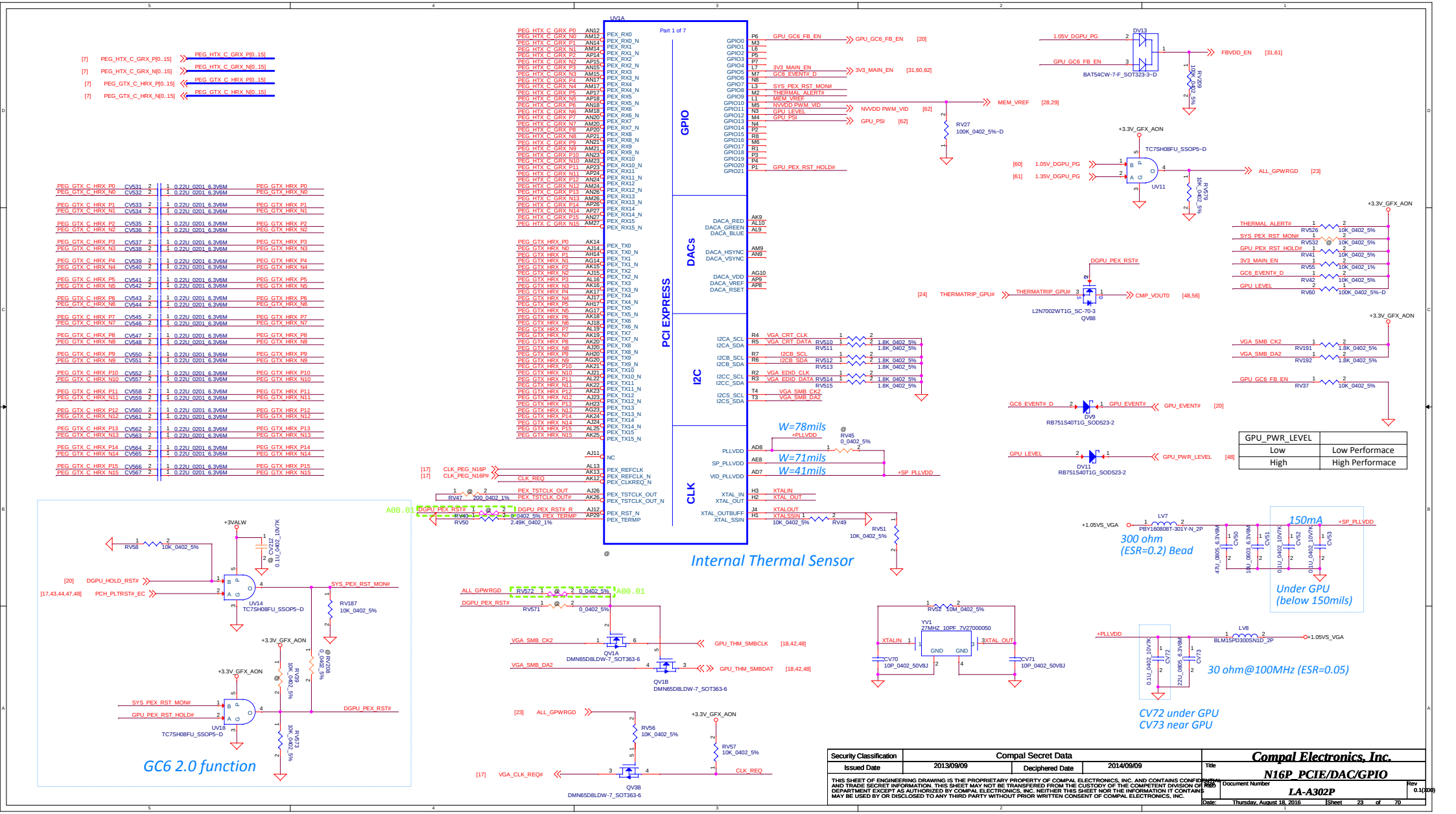
Date: Thursday, August 18, 2016 | Sheet 22 of 70



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Issued Date	2013/09/09
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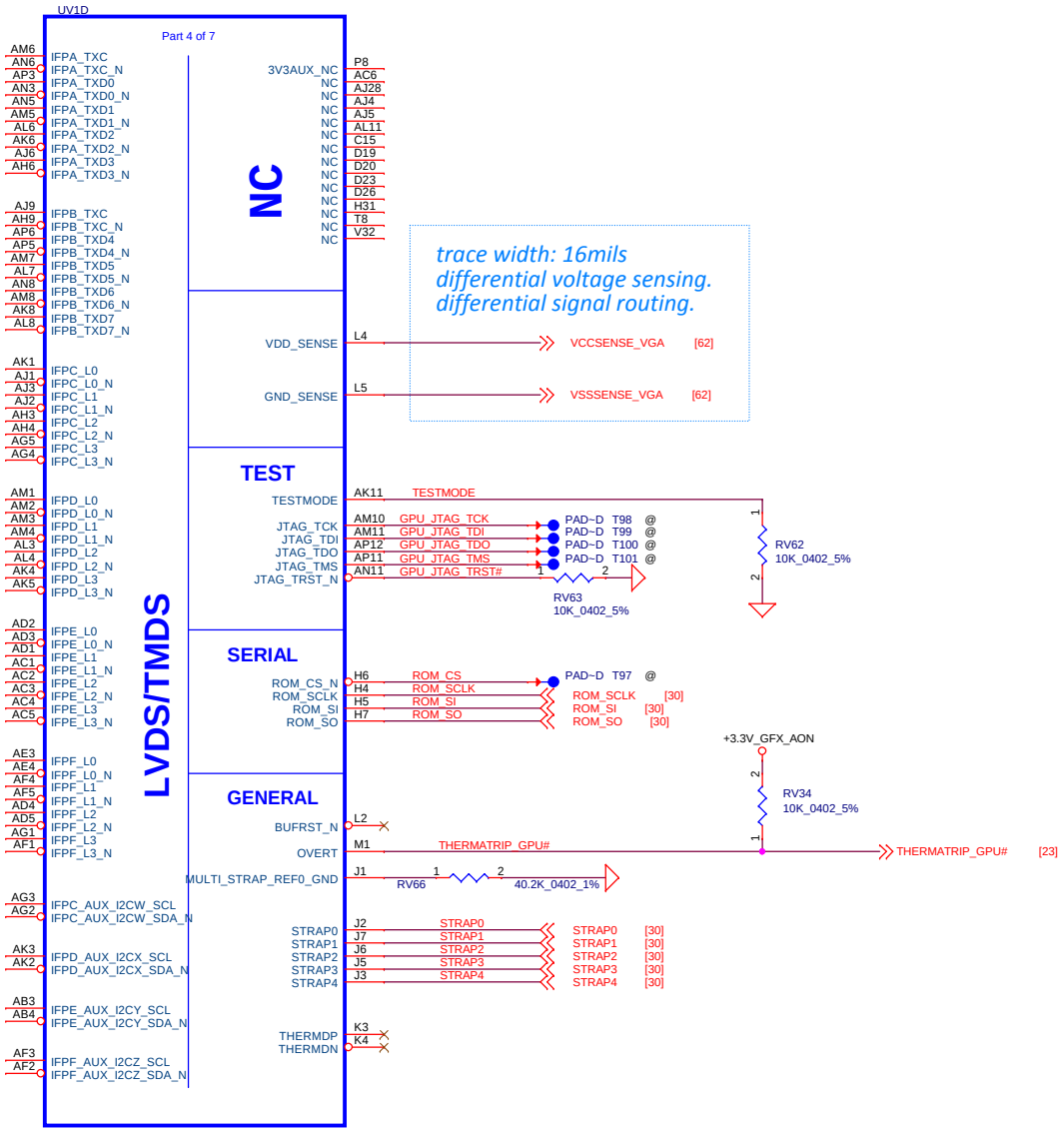
Compal Electronics, Inc.

Title: N16P_PCIE/DAC/GPIO

Size: C | Document Number: LA-A302P | Rev: 0.1(100)

Date: Thursday, August 18, 2016 | Sheet 23 of 70



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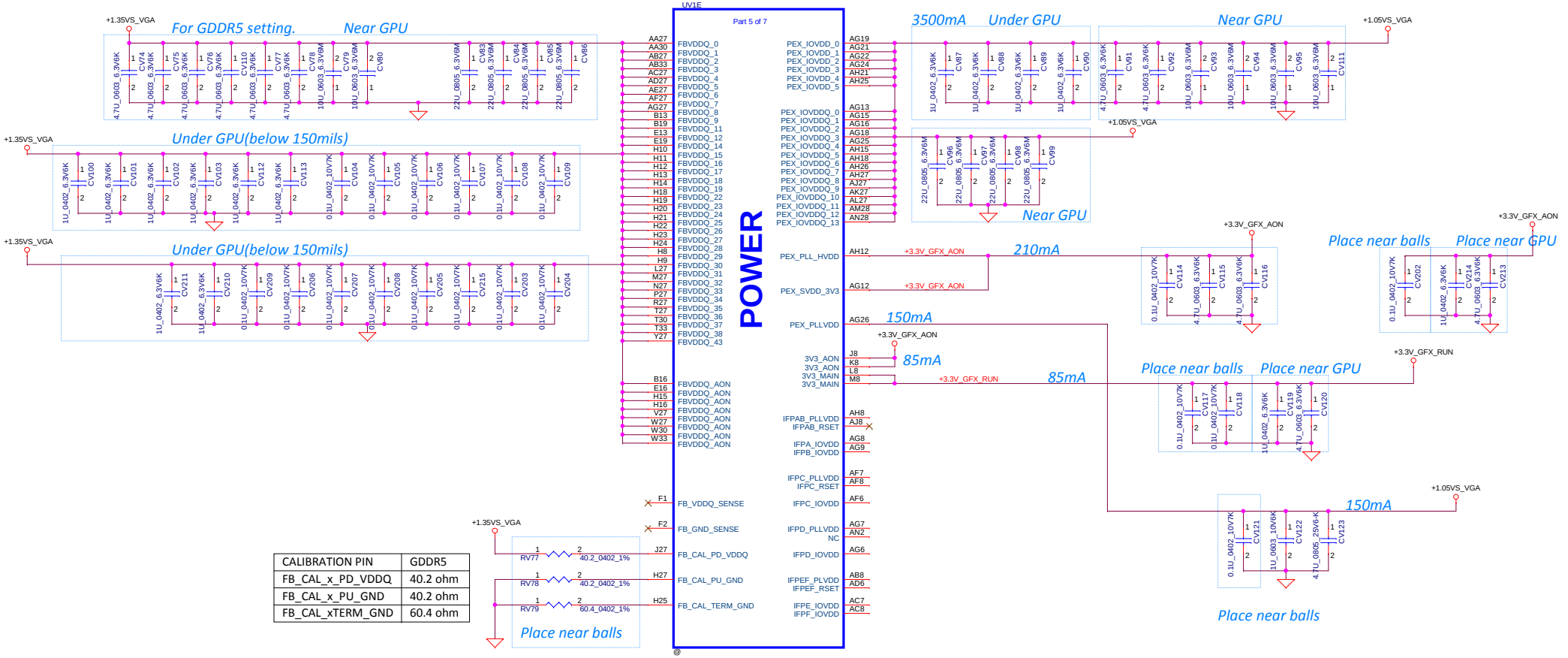
Compal Electronics, Inc.

Title: **N16P_eDP/HDMI/mDP**

Size | Document Number: **LA-A302P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 24 of 70



CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2 ohm
FB_CAL_x_PU_GND	40.2 ohm
FB_CAL_xTERM_GND	60.4 ohm

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Compal Electronics, Inc.			
Title	N16P_Power		
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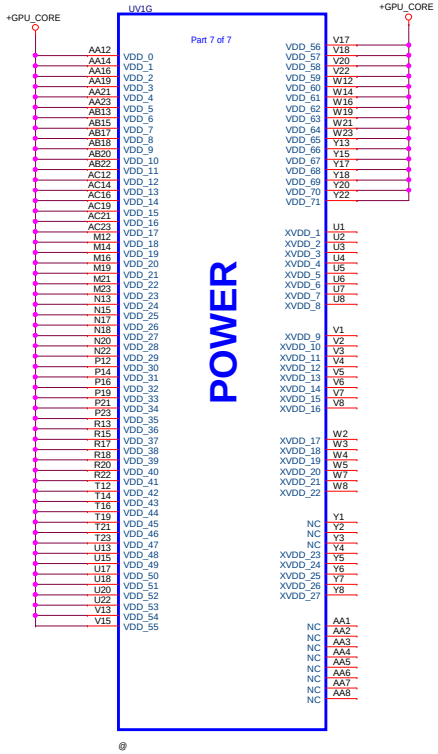
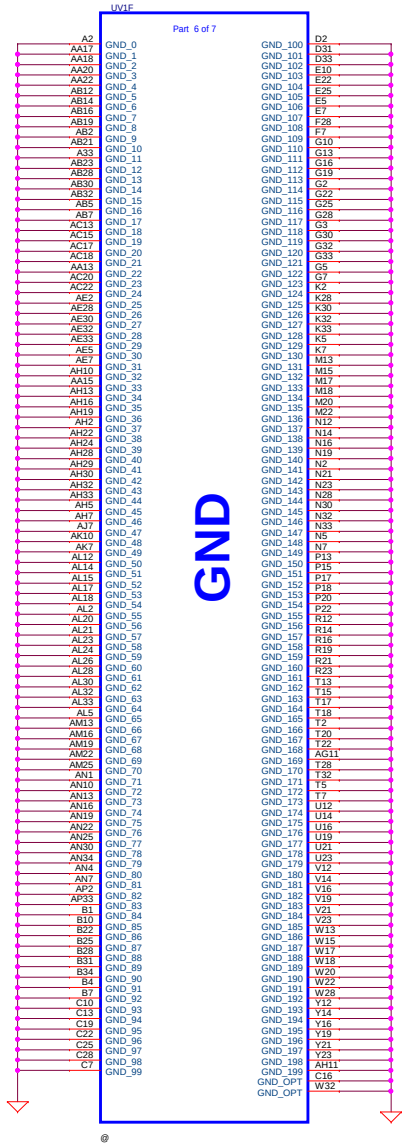
58+30%A





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Compal Electronics, Inc.

Title: **N16P_VGA CORE/GND**

Size	Document Number	Rev
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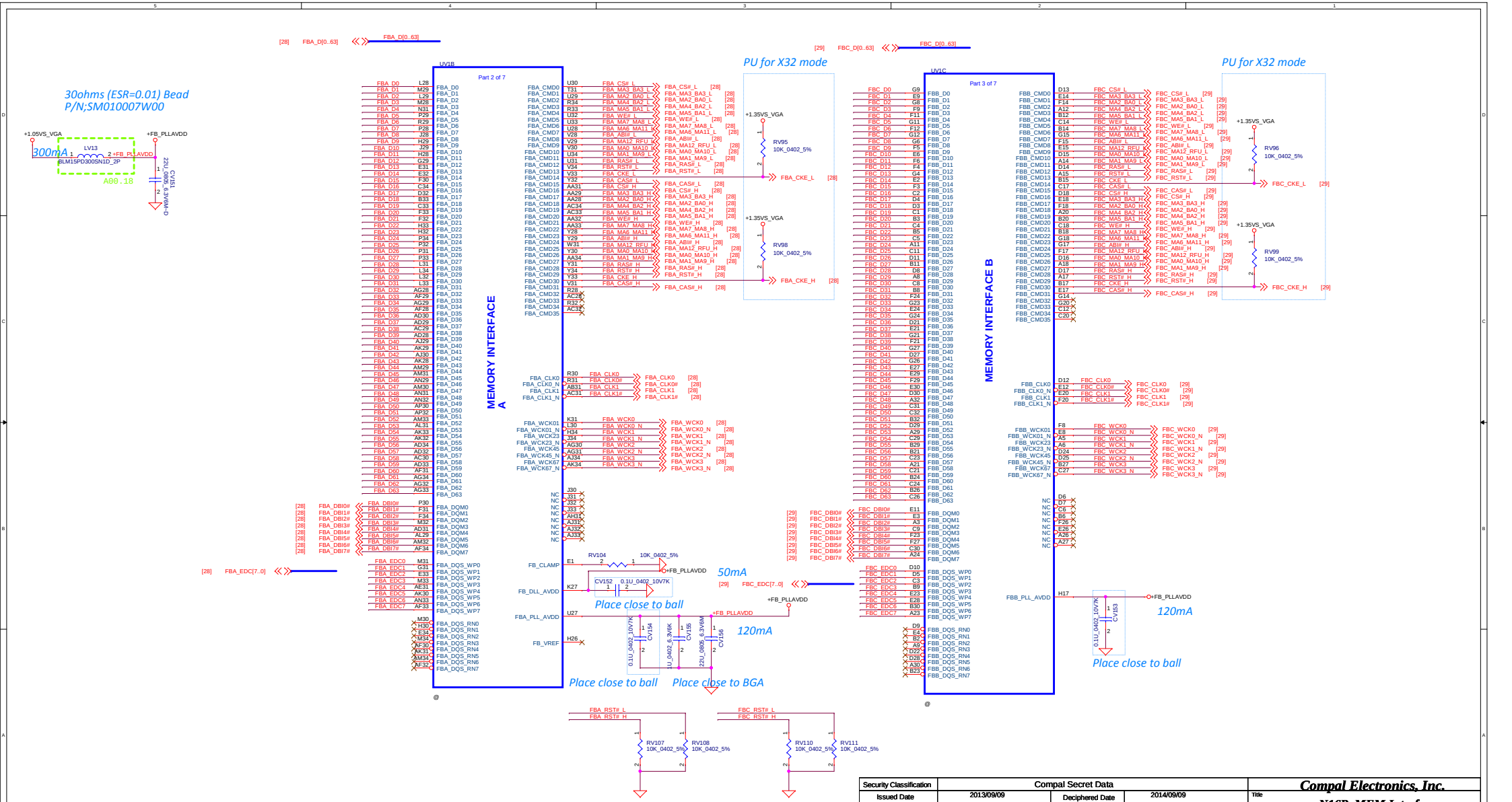

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Compal Electronics, Inc.

Title: **N16P_MEM Interface**

Size: C | Document Number: **LA-A302P** | Rev: 0.1(100)

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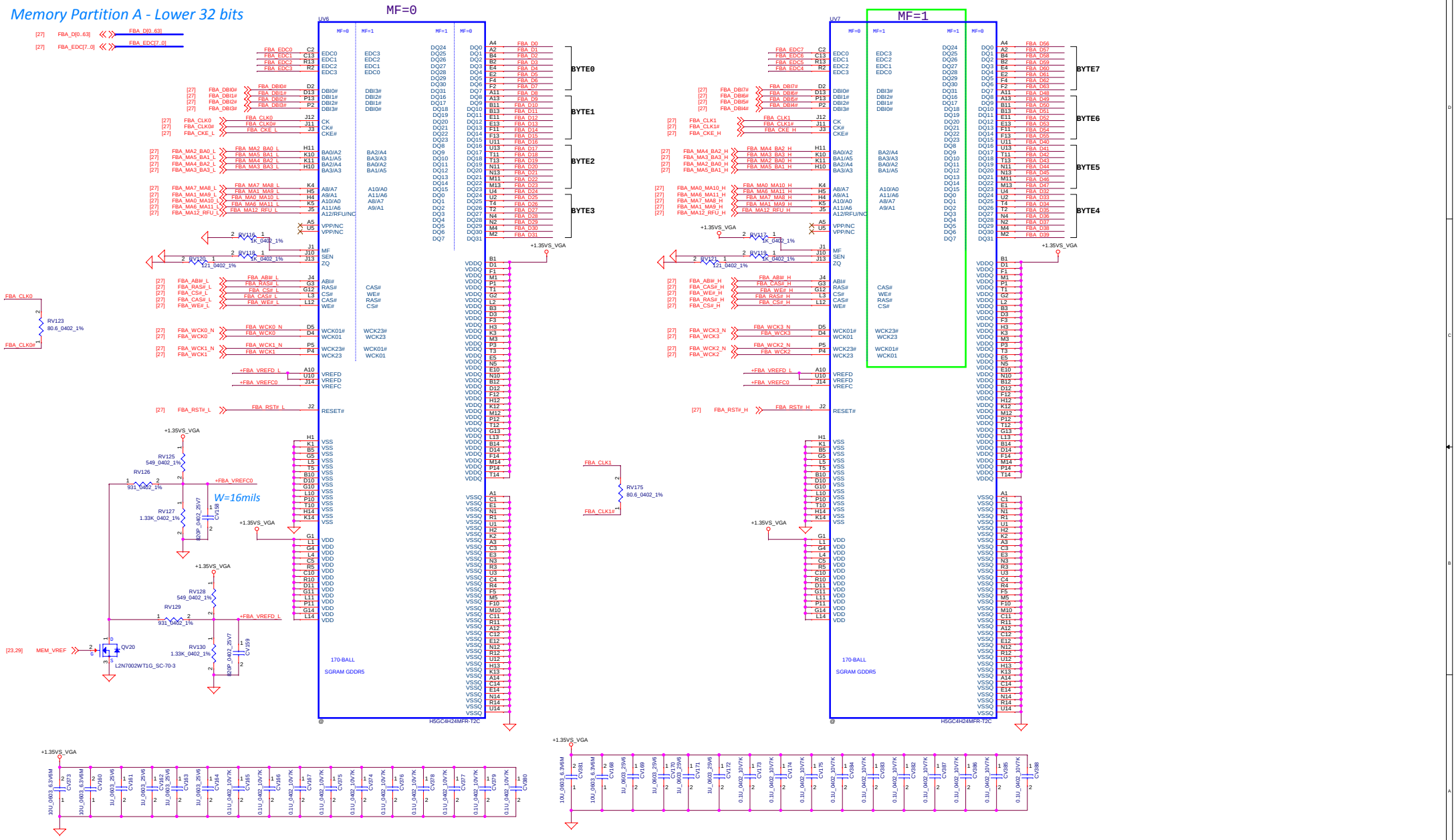
Memory Partition A - Lower 32 bits



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Issued Date	2013/09/09	Deciphered Date	2014/09/09

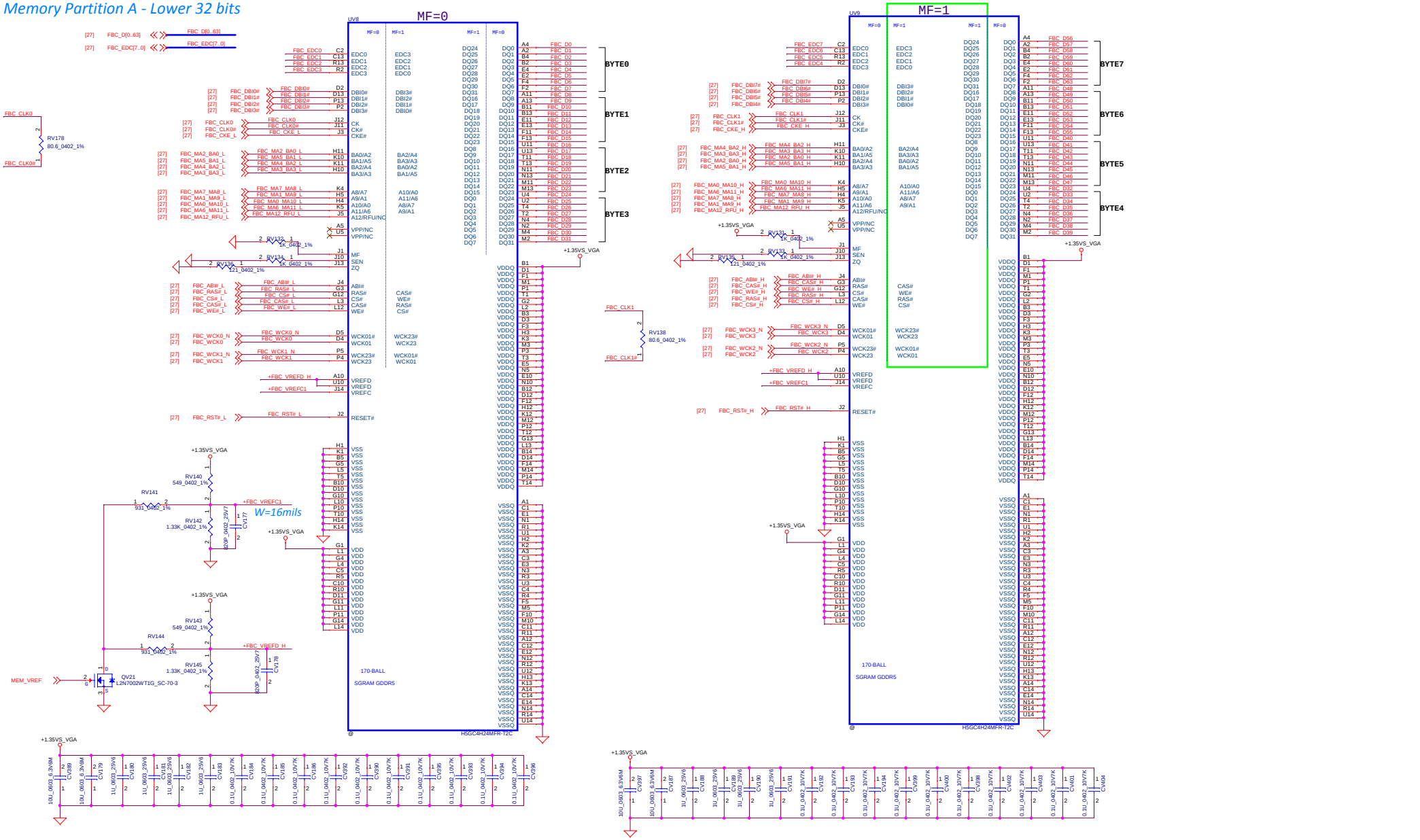
Compal Electronics, Inc.

Title: N16P GDDR5 A

Size: | Document Number: LA-A302P | Rev: 0.1(0.00)

Date: Thursday, August 18, 2016 | Sheet 28 of 70

Memory Partition A - Lower 32 bits



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Compal Electronics, Inc.

Title: **N16P GDDR5 B**

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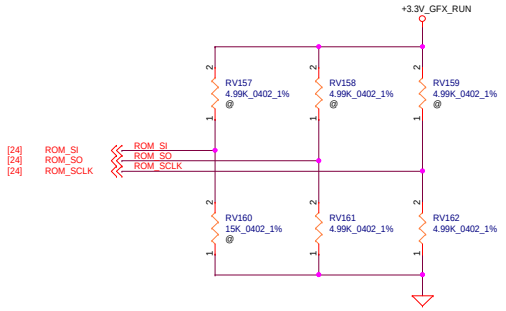

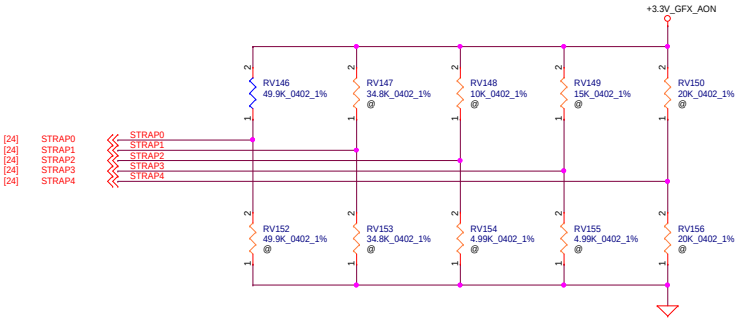

4Gb G5	Vendor PN	Die Revision	Strap
Hynix	H5GC4H24AJR-**R0C**	A-die	0x6
Micron	EDW4032BABG-**70**-F	A-die	0x4
8Gb G5	**Vendor PN**	**Die Revision**	**Strap**
Samsung	K4G80325FB-HC**28**	B-die	0x8
Micron	MT51J256M32HF-**70**:A	A-die	0x9

Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1 STRAP2 STRAP3 STRAP4	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			

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Title: N16P_MISC		
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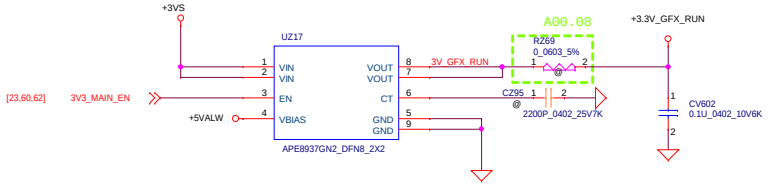
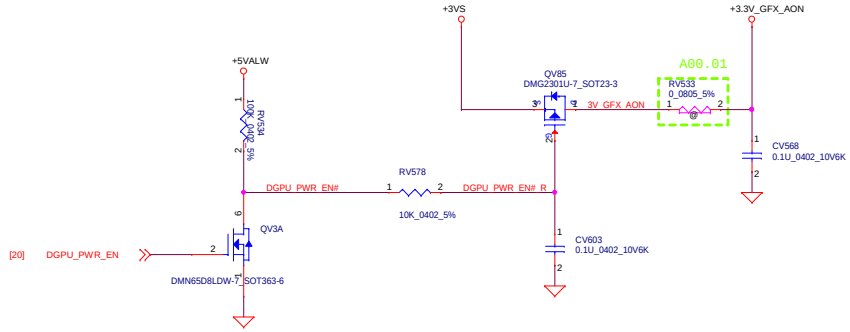
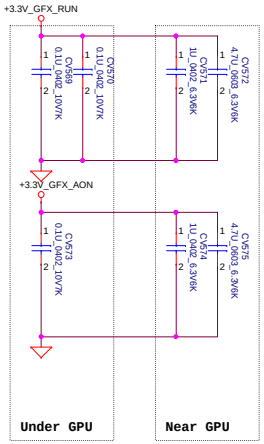
+3.3V_GFX_RUN

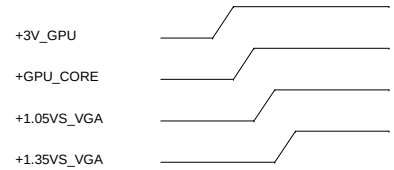


+3VALW to +3.3V_GFX_AON



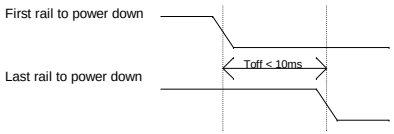


GPU Power Up Power Rail Sequence

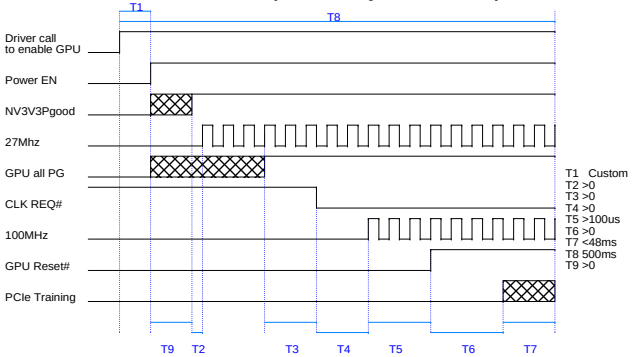


The ramp time for any rail must be more than 40us.

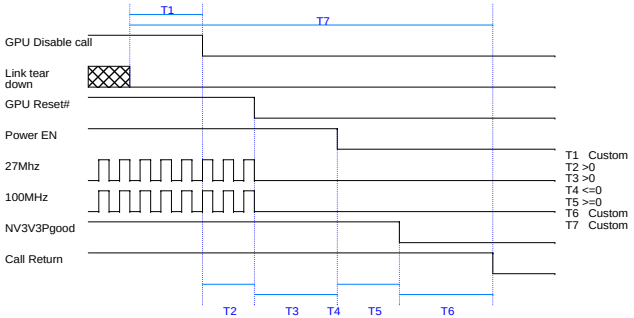
GPU Power Down Sequence



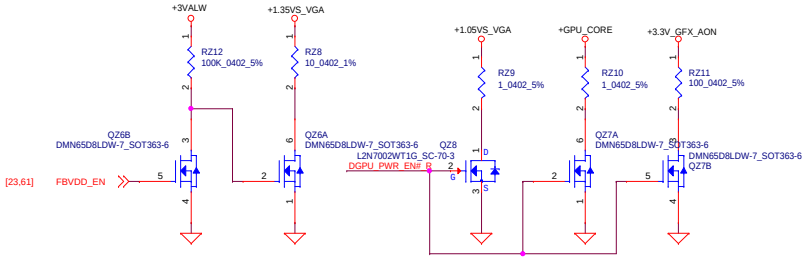
GPU Power Up Sub-system Sequence



GPU Power Down Sub-system Sequence



Discharge



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Title: **GPU DC/DC interface**

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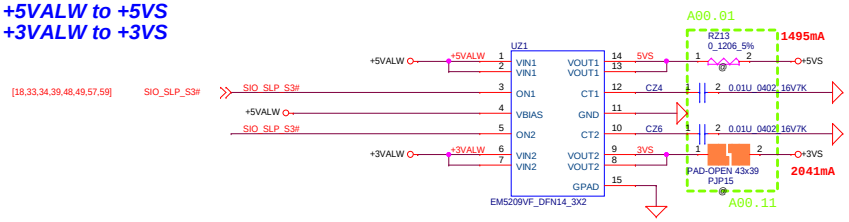
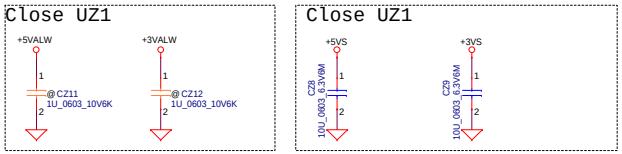
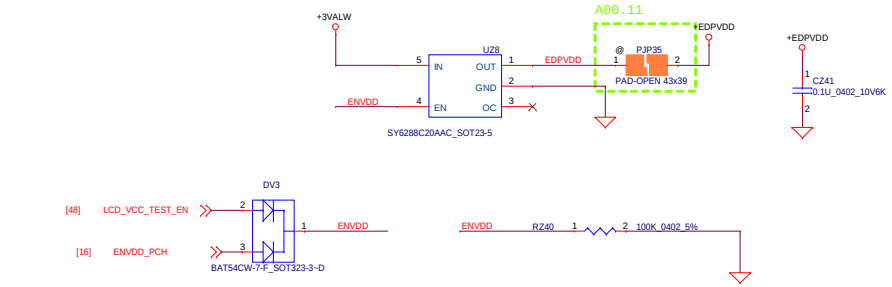
+5VALW to +5VS
+3VALW to +3VS

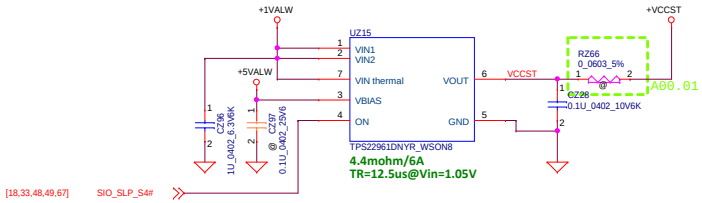




eDP & Camera Load Switch



+VCCST Load Switch



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Compal Electronics, Inc.

Title: **SYS DC/DC Interface**

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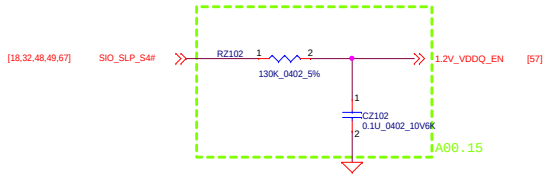
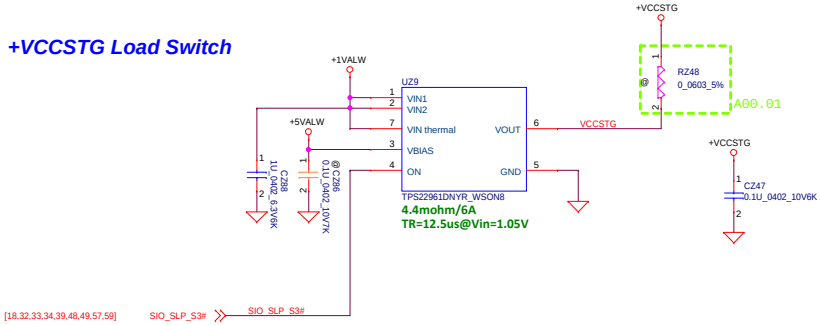
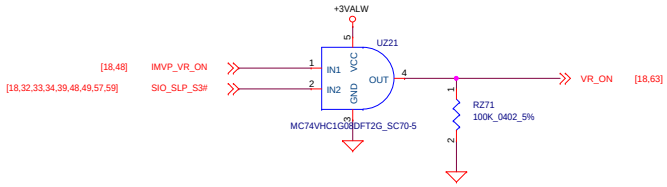
+1.2V_DDR Enable

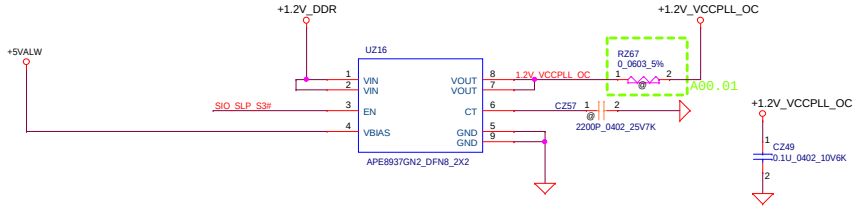


+VCCSTG Load Switch





+VCCPLL_OC Load Switch



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Compal Electronics, Inc.

Title: **EC ENE-KB9012/ KC3810**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

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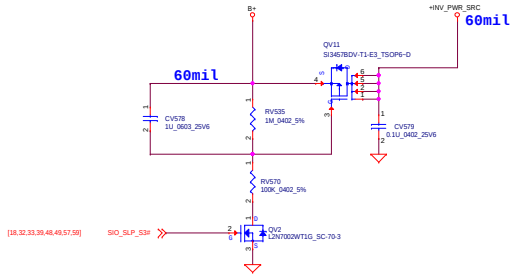
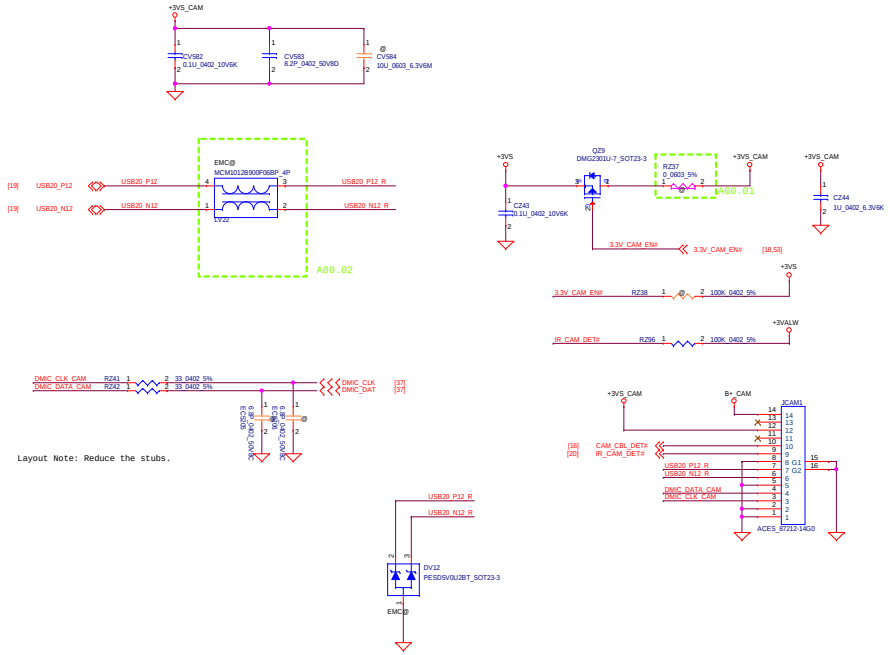
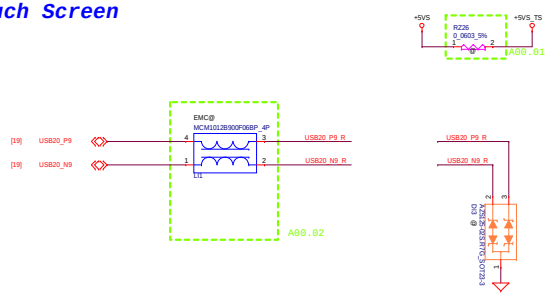
LCD backlight PWR CTRL



CCD +DMIC Conn.

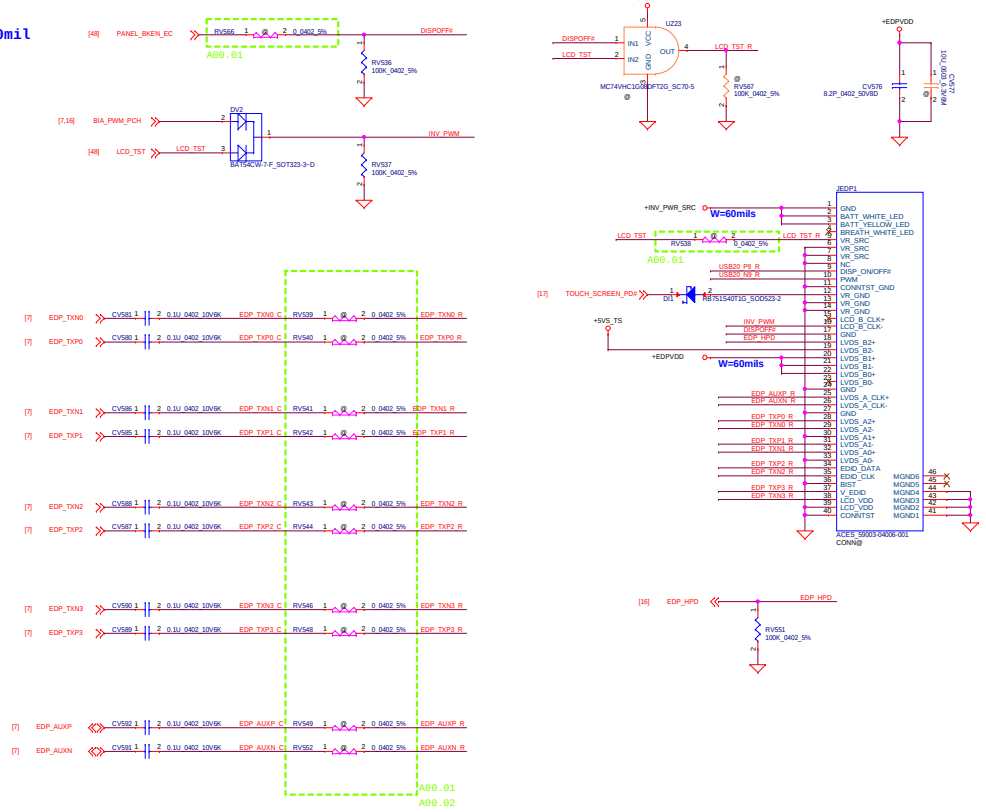


Touch Screen



eDP & TS Conn.

60mil



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			Size: Document Number: LA-D991P Rev: 0.1(X00)
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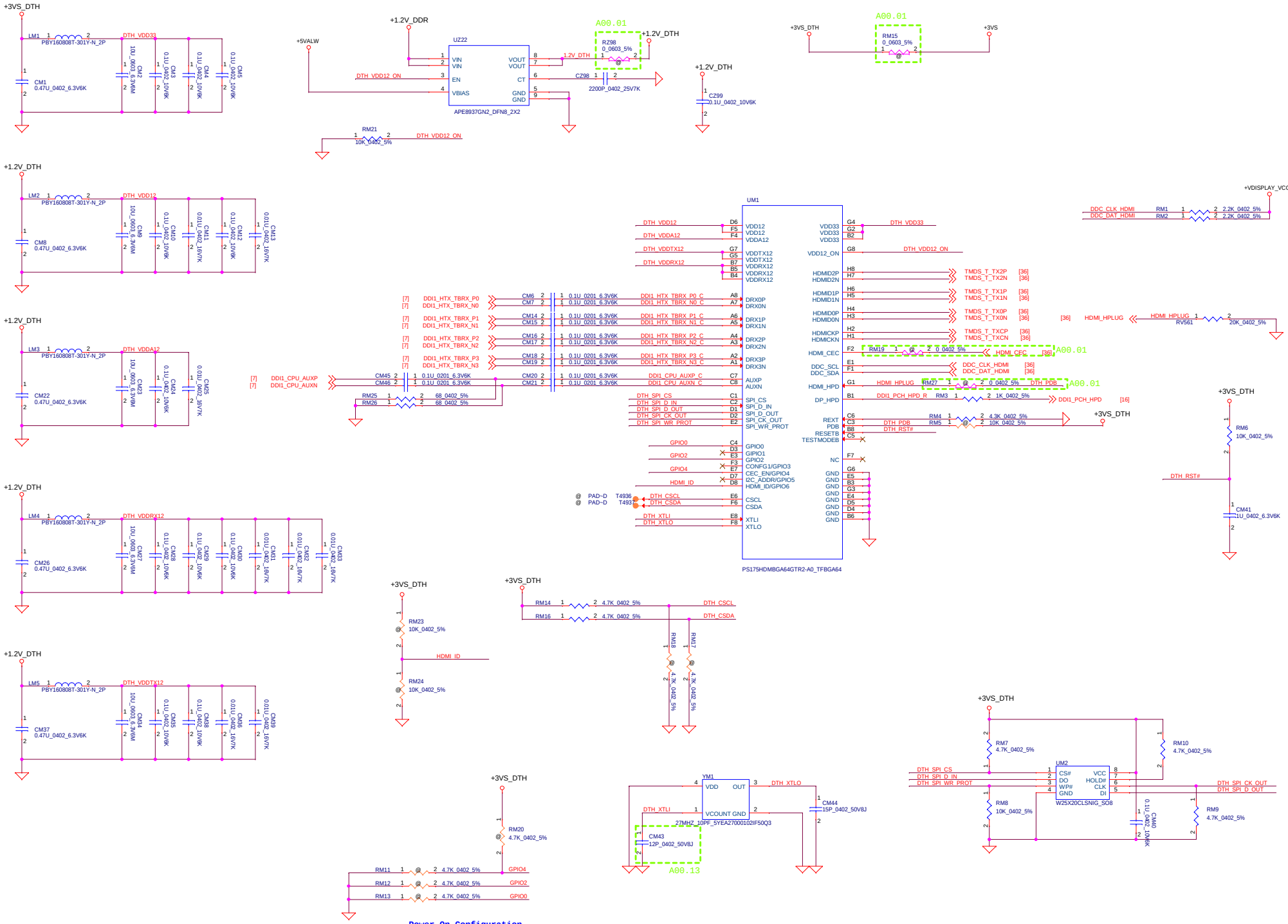

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Title: **DC/DC INTERFACE**

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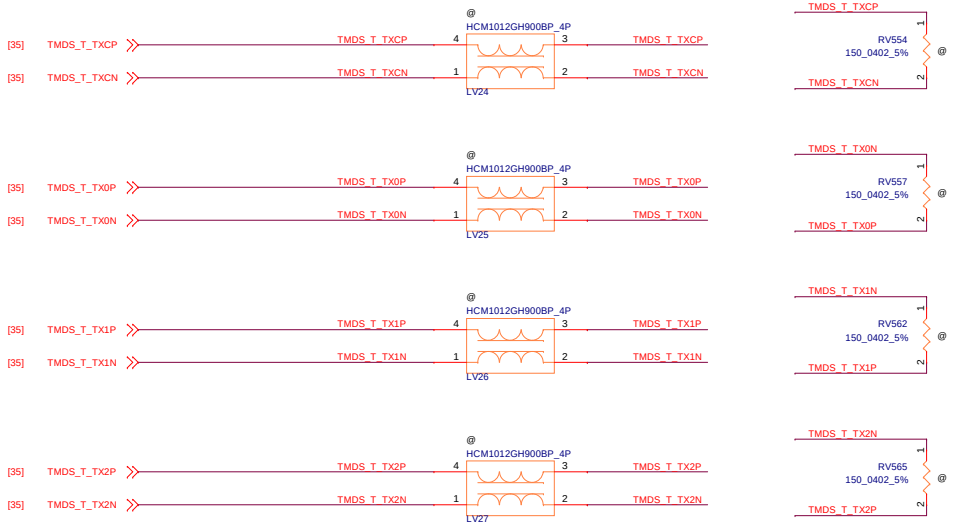
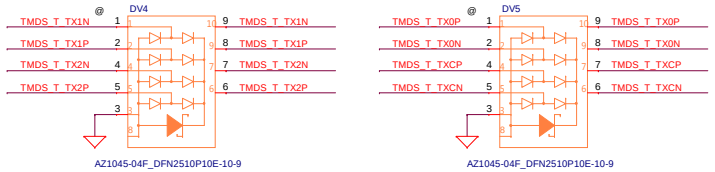
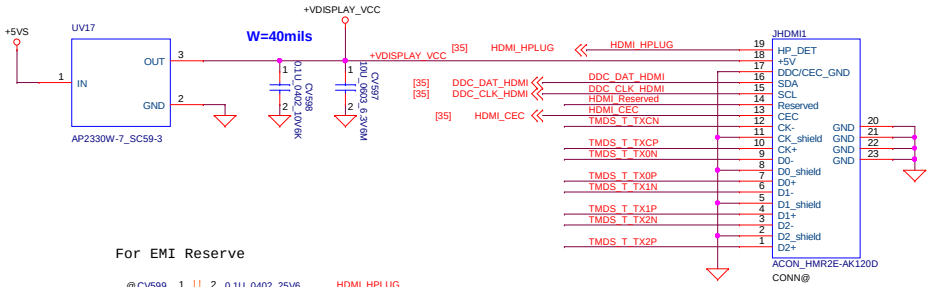
Place close to JHDMI1

Place between ESD and CM-Choke

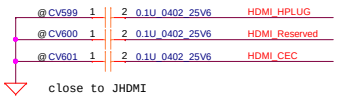




HDMI conn



For EMI Reserve



close to JHDMI

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Title: HDMI

Size	Document Number	Rev
Custom	LA-C361P	0.1(X00)

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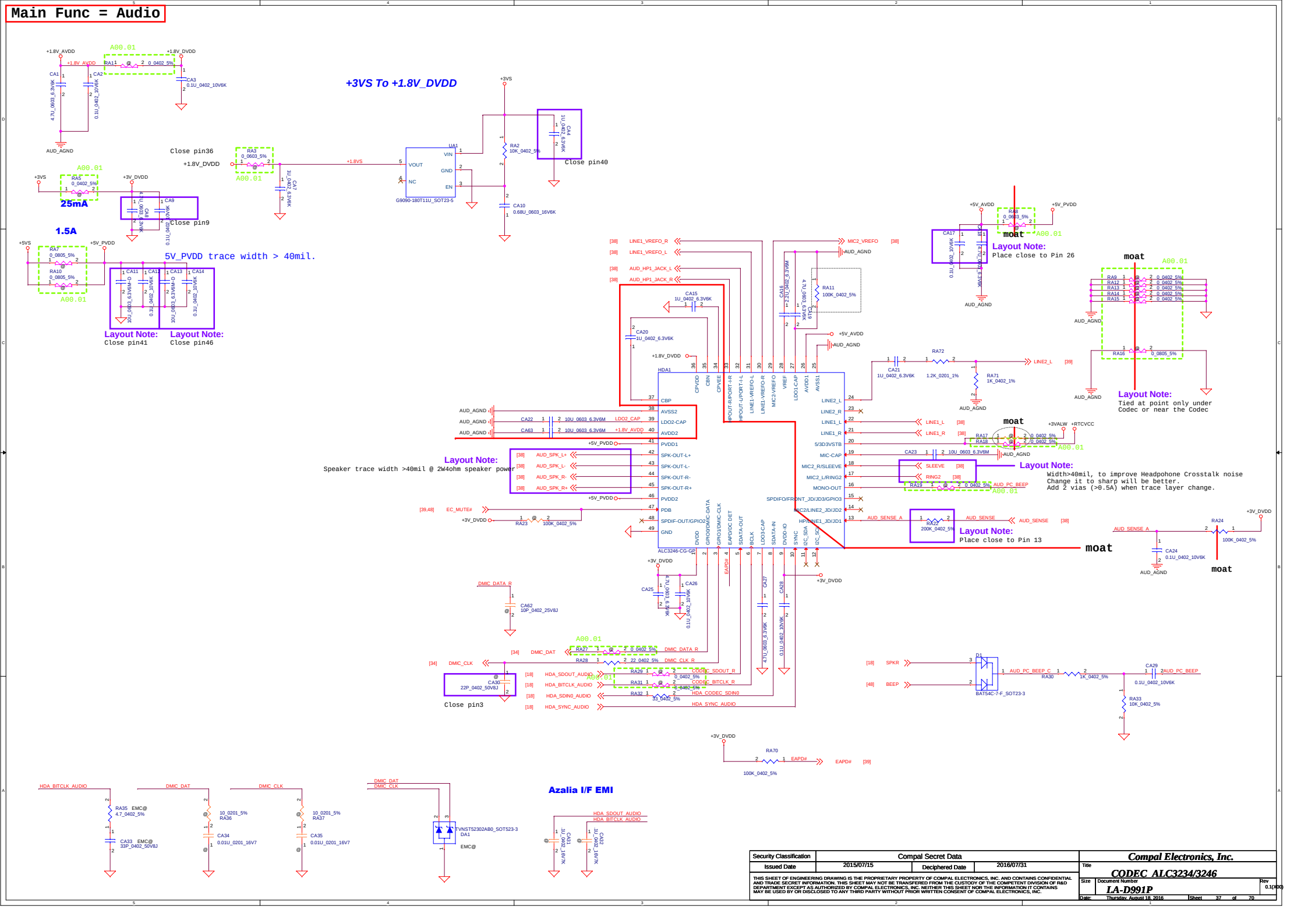
Main Func = Audio



Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

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Compal Electronics, Inc.

Title: **CODEC ALC3234/3246**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

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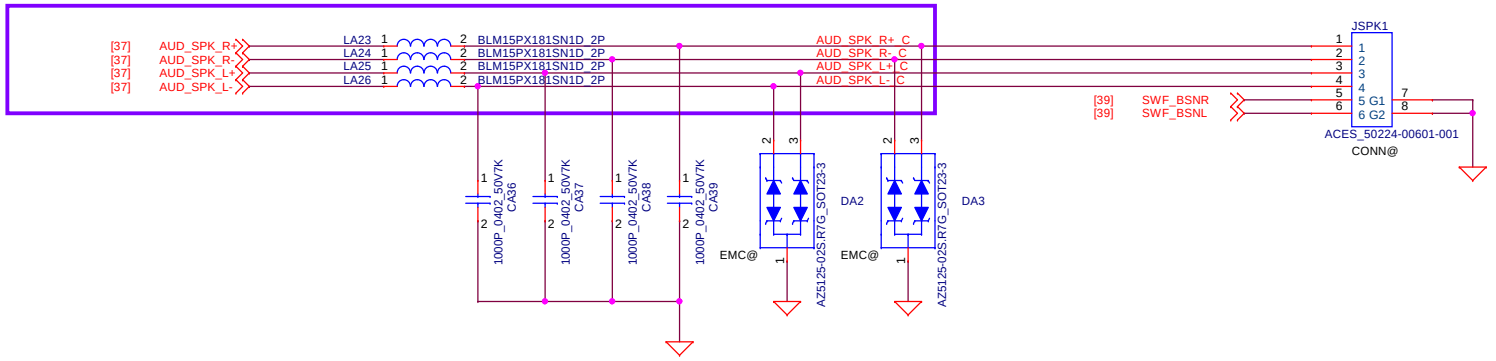
Main Func = Audio

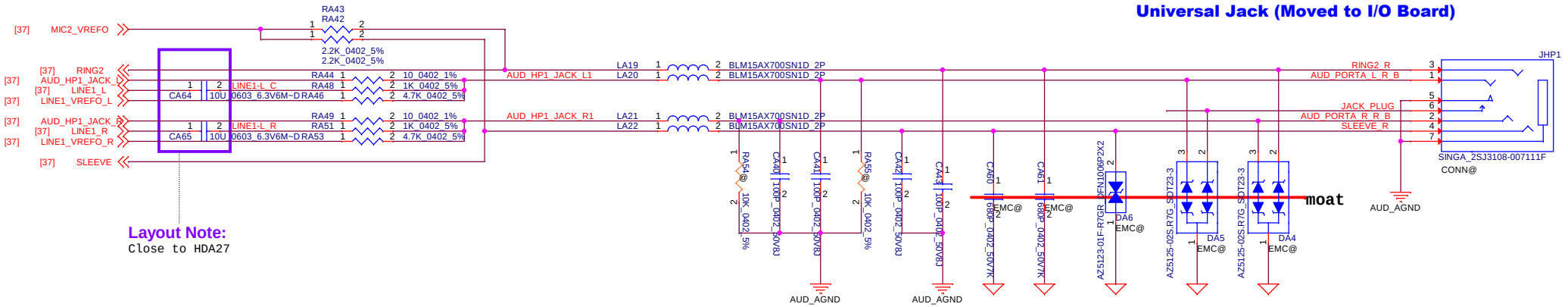
Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

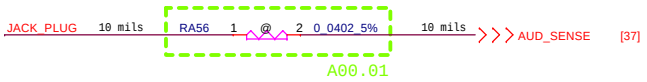


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-

Universal Jack (Moved to I/O Board)



Layout Note:
Close to HDA27



Security Classification	Compal Secret Data		
Issued Date	2015/07/15	Deciphered Date	2016/07/31

Compal Electronics, Inc.

Title: **SPKR/JACK**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

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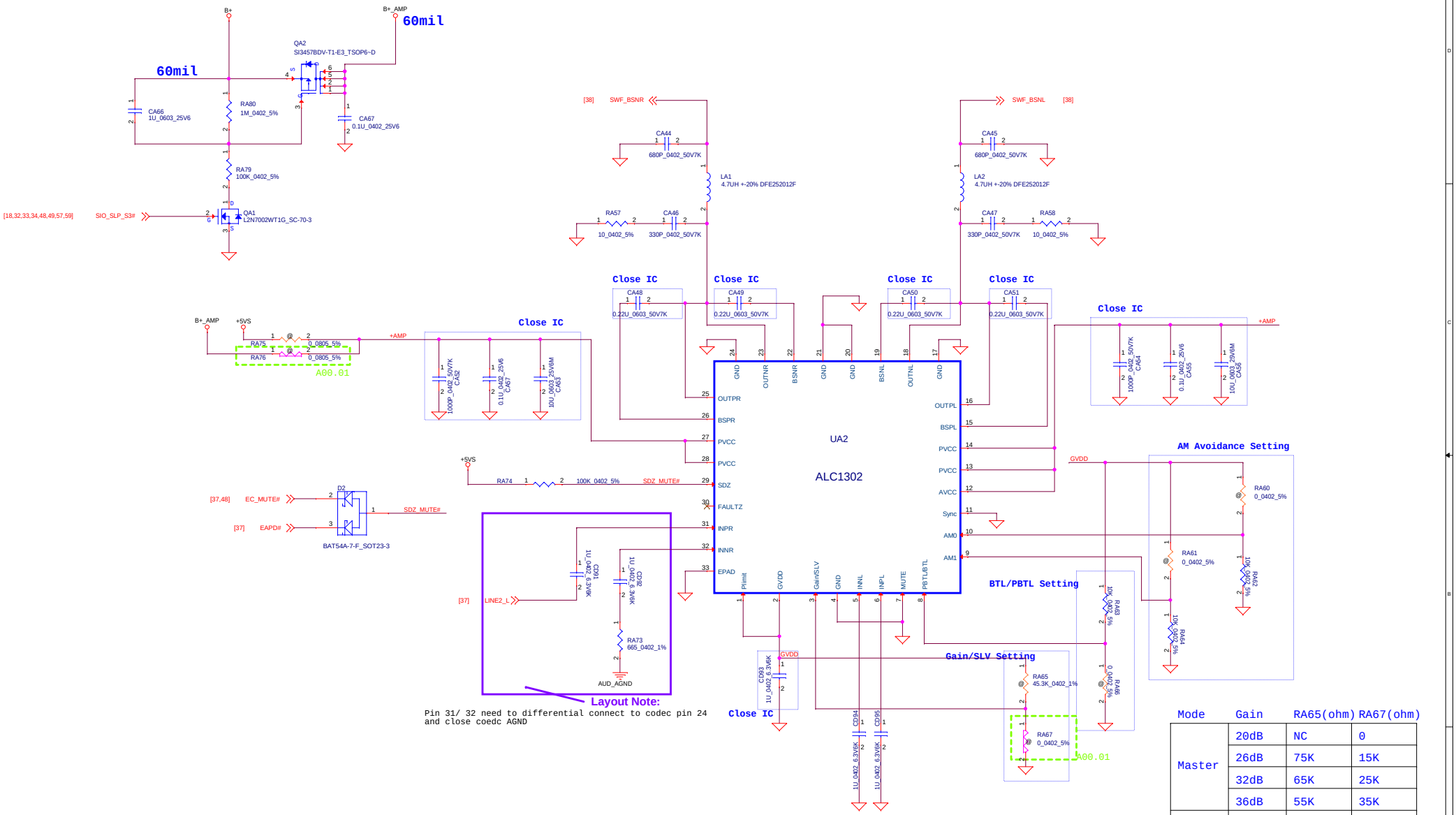
Subwoofer AMP



Mode	Gain	RA65(ohm)	RA67(ohm)
Master	20dB	NC	0
	26dB	75K	15K
	32dB	65K	25K
	36dB	55K	35K
Slave	20dB	45K	45K
	26dB	35K	55K
	32dB	25K	65K
	36dB	0	NC

Compal Electronics, Inc.	
Title	P3-SMART AMP
Size	Document Number: LA-D991P
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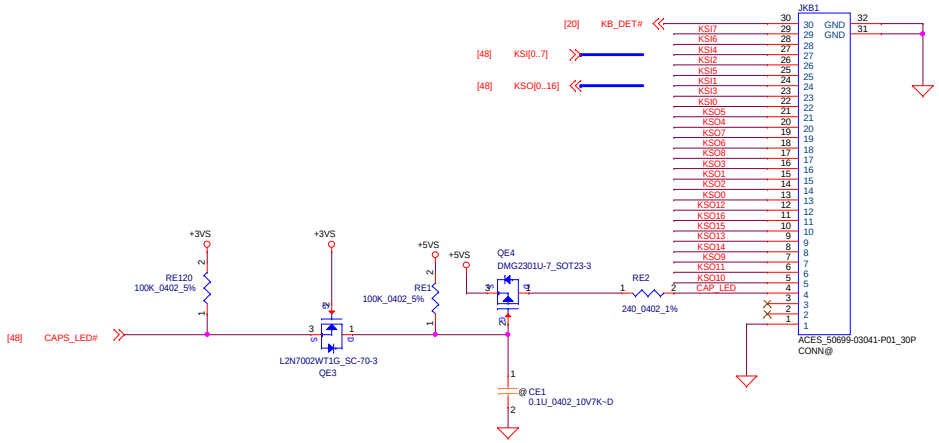
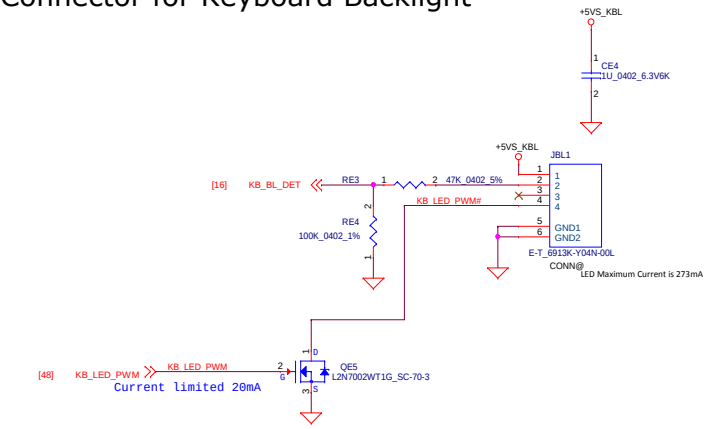
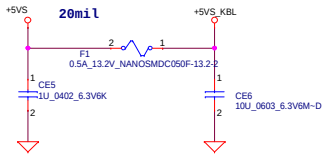
Connector for Keyboard



Connector for Keyboard Backlight



Fuse for Backlight



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: P03-KB Controller			
Size	Document Number: LA-D991P		Rev: 0.1(X00)
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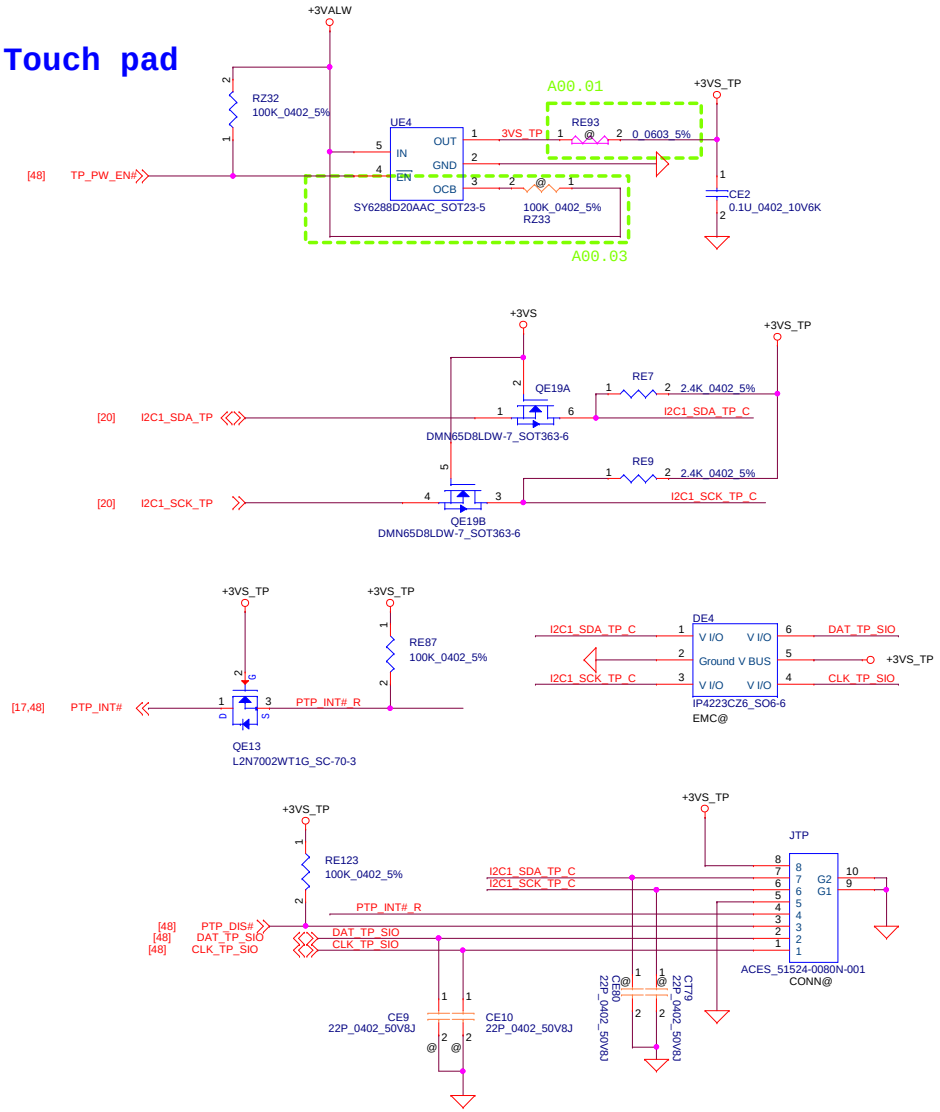
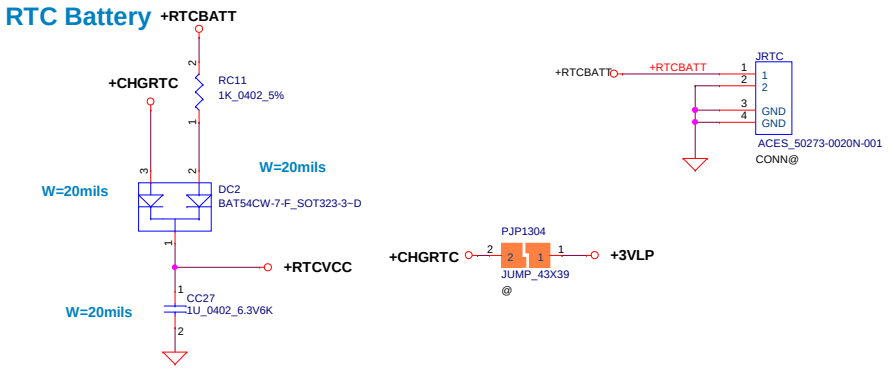
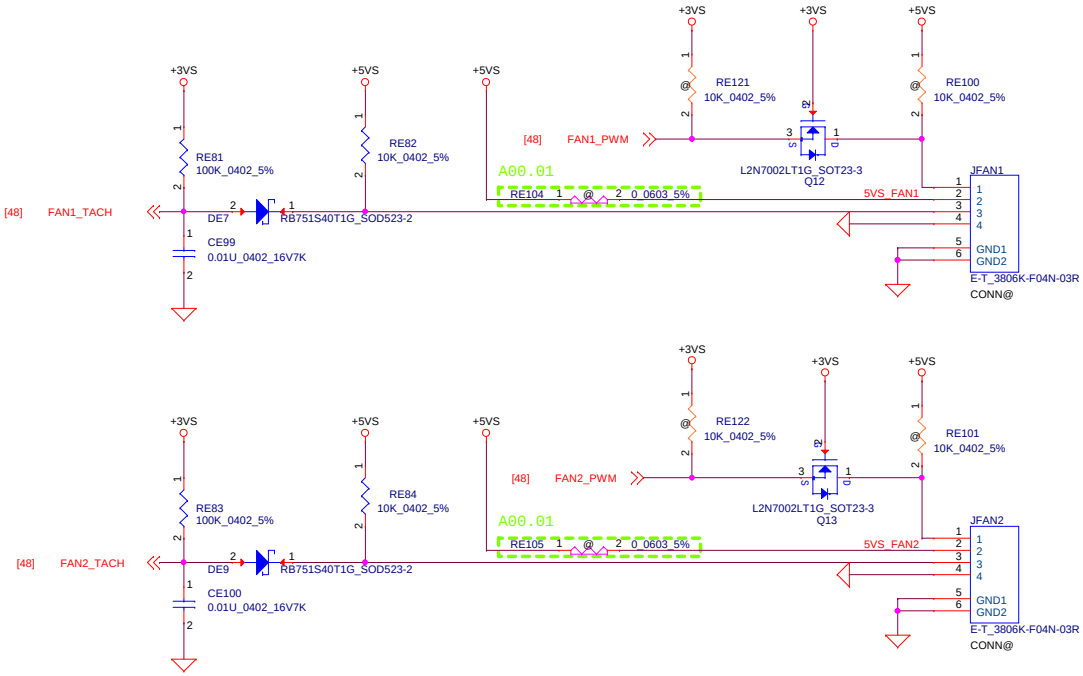
Touch pad



RTC Battery non- Charge Function



PWM FAN



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title	FAN/TP/KB/PWR SW		
Size	Document Number		Rev
Custom	LA-D991P		0.1(X00)
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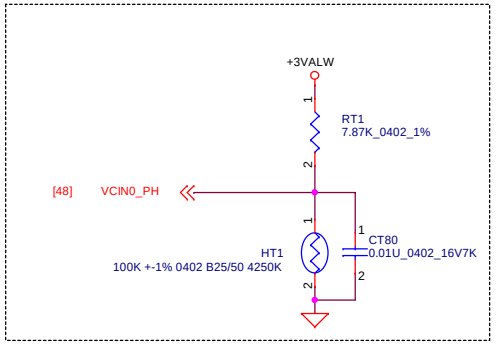
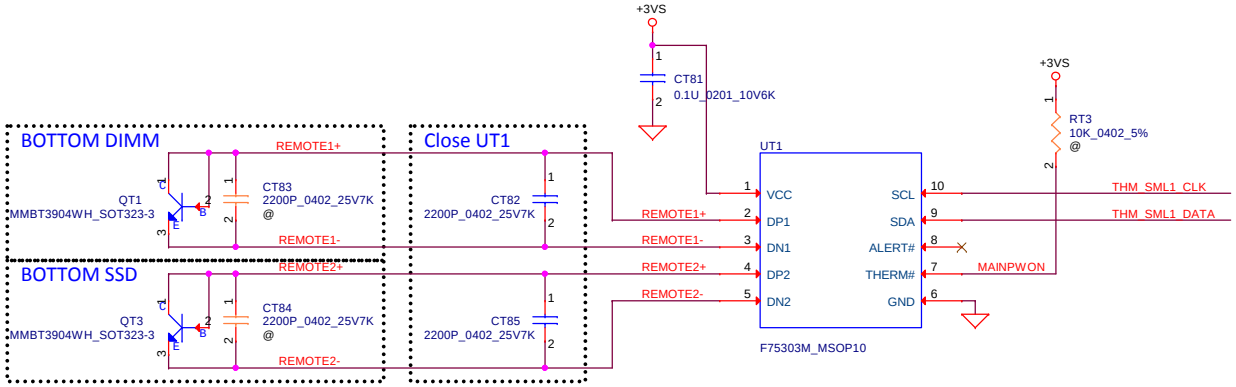
Main Func : Fan/Thermal

CPU TOP side



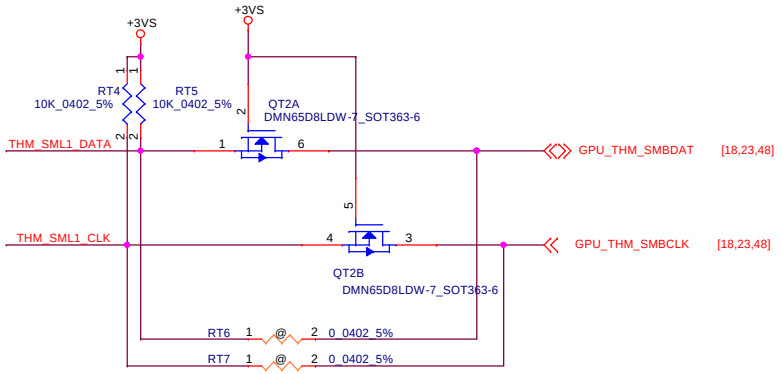
Fintek thermal sensor
placed TOP near between GPU & CPU



REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Address 1001_101xb

2nd source
SA000029210-->EMC1403-2-AIZL-TR



Compal Electronics, Inc.

Title: Thermal Sensor

Size | Document Number: LA-D991P | Rev: 0.1(0.00)

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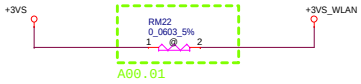
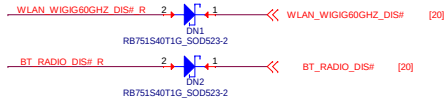
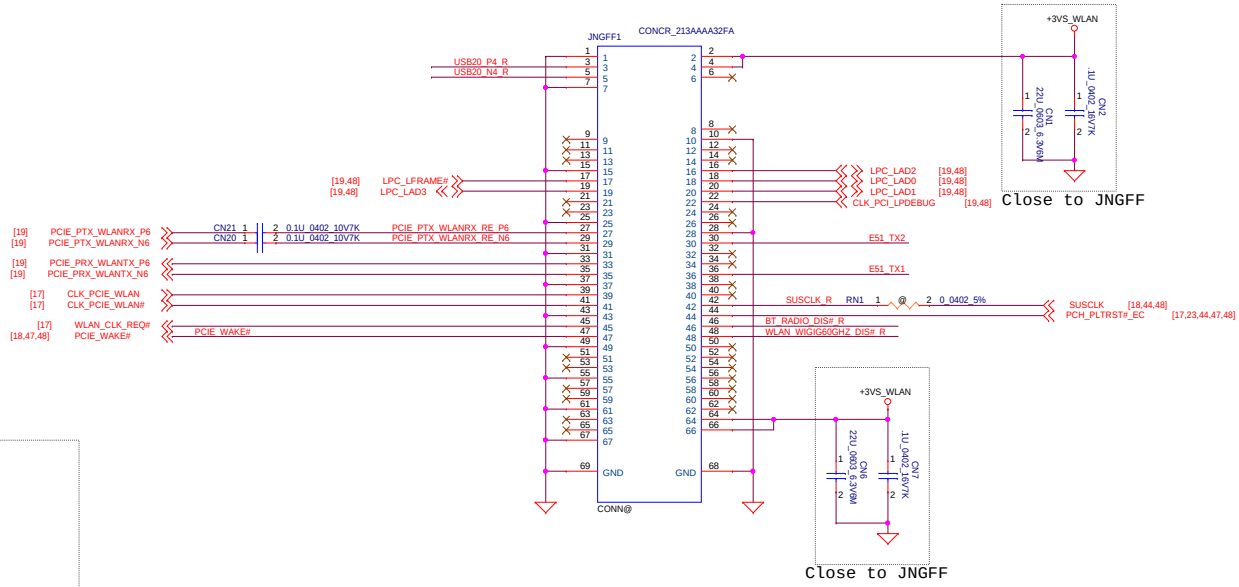
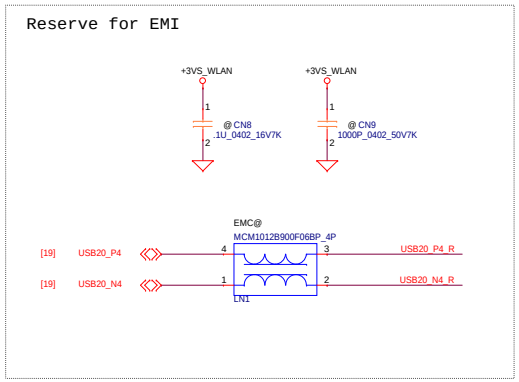
M.2 Slot-A Key-A (WLAN + BT)



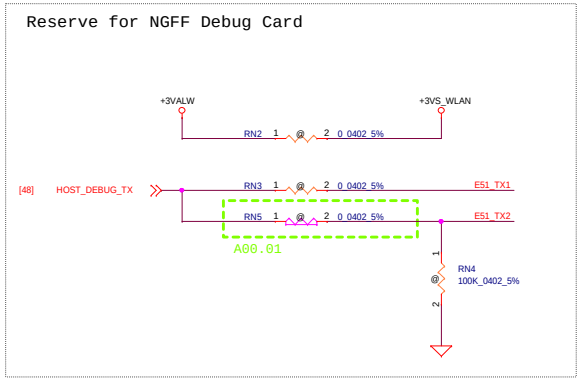




Reserve for EMI



Reserve for NGFF Debug Card



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: NGFF

Size	Document Number	Rev
C	LA-D991P	0.1(000)

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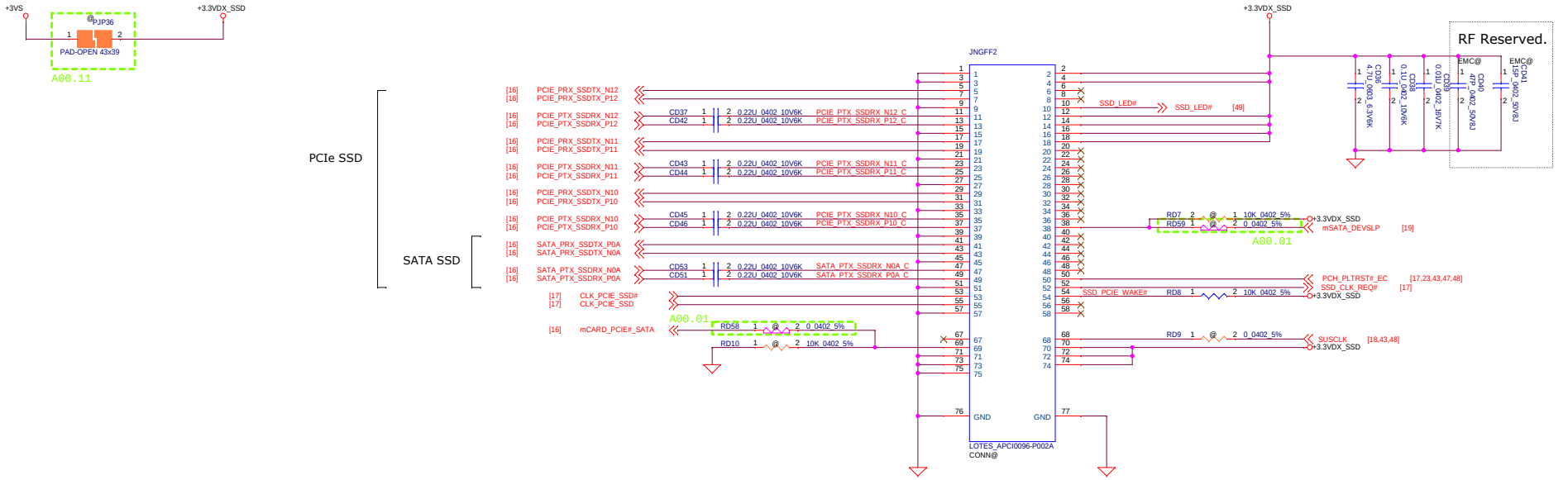
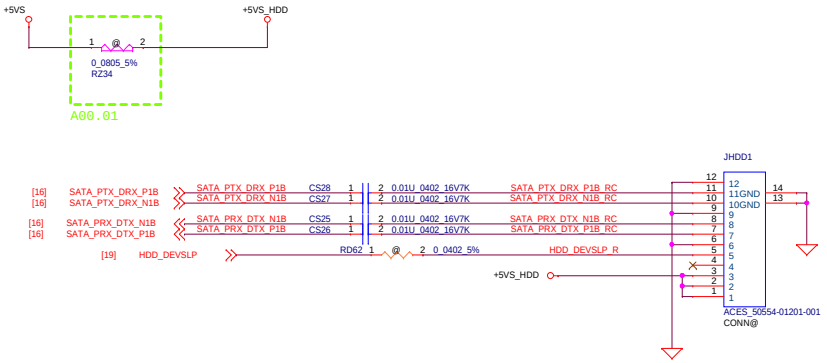
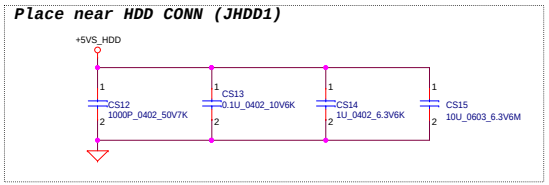
M.2 Slot-C Key-M (SSD)



HDD CONN





Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.			
Title: SSD			
Size: C	Document Number: LA-D991P		Rev: 0.1(000)
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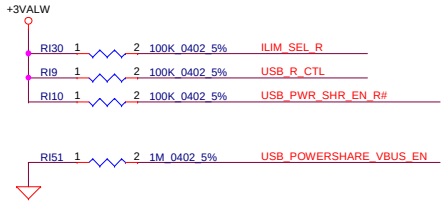
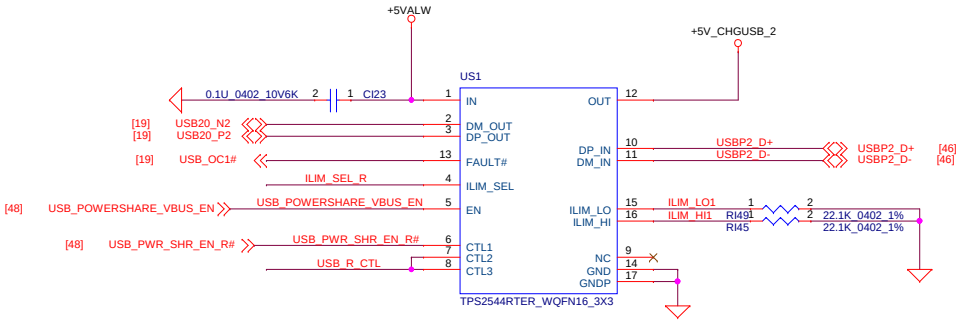
USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode
	CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting)
	ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI =2.2A)



USB3.0 / USB2.0 Port1



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Title	USB Powershare		
Size	Document Number		Rev
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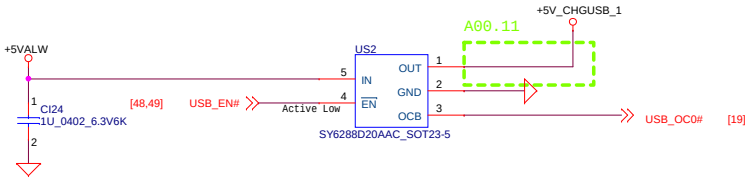
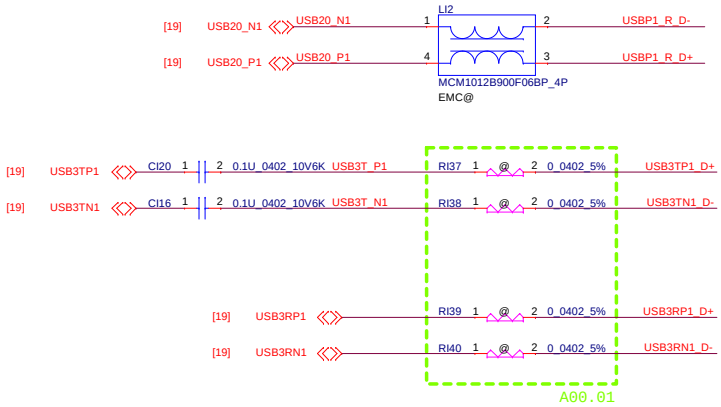
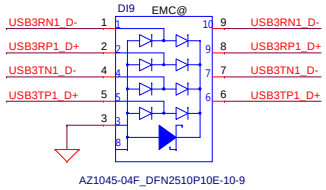
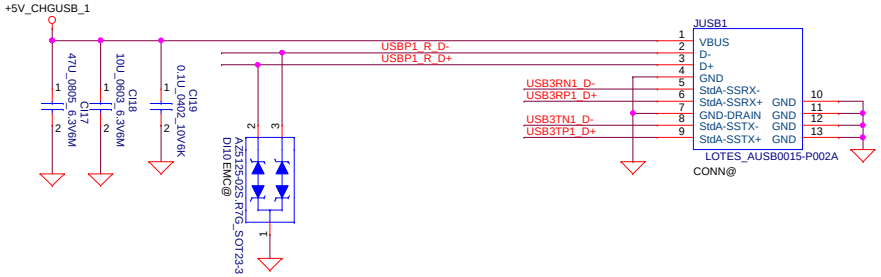


USB3.0 / USB2.0 Port1

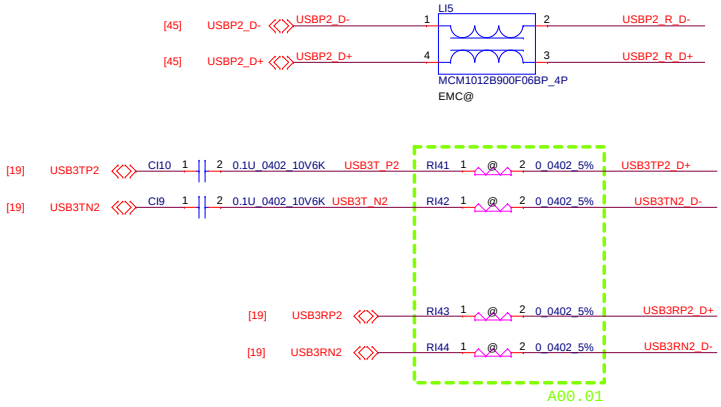


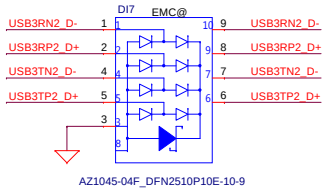


Place close to JUSB1

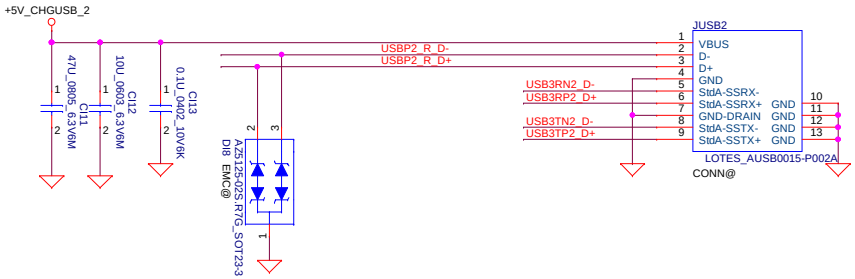


USB3.0 / USB2.0 Port2 (Power share)





Place close to JUSB2



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: USB conn.

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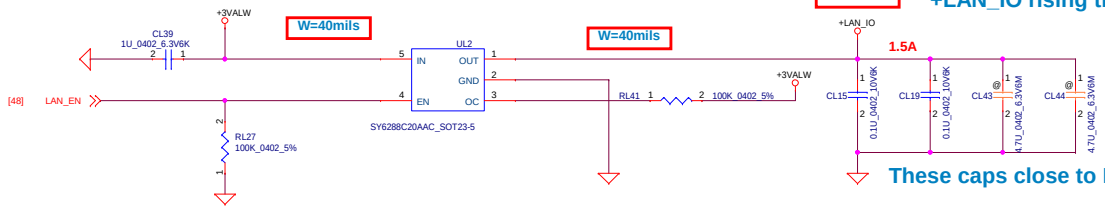
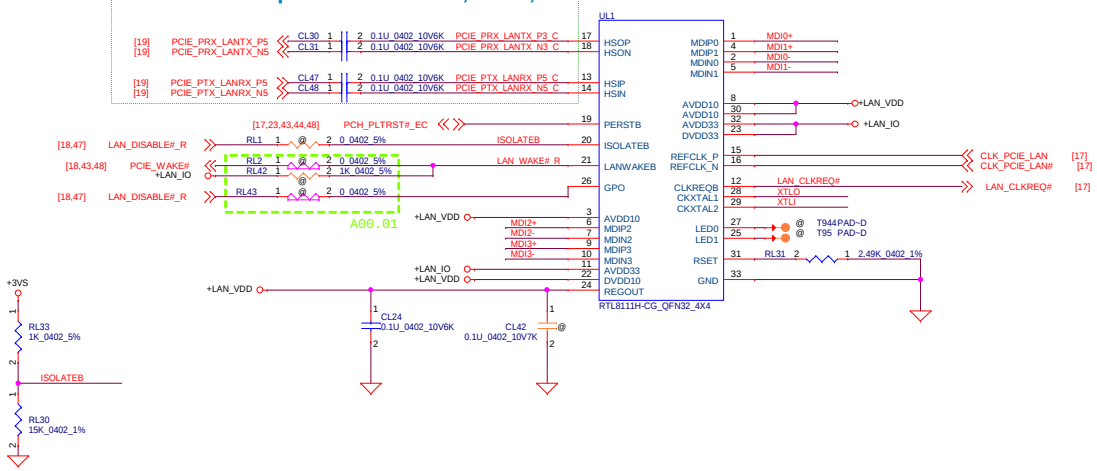
W=40mils

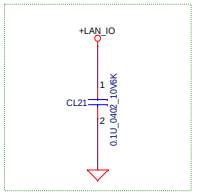
+LAN_IO rising time : >1ms and <100ms



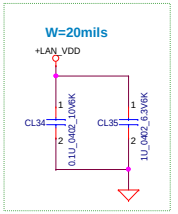
These caps close to Pin 11,32

These caps close to Pin 17,18/ 13,14

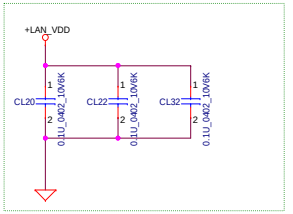




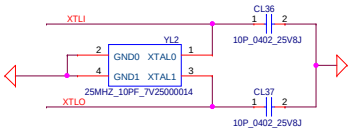
These caps close to Pin 23

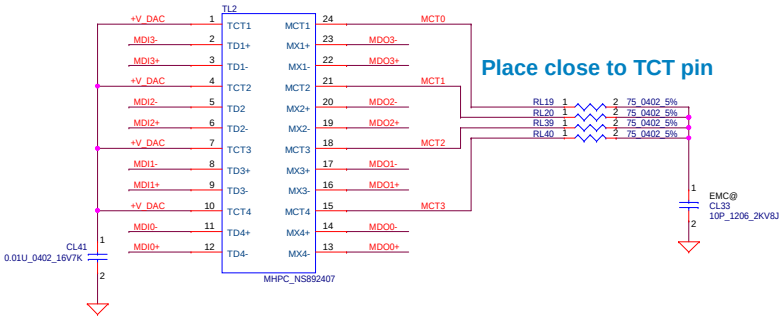


These caps close to Pin 22

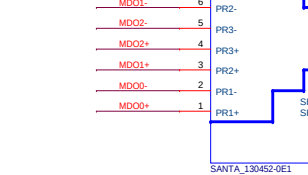


These caps close to Pin 3,8,30





Place close to TCT pin



Security Classification	Compal Secret Data		
Issued Date	2013/08/01	Deciphered Date	2014/07/31

Compal Electronics, Inc.

Title: LAN RTL8111GUS-CG

Size | Document Number: LA-D991P | Rev: 0.1(XXX)

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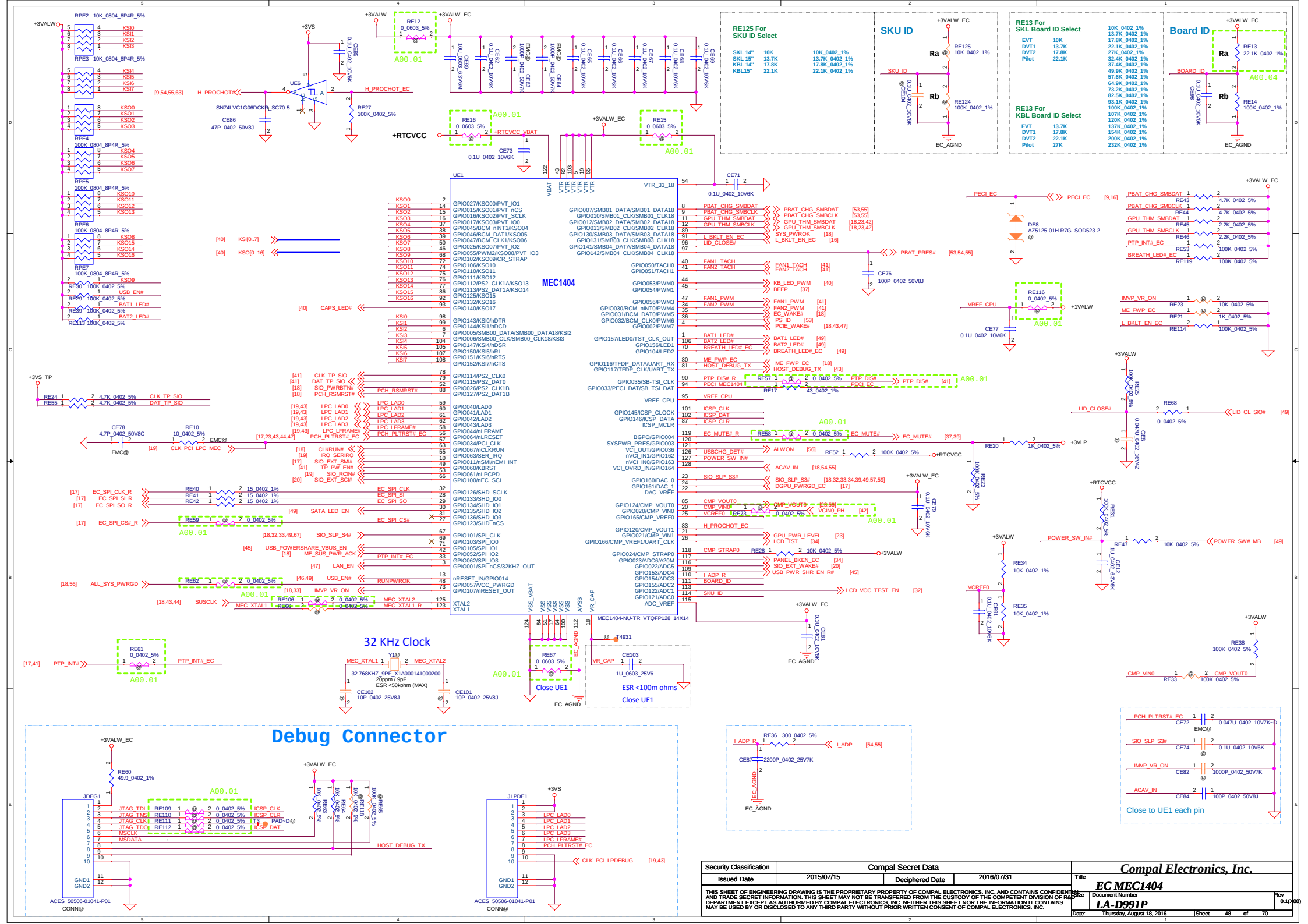
MEC1404
Debug Connector
32 KHz Clock
Close UE1
ESR <100m ohms
Close UE1
Close to UE1 each pin
RE125 For SKU ID Select
SKU ID
RE13 For SKL Board ID Select
RE13 For KBL Board ID Select
Board ID
Security Classification
Compal Secret Data
Issued Date
2015/07/15
Deciphered Date
2016/07/31
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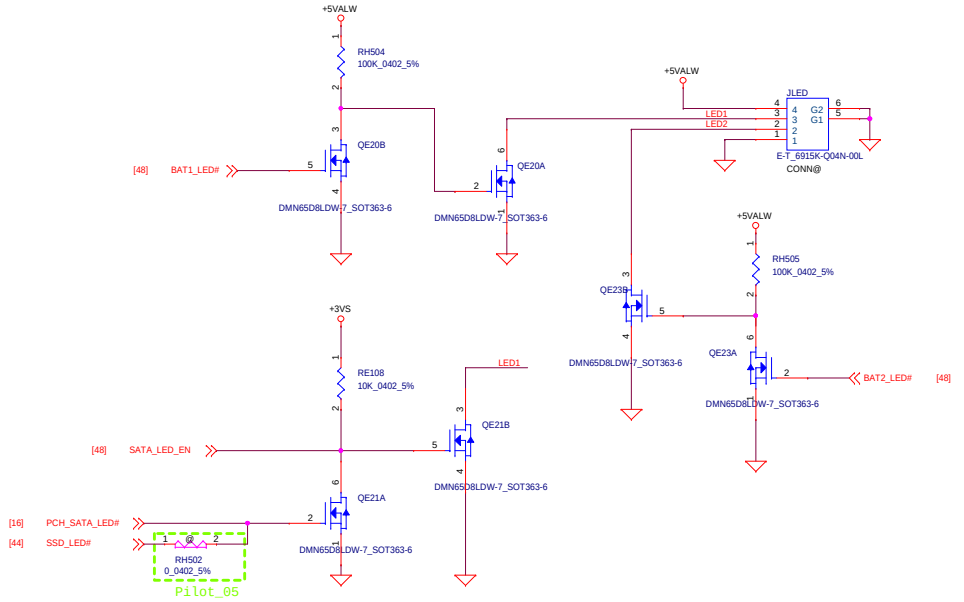
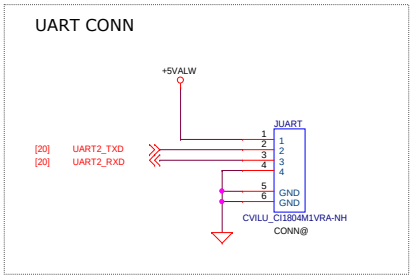
Compal Electronics, Inc.
Title
EC MEC1404
Size
Document Number
LA-D991P
Rev
0.1(X00)
Date:
Thursday, August 18, 2016
Sheet
48
of
70

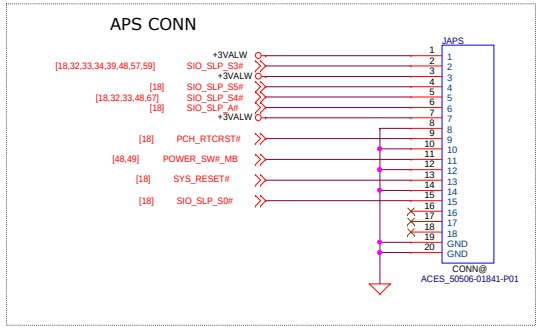
LED Board Connector

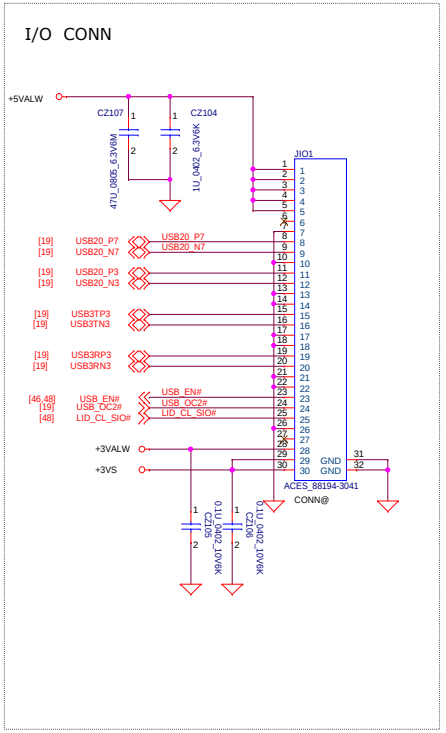
+5VALW - Trace width : 20mil



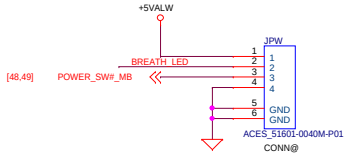
I/O & APS & UART CONN



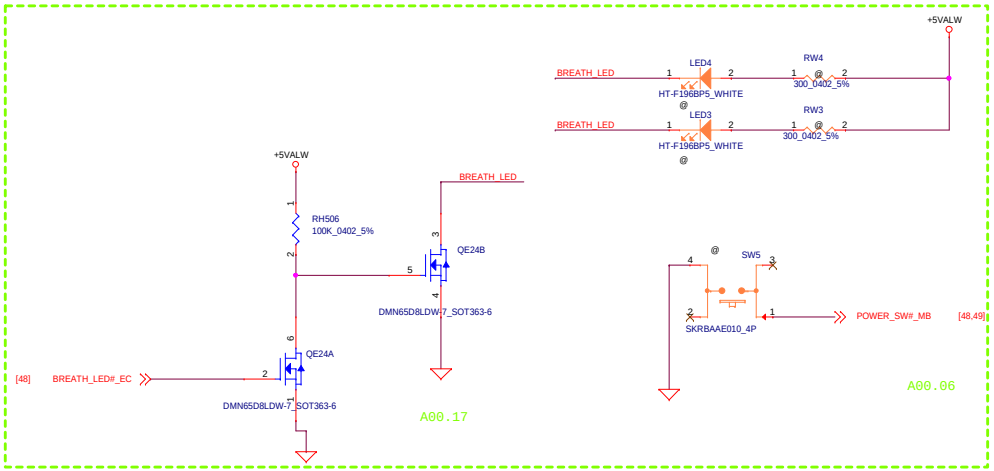




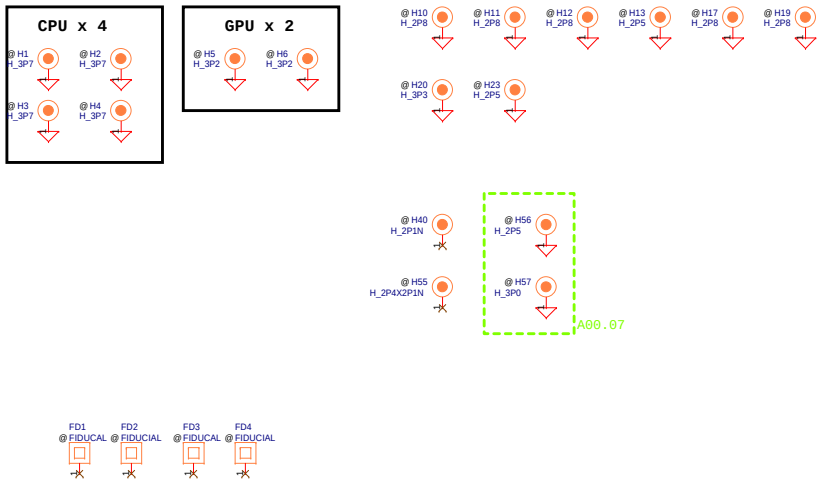
TO PWR BOARD



Power Button & LED (Reserve)



Screw Hole



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: TPM/BTB conn.

Size	Document Number	Rev
	LA-D991P	0.1(X00)

Date: Tuesday, November 01, 2016 Sheet 49 of 70

MODEL NAME : *BCV00/ BCV10*

PCB NO : *LA-D991P*

Bom Structure

PCB

ZZZ R1@

PCB 1QT LA-D991P REV0 M/B

CPU

UH1 CPUI5@

SKL-H_SR2FP

UH1 CPUI7@

SKL-H_SR2FQ

UH1 QSCPU@

SKL-H_QJMK

PCH

UH2 R1@

PCH-HM170

GPU

UV1 14GT@

N16P-GT-A2

UV1 15GX@

N16P-GX-A2

Micron 2G X7668431L02 : M2G@

RV160 M2G@ 24.9K_0402_1% SD034249280

UV6 EDW4032BABG-70-F-R_FBGA170P~D M2G@

UV7 EDW4032BABG-70-F-R_FBGA170P~D M2G@

UV8 EDW4032BABG-70-F-R_FBGA170P~D M2G@

UV9 EDW4032BABG-70-F-R_FBGA170P~D M2G@

Hynix 2G X7668431L01 : H2G@

RV160 H2G@ 34.8K_0402_1% SD034348280

UV6 H5GC4H24AJR-R0C_FBGA170P~D H2G@

UV7 H5GC4H24AJR-R0C_FBGA170P~D H2G@

UV8 H5GC4H24AJR-R0C_FBGA170P~D H2G@

UV9 H5GC4H24AJR-R0C_FBGA170P~D H2G@

Samsung 4G X7668431L03 : S4G@

RV157 S4G@ 4.99K_0402_1% SD034499180

UV6 K4G80325FB-HC28_FBGA170P~D S4G@

UV7 K4G80325FB-HC28_FBGA170P~D S4G@

UV8 K4G80325FB-HC28_FBGA170P~D S4G@

UV9 K4G80325FB-HC28_FBGA170P~D S4G@

Micron 4G X7668431L04 : M4G@

RV157 M4G@ 10K_0402_1% SD034100280

UV6 MT51J256M32HF-70:A_FBGA170P~D M4G@

UV7 MT51J256M32HF-70:A_FBGA170P~D M4G@

UV8 MT51J256M32HF-70:A_FBGA170P~D M4G@

UV9 MT51J256M32HF-70:A_FBGA170P~D M4G@

Security Classification	Compal Secret Data		
Issued Date	2013/04/10	Deciphered Date	2014/05/01

Compal Electronics, Inc.

Title: *NOTE*

Size | Document Number: *LA-D991P* | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 50 of 70

Version Change List (P. I. R. List)

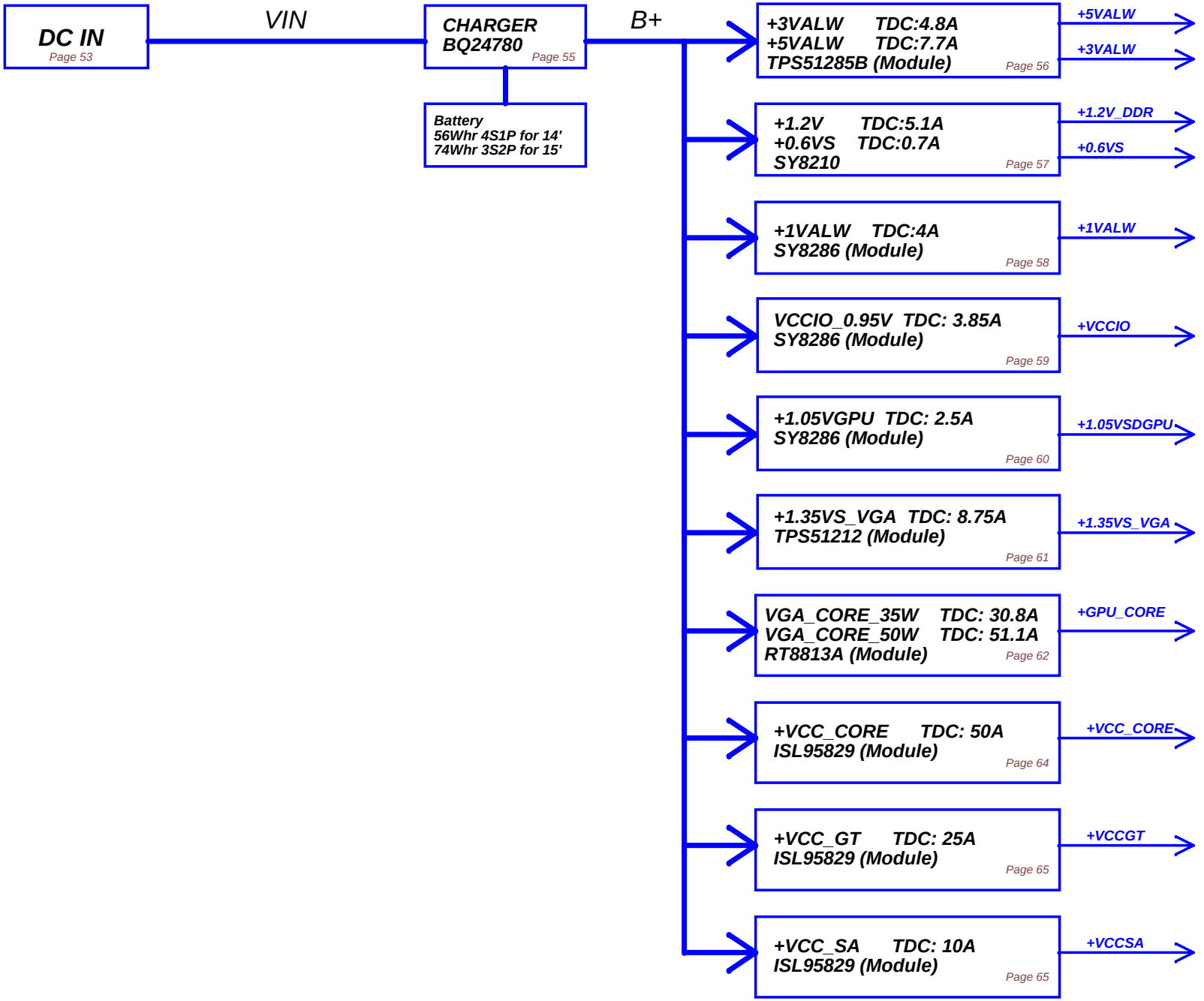
Security Classification	Compal Secret Data		
Issued Date	2013/04/10	Deciphered Date	2014/05/01

Compal Electronics, Inc.

Title: **NOTE**

Size | Document Number: **LA-D991P** | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 51 of 70



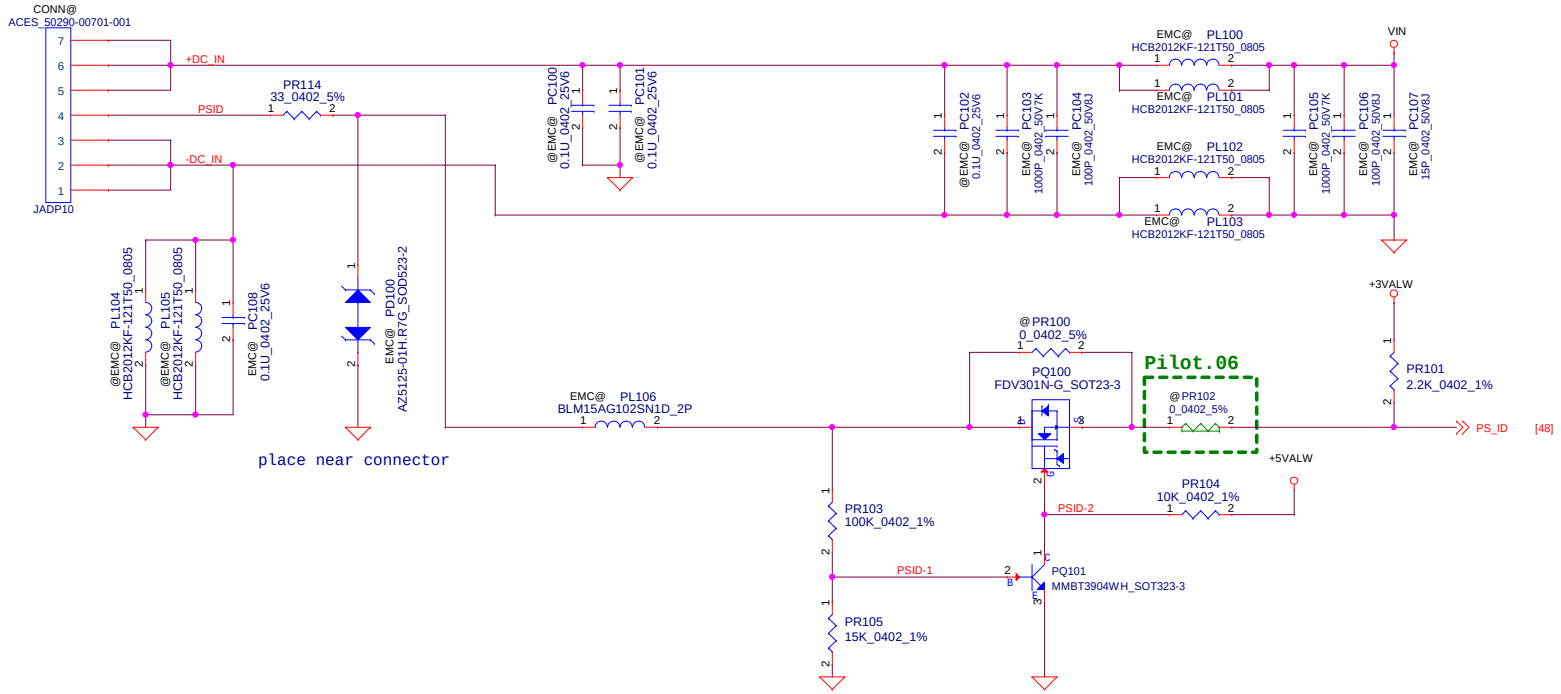
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

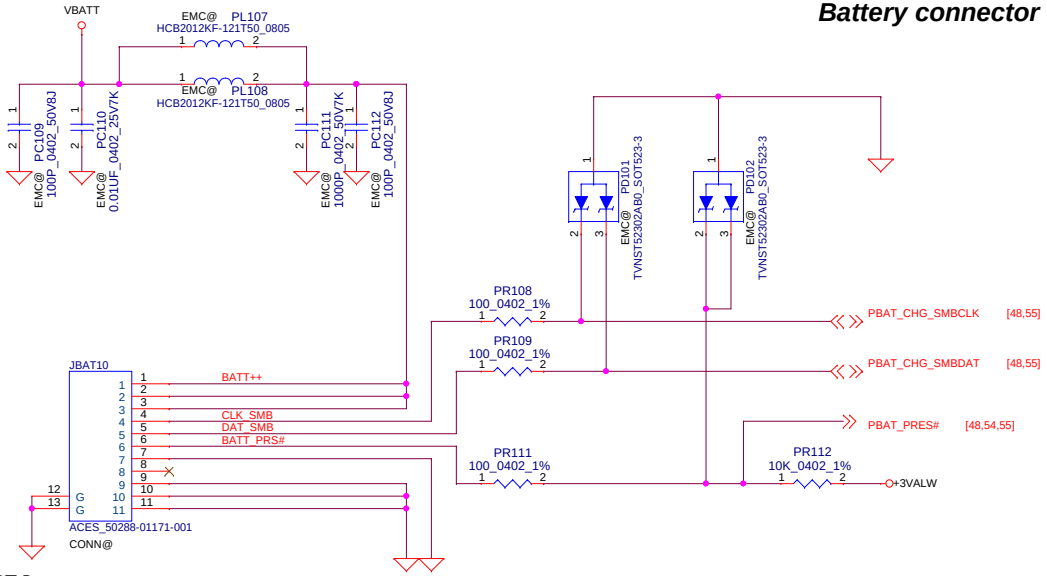
Title: **Power Block Diagram**

Size	Document Number	Rev
		0.1(X00)

Date: Thursday, August 18, 2016 Sheet 52 of 70



Battery connector



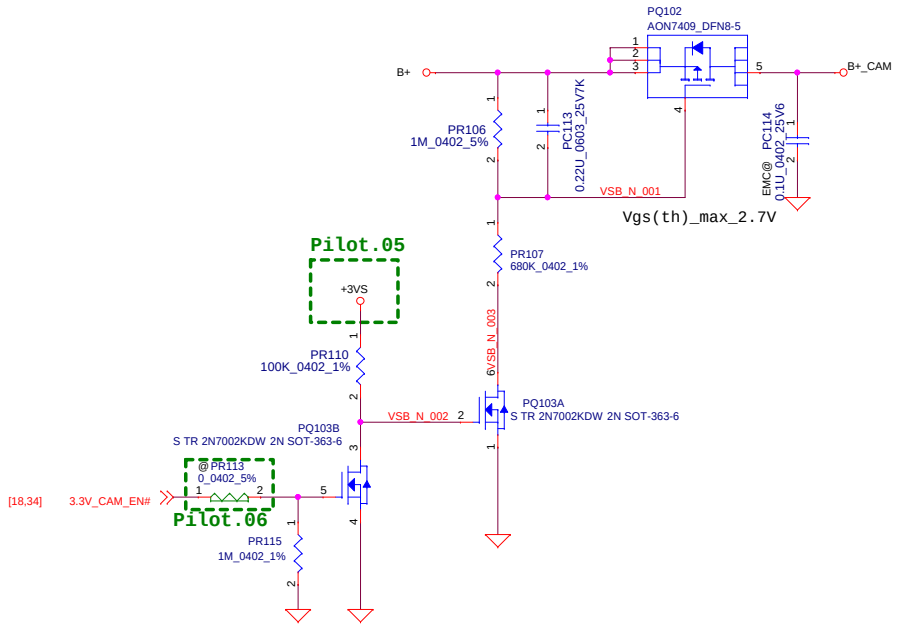
SMART Battery:
01.BAT1+
02.BAT2+
03.BAT3+
04.CLK_SMB
05.DAT_SMB
06.BATT_PRS
07.SYS_PRS
08.Battery Voltage
09.GND1
10.GND2
11.GND3

Battery
56Whr 4S1P for 14'
74Whr 3S2P for 15'

Smart Adapter circuit (39.1)

For Camera LS

Rds= 12.8mo(typ) 17(max)mo
.1.885mW@3W backlight



Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

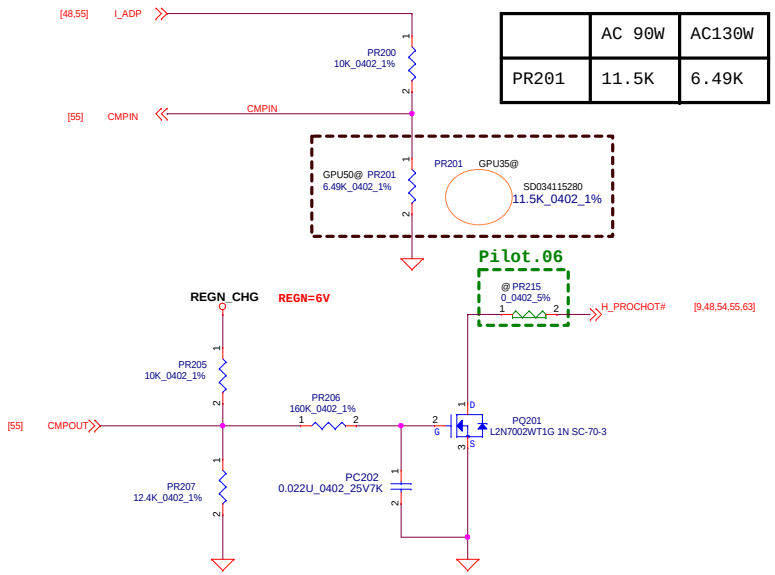
Compal Electronics, Inc.

Title: ***PWR_DCIN / BATT CONN***

Size | Document Number | Rev 0.1(X00)

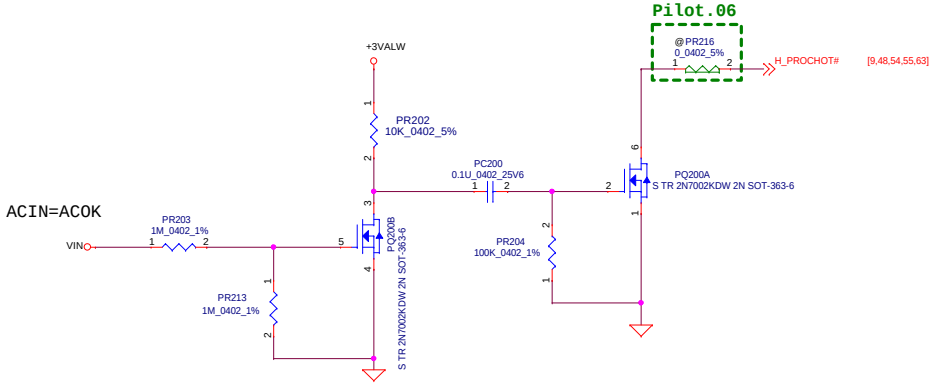
Date: Thursday, August 18, 2016 | Sheet 53 of 70

When CMPIN> Vref(2.3V/1.3V)
CMPOUT=floating

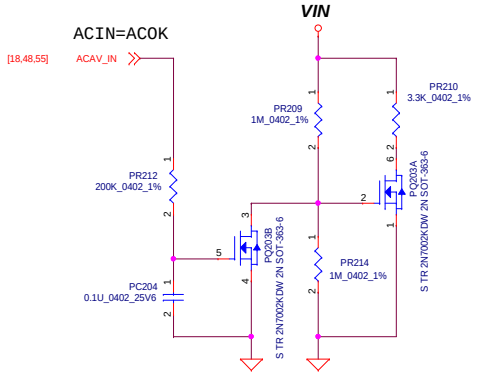


	AC 90W	AC130W
PR201	11.5K	6.49K

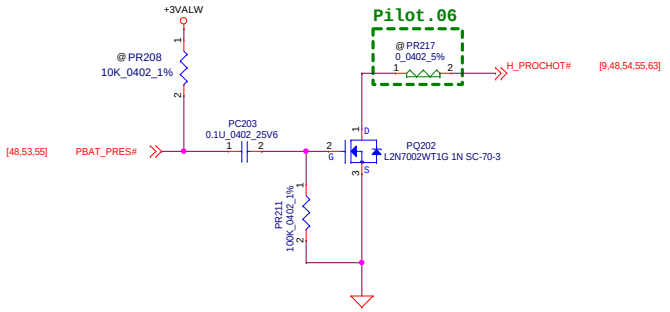
ENG0012879 Circuit-1
Delay Adapter OC H_PROCHOT# 2ms while Hybrid power transition



Ref ENG0012879 Circuit-2
HW Asserts H_PROCHOT# when ac adapter is being unplugged and keep low for 10ms until SW prochot# is issuded by EC



Erp lot 6 circuit



Ref ENG0012879 Circuit-4
HW Asserts H_PROCHOT# when battery is being unplugged and keep low for 10ms until SW prochot# is issuded by EC

Rest of support elements (37.1)

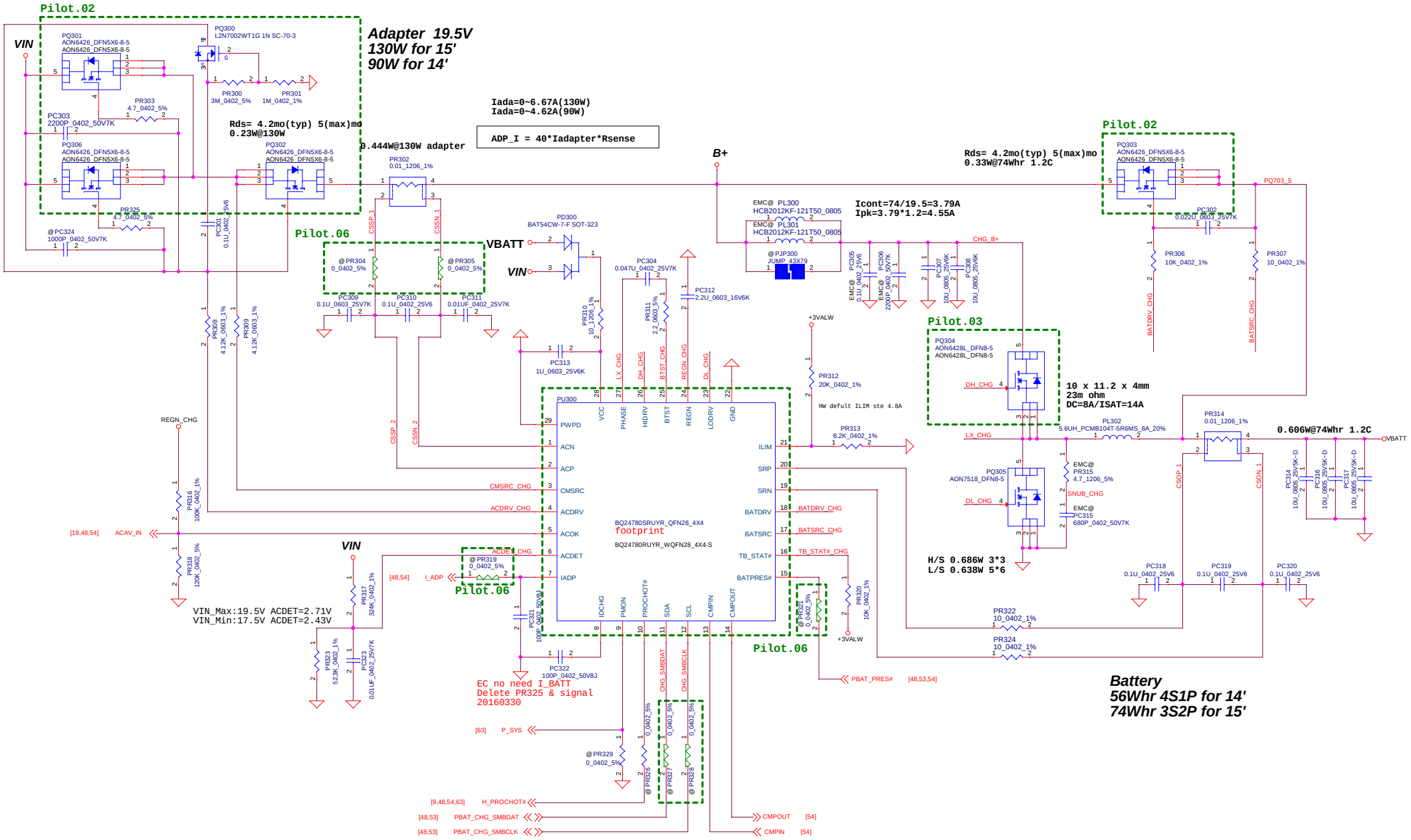
Security Classification	Compal Secret Data		
Issued Date	2011/08/25	Deciphered Date	2012/07/25

Compal Electronics, Inc.

Title: **PWR_PROCHOT#**

Size	Document Number	Rev
		0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 54 of 70



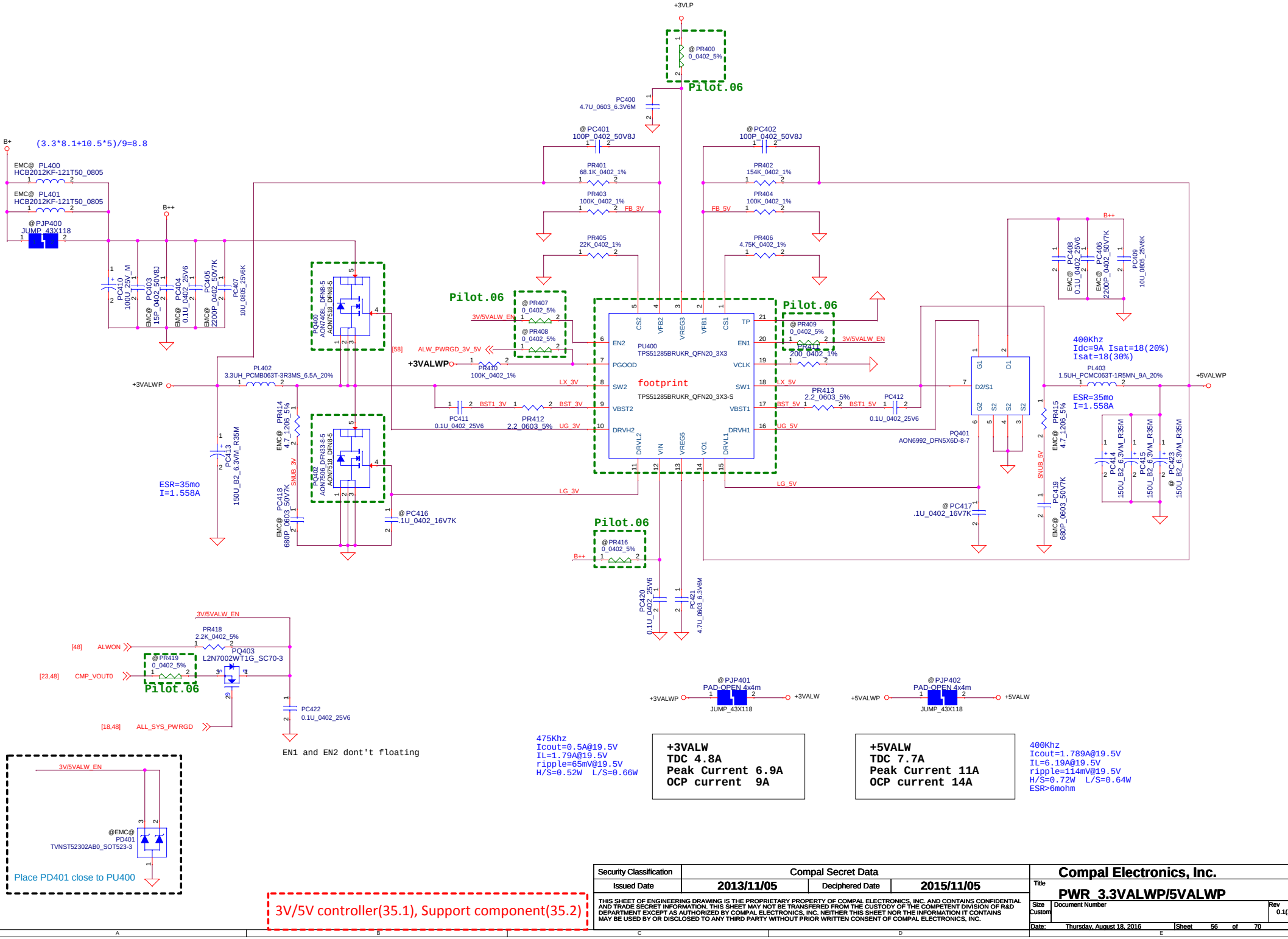
Security Classification	Compal Secret Data		
Issued Date	2013/11/05	Deciphered Date	2015/11/05

Compal Electronics, Inc.

Title: PWR_CHARGER(BQ24780S)

Size	Document Number	Rev
Custom		0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 55 of 70



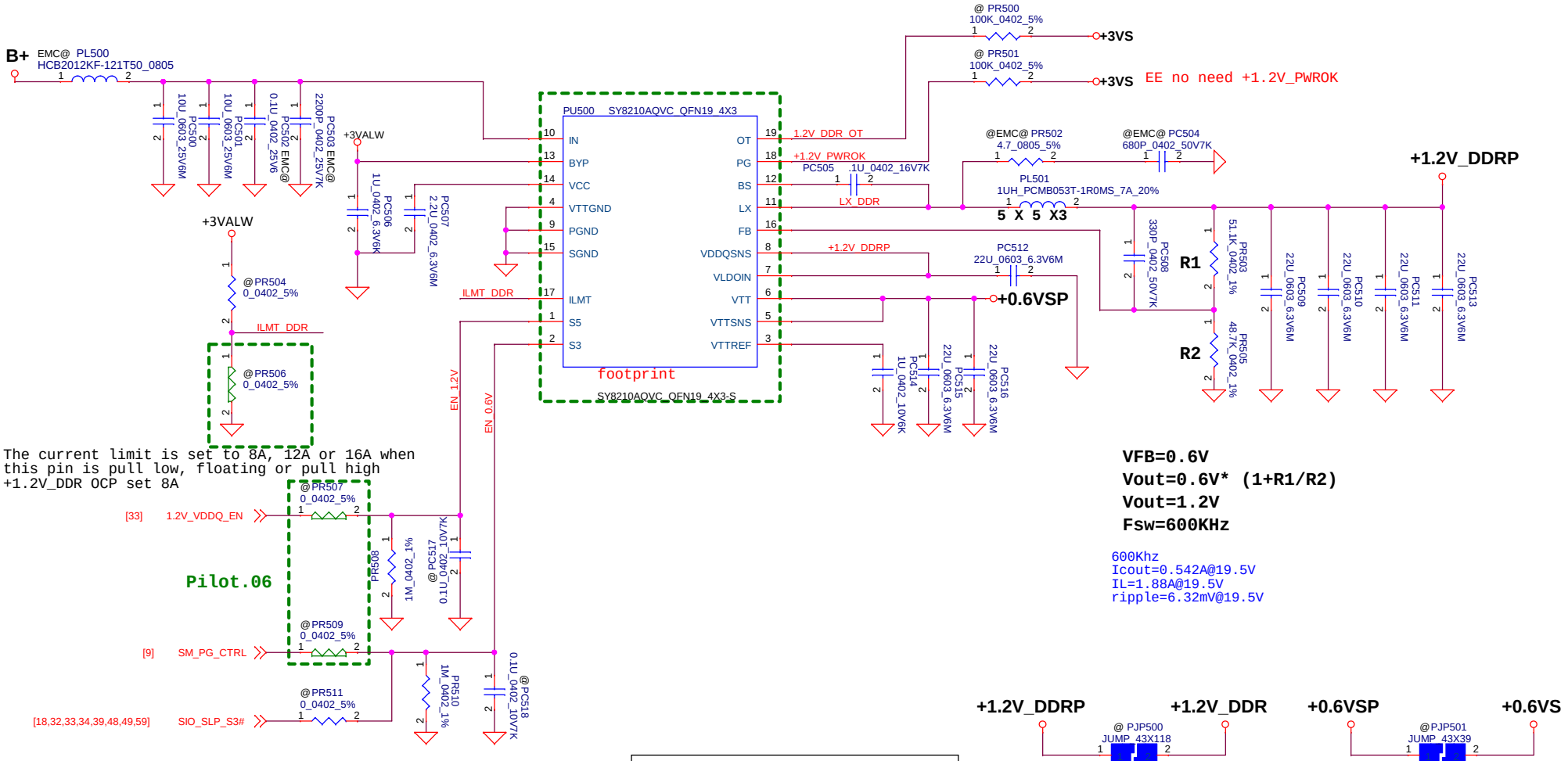
Security Classification	Compal Secret Data		
Issued Date	2013/11/05	Deciphered Date	2015/11/05

Compal Electronics, Inc.

Title: **PWR_3.3VALWP/5VALWP**

Size	Document Number	Rev
Custom		0.1(100)

Date: Thursday, August 18, 2016 Sheet 56 of 70



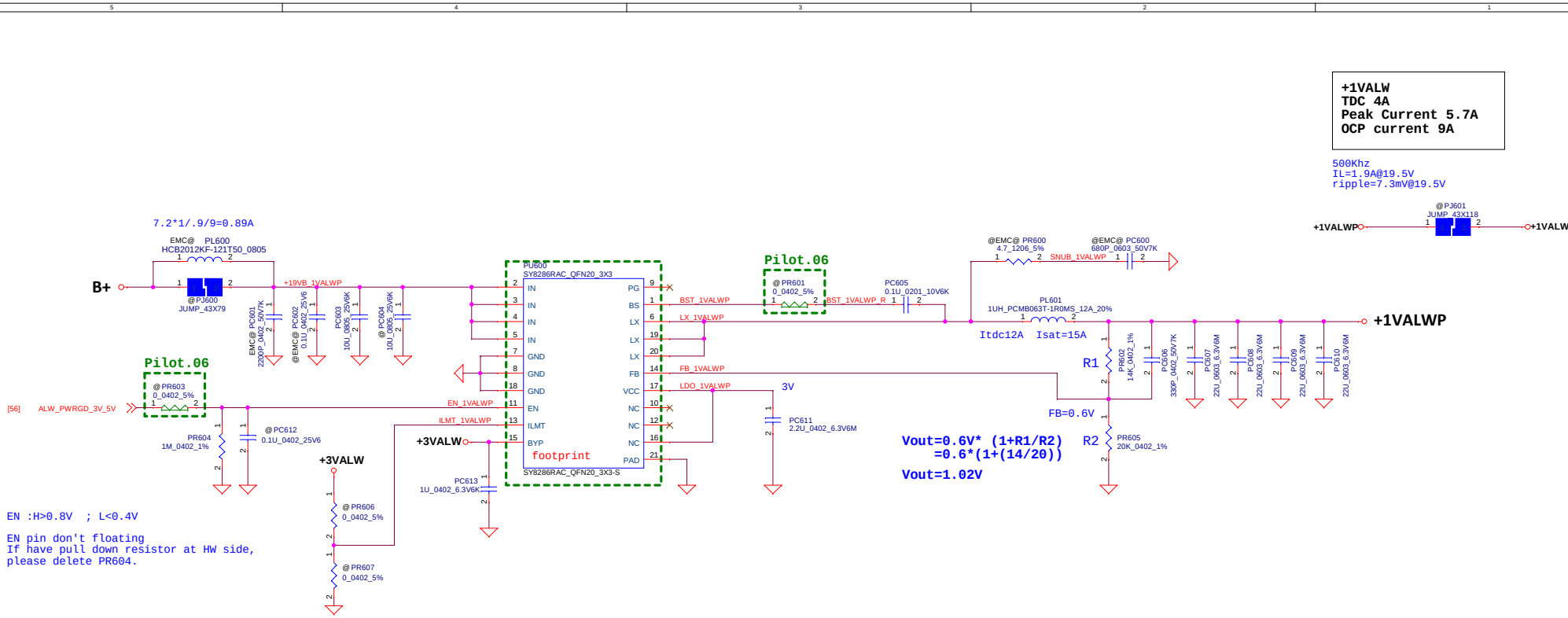
Security Classification	Compal Secret Data		
Issued Date	2014/10/17	Deciphered Date	2014/12/05

Compal Electronics, Inc.

Title: PWR_+1.2V_DDR/0.6VS(SY8210)

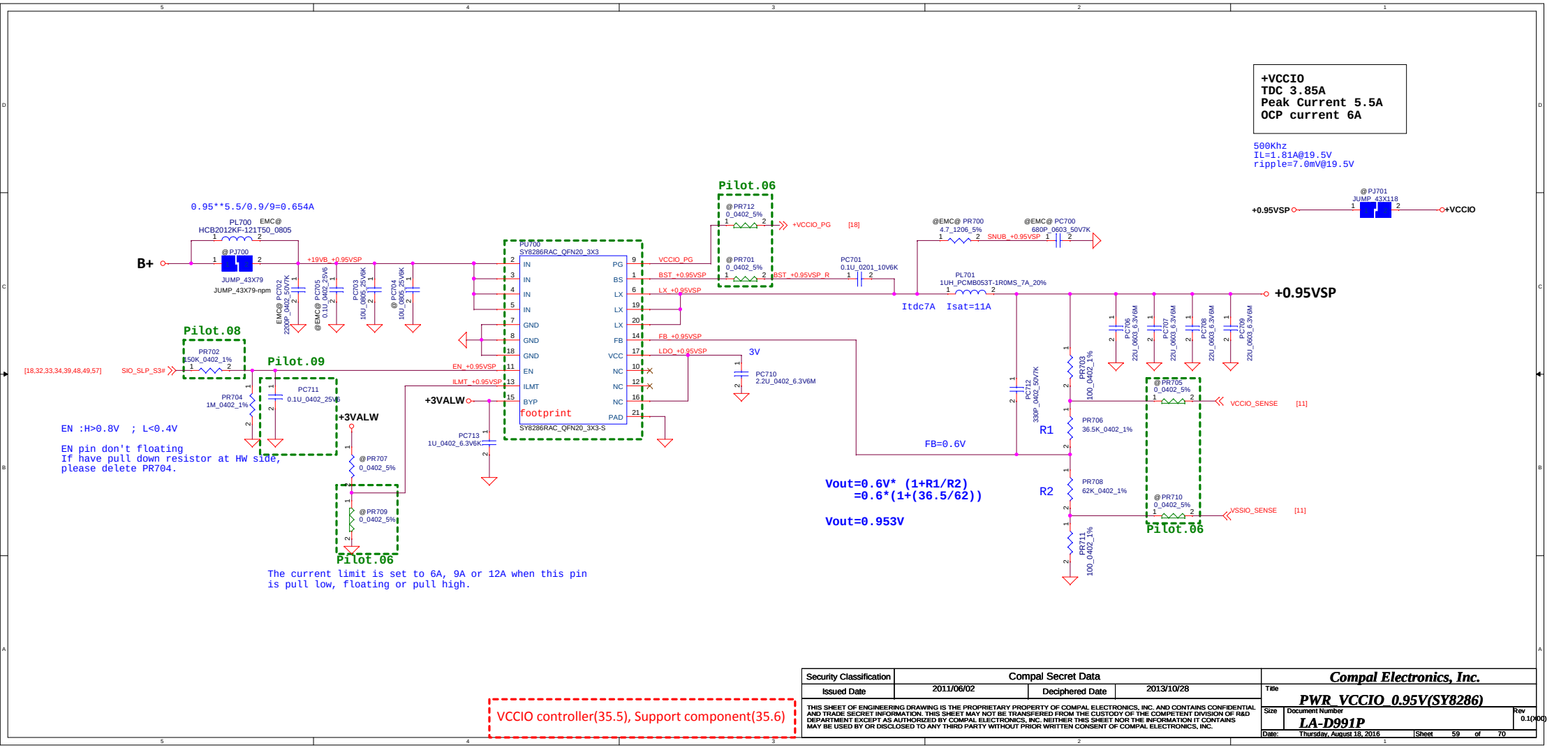
Size | Document Number: LA-D991P | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 57 of 70



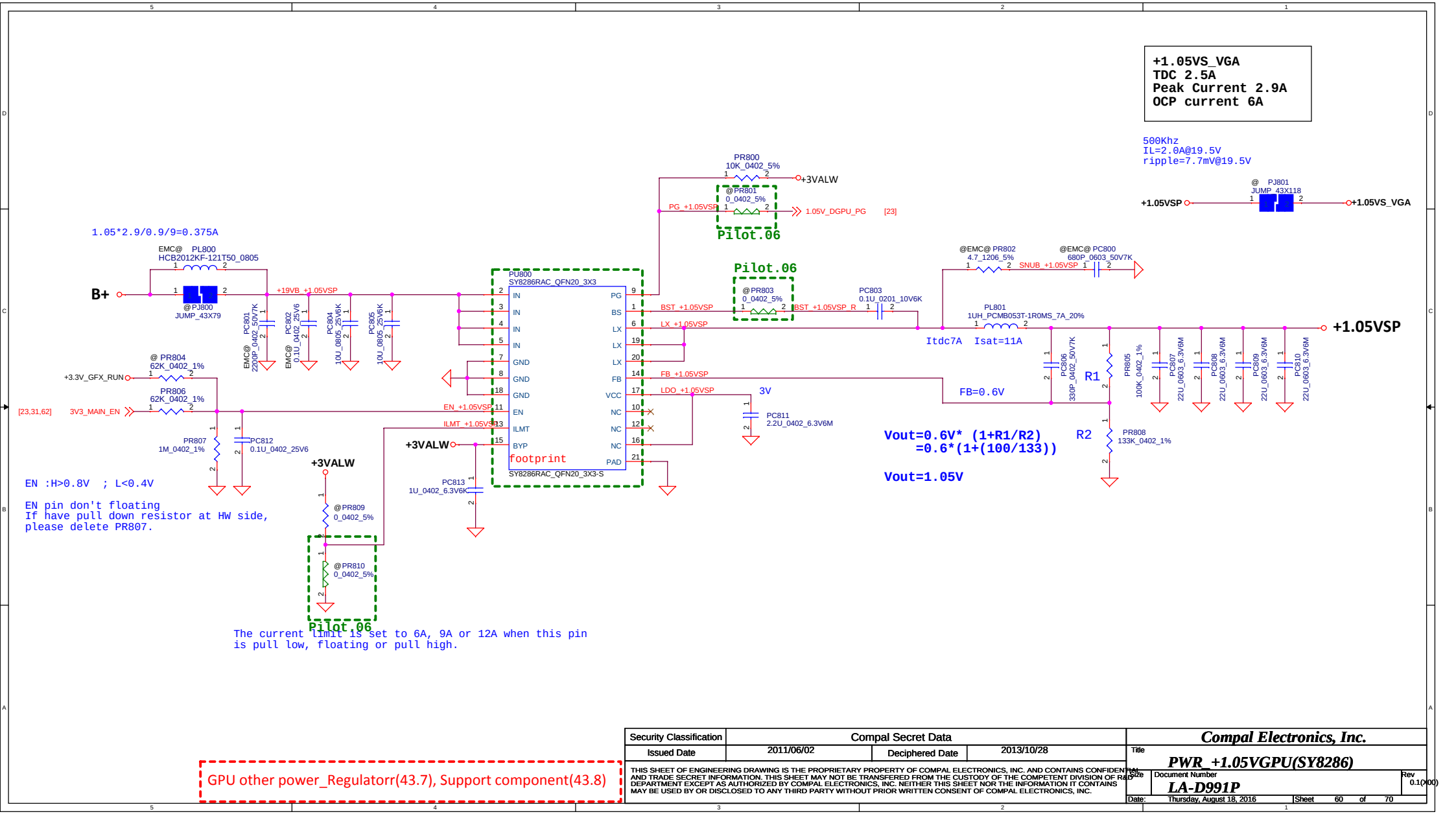
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title: PWR_+1VALW (SY8288)			
Size	Document Number: LA-D991P		Rev: 0.1(X00)
Date: Thursday, August 18, 2016	Sheet 58 of 70		



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.			
Title	PWR_VCCIO_0.95V(SY8286)		
Size	Document Number		Rev
	LA-D991P		0.1(X00)
Date: Thursday, August 18, 2016	Sheet 59 of 70		



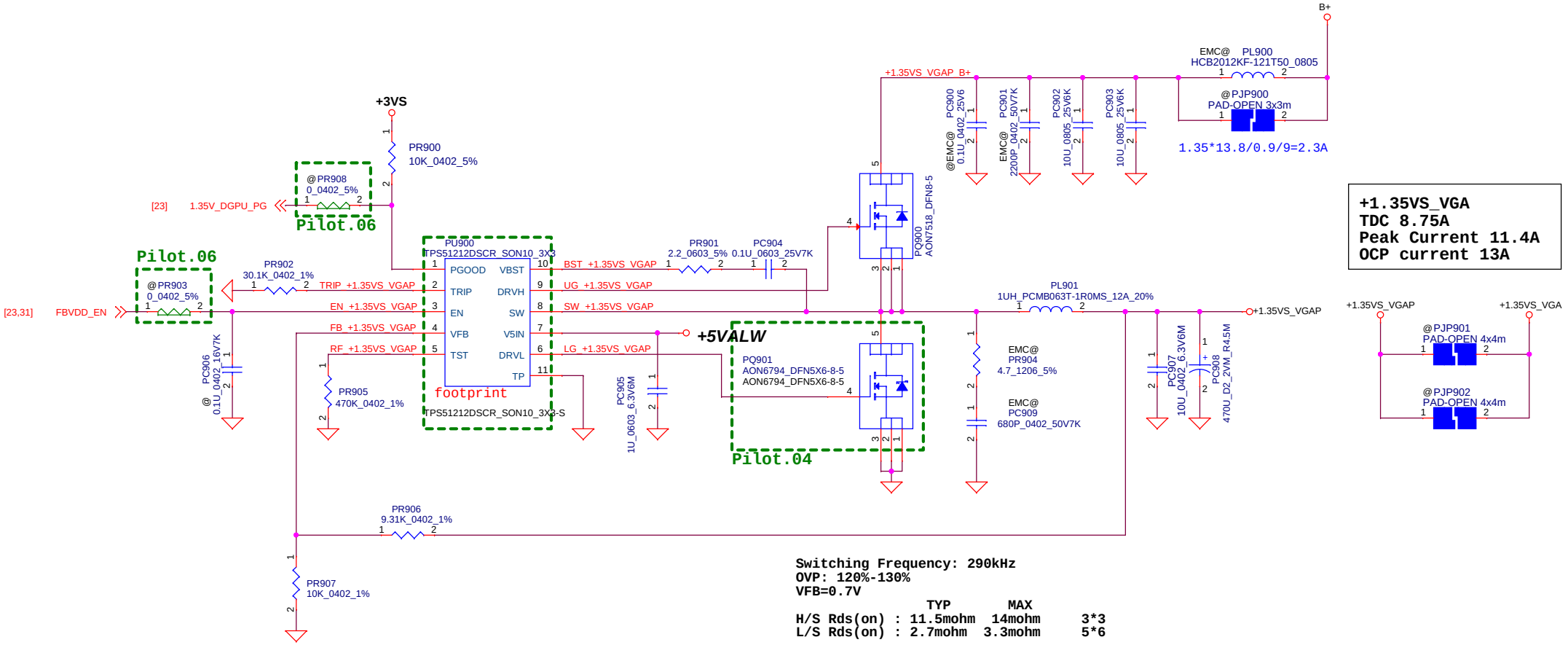
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: PWR_+1.05VGPU(SY8286)

Size | Document Number: LA-D991P | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 60 of 70



+1.35VS_VGA
TDC 8.75A
Peak Current 11.4A
OCP current 13A

Switching Frequency: 290kHz
OVP: 120%-130%
VFB=0.7V

	TYP	MAX	
H/S Rds(on) :	11.5mohm	14mohm	3*3
L/S Rds(on) :	2.7mohm	3.3mohm	5*6

Ripple=34.3mV
△I=4.33A

GPU other power_Regulatorr(43.5), Support component(43.6)

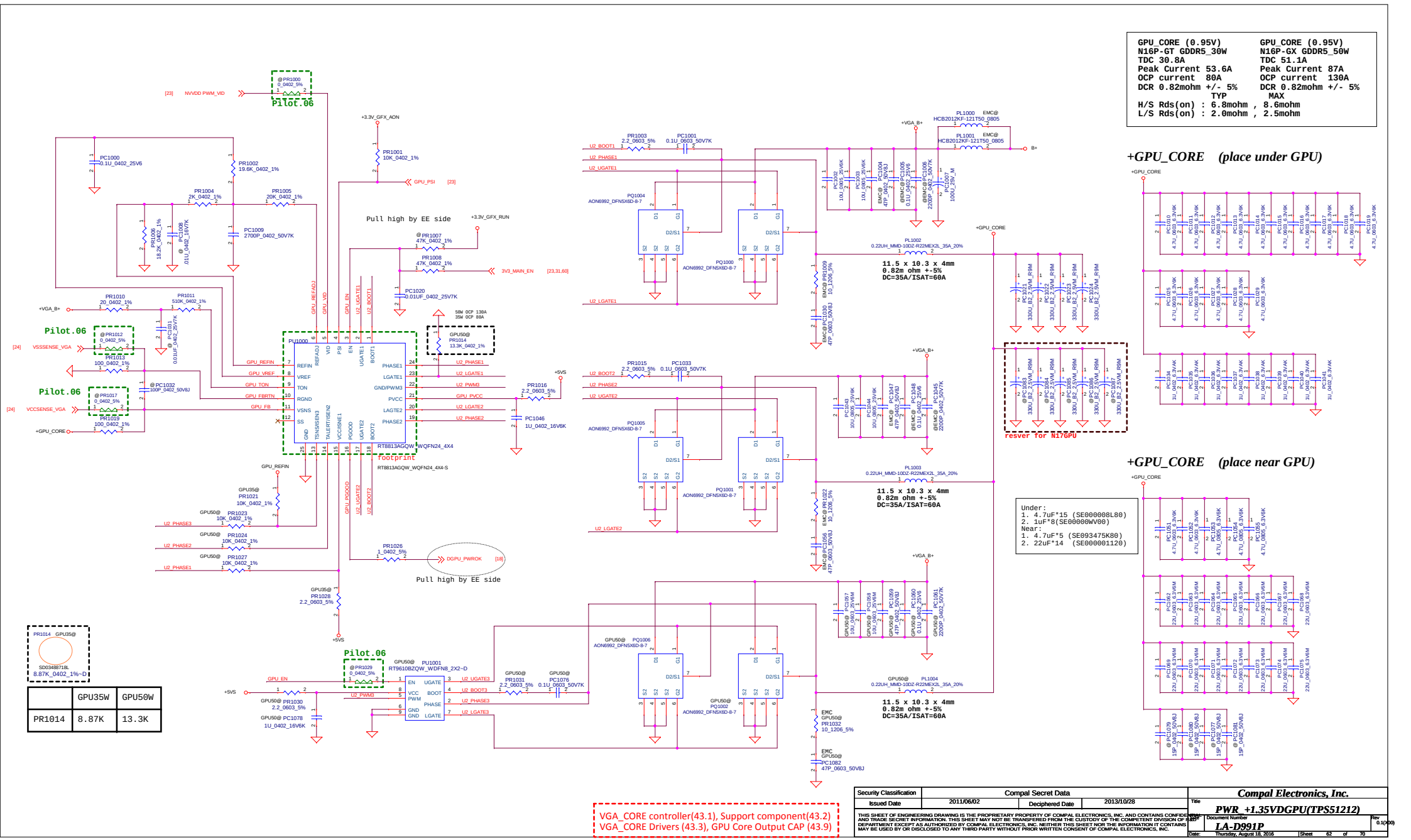
Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

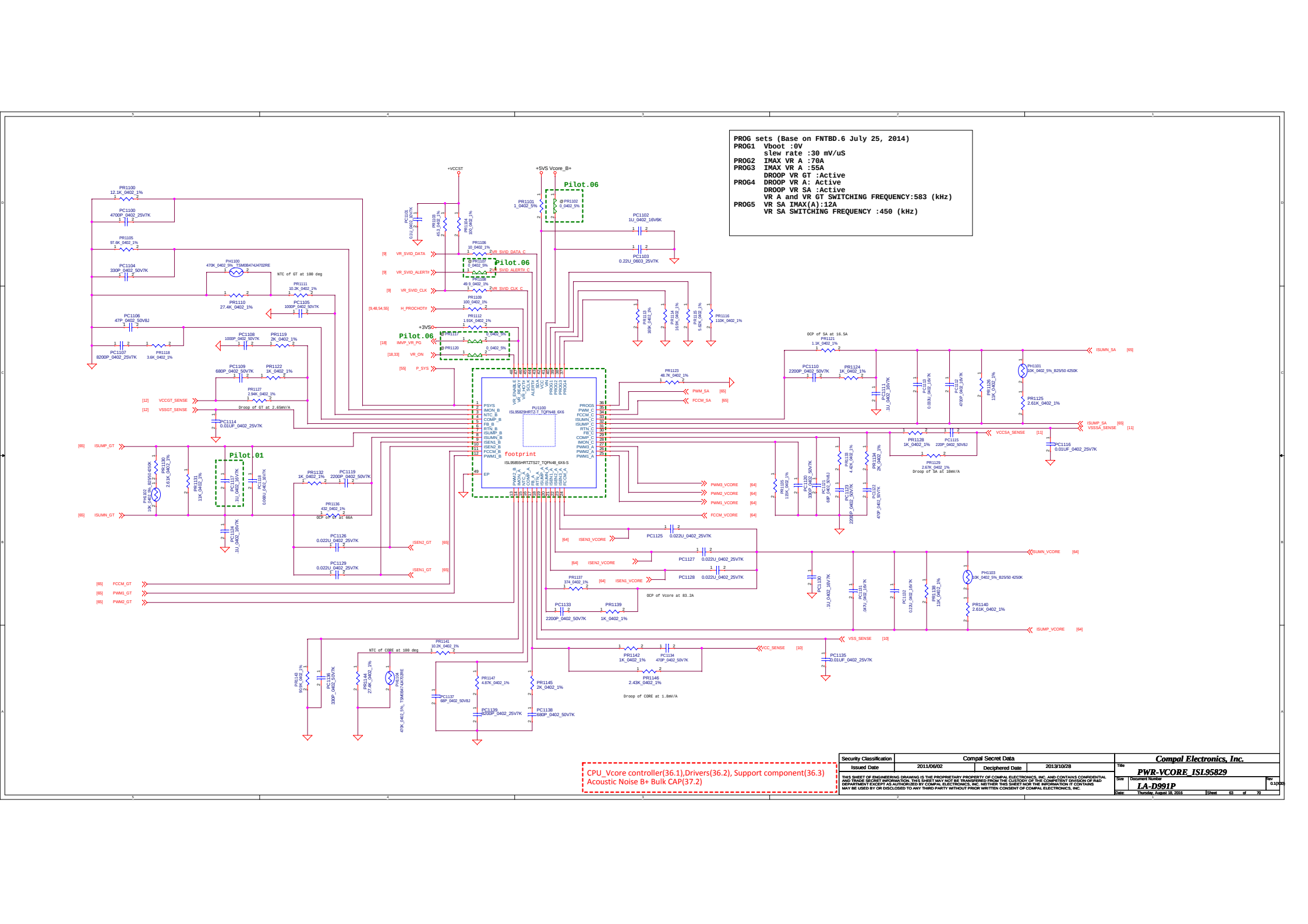
Title: PWR_+1.35VDGPU(TPS51212)

Size | Document Number: LA-D991P | Rev: 0.1(X00)

Date: Thursday, August 18, 2016 | Sheet 61 of 70



	GPU35W	GPU50W
PR1014	8.87K	13.3K


PROG sets (Base on FNTBD.6 July 25, 2014)
PROG1 Vboot :0V
slew rate :30 mV/uS
PROG2 IMAX VR A :70A
PROG3 IMAX VR A :55A
DROOP VR GT :Active
PROG4 DROOP VR A: Active
DROOP VR SA :Active
VR A and VR GT SWITCHING FREQUENCY:583 (kHz)
PROG5 VR SA IMAX(A):12A
VR SA SWITCHING FREQUENCY :450 (kHz)
Pilot.06
Pilot.01
footprint
ISL95829HRT2-T_TQFN48_6X6
ISL95855HRTZTS27_TQFN48_6X6-S
NTC of GT at 100 deg
NTC of CORE at 100 deg
Droop of GT at 2.65mV/A
Droop of SA at 10mV/A
Droop of CORE at 1.8mV/A
OCP of Vcore at 83.2A
OCP of SA at 16.5A
OCP of GT at 86A
CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3)
Acoustic Noise B+ Bulk CAP(37.2)
Compal Secret Data
2011/06/02
2013/10/28
Compal Electronics, Inc.
PWR-VCORE_ISL95829
LA-D991P
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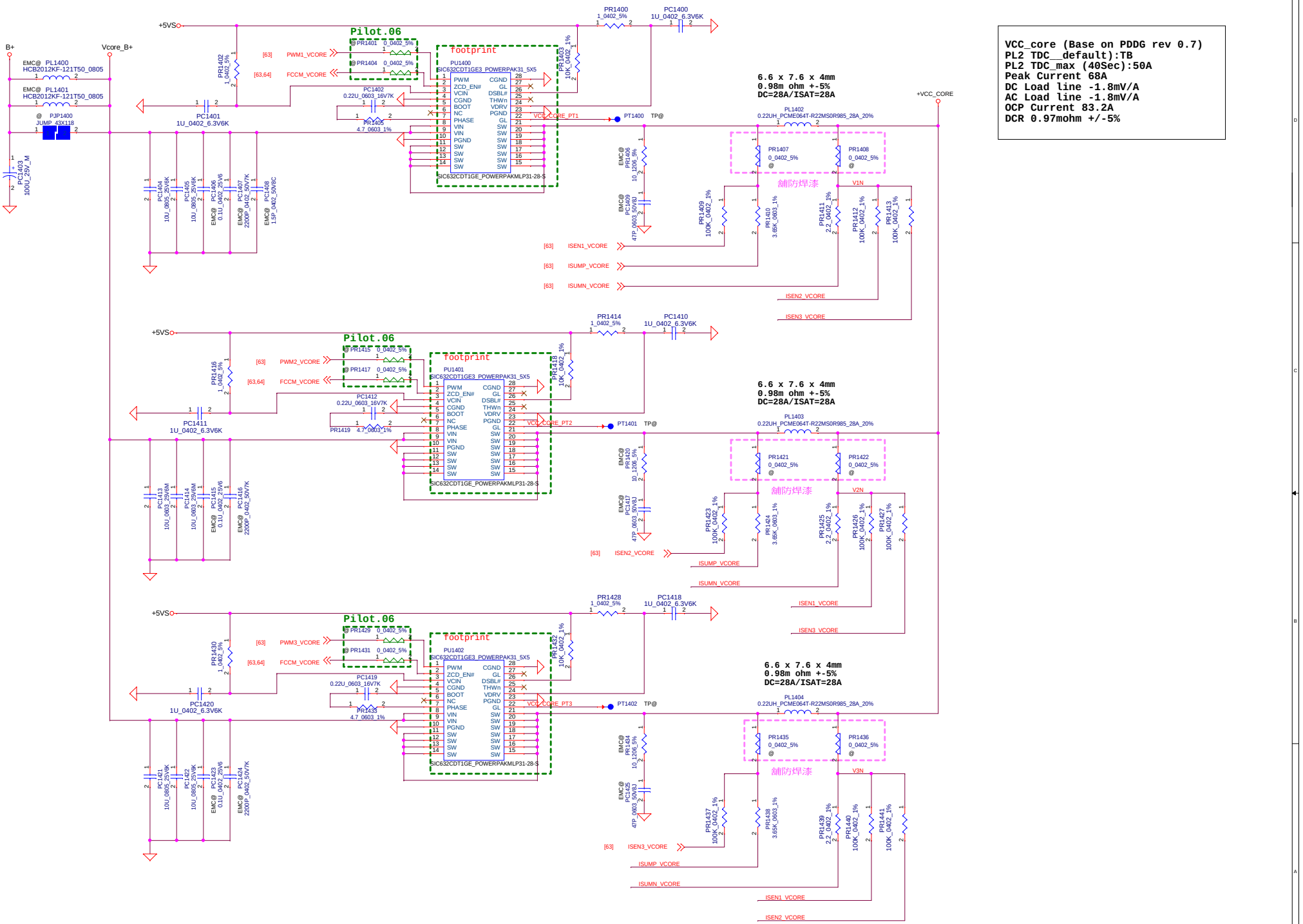
VCC_core (Base on PDDG rev 0.7)
PL2 TDC__default):TB
PL2 TDC_max (40Sec):50A
Peak Current 68A
AC Load line -1.8mV/A
OCP Current 83.2A
DCR 0.97mohm +/-5%
6.6 x 7.6 x 4mm
0.98m ohm +-5%
DC=28A/ISAT=28A
Pilot.06
footprint
SIC632CDT1GE3_POWERPAKMLP31-28-S
舖防焊漆
+5VS
+VCC_CORE
B+
Vcore_B+
PWM1_VCORE
PWM2_VCORE
PWM3_VCORE
FCCM_VCORE
ISEN1_VCORE
ISEN2_VCORE
ISEN3_VCORE
ISUMP_VCORE
ISUMN_VCORE
VCC_CORE_PT1
VCC_CORE_PT2
VCC_CORE_PT3
CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3),
CPU_Core output CAP(36.4),Acoustic Noise B+ Bulk CAP(37.2)
Compal Secret Data
2011/06/02
2013/10/28
Compal Electronics, Inc.
PWR-VCORE_VCORE
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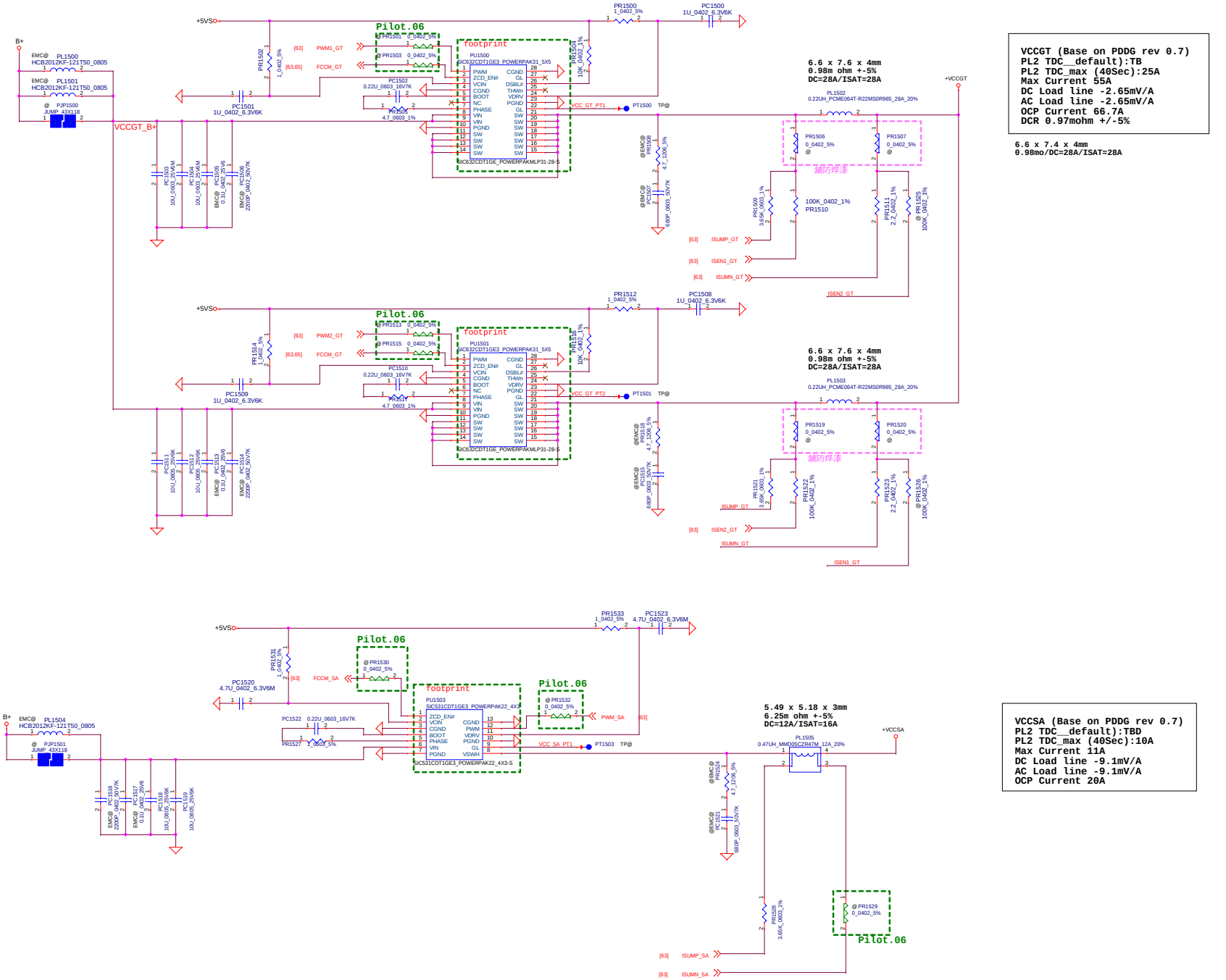
VCCGT (Base on PDDG rev 0.7)
PL2 TDC__default):TB
PL2 TDC_max (40Sec):25A
Max Current 55A
DC Load line -2.65mV/A
AC Load line -2.65mV/A
OCP Current 66.7A
DCR 0.97mohm +/-5%
6.6 x 7.4 x 4mm
0.98mo/DC=28A/ISAT=28A
6.6 x 7.6 x 4mm
0.98m ohm +-5%
DC=28A/ISAT=28A
6.6 x 7.6 x 4mm
0.98m ohm +-5%
DC=28A/ISAT=28A
VCCSA (Base on PDDG rev 0.7)
PL2 TDC__default):TBD
PL2 TDC_max (40Sec):10A
Max Current 11A
DC Load line -9.1mV/A
AC Load line -9.1mV/A
OCP Current 20A
5.49 x 5.18 x 3mm
6.25m ohm +-5%
DC=12A/ISAT=16A
Pilot.06
footprint
+5VS
+VCCGT
+VCCSA
VCCGT_B+
B+
CPU_Vcore controller(36.1),Drivers(36.2), Support component(36.3), GFX output CAP(36.5)
Security Classification
Compal Secret Data
Issued Date
2011/06/02
Deciphered Date
2013/10/28
Compal Electronics, Inc.
PWR_VCORE_VGT,VSA
LA-D991P
Thursday, August 18, 2016
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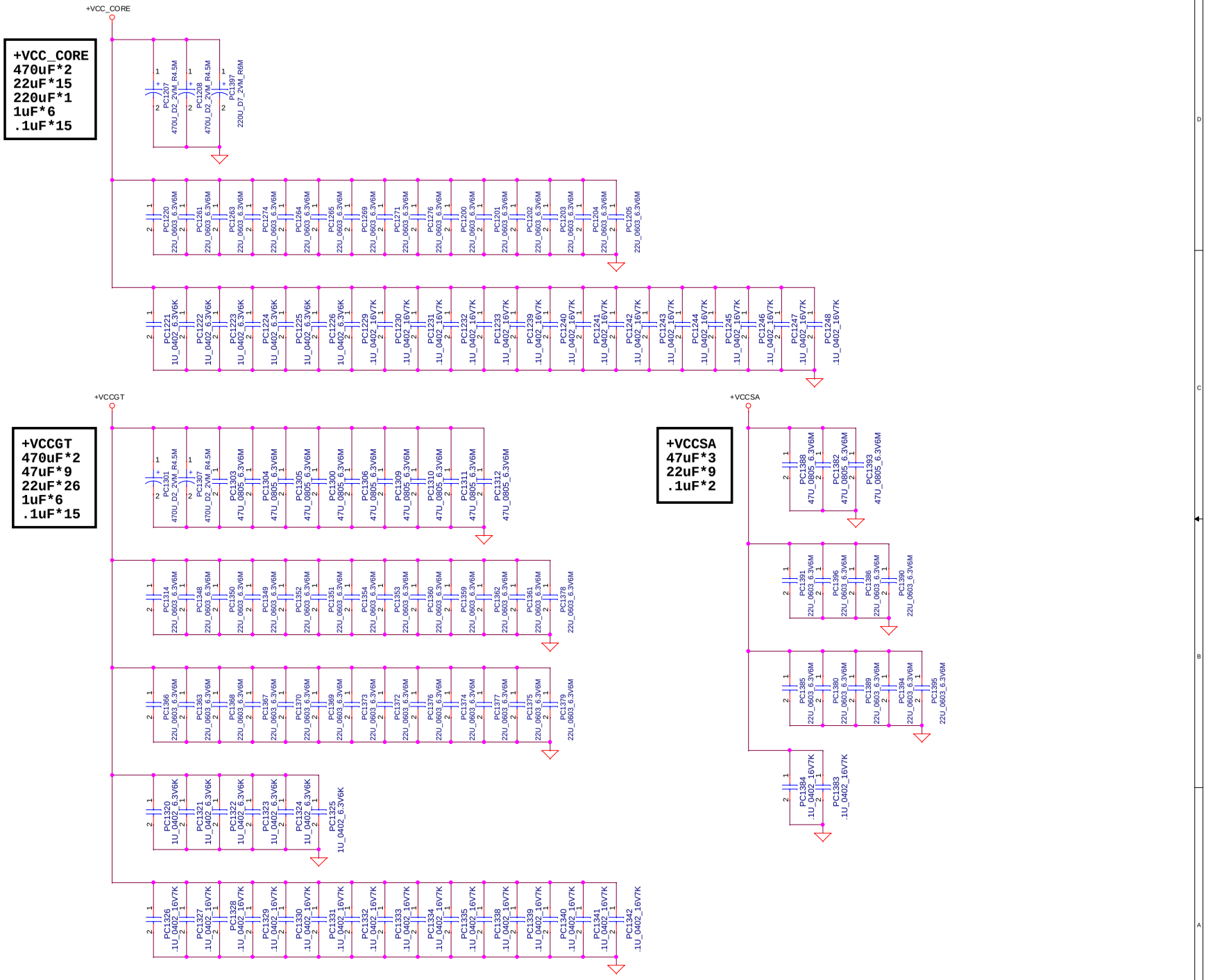

Vcc_CORE output CAP(36.4), Vcc_GT output CAP(36.5), Vcc_SA output CAP(36.6)

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2013/10/28

Compal Electronics, Inc.

Title: **PWR_PROCESSOR_DECOUPING**

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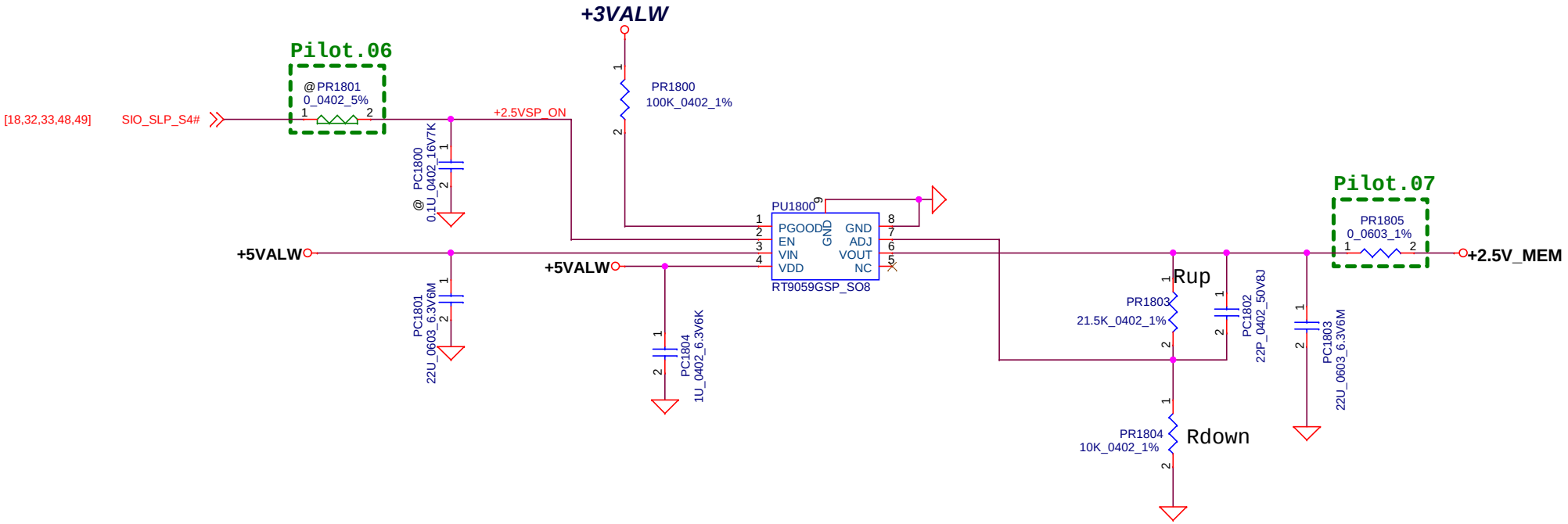
2.5V_MEM controller(35.13), Support component(35.14)

+2.5V_MEM
TDC 0.63A
Peak Current 0.9A
OCP Current 3.5A



Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: PWR_+2.5V_MEM

Size | Document Number: LA-D991P | Rev: 0.1(X00)

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Title	<Title>
Size: A	Document Number: <Doc>
Rev	0.1(X00)
Date:	Thursday, August 18, 2016
Sheet	68 of 70

Version Change List (P. I. R. List) Page 1

Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.

Title	<Title>
Size A	Document Number <Doc>
Rev	<RevCode>
Date:	Thursday, August 18, 2016
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