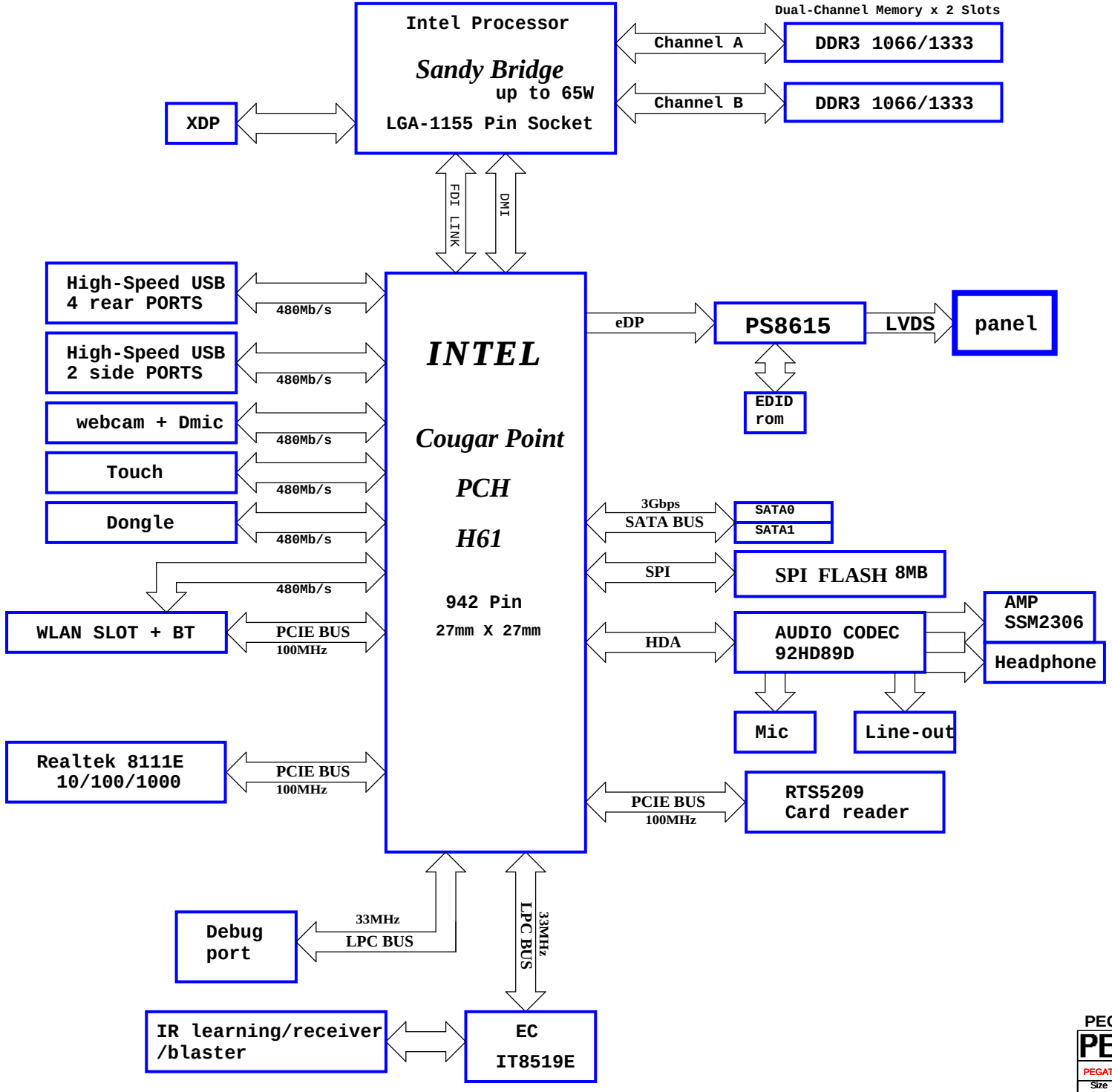


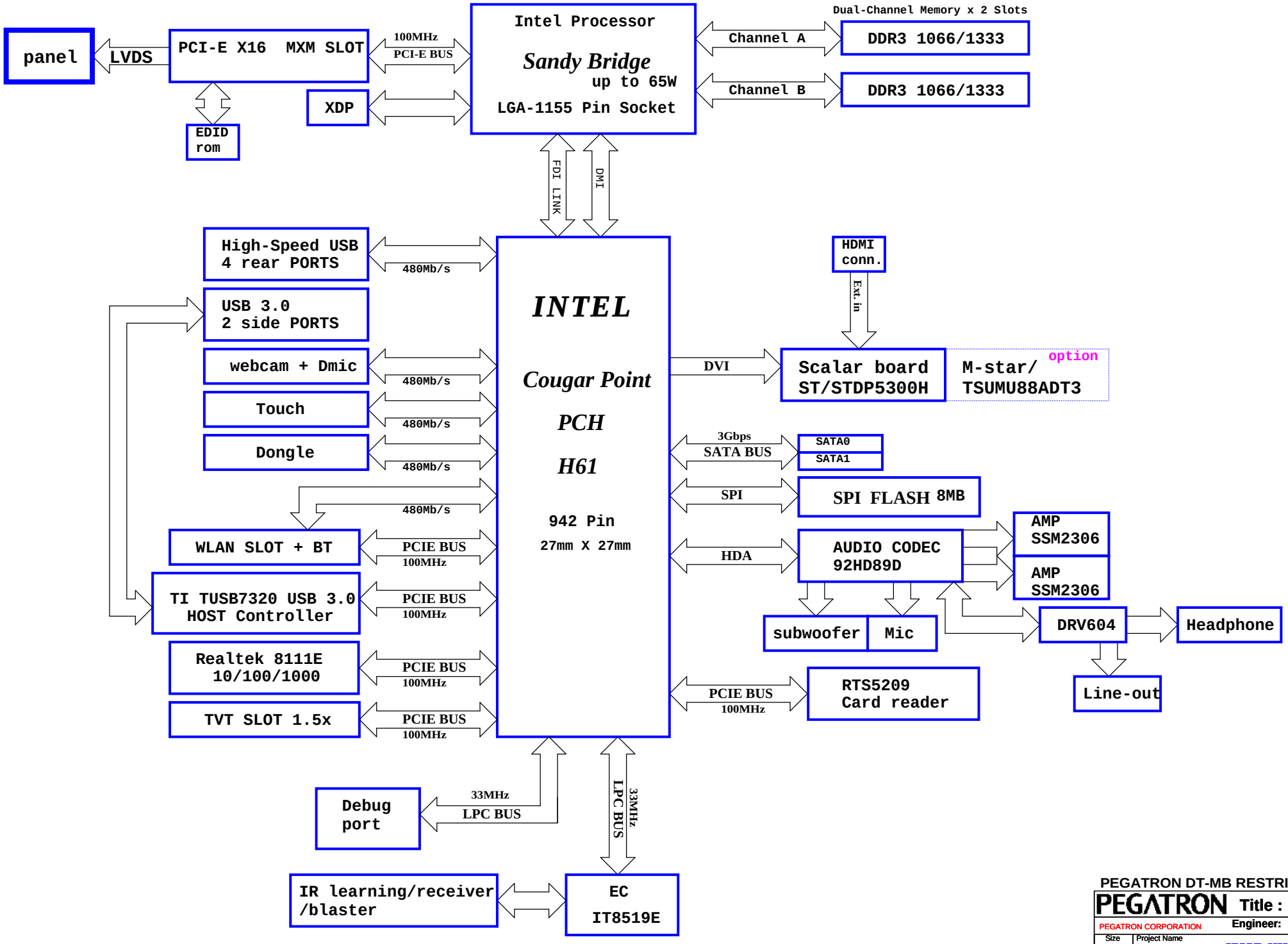
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : BLOVK DIAGRAM

PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 1 of 80



PEGATRON DT-MB RESTRICTED SECRET

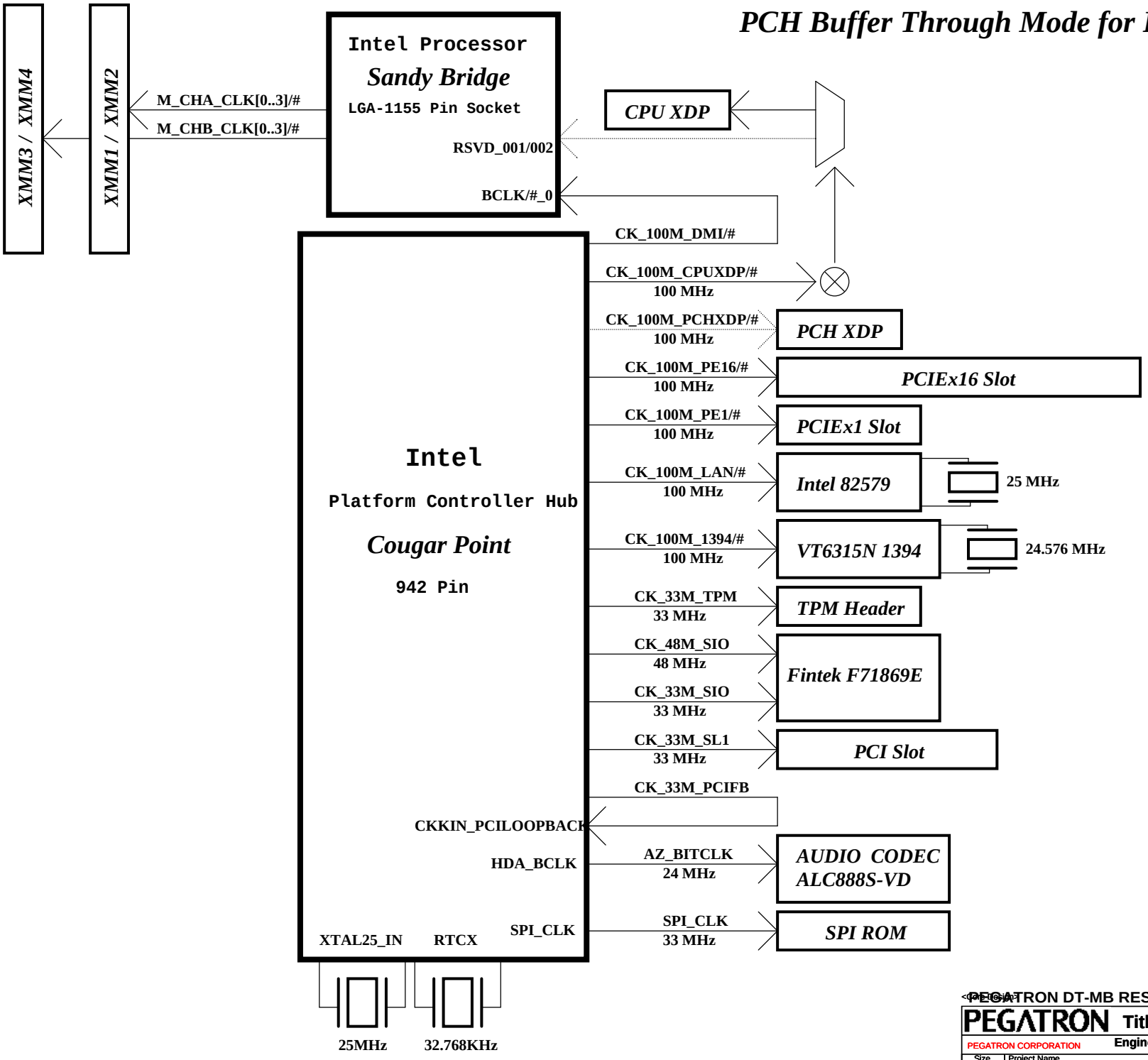
PEGATRON Title : BLOVK DIAGRAM

PEGATRON CORPORATION Engineer: Ethan_Chen

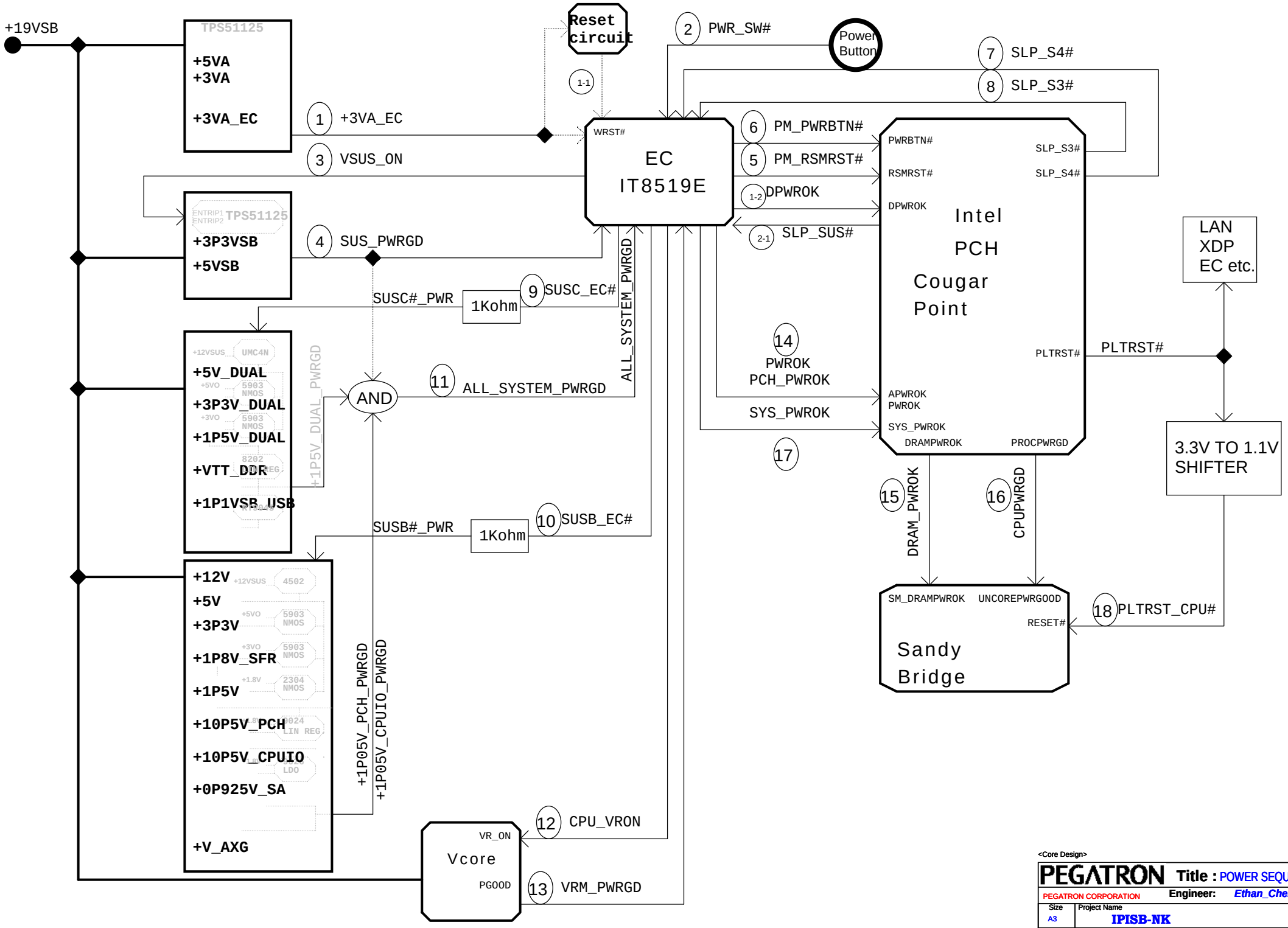
Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 2 of 80

PCH Buffer Through Mode for Pre-Silicon



PEGATRON	Title : CLCOK DISTRIBUTION	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 3 of 80	



<Core Design>

PEGATRON

Title : POWER SEQUENCE

PEGATRON CORPORATION

Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 4 of 80

<Core Design>

PEGATRON

Title : POWER SEQUENCE

PEGATRON CORPORATION

Engineer: Ethan_Chen

Size	Project Name	Rev
A	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 5 of 80

<Core Design>

PEGATRON	Title : POWER SEQUENCE	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: A	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 6 of 80	

<Core Design>

PEGATRON Title : POWER SEQUENCE

PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 7 of 80

<Core Design>

PEGATRON

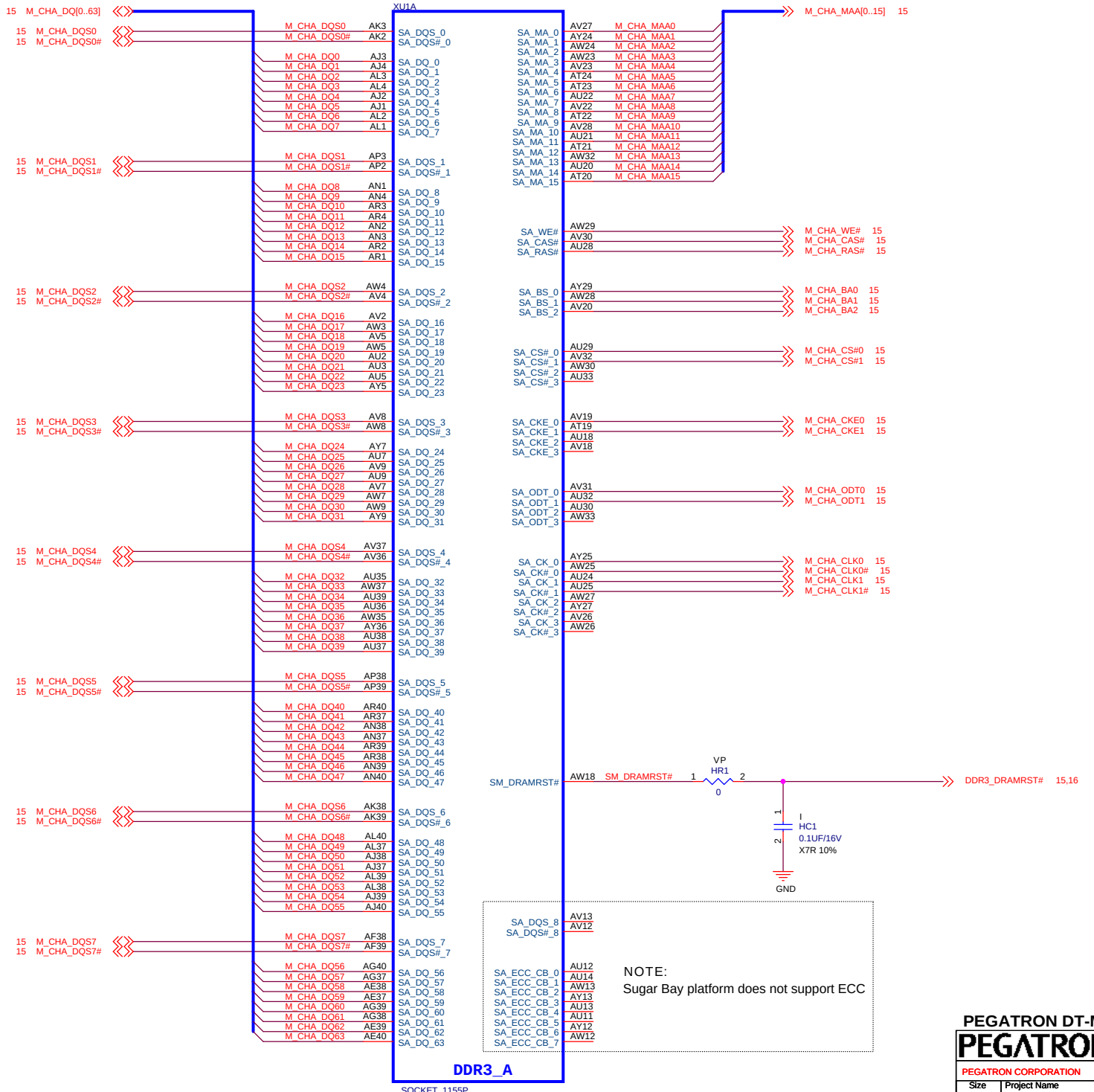
Title : POWER SEQUENCE

PEGATRON CORPORATION

Engineer: Ethan_Chen

Size	Project Name	Rev
A	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 8 of 80



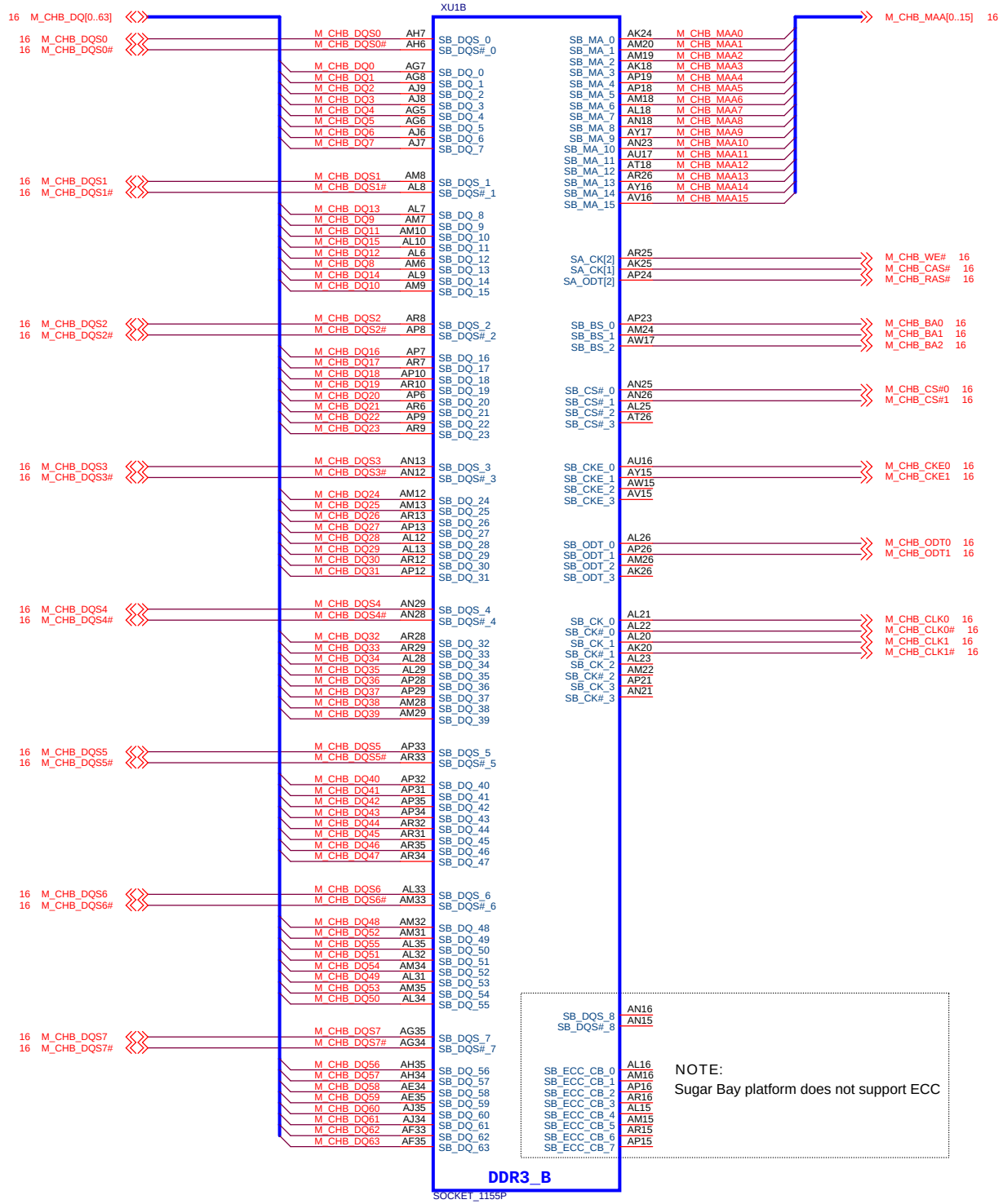
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3_A 1-6

PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 9 of 80



PEGATRON DT-MB RESTRICTED SECRET

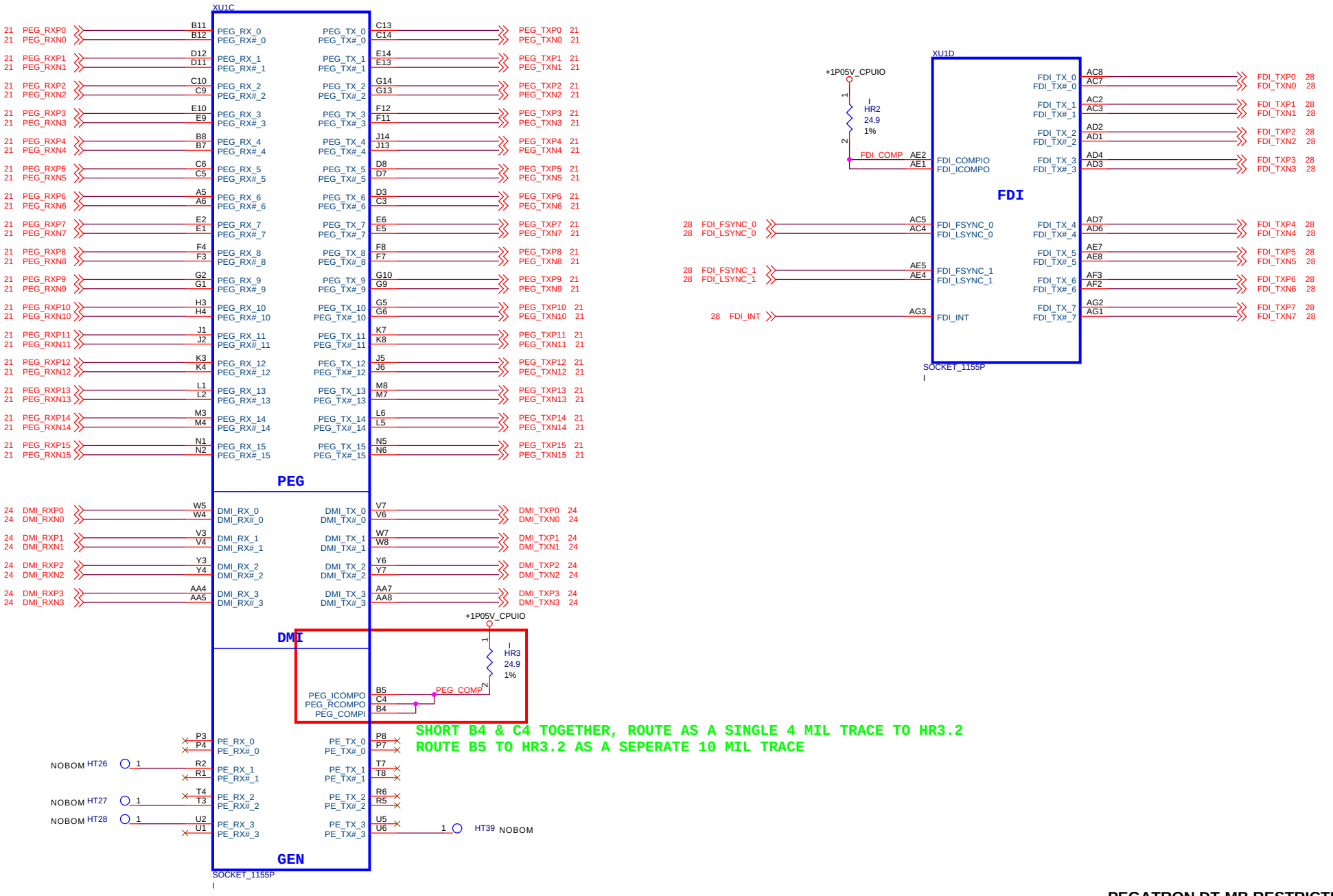
PEGATRON CORPORATION

Title : DDR3_B 2-6

Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 10 of 80



Processor PCI Express* Receive/ Transmit Differential Pair. These signals are available for Workstation only.

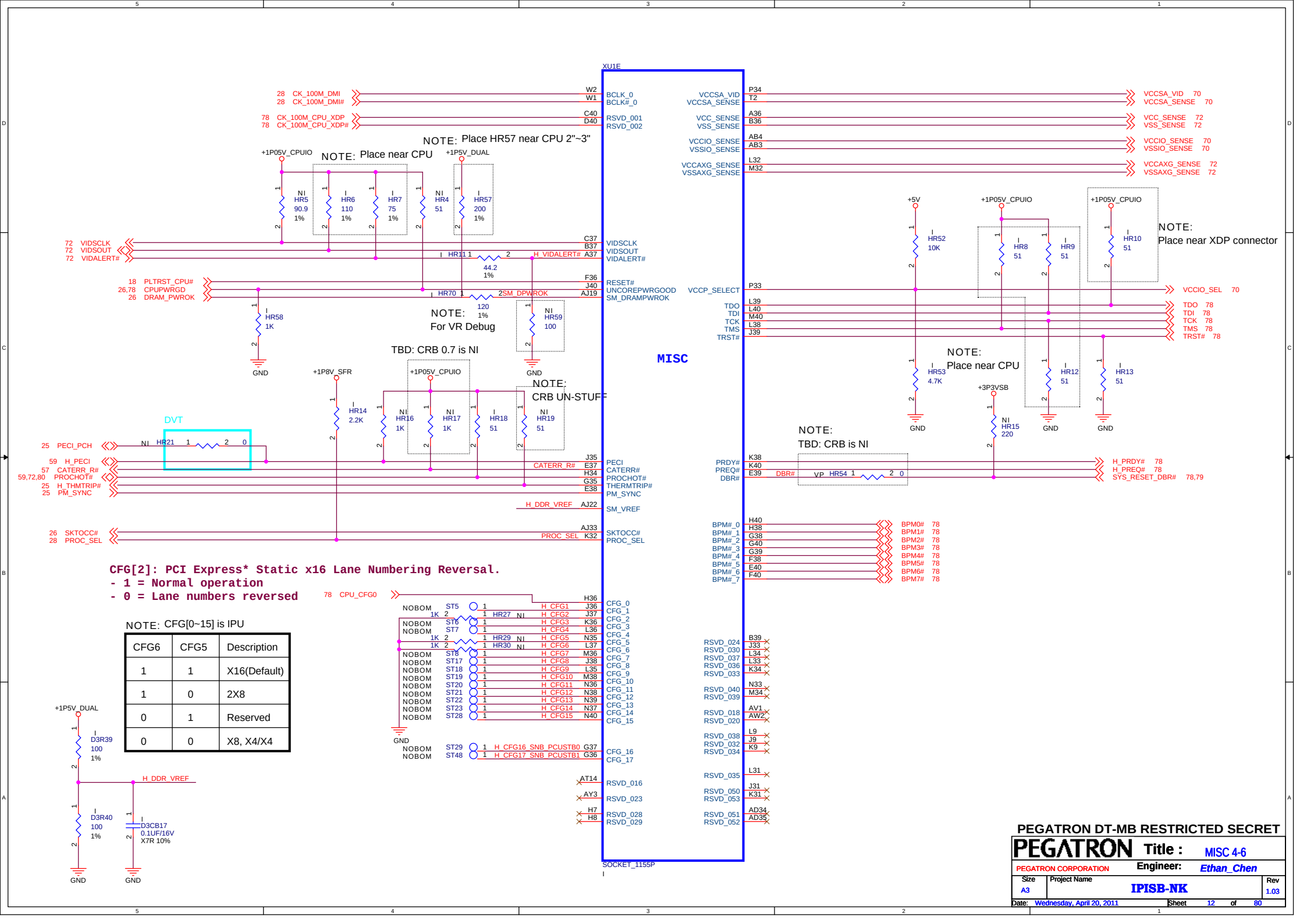
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : PCIE/DMI/FDI 3-6

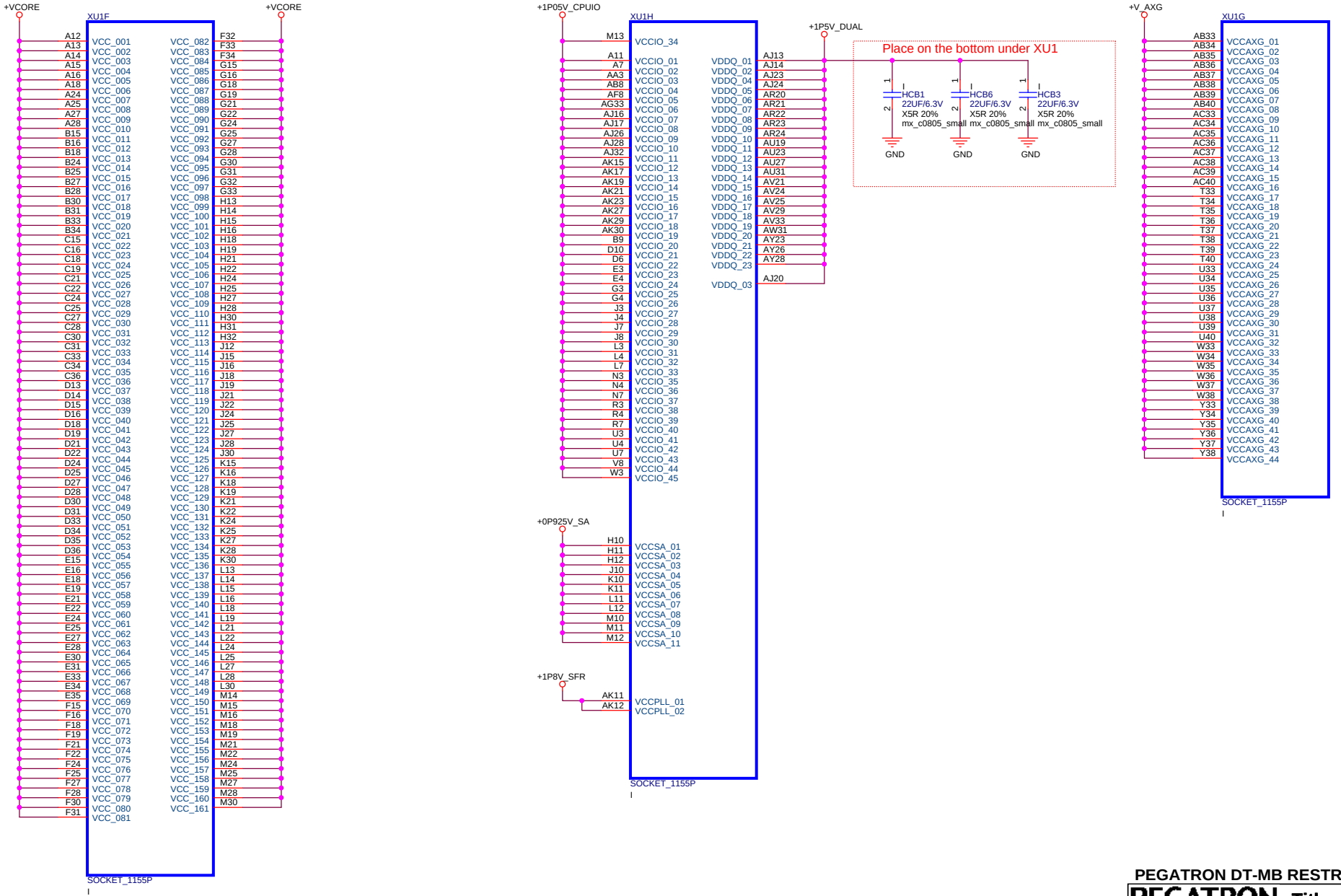
PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 11 of 80



CFG6	CFG5	Description
1	1	X16(Default)
1	0	2X8
0	1	Reserved
0	0	X8, X4/X4



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON

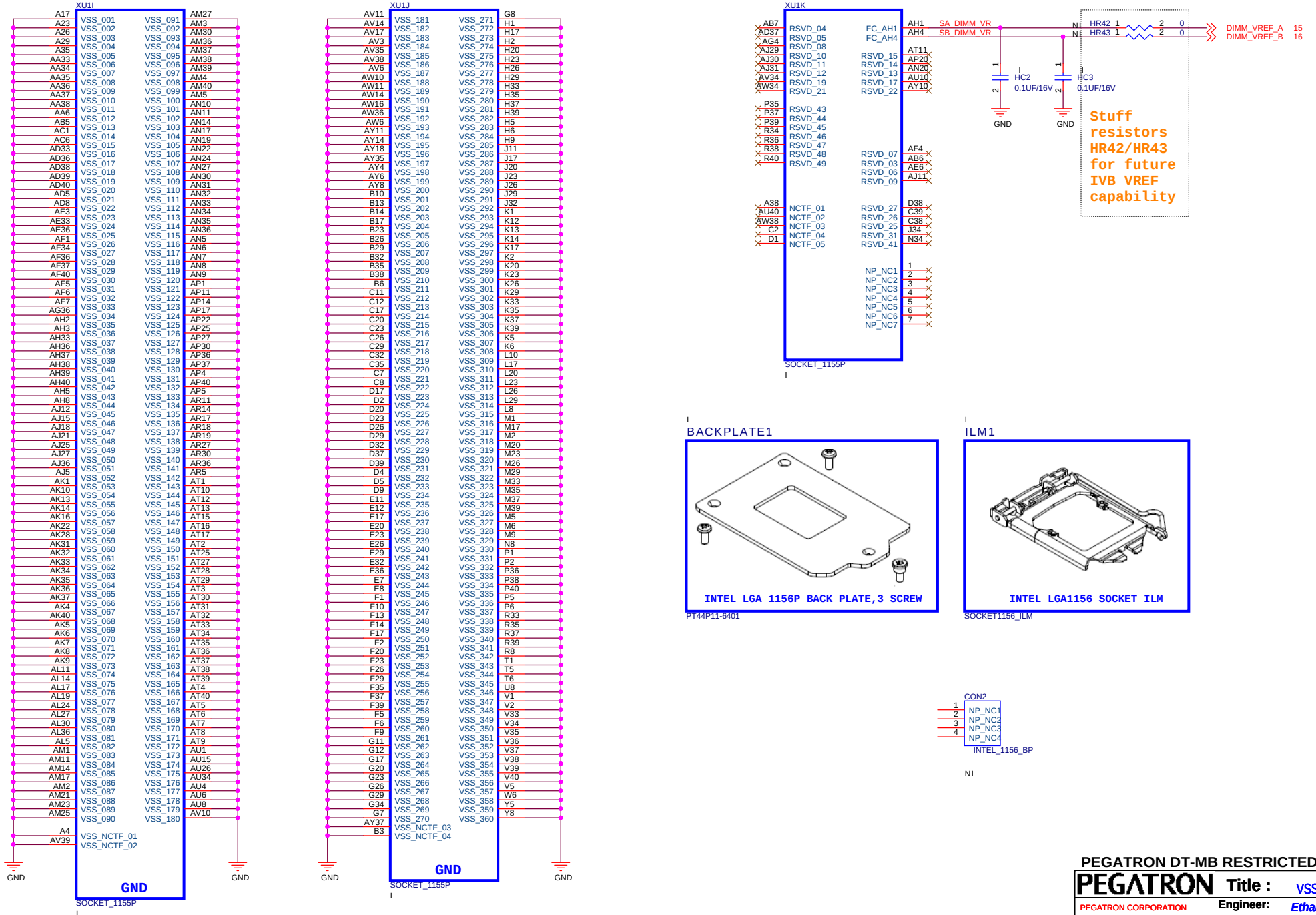
Title : VCC 5 - 6

PEGATRON CORPORATION

Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 13 of 80



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON

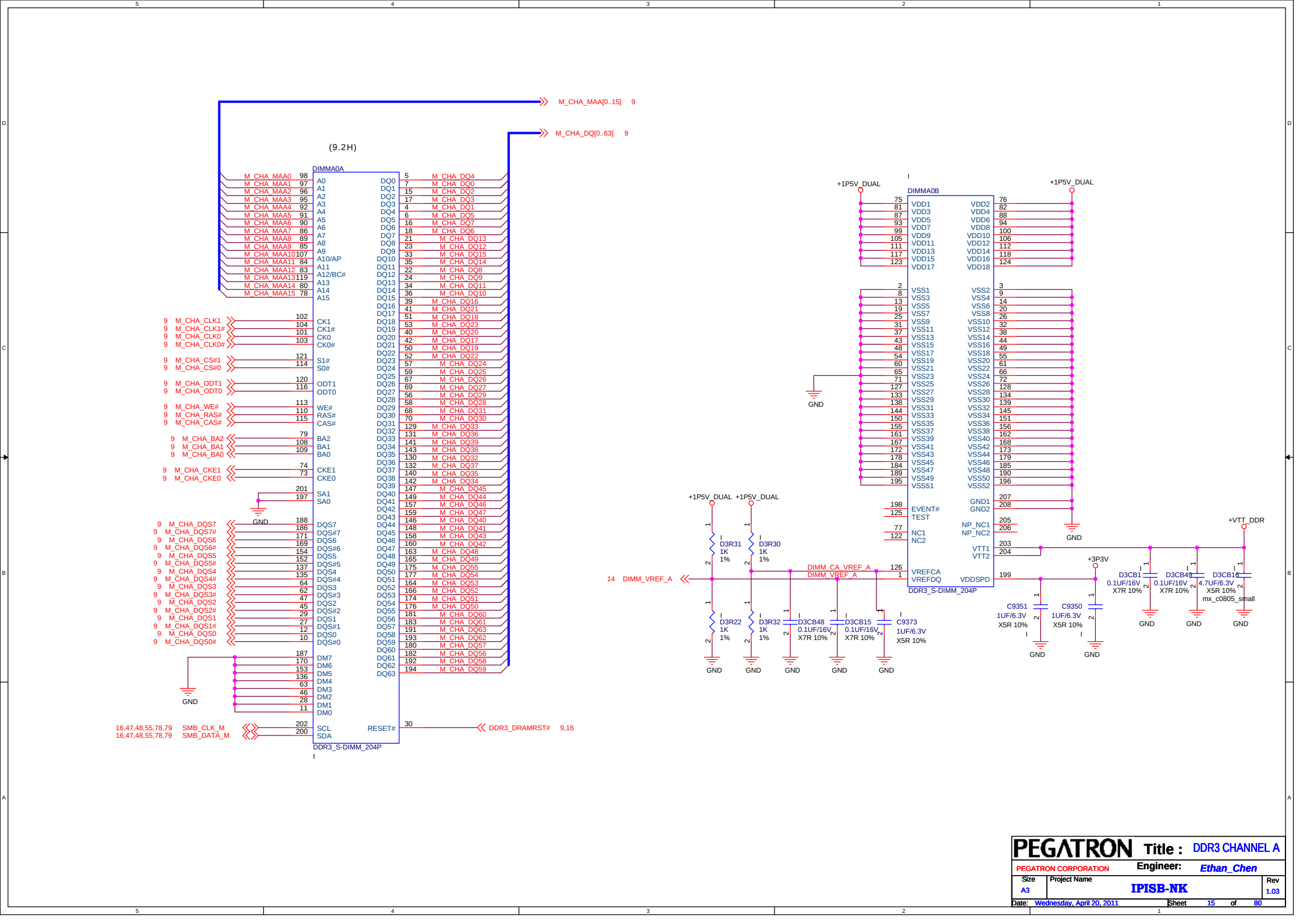
Title : VSS 6 - 6

PEGATRON CORPORATION

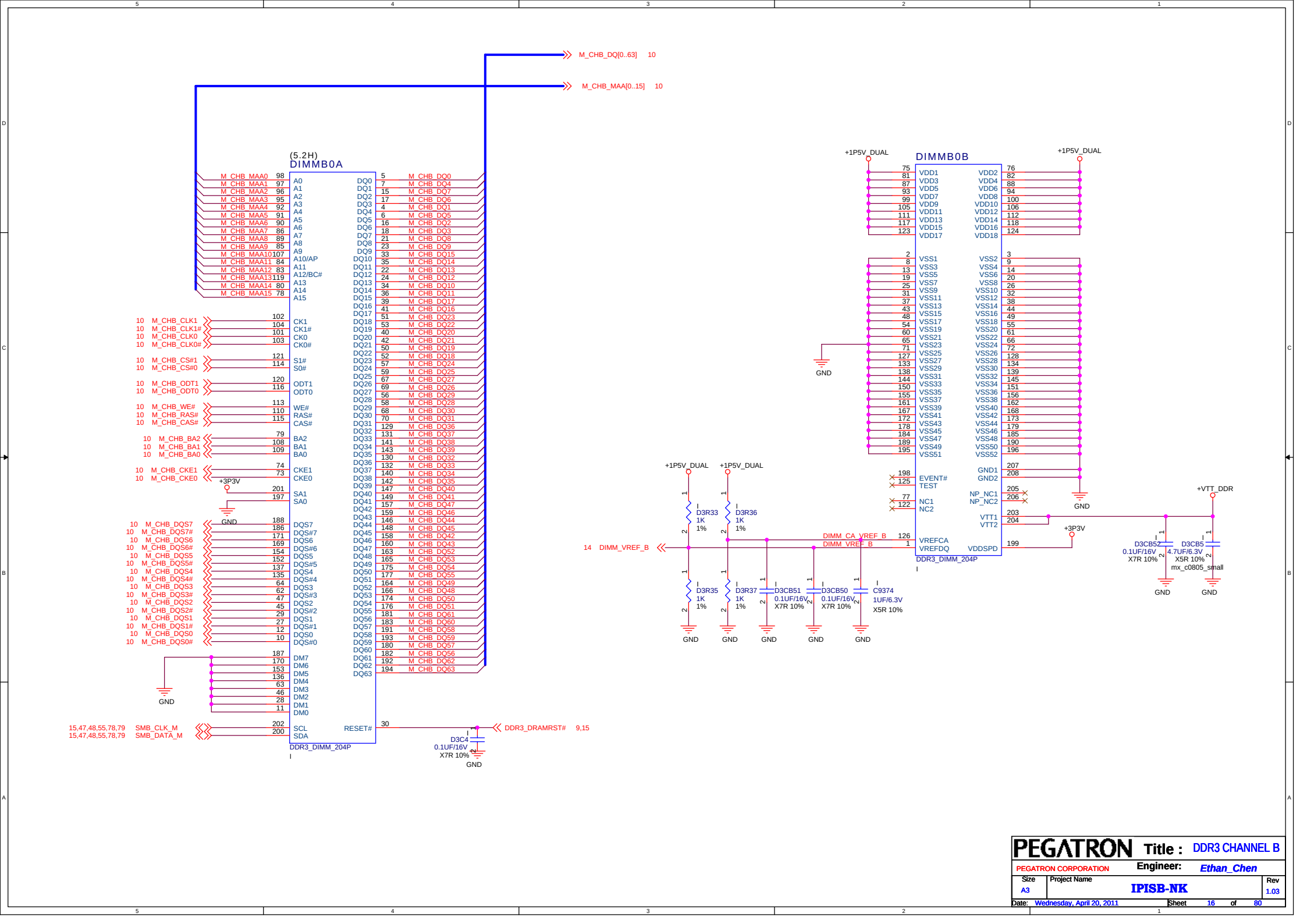
Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Thursday, April 21, 2011 Sheet 14 of 80



PEGATRON	Title :	DDR3 CHANNEL A	
PEGATRON CORPORATION	Engineer:	Ethan_Chen	
Size: A3	Project Name: IPISB-NK		Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 15 of 80		



PEGATRON

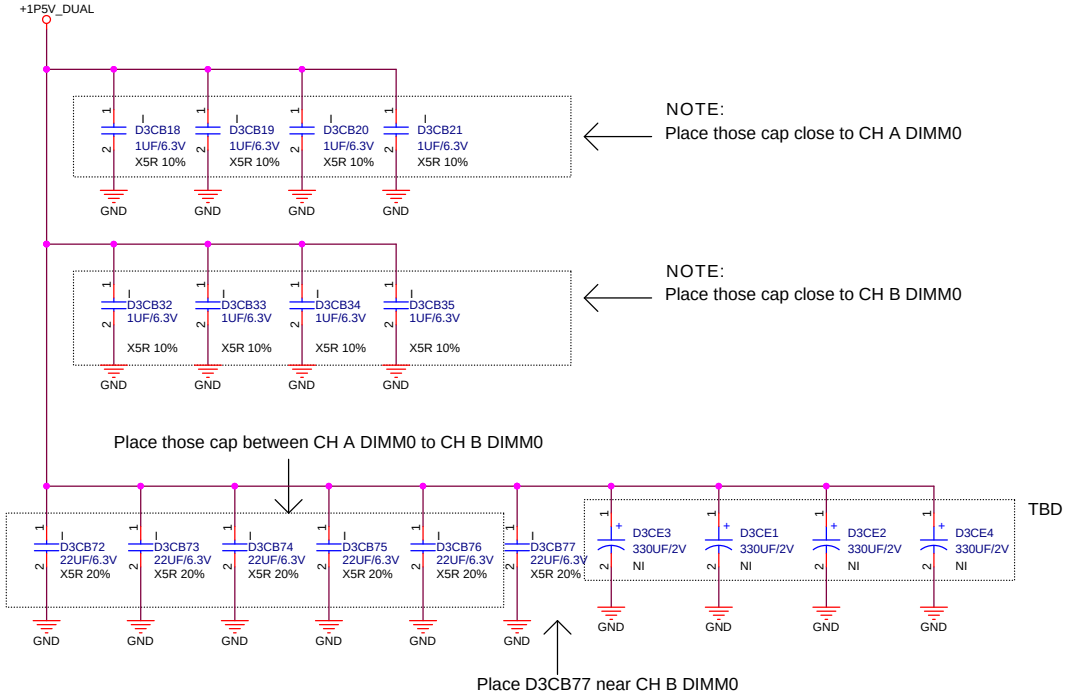
Title : DDR3 CHANNEL B

PEGATRON CORPORATION

Engineer: Ethan_Chen

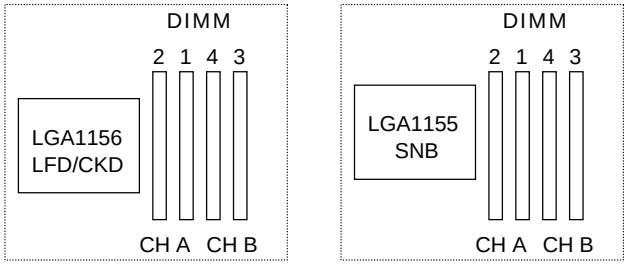
Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 16 of 80



NOTE:

DIMM Placement for different platform



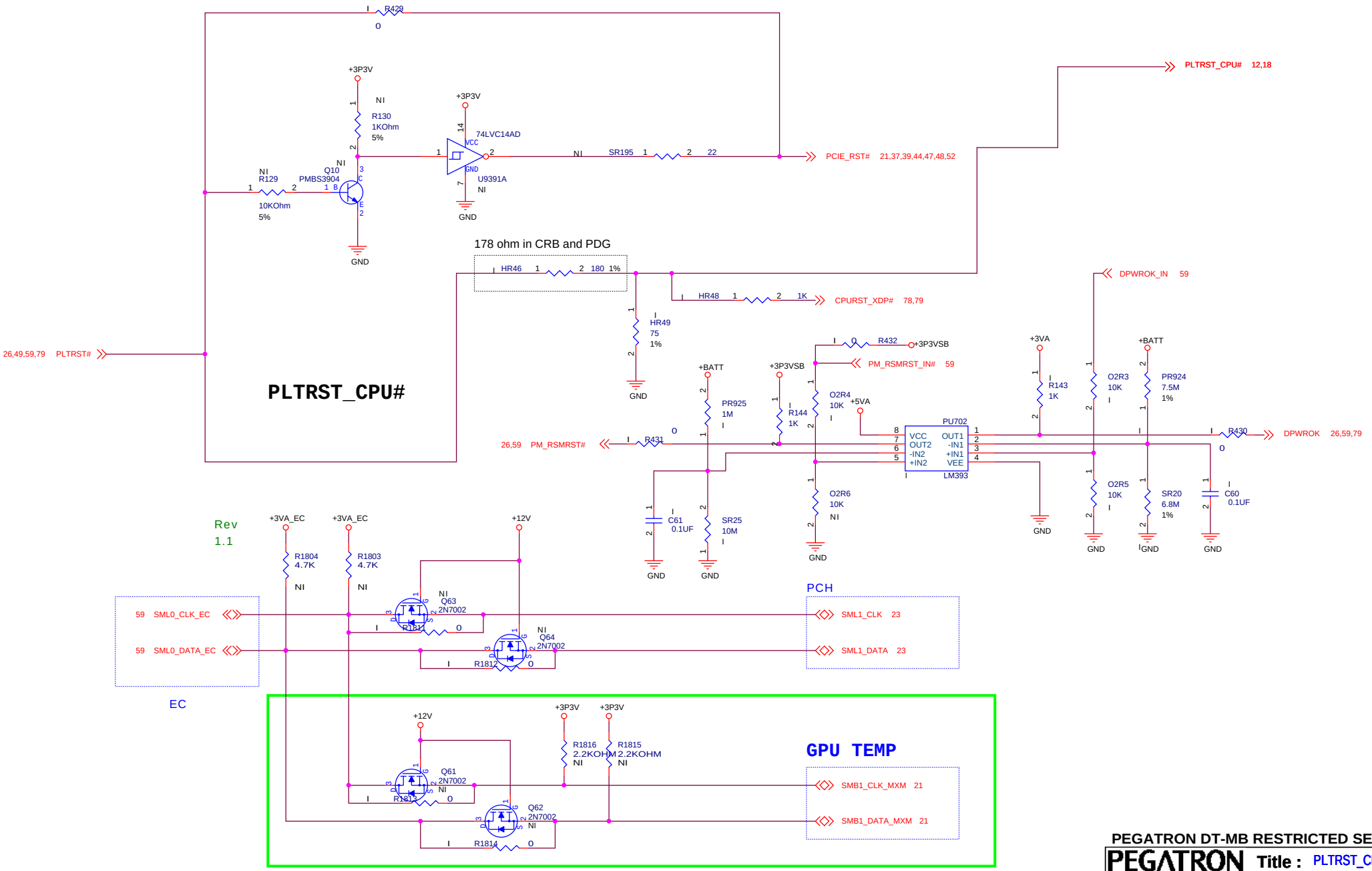
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3 TERMINATION A&B

PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

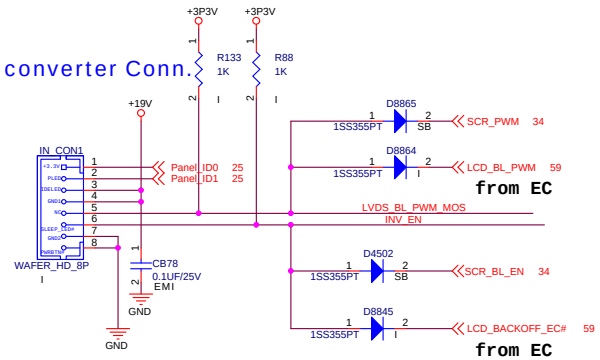
Date: Thursday, April 21, 2011 Sheet 17 of 80

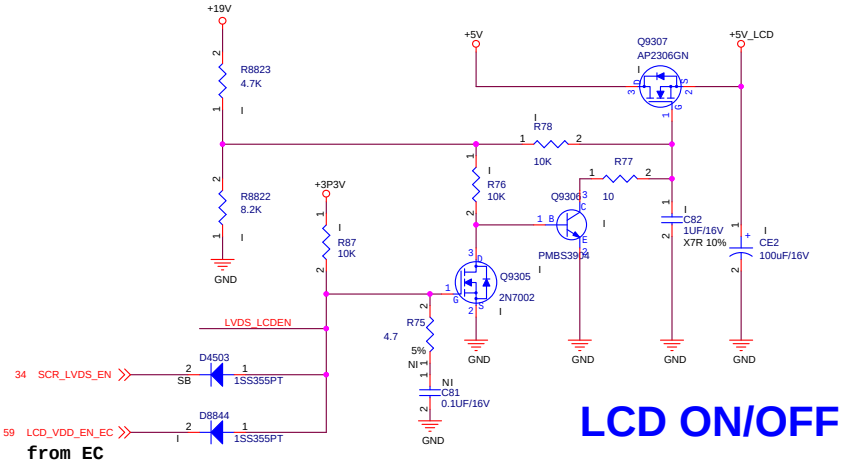


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	PLTRST_CPU#&SMbus
PEGATRON CORPORATION	Engineer:	Ethan_Chen
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Friday, April 22, 2011	Sheet 18 of 80	

PEGATRON	Title : PLTRST_CPU#&SMbus
PEGATRON CORPORATION	Engineer: Ethan_Chen
Size: A	Project Name: IPISB-NK
Rev: 1.03	
Date: Wednesday, April 20, 2011	Sheet 19 of 80





PEGATRON	Title : converter	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: Custom	Project Name: IPISB-NK	Rev: 1.03
Date: Friday, April 22, 2011	Sheet 20 of 80	

typeA NUT

H_MXM1 — TC217BC136D106 — GND

H_MXM2 — TC217BC136D106 — GND

4.5.1. DVI and HDMI Signal Mapping

Table 4-5 details the signal mapping of DP to DVI/HDMI for proper Interface connections.

Table 4-5. DisplayPort to DVI/HDMI Signal Mapping

DisplayPort	DVI/HDMI
DP_x_L0	TX_x_D2
DP_x_L0#	TX_x_D2#
DP_x_L1	TX_x_D1
DP_x_L1#	TX_x_D1#
DP_x_L2	TX_x_D0
DP_x_L2#	TX_x_D0#
DP_x_L3	TX_x_CLK
DP_x_L3#	TX_x_CLK#
DP_x_AUX	DDC_x_CLK
DP_x_AUX#	DDC_x_DATA

MXM1A

DP_A_AUX, DP_A_AUX#, DP_A_HPD, DP_A_L0, DP_A_L0#, DP_A_L1, DP_A_L1#, DP_A_L2, DP_A_L2#, DP_A_L3, DP_A_L3#

DP_B_AUX, DP_B_AUX#, DP_B_HPD, DP_B_L0, DP_B_L0#, DP_B_L1, DP_B_L1#, DP_B_L2, DP_B_L2#, DP_B_L3, DP_B_L3#

DP_C_AUX, DP_C_AUX#, DP_C_HPD, DP_C_L0, DP_C_L0#, DP_C_L1, DP_C_L1#, DP_C_L2, DP_C_L2#, DP_C_L3, DP_C_L3#

DP_D_AUX, DP_D_AUX#, DP_D_HPD, DP_D_L0, DP_D_L0#, DP_D_L1, DP_D_L1#, DP_D_L2, DP_D_L2#, DP_D_L3, DP_D_L3#

DVI_HPD

LVDS_LTX0, LVDS_LTX0#, LVDS_LTX1, LVDS_LTX1#, LVDS_LTX2, LVDS_LTX2#, LVDS_LTX3, LVDS_LTX3#, LVDS_LCLK, LVDS_LCLK#

LVDS_UTX0, LVDS_UTX0#, LVDS_UTX1, LVDS_UTX1#, LVDS_UTX2, LVDS_UTX2#, LVDS_UTX3, LVDS_UTX3#, LVDS_UCLK, LVDS_UCLK#, LVDS_DDC_CLK, LVDS_DDC_DAT

PNL_BL_EN, PNL_BL_PWM, PNL_PWR_EN, PRSNT_L#, PRSNT_R#, PWR_EN, PWR_GOOD, PWR_SRC_1, PWR_SRC_2, PWR_LEVEL, SMB_CLK, SMB_DAT

VGA_BLUE, VGA_RED, VGA_GREEN, VGA_HSYNC, VGA_VSYNC, VGA_DISABLE#, VGA_DDC_DAT, VGA_DDC_CLK

MXM_314P

PEX_TX0 PEX_TX0# PEX_RX0 PEX_RX0# … PEX_TX15 PEX_TX15# PEX_RX15 PEX_RX15#

PEX_REFCLK, PEX_REFCLK#, PEX_RST#, PEX_STD_SW#

TH_PWM, TH_OVERT#, TH_ALERT#, HDMI_CEC, NP_NC1, NP_NC2, SIDE1, SIDE2, GPIO0, GPIO1, GPIO2

MXM1B

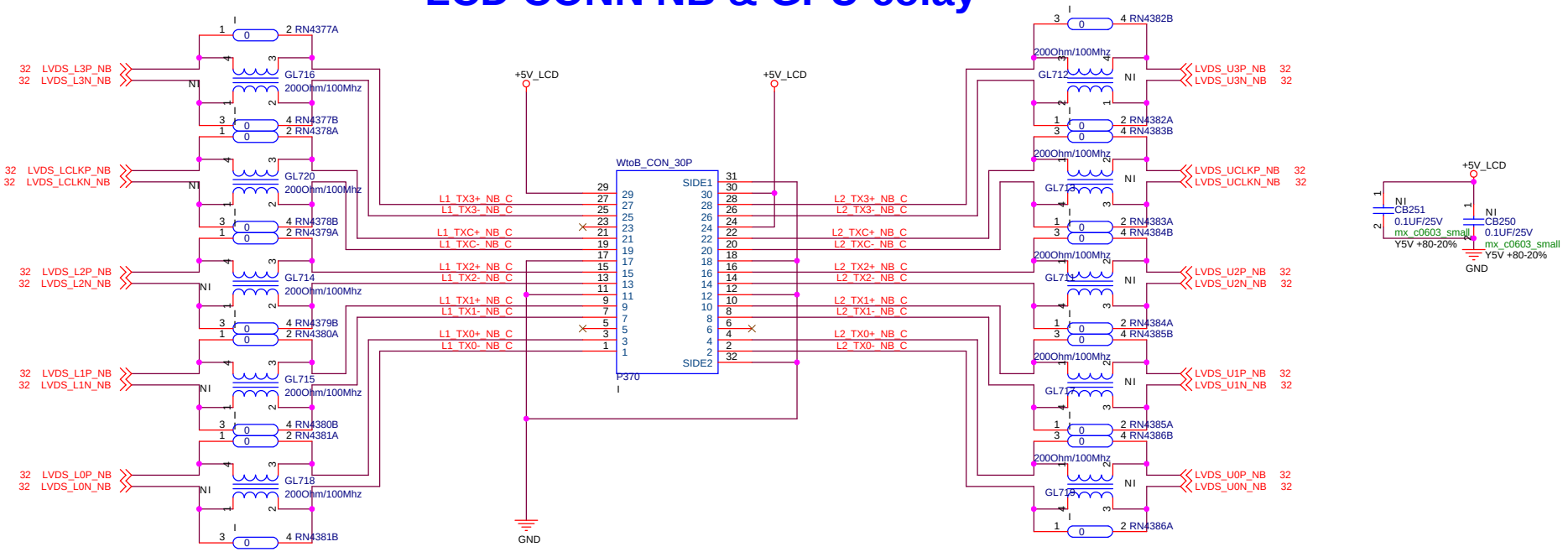
5V_1, 3V3_1, 3V3_2, WAKE#, CLK_REQ#, OEM_1 … OEM_8, RSVD_1 … RSVD_24, GND_1 … GND_93, PWR_SRC_2_1 … PWR_SRC_1_9

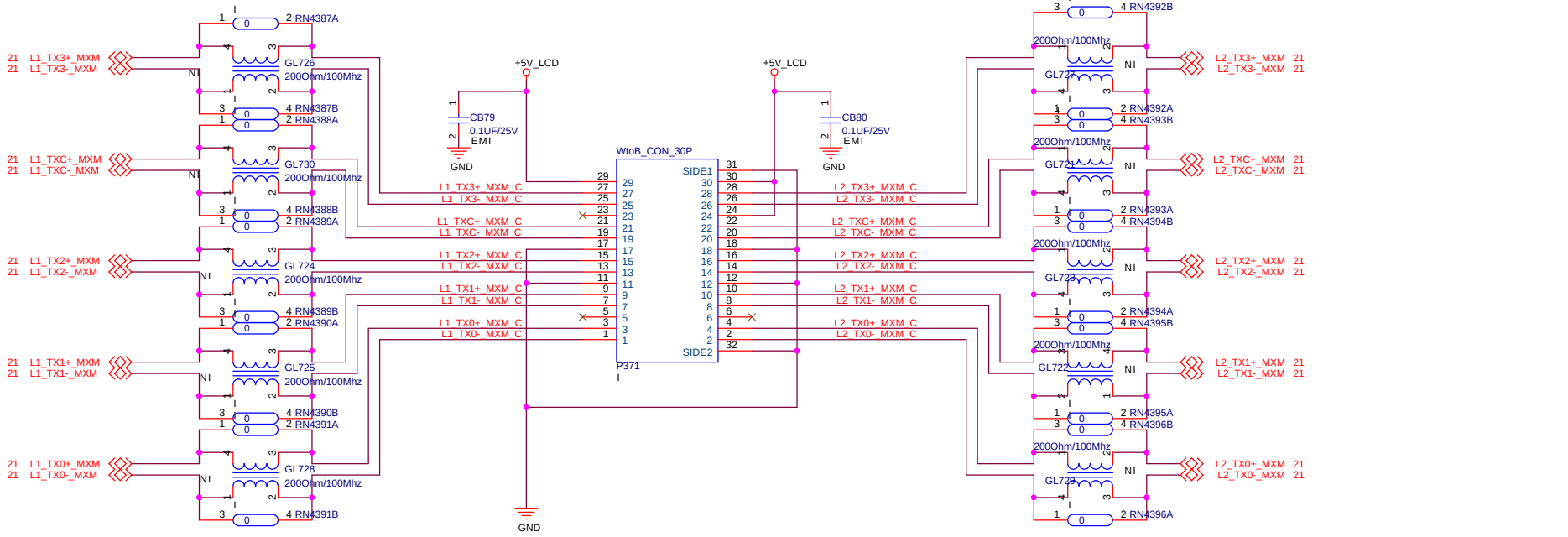
MXM_314P

PEX_STD_SW#:
PCI-Express swing select pin, system must tie to GND to select high (desktop) swing level or float (NC) for low swing.

PEGATRON	Title :	MXM	
PEGATRON CORPORATION	Engineer:	Ethan_Chen	
Size: Custom	Project Name: IPISB-NK		Rev: 1.03
Date: Thursday, April 21, 2011	Sheet 21 of 80		

LCD CONN NB & GPU colay





PEGATRON Title : LVDS CON

PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Thursday, April 21, 2011 Sheet 22 of 80

NOTE: Strapping Options Flash

GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

strapping GPIO, don't use it.

I2C/en(dis)able/S3 for accelerometer

U2A

PCI

SMBUS

RTC

SPI

Rev=1.0

COUGARPOINT

XY5 Crystal Holder

PEGATRON

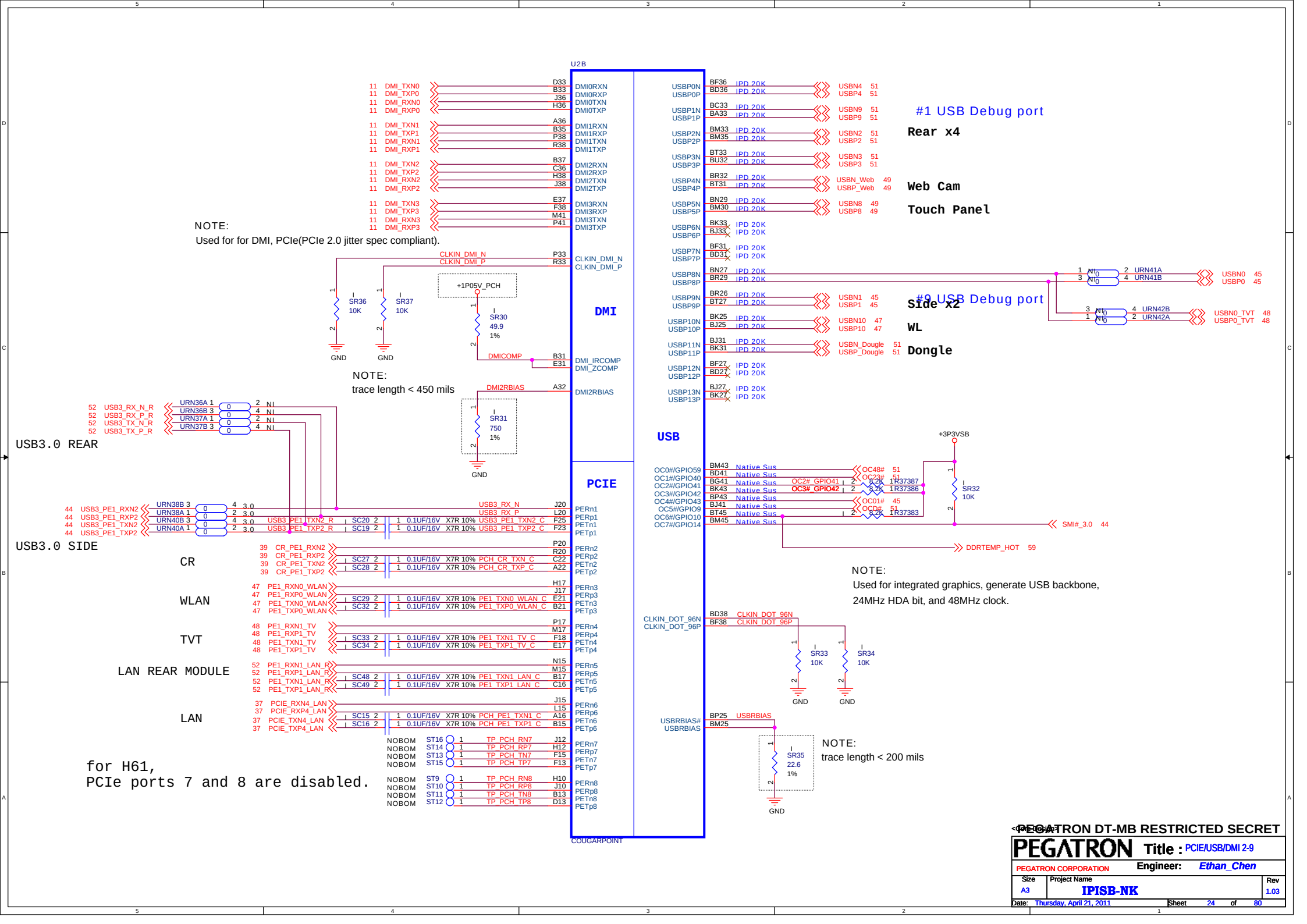
Title : PCI/SM/SPI/RTC 1-9

PEGATRON CORPORATION

Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 23 of 80


U2B
DMI
PCIE
USB
COUGARPOINT
NOTE:
Used for for DMI, PCIe(PCIe 2.0 jitter spec compliant).
NOTE:
trace length < 450 mils
#1 USB Debug port
Rear x4
Web Cam
Touch Panel
#9 USB Debug port
Side x2
WL
Dongle
USB3.0 REAR
USB3.0 SIDE
CR
WLAN
TVT
LAN REAR MODULE
LAN
NOTE:
Used for integrated graphics, generate USB backbone, 24MHz HDA bit, and 48MHz clock.
NOTE:
trace length < 200 mils
for H61,
PCIe ports 7 and 8 are disabled.
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : PCIE/USB/DMI 2-9
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Thursday, April 21, 2011
Sheet 24 of 80

NOTE:

SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT

U2C

CLINK
FAN
GPIO
HOST

CL_CLK1 BA50 (IPU 32/ IPD 100)
CL_DATA1 BF50 (IPU 32/ IPD 100)
CL_RST1# BF49
APWROK BC46 ← 21,26,59 PCH_PWROK
DVT
NI SC30 100PF/50V

PWM0 ← NOBOM ST24 1 TP_PCH_PWM0 BN21
PWM1 ← NOBOM ST25 1 TP_PCH_PWM1 BT21
PWM2 ← NOBOM ST26 1 TP_PCH_PWM2 BM20
PWM3 ← NOBOM ST27 1 TP_PCH_PWM3 BN19
59 DDRTEMP_WARM
20,21,36,46 MXM_PRESENT#
21 MXM_ALERT#
21 MXM_OVERT#

+3P3V
SR45 SR46 SR47 SR48 SR49 SR50 SR51 SR52 10K
REVID

TACH0/GPIO17 BT17 (IPU 20K GPI Core)
TACH1/GPIO1 BR19 (IPU 20K GPI Core)
TACH2/GPIO6 BA22 (IPU 20K GPI Core)
TACH3/GPIO7 BR16 (IPU 20K GPI Core)
TACH4/GPIO68 BU16 (IPU 20K GPI Core)
TACH5/GPIO69 BM18 (IPU 20K GPI Core)
TACH6/GPIO70 BN17 (IPU 20K Native Core)
TACH7/GPIO71 BP15 (IPU 20K Native Core)

SST BC43 (IPD 10K)
NI SC31 220PF/50V X7R 10%
21 MXM_PWR_EN
32 EDPRST
49 LPC_SMI#
DVT NI SR90 10K

GPIO 17/38/39: Board ID.
100: 1.00
101: 1.01
110: 1.02
111: 1.03
0xx: TBD

SCLOCK/GPIO22 BA53 (GPI Core)
SLOAD/GPIO38 BE54 (GPI Core)
SDATAOUT0/GPIO39 BF55 (GPI Core)
SDATAOUT1/GPIO48 AW53 (GPI Core)

CLKIN_SATA_N AF55
CLKIN_SATA_P AG56
CLKIN_SATA_N
CLKIN_SATA_P
SR28 10K SR39 10K

+3P3V
SR55 SR56 SR57 SR58 10K
REVBC
SLOAD_GPIO38
SDATAOUT0/GPIO39
MFG_NET
NOBOM MFG1
GPI1 GPI2 GND NP_NC1 NP_NC2 NP_NC3
PEGATRON_MFG

GPIO 49/22: REV ID.
0: REV B
1: REV C

E20 0 SB
NI SR69 10K
NI SR71 10K

AY20 NC_1

COUGARPOINT

SATA0RXN AC56 SATA_RXN0 33
SATA0RXP AB55 SATA_RXP0 33
SATA0TXN AE46 SATA_TXN0 33
SATA0TXP AE44 SATA_TXP0 33
SATA1RXN AA53 SATA_RXN1 33
SATA1RXP AA56 SATA_RXP1 33
SATA1TXN AG49 SATA_TXN1 33
SATA1TXP AG47 SATA_TXP1 33
SATA2RXN AL50
SATA2RXP AL49
SATA2TXN AL56
SATA2TXP AL53
SATA3RXN AN46
SATA3RXP AN44
SATA3TXN AN56
SATA3TXP AM55
SATA4RXN AN49
SATA4RXP AN50
SATA4TXN AT50
SATA4TXP AT49
SATA5RXN AT46
SATA5RXP AT44
SATA5TXN AV50
SATA5TXP AV49

NOTE: Strapping Options Flash

GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI

SATA0GP/GPIO21 BC54 (GPI Core)
SATA1GP/GPIO19 AY52 (GPI Core IPU 20K) SATA1GP_GPIO19
SATA2GP/GPIO36 BB55 (GPI Core IPD 20K) SATA2GP_GPIO36
SATA3GP/GPIO37 BG53 (GPI Core IPD 20K) SATA3GP_GPIO37
SATA4GP/GPIO16 AU56 (GPI Core)
SATA5GP/GPIO49 BA56 (GPI Core) SATA5GP_GPIO49

Panel_ID0 → Panel_ID0 20
10K SR60 SR61 SR62 SR63 SR64 SR65 (NI)
+3P3V
Panel_ID1 → Panel_ID1 20

NOTE: trace length < 450 mils
+1P05V_PCH SR66 37.4 1%
+1P05V_PCH SR67 49.9 1%
SR138 10K
SR298 10K
DVT NI SR89 10K
+3P3V SR68 10K

SATAICOMPI AJ55
SATAICOMPO AJ53 SATAICOMP
SATA3COMPI AE54
SATA3RCOMPO AE52 SATA3COMP
NOTE: trace length < 200 mils

SATALED# BF57 OD → HD_LED# 54

TP16 AE50
SATA3RBIAS AC52 SATA3RBIAS
SR70 750 1%
NOTE: trace length < 450 mils

+3P3V SR74 10K
+3P3V SR72 10K
+3P3V SR73 10K

BB57 → A20GATE 59
BN56 IPU 20K INIT3_3V# → RST_KB# 59
BG56 → SERIRQ 49,59
AV52 → H_THMTRIP# 12
E56 → PECI_PCH 12
H48 IPD 0.35K → PM_SYNC 12
F55

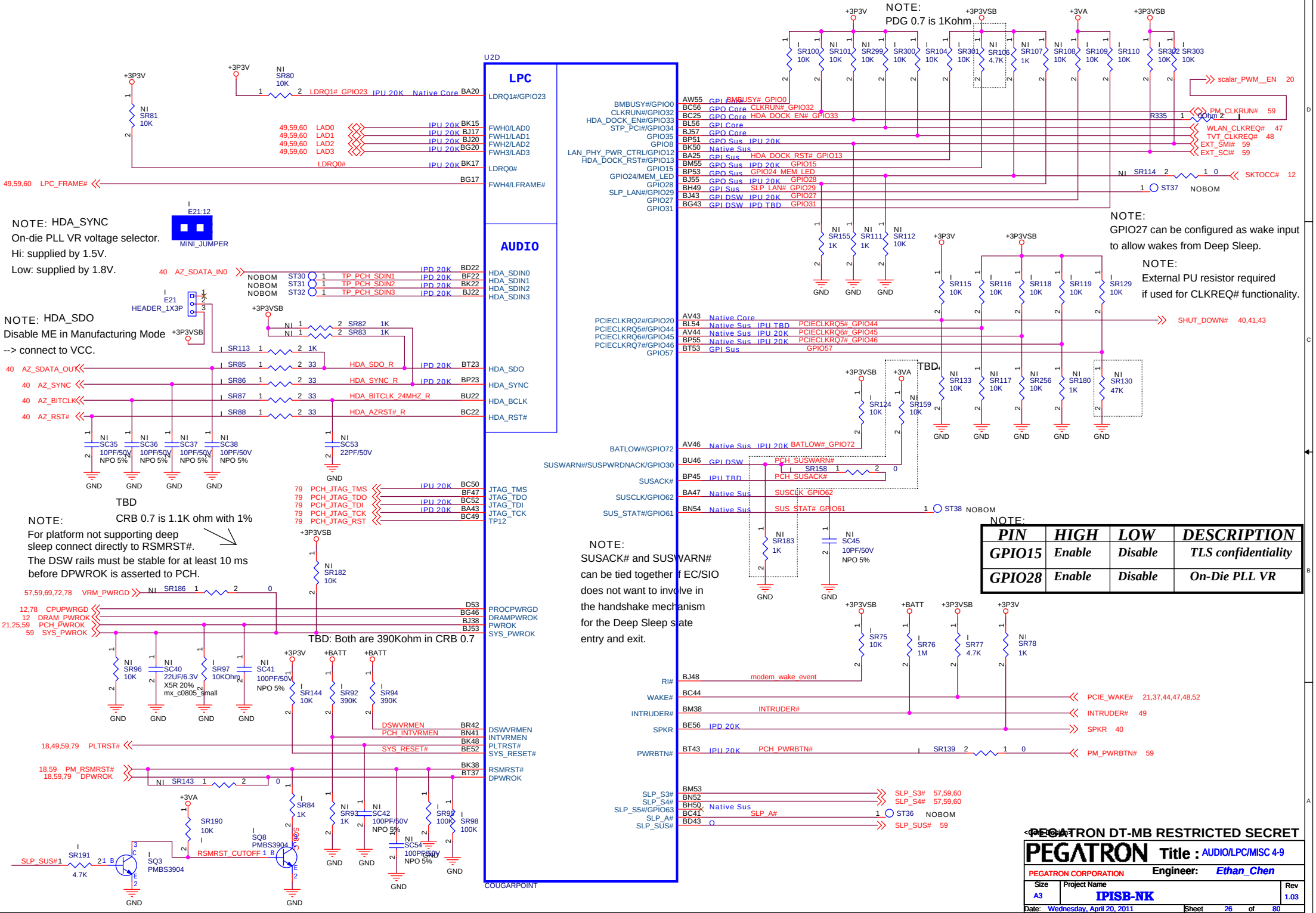
A20GATE
INIT3_3V#
RCIN#
SERIRQ
THRMTRIP#
PECI
PMSYNCH

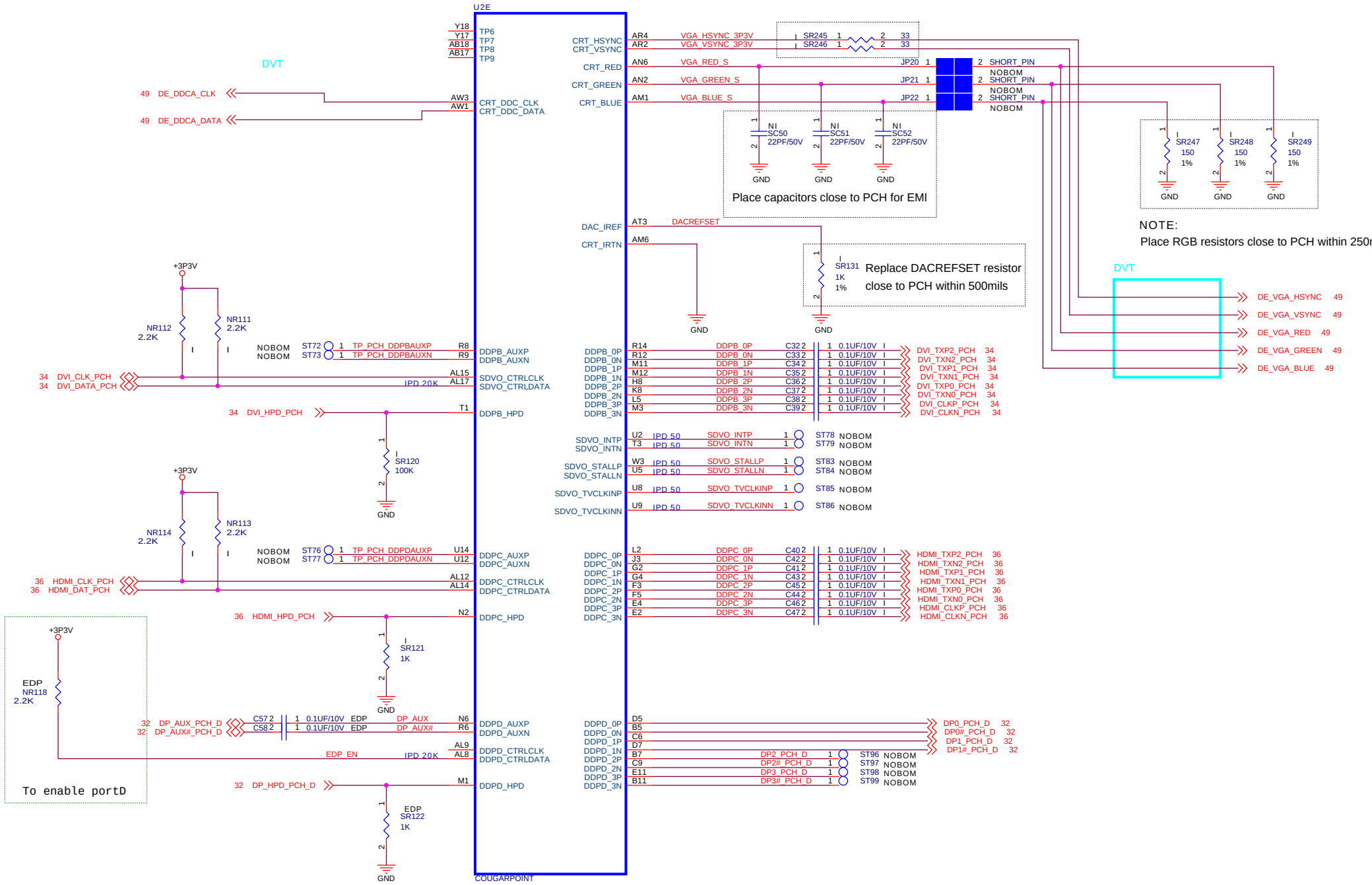
NI SR79 1K

<Core Design>

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SATA/HOST/FAN 3-9
PEGATRON CORPORATION Engineer: Ethan_Chen
Size A3 | Project Name IPISB-NK | Rev 1.03
Date: Wednesday, April 20, 2011 | Sheet 25 of 80


U2D
LPC
AUDIO
COUGARPOINT
NOTE: HDA_SYNC
On-die PLL VR voltage selector.
Hi: supplied by 1.5V.
Low: supplied by 1.8V.
NOTE: HDA_SDO
Disable ME in Manufacturing Mode
--> connect to VCC.
TBD
CRB 0.7 is 1.1K ohm with 1%
NOTE:
For platform not supporting deep sleep connect directly to RSMRST#.
The DSW rails must be stable for at least 10 ms before DPWROK is asserted to PCH.
TBD: Both are 390Kohm in CRB 0.7
NOTE:
PDG 0.7 is 1Kohm
NOTE:
SUSACK# and SUSWARN# can be tied together f EC/SIO does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.
NOTE:
GPIO27 can be configured as wake input to allow wakes from Deep Sleep.
NOTE:
External PU resistor required if used for CLKREQ# functionality.
PIN | HIGH | LOW | DESCRIPTION
GPIO15 | Enable | Disable | TLS confidentiality
GPIO28 | Enable | Disable | On-Die PLL VR
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : AUDIO/LPC/MISC 4-9
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Wednesday, April 20, 2011
Sheet 26 of 80



PEGATRON

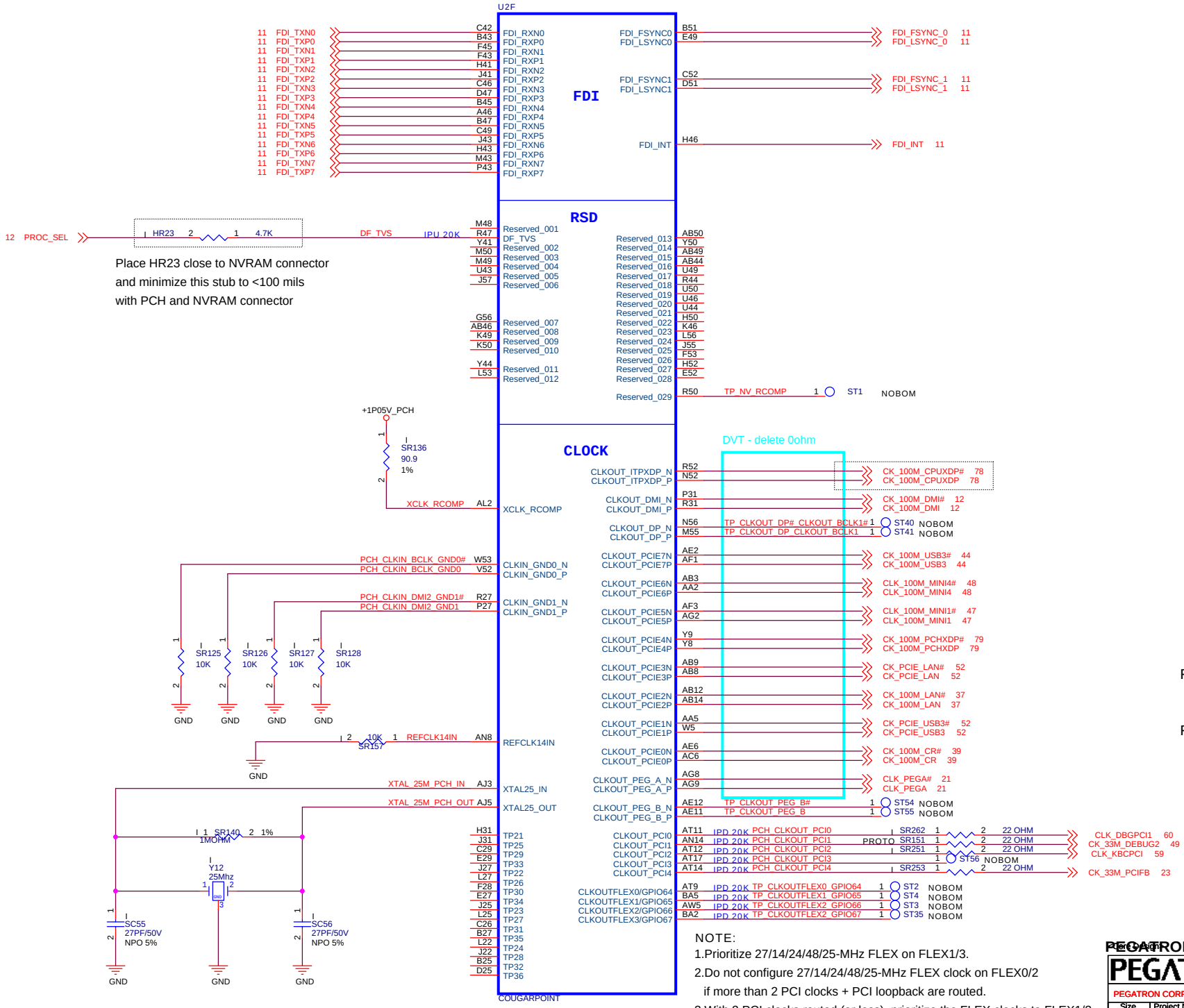
Title : VGA/DP/HDMI 5-9

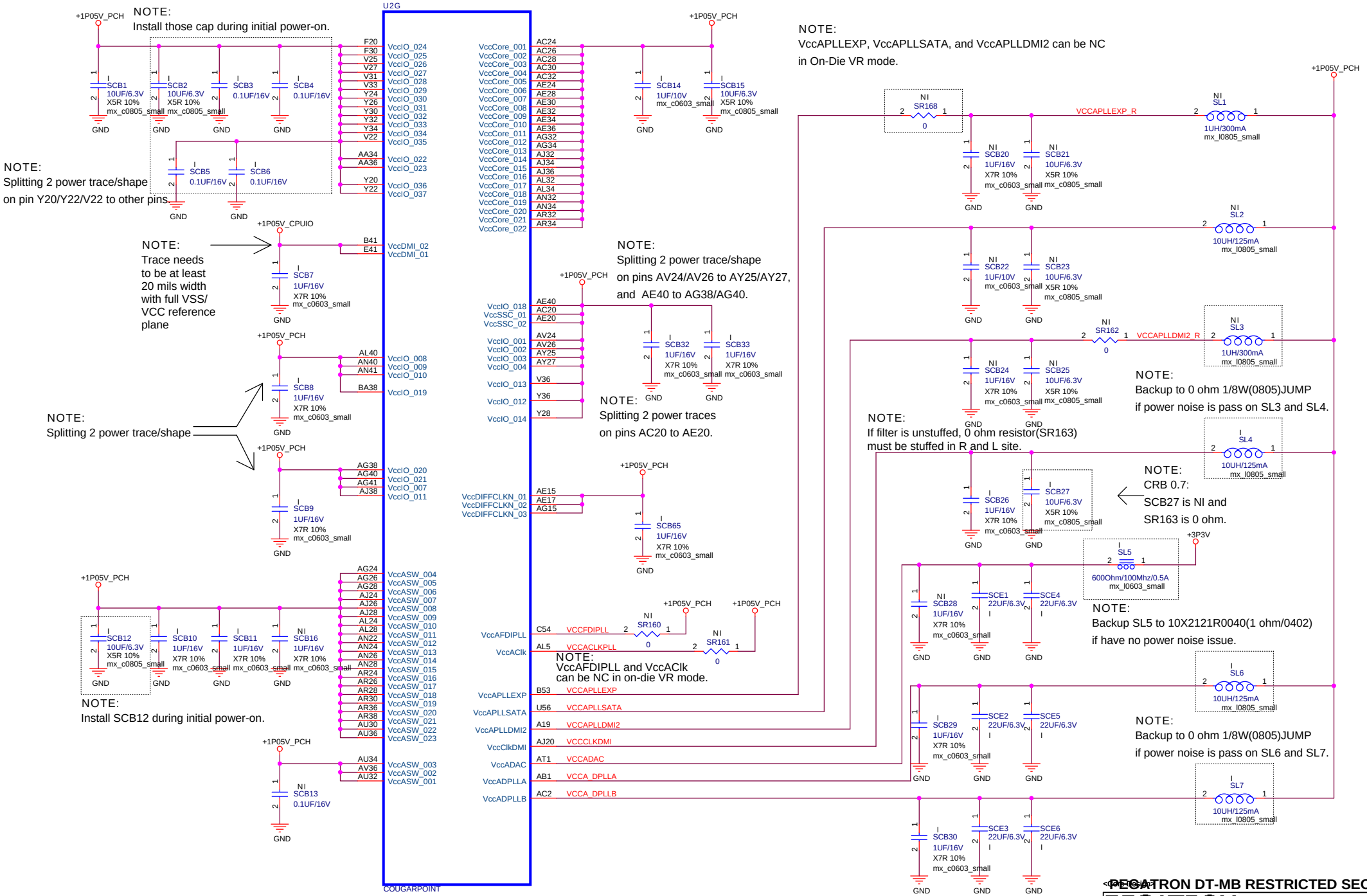
PEGATRON CORPORATION

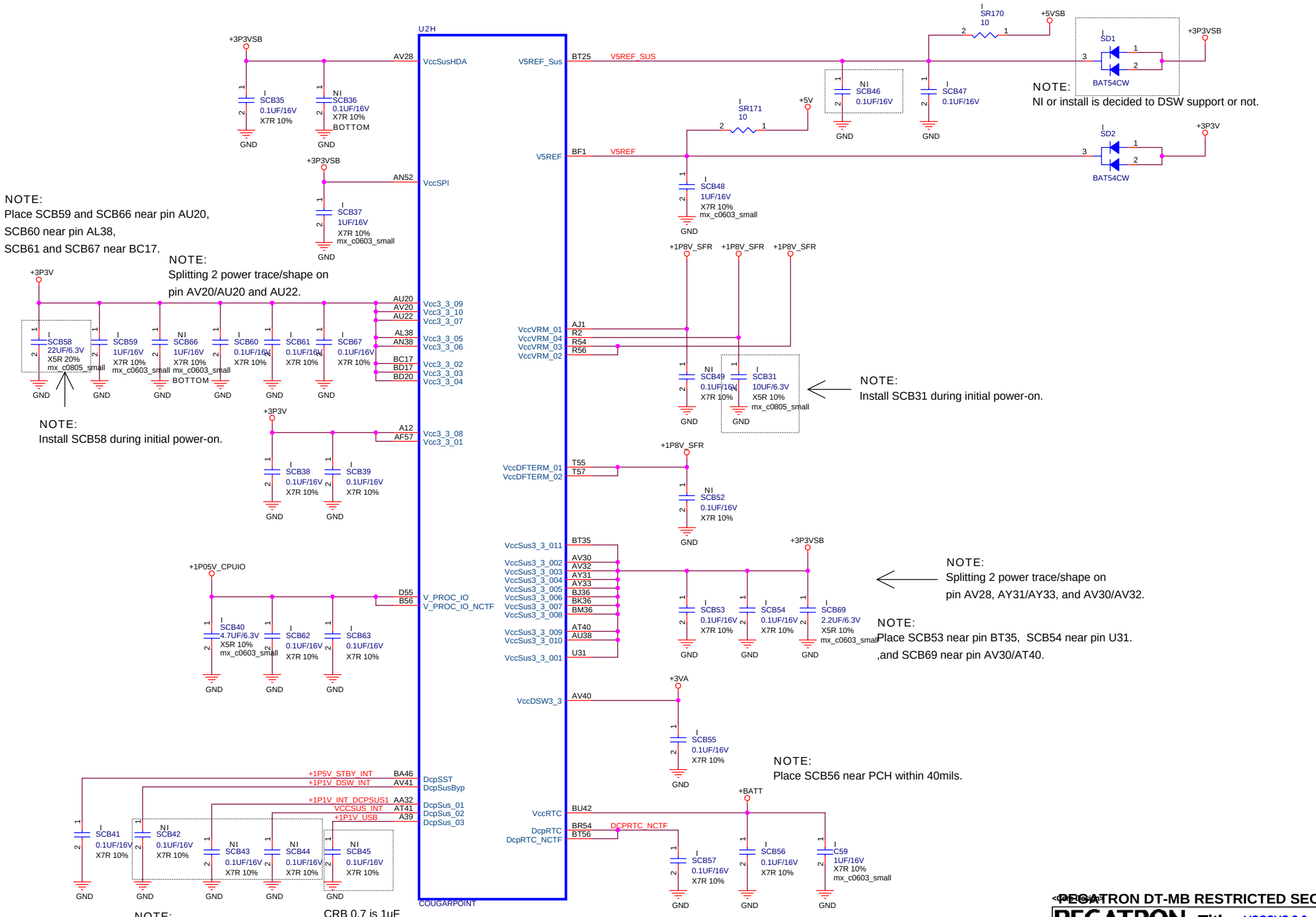
Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 27 of 80


U2F
FDI
RSD
CLOCK
COUGARPOINT
FDI_TXN0
FDI_TXP0
FDI_TXN1
FDI_TXP1
FDI_TXN2
FDI_TXP2
FDI_TXN3
FDI_TXP3
FDI_TXN4
FDI_TXP4
FDI_TXN5
FDI_TXP5
FDI_TXN6
FDI_TXP6
FDI_TXN7
FDI_TXP7
FDI_RXN0
FDI_RXP0
FDI_RXN1
FDI_RXP1
FDI_RXN2
FDI_RXP2
FDI_RXN3
FDI_RXP3
FDI_RXN4
FDI_RXP4
FDI_RXN5
FDI_RXP5
FDI_RXN6
FDI_RXP6
FDI_RXN7
FDI_RXP7
FDI_FSYNC0
FDI_LSYNC0
FDI_FSYNC1
FDI_LSYNC1
FDI_INT
FDI_FSYNC_0
FDI_LSYNC_0
FDI_FSYNC_1
FDI_LSYNC_1
FDI_INT
PROC_SEL
HR23
4.7K
DF_TVS
IPU 20K
Reserved_001
Reserved_002
Reserved_003
Reserved_004
Reserved_005
Reserved_006
Reserved_007
Reserved_008
Reserved_009
Reserved_010
Reserved_011
Reserved_012
Reserved_013
Reserved_014
Reserved_015
Reserved_016
Reserved_017
Reserved_018
Reserved_019
Reserved_020
Reserved_021
Reserved_022
Reserved_023
Reserved_024
Reserved_025
Reserved_026
Reserved_027
Reserved_028
Reserved_029
TP_NV_RCOMP
ST1
NOBOM
Place HR23 close to NVRAM connector
and minimize this stub to <100 mils
with PCH and NVRAM connector
+1P05V_PCH
SR136
90.9
1%
XCLK_RCOMP
DVT - delete 0ohm
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE0N
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
CLKOUT_PCI0
CLKOUT_PCI1
CLKOUT_PCI2
CLKOUT_PCI3
CLKOUT_PCI4
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CK_100M_CPUXDP#
CK_100M_CPUXDP
CK_100M_DMI#
CK_100M_DMI
TP_CLKOUT_DP#_CLKOUT_BCLK1#
TP_CLKOUT_DP_CLKOUT_BCLK1
ST40
ST41
CK_100M_USB3#
CK_100M_USB3
CLK_100M_MINI4#
CLK_100M_MINI4
CLK_100M_MINI1#
CLK_100M_MINI1
CK_100M_PCHXDP#
CK_100M_PCHXDP
CK_PCIE_LAN#
CK_PCIE_LAN
CK_100M_LAN#
CK_100M_LAN
CK_PCIE_USB3#
CK_PCIE_USB3
CK_100M_CR#
CK_100M_CR
CLK_PEGA#
CLK_PEGA
TP_CLKOUT_PEG_B#
TP_CLKOUT_PEG_B
ST54
ST55
PCH_CLKOUT_PCI0
PCH_CLKOUT_PCI1
PCH_CLKOUT_PCI2
PCH_CLKOUT_PCI3
PCH_CLKOUT_PCI4
PROTO
SR262
SR151
SR251
SR253
22 OHM
CLK_DBGPCI1
CK_33M_DEBUG2
CLK_KBCPCI
CK_33M_PCIFB
ST56
TP_CLKOUTFLEX0_GPIO64
TP_CLKOUTFLEX1_GPIO65
TP_CLKOUTFLEX2_GPIO66
TP_CLKOUTFLEX2_GPIO67
ST2
ST4
ST3
ST35
PCH_CLKIN_BCLK_GND0#
PCH_CLKIN_BCLK_GND0
PCH_CLKIN_DMI2_GND1#
PCH_CLKIN_DMI2_GND1
CLKIN_GND0_N
CLKIN_GND0_P
CLKIN_GND1_N
CLKIN_GND1_P
SR125
SR126
SR127
SR128
10K
GND
SR157
REFCLK14IN
XTAL_25M_PCH_IN
XTAL_25M_PCH_OUT
XTAL25_IN
XTAL25_OUT
SR140
1MOHM
Y12
25Mhz
SC55
SC56
27PF/50V
NPO 5%
TP21
TP25
TP29
TP33
TP22
TP26
TP30
TP34
TP23
TP27
TP31
TP35
TP24
TP28
TP32
TP36
FRO REAR I/O MODULE, LAN
FRO REAR I/O MODULE, USB3.0
NOTE:
1.Prioritize 27/14/24/48/25-MHz FLEX on FLEX1/3.
2.Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0/2
if more than 2 PCI clocks + PCI loopback are routed.
3.With 2 PCI clocks routed (or less), prioritize the FLEX clocks to FLEX1/3
a. 27MHz(SSC/non-SSC) b.14.31818MHz c.24/48 d.25MHz
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : CLK/NVRAM/FDI 6-9
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Wednesday, April 20, 2011
Sheet 28 of 80


U2G
NOTE:
Install those cap during initial power-on.
NOTE:
Splitting 2 power trace/shape
on pin Y20/Y22/V22 to other pins.
NOTE:
Trace needs
to be at least
20 mils width
with full VSS/
VCC reference
plane
NOTE:
Splitting 2 power trace/shape
NOTE:
Install SCB12 during initial power-on.
NOTE:
Splitting 2 power trace/shape
on pins AV24/AV26 to AY25/AY27,
and AE40 to AG38/AG40.
NOTE:
Splitting 2 power traces
on pins AC20 to AE20.
NOTE:
VccAFDIPLL and VccAClk
can be NC in on-die VR mode.
NOTE:
VccAPLLEXP, VccAPLLSATA, and VccAPLLDMI2 can be NC
in On-Die VR mode.
NOTE:
If filter is unstuffed, 0 ohm resistor(SR163)
must be stuffed in R and L site.
NOTE:
Backup to 0 ohm 1/8W(0805)JUMP
if power noise is pass on SL3 and SL4.
NOTE:
CRB 0.7:
SCB27 is NI and
SR163 is 0 ohm.
NOTE:
Backup SL5 to 10X2121R0040(1 ohm/0402)
if have no power noise issue.
NOTE:
Backup to 0 ohm 1/8W(0805)JUMP
if power noise is pass on SL6 and SL7.
COUGARPOINT
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : VCC/PLL 7-9
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Wednesday, April 20, 2011
Sheet 29 of 80

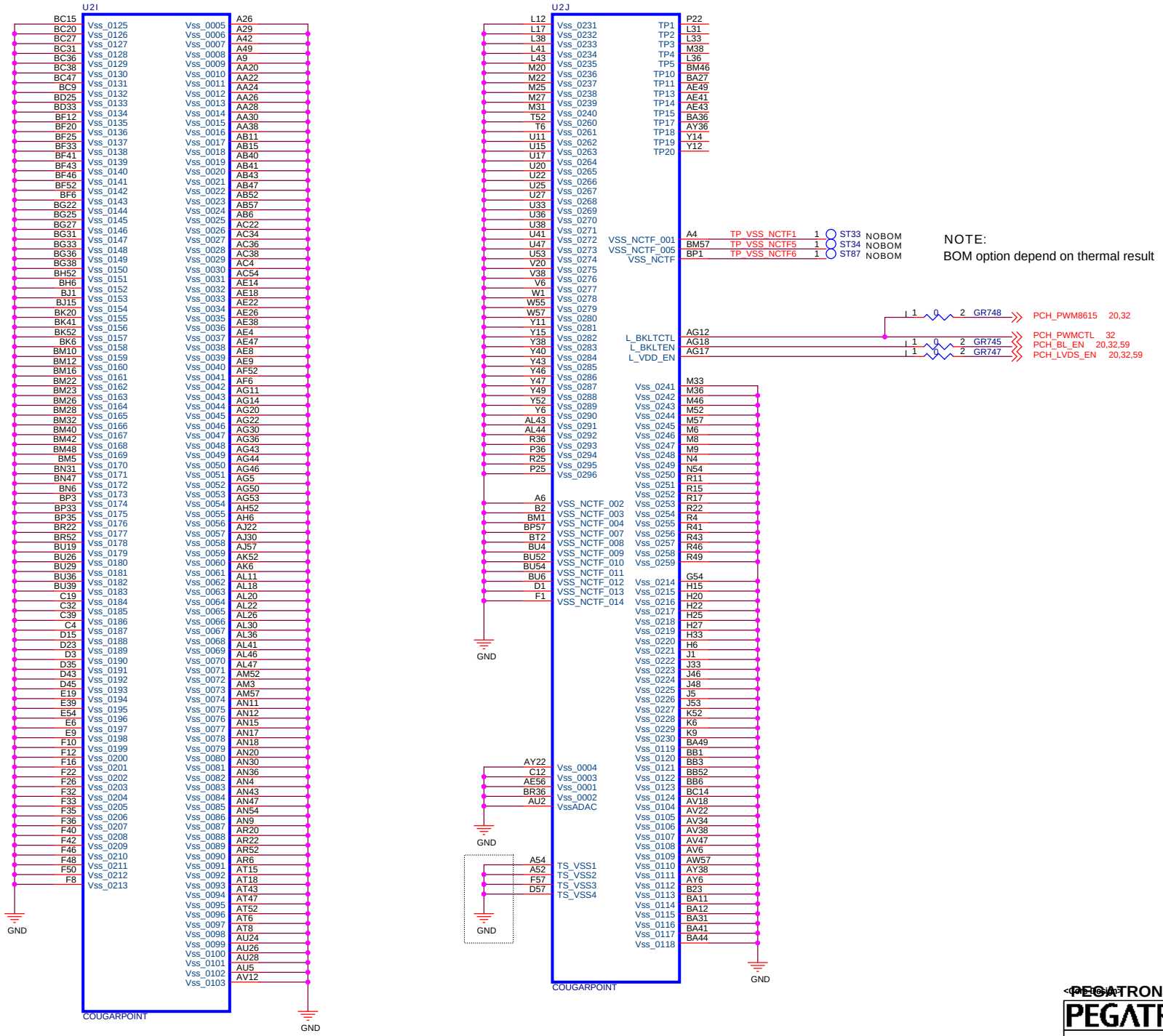


PEGATRON Title : VCCSUS 8-9

PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 30 of 80

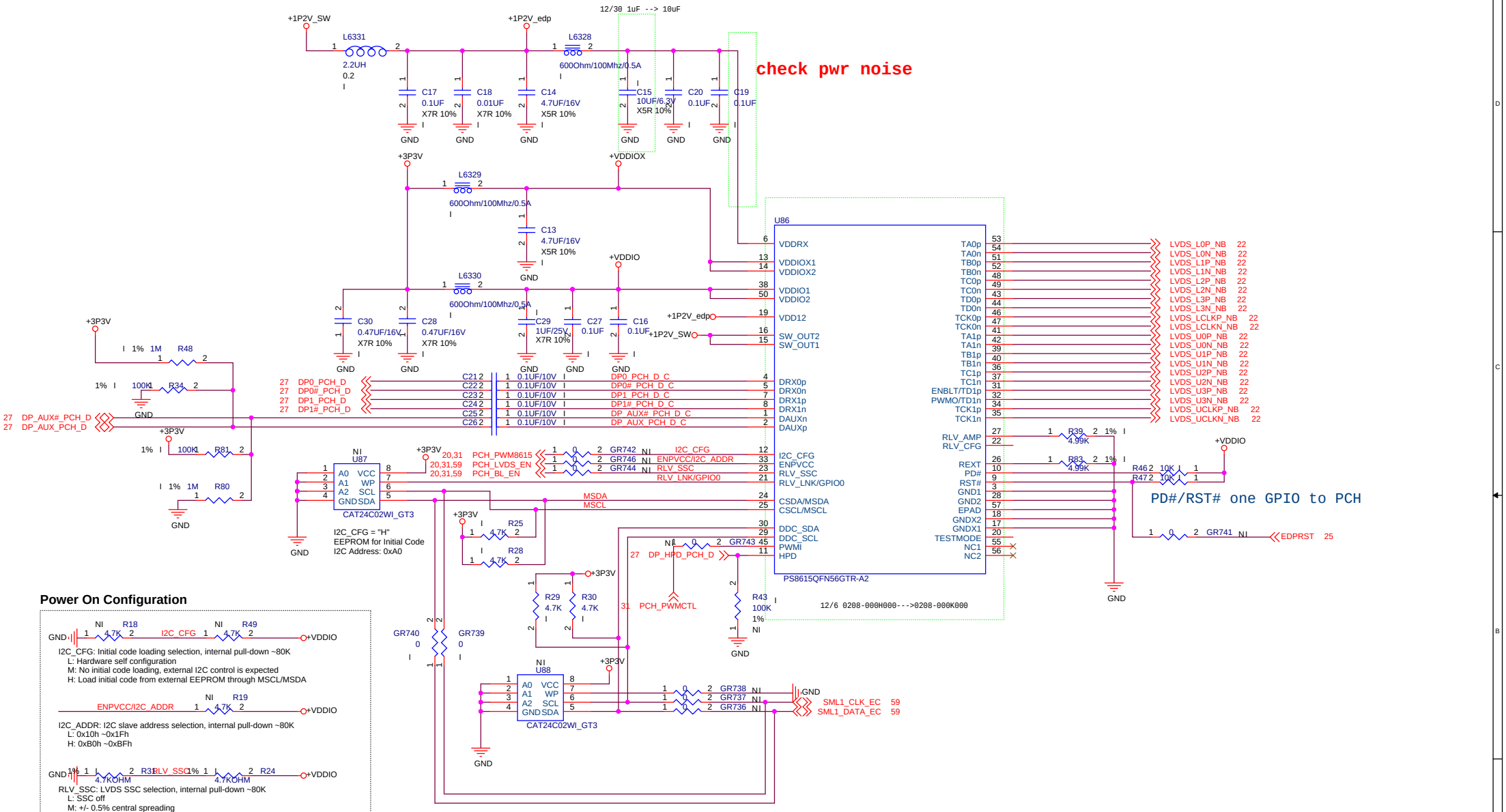


PEGATRON Title : VSS 9-9

PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 31 of 80



Power On Configuration

R18 4.7K I2C_CFG R49 4.7K +VDDIO

I2C_CFG: Initial code loading selection, internal pull-down ~80K
- L: Hardware self configuration
- M: No initial code loading, external I2C control is expected
- H: Load initial code from external EEPROM through MSCL/MSDA

ENPVCC/I2C_ADDR R19 4.7K +VDDIO

I2C_ADDR: I2C slave address selection, internal pull-down ~80K
- L: 0x10h ~0x1Fh
- H: 0xB0h ~0xBFh

R31 4.7KOHM RLV_SSC R24 4.7KOHM +VDDIO

RLV_SSC: LVDS SSC selection, internal pull-down ~80K
- L: SSC off
- M: +/- 0.5% central spreading
- H: +/- 1% central spreading

R36 4.7K RLV_CFG R84 4.7K +VDDIO

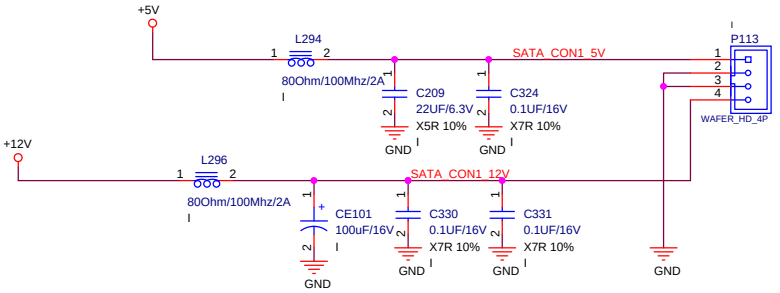
RLV_CFG: LVDS color depth and data mapping selection, internal pull-down ~80K
- L: 8-bit LVDS, VESA mapping
- M: 8-bit LVDS, JEIDA mapping
- H: 6-bit LVDS, both VESA and JEIDA mapping

RLV_LNK/GPIO0 R37 4.7K +VDDIO

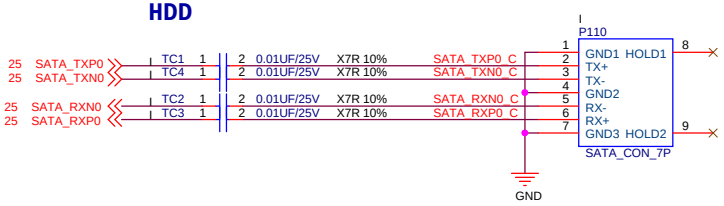
RLV_LNK: LVDS single link or dual link selection, internal pull-down ~80K
- L: Single link LVDS
- H: Dual link LVDS

PEGATRON	Title : PS8615	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Thursday, April 21, 2011	Sheet 32 of 80	

SATA CONNECTOR

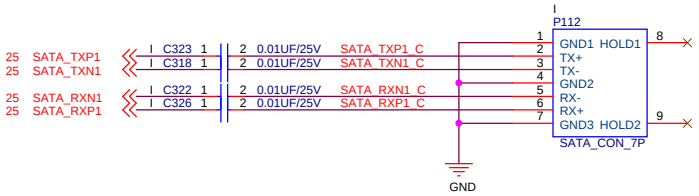


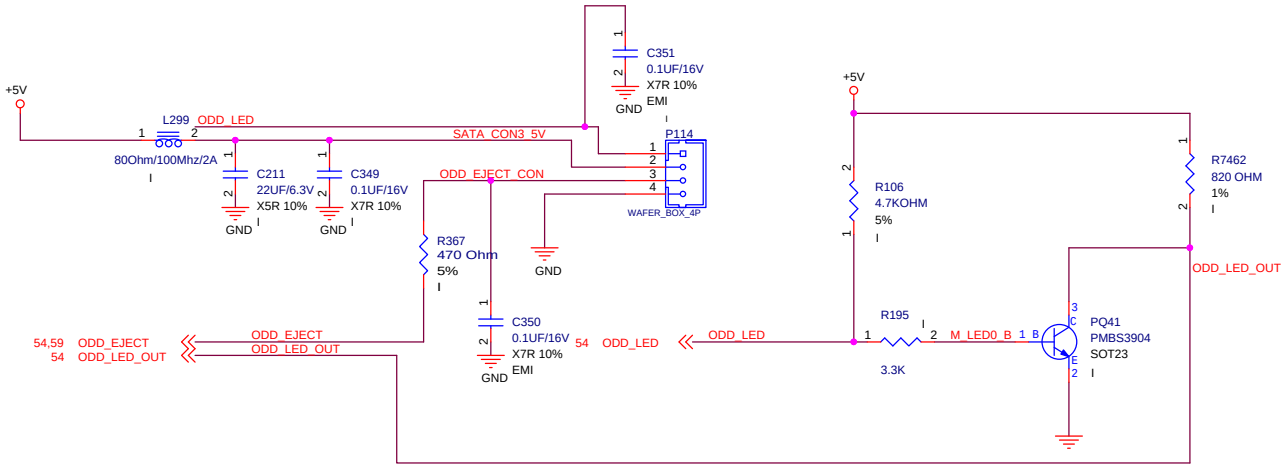
CHANNEL 0 MASTER
Dark Blue
HDD



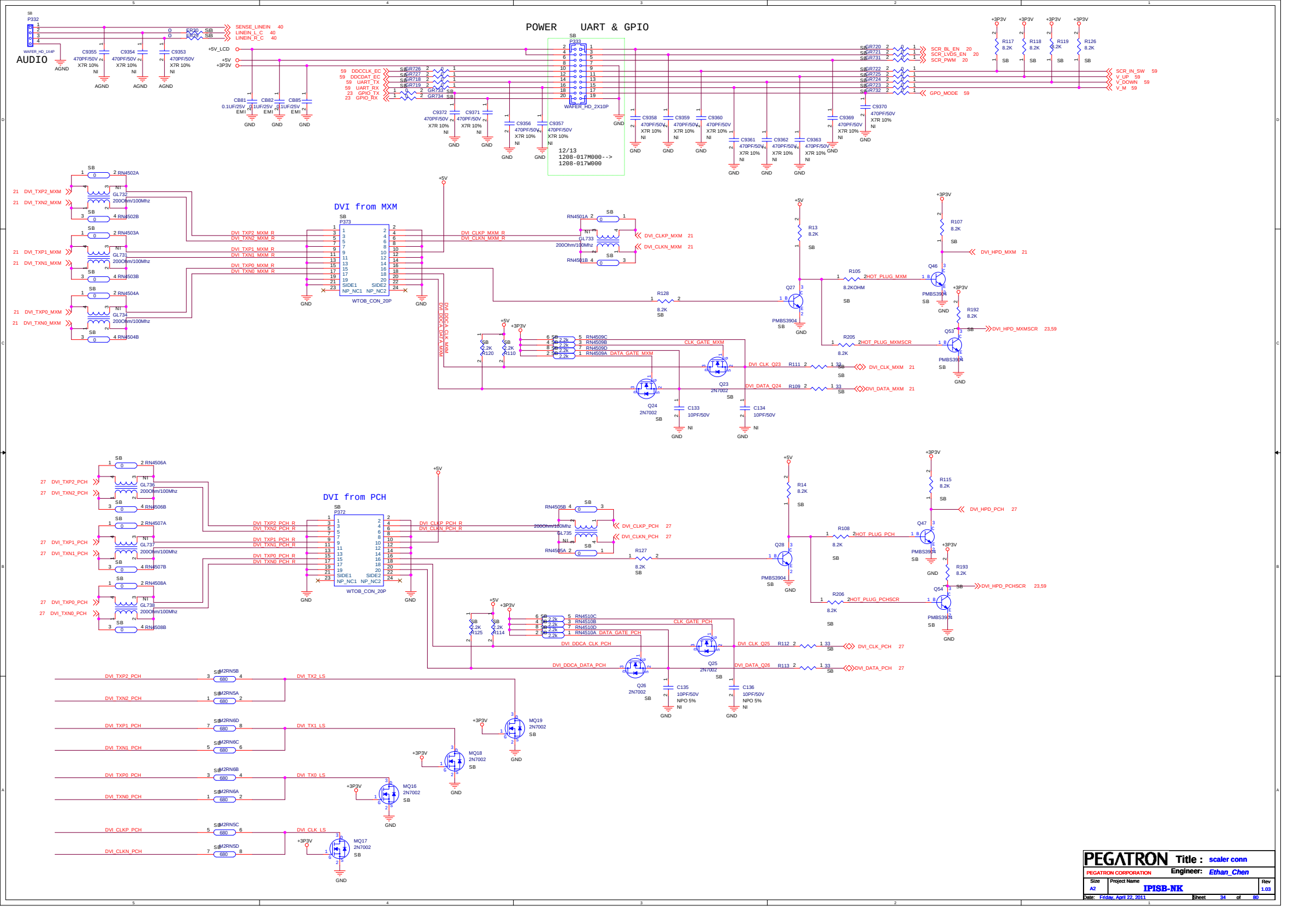
CHANNEL 1 MASTER
White

ODD





PEGATRON	Title : SATA		
PEGATRON CORPORATION	Engineer: Ethan_Chen		
Size: A3	Project Name: IPISB-NK		Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 33 of 80		


POWER UART & GPIO
AUDIO
DVI from MXM
DVI from PCH
WTOB_CON_20P
WAFER_HD_2X10P
12/13
1208-017M000-->
1208-017W000
PEGATRON
Title : scaler conn
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size A2
Project Name IPISB-NK
Rev 1.03
Date: Friday, April 22, 2011
Sheet 34 of 80

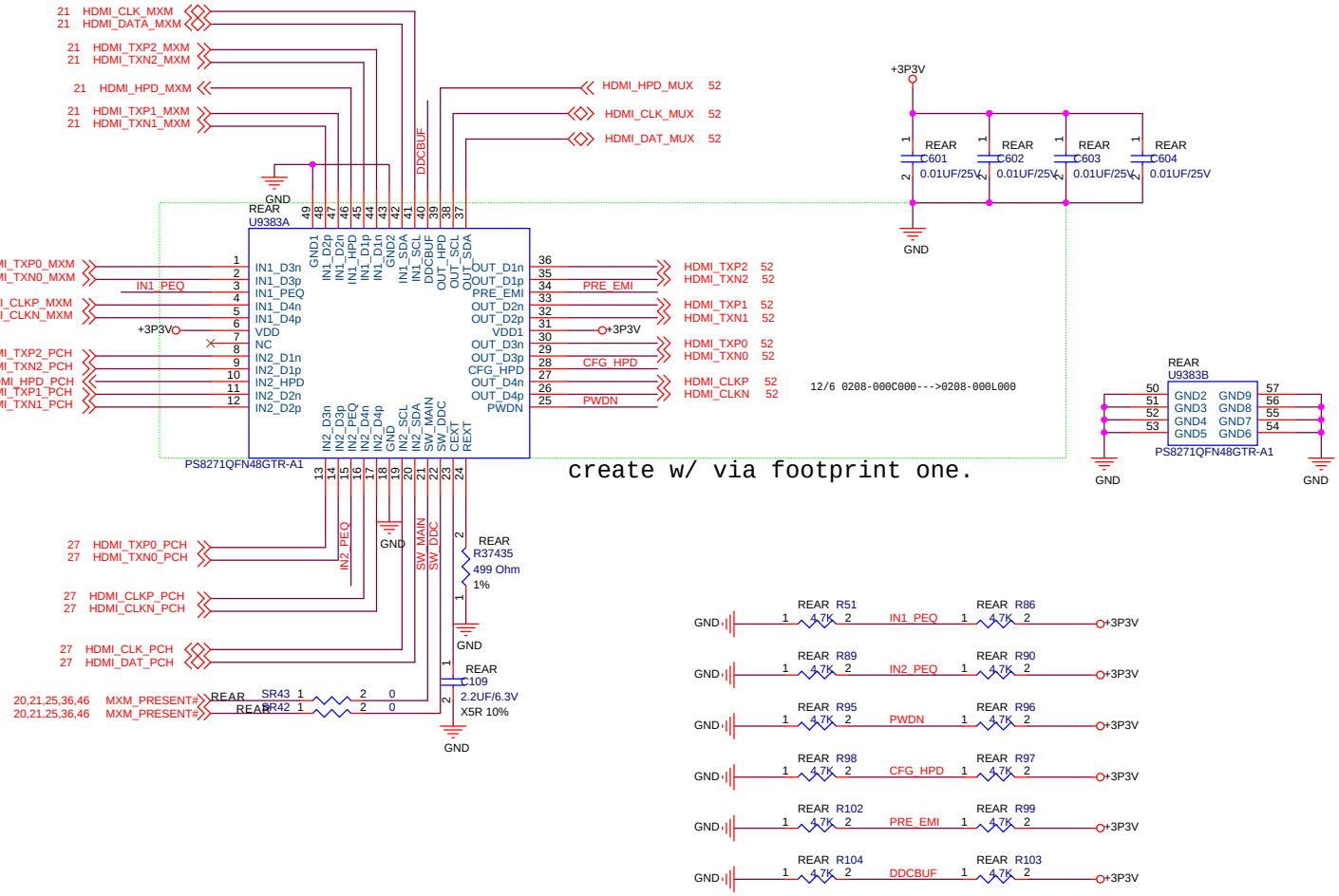
<Core Design>

PEGATRON Title : N/A

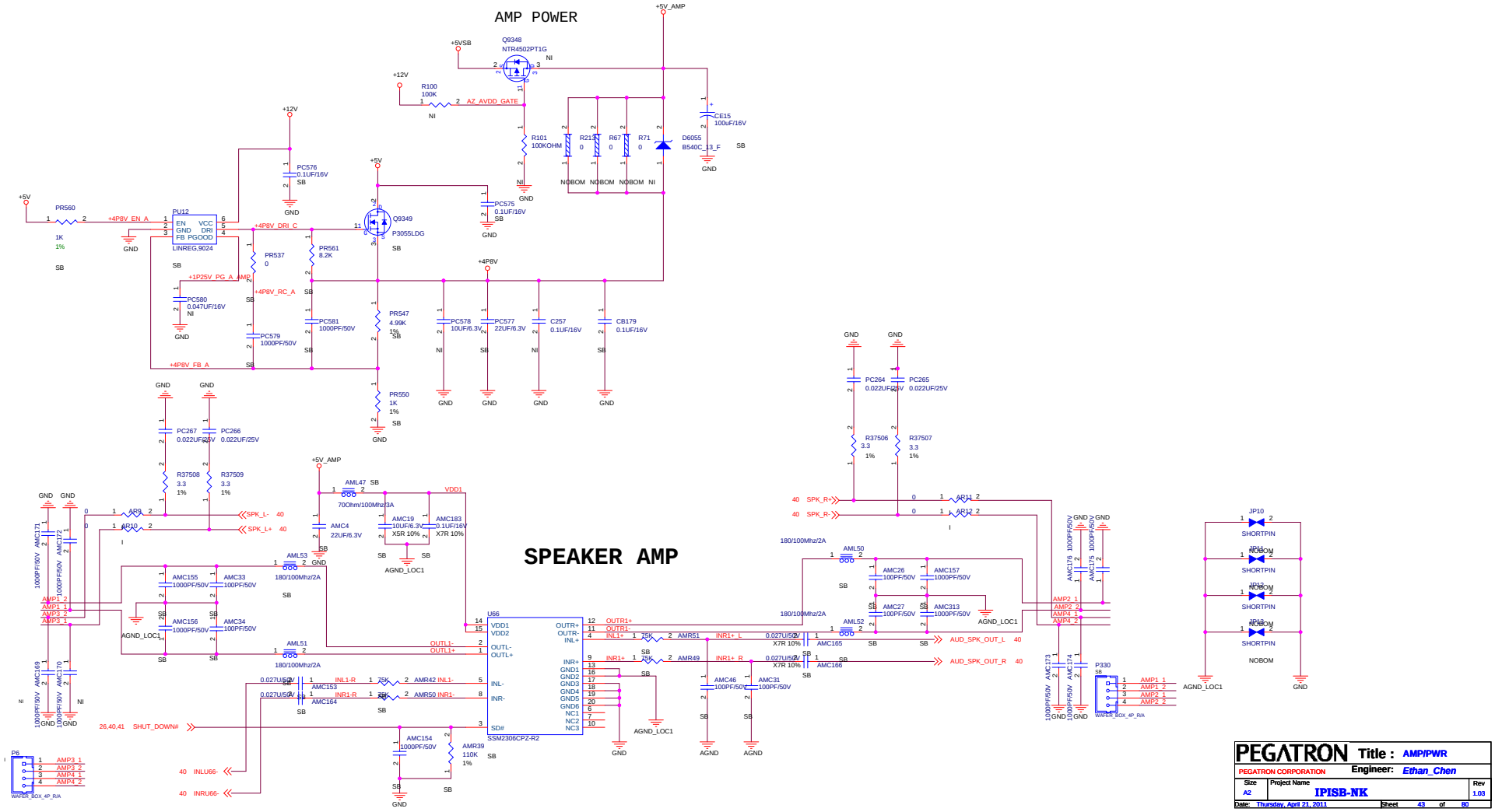
Pegatron Corp. Engineer: Ethan_Chen

Size	Project Name	Rev
C	IPISB-NK	1.03

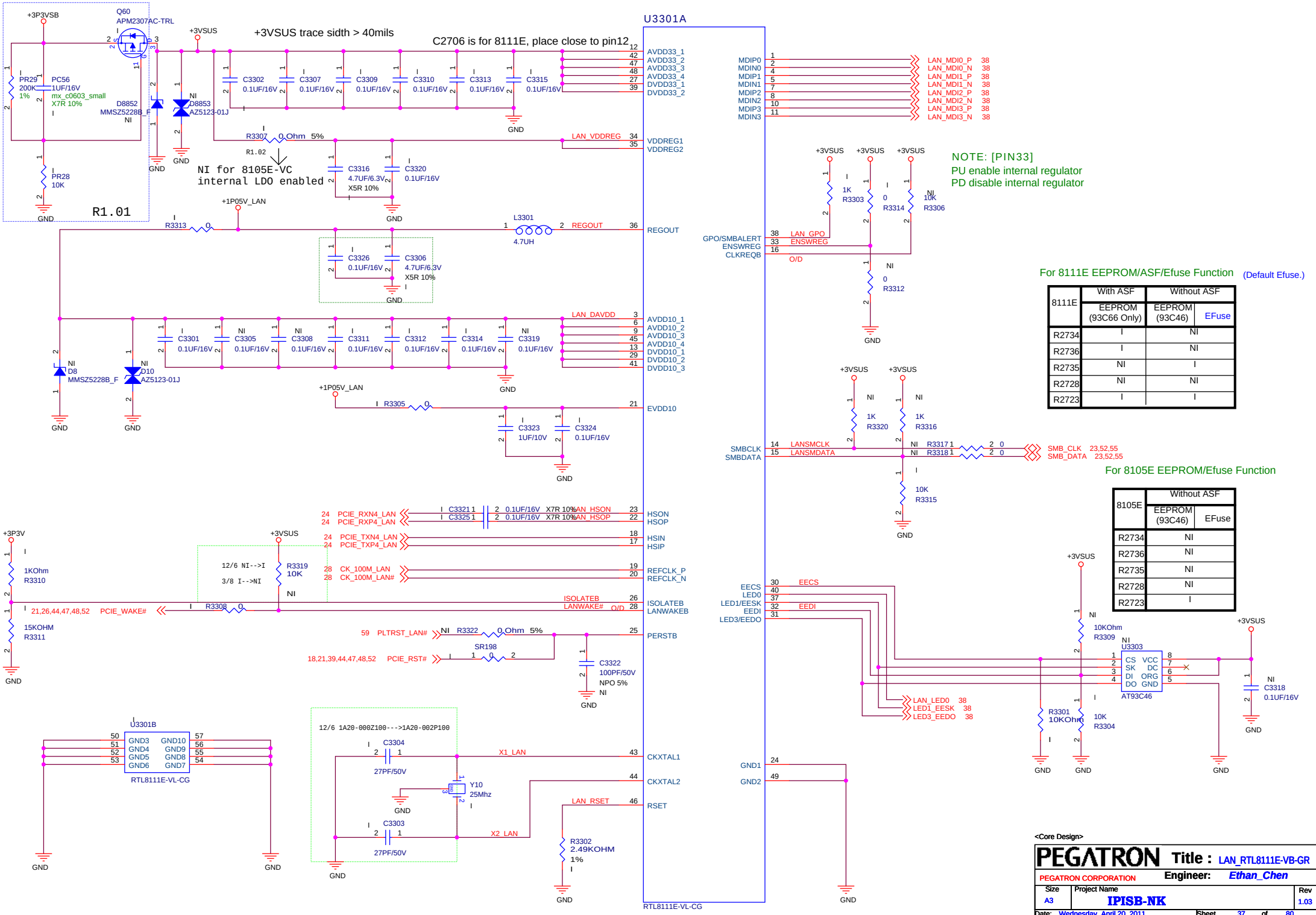
Date: Wednesday, April 20, 2011 Sheet 35 of 80



PEGATRON	Title : HDMI mux	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 36 of 80	

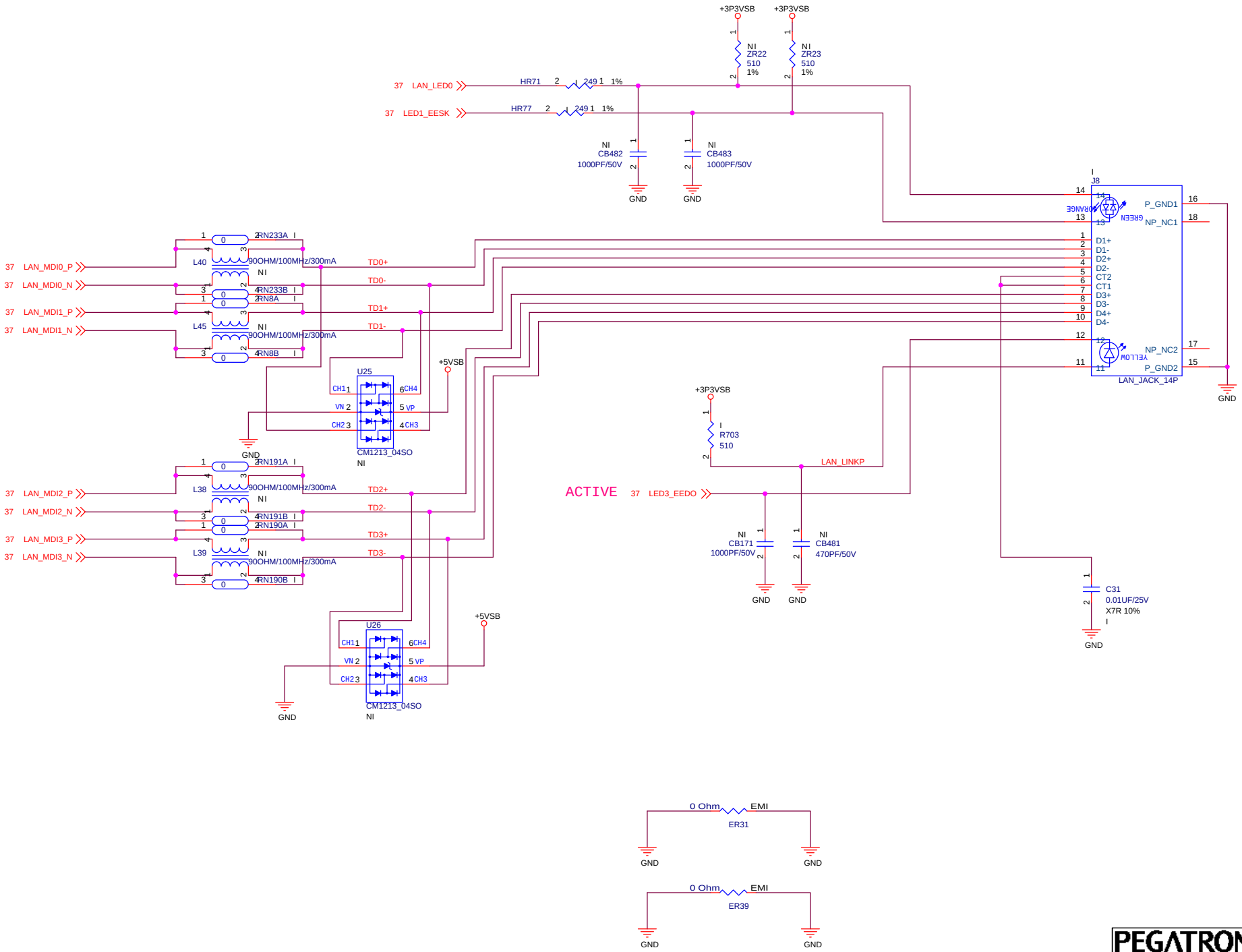


PEGATRON	Title : AMP/PWR		
PEGATRON CORPORATION	Engineer: Ethan_Chen		
Size: A2	Project Name: IPISB-NK		Rev: 1.03
Date: Thursday, April 21, 2011	Sheet 43 of 80		

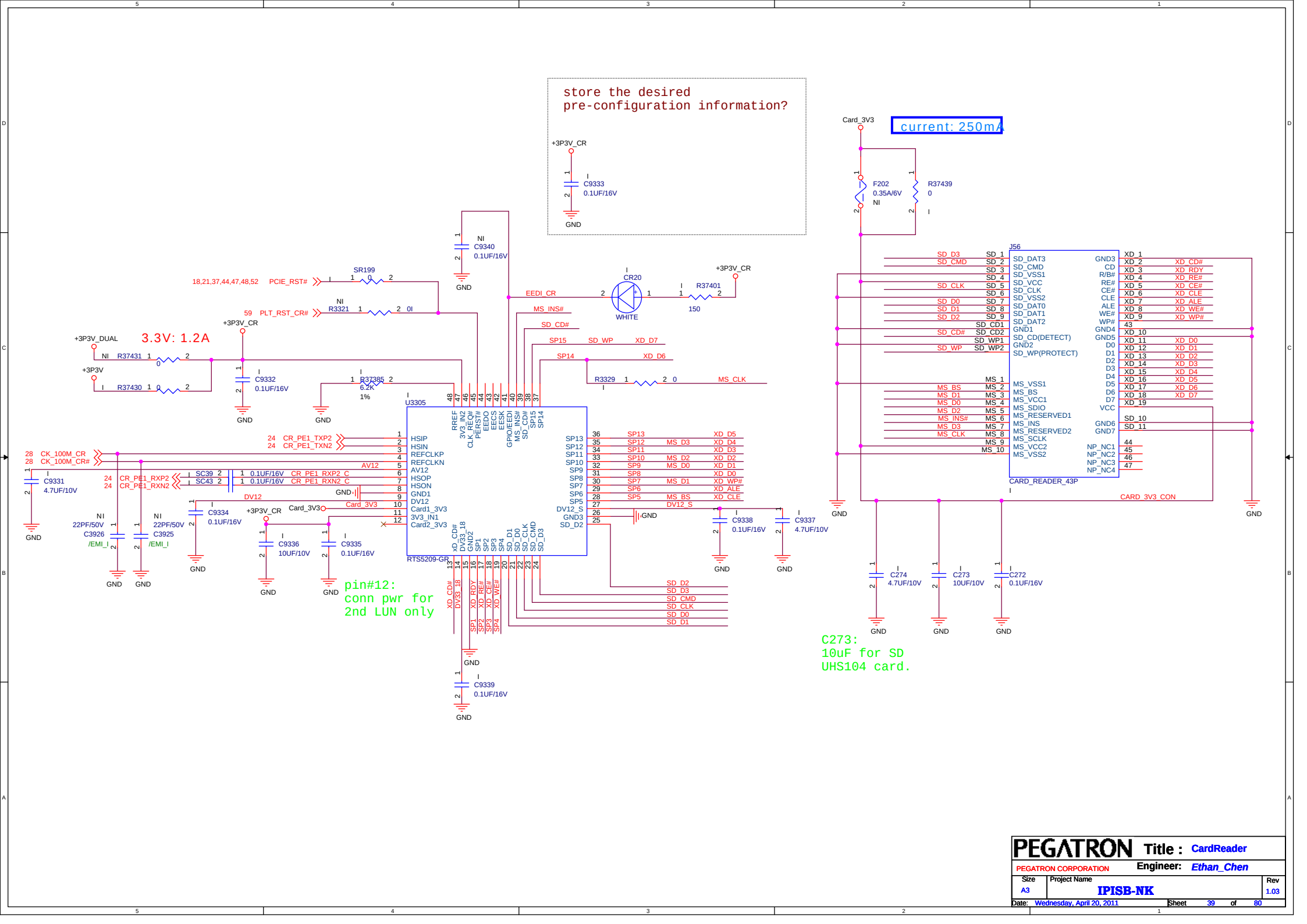


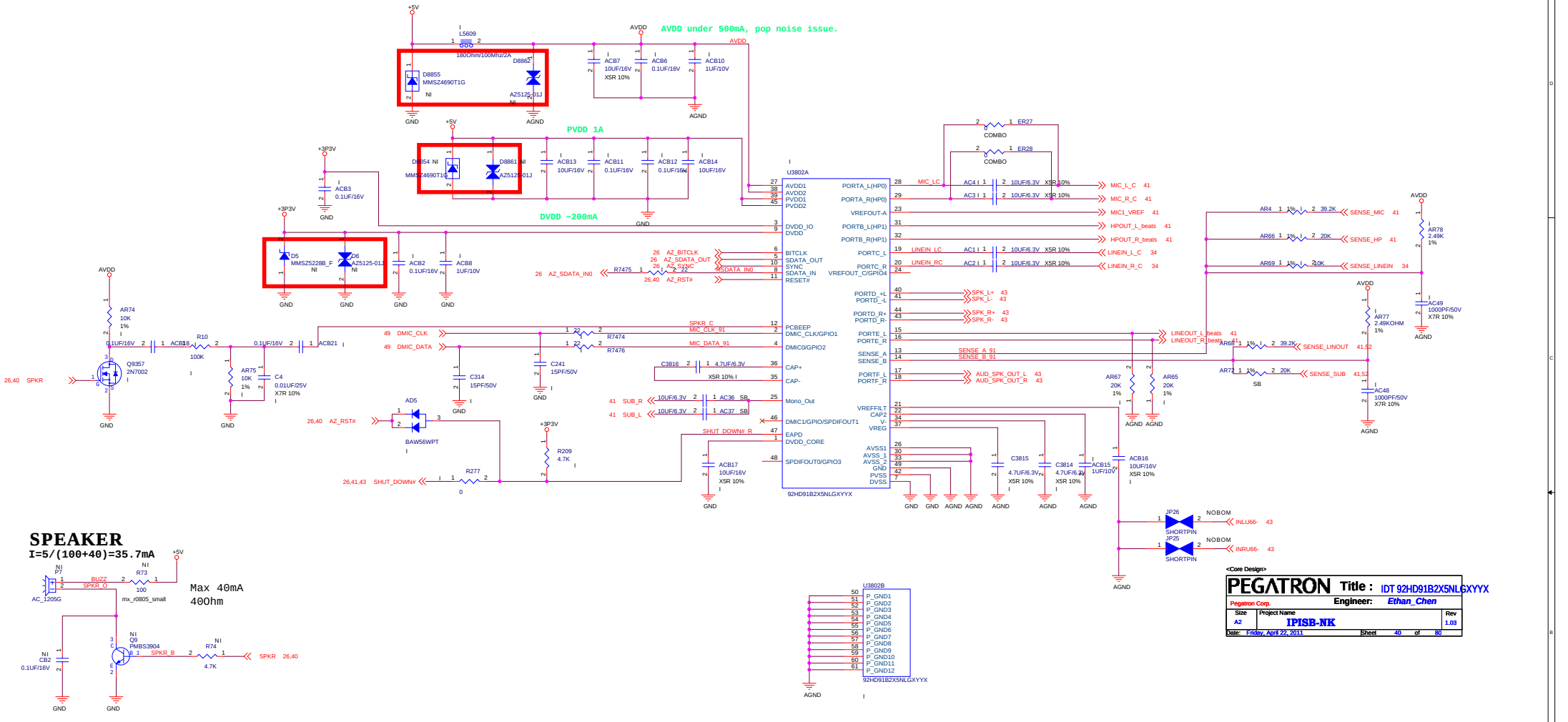
8111E	With ASF	Without ASF	
	EEPROM (93C66 Only)	EEPROM (93C46)	EFuse
R2734	I	NI	
R2736	I	NI	
R2735	NI	I	
R2728	NI	NI	
R2723	I	I	

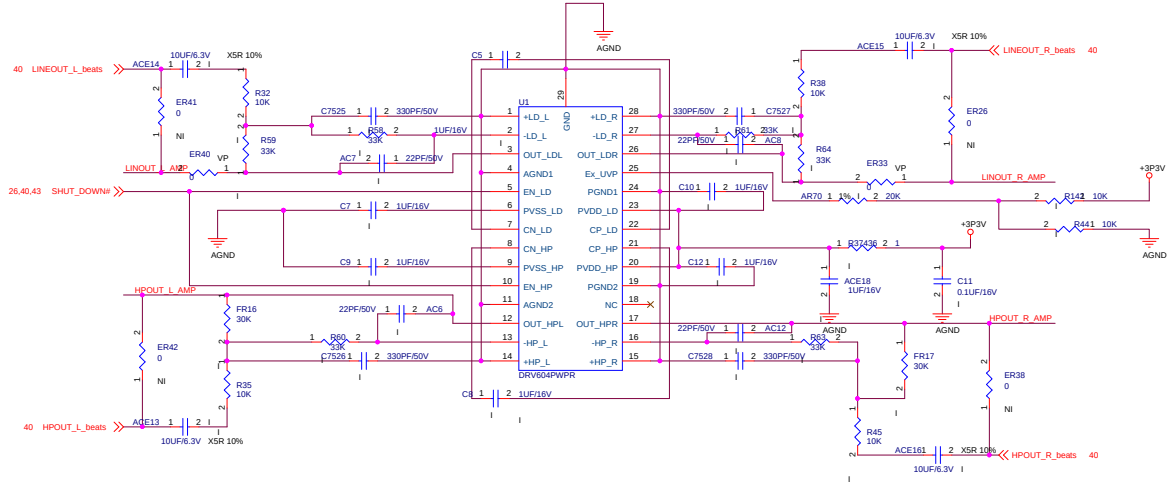
8105E	Without ASF	
	EEPROM (93C46)	EFuse
R2734	NI	
R2736	NI	
R2735	NI	
R2728	NI	
R2723	I	



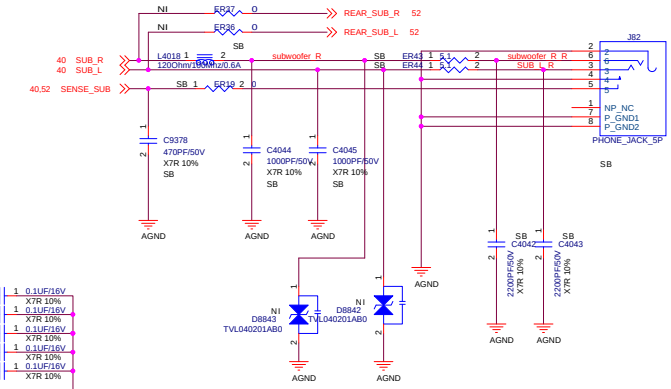
PEGATRON	Title :	LAN-CONN
PEGATRON CORPORATION	Engineer:	Ethan_Chen
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 38 of 80	

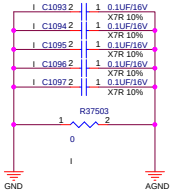

store the desired
pre-configuration information?
+3P3V_CR
C9333
0.1UF/16V
GND
current: 250mA
Card_3V3
F202
0.35A/6V
NI
R37439
0
3.3V: 1.2A
+3P3V_DUAL
+3P3V
R37431
R37430
C9332
0.1UF/16V
NI
C9340
0.1UF/16V
SR199
18,21,37,44,47,48,52
PCIE_RST#
NI
R3321
59
PLT_RST_CR#
EEDI_CR
CR20
WHITE
R37401
150
MS_INS#
SD_CD#
SP15
SD_WP
XD_D7
SP14
XD_D6
R3329
MS_CLK
R37385
6.2K
1%
U3305
RTS5209-GR
RREF
3V3_IN2
CLK_REQ#
PERST#
EEDO
EECS
EESK
GPIO/EEDI
MS_INS#
SD_CD#
SP15
SP14
HSIP
HSIN
REFCLKP
REFCLKN
AV12
HSOP
HSON
GND1
DV12
Card1_3V3
3V3_IN1
Card2_3V3
DV12_S
GND3
SD_D2
XD_CD#
DV33_18
GND2
SP1
SP2
SP3
SP4
SD_D1
SD_D0
SD_CLK
SD_CMD
SD_D3
XD_RDY
XD_RE#
XD_CE#
XD_WE#
28 CK_100M_CR
28 CK_100M_CR#
24 CR_PE1_TXP2
24 CR_PE1_TXN2
24 CR_PE1_RXP2
24 CR_PE1_RXN2
SC39
SC43
0.1UF/16V
CR_PE1_RXP2_C
CR_PE1_RXN2_C
C9331
4.7UF/10V
C9334
0.1UF/16V
C9336
10UF/10V
C9335
0.1UF/16V
C9338
0.1UF/16V
C9337
4.7UF/10V
C9339
0.1UF/16V
NI
22PF/50V
C3926
/EMI_I
C3925
/EMI_I
pin#12:
conn pwr for
2nd LUN only
J56
CARD_READER_43P
SD_DAT3
SD_CMD
SD_VSS1
SD_VCC
SD_CLK
SD_VSS2
SD_DAT0
SD_DAT1
SD_DAT2
GND1
SD_CD(DETECT)
GND2
SD_WP(PROTECT)
MS_VSS1
MS_BS
MS_VCC1
MS_SDIO
MS_RESERVED1
MS_INS
MS_RESERVED2
MS_SCLK
MS_VCC2
MS_VSS2
GND3
CD
R/B#
RE#
CE#
CLE
ALE
WE#
WP#
GND4
GND5
D0
D1
D2
D3
D4
D5
D6
D7
VCC
GND6
GND7
NP_NC1
NP_NC2
NP_NC3
NP_NC4
CARD_3V3_CON
C274
4.7UF/10V
C273
10UF/10V
C272
0.1UF/16V
C273:
10uF for SD
UHS104 card.
PEGATRON
Title : CardReader
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size
A3
Project Name
IPISB-NK
Rev
1.03
Date: Wednesday, April 20, 2011
Sheet 39 of 80


AVDD under 500mA, pop noise issue.
PVDD 1A
DVDD ~200mA
U3802A
92HD91B2X5NLGXYYX
SPEAKER
I=5/(100+40)=35.7mA
Max 40mA
40Ohm
U3802B
PEGATRON
Title : IDT 92HD91B2X5NLGXYYX
Pegatron Corp.
Engineer: Ethan_Chen
Project Name
IPISB-NK
Size
A2
Rev
1.03
Date: Friday, April 22, 2011
Sheet 40 of 80

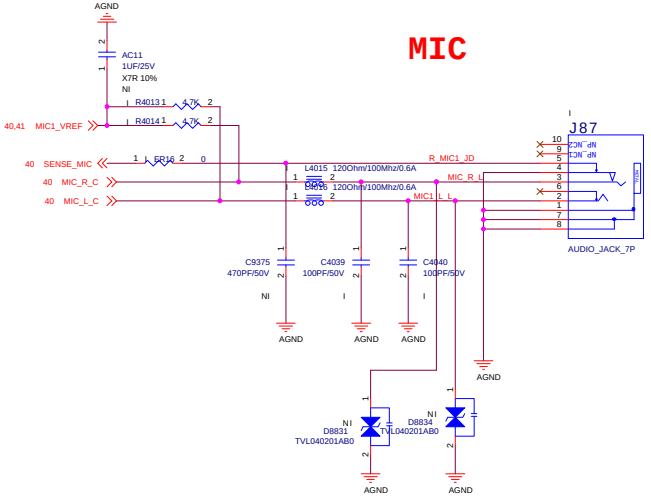


Subwoofer

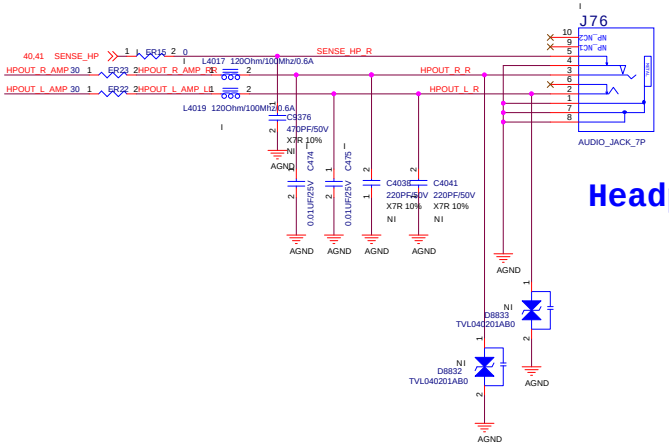




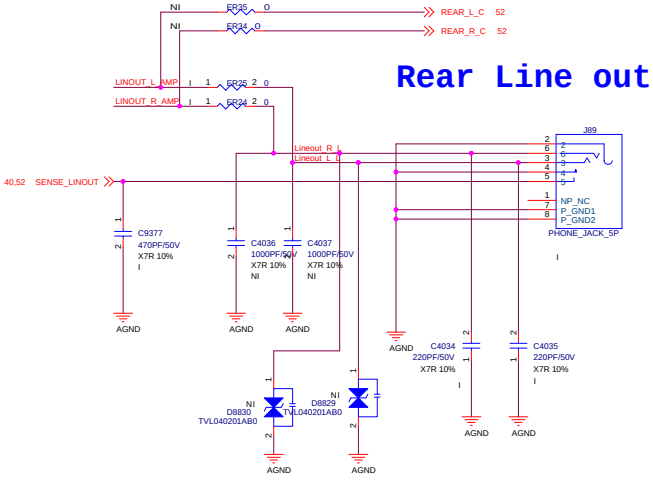
MIC

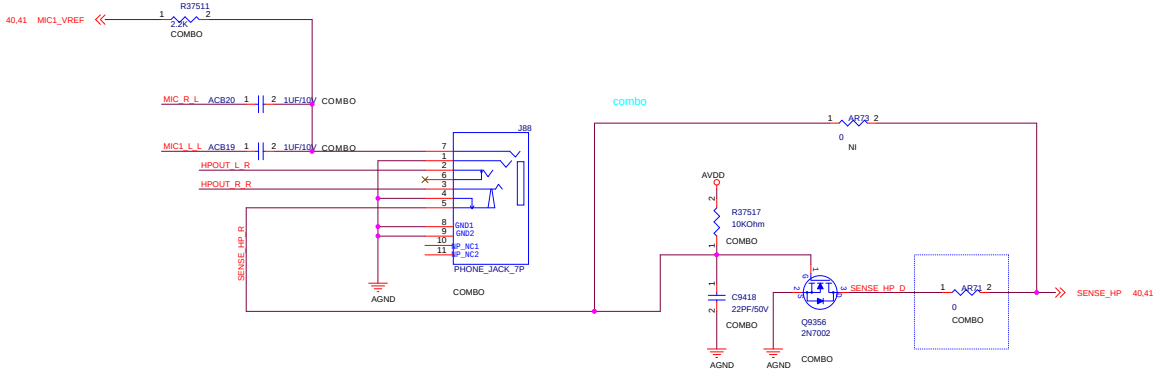


Headphone



Rear Line out





<Core Design>

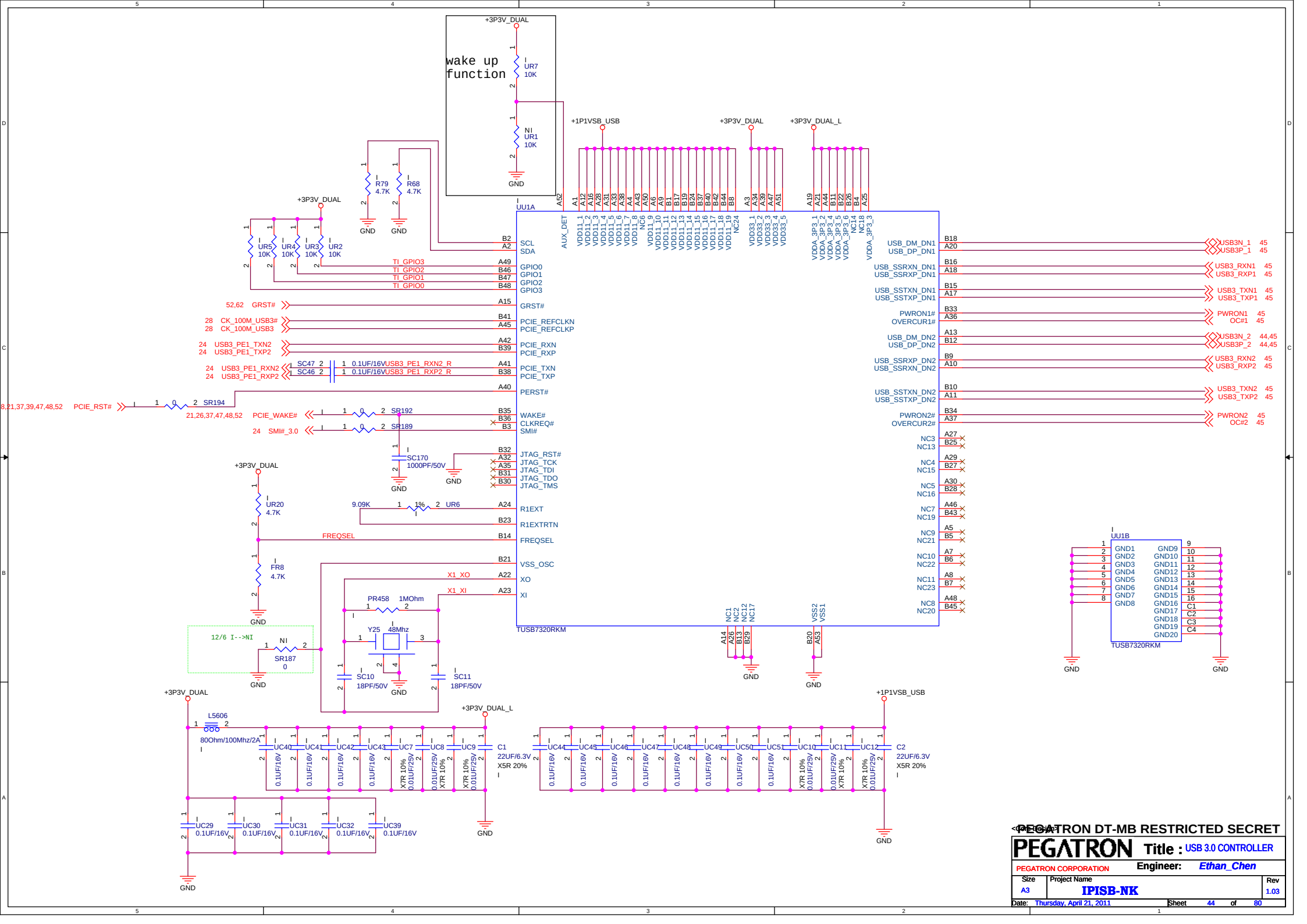
PEGATRON Title : Audio Jack

Pegatron Corp. Engineer: Ethan_Chen

Size	Project Name	Rev
A2	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 41 of 80

PEGATRON	Title :	IDT/89D3	
PEGATRON CORPORATION	Engineer:	*Ethan_Chen*	
Size: C	Project Name: IPISB-NK		Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 42 of 80		



PEGATRON

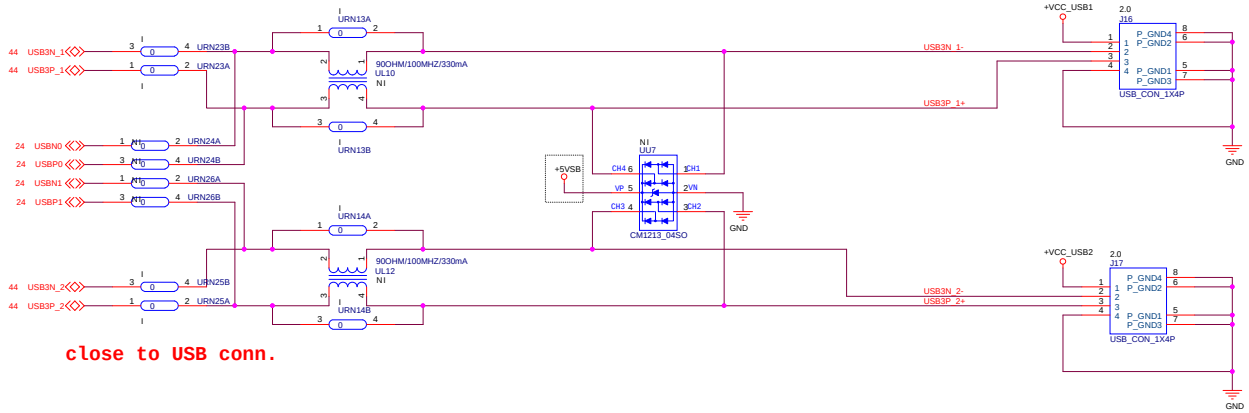
Title : USB 3.0 CONTROLLER

PEGATRON CORPORATION

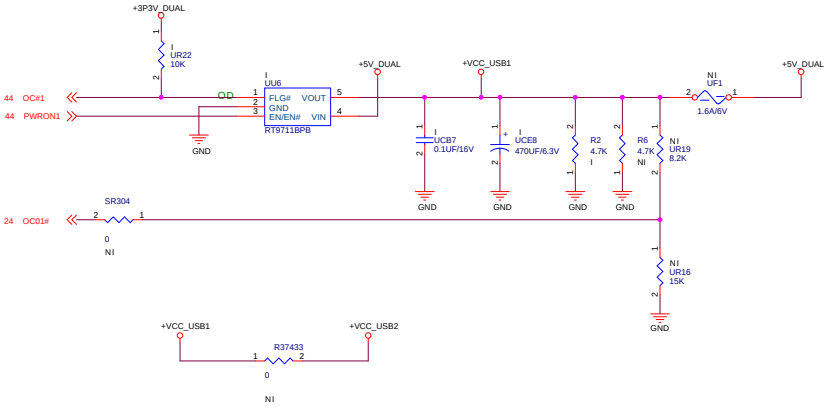
Engineer: Ethan_Chen

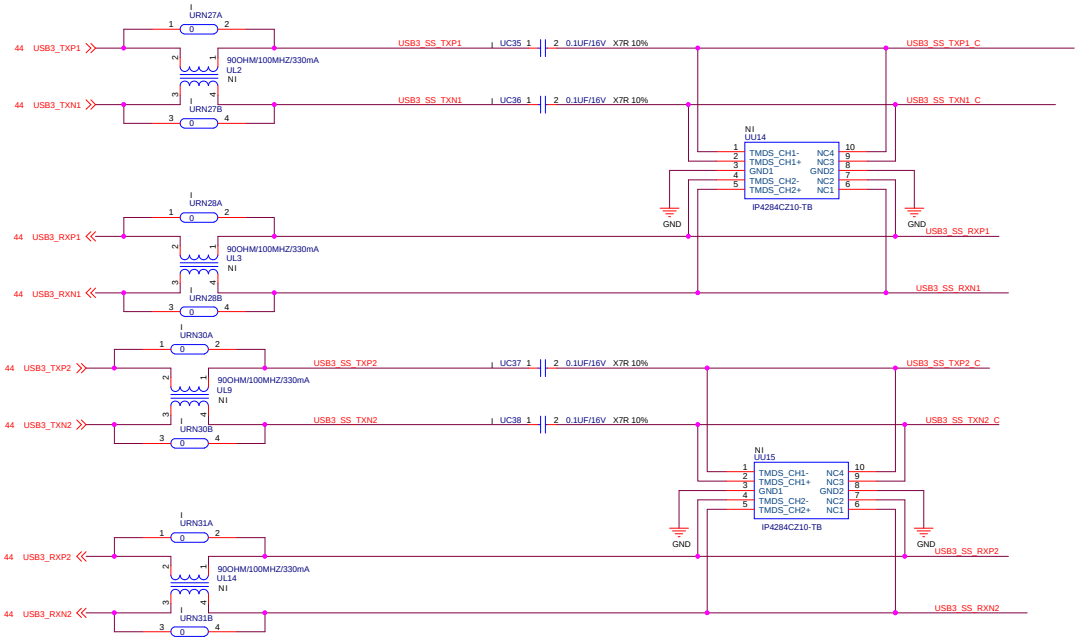
Size	Project Name	Rev
A3	IPISB-NK	1.03

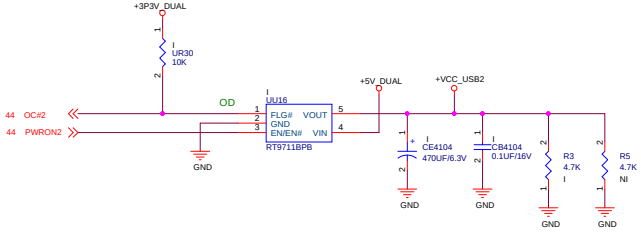
Date: Thursday, April 21, 2011 Sheet 44 of 80

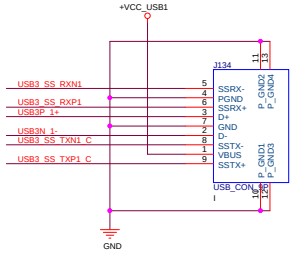


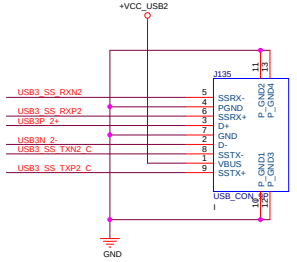
close to USB conn.











NOTE:
0722-0066000 ESD PROTECTION SOT1059 NXP/IP4284CZ10-TB
0722-003Y000 ESD PROTECTION TSLP-9-1 INFINEON/ESD5V3U4U-HDMI

1213-00LN000 USB2.0

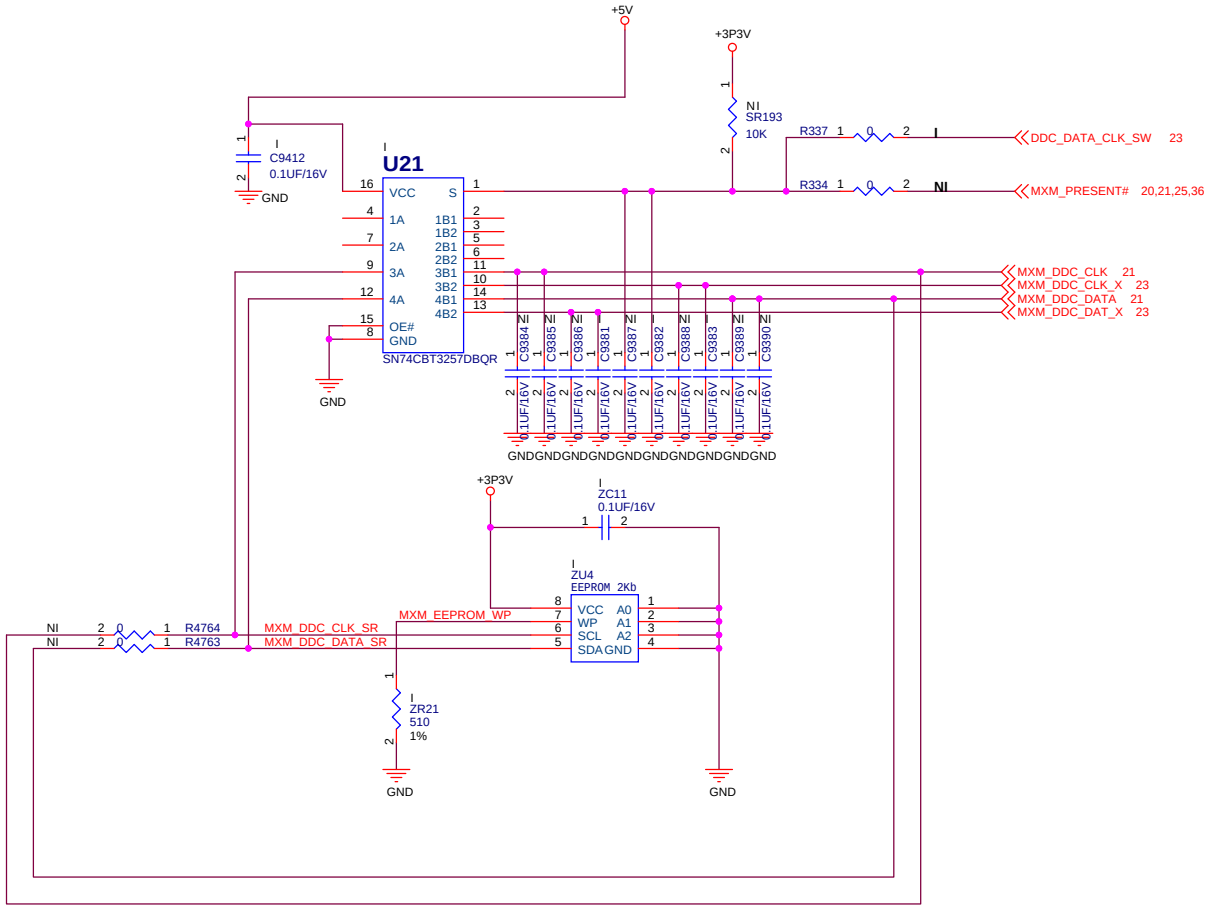
PIN NO.	1	2	3	4
SIGNAL NAME	VBUS	D-	D+	PGND
REMARK	USB2.0 CONTACT PIN			

Gold flash only

Co-lay USB connecter
1213-00LH000 USB3.0
1213-00LN000 USB2.0

<Core Design>

PEGATRON Title : USB colay
PEGATRON CORPORATION Engineer: Ethan_Chen
Size A2 | Project Name IPISB-NK | Rev 1.03
Date: Wednesday, April 20, 2011 | Sheet 45 of 80



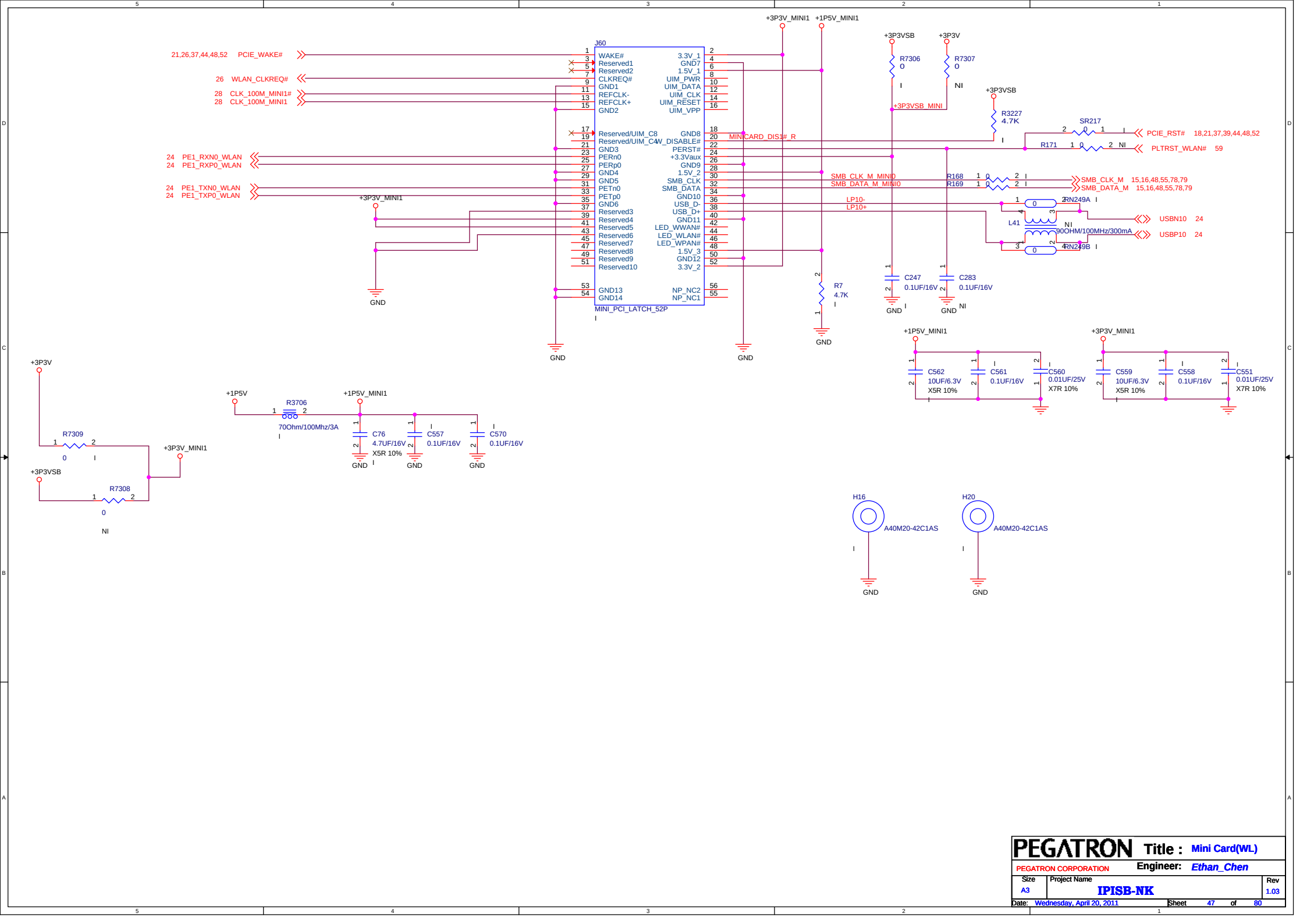
<Core Design>

PEGATRON Title : N/A

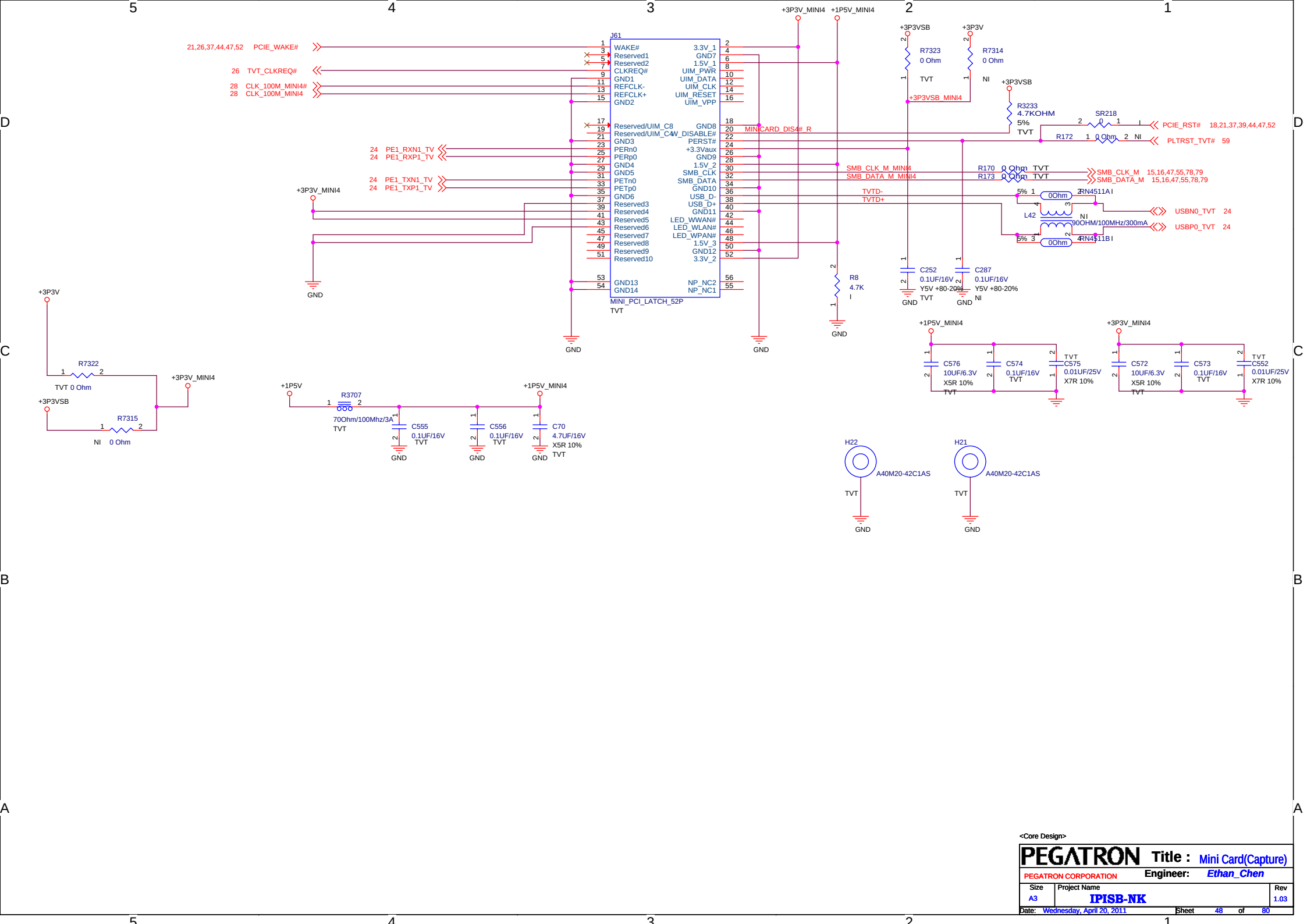
PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 46 of 80



PEGATRON	Title :	Mini Card(WL)
PEGATRON CORPORATION	Engineer:	Ethan_Chen
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 47 of 80	



<Core Design>

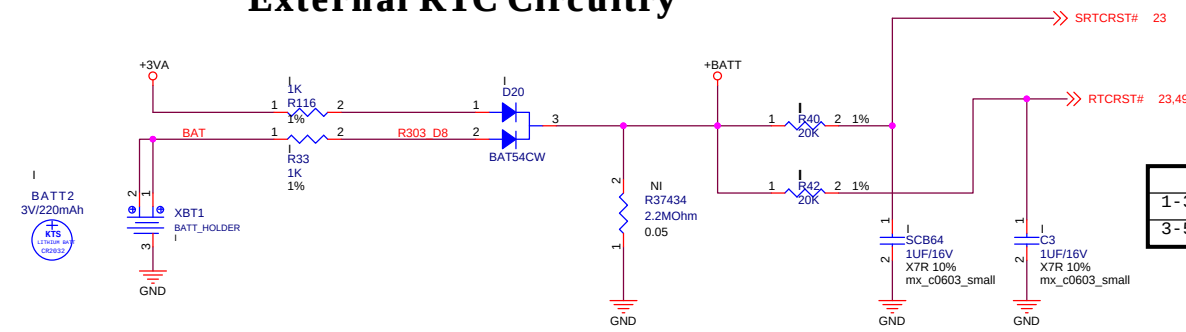
PEGATRON Title : Mini Card(Capture)

PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 48 of 80

External RTC Circuitry



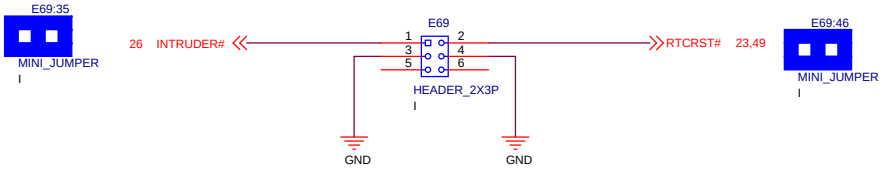
	PASSWORD
1-3	CLEAR
3-5	Default

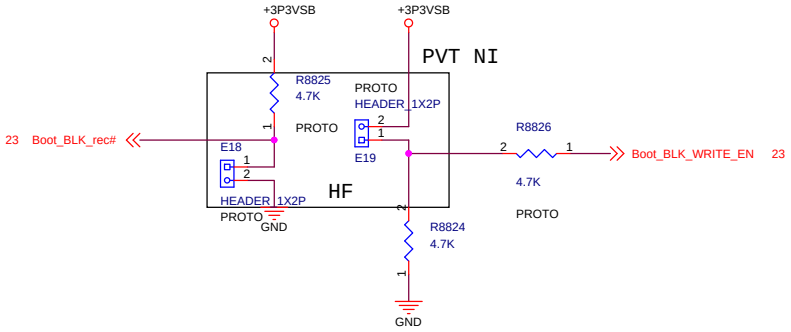
CLR CMOS AND PASSWORD CIRCUIT

	CMOS RTC
2-4	CLEAR
4-6	Default

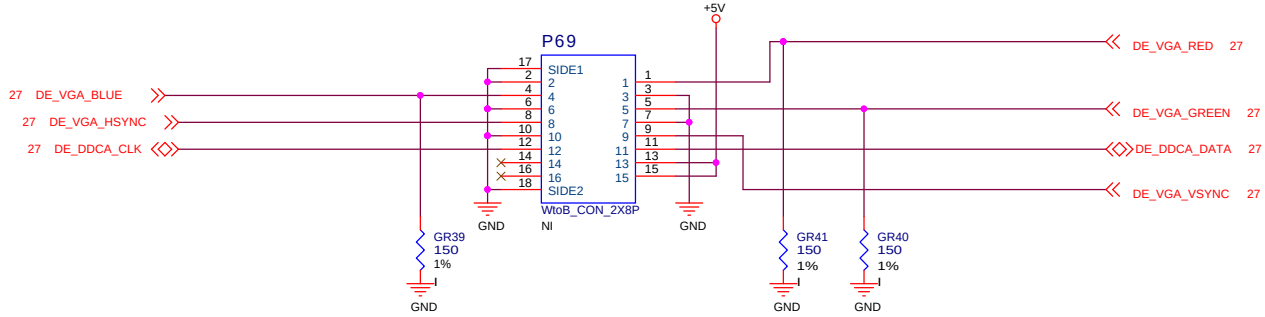
Battery Socket

NOTE:
Place C6 near PCH.

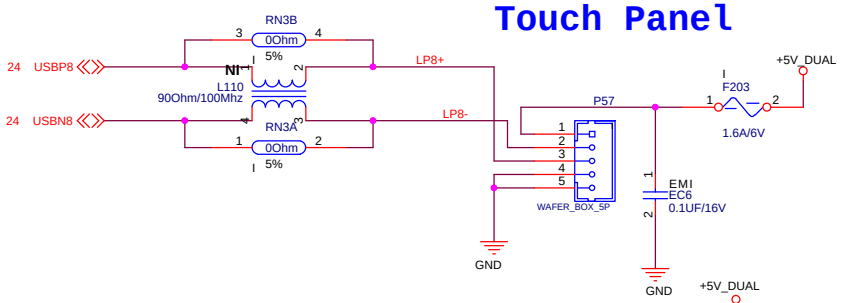


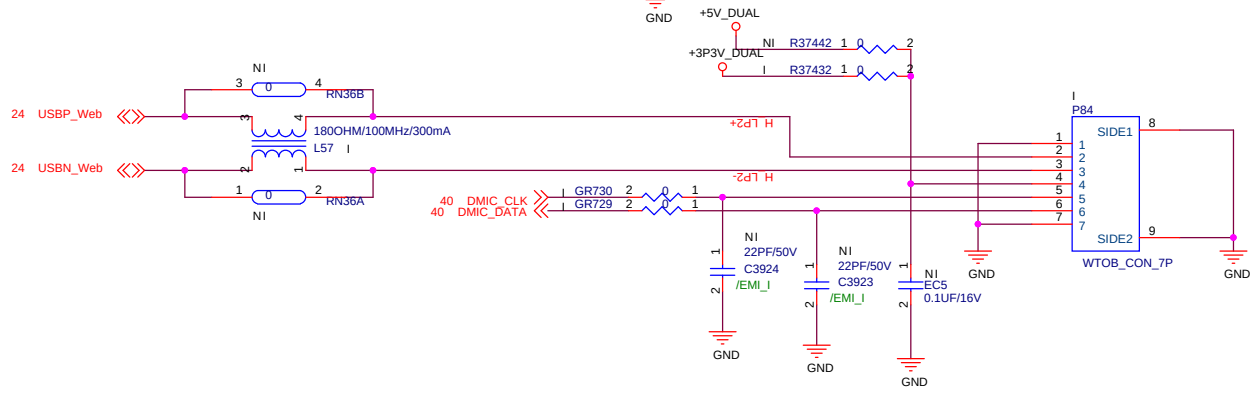


VGA Debug

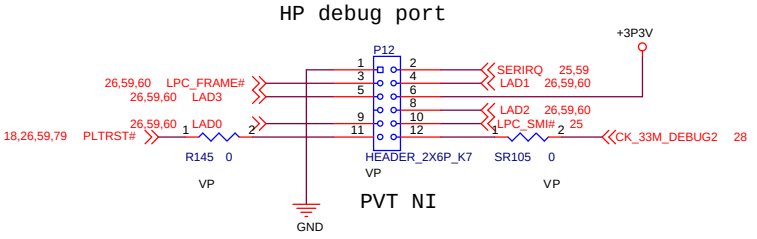


Touch Panel





HP debug port



PEGATRON

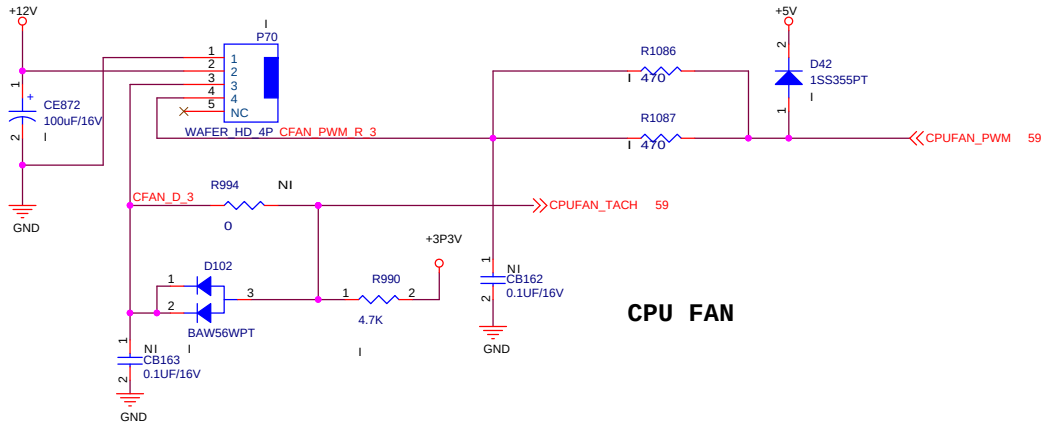
Title : SATA

PEGATRON CORPORATION

Engineer: Ethan_Chen

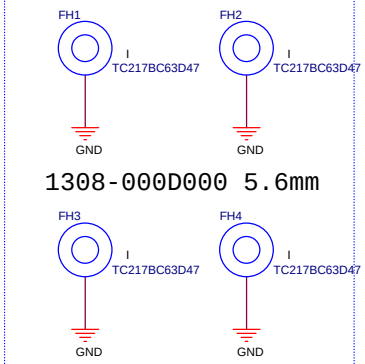
Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 49 of 80

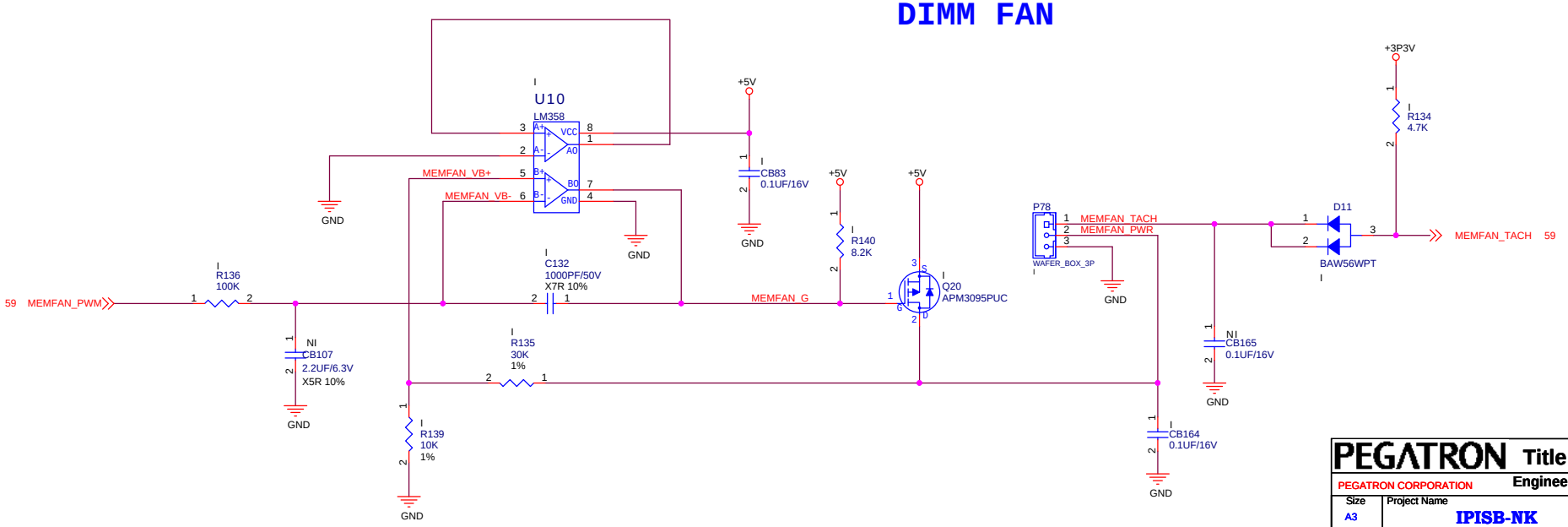


CPU FAN

DIMM FAN NUT

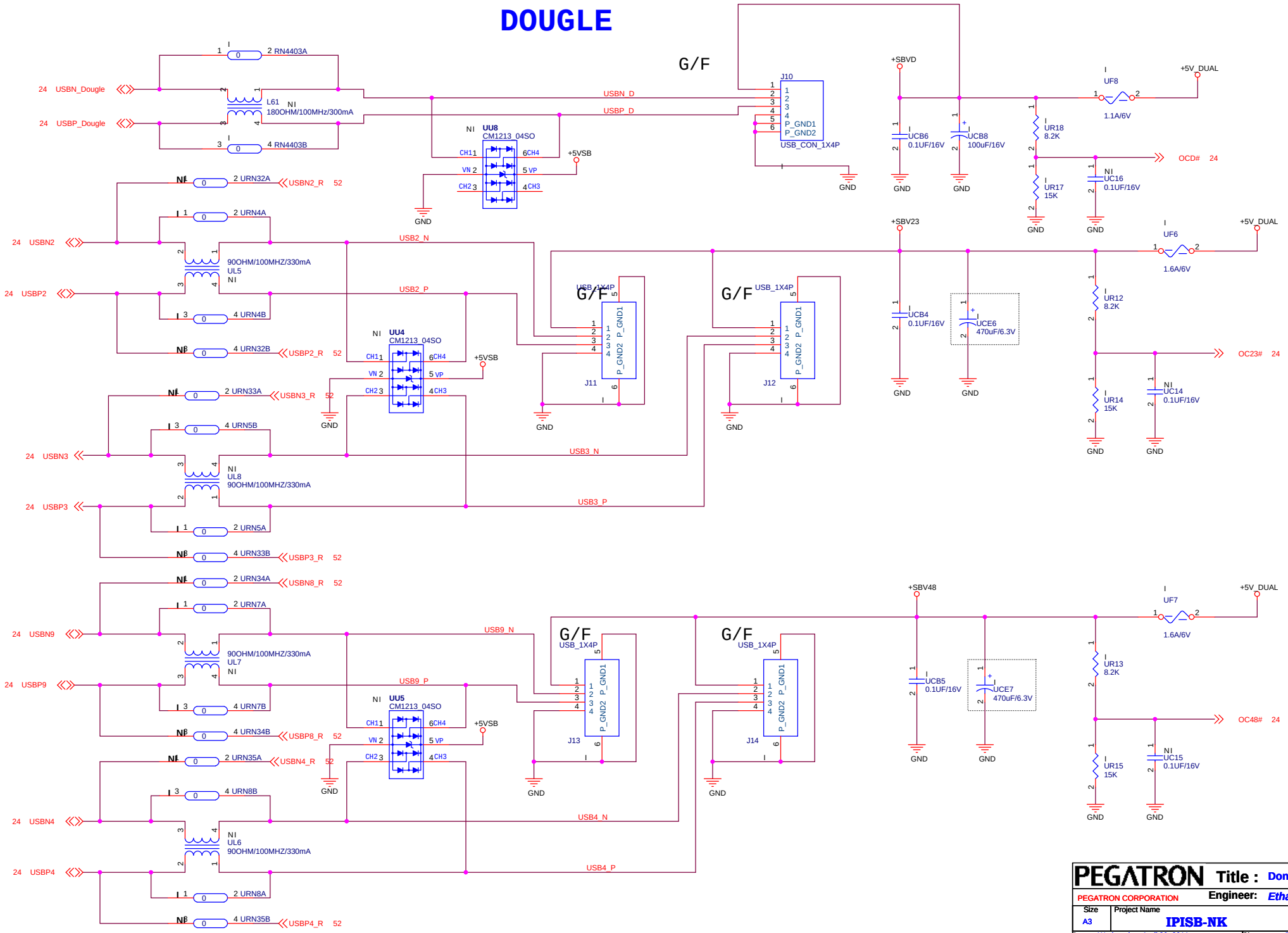


DIMM FAN



PEGATRON	Title : FAN	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 50 of 80	

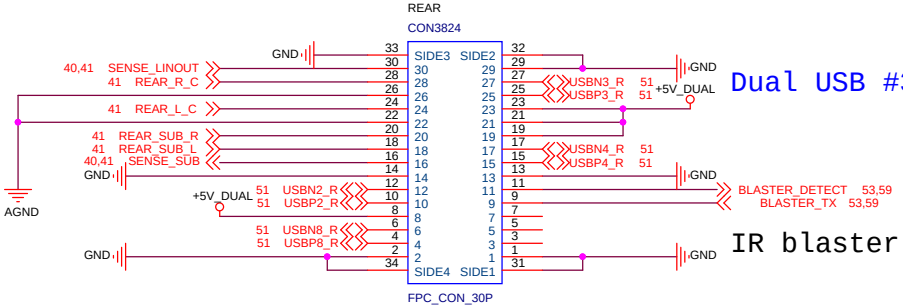
DOUGLE



PEGATRON	Title :	Dongle&rear USB
PEGATRON CORPORATION	Engineer:	Ethan_Chen
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 51 of 80	

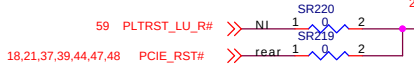
Line-out + subwoofer

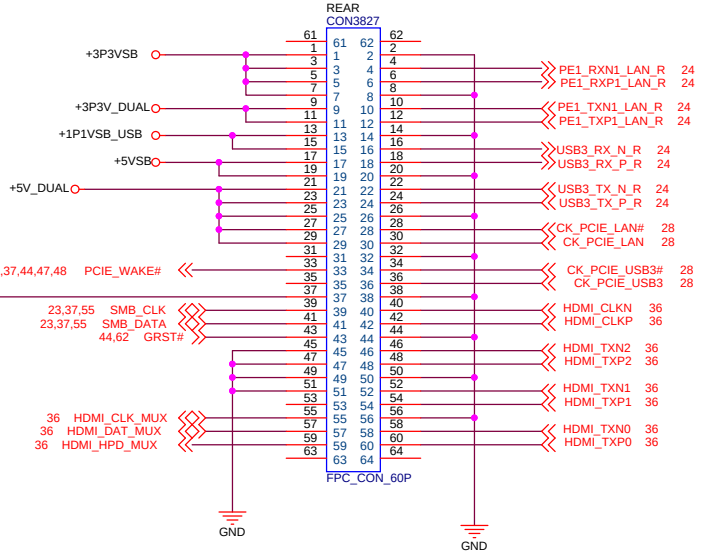
Dual USB #1,2



Dual USB #3,4

IR blaster





PEGATRON

Title : accelerometer

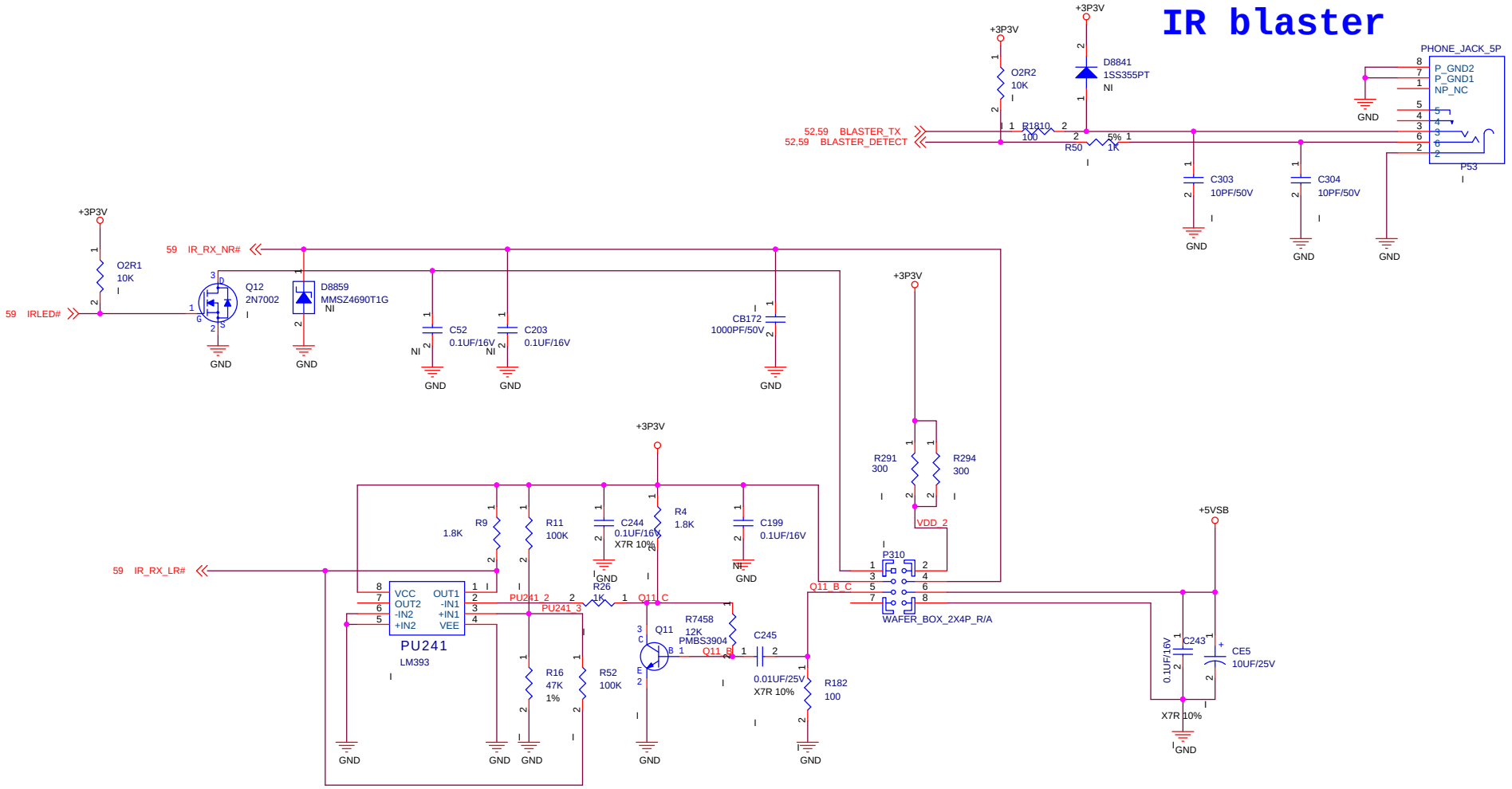
PEGATRON CORPORATION

Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 52 of 80

IR blaster



<Core Design>

PEGATRON

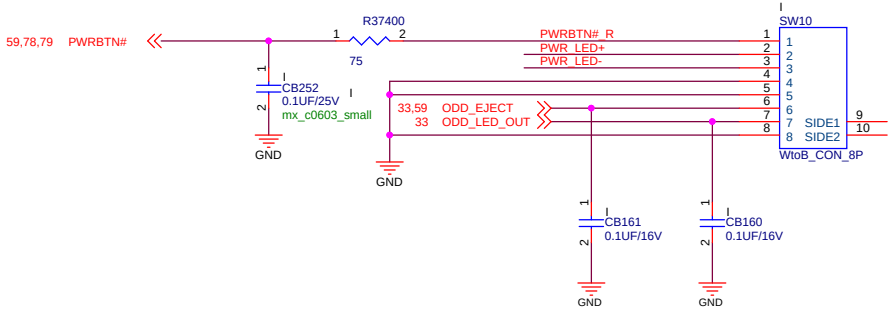
Title : IR LEDs

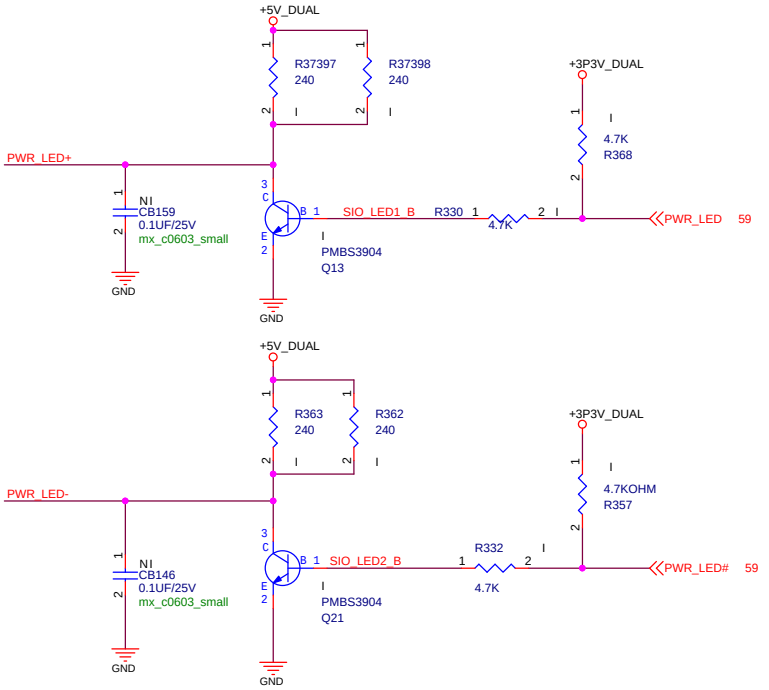
PEGATRON CORPORATION

Engineer: Ethan_Chen

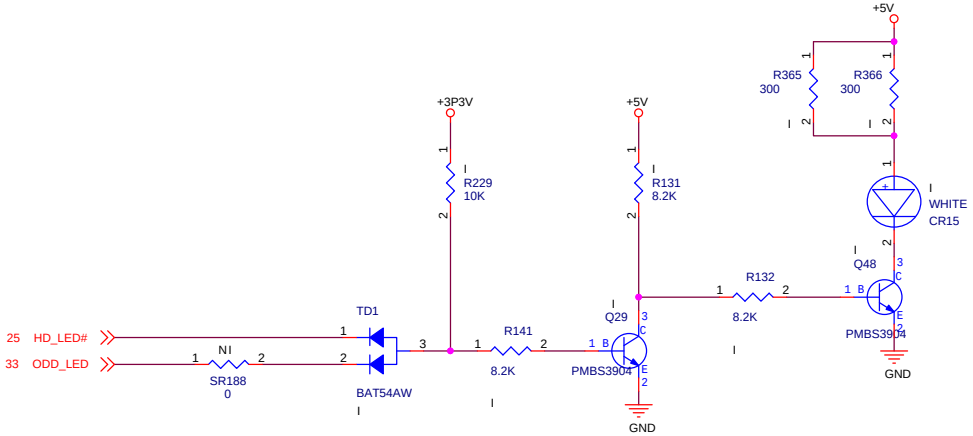
Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Thursday, April 21, 2011 Sheet 53 of 80

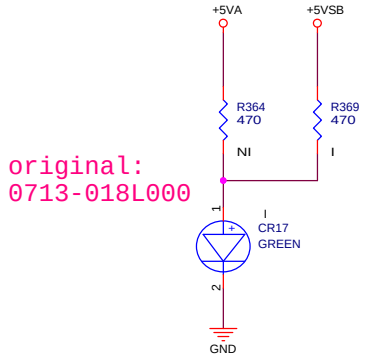




HDD LED



Power supply LED



<Core Design>

PEGATRON Title : PWE LED

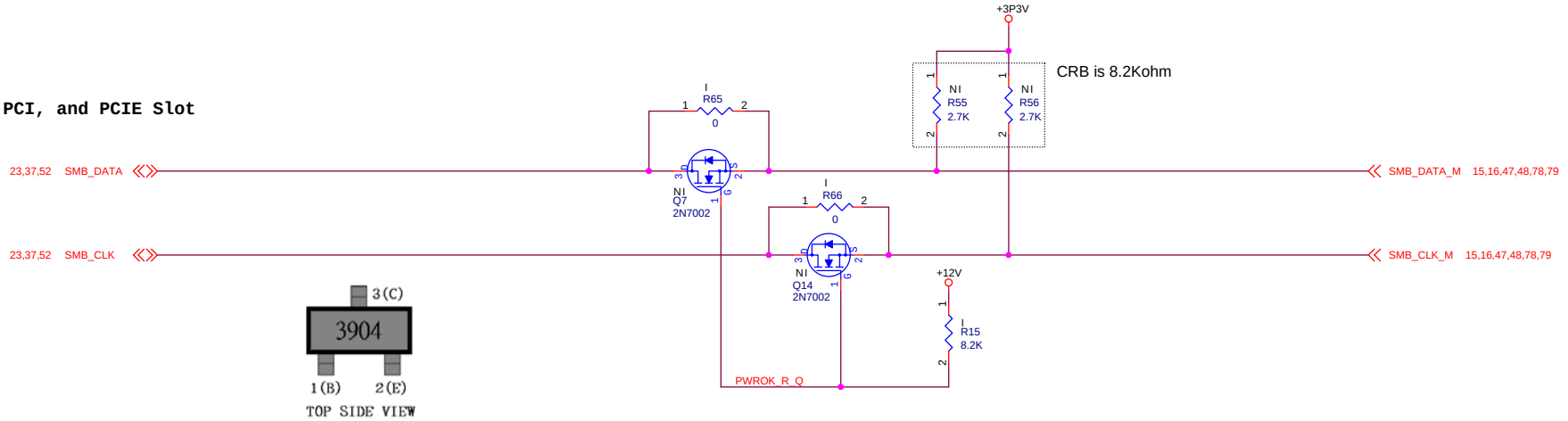
PEGATRON CORP. Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

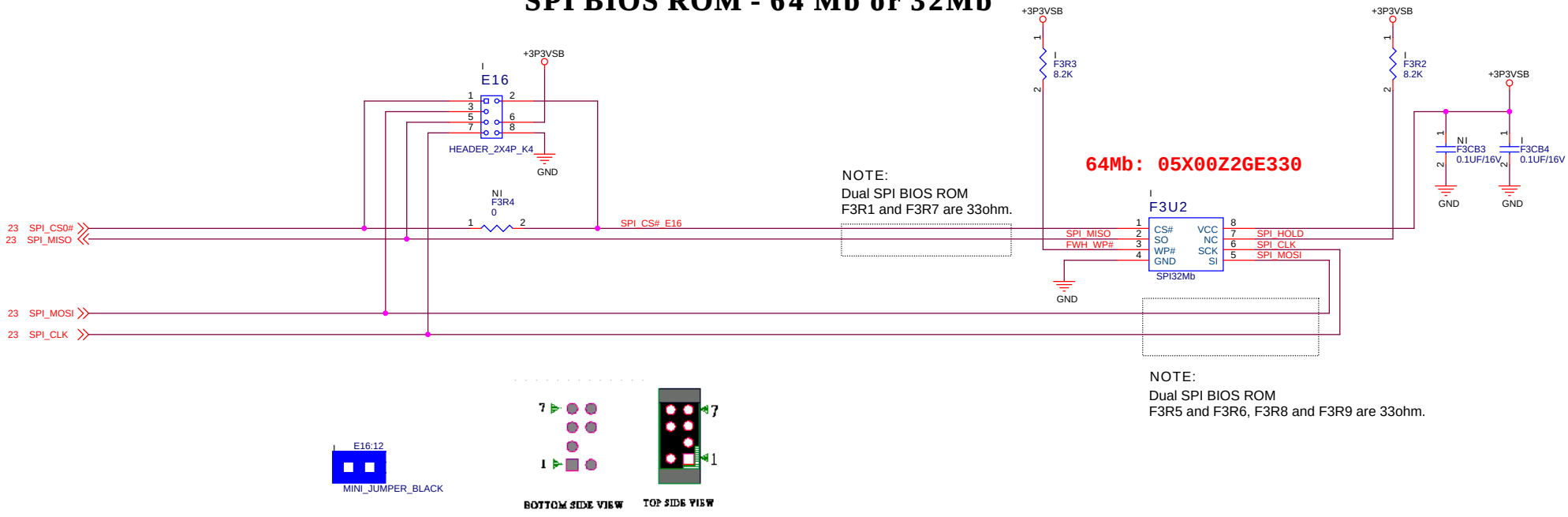
Date: Thursday, April 21, 2011 Sheet 54 of 80

SM BUS Control

To PCH, PCI, and PCIE Slot

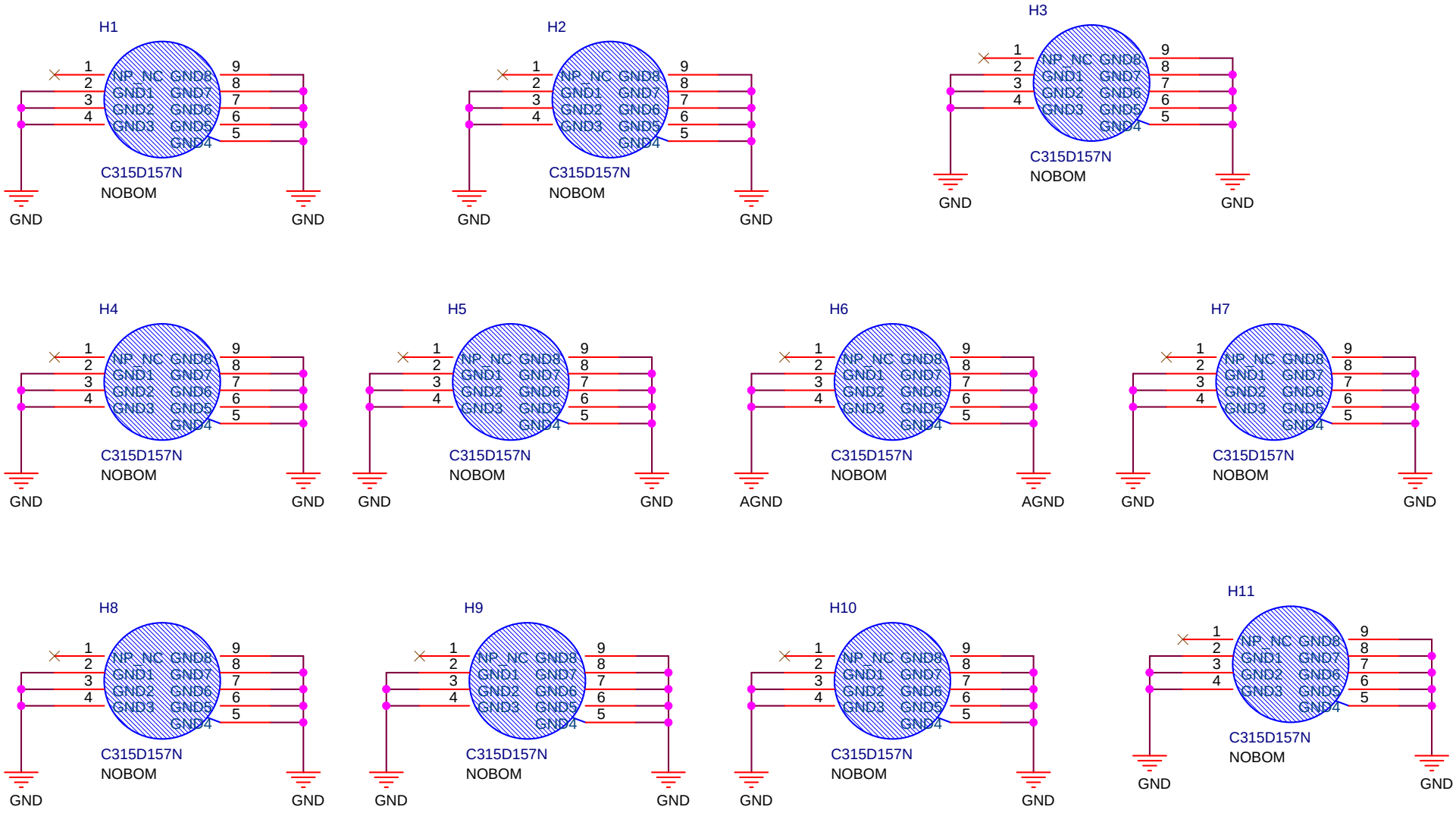


SPI BIOS ROM - 64 Mb or 32Mb



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	SM BUS & SPI ROM
PEGATRON CORPORATION	Engineer:	Ethan_Chen
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 55 of 80	



08M1-14B2200 08M1-14B3100
08M1-14B2000 08M1-14B3000
08M1-14B2100 08M1-14B3200

PCB_BRD1

IPISB-NK 1.01

VESA mount hole

<Core Design>

PEGATRON

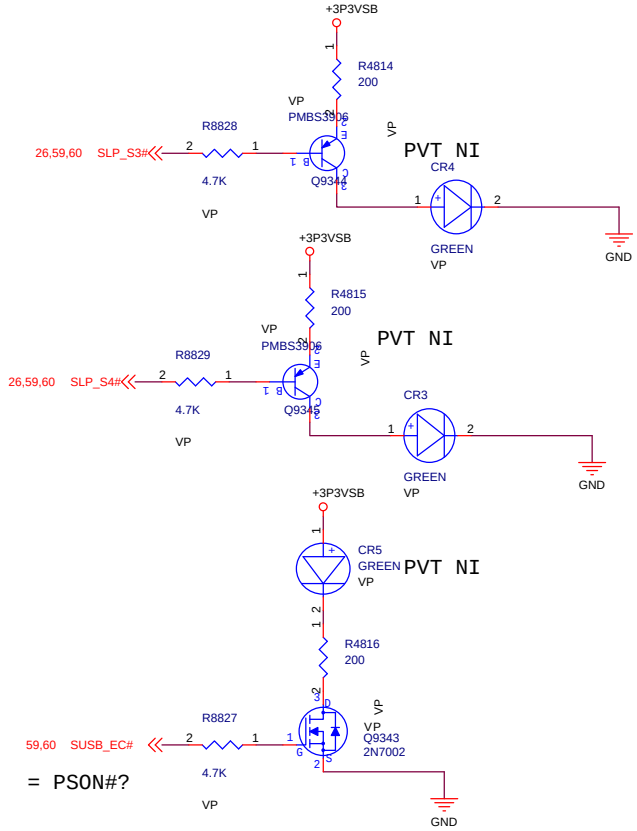
Title : SCREW HOLE

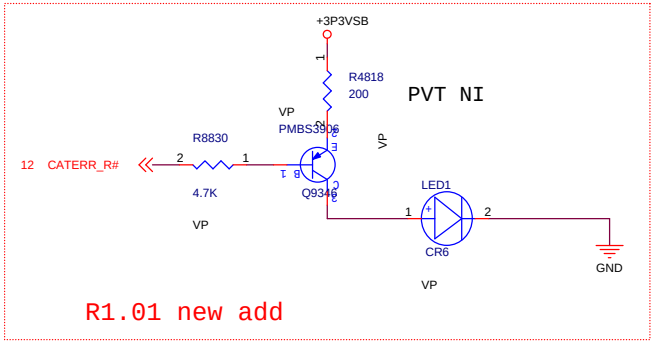
PEGATRON CORPORATION

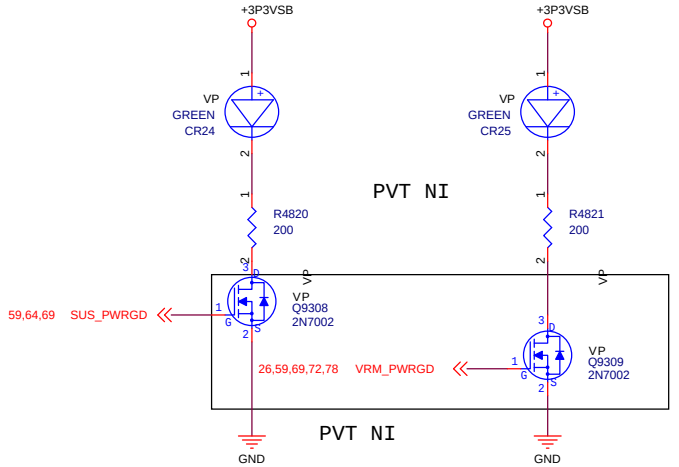
Engineer: Ethan_Chen

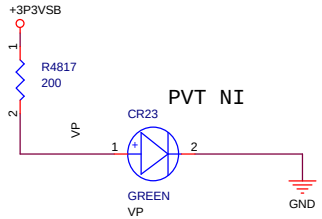
Size	Project Name	Rev
A	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 56 of 80









PEGATRON	Title : Debug LED	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 57 of 80	

PEGATRON

Title : PLTRST_CPU#&SMbus

PEGATRON CORPORATION

Engineer: *Ethan_Chen*

Size	Project Name	Rev
A	**IPISB-NK**	1.03

Date: Wednesday, April 20, 2011 Sheet 58 of 80

place under ChA dimm

66~73 GPI (input only)

UART: 0 to 3.3V level

Please place crystal circuit near to EC

PLEASE DO NOT PLACE ANY PULL-UP RESISTOR ON GPG0, GPG2 AND GPG6 (Reserved hardware strapping).

<Core Design>

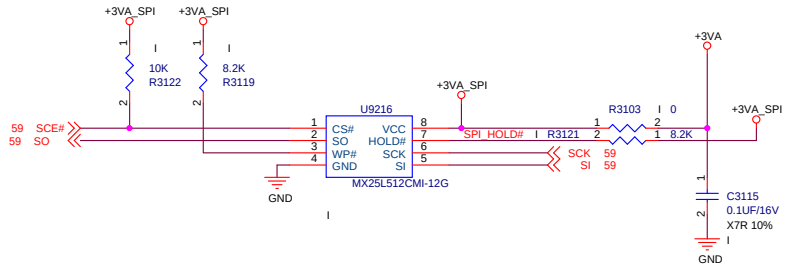
PEGATRON Title : EC_IT8519E-1

PEGATRON CORPORATION Engineer: Ethan_Chen

Size: Custom | Project Name: IPISB-NK | Rev: 1.03

Date: Thursday, April 21, 2011 | Sheet 59 of 80

SPI ROM+
External programming conn.



Touch PAD(deleted)

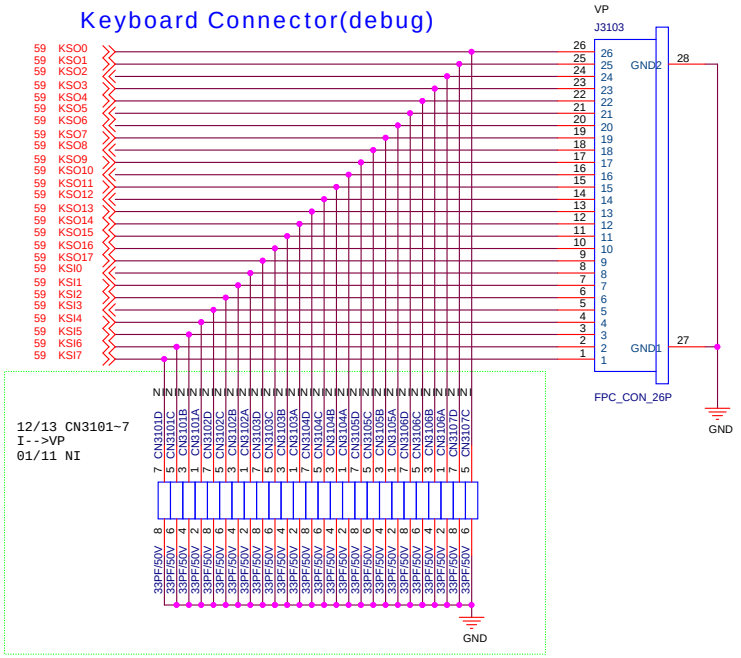
05X00Z2FC330 32Mb

0500-00P5000 (512Kb SPI)

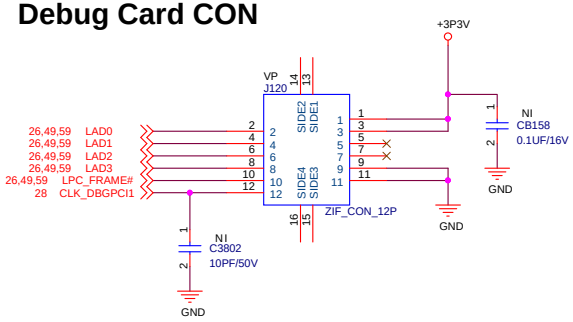
For Instant Key & Switch

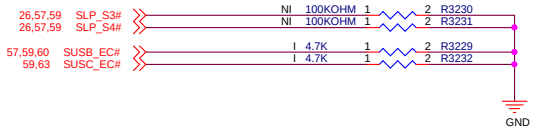
Note: **Close to EC**

Keyboard Connector(debug)

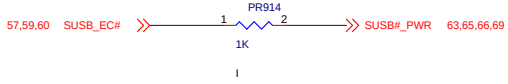


Debug Card CON





For EC PU/PD



<Core Design>

PEGATRON

Title : EC_IT8519E-2

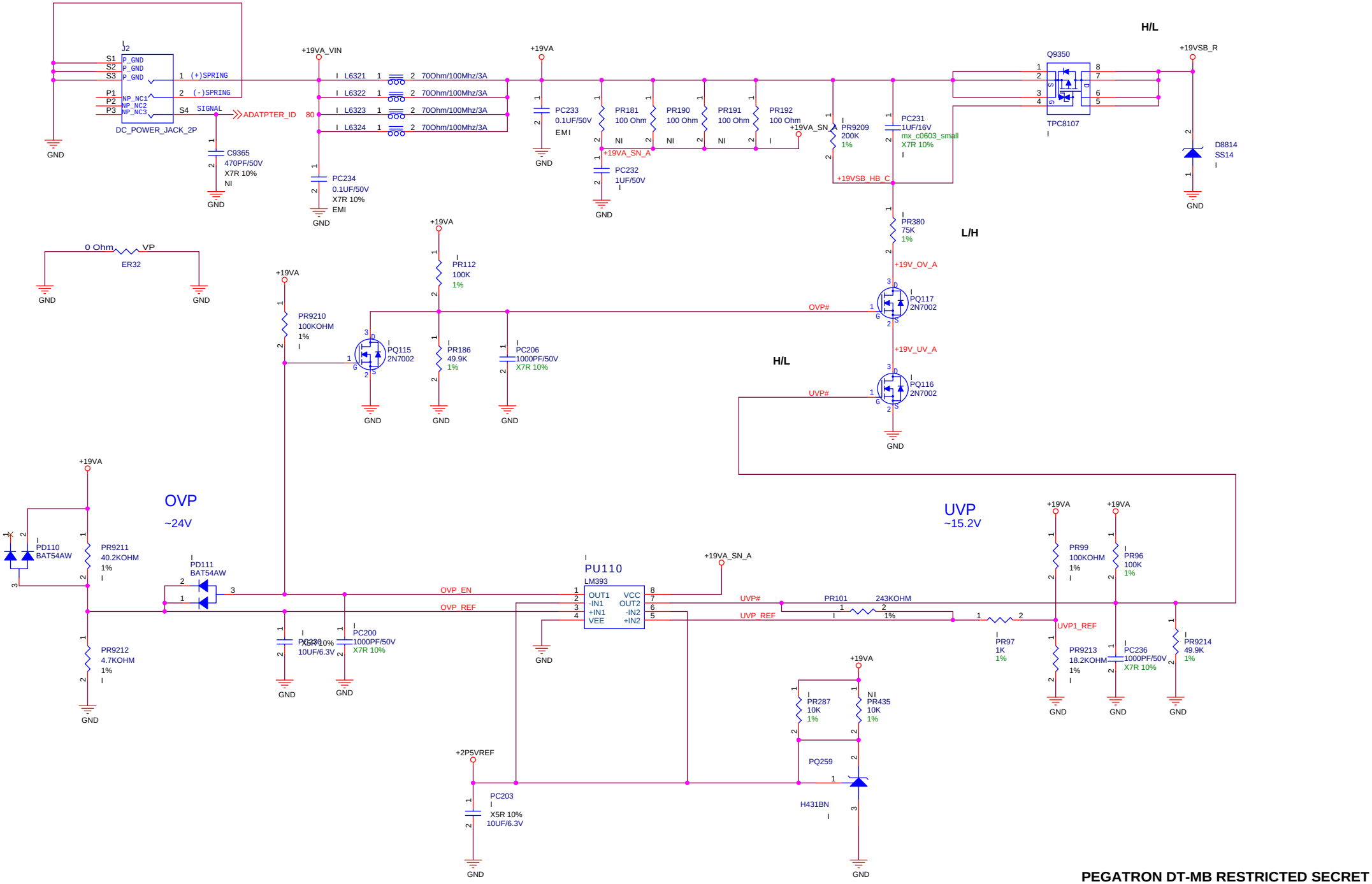
PEGATRON CORPORATION

Engineer: Ethan_Chen

Size	Project Name	Rev
Custom	IPISB-NK	1.03

Date: Thursday, April 21, 2011 Sheet 60 of 80

change to SIMULA /AJ261B-Y090-42F, p/n applying....



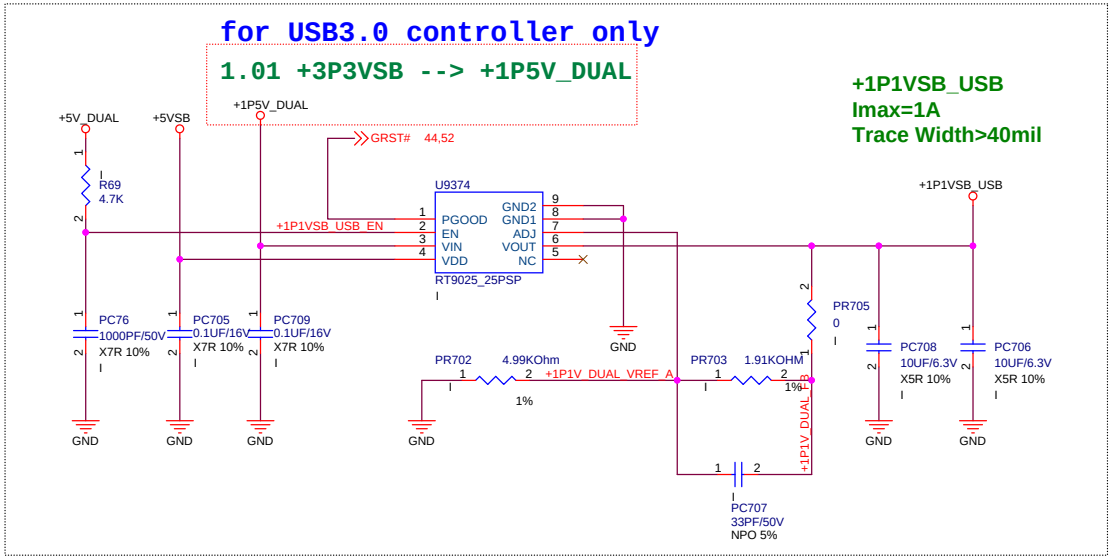
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : UVP, OVP & +19VSB

PEGATRON CORPORATION Engineer: Ethan_Chen

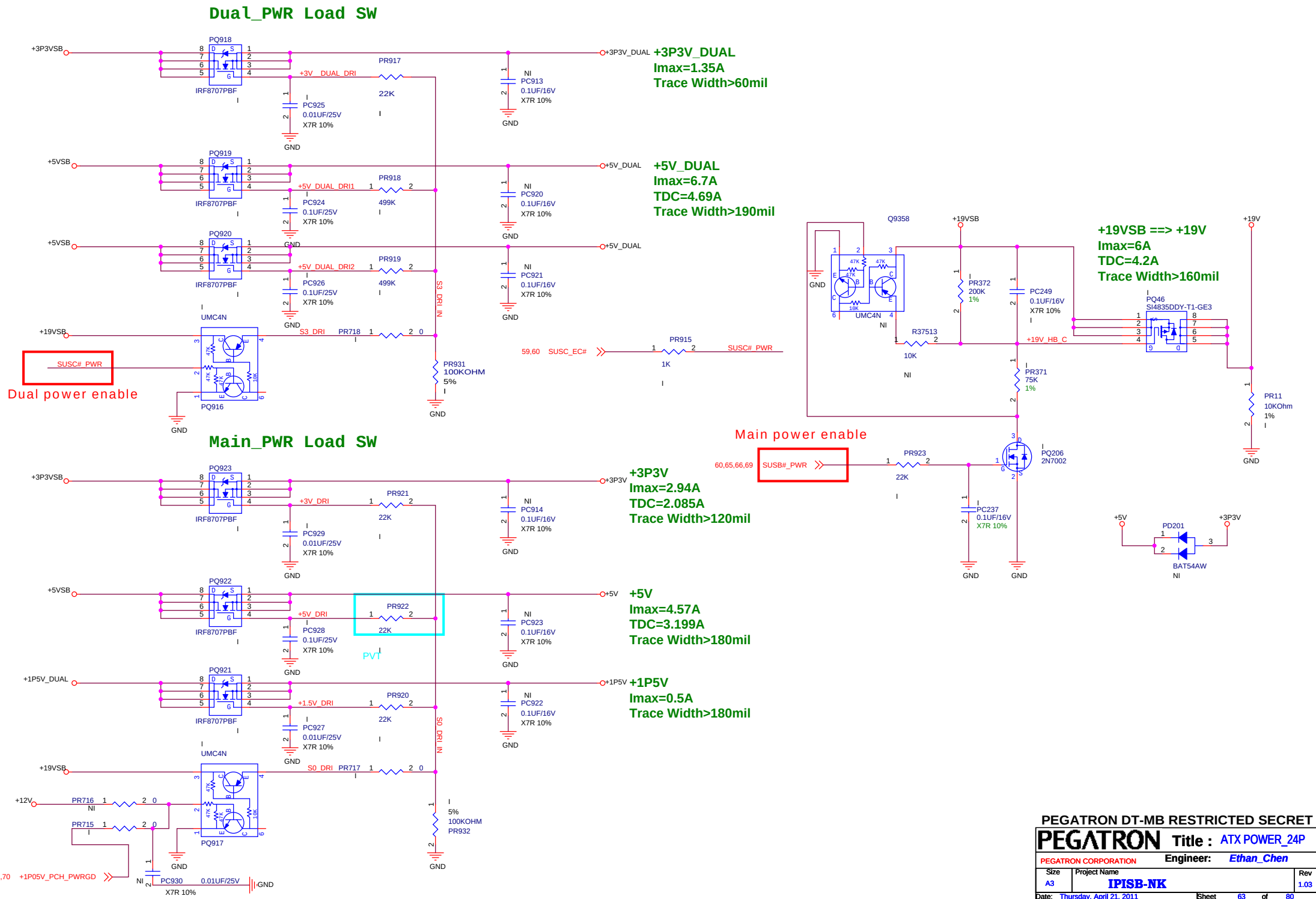
Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 61 of 80



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +1P1VSB_USB	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Thursday, April 21, 2011	Sheet 62 of 80	


Dual_PWR Load SW
+3P3VSB
PQ918
IRF8707PBF
PR917
22K
+3V_DUAL_DRI
PC925
0.01UF/25V
X7R 10%
GND
NI
PC913
0.1UF/16V
X7R 10%
+3P3V_DUAL
+3P3V_DUAL
Imax=1.35A
Trace Width>60mil
+5VSB
PQ919
IRF8707PBF
PR918
499K
+5V_DUAL_DRI1
PC924
0.1UF/25V
X7R 10%
NI
PC920
0.1UF/16V
X7R 10%
+5V_DUAL
+5V_DUAL
Imax=6.7A
TDC=4.69A
Trace Width>190mil
+5VSB
PQ920
IRF8707PBF
PR919
499K
+5V_DUAL_DRI2
PC926
0.1UF/25V
X7R 10%
NI
PC921
0.1UF/16V
X7R 10%
+5V_DUAL
UMC4N
+19VSB
S3_DRI
PR718
S3_DRI_IN
PR931
100KOHM
5%
SUSC# PWR
PQ916
Dual power enable
59,60 SUSC_EC#
PR915
1K
SUSC# PWR
Q9358
UMC4N
+19VSB
PR372
200K
1%
PC249
0.1UF/16V
X7R 10%
R37513
10K
NI
+19V_HB_C
PQ46
SI4835DDY-T1-GE3
PR371
75K
1%
+19V
PR11
10KOhm
1%
+19VSB ==> +19V
Imax=6A
TDC=4.2A
Trace Width>160mil
Main power enable
60,65,66,69 SUSB#_PWR
PR923
22K
PQ206
2N7002
PC237
0.1UF/16V
X7R 10%
+5V
PD201
+3P3V
BAT54AW
NI
Main_PWR Load SW
+3P3VSB
PQ923
IRF8707PBF
PR921
22K
+3V_DRI
PC929
0.01UF/25V
X7R 10%
NI
PC914
0.1UF/16V
X7R 10%
+3P3V
+3P3V
Imax=2.94A
TDC=2.085A
Trace Width>120mil
+5VSB
PQ922
IRF8707PBF
PR922
22K
+5V_DRI
PC928
0.1UF/25V
X7R 10%
PVT
NI
PC923
0.1UF/16V
X7R 10%
+5V
+5V
Imax=4.57A
TDC=3.199A
Trace Width>180mil
+1P5V_DUAL
PQ921
IRF8707PBF
PR920
22K
+1.5V_DRI
PC927
0.01UF/25V
X7R 10%
NI
PC922
0.1UF/16V
X7R 10%
+1P5V
+1P5V
Imax=0.5A
Trace Width>180mil
+19VSB
UMC4N
S0_DRI
PR717
S0_DRI_IN
PR932
5%
100KOHM
+12V
PR716
NI
PR715
PQ917
69,70 +1P05V_PCH_PWRGD
PC930
0.01UF/25V
X7R 10%
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : ATX POWER_24P
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Thursday, April 21, 2011
Sheet 63 of 80

+19VSB
Iin=3.27A
Trace Width>130mil

+5VSB
Imax=12.41A
TDC=8.687A
Trace Width>500mil

+19VSB
Iin=1.63A
Trace Width>65mil

+3P3VSB
Imax=9.43A
TDC=6.601A
Trace Width>380mil

EC power

EVT2

U9372
TPS51125ARGER

PEGATRON

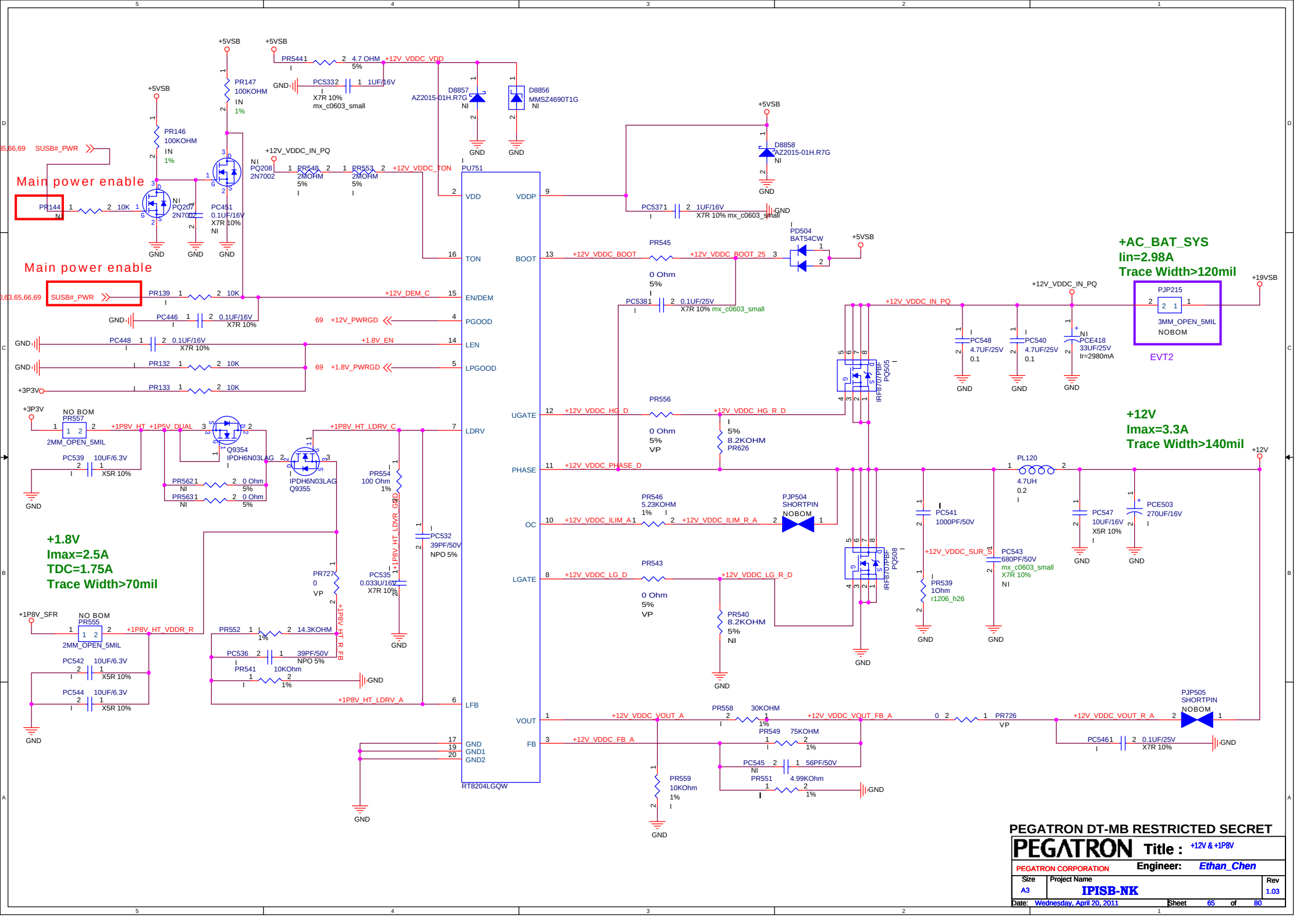
Title : +3VA&+3VSB&+5VSB

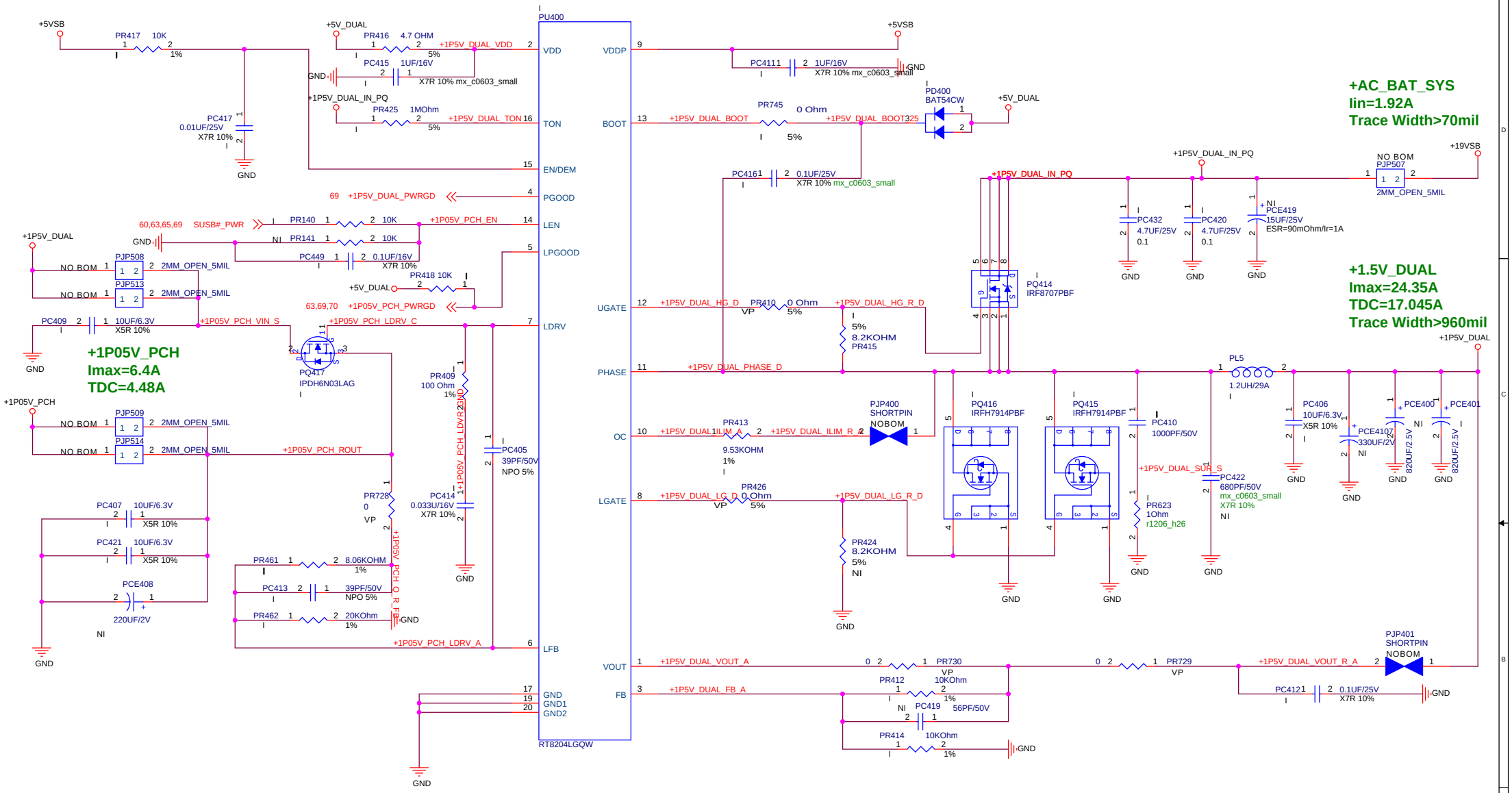
PEGATRON CORPORATION

Engineer: Ethan_Chen

Size	Project Name	Rev
Custom	IPISB-NK	1.03

Date: Thursday, April 21, 2011 Sheet 64 of 80


Main power enable
Main power enable
+1.8V
Imax=2.5A
TDC=1.75A
Trace Width>70mil
+AC_BAT_SYS
Iin=2.98A
Trace Width>120mil
EVT2
+12V
Imax=3.3A
Trace Width>140mil
RT8204LGQW
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : +12V & +1P8V
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Wednesday, April 20, 2011
Sheet 65 of 80



PEGATRON

Title : +1P5V_DUAL&+1P05V_PCH

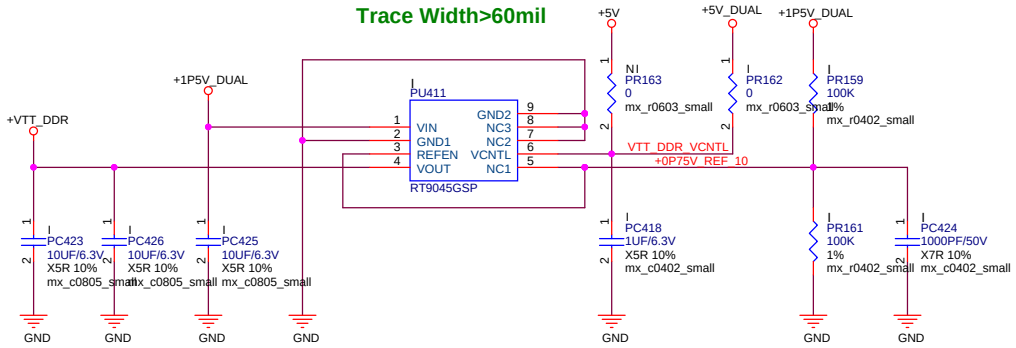
PEGATRON CORPORATION

Engineer: Ethan_Chen

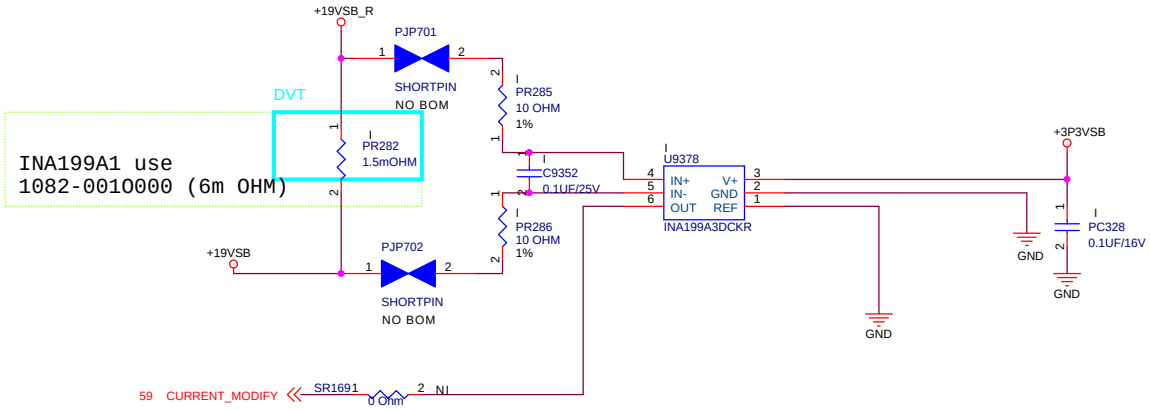
Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 66 of 80

+VTT_DDR
Imax=1.5A
Trace Width>60mil

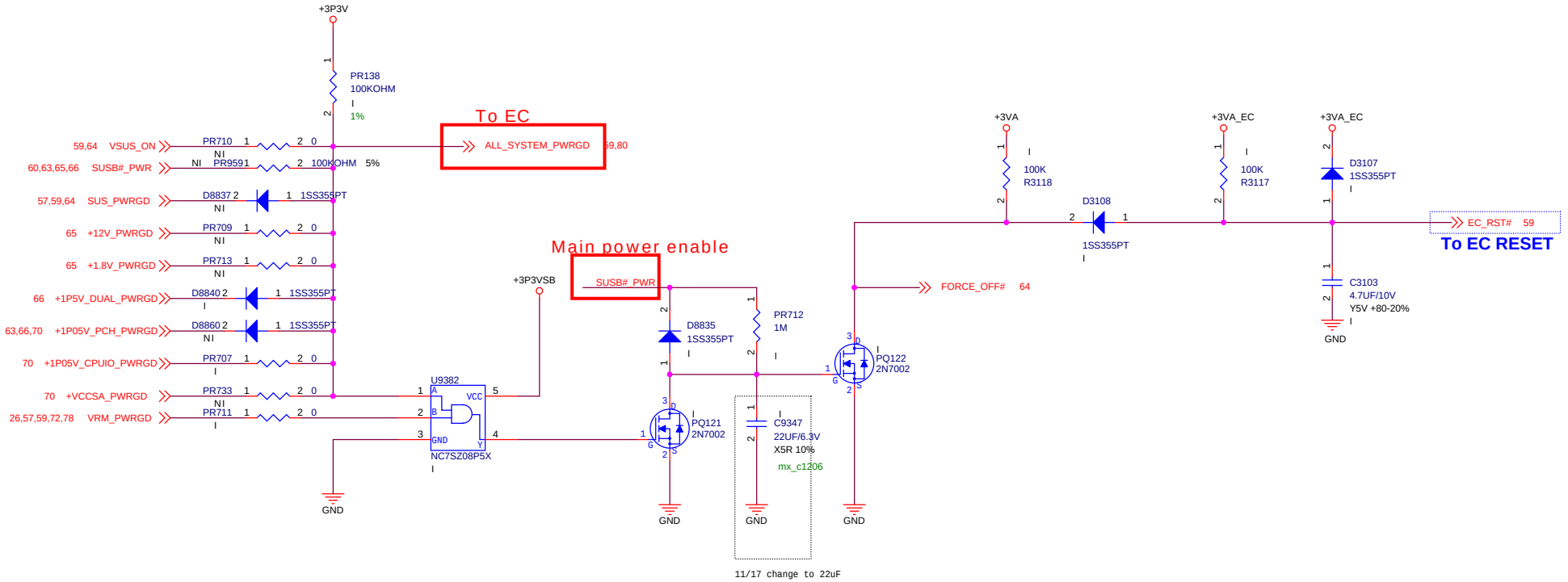


PEGATRON	Title : +VTT_DDR	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 67 of 80	

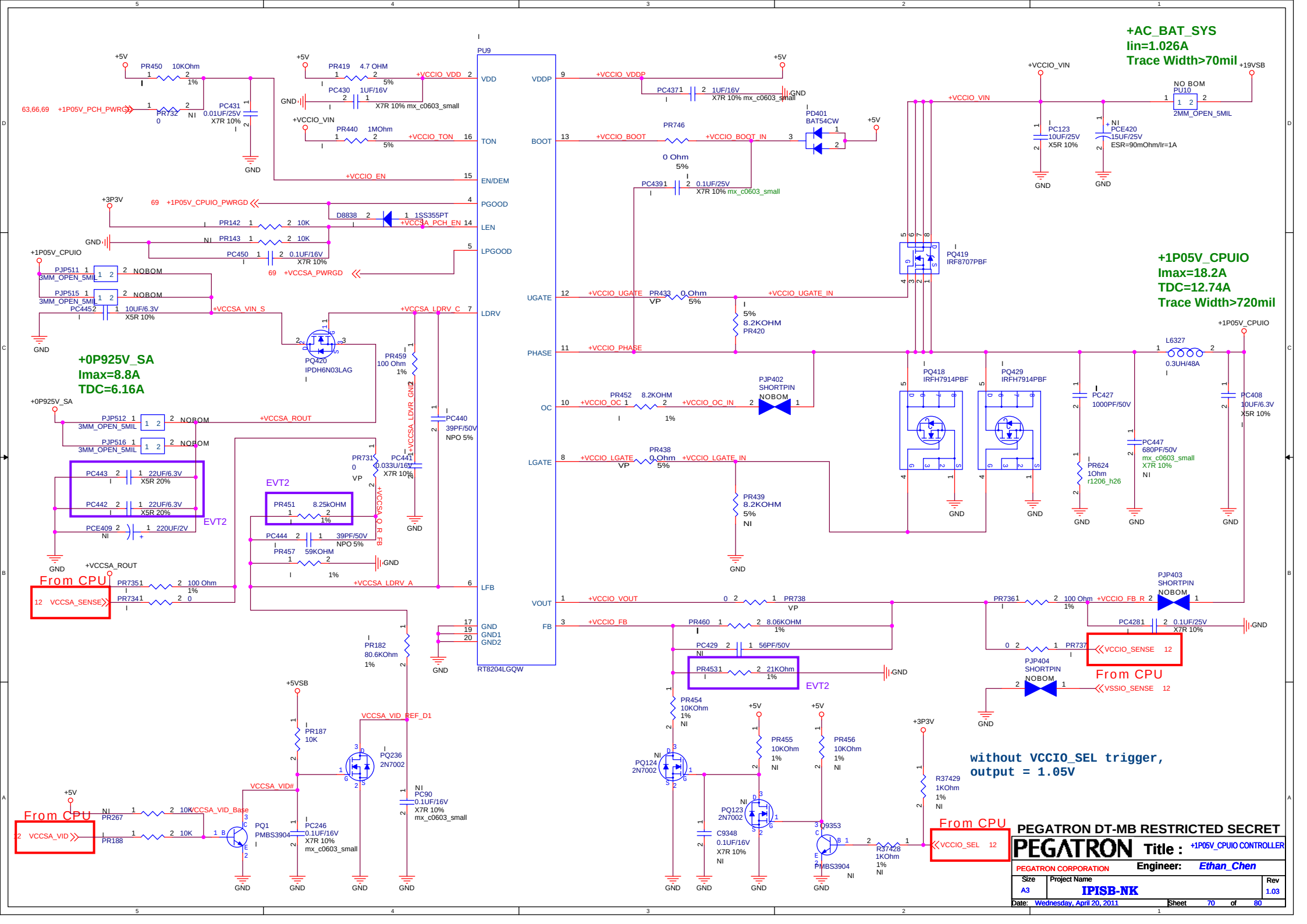


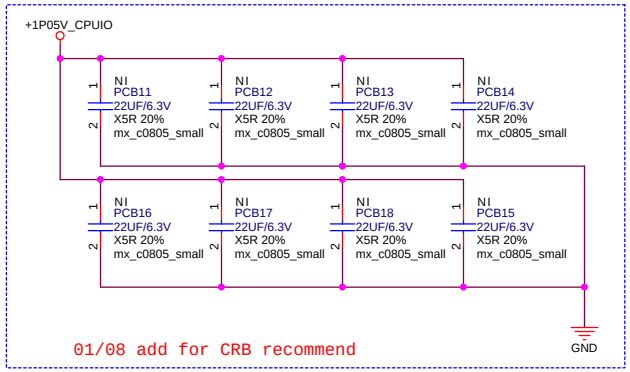
PEGATRON DT-MB RESTRICTED SECRET

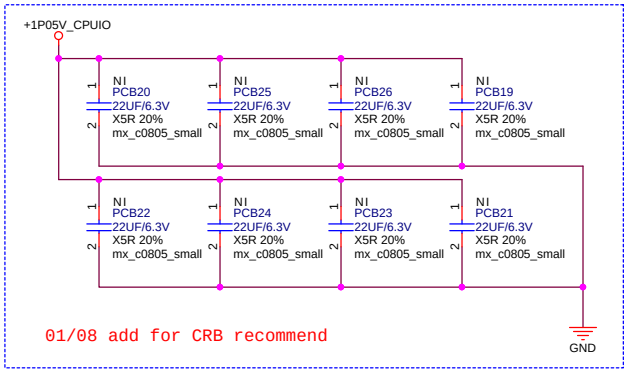
PEGATRON	Title : N/A	
PEGATRON CORPORATION	Engineer: Ethan_Chen	
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 68 of 80	

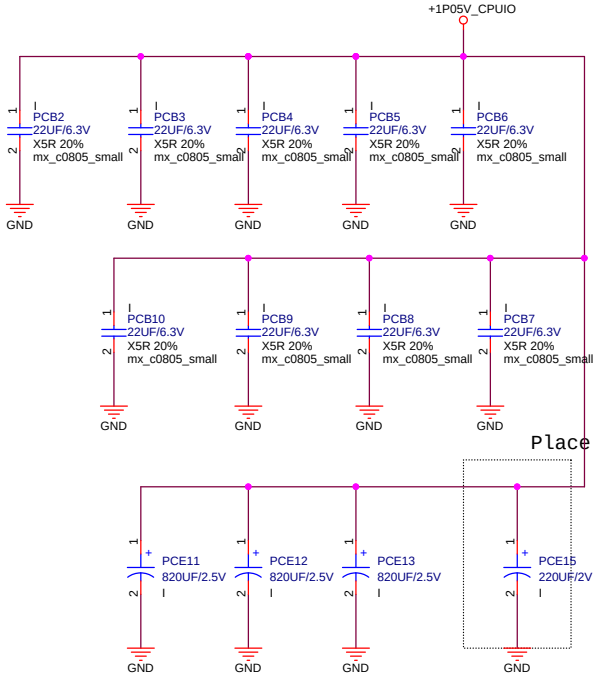


PEGATRON	Title :	+1P05V_ME
PEGATRON CORPORATION	Engineer:	Ethan_Chen
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 69 of 80	


+AC_BAT_SYS
Iin=1.026A
Trace Width>70mil
+1P05V_CPUIO
Imax=18.2A
TDC=12.74A
Trace Width>720mil
+0P925V_SA
Imax=8.8A
TDC=6.16A
PU9
RT8204LGQW
VDD
VDDP
TON
BOOT
EN/DEM
PGOOD
LEN
LPGOOD
UGATE
PHASE
LDRV
OC
LGATE
VOUT
FB
GND
GND1
GND2
LFB
+5V
+19VSB
+3P3V
+5VSB
+VCCIO_VIN
+VCCIO_VDD
+VCCIO_VDDP
+VCCIO_TON
+VCCIO_EN
+VCCIO_BOOT
+VCCIO_BOOT_IN
+VCCIO_UGATE
+VCCIO_UGATE_IN
+VCCIO_PHASE
+VCCIO_OC
+VCCIO_OC_IN
+VCCIO_LGATE
+VCCIO_LGATE_IN
+VCCIO_VOUT
+VCCIO_FB
+VCCIO_FB_R
+1P05V_PCH_PWRGD
+1P05V_CPUIO_PWRGD
+VCCSA_PCH_EN
+VCCSA_PWRGD
+VCCSA_VIN_S
+VCCSA_LDRV_C
+VCCSA_LDRV_A
+VCCSA_LDRV_GND
+VCCSA_ROUT
+VCCSA_OCP_FB
+1P05V_CPUIO
+0P925V_SA
PR450 10KOhm 1%
PR732 0 NI
PC431 0.01UF/25V X7R 10%
PR419 4.7 OHM 5%
PC430 1UF/16V X7R 10% mx_c0603_small
PR440 1MOhm 5%
PC4371 1UF/16V X7R 10% mx_c0603_small
PR746 0 Ohm 5%
PC4391 0.1UF/25V X7R 10% mx_c0603_small
PD401 BAT54CW
PC123 10UF/25V X5R 10%
PCE420 15UF/25V ESR=90mOhm/Ir=1A
NO BOM PU10 2MM_OPEN_5MIL
PR142 10K
PR143 10K NI
PC450 0.1UF/16V X7R 10%
D8838 1SS355PT
PJP511 3MM_OPEN_5MIL NOBOM
PJP515 3MM_OPEN_5MIL NOBOM
PC4452 10UF/6.3V X5R 10%
PQ420 IPDH6N03LAG
PR459 100 Ohm 1%
PC440 39PF/50V NPO 5%
PR433 0 Ohm 5% VP
PR420 8.2KOHM 5%
PQ419 IRF8707PBF
PQ418 IRFH7914PBF
PQ429 IRFH7914PBF
L6327 0.3UH/48A
PC427 1000PF/50V
PC447 680PF/50V mx_c0603_small X7R 10% NI
PR624 1Ohm r1206_h26
PC408 10UF/6.3V X5R 10%
PR452 8.2KOHM 1%
PJP402 SHORTPIN NOBOM
PR439 8.2KOHM 5% NI
PR438 0 Ohm 5% VP
PJP512 3MM_OPEN_5MIL NOBOM
PJP516 3MM_OPEN_5MIL NOBOM
PC443 22UF/6.3V X5R 20%
PC442 22UF/6.3V X5R 20%
PCE409 220UF/2V NI
EVT2
PR731 0 VP
PC441 0.033U/16V X7R 10%
PR451 8.25kOHM 1%
PC444 39PF/50V NPO 5%
PR457 59KOHM 1%
From CPU
12 VCCSA_SENSE
PR7351 100 Ohm 1%
PR7341 0
PR182 80.6KOHM 1%
PR460 8.06KOHM 1%
PC429 56PF/50V NI
PR4531 21KOhm 1%
PR454 10KOhm 1% NI
PR455 10KOhm 1% NI
PR456 10KOhm 1% NI
PQ124 2N7002 NI
PQ123 2N7002 NI
C9348 0.1UF/16V X7R 10% NI
Q9353 PMBS3904 NI
R37429 1KOhm 1% NI
R37428 1KOhm 1% NI
PR7361 100 Ohm 1%
PC4281 0.1UF/25V X7R 10%
PR737
PJP403 SHORTPIN NOBOM
PJP404 SHORTPIN NOBOM
VCCIO_SENSE 12
VSSIO_SENSE 12
From CPU
VCCSA_VID_REF_D1
PR187 10K
PQ236 2N7002
VCCSA_VID#
VCCSA_VID_Base
PR267 10K NI
PR188 10K
PQ1 PMBS3904
PC246 0.1UF/16V X7R 10% mx_c0603_small
NI PC90 0.1UF/16V X7R 10% mx_c0603_small
From CPU
VCCSA_VID 12
From CPU
VCCIO_SEL 12
without VCCIO_SEL trigger,
output = 1.05V
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : +1P05V_CPUIO CONTROLLER
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Wednesday, April 20, 2011
Sheet 70 of 80







VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22µF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2 3
0805 placeholders	16				Backside	

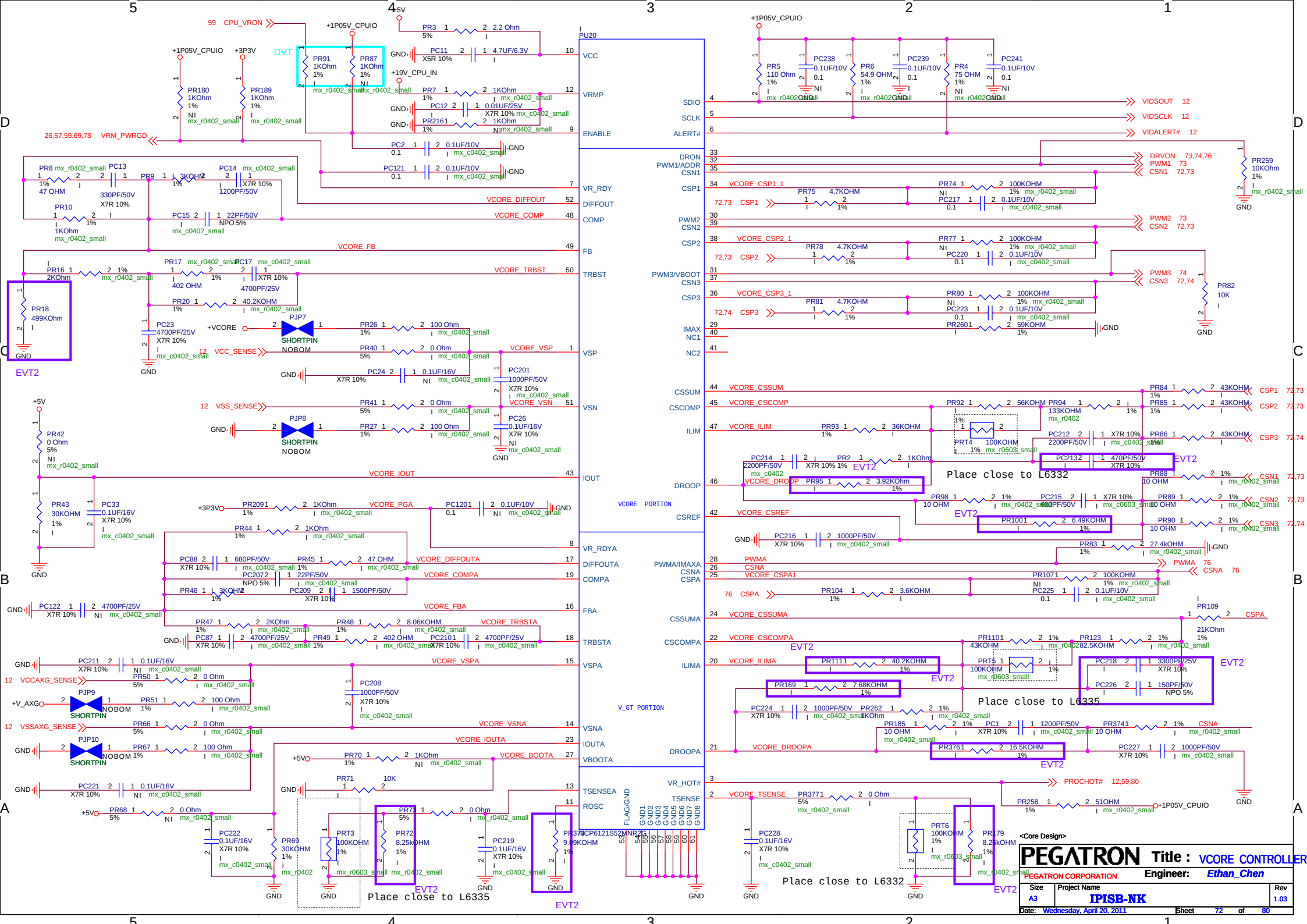
PEGATRON DT-MB RESTRICTED SECRET

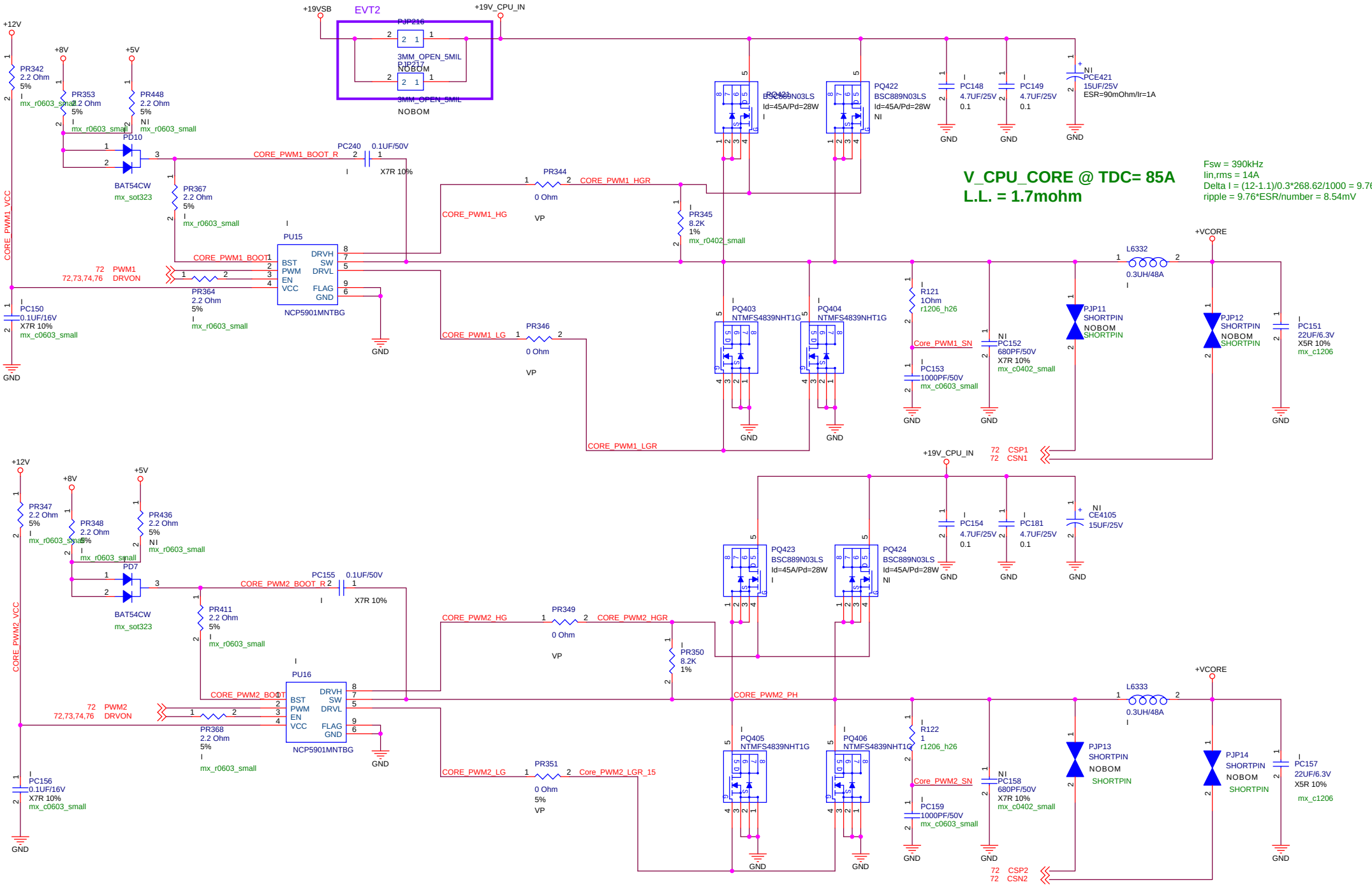
PEGATRON Title : 1P05V_CPUIO CAP

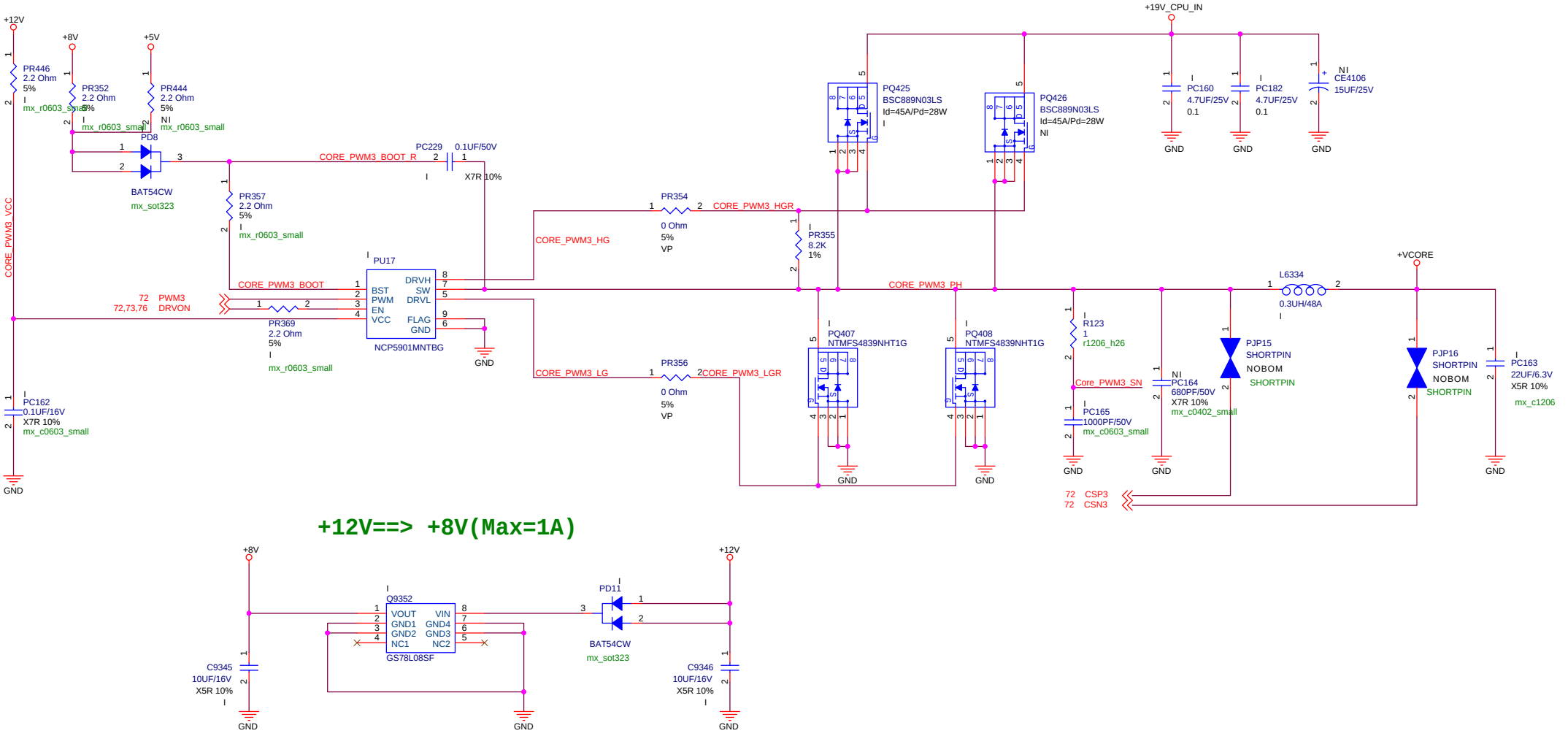
PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 71 of 80


PU20
VCC
VRMP
ENABLE
VR_RDY
DIFFOUT
COMP
FB
TRBST
VSP
VSN
IOUT
VR_RDYA
DIFFOUTA
COMPA
FBA
TRBSTA
VSPA
VSNA
IOUTA
VBOOTA
TSENSEA
ROSC
SDIO
SCLK
ALERT#
DRON
PWM1/ADDR
CSN1
CSP1
PWM2
CSN2
CSP2
PWM3/VBOOT
CSN3
CSP3
IMAX
NC1
NC2
CSSUM
CSCOMP
ILIM
DROOP
CSREF
PWMA/IMAXA
CSNA
CSPA
CSSUMA
CSCOMPA
ILIMA
DROOPA
VR_HOT#
TSENSE
FLAG/GND
VCORE PORTION
V_GT PORTION
MCP6121S52MNR2G
Place close to L6332
Place close to L6335
Place close to L6332
Place close to L6335
EVT2
DVT
<Core Design>
PEGATRON
Title : VCORE CONTROLLER
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Wednesday, April 20, 2011
Sheet 72 of 80


+19VSB
EVT2
+19V_CPU_IN
PJP216
3MM_OPEN_5MIL
PJ6217
NOBOM
+12V
+8V
+5V
PR342 2.2 Ohm 5%
PR353 2.2 Ohm 5%
PR448 2.2 Ohm 5%
PD10
BAT54CW
mx_sot323
PC240 0.1UF/50V
X7R 10%
CORE_PWM1_BOOT_R
CORE_PWM1_VCC
PR367 2.2 Ohm 5%
PR364 2.2 Ohm 5%
PU15
NCP5901MNTBG
DRVH
SW
DRVL
BST
PWM
EN
VCC
FLAG
GND
CORE_PWM1_BOOT
CORE_PWM1_HG
CORE_PWM1_HGR
CORE_PWM1_LG
CORE_PWM1_LGR
PR344 0 Ohm
PR345 8.2K 1%
PR346 0 Ohm
PQ421 BSC889N03LS Id=45A/Pd=28W
PQ422 BSC889N03LS Id=45A/Pd=28W
PQ403 NTMFS4839NHT1G
PQ404 NTMFS4839NHT1G
PC148 4.7UF/25V 0.1
PC149 4.7UF/25V 0.1
PCE421 15UF/25V ESR=90mOhm/Ir=1A
R121 1Ohm r1206_h26
Core_PWM1_SN
PC152 680PF/50V X7R 10%
PC153 1000PF/50V
L6332 0.3UH/48A
+VCORE
PJP11 SHORTPIN NOBOM SHORTPIN
PJP12 SHORTPIN NOBOM SHORTPIN
PC151 22UF/6.3V X5R 10%
PC150 0.1UF/16V X7R 10%
72 PWM1
72,73,74,76 DRVON
72 CSP1
72 CSN1
V_CPU_CORE @ TDC= 85A
L.L. = 1.7mohm
Fsw = 390kHz
Iin,rms = 14A
Delta I = (12-1.1)/0.3*268.62/1000 = 9.76A
ripple = 9.76*ESR/number = 8.54mV
PR347 2.2 Ohm 5%
PR348 2.2 Ohm 5%
PR436 2.2 Ohm 5%
PD7
PC155 0.1UF/50V
CORE_PWM2_BOOT_R
CORE_PWM2_VCC
PR411 2.2 Ohm 5%
PR368 2.2 Ohm 5%
PU16
CORE_PWM2_BOOT
CORE_PWM2_HG
CORE_PWM2_HGR
CORE_PWM2_LG
CORE_PWM2_LGR
CORE_PWM2_PH
PR349 0 Ohm
PR350 8.2K 1%
PR351 0 Ohm 5%
Core_PWM2_LGR_15
PQ423 BSC889N03LS Id=45A/Pd=28W
PQ424 BSC889N03LS Id=45A/Pd=28W
PQ405 NTMFS4839NHT1G
PQ406 NTMFS4839NHT1G
PC154 4.7UF/25V 0.1
PC181 4.7UF/25V 0.1
CE4105 15UF/25V
R122 1 r1206_h26
Core_PWM2_SN
PC158 680PF/50V X7R 10%
PC159 1000PF/50V
L6333 0.3UH/48A
PJP13 SHORTPIN NOBOM SHORTPIN
PJP14 SHORTPIN NOBOM SHORTPIN
PC157 22UF/6.3V X5R 10%
PC156 0.1UF/16V X7R 10%
72 PWM2
72,73,74,76 DRVON
72 CSP2
72 CSN2
GND
VP
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : VCORE DRIVER1-2
Pegatron Corp.
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Wednesday, April 20, 2011
Sheet 73 of 80



+12V==> +8V(Max=1A)

PEGATRON DT-MB RESTRICTED SECRET

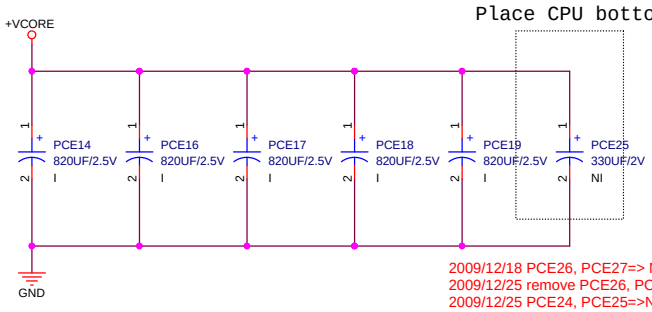
PEGATRON Pegatron Corp.	Title : VCORE DRIVER 2-2	
	Engineer: Ethan_Chen	
Size: A3	Project Name: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 74 of 80	

Output CAP

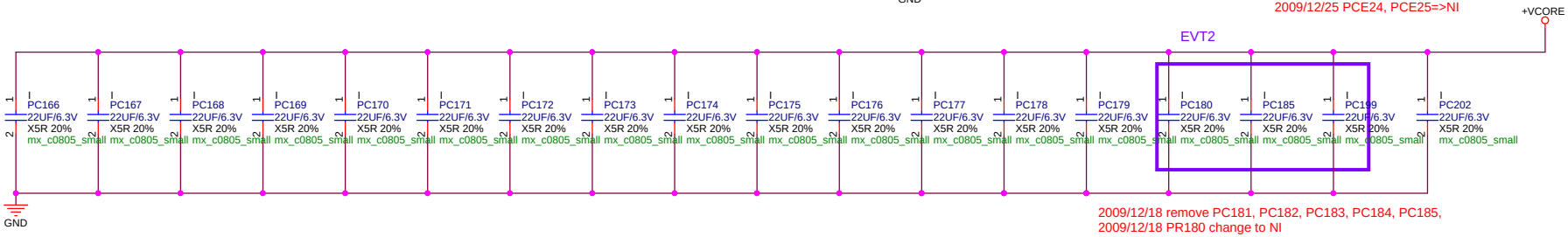
Table 10-2. Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

PL-CAP *4 +2(NI)
MLCC *18 +3(NI)



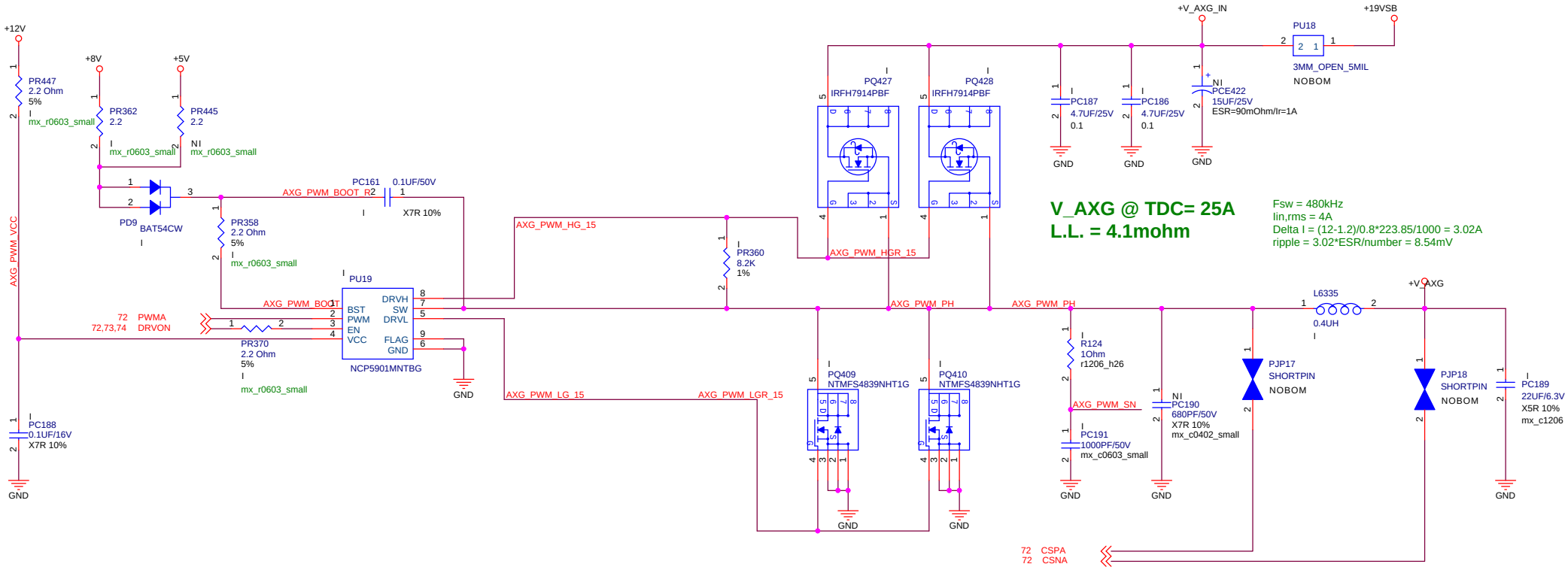
2009/12/18 PCE26, PCE27=> NI
2009/12/25 remove PCE26, PCE27
2009/12/25 PCE24, PCE25=>NI



2009/12/18 remove PC181, PC182, PC183, PC184, PC185,
2009/12/18 PR180 change to NI
2009/12/21 PR180 change to I
2009/12/21 add PC185, PC199
2009/12/25 add PC200, PC201, PC202,
2009/01/09 remove PC200, PC201

<Core Design>

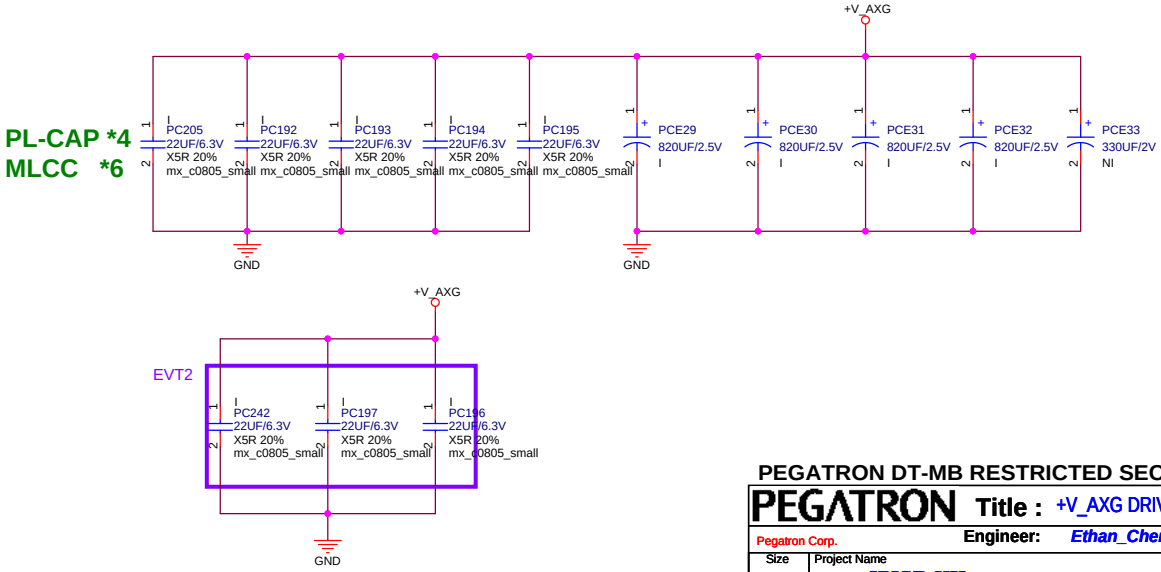
Title: <Title>		
Size: A3	Document Number: IPISB-NK	Rev: 1.03
Date: Wednesday, April 20, 2011	Sheet 75 of 80	



Output CAP

Table 30-4. VCCAXG Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2 3
4.7µF X5R	3	7mΩ	0.6nH	Input		1



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +V_AXG DRIVER

Pegatron Corp. Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 76 of 80

PEGATRON

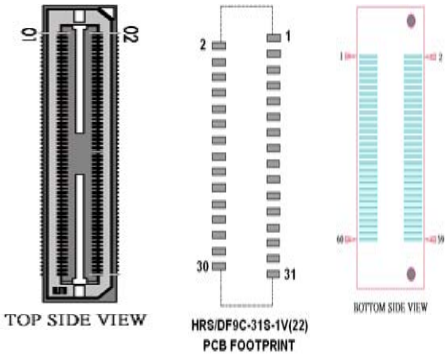
Title : PLTRST_CPU#&SMbus

PEGATRON CORPORATION

Engineer: *Ethan_Chen*

Size	Project Name	Rev
A	**IPISB-NK**	1.03

Date: Wednesday, April 20, 2011 Sheet 77 of 80



INTEL CPU XDP DEBUG PORT

NI
XDP1

+1P05V_CPUIO
PROTO
HCB20
0.1UF/16V
GND

VCC_OBS_AB
VCC_OBS_CD

TCK1 TCK0 TDO TRSTn TDI TMS
TCK 12
TDO 12
TRST# 12
TDI 12
TMS 12

+1P05V_CPUIO
NI
HR61
1.5K
PROTO
HR62
249 1%
HOOK0 CPUXDP_HOOK0
CPUPWRGD 12,26

+1P05V_CPUIO
NI
HR63
1K

NOTE:
Place HR64 near HR24, reduce stub

12 H_PREQ#
12 H_PRDY#
12 BPM0#
12 BPM1#
12 BPM2#
12 BPM3#
OBSFN_A0
OBSFN_A1
OBSDATA_A0
OBSDATA_A1
OBSDATA_A2
OBSDATA_A3

OBSFN_B0
OBSFN_B1
OBSDATA_B0
OBSDATA_B1
OBSDATA_B2
OBSDATA_B3
12 BPM4#
12 BPM5#
12 BPM6#
12 BPM7#

NOTE:
CRB is BTM

28 CK_100M_CPUXDP
28 CK_100M_CPUXDP#
PROTO HR68
PROTO HR69
CPU_XDPCLK
CPU_XDPCLK#
PROTO HR72
PROTO HR73
CPU_ITPCLK_HOOK4
CPU_ITPCLK#_HOOK5
ITPCLK/HOOK4
ITPCLK#/HOOK5

12 CK_100M_CPU_XDP
12 CK_100M_CPU_XDP#
NI HR74
NI HR75

NOTE:
Please close to each other to reduse stub.

HOOK1 CPUXDP_HOOK1
HOOK2 CPUXDP_HOOK2
HOOK3 CPUXDP_HOOK3
HOOK6/RESET#
HOOK7/DBR#
PROTO HR66 3.3K
PROTO HR64 1K
PROTO HR67 0
PWRBTN# 54,59,79
CPU_CFG0 12
VRM_PWRGD 26,57,59,69,72
CPURST_XDP# 18,79
SYS_RESET_DBR# 12,79

15,16,47,48,55,79 SMB_DATA_M
15,16,47,48,55,79 SMB_CLK_M
SDA
SCL

OBSFN_C0
OBSFN_C1
OBSDATA_C0
OBSDATA_C1
OBSDATA_C2
OBSDATA_C3

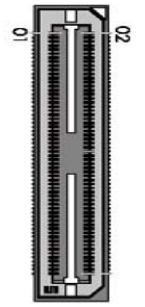
OBSFN_D0
OBSFN_D1
OBSDATA_D0
OBSDATA_D1
OBSDATA_D2
OBSDATA_D3

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18
NP_NC1
NP_NC2
NC
GND

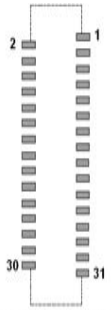
BtoB_CON_60P

PEGATRON CORPORATION
Title : CPU XDP DEBUG
Engineer: Ethan_Chen
Size A3
Project Name IPISB-NK
Rev 1.03
Date: Wednesday, April 20, 2011
Sheet 78 of 80

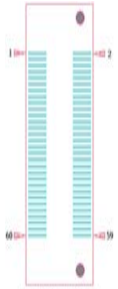
INTEL PCH XDP DEBUG PORT



TOP SIDE VIEW



HRS/DF9C-31S-1V(22)
PCB FOOTPRINT


BOTTOM SIDE VIEW

NOTE:
Place strap resistors of TDO near to XDP connector,
and TDI and TMS near to CPU.

TBD

NOTE:
Place SR214 near to source in order to avoid stub.

NI
XDP2
BtoB_CON_60P

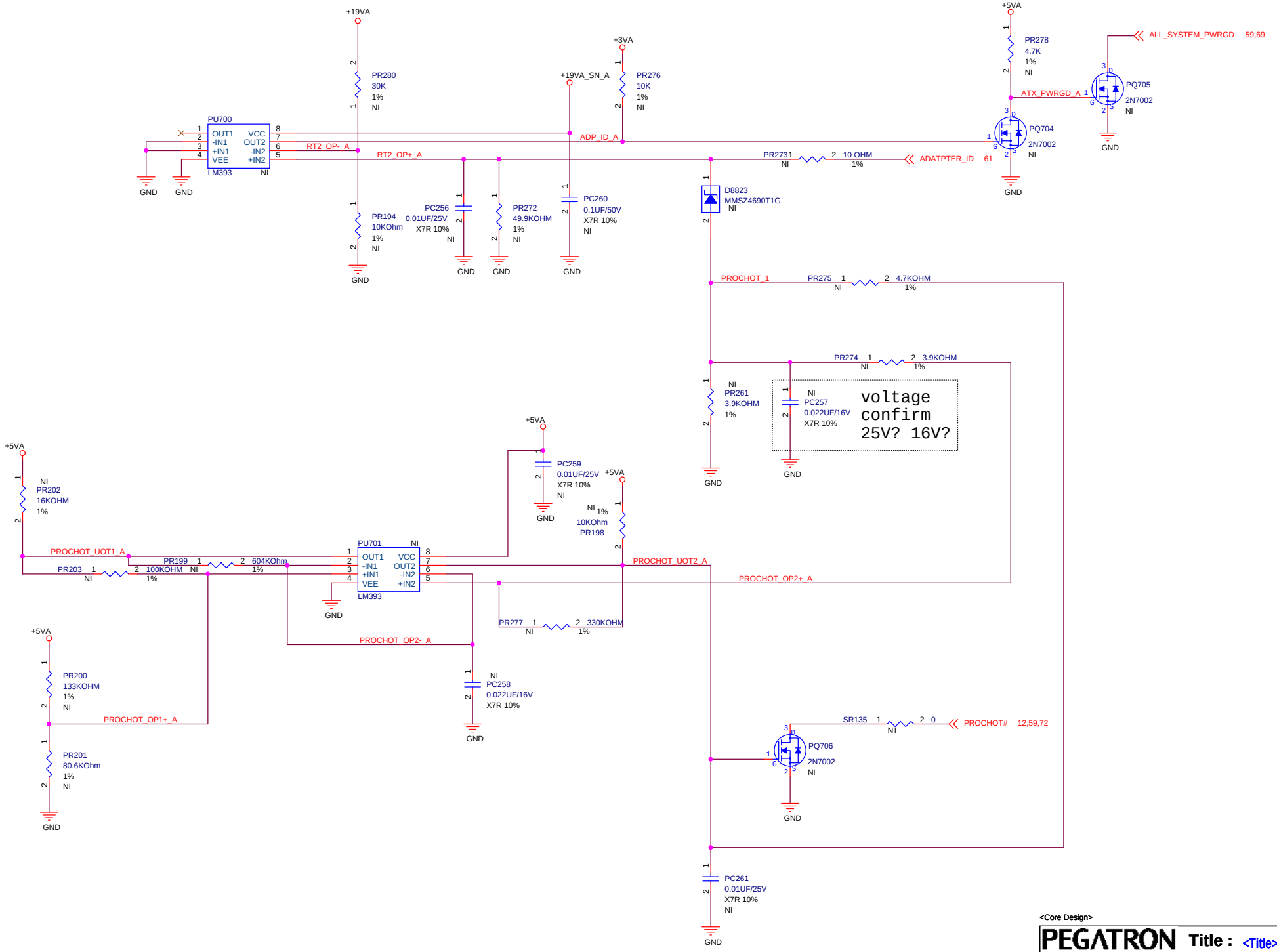
+3P3VSB
+3VA
+1P05V_PCH
+1P05V_CPUIO
GND
NC

PROTO SR200 0
NI SCB80 0.1UF/16V
PROTO SR202 0 mx_r0805_small
3P3VSB_CPUXDP_JTAG
NI SR204 200
NI SR206 200
NI SR208 200
NI SR184 20K
PROTO SR210 1K
NI SR211 0
PROTO SR201 0
PROTO SR212 51
NI SCB34 0.1UF/16V
PROTO SR203 51
PROTO SR205 100
PROTO SR207 100
PROTO SR209 100
PROTO SR258 10K
NI SCB17 1UF/10V mx_c0603_small
NI SR213 0
PROTO SR214 0
NI SR215 0
NI SR221 0
PROTO SR260 0
SR296 0 PROTO
NI SR216 0
NI SR250 0

PCH_JTAG_TCK 26
PCH_JTAG_TDO 26
PCH_JTAG_RST 26
PCH_JTAG_TDI 26
PCH_JTAG_TMS 26
PCH_JTAG_RST_R
PCHXDP_VCC_OBS
PCHXDP_HOOK0_PWRGD
PCHXDP_HOOK1
PCHXDP_ITPCLK/HOOK4
PCHXDP_HOOK6/RESET#
HOOK7_DBR#
PCHXDP_GND18
SYS_RESET_DBR# 12,78
CK_100M_PCHXDP 28
CK_100M_PCHXDP# 28
PWRBTN# 54,59,78
PLTRST# 18,26,49,59
CPURST_XDP# 18,78
DPWROK 18,26,59
15,16,47,48,55,78 SMB_DATA_M
15,16,47,48,55,78 SMB_CLK_M

VCC_OBS_AB
VCC_OBS_CD
TCK1
TCK0
TDO
TRSTn
TDI
TMS
HOOK0
HOOK1
HOOK2
HOOK3
HOOK6/RESET#
HOOK7/DBR#
OBSFN_A0
OBSFN_A1
OBSDATA_A0
OBSDATA_A1
OBSDATA_A2
OBSDATA_A3
OBSFN_B0
OBSFN_B1
OBSDATA_B0
OBSDATA_B1
OBSDATA_B2
OBSDATA_B3
ITPCLK/HOOK4
ITPCLK#/HOOK5
SDA
SCL
OBSFN_C0
OBSFN_C1
OBSDATA_C0
OBSDATA_C1
OBSDATA_C2
OBSDATA_C3
OBSFN_D0
OBSFN_D1
OBSDATA_D0
OBSDATA_D1
OBSDATA_D2
OBSDATA_D3
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
GND18
NP_NC1
NP_NC2

PEGATRON
Title : PCH XDP DEBUG
PEGATRON CORPORATION
Engineer: Ethan_Chen
Size: A3
Project Name: IPISB-NK
Rev: 1.03
Date: Wednesday, April 20, 2011
Sheet 79 of 80


+19VA
PR280
30K
1%
NI
PU700
OUT1
-IN1
+IN1
VEE
VCC
OUT2
-IN2
+IN2
LM393
NI
RT2_OP- A
RT2_OP+ A
PR194
10KOhm
1%
NI
PC256
0.01UF/25V
X7R 10%
NI
PR272
49.9KOHM
1%
NI
+19VA_SN_A
+3VA
PR276
10K
1%
NI
PC260
0.1UF/50V
X7R 10%
NI
ADP_ID_A
D8823
MMSZ4690T1G
NI
PR2731
NI
10 OHM
1%
ADATPTER_ID
61
+5VA
PR278
4.7K
1%
NI
ATX_PWRGD_A
PQ705
2N7002
NI
ALL_SYSTEM_PWRGD
59,69
PQ704
2N7002
NI
GND
PROCHOT_1
PR275
NI
4.7KOHM
1%
PR274
NI
3.9KOHM
1%
NI
PR261
3.9KOHM
1%
NI
PC257
0.022UF/16V
X7R 10%
voltage
confirm
25V? 16V?
+5VA
NI
PR202
16KOHM
1%
PROCHOT_UOT1_A
PR199
604KOhm
1%
PR203
NI
100KOHM
1%
PU701
NI
PROCHOT_UOT2_A
PROCHOT_OP2+ A
PROCHOT_OP2- A
PC259
0.01UF/25V
X7R 10%
NI
NI
1%
10KOhm
PR198
PR277
NI
330KOHM
1%
PR200
133KOHM
1%
NI
PROCHOT_OP1+ A
PR201
80.6KOhm
1%
NI
NI
PC258
0.022UF/16V
X7R 10%
SR135
NI
0
PROCHOT#
12,59,72
PQ706
2N7002
NI
PC261
0.01UF/25V
X7R 10%
NI
<Core Design>
PEGATRON
Title : <Title>
<OrgName>
Engineer: Ethan_Chen
Size
A3
Project Name
IPISB-NK
Rev
1.03
Date: Wednesday, April 20, 2011
Sheet 80 of 80