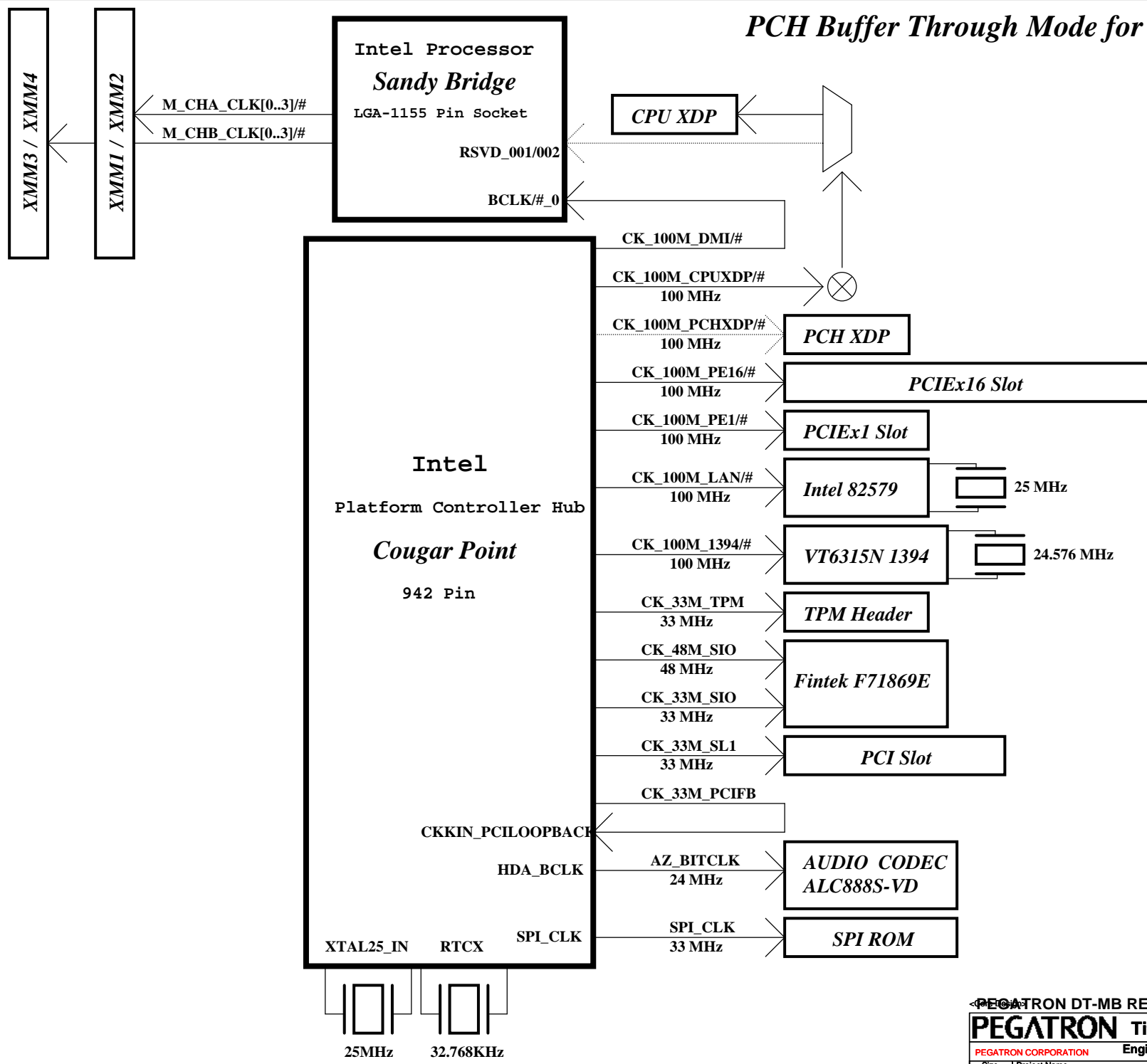
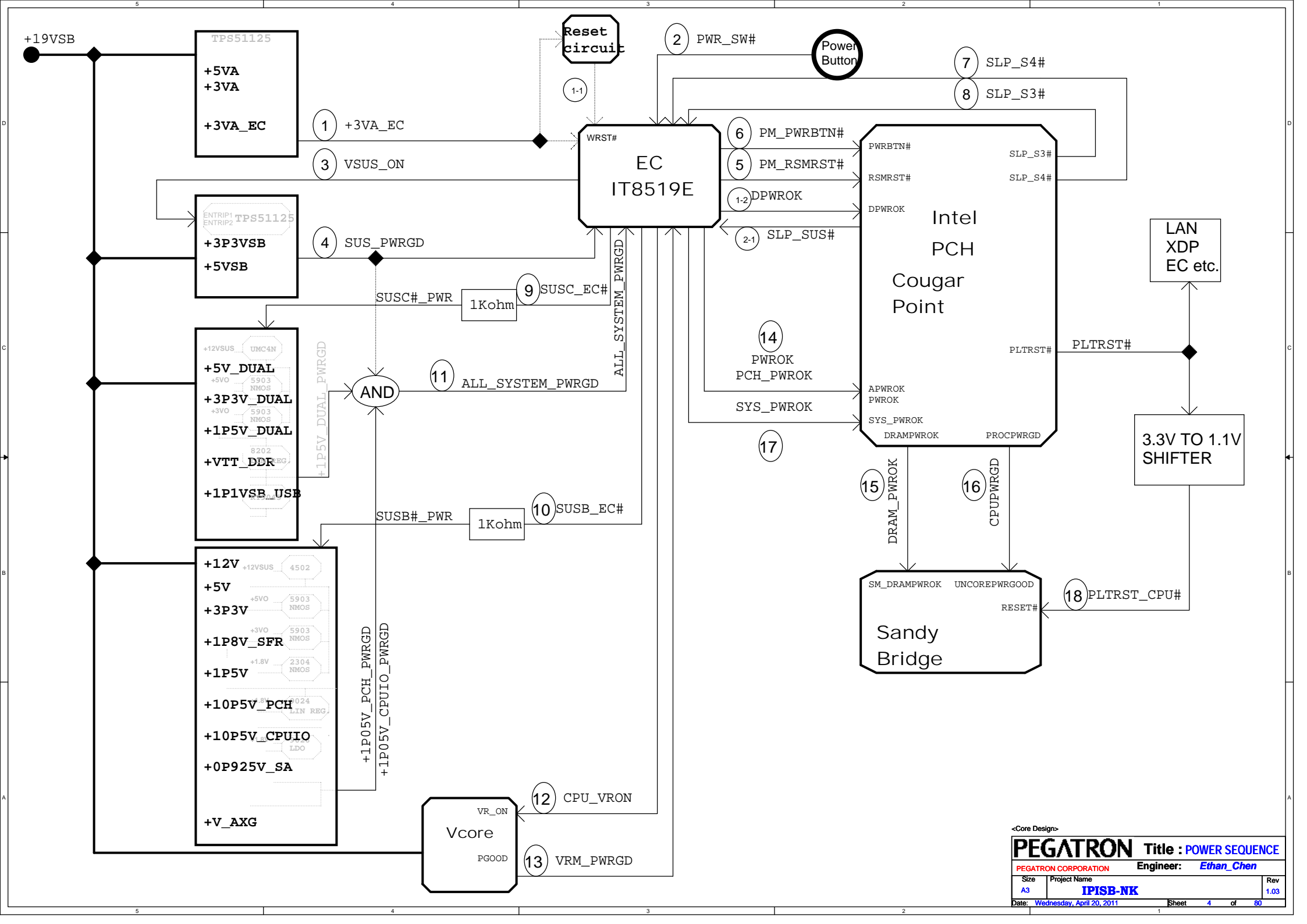
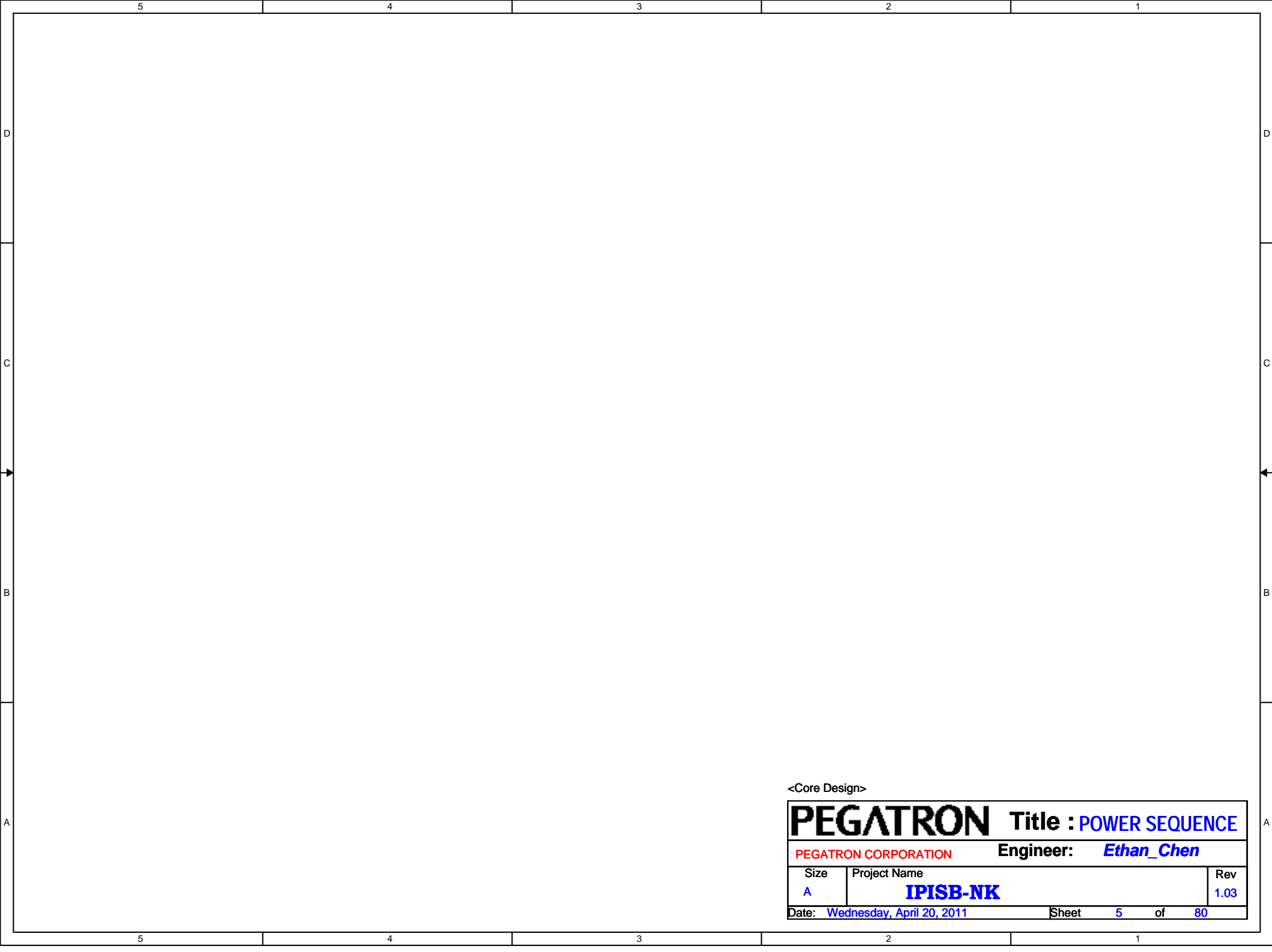


PCH Buffer Through Mode for Pre-Silicon

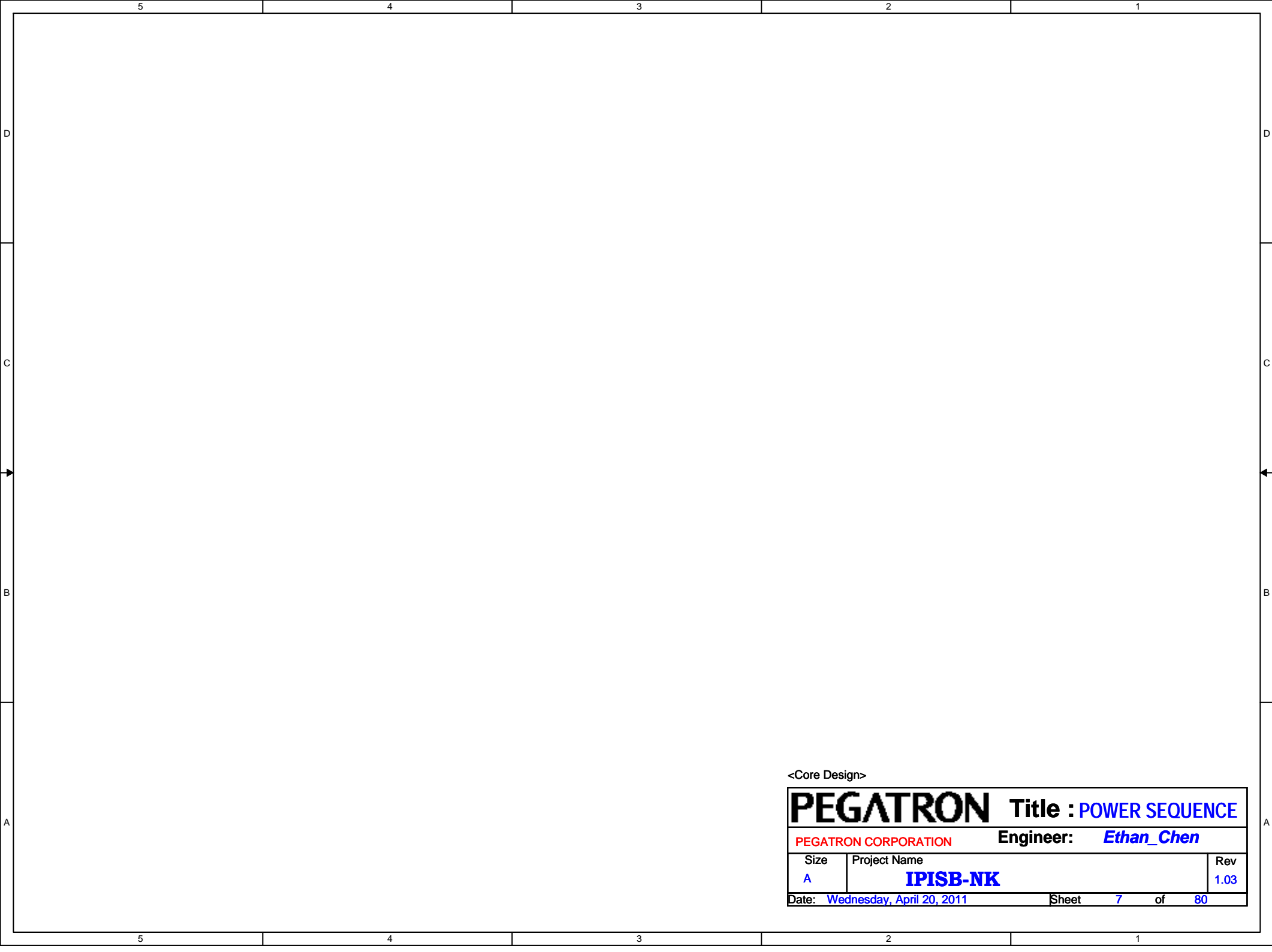






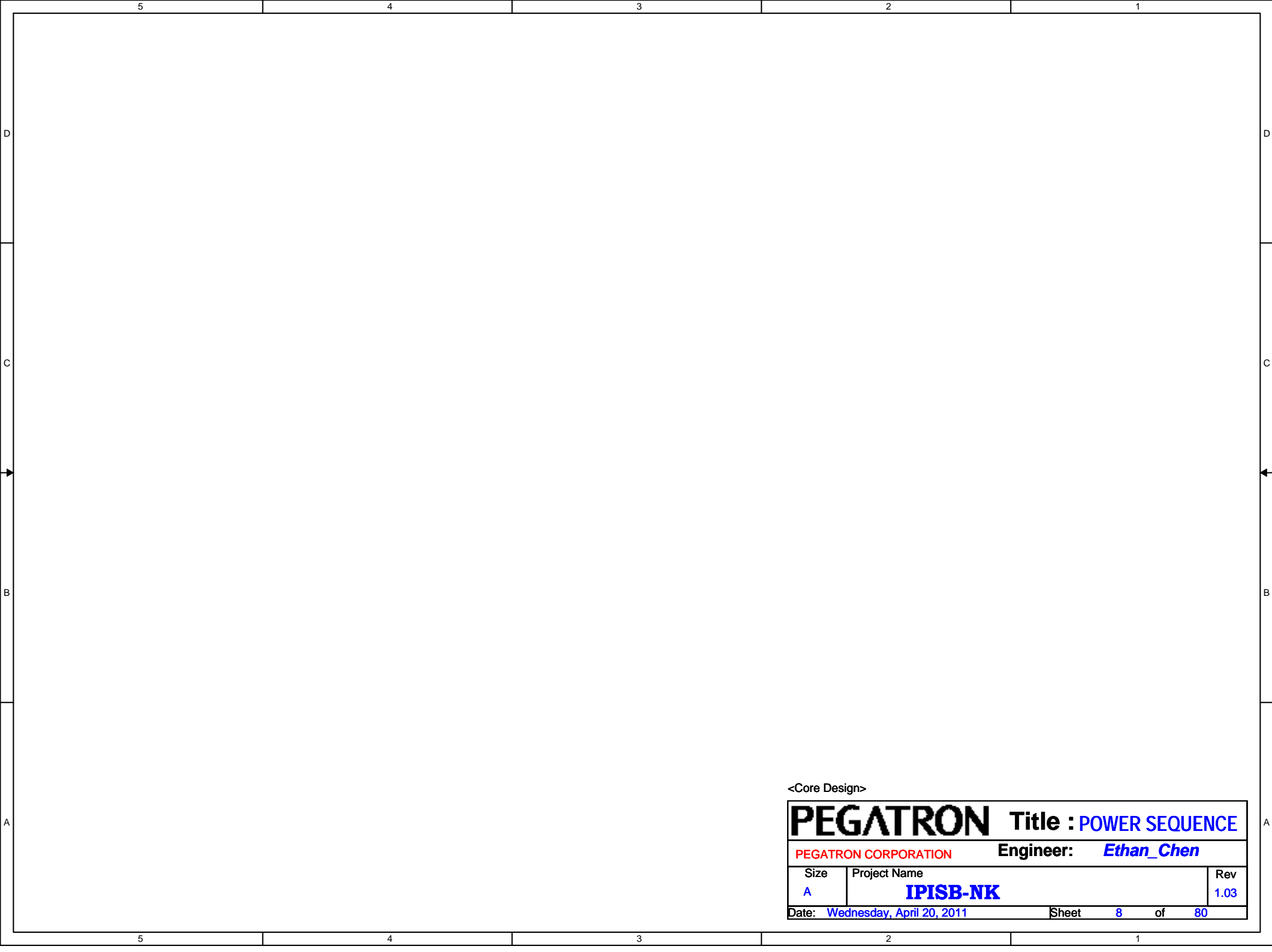
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PEGATRON		Title : POWER SEQUENCE	
PEGATRON CORPORATION		Engineer: Ethan_Chen	
Size A	Project Name IPISB-NK		Rev 1.03
Date: Wednesday, April 20, 2011		Sheet 5 of 80	



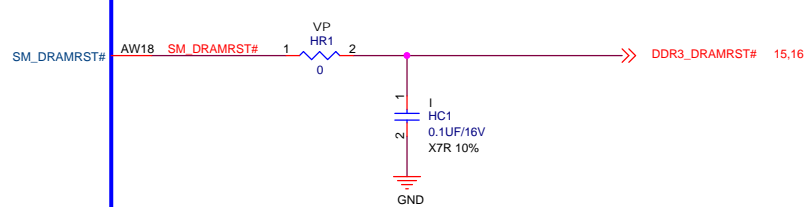
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PEGATRON		Title : POWER SEQUENCE	
PEGATRON CORPORATION		Engineer: Ethan_Chen	
Size	Project Name		Rev
A	IPISB-NK		1.03
Date: Wednesday, April 20, 2011		Sheet	7 of 80

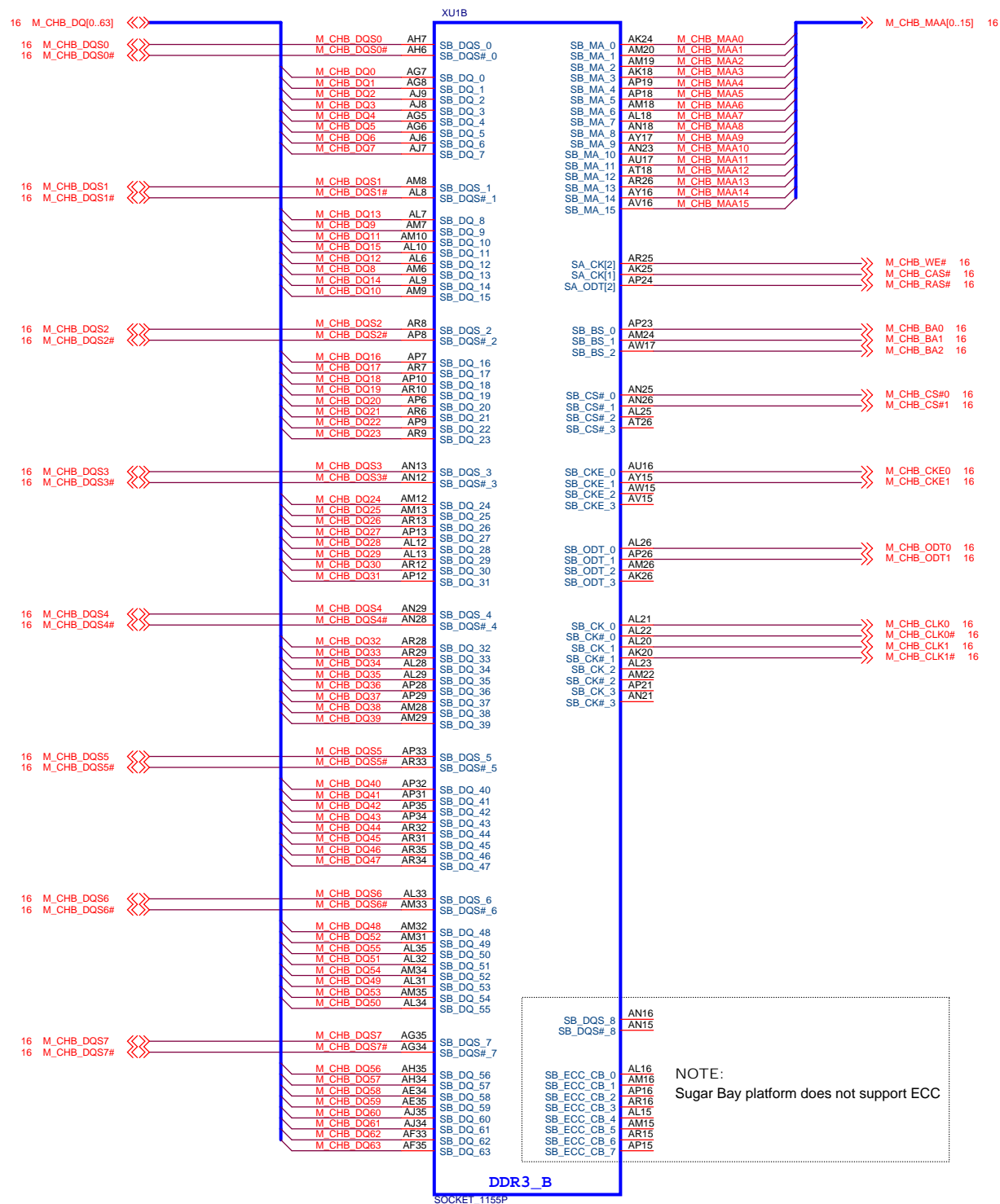


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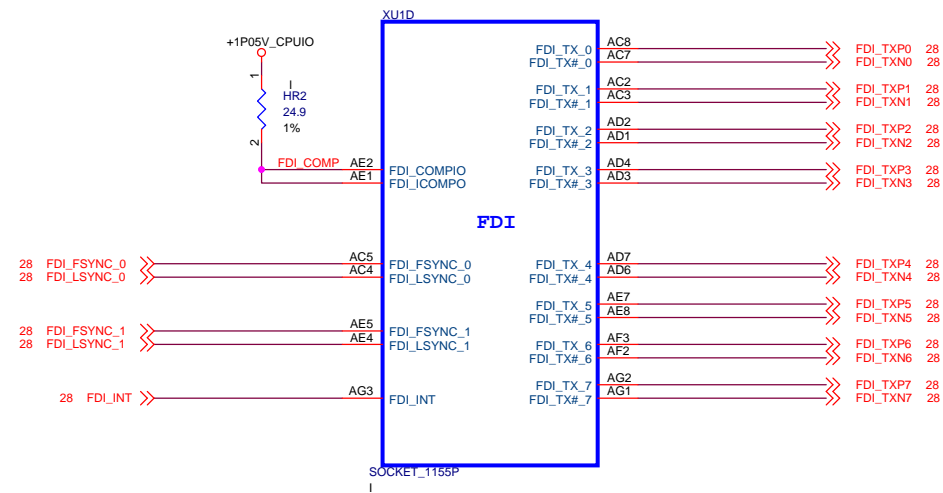
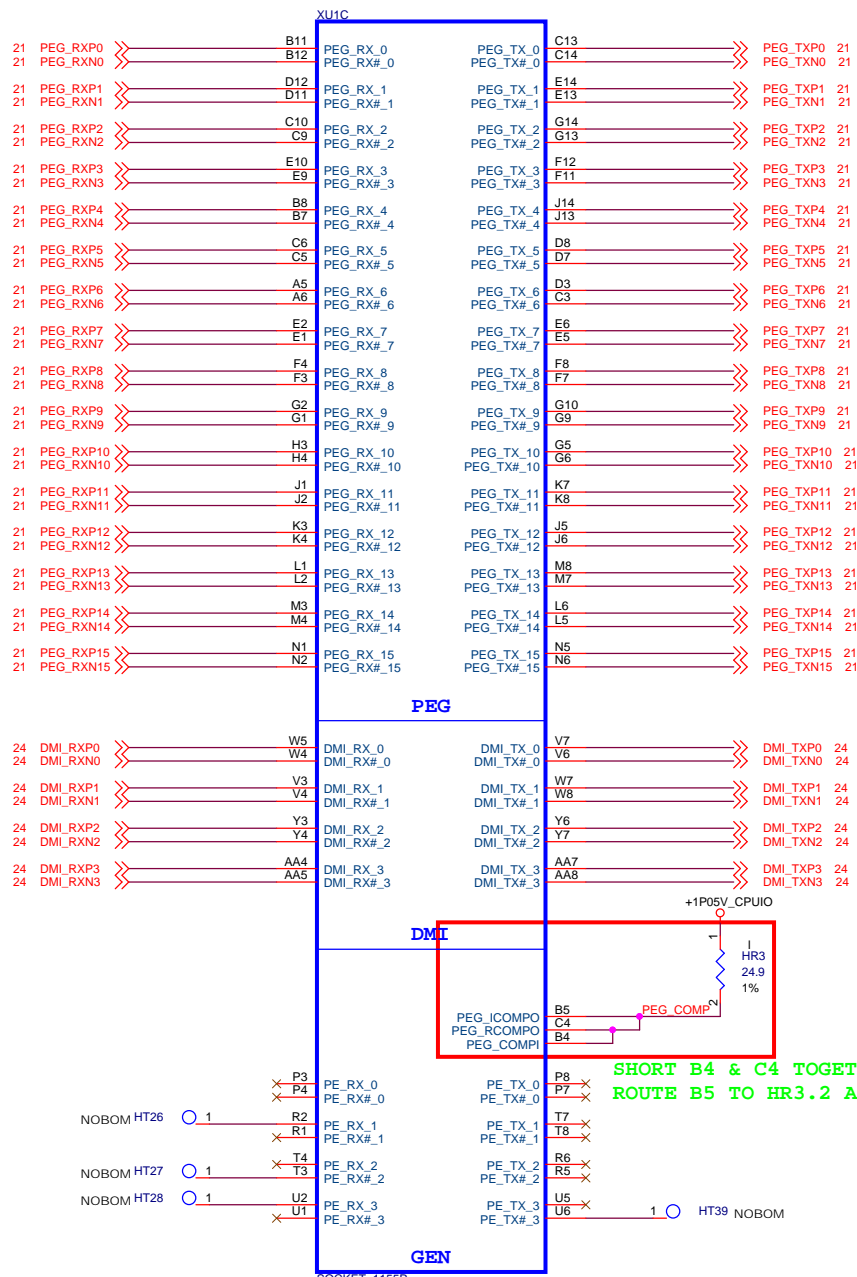
PEGATRON		Title : POWER SEQUENCE	
PEGATRON CORPORATION		Engineer:	<i>Ethan_Chen</i>
Size A	Project Name IPISB-NK		Rev 1.03
Date: Wednesday, April 20, 2011		Sheet	8 of 80



DDR3_A

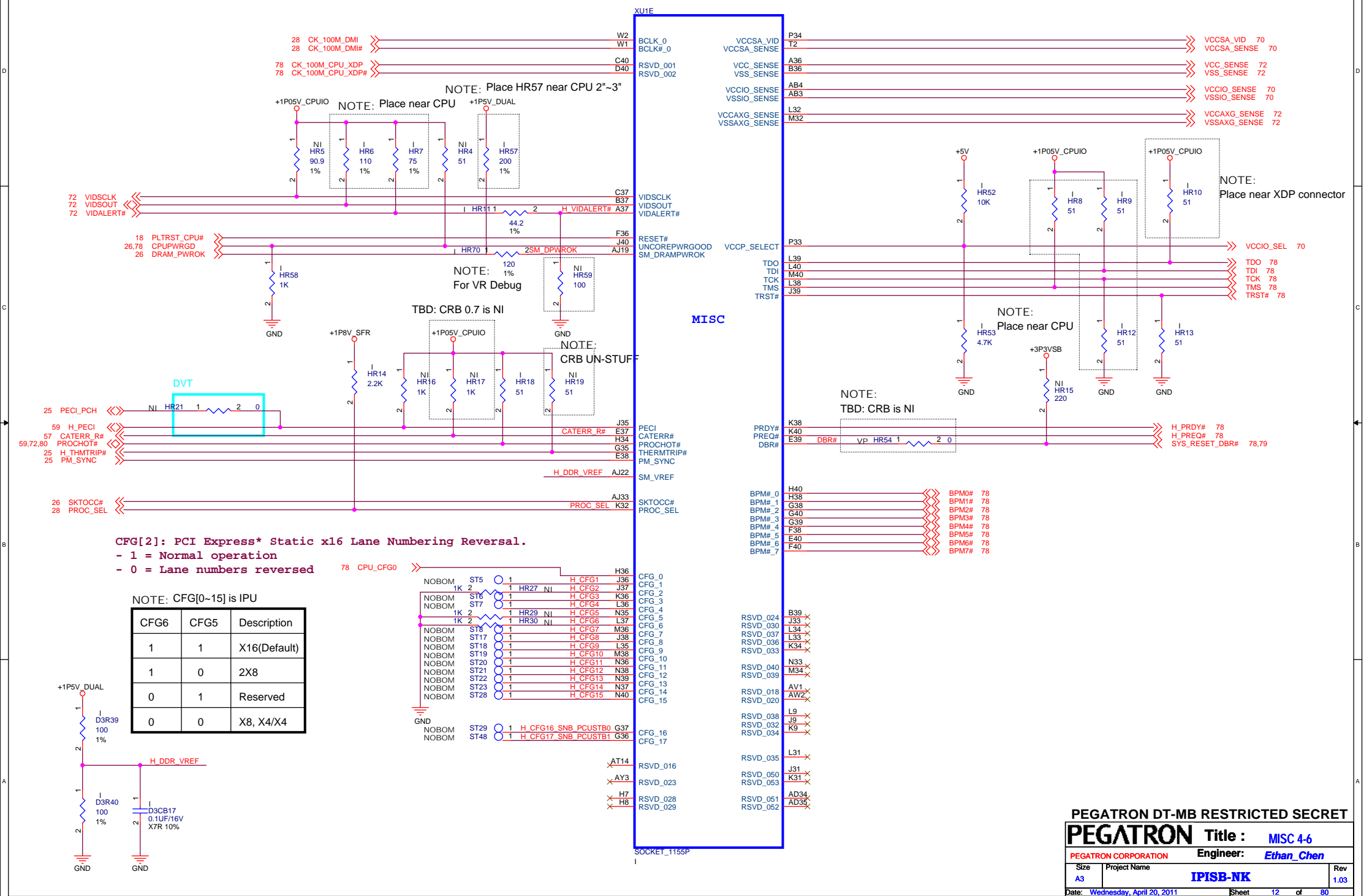


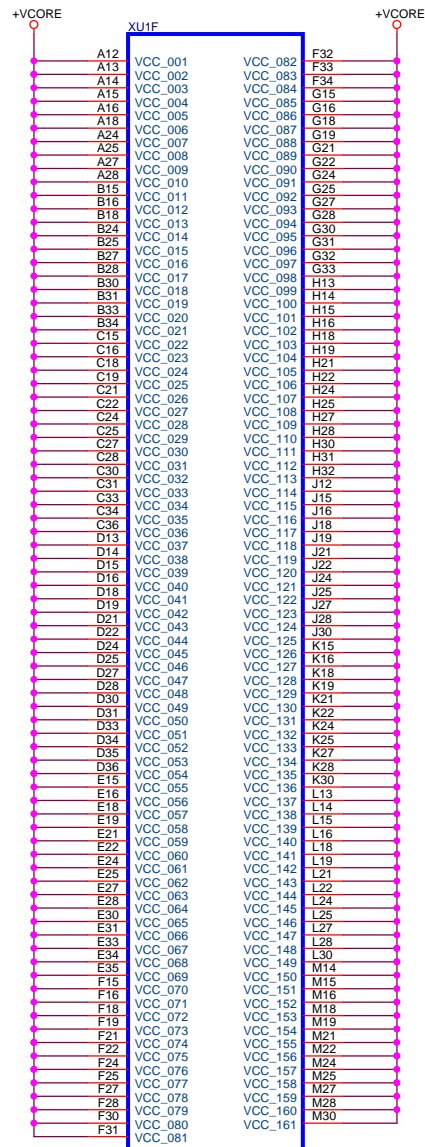
NOTE:
Sugar Bay platform does not support ECC



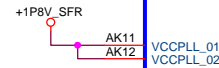
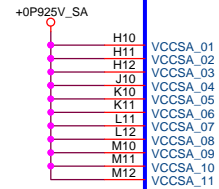
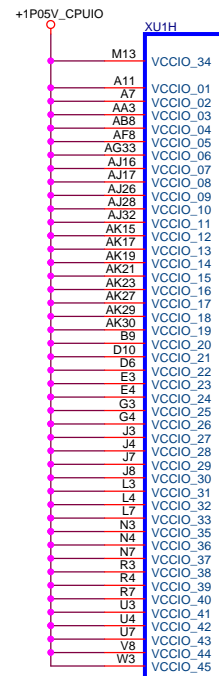
SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO HR3.2
ROUTE B5 TO HR3.2 AS A SEPERATE 10 MIL TRACE

Processor PCI Express*
Receive/ Transmit
Differential Pair. These
signals are available for
Workstation only.

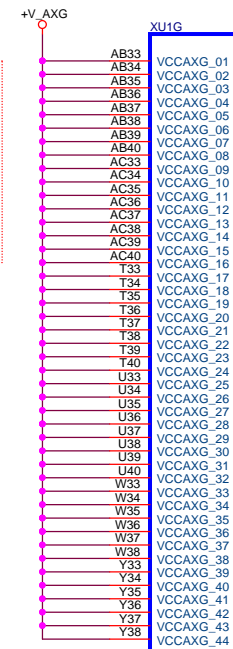
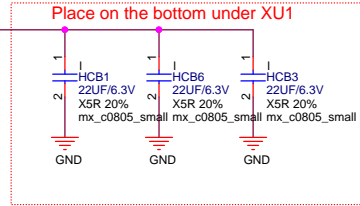




SOCKET_1155P



SOCKET_1155P



SOCKET_1155P

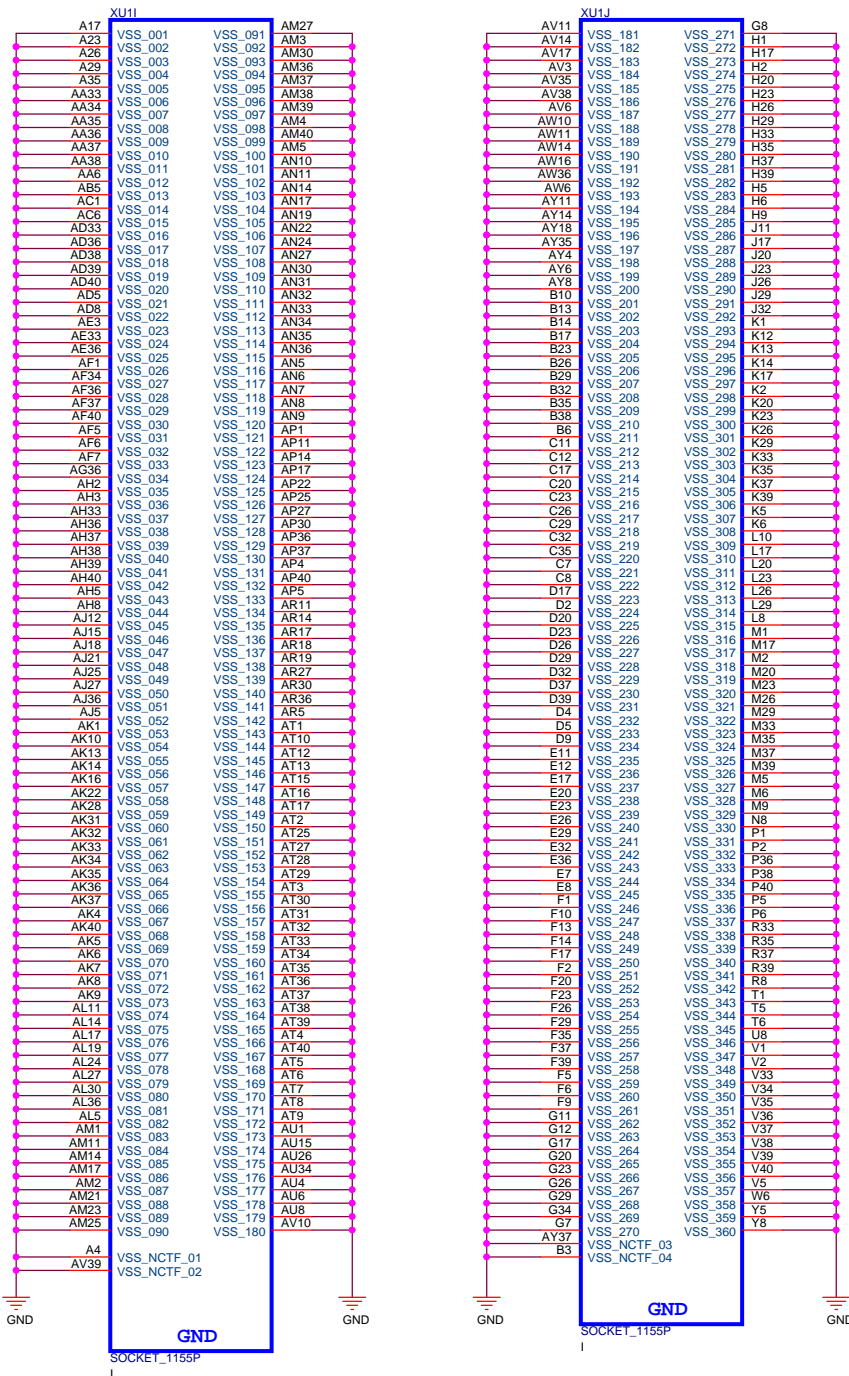
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCC 5 - 6

PEGATRON CORPORATION Engineer: Ethan_Chen

Size A3 Project Name IPISB-NK Rev 1.03

Date: Wednesday, April 20, 2011 Sheet 13 of 80



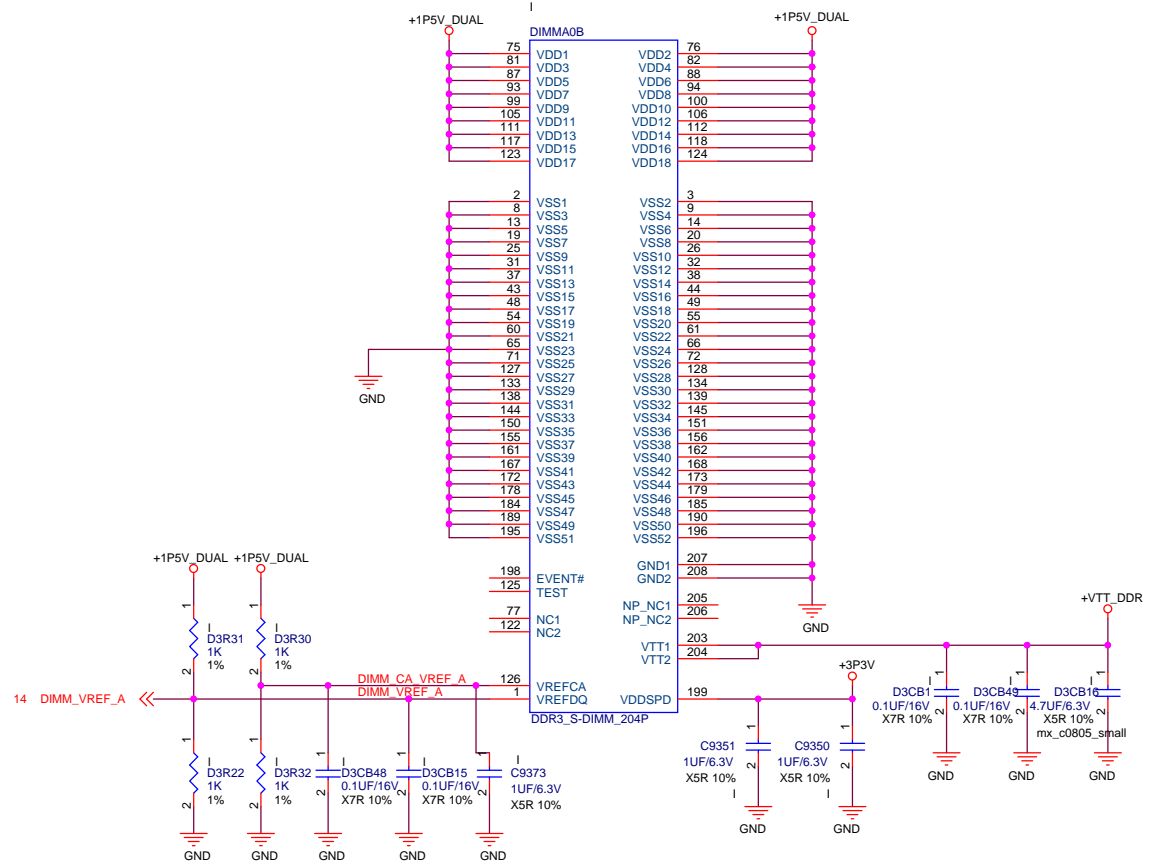
PEGATRON DT-MB RESTRICTED SECRET

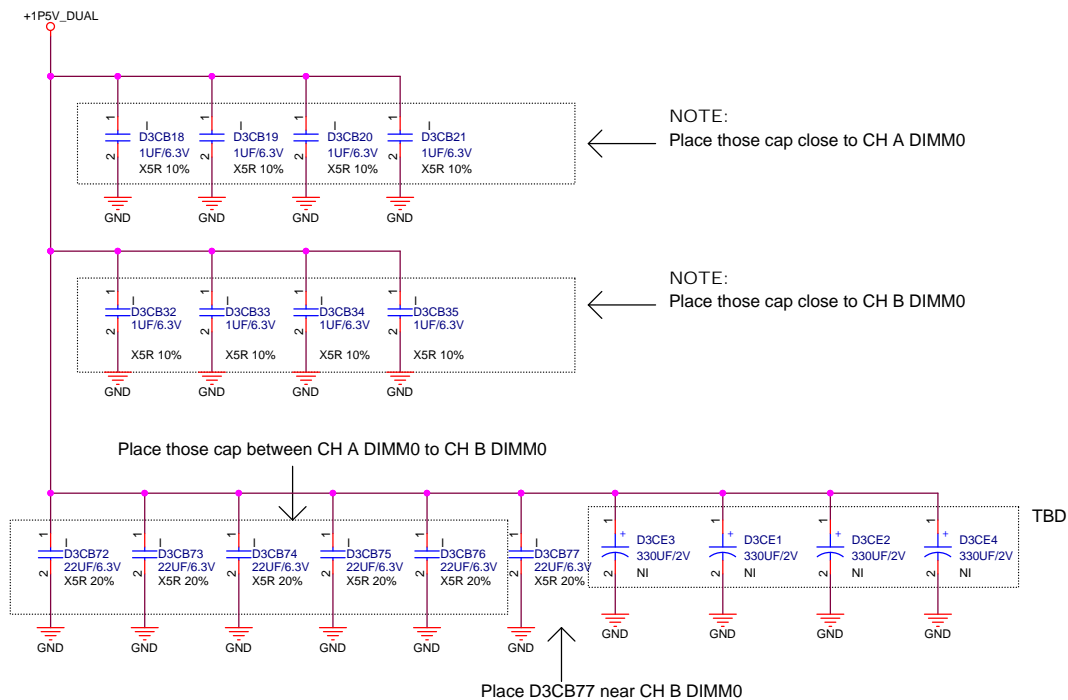
PEGATRON Title : VSS 6 - 6

PEGATRON CORPORATION Engineer: Ethan Chen

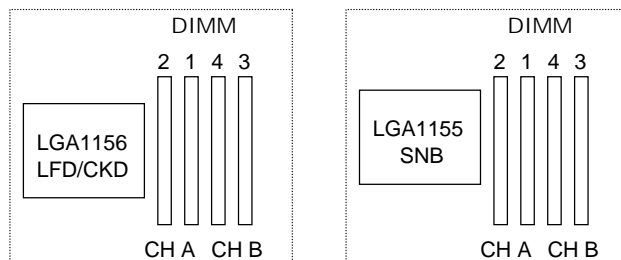
Size A3 Project Name IPISB-NK Rev 1.03

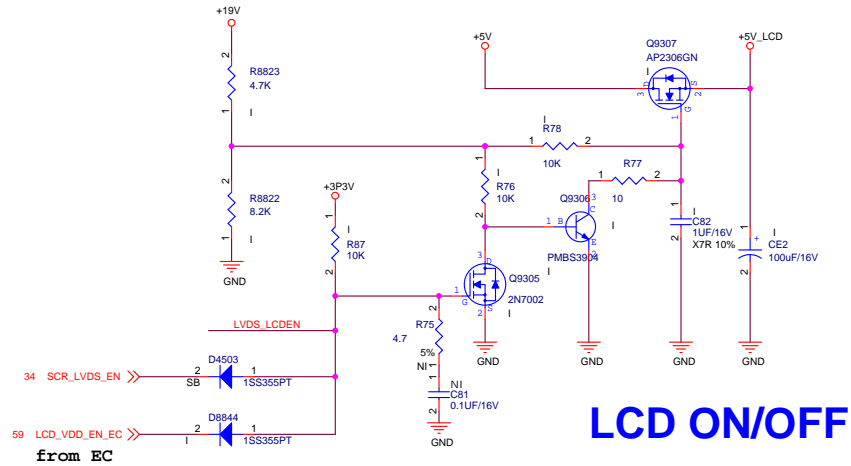
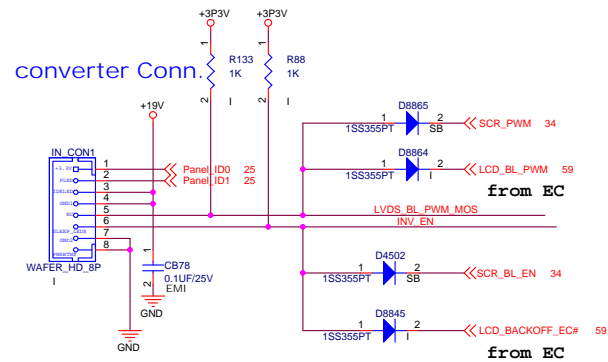
Date: Thursday, April 21, 2011 Sheet 14 of 80

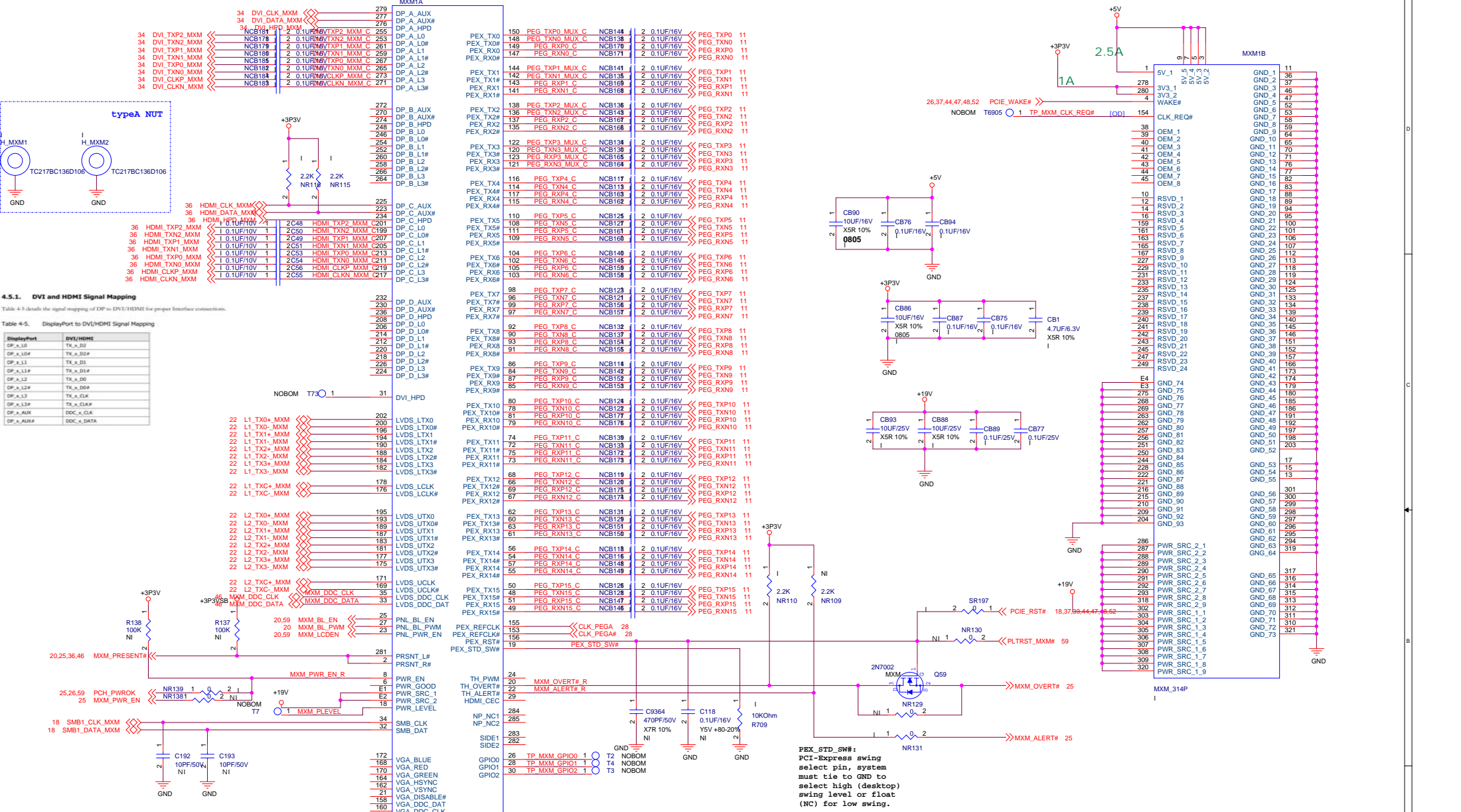




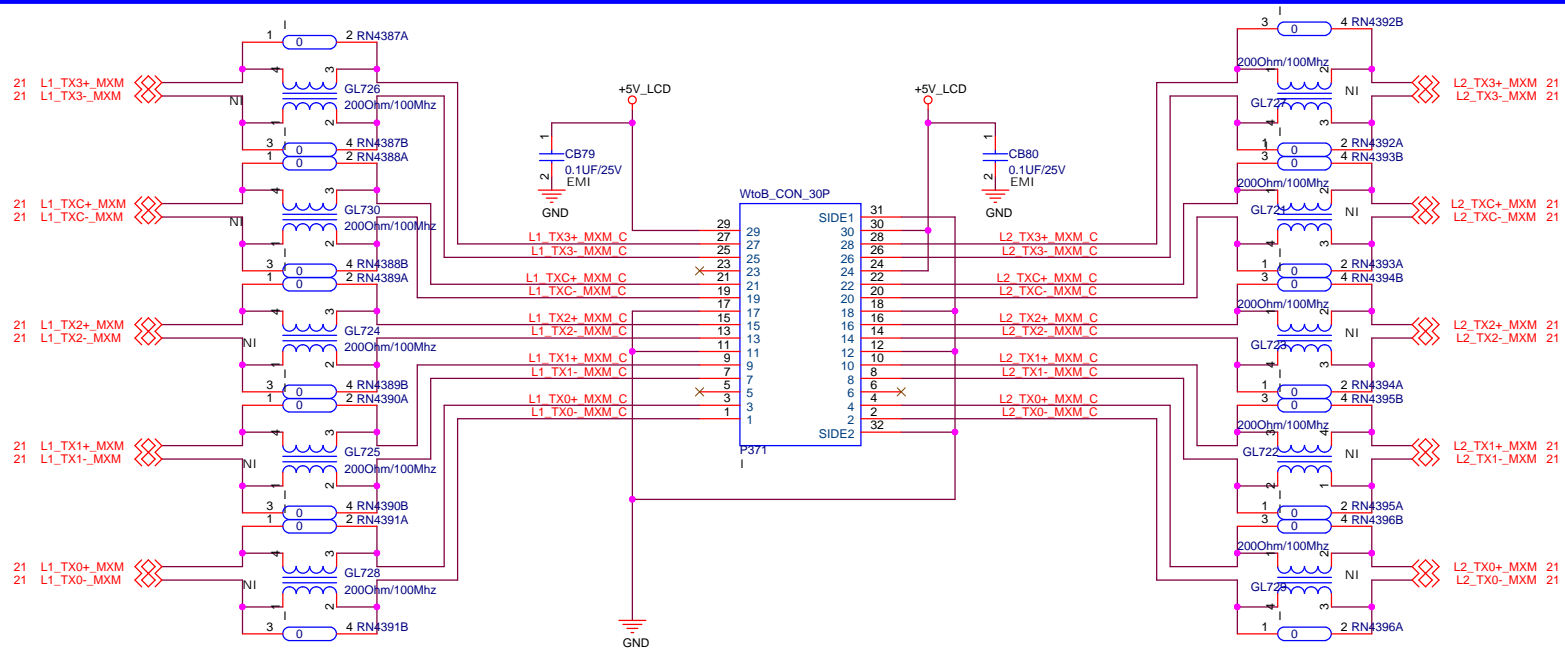
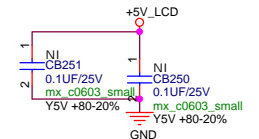
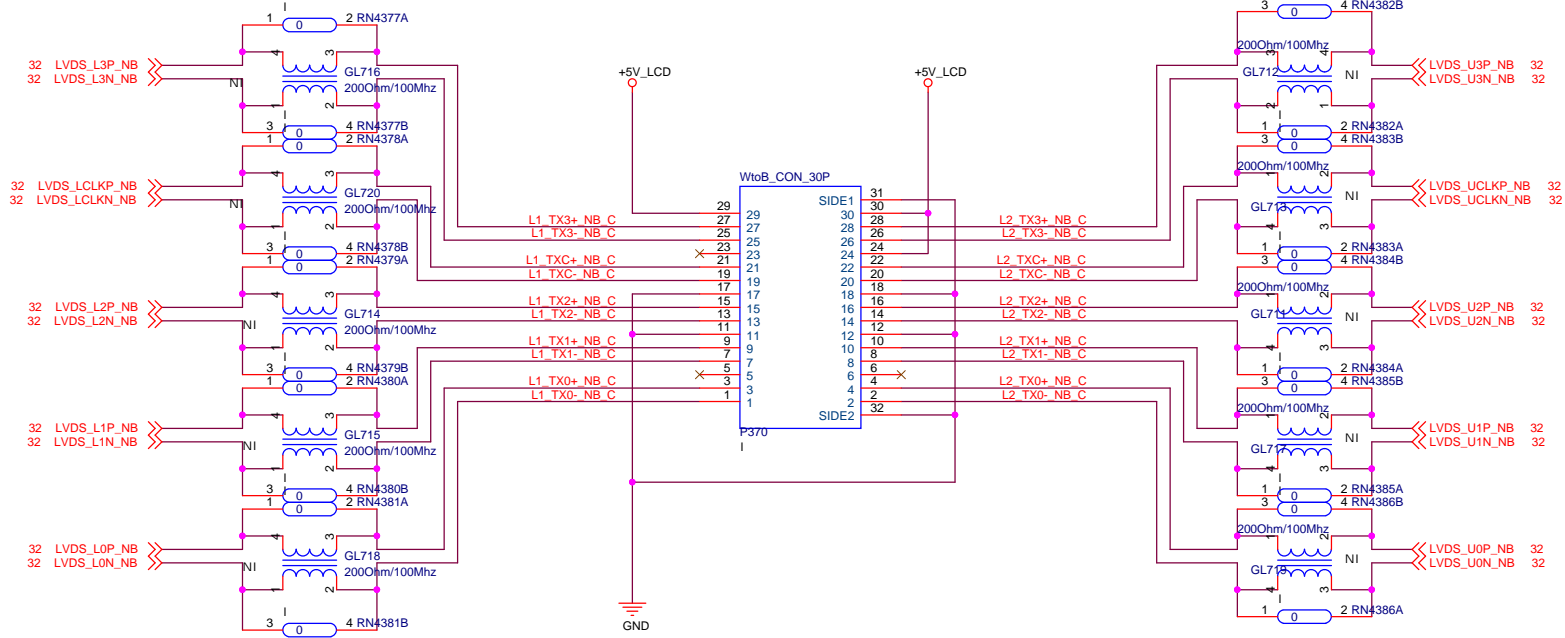
NOTE:
DIMM Placement for different platform



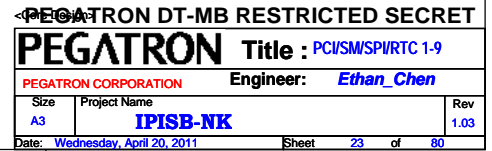


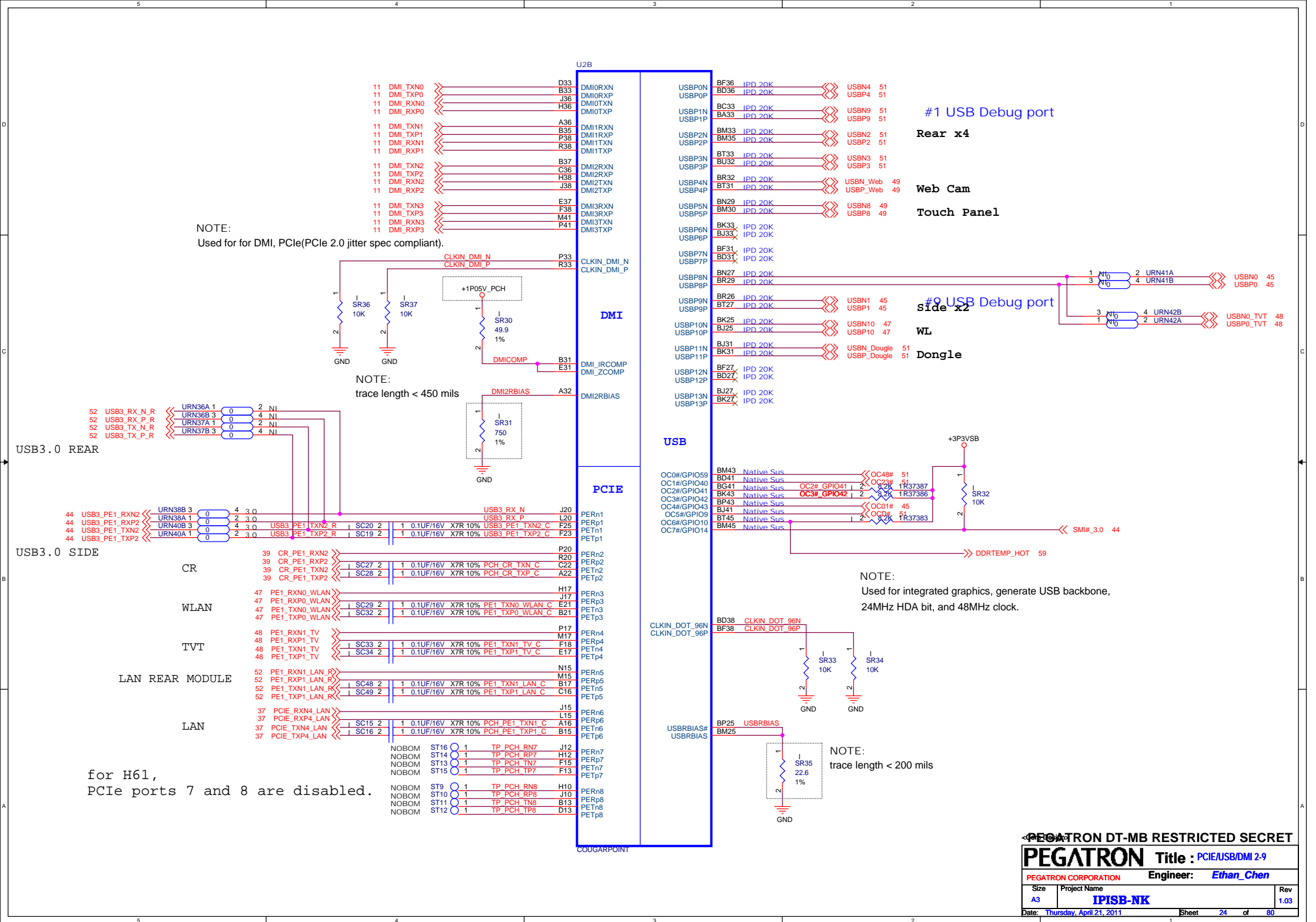


LCD CONN NB & GPU colay

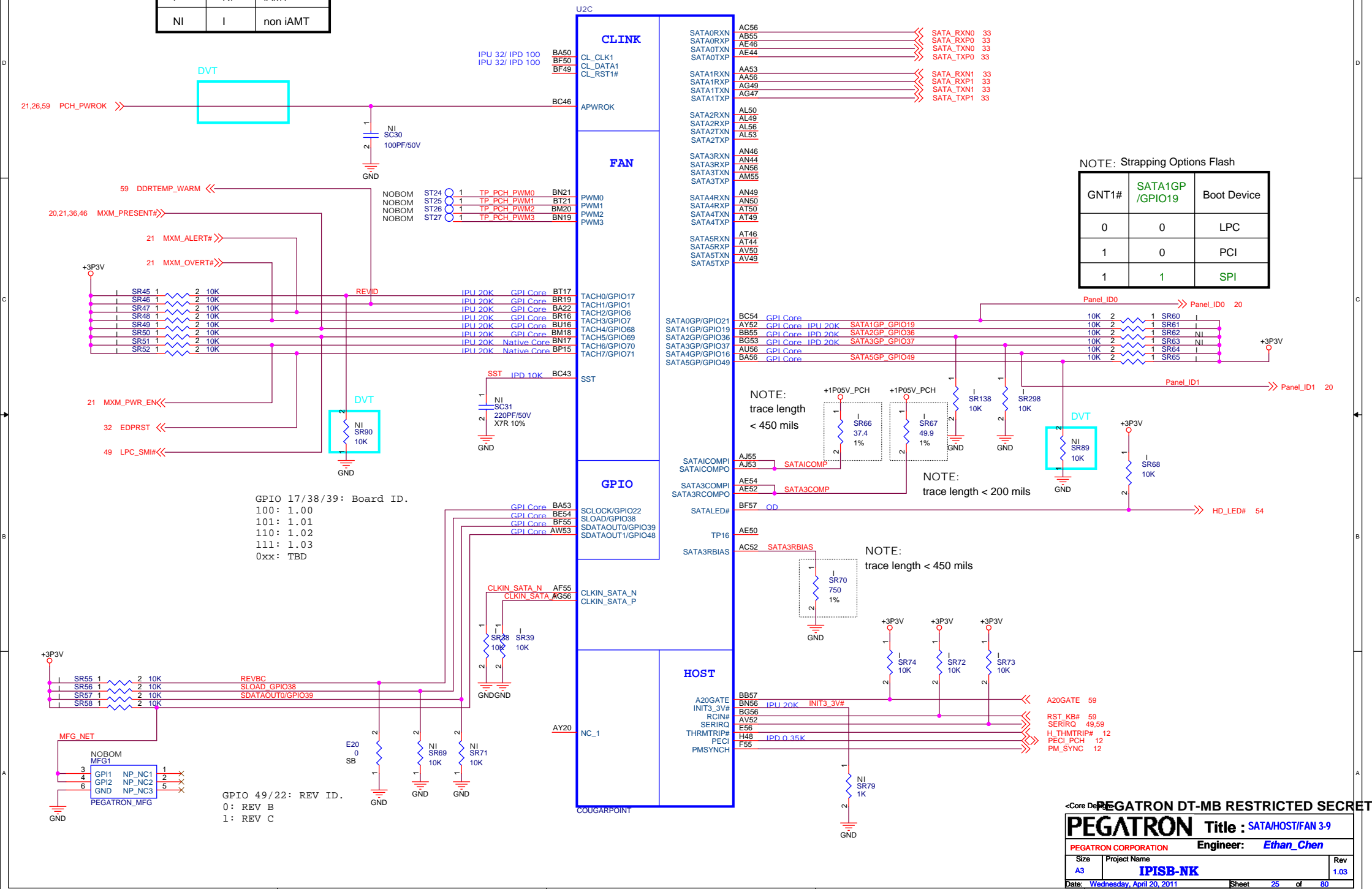


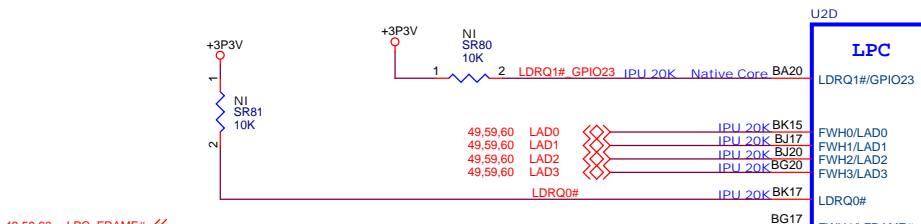
GNT1#	SATA1GP /GPIO19	Boot Device
0	0	LPC
1	0	PCI
1	1	SPI



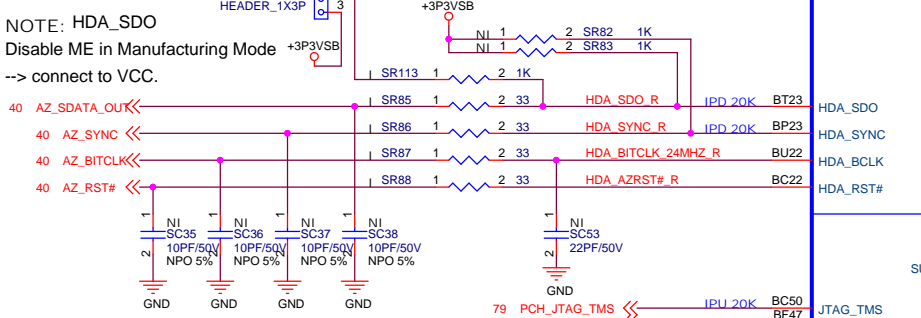


SR40	SR41	Description
I	NI	iAMT
NI	I	non iAMT

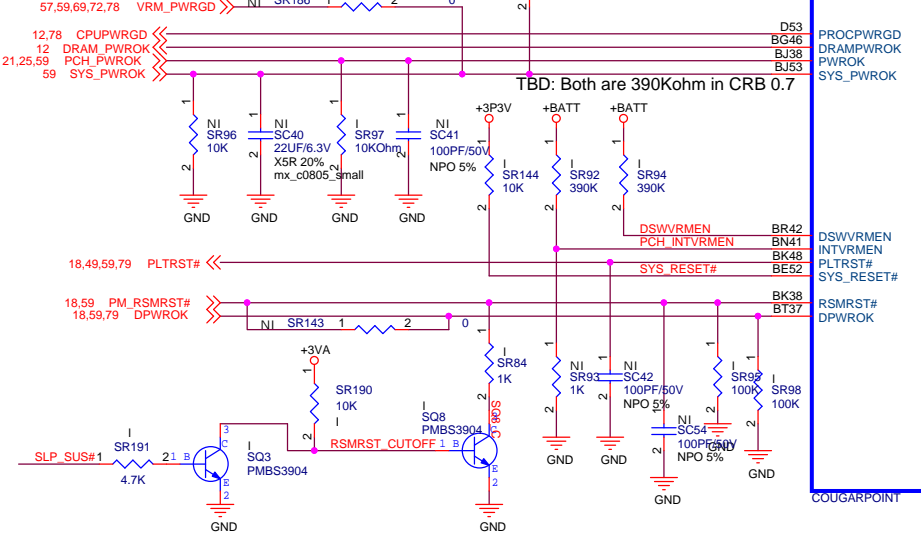




NOTE: HDA_SYNC
On-die PLL VR voltage selector.
Hi: supplied by 1.5V.
Low: supplied by 1.8V.



NOTE: HDA_SDO
Disable ME in Manufacturing Mode
--> connect to VCC.



BMBUSY#/GPIO0
CLKRUN#/GPIO32
HDA_DOCK_EN#/GPIO33
STP_PCH#/GPIO34
GPIO35
GPIO38
LAN_PHY_PWR_CTRL#/GPIO12
HDA_DOCK_RST#/GPIO13
GPIO15
GPIO24/MEM_LED
GPIO28
SLP_LAN#/GPIO29
GPIO27
GPIO31

PCIECLKRQ2#/GPIO20
PCIECLKRQ5#/GPIO44
PCIECLKRQ6#/GPIO45
PCIECLKRQ7#/GPIO46
GPIO57

BATLOW#/GPIO72
SUSWARN#/SUSPWRDNACK#/GPIO30
SUSACK#
SUSCLK#/GPIO62
SUS_STAT#/GPIO61

NOTE:
SUSACK# and SUSWARN#
can be tied together if EC/SIO
does not want to involve in
the handshake mechanism
for the Deep Sleep state
entry and exit.

RI#
WAKE#
INTRUDER#
SPKR
PWRBTN#

SLP_S3#
SLP_S4#
SLP_S5#/GPIO63
SLP_A#
SLP_SUS#

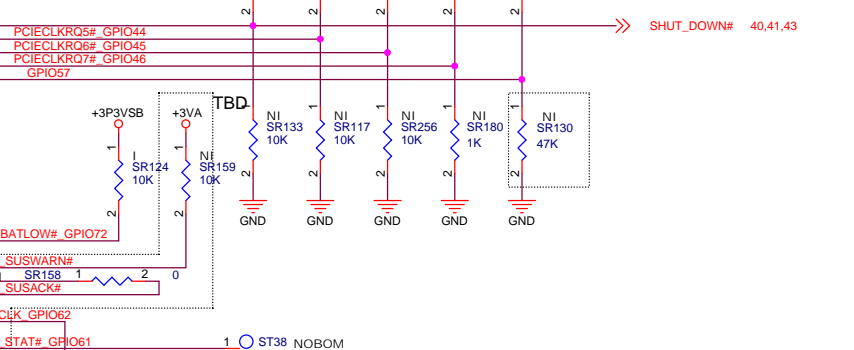
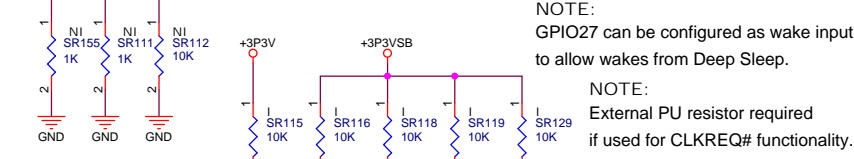
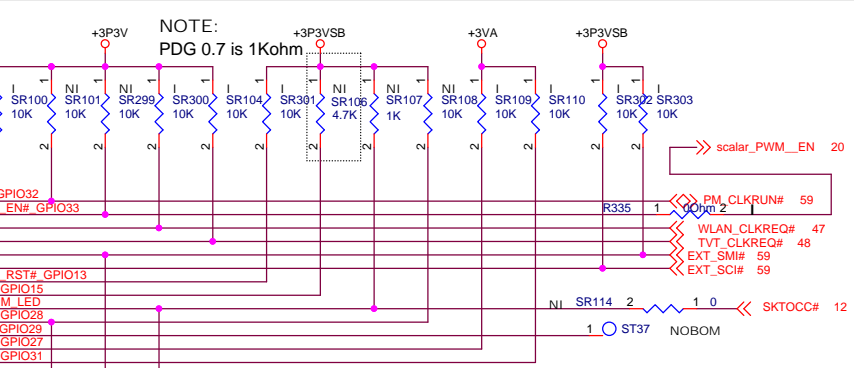
AW55 GPI BMBUSY# GPIO0
BC56 GPO Core CLKRUN# GPIO32
BC25 GPO Core HDA_DOCK_EN# GPIO33
BL56 GPO Core STP_PCH# GPIO34
BJ57 GPO Core GPIO35
BP51 GPO Sus IPU 20K GPIO38
BK50 Native Sus LAN_PHY_PWR_CTRL# GPIO12
BA25 GPO Sus HDA_DOCK_RST# GPIO13
BM55 GPO Sus IPU 20K GPIO15
BP53 GPO Sus GPIO24 MEM_LED
BJ55 GPO Sus IPU 20K GPIO28
BH49 GPI Sus SLP_LAN# GPIO29
BJ43 GPI DSW IPU 20K GPIO27
BG43 GPI DSW IPD TBD GPIO31

AV43 Native Core
BL54 Native Sus IPU TBD
AV44 Native Sus IPU 20K
BP55 Native Sus IPU 20K
BT53 GPI Sus

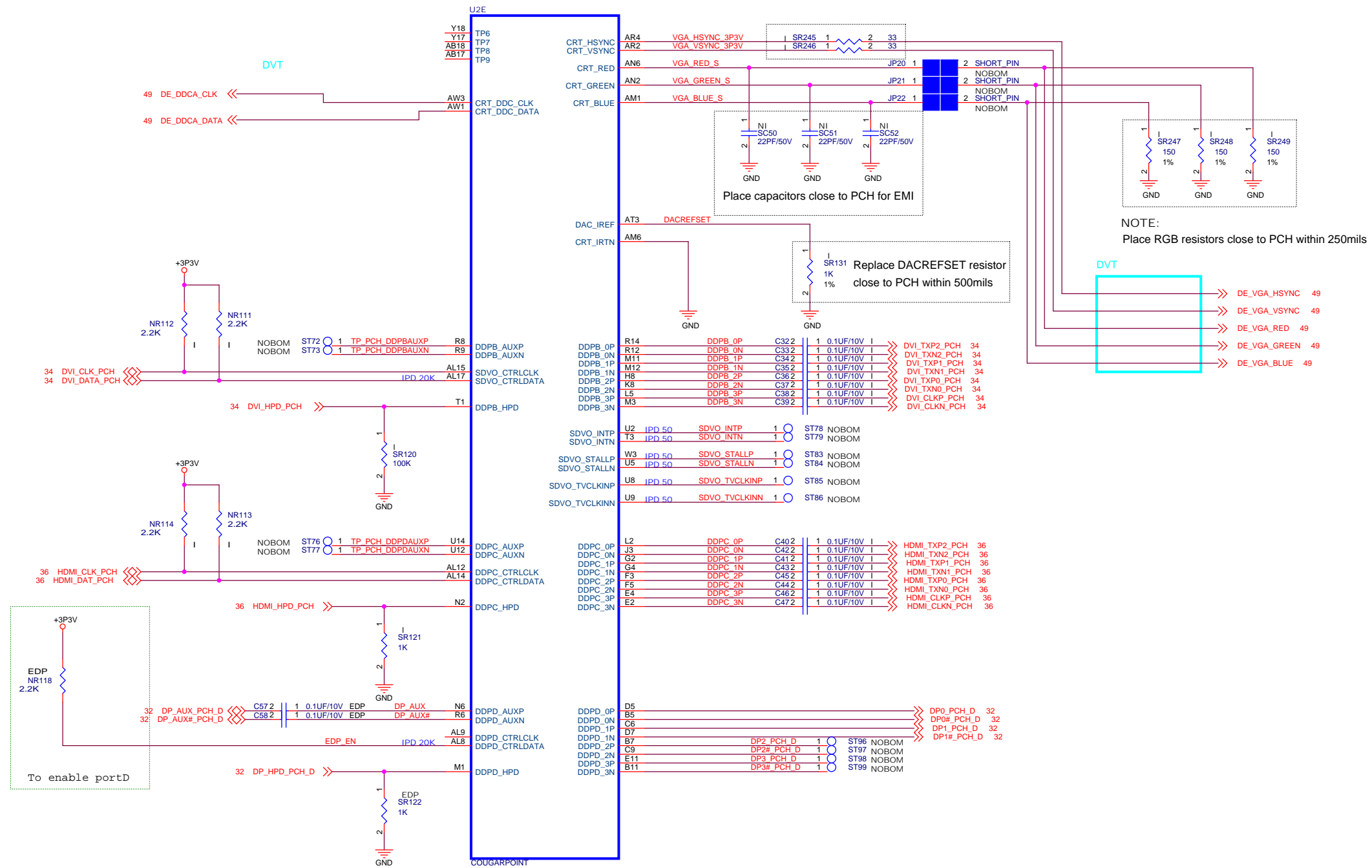
AV46 Native Sus IPU 20K BATLOW# GPIO72
BU46 GPI DSW PCH_SUSWARN#
BP45 IPU TBD PCH_SUSACK#
BA47 Native Sus SUSCLK# GPIO62
BN54 Native Sus SUS_STAT# GPIO61

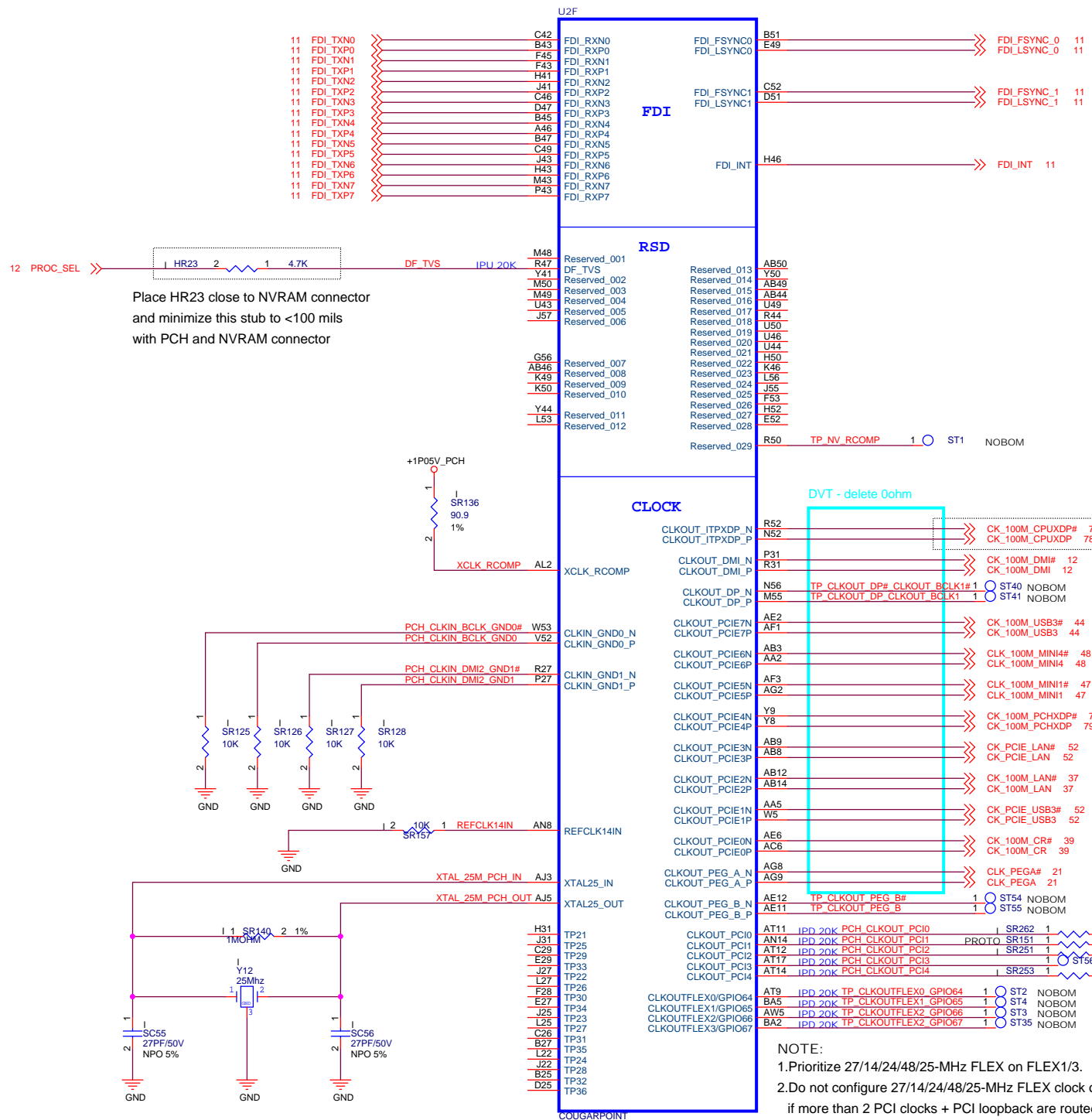
BJ48 modem_wake_event
BC44 WAKE#
BM38 INTRUDER#
BE56 IPU 20K
BT43 IPU 20K PCH_PWRBTN#

BM53 SLP_S3#
BN52 SLP_S4#
BH50 Native Sus SLP_A#
BC41 SLP_S5#
BD43 SLP_SUS#



PIN	HIGH	LOW	DESCRIPTION
GPIO15	Enable	Disable	TLS confidentiality
GPIO28	Enable	Disable	On-Die PLL VR





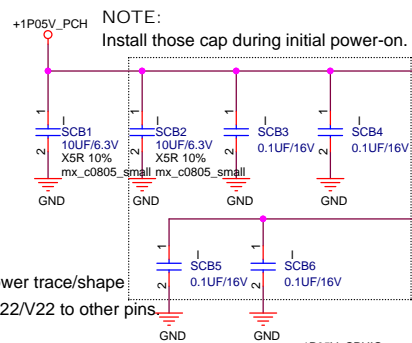
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CLK/NVRAM/FDI 6-9

PEGATRON CORPORATION Engineer: **Ethan_Chen**

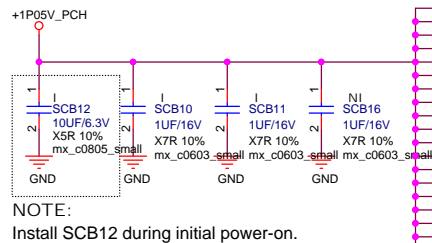
Size	Project Name	Rev
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NOTE:
Trace needs to be at least 20 mils width with full VSS/VCC reference plane

NOTE:
Splitting 2 power trace/shape



U2G
COUGARPOINT

VccCore_001
VccCore_002
VccCore_003
VccCore_004
VccCore_005
VccCore_006
VccCore_007
VccCore_008
VccCore_009
VccCore_010
VccCore_011
VccCore_012
VccCore_013
VccCore_014
VccCore_015
VccCore_016
VccCore_017
VccCore_018
VccCore_019
VccCore_020
VccCore_021
VccCore_022

VccIO_018
VccSSC_01
VccSSC_02
VccIO_001
VccIO_002
VccIO_003
VccIO_004
VccIO_013
VccIO_012
VccIO_014

VccDIFFCLKN_01
VccDIFFCLKN_02
VccDIFFCLKN_03

VccAFDIPLL
VccAClk

VccAPLLEXP
VccAPLLSATA
VccAPLLDMI2
VccClkDMI

VccADAC
VccADPLL
VccADPLLB

AC24
AC26
AC28
AC30
AC32
AE24
AE28
AE30
AE32
AE34
AE36
AG32
AG34
AJ32
AJ34
AJ36
AL32
AL34
AN32
AN34
AR32
AR34

AE40
AC20
AE20
AV24
AV26
AY25
AY27
V36
Y36
Y28

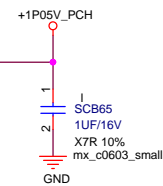
AE15
AE17
AG15

C54
AL5
B53
U56
A19
AJ20
AT1
AB1
AC2

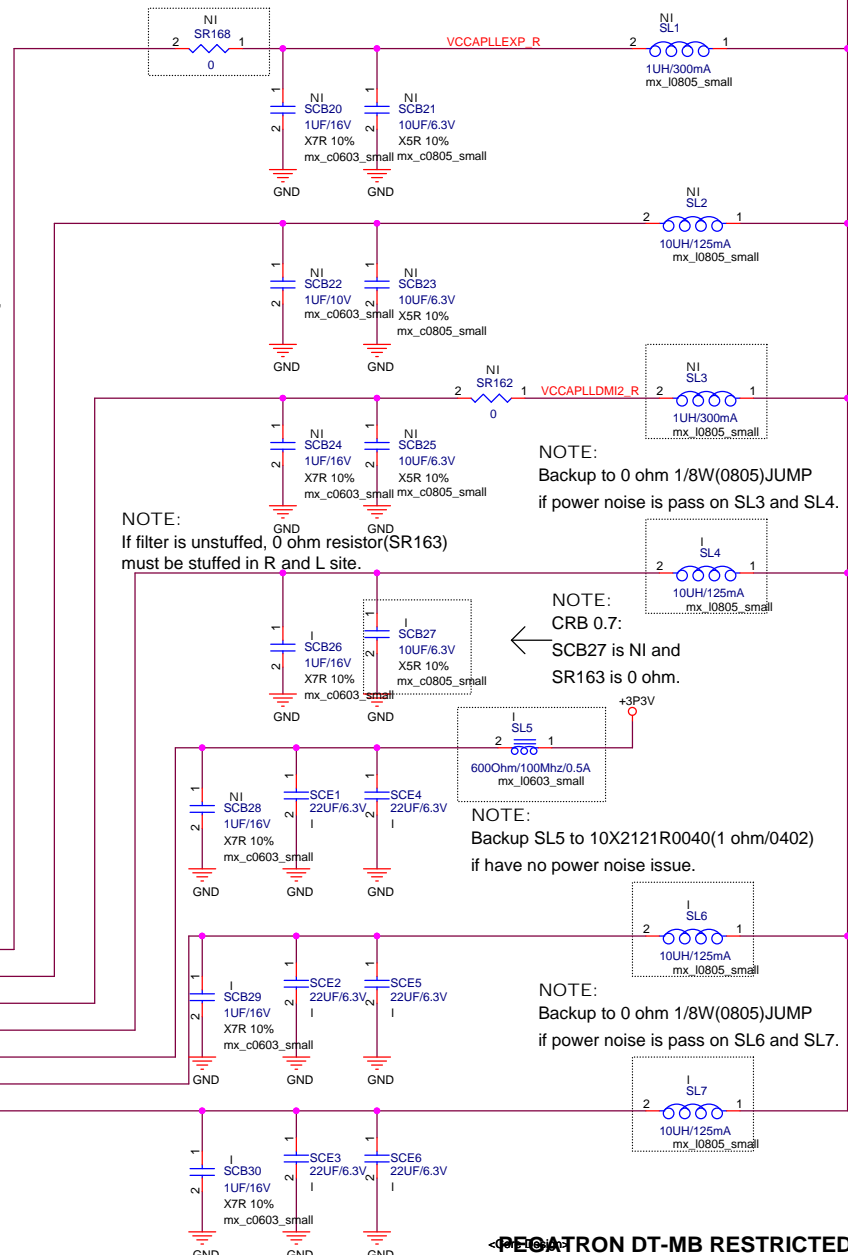
NOTE:
VccAFDIPLL and VccAClk can be NC in on-die VR mode.

NOTE:
Splitting 2 power trace/shape on pins AV24/AV26 to AY25/AY27, and AE40 to AG38/AG40.

NOTE:
Splitting 2 power traces on pins AC20 to AE20.



NOTE:
VccAPLLEXP, VccAPLLSATA, and VccAPLLDMI2 can be NC in On-Die VR mode.



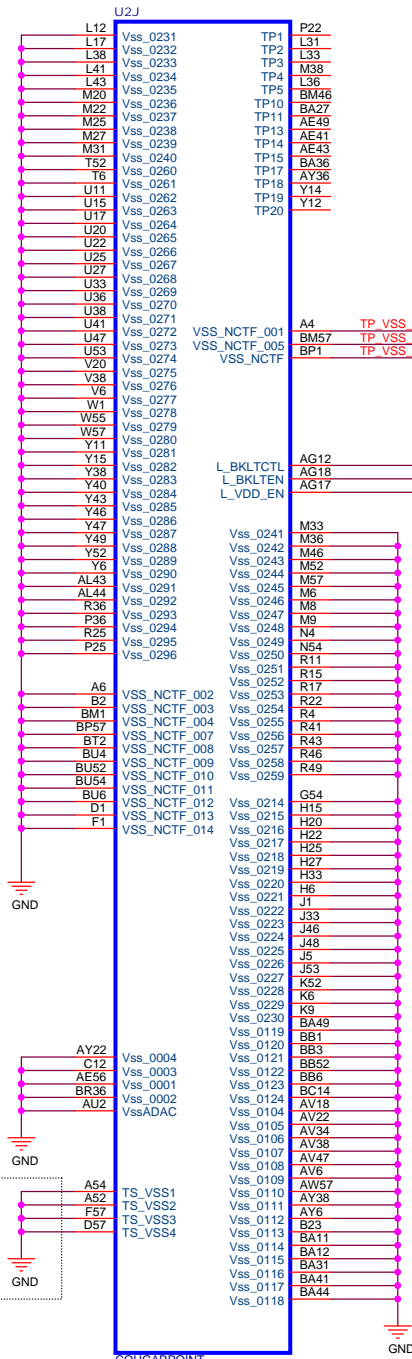
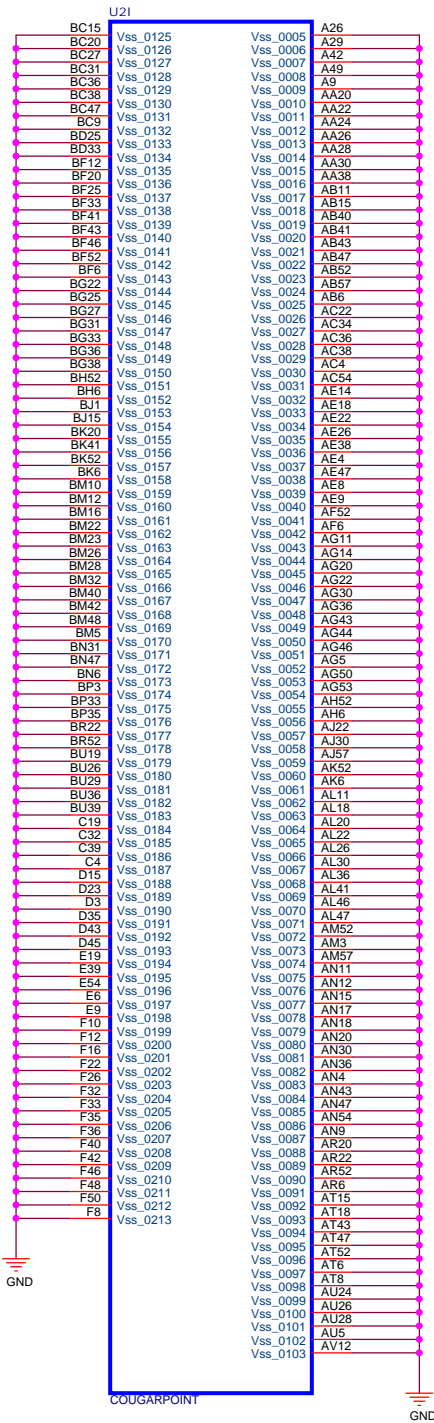
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCC/PLL 7-9

PEGATRON CORPORATION Engineer: Ethan_Chen

Size A3 Project Name IPISB-NK Rev 1.03

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VSS_NCTF_001
VSS_NCTF_005
VSS_NCTF

L_BKLTCTL
L_BKLTEN
L_VDD_EN

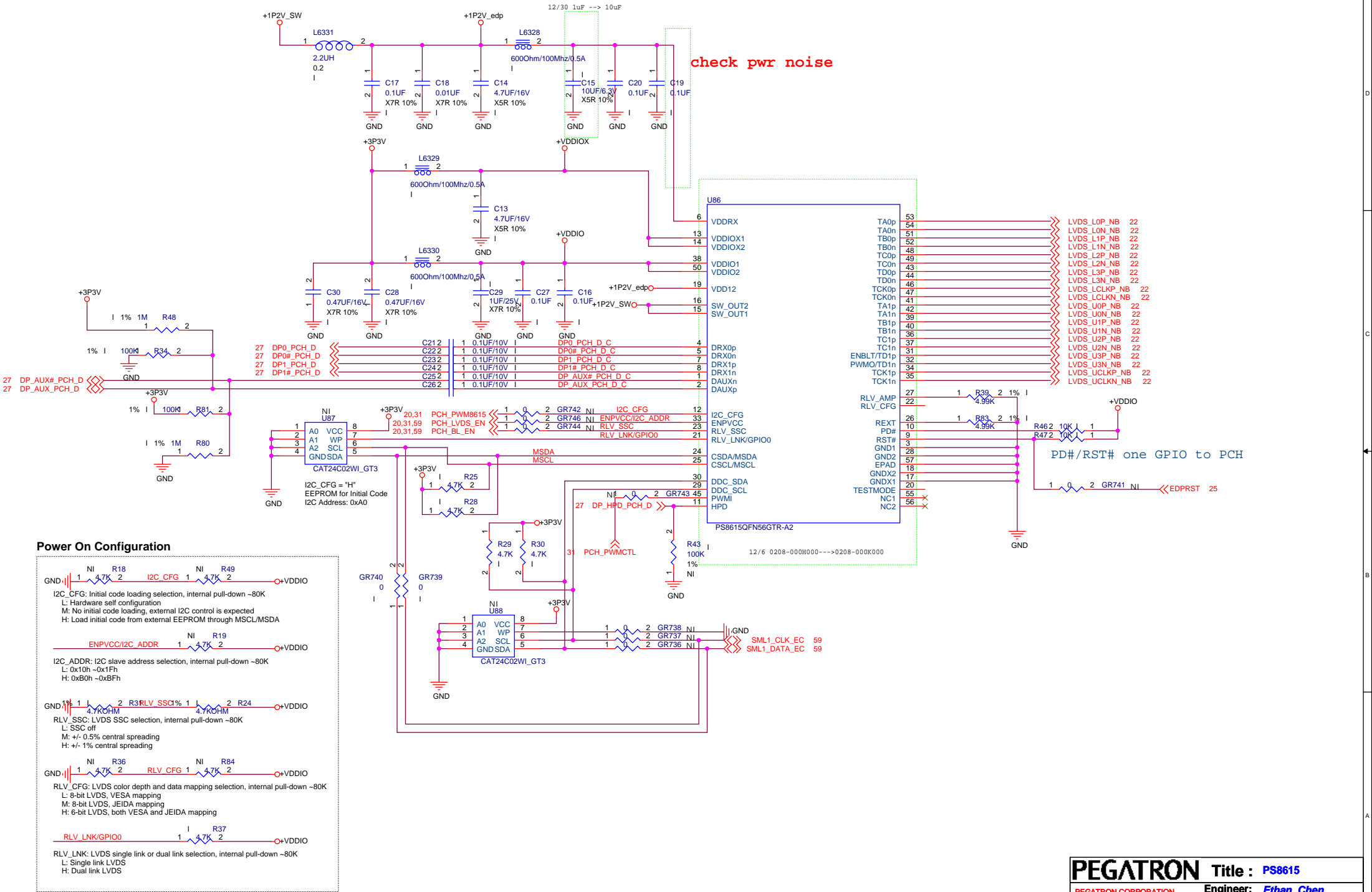
Vss_0241
Vss_0242
Vss_0243
Vss_0244
Vss_0245
Vss_0246
Vss_0247
Vss_0248
Vss_0249
Vss_0250
Vss_0251
Vss_0252
Vss_0253
Vss_0254
Vss_0255
Vss_0256
Vss_0257
Vss_0258
Vss_0259
Vss_0214
Vss_0215
Vss_0216
Vss_0217
Vss_0218
Vss_0219
Vss_0220
Vss_0221
Vss_0222
Vss_0223
Vss_0224
Vss_0225
Vss_0226
Vss_0227
Vss_0228
Vss_0229
Vss_0230
Vss_0231
Vss_0232
Vss_0233
Vss_0234
Vss_0235
Vss_0236
Vss_0237
Vss_0238
Vss_0239
Vss_0240
Vss_0260
Vss_0261
Vss_0262
Vss_0263
Vss_0264
Vss_0265
Vss_0266
Vss_0267
Vss_0268
Vss_0269
Vss_0270
Vss_0271
Vss_0272
Vss_0273
Vss_0274
Vss_0275
Vss_0276
Vss_0277
Vss_0278
Vss_0279
Vss_0280
Vss_0281
Vss_0282
Vss_0283
Vss_0284
Vss_0285
Vss_0286
Vss_0287
Vss_0288
Vss_0289
Vss_0290
Vss_0291
Vss_0292
Vss_0293
Vss_0294
Vss_0295
Vss_0296

VSS_NCTF_002
VSS_NCTF_003
VSS_NCTF_004
VSS_NCTF_007
VSS_NCTF_008
VSS_NCTF_009
VSS_NCTF_010
VSS_NCTF_011
VSS_NCTF_012
VSS_NCTF_013
VSS_NCTF_014
Vss_0004
Vss_0003
Vss_0001
Vss_0002
Vss_0004
Vss_0105
Vss_0106
Vss_0107
Vss_0108
Vss_0109
Vss_0110
Vss_0111
Vss_0112
Vss_0113
Vss_0114
Vss_0115
Vss_0116
Vss_0117
Vss_0118

TS_VSS1
TS_VSS2
TS_VSS3
TS_VSS4

NOTE:
BOM option depend on thermal result

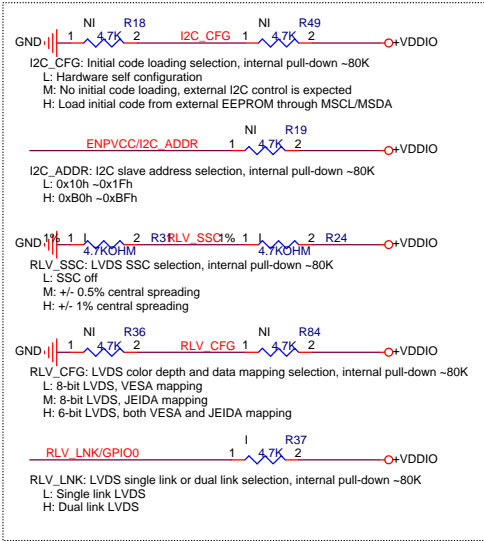




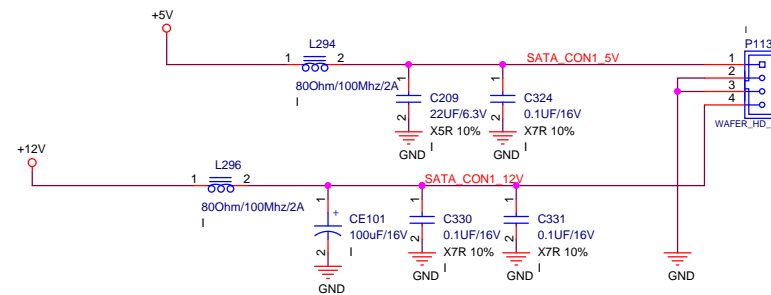
check pwr noise

PD#/RST# one GPIO to PCH

Power On Configuration

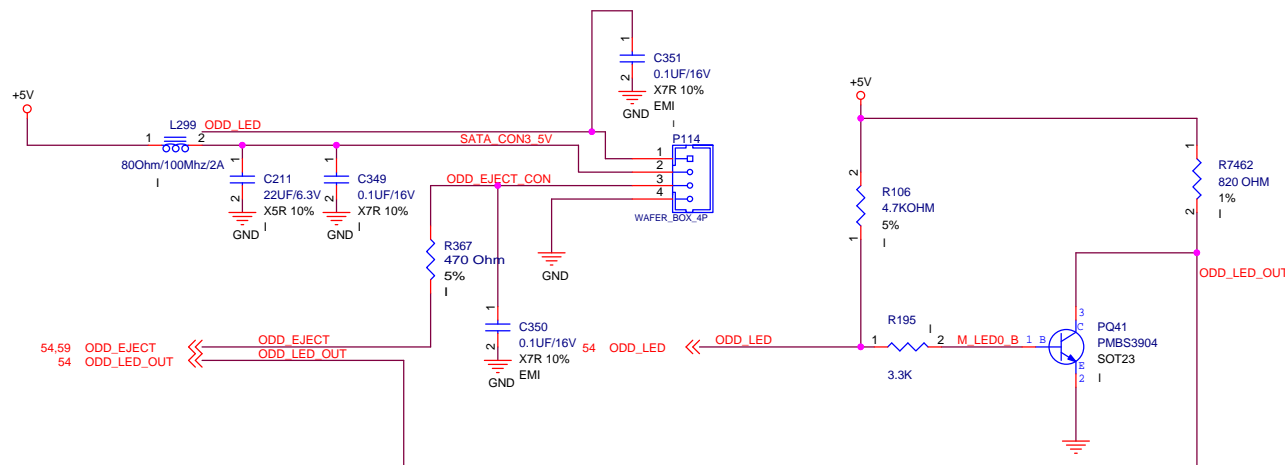
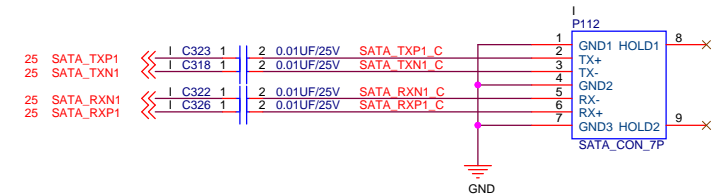
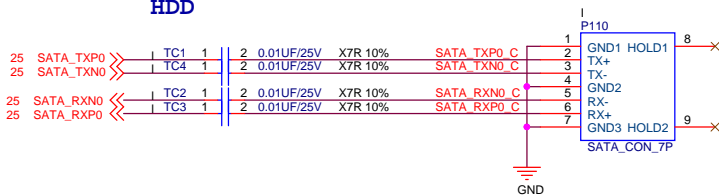


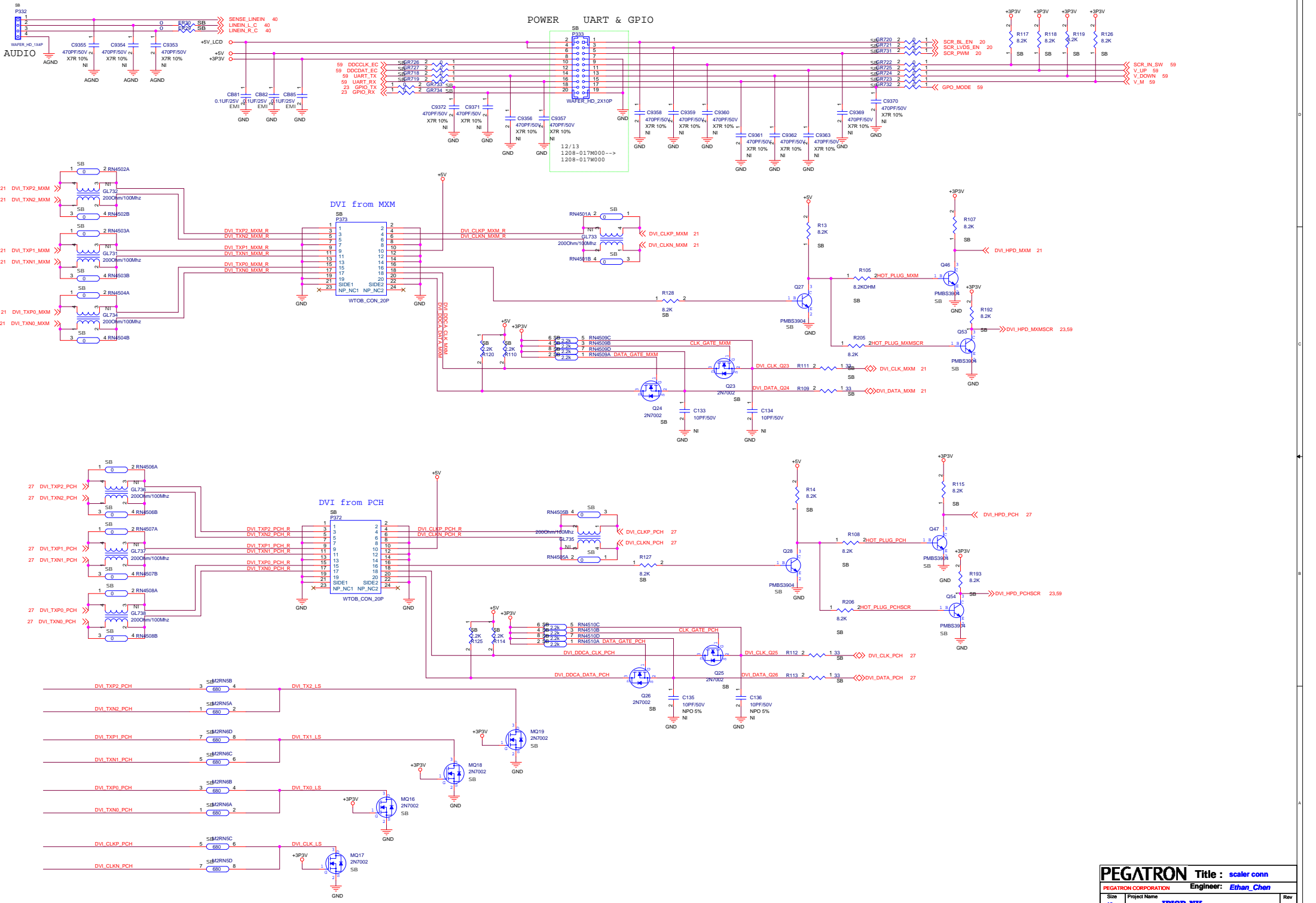
SATA CONNECTOR

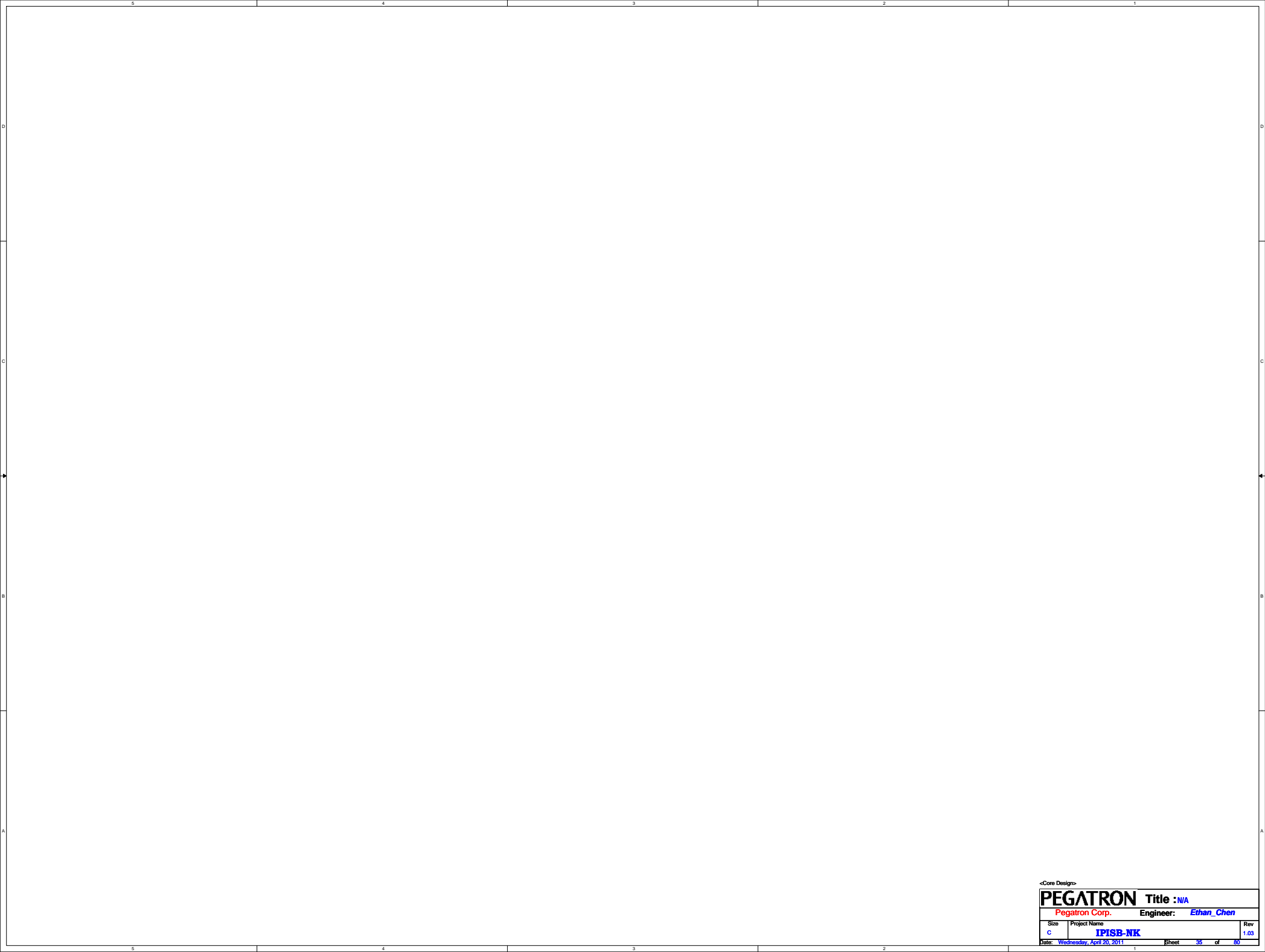


CHANNEL 1 MASTER
White
ODD

CHANNEL 0 MASTER
Dark Blue
HDD







<Core Design>

PEGATRON

Pegatron Corp.

Size

C

Title : N/A

Engineer: Ethan_Chen

Project Name

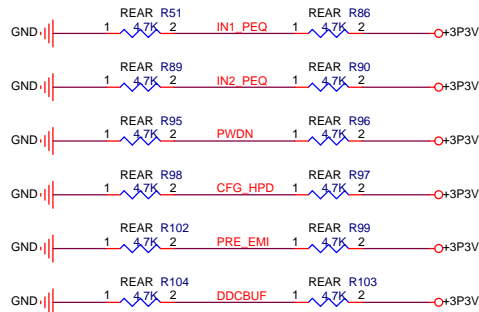
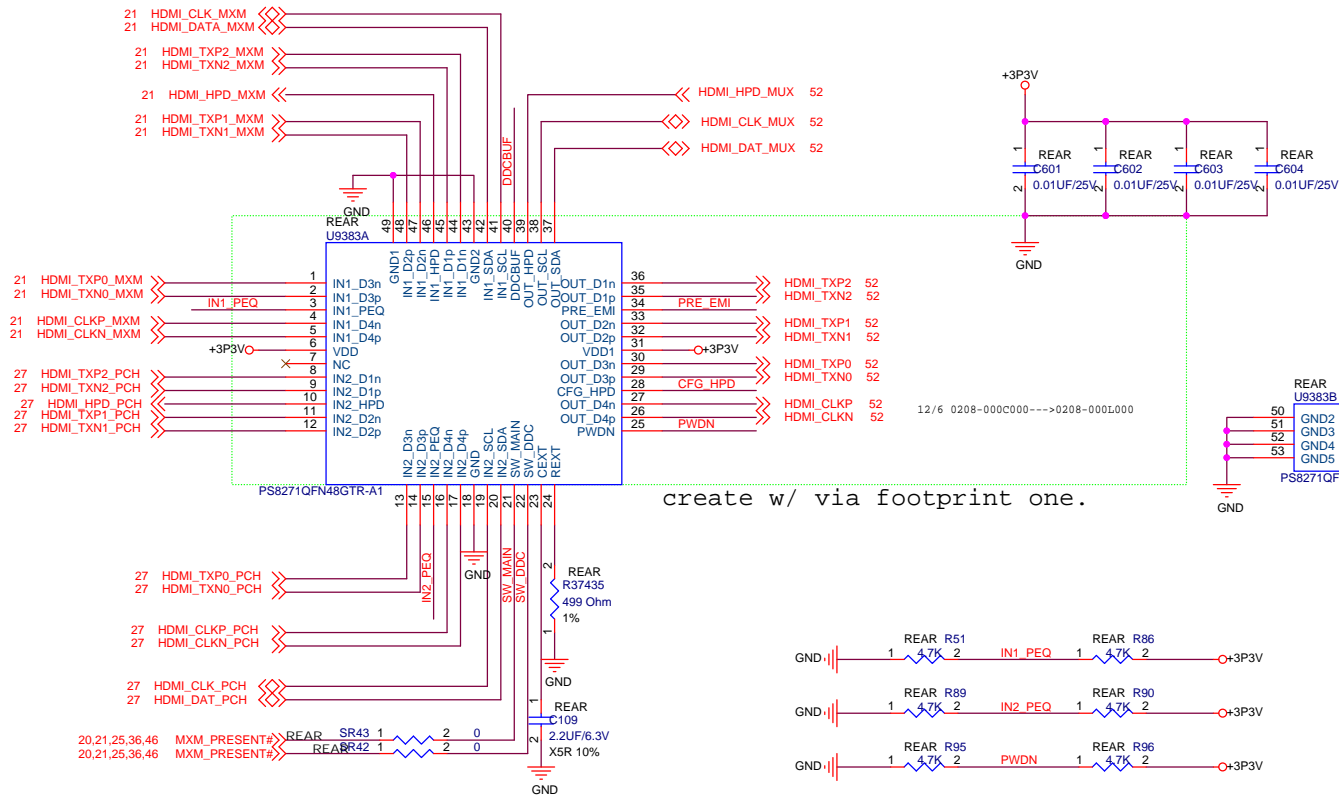
IPISB-NK

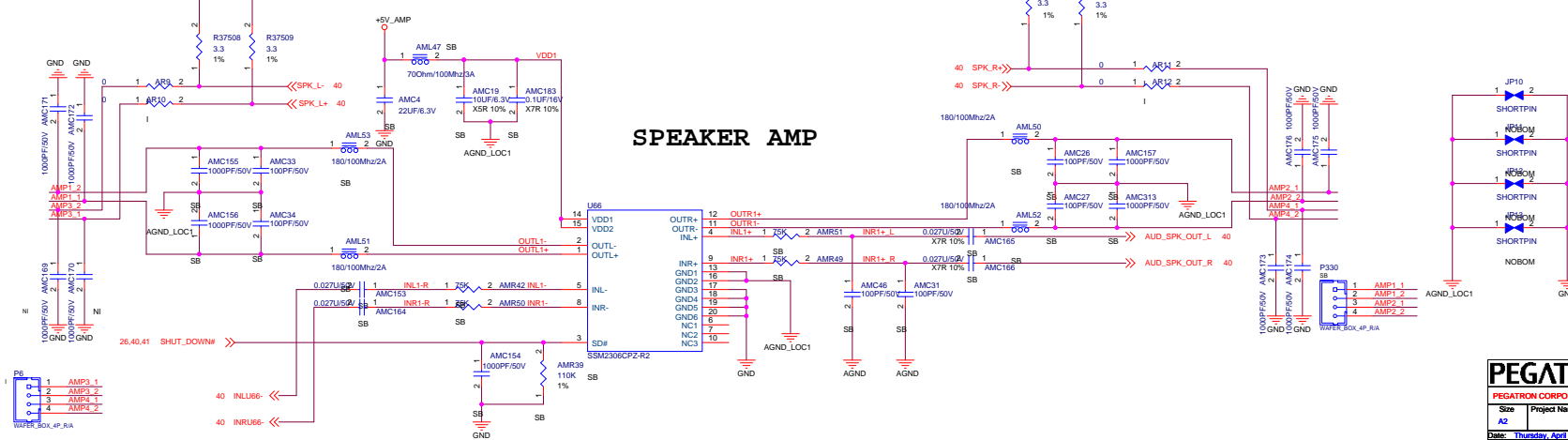
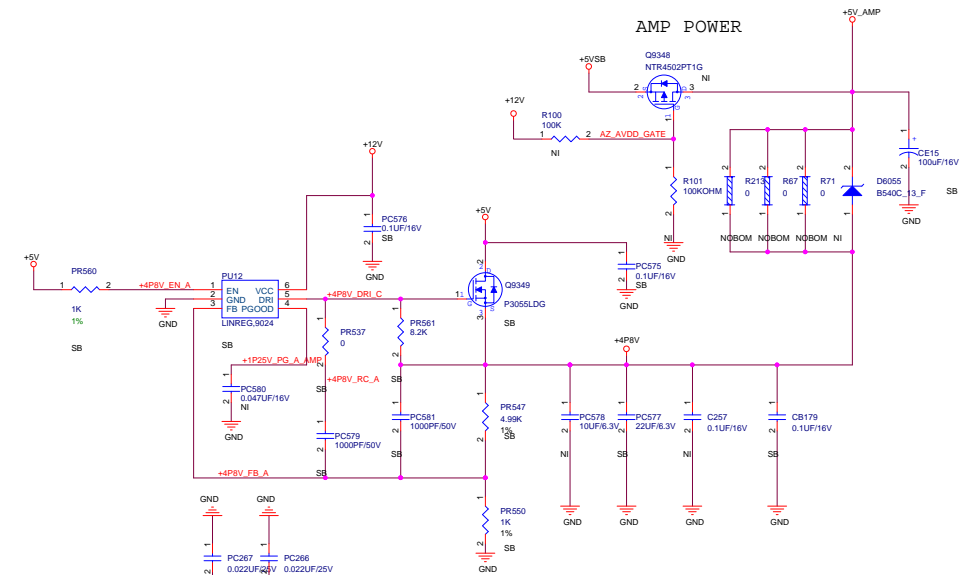
Date: Wednesday, April 20, 2011

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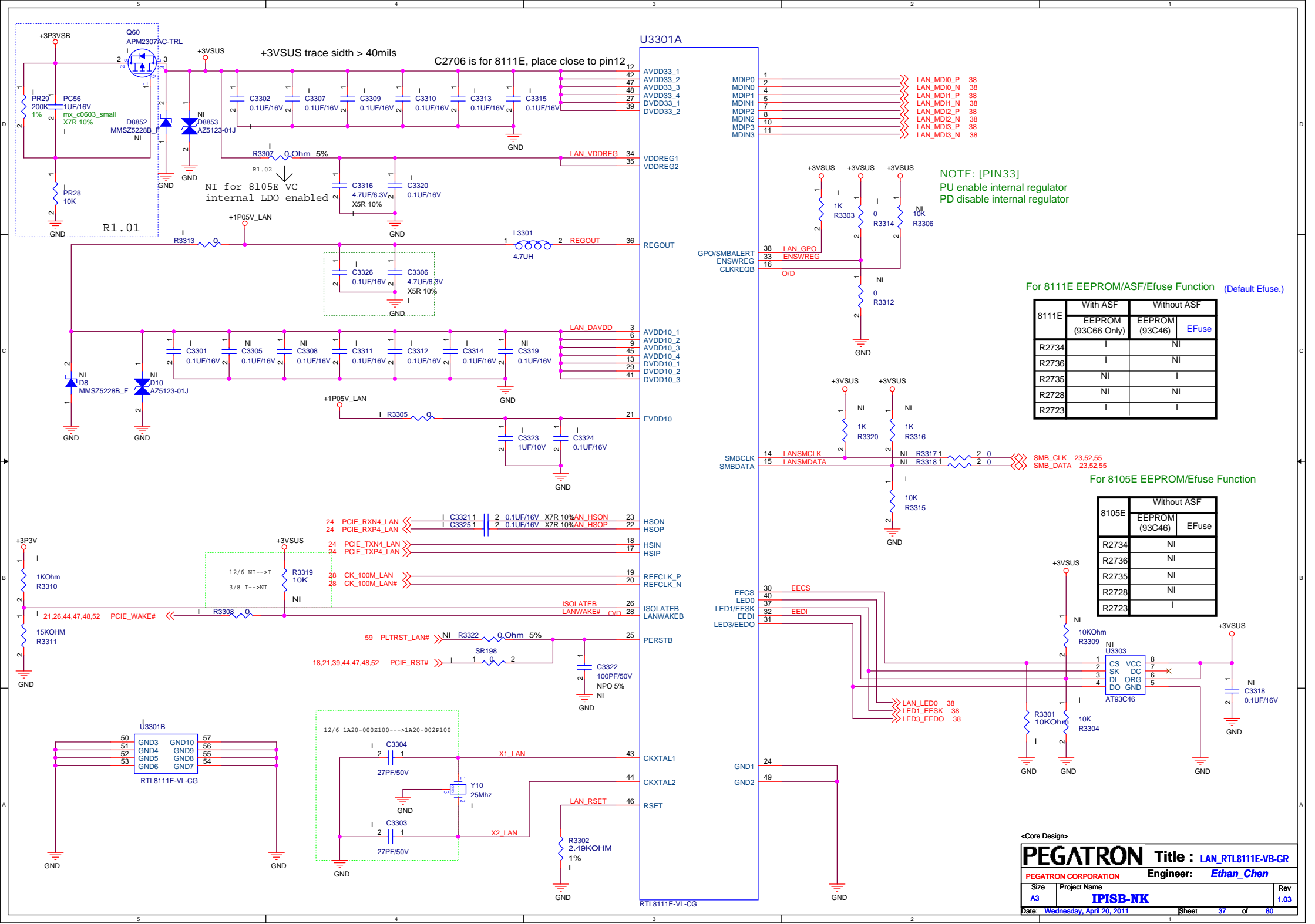
Rev

1.03

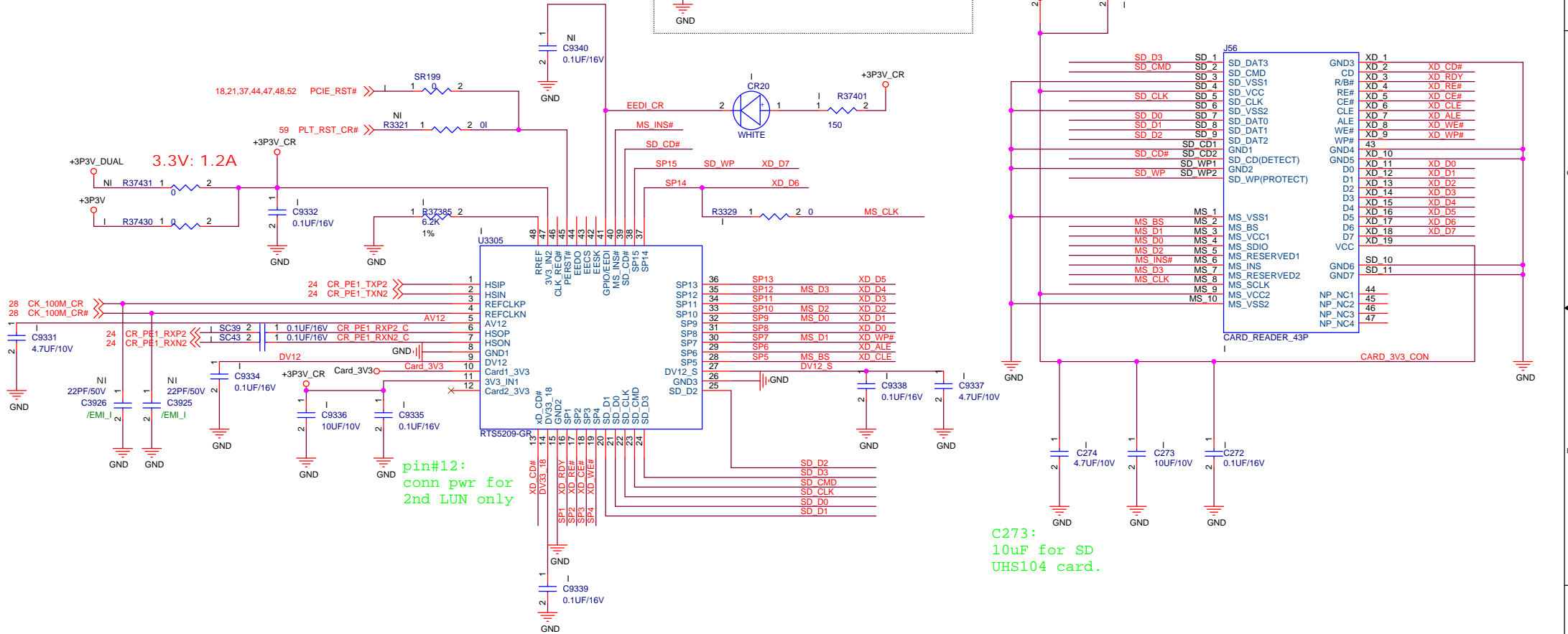
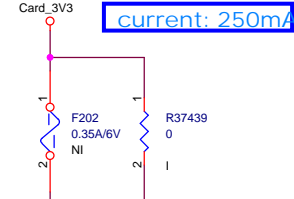
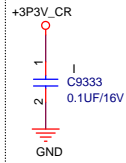




PEGATRON		Title : AMP/PWR	
PEGATRON CORPORATION		Engineer: Ethan_Chen	
Size A2	Project Name IPISE-NK	Rev 1.03	
Date: Thursday, April 21, 2011		Sheet 43 of 80	

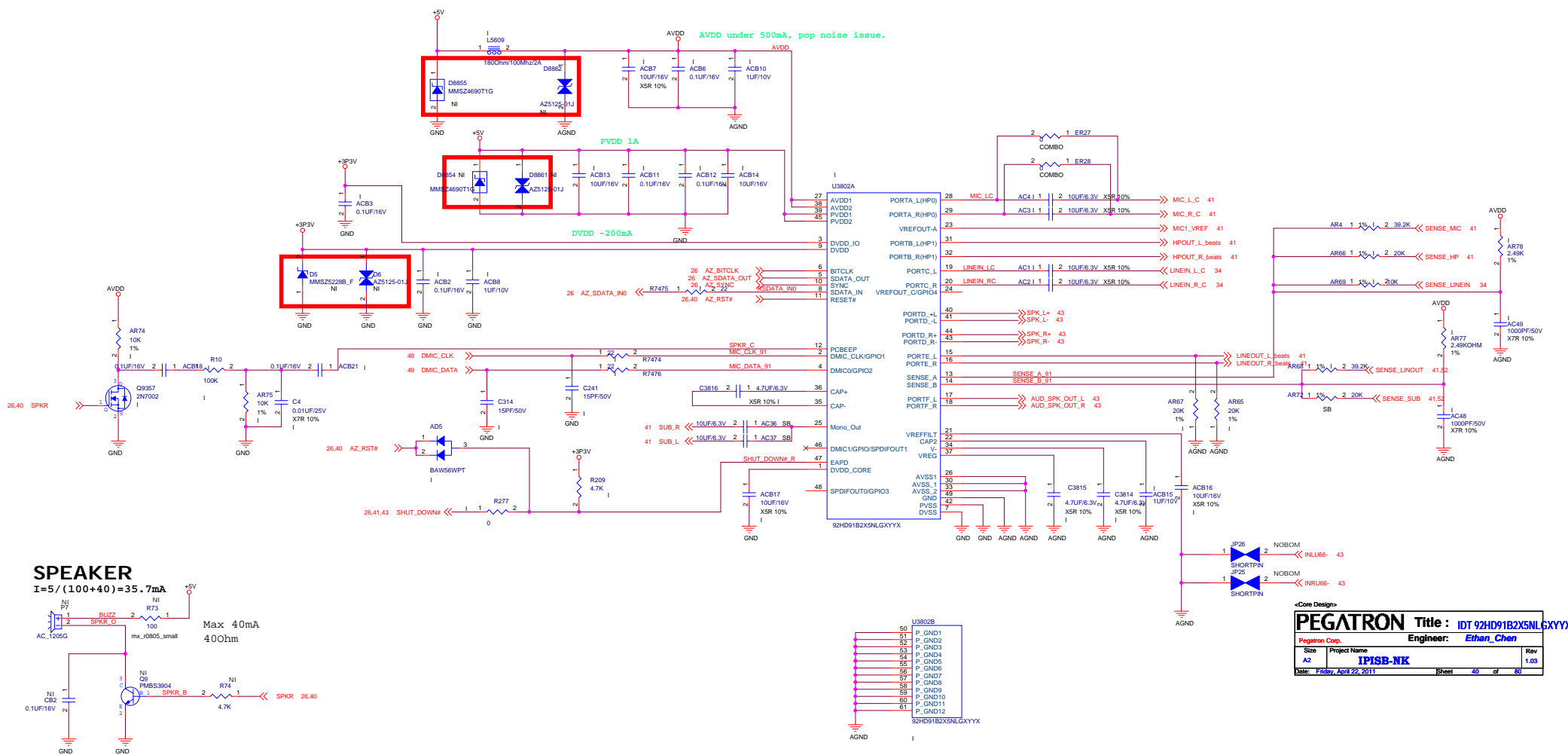


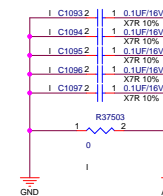
store the desired
pre-configuration information?



C273:
10uF for SD
UHS104 card.

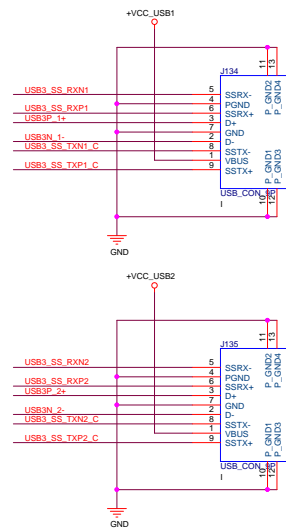
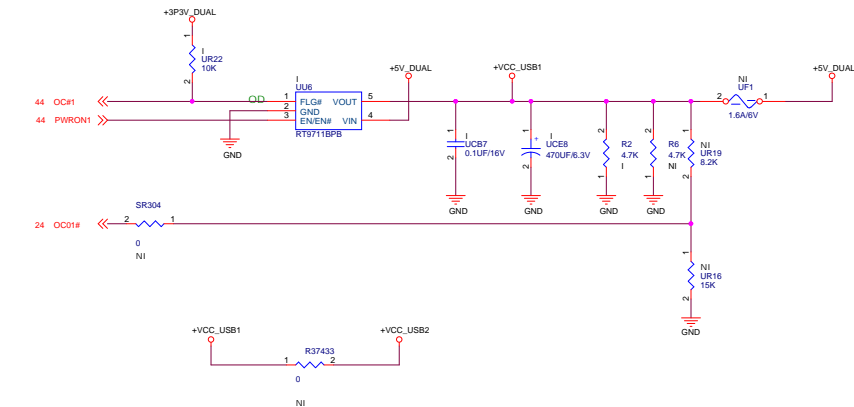
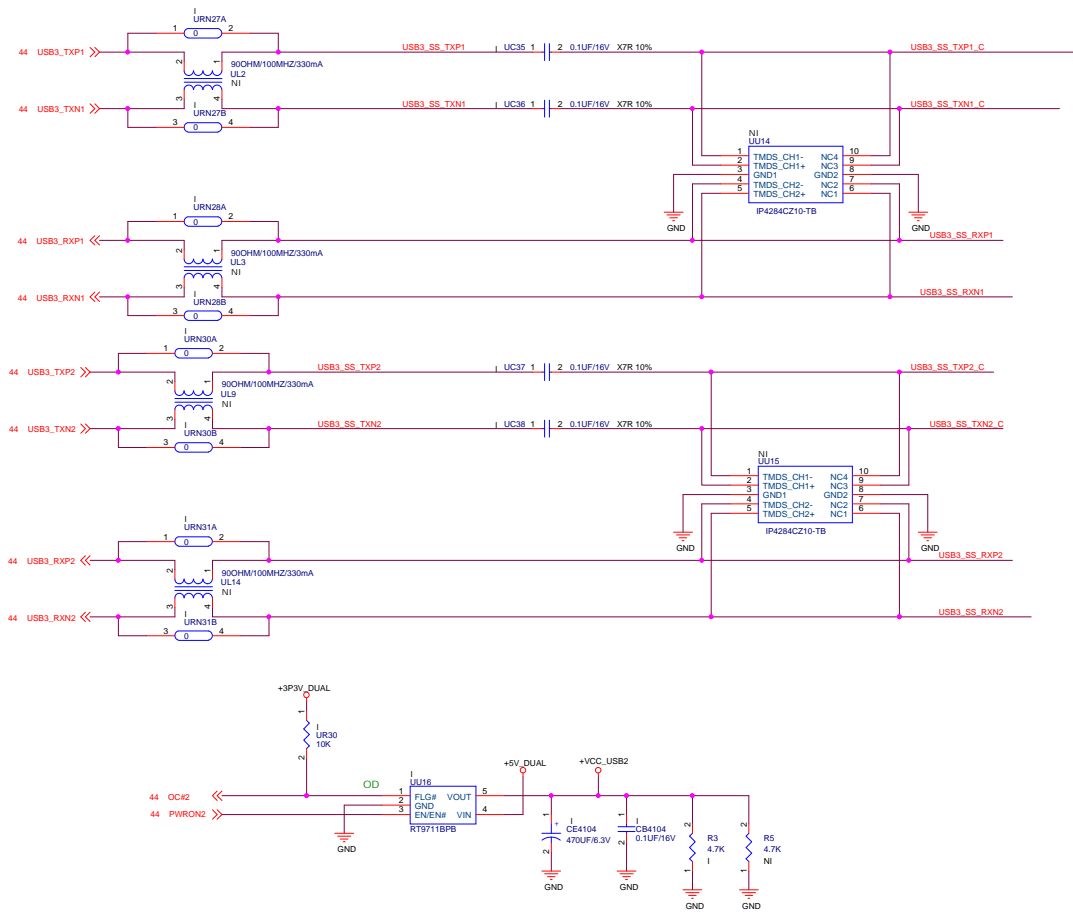
pin#12:
conn pwr for
2nd LUN only





PEGATRON		Title :	IDT789D3
PEGATRON CORPORATION		Engineer:	Ethan_Chen
Size C	Project Name IPISB-NK	Rev 1.03	
Date: Wednesday, April 20, 2011		Sheet	42 of 80

close to USB conn.

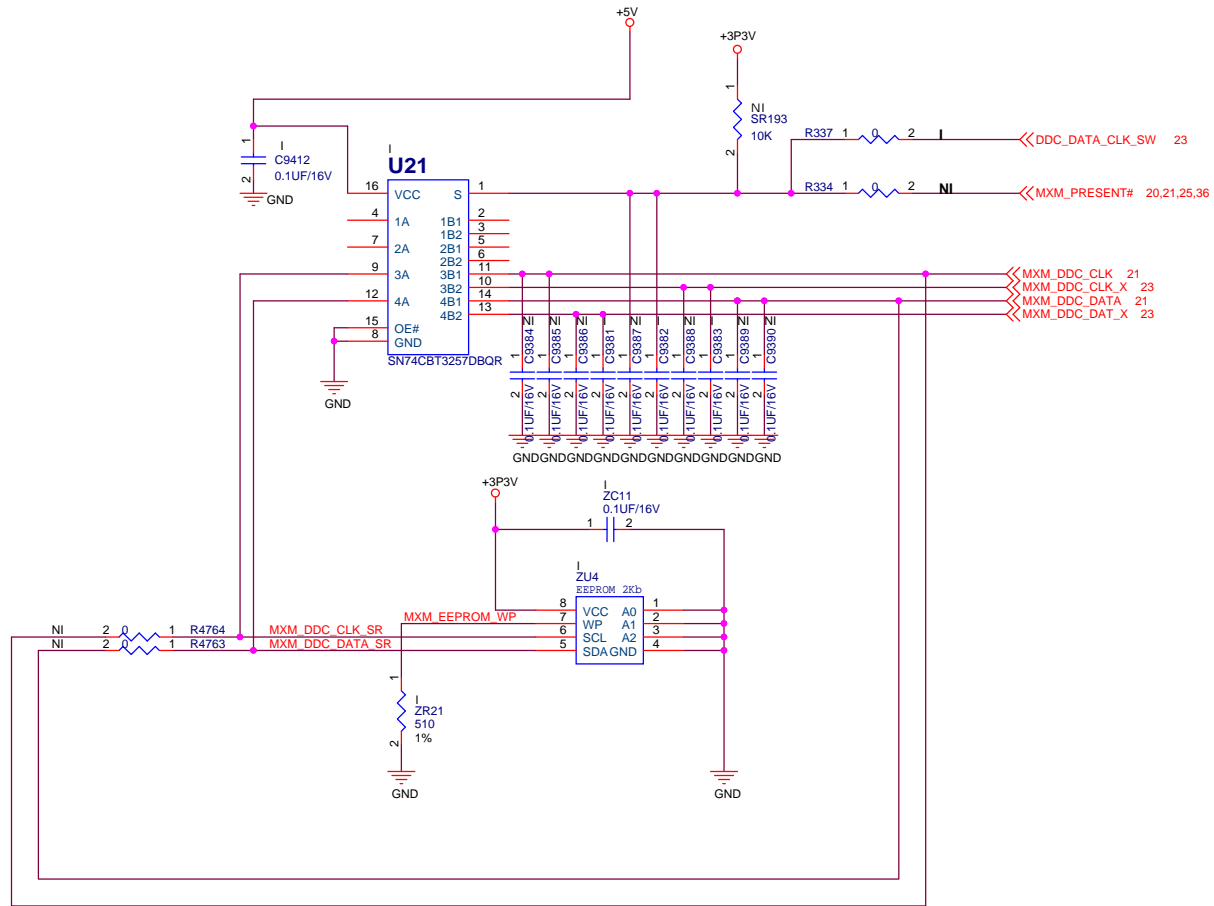


NOTE:
0722-0066000 ESD PROTECTION SOT1059 NXP/IP4284CZ10-TB
0722-003Y000 ESD PROTECTION TSLP-9-1 INFINEON/ESD5V3U4U-HDMI

1213-00LN000 USB2.0

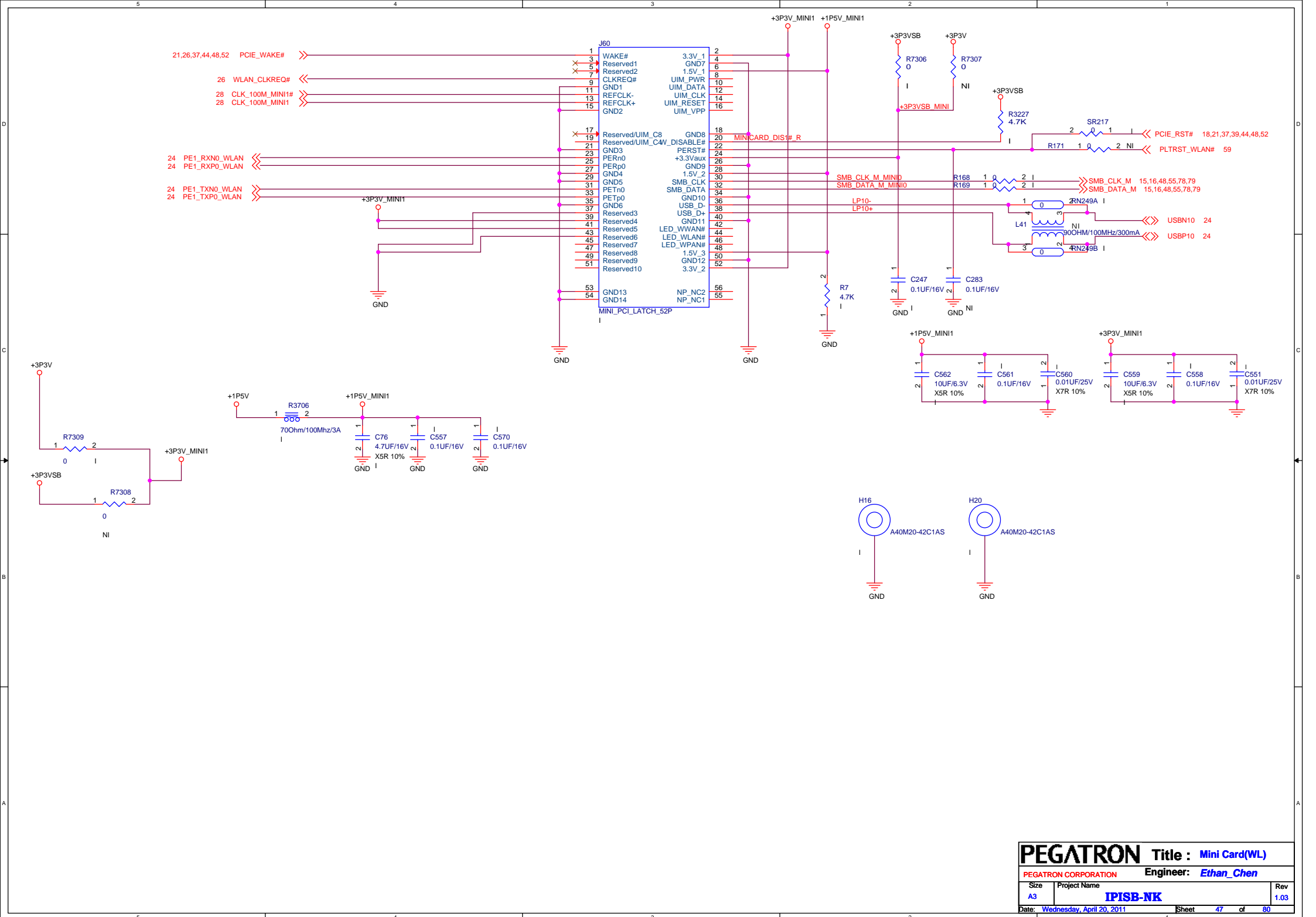
PIN NO.	1	2	3	4
SIGNAL NAME	VBUS	D-	D+	PGND
REMARK	USB2.0 CONTACT PIN			

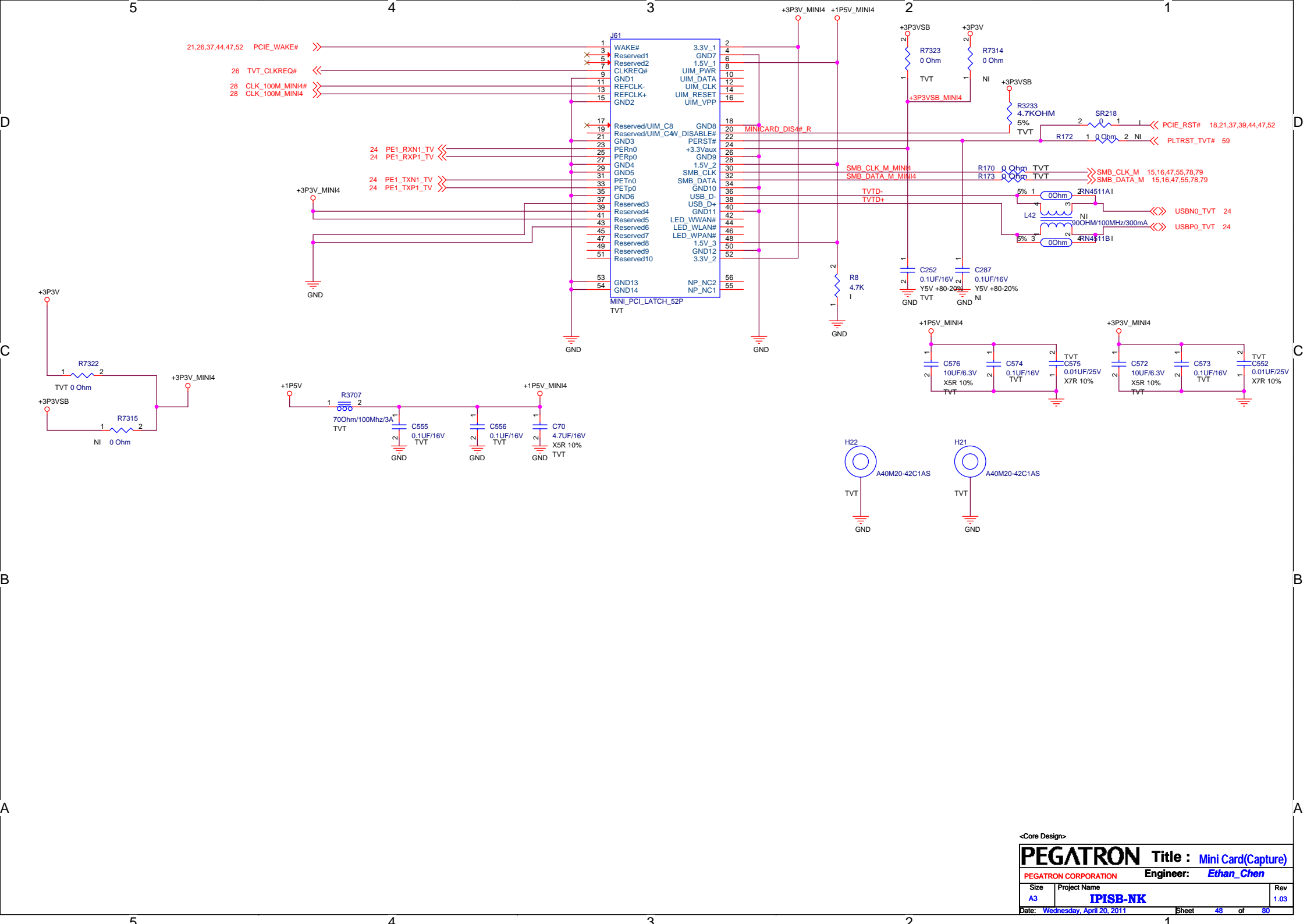
Gold flash only
Co-lay USB connector
1213-00LH000 USB3.0
1213-00LN000 USB2.0



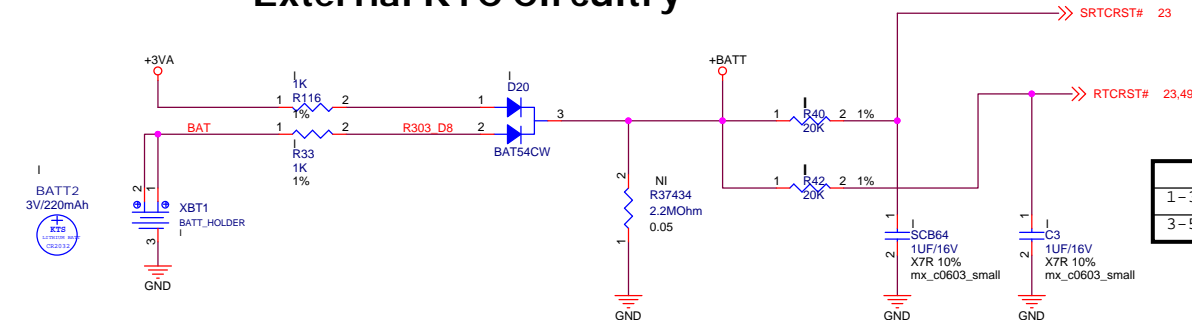
<Core Design>

PEGATRON		Title : <i>N/A</i>	
PEGATRON CORPORATION		Engineer: <i>Ethan_Chen</i>	
Size A3	Project Name IPISB-NK	Rev 1.03	
Date: Wednesday, April 20, 2011		Sheet 46 of 80	





External RTC Circuitry



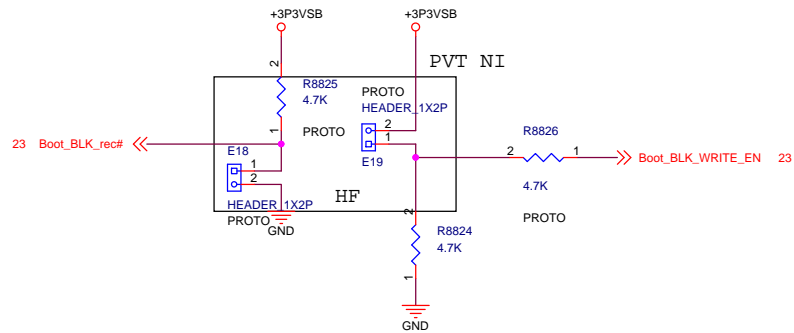
Battery Socket

NOTE:
Place C6 near PCH.

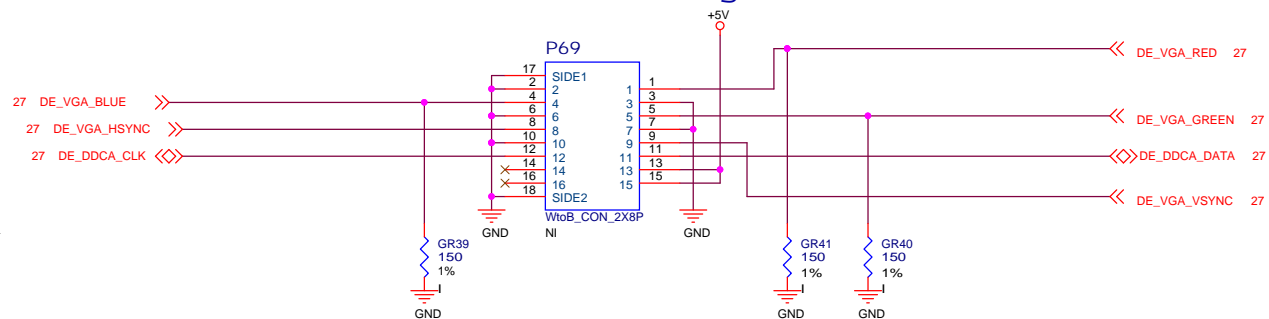
CLR CMOS AND PASSWORD CIRCUIT

PASSWORD	
1-3	CLEAR
3-5	Default

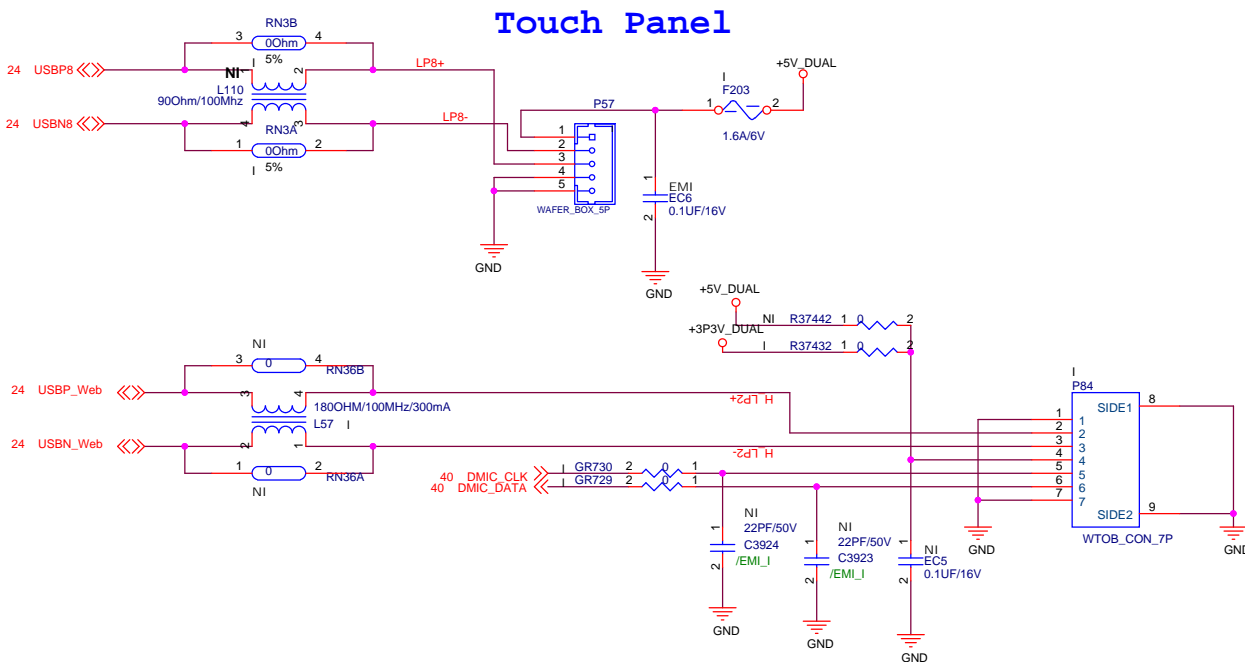
CMOS RTC	
2-4	CLEAR
4-6	Default



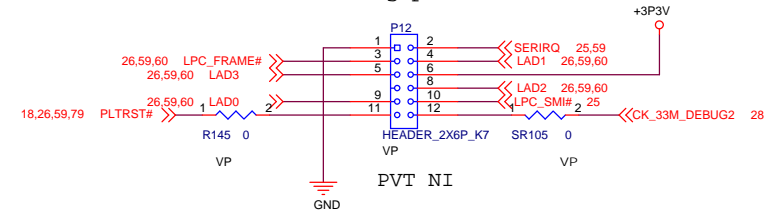
VGA Debug

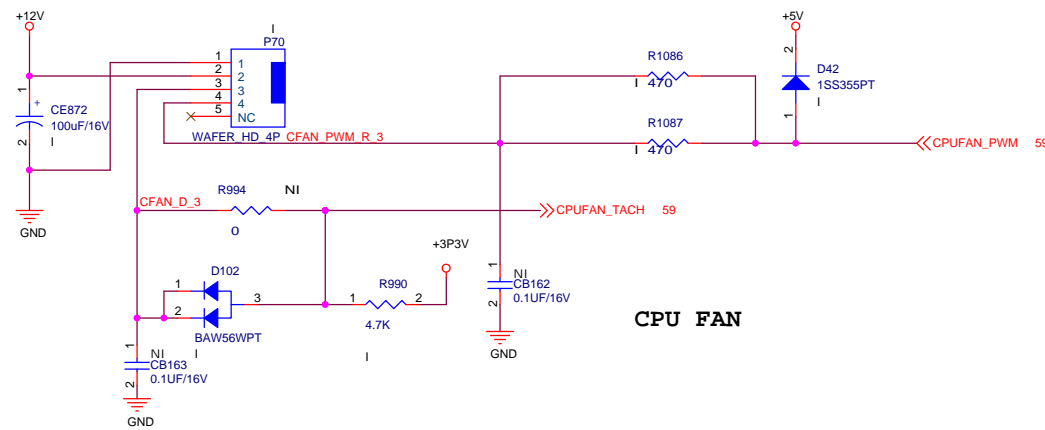


Touch Panel



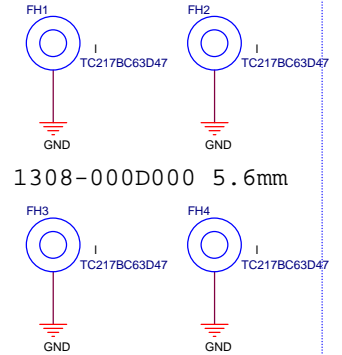
HP debug port



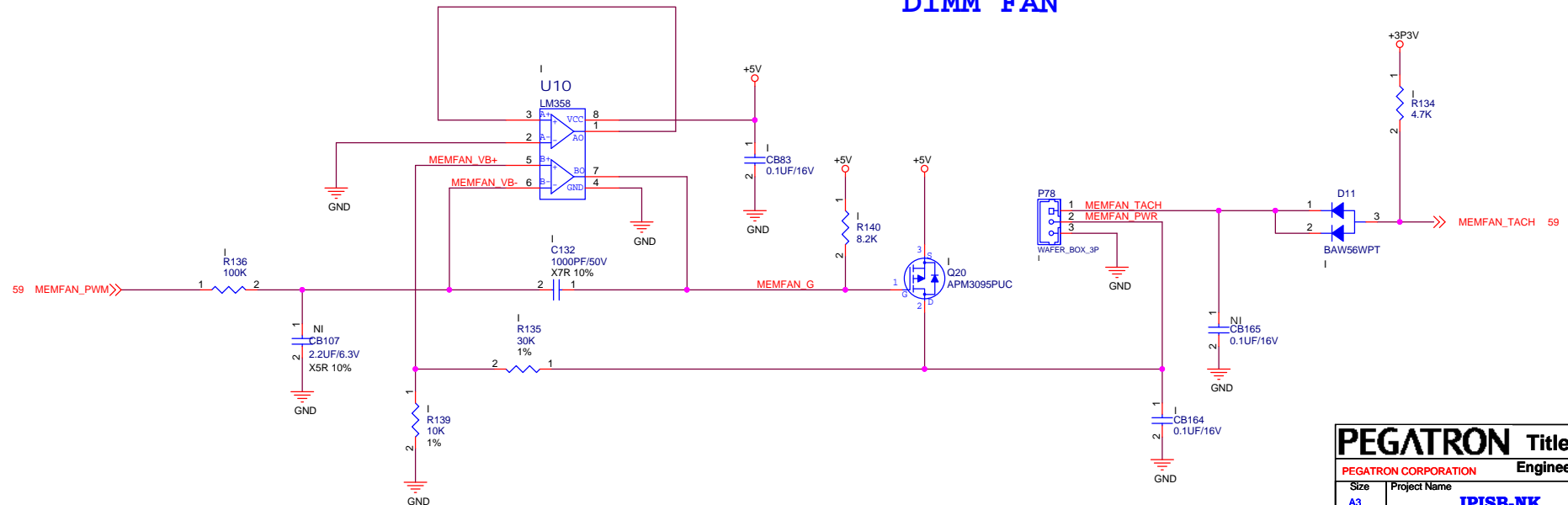


CPU FAN

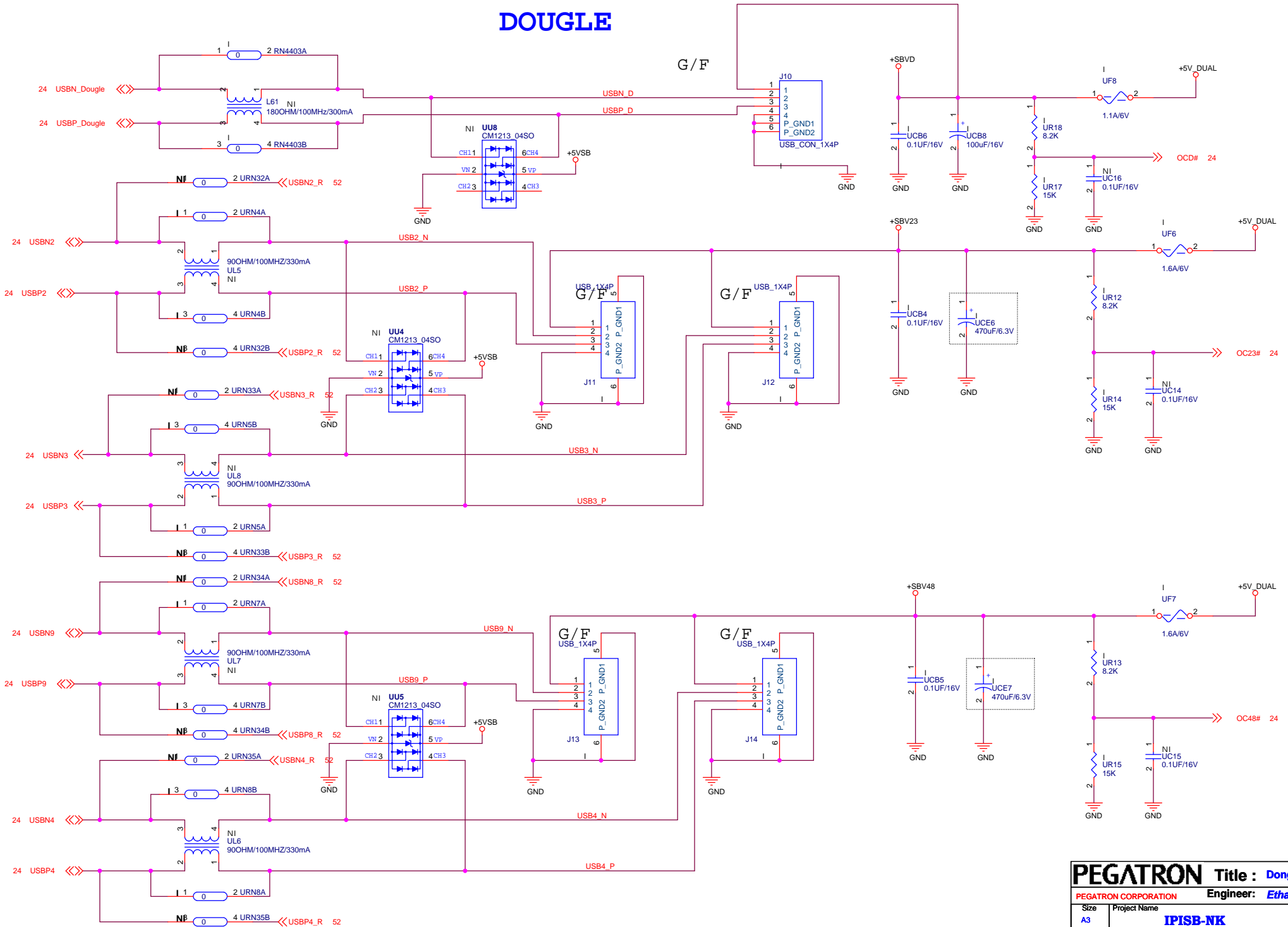
DIMM FAN NUT

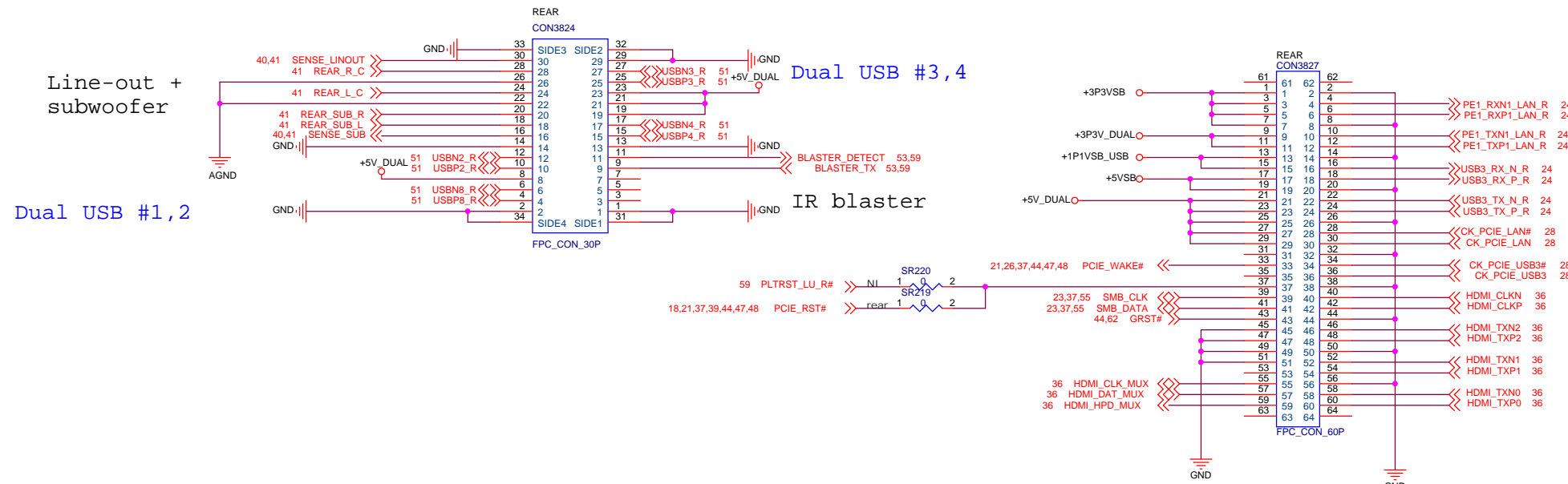


DIMM FAN

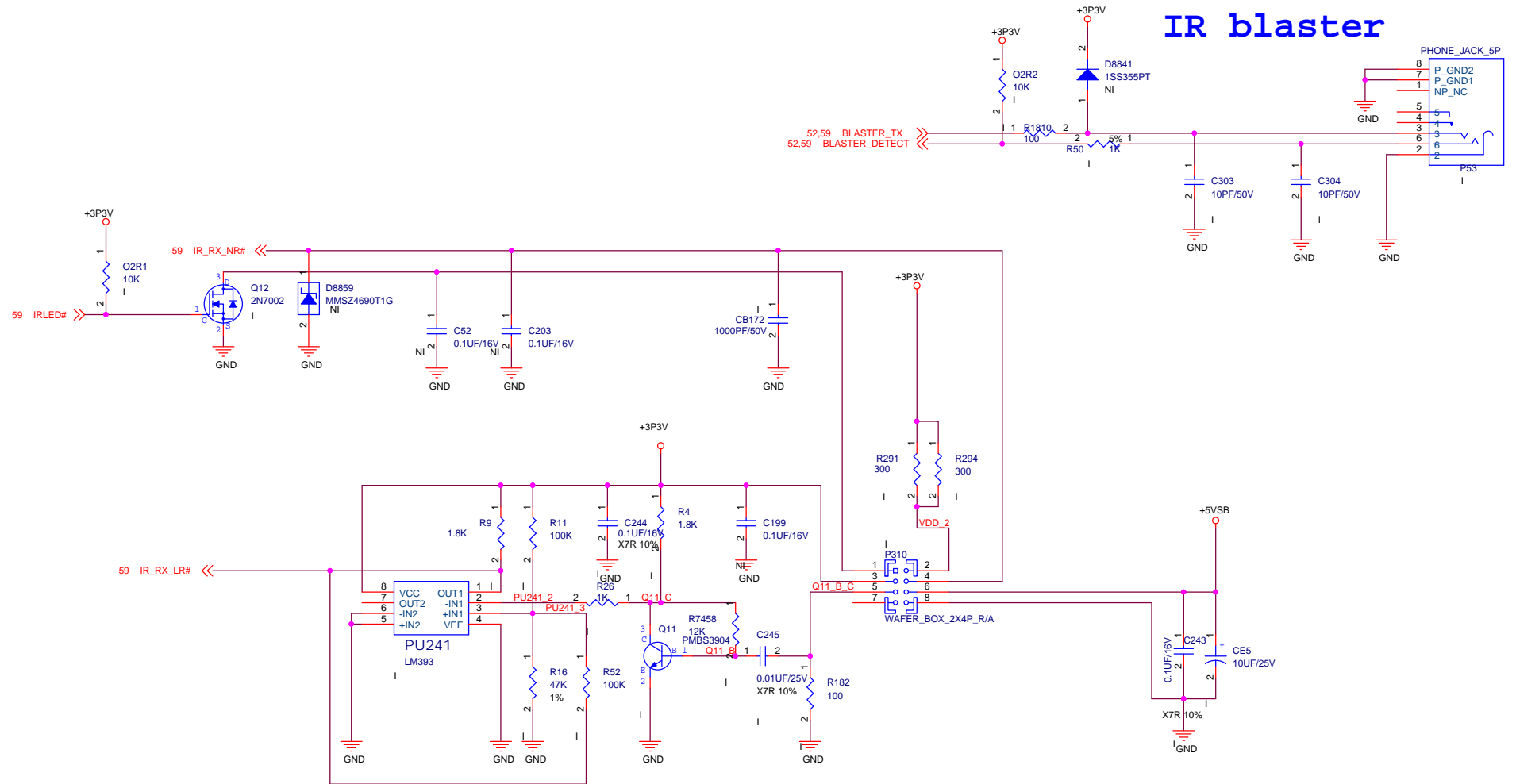


DOUGLE





IR blaster

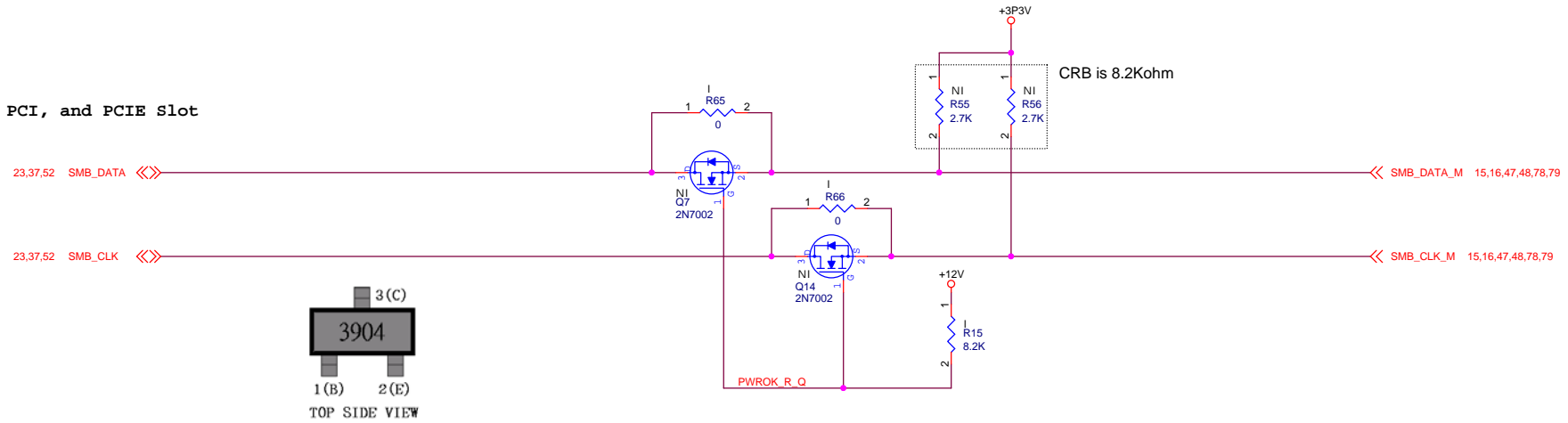


<Core Design>

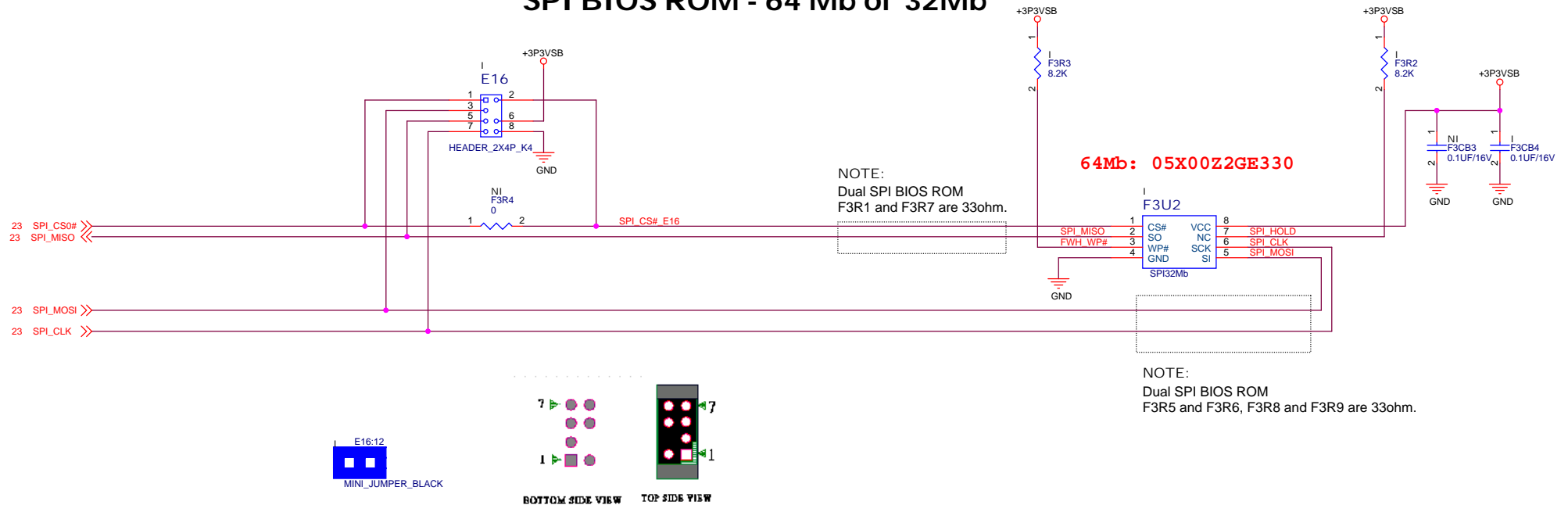
PEGATRON		Title : IR LEDs	
PEGATRON CORPORATION		Engineer: Ethan_Chen	
Size A3	Project Name IPISB-NK	Date: Thursday, April 21, 2011	Rev 1.03
Sheet 53 of 80			

SM BUS Control

To PCH, PCI, and PCIE Slot



SPI BIOS ROM - 64 Mb or 32Mb



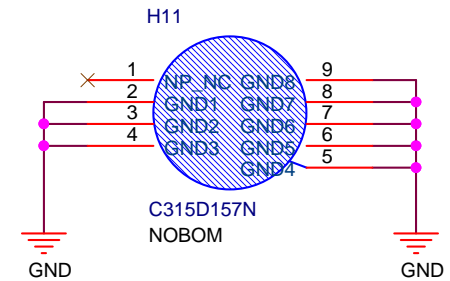
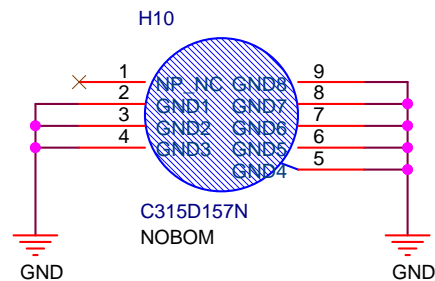
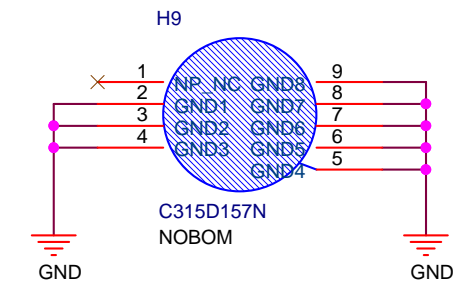
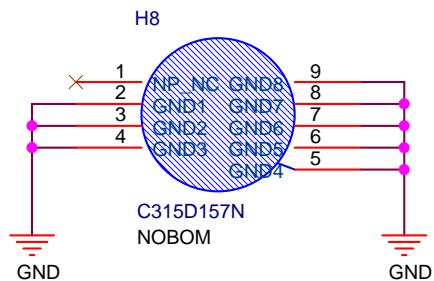
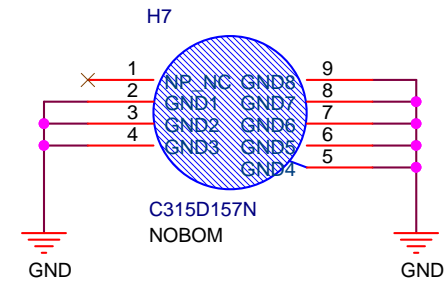
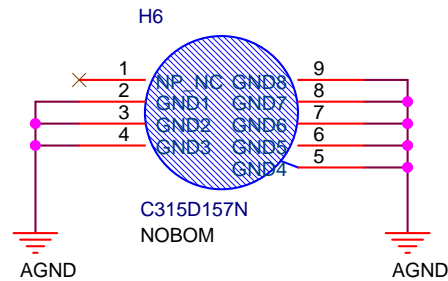
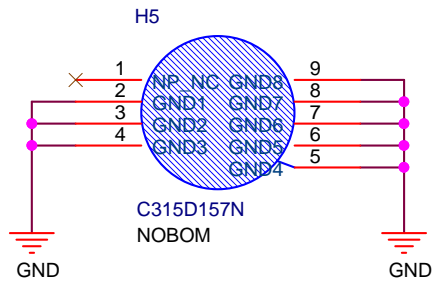
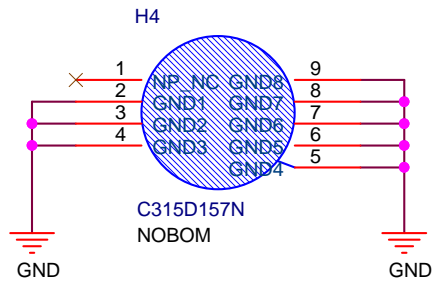
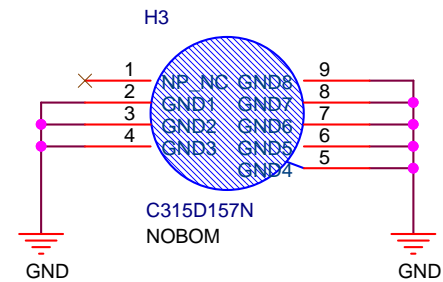
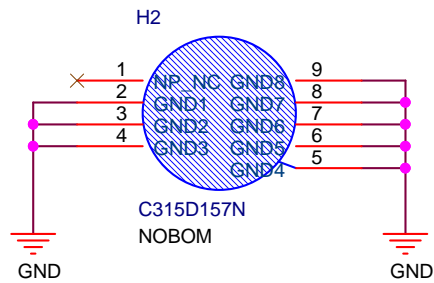
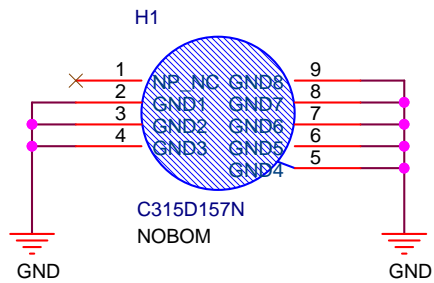
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SM BUS & SPI ROM

PEGATRON CORPORATION Engineer: Ethan_Chen

Size	Project Name	Rev
A3	IPISB-NK	1.03

Date: Wednesday, April 20, 2011 Sheet 55 of 80

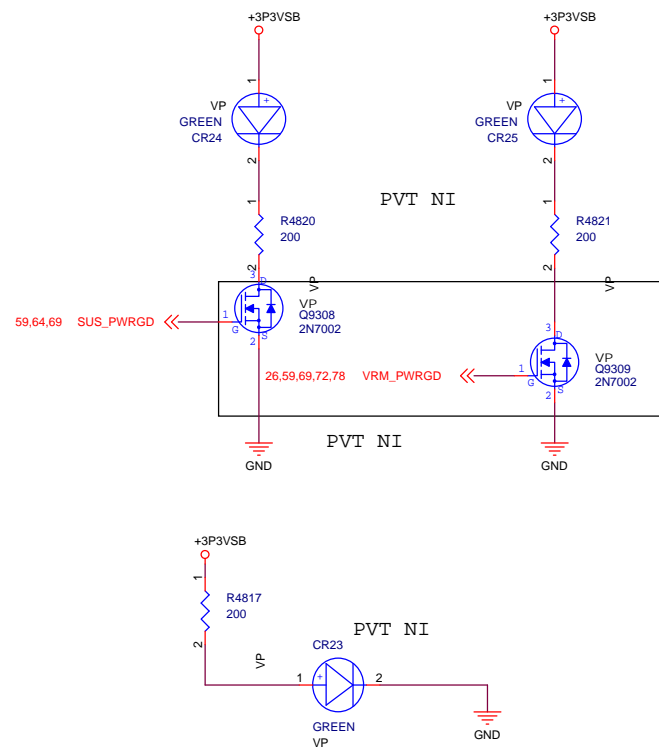
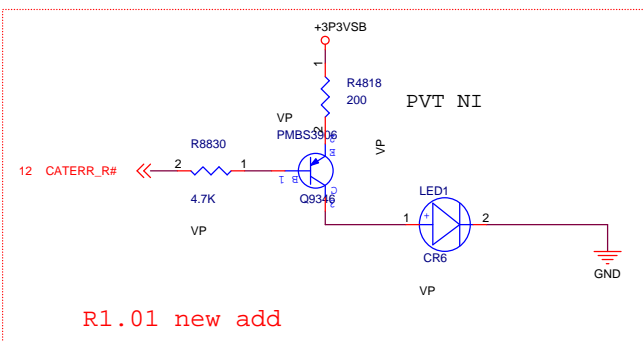
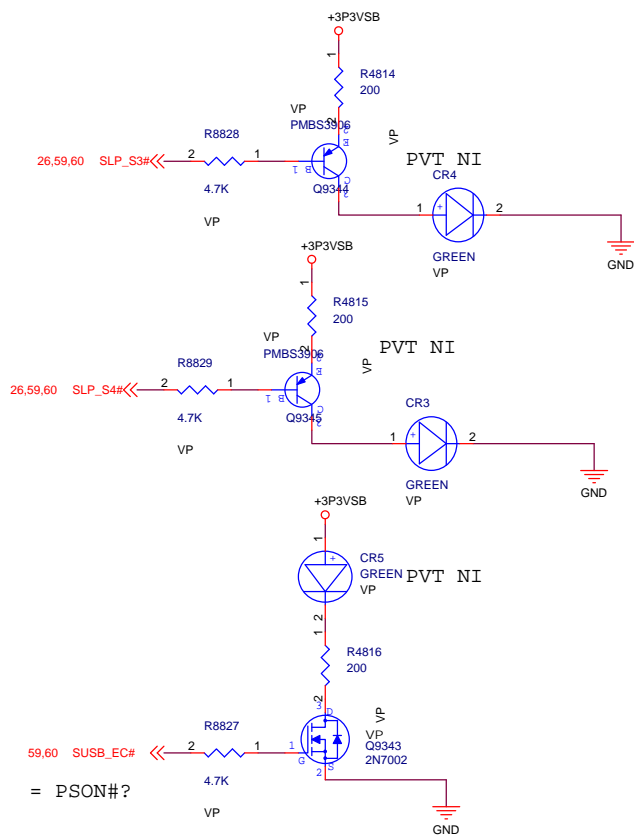


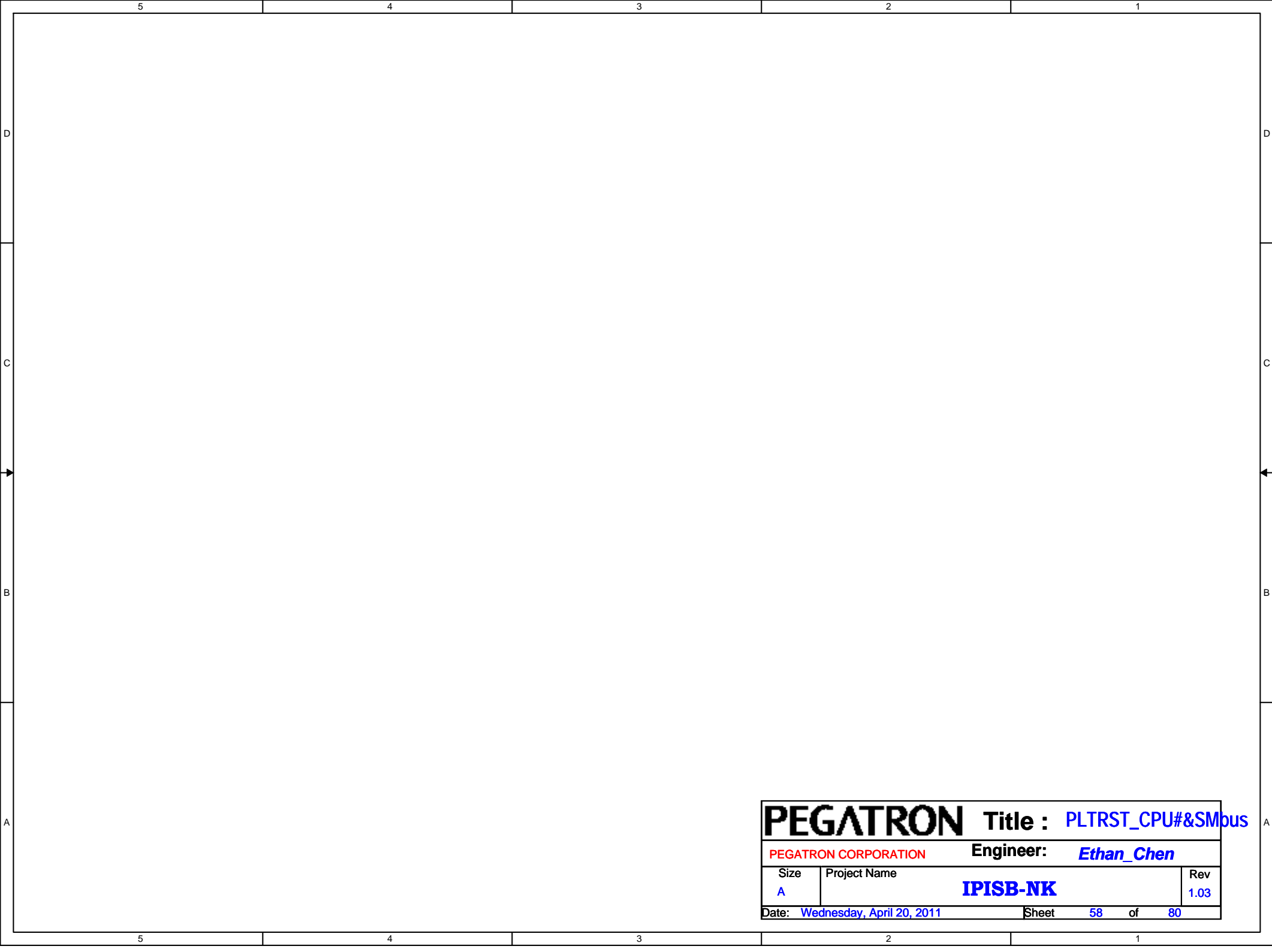
08M1-14B2200 08M1-14B3100
08M1-14B2000 08M1-14B3000
08M1-14B2100 08M1-14B3200

VESA mount hole

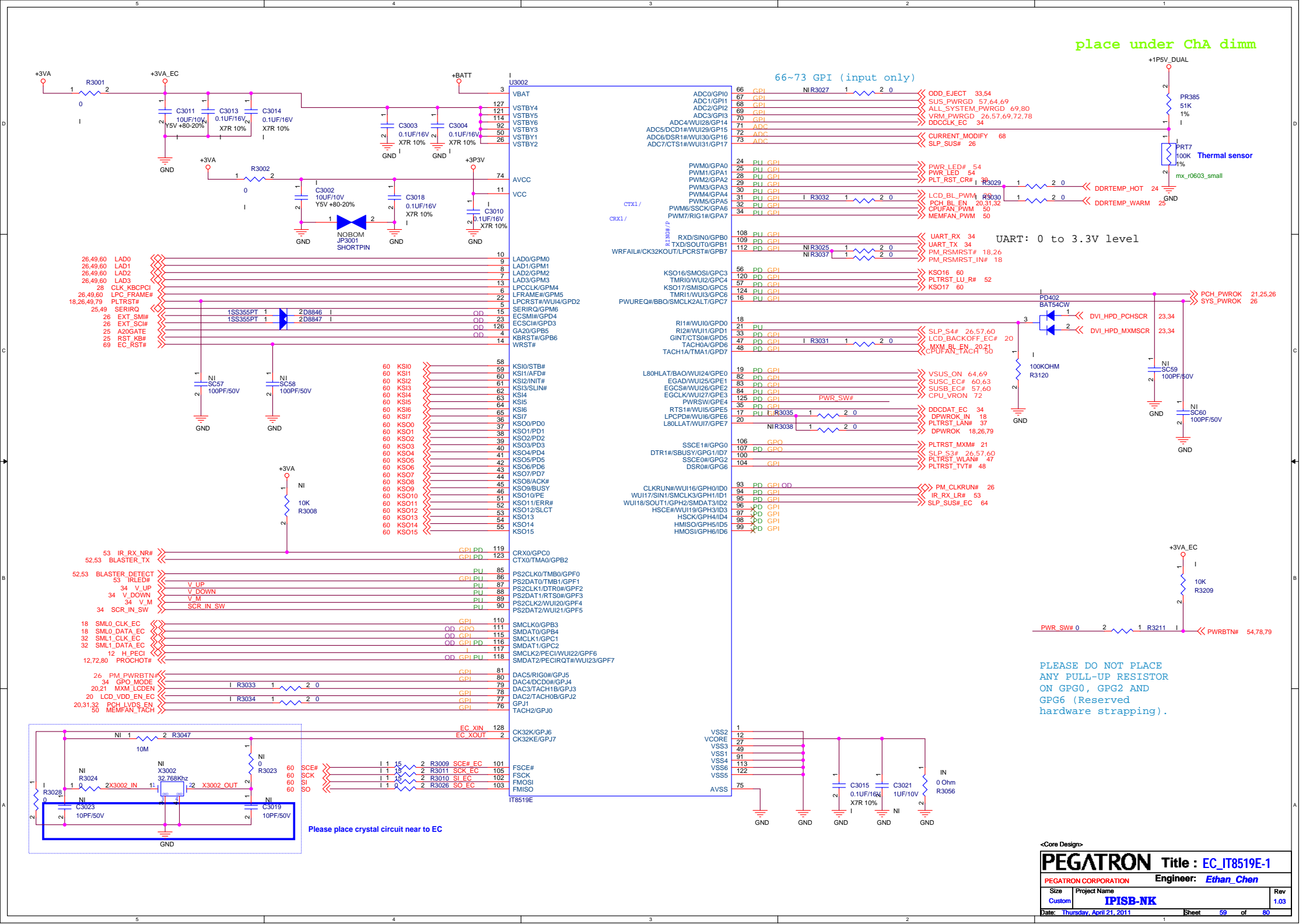
<Core Design>

PEGATRON		Title : SCREW HOLE	
PEGATRON CORPORATION		Engineer: Ethan_Chen	
Size A	Project Name IPISB-NK		Rev 1.03
Date: Wednesday, April 20, 2011		Sheet 56 of 80	





PEGATRON		Title : PLTRST_CPU#&Smbus	
PEGATRON CORPORATION		Engineer: Ethan_Chen	
Size A	Project Name IPISB-NK		Rev 1.03
Date: Wednesday, April 20, 2011		Sheet 58 of 80	



SPI ROM+ External programming conn.

The diagram illustrates the external programming connection for the SPI ROM+ (U9216, MX25L512CMI-12G). The chip is connected to a +3VA supply and ground. The connections are as follows:

- Pin 1 (CS#):** Connected to SCE# through a 10K resistor (R3122) to +3VA_SPI.
- Pin 2 (SO):** Connected to SO through an 8.2K resistor (R3119) to +3VA_SPI.
- Pin 3 (VCC):** Connected to +3VA_SPI.
- Pin 4 (WP#):** Connected to GND.
- Pin 5 (HOLD#):** Connected to SPI_HOLD#.
- Pin 6 (SCK):** Connected to SCK through a 10K resistor (R3121) to +3VA_SPI.
- Pin 7 (SI):** Connected to SI through an 8.2K resistor (R3103) to +3VA_SPI.
- Pin 8 (GND):** Connected to GND.

A 0.1uF capacitor (C3115) is connected between +3VA and GND, with a 10% tolerance. The diagram is labeled with component values and pin numbers.

05X00Z2FC330 32Mb
0500-00P5000 (512Kb SPI)

Note: Close to EC

Debug Card CON

26,49,59 LAD0
26,49,59 LAD1
26,49,59 LAD2
26,49,59 LAD3
26,49,59 LPC_FRAME#
28 CLK_DBGPC11

VP J120 14 13
SIDE1 SIDE2
SIDE3 SIDE4
SIDE5 SIDE6
SIDE7 SIDE8
SIDE9 SIDE10
SIDE11 SIDE12
16 15
ZIF_CON_12P

1 1
2 2
3 3
4 4
5 5
6 6
7 7
8 8
9 9
10 10
11 11
12 12

NI C3802 10PF/50V
GND

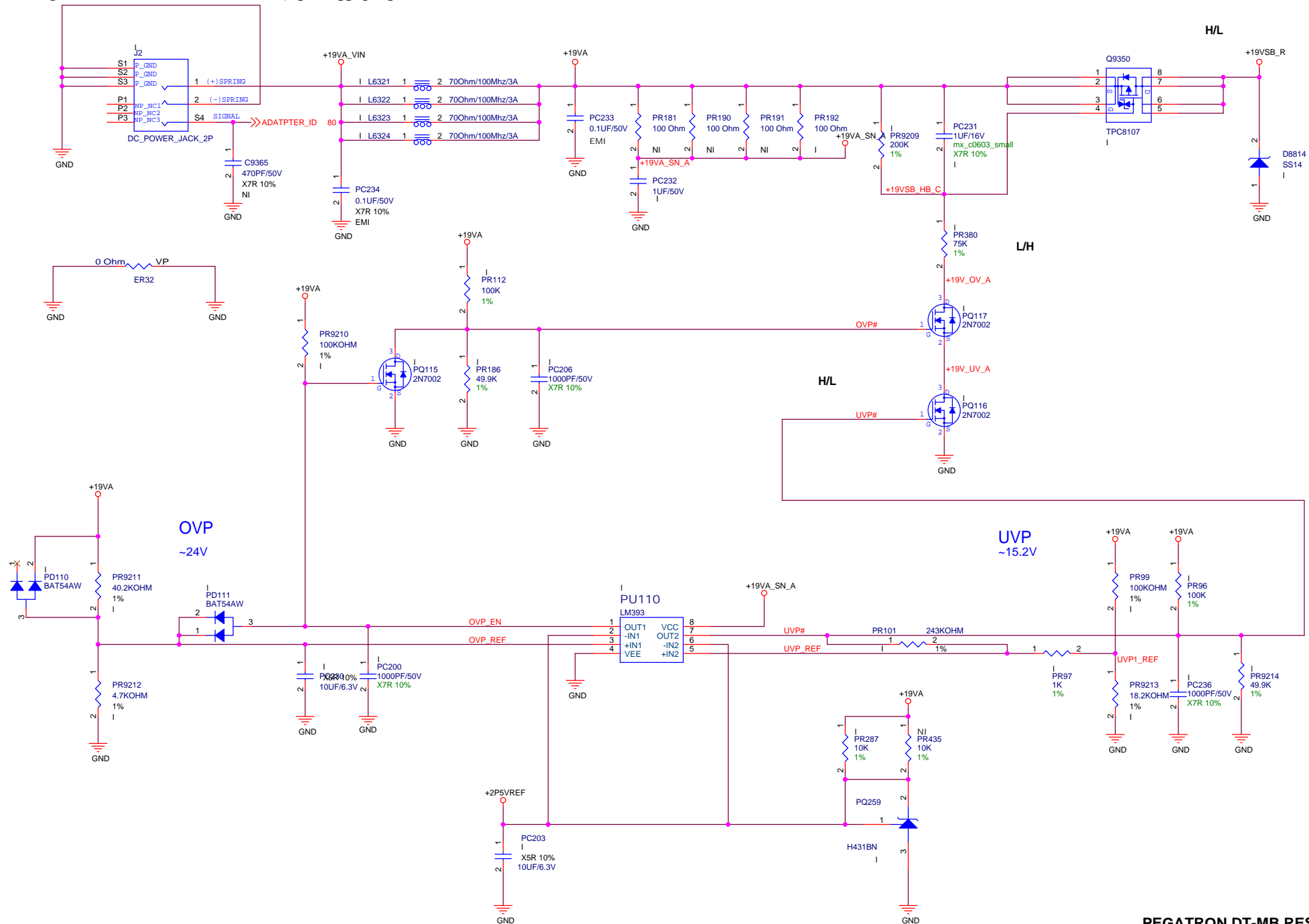
+3P3V
NI CB158 0.1UF/16V
GND

57,59,60 SUSB_EC# 1 PR914 2 SUSB_PWR 63,65,66,69
1K

[illegible]

<Core Design>			
PEGATRON		Title : ECJT8519E-2	
PEGATRON CORPORATION		Engineer: Ethan_Chen	
Size Custom	Project Name IPISB-NK		Rev 1.03
Date: Thursday, April 21, 2011		Sheet 60 of 80	

change to SIMULA /AJ261B-Y090-42F, p/n applying....



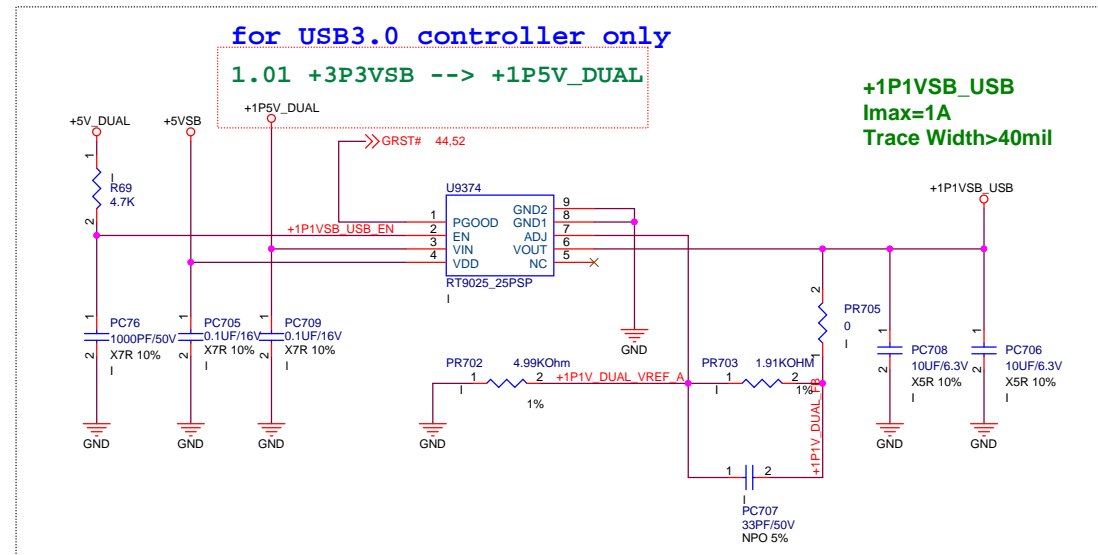
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : UVP, OVP & +19VSB

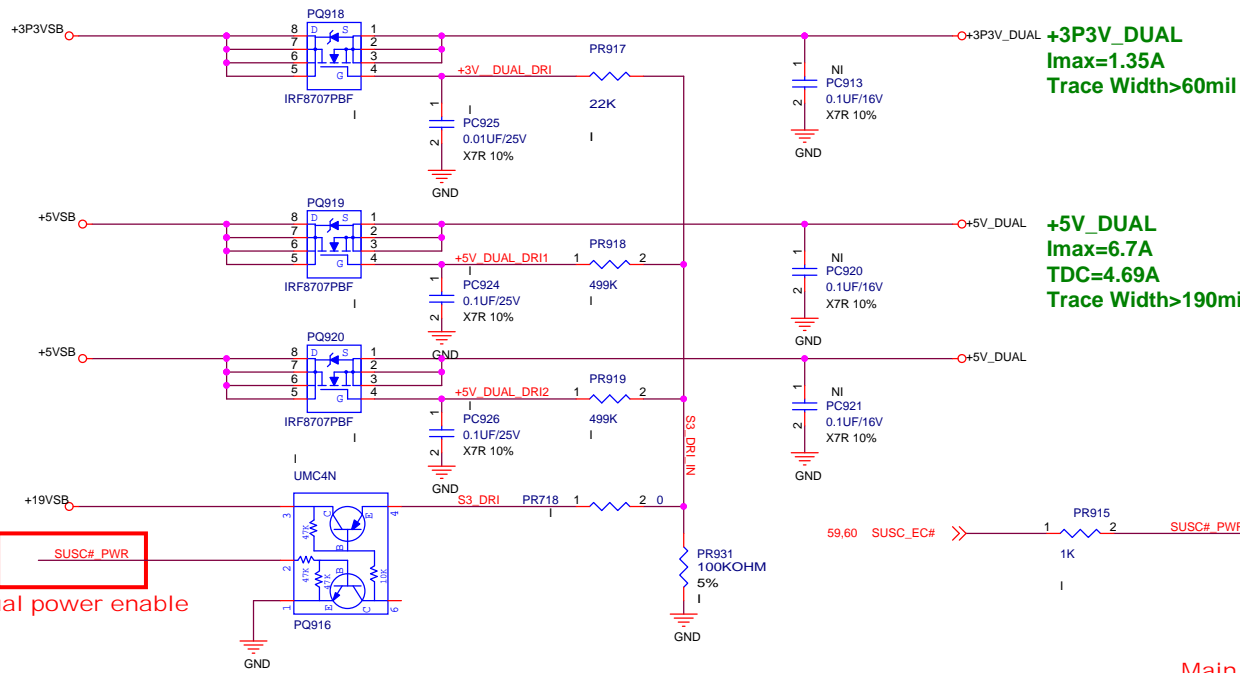
PEGATRON CORPORATION Engineer: Ethan_Chen

Size A3	Project Name IPISB-NK	Rev 1.03
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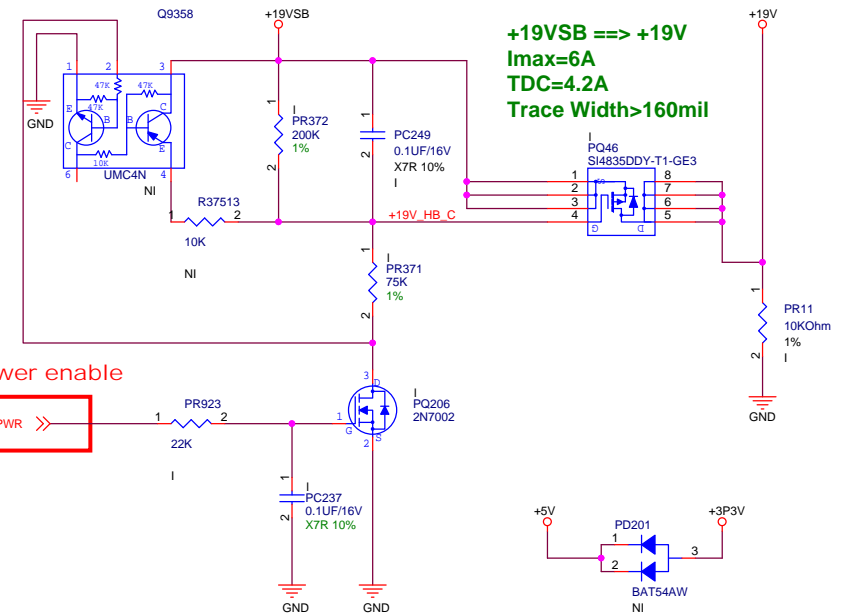
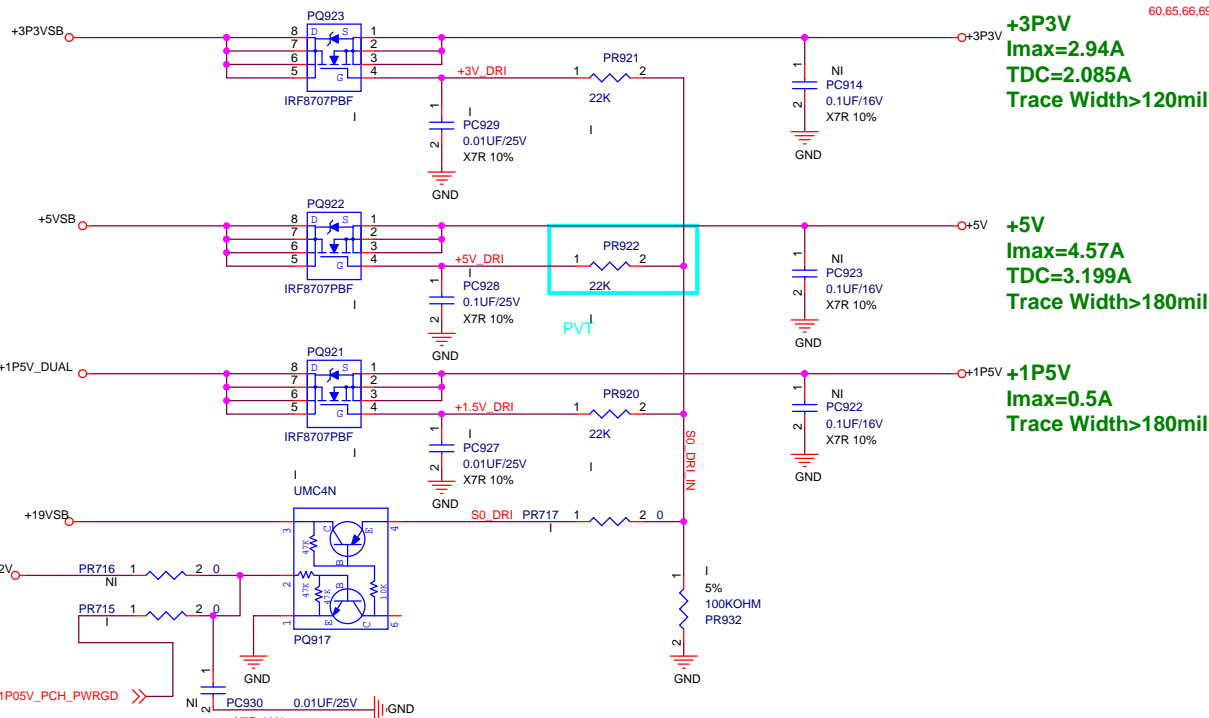
Date: Wednesday, April 20, 2011 Sheet 61 of 80



Dual_PWR Load SW



Main_PWR Load SW



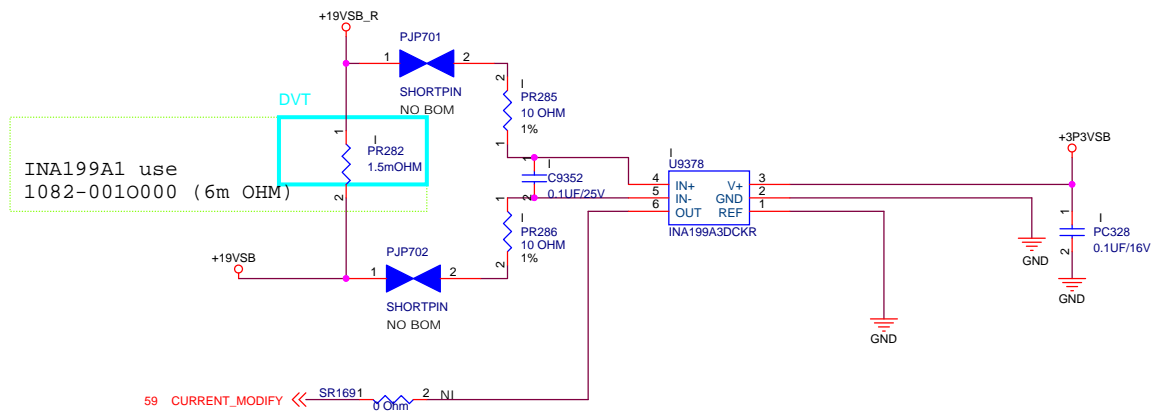
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : ATX POWER_24P

PEGATRON CORPORATION Engineer: Ethan_Chen

Size A3 Project Name IPISB-NK Rev 1.03

Date: Thursday, April 21, 2011 Sheet 63 of 80



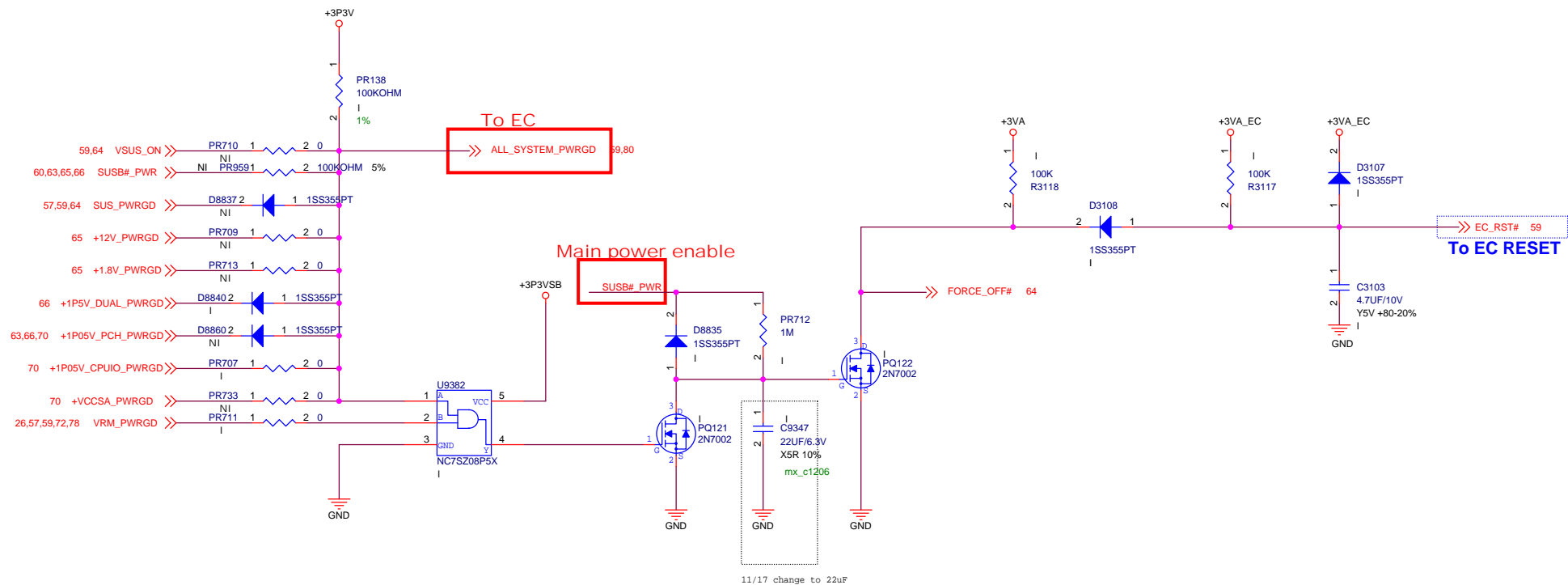
PEGATRON DT-MB RESTRICTED SECRET

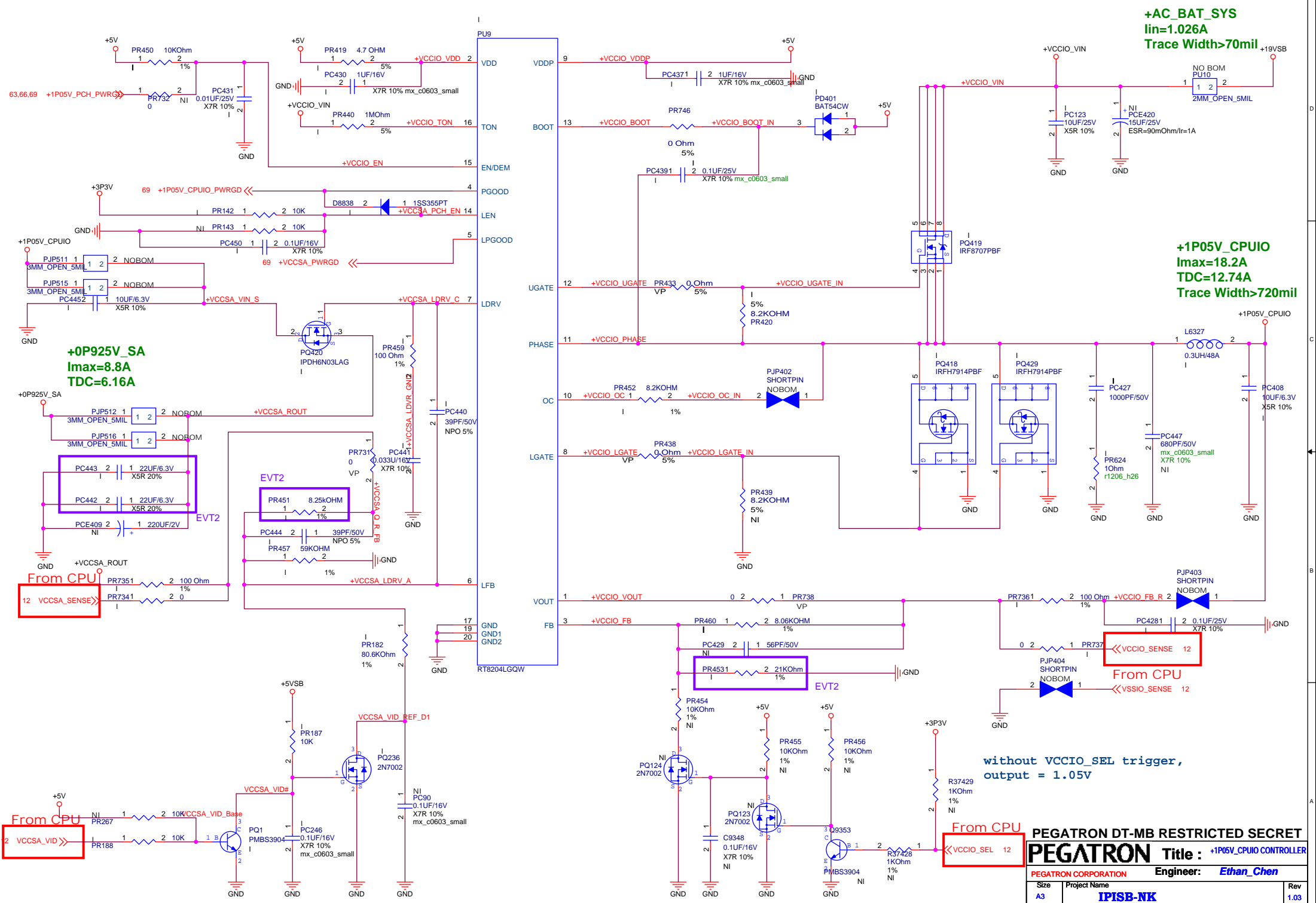
PEGATRON Title : N/A

PEGATRON CORPORATION Engineer: Ethan_Chen

Size A3	Project Name IPISB-NK	Rev 1.03
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Date: Wednesday, April 20, 2011 Sheet 68 of 80



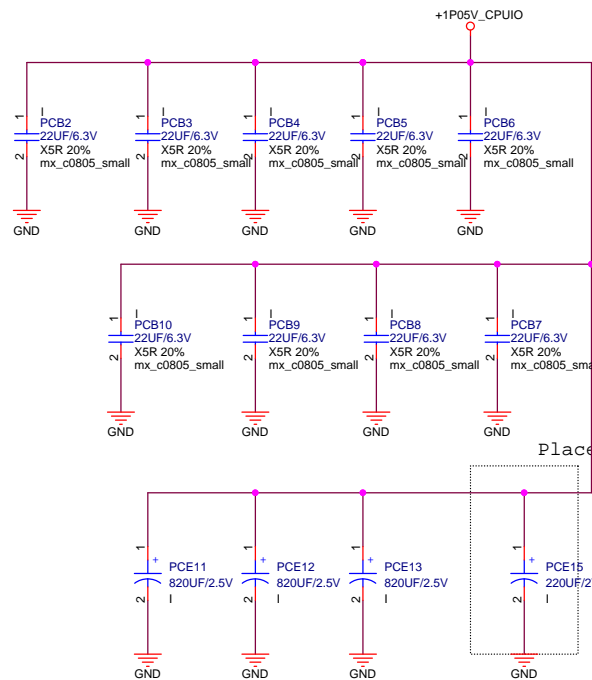
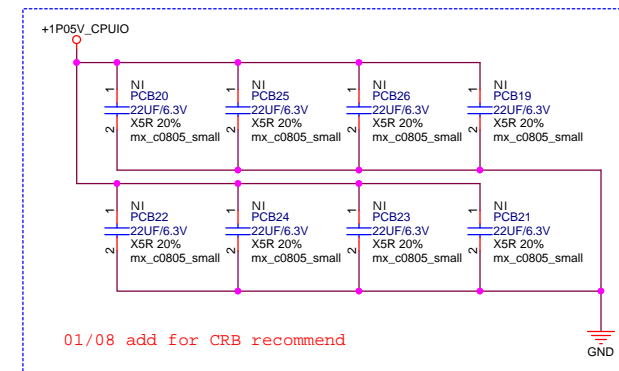
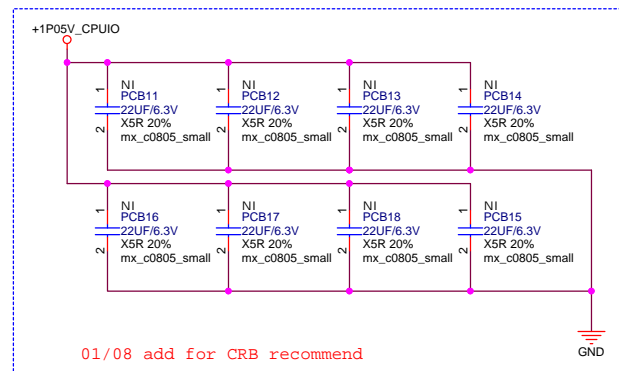


+AC_BAT_SYS
lin=1.026A
Trace Width>70mil

+1P05V_CPUIO
Imax=18.2A
TDC=12.74A
Trace Width>720mil

+0P925V_SA
Imax=8.8A
TDC=6.16A

without VCCIO_SEL trigger,
output = 1.05V



VCCIO Decoupling Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560μF	3	7mΩ	1.4nH	Output	Various. See layout figures	1
22μF 0805 X5R	9	5mΩ	0.55nH	Output	Inside processor socket cavity	1, 2 3
0805 placeholders	16				Backside	

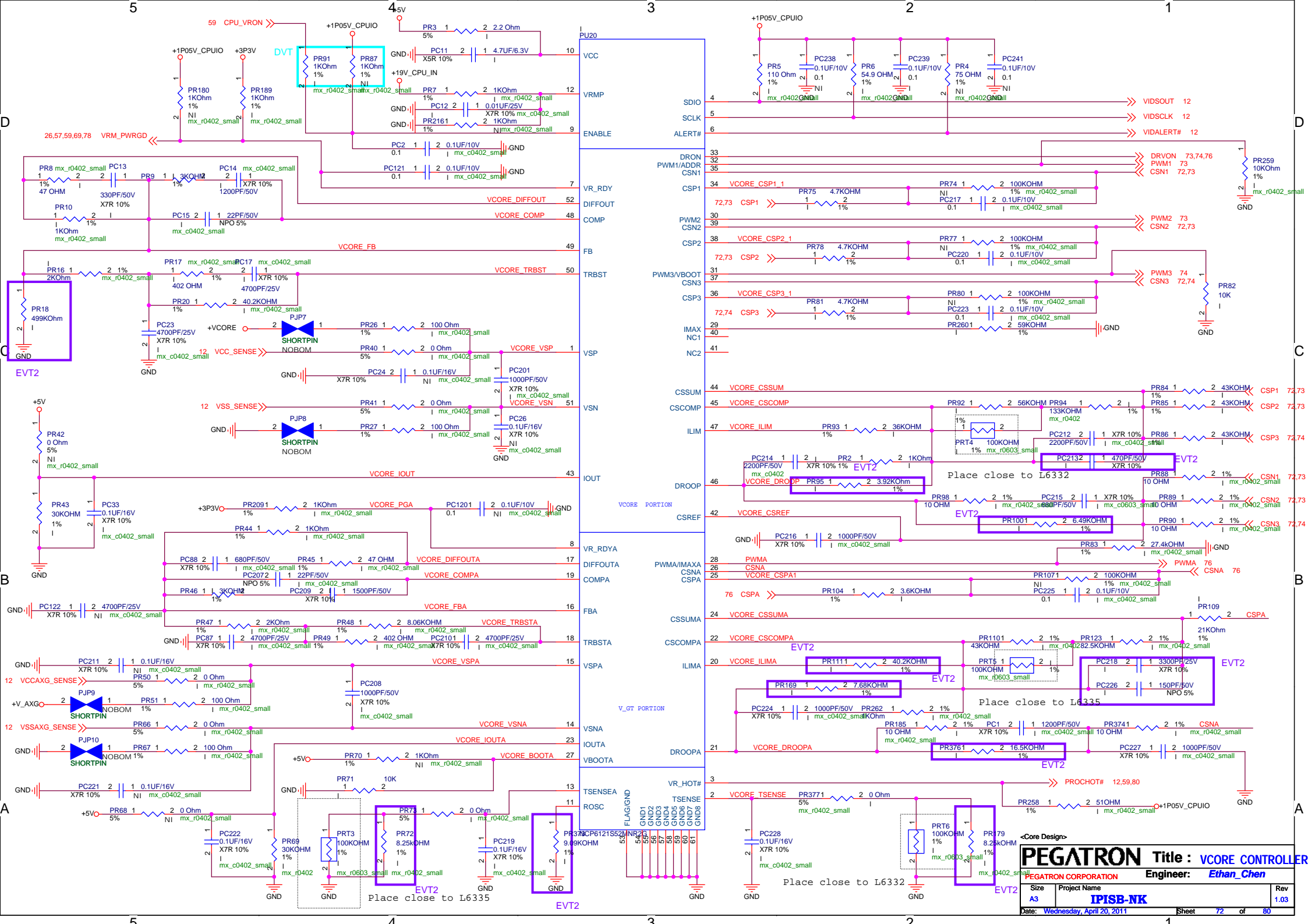
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 1P05V_CPUIO CAP

PEGATRON CORPORATION Engineer: Ethan_Chen

Size A3 Project Name IPISB-NK Rev 1.03

Date: Wednesday, April 20, 2011 Sheet 71 of 80



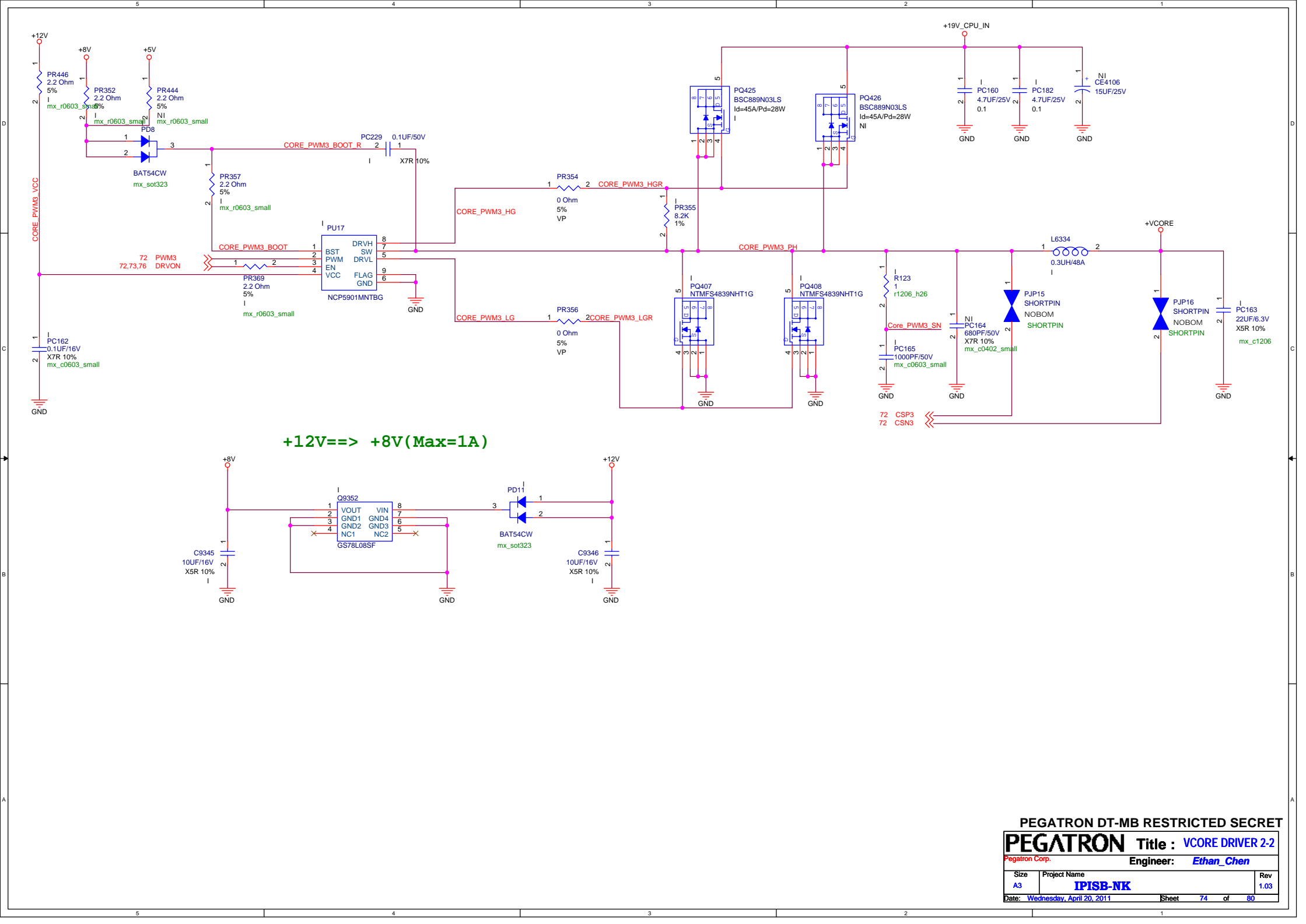
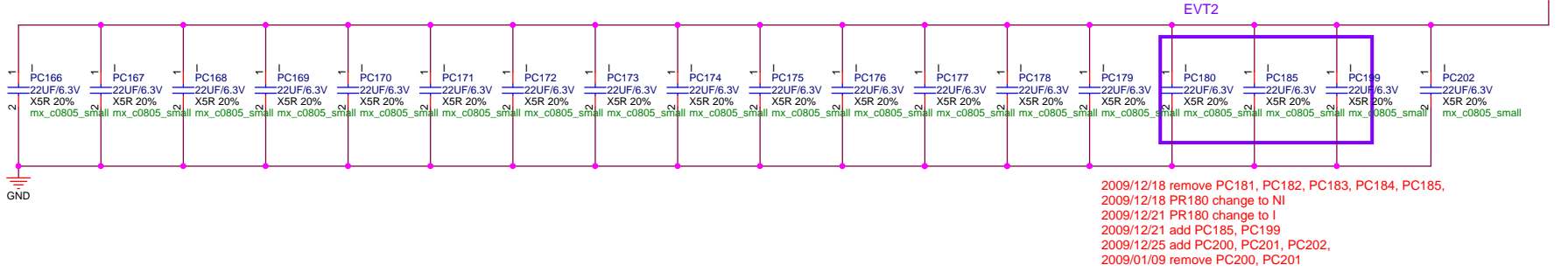
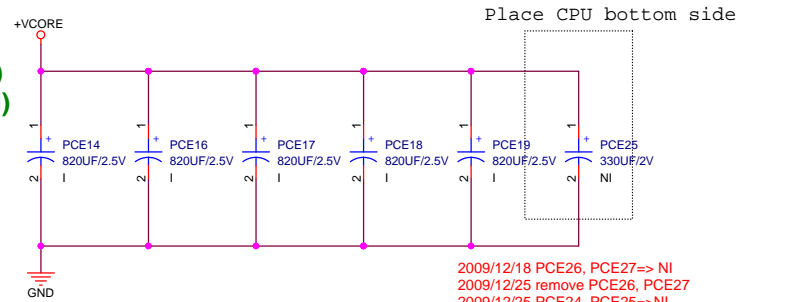
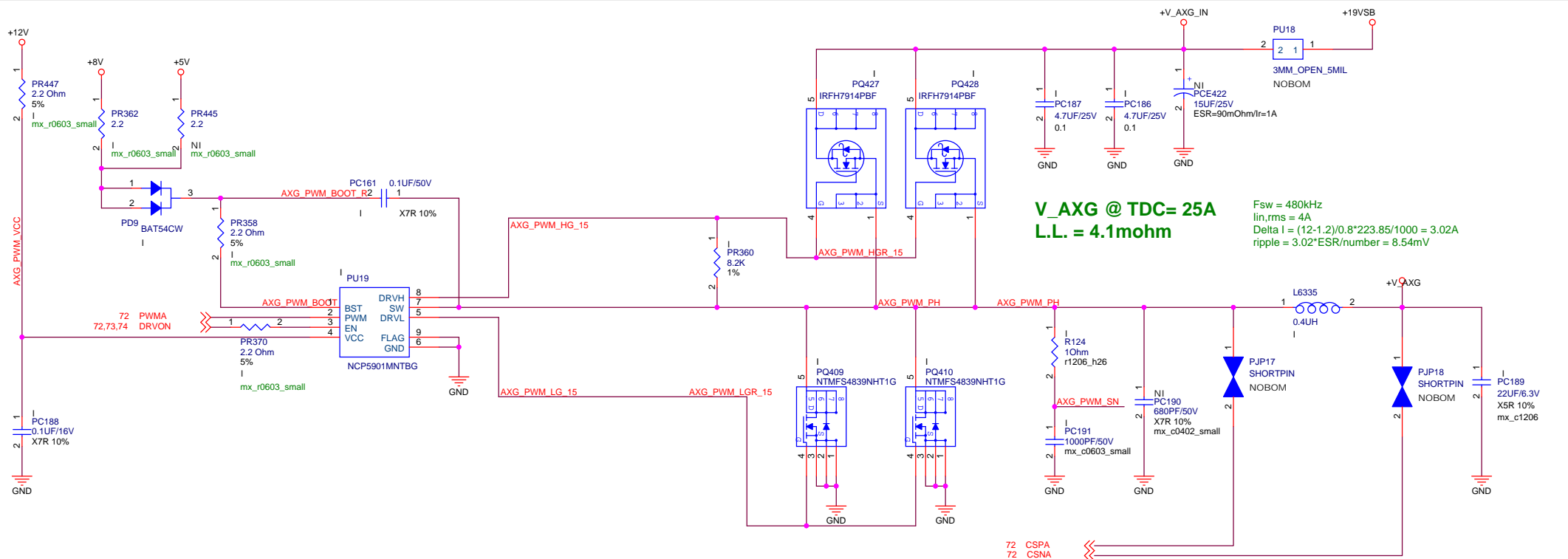


Table 2-2 Processor Requirements

Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560µF	4	7mΩ	1.4nH	Output	North of processor - as close to RM keep-out as possible	1
22µF 0805 X5R	18	5mΩ	0.55nH	Output	14 - Inside processor socket cavity 4- North of processor - as close to RM keep-out as possible	1, 2 3
Aluminum Electrolytic 390µF	4	51mΩ	6.1nH	Input		1
4.7µF X5R	9	7mΩ	0.6nH	Input		1

PL-CAP *4 +2(NI)
MLCC *18 +3(NI)



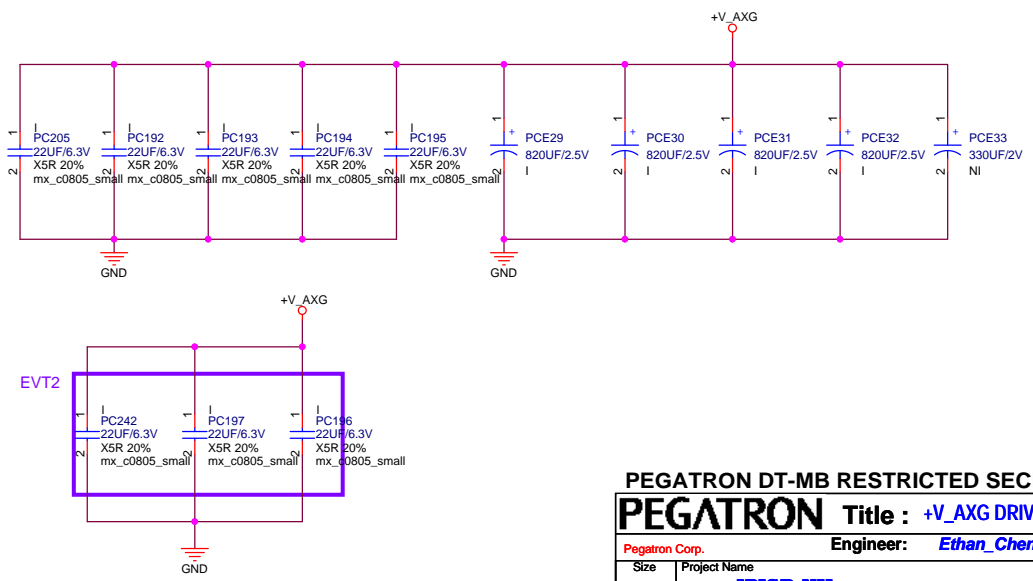


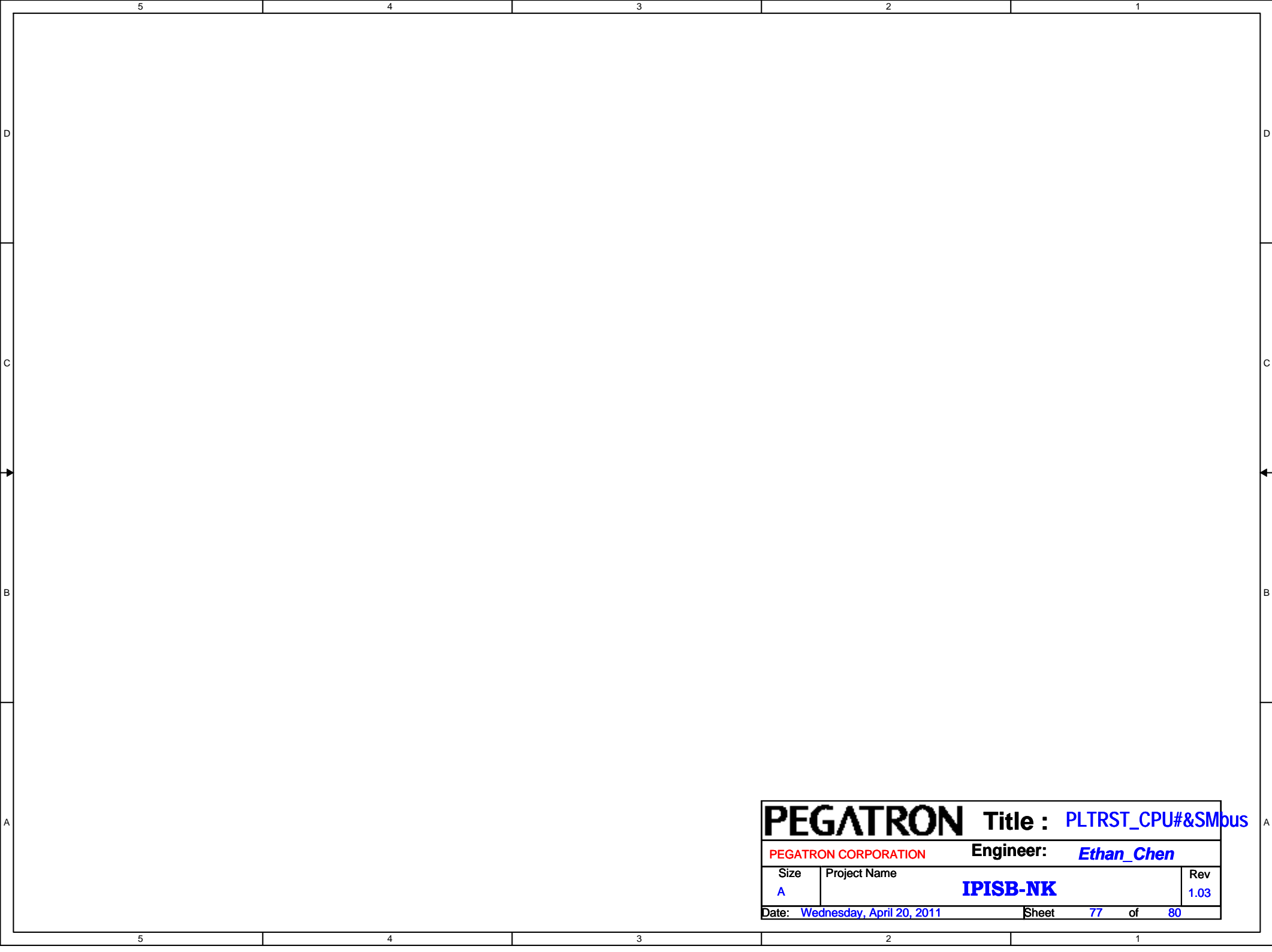
Output CAP

Table 30-4. VCCAXG Decoupling Requirements

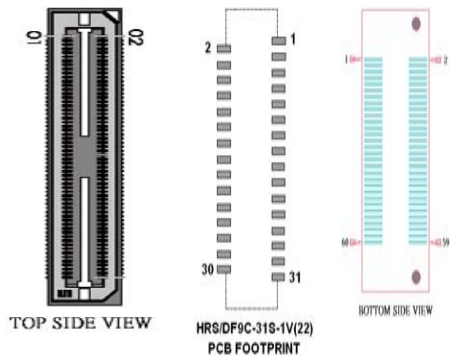
Capacitance	Qty	ESR (each)	ESL (each)	Filter	Placement	Notes
Aluminum Polymer 560μF	4	7mΩ	1.4nH	Output	East of processor - as close to RM keep-out as possible	1
22μF 0805 X5R	6	5mΩ	0.55nH	Output	4 - inside processor socket cavity 2(empty) - Bottom of board, near socket	1, 2, 3
4.7μF X5R	3	7mΩ	0.6nH	Input		1

PL-CAP *4
MLCC *6

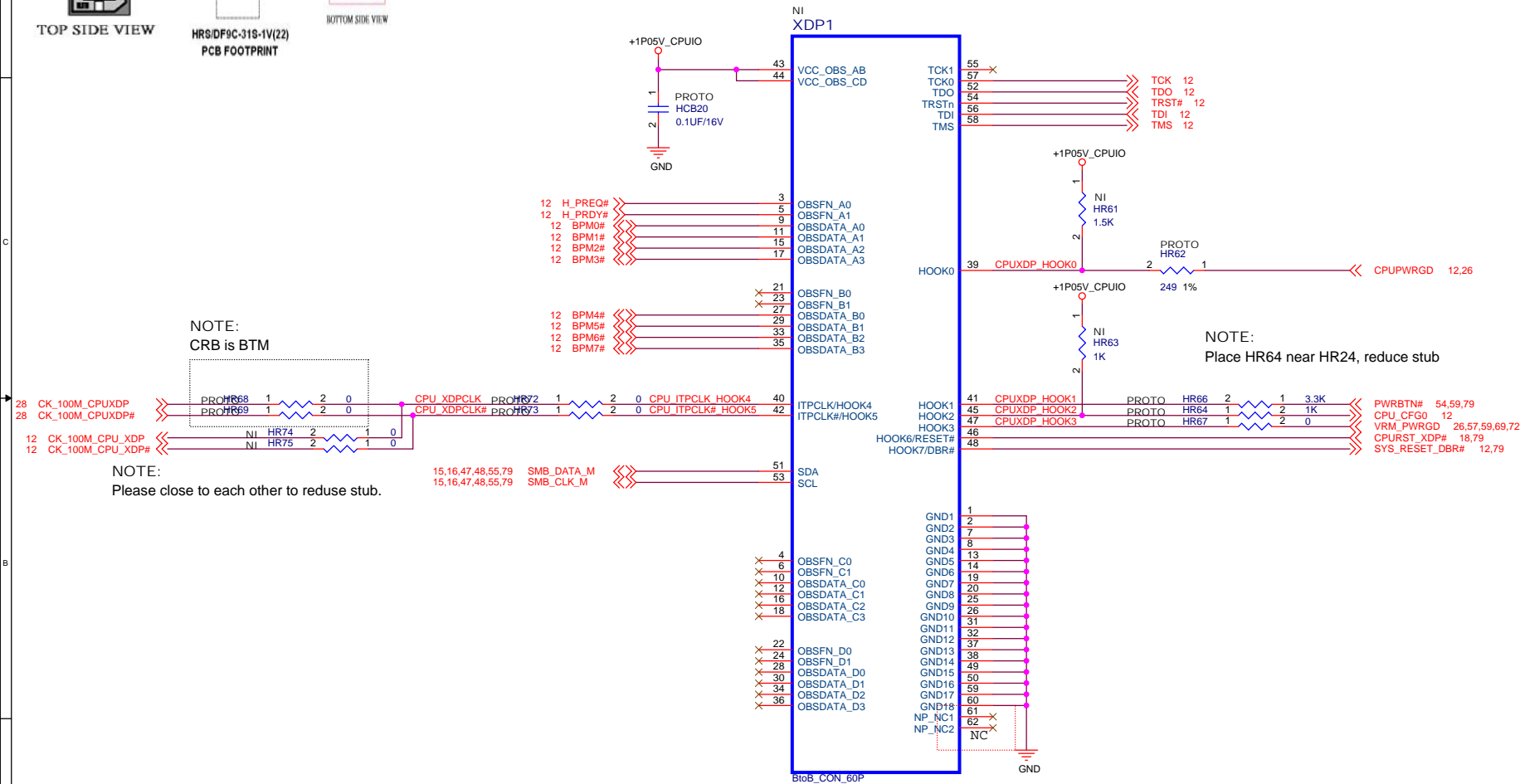




PEGATRON		Title : PLTRST_CPU#&Smbus	
PEGATRON CORPORATION		Engineer: Ethan_Chen	
Size A	Project Name IPISB-NK		Rev 1.03
Date: Wednesday, April 20, 2011		Sheet 77 of 80	



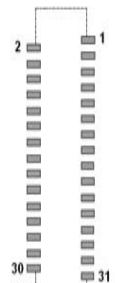
INTEL CPU XDP DEBUG PORT



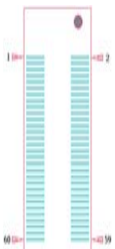
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : CPU XDP DEBUG	
PEGATRON CORPORATION		Engineer: <i>Ethan_Chen</i>	
Size A3	Project Name IPISB-NK	Rev 1.03	
Date: Wednesday, April 20, 2011		Sheet 78 of 80	

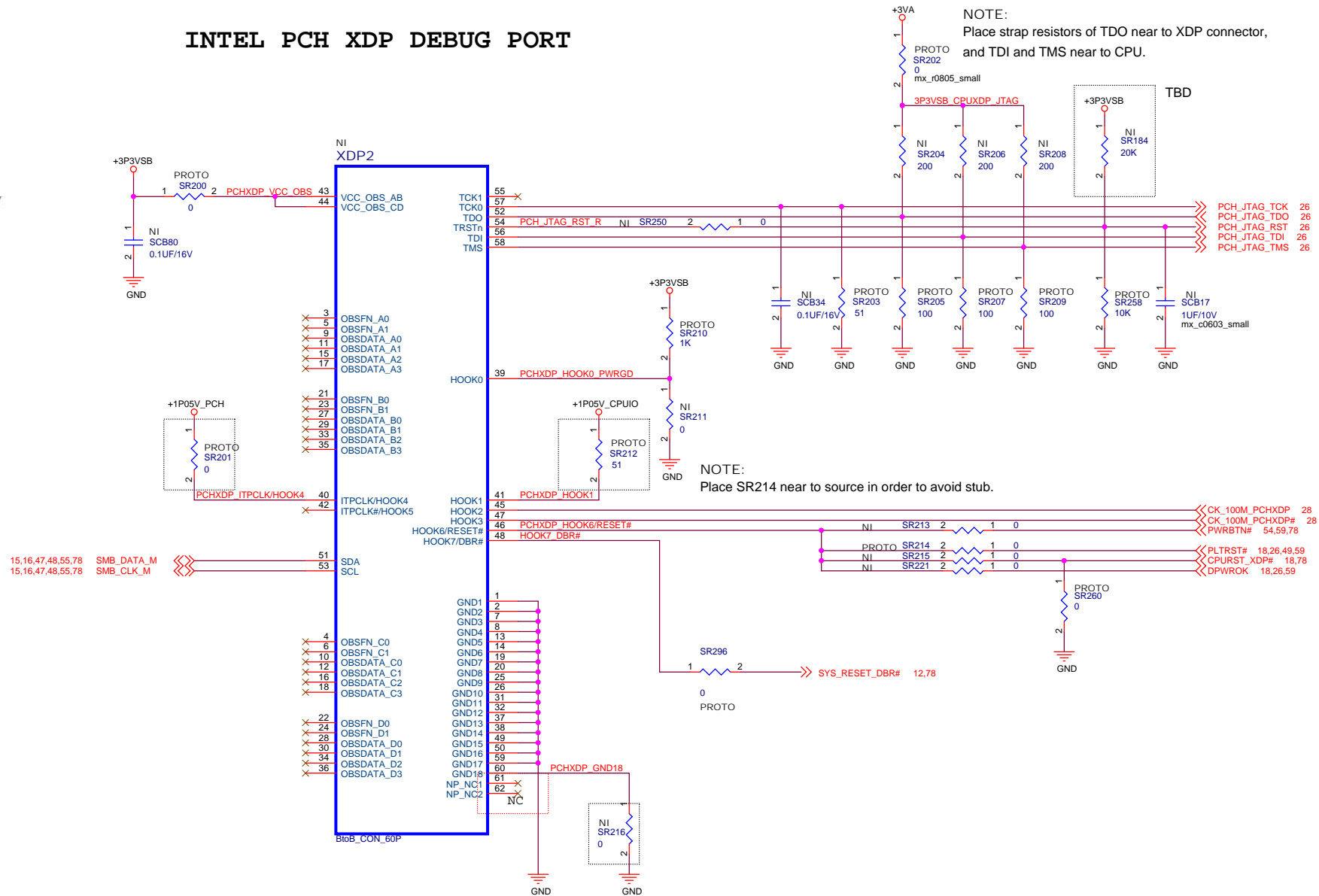
TOP SIDE VIEW



HRS/DF9C-31S-1V(22)
PCB FOOTPRINT



BOTTOM SIDE VIEW



PEGATRON Title : PCH XDP DEBUG

Size A3	Project Name IPISB-NK	Rev 1.03
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