Nirvana 13 UMA Schematics Document

Sandy Bridge
Intel PCH

2011-01-18
REV : A00

DY :None Installed
10mW: External circuit for 10mW solution installed.
BT: Stand alone BT Module.
GSENSOR_ADI: Stuff for ADI G-Sensor.
VCCSA_PWM: Stuff for VCCSA PWM solution.
VCCSA_LDO: Stuff for VCCSA LDO solution.
P2800A1: Stuff for P2800EA1

<Core Design>

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Title: Cover		
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Nirvana 13 UMA Block Diagram (6 layers)

Project Code: 91.4ID01.001
PCB P/N :10261
Revision : -1

PCB LAYER
UMA
L1:Top L2:VCC L3:Signal L4:Signal L5:GND L6:Bottom

CPU DC/DC VT1316+VT1317 42	
INPUTS	OUTPUTS
5V_S5	VCC_CORE

SYSTEM DC/DC VT1316+VT1317 44	
INPUTS	OUTPUTS
5V_S5	VCC_GFXCORE

SYSTEM DC/DC TPS51461/APL5916 48	
INPUTS	OUTPUTS
5V_S5	0D85V_S0

SYSTEM DC/DC TPS51216 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

TI CHARGER BQ24745 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC TPS51427 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC TPS51311 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

Switches 36	
INPUTS	OUTPUTS
1D5V_S3	1D5V_S0
5V_S5	5V_S0
3D3V_S5	3D3V_S0

Intel CPU
Sandy Bridge
4,5,6,7,8,9,10,11,12,13

DDRIII 1066/1333 Channel A → DDRIII Slot 1 1066/1333
DDRIII 1066/1333 Channel B → DDRIII Slot 2 1066/1333

FDIx4x2 / DMIx4

Intel PCH Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25,26

HDMI 51 — HDMI
LCD 49 — LVDS(Single Channel)
CRT 50 — RGB CRT

SD/MMC+/MS/MS Pro/xD/SDXC (8 in 1) 74 — Card Reader RTS5138 32 — USB 2.0 x 1
Bluetooth V3.0 63 — USB 2.0 x 1
Finger Print 64 — USB 2.0 x 1
CAMERA w/ Digital MIC 49 — USB 2.0 x 1
USB2.0 x 4

HDA → CODEC IDT 92HD87B1 29
HP
MIC IN
1CH SPEAKER

SPI → Flash ROM 4MB 60
LPC Bus → KBC NUVOTON NPCE795PA 27 (ADC, DAC)
SMBus → Free Fall Sensor 79

KBC → Touch PAD 69
KBC → Int. KB 69
KBC → Thermal Sensor Main:ENEP2800 28
KBC → FAN Controller Main:ENEP2793 28 → Fan 55

PCIE x 1 → 10/100/1000 LOM Realtek RTL8111E-VB → RJ45 CONN (On Daughter Board)
PCIE x 1 → USB3.0 Controller NEC uPD720200F1 → USB3.0 x 2
PCIE x 1,USB2.0 x 1 → Mini-Card WWAN → SIM
PCIE x 1,USB2.0 x 1 → Mini-Card 802.11a/b/g 65
USB2.0 x 1 → USB CHARGE PI5USB14550 57 → ESATA/USB Combo 57
SATA x 1
SATA x 2 → HDD 56
SATA x 2 → ODD 56

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Block Diagram		
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PCH Strapping

Huron River Schematic Checklist Rev.1_0

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Enable when Pull-up.
INIT3_3V#	Weak internal pull-up. This signal should not be pulled low. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3 power rail.
INTVRMEN	**Integrated 1.05 V VRM Enable / Disable** Integrated 1.05 V VRMs is enabled when high. This signal should always be pulled high
DF_TVS	**DMI and FDI Tx/Rx Termination Voltage** Weak internal pull-down. It needs to be connected to PROC_SELECT with a 1K±5% pull-up resistor to PCH VCCPNAND rail and a 4.7K±5% series resistor.
SATA1GP /GPIO19	**Boot BIOS Strap bit 0** This Signal has a weak internal pull-up. Note: This field determines the destination of accesses to the BIOS memory range. This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 PCI 1 1 SPI 0 0 LPC
HDA_SDO	Signal has a weak internal pull-down. Default: the security measures defined in the Flash Descriptor will be in effect. Pull-up: the Flash Descriptor Security will be overridden. This strap should only be asserted high via external pull-up in manufacturing or debug environments ONLY.
HDA_SYNC	**On-Die PLL Voltage Regulator Voltage Select** This signal has a weak internal pull-down. On Die PLL VR is supplied by 1.5 V when sampled high, 1.8 V when sampled low. Needs to be pulled High for Huron River platform.
GPIO15	**TLS Confidentiality** Low - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality This signal has a weak internal pull-down. NOTE: A strong pull-up may be needed for GPIO functionality
DSWVRMEN	**Deep S4/S5 Well On-Die Voltage Regulator Enable** This signal enables the internal Deep Sleep 1.05 V regulators. This signal must be always pulled-up to VccRTC.
GPIO28	**On-Die PLL Voltage Regulator** This signal has a weak internal pull-up. The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled. If not used, 8.2-kΩ to 10-kΩ pull-up to +V3.3A power-rail.

Processor Strapping

Huron River Schematic Checklist Rev.1_0

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	0
CFG[4]	**Display Port Presence strap**	**1:** Disabled - No Physical Display Port attached to Embedded Display Port. **0:** Enabled - An external Display Port device is connectd to the Embedded Display Port	1
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE	5V 3.3V 1.8V 1.5V 1.05V 0.95 ~ 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V~14.1V 6V~14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	X
LANE2	LAN (I/O Board)
LANE3	Mini Card2(WWAN)
LANE4	Mini Card1(WLAN)
LANE5	USB3.0
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	X
1	ESATA / USB COMBO
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	X
9	X
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address Hex Bus
EC SMBus 1 Battery Capacity Board		KBC_SDA1/KBC_SCL1 KBC_SDA1/KBC_SCL1
EC SMBus 2 PCH MXM LCD Thermal Sensor		KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2 KBC_SDA2/KBC_SCL2
PCH SMBus CK505 Clock Generator SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

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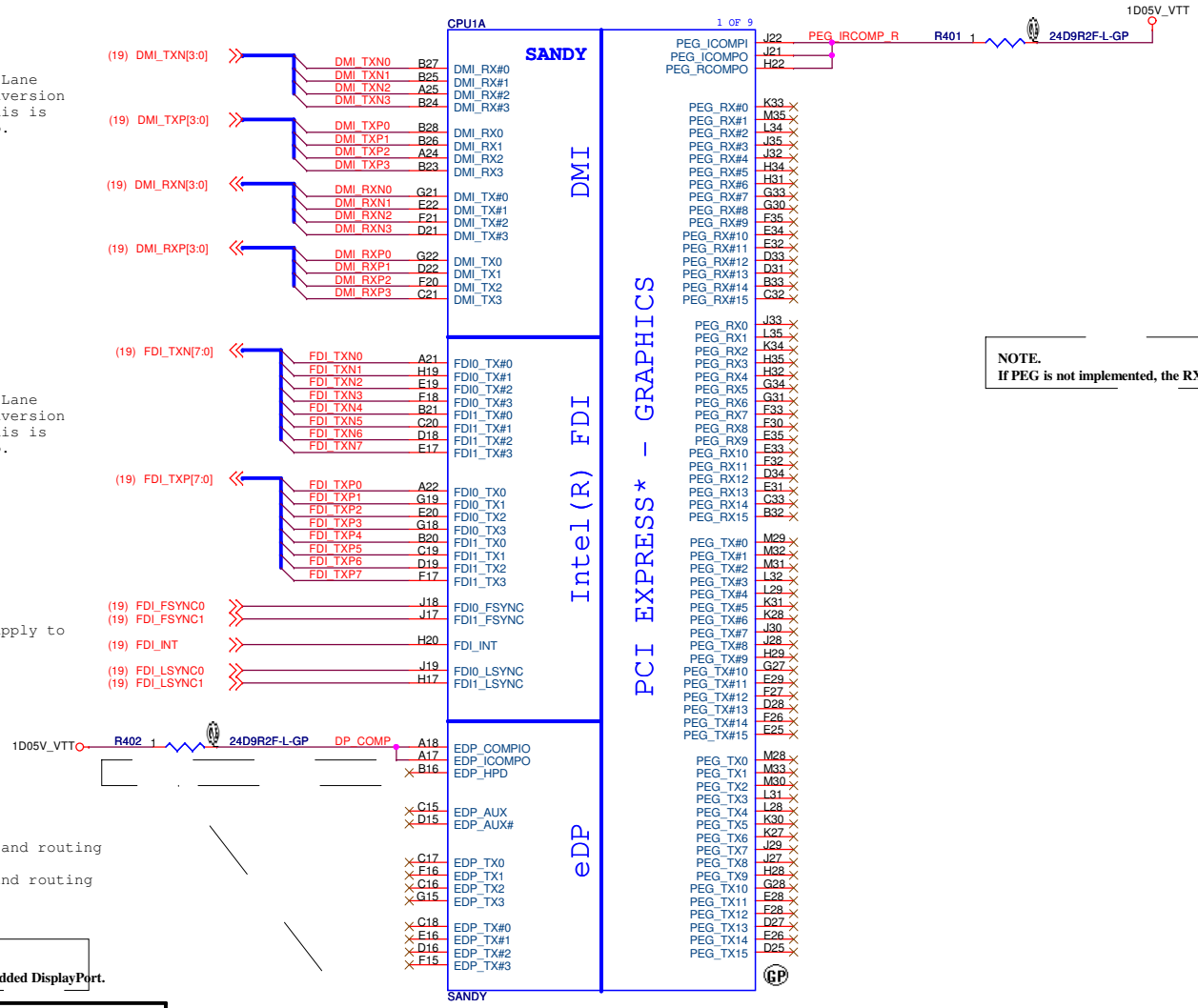
SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.



NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

<Core Design>

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Title: CPU 1/7(PEG/DMI/FDI/eDP)

Size	Document Number	Rev
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SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

CPU1B — SANDY — 2 OF 9

SNB_IVB# C26 (18) H_SNB_IVB#
SKTOCC# AN34 TPAD14-GP TP501 SKTOCC# R
CATERR# AL33 TPAD14-GP TP502 H_CATERR#
PECI AN33 (22,27) H_PECI
PROCHOT# AL32 (27,40,42) H_PROCHOT# R513 56R2J-4-GP H_PROCHOT# R
THERMTRIP# AN32 (22,36) H_THERMTRIP#

MISC / THERMAL

BCLK A28 BCLK# A27 — CLK_EXP_P (20) CLK_EXP_N (20)
DPLL_REF_SSCLK A16 DPLL_REF_SSCLK# A15 — CLK_DP_P_R CLK_DP_N_R — RN502 SRN1KJ-7-GP — 1D05V_VTT

CLOCKS

20110104 A00:
merge R512,R514 to RN502 1k array resistor.
20110113 A00:
Swap RN502 base on swap report.

SM_DRAMRST# R8 — R502 4K99R2F-L-GP — SM_DRAMRST# (37)
SM_RCOMP0 AK1 SM_RCOMP_0 R506 140R2F-GP
SM_RCOMP1 A5 SM_RCOMP_1 R507 25D5R2F-GP
SM_RCOMP2 A4 SM_RCOMP_2 R508 200R2F-L-GP

DDR3 MISC

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

1D05V_VTT — R501 62R2J-GP — H_PROCHOT#
C502 SC47P50V2JN-3GP
20100622 V1.2
CRB : 47pf
CEKLT:43pf
Connect EC to PROCHOT# through inverting OD buffer.

R503 10KR2J-3-GP — H_CPUPWRGD_R

PRDY# AP29 PREQ# AP27
TCK AR26 XDP_TCLK
TMS AR27 XDP_TMS
TRST# AP30 XDP_TRST#
TDI AR28 XDP_TDI
TDO AP26 XDP_TDO
DBR# AL35 XDP_DBRESET#
BPM#0 AT28
BPM#1 AR29
BPM#2 AR30
BPM#3 AT30
BPM#4 AP32
BPM#5 AR31
BPM#6 AT31
BPM#7 AR32

JTAG & BPM

PM_SYNC AM34 (19) H_PM_SYNC
UNCOREPWRGOOD AP33 (22,36) H_CPUPWRGD — R504 0R0402-PAD — H_CPUPWRGD_R
SM_DRAMPWROK V8 (19,37) PM_DRAM_PWRGD — R505 0R2J-2-GP — VDDPWRGOOD
(37) VDDPWRGOOD
RESET# AR33 (18,27,65,71,82) PLT_RST# — R510 1K5R2F-2-GP — BUF_CPU_RST#
R509 750R2F-GP
DY C501 SC220P50V2KX-3GP

PWR MANAGEMENT

SANDY

1D05V_VTT — RN501 SRN51J-1-GP — XDP_TDI XDP_TMS XDP_TDO XDP_TCLK
XDP_TRST# — R511 51R2J-2-GP

3D3V_S0 — XDP_DBRESET# — R516 10KR2J-3-GP
20100722 Modify:
Change R516 10K from 1K

XDP_DBRESET# >>> XDP_DBRESET# (19)

Buffered reset to CPU

1D05V_VTT — DY R518 75R2J-1-GP
3D3V_S0 — DY C503 SCD1U10V2KX-5GP
U501 74VHC1G09DFT2G-GP 73.01G09.AAH
(18,27,65,71,82) PLT_RST# — IN B, IN A, GND, VCC, OUT Y — BUFO_CPU_RST# — R517 43R2J-GP — BUF_CPU_RST#
DY R515 0R2J-2-GP

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Title: CPU 2/7(THERMAL/CLOCK/PM)
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SSID = CPU

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SANDY

DDR SYSTEM MEMORY A

(14) M_A_DQ[63:0]

M_A_DQ0	C5	SA_DQ0
M_A_DQ1	D5	SA_DQ1
M_A_DQ2	D3	SA_DQ2
M_A_DQ3	D2	SA_DQ3
M_A_DQ4	D6	SA_DQ4
M_A_DQ5	C6	SA_DQ5
M_A_DQ6	C2	SA_DQ6
M_A_DQ7	C3	SA_DQ7
M_A_DQ8	F10	SA_DQ8
M_A_DQ9	F8	SA_DQ9
M_A_DQ10	G10	SA_DQ10
M_A_DQ11	G9	SA_DQ11
M_A_DQ12	F9	SA_DQ12
M_A_DQ13	F7	SA_DQ13
M_A_DQ14	G8	SA_DQ14
M_A_DQ15	G7	SA_DQ15
M_A_DQ16	K4	SA_DQ16
M_A_DQ17	K5	SA_DQ17
M_A_DQ18	K1	SA_DQ18
M_A_DQ19	J1	SA_DQ19
M_A_DQ20	J5	SA_DQ20
M_A_DQ21	J4	SA_DQ21
M_A_DQ22	J2	SA_DQ22
M_A_DQ23	K2	SA_DQ23
M_A_DQ24	M8	SA_DQ24
M_A_DQ25	N10	SA_DQ25
M_A_DQ26	N8	SA_DQ26
M_A_DQ27	N7	SA_DQ27
M_A_DQ28	M10	SA_DQ28
M_A_DQ29	M9	SA_DQ29
M_A_DQ30	N9	SA_DQ30
M_A_DQ31	M7	SA_DQ31
M_A_DQ32	AG6	SA_DQ32
M_A_DQ33	AG5	SA_DQ33
M_A_DQ34	AK6	SA_DQ34
M_A_DQ35	AK5	SA_DQ35
M_A_DQ36	AH5	SA_DQ36
M_A_DQ37	AH6	SA_DQ37
M_A_DQ38	AJ5	SA_DQ38
M_A_DQ39	AJ6	SA_DQ39
M_A_DQ40	AJ8	SA_DQ40
M_A_DQ41	AK8	SA_DQ41
M_A_DQ42	AJ9	SA_DQ42
M_A_DQ43	AK9	SA_DQ43
M_A_DQ44	AH8	SA_DQ44
M_A_DQ45	AH9	SA_DQ45
M_A_DQ46	AL9	SA_DQ46
M_A_DQ47	AL8	SA_DQ47
M_A_DQ48	AP11	SA_DQ48
M_A_DQ49	AN11	SA_DQ49
M_A_DQ50	AL12	SA_DQ50
M_A_DQ51	AM12	SA_DQ51
M_A_DQ52	AM11	SA_DQ52
M_A_DQ53	AL11	SA_DQ53
M_A_DQ54	AP12	SA_DQ54
M_A_DQ55	AN12	SA_DQ55
M_A_DQ56	AJ14	SA_DQ56
M_A_DQ57	AH14	SA_DQ57
M_A_DQ58	AL15	SA_DQ58
M_A_DQ59	AK15	SA_DQ59
M_A_DQ60	AL14	SA_DQ60
M_A_DQ61	AK14	SA_DQ61
M_A_DQ62	AJ15	SA_DQ62
M_A_DQ63	AH15	SA_DQ63

(14) M_A_BS0	AE10	SA_BS0
(14) M_A_BS1	AF10	SA_BS1
(14) M_A_BS2	V6	SA_BS2
(14) M_A_CAS#	AE8	SA_CAS#
(14) M_A_RAS#	AD9	SA_RAS#
(14) M_A_WE#	AF9	SA_WE#

SA_CLK0	AB6	M_A_DIM0_CLK_DDR0 (14)
SA_CLK#0	AA6	M_A_DIM0_CLK_DDR#0 (14)
SA_CKE0	V9	M_A_DIM0_CKE0 (14)
SA_CLK1	AA5	M_A_DIM0_CLK_DDR1 (14)
SA_CLK#1	AB5	M_A_DIM0_CLK_DDR#1 (14)
SA_CKE1	V10	M_A_DIM0_CKE1 (14)
SA_CLK2	AB4	
SA_CLK#2	AA4	
SA_CKE2	W9	
SA_CLK3	AB3	
SA_CLK#3	AA3	
SA_CKE3	W10	
SA_CS#0	AK3	M_A_DIM0_CS#0 (14)
SA_CS#1	AL3	M_A_DIM0_CS#1 (14)
SA_CS#2	AG1	
SA_CS#3	AH1	
SA_ODT0	AH3	M_A_DIM0_ODT0 (14)
SA_ODT1	AG3	M_A_DIM0_ODT1 (14)
SA_ODT2	AG2	
SA_ODT3	AH2	

SA_DQS#0	C4	M_A_DQS#0	M_A_DQS#[7:0] (14)
SA_DQS#1	G6	M_A_DQS#1	
SA_DQS#2	J3	M_A_DQS#2	
SA_DQS#3	M6	M_A_DQS#3	
SA_DQS#4	AL6	M_A_DQS#4	
SA_DQS#5	AM8	M_A_DQS#5	
SA_DQS#6	AR12	M_A_DQS#6	
SA_DQS#7	AM15	M_A_DQS#7	
SA_DQS0	D4	M_A_DQS0	M_A_DQS[7:0] (14)
SA_DQS1	F6	M_A_DQS1	
SA_DQS2	K3	M_A_DQS2	
SA_DQS3	N6	M_A_DQS3	
SA_DQS4	AL5	M_A_DQS4	
SA_DQS5	AM9	M_A_DQS5	
SA_DQS6	AR11	M_A_DQS6	
SA_DQS7	AM14	M_A_DQS7	

SA_MA0	AD10	M_A_A0	M_A_A[15:0] (14)
SA_MA1	W1	M_A_A1	
SA_MA2	W2	M_A_A2	
SA_MA3	W7	M_A_A3	
SA_MA4	V3	M_A_A4	
SA_MA5	V2	M_A_A5	
SA_MA6	W3	M_A_A6	
SA_MA7	W6	M_A_A7	
SA_MA8	V1	M_A_A8	
SA_MA9	W5	M_A_A9	
SA_MA10	AD8	M_A_A10	
SA_MA11	V4	M_A_A11	
SA_MA12	W4	M_A_A12	
SA_MA13	AF8	M_A_A13	
SA_MA14	V5	M_A_A14	
SA_MA15	V7	M_A_A15	

(15) M_B_DQ[63:0]

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SANDY

DDR SYSTEM MEMORY B

M_B_DQ0	C9	SB_DQ0
M_B_DQ1	A7	SB_DQ1
M_B_DQ2	D10	SB_DQ2
M_B_DQ3	C8	SB_DQ3
M_B_DQ4	A9	SB_DQ4
M_B_DQ5	A8	SB_DQ5
M_B_DQ6	D9	SB_DQ6
M_B_DQ7	D8	SB_DQ7
M_B_DQ8	G4	SB_DQ8
M_B_DQ9	F4	SB_DQ9
M_B_DQ10	F1	SB_DQ10
M_B_DQ11	G1	SB_DQ11
M_B_DQ12	G5	SB_DQ12
M_B_DQ13	F5	SB_DQ13
M_B_DQ14	F2	SB_DQ14
M_B_DQ15	G2	SB_DQ15
M_B_DQ16	J7	SB_DQ16
M_B_DQ17	J8	SB_DQ17
M_B_DQ18	K10	SB_DQ18
M_B_DQ19	K9	SB_DQ19
M_B_DQ20	J9	SB_DQ20
M_B_DQ21	J10	SB_DQ21
M_B_DQ22	K8	SB_DQ22
M_B_DQ23	K7	SB_DQ23
M_B_DQ24	M5	SB_DQ24
M_B_DQ25	N4	SB_DQ25
M_B_DQ26	N2	SB_DQ26
M_B_DQ27	N1	SB_DQ27
M_B_DQ28	M4	SB_DQ28
M_B_DQ29	N5	SB_DQ29
M_B_DQ30	M2	SB_DQ30
M_B_DQ31	M1	SB_DQ31
M_B_DQ32	AM5	SB_DQ32
M_B_DQ33	AM6	SB_DQ33
M_B_DQ34	AR3	SB_DQ34
M_B_DQ35	AP3	SB_DQ35
M_B_DQ36	AN3	SB_DQ36
M_B_DQ37	AN2	SB_DQ37
M_B_DQ38	AN1	SB_DQ38
M_B_DQ39	AP2	SB_DQ39
M_B_DQ40	AP5	SB_DQ40
M_B_DQ41	AN9	SB_DQ41
M_B_DQ42	AT5	SB_DQ42
M_B_DQ43	AT6	SB_DQ43
M_B_DQ44	AP6	SB_DQ44
M_B_DQ45	AN8	SB_DQ45
M_B_DQ46	AR6	SB_DQ46
M_B_DQ47	AR5	SB_DQ47
M_B_DQ48	AR9	SB_DQ48
M_B_DQ49	AJ11	SB_DQ49
M_B_DQ50	AT8	SB_DQ50
M_B_DQ51	AT9	SB_DQ51
M_B_DQ52	AH11	SB_DQ52
M_B_DQ53	AR8	SB_DQ53
M_B_DQ54	AJ12	SB_DQ54
M_B_DQ55	AH12	SB_DQ55
M_B_DQ56	AT11	SB_DQ56
M_B_DQ57	AN14	SB_DQ57
M_B_DQ58	AR14	SB_DQ58
M_B_DQ59	AT14	SB_DQ59
M_B_DQ60	AT12	SB_DQ60
M_B_DQ61	AN15	SB_DQ61
M_B_DQ62	AR15	SB_DQ62
M_B_DQ63	AT15	SB_DQ63

(15) M_B_BS0	AA9	SB_BS0
(15) M_B_BS1	AA7	SB_BS1
(15) M_B_BS2	R6	SB_BS2
(15) M_B_CAS#	AA10	SB_CAS#
(15) M_B_RAS#	AB8	SB_RAS#
(15) M_B_WE#	AB9	SB_WE#

SB_CLK0	AE2	M_B_DIM0_CLK_DDR0 (15)
SB_CLK#0	AD2	M_B_DIM0_CLK_DDR#0 (15)
SB_CKE0	R9	M_B_DIM0_CKE0 (15)
SB_CLK1	AE1	M_B_DIM0_CLK_DDR1 (15)
SB_CLK#1	AD1	M_B_DIM0_CLK_DDR#1 (15)
SB_CKE1	R10	M_B_DIM0_CKE1 (15)
SB_CLK2	AB2	
SB_CLK#2	AA2	
SB_CKE2	T9	
SB_CLK3	AA1	
SB_CLK#3	AB1	
SB_CKE3	T10	
SB_CS#0	AD3	M_B_DIM0_CS#0 (15)
SB_CS#1	AE3	M_B_DIM0_CS#1 (15)
SB_CS#2	AD6	
SB_CS#3	AE6	
SB_ODT0	AE4	M_B_DIM0_ODT0 (15)
SB_ODT1	AD4	M_B_DIM0_ODT1 (15)
SB_ODT2	AD5	
SB_ODT3	AE5	

SB_DQS#0	D7	M_B_DQS#0	M_B_DQS#[7:0] (15)
SB_DQS#1	F3	M_B_DQS#1	
SB_DQS#2	K6	M_B_DQS#2	
SB_DQS#3	N3	M_B_DQS#3	
SB_DQS#4	AN5	M_B_DQS#4	
SB_DQS#5	AP9	M_B_DQS#5	
SB_DQS#6	AK12	M_B_DQS#6	
SB_DQS#7	AP15	M_B_DQS#7	
SB_DQS0	C7	M_B_DQS0	M_B_DQS[7:0] (15)
SB_DQS1	G3	M_B_DQS1	
SB_DQS2	J6	M_B_DQS2	
SB_DQS3	M3	M_B_DQS3	
SB_DQS4	AN6	M_B_DQS4	
SB_DQS5	AP8	M_B_DQS5	
SB_DQS6	AK11	M_B_DQS6	
SB_DQS7	AP14	M_B_DQS7	

SB_MA0	AA8	M_B_A0	M_B_A[15:0] (15)
SB_MA1	T7	M_B_A1	
SB_MA2	R7	M_B_A2	
SB_MA3	T6	M_B_A3	
SB_MA4	T2	M_B_A4	
SB_MA5	T4	M_B_A5	
SB_MA6	T3	M_B_A6	
SB_MA7	R2	M_B_A7	
SB_MA8	T5	M_B_A8	
SB_MA9	R3	M_B_A9	
SB_MA10	AB7	M_B_A10	
SB_MA11	R1	M_B_A11	
SB_MA12	T1	M_B_A12	
SB_MA13	AB10	M_B_A13	
SB_MA14	R5	M_B_A14	
SB_MA15	R4	M_B_A15	

<Core Design>

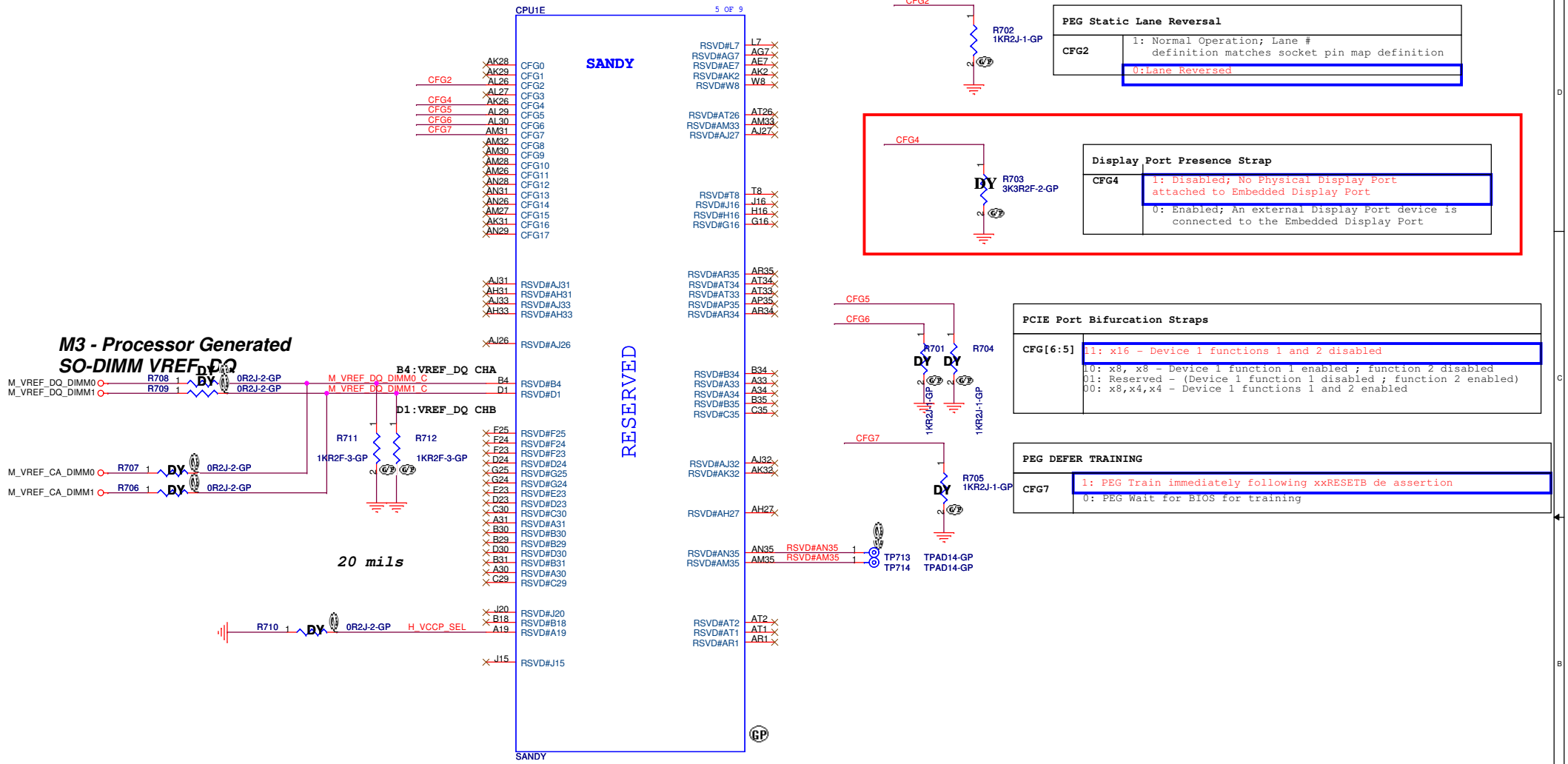
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU 3/7(DDR)

Size | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 18, 2011 | Sheet 6 of 103

SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port
	0: Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	11: x16 – Device 1 functions 1 and 2 disabled
	10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled
	01: Reserved – (Device 1 function 1 disabled ; function 2 enabled)
	00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: PEG Train immediately following xxRESETB de assertion
	0: PEG Wait for BIOS for training

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

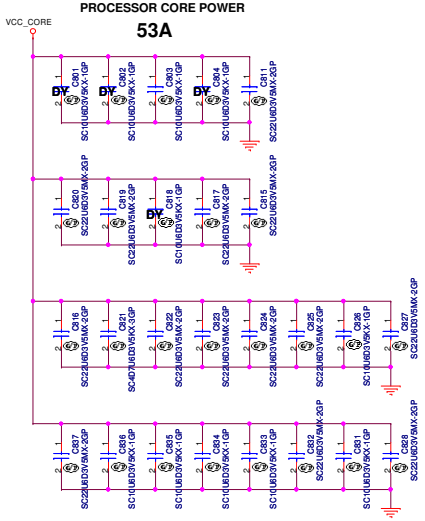
Title: CPU 4/7(RESERVED)

Size | Document Number: Nirvana 13 | Rev: A00

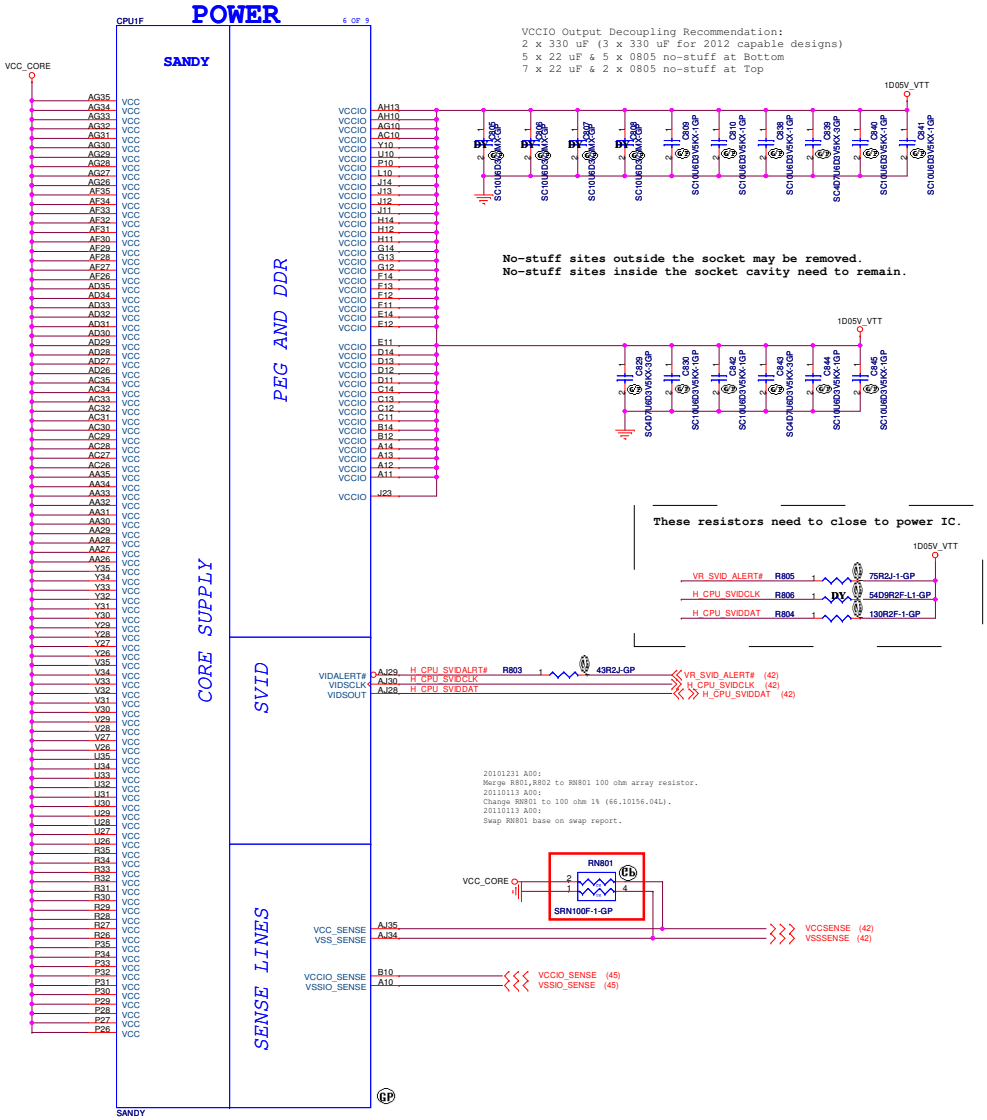
Date: Wednesday, December 22, 2010 | Sheet 7 of 103

SSID = CPU

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity



VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

These resistors need to close to power IC.

20101231 A00:
Merge R801,R802 to RN801 100 ohm array resistor.
20110113 A00:
Change RN801 to 100 ohm 1% (66.10156.04L).
20110113 A00:
Swap RN801 base on swap report.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU 5/7(VCC_CORE)
Size: Document Number: Nirvana 13 Rev: A00
Date: Tuesday, January 18, 2011 Sheet 8 of 103

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

20101231 A00:
Merge R906,R907 to RN902 100 ohm array resistor.
20110113 A00:
Change RN801 to 100 ohm 1% (66.10156.04L).
20110113 A00:
Swap RN902 base on swap report.

POWER

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

VCC_GFXCORE

PROCESSOR VAXG: 33A

C901 SC10U6D3V5KX-1GP (DY)
C902 SC4D7U6D3V5KX-3GP
C903 SC4D7U6D3V5KX-3GP
C904 SC4D7U6D3V5KX-3GP
C905 SC22U6D3V5MX-2GP
C906 SC4D7U6D3V5KX-3GP
C908 SC10U6D3V3MX-GP (DY)
C920 SC10U6D3V3MX-GP (DY)
C921 SC10U6D3V3MX-GP (DY)

CPU1G — SANDY — 7 OF 9

VAXG: AT24, AT23, AT21, AT20, AT18, AT17, AR24, AR23, AR21, AR20, AR18, AR17, AP24, AP23, AP21, AP20, AP18, AP17, AN24, AN23, AN21, AN20, AN18, AN17, AM24, AM23, AM21, AM20, AM18, AM17, AL24, AL23, AL21, AL20, AL18, AL17, AK24, AK23, AK21, AK20, AK18, AK17, AJ24, AJ23, AJ21, AJ20, AJ18, AJ17, AH24, AH23, AH21, AH20, AH18, AH17

GRAPHICS

SENSE LINES
VAXG_SENSE — AK35 — VCC_AXG_SENSE (42)
VSSAXG_SENSE — AK34 — VSS_AXG_SENSE (42)

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF
SM_VREF — AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT (37)

RN902 (CB)
VCC_AXG_SENSE — 2
VSS_AXG_SENSE — 1
4 — VCC_GFXCORE
SRN100F-1-GP

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

PROCESSOR VDDQ: 10A

1D5V_S0
VDDQ: AF7, AF4, AF1, AC7, AC4, AC1, Y7, Y4, Y1, U7, U4, U1, P7, P4, P1
C909 SC10U6D3V3MX-GP (DY)
C910 SC10U6D3V3MX-GP (DY)
C911 SC10U6D3V3MX-GP (DY)
C912 SC10U6D3V5KX-1GP
C913 SC4D7U6D3V5KX-3GP
C914 SC10U6D3V5KX-1GP
TC901 ST330U2VDM4-GP
C907 SCD1U10V2KX-5GP (DY)
C918 SCD1U10V2KX-5GP (DY)
C919 SCD1U10V2KX-5GP (DY)
C925 SCD1U10V2KX-5GP (DY)
1D5V_S3

79.33719.20L
2nd = 77.C3371.13L

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

0D85V_S0

PROCESSOR VCCSA: 6A

C916 SC10U6D3V5KX-1GP
C915 SC10U6D3V5KX-1GP
C917 SC10U6D3V5KX-1GP

SA RAIL

VCCSA: M27, M26, L26, J26, J25, J24, H26, H25

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

Removed DIS_ONLY Disable Resistor.
R904,R905,R901,R903

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C923 SC10U6D3V5KX-1GP
C922 SC1U10V2KX-1GP
C924 SC1U10V2KX-1GP

1.8V RAIL

VCCPLL: B6, A6, A2

MISC

VCCSA_SENSE — H23 — VCCUSA_SENSE — VCCUSA_SENSE (48)

FC_C22 / VCCSA_VID1 — C22, C24 — H_FC_C22 / VCCSA_SEL — H_FC_C22 (48) / VCCSA_SEL (48)

RN901
SRN1KJ-7-GP

SANDY

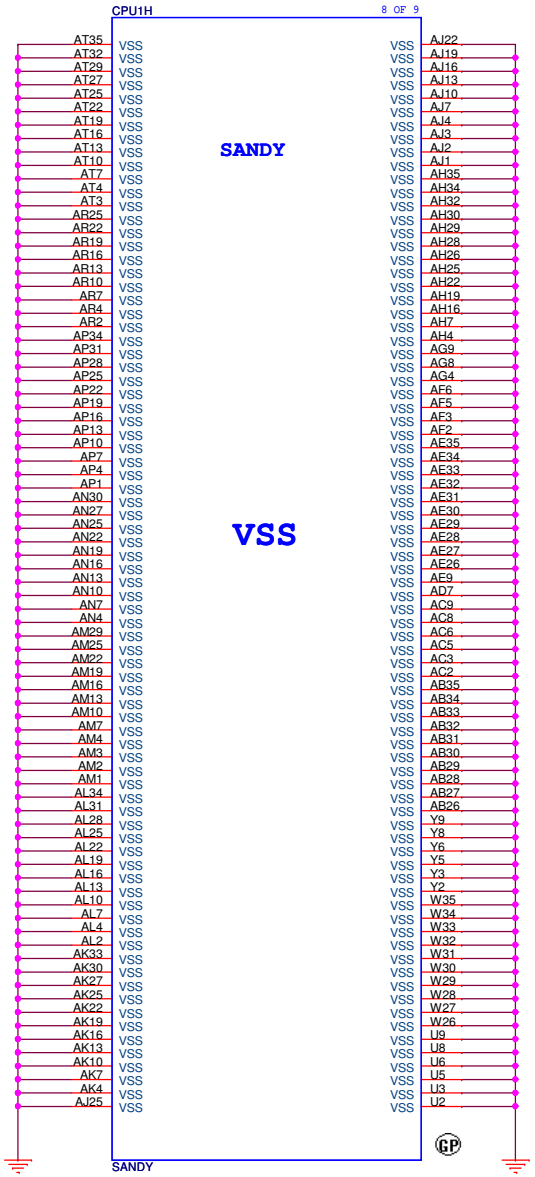
VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

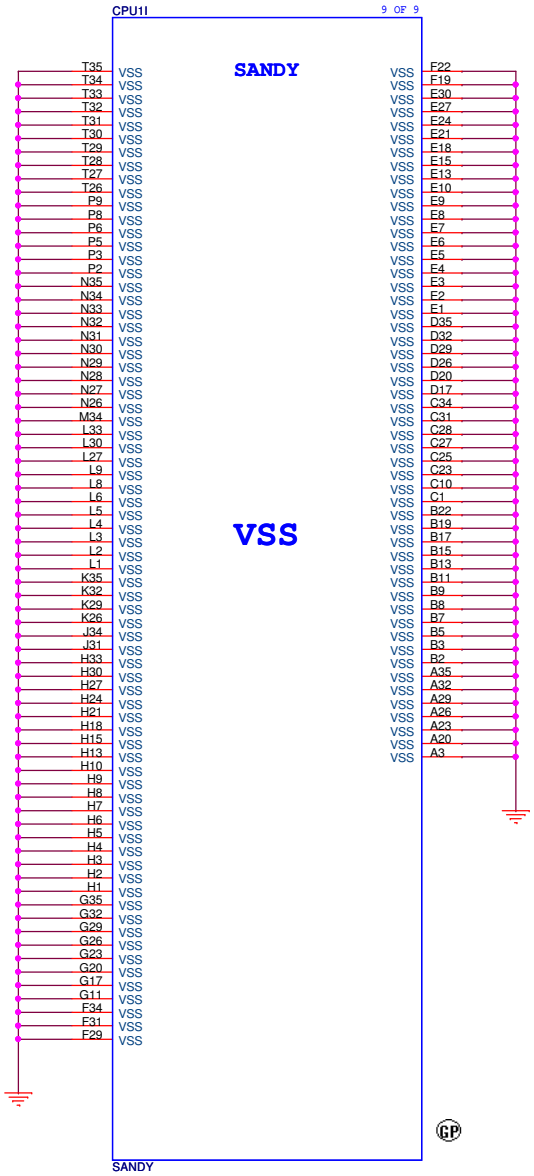
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU 6/7(VCC_GFX_CORE)
Size: | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 9 of 103

SSID = CPU





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU 7/7(VSS)	
Size	Document Number: Nirvana 13	Rev: A00
Date: Wednesday, December 22, 2010	Sheet 10 of 103	

(Blanking)

Remove the XDP connector for space saving 6/28

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP

Size: A3 | Document Number: NIRVANA 13 | Rev: A00

Date: Wednesday, December 22, 2010 | Sheet 11 of 103

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Wednesday, December 22, 2010 | Sheet 12 of 103

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<Core Design>

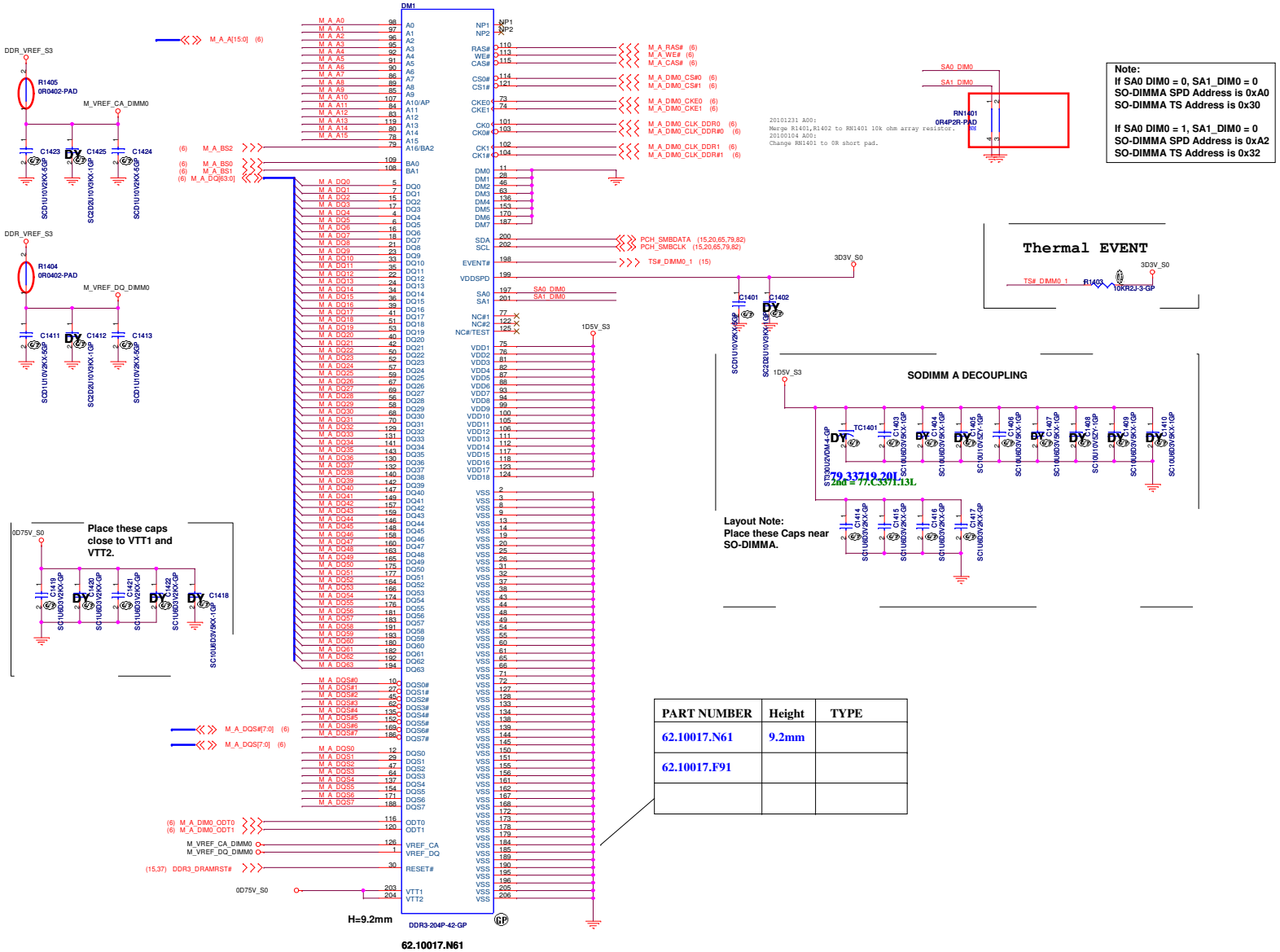
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Wednesday, December 22, 2010 | Sheet 13 of 103

SSID = MEMORY



PART NUMBER	Height	TYPE
62.10017.N61	9.2mm	
62.10017.F91		

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-DIMM1 SOCKET1

Size | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 18, 2011 | Sheet 14 of 103

SSID = MEMORY

DM2

DDR3-204P-48-GP

62.10017.P41

H=5.2mm

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

20100104 A00:
Change R1502 to 0R0402 short pad.

20101224 A00:
0402 0R pad: R1503 R1504.

Place these caps close to VTT1 and VTT2.

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

PART NUMBER	Height	TYPE
62.10017.P41	5.2mm	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-DIMM2 SOCKET2

Size | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 18, 2011 | Sheet 15 of 103

(Blanking)

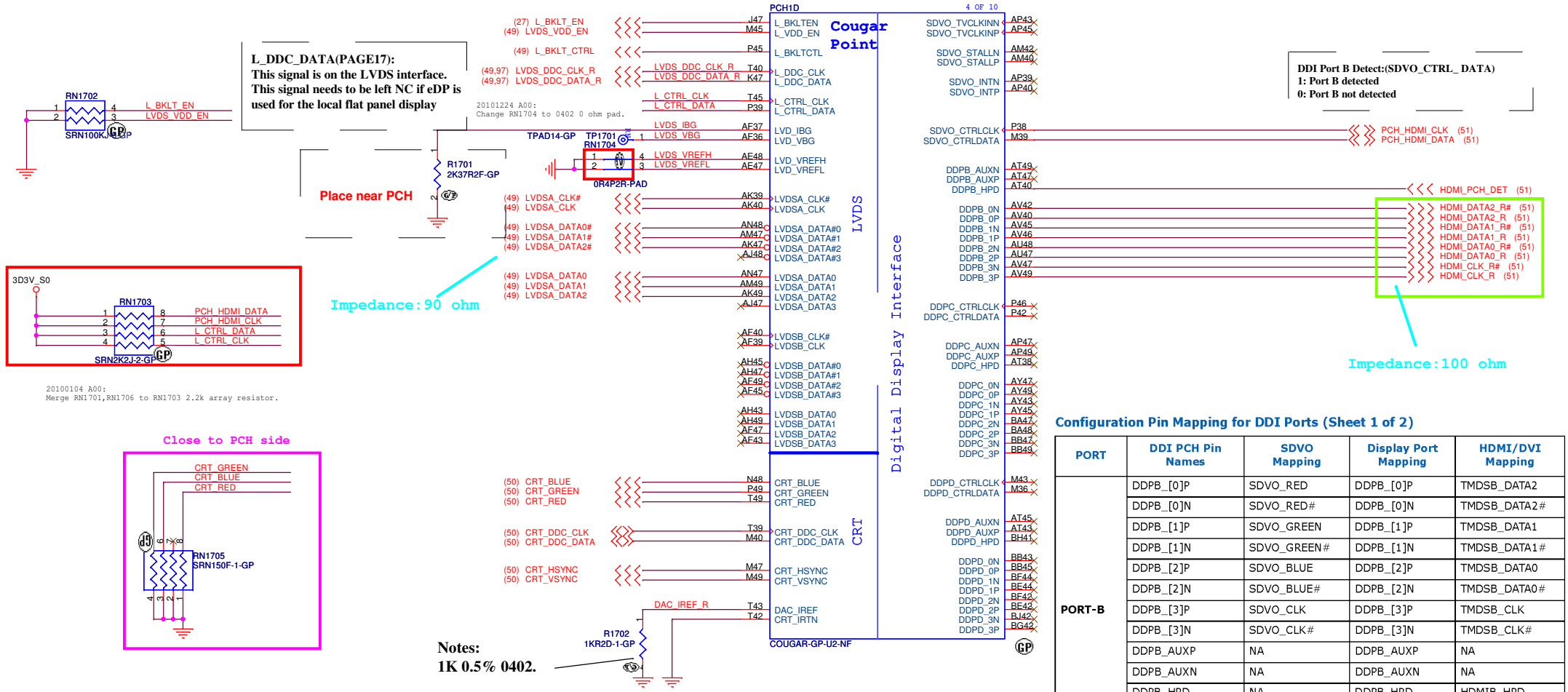
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Wednesday, December 22, 2010 | Sheet 16 of 103



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 1/9(LVDS/CRT/DDI)

Size | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 18, 2011 | Sheet 17 of 103

SSID = PCH

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

RN1801 SRN8K2J-2-GP: INT_PIRQB#, INT_PIRQF#, INT_PIRQA# → 3D3V_S0; INT_PIRQD#, INT_PIRQE#, INT_PIRQC#, INT_PIRQG# → 3D3V_S0

R1801 DY 4K7R2J-2-GP PCI_GNT3#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

RN1803 SRN10KJ-5-GP: DGPU_HOLD_RST#, DGPU_PWR_EN#

R1802 DY 1KR2J-1-GP BBS_BIT1

R1803 DY 1KR2J-1-GP BBS_BIT0 (21)

BOOT BIOS Strap

GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

PCH1E — Cougar Point — 5 OF 10

RSVD: TP1–TP20, TP21–TP24, TP25–TP40

NVRAM: RSVD, DF_TVS, NV_ALE, NV_CLE, NV_RCOMP → TP1803 TPAD14-GP

USB Ext. port 1 (HS)
External debug port use on Huron river platform

PCI: PIRQA#, PIRQB#, PIRQC#, PIRQD#, REQ1#/GPIO50, REQ2#/GPIO52, REQ3#/GPIO54, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5, PME#, PLTRST#, CLKOUT_PCI0–CLKOUT_PCI4

USB: USBP0N–USBP13N/P, USBRBIAS#, USBRBIAS, OC0#/GPIO59, OC1#/GPIO40, OC2#/GPIO41, OC3#/GPIO42, OC4#/GPIO43, OC5#/GPIO9, OC6#/GPIO10, OC7#/GPIO14

COUGAR-GP-U2-NF

USB_PN1 (57), USB_PP1 (57), USB_PN2 (64), USB_PP2 (64), USB_PN3 (63), USB_PP3 (63), USB_PN4 (82), USB_PP4 (82), USB_PN5 (32), USB_PP5 (32), USB_PN11 (65), USB_PP11 (65), USB_PN12 (49), USB_PP12 (49)

R1811 22D6R2F-L1-GP USB_RBIAS

USB_OC#0_1 (61), FFS_INT2_R (79)

R1814 8K2R2J-3-GP

TP1807 TPAD14-GP DGPU_HOLD_RST#, DGPU_SELECT#, DGPU_PWR_EN#

TP1806 TPAD14-GP DGPU_PWM_SELECT#

TP1801 TPAD14-GP BBS_BIT1, PCI_GNT3#

TP1802 TPAD14-GP PCI_PME#

(79) HDD_FALL_INT1
(56) SATA_ODD_DA#
(82) USB30_SMI#
(69) KB_LED_BL_DET

R1812 0R0402-PAD INT_PIRQE#
R1813 0R0402-PAD INT_PIRQF#
R1815 0R0402-PAD INT_PIRQG#
R1817 0R0402-PAD INT_PIRQH#

RN1804 SRN22-3-GP

20101231 A00:
Merge R1804,R1806 to RN1804 22 ohm array resistor.
20110113 A00:
Swap RN1804 base on swap report.

(65,71) CLK_PCI_LPC
(20) CLK_PCI_FB
(27) CLK_PCI_KBC

R1805 22R2J-2-GP CLK_PCI_LPC_R, CLK_PCI_FB_R, CLK_PCI_KBC_R

EC1801 DY SC4D7P50V2CN-1GP
EC1802 DY SC4D7P50V2CN-1GP

KBC CLK EMI

20101224 A00:
0402 0R pad: R1807.

R1807 0R0402-PAD (5,27,65,71,82) PLT_RST# → PCI_PLTRST#

R1816 DY 100KR2J-GP

C1801 DY SC220P50V2KX-3GP

R1818 10KR2J-3-GP FFS_INT2_R

RN1802 SRN8K2J-2-GP: USB_OC#2_3, USB_OC#6_7, USB_OC#0_1 → 3D3V_S5; USB_OC#12_13, USB_OC#8_9, USB_OC#10_11, USB_OC#4_5

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

1D8V_S0 — R1808 2K2R2J-2-GP — R1809 1KR2J-1-GP — NV_CLE → H_SNB_IVB# (5)

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

1D8V_S0 — R1810 1KR2J-1-GP DY — NV_ALE

Danbury Technology:
Disabled when Low.
Enable when High.

USB Table

Pair	Device
0	X
1	E-SATA / USB Combo
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	X
9	X
10	X
11	Mini Card1 (WLAN)
12	CAMERA
13	X

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 2/9(PCI/USB/NVRAM)
Size: Document Number: Nirvana 13 Rev: A00
Date: Tuesday, January 18, 2011 Sheet 18 of 103

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.

PCH1C — 3 OF 10 — Cougar Point

DMI: DMI0RXN, DMI1RXN, DMI2RXN, DMI3RXN, DMI0RXP, DMI1RXP, DMI2RXP, DMI3RXP, DMI0TXN, DMI1TXN, DMI2TXN, DMI3TXN, DMI0TXP, DMI1TXP, DMI2TXP, DMI3TXP

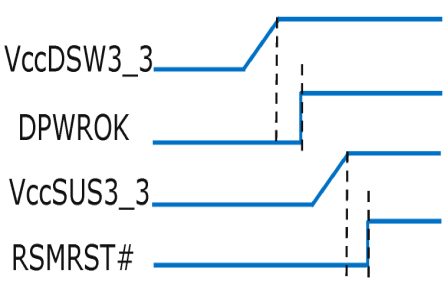
FDI: FDI_RXN0–7, FDI_RXP0–7, FDI_INT, FDI_FSYNC0, FDI_FSYNC1, FDI_LSYNC0, FDI_LSYNC1, FDI_TXN0–7, FDI_TXP0–7

System Power Management: DSWVRMEN, DPWROK, WAKE#, CLKRUN#/GPIO32, SUS_STAT#/GPIO61, SUSCLK/GPIO62, SLP_S5#/GPIO63, SLP_S4#, SLP_S3#, SLP_A#, SLP_SUS#, PMSYNCH, SLP_LAN#/GPIO29, SUSACK#, SYS_RESET#, SYS_PWROK, PWROK, APWROK, DRAMPWROK, RSMRST#, SUSWARN#/SUSPWRDNACK/GPIO30, PWRBTN#, ACPRESENT/GPIO31, BATLOW#/GPIO72, RI#

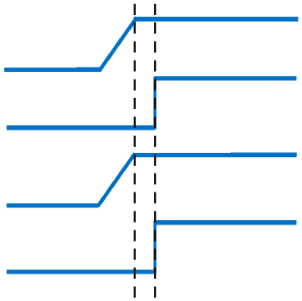
COUGAR-GP-U2-NF

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

Deep S4/S5 Supported



Deep S4/S5 **Not** Supported



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

DSWODVREN – On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SSID = PCH

PCH1B — Cougar Point — 2 OF 10

PCI-E*: W-WAN, LAN, Card Reader, WLAN, USB3.0, Intel GBE LAN, Dock, NEW CARD

SMBUS: SMBALERT#/GPIO11, SMBCLK, SMBDATA, SML0ALERT#/GPIO60, SML0CLK, SML0DATA, SML1ALERT#/PCHHOT#/GPIO74, SML1CLK/GPIO58, SML1DATA/GPIO75

Controller Link: CL_CLK1, CL_DATA1, CL_RST1#

CLOCKS: PEG_A_CLKRQ#/GPIO47, CLKOUT_PEG_A_N/P, CLKOUT_DMI_N/P, CLKOUT_DP_N/P, CLKIN_DMI_N/P, CLKIN_GND1_N/P, CLKIN_DOT_96N/P, CLKIN_SATA_N/P, REFCLK14IN, CLKIN_PCILOOPBACK, XTAL25_IN/OUT, XCLK_RCOMP

FLEX CLOCKS: CLKOUTFLEX0/GPIO64, CLKOUTFLEX1/GPIO65, CLKOUTFLEX2/GPIO66, CLKOUTFLEX3/GPIO67

COUGAR-GP-U2-NF

20101224 A00: Change RN2011~RN2014 to 0402 0 ohm pad.

20101224 A00: Change RN2010 to 0402 0 ohm pad.

20110112 A00: Change C2007,C2008 to 15pF from 12pF base on vendor's report.

WWAN CLK — RN2011 0R4P2R-PAD

WLAN CLK — RN2012 0R4P2R-PAD

LAN CLK — RN2014 0R4P2R-PAD

USB3.0 CLK — RN2013 0R4P2R-PAD

PCIECLKRQ1# and PCIECLKRQ2# Support S0 power only

PL 10K FOR Integrated CLOCK GEN mode.

need very close to PCH

For RTS5138

- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

2nd = 84.DM601.03F
84.2N702.A3F
2N7002KDW-GP

82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

UMA_DISCRETE#
UMA: 1 1
DIS :0 1
SG(PX) : 0 0
ATI(Muxless) : 1 0

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH 4/9(PCI-E/SMBUS/CLOCK/CL)
Size: | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 20 of 103

SSID = PCH

20110110 A00:
Merge R2115,R2116 to RN2101.

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.

20100721 Modify:
Remove TP2105 and change PCH_GPIO33 to CE.

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

NO REBOOT STRAP

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

PCH1A — Cougar Point — 1 OF 10 — COUGAR-GP-U2-NF

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17
LPC: FWH0/LAD0 C38, FWH1/LAD1 A38, FWH2/LAD2 B37, FWH3/LAD3 C37, FWH4/LFRAME# D36, LDRQ0# E36, LDRQ1#/GPIO23 K36, SERIRQ V5
IHDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN#/GPIO33 C36, HDA_DOCK_RST#/GPIO13 N32
JTAG: JTAG_TCK J3, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1
SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3
SATA 6G: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5, SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10, SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4
SATA: SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1, SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1, SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO Y11, SATAICOMPI Y10, SATA3RCOMPO AB12, SATA3COMPI AB13, SATA3RBIAS AH1, SATALED# P3, SATA0GP/GPIO21 V14, SATA1GP/GPIO19 P1

HDD1 — SATA_RXN0 (56), SATA_RXP0 (56), SATA_TXN0 (56), SATA_TXP0 (56)
HDD2
ODD — SATA_RXN4 (56), SATA_RXP4 (56), SATA_TXN4 (56), SATA_TXP4 (56)
ESATA — SATA_RXN5 (57), SATA_RXP5 (57), SATA_TXN5 (57), SATA_TXP5 (57)

SATA_COMP R2112 37D4R2F-GP
SATA3_COMP R2113 49D9R2F-GP
RBIAS_SATA3 R2114 750R2F-GP
1D05V_VTT

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Title: PCH 5/9(SPI/RTC/LPC/SATA/IHDA)
Size: | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 21 of 103

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

	GSENSOR_ADI	GSENSOR_ST
R2205	DY	10K
R2206	100K	DY

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

[VRAM_SIZE1:VRAM_SIZE2]
LL=512M / HL=1G / LH=2G

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

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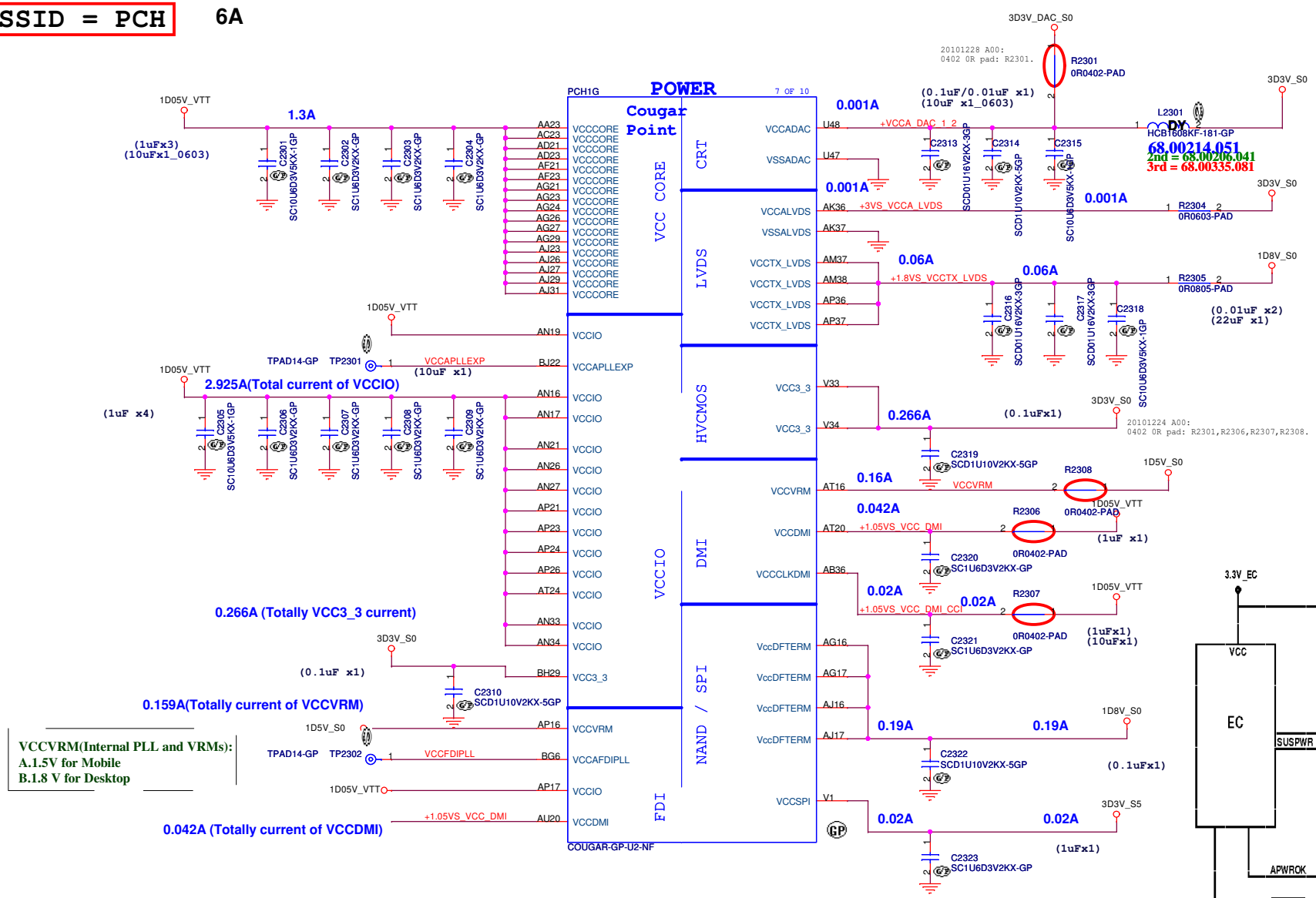
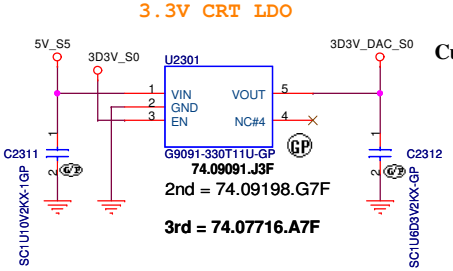
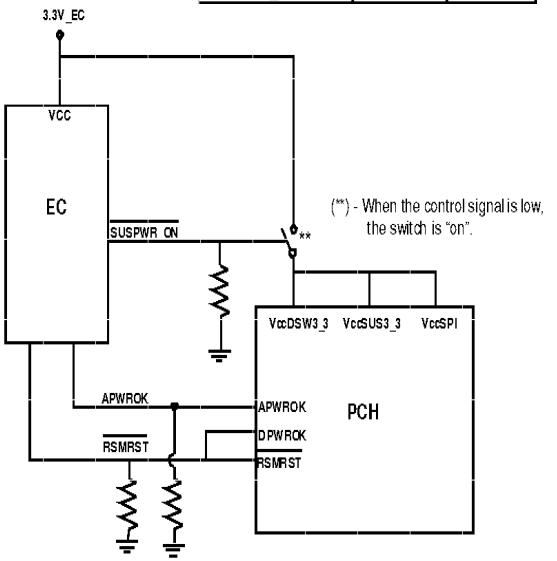
Title: PCH 6/9(GPIO/CPU)
Size: | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 22 of 103

SSID = PCH 6A

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06







<Core Design>

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Title: PCH 7/9(POWER1)
Size: | Document Number: Nirvana 13 | Rev: A00
Date: Wednesday, December 29, 2010 | Sheet 23 of 103

SSID = PCH

PCH1J — POWER — 10 OF 10 — Cougar Point

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

<Core Design>

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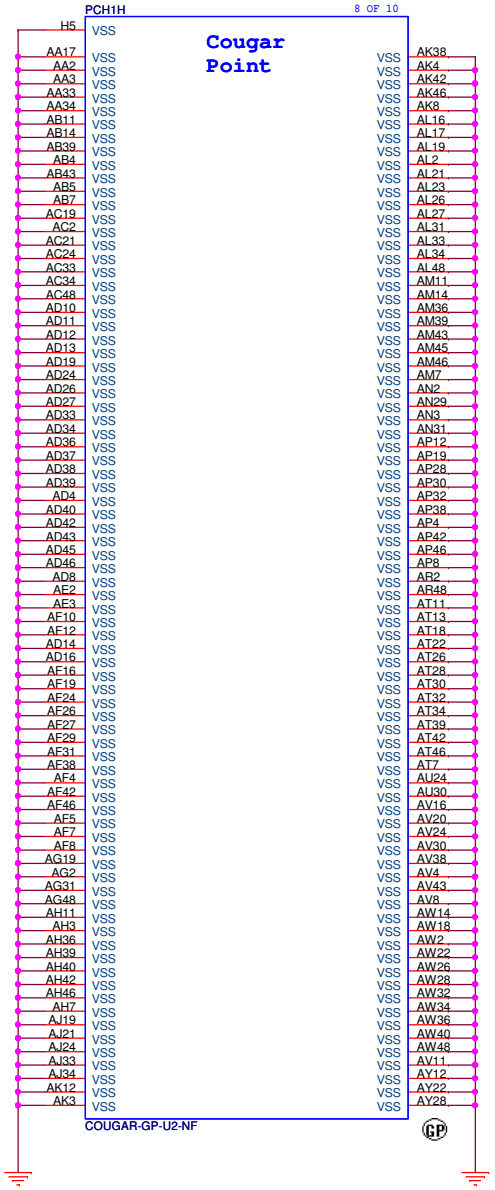
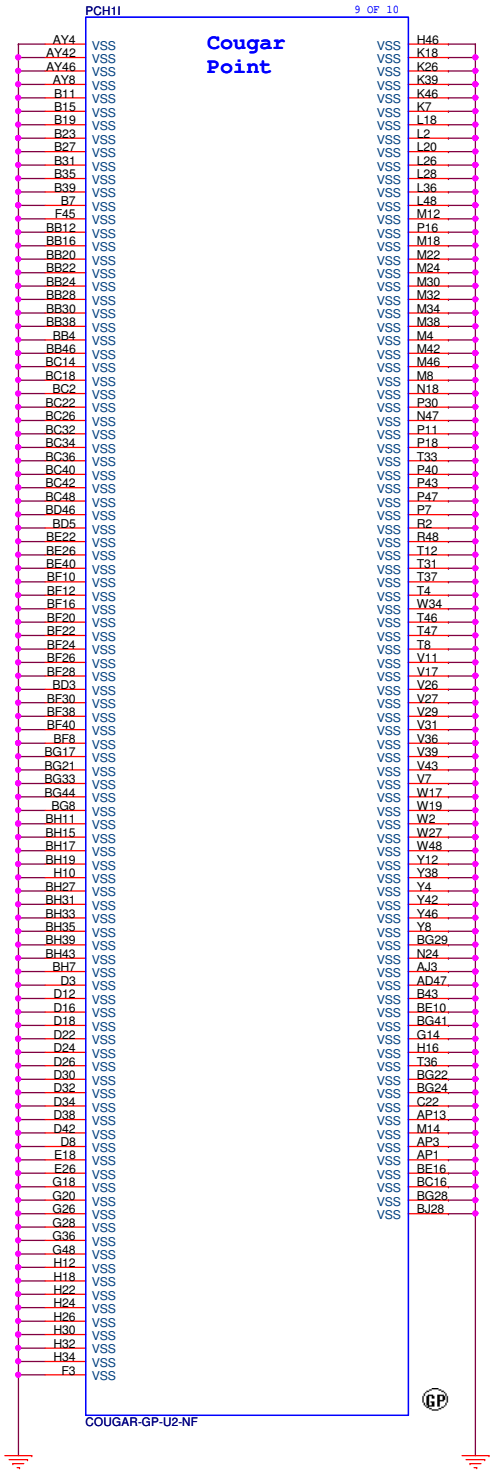
Title: PCH 8/9(POWER2)
Size: | Document Number: Nirvana 13 | Rev: A00
Date: Friday, December 24, 2010 | Sheet 24 of 103

SSID = PCH





<Core Design>

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Title: PCH 9/9(VSS)

Size | Document Number: Nirvana 13 | Rev: A00

Date: Wednesday, December 22, 2010 | Sheet 25 of 103

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Nirvana 13 | Rev: A00

Date: Wednesday, December 22, 2010 | Sheet 26 of 103

SSID = KBC

PCB VERSION AD(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
DQ15_UMA	100.0K	10.0K(64.10025.6DL)	3.0V
DQ15_ATI	100.0K	20.0K(64.20025.6DL)	2.75V
DQ15_NVIDIA	100.0K	33.0K	2.48V
DN15_UMA	100.0K	47.0K(64.47025.6DL)	2.24V
DN15_ATI	100.0K	64.9K(64.64925.6DL)	2.0V
Reserved	100.0K	76.8K	1.87V
Reserved	100.0K	100.0K	1.65V
DN13_UMA	100.0K	143.0K	1.358V
DN13_ATI	100.0K	174.0K	1.204V
DQ15_Ventura	100.0K	215.0K	1.048V

NOTES:
The NPCE795P GPIO/PWM outputs that are connected to LEDs have high drive buffers (20mA) and can be connected directly to the LEDs.

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

ROSA Multi GPIO setting

EC_GPIO47 High Active

PSL SOLUTION **10mW SOLUTION**

VBACKUP

PSL_IN1

PSL_OUT

EC GPIO standard PH/PL

MEDIA BUTTON CONTROL

NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,E51_TXD.

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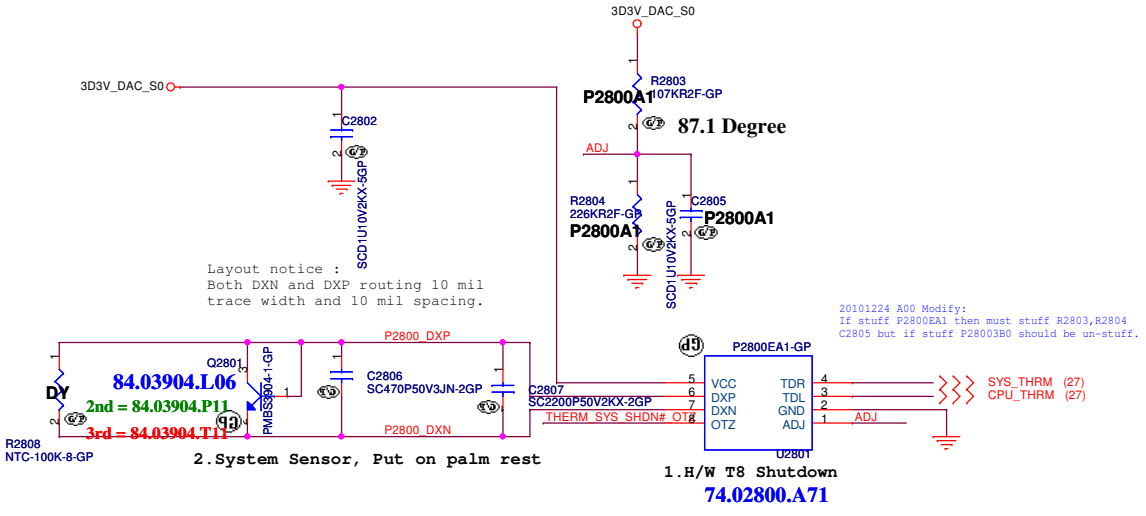
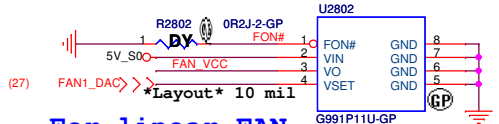
Title: KBC Nuvoton NPCE785P
Size: A2 | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 27 of 103

SSID = Thermal

Thermal sensor P2800

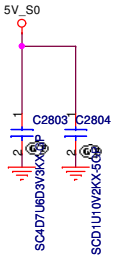


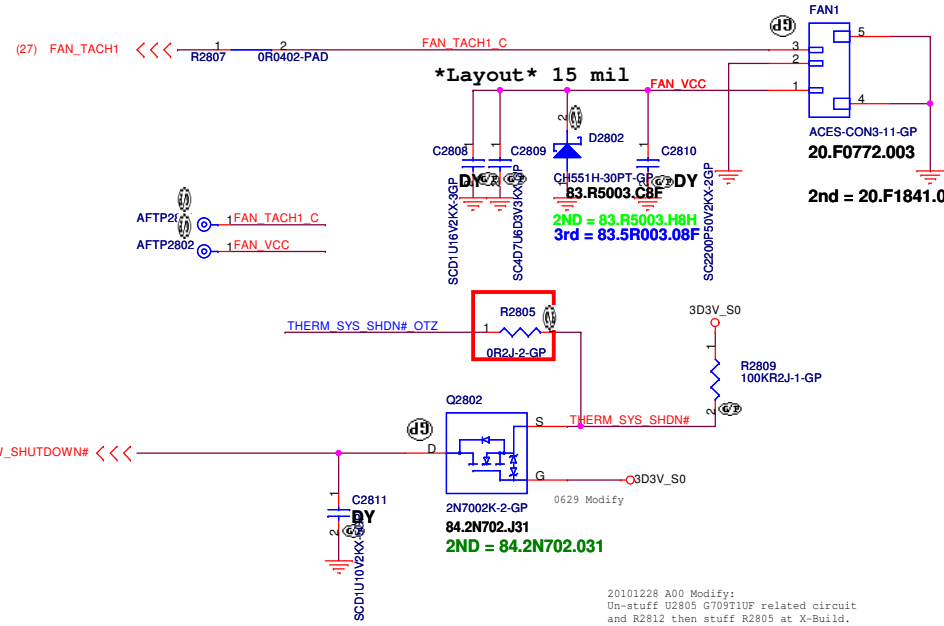
Fan controller

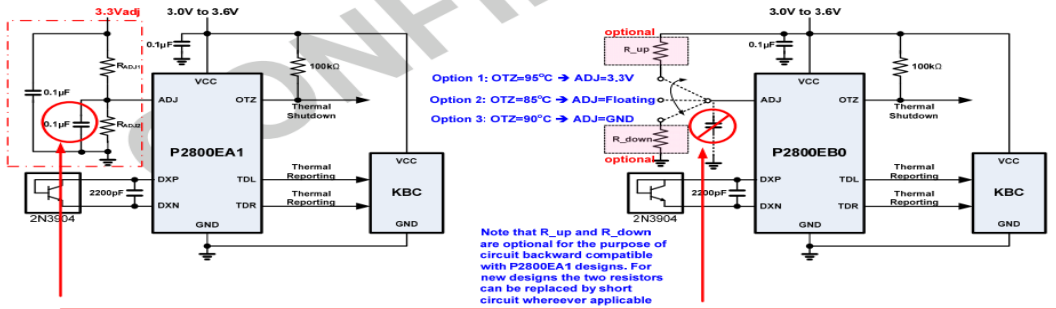


For linear FAN

PIN#	I/O	FUNCTION
1	I	Internal Pull-high (P2793A). The IC will be functioning when /FON voltage is above 1.6V. When /FON is low(<0.4V), VOUT will be fully on
2	O	Input Voltage
3	O	Output Voltage
4	I	The voltage on this input pin controls the VOUT voltage by the formula: VOUT=1.6 * VSET When VSET is under 0.8V, the IC will be shutdown
5,6,7,8	O	Ground

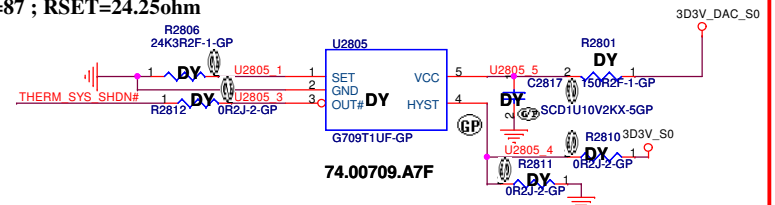






Note:
The original 0.1uF capacitor for P2800EA1 deisgn must be REMOVED on the ADJ pin of P2800EB0

RSET = 0.0012T 2 — 0.9308T + 96.147
T=87 ; RSET=24.25ohm



Hysterisis is 10°C for HYST = VCC, 2°C for HYST = GND.

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL P2800 / Fan control
Size: A3 | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 28 of 103

SSID = AUDIO

U2901 92HD87B1A5NDGXTBX8-GP
71.92H87.A03

Close to codec

Put C2921 and C2922 close to codec

AUD_PC_BEEP
Trace width>15 mils

From PCH

From EC

Close to codec

Azalia I/F EMI

Close to Pin13

Close to Pin14

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD87B1

Size	Document Number	Rev
A3	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 29 of 103

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: Nirvana 13 | Rev: A00

Date: Wednesday, December 22, 2010 | Sheet 30 of 103

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<Core Design>

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Title: *Reserved*

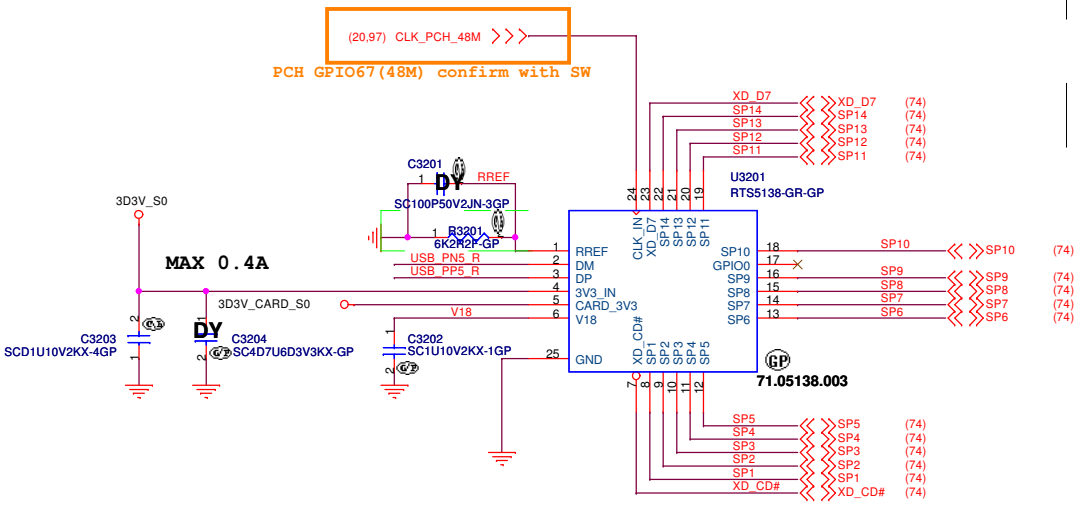
Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

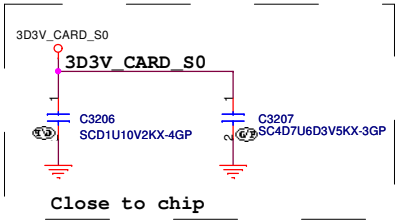
Date: Wednesday, December 22, 2010 | Sheet 31 of 103

SSID = SDIO

PIN	TYPE	FUNCTION	RTS5138 NET
1	SD	SD-DAT2	SP13
2	SD	SD-CD/DAT3	SP12
3	MMC_PLUS	MMC-DAT4	SP11
4	SD	SD-CMD	SP10
5	MMC_PLUS	MMC-DAT5	SP9
6	SD	SD-VSS	POWER
7	SD	SD-VDD	POWER
8	MemoryStick	MS-VSS	POWER
9	MemoryStick	MS-VCC	POWER
10	MemoryStick	MS-SCLK	SP1
11	MemoryStick	MS-DATA3	SP5
12	MemoryStick	MS-INS	SP2
13	MemoryStick	MS-DATA2	SP8
14	MemoryStick	MS-DATA0	SP9
15	MemoryStick	MS-DATA1	SP12
16	MemoryStick	MS-BS	SP14
17	MemoryStick	MS-VSS	POWER
18	SD	SD-CLK	SP8
19	MMC_PLUS	MMC-DAT6	SP7
20	SD	SD-VSS	POWER
21	MMC_PLUS	MMC-DAT7	SP5
22	SD	SD-DAT0	SP4
23	SD	SD-DAT1	SP3
24	SD	SD-COM(SW)	
25	SD	SD-CD(SW)	SP6
26	XD	XD-GND	POWER
27	XD	XD-CD	XD_CD#
28	XD	XD-R/-B	SP1
29	XD	XD-RE	SP2
30	XD	XD-CE	SP3
31	XD	XD-CLE	SP4
32	XD	XD-ALE	SP5
33	XD	XD-WE	SP6
34	XD	XD-WP	SP7
35	XD	XD-GND	POWER
36	XD	XD-D0	SP8
37	XD	XD-D1	SP9
38	XD	XD-D2	SP10
39	XD	XD-D3	SP11
40	XD	XD-D4	SP12
41	XD	XD-D5	SP13
42	XD	XD-D6	SP14
43	XD	XD-D7	XD-D7
44	XD	XD-VCC	POWER
45	SD	SD-WP(SW)	SP1

48MHz clock input trace of characteristic impedance (Zo) must be 50 ±15%.

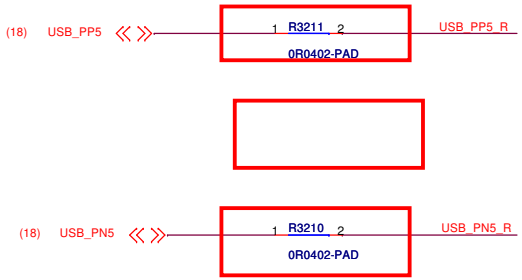




The maximum range of the PMOS output current
1. xD-Picture Card: 250mA
2. SD/MMC Card: 250mA
3. MS/MSPRO/Duo-HG: 250mA

POWER TRACE
1.RTS5138: pin 4 (3V3_IN) trace fixed width is 30 mils (minimum).
2.RTS5138: pin 5 (CARD_3V3) trace fixed width is 30 mils (minimum).
3.RTS5138: pin 6 (V18) trace fixed width is 12 mils (minimum).
Keep the trace routing lengths as short as possible.
4.RTS5138: pin 1(RREF) trace fixed width is 12 mils (minimum).
5.RTS5138: pin 1(RREF) trace must far away 48MHz clock trace.
6.De-coupling and Bulk capacitor should place near to RT5138 chip and Combo Socket.
7.It is recommended that use of ferrites bead on power trace.
8.Via size: Pad>=32 mils, Finished hole>=16 mils.

The pin2 / pin3 (DM/DP) of RTS5138 chip trace layout with differential characteristic impedance (Zdiff) is 90Ω± 10%



20101227 A00:
Change R3210,R3211 to 0R 0402 pad.
20100104 A00:
Remove TR3201.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader RTS5138
Size: A3 | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 32 of 103

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Wednesday, December 22, 2010 | Sheet 33 of 103

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Wednesday, December 22, 2010 | Sheet 34 of 103

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

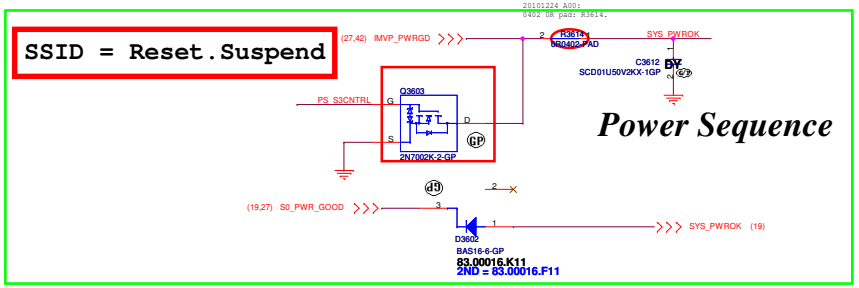
Title: *Reserved*

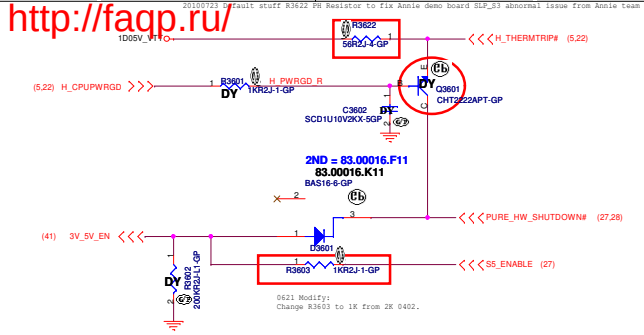
Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Wednesday, December 22, 2010 | Sheet 35 of 103

SSID = Reset.Suspend

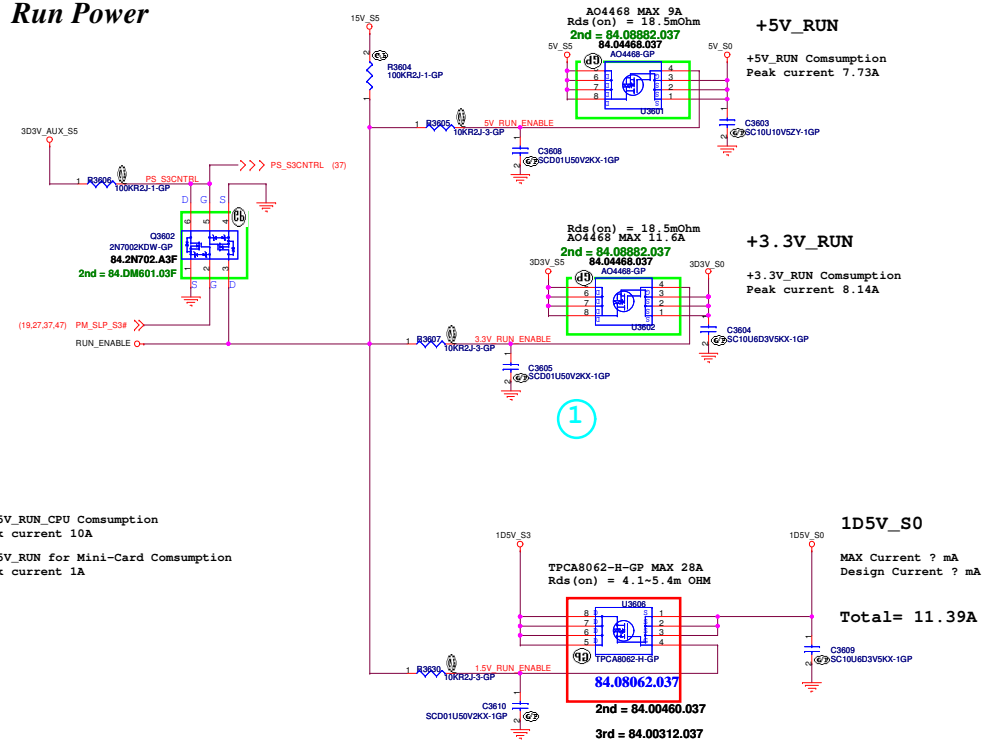
Power Sequence





SSID = Reset.Suspend

Run Power



<Core Design>

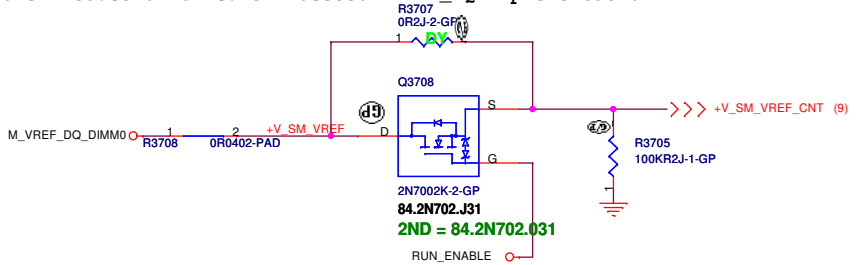
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

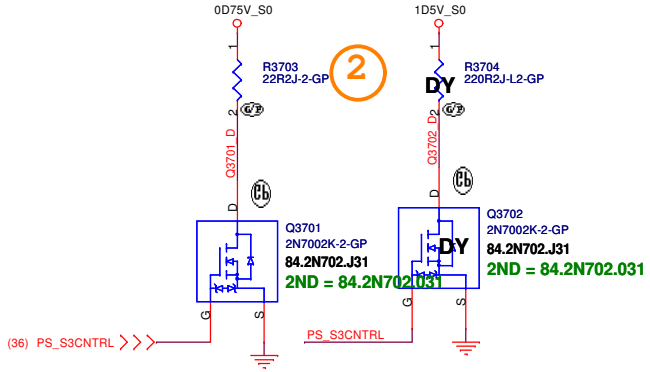
Size: A2 | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 18, 2011 | Sheet 36 of 103

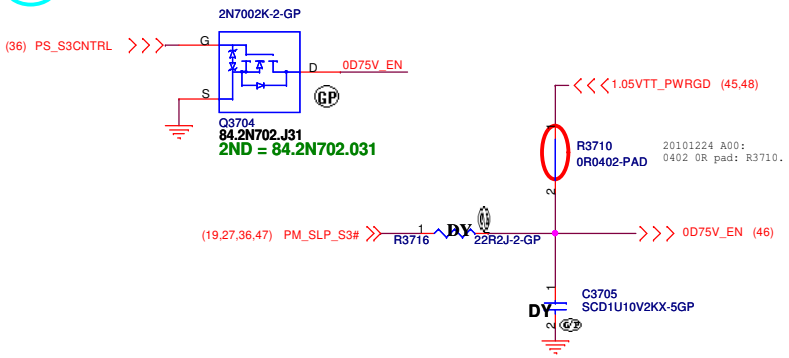
Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation



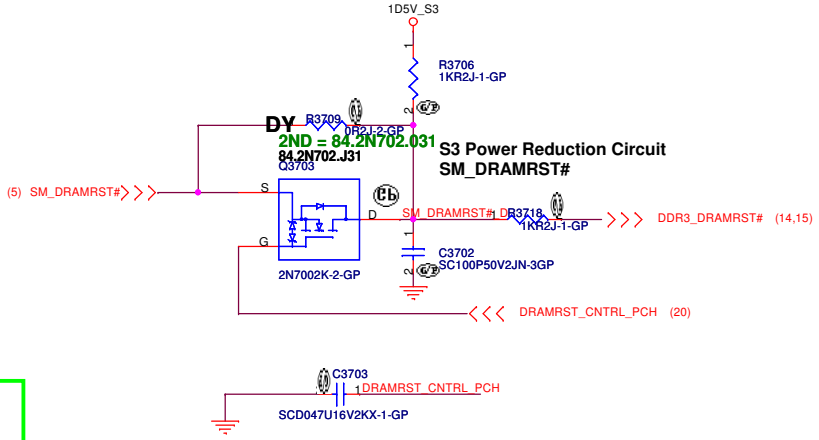
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



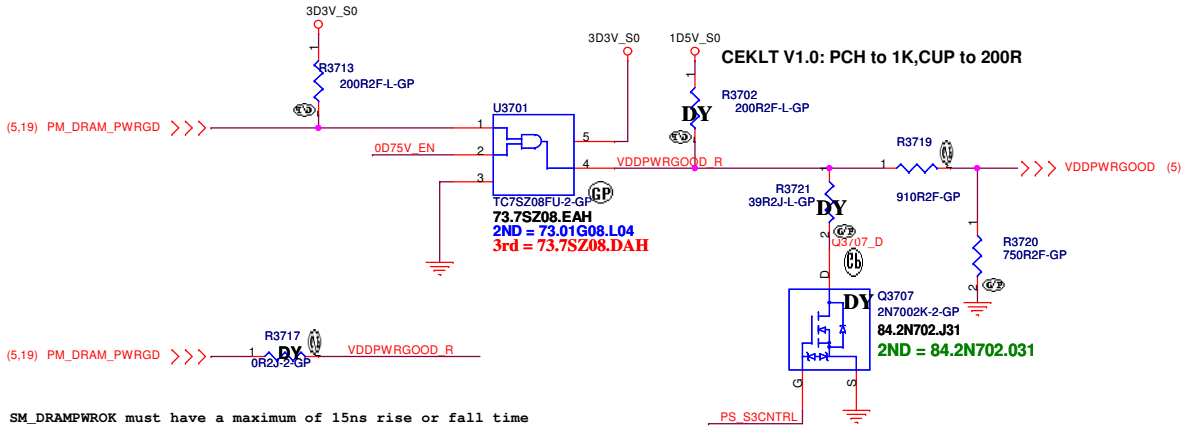
5 S3 Power Reduction



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



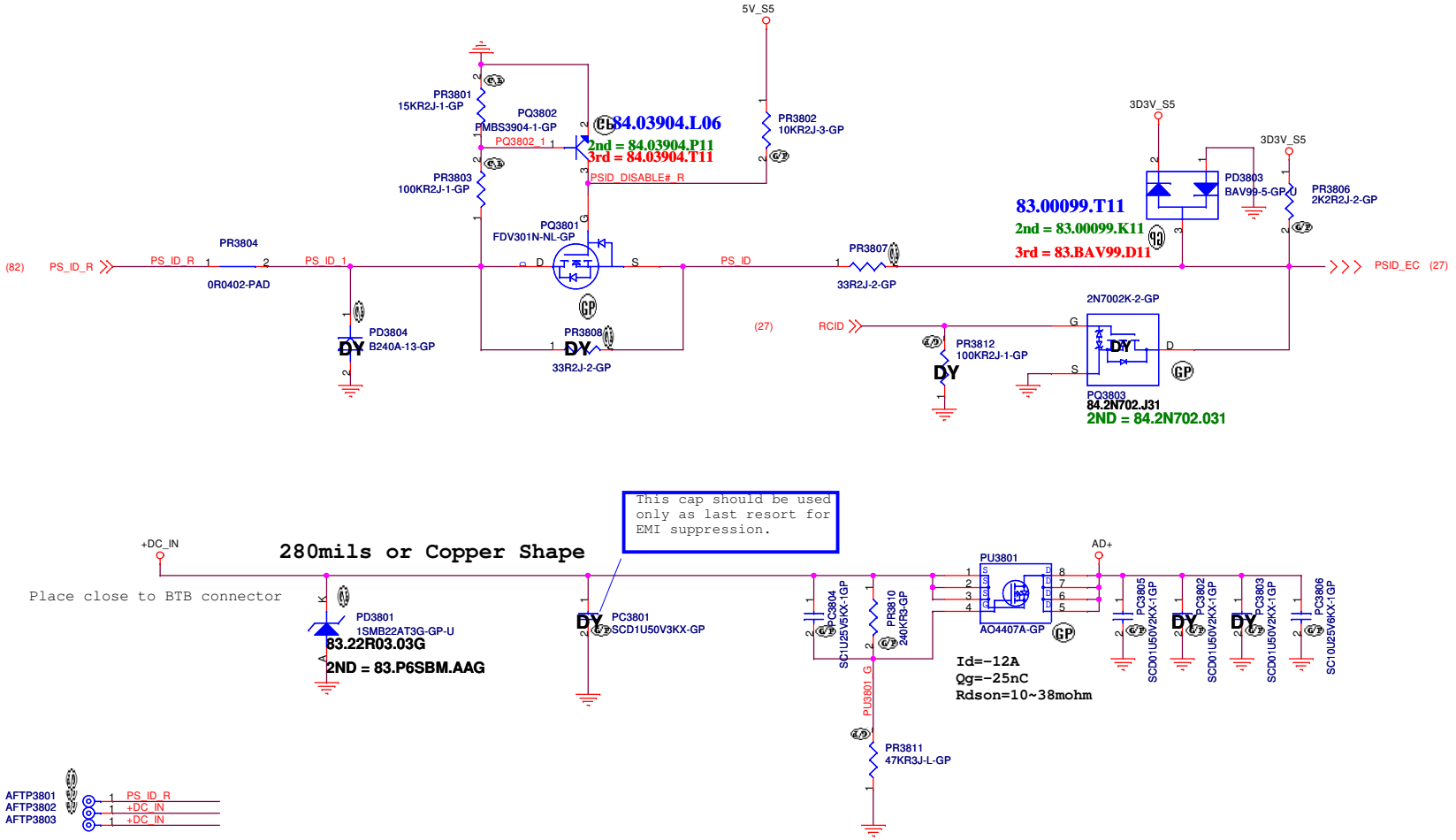
Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
S3 Power Reduction		
Size: A3	Document Number: Nirvana 13	Rev: A00
Date: Tuesday, January 18, 2011	Sheet 37 of 103	



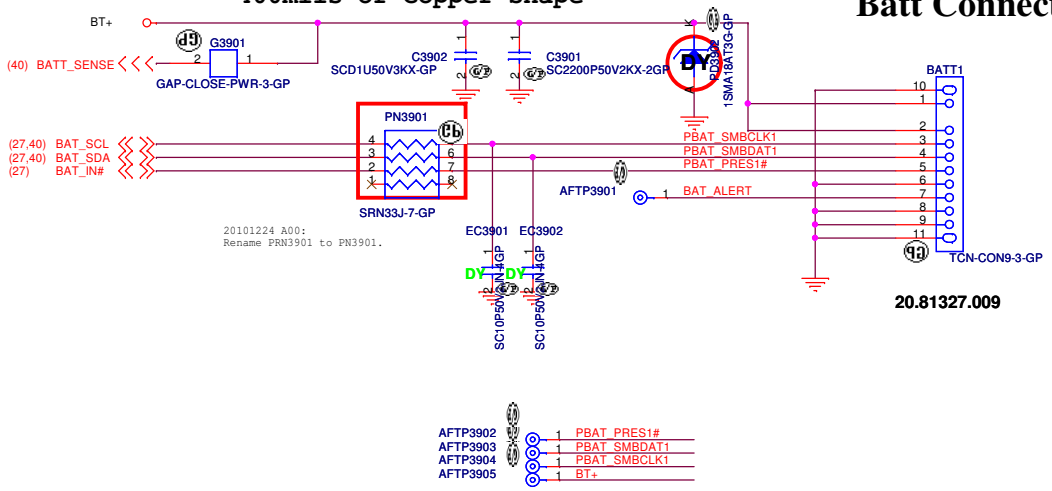
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN Jack		
Size: A3	Document Number: Nirvana 13	Rev: A00
Date: Tuesday, January 18, 2011	Sheet 38 of 103	

400mils or Copper Shape

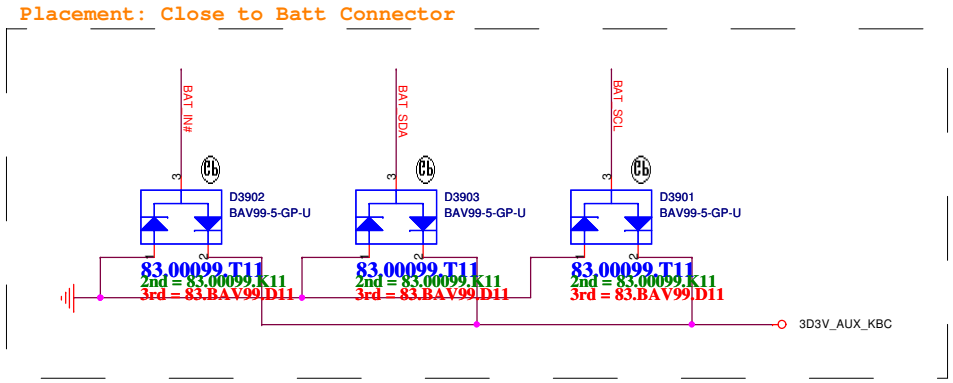
Batt Connecter



20.81327.009

For actual location, need to be swap all pin

Placement: Close to Batt Connector

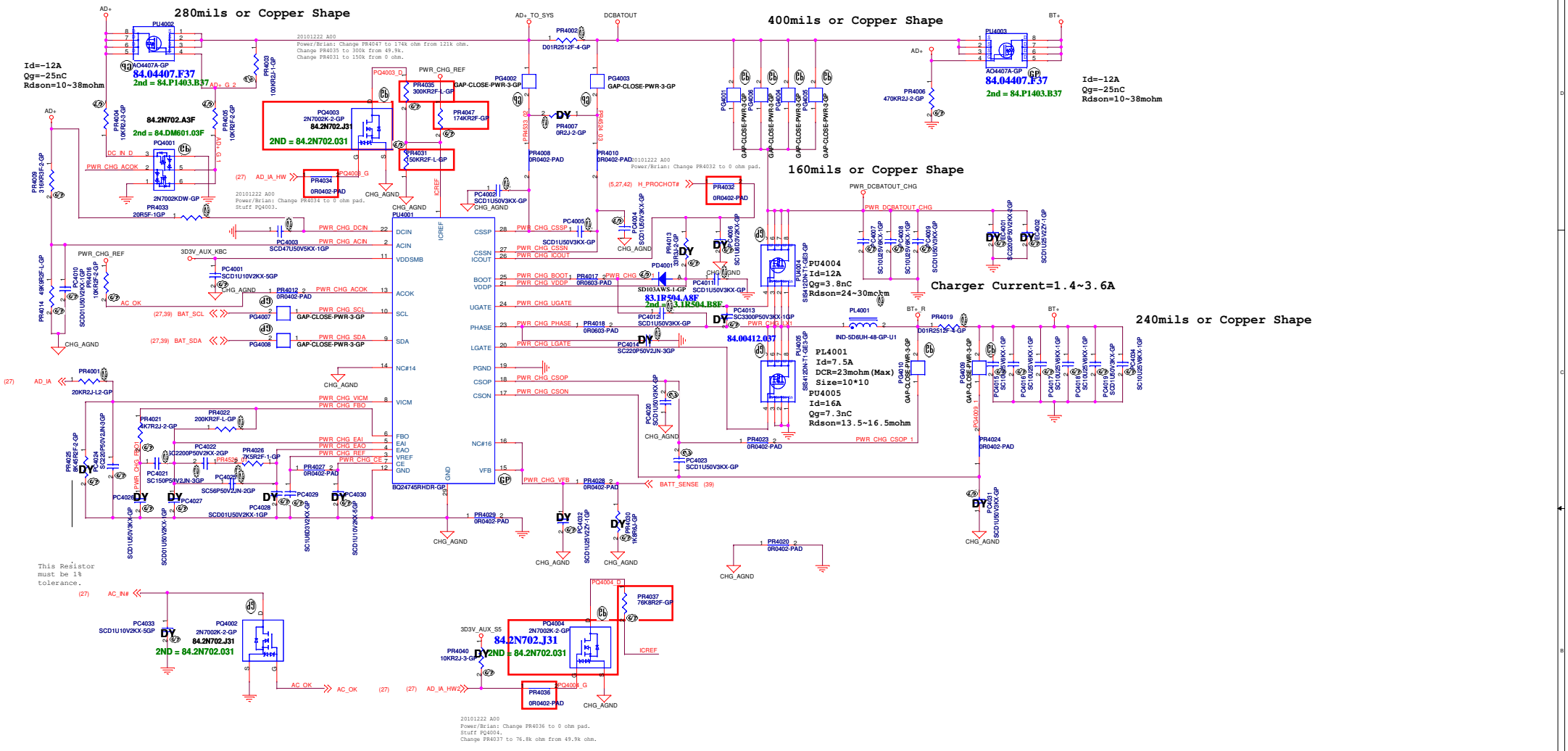


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN		
Size: A3	Document Number: Nirvana 13	Rev: A00
Date: Tuesday, January 18, 2011	Sheet 39 of 103	

SSID = Charger



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHARGER BQ24745	
Size	Document Number: Nirvana 13	Rev: A00
Date: Tuesday, January 18, 2011	Sheet 40 of 103	

Vout (5V) =VFB1* (1+R1/R2)

Design Current = 16A
25.1A<OCP< 29.3A

Design Current = 7.4A
11.6A<OCP< 13.7A

Connect VFB1to GND for fixe 5V opteration

V_REFIN2=VREF2*PR4109/ (PR4109+PR4105)
Vout (3.3V) =V_REFIN2* (1+R1/R2)

Connect REFIN2 to V5FILT for fixed 3.3V operation

74.09091.J3F
2nd = 74.09198.G7F
3rd = 74.07716.A7F

84.07410.A37
84.07702.037
77.22271.27L
79.10712.L02
2nd = 79.10712.6JL

SKIPSEL	GND	FLOAT/VREF2	V5IN
Mode	Auto Skip	OOA.	PWM Only

TONSEL	GND	VREF2 or Float	V5FILT
Ch1	400 kHz	400 kHz	200 kHz
Ch2	500 kHz	300 kHz	300 kHz

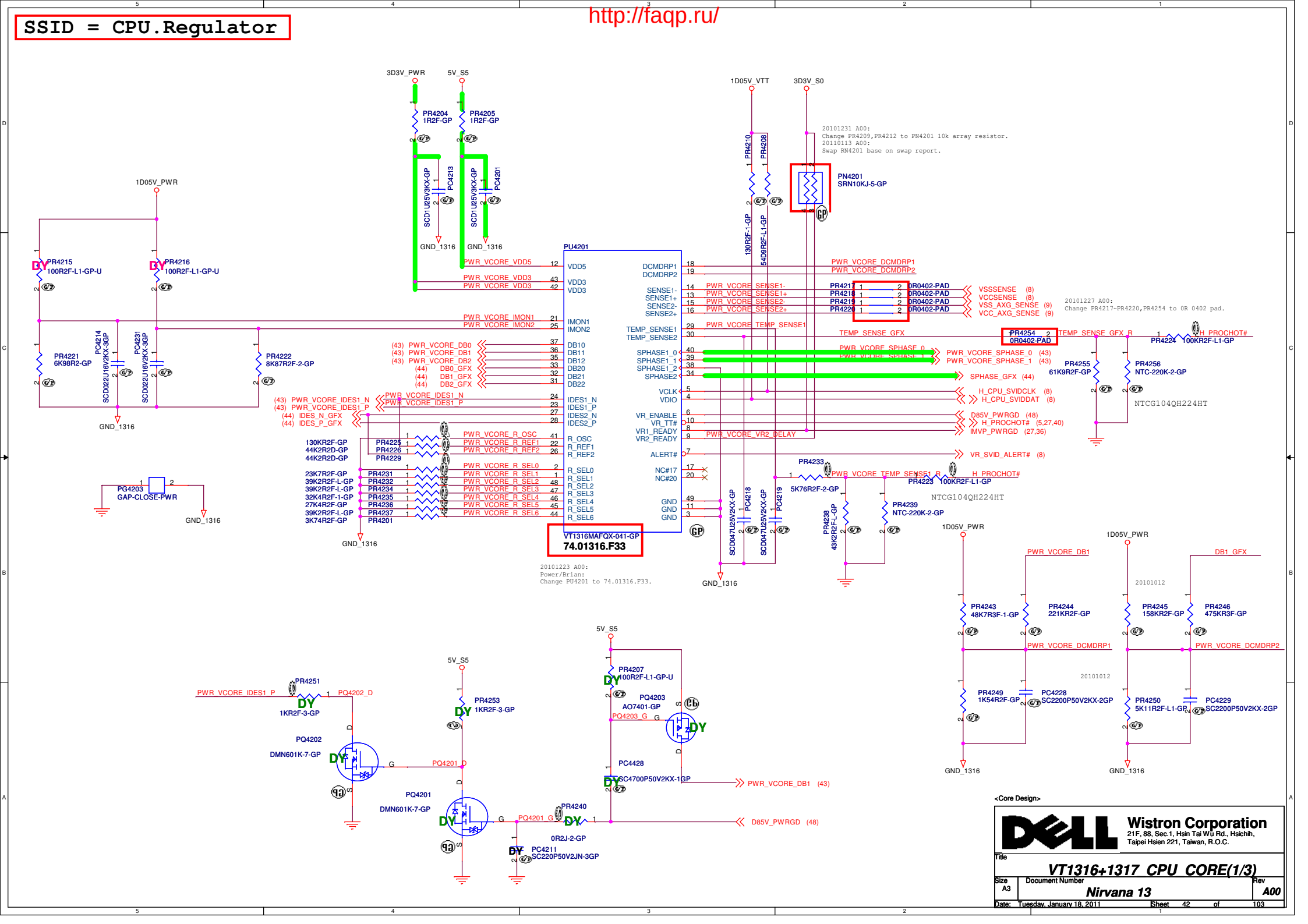
1A= 40mils
0.5A= 20mils
0.375A= 15mils

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51427_5V/3D3V
Size: A2
Document Number: Nirvana 13
Rev: A00
Date: Tuesday, January 18, 2011
Sheet 41 of 103

SSID = CPU.Regulator



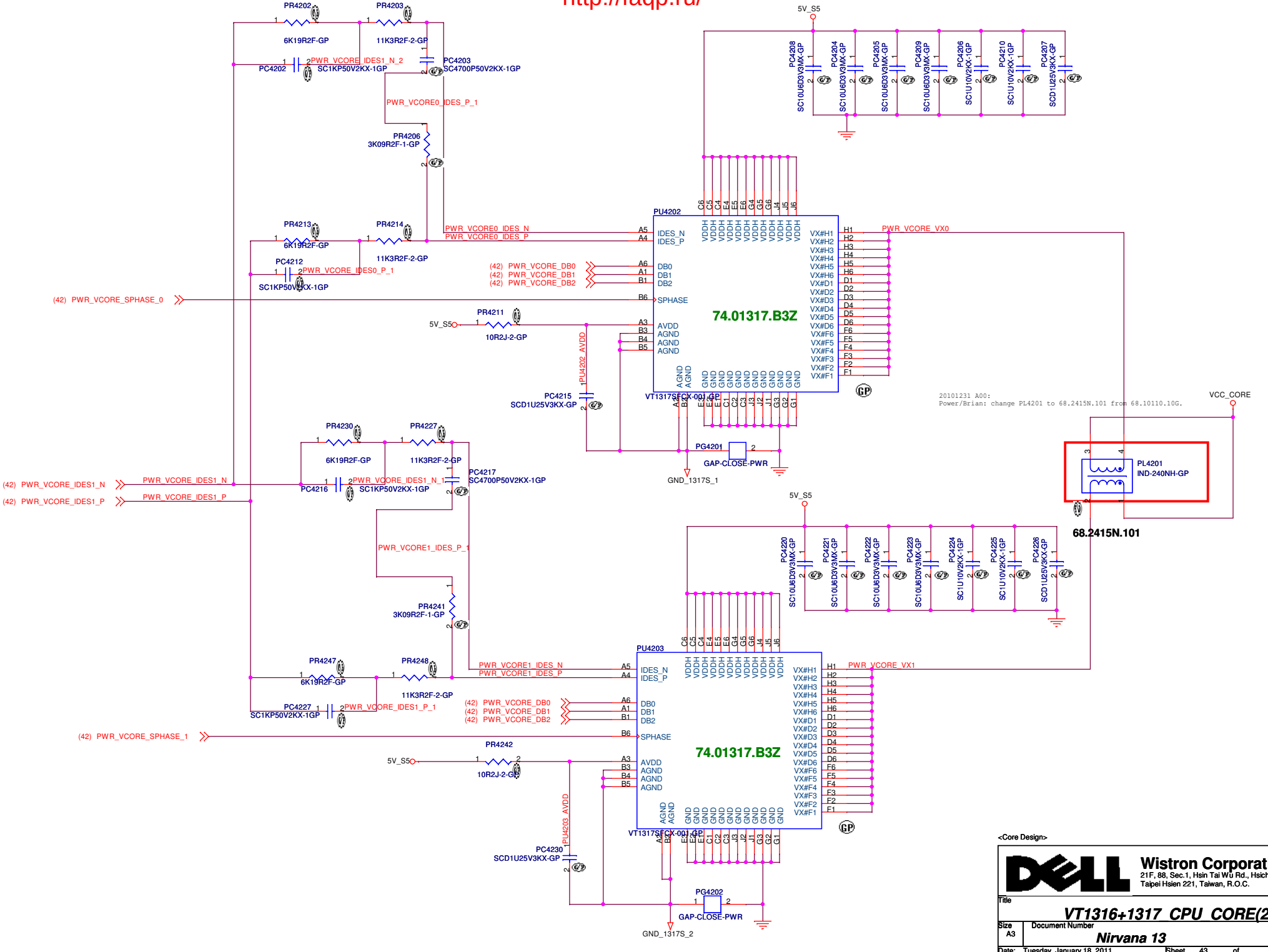
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317 CPU CORE(1/3)

Size: A3 | Document Number: Nirvana 13 | Rev: A00

Date: Tuesday, January 18, 2011 | Sheet 42 of 103



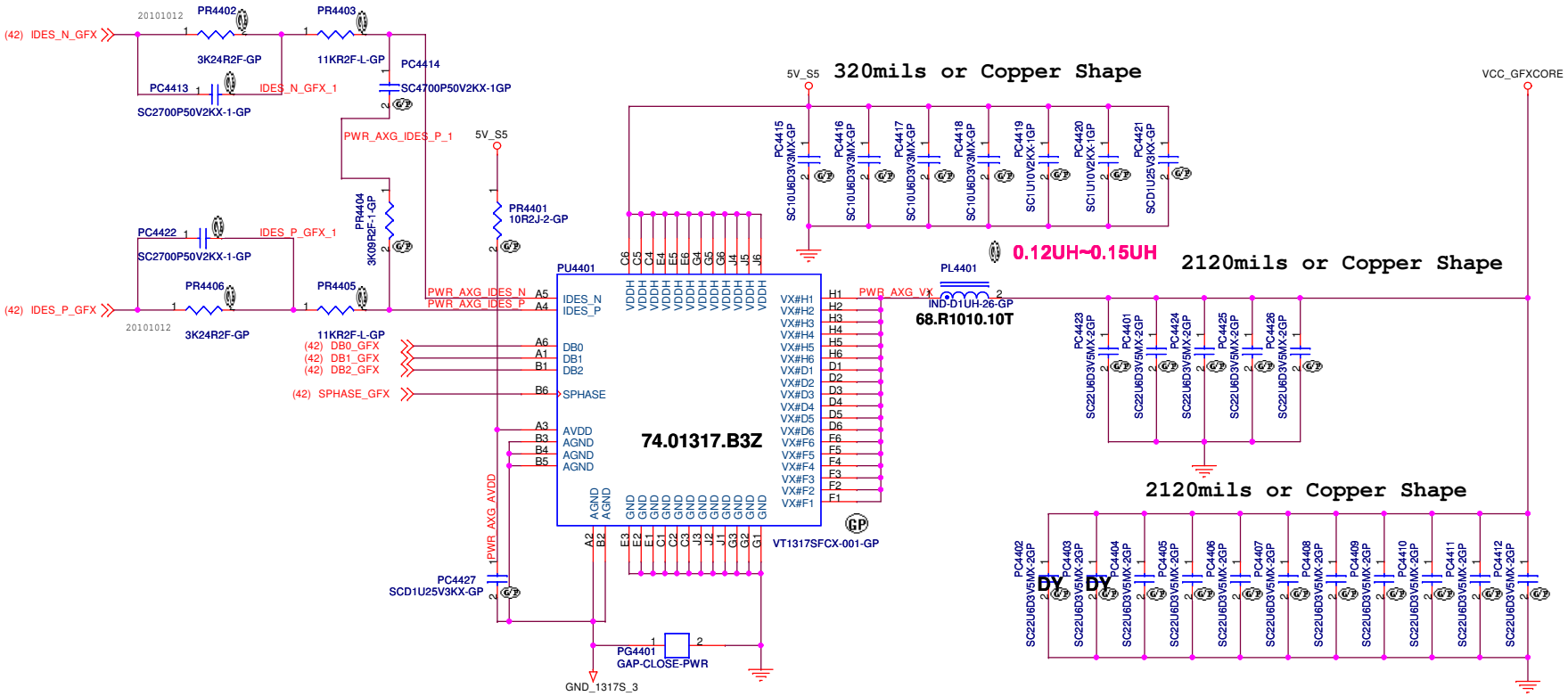
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317_CPU_CORE(2/3)

Size	Document Number	Rev
A3	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 43 of 103



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317_AXG_CORE(3/3)

Size: A3 | Document Number: Nirvana 13 | Rev: A00

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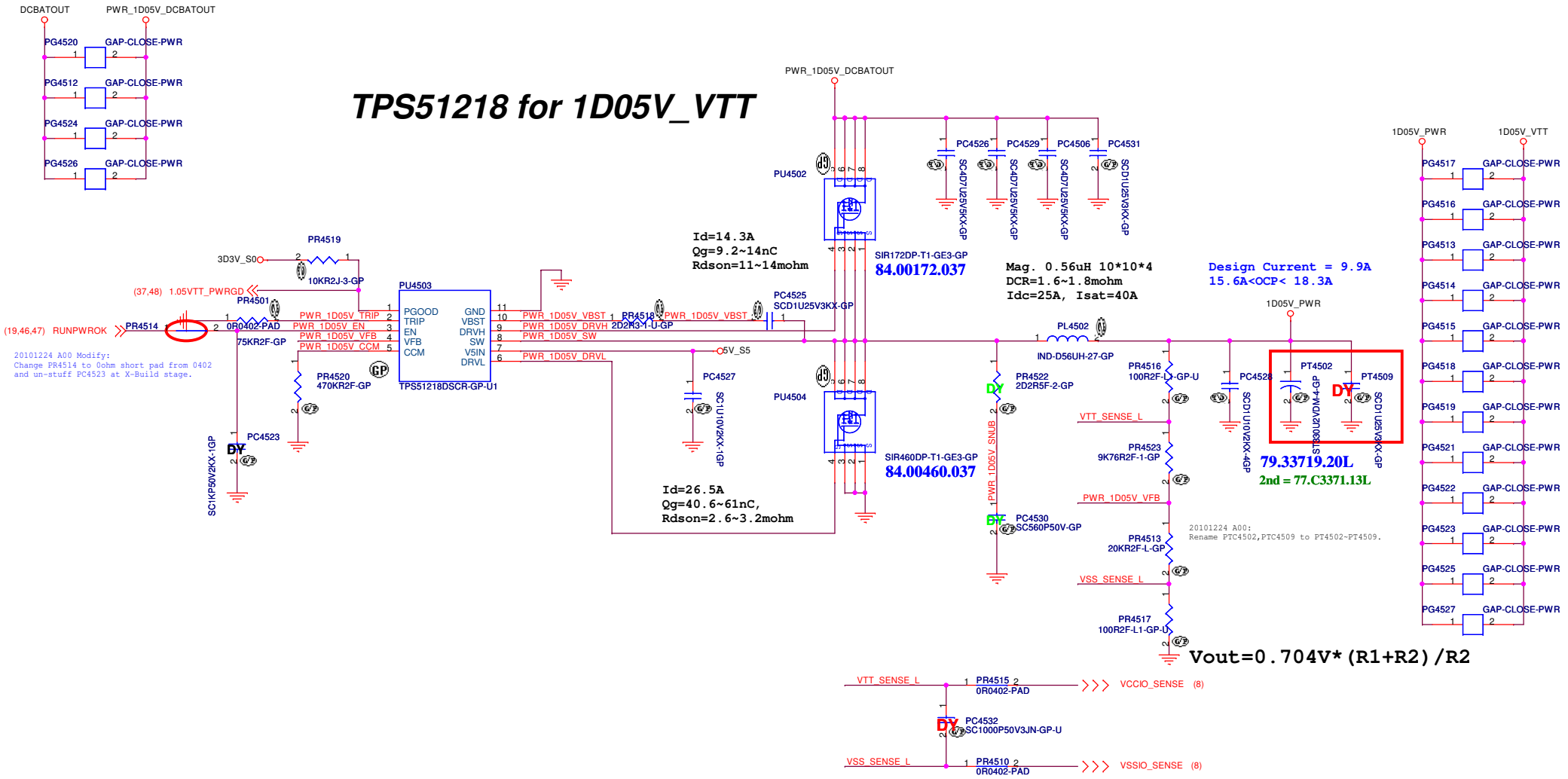
TPS51218 for 1D05V_VTT

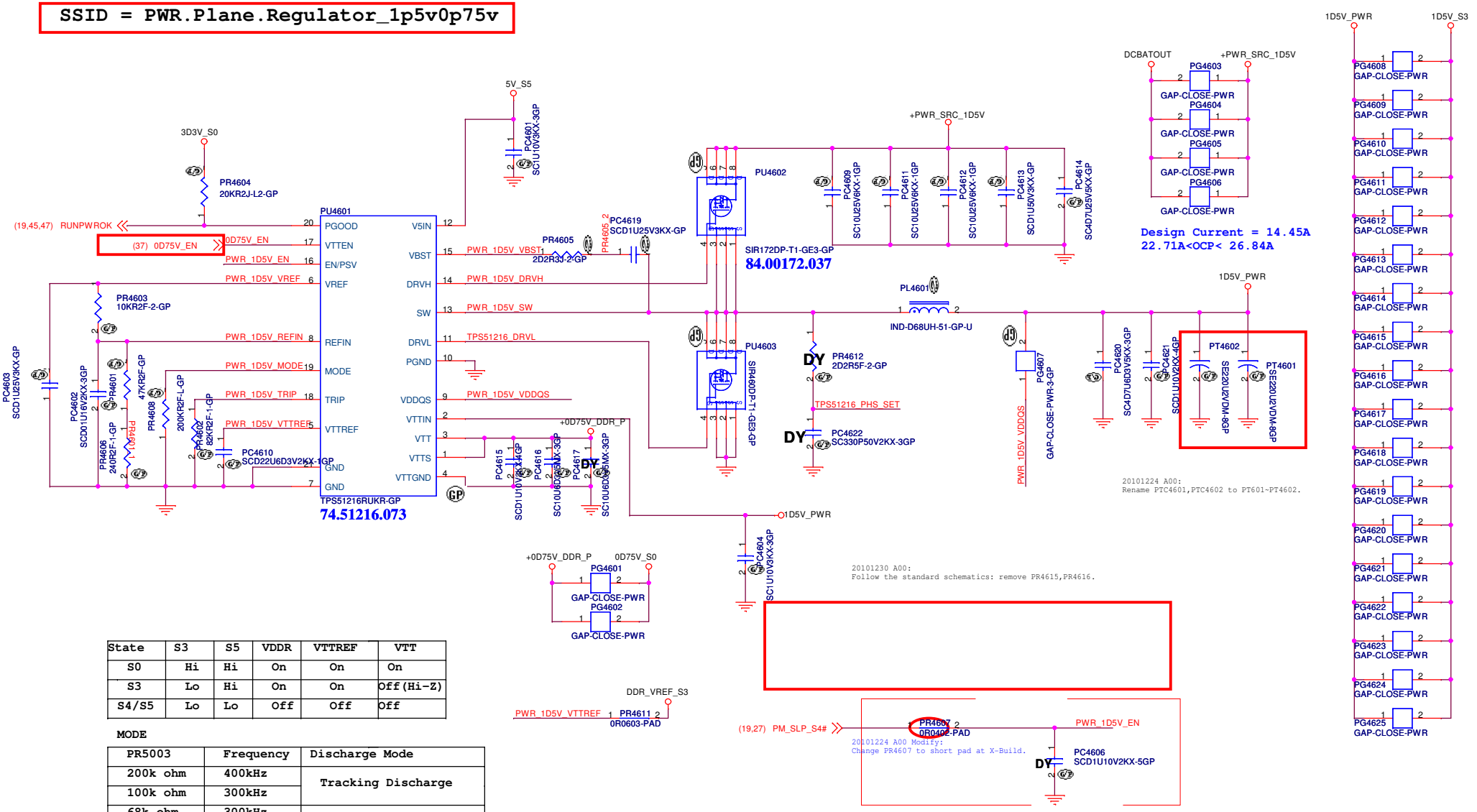


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51218_1D05V_VTT	
Size A3	Document Number Nirvana 13	Rev A00
Date: Tuesday, January 18, 2011	Sheet 45 of 103	

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR5003	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

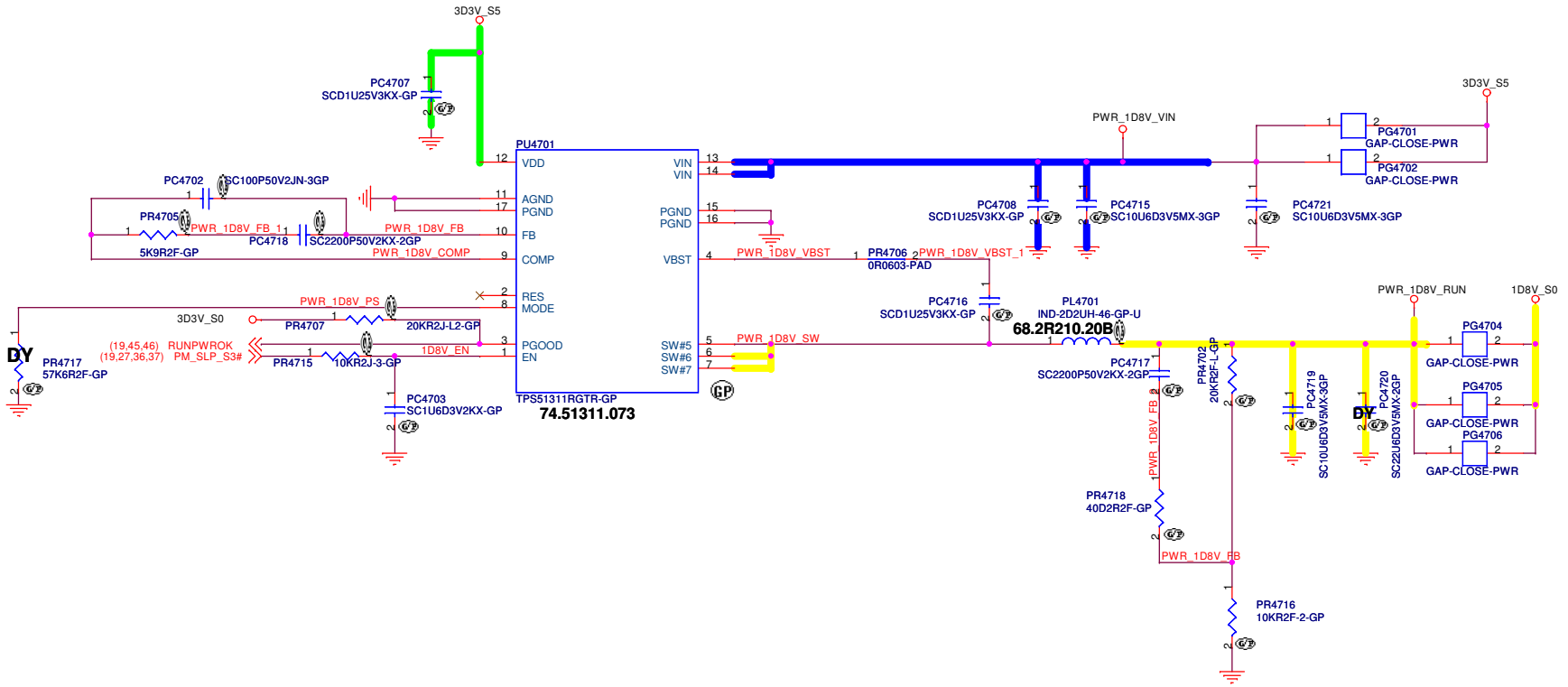
Title: TPS51116 +1.5V SUS

Size	Document Number	Rev
A3	Nirvana 13	A00

Date: Tuesday, January 18, 2011 Sheet 46 of 103

SSID = PWR.Plane.Regulator_1p8v

1A= 40mils
1.5A= 60mils
0.5A= 20mils



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51311_ +1.8V_RUN

Size	Document Number	Rev
A3	Nirvana 13	A00

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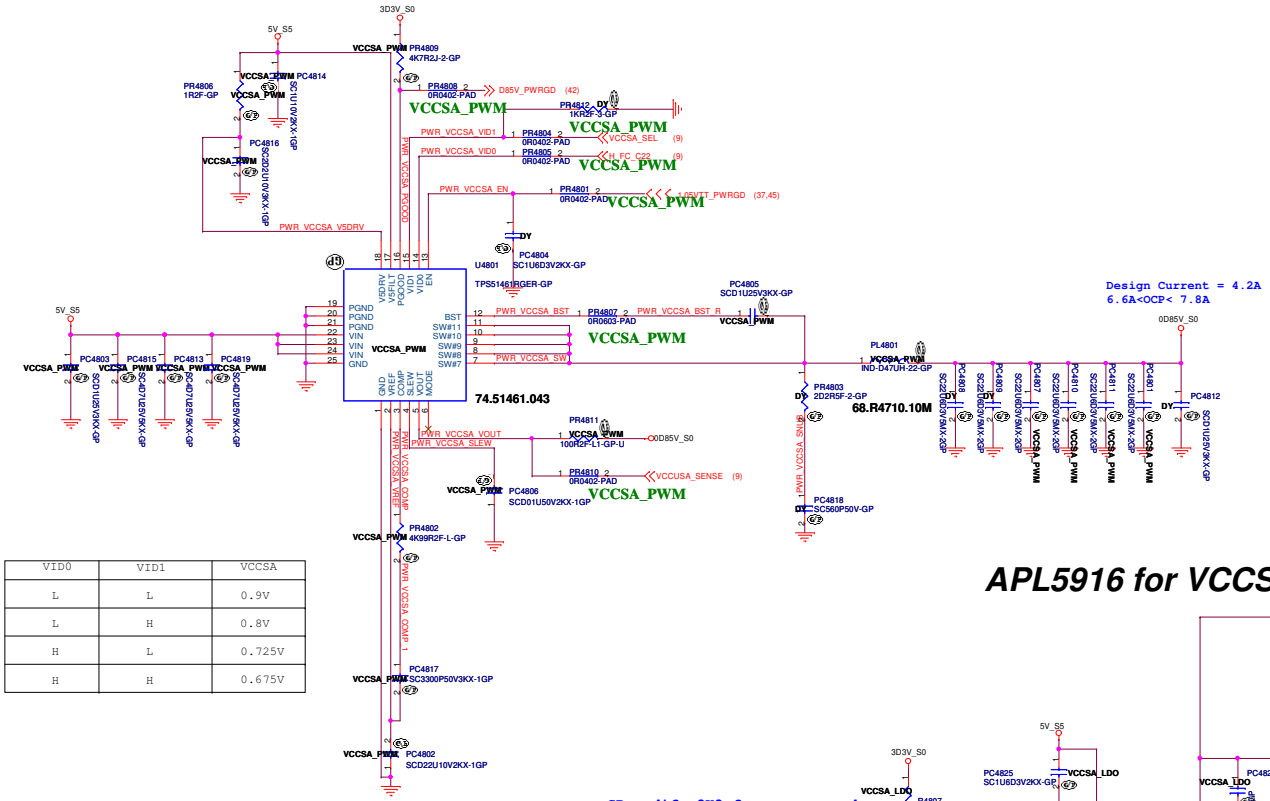
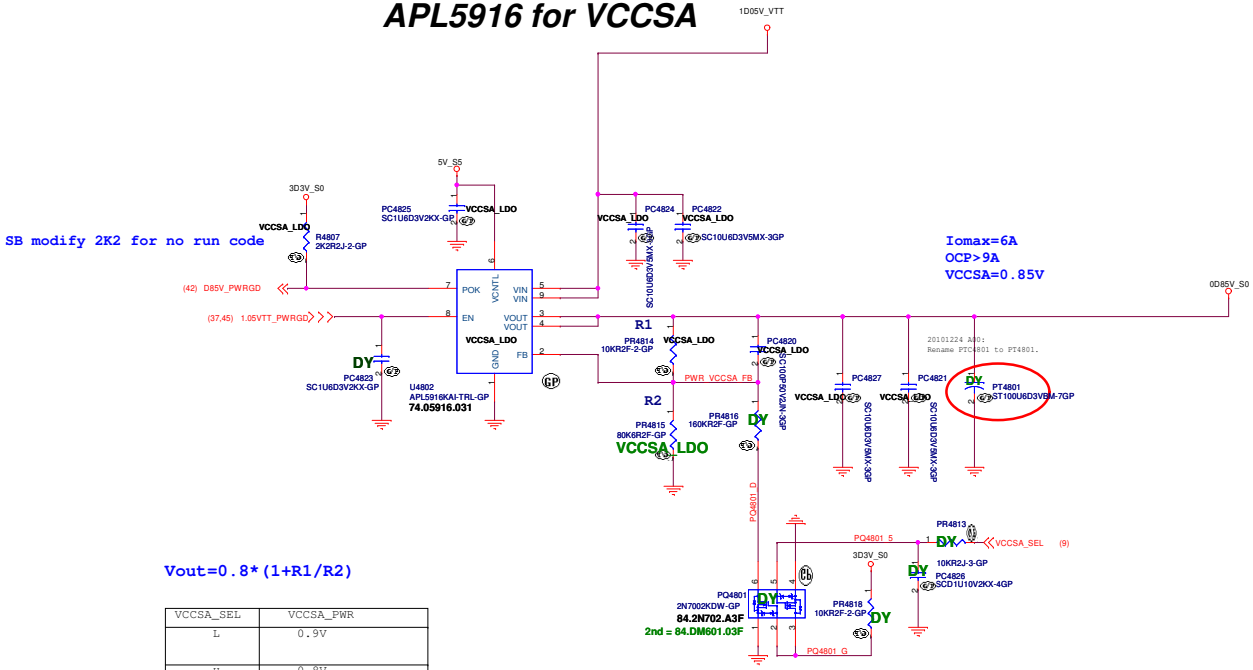
TPS51461 for VCCSA



VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

APL5916 for VCCSA



Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

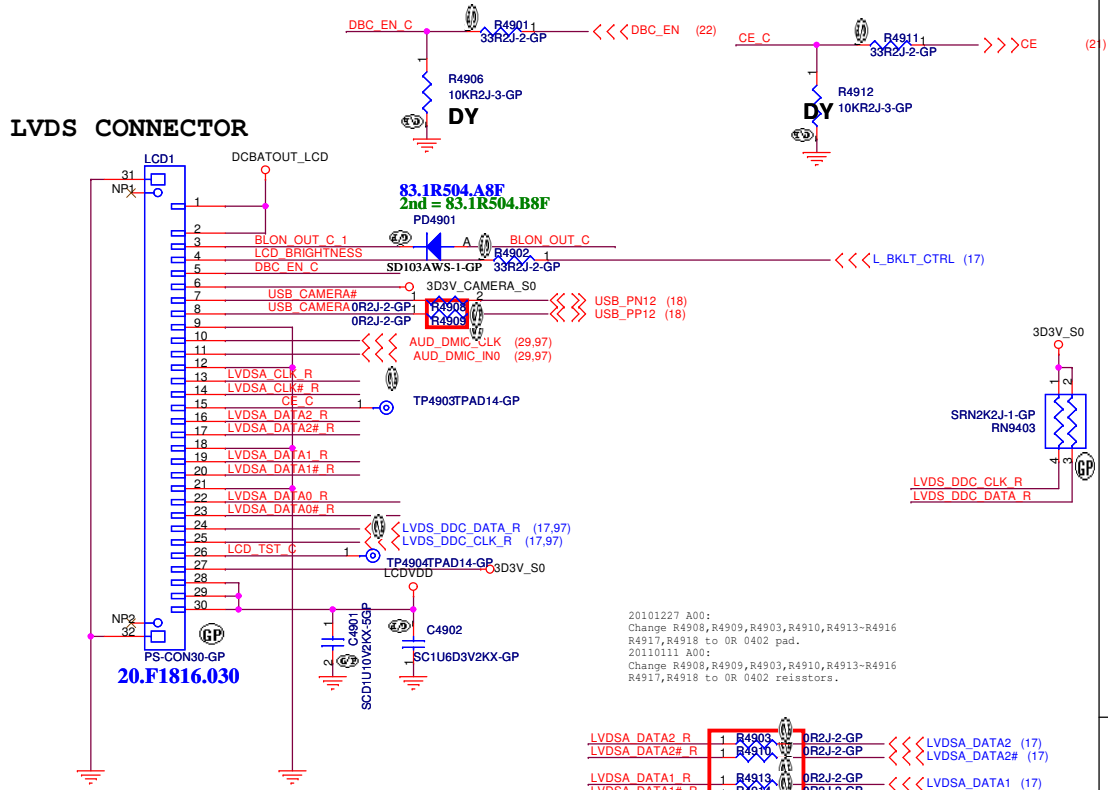
Title: TPS51461_VCCSA

Size: A2 | Document Number: Nirvana 13 | Rev: A00

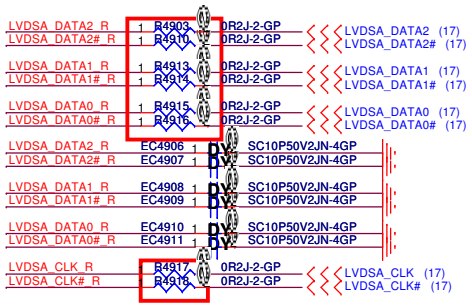
Date: Tuesday, January 18, 2011 | Sheet 48 of 103

SSID = VIDEO

LVDS CONNECTOR

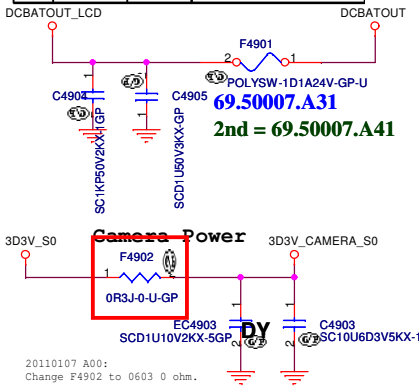


20101227 A00:
Change R4908,R4909,R4903,R4910,R4913~R4916
R4917,R4918 to 0R 0402 pad.
20110111 A00:
Change R4908,R4909,R4903,R4910,R4913~R4916
R4917,R4918 to 0R 0402 reisstors.



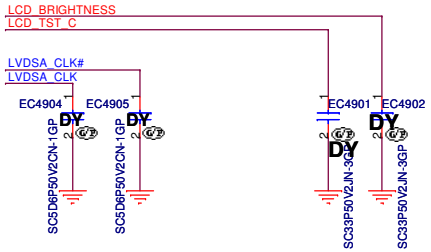
CAMERA and DIGITAL MIC PIN DEFINE!

Pin No.	Name	Pin Type	Function Description
1	Diag_Loop	PAD	Cable Connection Detection
2	D+	Data Pin	USB Data transmission
3	D-	Data Pin	USB Data transmission
4	USB+3.3V	Power Pin	Power Supply
5	DMIC_CLK	Data Pin	Digital MIC CLOCK
6	DIMC-GND	GND	Digital MIC GND
7	DIMC_DATA	Data Pin	Digital MIC DATA
8	GND	GND	System Ground



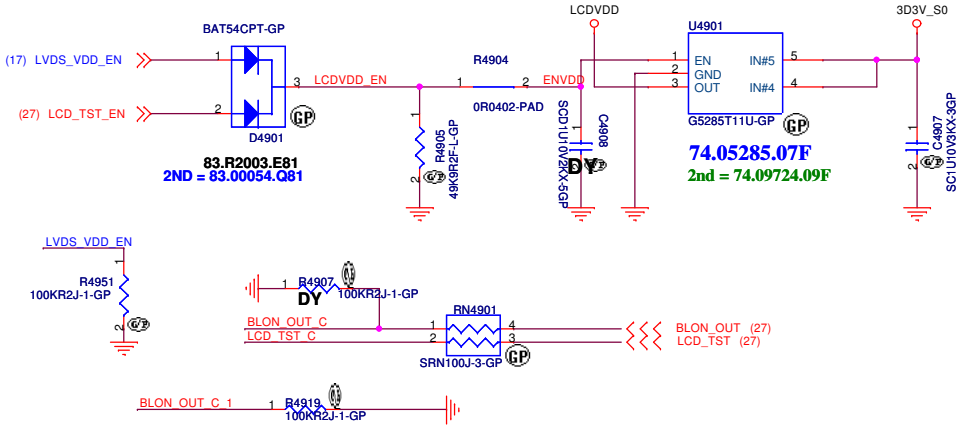
20110107 A00:
Change F4902 to 0603 0 ohm.

For EMI request
Close to LVDS connector



SSID = VIDEO

LCD POWER for ROSA



20100104 A00:
Remove TR4902.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size	Document Number	Rev
A3	Nirvana 13	A00

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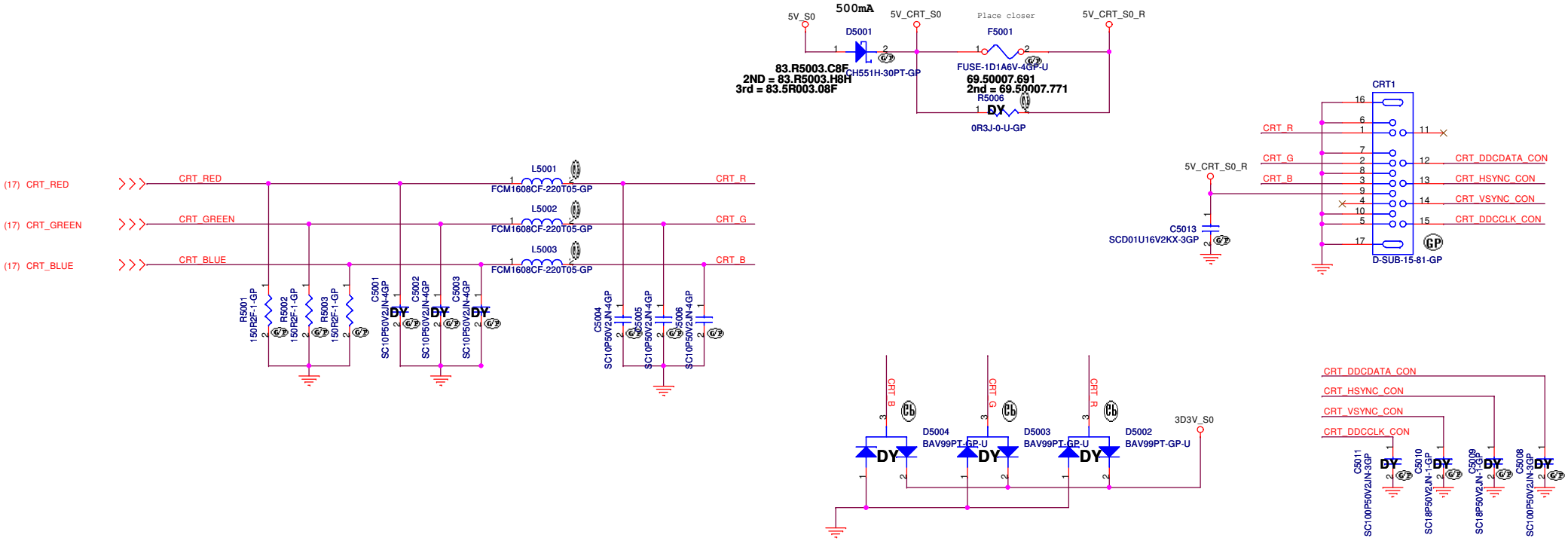
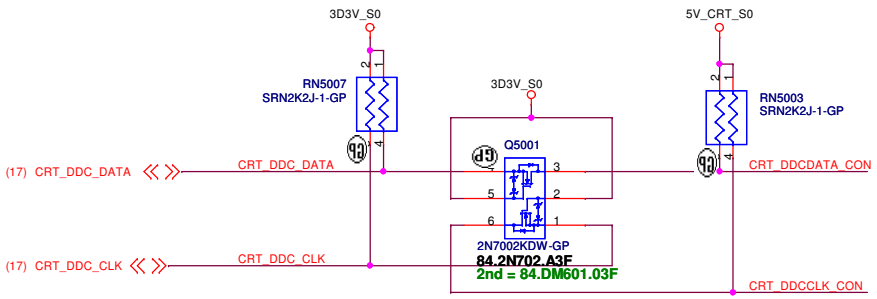
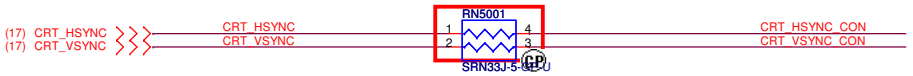


CRT DDCDATA & DDCCLK level shift



CRT Hsync & Vsync level shift



20101231 A00:
Change R5004,R5005 to RN5001 33 ohm array resistor.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Connector

Size	Document Number	Rev
A3	Nirvana 13	A00

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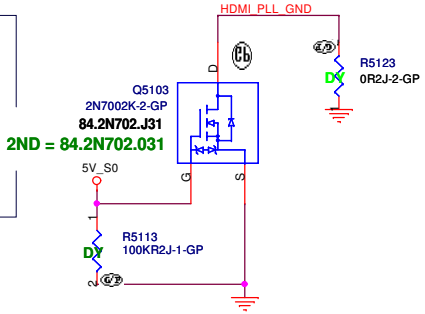
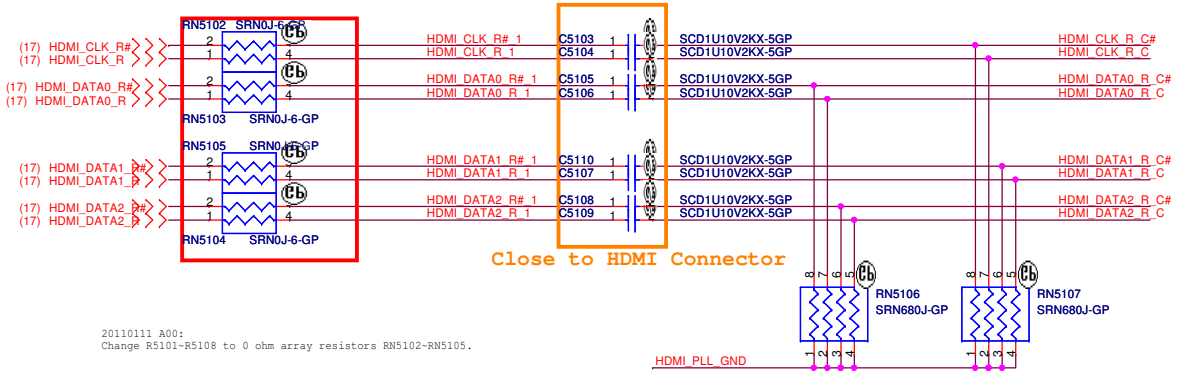
SSID = VIDEO

HDMI Level Shifter & CONNECTOR

Removed LEVEL SHIFTER base on DELL feedback spec.
(No support 220MHZ deep color mode, so can be removed
HDMI LEVEL SHIFTER circuit.





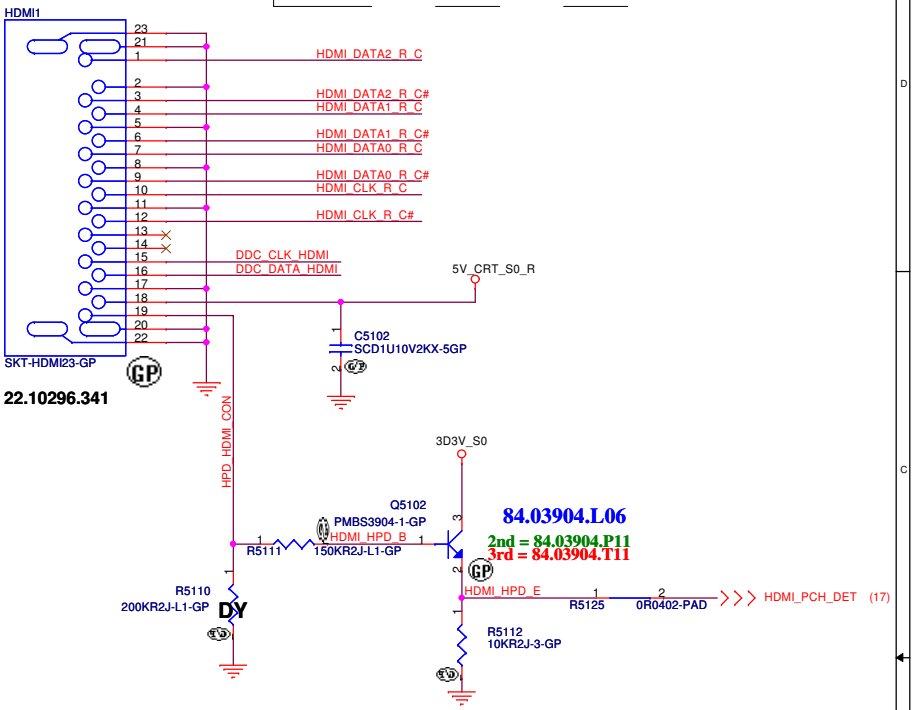
20110111 A00:
Change R5101~R5108 to 0 ohm array resistors RN5102~RN5105.

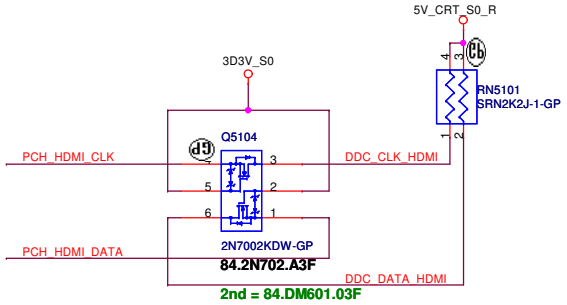
20100723 Swap RN5106 and RN5107 base in the swap report.

suggestion to stuff 680-ohm for UMA.

HDMI CONN

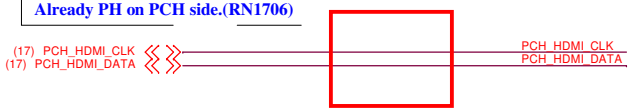
Removed HDMI_IN# CIRCUIT
connect to KBC GPIO.

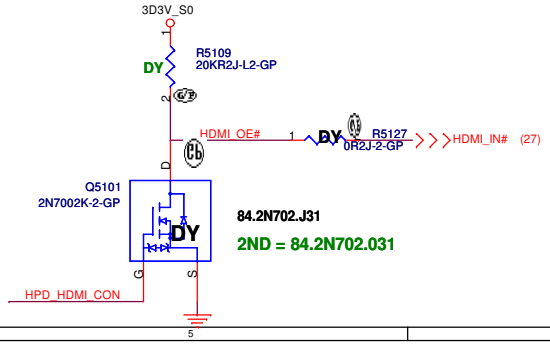




20101224 A00:
Change RN5117 to 0402 0 ohm pad.
20110111 A00:
Change RN5117 to 0 ohm resistor.
20110118 A00:
Remove RN5117 for PCH_HDMI_CLK and PCH_HDMI_DATA.

Already PH on PCH side.(RN1706)





Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

Wistron Corporation
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Title: HDMI Level Shifter/Connector
Size: A3 | Document Number: Nirvana 13 | Rev: A00
Date: Tuesday, January 18, 2011 | Sheet 51 of 103

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

Date: Wednesday, December 22, 2010 | Sheet 52 of 103

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch

Size: A3 | Document Number: Nirvana 13 | Rev: A00

Date: Wednesday, December 22, 2010 | Sheet 53 of 103

(Blanking)

<Core Design>

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Title: Reserved

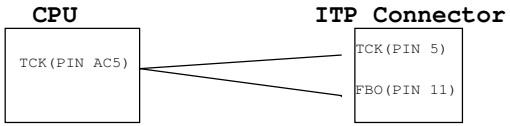
Size: A3 | Document Number: Nirvana 13 | Rev: A00

Date: Wednesday, December 22, 2010 | Sheet 54 of 103

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

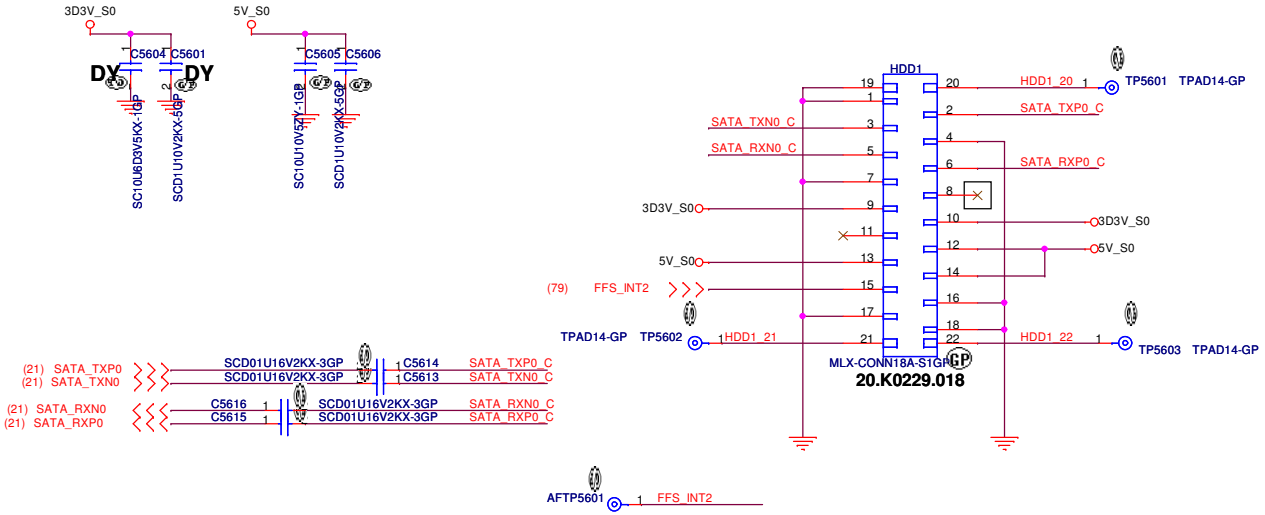
Title: ITP

Size: A3 | Document Number: Nirvana 13 | Rev: A00

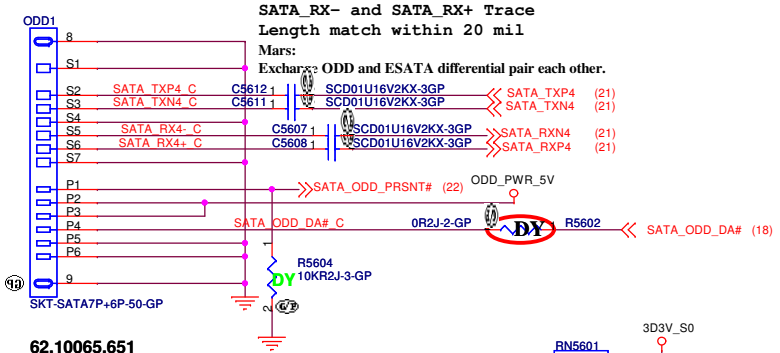
Date: Wednesday, December 22, 2010 | Sheet 55 of 103

SSID = SATA

SATA HDD Connector

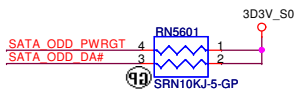


ODD Connector

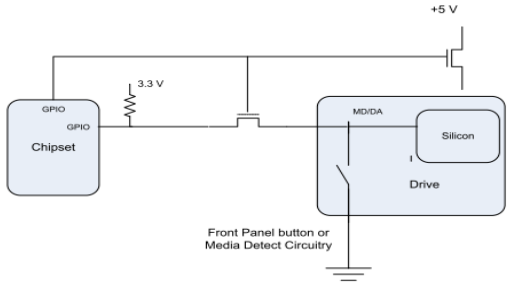


SATA_RX- and SATA_RX+ Trace Length match within 20 mil
Mars:
Exchange ODD and ESATA differential pair each other.

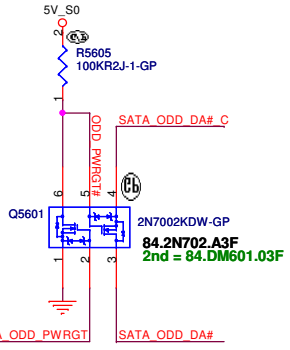
62.10065.651
2nd = 62.10065.221



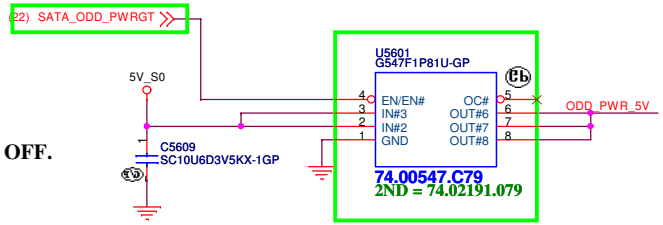
SUPPORT ZERO SATA ODD



When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON



SATA Zero Power ODD



Current limit
Active High
typ =>2A

<Core Design>

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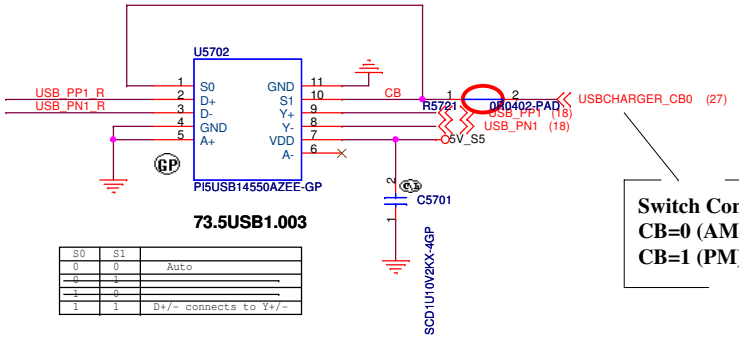
Title	HDD/ODD	
Size A3	Document Number Nirvana 13	Rev A00
Date: Tuesday, January 18, 2011	Sheet 56 of 103	

SSID = ESATA

USB CHARGER

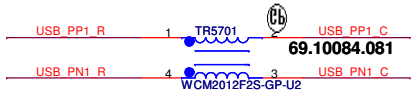


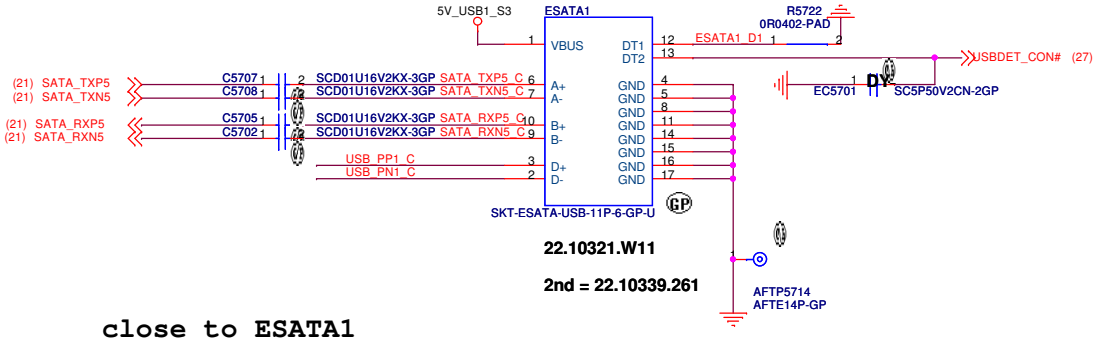
S0	S1	
0	0	Auto
0	1	
1	0	
1	1	D+/- connects to Y+/-

Switch Control Bit:
CB=0 (AM):auto detection charger identification active.
CB=1 (PM):connect DP/DM to TDP/TDM.

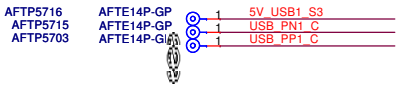
ESATA CONN

20100104 A00:
Remove R5718,R5719





close to ESATA1



<Core Design>

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Title		
USB/ESATA		
Size: A3	Document Number: Nirvana 13	Rev: A00
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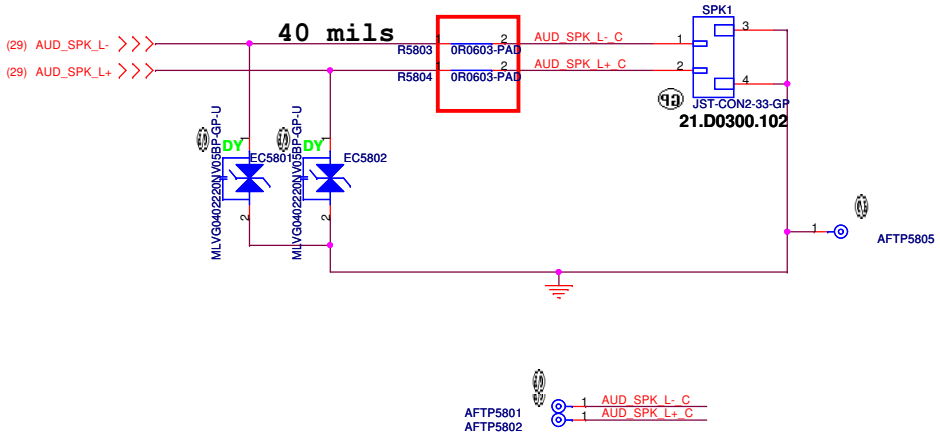
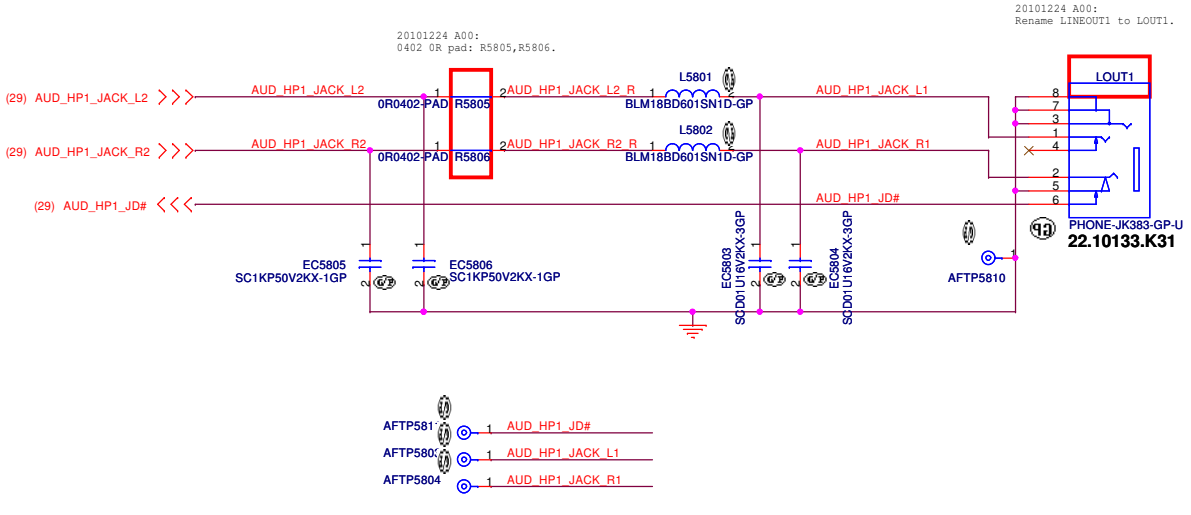
SSID = AUDIO

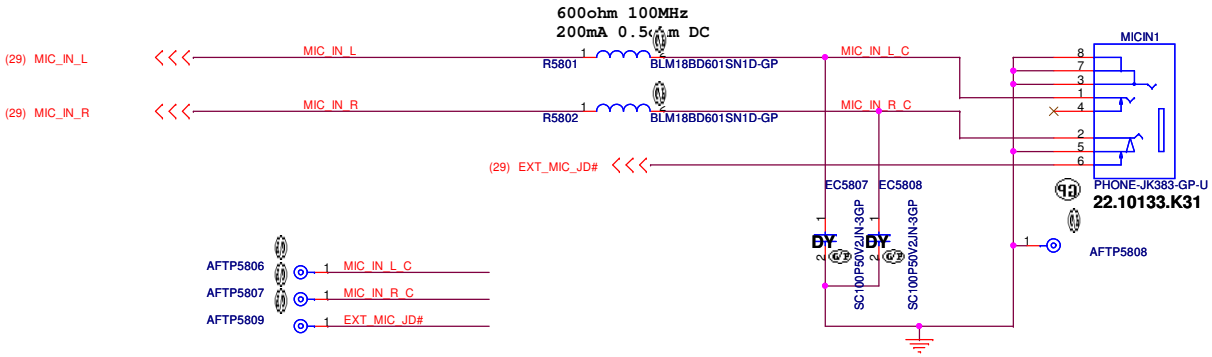
Speaker Connector



LINE OUT



MIC IN



<Core Design>

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Title: Audio Jack		
Size: A3	Document Number: Nirvana 13	Rev: A00
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<Core Design>

Wistron Corporation
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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

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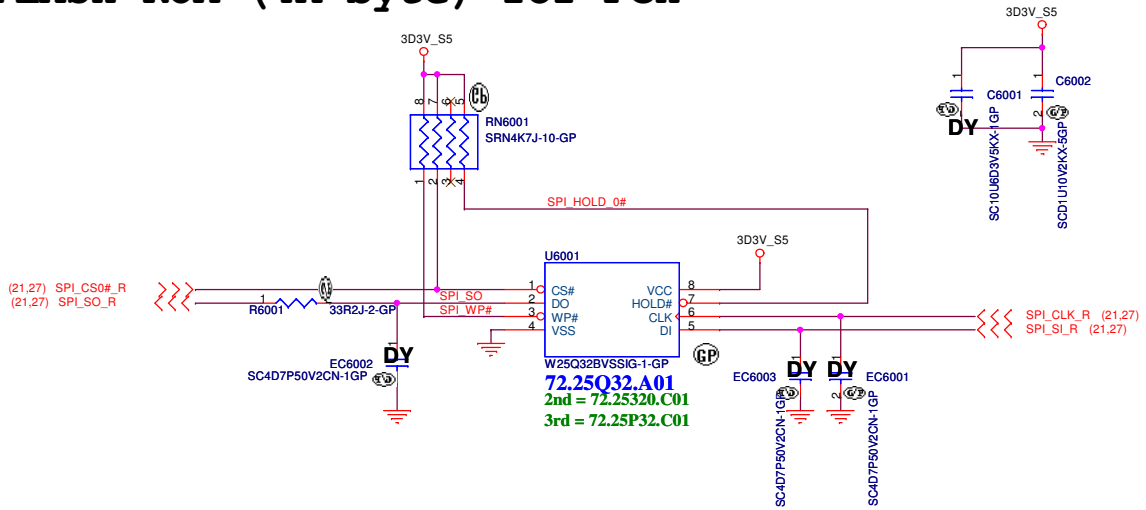
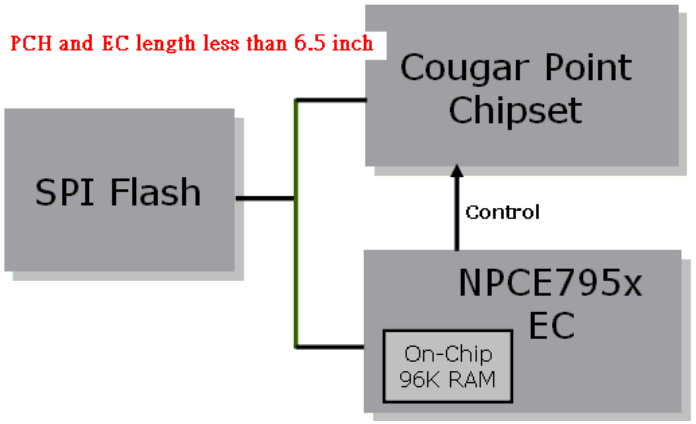
SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH

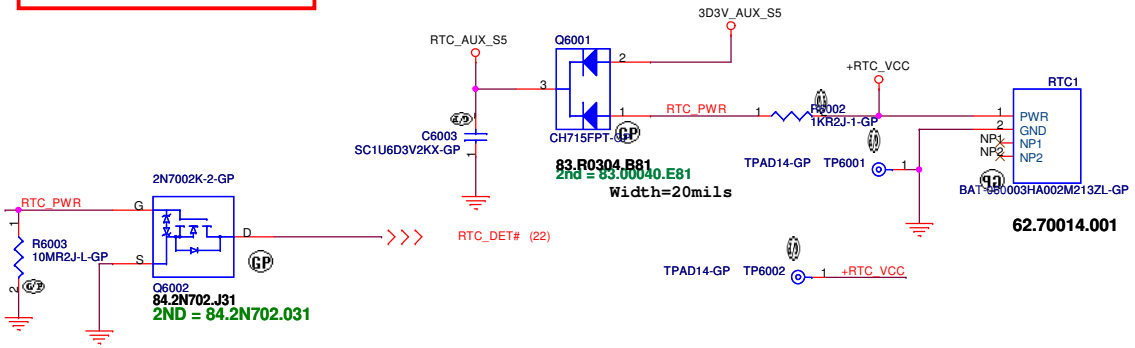


Priority	Wistron P/N	Manufacturer	Vendor P/N
1	72.25Q32.A01	WINDBOND	W25Q32BVSSIG
2	72.25320.C01	MXIC	MX25L3206EM2I-12G
3	72.25P32.C01	NUMONYX	M25PX32-VMW6F

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil



SSID = RBATT



<Core Design>

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Title		
Flash/RTC		
Size: A3	Document Number: Nirvana 13	Rev: A00
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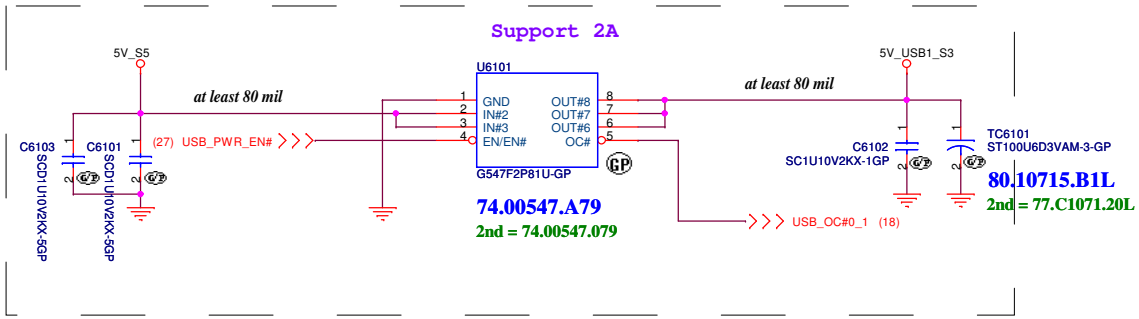
SSID = USB

Close to ESATA Combo connector

Support 2A

USB POWER SW
Main G547F2P81U-GP P/N:74.00547.A79



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB2.0 Power SW		
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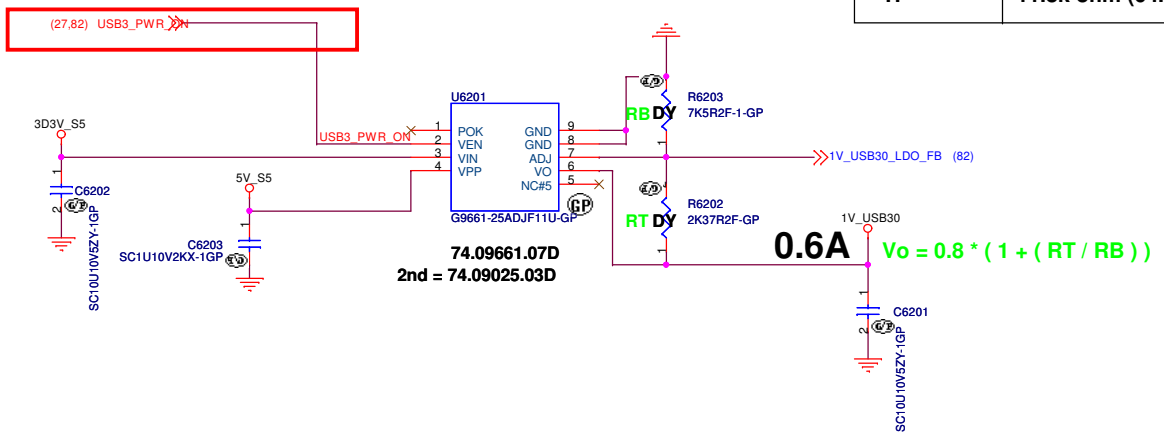
1V_USB30 LDO

```
20101227 A00:
Change R6205 to 0R 0402 pad.
20101228 A00:
VGA_THRM change to USB_PWR_EN.
20101229 A00:
Remove R6205,R6201 and rename USB3_PWR_ON from USB_PWR_EN.
```

USB3.0 Host	RT (R6202)	RB (R6203)	VOUT
NEC	2.37k ohm (64.23715.6DL)	7.5k ohm (64.75015.6DL)	1.05V
TI	11.8k ohm (64.11825.6DL)	30.9k ohm (64.30925.6DL)	1.1V



<Core Design>

Wistron Corporation
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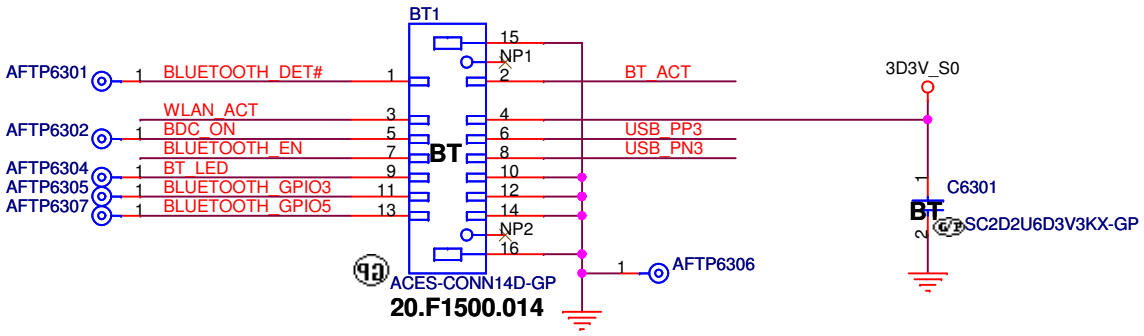
Title: USB 3.0 Port

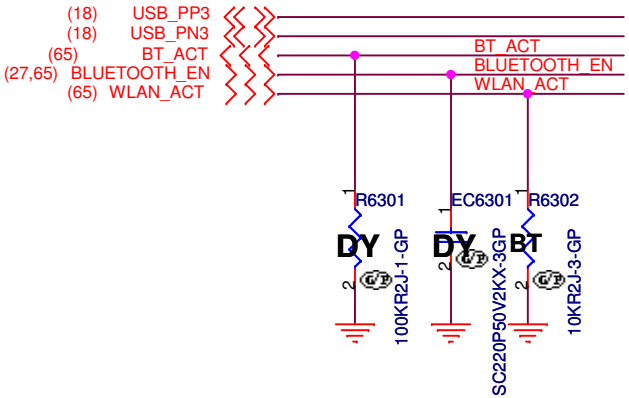
Size: A3 | Document Number: Nirvana 13 | Rev: A00

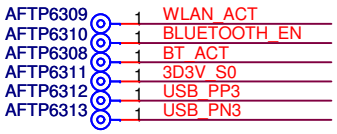
Date: Tuesday, January 18, 2011 | Sheet 62 of 103

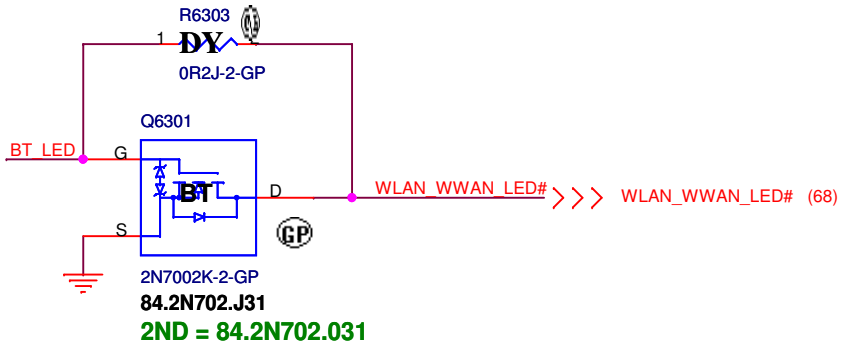
SSID = User.Interface

Bluetooth Module









<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Bluetooth		
Size: A4	Document Number: Nirvana 13	Rev: A00
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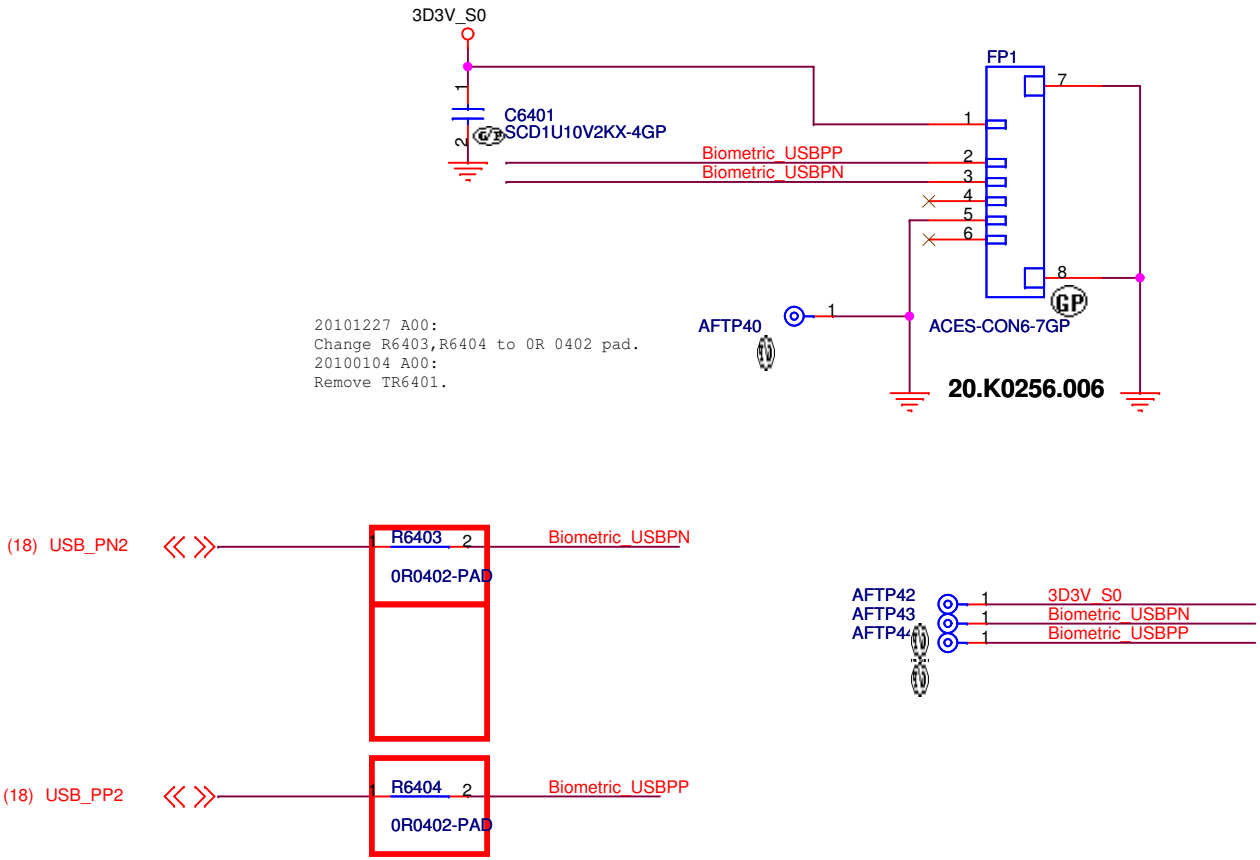

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Finger Printer Conn***

Size	Document Number	Rev
A4	***Nirvana 13***	***A00***

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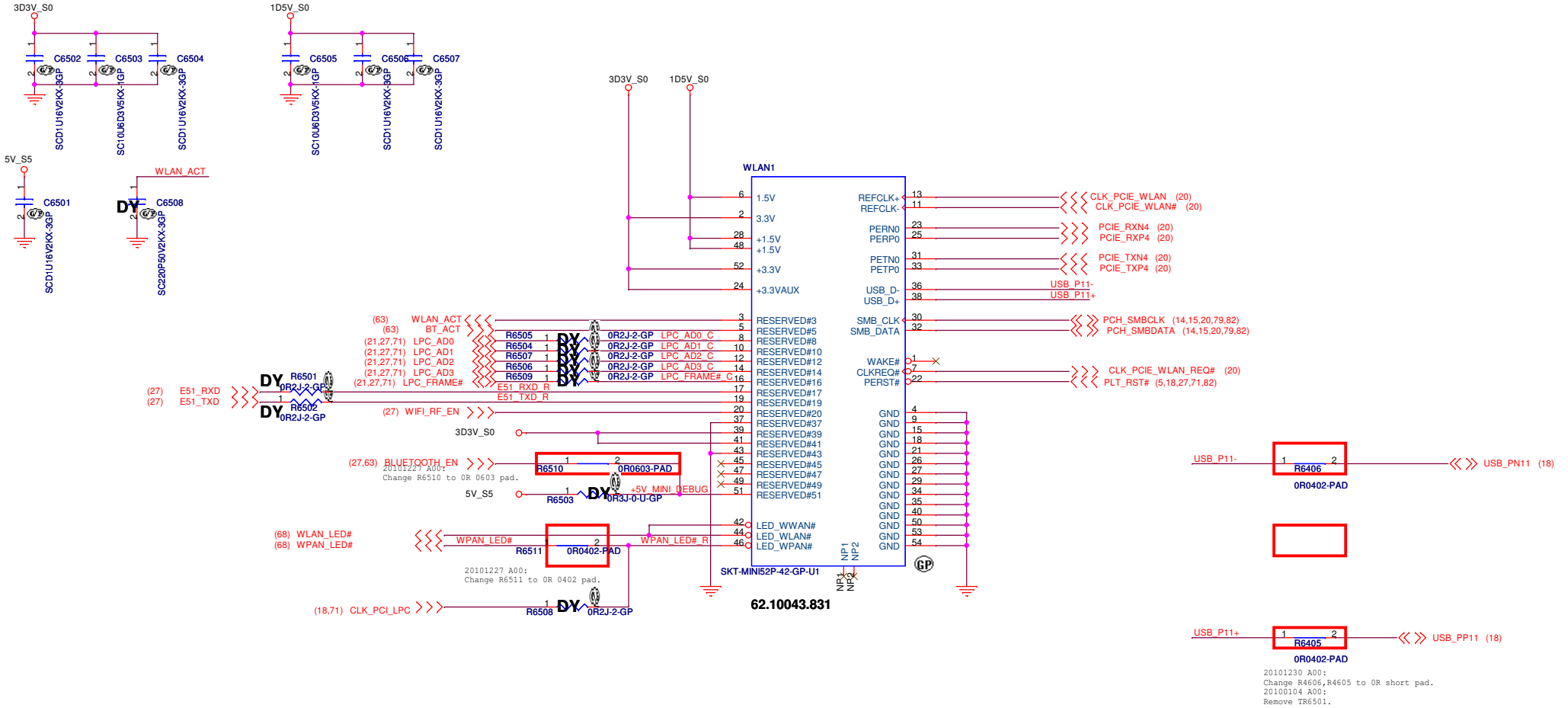
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



20101227 A00:
Change R6510 to 0R 0603 pad.

20101227 A00:
Change R6511 to 0R 0402 pad.

20101230 A00:
Change R4606,R4605 to 0R short pad.
20100104 A00:
Remove TR6501.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***MINICARD(WLAN)/ITP CONN***	
Size: A3	Document Number: ***Nirvana 13***	Rev: ***A00***
Date: Tuesday, January 18, 2011	Sheet 65 of 103	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Reserved

Size	Document Number	Rev
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SSID = User.Interface

Power LED(White)

20110103 A00:
Change R6804,R6806,R6808,R6810 to 620 ohm 5%.
20100106 A00:
Change R6804,R6806,R6808,R6810 to 1k ohm 5%.

Q6801 PDTA143ET-GP
5V_S5
PWRLED# C
LED_PWR
EC6801 SC220P50V2KX-3GP
R6804 1KR2J-1-GP → PWR LED B
R6807 1KR2J-1-GP → POWER_SW_LED_B
84.00143.M11
2nd = 84.02143.011
3rd = 84.00143.N11

20110103 A00:
Change R6801 to 1k.

LED BD Connector

LEDBD1 ACES-CON6-13-GP
20.K0320.006
PWR_LED_B
SATA_LED
BAT_WHITE
BAT_AMBER
LED_WLAN_OUT_B

SATA HDD LED(White)

Q6802 PDTA143ET-GP
5V_S0
SATA_LED# C
SATA_LED_R
R6805 1KR2J-1-GP → SATA_LED
EC6805 SC220P50V2KX-3GP
84.00143.M11
2nd = 84.02143.011
3rd = 84.00143.N11

RN6801 SRN15KJ-2-GP
(27) PWRLED# → PWRLED# C
(27) BATT_WHITE_LED# → WHITE_LED_BAT#
(27) CHG_AMBER_LED# → AMBER_LED_BAT#
(21) SATA_LED# → SATA_LED# C

Battery LED1(White)

Q6805 PDTA143ET-GP
5V_AUX_S5
WHITE_LED_BAT#
WHITE_LED_BAT
R6808 1KR2J-1-GP → BAT_WHITE
EC6804 SC220P50V2KX-3GP
84.00143.M11
2nd = 84.02143.011
3rd = 84.00143.N11

AFTP6801 1PWR_LED_B
AFTP6802 1SATA_LED
AFTP6803 1BAT_WHITE
AFTP6804 1BAT_AMBER
AFTP6805 1LED_WLAN_OUT_B
AFTP6806 1 KBC_PWRBTN# C
AFTP6807 1 POWER_SW_LED_B

Battery LED2(Amber)

Q6804 PDTA143ET-GP
5V_AUX_S5
AMBER_LED_BAT#
AMBER_LED_BAT
R6809 390R2J-1-GP → BAT_AMBER
EC6802 SC220P50V2KX-3GP
84.00143.M11
2nd = 84.02143.011
3rd = 84.00143.N11

(63) WLAN_WWAN_LED → WLAN_WWAN_LED#
3D3V_S0
R6805 100KR2J-1-GP
U6801 83.BAT54.U81 BAT54A-5-GP
(65) WLAN_LED#
(82) WWAN_LED#
(65) WPAN_LED#
D6801 BAS16-6-GP
83.00016.K11
2ND = 83.00016.F11
WLAN_WWAN_LED#
R6802 15KR2J-1-GP
LED_WLAN_OUT_R#

WLAN LED (White)

Q6803 PDTA143ET-GP
5V_S0
WLAN_LED
R6810 1KR2J-1-GP → LED_WLAN_OUT_B
EC6803 SC220P50V2KX-3GP
84.00143.M11
2nd = 84.02143.011
3rd = 84.00143.N11

TPLOCK LED

(27) TP_LOCK_LED#
R6807 15KR2J-1-GP
Q6804_B
Q6812 PDTA143ET-GP
5V_S0
TP_LOCK_LED_B
R6813 390R2J-1-GP
TP_LOCK_LED_A
LED1 LED-Y-57-GP 83.01921.P70
EC6804 SC220P50V2KX-3GP
84.00143.M11
2nd = 84.02143.011
3rd = 84.00143.N11

Need change to LOW actived from KBC GPIO

Power button LED(White)

20101224 A00:
Rename PWRBTN1 to PWRBT1.

(27) KBC_PWRBTN#
R6803 100R2J-2-GP
KBC_PWRBTN# C
POWER_SW_LED_B
PWRBT1 ACES-CON4-10-GP-U
20.K0320.004
EC6806 SCD1U10V2KX-3GP
EC6807 SCD1U10V2KX-3GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED Bord/Power Button
Size: A2
Document Number: Nirvana 13
Rev: A00
Date: Tuesday, January 18, 2011
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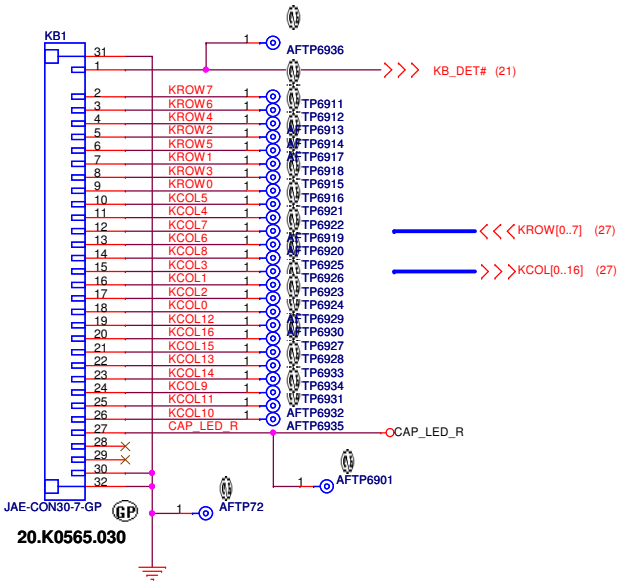
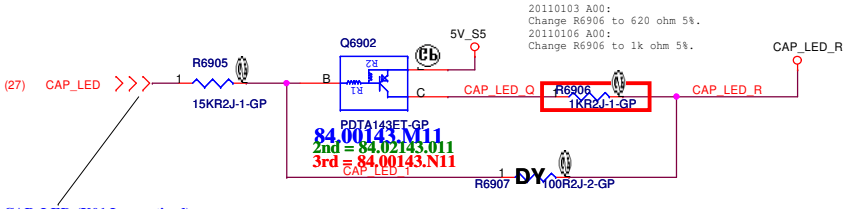
SSID = KBC

Internal KeyBoard Connector

PIN No.	Description
1	Diag_Loop=GPIO_1(TPC)
2	KSI[7] = KBD S8
3	KSI[6] = KBD S7
4	KSI[4] = KBD S5
5	KSI[2] = KBD S3
6	KSI[5] = KBD S6
7	KSI[1] = KBD S2
8	KSI[3] = KBD S4
9	KSI[0] = KBD S1
10	KSO[5] = KBD D6
11	KSO[4] = KBD D5
12	KSO[7] = KBD D8
13	KSO[6] = KBD D7
14	KSO[8] = KBD D9
15	KSO[3] = KBD D4
16	KSO[1] = KBD D2
17	KSO[2] = KBD D3
18	KSO[0] = KBD D1
19	KSO[12] = KBD D13
20	KSO[16] = KBD D17
21	KSO[15] = KBD D16
22	KSO[13] = KBD D14
23	KSO[14] = KBD D15
24	KSO[9] = KBD D10
25	KSO[11] = KBD D12
26	KSO[10] = KBD D11
27	CapsLock LED
28	N/C
29	N/C
30	GND

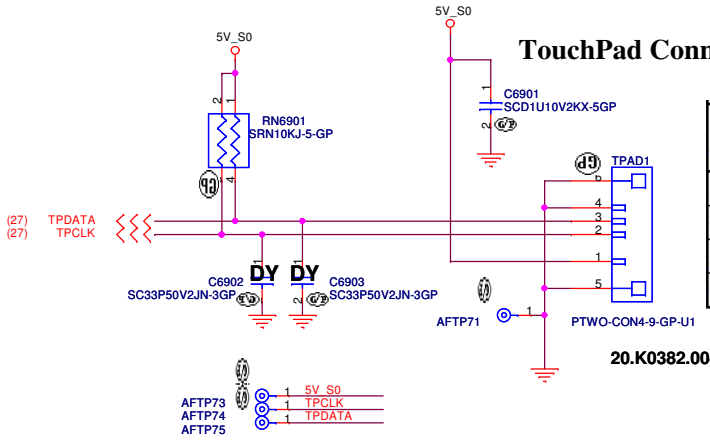


CAP LED CONTROL



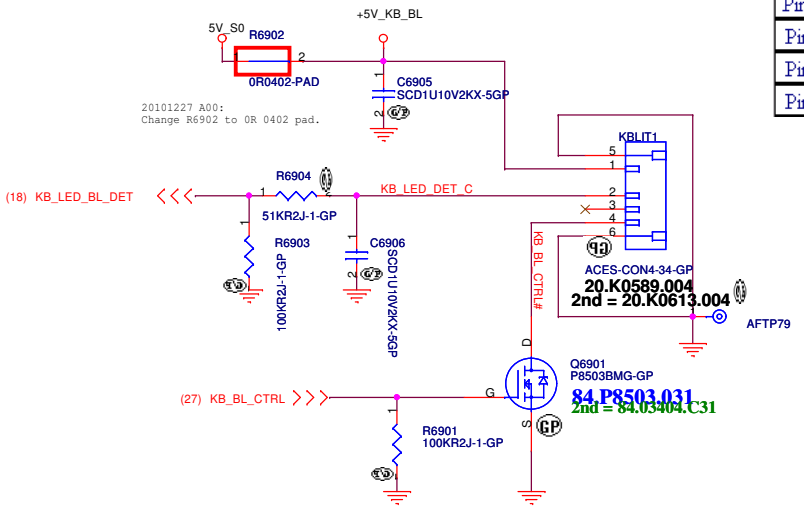
TouchPad LOCKED

TouchPad Connector

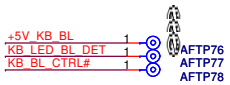


Touch Pad CN1 CONN. (FFC)	
Pin 1	5V_S0
Pin 2	TPCLK
Pin 3	TPDATA
Pin 4	GND

KB Backlight Connector



MB CONN. (FFC)	
Pin 1	+5V_KB_BL
Pin2	KB_LED_DET_C
Pin3	NC
Pin4	KB_BL_CTRL#



<Core Design>

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Title: Key Board/Touch Pad/Media Board

Size	Document Number	Rev
A3	Nirvana 13	A00

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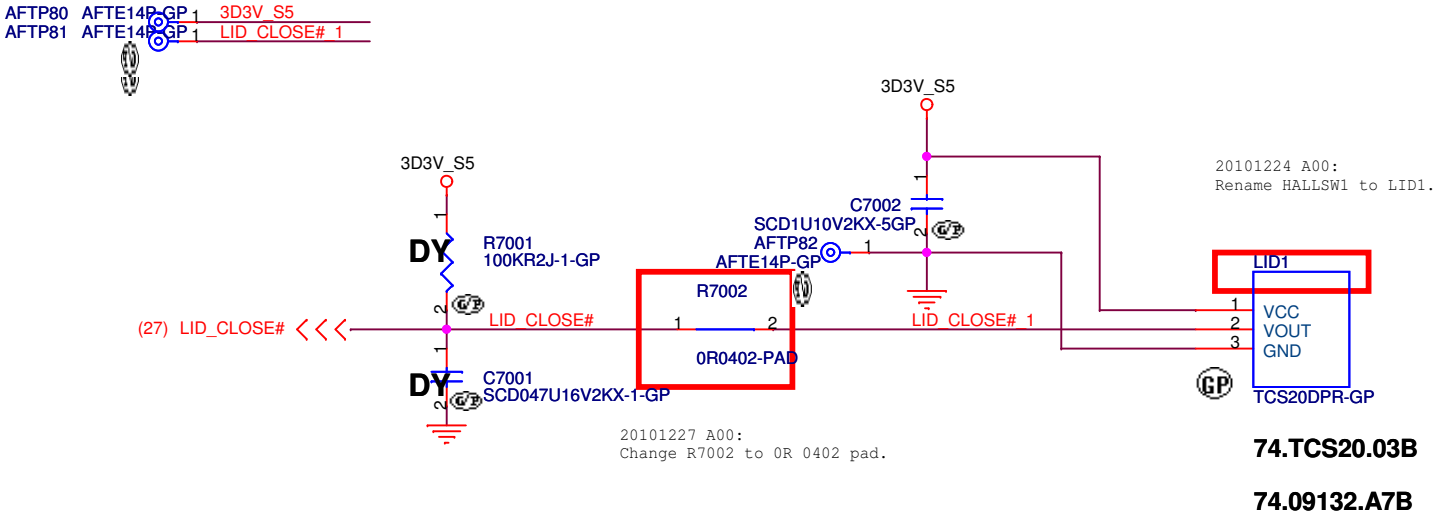

<Core Design>

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Title: ***Hall Sensor***

Size	Document Number	Rev
A4	***Nirvana 13***	***A00***

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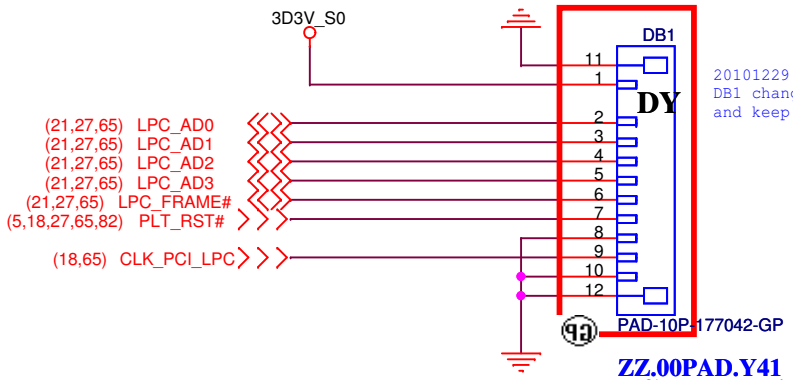

20101229 A00 Modify:
DB1 change to ZZ.00PAD.Y41(solder mask type)
and keep un-stuff at X-Build stage.

ZZ.00PAD.Y41
PCB Footprint = PAD-10P-177042

<Core Design>

Wistron Corporation
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Title: ***Dubug CONN***

Size	Document Number	Rev
A4	***Nirvana 13***	***A00***

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *Nirvana 13* | Rev: *A00*

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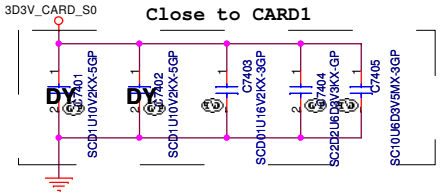
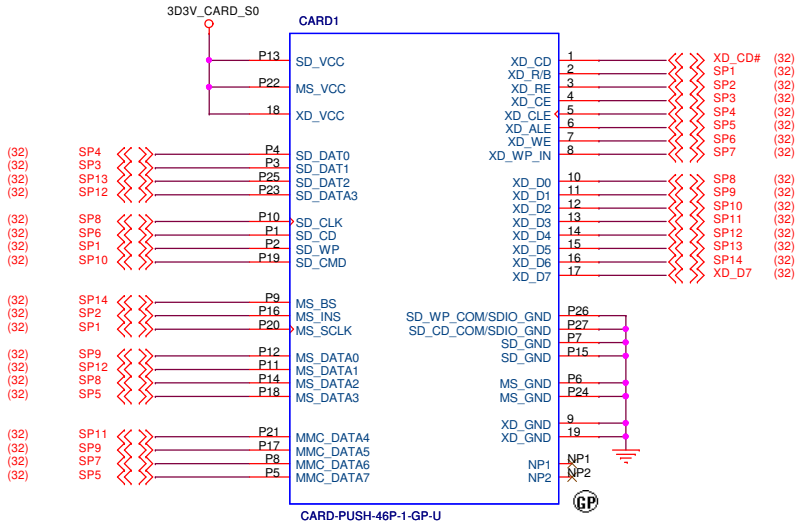
SSID = SDIO



SD/XD/MS/MMC+ Card Reader

WITHOUT CARD	WP, CD, GND
CARD INSERTED WP—SW:LOCK	WP, CD, GND
CARD INSERTED WP—SW:UNLOCK	WP, CD, GND

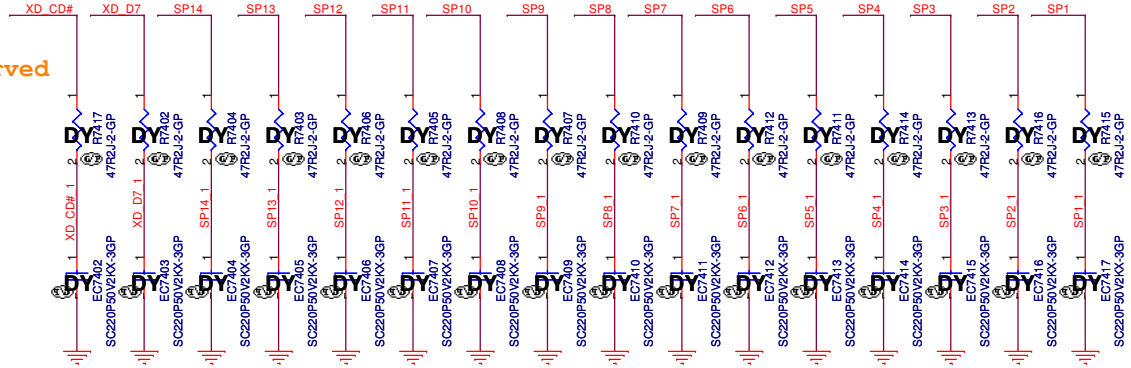


20.I0129.001

2nd = 20.I0135.001

PIN	TYPE	FUNCTION	RTS5138 NET
1	SD	SD-DAT2	SP13
2	SD	SD-CD/DAT3	SP12
3	MMC_PLUS	MMC-DAT4	SP11
4	SD	SD-CMD	SP10
5	MMC_PLUS	MMC-DAT5	SP9
6	SD	SD-VSS	POWER
7	SD	SD-VDD	POWER
8	MemoryStick	MS-VSS	POWER
9	MemoryStick	MS-VCC	POWER
10	MemoryStick	MS-SCLK	SP1
11	MemoryStick	MS-DATA3	SP5
12	MemoryStick	MS-INS	SP2
13	MemoryStick	MS-DATA2	SP8
14	MemoryStick	MS-DATA0	SP9
15	MemoryStick	MS-DATA1	SP12
16	MemoryStick	MS-BS	SP14
17	MemoryStick	MS-VSS	POWER
18	SD	SD-CLK	SP8
19	MMC_PLUS	MMC-DAT6	SP7
20	SD	SD-VSS	POWER
21	MMC_PLUS	MMC-DAT7	SP5
22	SD	SD-DAT0	SP4
23	SD	SD-DAT1	SP3
24	SD	SD-COM(SW)	
25	SD	SD-CD(SW)	SP6
26	XD	XD-GND	POWER
27	XD	XD-CD	XD_CD#
28	XD	XD-R/-B	SP1
29	XD	XD-RE	SP2
30	XD	XD-CE	SP3
31	XD	XD-CLE	SP4
32	XD	XD-ALE	SP5
33	XD	XD-WE	SP6
34	XD	XD-WP	SP7
35	XD	XD-GND	POWER
36	XD	XD-D0	SP8
37	XD	XD-D1	SP9
38	XD	XD-D2	SP10
39	XD	XD-D3	SP11
40	XD	XD-D4	SP12
41	XD	XD-D5	SP13
42	XD	XD-D6	SP14
43	XD	XD-D7	XD-D7
44	XD	XD-VCC	POWER
45	SD	SD-WP(SW)	SP1

For EMI Reserved



<Core Design>

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Title: CARD Reader CONN

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<Core Design>

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Title: Reserved

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<Core Design>

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<Core Design>

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<Core Design>

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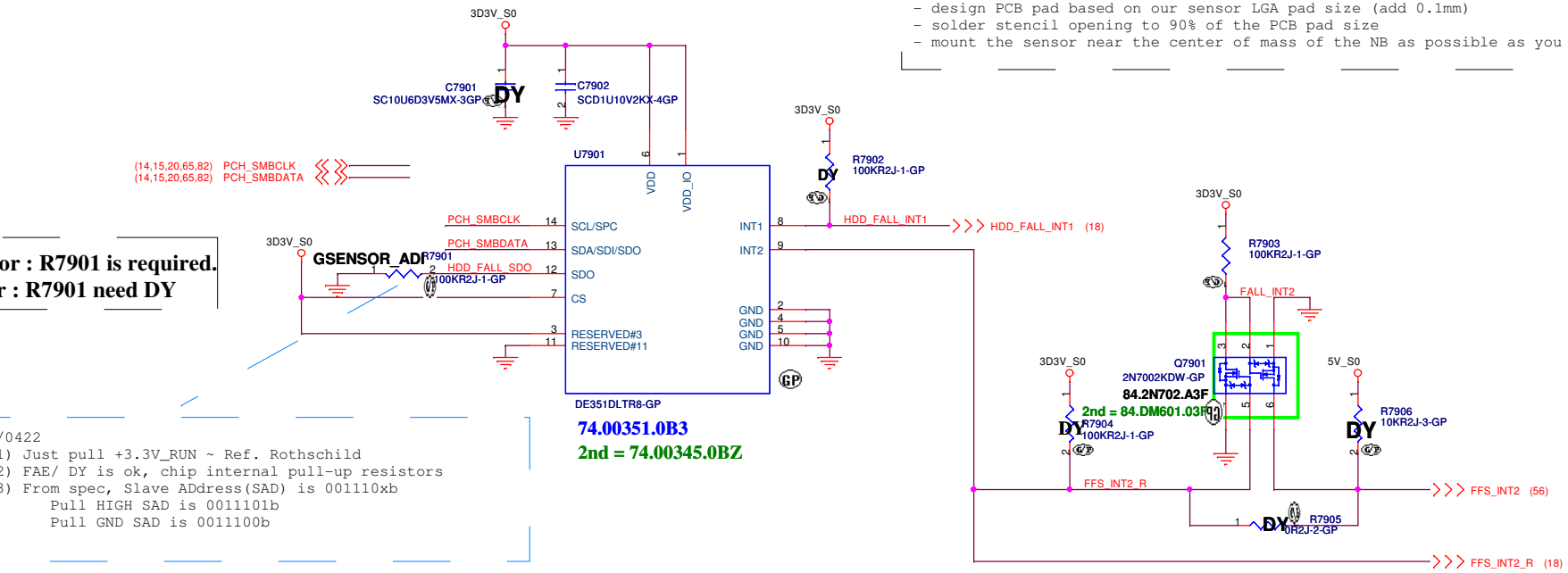
SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

For ADI G-sensor : R7901 is required.
For ST G-sensor : R7901 need DY



09/0422
(#1) Just pull +3.3V_RUN ~ Ref. Rothschild
(#2) FAE/ DY is ok, chip internal pull-up resistors
(#3) From spec, Slave ADdress(SAD) is 001110xb
Pull HIGH SAD is 0011101b
Pull GND SAD is 0011100b

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title	Free Fall Sensor	
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<Core Design>

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<Core Design>

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Title: Reserved

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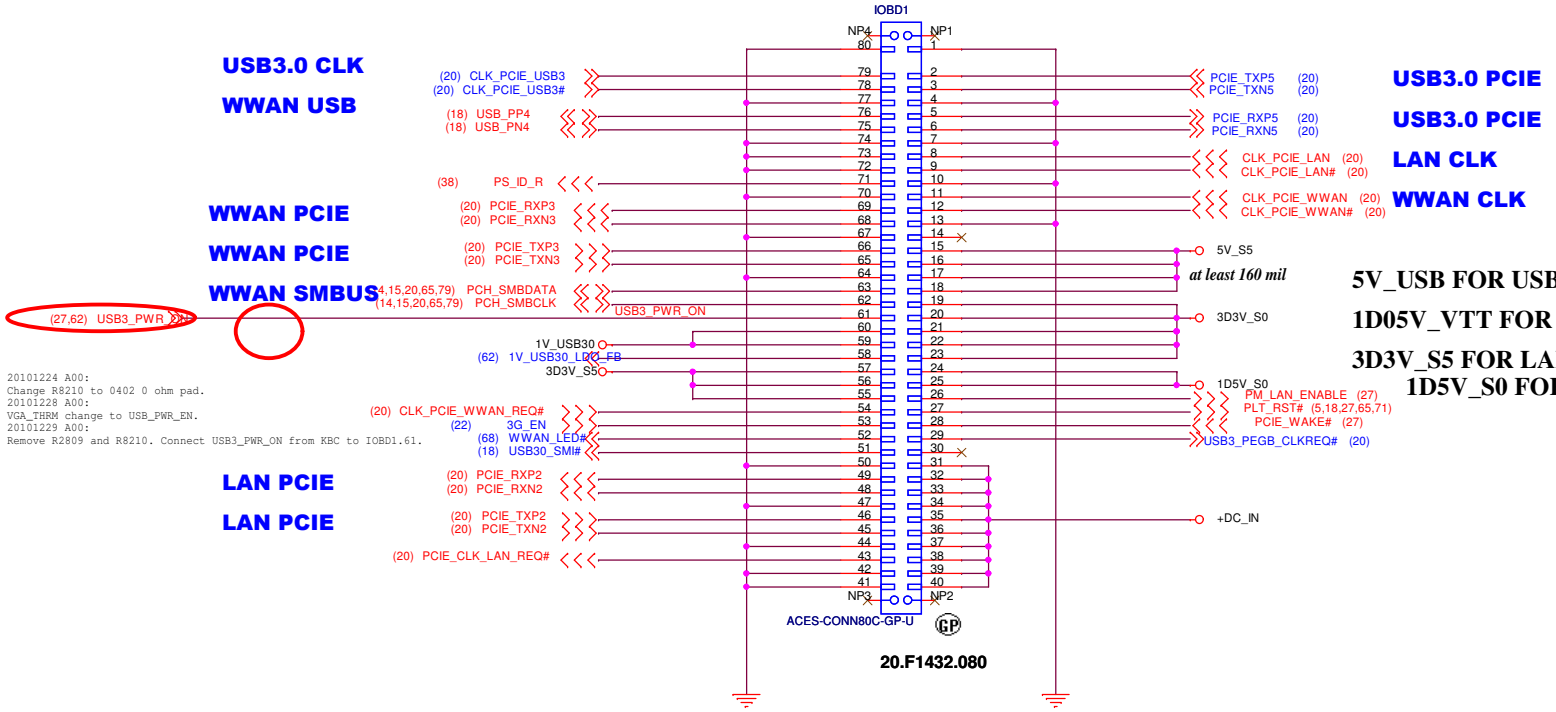
IO Board CONN 80 pin




```
20101224 A00:
Change R8210 to 0402 0 ohm pad.
20101228 A00:
VGA_THRM change to USB_PWR_EN.
20101229 A00:
Remove R2809 and R8210. Connect USB3_PWR_ON from KBC to IOBD1.61.
```

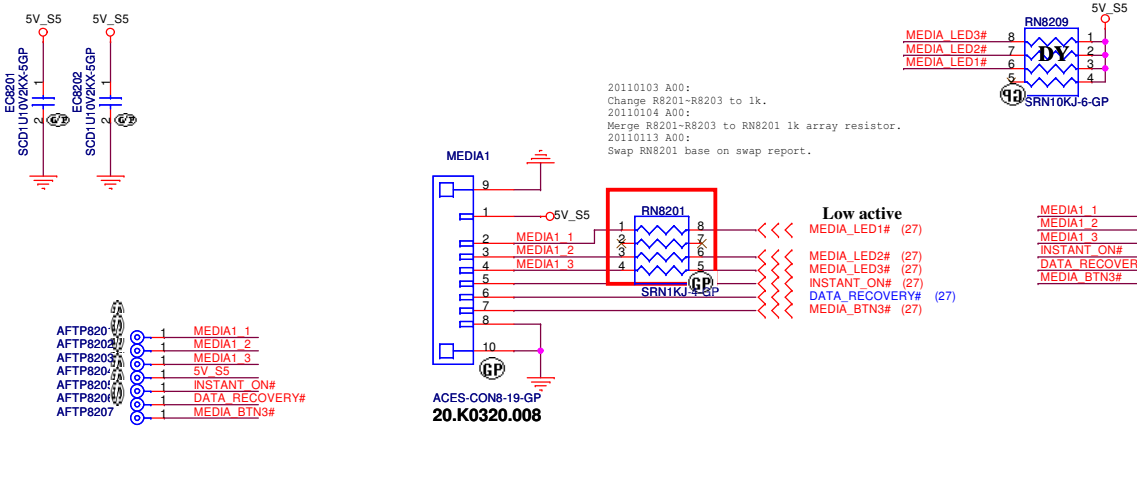
5V_USB FOR USB3.0 POWER at least 4A

1D05V_VTT FOR USB3.0 POWER at least ?A

3D3V_S5 FOR LAN POWER at least over 3pin amount.

1D5V_S0 FOR USB3.0 POWER at least ?A

Media Button Board Connector




```
20110103 A00:
Change R8201-R8203 to 1k.
20110104 A00:
Merge R8201-R8203 to RN8201 1k array resistor.
20110113 A00:
Swap RN8201 base on swap report.
```

<Core Design>

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Title	IO Board Connector	
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<Core Design>

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<Core Design>

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<Core Design>

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Title: Reserved

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<Core Design>

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Title: Reserved

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<Core Design>

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<Core Design>

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<Core Design>

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<Core Design>

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<Core Design>

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<Core Design>

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<Core Design>

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<Core Design>

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H1 HT85B85X925R29-S-GP
H2 HOLE335R115-GP ZZ.00PAD.D01
H3 STF276R160H209-1-GP 34.4ID01.001
H5 HOLE256R115-GP ZZ.00PAD.D11
H6 HT85BE85R29-U-5-GP ZZ.00PAD.D41
H7 HOLE256R115-GP ZZ.00PAD.D11
H8 HOLE256R115-GP
H10 HT85BE85R29-U-5-GP
H11 HOLE197R166-1-GP ZZ.00PAD.V71
H13 HOLE197R166-1-GP ZZ.00PAD.V71
H14 HT85BE85R29-U-5-GP ZZ.00PAD.D41
H12 HOLE197R166-1-GP ZZ.00PAD.V71
H15 HOLE335R115-GP ZZ.00PAD.D01
H16 HT85B85X925R29-S-GP
H17 HOLE276R158-GP ZZ.00PAD.U61
SPR1 SPRING-51-GP 34.4F822.002
SPR2 SPRING-24-GP-U
SPR3 SPRING-24-GP-U
SPR6 SPRING-24-GP-U
SPR4 SPRING-24-GP-U 34.45T31.001
SPR7 SPRING-57-GP 34.42T14.002
SPR8 SPRING-51-GP 34.4F822.002

EMI Request

AUD_DMIC_CLK — R9701 4.7R2J-2-GP — EC9719 SCD1U10V2KX-5GP
AUD_DMIC_IN0 — R9702 4.7R2J-2-GP — EC9720 SCD1U10V2KX-5GP
LVDS_DDC_DATA_R — EC9721 SCD1U10V2KX-5GP
LVDS_DDC_CLK_R — EC9722 SCD1U10V2KX-5GP

CLK_PCH_48M — EC9723 SCD1U10V2KX-5GP
(20,32) CLK_PCH_48M
(29,49) AUD_DMIC_CLK
(29,49) AUD_DMIC_IN0
(17,49) LVDS_DDC_DATA_R
(17,49) LVDS_DDC_CLK_R

EC9738 SCD1U10V2KX-5GP 3D3V_S0 — 5V_S5
EC9739 SCD1U10V2KX-5GP 5V_S0 — 3D3V_S0
EC9740 SCD1U10V2KX-5GP 5V_S5 — +DC_IN
EC9741 SCD1U10V2KX-5GP 5V_S5 — DCBATOUT
EC9742 SCD1U10V2KX-5GP 5V_S5 — 5V_S0
EC9743 SCD1U10V2KX-5GP 1D05V_VTT — 3D3V_S0
EC9744 SCD1U10V2KX-5GP 5V_S0 — 3D3V_S0
EC9745 SCD1U10V2KX-5GP 1D05V_VTT — 3D3V_S0
EC9746 SCD1U10V2KX-5GP 3D3V_S0 — 5V_S0
EC9747 SCD1U10V2KX-5GP 1D5V_S3 — 5V_S5
EC9748 SCD1U10V2KX-5GP 5V_S0 — 3D3V_S0

RF Request

1D05V_VTT: EC9724, EC9725, EC9726
5V_S5: EC9728, EC9729
5V_S0: EC9730, EC9731, EC9732
3D3V_S0: EC9735, EC9736, EC9737
(SCD1U10V2KX-5GP)

EC9727 SCD1U10V2KX-5GP 3D3V_S0 — 1D05V_VTT
EC9734 SCD1U10V2KX-5GP
EC9733 SCD1U10V2KX-5GP 3D3V_S0 — 5V_S0

<Core Design>

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Title: UNUSED PARTS/EMI Capacitors
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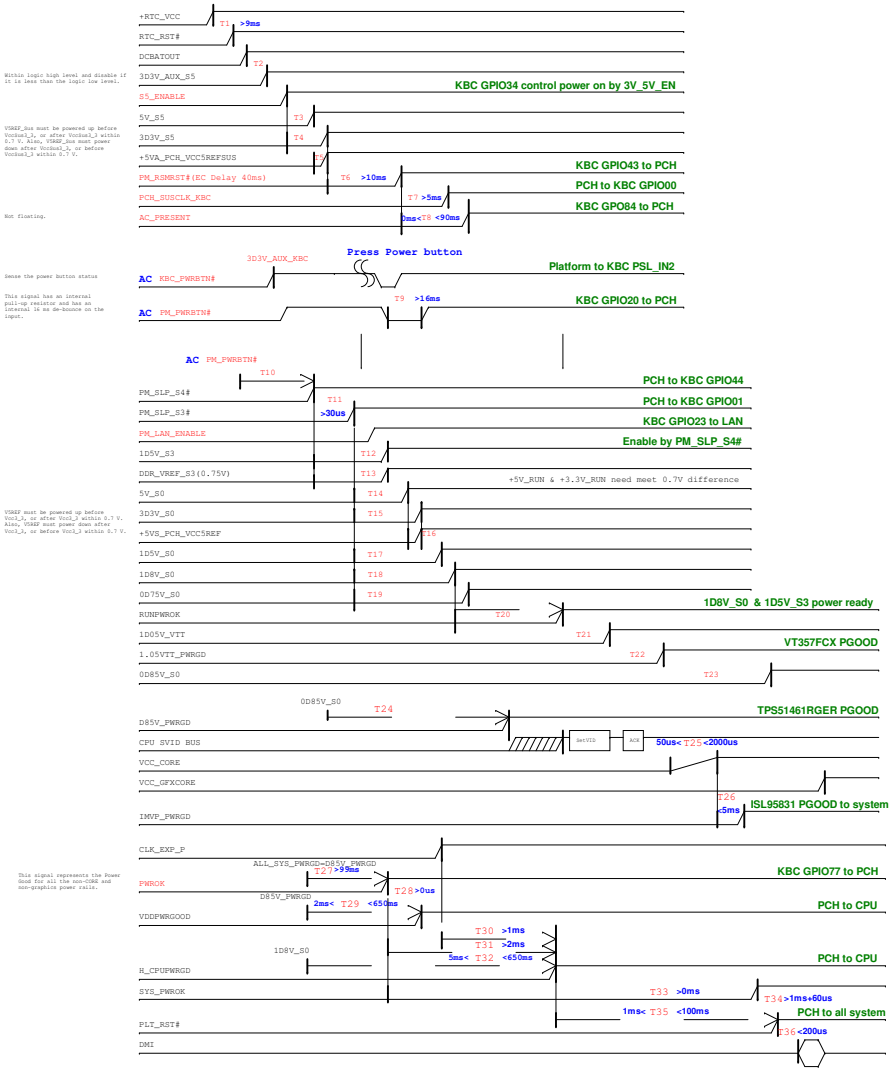
Date: Tuesday, January 18, 2011 | Sheet 97 of 103

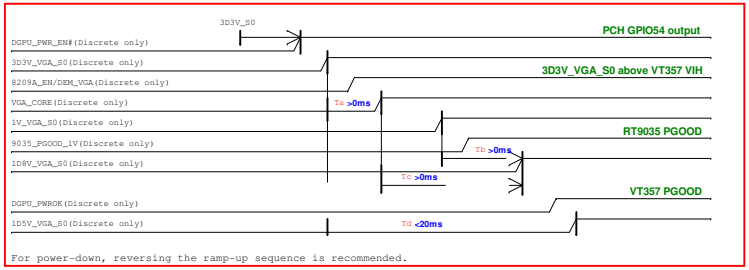
Huron River Platform Power Sequence

(AC mode)

red word: KBC GPIO



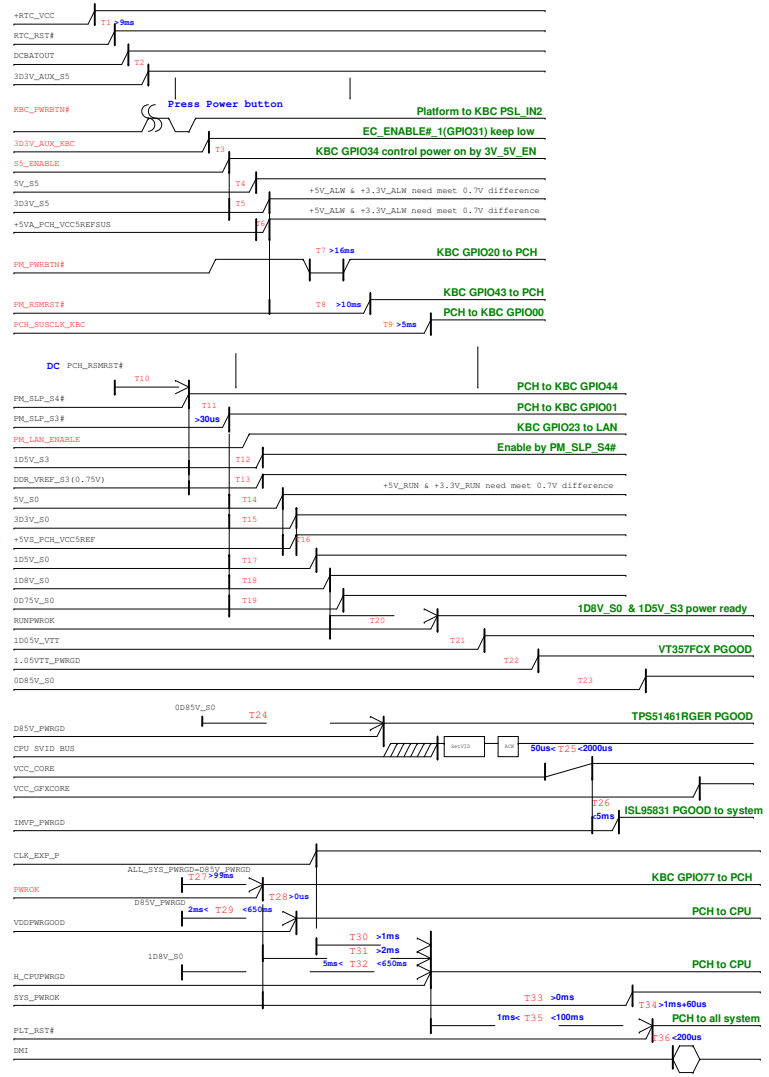
Robson XT Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

(DC mode)

red word: KBC GPIO



<Core Design>

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Title: Power Sequence

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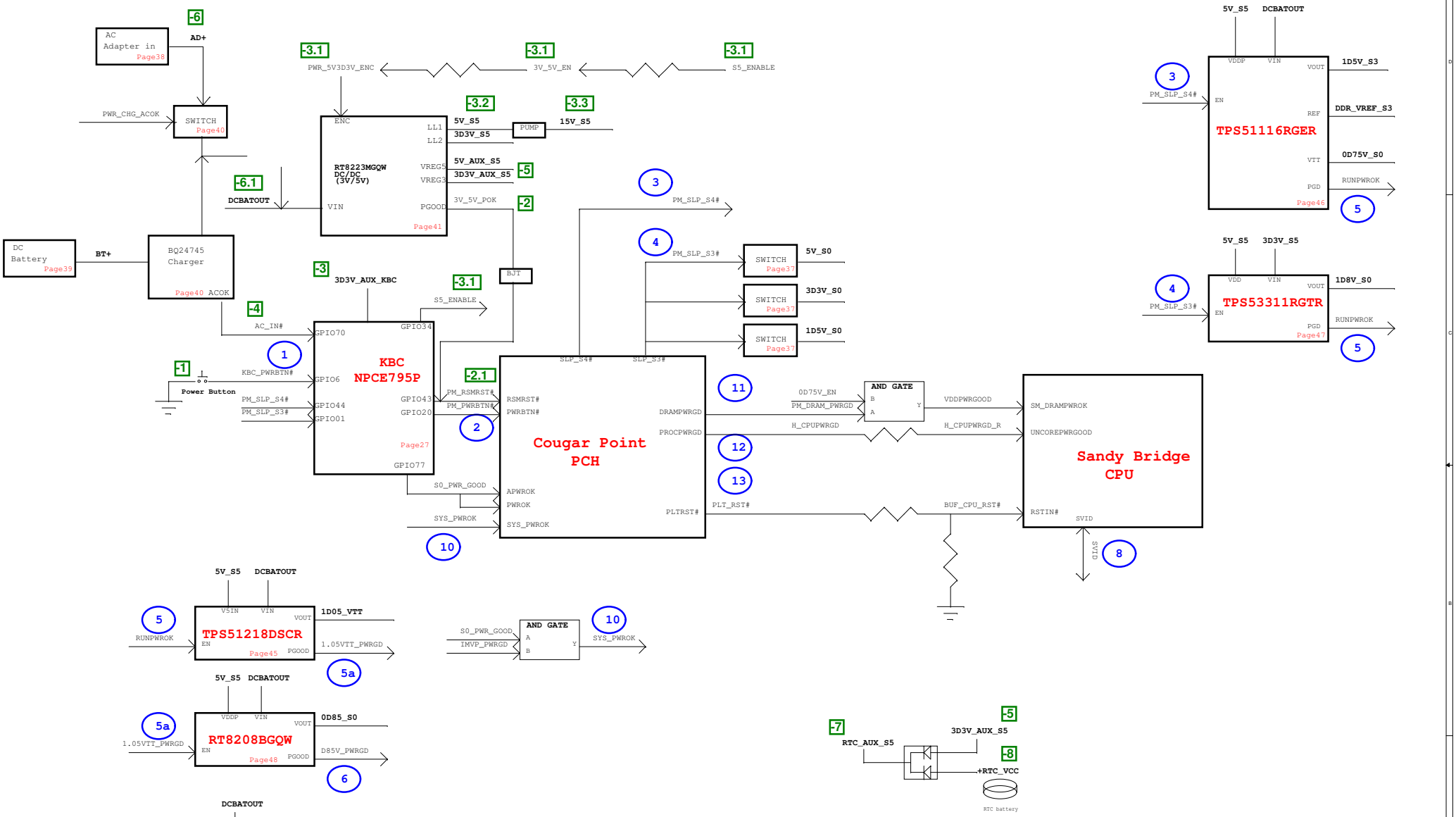
Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13

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Title: Power Up Sequence Diagram

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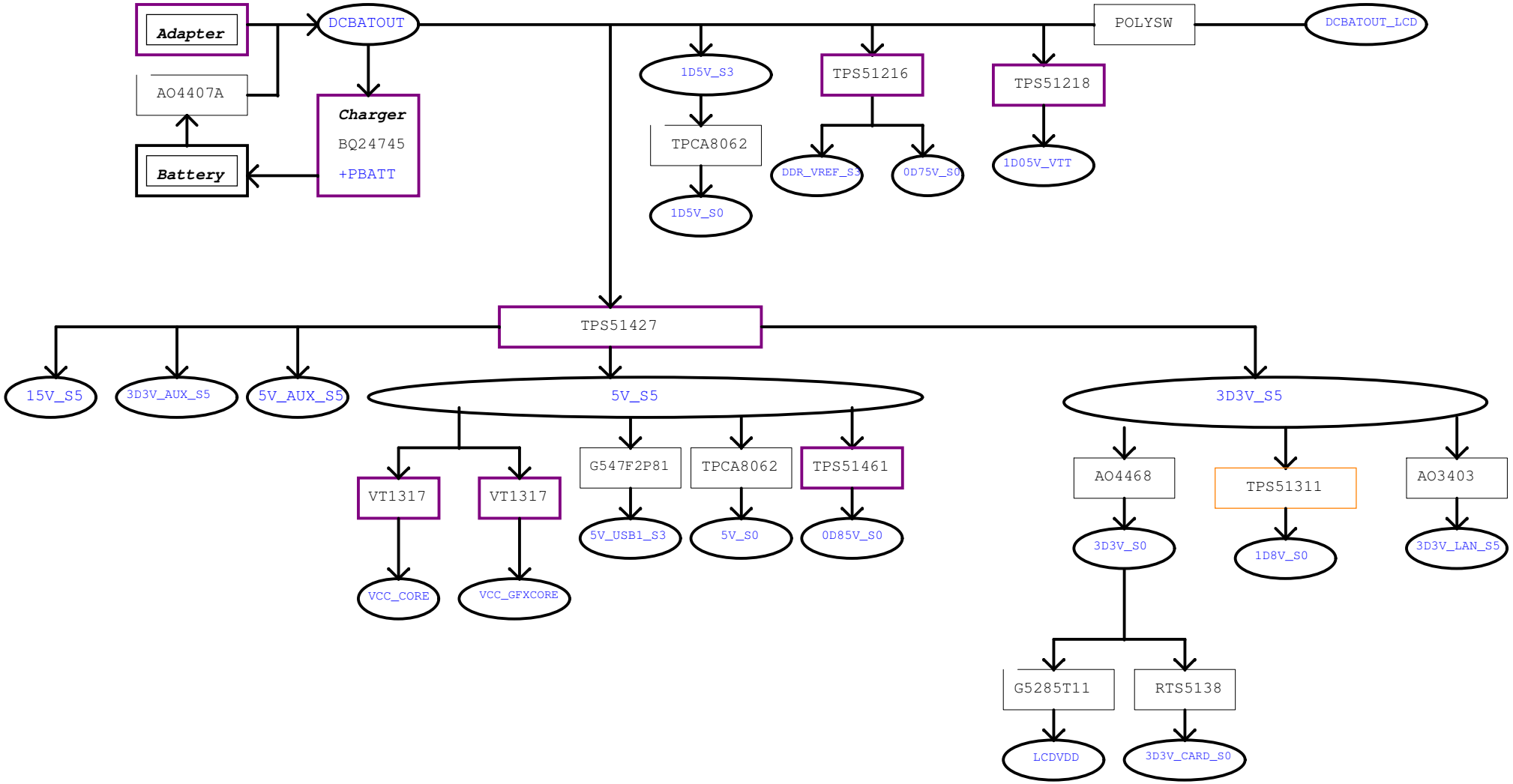

Power Shape

Regulator	LDO	Switch

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Title: *Power Block Diagram*

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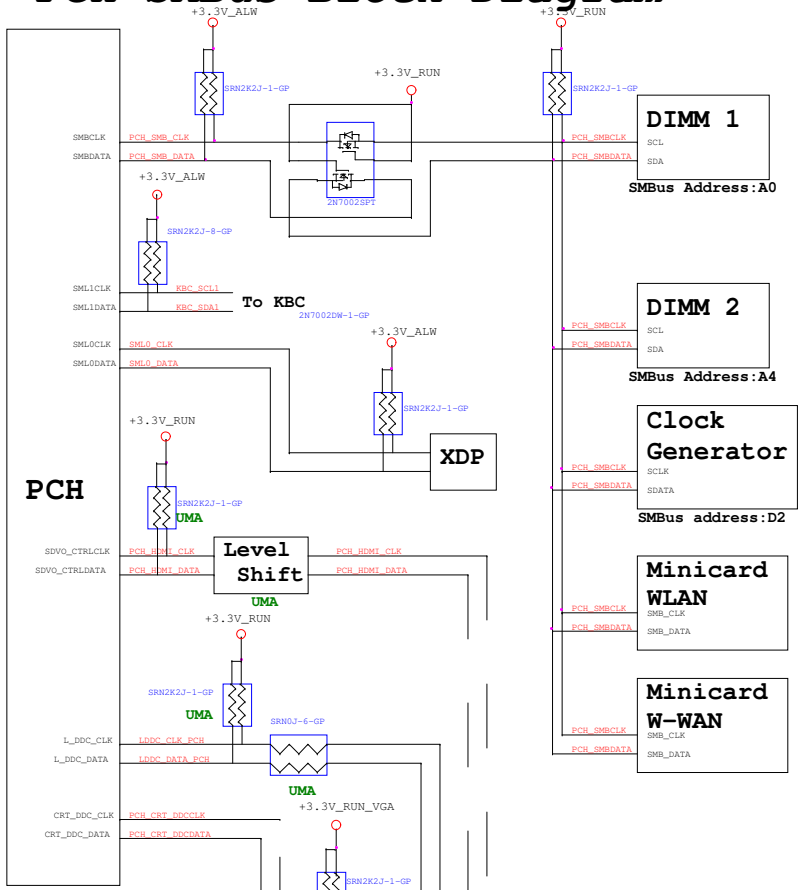
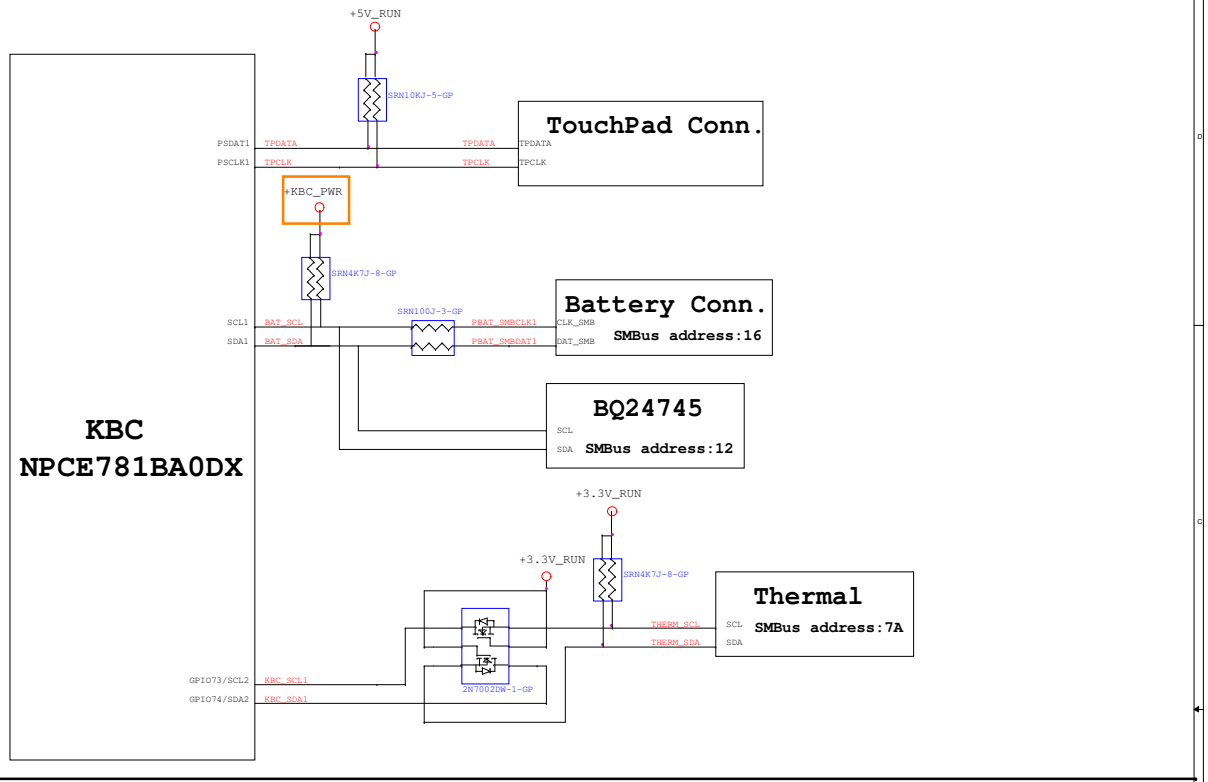
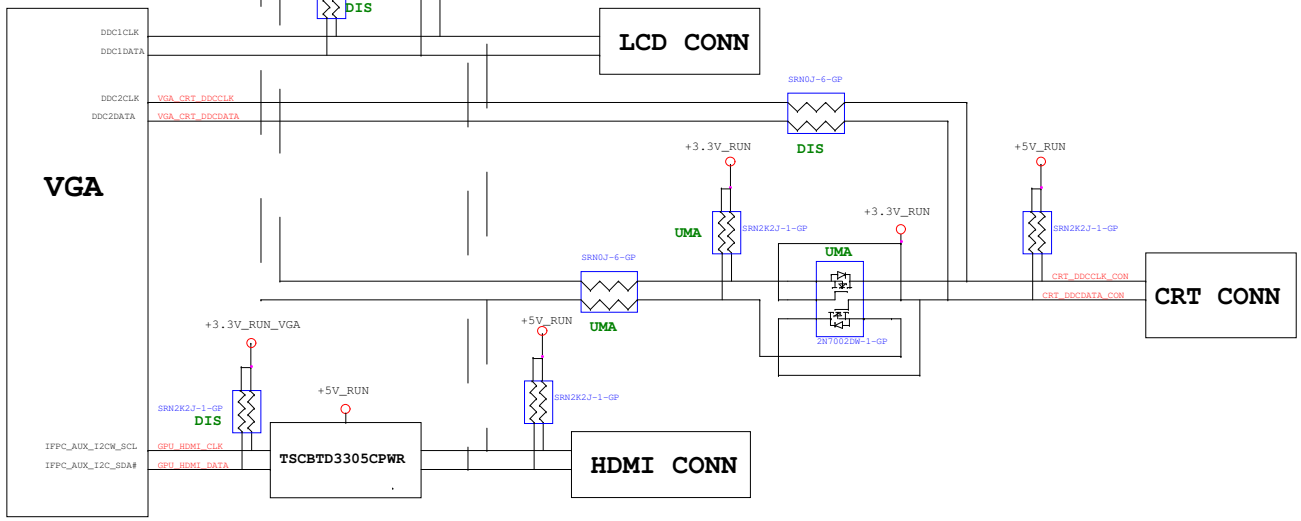
PCH SMBus Block Diagram



KBC SMBus Block Diagram





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Title: SMBUS Block Diagram

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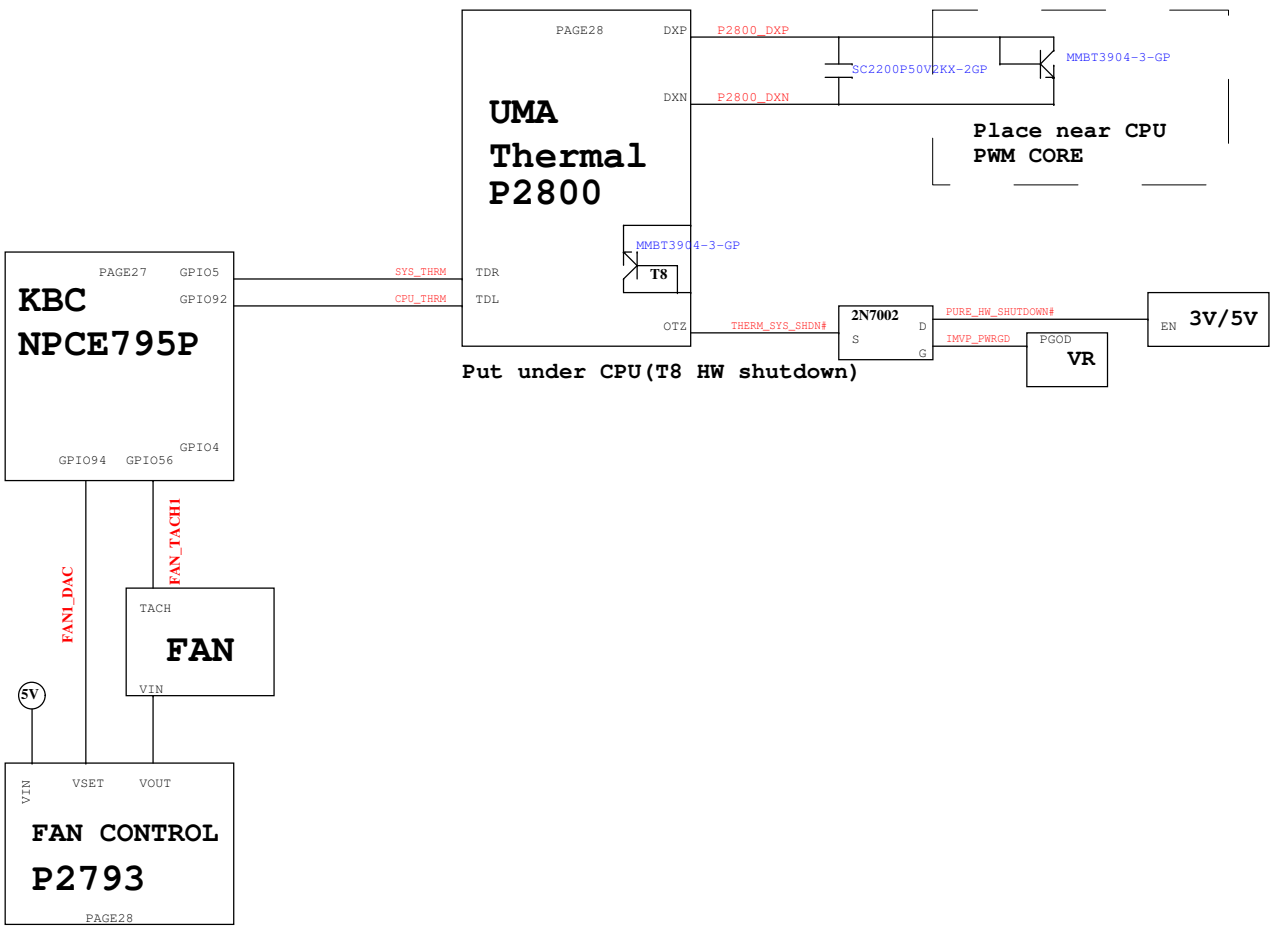
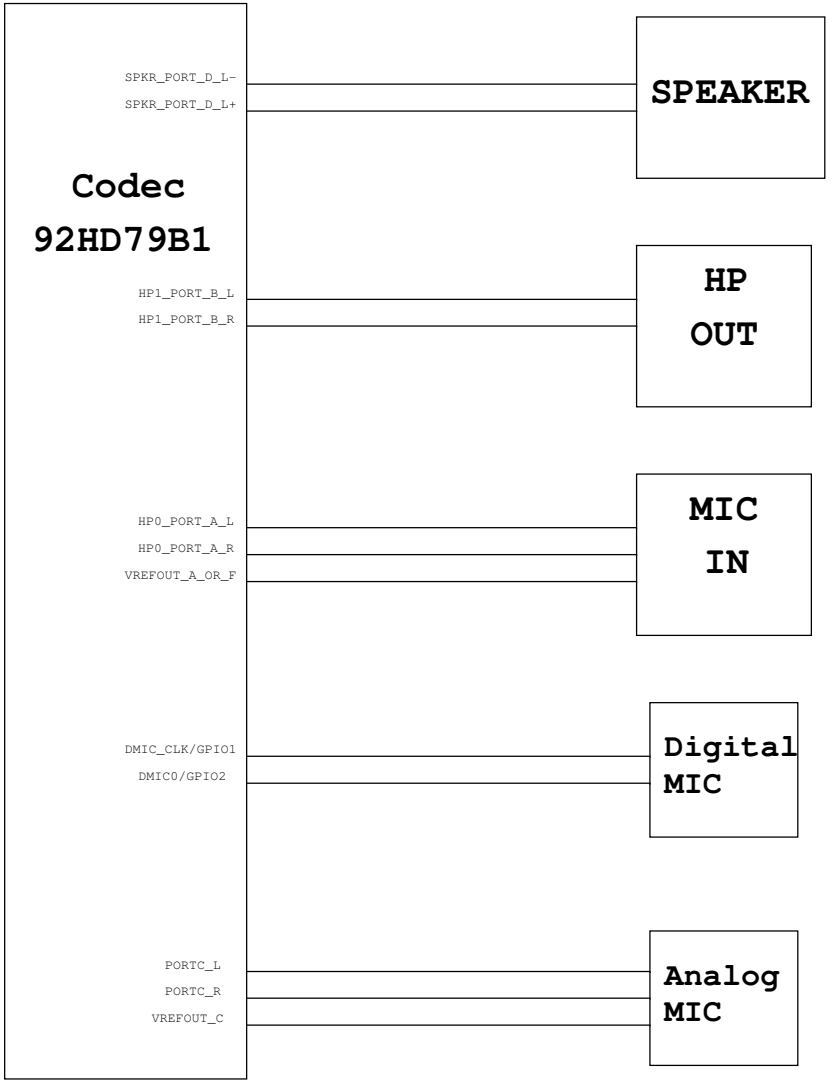
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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Version	Date	Page	Function	Change Item
A00	20101222	40	Power	Power/Brian: Change PR4047 to 174k ohm from 121k ohm. Change PR4035 to 300k from 49.9k. Change PR4031 to 150k from 0 ohm. Change PR4034 to 0 ohm pad. Stuff PQ4003. Change PR4036 to 0 ohm pad. Stuff PQ4004. Change PR4037 to 76.8k ohm from 49.9k ohm. Change PR4032 to 0 ohm pad.
A00	20101222	42	Power	Power/Brian: Change PU4201 to 74.01316.F33.
A00	20101224		EE	Change all of 0ohm to short pad at X-build stage: 0402: R1404 R1405 R1503 R1504 R5010~R5012 R1807 R2301 R2306 R2307 R2308 R2404 R2405 R2735 R2737 R2758 R2759 R2760 R3614 R3710 0603: R5803 R5804 R8507 Parallel resistor: RN1704 RN2010 RN2011 RN2012 RN2013 RN2014 RN2016 RN5117,RN5112,RN5113,RN5114,RN5115
A00	20101224		EE	Rename PRN3901 to PN3901. Rename PTC4101~PTC4103 to PT4101~PT4103. Rename PTC4502,PTC4509 to PT4502~PT4509. Rename PTC4601,PTC4602 to PT601~PT4602. Rename PTC4801 to PT4801. Rename LINEOUT1 to LOUT1. Rename PWRBTN1 to PWRBT1. Rename HALLSW1 to LID1.
A00	20101224	27	EE	Change R2724 to 47K from 33K.
A00	20101224	28	EE	If stuff P2800EA1 then must stuff R2803,R2804 C2805 but if stuff P28003B0 should be un-stuff.
A00	20101224	45,46	Power	Change PR4514,PR4607 to 0ohm short pad from 0402 and un-stuff PC4523 at X-Build stage.
A00	20101224	28	EE	If stuff P2800EA1 then must stuff R2803,R2804 C2805 but if stuff P28003B0 should be un-stuff.
A00	20101227	32,42,49 62,64,65 69,70	EE	Change R3210,R3211;PR4217~PR4220,PR4254;R4908,R4909,R4903,R4910,R4913~R4916, R4917,R4918;R6205;R6403,R6404;R6511;R6902;R7002 to 0R 0402 pad.
A00	20101228	23	EE	0402 0R pad: R2301.
A00	20101228	27,62,82	EE	VGA_THRM change to USB_PWR_EN.
A00	20101228	27	EE	Change R2756,R2763,R2766 to 0R short pad.
A00	20101228	28	EE	Un-stuff U2805 G709T1UF related circuit and R2812 then stuff R2805 at X-Build.
A00	20101229	71	EE	DB1 change to ZZ.00PAD.Y41(solder mask type) and keep un-stuff at X-Build stage.
A00	20101229	27,62,82	EE	Rename USB_PWR_EN to USB3_PWR_ON. Remove R6205,R620. Remove R2809 and R8210. Connect USB3_PWR_ON from KBC to IOBD1.61.
A00	20101230	41,46,65	EE	Change PR4119 to 0R short pad. Change PR4114 to 0R short pad. Follow the standard schematics: remove PR4615,PR4616. Change R6406,R6405 to 0R short pad. Change PR4116 to 0R0603 short pad. Change PR4106 to 0R0603 short pad. Change R6510 to 0R 0603 pad. Change PR4103,PR4104 to 0R0805 short pad.
A00	20101231	43	Power	Power/Brian: change PL4201 to 68.2415N.101 from 68.10110.10G.
A00	20101231	42,50,18 14,9,8	EE	Change PR4209,PR4212 to PN4201 10k array resistor. Change R5004,R5005 to RN5001 33 ohm array resistor. Merge R1804,R1806 to RN1804 22 ohm array resistor. Merge R1401,R1402 to RN1401 10k ohm array resistor. Merge R906,R907 to RN902 100 ohm array resistor. Merge R801,R802 to RN801 100 ohm array resistor.
A00	20110103	68,82	EE	Change R6801,R8201~R8203 to 1k.
A00	20110103	68,82	EE	Change R6801,R8201~R8203 to 1k.
A00	20110104	5	EE	merge R512,R514 to RN502 1k array resistor.
A00	20110104	8	EE	Swap VCC_CORE to RN801.4 and VCCSENSE to RN801.1.
A00	20110104	9	EE	Swap VCC_GFXCORE to RN902.1 and VCC_AXG_SENSE to RN902.4.
A00	20110104	14	EE	Change RN1401 to 0R short pad.
A00	20110104	15	EE	Change R1502 to 0R0402 short pad.
A00	20110104	17	EE	Merge RN1701,RN1706 to RN1703 2.2k array resistor.
A00	20110104	32,49,57 64	EE	Remove TR3201,TR4902,R5718,R5719,TR6401
A00	20110104	68,69	EE	Change R6804,R6806,R6808,R6810,R6906 to 620 ohm 5%.
A00	20110104	82	EE	Merge R8201~R8203 to RN8201 1k array resistor.
A00	20110107	68,69	EE	Change R6804,R6806,R6808,R6810,R6906 to 1k ohm 5%.

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Version	Date	Page	Function	Change Item
A00	20110107	49	EE	Change F4902 to 0603 0 ohm.
A00	20110110	21	EE	Merge R2115,R2116 to RN2101.
A00	20110110	41	Power	Change PG4110,PG4112,PG4114~PG4119,PG4122,PG4126,PG4129,PG4131,PG4133,PG4135~PG4138,PG4140,PG4142,PG4102~PG4109,PG4111,PG4113,PG4118,PG4120,PG4123,PG4101,PG4127,PG4130,PG4132,PG4134, PG4139,PG4141 to ZZ.CLOSE.001.
A00	20110110	41	Power	Add PT4104 47uF.
A00	20110111	49,51	EE	Change R4908,R4909,R4903,R4910,R4913~R4916 R4917,R4918 to 0R 0402 reisstors. Change R5101~R5108 to 0 ohm array resistors RN5102~RN5105. Change RN5117 to 0 ohm resistor.
A00	20110112	20	EE	Change C2007,C2008 to 15pF from 12pF base on vendor's report.
A00	20110112	41	EE	Change PT4104 to 100uF.
A00	20110113	8,9	EE	Change RN801,RN902 to 100 ohm 1% (66.10156.04L).
A00	20110113	5,8,9 17,18,21 42,82	EE	Swap RN502,RN801,RN902,RN1703,RN1804,RN2101,RN4201,RN8201 base on swap report.
A00	20110118	51	EE	Remove RN5117 for PCH_HDMI_CLK and PCH_HDMI_DATA.

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Title: Change History

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