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ACLU9 M/B Schematics Document

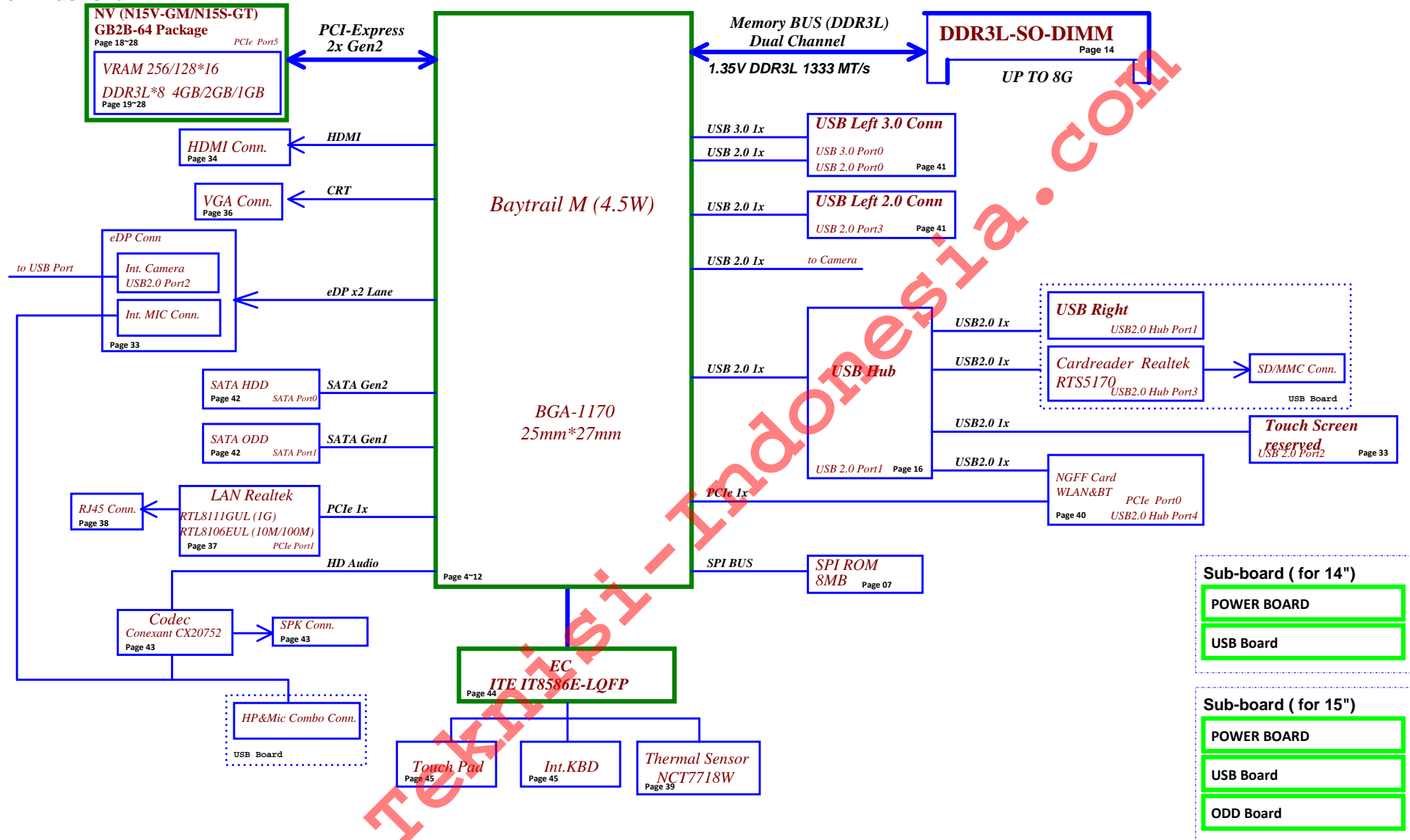
Intel BayTrail M-Processor with DDRIII L + NV (N15V-GM/N15S-GT) GPU

2013-12-22

REV: 0.2

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Power Plane State	B+ +3VL	+3VALW +5VALW	+3VALW_SOC +1.0VALW +1.8VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS +0.68VS CPU_CORE GFX_CORE
S0	O	O	O	O	O
S3	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	+VALW	+VALW_PCH	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	ON	OFF	OFF	OFF

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X


SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

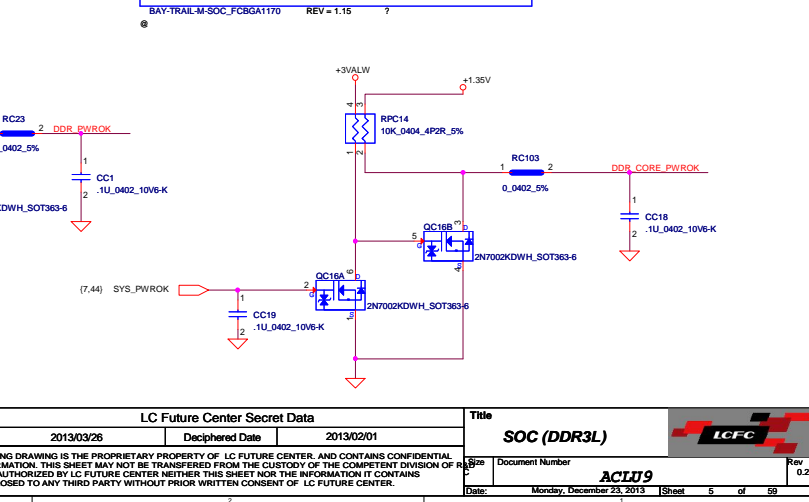
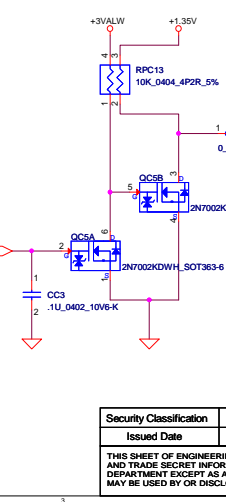
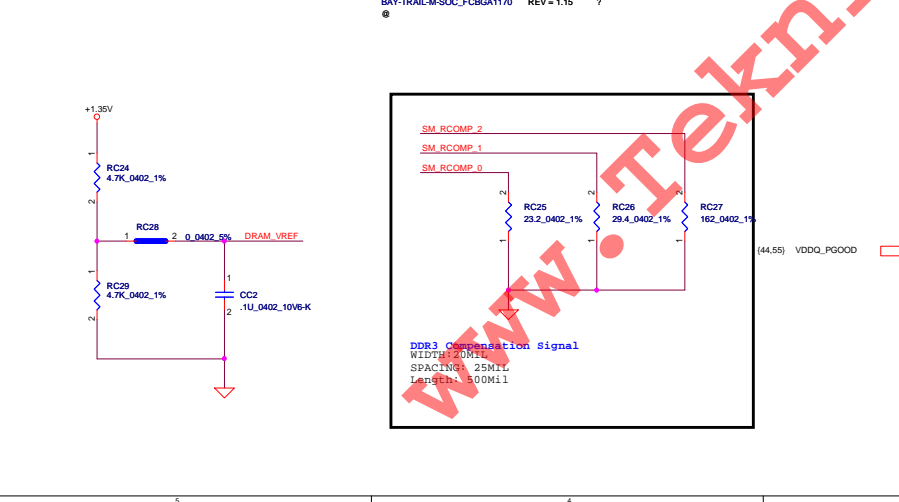
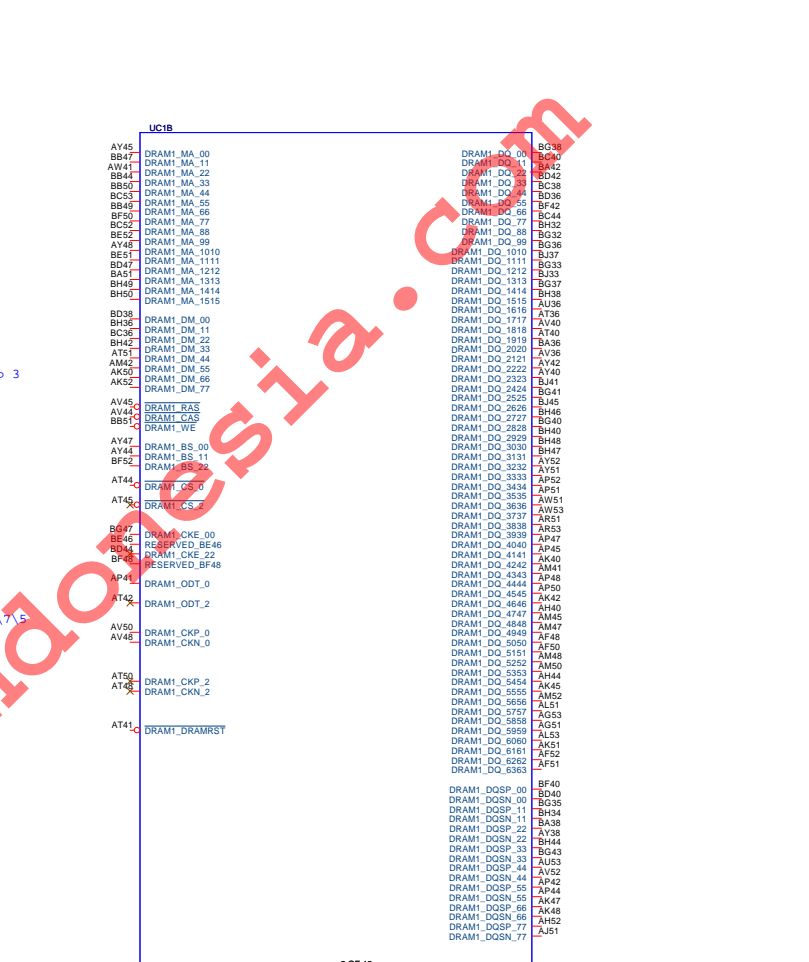
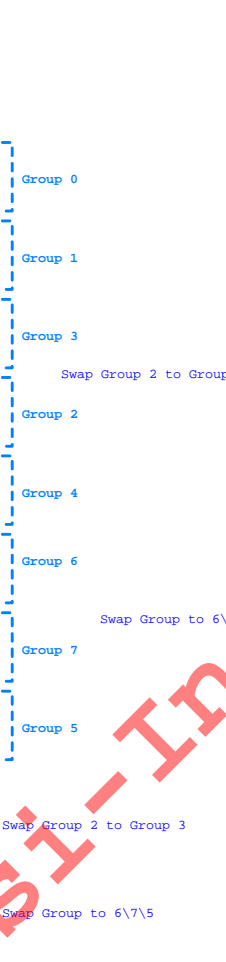
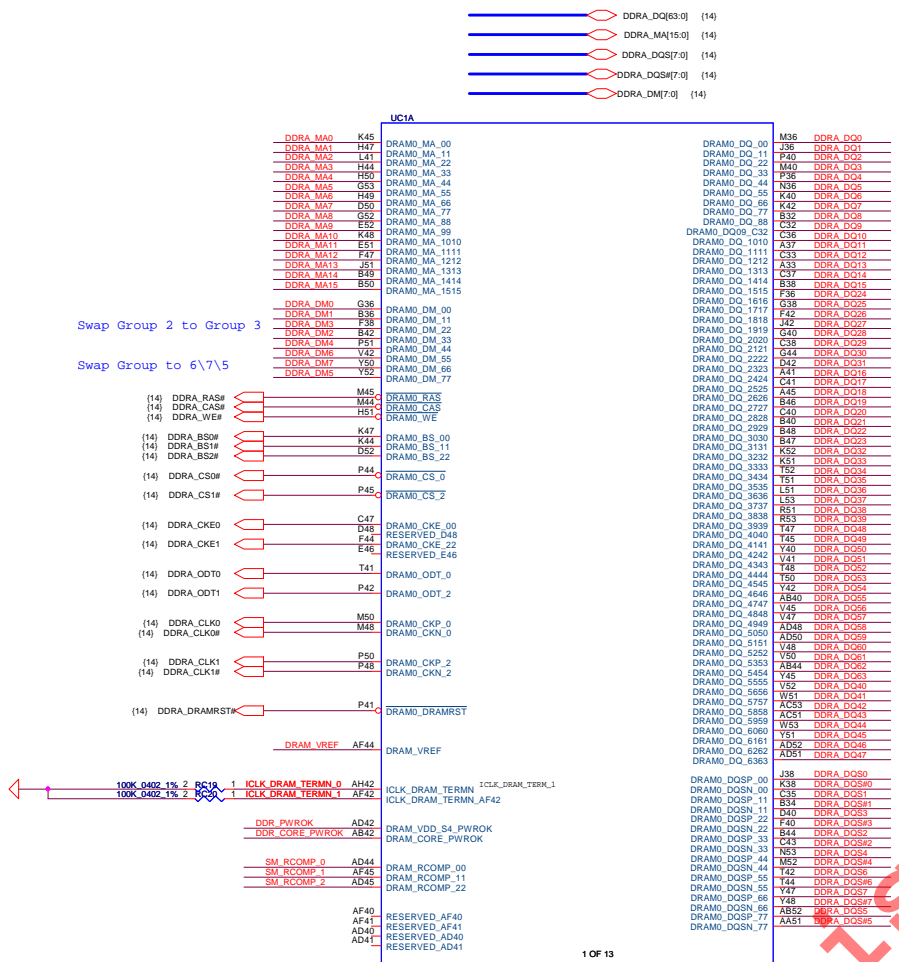
USB 2.0	USB 3.0	Port	3 External USB Port
EHCI1	XHCI 1	0	USB Port (Left Side)
		1	USB Port (Right Side)
		2	USB Port (Left Side)
		3	USB HUB
USB HUB		1	Camera
		2	Cardreader
		3	BT(WLAN)
		4	TOUCH PANEL


[illegible]

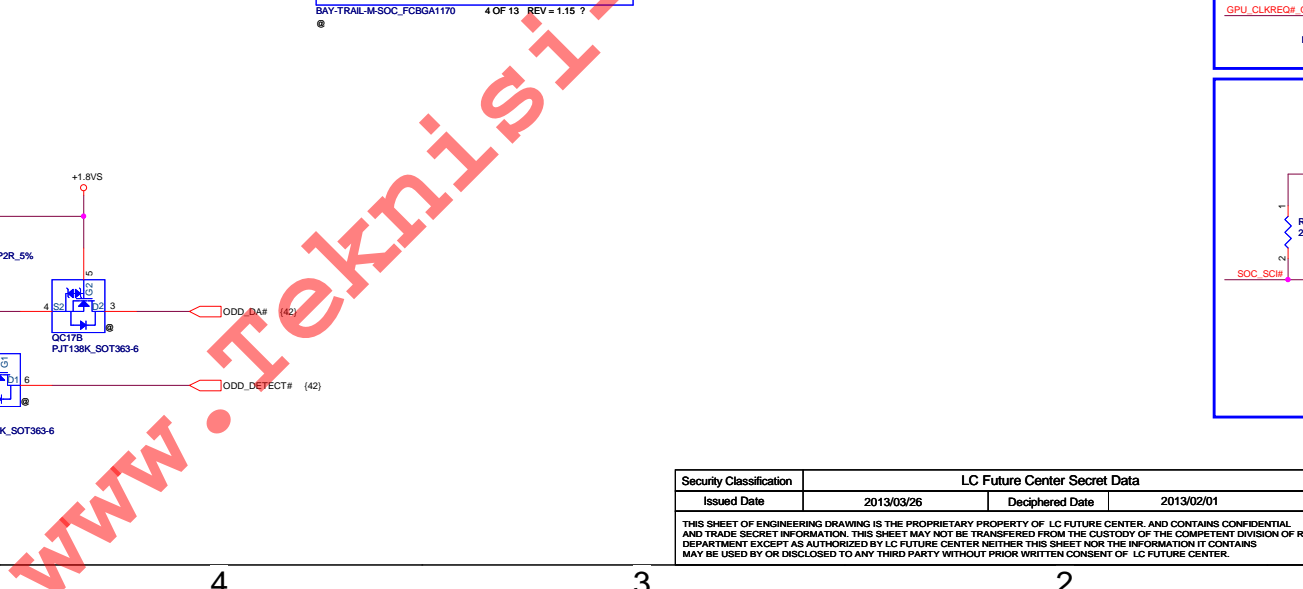
Port	Device
1	Discrete GPU
2	Discrete GPU
3	WLAN
4	LAN
5	
6	
7	
8	

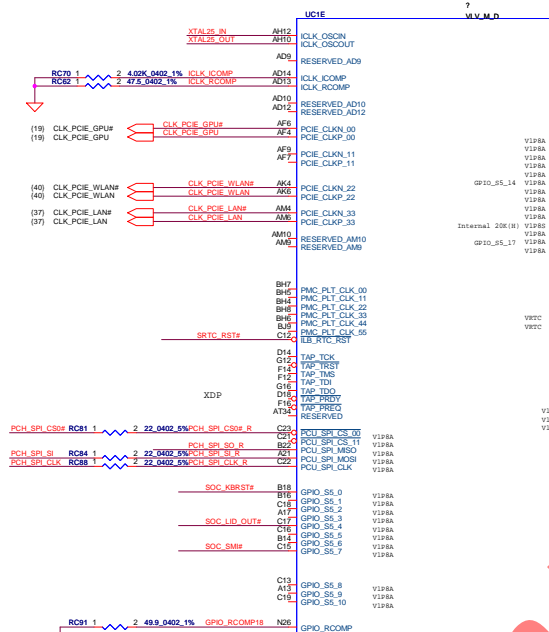
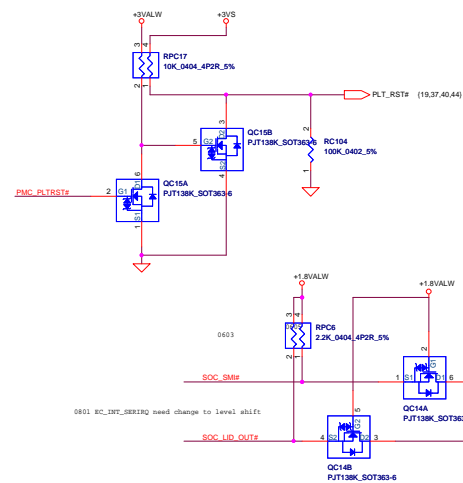
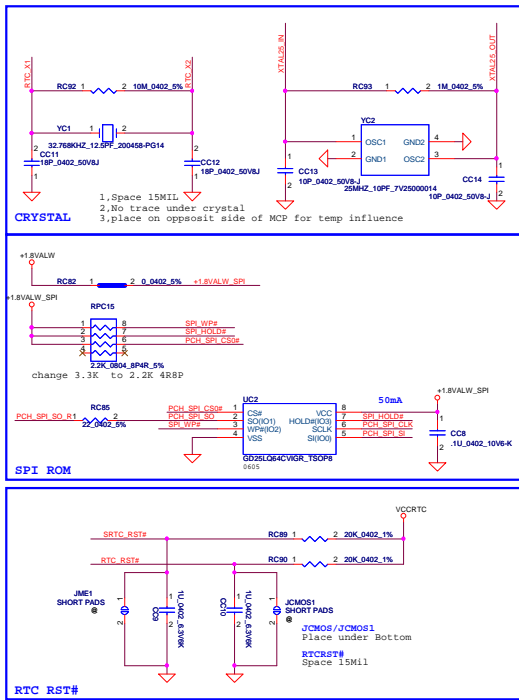
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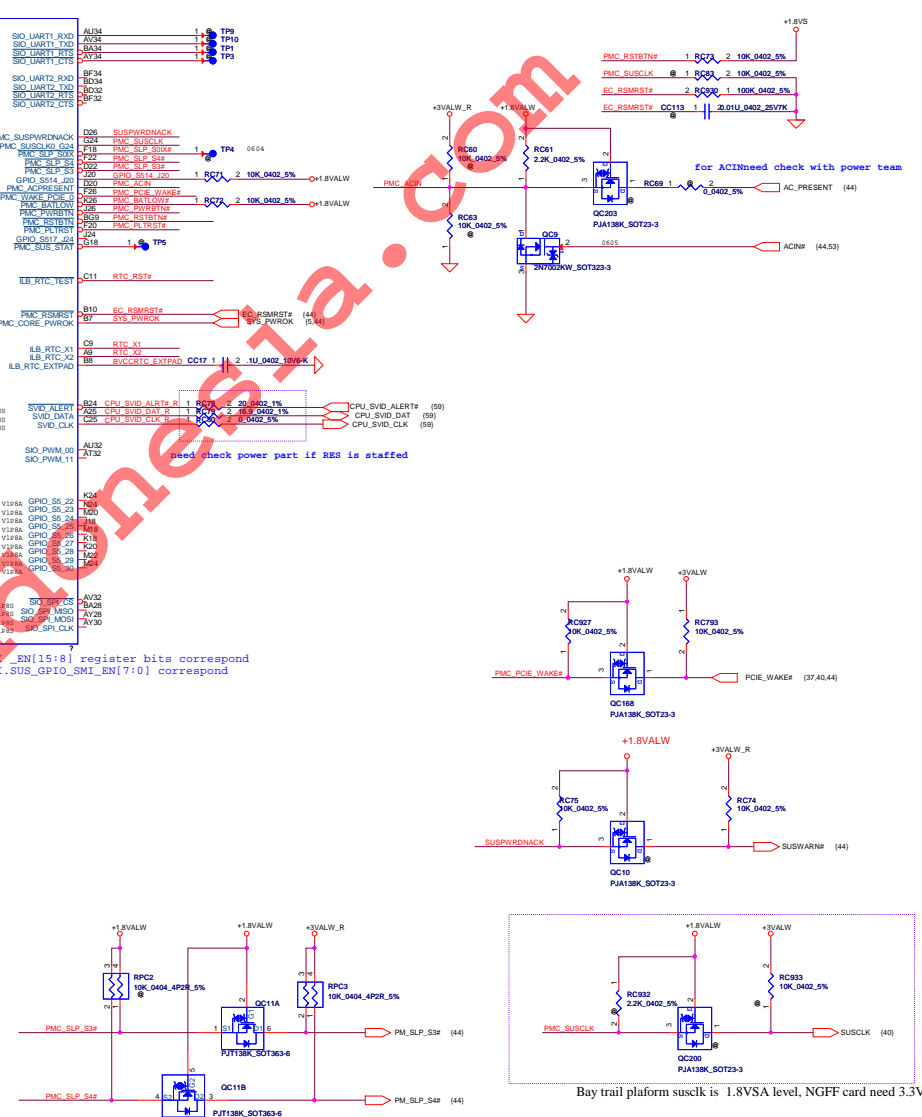


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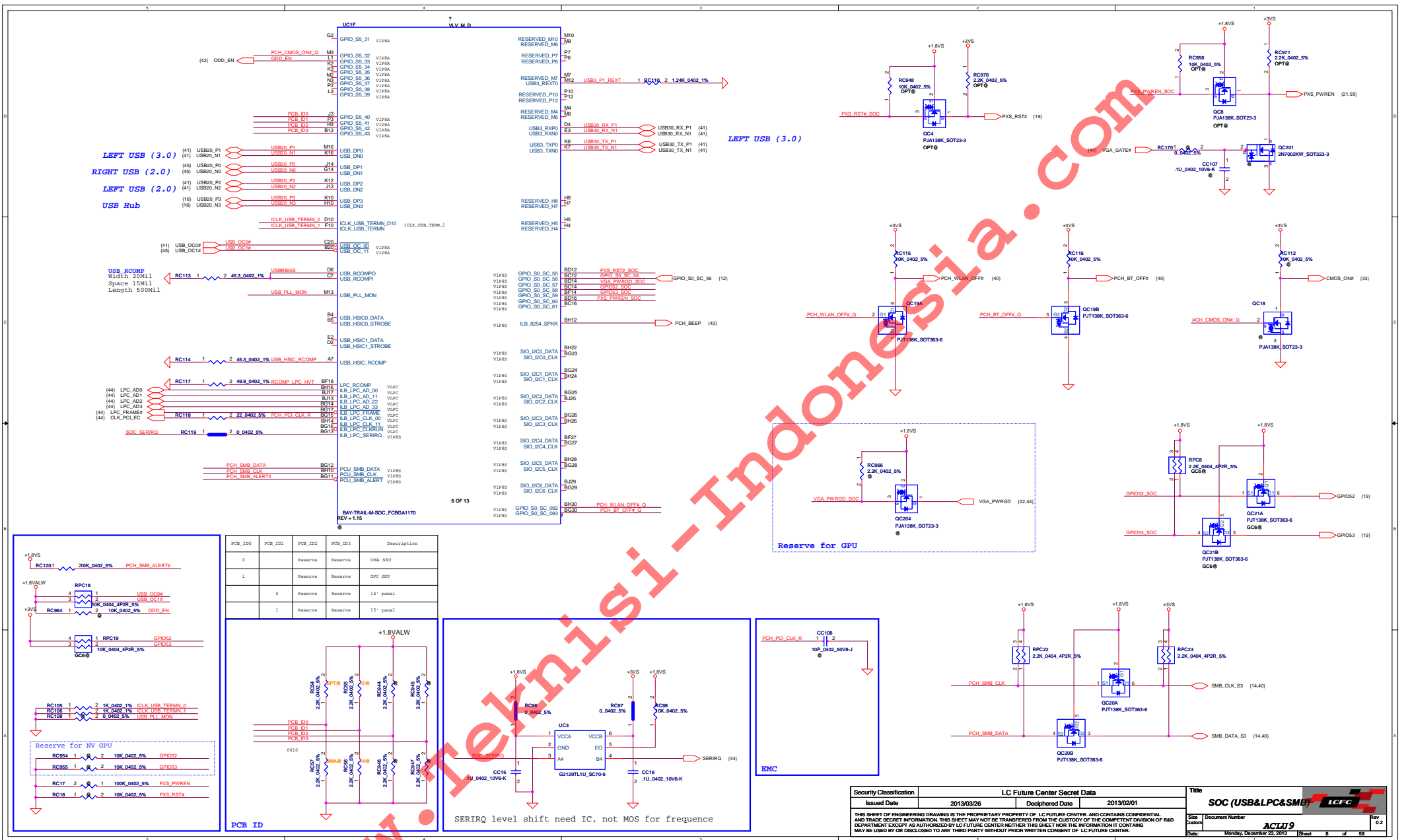


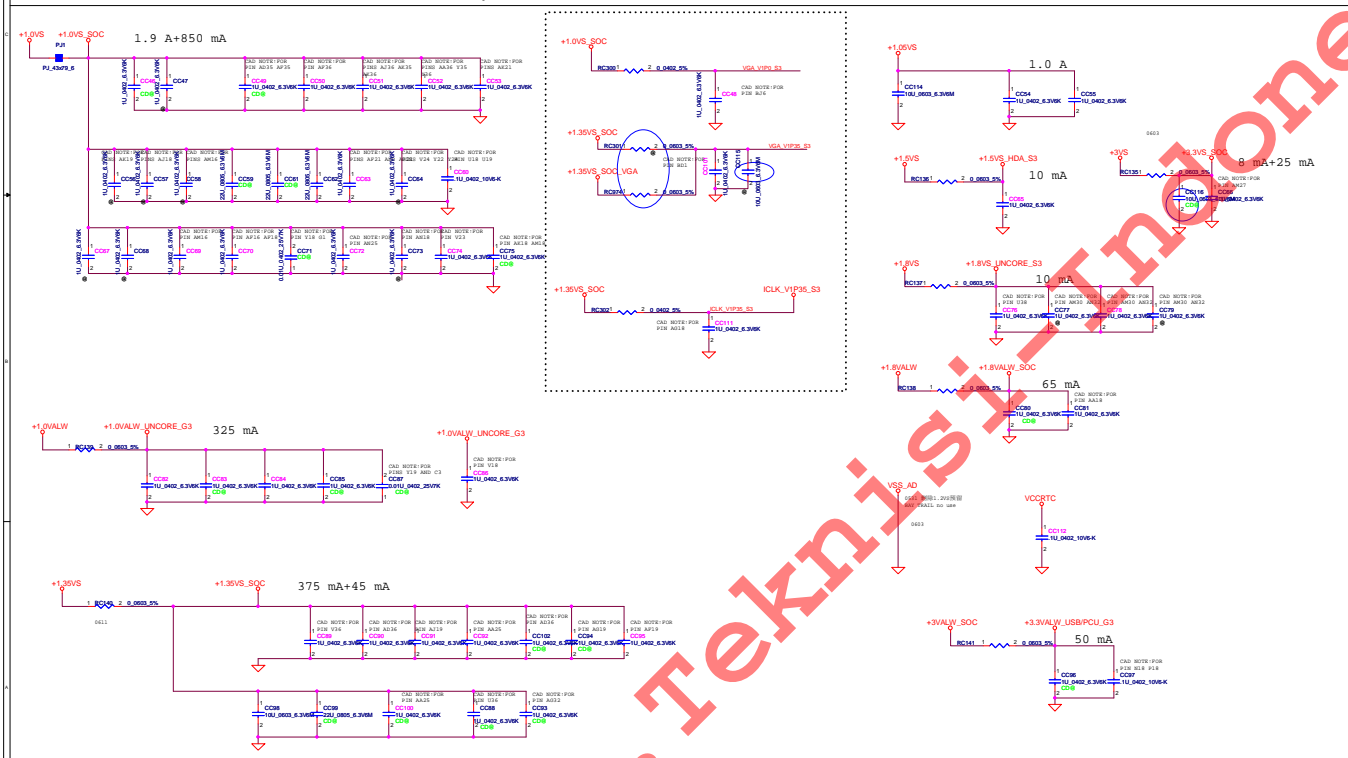



The ALT_GPIO_SMI_CORE_GPIO_SMI_STS[31:24] & ALT_GPIO_SMI_CORE_GPIO_SMI_STS[23:16] & ALT_GPIO_SMI_SUS_GPIO_SMI_STS[7:0] correspond to GPIO_S5[7:0]. ALT_GPIO_SMI_SUS_GPIO_SMI_STS[23:16] & ALT_GPIO_SMI_SUS_GPIO_SMI_STS[7:0] correspond to GPIO_S5[7:0].

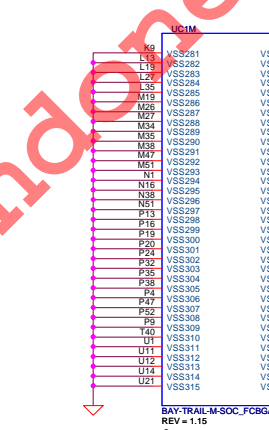
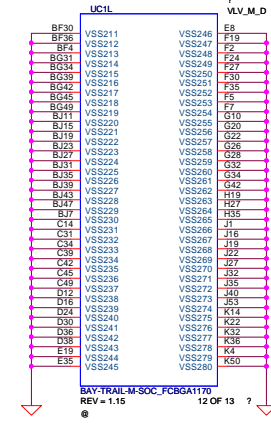
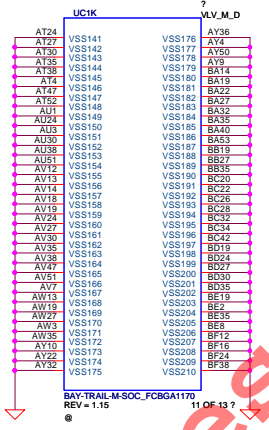
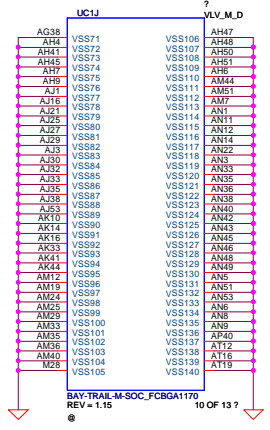
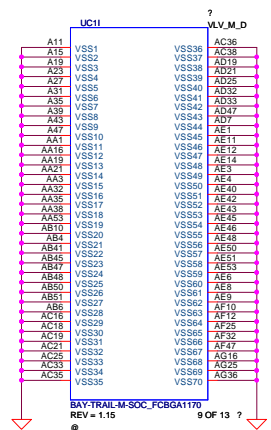


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<p>Date: Monday, December 24, 2013</p>			<p>Time: 10:48 AM</p>	



Hardware STRAPS (Follow up CRB& VIENNA)

GPIO_NC13
GPIO_S0_SC_56
I2S_2_FS
I2S_2_TXD
PCH_HDMI_DDC_DAT
DDI0_DDCDATA

MDSI_DDCDATA(Checklist request 10K pull down)
GPIO_S0_SC_56(Internal Pull-up)
GPIO_S0_SC[063] (Internal Pull-up)
GPIO_S0_SC[065](Internal Pull-up)
DDI1_DDCDATA
DDI0_DDCDATA

GPIO_S0_SC_56:

A16 Top Swap

0=Top address bit is unchanged

1=Top address bit is inverted

GPIO_S0_SC[063]

Multiplexed with Hardware Straps Pin LPE_I2S2_FRM

BIOS Boot Selection

0=LPC

1=SPI

GPIO_S0_SC[065]

Multiplexed with LPE_I2S2_DATAOUT

Security Flash Descriptors

0=Override

1=Normal Operation

DDI0_DDCDATA:

DDI0 strap

0=DDI0 not detected

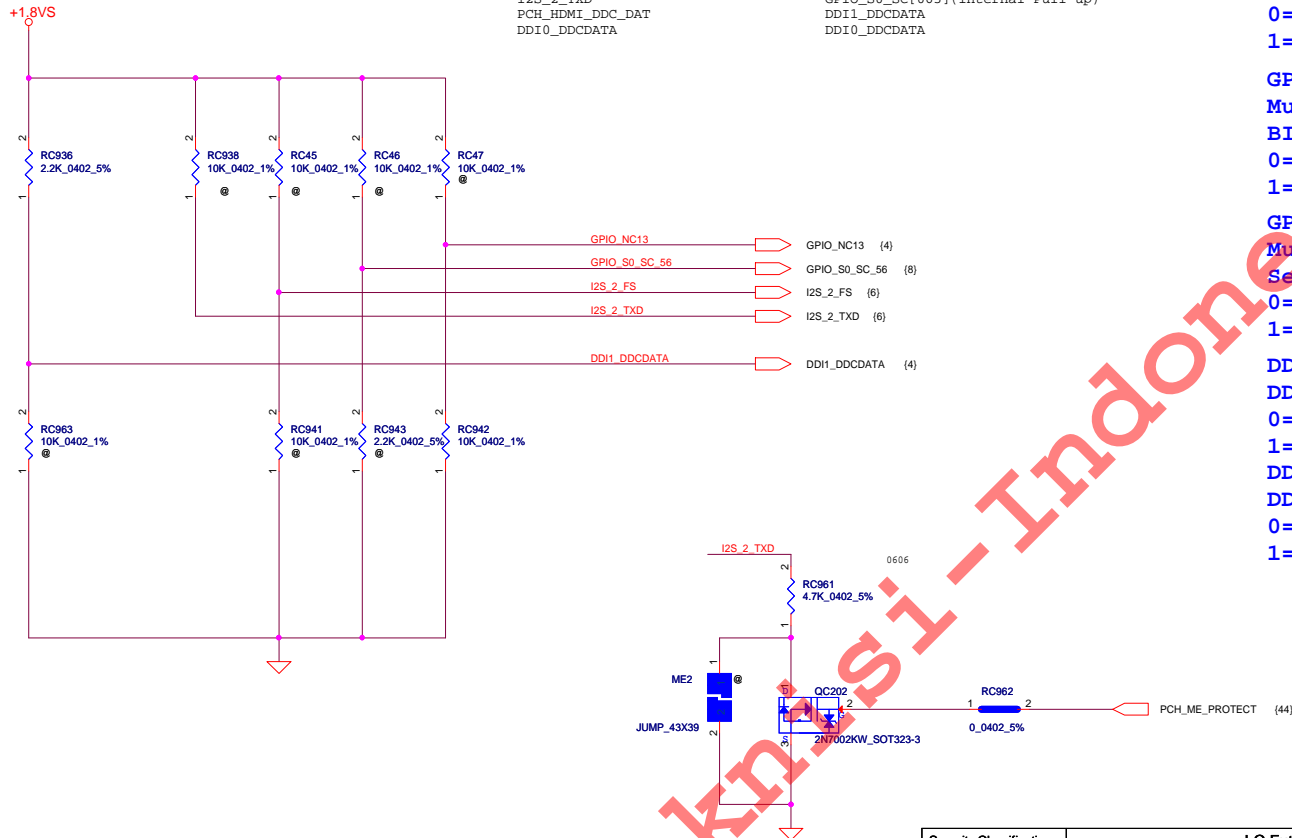
1=DDI0 detected


DDI1_DDCDATA:

DDI1 strap


0=DDI1 not detected

1=DDI1 detected



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DDR3 SO-DIMM A

Figure 10-10 shows the pin configuration for the DDR4 memory module. The diagram is a detailed pinout for a 28-pin package, showing connections for VDD, VSS, and various data and control signals. The pin numbers are listed on the left, and the signal names are listed on the right. The diagram is divided into two main sections: the top section for VDD and VSS connections, and the bottom section for data and control signals. The top section shows connections for VDD (pins 1, 5, 9, 13, 17, 21, 25, 29, 33, 37, 41, 45, 49, 53, 57, 61, 65, 69, 73, 77, 81, 85, 89, 93, 97, 101, 105, 109, 113, 117, 121, 125, 129, 133, 137, 141, 145, 149, 153, 157, 161, 165, 169, 173, 177, 181, 185, 189, 193, 197, 201, 205, 209, 213, 217, 221, 225, 229, 233, 237, 241, 245, 249, 253, 257, 261, 265, 269, 273, 277, 281, 285, 289, 293, 297, 301, 305, 309, 313, 317, 321, 325, 329, 333, 337, 341, 345, 349, 353, 357, 361, 365, 369, 373, 377, 381, 385, 389, 393, 397, 401, 405, 409, 413, 417, 421, 425, 429, 433, 437, 441, 445, 449, 453, 457, 461, 465, 469, 473, 477, 481, 485, 489, 493, 497, 501, 505, 509, 513, 517, 521, 525, 529, 533, 537, 541, 545, 549, 553, 557, 561, 565, 569, 573, 577, 581, 585, 589, 593, 597, 601, 605, 609, 613, 617, 621, 625, 629, 633, 637, 641, 645, 649, 653, 657, 661, 665, 669, 673, 677, 681, 685, 689, 693, 697, 701, 705, 709, 713, 717, 721, 725, 729, 733, 737, 741, 745, 749, 753, 757, 761, 765, 769, 773, 777, 781, 785, 789, 793, 797, 801, 805, 809, 813, 817, 821, 825, 829, 833, 837, 841, 845, 849, 853, 857, 861, 865, 869, 873, 877, 881, 885, 889, 893, 897, 901, 905, 909, 913, 917, 921, 925, 929, 933, 937, 941, 945, 949, 953, 957, 961, 965, 969, 973, 977, 981, 985, 989, 993, 997, 1001, 1005, 1009, 1013, 1017, 1021, 1025, 1029, 1033, 1037, 1041, 1045, 1049, 1053, 1057, 1061, 1065, 1069, 1073, 1077, 1081, 1085, 1089, 1093, 1097, 1101, 1105, 1109, 1113, 1117, 1121, 1125, 1129, 1133, 1137, 1141, 1145, 1149, 1153, 1157, 1161, 1165, 1169, 1173, 1177, 1181, 1185, 1189, 1193, 1197, 1201, 1205, 1209, 1213, 1217, 1221, 1225, 1229, 1233, 1237, 1241, 1245, 1249, 1253, 1257, 1261, 1265, 1269, 1273, 1277, 1281, 1285, 1289, 1293, 1297, 1301, 1305, 1309, 1313, 1317, 1321, 1325, 1329, 1333, 1337, 1341, 1345, 1349, 1353, 1357, 1361, 1365, 1369, 1373, 1377, 1381, 1385, 1389, 1393, 1397, 1401, 1405, 1409, 1413, 1417, 1421, 1425, 1429, 1433, 1437, 1441, 1445, 1449, 1453, 1457, 1461, 1465, 1469, 1473, 1477, 1481, 1485, 1489, 1493, 1497, 1501, 1505, 1509, 1513, 1517, 1521, 1525, 1529, 1533, 1537, 1541, 1545, 1549, 1553, 1557, 1561, 1565, 1569, 1573, 1577, 1581, 1585, 1589, 1593, 1597, 1601, 1605, 1609, 1613, 1617, 1621, 1625, 1629, 1633, 1637, 1641, 1645, 1649, 1653, 1657, 1661, 1665, 1669, 1673, 1677, 1681, 1685, 1689, 1693, 1697, 1701, 1705, 1709, 1713, 1717, 1721, 1725, 1729, 1733, 1737, 1741, 1745, 1749, 1753, 1757, 1761, 1765, 1769, 1773, 1777, 1781, 1785, 1789, 1793, 1797, 1801, 1805, 1809, 1813, 1817, 1821, 1825, 1829, 1833, 1837, 1841, 1845, 1849, 1853, 1857, 1861, 1865, 1869, 1873, 1877, 1881, 1885, 1889, 1893, 1897, 1901, 1905, 1909, 1913, 1917, 1921, 1925, 1929, 1933, 1937, 1941, 1945, 1949, 1953, 1957, 1961, 1965, 1969, 1973, 1977, 1981, 1985, 1989, 1993, 1997, 2001, 2005, 2009, 2013, 2017, 2021, 2025, 2029, 2033, 2037, 2041, 2045, 2049, 2053, 2057, 2061, 2065, 2069, 2073, 2077, 2081, 2085, 2089, 2093, 2097, 2101, 2105, 2109, 2113, 2117, 2121, 2125, 2129, 2133, 2137, 2141, 2145, 2149, 2153, 2157, 2161, 2165, 2169, 2173, 2177, 2181, 2185, 2189, 2193, 2197, 2201, 2205, 2209, 2213, 2217, 2221, 2225, 2229, 2233, 2237, 2241, 2245, 2249, 2253, 2257, 2261, 2265, 2269, 2273, 2277, 2281, 2285, 2289, 2293, 2297, 2301, 2305, 2309, 2313, 2317, 2321, 2325, 2329, 2333, 2337, 2341, 2345, 2349, 2353, 2357, 2361, 2365, 2369, 2373, 2377, 2381, 2385, 2389, 2393, 2397, 2401, 2405, 2409, 2413, 2417, 2421, 2425, 2429, 2433, 2437, 2441, 2445, 2449, 2453, 2457, 2461, 2465, 2469, 2473, 2477, 2481, 2485, 2489, 2493, 2497, 2501, 2505, 2509, 2513, 2517, 2521, 2525, 2529, 2533, 2537, 2541, 2545, 2549, 2553, 2557, 2561, 2565, 2569, 2573, 2577, 2581, 2585, 2589, 2593, 2597, 2601, 2605, 2609, 2613, 2617, 2621, 2625, 2629, 2633, 2637, 2641, 2645, 2649, 2653, 2657, 2661, 2665, 2669, 2673, 2677, 2681, 2685, 2689, 2693, 2697, 2701, 2705, 2709, 2713, 2717, 2721, 2725, 2729, 2733, 2737, 2741, 2745, 2749, 2753, 2757, 2761, 2765, 2769, 2773, 2777, 2781, 2785, 2789, 2793, 2797, 2801, 2805, 2809, 2813, 2817, 2821, 2825, 2829, 2833, 2837, 284

	DDRA_DQ[0..63]	{5}
	DDRA_DQS[0..7]	{5}
	DDRA_DQS#[0..7]	{5}
	DDRA_MA[0..15]	{5}
	DDRA_DM[7:0]	{5}

(10uF_0603_6.3V)*8
(0.1uF 402 10V)*4


The diagram shows a circuit for a DDR2 memory module. A +1.35V supply is connected to a network of resistors. RD1 (4.7K_0402_1%) and RD2 (4.7K_0402_1%) are connected in series between the supply and ground. RD5 (0_0402_5%) is connected between the supply and the DDR_DQ signal line. The DDR_DQ signal line is also connected to the memory module.

The circuit diagram shows a 5-bit DAC implemented using five op-amp buffers (CD68, CD69, CD66, CD67, CD65) and resistors. The inputs are labeled 0 through 4, corresponding to bits 0 through 4. The output is labeled 5. The circuit is powered by a +1.35V supply. The resistors are labeled with values: 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768, 65536, 131072, 262144, 524288, 1048576, 2097152, 4194304, 8388608, 16777216, 33554432, 67108864, 134217728, 268435456, 536870912, 1073741824, 2147483648, 4294967296, 8589934592, 17179869184, 34359738368, 68719476736, 137438953472, 274877906944, 549755813888, 1099511627776, 2199023255552, 4398046511104, 8796093022208, 17592186044416, 35184372088832, 70368744177664, 140737488355328, 281474976710656, 562949953421312, 1125899906842624, 2251799813685248, 4503599627370496, 9007199254740992, 18014398509481984, 36028797018963968, 72057594037927936, 144115188075855872, 288230376151711744, 576460752303423488, 1152921504606846976, 2305843009213693952, 4611686018427387904, 9223372036854775808, 18446744073709551616, 36893488147419103232, 73786976294838206464, 147573952589676412928, 295147905179352825856, 590295810358705651712, 1180591620717411303424, 2361183241434822606848, 4722366482869645213696, 9444732965739290427392, 18889465931478580854784, 37778931862957161709568, 75557863725914323419136, 151115727451828646838272, 302231454903657293676544, 604462909807314587353088, 1208925819614629174706176, 2417851639229258349412352, 4835703278458516698824704, 9671406556917033397649408, 19342813113834066795298816, 38685626227668133590597632, 77371252455336267181195264, 154742504910672534362390528, 309485009821345068724781056, 618970019642690137449562112, 1237940039285380274899124224, 2475880078570760549798248448, 4951760157141521099596496896, 9903520314283042199192993792, 19807040628566084398385987584, 39614081257132168796771975168, 79228162514264337593543950336, 158456325028528675187087900672, 316912650057057350374175801344, 633825300114114700748351602688, 1267650600228229401496703205376, 2535301200456458802993406410752, 5070602400912917605986812821504, 10141204801825835211973625643008, 20282409603651670423947251286016, 40564819207303340847894502572032, 81129638414606681695789005144064, 162259276829213363391578010288128, 324518553658426726783156020576256, 649037107316853453566312041152512, 1298074214633706907132624082305024, 2596148429267413814265248164610048, 5192296858534827628530496329220096, 10384593717069655257060992658440192, 20769187434139310514121985316880384, 41538374868278621028243970633760768, 83076749736557242056487941267521536, 166153499473114484112975882535043072, 332306998946228968225951765070086144, 664613997892457936451903530140172288, 1329227995784915872903807060280344576, 2658455991569831745807614120560689152, 5316911983139663491615228241121378304, 10633823966279326983230456482242756608, 21267647932558653966460912964485513216, 42535295865117307932921825928971026432, 85070591730234615865843651857942052864, 170141183460469231731687303715884105728, 340282366920938463463374607431768211456, 680564733841876926926749214863536422912, 1361129467683753853853498429727072845824, 2722258935367507707706996859454145691648, 5444517870735015415413993718908291383296, 10889035741470030830827987437816582766592, 21778071482940061661655974875633165533184, 43556142965880123323311949751266331066368, 87112285931760246646623899502532662132736, 174224571863520493293247799005065324265472, 348449143727040986586495598010130648530944, 696898287454081973172991196020261297061888, 1393796574908163946345982392040522594123776, 2787593149816327892691964784081045188247552, 5575186299632655785383929568162090376495104, 11150372599265311570767859136324180752990208, 22300745198530623141535718272648361505980416, 44601490397061246283071436545296723011960832, 89202980794122492566142873090593446023921664, 178405961588244985132285746181186892047843328, 356811923176489970264571492362373784095686656, 713623846352979940529142984724747568191373312, 1427247692705959881058285969449495136382746624, 2854495385411919762116571938898990272765493248, 5708990770823839524233143877797980545530986496, 11417981541647679048466287755595961091061972992, 22835963083295358096932575511191922182123945984,


cost down bom to change 0.1uF

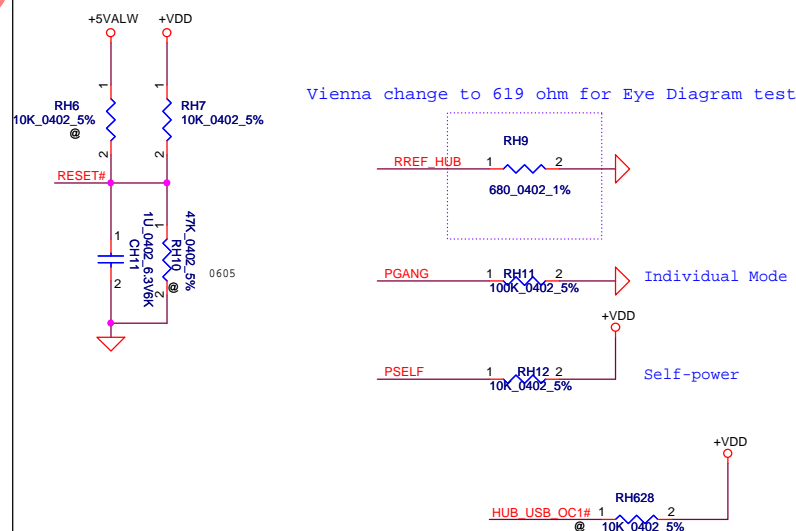
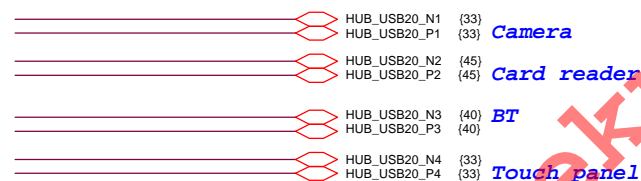
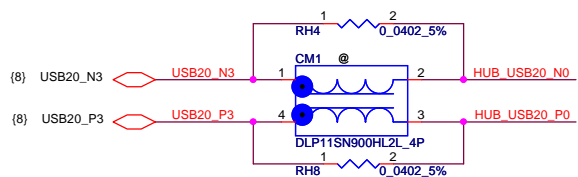
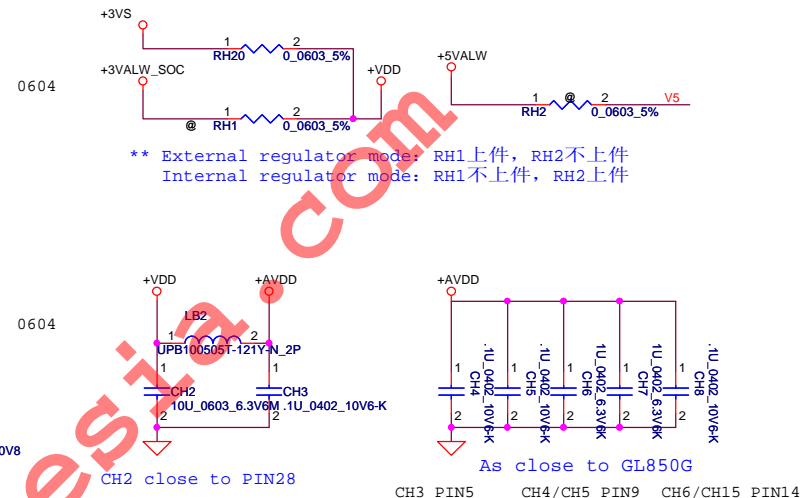
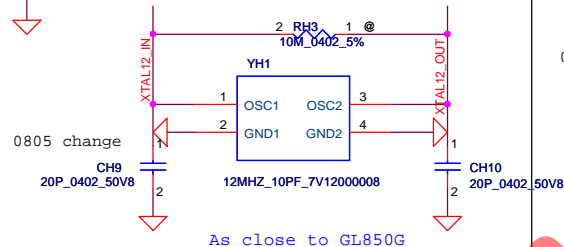
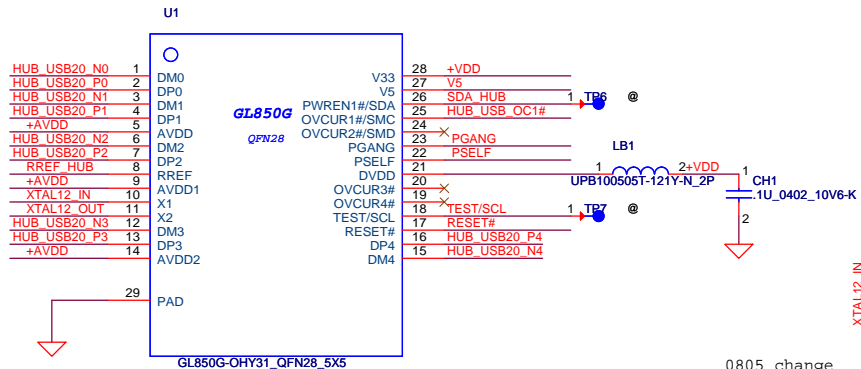
For RF request

Diagram illustrating a two-wire bus system with two nodes, RD10 and RD11, connected to a common ground. The bus is labeled SA0 and SA1. The nodes are labeled RD10 and RD11, with associated values 1, 2, 0.0402, and 5%.

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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

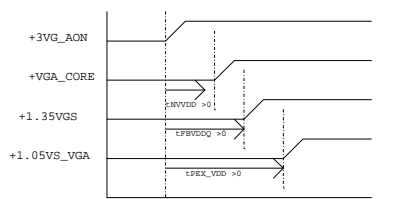
Products	GPU (4)	Mem (1.5)	NVCLK /MCLK (MHz)	NVVDD (V)		FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)
N14X 128bit 2GB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

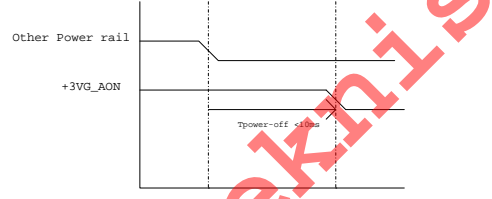
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence

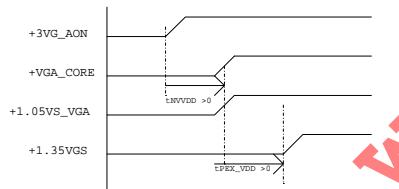


1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms
2. Optimus System VDD3 avoids drop down earlier than NVDD and FBVDDQ

N15S-GT Power Sequence

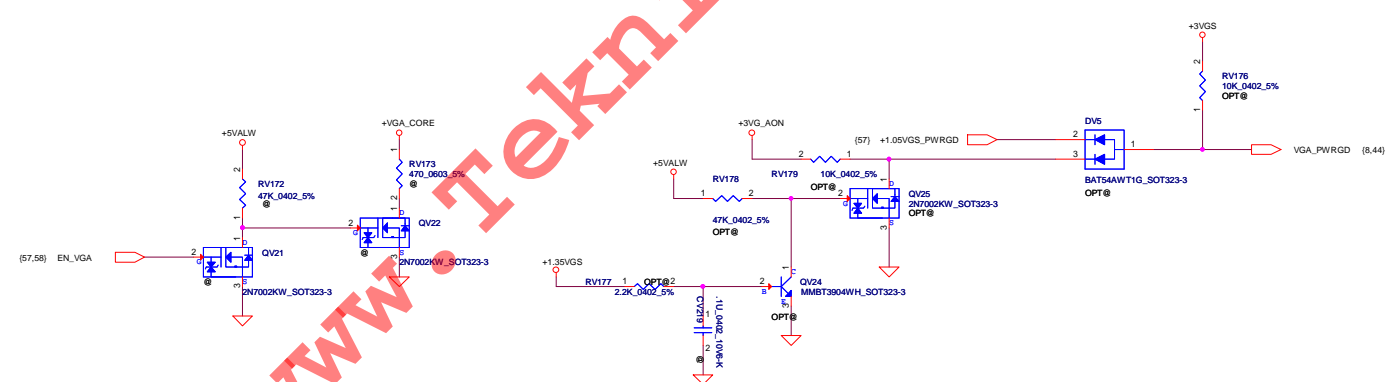
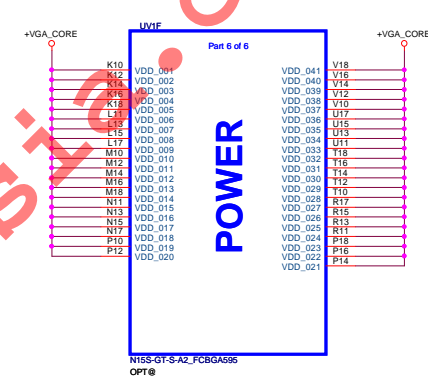
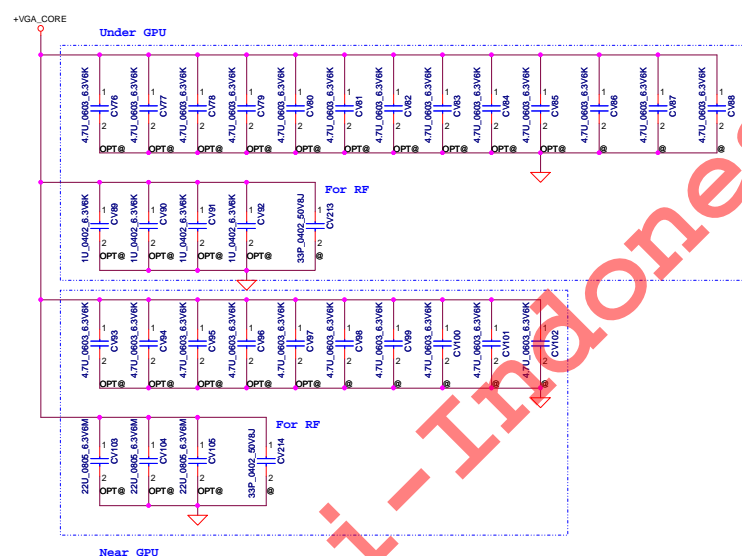
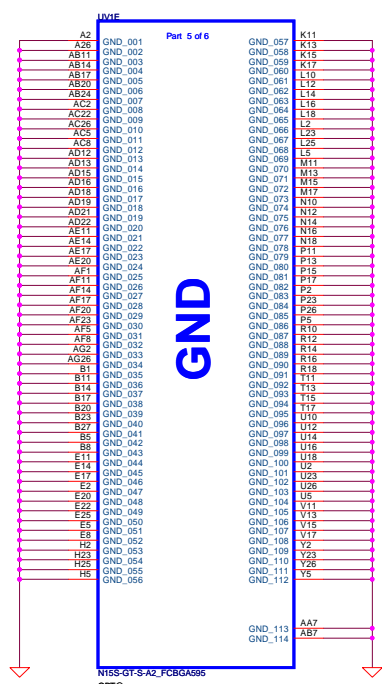


1. all power rail ramp up time should be larger than 40us

N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

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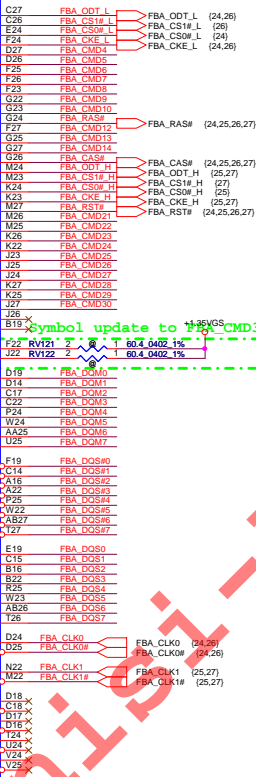


LV1B

Part 2 of 6

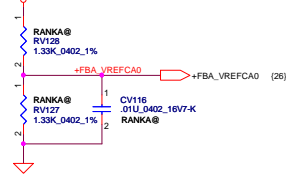
MEMORY INTERFACE A

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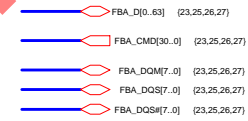
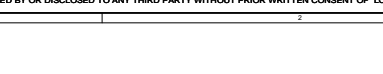
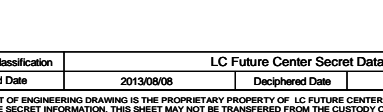
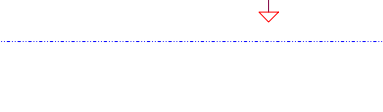
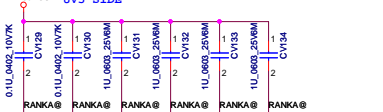
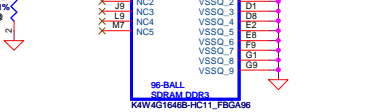
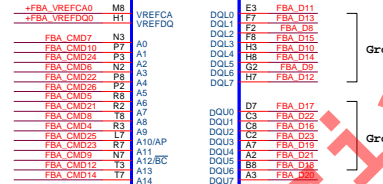
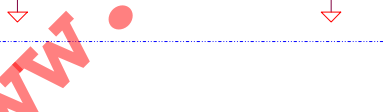
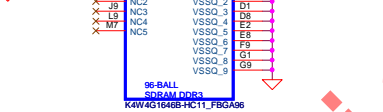
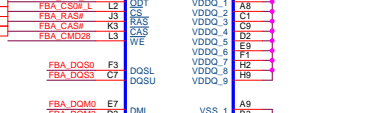
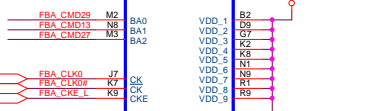
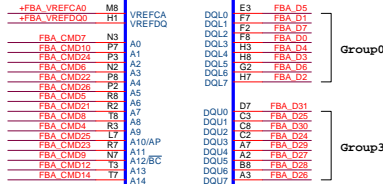
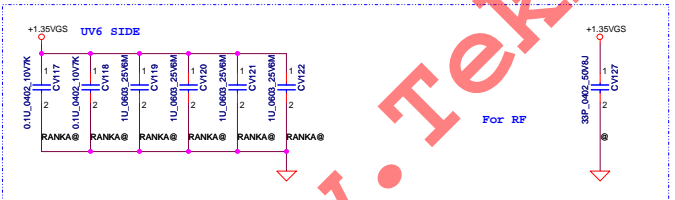
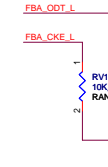
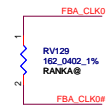
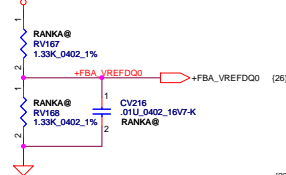


at least 16 mils width(optimal)
20 mils spacing to other signals/planes

+1.35VGS

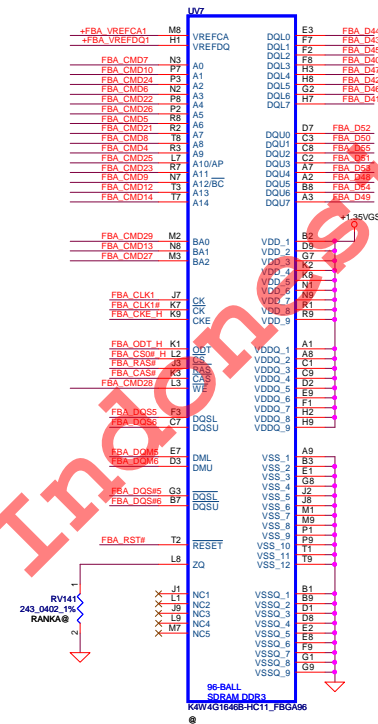
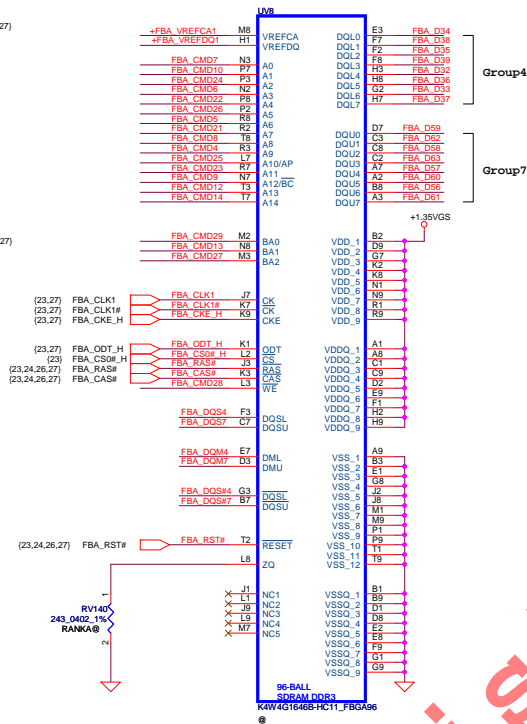


+1.35VGS

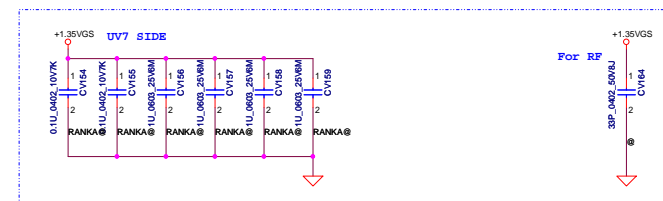
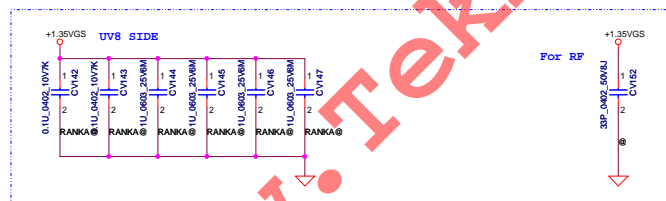


CMD mapping mod Mode E

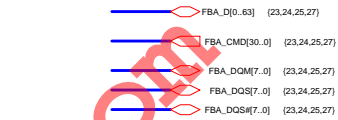
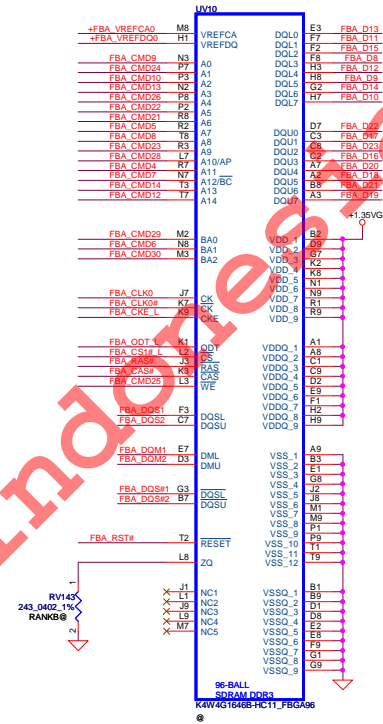
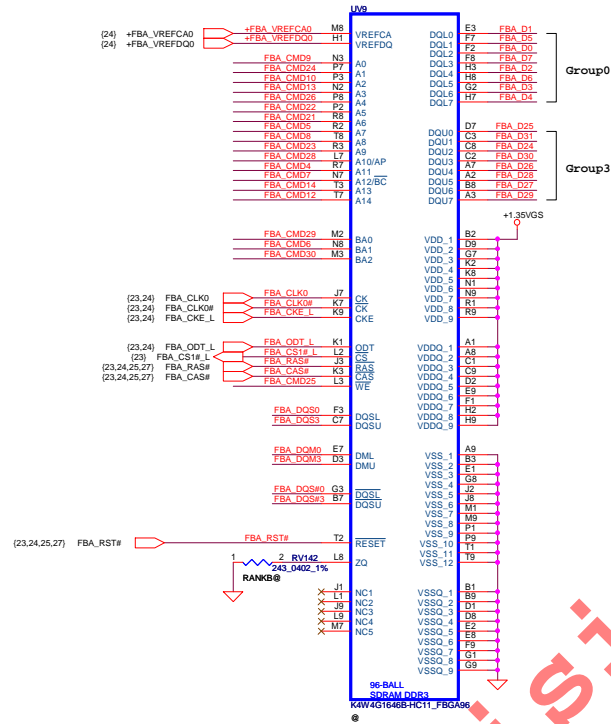
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Address	0...31	32..63
FBX_CMD0	ODT_L	ODT_L
FBX_CMD1		CS1#_L
FBX_CMD2	CS0#_L	
FBX_CMD3	CKE_L	CKE_L
FBX_CMD4	A9	A11
FBX_CMD5	A6	A7
FBX_CMD6	A3	BA1
FBX_CMD7	A0	A12
FBX_CMD8	A8	A8
FBX_CMD9	A12	A0
FBX_CMD10	A1	A2
FBX_CMD11	RAS#	RAS#
FBX_CMD12	A13	A14
FBX_CMD13	BA1	A3
FBX_CMD14	A14	A13
FBX_CMD15	CAS#	CAS#
FBX_CMD16	ODT_H	ODT_H
FBX_CMD17		CS1#_H
FBX_CMD18	CS0#_H	
FBX_CMD19	CKE_H	CKE_H
FBX_CMD20	RST	RST
FBX_CMD21	A7	A6
FBX_CMD22	A4	A5
FBX_CMD23	A11	A9
FBX_CMD24	A2	A1
FBX_CMD25	A10	WE#
FBX_CMD26	A5	A4
FBX_CMD27	BA2	BA2
FBX_CMD28	WE#	A10
FBX_CMD29	BA0	BA0
FBX_CMD30		BA2



	Rank0		Rank1	
Address	0..31	32..63	0..31	32..63
Fbx_CMD0	ODT_L		ODT_L	
Fbx_CMD1			CSI#_L	
Fbx_CMD2	CS0#_L			
Fbx_CMD3	CKE_L		CKE_L	
Fbx_CMD4	A9	A9	A11	A11
Fbx_CMD5	A6	A6	A7	A7
Fbx_CMD6	A3	A3	BA1	BA1
Fbx_CMD7	A0	A0	A12	A12
Fbx_CMD8	A8	A8	A8	A8
Fbx_CMD9	A12	A12	A0	A0
Fbx_CMD10	A1	A1	A2	A2
Fbx_CMD11	RAS#	RAS#	RAS#	RAS#
Fbx_CMD12	A13	A13	A14	A14
Fbx_CMD13	BA1	BA1	A3	A3
Fbx_CMD14	A14	A14	A13	A13
Fbx_CMD15	CAS#	CAS#	CAS#	CAS#
Fbx_CMD16		ODT_H		ODT_H
Fbx_CMD17				CSI#_H
Fbx_CMD18		CS0#_H		
Fbx_CMD19		CKE_H		CKE_H
Fbx_CMD20	RST	RST	RST	RST
Fbx_CMD21	A7	A7	A6	A6
Fbx_CMD22	A4	A4	A5	A5
Fbx_CMD23	A11	A11	A9	A9
Fbx_CMD24	A2	A2	A1	A1
Fbx_CMD25	A10	A10	WE#	WE#
Fbx_CMD26	A5	A5	A4	A4
Fbx_CMD27	BA2	BA2		
Fbx_CMD28	WE#	WE#	A10	A10
Fbx_CMD29	BA0	BA0	BA0	BA0
Fbx_CMD30			BA2	BA2

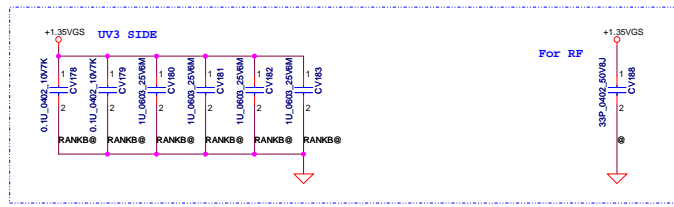
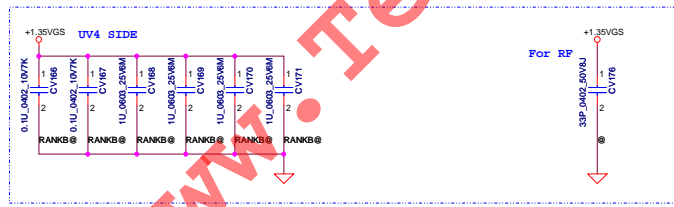


at least 16 mils width (optimal)
20 mils spacing to other signals / planes

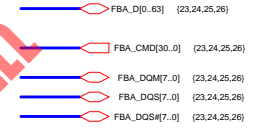
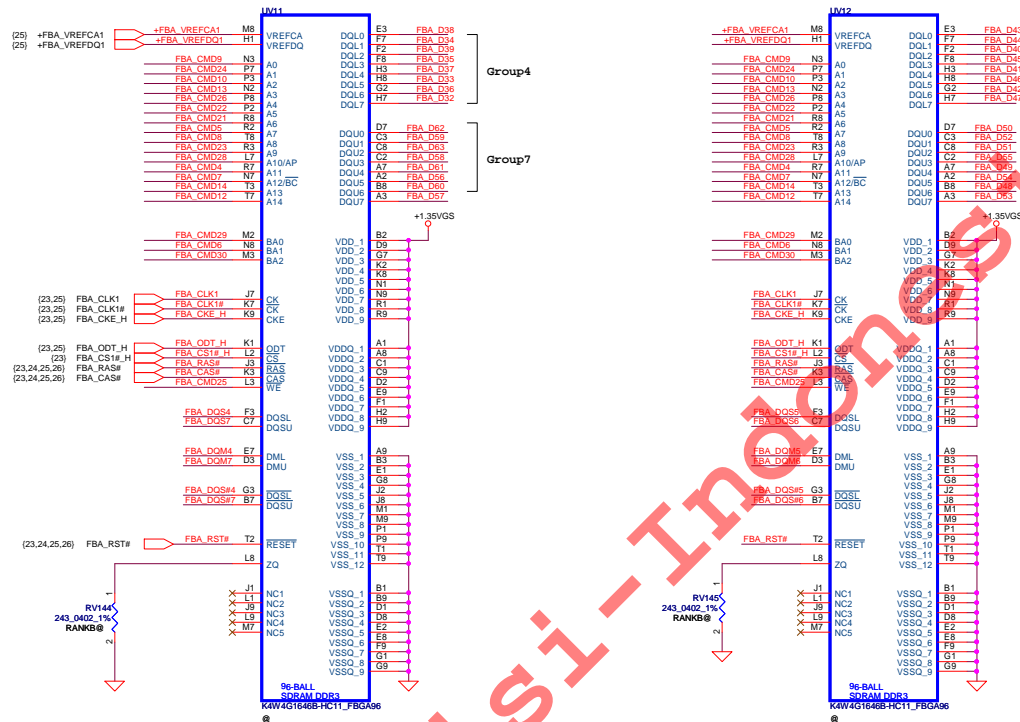


CMD mapping mod Mode E

Addresses	Rank0	Rank1
FBX_CMD0	0..31	32..63
FBX_CMD1	ODT_L	ODT_L
FBX_CMD2	CS0#_L	CS1#_L
FBX_CMD3	CKE_L	CKE_L
FBX_CMD4	A9	A11
FBX_CMD5	A6	A7
FBX_CMD6	A3	BA1
FBX_CMD7	A0	A12
FBX_CMD8	A8	A8
FBX_CMD9	A12	A0
FBX_CMD10	A1	A2
FBX_CMD11	RAS#	RAS#
FBX_CMD12	A13	A14
FBX_CMD13	BA1	A3
FBX_CMD14	A14	A13
FBX_CMD15	CAS#	CAS#
FBX_CMD16	ODT_H	ODT_H
FBX_CMD17		CS1#_H
FBX_CMD18	CS0#_H	
FBX_CMD19	CKE_H	CKE_H
FBX_CMD20	RST	RST
FBX_CMD21	A7	A6
FBX_CMD22	A4	A5
FBX_CMD23	A11	A9
FBX_CMD24	A2	A1
FBX_CMD25	A10	WE#
FBX_CMD26	A5	A4
FBX_CMD27	BA2	BA2
FBX_CMD28	WE#	A10
FBX_CMD29	BA0	BA0
FBX_CMD30		BA2

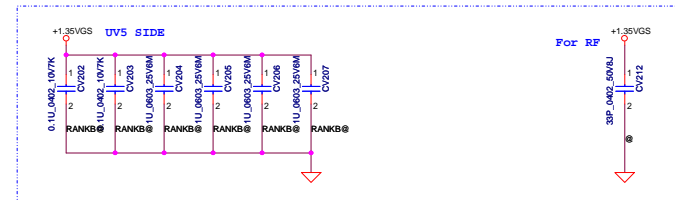
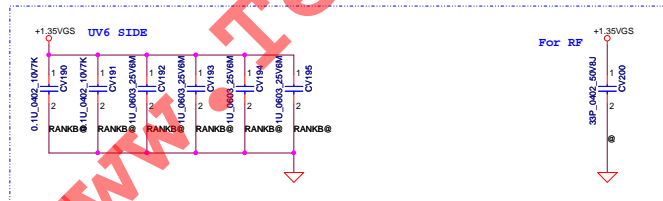


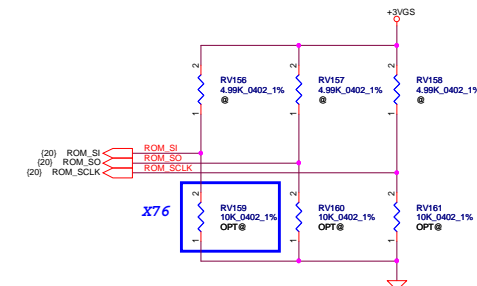
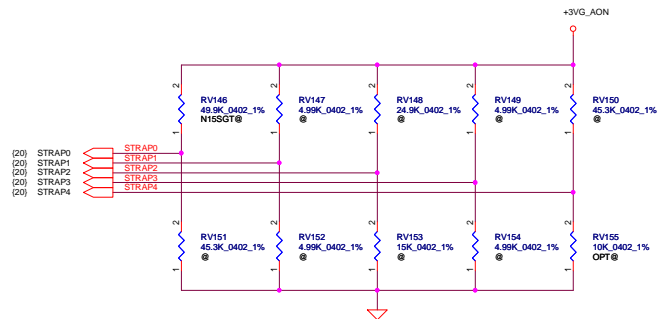
at least 16 mils width(optimal)
20 mils spacing to other signals/planes



CMD mapping mod Mode E

Address	Rank0		Rank1	
	0..31	32..63	0..31	32..63
FbX_CMD0	ODT_L		ODT_L	
FbX_CMD1			CS1#_L	
FbX_CMD2	CS0#_L			
FbX_CMD3	CKE_L		CKE_L	
FbX_CMD4	A9	A9	A11	A11
FbX_CMD5	A6	A6	A7	A7
FbX_CMD6	A3	A3	BA1	BA1
FbX_CMD7	A0	A0	A12	A12
FbX_CMD8	A8	A8	A8	A8
FbX_CMD9	A12	A12	A0	A0
FbX_CMD10	A1	A1	A2	A2
FbX_CMD11	RAS#	RAS#	RAS#	RAS#
FbX_CMD12	A13	A13	A14	A14
FbX_CMD13	BA1	BA1	A3	A3
FbX_CMD14	A14	A14	A13	A13
FbX_CMD15	CAS#	CAS#	CAS#	CAS#
FbX_CMD16		ODT_H		ODT_H
FbX_CMD17			CS1#_H	
FbX_CMD18		CS0#_H		
FbX_CMD19		CKE_H		CKE_H
FbX_CMD20	RST	RST	RST	RST
FbX_CMD21	A7	A7	A6	A6
FbX_CMD22	A4	A4	A5	A5
FbX_CMD23	A11	A11	A9	A9
FbX_CMD24	A2	A2	A1	A1
FbX_CMD25	A10	A10	WE#	WE#
FbX_CMD26	A5	A5	A4	A4
FbX_CMD27	BA2	BA2		
FbX_CMD28	WE#	WE#	A10	A10
FbX_CMD29	BA0	BA0	BA0	BA0
FbX_CMD30			BA2	BA2





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
SD03449918J		
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
SD03449928J		
30.1K	1101	0101
SD03440128J		
34.8K	1110	0110
SD03449928J	1111	0111
45.3K		
SD03445328J		

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

X76

GPU	FB Memory (DDR3)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N15S-GT	Hynix 900MHz	H5TC4G63AFR-11C	0x3						
		256M x 16	PD 20K						
	Micron 900MHz	MT41J256M16HA-093G:E	0x4						
		256M x 16	PD 24.9K						
	Samsung 900MHz	K4W4G1646D-BC1A	0x5						
		256M x 16	PD 30.1K						
				PD 4.99K	PD 4.99K	PU 49.9K	Un-stuff	Un-stuff	Un-stuff

GPU	FB Memory (DDR3)	STRAP3	STRAP2	STRAP1	STRAP0	STRAP4	ROM_SI	ROM_SO	ROM_SCLK
N15V-QM	Hynix 900MHz	H5TC4G63AFR-11C	0x4	PD 10K	PU 10K	PD 10K	PD 10K		
		256M x 16	0x4						
	Micron 900MHz	MT41J256M16HA-093G:E	0xD	PU 10K	PU 10K	PD 10K	PU 10K		
		256M x 16	0xD						
	Hynix 900MHz	H5TC2G63FFR-11C	0xC	PU 10K	PU 10K	PD 10K	PD 10K	PD 10K	PD 10K
		128M x 16	0xC						
	Micron 900MHz	MT41J128M16JT-093G	0x1	PD 10K	PD 10K	PD 10K	PU 10K		
		128M x 16	0x1						
	Samsung 900MHz	K4W2G1646Q-BC1A	0xE	PU 10K	PU 10K	PD 10K			
		128M x 16	0xE						

VRAM	X76	VRAM P/N
Samsung	X7604112001	SA00005SH40
Micron	X7604012002	SA00005M120
Hynix	X7604012001	SA00005VS00

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4

3

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Monday, December 23, 2013

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of

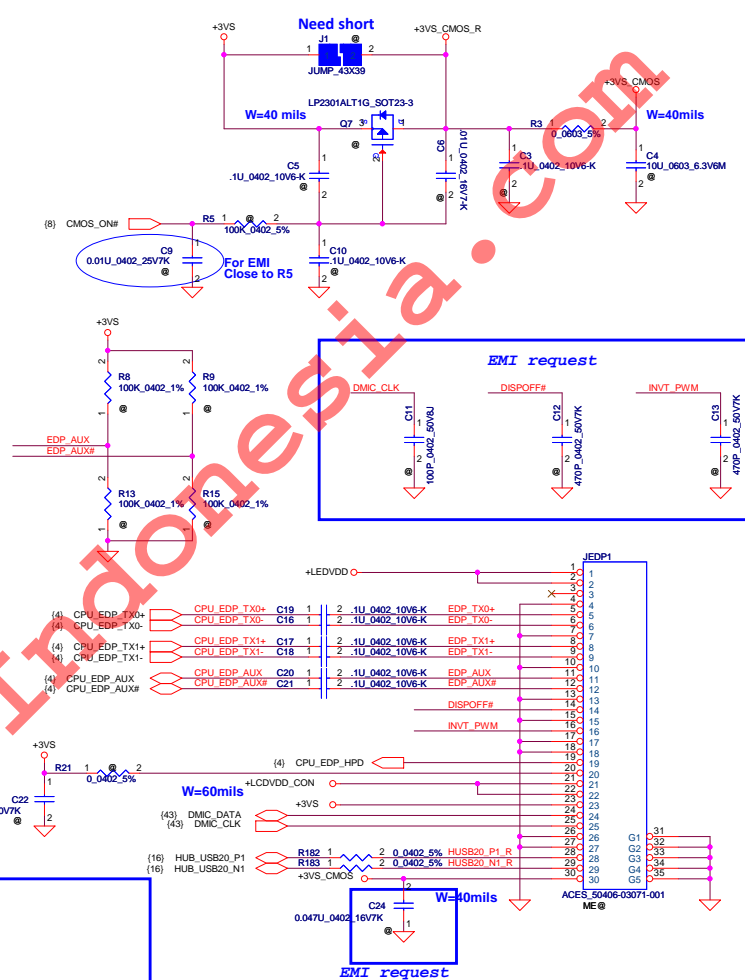
59

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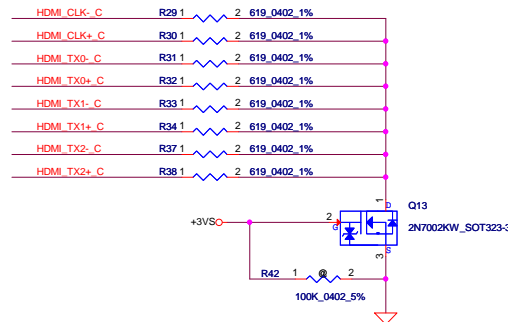
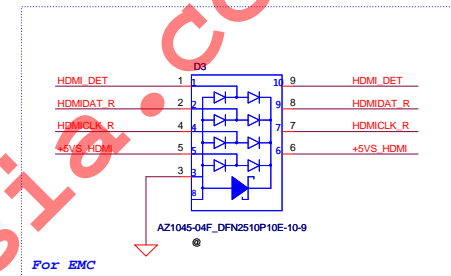
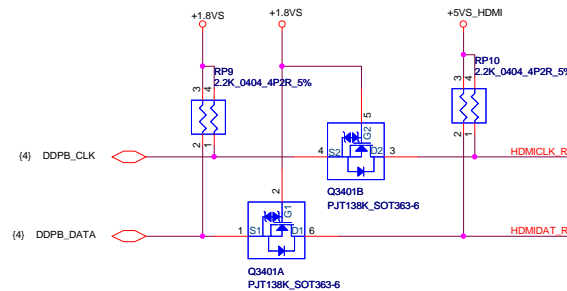
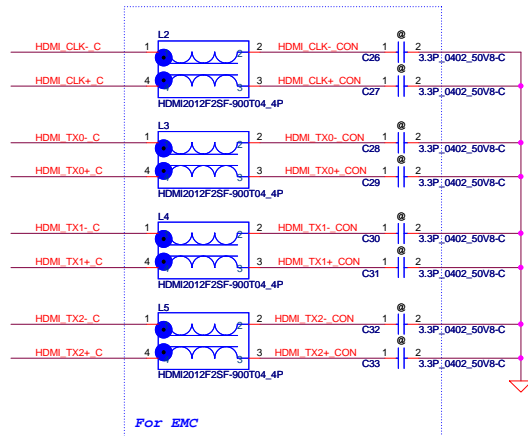
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CMOS Camera

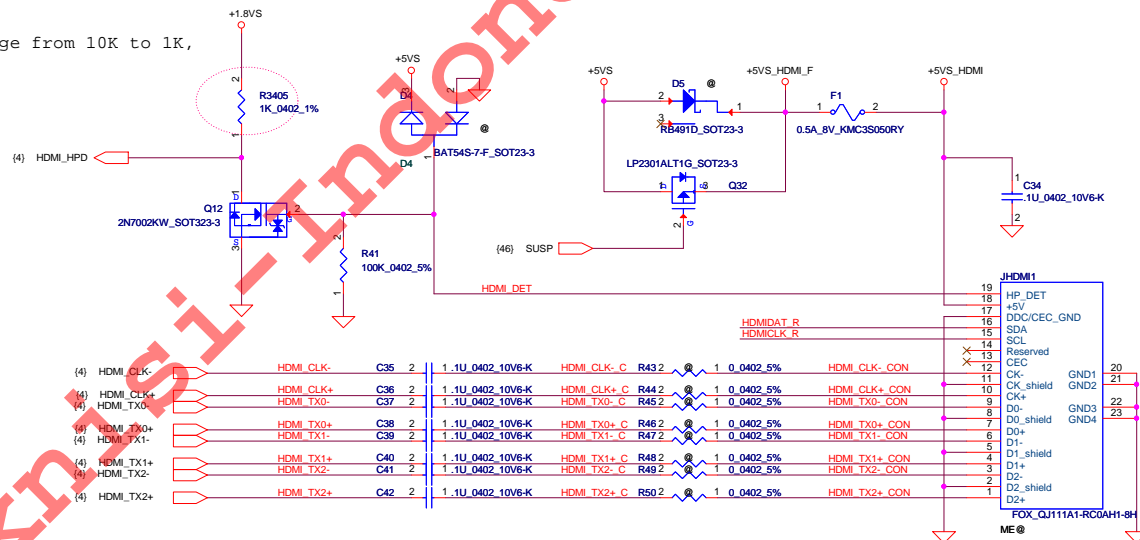


Touch Screen

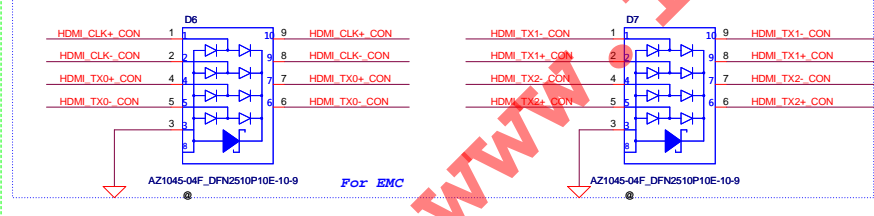
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R4602 change from 10K to 1K, as Vienna



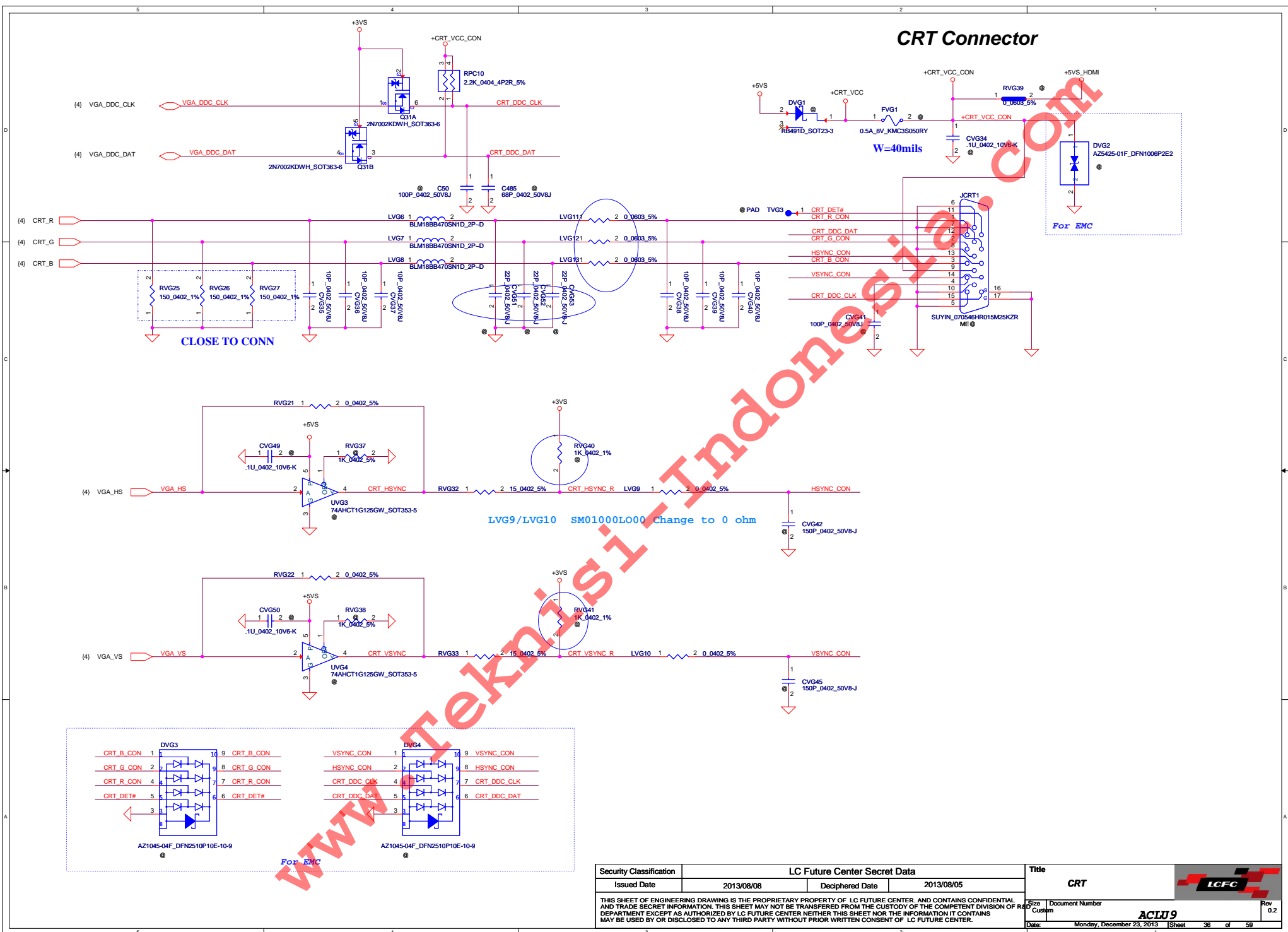
Close to JHDMI1



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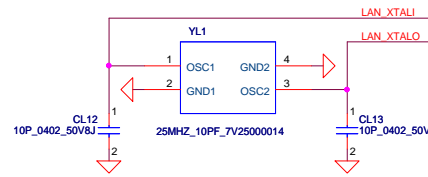
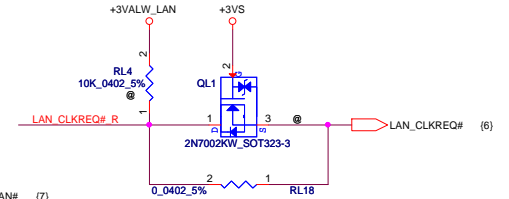
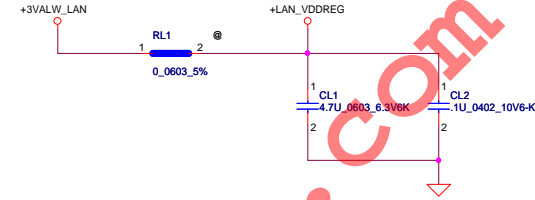
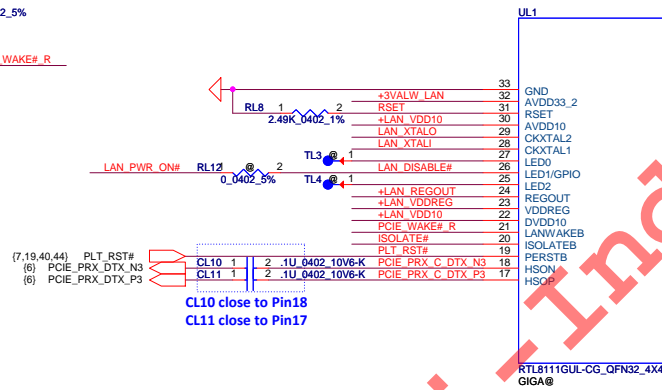
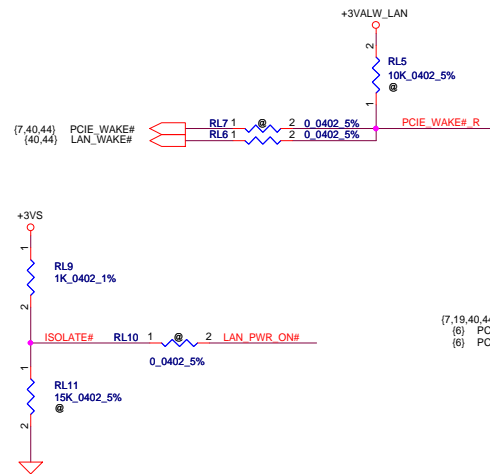
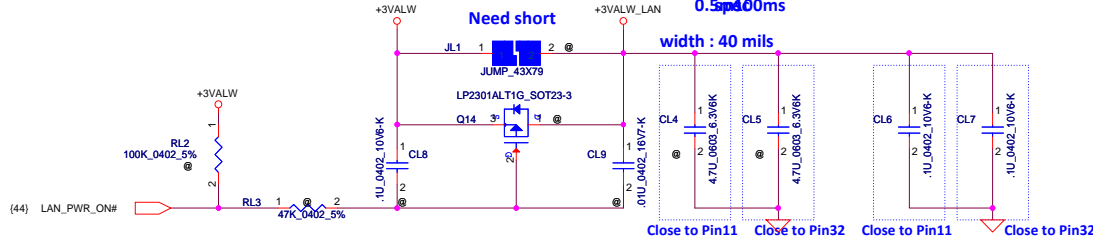


+3VALW TO +3VALW_LAN

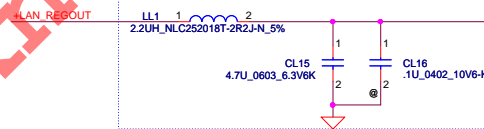
+3VALW_LAN rising time (10%~90%):
0.5~100ms

Need short

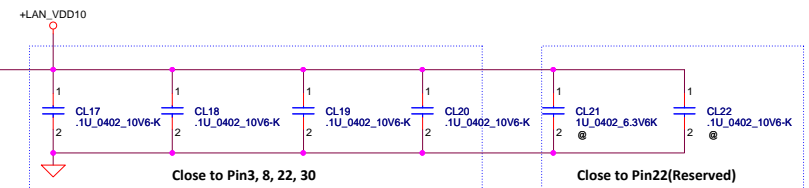
width : 40 mils



For RTL8111GUL/ RTL8106EUL (SWR mode)

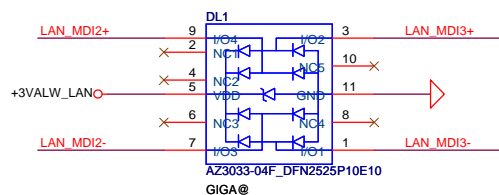


Layout Note: LL1 must be within 200mil to Pin24,
CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

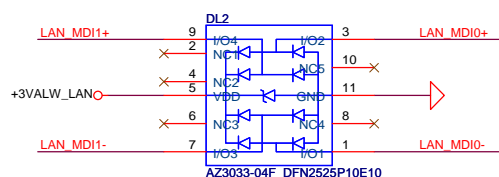


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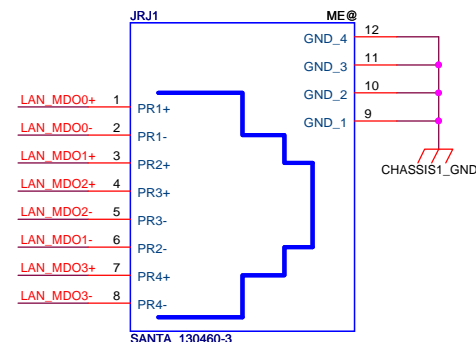
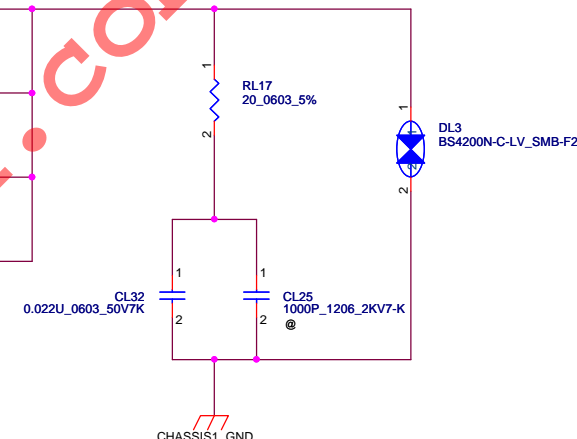
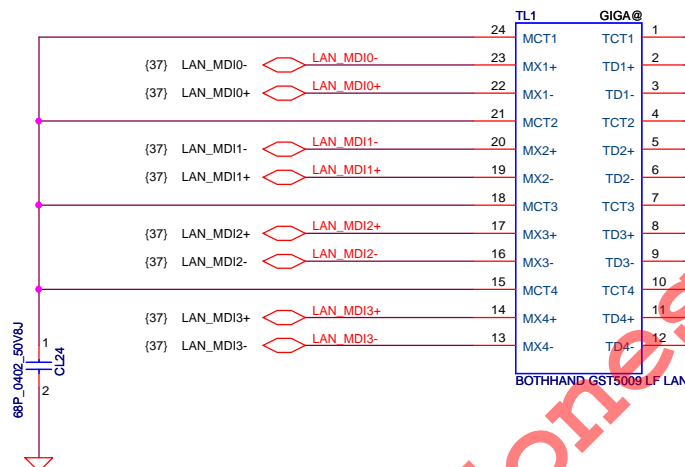
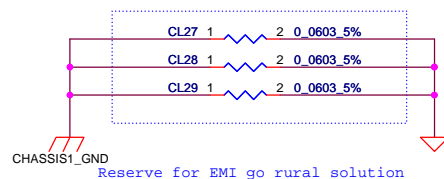
DL1/DL2
1'S PN:SC300003M00



Place Close to TL1

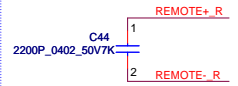


Place Close to TL2

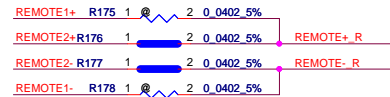
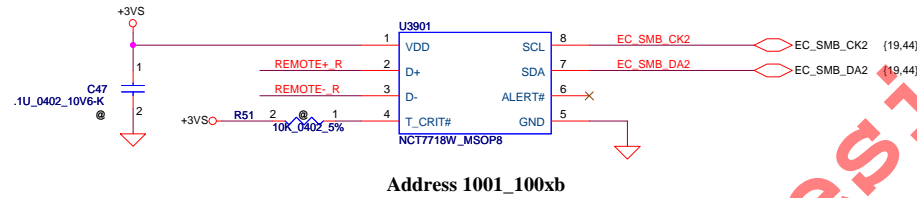


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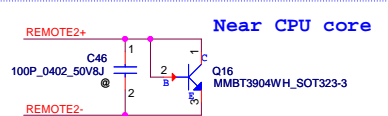
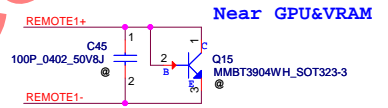
Close to U3901



SMSC thermal sensor placed near DIMM

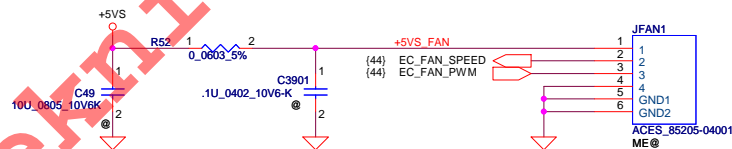


REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"



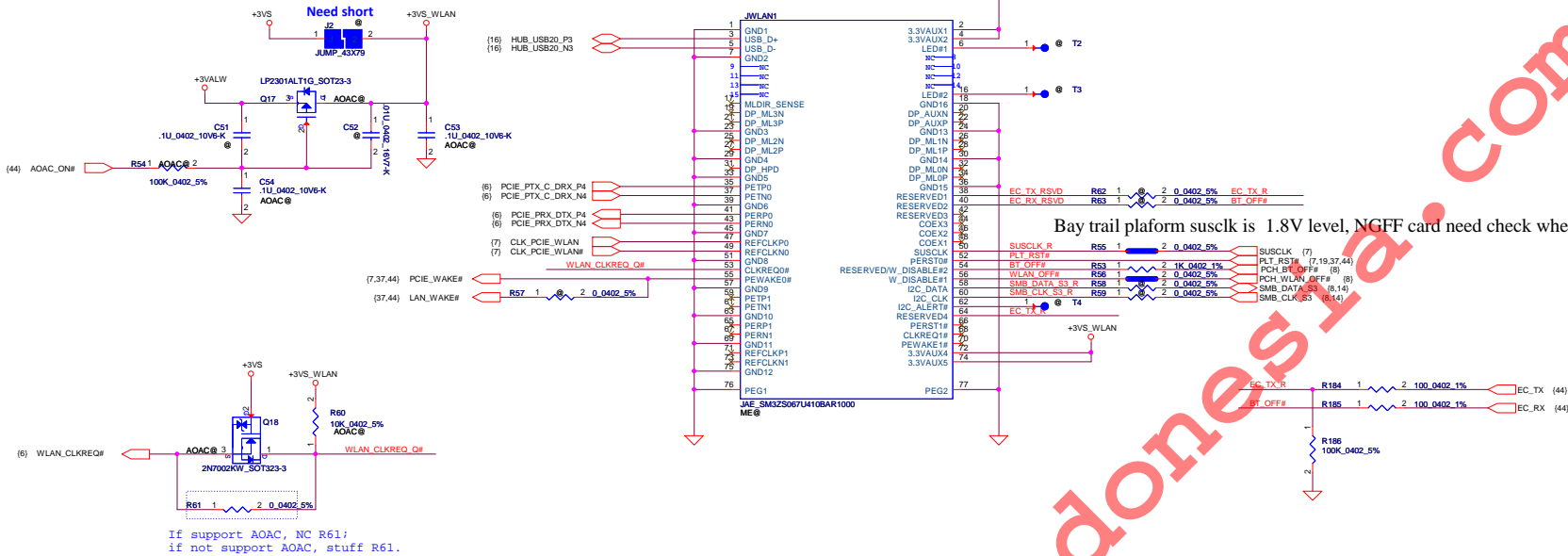
Baytrail SOC use thermal sensor to read the thermal,
Baytrail don't has PECI signal



FAN Conn



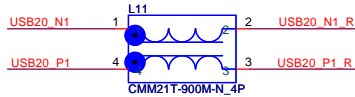
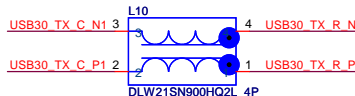
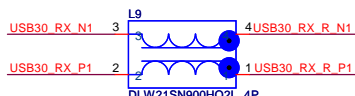
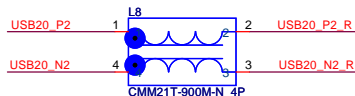
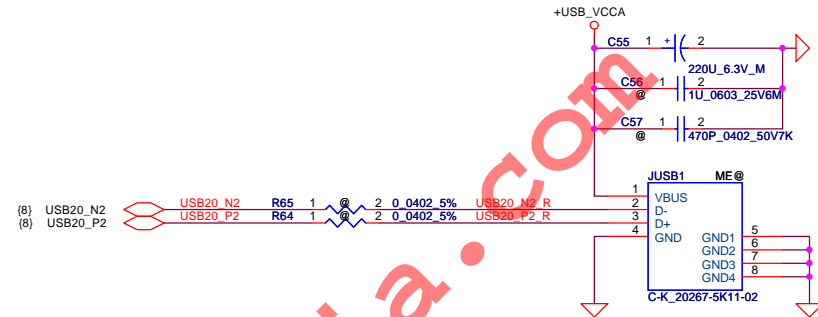
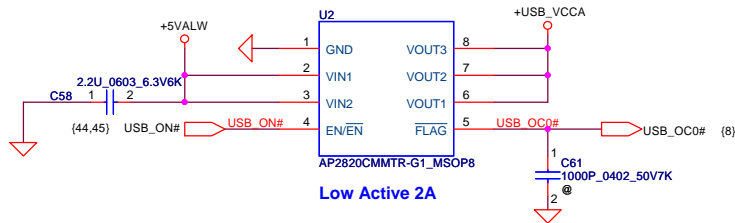
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Mini-Express Card(WLAN/WiMAX)

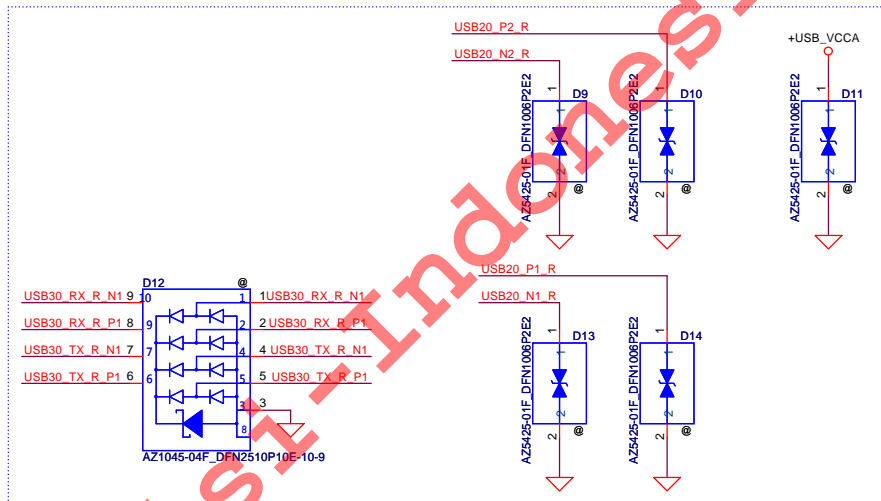


Security Classification	LC Future Center Secret Data			Title	 NGFF WLAN	
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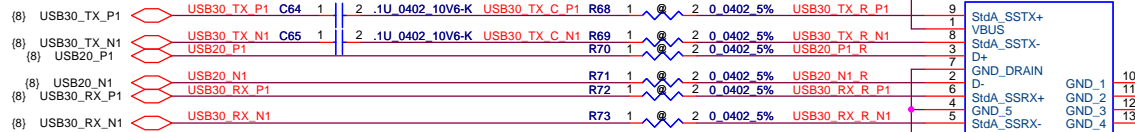
LEFT SIDE USB3.0 PORT X2



For EMC

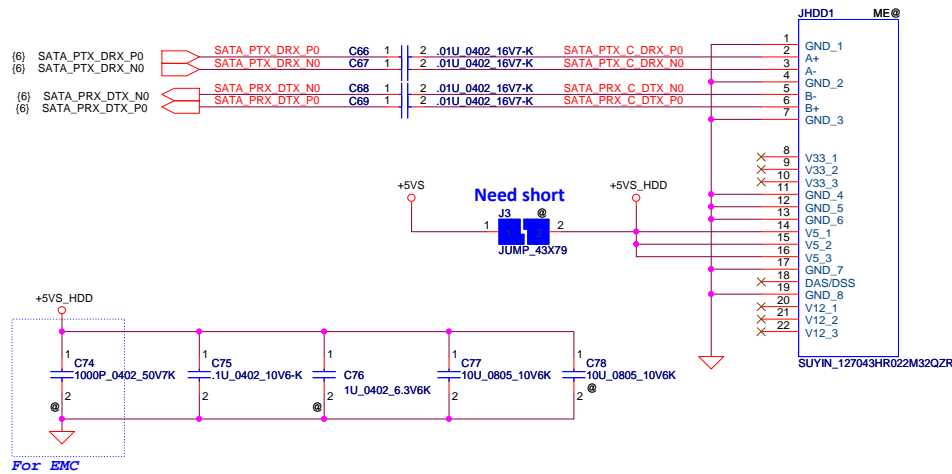


For EMC

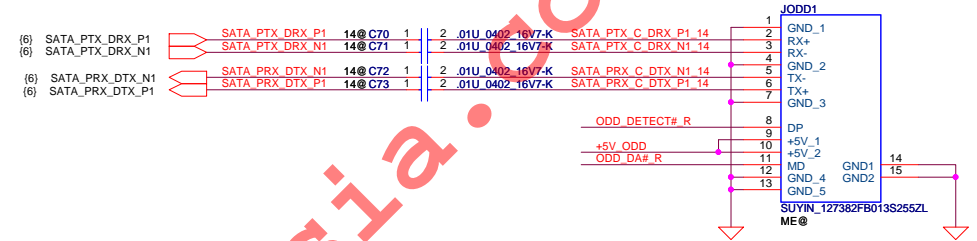


Security Classification		LC Future Center Secret Data		Title	
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Custm	ACLU9				
Date:	Monday, December 23, 2013	Sheet	41	of 59	

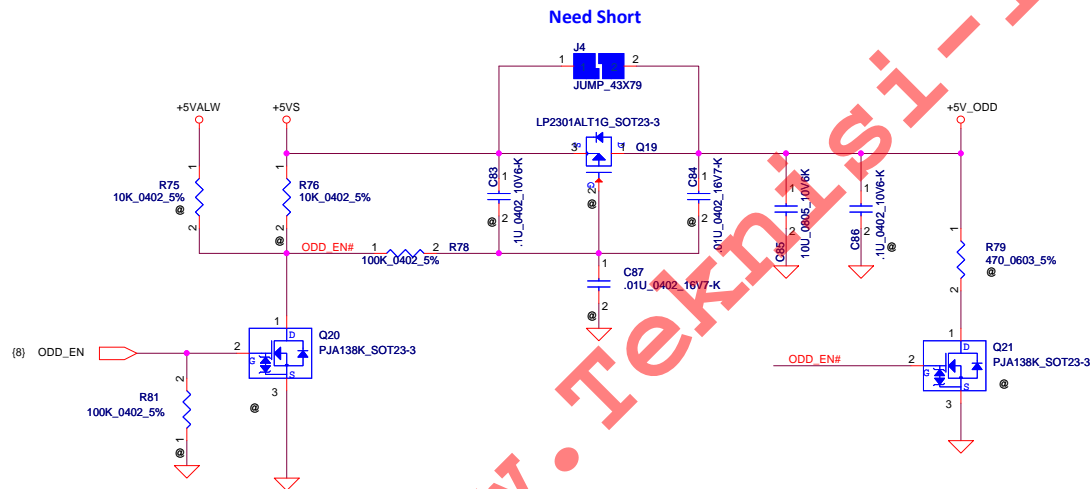
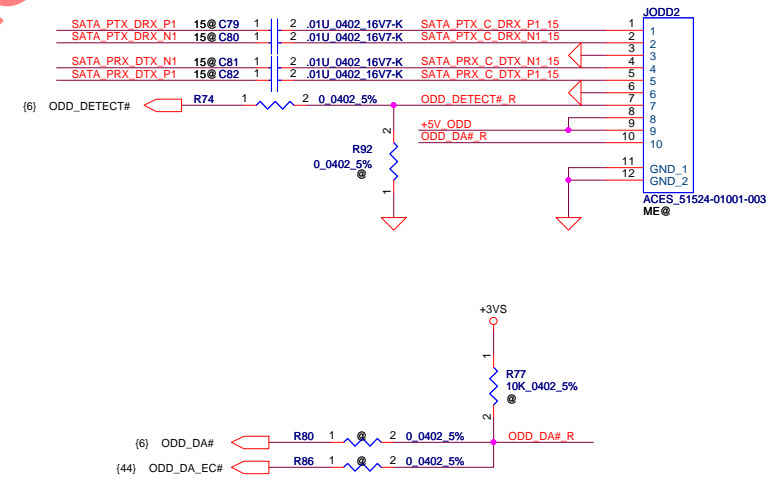
SATA HDD Conn.



FOR 14" SATA ODD Conn.

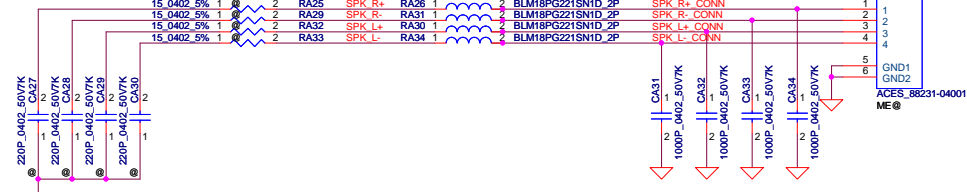
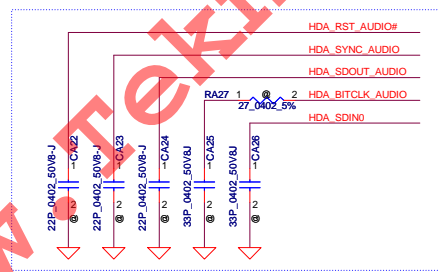
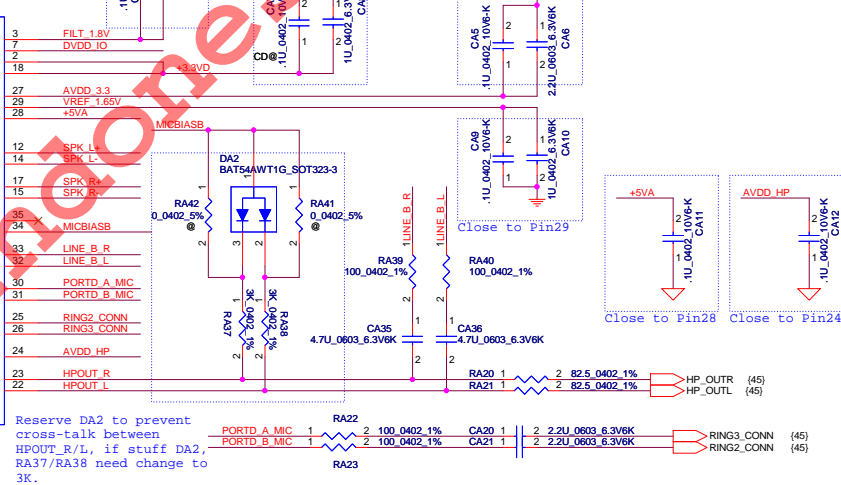
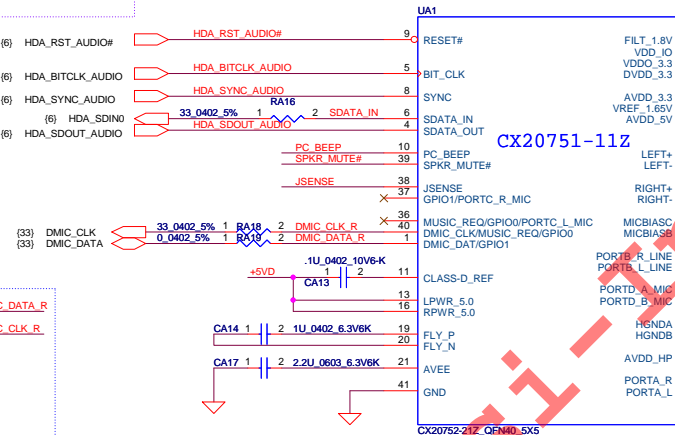
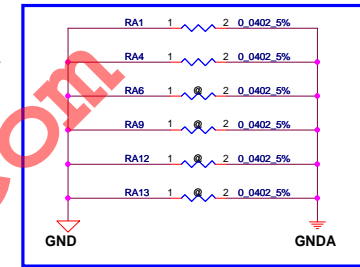
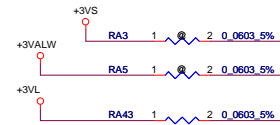
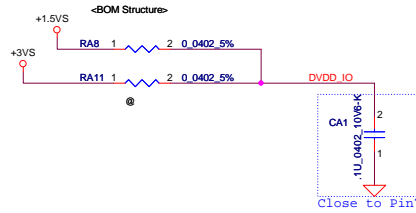
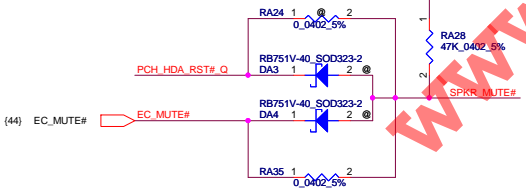
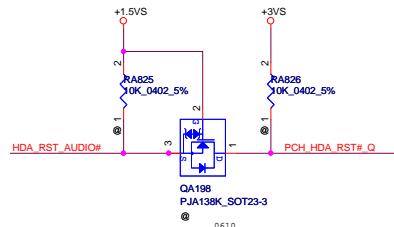
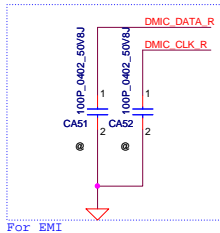
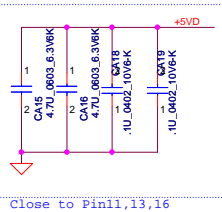
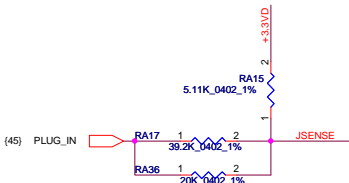
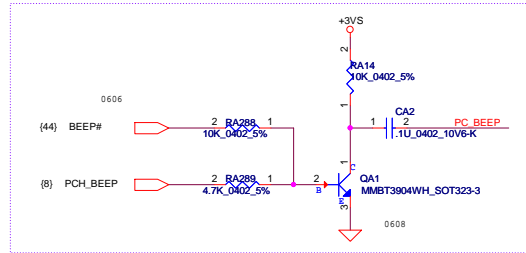


FOR 15" SATA ODD FFC Conn

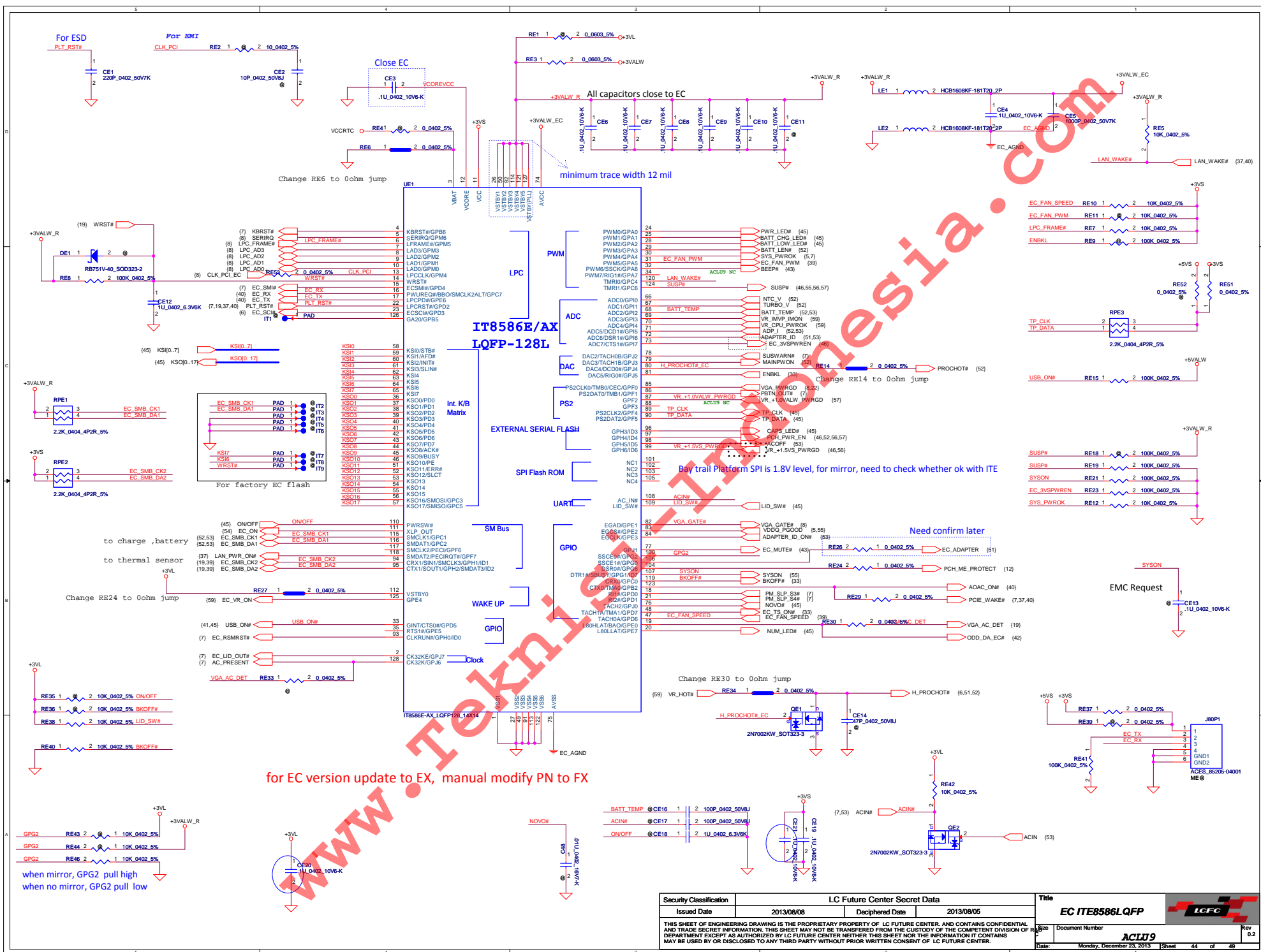


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				Sheet 42	of 59

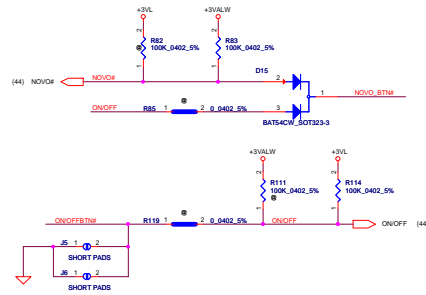
Same as Vienna



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LCFC				ACLU9
Date: Monday, December 23, 2013				Sheet 43 of 59

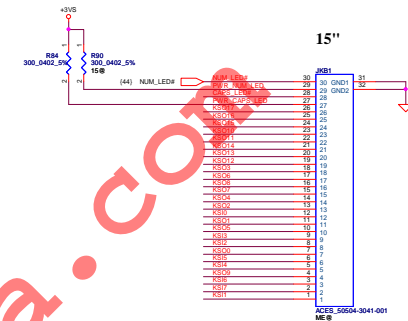
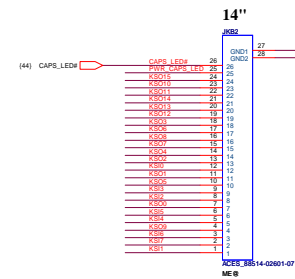
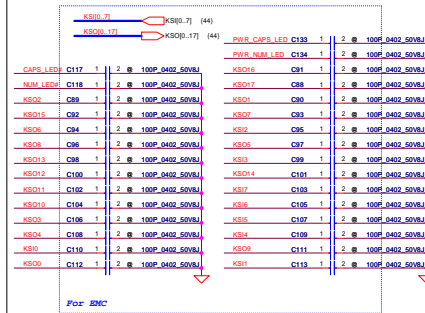


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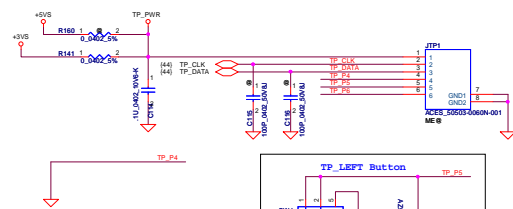


TP/B Connector

K/B Connector

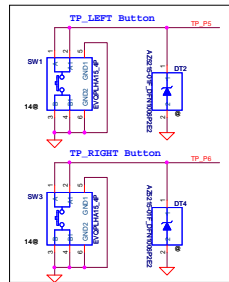


14"	15"
KR_1_K011_14	KR00_15
KR_2_K017_14	KR12_15
KR_3_K016_14	KR13_15
KR_4_K018_14	KR14_15
KR_5_K014_14	KR01_15
KR_6_K015_14	KR10_15
KR_7_K005_14	KR02_15
KR_8_KR12_14	KR04_15
KR_9_KR13_14	KR07_15
KR_10_K015_14	KR08_15
KR_11_KR01_14	KR06_15
KR_12_KR14_14	KR15_15
KR_13_KR02_14	KR09_15
KR_14_KR04_14	KR03_15
KR_15_KR07_14	KR04_15
KR_16_KR08_14	KR01_14
KR_17_KR06_14	KR01_15
KR_18_KR03_14	KR05_15
KR_19_KR01_14	KR06_15
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KR_21_KR04_14	KR_14RD_PRR_15
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KR_24_KR15_14	KRD_LNDR_15

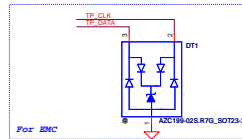


For 14"		For 15"	
1	VDD	1	VDD
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	GND
5	TP-L	5	TP-L
6	TP-R	6	TP-R

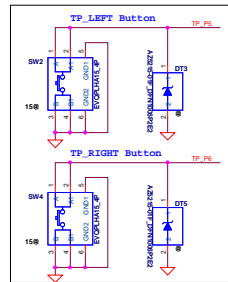
Change to same as ACLUA



For 14"

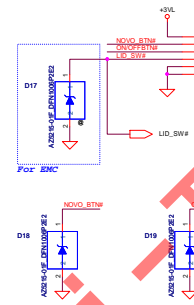


For



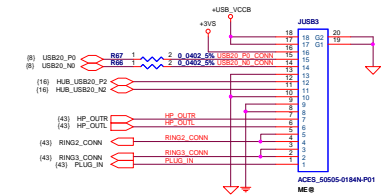
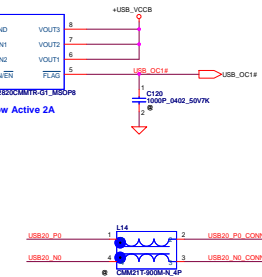
For 15"

PWR/B Connector

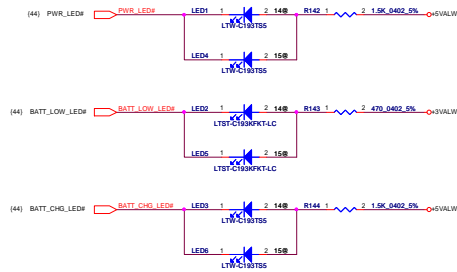



USB I/O Connector

Right Side USB2.0 Port X 1 (USB/B)



LED

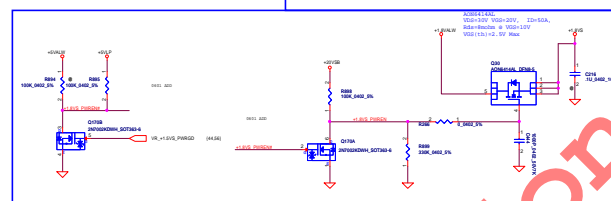
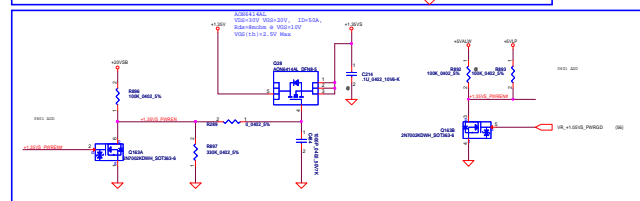
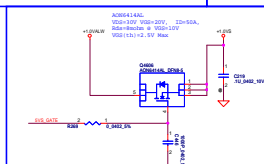
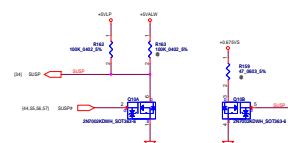
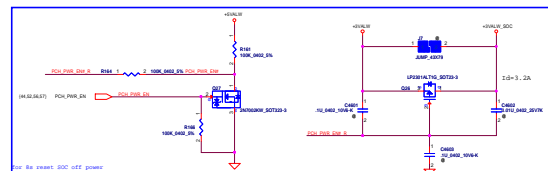
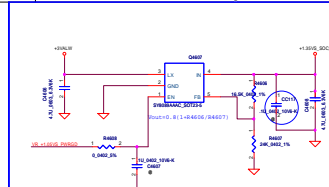
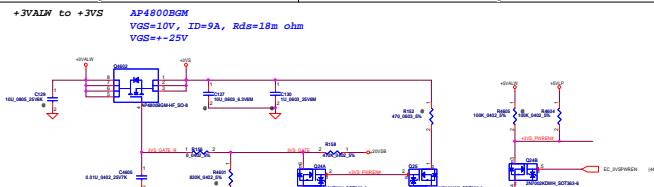
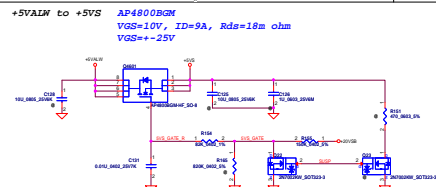


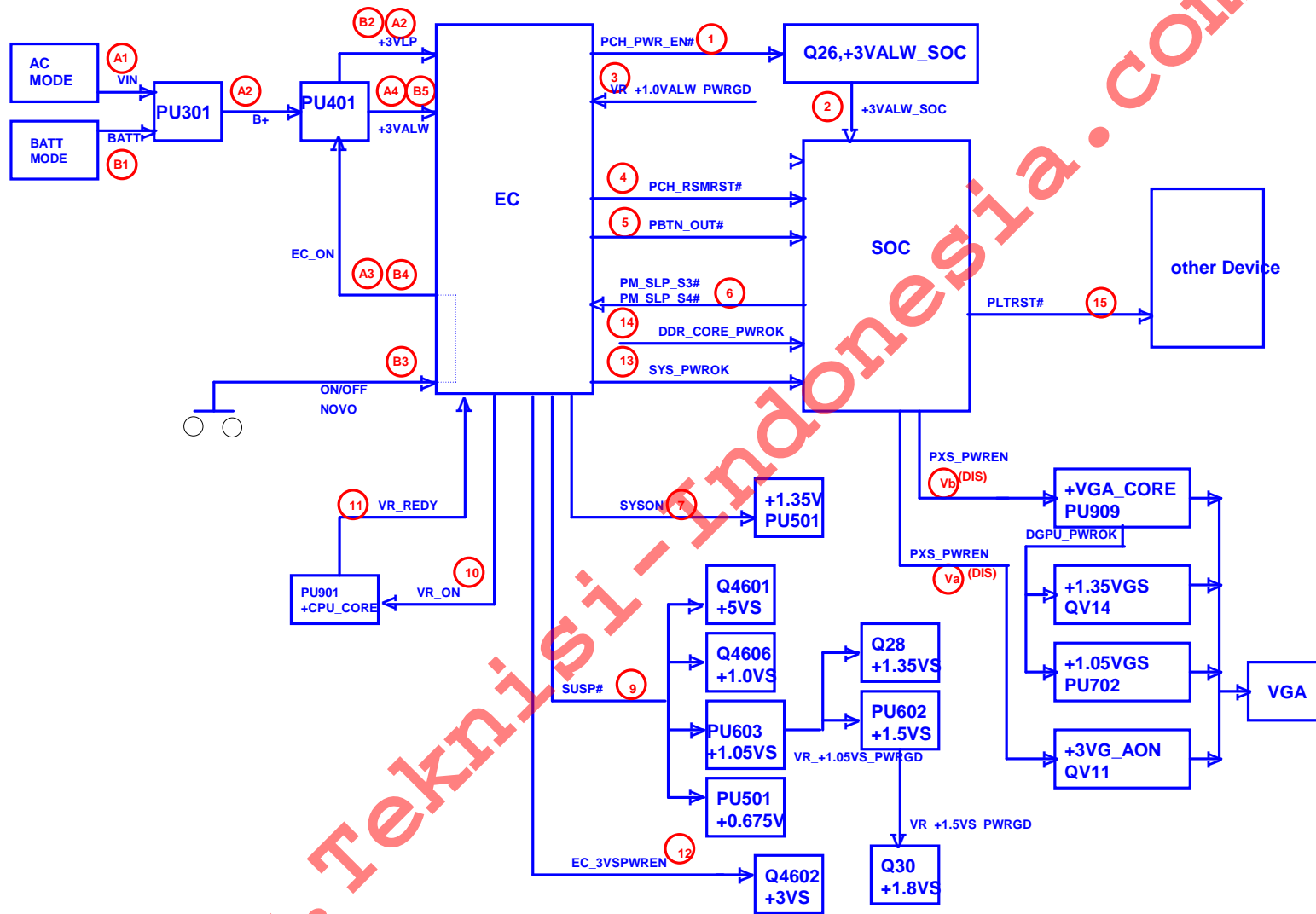
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Issued Date	2013/08/08	Deciphered Date	2013/08/05	

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Title	Power sequence Block		
Size	Document Number	Rev	0.2
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54321

D
C
B
A

54321

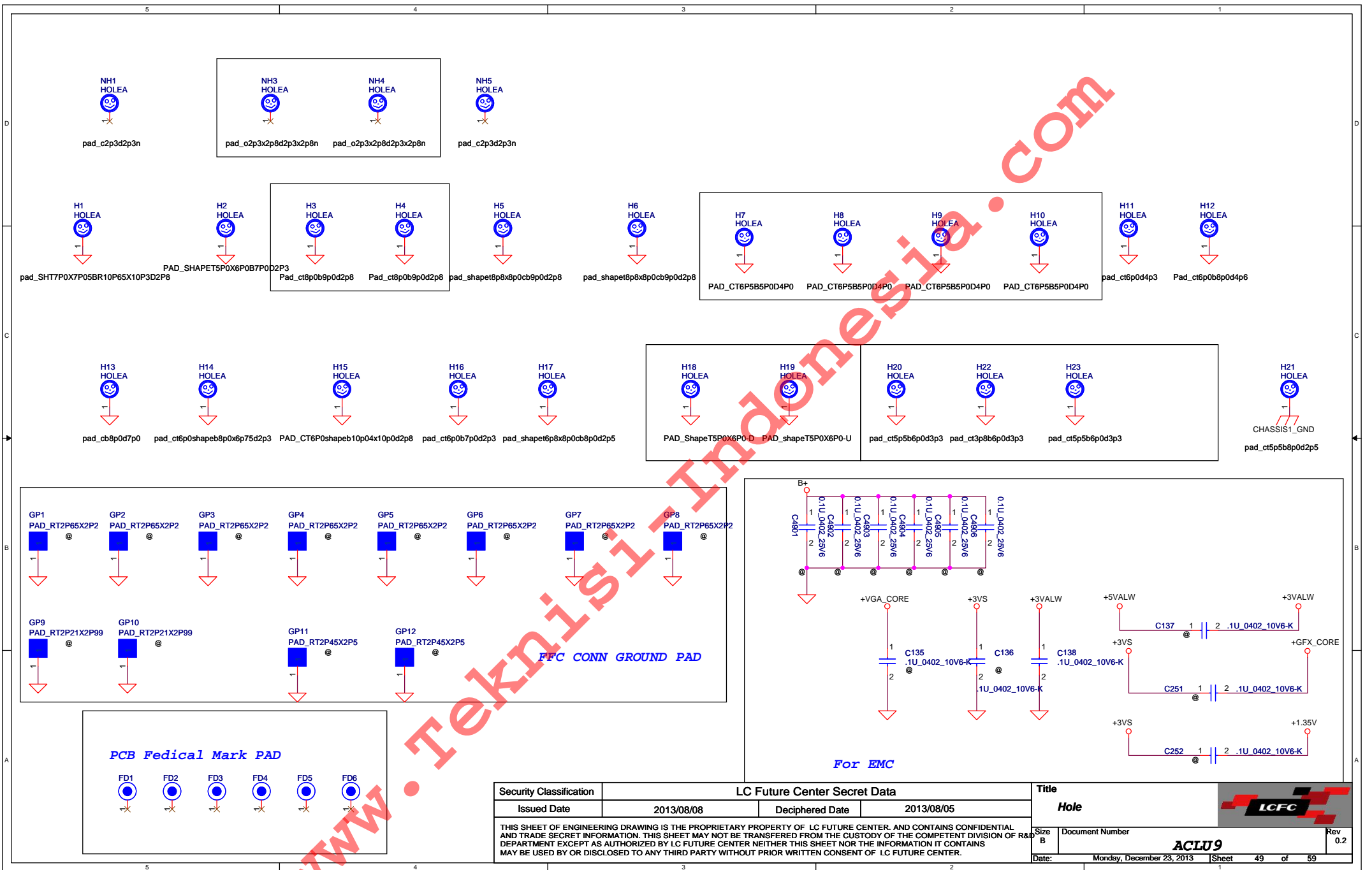
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C
B
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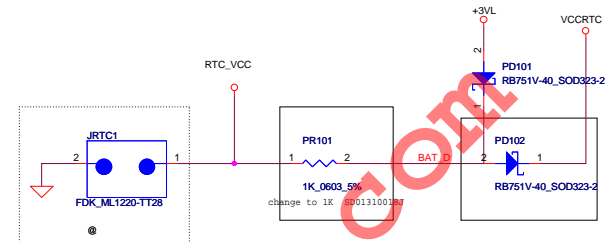
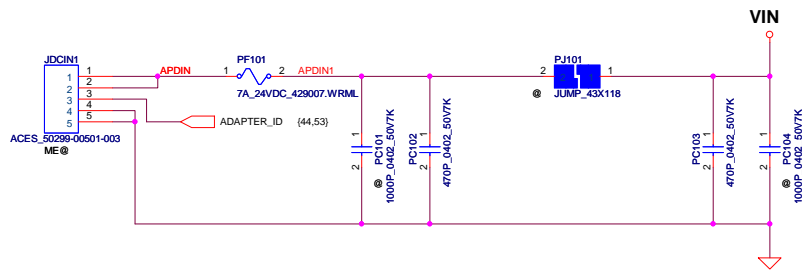
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54321

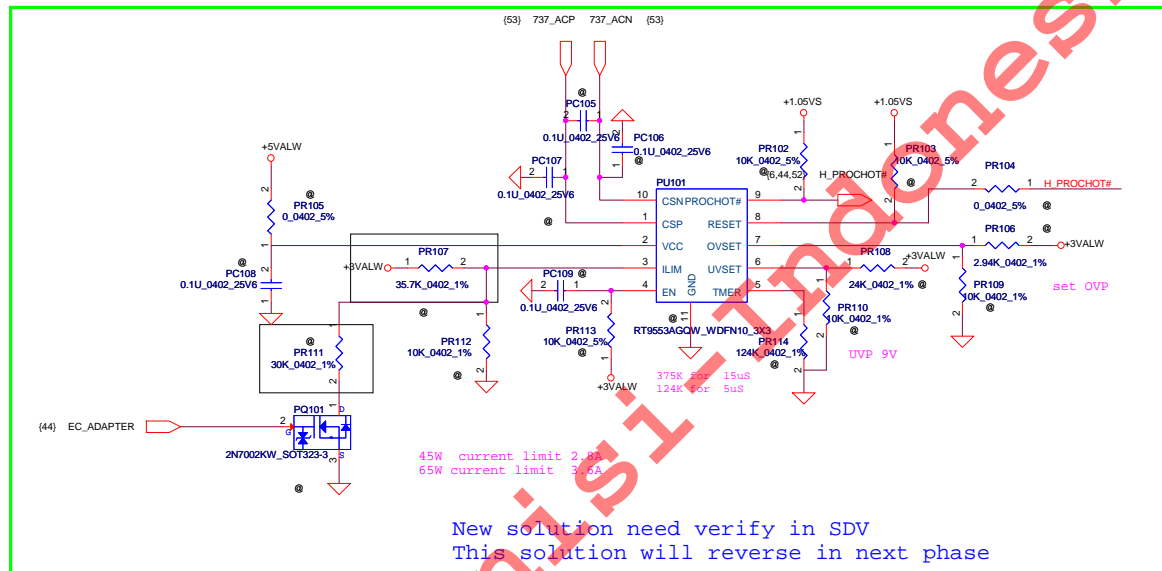
D
C
B
A

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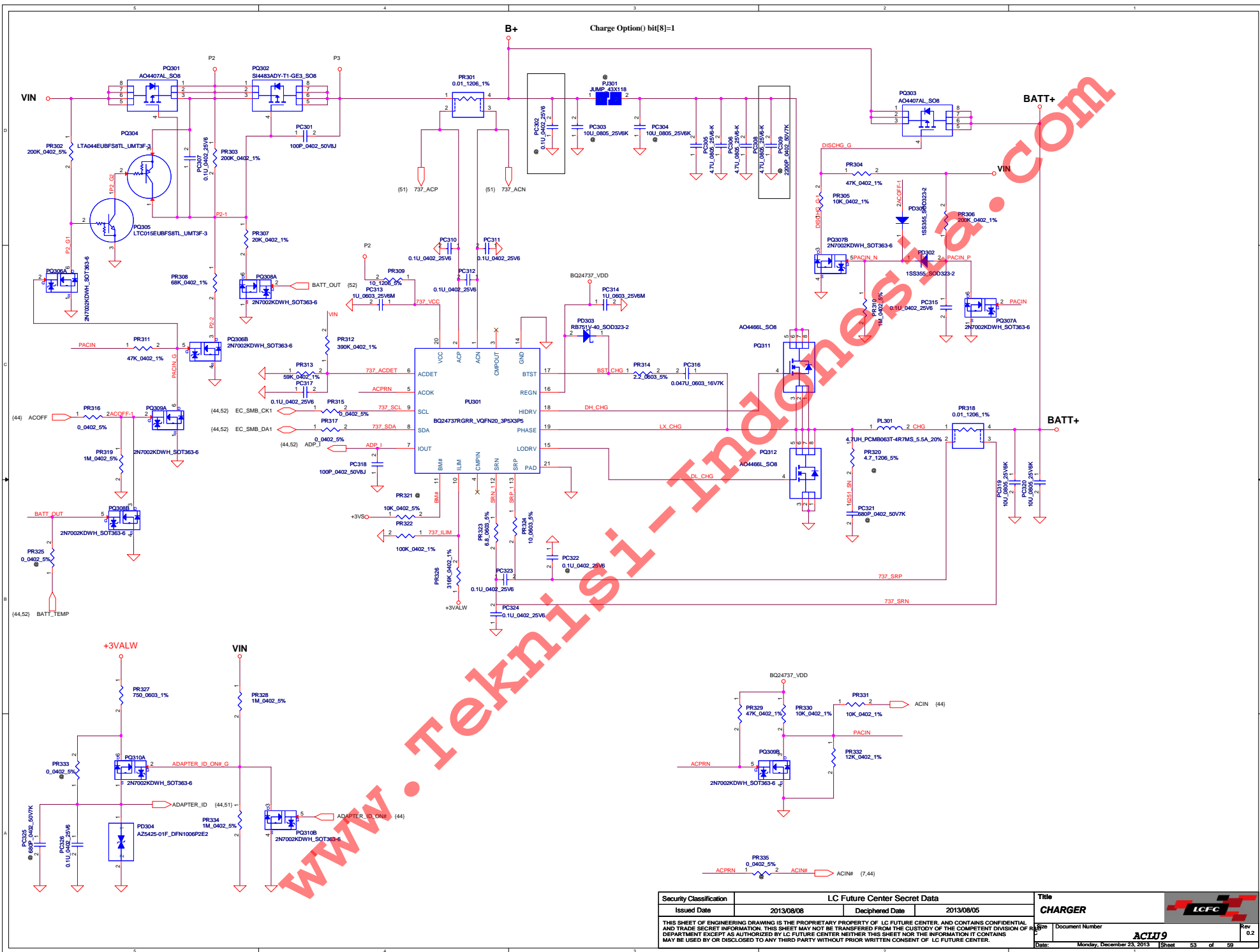
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+3VALW 20MIL
VCCRTC 20MIL
BAT_D 20MIL



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Issued Date	2013/08/08	Deciphered Date	2013/08/05
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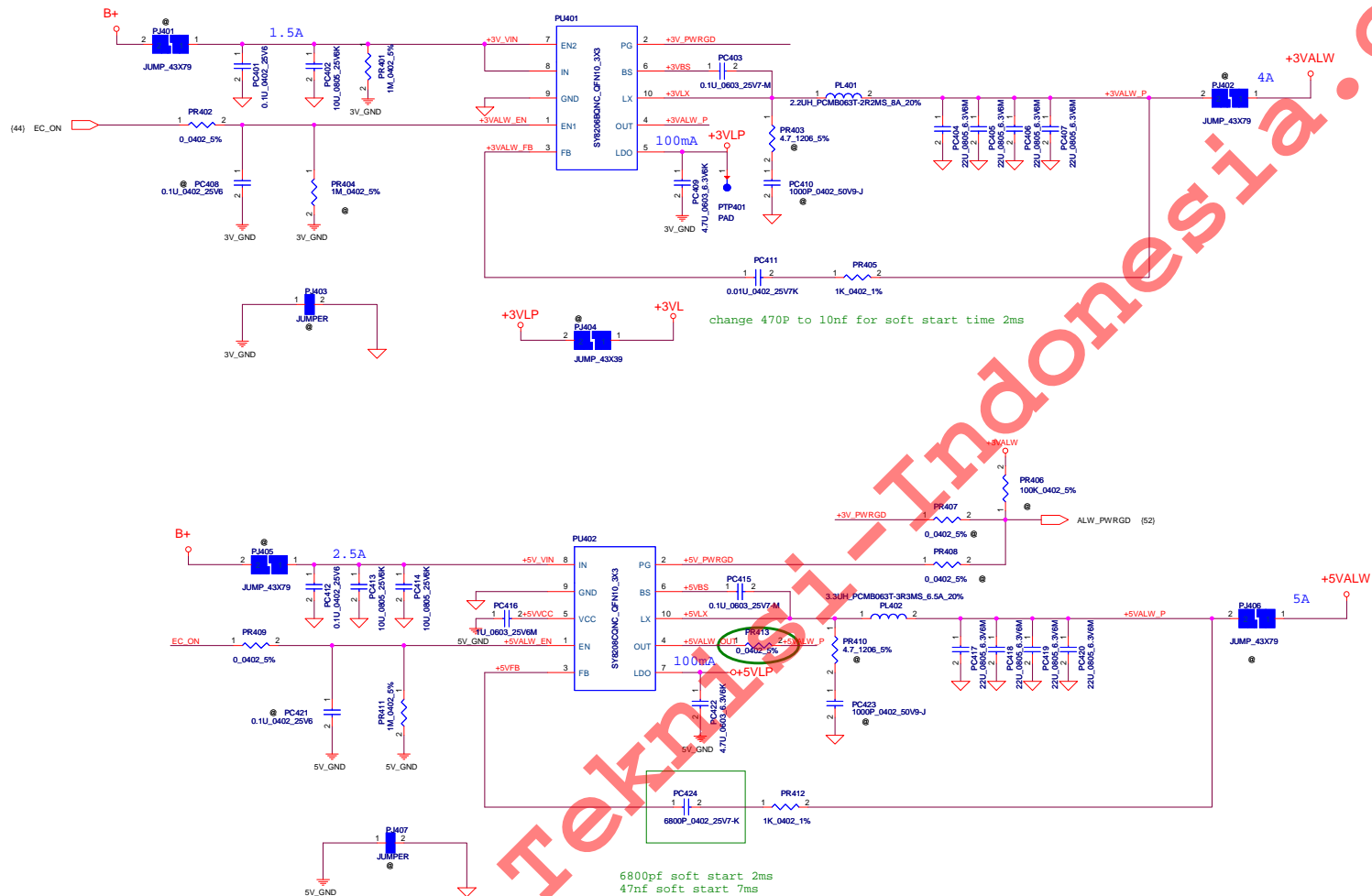
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Size	Document Number	Rev	0.2
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Document Number	ACLU9	
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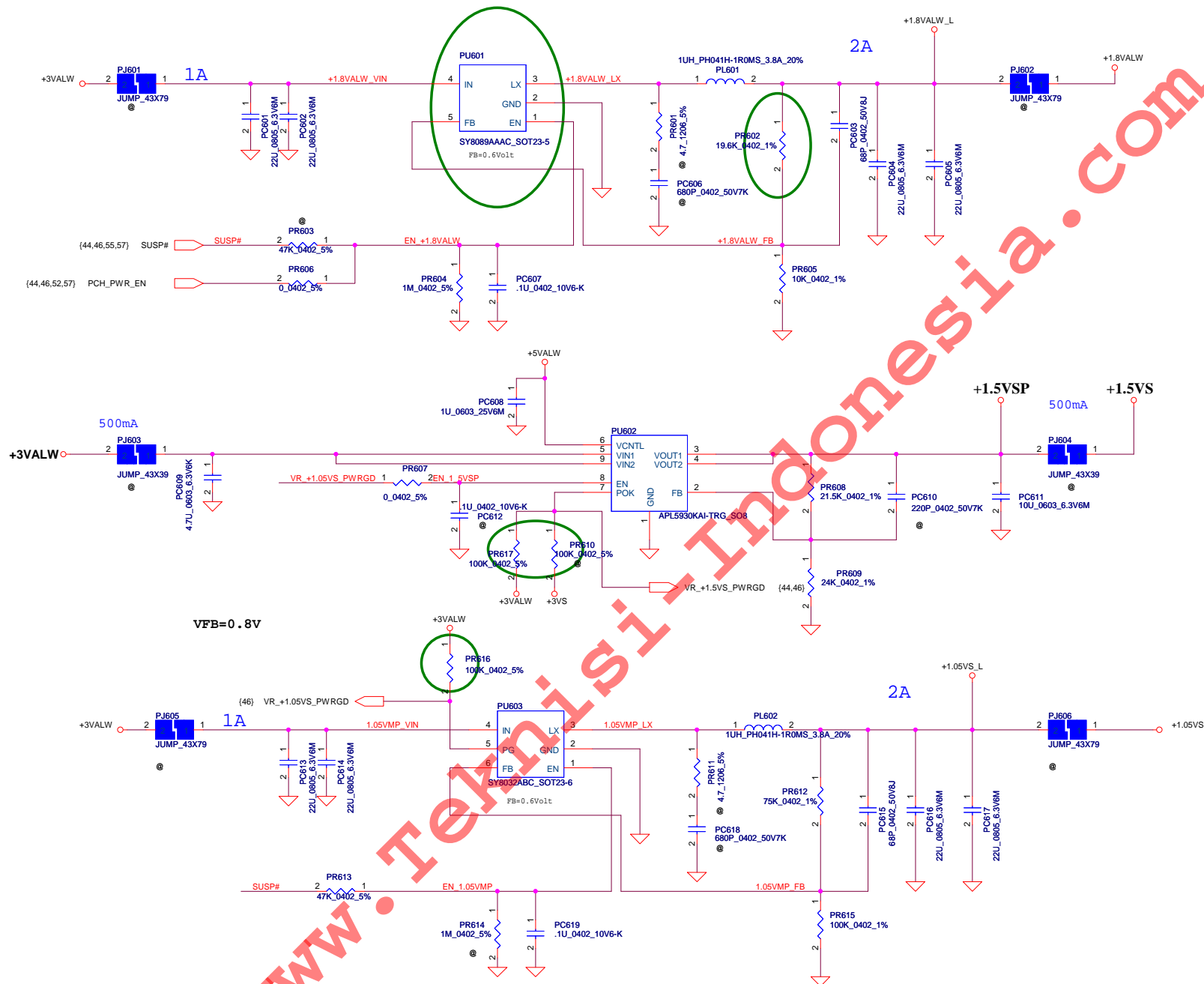


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Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Size	Document Number	Rev	
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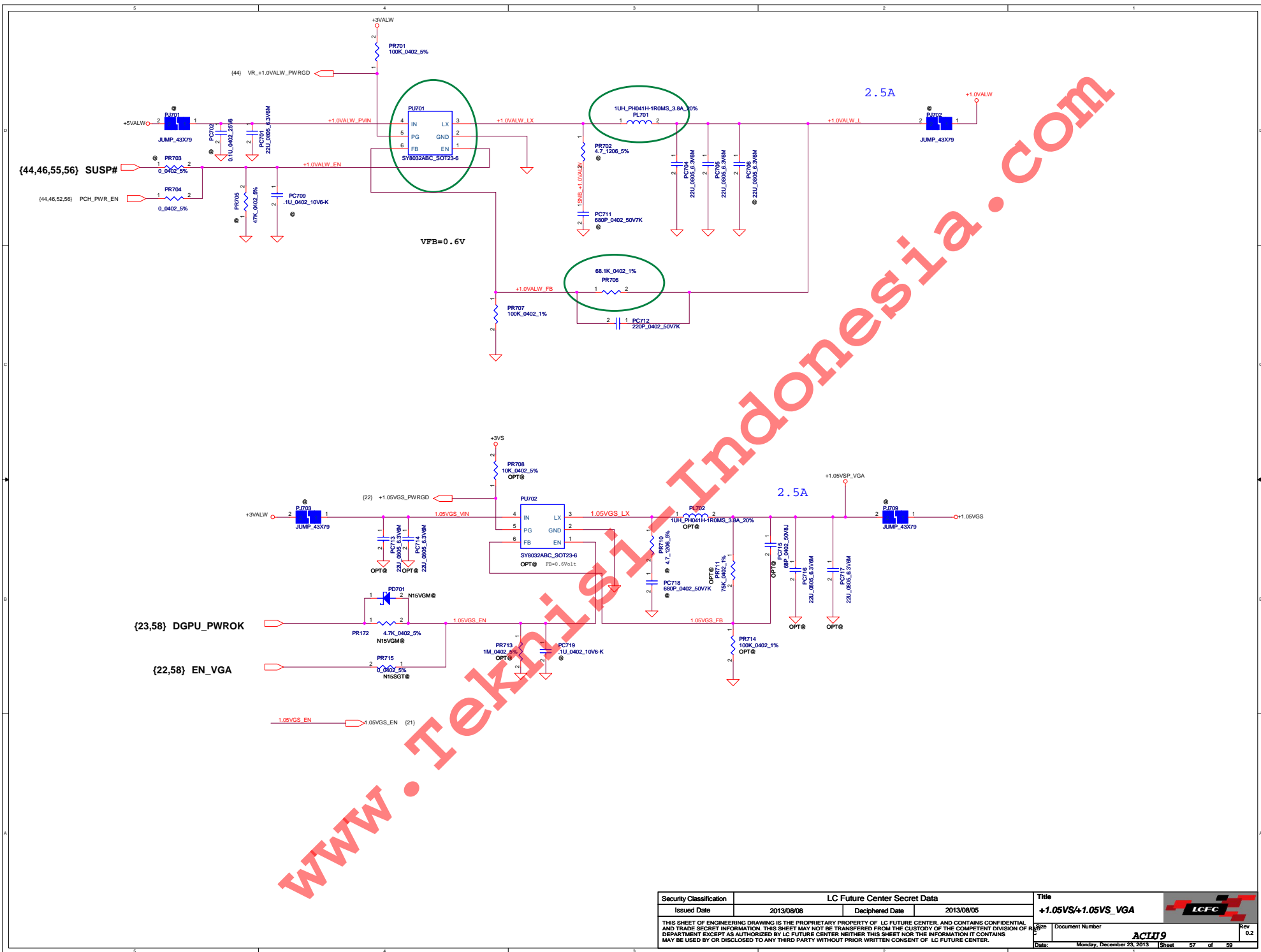


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		B	D
		N15S-GT	N15V-GM
R1	PR9440	20	27
R2	PR9434	20	7.5
R3	PR9436	2	0
R4	PR9437	18	6.2
R5	PR9431	0	1.74
C(nF)	PC1277	2.7	5.6

N15S-GT use config-B
N15V-GM use config-D

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Issued Date	2013/08/08	Deciphered Date	2013/08/05	PWR-VGA_CORE		
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