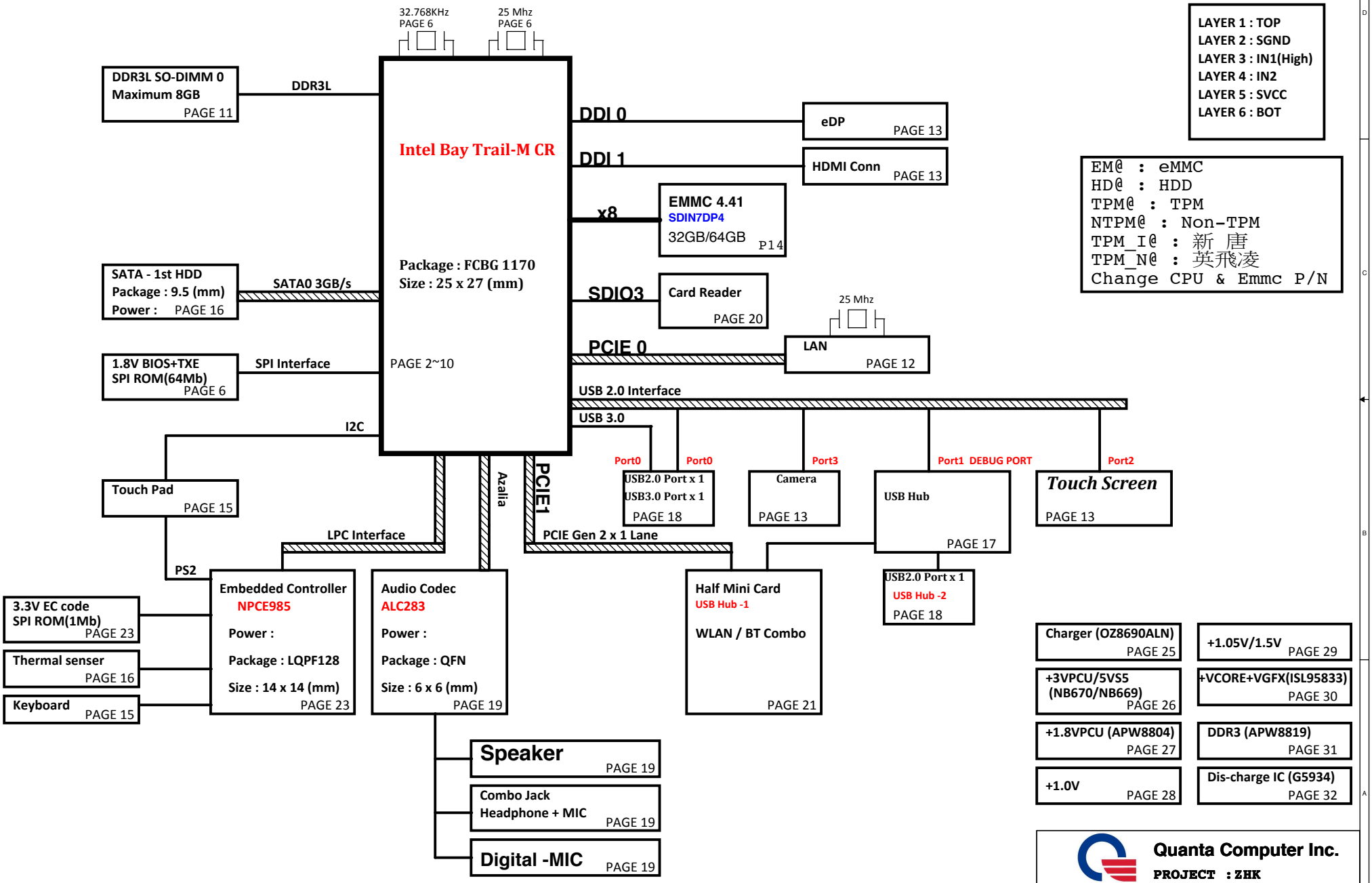
R2 UMA(11.6")

01

Intel Bay Trail-M Platform Block Diagram



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

```
EM@  : eMMC
HD@  : HDD
TPM@ : TPM
NTPM@ : Non-TPM
TPM_I@ : 新 唐
TPM_N@ : 英飛凌
Change CPU & Emmc P/N
```

Charger (OZ8690ALN) PAGE 25

+1.05V/1.5V PAGE 29

+3VPCU/5VS5 (NB670/NB669) PAGE 26

+VCORE+VGFX(ISL95833) PAGE 30

+1.8VPCU (APW8804) PAGE 27

DDR3 (APW8819) PAGE 31

+1.0V PAGE 28

Dis-charge IC (G5934) PAGE 32

Quanta Computer Inc.

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	Intel Block Diagram	1A
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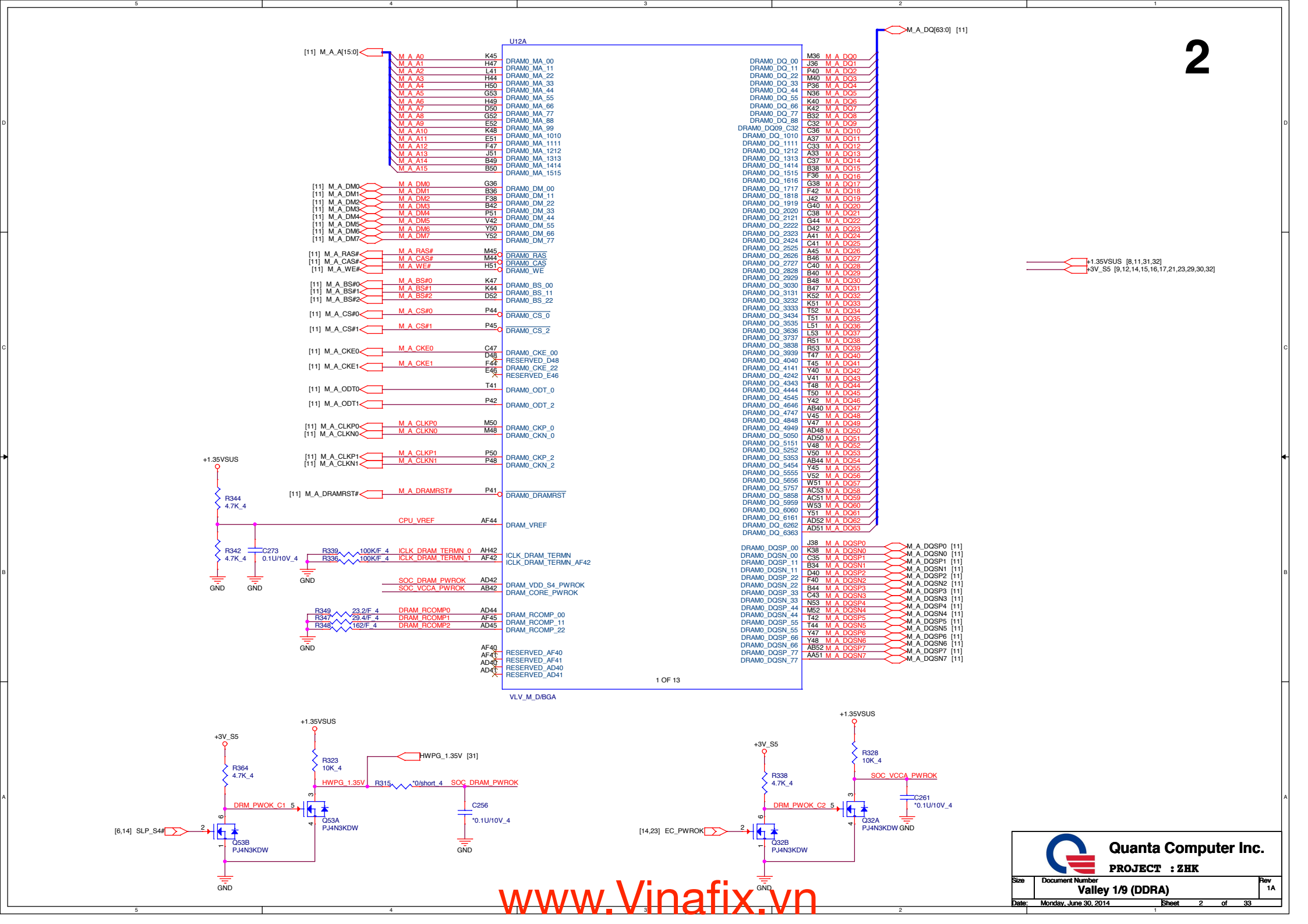
2
U12A
[11] M_A_A[15:0]
M_A_A0 K45
M_A_A1 H47
M_A_A2 L41
M_A_A3 H44
M_A_A4 H50
M_A_A5 G53
M_A_A6 H49
M_A_A7 D50
M_A_A8 G52
M_A_A9 E52
M_A_A10 K48
M_A_A11 E51
M_A_A12 F47
M_A_A13 J51
M_A_A14 B49
M_A_A15 B50
DRAM0_MA_00
DRAM0_MA_11
DRAM0_MA_22
DRAM0_MA_33
DRAM0_MA_44
DRAM0_MA_55
DRAM0_MA_66
DRAM0_MA_77
DRAM0_MA_88
DRAM0_MA_99
DRAM0_MA_1010
DRAM0_MA_1111
DRAM0_MA_1212
DRAM0_MA_1313
DRAM0_MA_1414
DRAM0_MA_1515
[11] M_A_DM0
[11] M_A_DM1
[11] M_A_DM2
[11] M_A_DM3
[11] M_A_DM4
[11] M_A_DM5
[11] M_A_DM6
[11] M_A_DM7
M_A_DM0 G36
M_A_DM1 B36
M_A_DM2 F38
M_A_DM3 B42
M_A_DM4 P51
M_A_DM5 V42
M_A_DM6 Y50
M_A_DM7 Y52
DRAM0_DM_00
DRAM0_DM_11
DRAM0_DM_22
DRAM0_DM_33
DRAM0_DM_44
DRAM0_DM_55
DRAM0_DM_66
DRAM0_DM_77
[11] M_A_RAS#
[11] M_A_CAS#
[11] M_A_WE#
M_A_RAS# M45
M_A_CAS# M44
M_A_WE# H51
DRAM0_RAS
DRAM0_CAS
DRAM0_WE
[11] M_A_BS#0
[11] M_A_BS#1
[11] M_A_BS#2
M_A_BS#0 K47
M_A_BS#1 K44
M_A_BS#2 D52
DRAM0_BS_00
DRAM0_BS_11
DRAM0_BS_22
[11] M_A_CS#0
M_A_CS#0 P44
DRAM0_CS_0
[11] M_A_CS#1
M_A_CS#1 P45
DRAM0_CS_2
[11] M_A_CKE0
M_A_CKE0 C47
D48
DRAM0_CKE_00
RESERVED_D48
[11] M_A_CKE1
M_A_CKE1 F44
E46
DRAM0_CKE_22
RESERVED_E46
[11] M_A_ODT0
T41
DRAM0_ODT_0
[11] M_A_ODT1
P42
DRAM0_ODT_2
[11] M_A_CLKP0
[11] M_A_CLKN0
M_A_CLKP0 M50
M_A_CLKN0 M48
DRAM0_CKP_0
DRAM0_CKN_0
[11] M_A_CLKP1
[11] M_A_CLKN1
M_A_CLKP1 P50
M_A_CLKN1 P48
DRAM0_CKP_2
DRAM0_CKN_2
[11] M_A_DRAMRST#
M_A_DRAMRST# P41
DRAM0_DRAMRST
CPU_VREF AF44
DRAM_VREF
+1.35VSUS
R344 4.7K_4
R342 4.7K_4
C273 0.1U/10V_4
GND
R339 100K/F_4
R336 100K/F_4
ICLK_DRAM_TERMN_0 AH42
ICLK_DRAM_TERMN_1 AF42
ICLK_DRAM_TERMN
ICLK_DRAM_TERMN_AF42
SOC_DRAM_PWROK AD42
SOC_VCCA_PWROK AB42
DRAM_VDD_S4_PWROK
DRAM_CORE_PWROK
R349 23.2/F_4
R347 29.4/F_4
R348 162/F_4
DRAM_RCOMP0 AD44
DRAM_RCOMP1 AF45
DRAM_RCOMP2 AD45
DRAM_RCOMP_00
DRAM_RCOMP_11
DRAM_RCOMP_22
AF40 RESERVED_AF40
AF41 RESERVED_AF41
AD40 RESERVED_AD40
AD41 RESERVED_AD41
1 OF 13
VLV_M_D/BGA
M_A_DQ[63:0] [11]
DRAM0_DQ_00 M36 M_A_DQ0
DRAM0_DQ_11 J36 M_A_DQ1
DRAM0_DQ_22 P40 M_A_DQ2
DRAM0_DQ_33 M40 M_A_DQ3
DRAM0_DQ_44 P36 M_A_DQ4
DRAM0_DQ_55 N36 M_A_DQ5
DRAM0_DQ_66 K40 M_A_DQ6
DRAM0_DQ_77 K42 M_A_DQ7
DRAM0_DQ_88 B32 M_A_DQ8
DRAM0_DQ09_C32 C32 M_A_DQ9
DRAM0_DQ_1010 C36 M_A_DQ10
DRAM0_DQ_1111 A37 M_A_DQ11
DRAM0_DQ_1212 C33 M_A_DQ12
DRAM0_DQ_1313 A33 M_A_DQ13
DRAM0_DQ_1414 C37 M_A_DQ14
DRAM0_DQ_1515 B38 M_A_DQ15
DRAM0_DQ_1616 F36 M_A_DQ16
DRAM0_DQ_1717 G38 M_A_DQ17
DRAM0_DQ_1818 F42 M_A_DQ18
DRAM0_DQ_1919 J42 M_A_DQ19
DRAM0_DQ_2020 G40 M_A_DQ20
DRAM0_DQ_2121 C38 M_A_DQ21
DRAM0_DQ_2222 G44 M_A_DQ22
DRAM0_DQ_2323 D42 M_A_DQ23
DRAM0_DQ_2424 A41 M_A_DQ24
DRAM0_DQ_2525 C41 M_A_DQ25
DRAM0_DQ_2626 A45 M_A_DQ26
DRAM0_DQ_2727 B46 M_A_DQ27
DRAM0_DQ_2828 C40 M_A_DQ28
DRAM0_DQ_2929 B40 M_A_DQ29
DRAM0_DQ_3030 B48 M_A_DQ30
DRAM0_DQ_3131 B47 M_A_DQ31
DRAM0_DQ_3232 K52 M_A_DQ32
DRAM0_DQ_3333 K51 M_A_DQ33
DRAM0_DQ_3434 T52 M_A_DQ34
DRAM0_DQ_3535 T51 M_A_DQ35
DRAM0_DQ_3636 L51 M_A_DQ36
DRAM0_DQ_3737 L53 M_A_DQ37
DRAM0_DQ_3838 R51 M_A_DQ38
DRAM0_DQ_3939 R53 M_A_DQ39
DRAM0_DQ_4040 T47 M_A_DQ40
DRAM0_DQ_4141 T45 M_A_DQ41
DRAM0_DQ_4242 Y40 M_A_DQ42
DRAM0_DQ_4343 V41 M_A_DQ43
DRAM0_DQ_4444 T48 M_A_DQ44
DRAM0_DQ_4545 T50 M_A_DQ45
DRAM0_DQ_4646 Y42 M_A_DQ46
DRAM0_DQ_4747 AB40 M_A_DQ47
DRAM0_DQ_4848 V45 M_A_DQ48
DRAM0_DQ_4949 V47 M_A_DQ49
DRAM0_DQ_5050 AD48 M_A_DQ50
DRAM0_DQ_5151 AD50 M_A_DQ51
DRAM0_DQ_5252 V48 M_A_DQ52
DRAM0_DQ_5353 V50 M_A_DQ53
DRAM0_DQ_5454 AB44 M_A_DQ54
DRAM0_DQ_5555 Y45 M_A_DQ55
DRAM0_DQ_5656 V52 M_A_DQ56
DRAM0_DQ_5757 W51 M_A_DQ57
DRAM0_DQ_5858 AC53 M_A_DQ58
DRAM0_DQ_5959 AC51 M_A_DQ59
DRAM0_DQ_6060 W53 M_A_DQ60
DRAM0_DQ_6161 Y51 M_A_DQ61
DRAM0_DQ_6262 AD52 M_A_DQ62
DRAM0_DQ_6363 AD51 M_A_DQ63
DRAM0_DQSP_00 J38 M_A_DQSP0 [11]
DRAM0_DQSN_00 K38 M_A_DQSN0 [11]
DRAM0_DQSP_11 C35 M_A_DQSP1 [11]
DRAM0_DQSN_11 B34 M_A_DQSN1 [11]
DRAM0_DQSP_22 D40 M_A_DQSP2 [11]
DRAM0_DQSN_22 F40 M_A_DQSN2 [11]
DRAM0_DQSP_33 B44 M_A_DQSP3 [11]
DRAM0_DQSN_33 C43 M_A_DQSN3 [11]
DRAM0_DQSP_44 N53 M_A_DQSP4 [11]
DRAM0_DQSN_44 M52 M_A_DQSN4 [11]
DRAM0_DQSP_55 T42 M_A_DQSP5 [11]
DRAM0_DQSN_55 T44 M_A_DQSN5 [11]
DRAM0_DQSP_66 Y47 M_A_DQSP6 [11]
DRAM0_DQSN_66 Y48 M_A_DQSN6 [11]
DRAM0_DQSP_77 AB52 M_A_DQSP7 [11]
DRAM0_DQSN_77 AA51 M_A_DQSN7 [11]
+1.35VSUS [8,11,31,32]
+3V_S5 [9,12,14,15,16,17,21,23,29,30,32]
+3V_S5
R364 4.7K_4
+1.35VSUS
R323 10K_4
HWPG_1.35V [31]
HWPG_1.35V
R315 *0/short_4
SOC_DRAM_PWROK
C256 *0.1U/10V_4
DRM_PWOK_C1
[6,14] SLP_S4#
Q53B PJ4N3KDW
Q53A PJ4N3KDW
GND
+3V_S5
R338 4.7K_4
+1.35VSUS
R328 10K_4
SOC_VCCA_PWROK
C261 *0.1U/10V_4
DRM_PWOK_C2
[14,23] EC_PWROK
Q32B PJ4N3KDW
Q32A PJ4N3KDW
GND
Quanta Computer Inc.
PROJECT : ZHK
Size
Document Number
Valley 1/9 (DDRA)
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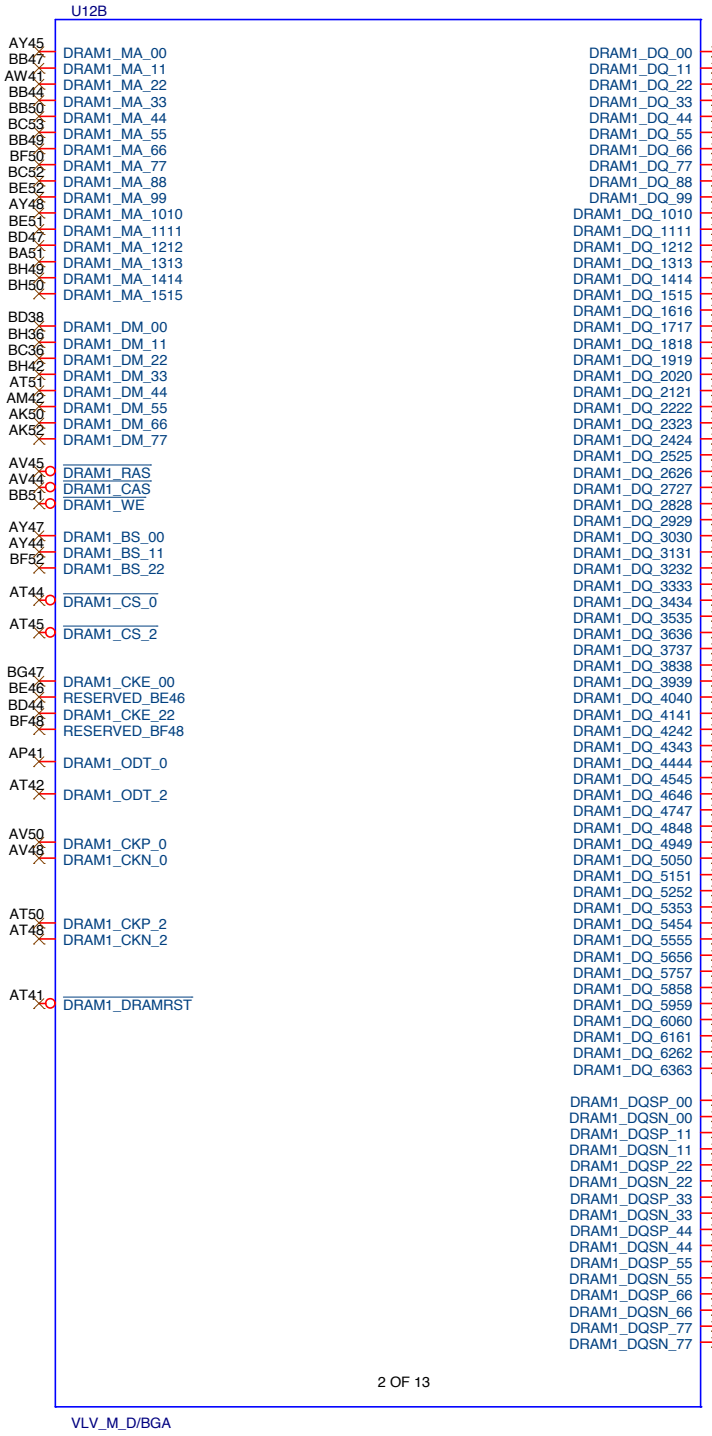

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Quanta Computer Inc.

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	Valley 2/9 (DDRB)	1A
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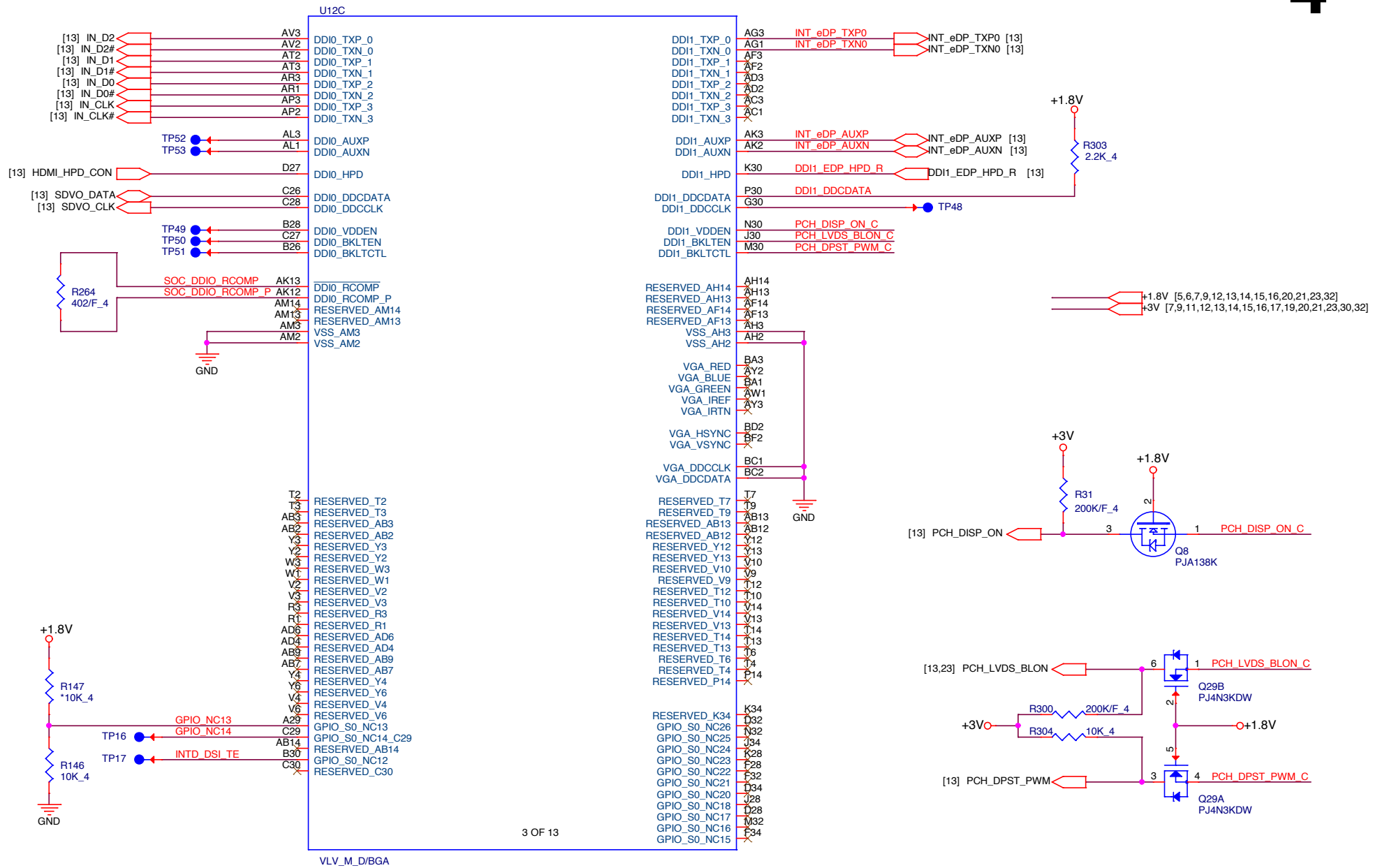

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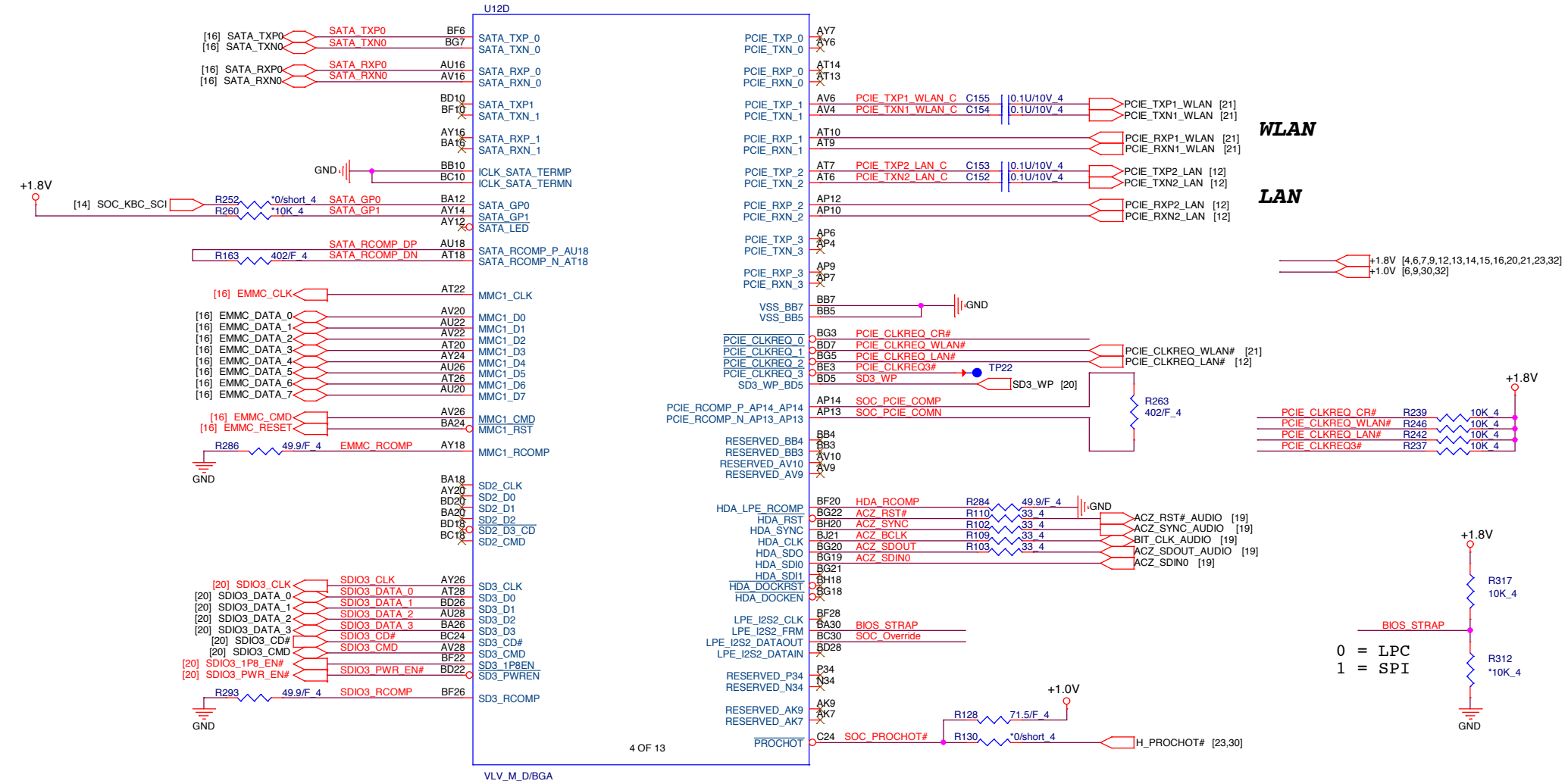
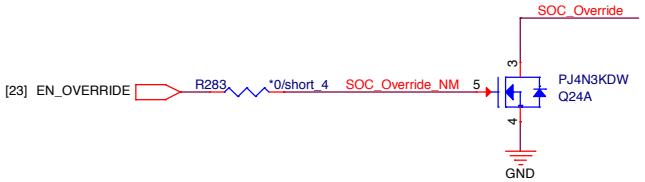
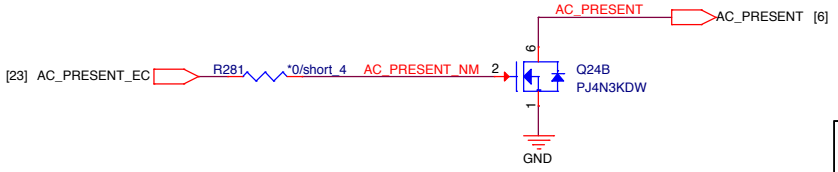


Security Flash Descriptors
0 = Override
1 = Normal Operation



AC Present: This input pin indicates when the platform is plugged into AC power.



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Size	Document Number: Valley 4/9 (SD/PCIE/SATA)	Rev: 1A
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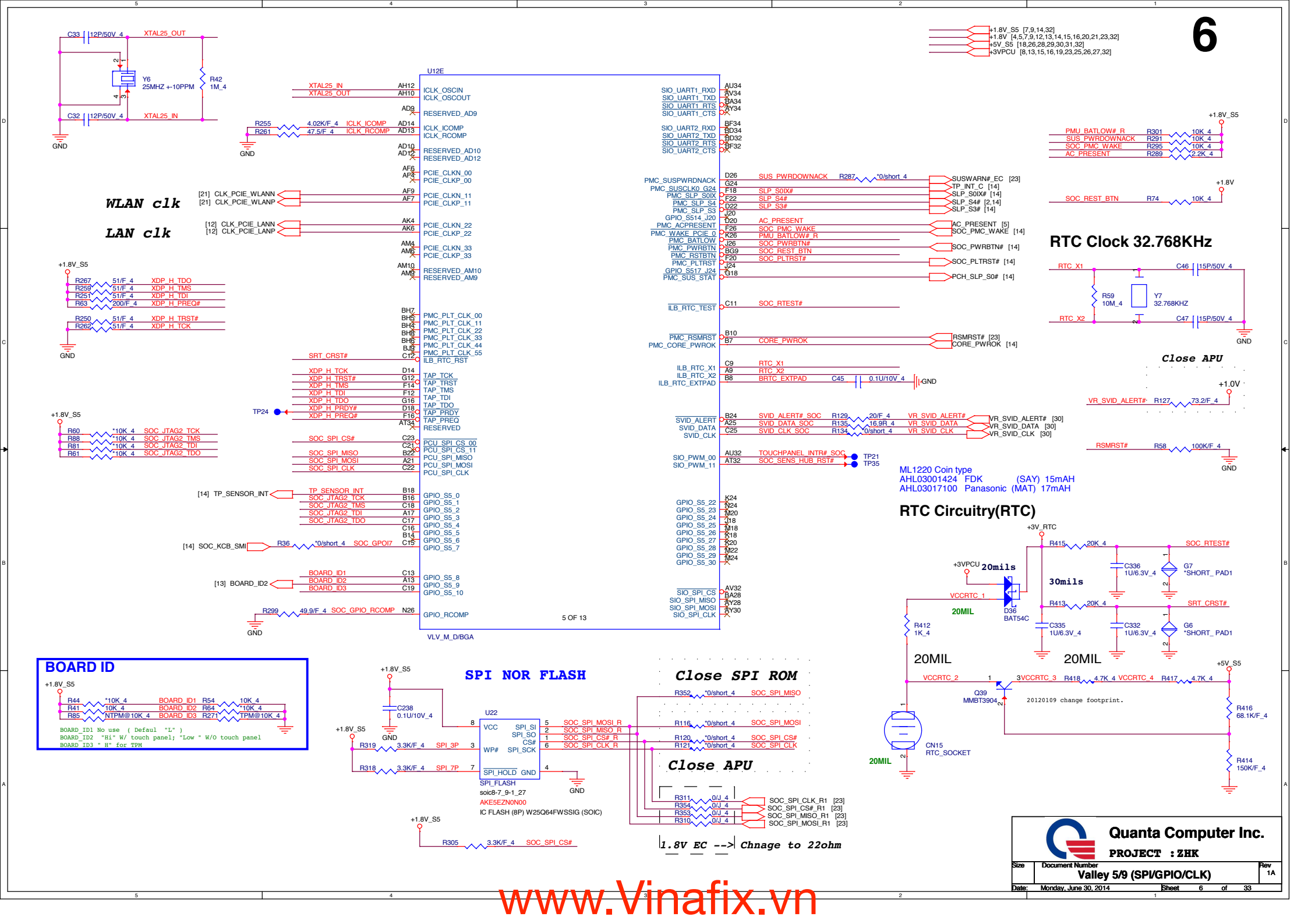

Port 1 is debug port

USB 2.0 / 3.0 Base

HUB1

Touch Panel

CAMERA

U12F

+1.8V_S5 — R48 *10K_4 — SOC_PWR_BUT

GPIO_S5_31 (G2)
GPIO_S5_32 (M3)
GPIO_S5_33 (L1)
GPIO_S5_34 (K2)
GPIO_S5_35 (K3)
GPIO_S5_36 (M2)
GPIO_S5_37 (N3)
GPIO_S5_38 (P2)
GPIO_S5_39 (L3)
GPIO_S5_40 (J3)
GPIO_S5_41 (P3)
GPIO_S5_42 (H3)
GPIO_S5_43 (B12)

[18] USBP0+ / [18] USBP0- — USB_DP0 (M16) / USB_DN0 (K16)
[17] USB_H1_P / [17] USB_H1_N — USB_DP1 (J14) / USB_DN1 (G14)
[13] USBP2+ / [13] USBP2- — USB_DP2 (K12) / USB_DN2 (J12)
[13] USBP3+ / [13] USBP3- — USB_DP3 (K10) / USB_DN3 (H10)

R249 1K/F_4 — ICLK_USB_TERMN_0 — D10 — ICLK_USB_TERMN_D10
R248 1K/F_4 — ICLK_USB_TERMN_1 — F10 — ICLK_USB_TERMN
GND

[18] SOC_USB_OC0
R105 10K_4 / R104 10K_4 — +1.8V_S5 — C20 / B20 — USB_OC_00 / USB_OC_11

R247 45.3/F_4 — USB_RCOMP — D6 / C7 — USB_RCOMPO / USB_RCOMPI
GND

R270 *0_4 — GND — M13 — USB_PLL_MON

B4 / B5 — USB_HSIC0_DATA / USB_HSIC0_STROBE
E2 / D2 — USB_HSIC1_DATA / USB_HSIC1_STROBE

GND — R55 45.3/F_4 — USB_HSIC_RCOMP — A7 — USB_HSIC_RCOMP
R285 49.9/F_4 — LPC_RCOMP — BF18 — LPC_RCOMP

12.5 Ohm

[15,21,23] LAD0 — LAD0 — BH16 — ILB_LPC_AD_00
[15,21,23] LAD1 — LAD1 — BJ17 — ILB_LPC_AD_11
[15,21,23] LAD2 — LAD2 — BJ13 — ILB_LPC_AD_22
[15,21,23] LAD3 — LAD3 — BG14 — ILB_LPC_AD_33
[15,21,23] LFRAME# — LFRAME# — BG17 — ILB_LPC_FRAME
SOC_CLKOUT_0 — BG15 — ILB_LPC_CLK_00
SOC_CLKOUT_1 — BH14 — ILB_LPC_CLK_11
SOC_CLKRUN# — BG16 — ILB_LPC_CLKRUN
[14,15] SOC_SERIRQ — SOC_SERIRQ — BG13 — ILB_LPC_SERIRQ

[15] PCLK_TPM — R98 22_4
[23] CLK_24M_KBC — R90 22_4
[21] CLK_24M_DEBUG — R274 22_4
[15,23] CLKRUN# — R279 22_4

[14] SMB_SOC_DATA
[14] SMB_SOC_CLK
+1.8V — R79 2.2K_4 SMB_SOC_DATA — BG12 — PCU_SMB_DATA
R73 2.2K_4 SMB_SOC_CLK — BH10 — PCU_SMB_CLK
R80 2.2K_4 SMB_SOC_ALERTB_C — BG11 — PCU_SMB_ALERT

SOC_CLKRUN# — R167 8.2K_4 — +3V

RESERVED_M10 (M10) / RESERVED_M9 (M9)
RESERVED_P7 (P7) / RESERVED_P6 (P6)
RESERVED_M7 (M7) / USB3_REXT0 (M12) — USB3_P0_REXT — R351 *1.24K/F_4 — USB3_P1_REXT — R258 1.24K/F_4 — GND
RESERVED_P10 (P10) / RESERVED_P12 (P12)
RESERVED_M4 (M4) / RESERVED_M6 (M6)
USB3_RXP0 (D4) / USB3_RXN0 (E3) — USB30_RX1+ [18] / USB30_RX1- [18]
USB3_TXP0 (K6) / USB3_TXN0 (K7) — USB30_TX1+ [18] / USB30_TX1- [18]
RESERVED_H8 (H8) / RESERVED_H7 (G7)
RESERVED_H5 (H5) / RESERVED_H4 (G4)

Top Swap (A16 Override)
0 = Top address bit is unchanged
1 = Top address bit is inverted

GPIO_S0_SC_55 (BD12)
GPIO_S0_SC_56 (BC12) — GPIO_S0_SC_56
GPIO_S0_SC_57 (BD14) — SOC_UART_TX
GPIO_S0_SC_58 (BC14)
GPIO_S0_SC_59 (BF14) — SOC_SENSOR_HUB_WAKE
GPIO_S0_SC_60 (BD16) — TOUCH_PANEL_SOC_RST#
GPIO_S0_SC_61 (BC16) — SOC_UART_RX

+1.8V — R253 *10K_4 / R254 *10K_4 — GND

ILB_8254_SPKR (BH12) — ACZ_SPKR [19]

SOC_UART_TX — R273 *0_4 — SOC_UART_RX
Un-Stuff for Test Only

SIO_I2C0_DATA (BH22) / SIO_I2C0_CLK (BG23) — I2C_0_SDA / I2C_0_SCL — R108 22_4 / R117 22_4 — I2C_6_SDA / I2C_6_SCL — I2C_6_SDA [14] / I2C_6_SCL [14]
SIO_I2C1_DATA (BG24) / SIO_I2C1_CLK (BH24)
SIO_I2C2_DATA (BG25) / SIO_I2C2_CLK (BJ25)
SIO_I2C3_DATA (BG26) / SIO_I2C3_CLK (BH26)
SIO_I2C4_DATA (BF27) / SIO_I2C4_CLK (BG27)
SIO_I2C5_DATA (BH28) / SIO_I2C5_CLK (BG28) — I2C_5_SDA / I2C_5_SCL — TP33 / TP34
SIO_I2C6_DATA (BJ29) / SIO_I2C6_CLK (BG29)
GPIO_S0_SC_092 (BH30) / GPIO_S0_SC_093 (BG30) — TP_NC / TP_NC1 — TP27 / TP32

I2C pull up:
Standard/ Fast Mode --> 560 ohm
Hight speed mode --> CLK- 560 ohm;
DATA- 910 ohm

+1.8V — TOUCH_PANEL_SOC_RST# — R269 *10K_4
SOC_SENSOR_HUB_WAKE — R265 *10K_4

+1.8V — I2C_6_SDA — R118 560_4
I2C_6_SCL — R119 560_4
I2C_5_SDA — R140 *2.2K_4
I2C_5_SCL — R145 *2.2K_4
TP_NC — R155 *2.2K_4
TP_NC1 — R156 *2.2K_4

+1.8V_S5 [6,9,14,32]
+1.8V [4,5,6,9,12,13,14,15,16,20,21,23,32]
+3V [4,9,11,12,13,14,15,16,17,19,20,21,23,30,32]

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VLV_M_D/BGA
REV = 1.15

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+VCC_GFX +VCC_CORE

R236 100/F_4

R296 100/F_4

VCC_SENSE
VCC_AXG_SENSE
VSS_SENSE

R314 100/F_4

GND

+VCC_CORE [22,30]
+VCC_GFX [22,30]
+1.35VSUS [2,11,31,32]

U12G

[30] VCC_SENSE
[30] VCC_AXG_SENSE
[30] VSS_SENSE
[30] VSS_AXG_SENSE

VCC_SENSE P28 CORE_VCC_SENSE_P28
VCC_AXG_SENSE BB8 UNCORE_VNN_SENSE
VSS_SENSE N28 CORE_VSS_SENSE_N28

R290 *0/short_4

+1.35VSUS_VSM

R334 *0/short_4

+1.35VSUS

AD38 DRAM_VDD_S4_AD38
AF38 DRAM_VDD_S4_AF38
A48 DRAM_VDD_S4
AK38 DRAM_VDD_S4_AK38
AM38 DRAM_VDD_S4_AM38
AV41 DRAM_VDD_S4_AV41
AV42 DRAM_VDD_S4_AV42
BB46 DRAM_VDD_S4_BB46

DRAM_VDD_S4_BD49 BD49
DRAM_VDD_S4_BD52 BD52
DRAM_VDD_S4_BD53 BD53
DRAM_VDD_S4_BF44 BF44
DRAM_VDD_S4_BG51 BG51
DRAM_VDD_S4_BJ48 BJ48
DRAM_VDD_S4_C51 C51
DRAM_VDD_S4_D44 D44
DRAM_VDD_S4_F49 F49
DRAM_VDD_S4_F52 F52
DRAM_VDD_S4_F53 F53
DRAM_VDD_S4_H46 H46
DRAM_VDD_S4_M41 M41
DRAM_VDD_S4_M42 M42
DRAM_VDD_S4_V38 V38
DRAM_VDD_S4_Y38 Y38

+1.35VSUS

C277 2.2U/6.3V_6
C271 2.2U/6.3V_6
C293 2.2U/6.3V_6
C292 2.2U/6.3V_6
C295 1U/6.3V_4
C294 0.1U/10V_4

GND

+VCC_CORE

AA27 CORE_VCC_S0IX_AA27
AA29 CORE_VCC_S0IX_AA29
AA30 CORE_VCC_S0IX_AA30
AC27 CORE_VCC_S0IX_AC27
AC29 CORE_VCC_S0IX_AC29
AC30 CORE_VCC_S0IX_AC30
AD27 CORE_VCC_S0IX_AD27
AD29 CORE_VCC_S0IX_AD29
AD30 CORE_VCC_S0IX_AD30
AF27 CORE_VCC_S0IX_AF27
AF29 CORE_VCC_S0IX_AF29
AG27 CORE_VCC_S0IX_AG27
AG29 CORE_VCC_S0IX_AG29
AG30 CORE_VCC_S0IX_AG30
P26 CORE_VCC_S0IX_P26
P27 CORE_VCC_S0IX_P27
U27 CORE_VCC_S0IX_U27
U29 CORE_VCC_S0IX_U29
V27 CORE_VCC_S0IX_V27
V29 CORE_VCC_S0IX_V29
V30 CORE_VCC_S0IX_V30
Y27 CORE_VCC_S0IX_Y27
Y29 CORE_VCC_S0IX_Y29
Y30 CORE_VCC_S0IX_Y30

C237 10U/6.3V_6
C230 4.7U/6.3V_6
C167 4.7U/6.3V_6
C231 2.2U/6.3V_6
C176 2.2U/6.3V_6
C179 22U/6.3V_6
C175 22U/6.3V_6
C178 22U/6.3V_6

GND

UNCORE_VNN_S3_AA24
UNCORE_VNN_S3_AC22
UNCORE_VNN_S3_AC24
UNCORE_VNN_S3_AD22
UNCORE_VNN_S3_AD24
UNCORE_VNN_S3_AF22
UNCORE_VNN_S3_AF24
UNCORE_VNN_S3_AG22
UNCORE_VNN_S3_AG24
UNCORE_VNN_S3_AJ22
UNCORE_VNN_S3_AJ24
UNCORE_VNN_S3_AK22
UNCORE_VNN_S3_AK24
UNCORE_VNN_S3_AK25
UNCORE_VNN_S3_AK27
UNCORE_VNN_S3_AK29
UNCORE_VNN_S3_AK30
UNCORE_VNN_S3_AK32
UNCORE_VNN_S3_AM22

AA24
AC22
AC24
AD22
AD24
AF22
AF24
AG22
AG24
AJ22
AJ24
AK22
AK24
AK25
AK27
AK29
AK30
AK32
AM22

+VCC_GFX

C158 10U/6.3V_6
C50 10U/6.3V_6
C58 10U/6.3V_6
C229 1U/6.3V_4
C214 1U/6.3V_4
C218 1U/6.3V_4
C244 0.1U/10V_4
C234 0.1U/10V_4
C151 0.1U/10V_4

GND

TP26 SOC_CORE_PINAF30 AF30 TP_CORE_V1P05_S4

7 OF 13

TP2_CORE_VCC_S0IX AA22 SOC_CORE_PIN_AA22 TP25

VLV_M_D/BGA
REV = 1.15

+1.35VSUS_VSM

C270 0.1U/10V_4
C267 0.1U/10V_4

GND

IO Thrm Protect

+3VPCU

R345 *10K/J_4

default 25 degree for detect temperature

THRM_MOINTOR [23]

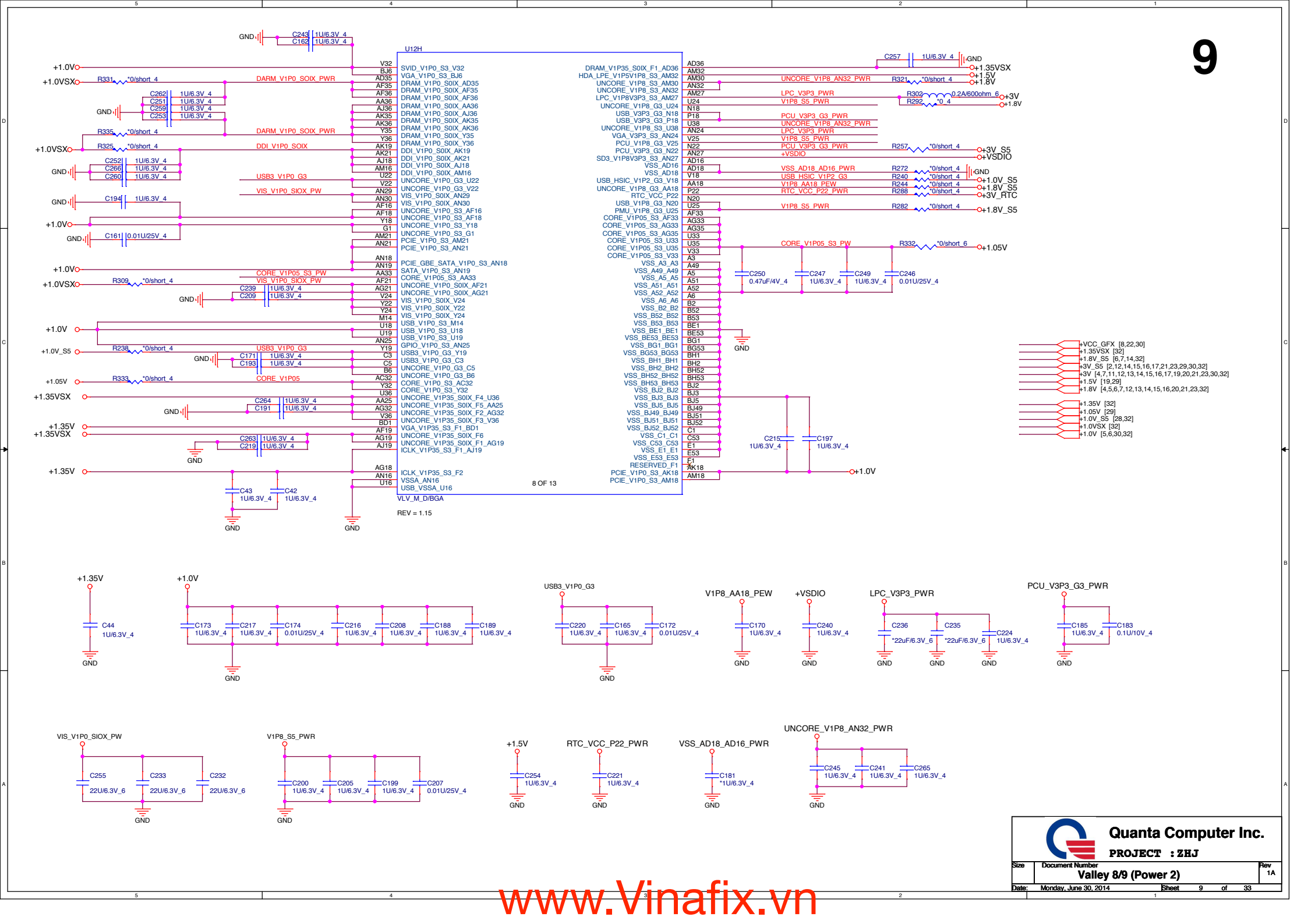
R337 *0_4

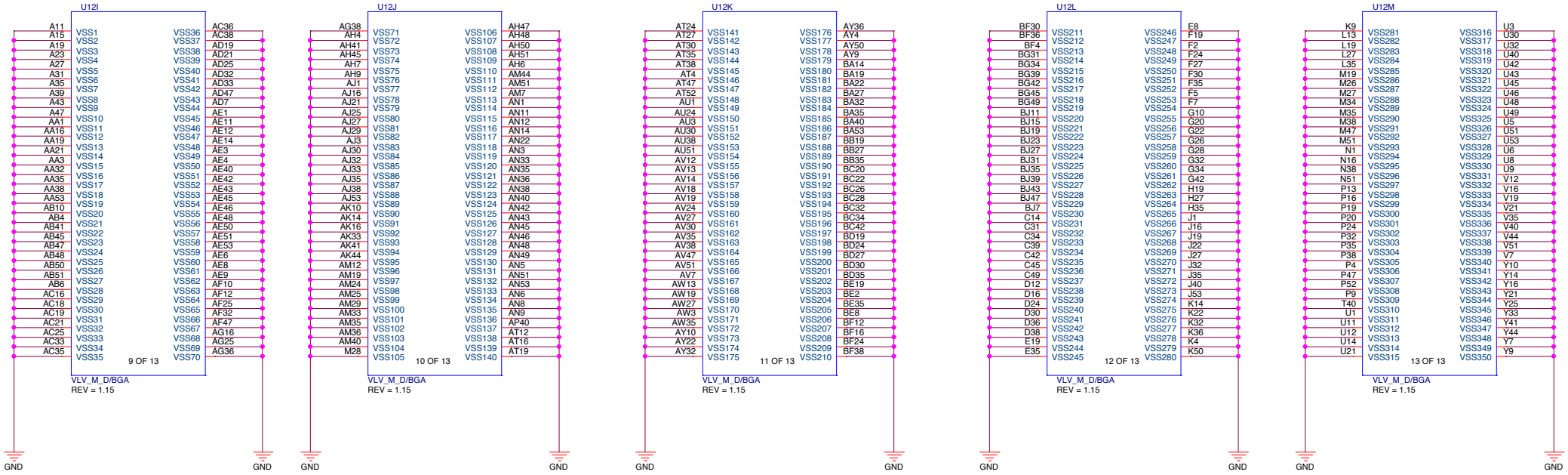
C274 *0.1u/10V_4

THER_CPU

R327 *10K_6_NTC

Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Valley 7/9 (Power 1)	Rev 2A
Date: Monday, June 30, 2014	Sheet 8 of 33	

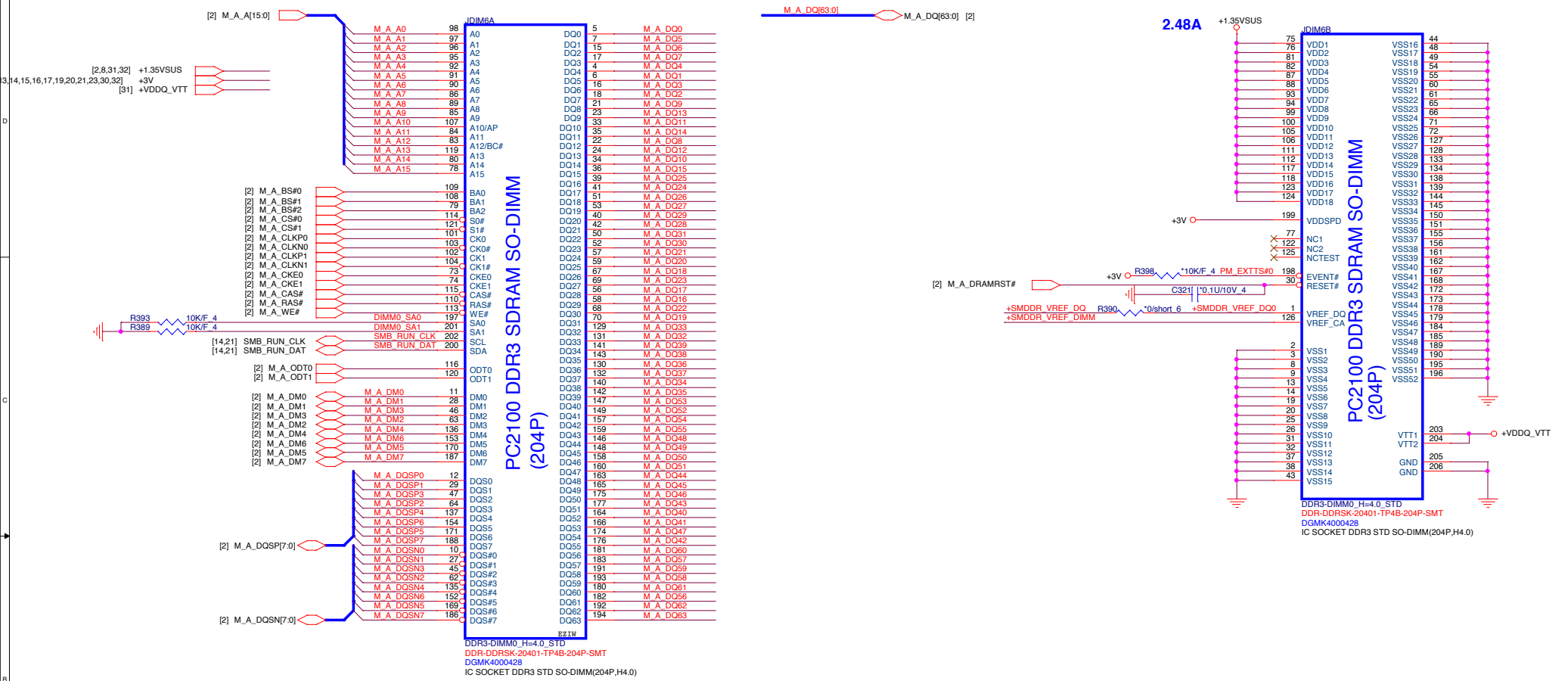

9
U12H
8 OF 13
VLV_M_D/BGA
REV = 1.15
Quanta Computer Inc.
PROJECT : ZHJ
Valley 8/9 (Power 2)
Size
Document Number
Rev
1A
Date: Monday, June 30, 2014
Sheet 9 of 33
www.Vinafix.vn

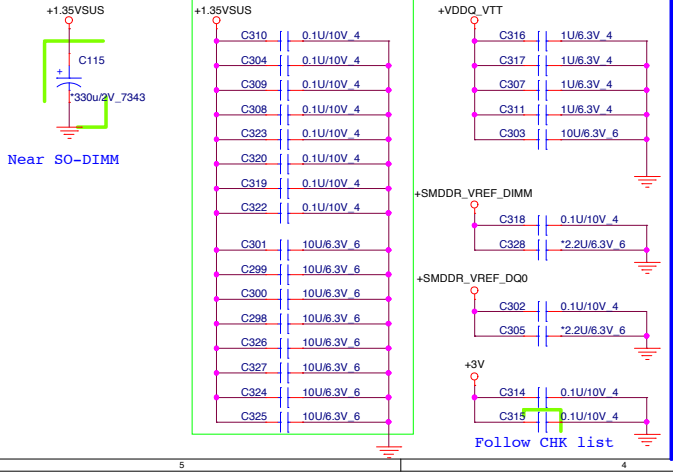


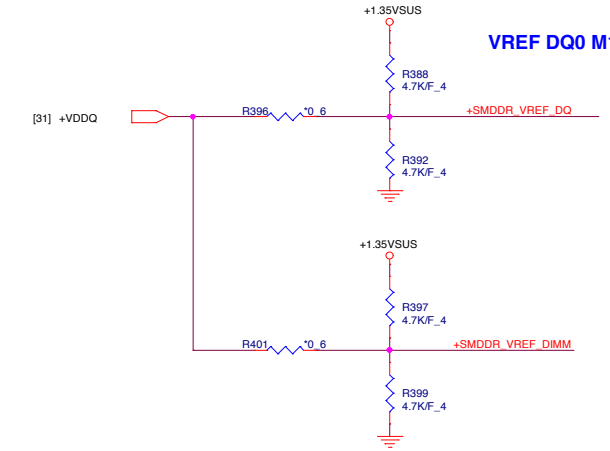
Quanta Computer Inc.

PROJECT : ZHK

Size	Document Number	Rev
	Valley 9/9 (GND)	1A
Date: Monday, June 30, 2014	Sheet 10 of 33	





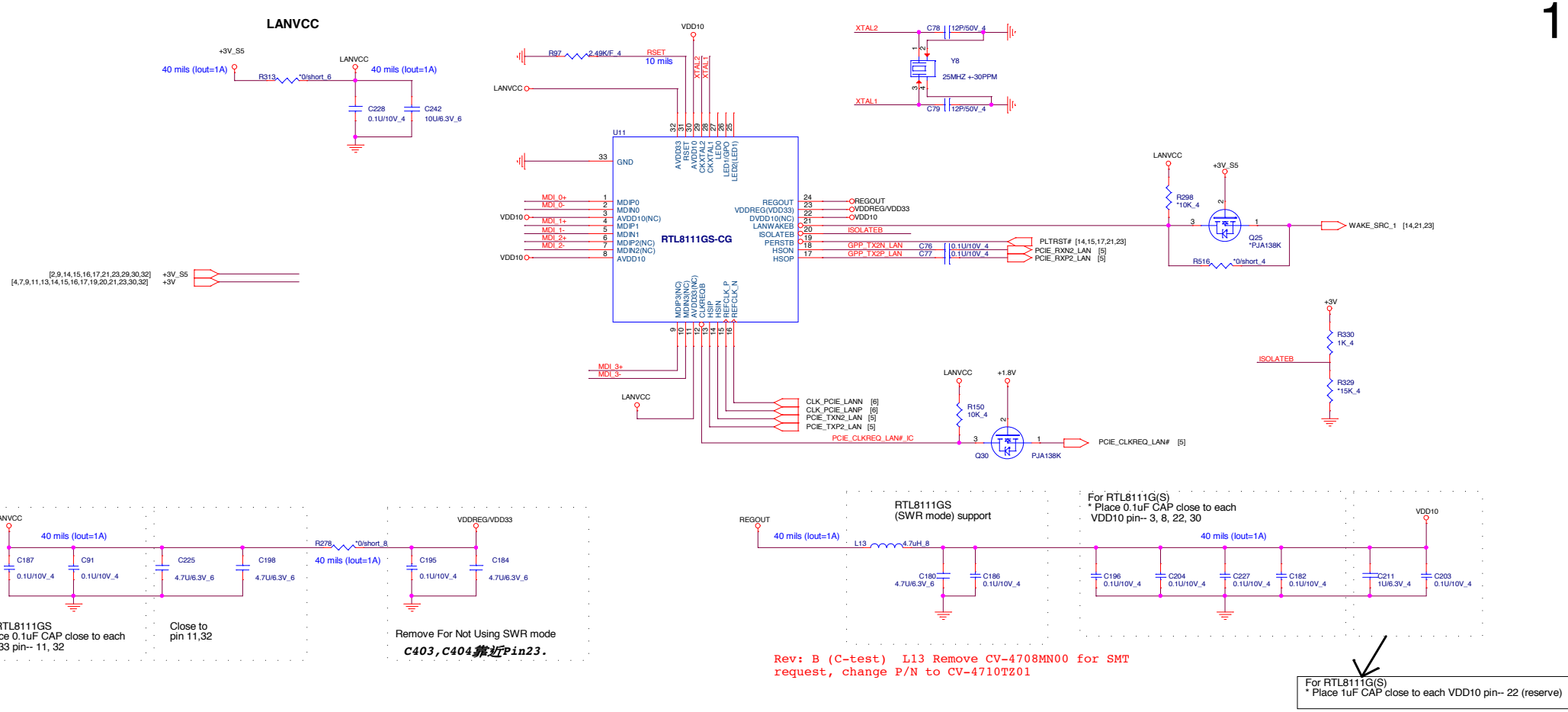


Quanta Computer Inc.

PROJECT : ZHK

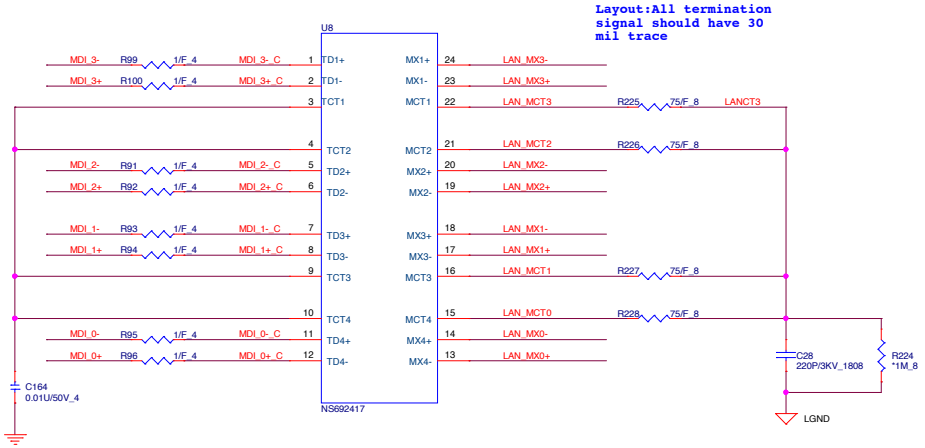
Size	Document Number	Rev
	DDR3 DIMM0-STD(4.0H)	1A

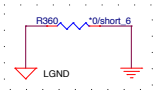
Date: Monday, June 30, 2014 Sheet 11 of 33



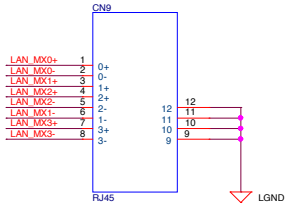
Rev: B (C-test) L13 Remove CV-4708MN00 for SMT request, change P/N to CV-4710TZ01

Tramsformer





RJ45 Connector



Rev: B (C-test) CN9 change main source P/N to DFTJ08FR414
2nd source : DFTJ08FR417

Quanta Computer Inc.
PROJECT : ZHK
Size | Document Number: LAN (RTL8111GS) | Rev: 1A
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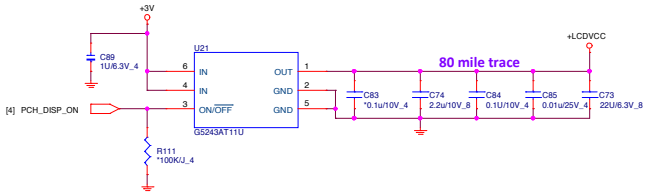
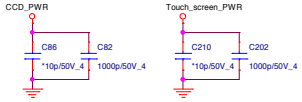
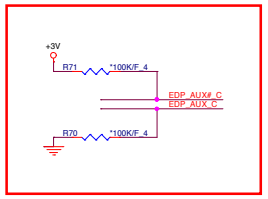
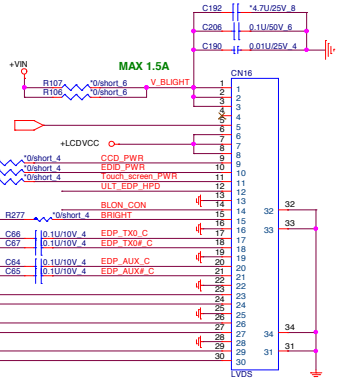
LVDS Conn.



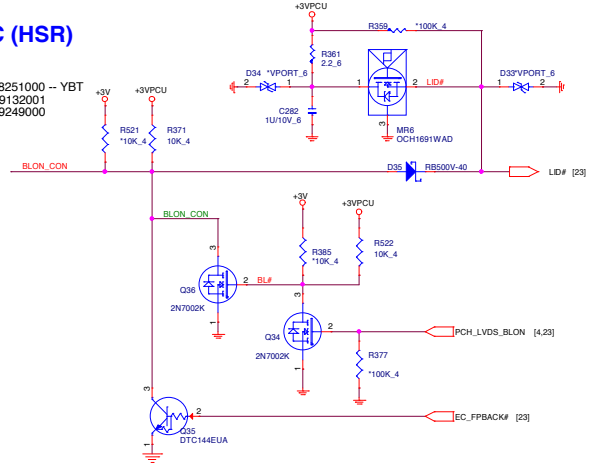


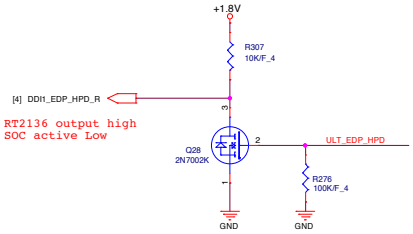




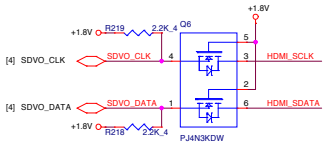
HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000



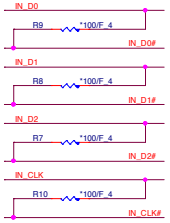


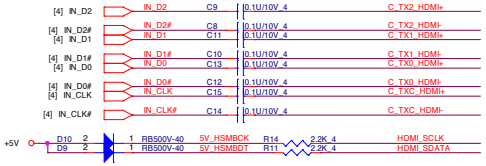
HDMI Conn.

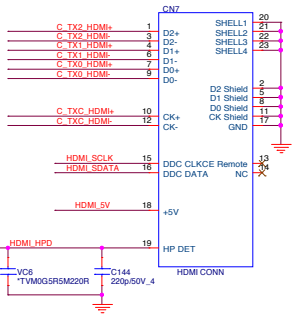


HDMI SMBus Isolation

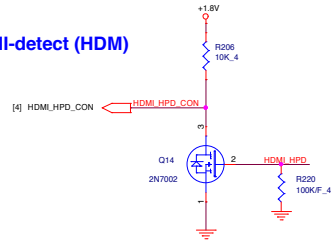
EMI (EMC)

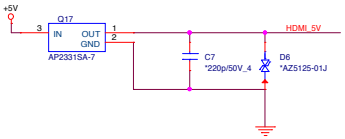


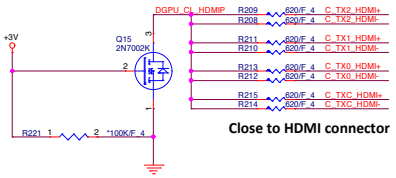




HDMI-detect (HDM)







Close to HDMI connector

Quanta Computer Inc.
PROJECT : ZHK
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[6,7,9,32] +1.8V_S5
[2,9,12,15,16,17,21,23,29,30,32] +3V_S5
[4,5,6,7,9,12,13,15,16,20,21,23,32] +1.8V
[4,7,9,11,12,13,15,16,17,19,20,21,23,30,32] +3V

+1.8V
R84
4.7K_4
[7,15] SOC_SERIRQ SOC_SERIRQ R83 *0/short_4 SERIRQ SERIRQ [23]

Reserve for +1.8V new EC

+1.8V_S5
[6] PCH_SLP_S0# PCH_SLP_S0# Q18 *PJA138K R230 *10K_4 +3V PCH_SLP_S0_N PCH_SLP_S0_N [23]

+1.8V_S5
R550 0_4
R551 *0_4
+3V_S5

+1.8V_S5 R280 10K_4
[6] SOC_PWRBTN#
[6] SOC_PMC_WAKE
U25 74LVC2G07GW
DNBSWON# [23]
WAKE_SRC_1 [12,21,23]
R266 10K_4 +3V_S5

+1.8V_S5 R256 *10K_4
[6] SOC_KCB_SMI
+3V_S5
[5] SOC_KBC_SCI
+1.8V R243 10K_4
U26 74LVC2G07GW
SIO_EXT_SMI# [23]
SIO_EXT_SCI# [23]

+1.8V
[6] TP_INT_C
Q12 *PJA138K
R153 *4.7K_4 +3V
TOUCH_SCREEN_SEL [13]
toTouch screen INT

PJ4N3KDW
Q40A
[7] SMB_SOC_CLK SMB_RUN_CLK [11,21]
R67 4.7K_4
+1.8V +3V
R62 4.7K_4
[7] SMB_SOC_DATA SMB_RUN_DAT [11,21]
Q40B PJ4N3KDW

[2,23] EC_PWROK R56 *0/short_4
[23] DPWROK_EC R57 *0_4
CORE_PWROK [6]
R49 100K/F_4
GND

[6] SLP_S3# R86 *0_4 R320 *10K_4 GND
Q23A PJ4N3KDW
SUSB# [23]
+1.8V_S5 R268 *10K_4 +1.8VPCU
R245 *10K_4
[2,6] SLP_S4# Q23B PJ4N3KDW
SUSC# [23]
R87 *0_4 R324 *10K_4 GND

[6] SLP_S0IX# R241 10K_4 +3V_S5
Q21A PJ4N3KDW
SLP_SUS#_EC [23]
+1.8V_S5
[6] SOC_PLTRST# Q21B PJ4N3KDW
PLTRST# [12,15,17,21,23]
R235 10K_4 +3V

+TPVDD_1
+1.8V
R426 200K/F_4
R404 2.2K_4
R408 2.2K_4
GND C339 0.1U/25V_4
U27 PCA9306
C338 0.1U/25V_4 GND
[7] I2C_6_SDA
[7] I2C_6_SCL
I2C_6_SDA_R [15]
I2C_6_SCL_R [15]

For Touch pad : POWER-A

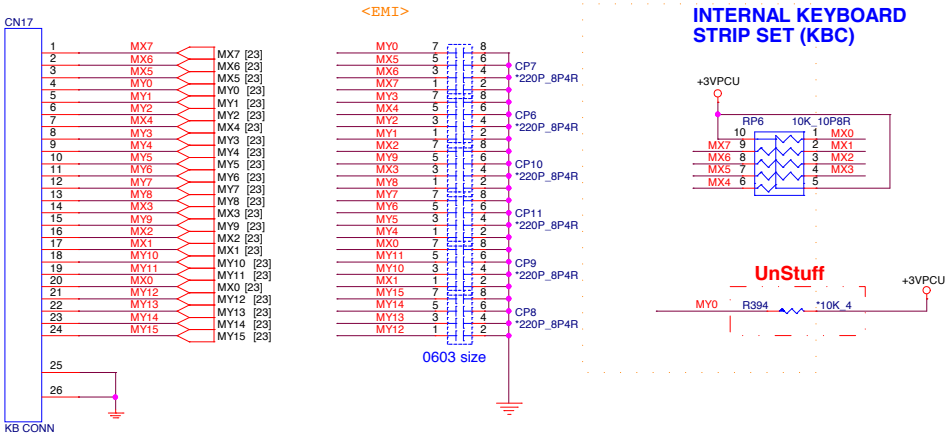
+1.8V_S5
R513 10K_4
[6] TP_SENSOR_INT
TP_SENSOR_INT
Q42 2N7002
GND
+TPVDD_1
R523 10K_4
R534 10K_4
TP_SENSOR_INT_R
TP_SENSOR_INT_R [15,23]
Q45 2N7002
GND

Quanta Computer Inc.
PROJECT : ZHK

Size	Document Number	Rev
	Level Shfiter	1A
Date: Monday, June 30, 2014	Sheet 14 of 33	

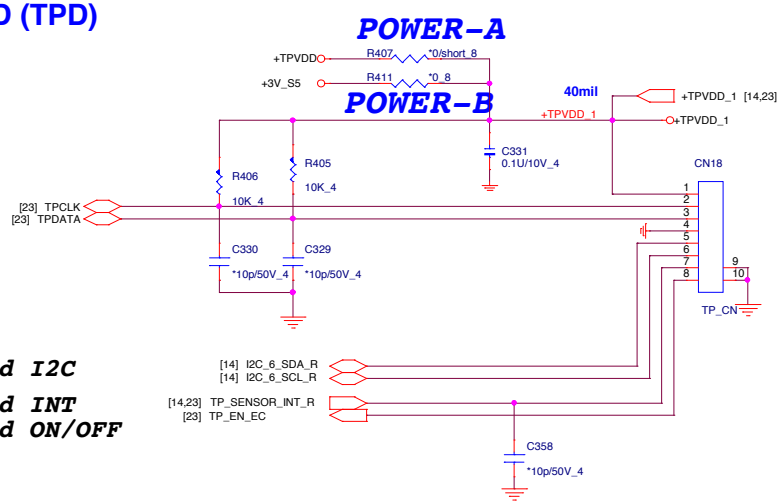
KEYBOARD (KBC)

<20110214(E1A)>
Change CP1~CP6 footprint from
8p4r-0402-smt to 8P4R, for SMT open issue.



Rev: B (C-test) CN17 change ACS P/N from DFFC24FR000 to DFFC24FR110

TOUCH PAD (TPD)



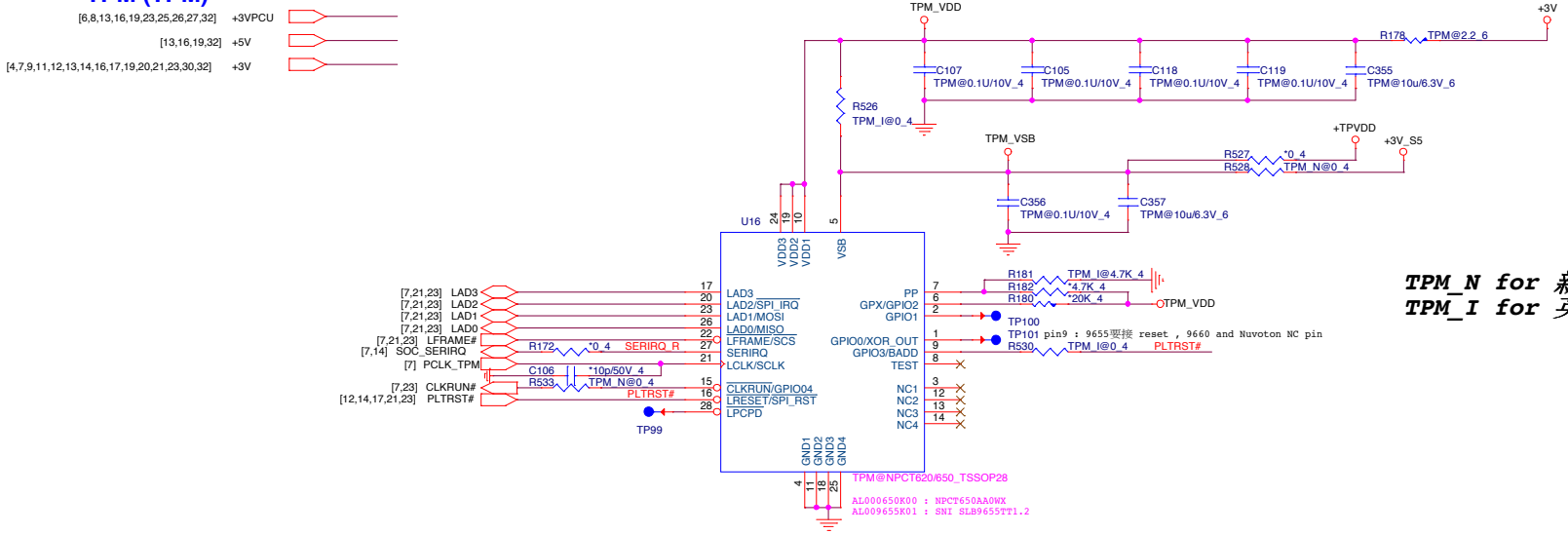
Touch pad I2C

Touch pad INT

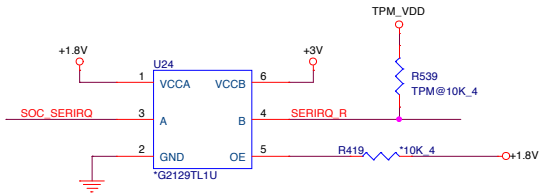
Touch pad ON/OFF

ACER DEFINE
VDD
PS2-CLK
PS2-DATA
GND
I2C-DATA
I2C-CLK
ATTN (INT)
SER-OFF.

TPM (TPM)



TPM_N for 新 唐
TPM_I for 英飛凌---- default



note: serie need to add level shift

Quanta Computer Inc.
PROJECT : ZHK

Size	Document Number	Rev
	KB/BT/TP	1A

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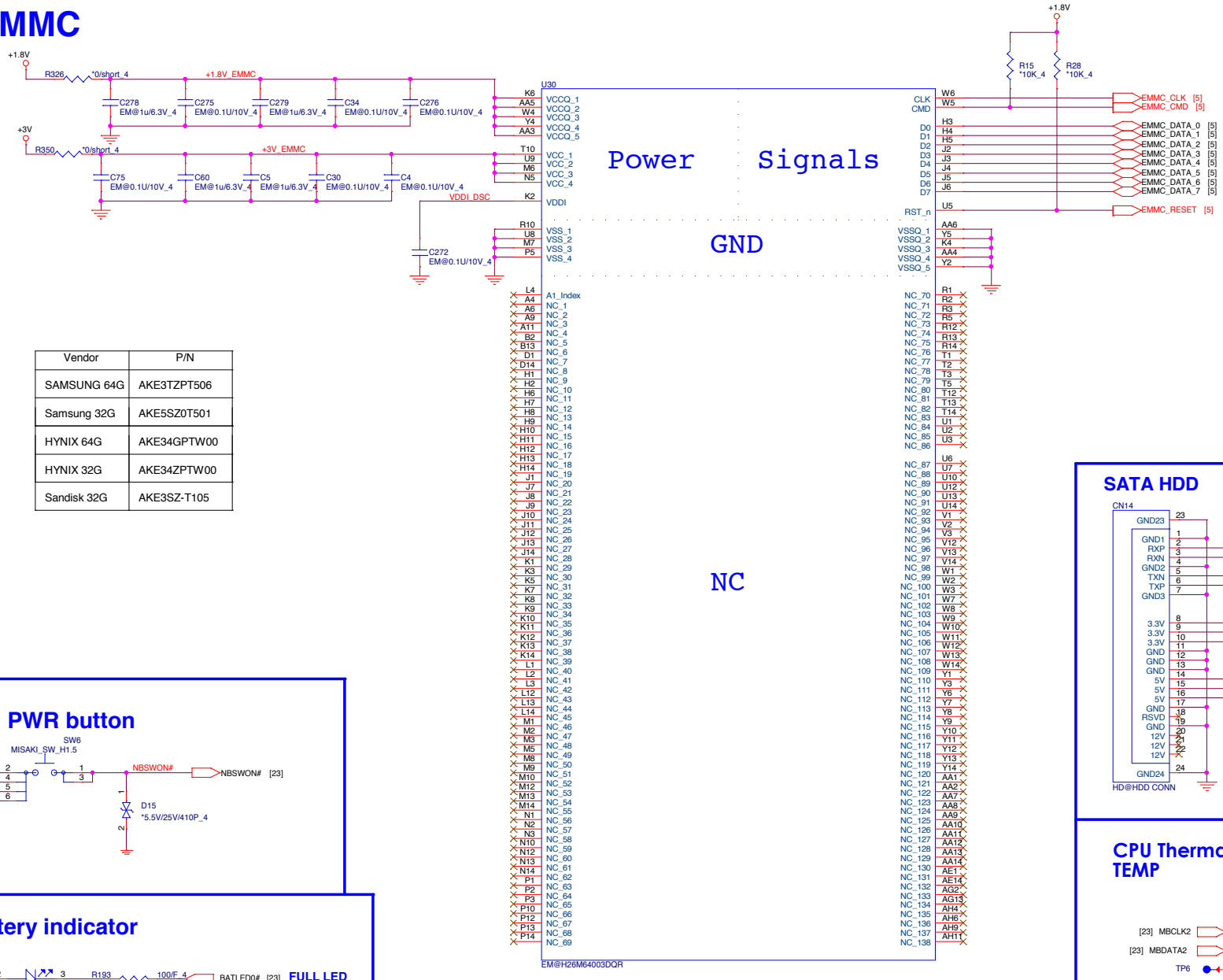
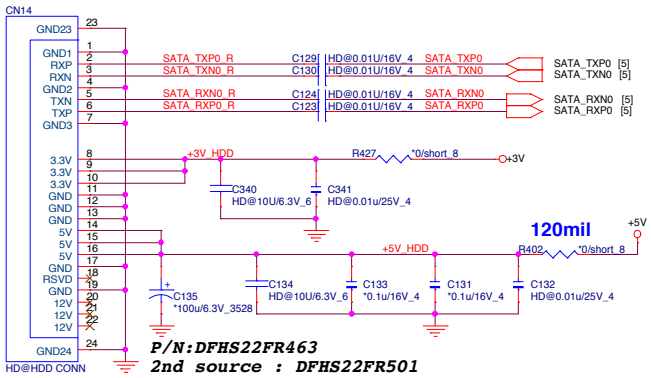
eMMC



Vendor	P/N
SAMSUNG 64G	AKE3TZPT506
Samsung 32G	AKE5SZ0T501
HYNIX 64G	AKE34GPTW00
HYNIX 32G	AKE34ZPTW00
Sandisk 32G	AKE3SZ-T105

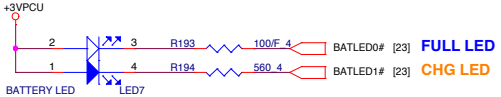
+5V [13,19,32]
+3VPCU [6,8,13,15,19,23,25,26,27,32]
+3V [4,7,9,11,12,13,14,15,17,19,20,21,23,30,32]
+3V_S5 [2,9,12,14,15,17,21,23,29,30,32]

SATA HDD

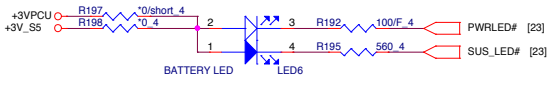


PWR button

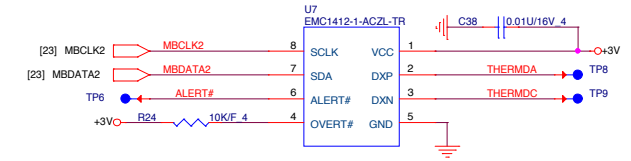
Battery indicator



PWR indicator



CPU Thermal sensor(THS) / MB Local TEMP



Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

Quanta Computer Inc.
PROJECT : ZHK

Size	Document Number	Rev
	HDD/Hall/eMMC/LED	1A
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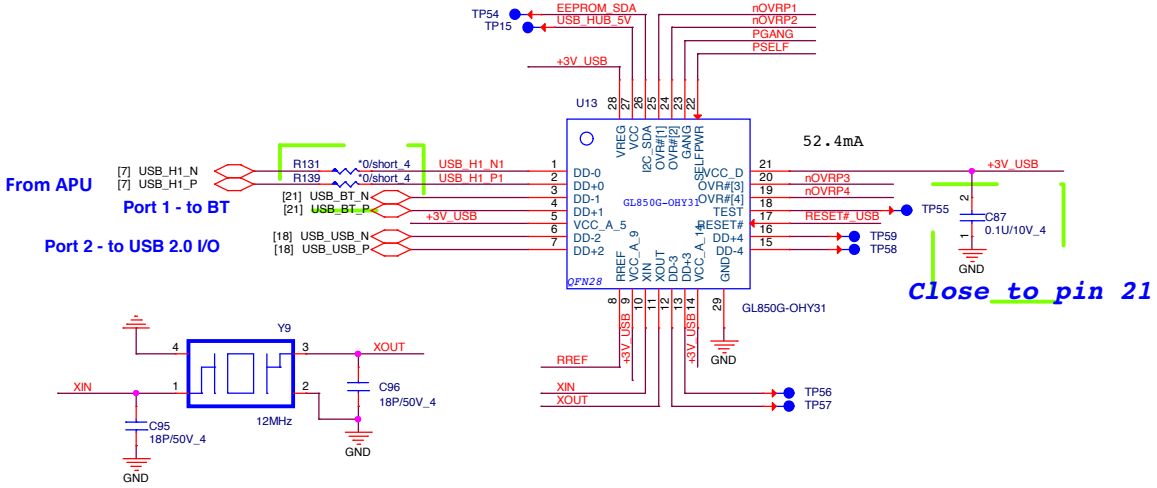

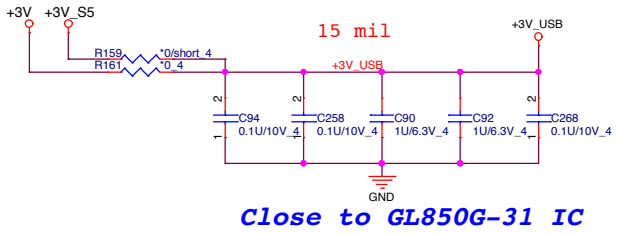

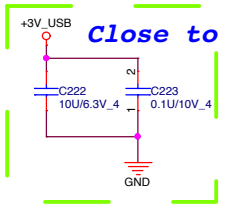

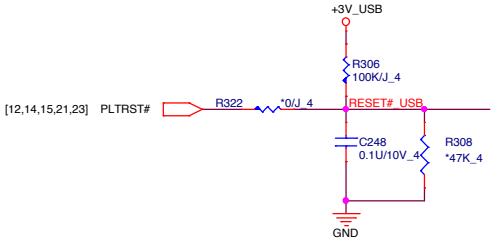

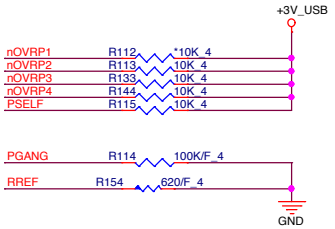

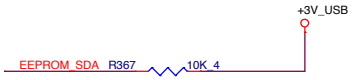

[2,9,12,14,15,16,21,23,29,30,32] +3V_S5
[4,7,9,11,12,13,14,15,16,19,20,21,23,30,32] +3V

Quanta Computer Inc.
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	USB HUB -1	1A
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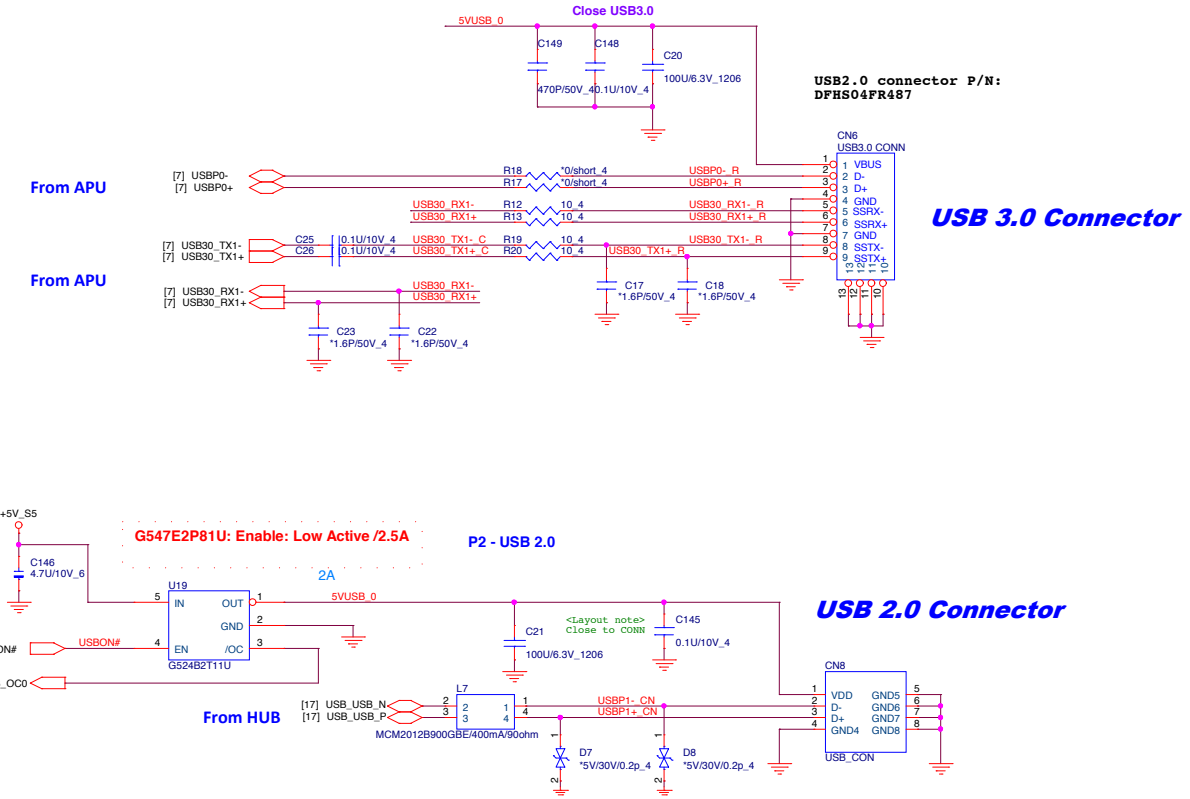
[6,26,28,29,30,31,32] +5V_S5



Quanta Computer Inc.

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	USB / eMMC CONN	1A

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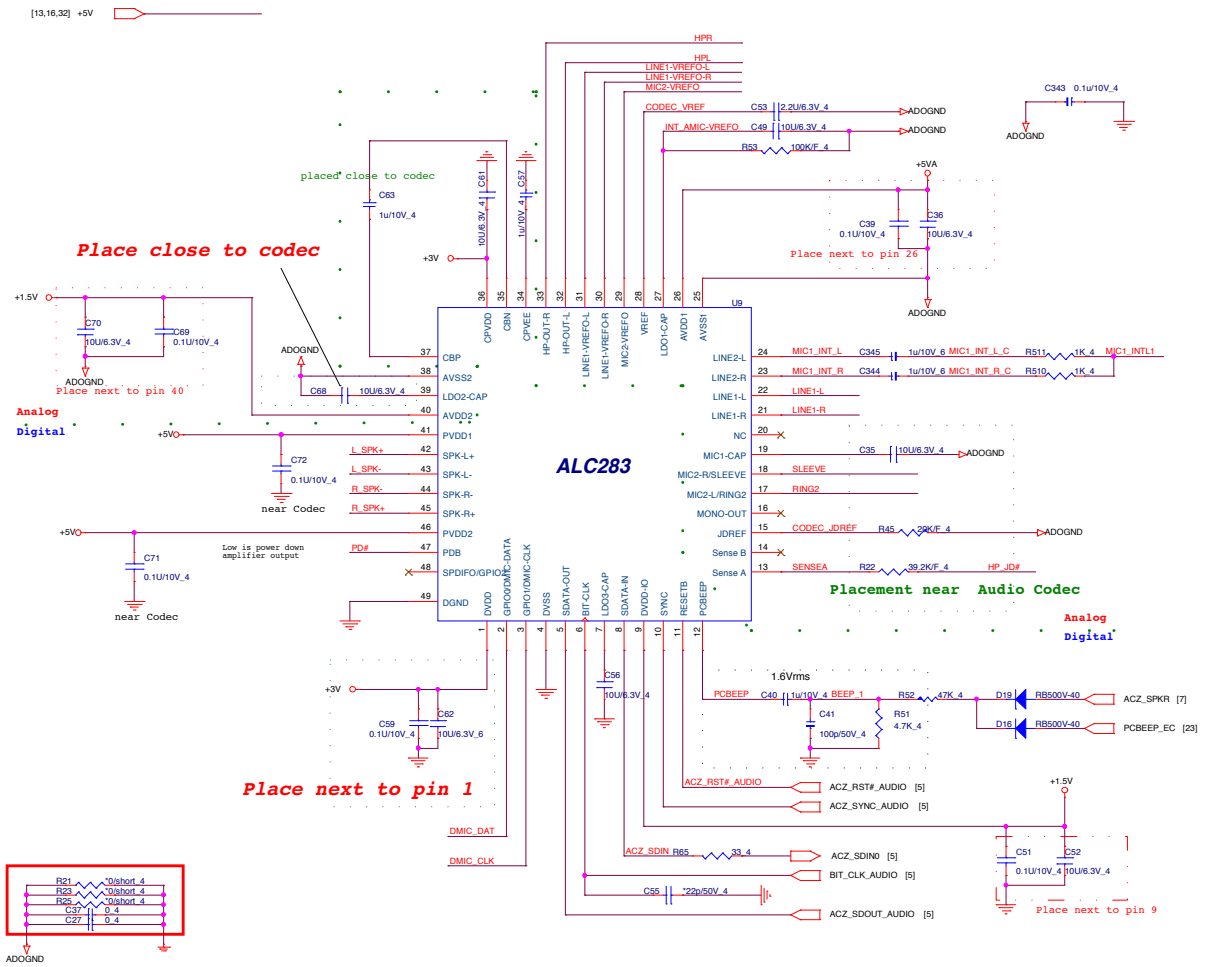
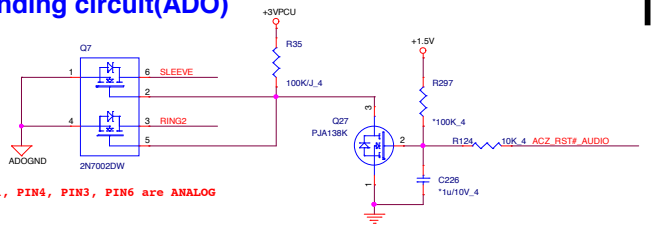
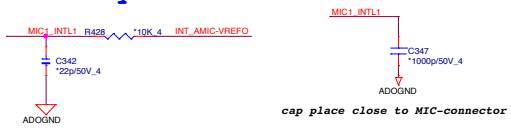
Codec(ADO)



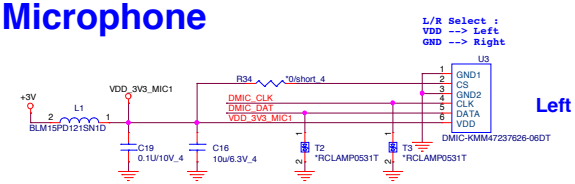
Grounding circuit(ADO)

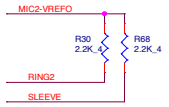


INT MIC array



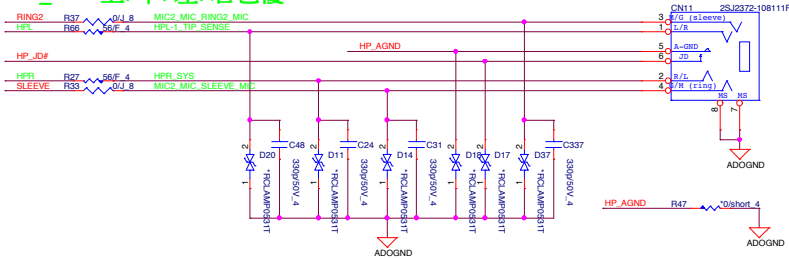
Microphone

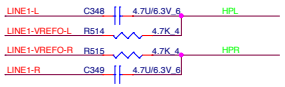




note : change next P/N: DFTJ06FR653
CONN DIP PHONE JACK 6P FR(H4.5)
foot print: phjk-2sj3072-108111f-6p

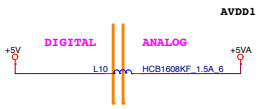
HP_MIC 上/下/左/右包覆AGND



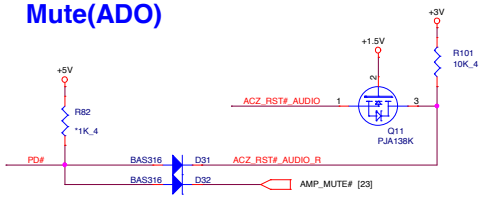


Close to Audio Jack

Codec PWR 5V(ADO)

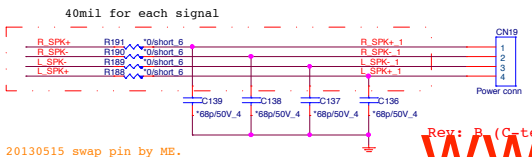


Mute(ADO)



Internal Speaker

footprint 88266-040xx-xxx-4p-1



Rev: B (C-test) CN19 change ACS P/N from DFHD04MRA75 to DFHD04MR211

Quanta Computer Inc.
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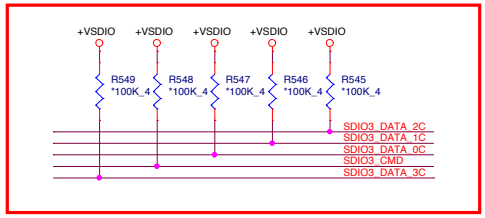
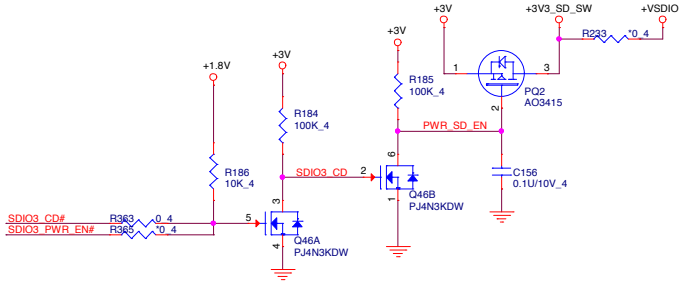
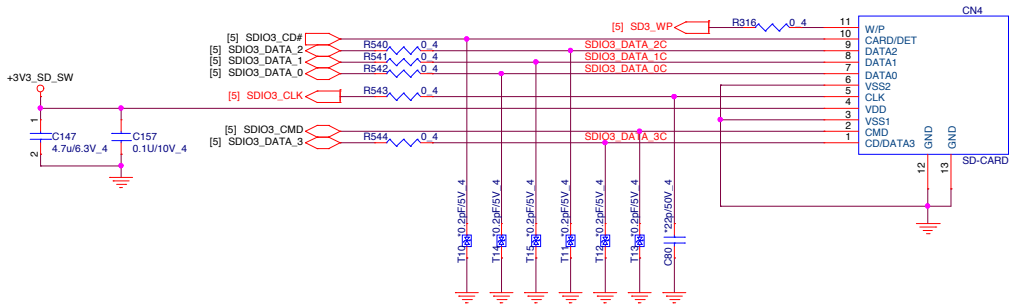
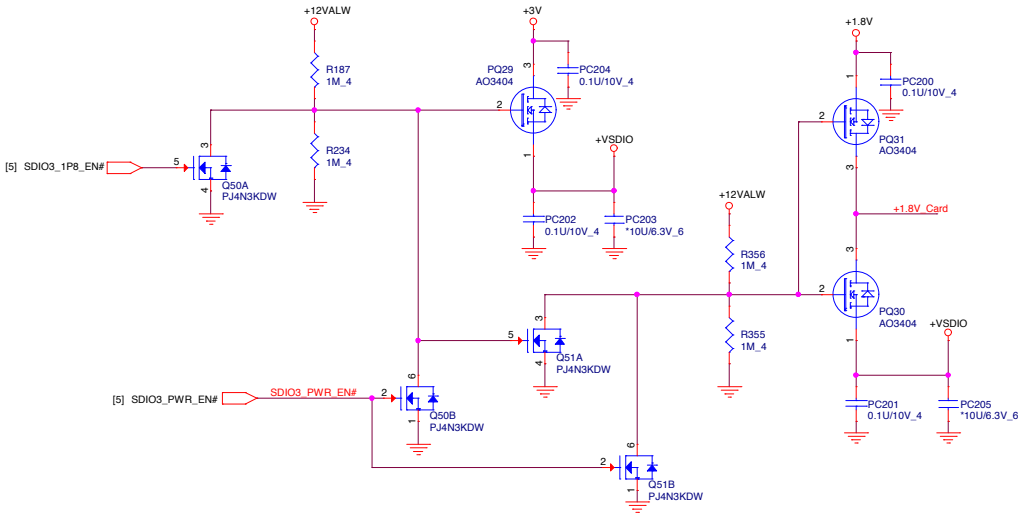


SD_CARD_DET_N
L: Card inserted
H: Card remove







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	Cardreader GL834L	1A

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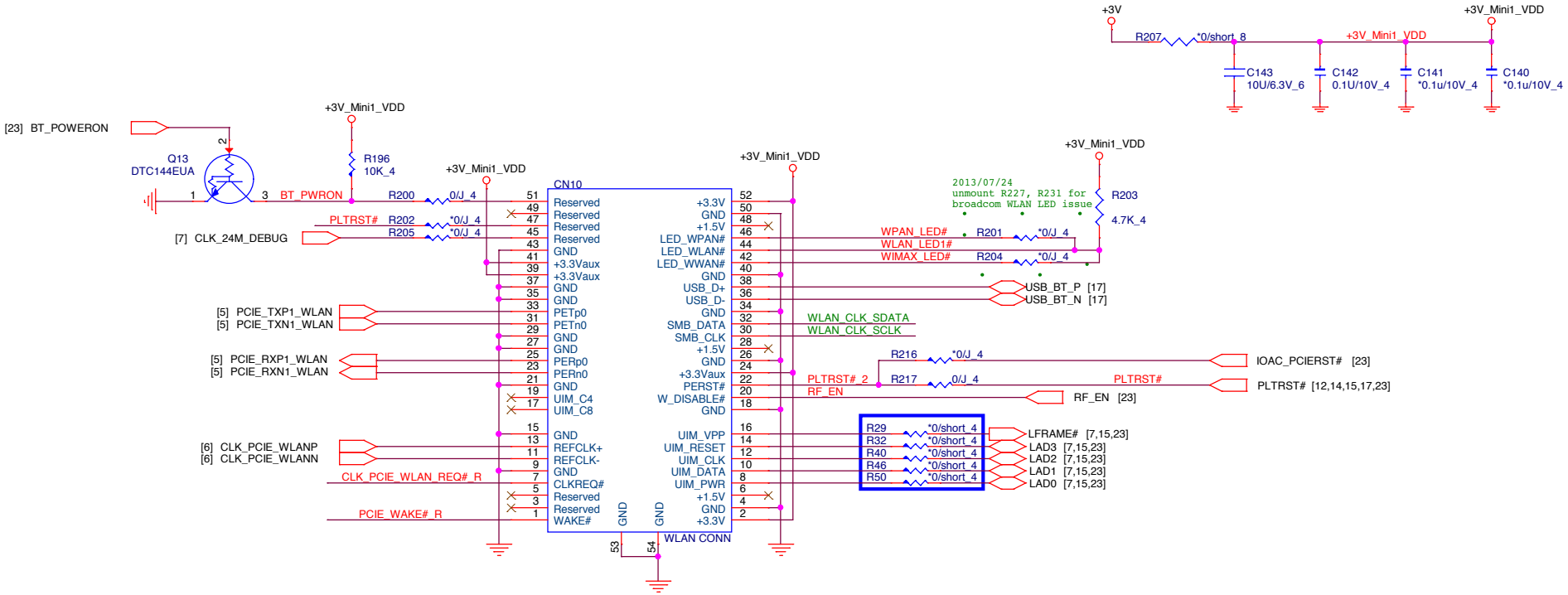
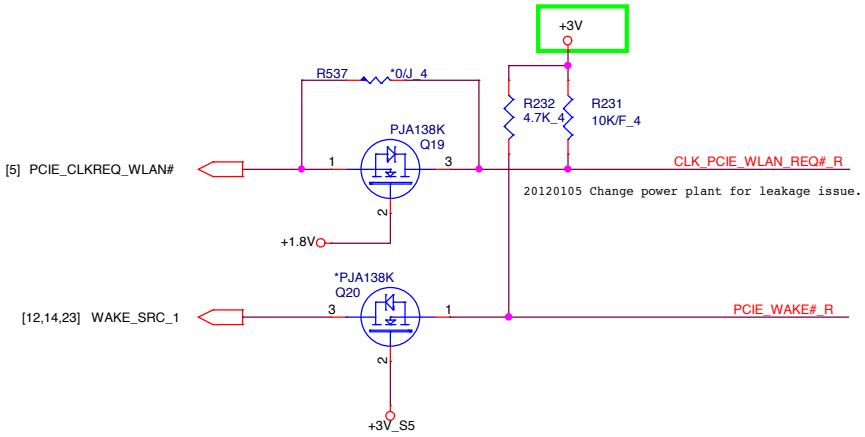
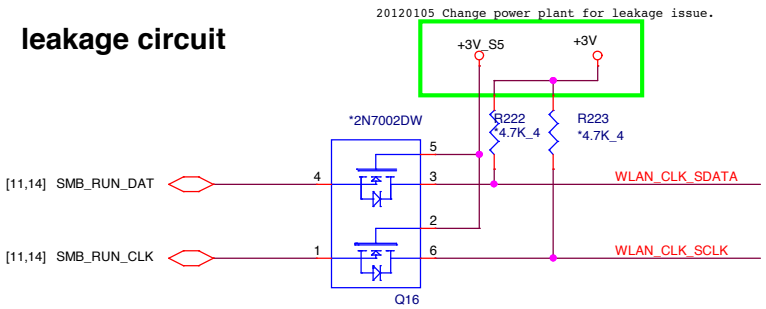
WLAN





leakage circuit



[4,5,6,7,9,12,13,14,15,16,20,23,32] +1.8V
[4,7,9,11,12,13,14,15,16,17,19,20,23,30,32] +3V
[2,9,12,14,15,16,17,23,29,30,32] +3V_S5

Quanta Computer Inc.
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	WiFi & BT	1A
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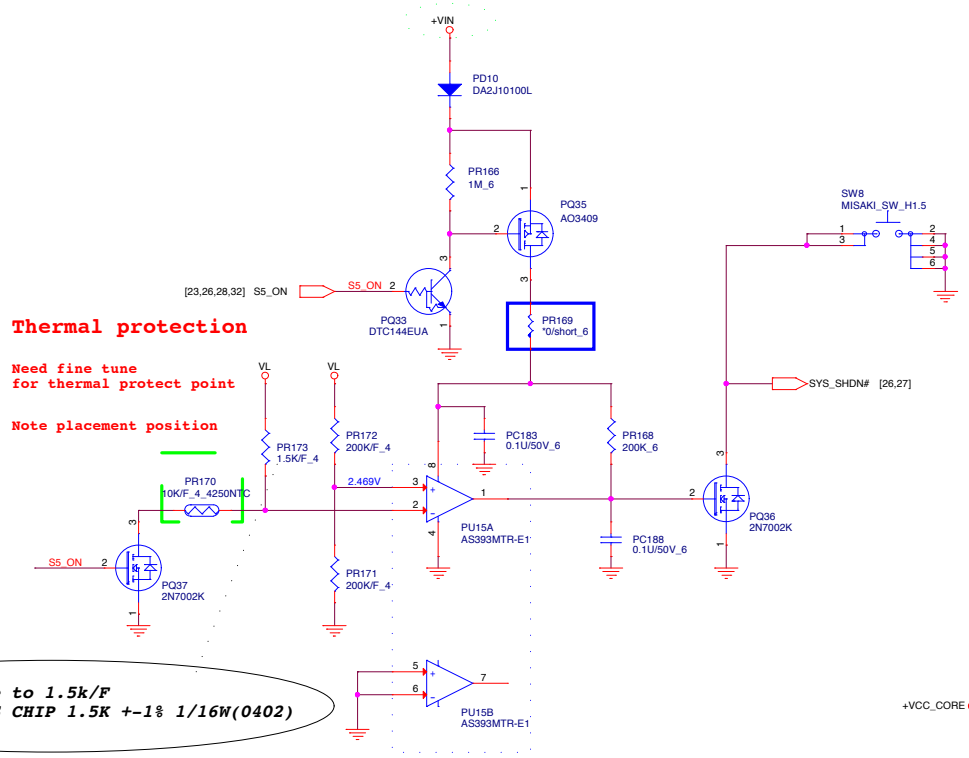
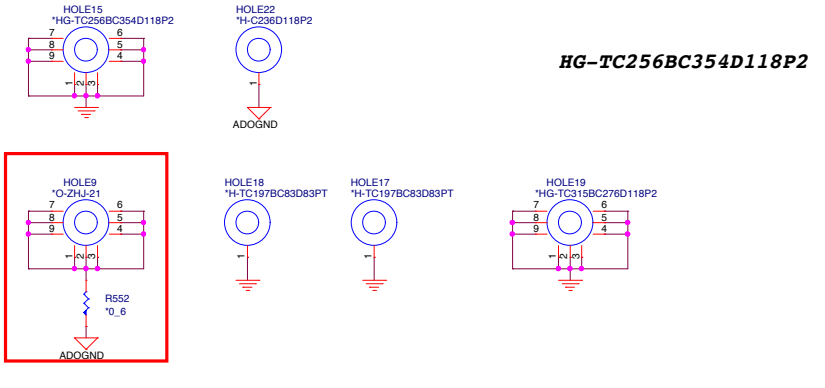
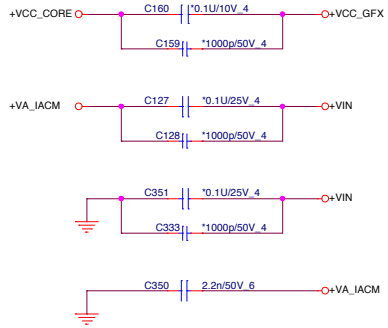


note: PR173 change to 1.5k/F
CS21502FB14 RES CHIP 1.5K +-1% 1/16W(0402)

For EC control thermal protection (output 3.3V)





Quanta Computer Inc.
PROJECT : ZHJ
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1.8V p/n: AJ009850F02
Discription:IC CONTROLLER(128P)NPCE985LB1DX(LQFP)

note:
GPIO75 EMU_LIDTouch panel enable/disable#Follow ZEA -->ZHJ None
GPIO70 TP_EN_ECTouch pad enable/disable# -->ok
GPIO27 TP_INT_EC#Touch pad interrupt

EC(KBC)

L18 PBY160808T-250Y-N/3A/25ohm_6 — 30mil — +A3VPCU
C109 0.1U/10V_4, C103 10U/6.3V_6
E775AGND, VCCSPI
+3VPCU R376 2.2_6 +3VPCU_EC — 0.03A(30mils)
C290 4.7U/6.3V_6, C102 0.1U/10V_4, C288 *.1u/16V_4, C125 0.1U/10V_4, C296 39p/50V_4, C108 0.1U/10V_4

985L-A0 connects to +3vpcu / 985L-B1 connects to +1.8v_s5
220121130 change to 39p capacitor for ESD

+1.8VPCU R357 0/J_6 VCCSPI — C284 10u/6.3V_6

PLTRST# — C359 *0.1U/10V_4

+3V R395 10K_4 SIO_EXT_SC# — R370 10K_4 SIO_EXT_SMI#
2013/07/30
Reserve R477, R478 for EC chip PU function issue.

U18 NPCE985LA0DX

[7,15,21] LFRAME#	3	LFRAME
[7,15,21] LAD0	126	LAD0
[7,15,21] LAD1	127	LAD1
[7,15,21] LAD2	128	LAD2
[7,15,21] LAD3	1	LAD3
[7] CLK_24M_KBC	2	LCLK
[7,15] CLKRUN#	8	GPIO11/CLKRUN
SIO_A20GATE	121	GPIO85/GA20
SIO_RCIN#	122	KBRST/GPIO86
TP19		
[14] SIO_EXT_SCI#	29	ECSCI/GPIO54
TP31	6	GPIO24/LDRQ
[19] AMP_MUTE#	124	GPIO10/LPCPD
[12,14,15,17,21] PLTRST#	7	LRESET
[21] IOAC_PCIERST#	123	GPIO67/PWUREQ
[14] SERIRQ	125	SERIRQ
[14] SIO_EXT_SMI#	9	GPIO65/SMI

LPC

[15] MX0	54	KBSIN0
[15] MX1	55	KBSIN1
[15] MX2	56	KBSIN2
[15] MX3	57	KBSIN3
[15] MX4	58	KBSIN4
[15] MX5	59	KBSIN5
[15] MX6	60	KBSIN6
[15] MX7	61	KBSIN7
[15] MY0	53	KBSOUT0/JENK
[15] MY1	52	KBSOUT1/TCK
[15] MY2	51	KBSOUT2/TMS
[15] MY3	50	KBSOUT3/TDI
[15] MY4	49	KBSOUT4/JEN0
[15] MY5	48	KBSOUT5/TDO
[15] MY6	47	KBSOUT6/RDY
[15] MY7	43	KBSOUT7
[15] MY8	42	KBSOUT8
[15] MY9	41	KBSOUT9/SDP_VIS
[15] MY10	40	KBSOUT10/P80_CLK
[15] MY11	39	KBSOUT11/P80_DAT
[15] MY12	38	KBSOUT12/GPIO64
[15] MY13	37	KBSOUT13/GPIO63
[15] MY14	36	KBSOUT14/GPIO62
[15] MY15	35	KBSOUT15/GPIO61/XOR_OUT
	34	GPIO60/KBSOUT16
	33	GPIO57/KBSOUT17

KB

pin14 +VCC_GFX, pin22 +3V_D for ATI, pin24 +1V for ATI, pin26 +1.8V_GPU for ATI, pin28 GPU_RST#
pin13 GFX_PWRGD, pin21 dGPU_VRON, pin23 +VGPU_CORE, pin25 +1.5V_GPU, pin27 dGPU_PWROK

note: gpio27 -->TOUCH_PAD_INT

[25] MBCLK	70	GPIO17/SCL1
[25] MBDATA	69	GPIO22/SDA1
[16] MBCLK2	67	GPIO73/SCL2
[16] MBDATA2	68	GPIO74/SDA2
	119	GPIO23/SCL3
	120	GPIO31/SDA3

SMB

Reserve for writing ME ROM

[15] TPCLK	72	GPIO37/PSCLK1
[15] TPDATA	71	GPIO35/PSDAT1
[5] EN_OVERRIDE	10	GPIO26/PSCLK2
	11	GPIO27/PSDAT2
[14,15] TP_SENSOR_INT_R — R420 *0/J_4 — TP_INT_EC#	77	GPIO00/32KCLKIN
[25,30] MAINON		

PS/2

PECI interface should be used on Bay Trail platform, thus VTT pin can wire to GND and PECI signal can be left un-connected.

TP36 — R372 *0/short_4 — +1.05V_VTT_EC
R374 *43_4 — EC_PECR_R

VTT	12	
PECI	13	

GND1 5, GND2 45, GND3 78, GND4 89, GND5 116, GND6 103, AGND, VCORF 44

L14 PBY160808T-250Y-N/3A/25ohm_6 — E775AGND
VCORF uR — C126 1U/6.3V_4

+TPVDD_1 — Q41 2N7002K
TP_SENSOR_INT_R — TP_INT_EC#

prevent leakage :
EC internal pull high

R165 2.2_6 — +1.8V — 985L-A0 connects to +3v / 985L-B1 connects to +1.8v
10mA
R166 0/J_6 — D24 *RB500V-40 — C101 4.7U/6.3V_6, C97 0.1U/10V_4, C98 0.1U/10V_4

E775AGND C104 *10u/6.3V_6 ICMNT
C110 0.01u/25V_4

	97	TEMP_MBAT [25]
ICMNT_R R173 *0/short_4 ICMNT	98	ICMNT [25]
	99	
	100	THRM_MOINTOR [8]

A/D

EC_DRAMRST_CNTRL	101	TP18
	105	
	106	

D/A

	64	ACIN [25]
	79	SLP_SUS#_EC [14]
	95	NBSWON# [16]
	96	SLP_SUS_ON [31]
	108	LID# [13]
	93	
	94	EC_FPBACK# [13]
	114	BT_POWERON [21]
	109	DPWROK_EC [14]
	15	
VRON	80	TP45
	17	
	20	SUSC# [14]
	21	SUSB# [14]
	24	
	25	
	26	TP_POWER_ON [32]
CARD_ON_OFF	27	S5_ON [22,26,28,32]
	28	TP44
TP_EN_EC	73	PCH_SLP_S0_N [14]
PWROK_EC_uR R375 *0/short_4	74	TP_EN_EC [15]
RSMRST#_uR R373 *0/short_4	75	EC_PWROK [2,14]
EMU_LID	82	RSMRST# [6]
	83	EMU_LID [13]
	84	RF_EN [21]
	91	WAKE_SRC_1 [12,14,21]
	110	DNBSWON# [14]
	112	
	107	USBON# [18]

GPIO

Note: GPIO75 (pin82) for TOUCHPANEL_ON
pin91 in 985L is 1.8V only

	31	
	17	
FANSIG	63	SUSON [31]
		TP20

TIMER

	32	
	118	
	62	PCBEEP_EC [19]
	65	PWRLED# [16]
	22	BATLED0# [16]
CPUFAN#		TP38
SUS_LED#	16	SUS_LED# [16]
	81	
	66	BATLED1# [16]

<20090721_FAE suggestion>
Stuff 100K and close to EC side for improving power consumption

SOC_SPI_MISO_R1 — R362 100K/J_4

	113	
R535 *0/short_4	14	SUSWARN#_EC [6]
	23	PCH_LVDS_BLON [4,13]
PROCHOT_EC	111	

IR

	86	SOC_SPI_MISO_R1 [6]
	87	SOC_SPI_MOSI_R1 [6]
	90	SOC_SPI_CS#_R1 [6]
	92	SOC_SPI_CLK_R1 [6]
	30	TP41

FIU

20111129 add 33ohm series resistor and for EC FAE suggestion contact to SPI 4M ROM and close to Flash.

VCC_POR# R366 *47K/F_4	85	+3VPCU
	104	AC_PRESENT_EC [5]

VCC_POR
VREF

HWPG(KBC)

+3V_S5 — R382 10K/J_4 — HWPG_1.5V [29,32]

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU

985L-A0 connects to +3v / 985L-B1 connects to +1.8v

SM BUS PU(KBC)

2013/07/31 SMBus Tr fail (spec 1000 ns max, result 1046 ns) Change PU resister(R424,R428) from 10K to 4.7K

+3VPCU
MBCLK R378 4.7K_4
MBDATA R384 4.7K_4
TP_EN_EC R536 *10K/J_4
MBCLK2 R386 10K/J_4
MBDATA2 R383 10K/J_4

H_PROCHOT# [5,30]
PROCHOT_EC — Q33 2N7002K — R358 100K/J_4
Q47 need Replacement at BOT layer.

S5_ON — R391 4.7K_4 — +3VPCU
20120217 Change R630 from10k to 47k for S5 current reduce..

<20130722>Change power from +3V to +3V_S5 for power sequence issue
+3V_S5
[28] HWPG_1.0V
[29,32] HWPG_1.05V — HWPG_1.05V R160 10K/J_4, R162 10K/J_4, R164 10K/J_4
[27] HWPG_1.8V

MAINON — R368 100K/F_4 — GND
SLP_SUS_ON — R343 100K/F_4 — GND
S5_ON — R387 *100K/F_4 — GND
SUSON — R171 100K/F_4 — GND

Quanta Computer Inc.
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COMPRESED IMAGE

Quanta Computer Inc.
PROJECT : ZHK

Size	Document Number	Rev
	Power sequence	1A

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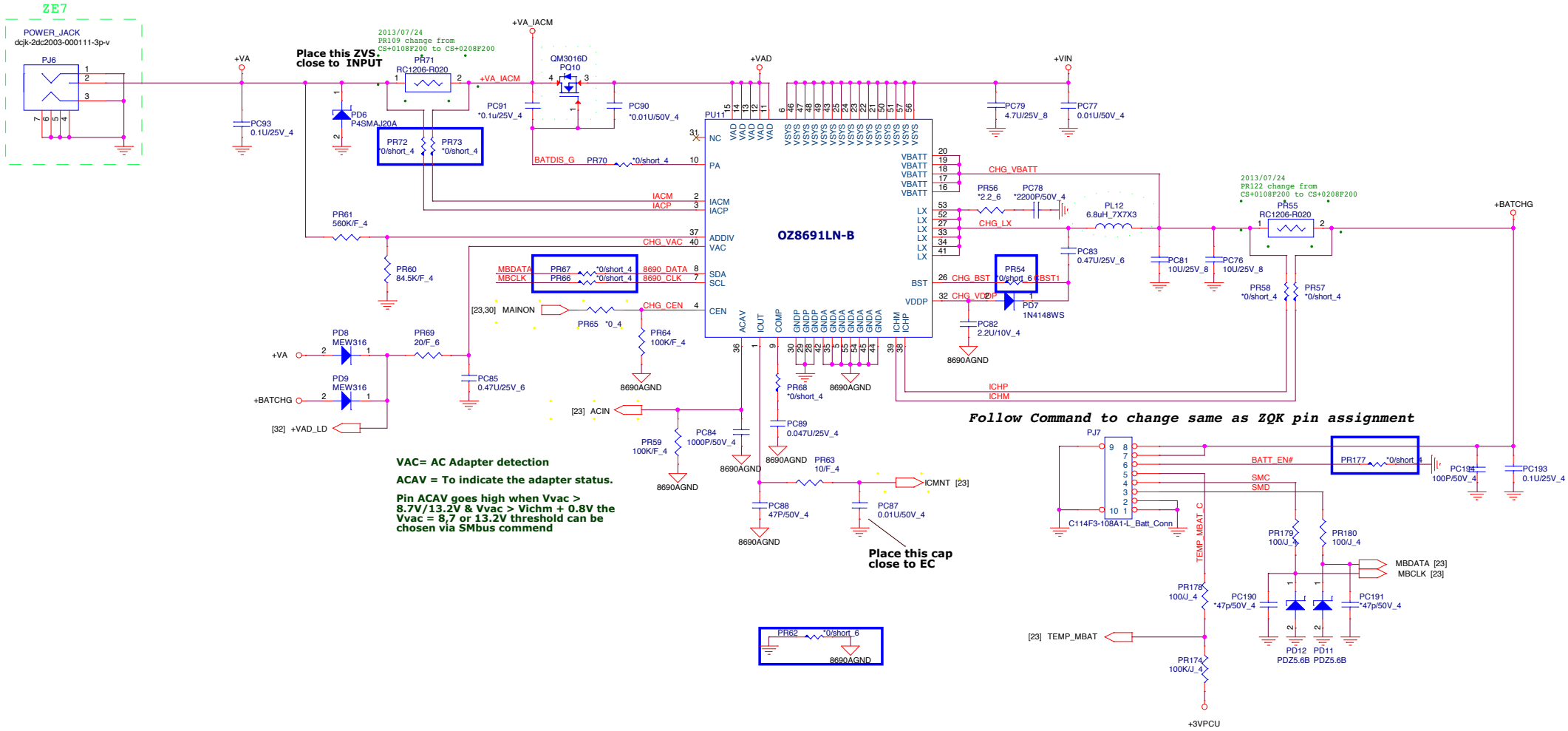

Quanta Computer Inc.		
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Size	Document Number: Charger (OZ8690ALN)	Rev: 1A
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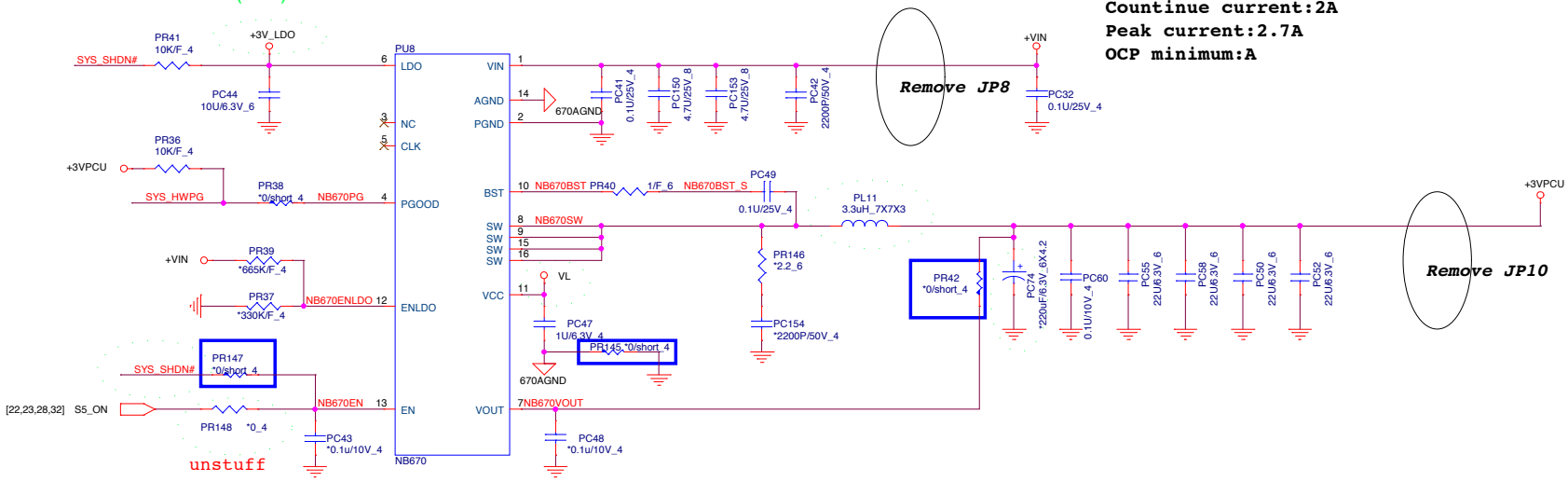
DC/DC +3VPCU/+5V_S5

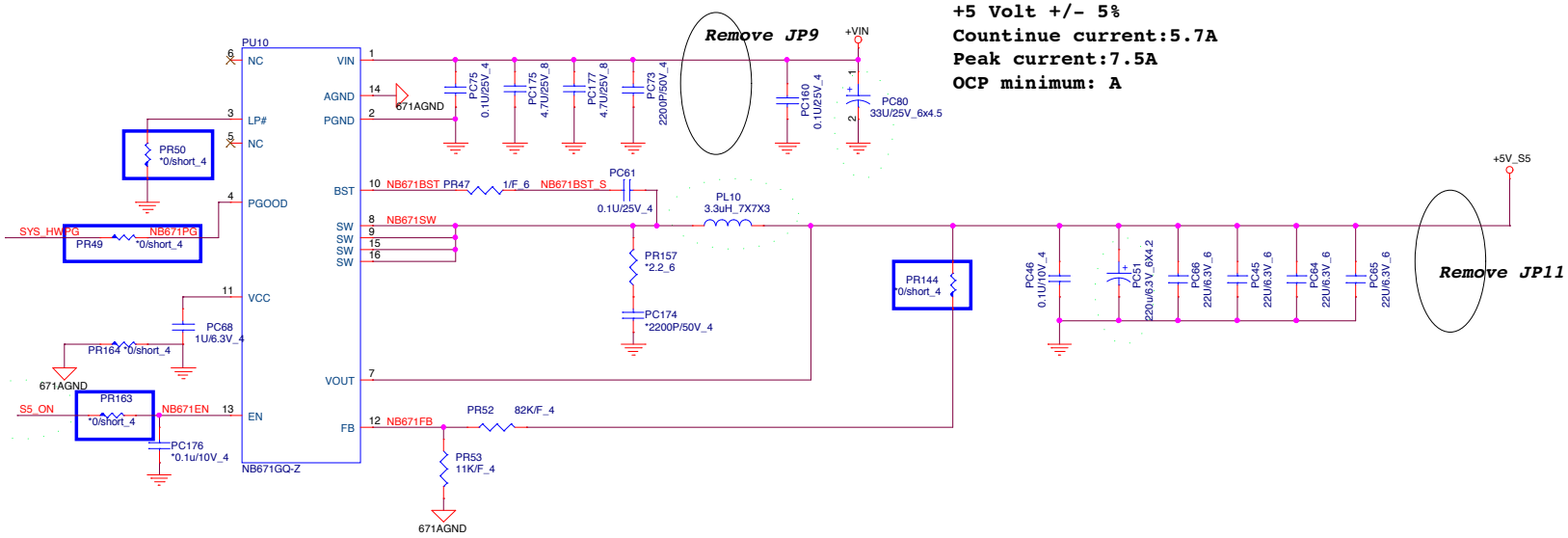
+3VPCU [6,8,13,15,16,19,23,25,27,32]
+5V_S5 [6,18,28,29,30,31,32]
SYS_SHDN# [22,27]

LDO(MAX)=100mA

+3.3 Volt +/- 5%
Countinue current:2A
Peak current:2.7A
OCP minimum:A



+5 Volt +/- 5%
Countinue current:5.7A
Peak current:7.5A
OCP minimum: A



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: 3/5VS5 (NB670/NB669)	Rev: 1A
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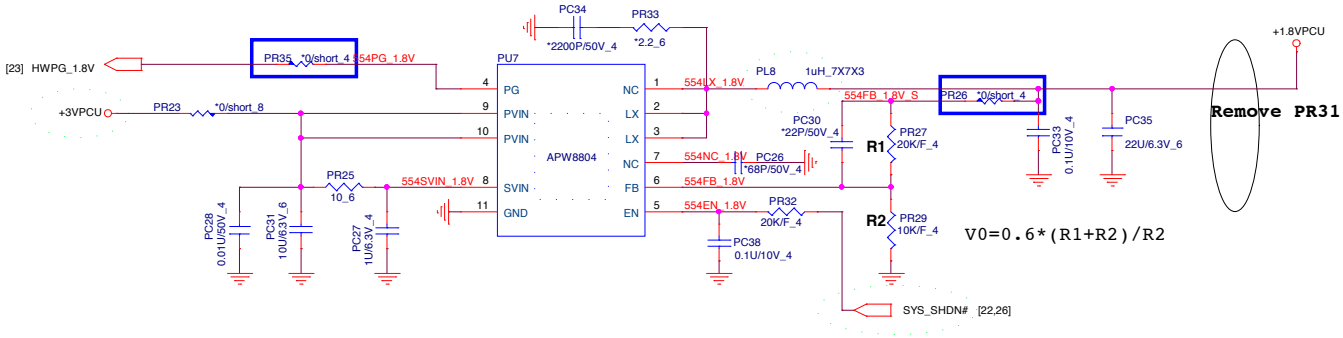
[14,23,32] +1.8VPCU
[6,8,13,15,16,19,23,25,26,32] +3VPCU

+1.8V Volt +/- 5%
Countinue current:0.08A
Peak current:0.11A
OCP minimum:A



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: +1.8VPCU	Rev: 1A
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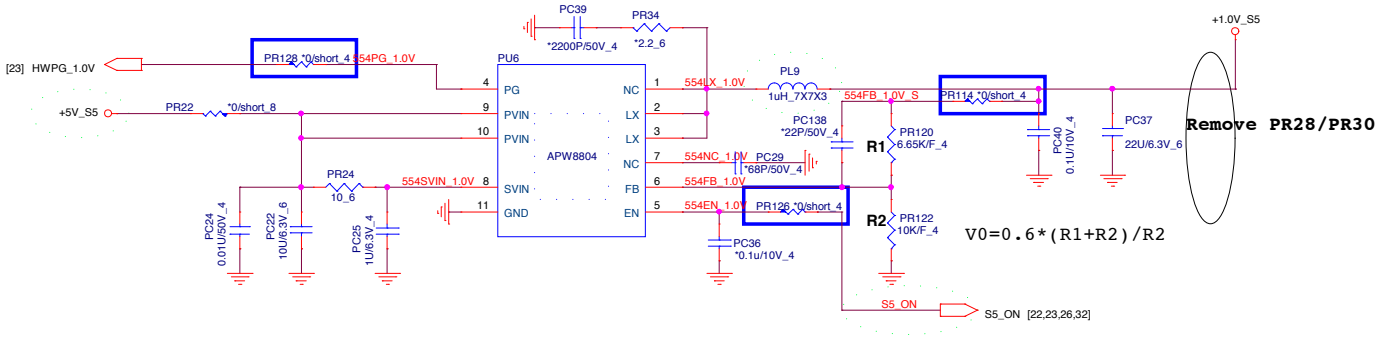
[9,32] +1.0V_S5
[6,18,26,29,30,31,32] +5V_S5

+1.0V Volt +/- 5%
Countinue current:2.4A
Peak current:3.2A
OCP minimum:A



Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	+1.0V	1A
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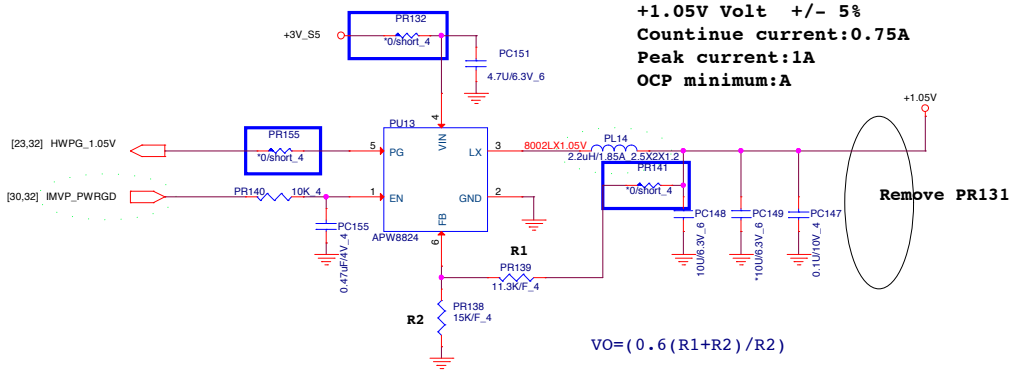
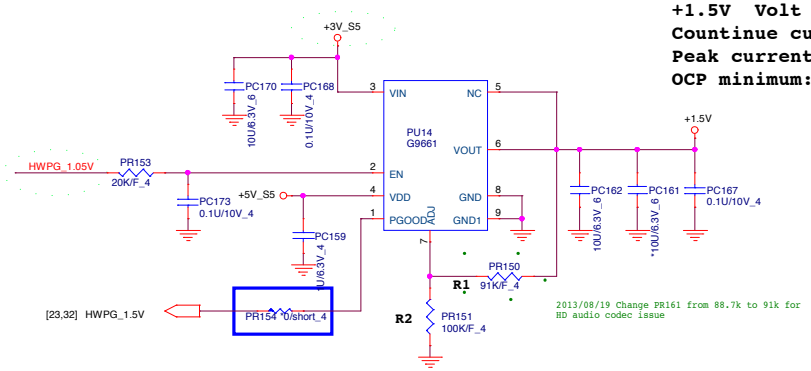
[2,9,12,14,15,16,17,21,23,30,32] +3V_S5

[9] +1.05V

[9,19] +1.5V



+1.05V Volt +/- 5%
Countinue current:0.75A
Peak current:1A
OCP minimum:A



+1.5V Volt +/- 5%
Countinue current:0.023A
Peak current:0.03A
OCP minimum:A

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	+1.05V/1.5V	1A

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20130617 Change +1.05V to +1.0V

Close to VR

VR_SVID_ALERT# close to CPU

VR_SVID_DATA and VR_SVID_CLK close to VR

[5,6,9,32] +1.0V
[8,22] +VCC_GFX
[13,22,25,26,31,32] +VIN
[6,18,26,28,29,31,32] +5V_S5

Parallel

Close to the CPU side.

AXG

Remove JP6

+VCC_GFX
TDC : A
PEAK : 14A
OCP : A
Width : mil

GFX_CORE Load Line :
-5.9mV/A for 2.xW SDP

Close to the VR side.

Close with AXG inductor

Core

Remove JP7

delete PC11

+VCC_CORE
TDC : A
PEAK : 12A
OCP : A
Width : mil

VCORE Load Line :
-5.9mV/A for 2.xW SDP

Close to the VR side.

Close with phase1 inductor

Parallel

Close to the CPU side.

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	+VCC_CORE/+VGFX (ISL95833)	2A
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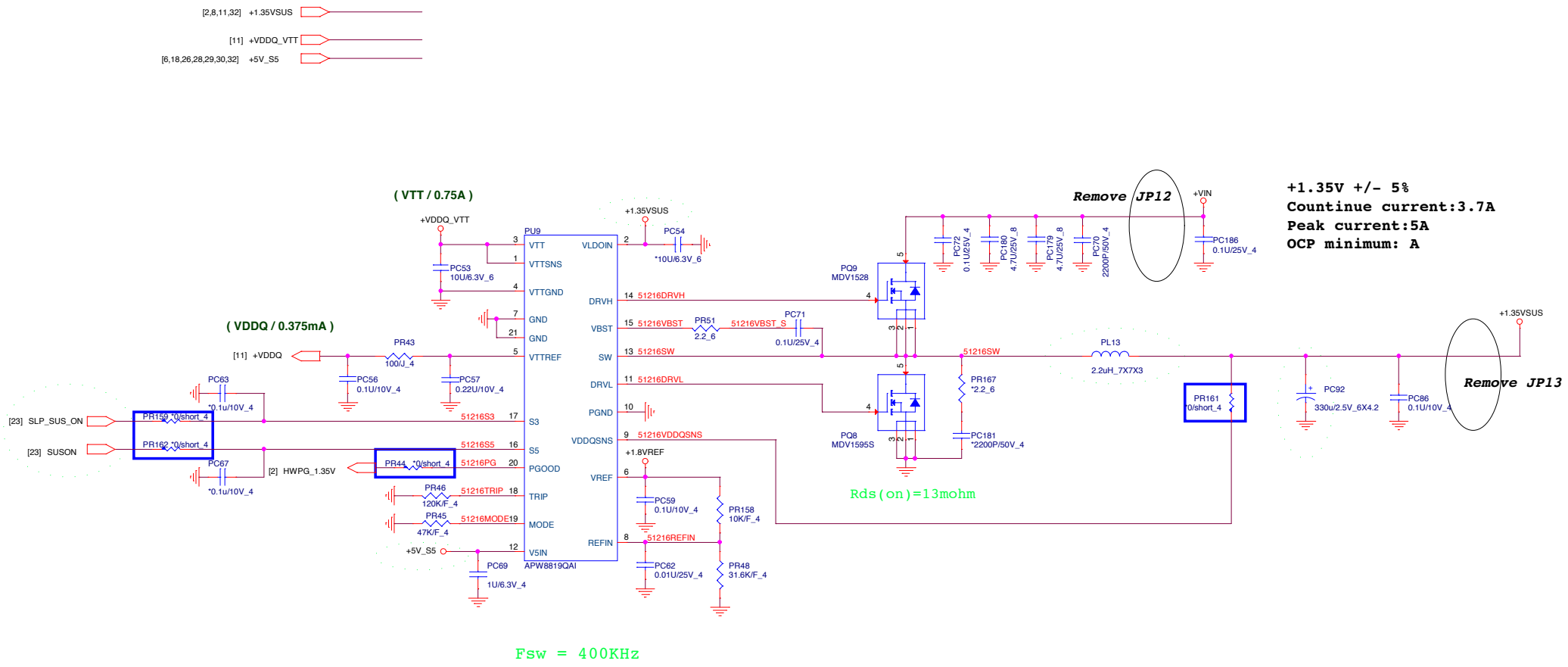

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Size	Document Number	Rev
	DDR3 (APW8819)	1A

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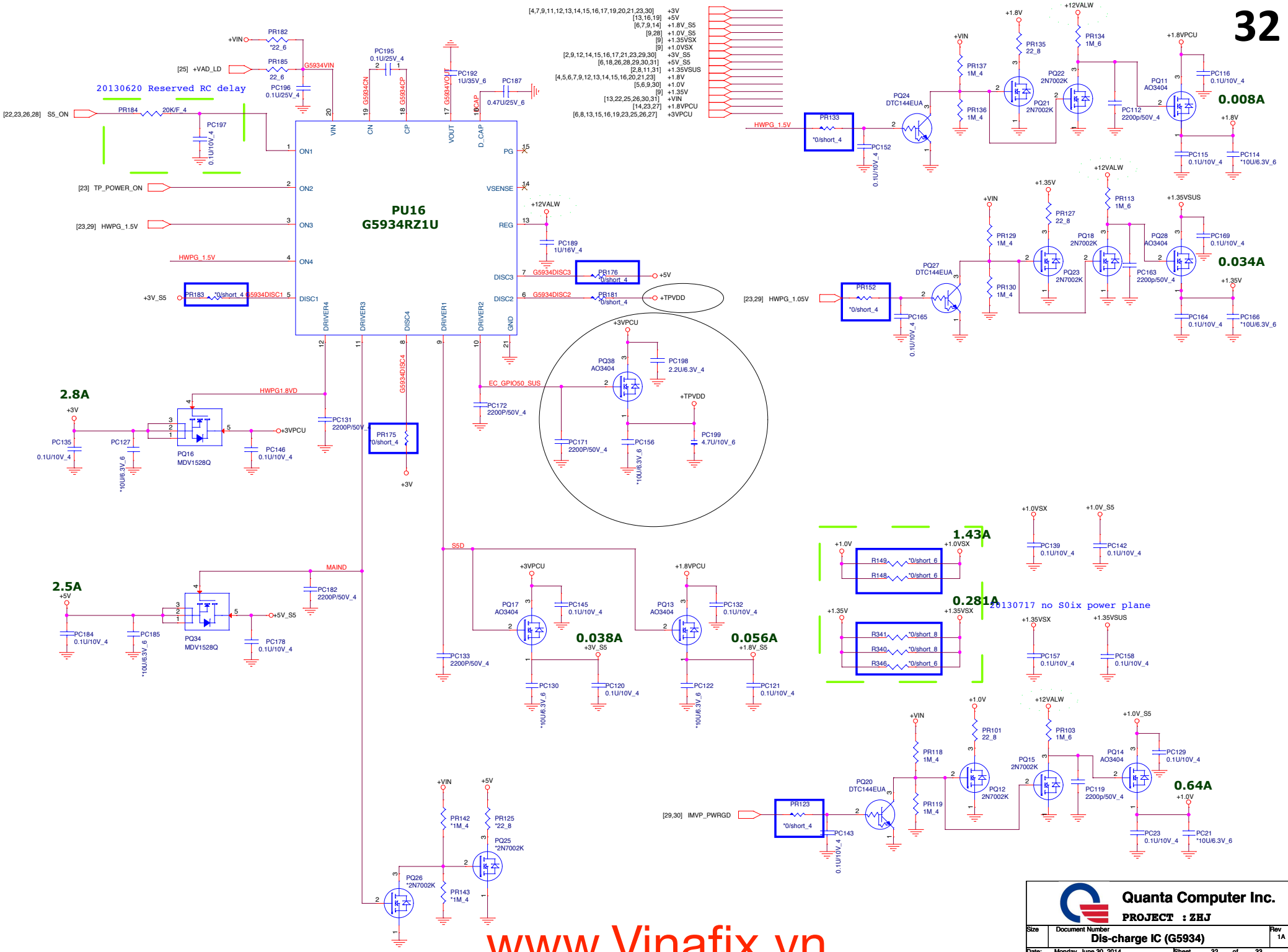

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Size	Document Number	Rev
	Dis-charge IC (G5934)	1A
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Model	Version	CHANGE LIST
ZHK	3A	1. Stuff C27 & C37 for ESD. (page19) 2. Reserve C359 for EMI (page23) 3. R361 Change 0 OHM to 2.2 ohm for ESD(page13) 4. Reserve R545 ,R546 ,R547 ,R548 & R549 for Cardread function(page20) 5. Reserve R552 for ESD (page22) 6. Reserve R70 & R71 for eDP AUX (page13) 7. Add PQ31 for cardread function.

DOC NO.	PROJECT MODEL :	ZHK	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISON:	

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PROJECT : ZHK