SW9 (14") BLOCK DIAGRAM

01

PCB STACK UP
6L Dis. & UMA

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CPU
Arrandale 45nm processor
PAGE 3~6

DDRIII-SODIMM1 PAGE 12 — DDRIII 800/1066 MT/s, 1333MT/s CFD only
DDRIII-SODIMM2 PAGE 13 — DDRIII 800/1066 MT/s, 1333MT/s CFD only

PCI-Express 16X

nVIDIA (40nm)
N11M-GE1 512MB
64 Bit
533p
PAGE 14~18
27MHz

HDMI CON PAGE 20
CRT PAGE 20
Dual Link
LCD CONN PAGE 19

HDMI Level Shifter
Chrontel CH7318C-BF-TR
PAGE 2

DMI LINK
32.768KHz
25MHz

SATA - HDD PAGE 25 — SATA0 150MB
SATA - CD-ROM PAGE 25 — SATA1 150MB
E-SATA PAGE 26 — SATA5 150MB

CRT
LVDS

PCH
Ibex-M(Intel HM55)
PAGE 7~11

CLOCK GEN
9LRS3197
PAGE 2
14.318MHz

Mini PCI-E Card x2
Express Card x1
6,8,10

USB2.0
0,1,2 — USB2.0 Ports X2 PAGE 21
12 — BlueTooth PAGE 22
5 — Webcam PAGE 19
4 — RTS5159 PAGE 21

PCI-E
X1 — Mini PCI-E Card (Wireless LAN / Robson) PAGE 28
SIM Card PAGE 28
X1 — LAN Atheros PCIE-LAN AR8131(M) GagaLAN PAGE 24
25MHz
RJ45/RJ11 PAGE 24
X1 — Express Card

32.768KHz
Keyboard PAGE 26
Touch Pad PAGE 25
ENE KBC
KB3926 C0
PAGE 27
LPC

GMT G9931P1U
FAN PAGE 26
SPI PAGE 27
SPI PAGE 7
MDC CONN PAGE 23

Azalia

Analog ALC272 PAGE 22
microphone PAGE 22
Audio Jacks (Phone/ MIC) PAGE 22
AUDIO Amplifier TPA6017A2 PAGE 23
Jack to Speaker PAGE 23

- UMA GPU CORE (RT8152A) PAGE 31
- SYSTEM POWER RT8206B PAGE 32
- VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204) PAGE 33
- CPU CORE ADP3212 PAGE 34
- VGACORE(1.025V) RT8208A PAGE 35
- DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 36
- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 38

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Quanta Computer Inc.

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Custom	Block Diagram	1A

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CLOCK GENERATOR

+1.05V — L28 HCB1608KF-181T15_6 — +VDDIO_CLK

C640	.1U/10V_4
C644	.1U/10V_4
C643	10U/6.3V_6S
C642	*10U/6.3V_6S

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

U17 — RTM875N-632-GRT — QFN32 — RTM875N-632-VB-GRT

+3V

C646	4.7U/6.3V_6
C654	4.7U/6.3V_6
C652	.1U/10V_4
C641	.1U/10V_4
C645	.1U/10V_4
C651	.1U/10V_4
C653	.1U/10V_4

+VDDIO_CLK

VDD_USB (1), VDD_LCD (5), VDD_SRC (17), VDD_CPU (24), VDD_REF (29), VDD_CPU_IO (18), VDD_SRC_IO (15), SDATA (31), SCLK (32), CPU_STOP# (16), REF_0/CPU_SEL (30), CK_PWRGD/PD#_3.3 (25), XOUT (27), XIN (28), VSS_SATA (9), VSS_USB (2), VSS_LCD (8)

CPU-0 (23), CPU-0# (22), CPU-1 (20), CPU-1# (19), DOT96T_LPR (3), DOT96C_LPR (4), SRC-1 (13), SRC-1# (14), SATA (10), SATA# (11), 27MHz_nonSS (6), 27MHz_SS (7), GND (33), VSS_REF (26), VSS_CPU (21), VSS_SRC (12)

[8,12,13] CGDAT_SMB
[8,12,13] CGCLK_SMB

[8] CLK_ICH_14M — C389 10P/50V_4 — EMI 11/26

R273 10K/F_4 — R295 33_4 — CPU_SEL

CK_PWRGD_R

XTAL_OUT — XTAL_IN

Place the 33 ohm resistors close to the CK 505

CLK_BUF_BCLK_P [8]
CLK_BUF_BCLK_N [8]
133 or 100 Mhz output to PCH

CLK_BUF_DREFCLK [8]
CLK_BUF_DREFCLK# [8]
96Mhz output for generate 48Mhz (USB) and 24 Mhz (HDA)clk

CLK_BUF_PCIE_3GPLL [8]
CLK_BUF_PCIE_3GPLL# [8]
100Mhz output for DMI reference clk

CLK_BUF_DREFSSCLK [8]
CLK_BUF_DREFSSCLK# [8]
100Mhz output for SATA reference clk

CLK_VGA_27M_NOSS — R280 *33_4
CLK_VGA_27M_SS — R278 *33_4
Discrete Only
CLK_27M_NONSS [16]
CLK_27M_SS [16]

C647 18P/50V_4 — EMI 11/26

+3V — R297 1K/F_4 — CK_PWRGD_R — Q28 2N7002E — R298 100K/F_4 — [34] VR_PWRGD_CLKEN#

Y3 — XTAL_IN — 2XTAL_OUT — 14.318MHZ — C388 33P/50V_4 — C387 33P/50V_4

+3V — R294 *10K/F_4 — CPU_SEL — R296 10K/F_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

CPU bracket Hole.

H19 *h-c256d165p2 — H20 *h-c256d165p2 — H35 *h-c256d165p2 — H34 *h-c256d165p2

PAD and HOLE

H31 *h-s276d118p2 — H7 *H-C236D162P2 — H17 *h-c315d118p2 — H11 *h-c315d118p2 — H12 *h-c315d118p2 — H36 H-C236D63P2

H5 *O-SW9-4

AGND

H24 *H-c98d98n — H9 *O-sw9-2 — H10 *O-sw9-3 — H21 *O-sw9-5 — H22 *O-sw9-5

MINI CARD Hole.

H6 *H-C236D162P2 — H8 *H-C236D162P2 — H2 *H-C236D63P2 — H1 *H-C236D63P2

MDC Hole.

H40 H-C236D62P2 — H39 H-C236D62P2

EMI capacitive

+VIN — 10/12

C336	.1U/25V_4
C481	.1U/25V_4
C565	.1U/25V_4
C570	.1U/25V_4
C572	.1U/25V_4
C637	.1U/25V_4
C638	.1U/25V_4
C639	.1U/25V_4

EMI

C378	*.22U/10V_4
C350	*.22U/10V_4
C374	*.22U/10V_4

+3VO

C31	*.1U/10V_4
C323	*.1U/10V_4
C133	*.1U/10V_4
C427	*.1U/10V_4

VGA bracket Hole.

H14 *h-c256d165p2 — H15 *h-c256d165p2

H37 H-C236D63P2 — H16 *h-c315d118p2 — H13 *h-c315d118p2 — H38 *H-C315D118P2

H32 *o-sw9-7 — H18 *h-c315d118p2 — H33 *o-sw9-6

PAD2 MDC_SPRING — PAD3 MDC_SPRING — PAD6 MDC_SPRING

PAD4 MDC_SPRING — PAD5 MDC_SPRING

PAD1 *EMI PAD — PAD7 *EMI PAD — PAD8 *PAD-RE406X157

H3 *h-o110x130d110x130n — H4 *h-o039x102d39x102n

[7,8,9,11,27,31,33,34,39] +1.05V
[3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V

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Quanta Computer Inc.

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Custom	CLOCK & Screw Holes	1A

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	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

U22A

DMI
Intel(R) FDI
PCI EXPRESS -- GRAPHICS

2.7GT/s data rate

Discrete Only

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

U22B

MISC
THERMAL
CLOCKS
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

JTAG MAPPING

Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89

Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

PROJECT : SW9
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Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	1A

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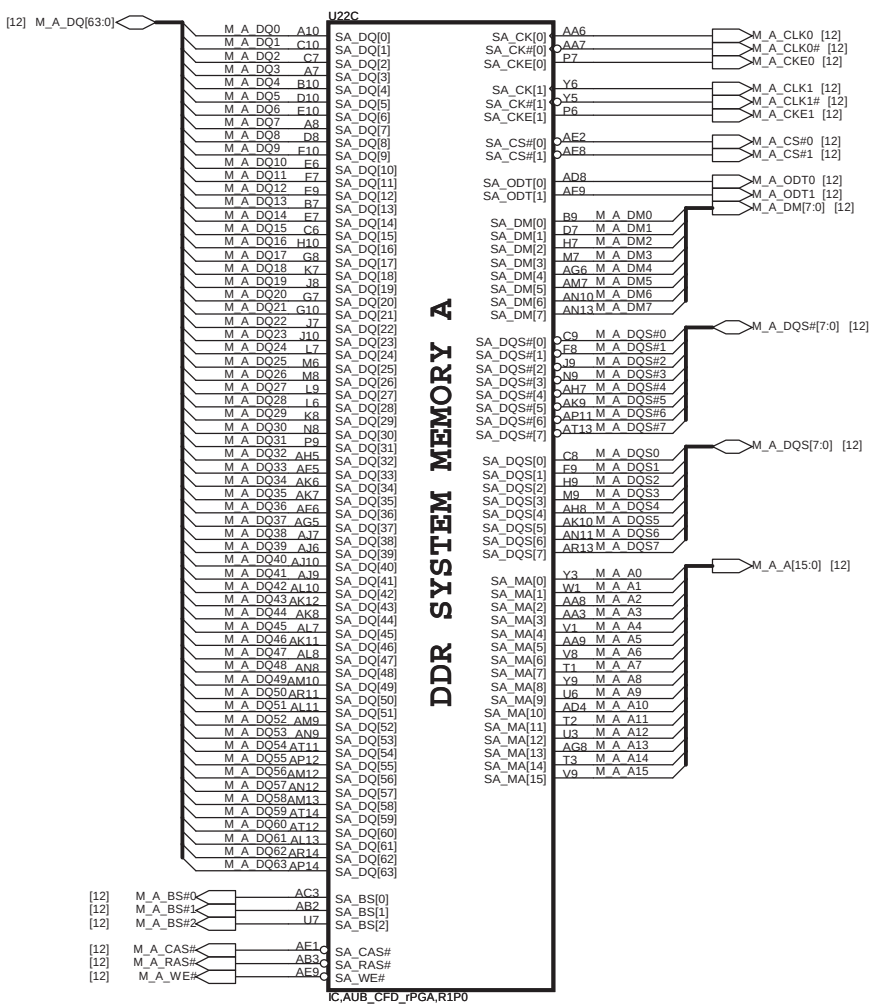
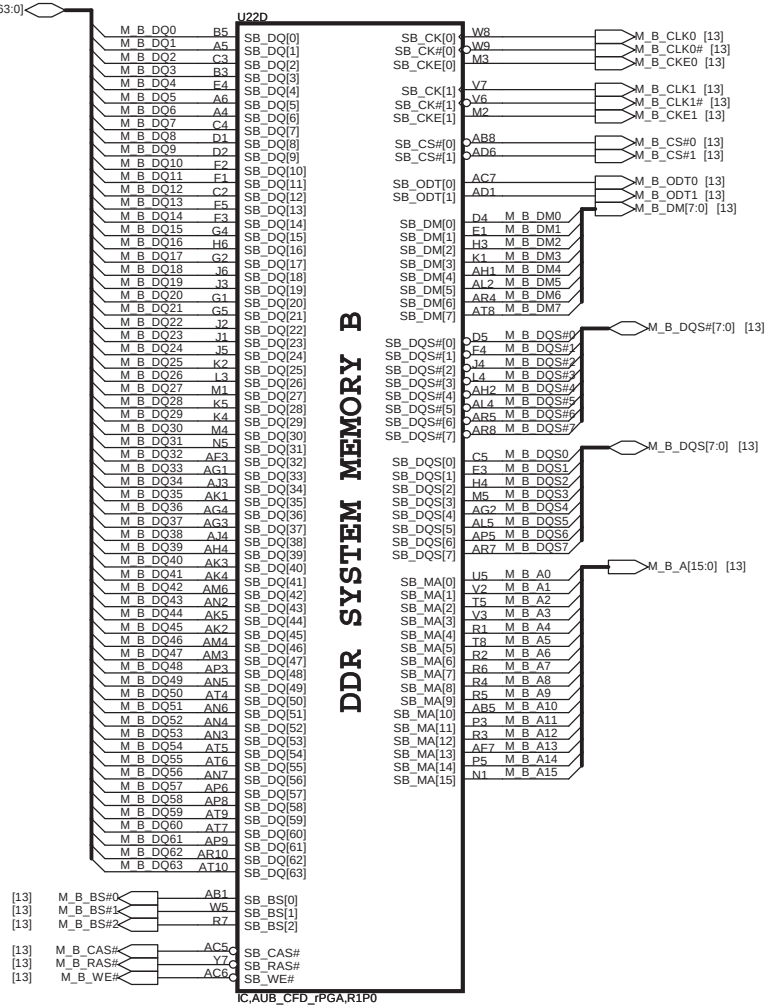
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	1A

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	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

	DIS	UMA
Ra	0 ohm	NA

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 3/4(POWER)	1A

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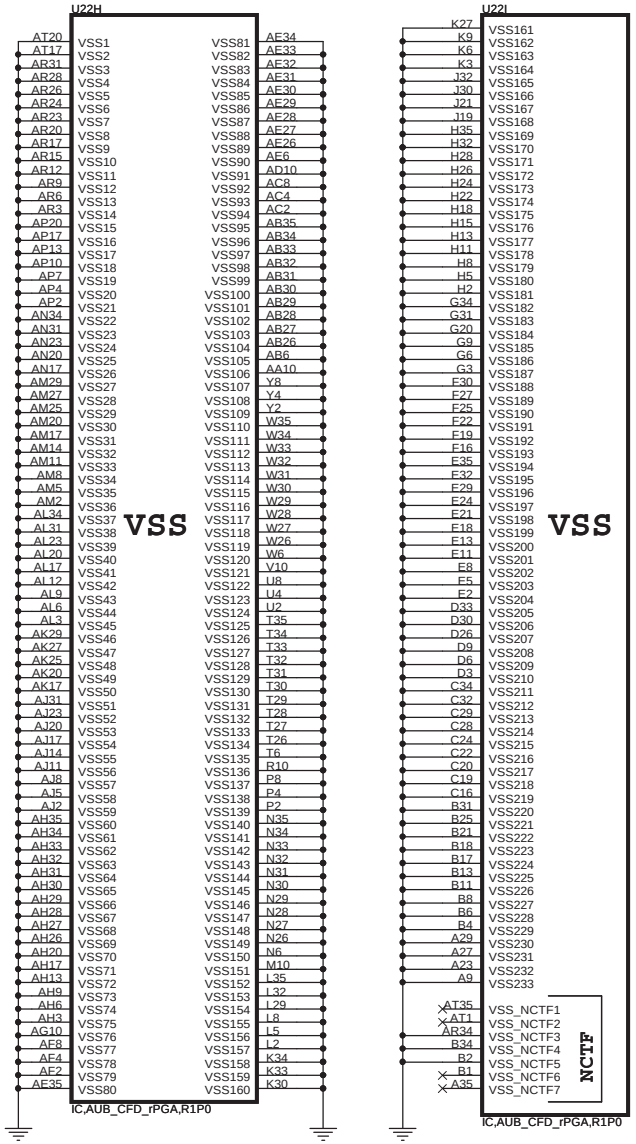
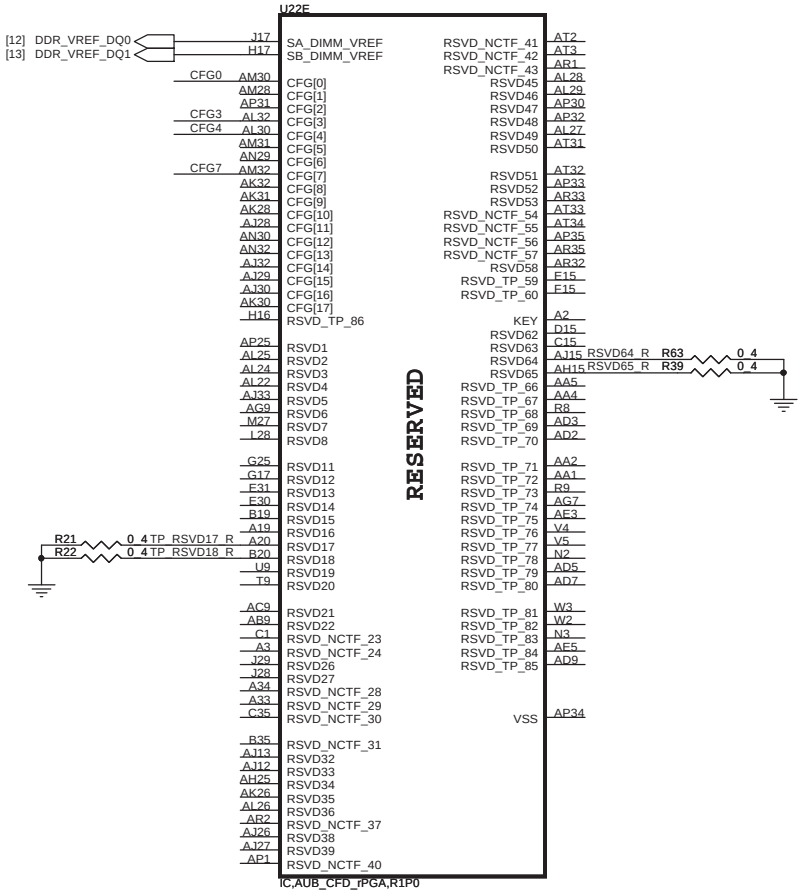
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

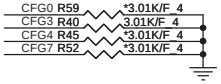


AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1



For discrete only

```
CFG[ 1:0 ] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG
```

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1A

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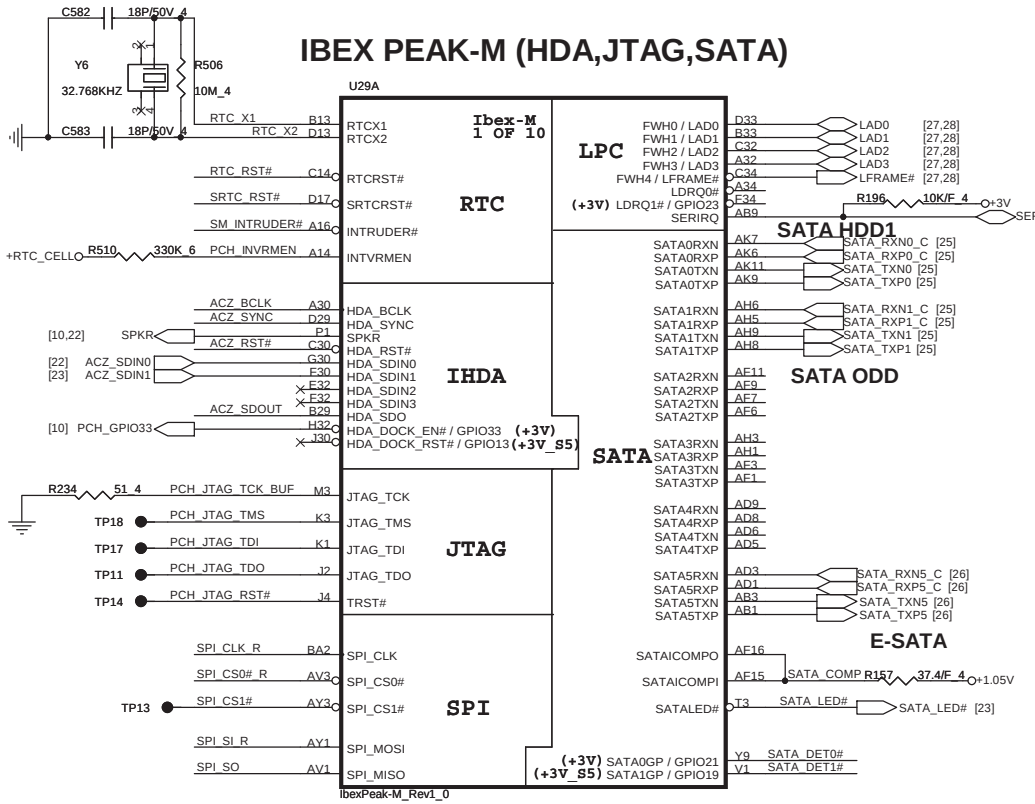
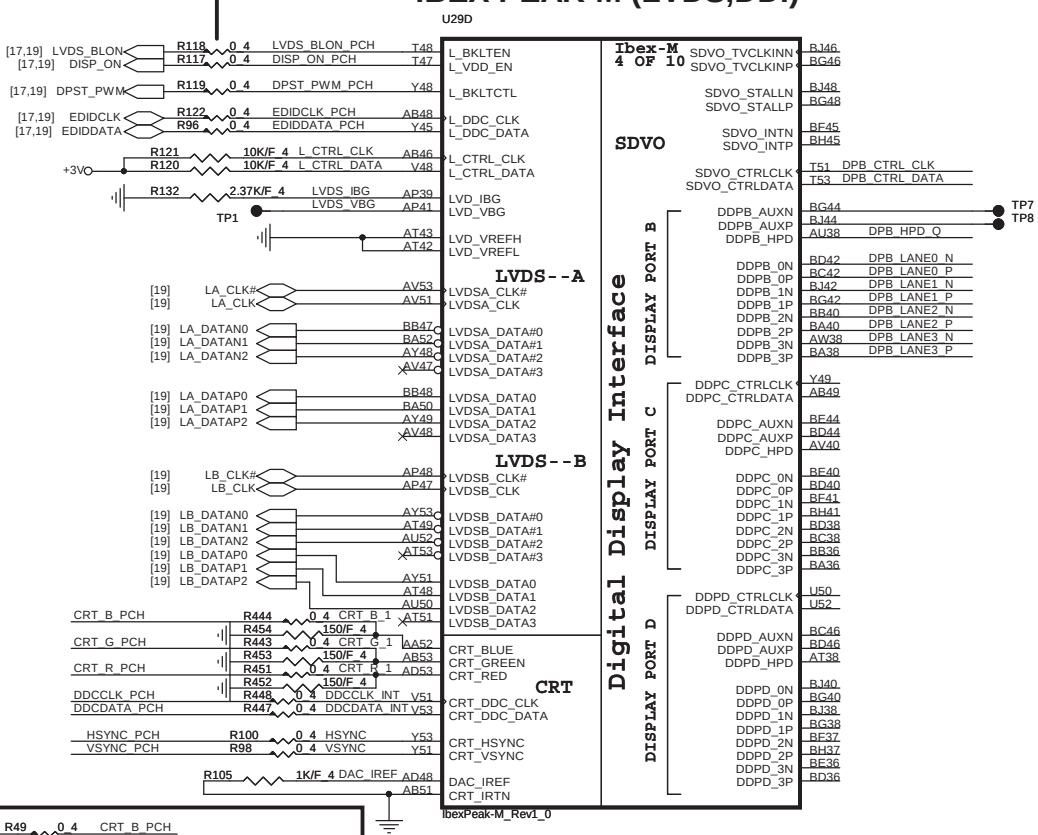
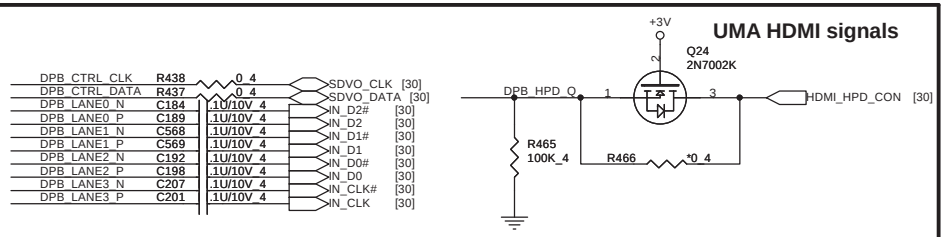
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

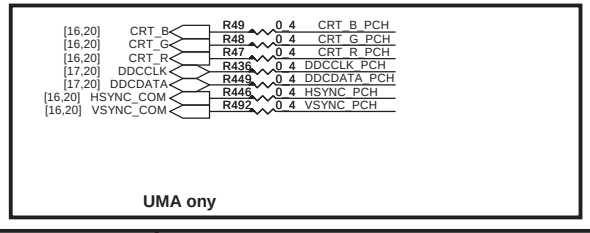
IBEX PEAK-M (HDA,JTAG,SATA)



IBEX PEAK-M (LVDS,DDI)

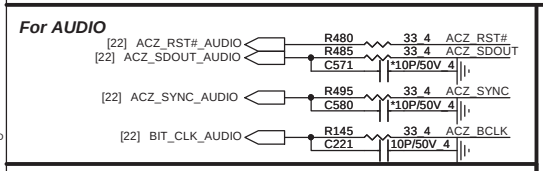


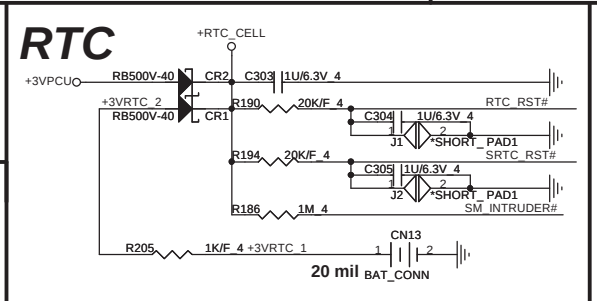


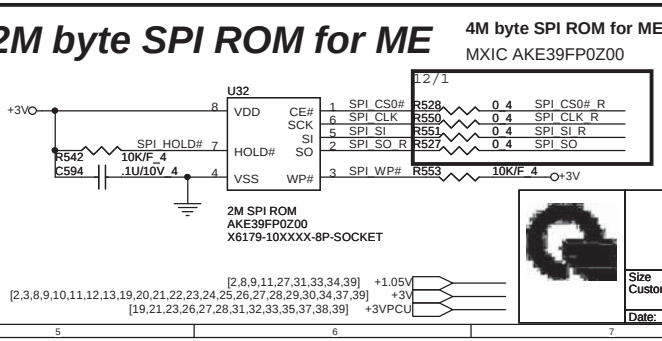


1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

R522 10K/F_4 SATA_LED#
R207 *10K/F_4 SATA_DET0#
R536 *10K/F_4 SATA_DET1#
R232 10K/F_4
R552 10K/F_4







PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A

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IBEX PEAK-M (GND)

U29I

AY7	VSS[159]	VSS[259]	H49
B11	VSS[160]	VSS[260]	H5
B15	VSS[161]	VSS[261]	J24
B19	VSS[162]	VSS[262]	K11
B23	VSS[163]	VSS[263]	K43
B31	VSS[164]	VSS[264]	K47
B35	VSS[165]	VSS[265]	K7
B39	VSS[166]	VSS[266]	L14
B43	VSS[167]	VSS[267]	L18
B47	VSS[168]	VSS[268]	L2
B7	VSS[169]	VSS[269]	L22
BG12	VSS[170]	VSS[270]	L32
BB12	VSS[171]	VSS[271]	L36
BB16	VSS[172]	VSS[272]	L40
BB20	VSS[173]	VSS[273]	L52
BB24	VSS[174]	VSS[274]	M12
BB30	VSS[175]	VSS[275]	M16
BB34	VSS[176]	VSS[276]	M20
BB38	VSS[177]	VSS[277]	N38
BB42	VSS[178]	VSS[278]	M34
BB49	VSS[179]	VSS[279]	M38
BB5	VSS[180]	VSS[280]	M42
BC10	VSS[181]	VSS[281]	M46
BC14	VSS[182]	VSS[282]	M49
BC18	VSS[183]	VSS[283]	M5
BC2	VSS[184]	VSS[284]	M8
BC22	VSS[185]	VSS[285]	N24
BC32	VSS[186]	VSS[286]	P11
BC36	VSS[187]	VSS[287]	AD15
BC40	VSS[188]	VSS[288]	P22
BC44	VSS[189]	VSS[289]	P30
BC52	VSS[190]	VSS[290]	P32
BH9	VSS[191]	VSS[291]	P34
BD48	VSS[192]	VSS[292]	P42
BD49	VSS[193]	VSS[293]	P45
BD5	VSS[194]	VSS[294]	P47
BE12	VSS[195]	VSS[295]	R2
BE16	VSS[196]	VSS[296]	R52
BE20	VSS[197]	VSS[297]	T12
BE24	VSS[198]	VSS[298]	T41
BE30	VSS[199]	VSS[299]	T46
BE34	VSS[200]	VSS[300]	T49
BE38	VSS[201]	VSS[301]	T5
BE42	VSS[202]	VSS[302]	T8
BE46	VSS[203]	VSS[303]	U30
BE48	VSS[204]	VSS[304]	U31
BE50	VSS[205]	VSS[305]	U32
BE6	VSS[206]	VSS[306]	U34
BE8	VSS[207]	VSS[307]	P38
BF3	VSS[208]	VSS[308]	V11
BF49	VSS[209]	VSS[309]	P16
BF51	VSS[210]	VSS[310]	V19
BG18	VSS[211]	VSS[311]	V20
BG24	VSS[212]	VSS[312]	V22
BG4	VSS[213]	VSS[313]	V30
BG50	VSS[214]	VSS[314]	V31
BH11	VSS[215]	VSS[315]	V32
BH15	VSS[216]	VSS[316]	V34
BH19	VSS[217]	VSS[317]	V35
BH23	VSS[218]	VSS[318]	V38
BH31	VSS[219]	VSS[319]	V43
BH35	VSS[220]	VSS[320]	V45
BH39	VSS[221]	VSS[321]	V46
BH43	VSS[222]	VSS[322]	V47
BH47	VSS[223]	VSS[323]	V49
BH7	VSS[224]	VSS[324]	V5
C12	VSS[225]	VSS[325]	V7
C50	VSS[226]	VSS[326]	V8
D51	VSS[227]	VSS[327]	W2
E12	VSS[228]	VSS[328]	W52
E16	VSS[229]	VSS[329]	Y11
E20	VSS[230]	VSS[330]	Y12
E24	VSS[231]	VSS[331]	Y15
E30	VSS[232]	VSS[332]	Y19
E34	VSS[233]	VSS[333]	Y23
E38	VSS[234]	VSS[334]	Y28
E42	VSS[235]	VSS[335]	Y30
E46	VSS[236]	VSS[336]	Y31
E48	VSS[237]	VSS[337]	Y32
E6	VSS[238]	VSS[338]	Y38
E8	VSS[239]	VSS[339]	Y43
F49	VSS[240]	VSS[340]	Y46
F5	VSS[241]	VSS[341]	P49
G10	VSS[242]	VSS[342]	Y5
G14	VSS[243]	VSS[343]	Y6
G18	VSS[244]	VSS[344]	Y8
G2	VSS[245]	VSS[345]	P24
G22	VSS[246]	VSS[346]	T43
G32	VSS[247]	VSS[347]	AD51
G36	VSS[248]	VSS[348]	AT8
G40	VSS[249]	VSS[349]	AD47
G44	VSS[250]	VSS[350]	Y47
G52	VSS[251]	VSS[351]	AT12
AE39	VSS[252]	VSS[352]	AM6
H16	VSS[253]	VSS[353]	AT13
H20	VSS[254]	VSS[354]	AM5
H30	VSS[255]	VSS[355]	AK45
H34	VSS[256]	VSS[356]	AK39
H38	VSS[257]	VSS[366]	AV14
H42	VSS[258]		

IbexPeak-M_Rev1_0

IBEX PEAK-M (PCI-E,SMBUS,CLK)

U29B

Ibex-M 2 OF 10

PCI-E*

[WLAN] [LAN] Robson MiniWLAN WWAN LAN

SMBus

(+3V_S5) SMBALERT# / GPIO11 — B9 SMBALERT# 10K/F_4 R515
SMBCLK — H14 PCLK_SMB 2.2K_4 R164
SMBDATA — C8 PDAT_SMB 2.2K_4 R167
(+3V_S5) SML0ALERT# / GPIO60 — J14 SMBL0ALERT# 10K/F_4 R161
SML0CLK — C6 SMB_CLK_ME0 4.7K_4 R188
SML0DATA — G8 SMB_DATA_ME0 4.7K_4 R191
(+3V_S5) SML1ALERT# / GPIO74 — M14 SML1ALERT# 10K/F_4 R158
(+3V_S5) SML1CLK / GPIO58 — F10 SMB_CLK_ME1 4.7K_4 R171
(+3V_S5) SML1DATA / GPIO75 — G12 SMB_DATA_ME1 4.7K_4 R172

+3VS5

SMB_CLK_ME0 — SMB_CLK_ME0 [24]
SMB_DATA_ME0 — SMB_DATA_ME0 [24]
FOR LAN IC

Controller Link

CL_CLK1 — T13
CL_DATA1 — T11
CL_RST1# — T9

PEG

(+3V_S5) PEG_A_CLKRQ# / GPIO47 — H1 PEG_CLKREQ# — PEG_CLKREQ# [14]
CLKOUT_PEG_A_N — AD43 — CLK_PCIE_VGA# [14]
CLKOUT_PEG_A_P — AD45 — CLK_PCIE_VGA [14]
CLKOUT_DMI_N — AN4 — CLK_PCIE_3GPLL# [3]
CLKOUT_DMI_P — AN2 — CLK_PCIE_3GPLL [3]

From CLK BUFFER

CLKOUT_DP_N / CLKOUT_BCLK1_N — AT1 — DREFSSCLK# [3]
CLKOUT_DP_P / CLKOUT_BCLK1_P — AT3 — DREFSSCLK [3]
CLKIN_DMI_N — AW24 — CLK_BUF_PCIE_3GPLL# [2]
CLKIN_DMI_P — BA24 — CLK_BUF_PCIE_3GPLL [2]
CLKIN_BCLK_N — AP3 — CLK_BUF_BCLK_N [2]
CLKIN_BCLK_P — AP1 — CLK_BUF_BCLK_P [2]
CLKIN_DOT_96N — F18 — CLK_BUF_DREFCLK# [2]
CLKIN_DOT_96P — E18 — CLK_BUF_DREFCLK [2]
CLKIN_SATA_N / CKSSCD_N — AH13 — CLK_BUF_DREFSSCLK# [2]
CLKIN_SATA_P / CKSSCD_P — AH12 — CLK_BUF_DREFSSCLK [2]
REFCLK14IN — P41 — CLK_ICH_14M [2]
CLKIN_PCILOOPBACK — J42 CLK_PCI_FB — CLK_PCI_FB [9]
XTAL25_IN — AH51 PCH_XT25MHZ_IN
XTAL25_OUT — AH53 PCH_XT2MHZ_OUT
XCLK_RCOMP — AF38 XCLK_RCOMP — R126 90.9/F_4 — +1.05V

Clock Flex

(+3V) CLKOUTFLEX0 / GPIO64 — T45 CLK_FLEX0 — T11
(+3V) CLKOUTFLEX1 / GPIO65 — P43 CLK_FLEX1 — T12
(+3V) CLKOUTFLEX2 / GPIO66 — T42 CLK_FLEX2 — T13
(+3V) CLKOUTFLEX3 / GPIO67 — N50 CLK_FLEX3 — R135 22_4 — CLK_48M_CR [21]

1203 Intel EDS1.0 spec change to no support 27and 24MHZ

[28] PCIE_RXN0 — PCIE_RXN0 BG30
[28] PCIE_RXP0 — PCIE_RXP0 BJ30
[28] PCIE_TXN0 — C575 .1U/10V_4 — PCIE_TXN0_C BF29
[28] PCIE_TXP0 — C578 .1U/10V_4 — PCIE_TXP0_C BH29

[24] PCIE_RXN1_LAN — AW30
[24] PCIE_RXP1_LAN — BA30
[24] PCIE_TXN1_LAN — C247 .1U/10V_4 — PCIE_TXN1_C BC30
[24] PCIE_TXP1_LAN — C234 .1U/10V_4 — PCIE_TXP1_C BD30

AU30 AT30 AU32 AV32

[28] PCIE_RXN4 — PCIE_RXN4 BA32
[28] PCIE_RXP4 — PCIE_RXP4 BB32
[28] PCIE_TXN4 — C218 .1U/10V_4 — PCIE_TXN4_C BD32
[28] PCIE_TXP4 — C224 .1U/10V_4 — PCIE_TXP4_C BE32

BF33 BH33 BG32 BJ32

BA34 AW34 BC34 BD34

AT34 AU34 AU36 AV36

BG34 BJ34 BG36 BJ36

AK48 AK47

PCIE_CLK_REQ0# — P9
[28] CLK_PCIE_WLAN#R — AM43
[28] CLK_PCIE_WLAN — AM45
[28] PCIE_CLK_REQ1# — R213 0_4 — CLK1_OE# — U4
[28] CLK_PCIE_WWAN#R — AM47
[28] CLK_PCIE_WWAN — AM48
[28] PCIE_CLK_REQ2# — R523 0_4 — CLK2_OE# — N4
[24] CLK_PCIE_LAN#R — AH42
[24] CLK_PCIE_LAN — AH41
[24] PCIE_CLK_REQ3# — R517 0_4 — PCIE_CLK_REQ3#_R — A8
AM51 AM53
PCIE_CLK_REQ4#_R — M9
AJ50 AJ52
PCIE_CLK_REQ5# — H6
AK53 AK51
PCIE_CLK_REQB#_R — P13

CLKOUT_PCIE0N CLKOUT_PCIE0P
PCIECLKRQ0# / GPIO73 (+3V_S5)
CLKOUT_PCIE1N CLKOUT_PCIE1P
PCIECLKRQ1# / GPIO18 (+3V)
CLKOUT_PCIE2N CLKOUT_PCIE2P
PCIECLKRQ2# / GPIO20 (+3V)
CLKOUT_PCIE3N CLKOUT_PCIE3P
PCIECLKRQ3# / GPIO25 (+3V_S5)
CLKOUT_PCIE4N CLKOUT_PCIE4P
PCIECLKRQ4# / GPIO26 (+3V_S5)
CLKOUT_PCIE5N CLKOUT_PCIE5P
PCIECLKRQ5# / GPIO44 (+3V_S5)
CLKOUT_PEG_B_N CLKOUT_PEG_B_P
PEG_B_CLKRQ# / GPIO56 (+3V_S5)

CLK1_OE# — R214 10K/F_4
CLK2_OE# — R524 10K/F_4
+3V

+3VS5
PCIE_CLK_REQ0# — R178 10K/F_4
PCIE_CLK_REQ3#_R — R518 10K/F_4
PCIE_CLK_REQ4#_R — R180 10K/F_4
PCIE_CLK_REQB#_R — R155 10K/F_4
PCIE_CLK_REQ5# — R192 10K/F_4
PEG_CLKREQ# — R526 *10K/F_4

SMB_CLK_ME1 — Q13 2N7002E — MBCLK2 [17,27]
R269 2.2K_4
+3V
R270 2.2K_4
SMB_DATA_ME1 — Q14 2N7002E — MBDATA2 [17,27]

PDAT_SMB — Q10 2N7002E — CGDAT_SMB [2,12,13]
R211 10K/F_4
+3V
R210 10K/F_4
PCLK_SMB — Q9 2N7002E — CGCLK_SMB [2,12,13]

[9] PLT_RST-R# — PLT_RST-R#
U13 *MC74VHC1G08DFT2G
C330 *.1U/10V_4
PLTRST# [3,24,27,28,29]
R245 100K/F_4
R247 0_4
R248 *100K/F_4

R481 1M_4
Y7
PCH_XT2MHZ_OUT — PCH_XT25MHZ_IN
C786 18P/50V_4
C787 18P/50V_4
25MHZ

[3,9,10,11,14,37] +3VS5
[2,7,9,11,27,31,33,34,39] +1.05V
[2,3,7,9,10,11,12,13,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 2/5 (PCIE, SMBUS,CK)	1A

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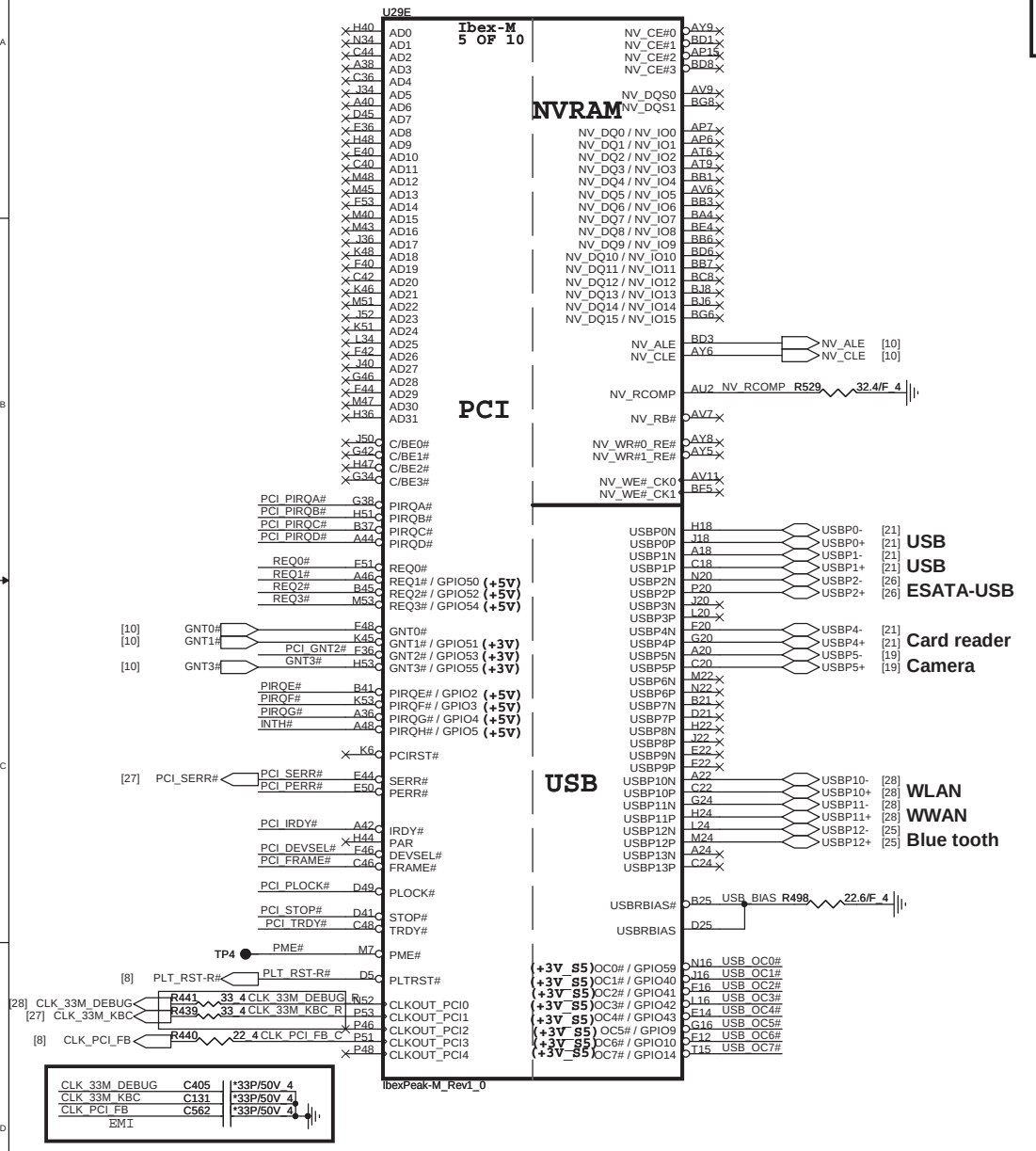
IBEX PEAK-M (PCI,USB,NVRAM)



CLK_33M_DEBUG C405 *33P/50V_4
CLK_33M_KBC C131 *33P/50V_4
CLK_PCI_FB C562 *33P/50V_4
EMI

For Switchable only

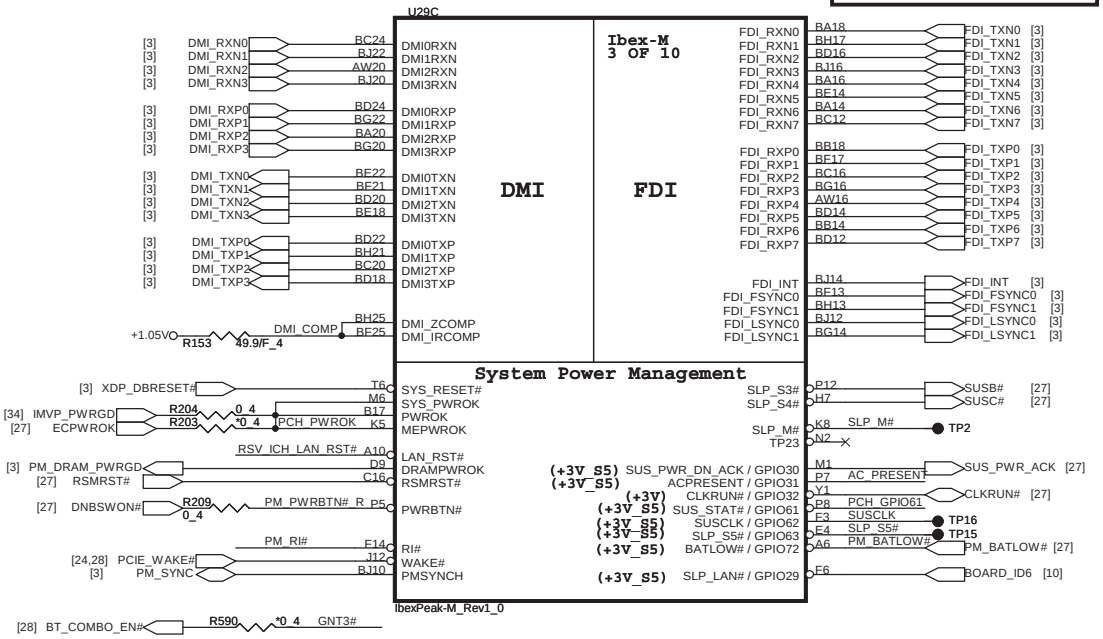
[27,29] DGPU_HOLD_RST# R587 *0_4 SATA2GP SATA2GP [10]
[27] DGPU_PWR_EN# R386 *0_4 REQ1#
[27,30] DGPU_SELECT# R387 *0_4 REQ2#
[27] EDID_SELECT# R585 *0_4 REQ3#
[27,29] DGPU_PWROK R588 *0_4 SATA3GP SATA3GP [10]

PCH_GPIO61 R586 10K/F_4 +3VS5

Discrete Only

FDI_INT R505 *1K/F_4
FDI_FSYNC0 R514 *1K/F_4
FDI_FSYNC1 R509 *1K/F_4
FDI_LSYNC0 R511 *1K/F_4
FDI_LSYNC1 R508 *1K/F_4

IBEX PEAK-M (DMI,FDI,GPIO)



[3] DMI_RXN0 BC24
[3] DMI_RXN1 BJ22
[3] DMI_RXN2 AW20
[3] DMI_RXN3 BJ20
[3] DMI_RXP0 BD24
[3] DMI_RXP1 BG22
[3] DMI_RXP2 BA20
[3] DMI_RXP3 BG20
[3] DMI_TXN0 BF22
[3] DMI_TXN1 BF21
[3] DMI_TXN2 BD20
[3] DMI_TXN3 BE18
[3] DMI_TXP0 BD22
[3] DMI_TXP1 BH21
[3] DMI_TXP2 BC20
[3] DMI_TXP3 BD18
+1.05VO R153 49.9/F_4 DMI_COMP BH25 BF25

FDI_RXN0 BA18 FDI_TXN0 [3]
FDI_RXN1 BH17 FDI_TXN1 [3]
FDI_RXN2 BD16 FDI_TXN2 [3]
FDI_RXN3 BJ16 FDI_TXN3 [3]
FDI_RXN4 BA16 FDI_TXN4 [3]
FDI_RXN5 BE14 FDI_TXN5 [3]
FDI_RXN6 BA14 FDI_TXN6 [3]
FDI_RXN7 BC12 FDI_TXN7 [3]
FDI_RXP0 BB18 FDI_TXP0 [3]
FDI_RXP1 BF17 FDI_TXP1 [3]
FDI_RXP2 BC16 FDI_TXP2 [3]
FDI_RXP3 BG16 FDI_TXP3 [3]
FDI_RXP4 AW16 FDI_TXP4 [3]
FDI_RXP5 BD14 FDI_TXP5 [3]
FDI_RXP6 BB14 FDI_TXP6 [3]
FDI_RXP7 BD12 FDI_TXP7 [3]
FDI_INT BJ14 FDI_INT [3]
FDI_FSYNC0 BE13 FDI_FSYNC0 [3]
FDI_FSYNC1 BH13 FDI_FSYNC1 [3]
FDI_LSYNC0 BJ12 FDI_LSYNC0 [3]
FDI_LSYNC1 BG14 FDI_LSYNC1 [3]

[3] XDP_DBRESET# T6
[34] IMVP_PWRGD R204 0_4 M6
[27] ECPWROK R203 *0_4 PCH_PWROK B17
RSV_ICH_LAN_RST# A10
[3] PM_DRAM_PWRGD D9
[27] RSMRST# C16
[27] DNBSWON# R209 0_4 PM_PWRBTN#_R P5
PM_RI# F14
[24,28] PCIE_WAKE# J12
[3] PM_SYNC BJ10
[28] BT_COMBO_EN# R590 *0_4 GNT3#

SLP_S3# P12 SUSB# [27]
SLP_S4# H7 SUSC# [27]
SLP_M# K8 SLP_M# TP2
TP23 N2
M1 SUS_PWR_ACK [27]
AC_PRESENT P7
Y1
CLKRUN# [27] P8 PCH_GPIO61
TP16 F3 SUSCLK
TP15 E4 SLP_S5#
PM_BATLOW# A6 PM_BATLOW# [27]
F6 BOARD_ID6 [10]

BT_COMBO_EN# R139 *1K/F_4

RP34 10P8R-8.2K
PCI_IRDY# PCI_STOP# PCI_PIRQA# PCI_PIRQC# PCI_PIRQD# PCI_SERR# REQ1# PCI_FRAME# +3V

RP27 10P8R-8.2K
USB_OC4# USB_OC5# USB_OC6# USB_OC7# USB_OC0# USB_OC1# USB_OC2# USB_OC3# +3VS5

RP33 10P8R-8.2K
PCI_DEVSEL# PCI_PLOCK# PCI_PERR# REQ3# PCI_TRDY# INTH# REQ0# PCI_PIRQB# +3V

REQ2# R116 8.25K/F_4
PIRQE# R115 8.25K/F_4
PIRQF# R471 8.25K/F_4
PIRQG# R131 8.25K/F_4
11/17
CLKRUN# R532 8.25K/F_4
XDP_DBRESET# R200 1K/F_4
PM_RI# R162 10K/F_4
PM_BATLOW# R519 10K/F_4
PCIE_WAKE# R170 1K/F_4
[27] AC_PRESENT SUS_PWR_ACK R525 10K/F_4
AC_PRESENT R177 10K/F_4
11/17
RSMRST# R503 10K/F_4
RSV_ICH_LAN_RST# R513 10K/F_4
PCH_PWROK R501 10K/F_4

[2,7,8,11,27,31,33,34,39] +1.05V
[2,3,7,8,10,11,12,13,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[3,8,10,11,14,37] +3VS5

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/5(PCI,ONFI,USB,DMI)	1A

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IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

IBEX PEAK-M (GND)

11/17

GPIO27 left NC for internal VR.

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6"/ 14"			0=QL4/TW9 1=QL2/SW9				
MDC				0=YES 1=NO			

Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

BOARD ID SETTING

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP	1-X High = Strong (Default)

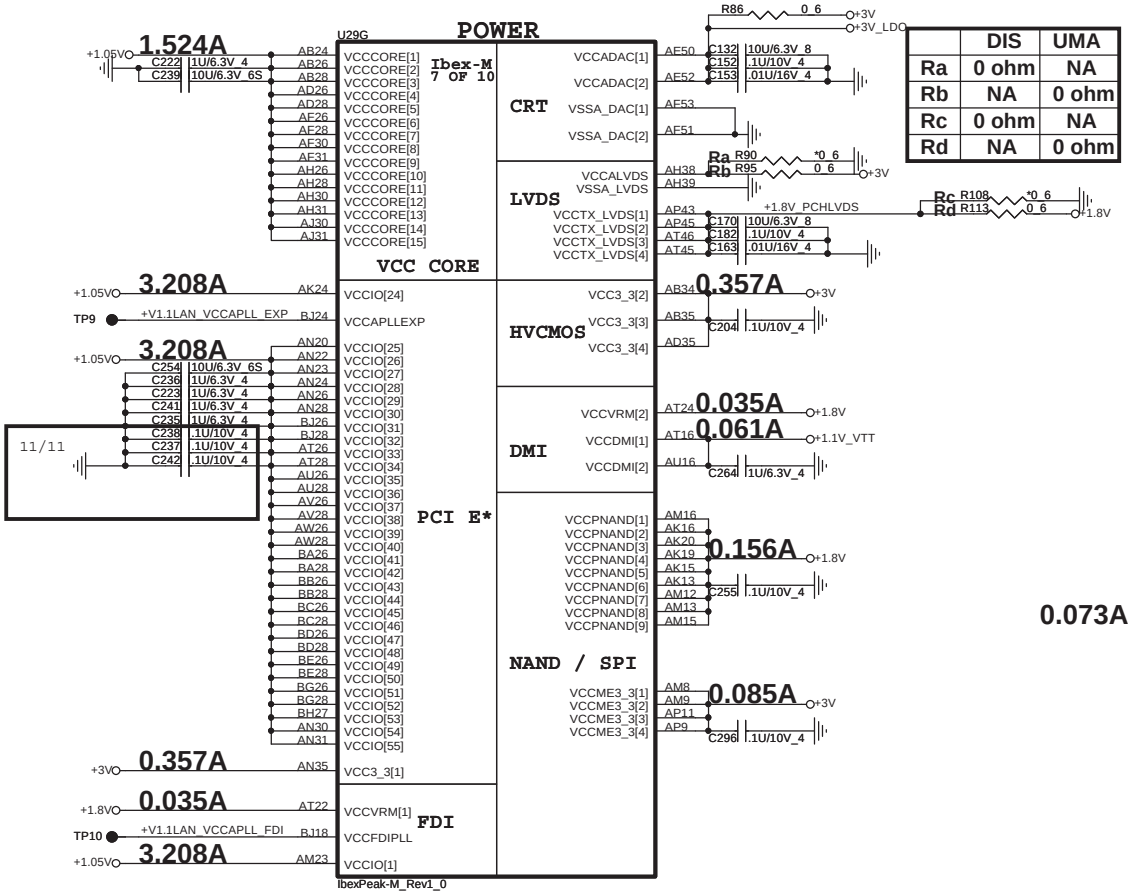
Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

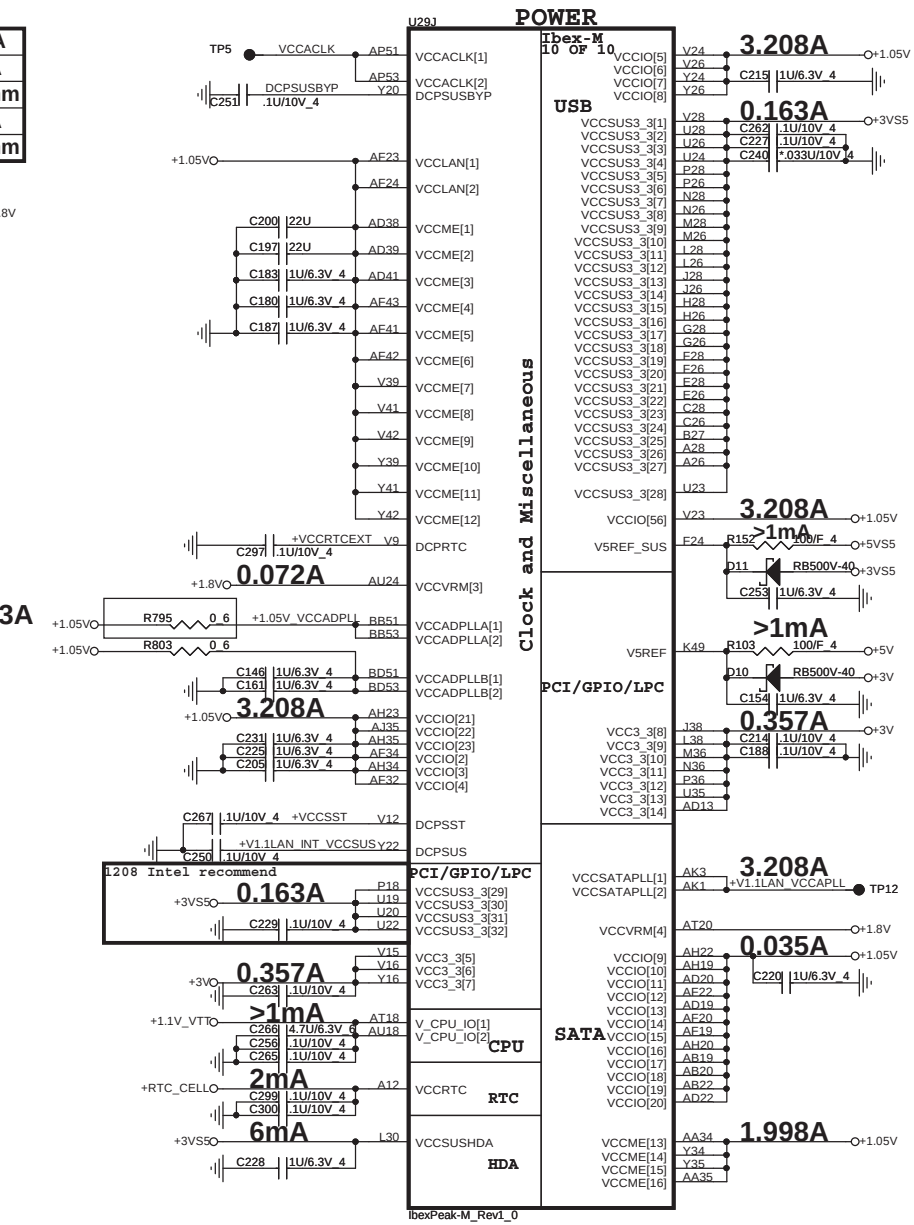
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

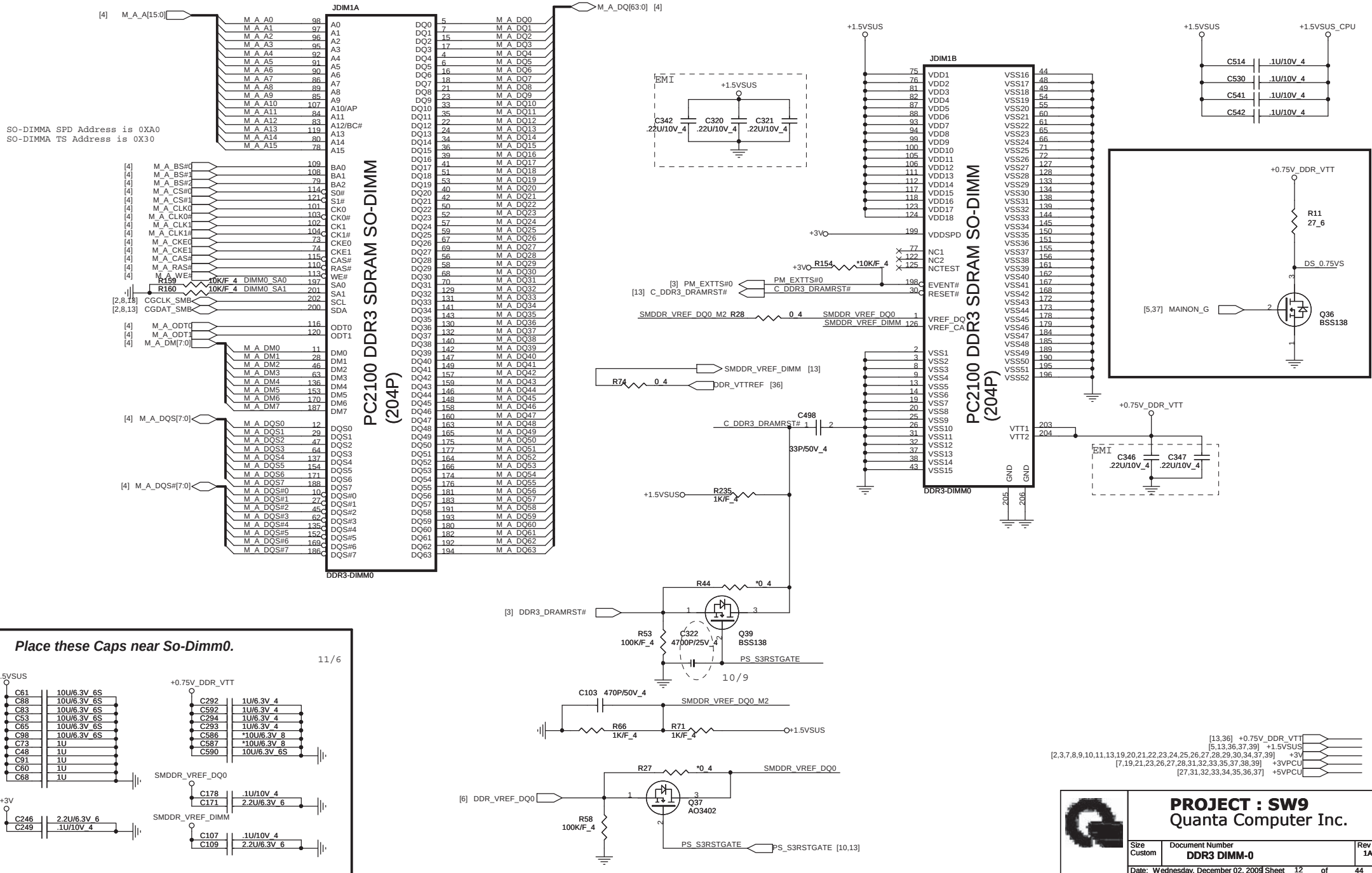
No Reboot Strap

Project	PROJECT : SW9 Quanta Computer Inc.
Size / Custom	Document Number: PCH 4/5 (GPIO & Strap)
Rev	1A
Date: Wednesday, December 02, 2009	Sheet 10of 44



	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm





Place these Caps near So-Dimm0.

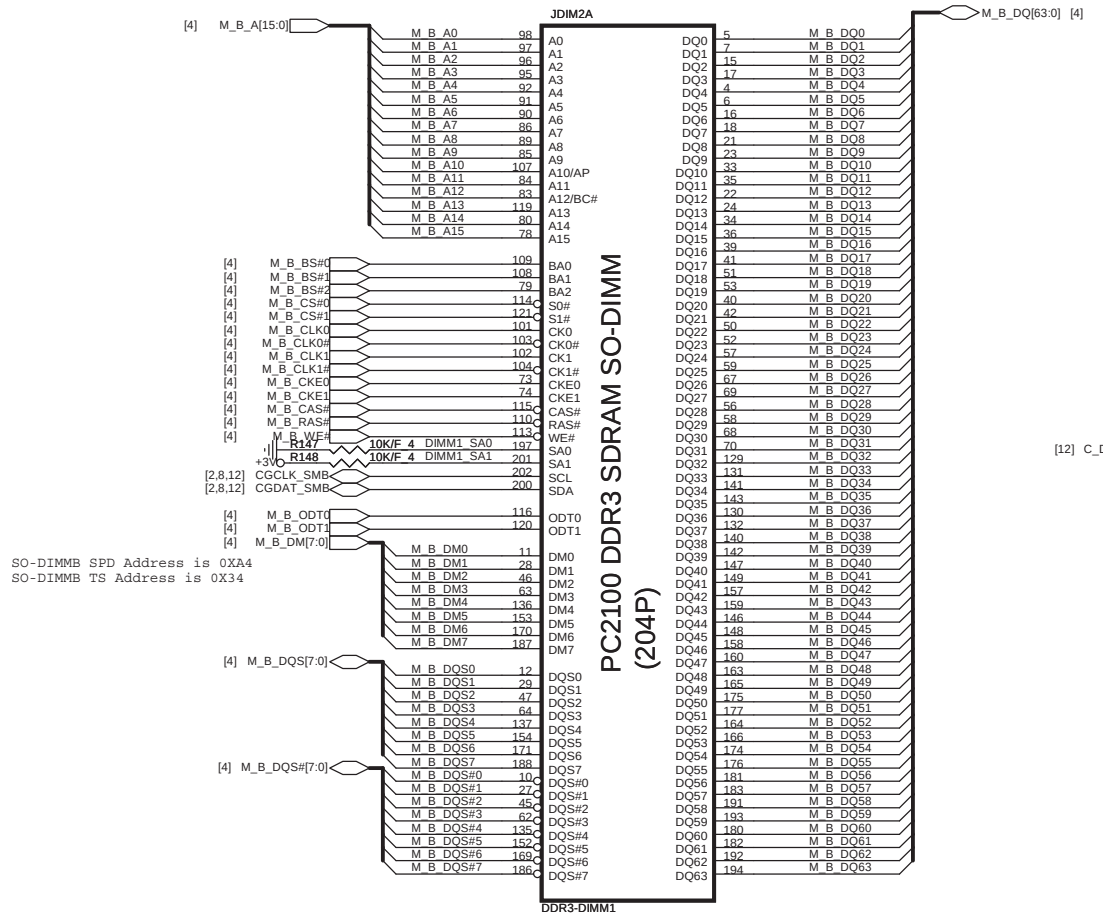
11/6

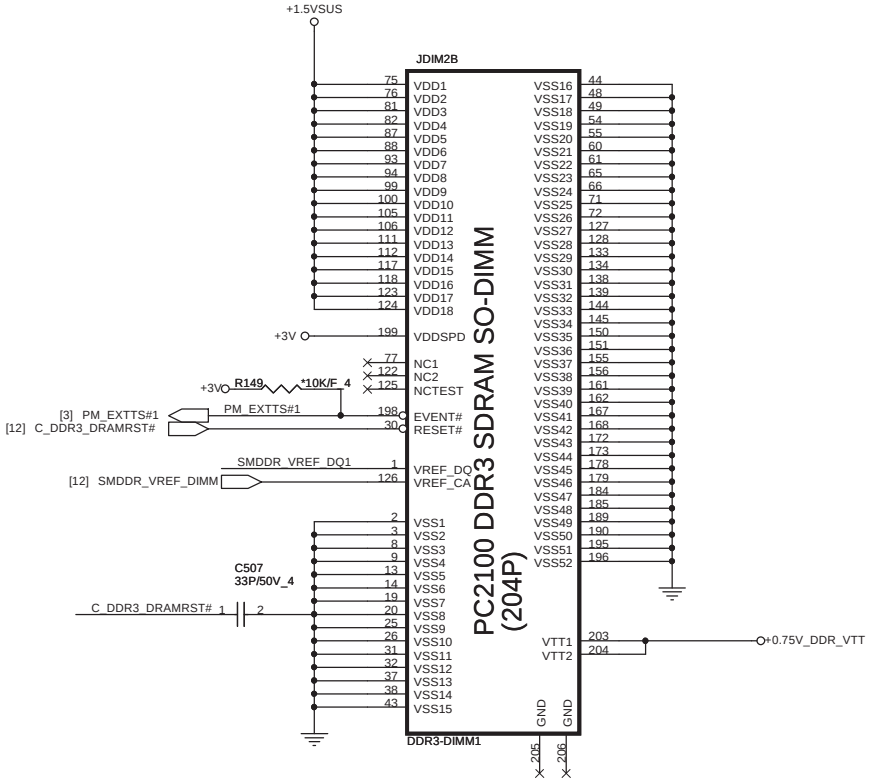
[13,36] +0.75V_DDR_VTT
[5,13,36,37,39] +1.5VSUS
[2,3,7,8,9,10,11,13,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[7,19,21,23,26,27,28,31,32,33,35,37,38,39] +3VPCU
[27,31,32,33,34,35,36,37] +5VPCU

PROJECT : SW9
Quanta Computer Inc.

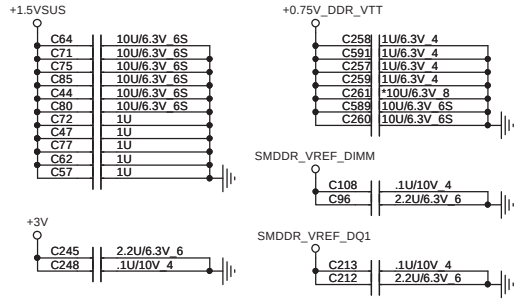
Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A

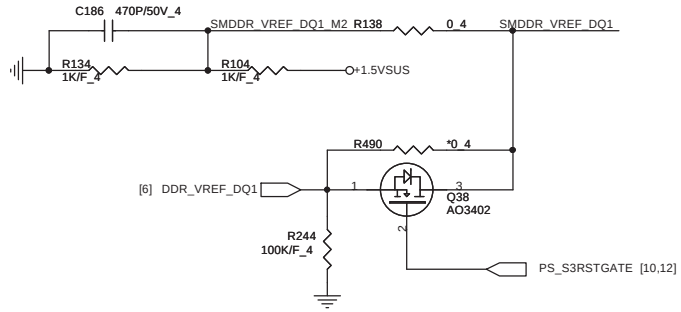
Date: Wednesday, December 02, 2009 Sheet 12 of 44





Place these Caps near So-Dimm1.





[12,36] +0.75V_DDR_VTT
[5,12,36,37,39] +1.5VSUS
[2,3,7,8,9,10,11,12,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[7,19,21,23,26,27,28,31,32,33,35,37,38,39] +3VPCU
[27,31,32,33,34,35,36,37] +5VPCU

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A

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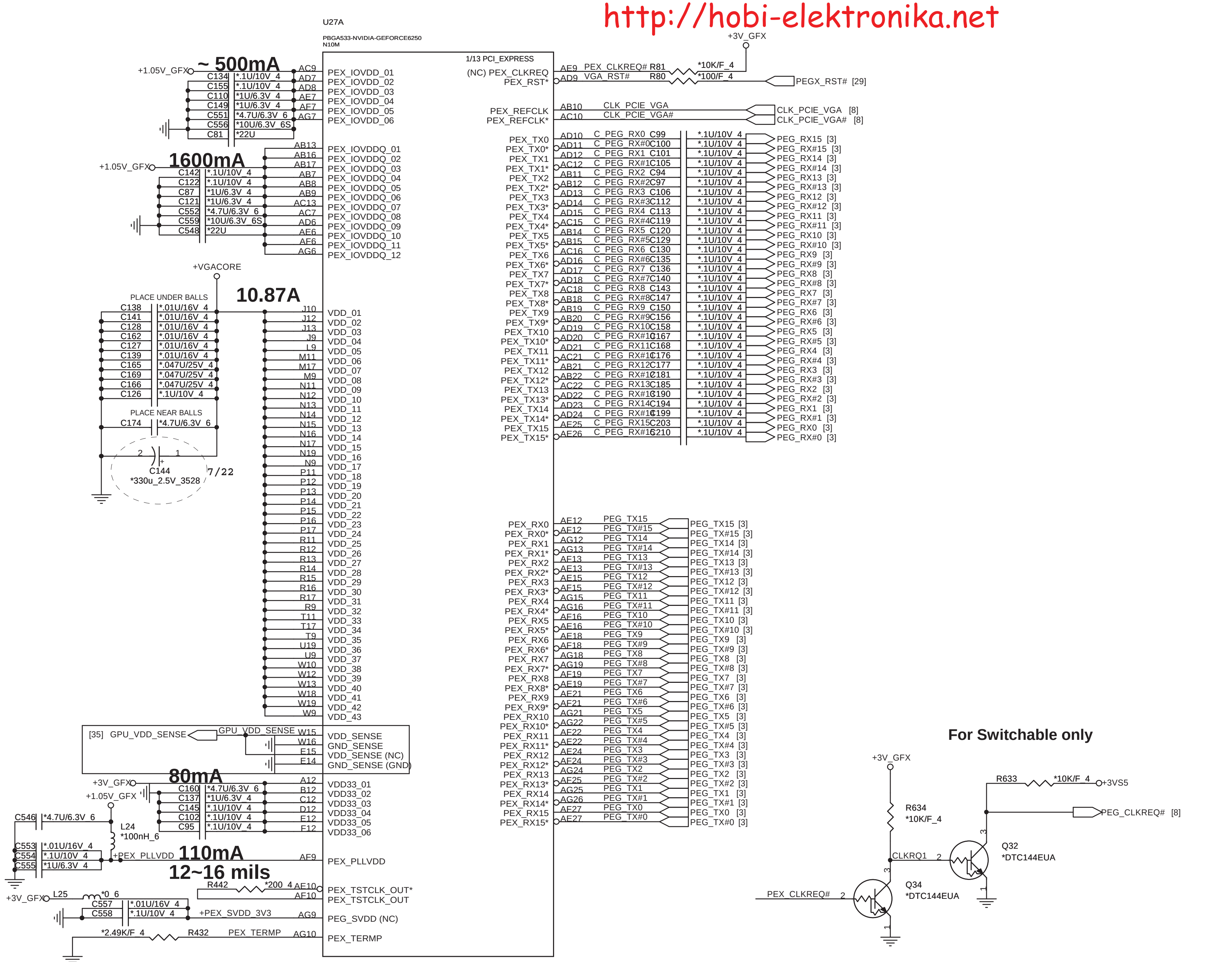
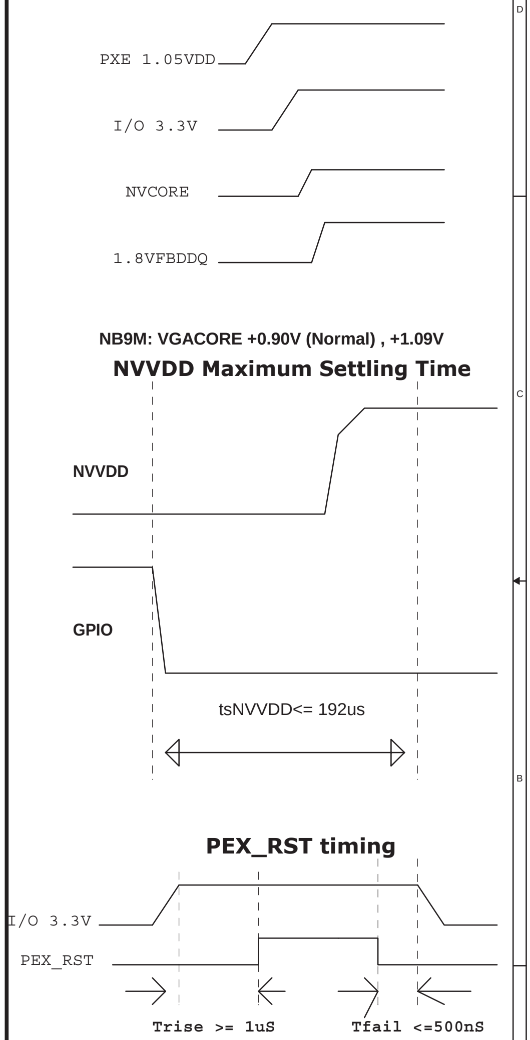


power up sequence



VGA Thermal Circuit ==> Del 6/16

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (PCIE I/F) 1/5	1A

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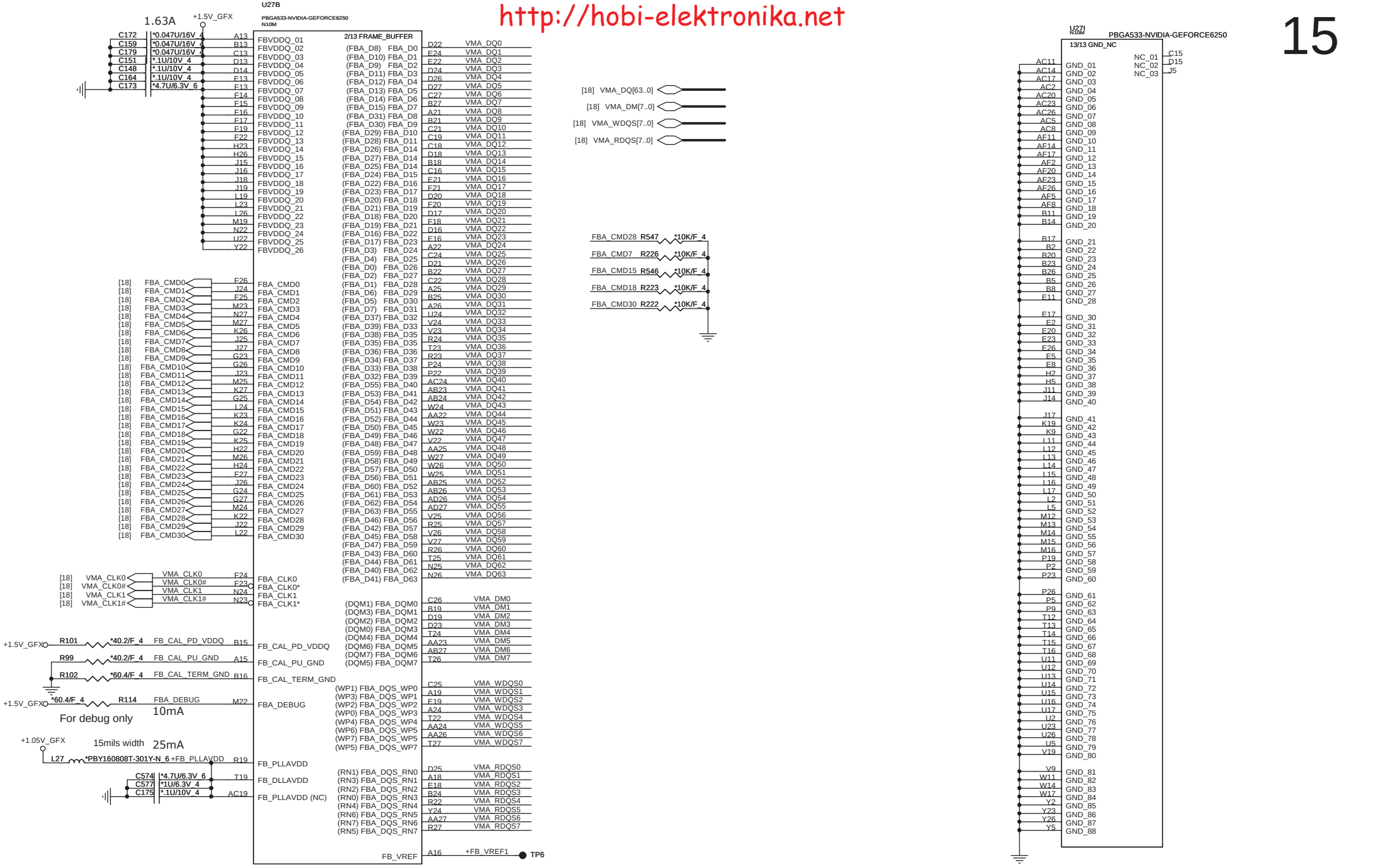

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (MEMORY I/F) 2/5	1A

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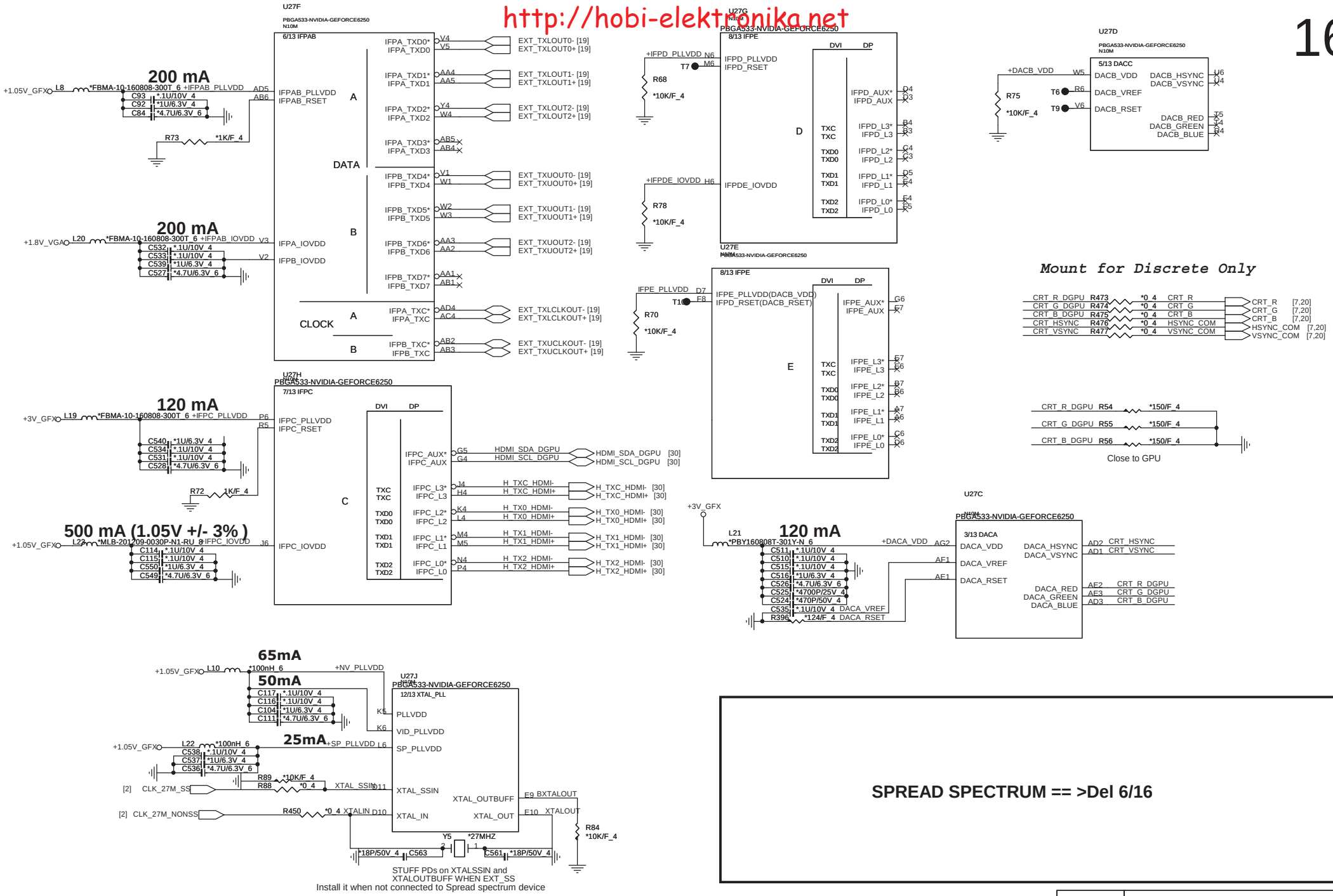
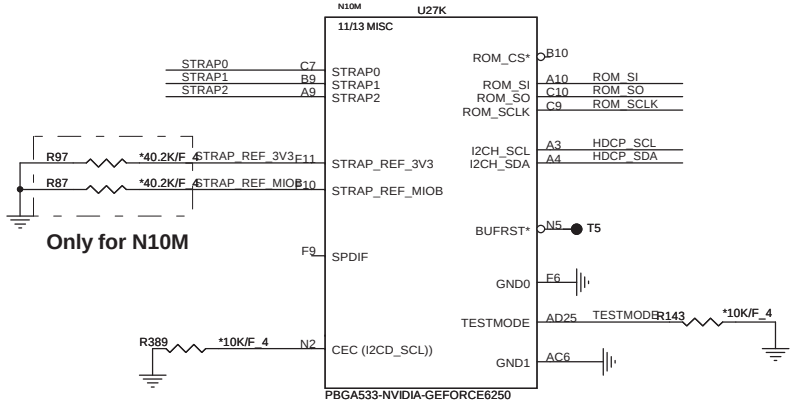
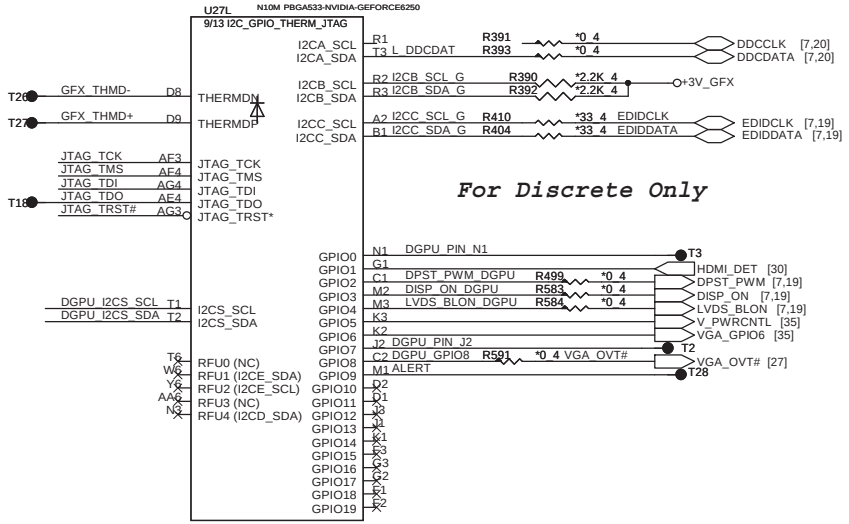
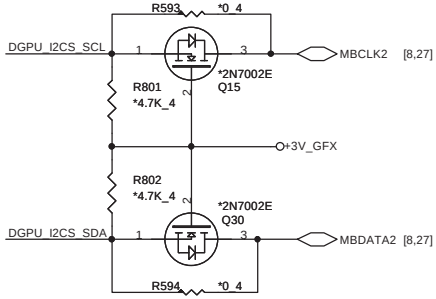


PROJECT : SW9 Quanta Computer Inc.		
Size: Custom	Document Number: N10M-GE (DISPLAY) 3/5	Rev: 1A
Date: Wednesday, December 02, 2009	Sheet 16 of 44	







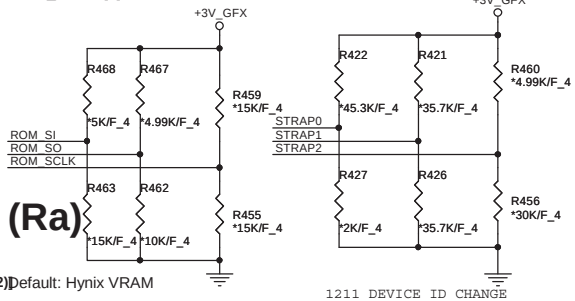
Mount Q15 , Q30 , R801 , R802
For Switchable only

CHIP	PCI_DEVID:	STRAP2
N11P-GE1	0x0A29	1001 PU 10K
N11M-GE1	0x0A75	1010 PD 30K

Logical Strap Bit Mapping		
	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SEE Datasheet for details on N10P Straps!

PCI_DEVID[4]/SUBVENDOR



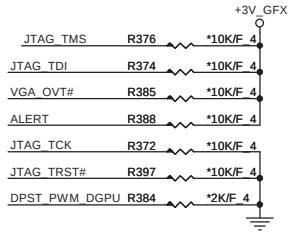
4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)] Default: Hynix VRAM
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

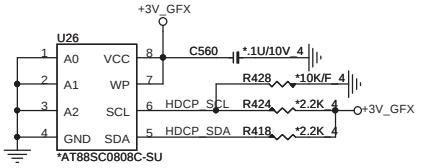
VRAM Configuration Table

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
	0000		Reserved		
AKD58GGT^01	0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
AKD5LZGTW00	0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
AKD5LGGT502	0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
	0101		Reserved		
	0110				
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)



HDCP ROM



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

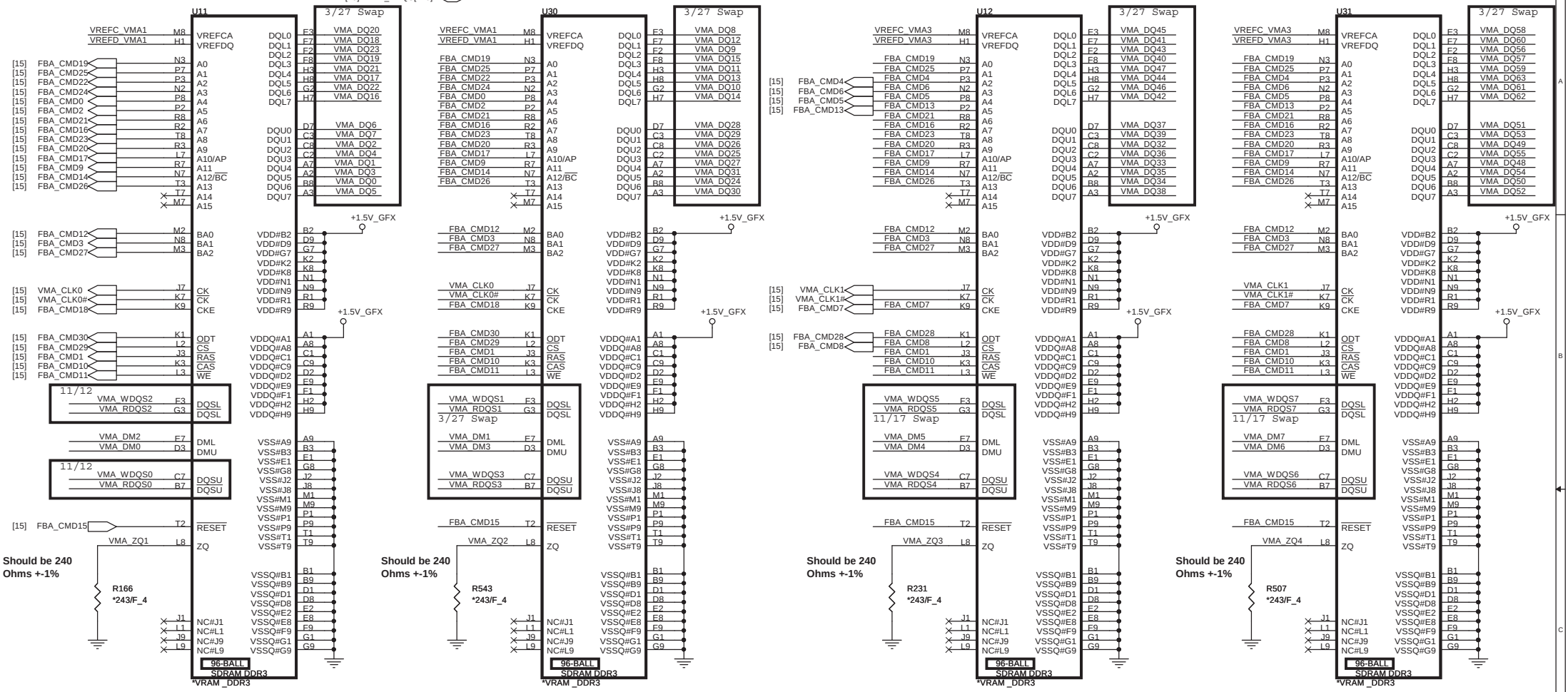
PROJECT : SW9
Quanta Computer Inc.

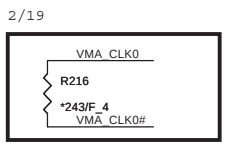
Size	Document Number	Rev
Custom	N10M-GE (GPIO&STRAPS) 4/5	1A

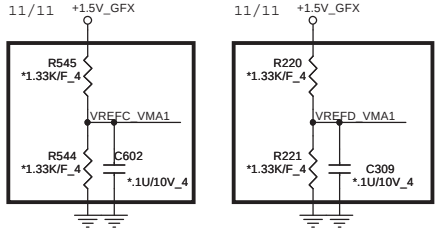
Date: Wednesday, December 02, 2009 Sheet 17 of 44

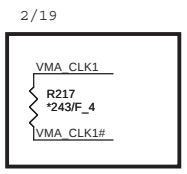
CHANNEL A: 256MB/512MB DDR3

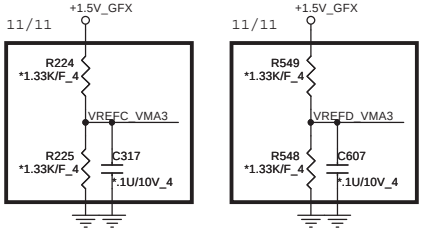
[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

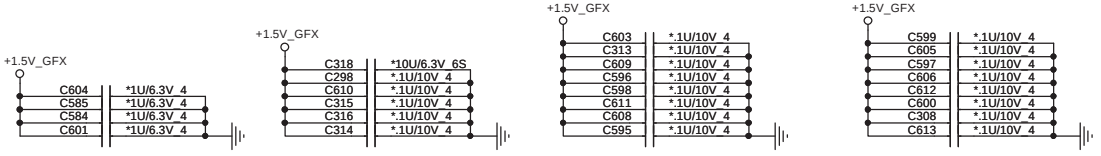












1211 for Nvidia request add transition cap

[15,29,39] +1.5V_GFX

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE VRAM-1(DDR3 BGA96	1A

Date: Wednesday, December 02, 2009 Sheet 18 of 44

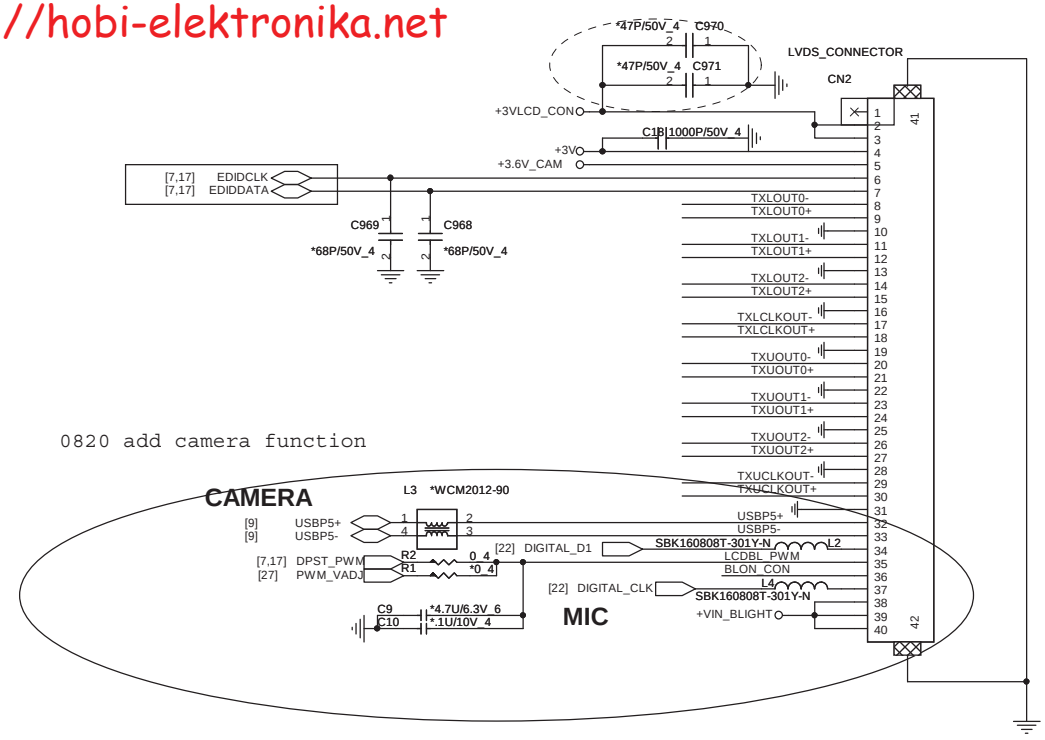
1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

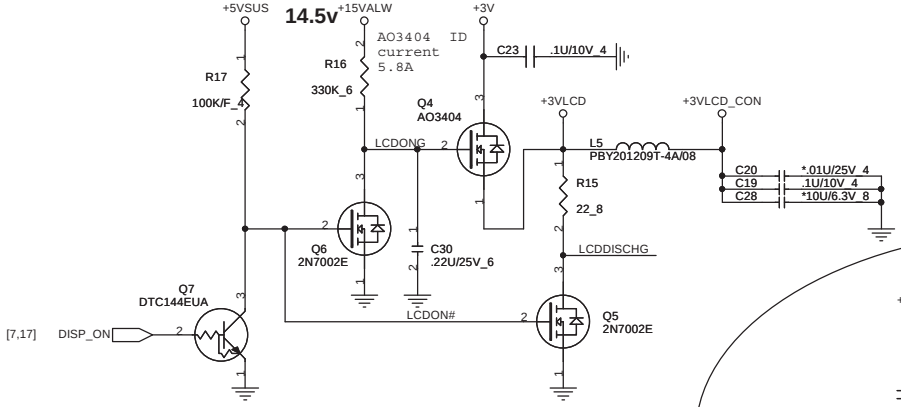
OPTION SIGNAL FROM NB FOR UMA VGA

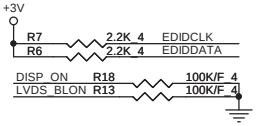
[7] LA_CLK	RP8	4P2R-S-0	TXLCLKOUT+		
[7] LA_CLK#			TXLCLKOUT-		
[7] LA_DATAP0	RP6	4P2R-S-0	TXLOUT0+		
[7] LA_DATAN0			TXLOUT0-		
[7] LA_DATAP1	RP5	4P2R-S-0	TXLOUT1+		
[7] LA_DATAN1			TXLOUT1-		
[7] LA_DATAP2	RP7	4P2R-S-0	TXLOUT2+		
[7] LA_DATAN2			TXLOUT2-		
[7] LB_CLK#	RP1	4P2R-S-0	TXUCLKOUT-		
[7] LB_CLK			TXUCLKOUT+		
[7] LB_DATAP0	RP4	4P2R-S-0	TXUOUT0+		
[7] LB_DATAN0			TXUOUT0-		
[7] LB_DATAP1	RP2	4P2R-S-0	TXUOUT1+		
[7] LB_DATAN1			TXUOUT1-		
[7] LB_DATAP2	RP3	4P2R-S-0	TXUOUT2+		
[7] LB_DATAN2			TXUOUT2-		

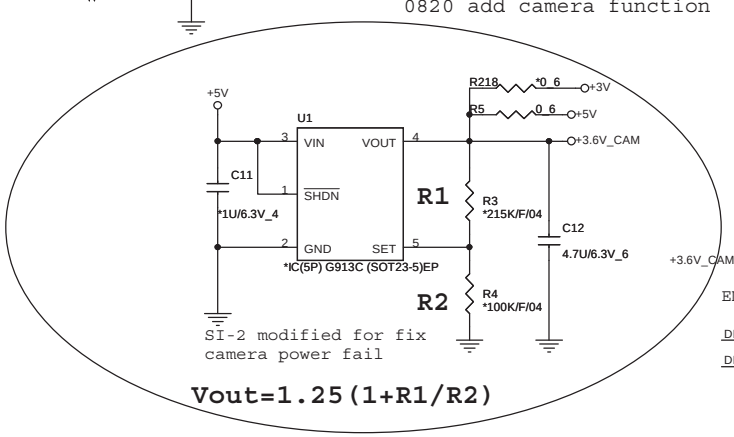
OPTION SIGNAL FROM Nvidia to VGA

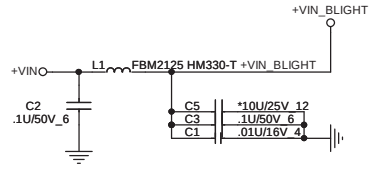
[16] EXT_TXLCLKOUT-	*4P2R-S-0	RP16	TXLCLKOUT-
[16] EXT_TXLCLKOUT+			TXLCLKOUT+
[16] EXT_TXLOUT0+	*4P2R-S-0	RP14	TXLOUT0+
[16] EXT_TXLOUT0-			TXLOUT0-
[16] EXT_TXLOUT1-	*4P2R-S-0	RP13	TXLOUT1-
[16] EXT_TXLOUT1+			TXLOUT1+
[16] EXT_TXLOUT2-	*4P2R-S-0	RP15	TXLOUT2-
[16] EXT_TXLOUT2+			TXLOUT2+
[16] EXT_TXUCLKOUT-	*4P2R-S-0	RP9	TXUCLKOUT-
[16] EXT_TXUCLKOUT+			TXUCLKOUT+
[16] EXT_TXUOUT0-	*4P2R-S-0	RP12	TXUOUT0-
[16] EXT_TXUOUT0+			TXUOUT0+
[16] EXT_TXUOUT1+	*4P2R-S-0	RP10	TXUOUT1+
[16] EXT_TXUOUT1-			TXUOUT1-
[16] EXT_TXUOUT2-	*4P2R-S-0	RP11	TXUOUT2-
[16] EXT_TXUOUT2+			TXUOUT2+

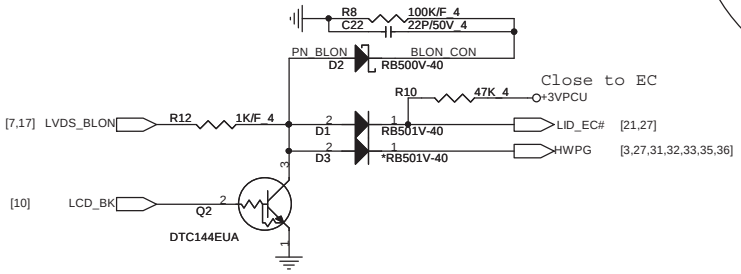


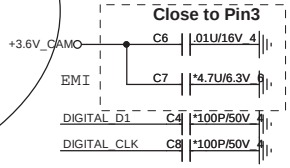












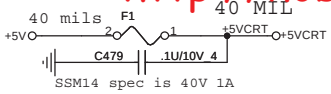
[11,20,22,23,25,26,28,30,37] +5V
[2,3,7,8,9,10,11,12,13,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[7,21,23,26,27,28,31,32,33,35,37,38,39] +3VPCU
[21,25,26,37] +5VSUS
[32,37] +15VALW
[2,31,32,33,34,35,36,37,38,39] +VIN

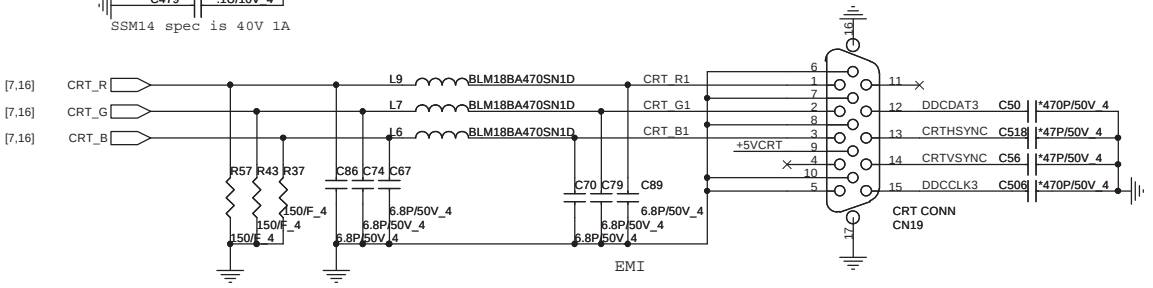
PROJECT : SW9
Quanta Computer Inc.

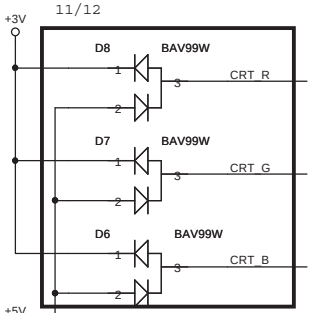
Size	Document Number	Rev
Custom	LCD CONN	1A

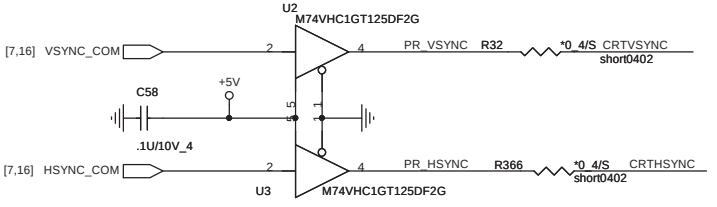
Date: Thursday, December 03, 2009 Sheet 19 of 44

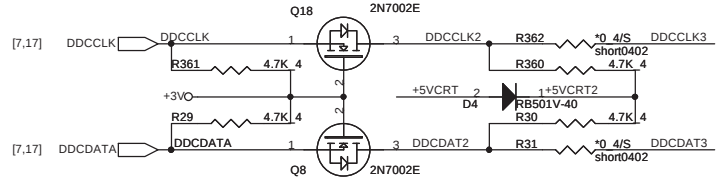
CRT PORT

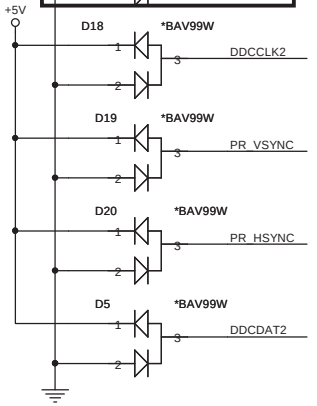












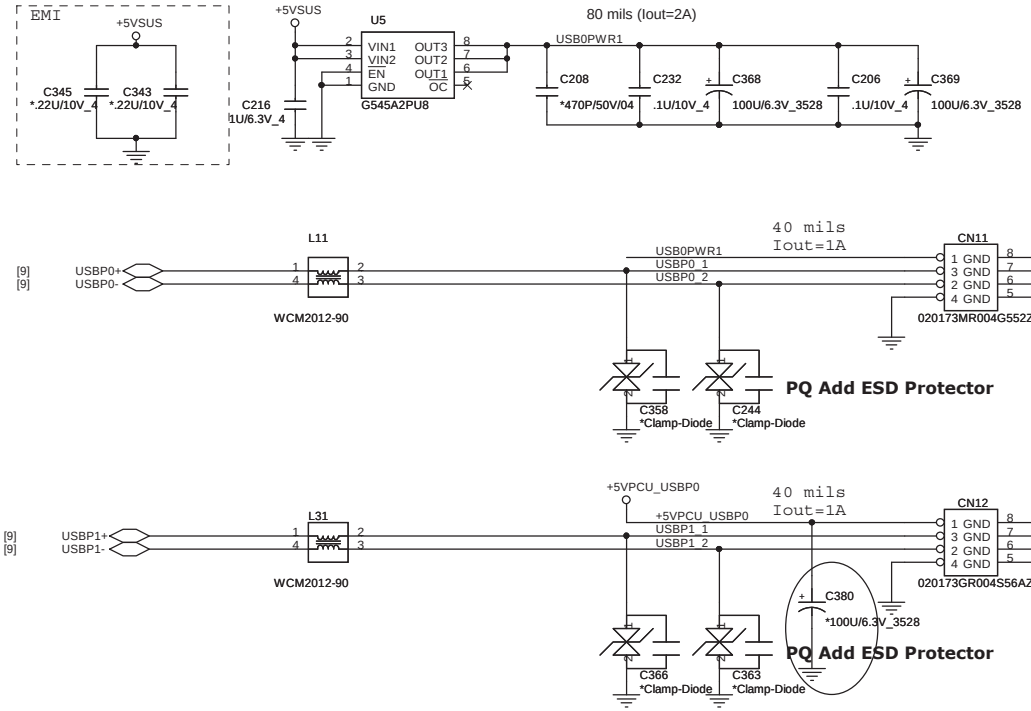
[2,3,7,8,9,10,11,12,13,19,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[11,19,22,23,25,26,28,30,37] +5V

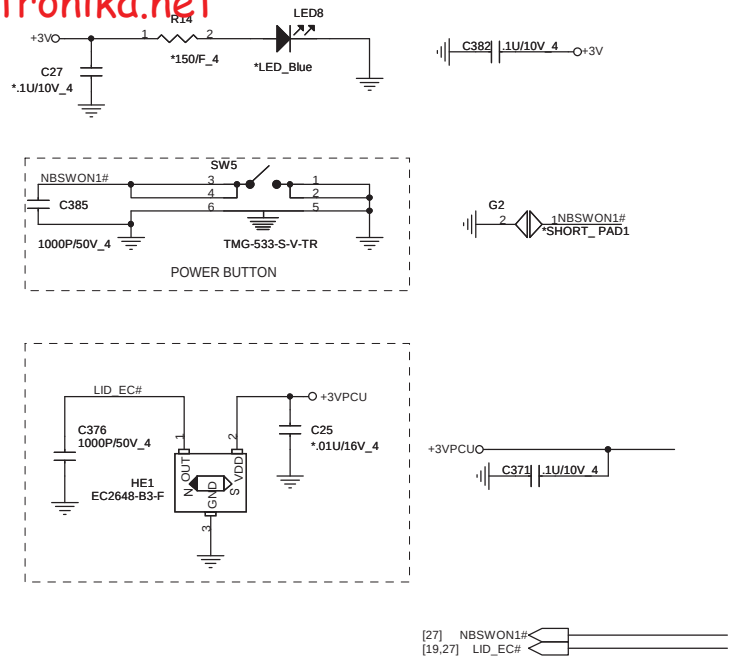
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A

Date: Wednesday, December 02, 2009 Sheet 20 of 44

USB CONNECTOR

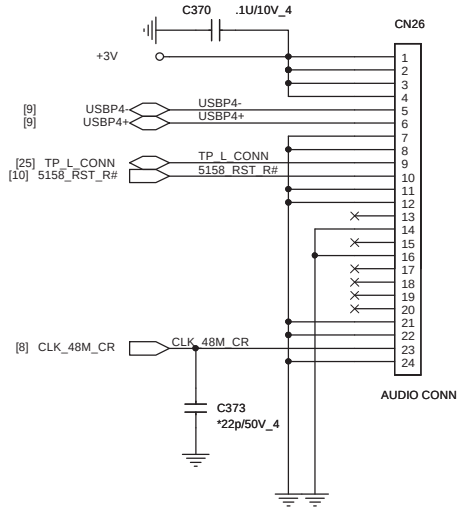




1. NBSWON1#
2. GND
3. GND
4. LID_EC#
5. +3V
6. +3VPCU

TO M/B CON.

PV Change CN2 footprint 88501-2001-24p-l-nb5



[7,19,23,26,27,28,31,32,33,35,37,38,39] +3VPCU
[2,3,7,8,9,10,11,12,13,19,20,22,23,24,25,26,27,28,29,30,34,37,39] +3V

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159 &CR SOCKET	1A

Date: Wednesday, December 02, 2009 Sheet 21 of 44

Close to Pin1
+3V +3V_DVDD
C411 1U/6.3V_4
C410 1U/10V_4
C400 10U/6.3V_8

+4.75VAVDD
L29 *0_8
+5V
AGND
C418 10U/6.3V_8
C683 .1U/10V_4
C673 4.7U/6.3V_6
C684 1U/6.3V_4
U35
Vout Vin
BYP
GND EN
TPS793475
+5V
C669 10U/6.3V_8
C672 .1U/10V_4
C670 1U/6.3V_4
C671 .047U/25V_4
R563 10K_4
Vset=1.242V

Close to Pin9
C409 .1U/10V_4
+3V_DVDD
C676 .1U/10V_4
Close to Pin1
+4.75VAVDD
Close to Pin38
C431 10U/6.3V_8
C688 .1U/10V_4
C698 1U/10V_4
C417 10U/6.3V_8

U37
ALC272
DVDD DVDD-I/O AVDD2 AVDD1
SDATA-OUT
BIT-CLK
SDATA-IN
SYNC
RESET#
GPIO0-DMIC-12
DMIC-CLK
EAPD
MONO
SURR-L
SURR-R
NC
DMIC-CLK3/4
SPDIFO2
SPDIFO1
GPIO3/DMIC-34
PCBEEP
DVSS DVSS-I/O
FRONT-R
FRONT-L
HPOUT-R
HPOUT-L
LINE1-R
LINE1-L
LINE2-VREFO
MIC2-VREFO
LINE1-VREFO
MIC2-R
MIC2-L
LINE2-R
LINE2-L
MIC1-R
MIC1-L
Sense A
Sense B
CBN
CBP
CPVEE JDREF AVSS2 AVSS1 VREF MIC1-VREFO-L

[7] ACZ_SDOUT_AUDIO
[7] BIT_CLK_AUDIO
[7] ACZ_SDIN0
[7] ACZ_SYNC_AUDIO
[7] ACZ_RST#_AUDIO
R271 *22_4
ACZ_SDIN0_ADC
R565 33_4
[19] DIGITAL_D1
[19] DIGITAL_CLK
L30 BK1005HS601-T_4
[23] EAPD#

HP-R C407 .47U/10V_6 HP_R_C [23]
HP-L C434 .47U/10V_6 HP_L_C [23]
To Internal Speakers
AGND SHIELD
EARPO_R R581 75/F_4 EARP_R
EARPO_L R332 75/F_4 EARP_L

C691 2.2U/6.3V_6
C689 2.2U/6.3V_6
MIC1_R1 R577 1K/F_4 EXT_MIC_R R579 2.2K_4
MIC1_L1 R576 1K/F_4 EXT_MIC_L R575 2.2K_4
D26 RB501V-40
D25 RB501V-40
VREFOUT_B_L
TO Audio Jack MIC
SENSE_A R574 20K/F_4 SA_MIC#
SENSE_B R582 5.1K/F_4 SA_HP#
TO AUDIO/B CON.
C422 2.2U/6.3V_6

BIT_CLK_AUDIO C674 *27P/50V_4
ACZ_SDIN0_ADC C675 *27P/50V_4
FOR EMI

+3V_DVDD
C412 0.047U/10V
[7,10] SPKR
[27] PC_BEEP_EC
U20
NC7SZ86
R328 100K_4
C401 .1U/10V_4
C408 100P/50V_4
R316 10K/F_4
R326 10K_4
R321 150K/F_4

R324 0_6
R322 0_6
C415 1000P/50V_4
C414 1000P/50V_4
AGND

VREFOUT_B_L C696 *1U/6.3V_4
VREF_FLT C430 *10U/6.3V_8
C697 .1U/10V_4
R573 20K/F_4
C699 2.2U/6.3V_6

[19,21,25,26,37] +5VSUS
[11,19,20,23,25,26,28,30,37] +5V
[2,3,7,8,9,10,11,12,13,19,20,21,23,24,25,26,27,28,29,30,34,37,39] +3V

AUDIO CONNECTOR

10/07

EARP_L L34 0_6 EARP_L1
EARP_R L35 0_6 EARP_R1
R266 22K/F_6
R267 22K/F_6
R265 *1K/F_4
R263 *1K/F_4
C15 100P/50V_4
C16 100P/50V_4
C29 Clamp-Diode
C26 Clamp-Diode
Change HP-PLG link

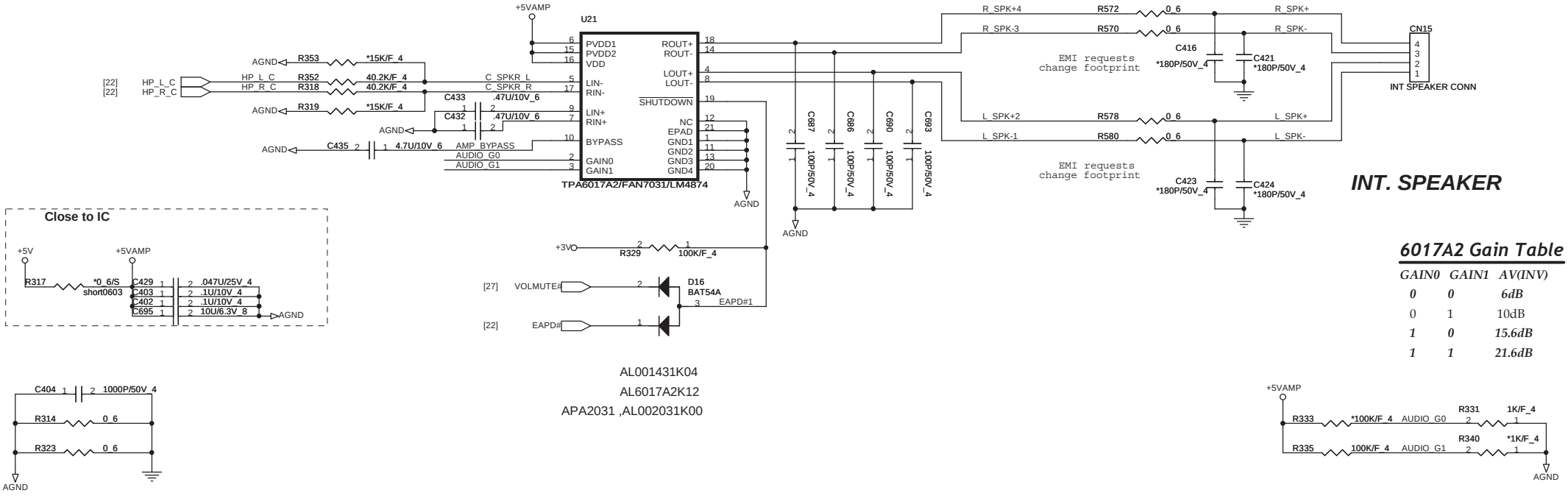
CN1
HP-JACK-GREEN
Normal close
headphone close to USB Port
SA_HP# SA_HP# C
D30 *3301D-ESD
+4.75VAVDD
R336 *10K_4
Q44 DMN601K-7

AUDIO JACKS CHANGE TO NORMAL OPEN

C17 100P/50V_4
EXT_MIC_L L32 0_6 MIC_IN_L
EXT_MIC_R L33 0_6 MIC_IN_R
C24 100P/50V_4
CN4
MIC-JACK-PINK
Normal close
Mic close to front side
SA_MIC# SA_MIC# C
D31 *3301D-ESD
R337 10K_4
Q43 DMN601K-7

PROJECT : SW9
Quanta Computer Inc.
Size Custom
Document Number Azalia ALC272/BT CONN
Rev 1A
Date: Wednesday, December 02, 2009 Sheet 22 of 44

AUDIO AMPLIFIER



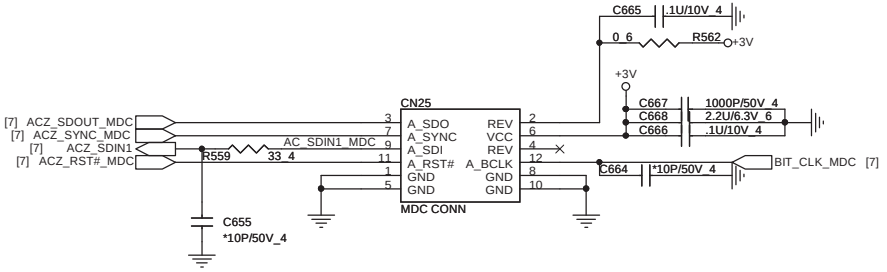
INT. SPEAKER

6017A2 Gain Table

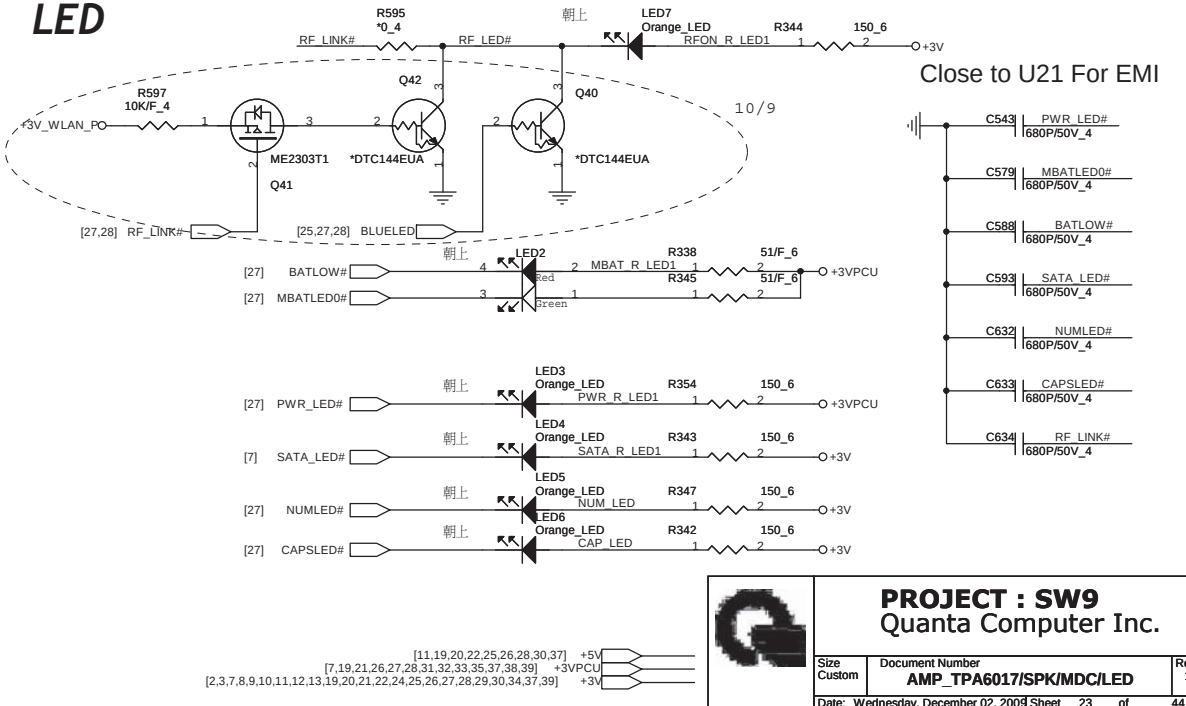
GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

AL001431K04
AL6017A2K12
APA2031 ,AL002031K00

MDC CONNECTOR



LED

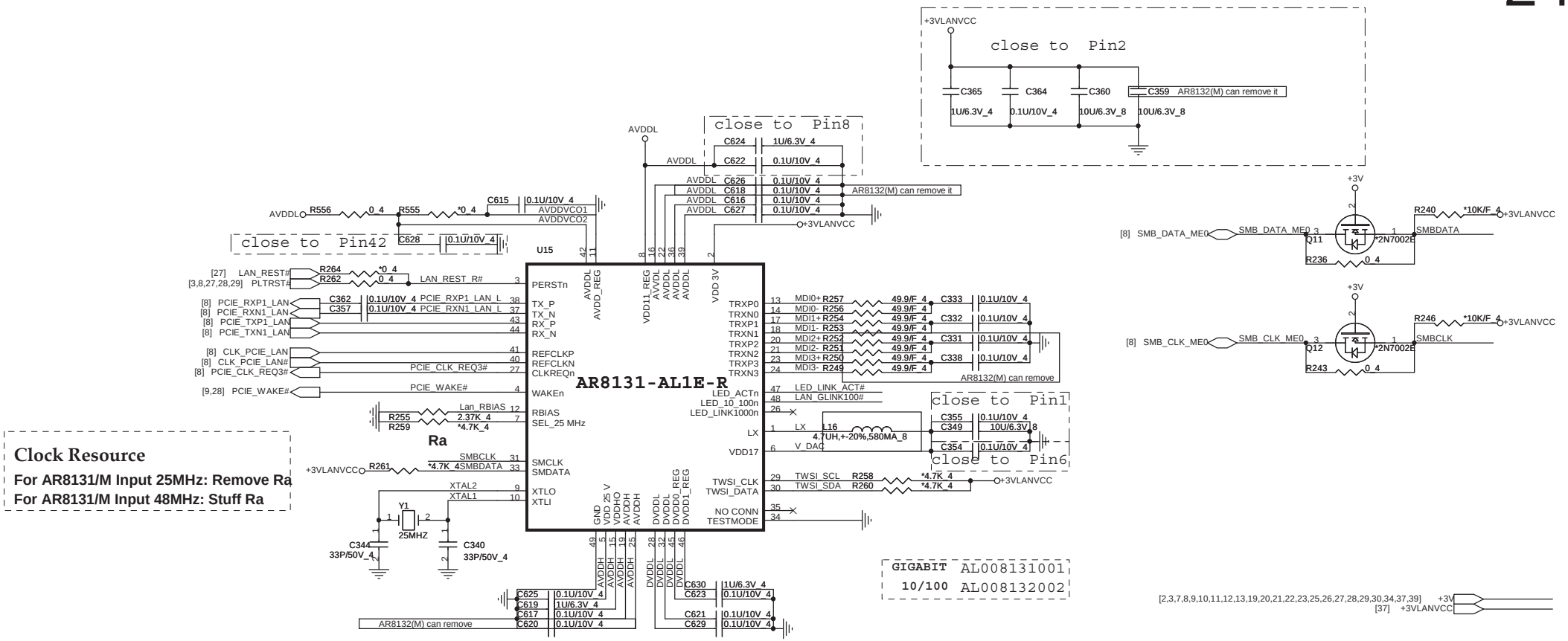


[11,19,20,22,25,26,28,30,37] +5V
[7,19,21,26,27,28,31,32,33,35,37,38,39] +3VPCU
[2,3,7,8,9,10,11,12,13,19,20,21,22,24,25,26,27,28,29,30,34,37,39] +3V

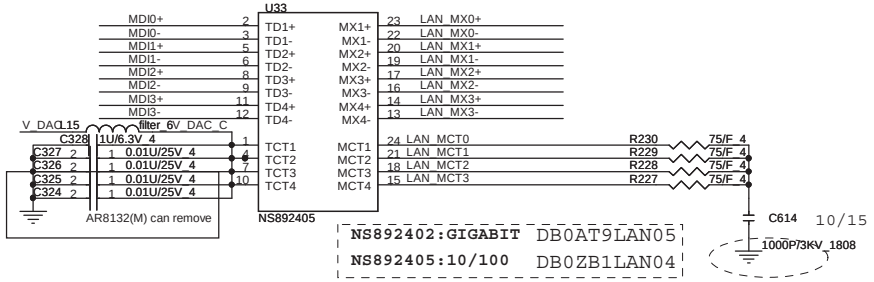
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/SPK/MDC/LED	1A

Date: Wednesday, December 02, 2009 Sheet 23 of 44



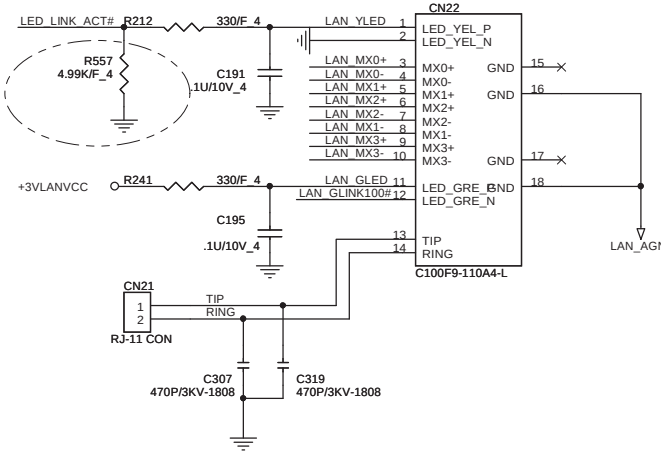
Transformer for 10/100/1000

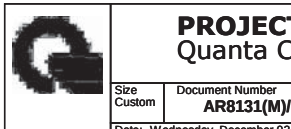


Lan Connector

RJ45

C105,C135 FOR EMI CLOSE TO RJ45



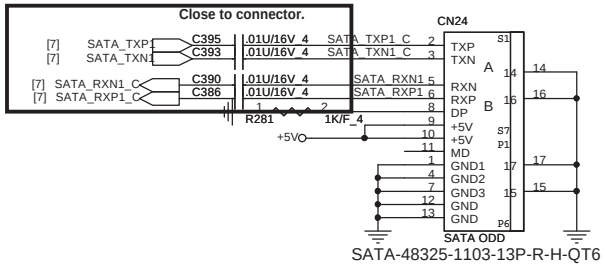


PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AR8131(M)/RJ45	1A

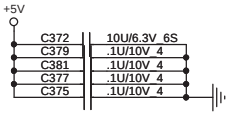
Date: Wednesday, December 02, 2009 Sheet 24 of 44

SATA ODD

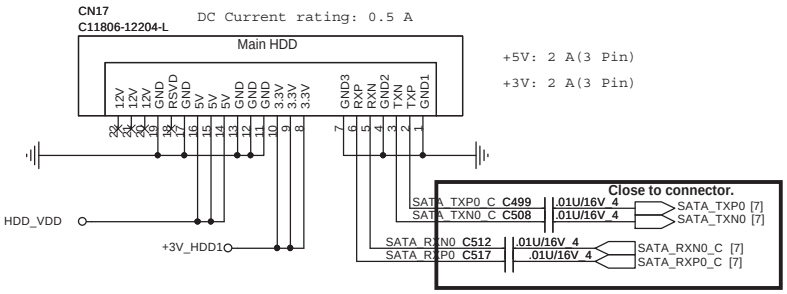


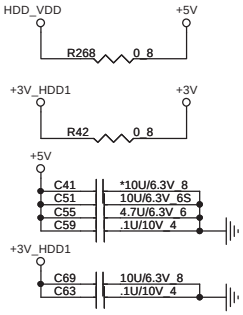
SATA-48325-1103-13P-R-H-QT6

120 mils

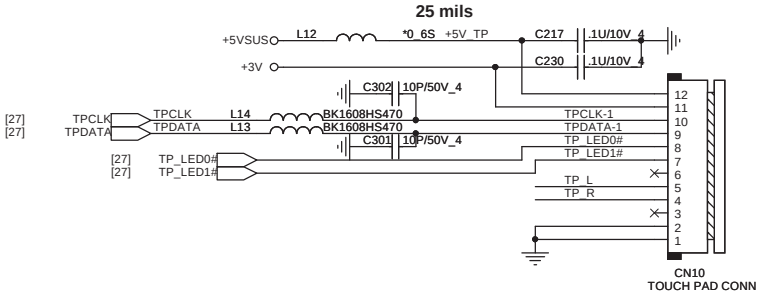


SATA_1 CONNECTOR

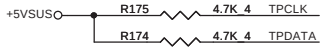




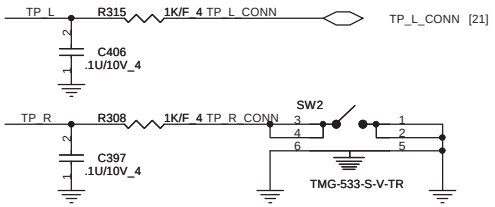
TOUCH PAD CONNECTOR



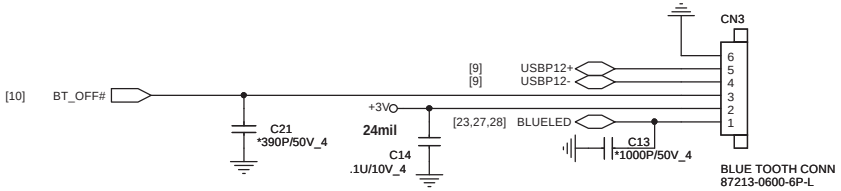
close conn



TOUCH PAD L/R SW1,SW2 in QL2 use, SW3,SW4 in SW9 use



Bluetooth



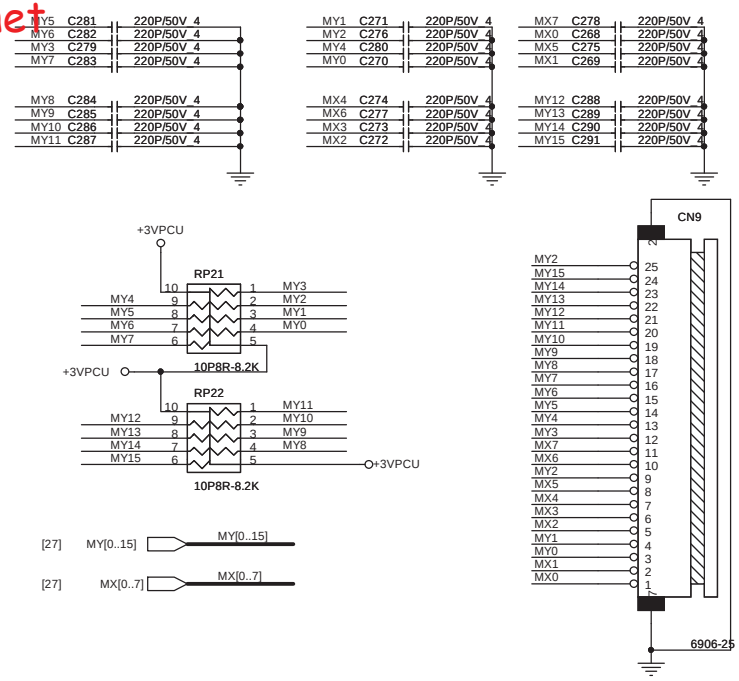
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,26,27,28,29,30,34,37,39] +3V
[11,19,20,22,23,26,28,30,37] +5V
[19,21,26,37] +5VSUS

PROJECT : SW9
Quanta Computer Inc.

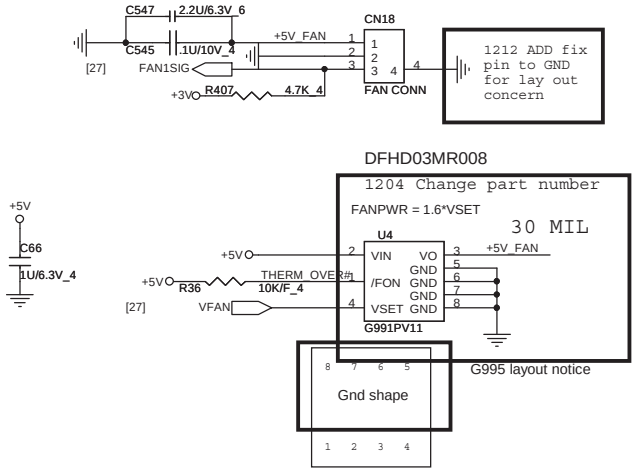
Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD/TP	1A

Date: Wednesday, December 02, 2009 Sheet 25 of 44

KEYBOARD Con.

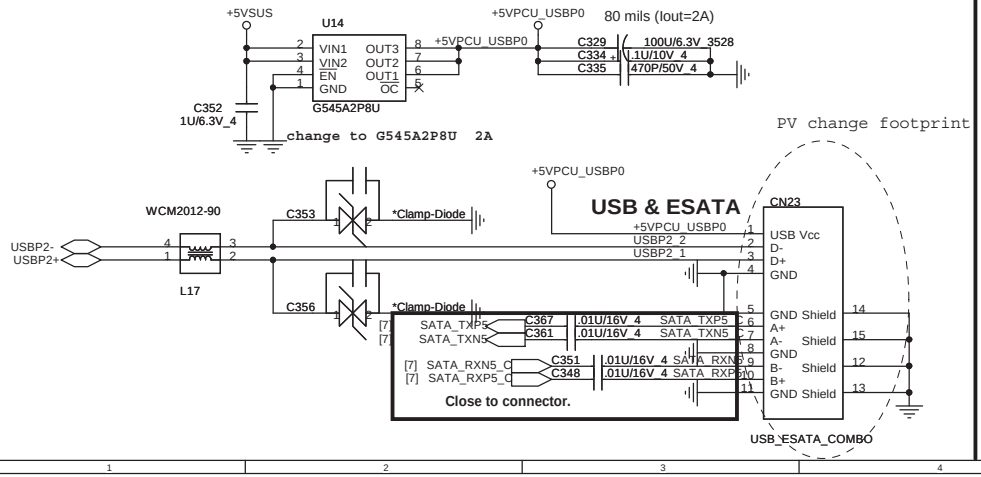


CPU FAN



Capacity board Con.

E-SATA/USB COMBO



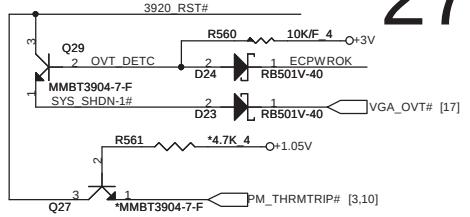
[11,19,20,22,23,25,28,30,37] +5V
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,27,28,29,30,34,37,39] +3V
[7,19,21,23,27,28,31,32,33,35,37,38,39] +3VPCU
[27,31,32,33,34,35,36,37] +5VPCU

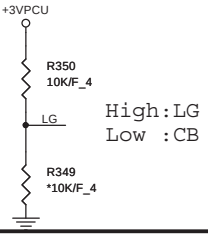
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/PWR/ESATA/FAN/CAM/MIC	1A

Date: Wednesday, December 02, 2009 Sheet 26 of 44

thermal shutdown circuit





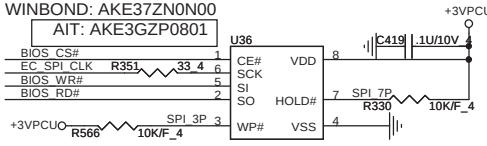
SPI BIOS

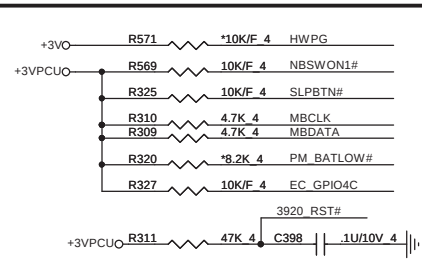
512K byte SPI ROM for EC

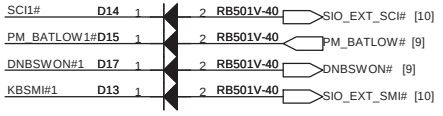
MXIC: AKE3KZP0001
WINBOND: AKE37ZN0N00
AIT: AKE3GZP0801

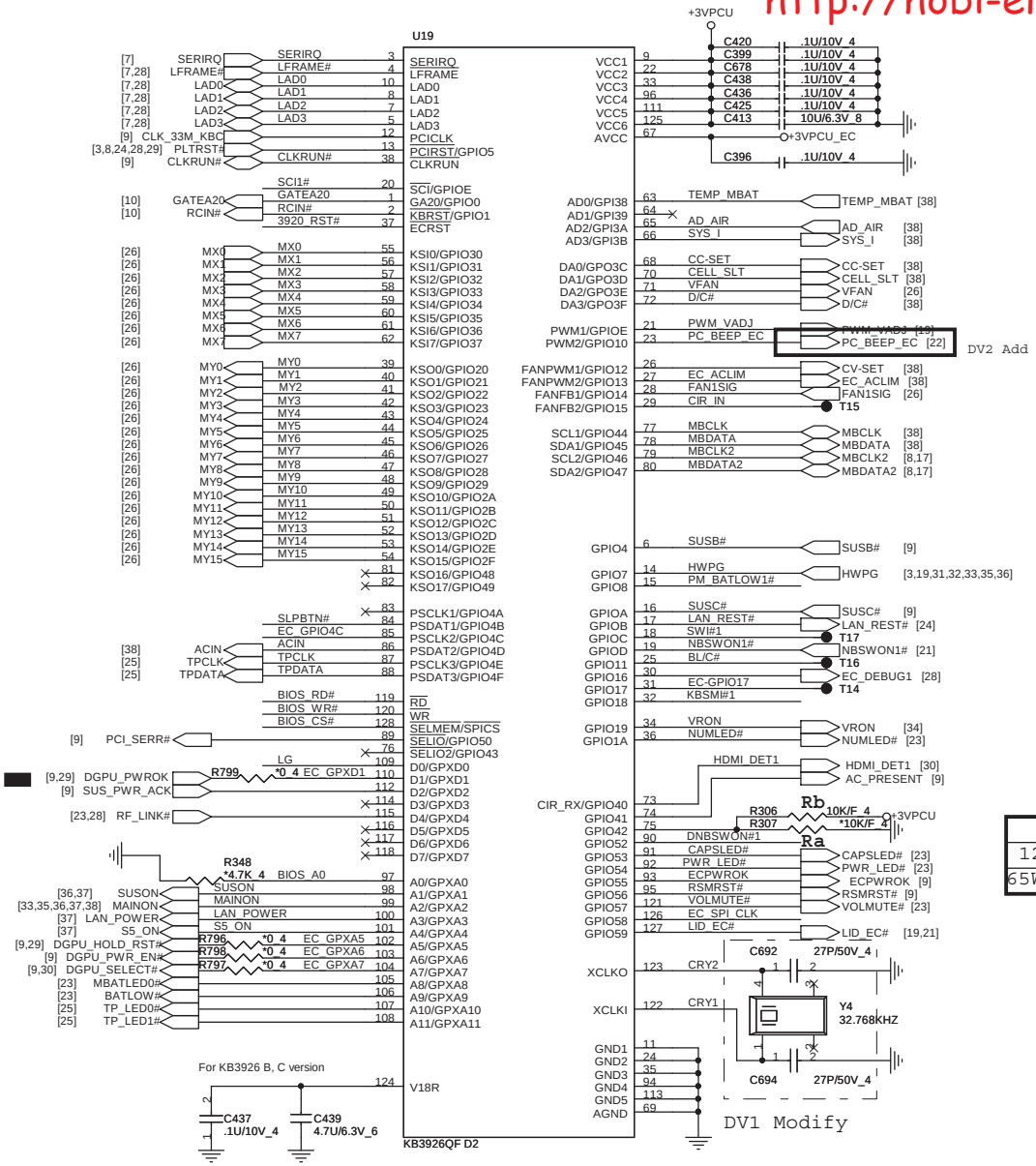
SPI ROM Socket

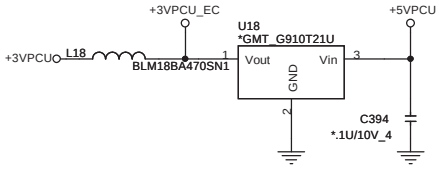
DG008000031

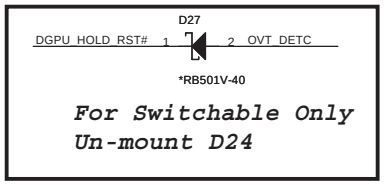






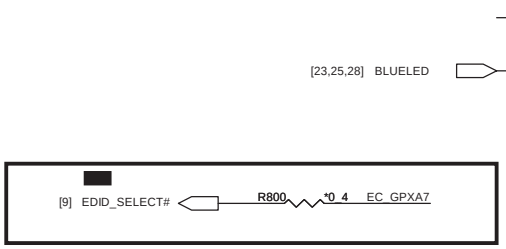


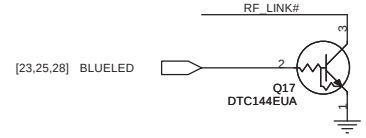




Adapter table select

ID	Ra	Rb
120W	10K	N/A
65W/90W	N/A	10K





[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,28,29,30,34,37,39] +3V
[7,19,21,23,26,28,31,32,33,35,37,38,39] +3VPCU
[31,32,33,34,35,36,37] +5VPCU

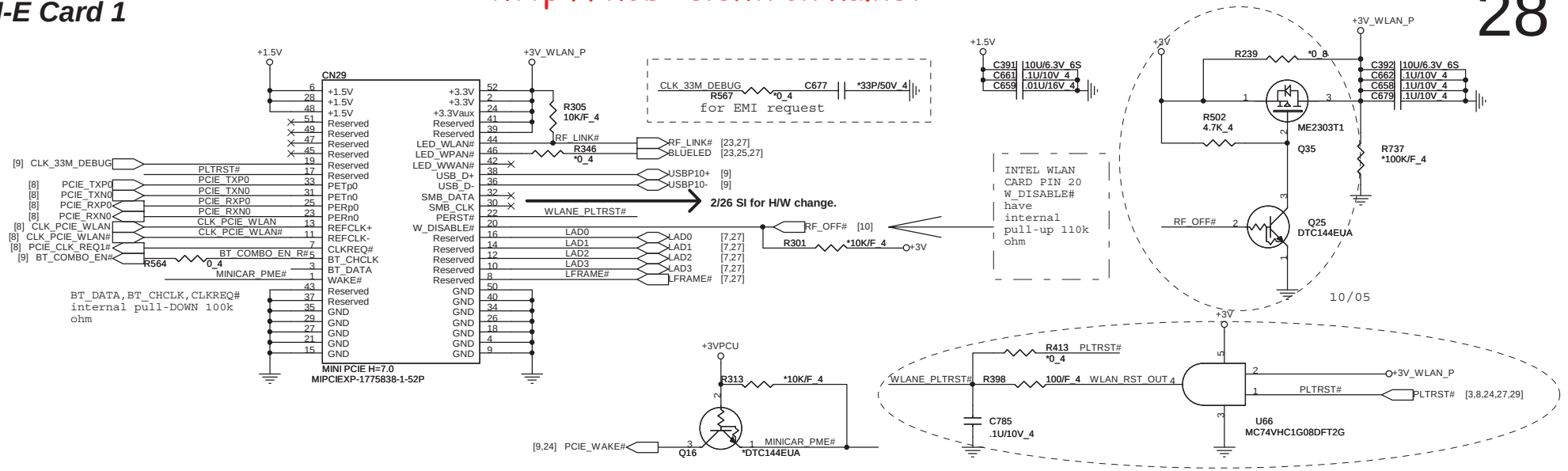
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3926/ROM/TP	1A

Date: Wednesday, December 02, 2009 Sheet 27 of 44

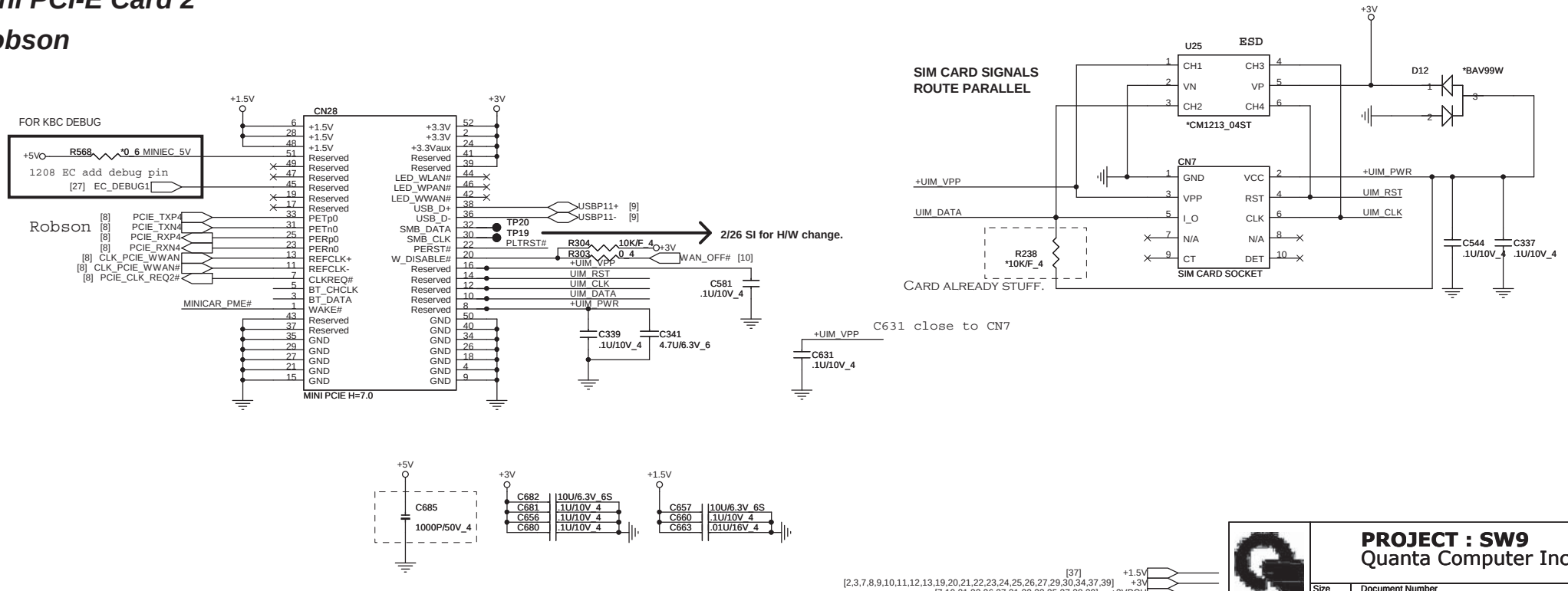
Mini PCI-E Card 1

WLAN



Mini PCI-E Card 2

Robson



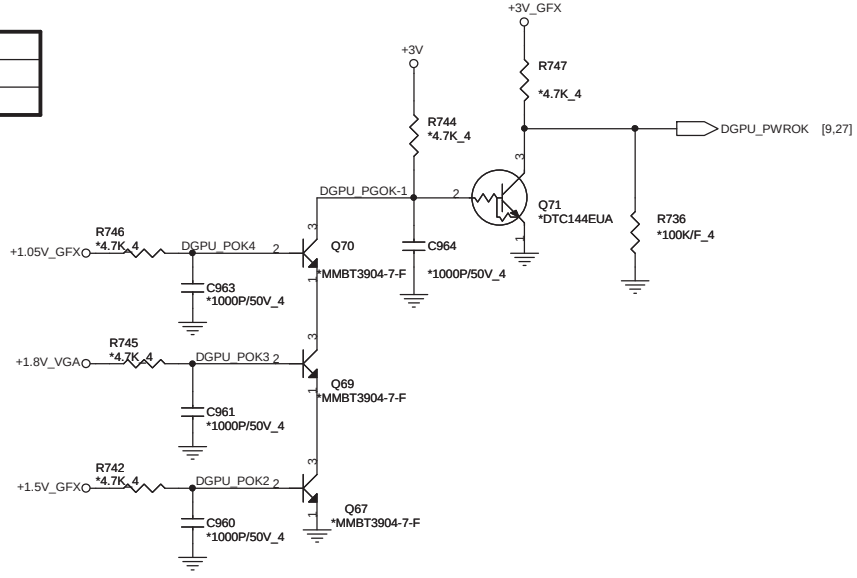
PROJECT : SW9	Quanta Computer Inc.
Size: Custom	Document Number: MINI PCIE CONN X2
Rev: 1A	
Date: Wednesday, December 02, 2009	Sheet 28 of 44

DEL Switch IC

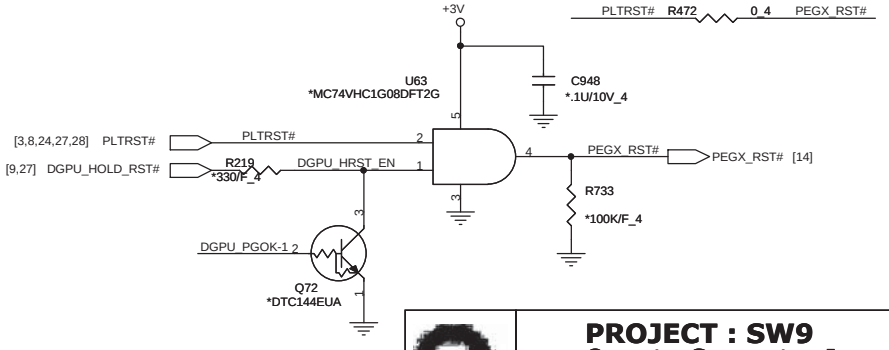
DEL Switch IC

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

SELx	Ay
LOW	B1
HIGH	B2



Discrete Only



PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS / CRT Switch	1A

Date: Wednesday, December 02, 2009 Sheet 29 of 44

DGPU_HDMI

[16] H_TX2_HDMI+ C226 *.1U/10V_4 DGPU_TX2_HDMI+
[16] H_TX2_HDMI- C233 *.1U/10V_4 DGPU_TX2_HDMI-
[16] H_TX1_HDMI+ C219 *.1U/10V_4 DGPU_TX1_HDMI+
[16] H_TX1_HDMI- C209 *.1U/10V_4 DGPU_TX1_HDMI-
[16] H_TX0_HDMI+ C243 *.1U/10V_4 DGPU_TX0_HDMI+
[16] H_TX0_HDMI- C252 *.1U/10V_4 DGPU_TX0_HDMI-

[16] H_TXC_HDMI+ C202 *.1U/10V_4 DGPU_TXC_HDMI+
[16] H_TXC_HDMI- C193 *.1U/10V_4 DGPU_TXC_HDMI-

HDMISwitch

U64 PI3HDMI201

DGPU_TXC_HDMI- 55 CLK-A
DGPU_TXC_HDMI+ 56 CLK+A
DGPU_TX0_HDMI- 2 D0-A
DGPU_TX0_HDMI+ 3 D0+A
DGPU_TX1_HDMI- 5 D1-A
DGPU_TX1_HDMI+ 6 D1+A
DGPU_TX2_HDMI- 8 D2-A
DGPU_TX2_HDMI+ 9 D2+A

HPD_SINK 47 HDMI_DET_S
SDA_SINK 46 HDMI_SDATA
SCL_SINK 45 HDMI_SCLK

CLK- 43 C_TXC_HDMI-
CLK+ 42 C_TXC_HDMI+
D0- 40 C_TX0_HDMI-
D0+ 39 C_TX0_HDMI+
D1- 37 C_TX1_HDMI-
D1+ 36 C_TX1_HDMI+
D2- 34 C_TX2_HDMI-
D2+ 33 C_TX2_HDMI+

[17] HDMI_DET HDMI_DET 51 HPDA
[16] HDMI_SDA_DGPU 52 SDAA
[16] HDMI_SCL_DGPU 53 SCLA
[7] HDMI_HPD_CON 23 HPDB
[7] SDVO_DATA 24 SDAB
[7] SDVO_CLK 25 SCLB

PAD_GND 57
GND 4, 10, 16, 22, 32, 38, 44, 54

[7] IN_CLK# 11 CLK-B
[7] IN_CLK 12 CLK+B
[7] IN_D0# 14 D0-B
[7] IN_D0 15 D0+B
[7] IN_D1# 17 D1-B
[7] IN_D1 18 D1+B
[7] IN_D2# 20 D2-B
[7] IN_D2 21 D2+B

EQ_S1, EQ_S0, OC_S2, OC_S1, OC_S0, SEL2, SEL1

HSW_EQS1 26, HSW_EQS0 28, HSW_OCS2 29, HSW_OCS1 30, HSW_OCS0 31, HSW_ON# 50, HSW_SEL2 27, HSW_SEL1 49

+5V, VDD 48, 41, 35, 19, 13, 7, 1

To HDMI Conn.

IGPU_HDMI

+3V
R486 2K/F_4 SDVO_DATA
R500 2K/F_4 SDVO_CLK

C955 0.1U/10V_4
C954 0.1U/10V_4
C945 0.1U/10V_4
C950 0.1U/10V_4

OC SETTING
S2 S1 S0 = 1 : 1 : 1 500mV 0dB Defualt
S2 S1 S0 = 1 : 1 : 0 750mV 0dB
S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
S2 S1 S0 = 1 : 0 : 0 600mV 0dB
S2 S1 S0 = 0 : 1 : 1 500mV 0dB
S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
S2 S1 S0 = 0 : 0 : 0 500mV 6dB

EQ SETTING
S1 S0 = 1 : 1 3dB Defualt
S1 S0 = 1 : 0 8dB
S1 S0 = 0 : 1 3dB
S1 S0 = 0 : 0 15dB

HSW_EQS1 R628 *4.7K_4
HSW_EQS0 R627 *4.7K_4
HSW_OCS2 R626 *4.7K_4
HSW_OCS1 R625 *4.7K_4
HSW_OCS0 R624 *4.7K_4
HSW_ON# R623 4.7K_4

OE#	SEL2	SEL1	Ay
0	X	1	A
0	1	0	B

+3V
R630 *4.7K_4
HSW_SEL1
Q33 *DTC144EUA
R629 4.7K_4
2 DGPU_SELECT# DGPU_SELECT# [9,27]
R631 *0_4 HSW_SEL2
R632 4.7K_4
+3V

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

Mount R629 / R632 for UMA only

Only for NVIDIA

+3V_GFX
Q26 *2N7002E
R146 *499/F_4 DGPU_TXC_HDMI-
R150 *499/F_4 DGPU_TXC_HDMI+
R144 *499/F_4 DGPU_TX0_HDMI-
R137 *499/F_4 DGPU_TX0_HDMI+
R151 *499/F_4 DGPU_TX1_HDMI-
R156 *499/F_4 DGPU_TX1_HDMI+
R136 *499/F_4 DGPU_TX2_HDMI-
R124 *499/F_4 DGPU_TX2_HDMI+

DGPU_TXC_HDMI- RP35 *0_4P2R C_TXC_HDMI-
DGPU_TXC_HDMI+ C_TXC_HDMI+
DGPU_TX0_HDMI- RP38 *0_4P2R C_TX0_HDMI-
DGPU_TX0_HDMI+ C_TX0_HDMI+
DGPU_TX1_HDMI- RP36 *0_4P2R C_TX1_HDMI-
DGPU_TX1_HDMI+ C_TX1_HDMI+
DGPU_TX2_HDMI- RP37 *0_4P2R C_TX2_HDMI-
DGPU_TX2_HDMI+ C_TX2_HDMI+

HDMI_DET R469 *0_4 HDMI_DET_S
HDMI_SCL_DGPU R458 *4.7K_4 HDMI_SCLK
HDMI_SDA_DGPU R457 *4.7K_4 HDMI_SDATA
+3V_GFX D21 *RB501V-40
+3V_GFX D28 *RB501V-40
+3V
*FDV301N Q23
*FDV301N Q22

For Switchable Only

HDMI PORT

CN20 HDMI CONN
SHELL1 20
D2+ 1
D2 Shield 2
D2- 3
D1+ 4
D1 Shield 5
D1- 6
D0+ 7
D0 Shield 8
D0- 9
CK+ 10
CK Shield 11
CK- 12
CE Remote 13
NC 14
DDC CLK 15
DDC DATA 16
GND 17
+5V 18
HP DET 19
SHELL2 21

C_TX2_HDMI+ 1
C_TX2_HDMI- 3
C_TX1_HDMI+ 4
C_TX1_HDMI- 6
C_TX0_HDMI+ 7
C_TX0_HDMI- 9
C_TXC_HDMI+ 10
C_TXC_HDMI- 12

+5V_HDMIC D9 RB501V-40
+5V_HDMIC D29 RB501V-40

R112 2.2K/F_4
R109 2.2K/F_4
HDMI_SCLK R111 0_4 HDMISCL
HDMI_SDATA R110 0_4 HDMISDA
C567 *10P/50V_4
C566 *10P/50V_4
+5V F2 FUSE1A6V_POLY +5V_HDMIC

[27] HDMI_DET1 R464 *0_4
HDMI_DET_S R461 10K/F_4
HDMI_DET_N L26 BLM18BA470SN1D
HDMI_DET_C C564 220P/50V_4

D22 BAV99W
R488 110K/F_4
+3V

+5V_HDMIC C157 *.01U/16V_4
for EMI request

R806 *100/F_4 C_TX2_HDMI+ C_TX2_HDMI-
R807 *100/F_4 C_TX1_HDMI+ C_TX1_HDMI-
R808 *100/F_4 C_TX0_HDMI+ C_TX0_HDMI-
R809 *100/F_4 C_TXC_HDMI+ C_TXC_HDMI-

Close to CN20

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
A3	HDMI Switch	1A

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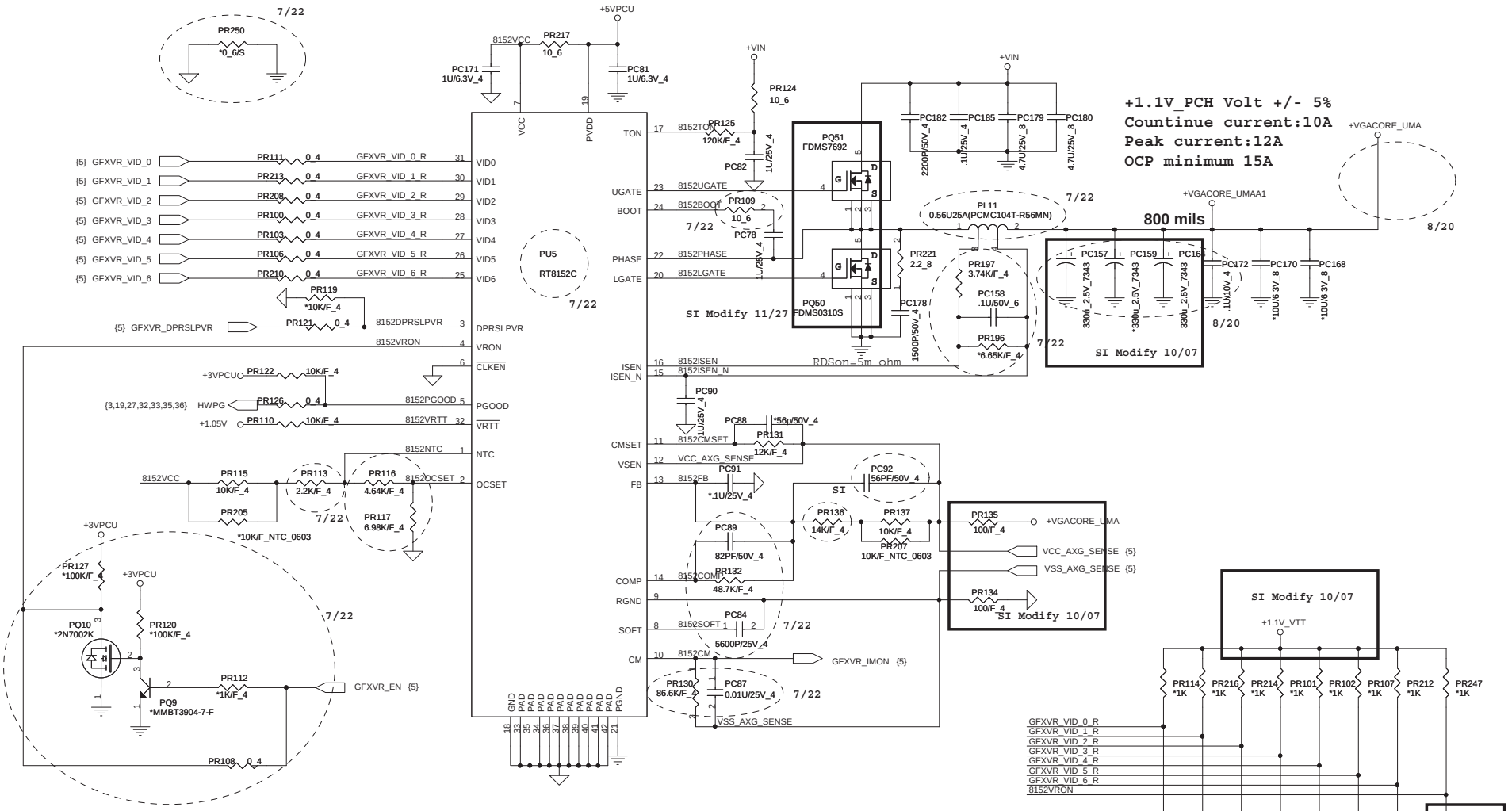
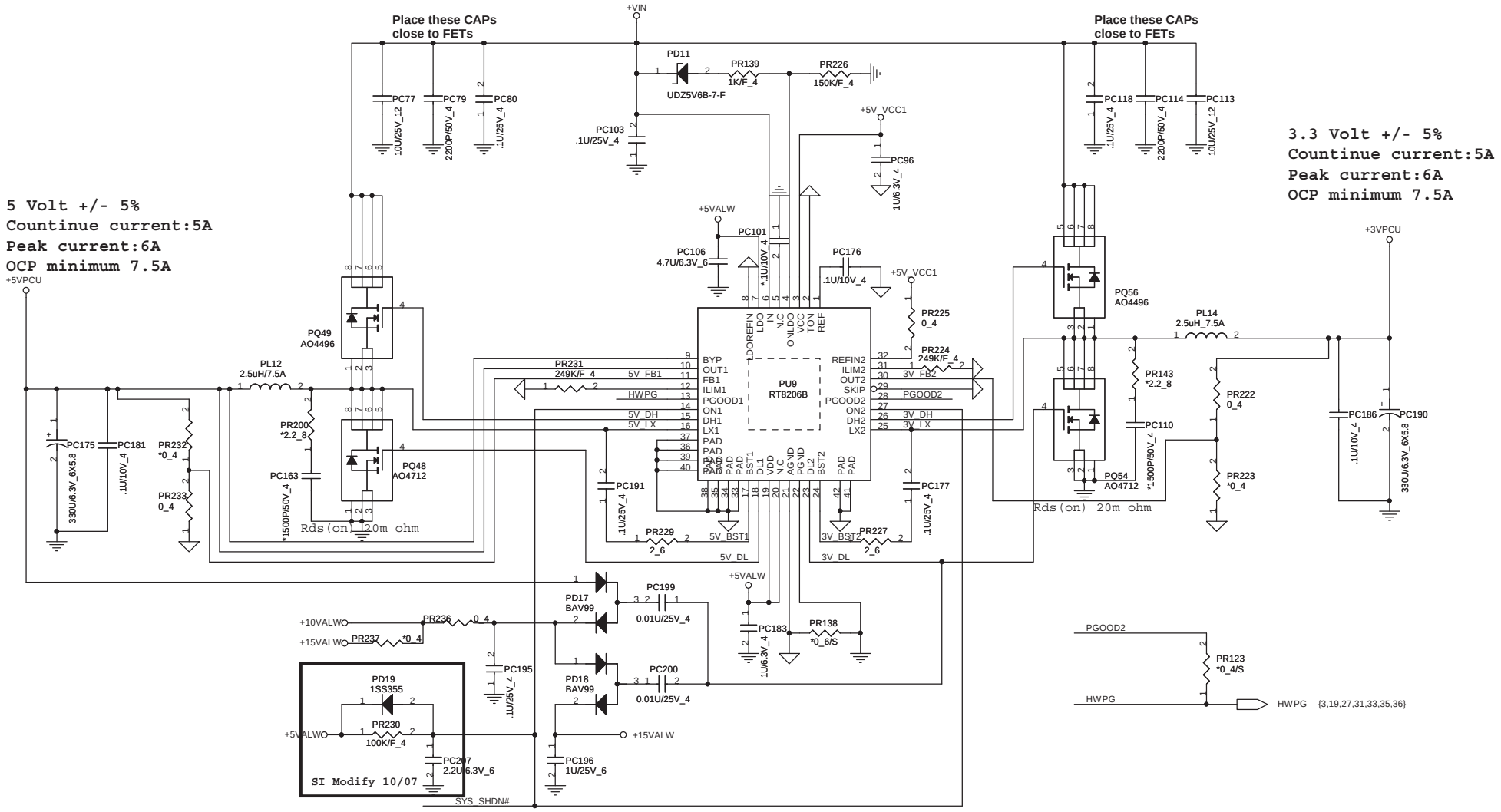
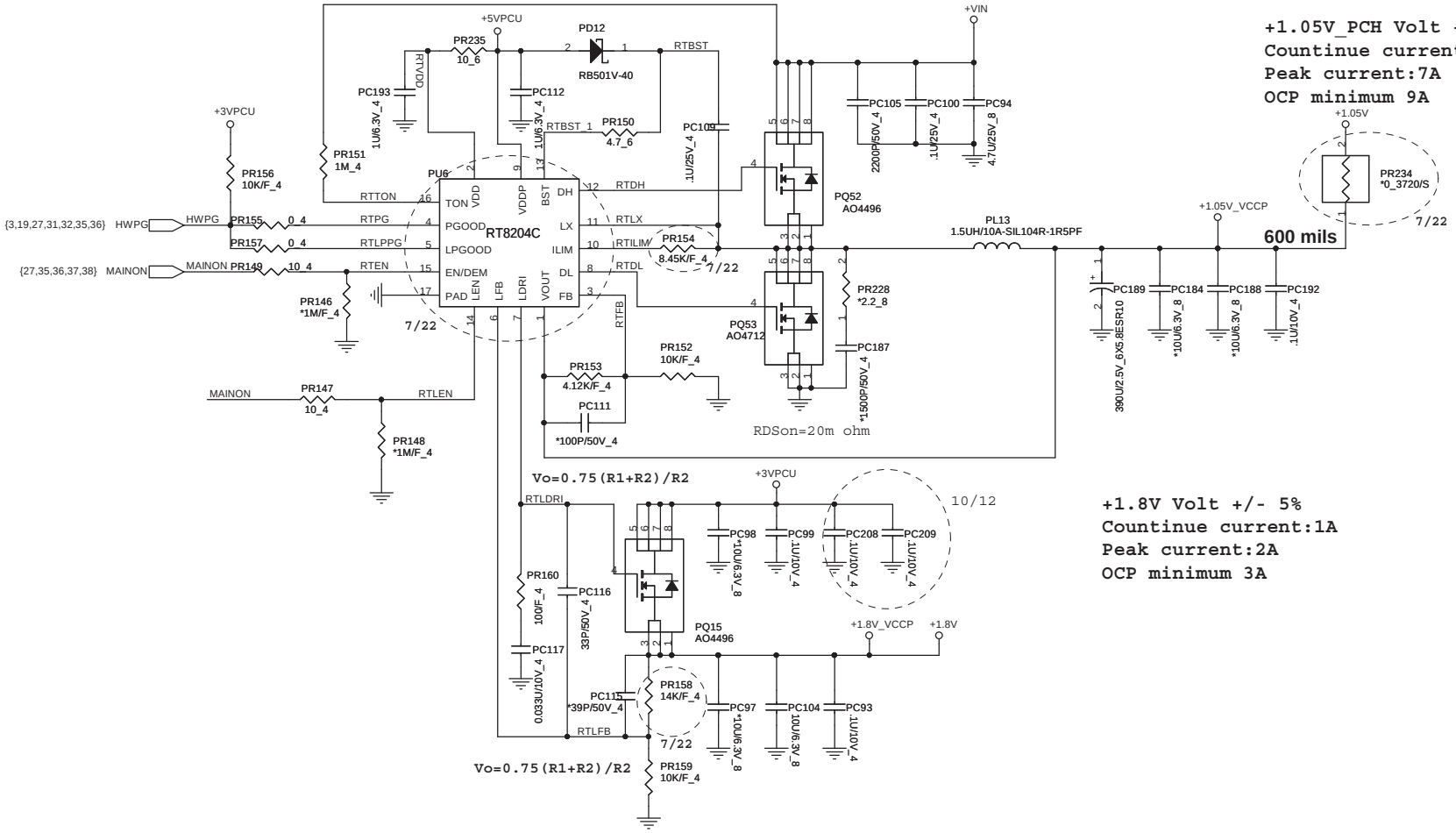




PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A

Date: Wednesday, December 02, 2009 Sheet 32 of 44



+1.05V_PCH Volt +/- 5%
Countinue current:4A
Peak current:7A
OCP minimum 9A

+1.8V Volt +/- 5%
Countinue current:1A
Peak current:2A
OCP minimum 3A

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH +1.05V (RT8204)	1A

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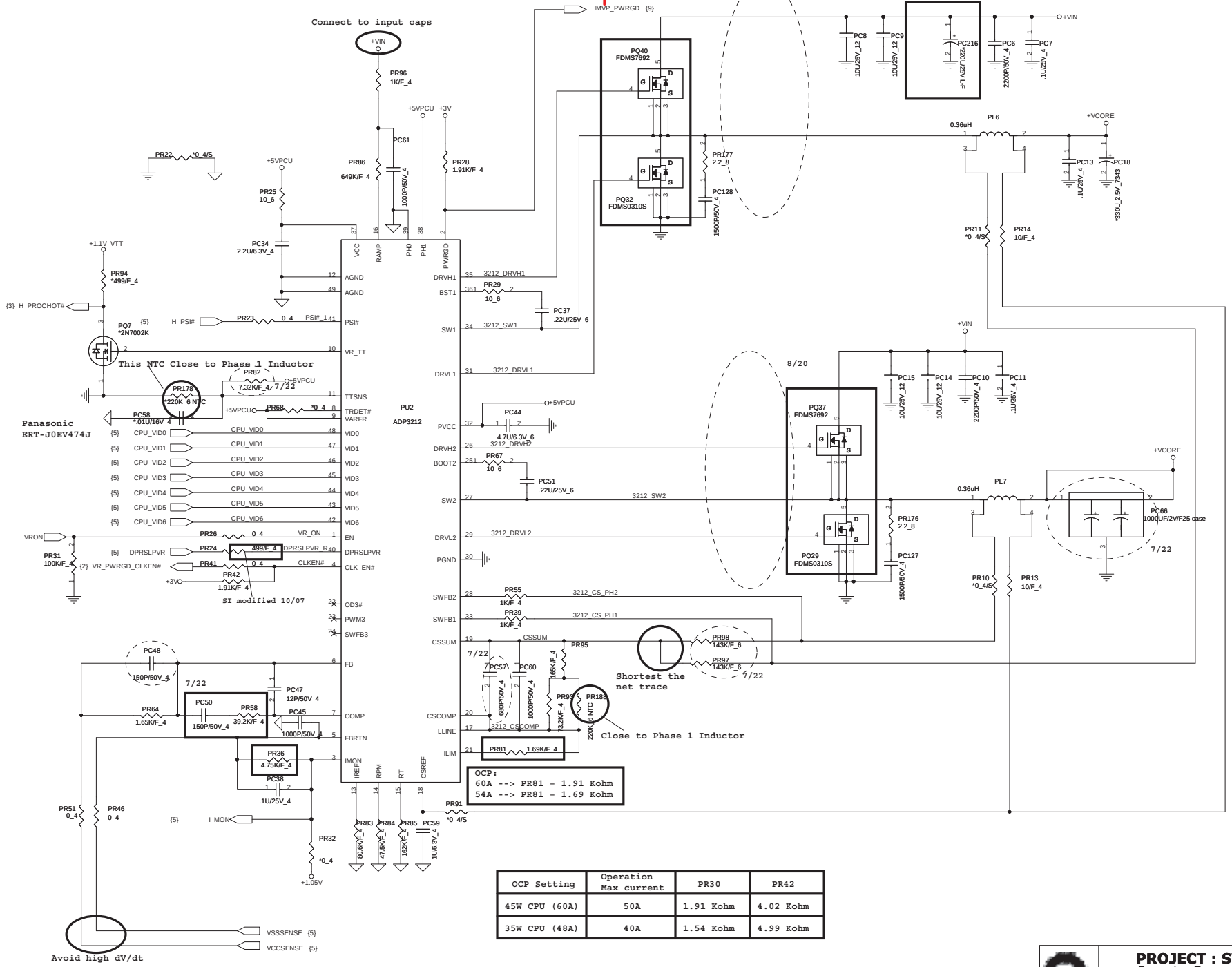

OCP Setting	Operation Max current	PR30	PR42
45W CPU (60A)	50A	1.91 Kohm	4.02 Kohm
35W CPU (48A)	40A	1.54 Kohm	4.99 Kohm

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (ADP3212)	1A

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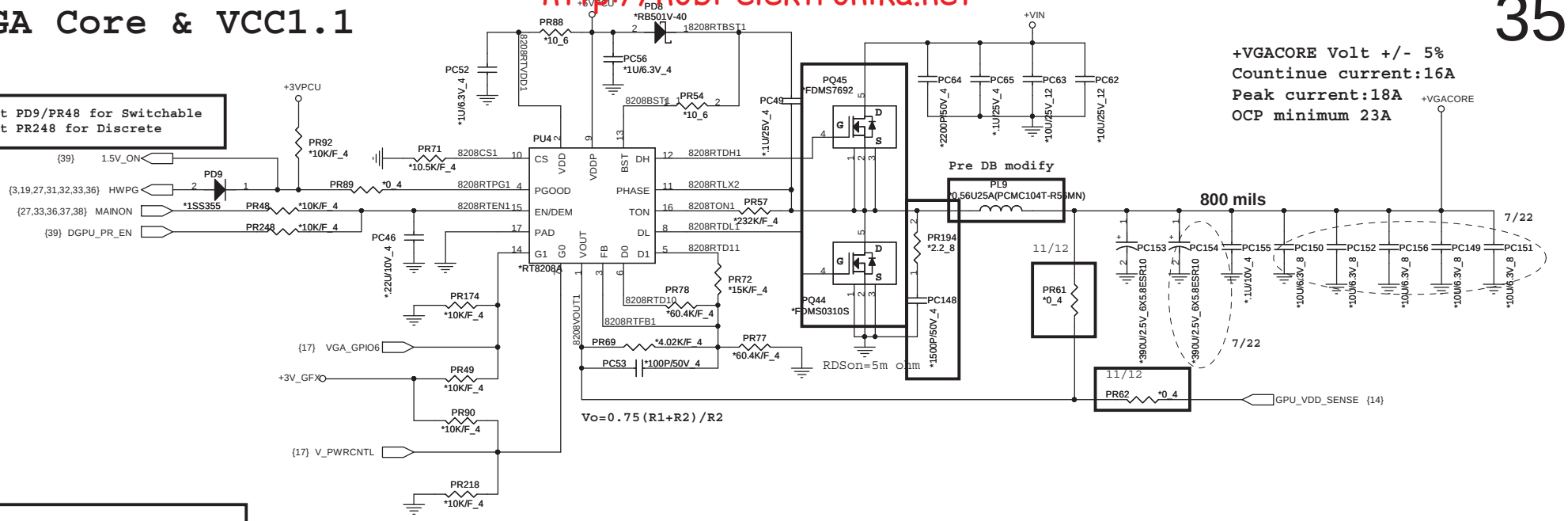
VGA Core & VCC1.1

1 : un-Mount PD9/PR48 for Switchable
2 : un-Mount PR248 for Discrete

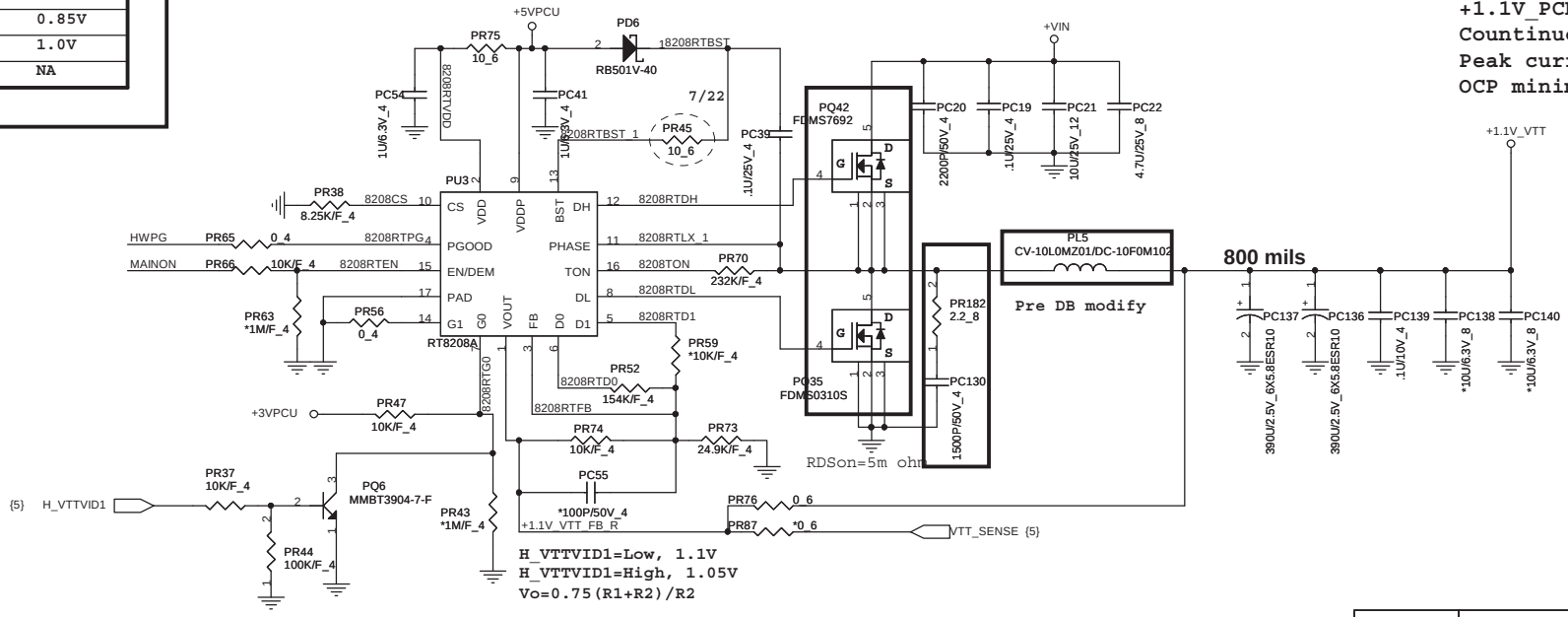
+VGACORE Volt +/- 5%
Countinue current:16A
Peak current:18A
OCP minimum 23A



4/1

VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5	N10M-GS
0	0	0.8V
0	1	0.85V
1	0	1.0V
1	1	NA

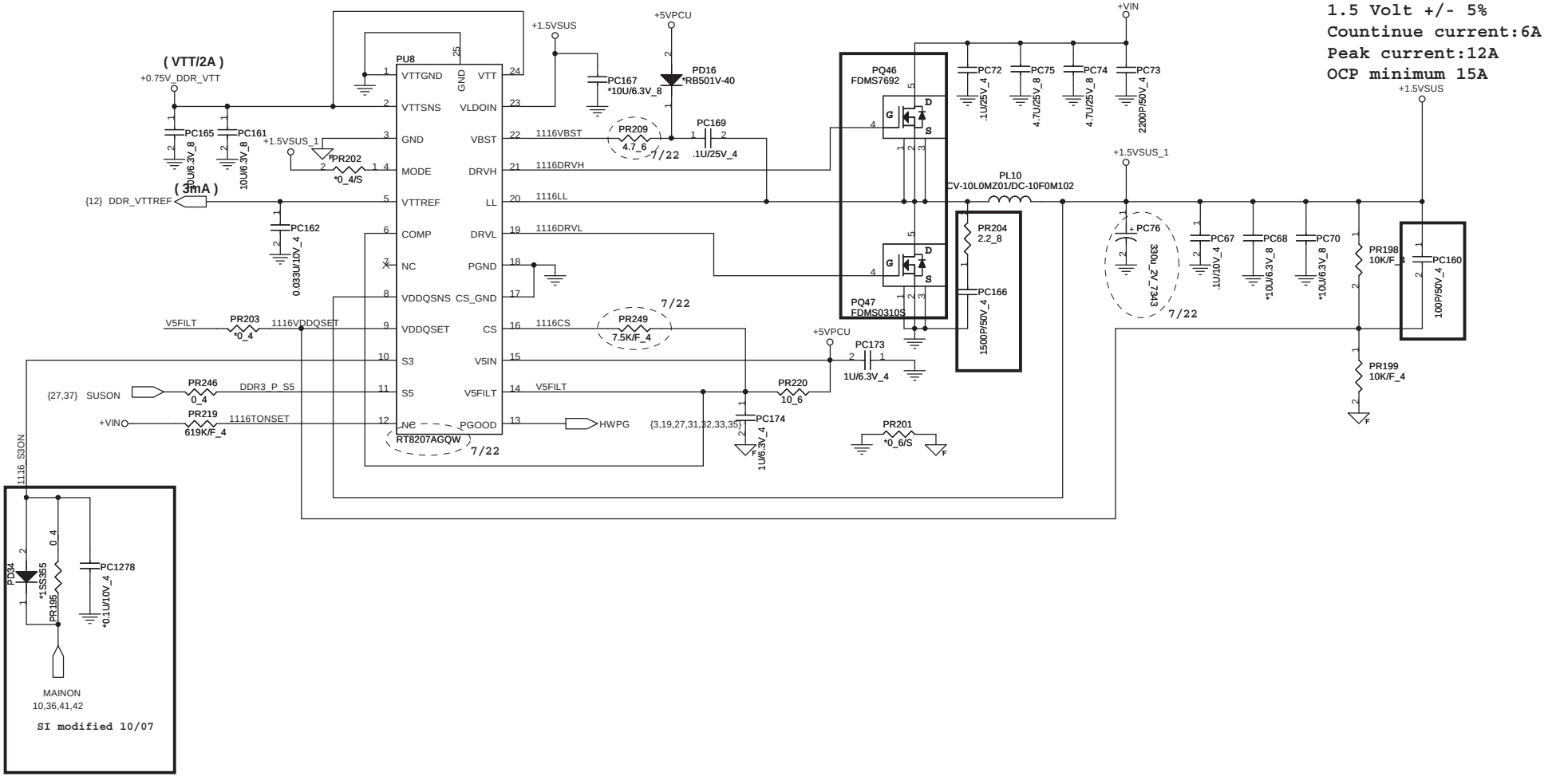
+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A



PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V_VTT/VGA Core RT820A	1A

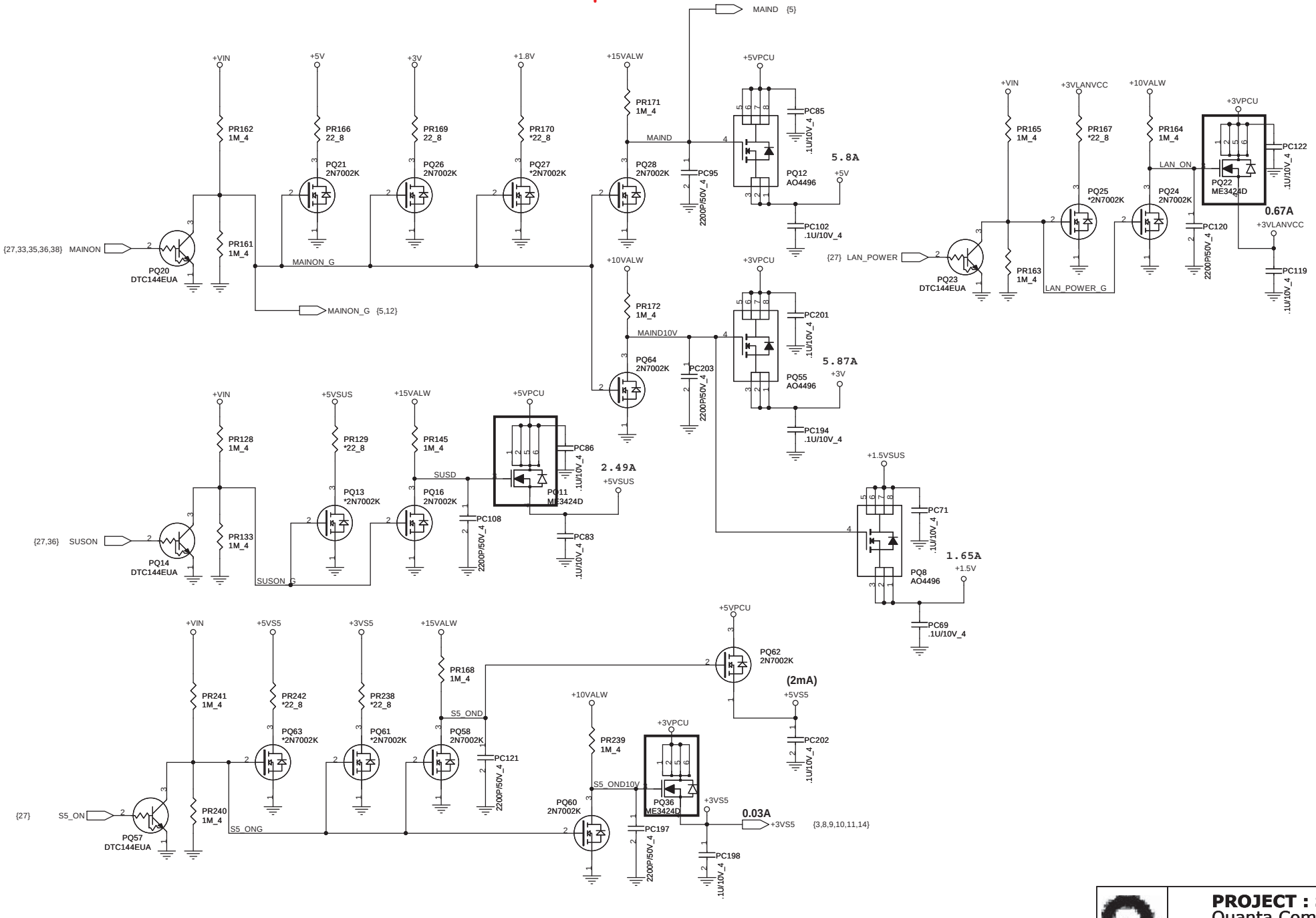
Date: Wednesday, December 02, 2009 Sheet 35 of 44



PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

Date: Wednesday, December 02, 2009 Sheet 36 of 44



PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	1A

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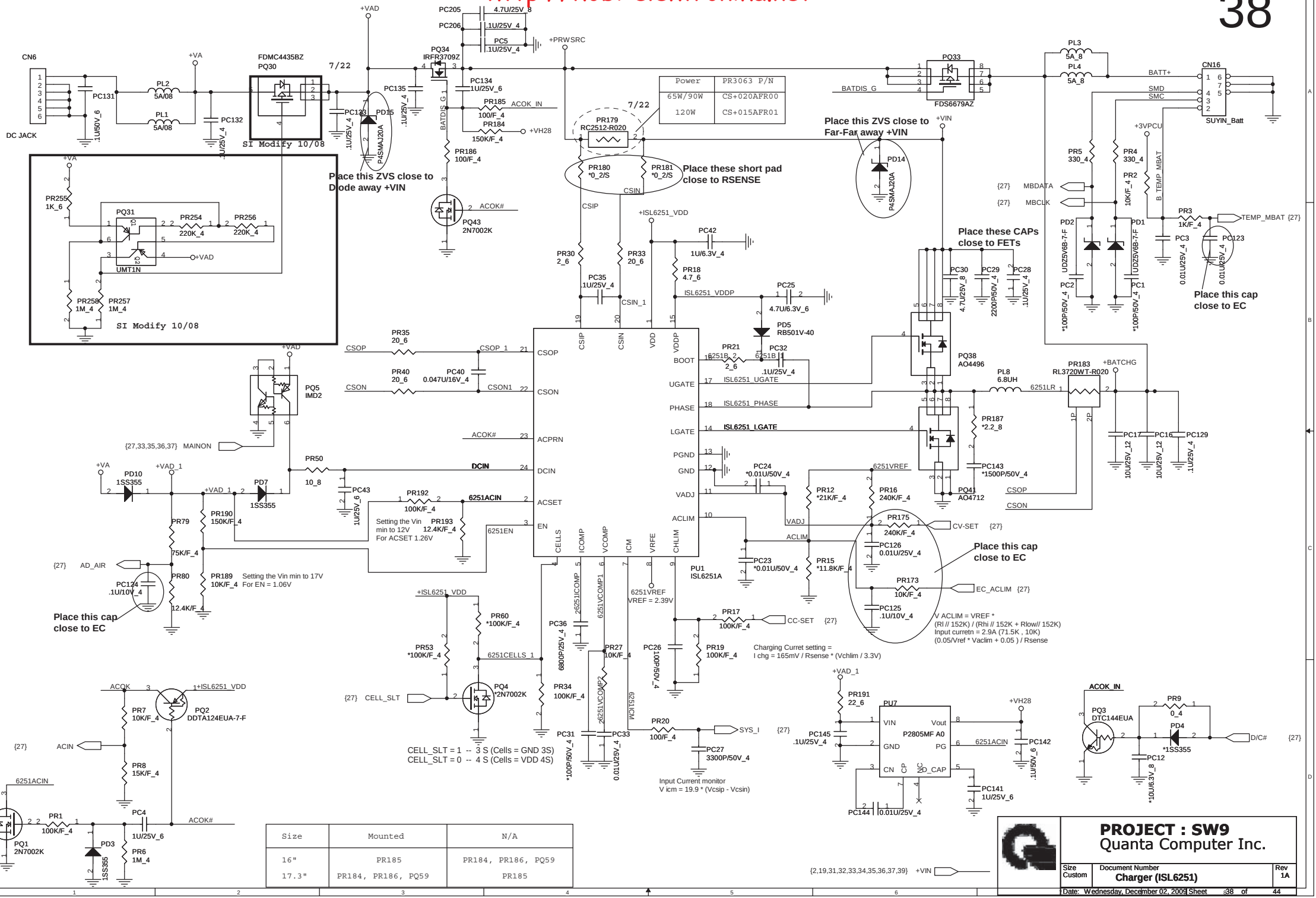

Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

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Size	Document Number	Rev
Custom	Charger (ISL6251)	1A

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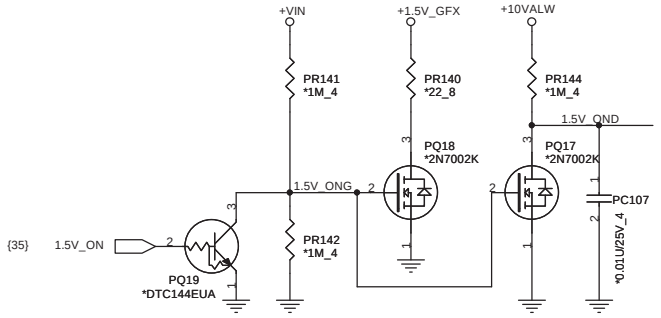
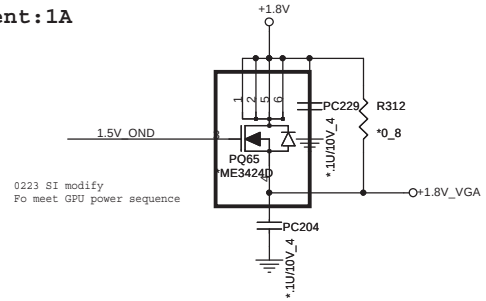
For Discrete or switchable Only

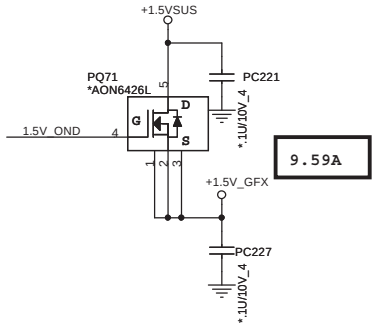


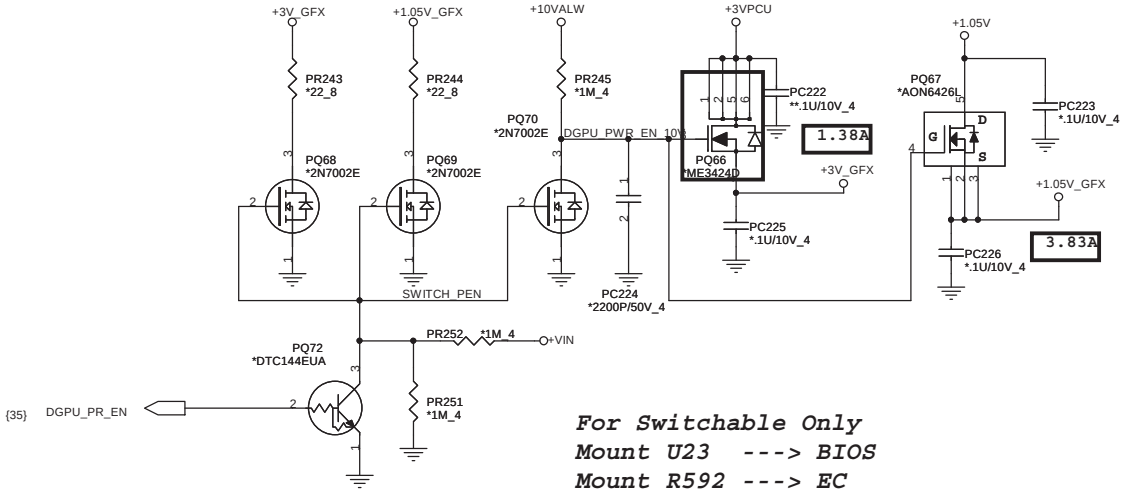
Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete or switchable Only

+1.8 Volt +/- 0.1V
Countinue current:0.3A
Peak current:1A



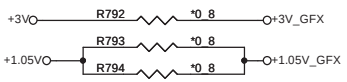




For Switchable Only
Mount U23 ---> BIOS
Mount R592 ---> EC

R51 co-lay PQ71
R53/R54 co-lay PQ68

For Discrete Only



For Hybrid DGPU Power Rails Sequence
1. +3V_GFX, +1.05V_GFX
2. +VGA_CORE -> DGPU_PG
3. 1.5V_GFX, +1.8V_GFX

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Size	Document Number	Rev
A3	Switchable Power	1A

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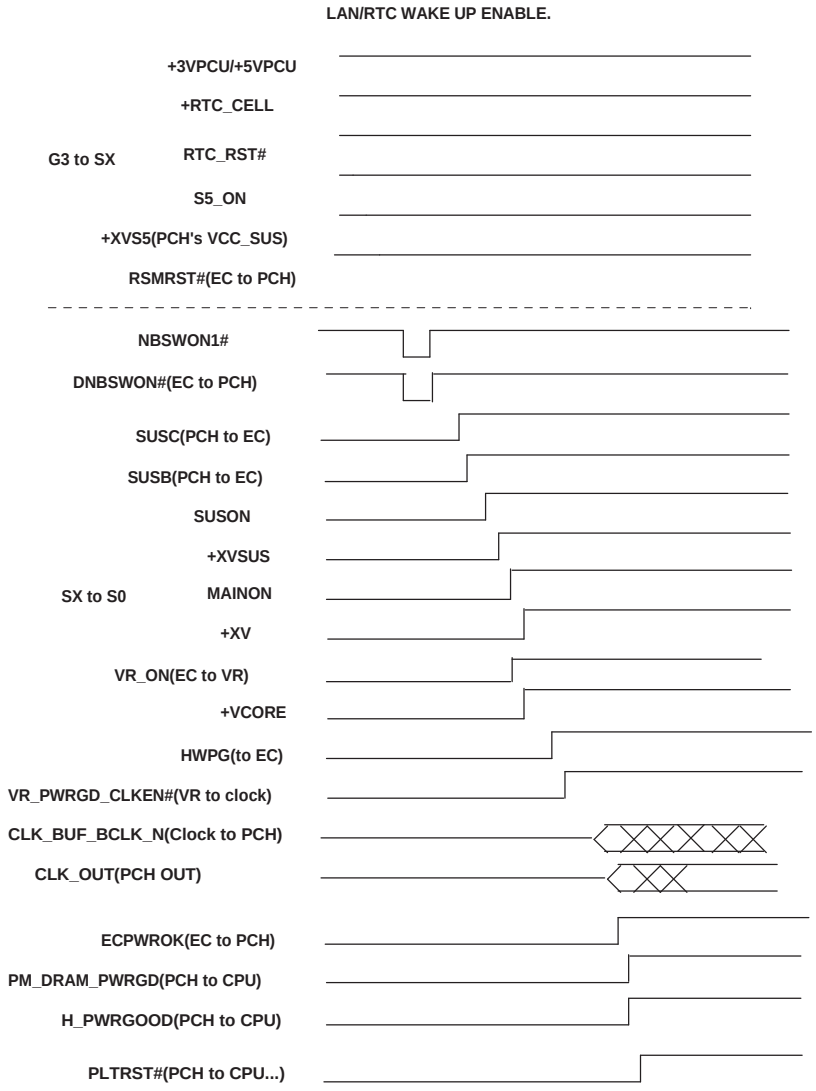
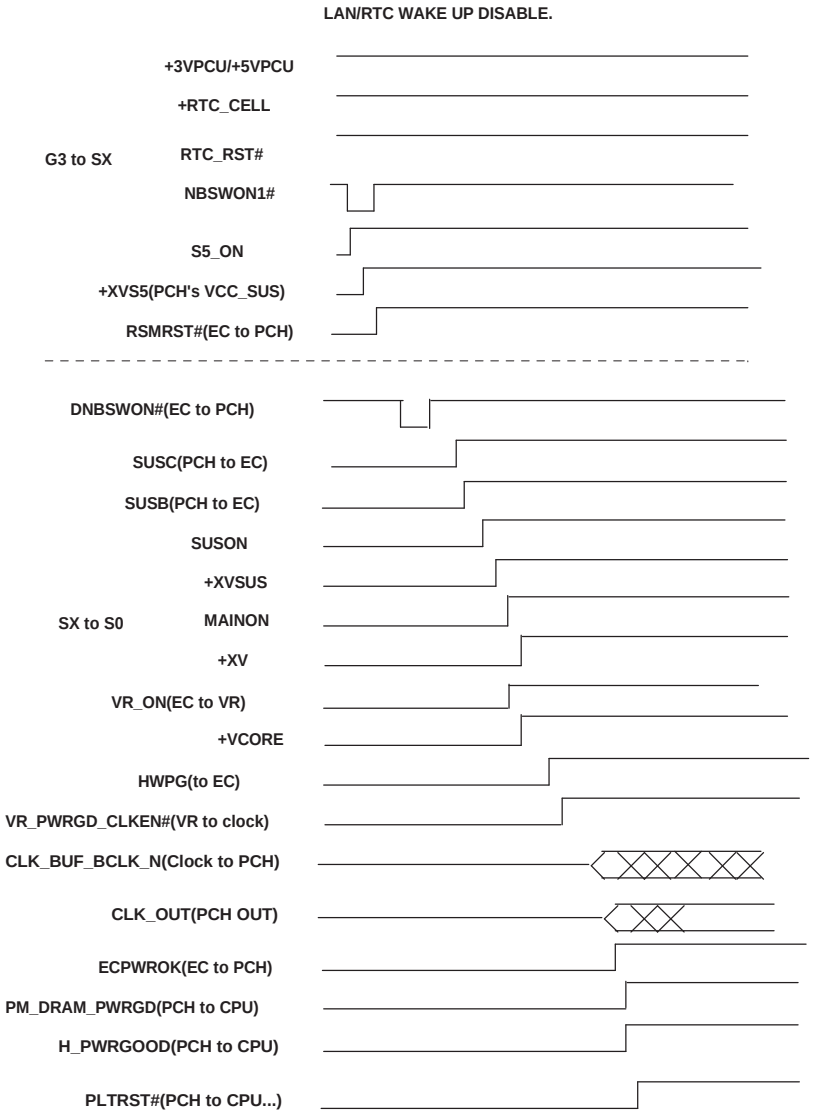
Power up sequence





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Size	Document Number	Rev
Custom	Power up sequence	1A

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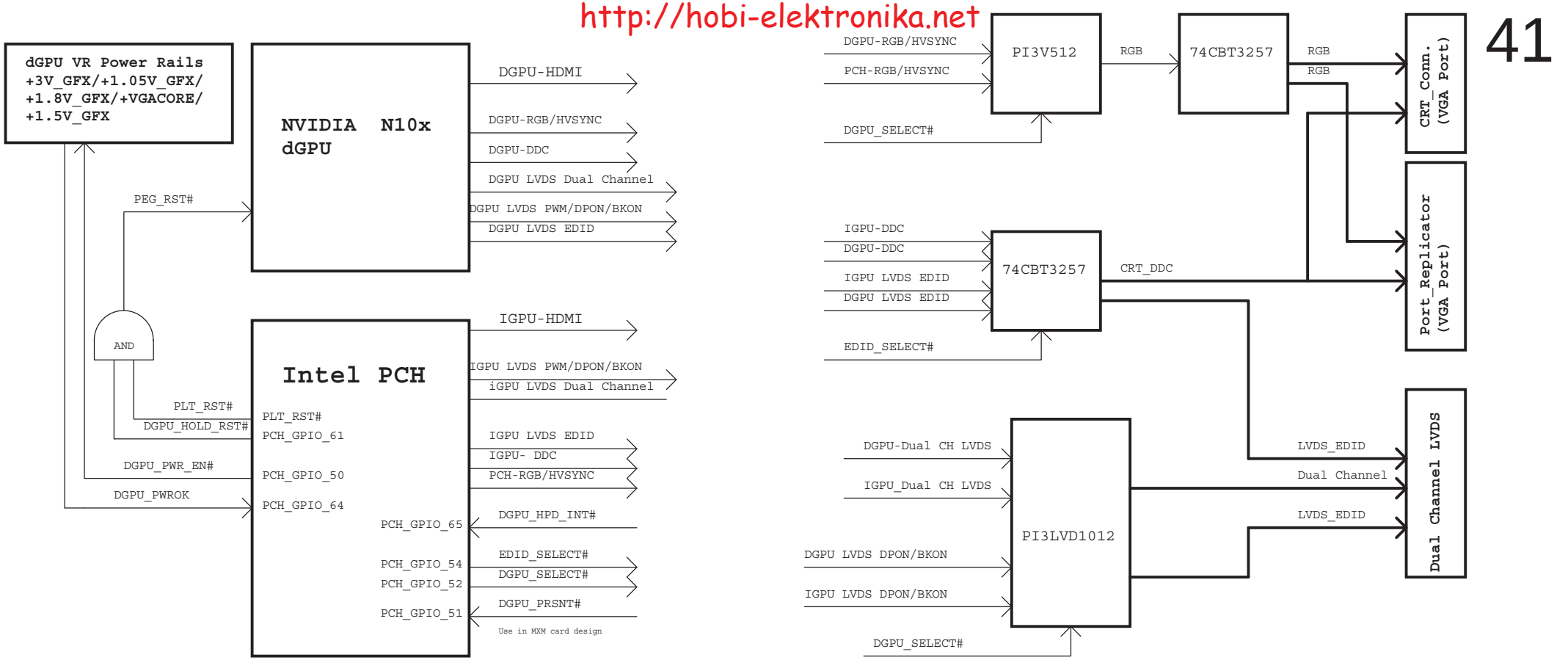

Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO61	DGPU_HOLD_RST#
PCH_GPIO50	DGPU_PWR_EN#
PCH_GPIO64	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO51	DGPU_PRSNT#
PCH_GPIO53	PWM_SELECT#

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Size	Document Number	Rev
Custom	Switch Blockdiagram	1A

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