MODEL NAME : VBW11
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WN000 LA-9984P M/B
DA40001FP00 LS-9102P USB/B
DA40001FR00 LS-9104P ODD/B
DA40001G400 LS-9105P POWER BUTTON/B
DA40001FQ00 LS-9106P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Mainstream2
UMA/DIS AMD Venus XT

2013-05-17 Rev: 1.0

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
VENUS@ : VENUS Pro,VENUS XT
VENUSXT@ : VENUS XT
VENUSPRO@ : VENUS Pro
@VENUS@ : VENUS nopop component
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

BOM config
UMA : UMA@,EMI@,ESD@,RF@,XDP@
DIS VENUS : VENUS@,VENUSXT@,DIS@,EMI@,ESD@,RF@,XDP@

ZZZ1 R1@
PCB VBW11 LA9984P/LS9102P/LS9104P/LS9105P/LS9106P
DA8000WN000

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: Cover Page
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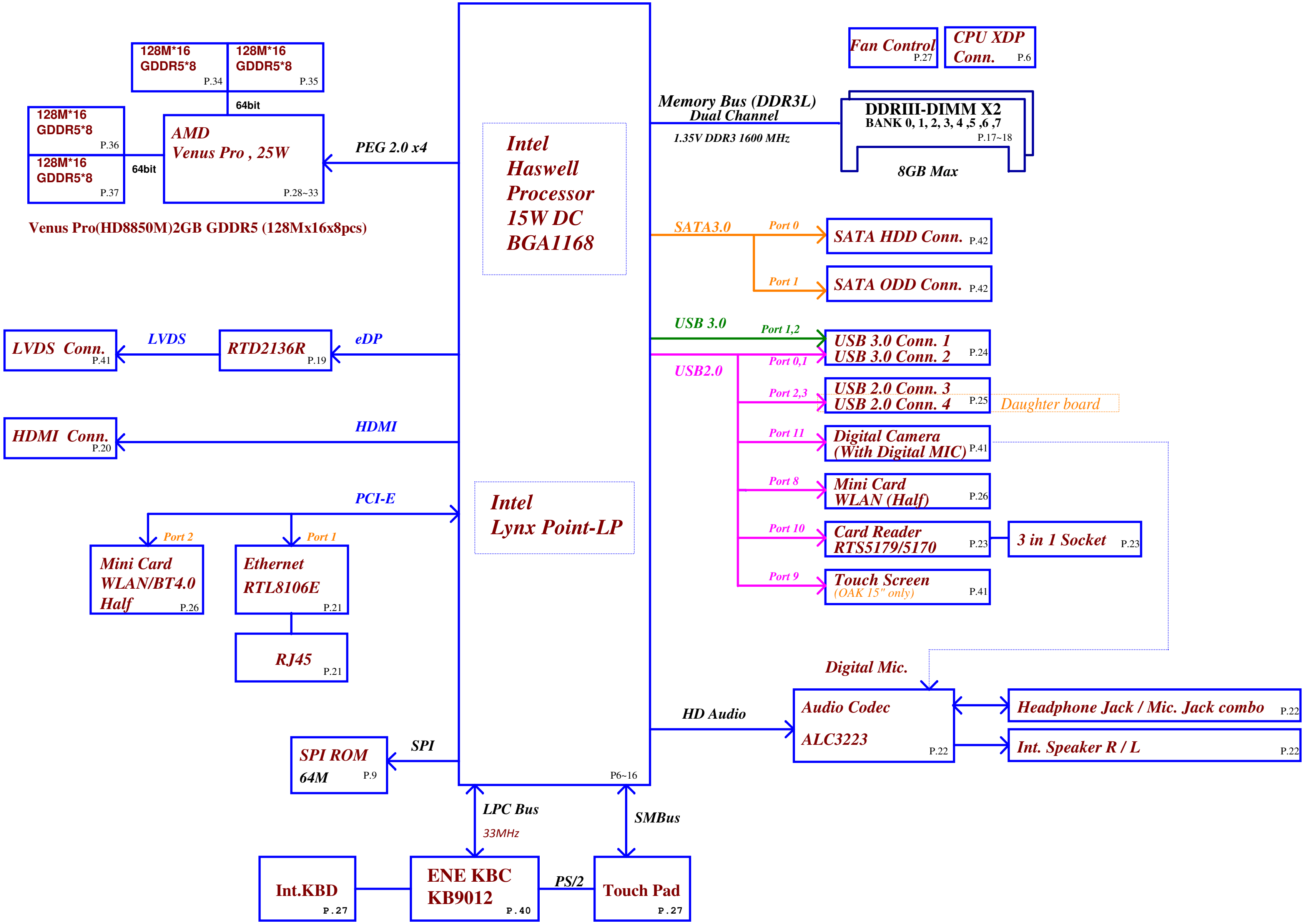
				Date: Wednesday, May 22, 2013; Sheet 1 of 57



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Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: Block diagram
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				Date: Wednesday, May 22, 2013 / Sheet 2 of 57

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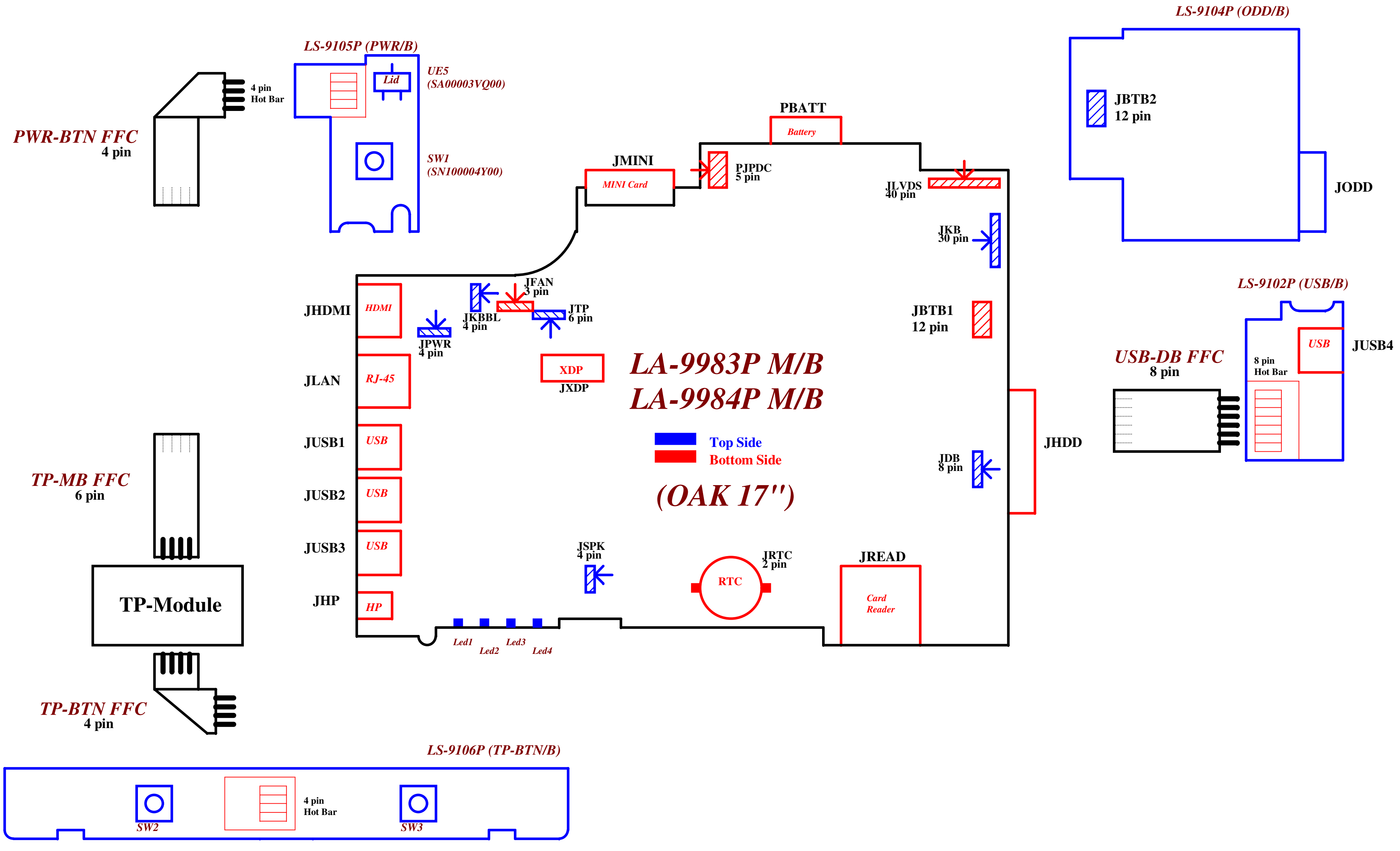
Project Code : VAW10 / VAW11
File Name : LA-9983P / LA-9984P



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Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: DB block diagram
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				Date: Wednesday, May 22, 2013 Sheet 3 of 57

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

Board ID TABLE

ID	PCB Revision UMA	Sun XT	VenusPro	VenusXT
0	SSI&A02			
1		SSI&A02		
2			SSI&A02	
3				SSI&A02
4	PT			
5		PT		
6			PT	
7				PT
8	ST			
9		ST		
10			ST	
11				ST
12	XB			
13		XB		
14			XB	
15				XB
16	A01			
17		A01		
18			A01	
19				A01

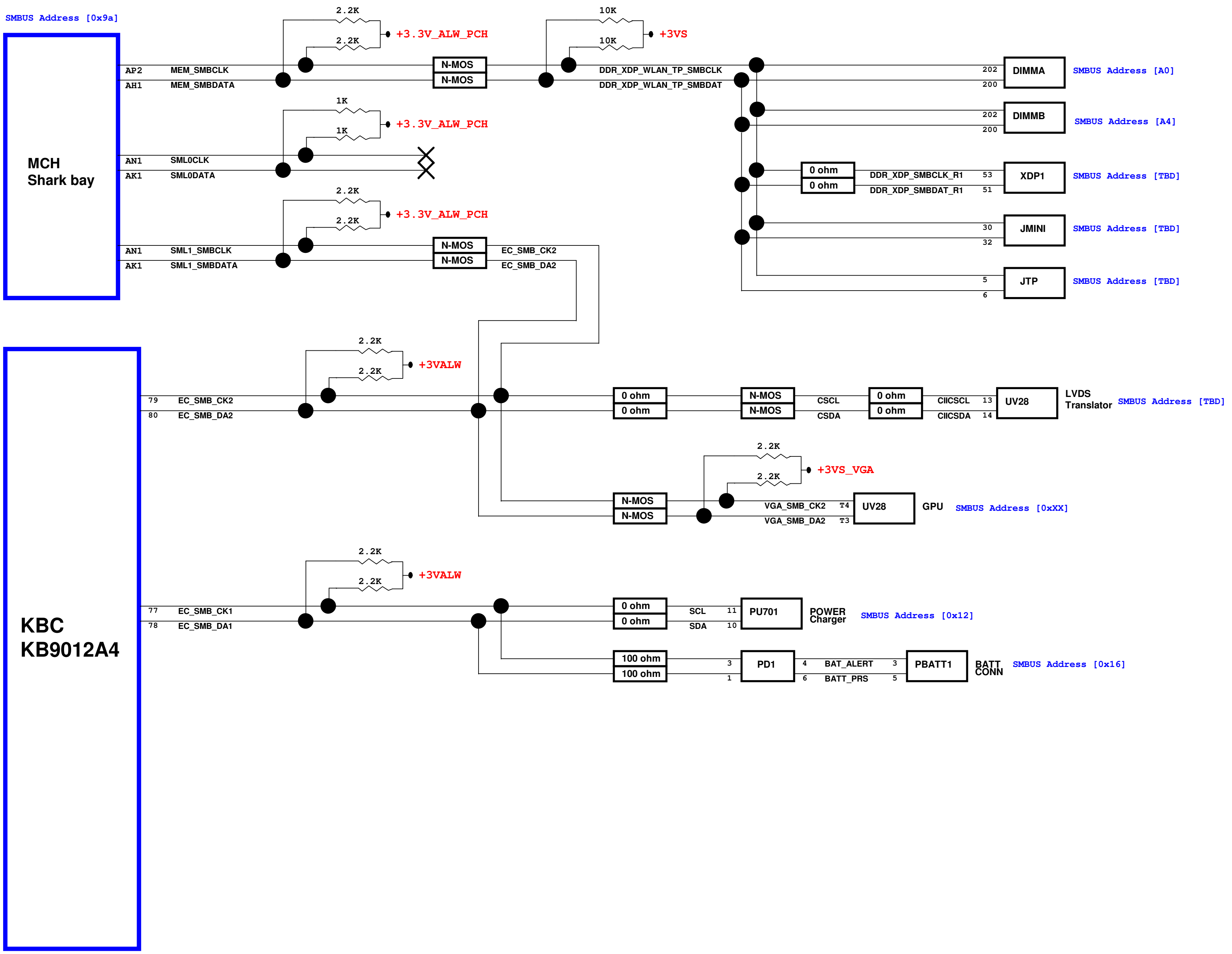
Symbol Note :

: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT		
	USB3.0	
	Port1	USB connector 2
	Port2	USB connector 1
	Port3	
	Port4	
	USB2.0	
	Port0	USB connector 2
	Port1	USB connector 1
	Port2	USB connector 3
	Port3	USB connector 4 (DB)
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (N14P)
	Lane 6	PEG (N14P)
	SATA	
	SATA0	HDD
	SATA1	ODD
	SATA2	
	SATA3	



Security Classification	Compal Secret Data		
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Title: *SMBus block diagram*

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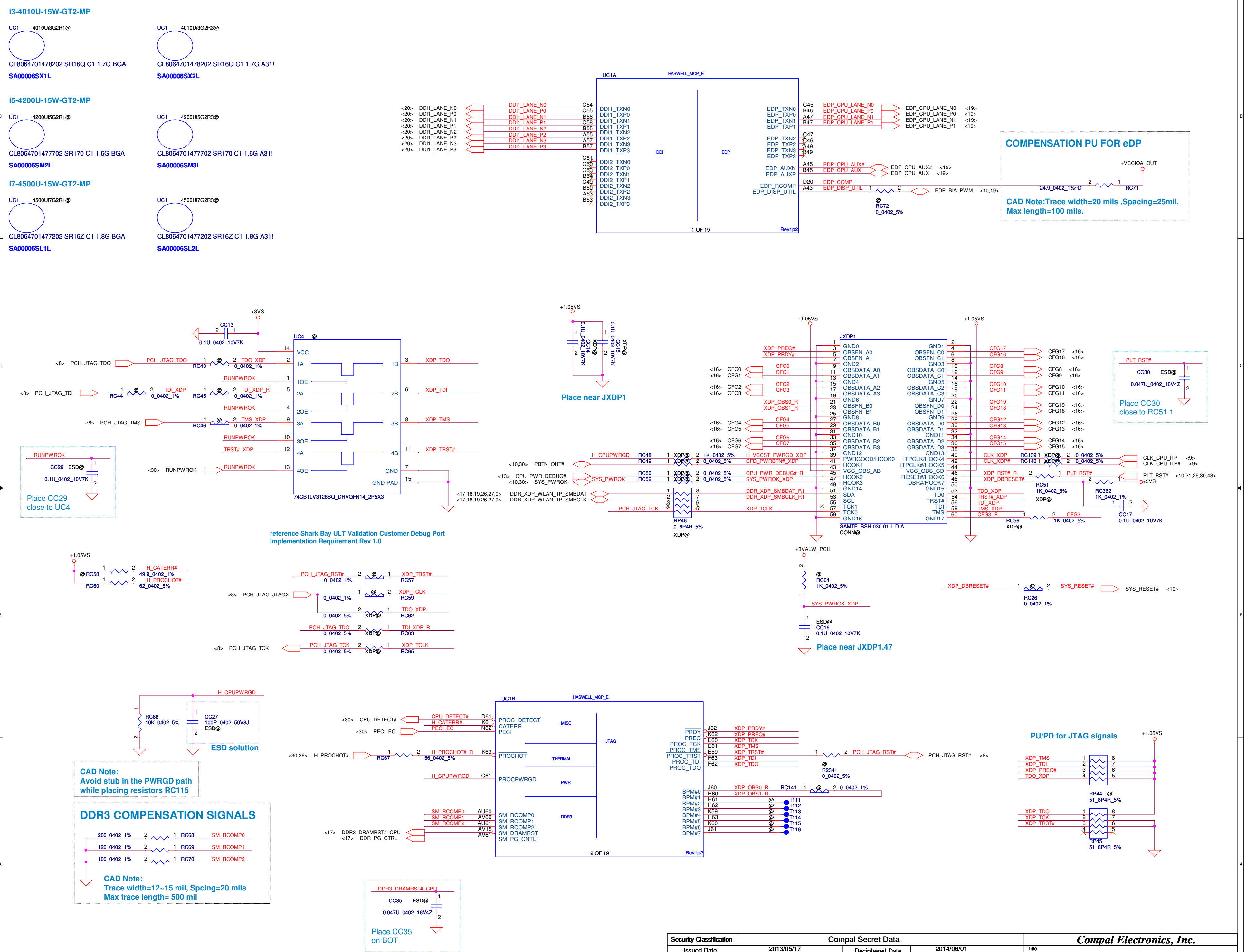
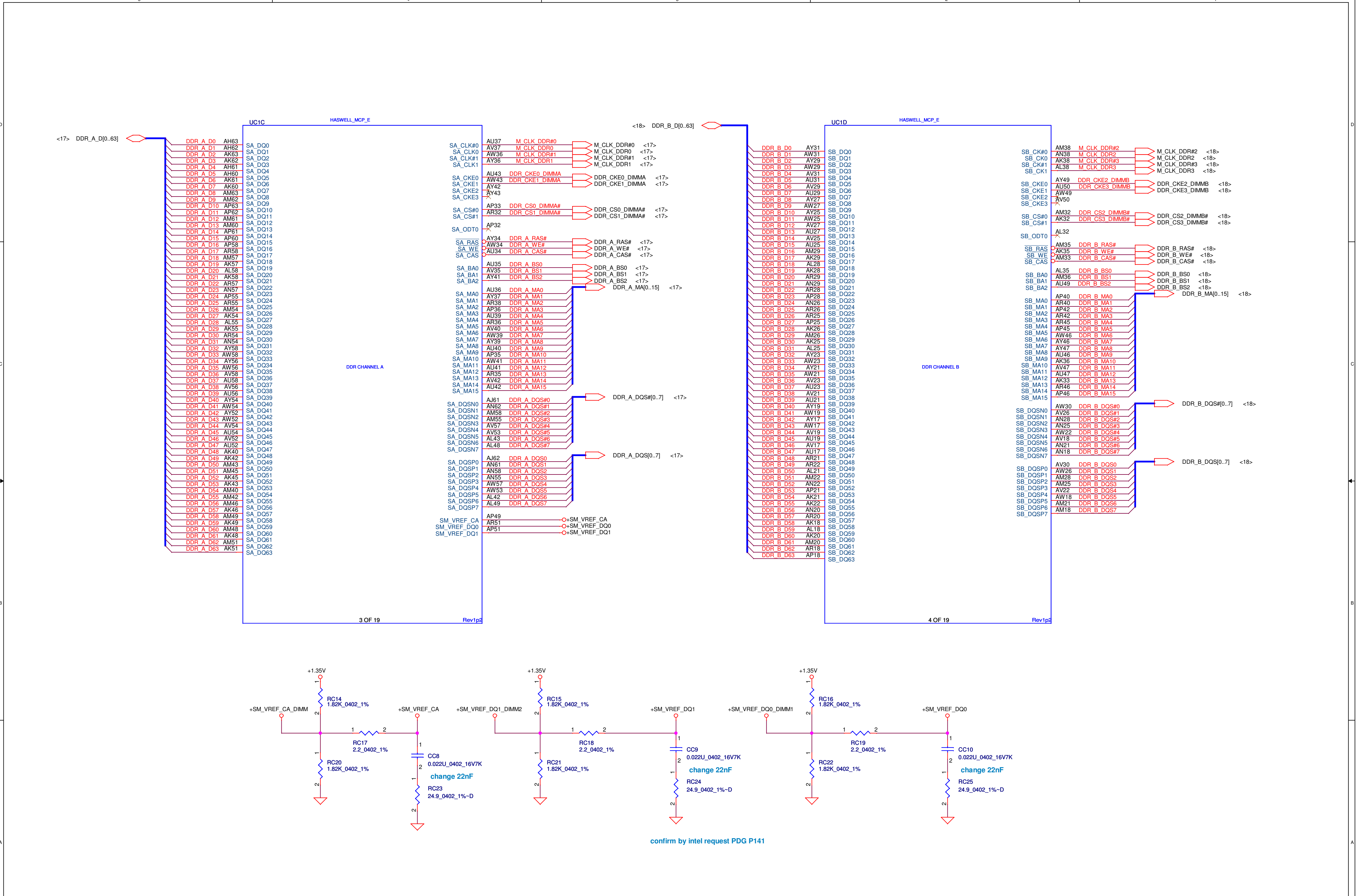
Date: Wednesday, May 22, 2013 | Sheet 5 of 57



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: MCP(1,2/19) eDP,XDP,MISC

Size | Document Number: LA-9984P | Rev 1.0

Date: Wednesday, May 22, 2013 | Sheet 6 of 55



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date 2014/06/01	Title: MCP(3,4/19) DDR3
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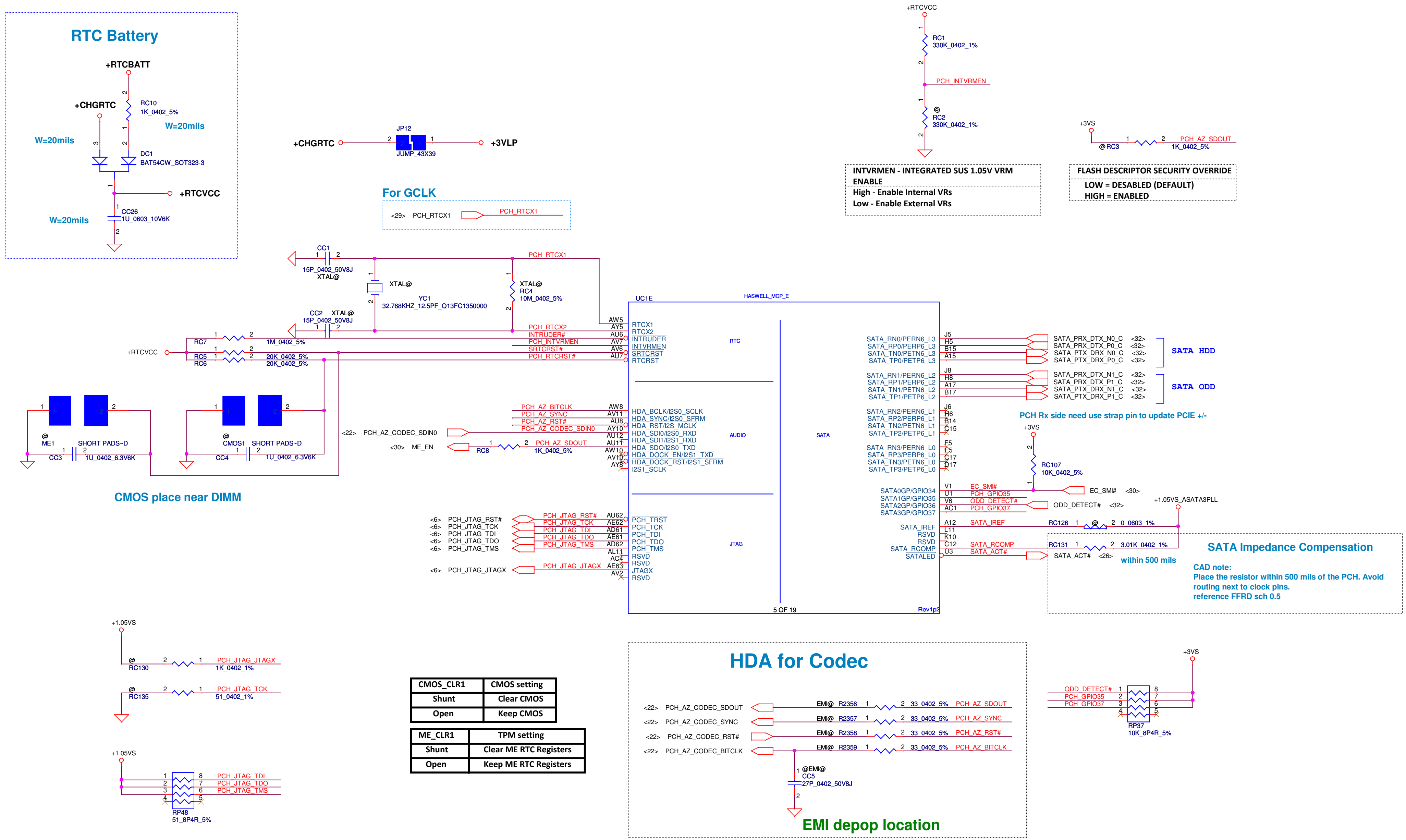
			Date: Wednesday, May 22, 2013 / Sheet 7 of 57



CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

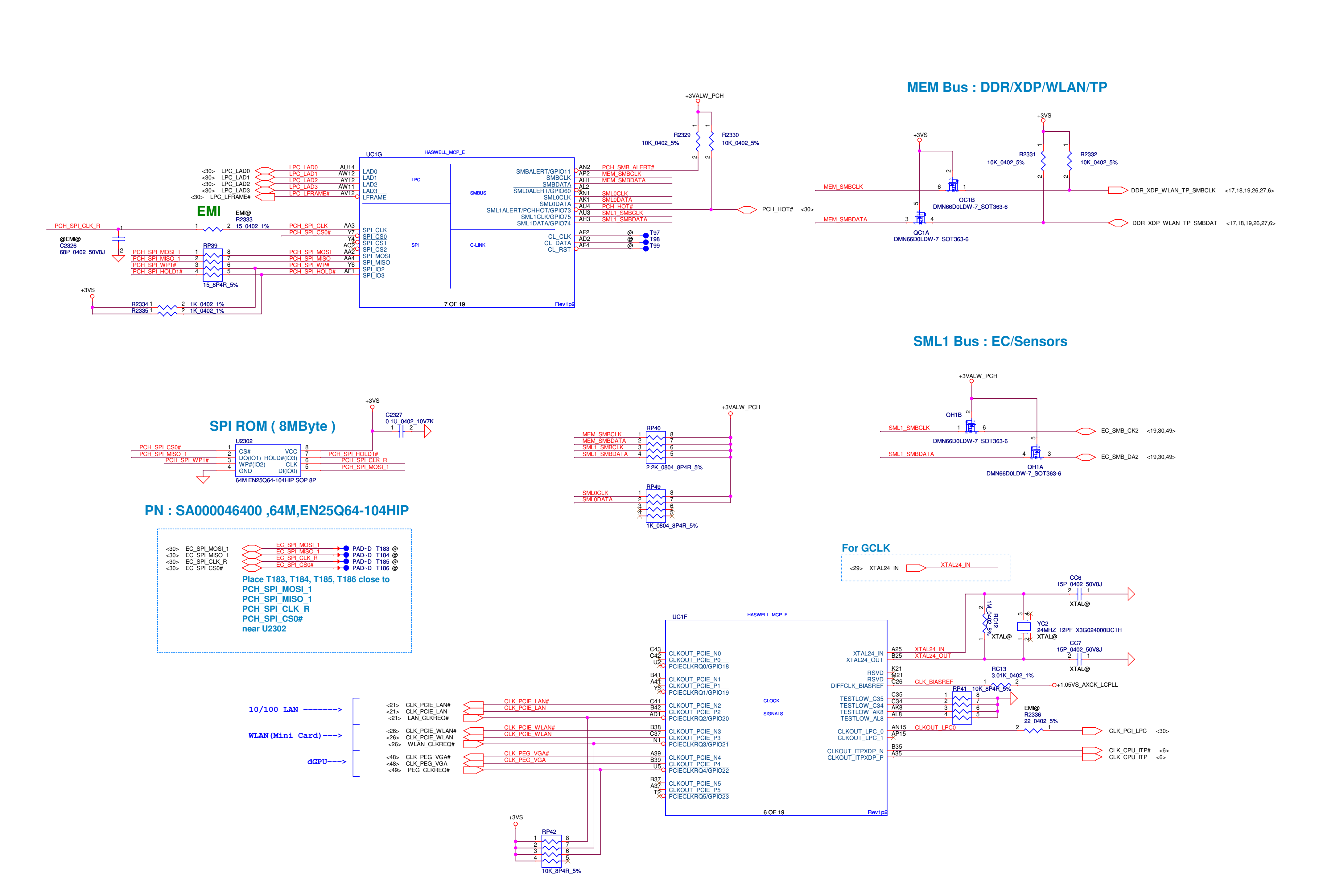
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: **MCP(5/19) RTC,SATA,HDA,JTAG**

Size | Document Number: **LA-9984P** | Rev 1.0

Date: Wednesday, May 22, 2013



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Issued Date	2013/05/17	Deciphered Date	2014/06/01

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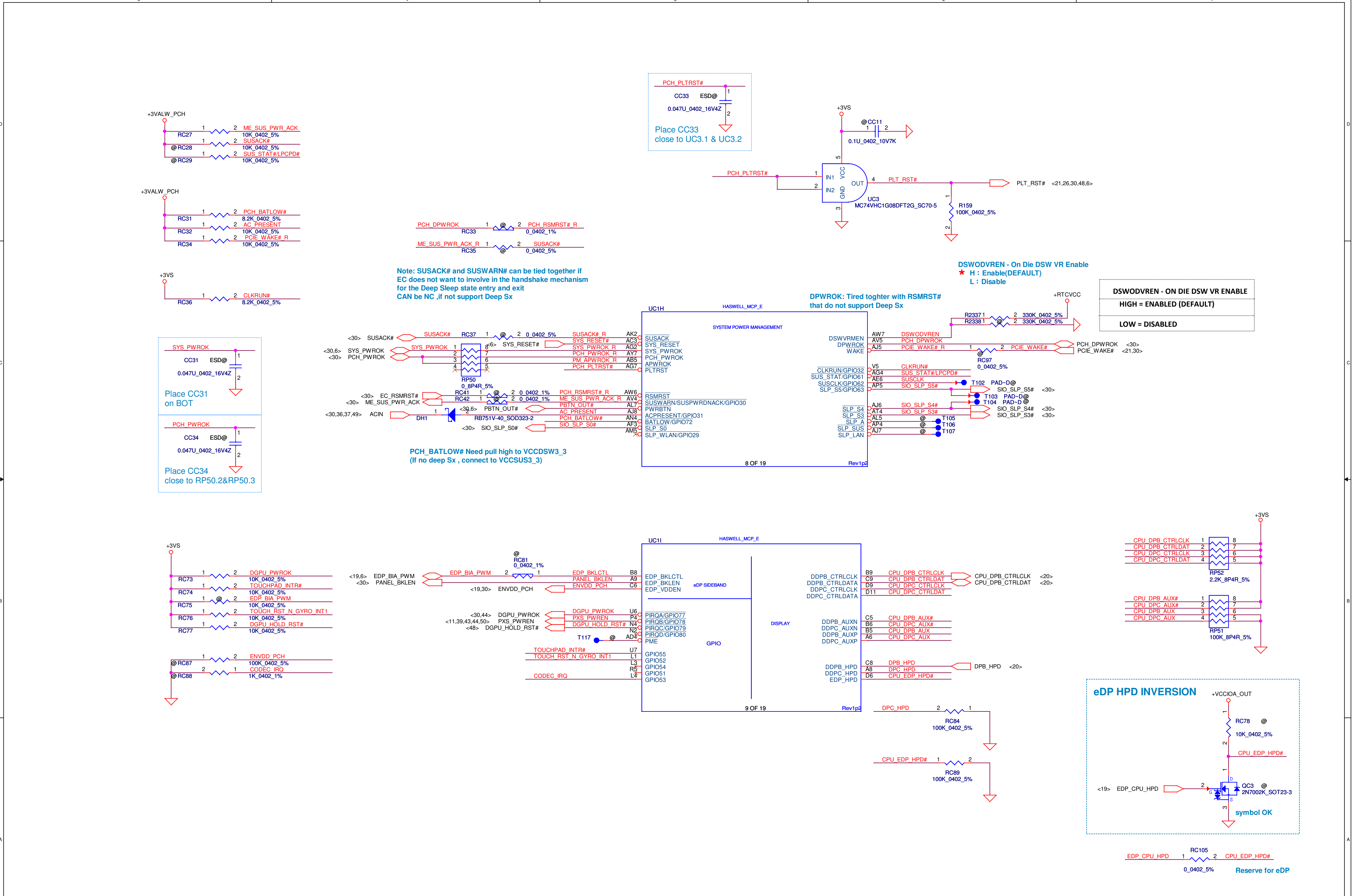
Compal Electronics, Inc.

Title: MCP(6,7/19) CLK,SMB,SPI,LPC

Size | Document Number: LA-9984P | Rev 1.0

Date: Wednesday, May 22, 2013 | Sheet 9 of 57



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: MCP(8,9/19) DDI,EDP,GPIO
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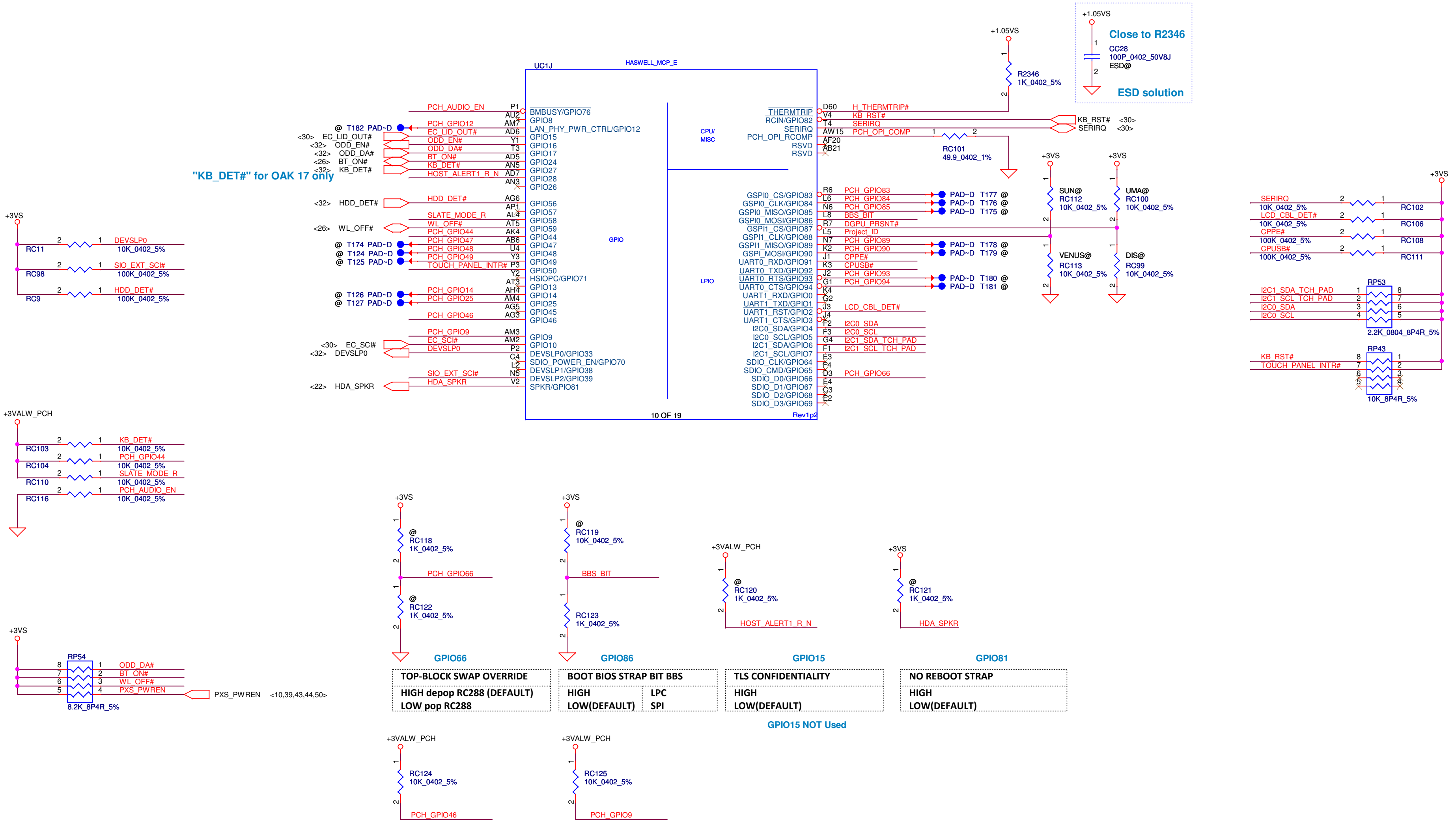
				Date: Wednesday, May 22, 2013 / Sheet 10 of 57



GPIO66

TOP-BLOCK SWAP OVERRIDE
HIGH depop RC288 (DEFAULT)
LOW pop RC288

GPIO86

BOOT BIOS STRAP BIT BBS	
HIGH	LPC
LOW(DEFAULT)	SPI

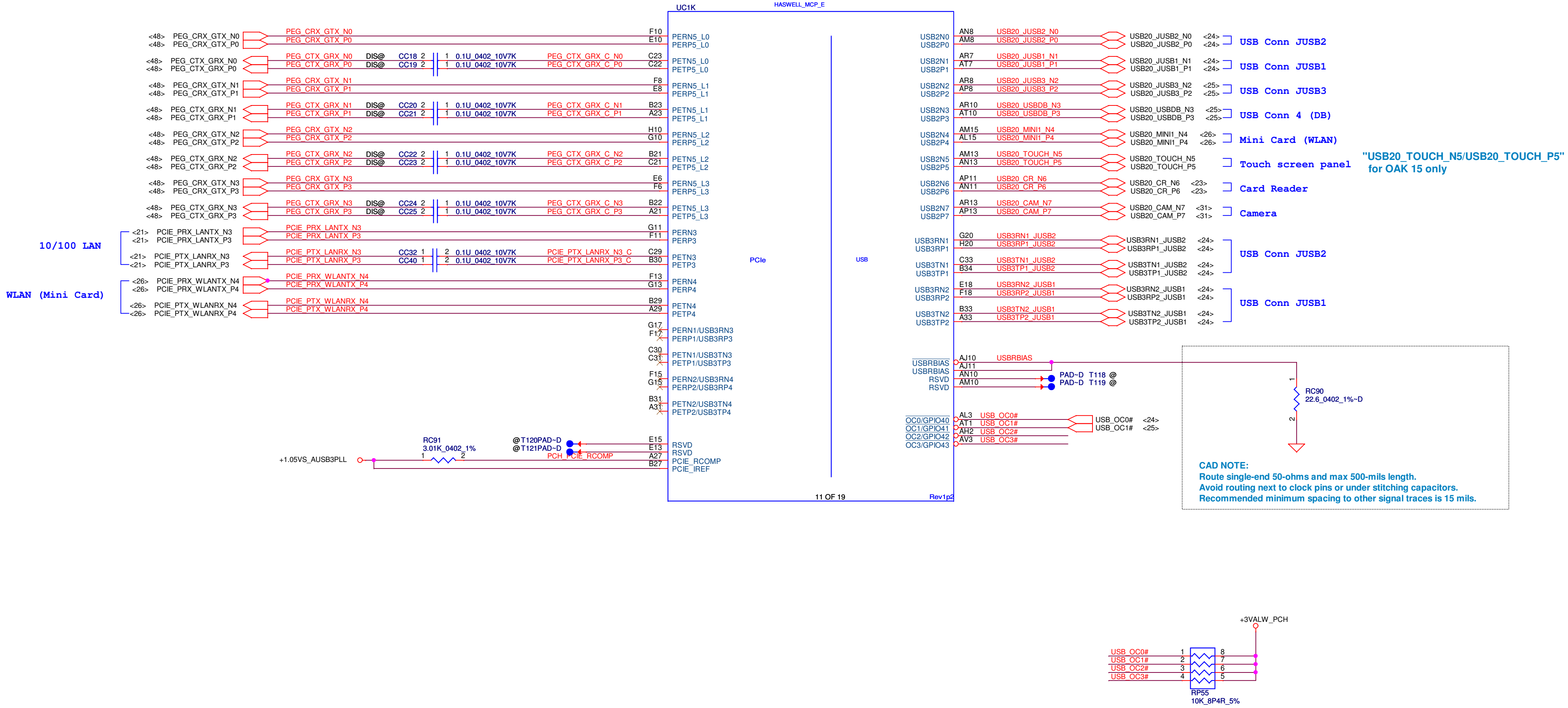
GPIO15

TLS CONFIDENTIALITY
HIGH
LOW(DEFAULT)

GPIO15 NOT Used

GPIO81

NO REBOOT STRAP
HIGH
LOW(DEFAULT)



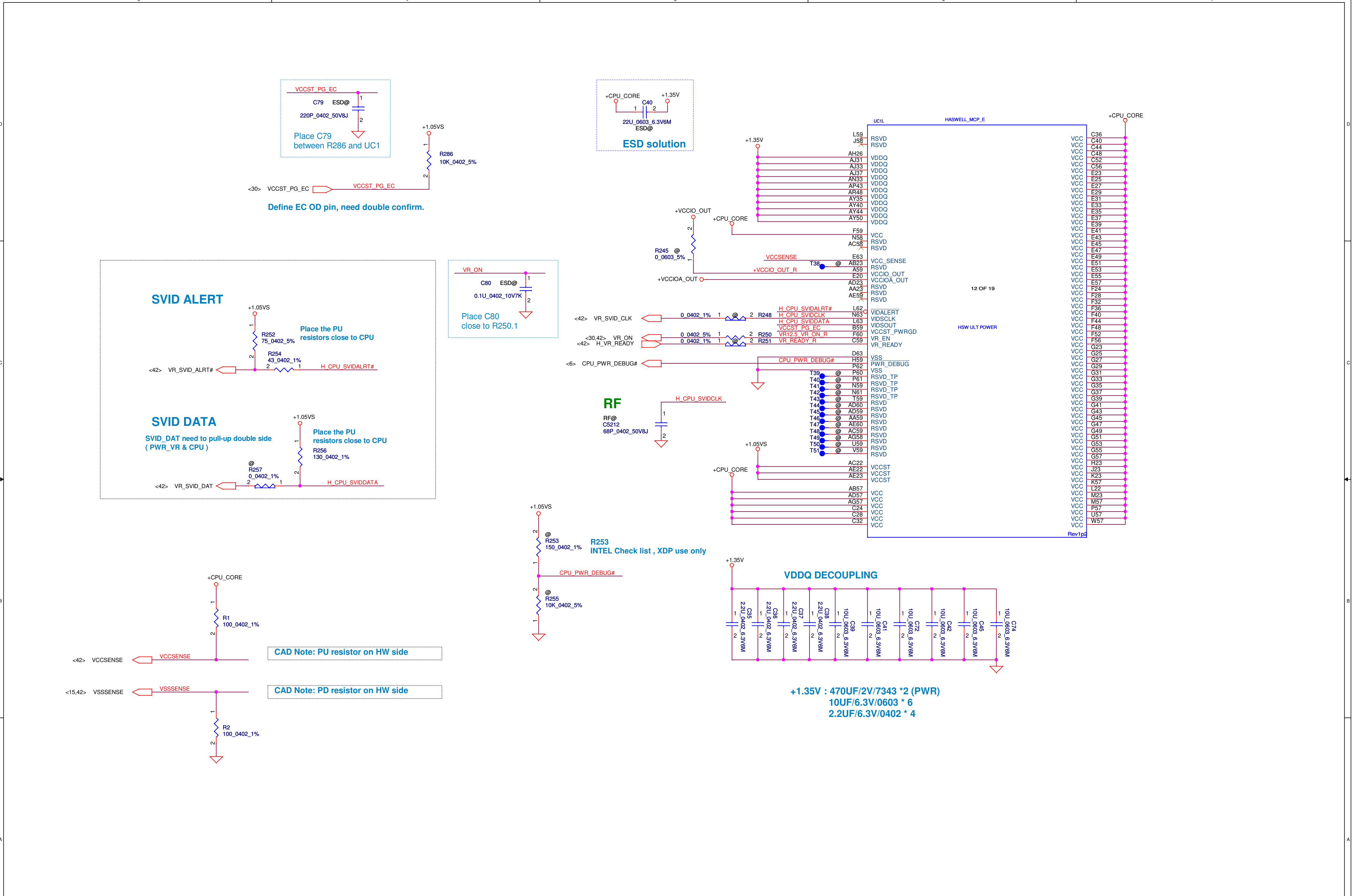
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: **MCP(11/19) PCIE,USB**

Size | Document Number: **LA-9984P** | Rev 1.0

Date: Wednesday, May 22, 2013 | Sheet 12 of 57



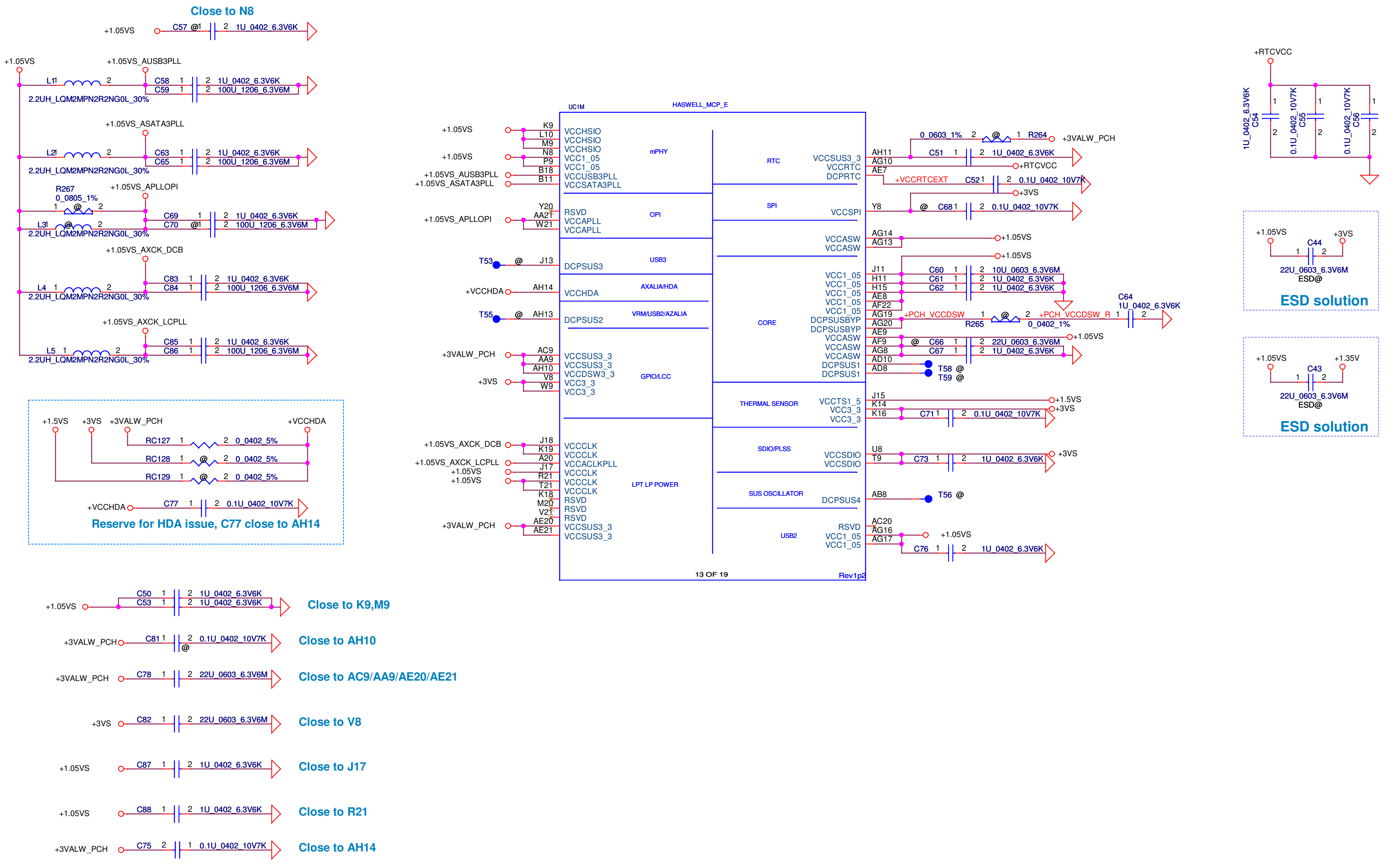
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: *MCP(12/19) Power*

Size	Document Number	Rev
	LA-9984P	1.0

Date: Wednesday, May 22, 2013 | Sheet 13 of 57



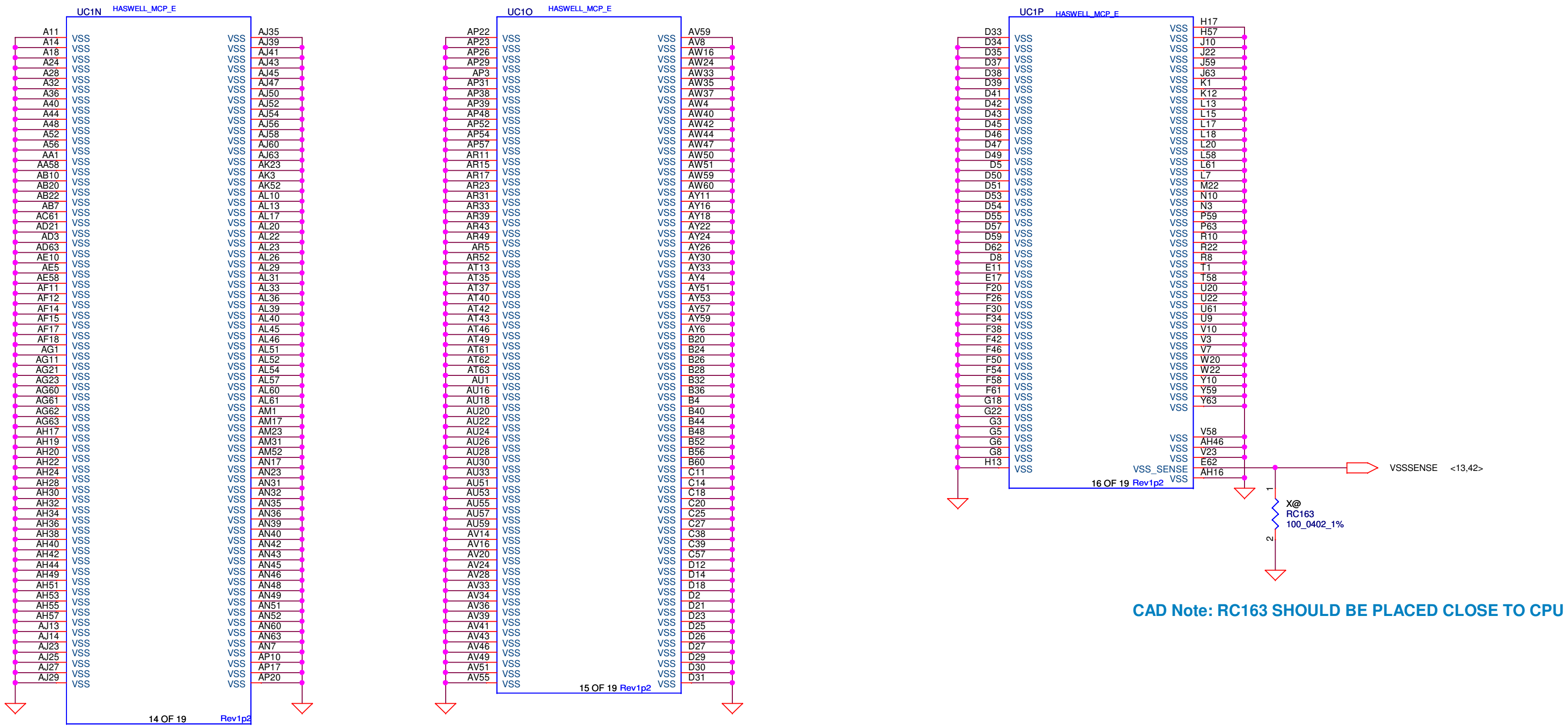
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: **MCP(13/19) Power**

Size | Document Number: **LA-9984P** | Rev: 1.0

Date: Wednesday, May 22, 2013 |



CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

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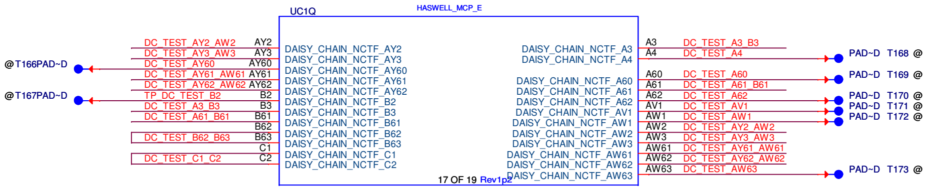
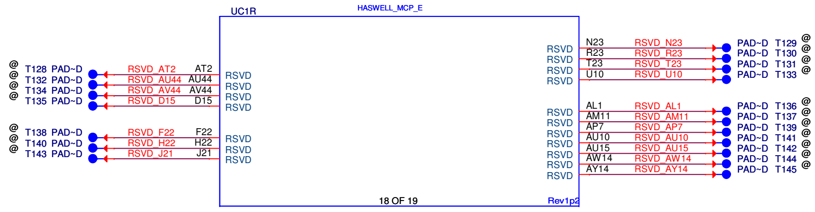
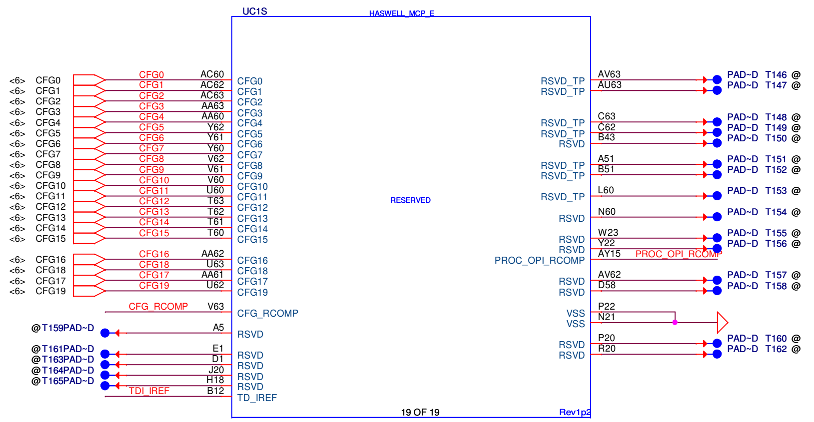
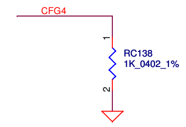
				Date: Wednesday, May 22, 2013 Sheet 15 of 57



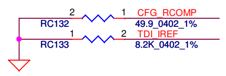




CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port



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Issued Date	2013/05/17	Deciphered Date 2014/06/01	Title: MCP(17,18,19/19) CFG,RSVD
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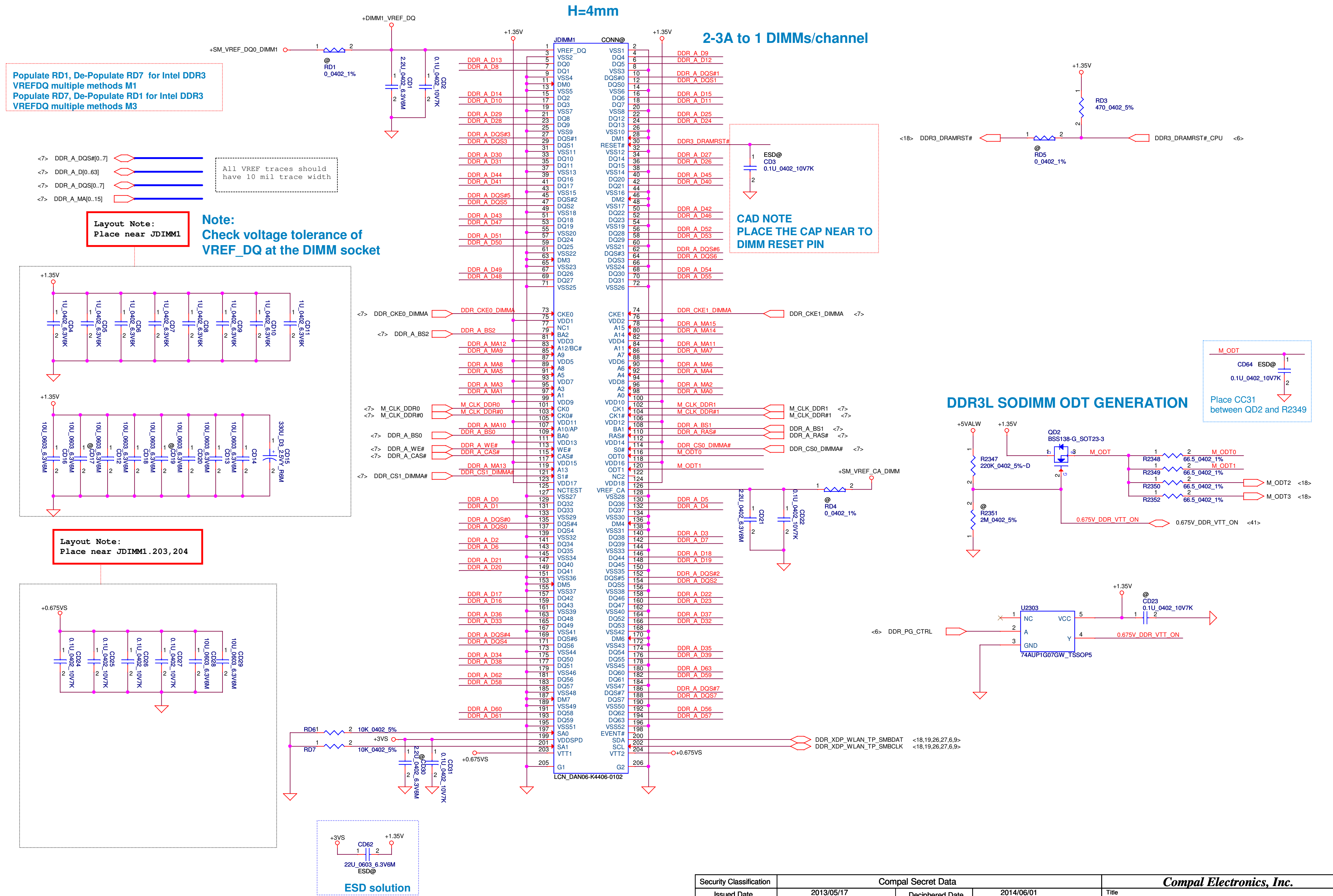
			Date: Wednesday, May 22, 2013 Sheet 16 of 57



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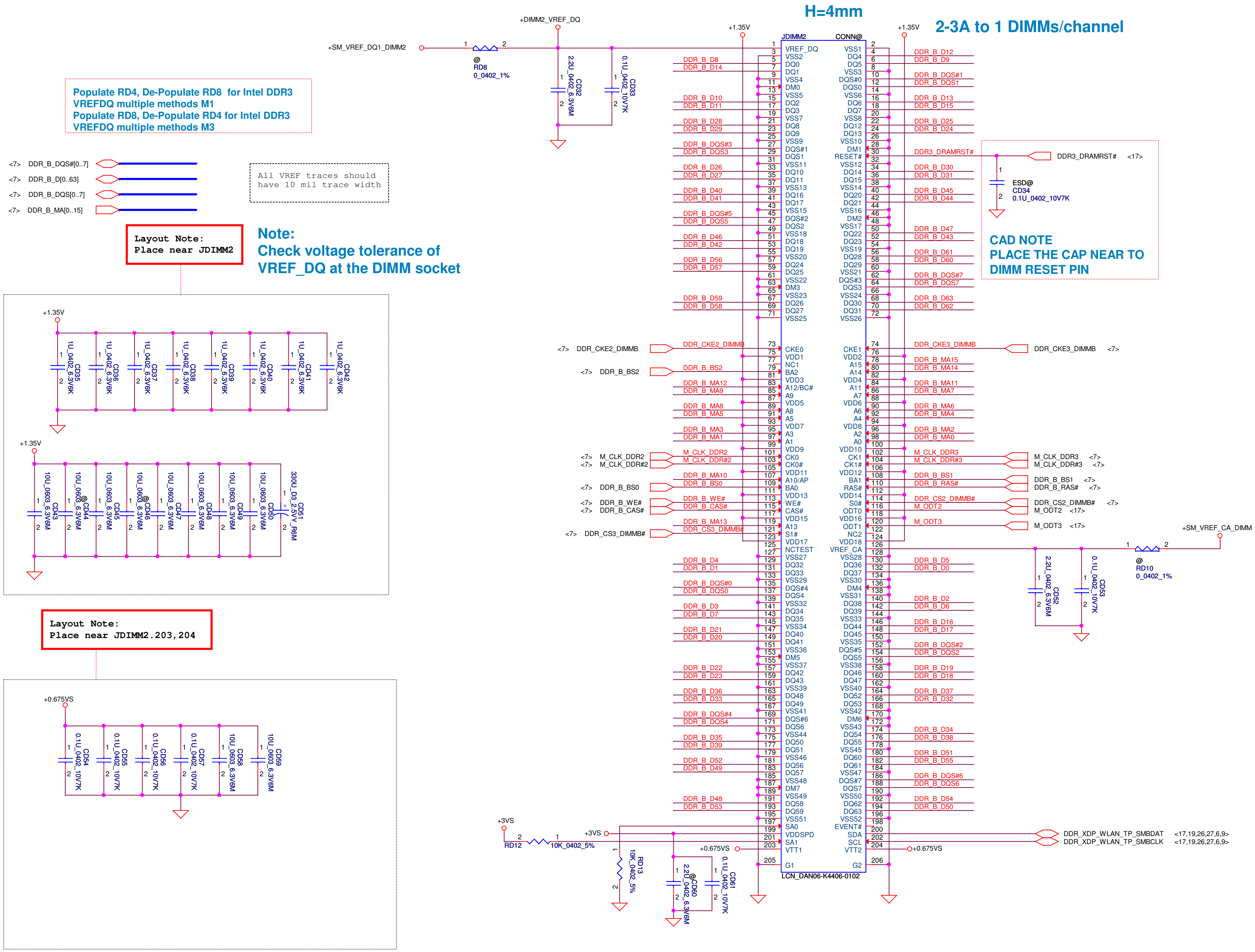
			Date: Wednesday, May 22, 2013 Sheet 17 of 57



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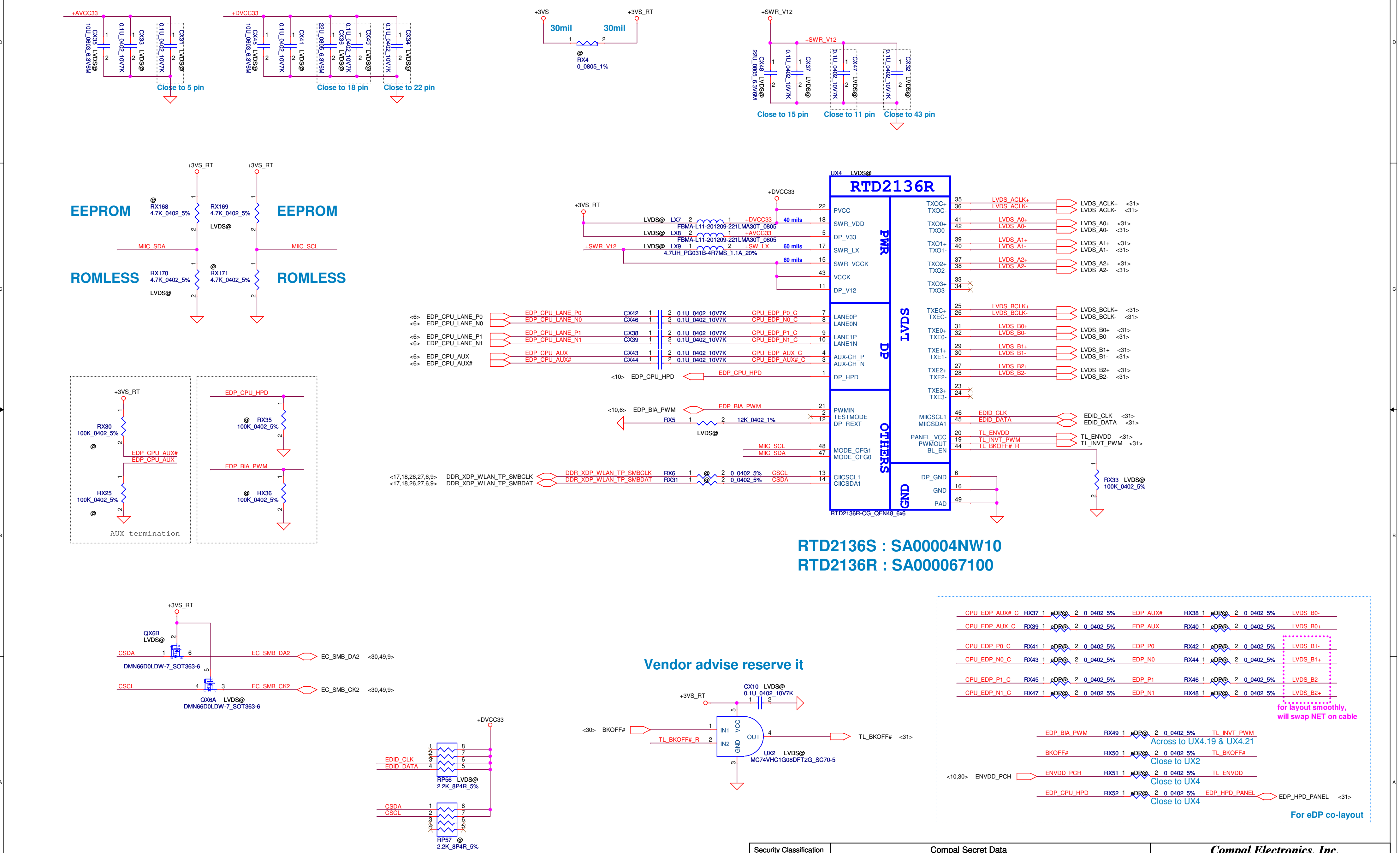
Compal Electronics, Inc.

Title: DDRIII DIMMB

Size | Document Number: LA-9984P | Rev 1.0

Date: Wednesday, May 22, 2013 | Sheet 18 of 57



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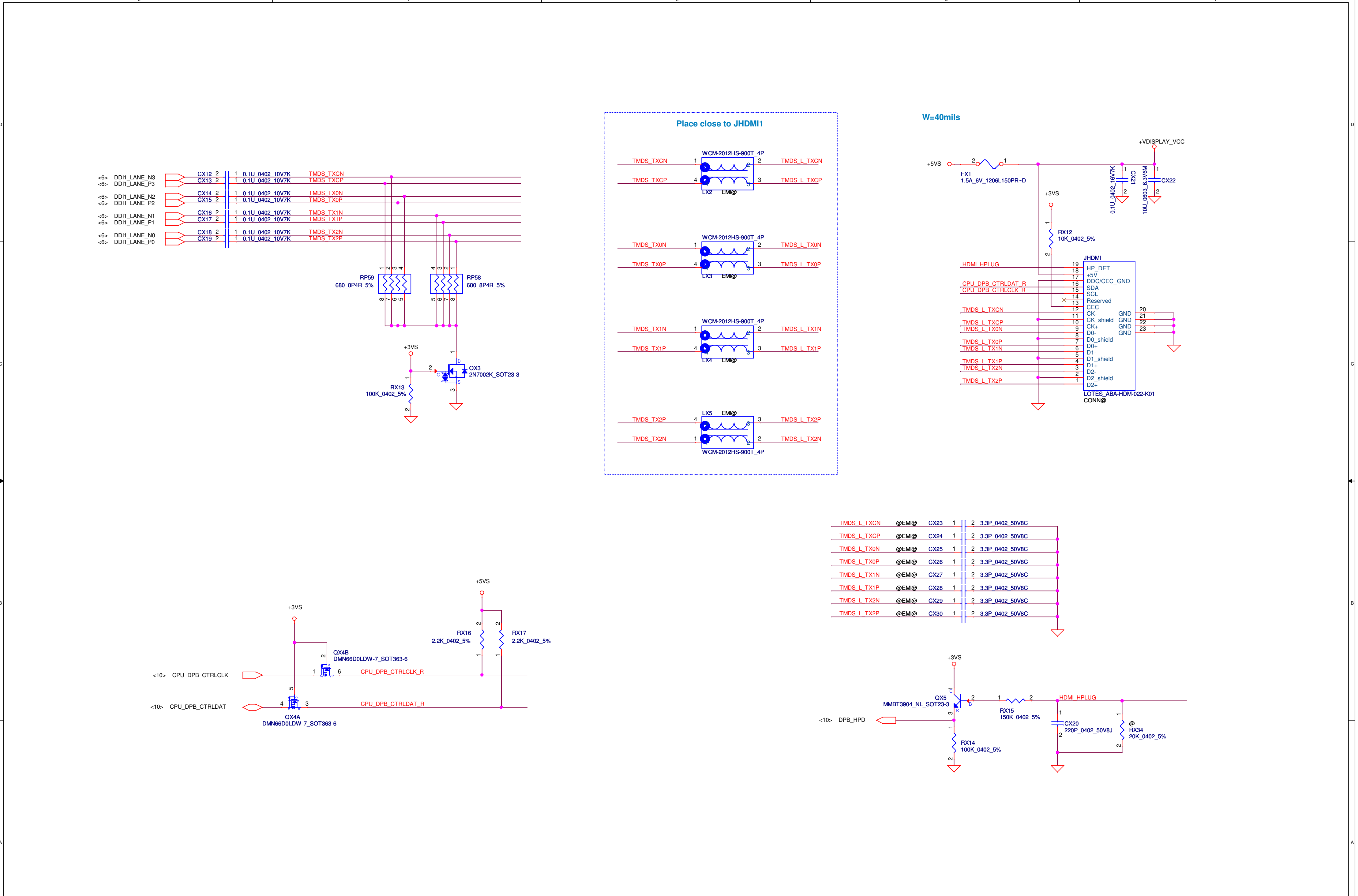
			Date: Wednesday, May 22, 2013 / Sheet 19 of 57



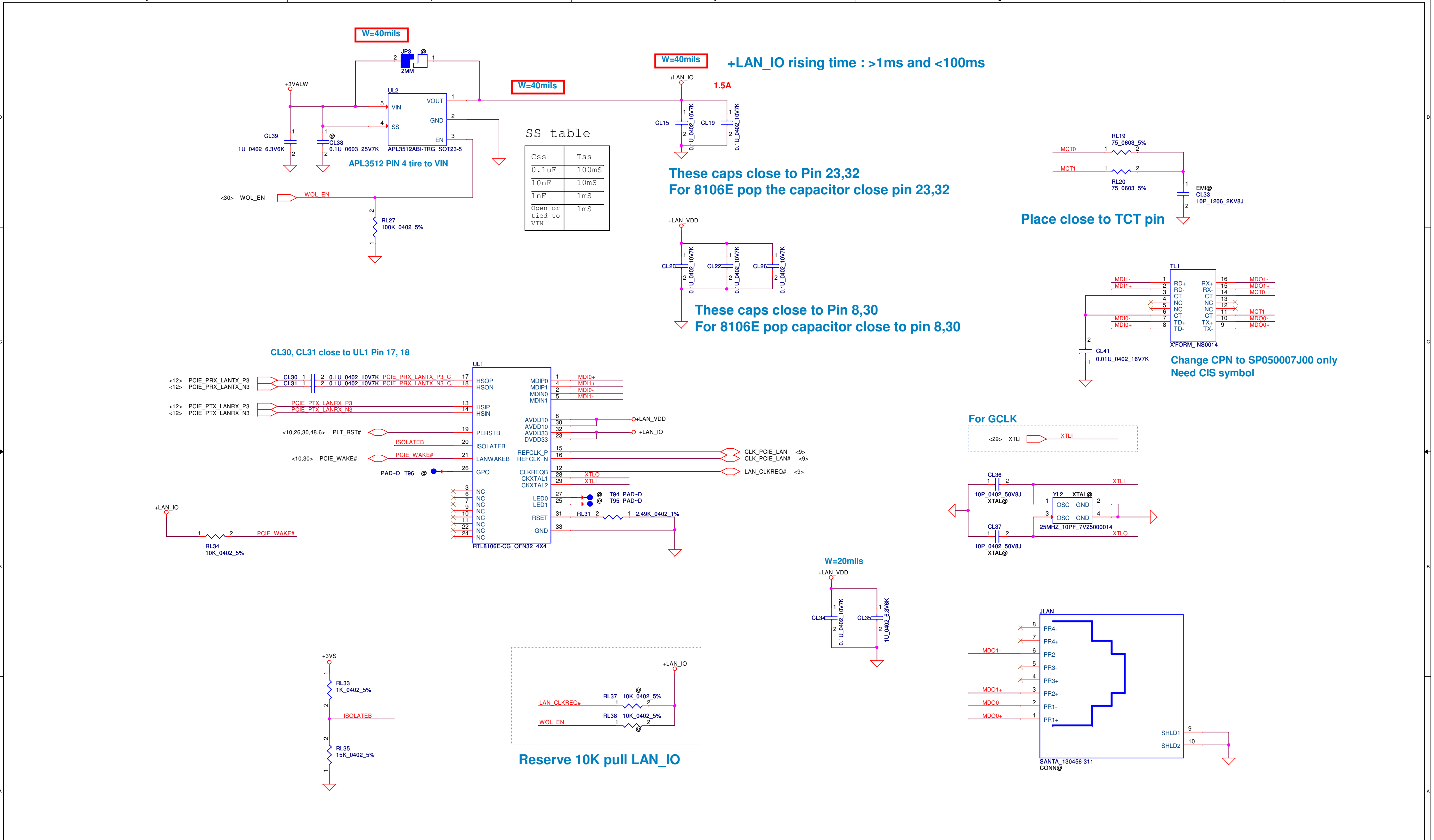
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: HDMI

Size | Document Number: LA-9984P | Rev 1.0

Date: Wednesday, May 22, 2013 |



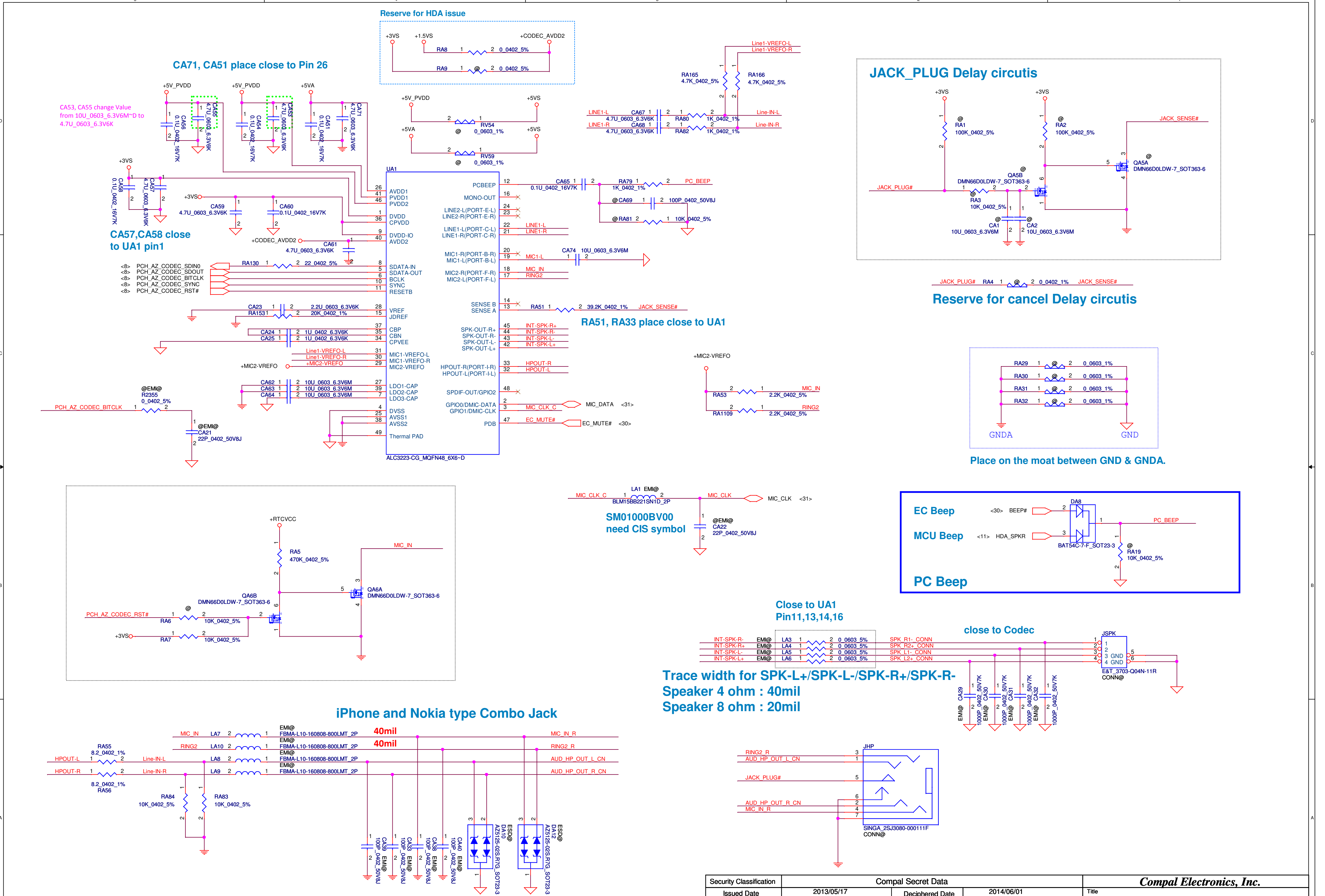
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: **LAN RTL8106E**

Size | Document Number: **LA-9984P** | Rev 1.0



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date 2014/06/01	Title: Audio Codec ALC3223
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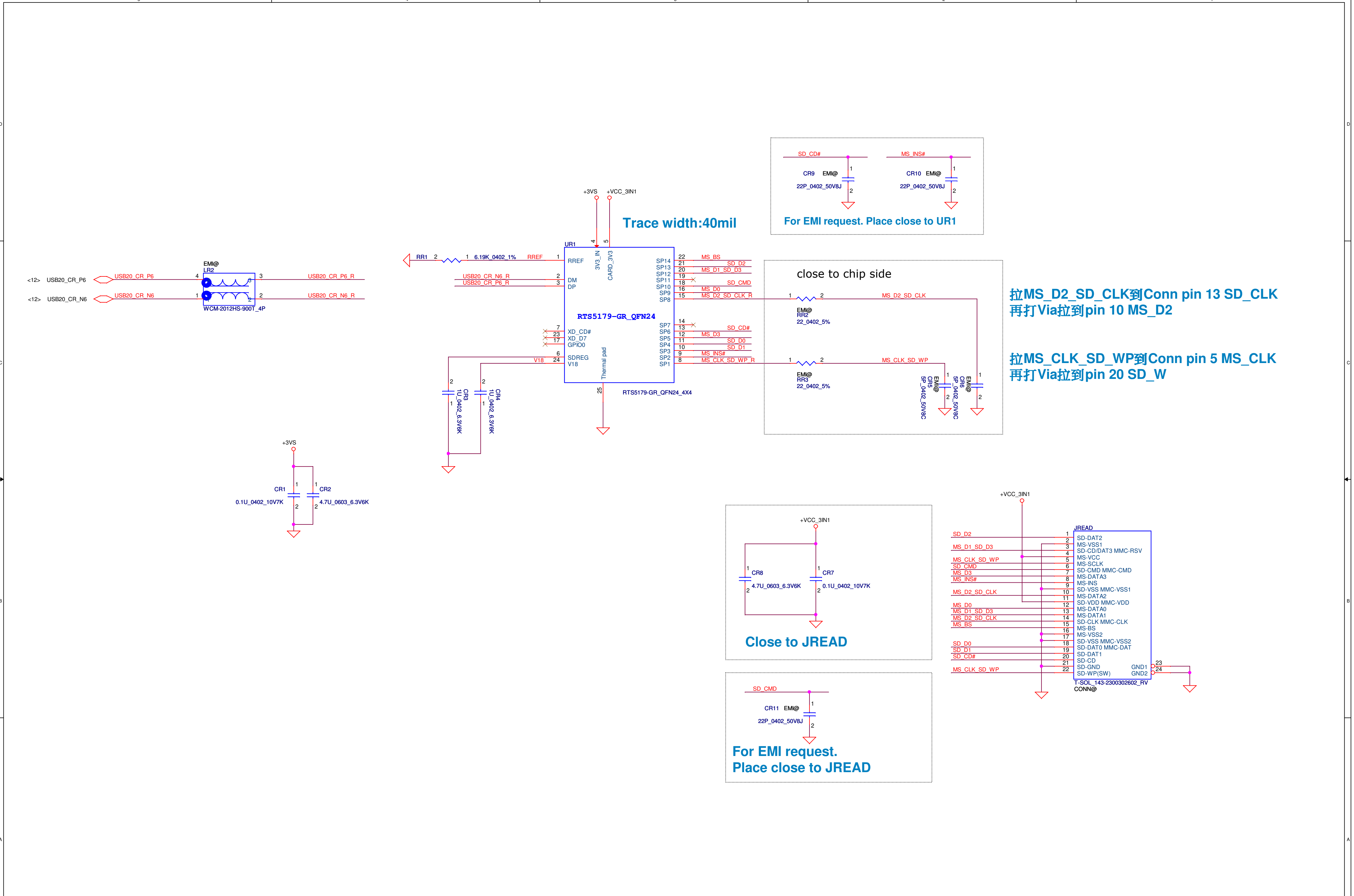
			Date: Wednesday, May 22, 2013 / Sheet 22 of 57



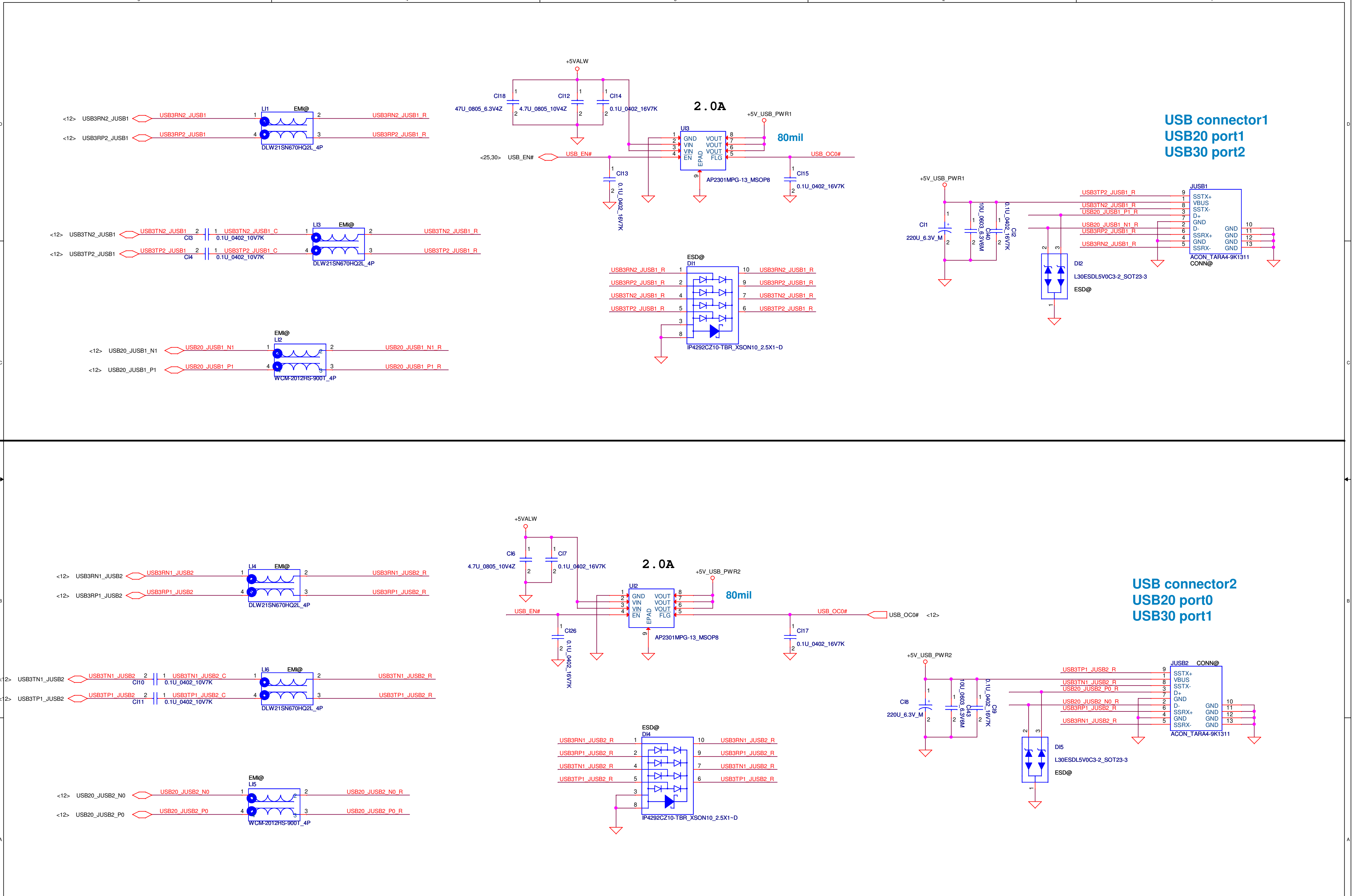
Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

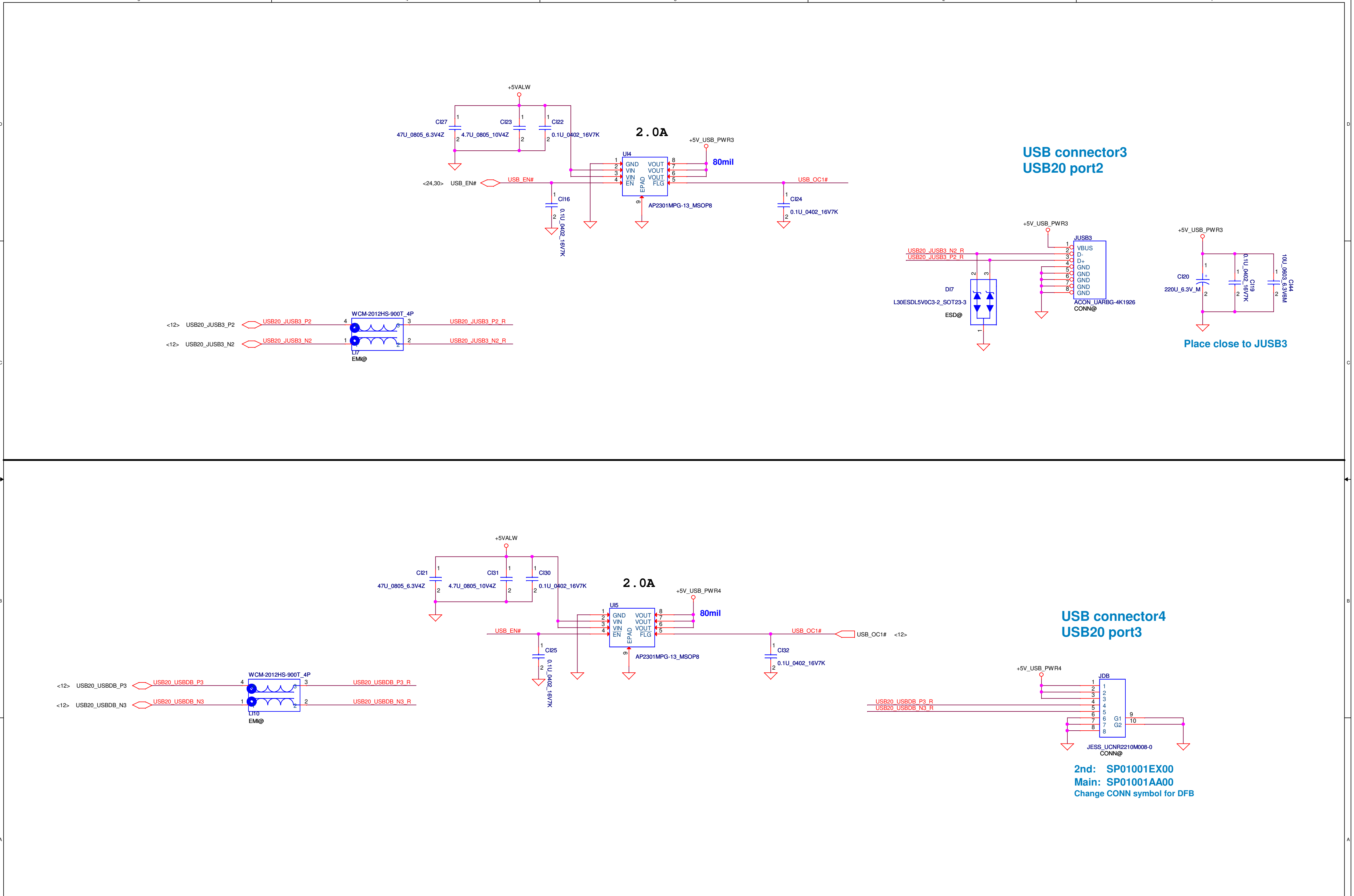
Title: *Card Reader RTS5179*

Size | Document Number: *LA-9984P* | Rev 1.0

Date: Wednesday, May 22, 2013 | Sheet 23 of 57



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: USB3.0
				Size / Document Number: LA-9984P / Rev 1.0
				Date: Wednesday, May 22, 2013 / Sheet 24 of 57

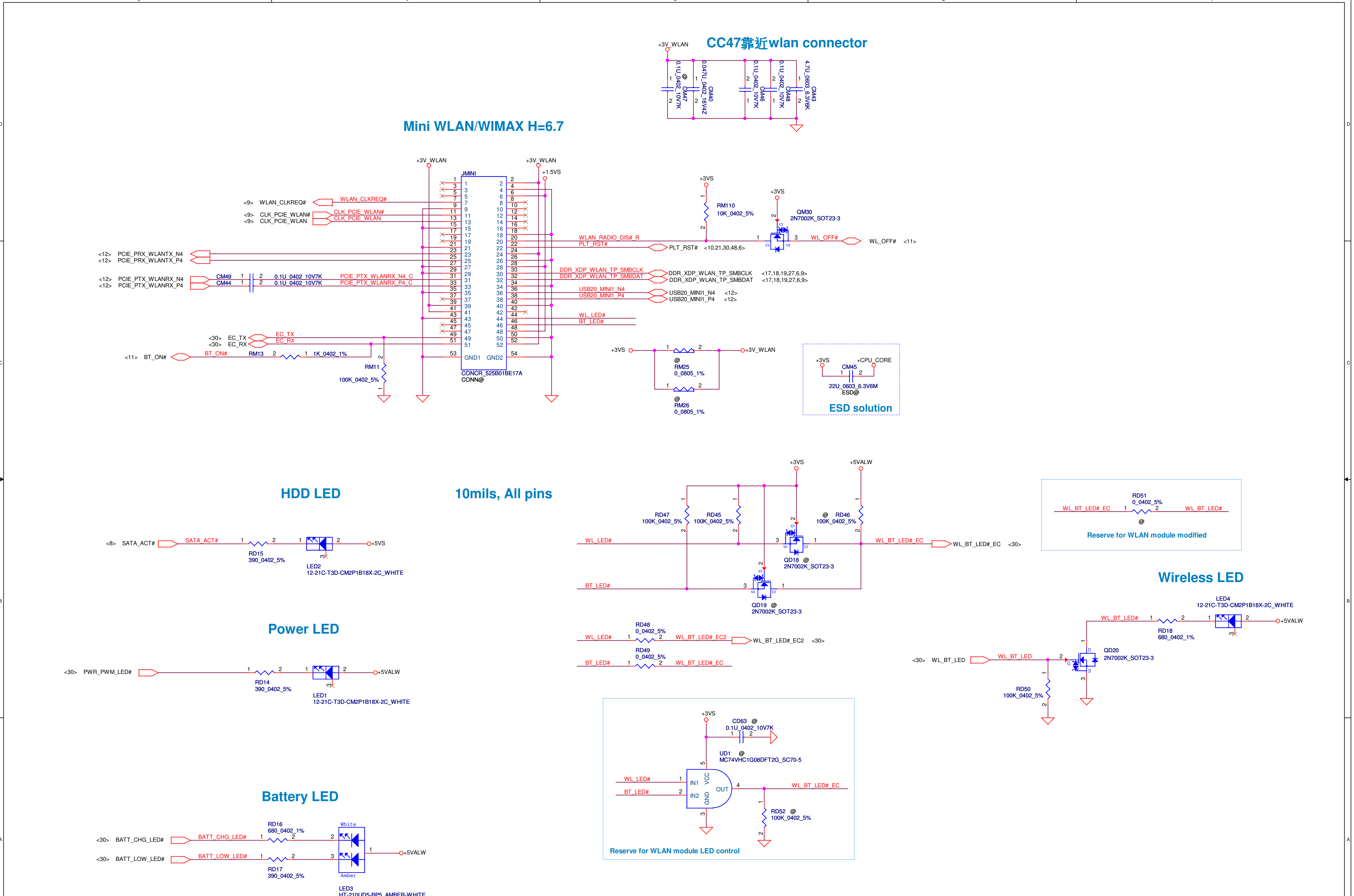


Compal Electronics, Inc.

Title: *MB to USB2.0 DB*

Document Number: *LA-9984P* | Rev 1.0

Date: Wednesday, May 22, 2013



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date 2014/06/01	Title: Mini Card/LED
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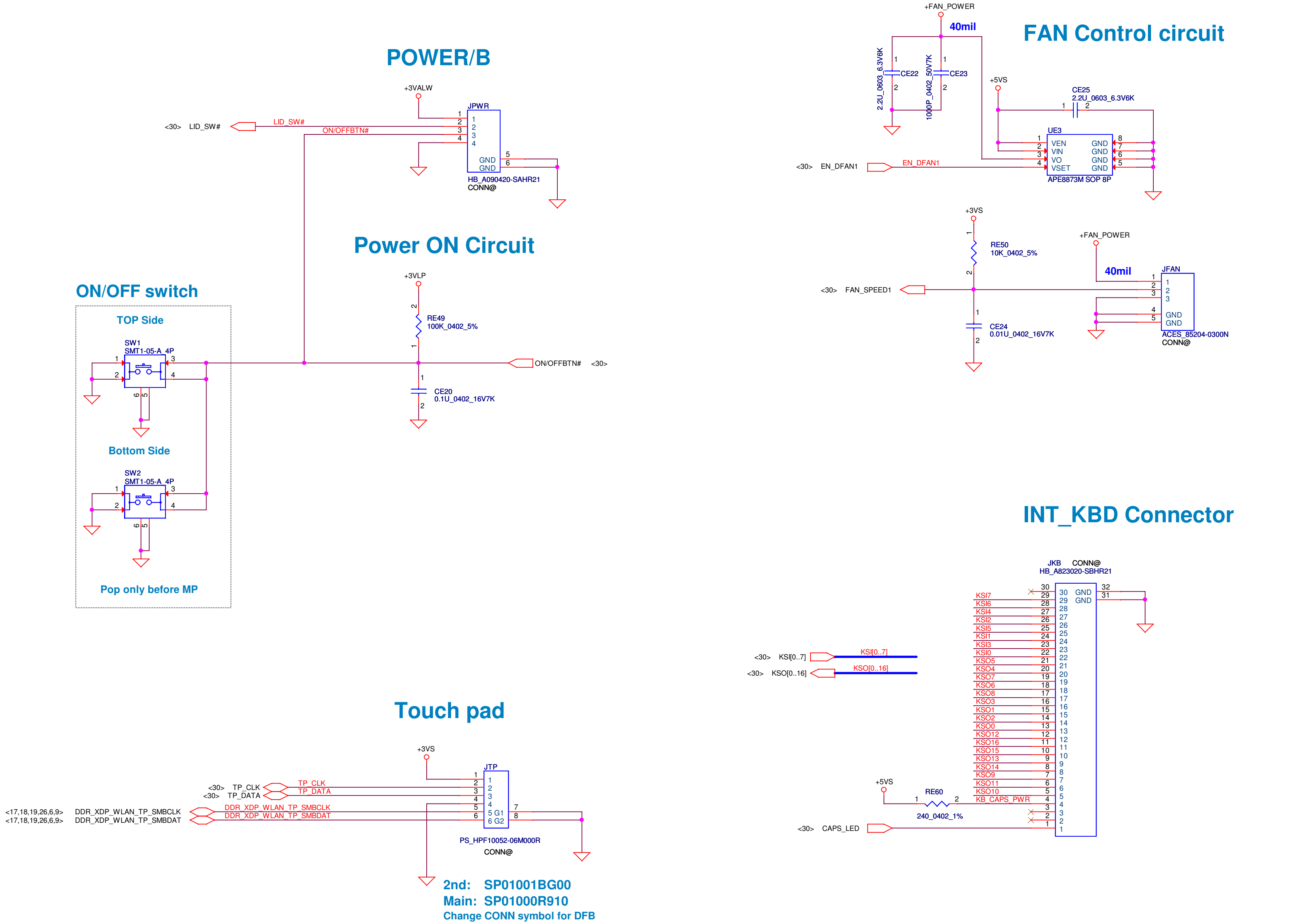
			Date: Wednesday, May 22, 2013 Sheet 26 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

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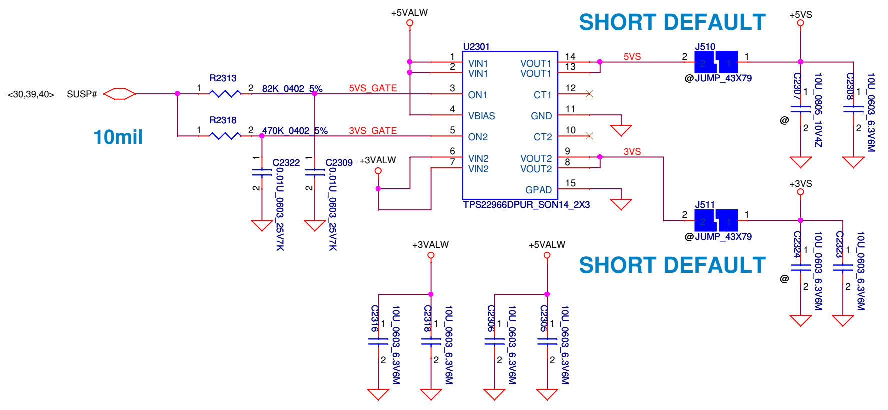
Compal Electronics, Inc.

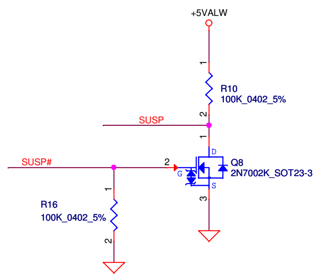
Title	FAN/TP/PWR SW	
Size	Document Number: LA-9984P	Rev 1.0
Date: Wednesday, May 22, 2013	Sheet 27 of 57	

+5VS and +3VS switch

SHORT DEFAULT

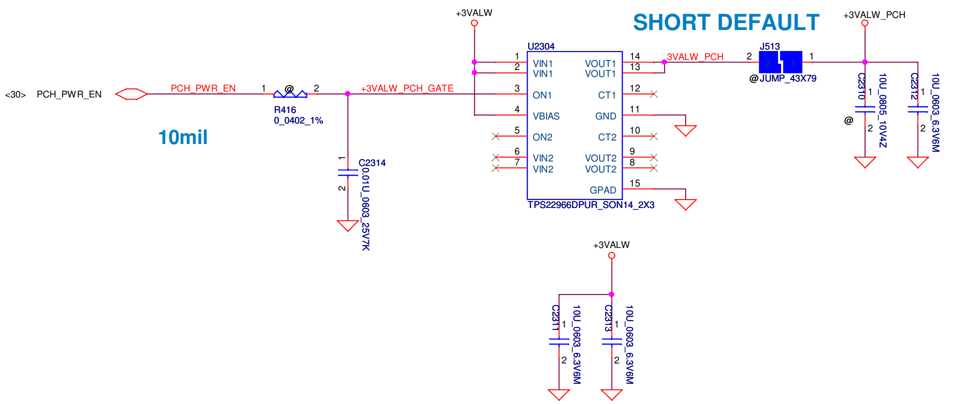


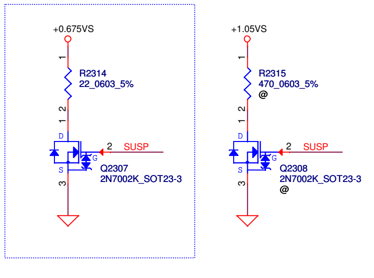
SHORT DEFAULT



+3VALW_PCH switch

SHORT DEFAULT





For Intel S3 Power Reduction

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: DC/DC Interface
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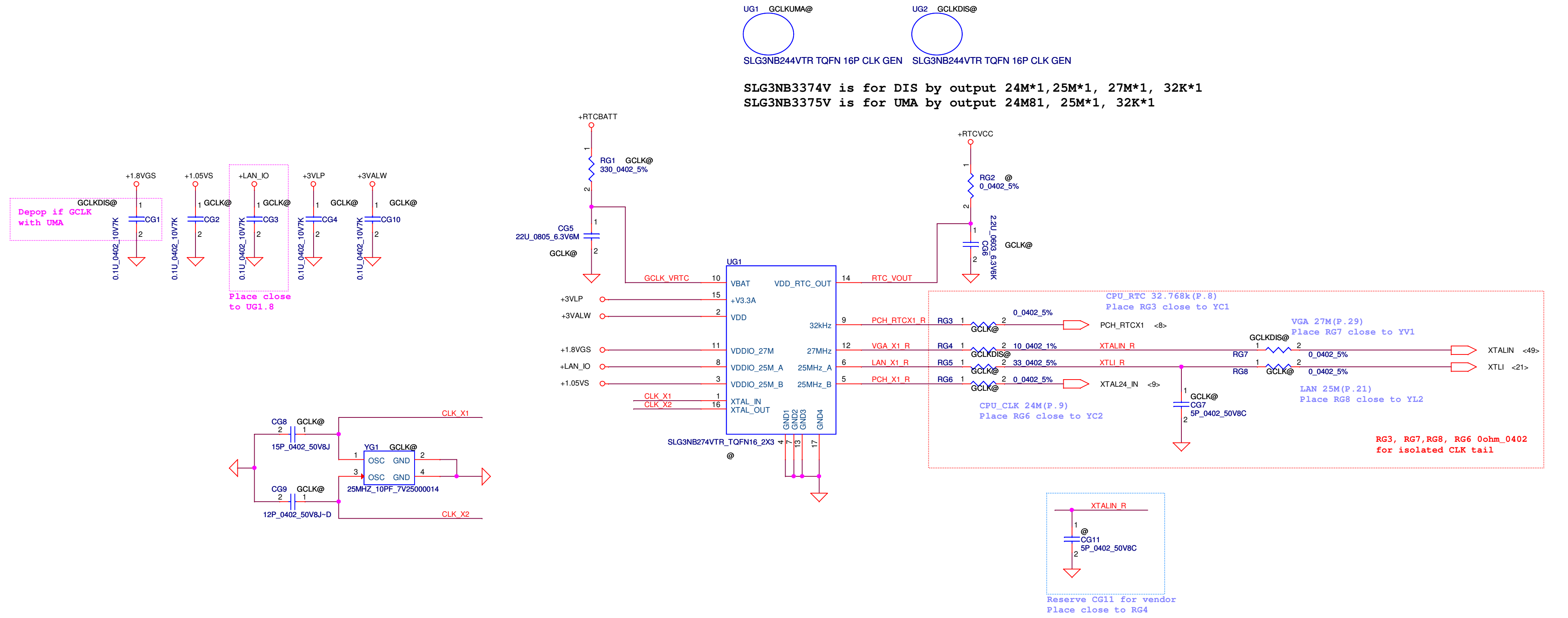
				Date: Wednesday, May 22, 2013 / Sheet 28 of 57



Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

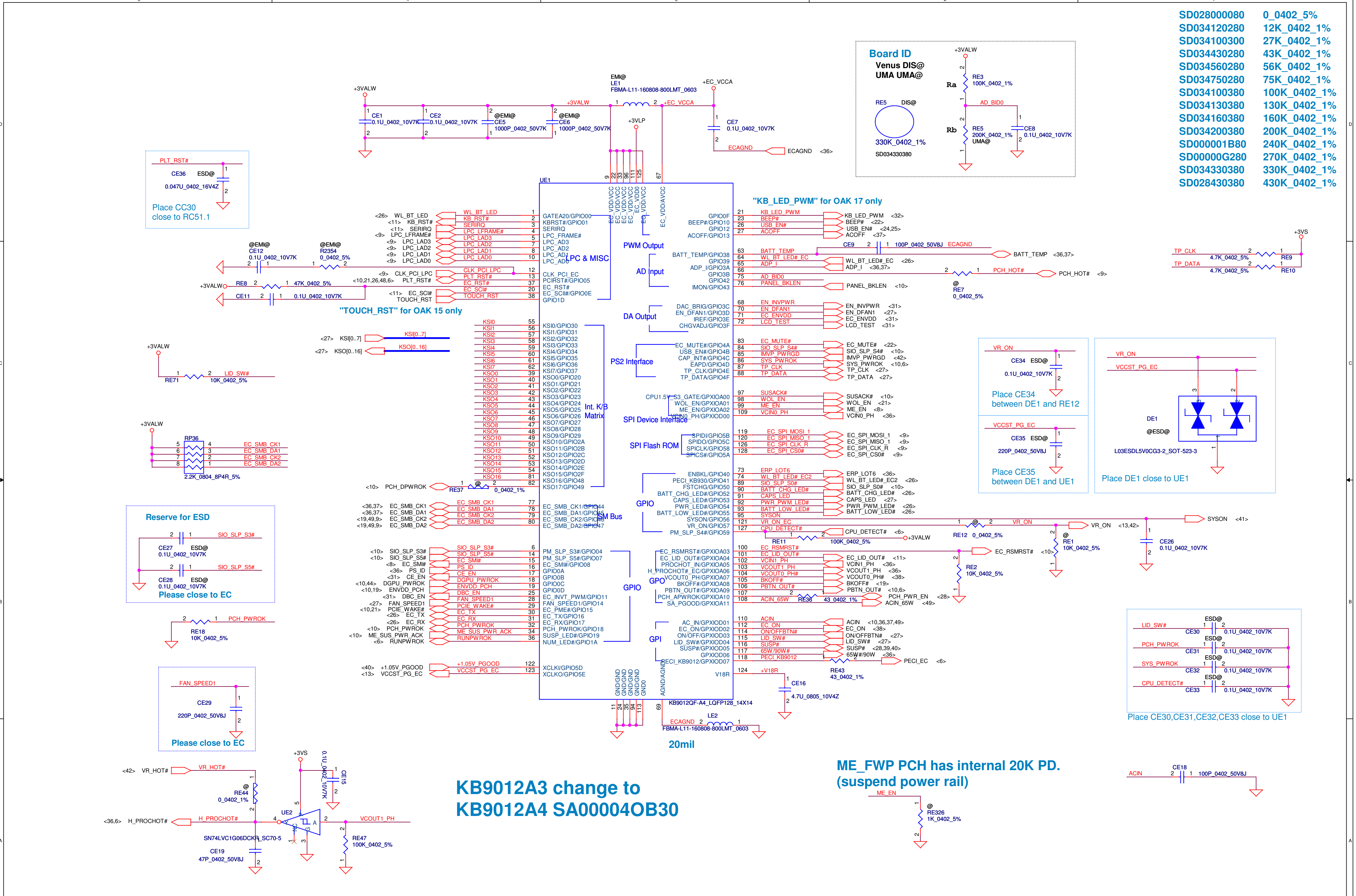
Compal Electronics, Inc.

Title: **GCLK**

Size | Document Number: **LA-9984P** | Rev 1.0

Date: Wednesday, May 22, 2013 | Sheet 23 of 57

SD028000080	0_0402_5%
SD034120280	12K_0402_1%
SD034100300	27K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD000001B80	240K_0402_1%
SD00000G280	270K_0402_1%
SD034330380	330K_0402_1%
SD028430380	430K_0402_1%

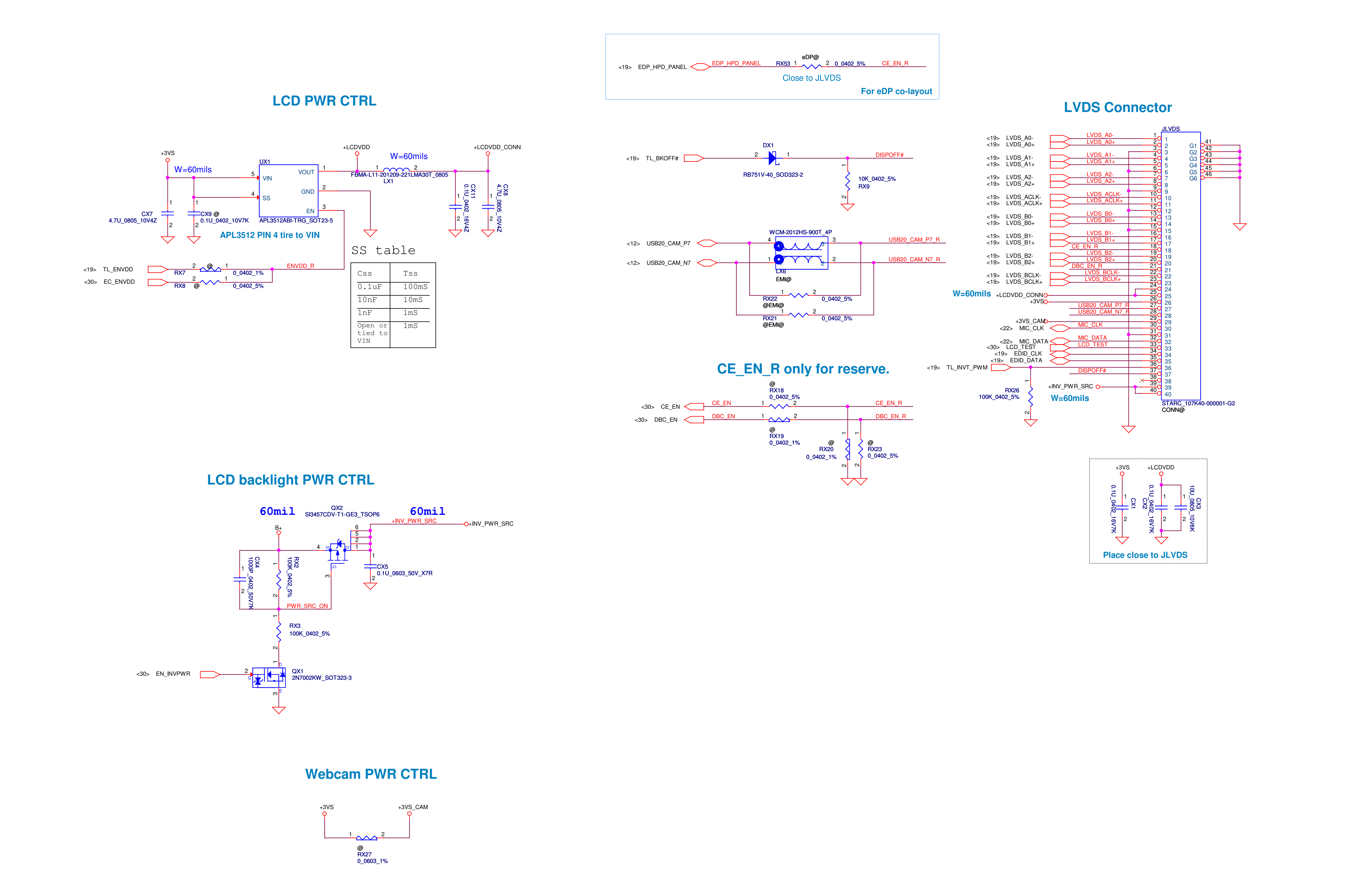


Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: **EC ENE-KB9012**

Size | Document Number: **LA-9984P** | Rev 1.0



SS table

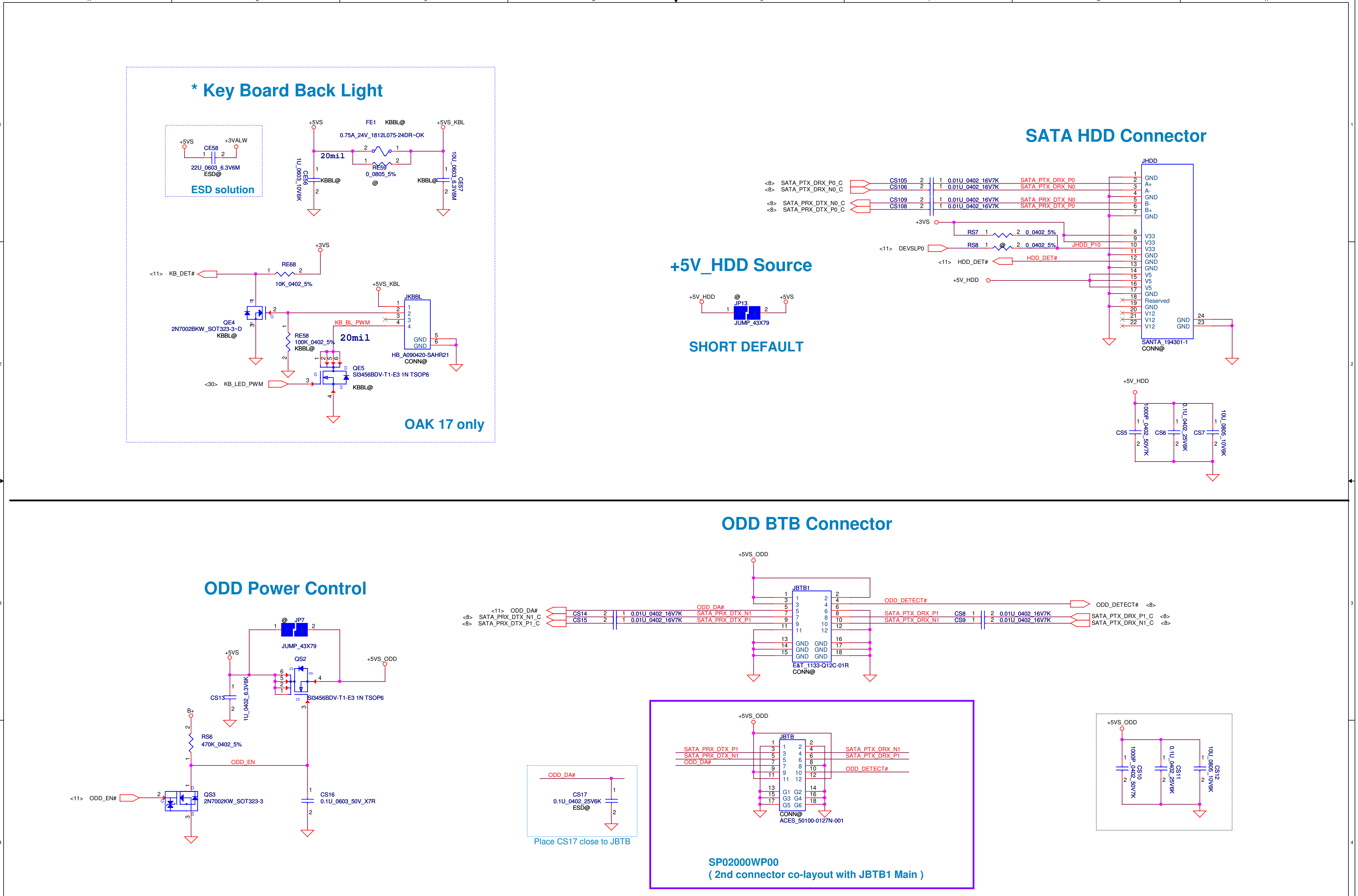
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01

Compal Electronics, Inc.

Title: LVDS/webcam

Size | Document Number: LA-9984P | Rev 1.0



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: HDD/ODD/KB-BL
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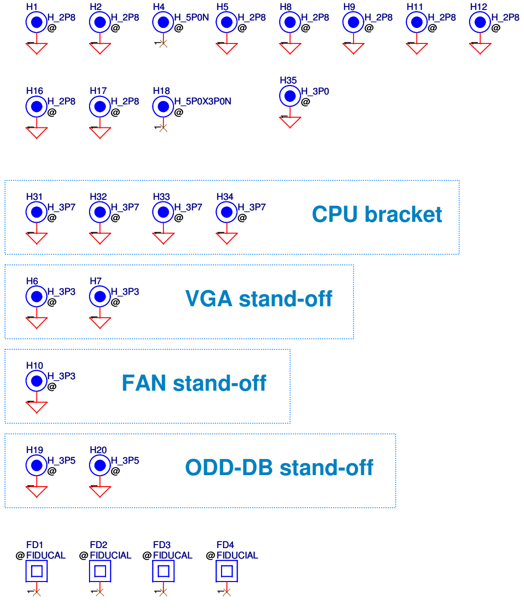
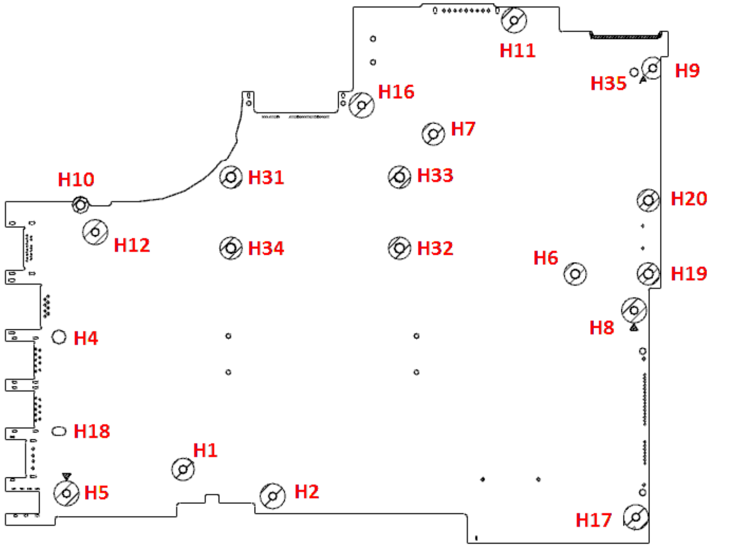
				Date: Wednesday, May 22, 2013 / Sheet 32 of 57

Screw Hole





Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/17	Deciphered Date	2014/06/01	Title: Screw Hole
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size / Document Number: LA-9984P / Rev 1.0
				Date: Wednesday, May 22, 2013 / Sheet 33 of 57

Version Change List (P. I. R. List)   Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
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37							
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39							
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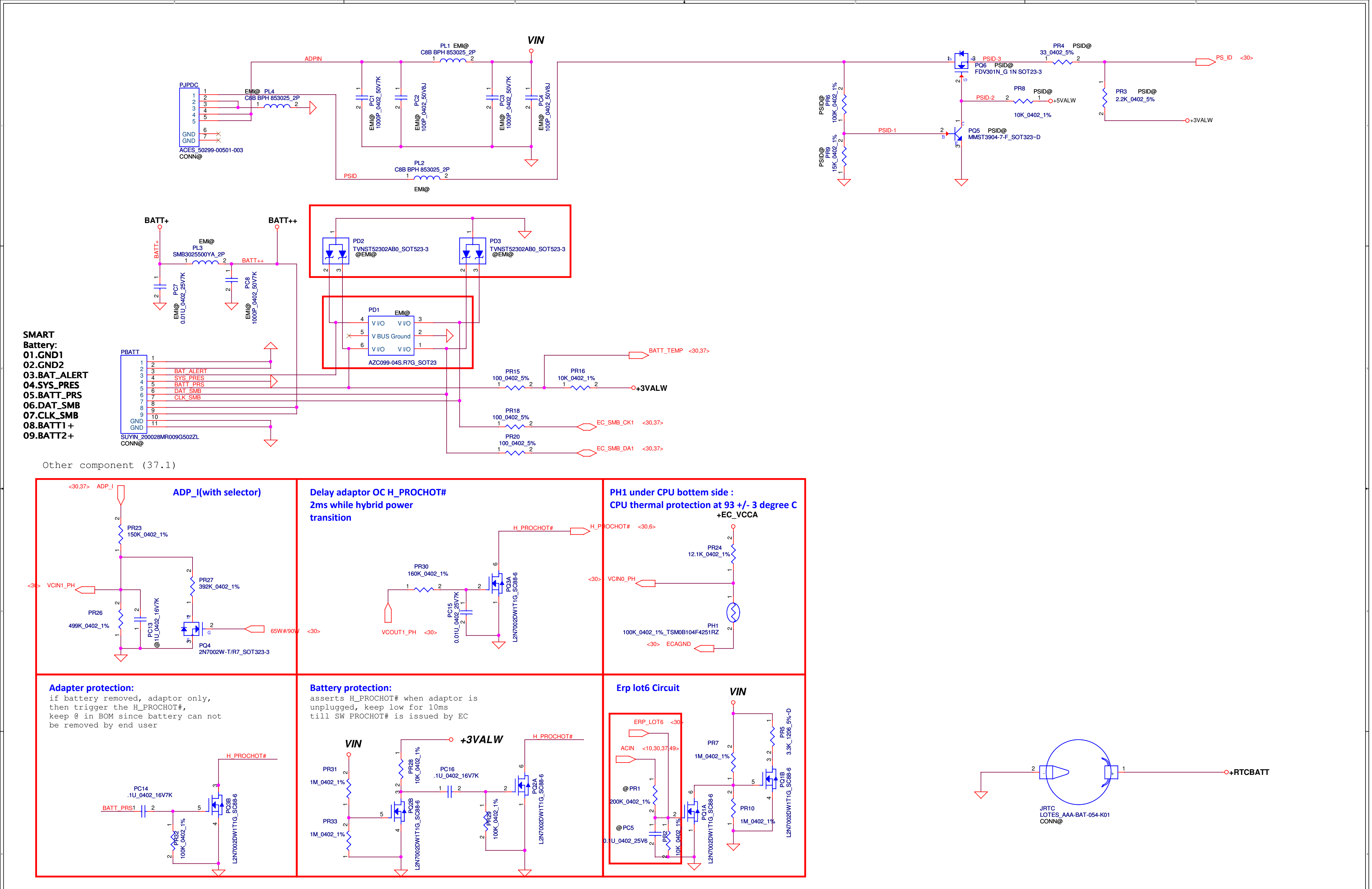
41							

Version Change List (P. I. R. List) Page 2

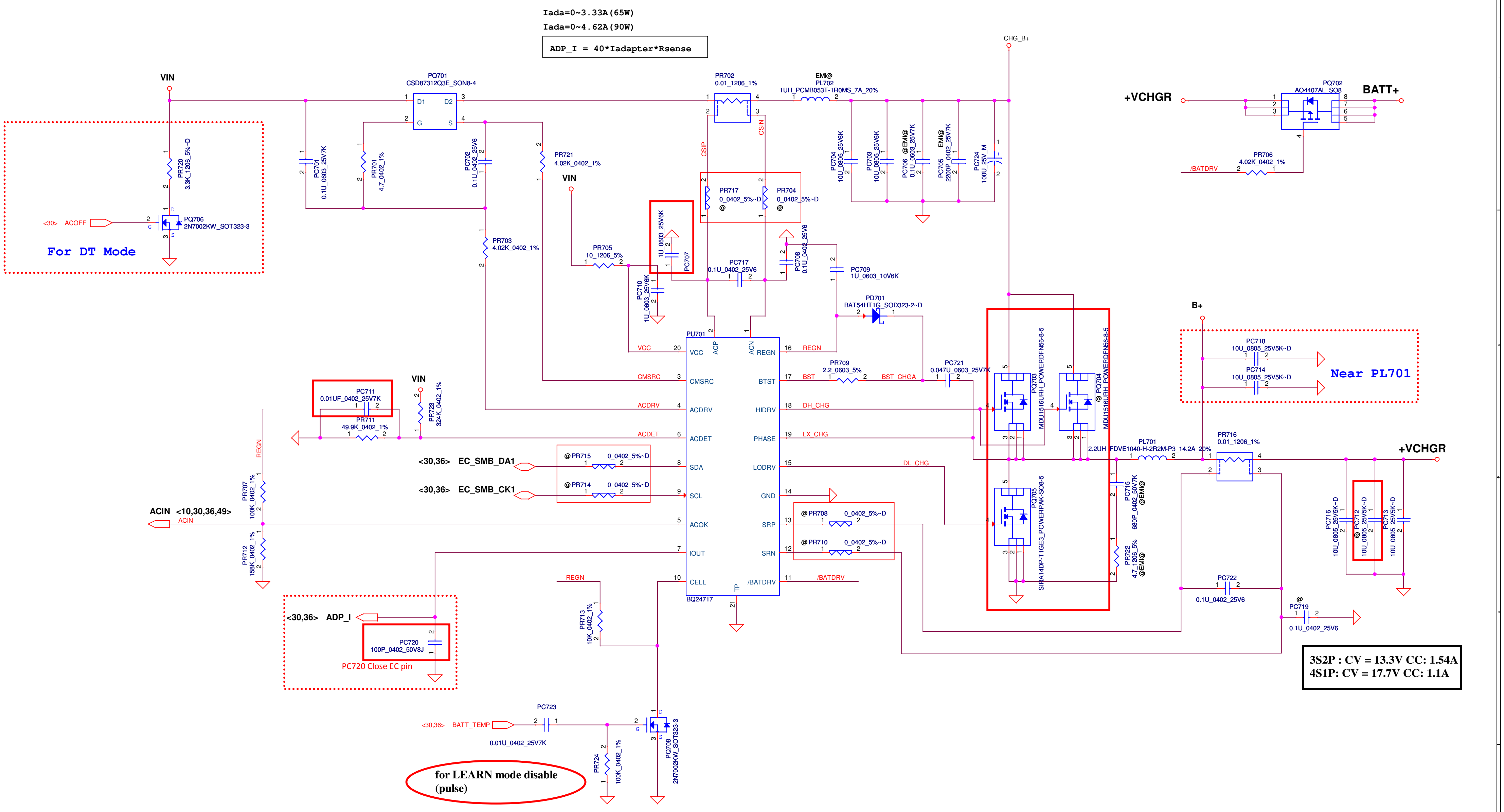
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
44							
45							
46							
47							
48							
49							
50							
51							
52							
53							
54							

Security Classification	Compal Secret Data		
Issued Date	2013/05/17	Deciphered Date	2014/06/01



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/21	Deciphered Date	2014/05/01	Title: PWR_DCIN/BATT CONN/OTP

Size	Document Number	Rev
	LA-9984P	0.4



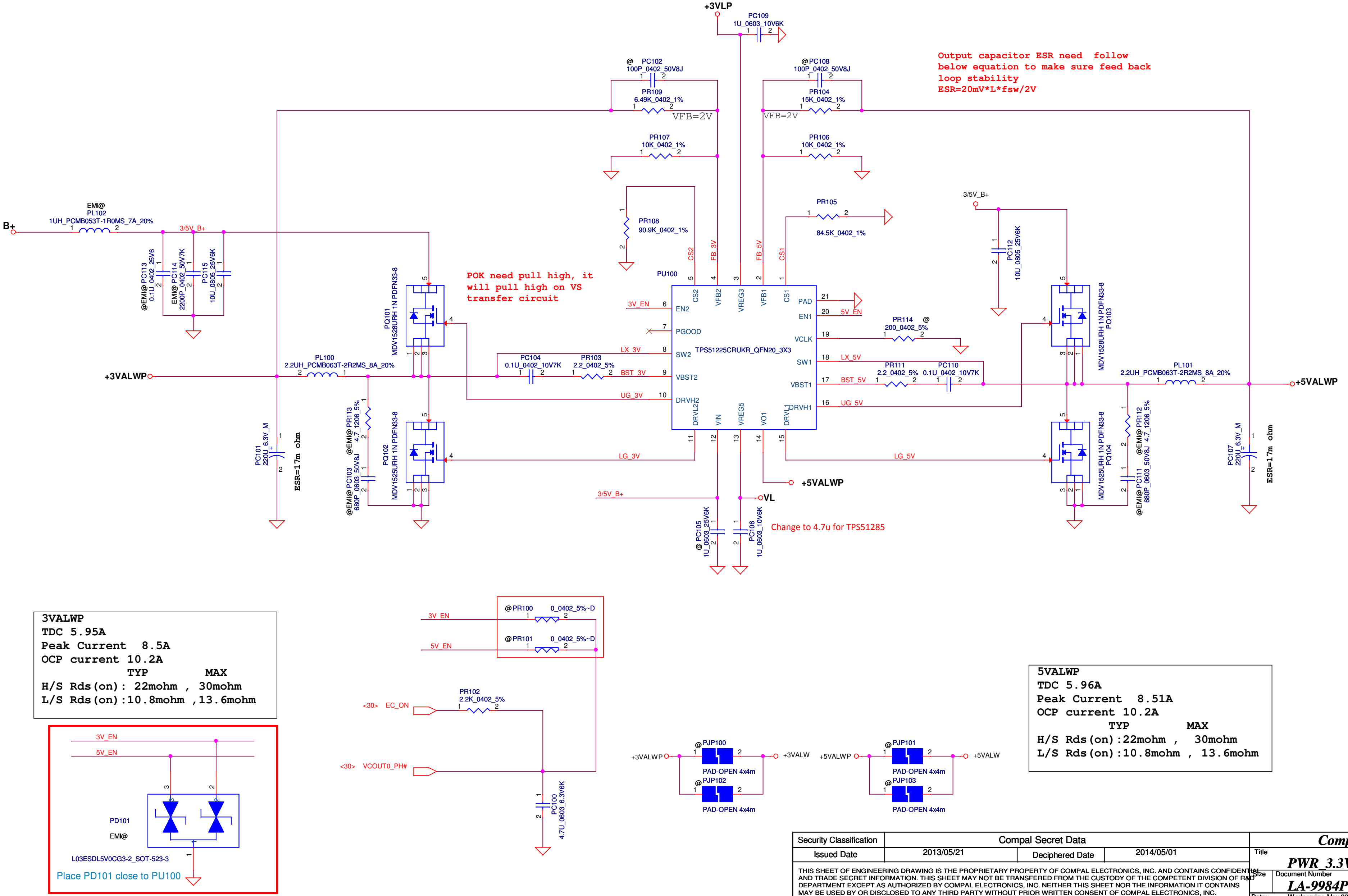
Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.

Title: **PWR_CHARGER**

Size | Document Number: **LA-9984P** | Rev 0.4

Date: Wednesday, May 22, 2013 |



3VALWP
TDC 5.95A
Peak Current 8.5A
OCP current 10.2A

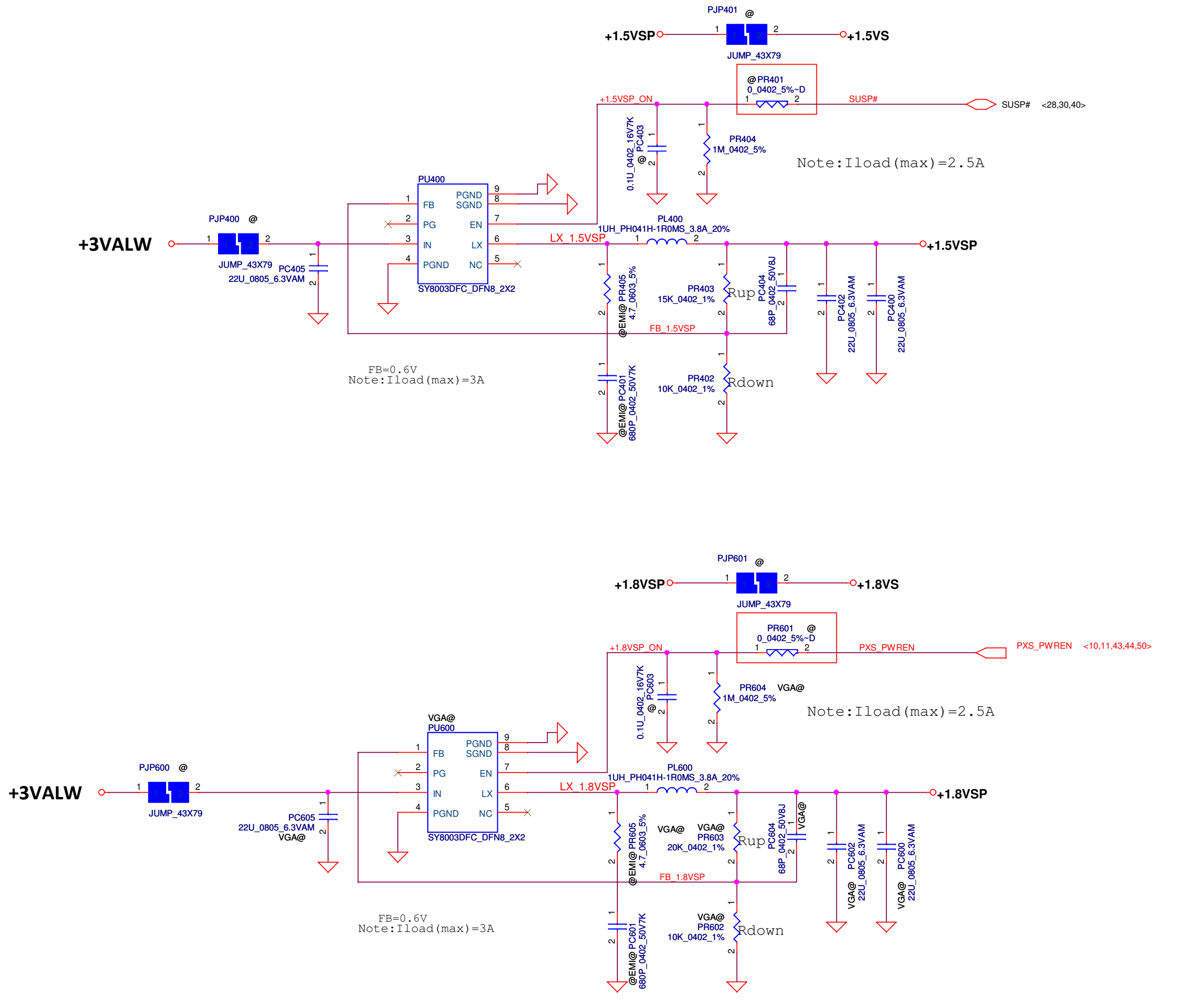
	TYP	MAX
H/S Rds(on):	22mohm	30mohm
L/S Rds(on):	10.8mohm	13.6mohm

5VALWP
TDC 5.96A
Peak Current 8.51A
OCP current 10.2A

	TYP	MAX
H/S Rds(on):	22mohm	30mohm
L/S Rds(on):	10.8mohm	13.6mohm

Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.
Title: PWR_3.3VALWP/5VALWP
Size | Document Number: LA-9984P | Rev 0.4
Date: Wednesday, May 22, 2013



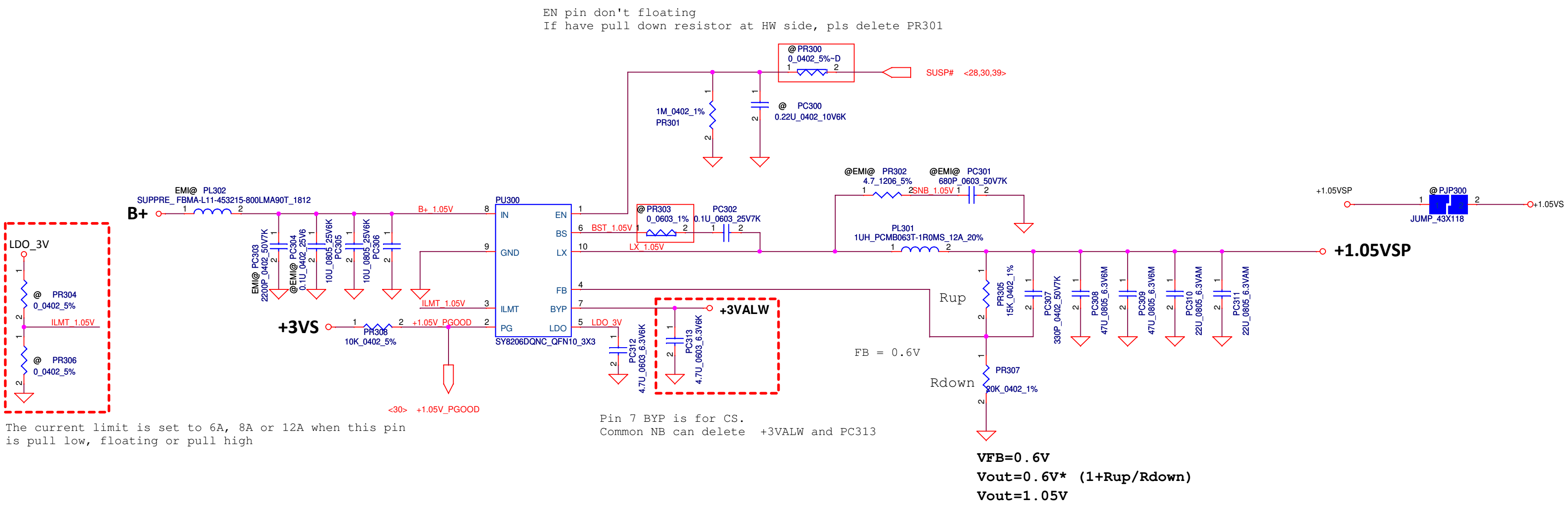
Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.

Title: **PWR_1.5VSP / 1.8VSP**

Size	Document Number	Rev
	LA-9984P	0.4

Date: Wednesday, May 22, 2013



+1.05VSP
TDC 5A
Peak Current 6.6A
OCP current 8A

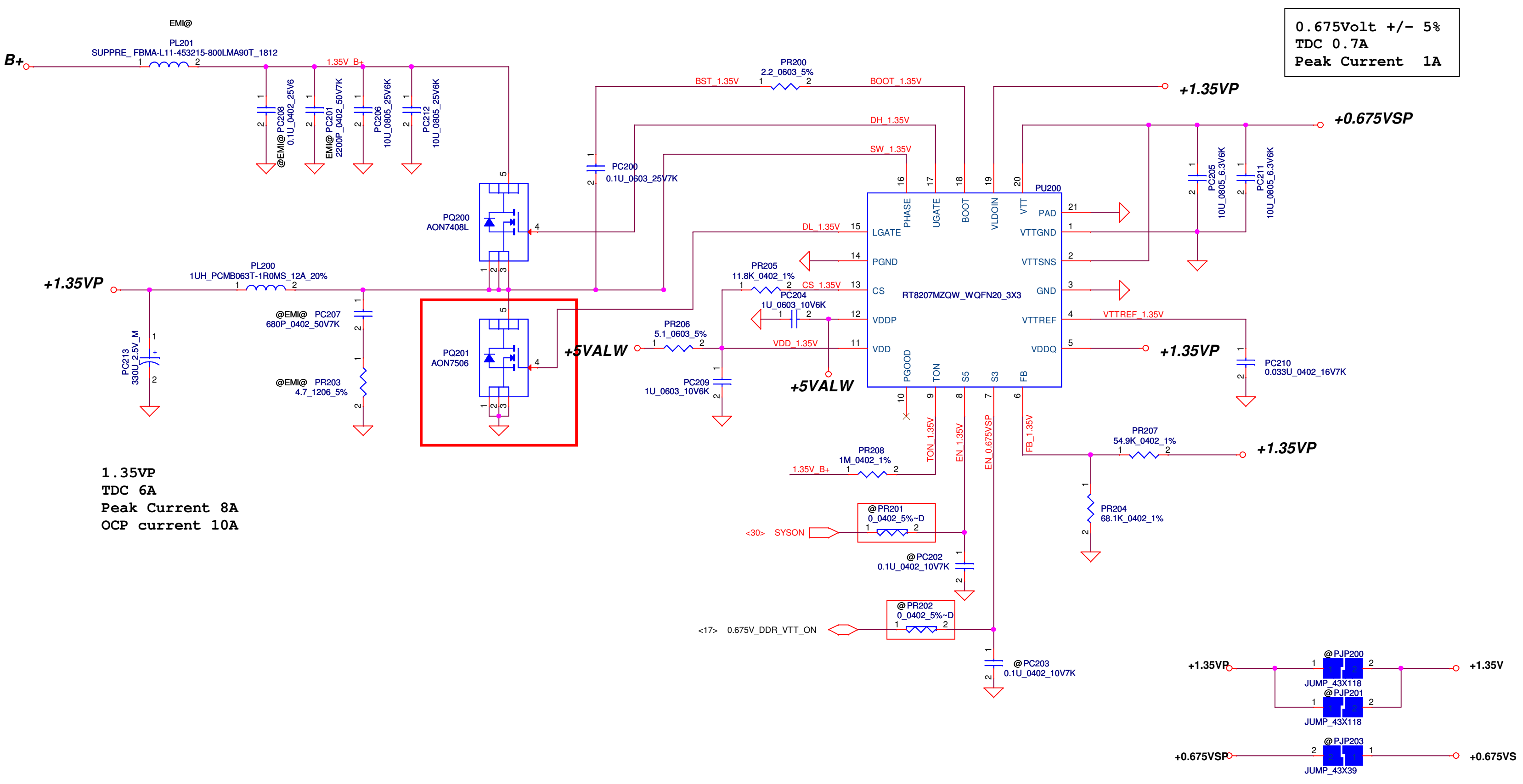
Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.

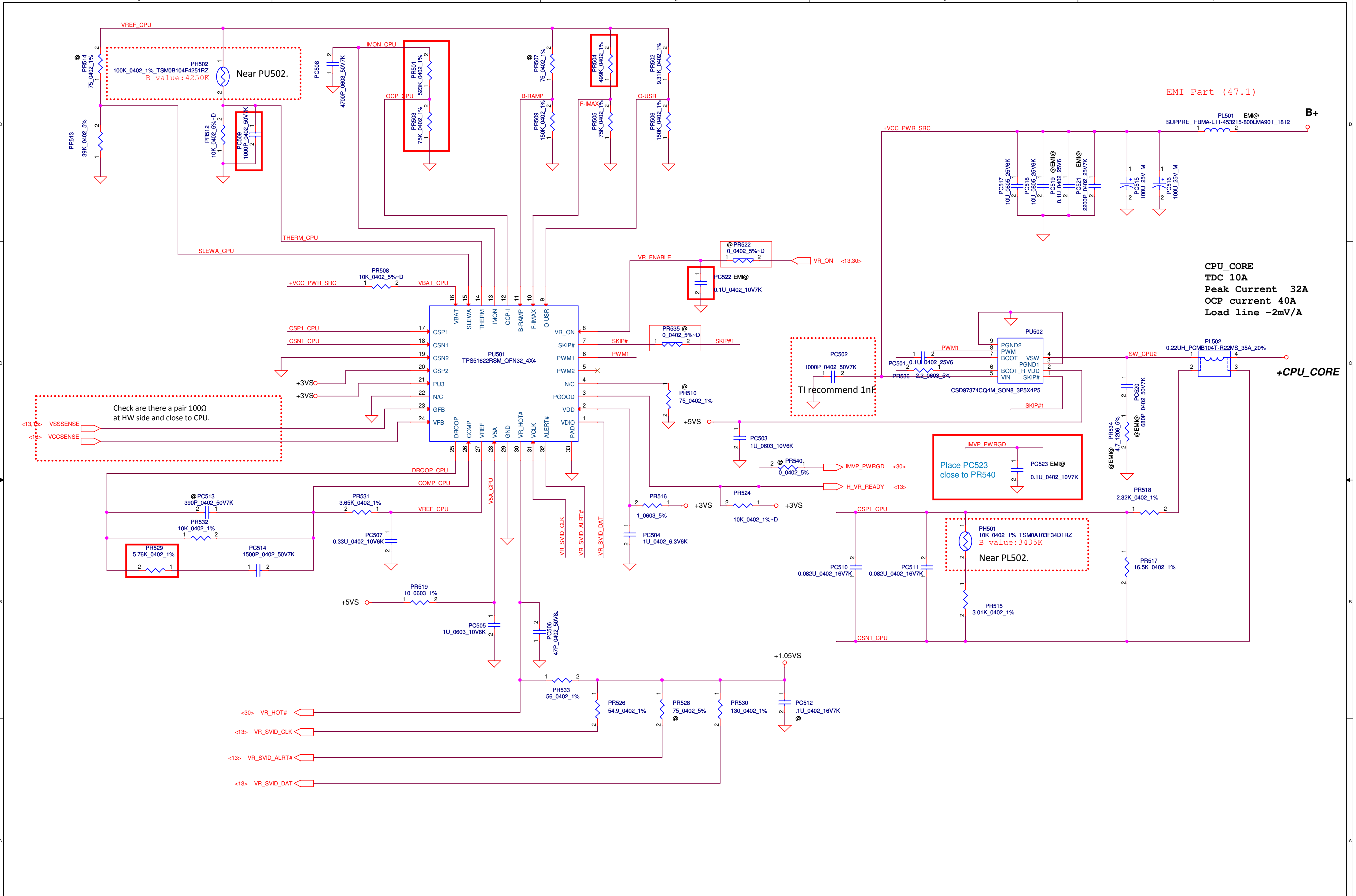
Title: PWR_+VCCIO

Size: C | Document Number | Rev: 0.4

Date: Wednesday, May 22, 2013 |



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/21	Deciphered Date 2014/05/01	Title: PWR_+1.35VP/0.675VSP
			Size / Document Number: LA-9984P / Rev 0.4
			Date: Wednesday, May 22, 2013 / Sheet 41 of 57



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2013/05/21	Deciphered Date 2014/05/01	Title: PWR_VCORE

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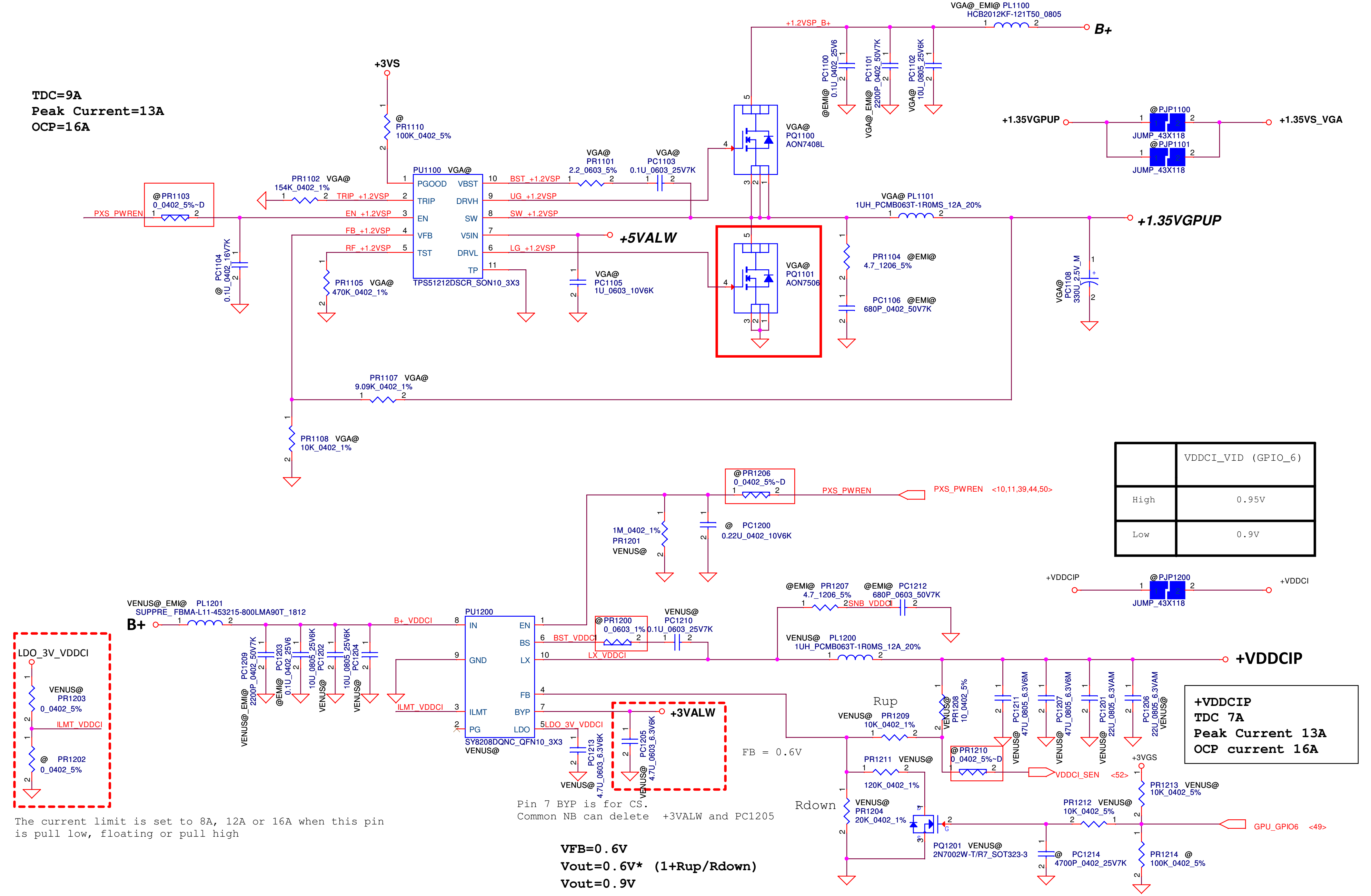
Size | Document Number: LA-9984P | Rev 0.4

Date: Wednesday, May 22, 2013 | Sheet 42 of 57



TDC=9A
Peak Current=13A
OCP=16A

	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V

+VDDCIP
TDC 7A
Peak Current 13A
OCP current 16A

FB = 0.6V

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

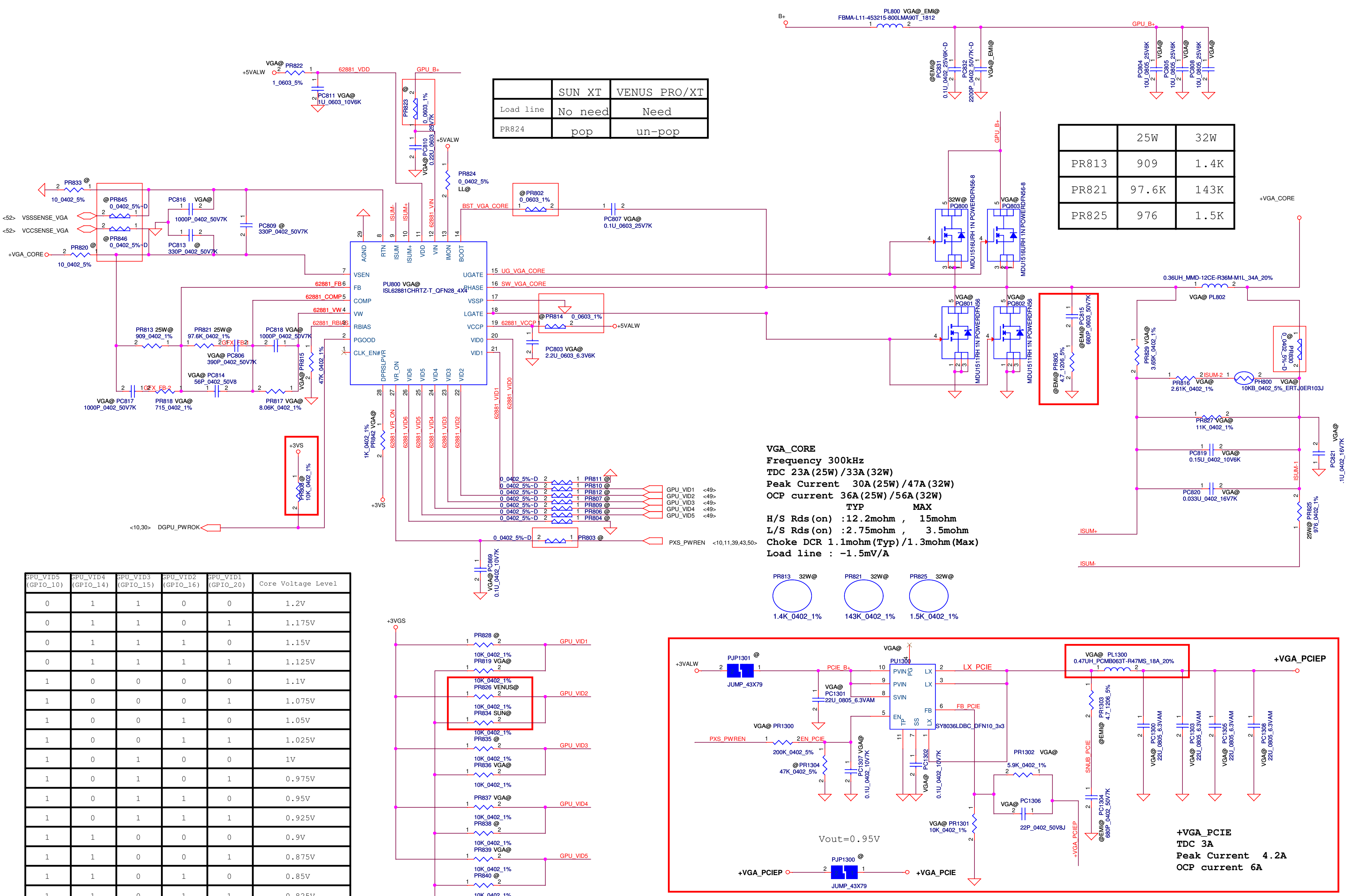
Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.9V

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/21	Deciphered Date	2014/05/01	Title: PWR_+1.35VGPU/VDDCIP

Size | Document Number: LA-9984P | Rev 0.4

Date: Wednesday, May 22, 2013 | Sheet 43 of 57



	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

VGA_CORE
Frequency 300kHz
TDC 23A(25W)/33A(32W)
Peak Current 30A(25W)/47A(32W)
OCP current 36A(25W)/56A(32W)

	TYP	MAX
H/S Rds(on)	:12.2mohm ,	15mohm
L/S Rds(on)	:2.75mohm ,	3.5mohm

Choke DCR 1.1mohm(Typ)/1.3mohm(Max)
Load line : -1.5mV/A

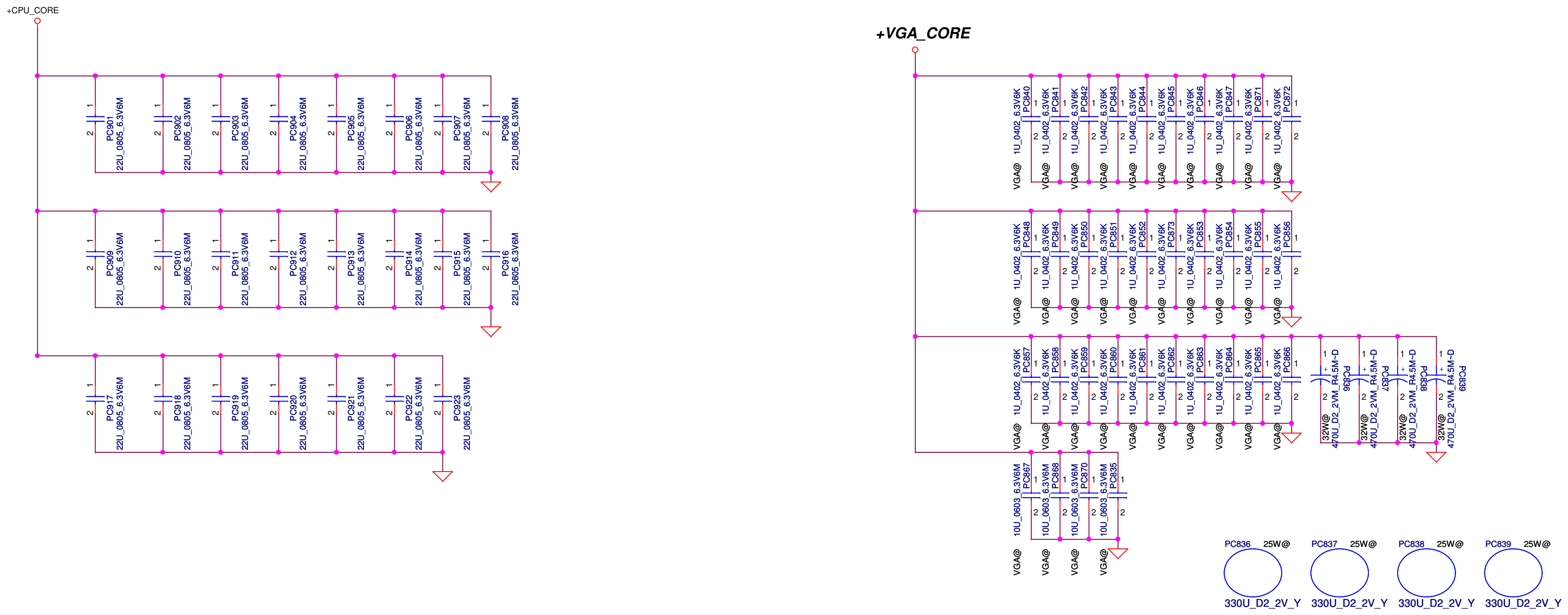
GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

Initial voltage:0.85V(Venus)
0.9V(Sun)

+VGA_PCIE
TDC 3A
Peak Current 4.2A
OCP current 6A

Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

Compal Electronics, Inc.
Title: *PWR_VGA_CORE/PCIE*
Size / Document Number: *LA-9984P* Rev 0.4



Security Classification	Compal Secret Data		
Issued Date	2013/05/21	Deciphered Date	2014/05/01

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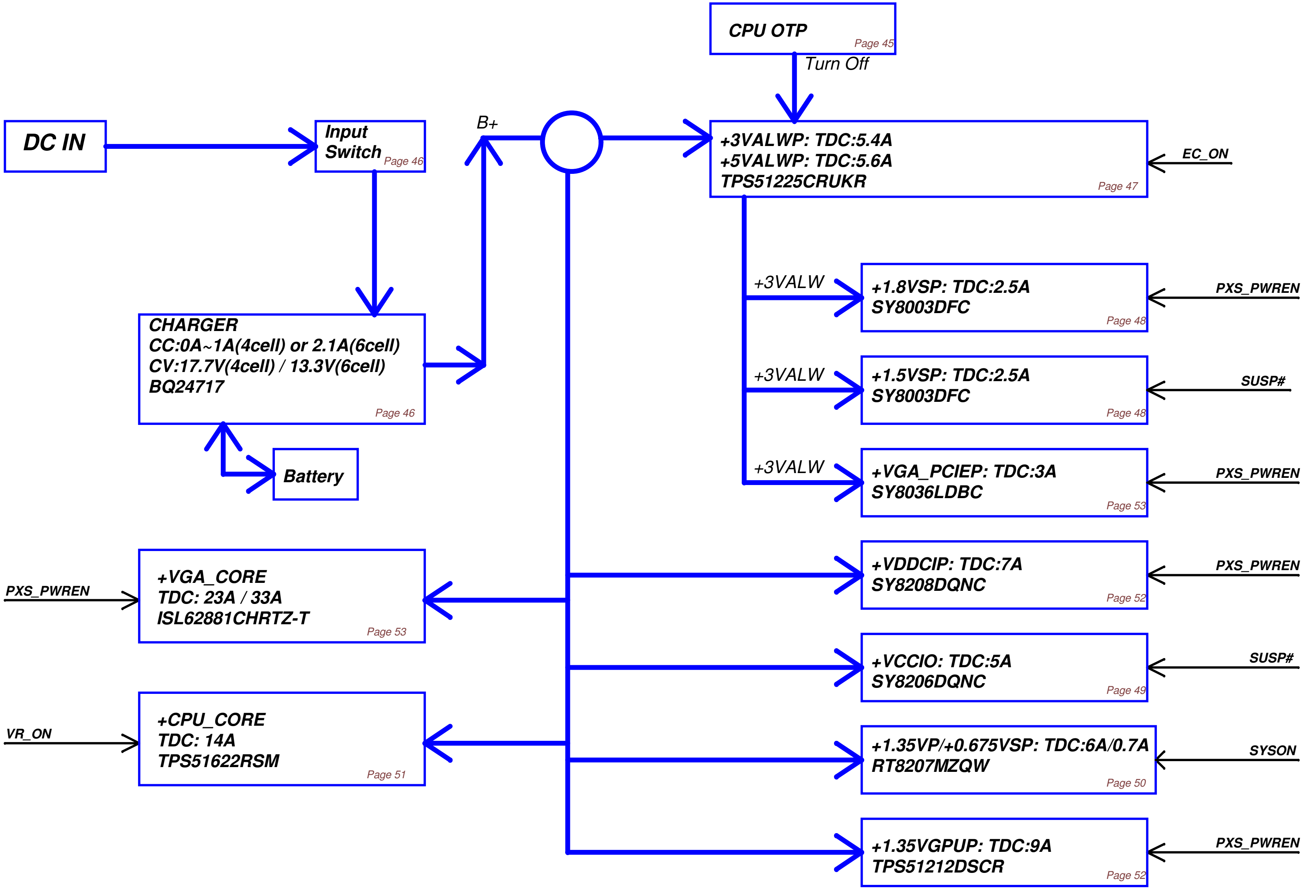
Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

Size | Document Number: **LA-9984P** | Rev 0.4

Date: Wednesday, May 22, 2013 | Sheet 45 of 57

Power block

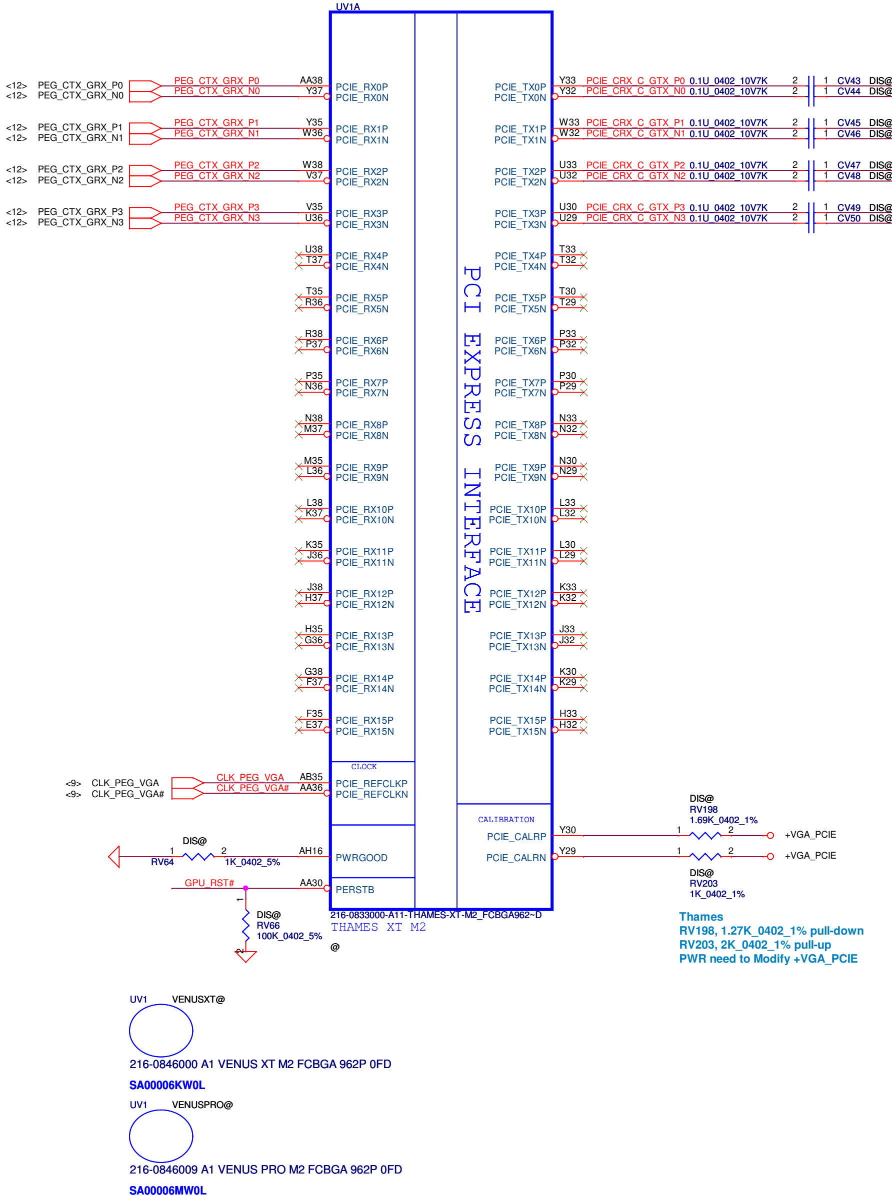


Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2013/05/21	Deciphered Date	2014/05/01	Title: PWR_POWER BLOCK DIAGRAM
				Size: / Document Number: LA-9984P / Rev: 0.4
				Date: Wednesday, May 22, 2013 / Sheet 46 of 57

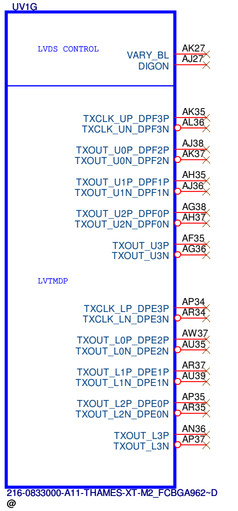
Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	CHARGER	13/01/30	Morris	adjust design parameter from vendor recommend	delete PD702 change PC712 to unpop change PQ704 to unpop change PC707 from 0.1uF_0402 to 1uF_0603 change PC720 from 0.1uF to 100pF change PC711 from 1000pF to 0.01uF change PQ705 from SB00000SD00 to SB00000WY00	0.3
2	42	VCORE	13/01/30	Morris	adjust design parameter from vendor recommend	change PC509 from 0.1uF to 1000pF change PR529 from 3.83K to 5.76K change PR504 from 523K to 499K	0.3
3	36	DCIN/BATT CONN/OTP	13/01/30	Morris	change from ESD request	change PD1 from SC300002E00 to SC300001G00	0.3
4	38	3.3VALWP/5VALWP	13/02/01	Morris	add ESD diode from ESD request	add PD101(SCA00002A00)	0.3
5	42	VCORE	13/02/21	Morris	adjust design parameter from fine tune result	change PR501 from 422K to 523K change PR503 from 56K to 75K	0.3
6	44	VGA_CORE/PCIE	13/02/21	Morris	unpop from EE request	unpop PR808	0.3
7	44	VGA_CORE/PCIE	13/03/05	Morris	adjust output voltage from vender request	unpop PR826 and pop PR834 (only for Sun XT)	0.3
8	37 38 39 40 41 42	CHARGER 3.3VALWP/5VALWP 1.5VSP/1.8VSP +VCCIO +1.35VP/0.675VSP VCORE	13/03/28	Morris	verify function ok, so delete 0 ohm to short	unpop PR100,PR101,PR201,PR202,PR300,PR303,PR401,PR522,PR535, PR704,PR708,PR710,PR714,PR715,PR717	0.4
9	36	DCIN/BATT CONN/OTP	13/04/09	Morris	design change for solve issue	unpop PR1 and PC5	0.4
10	41 43	+1.35VP/0.675VSP +1.35VGPU/VDDCI	13/04/09	Morris	part shortage issue	change PQ201 and PQ1101 from SB00000T600 to SB000010A00	0.4
11	39 43 44	1.5VSP/1.8VSP +1.35VGPU/VDDCI VGA_CORE/PCIE	13/04/09	Morris	verify function ok, so delete 0 ohm to short	unpop PR601,PR802,PR803,PR814,PR823,PR830,PR845,PR846, PR1103,PR1200,PR1206,PR1210	0.4
12	43	+1.35VGPU/VDDCI	13/04/09	Morris	unpop VDDCI parts from vendor recommend and EEverify ok only for Sun XT	unpop PL1200,PL1201,PU1200,PQ1201,PR1201,PR1203,PR1204,PR1208,PR1209, PR1211,PR1212,PR1213,PC1201,PC1202,PC1204,PC1205,PC1206,PC1207, PC1209,PC1210,PC1211,PC1213 (only for Sun XT)	0.4
13	44	VGA_CORE/PCIE	13/04/12	Morris	part shortage issue	change PL1300 from SH00000GQ00 to SH00000PK00	0.4
14	36	DCIN/BATT CONN/OTP	13/04/12	Morris	customer request	add PR2 10Kohm	0.4
15	42	VCORE	13/04/15	Morris	EMI request	pop PC522 and add PC523 0.1uF	0.4

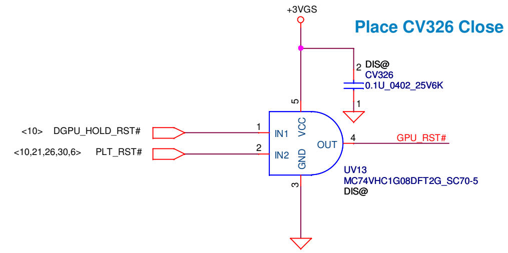
GFX PCIE LANE REVERSAL



LVDS Interface



Place CV326 Close to UV13



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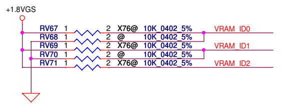
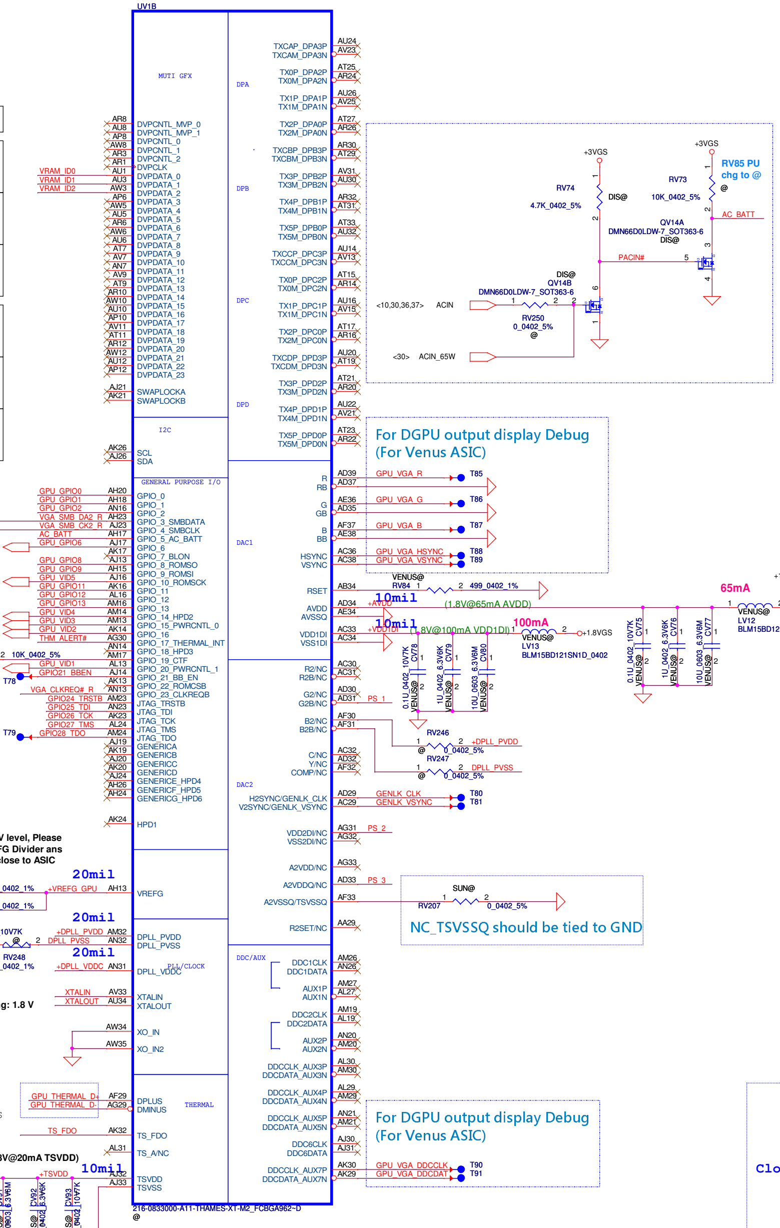
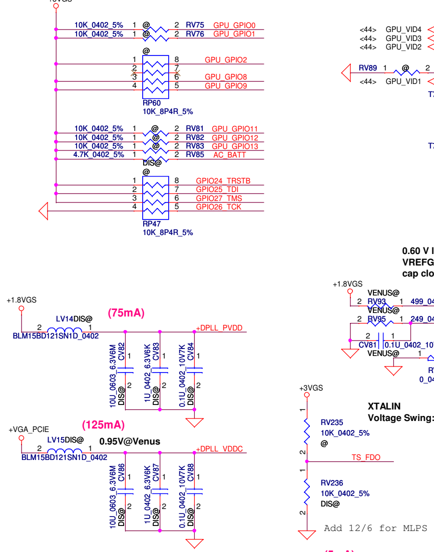


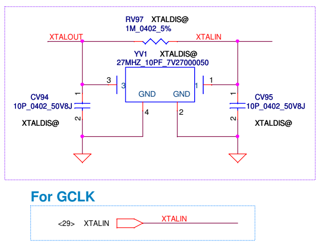
Vendor		VRAM_ID0	VRAM_ID1	VRAM_ID2
* 128Mx16bits (64Mx32bits) GDDR5	H5GQ2H24AFR-T2C Hynix 2Gb SA00004GD1L(R1) SA00004GD2L(R3)	RV67 1	RV69 1	RV71 1
128Mx16bits (64Mx32bits) GDDR5	K4G20325FD-FC04 Samsung 2Gb SA00005B70L(R1) SA00005B71L(R3)	RV68 0	RV69 1	RV71 1
		RV67 1	RV70 0	RV71 1
128MX16bits DDR3	H5TC2G63FFR-11C Hynix 1Gb SA00006H40L(R1) SA00006H41L(R3)			
128MX16bits DDR3	K4W2G1646E-BY11 Samsung 1Gb SA00005SH0L(R1) SA00005SH1L(R3)			
128MX16bits DDR3	MT41K128M16JT-107G:K Micron 1Gb SA00005XB0L(R1) SA00005XB1L(R3)			

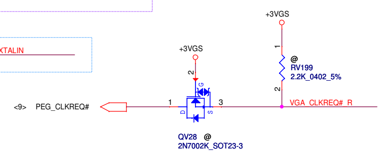
STRAPS



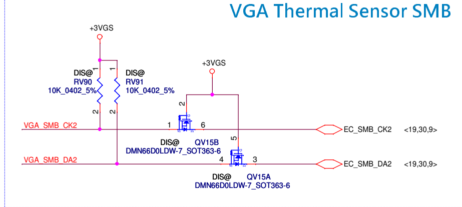


For GCLK





VGA Thermal Sensor SMB



SUN internal VGA Thermal Sensor
Address 0x714

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

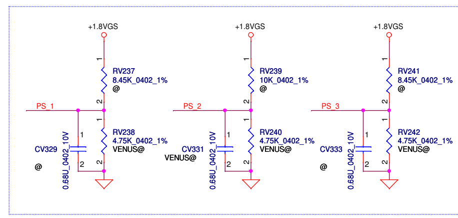
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING — 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS — 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test — 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM — 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21 H2SYNC GENERICC GPIO2 GPIO8

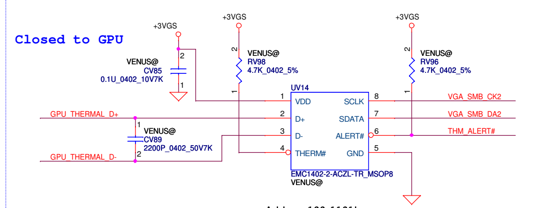
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)



SUN MLPs PS_3	RV241	RV242	Bits [3:1]
* Hynix	NC	4.75k	000
Samsung	8.45k	2k	001
Micron	4.75k	NC	111

VENUS MLPs
PS_3 used default

External Thermal Sensor EMC1402-2-ACZL-TR



Address:100_1101b
Main : SA00001Z710
2nd : SA00003PU00

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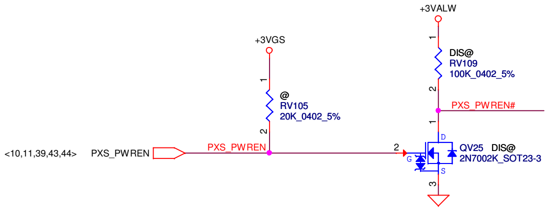
PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

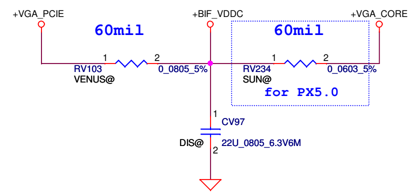
Note:

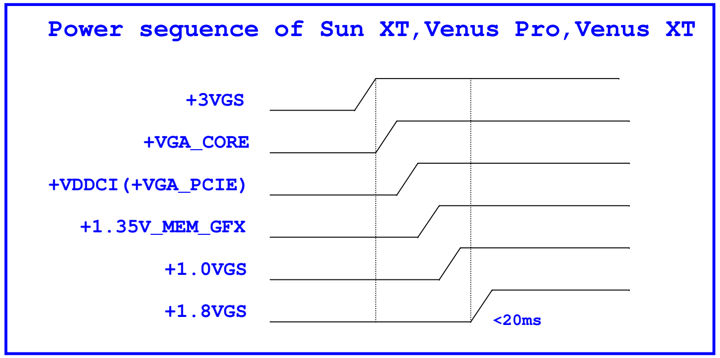
PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF



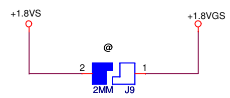
for PX4.0 and PX5.0

Switch circuits in BACO desingns for Thames/Seymour only
55mA@1.0V, in BACO mode



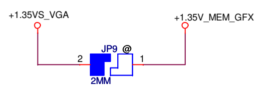


+1.8VS TO +1.8VGS



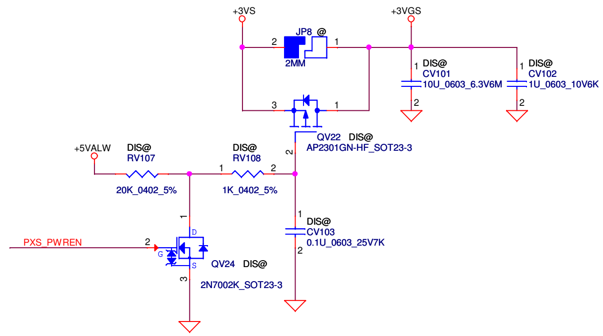
SHORT DEFAULT

+1.35VS_VGA TO +1.35V_MEM_GFX



SHORT DEFAULT

+3VS TO +3VGS



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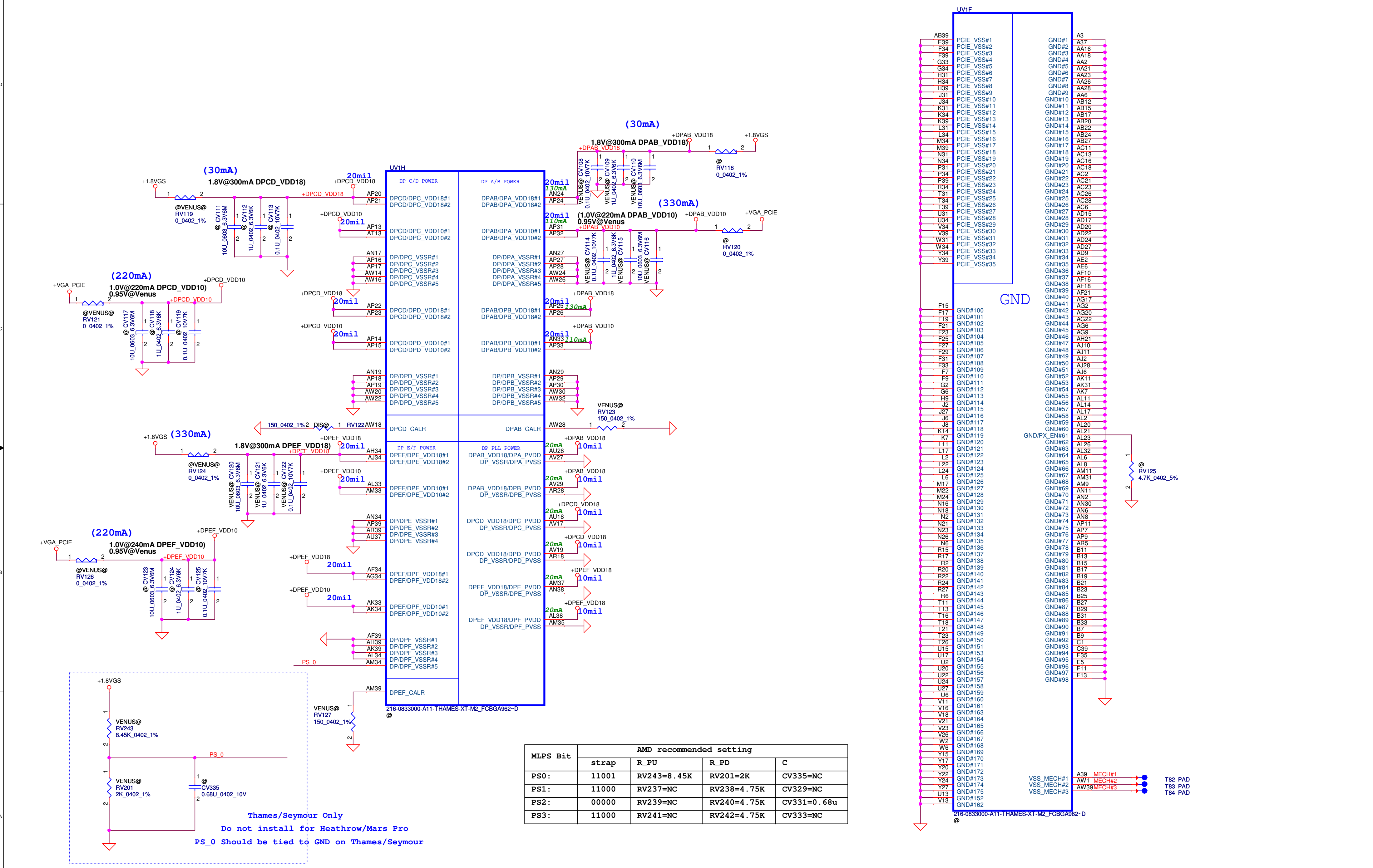
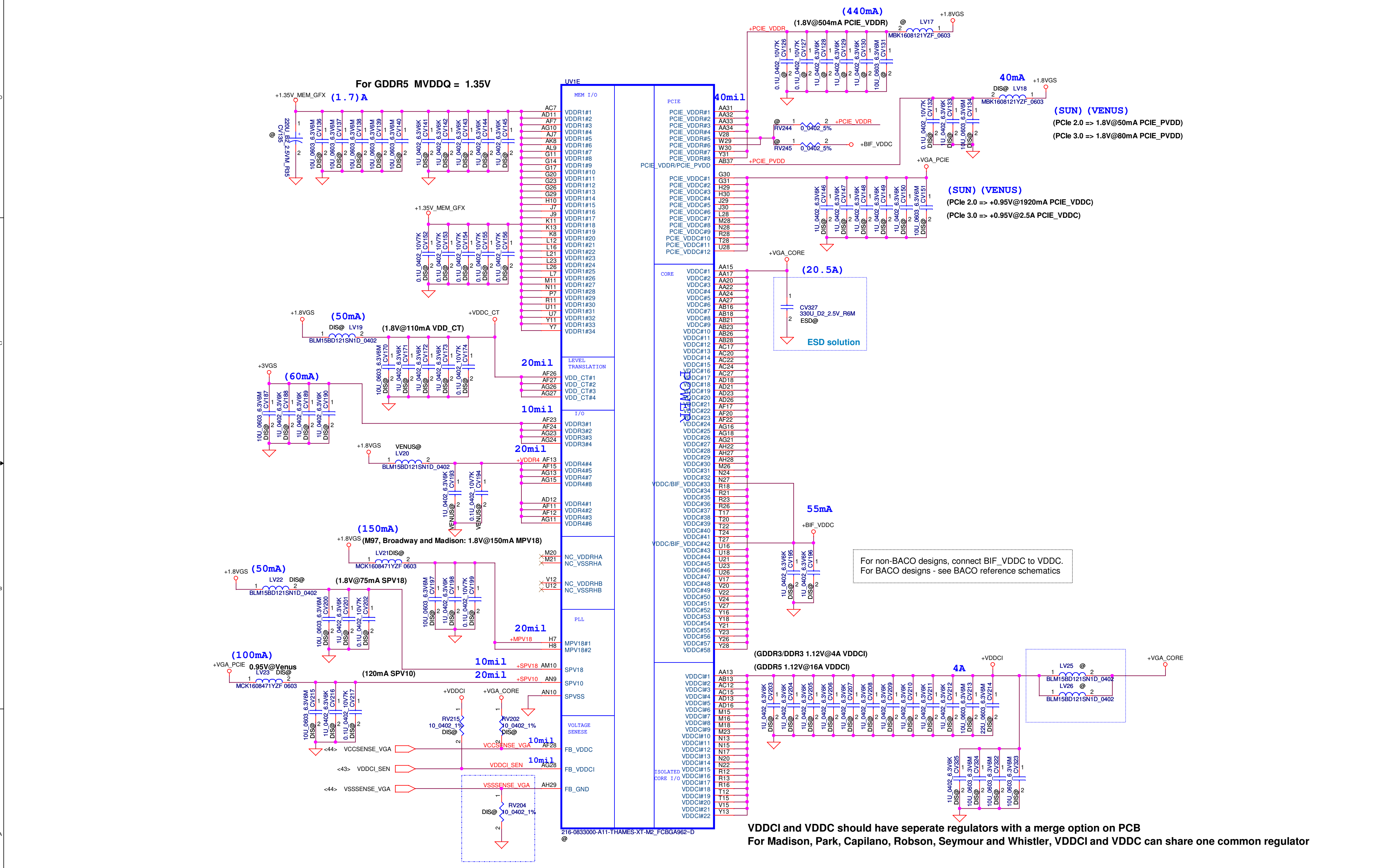


MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

Compal Electronics, Inc.

Title: ATI_Venus Pro_M2_PWR_GND

Size | Document Number: LA-9984P | Rev 1.0



VDDCI and VDDC should have seperate regulators with a merge option on PCB

For Madison, Park, Capilano, Robson, Seymour and Whistler, VDDCI and VDDC can share one common regulator

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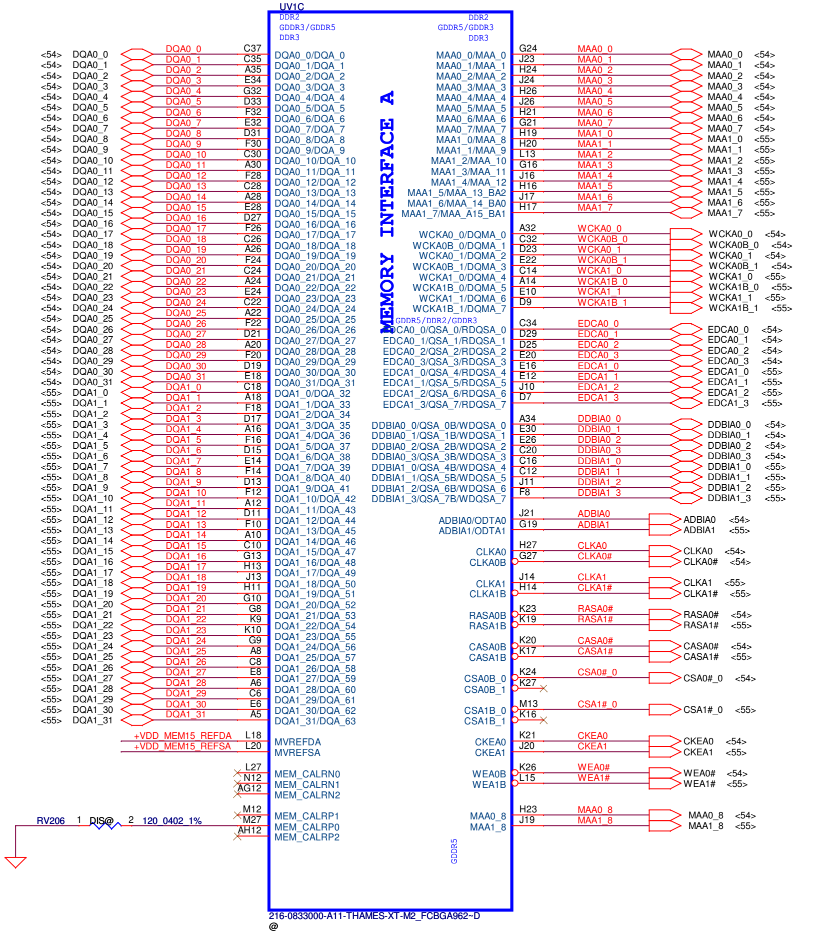
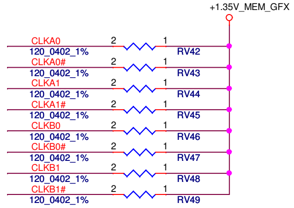
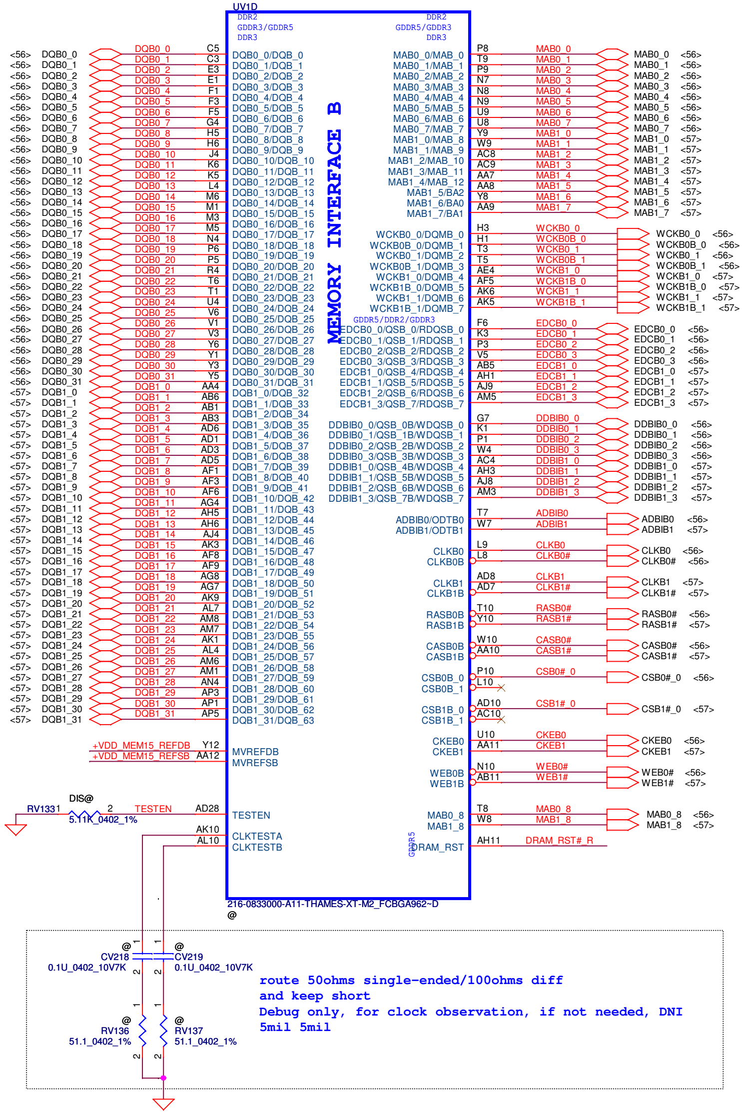


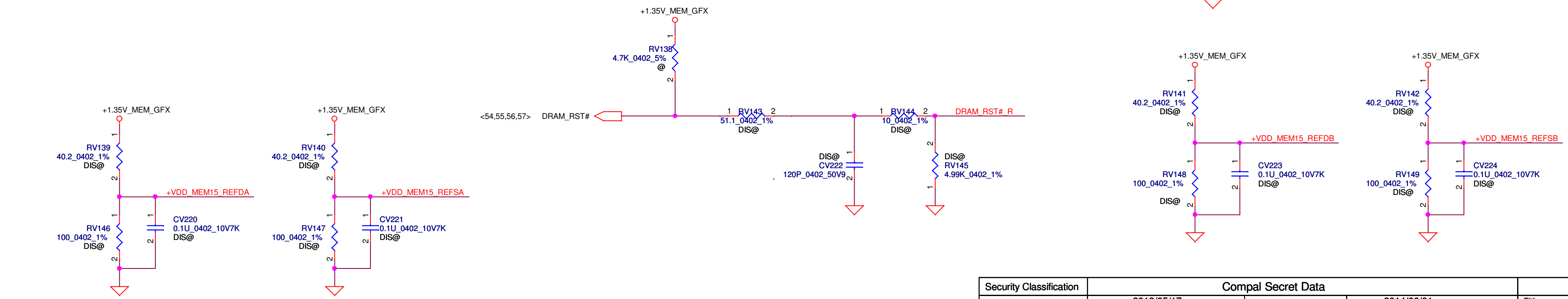
GDDR5 CMD Mapping Table

<0..31>	<32..63>	Memory
CMD12	CMD28	RAS#
CMD15	CMD31	CAS#
CMD5	CMD21	WE#
CMD0	CMD16	CS#
CMD8	CMD24	ABI#
CMD10	CMD26	A0_A10
CMD11	CMD27	A1_A9
CMD2	CMD18	A2_BA0
CMD1	CMD17	A3_BA3
CMD3	CMD19	A4_BA2
CMD4	CMD20	A5_BA1
CMD7	CMD23	A6_A11
CMD6	CMD22	A7_A8
CMD9	CMD25	A12_FRU
CMD14	CMD30	CKE#
CMD13	CMD29	RESET#





This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2



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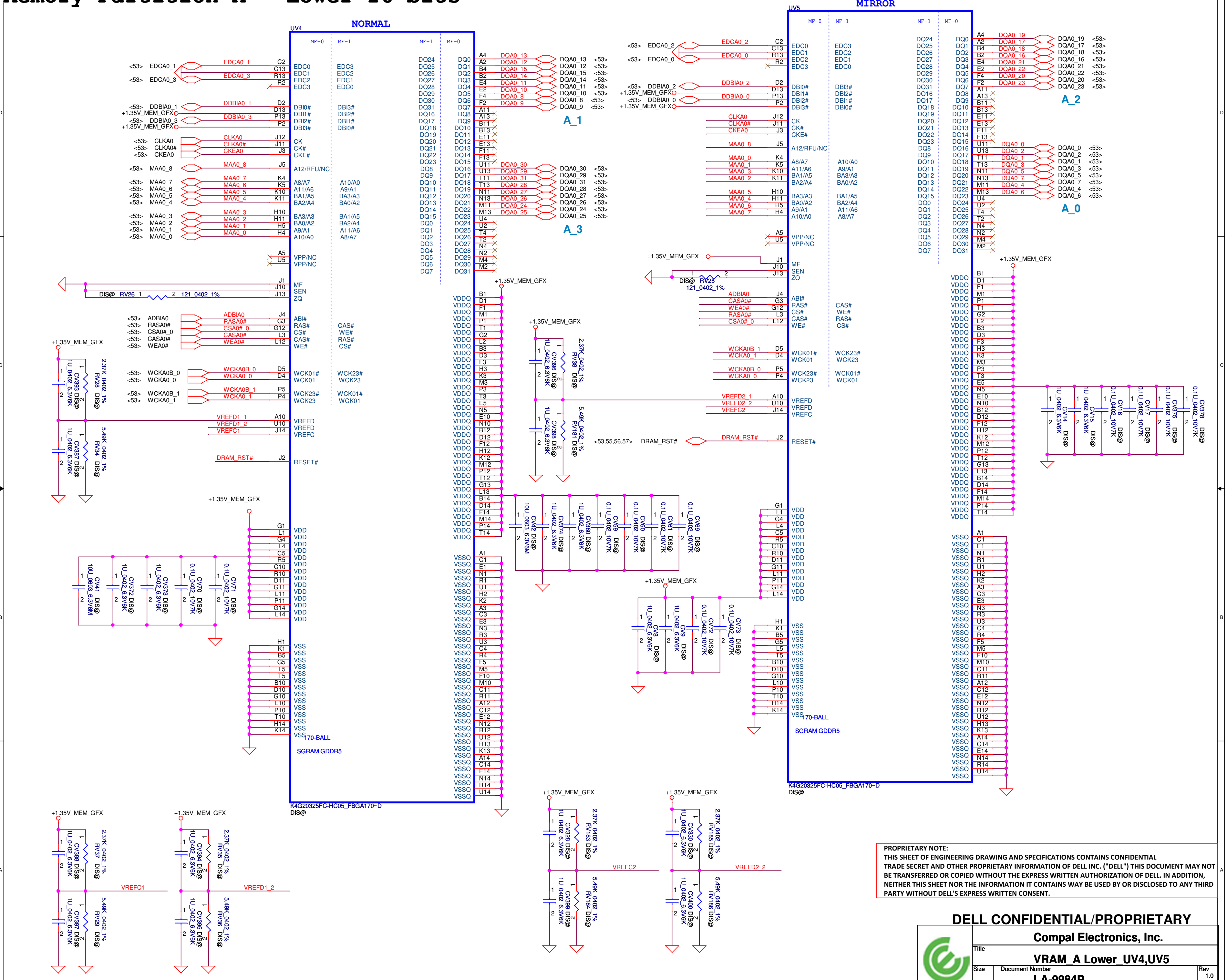
Memory Partition A - Lower 16 bits

64X32 GDDR5



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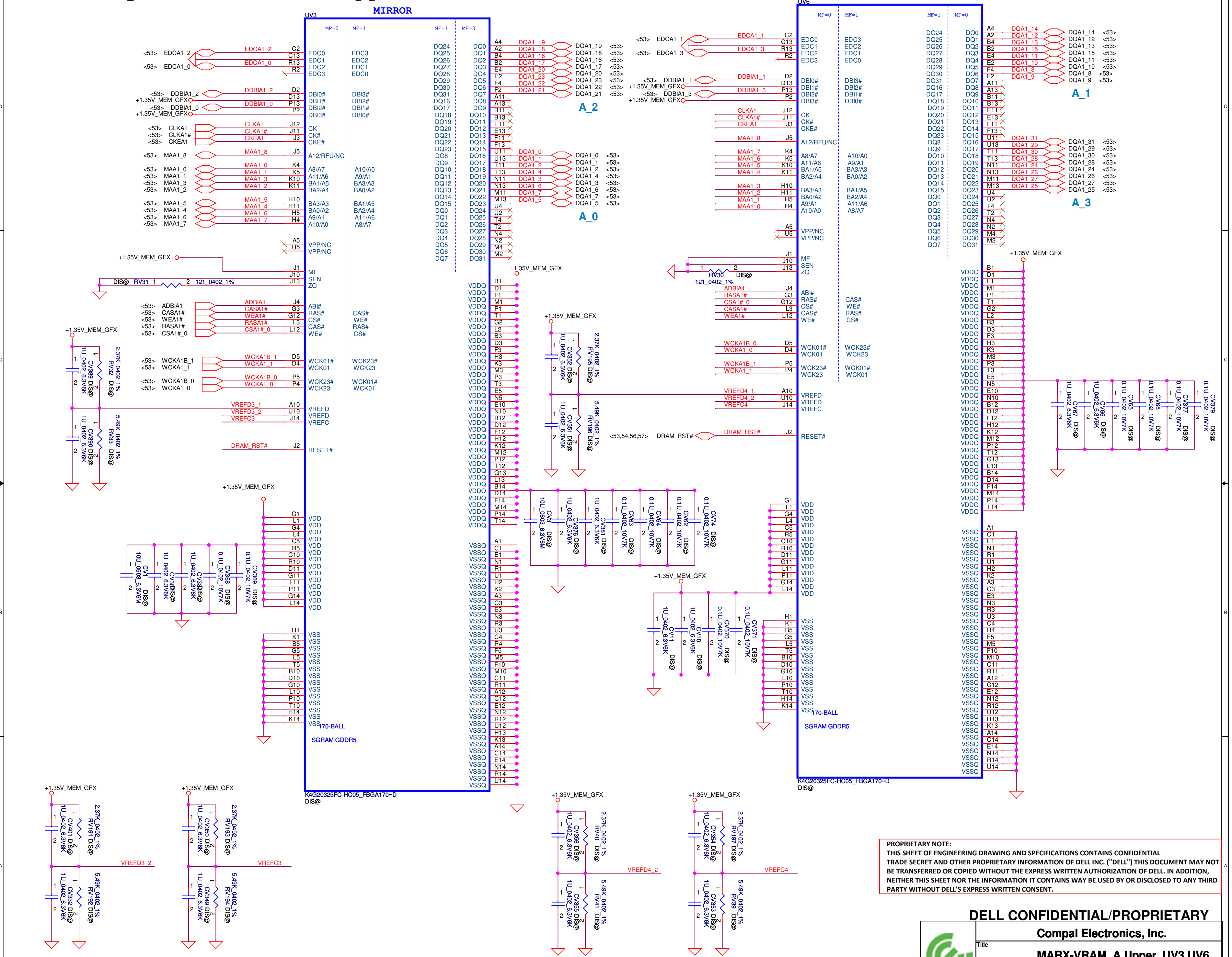
Memory Partition A - Upper 16 bits



Compal Electronics, Inc.

Title: MARX-VRAM_A Upper_UV3,UV6

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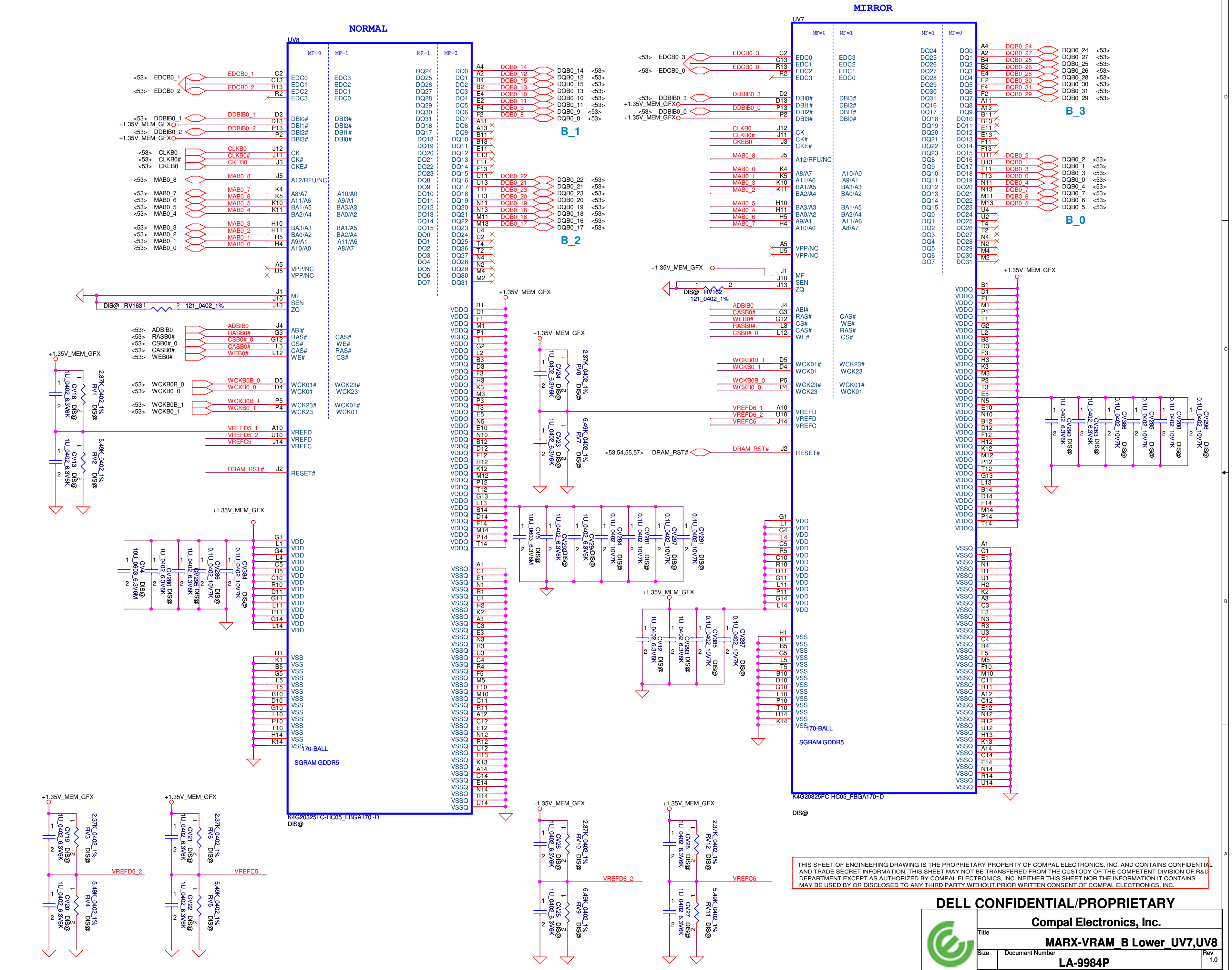
Memory Partition B - Lower 16 bits



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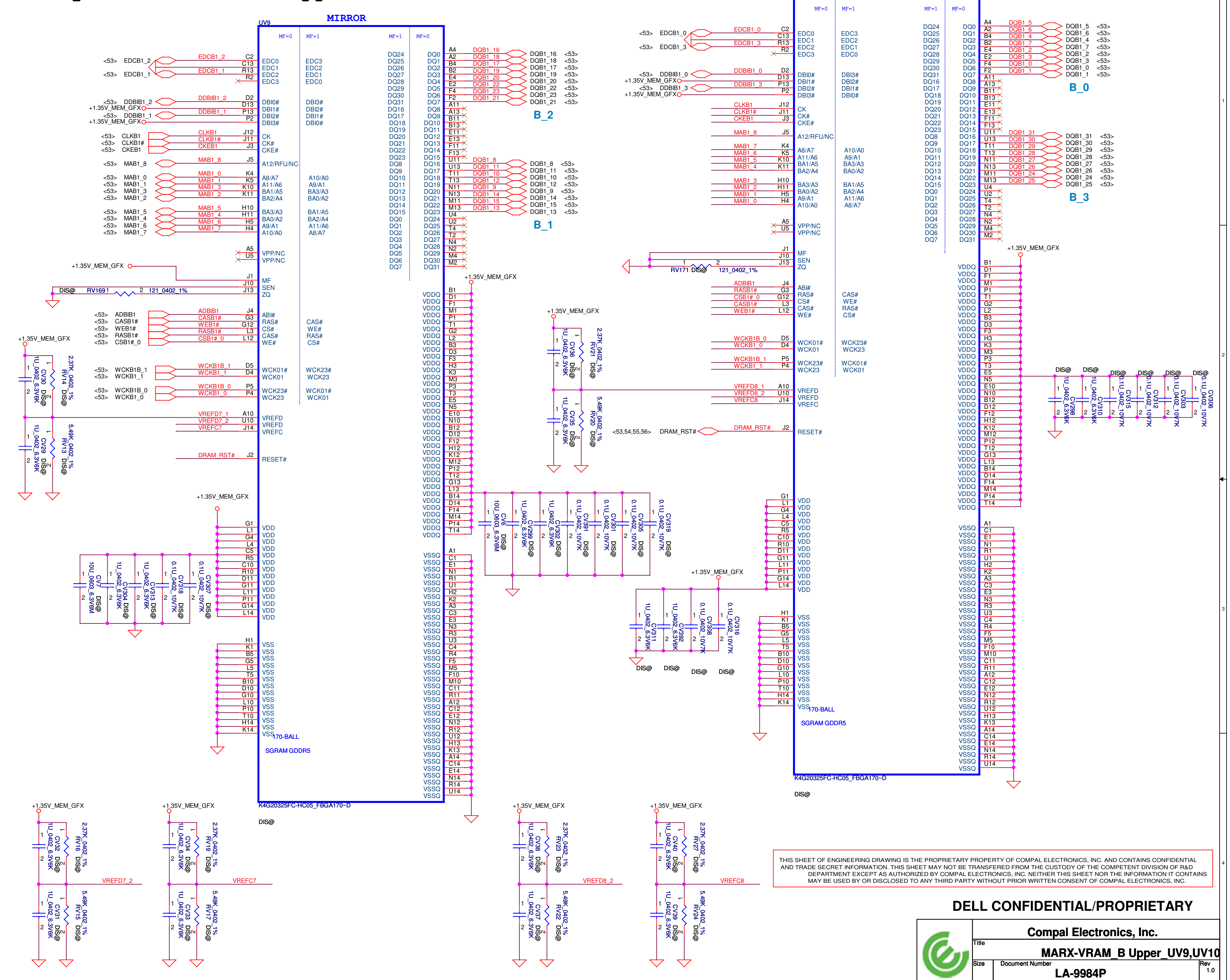
Memory Partition B - Upper 16 bits



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