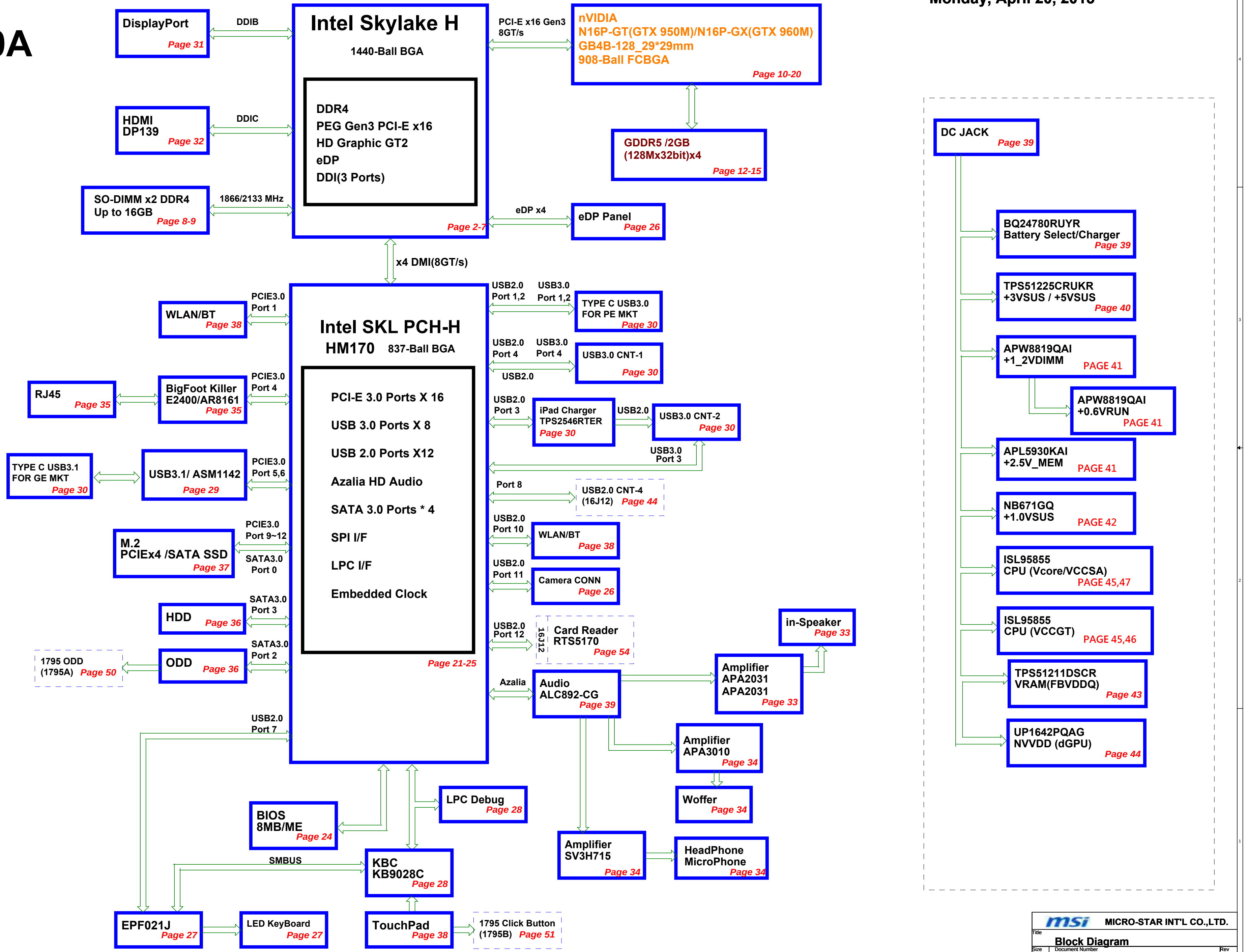
MS-16J5/MS-1795

Intel Skylake Mobile

Ver:0A

Monday, April 20, 2015



msi	MICRO-STAR INT'L CO.,LTD.
Title	Block Diagram
Size / Document Number	MS-16J5
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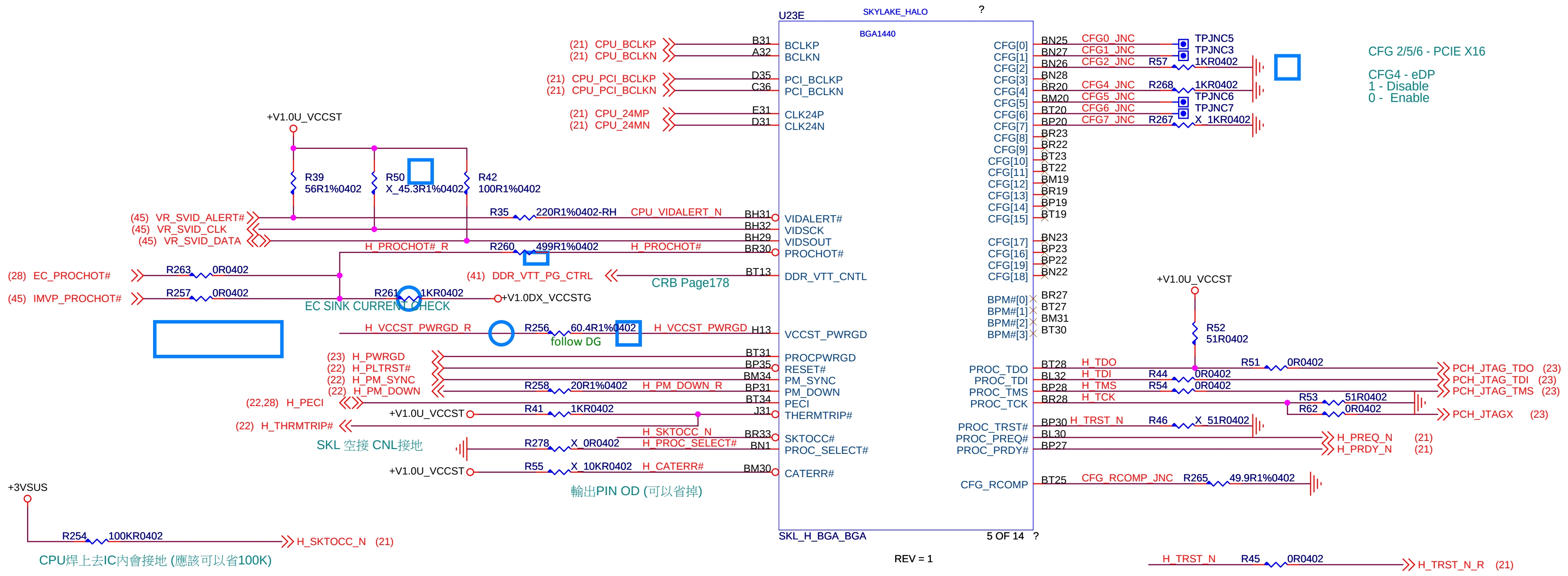
Date:	Sheet 1 of 55



MSR Privacy Bit Feature	
CFG3	1 = Debug capability is determined by IA32_Debug_Interface_MSR (0xC80) bit[0] setting 0 = IA32_Debug_Interface_MSR (0xC80) bit[0] default setting overridden

eDP Enable	
CFG4	1 = Disabled 0 = Enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

PCIE Express * Static X16 Lane Numbering Reversal	
CFG2	CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. 1 = Normal operation 0 = Lane numbers reversed.

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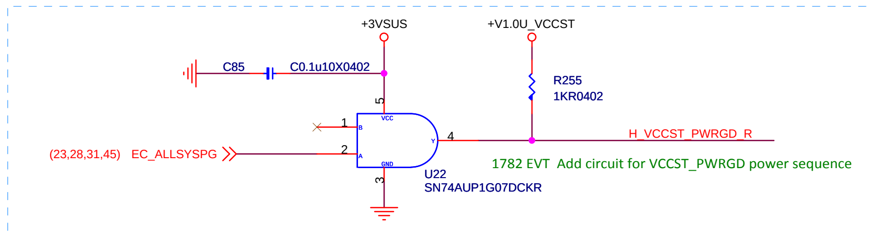
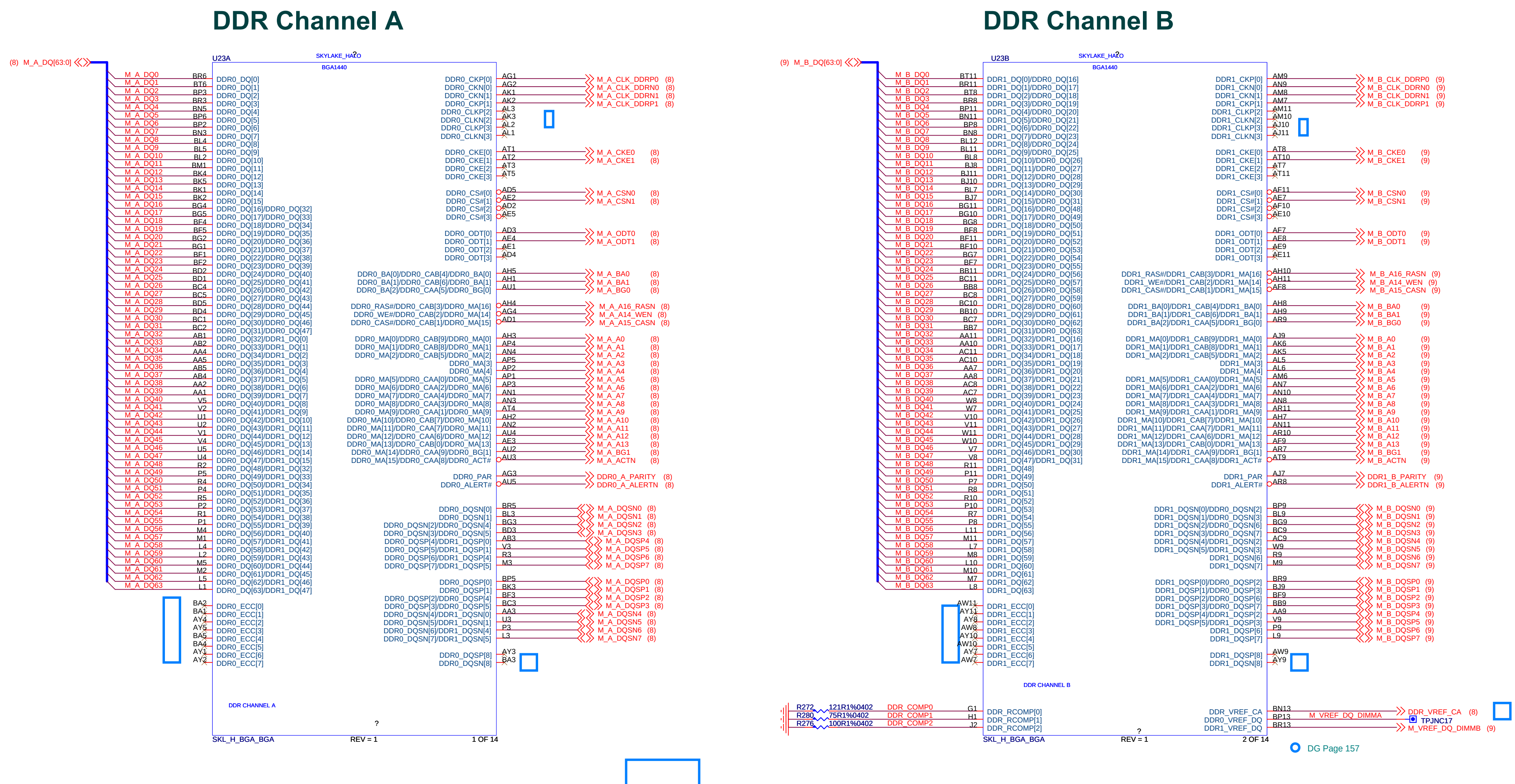
PCI Express* Bifurcation	
CFG[6:5]	00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*



MICRO-STAR INT'L CO.,LTD.

Title		
Skylake(HOST)		
Size: A3	Document Number: MS-16J5	Rev: 0A
Date: Tuesday, April 21, 2015	Sheet 2 of 55	

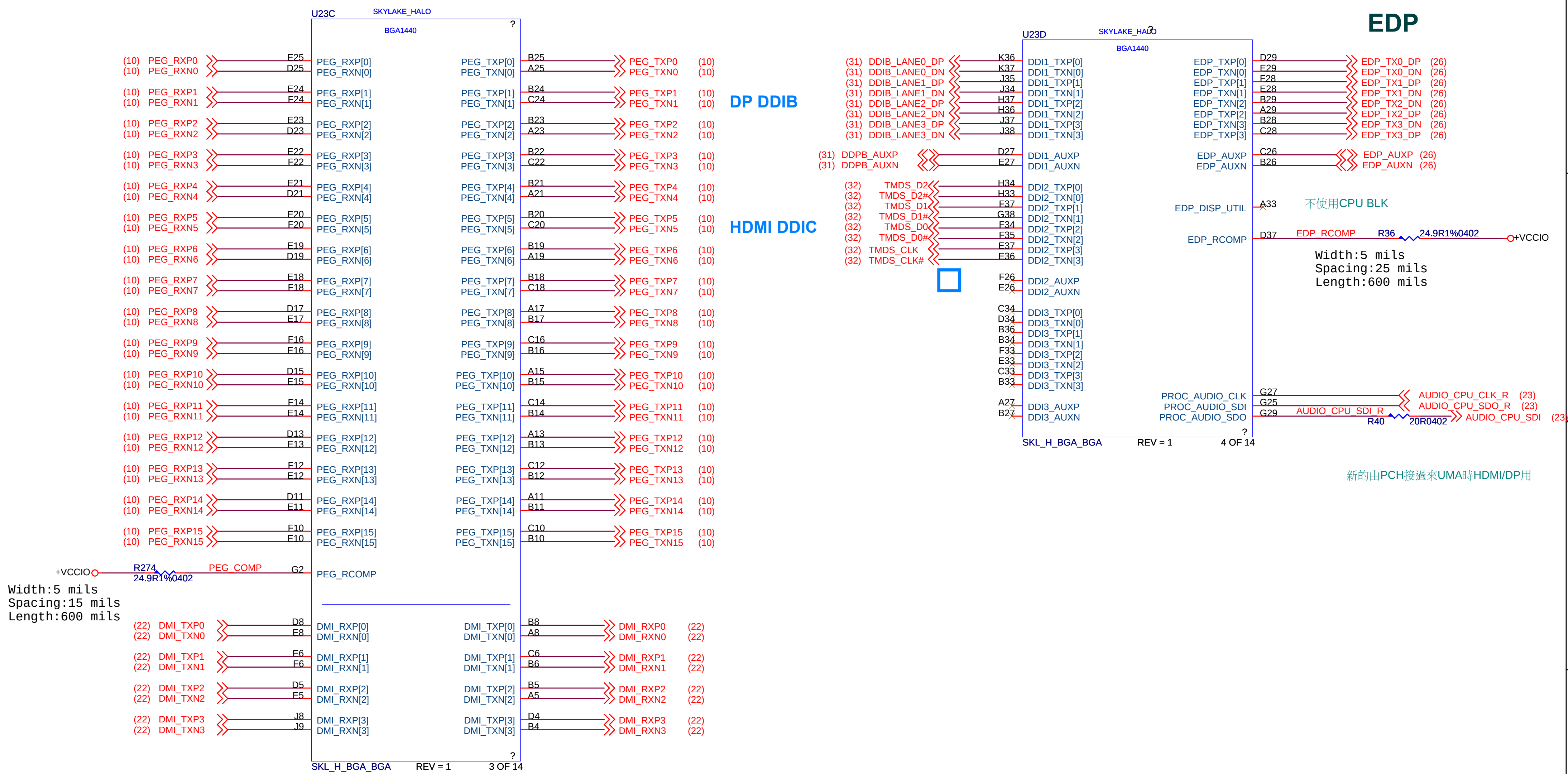


MICRO-STAR INT'L CO.,LTD.

Title: **Skylake(DDR4)**

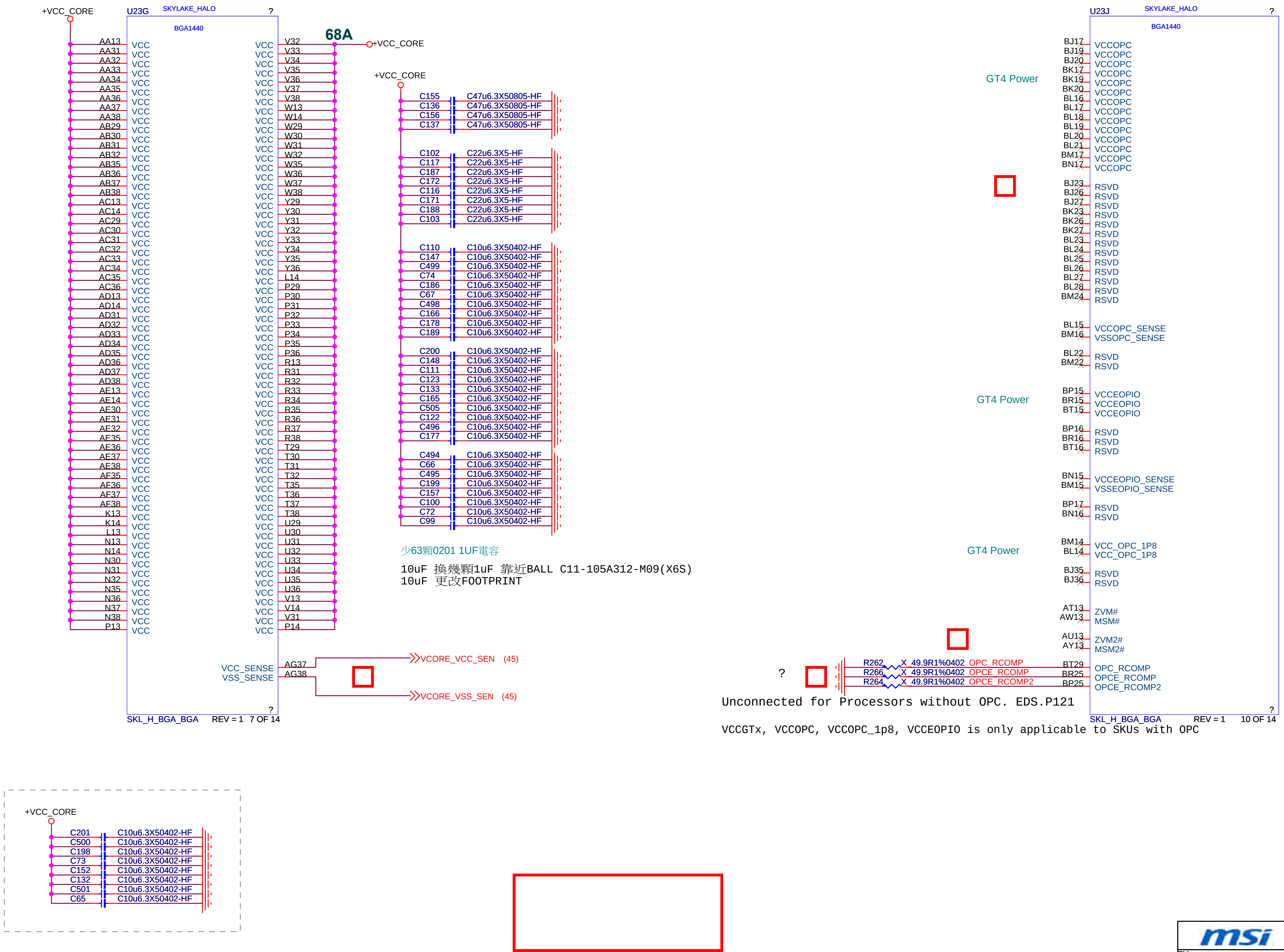
Size	Document Number	Rev
Custom	MS-16J5	0A

Date: Tuesday, April 21, 2015 Sheet 3 of 55



MICRO-STAR INT'L CO.,LTD.

Title	Skylake(DMI/Display)	
Size B	Document Number MS-16J5	Rev 0A
Date: Tuesday, April 21, 2015	Sheet 4 of 55	

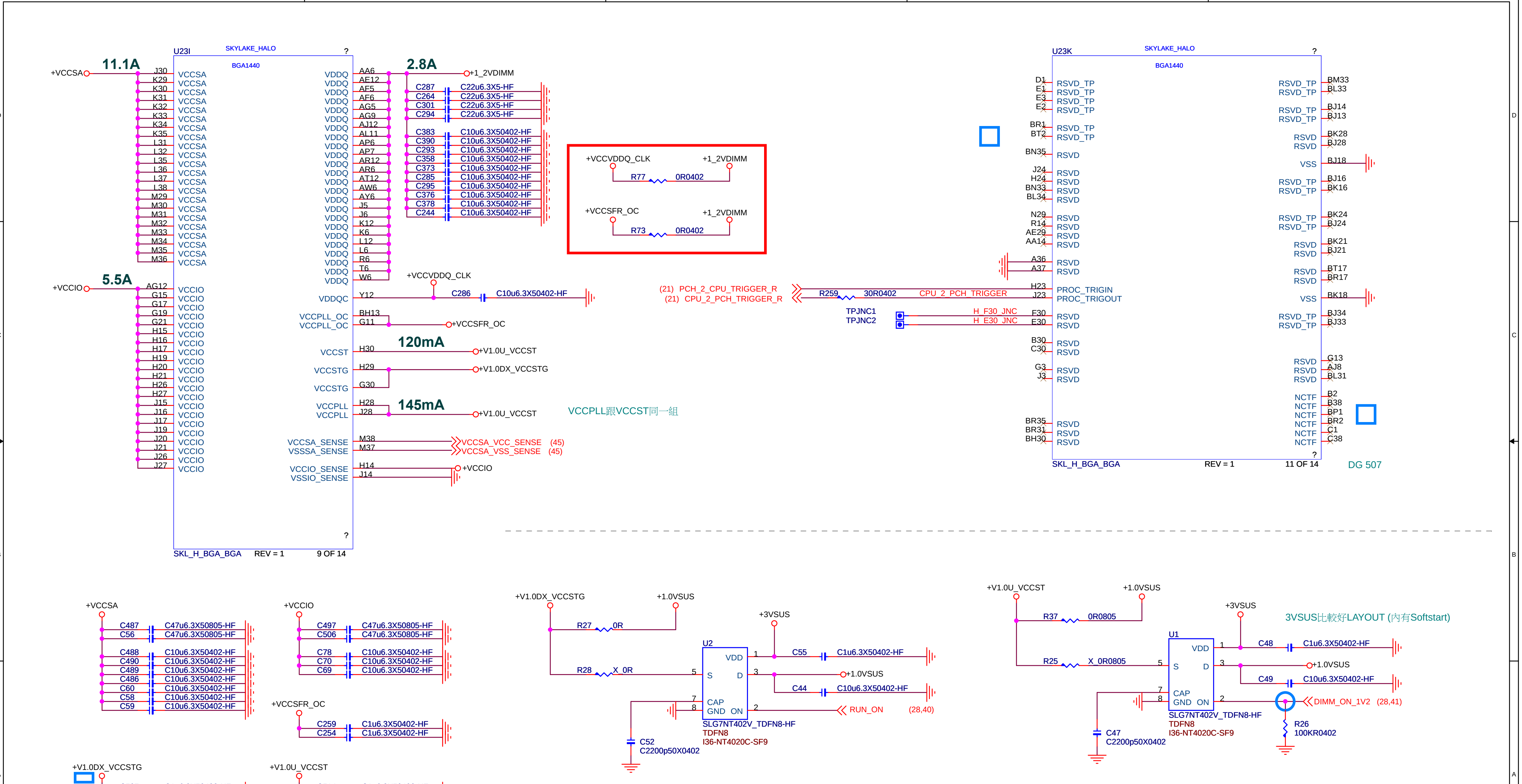


MICRO-STAR INT'L CO.,LTD.

Title: Skylake(Power1)

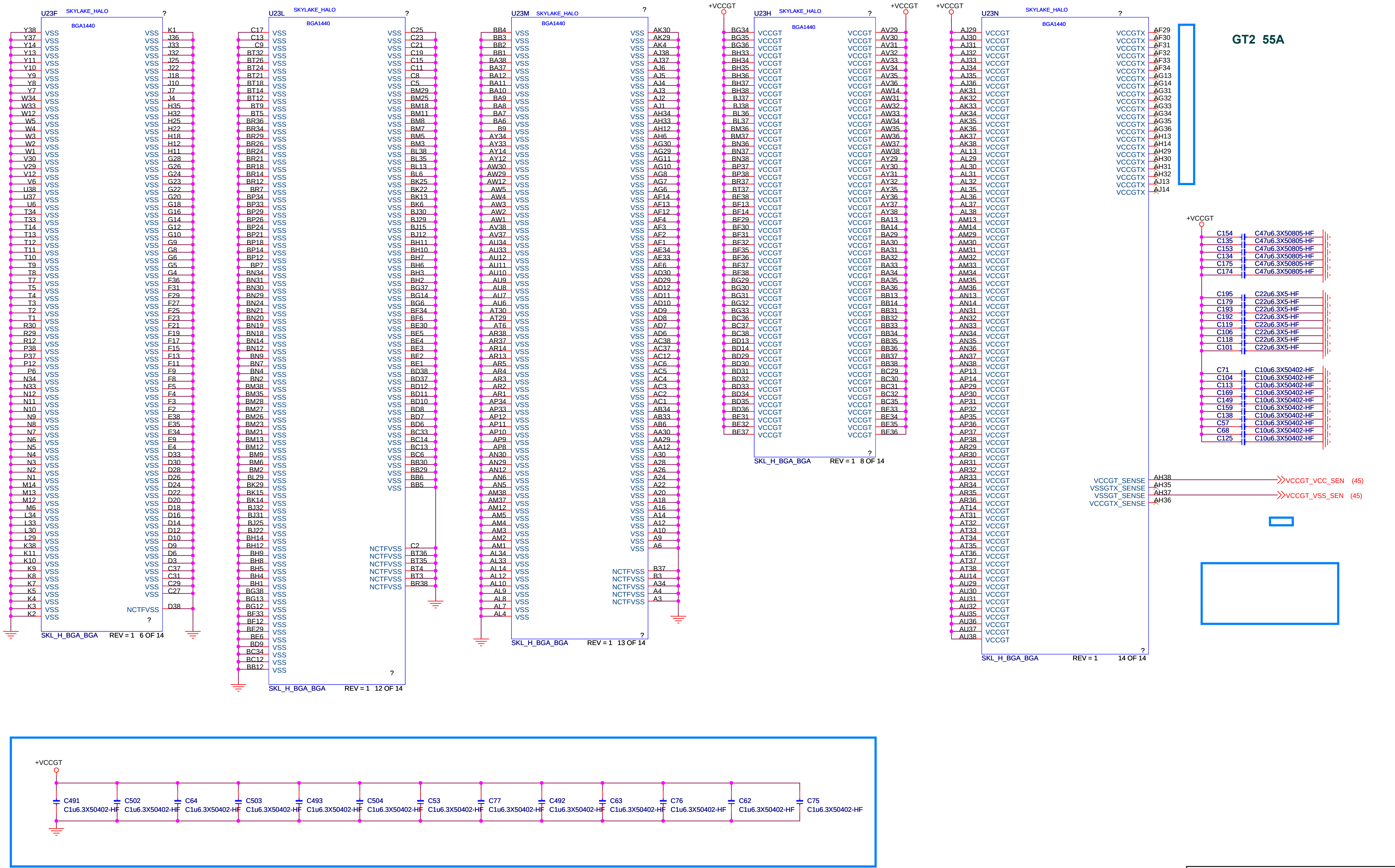
Size	Document Number	Rev
A3	MS-16J5	0A

Date: Tuesday, April 21, 2015 Sheet 5 of 55



msi MICRO-STAR INT'L CO.,LTD.

Title	Skylake(Power2)	
Size: Custom	Document Number: MS-16J5	Rev: 0A
Date: Tuesday, April 21, 2015	Sheet 6 of 55	



MICRO-STAR INT'L CO.,LTD.

Title	Skylake(Power3)
Size: Custom	Document Number: MS-16J5
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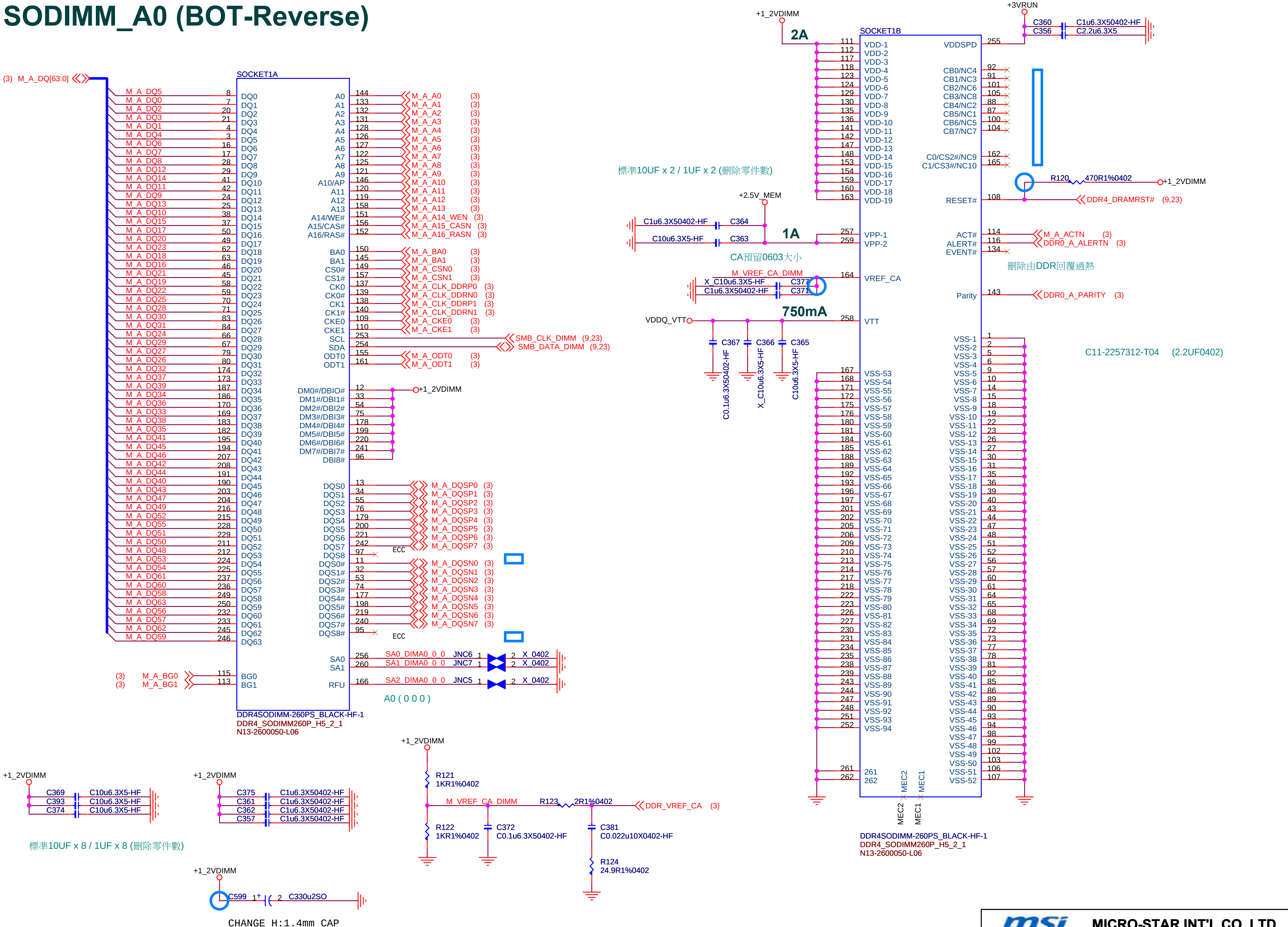
SODIMM_A0 (BOT-Reverse)



msi	MICRO-STAR INT'L CO.,LTD.
Title	DDR4_SODIMM_A0
Size: Custom	Document Number: MS-16J5
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Date:	Tuesday, April 21, 2015
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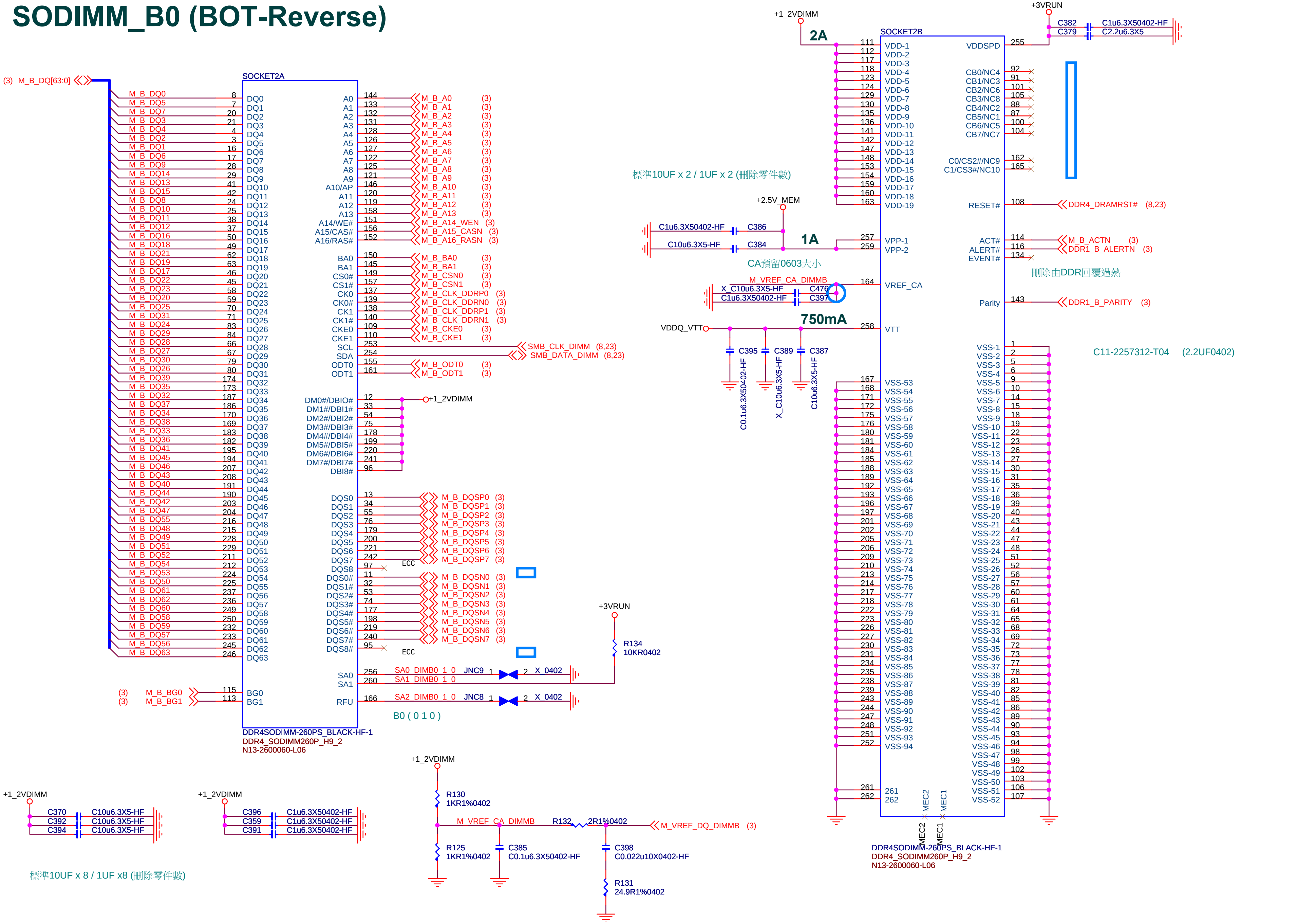
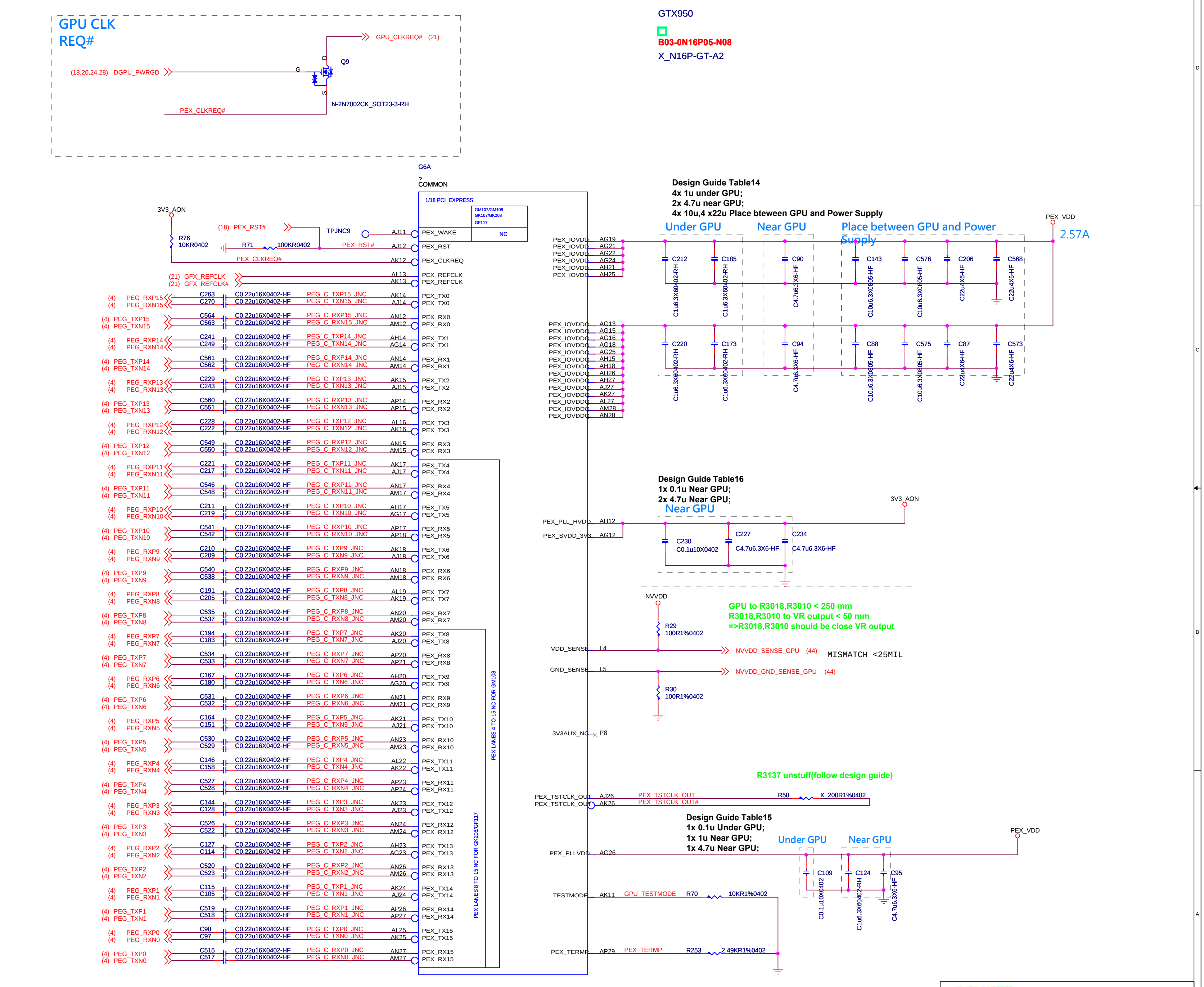
SODIMM_B0 (BOT-Reverse)



MICRO-STAR INT'L CO.,LTD.		
Title: DDR4_SODIMM_B0		
Size: Custom	Document Number: MS-16J5	Rev: 0A
Date: Tuesday, April 21, 2015	Sheet 9 of 55	

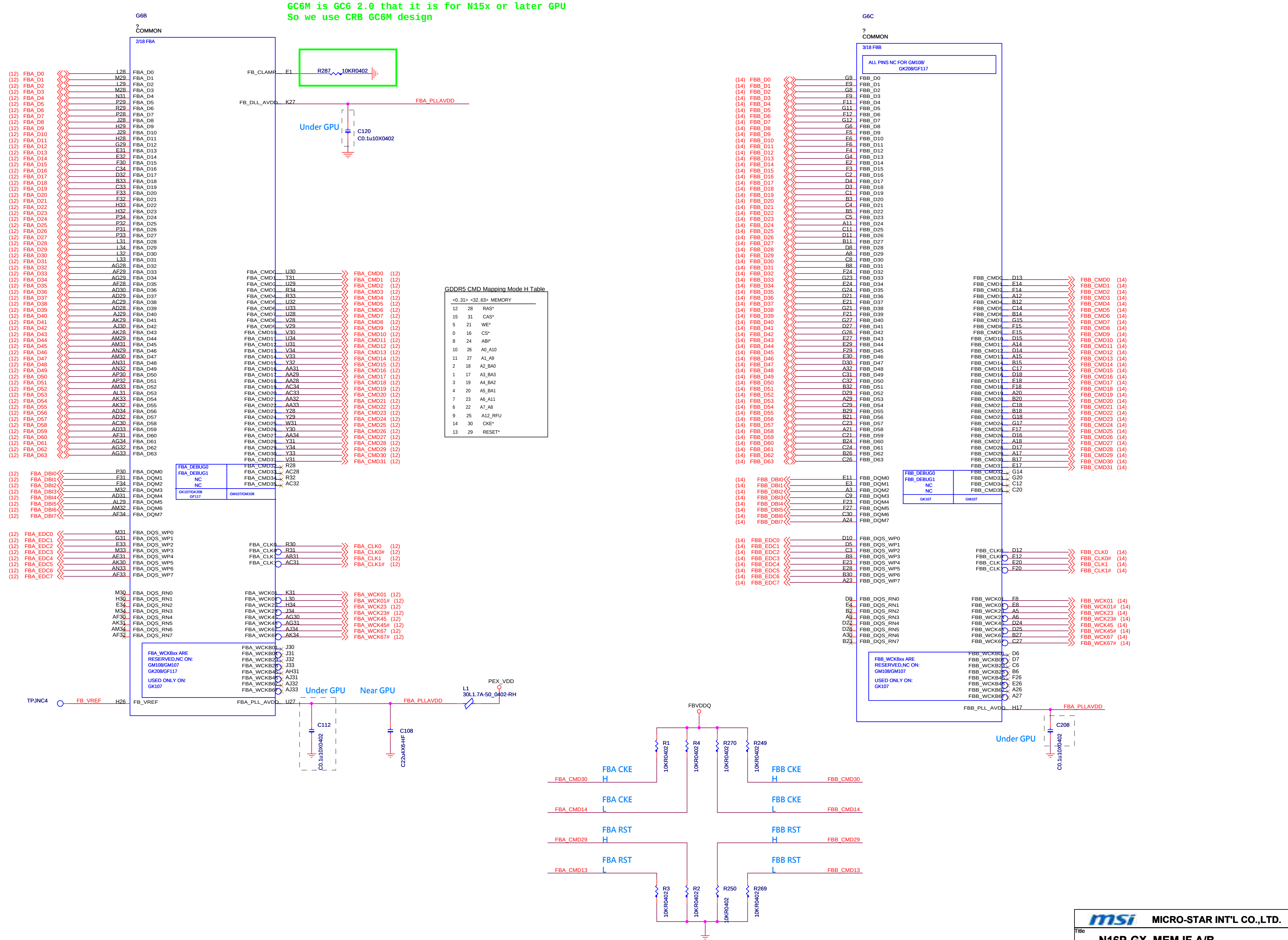
N16P-GX(PCI-Express Gen3 x16 Interface)



MICRO-STAR INT'L CO.,LTD.	
Title	N16P-GX_PCI-E Host
Size: Custom	Document Number: MS-16J5	Rev: 0A
Date: Tuesday, April 21, 2015	Sheet 10 of 55

N16P-GX(Frame Buffer Interface)

GC6M is GC6 2.0 that it is for N15x or later GPU
So we use CRB GC6M design



GDDR5 CMD Mapping Mode H Table

<0..31>	<32..63>	MEMORY
12	28	RAS*
15	31	CAS*
5	21	WE*
0	16	CS*
8	24	ABI*
10	26	A0_A10
11	27	A1_A9
2	18	A2_BA0
1	17	A3_BA3
3	19	A4_BA2
4	20	A5_BA1
7	23	A6_A11
6	22	A7_A8
9	25	A12_RFU
14	30	CKE*
13	29	RESET*

msi	MICRO-STAR INT'L CO.,LTD.
Title	N16P-GX_MEM IF A/B
Size Custom	Document Number MS-16J5
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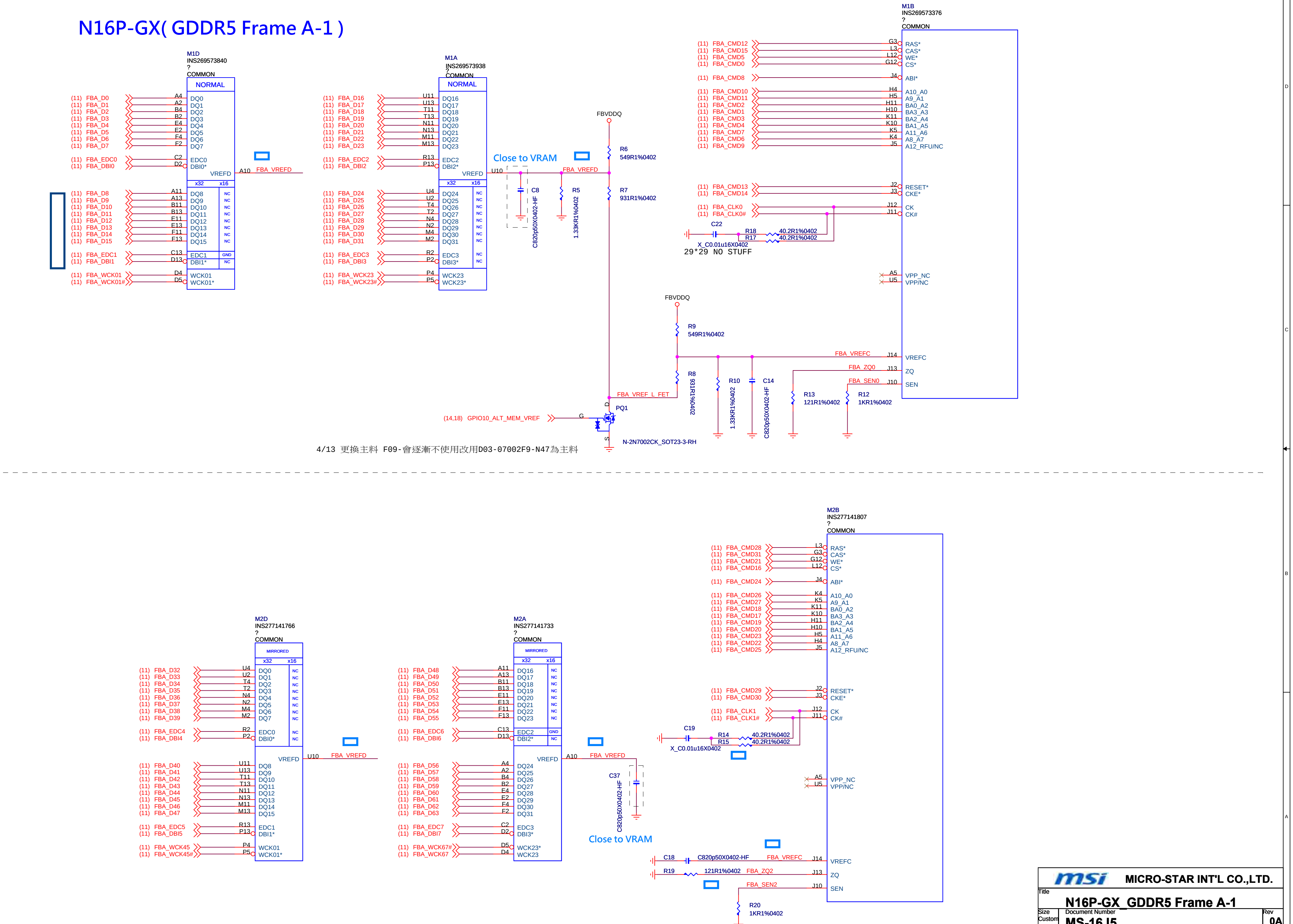
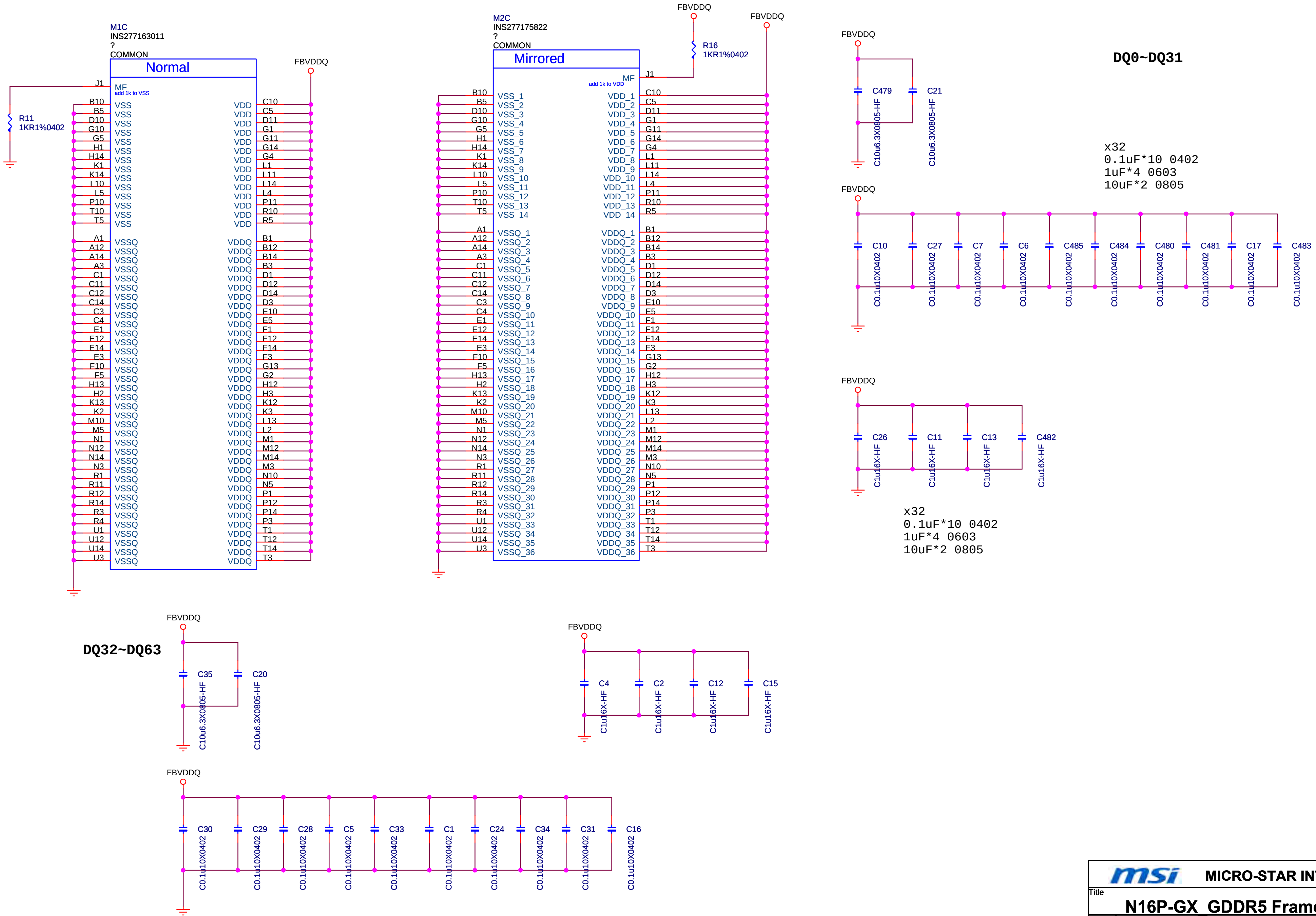
N16P-GX(GDDR5 Frame A-1)



MICRO-STAR INT'L CO.,LTD.	
Title	N16P-GX_GDDR5 Frame A-1
Size: Custom	Document Number: MS-16J5 — Rev 0A
Date: Tuesday, April 21, 2015	Sheet 12 of 55

N16P-GX(GDDR5 Frame A-2)



MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX_GDDR5 Frame A-2	
Size A3	Document Number MS-16J5	Rev 0A
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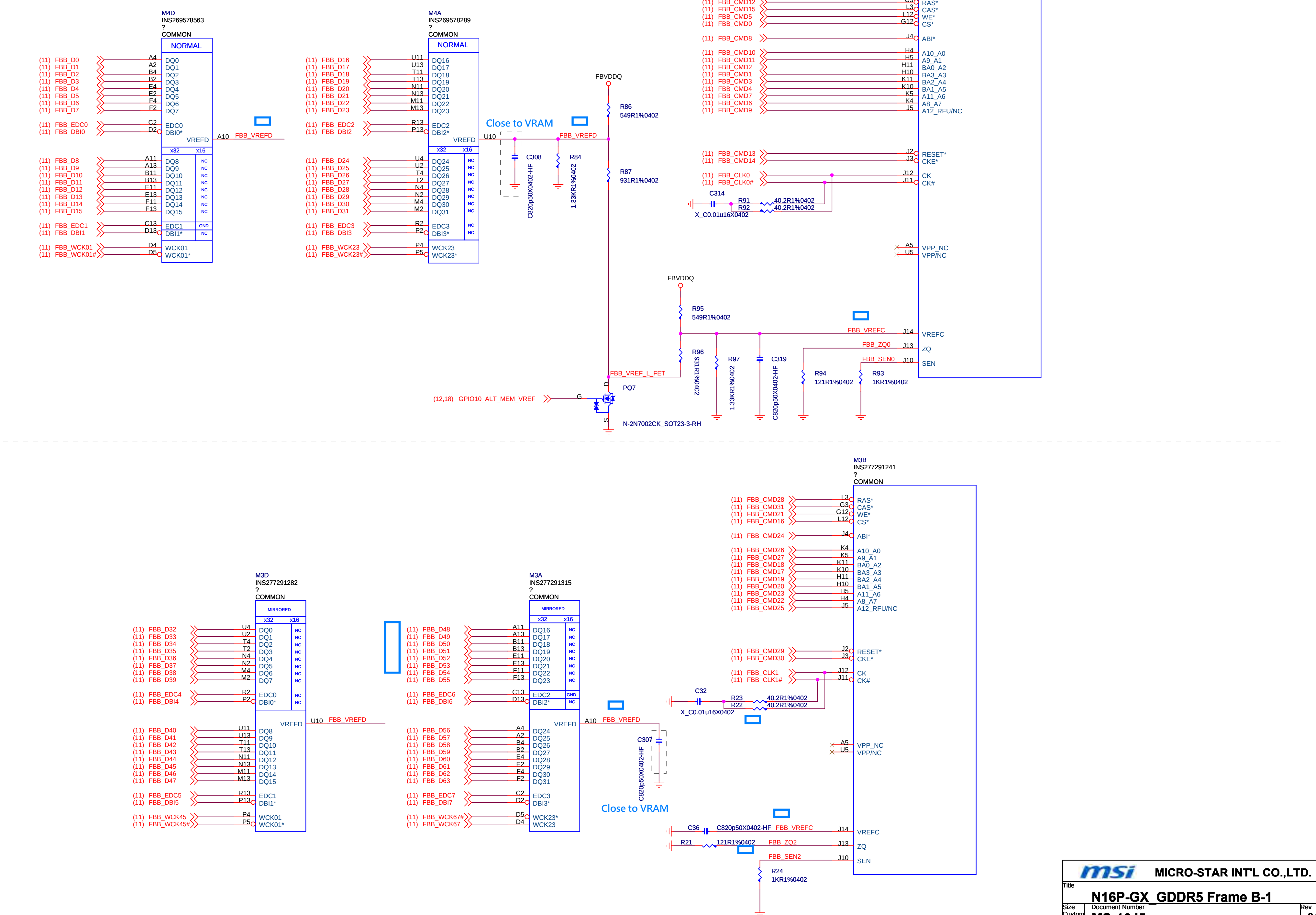
N16P-GX(GDDR5 Frame B-1)



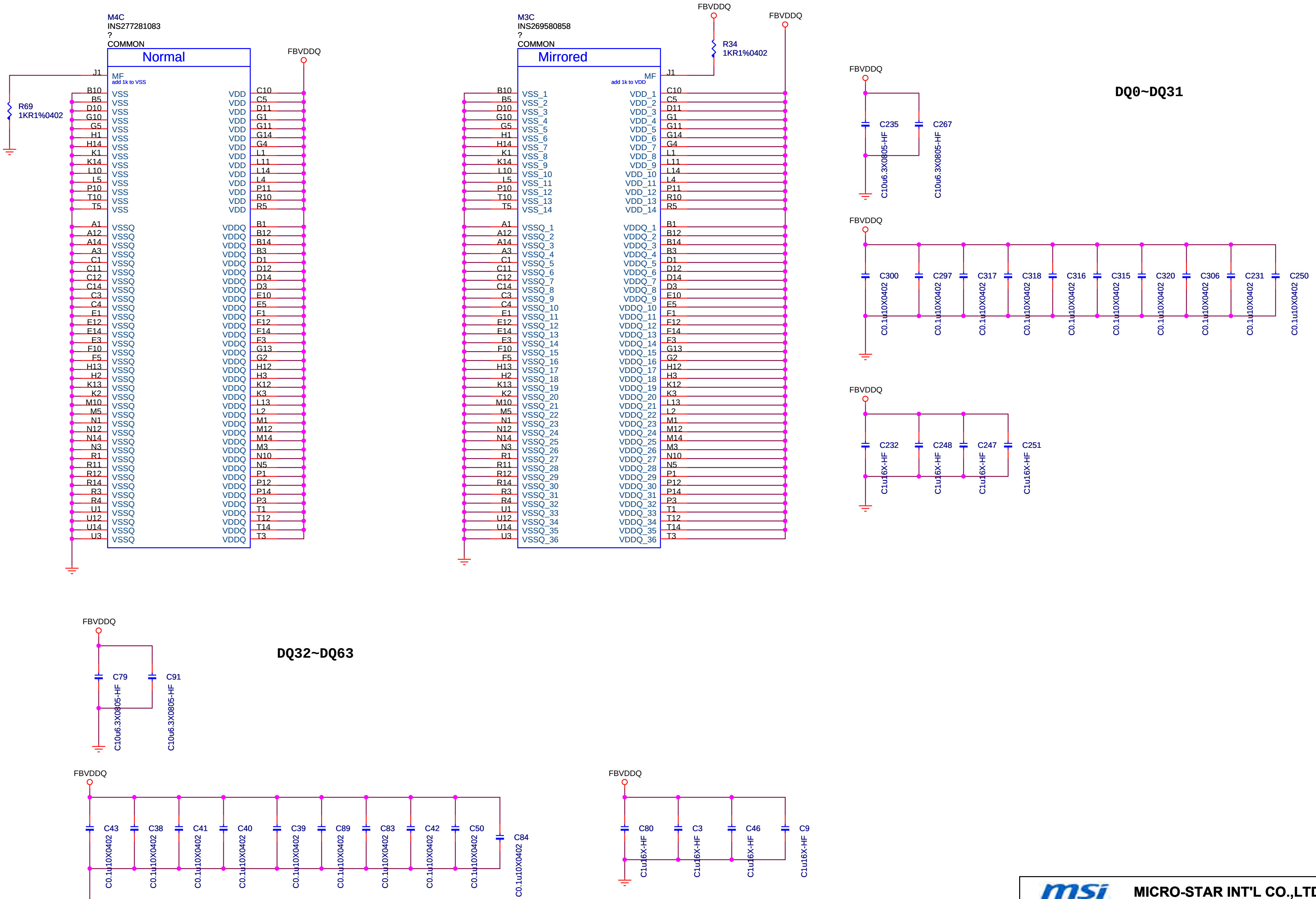
MICRO-STAR INT'L CO.,LTD.

Title: N16P-GX_GDDR5 Frame B-1

Size: Custom | Document Number: MS-16J5 | Rev: 0A

Date: Tuesday, April 21, 2015 | Sheet 14 of 55

N16P-GX(GDDR5 Frame B-2)



MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX_GDDR5 Frame B-2
Size A3	Document Number MS-16J5
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Date:	Tuesday, April 21, 2015
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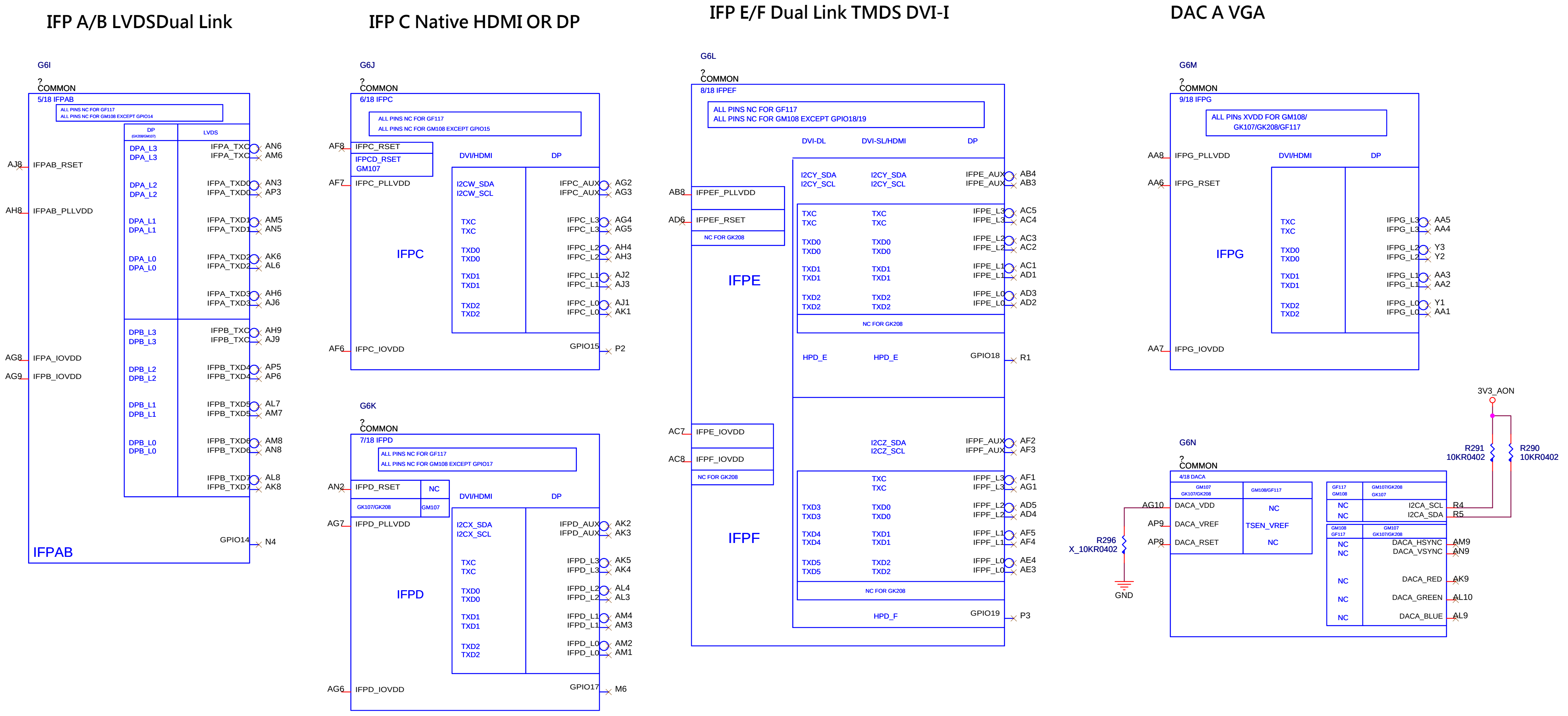
N16P-GX(Display IF)



MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX_Display IF
Size	Custom
Document Number	MS-16J5
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Date:	Tuesday, April 21, 2015
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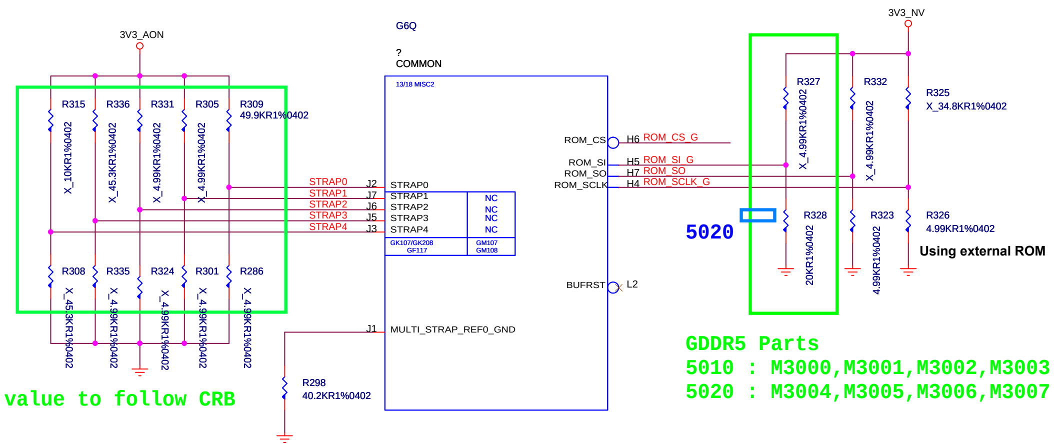
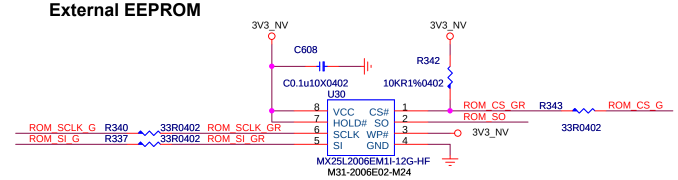
ROM, MULTI-LEVEL STRAPS



Modify R value to follow CRB

GDDR5 Parts
5010 : M3000,M3001,M3002,M3003
5020 : M3004,M3005,M3006,M3007

External EEPROM



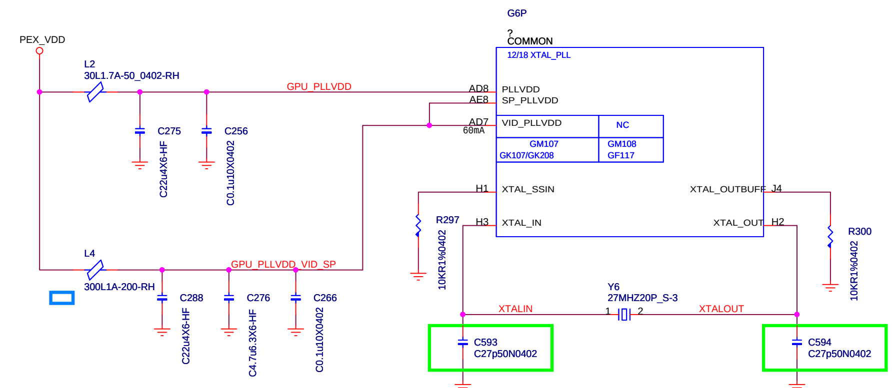
M31-2006E02-M24

DEFAULT SETTING

BOT 記得轉階層

ROM_S2	Samsung 128Mx32bit R11-0203T12-W08 X_20KR1%0402	V_BOT5	5020 M12-4132525-S02 X_K4G41325FC-HC03
ROM_H2	Hynix 128Mx32bit R11-0153T12-W08 X_15KR1%0402	V_BOT4	5020 M12-5GC4H05-H23 X_H5GC4H24MFR-T2C
ROM_M2	Micron 128Mx32bit R11-2492T12-W08 X_24.9KR1%0402	V_BOT6	5020 M12-4032B05-E59 X_EDW4032BABG-60-F-HF
ROM_H3	Hynix 128Mx32bit R11-3482T12-W08 X_34.8KR1%0402	V_BOT7	5020 M12-5GC4H65-H23 X_H5GC4H24AJR-T2C

ROM_SI	RAM_CFG[3:0]		
	Micron GDDR5 : M12-4032B05-E59	0x4 25K PD	Micron 128Mx32bit
	Samsung GDDR5 : M12-4132525-S02 V	0x3 20K PD	Samsung 128Mx32bit
	Hynix GDDR5 : M12-5GC4H05-H23	0x2 15K PD	Hynix 128Mx32bit
	Hynix GDDR5 : H5GC4H24AJR-T2C V	0x6 35K PD	
ROM_SO	DEVID_SEL PCIE_CFG SMB_ALT_ADDR VGADEVICE	5K PD	
ROM_SCLK	SOR_EXposed[3:0]	5K PD	
STRAP0		50K PU 3V3_AON	
STRAP1		Reserved	
STRAP2		Reserved	
STRAP3		Reserved	
STRAP4		Reserved	



C3438 and C3439 change to 27pF for SA

	GND	3V3
5K	0000	1000
10K	0001	1001
15K	0010	1010
20K	0011	1011
25K	0100	1100
30K	0101	1101
35K	0110	1110
45K	0111	1111
	PD	PU

MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX_ROM & HW Straps	
Size Custom	Document Number MS-16J5	Rev 0A
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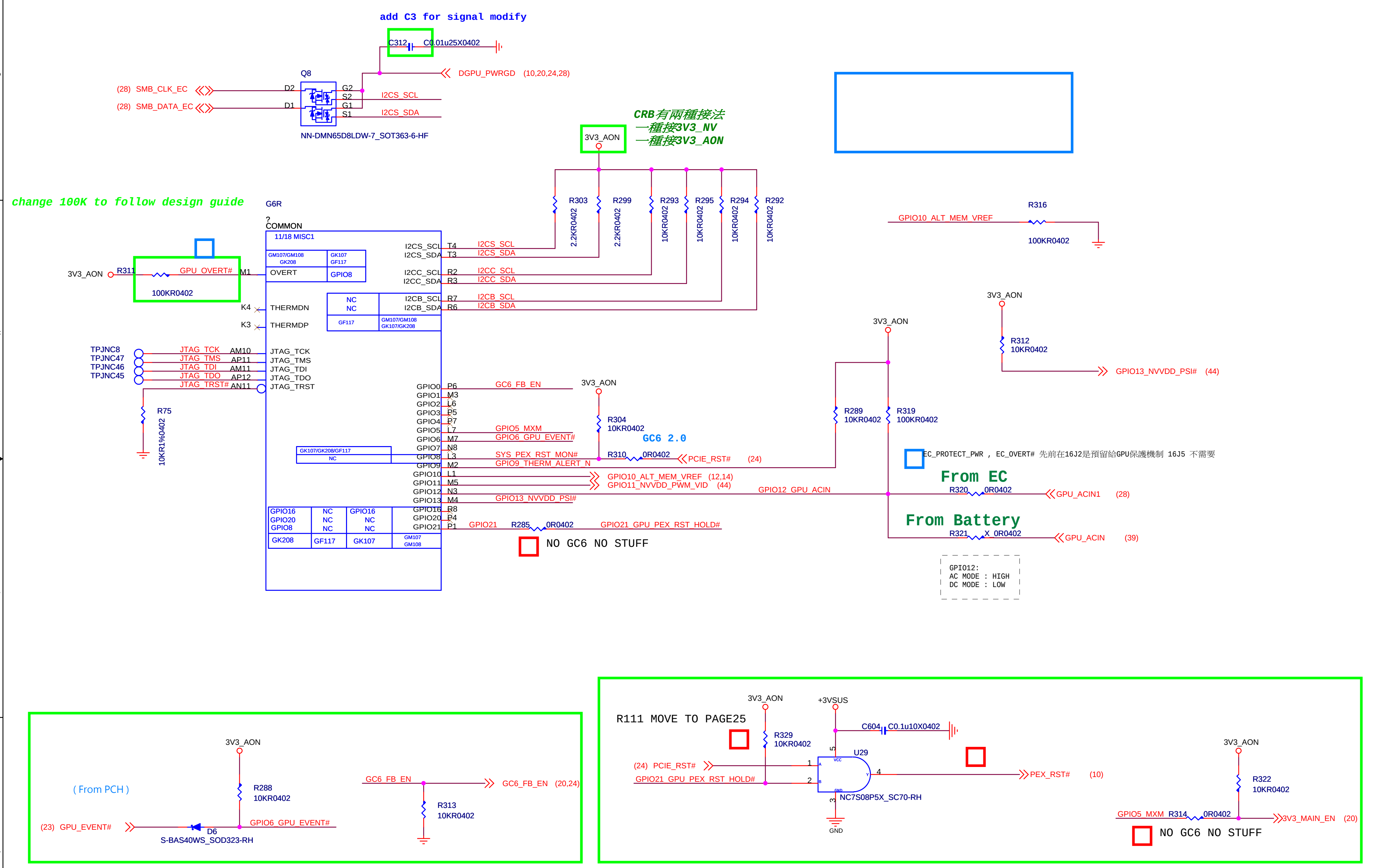

MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX_Thermal & GPIO	
Size: Custom	Document Number: MS-16J5	Rev: 0A
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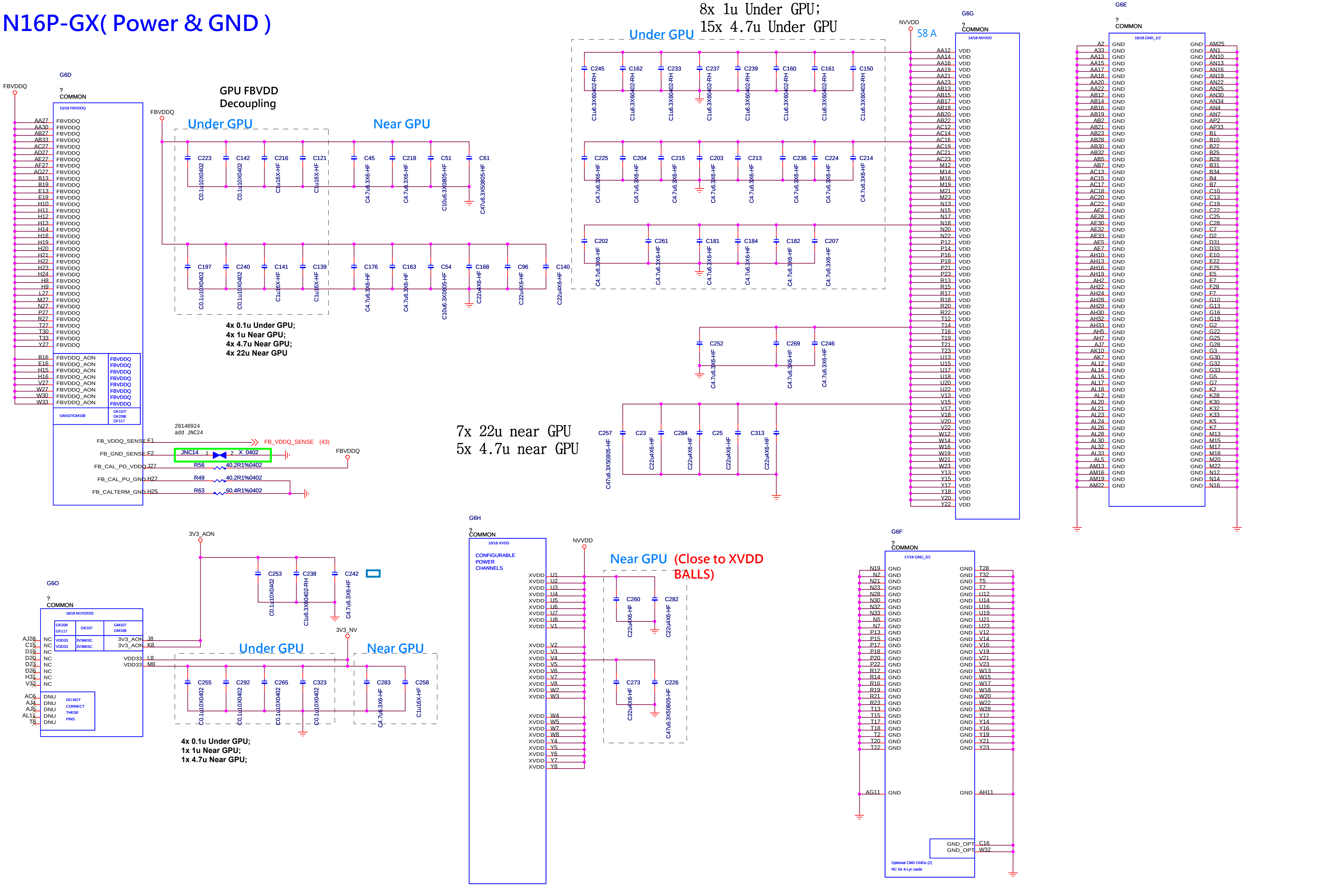
N16P-GX(Power & GND)



MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX_Power & GND
Size: Custom	Document Number: MS-16J5
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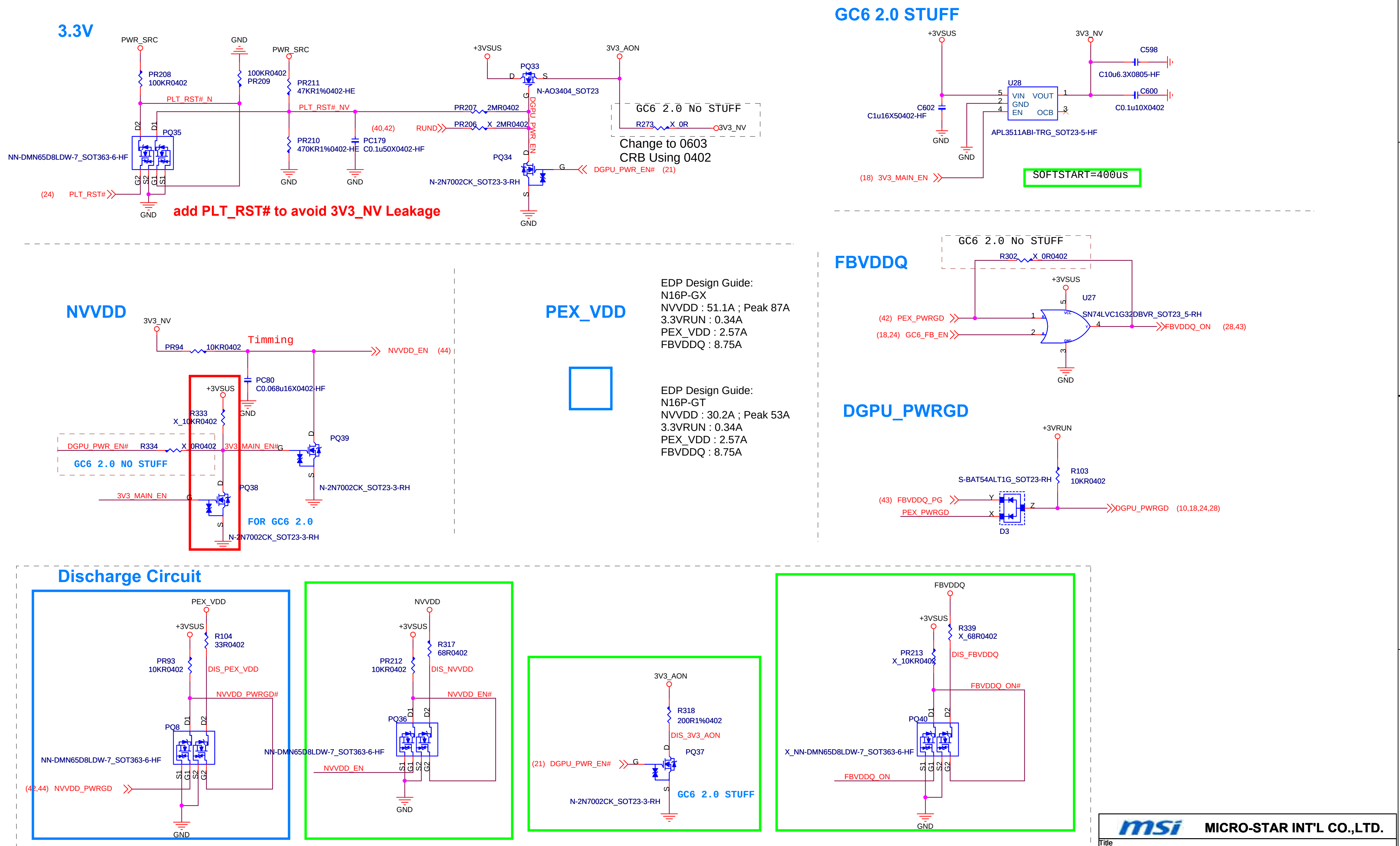
N16P-GX(Power Control)

nVIDIA Power Sequence Control

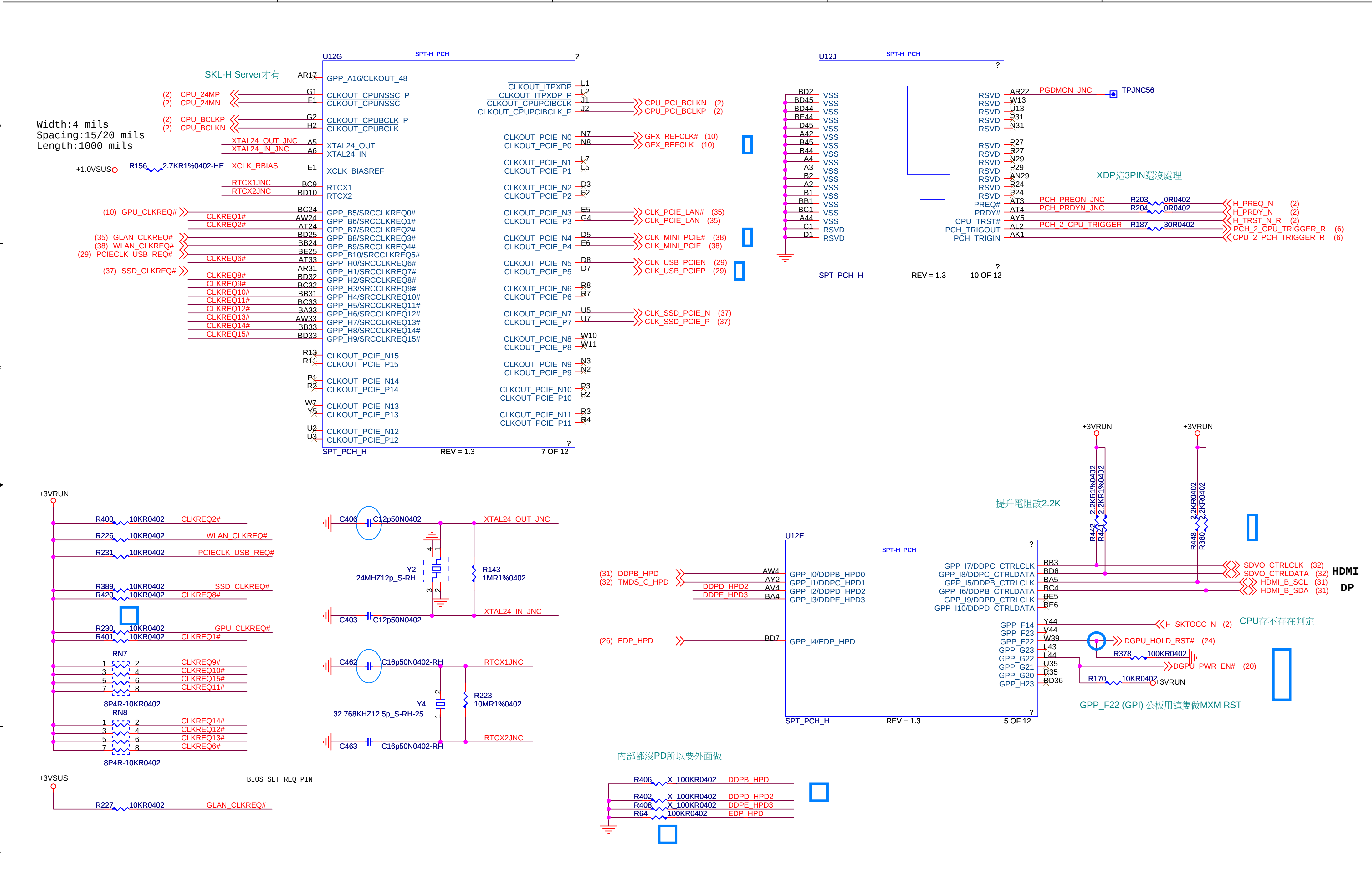
3V3_AON -> 3V3_NV -> NVVDD ->PEX_VDD -> FBVDDQ -> DGPUPWRGD



4/13更換料號
D03-7002D10-D07 轉到 D03-65D8L09-D07

MICRO-STAR INT'L CO.,LTD.

Title	N16P-GX_Power Control	
Size Custom	Document Number MS-16J5	Rev 0A
Date: Tuesday, April 21, 2015	Sheet 20 of 55	



MICRO-STAR INT'L CO.,LTD.

Title	PCH_1(CLK/DDI)	
Size A3	Document Number MS-16J5	Rev 0A
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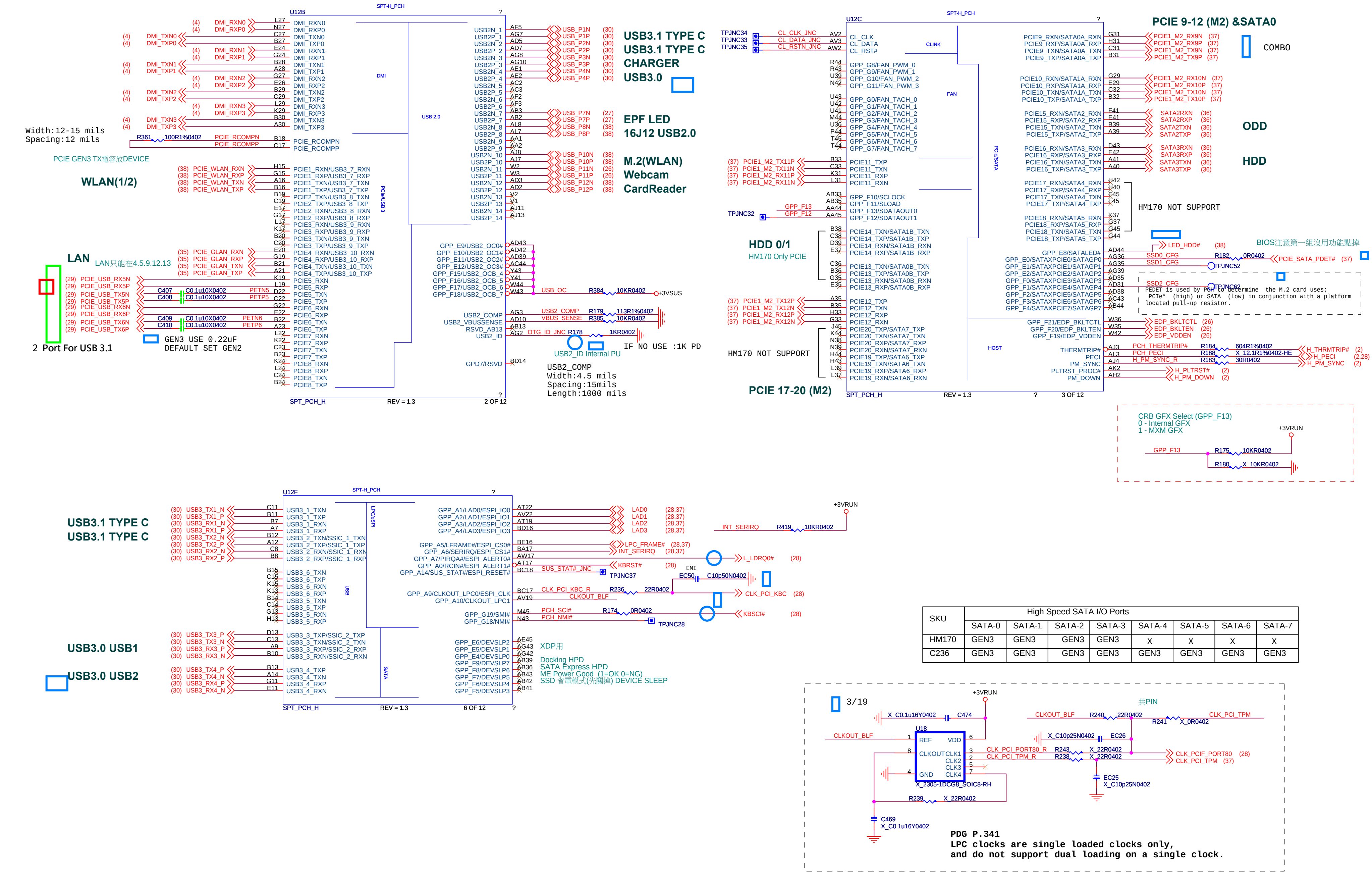

SKU	High Speed SATA I/O Ports							
	SATA-0	SATA-1	SATA-2	SATA-3	SATA-4	SATA-5	SATA-6	SATA-7
HM170	GEN3	GEN3	GEN3	GEN3	X	X	X	X
C236	GEN3	GEN3	GEN3	GEN3	GEN3	GEN3	GEN3	GEN3

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Title: PCH_2(USB/SATA/PCIE)

Size: C | Document Number: MS-16J5 | Rev: 0A

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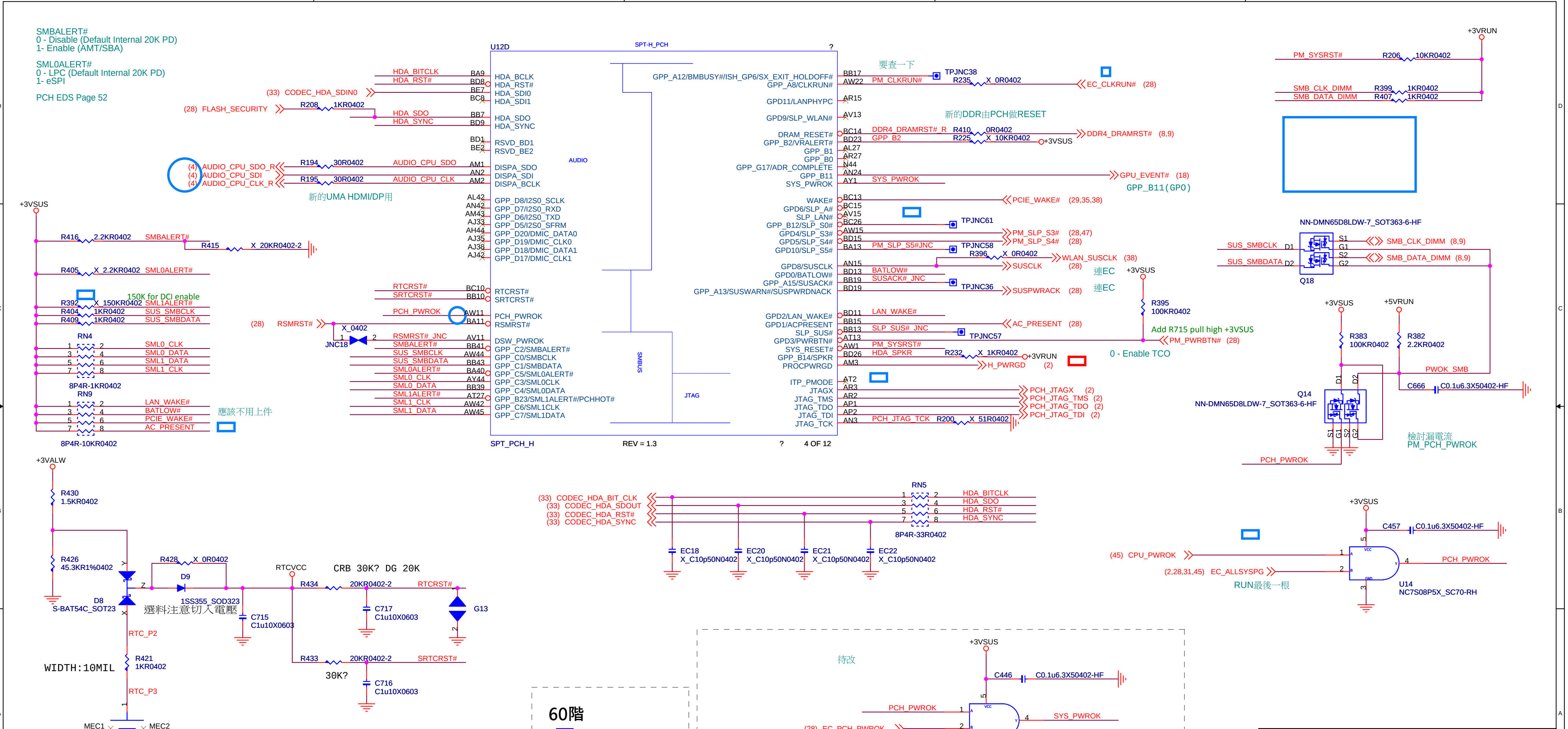
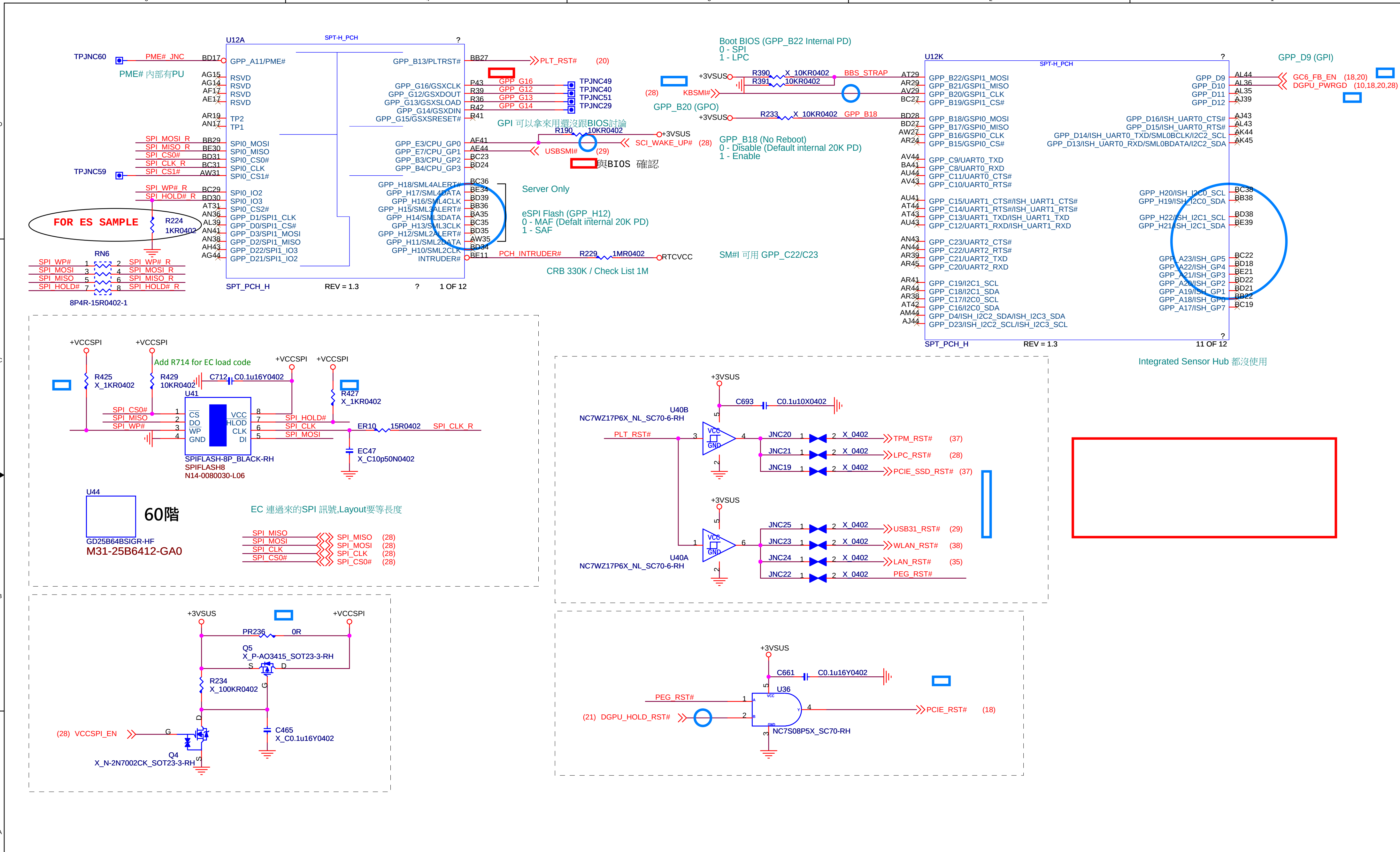


MICRO-STAR INT'L CO.,LTD.

Title: PCH_3(HDA/RTC/SMBUS)

Size	Document Number	Rev
Custom	MS-16J5	0A

Date: Tuesday, April 21, 2015 Sheet 23 of 55

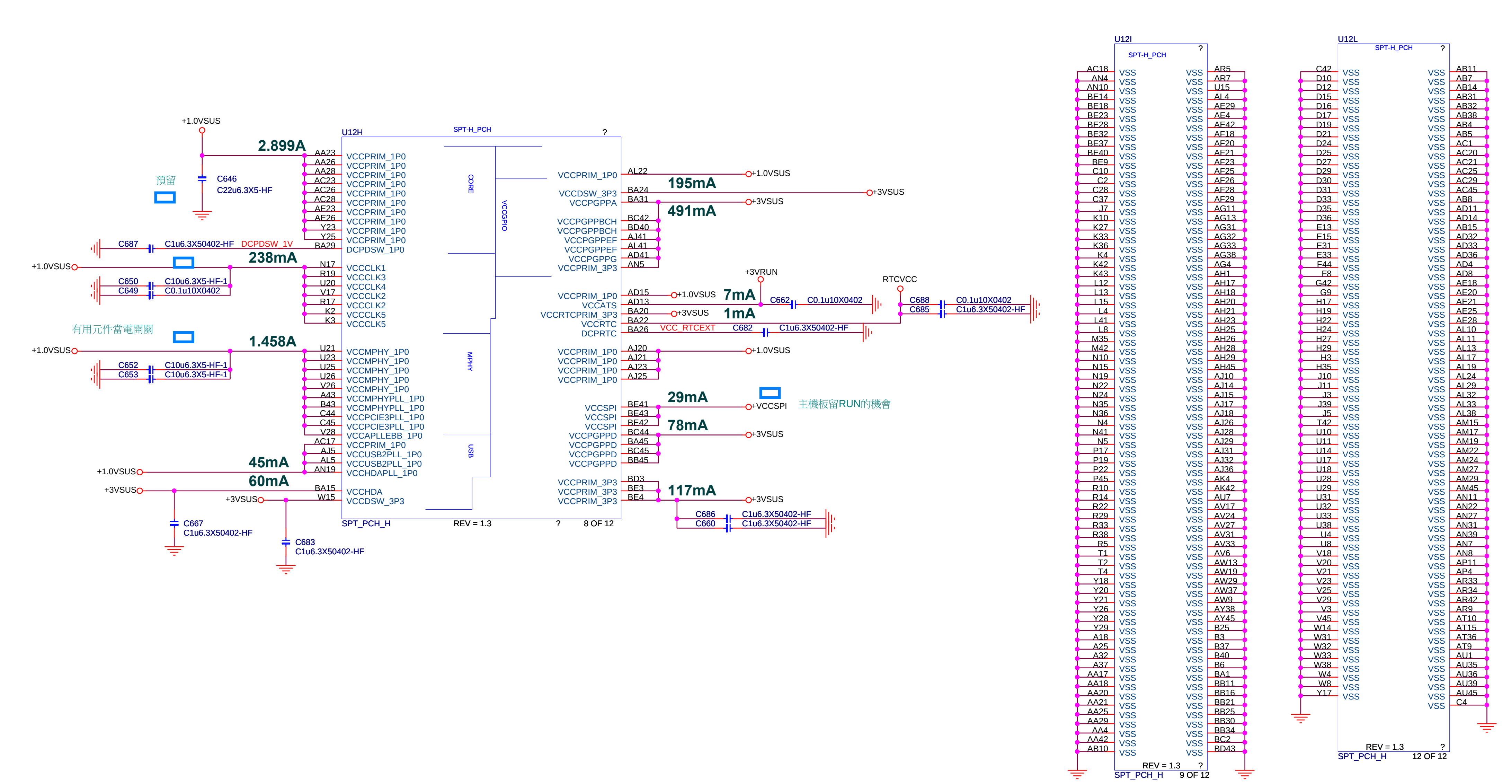


MICRO-STAR INT'L CO.,LTD.

Title: PCH_4(SPI/GPIO)

Size	Document Number	Rev
Custom	MS-16J5	0A

Date: Tuesday, April 21, 2015 Sheet 24 of 55



MICRO-STAR INT'L CO.,LTD.

Title	PCH_5(Power1)	
Size: Custom	Document Number: MS-16J5	Rev: 0A
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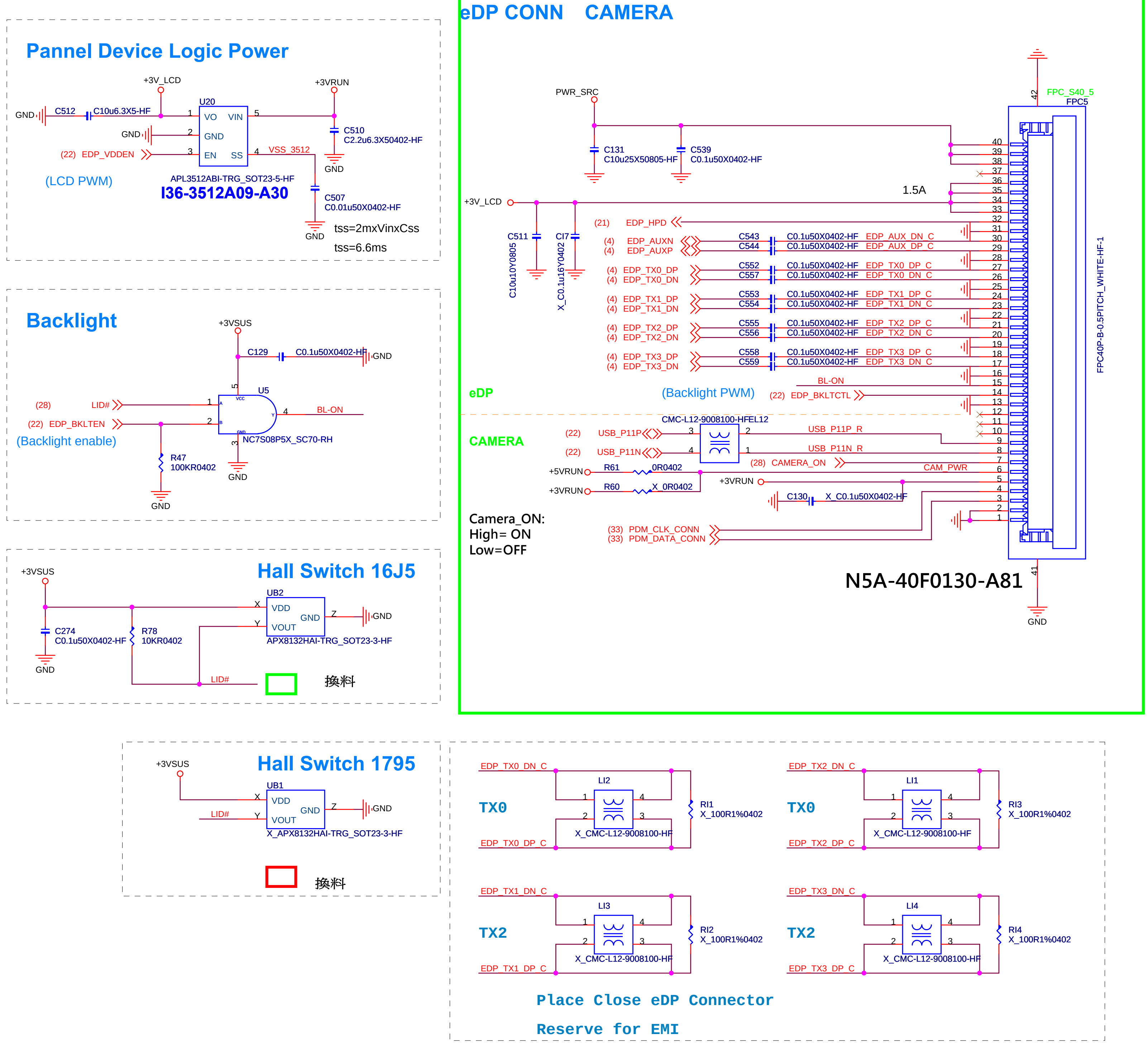
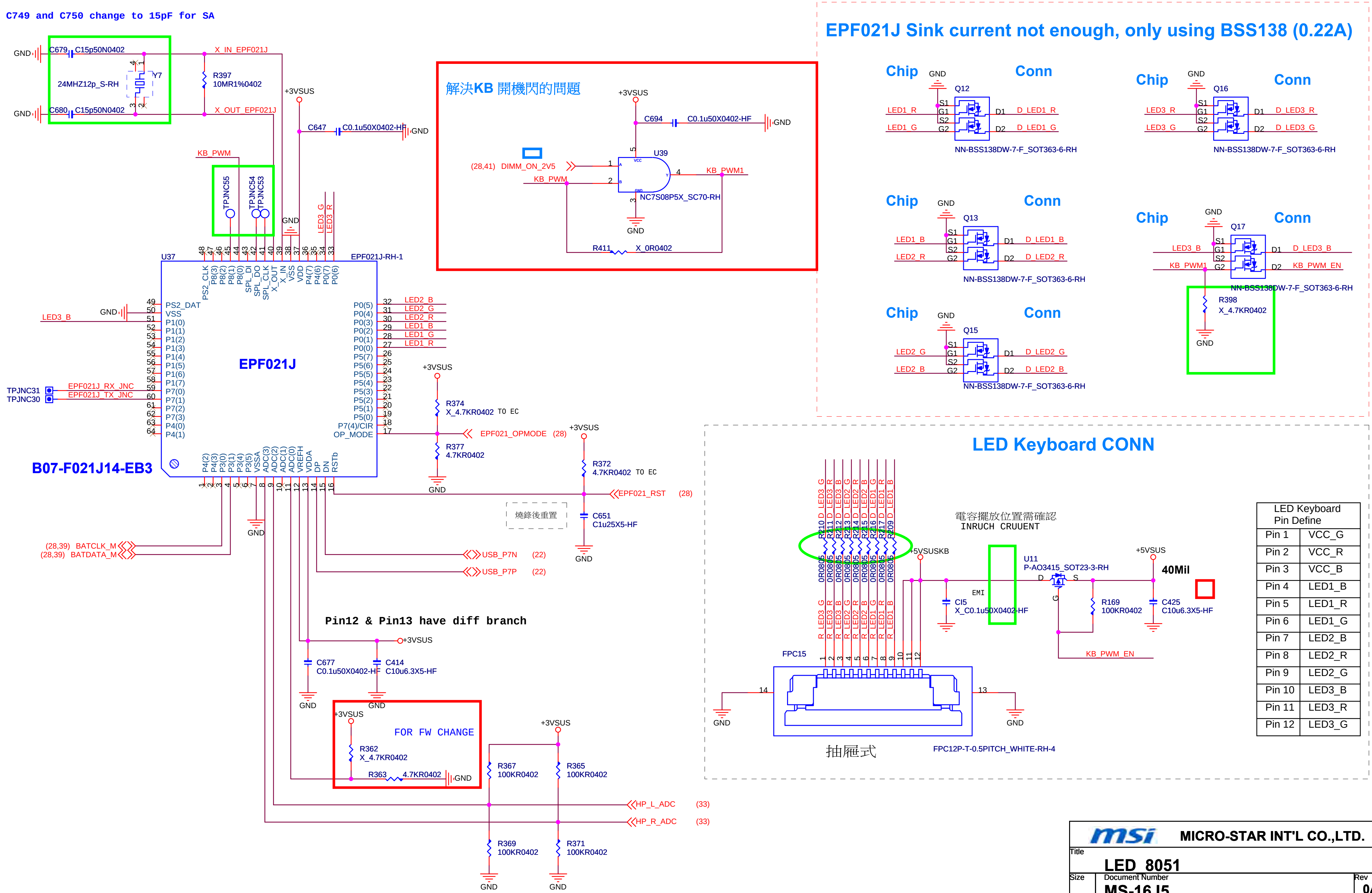
eDP



LCD Module Pin Define

Pin No	Symbol	Description
1	WP	EEPROM Write Protect(Keep open)
2	H_GND	High Speed Ground(0V)
3	eDP_Rx_3N	Complement Signal Link Lane 3
4	eDP_Rx_3P	True Signal Link Lane 3
5	H_GND	High Speed Ground(0V)
6	eDP_Rx_2N	Complement Signal Link Lane 2
7	eDP_Rx_2P	True Signal Link Lane 2
8	H_GND	H_GND
9	eDP_Rx_1N	Complement Signal Link Lane 1
10	eDP_Rx_1P	True Signal Link Lane 1
11	H_GND	H_GND
12	eDP_Rx_0N	Complement Signal Link Lane 0
13	eDP_Rx_0P	True Signal Link Lane 0
14	H_GND	H_GND
15	eDP_AUX_CH_P	True Signal Aux Channel
16	eDP_AUX_CH_N	Complement Signal Aux Channel
17	H_GND	H_GND
18	LCD_VCC	LCD logic and driver power
19	LCD_VCC	LCD logic and driver power
20	LCD_VCC	LCD logic and driver power
21	LCD_VCC	LCD logic and driver power
22	TEST	LCD Test Port
23	LCD_GND	LCD logic and driver ground(0V)
24	LCD_GND	LCD logic and driver ground(0V)
25	LCD_GND	LCD logic and driver ground(0V)
26	LCD_GND	LCD logic and driver ground(0V)
27	eDP_HPD	HPD signal pin
28	BL_GND	Backlight ground(0V)
29	BL_GND	Backlight ground(0V)
30	BL_GND	Backlight ground(0V)
31	BL_GND	Backlight ground(0V)
32	BL_ENABLE	Backlight enable
33	BL_PWM_DIM	System PWM signal input
34	SDA	I2C-bus Data
35	SCL	I2C-bus Clock
36	BL_PWR	Backlight power (5~21V)
37	BL_PWR	Backlight power (5~21V)
38	BL_PWR	Backlight power (5~21V)
39	BL_PWR	Backlight power (5~21V)
40	HSYNC	HSYNC output from Tcon

LED 8051 Controller



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

MICRO-STAR INT'L CO.,LTD.

Title: LED 8051

Size | Document Number: MS-16J5 | Rev: 0A

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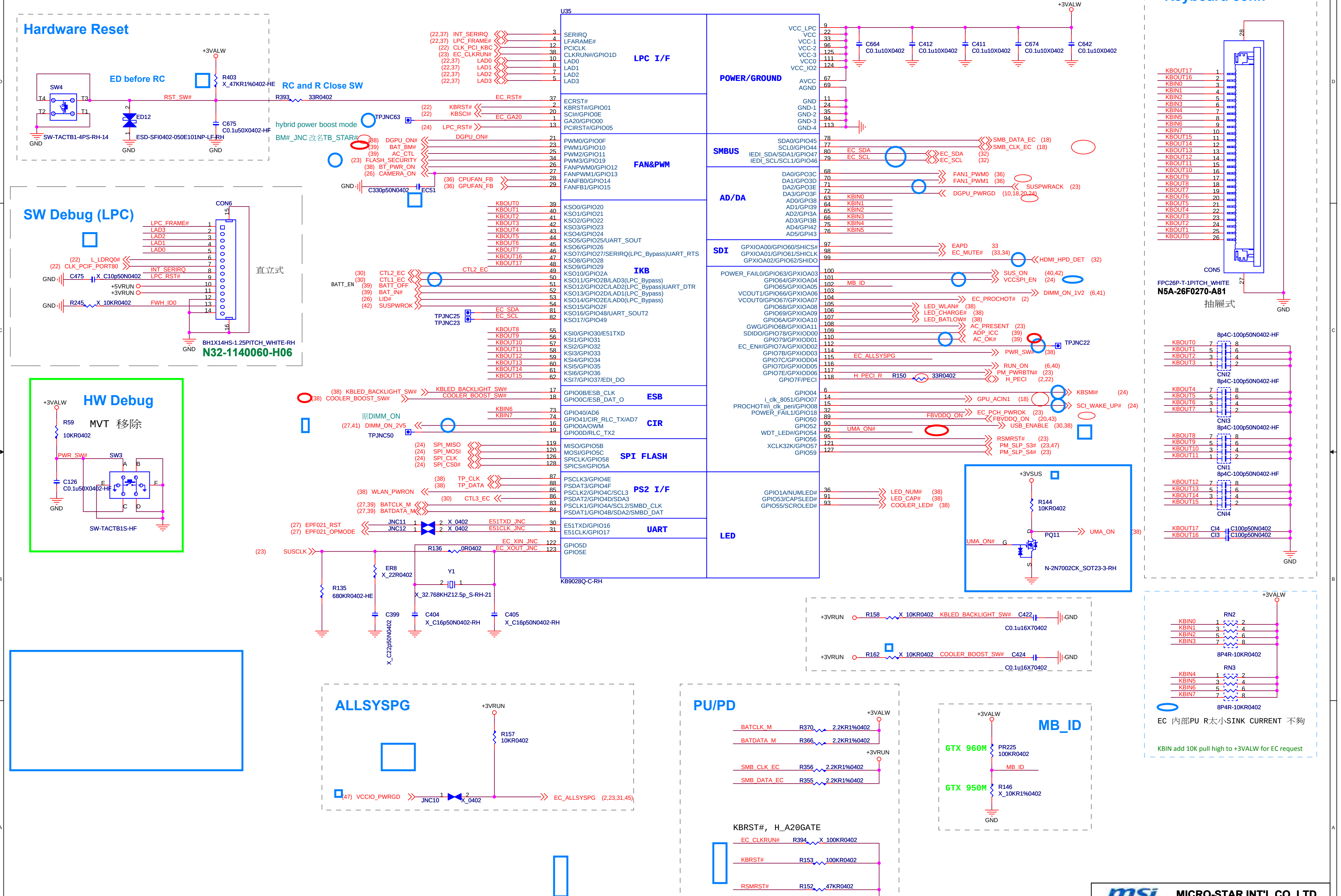
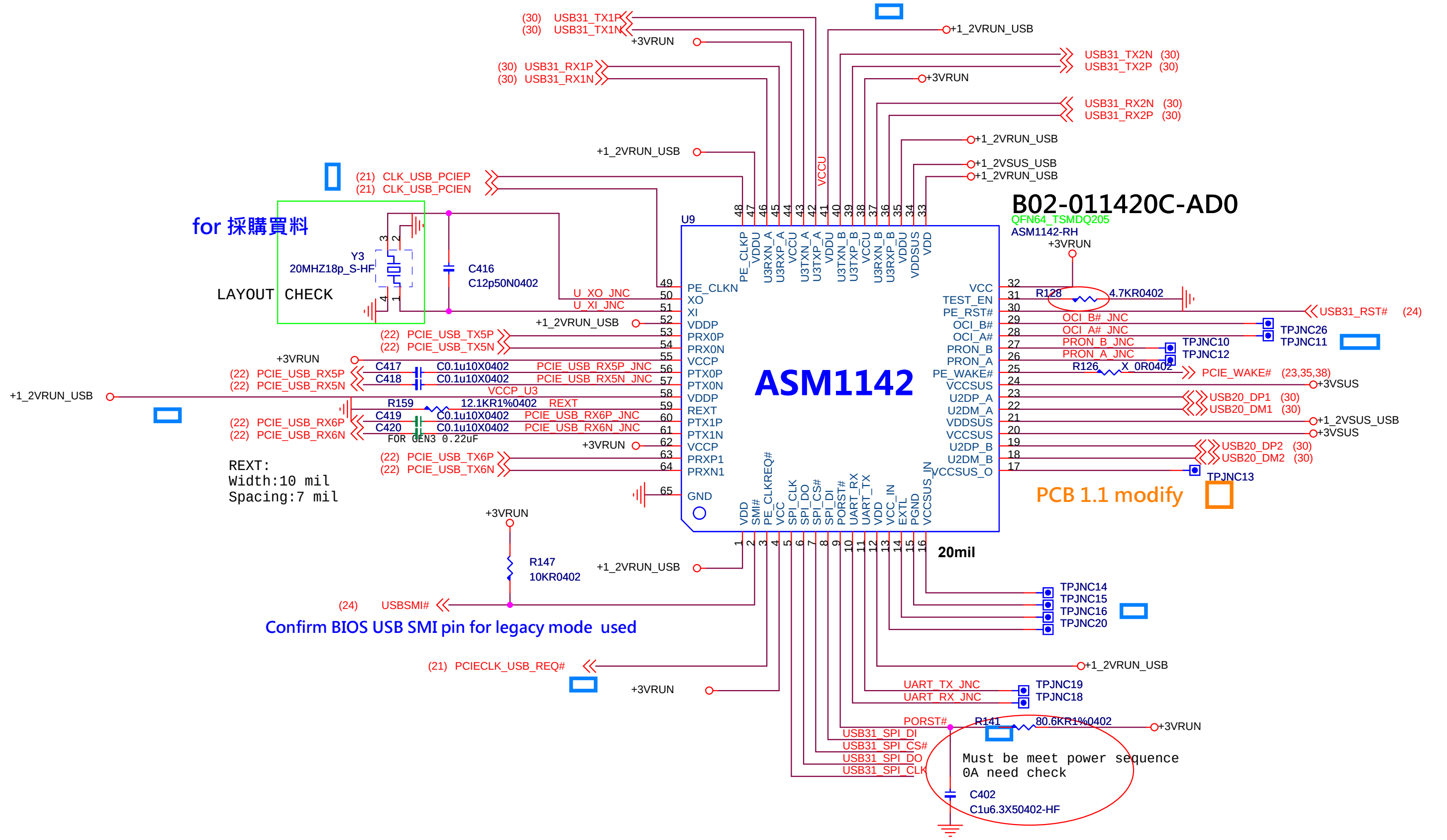
KBC/EC/uP (ENE9028)

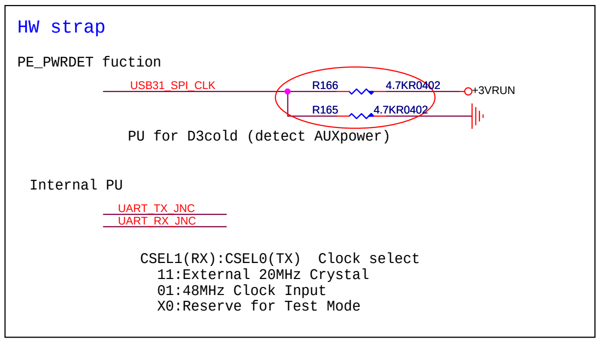


MICRO-STAR INT'L CO.,LTD.			
Title	KBC(KB3930QFB1)		
Size	Document Number	MS-16J5	Rev 0A
Date:	Tuesday, April 21, 2015	Sheet 28	of 55

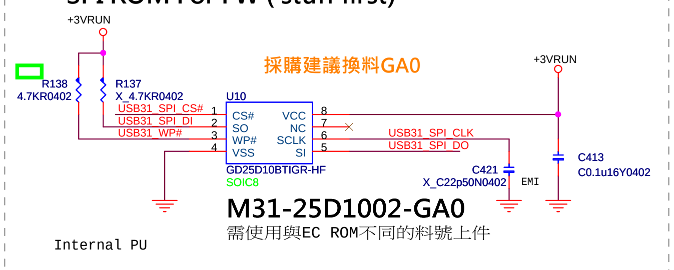
USB 3.0/ USB.3.1

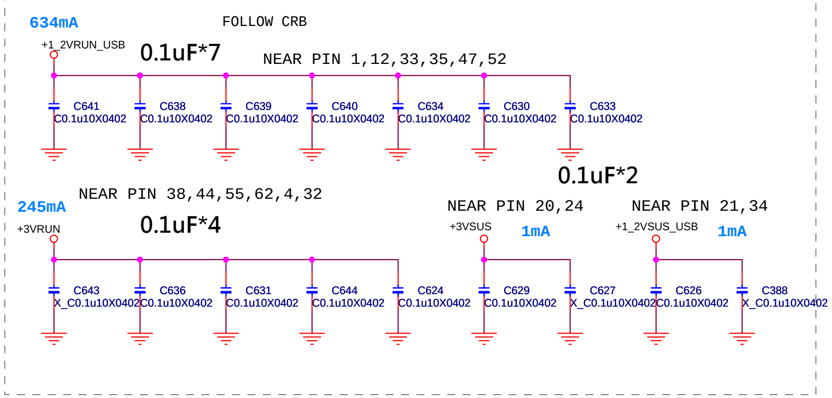
PCIE to USB 3.1

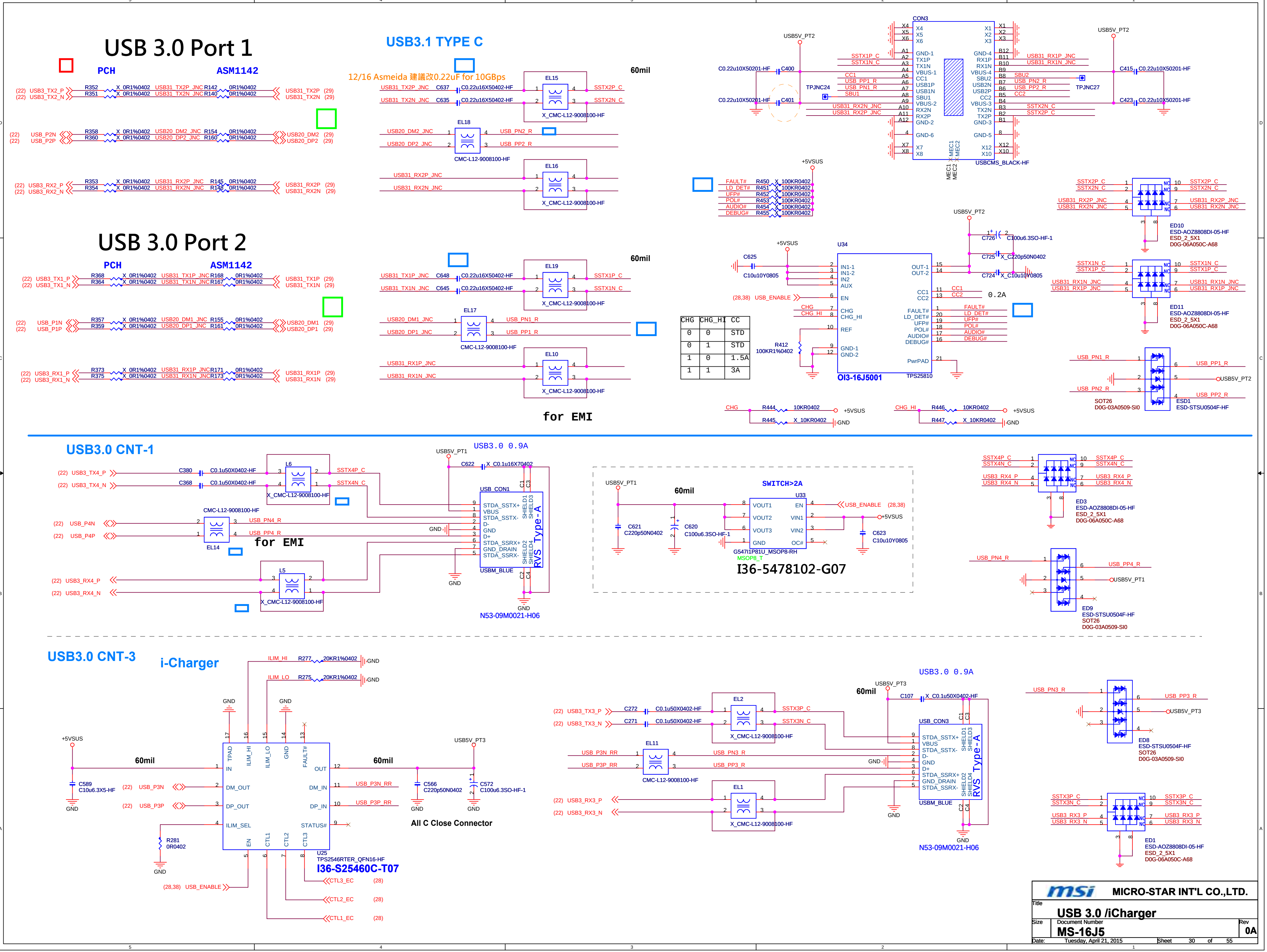




SPI ROM For FW (stuff first)







CHG	CHG_HI	CC
0	0	STD
0	1	STD
1	0	1.5A
1	1	3A

MICRO-STAR INT'L CO.,LTD.

Title	USB 3.0 /iCharger
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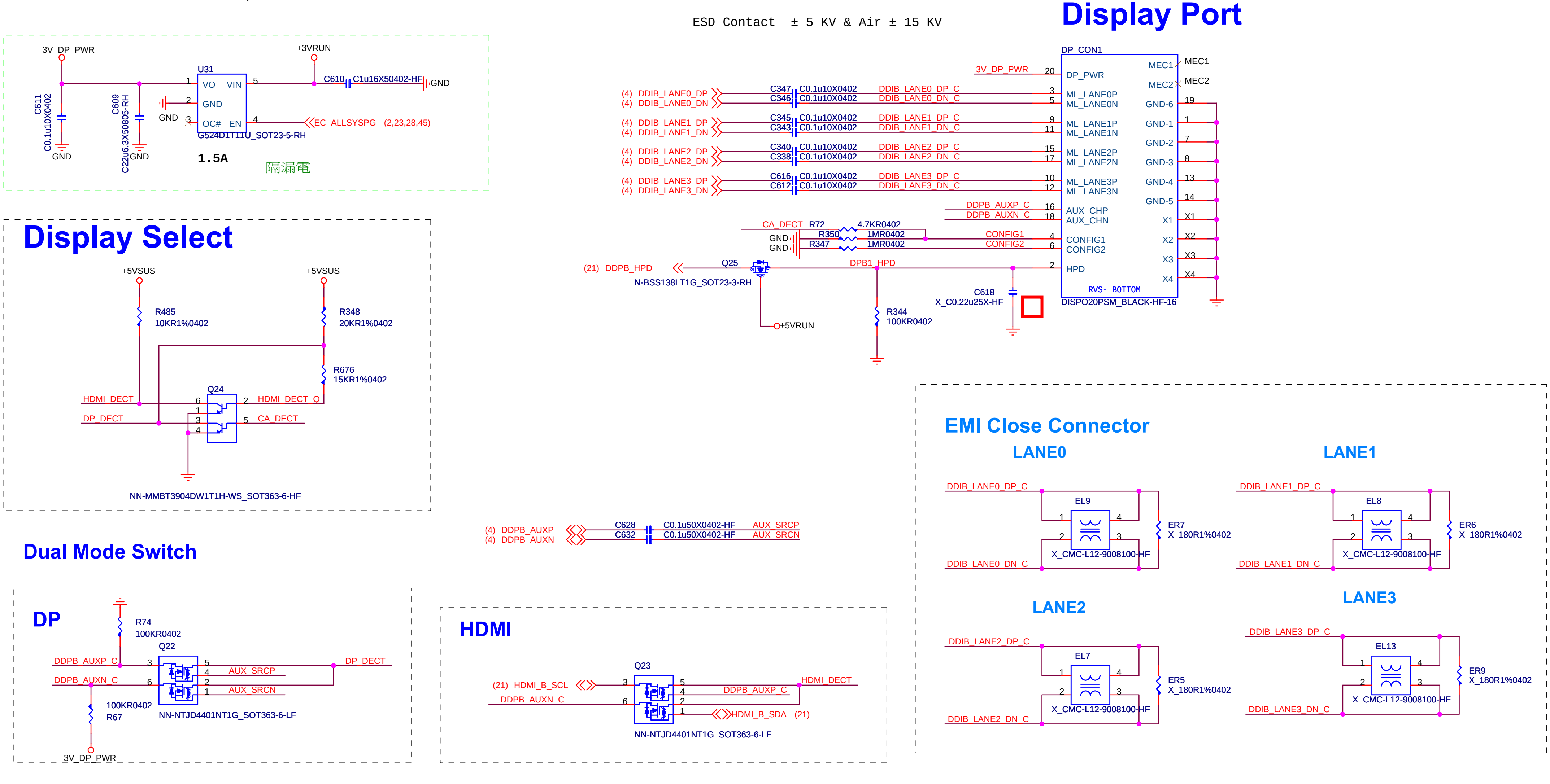
Display Port

The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



msi MICRO-STAR INT'L CO.,LTD.

Title	DP	
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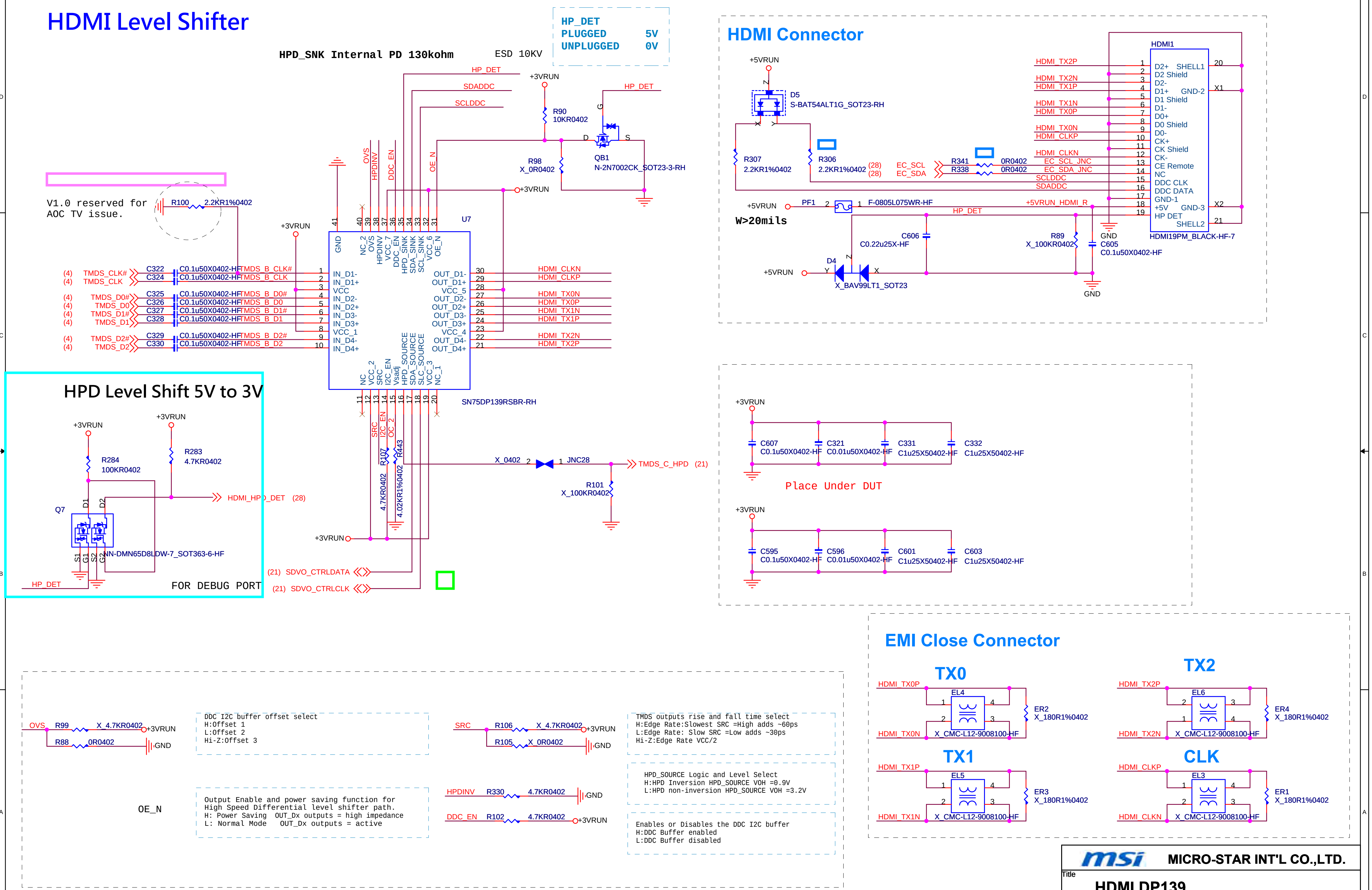

msi	MICRO-STAR INT'L CO.,LTD.	
Title	HDMI DP139	
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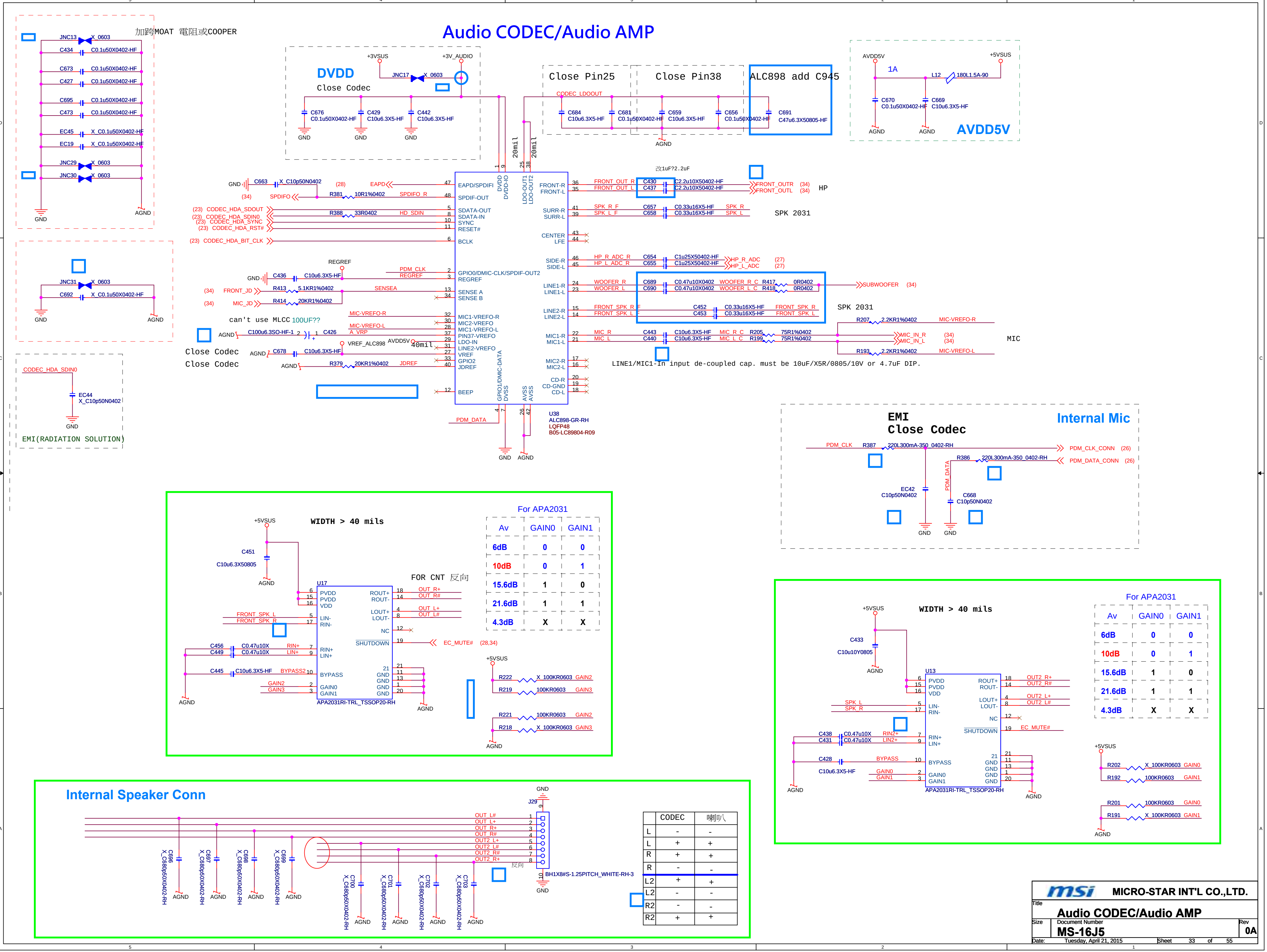
Audio CODEC/Audio AMP



For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

For APA2031

Av	GAIN0	GAIN1
6dB	0	0
10dB	0	1
15.6dB	1	0
21.6dB	1	1
4.3dB	X	X

	CODEC	喇叭
L	-	-
L	+	+
R	+	+
R	-	-
L2	+	+
L2	-	-
R2	-	-
R2	+	+

MICRO-STAR INT'L CO.,LTD.

Title: Audio CODEC/Audio AMP

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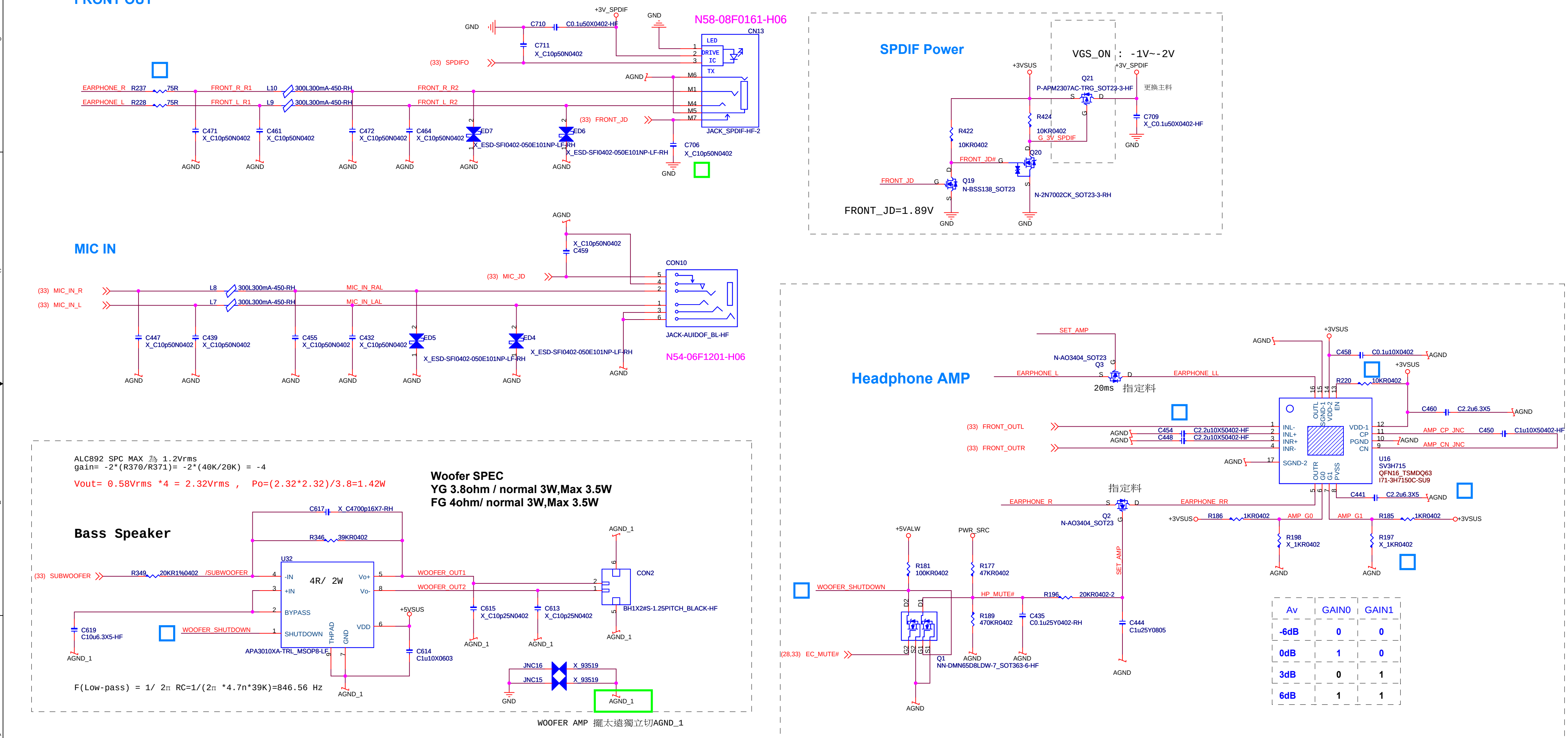
Audio CONN /Woffer



ALC892 SPC MAX 為 1.2Vrms
gain= -2*(R370/R371)= -2*(40K/20K) = -4

Vout= 0.58Vrms *4 = 2.32Vrms , Po=(2.32*2.32)/3.8=1.42W

Woofer SPEC
YG 3.8ohm / normal 3W,Max 3.5W
FG 4ohm/ normal 3W,Max 3.5W

F(Low-pass) = 1/ 2π RC=1/(2π *4.7n*39K)=846.56 Hz

WOOFER AMP 擺太遠獨立切AGND_1

Av	GAIN0	GAIN1
-6dB	0	0
0dB	1	0
3dB	0	1
6dB	1	1

MICRO-STAR INT'L CO.,LTD.

Title: **Audio / Woffer**

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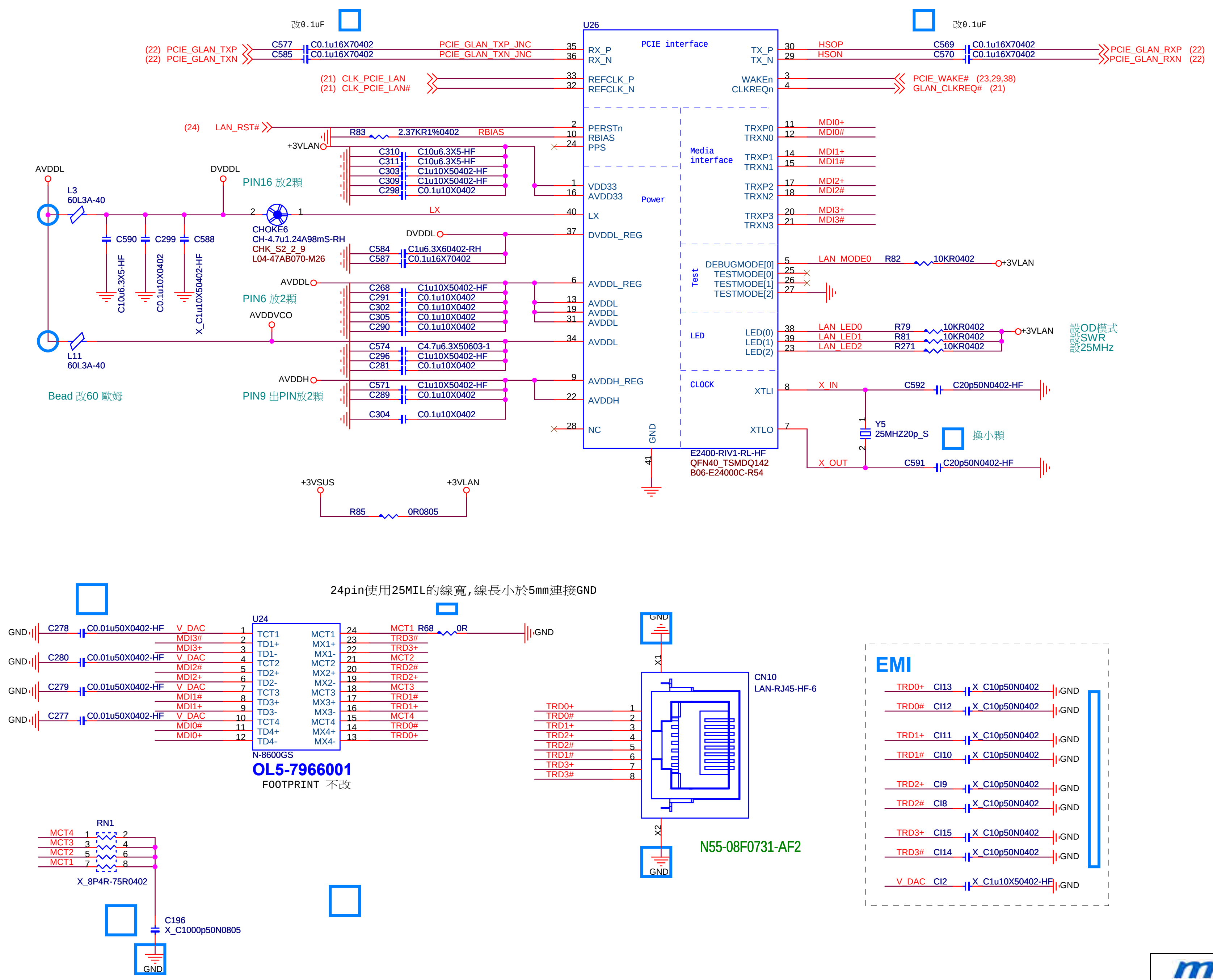
GIGA LAN(BigFoot BFN2400B)



msi MICRO-STAR INT'L CO.,LTD.

Title: GIGA LAN(BigFoot BFN2400/AR8161)

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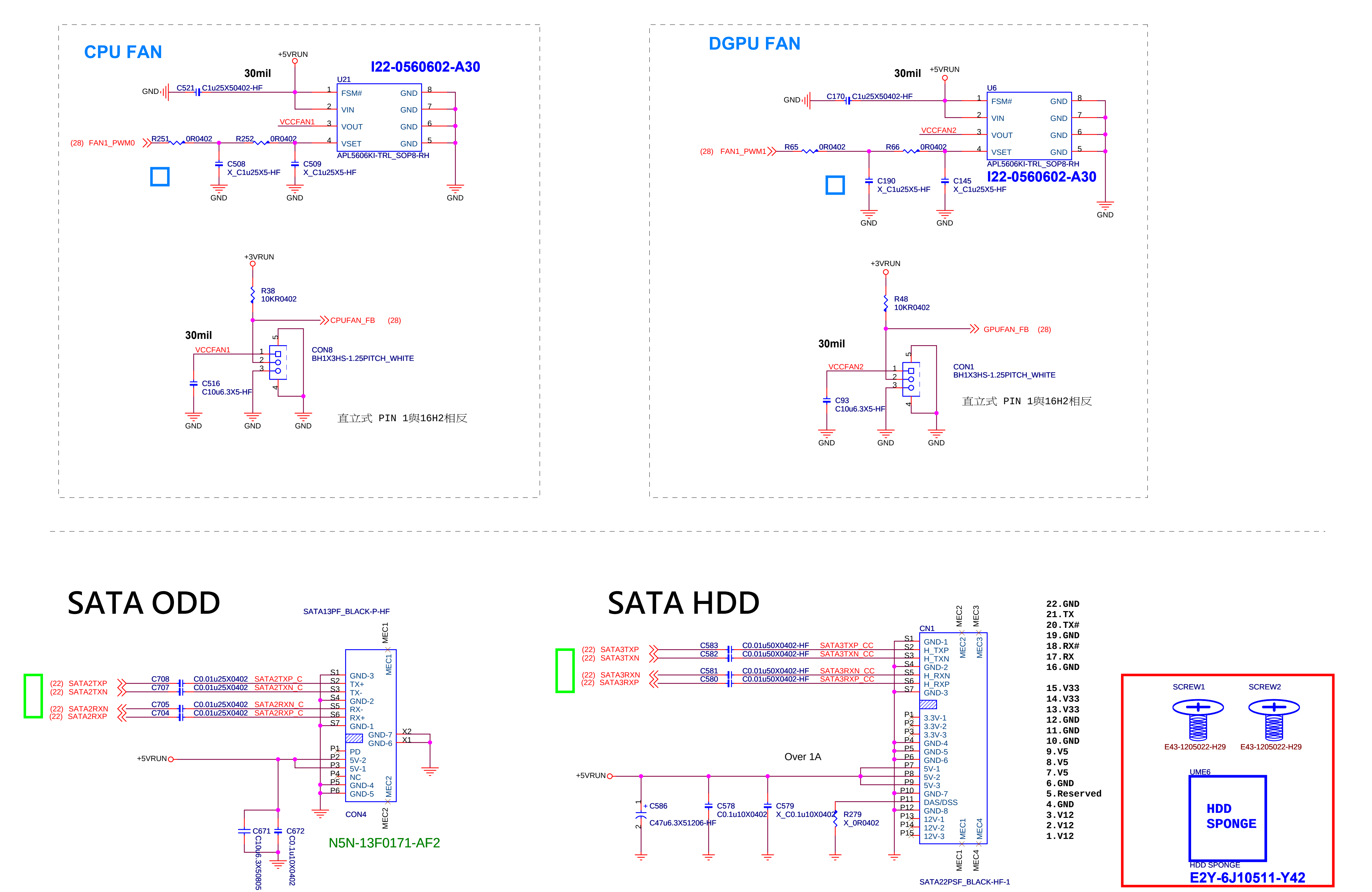

Title
ODD/HDD/FAN

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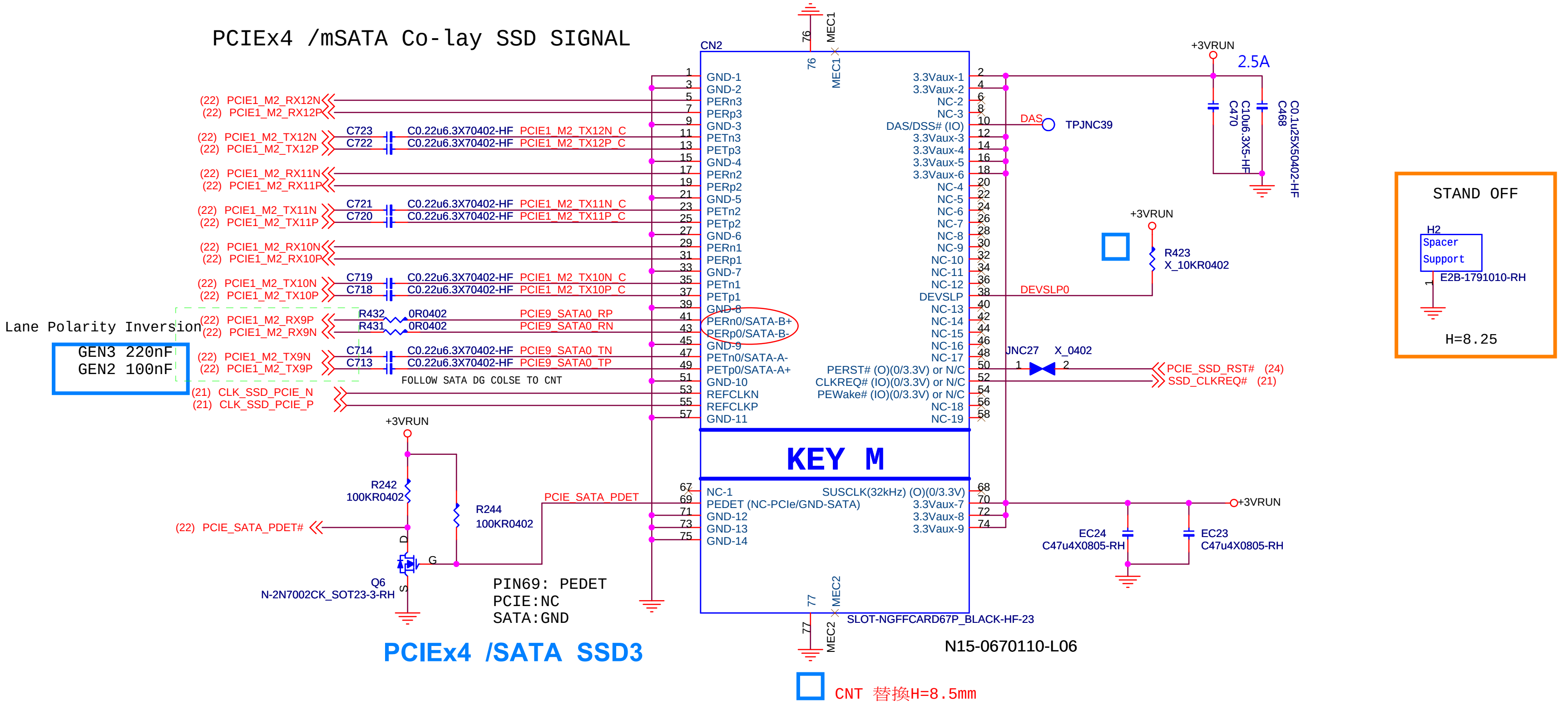
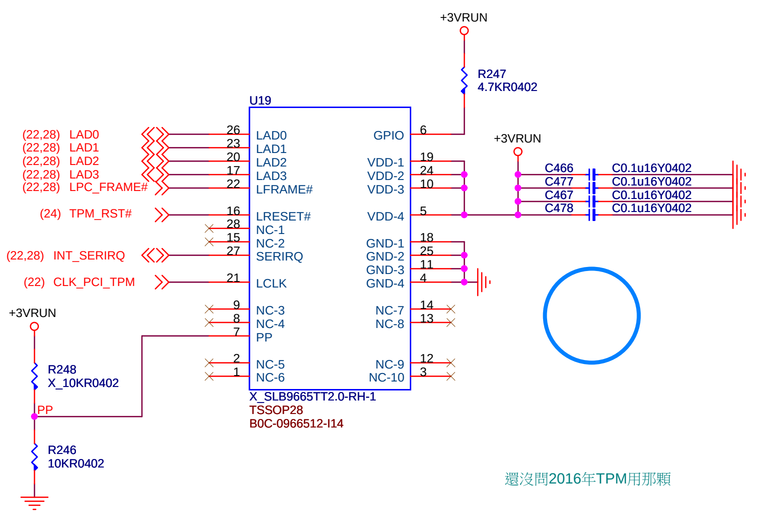
PCIEx4 /mSATA Co-lay SSD SIGNAL



TPM



msi	MICRO-STAR INT'L CO.,LTD.	
Title: SSD		
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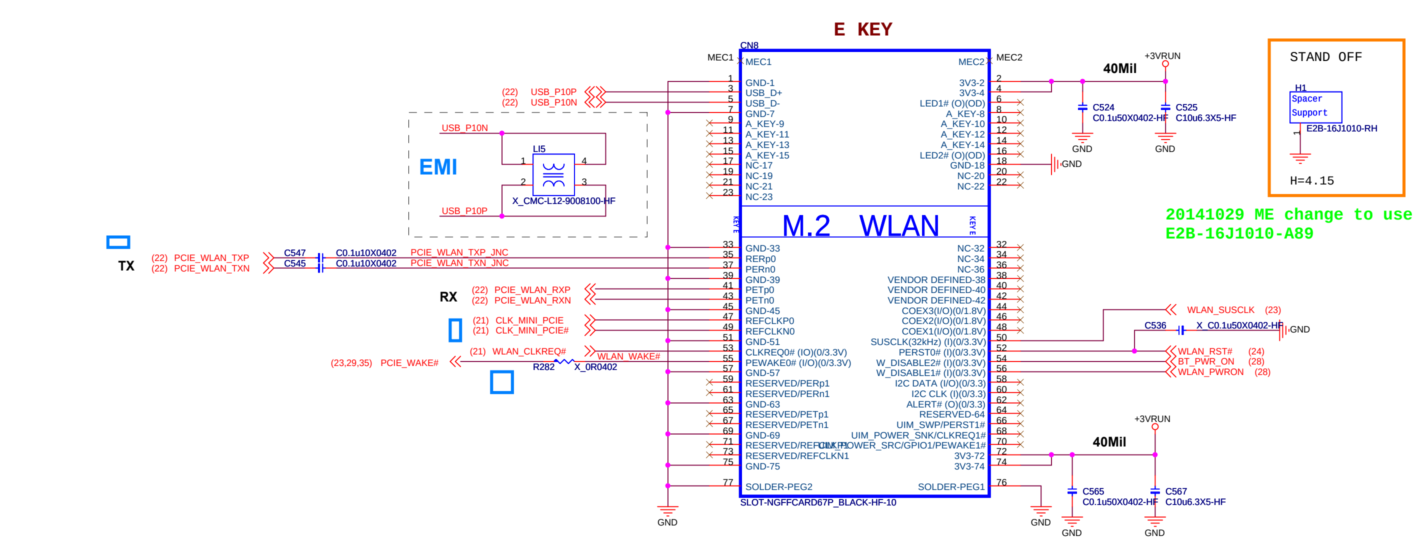
WLAN/LED

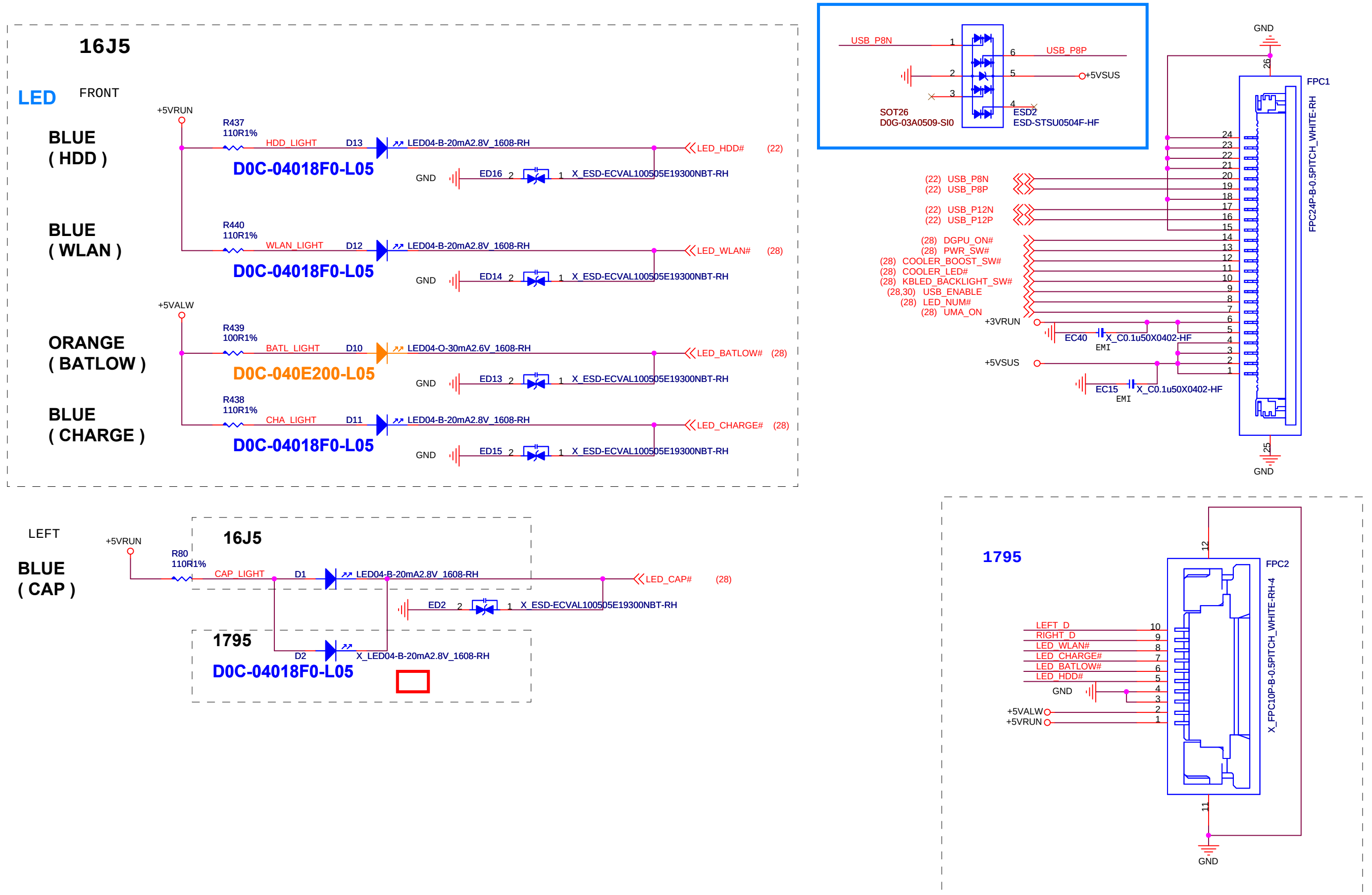
WLAN

E KEY

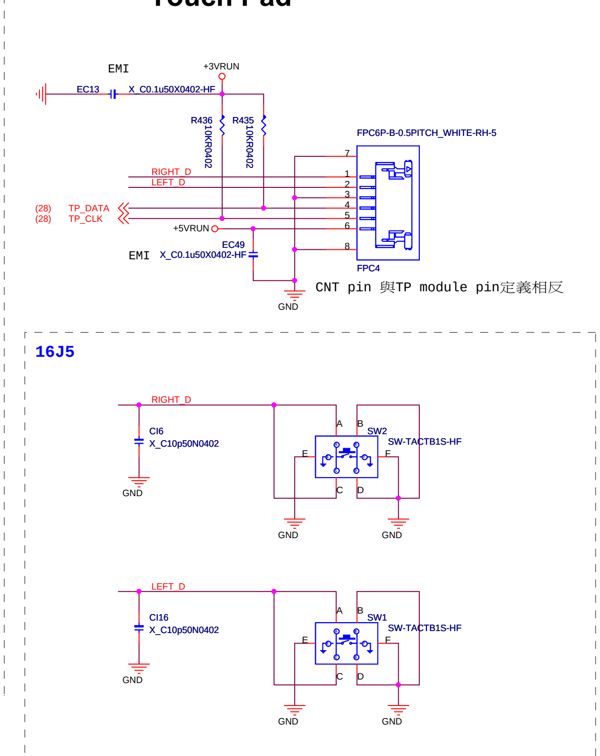


20141029 ME change to use
E2B-16J1010-A89

Pin 1	GND		
Pin 3	USB_D+	Pin 2	3.3V
Pin 5	USB_D-	Pin 4	3.3V
Pin 7	GND	Pin 6	LED1#
Pin 9	Module Key	Pin 8	Module Key
Pin 11	Module Key	Pin 10	Module Key
Pin 13	Module Key	Pin 12	Module Key
Pin 15	Module Key	Pin 14	Module Key
Pin 17	N/C	Pin 16	LED2#
Pin 19	N/C	Pin 18	GND
Pin 21	N/C	Pin 20	N/C
Pin 23	N/C	Pin 22	N/C
Pin 25	Module Key	Pin 24	Module Key
Pin 27	Module Key	Pin 26	Module Key
Pin 29	Module Key	Pin 28	Module Key
Pin 31	Module Key	Pin 30	Module Key
Pin 33	GND	Pin 32	N/C
Pin 35	PERP0	Pin 34	N/C
Pin 37	PERN0	Pin 36	N/C
Pin 39	GND	Pin 38	Clink Reset (I 3.3V)
Pin 41	PETP0	Pin 40	N/C
Pin 43	PETN0	Pin 42	N/C
Pin 45	GND	Pin 44	N/C
Pin 47	REFCLKP0	Pin 46	N/C
Pin 49	REFCLKN0	Pin 48	N/C
Pin 51	GND	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 53	CLKREQ0#	Pin 52	PERST0#
Pin 55	PEWAKE0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 57	GND	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 59	N/C	Pin 58	N/C
Pin 61	N/C	Pin 60	N/C
Pin 63	GND	Pin 62	N/C
Pin 65	N/C	Pin 64	Resever
Pin 67	N/C	Pin 66	N/C
Pin 69	GND	Pin 68	N/C
Pin 71	N/C	Pin 70	N/C
Pin 73	N/C	Pin 72	3.3V
Pin 75	GND	Pin 74	3.3V



Touch Pad



msi	MICRO-STAR INT'L CO.,LTD.
Title	WLAN /LED/TP
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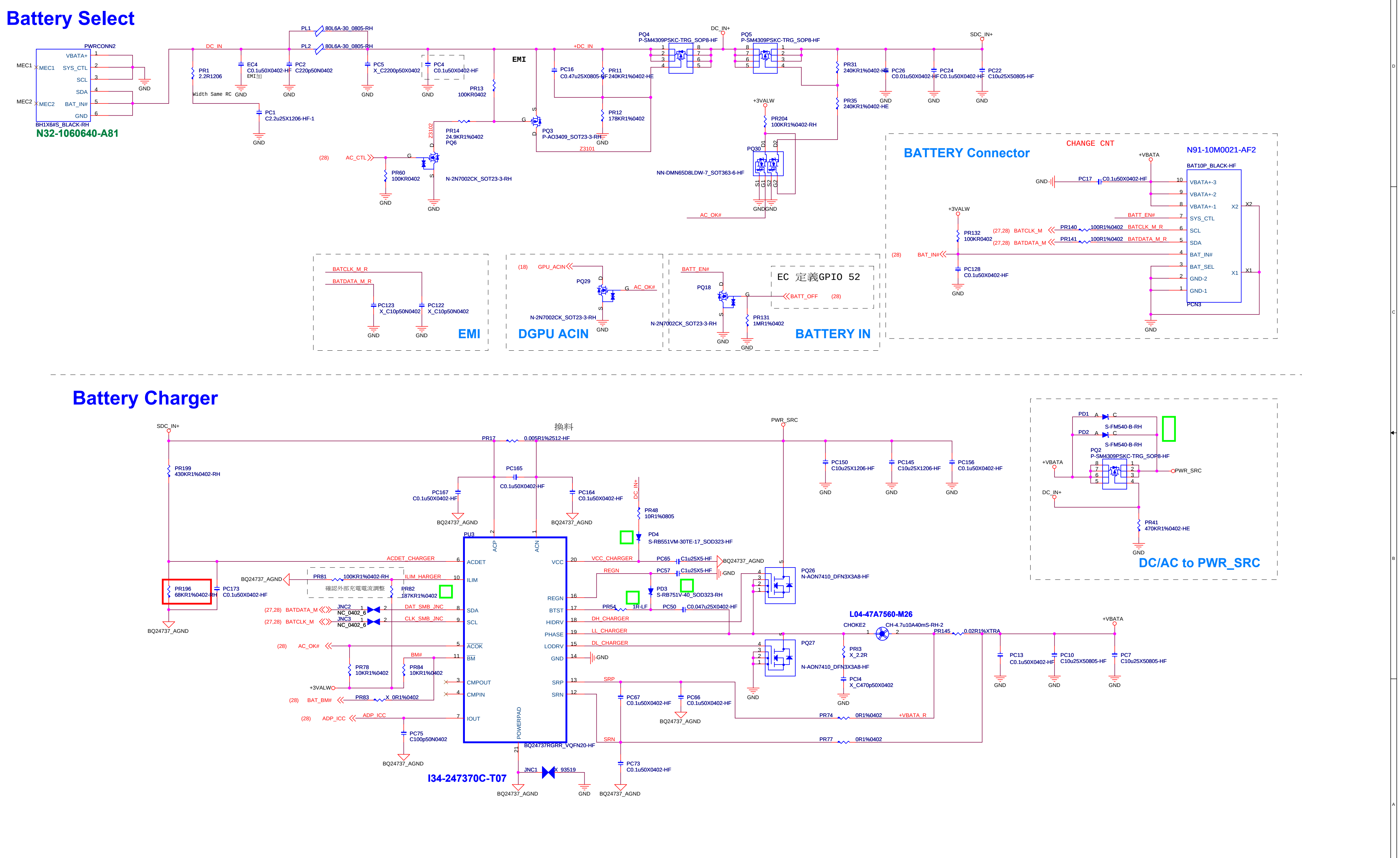
Battery Select/Charger



msi MICRO-STAR INT'L CO.,LTD.

Title: Battery Select/Charger

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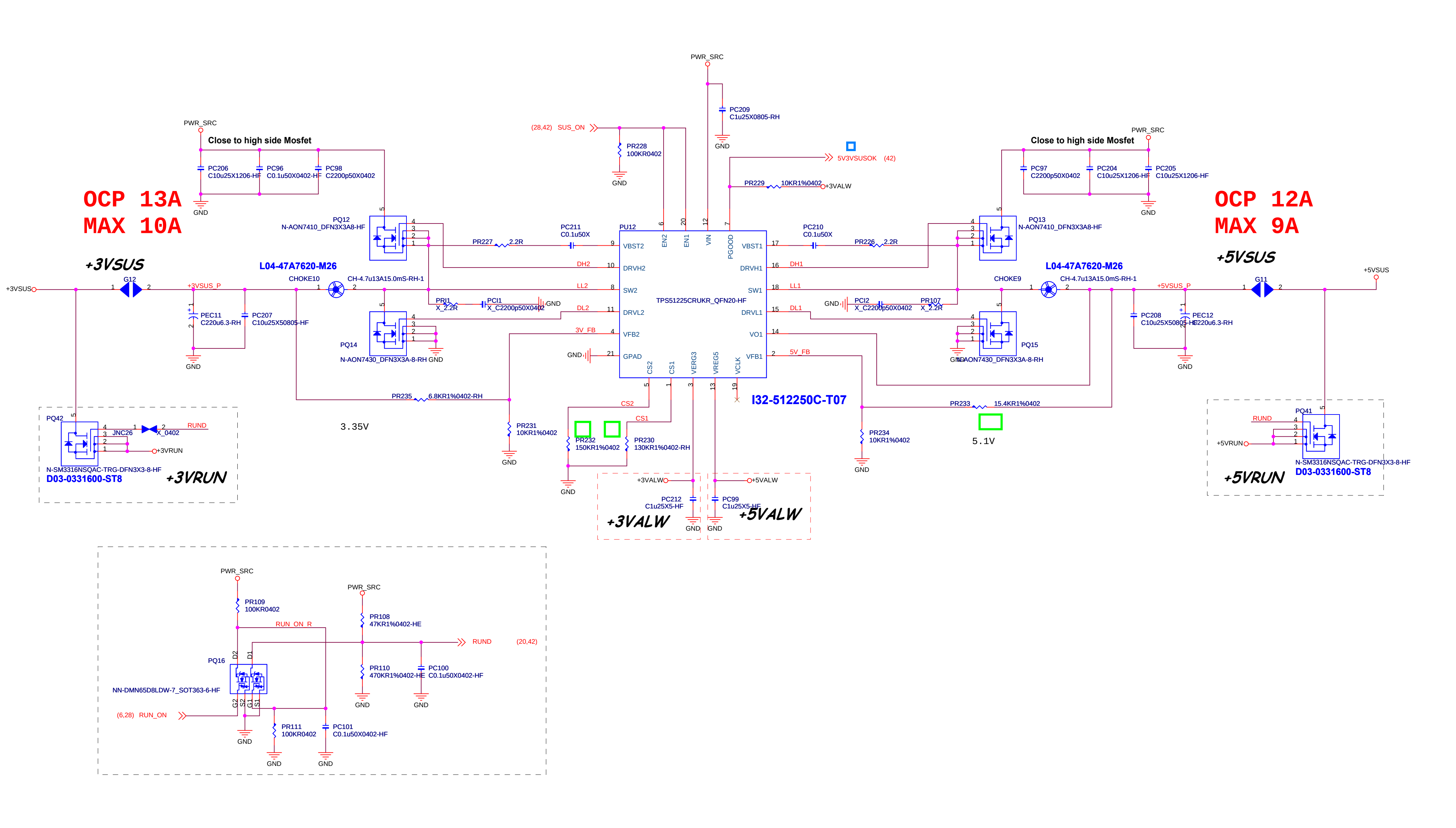
System Power



MICRO-STAR INT'L CO.,LTD.

Title	System Power	
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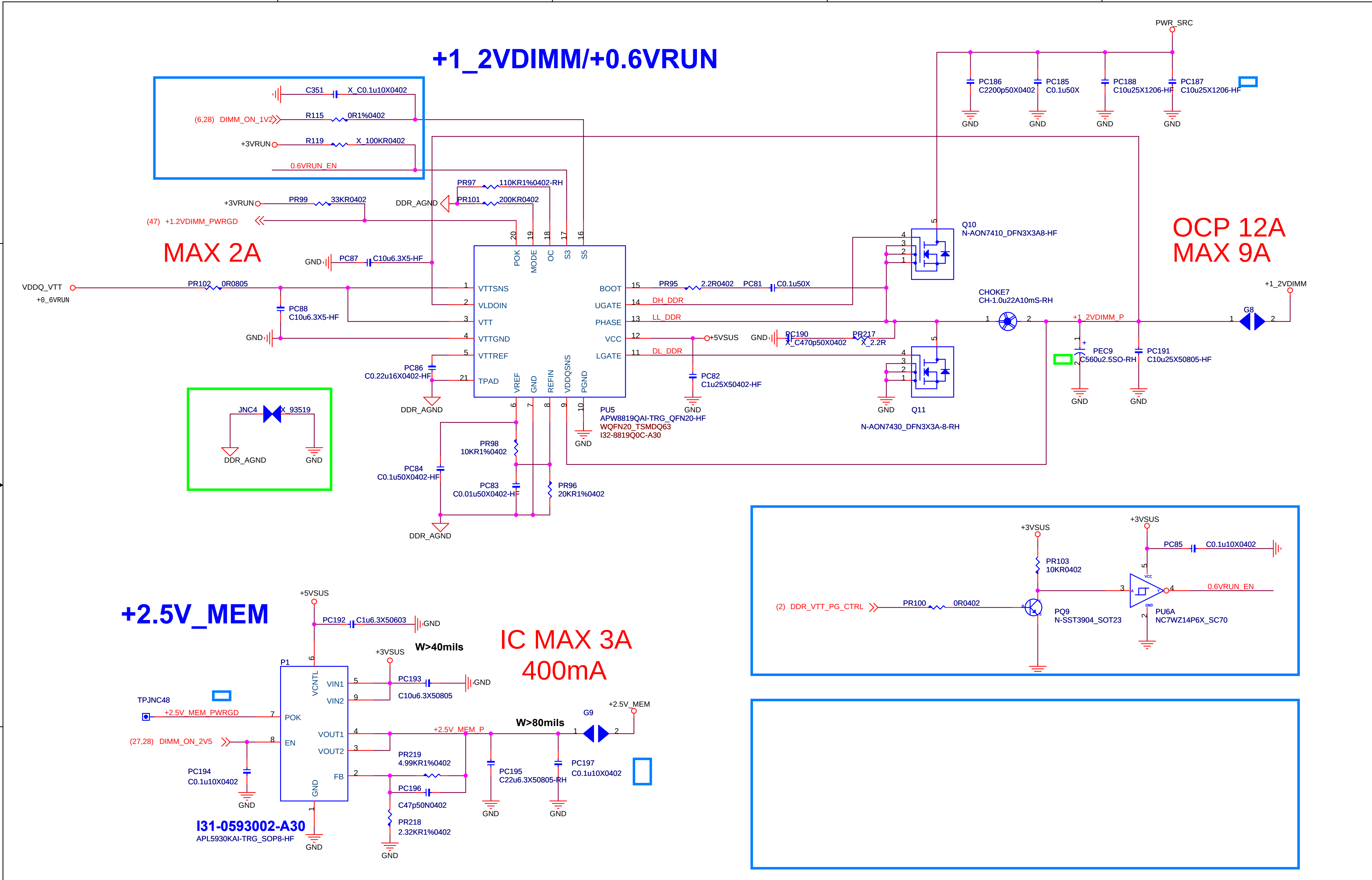

MICRO-STAR INT'L CO.,LTD.

Title	+1.2VDIMM/+0.6VRUN/+2.5VMEM
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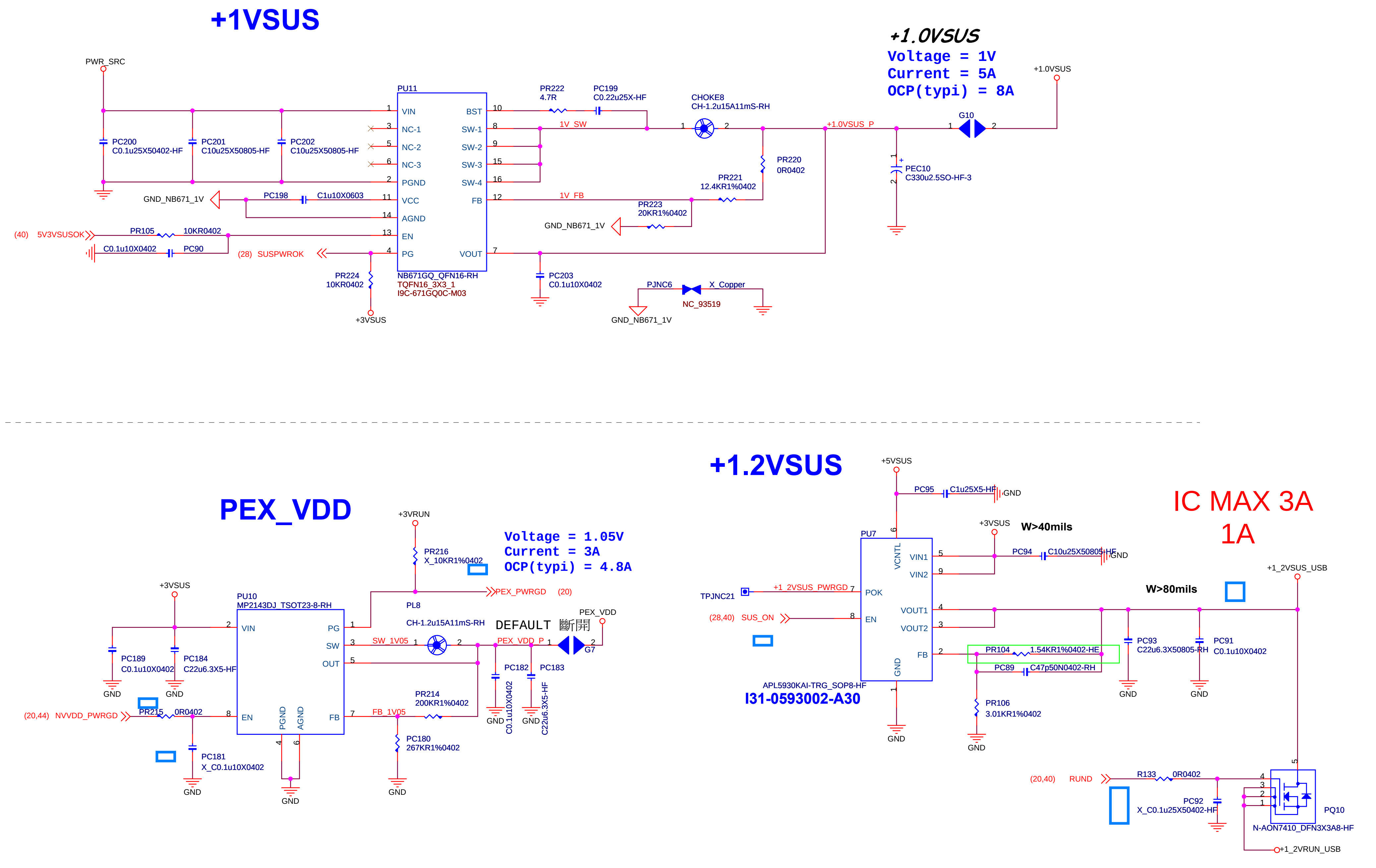

MICRO-STAR INT'L CO.,LTD.

Title	1VSUS /PEX_VDD/1.2VSUS	
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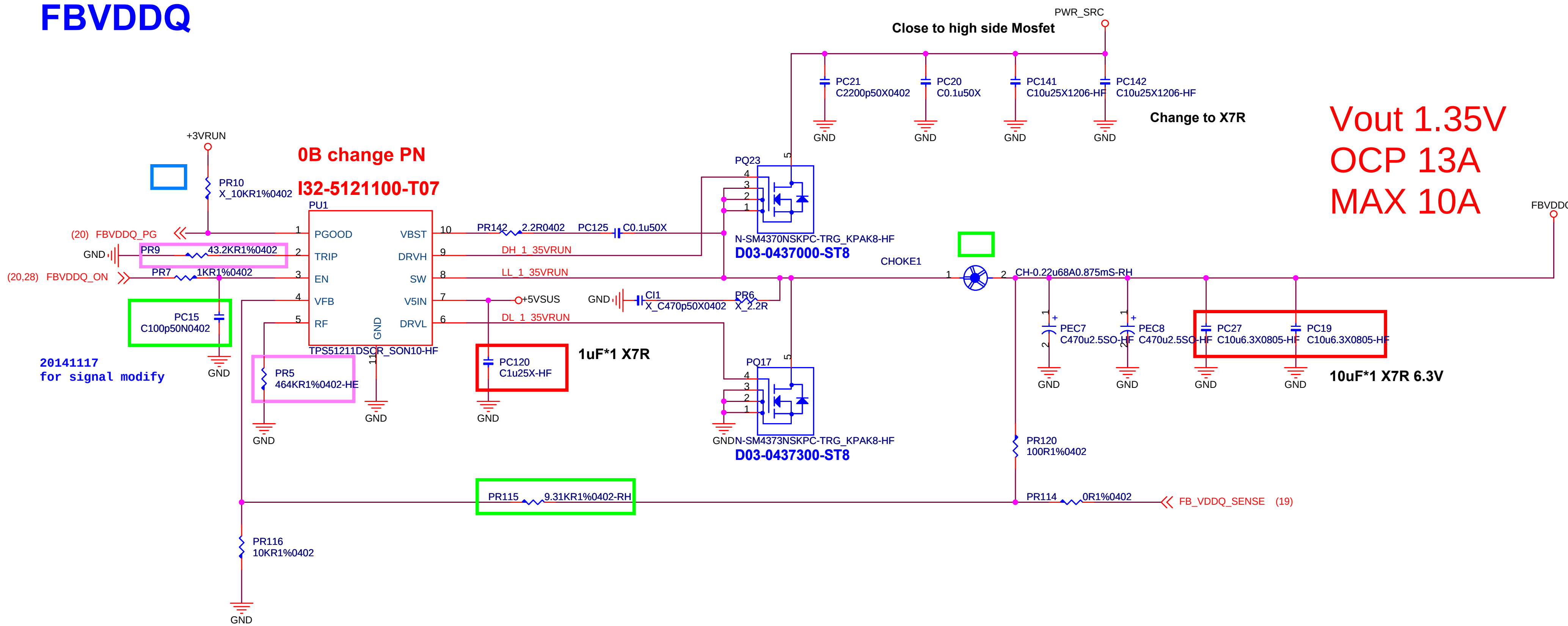
DGPU POWER FBVDDQ

FBVDDQ



MICRO-STAR INT'L CO.,LTD.

Title: DGPU POWER FBVDDQ

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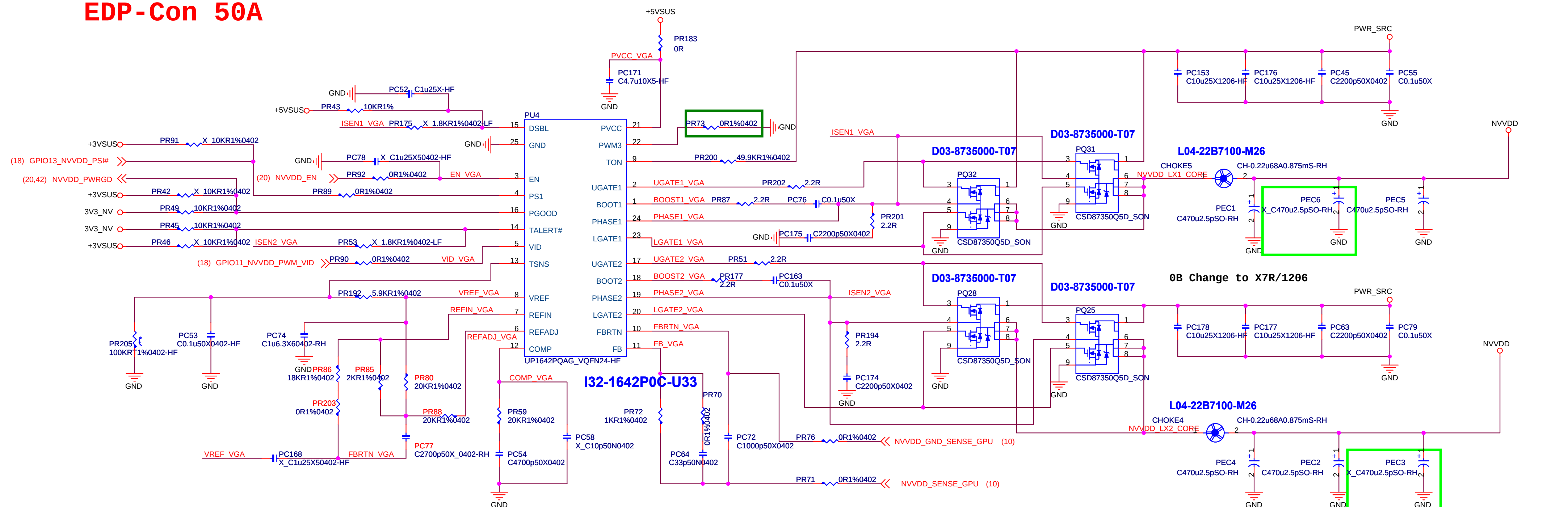
DGPU POWER / UP1642PQAG

DGPU POWER NVVDD

CONFIG A
VBoot:0.875V
Vmin:0.6V / Vmax:1.2V

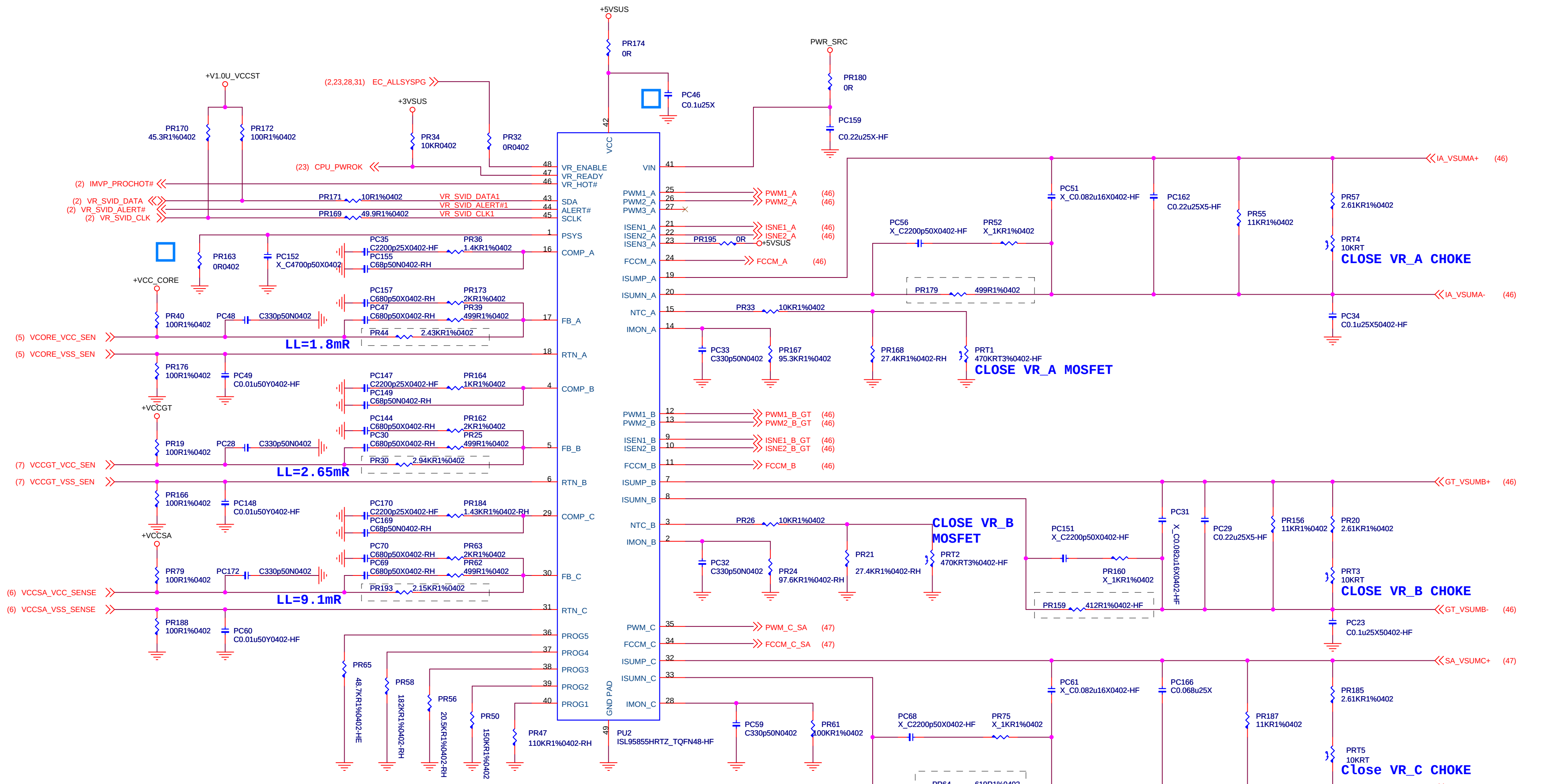
EDP-Peak 87A
EDP-Con 50A



	PR56	PR52	PR53	PR54	PR121	PC45
CONFIG	R1	R2	R3	R4	R5	C
N16E-GT N16P-GX-B	20K	20K	2K	18K	0	2.7nF

20141029 power modify for GPU power setting
PR52,PR56: 39K ohm to 20K ohm
PR53: 1.5K ohm to 2K ohm
PR54: 30K ohm to 18K ohm
PR121: 1.5K ohm to 0 ohm
PC45: 1.5nF to 2.7nF

Skylake H-line 42 45W ISL95855



SKL-H(4+2)

PROG1	110KR	Vboot=0V, Selw rate=30mV/us, VR_A=IA, VR_B=GT, VR_C=SA
PROG2	150KR	IMAX VR_A=70A, VR_A PSI1=1PH
PROG3	20.5KR	IMAX VR_B=60A, DROOP VR_B Active
PROG4	182KR	DROOP VR_A Active, DROOP VR_C Active, VR_A VR_B Frequency=750kHz
PROG5	48.7KR	IMAX VR_C=12A, Frequency=450kHz

MICRO-STAR INT'L CO.,LTD.

Title: Skylake CPU Power

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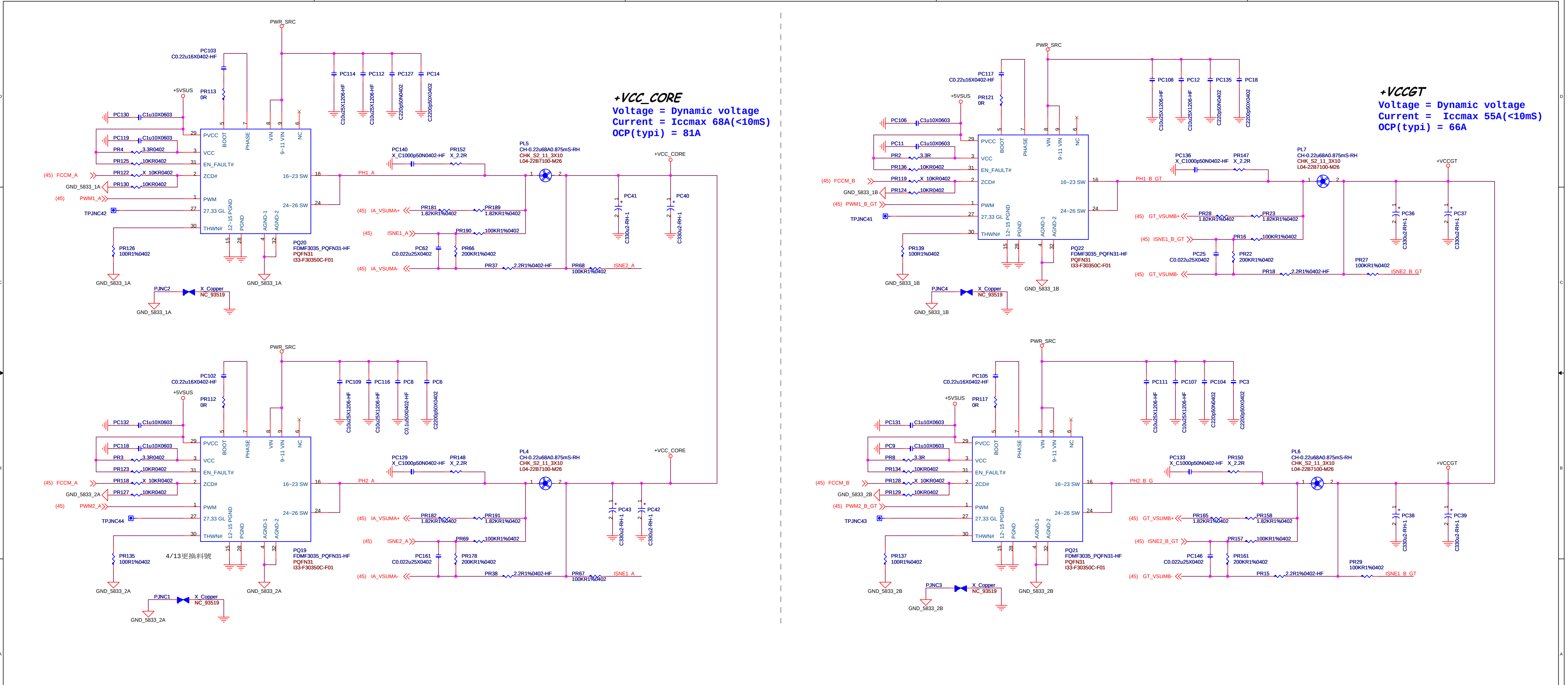

MICRO-STAR INT'L CO.,LTD.

Title: Skylake VCore/VCCGT

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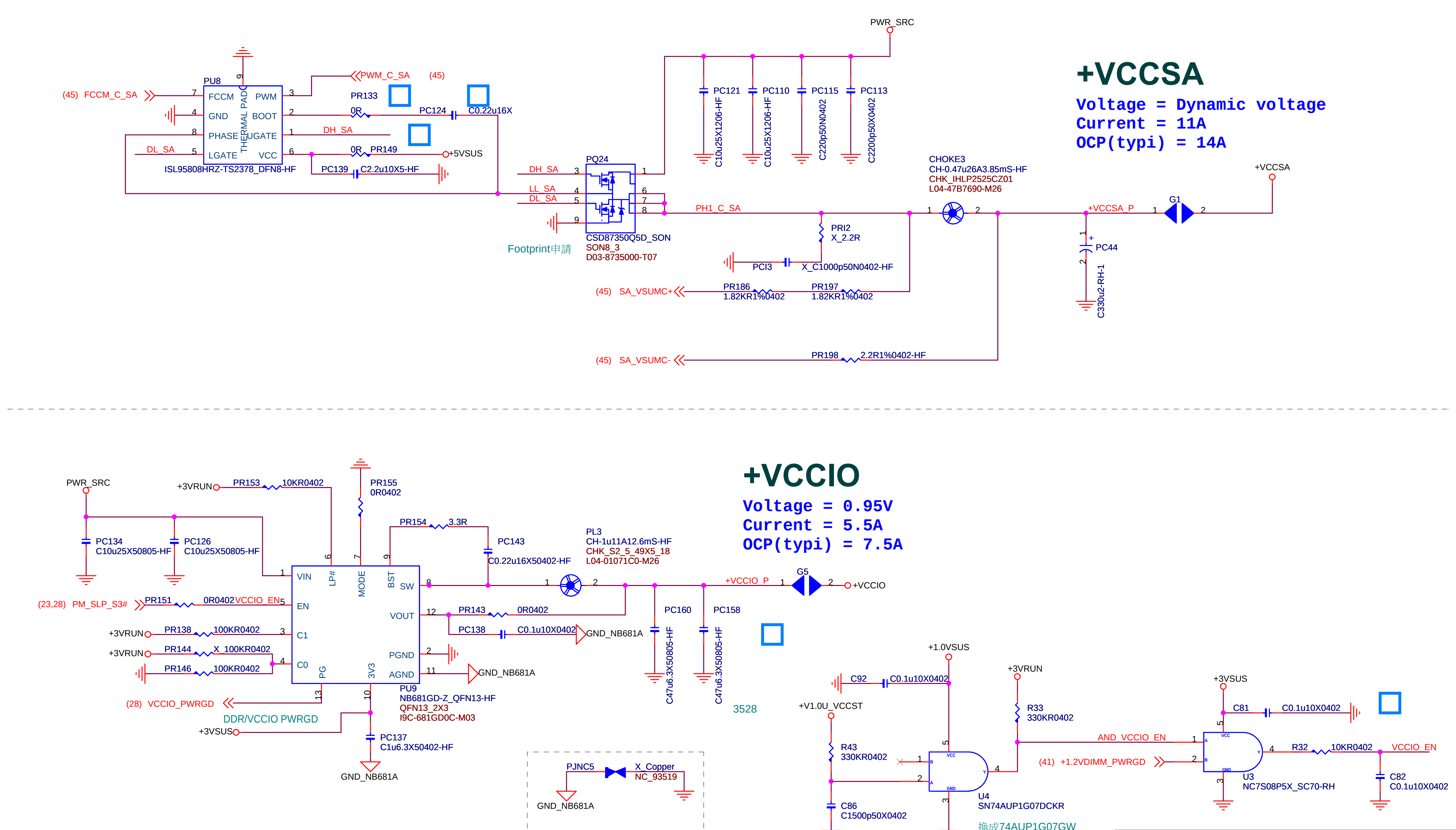

MICRO-STAR INT'L CO.,LTD.

Title: Skylake VCCSA/VCCIO

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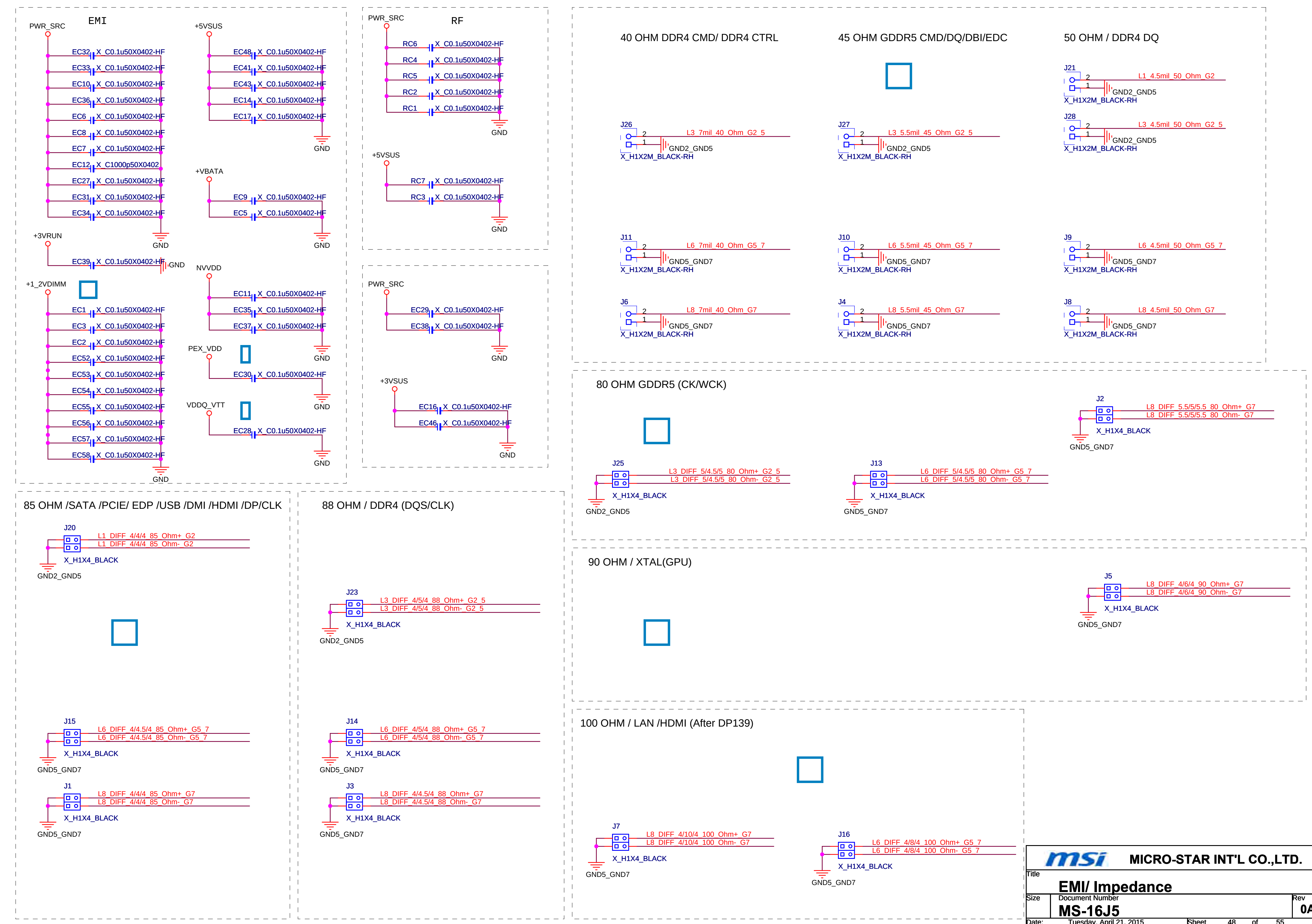

MICRO-STAR INT'L CO.,LTD.

Title: EMI/ Impedance

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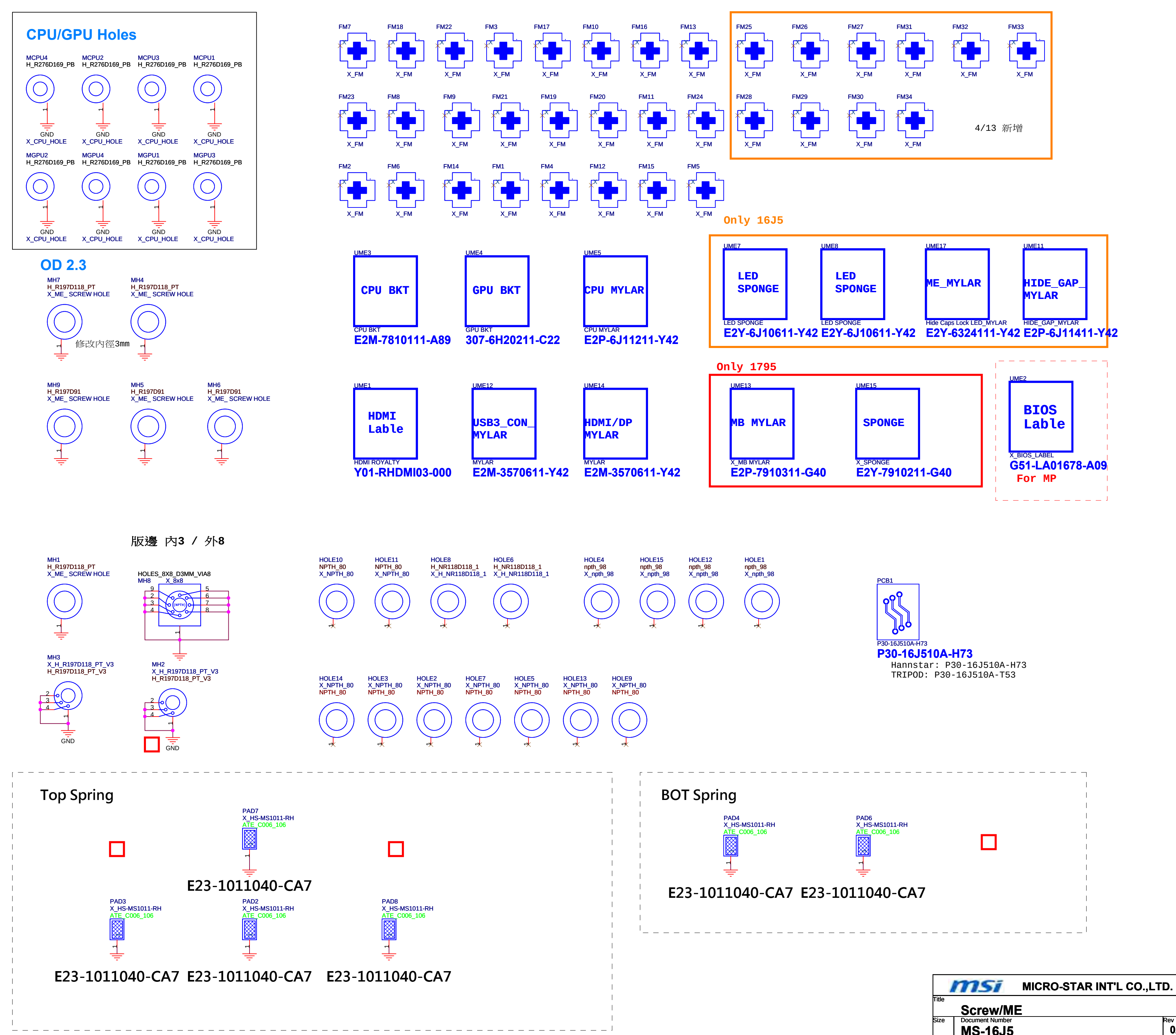

MICRO-STAR INT'L CO.,LTD.

Title	Screw/ME	
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