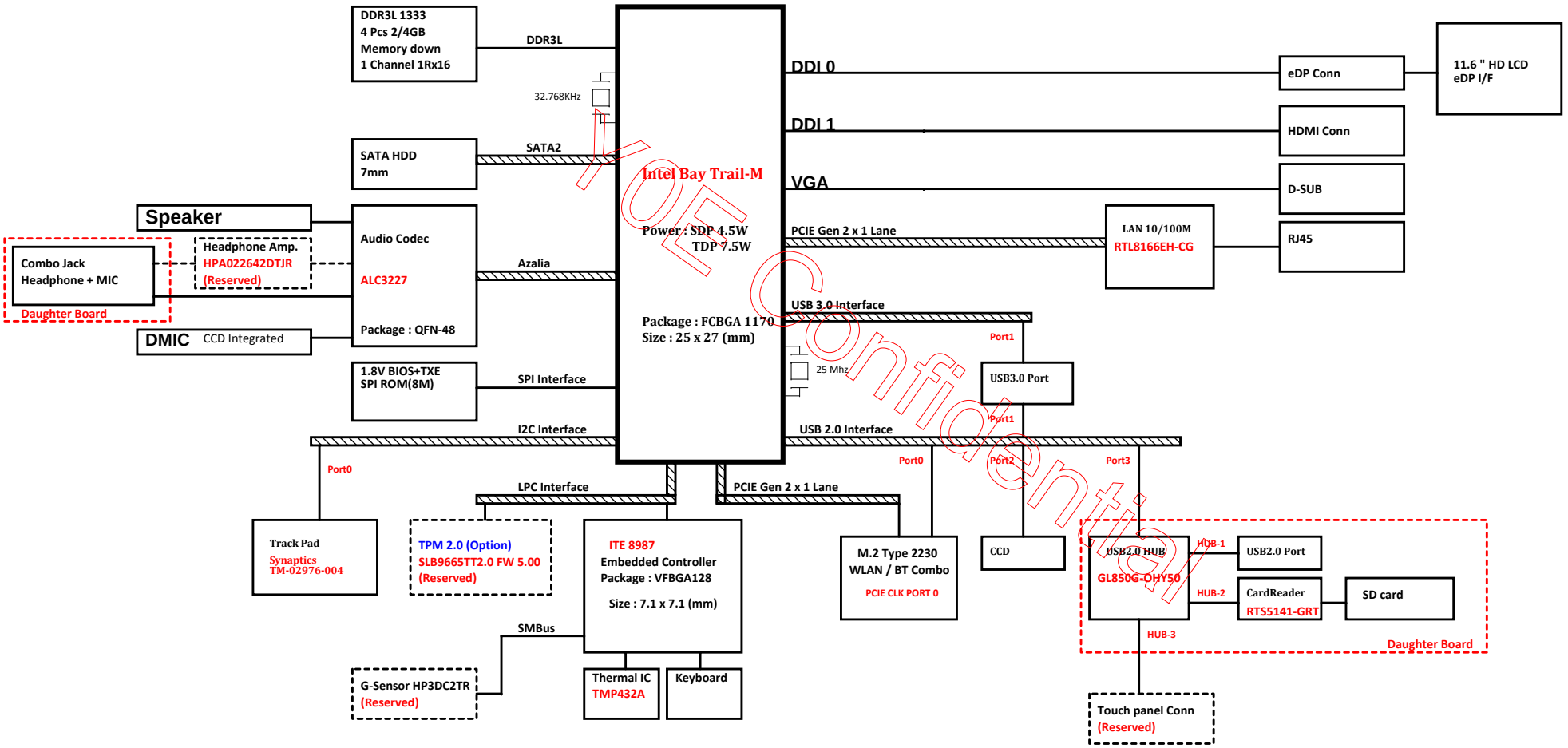
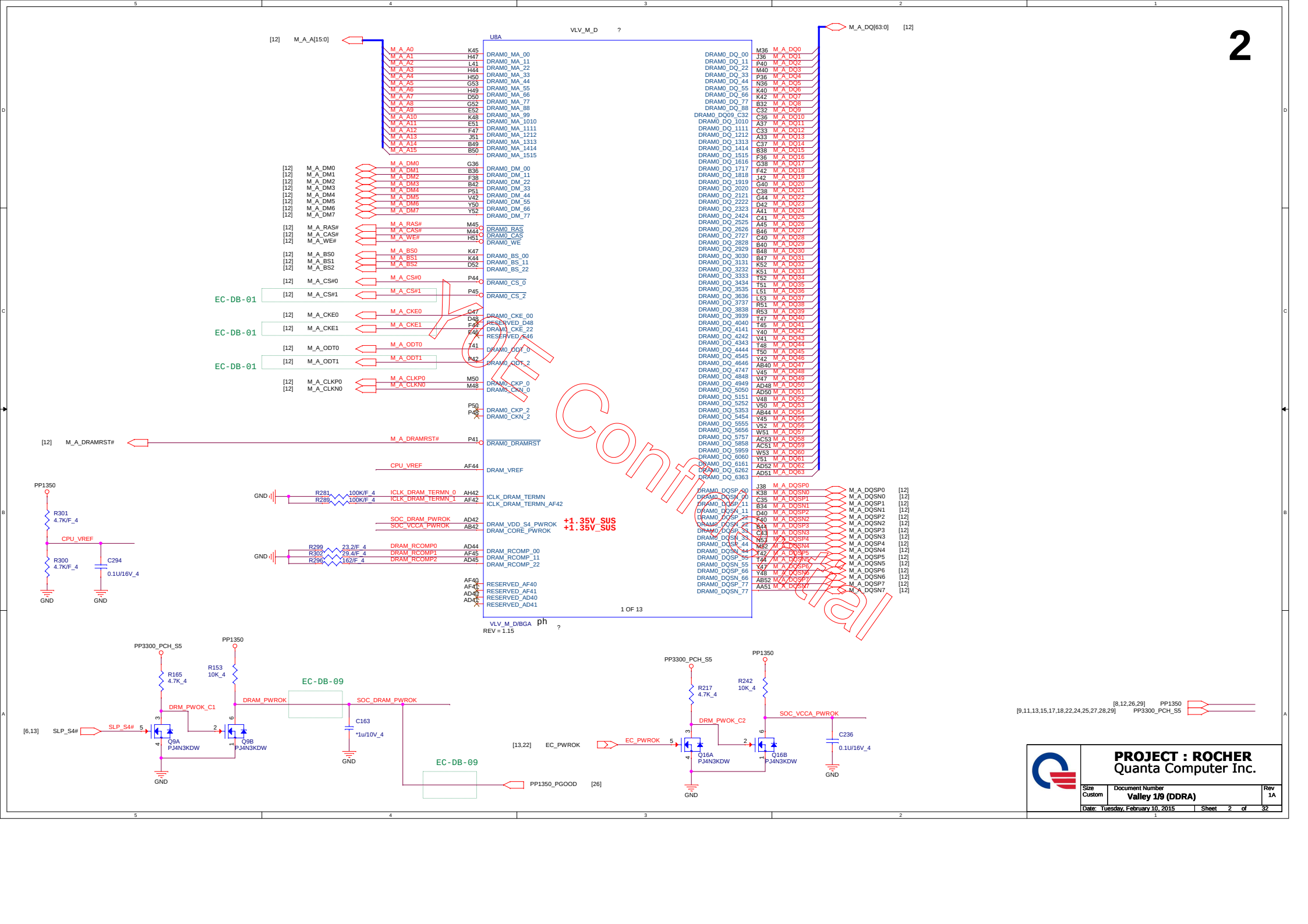
HP Rocher 1.0 RFQ
Intel Bay Trail-M Platform Block Diagram

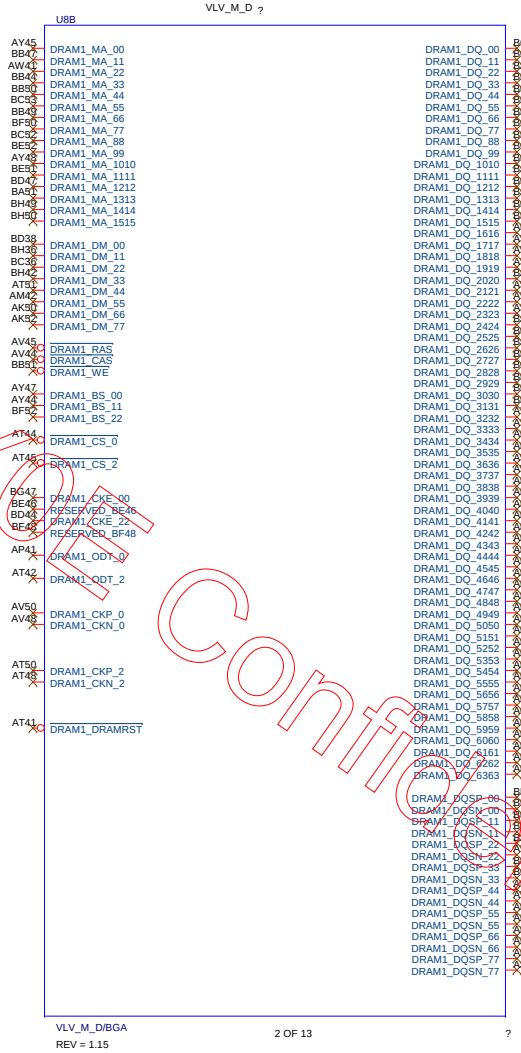


PROJECT : ROCHER
Quanta Computer Inc.

Size	Document Number	Rev
C	Block Diagram	1A

Date: Tuesday, February 10, 2015 | Sheet 1 of 32

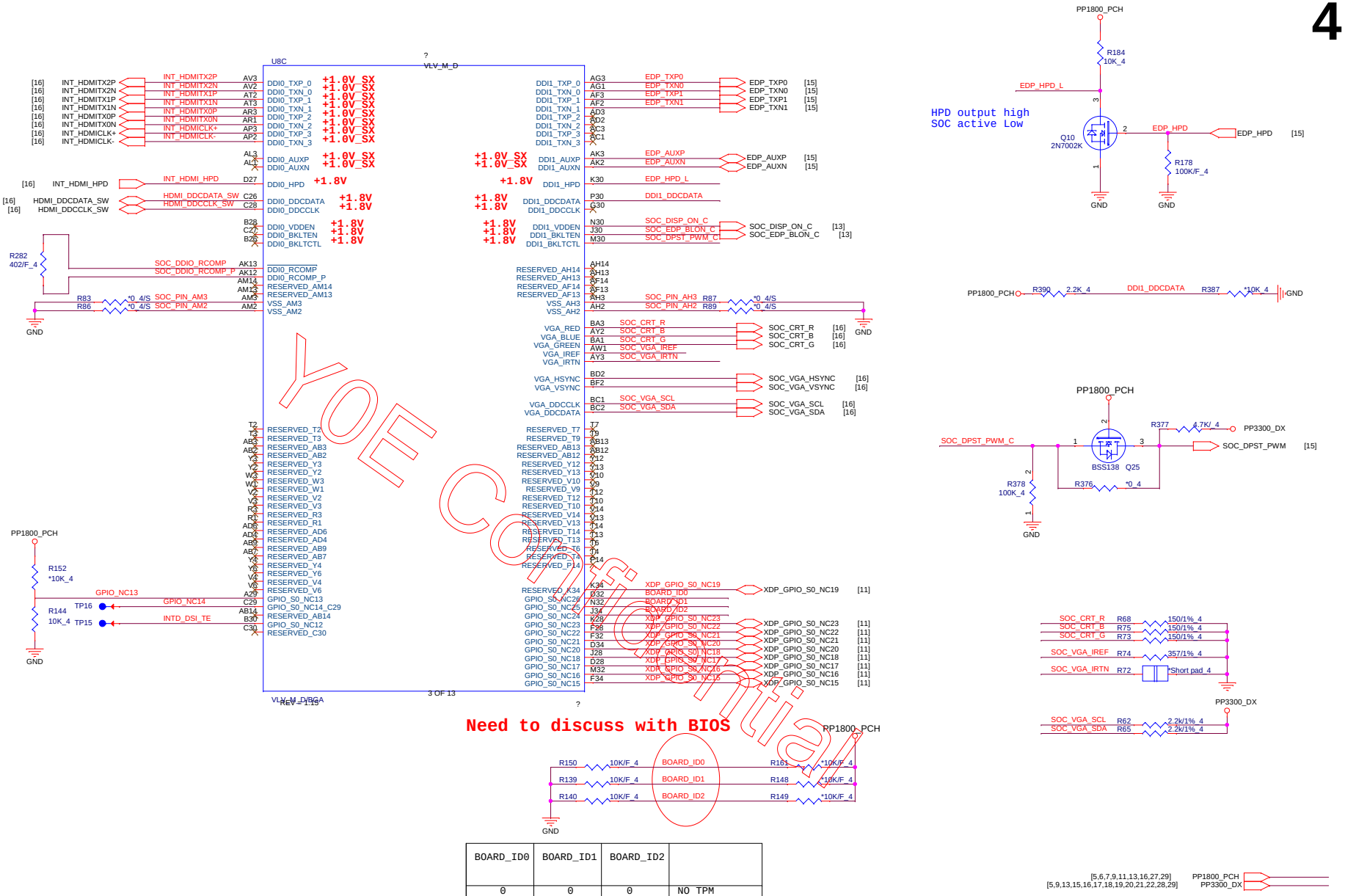

U8A
VLV_M_D ?
[12] M_A_A[15:0]
M_A_DQ[63:0] [12]
DRAM0_MA_00
DRAM0_MA_11
DRAM0_MA_22
DRAM0_MA_33
DRAM0_MA_44
DRAM0_MA_55
DRAM0_MA_66
DRAM0_MA_77
DRAM0_MA_88
DRAM0_MA_99
DRAM0_MA_1010
DRAM0_MA_1111
DRAM0_MA_1212
DRAM0_MA_1313
DRAM0_MA_1414
DRAM0_MA_1515
DRAM0_DM_00
DRAM0_DM_11
DRAM0_DM_22
DRAM0_DM_33
DRAM0_DM_44
DRAM0_DM_55
DRAM0_DM_66
DRAM0_DM_77
DRAM0_RAS
DRAM0_CAS
DRAM0_WE
DRAM0_BS_00
DRAM0_BS_11
DRAM0_BS_22
DRAM0_CS_0
DRAM0_CS_2
DRAM0_CKE_00
RESERVED_D48
DRAM0_CKE_22
RESERVED_E46
DRAM0_ODT_0
DRAM0_ODT_2
DRAM0_CKP_0
DRAM0_CKN_0
DRAM0_CKP_2
DRAM0_CKN_2
DRAM0_DRAMRST
DRAM_VREF
ICLK_DRAM_TERMN
ICLK_DRAM_TERMN_AF42
DRAM_VDD_S4_PWROK
DRAM_CORE_PWROK
DRAM_RCOMP_00
DRAM_RCOMP_11
DRAM_RCOMP_22
RESERVED_AF40
RESERVED_AF41
RESERVED_AD40
RESERVED_AD41
1 OF 13
VLV_M_D/BGA ph ?
REV = 1.15
EC-DB-01
EC-DB-01
EC-DB-01
[12] M_A_DRAMRST#
CPU_VREF
GND
R281 100K/F_4
R289 100K/F_4
SOC_DRAM_PWROK
SOC_VCCA_PWROK
+1.35V_SUS
+1.35V_SUS
R299 23.2/F_4
R302 29.4/F_4
R296 162/F_4
DRAM_RCOMP0
DRAM_RCOMP1
DRAM_RCOMP2
PP1350
R301 4.7K/F_4
R300 4.7K/F_4
C294 0.1U/16V_4
GND
GND
PP3300_PCH_S5
PP1350
R165 4.7K_4
R153 10K_4
DRM_PWOK_C1
DRAM_PWROK
SOC_DRAM_PWROK
EC-DB-09
C163 *1u/10V_4
GND
EC-DB-09
[6,13] SLP_S4#
SLP_S4#
Q9A PJ4N3KDW
Q9B PJ4N3KDW
PP1350_PGOOD [26]
[13,22] EC_PWROK
EC_PWROK
PP3300_PCH_S5
PP1350
R217 4.7K_4
R242 10K_4
DRM_PWOK_C2
SOC_VCCA_PWROK
Q16A PJ4N3KDW
Q16B PJ4N3KDW
C236 0.1U/16V_4
GND
[8,12,26,29] PP1350
[9,11,13,15,17,18,22,24,25,27,28,29] PP3300_PCH_S5
PROJECT : ROCHER
Quanta Computer Inc.
Size Custom
Document Number Valley 1/9 (DDRA)
Rev 1A
Date: Tuesday, February 10, 2015
Sheet 2 of 32



PROJECT : ROCHER
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 2/9 (DDRB)	1A

Date: Tuesday, February 10, 2015 Sheet 3 of 32



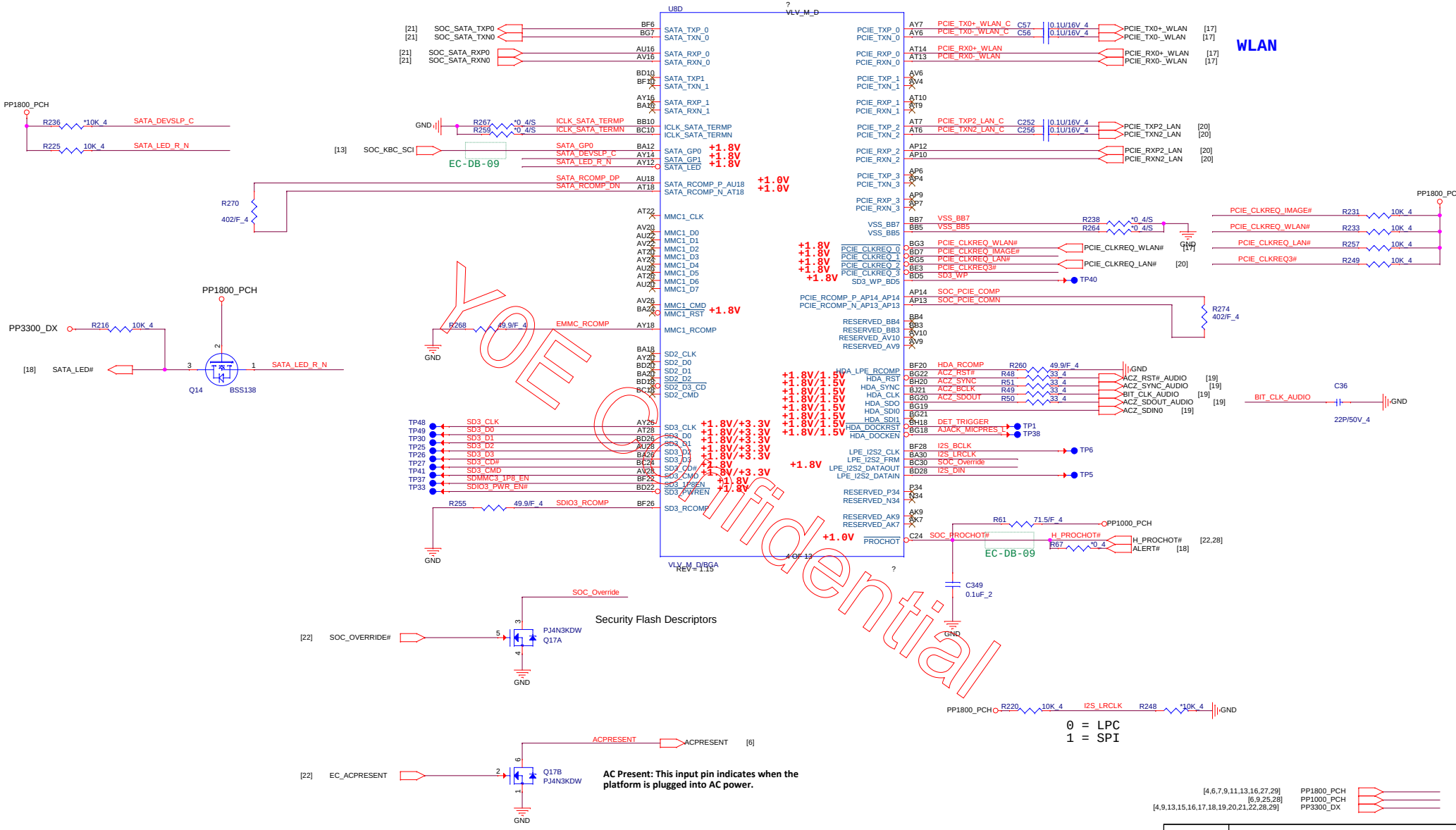
YOE confidential

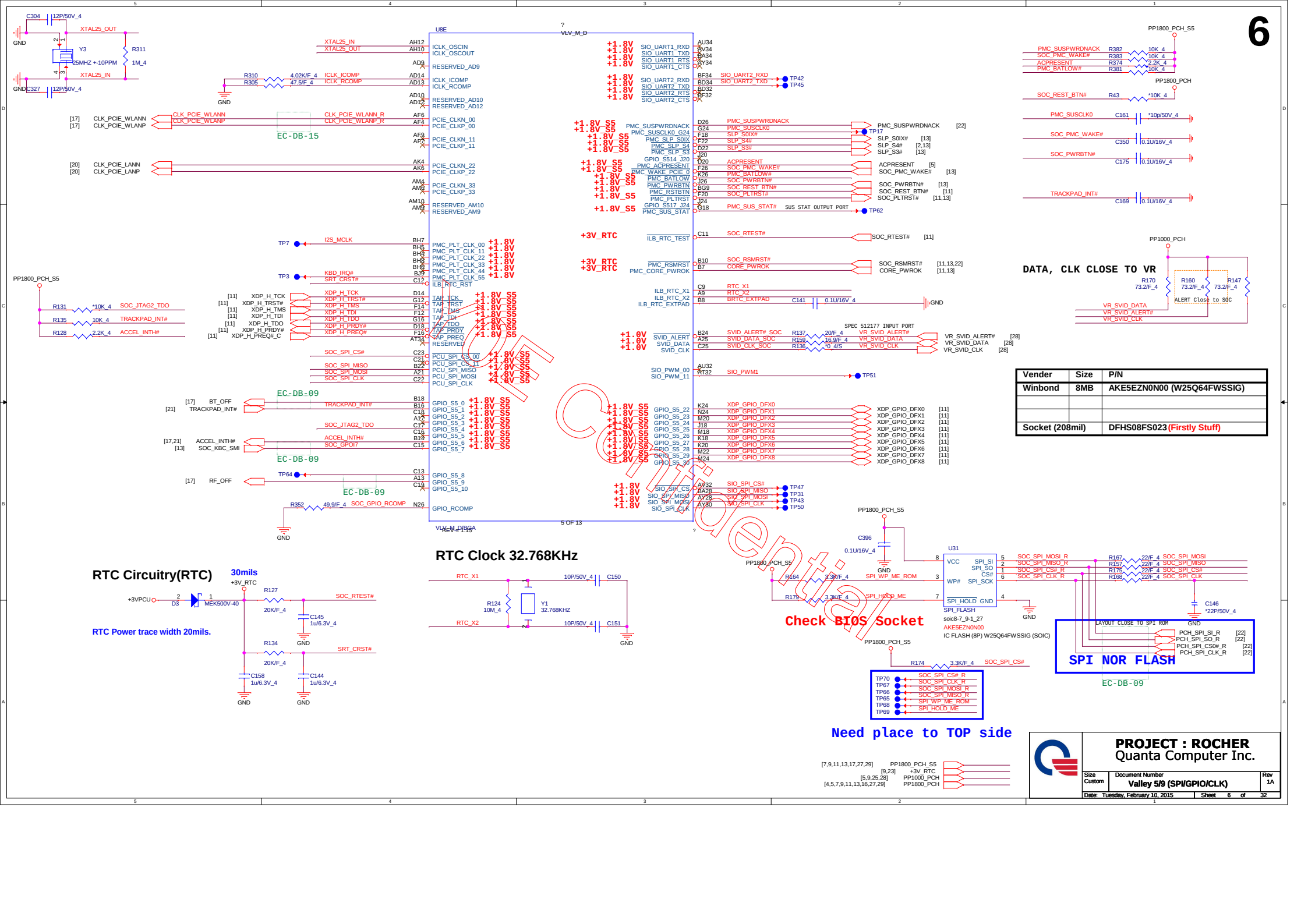
Need to discuss with BIOS

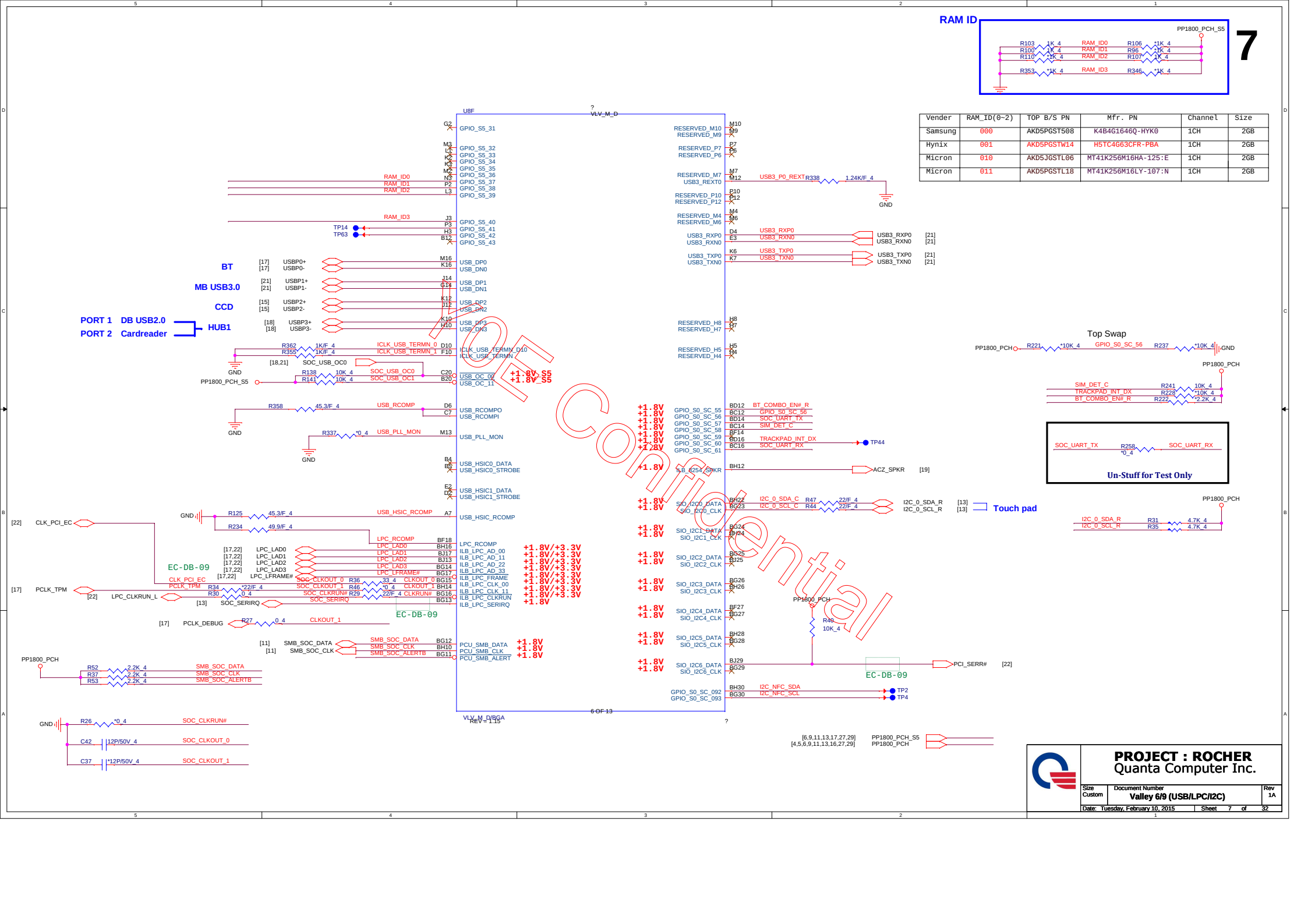
BOARD_ID0	BOARD_ID1	BOARD_ID2	
0	0	0	NO TPM
1	0	0	TPM
0	1	0	

PROJECT : ROCHER
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 3/9 (Display)	1A
Date: Tuesday, February 10, 2015	Sheet 4 of 32	


U8D
VLV_M_D
WLAN
EC-DB-09
Security Flash Descriptors
SOC_Override
ACPRESENT
0 = LPC
1 = SPI
AC Present: This input pin indicates when the platform is plugged into AC power.
Xpec Confidential
VLV_M_D/BGA
REV = 1.15
4 OF 13


6
U8E
VLV_M_D
5 OF 13
VLV_M_D0A
REV = 1.13
RTC Clock 32.768KHz
RTC Circuitry(RTC)
30mils
RTC Power trace width 20mils.
Check BIOS Socket
Need place to TOP side
SPI NOR FLASH
DATA, CLK CLOSE TO VR
Vender | Size | P/N
Winbond | 8MB | AKE5EZN0N00 (W25Q64FWSSIG)
Socket (208mil) | DFHS08FS023 (Firstly Stuff)
PROJECT : ROCHER
Quanta Computer Inc.
Valley 5/9 (SPI/GPIO/CLK)
Rev 1A
Tuesday, February 10, 2015
Sheet 6 of 32
Confidential



Vender	RAM_ID(0~2)	TOP B/S PN	Mfr. PN	Channel	Size
Samsung	000	AKD5PGST508	K4B4G1646Q-HYK0	1CH	2GB
Hynix	001	AKD5PGSTW14	H5TC4G63CFR-PBA	1CH	2GB
Micron	010	AKD5JGSTL06	MT41K256M16HA-125:E	1CH	2GB
Micron	011	AKD5PGSTL18	MT41K256M16LY-107:N	1CH	2GB

PROJECT : ROCHER
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 6/9 (USB/LPC/I2C)	1A

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layout suggestion by intel,
VSS_AXG_SENSE didn't
connect to VSS_SENSE, will
connect the GND via near
VCC_AXG_SENSE

for layout, add 0hm between
GND and VSS_AXG_SENSE

[28] VSS_AXG_SENSE — R263 *0_4/S — GND

+VCC_GFX +VCC_CORE

R278 100/F_4 R345 100/F_4

VCC_SENSE
VCC_AXG_SENSE
VSS_SENSE

R356 100/F_4

GND

U8G

?
VLV_M_D

[28] VCC_SENSE
[28] VCC_AXG_SENSE
[28] VSS_SENSE

P28 CORE_VCC_SENSE_P28
BB8 UNCORE_VNN_SENSE
N28 CORE_VSS_SENSE_N28

PP1350

C257 1U/6.3V_4
C268 1U/6.3V_4
C276 0.1U/16V_4

AD38 DRAM_VDD_S4_AD38
AF38 DRAM_VDD_S4_AF38
A48 DRAM_VDD_S4
AK38 DRAM_VDD_S4_AK38
AM38 DRAM_VDD_S4_AM38
AV41 DRAM_VDD_S4_AV41
AV42 DRAM_VDD_S4_AV42
BB46 DRAM_VDD_S4_BB46

+VCC_CORE

C282 22uF/6.3VT_6
C296 22uF/6.3VT_6
C302 22uF/6.3VT_6
C321 10uF/6.3V_4
C137 10u/6.3V_4
C355 22u/6.3V_8
C344 22u/6.3V_8
C126 22u/6.3V_6
C360 22u/6.3V_6
C364 22u/6.3V_8
C123 22u/6.3V_8
C124 22u/6.3V_8

AA27 CORE_VCC_S0IX_AA27
AA29 CORE_VCC_S0IX_AA29
AA30 CORE_VCC_S0IX_AA30
AC27 CORE_VCC_S0IX_AC27
AC29 CORE_VCC_S0IX_AC29
AC30 CORE_VCC_S0IX_AC30
AD27 CORE_VCC_S0IX_AD27
AD29 CORE_VCC_S0IX_AD29
AD30 CORE_VCC_S0IX_AD30
AF27 CORE_VCC_S0IX_AF27
AF29 CORE_VCC_S0IX_AF29
AG27 CORE_VCC_S0IX_AG27
AG29 CORE_VCC_S0IX_AG29
AG30 CORE_VCC_S0IX_AG30
P26 CORE_VCC_S0IX_P26
P27 CORE_VCC_S0IX_P27
U27 CORE_VCC_S0IX_U27
U29 CORE_VCC_S0IX_U29
V27 CORE_VCC_S0IX_V27
V29 CORE_VCC_S0IX_V29
V30 CORE_VCC_S0IX_V30
Y27 CORE_VCC_S0IX_Y27
Y29 CORE_VCC_S0IX_Y29
Y30 CORE_VCC_S0IX_Y30

AF30 TP_CORE_V1P05_S4

7 OF 13

VLV_M_D/BGA
REV = 1.15

DRAM_VDD_S4_BD49 BD49
DRAM_VDD_S4_BD52 BD52
DRAM_VDD_S4_BD53 BD53
DRAM_VDD_S4_BF44 BF44
DRAM_VDD_S4_BG51 BG51
DRAM_VDD_S4_BJ48 BJ48
DRAM_VDD_S4_C51 C51
DRAM_VDD_S4_D44 D44
DRAM_VDD_S4_F49 F49
DRAM_VDD_S4_F52 F52
DRAM_VDD_S4_F53 F53
DRAM_VDD_S4_H46 H46
DRAM_VDD_S4_M41 M41
DRAM_VDD_S4_M42 M42
DRAM_VDD_S4_V38 V38
DRAM_VDD_S4_Y38 Y38

PP1350

C346 1U/6.3V_4
C351 22uF/6.3VT_6
C237 1U/6.3V_4
C247 22uF/6.3VT_6
C244 1U/6.3V_4
C246 22uF/6.3VT_6

GND

UNCORE_VNN_S3_AA24 AA24
UNCORE_VNN_S3_AC22 AC22
UNCORE_VNN_S3_AC24 AC24
UNCORE_VNN_S3_AD22 AD22
UNCORE_VNN_S3_AD24 AD24
UNCORE_VNN_S3_AF22 AF22
UNCORE_VNN_S3_AF24 AF24
UNCORE_VNN_S3_AG22 AG22
UNCORE_VNN_S3_AG24 AG24
UNCORE_VNN_S3_AJ22 AJ22
UNCORE_VNN_S3_AJ24 AJ24
UNCORE_VNN_S3_AK22 AK22
UNCORE_VNN_S3_AK24 AK24
UNCORE_VNN_S3_AK25 AK25
UNCORE_VNN_S3_AK27 AK27
UNCORE_VNN_S3_AK29 AK29
UNCORE_VNN_S3_AK30 AK30
UNCORE_VNN_S3_AK32 AK32
UNCORE_VNN_S3_AM22 AM22

TP2_CORE_VCC_S0IX AA12

+VCC_GFX

C273 10uF/6.3V_4
C119 10U/6.3V_6
C293 10U/6.3V_6
C121 22u/6.3V_6
C278 10u/6.3V_4
C308 10u/6.3V_4
C301 22u/6.3V_6
C120 22u/6.3V_6

GND

C297 22uF/6.3VT_6
C283 22uF/6.3VT_6
C269 22uF/6.3VT_6

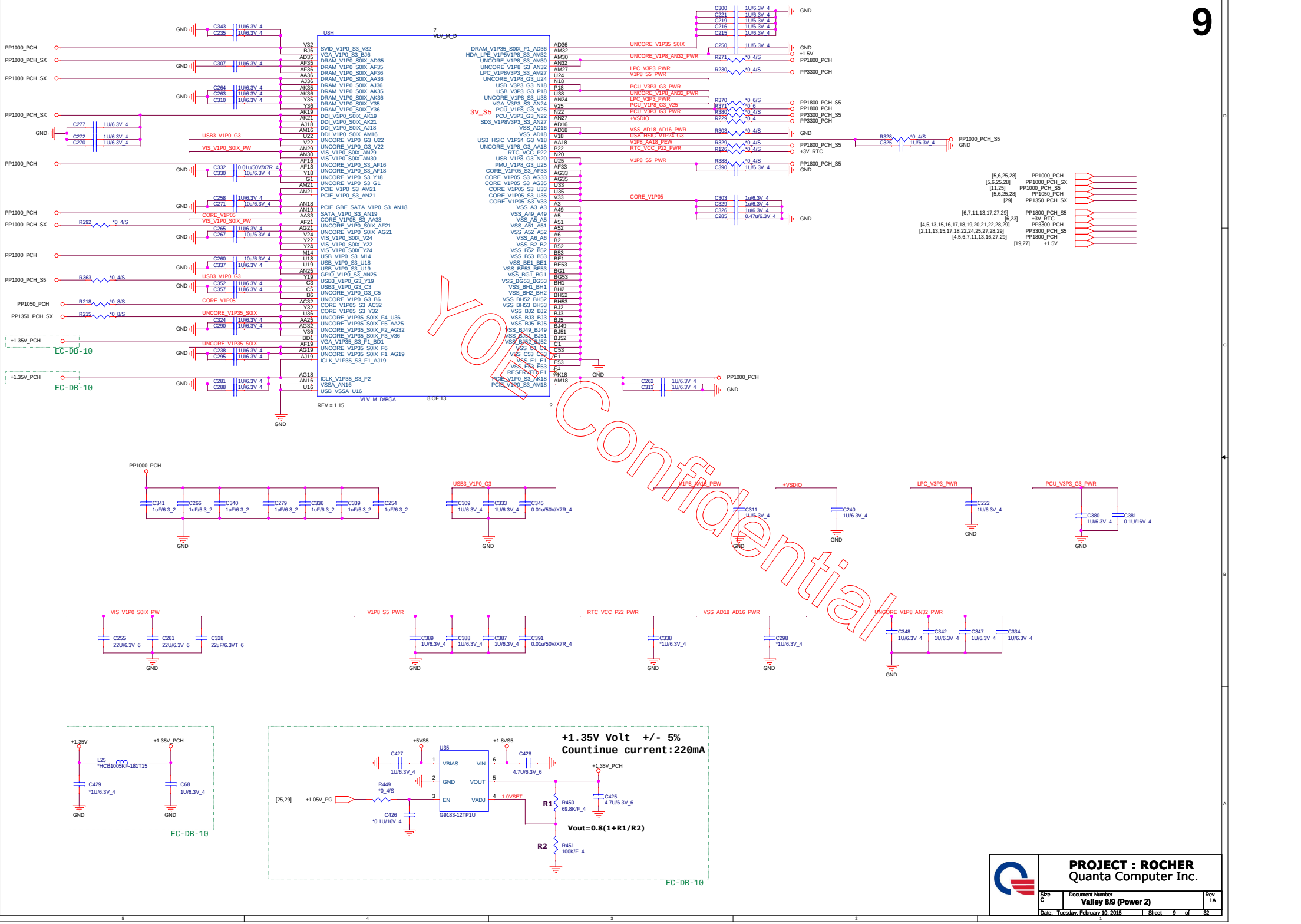
+VCC_GFX

C322 22u/6.3V_8

[28] +VCC_GFX
[28] +VCC_CORE
[2,12,26,29] PP1350

PROJECT : ROCHER
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 7/9 (Power 1)	1A
Date: Tuesday, February 10, 2015	Sheet 8 of 32	


U8H
VLV_M_D
VLV_M_D/BGA
8 OF 13
REV = 1.15
3V_S5
EC-DB-10
EC-DB-10
EC-DB-10
PP1000_PCH
PP1000_PCH_SX
PP1000_PCH_S5
PP1050_PCH
PP1350_PCH_SX
+1.35V_PCH
USB3_V1P0_G3
VIS_V1P0_S0IX_PW
CORE_V1P05
UNCORE_V1P35_S0IX
UNCORE_V1P8_AN32_PWR
LPC_V3P3_PWR
PCU_V3P3_G3_PWR
+VSDIO
V1P8_S5_PWR
RTC_VCC_P22_PWR
VSS_AD18_AD16_PWR
+1.35V Volt +/- 5%
Countinue current:220mA
Vout=0.8(1+R1/R2)
G9183-12TP1U
Confidential
PROJECT : ROCHER
Quanta Computer Inc.
Valley 8/9 (Power 2)
Rev 1A
Tuesday, February 10, 2015
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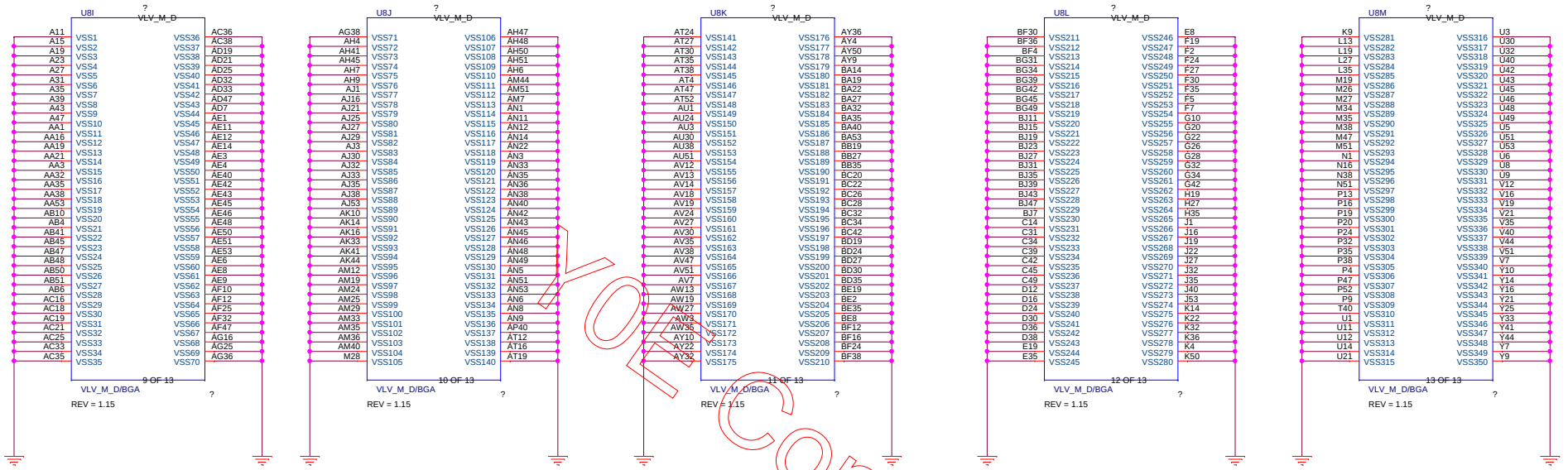
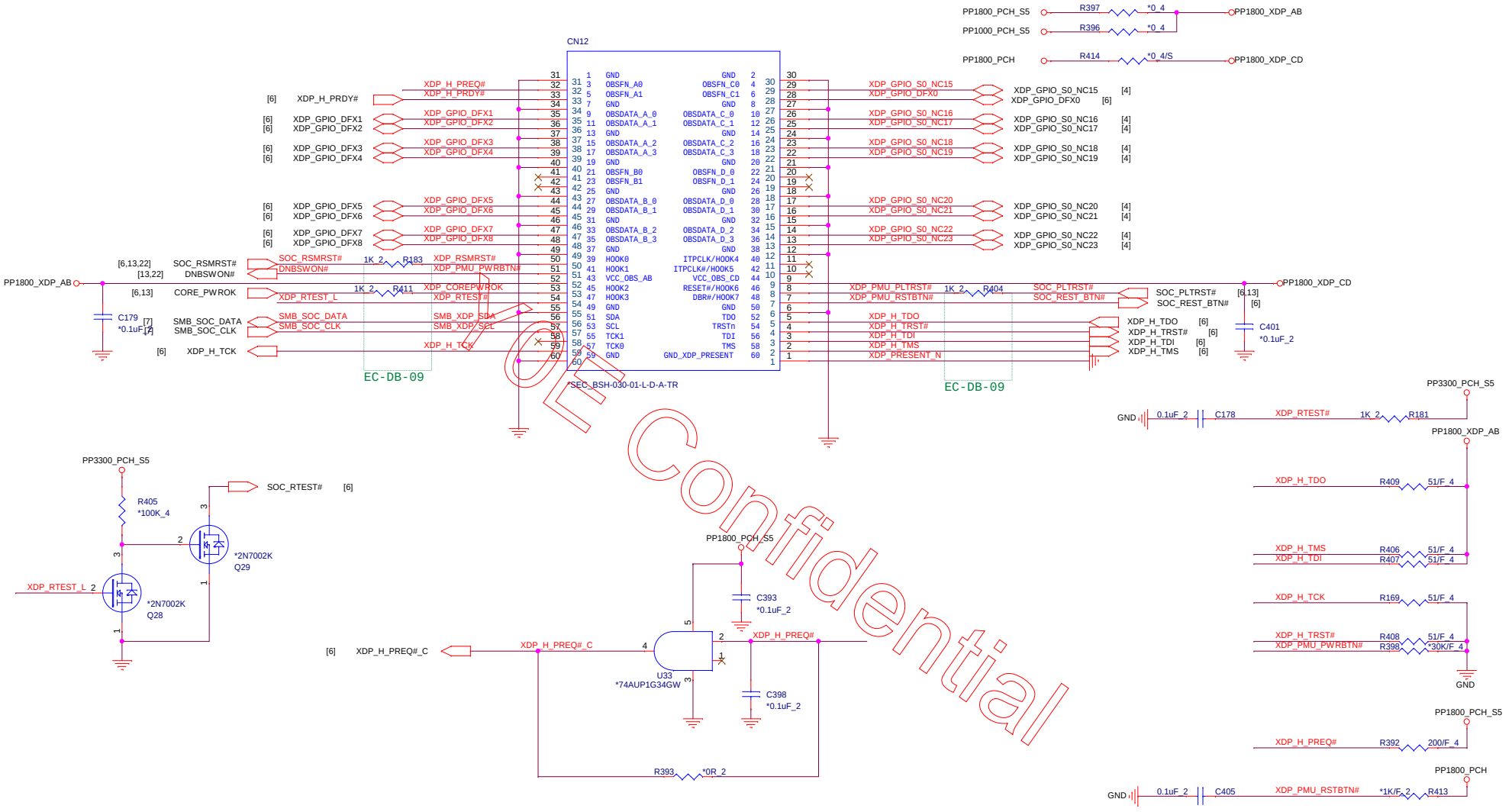


PROJECT : ROCHER
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Valley 9/9 (GND)	1A

Date: Tuesday, February 10, 2015 | Sheet 10 of 32

INTEL Debug Port

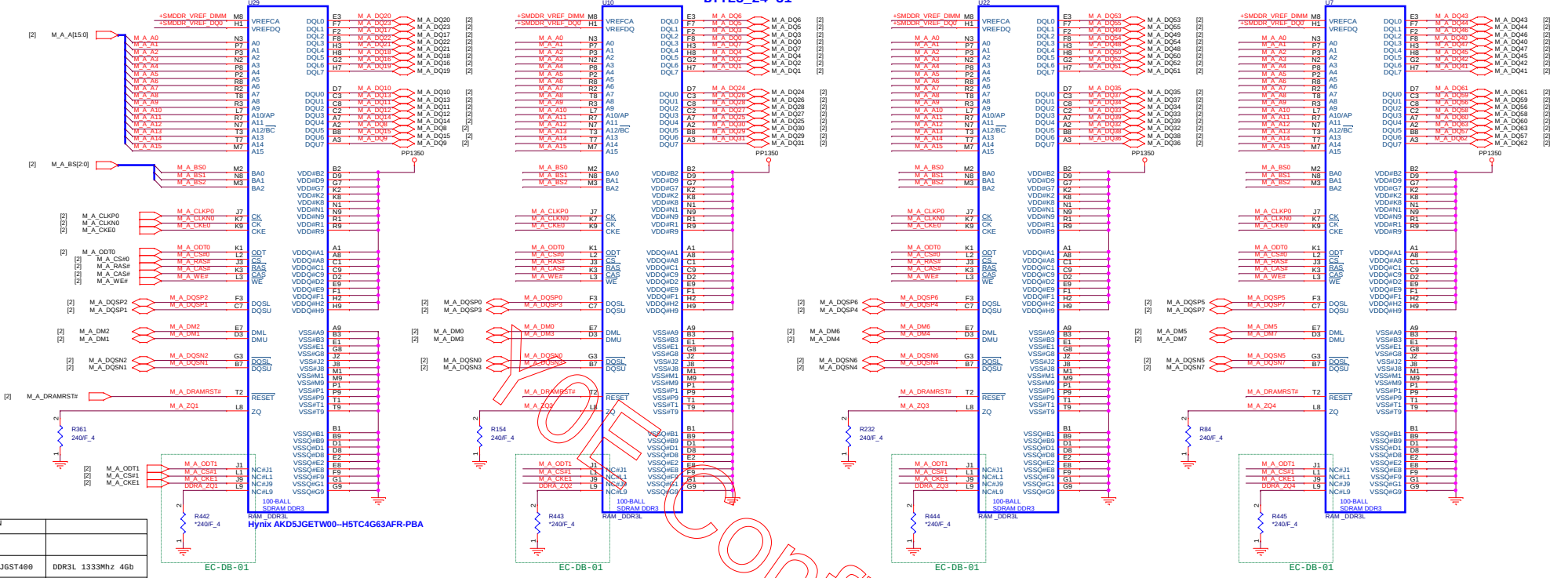


[2,9,13,15,17,18,22,24,25,27,28,29] PP3300_PCH_S5
[6,7,9,13,17,27,29] PP1800_PCH_S5
[4,5,6,7,9,13,16,27,29] PP1800_PCH
[9,25] PP1000_PCH_S5

PROJECT : ROCHER
Quanta Computer Inc.

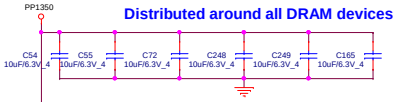
Size	Document Number	Rev
Custom	CPU/PCH XDP	1A
Date: Tuesday, February 10, 2015	Sheet 11 of 32	

BYTE2_16-23
BYTE1_8-15
BYTE0_0-7
BYTE3_24-31
BYTE4_32-39
BYTE6_48-55
BYTE5_40-47
BYTE7_56-63

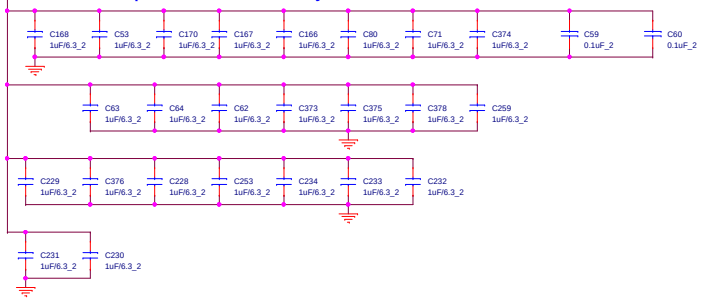


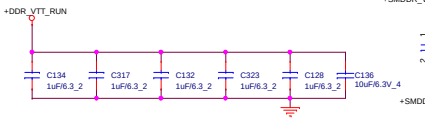
Vendor	P/N	
Hynix		
Elpida	AKD5JGST400	DDR3L 1333Mhz 4Gb
	AKD5JGST404	DDR3L 1600Mhz 4Gb

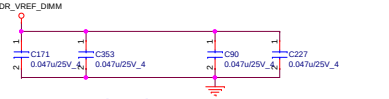
Distributed around all DRAM devices (CHA and CHB)

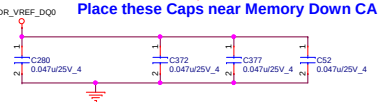


Place these Caps near each X16 Memory Down

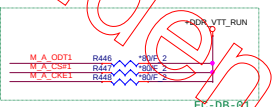


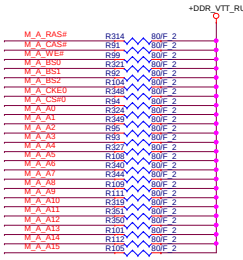


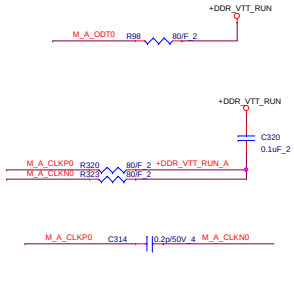




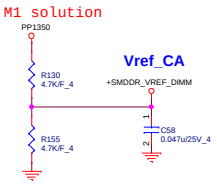
Place these Caps near Memory Down CA & DQ pin



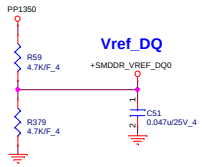




M1 solution



M1 solution

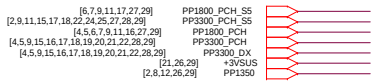


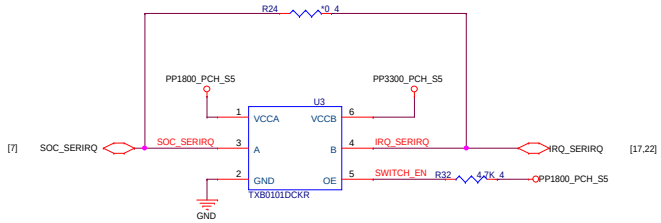
[2,8,26,29] PP1350
[26] +DDR_VTT_RUN

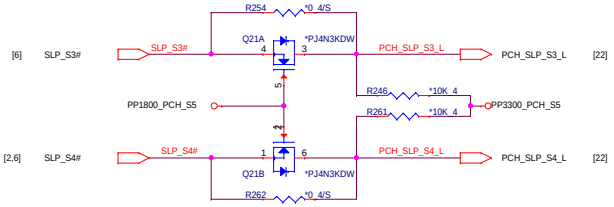
PROJECT : ROCHER
Quanta Computer Inc.

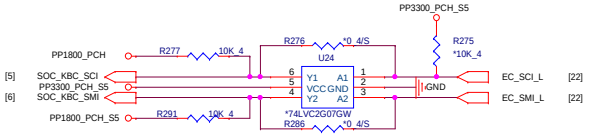
Size	Document Number	Rev
Custom	DDR3L MEMORY DOWNx16 A	1A

Date: Tuesday, February 10, 2015 | Sheet 12 of 32

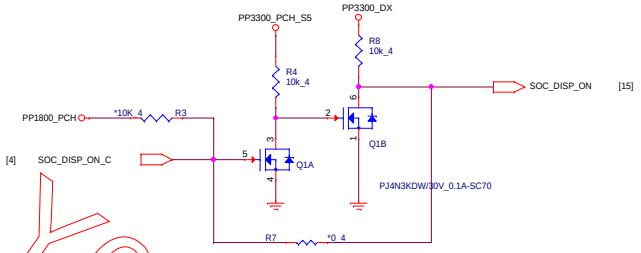


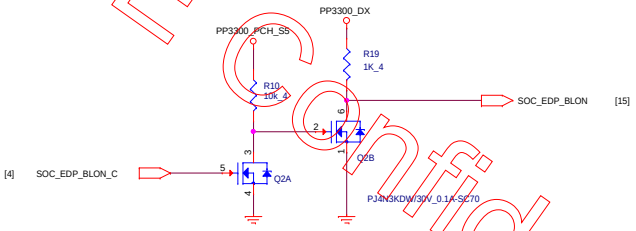




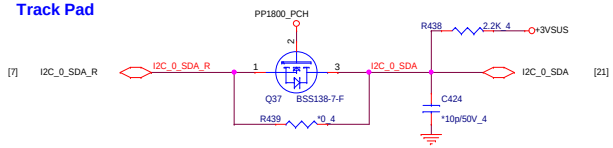


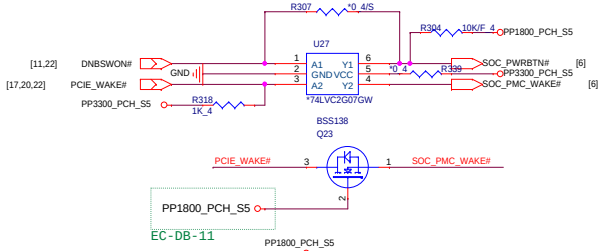
eDP control pin (For eDP)

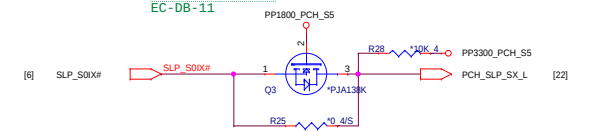


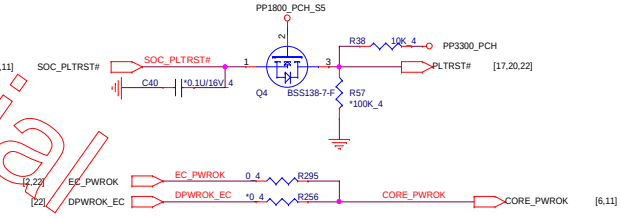


Track Pad









PROJECT : ROCHER
Quanta Computer Inc.

Size	Document Number	Rev
C	Level Shfiter (SOC_EC)	1A

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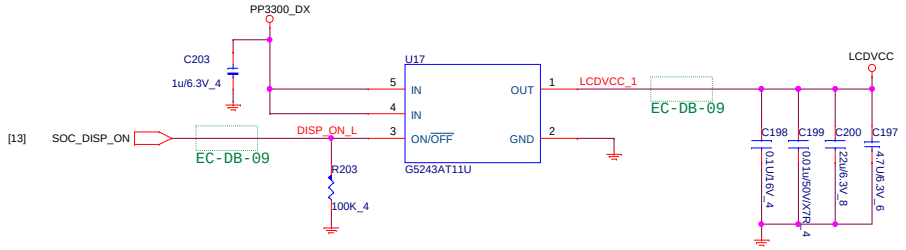
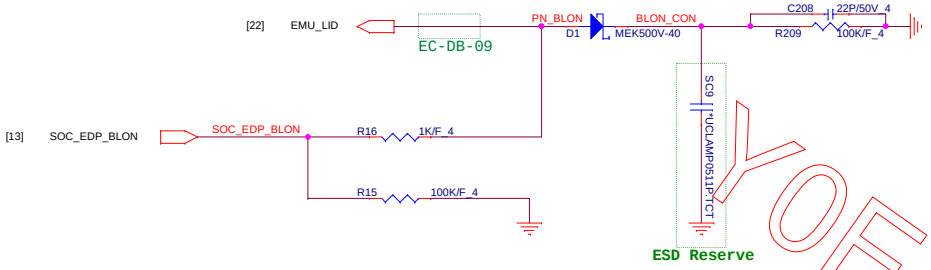
2014/11/11 remove eDP to LVDS converter

	PROJECT : ROCHER Quanta Computer Inc.	
Size Custom	Document Number **LVDS converter RTD2132N**	Rev 1A
Date: Tuesday, February 10, 2015	Sheet 14 of 32	

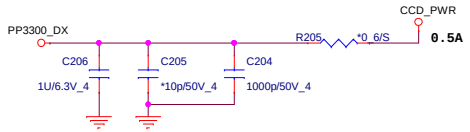
eDP /LVDS Power(VGA)



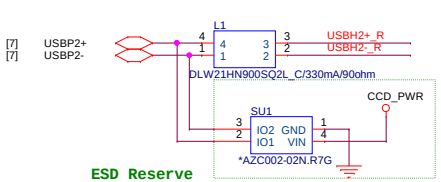
LID Switch



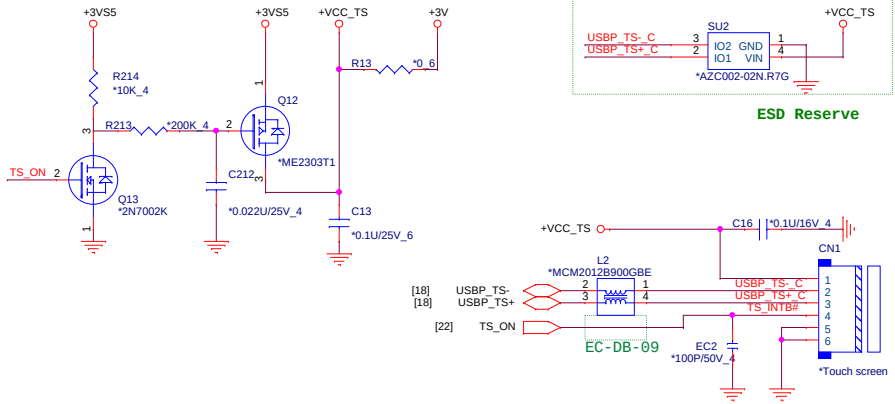
CCD power(CCD)

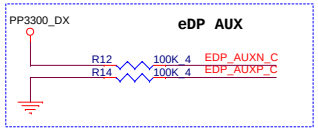


CCD USB(CCD)



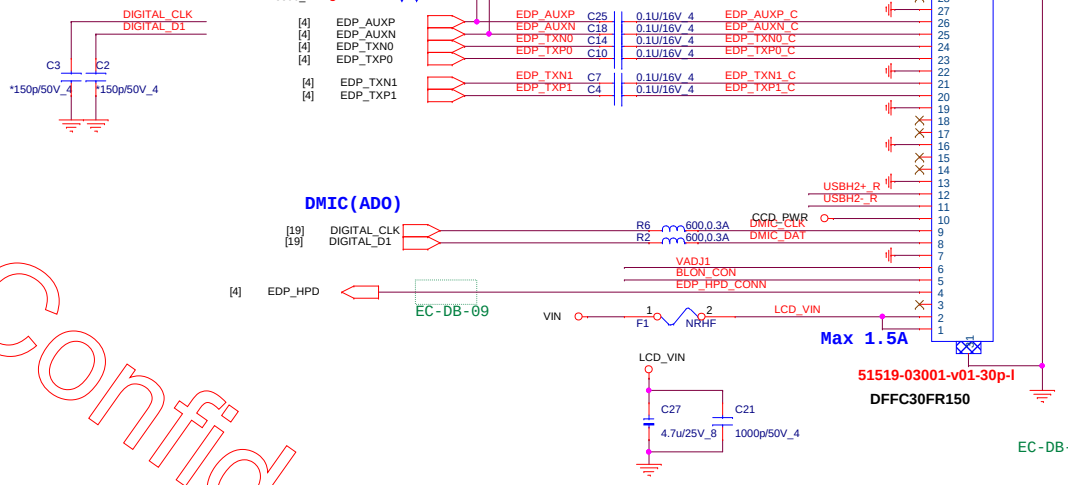
Touch screen

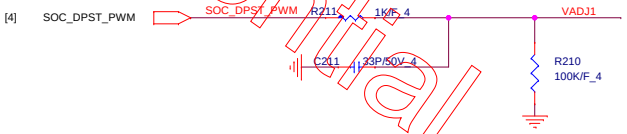




eDP/LVDS

Need New LCD Cable





[4,5,9,13,16,17,18,19,20,21,22,28,29] PP3300_DX
[18,23,24,25,26,28,29,30] VIN
[4,5,9,13,16,17,18,19,20,21,22,28,29] +3V
[2,9,11,13,17,18,22,24,25,27,28,29] +3VS5

PROJECT : ROCHER
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS/eDP/CCD/DMIC	1A
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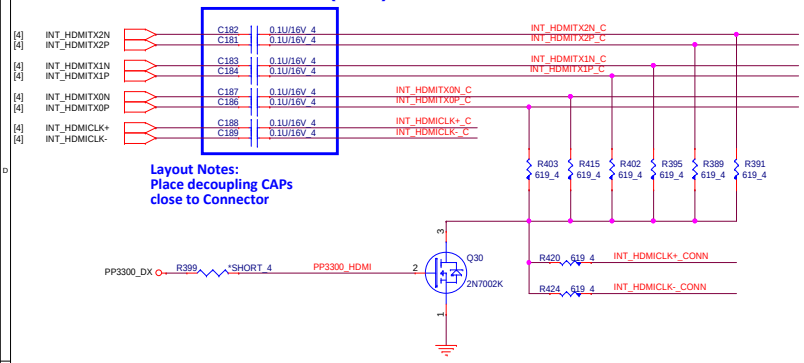
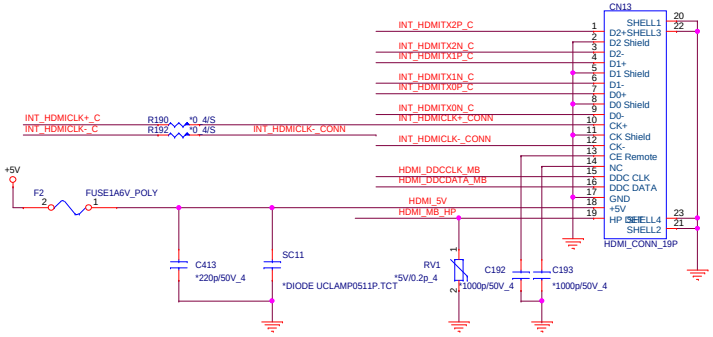
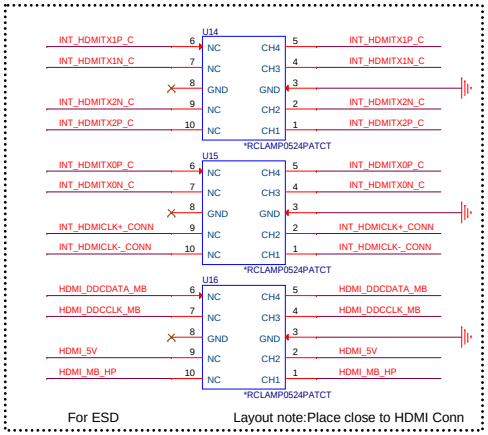
HDMI Cost Reduced level shift (HDM)



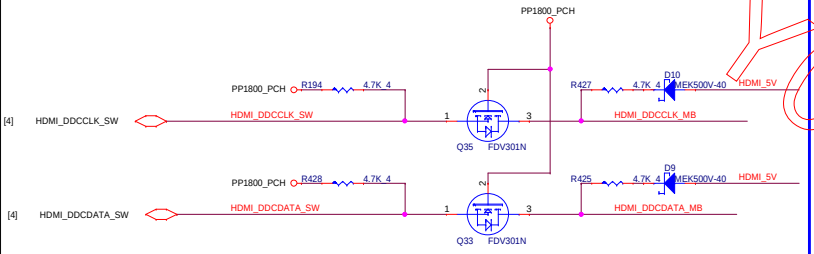
HDMI connector (HDM)



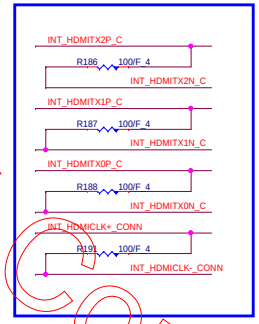
ESD 靠近HDMI CONNECTOR(CN9)



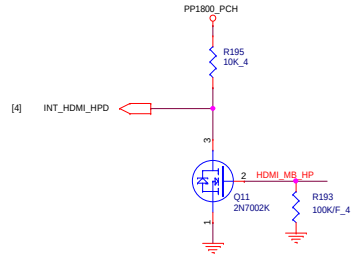
HDMI DDC (HDM)

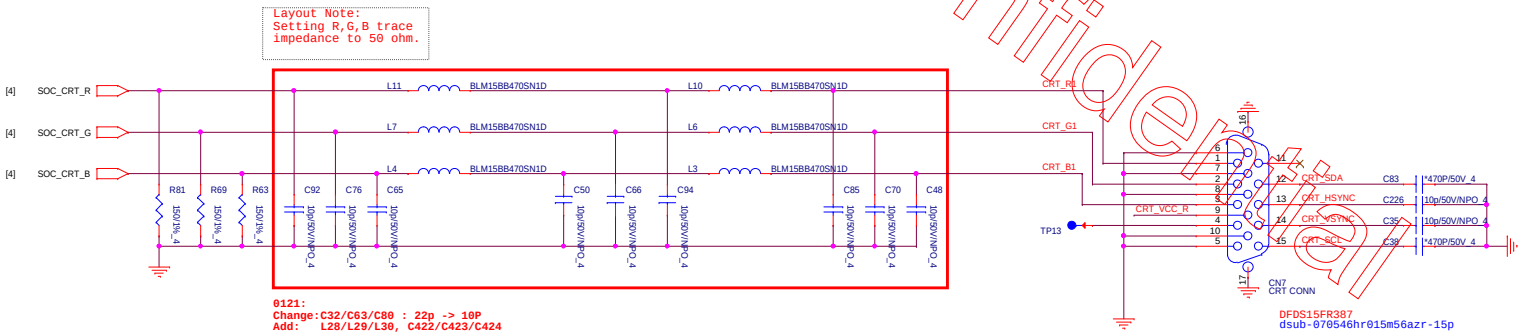


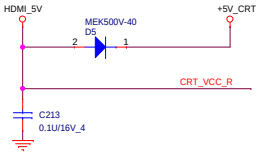
EMI



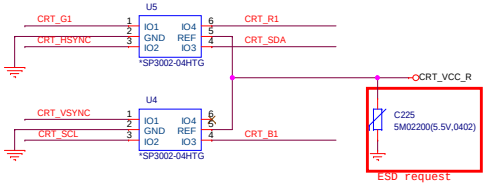
HDMI-detect (HDM)

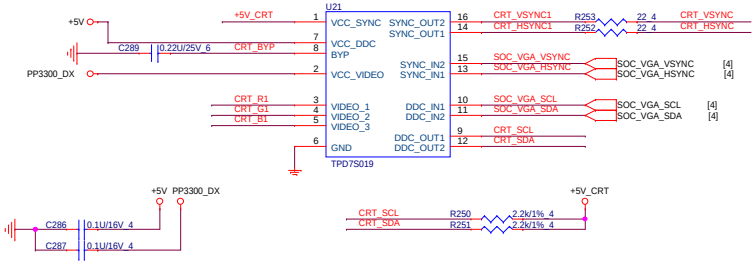






ESD PROTECTION





[4,5,9,13,15,17,18,19,20,21,22,28,29] PP3300_DX
[4,5,6,7,9,11,13,27,29] PP1800_PCH
[17,19,21,29] +5V

PROJECT : ROCHER Quanta Computer Inc.		
Size: C	Document Number: HDMI	Rev: 1A
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Mini Card WLAN/BT

BT

Mini Card
WLAN/BT(Option)

H=4.0

NGFF

CN5

NGFF_CONN_75P

EC-DB-04

EC-DB-09

Support Wake Function(Reserve)

For EMI Suggestion

TPM (CLG)

TPM SLB9655

*SLB9660TT1.2

4 x100nF (place close to device VDD/GND pins)

pin5,6,9,19,25,28 are difference between both

If stuff ST TPM,C250
change to 10uF
(CH6101M9B02)

near pin 21 as possible

FAE : a 0ohm between pin9 to LRESET signals

add pullup 10K on
SERIRQ_R to TPM_VDD

LID

LID SENSOR

APX9132H

Accelerometer Sensor

AL003DC2A00

PROJECT : ROCHER	
Quanta Computer Inc.	
Size: C	Document Number: WLAN/TPM/LED/LID/SW
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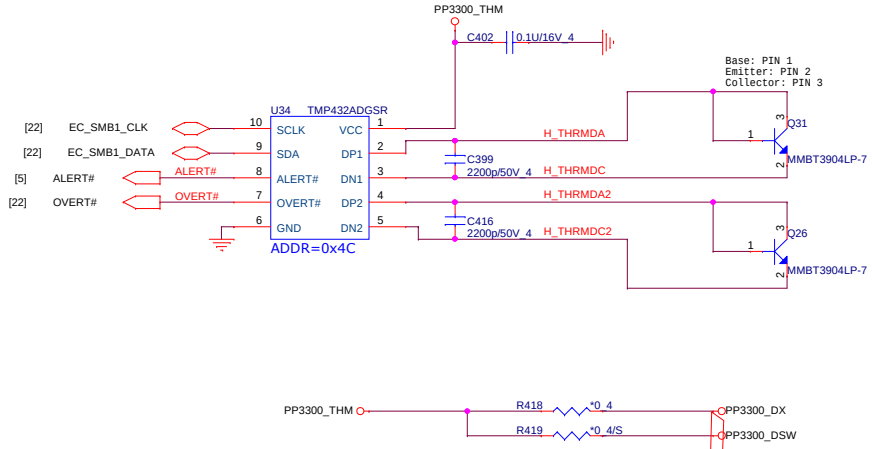
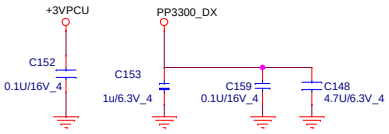
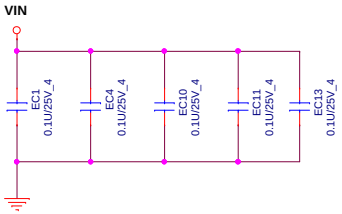
Thermal Sensor(THM)



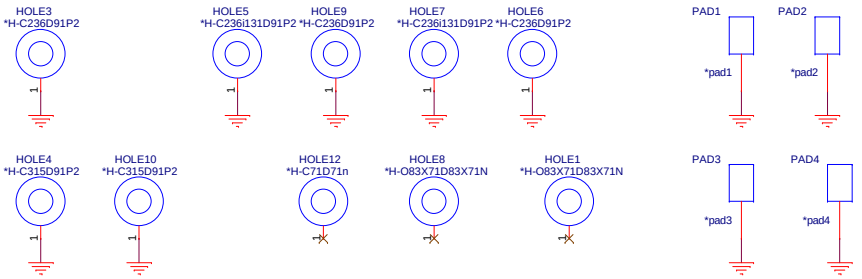




EC-PV-07

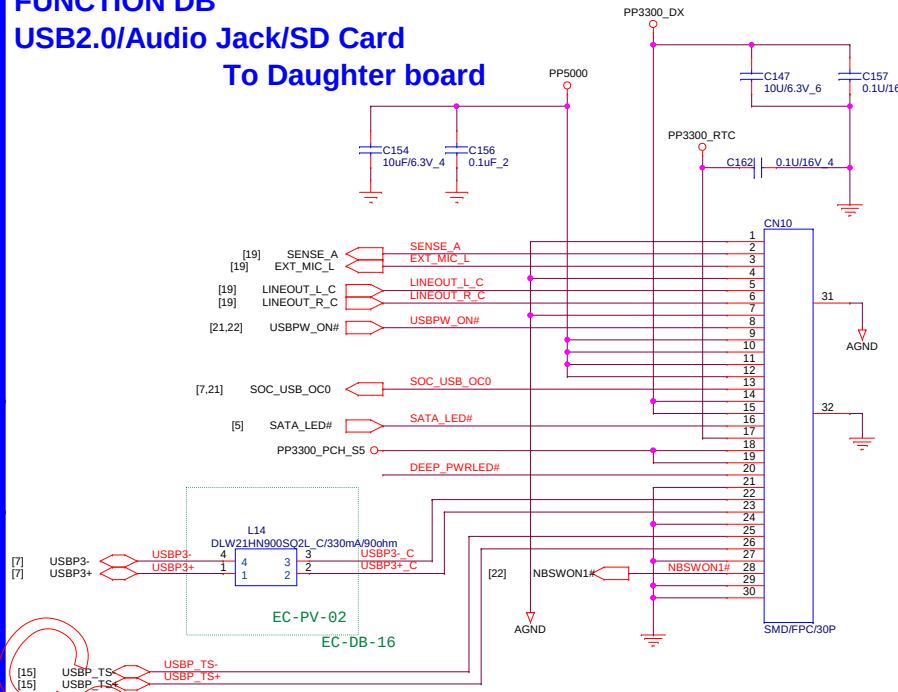
HOLE(OTH)

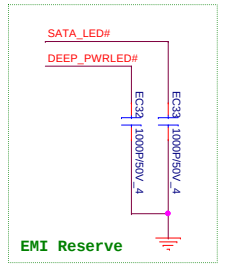
EC-PV-06

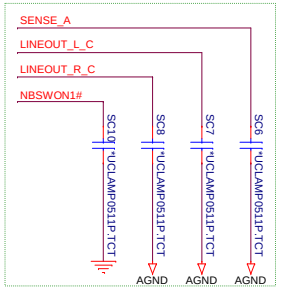


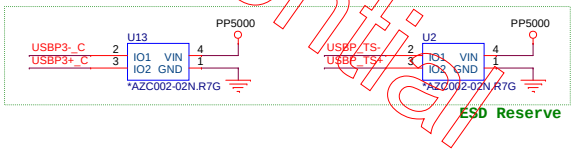
FUNCTION DB
USB2.0/Audio Jack/SD Card
To Daughter board

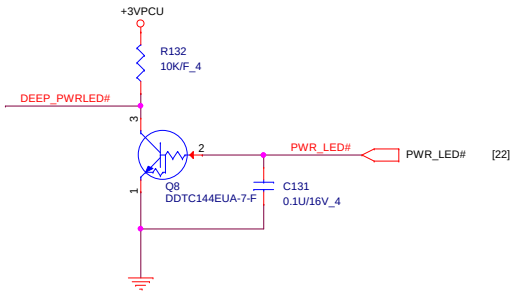
18







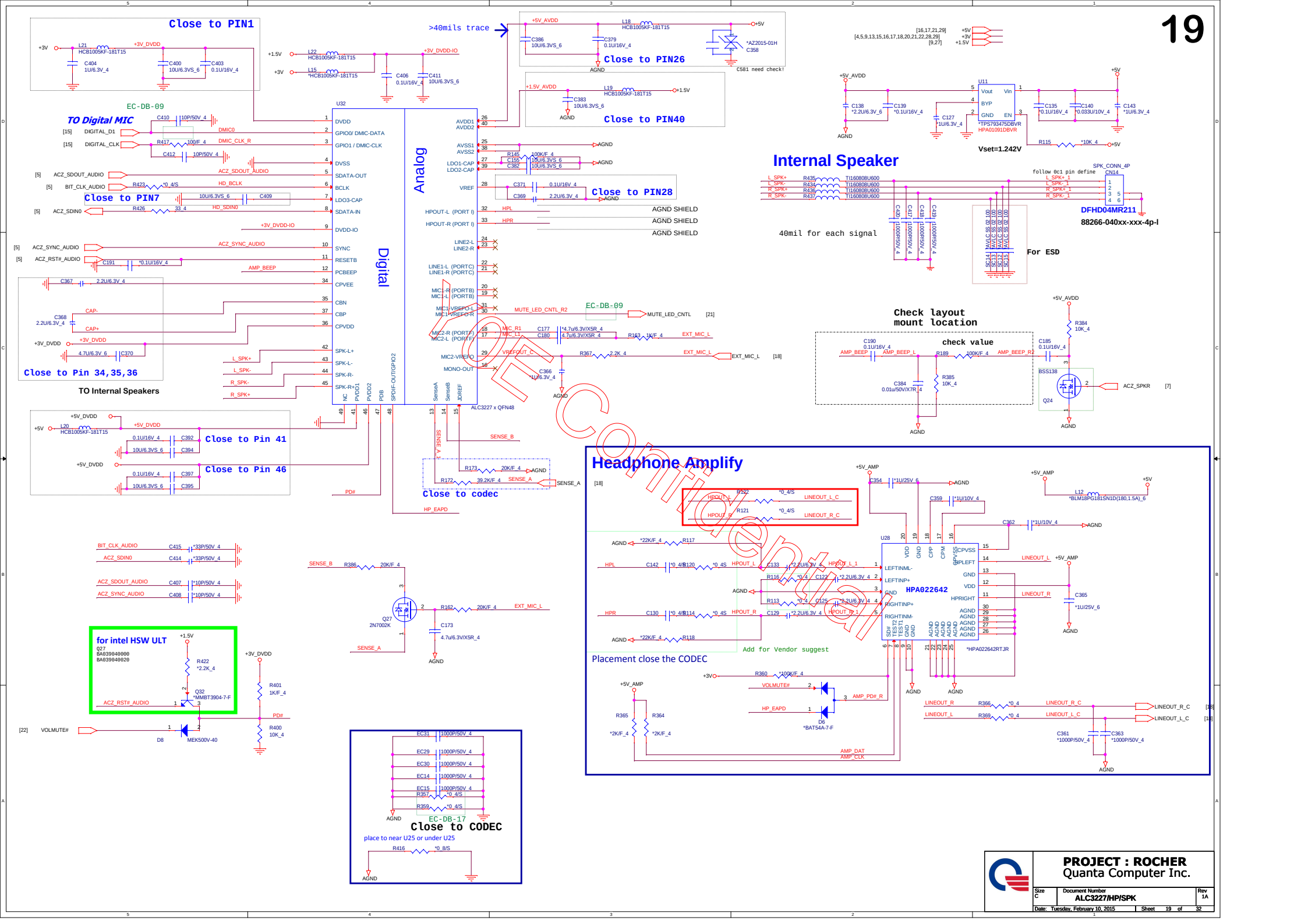


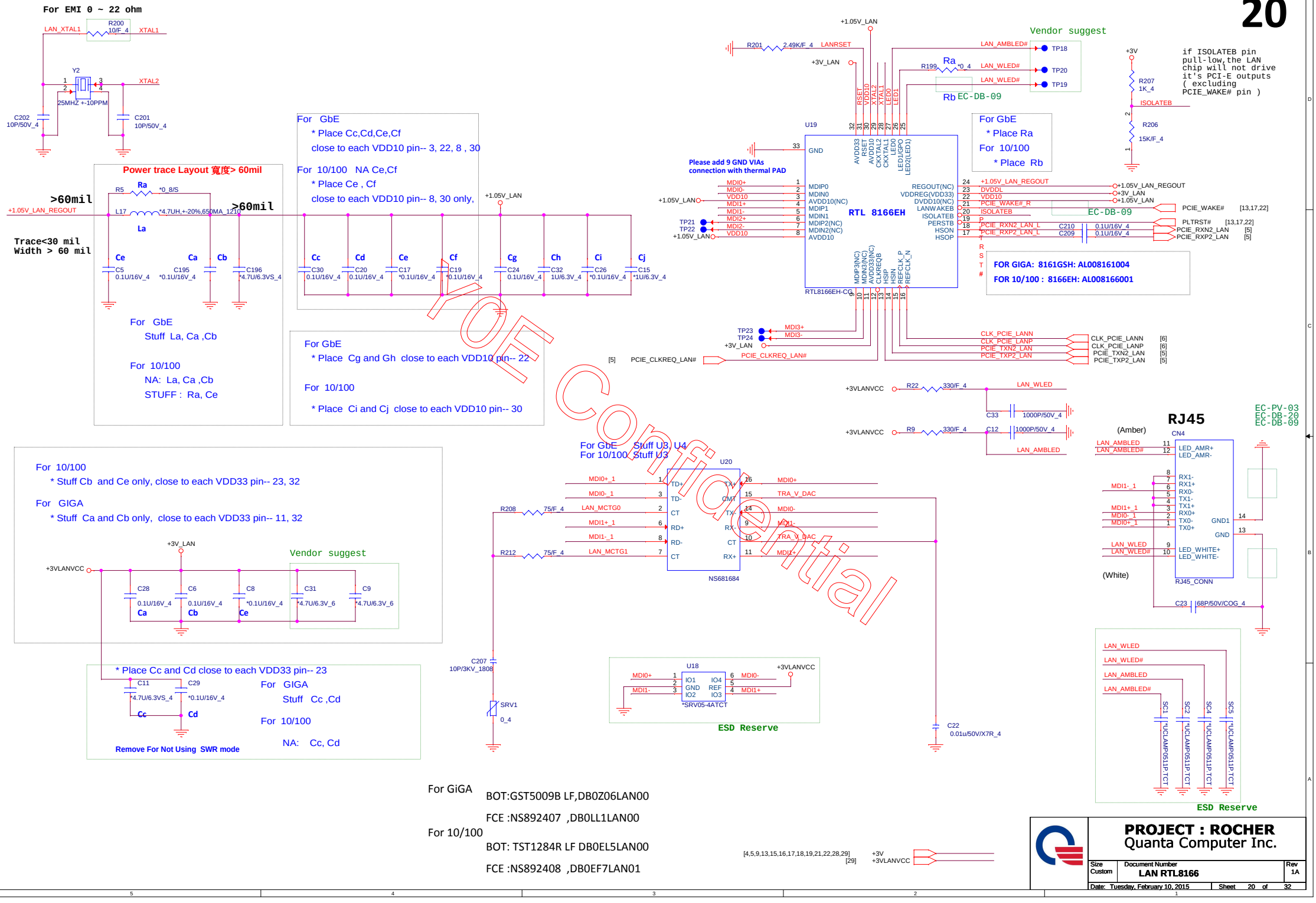


[4,5,9,13,15,16,17,19,20,21,22,28,29] PP3300_DX
[2,9,11,13,15,17,22,24,25,27,28,29] PP3300_DSW
[6,17,21,22,23,24,27] +3VPCU
[15,23,24,25,26,28,29,30] VIN
[9,21,24,25,27,28,29] PP5000
[6,17,21,22,23,24,27] PP3300_RTC

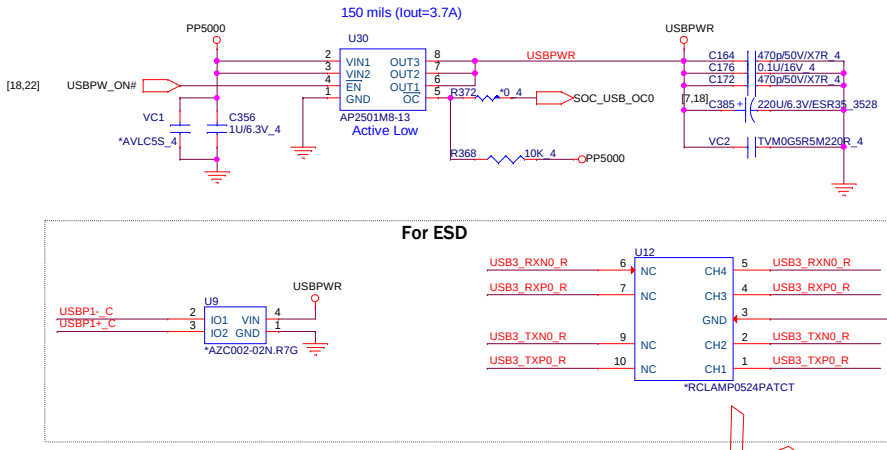
PROJECT : ROCHER
Quanta Computer Inc.

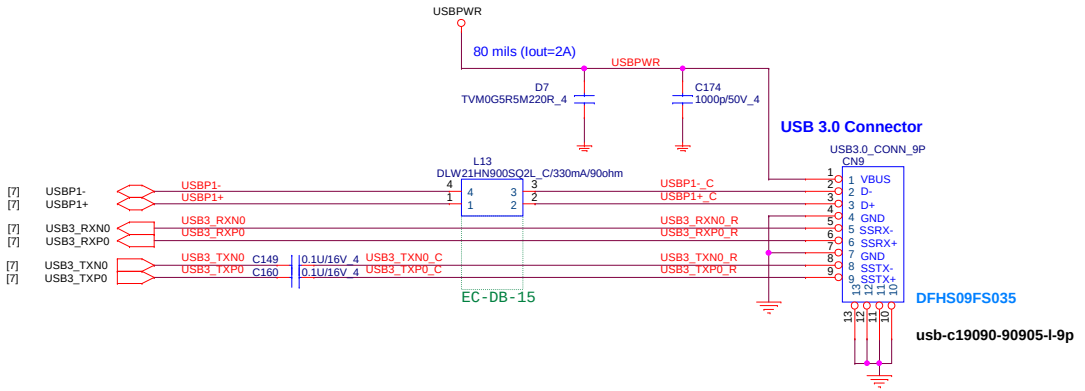
Size	Document Number	Rev
Custom	DB CN /Thermal sensor/Hole	1A
Date: Tuesday, February 10, 2015	Sheet 18 of 32	


Close to PIN1
>40mils trace
Close to PIN26
Close to PIN40
Close to PIN7
Close to PIN28
EC-DB-09
TO Digital MIC
Analog
Digital
U32
ALC3227 x QFN48
AGND SHIELD
Close to Pin 34,35,36
TO Internal Speakers
Close to Pin 41
Close to Pin 46
Close to codec
Internal Speaker
DFHD04MR211
88266-040xx-xxx-4p-l
40mil for each signal
For ESD
Vset=1.242V
Check layout
mount location
check value
Headphone Amplify
HPA022642
Add for Vendor suggest
Placement close the CODEC
for intel HSW ULT
Close to CODEC
place to near U25 or under U25
EC-DB-17
Quanta Confidential
PROJECT : ROCHER
Quanta Computer Inc.
ALC3227/HP/SPK
Tuesday, February 10, 2015



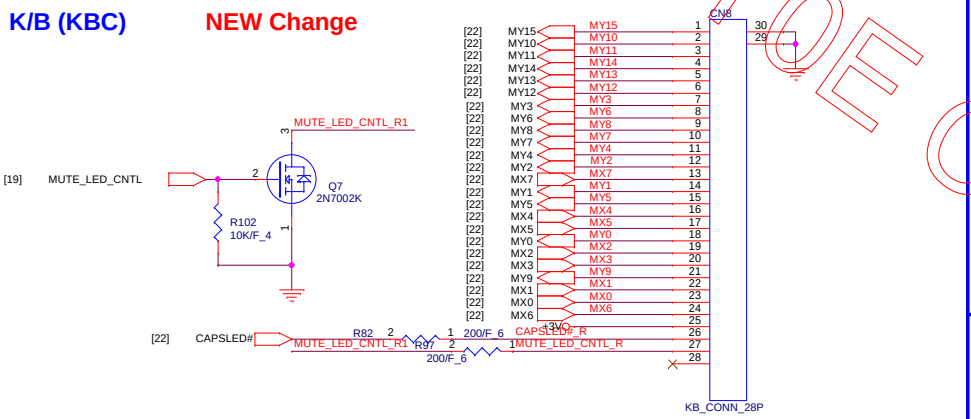
USB3.0

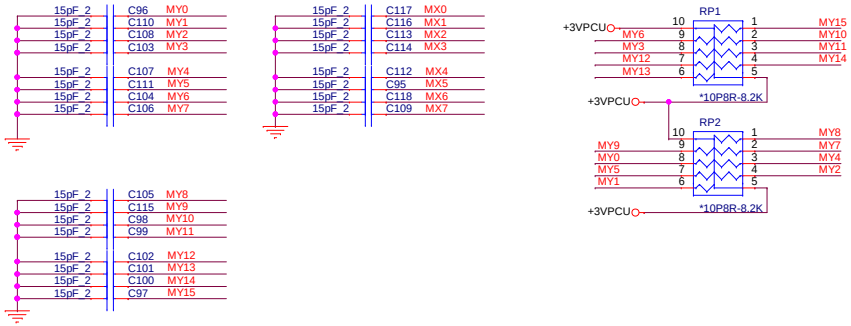




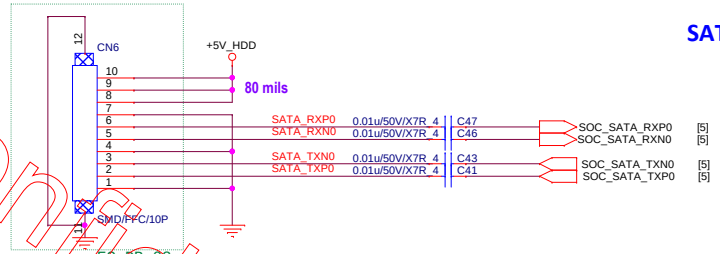
K/B (KBC)

NEW Change

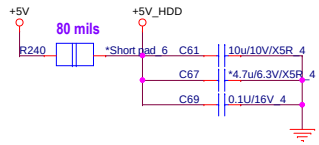




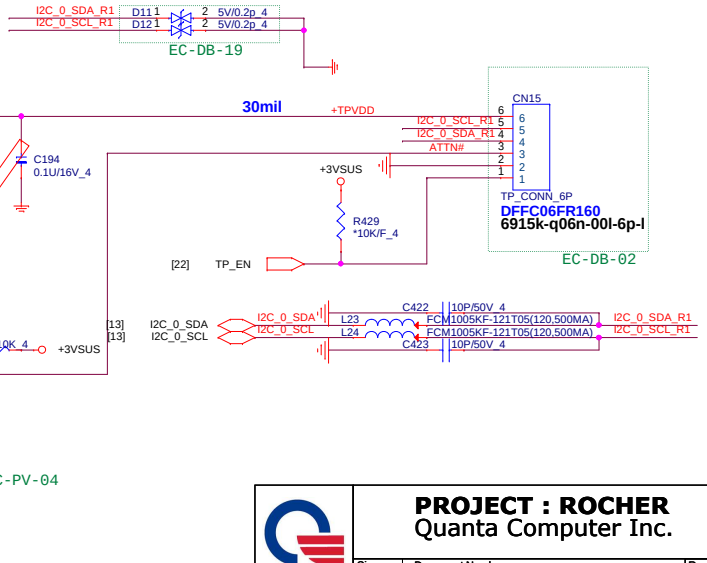
SATA HDD Connector



SATA Power



Track PAD BOARD CONN (TPD)



PROJECT : ROCHER Quanta Computer Inc.		
Size: Custom	Document Number: USB3/HDD/KB/TP	Rev: 1A
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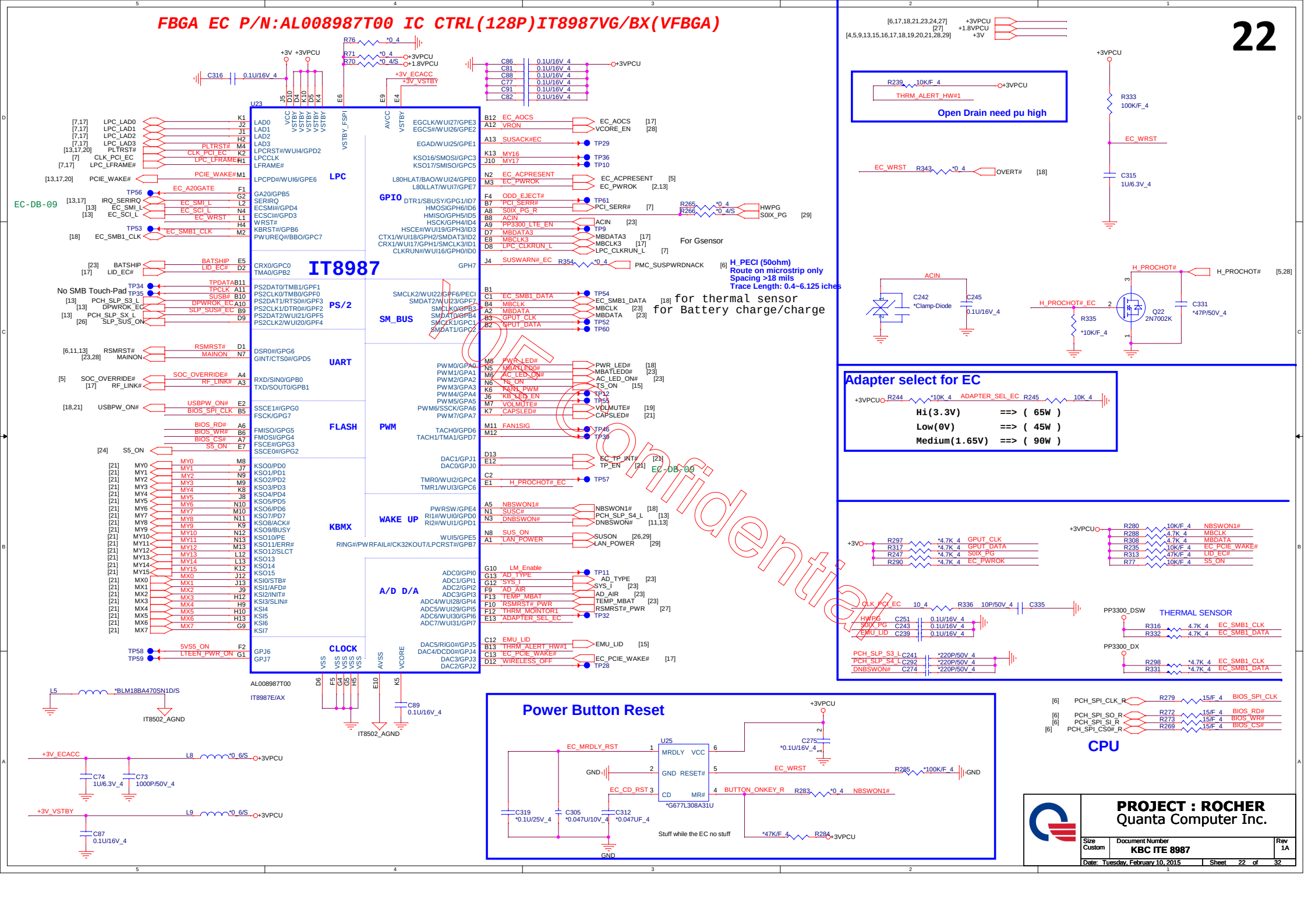
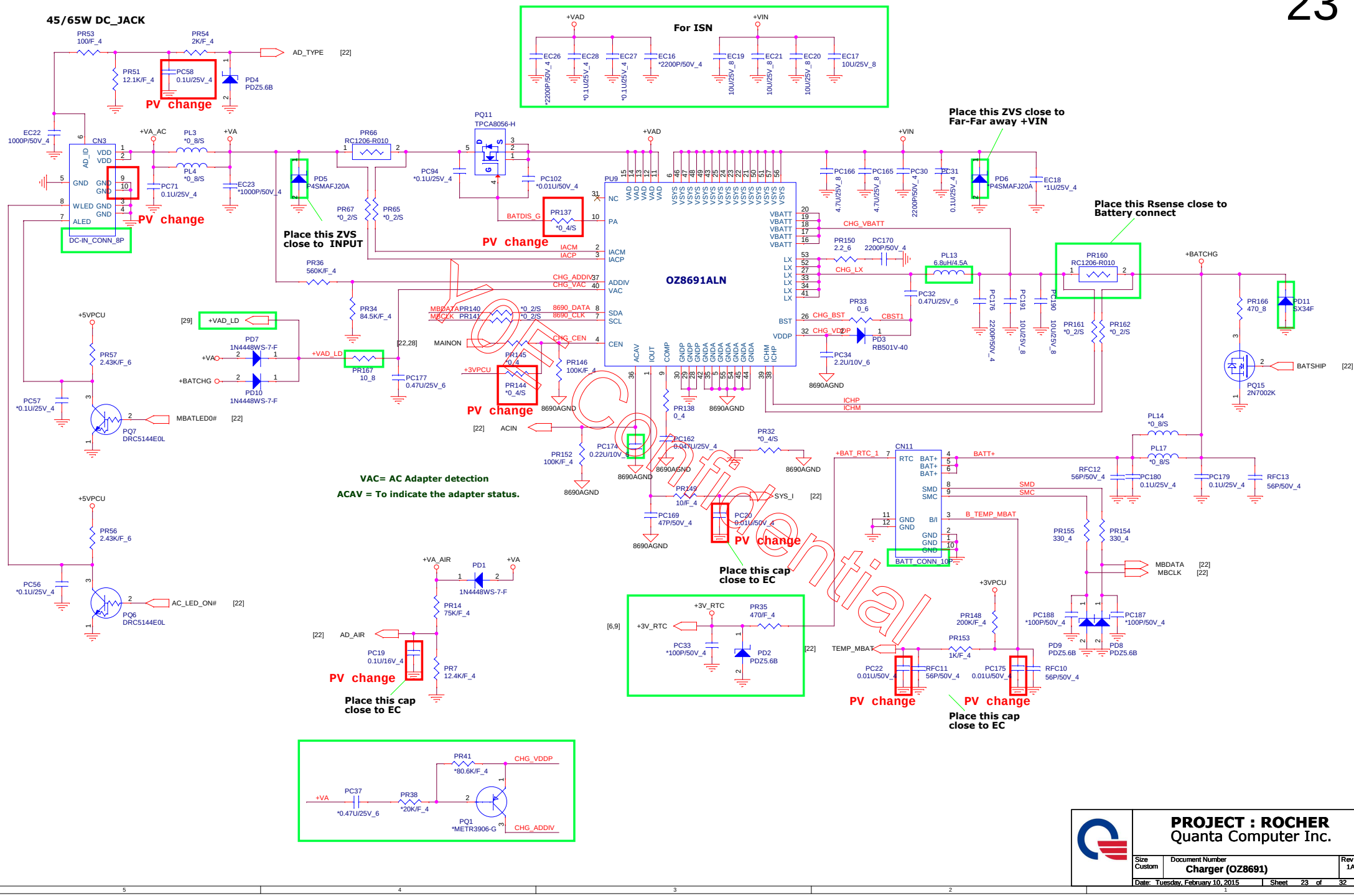
FBGA EC P/N:AL008987T00 IC CTRL(128P)IT8987VG/BX(VFBGA)

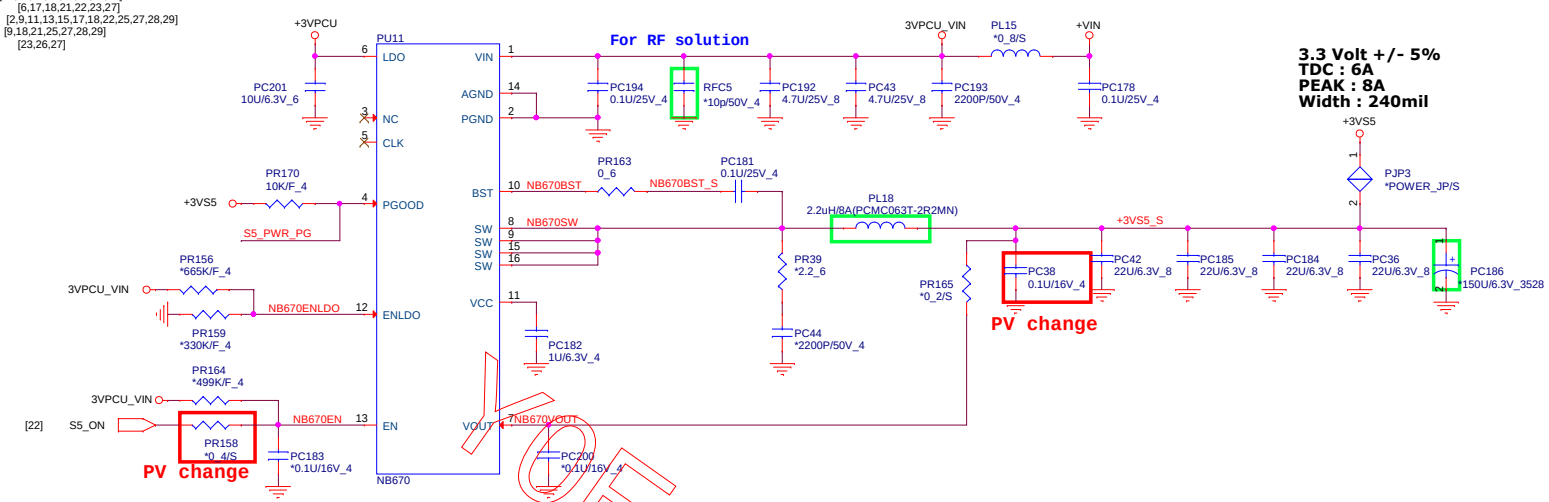


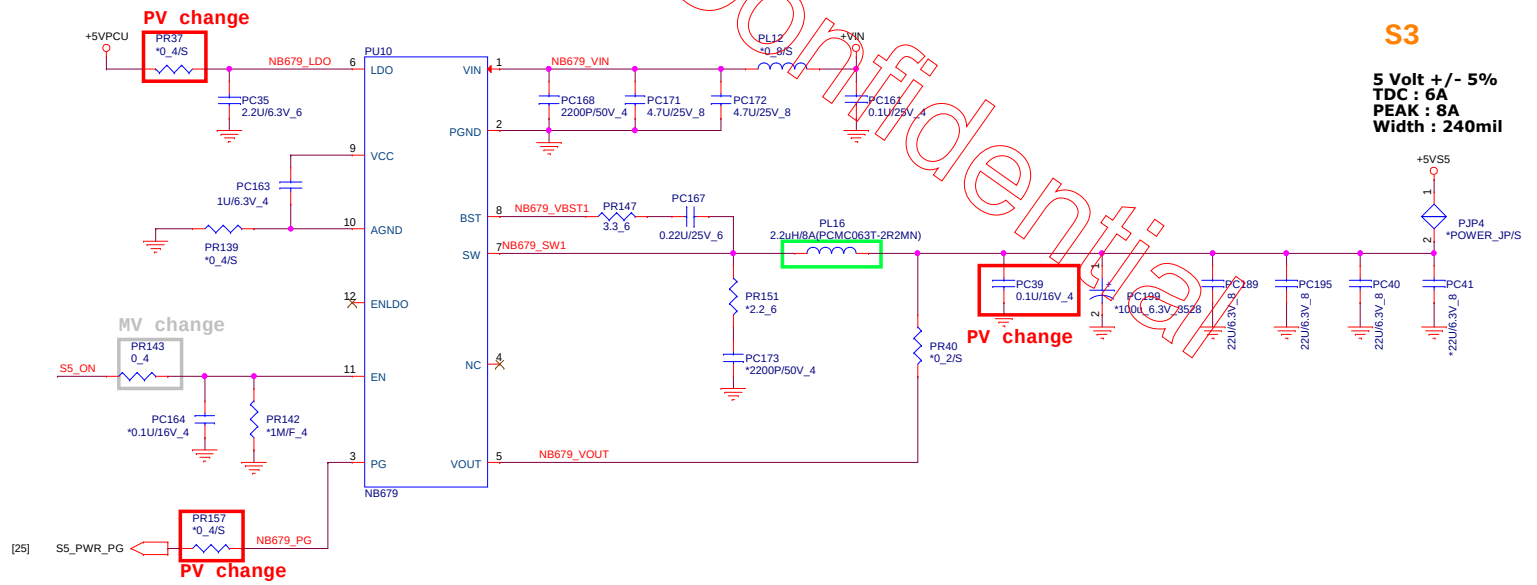
PROJECT : ROCHER	Quanta Computer Inc.
Size: Custom	Document Number: KBC ITE 8987
Rev: 1A	
Date: Tuesday, February 10, 2015	Sheet 22 of 32


45/65W DC_JACK
For ISN
PV change
Place this ZVS close to Far-Far away +VIN
Place this ZVS close to INPUT
Place this Rsense close to Battery connect
OZ8691ALN
VAC= AC Adapter detection
ACAV = To indicate the adapter status.
Place this cap close to EC
Quanta Confidential
PROJECT : ROCHER
Quanta Computer Inc.
Charger (OZ8691)
Tuesday, February 10, 2015

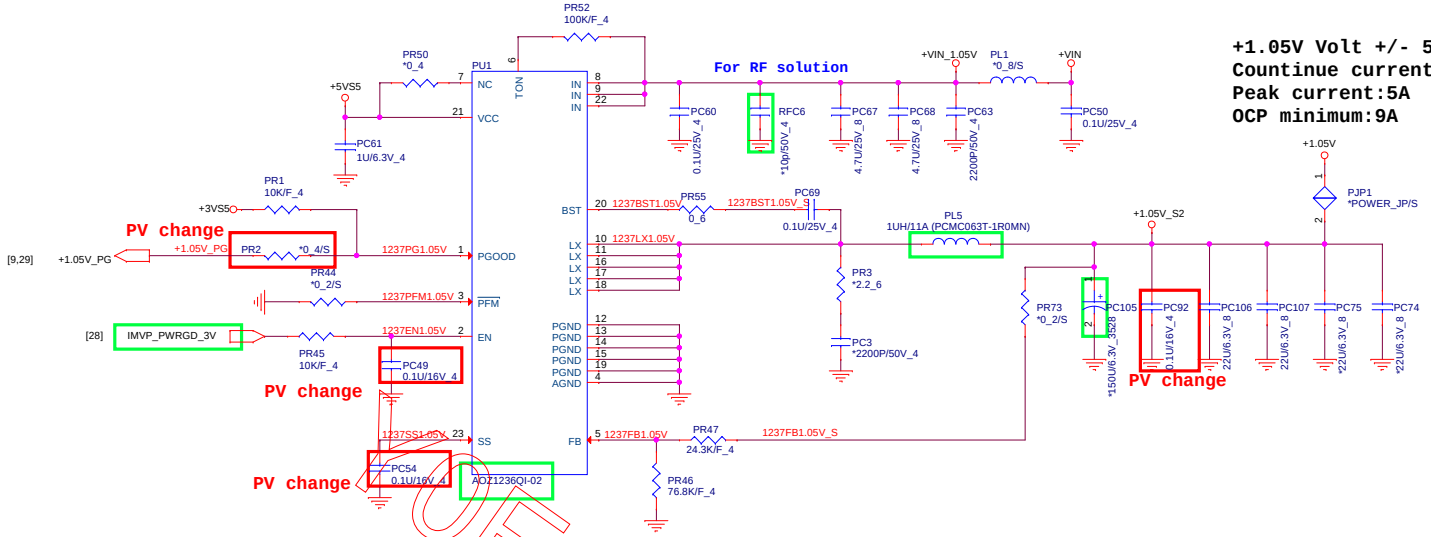
DC/DC +3VS5/+5VS5

+VIN [15,18,23,25,26,28,29,30]
+3VPCU [6,17,18,21,22,23,27]
+3VS5 [2,9,11,13,15,17,18,22,25,27,28,29]
+5VS5 [9,18,21,25,27,28,29]
+5VPCU [23,26,27]

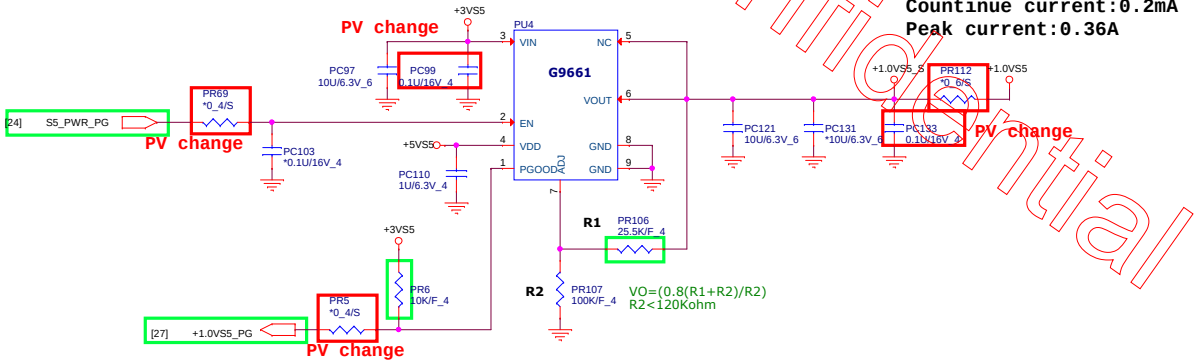




PROJECT : ROCHER Quanta Computer Inc.		
Size: Custom	Document Number: 3V/5V (NB670/NB669)	Rev: 1A
Date: Tuesday, February 10, 2015	Sheet 24 of 32	



+1.05V Volt +/- 5%
Countinue current:3.75A
Peak current:5A
OCP minimum:9A



+1.0VS5 Volt +/- 5%
Countinue current:0.2mA
Peak current:0.36A

+VIN	[15,18,23,24,26,28,29,30]
+3VS5	[2,9,11,13,15,17,18,22,24,27,28,29]
+5VS5	[9,18,21,24,27,28,29]
+1.0VS5	[9,11]
+1.05V	[5,6,9,28]

PROJECT : ROCHER
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V/+1.5V (SY8002)	1A
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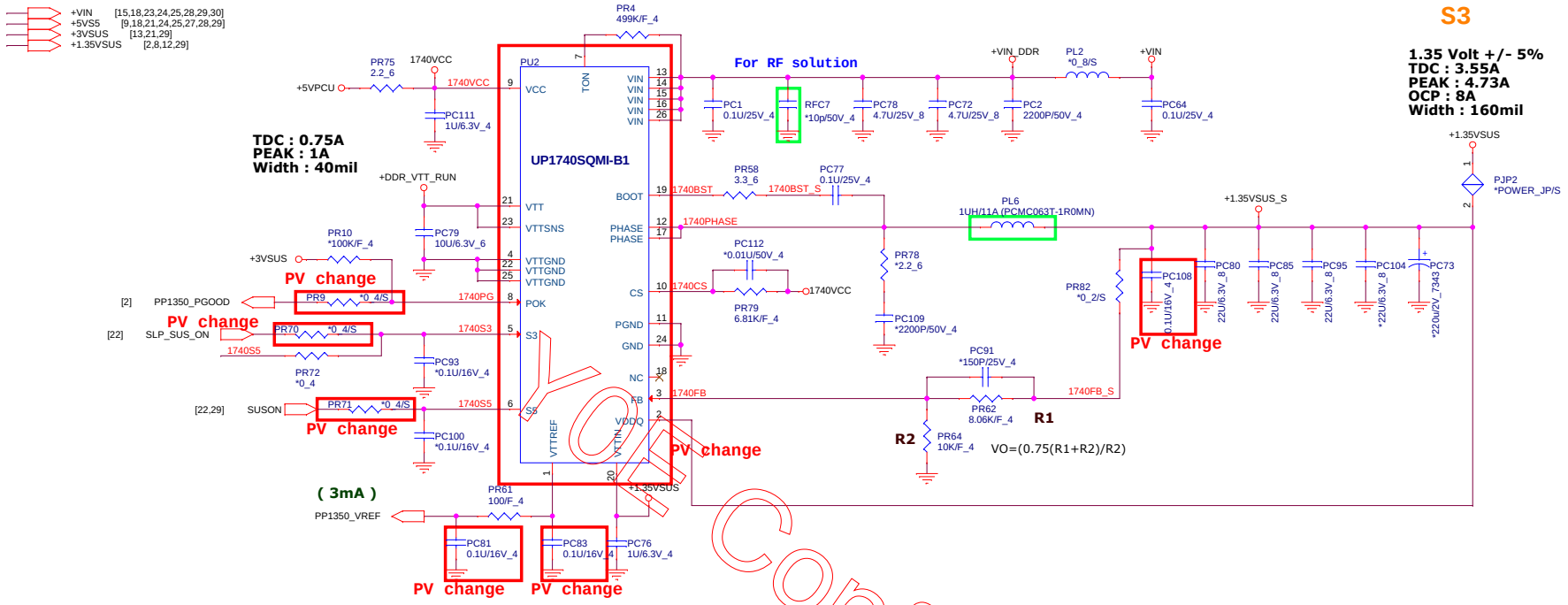

	S3	S5	+1.35VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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Size	Document Number	Rev
Custom	DDR 1.35V(UP1740S)	1A

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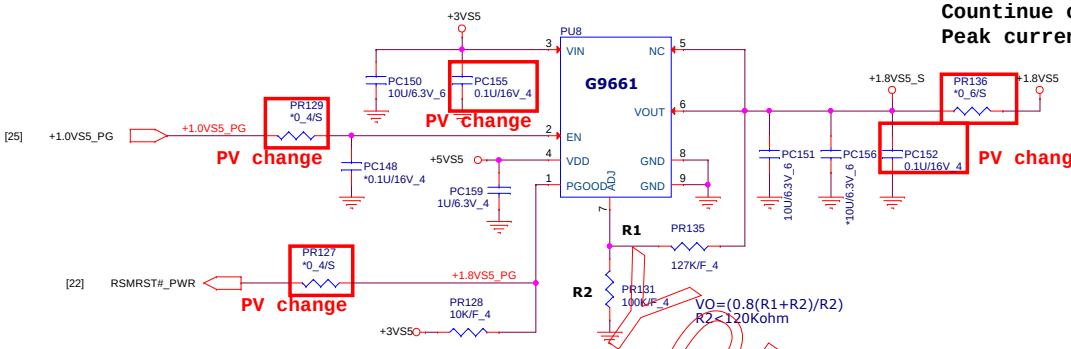
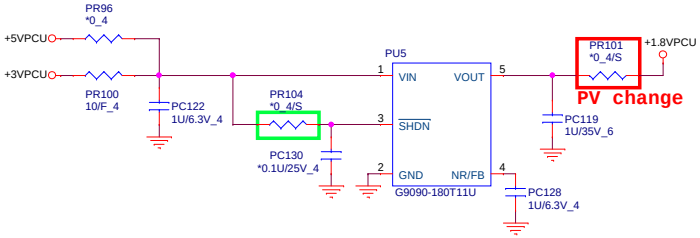
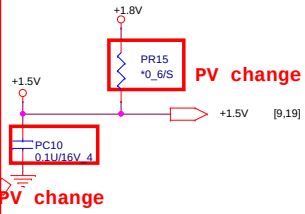
+1.8VS5 [6,7,9,11,13,17,29]
+5VS5 [9,18,21,24,25,28,29]
+3VS5 [2,9,11,13,15,17,18,22,24,25,28,29]
+3VPCU [6,17,18,21,22,23,24]
+5VPCU [23,24,26]
+1.8VPCU [22]

+1.8VS5 Volt +/- 5%
Countinue current:0.105mA
Peak current:0.3A





+1.5V +/- 5%
Countinue current:0.3A
Peak current:0.75A
OCP current:1.2A



Delete PU7

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Size	Document Number	Rev
Custom	1.0VS5/1.8VS5/1.24VS5	1A

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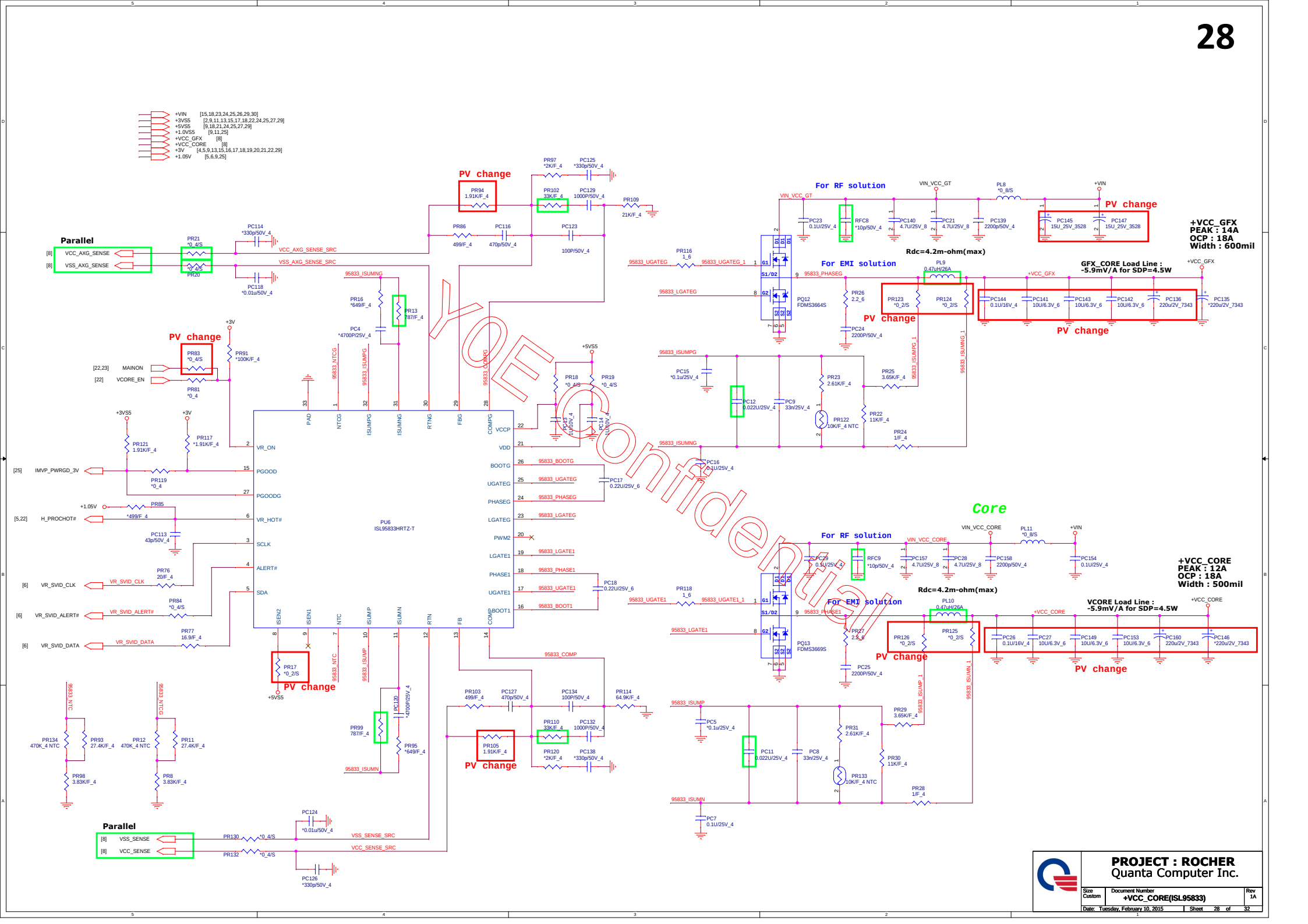

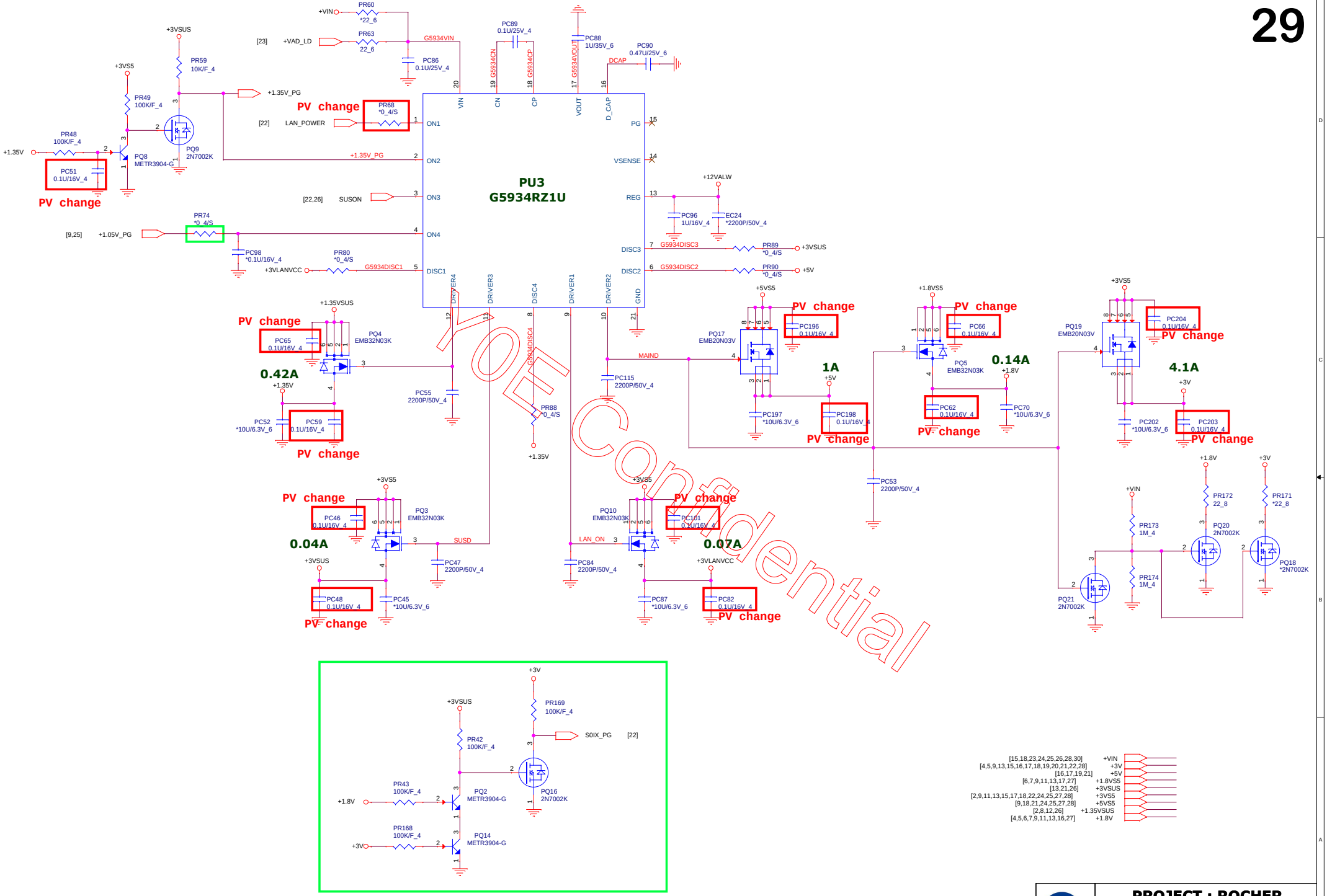

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Size	Document Number	Rev
Custom	Dis-charge IC (G5934RZ1U)	1A
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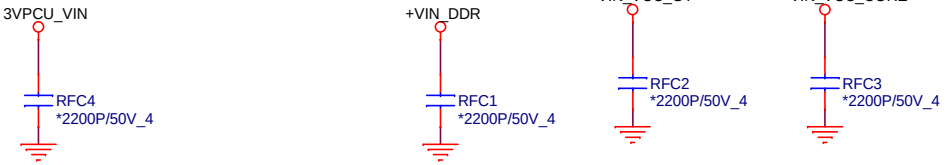
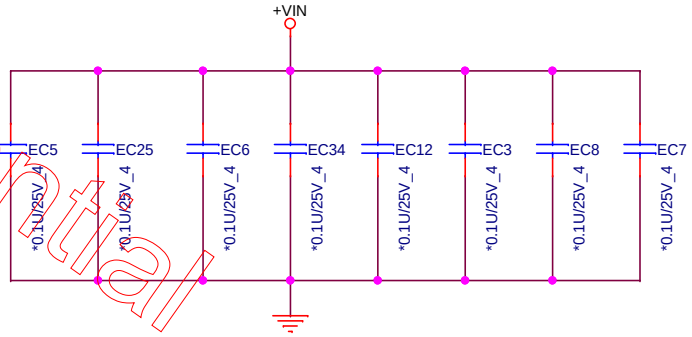


VIN_VCC_CORE → VIN_VCC_CORE [28]

VIN_VCC_GT → VIN_VCC_GT [28]

TOP

BOTTOM



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Size	Document Number	Rev
Custom	EMI/RF	1A
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Y0E Schematic EC Tracking Record A to C version(DB/PV Planar)

EC #	Page	Description	Part Affected
EC-DB-01	2,12	Reserve M_A_ODT1/M_A_CS#1/M_A_CKE1 signals and R442~R448 for DDP memory.	R442~R448
EC-DB-02	21	Change footprint and material of CN15 for SMT issue.	CN15
EC-DB-03	21	Change footprint and material of CN6 for ME change.	CN6
EC-DB-04	17	Change footprint and material of CN5 for ME change.	CN5
EC-DB-05	23~29	Change PR137,PR144,PR37,PR143,PR157,PR158,PR2,PR5,PR69,PR112,PR9,PR70,PR71, PR101,PR127,PR129,PR136,PR83, and PR68 from 0 ohm to short pad for power update.	PR137,PR144,PR37,PR143,PR157,PR158,PR2,PR5,PR69,PR112,PR9, PR70,PR71,PR101,PR127,PR129,PR136,PR83, and PR68
EC-DB-06	26	Change pin defined and footprint of PU2 for power update.	PU2
EC-DB-07	23~29	Change footprint of PR17,PR123,PR124,PR125, and PR126 for power update.	PR17,PR123,PR124,PR125, and PR126
EC-DB-08	28	Un-staff PC146 and staff PC160 for power update.	PC146 and PC160
EC-DB-09	2,5,6,7, 11,13, 15~22	Remove R143,R146,R223,R64,R151,R156,R158,R166,R129,R171,R375,R39,R394,R182,R185, R180,R412,R410,R312,R21,R90,R66,R315,R421,R373,R204,R432,R334,R243,R45,R33,R202, R197,R17,R20,R42,R56,R198,R1,R330, and R23 for test point coverage.	R143,R146,R223,R64,R151,R156,R158,R166,R129,R171,R375,R39,R394, R182,R185,R180,R412,R410,R312,R21,R90,R66,R315,R421,R373,R204, R432,R334,R243,R45,R33,R202,R197,R17,R20,R42,R56,R198,R1, and R23
EC-DB-10	9	Add +1.35V LDO (U35) and reserve L25 and C429 for CRT ripple issue.	U35,C427,R449,C426,C428,C425,R450,R451,C68,L25, and C429
EC-DB-11	13	Change connection of Q23.2 from PP1800_PCH to PP1800_PCH_S5 for WOL issue.	Q23
EC-DB-12	23	Pin9 and Pin10 of CN3 connect to GND for ESD suggestion.	CN3
EC-DB-13	27	Remove PU7, PR111, PR113, PC137, PR87, PC117, PR108, PR115, PL7, PR92, and PC6 for layout space.	PU7, PR111, PR113, PC137, PR87, PC117, PR108, PR115, PL7, PR92, and PC6
EC-DB-14	28	Staff PC145, PC147, PC135, PC27, PC149, and PC153 for power issue.	PC145, PC147, PC135, PC27, PC149, and PC153
EC-DB-15	6,21	Remove R293, R294, R119, R123, R133, and R142 for test point coverage.	R293, R294, R119, R123, R133, and R142
EC-DB-16	18	Un-staff R176 and R177, and staff L14 for EMI suggestion.	R176, R177, and L14
EC-DB-17	19	Change R357 and R359 from 0 ohm to short pad for cost saving.	R357 and R359
EC-DB-18	15	Change footprint and material of CN2 for ME change.	CN2
EC-DB-19	21	Staff D11 and D12 for ESD suggestion.	D11 and D12
EC-DB-20	20	Change footprint and material of CN4 for ME change.	CN4
EC-DB-21	28	Staff PC141,PC142,PC143,PC27,PC149, and PC153 for fixing overshoot issue.	PC141,PC142,PC143,PC27,PC149, and PC153
EC-DB-22	28	Change PR94 and PR105 from 1.78k ohm to 1.91k ohm for Vcore load line fine-tune.	PR94 and PR105

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Size	Document Number	Rev
Custom	DB to PV EC History	1A

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Y0E Schematic EC Tracking Record C to MP version(PV/MV Planar)

EC #	Page	Description	Part Affected
EC-PV-01	24	Reverse 0R (PR143) for fixing acoustic issue.	PR143
EC-PV-02	18	Remove R177 and R176 for SMT issue.	R177 and R176
EC-PV-03	20	Change footprint and LED connection of CN4 for LED location of HP requirement.	CN4
EC-PV-04	21	Add D13 and un-staff Q36 for Touch Pad leakage issue.	D13 and Q36
EC-PV-05	9,19, 20,22	Change C130,C142,R121,R122,R266,R449, and R5 from 0 ohm to short pad for cost saving.	C130,C142,R121,R122,R266,R449, and R5
EC-PV-06	18	Remove Hole 2 and Hole 11, and add PAD1~4 for ME requirement.	Hole 2, Hole 11, and PAD1~4
EC-PV-07	18	Add PAD5 for ESD requirement.	PAD5