JE40 HR
DIS/UMA/Muxless Schematics Document
Sandy Bridge
Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 1 of 102	

JE40 HR Block Diagram (Discrete/UMA/co-lay)

Project code : 91.4IQ01.001
PCB P/N : 48.4IQ01.0SA
Revision : 10267-1

##OnMainBoard

VRAM
2GB/1GB/512MB
88,89,90,91

DDR3
800MHz

Nvidia N12P
83.84,85,86,87

PCIe x 16
(Discrete only)

Intel CPU
Sandy Bridge
FSB: 1066 MHz
4,5,6,7,8,9,10,11,12,13

DDRIII 1066/1333 Channel A
DDRIII 1066/1333 Channel B

DDRIII Slot 0 1066/1333 14
DDRIII Slot 1 1066/1333 15

Discreet/UMA/PX Co-lay

FDIx4x2
(UMA only)

DMIx4

HDMI 51
LCD 49
CRT 50

HDMI
LVDS(Dual Channel)
RGB CRT

Level shifter 57

Intel
PCH
Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25,26

PCIE x 1
USB x 2
USB3.0
uPD720200
75

PCIE x 1
USB x 1
Mini-Card
802.11a/b/g
65

PCIE x 1
1000 NIC
BCM57780A1
31

RJ45 CONN 59

SD/MMC+/MS/
MS Pro/xD

PCIE x 1,USB x 1
Mini-Card
WWAN 66

SIM 66

USB 2.0 x 1
Right Side:
USB x 1

Left Side:
USB x 1

Bluetooth 63

CAMERA 49

64

USB2.0 x 4

AZALIA

Azalia
CODEC
ALC271X
29

Internal Analog MIC
HP1
MIC IN
2CH SPEAKER

SPI
Flash ROM
4MB 60

LPC Bus
LPC debug port
71

SATA x 2
HDD 56
ODD 56

KBC
NUVOTON
NPCE795P
27

SMBus

Touch PAD
Int. KB
Thermal
ENE P2800
ENE P2793
Fan 28

SYSTEM DC/DC APL5916KAI 48	
INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0

CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER

L1:Top L4:Signal
L2:VCC L5:GND
L3:Signal L6:Bottom

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Block Diagram
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 2 of 102

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 3 of 102

SSID = CPU

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

JE40 delete eDP function

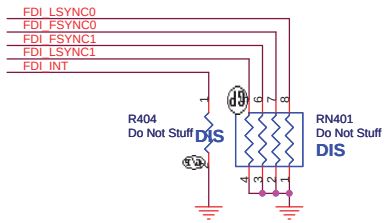
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

Stuff to disable internal graphics function for power saving.



HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/DMI/FDI)

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 4 of 102

SSID = CPU

CPU1B
SANDY

2 0F 9

SANDY

MISC
CLOCKS
THERMAL
DDR3 MISC
PWR MANAGEMENT
JTAG & BPM

18 H_SNB_IVB# C26 SNB_IVB#
JE40 modify AN34 SKTOCC#
JE40 modify AL33 CATERR#
22,27 H_PECI AN33 PECI
27,42 H_PROCHOT# 1 R513 56R2J-4-GP H_PROCHOT# R AL32 PROCHOT#
22,36 H_THERMTRIP# AN32 THERMTRIP#

19 H_PM_SYNC AM34 PM_SYNC
1 R503 2 10KR2J-4-GP
22,36,97 H_CPUPWRGD AP33 UNCOREPWRGOOD
19,37 PM_DRAM_PWRGD 1 R505 DX Do Not Stuff V8 SM_DRAMPWROK
37 VDDPWRGOOD
BUF_CPU_RST# AR33 RESET#

BCLK A28 CLK_EXP_P 20
BCLK# A27 CLK_EXP_N 20
DPLL_REF_SSCLK A16 CLK_DP_P_R
DPLL_REF_SSCLK# A15 CLK_DP_N_R
RN502 Do Not Stuff DIS
JE40 modify
1D05V_VTT

SM_DRAMRST# R8
1 R502 4K99R2F-L-GP
SM_DRAMRST# 37

SM_RCOMP0 AK1 SM_RCOMP_0 R506 140R2F-GP
SM_RCOMP1 A5 SM_RCOMP_1 R507 25D5R2F-GP
SM_RCOMP2 A4 SM_RCOMP_2 R508 200R2F-L-GP

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

PRDY# AP29
PREQ# AP27
JE40 modify
TCK AR26
TMS AR27
TRST# AP30 XDP_TRST#
TDI AR28
TDO AP26 XDP_TDO
DBR# AL35 XDP_DBRESET#
BPM#0 AT28
BPM#1 AR29
BPM#2 AR30
BPM#3 AT30
BPM#4 AP32
BPM#5 AR31
BPM#6 AT31
BPM#7 AR32
JE40 modify

1D05V_VTT
RN501 SRN51J-GP
XDP_TDO
XDP_TRST#

3D3V_S0
RN503 SRN1K5J-1-GP
XDP_DBRESET#
18,27,31,36,65,66,71,82,97 PLT_RST# BUF_CPU_RST#

1D05V_VTT
1 R501 62R2J-GP H_PROCHOT#
C502 SC47P50V2JN-3GP

CRB : 47pf
CEKLT:43pf
Connect EC to PROCHOT# through inverting OD buffer.

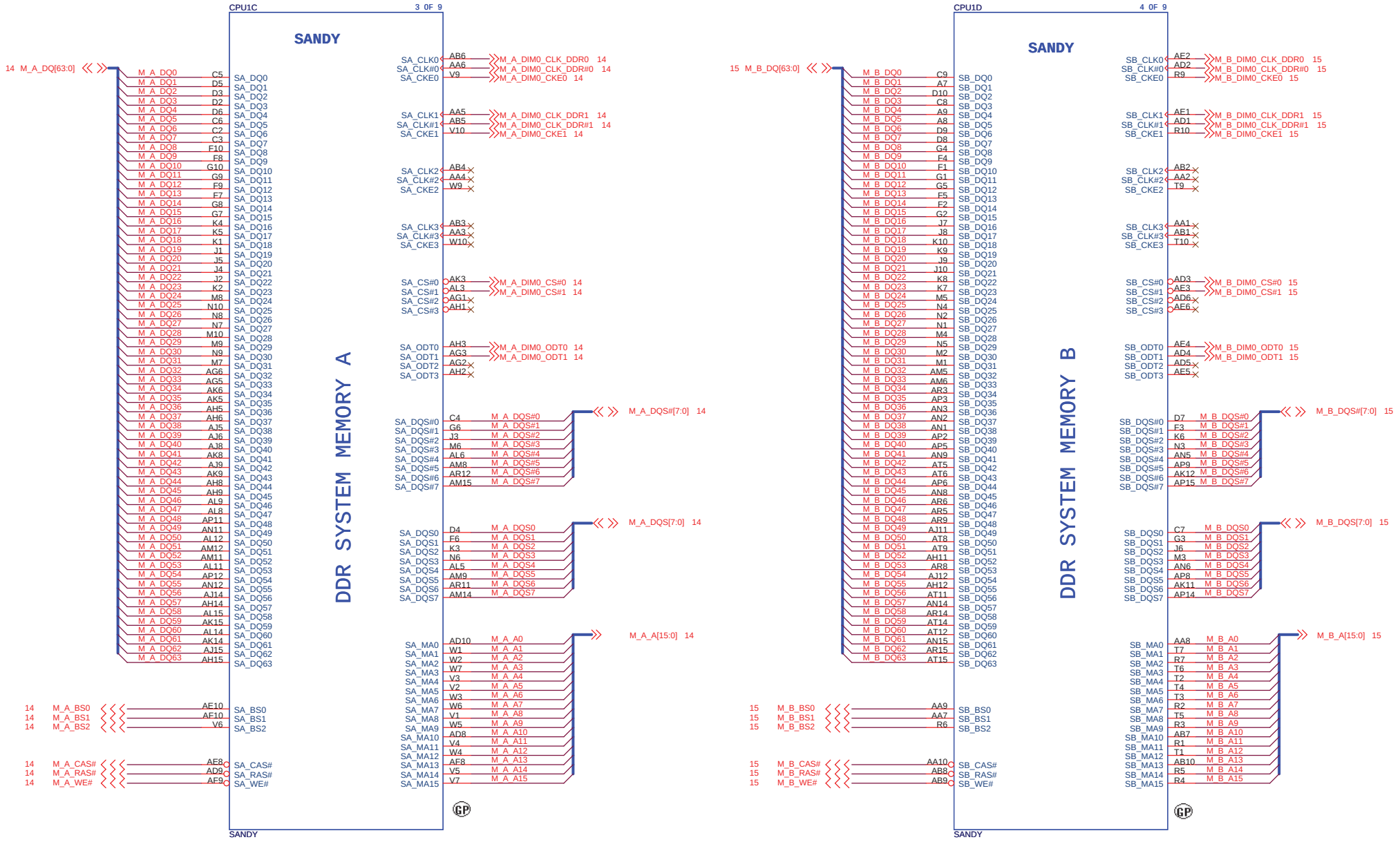
```
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through
1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP
through 1K +/- 5% resistorpower (~15 mW) may be
wasted.
```

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU (THERMAL/CLOCK/PM)		
Size: Custom	Document Number: JE40-HR		Rev: -1
Date: Thursday, December 02, 2010	Sheet 5 of 102		

SSID = CPU



HR UMA

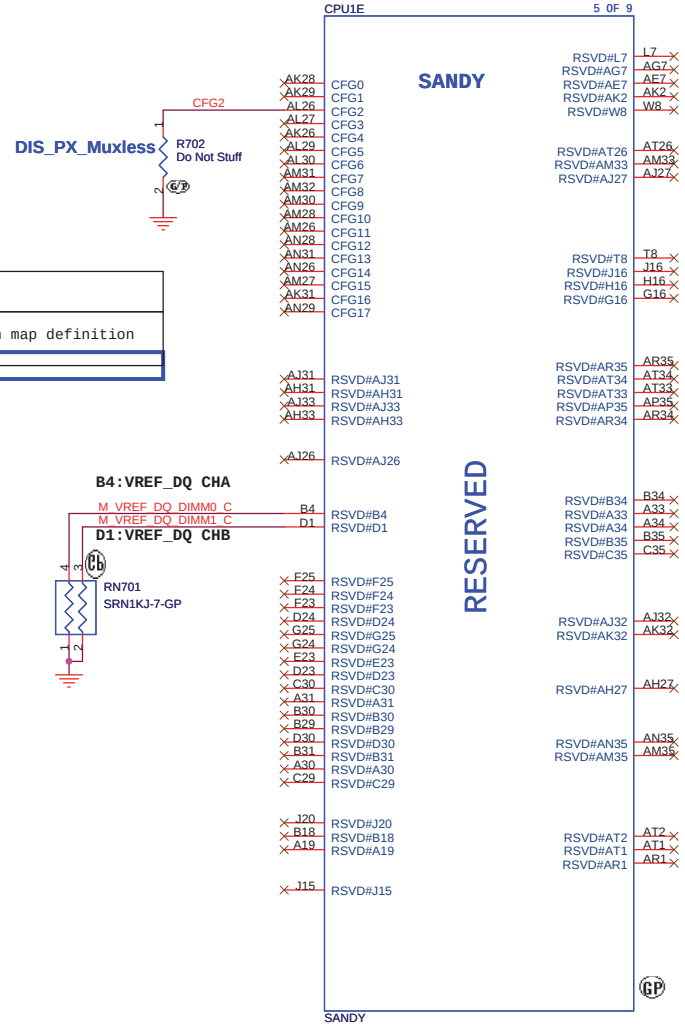
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (DDR)

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 6 of 102

SSID = CPU



PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0:Lane Reversed

HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU (RESERVED)
Size A3 / Document Number	JE40-HR / Rev -1
Date: Thursday, December 02, 2010	Sheet 7 of 102

SSID = CPU

POWER

CPU1F — 6 OF 9 — SANDY

PROCESSOR CORE POWER

53A

VCC_CORE

C801 Do Not Stuff, C802 Do Not Stuff, C803 Do Not Stuff, C804 Do Not Stuff, C811 Do Not Stuff
C820 Do Not Stuff, C819 Do Not Stuff, C818 Do Not Stuff, C817 Do Not Stuff, C815 Do Not Stuff
C816, C821 Do Not Stuff, C822, C823, C824, C825, C826, C827 — SC10U6D3V5KX-1GP
C837, C836, C835, C834, C833, C832 Do Not Stuff, C831 Do Not Stuff, C828 — SC10U6D3V5KX-1GP

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCC_CORE

VCC: AG35, AG34, AG33, AG32, AG31, AG30, AG29, AG28, AG27, AG26, AF35, AF34, AF33, AF32, AF31, AF30, AF29, AF28, AF27, AF26, AD35, AD34, AD33, AD32, AD31, AD30, AD29, AD28, AD27, AD26, AC35, AC34, AC33, AC32, AC31, AC30, AC29, AC28, AC27, AC26, AA35, AA34, AA33, AA32, AA31, AA30, AA29, AA28, AA27, AA26, Y35, Y34, Y33, Y32, Y31, Y30, Y29, Y28, Y27, Y26, V35, V34, V33, V32, V31, V30, V29, V28, V27, V26, U35, U34, U33, U32, U31, U30, U29, U28, U27, U26, R35, R34, R33, R32, R31, R30, R29, R28, R27, R26, P35, P34, P33, P32, P31, P30, P29, P28, P27, P26

SANDY

CORE SUPPLY

PEG AND DDR

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

VCCIO: AH13, AH10, AG10, AC10, Y10, U10, P10, L10, J14, J13, J12, J11, H14, H12, H11, G14, G13, G12, F14, F13, F12, F11, F14, F12, E11, D14, D13, D12, D11, C14, C13, C12, C11, B14, B12, A14, A13, A12, A11, J23

1D05V_VTT

C805, C806, C807, C809, C810, C838, C839, C840, C841 — SC10U6D3V5KX-1GP

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

1D05V_VTT

C812, C813, C814, C829, C830, C842 Do Not Stuff, C843 Do Not Stuff, C844, C845 — SC10U6D3V5KX-1GP

SVID

VIDALERT# AJ29 — H_CPU_SVIDALRT# — R803 43R2J-GP — VR_SVID_ALERT# 42
VIDSCLK AJ30 — H_CPU_SVIDCLK 42
VIDSOUT AJ28 — H_CPU_SVIDDAT 42

For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V_VTT
H_CPU_SVIDDAT — R804 — 130R2F-1-GP

SENSE LINES

VCC_CORE

R801,R802 close to CPU

R801 100R2F-L1-GP-U
R802 100R2F-L1-GP-U

VCC_SENSE AJ35 — VCCSENSE 42
VSS_SENSE AJ34 — VSSSENSE 42
VCCIO_SENSE B10 — VCCIO_SENSE 45
VSSIO_SENSE A10 — VSSIO_SENSE 45

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)
Size: Custom | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 8 of 102

SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU

POWER

CPU1G — 7 OF 9 — SANDY

VCC_GFXCORE

PROCESSOR VAXG: 24A

C901 Do Not Stuff DY UMA_PX_Muxless
C902 SC10U6D3V5KX-1GP
C903 SC10U6D3V5KX-1GP
C904 SC10U6D3V5KX-1GP
C905 SC10U6D3V5KX-1GP
C906 Do Not Stuff DY UMA_PX_Muxless
C907 Do Not Stuff DY UMA_PX_Muxless
C908 SC10U6D3V5KX-1GP
C918 Do Not Stuff DY UMA_PX_Muxless
C919 SC10U6D3V5KX-1GP
C920 SC10U6D3V5KX-1GP
C921 SC10U6D3V5KX-1GP DY UMA_PX_Muxless

VAXG: AT24 AT23 AT21 AT20 AT18 AT17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17

VCC_GFXCORE

R903 Do Not Stuff DIS
R904 Do Not Stuff DIS
R905 Do Not Stuff DIS
R901 Do Not Stuff DIS

Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

SENSE LINES

VAXG_SENSE AK35
VSSAXG_SENSE AK34
VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF AL1 → +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

DDR3 -1.5V RAILS

1D5V_S0

PROCESSOR VDDQ: 10A

VDDQ: AE7 AE4 AE1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 Do Not Stuff DY
C910 SC10U6D3V5KX-1GP
C911 SC10U6D3V5KX-1GP
C912 SC10U6D3V5KX-1GP
C913 SC10U6D3V5KX-1GP
C914 Do Not Stuff DY

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

VCCSA: M27 M26 L26 J26 J25 J24 H26 H25

C916 Do Not Stuff DY
C915 SC10U6D3V5KX-1GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

0D85V_S0
R902 10R2J-2-GP
R902 need be close to pin H23.
VCCSA_SENSE H23 → VCCUSA_SENSE
TP901 Do Not Stuff

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

VCCPLL: B6 A6 A2

C922 SC1U10V2KX-1GP

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

MISC

FC_C22 C22
VCCSA_VID1 C24
H_FC_C22
VCCSA_SEL 48

RN901 SRN1KJ-7-GP

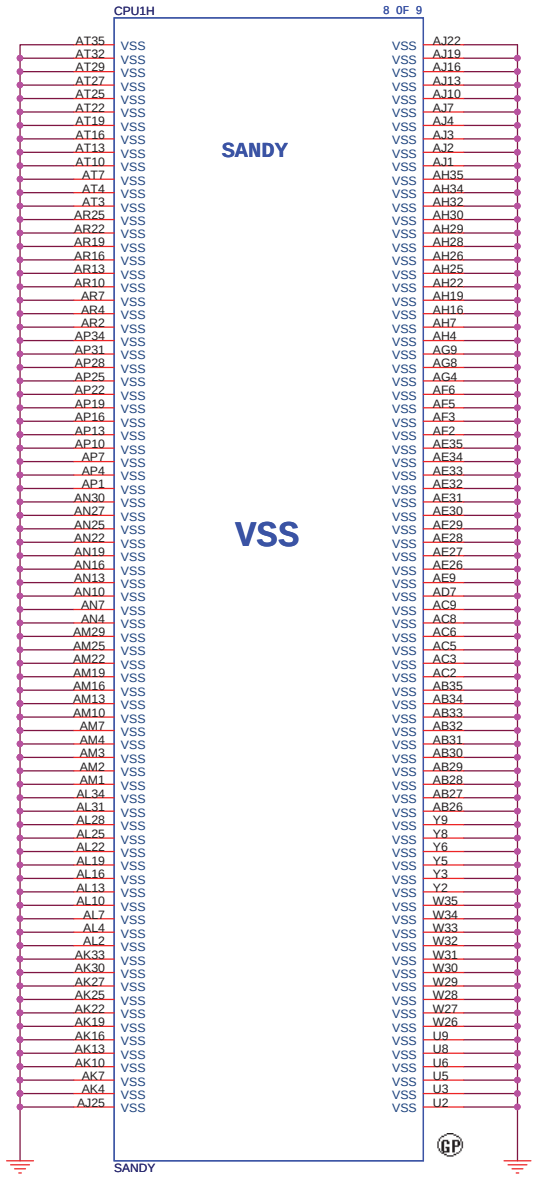
SANDY

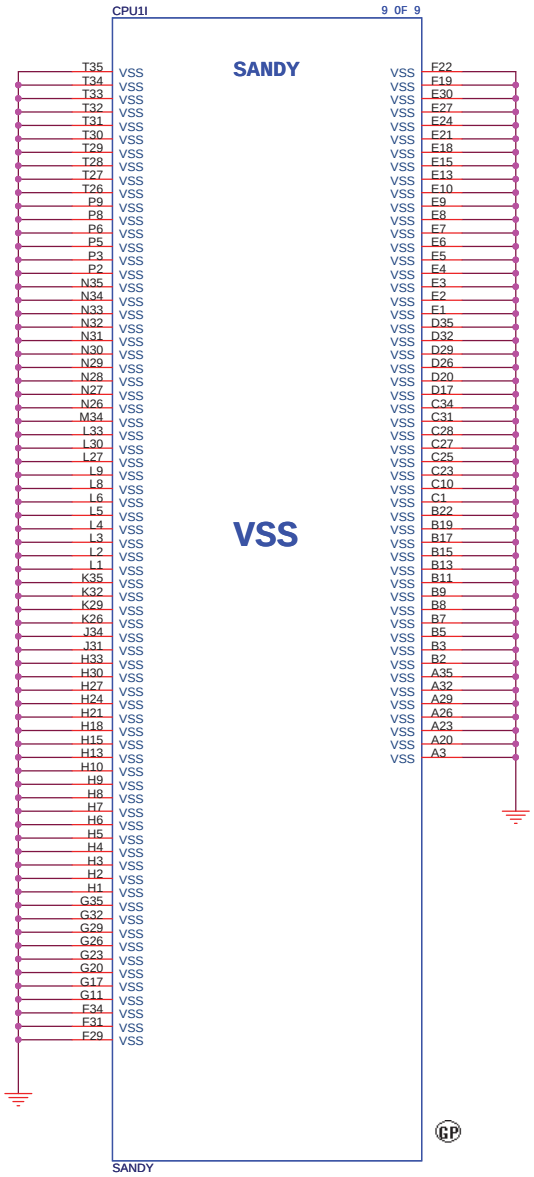
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 9 of 102

SSID = CPU





HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (VSS)*		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 10 of 102	

JE40 delete XDP function

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 11 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 12 of 102

(Blanking)

HR UMA

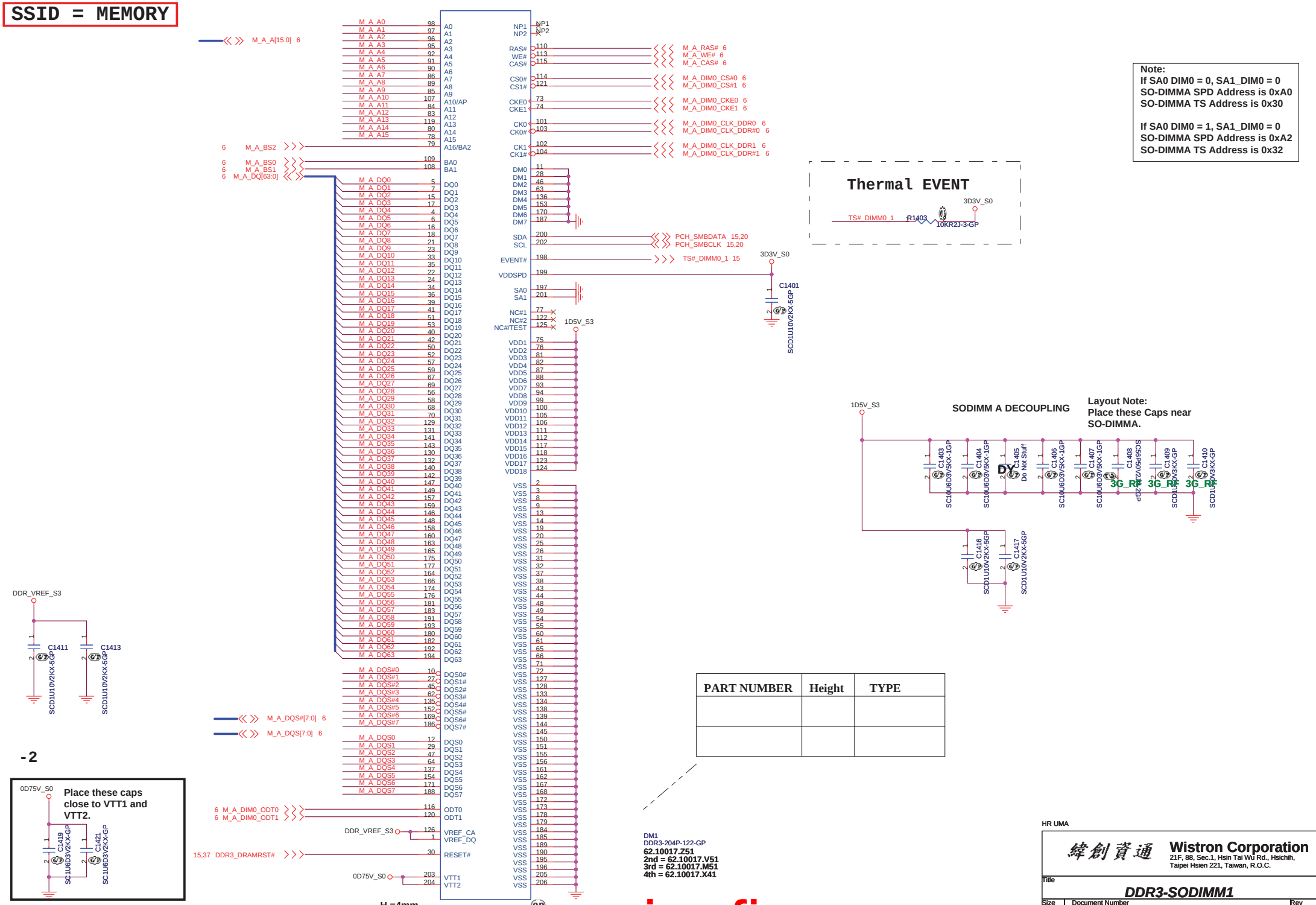
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 13 of 102

SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

PART NUMBER	Height	TYPE

HR UMA

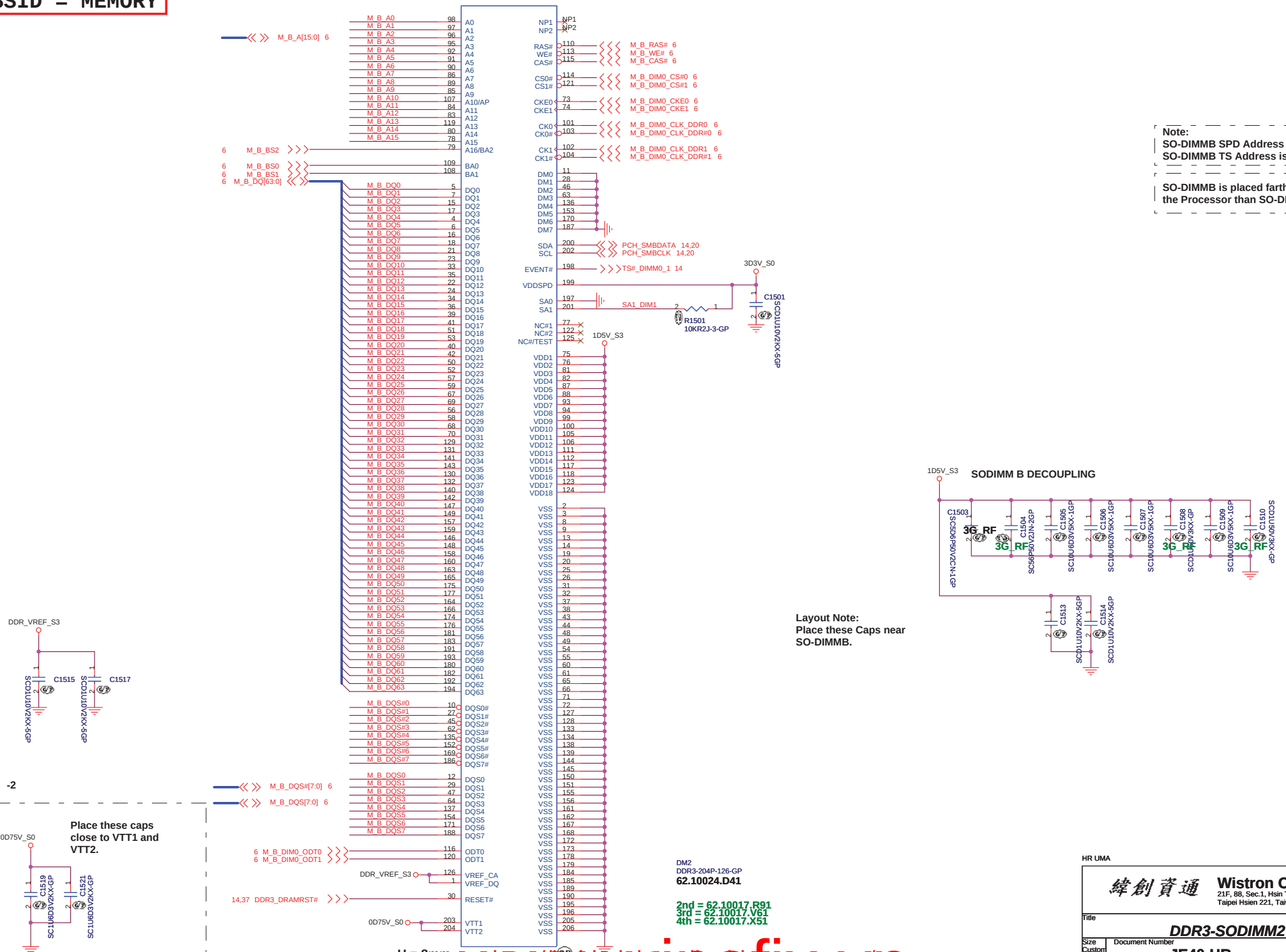
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**

Size	Document Number	Rev
Custom	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 14 of 102

SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

SODIMM B DECOUPLING

Layout Note:
Place these Caps near SO-DIMMB.

-2

H = 8mm

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***DDR3-SODIMM2***	
Size: Custom	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 15 of 102	

(Blanking)

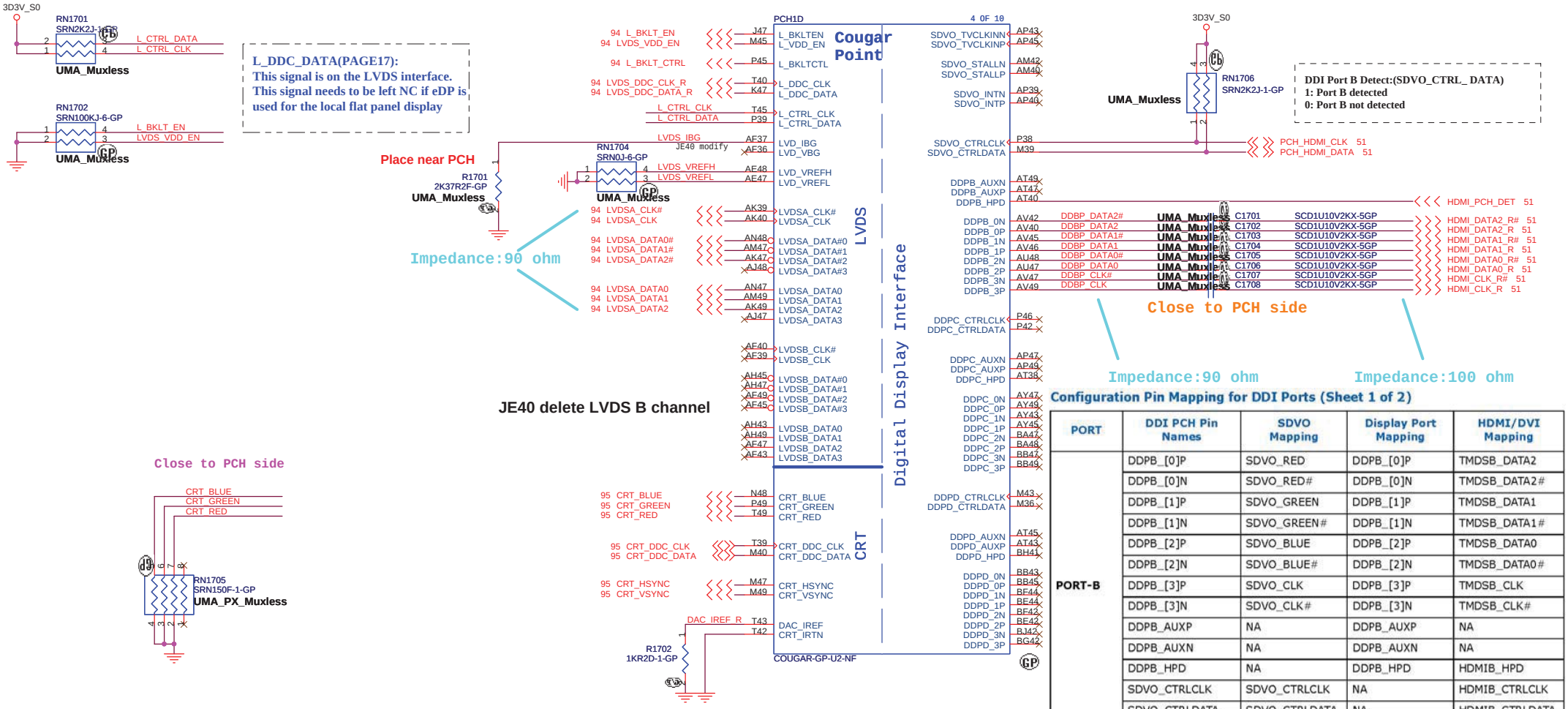
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR3-SODIMM2***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 16 of 102



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

HR UMA

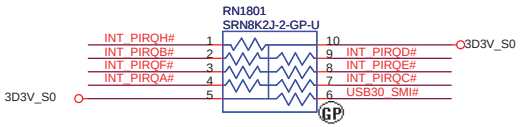
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: JE40-HR | Rev: -1

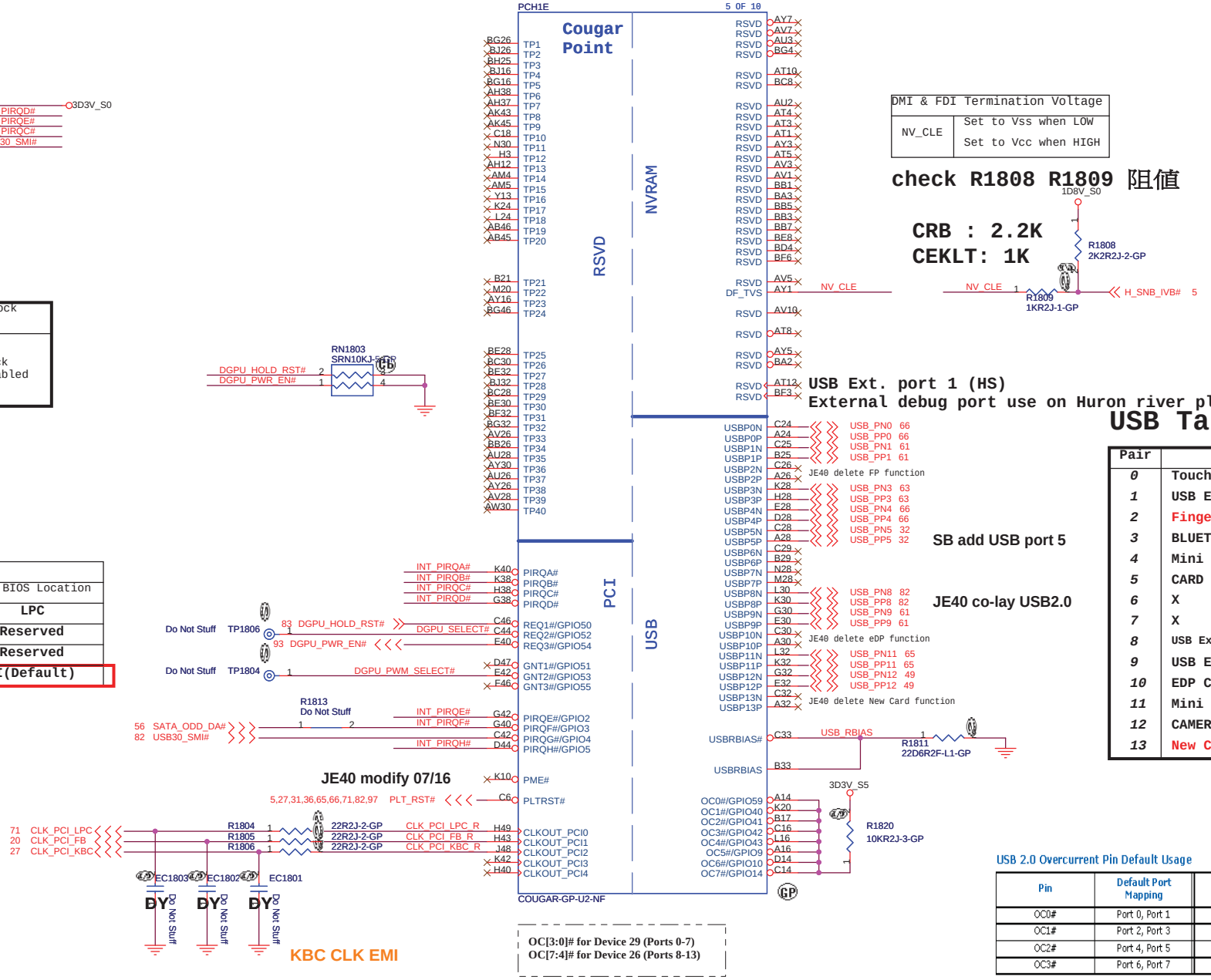
Date: Thursday, December 02, 2010 | Sheet 17 of 102

SSID = PCH



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

check R1808 R1809 阻值

CRB : 2.2K
CEKLT: 1K

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

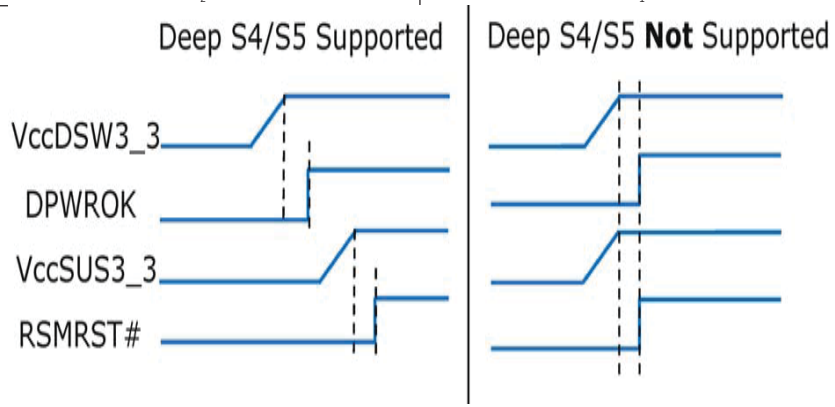
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

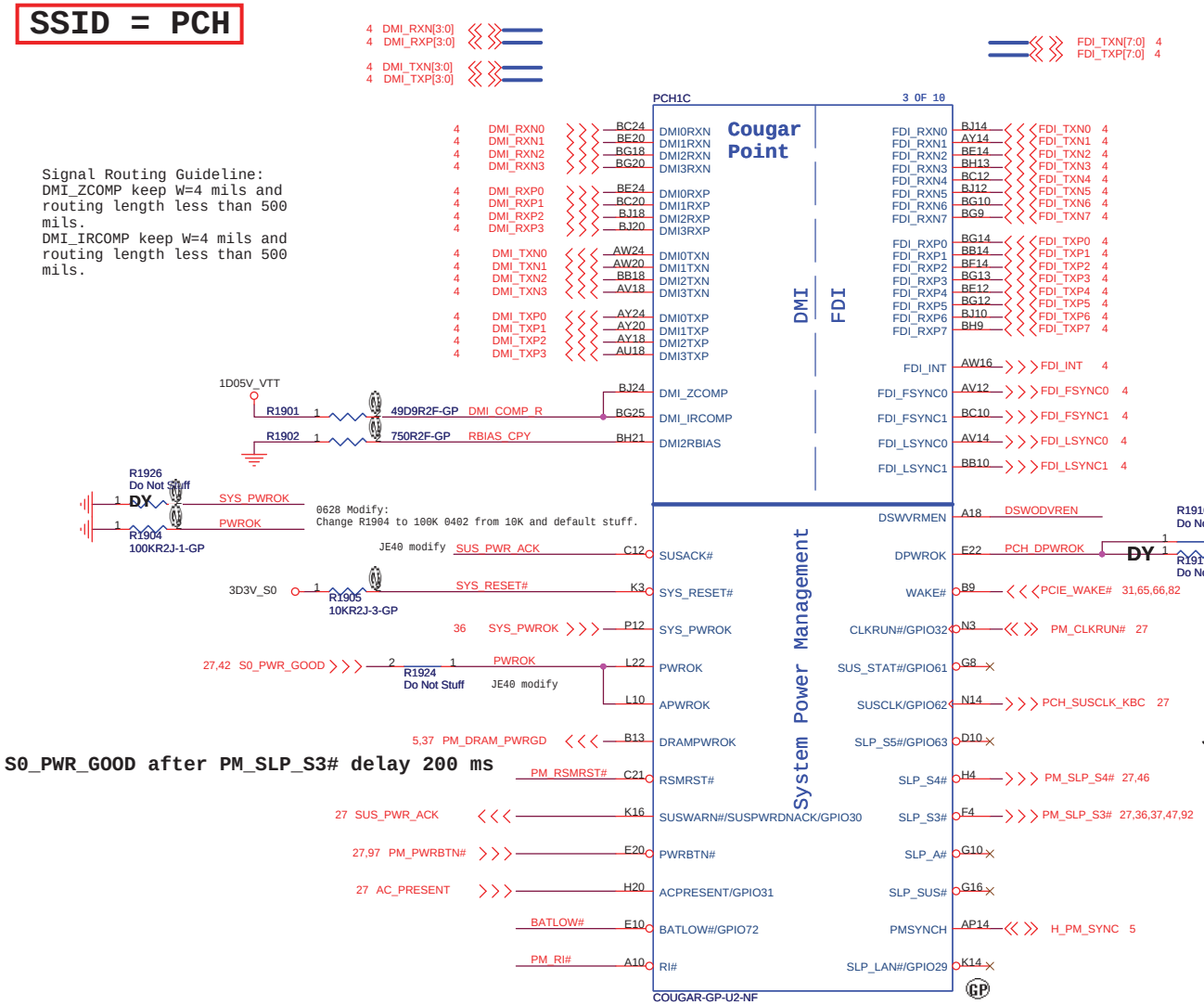
Title: PCH (PCI/USB/NVRAM)
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 18 of 102

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as 'no connect'
4.SUSWARN# used as SUSPWRDNACK/GPIO30

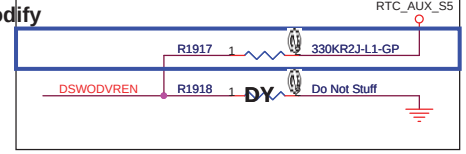


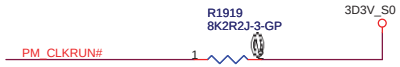
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

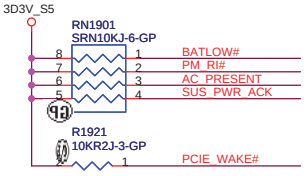
JE40 modify 07/16

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify

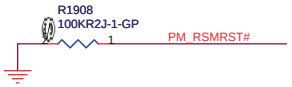




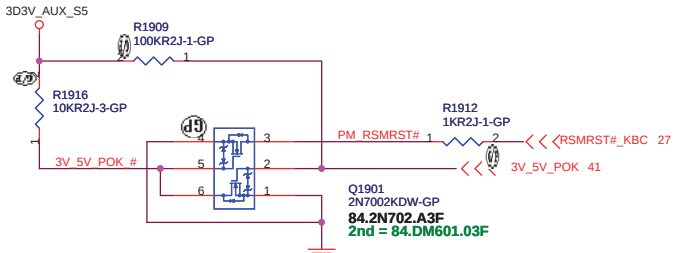


PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor



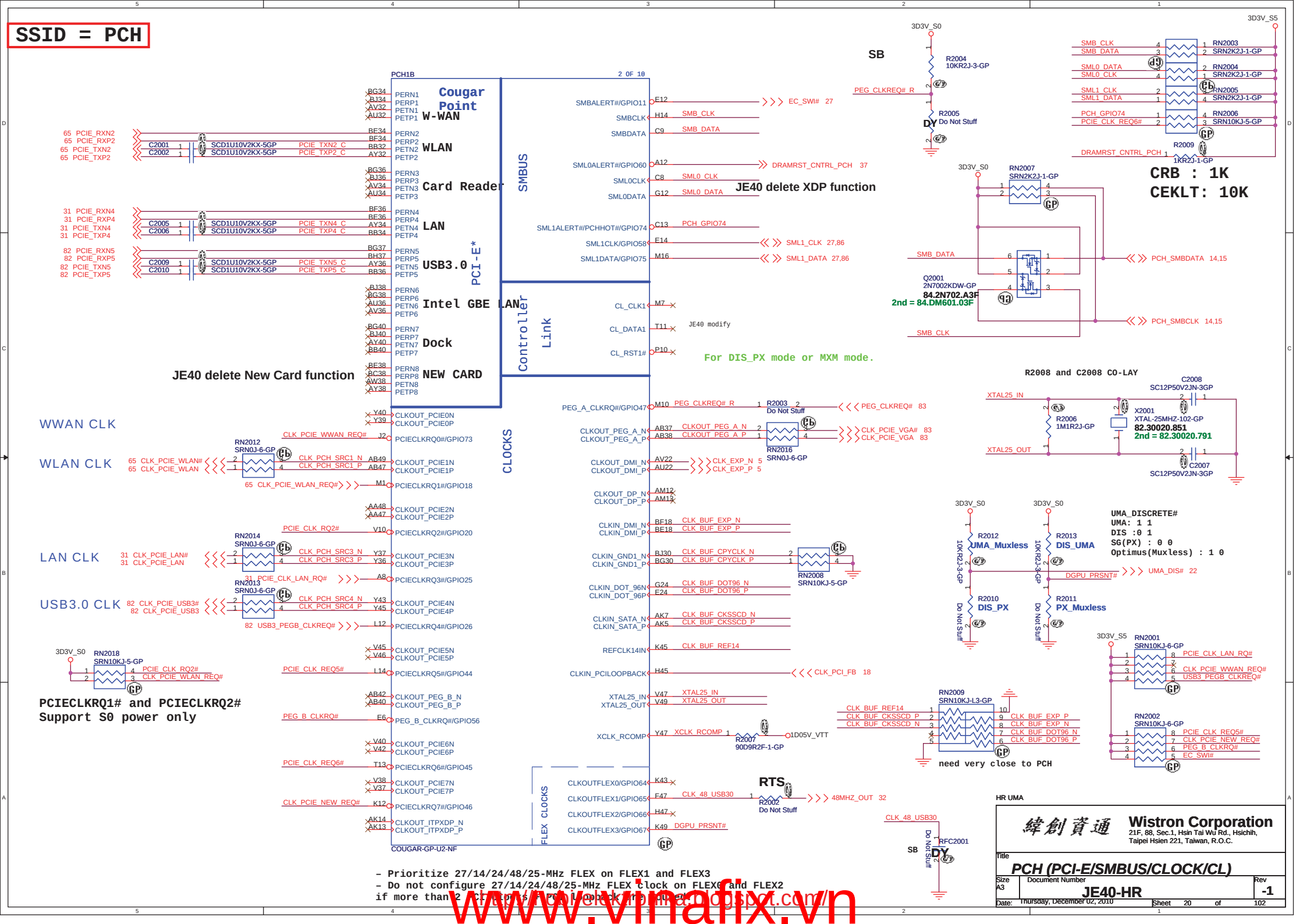
PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K



HR UMA

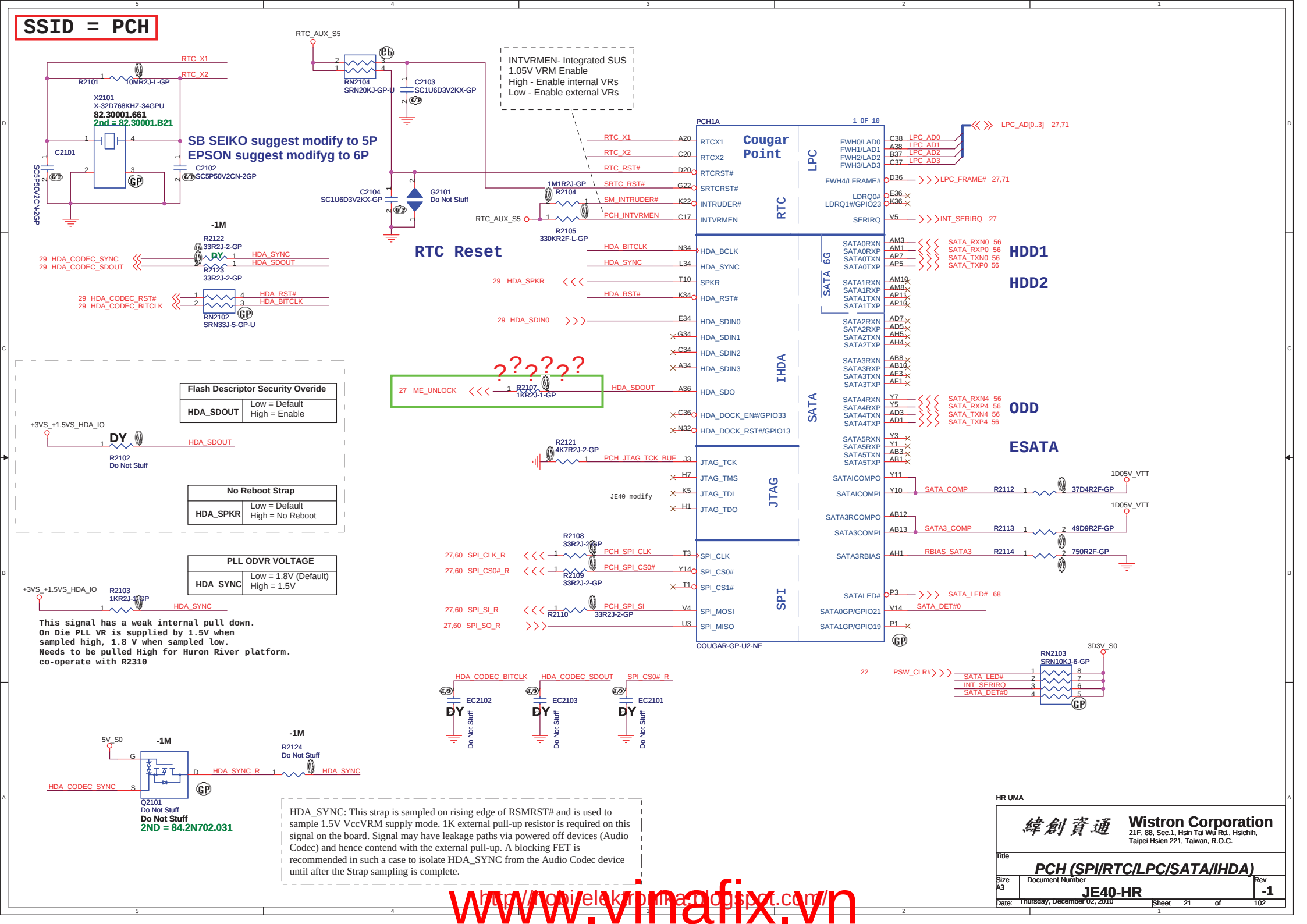
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: PCH (DM I/FDI/PM)		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 19 of 102	

SSID = PCH



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: PCH (PCI-E/SMBUS/CLOCK/CL)	
Size: A3	Document Number: JE40-HR
Rev: -1	
Date: Thursday, December 02, 2010	Sheet 20 of 102

SSID = PCH



HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH (SPI/RTC/LPC/SATA/IHDA)
Size A3	Document Number JE40-HR Rev -1
Date: Thursday, December 02, 2010	Sheet 21 of 102

SSID = PCH

Note:
For PCH debug with XDP, need to NO STUFF R2218

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_RCIN# — H_A20GATE

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

3D3V_S0 — R2220 10KR2J-3-GP — FFS_INT2_R

	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY

Pass Word Clear

GFX_CRB_DET — R2206 100KR2J-1-GP

3D3V_S0 — RN2201 SRN10KJ-6-GP — EC_SMI# / DGPU_HPD_INTR# / EC_SCI#

RN2202 SRN10KJ-6-GP — MFG_MODE / FP_DET# / S_GPIO / PCH_TEMP_ALERT#

3D3V_S5 — RN2204 SRN10KJ-6-GP — USB3_PWR_ON / PCH_GPIO12 / PCH_GPIO24

PCH_GPIO15 — R2201 1KR2J-1-GP

3D3V_S0 — R2202 10KR2J-3-GP — SATA_ODD_PRSNT#

27 EC_SCI# — 56 SATA_ODD_PRSNT#

92,93 DGPU_PWROK

0806 delete TP2202, TP2203
Do Not Stuff TP2202 — PCH_GPIO22
Do Not Stuff TP2203 — PCH_GPIO24
PCH_GPIO27
PLL_ODVR_EN

21 PSW_CLR# — JE40 delete FP function — G2201 Do Not Stuff

JE40 delete G Sensor

27 PCH_TEMP_ALERT# — Do Not Stuff TP2210 — USB3_PWR_ON

Do Not Stuff TP2206 — PCH_NCTF_1

Do Not Stuff TP2208 — PCH_NCTF_3

Do Not Stuff TP2207 — PCH_NCTF_2

Do Not Stuff TP2209 — PCH_NCTF_4

PCH1F — 6 OF 10 — **Cougar Point** — COUGAR-GP-U2-NF

GPIO: S_GPIO, EC_SMI#, DGPU_HPD_INTR#, ICC_EN#, PCH_GPIO12, PCH_GPIO15, SATA_ODD_PRSNT#, PCH_GPIO22, PCH_GPIO24, PCH_GPIO27, PLL_ODVR_EN, FP_DET#, DMI_OVRVLTG, FDI_OVRVLTG, MFG_MODE, GFX_CRB_DET, FFS_INT2_R, PCH_TEMP_ALERT#, USB3_PWR_ON

CPU/MISC: TACH4/GPIO68, TACH5/GPIO69, TACH6/GPIO70, TACH7/GPIO71, A20GATE, PECI, RCIN#, PROCPWRGD, THRMTRIP#, INIT3_3V#, TS_VSS1–4, NC_1

NCTF: NCTF_VSS#A4 … NCTF_VSS#F49 (NCTF TEST PIN: A4, A44, A45, A46, A5, A6, B3, B47, BD1, BD49, BE1, BE49, BF1, BF49; BG2, BG48, BH3, BH47, BJ4, BJ44, BJ45, BJ46, BJ5, BJ6, C2, C48; D1, D49, E1, E49, F1, F49)

SB add Zero ODD function

C40 SATA_ODD_PWRGT 56
B41 UMA_DIS# 20
C41 VRAM_SIZE1
A40 VRAM_SIZE2

P4 H_A20GATE 27
AU16 H_PECI_R — R2203 Do Not Stuff — DY — H_PECI 5,27
P5 H_RCIN# 27
AY11 H_CPUPWRGD 5,36,97
AY10 PCH_THERMTRIP_R
T14

RN2205 Do Not Stuff — DY — SB — 1D05V_VTT
PCH_THERMTRIP_R — R2204 54D9R2F-L1-GP — H_THERMTRIP# 5,36

AH8 / AK11 / AH10 / AK10 / P37

SB 公板 check different , check need modify or not check intel , R2204

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

ICC_EN# — R2211 1KR2J-1-GP

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

SB VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

3D3V_S0 — R2218 10KR2J-3-GP — UMA_VRAM800MHZ — PCH_GPIO22 — R2219 10KR2J-3-GP — VRAM900MHZ

VRAM Size

3D3V_S0 — 2G R2214 Do Not Stuff — 1G R2216 Do Not Stuff — VRAM_SIZE1 / VRAM_SIZE2

1G_512M R2215 Do Not Stuff — 512M_2G R2217 Do Not Stuff

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN — R2212 DY Do Not Stuff

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**
Size: A3 | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 22 of 102

SSID = PCH 6A

POWER

Cougar Point

PCH1G

7 OF 10

COUGAR-GP-U2-NF

VCC CORE | CRT | LVDS | HVCMOS | DMI | VCCIO | NAND / SPI | FDI

1D05V_VTT 1.3A

(1uFx3) (10uFx1_0603)

C2301 SC10U6D3V5KX-1GP, C2302 SC1U6D3V2KX-GP, C2303 SC1U6D3V2KX-GP, C2304 SC1U6D3V2KX-GP

VCCCORE: AA23, AC23, AD21, AD23, AE21, AE23, AG21, AG23, AG24, AG26, AG27, AG29, AJ23, AJ26, AJ27, AJ29, AJ31

1D05V_VTT AN19 VCCIO

JE40 modify 07/16

JE40 modify BJ22 VCCAPLLEXP

1D05V_VTT 2.925A(Total current of VCCIO)

(1uF x4)

C2306 DY Do Not Stuff, C2307 SC1U6D3V2KX-GP, C2308 SC1U6D3V2KX-GP, C2309 SC1U6D3V2KX-GP

VCCIO: AN16, AN17, AN21, AN26, AN27, AP21, AP23, AP24, AP26, AT24, AN33, AN34

0.266A (Totally VCC3_3 current)

(0.1uF x1)

3D3V_S0 BH29 VCC3_3

C2310 SCD1U10V2KX-5GP

0.159A(Totally current of VCCVRM)

-2 modify power net name

VCCVRM_S0 AP16 VCCVRM

0806 check VCCAFDIPLL BG6 VCCAFDIPLL

1D05V_VTT AP17 VCCIO

0.042A (Totally current of VCCDMI)

1D05V_VTT AU20 VCCDMI

JE40 modify

(0.1uF/0.01uF x1) (10uF x1_0603)

R2301 Do Not Stuff DIS, 3D3V_S0

3D3V_DAC_S0

U48 +VCCA_DAC_1_2, R2315 Do Not Stuff

U47

C2313 SCD01U16V2KX-3GP, C2314 SCD01U16V2KX-5GP, C2315 DY Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

0.001A

R2304 0R3J-0-U-GP, 3D3V_S0

UMA_PX_Muxless

VCCADAC, VSSADAC, VCCALVDS, VSSALVDS

AK36 +3VS_VCCA_LVDS

AK37 R2303 Do Not Stuff

VCCTX_LVDS: AM37, AM38, AP36, AP37

0.06A

R2309 Do Not Stuff DIS

C2316 SCD01U16V2KX-3GP, C2317 SCD01U16V2KX-3GP, C2318 DY Do Not Stuff

UMA_PX_Muxless UMA_PX_Muxless

+1.8VS_VCCTX_LVDS

R2305 0R5J-5-U-GP, 1D8V_S0

UMA_PX_Muxless

(0.01uF x2) (22uF x1)

VCC3_3: V33, V34

3D3V_S0

C2319 SCD1U10V2KX-5GP

-2 modify power net name

VCCVRM_S0 AT16 VCCVRM

1D05V_VTT

VCCDMI AT20 JE40 modify (1uF x1)

C2320 SC1U6D3V2KX-GP

VCCCLKDMI AB36

0.02A

L2303 IND-10UH-218-GP, 1D05V_VTT

+1.05VS_VCC_DMI_CCI

68.10050.10Y

2nd = 68.10090.10B

C2321 SC1U6D3V2KX-GP, C2325 DY Do Not Stuff

(1uFx1) (10uFx1)

VccDFTERM: AG16, AG17, AJ16, AJ17

1D8V_S0

0.19A

JE40 modify

C2326 SCD1U10V2KX-5GP, C2322 SCD1U10V2KX-5GP

VCCSPI V1

0.02A

3D3V_S5

C2323 SC1U6D3V2KX-GP (1uFx1)

U2301 for ANNIE flicker issue

R2312 for don't flicker solution

3.3V CRT LDO

U2301 G9091-330T11U-GP

74.09091.J3F

2nd = 74.09198.G7F

5V_S0, 3D3V_DAC_S0

VIN VOUT GND EN NC#4

C2311 SC1U6V2KX-1GP

UMA_PX_Muxless UMA_PX_Muxless UMA_PX_Muxless

C2312 SC1U6D3V2KX-GP, C2327 SC1U6D3V3MX-GP

SB add C2327

-1M add LDO for VCCVRM_S0

3D3V_S0 1D5V_S0 VCCVRM_S0

U2302 G913CF-GP

74.00913.A3F

SHDN# GND IN SET OUT

DY

C2328 DY SC1U10V3KX-3GP

C2329 DY SC4D7U6D3V3KX-GP

C2330 DY SC22P50V2JN-4GP, R2316 DY 2K8R2F-GP

C2331 DY SCD1U10V2KX-5GP, R2317 DY 10KR2J-3-GP

Vout=1.25*(1+R1/R2)

Refer to NPCE795 shared SPI flash architecture

3.3V_BC

VCC

EC

SUSPWR_ON

(**) - When the control signal is low, the switch is 'on'.

VccDSW3_3 VccSUS3_3 VccSPI

APWROK RSMRST

PCH

SB 公板suggest delete 3D3V_S0, R2313

SPI only support 3D3V_S5

The same BIOS SPI ROM power

HR UMA

緯創資通 Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 23 of 102

JE40 modify 07/16

SSID = PCH

POWER

PCH1J — 10 OF 10

Cougar Point

USB | Clock and Miscellaneous | PCI/GPIO/LPC | SATA | CPU | MISC | RTC | HDA

COUGAR-GP-U2-NF

Clock and Miscellaneous

- JE40 modify AD49 VCCACLK
- (0.1uFx1) 3D3V_S5 0.002A T16 VCCDSW3_3
- (10uFx1) (1uFx1)
- JE40 modify V12 DCPSUSBYP
- 3D3V_S0 — C2402 SC1U10V2KX-1GP — JE40 modify T38 VCC3_3
- JE40 modify BH23 VCCAPLLDMI2
- 1D05V_VTT (10uFx1) AL29 VCCIO
- JE40 modify AL24 DCPSUS
- 1D05V_VTT — 1.01A (Total current of VCCASW) — C2403 C2404 C2406 C2407 C2408 DY Do Not Stuff — (22uFx2_0603) (1uFx3)
- VCCASW: AA19, AA21, AA24, AA26, AA27, AA29, AA31, AC26, AC27, AC29, AC31, AD29, AD31, W21, W23, W24, W26, W29, W31, W33
- 0.16A (Totally current of VCCVRM)
- +VCCRTCEXT — C2411 SCD1U10V2KX-5GP (0.1uFx1) — -1M VCCVRM_S0 Y49 VCCVRM
- +1.05VS_VCCA_A_DPL BD47 VCCADPLLA
- +1.05VS_VCCA_B_DPL BF47 VCCADPLLB
- JE40 modify 07/16
- 1D05V_VTT — C2412 SC1U6D3V2KX-GP — JE40 modify (1uFx1) — AF17 VCCIO, AF33 VCCDIFFCLKN, AF34 VCCDIFFCLKN, AG34 VCCDIFFCLKN
- (1uFx1) — 0.055A — C2414 SC1U6D3V2KX-GP
- 1D05V_VTT — C2413 SC1U6D3V2KX-GP — JE40 modify (1uFx1) — 0.095A — AG33 VCCSSC
- +VCCSST — (0.1uFx1) — C2415 SCD1U10V2KX-5GP — JE40 modify — V16 DCPSST, T17 DCPSUS, V19 DCPSUS
- (1uFx1)
- 1D05V_VTT — 0.001A — (0.1uFx2) (4.7uFx1_0603) — C2417 C2418 C2419 DY Do Not Stuff — BJ8 V_PROC_IO
- RTC_AUX_S5 — 6uA — (0.1uFx2) (1uFx1) — C2420 SC1U6D3V2KX-GP — A22 VCCRTC
- 1D05V_VTT — L2402 IND-10UH-218GP — 0.08A — (1uFx1) (220uFx1) — +1.05VS_VCCA_A_DPL — 68.10050.10Y — 2nd = 68.10090.10B — C2409 SC1U6D3V2KX-GP
- L2403 IND-10UH-218GP — 0.08A — (1uFx1) (220uFx1) — +1.05VS_VCCA_B_DPL — 68.10050.10Y — 2nd = 68.10090.10B — C2410 SC1U6D3V2KX-GP

USB

- 1D05V_VTT — C2423 SC1U6D3V2KX-GP (1uFx1) — VCCIO N26, P26, P28, T27, T29
- 3D3V_S5 — 0.097A (Totally current of VCCSUS3_3) — (0.1uFx1) C2424 SCD1U10V2KX-5GP — VCCSUS3_3 T23, T24, V23, V24
- 3D3V_S5 — (0.1uFx1) C2425 SCD1U10V2KX-5GP — VCCSUS3_3 P24
- VCCIO T26 1D05V_VTT
- V5REF_SUS M26 +5VA_PCH_VCC5REFSUS — 0.001A

PCI/GPIO/LPC

- DCPSUS AN23 JE40 modify
- VCCSUS3_3 AN24 3D3V_S5 JE40 modify
- V5REF P34 +5VS_PCH_VCC5REF — 0.001A
- VCCSUS3_3 N20, N22, P20, P22 — 3D3V_S5 (1uFx1) JE40 modify 07/16 — C2428 SC1U6D3V2KX-GP
- VCC3_3 AA16, W16, T34 — 3D3V_S0 (0.1uFx2) — C2430 SCD1U10V2KX-5GP, C2431 SCD1U10V2KX-5GP
- VCC3_3 AJ2 — 3D3V_S0 (0.1uFx1) — C2429 SCD1U10V2KX-5GP
- VCCIO AF13, AH13, AH14, AF14 — 1D05V_VTT (1uFx1) — C2432 SC1U6D3V2KX-GP
- VCCAPLLSATA AK1 JE40 modify
- VCCVRM AF11 VCCVRM_S0 — -1M modify power net name
- VCCIO AC16, AC17, AD17 — 1D05V_VTT — JE40 modify (1uFx1) JE40 modify 07/16 — C2435 SC1U6D3V2KX-GP

SATA

MISC

- VCCASW T21, V21, T19 — 1D05V_VTT — C2434 SC1U6D3V2KX-GP

HDA

- VCCSUSHDA P32 — +3VS_+1.5VS_HDA_IO — 0.01A — (0.1uFx1) — C2433 SCD1U10V2KX-5GP

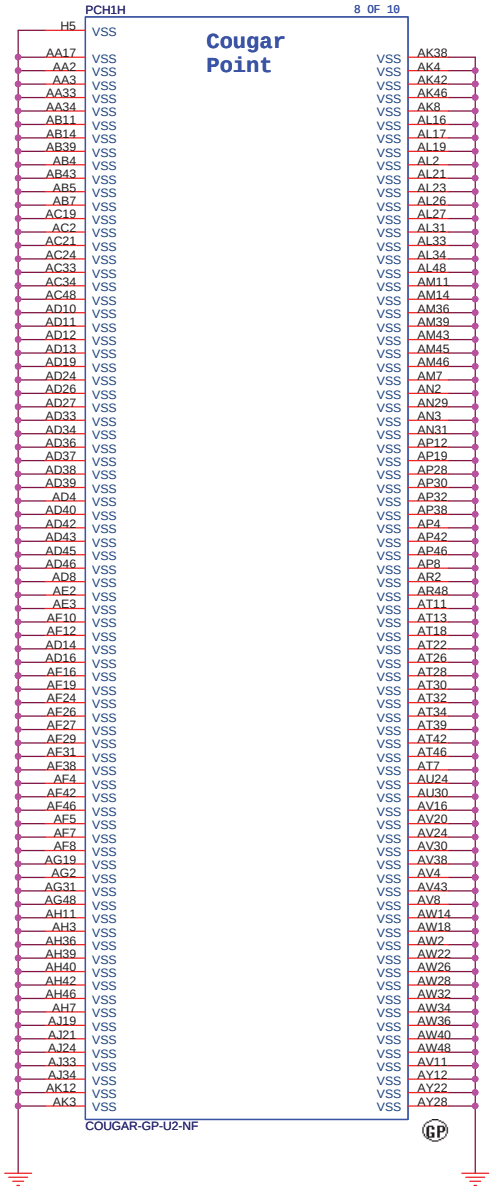
JE40 modify 07/16

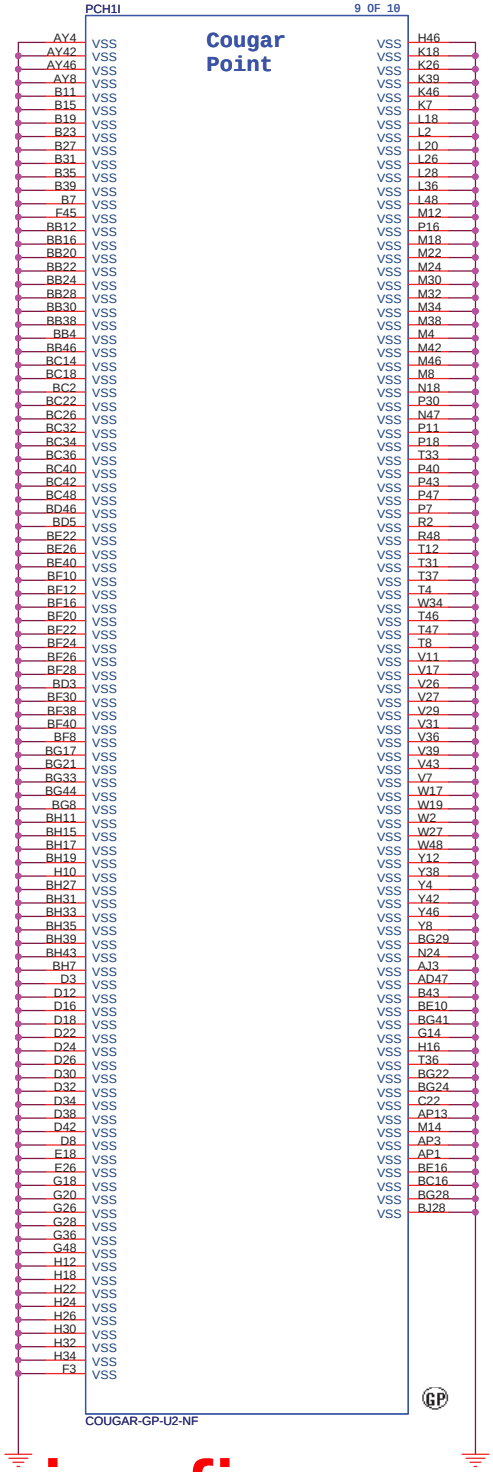
- 3D3V_S5 5V_S5 — D2401 Do Not Stuff — DY Do Not Stuff — 2nd = 83.R2004.B8F — R2408 10R2J-2-GP (0.1uFx1) — C2426 SCD1U10V2KX-5GP
- 3D3V_S0 5V_S0 — D2402 Do Not Stuff — DY Do Not Stuff — 2nd = 83.R2004.B8F — R2407 10R2J-2-GP (1uFx1) — C2427 SC1U10V2KX-1GP
- R2414 Do Not Stuff — 3D3V_S5 — DY — 1D5V_S5 — R2402 DY Do Not Stuff
- U2401 Do Not Stuff — 3D3V_S5 — VIN GND EN — DY VOUT NC#4 — 1D5V_S5 — C2436 DY Do Not Stuff — C2416 DY Do Not Stuff — C2405 DY Do Not Stuff
- +3VS_+1.5VS_HDA_IO -1M — R2409 Do Not Stuff — 3D3V_S5 — R2415 DY Do Not Stuff — 1D5V_S0 — R2413 DY Do Not Stuff — 1D5V_S5

HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*PCH (POWER2)*
Size A3	Document Number JE40-HR — Rev -1
Date: Thursday, December 02, 2010	Sheet 24 of 102

SSID = PCH





HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *PCH (VSS)*		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 25 of 102	

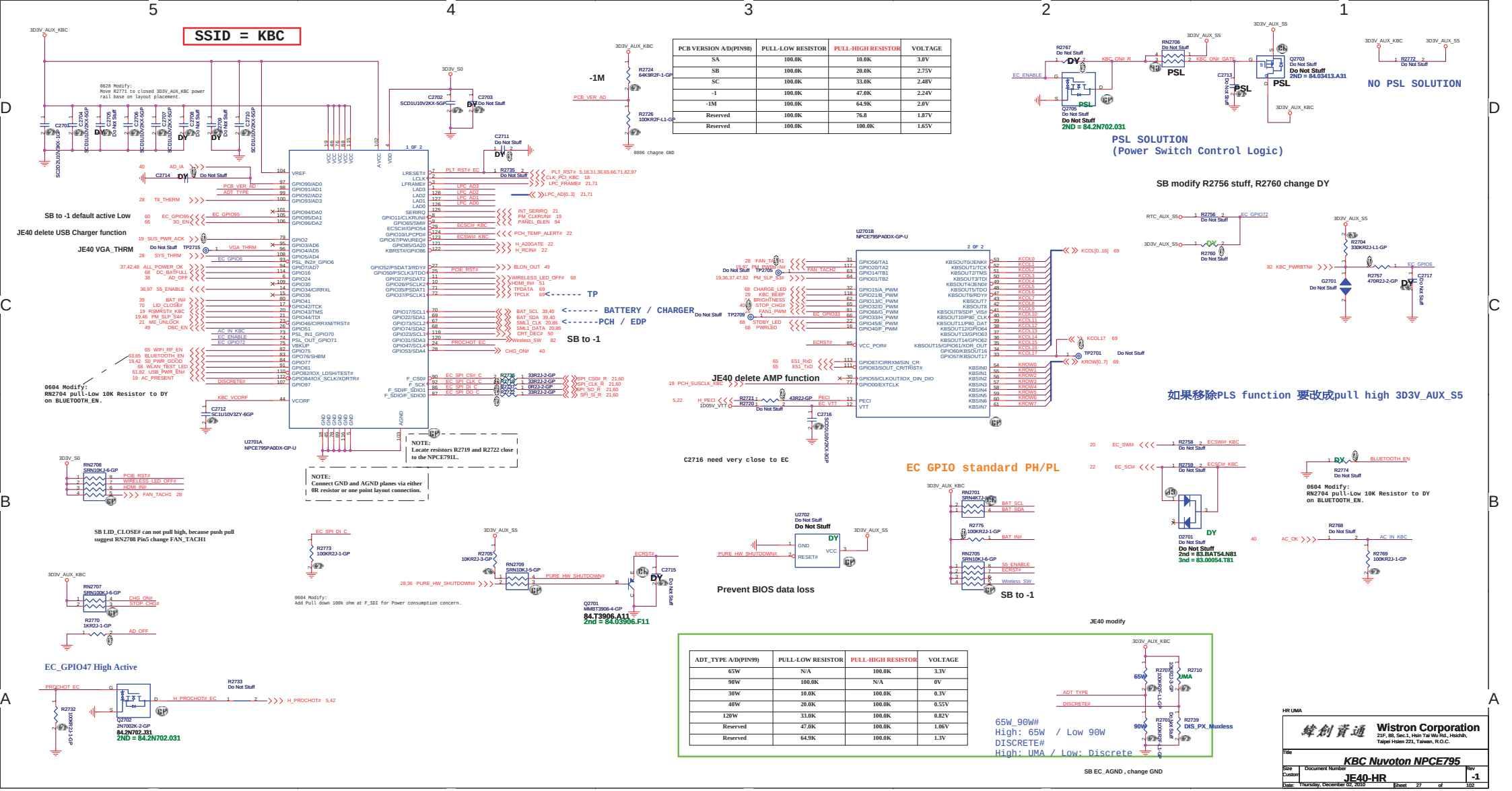
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Clock(colay)***

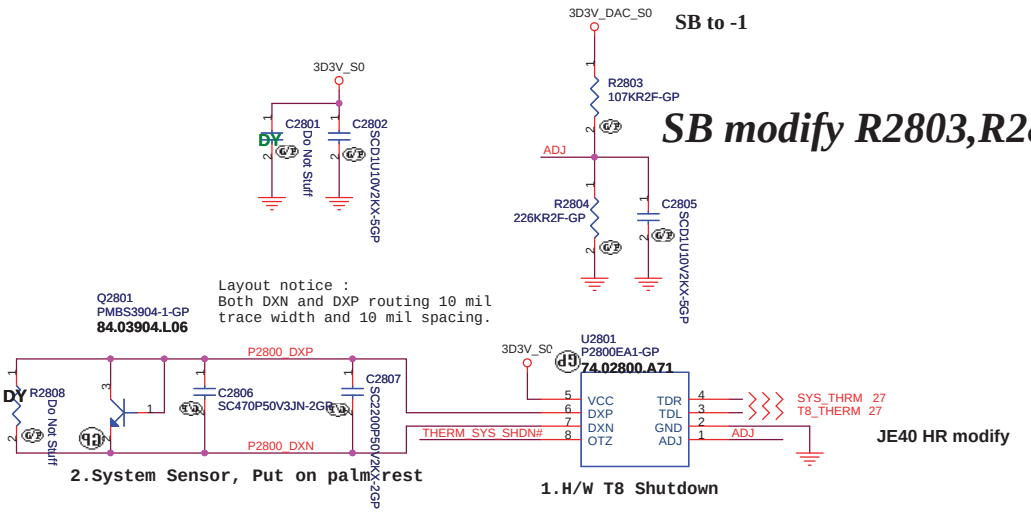
Size	Document Number	Rev
A4	**JE40-HR**	**-1**

Date: Thursday, December 02, 2010 Sheet 26 of 102



SSID = Thermal

Thermal sensor P2800



SB modify R2803,R2804 setting

ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

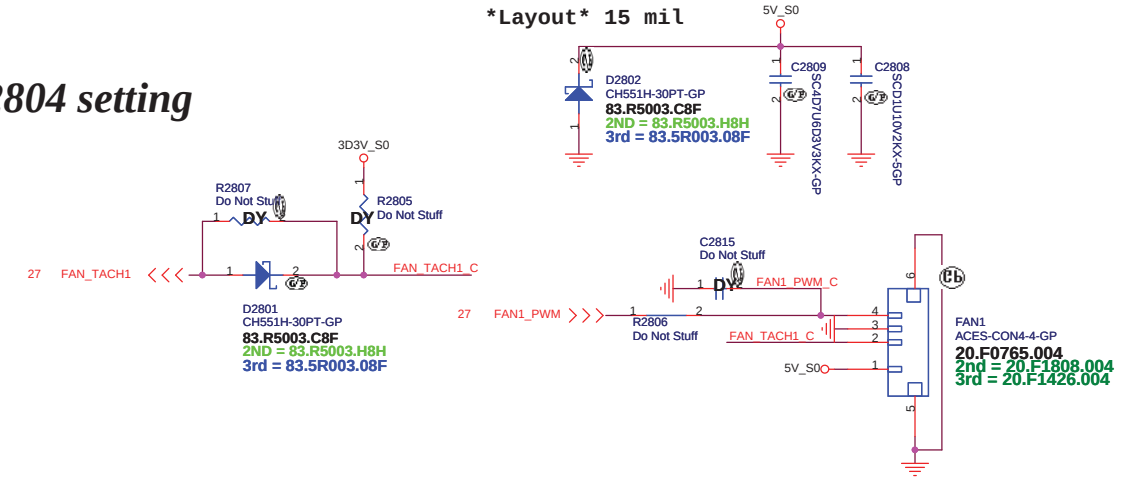
RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

VGA Thermal sensor P2800

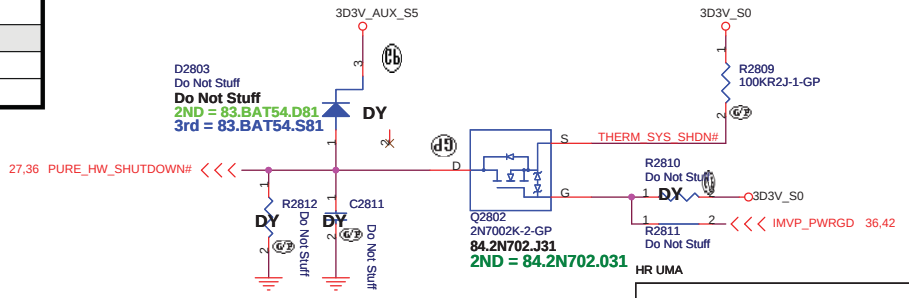
SMBUS modify to Page 84

Fan controller P2793

Layout 15 mil



For PWM FAN

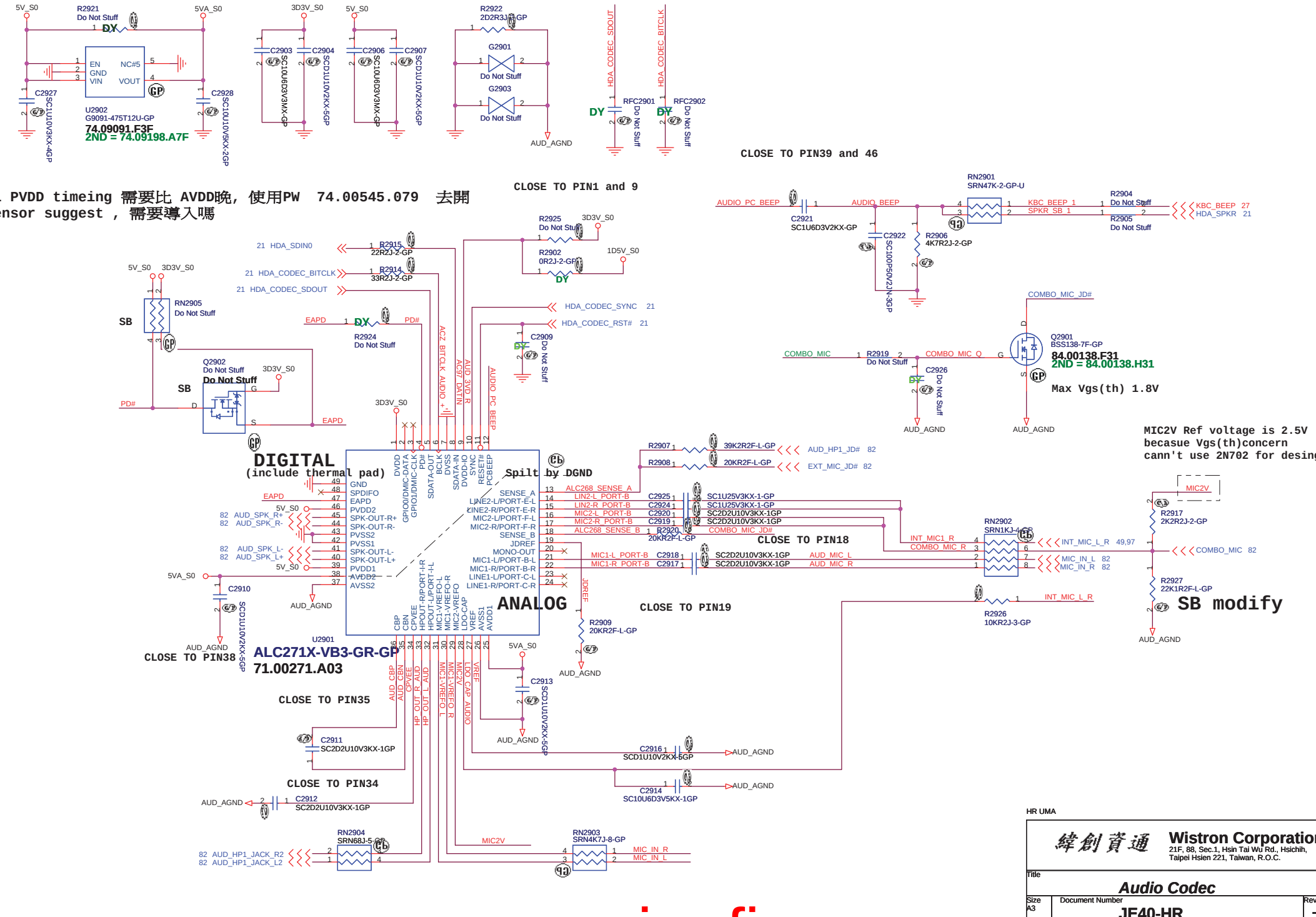


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 28 of 102


-1 PVDD timeing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎
CLOSE TO PIN1 and 9
CLOSE TO PIN39 and 46
DIGITAL
(include thermal pad)
Spilt by DGND
ANALOG
ALC271X-VB3-GR-GP
71.00271.A03
U2901
U2902
G9091-475T12U-GP
74.09091.F3F
2ND = 74.09198.A7F
RN2905
Do Not Stuff
SB
Q2902
Do Not Stuff
R2924
Do Not Stuff
R2925
Do Not Stuff
R2902
0R2J-2-GP
C2909
Do Not Stuff
RN2901
SRN47K-2-GP-U
R2904
Do Not Stuff
R2905
Do Not Stuff
C2921
SC1U6D3V2KX-GP
C2922
SC100P50V2JN-3GP
R2906
4K7R2J-2-GP
Q2901
BSS138-7F-GP
84.00138.F31
2ND = 84.00138.H31
Max Vgs(th) 1.8V
R2919
Do Not Stuff
C2926
Do Not Stuff
MIC2V Ref voltage is 2.5V
becasue Vgs(th)concern
cann't use 2N702 for desing
CLOSE TO PIN18
CLOSE TO PIN19
CLOSE TO PIN38
CLOSE TO PIN35
CLOSE TO PIN34
RN2902
SRN1KJ-4-GP
R2926
10KR2J-3-GP
R2917
2K2R2J-2-GP
R2927
22K1R2F-L-GP
SB modify
RN2904
SRN68J-5-GP
RN2903
SRN4K7J-8-GP
HR UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec
JE40-HR
-1
Thursday, December 02, 2010
Sheet 29 of 102
http://dobivelektronika.blogspot.com/
www.vinafix.vn

AUDIO OP AMPLIFIER

JE40 delete AMP function

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Audio AMP***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 30 of 102	

SB modify L3101,2,4,5,6 to 0 ohm

SB modify R3102 DY, R3104 to pull low

SB mmodify vendor suggest

SB delete EEPROM

128K byte

SB delete R3112

SB delete R3117

SB delete R3129 for LDO power

Card-reader Off-Page

Check VDDO_CR power plan

SB for B version

SB for B version can no use LDO delete LDO

SB to -1 modify to short pad

SB C3134, C3135 change 15P

68.00248.011

2nd = 68.00217.241

82.30020.851

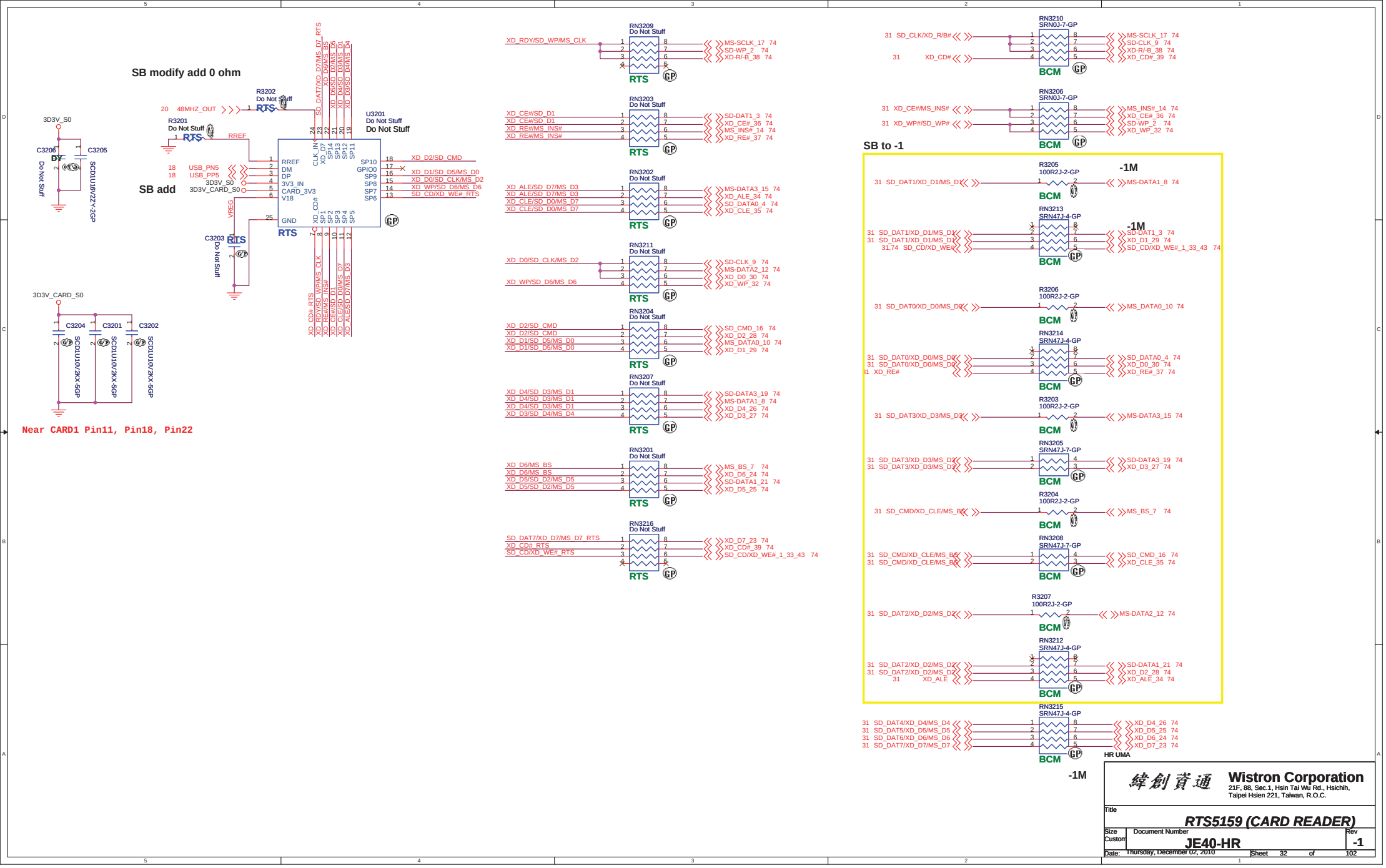
71.57785.M02

Change:71.57785.M03

10月底改打71.57785.M03

DY DY

HR UMA	
緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	BCM57780
Size: Custom	Document Number: JE40-HR
Rev	-1
Date: Thursday, December 02, 2010	Sheet 31 of 102



(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 33 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 34 of 102

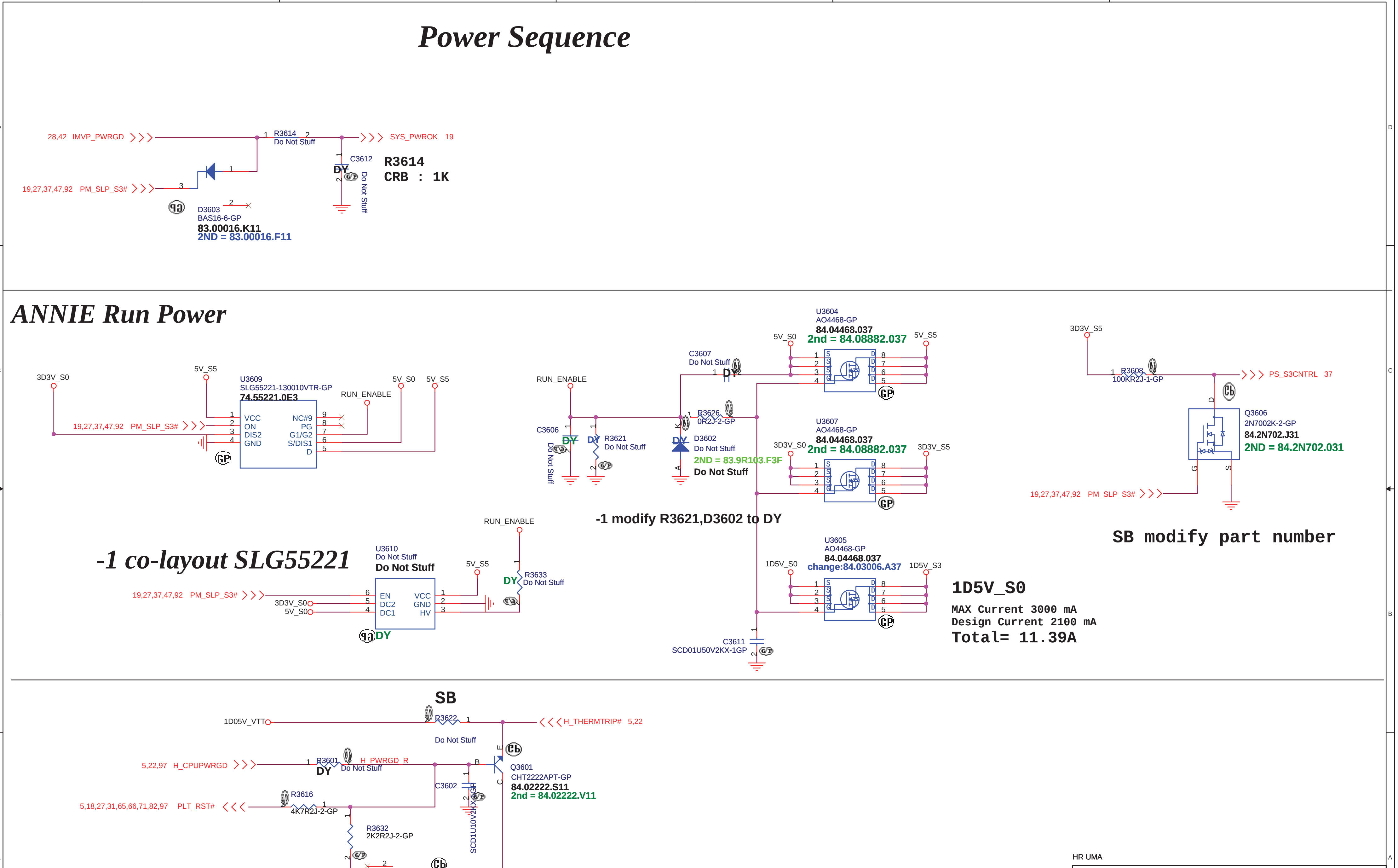
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Controller***

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 35 of 102



HR UMA

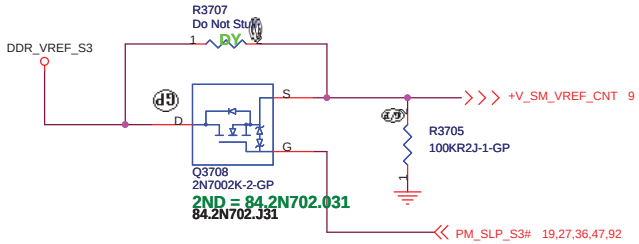
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

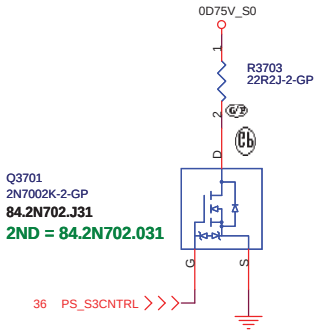
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 36 of 102

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

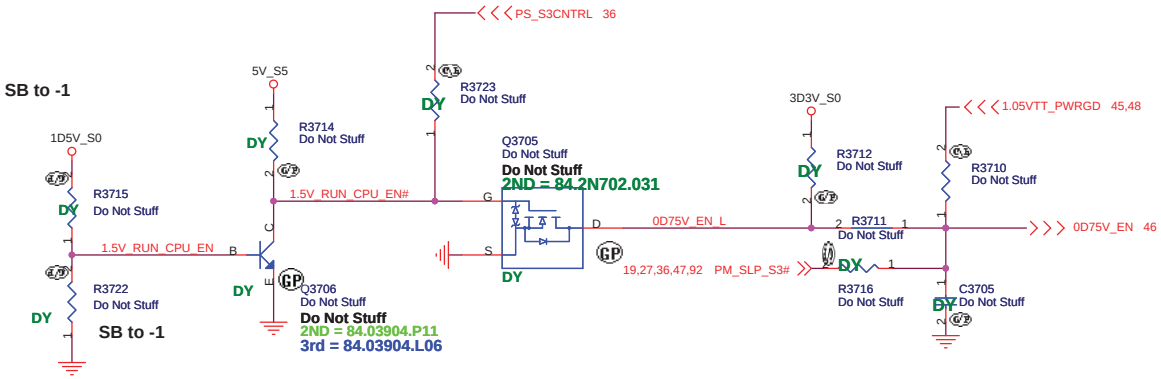


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

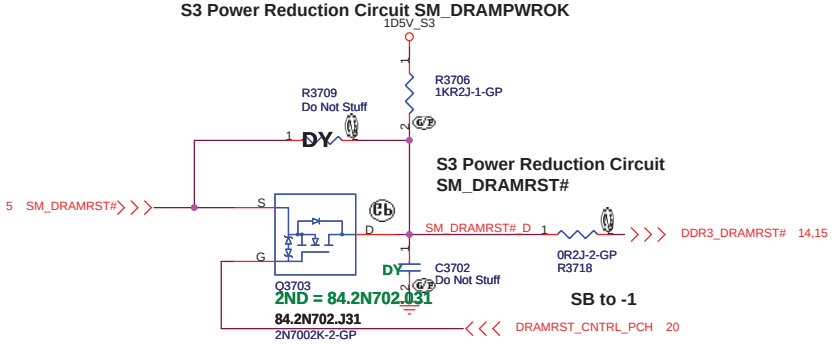


5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

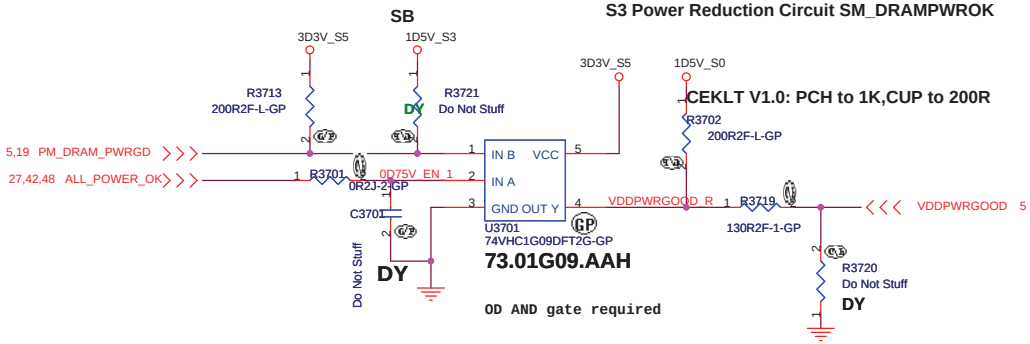
SB to -1 reserve R3723



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55 * 200mV and the edge must be monotonic

HR UMA

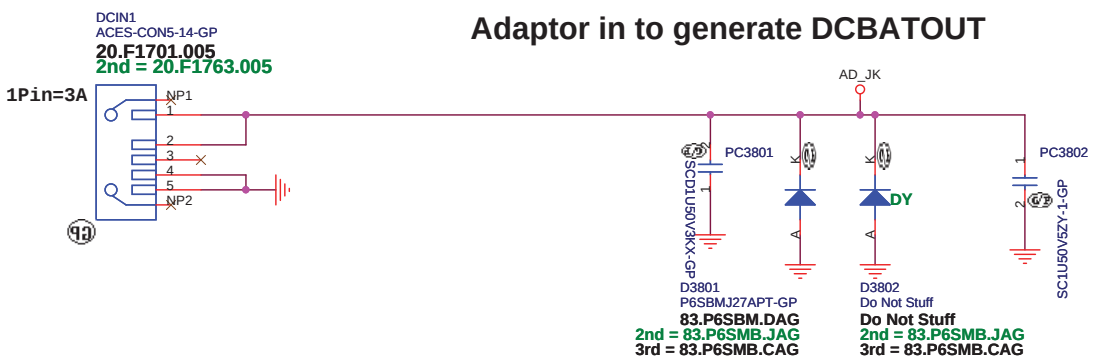
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ADAPTER

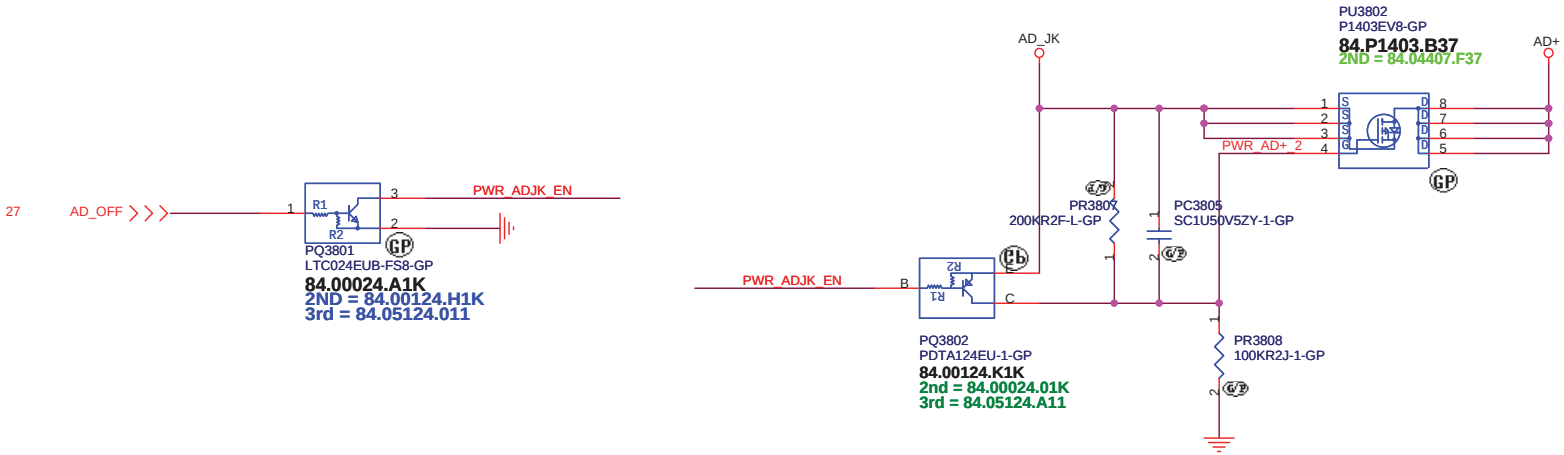
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 37 of 102

ANNIE solution



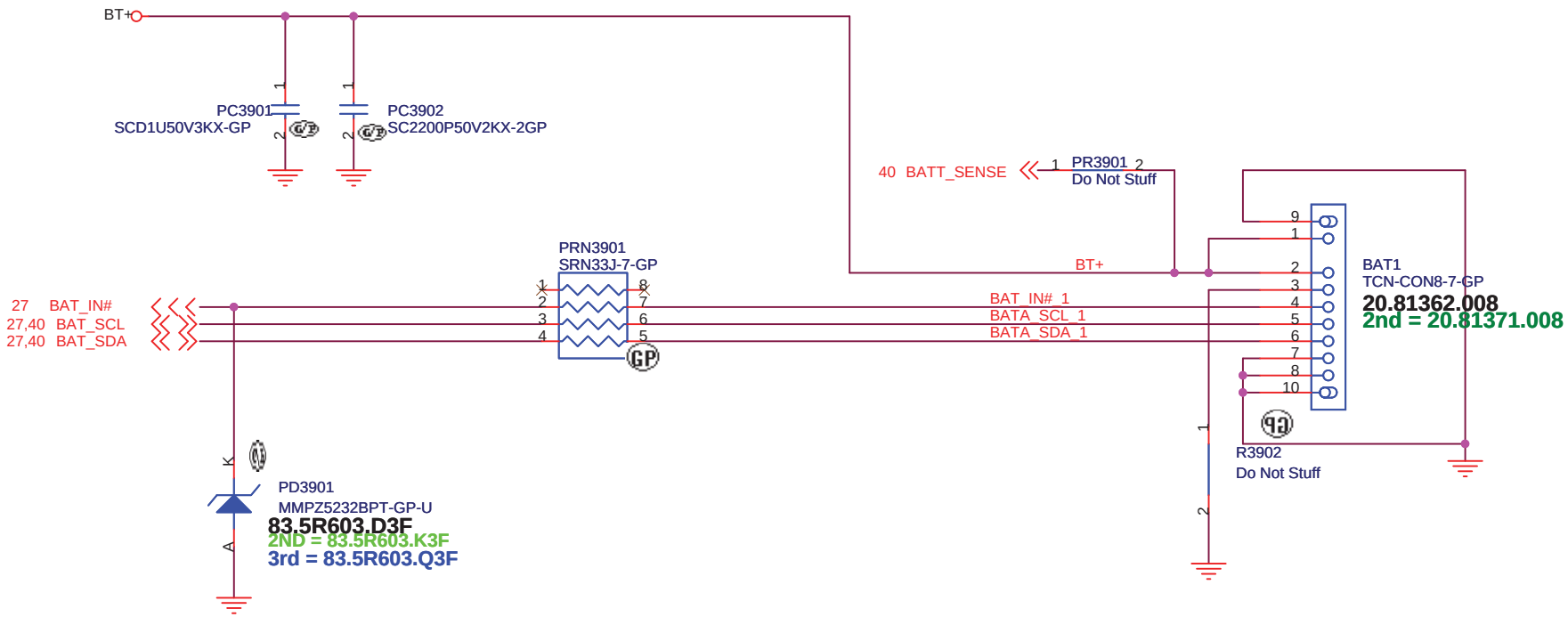
JE40 change DCIN1 part number



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *DCIN JACK*		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 38 of 102	

BATTERY CONNECTOR



EC Protect

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BATT CONN**

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 39 of 102

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

NEAR

ADD A 24V ZENAR

20100706 Wayne

20100721

20101018

JE40 HR RF

-1M

-1M

AC_OK to KBC

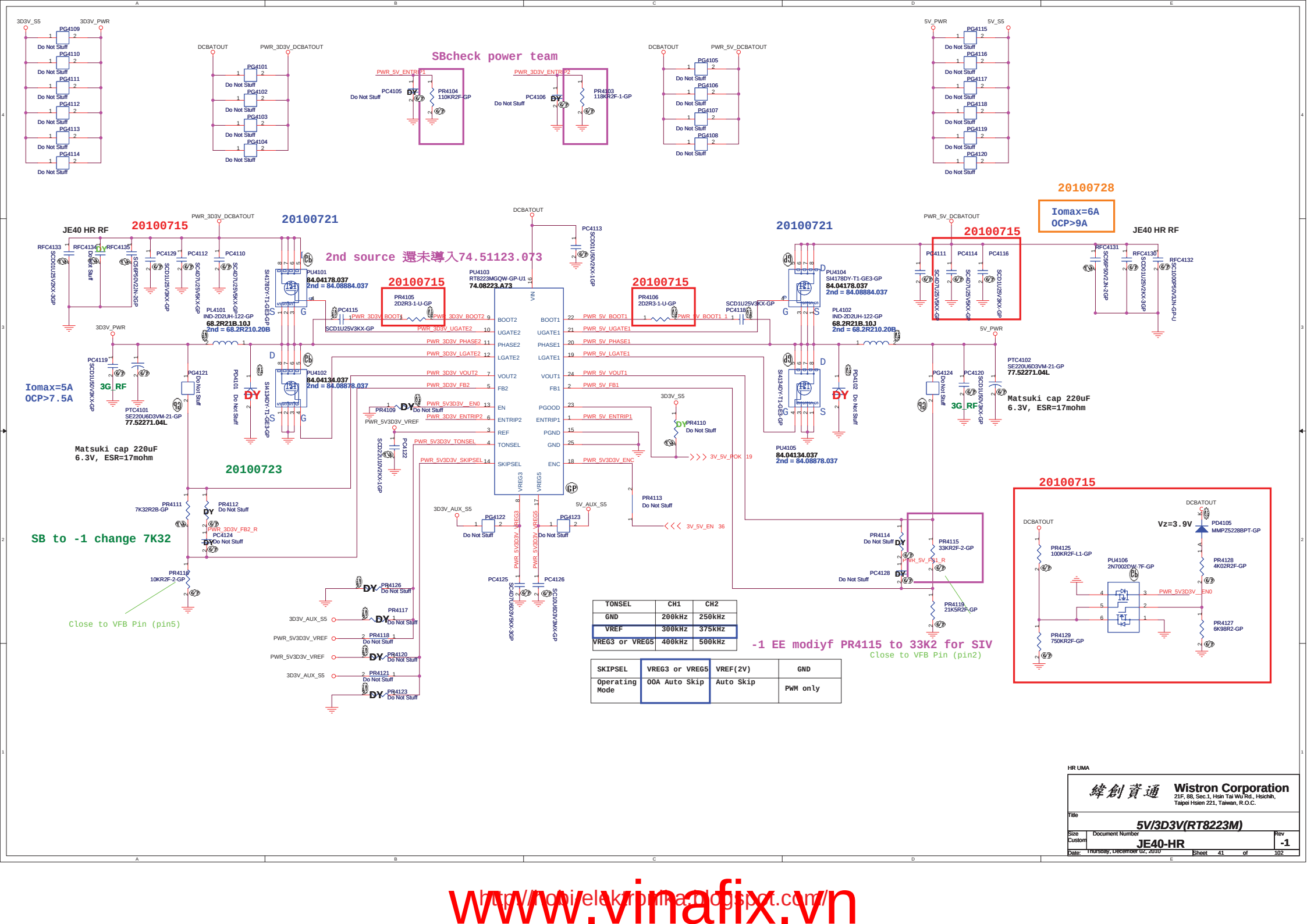
HR UMA

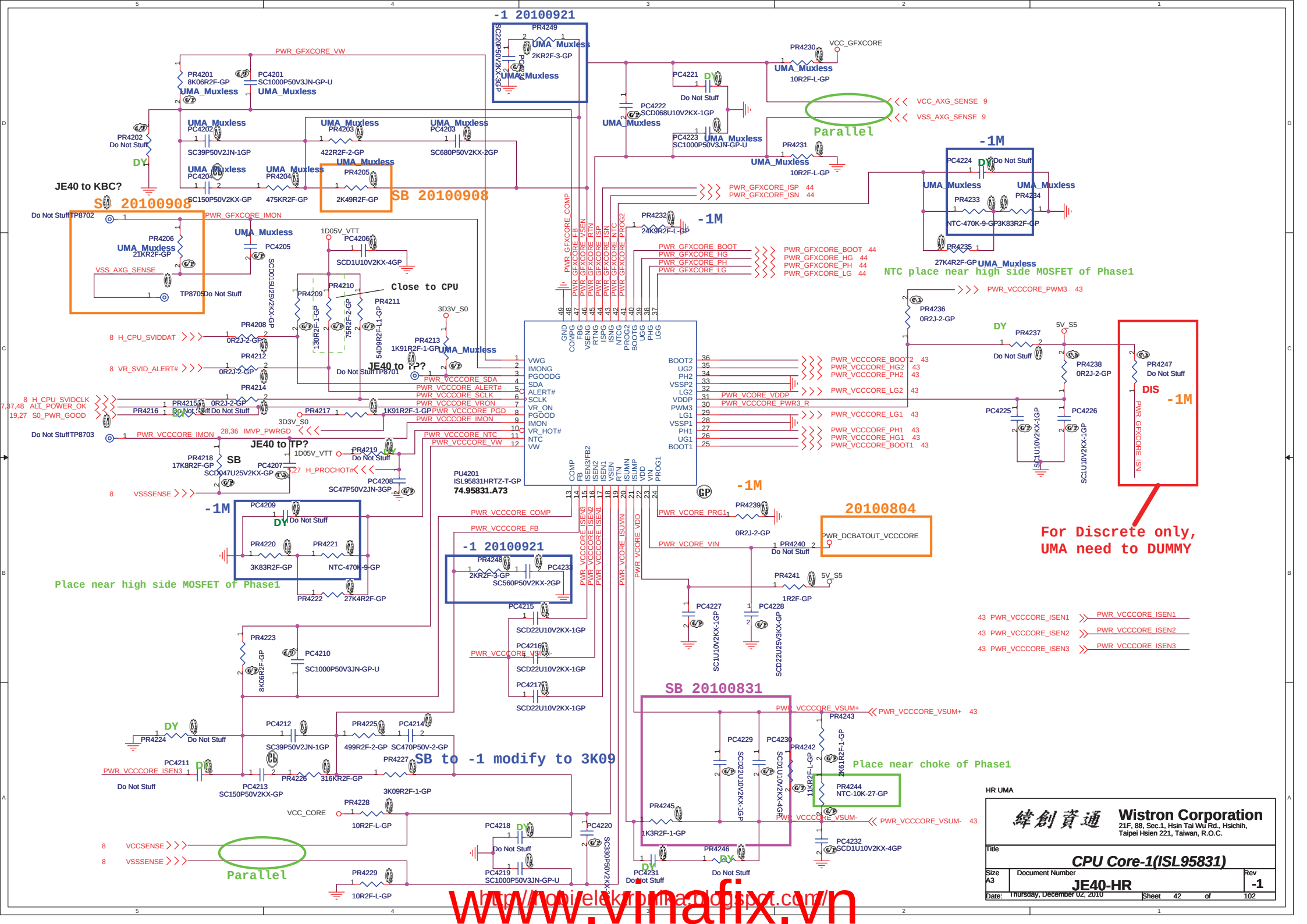
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

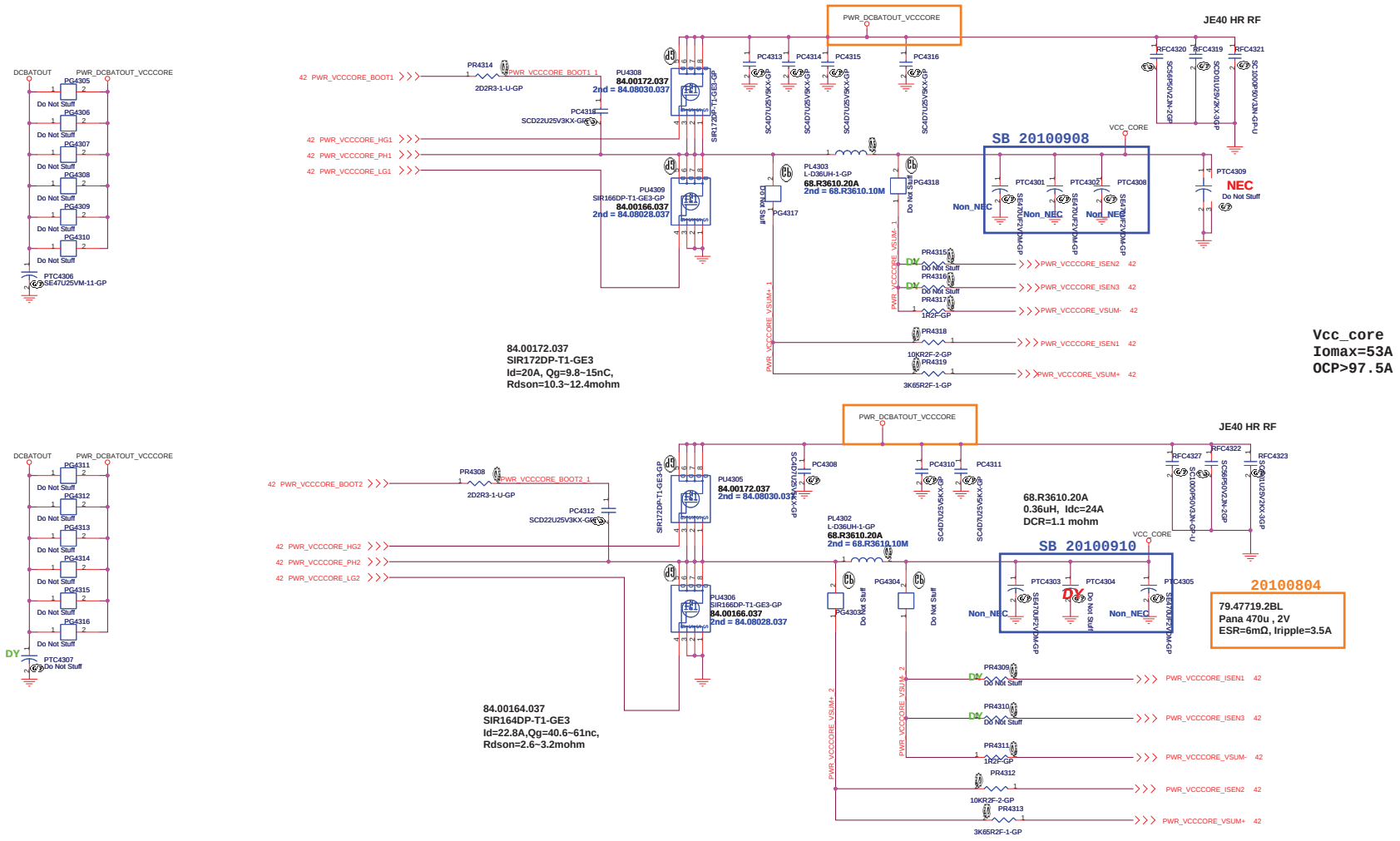
Title: CHARGER BQ24745

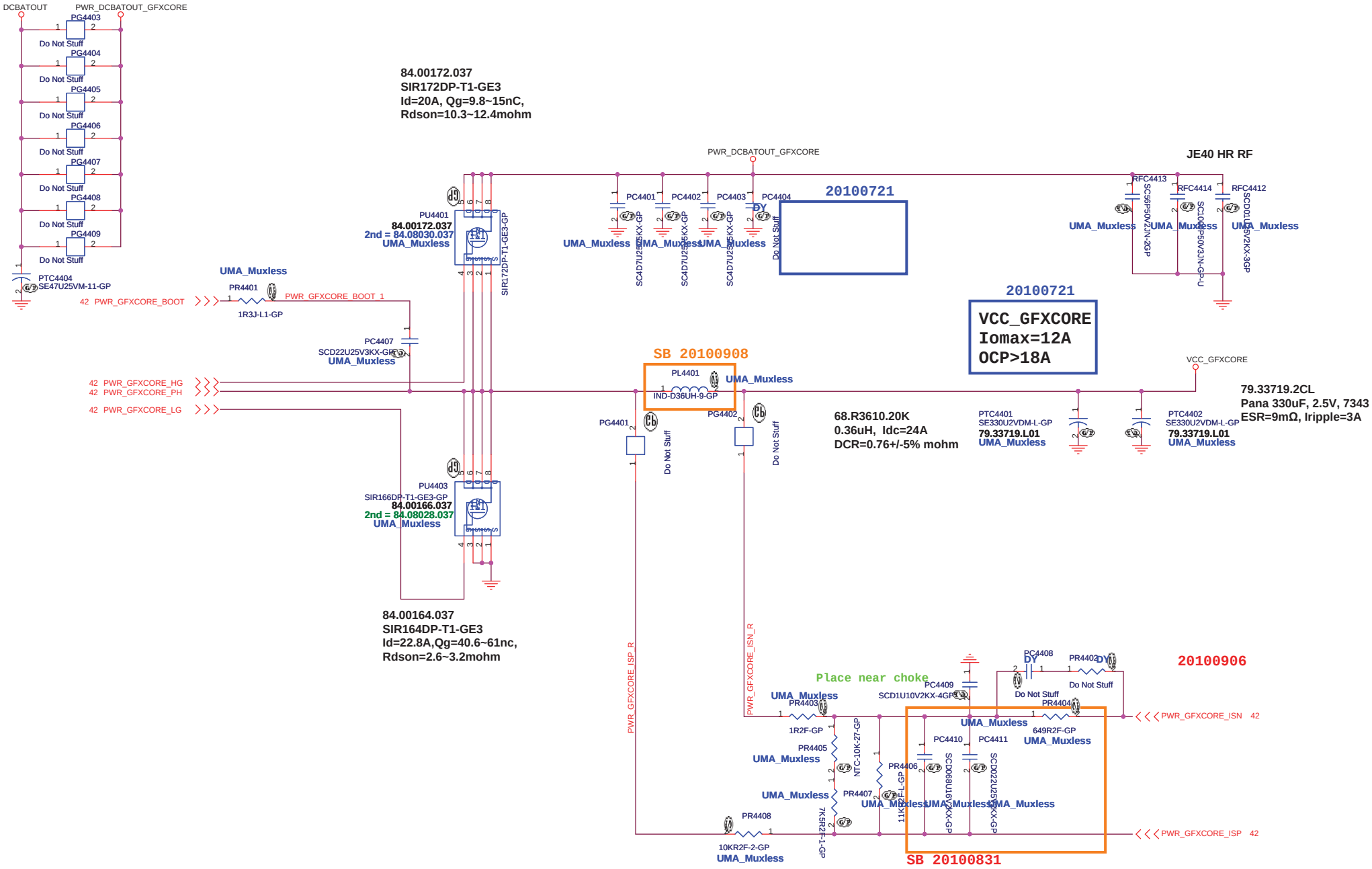
Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 40 of 102




-1 20100921
SB 20100908
JE40 to KBC?
Close to CPU
-1M
NTC place near high side MOSFET of Phase1
Parallel
JE40 to TP?
SB
20100804
For Discrete only,
UMA need to DUMMY
Place near high side MOSFET of Phase1
SB 20100831
SB to -1 modify to 3K09
Place near choke of Phase1
PU4201
ISL95831HRTZ-T-GP
74.95831.A73
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Core-1(ISL95831)
JE40-HR
Thursday, December 02, 2010
http://mobilekhmha.blogspot.com/
www.vinafix.vn





HR UMA

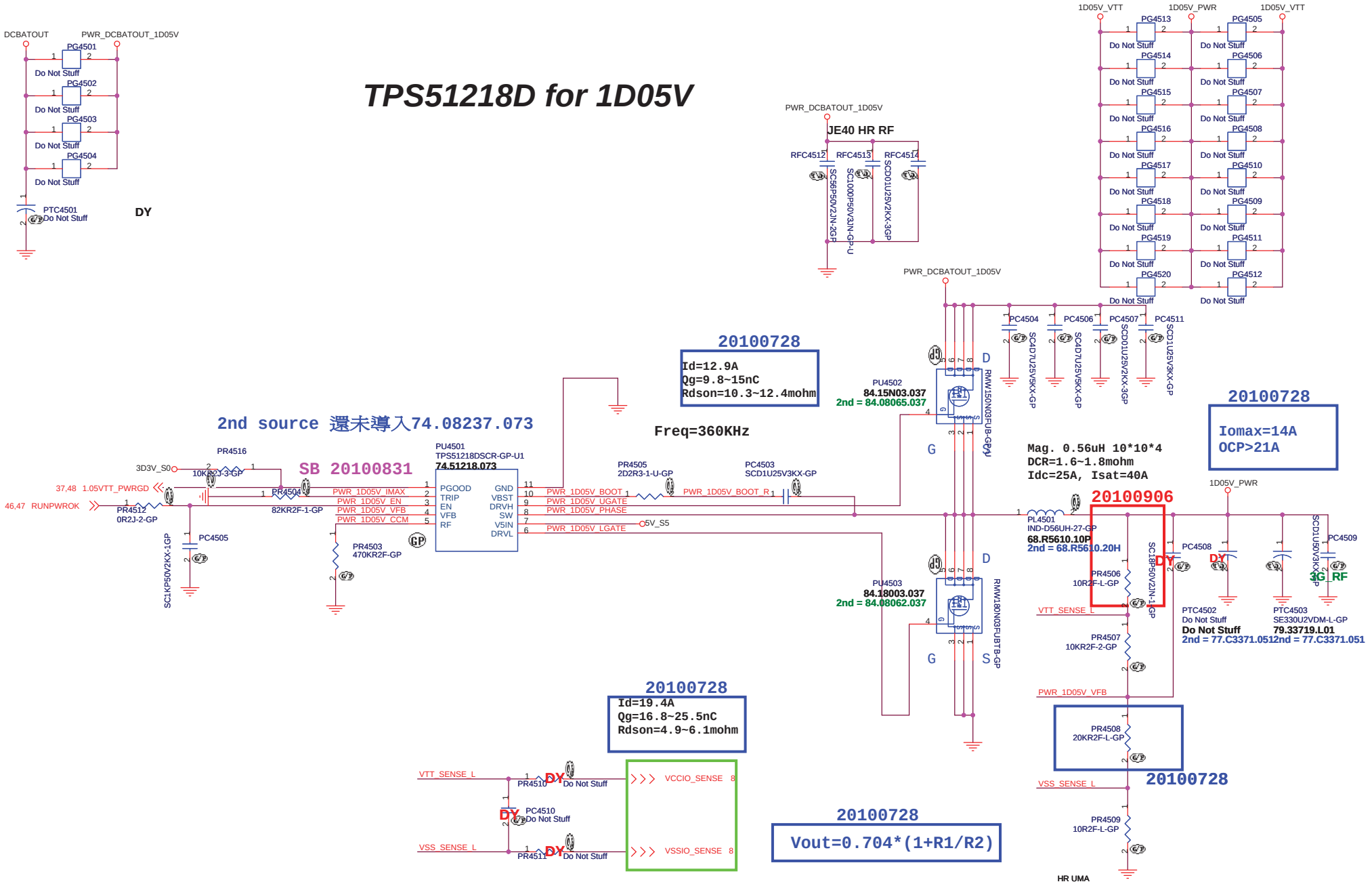
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Core-3(ISL95831)

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 44 of 102

TPS51218D for 1D05V



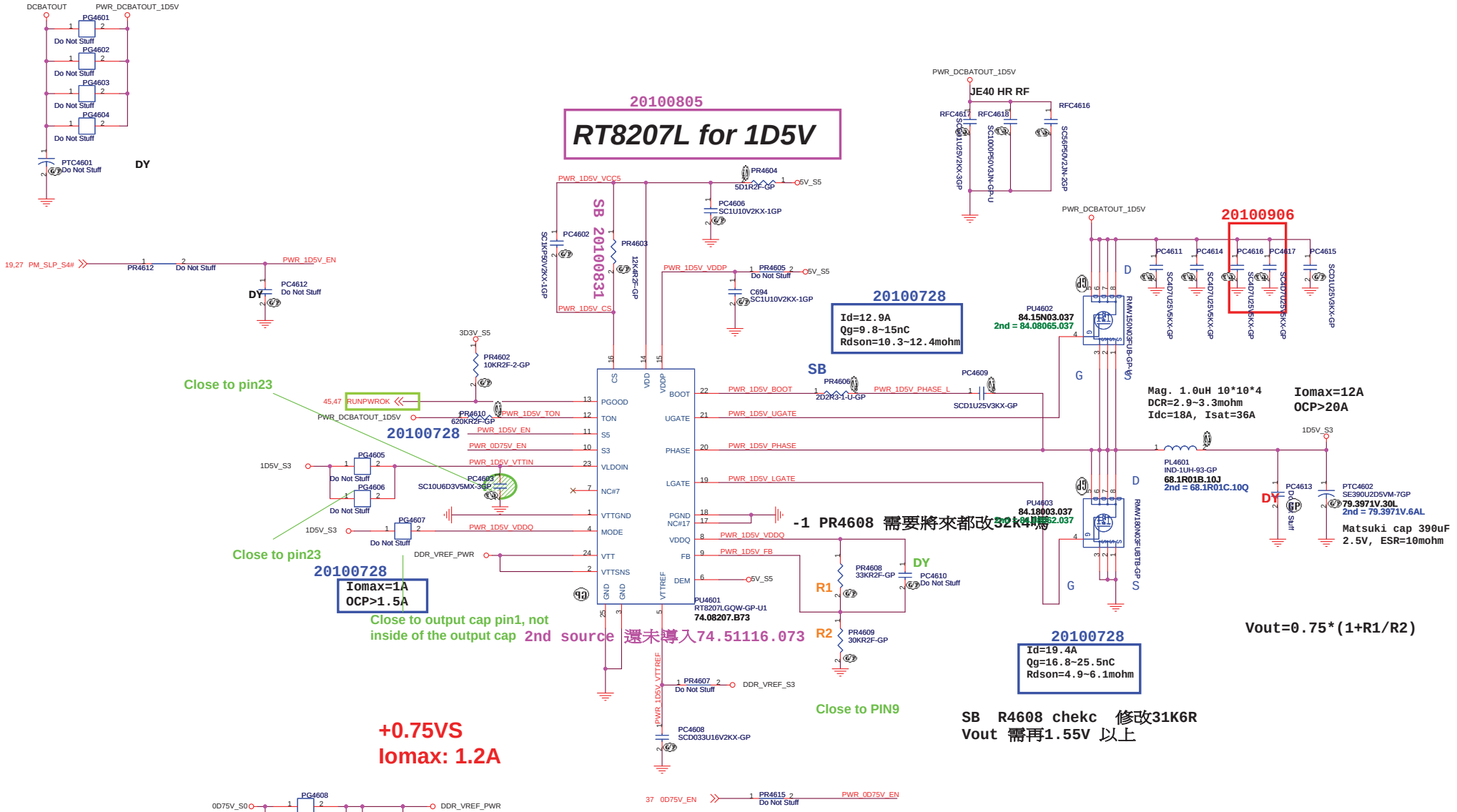
HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DC to DC 1D05V(TPS51218D)	
Size A3	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 45 of 102	

SSID = PWR.Plane.Regulator_1p5v0p75v

20100805

RT8207L for 1D5V

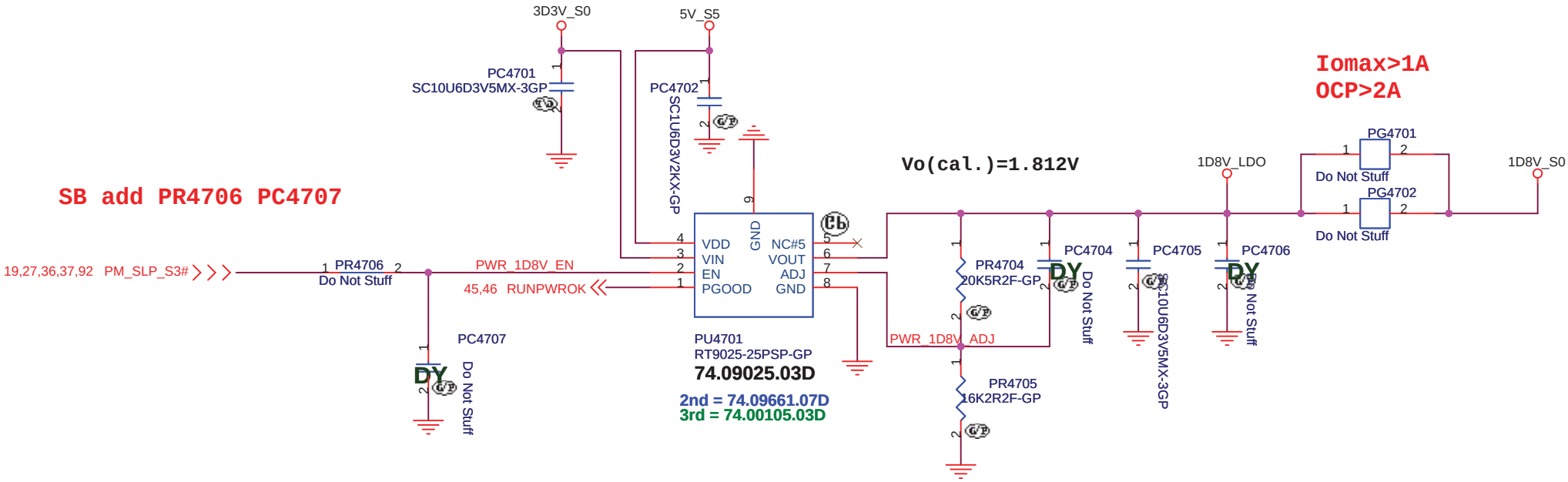


HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: TPS5111		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 46 of 102	

SSID = PWR.Plane.Regulator_1p8v

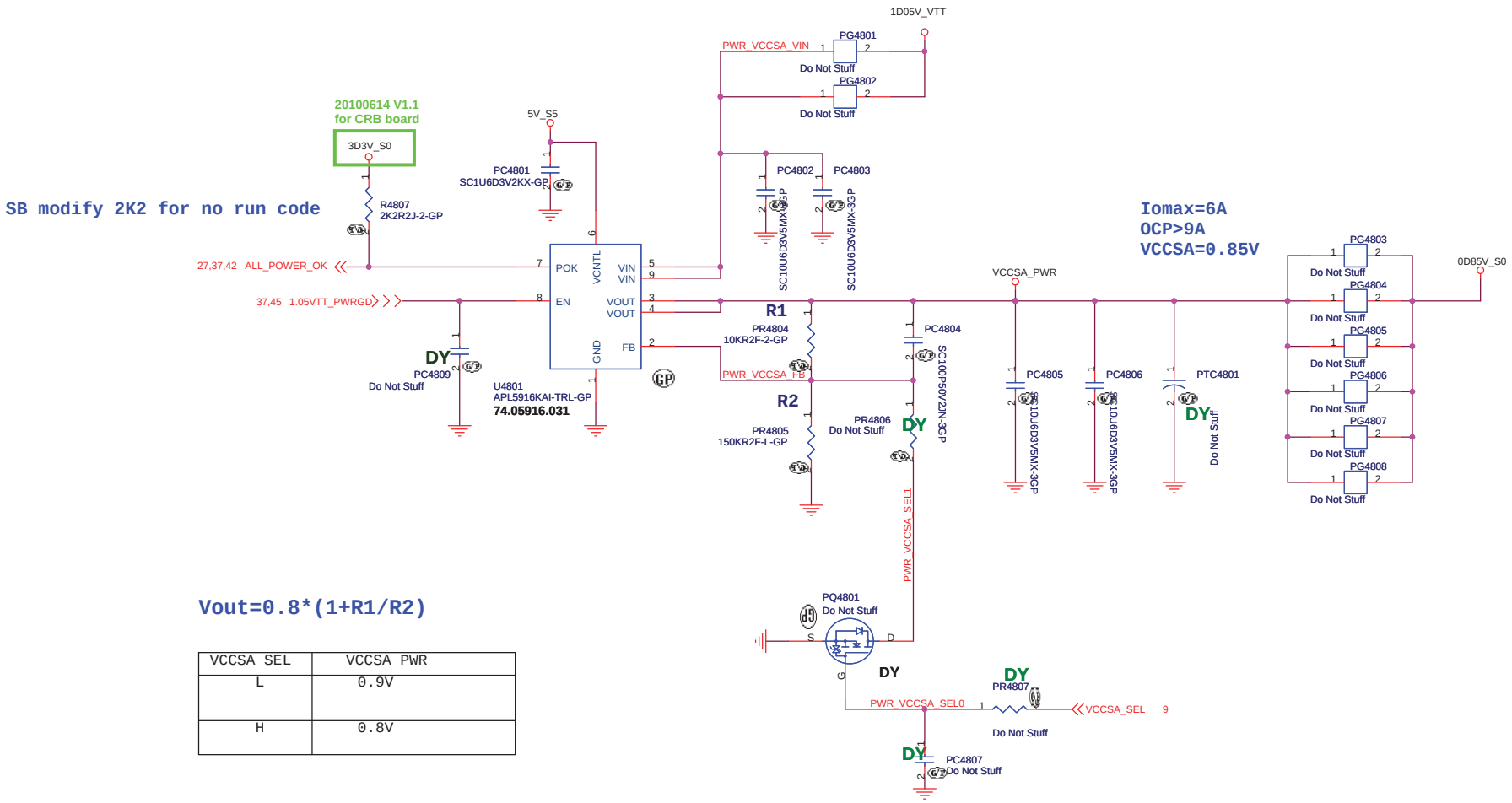
RT9025 for 1D8V_S0



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *LDO_1D8V(RT9025)*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 47 of 102	

APL5916 for VCCSA



Vout=0.8*(1+R1/R2)

VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

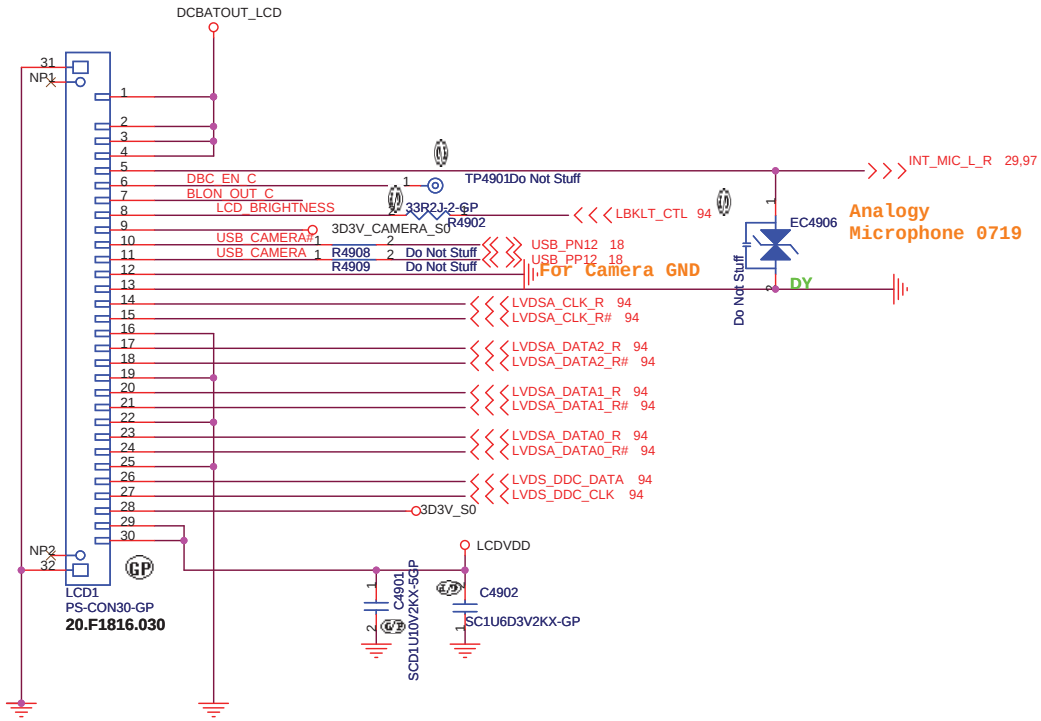
Title: LDO VCCSA(APL5916)

Size	Document Number	Rev
A3	JE40-HR	-1

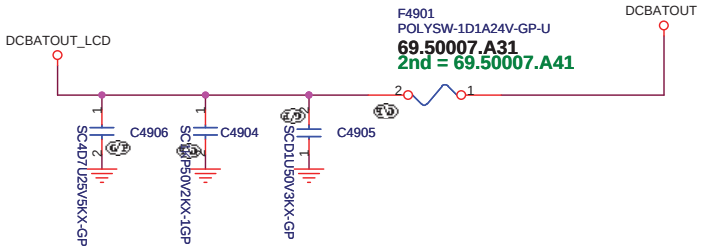
Date: Thursday, December 02, 2010 Sheet 48 of 102

SSID = VIDEO

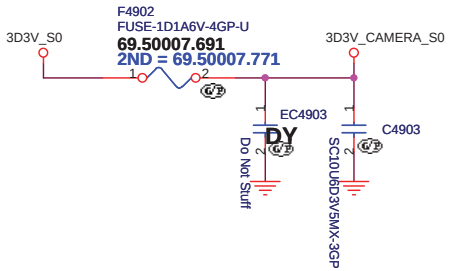
LVDS CONNECTOR



INVERTER POWER

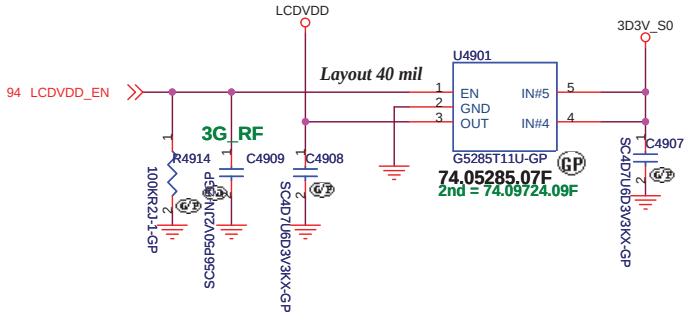


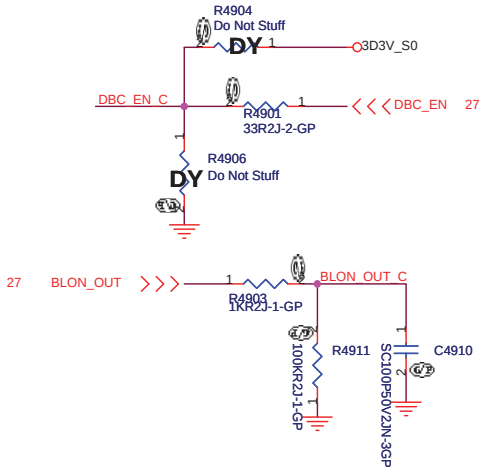
Camera Power



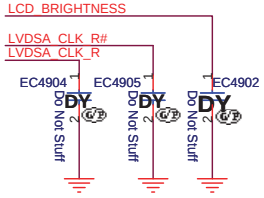
SSID = VIDEO

LCD POWER for ANNIE





For EMI request
Close to LVDS connector



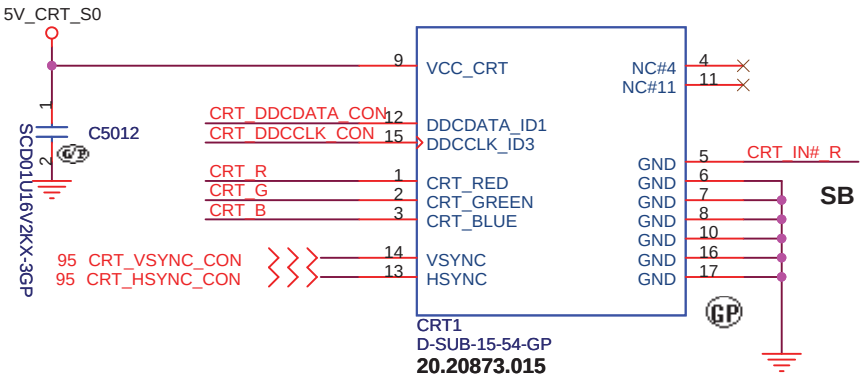
HR UMA

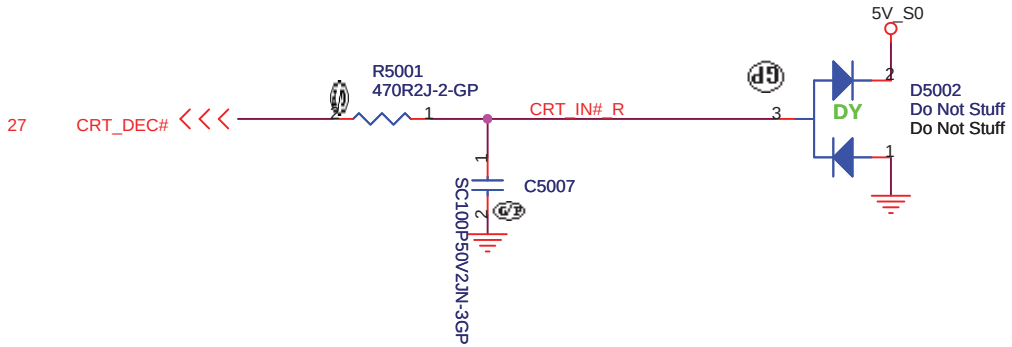
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

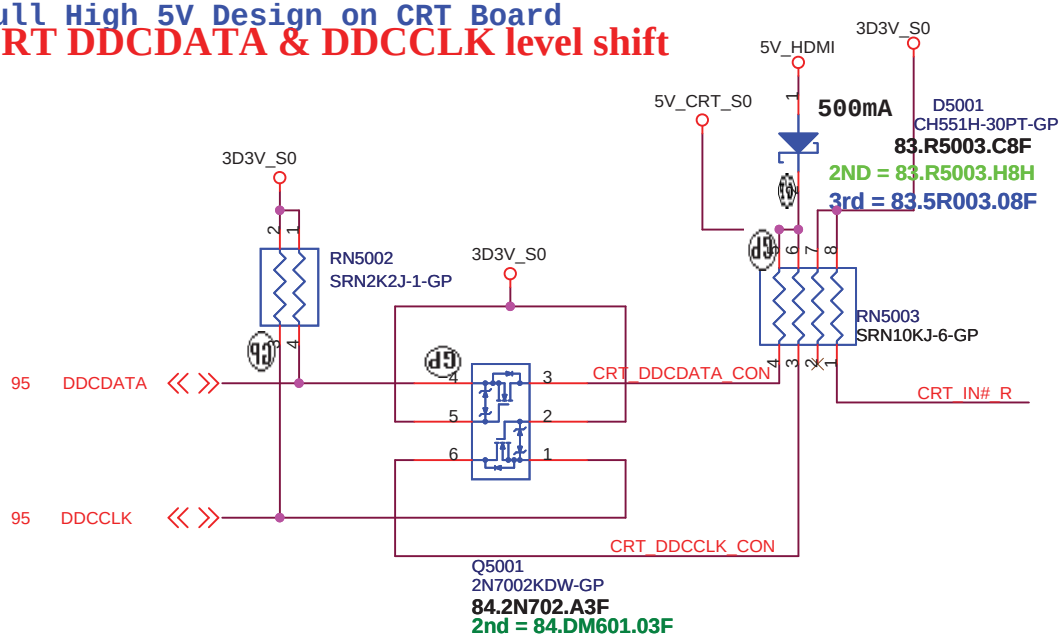
Title	LCD Connector	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 49 of 102	

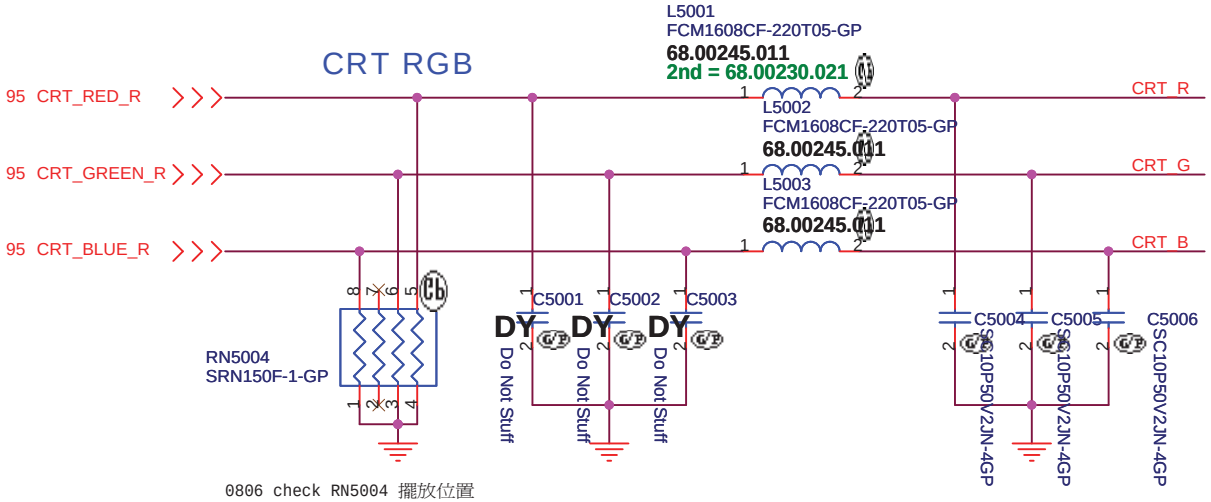
Pull High 5V Design on CRT Board

CRT DDCDATA & DDCCLK level shift

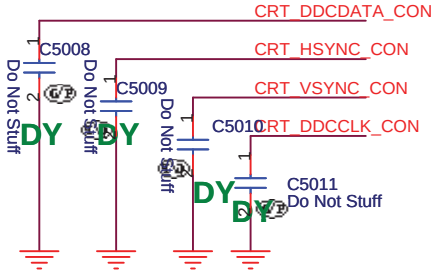








0806 check RN5004 擺放位置



HR UMA

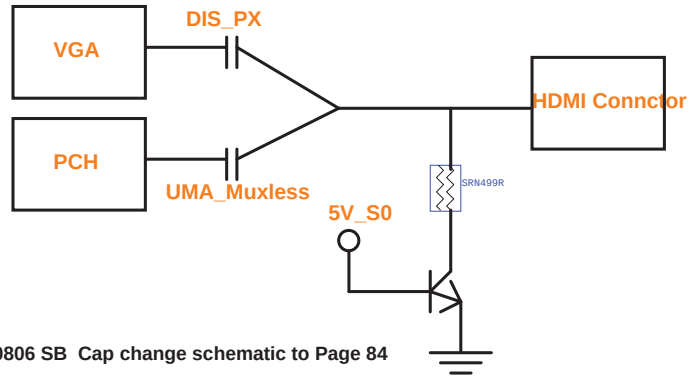
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **CRT Connector**		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 50 of 102	

SSID = VIDEO

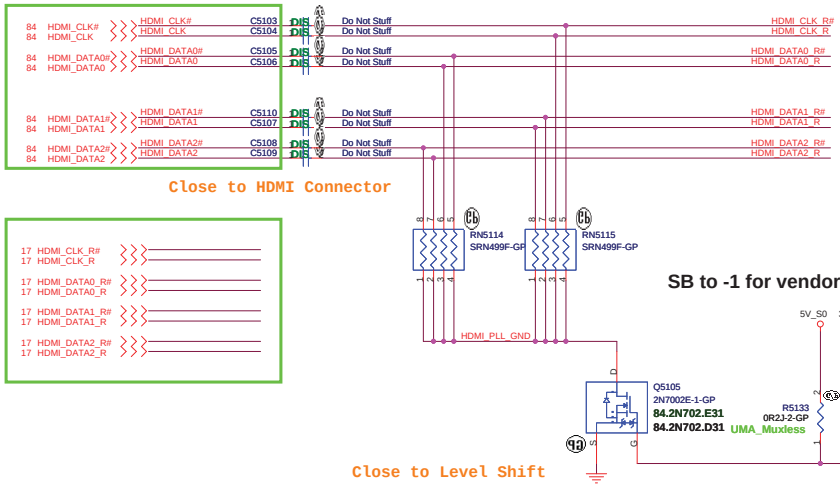
HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resister

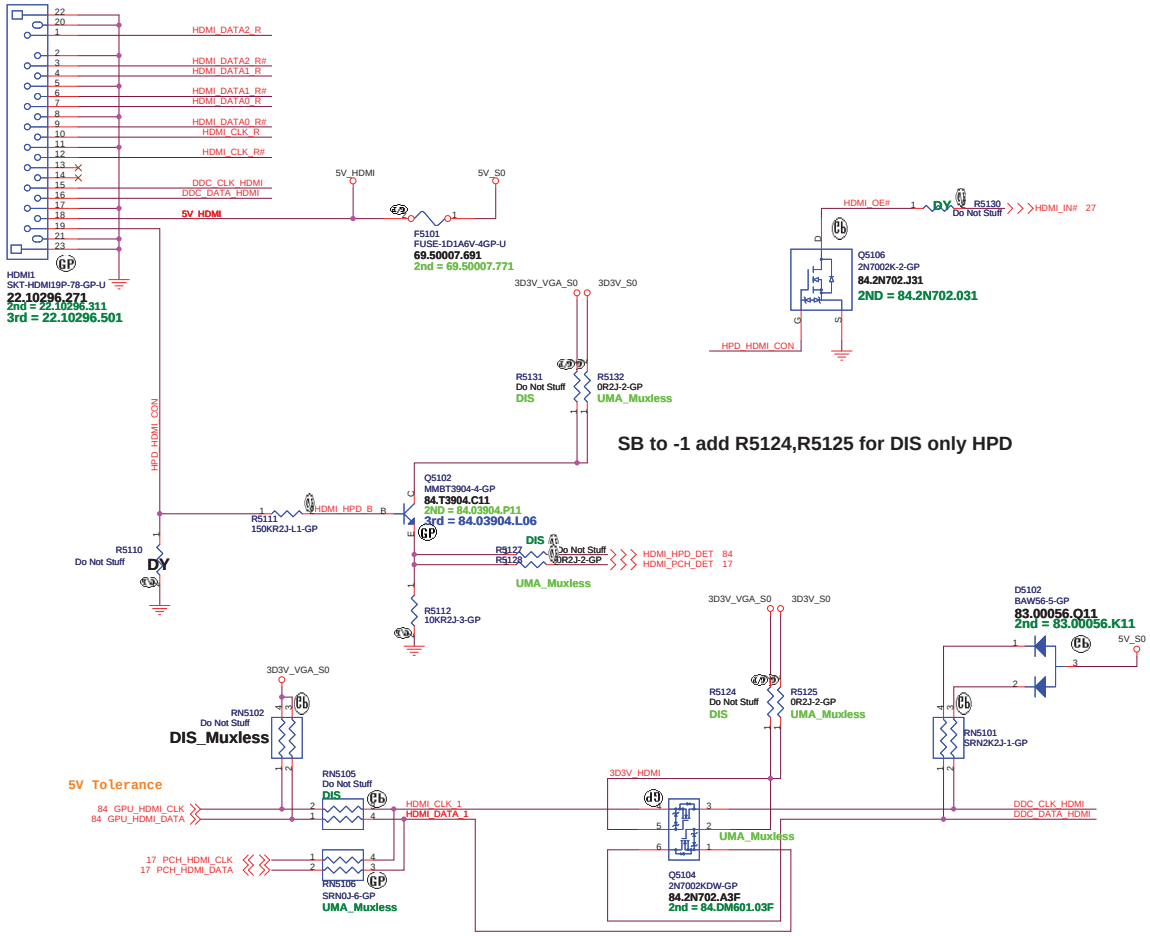
HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84



HDMI CONN



HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector

Size	Document Number	Rev
Custom	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 51 of 102

LED BACKLIGHT CONVERTER POWER

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *eDP*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 52 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***S-VIDEO***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 53 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

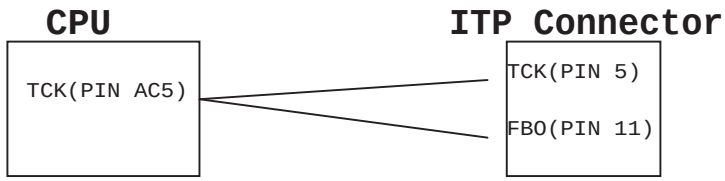
Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

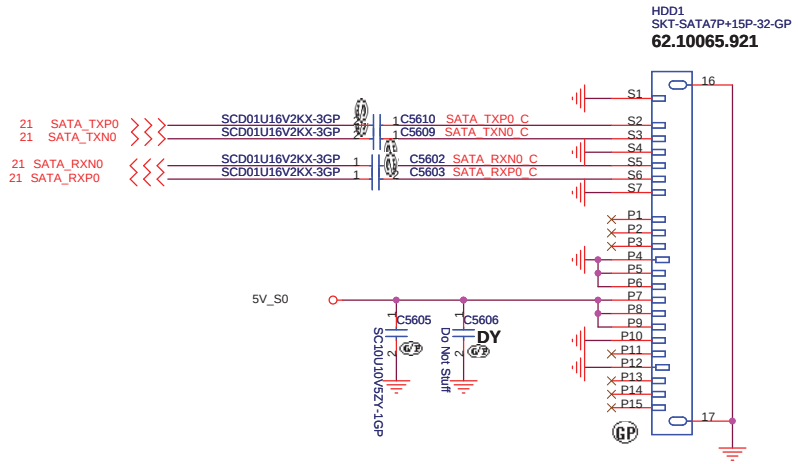


HR UMA

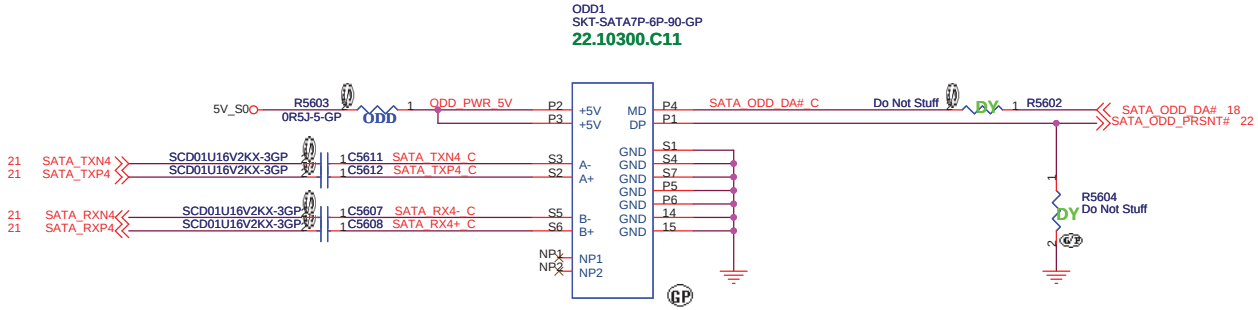
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ITP		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 55 of 102	

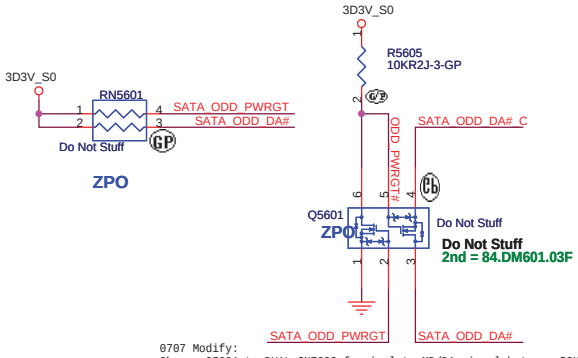
SSID = SATA

SATA HDD Connector



ODD Connector



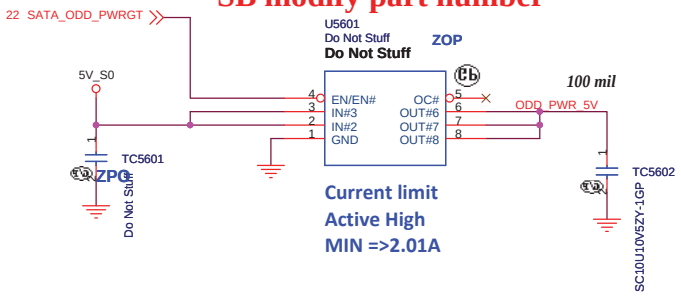


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDD/ODD		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 56 of 102	

ESATA Power

USB CHARGER

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *E-SATA/USB CHARGER*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 57 of 102

SSID = AUDIO

Speaker Connector

LINE1 OUT
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

Internal
Microphone

JE40 delete Line in function

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Jack

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 58 of 102

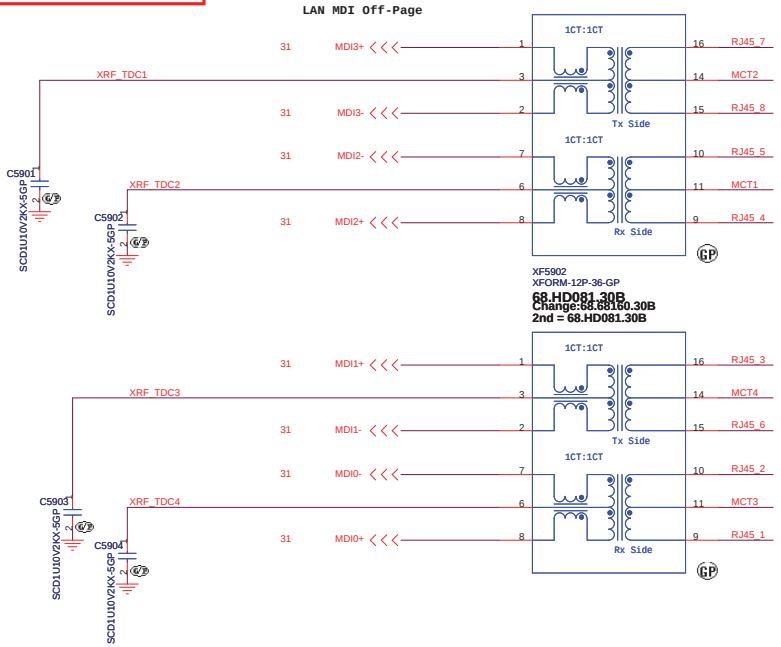
GIGA Lan Transformer

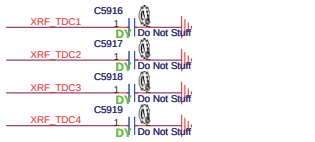
SSID = LOM

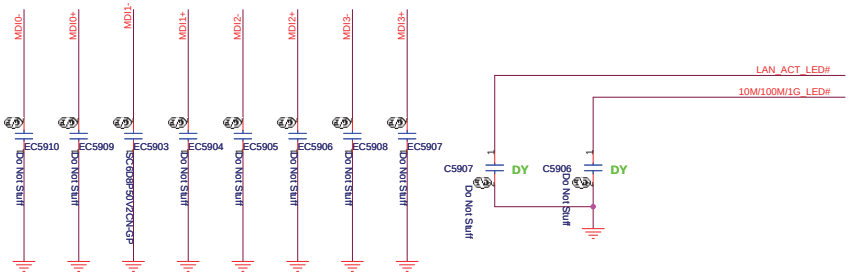
LAN MDI Off-Page

XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B

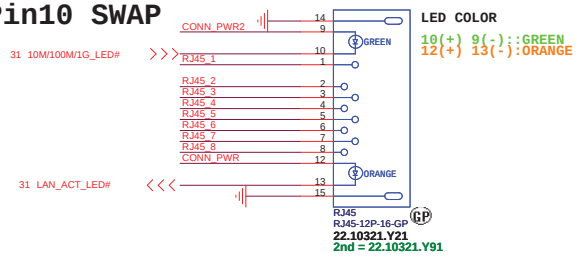
XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B



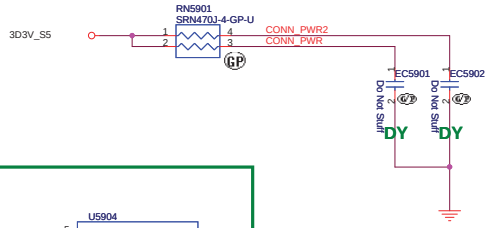




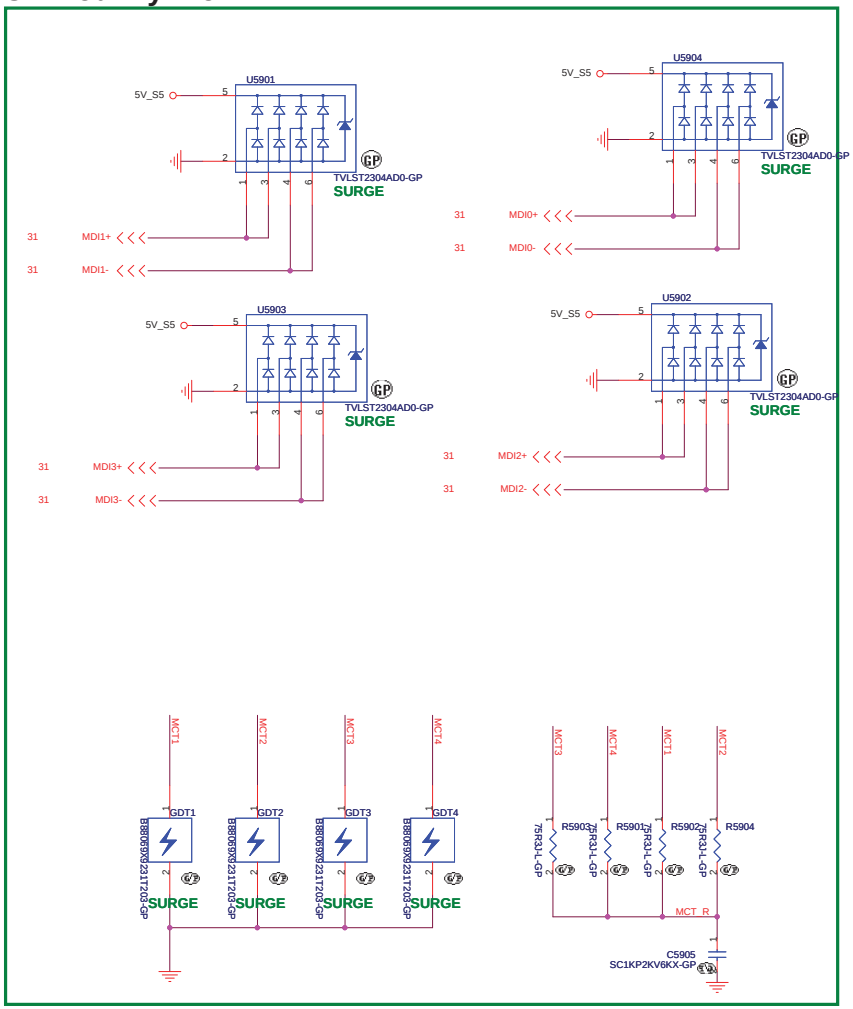
SB modiyf Pin9 Pin10 SWAP



LED COLOR
10(+) 9(-)::GREEN
12(+) 13(-):ORANGE



SB modify For EMI

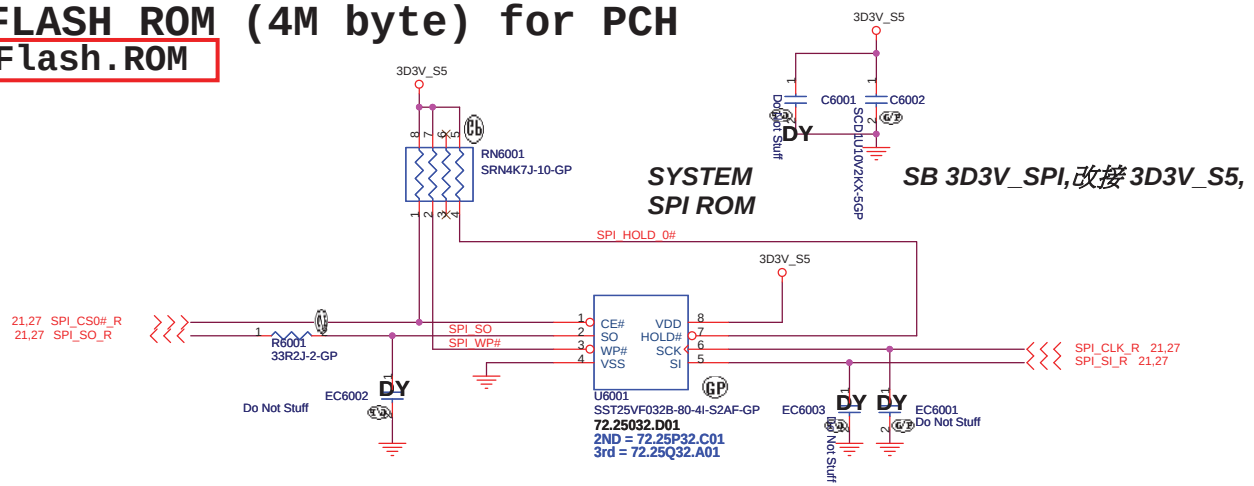


HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	LAN CONNECTOR	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 59 of 102	

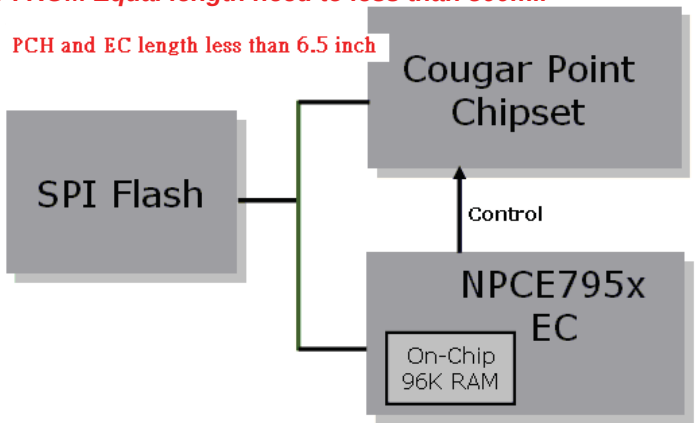
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

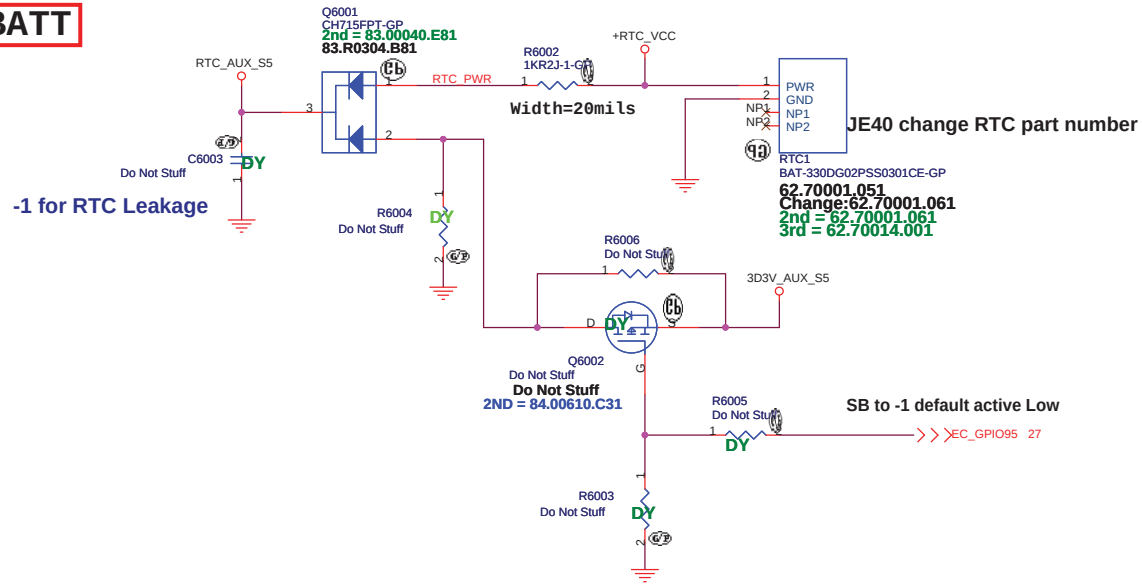


SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



SSID = RBATT

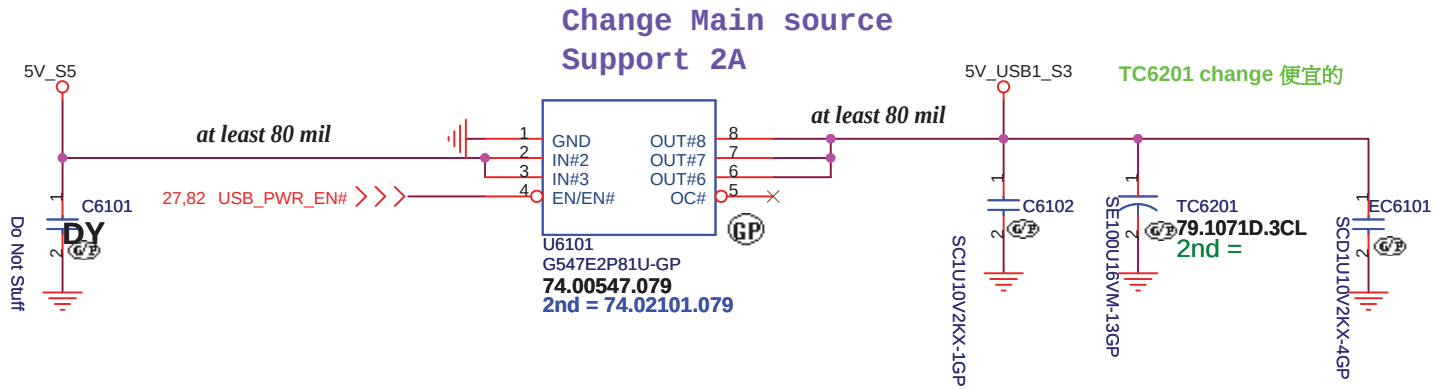


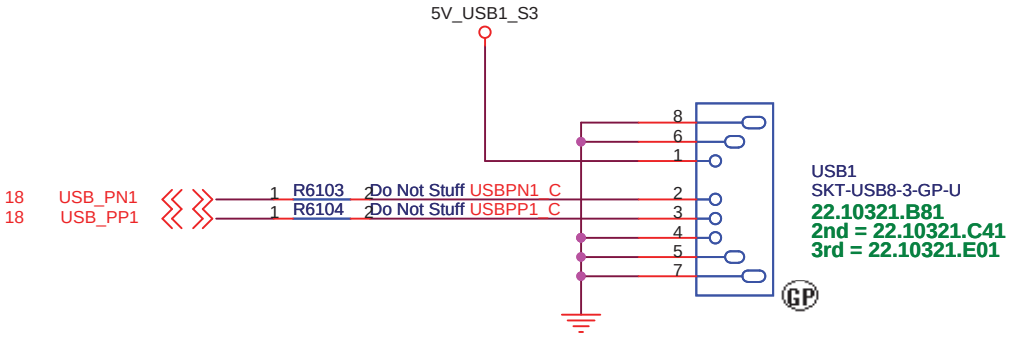
HR UMA

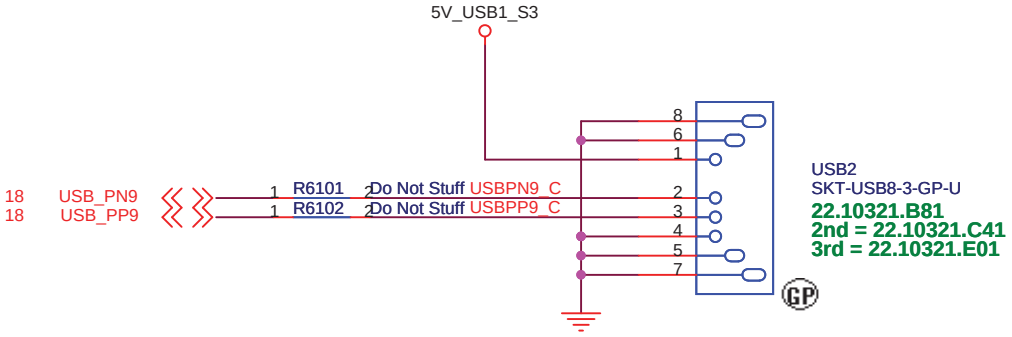
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *Flash/RTC*		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 60 of 102	

SSID = USB

IO Board USB Power







HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Power SW***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 61 of 102

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB 3.0 Port***

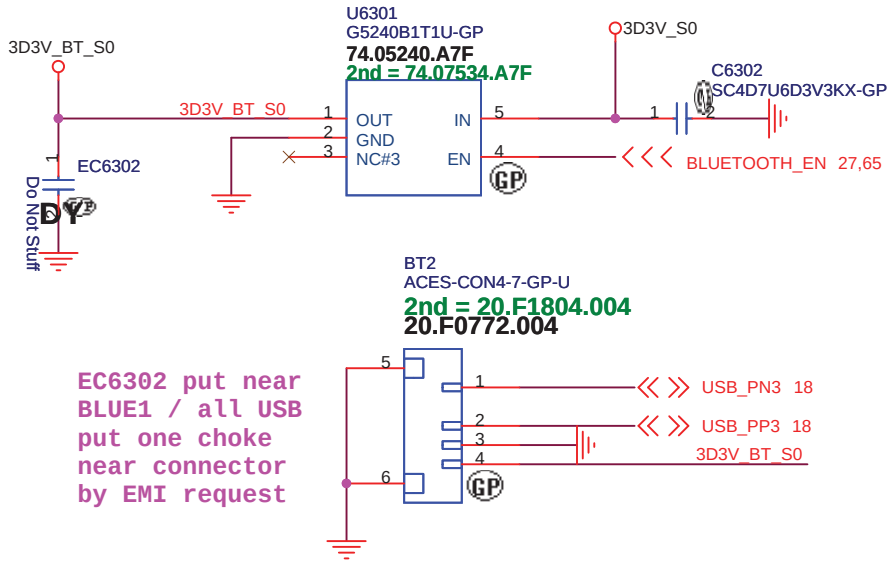
Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 62 of 102

SSID = User.Interface

Bluetooth Module conn.

ANNIE Bluetooth Module



EC6302 put near BLUE1 / all USB put one choke near connector by EMI request

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Bluetooth***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 63 of 102

Finger printer

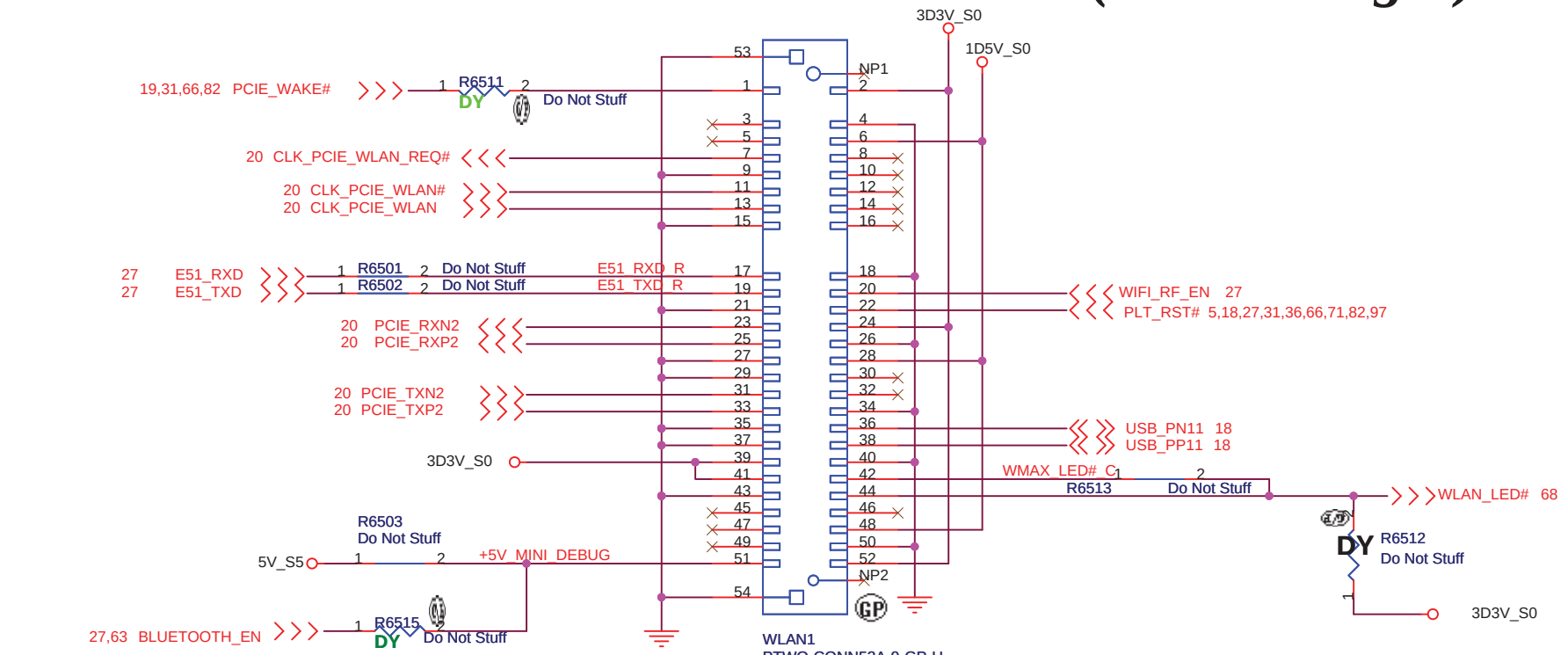
JE40 delete FP function

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ***RESERVED***		
Size: A4	Document Number: **JE40-HR**	Rev: **-1**
Date: Thursday, December 02, 2010	Sheet 64 of 102	

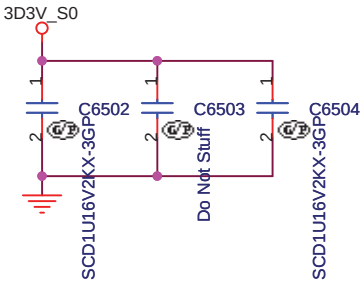
SSID = Wireless

Mini Card Connector(802.11a/b/g/n)

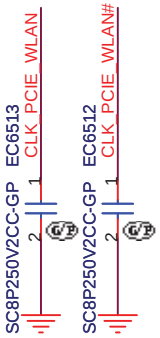


20.F1519.052

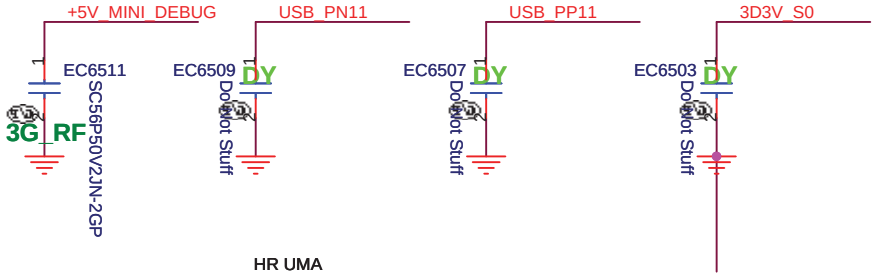
2nd = 62.10043.A51
3rd = 20.F1693.052
4th = 20.F1743.052



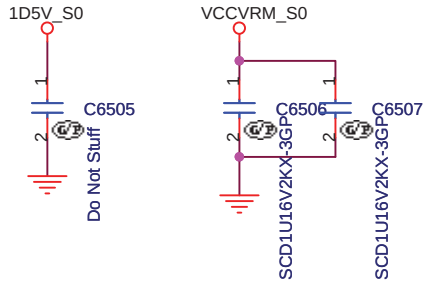
SB modify for SIV



RF suggestion



-2



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***MINICARD(WLAN)/ITP CONN***

Size	Document Number	Rev
A4	JE40-HR	-1

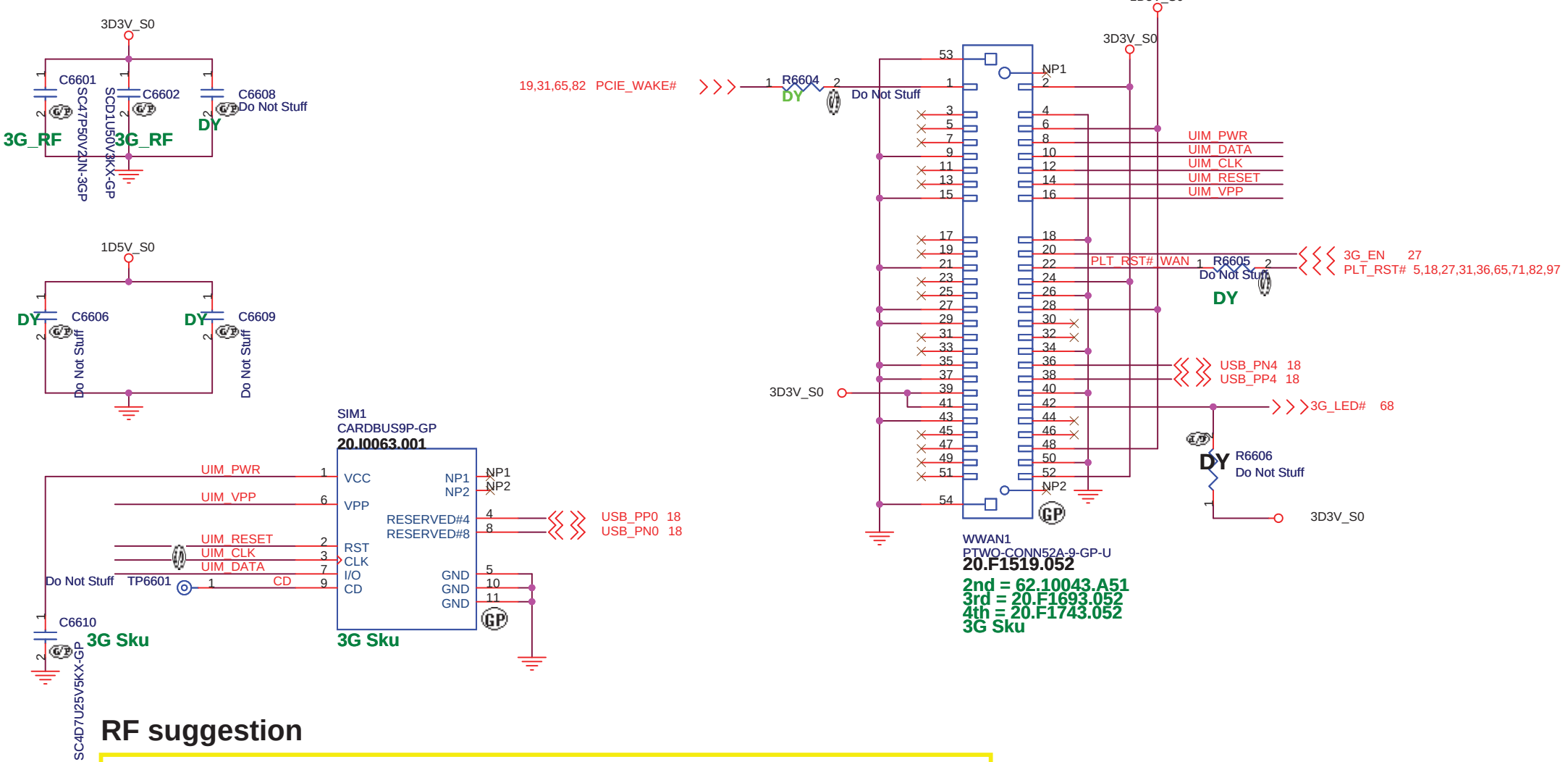
Date: Thursday, December 02, 2010 Sheet 65 of 102

SSID = Wireless

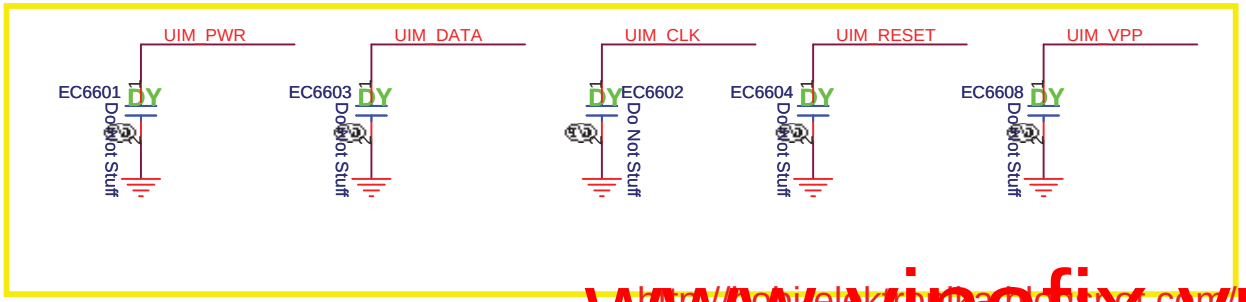
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **WWAN Connector**		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 66 of 102	

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

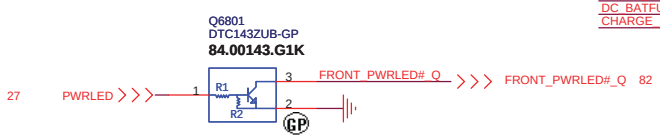
Title: ***Reserved***

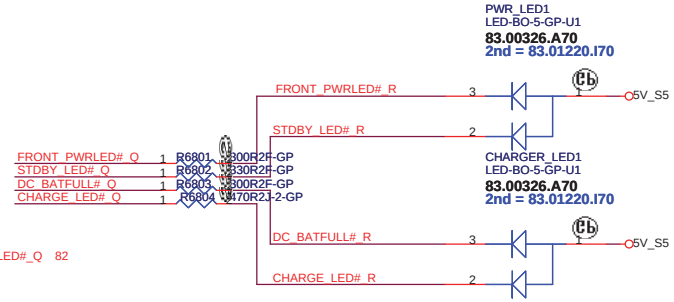
Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 67 of 102

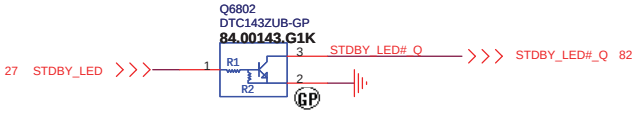
SSID = User.Interface

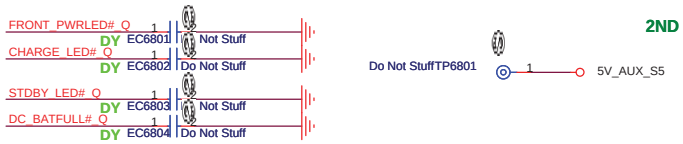
Power button LED



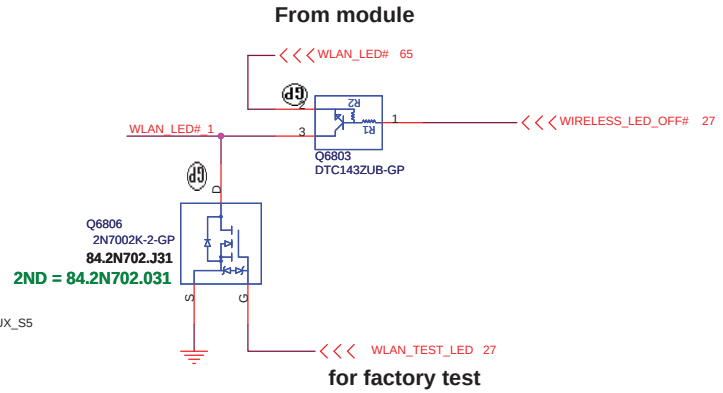


Power STDBY_LED

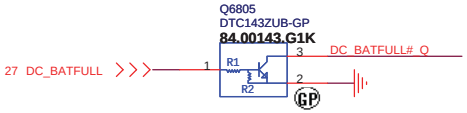




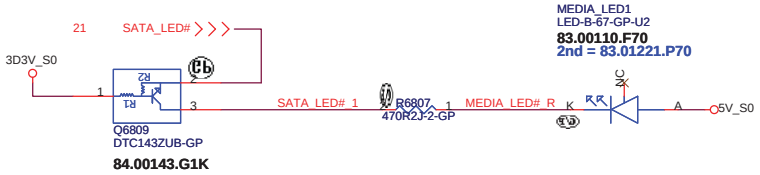
WLAN_LED



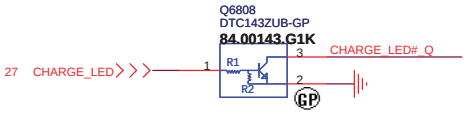
Battery LED2(DC_BATFULL)

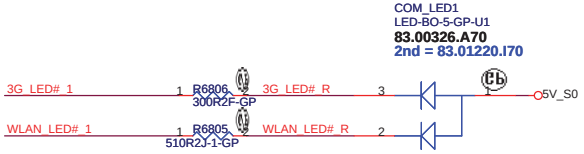


SATA HDD LED

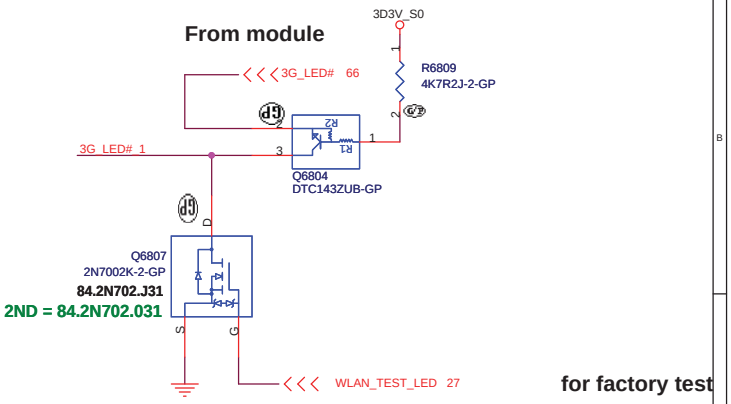


Battery LED1(CHARGE)





3G LED



HR UMA

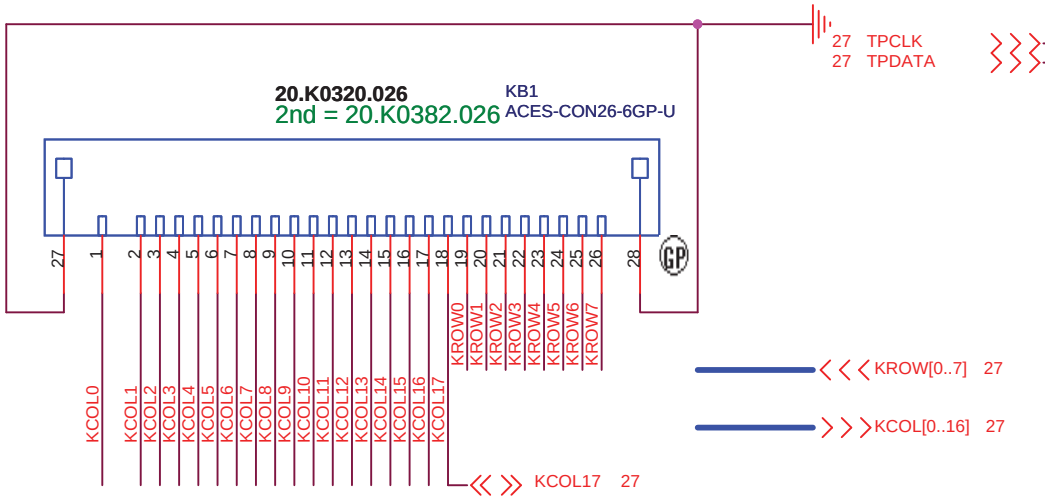
緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LED Bard/Power Button		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 68 of 102	

SSID = KBC

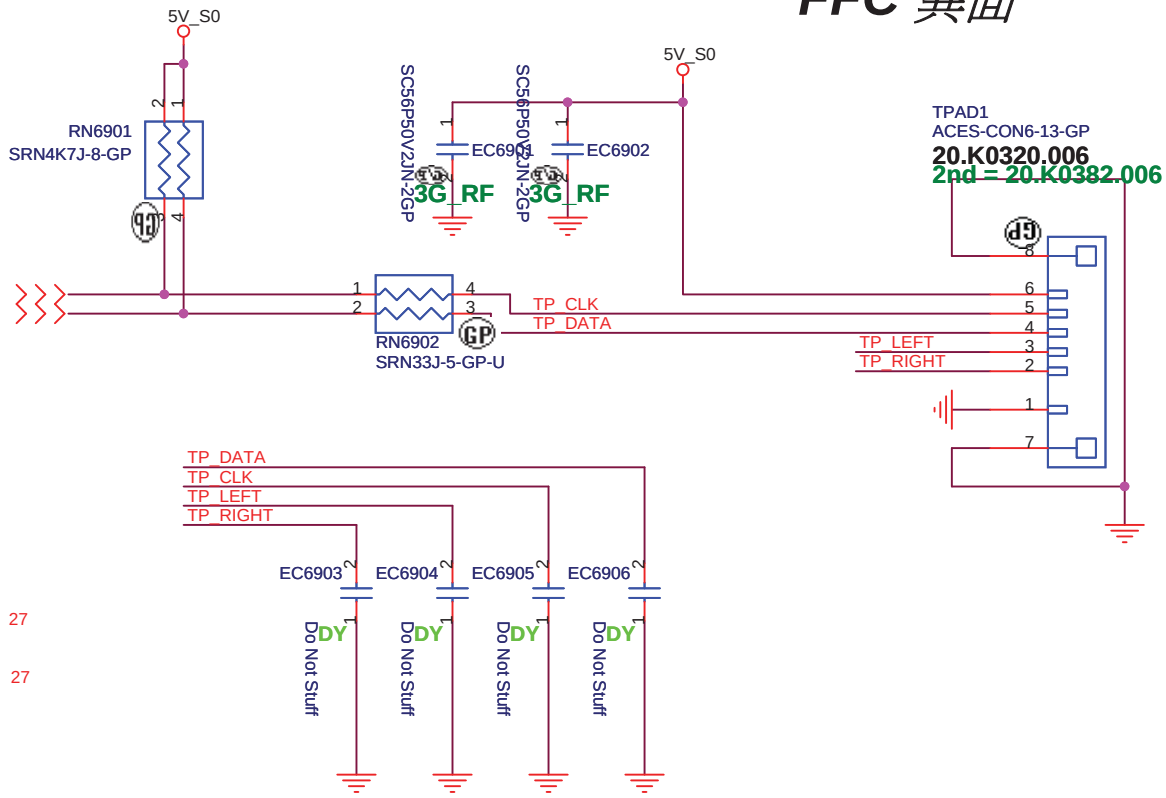
TOUCH PAD

FFC 異面

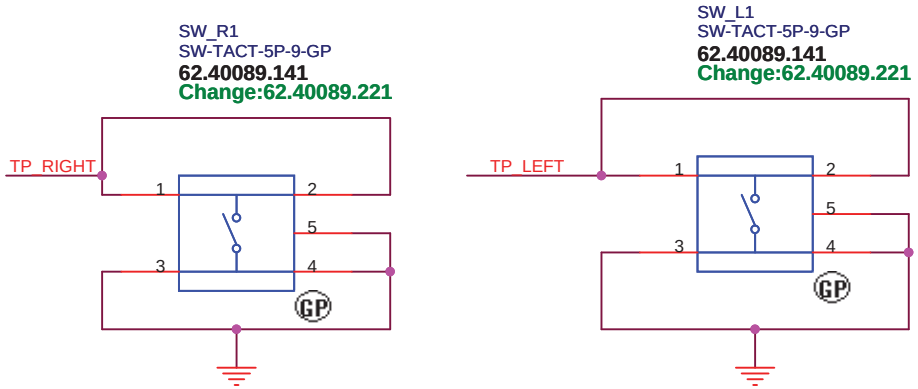
Internal KeyBoard Connector



MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

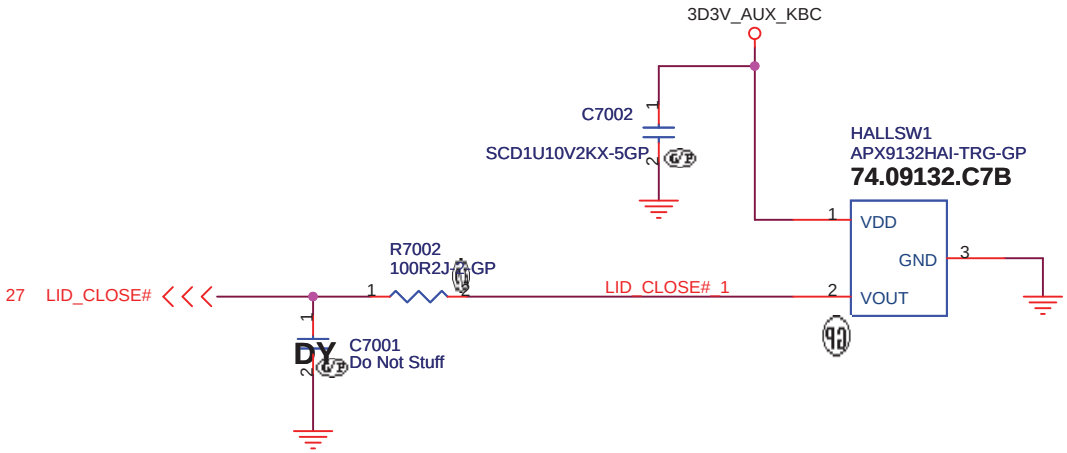


26 K/B 1 **SB to -1 modify Part number**



HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***Key Board/Touch Pad***	
Size A4	Document Number **JE40-HR**	Rev -1
Date: Thursday, December 02, 2010	Sheet 69 of 102	



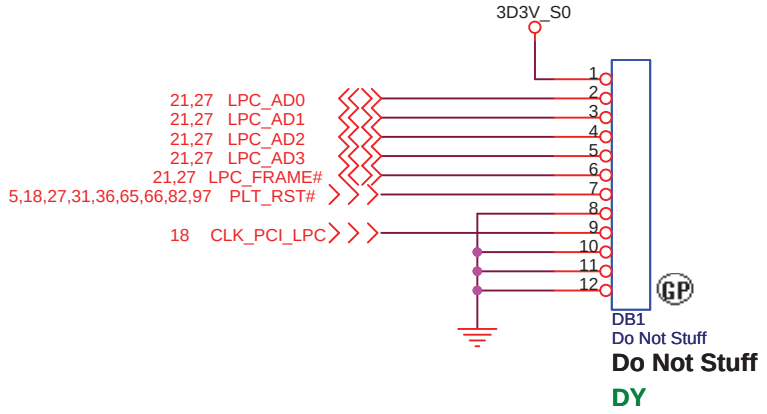
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Hall Sensor***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 70 of 102



HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Dubug connector***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 71 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 72 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

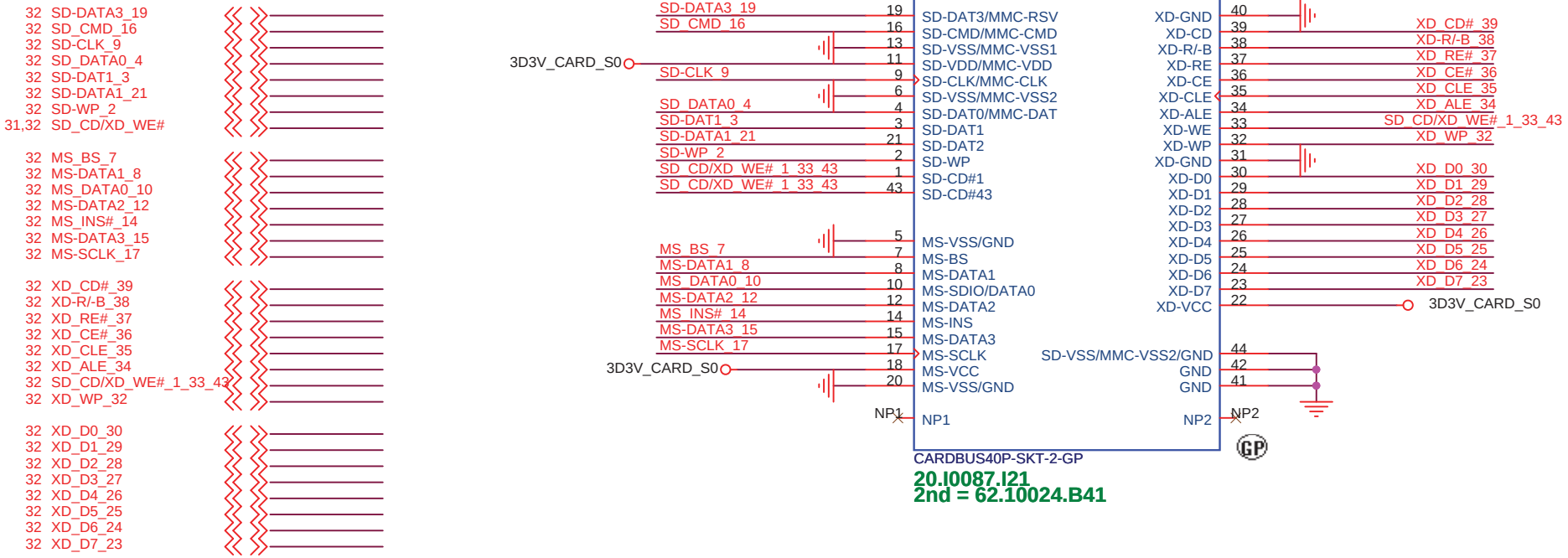
Title: *Reserved*

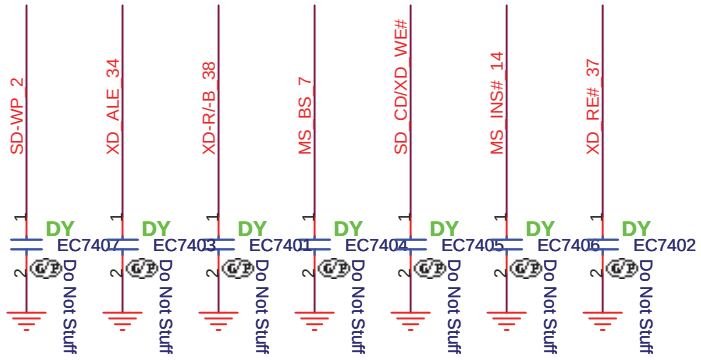
Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 73 of 102

SD/XD/MS Card Reader

SSID = SDIO





HR UMA

綽創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARD Reader CONN**

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 74 of 102

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: New Card

Size	Document Number	Rev
A3	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 75 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 76 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 77 of 102

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 78 of 102

SSID = User.Interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Free Fall Sensor*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 79 of 102	

(Blanking)

HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

Date: Thursday, December 02, 2010 Sheet 80 of 102

(Blanking)

HR UMA

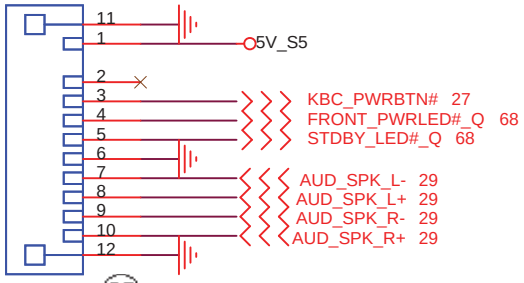
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	JE40-HR	-1

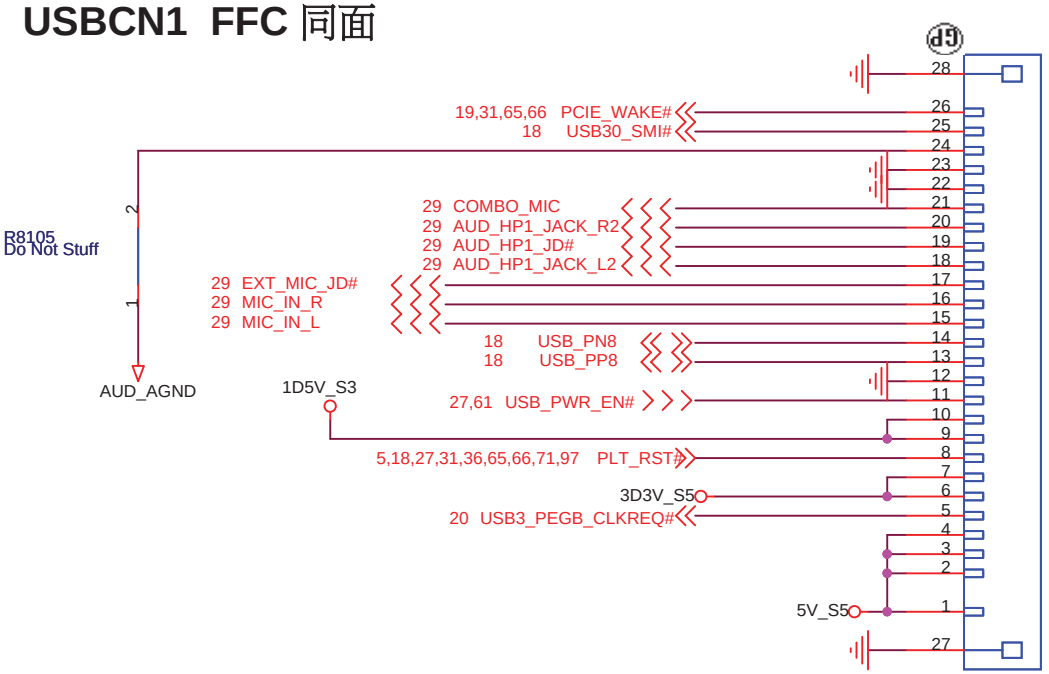
Date: Thursday, December 02, 2010 Sheet 81 of 102

PWRCN1 FFC 異面



PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010

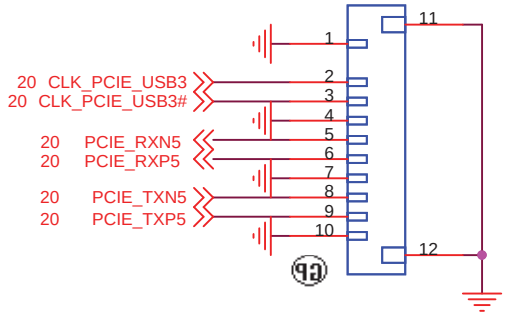
USBCN1 FFC 同面



USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026

0806 change 10Pin

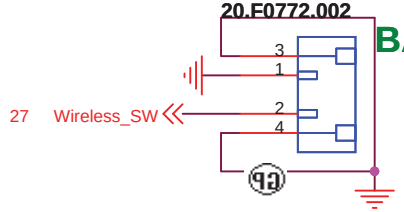
USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010



USBCN2 FFC 同面

-1 add RF connector
BAE40 Only

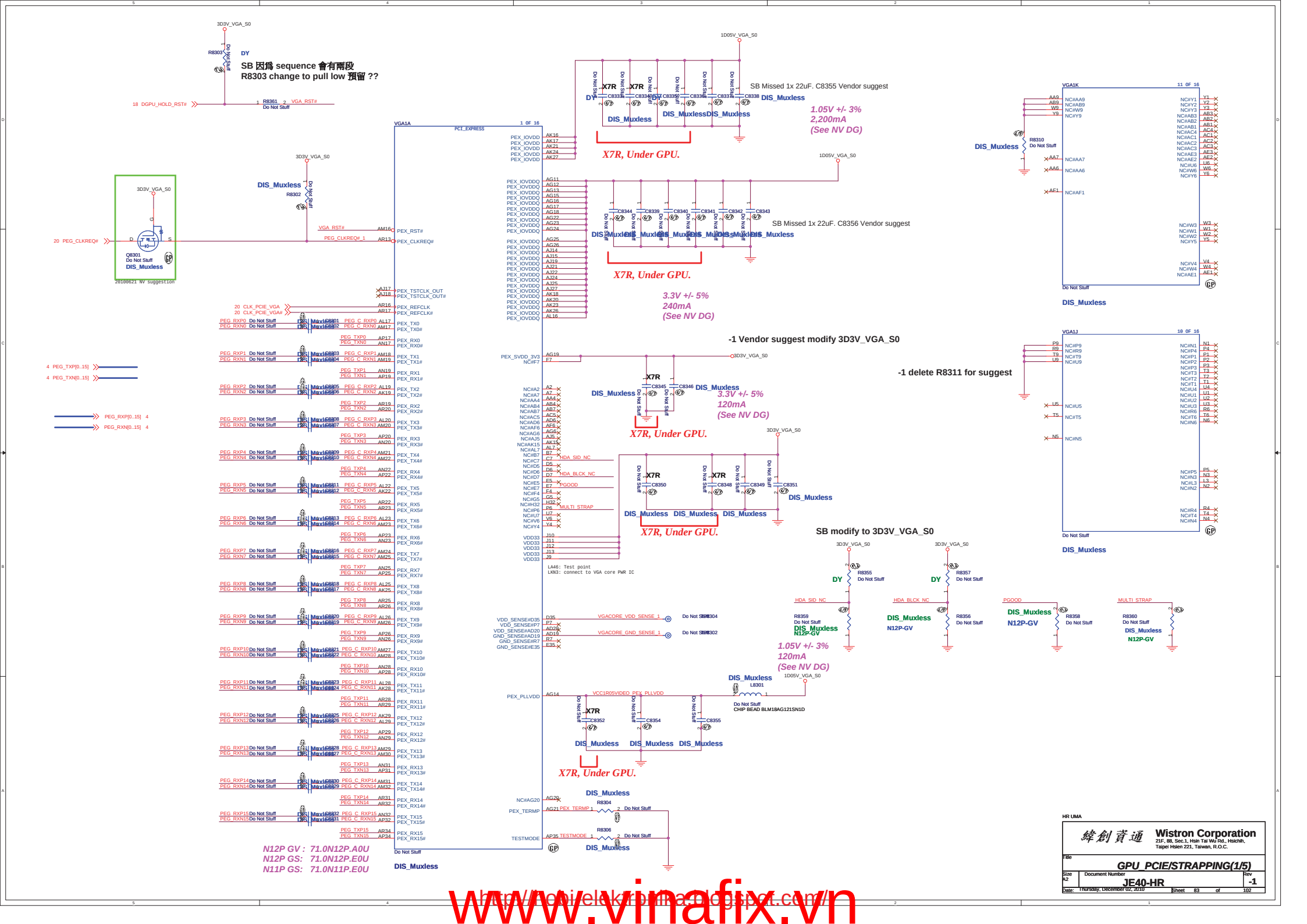
RF_CN1
ACES-CON2-11-GP
20.F0772.002
BAE40



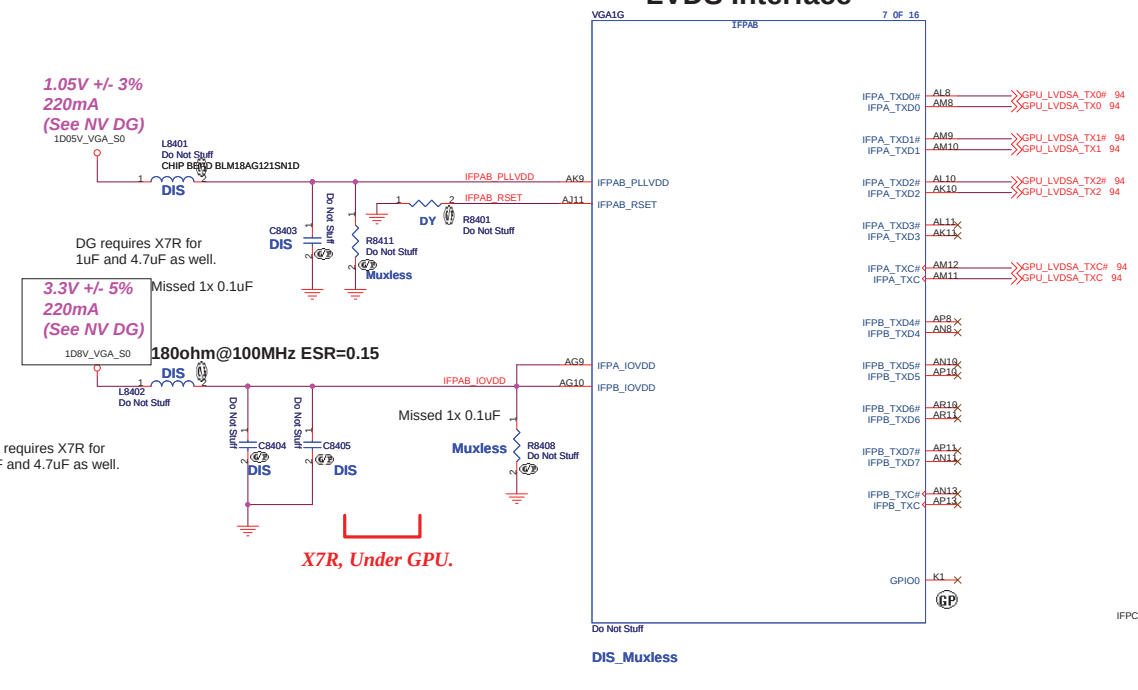
Cabele Wire to BD

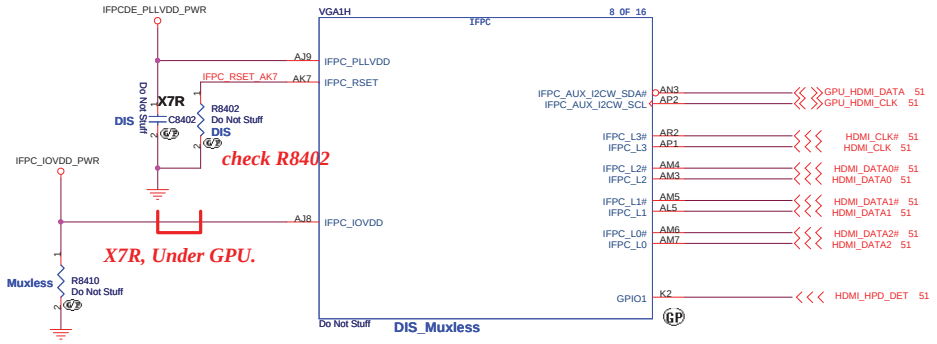
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *IO Board Connector*		
Size: A4	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 82 of 102	

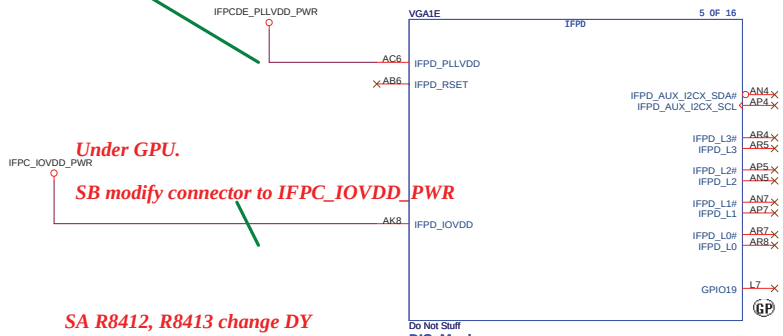


LVDS Interface

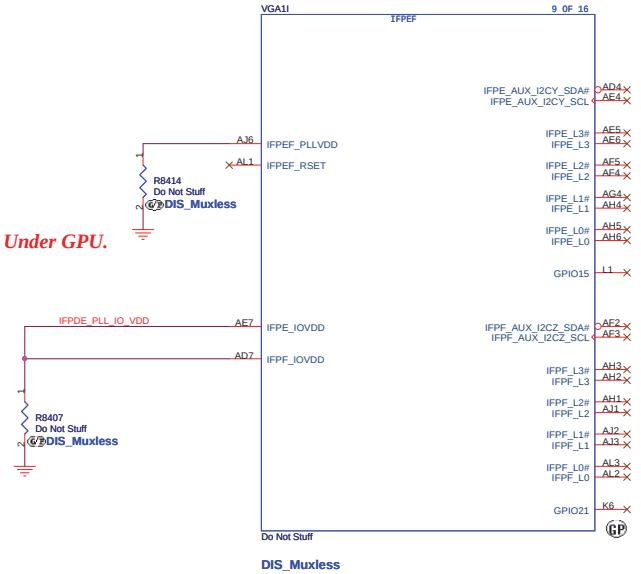




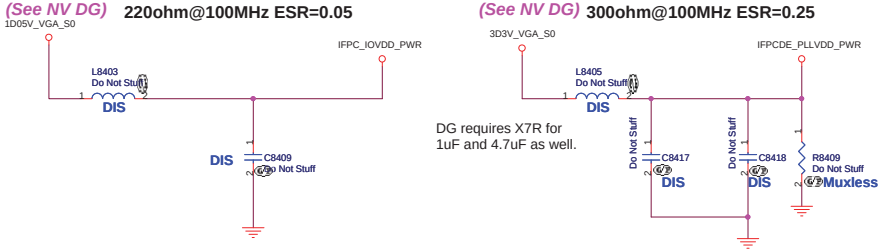
SB modify connector to IFPCDE_PLLVDD_PWR



SA R8412, R8413 change DY
SB R8412, R8413 change delete



HDMI Interface



HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: GPU Memory(2/5)		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 84 of 102	

EDP 10A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz

X7R, Under GPU.

X7R, Near GPU.

1.05V +/- 3%
200mA
(See NV DG)

X7R, Under GPU.

FBCLK Termination place on VRAM side

FBCLK Termination place on VRAM side

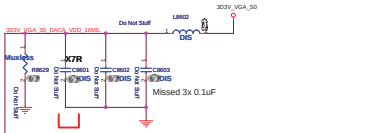
Group A

Group B

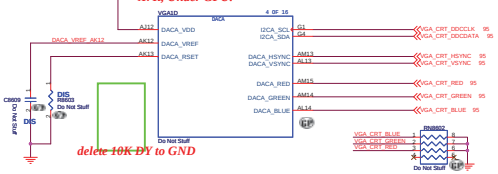
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	GPU_DP/LVDS/CRT/GPIO(3/5)
Size / Document Number / Rev	Custom / JE40-HR / -1
Date	Thursday, December 02, 2010
Sheet	85 of 102

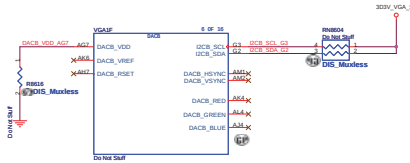
300ohm@100MHz ESR=0.25ohm

3.3V +/- 5%
120mA
(See NV DG)



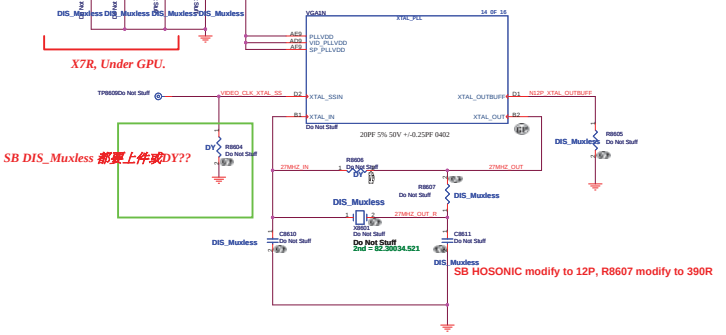
X7R, Under GPU.



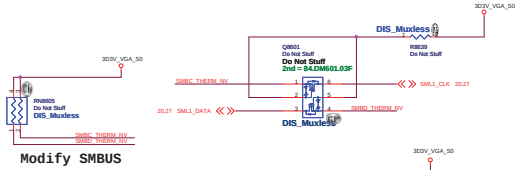


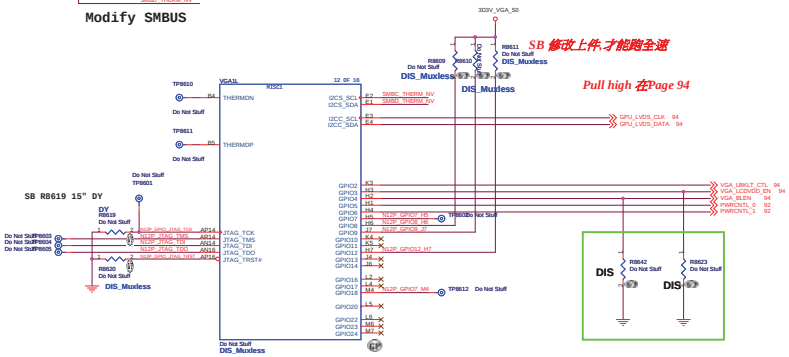
1.05V +/- 3%
150mA
(See NV DG)

X7R, Under GPU.



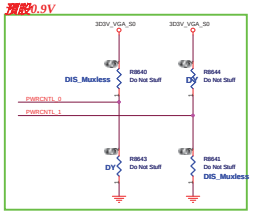
VGA Thermal sensor P2800





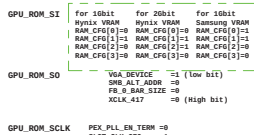
SJM50-CP SUPPORT							
P-STATE	NVVDD_ALTV1	NVVDD_ALTV0	N11M-GE1	N11M-GE2	N11M-OP1	N11P-GE1	N11P-GE Fermi
P12	0	0	0.85V	0.85V	0.85V	0.80V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.9V
P0	1	0	1.02V	1.02V	1.02V	0.95V	0.95V

預設0.9V



NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL



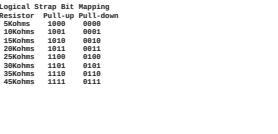
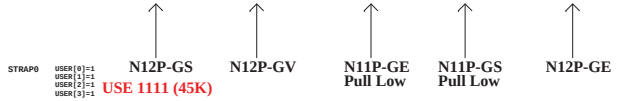
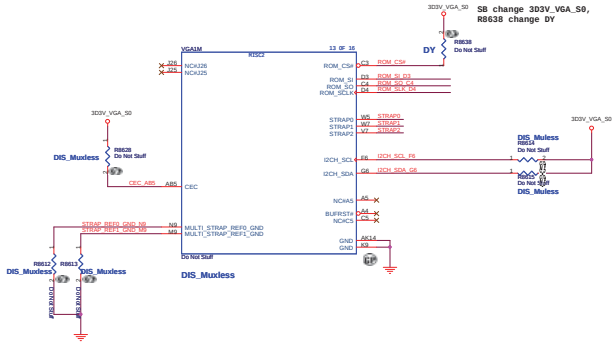


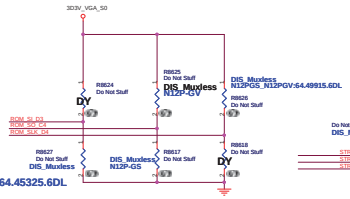
TABLE NVIDIA -1 modify N12P GV setting

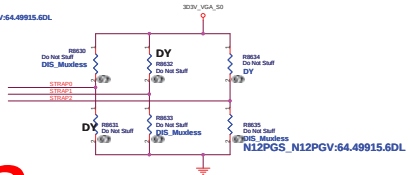
71.0N12P.E0U → 71.0N12P.A0U

	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL





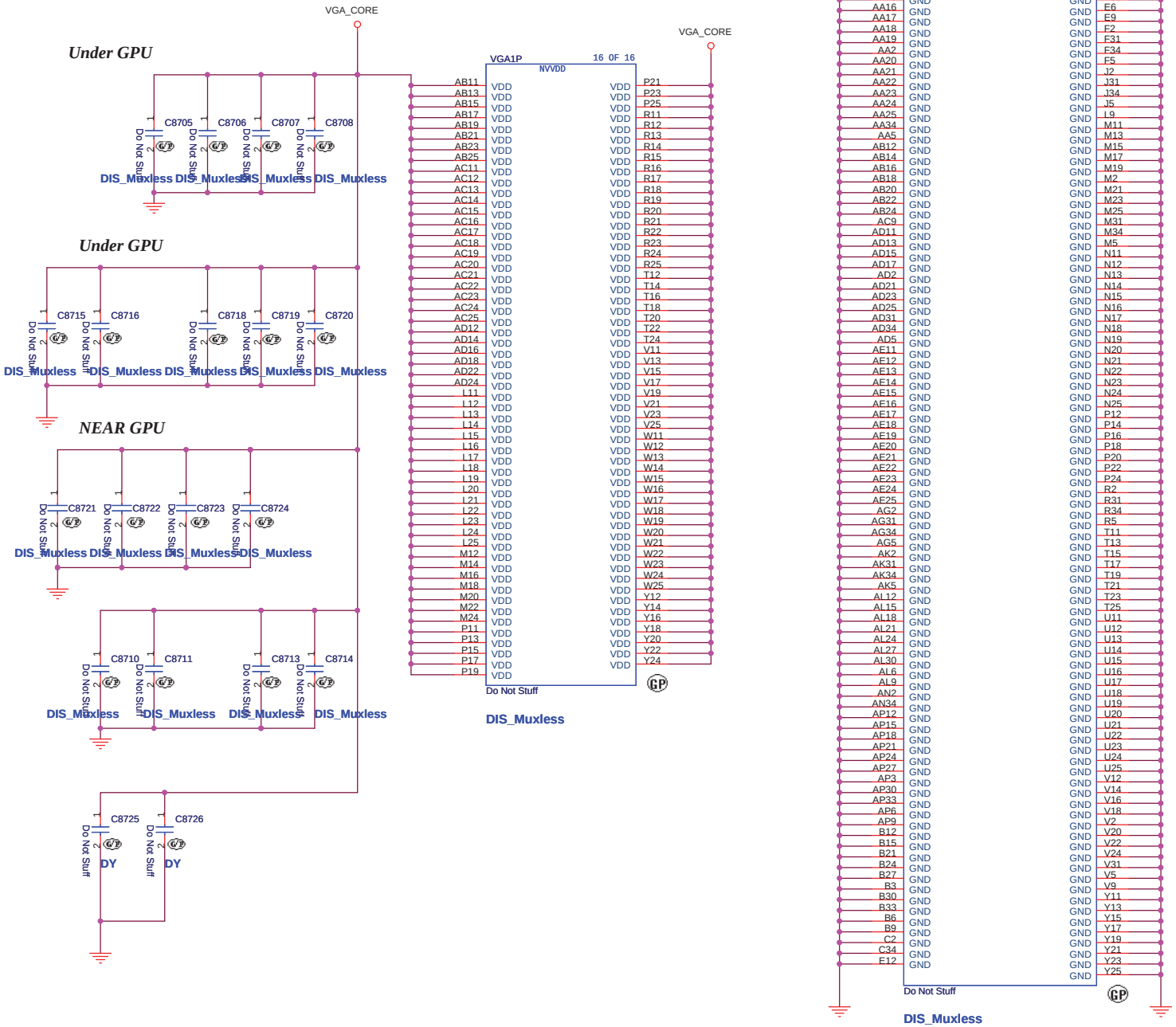




Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL

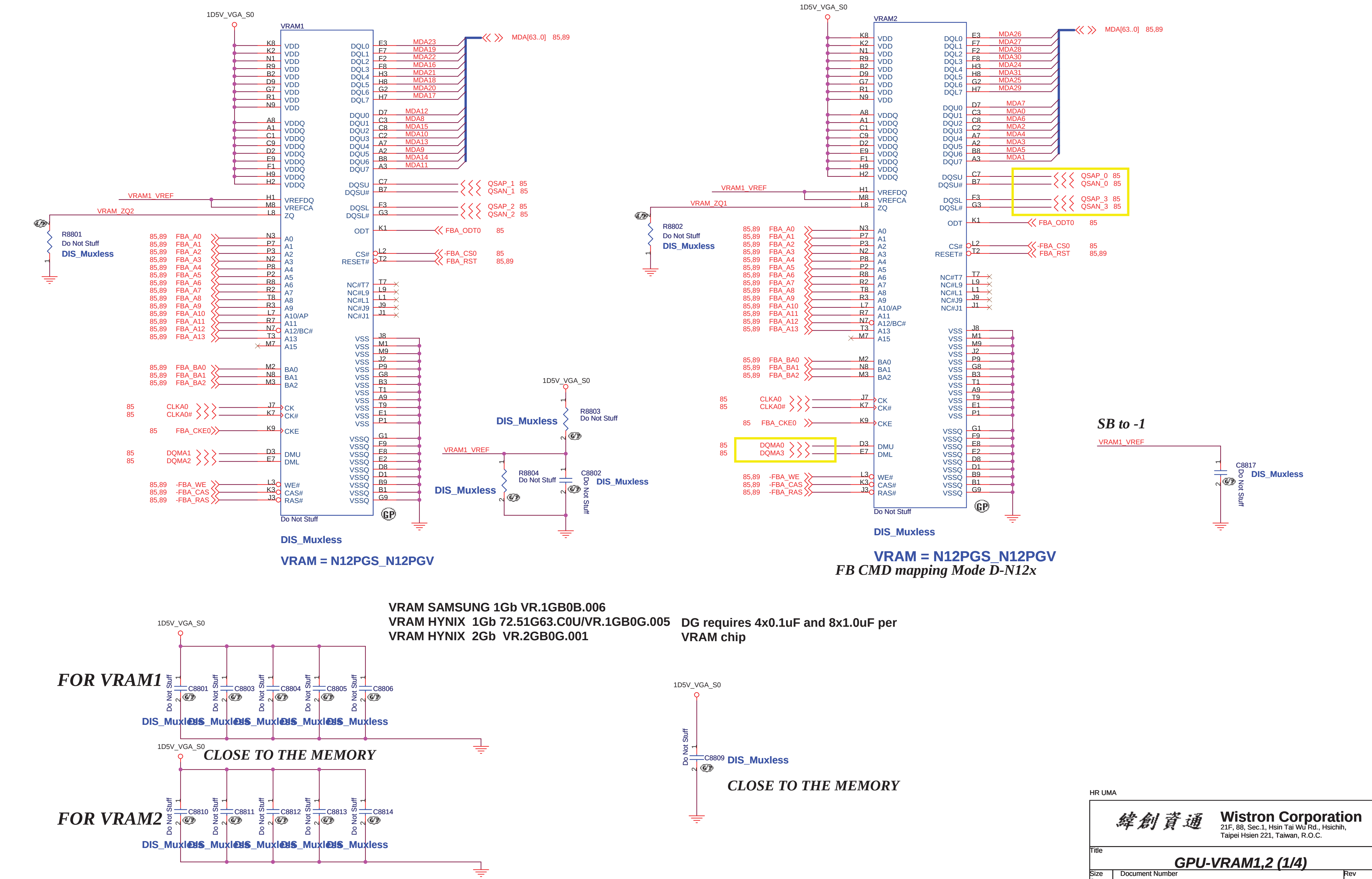
Wistron Corporation	鮮創資通
2SF, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: GPU_POWER(4/5)	
Size: A1	Document Number: JE40-HR
Rev: -1	
Date: Thursday, December 09, 2010	Sheet 88 of 102

EDP 50A
(TDP 37W)



HR UMA

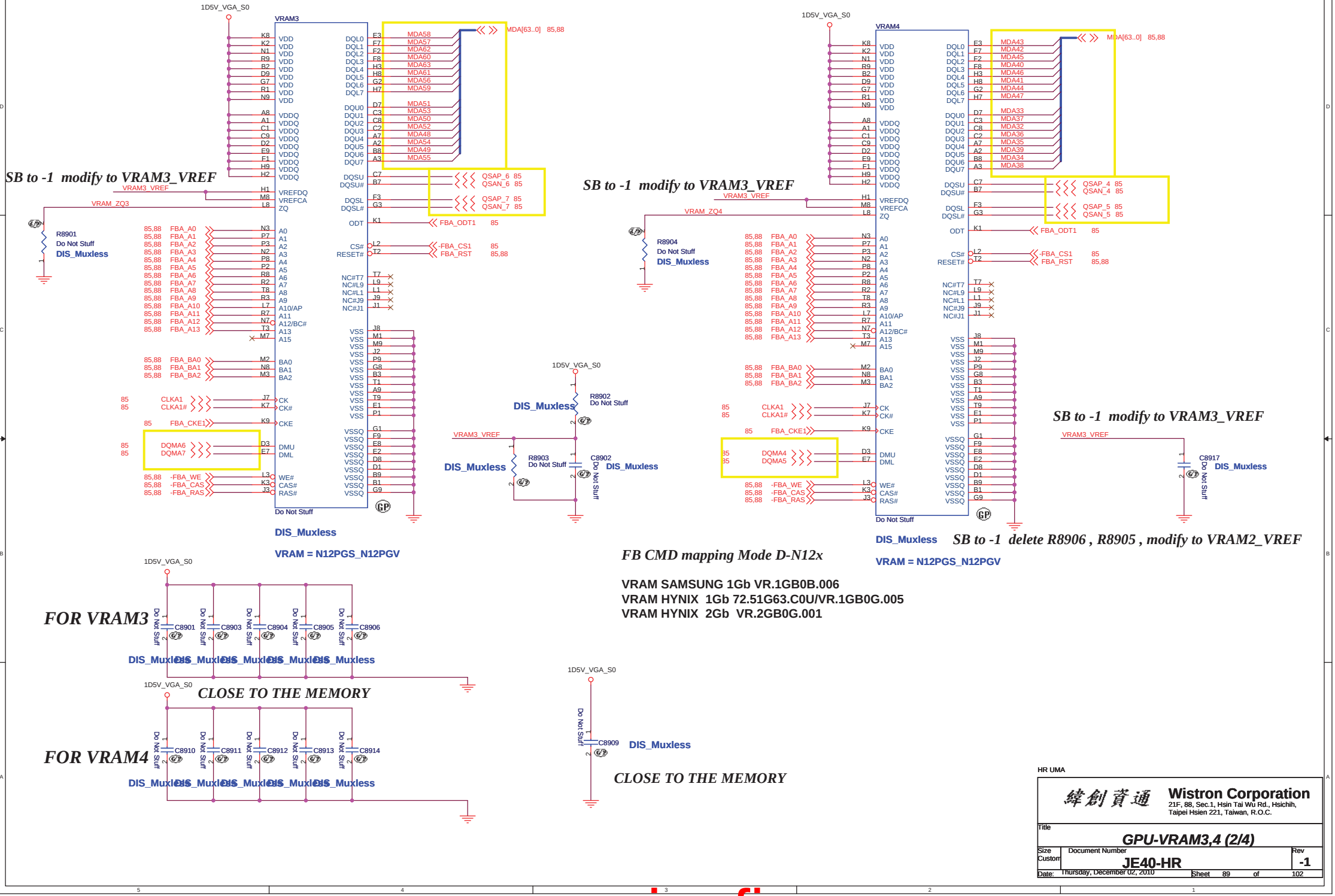
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: GPU_DPPWR/GND(5/5)	
Size: A3	Document Number: JE40-HR
Rev: -1	
Date: Thursday, December 02, 2010	Sheet 87 of 102

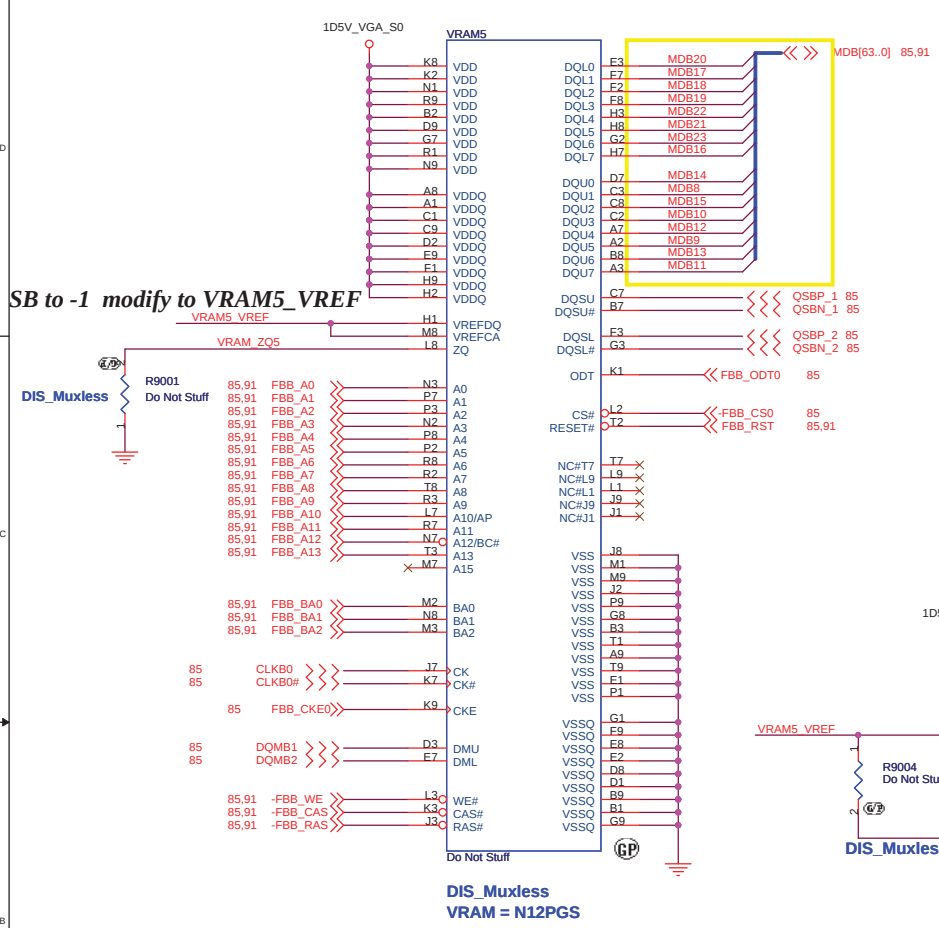


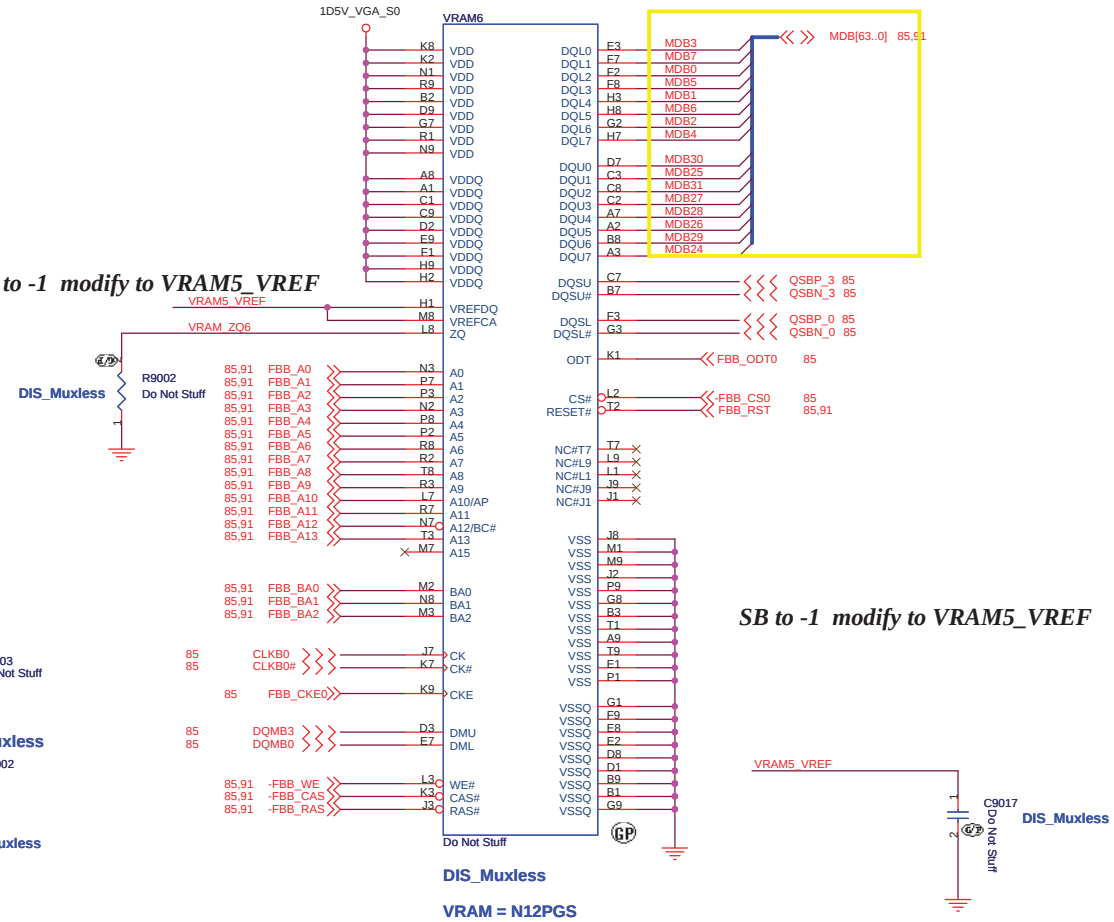
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

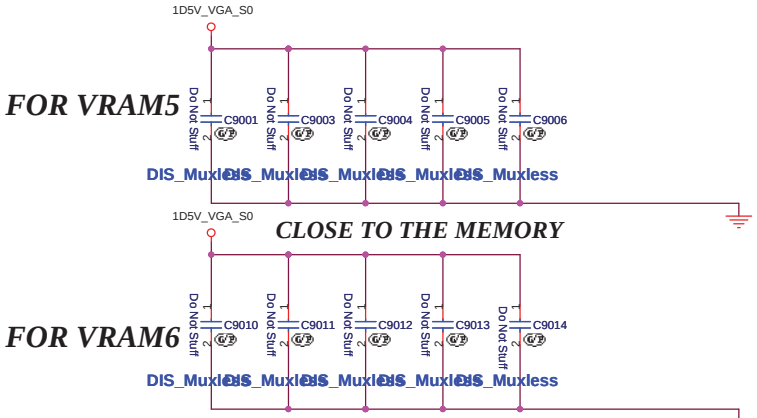
Title		
GPU-VRAM1,2 (1/4)		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 88 of 102	



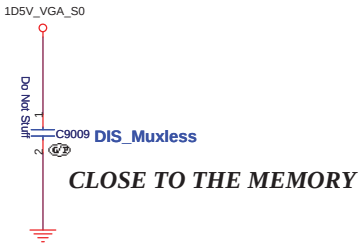




VRAM SAMSUNG 1Gb VR.1GB0B.006
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
VRAM HYNIX 2Gb VR.2GB0G.001



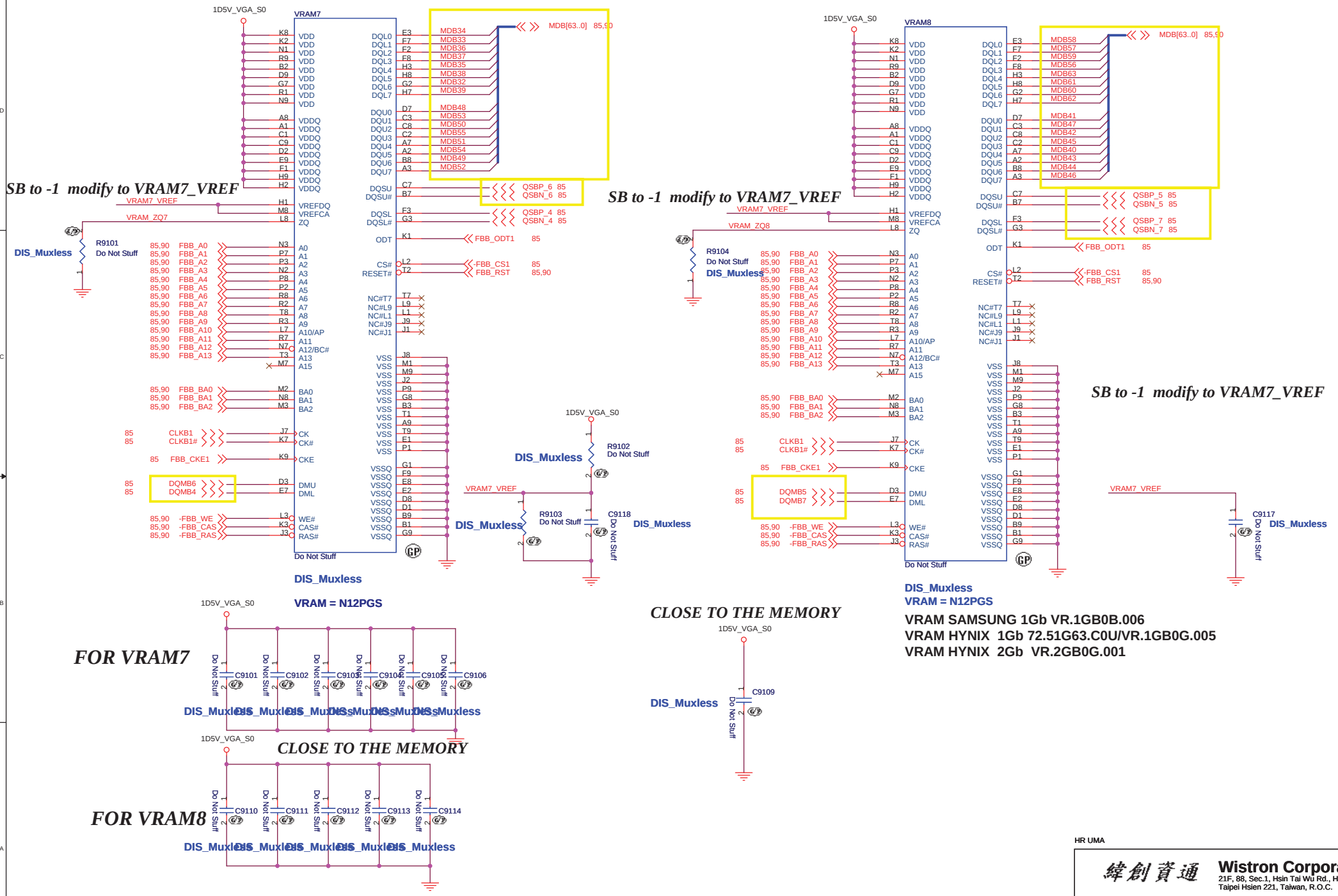
DG requires 4x0.1uF and 8x1.0uF per VRAM chip



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)
Size: Custom | Document Number: JE40-HR | Rev: -1
Date: Thursday, December 02, 2010 | Sheet 90 of 102



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM7,8 (4/4)

Size: Custom | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 91 of 102

SSID = PWR.Plane.Regulator_GFX

20100715

20100719

SB 20100831

SB 20100831

RT8208A

N12P GS

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.825V
P0 - HOT	L	H	0.975V
P0 - COLD	H	L	1.00V
	H	H	

N12P GV

P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

Switching freq-->350KHz

Frequency setting
470K -->165KHz
200K -->323KHz
100K -->500KHz

Vout=0.75V*(R1+R2)/R2

Design Current = 21.94A
24.14A<OCP< 28.53A

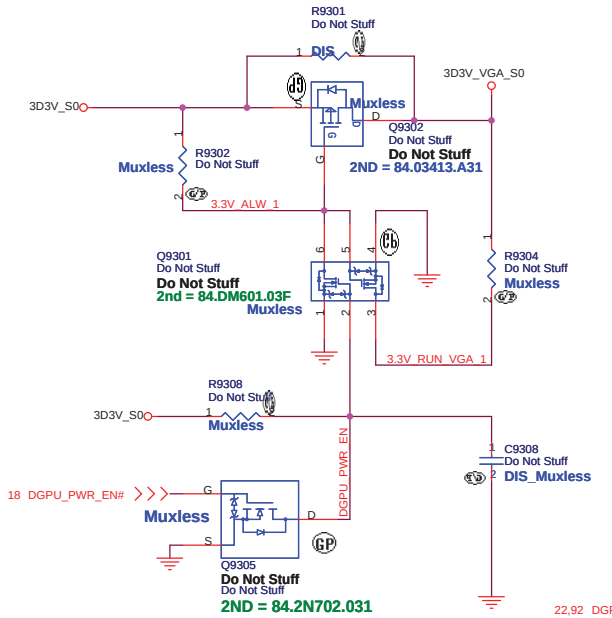
Vout=0.75V*(R1+R2)/R2

SB to -1 modify PR9213 VGA_Core to 1.05V

Title	RT8208B_+VGA_CORE
Size	Custom
Document Number	JE40-HR
Rev	-1
Date	Thursday, December 02, 2010
Sheet	92 of 102

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

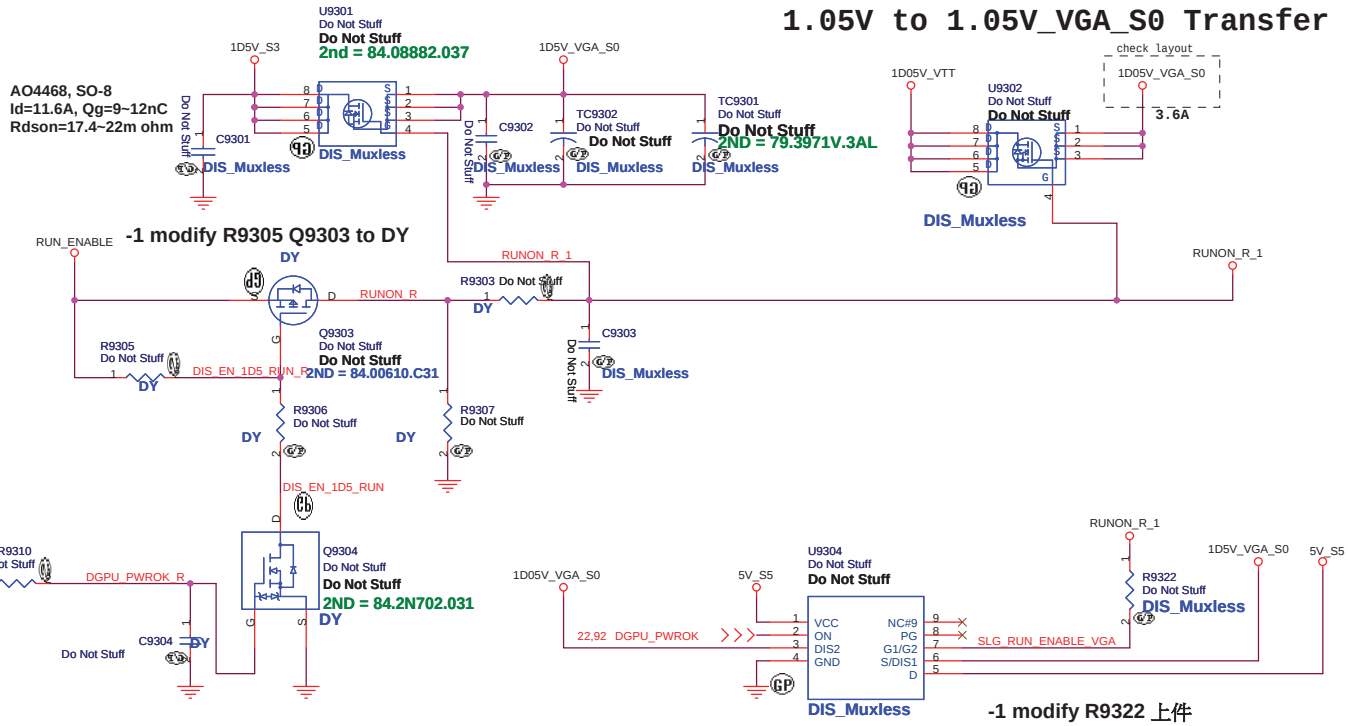
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0

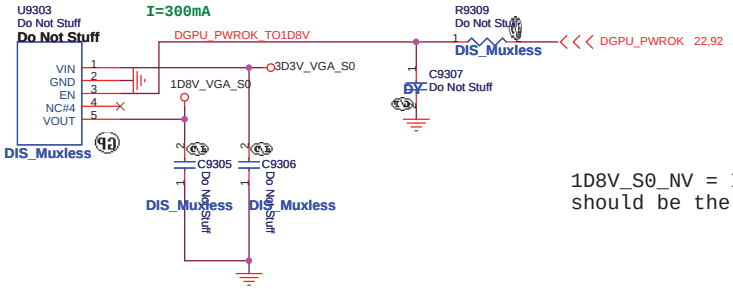
SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer



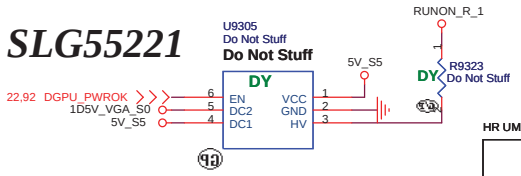
RT9025 for 1D8V_VGA

+3VS to 1.8V Transfer



1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

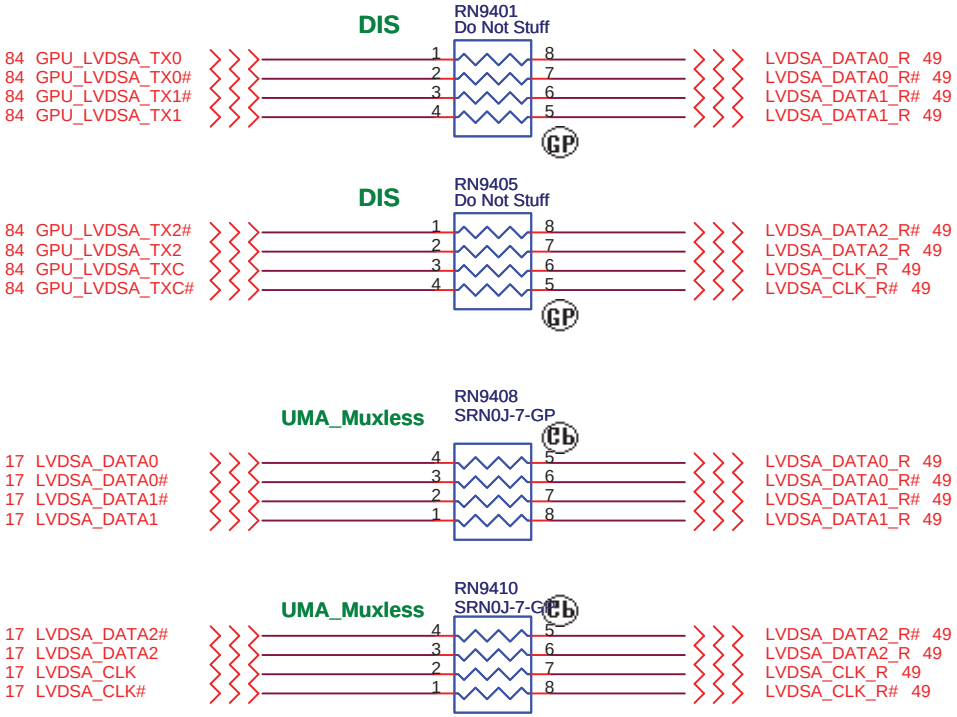
-1 co-layout SLG55221

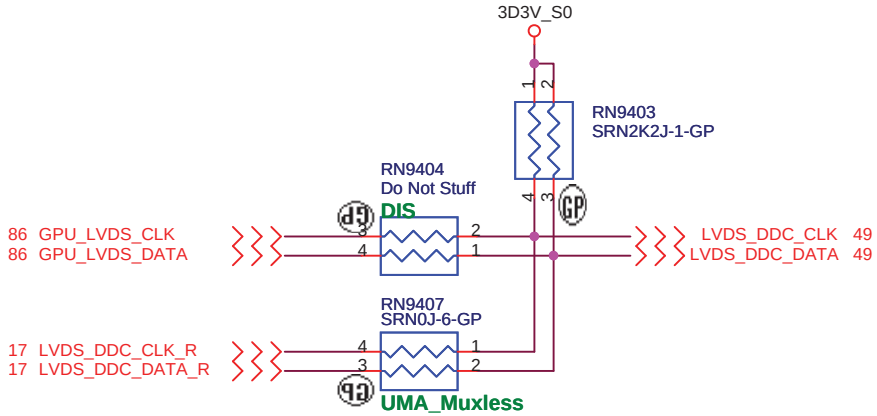


HR UMA

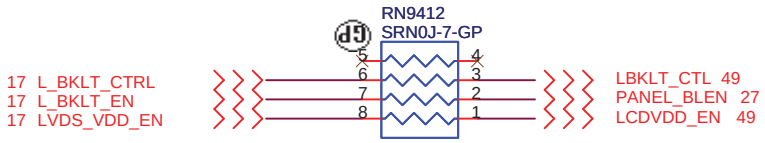
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DISCRETE VGA POWER		
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 93 of 102	

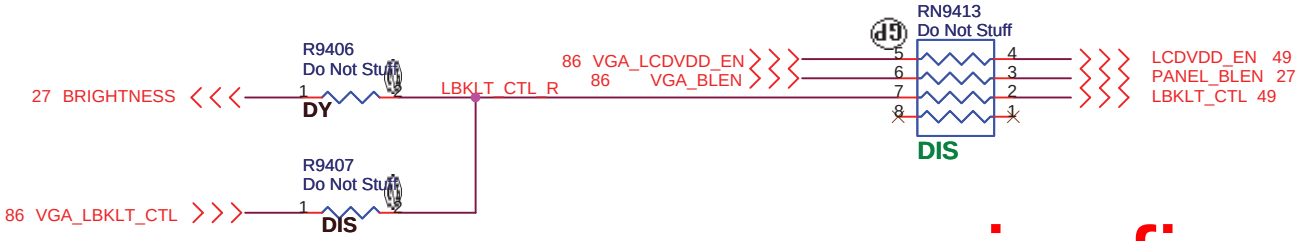
LVDS Channel A





Panel BL brightness/Power En/BL En

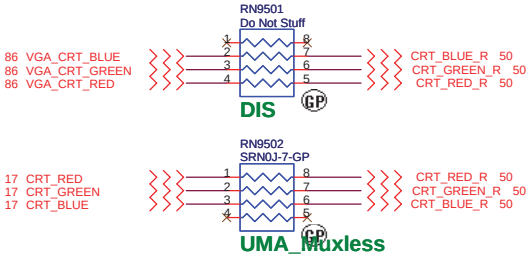




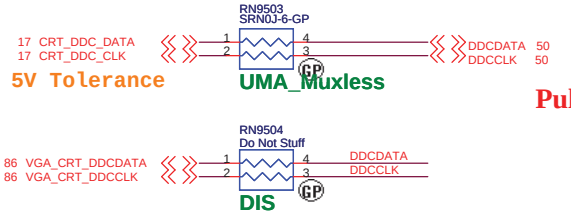
HR UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***LVDS_Switch***	
Size A4	Document Number **JE40-HR**	Rev **-1**
Date: Thursday, December 02, 2010	Sheet 94 of 102	

Close to CRT Board CONN

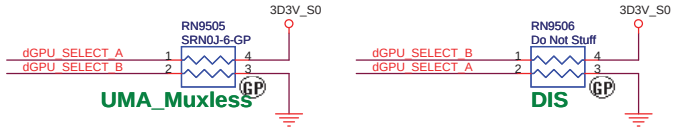


CRT DDCDATA & DDCCLK



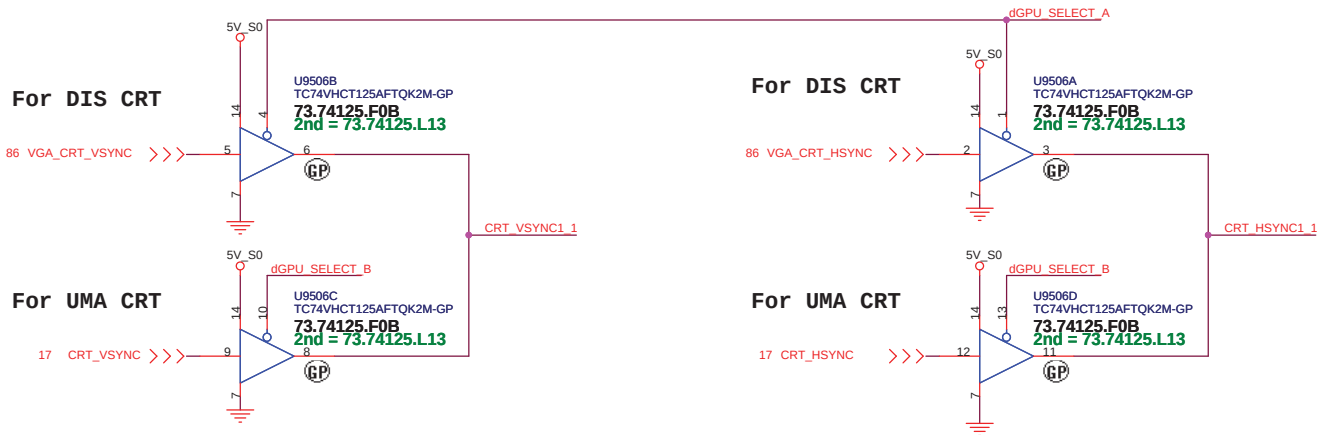
Pull high 在CRT

SB to -1 modify 4 port Logic

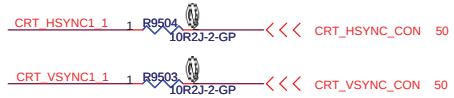


CRT Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA



SB to -1 modify R9503,R9504 to 10 ohm



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT Switch

Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 95 of 102

SSID = SDIO

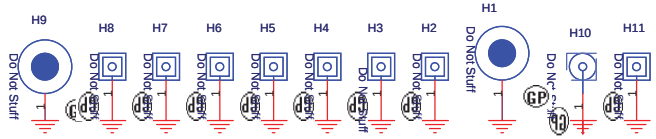
HR UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

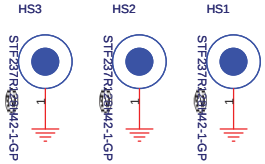
Title: ***TOUCH PANEL***

Size	Document Number	Rev
A2	JE40-HR	-1

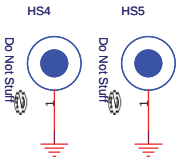
Date: Thursday, December 02, 2010 Sheet 96 of 102

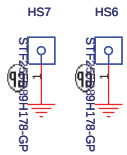


CPU



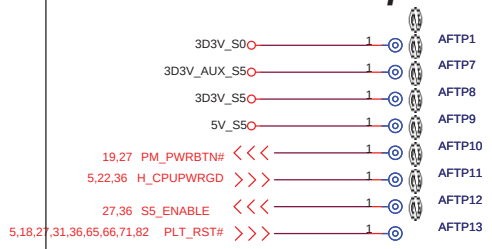
VGA





3G Sku

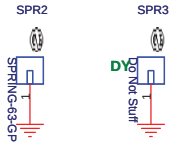
Check test point



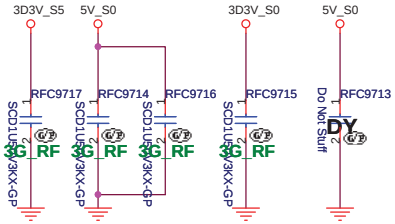
Test Point放在Dimm Door打開可量測處

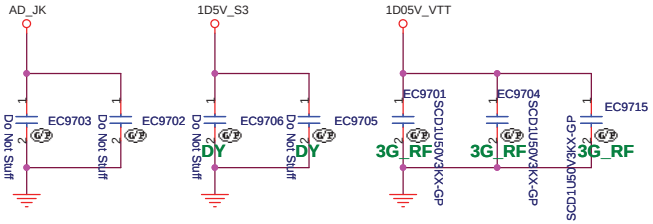
SB to -1 BOM add SPR2

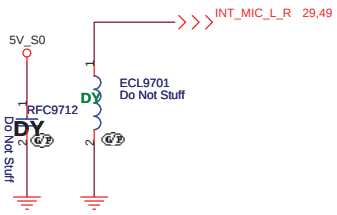
-2 delete SPR5

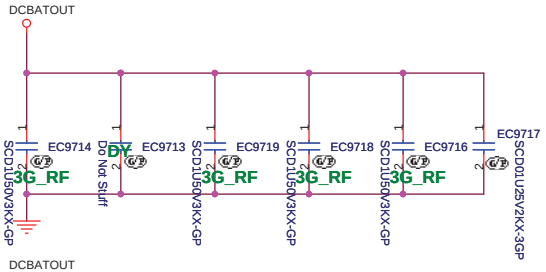


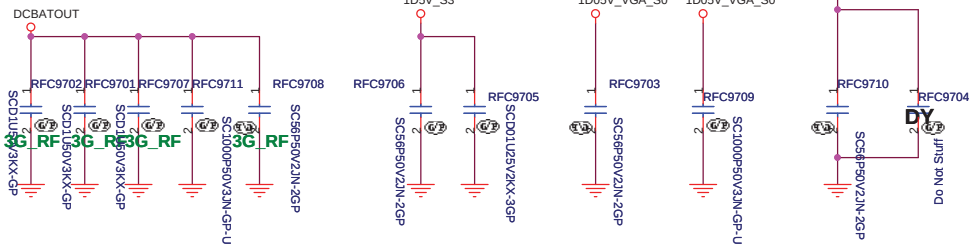
Change:34.40V16.001

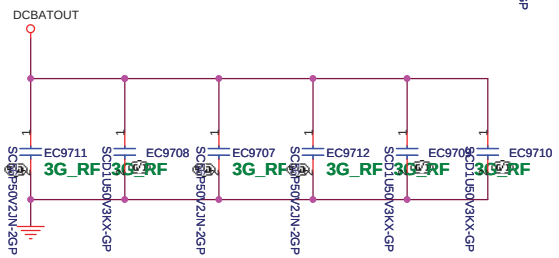








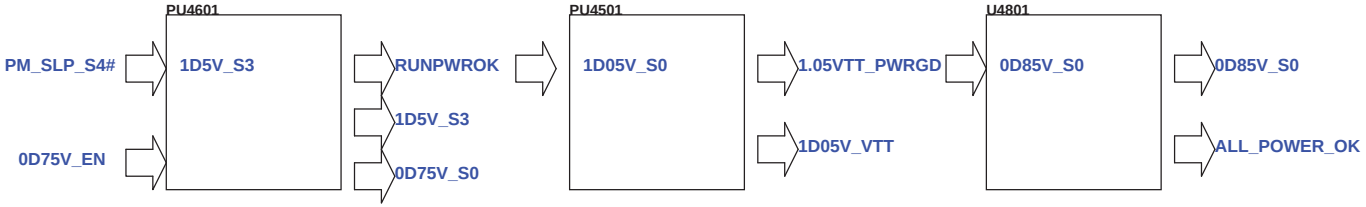


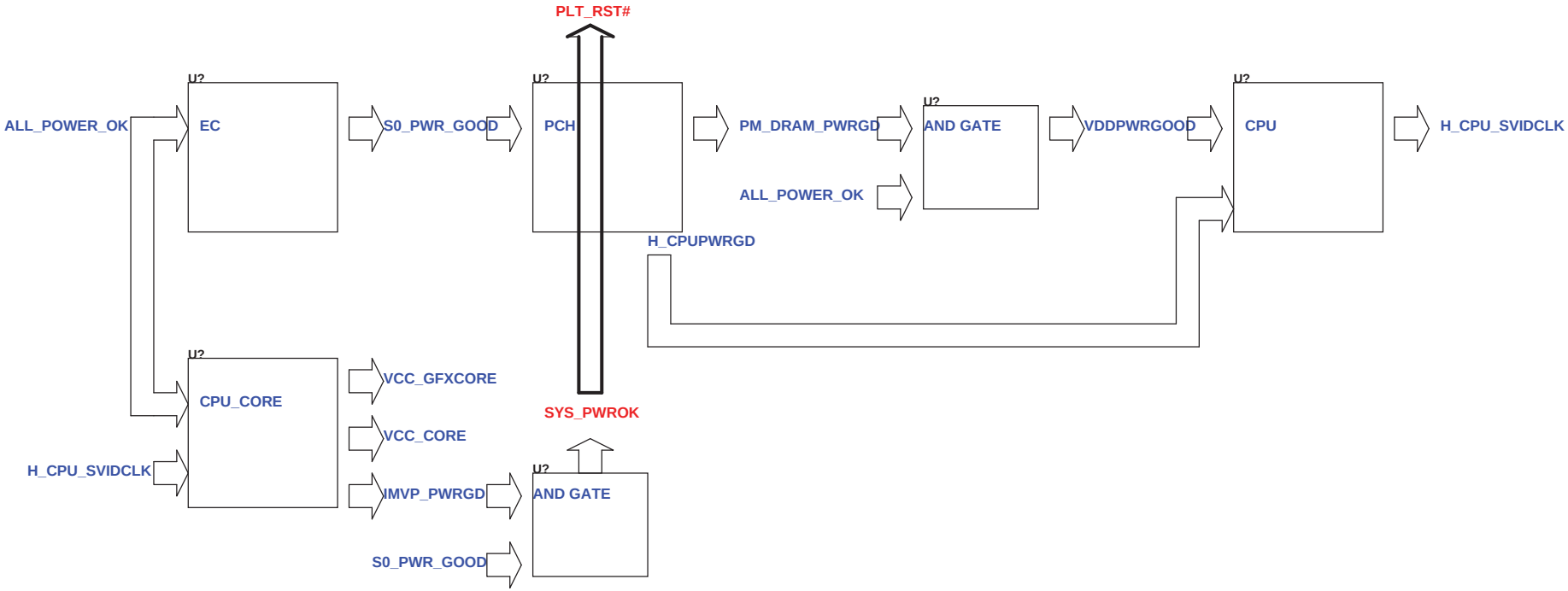


HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *UNUSED PARTS/EMI Capacitors*		
Size: A3	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 97 of 102	

Power Sequence





HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Change History

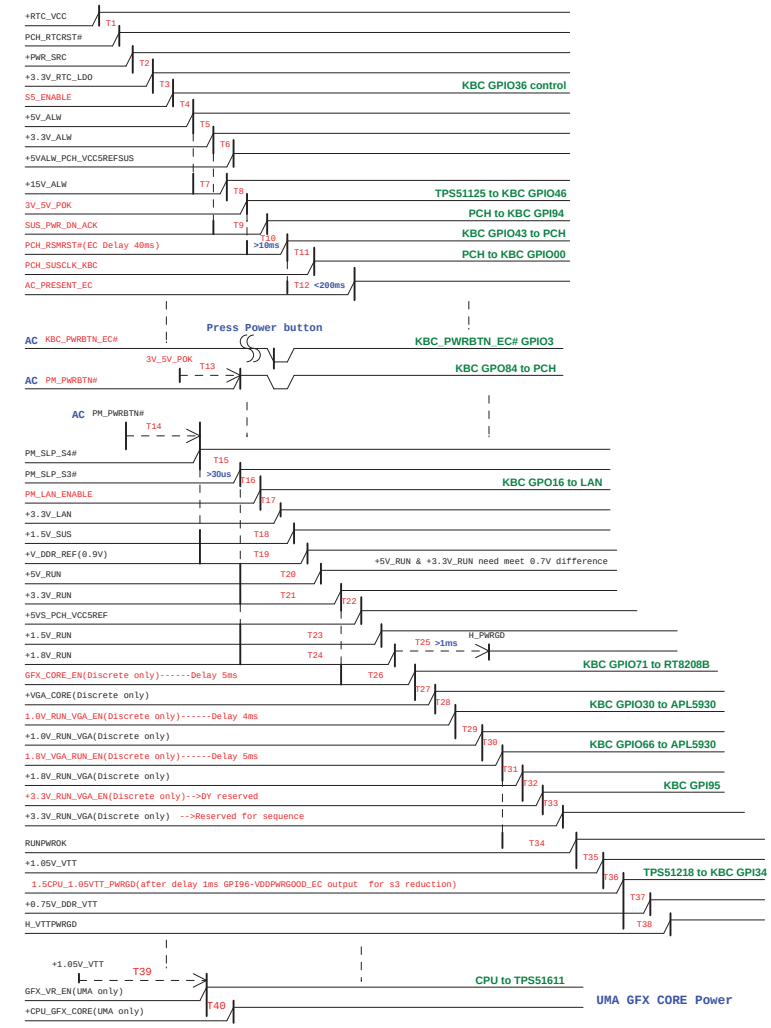
Size: A3 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 98 of 102

Intel-Power Up Sequence

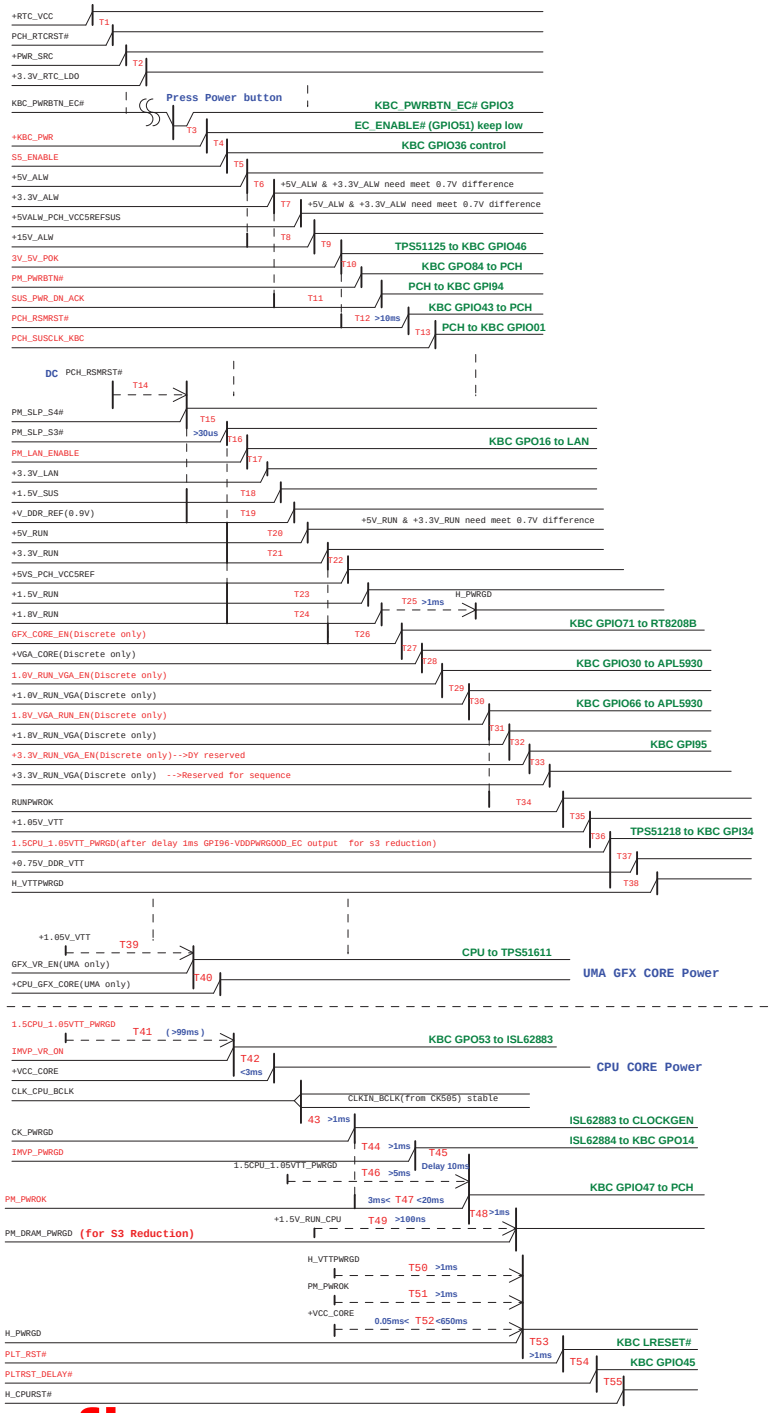
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



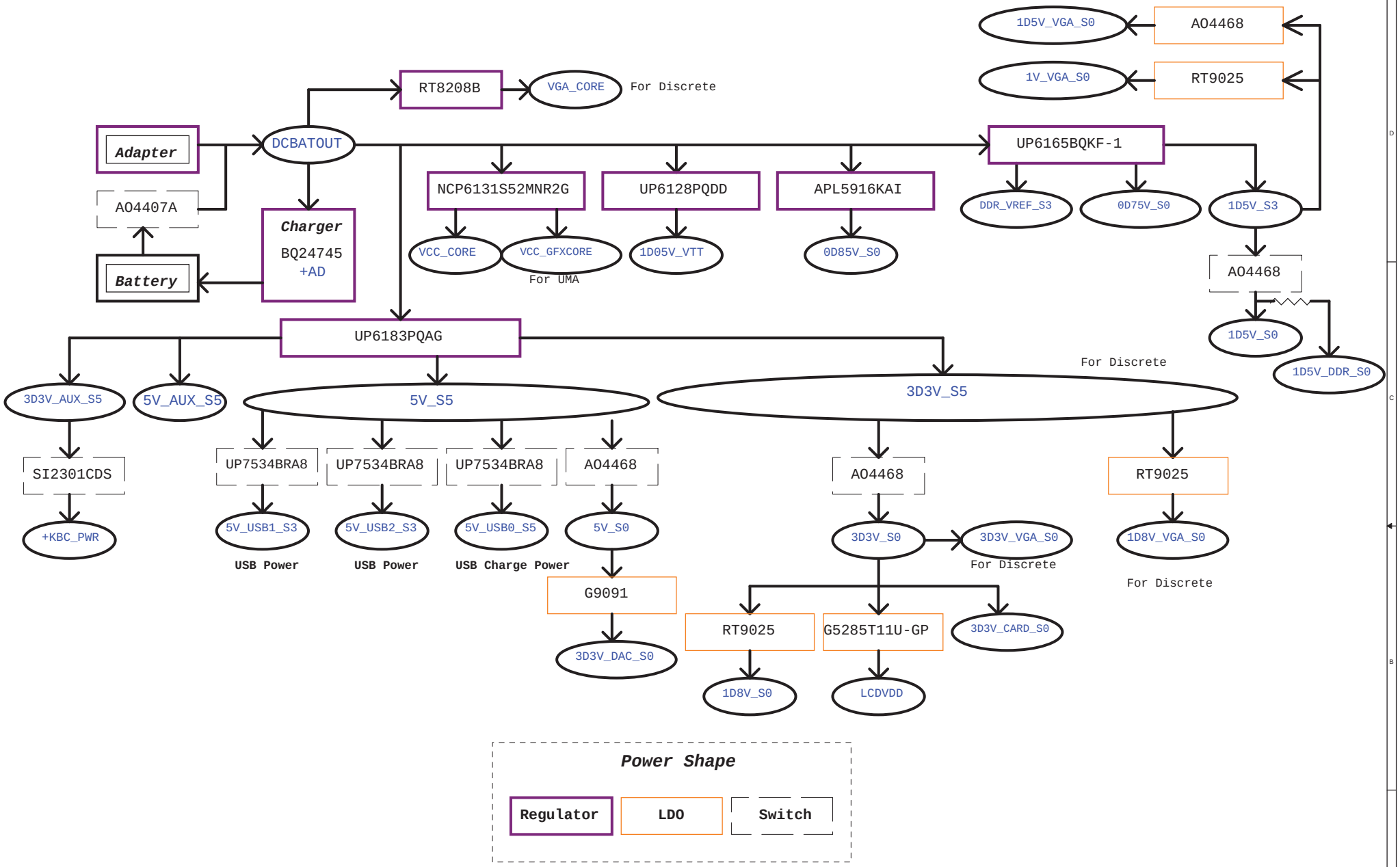
HR UMA

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence

Size: A1 | Document Number: JE40-HR | Rev: -1

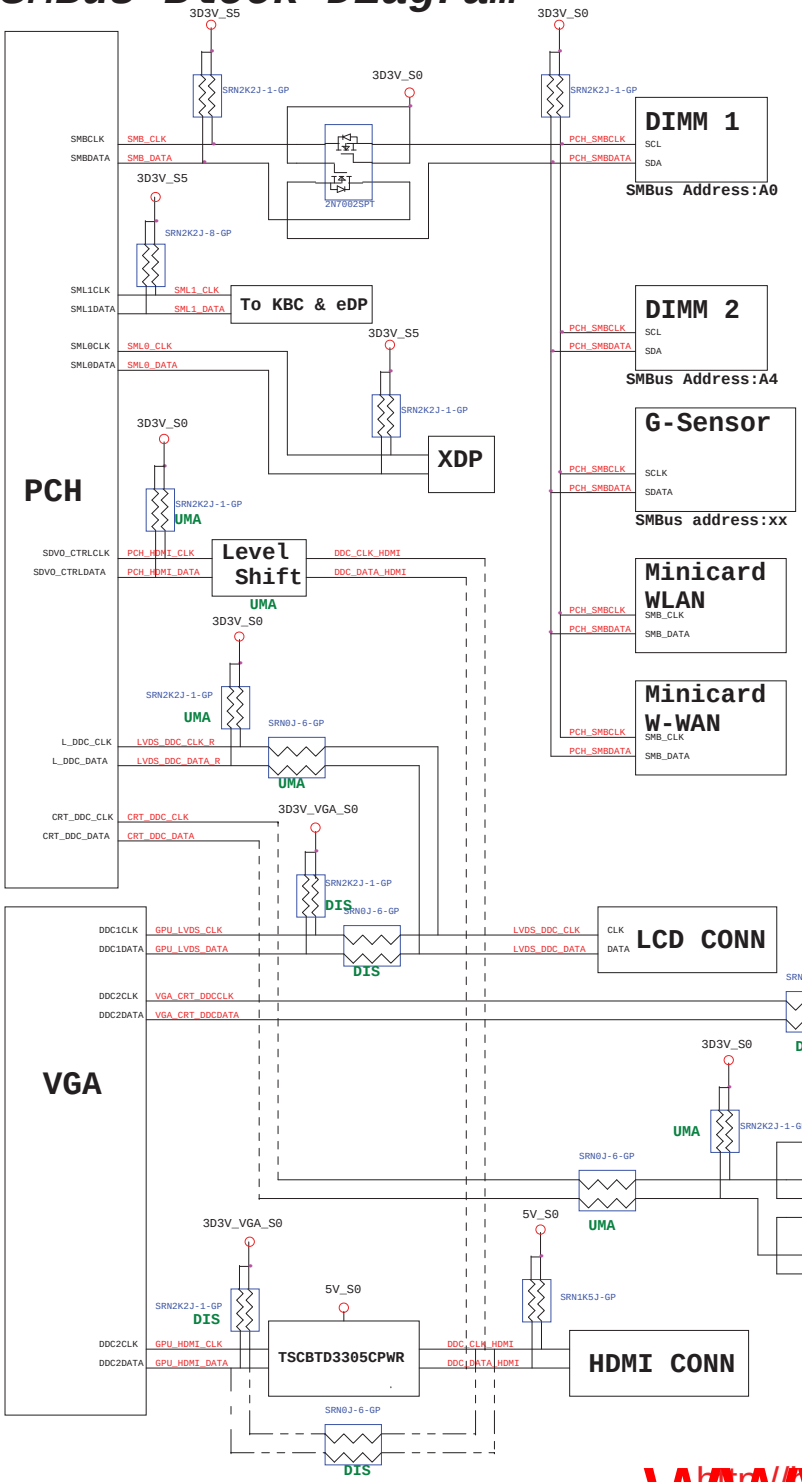
Date: Thursday, December 06, 2007 | Sheet 68 of 102



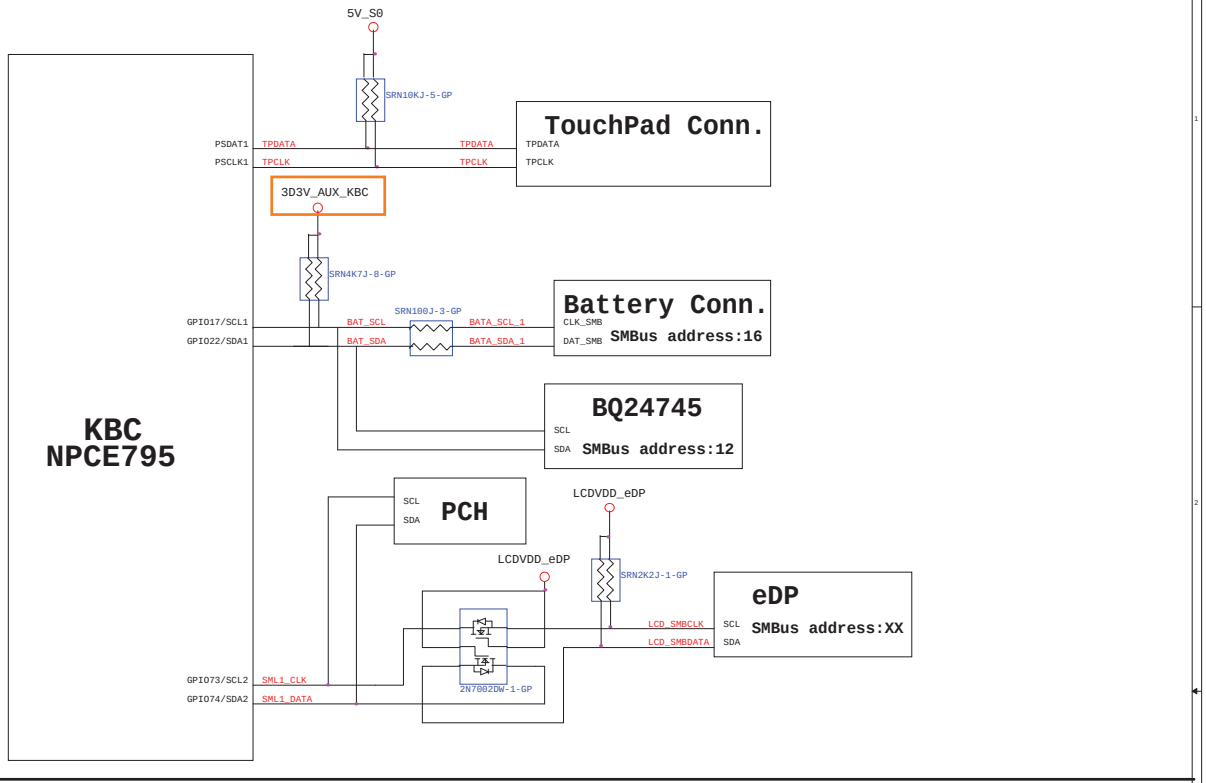
HR UMA

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Power Block Diagram
Size A3	Document Number JE40-HR Rev -1
Date: Thursday, December 02, 2010	Sheet 100 of 102

PCH SMBus Block Diagram



KBC SMBus Block Diagram



HR UMA

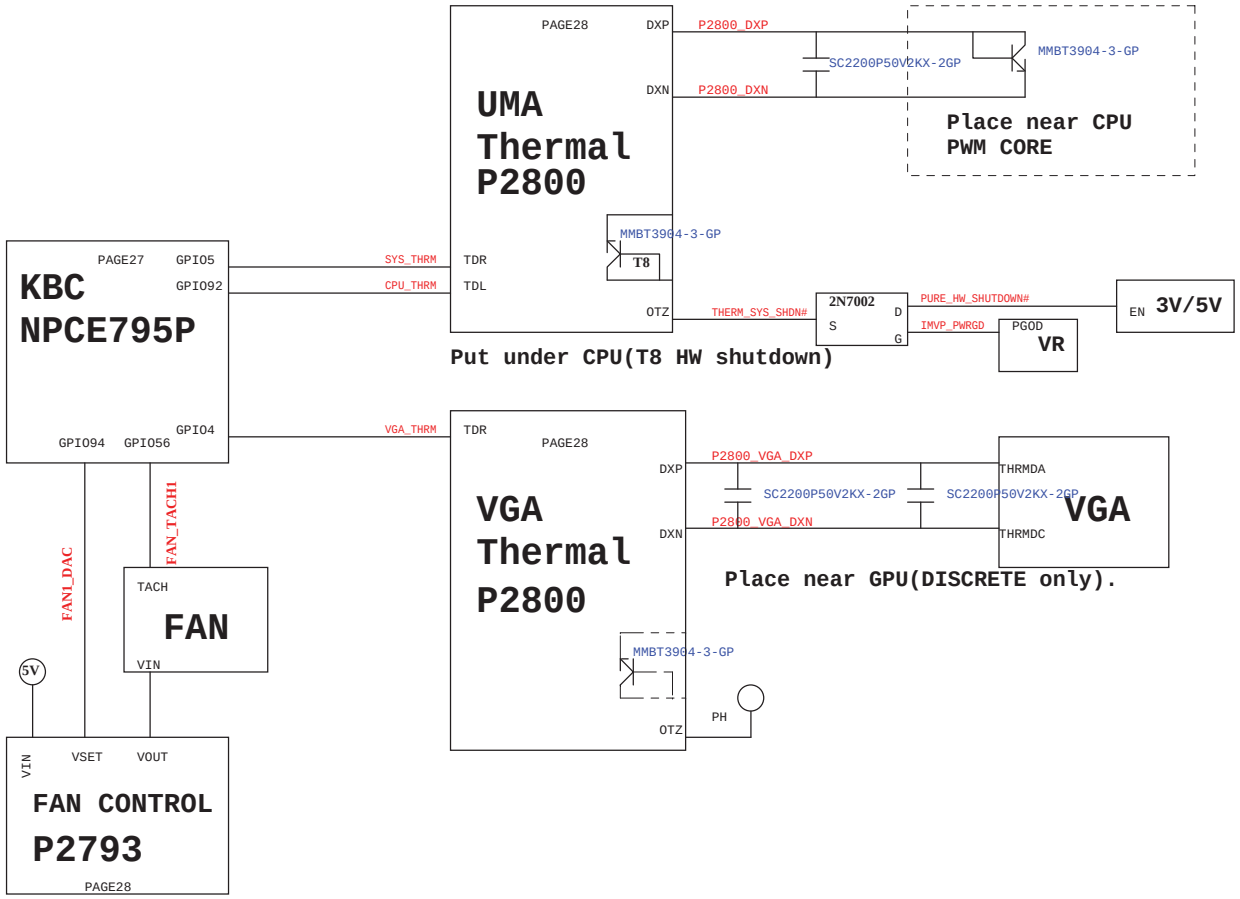
Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS Block Diagram

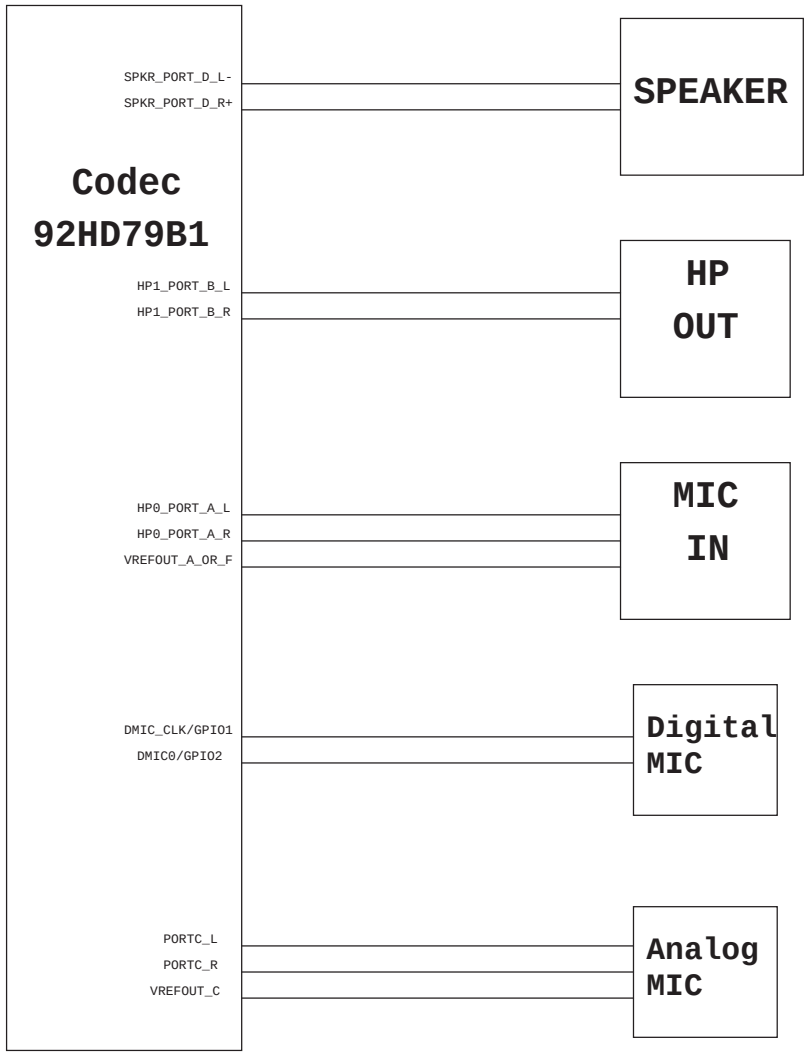
Size: A2 | Document Number: JE40-HR | Rev: -1

Date: Thursday, December 02, 2010 | Sheet 101 of 102

Thermal Block Diagram



Audio Block Diagram



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Thermal/Audio Block Diagram	
Size: Custom	Document Number: JE40-HR	Rev: -1
Date: Thursday, December 02, 2010	Sheet 102 of 102	