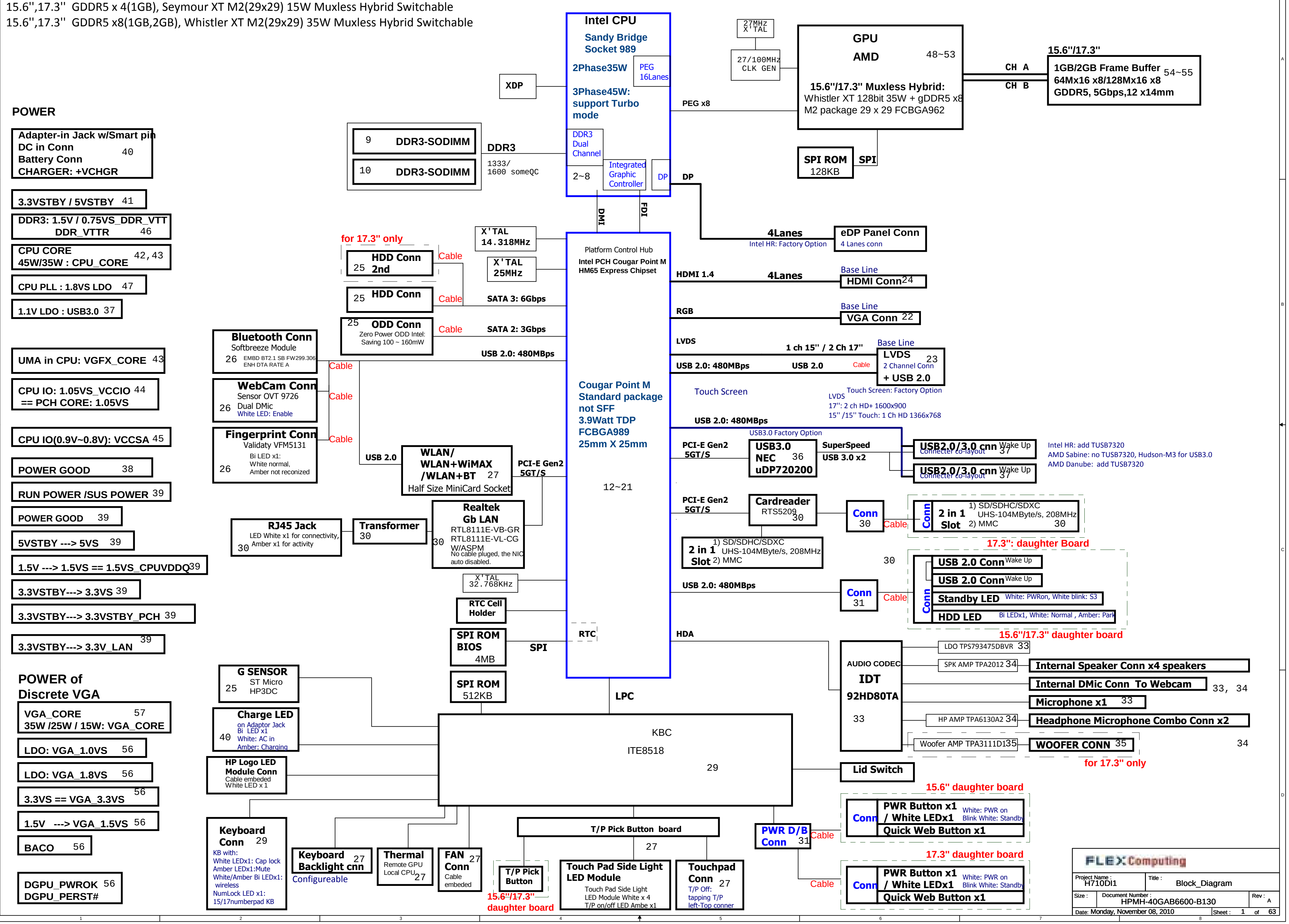
15.6" Grant 1.0 / 17.3" Bogart 1.0

Intel Huron River Sandy Bridge 32nm SV PGA988B i3, i5 DC 35W/ i7 QC 45W

15.6'',17.3'' GDDR5 x 4(1GB), Seymour XT M2(29x29) 15W Muxless Hybrid Switchable
15.6'',17.3'' GDDR5 x8(1GB,2GB), Whistler XT M2(29x29) 35W Muxless Hybrid Switchable



FLEX Computing

Project Name : H710DI1	Title : Block_Diagram	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : A
Date: Monday, November 08, 2010	Sheet : 1 of 63	

Layout
DMI
Differential 85ohm (single 50)
n,p mismatch <5mils
maximum mis-match between inter-pairs : 7000 mils (177.8 mm)
Max: [2000 to 8000 mils, 3vias]
436735 Huron River Design Guide 1.0

Layout
FDI
Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
3vias : 2000 to 8000 mils
4vias : 2000 to 6500 mils
436735 Huron River Design Guide 1.0

Note:
FDI (Flexible Display Interface):
Carries display traffic
from the integrated graphics controller
to the legacy display connectors in the PCH.

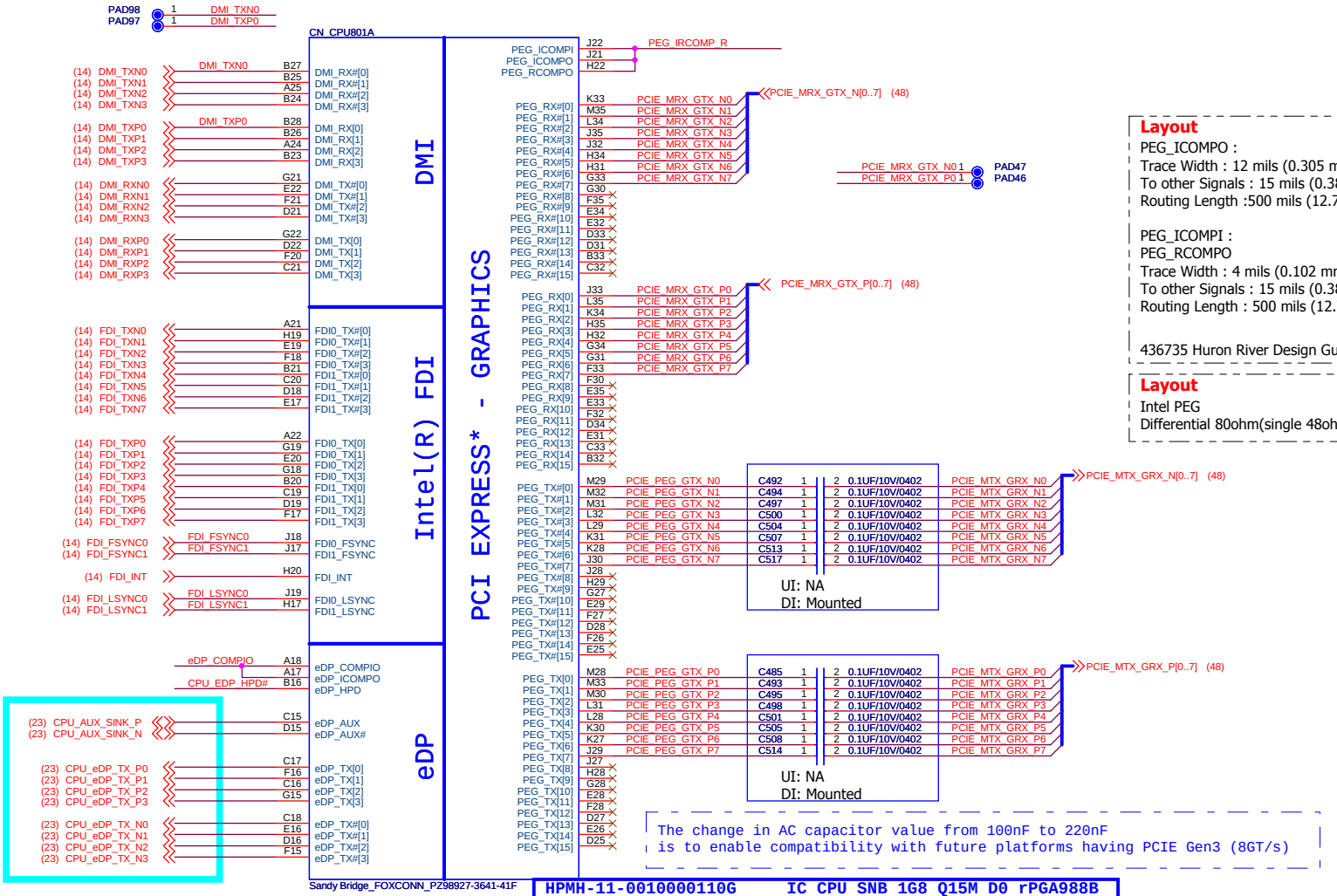
Layout
DP_ICOMPO :
Trace Width : 12 mils (0.305 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length :500 mils (12.7 mm)

DP_COMPIO :
PEG_RCOMPO
Trace Width : 4 mils (0.102 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

436735 Huron River Design Guide 1.0

Layout
eDP
Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
2vias : 2000 - 8000 mils
4vias : 2000 - 8000 mils
436735 Huron River Design Guide 1.0

Layout(Switchable Graphics Topology)
eDP
Differential 85ohm (single 50)
n,p mismatch <5mils
pair to pair mismatch < 7 inches
Max:
4vias : 2000 - 5000 mils
436735 Huron River Design Guide 1.0



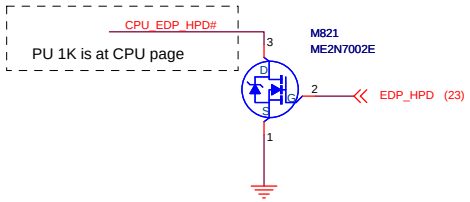
Layout
PEG_ICOMPO :
Trace Width : 12 mils (0.305 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length :500 mils (12.7 mm)

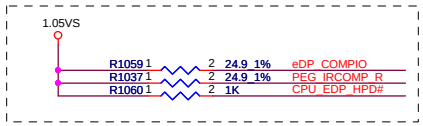
PEG_ICOMPI :
PEG_RCOMPO
Trace Width : 4 mils (0.102 mm)
To other Signals : 15 mils (0.381 mm)
Routing Length : 500 mils (12.7 mm)

436735 Huron River Design Guide 1.0

Layout
Intel PEG
Differential 80ohm(single 48ohm)

The change in AC capacitor value from 100nF to 220nF
is to enable compatibility with future platforms having PCIE Gen3 (8GT/s)

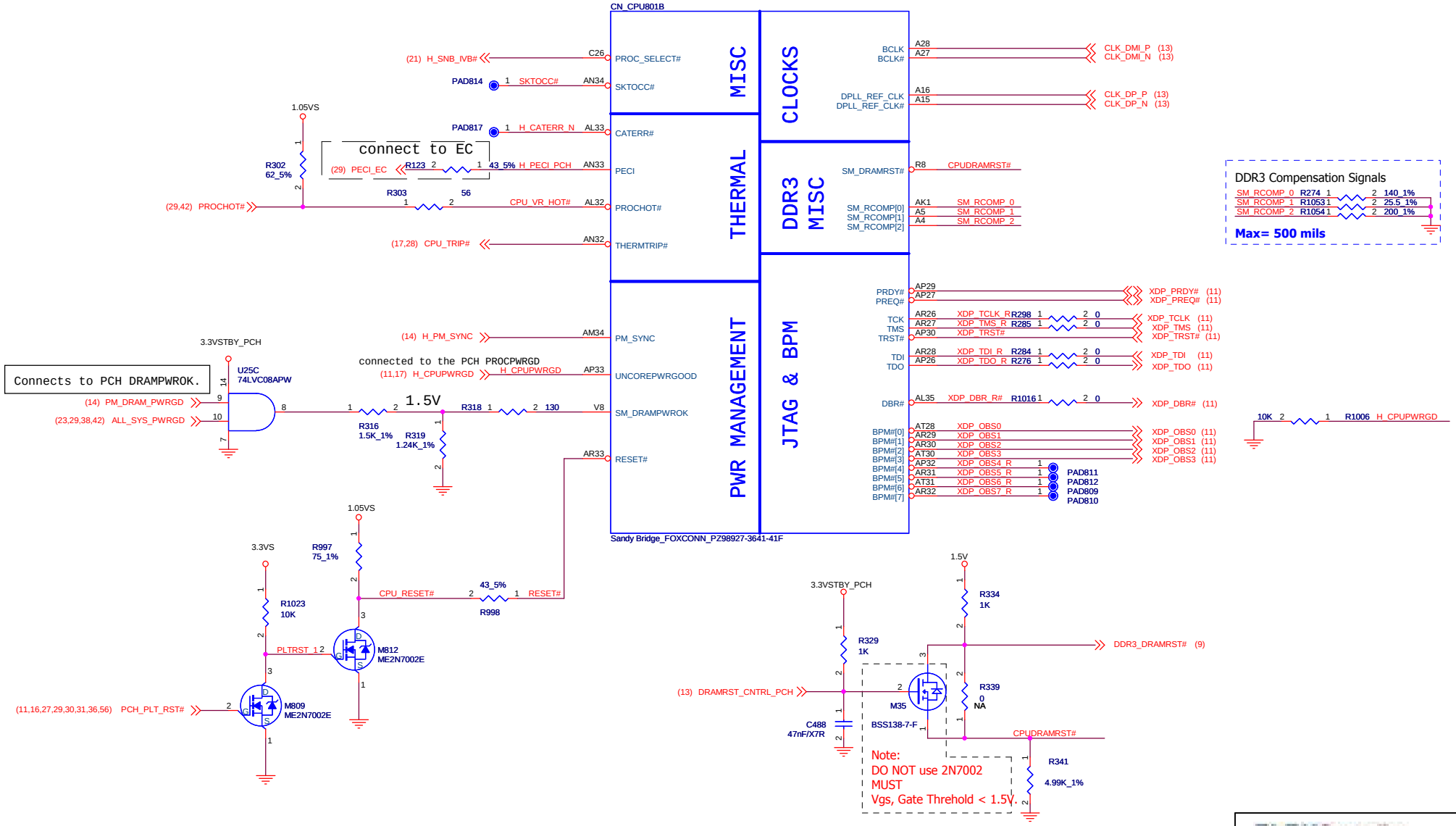




HPMH-11-0010000110G	IC CPU SNB 1G8 Q15M D0 rPGA988B
HPMH-11-0010000111G	IC CPU SNB 2G Q15C D0 rPGA988B
HPMH-11-0010000112G	IC CPU SNB 2G2 Q154 D0 rPGA988B
HPMH-11-0010000113G	IC CPU SNB 2G5 Q17N J0 rPGA988B
HPMH-11-0010000114G	IC CPU SNB 2G6 Q16P J0 rPGA988B
HPMH-11-0010000115G	IC CPU SNB 2G7 Q16M J0 rPGA988B
HPMH-11-0010000116G	IC CPU SNB 2G5 Q17N J0 rPGA988B
HPMH-11-0010000117G	IC CPU SNB 2G2 Q1CL D1 rPGA988B
HPMH-11-0010000118G	IC CPU SNB 2G3 Q1CG D1 rPGA988B
HPMH-11-0010000119G	IC CPU SNB 2G Q1CN D1 rPGA988B
HPMH-11-0010000120G	IC CPU SNB 2G Q1NS D2 rPGA988B
HPMH-11-0010000121G	IC CPU SNB 2G2 Q1NN D2 rPGA988B
HPMH-11-0010000122G	IC CPU SNB 2G3 Q1NC D2 rPGA988B
HPMH-11-0010000123G	IC CPU SNB 2G1 Q1SP J1 rPGA988B
HPMH-11-0010000124G	IC CPU SNB 2G3 Q1SD J1 rPGA988B
HPMH-11-0010000125G	IC CPU SNB 2G5 Q1RX J1 rPGA988B
HPMH-11-0010000126G	IC CPU SNB 2G6 Q1S6 J1 rPGA988B
HPMH-11-0010000127G	IC CPU SNB 2G7 Q1S2 J1 rPGA988B
HPMH-11-0010000128G	IC CPU SNB 2G SR02Y D2 rPGA988B
HPMH-11-0010000129G	IC CPU SNB 2G2 SR014 D2 rPGA988B
HPMH-11-0010000130G	IC CPU SNB 2G3 SR012 D2 rPGA988B

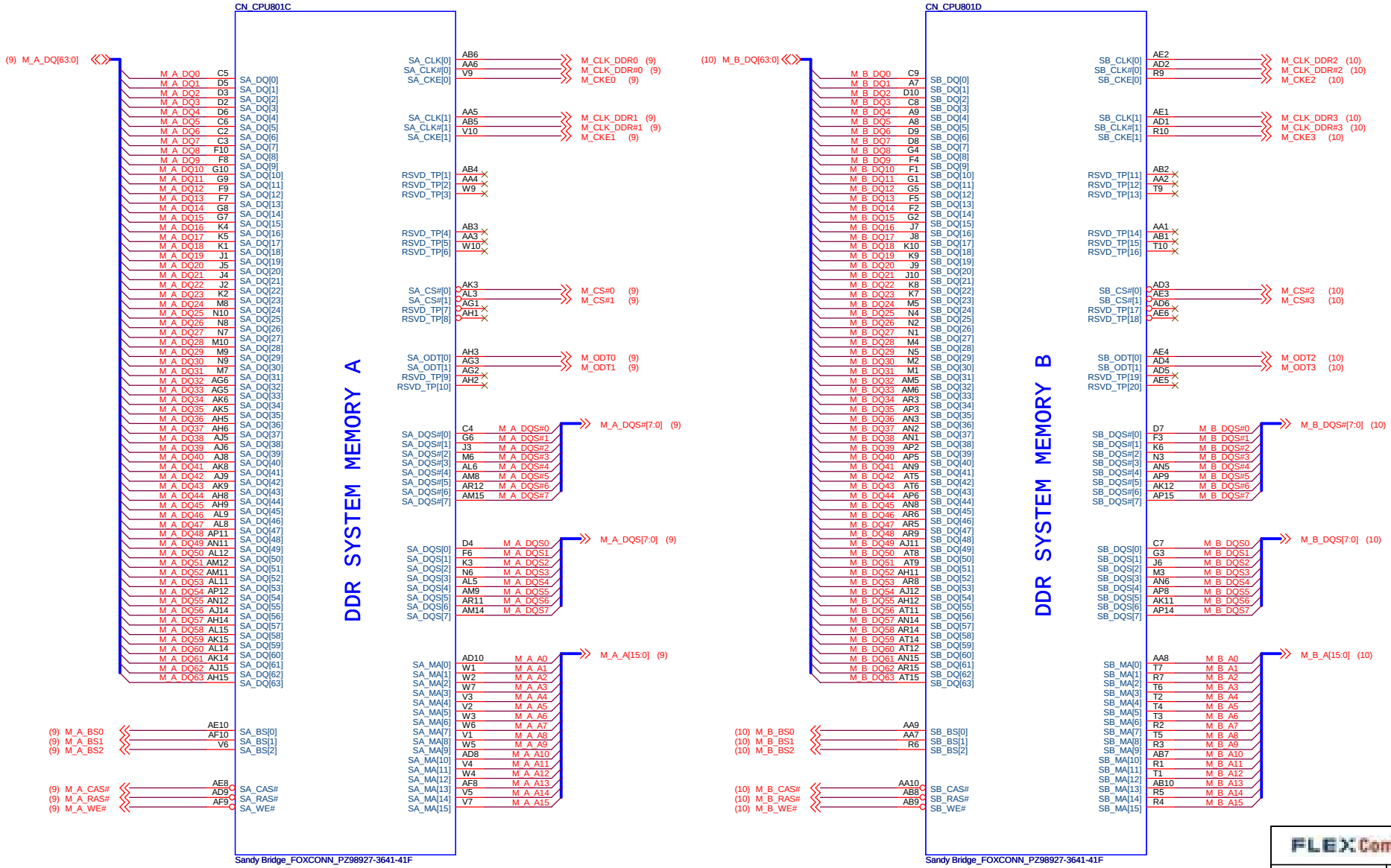
FLEXComputing

Project Name : H710DI1	Title : CPU_1/7_DMI_FDI_PCIE	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 2 of 63	



FLEX Computing

Project Name : H710DI1	Title : CPU_2/7_CLK_MISC_THERM
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 3 of 63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M_A_DQ1 D5
M_A_DQ2 D3
M_A_DQ3 D2
M_A_DQ4 D6
M_A_DQ5 C6
M_A_DQ6 C2
M_A_DQ7 C3
M_A_DQ8 F10
M_A_DQ9 F8
M_A_DQ10 G10
M_A_DQ11 G9
M_A_DQ12 F9
M_A_DQ13 F7
M_A_DQ14 G8
M_A_DQ15 G7
M_A_DQ16 K4
M_A_DQ17 K5
M_A_DQ18 K1
M_A_DQ19 J1
M_A_DQ20 J5
M_A_DQ21 J4
M_A_DQ22 J2
M_A_DQ23 K2
M_A_DQ24 M8
M_A_DQ25 N10
M_A_DQ26 N8
M_A_DQ27 N7
M_A_DQ28 M10
M_A_DQ29 M9
M_A_DQ30 N9
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M_A_DQ33 AG5
M_A_DQ34 AK6
M_A_DQ35 AK5
M_A_DQ36 AH5
M_A_DQ37 AH6
M_A_DQ38 AJ5
M_A_DQ39 AJ6
M_A_DQ40 AJ8
M_A_DQ41 AK8
M_A_DQ42 AJ9
M_A_DQ43 AK9
M_A_DQ44 AH8
M_A_DQ45 AH9
M_A_DQ46 AL9
M_A_DQ47 AL8
M_A_DQ48 AP11
M_A_DQ49 AN11
M_A_DQ50 AL12
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M_A_DQ59 AK15
M_A_DQ60 AL14
M_A_DQ61 AK14
M_A_DQ62 AJ15
M_A_DQ63 AH15
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AF10
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AA6
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AA3
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AL3
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M_CS#1 (9)
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N6 M_A_DQS3
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AM14 M_A_DQS7
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W2 M_A_A2
W7 M_A_A3
V3 M_A_A4
V2 M_A_A5
W3 M_A_A6
W6 M_A_A7
V1 M_A_A8
W5 M_A_A9
AD8 M_A_A10
V4 M_A_A11
W4 M_A_A12
AF8 M_A_A13
V5 M_A_A14
V7 M_A_A15
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M_B_DQ36 AN3
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AA7
R6
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AB8
AB9
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AD1
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AB1
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AE3
AD6
AE6
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AD5
AE5
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M_ODT3 (10)
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K6 M_B_DQS#2
N3 M_B_DQS#3
AN5 M_B_DQS#4
AP9 M_B_DQS#5
AK12 M_B_DQS#6
AP15 M_B_DQS#7
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J6 M_B_DQS2
M3 M_B_DQS3
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AP14 M_B_DQS7
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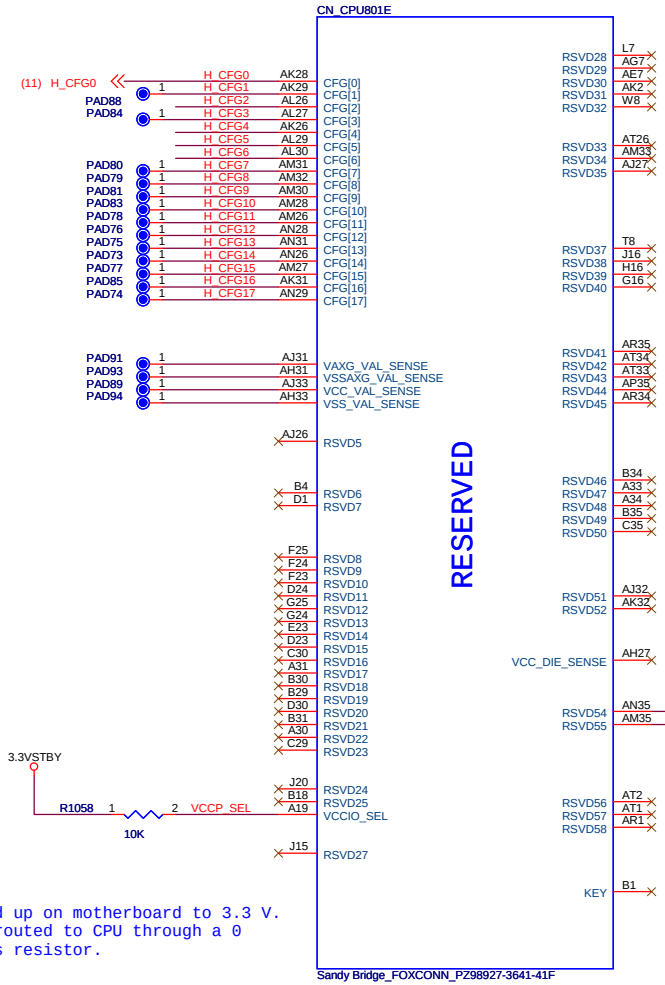
R7 M_B_A2
T6 M_B_A3
T2 M_B_A4
T4 M_B_A5
T3 M_B_A6
R2 M_B_A7
T5 M_B_A8
R3 M_B_A9
AB7 M_B_A10
R1 M_B_A11
T1 M_B_A12
AB10 M_B_A13
R5 M_B_A14
R4 M_B_A15
M_B_A[15:0] (10)
Sandy Bridge_FOXCONN_PZ98927-3641-41F
Sandy Bridge_FOXCONN_PZ98927-3641-41F
FLEX Computing
Project Name : H710DI1
Title : CPU_3/7_DDR3
Size :
Document Number : HPMH-40GAB6600-B130
Rev : B
Date: Monday, November 08, 2010
Sheet : 4 of 63

CFG Straps for PROCESSOR



Pulled up on motherboard to 3.3 V.
Also routed to CPU through a 0 series resistor.

VCCIO_SEL On CRB
H_SNB_IVB#_PWRCTRL = low, 1.0V
H_SNB_IVB#_PWRCTRL = high/NC, 1.05V

Voltage selection for VCCIO: For Huron River platforms, this pin must be pulled high on the motherboard

H_CFG5 R267 1 2 1K
H_CFG6 1
PAD82

PCIE Port Bifurcation Straps	
CFG[6:5]	11:(Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled function 2 disabled 01: Reserved - Device 1 function 1 disabled function 2 enabled 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

H_CFG7 R258 1 2 1K NA

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

CFG[17:7]	Reserved configuration lanes. A test point may be placed on the board for these lands.

CFG[1:0]	Reserved configuration lane. A test point may be placed on the board for this lane.

H_CFG2 1
PAD86

PEG Static Lane Reversal - CFG2 is for the 16x	
CFG[2]	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane numbers reversed

H_CFG3 1
PAD87

PCI Express* Static x4 Lane Numbering Reversal.	
CFG[3]	1 : Normal operation 0 : Lane numbers reversed

H_CFG4 R269 1 2 1K
NA

LVDS NA
eDP Mount

Display Port Presence Strap(eDP enable)	
CFG[4]	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

FLEXComputing

Project Name : H710DI1	Title : CPU_4/7_RSVD_CFG	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 5 of 63	

POWER

CN_CPU801F

CPU_CORE

36A~52A

C1055 10UF/6.3V/0603
C459 10UF/6.3V/0603
C1062 10UF/6.3V/0603
C412 10UF/6.3V/0603
C460 10UF/6.3V/0603
C457 10UF/6.3V/0603
C461 10UF/6.3V/0603
C458 10UF/6.3V/0603
C436 10UF/6.3V/0603
C435 10UF/6.3V/0603
C1059 22UF/6.3V/0805
C1056 22UF/6.3V/0805
C416 22UF/6.3V/0805
C438 22UF/6.3V/0805
C437 22UF/6.3V/0805
C1057 22UF/6.3V/0805
C1058 22UF/6.3V/0805
C1063 22UF/6.3V/0805
C1065 22UF/6.3V/0805
C413 22UF/6.3V/0805
C414 22UF/6.3V/0805
C439 22UF/6.3V/0805
C440 22UF/6.3V/0805
C1066 22UF/6.3V/0805
C415 22UF/6.3V/0805
C408 330UF/2.5V/1.9mm
C487 330UF/2.5V/1.9mm
C1064 22UF/6.3V/0805
modify for FN

AG35 VCC1
AG34 VCC2
AG33 VCC3
AG32 VCC4
AG31 VCC5
AG30 VCC6
AG29 VCC7
AG28 VCC8
AG27 VCC9
AG26 VCC10
AF35 VCC11
AF34 VCC12
AF33 VCC13
AF32 VCC14
AF31 VCC15
AF30 VCC16
AF29 VCC17
AF28 VCC18
AF27 VCC19
AF26 VCC20
AD35 VCC21
AD34 VCC22
AD33 VCC23
AD32 VCC24
AD31 VCC25
AD30 VCC26
AD29 VCC27
AD28 VCC28
AD27 VCC29
AD26 VCC30
AC35 VCC31
AC34 VCC32
AC33 VCC33
AC32 VCC34
AC31 VCC35
AC30 VCC36
AC29 VCC37
AC28 VCC38
AC27 VCC39
AC26 VCC40
AA35 VCC41
AA34 VCC42
AA33 VCC43
AA32 VCC44
AA31 VCC45
AA30 VCC46
AA29 VCC47
AA28 VCC48
AA27 VCC49
AA26 VCC50
Y35 VCC51
Y34 VCC52
Y33 VCC53
Y32 VCC54
Y31 VCC55
Y30 VCC56
Y29 VCC57
Y28 VCC58
Y27 VCC59
Y26 VCC60
V35 VCC61
V34 VCC62
V33 VCC63
V32 VCC64
V31 VCC65
V30 VCC66
V29 VCC67
V28 VCC68
V27 VCC69
V26 VCC70
U35 VCC71
U34 VCC72
U33 VCC73
U32 VCC74
U31 VCC75
U30 VCC76
U29 VCC77
U28 VCC78
U27 VCC79
U26 VCC80
R35 VCC81
R34 VCC82
R33 VCC83
R32 VCC84
R31 VCC85
R30 VCC86
R29 VCC87
R28 VCC88
R27 VCC89
R26 VCC90
P35 VCC91
P34 VCC92
P33 VCC93
P32 VCC94
P31 VCC95
P30 VCC96
P29 VCC97
P28 VCC98
P27 VCC99
P26 VCC100

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

1.05VS

8.5A

MB Bottom Socket Cavity

C1061 22UF/6.3V/0805
C1069 22UF/6.3V/0805
C1071 22UF/6.3V/0805
C453 22UF/6.3V/0805
C469 22UF/6.3V/0805

MB Top Socket Cavity

C478 22UF/6.3V/0805
C1068 22UF/6.3V/0805
C1076 22UF/6.3V/0805
C1084 22UF/6.3V/0805
C1085 22UF/6.3V/0805
C523 22UF/6.3V/0805
C1082 22UF/6.3V/0805
C534 330UF/2.5V/1.9mm

VCCIO at CPU

AH13 VCCIO1
AH10 VCCIO2
AG10 VCCIO3
AC10 VCCIO4
Y10 VCCIO5
U10 VCCIO6
P10 VCCIO7
L10 VCCIO8
J14 VCCIO9
J13 VCCIO10
J12 VCCIO11
J11 VCCIO12
H14 VCCIO13
H12 VCCIO14
H11 VCCIO15
G14 VCCIO16
G13 VCCIO17
G12 VCCIO18
F14 VCCIO19
F13 VCCIO20
F12 VCCIO21
F11 VCCIO22
E14 VCCIO23
E12 VCCIO24
E11 VCCIO25
D14 VCCIO26
D13 VCCIO27
D12 VCCIO28
D11 VCCIO29
C14 VCCIO30
C13 VCCIO31
C12 VCCIO32
C11 VCCIO33
B14 VCCIO34
B12 VCCIO35
A14 VCCIO36
A13 VCCIO37
A12 VCCIO38
A11 VCCIO39
J23 VCCIO40

7/06 delet 330uF X2
poewr side have 330uF X3
(3x 330 µF for 2012 capable designs)
follow Huron River Platform Power Delivery (439028)

50 ohm reference GND

AJ29 VIDALERT# SVID_ALRT_R# R266 1 2 43_5% VR_SVID_ALERT# (42)
AJ30 VIDSCLK VR_SVID_CLK VR_SVID_CLK (42)
AJ28 VIDSOUT VR_SVID_DATA VR_SVID_DATA (42)

1.05VS
VR_SVID_ALERT# R305 1 2 75_1%
VR_SVID_DATA R306 1 2 130_1%

Layout Note:
Alert#(AJ29) signal must be routed between the Clock and Data lines to reduce the cross talk between them. Spacing recommendations from the “Asynchronous Signal General Routing Guideline” of the Huron River PDG have to be met.

AJ35 VCC_SENSE VCC_SENSE (42)
AJ34 VSS_SENSE VSS_SENSE (42)

B10 VCCIO_SENSE VCCIO_SENSE (44)
A10 VSSIO_SENSE VSSIO_SENSE (44)

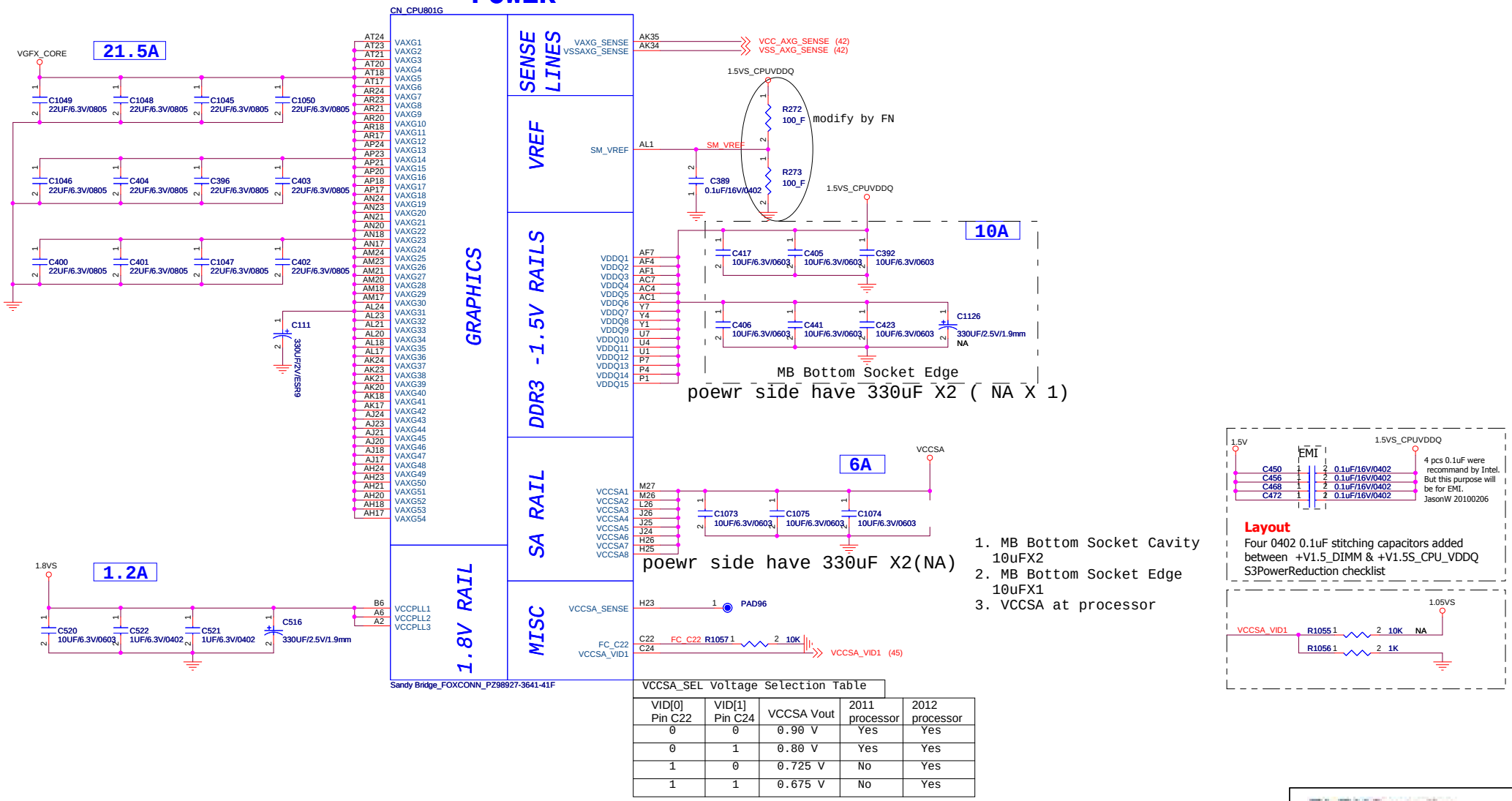
1.05VS
VCCIO_SENSE R343 1 2 10 NA
VSSIO_SENSE R345 1 2 10 NA

Sandy Bridge_FOXCONN_PZ98927-3641-41F

FLEXComputing

Project Name : H710DI1	Title : CPU_5/7_VCC_VCCIO
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 6 of 63

POWER



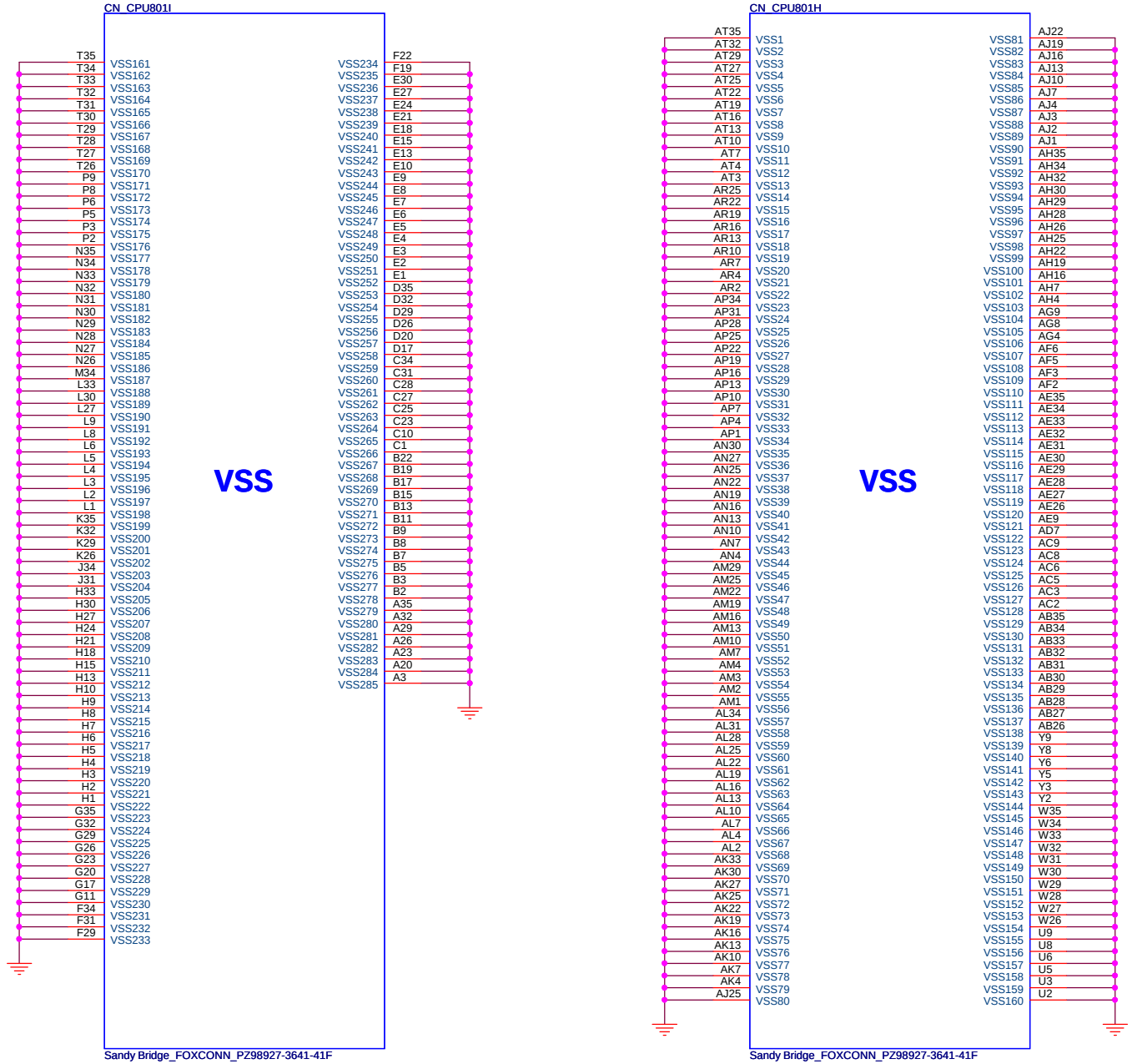
VCCSA_SEL Voltage Selection Table

VID[0] Pin C22	VID[1] Pin C24	VCCSA Vout	2011 processor	2012 processor
0	0	0.90 V	Yes	Yes
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes

Sandy Bridge_FOXCONN_PZ98927-3641-41F

FLEX Computing

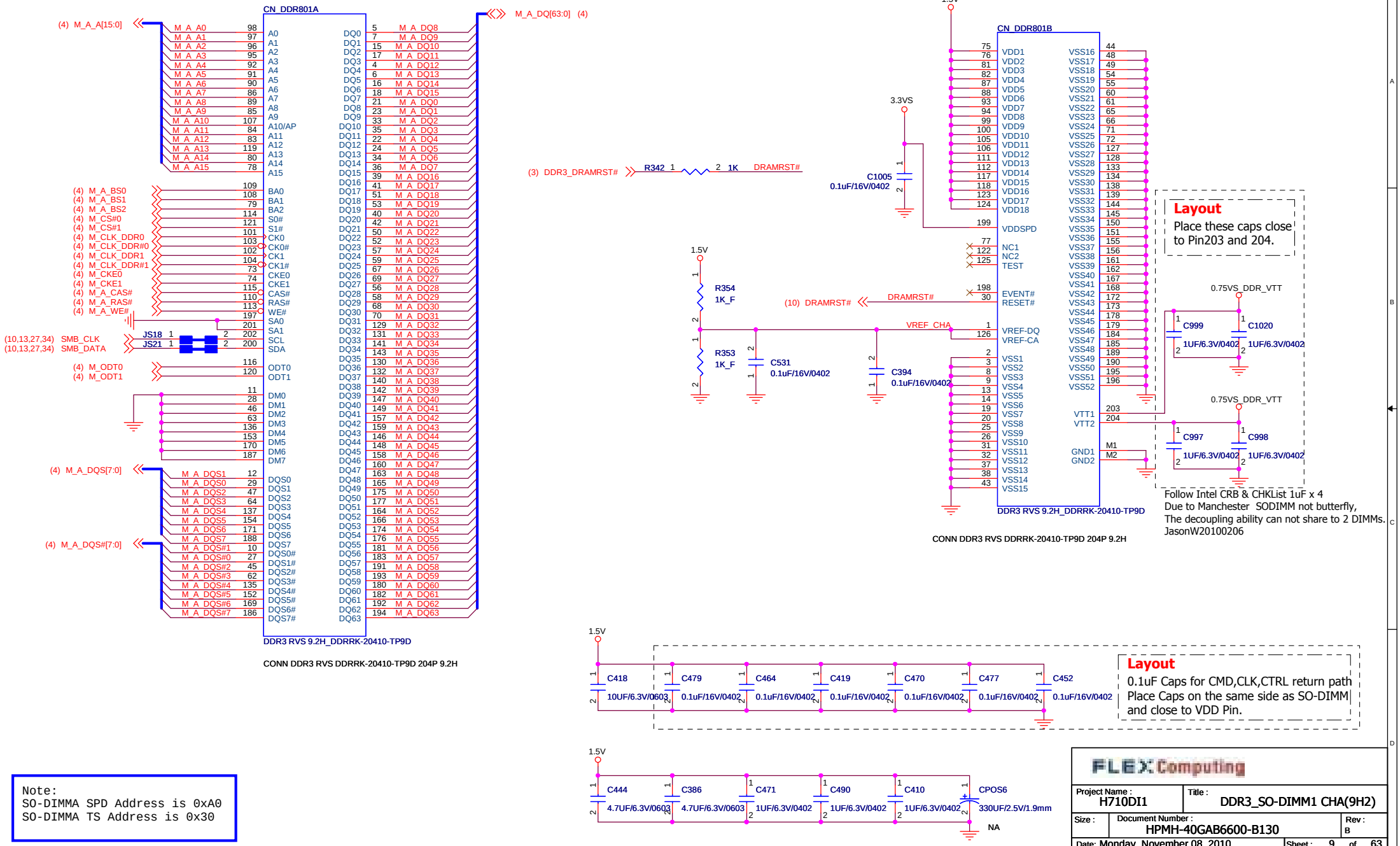
Project Name : H710DI1	Title : CPU_6/7_VGFX_VDDR3
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 7 of 63



FLEXComputing

Project Name : H710DI1	Title : CPU_7/7_VSS
Size :	Document Number : HPMH-40GAB6600-B130 / Rev : B
Date: Monday, November 08, 2010	Sheet : 8 of 63

Channel-A

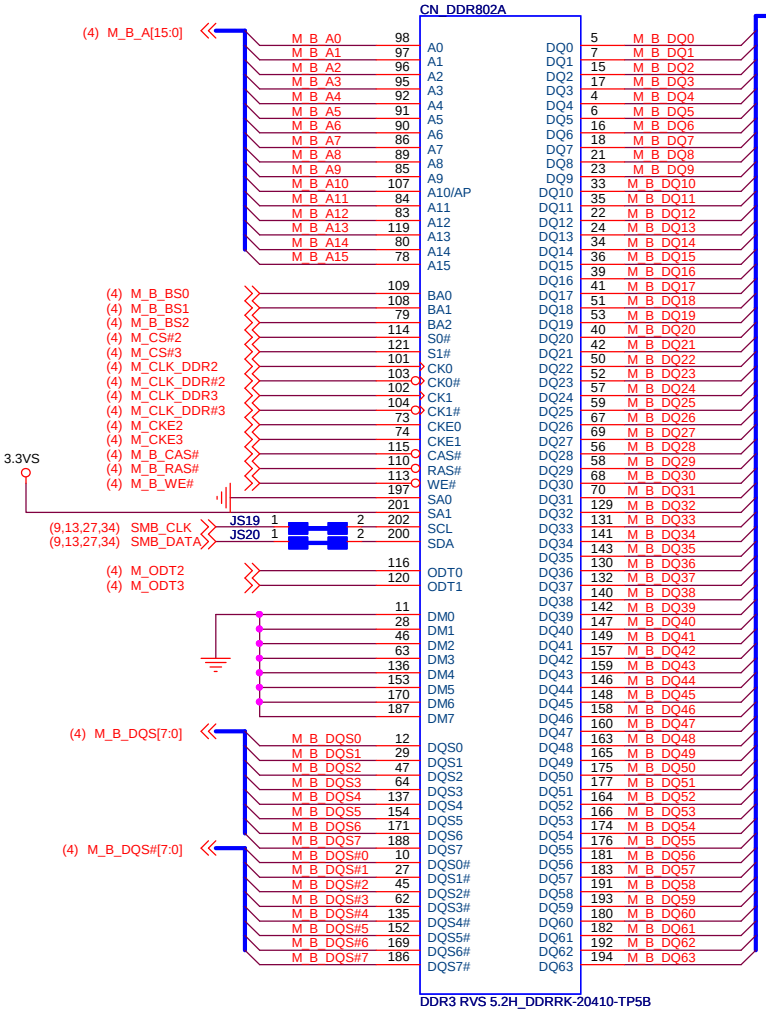


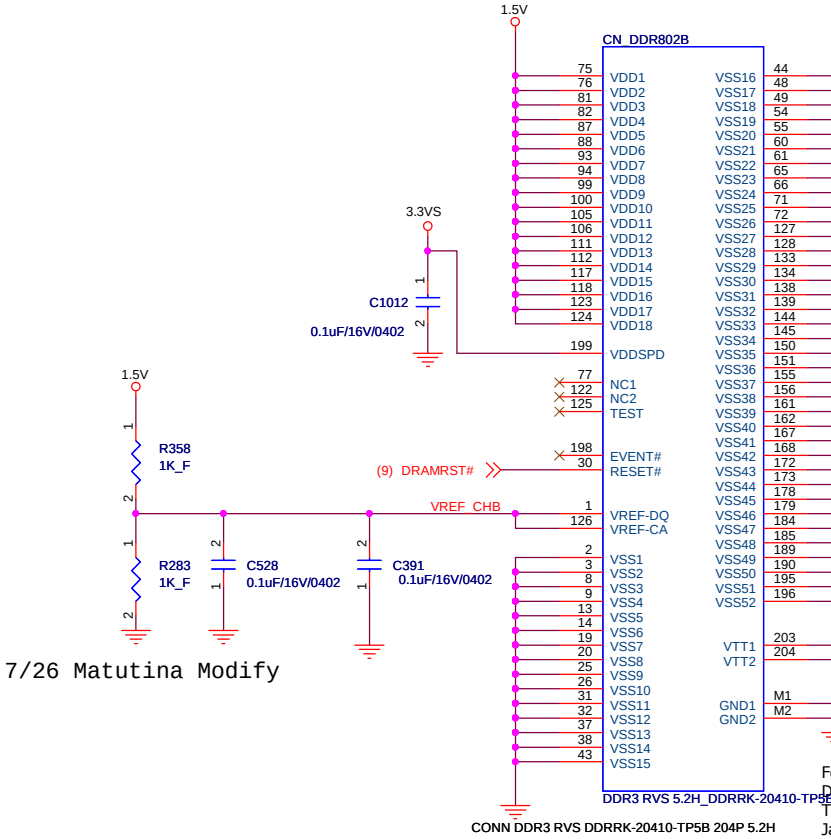
Note:
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

FLEXComputing

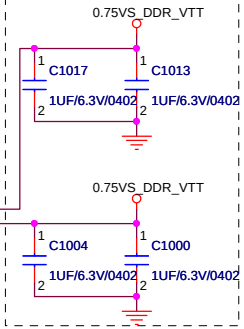
Project Name : H710DI1	Title : DDR3_SO-DIMM1 CHA(9H2)
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 9 of 63

Channel-B

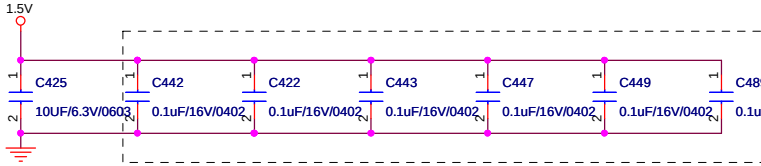




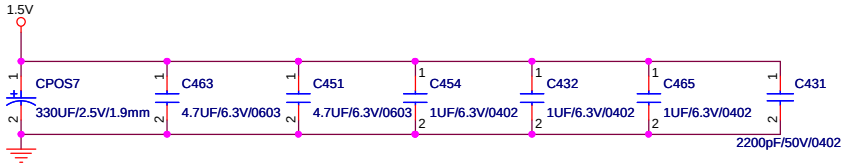
Layout
Place these caps close to Pin203 and 204.



Follow Intel CRB & CHKList 1uF x 4
Due to Manchester SODIMM not butterfly,
The decoupling ability can not share to 2 DIMMs.
JasonW20100206



Layout
0.1uF Caps for CMD,CLK,CTRL return path
Place Caps on the same side as SO-DIMM and close to VDD Pin .



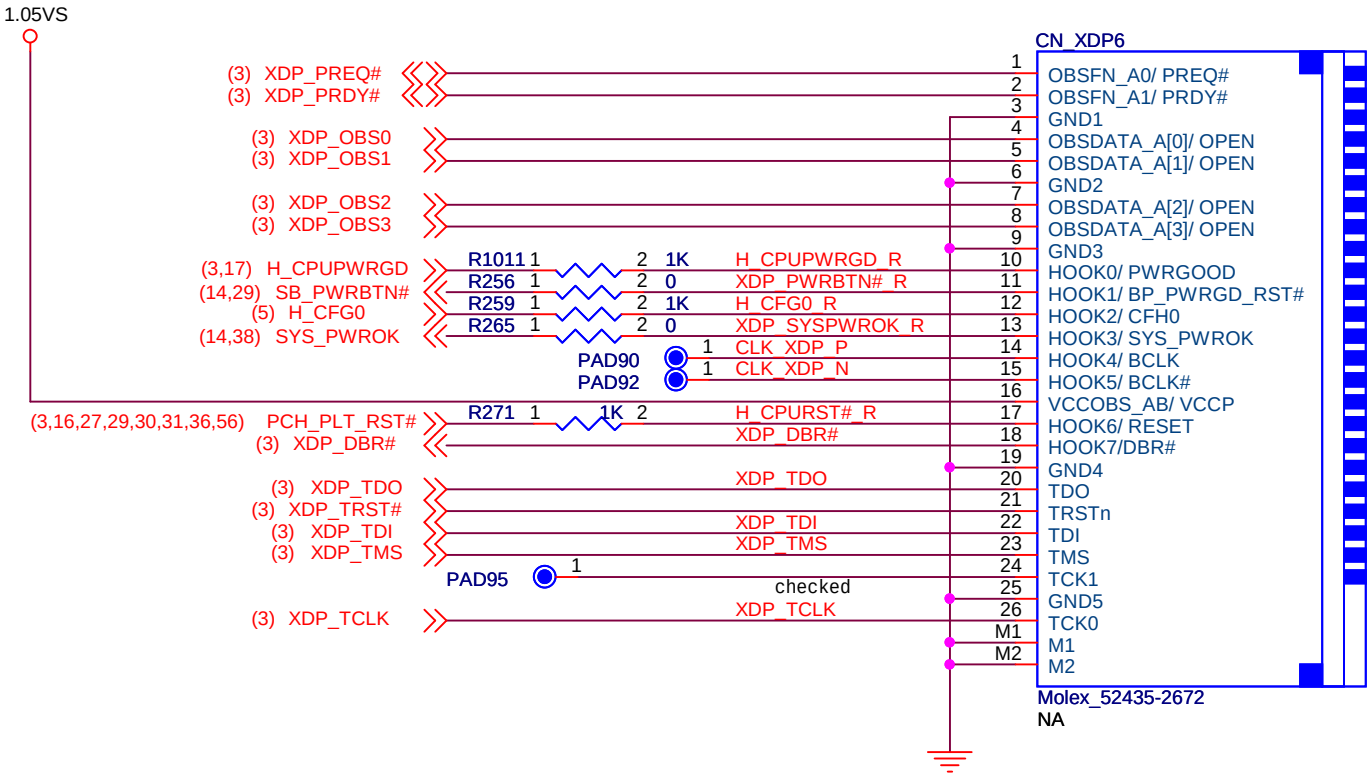
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

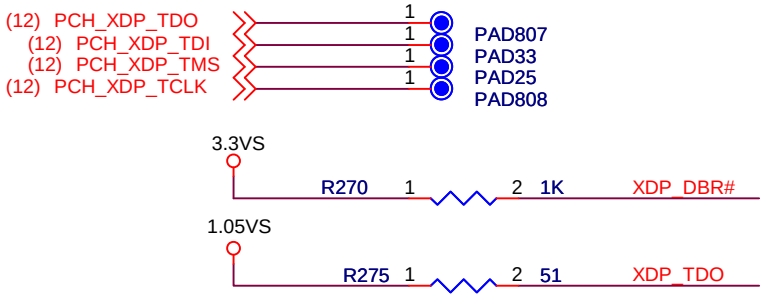
SO-DIMM Address		
SA0_DIM0 = 0, SA1_DIM0 = 0	SPD	0xA0
	TS	0x30
SA0_DIM1 = 0, SA1_DIM1 = 1	SPD	0xA4
	TS	0x34

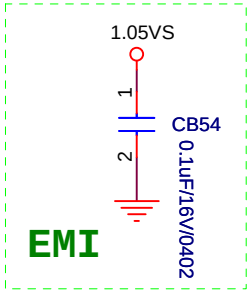
FLEXComputing

Project Name : H710DI1	Title : DDR3_SO-DIMM2 CHB(5H2)
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 10 of 63

Debug Port







FLEX Computing

Project Name : H710DI1	Title : XDP(PROCESSOR / PCH)
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 11 of 63

COUGARPOINT (HDA,JTAG,SPI,SATA)

Internal Pull-Up and Pull-Down

	Mark
Pull-Up	P+
Pull-Down	P-

U811A

RTC: RTCX1 A20, RTCX2 C20, RTCRST# D20, SRTCRST# G22, INTRUDER# K22, INTVRMEN C17

HDA: HDA_BCLK N34, HDA_SYNC L34, SPKR T10, HDA_RST# K34, HDA_SDIN0 E34, HDA_SDIN1 G34, HDA_SDIN2 C34, HDA_SDIN3 A34, HDA_SDO A36, HDA_DOCK_EN# / GPIO33 C36, HDA_DOCK_RST# / GPIO13 N32

JTAG: JTAG_TCK J3, JTAG_TMS H7, JTAG_TDI K5, JTAG_TDO H1

SPI: SPI_CLK T3, SPI_CS0# Y14, SPI_CS1# T1, SPI_MOSI V4, SPI_MISO U3

LPC: FWH0 / LAD0 C38, FWH1 / LAD1 A38, FWH2 / LAD2 B37, FWH3 / LAD3 C37, FWH4 / LFRAME# D36, LDRQ0# E36, LDRQ1# / GPIO23 K36, SERIRQ V5

SATA: SATA0RXN AM3, SATA0RXP AM1, SATA0TXN AP7, SATA0TXP AP5, SATA1RXN AM10, SATA1RXP AM8, SATA1TXN AP11, SATA1TXP AP10, SATA2RXN AD7, SATA2RXP AD5, SATA2TXN AH5, SATA2TXP AH4, SATA3RXN AB8, SATA3RXP AB10, SATA3TXN AF3, SATA3TXP AF1, SATA4RXN Y7, SATA4RXP Y5, SATA4TXN AD3, SATA4TXP AD1, SATA5RXN Y3, SATA5RXP Y1, SATA5TXN AB3, SATA5TXP AB1, SATAICOMPO Y11, SATAICOMPI Y10, SATA3RCOMPO AB12, SATA3COMPI AB13, SATA3RBIAS AH1, SATALED# P3, SATA0GP / GPIO21 V14, SATA1GP / GPIO19 P1

CougarPoint_Rev_1p0

To HDD 1 for 15''

To HDD 2 for 17''

H61 SATA ports 2 and 3 are disabled

For BIOS power saving check

7/14

To ODD

TO INDICATE LED BOARD

HPMH-10-0010000113G	IC Cougar Point PCH QNDL FCBGA989(MH65)B1
HPMH-10-0010000115G	IC Cougar Point PCH QNJG FCBGA989(HM67)B2
HPMH-10-0010000116G	IC Cougar Point PCH QNJH FCBGA989(HM65)B2
HPMH-10-0010000117G	IC Cougar Point PCH SLH9D FCBGA989(HM65)B2

STRAP and Audio

STRAP

EMI

VTAP Assumed as 1.1V

Close PCH

Design Guide 1.2 (#436735)
HDA_SYNC Potential Leakage Concern

17'' MOUNTED
15'' NA

15'' MOUNTED
17'' NA

INTVRMEN- Integrated SUS 1.05V VRM Enable

32Mbit (4M Byte) SPI

U814 EN25F32-100HIP HPMH-14-0090000064G

BIOS1 — BIOS Label — HPMH-B2685310G00016

HDMI0 — HDMI Label — HPMH-B2995007G00001

PCB1 — PCB — HPMH-41-AB6200-C00G

15'' RTC2 — RTC — BTRY LITHIUM COIN CR2032 JHT 3V 220mAh HPMH-83-2030000007G

17'' RTC3 — RTC_17inch — CABLE FOR RTC G AB650 HPMH-B3035050G00009 NA

FLEX Computing

Project Name : H710DI1	Title : PCH_1/10_LPC_ RTC_ HDA_SATA
Size :	Document Number : HPMH-40GAB6600-B130 — Rev : B
Date: Monday, November 08, 2010	Sheet : 12 of 63

COUGARPOINT (PCI-E,SMBUS,CLK)

PCI-E 2.0 x1	Usage
Lane 1	LAN
Lane2	WLAN
Lane 3	Card Reader
Lane 4	USB3.0
Lane 5	
Lane 6	
Lane 7	
Lane 8	

LAN

WLAN

Card Reader

USB3.0

U811B

PCI-E*

SMBUS

Controller Link

CLOCKS

FLEX CLOCKS

For BIOS power saving check

7/19 Matutina Modify

TO Audio
TO SO-DIMM
TO WLAN

TO KBC

TO dGPU

CRB use this pin to control DDR3_DRAMRST#

Clock termination for FCIM
1. External clock present: 10k unstuffed
2. External clock no present: 10k stuffed

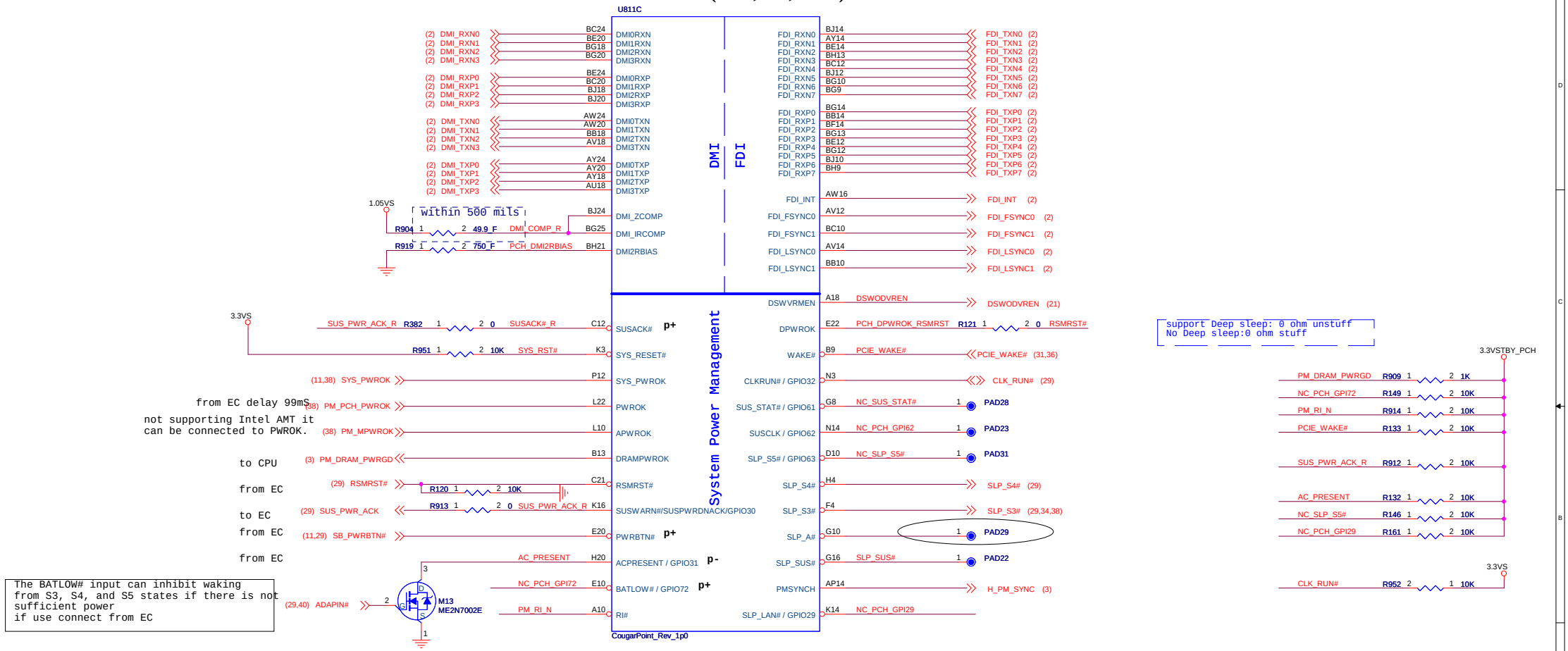
EMI

CougarPoint_Rev_1p0

FLEX Computing

Project Name : H710DI1	Title : PCH_2/10_PCIE_ SMBUS_ CLK
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 13 of 63

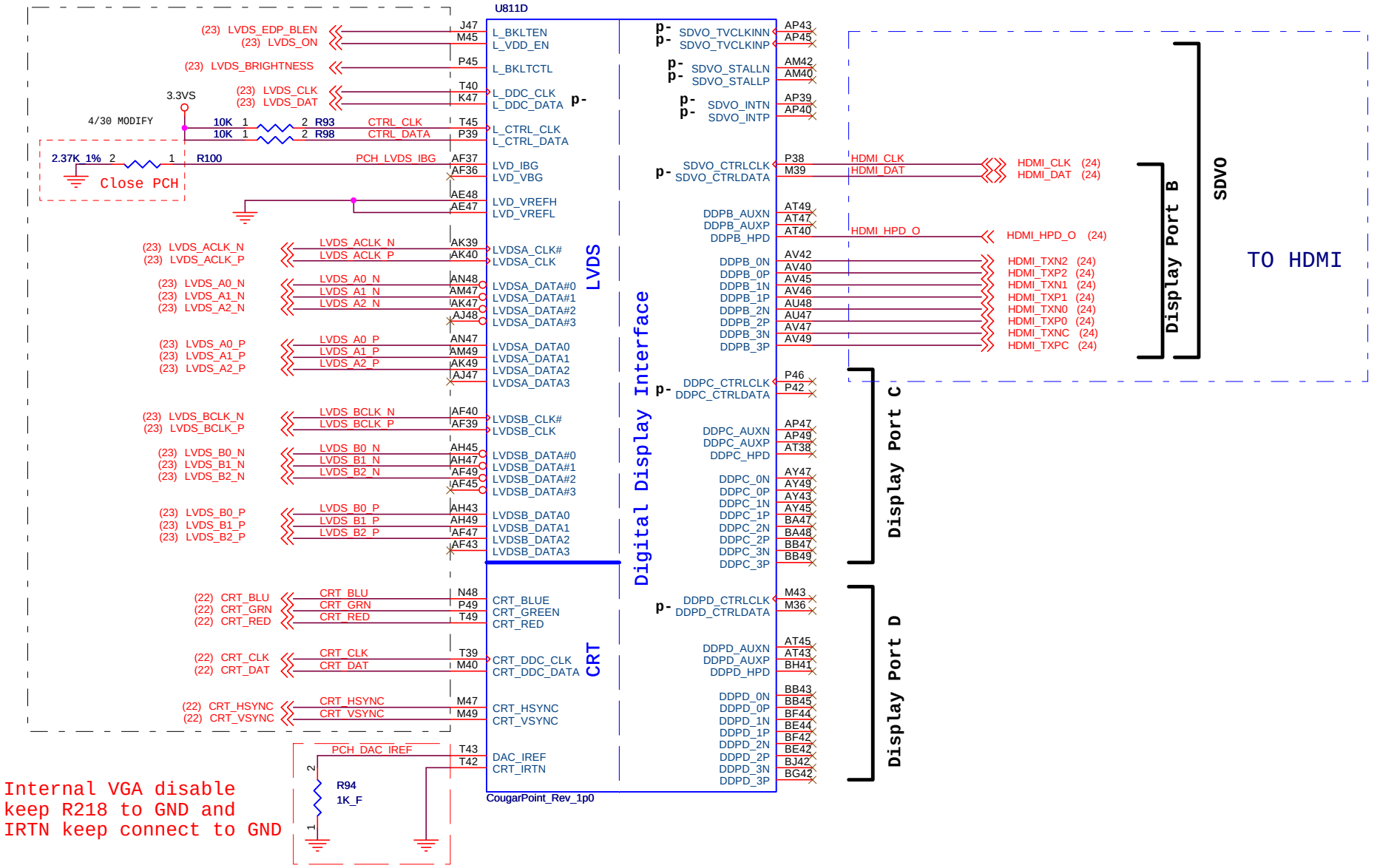
COUGARPOINT (DMI,FDI,GPIO)



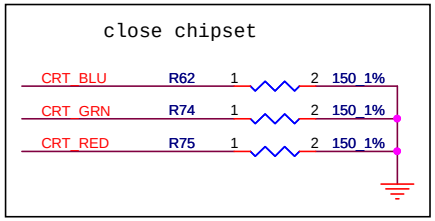
FLEXComputing

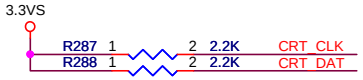
Project Name : H710DI1	Title : PCH_3/10_DMI_ FDI_SPM	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 14 of 63	

COUGARPOINT (LVDS,DDI)



close chipset

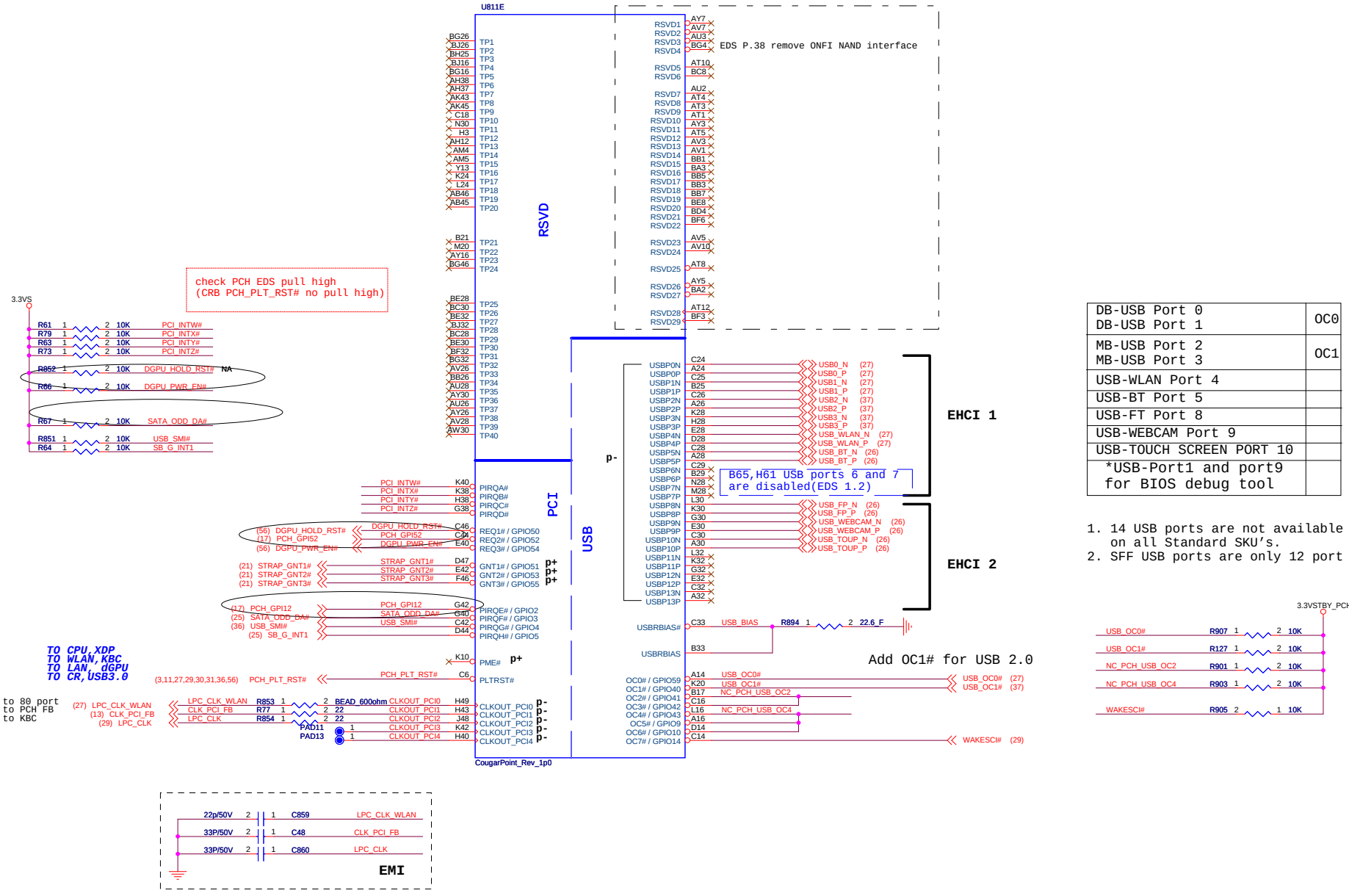




FLEXComputing

Project Name : H710DI1	Title : PCH_4/10_CRT_ LVDS_DDI
Size :	Document Number : HPMH-40GAB6600-B130 / Rev : B
Date: Monday, November 08, 2010	Sheet : 15 of 63

COUGARPOINT (PCI,USB,NVRAM)



DB-USB Port 0 DB-USB Port 1	OC0
MB-USB Port 2 MB-USB Port 3	OC1
USB-WLAN Port 4	
USB-BT Port 5	
USB-FT Port 8	
USB-WEBCAM Port 9	
USB-TOUCH SCREEN PORT 10	
*USB-Port1 and port9 for BIOS debug tool	

1. 14 USB ports are not available on all Standard SKU's.
2. SFF USB ports are only 12 port

Project Name : H710DI1		Title : PCH_5/10_PCI_USB_NVRAM	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 16 of 63	

COUGARPOINT (GPIO,VSS_NCTF,RSVD)

GPI048 SV_SET_UP	0ohm NA High = Strong (Default) 0ohm Mounted Low = Weak

PWA rev	GPI13(RJ807)	GPI57(RJ6)
SI	0	0
PV	0	1
MV	1	0
Reserved	1	1

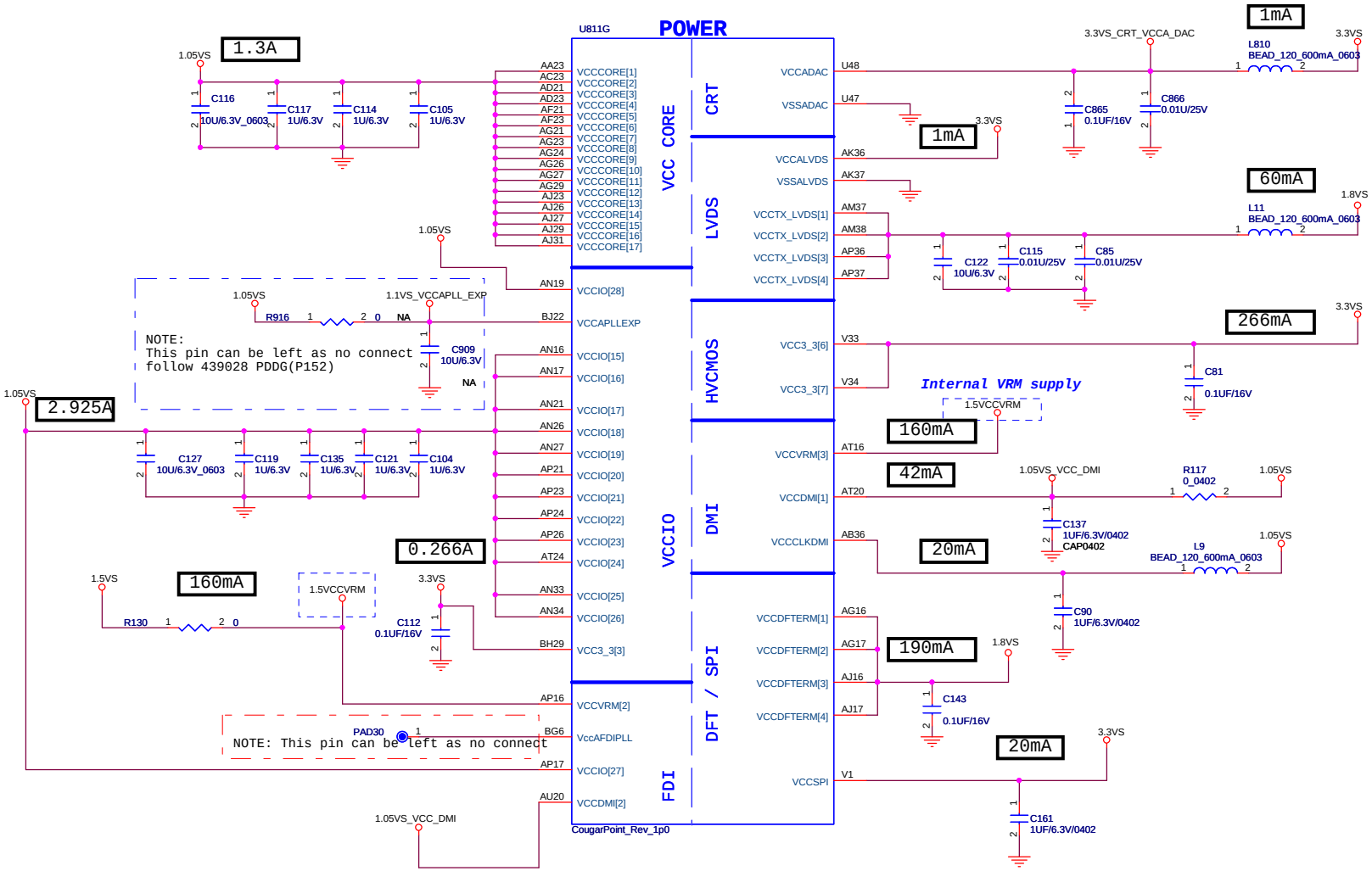
DC or QC HM65 or HM67	GPI12(RJ809) Bit 1	GPI52(RJ808) Bit 0
DC CPU(35W) HM65 PCH	0	0
DC CPU(35W) HM67 PCH	0	1
QC CPU(45W) HM67 PCH	1	0
QC CPU(45W) HM67 PCH	1	1

RJ806	RJ803	RJ804	RJ7	platform	platform ID	SI	PV	
0(B)	0(B)	0(B)	0(B)	Grant 1.0 SG w/ AMD Seymour & Intel Graphic (Beats)	0x1656			
0(B)	0(B)	0(B)	1(A)	Grant 1.0 SG w/ AMD Whistler & Intel Graphic (Beats)	0x1657	SKU4		
0(B)	0(B)	1(A)	0(B)	Grant 1.0 UMA (Beats)	0x1658	SKU2		
0(B)	0(B)	1(A)	1(A)	Grant 1.0 SG w/ AMD Seymour & Intel Graphic (non Beats/Dolby)	0x3581	SKU3		
0(B)	1(A)	0(B)	0(B)	Grant 1.0 SG w/ AMD Whistler & Intel Graphic (non Beats/Dolby)	0x3582			
0(B)	1(A)	0(B)	1(A)	Grant 1.0 UMA (non Beats/Dolby)	0x3583	SKU1		
0(B)	1(A)	1(A)	0(B)	Bogart 1.0 SG w/ AMD Seymour & Intel Graphic+Subwoofer(Beats)	0x1659	SKU5,6		
0(B)	1(A)	1(A)	1(A)	Bogart 1.0 SG w/ AMD Whistler & Intel Graphic+Subwoofer(Beats)	0x165A	SKU7,8		

FLEXComputing

Project Name : H710DI1	Title : PCH_6/10_CPU_GPIO_VSS_RSD	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 17 of 63	

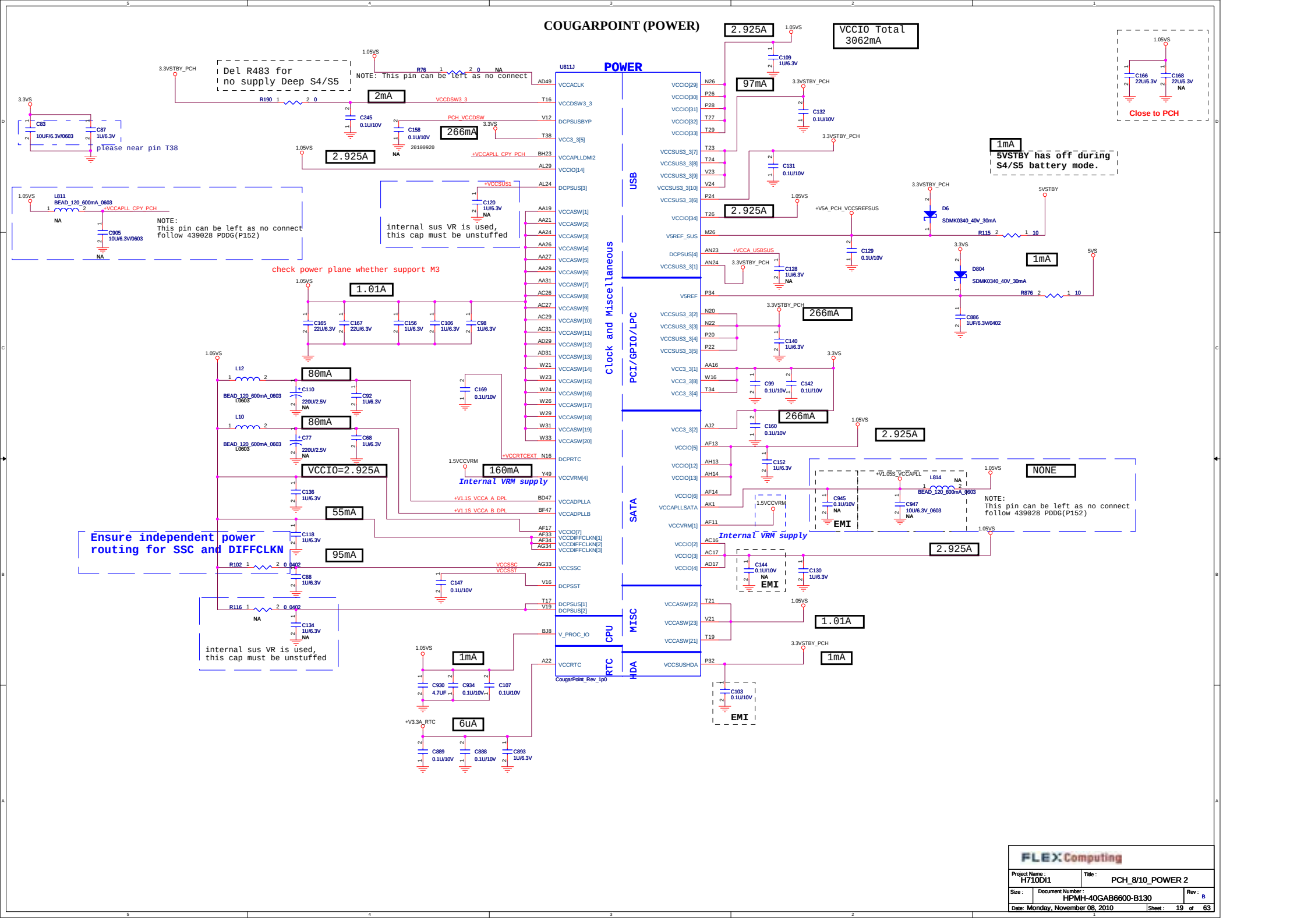
COUGARPOINT (POWER)



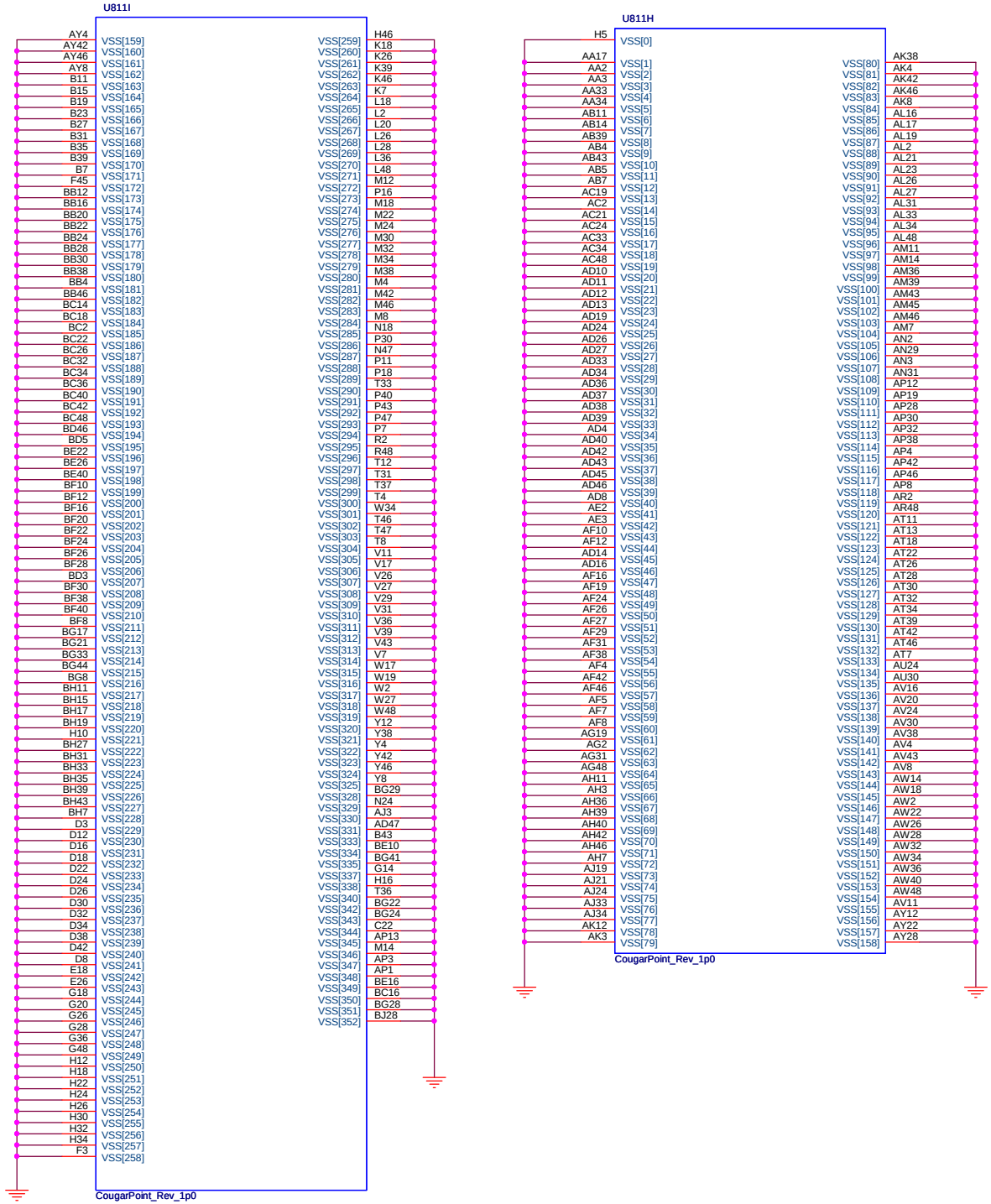
FLEX Computing

Project Name : H710DI1	Title : PCH_7/10_POWER 1	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 18 of 63	

COUGARPOINT (POWER)



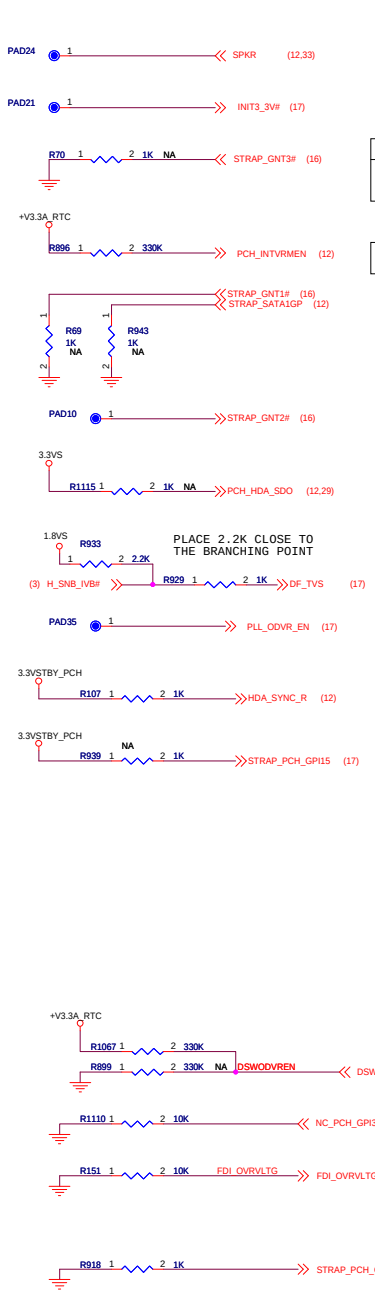
COUGARPOINT (GND)



FLEX Computing

Project Name : H710DI1	Title : PCH_9/10_GND	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 20 of 63	

Signal	Usage	When Sampled	Internal PULL	Comment
SPKR	No Reboot	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: If the signal is sampled high, this indicates that the system is strapped to the No Reboot mode L: Cougar Point will disable the TCO Timer system reboot feature (Chipset Config Registers: Offset (3410h:Bit 5). **Default**
INIT3_3V#	Reserved	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	This signal should not be pulled low
GNT[3]#/ GPIO[55]	Top-Block Swap Override	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Top Block Swap Mode disabled **Default** L: If the signal is sampled low, this indicates that the system is strapped to the Top Block swap mode
INTVRMEN	Integrated 1.05 V VRM Enable / Disable	Always	NA	H: Integrated 1.05V VRMs enabled **Default** This signal should always be External pulled high L: Integrated 1.05V VRMs disabled
GNT1#/ GPIO51/ SATA1GP/ GPIO19	Boot BIOS Strap bit [1] BBS[1] Boot BIOS Strap bit[0] BBS[0]	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	GNT1# SATA1GP Boot BIOS Location 0 0 LPC 0 1 Reserved 1 0 PCI 1 1 SPI **Default**
GNT2#/ GPIO53	ESI Strap (Server Only)	Rising edge of PWROK	Internal PU (The internal PU is disabled after PLTRST# de-asserts)	H: Should not be pulled low for desktop and mobile **Default** ESI compatible mode is for server platforms only. L: Configures DMI for ESI compatible operation
HDA_SDO	Flash Descriptor Security Override/ ME Debug Mode	Rising edge of RSMRST#	Internal PD	H: If sampled high,the Flash Descriptor Security will be overridden. L: If strap is sampled low, (Default) the security measures defined in the Flash Descriptor will be in effect. This signal should not be pulled high
DF_TVS	DMI and FDI Tx/ Rx Termination Voltage	Rising edge of PWROK	Internal PD	The internal pull-down is disabled after PLTRST# deasserts
GPIO28	On-Die PLL Voltage Regulator	Rising edge of RSMRST# pin	Internal PU	H: The On-Die PLL voltage regulator is enabled when sampled high **Default** L: When sampled low the On-Die PLL Voltage Regulator is disabled
HDA_SYNC	On-Die PLL Voltage Regulator Voltage Select	Rising edge of RSMRST# pin	Internal PD	H: On-Die PLL VR is supplied by 1.5 V **Default** L: On-Die PLL VR is supplied by 1.8 V
GPIO15	TLS Confidentiality	Rising edge of RSMRST# pin	Internal PD The weak internal pull-down is disabled after RSMRST# deasserts	H: Intel ME Crypto TLS cipher suite with confidentiality L: Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality **Default**
L_DDC_DATA	LVDS Detected	Rising edge of PWROK	Internal PD The internal pull-down is disabled after PLTRST# deasserts.	H:LVDS is detected **Default** L:LVDS is not detected
SDVO_CTRLDATA	Port B Detected	Rising Edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H:Port B is detected L:Port B is not detected **Default**
DDPC_CTRLDATA	Port C Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port C is detected L: Port C is not detected **Default**
DDPD_CTRLDATA	Port D Detected	Rising edge of PWROK	Internal PD (The internal PD is disabled after PLTRST# de-asserts)	H: Port D is detected L: Port D is not detected **Default**
DSWVRMEN	Deep S4/S5 Well On-Die Voltage Regulator Enable	Always	NA	If strap is sampled high, the Integrated Deep S4/S5 Well (DSW) On-Die VR mode is enabled.
SATA2GP/ GPIO36	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: This signal should not be pulled high when strap is sampled.
SATA3GP/ GPIO37	Reserved	Rising edge of PWROK	Internal PD (The internal pull-down is disabled after PLTRST# deasserts.)	NOTE: NOTE: This signal should not be pulled high when strap is sampled.
GPIO8	Reserved	Rising edge of RSMRST#	Internal PU (Pull-up is disabled after RSMRST# is deasserted.)	NOTE: This signal should not be pulled low



NO REBOOT	
NA	Low=Disable(Default)
MOUNTED	High=Enable

A16 swap override Strap	
STP_A16OVR	Low = A16 swap override High = Default

INTVRMEN- Integrated SUS 1.05V VRM Enable

Flash Descriptor Security Overide		
	NA	Low=Disable(Default)
PCH_HDA_SDO	MOUNTED	High=Enable

DMI & FDI Termination Voltage	
DF_TVS	Set to Vss when LOW Set to Vcc when HIGH

PLL ON DIE VR ENABLE	
PLL_ODVR_EN	ENABLE- UNSTUFF DISABLE-STUFF

HR only support 1.5 V
HDA_SYNC need PU to HDA SUS rail through 1k ohm for 451710_451710 SPEC

DSWODVREN - On Die DSW VR Enable	
Pull High	Enable (Default)
Pull Down	Disable

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

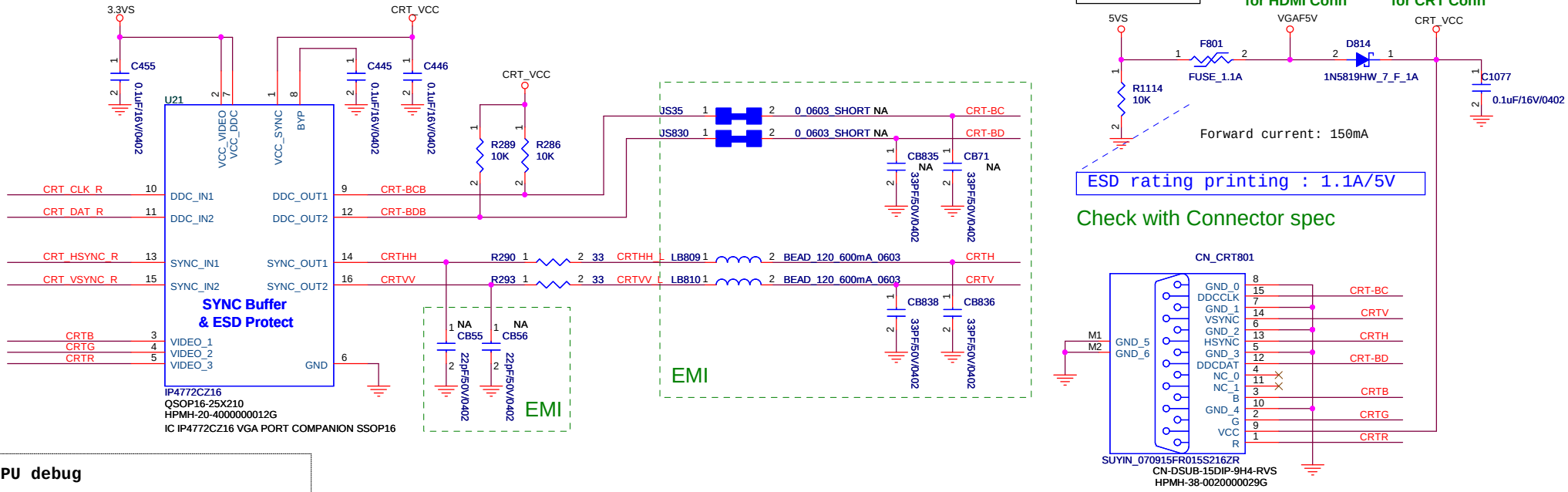
FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

GPIO8 Integrated Clock Chip Enable
High : Disable Low : Enable(default)

FLEXComputing

Project Name : H710DI1	Title : PCH_10/10_STRAP	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 21 of 63	

D-Sub



5V/1.1A

for HDMI Conn

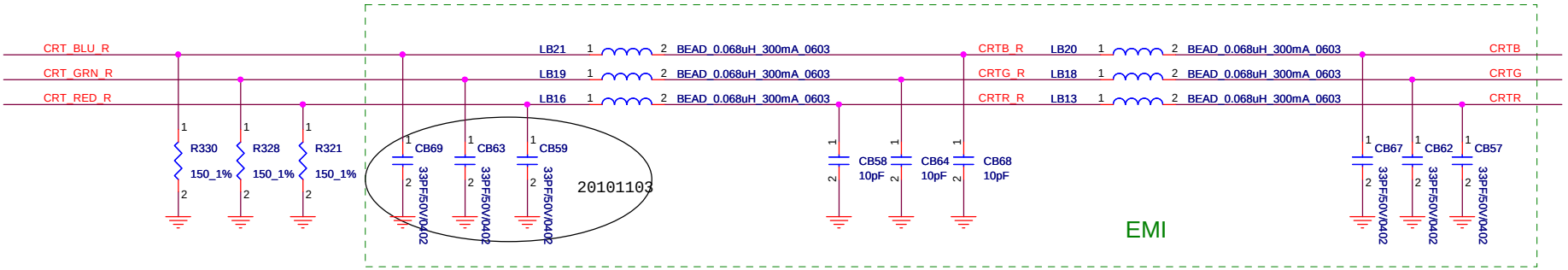
for CRT Conn

ESD rating printing : 1.1A/5V

Check with Connector spec

For DGPU debug

(15) CRT_CLK	JS825	1	2 NA	CRT_CLK_R
(15) CRT_DAT	JS826	1	2 NA	CRT_DAT_R
(15) CRT_HSYNC	JS828	1	2 NA	CRT_HSYNC_R
(15) CRT_VSYNC	JS827	1	2 NA	CRT_VSYNC_R

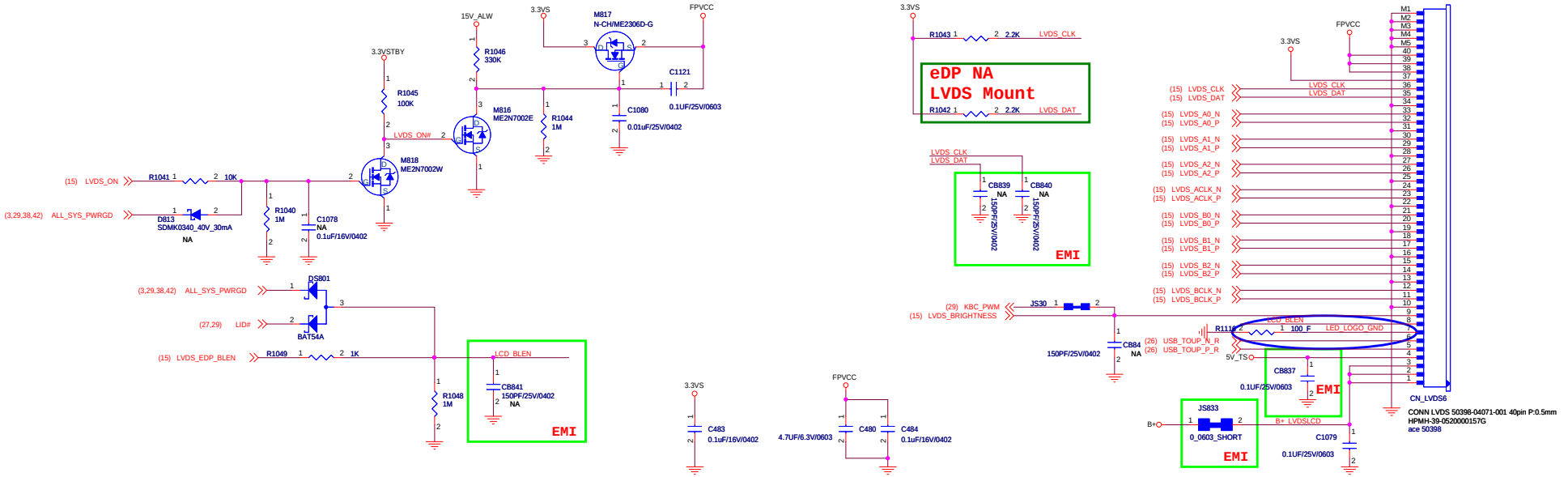


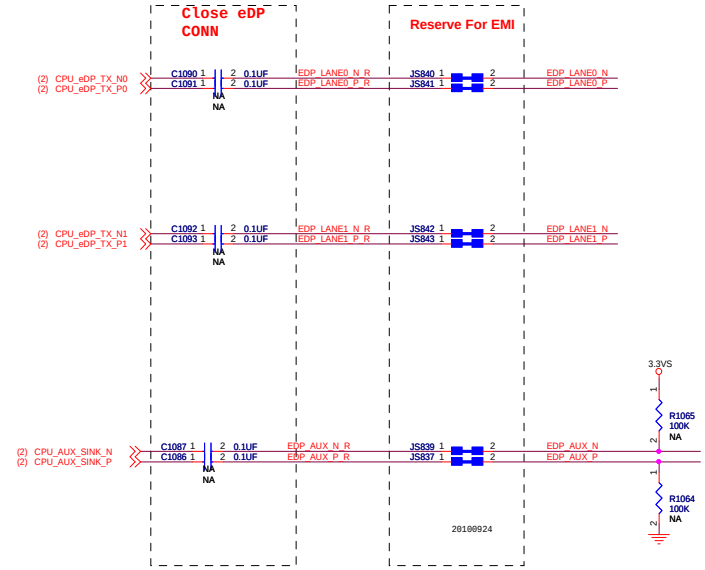
For DGPU debug

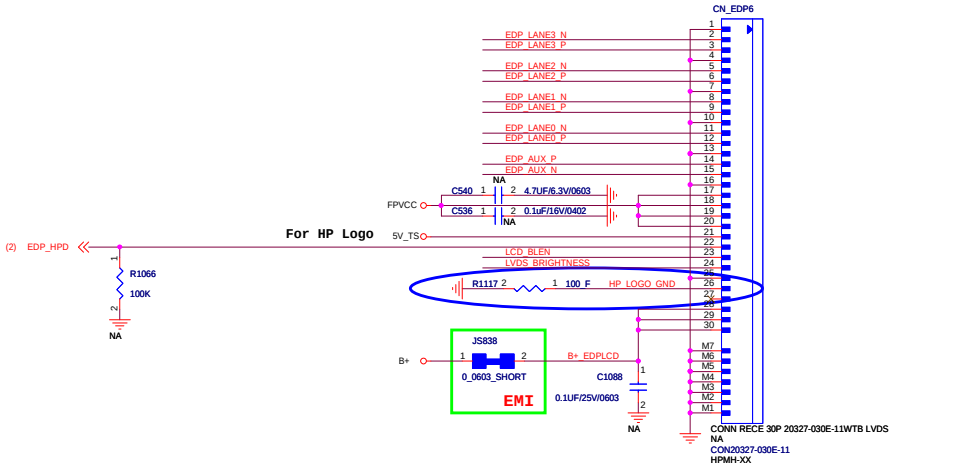
(15) CRT_BLU	JS832	1	2 NA	CRT_BLU_R
(15) CRT_GRN	JS831	1	2 NA	CRT_GRN_R
(15) CRT_RED	JS829	1	2 NA	CRT_RED_R

FLEXComputing

Project Name : H710DI1	Title : CRT CONN	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 22 of 63	







1. Check pin definition of eDP panel spec.
2. Confirm connector PN

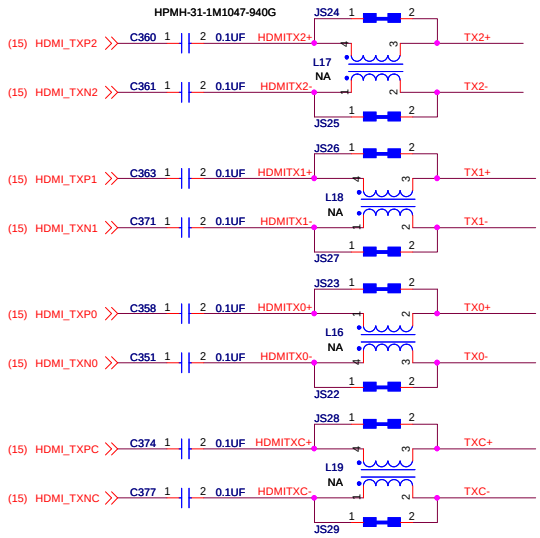
FLEX Computing		
Project Name : H710DI1	Title : eDP_LVDS CONN_HP Logo	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 23 of 63	

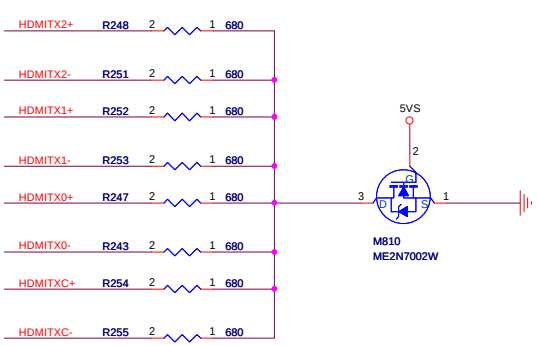
HDMI

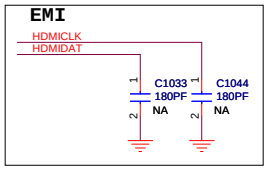
CLOSE to CN_HDMI1

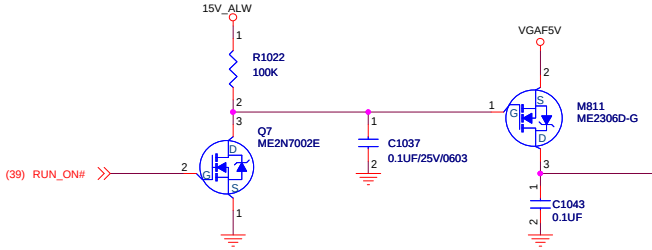
HPMH-32-4000000104G

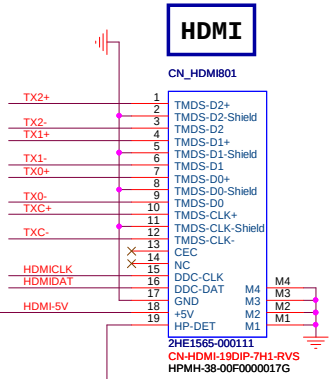
Intel Huron River: 680 ohm
AMD Danube: 715 ohm
AMD Sabine: 715 ohm

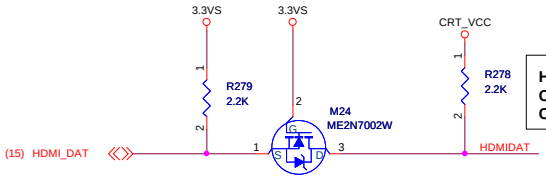




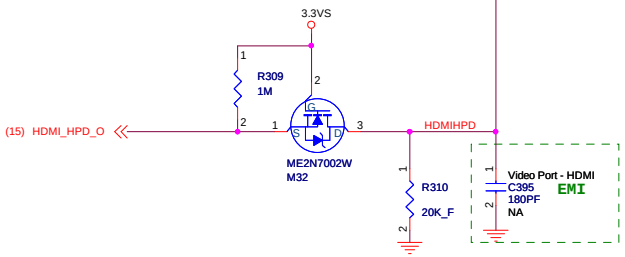


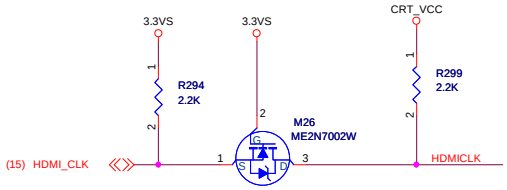






HDMI test
C1 -- Cp=45pf
C2 -- Cp=46pf (spec<50pf)



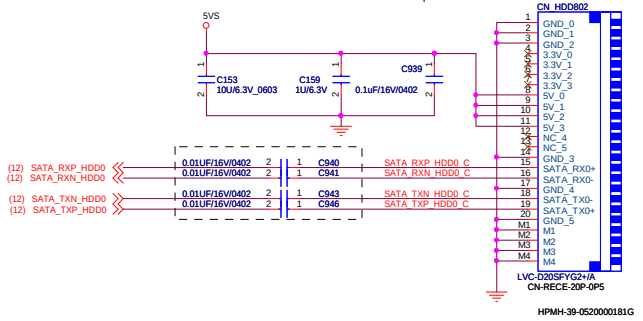


FLEX Computing

Project Name : H710DI1	Title : HDMI CONN
Size : Custom	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 24 of 63

HDD

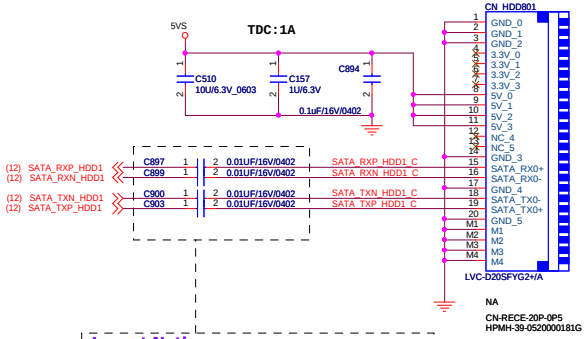
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist



2nd HDD

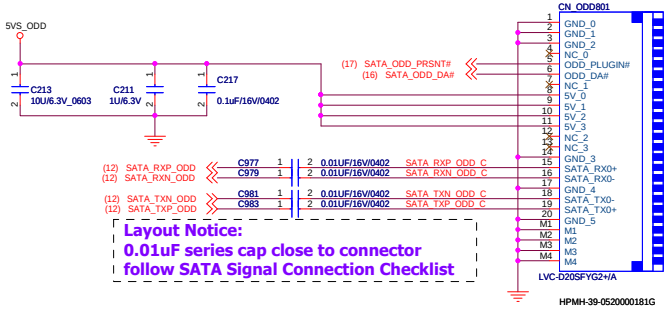
FOR 17" MB USE WTB CONNECTOR

CONN SPEC:0.3A/PIN



Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

ODD



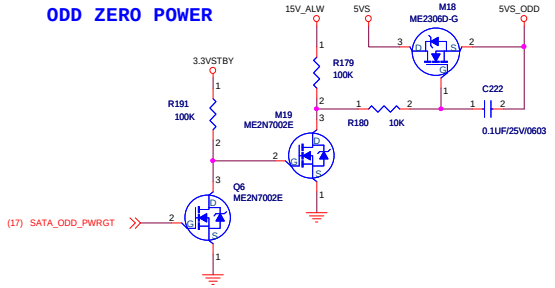
Layout Notice:
0.01uF series cap close to connector
follow SATA Signal Connection Checklist

TDC:2A

Change to Cable type Conn

ODD Zero Power

Check if meet max current!!

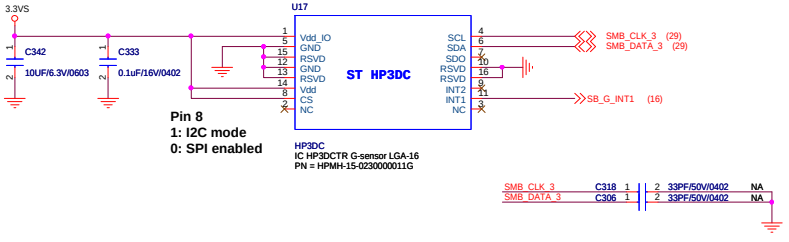


G-Sensor

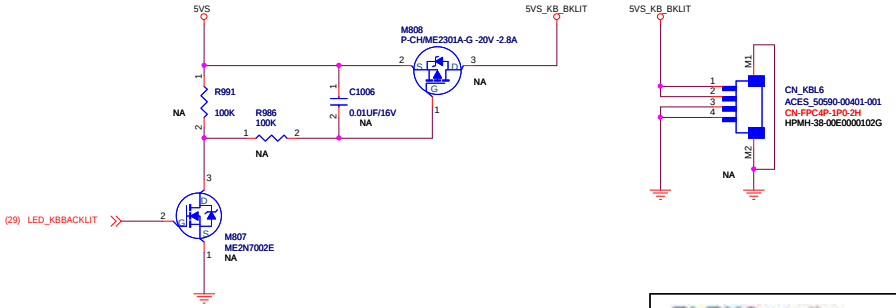
G-SENSOR

ST HP3DC

3.3VS
ADDR: 0011000x(30h) - SDO PD
ADDR: 0011010x(32h) - SDO NC
SINK: ??mA@VoL=0.33V(MAX)



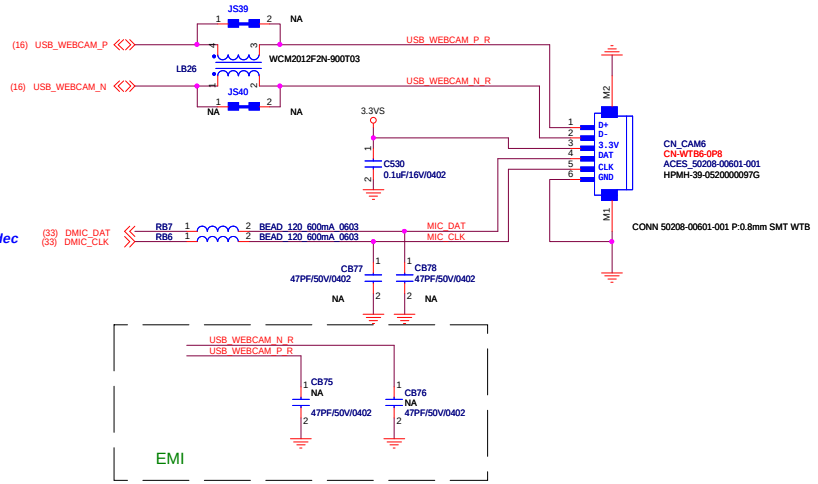
KB Backlit



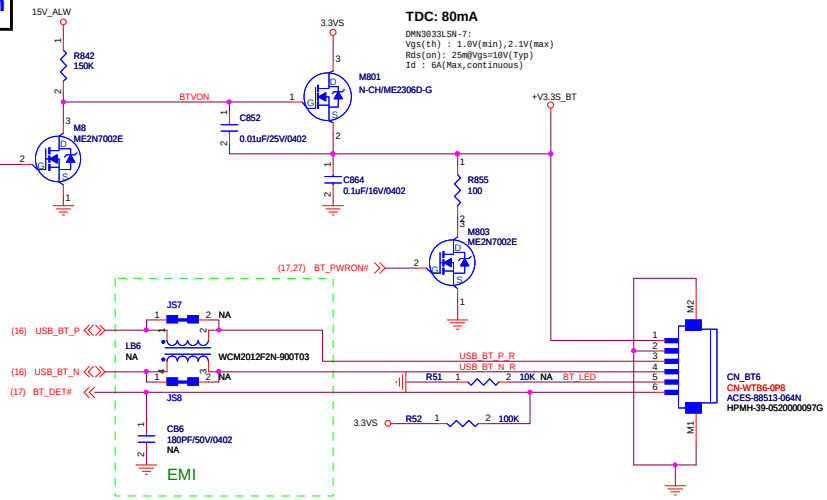
FLEX Computing

Project Name : H710DI1	Title : HDD_ODD_G-Sensor_KB BKL	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 25 of 63	

Web CAM



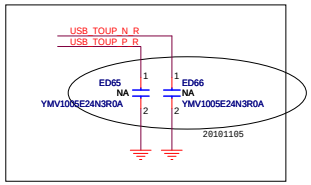
Blue Tooth

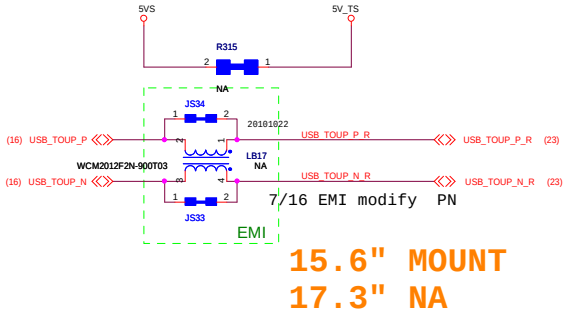


TouchScreen
(Module CONN)

Touch Screen power is 5V type

Peak 200mW 40mA

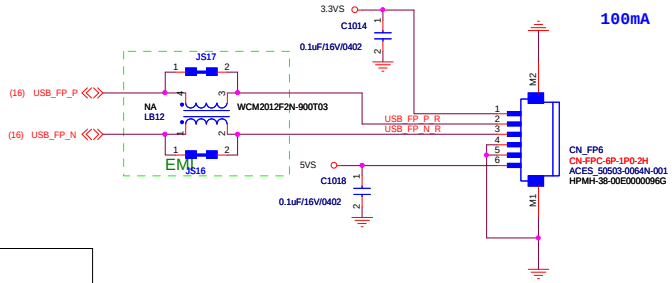


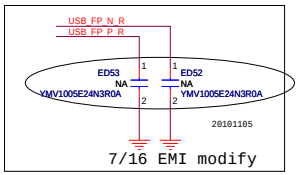


15.6" MOUNT
17.3" NA

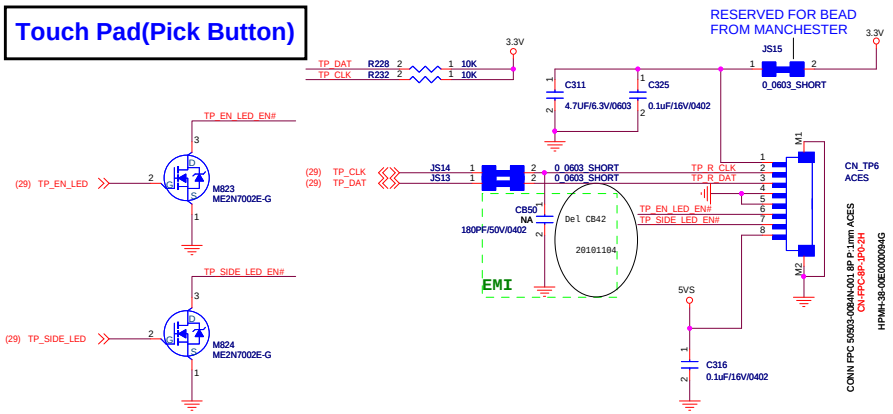
Finger Print

100mA

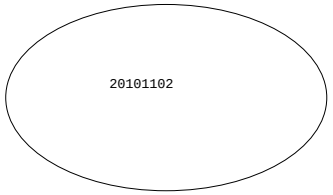




Touch Pad(Pick Button)



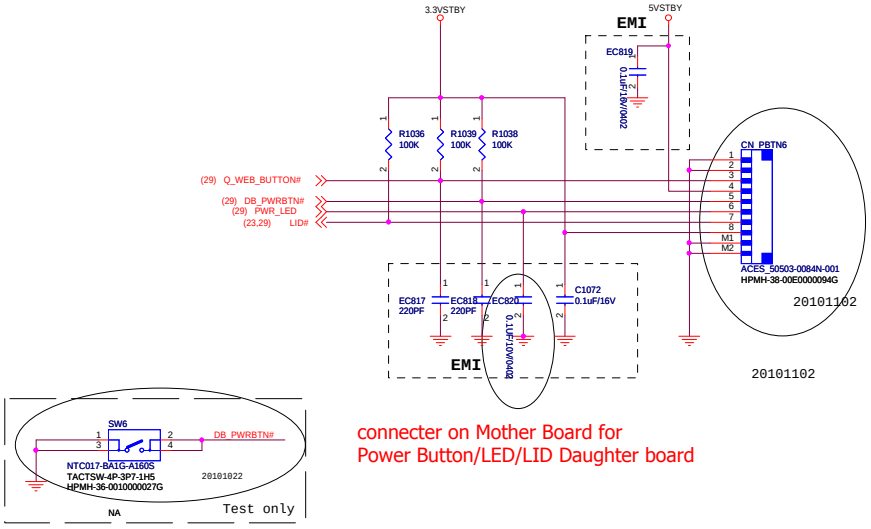
LID



FLEX Computing

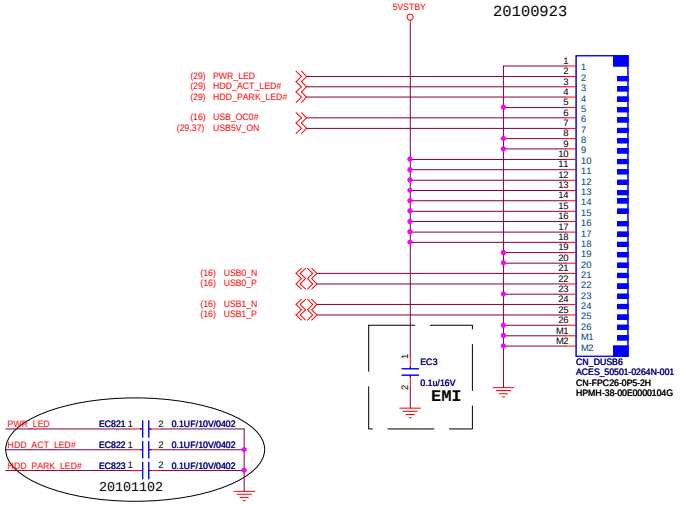
Project Name : H710DI1	Title : WebCAM_BT_FP_TS_TP_LID
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 26 of 63

PWRBTN BOARD

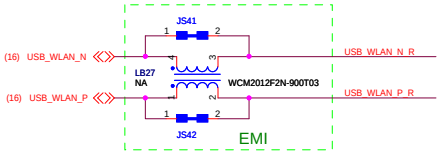


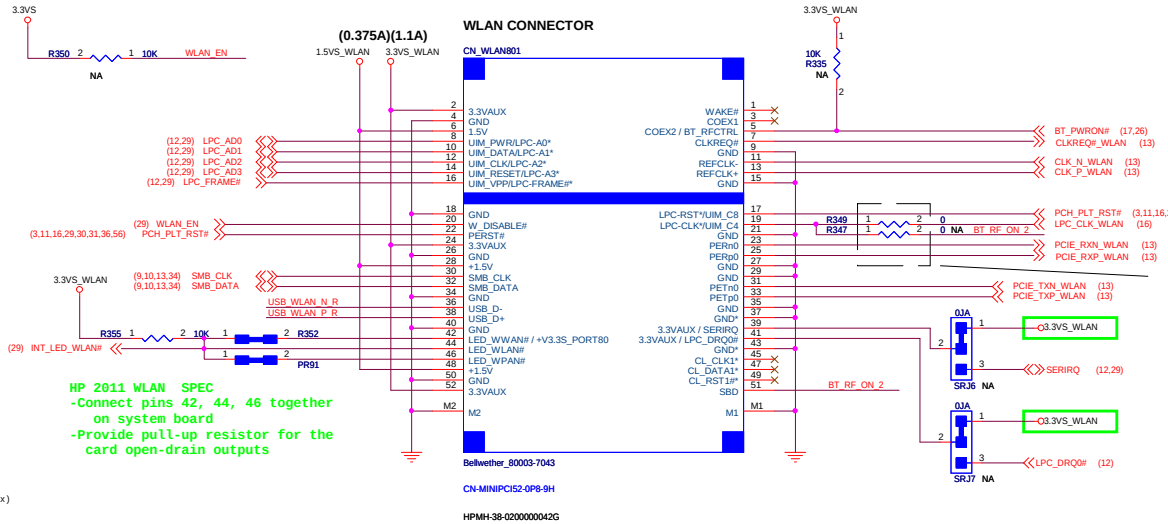
connecter on Mother Board for
Power Button/LED/LID Daughter board

USB BOARD



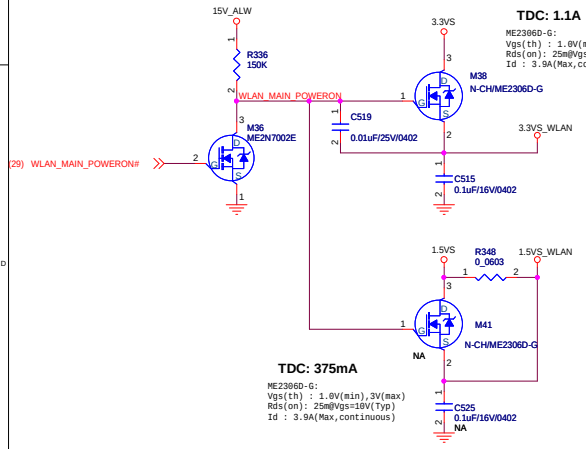
Mini-PCIE - WLAN (Half size)

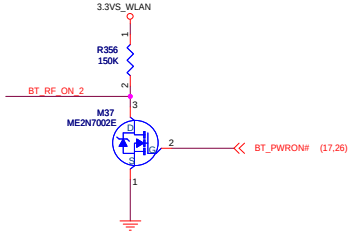


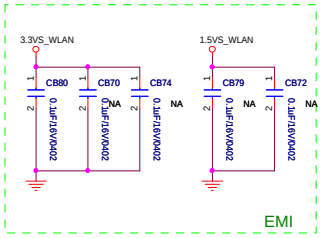


HP 2011 WLAN SPEC
-Connect pins 42, 44, 46 together
on system board
-Provide pull-up resistor for the
card open-drain outputs

HP 2011 WLAN SPEC 2'nd RF ON/OFF Pin
Primary path is to implement it on pin 51,
but 0 Ohm strap to pin 19 required for
Intel Rainbow Peak ES2 cards use
(QS will transition to pin 51).



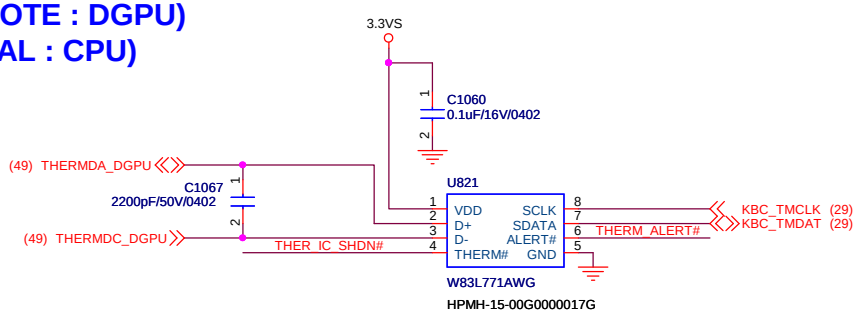




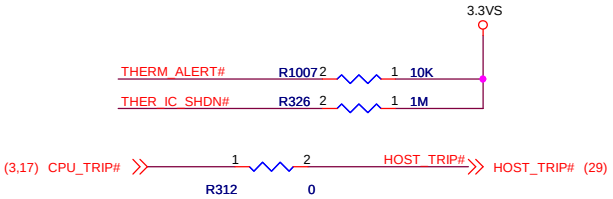
FLEX Computing

Project Name : H710D1	Title : MB to DB CONN_WLAN
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 27 of 63

Thermal Sensor
(REMOTE : DGPU)
(LOCAL : CPU)



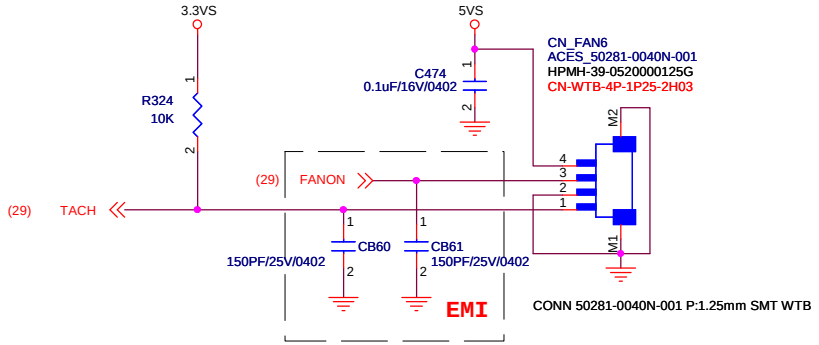
Place between CPU and VGA



THERMAL IC FOR CPU or DGPU

WINBOND	W83L771AWG	ODMH-15-00G0000017G 1001100x(98h)
ON SEMI	ADT7421ARMZ-REEL	???
GMT	G780P81U	???

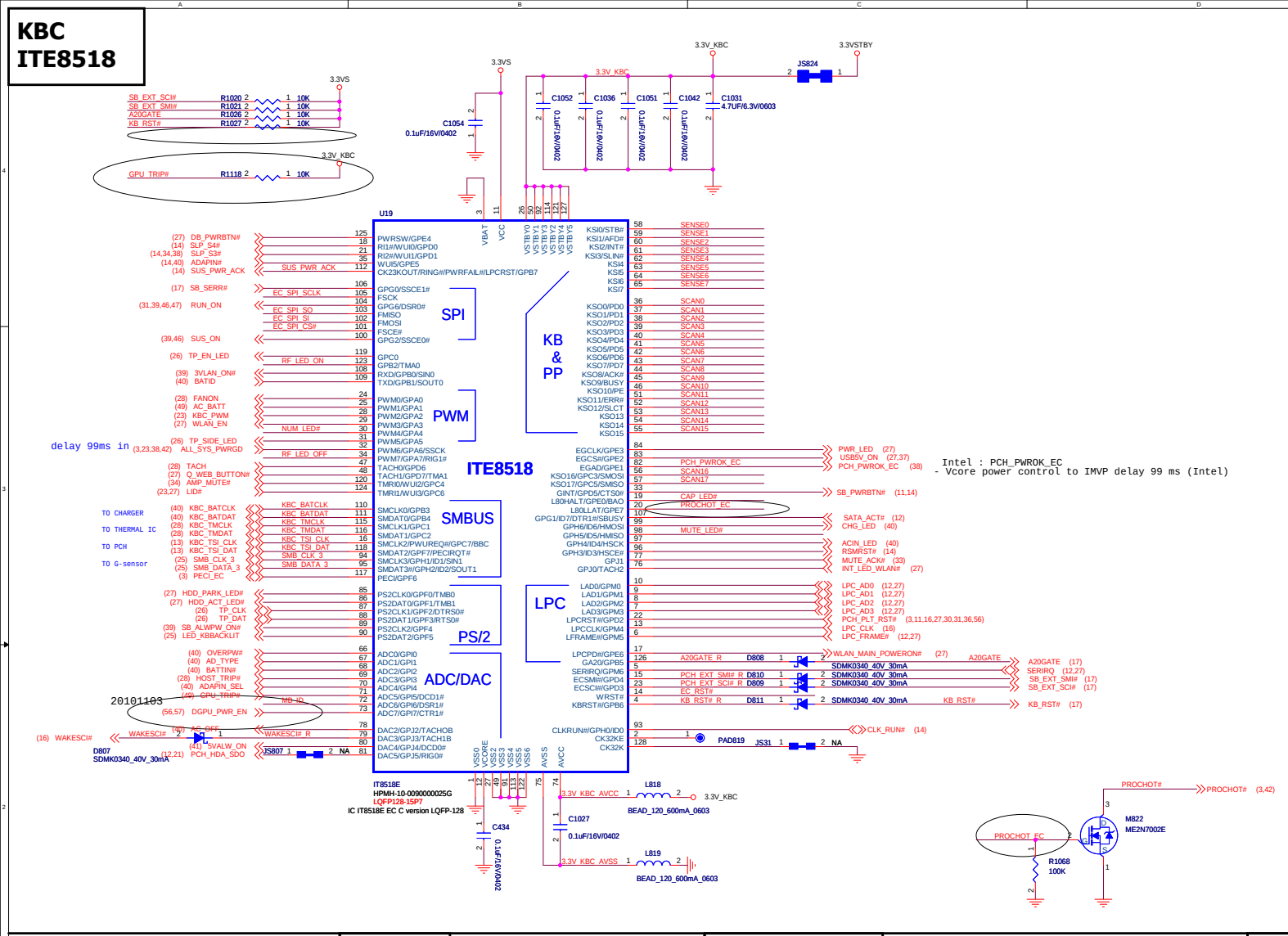
FAN CONN



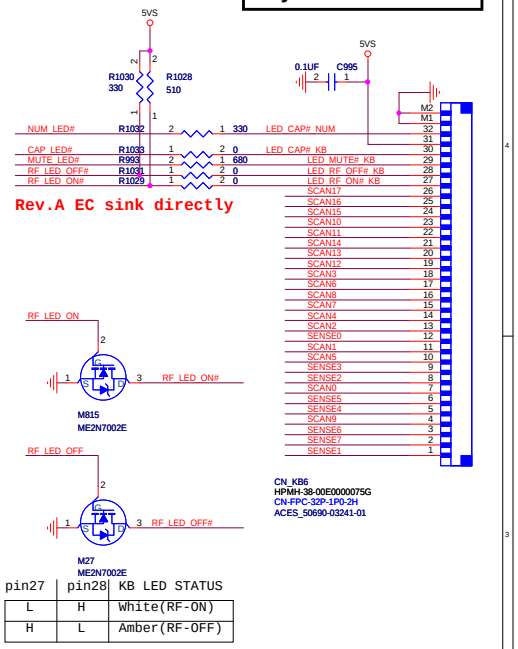
FLEX Computing

Project Name : H710DI1	Title : THERM IC_FAN	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 28 of 63	

KBC ITE8518

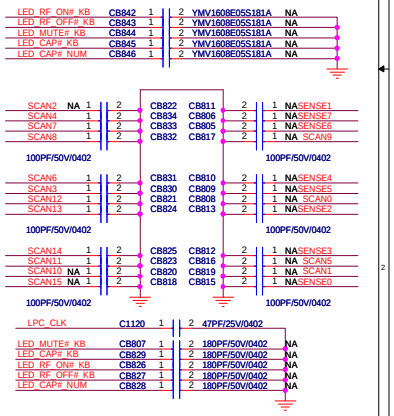


Keyboard Connector

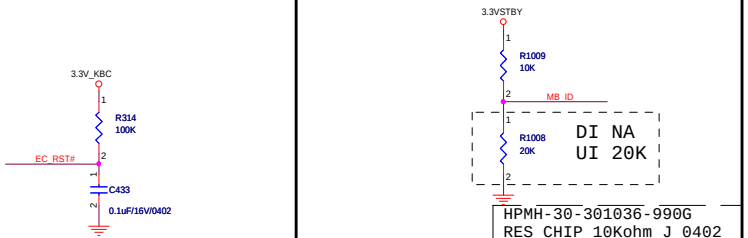


pin27	pin28	KB LED STATUS
L	H	White(RF-ON)
H	L	Amber(RF-OFF)

EMI



Board ID

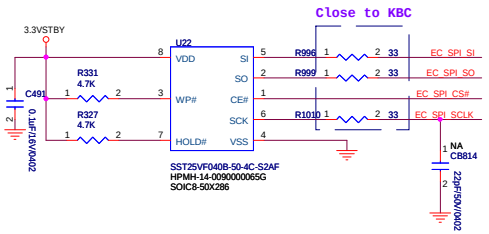


HPMH-30-301036-990G
RES CHIP 10Kohm J 0402

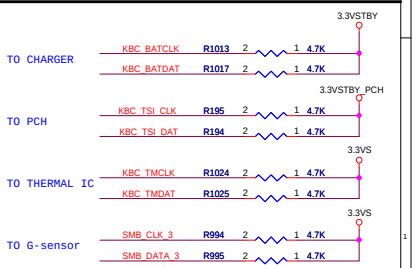
HPMH-30-102036-990G
RES CHIP 20Kohm J 0402

MB-ID		
3.3v	INTEL-DI	10K PULL UP
2.2v	INTEL-UI	10K PULL UP,20K PULL LOW
1.1v	AMD-DA	20K PULL UP,10K PULL LOW
0v	AMD-UA	10K PULL LOW

SPI ROM (512KB)



SM BUS

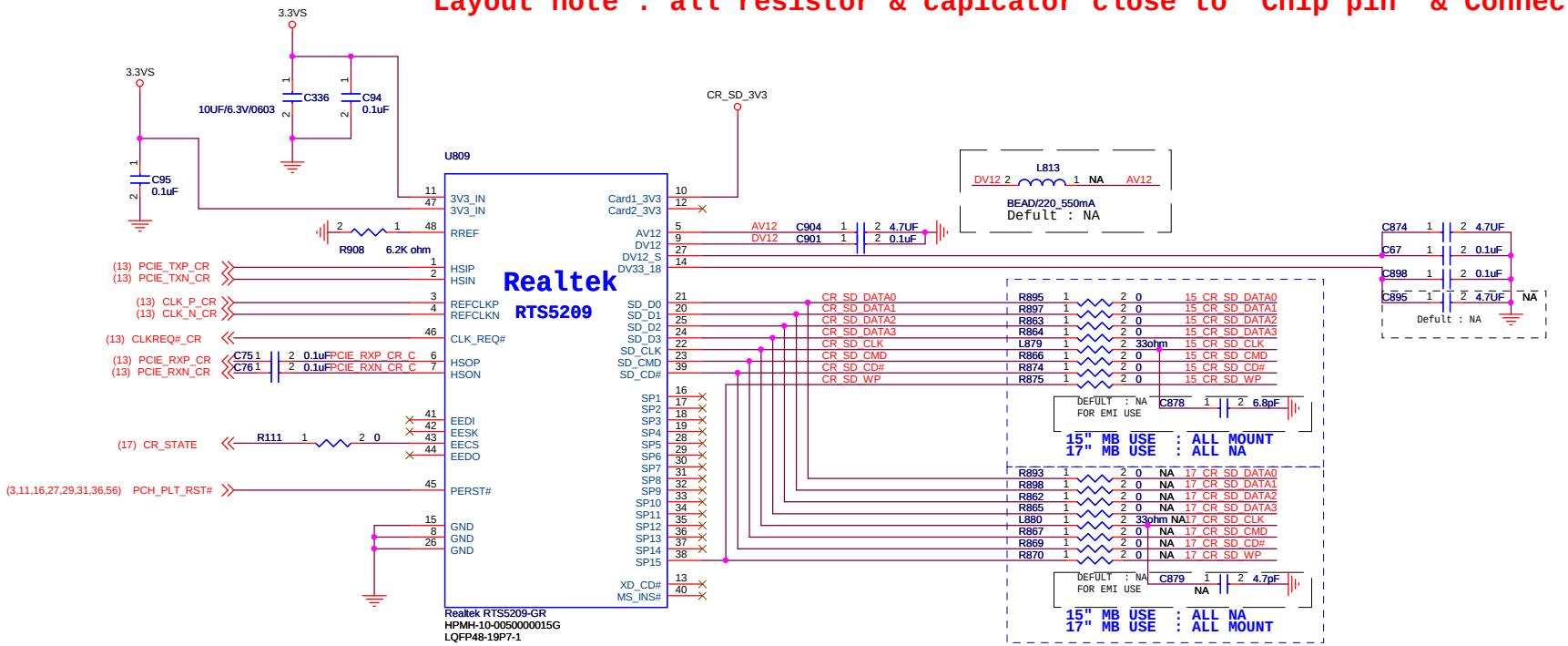


FLEX Computing

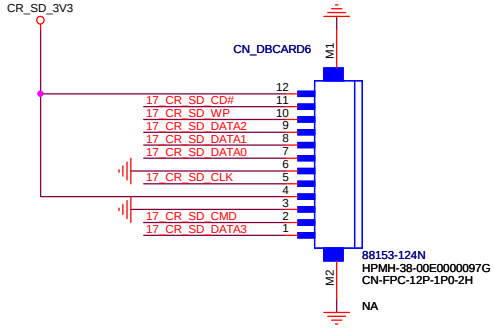
Project Name : H710DI1	Title : SPI_KBC(ITE8502E)
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 29 of 63

Card Reader

Layout note : all resistor & capicator close to Chip pin & Connector pin



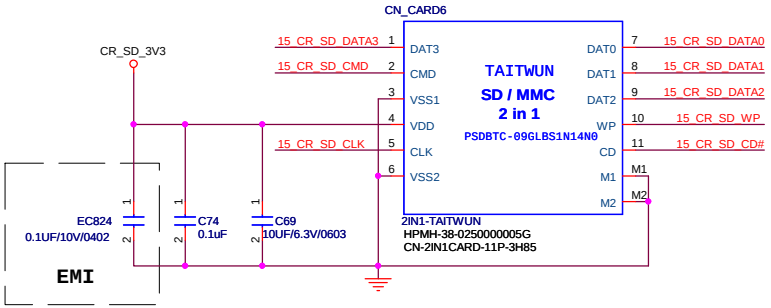
FOR 17" MB USE WTB CONNECTOR



FOR 15" MB ALL COMPONENT : NA

FOR 17" MB ALL COMPONENT : MOUNT

FOR 15" MB USE CardReader CONNECTOR



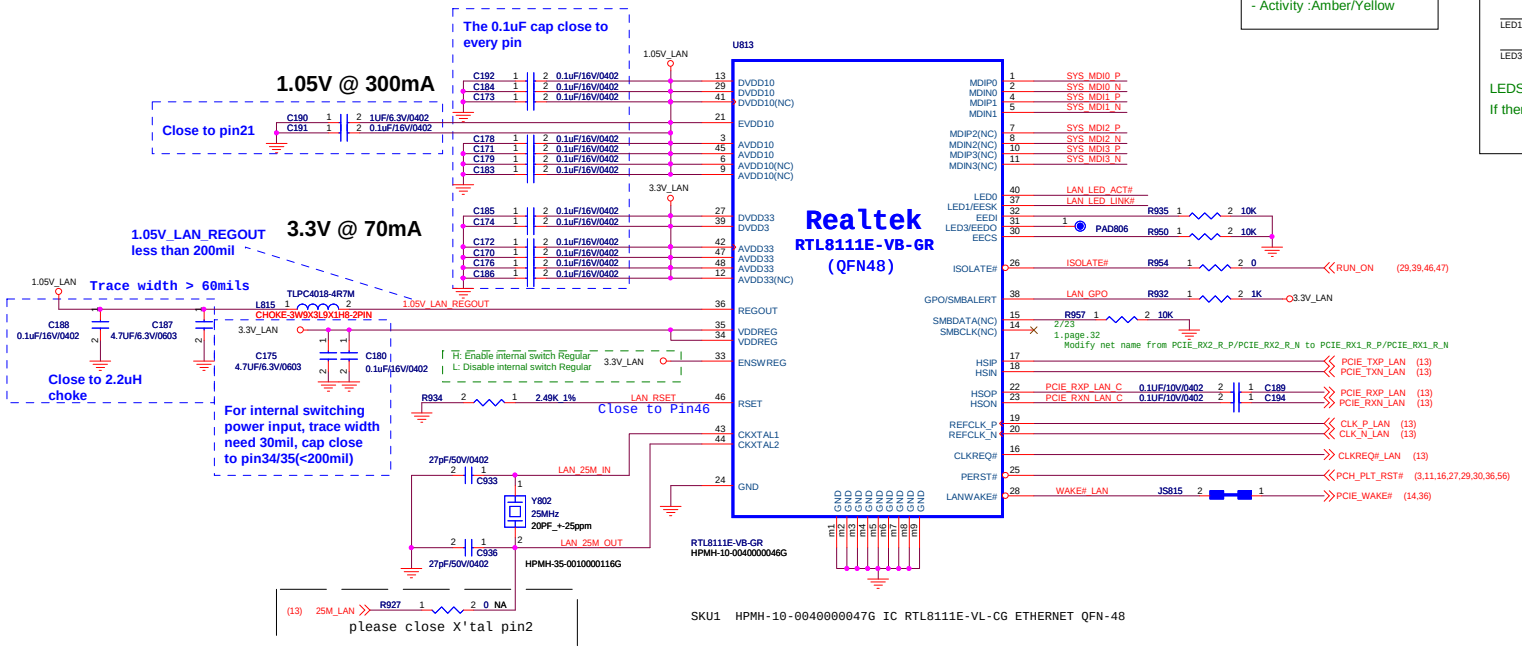
FOR 15" MB ALL COMPONENT : MOUNT

FOR 17" MB ALL COMPONENT : NA

FLEXComputing

Project Name : H710DI1	Title : Card Reader (R5U220)	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 30 of 63	

GBit LAN Controller



SKU1 HPMH-10-0040000047G IC RTL8111E-VL-CG ETHERNET QFN-48

Mini-spec requirements:
10/100/1000 :
- Link :White
- Activity :Amber/Yellow

RTL8111E

LEDS1-0	00	01	10	11
LED0	ACT ALL	LINK ALL /ACT ALL	LINK10 /ACT ALL	LINK10 /ACT10
LED1	LINK100	LINK100	LINK100	LINK100 /ACT100
LED3	LINK1000	LINK1000	LINK1000	LINK1000 /ACT1000

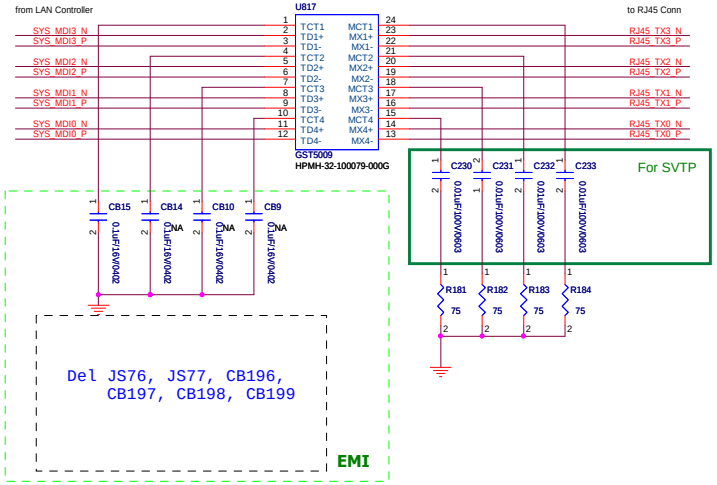
LEDS1-0s initial value comes from the EEPROM
If there is no EEPROM, the default value is 11

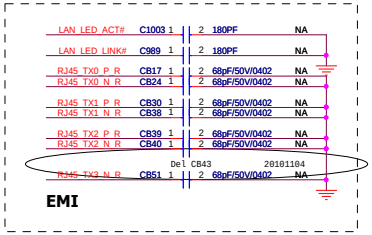
TRANSFORMER

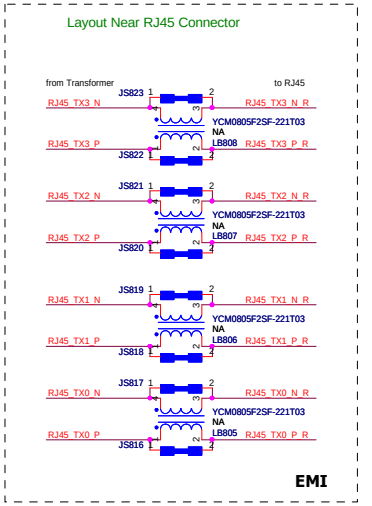
2009.09.22 ref. "RTL8102E_8111D 48PIN demo_board v200_2008.04.30"

Transformer :
Gbit P/N: 32-100079-000G(GST5009)
10/100 P/N: 32-0000000009G (TST1284)

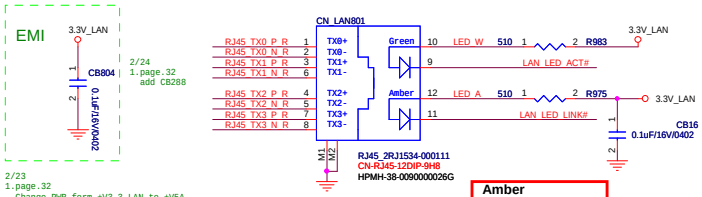
Layout near RJ45 Connector





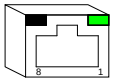


RJ45 Cable Connector



Amber
Vf=2V If =20mA
White
Vf=3.2V If =30mA

Reference:
RJ45 Phone Jack
Pin define:
1 TXD+0
2 TXD-0
3 TXD+1
4 TXD+2
5 TXD-2
6 TXD-1
7 TXD+3
8 TXD-3



SVTP_v4.03
2.6 - Ethernet Checklist - Rev C.xls

- Ch.3.1.4.4
Some older cheap RJ-45s only populate pins 1,2,3,6. 10/100 requires the other 4 pins for grounding. Gigabit Ethernet requires all 8 pins for data signals.

- Ch.3.1.4.13
Resistance from RJ-45 shell to any other chassis ground point (ohms) less than 1 ohm

- Ch.3.1.4.14 & Ch.3.1.4.15
Protection against non-standard power-over-Ethernet (PoE) : Resistance between pins 1,3 (TXD0P,TXD1P) and pins 4,7 (TXD2P,TXD3P) of the RJ-45 greater than 58K ohms.

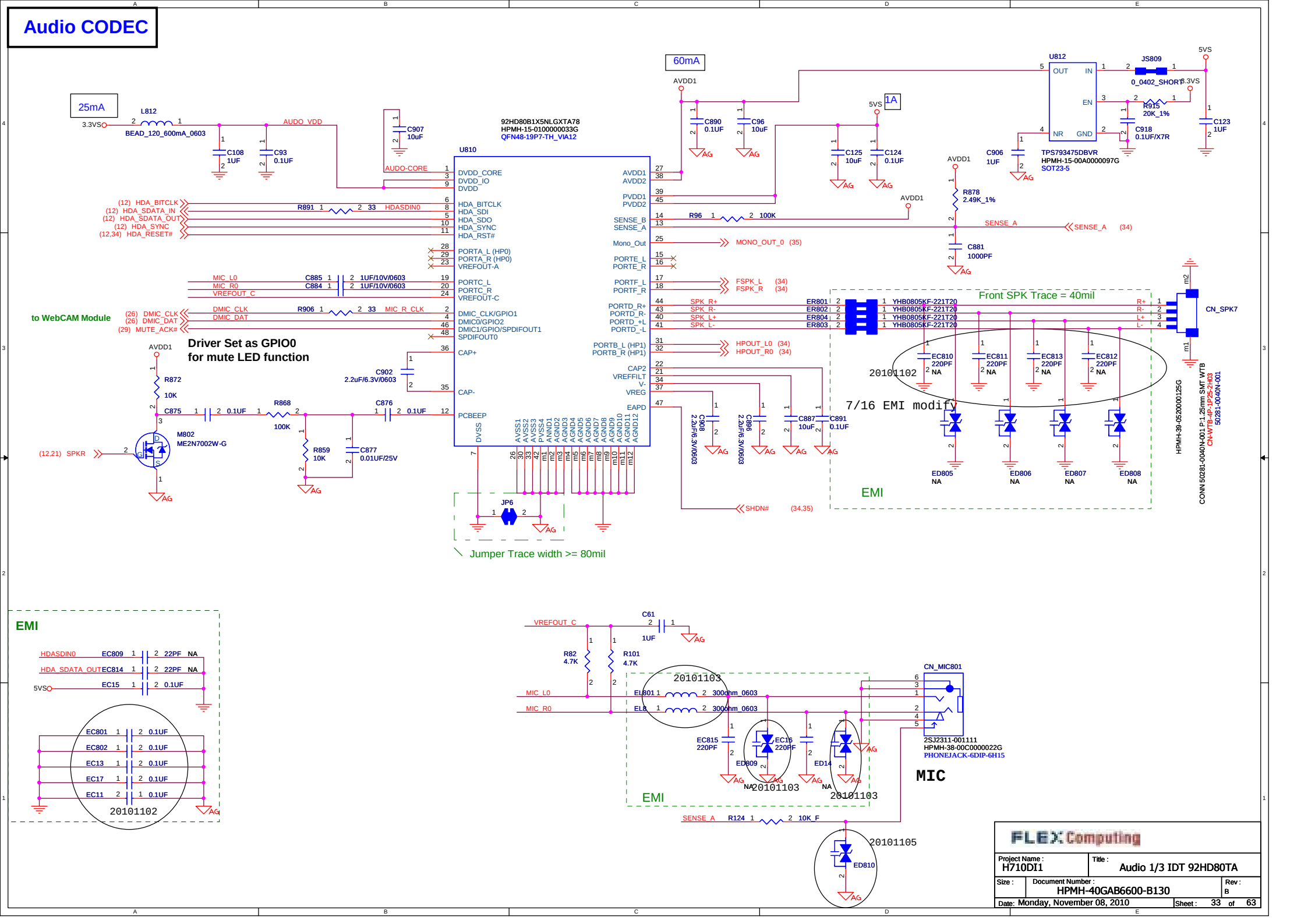
FLEX Computing

Project Name : H710DI1	Title : RJ45_LAN (RTL8111E-VB-GR)	
Size : C	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 31 of 63	

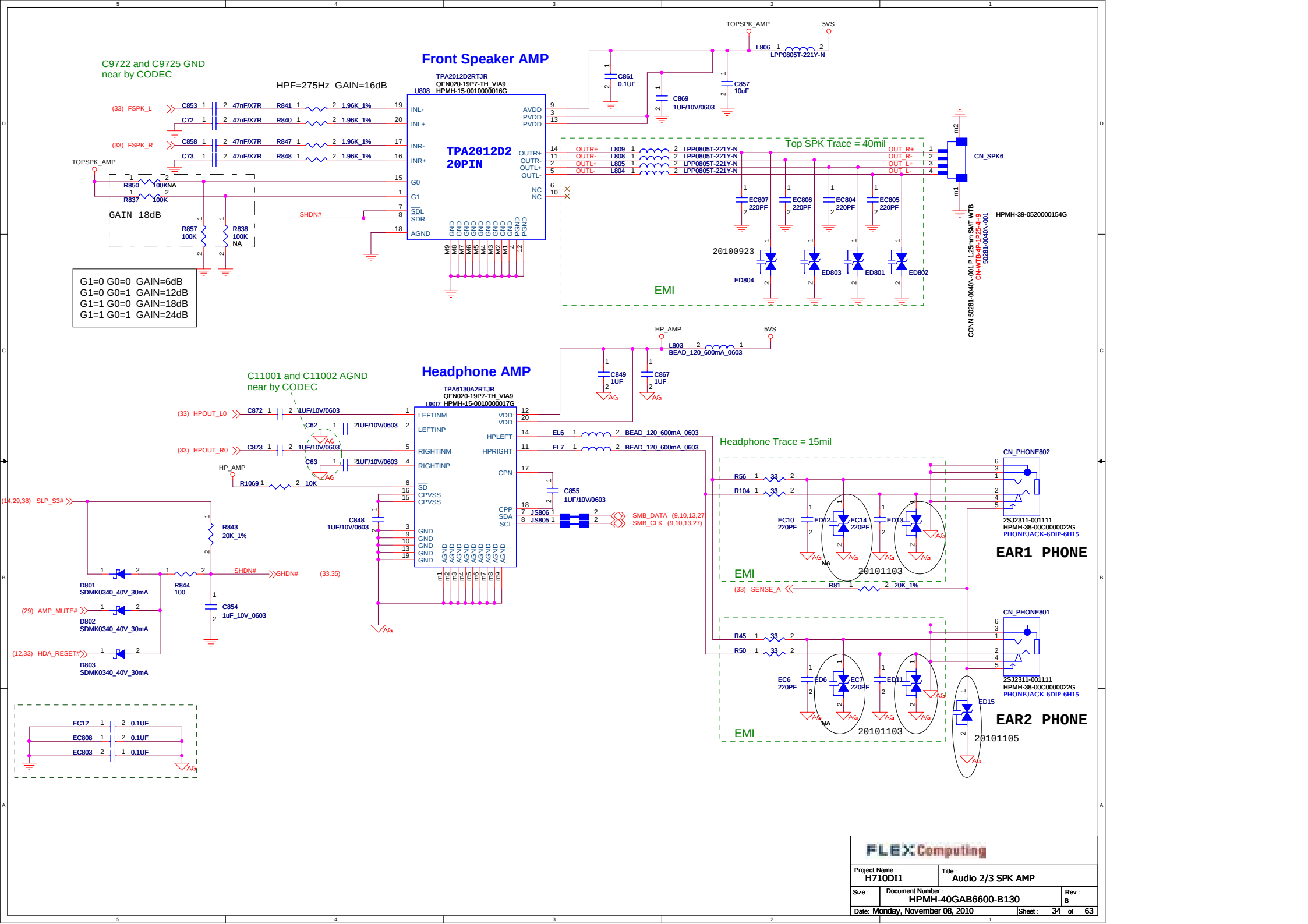
FLEX Computing

Project Name : H710DI1	Title : RESERVE	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 32 of 63	

Audio CODEC



FLEX Computing			
Project Name : H710DI1	Title : Audio 1/3 IDT 92HD80TA		
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 33 of 63	



FLEX Computing		
Project Name : H710DI1	Title : Audio 2/3 SPK AMP	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 34 of 63	

If without supply Woofer all page NA

WOOFER AMP

HPA00836PWPR
HTSSOP28-25P6X220-TH
U805

HPA00836PWPR
28PIN

+PWR_SRC_AMP
B+
L807 LPP0805T-221Y-N

C850 1000PF
C863 0.1UF/25V
C856 4.7uF/25V
C817 4.7uF/25V
C862 1000PF
C823 0.1UF/25V
C824 4.7uF/25V
C818 4.7uF/25V
R1070 10_0805
C868 1UF/25V
R1071 10K

PVCCR
PVCCL
AVCC
BSN
OUTN
BSP
OUTP
GND
PGND

C840 0.1uF/25V
L8 LPP0805T-221Y-N
R827 10
C828 470pF
C843 0.1uF/25V
L7 LPP0805T-221Y-N
R836 10
C851 470pF
EC9 1000PF
EC8 1000PF

Woofer SPK Trace = 40mil

CN_WOF6
ACES_88266-040001
CN-WTB-2P-1P25-2H03
CONN 50214-00201-001 P:1mm SMT WTB
HPMH-39-0520000126G

C9742 GND
near by CODEC

WOOFER_IN C844 1UF/10V/0603
R834 0
R835 0
C64 1UF/10V/0603

INN
INP
GAIN0
GAIN1
GVDD
PLIMIT
SD
FAULT
NC
AGND

5VS
R821 100K NA
R825 100K NA

GAIN 20dB

R822 100K
R826 100K

G1=0 G0=0 GAIN=20dB
G1=0 G0=1 GAIN=26dB
G1=1 G0=0 GAIN=32dB
G1=1 G0=1 GAIN=36dB

C839 1UF/10V/0603
R1072 49.9K_F
R1073 28.7K_F
C1094 1UF/10V/0603
(33,34) SHDN#

Kevin modify-0909

AVDD1
VREF_EQ
R824 10K_F
R830 10K_F
C847 4.7uF/0603
C845 0.1UF

(33) MONO_OUT_0
C846 1UF/10V/0603
R832 10K_F
C841 5600pF
R831 10K_F
C831 0.1UF
C822 47nF
C830 100PF/50V/0402
U804A
TLV2464
IC TLV2464CPWR Audio AMP TSSOP-14

R814 30.1K_F
C819 47nF
R816 10K_F
C826 100PF/50V/0402
R819 60.4K_F
U804B
R815 10K_F
C821 47nF

R820 30.1K_F
C827 47nF
R817 10K_F
C829 100PF/50V/0402
R818 60.4K_F
U804C
R813 10K_F
C825 47nF

C842 5600pF
R833 10K_F
C837 1UF/10V/0603
U804D
C838 100PF/50V/0402
WOOFER_IN

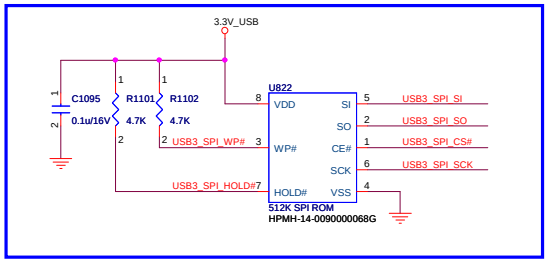
R823 0
NA

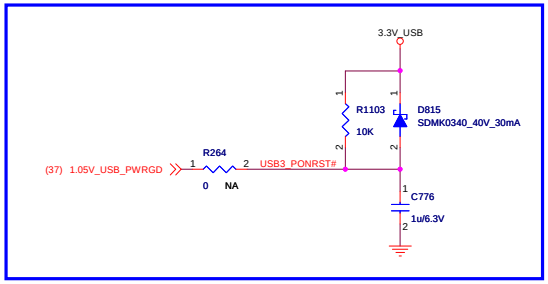
Always NA

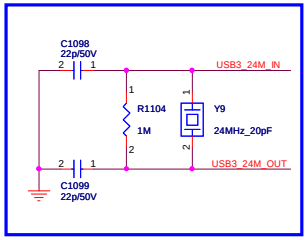
FLEX Computing

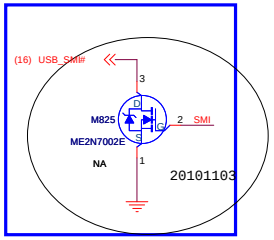
Project Name : H710DI1	Title : Audio 3/3 WOOFER AMP	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 35 of 63	

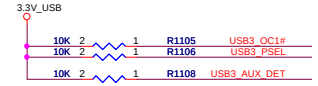
USB3.0 NEC uDP720200

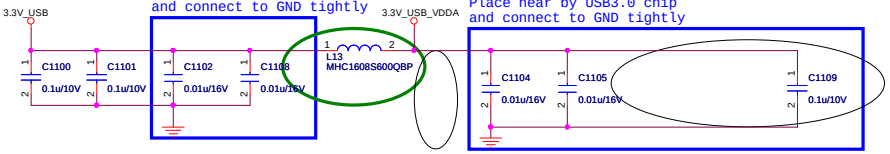


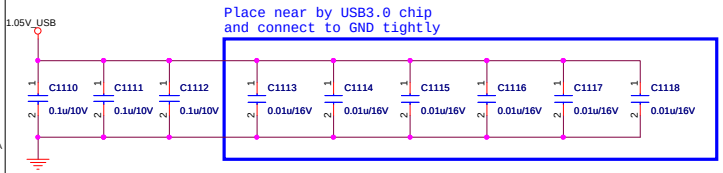


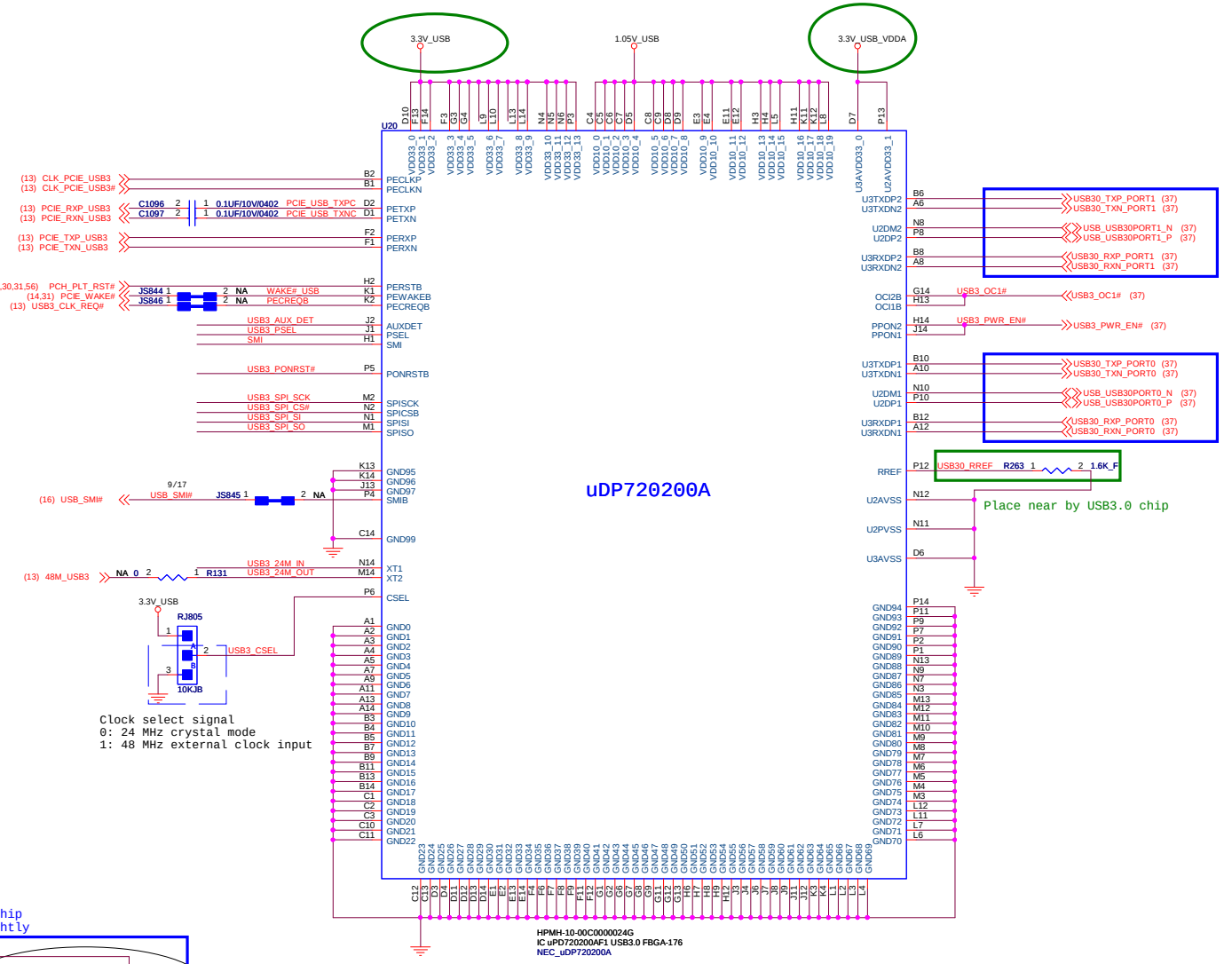










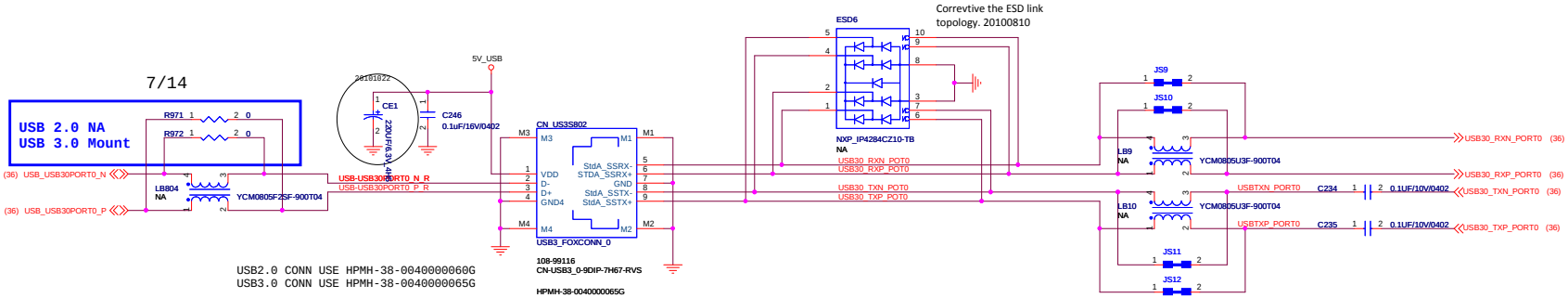


Clock select signal
0: 24 MHz crystal mode
1: 48 MHz external clock input

FLEX Computing			
Project Name : H710DI1		Title : USB30_uDP720200	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 36 of 63	

7/14

USB 2.0 NA
USB 3.0 Mount

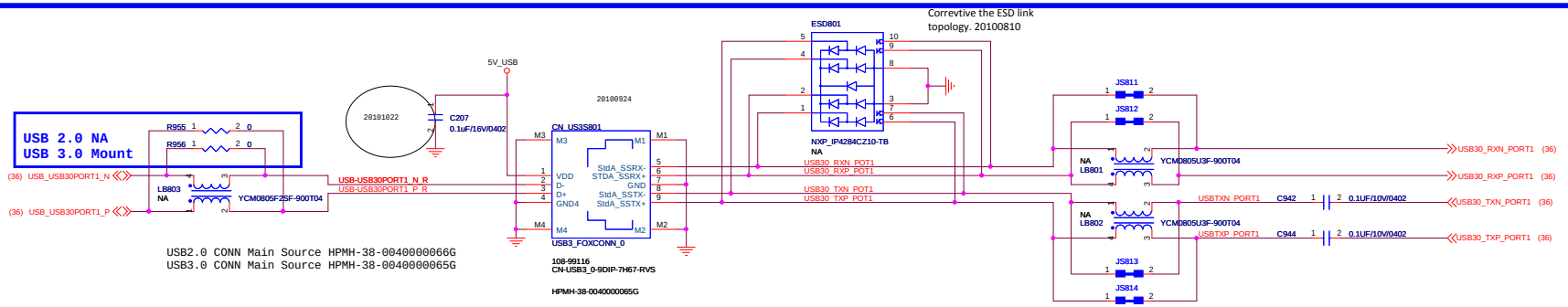


USB2.0 CONN USE HPMH-38-0040000060G
USB3.0 CONN USE HPMH-38-0040000065G

USB 2.0 2nd Source
HPMH-38-0040000078G
HPMH-38-0040000080G
HPMH-38-0040000087G

USB 3.0 2nd Source
HPMH-38-0040000085G
HPMH-38-0040000068G
HPMH-38-0040000088G

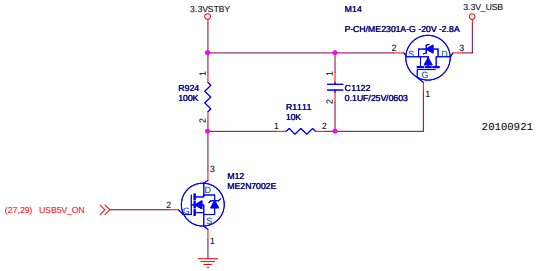
USB 2.0 NA
USB 3.0 Mount



USB2.0 CONN Main Source HPMH-38-0040000066G
USB3.0 CONN Main Source HPMH-38-0040000065G

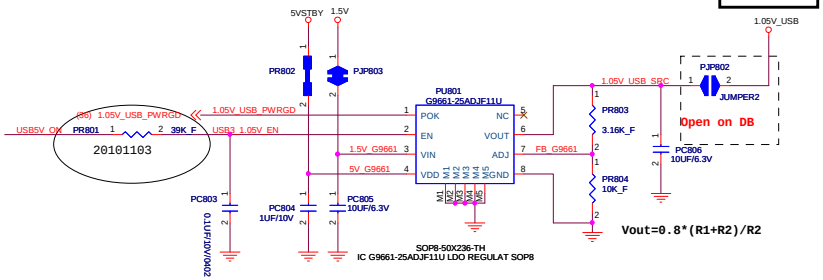
USB3.0 3.3V

500mW / 3.3V
(0.151Amp)

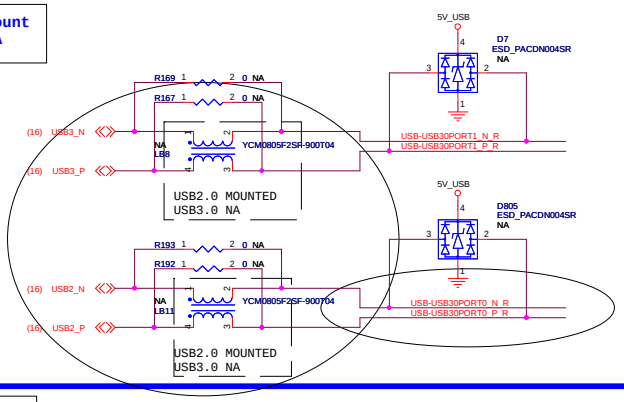


USB3.0 1.05V_USB

593mW / 1.05V
(0.72Amp)

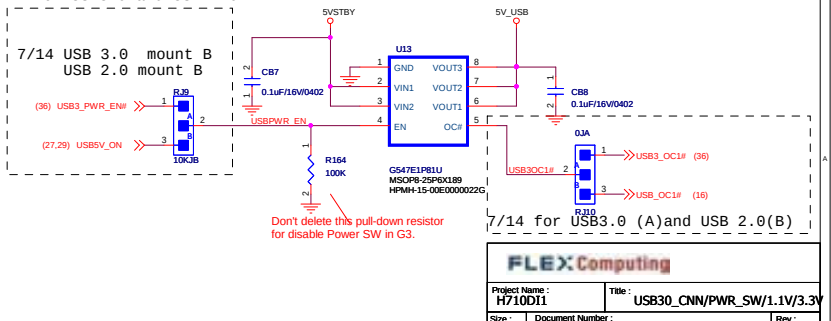


USB 2.0 Mount
USB 3.0 NA



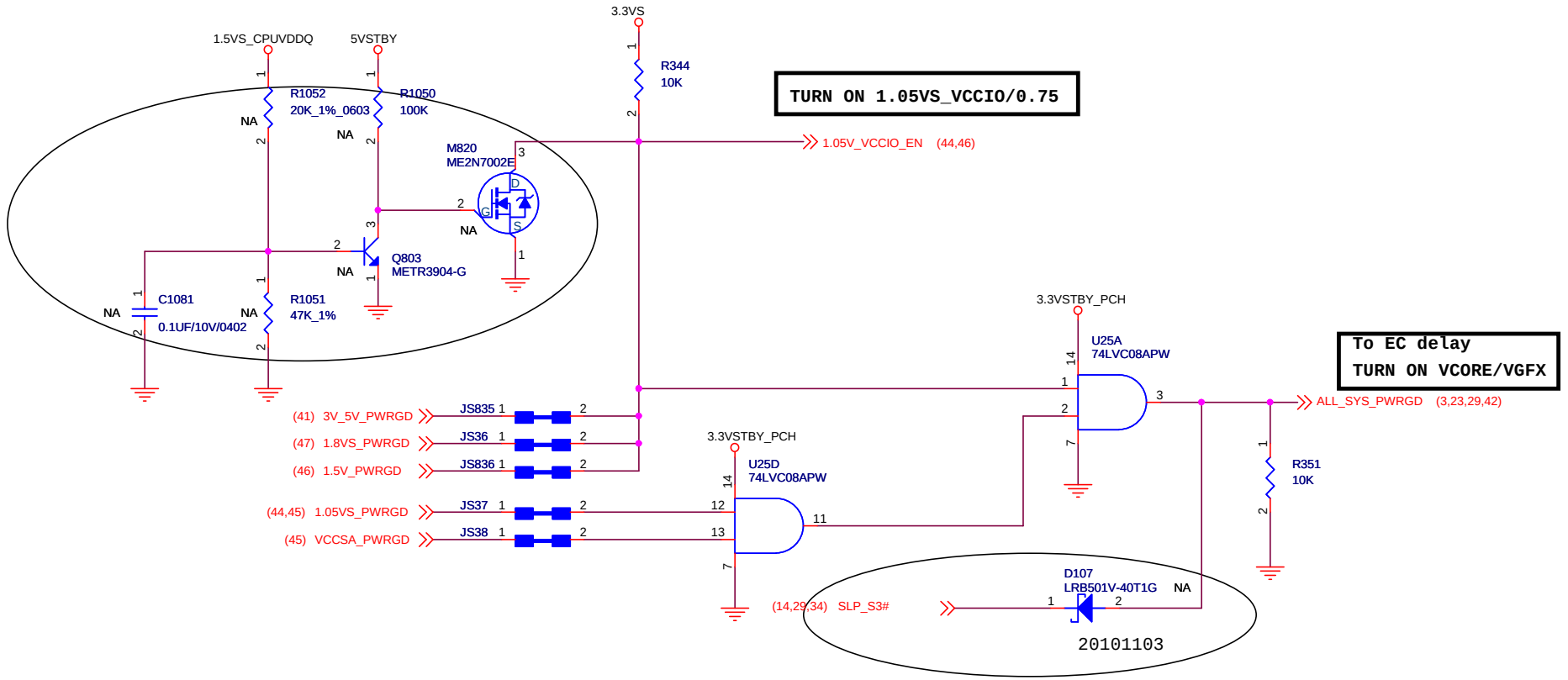
USB POWER SW

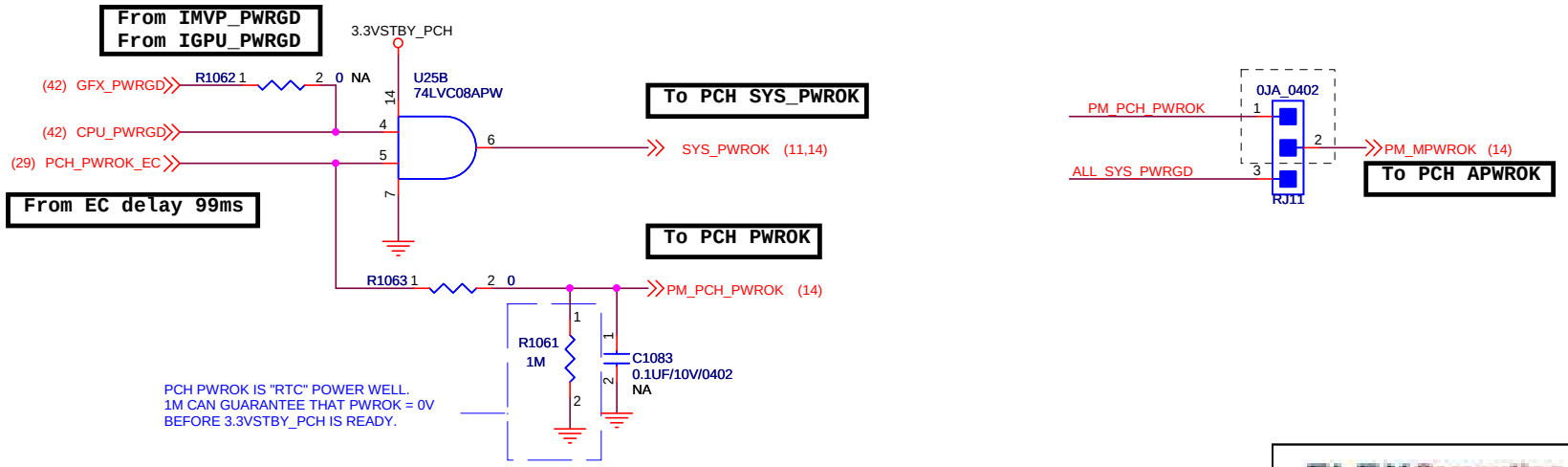
7/14 for USB3.0 and USB 2.0



FLEX Computing

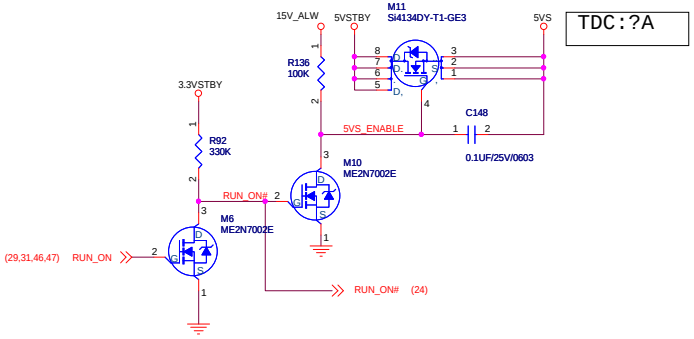
Project Name : H710DI1	Title : USB30_CNN/PWR_SW/1.1V/3.3V
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 37 of 63



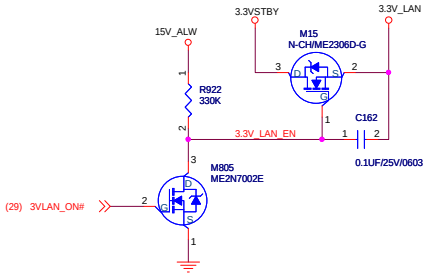


FLEXComputing

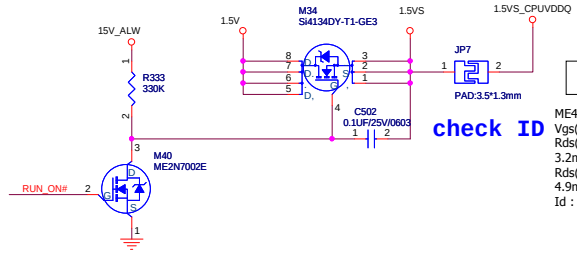
Project Name : H710DI1	Title : POWER_GOOD
Size : Custom	Document Number : HPMH-40GAB6600-B130
Rev : B	
Date: Monday, November 08, 2010	Sheet : 38 of 63



TDC:?A



TDC:0.3A

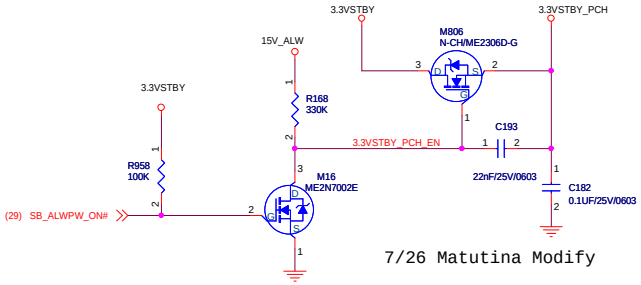


TDC:?A

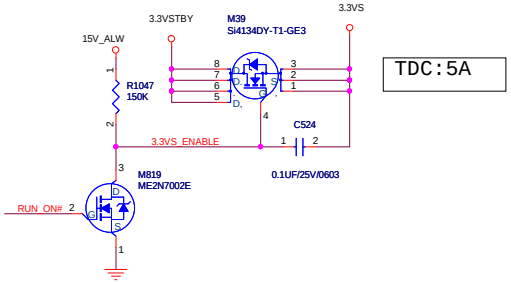
check ID

ME4626 :
Vgs(th): 3V(max)
Rds(on):
3.2m@Vgs = 10V (Max)
Rds(on):
4.9m@Vgs = 4.5V (Max)
Id : 23A

TDC:0.6A



7/26 Matutina Modify



TDC:5A

ME2306D:

Vgs(th) : 1.0V(min),3.0V(max)
Rds(on) : 31m@Vgs = 10V(MAX)
Rds(on) : 52m@Vgs = 4.5V(MAX)
Id : 3.9A(Max)

ME4894-G:

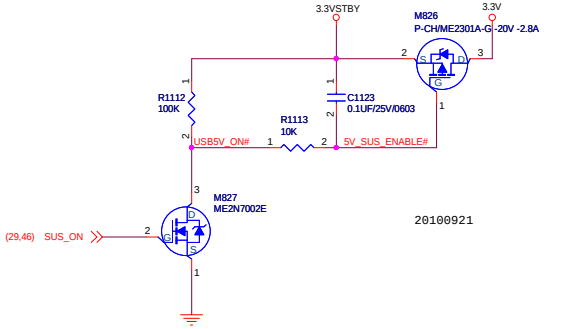
Vgs(th) : 1.0V(min),3.0V(max)
Rds(on) : 11.7m@Vgs = 10V (MAX)
Rds(on) : 18.2m@Vgs = 4.5V(MAX)
Id : 11.5A(Max)

ME2301A:

Vgs(th) : -0.9V(max)
Rds(on) : 75m@Vgs = -4.5V(MAX)
Id : -2.8A(Max)

3.3V

500mW / 3.3V

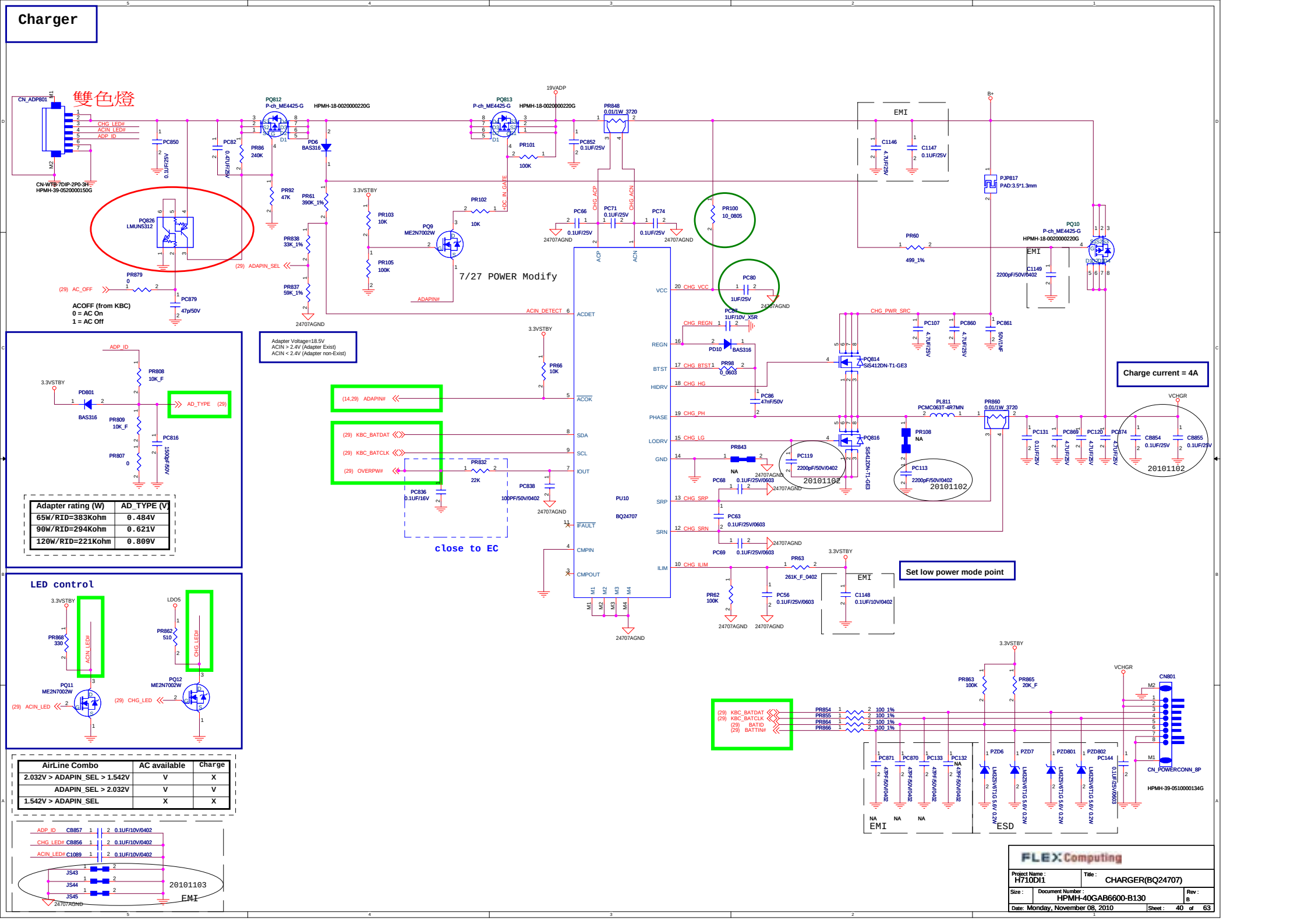


20100921

FLEX Computing

Project Name : H710DI1	Title : RUN_PWR & SUS_PWR
Size : Custom	Document Number : HPMH-40GAB6600-B130
Rev : B	
Date: Monday, November 08, 2010	Sheet : 39 of 63

Charger


雙色燈
CN_ADP801
CHG_LED#
ACIN_LED#
ADP_ID
CN-WTB-7DIP-2P0-3H
HPMH-39-0520000150G
PC850
0.1UF/25V
PC82
0.47UF/25V
PQ812
P-ch_ME4425-G
HPMH-18-0020000220G
PD6
BAS316
PR86
240K
PR92
47K
PQ826
LMUN5312
PR879
0
PC879
47p/50V
(29) AC_OFF
ACOFF (from KBC)
0 = AC On
1 = AC Off
PR838
33K_1%
PR837
59K_1%
(29) ADAPIN_SEL
24707AGND
PQ813
P-ch_ME4425-G
HPMH-18-0020000220G
19VADP
PR848
0.01/1W_3720
PR101
100K
PC852
0.1UF/25V
3.3VSTBY
PR103
10K
PR105
100K
PR102
10K
PQ9
ME2N7002W
ADAPIN#
7/27 POWER Modify
DC_IN_GATE
CHG_ADP
CHG_ACN
PC66
0.1UF/25V
PC71
0.1UF/25V
PC74
0.1UF/25V
PR100
10_0805
PC80
1UF/25V
PC81
1UF/10V_X5R
ACIN_DETECT
ACDET
ACP
ACN
VCC
REGN
BTST
HIDRV
PHASE
LODRV
GND
SRP
SRN
ILIM
ACOK
SDA
SCL
IOUT
IFAULT
CMPIN
CMPOUT
PU10
BQ24707
CHG_VCC
CHG_REGN
CHG_BTST
CHG_HG
CHG_PH
CHG_LG
CHG_SRP
CHG_SRN
CHG_ILIM
PD10
BAS316
PR98
0.0603
PC86
47nF/50V
PR843
NA
PC68
0.1UF/25V/0603
PC63
0.1UF/25V/0603
PC69
0.1UF/25V/0603
PR63
261K_F_0402
PC56
0.1UF/25V/0603
PR62
100K
C1148
0.1UF/10V/0402
EMI
B+
C1146
4.7UF/25V
C1147
0.1UF/25V
PJP817
PAD:3.5*1.3mm
PR60
499_1%
PQ10
P-ch_ME4425-G
HPMH-18-0020000220G
C1149
2200pF/50V/0402
CHG_PWR_SRC
PC107
4.7UF/25V
PC860
4.7UF/25V
PC861
50V/1uF
PQ814
SIS412DN-T1-GE3
PQ816
SIS412DN-T1-GE3
PL811
PCMC063T-4R7MN
PR860
0.01/1W_3720
PR108
NA
PC119
2200pF/50V/0402
PC113
2200pF/50V/0402
20101102
Charge current = 4A
VCHGR
PC131
0.1UF/25V
PC865
4.7UF/25V
PC120
4.7UF/25V
PC874
4.7UF/25V
CB854
0.1UF/25V
CB855
0.1UF/25V
20101102
ADP_ID
PR808
10K_F
PD801
BAS316
AD_TYPE (29)
PR809
10K_F
PR807
0
PC816
1500pF/50V
Adapter rating (W) | AD_TYPE (V)
65W/RID=383Kohm | 0.484V
90W/RID=294Kohm | 0.621V
120W/RID=221Kohm | 0.809V
Adapter Voltage=18.5V
ACIN > 2.4V (Adapter Exist)
ACIN < 2.4V (Adapter non-Exist)
(14,29) ADAPIN#
(29) KBC_BATDAT
(29) KBC_BATCLK
(29) OVERPW#
PR832
22K
PC836
0.1UF/16V
PC838
100PF/50V/0402
close to EC
Set low power mode point
LED control
PR868
330
ACIN_LED#
PQ11
ME2N7002W
(29) ACIN_LED
LDO5
PR862
510
CHG_LED#
PQ12
ME2N7002W
(29) CHG_LED
AirLine Combo | AC available | Charge
2.032V > ADAPIN_SEL > 1.542V | V | X
ADAPIN_SEL > 2.032V | V | V
1.542V > ADAPIN_SEL | X | X
ADP_ID CB857 0.1UF/10V/0402
CHG_LED# CB856 0.1UF/10V/0402
ACIN_LED# C1089 0.1UF/10V/0402
JS43
JS44
JS45
20101103
EMI
(29) KBC_BATDAT
(29) KBC_BATCLK
(29) BATID
(29) BATTIN#
PR854
PR855
PR864
PR866
100 1%
PR863
100K
PR865
20K_F
CN801
CN_POWERCONN_8P
HPMH-39-0510000134G
PC871
PC870
PC133
PC132
PC144
0.1UF/25V/0603
PZD6
PZD7
PZD801
PZD802
LMZ25V6T1G 5.6V 0.2W
ESD
NA
EMI
FLEX Computing
Project Name : H710DI1
Title : CHARGER(BQ24707)
Size :
Document Number : HPMH-40GAB6600-B130
Rev : B
Date: Monday, November 08, 2010
Sheet : 40 of 63

5V / 3.3VSTBY

Freq=300KHz
TDC = 7 A
OCP = 10 A

Freq=375KHz
TDC = 4 A
OCP = 5.7A

PU9
TPS51125RGER

5V/3.3VSTBY ON

TRIP 3V

TRIP 5V

Current limit

ENtrip floating active

* Options 1.
5VSTBY

* Options 2.

* Options 3.
(38) 3V_5V_PWRGD

Vo=(1+R1/R2)*2
(1+32.4K/21K)*2= 5..08V

Vo=(1+R1/R2)*2
= (1+13/20)*2 = 3.3V

For RT8205A
PR92 must MOUNTED
PR94 must NA

INTEL HR / AMD DANUBE
Options 1 - 5VSTBY / 5V
Options 2 - 5VALW_ON / SUS_ON
Options 3 - 3V_5V_PWRGD / 3.3V_5V_PWRGD
Options 4 - 15V_ALW / 15VSTBY
Options 5 - 5VSTBY / 5V

VREG5 : 5V -> 365KHz , 3.3V -> 460KHz
VREG3: 5V -> 300KHz , 3.3V -> 375KHz

7/28 power Modify

For PCB Acustic Noise

PU3-m1
For layout request, no connect anything.

+15V Charge pump

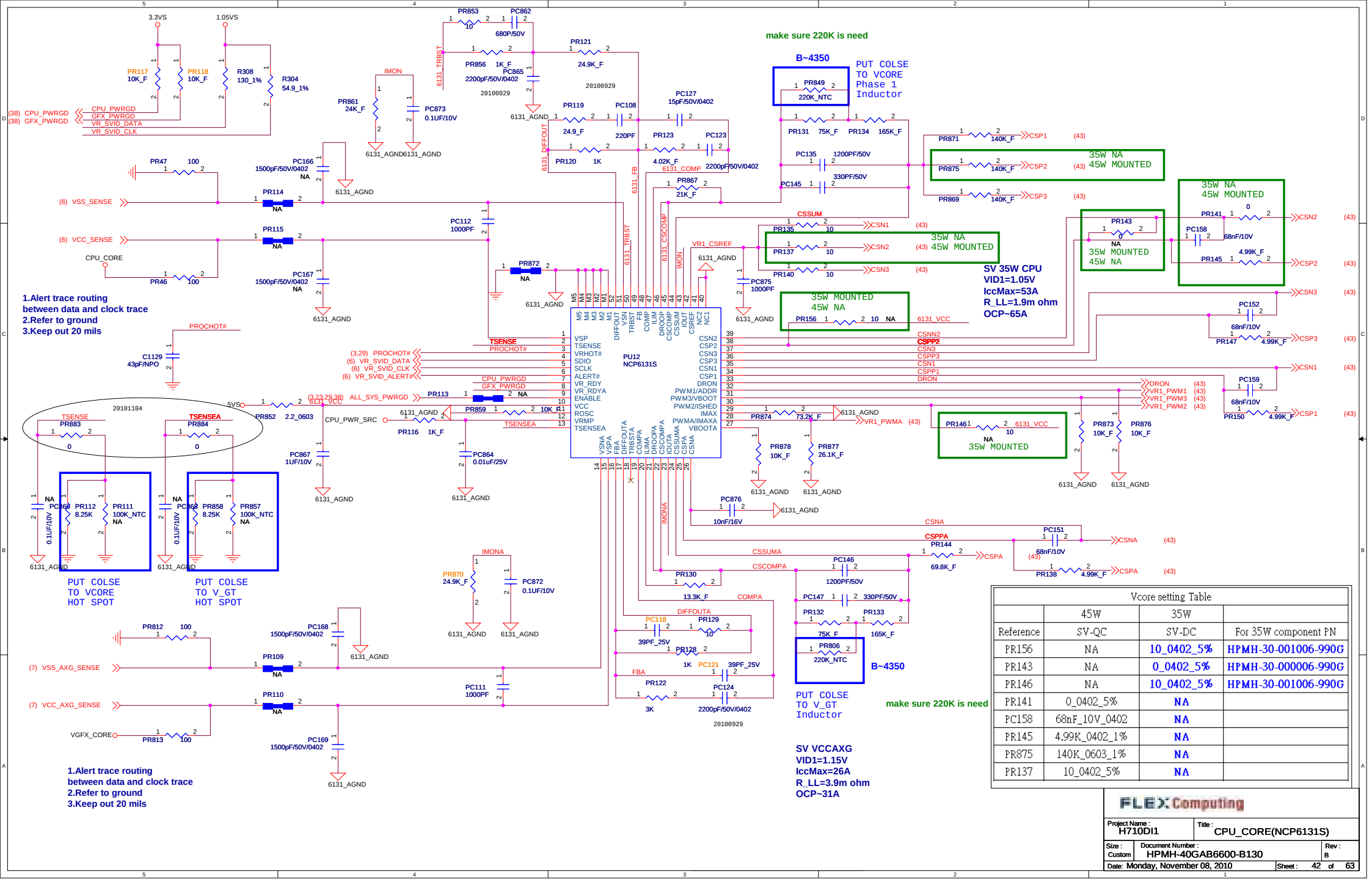
QFN024-19P7-TH_VIA4

Table 3. Enabling State

EN0	ENTRIP1	ENTRIP2	VREF	VREG5	VREG3	CH1	CH2	VCLK
GND	Don't Care	Don't Care	Off	Off	Off	Off	Off	Off
R to GND	Off	Off	On	On	On	Off	Off	Off
R to GND	On	Off	On	On	On	On	Off	Off
R to GND	Off	On	On	On	On	Off	On	Off
R to GND	On	On	On	On	On	On	On	Off
Open	Off	Off	On	On	On	Off	Off	Off
Open	On	Off	On	On	On	On	Off	On
Open	Off	On	On	On	On	Off	On	Off
Open	On	On	On	On	On	On	On	On

Project Name : H710DI1	Title : 5VSTBY_3VSTBY(TPS51125)
Size : Custom	Document Number : HPMH-40GAB6600-B130
Rev : B	
Date: Monday, November 08, 2010	Sheet : 41 of 63

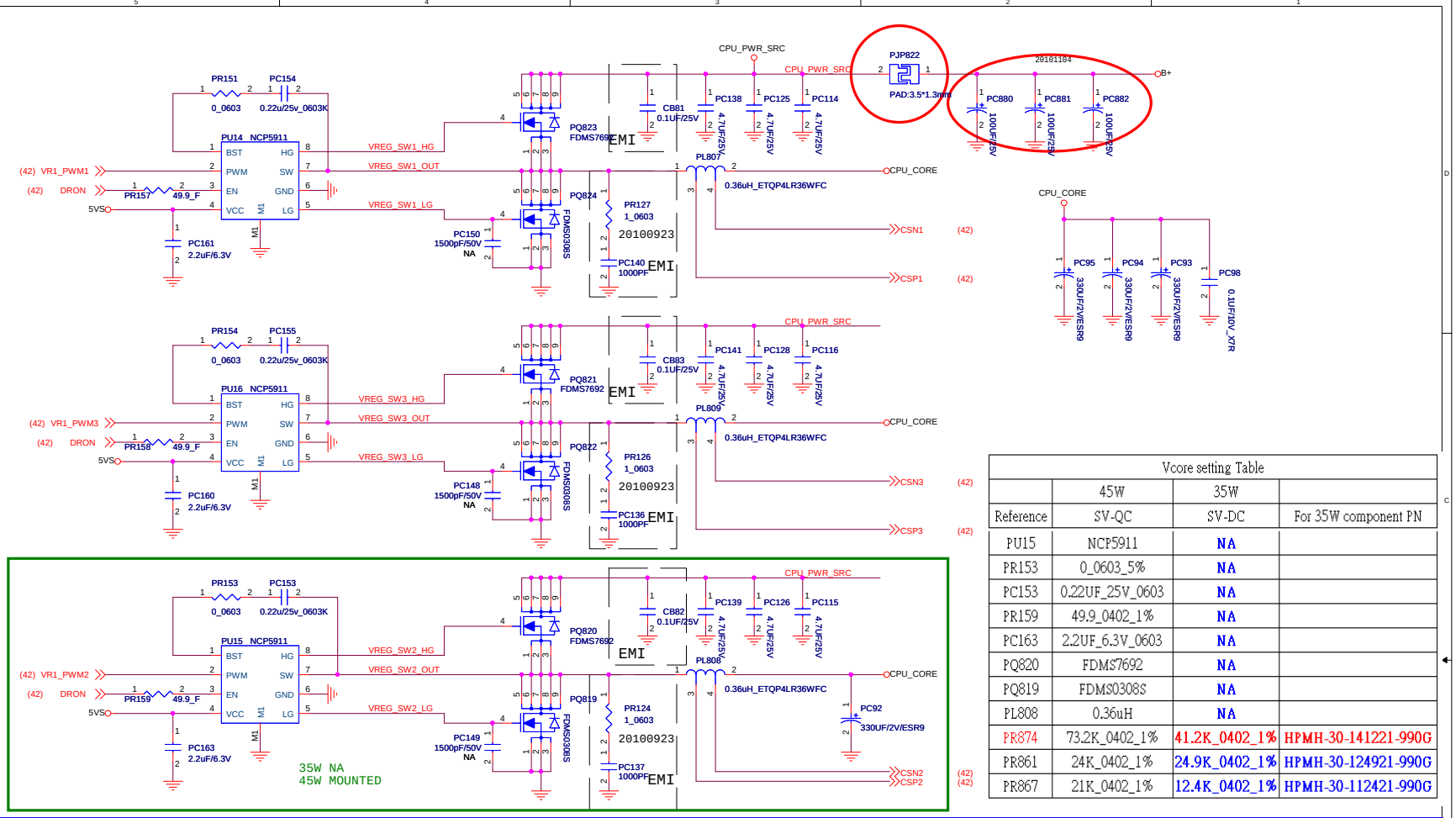
FLEXComputing



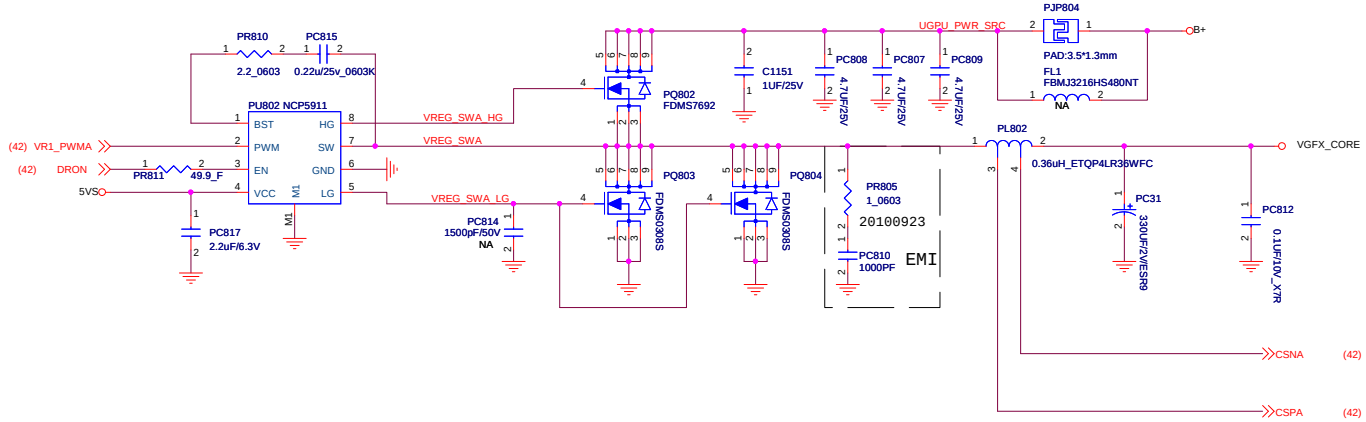
Vcore setting Table			
	45W	35W	
Reference	SV-QC	SV-DC	For 35W component PN
PR156	NA	10_0402_5%	HPMH-30-001006-990G
PR143	NA	0_0402_5%	HPMH-30-000006-990G
PR146	NA	10_0402_5%	HPMH-30-001006-990G
PR141	0_0402_5%	NA	
PC158	68nF_10V_0402	NA	
PR145	4.99K_0402_1%	NA	
PR875	140K_0603_1%	NA	
PR137	10_0402_5%	NA	

FLEXComputing

Project Name : H710DI1	Title : CPU_CORE(NCP6131S)
Size : Custom	Document Number : HPMH-40GAB6600-B130
Rev : B	
Date: Monday, November 08, 2010	Sheet : 42 of 63



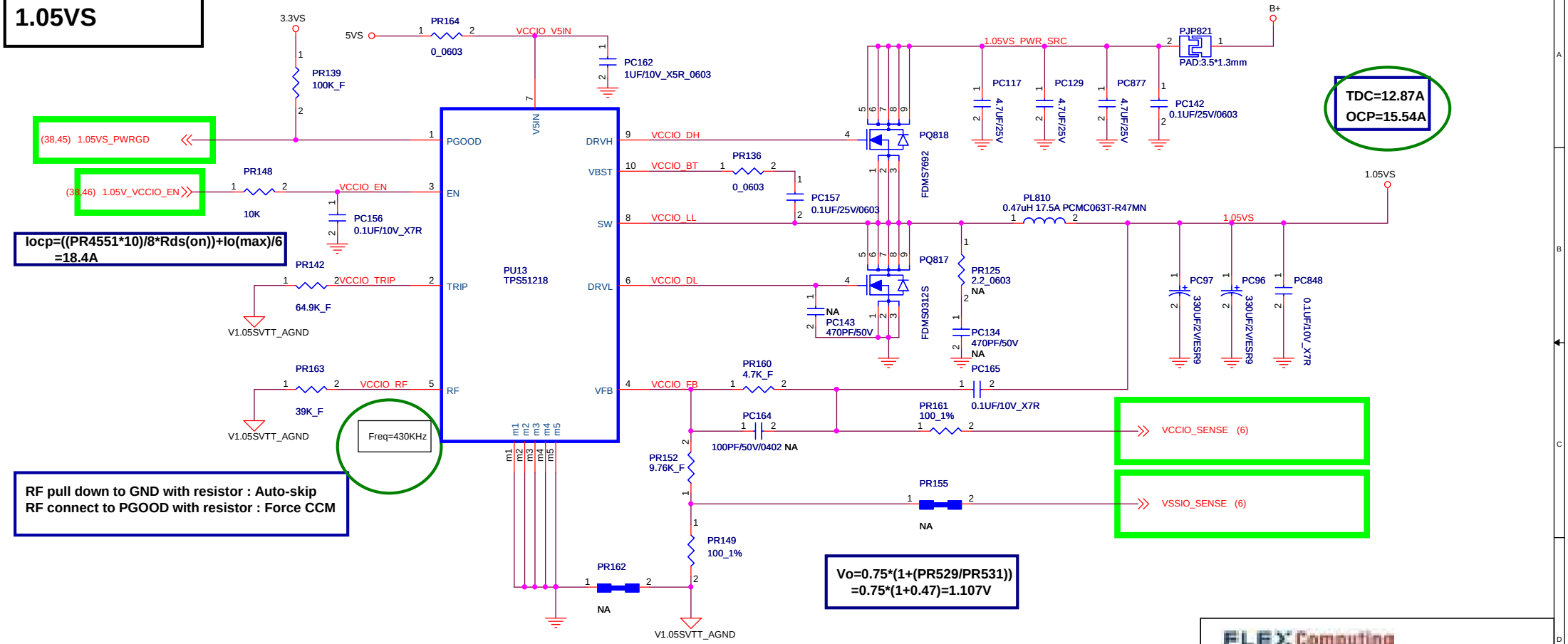
Vcore setting Table			
	45W	35W	
Reference	SV-QC	SV-DC	For 35W component PN
PU15	NCP5911	NA	
PR153	0_0603_5%	NA	
PC153	0.22UF_25V_0603	NA	
PR159	49.9_0402_1%	NA	
PC163	2.2UF_6.3V_0603	NA	
PQ820	FDMS7692	NA	
PQ819	FDMS0308S	NA	
PL808	0.36uH	NA	
PR874	73.2K_0402_1%	41.2K_0402_1%	HPMH-30-141221-990G
PR861	24K_0402_1%	24.9K_0402_1%	HPMH-30-124921-990G
PR867	21K_0402_1%	12.4K_0402_1%	HPMH-30-112421-990G



FLEX Computing

Project Name : H710DI1	Title : CPU_CORE_DRIVER(NCP5911)	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 43 of 63	

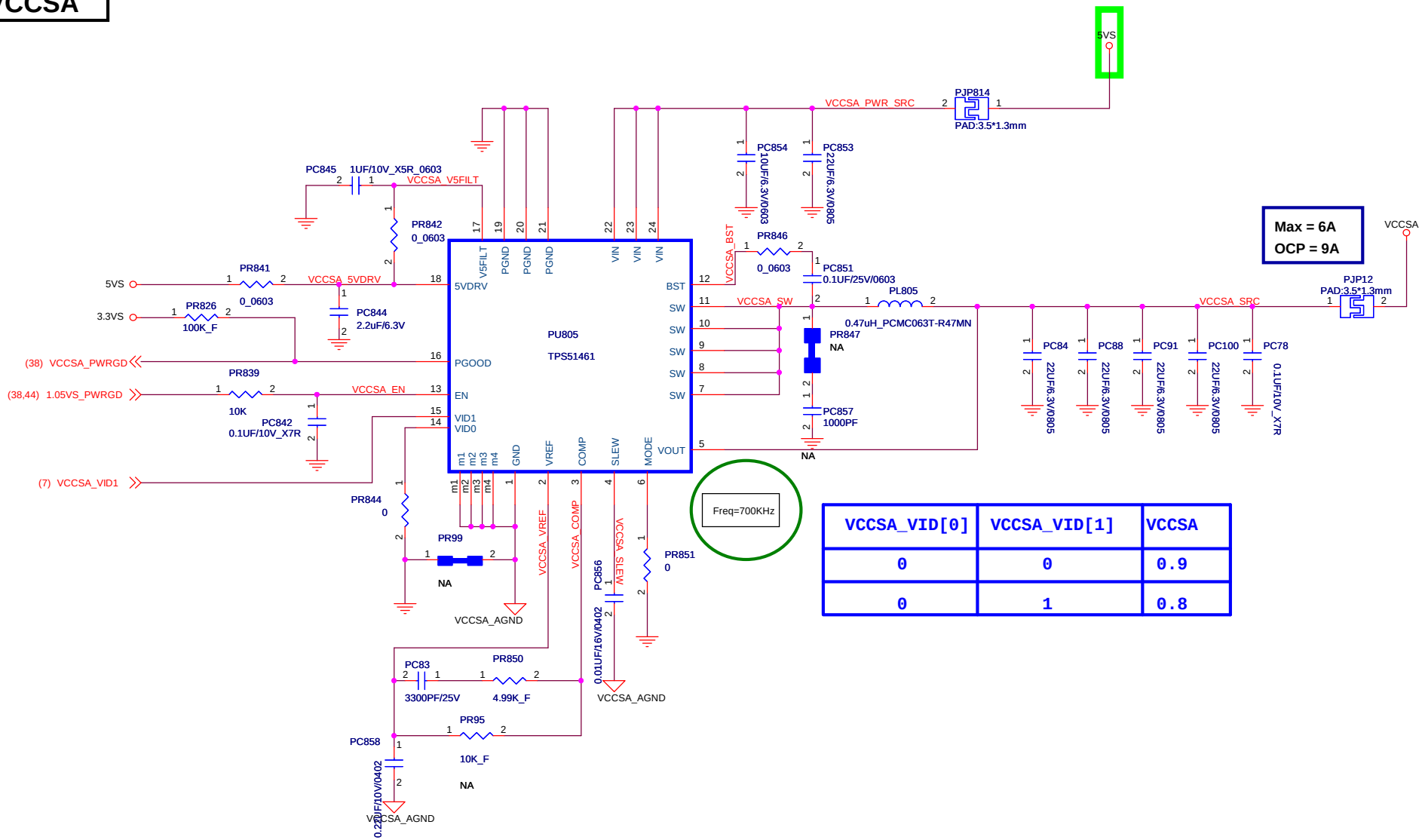
1.05VS_VCCIO
1.05VS



FLEX Computing

Project Name : H710DI1	Title : 1.05VS(TPS51218)
Size : Custom	Document Number : HPMH-40GAB6600-B130 / Rev : B
Date: Monday, November 08, 2010	Sheet : 44 of 63

VCCSA



VCCSA_VID[0]	VCCSA_VID[1]	VCCSA
0	0	0.9
0	1	0.8

FLEXComputing

Project Name : H710DI1	Title : ITE8509E/ 1.1VS
Size : B	Document Number : HPMH-40GAB6600-B130 / Rev : B
Date: Monday, November 08, 2010	Sheet : 45 of 63

1.5V

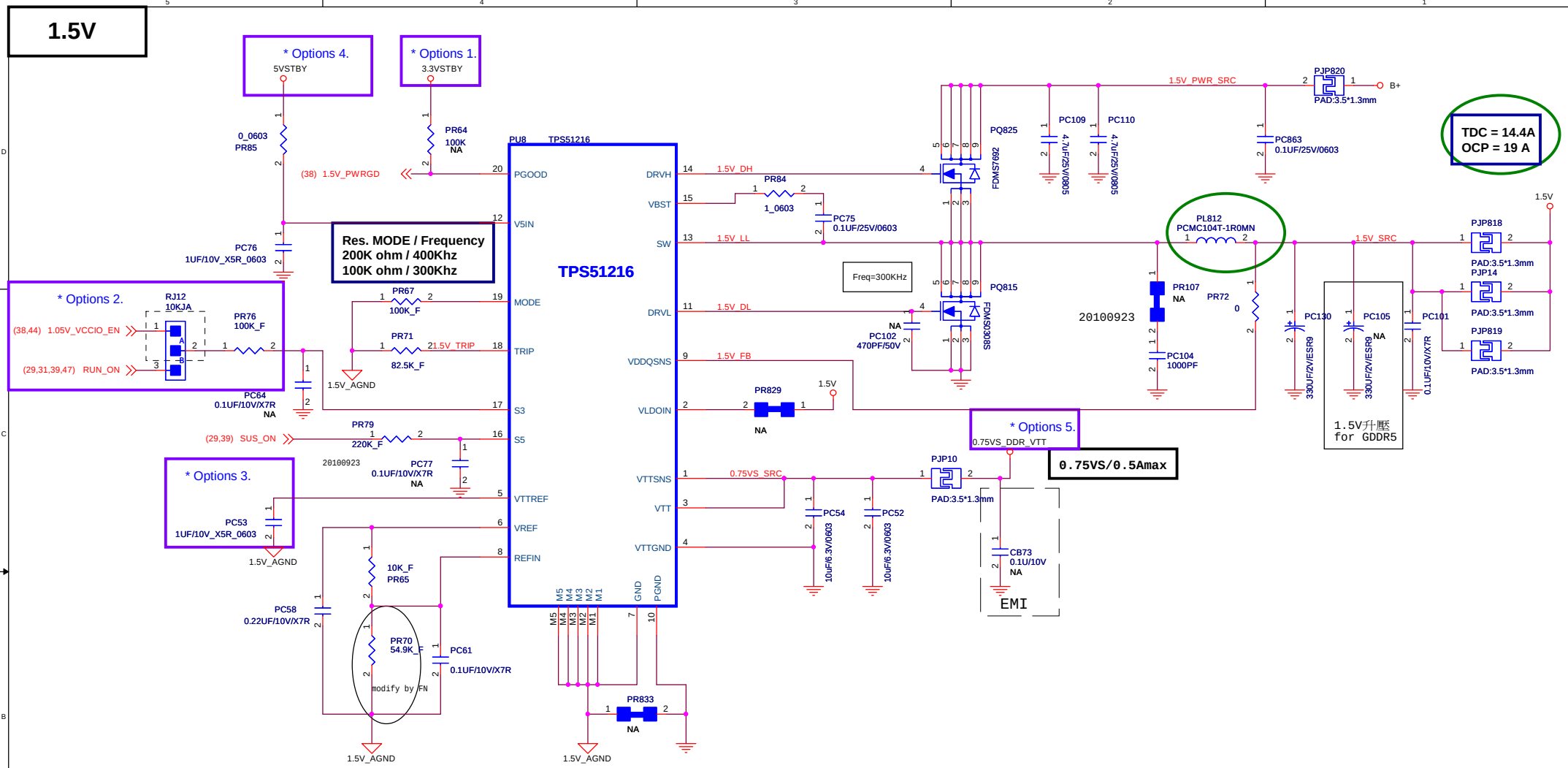


Table 1. S3 and S5 Control Table

STATE	S3	S5	VTTREF	VTT
S0	H	H	1	1
S3	L	H	1	0 (high-Z)
S4/S5	L	L	0 (discharge)	0 (discharge)

INTEL HR / AMD DANUBE

Options 1 - 3.3VSTBY / 3.3V

Options 2 - RUN_ON / SUS_ON

Options 3 - DDR_VTTR / V_DDR_VTT

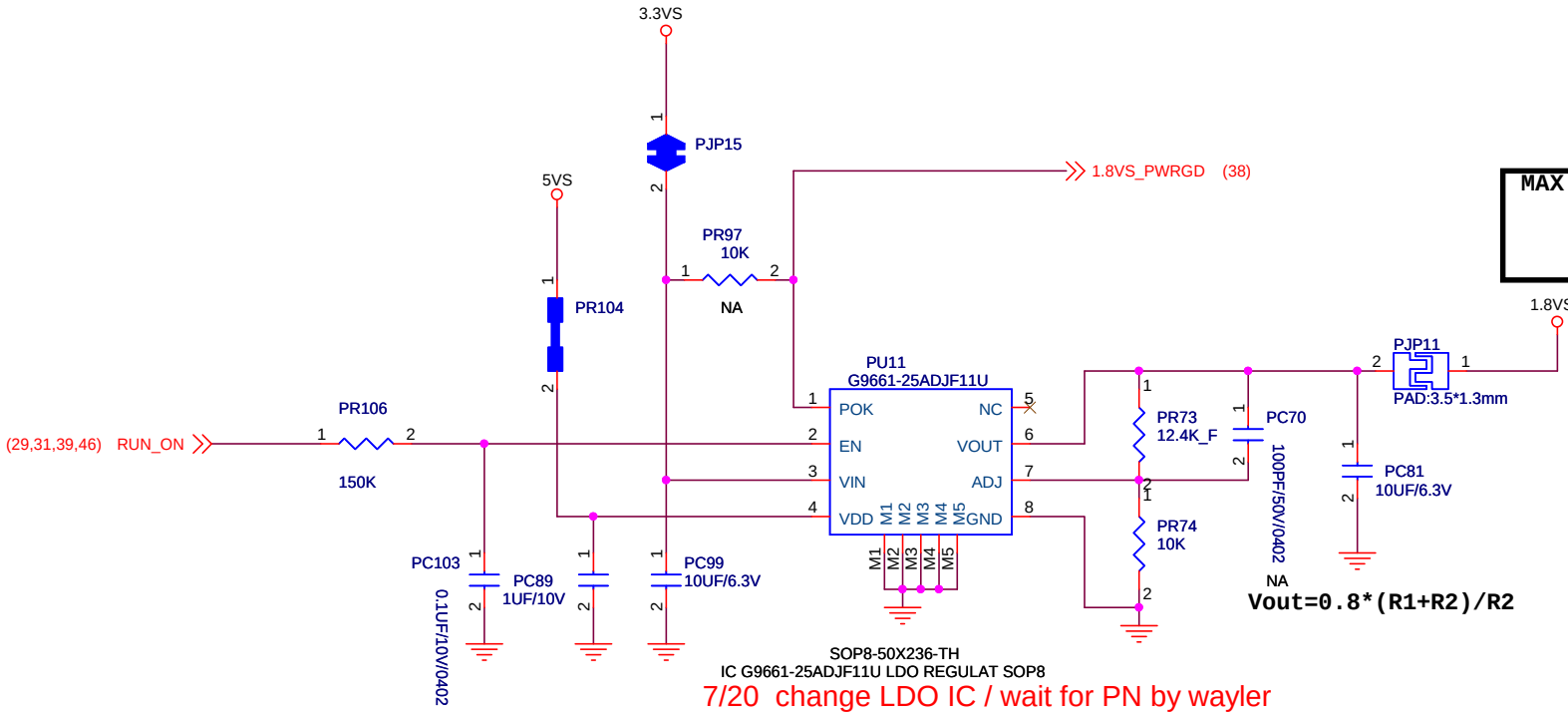
Options 4 - 5VSTBY / 5V

Options 5 - 0.75VS_DDR_VTT / 0.75V_DDR_VTT

FLEX Computing

Project Name : H710DI1	Title : DDR_PWR(TPS51216)
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 46 of 63

1.8VS



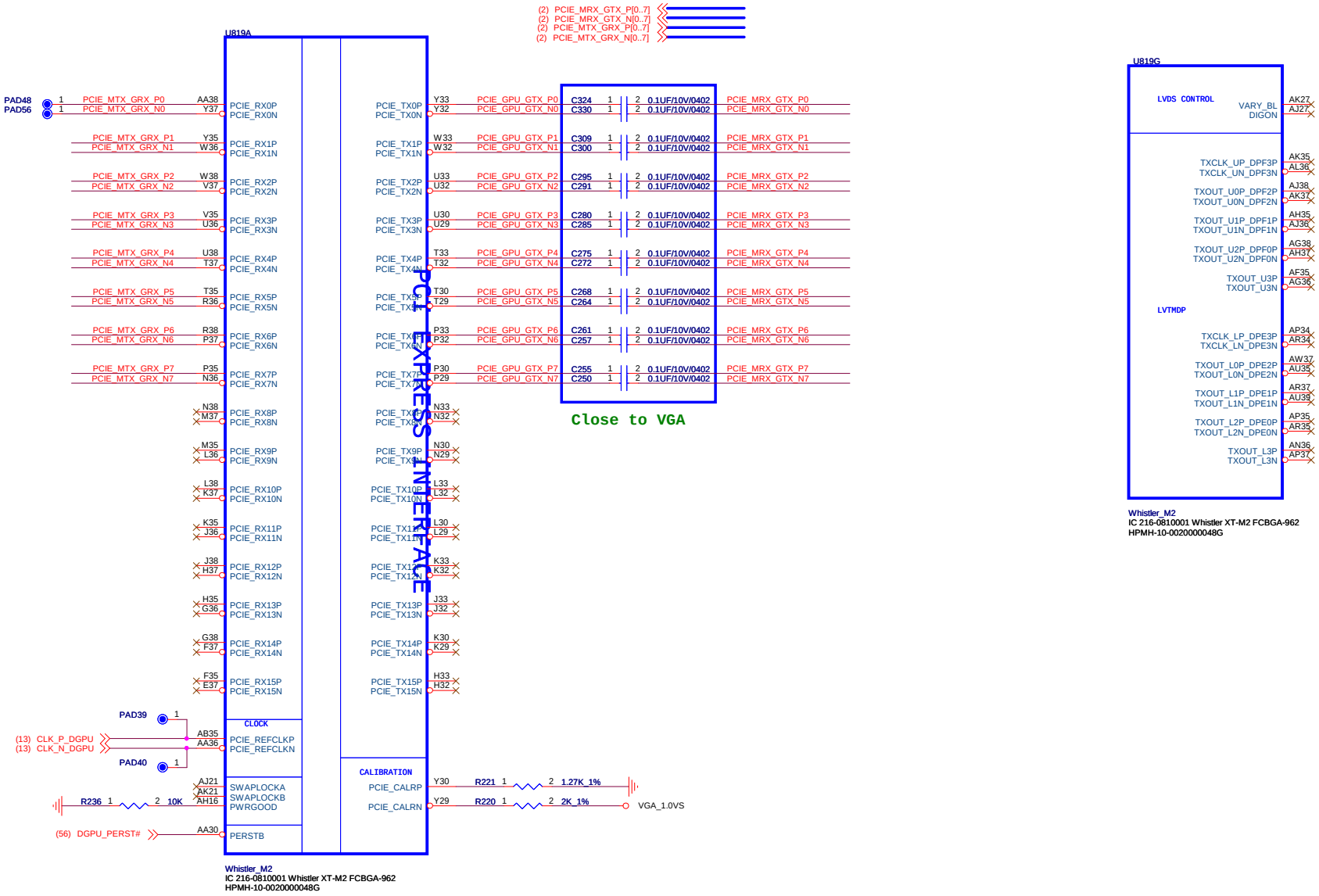
MAX:
UI=1.45A

1.8VS for CPU & PCH

Vout=0.8*(R1+R2)/R2

7/20 change LDO IC / wait for PN by wayler

FLEXComputing		
Project Name : H710DI1	Title : 1.8VS	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 47 of 63	



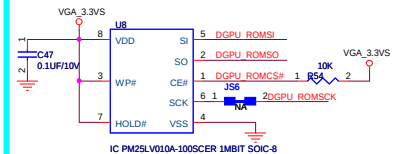
GPU TYPE	PN
Whistler XT	HPMH-10-0020000048G
Seymour-XT	HPMH-10-0020000049G

FLEXComputing

Project Name : H710DI1	Title : Capilano_1/5_PCIE/LVDS
Size :	Document Number : HPMH-40GAB6600-B130 / Rev : B
Date: Monday, November 08, 2010	Sheet : 48 of 63

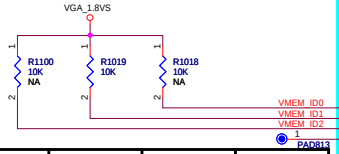
For del vBIOS ROM design:
1.P49 -U8,C47,R54
2.P53 -R1001,R1002,R1015

For GDDR5 used

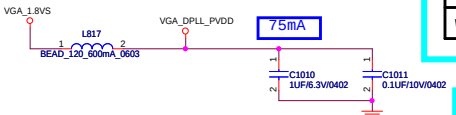


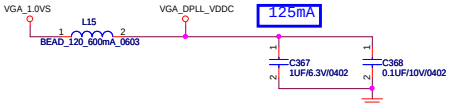
NA for del vBIOS ROM design.

VMEM_ID



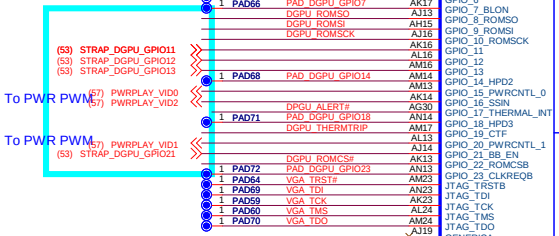
	DVPDATA_2	DVPDATA_1	DVPDATA_0
Seymour Hynix H5GQ2H24MFR-T2C (128Mx16) x4pcs	0	0	0
Seymour Samsung K4G20325FC-HC04 (128Mx16) x4pcs	0	0	1
Whistler Hynix H5GQ1H24AFR-T2C (64Mx16) x8pcs	0	1	0
Whistler Samsung K4G10325FE-HC04 (64Mx16) x8pcs	0	1	1
Seymour Hynix H5GQ1H24AFR-T2C (64Mx16) x4pcs	1	0	0
Seymour Samsung K4G10325FE-HC04 (64Mx16) x4pcs	1	0	1
Seymour Elpida EDW2032BABG-50-F(128Mx16) x4pcs	1	0	1
Whistler Elpida EDW1032BABG-50-F(64Mx16) x8pcs	1	1	1

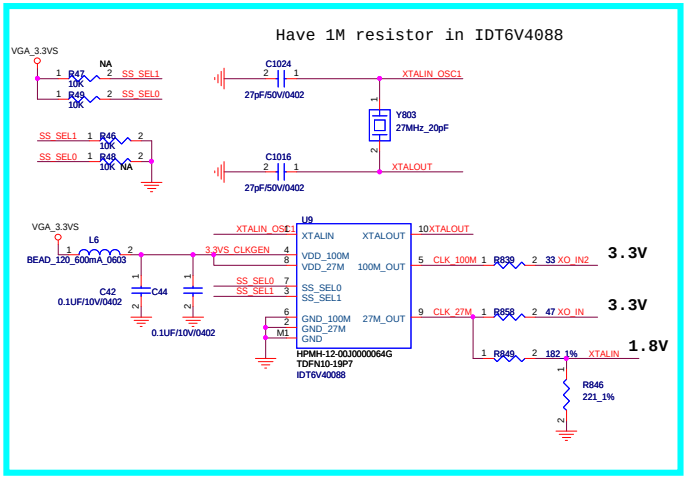


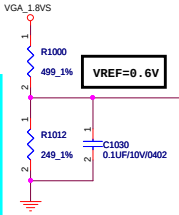


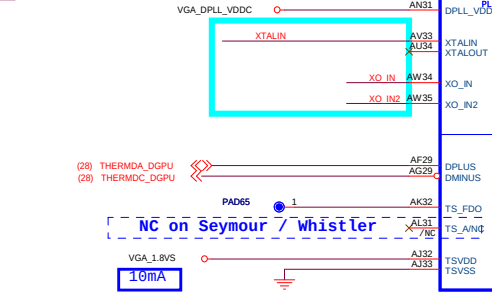
100 MHz Spread Selection Table

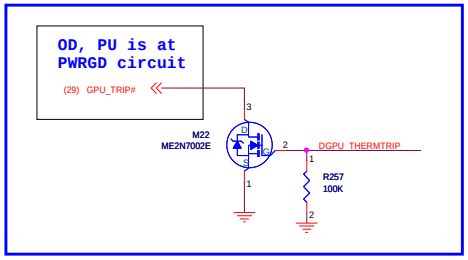
PIN3	PIN7	PIN5	
S1	S0	Down Spread%	
L	L	OFF	
L	M	-0.5	
L	H	-2.5	
M	L	-0.25	
M	M	-0.75	
M	H	-1.0	
H	L	-1.5	
H	M	-2.0	Default
H	H	-3.0	

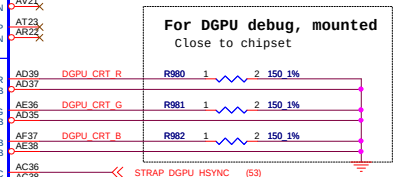


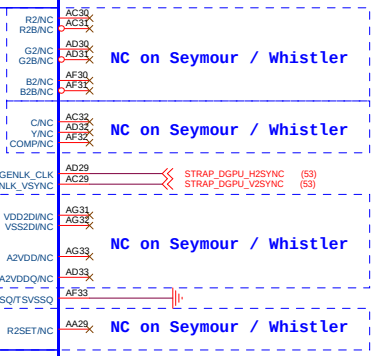


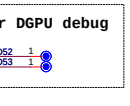






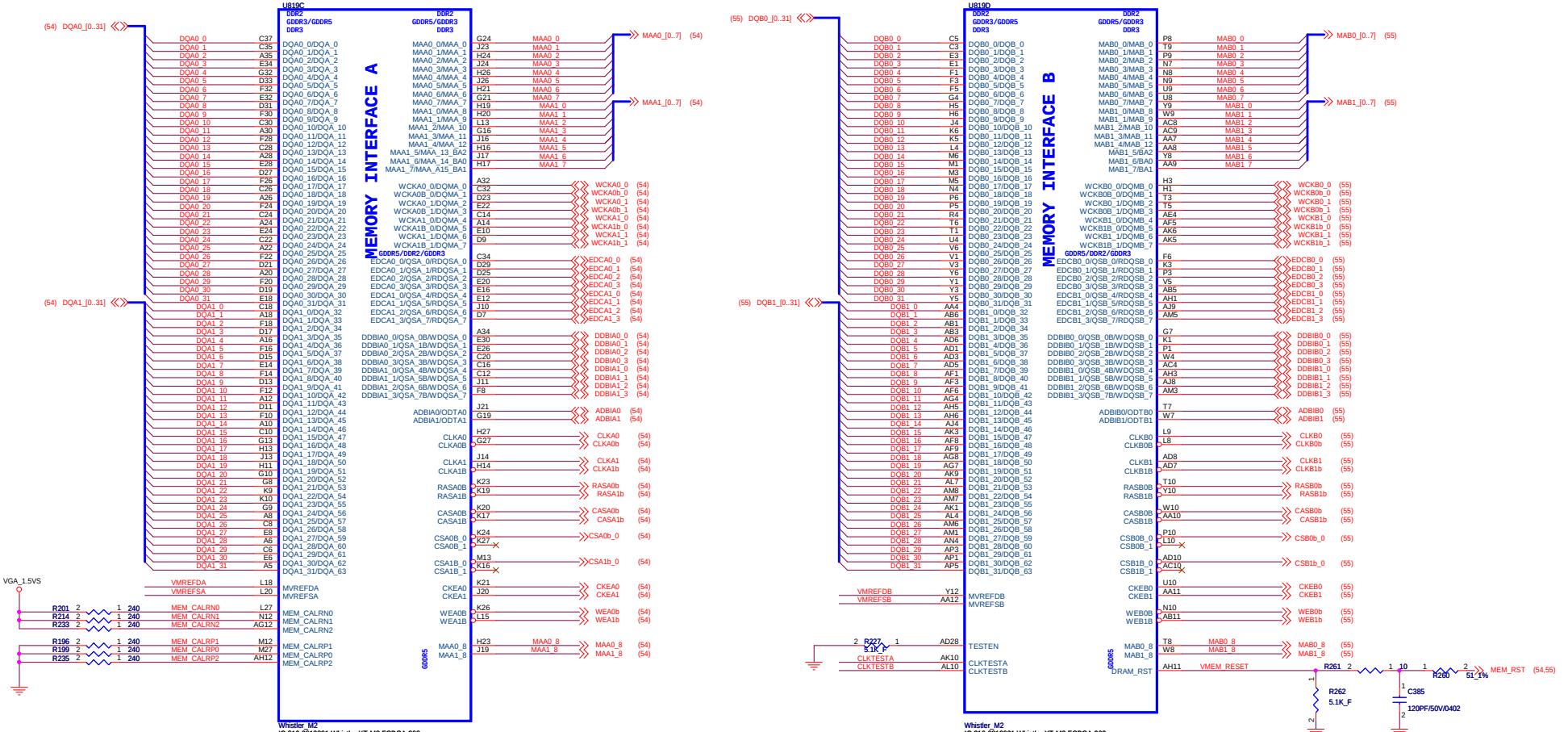






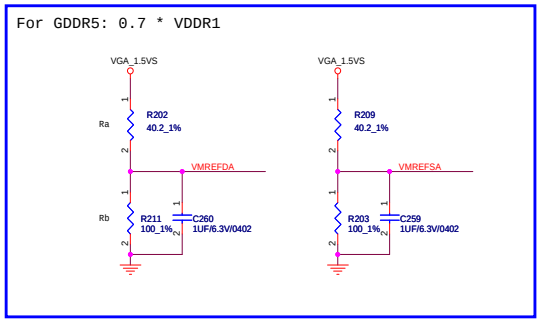
FLEX Computing

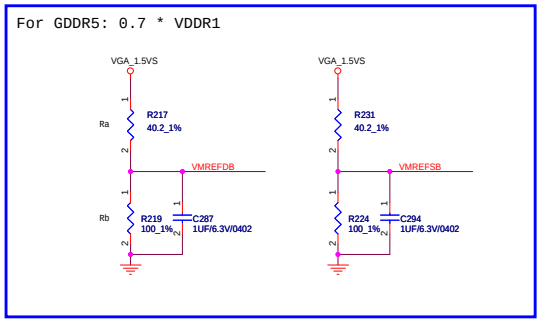
Project Name : H710DI1	Title : Capilano_2/5_DP/DAC/GPIO	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 49 of 63	

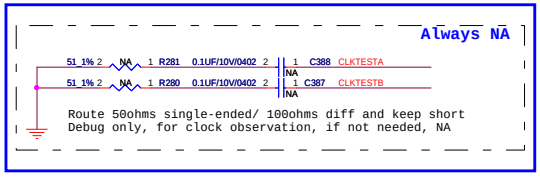


Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

VRAM TYPE		PN
Hynix H5GQ1H24AFR-T2C	64MX16(32MX32)	HPMH-14-0030000001G
Hynix H5GQ2H24MFR-T2C	128MX16(64MX32)	HPMH-14-0030000002G
SAMSUNG K4G10325FE-HC04	64MX16(32MX32)	HPMH-14-0030000003G
SAMSUNG K4G20325FC-HC04	128MX16(64MX32)	HPMH-14-0030000004G
Elpida EDW1032BABG-50-F	64MX16(32MX32)	HPMH-14-0030000005G
Elpida EDW2032BABG-50-F	128MX16(64MX32)	HPMH-14-0030000006G

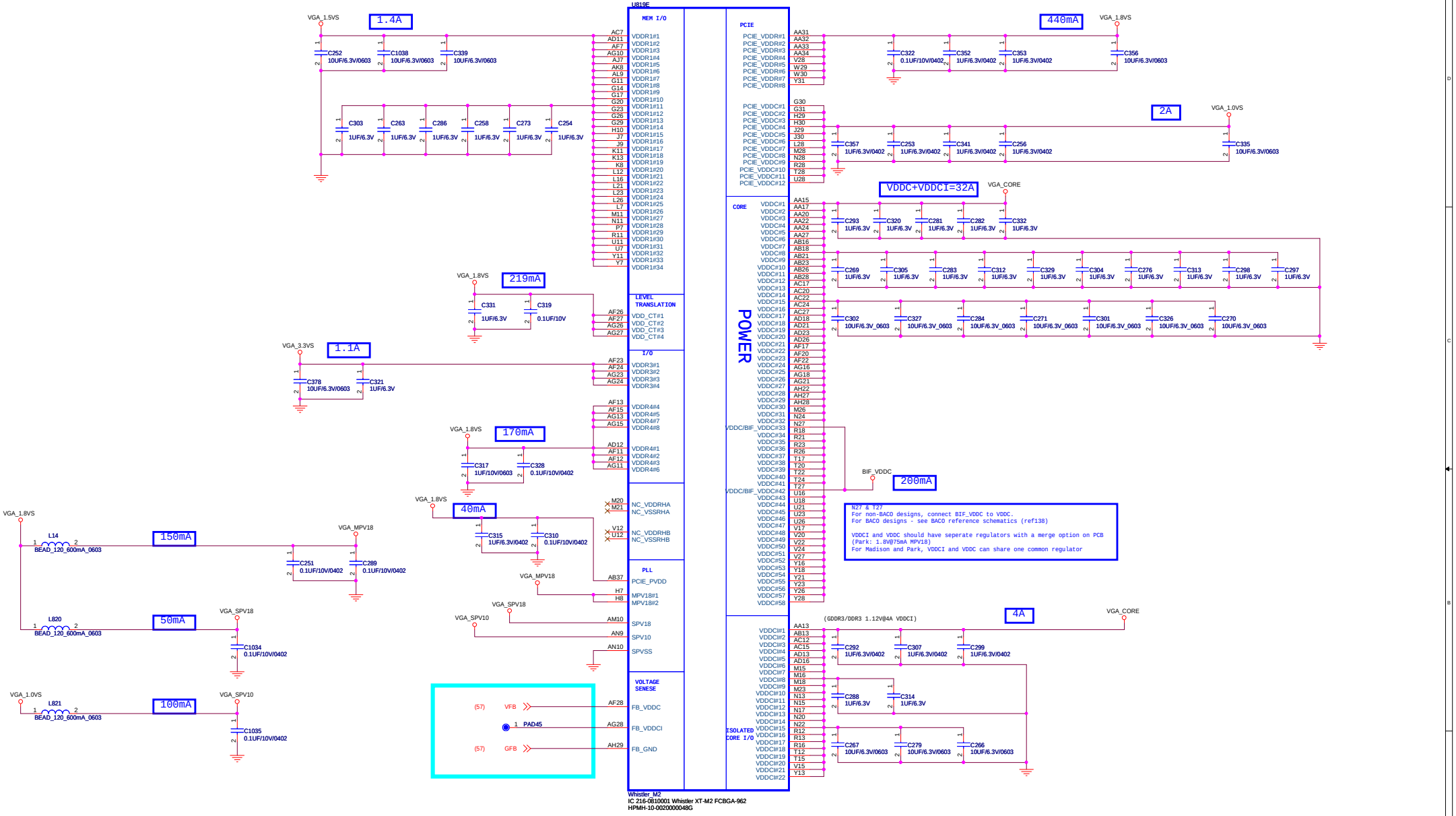






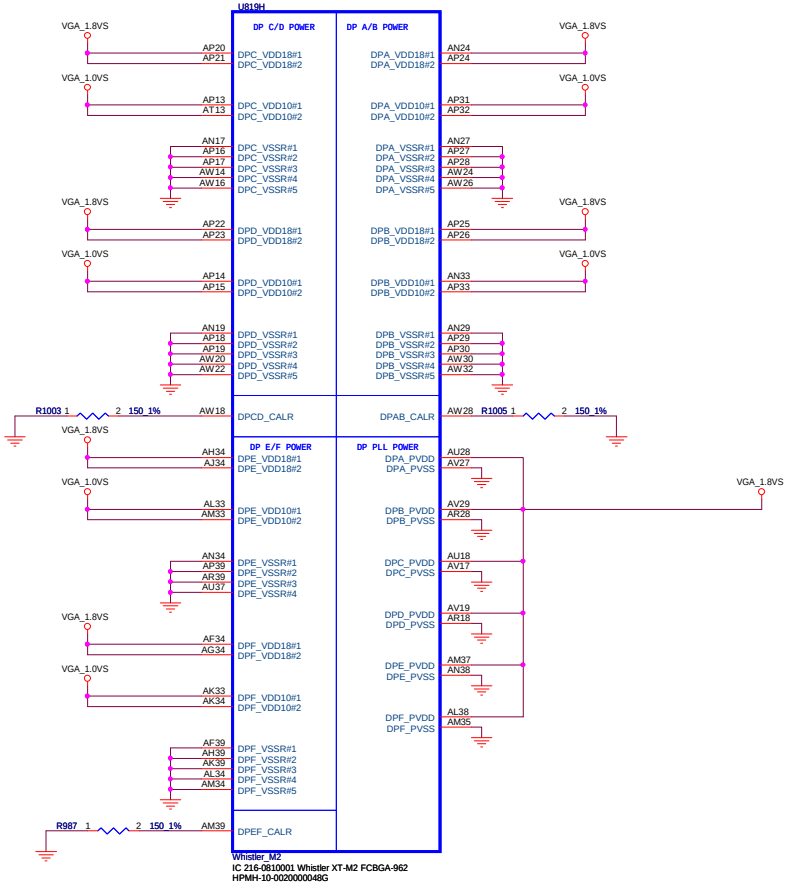
FLEX Computing

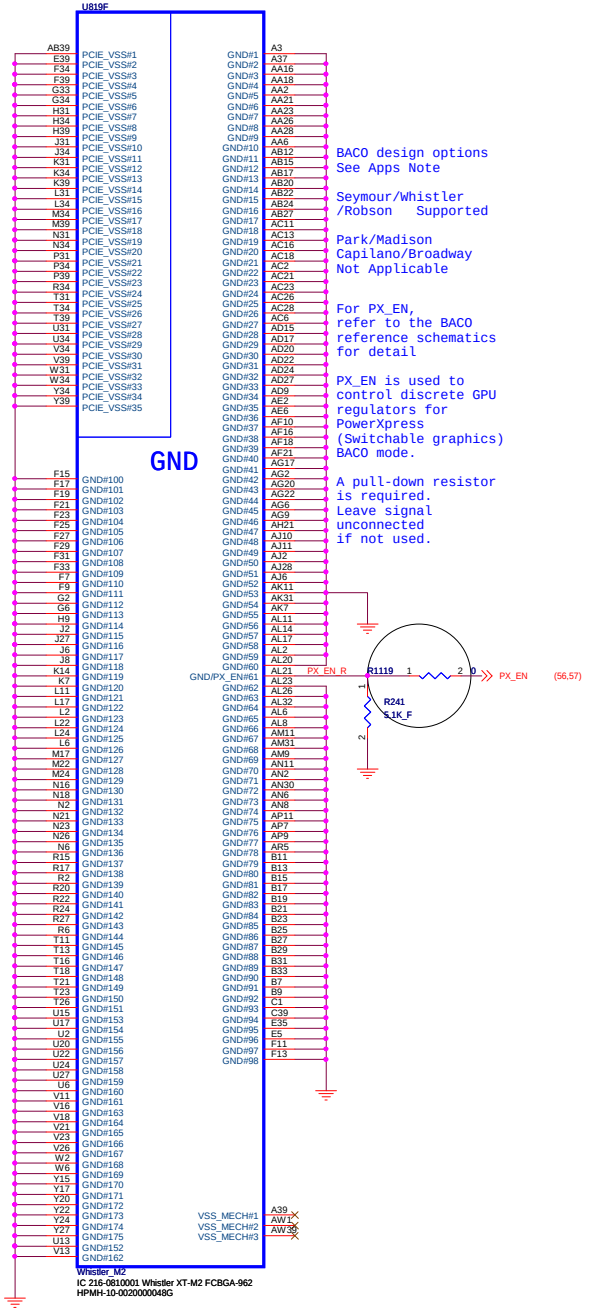
Project Name : H710DI1	Title : Capilano_3/5_VRAM_ IF
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 50 of 63



FLEX Computing

Project Name : H710DI1	Title : Capilano_4/5_PWR_IO
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 51 of 63





BACO design options
See Apps Note

Seymour/Whistler
/Robson Supported

Park/Madison
Capilano/Broadway
Not Applicable

For PX_EN,
refer to the BACO
reference schematics
for detail

PX_EN is used to
control discrete GPU
regulators for
PowerXpress
(Switchable graphics)
BACO mode.

A pull-down resistor
is required.
Leave signal
unconnected
if not used.

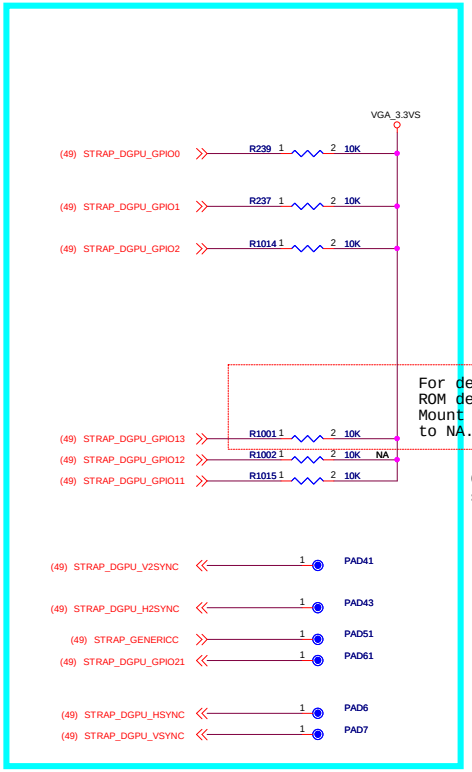
FLEX Computing			
Project Name : H710DI1		Title : Capilano_5/5_PWR_DAC/GND	
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010		Sheet : 52 of 63	

Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AC32 on M2	NC	DAC2 Output-C on M2 package
Ball AA29 on M2	NC	R2SET on M2 package
Ball AD32 on M2	NC	DAC2 Output- Y
Ball AG33 on M2	NC	A2VDD
Ball AD33 on M2	NC	A2VDDQ
Ball AF33 on M2	TSVSSQ	A2VSSQ
Ball AG33 AG32 on M2	NC	VDD2DI/VSS2DI
H2SYNC	GENLK_CLK: (3.3V) Reference clock input (3.3V) for pixel PLL received from frame-lock/ gen-lock interface	H2SYNC
V2SYNC	GENLK_VSYNC (3.3V) Frame timing indicator.Output to frame-lock/genlock interface	V2SYNC

Signal	Seymour/Whistler	Robson/Park Medison/Capilano Broadway
Ball AJ21 on M2 Ball AG13 on S3	SWAPLOCKA SwaplockA/B signals can be optionally used on a multi-GPU design with multiple display outputs to allow all displays in a group (group A or group B) to update at the same time and have synchronous left/right stereo timing. Genlock of the GPUs is also needed, either via a genlock system, or by feeding all GPUs with the same reference clock. Also connecting SwaplockB is preferred, but not required. SwaplockA/B are open drain, 3.3V signals. If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AJ21 is NC on M2 packages Ball AG13 is R2SET on S3 package
Ball AK21 on M2 Ball H12 on S3	SWAPLOCKB – see above On a multi-gpu design,SwaplockB from all GPUs are connected together with an external pull-up resistor (10K Ohms). If this feature is not required, these signals can be used as 3.3V GPIOs or left unconnected on the PCB.	Ball AK21 is NC on M2 packages Ball AH12 is DAC2 Output- on S3 package

CONFIGURATION STRAPS

STRAPS	PIN	DESCRIPTION	ASIC Deault	Status
TX_PWRS_ENB	GPIO0	Transmitter (Tx) power savings enable. 0: 50% Tx output swing 1: Full Tx output swing (DEFAULT)	0 Internal Pull Down	Mounted
TX_DEEMPH_EN	GPIO1	PCI Express transmitter deemphasis enable. 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (DEFAULT)		Mounted
RESERVED	GPIO2	0 : PCIe device as 2.5 GT/s capable 1 : PCIe device as 5.0 GT/s capable (DEFAULT)		Mounted
VGA_DIS	GPIO9	VGA disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0 : VGA Controller capacity enabled (DEFAULT) 1 : The device will not be recognized as the system's VGA controller		NA NA
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable the external BIOS ROM device: 0 - Disable external BIOS ROM device (DEFAULT) 1 - Enable external BIOS ROM device		Mounted
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	BIOS_ROM_EN = 1, Config[2:0] defines the ROM type. BIOS_ROM_EN = 0, Config[2:0] defines the primary memory aperture size Size of the primary memory apertures CONFIG[2:0] 128 MB 000 256 MB 001 (DEFAULT) 64 MB 010 32 MB 011		Mounted NA Mounted
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS L: Ignore VIP Device Strap (DEFAULT) H: Enable VIP Device Strap		NA
RESERVED RESERVED RESERVED RESERVED	H2SYNC GENERICC GPIO8 GPIO21_BB_EN			NA NA NA NA
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function (DEFAULT) 0 1 Audio for DisplayPort only 1 0 Audio for DisplayPort and HDMI if dongle is detected 1 1 Audio for both DisplayPort and HDMI		NA NA



GPIO 13,12,11 CONFIG[2:0] =>101 for PM25LV010

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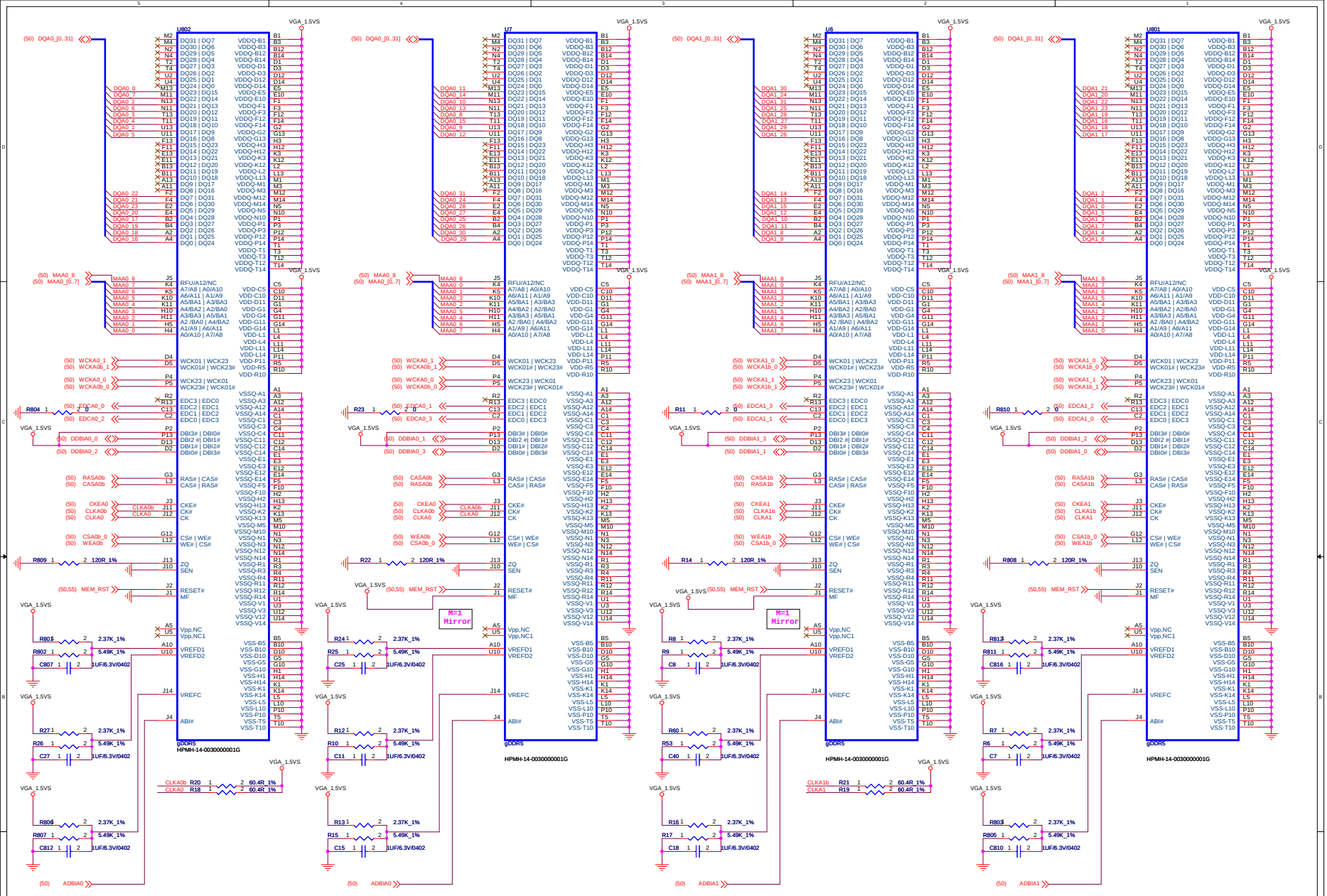
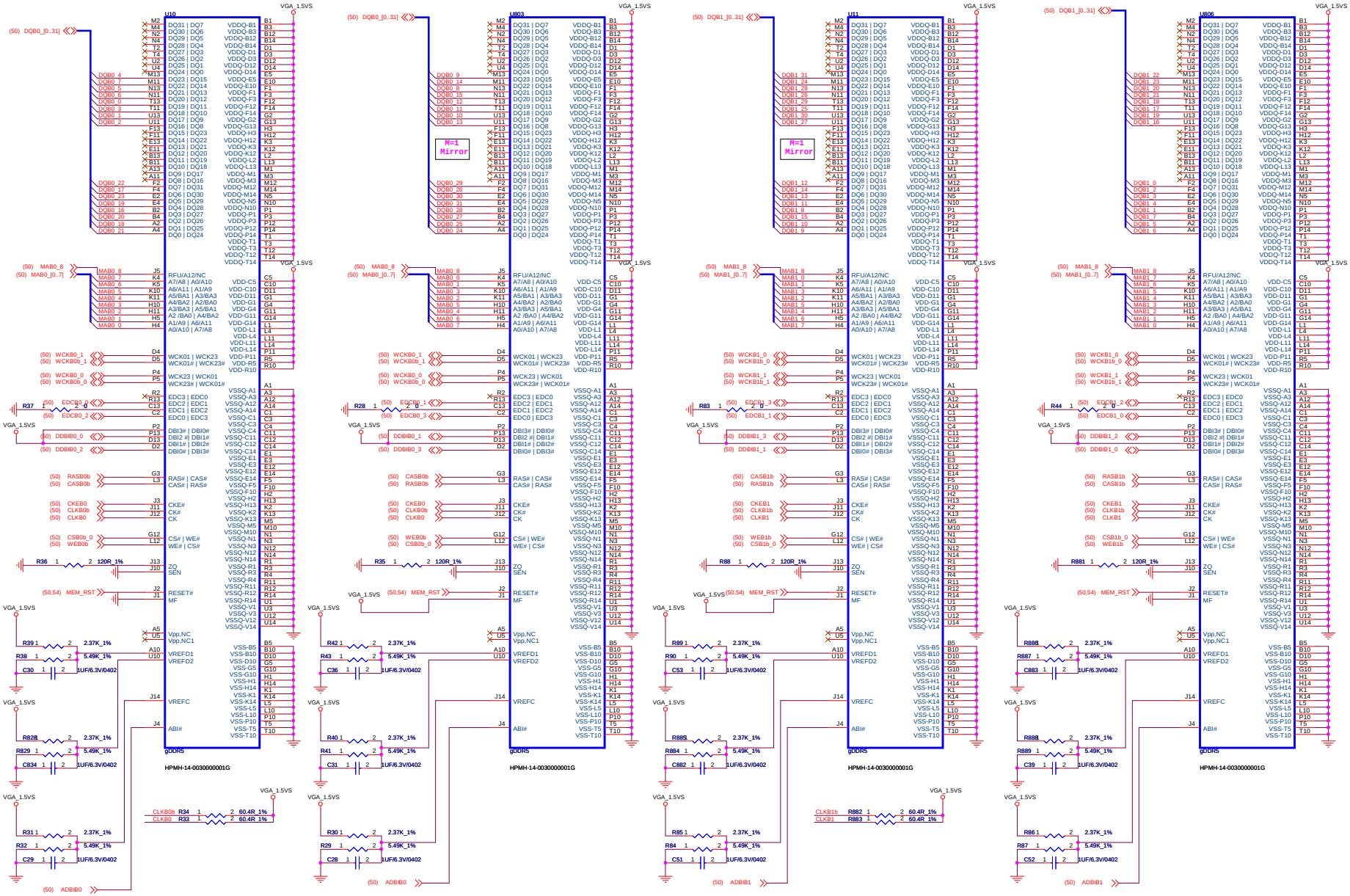
Project Name : H710DI1	Title : Capilano_STRAPS/ChipDiff	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 53 of 63	


U802
U7
U6
U801
VGA_1.5VS
gDDR5
HPMH-14-0030000001G
M=1
Mirror
Decoupling caps for clamshell configuration:
1X 10uf per 2 clamshell DRAM
8 X 1uf per 2 clamshell DRAM
NA for Seymour
GDDR5 Memory Channel A X16 Mode
FLEXComputing
Project Name : H710DI1
Title : Capilan_VRAM GDDR5 64MX16 A
Size : B
Document Number : HPMH-40GAB6600-B130
Rev : B
Date: Monday, November 08, 2010
Sheet : 54 of 63


U10
U803
U11
U806
VGA_1.5VS
(50) DQB0_[0..31]
(50) DQB1_[0..31]
(50) MAB0_8
(50) MAB0_[0..7]
(50) MAB1_8
(50) MAB1_[0..7]
M=1 Mirror
gDDR5
HPMH-14-0030000001G
(50) WCKB0_1
(50) WCKB0b_1
(50) WCKB0_0
(50) WCKB0b_0
(50) WCKB1_0
(50) WCKB1_1
R37 EDCB0_0
EDCB0_2
R28 EDCB0_1
EDCB0_3
R83 EDCB1_3
EDCB1_1
R44 EDCB1_2
EDCB1_0
DDBIB0_0
DDBIB0_2
DDBIB0_1
DDBIB0_3
DDBIB1_3
DDBIB1_1
DDBIB1_2
DDBIB1_0
RASB0b
CASB0b
RASB1b
CASB1b
CKEB0
CLKB0b
CLKB0
WEB0b
CSB0b_0
CKEB1
CLKB1b
CLKB1
WEB1b
CSB1b_0
R36 120R_1%
R35 120R_1%
R88 120R_1%
R881 120R_1%
(50,54) MEM_RST
R39 2.37K_1%
R38 5.49K_1%
C30 1UF/6.3V/0402
R828 2.37K_1%
R829 5.49K_1%
C834 1UF/6.3V/0402
R31 2.37K_1%
R32 5.49K_1%
C29 1UF/6.3V/0402
(50) ADBIB0
R42 2.37K_1%
R43 5.49K_1%
C36 1UF/6.3V/0402
R40 2.37K_1%
R41 5.49K_1%
C31 1UF/6.3V/0402
R30 2.37K_1%
R29 5.49K_1%
C28 1UF/6.3V/0402
CLKB0b R34 60.4R_1%
CLKB0 R33 60.4R_1%
R89 2.37K_1%
R90 5.49K_1%
C53 1UF/6.3V/0402
R885 2.37K_1%
R884 5.49K_1%
C882 1UF/6.3V/0402
R85 2.37K_1%
R84 5.49K_1%
C51 1UF/6.3V/0402
(50) ADBIB1
CLKB1b R882 60.4R_1%
CLKB1 R883 60.4R_1%
R886 2.37K_1%
R887 5.49K_1%
C883 1UF/6.3V/0402
R888 2.37K_1%
R889 5.49K_1%
C39 1UF/6.3V/0402
R86 2.37K_1%
R87 5.49K_1%
C52 1UF/6.3V/0402
C835 C833 C13 C6 C802 C804 C805 C24 C880
C803 C16 C806 C809 C19 C37 C836 C38 C12
1UF/6.3V/0402
10UF/6.3V/0603
Decoupling caps for clamshell configuration:
1X 10uf per 2 clamshell DRAM
8 X 1uf per 2 clamshell DRAM
GDDR5 Memory Channel B X16 Mode
FLEX Computing
Project Name : H710DI1
Title : Capilan_VRAM GDDR5 64MX16 B
Size :
Document Number : HPMH-40GAB6600-B130
Rev : B
Date: Monday, November 08, 2010
Sheet : 55 of 63

UI NA
DI Mount

AMD recommand Rds(on): 140m

M20B AM3922-T1-PF
M20A AM3922-T1-PF
VGA_1.0VS
VGA_1.0VS_M
PX_EN_PCIE_VDDC
200mA
BIF_VDDC
C247 10UF/6.3V/0603

AMD recommand Rds(on): 21m

M21 N-CH/ME2306D-G
M25 N-CH/ME2306D-G
VGA_CORE
VGA_CORE_M
PX_EN_VGA_CORE
HPMH-18-0020000170G
MOS N-ch ME2306D-G 30V 3.9A SOT-23 <MOUNTED>

ME2306D:
Vgs(th) : 1.0V(min),3.0V(max)
Rds(on) : 31m@Vgs = 10V(MAX)
Rds(on) : 52m@Vgs = 4.5V(MAX)
Id : 3.9A(Max)

5VS
R277 1K
R268 1K
20101022
PX_EN_VGA_CORE
PX_EN_PCIE_VDDC
M813 ME2N7002E
M23 ME2N7002W
(17,57) BACO_PWROK

TDC : 9A
For 8 pcs GDDR5 + DGPU

3.3VSTBY
R332 10K
15V_ALW
R1034 330K
1.5V
Q801 FDMS0308S
VGA_1.5VS
C32 22UF/6.3V/0805
C1053 0.1UF/25V/0603
VGA_1.5VS_EN
Q802 ME2N7002E
DGPU_EN#
Q9 ME2N7002E
DGPU_PWR_EN
PQ13 ME2N7002E-G
PX_EN (52,57)

PX_EN =0, for Normal Operation
PX_EN =1, for BACO MODE

TDC: 1.1A

15V_ALW
R401 20K
3.3VS
M52 ME2306D-G
VGA_3.3VS
R1121 10K
C600 0.1u/25V_0603
VGA_3.3VS_EN
R1120 1K
M53 ME2N7002E-G
M828 ME2N7002E-G
20101105

VGA_3.3VS EN
add 10k for
power down

PWROK_VGA_1.0VS
5VS
1.5V
PR818 NA
PJP808
R1035 28.7K_F
DGPU_PWR_EN
PU803 G9661-25ADJF11U
POK NC
EN VOUT
VIN ADJ
VDD MGND
C1070 0.1UF/10V/0402
PC822 1UF/10V
PC828 10UF/6.3V
SOP8-50X236-TH
IC G9661-25ADJF11U LDO REGULAT SOP8
PR814 2.49K_F
PC818 470PF/50V/X7R/0402
PR816 10K
PC819 10UF/6.3V
PJP806
PAD:3.5*1.3mm
VGA_1.0VS
EC816 0.1U/10V NA
EMI
Vout=0.8*(R1+R2)/R2

TDC : 2.22A

3.3VS
R402 10K
PWROK_VGA_1.0VS
PR827
PWROK_VGA_1.8VS
PR828
DGPU_PWR_EN
PR824 47K
D816 SDMK0340_40V_30mA
20101105
VGA_1.8VS EN
add diode for
power down.
Need mount

PWROK_VGA_1.8VS
PR823 NA
PJP809
PU804 G9661-25ADJF11U
PC826 0.1UF/10V/0402
PC824 1UF/10V
PC827 10UF/6.3V
SOP8-50X236-TH
IC G9661-25ADJF11U LDO REGULAT SOP8
PR817 12.4K_F
PC820 100PF/50V/X7R/0402
PR815 10K
PC821 10UF/6.3V
PJP807
PAD:3.5*1.3mm
VGA_1.8VS
Vout=0.8*(R1+R2)/R2

TDC : 1.1A

7/20 change LDO IC / wait for PN by wayler

UI NA
DI Mount

3.3VS
R400 10K
DGPU_PWR_EN
DGPU_PWR_EN (29,57)
M50 ME2N7002E
(16) DGPU_PWR_EN#

L	H
DGPU ON	DGPU OFF

(3,11,16,27,29,30,31,36) PCH_PLT_RST#
(16) DGPU_HOLD_RST#
RJ8
DGPU_PERST# (48)
0JB

UI NA
DI Mount(B)

FLEX Computing

Project Name : H710DI1	Title : DGPU_RUN PWR, PWRGD, BACO
Size :	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 56 of 63

VID4(PP2) (GPIO16)	VID3(PP1) (GPIO20)	VID2(PP0) (GPIO15)	VGA_CORE
0	0	1	1.05V
1	0	0	0.900V

VID							V_{DAC} (V)
6	5	4	3	2	1	0	
0	1	0	0	1	0	0	1.0500
0	1	1	0	0	0	0	0.9000

	15W	15W
TDC	15A	35A
OCP	22.5A	50A

深藍色框內爲15W NA

深藍色框內爲15W NA

深藍色框內爲15W NA

深藍色框內爲15W NA

深藍色框內爲15W NA

深藍色框內爲15W NA

15W 時需改值

15W 時MOUNTED

**TPS51728

TPS51217

5VS PU maybe leakage in BACO. Change to VGA_3.3VS

VGA_CORE EN change R and C for power down

OD, PU is at PCH/SB

PX_EN =0, for Normal Operation
PX_EN =1, for BACO MODE

PC17
35W==>HPMH-31-0020000064G 0.22u/25v_0603
15W==>HPMH-31-141047-950G 0.1uF/25V/0603

PL803
35W==>HPMH-32-800562-020G 0.56uH 25A PCMC104T-R56MN
15W==>HPMH-32-4000000181G 1uH 18A PCMC104T-1R0MN

PR6
35W==>HPMH-30-220021-990G 20K_0402_F
15W==>HPMH-30-154921-990G 54.9K_0402_F

PR13
35W==>HPMH-30-001006-990G 10_0402_J
15W==>HPMH-30-107521-990G 7.5K_0402_F

15W 時需改值

Seymour GDDR5 (15W)	
VID0	VGA_CORE
0	0.9
1	1.1

FLEX Computing

Project Name : H710DI1	Title : VGA_CORE(TPS51728)35W
Size : Custom	Document Number : HPMH-40GAB6600-B130 Rev : B
Date: Monday, November 08, 2010	Sheet : 57 of 63

FID9 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID802 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID11 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID804 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID801 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID10 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID803 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

FID7 FIDUCIAL CAD-016
NC, NO CONNECT TO ANY.

H26 PTH8_2.8 THR315B276_110 NA
H27 PTH8_2.8 THR315B276_110 NA
H25 PTH6.8_2.8 THR268_110 NA

CPU
H22 PTH7_4.7 THR276B189_150 NA
H23 PTH7_4.7 THR276B189_150 NA
H16 PTH7_4.7 THR276B189_150 NA
H17 PTH7_4.7 THR276B189_150 NA

H20 PTH6B7_2.8 THR236B276_110 NA
H12 PTH7_2.8 THR276B315_110 NA
H7 PTH7_2.8 THR276B315_110 NA AG
H8 PTH7_2.8 THR213B315_110 NA
H15 PTH7_2.8 THR276B315_110 NA

VGA
H18 PTH7_4.7 THR276B189_150 NA
H19 PTH7_4.7 THR276B189_150 NA
H13 PTH7_4.7 THR276B189_150 NA
H14 PTH7_4.7 THR276B189_150 NA

PCH
H11 PTH7_4.6 THR122B276_083
H10 PTH7_4.6 THR122B276_083

H9 PTH7_2.8 THR268B276_110 NA

H21 PTH7_2.8 NPTH106X087 NA
H24 PTH7_2.8 NPTH106X087 NA
H6 PTH7_2.8 NPTH087 NA

5VSTBY
放在gfx power 兩邊
C1124 C1125 C1128 C1127 0.1UF/10V/0402
1.05VS
C1131 C1130 C1145 0.1UF/10V/0402
for Intel Reserved

ME1 ME4 ME5 NA
ME2
20101103

5VS 5VSTBY
C820 C46 0.1UF/10V/0402 NA
C1008 C506 C163 0.1UF/10V/0402

3.3VS CPU_CORE
C535 C512 0.1UF/10V/0402 NA
C1139 C1140 C1141 C1142 0.1UF/10V/0402

1.5V
C533 C541 C539 C1143 C1144 0.1UF/10V/0402
CB853 0.1UF/10V/0402
20101102

5VSTBY 3.3VS
C496 C518 C181 C126 C84 C337 C1136 C1137 0.1UF/10V/0402 NA
C1138 0.1UF/10V/0402
CB879 0.1UF/10V/0402
20101105
20100923

3.3VS VGA_1.5VS
C393 C200 C201 0.1UF/10V/0402 NA
C473 0.1UF/10V/0402
C215 0.1UF/10V/0402 NA
C236 0.1UF/10V/0402
CB852 0.1UF/10V/0402
20101102

3.3VS VGA_CORE
C390 0.1UF/10V/0402 NA

5VSTBY 1.05VS
C49 0.1UF/10V/0402

1.05VS 3.3VS
C164 C323 C526 C60 C1133 C1134 C1135 0.1UF/10V/0402 NA
20100923

3.3VSTBY 3.3VS
C509 C532 0.1UF/10V/0402

3.3VS 1.05VS
C373 C229 0.1UF/10V/0402 NA

3.3VS 5VSTBY
C499 0.1UF/10V/0402 NA

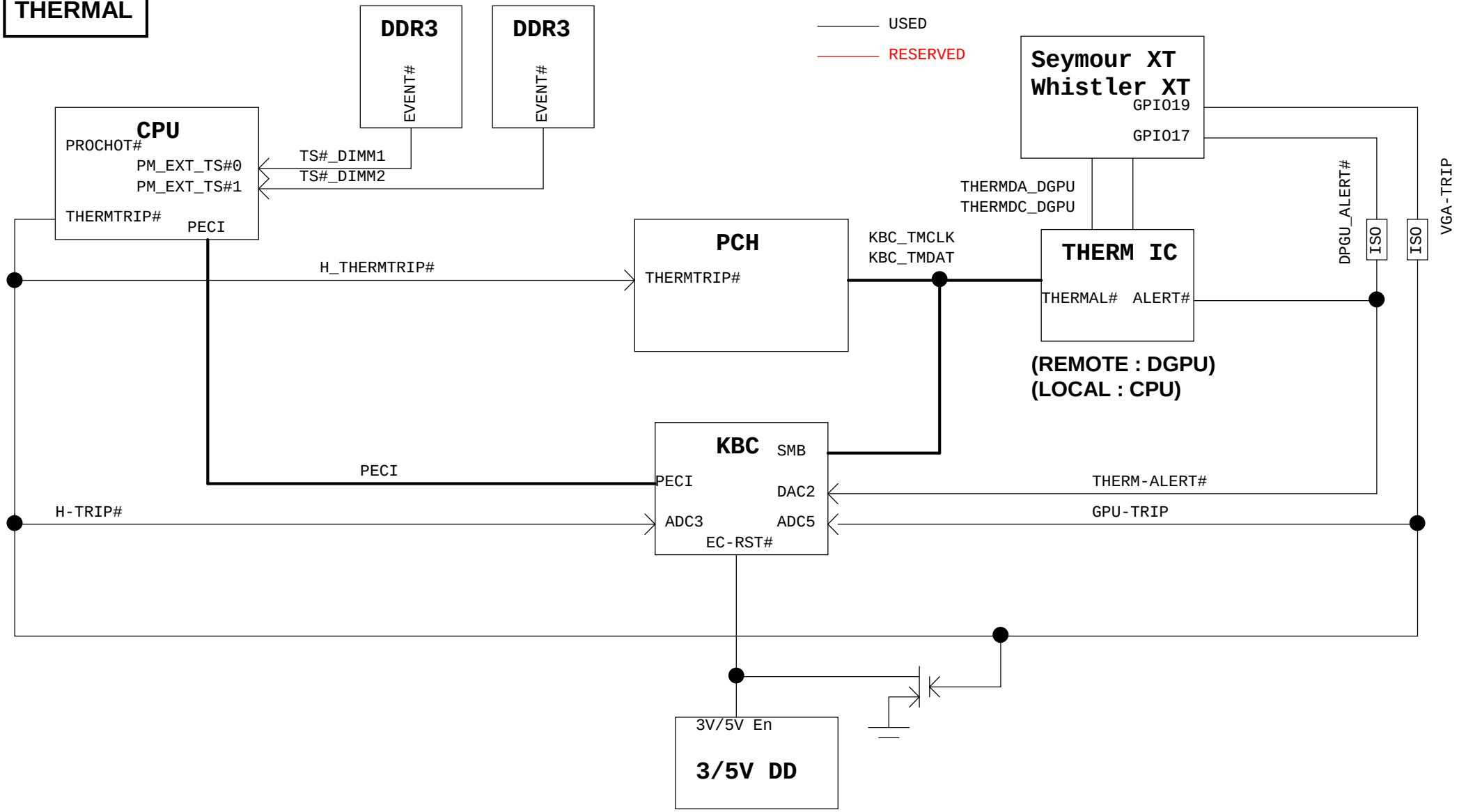
5VSTBY B+
CB49 0.1UF/25V
C1150 1UF/25V
CB4 1UF/25V
CB3 1UF/25V

B+ 3.3VS
CB90 CB848 CB122 CB106 CB5 CB48 CB878 CB803 CB847 CB849 CB850 CB851 0.1UF/25V
20101102

FLEXComputing

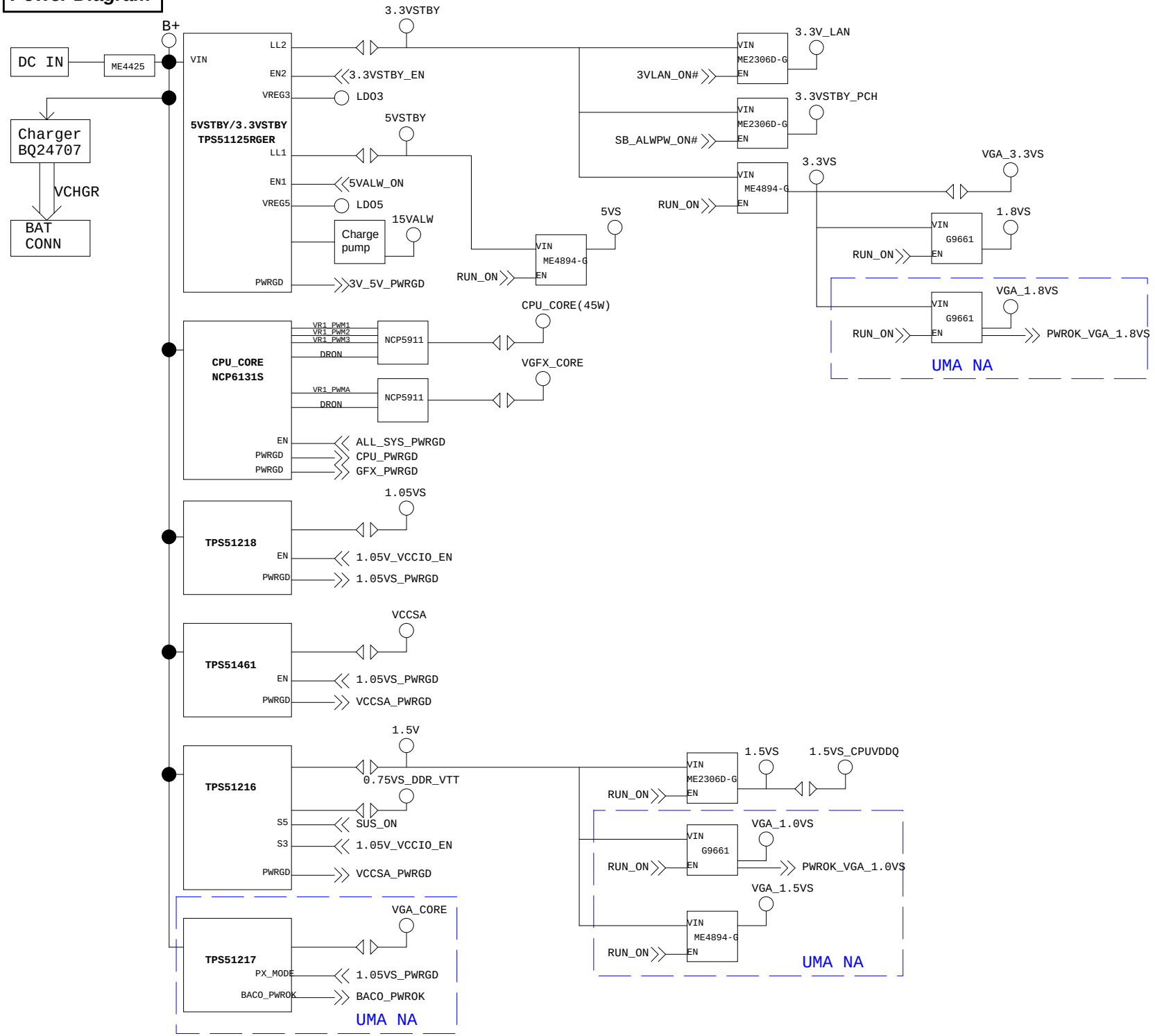
Project Name : H710DI1	Title : PAD_SCREW_ Moat Cap	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 58 of 63	

THERMAL



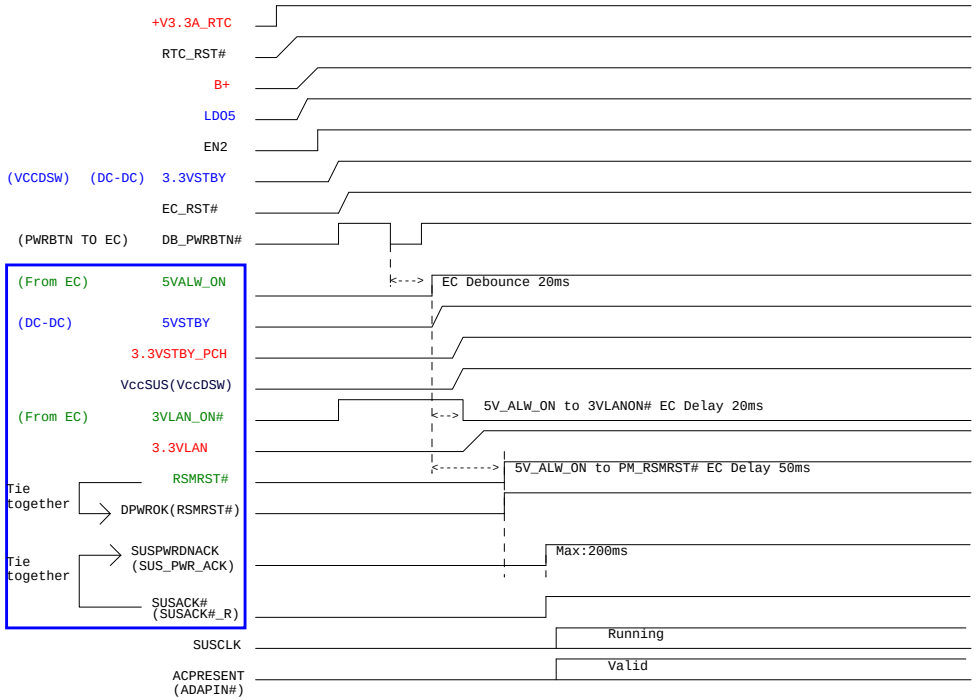
FLEX Computing		
Project Name : H710DI1	Title : Thermal Policy	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 59 of 63	

Power Diagram

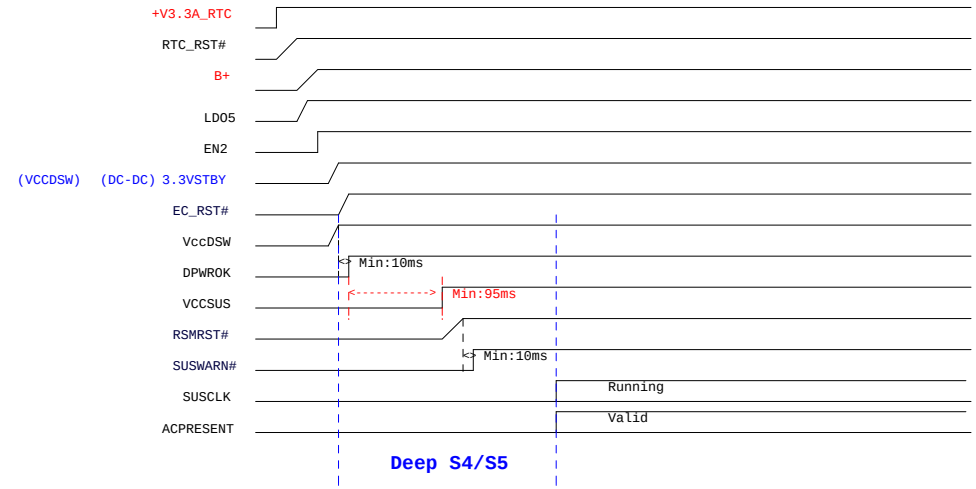


FLEX Computing			
Project Name : H710DI1	Title : Power Diagram		
Size :	Document Number : HPMH-40GAB6600-B130		Rev : B
Date: Monday, November 08, 2010	Sheet : 60 of 63		

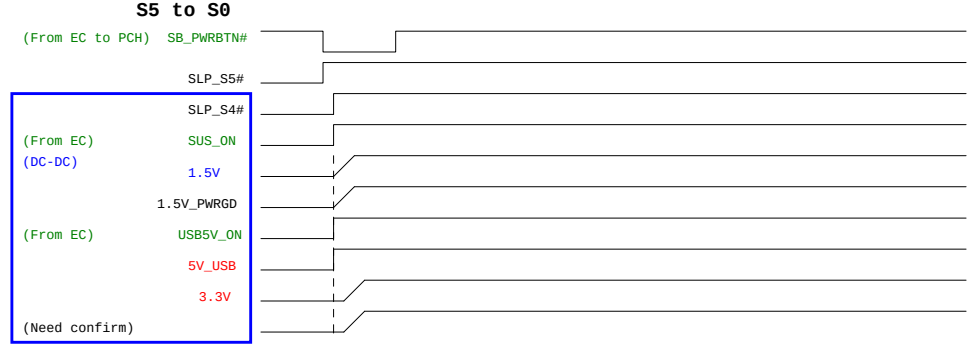
G3 to S0 (without Deep S4/S5)

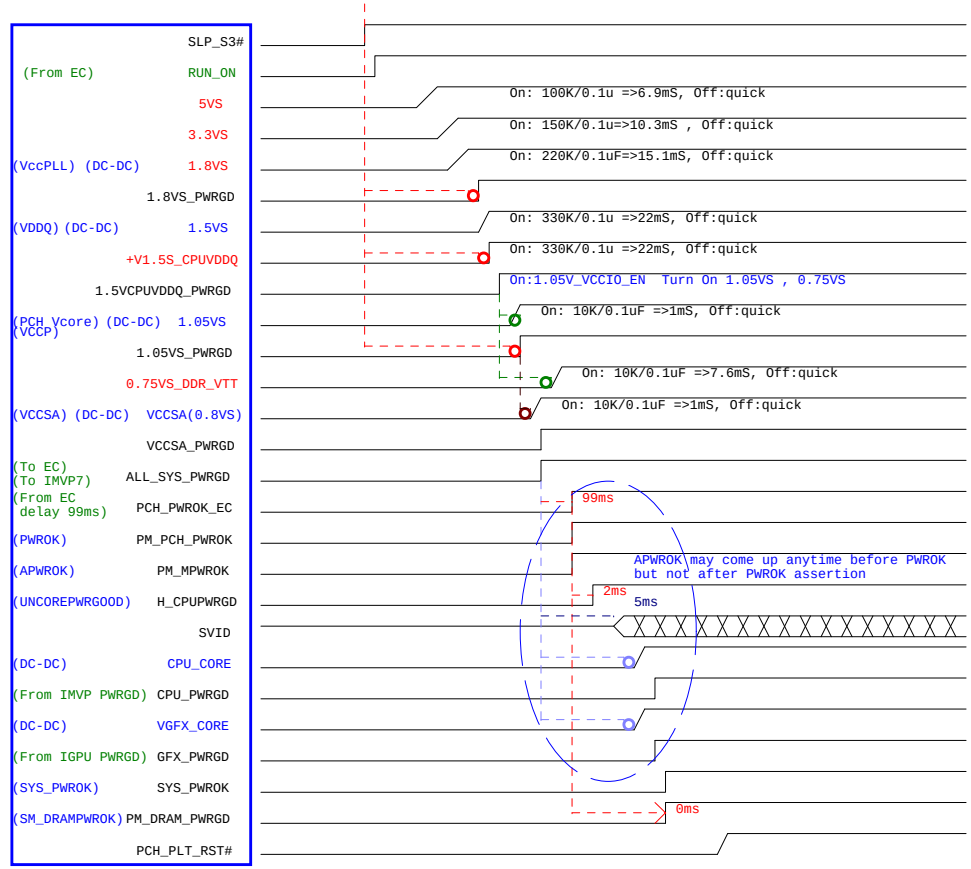


G3 to Sx (support Deep S4/S5) This Platform Without SUPPORT



S5 to S0





Blue: PWM

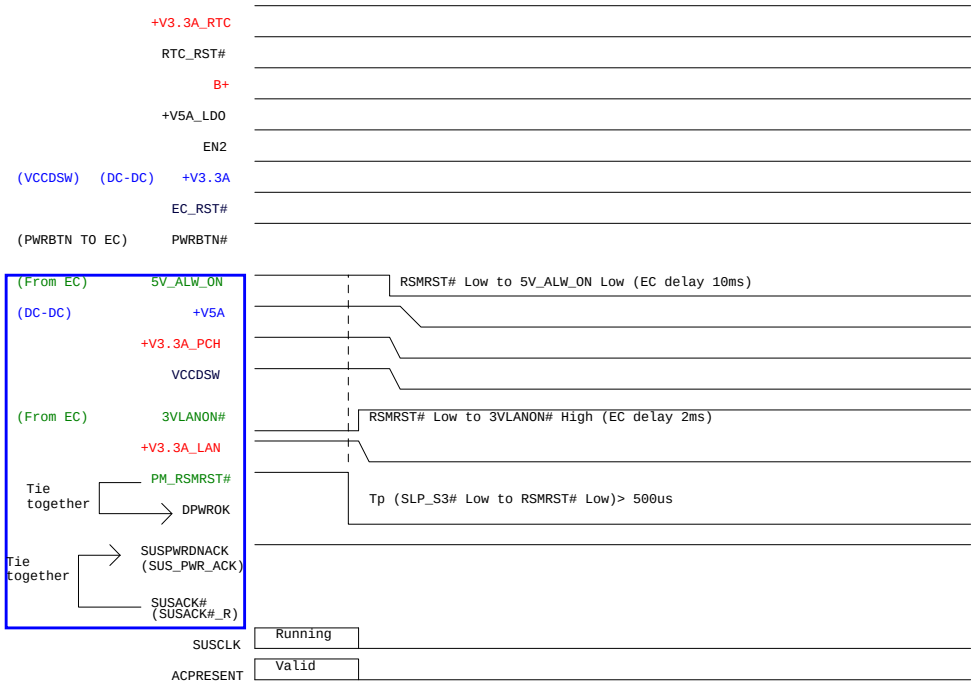
Green: EC

RED: MOSFET or Others

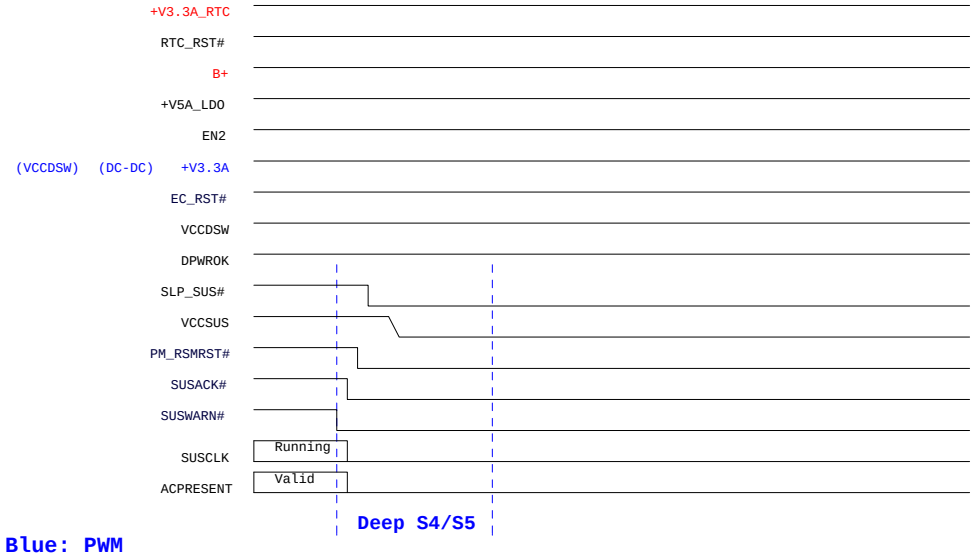
FLEXComputing

Project Name : H710DI1	Title : POWER ON SEQUENCING	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 61 of 63	

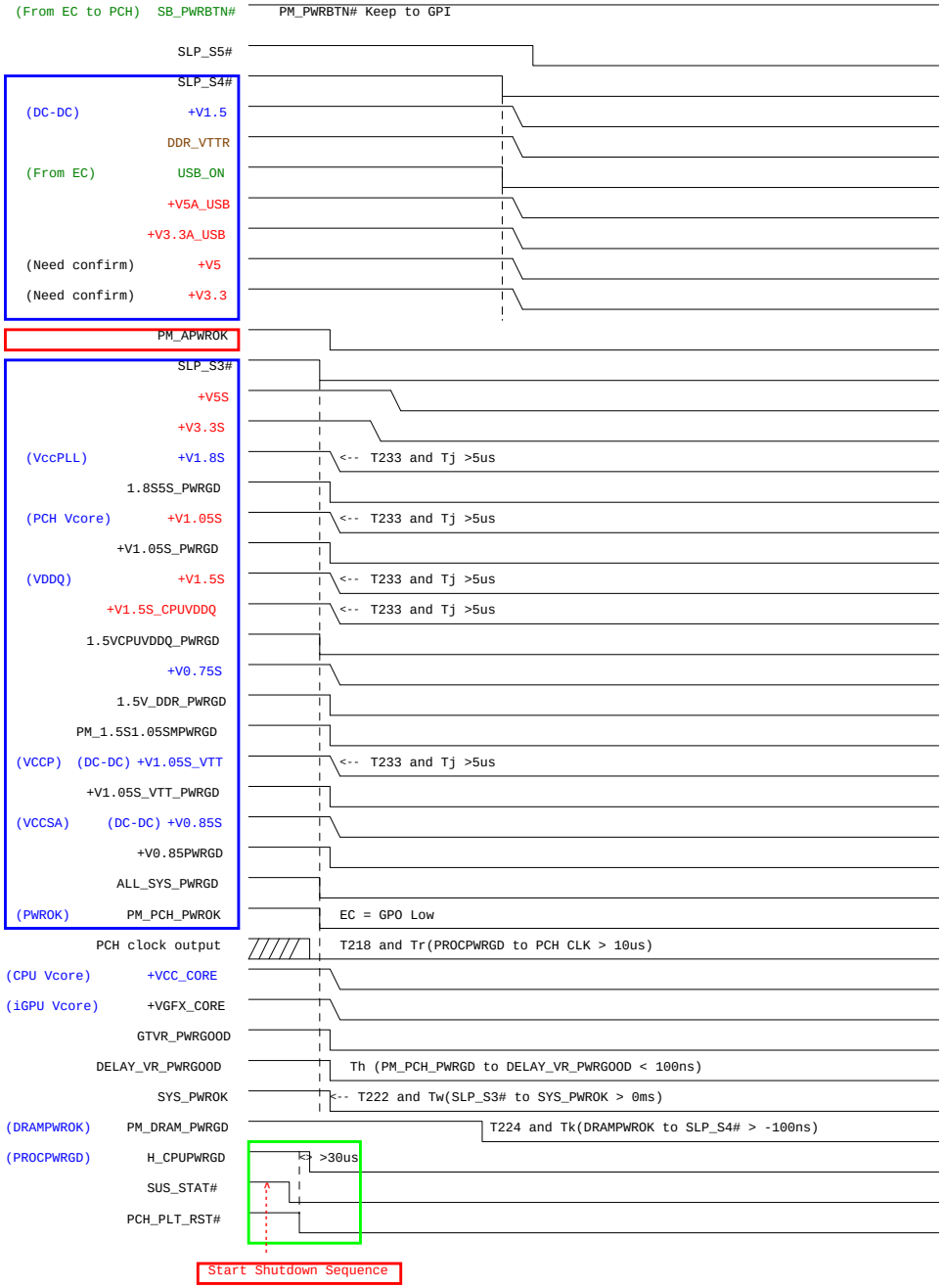
S0 to S5 (WoLAN Disable) (without Deep S4/S5)



S0 to S5 (support Deep S4/S5)



S0 to S4/S5



Blue: PWM

Green: EC

RED: MOSFET or Others

FLEX Computing			
Project Name: H710DI1		Title: POWER OFF SEQUENCING	
Size:	Document Number: HPMH-40GAB6600-B130		Rev: B
Date: Monday, November 08, 2010		Sheet: 62 of 63	

HPMH-40GAB6100-A1A0
RJ6 B 10K(HPMH-30-301036-990G) 010
RJ804 B 10K(HPMH-30-301036-990G) 020
H10&H11 HPMH-75110-0000051G PWA NUT G AB610 020
PC99 HPMH-31-1F1067-900G 010
PC123 HPMH-31-163328-940G 010
PC124 HPMH-31-163328-940G 010
PR822 HPMH-30-178721-990G 020
PC805 HPMH-31-1F1067-900G 020
PR157, PR158, PR159, PR811 料號改爲HPMH-30-249991-990G
CB77 NA
CB78 NA
CN_KBL6 NA
M807 NA
M808 NA
R991 NA
R986 NA
C1006 NA
R1047 改爲HPMH-30-101546-990G RES CHIP 150KOHM J 0402
PR106 改爲HPMH-30-202241-990G RES CHIP 220Kohm F 0402
PC103 改爲上HPMH-31-1M1047-940G
CAP CERA CHIP 10V 100nF K X7R 0402
PR79改爲HPMH-30-202241-990G RES CHIP 220Kohm F 0402
PR148 改爲HPMH-30-301036-990G RES CHIP 10Kohm J 0402
PR839 改爲HPMH-30-301036-990G RES CHIP 10Kohm J 0402
C1090,C1091,C1092,C1093,C1087,C1086,R1065 NA
R1064,C540,C536,R1066,C1088 NA
Add HPMH-B2995007G00001 HDMI COST FOR CASABLANCA AB610

20100830(base on A1A0 modify for SI)
change footprint CAP0402_BGA to CAP0402
change footprint RES0402_BGA to RES0402
change PN HPMH-18-0020000168G to HPMH-18-0020000202G
change Q803 & Q8 frome HPMH-18-003904-900G to
HPMH-18-0000000021G
M814 & PD9 NA
change F801 footprit from POLYSW-SMDC035 to
FUSE-3L4X1W8X1H
Connect PROCHOT to IMVP7

20100831
Del R91
Change BT_DET# frome EC pin 73 to PCH PGIO6
Change BT_PWRON# frome EC pin 20 to PCH PGIO16
Add R1068,R1067,M822
R899 NA

20100901
Change U22 footprint SOIC8-50X286

20100906
change PR106 to 150K
modify new CN_KB6 footprint (CN-FPC-32P-1P0-2H)
modify new CN_CARD6 footprint CN-2IN1CARD-11P-3H85)
modify CN_WOF6 footprint to CN-WTB-2P-1P25-2H03

20100907
change H13,H14,H18,H19,H16,H17,H22,H23
footprint THR276B189_150
Modify CN_RTC801 footprint to CN-WTB-2P-1P25-4H9
Modify CN_WOF6 footprint to CN-WTB-2P-1P25-2H03
Modify CN_SPK7 to CN-WTB-4P-1P25-4H9
Modify R840/R841/R847/R848 2.49K change to 1.96K_F
(PN: HPMH-30-0000000183G)(RES CHIP 1.96Kohm F 0402)
Add R1069

20100910(A)
Del DPA34,R851 NA
Modify USB 3.0 SMI connect to PCH
Page 35 modify Audio Woofer Schematics
Page 28 modify Thermal Schematics
20100910(B)
Del PD9
C868 change to 1u/25V_0603 (PN: HPMH-31-0010000012G)
(CAP CERA 25V 1uF K X5R 0603)

20100911
ADD PC166-PC169 to 1500pF (PC166,PC167 NA)

20100913
modify C111 from 470uF to 330uF
Modify PR849,PR806 footprint to 0603 package
Add PR173(VRHOT# pull high)
PC876 change to 10nF
Delete CB803
Add FL1 (PJP804 open)
PR810 change to 2.2ohm.
Change PECI Pad36 to Pad820

20100915
Modify P56 M20 Description to 140m
Modify FL1 Part number to PN
Modify CN_DUSB6 P18 from 5VSTBY to GND
and footprint from CN-FPC-18P-0P5-2H to CN-FPC-18P-1P0-2H
Modify LVDS CONN footprint CN-LVDS-40P-1H95
to CN-LVDS-40P-0P5-1H4
Modify CN_RTC801 footprint to CN-WTB-2P-1P25-4H9
Modify CN_WOF6 footprint CN-WTB-2P-1P25-2H03
Modify CN_SPK6 footprint CN-WTB-4P-1P25-4H9
Change VMEM_CSA#B0(Pad 36 to Pad 820)
Change PECI (Pad820 to Pad36)
Change PCH(U811)PN to HPMH-10-0010000113G
IC Cougar Point PCH QNDL FCBGA989
modify U810 Pin40,Pin41,Pin43,Pin44
Add U808 Pin2,5,11,14 netname
Modify P36 USB3.0 from TI to NEC
Modify P37 USB3_1.1V to 1.05V_USB

20100916
modify Audio CN_SPK6 and CNSPK7 footprint again

20100917
modify CN_DUSB6 Footprint
Del PR165~PR172,Del PC170~173
Modify ODD Zero Power Schematics
NC_PCH_GPIO49 change to SATA_ODD_PRSNT#
SATA_ODD_PRSNT#(GPIO36) change to NC_PCH_GPI36
Del Pad29 R964 , Add R1110
Add C1119 for SERIRQ,C1120 for LPC_CLK
Modify PR877 to 26.1K ,PR144 to 80.6K
U19 PIN 73: 換成THERM_ALERT#(本來的pin78) ,
原本的 BT_DET# 移除 (Intel change to SB)
U19 Pin78: 換成AC_OFF, 原本的THERM_ALERT#移到Pin73
Add PQ826 and PR879
Add M823 M824 for Touch Pad LED
Add JS845,M825 for USB3.0 SMI
Update M.E. modification of screw holes (H20,H25)

20100923
modify PR160 to 4.7K(HPMH-30-247011-990G)
modify PR163 to 39K(HPMH-30-139021-990G)
modify PL810 to 0.47uH (HPMH-32-4000000227G)
PC113 change to MOUNTED
PR108 change to 1 ohm and mounted.(HPMH-30-200106-950G)
PC119 change to 470PF/50V and mounted (HPMH-31-104717-940G)
PR851 change to MOUNTED
Add PQ13,PQ20,C1130,C1131,PC77,CB84,CB842~CB846
Del PJP8,JS32,D8,M28,R301
C860, C48 change from N.A to 33pf
EC817, EC818 change from N.A to mount (220PF)
CB60, CB61 change from N.A to mount (150pf)
原BACO_PWROK(GPIO2)改爲NC_PCH_GPI2
DGPU_PWROK (GPIO17) 改爲BACO_PWROK
NC_PCH_GPI50 (GPIO50) 改爲dGPU_HOLD_RST#
NC_PCH_GPI54 (GPIO54) 改爲DGPU_PWR_EN#
VGA_1.8VS, VGA_1.0VS, VGA_3.3VS,VGA_1.5VS,VGA_CORE
的enable改爲DGPU_PWR_EN
R879 ,R880 改爲L879,L880
EC810, EC811, EC812, EC813 change from N.A to 220pf
ED802, ED801, ED803, ED804 change from N.A to mount
(Flex P/N: HPMH-21-0200000012G, Footprint: CAP0603)
EC804, EC805, EC806, EC807 change from N.A to 220pf
PC870, PC871 change from 47pf to N.A
PR805, PR124, PR126, PR127 change from N.A to short pad
PR805, PR124, PR126, PR127 change from N.A to short pad
PC136, PC137, PC140, PC810 change from N.A to 1000pf
PR810, PR153, PR154, PR151 change from 0ohm to 2.2ohm
Add C1132 for KB_RST#
PR847 change from N.A to short pad
PC857 change from N.A to 1000pf
PR107 change from N.A to short pad
PC104 change from N.A to 1000pf
(C49, C509, C532, PC835, PC122, PC106, PC57,
PC48, PC878, PC811, PC801, PC802, PC813
C256, C60, C84, C337, C473, C236, C533,
C541, C539, C108, C506, C163 change from N.A to 0.1uf)
Add C1133~C1145
Add EM1~EM5
JS14/JS13/JS35/JS830 footprint change to RES0603-SHORT05
change C1037 to 0603 25V
Modify CN_DUSB6
Change R1108 to 10K
Change C234,C235,C942,C944 to 0.1uF

20100920
C158 change to NA for 1.05VS leakage
Modify C141 & C133 to 15PF for RTC
Add C1121 for FPVCC soft start
Add Y9 PN

20100921
Modify M14 to P MOS,R924 change to 100K
Del M804, Add R1111,C1122
Change USB3.0 POWER netname from 3.3V to 3.3V_USB
Add 3.3V SUS Power, Add R1112, R1113, C1123 , M826 M827
Add C1124,C1125 for 5VSTBY to GND (for noise)
Add C1127,C1128 for 1.05VS to GND (for noise)
Change C487,C407 to CPU Core for POWER
Add C1126 for 1.5VS_CPUVDDQ
Add C1129 for PROCHOT#

20100924
USB3.0 CONN (CN_US3S802,CN_US3S801)
footprint change to CN-USB3_0-9DIP-7H67-RVS
JS14/JS13/JS35/JS830 footprint change to RES0603-SHORT10
H8 THR213B315_110
H9 THR268B276_110
H20 THR236B276_110
Add R1114
Change U19(KBC)PN to HPMH-10-0090000025G
Del L823,L824,L822 for DFX
C193改爲22nF(HPMH-31-142237-950G
CAP CERA CHIP 25V 22nF K X7R 0603)
Y8改料號爲HPMH-35-0010000106G
X'TAL 32.768KHz QTFM28-32768K125P10R
Del PJP815,L9,R155
Add PC879
Add RJ806(for platform ID)
Add RJ807(for PWA rev)
Add U20 (USB3.0) PN
PR144 change to 0402 size
R165 from NA to MOUNTED
Change R909 to 1K

20100925
Modify USB3.0 power from 3.3V to 3.3_USB
Add U822,C1129 PN
CN_KBL6 from Mounted to NA
R853 change from 22 ohm to Bead 600ohm
(Flex P/N: HPMH-32-2000000092G)
C859 change from N.A to 22pf
C878, C879 change from 10pf to 6.8pf
(Flex P/N: HPMH-31-0000000031G)
Add C1146~C1149 (modify below)
ADD 1pcs 0.1uf capacitor between B+ and GND
ADD 1pcs 4.7uf capacitor between B+ and GND
ADD 1pcs 0.1uf capacitor between 3.3VSTBY and GND
ADD 2200pf capacitor between PQ10 pin4 and GND
PC119 change from N.A to 1000pf
PR108 change from N.A to short pad
PC113 change from N.A to 1000pf
PR98 change from 0 ohm to 2.2 ohm
PC47, PC72 change from N.A to 1000pf
PR93, PR56 change from 2.2 ohm to short pad
PC90,PC51 from NA to MOUNTED
Change R1109 pull hight from 3.3V_USB to 3.3VSTBY_PCH
Add JS846

20100926
Modify USB3.0 net USB_USB30PORT1_N
and USB_USB30PORT1_P (SWAP)
Modify USB3.0 net USB_USB30PORT0_N
and USB_USB30PORT0_P (SWAP)
Add R1115 for Intel recommend
Add L9 C1150

20100927
Add C1151
R851 from NA to MOUNTED
modify ME4,ME5 footprint same as ME1
Add D812 prevent leakage from EC to VGA

20100928
change C868 PN to 1uF/25V HPMH-31-0010000012G
PC836 pin 2 change to DGND
C1151 pin2 改爲UGPU_PWR_SRC
Del M17 ,USB3_PWR_EN# connect to RJ9 pin1
Swap USB_TOUP_N ,USB_TOUP_P
Swap USB_TOUP_N_R,USB_TOUP_P_R
Modify VGA Power from 15W to 35W
Modify U819 Add pin VFB and GFB and PWRPLAY_VID2

20100929
Change C1132 to 18p
PR856=1K_F(HPMH-30-210011-990G)(copy PR116)
PR121=24.9K_F(HPMH-30-124921-990G)(copy old PR856)
PC865=2200PF(HPMH-31-102227-940G)(copy C1149)
PC108=220PF(HPMH-31-102216-940G)(copy EC806)
PC127=15PF(HPMH-31-301506-940G)(copy C133)
PR123=4.02K_F(HPMH-30-240211-990G)
PC123=2200PF(HPMH-31-102227-940G)(copy C1149)
PR871=PR875=PR869=140K(HPMH-30-0000000104G)
PR144 change to 69.8K(HPMH-30-269821-990G)
PC124 change to 2200pF(HPMH-31-102227-940G)(copy C1149)
PC113, PC119 change to 470PF/50V
and mounted (HPMH-31-104717-940G)
PR98 change from 2.2 ohm to 0 ohm
PR153, PR154, PR151 change to 0_0603 (HPMH-30-000006-950G)
PC857 change to NA
L879, L880 change to 33ohm
C878, C879 change to 10pf
modify PU7 pin M5
FL1 NA
update P57 AGND to DGND

20100930
modify PC801,PC811 pin2 to 5VSTBY
modify HDMI HP-DET schematics

20101003
modify PC801,PC811 to 25V 1uF K X5R 0603
modify C1132 to 50V 1000pF J X7R 0402
modify PR16, PR17, PR18,PR24 to 3.01KOHM F 0402
modify PC13, PC14, PC12, PC19 to 50V 220pF 0402
modify PR42, PR41 to 110Kohm F 0402
modify PL803,PL801 to 1uH M PCMC104T-1R0MN
modify PR49, PR52 to 0ohm J 0603

20101004A
modify PQ826 Libraries

20101004B
modify PR10 NA, mounted PR9
PR34 NA
PR8 changes to mount 90.9K (HPMH-30-0000000130G)
PR25 change to 3.01K (HPMH-30-230111-990G)

20101007
modify Subsystem ID
R272 R273 modify to 100ohm

20101008
Modify C408 C487 from NA to Mounted
Change R1070 PN to 10 ohm 1206

20101013
HPMH-40GAB6100-B1A0 FAI build for temporary solution:
Original PN for HPMH-40GAB6100-B1A0 SKU1 build
1. M/B:38-0020000031G
CONN VGA 15P DS15146BAC067 DIP
HPMH-38-0020000029G
CONN VGA 15P 2DS1557-000111 DIP
2. M/B:38-00F0000019G
CONN HDMI 19P HD19E46BA3062 DIP
HPMH-38-00F0000017G
CONN HDMI 19P 2HE1565-000111 DIP
3. USB/B:31-0800000003G
CAP OS-CON 6.3V M 220uF 6SVPE220MX
HPMH-31-0730000029G
CAP SP 6.3V 220uF M MP6VLPS220MC4R2

↑ 10/19 REV.B100

change to Rev.C
1.modify CN_LVDS6 pin swap
2.Add R1116 for HP LOGO
3.Modify PQ826 footprint
4.PR15 Pin 2 changes from 3.3VS to 5VS.
5.PR34 mounted and change to 90.9K (HPMH-30-0000000130G) for voltage slew.
6.PR8 changes NA.
7.Pin 1 of PR10 changes from 3.3VS to 5VS.
8.PR49 and PR52 change from 2.2 ohm to 0 ohm (HPMH-30-000006-950G)
9.PC17 and PC16 change from 1uF to 0.22uF (HPMH-31-0020000064G)
10.PQ807 and PQ805 change from FDSM7692 to NTMFS4926N (HPMH-18-0020000247G)
11.PQ806 and PQ801 change from FDM0308S to NTMFS4935N (HPMH-18-0020000246G)
12.PL803 and PL801 change from 0.45uH to 0.56uH (HPMH-32-800562-020G)
13.PR6 changes from 20K to 64.9K (HPMH-30-164921-990G). (not 54.9K)

20101022
1.R277,R268 change from 10K to 1K for PX_EN_VGA_CORE rise time
2.swap LB17(1,4 pin對調;2,3 pin對調)
3.SW6 NA(sw6 for debug use)
Del CE6 , CE801,Add CE1 for USB3.0 cost

20101025
1.modify U25 Main source to HPMH-12-007408-620G

20101027
1.modify PCB PN to HPMH-41-AB6200-C00G
2.Add HDMI Label
3.Add Intel CPU PN table in P2
4.Add Intel PCH PN table in P12
5.Add R1117 100ohm for HP LOGO(eDP Conn)
Page 37
6.Update the net name of PU801 pin 3 as 1.5V_G9661.
7.Update the net name of PU801 pin 4 as 5V_G9661
Page 40
8.PR100 change to 0805 size (HPMH-30-201006-900G)
9.PC80 change to 0603 size (HPMH-31-0010000012G)
Page 41
10.PR69 change to 34.8K_F (HPMH-30-234821-990G)
11.PR68 change to 22K_F(HPMH-30-222021-990G)
Page 43
12.PR127, PR126, PR124, PR805 change to 1 ohm 5% (HPMH-30-200106-950G)
Page 44
13.update switching frequency to 430KHz
14.update OCP to 15.54A
Page 45
15.update switching frequency to 700KHz
Page 46
16.update the value of PL812 to PCMC104T-1R0MN
17.update OCP to 19A
Page 57 (please replace whole page),
18.update VID table for 35WDGPU(x2) and 15WDGPU (x1)
19.PR7 change to 15K_F and to be NA (HPMH-30-0000000078G)
20.PR10 change to mounted.
21.PR9 change to NA.
22.Pin1 of PR30 change to 5VS.
23.PC9 change to NA.
24.Pin2 of PR45 change to GND and to be NA
25.PR23 change to 30K_F and to be NA (HPMH-30-130021-990G)
26.modify R1070 footprint 1206 to 0805
27.modify L13 PN and footprint to 0603
28.modify USB3.0 power 3.3V_USB and 3.3V_USB_VDDA

20101028
1.Add pad29 for BIOS test
2.LB17 SWAP
3.change M23 from ME2N7002E to ME2N7002W
and footprint from SOT-23A to UMT-23
4.change C111 PN to HPMH-31-6B337Y-130G
5.D805 pin 3 pn2 swap for layout trace

20101029
1.modify U822 footprint
2.modify Page1 Block
3.modify PR34 as 150K
RES CHIP 150Kohm F 0402 HPMH-30-115031-990G

20101030
1.modify PC90 to CB90
2.modify PC835 to CB848
3.modify PC122 to CB122
4.modify PC106 to CB106
5.modify PC57 to CB5
6.modify PC48 to CB48
7.modify PC878 to CB878
8.modify PC802 to CB803
9.modify PC813 to CB847
10.modify PC51 to CB49
11.modify PC801 to CB4
12.modify PC811 to CB3
13.modify RJ6 from B to A for PV PWA.Rev
14.Add RJ808 and RJ809
15.Del R68 & R59

20101101
1.modify D805 Pin2 and Pin3
2.Del C1103,C1106,C1107
3.modify C1109 to 0.1uF/10V
4.PJP822 change footprint to JUMPER3P5-SHORT
5.Add two PC880,PC881 (68uF/25V) at B+
6.Delete PJP6

20101102
1.Add R1118 for GPU_TRIP#
2.R852 NA
3.PR70 change to 54.9K
4.R1052,R1050,R1051,C1081,Q803,M820 NA
5.CB67, CB62, CB57 change from 22pf to 33pf =>EMI
6.CB58, CB64, CB68 change from 22pf to 10pf =>EMI
7.Add EC820,EC821,EC822,EC823 =>EMI
(PWR_LED and GND,HDD_ACT_LED# and GND
HDD_PARK_LED# and GND)
8.CB834,CB833,CB832,CB831,CB830,CB825,CB824,
CB823,CB821 change from N.A to 100pf
9.C878 change from 10pf to 6.8pf
10.C879 change from 10pf to 4.7pf
11.Add EC824 between CR-SD_3V3 and GND
12.EC801, EC13, EC17, EC11 change from N.A to 0.1uf
13.EC810, EC811, EC813, EC812 change from 220pf to N.A
14.ER801,ER802,ER803,ER804 change from
shout pad to Bead 220ohm (HPMH-32-2000000106G)
15.modify ER801,ER802,ER803,ER804 footprint
from shout pad to L0805
16.Add CB849,CB850,CB851,CB852,CB853
17.modify CN_PBTN6 from 6 pin to 8 pin
18.modify LID to PWRBTN BOARD
19.Add 0.1uf*2pcs to net VCHGR CB854,CB855
20.Add 0.1uf capacitor between CHG_LED# and GND
CB856
21.modify RJ9 to B

20101103
1.M825 from mounted to NA
2.PR801 form 261K to 39K ohm for power up before USB3_PONRST#
3.Add metal spring EM2
4.L801, EL8 change from Bead 120ohm to Resistor 300ohm
5.Add ED810 between net SENSE A and GND
6.ED809, ED14 NA but change footprint and PN
(HPMH-21-0200000012G, Footprint: CAP0603)
7.ED13, ED11 change from N.A to mount,change footprint,PN
(HPMH-21-0200000012G, Footprint: CAP0603)
8.ADD ESD protection component between net SENSE_A and GND
(HPMH-21-0200000012G, Footprint: CAP0603)
9.Add R1119 for PX_EN
10.modify net PROCHOT_EC# to PROCHOT_EC
11.modify EC pin73 from THERM_ALERT# to DGPU_PWR_EN
12.Add JS43.JS44,JS45 between 24707AGND and GND
13.CB69, CB63, CB59 change from 22pf to 33pf
14.Add D107
15.Add M828 R1120 for VGA_3.3VS
16 net N22020819 change net name to DGPU_EN#

20101104A
1.Add PR883,PR884,PC882
2.modify PC880,PC881 footprint
3.Del PC28
4.Add VGA_CORE TDC/OCP table

20101104B
1.CB52,CB53,CB65,CB66 just change
component dimensions to ED52,ED53,ED65,ED66
2.Change ED52,ED53,ED65,ED66 PN to
HPMH-21-0200000012G, Footprint: CAP0603
3.Delete CB42,CB43
4.ED805,ED806,ED807,ED808 change
PN HPMH-21-0200000012G, Footprint: CAP0603
5.ED801 pin2 change from GND to AGND

20101105A
1.Change ED52,ED53,ED65,ED66 PN to
HPMH-21-0200000009G, Footprint: CAP0402
2.ED805,ED806,ED807,ED808 change
PN HPMH-21-0200000012G, Footprint: CAP402
3.ED801 pin2 change from AGND to GND
4.ED810,ED15 change from GND to AGND
5.Add CB879 between 5VSTBY and GND
6.Add D816.R1121,JS834,M829
7.PR30,PR802 change pin1 to VGA_3.3VS

20101105B
1.PR820 change pin1 to VGA_3.3VS

FLEX Computing

Project Name : H710DI1	Title : Modify History	
Size :	Document Number : HPMH-40GAB6600-B130	Rev : B
Date: Monday, November 08, 2010	Sheet : 63 of 63	