1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

D8 MLB ULTIMATE

LAST_MODIFIED=Mon Aug 27 13:33:38 2012

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
8	0001607319	ENGINEERING RELEASED	2012-08-28

DRAWING

TITLE=K72
ABBREV=DRAWING
LAST_MODIFIED=Mon Aug 27 13:33:38 2012

DRAWING TITLE: SCH,D8,MLB ULTIMATE

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D
REVISION: 8.0.0
BRANCH: prefsb
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System Block diagram can be found on Kismet

PATH: KISMET > K70/72 > BLOCK DIAGRAMS > K72 BLOCK DIAGRAM

PAGE TITLE
System Block Diagram

Apple Inc.

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Supply Module
AC/DC
Reg G3H 12V
PP12V_ACDC
VD2R
ID2R
PD2R
PP12V_G3H
PP12V_S0_BLC
PP12V_S0
PP12V_S5
U7801
Regulator
Vin
en G3H
Reg G3H 3V42
PP3V42_G3H
SMC, RTC, MojoMux
U7600
Regulator
Vin
en S5
LDO S5 5V
PP5V_S5
PCH, PwrCtl
Reg S5 3.3V
PP3V3_S5
Bootrom, PCH, SMC, XDP,
SD Card, USB Mux, VRD, PwrCtl
PP3V3_S4
ALS, CAM, BT
USB Hub, SMC, TBT I/O
V3V3
IW0R
PW0R
PP3V3_S4_AP
WIFI
PP3V3_S4_ENET
Ethernet
PP3V3_S0
Audio, LCD TCON, SnsCtl, VRD, PCH
SD Card, DP Mux, DP X-bar
V3V3
IW1R
PH1R
PP3V3_S0_SSD
SSD
PP3V3_TBTLC
TBT Router
en S4
Reg S4 5V
PP5V_S4
CAM, USB Ports, VRegCtl
VH05
IH05
PH05
PP5V_S0_HDD
HDD (5V)
PP5V_S0
Audio, PCH
VRegCtl, SnsCtl
U7700
Regulator
Vin
en S3
Reg S3 VDDQ
VM0R
IM0R
PM0R
PPVDDQ_S3_DDR
DIMM (1V5)
PP1V5_S0
Audio
VC0M
IC0M
PC0M
PP1V5_S0_CPU_MEM
CPU (Mem)
LDO S3 VTT
PPDDRVTT_S3
DIMM VREF Margining CA
en S0
LDO S0 VTT
PPDDRVTT_S0
DIMM (VTT)
PPHV_SW_TBTAPWR
TBT Port A
PPHV_SW_TBTBPWR
TBT Port B
U7100
Regulator
Vin
en S0
Reg S0 Core
Reg S0 AXG
VC0C
IC0C
PC0C
PPVCORE_S0_CPU
CPU (Core)
VC0G
IC0G
PC0G
PPVAXG_S0
CPU (AXG)
U7400
Regulator
Vin
en S0
Reg S0 VccIO
VD2R
IC0I
PC0I
PP1V05_S0_CPU
CPU (VccIO)
U7500
Regulator
Vin
en S0
Reg S0 VccSA
VD2R
IC0S
PC0S
PPVCCSA_S0
CPU
UB400
Regulator
Vin
en S0
Reg S0 GPU
VG0C
IG0C
PG0C
PPVCORE_S0_GPU
GPU (Core)
UB750
Regulator
Vin
en S0
Reg S0 GPU
FBVDDQ
VD2R
IG0F
PG0F
PPFBVDDQ_S0_GPU
GPU (FB)
UB700
Regulator
Vin
en S0
Reg S0 1V05
VD2R
IR1R
PR1R
P1V05_S0
GPU (IOVDD, PLLVDD)
VN1R
IN1R
PN1R
P1V05_S0_PCH
PCH (VCC, VccIO)
PP1V05_TBTCIO
TBT Router
PP1V05_TBTLC
TBT Router
Loads
Fan
LCD
GPU
Speaker amps
TBT IO
VD2R
IH02
PH02
PP12V_S0_HDD
HDD (12V)
U7750
Regulator
Vin
en S0
Reg S0 1.8V
PP5V_S0
PP1V8_S0_REG
CPU PLL

High-side Component Total Power Keys

PCTR = 1.176 * (PC0C + PC0G + PC0M) + PC0S + PC0I
PGTR = 1.176 * (PG0C + PG0F) + 5.7 (GK104/GK107_BLENDED_CONSTANT)
PH0R = PH02 + PH05

SYNC_MASTER=D8_MLB
SYNC_DATE=08/27/2012
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Power Block Diagram
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3662	PCBA,MLB,ULTIMATE,3.4G,GTX,SAM,2GB,D8	D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GTX,FB:2G_SAMSUNG,EEEE:F0V5
639-3950	PCBA,MLB,ULTIMATE,3.2G,GTX,SAM,2GB,D8	D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GTX,FB:2G_SAMSUNG,EEEE:F49R
639-3560	PCBA,MLB,ULTIMATE,3.4G,GT,SAM,1GB,D8	D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GT,FB:1G_SAMSUNG,EEEE:DYW3
639-3949	PCBA,MLB,ULTIMATE,3.2G,GT,SAM,1GB,D8	D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GT,FB:1G_SAMSUNG,EEEE:F49P
639-4087	PCBA,MLB,ULTIMATE,3.4G,GTX,HYN,2GB,D8	D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GTX,FB:2G_HYNIX,EEEE:F64W
639-4091	PCBA,MLB,ULTIMATE,3.2G,GTX,HYN,2GB,D8	D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GTX,FB:2G_HYNIX,EEEE:F652
639-4086	PCBA,MLB,ULTIMATE,3.4G,GT,HYN,1GB,D8	D8_COMMON,D8,CPU:4C_3P4GHZ,GPU:104GT,FB:1G_HYNIX,EEEE:F64V
639-4090	PCBA,MLB,ULTIMATE,3.2G,GT,HYN,1GB,D8	D8_COMMON,D8,CPU:4C_3P2GHZ,GPU:104GT,FB:1G_HYNIX,EEEE:F651
085-4435	PCBA,MLB,DEV,D8.ULTIMATE	DEVELOPMENT,D8_DEVEL

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_DYW3	CRITICAL	EEEE:DYW3
825-7896	1	LABEL,MLB,2D	EEEE_F0V5	CRITICAL	EEEE:F0V5
825-7896	1	LABEL,MLB,2D	EEEE_F49P	CRITICAL	EEEE:F49P
825-7896	1	LABEL,MLB,2D	EEEE_F49R	CRITICAL	EEEE:F49R
825-7896	1	LABEL,MLB,2D	EEEE_F4MW	CRITICAL	EEEE:F4MW
825-7896	1	LABEL,MLB,2D	EEEE_F4TY	CRITICAL	EEEE:F4TY
825-7896	1	LABEL,MLB,2D	EEEE_F64W	CRITICAL	EEEE:F64W
825-7896	1	LABEL,MLB,2D	EEEE_F652	CRITICAL	EEEE:F652
825-7896	1	LABEL,MLB,2D	EEEE_F64V	CRITICAL	EEEE:F64V
825-7896	1	LABEL,MLB,2D	EEEE_F651	CRITICAL	EEEE:F651

BOM Groups

BOM GROUP	BOM OPTIONS
D8_COMMON	COMMON,ALTERNATE,D8_COMMON1,D8_PROGPARTS,D8_PRODUCTION
D8_COMMON1	XDP,RSMRST:GATE,SPEAKERID,VREF:CPU,TBTHV:P12V
D8_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG,BLCMCU:PROG
D8_DEVEL	XDP_CONN,LPCPLUS,VREFMRGN:EXT,DEVEL_AUDIO,TEMPSNSDEV
D8_PRODUCTION	VREFMRGN:N,PRODUCTION

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4356	1	IVB,SR0T8,PRQ,N1,3.2,77W,4+1,1.1,6M,LGA	CPU	CRITICAL	CPU:4C_3P2GHZ
337S4247	1	IVB,SR0PK,PRQ,E1,3.4,77W,4+2,1.15,8M,LG	CPU	CRITICAL	CPU:4C_3P4GHZ

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4277	1	IC,PANTHER POINT,C1,SLJC7,PRQ,BDB2Z77	U1800	CRITICAL	
338S1113	1	IC,TBT,CR-4C,B1,PRQ,288 FCBGA,12X12MM	U3600	CRITICAL	
343S0616	1	IC,BCM57766A1,ENET&SD,8X8	U3900	CRITICAL	
337S4333	1	IC, GPU, NV GK104 7-4-PS-A2	UA000	CRITICAL	GPU:104GT
337S4333	1	IC, GPU, NV GK104 7-4-PS-A2	UA000	CRITICAL	GPU:104GT2
337S4332	1	IC, GPU, NV GK104 8-4-PS-A2,	UA000	CRITICAL	GPU:104GTX

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
341S3672	1	IC,EEPROM,CR,V14.1 (B1),D8	U3690	CRITICAL	TBTROM:PROG	
335S0865	1	IC,EEPROM,SERIAL,8KB,MLP8	U3690	CRITICAL	TBTROM:BLANK	
341S3673	1	IC,PROGRMD,EFI ROM,V00FC,D7/D8	U5110	CRITICAL	BOOTROM:PROG	ALTERNATE:335S0812
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5110	CRITICAL	BOOTROM:BLANK	
341S3394	1	IC,PROGRMD,SMC,A3,V2.2A32,D8	U4900	CRITICAL	SMC:PROG	
338S1098	1	IC,SMC,LX4FS1AH5BBCIGA3	U4900	CRITICAL	SMC:BLANK	
341S3675	1	IC,CAMERA FLASH,V7228,D7/D8	U4202	CRITICAL	CAMROM:PROG	
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK	
341S3645	1	IC,ENET 1MBIT, SPI,ROM, V1.13 D8	U3990	CRITICAL	CIVROM:PROG	ALTERNATE:335S0854
335S0862	1	IC,SERIAL FLASH,2MBIT, 2.7V, REF F	U3990	CRITICAL	CIVROM:BLANK	
341S3674	1	IC,BLC,MCU, PRPOGRAMMED, V0204, D8	U9700	CRITICAL	BLCMCU:PROG	
337S3978	1	IC,BLC MCU LPC2132FBD64/01, LQFP64	U9700	CRITICAL	BLCMCU:BLANK	

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0073	1	SOCKET.MOLEX,LGA1155,CPU-LF	U1000	CRITICAL	

CPU SOCKET ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
511S0071	511S0073		ALL	TYCO SOCKET
511S0072	511S0073		ALL	FOXCONN SOCKET

D8 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9505	1	SCH,MLB,D8,ULTIMATE	SCH1	CRITICAL	D8
820-3299	1	PCBF,MLB,D8,ULTIMATE	PCB1	CRITICAL	D8

D8 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB diodes
157S0084	157S0058		ALL	Enet Magnetics
341S3644	341S3645		U3990	CIVROM
376S0975	376S1081		ALL	P/NCH DUAL FET
128S0365	128S0368		ALL	150UF CAPS BLK
138S0803	138S0804		ALL	2.2UF CAPS SOFT
102S0880	102S0879		ALL	0.010 OHM,1%,1206

VRAM Module Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0619	4	IC,SGRAM,GDDR5,32MX32,1.5GHZ,G-DIE,HF	UA300,UA350,UA400,UA450	CRITICAL	FB:1G_SAMSUNG
333S0619	4	IC,SGRAM,GDDR5,32MX32,1.5GHZ,G-DIE,HF	UA500,UA550,UA600,UA650	CRITICAL	FB:1G_SAMSUNG
333S0620	4	IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,B-DIE	UA300,UA350,UA400,UA450	CRITICAL	FB:1G_HYNIX
333S0620	4	IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,B-DIE	UA500,UA550,UA600,UA650	CRITICAL	FB:1G_HYNIX
333S0631	4	IC,SGRAM,GDDR5,64MX32,D-DIE	UA300,UA350,UA400,UA450	CRITICAL	FB:2G_SAMSUNG
333S0631	4	IC,SGRAM,GDDR5,64MX32,D-DIE	UA500,UA550,UA600,UA650	CRITICAL	FB:2G_SAMSUNG
333S0630	4	IC,GDDR5,64MX32,A-DIE	UA300,UA350,UA400,UA450	CRITICAL	FB:2G_HYNIX
333S0630	4	IC,GDDR5,64MX32,A-DIE	UA500,UA550,UA600,UA650	CRITICAL	FB:2G_HYNIX

SYNC_MASTER=D8_MLB_ULTIMATE SYNC_DATE=06/15/2012

PAGE TITLE

BOM Configuration

Apple Inc.

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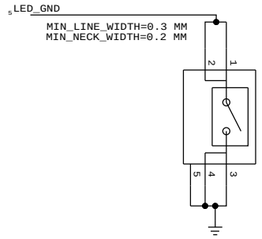
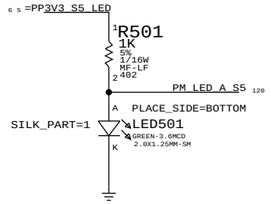
LED GND ISOLATION SWITCH

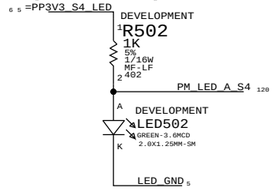


APN: 705S0137

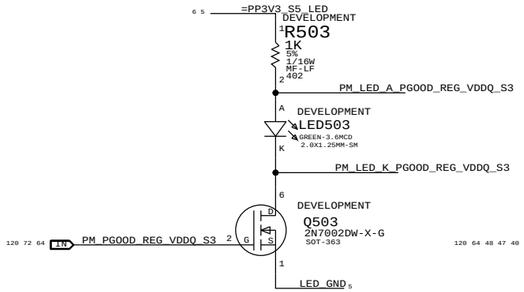
S5 LED



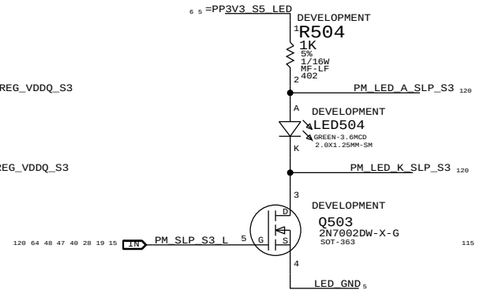
S4 (SLEEP) LED



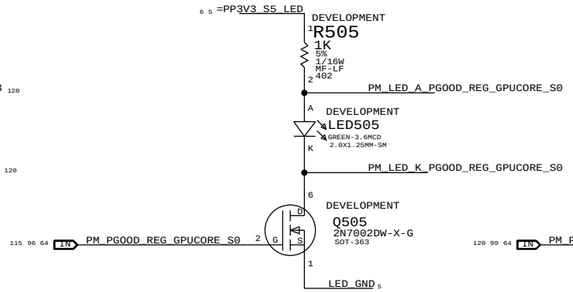
MEM 1V5_S3 LED



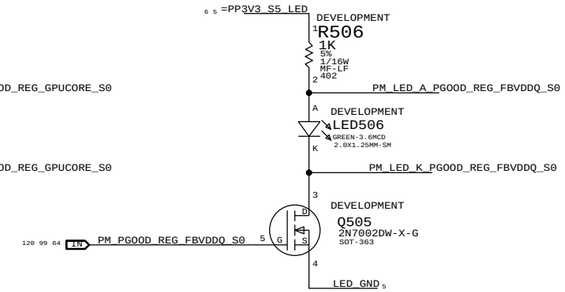
SLP_S3 LED



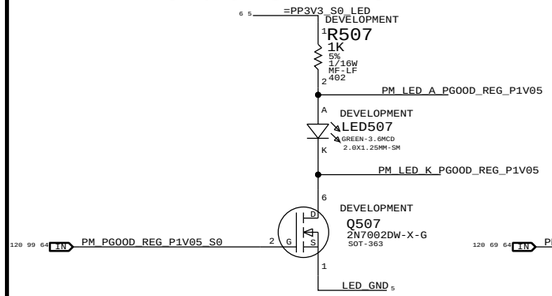
GPU VCORE LED



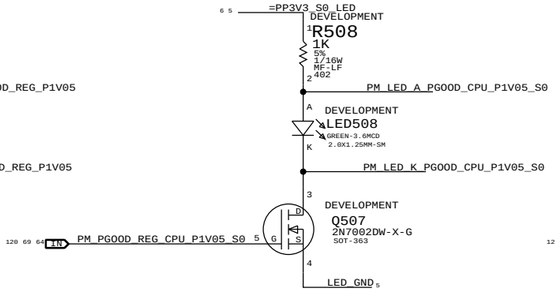
GPU FBVDD LED



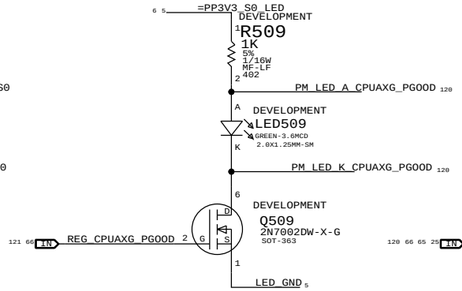
PCH/GPU 1V05 LED



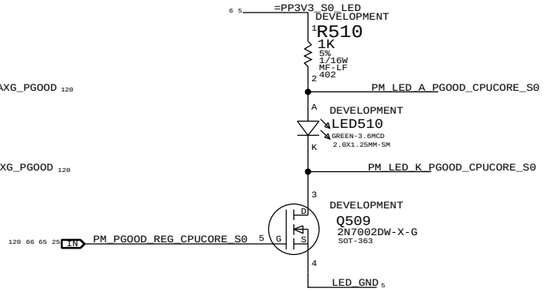
CPU 1V05_S0 LED



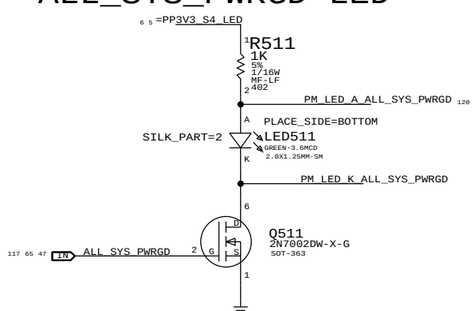
CPU AXG LED



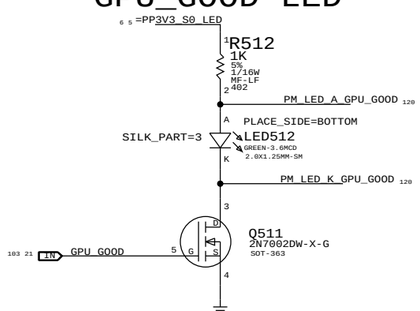
CPU VCORE LED



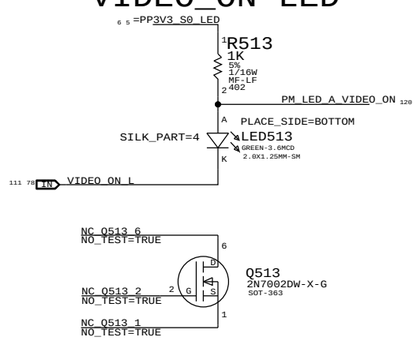
ALL_SYS_PWRGD LED



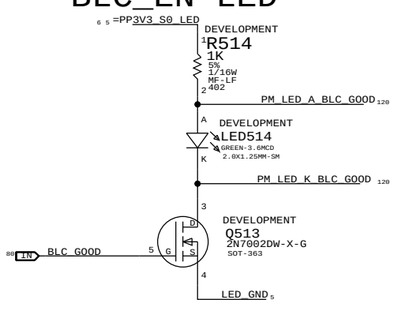
GPU_GOOD LED



VIDEO_ON LED



BLC_EN LED



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: DEBUG LEDS

Apple Inc.

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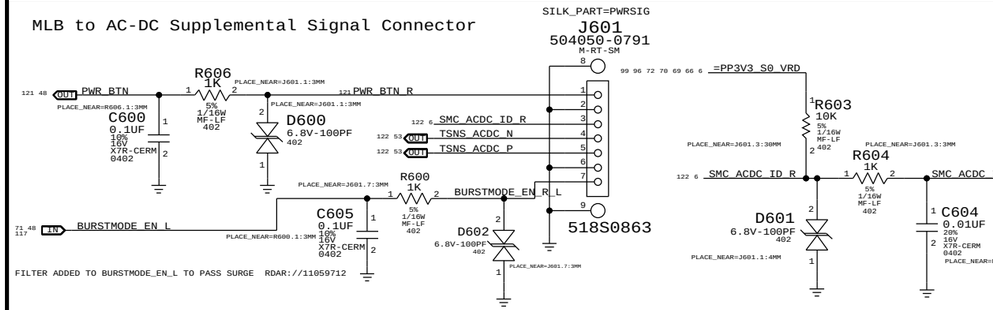
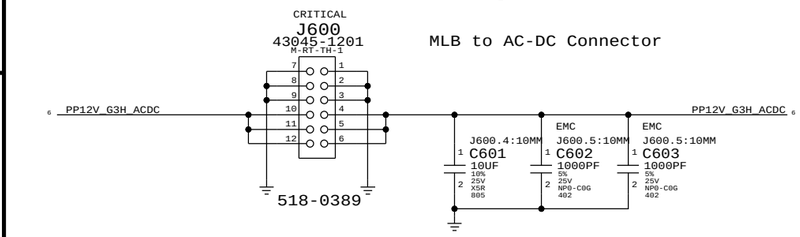
MLB to AC-DC Supplemental Signal Connector



MLB to AC-DC Connector



G3 Rails

Always on: Keeps the PCH RTC alive

PP3V3_G3 (MAKE_BASE=TRUE)	=PP3V3_G3_RTC	26 121
	=PP3V3_G3_PCH_RTC	22
	=PP3V3_G3_PCH	18 19

G3H Rails

On with AC/DC plugged in

PP12V_ACDC (MAKE_BASE=TRUE)	=PP12V_G3H_ACDC	6
	=PP12V_G3H_PWR	51
PP12V_G3H (MAKE_BASE=TRUE)	=PP12V_G3H_SNS	51
	=PP12V_G3H_P3V42	73
	=PP12V_G3H_FET_P12V_S0	74
	=PP12V_G3H_FET_P12V_S5	74
PP3V42_G3H (MAKE_BASE=TRUE)	=PP3V42_G3H_REG	73
	=PP3V3_G3H_BT	35
	=PP3V3_G3H_RTC_D	26
	=PP3V3_G3H_SMC	47 48 50
	=PP3V3_G3H_SMC_USBMUX	45
	=PPVIN_G3H_SMCVREF	48
	=PP3V3_G3H_LPCPLUS	49

S5 Rails

On when in S5

PP12V_S5 (MAKE_BASE=TRUE)	=PP12V_S5_FET	74
	=PP12V_S5_REG_P3V3P5V_S5	71
	=PP12V_S5_REG_VDDQ_S3	72
	=PP12V_S5_PWRCTL	64 65 74
	=PPHV_SW_TBTAPWRSW	77
	=PPHV_SW_TBTBPWRSW	79
	=PP12V_S5_SNS	51
PP5V_S5 (MAKE_BASE=TRUE)	=PP5V_S5_LDO	71
	=PP5V_S5_PWRCTL	71
	=PP5V_S5_PCH	24
PP3V3_S5 (MAKE_BASE=TRUE)	=PP3V3_S5_REG	71
	=PP3V3_S5_FET_P3V3_S0	74
	=PP3V3_S5_FET_P3V3_S4	74
	=PP3V3_S5_SMC	48
	=PP3V3_S5_LED	5
	=PP3V3_S5_PCH	19 24 26
	=PP3V3_S5_PCH_STRAPS	15
	=PP3V3_S5_PCH_VCCSUS_HDA	22 24
	=PP3V3_S5_PCH_VCCSUS_USB	22 24
	=PP3V3_S5_PCH_VCC_DSW	22 24
	=PP3V3_S5_PCH_VCC_SPI	22 24
	=PP3V3_S5_PWRCTL	64 65
	=PP3V3_S5_ROM	49
	=PP3V3_S5_VRD	71
	=PP3V3_S5_XDP	25
	=PP3V3_S5_SMC_USBMUX	45 46
	=PP3V3_S5_SENSE	51
	=PP3V3_S5_SDCARD	41

S4 Rails

Enabled when system has AC and is in run or sleep

PP5V_S4 (MAKE_BASE=TRUE)	=PP5V_S4_REG	71
	=PP5V_S4_REG_VDDQ_S3	72
	=PP5V_S4_FET_P5V_S0	74
	=PP5V_S4_MEMRESET	28
	=PP5V_S4_USB	45 46
	=PP5V_S4_CAMERA	42
PP3V3_S4 (MAKE_BASE=TRUE)	=PP3V3_S4_FET	74
	=PP3V3_S4_ALS	42
	=PP3V3_S4_AP_PWR	55
	=PP3V3_S4_CAMERA	42 43
	=PP3V3_S4_ENET	40
	=PP3V3_S4_LED	5
	=PP3V3_S4_MEMRESET	28
	=PP3V3_S4_PM	28
	=PP3V3_S4_PWRCTL	65 72 74
	=PP3V3_S4_SENSE	51
	=PP3V3_S4_SMBUS	50
	=PP3V3_S4_SMBUS_SMC	50
	=PP3V3_S4_SMC	48
	=PP3V3_S4_TBT	36 37 38 77 79
	=PP3V3_S4_TBTAPWRSW	48 77
	=PP3V3_S4_TBTBPWRSW	48 79
	=PP3V3_S4_USB_HUB	27
	=PP3V3_S4_VREFMRGN	34
	=PP3V3_S4_AUDIO_DIG	60
PP3V3_S4_AP (MAKE_BASE=TRUE)	PP3V3_S4_AP_SNS	55
	=PP3V3_S4_AP	15 35
PP3V3_S4_ENET (MAKE_BASE=TRUE)	PP3V3_S4_ENET_FET	40
	=PP3V3_S4_ENET_FET	39 40
	=PP3V3_S4_ENET_SYSCLK	26
	=PP3V3_S4_ENET_CLK	26

S3 Rails

Enabled when system is in run or sleep

PPVDDQ_S3 (MAKE_BASE=TRUE)	PPVDDQ_S3_REG	72
	=PPVDDQ_S3_DDR_PWR	51
	=PPVDDQ_S3_FET_VDDQ_S0	74
	=PPVDDQ_S3_LDO_DDRVTT	72
THIS IS 1.5V RAIL		
PPVDDQ_S3_DDR (MAKE_BASE=TRUE)	PPVDDQ_S3_DDR_SNS	51
	=PPVDDQ_S3_DDR_VREF	34
	=PPVDDQ_S3_MEM_A	29 30
	=PPVDDQ_S3_MEM_B	31 32
	=PPVDDQ_S3_MEMRESET	28
THIS IS 1.5V RAIL		
PPDDRVTT_S3 (MAKE_BASE=TRUE)	PPDDRVTT_S3_LDO	72
	=PPDDRVTT_S3_VREFCA	34
THIS IS 1.5V RAIL		

S0 Rails

Enabled when system is in run

PP12V_S0 (MAKE_BASE=TRUE)	PP12V_S0_FET	74
	=PP12V_S0_AUDIO_SPKRAMP	58 59
	=PP12V_S0_FAN	54
	=PP12V_S0_FBVDDQ_PWR	51
	=PP12V_S0_REG_GPUCORE	96
	=PP12V_S0_HDD_PWR	51
	=PP12V_S0_LCD	78
	=PP12V_S0_REG_CPUCORE	67
	=PP12V_S0_REG_CPU_P1V05_PWR	55
	=PP12V_S0_REG_CPU_VCCSA_PWR	55
	=PP12V_S0_REG_P1V05_PWR	55
	=PP12V_S0_PWRCTL	65
PP12V_S0_HDD (MAKE_BASE=TRUE)	PP12V_S0_HDD_SNS	51
	=PP12V_S0_HDD	52
PP12V_S0_BLC (MAKE_BASE=TRUE)	PP12V_S0_BLC_FET	74
	=PP12V_S0_BLC	82
PP12V_S0_FBVDDQ (MAKE_BASE=TRUE)	PP12V_S0_FBVDDQ_SNS	51
	=PP12V_S0_REG_FBVDDQ	99
PP12V_S0_CPU_P1V05 (MAKE_BASE=TRUE)	PP12V_S0_REG_CPU_P1V05_SNS	55
	=PP12V_S0_REG_CPU_P1V05	69
PP12V_S0_VCCSA (MAKE_BASE=TRUE)	PP12V_S0_REG_CPU_VCCSA_SNS	55
	=PP12V_S0_REG_VCCSA	70
PP12V_S0_P1V05 (MAKE_BASE=TRUE)	PP12V_S0_REG_P1V05_SNS	55
	=PP12V_S0_REG_P1V05	99
PP5V_S0 (MAKE_BASE=TRUE)	PP5V_S0_FET	74
	=PP5V_S0_AUDIO	56 63
	=PP5V_S0_BLC	82
	=PP5V_S0_HDD_PWR	51
	=PP5V_S0_ISENSE	51
	=PP5V_S0_LPCPLUS	49
	=PP5V_S0_PCH	24
	=PP5V_S0_REG_CPUCORE	66
	=PP5V_S0_REG_CPU_P1V05	69
	=PP5V_S0_REG_FBVDDQ	99
	=PP5V_S0_REG_P1V05	99
	=PP5V_S0_REG_P1V8	72
	=PP5V_S0_REG_VCCSA	70
	=PP5V_S0_VRD	72 96
PP5V_S0_HDD (MAKE_BASE=TRUE)	PP5V_S0_HDD_SNS	51
	=PP5V_S0_HDD	52
PP3V3_S0 (MAKE_BASE=TRUE)	PP3V3_S0_FET	74
	=PP3V3_S0_GPU_IFPX_PLLVDD	90
	=PP3V3_S0_GPU_MISC	92
	=PP3V3_S0_GPU_VDD33	91
	=PP3V3_S0_AUDIO	42 56 58 59 62
	=PP3V3_S0_AUDIO_DIG	60
	=PP3V3_S0_BLC	80
	=PP3V3_S0_DP	76 78
	=PP3V3_S0_ENET	39
	=PP3V3_S0_FAN	54
	=PP3V3_S0_GPU	83 91 92 95 96
	=PP3V3_S0_INTDPMUX	75
	=PP3V3_S0_LED	5
	=PP3V3_S0_LED_SATA	15 44
	=PP3V3_S0_MEM_A_SPD	29 30
	=PP3V3_S0_MEM_B_SPD	31 32
	=PP3V3_S0_P3V3TBTFET	38
	=PP3V3_S0_PCH	18 21 24
	=PP3V3_S0_PCH_GPIO	15 19 20 38
	=PP3V3_S0_PCH_PM	26
	=PP3V3_S0_PCH_STRAPS	15
	=PP3V3_S0_PCH_VCC	22 24
	=PP3V3_S0_PCH_VCC_ADAC	17
	=PP3V3_S0_PCH_VCC_GPIO	22 24
	=PP3V3_S0_PCH_VCC_HVCMOS	22 24
	=PP3V3_S0_PCH_VCC_PCI	22 24
	=PP3V3_S0_PWRCTL	28 74
	=PP3V3_S0_RSTBUF	26
	=PP3V3_S0_SDCARD	41
	=PP3V3_S0_SENSE	51 52 53 55
	=PP3V3_S0_SMBUS	50
	=PP3V3_S0_SMBUS_SMC	50
	=PP3V3_S0_SMBUS_TCON	50
	=PP3V3_S0_SMC	48 51 91
	=PP3V3_S0_TBTPWRCTL	38
	=PP3V3_S0_VRD	6 66 69 70 72 96 99
	=PP3V3_S0_SSD_PWR	51
PP3V3_S0_SSD (MAKE_BASE=TRUE)	PP3V3_S0_SSD_SNS	51
	=PP3V3_S0_SSD	44
PP1V8_S0 (MAKE_BASE=TRUE)	PP1V8_S0_REG	72
	=PP1V8_S0_CPU_PLL	13 16
	=PP1V8_S0_PCH	19
	=PP1V8_S0_PCH_VCC_DFTERM	22 24
	=PP1V8_S0_PCH_VCC_VRM	24
	=PP1V8_S0_PCH_CLK	26
PP1V5_S0 (MAKE_BASE=TRUE)	PP1V5_S0_FET	74
	=PP1V5_S0_AUD_DIG	56
	=PP1V5_S0_CPU_MEM_PWR	51
	=PP1V5_S0_DP	75
PP1V5_S0_CPU_MEM (MAKE_BASE=TRUE)	PP1V5_S0_CPU_MEM_SNS	51
	=PP1V5_S0_CPU_MEM	11 13 16
PPDDRVTT_S0 (MAKE_BASE=TRUE)	PPDDRVTT_S0_LDO	72
	=PPDDRVTT_S0_CLAMP	28
	=PPDDRVTT_S0_MEM_A	29 30
	=PPDDRVTT_S0_MEM_B	31 32
PPDDRVREF_DQ_MEM_A_S3 (MAKE_BASE=TRUE)	PPDDRVREF_DQ_MEM_A	34
	=PPDDRVREF_DQ_MEM_A	29 30
PPDDRVREF_CA_MEM_A_S3 (MAKE_BASE=TRUE)	PPDDRVREF_CA_MEM_A	34
	=PPDDRVREF_CA_MEM_A	29 30
PPDDRVREF_DQ_MEM_B_S3 (MAKE_BASE=TRUE)	PPDDRVREF_DQ_MEM_B	34
	=PPDDRVREF_DQ_MEM_B	31 32
PPDDRVREF_CA_MEM_B_S3 (MAKE_BASE=TRUE)	PPDDRVREF_CA_MEM_B	34
	=PPDDRVREF_CA_MEM_B	31 32
PP1V05_S0_CPU (MAKE_BASE=TRUE)	PP1V05_S0_CPU_REG	69
	=PPVCCIO_S0_CPU	10 11 13 16 28 66
	=PPVCCIO_S0_SMC	48
	=PPVCCIO_S0_XDP	25
PP1V05_S0 (MAKE_BASE=TRUE)	PP1V05_S0_REG	99
	=PP1V05_S0_PCH_PWR	51
	=PP1V05_S0_P1V05TBTFET	38
	=PP1V05_S0_GPU_IFPCD_IOVDD	90
	=PP1V05_S0_GPU_IFPEF_IOVDD	90
	=PP1V05_S0_GPU_PEX_PLLVDD	83 95
	=PP1V05_S0_GPU_PEX_IOVDD	83
PPVCORE_S0_CPU (MAKE_BASE=TRUE)	PPCPUCORE_S0_REG	67 68
	=PPVCORE_S0_CPU	13 16 51 66
PPVAXG_S0 (MAKE_BASE=TRUE)	PPCPUAXG_S0_REG	17 68
	=PPVAXG_S0_CPU	13 17 51 66
PPVCCSA_S0 (MAKE_BASE=TRUE)	PPVCCSA_S0_REG	70
	=PPVCCSA_S0_CPU	13 16

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

PP3V3_TBTLC (MAKE_BASE=TRUE)	=PP3V3_TBTLC_FET	38
	=PP3V3_TBT_PCH_GPIO	15
	=PP3V3_TBTLC_RTR	15 36 37 38 50
	=PP3V3_TBT_CLK	26
PP1V05_TBTLC (MAKE_BASE=TRUE)	=PP1V05_TBTLC_FET	38
	=PP1V05_TBTLC_RTR	37
PP1V05_TBTCIO (MAKE_BASE=TRUE)	=PP1V05_TBTCIO_FET	38
	=PP1V05_TBTCIO_RTR	37

Ground/Common

GND (MAKE_BASE=TRUE)

GPU Rails (S0)

Enabled when system is in run

PPVCORE_S0_GPU (MAKE_BASE=TRUE)	PPGPUCORE_S0_REG	97 98
	=PPVCORE_S0_GPU	51 93
PPFBVDDQ_S0_GPU (MAKE_BASE=TRUE)	PP1V5R1V35_S0_GPU_REG	99 115
	=PP1V35_S0_GPU_FBVDDQ	84 85 86 87 88 89
PP1V05_S0_PCH (MAKE_BASE=TRUE)	PP1V05_S0_PCH_SNS	51
	=PP1V05_S0_PCH	18
	=PP1V05_S0_PCH_VCCCLKDMI	22 24
	=PP1V05_S0_PCH_VCCIO_DMI	22 24
	=PP1V05_S0_PCH_VCCIO_PCIE	18 19 22 24
	=PP1V05_S0_PCH_VCCIO_SATA	18 22 24
	=PP1V05_S0_PCH_VCCIO_USB	22 24
	=PP1V05_S0_PCH_VCC_ADPLL	17
	=PP1V05_S0_PCH_VCC_ASW	22 24
	=PP1V05_S0_PCH_VCC_CORE	22 24
	=PP1V05_S0_PCH_VCC_DIFFCLK	22 24
	=PP1V05_S0_PCH_VCC_DMI	22 24
	=PP1V05_S0_PCH_VCC_SSC	22 24
	=PP1V05_S0_PCH_V_PROC_IO	22 24

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
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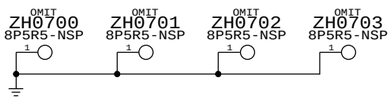
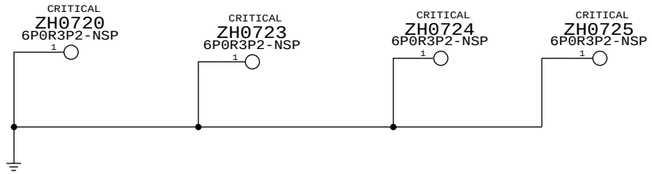
CPU Heatsink

4MM PLATED HOLES (998-4158)



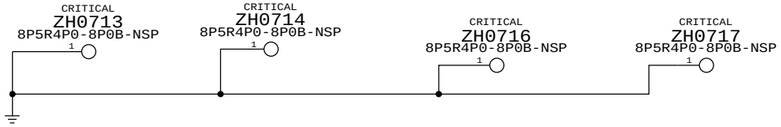
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



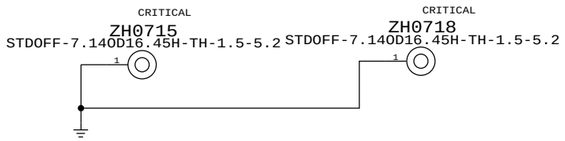
Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



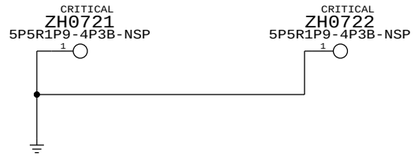
Rear Cover

860-1487 (PCB STANDOFF)



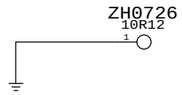
WIRELESS CARD MTG HOLES

998-4938 (PLATED HOLES, 1.9MM INNER DIAMETER, 4.3MM PAD)



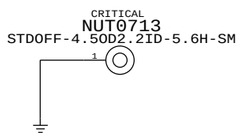
HEATPIPE MTG HOLES

998-4640 (PLATED HOLES, 10MM DIA, 12MM PAD)



SSD STANDOFF

APN: 860-1461



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Holes/PD parts

Apple Inc.

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CPU Reserved

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>	MAKE_BASE=TRUE NO_TEST=TRUE
10	CPU_CFG<15..12>	TP_CPU_CFG<15..12>	MAKE_BASE=TRUE

CPU Memory

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSNX<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSPX<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSNX<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSPX<8>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCIe

18	TP_PCIE1_D2RN	NC_PCIE1_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE1_D2RP	NC_PCIE1_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE1_R2D_CN	NC_PCIE1_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE1_R2D_CP	NC_PCIE1_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_D2RN	NC_PCIE2_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_D2RP	NC_PCIE2_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_R2D_CN	NC_PCIE2_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_R2D_CP	NC_PCIE2_R2D_PNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_N	NC_DMI_MIDBUS_CLK100NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_P	NC_DMI_MIDBUS_CLK100PX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE0N	NC_PCIE_CLK100M_PE0NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE0P	NC_PCIE_CLK100M_PE0PX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4PX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5PX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6NX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6PX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7NX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7PX	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_N<3..0>	NC_PE_TNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_P<3..0>	NC_PE_TPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_N<3..0>	NC_PE_RNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_P<3..0>	NC_PE_RPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH USB

20	USB_PCH_4_N	NC_USB_PCH_4NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_4_P	NC_USB_PCH_4PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_N	NC_USB_PCH_5NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_P	NC_USB_PCH_5PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_N	NC_USB_PCH_6NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_P	NC_USB_PCH_6PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_N	NC_USB_PCH_11NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_P	NC_USB_PCH_11PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_N	NC_USB_PCH_12NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_P	NC_USB_PCH_12PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_N	NC_USB_PCH_13NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_P	NC_USB_PCH_13PX	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCH_CLK25M_XTALOUT	NC_PCH_CLK25M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Unused Display

19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_N	NC_DP_IG_B_AUXNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_P	NC_DP_IG_B_AUXPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_HPD	NC_DP_IG_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_N	NC_DP_IG_C_AUXNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_P	NC_DP_IG_C_AUXPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_HPD	NC_DP_IG_C_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXN	NC_DP_IG_D_AUXNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXP	NC_DP_IG_D_AUXPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_HPD	NC_DP_IG_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTCTL	NC_PCH_L_BKLTCTL	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN	MAKE_BASE=TRUE NO_TEST=TRUE

PCH SATA

18	TP_SATA_C_R2D_CN	NC_SATA_C_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_R2D_CP	NC_SATA_C_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RN	NC_SATA_C_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RP	NC_SATA_C_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RN	NC_SATA_D_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RP	NC_SATA_D_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RN	NC_SATA_E_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RP	NC_SATA_E_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RN	NC_SATA_F_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RP	NC_SATA_F_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Reserved

19	TP_PCH_RESERVE_0	NC_PCH_RESERVE_0	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_1	NC_PCH_RESERVE_1	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_2	NC_PCH_RESERVE_2	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_3	NC_PCH_RESERVE_3	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_4	NC_PCH_RESERVE_4	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_5	NC_PCH_RESERVE_5	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_6	NC_PCH_RESERVE_6	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_7	NC_PCH_RESERVE_7	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_8	NC_PCH_RESERVE_8	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_9	NC_PCH_RESERVE_9	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_10	NC_PCH_RESERVE_10	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_11	NC_PCH_RESERVE_11	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_12	NC_PCH_RESERVE_12	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_13	NC_PCH_RESERVE_13	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_14	NC_PCH_RESERVE_14	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_15	NC_PCH_RESERVE_15	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_16	NC_PCH_RESERVE_16	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_17	NC_PCH_RESERVE_17	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_18	NC_PCH_RESERVE_18	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_19	NC_PCH_RESERVE_19	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_20	NC_PCH_RESERVE_20	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_21	NC_PCH_RESERVE_21	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_22	NC_PCH_RESERVE_22	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_23	NC_PCH_RESERVE_23	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_24	NC_PCH_RESERVE_24	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_25	NC_PCH_RESERVE_25	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_26	NC_PCH_RESERVE_26	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_27	NC_PCH_RESERVE_27	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_28	NC_PCH_RESERVE_28	MAKE_BASE=TRUE NO_TEST=TRUE

PCH and CPU FDI

10	TP_CPU_FDI_TX_N<7..0>	NC_CPU_FDI_TNX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_TX_P<7..0>	NC_CPU_FDI_TPX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_N<7..0>	NC_PCH_FDI_RNX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_P<7..0>	NC_PCH_FDI_RPX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_FSYNC<1..0>	NC_CPU_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_LSYNC<1..0>	NC_CPU_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_INT	NC_CPU_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_FSYNC<1..0>	NC_PCH_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_LSYNC<1..0>	NC_PCH_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_INT	NC_PCH_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Test Points

21	TP_PCH_TP1	NC_PCH_TP1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP2	NC_PCH_TP2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP3	NC_PCH_TP3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP4	NC_PCH_TP4	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP5	NC_PCH_TP5	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP6	NC_PCH_TP6	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP7	NC_PCH_TP7	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP8	NC_PCH_TP8	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP9	NC_PCH_TP9	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP10	NC_PCH_TP10	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP11	NC_PCH_TP11	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP12	NC_PCH_TP12	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP13	NC_PCH_TP13	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP14	NC_PCH_TP14	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP15	NC_PCH_TP15	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP16	NC_PCH_TP16	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP17	NC_PCH_TP17	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP18	NC_PCH_TP18	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP19	NC_PCH_TP19	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP20	NC_PCH_TP20	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCH_PCI_GNT0_L	NC_PCI_GNT0_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_INIT3V3_L	NC_PCH_INIT3V3_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT2	NC_PCI_CLK33M_OUT2	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

Unused Signal Aliases

Apple Inc.

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ALIASES (BLANK)

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

Signal Aliases

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SHORT B4 & C4 TOGETHER, ROUTE AS A SINGLE 4 MIL TRACE TO R1010.1
ROUTE B5 TO R1010.1 AS A SEPERATE 12 MIL TRACE.

OMIT TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 1 OF 10

DMI
DMI_RX_0*
DMI_RX_1*
DMI_RX_2*
DMI_RX_3*
DMI_RX_0
DMI_RX_1
DMI_RX_2
DMI_RX_3
DMI_TX_0*
DMI_TX_1*
DMI_TX_2*
DMI_TX_3*
DMI_TX_0
DMI_TX_1
DMI_TX_2
DMI_TX_3

FLEXIBLE DISPLAY INTERFACE
(Unused)
FDI_TX_0*
FDI_TX_1*
FDI_TX_2*
FDI_TX_3*
FDI_TX_4*
FDI_TX_5*
FDI_TX_6*
FDI_TX_7*
FDI_TX_0
FDI_TX_1
FDI_TX_2
FDI_TX_3
FDI_TX_4
FDI_TX_5
FDI_TX_6
FDI_TX_7
FDI_FSYNC_0
FDI_FSYNC_1
FDI_INT
FDI_LSYNC_0
FDI_LSYNC_1
FDI_COMPIO
FDI_ICOMPO

PCI EXPRESS -- GRAPHICS
(Available for Workstation only)
PCI EXPRESS
PE_RX_0*
PE_RX_1*
PE_RX_2*
PE_RX_3*
PE_RX_0
PE_RX_1
PE_RX_2
PE_RX_3
PE_TX_0*
PE_TX_1*
PE_TX_2*
PE_TX_3*
PE_TX_0
PE_TX_1
PE_TX_2
PE_TX_3

PEG_COMPI
PEG_ICOMPO
PEG_RCOMPO
PEG_RX_0*
PEG_RX_1*
PEG_RX_2*
PEG_RX_3*
PEG_RX_4*
PEG_RX_5*
PEG_RX_6*
PEG_RX_7*
PEG_RX_8*
PEG_RX_9*
PEG_RX_10*
PEG_RX_11*
PEG_RX_12*
PEG_RX_13*
PEG_RX_14*
PEG_RX_15*
PEG_RX_0
PEG_RX_1
PEG_RX_2
PEG_RX_3
PEG_RX_4
PEG_RX_5
PEG_RX_6
PEG_RX_7
PEG_RX_8
PEG_RX_9
PEG_RX_10
PEG_RX_11
PEG_RX_12
PEG_RX_13
PEG_RX_14
PEG_RX_15
PEG_TX_0*
PEG_TX_1*
PEG_TX_2*
PEG_TX_3*
PEG_TX_4*
PEG_TX_5*
PEG_TX_6*
PEG_TX_7*
PEG_TX_8*
PEG_TX_9*
PEG_TX_10*
PEG_TX_11*
PEG_TX_12*
PEG_TX_13*
PEG_TX_14*
PEG_TX_15*
PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

PLACE_NEAR=U1000.AE2:6.3MM
R1011 0 5% 1/16W MF-LF 402
PLACE_NEAR=U1000.B4:12.7MM
R1010 24.9 1% 1/10W MF-LF 402
=PPVCCIO_S0_CPU

OMIT TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 5 OF 10

RESERVED
RSVD_C38
RSVD_C39
RSVD_D38
RSVD_H7
RSVD_H8
RSVD_J9
RSVD_J31
RSVD_J33
RSVD_J34
RSVD_K9
RSVD_K31
RSVD_K34
RSVD_L9
RSVD_L31
RSVD_L33
RSVD_L34
RSVD_M34 ThermDC
RSVD_N33 ThermDA
RSVD_N34
RSVD_P35
RSVD_P37
RSVD_P39
RSVD_R34
RSVD_R36
RSVD_R38
RSVD_R40
RSVD_AB6
RSVD_AB7
RSVD_AD34
RSVD_AD35
RSVD_AD37
RSVD_AE6
RSVD_AF4
RSVD_AG4
RSVD_AJ11
RSVD_AJ29
RSVD_AJ30
RSVD_AJ31
RSVD_AN20
RSVD_AP20
RSVD_AT11
RSVD_AT14
RSVD_AU10
RSVD_AV34
RSVD_AW34
RSVD_AY10
RSVD_NCTF_AV1
RSVD_NCTF_AW2
RSVD_NCTF_AY3
RSVD_NCTF_B39
NCTF_A38
NCTF_C2
NCTF_D1
NCTF_AU40
NCTF_AW38

NC_SNS_CPU_THERMDN NO TESTPOINT
NC_SNS_CPU_THERMDP NO TESTPOINT

CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17

INTEL SUGGESTS TO KEEP THESE TPS

(IVY BRIDGE EDS #473717 TABLE 6-5)

CFG [1:0]	RESERVED CONFIGURATION LANE	
CFG [2]	PCIE STATIC X16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [3]	PCIE STATIC X4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [4]	RESERVED CONFIGURATION LANE	
CFG [6:5]	PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = 1 X8, 2 X4
CFG [17:7]	RESERVED CONFIGURATION LANE	

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012
PAGE TITLE: CPU DMI/PEG/FDI/RSVD
Apple Inc.
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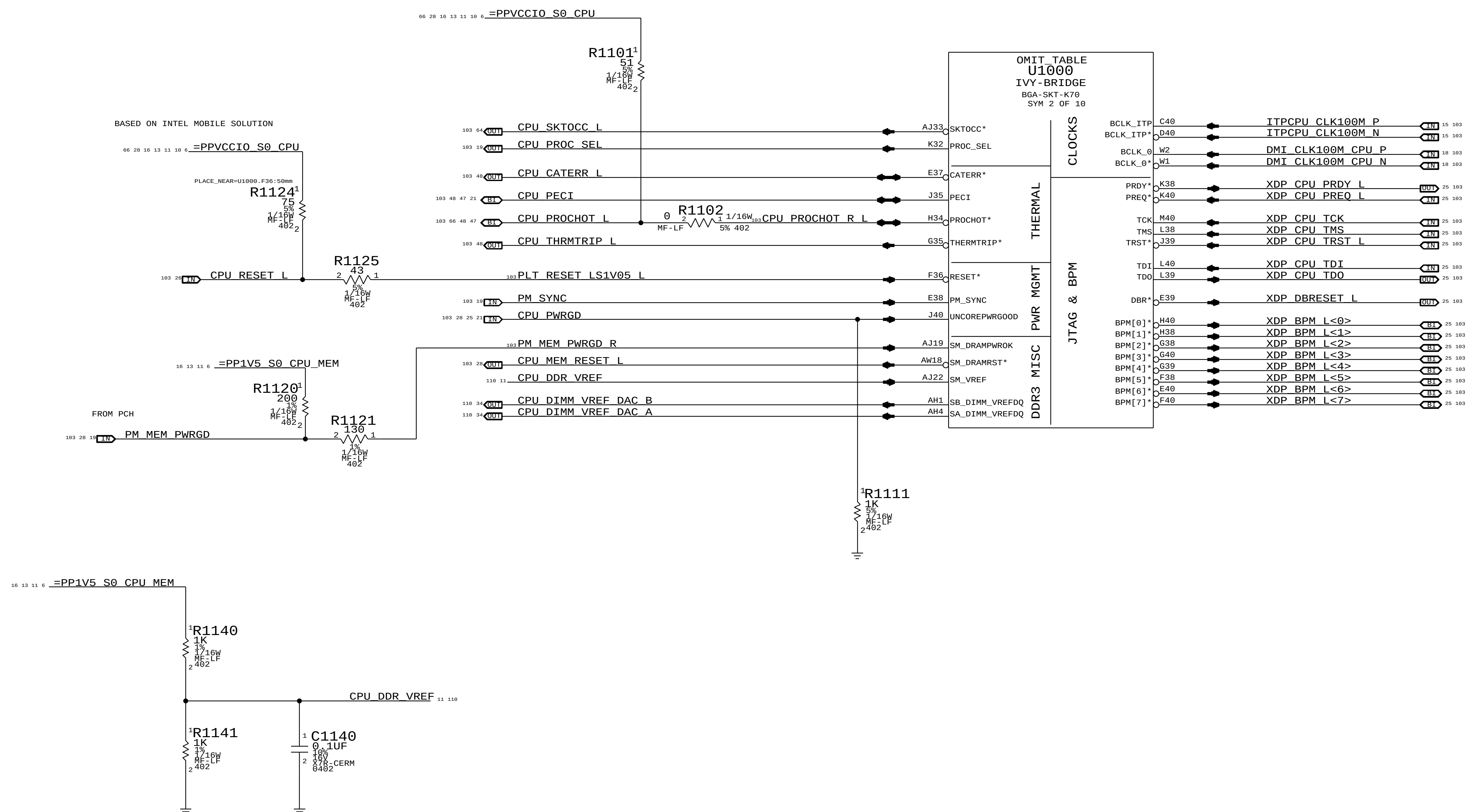
BASED ON INTEL MOBILE SOLUTION
=PPVCCIO_S0_CPU
PLACE_NEAR=U1000.F36:50mm
R1124
75
5%
1/16W
MF-LF
402
CPU_RESET_L
R1125
43
5%
1/16W
MF-LF
402
R1101
51
5%
1/16W
MF-LF
402
CPU_SKTOCC_L
CPU_PROC_SEL
CPU_CATERR_L
CPU_PECI
CPU_PROCHOT_L
R1102
0
MF-LF
1/16W
5% 402
CPU_PROCHOT_R_L
CPU_THRMTRIP_L
PLT_RESET_LS1V05_L
PM_SYNC
CPU_PWRGD
=PP1V5_S0_CPU_MEM
R1120
200
1%
1/16W
MF-LF
402
FROM PCH
PM_MEM_PWRGD
R1121
130
1%
1/16W
MF-LF
402
PM_MEM_PWRGD_R
CPU_MEM_RESET_L
CPU_DDR_VREF
CPU_DIMM_VREF_DAC_B
CPU_DIMM_VREF_DAC_A
R1111
1K
5%
1/16W
MF-LF
402
OMIT_TABLE
U1000
IVY-BRIDGE
BGA-SKT-K70
SYM 2 OF 10
SKTOCC*
PROC_SEL
CATERR*
PECI
PROCHOT*
THERMTRIP*
RESET*
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
SM_DRAMRST*
SM_VREF
SB_DIMM_VREFDQ
SA_DIMM_VREFDQ
CLOCKS
THERMAL
PWR MGMT
DDR3 MISC
JTAG & BPM
BCLK_ITP
BCLK_ITP*
BCLK_0
BCLK_0*
PRDY*
PREQ*
TCK
TMS
TRST*
TDI
TDO
DBR*
BPM[0]*
BPM[1]*
BPM[2]*
BPM[3]*
BPM[4]*
BPM[5]*
BPM[6]*
BPM[7]*
ITPCPU_CLK100M_P
ITPCPU_CLK100M_N
DMI_CLK100M_CPU_P
DMI_CLK100M_CPU_N
XDP_CPU_PRDY_L
XDP_CPU_PREQ_L
XDP_CPU_TCK
XDP_CPU_TMS
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TDO
XDP_DBRESET_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_BPM_L<6>
XDP_BPM_L<7>
=PP1V5_S0_CPU_MEM
R1140
1K
1%
1/16W
MF-LF
402
CPU_DDR_VREF
R1141
1K
1%
1/16W
MF-LF
402
C1140
0.1UF
10%
16V
X7R-CERM
0402

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

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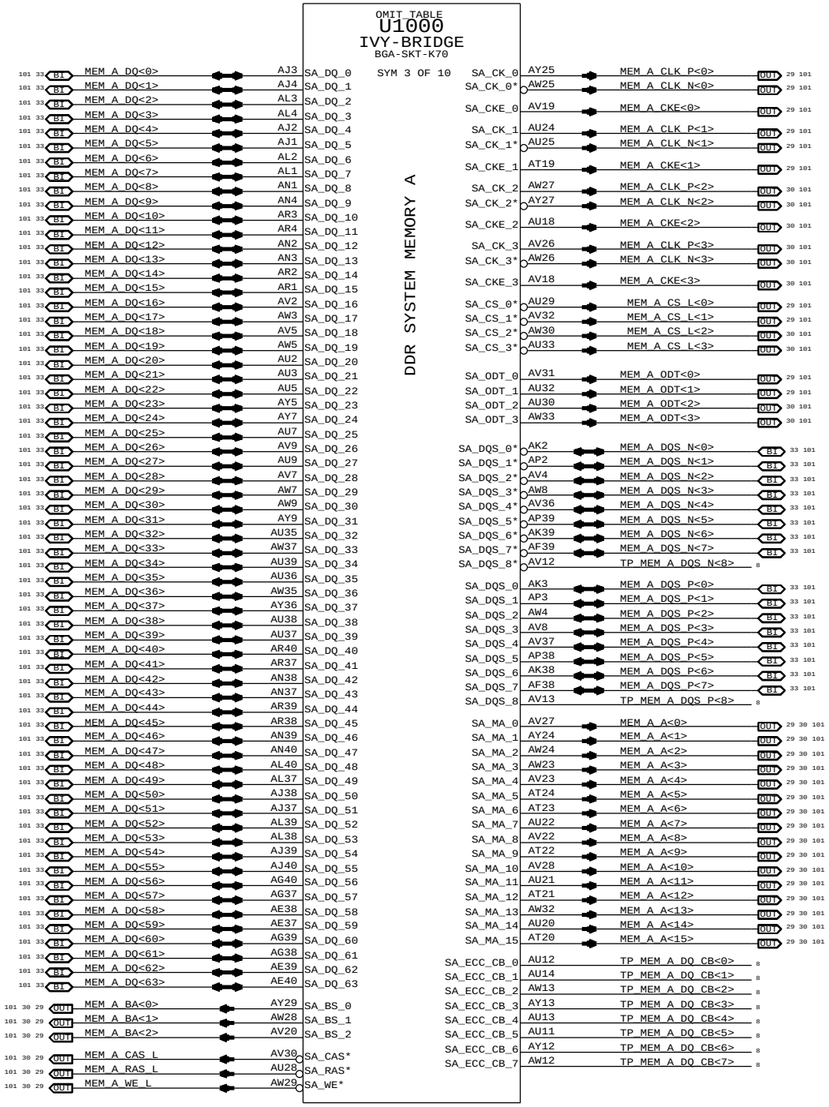

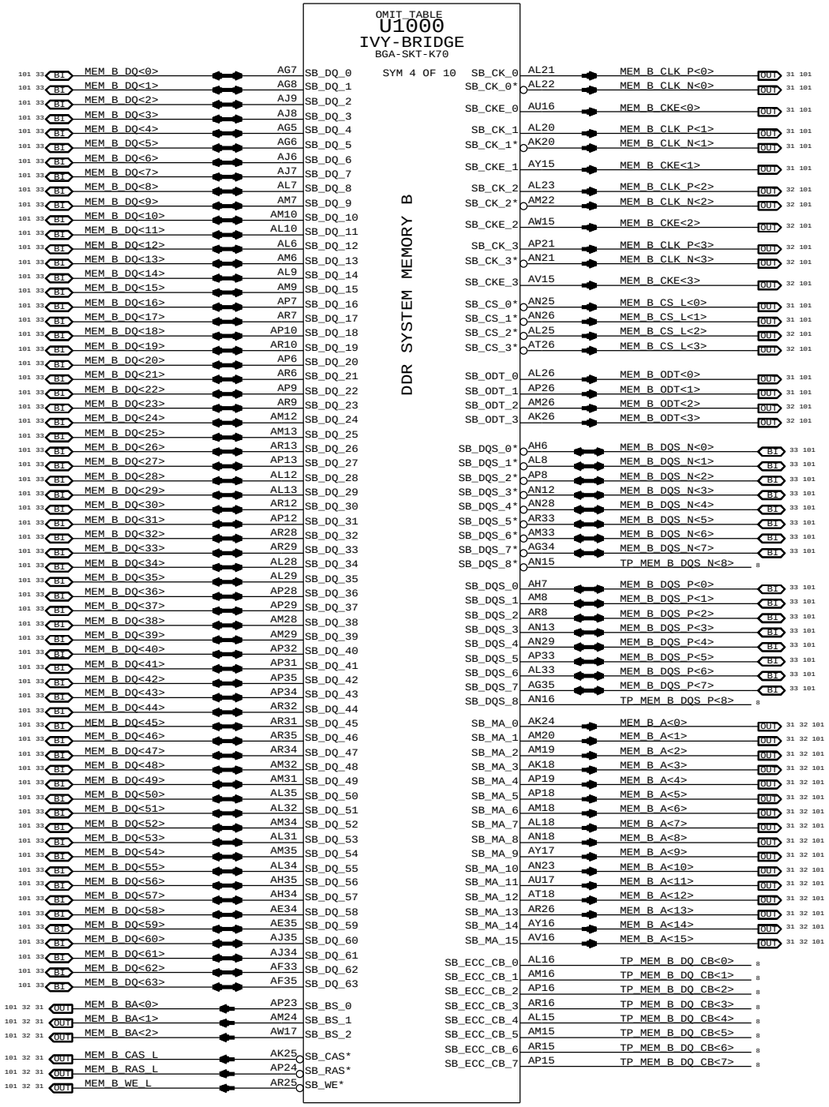

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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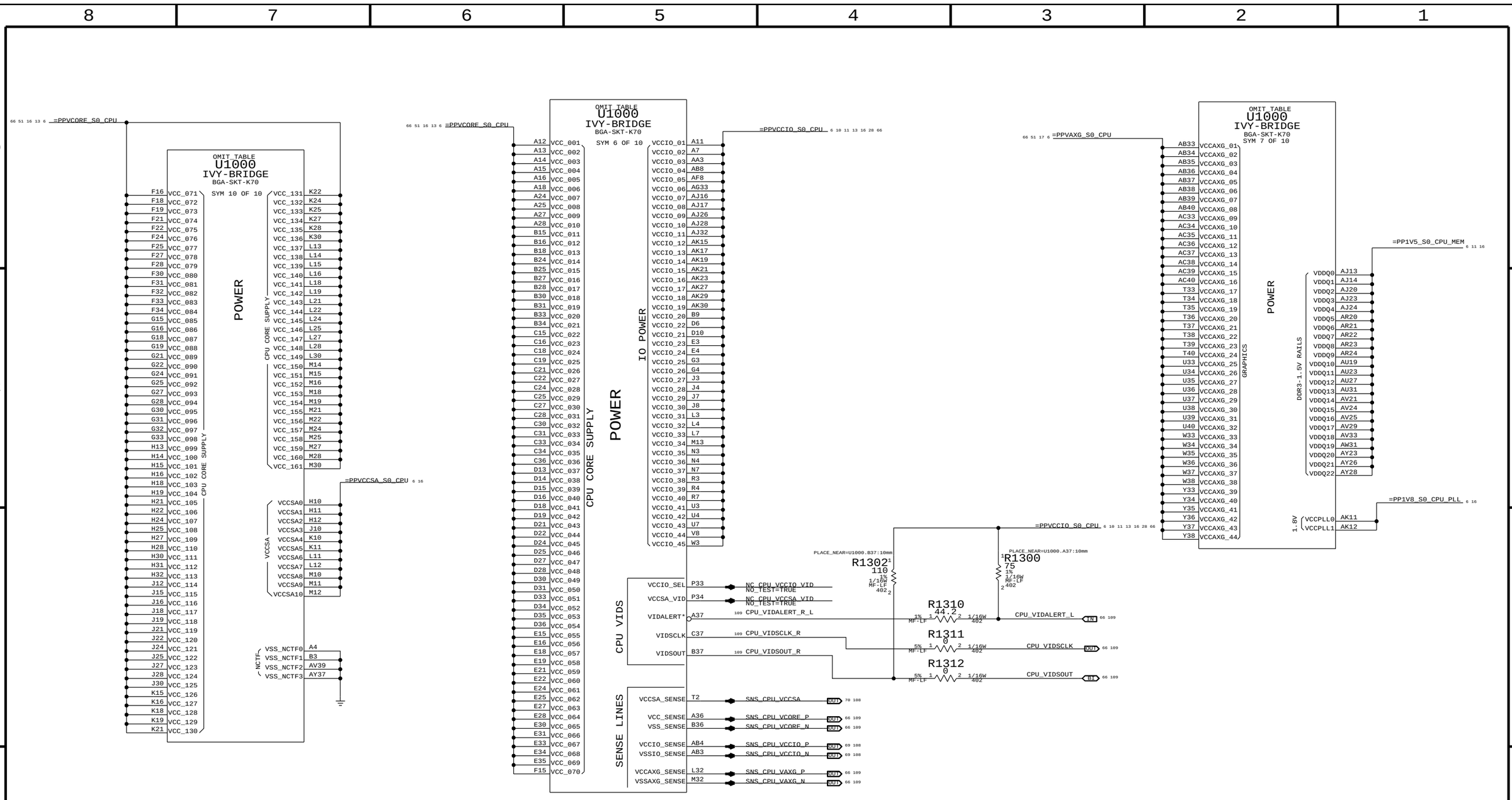

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
CPU POWER

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D
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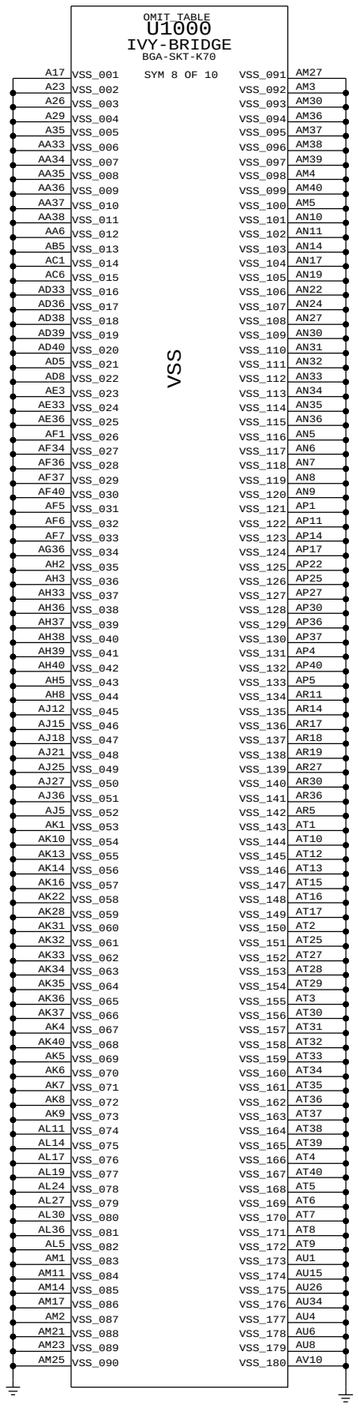

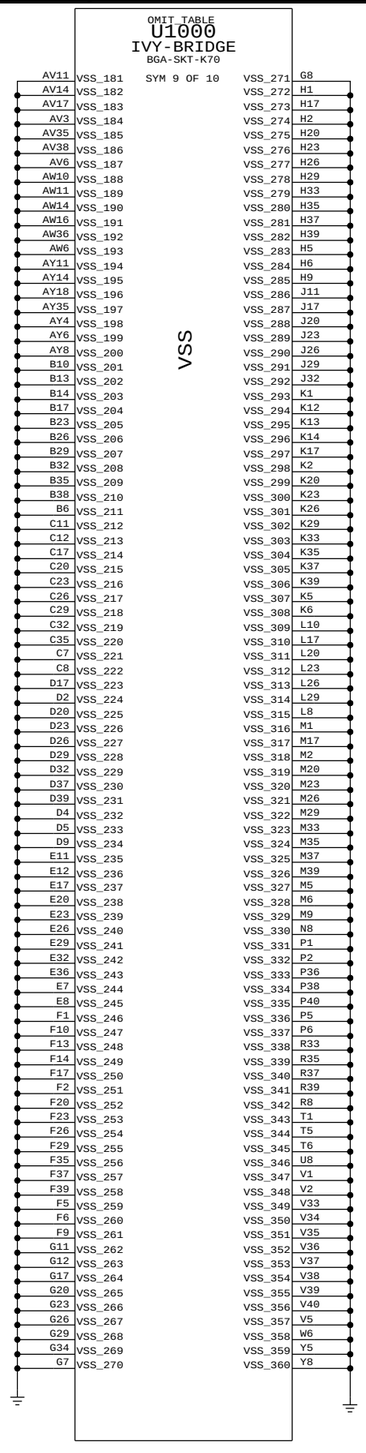

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

CPU GROUNDS

Apple Inc.

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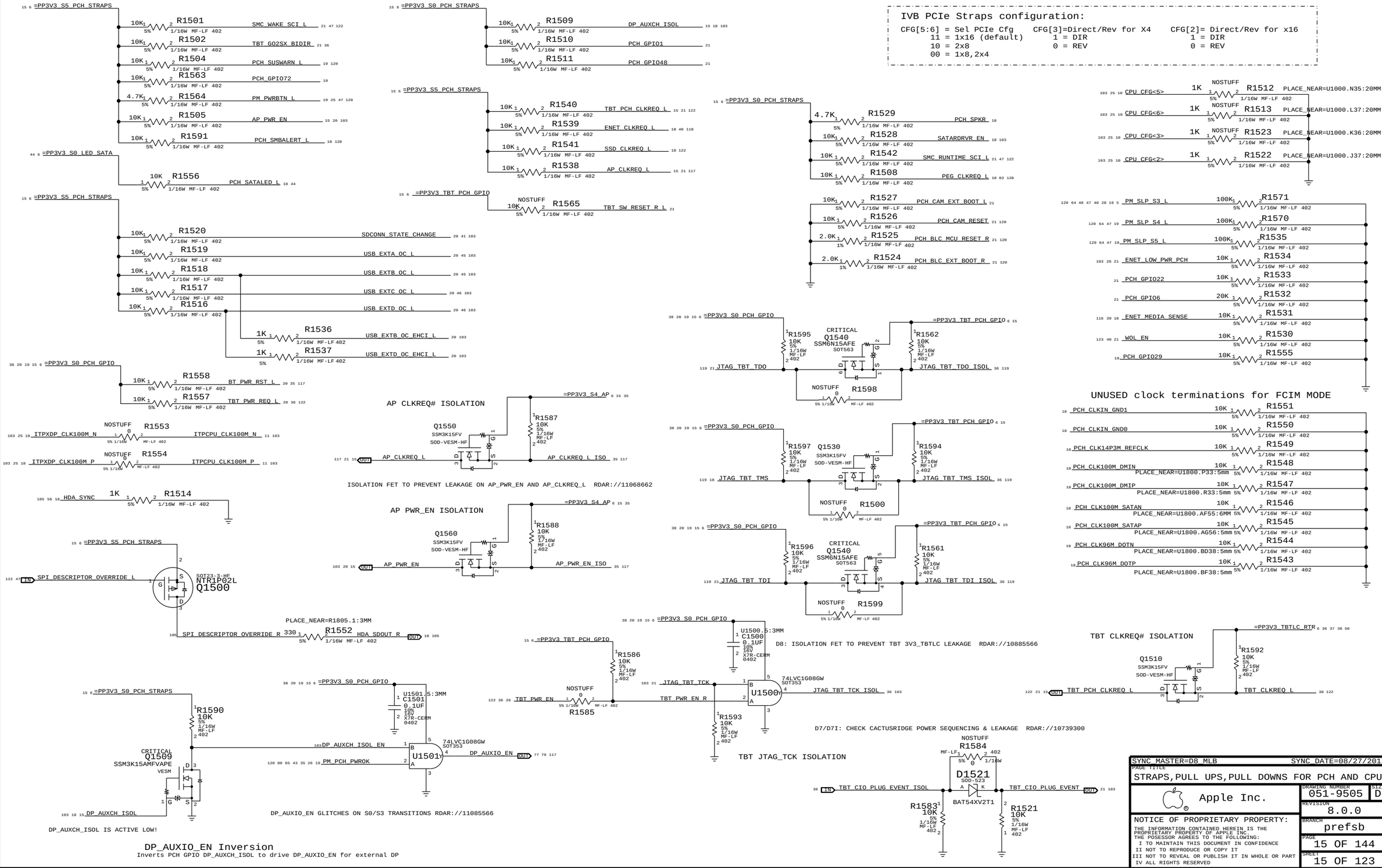
IVB PCIe Straps configuration:
CFG[5:6] = Sel PCIe Cfg
11 = 1x16 (default)
10 = 2x8
00 = 1x8,2x4
CFG[3]=Direct/Rev for X4
1 = DIR
0 = REV
CFG[2]= Direct/Rev for x16
1 = DIR
0 = REV
=PP3V3_S5_PCH_STRAPS
R1501 10K SMC_WAKE_SCI_L
R1502 10K TBT_GO2SX_BIDIR
R1504 10K PCH_SUSWARN_L
R1563 10K PCH_GPIO72
R1564 4.7K PM_PWRBTN_L
R1505 10K AP_PWR_EN
R1591 10K PCH_SMBALERT_L
=PP3V3_S0_LED_SATA
R1556 10K PCH_SATALED_L
=PP3V3_S5_PCH_STRAPS
R1520 10K SDCONN_STATE_CHANGE
R1519 10K USB_EXTA_OC_L
R1518 10K USB_EXTB_OC_L
R1517 10K USB_EXTC_OC_L
R1516 10K USB_EXTD_OC_L
R1536 1K USB_EXTB_OC_EHCI_L
R1537 1K USB_EXTD_OC_EHCI_L
=PP3V3_S0_PCH_GPIO
R1558 10K BT_PWR_RST_L
R1557 10K TBT_PWR_REQ_L
NOSTUFF R1553 0 ITPXDP_CLK100M_N ITPCPU_CLK100M_N
NOSTUFF R1554 0 ITPXDP_CLK100M_P ITPCPU_CLK100M_P
HDA_SYNC 1K R1514
=PP3V3_S5_PCH_STRAPS
SPI_DESCRIPTOR_OVERRIDE_L
Q1500 NTR1P02L SOT23-3-HF
SPI_DESCRIPTOR_OVERRIDE_R
PLACE_NEAR=R1805.1:3MM
R1552 330
HDA_SDOUT_R
=PP3V3_S0_PCH_STRAPS
R1590 10K
CRITICAL
Q1509 SSM3K15AMFVAPE VESM
DP_AUXCH_ISOL
DP_AUXCH_ISOL IS ACTIVE LOW!
DP_AUXIO_EN Inversion
Inverts PCH GPIO DP_AUXCH_ISOL to drive DP_AUXIO_EN for external DP
=PP3V3_S0_PCH_GPIO
U1501.5:3MM
C1501 0.1UF 10% 16V X7R-CERM 0402
U1501 74LVC1G08GW SOT353
DP_AUXCH_ISOL_EN
PM_PCH_PWROK
DP_AUXIO_EN
DP_AUXIO_EN GLITCHES ON S0/S3 TRANSITIONS RDAR://11085566
AP CLKREQ# ISOLATION
=PP3V3_S4_AP
R1587 10K
Q1550 SSM3K15FV SOD-VESM-HF
AP_CLKREQ_L
AP_CLKREQ_L_ISO
ISOLATION FET TO PREVENT LEAKAGE ON AP_PWR_EN AND AP_CLKREQ_L RDAR://11068662
AP PWR_EN ISOLATION
=PP3V3_S4_AP
R1588 10K
Q1560 SSM3K15FV SOD-VESM-HF
AP_PWR_EN
AP_PWR_EN_ISO
=PP3V3_S0_PCH_STRAPS
R1509 10K DP_AUXCH_ISOL
R1510 10K PCH_GPIO1
R1511 10K PCH_GPIO48
=PP3V3_S5_PCH_STRAPS
R1540 10K TBT_PCH_CLKREQ_L
R1539 10K ENET_CLKREQ_L
R1541 10K SSD_CLKREQ_L
R1538 10K AP_CLKREQ_L
=PP3V3_TBT_PCH_GPIO
NOSTUFF R1565 10K TBT_SW_RESET_R_L
=PP3V3_S0_PCH_STRAPS
R1529 4.7K PCH_SPKR
R1528 10K SATARDRVR_EN
R1542 10K SMC_RUNTIME_SCI_L
R1508 10K PEG_CLKREQ_L
R1527 10K PCH_CAM_EXT_BOOT_L
R1526 10K PCH_CAM_RESET
R1525 2.0K PCH_BLC_MCU_RESET_R
R1524 2.0K PCH_BLC_EXT_BOOT_R
=PP3V3_S0_PCH_GPIO
R1595 10K
CRITICAL
Q1540 SSM6N15AFE SOT563
=PP3V3_TBT_PCH_GPIO
R1562 10K
JTAG_TBT_TDO
JTAG_TBT_TDO_ISOL
NOSTUFF R1598 0
=PP3V3_S0_PCH_GPIO
R1597 10K
Q1530 SSM3K15FV SOD-VESM-HF
=PP3V3_TBT_PCH_GPIO
R1594 10K
JTAG_TBT_TMS
JTAG_TBT_TMS_ISOL
NOSTUFF R1500 0
=PP3V3_S0_PCH_GPIO
R1596 10K
CRITICAL
Q1540 SSM6N15AFE SOT563
=PP3V3_TBT_PCH_GPIO
R1561 10K
JTAG_TBT_TDI
JTAG_TBT_TDI_ISOL
NOSTUFF R1599 0
=PP3V3_S0_PCH_GPIO
U1500.5:3MM
C1500 0.1UF 10% 16V X7R-CERM 0402
=PP3V3_TBT_PCH_GPIO
R1586 10K
TBT_PWR_EN
NOSTUFF R1585 0
JTAG_TBT_TCK
U1500 74LVC1G08GW SOT353
JTAG_TBT_TCK_ISOL
R1593 10K
TBT JTAG_TCK ISOLATION
D8: ISOLATION FET TO PREVENT TBT 3V3_TBTLC LEAKAGE RDAR://10885566
D7/D7I: CHECK CACTUSRIDGE POWER SEQUENCING & LEAKAGE RDAR://10739300
NOSTUFF R1584 0
D1521 SOD-523 BAT54XV2T1
TBT_CIO_PLUG_EVENT_ISOL
TBT_CIO_PLUG_EVENT
R1583 10K
R1521 10K
CPU_CFG<5> 1K NOSTUFF R1512 PLACE_NEAR=U1000.N35:20MM
CPU_CFG<6> 1K NOSTUFF R1513 PLACE_NEAR=U1000.L37:20MM
CPU_CFG<3> 1K NOSTUFF R1523 PLACE_NEAR=U1000.K36:20MM
CPU_CFG<2> 1K R1522 PLACE_NEAR=U1000.J37:20MM
PM_SLP_S3_L 100K R1571
PM_SLP_S4_L 100K R1570
PM_SLP_S5_L 100K R1535
ENET_LOW_PWR_PCH 10K R1534
PCH_GPIO22 10K R1533
PCH_GPIO6 20K R1532
ENET_MEDIA_SENSE 10K R1531
WOL_EN 10K R1530
PCH_GPIO29 10K R1555
UNUSED clock terminations for FCIM MODE
PCH_CLKIN_GND1 10K R1551
PCH_CLKIN_GND0 10K R1550
PCH_CLK14P3M_REFCLK 10K R1549
PCH_CLK100M_DMIN 10K R1548 PLACE_NEAR=U1800.P33:5mm
PCH_CLK100M_DMIP 10K R1547 PLACE_NEAR=U1800.R33:5mm
PCH_CLK100M_SATAN 10K R1546 PLACE_NEAR=U1800.AF55:6MM
PCH_CLK100M_SATAP 10K R1545 PLACE_NEAR=U1800.AG56:5mm
PCH_CLK96M_DOTN 10K R1544 PLACE_NEAR=U1800.BD38:5mm
PCH_CLK96M_DOTP 10K R1543 PLACE_NEAR=U1800.BF38:5mm
TBT CLKREQ# ISOLATION
=PP3V3_TBTLC_RTR
R1592 10K
Q1510 SSM3K15FV SOD-VESM-HF
TBT_PCH_CLKREQ_L
TBT_CLKREQ_L
SYNC_MASTER=D8_MLB
SYNC_DATE=08/27/2012
PAGE TITLE
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU
Apple Inc.
DRAWING NUMBER 051-9505
SIZE D
REVISION 8.0.0
BRANCH prefsb
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CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613): REPLACED WITH 603 PER RDAR://10700439

16 13 6 =PPVCORE_S0_CPU

C1600 C1601 C1602 C1603 C1604 C1605 C1606 C1607 C1608 C1609
22UF 20% 6.3V X5R-CERM2 0603

C1610 C1611 C1612 C1613
22UF 20% 6.3V X5R-CERM2 0603

BULK CAPS ON CPU VREG PAGE 72

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

13 11 10 6 66 28 =PPVCCIO_S0_CPU

PLACEMENT_NOTE (C1650-C1657):

C1650 C1651 C1652 C1653 C1654 C1655 C1656 C1657
22UF 20% 6.3V X5R-CERM2 0603

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

C1660 C1661 C1662 C1663 C1664 C1665
10uF 20% 6.3V X5R 603

BULK CAPS ON CPU VREG PAGE 74

CRITICAL
C1670
330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

Memory (CPU VCCDDR) DECOUPLING

13 11 6 =PP1V5_S0_CPU_MEM

C1676 C1677 C1678 C1679 C1680 C1681 C1682 C1683 C1684 C1685 C1686
22UF 20% 6.3V X5R-CERM2 0603
1UF 20% 6.3V X5R 0201

CRITICAL
NOSTUFF
C1687
330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 1x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 C1694 C1692 C1691 C1695 C1690 C1696 C1697
1UF 10% 10V X5R 402
2.2UF 10% 6.3V X5R 402
4.7UF 10% 6.3V X5R-CERM 603
10UF 20% 6.3V X5R 603
22UF 20% 6.3V X5R-CERM2 0603
47UF 20% 6.3V X5R 0805

BULK CAPS ON VTT REG PAGE 77

10x 10UF and 10x 1UF CAPACITORS

66 51 16 13 6 =PPVCORE_S0_CPU

Place inside socket cavity

C1620 C1621 C1622 C1623 C1624 C1625 C1626 C1627 C1628 C1629
10UF 20% 10V X5R 603

C1630 C1631 C1632 C1633 C1634 C1635 C1636 C1637 C1638 C1639
1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

2x 10uF 0603. INTEL RECOMMENDATION 2X 10uF 0805

13 6 =PPVCCSA_S0_CPU

C1666 C1667
10UF 20% 6.3V X5R 603

Bulk decoupling is on VCCSA reg page 75

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PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

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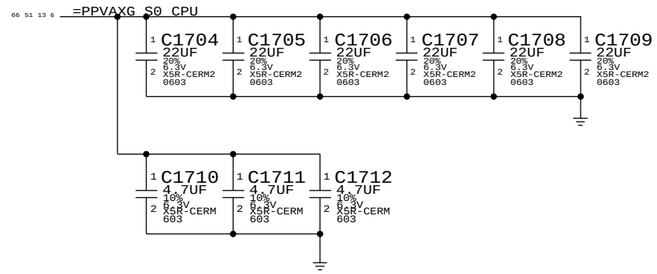
VAXG DECOUPLING

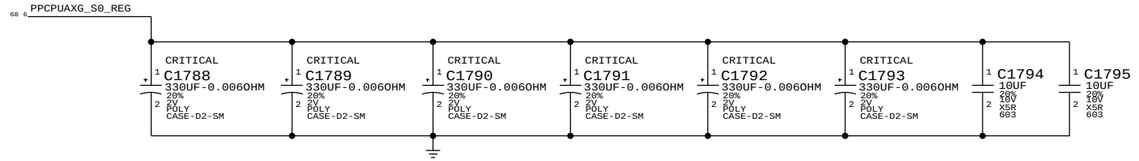
INTEL RECOMMENDATION 4X22UF 0805,3X 4.7UF

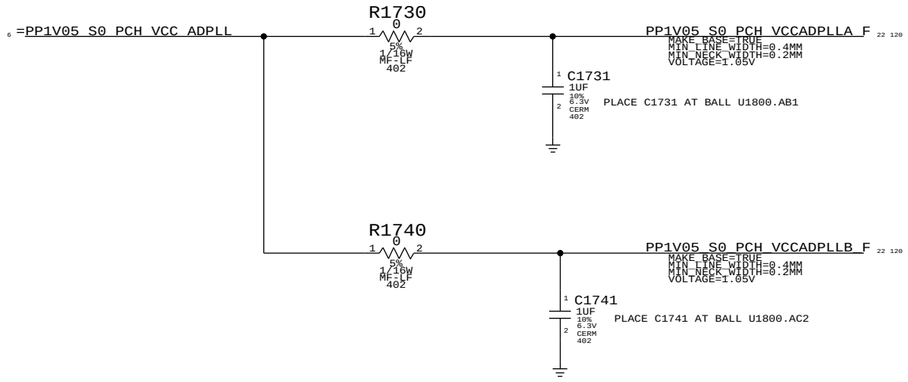
PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity



AXG BULK CAPS





SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: GFX DECOUPLING & PCH PWR ALIAS

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D

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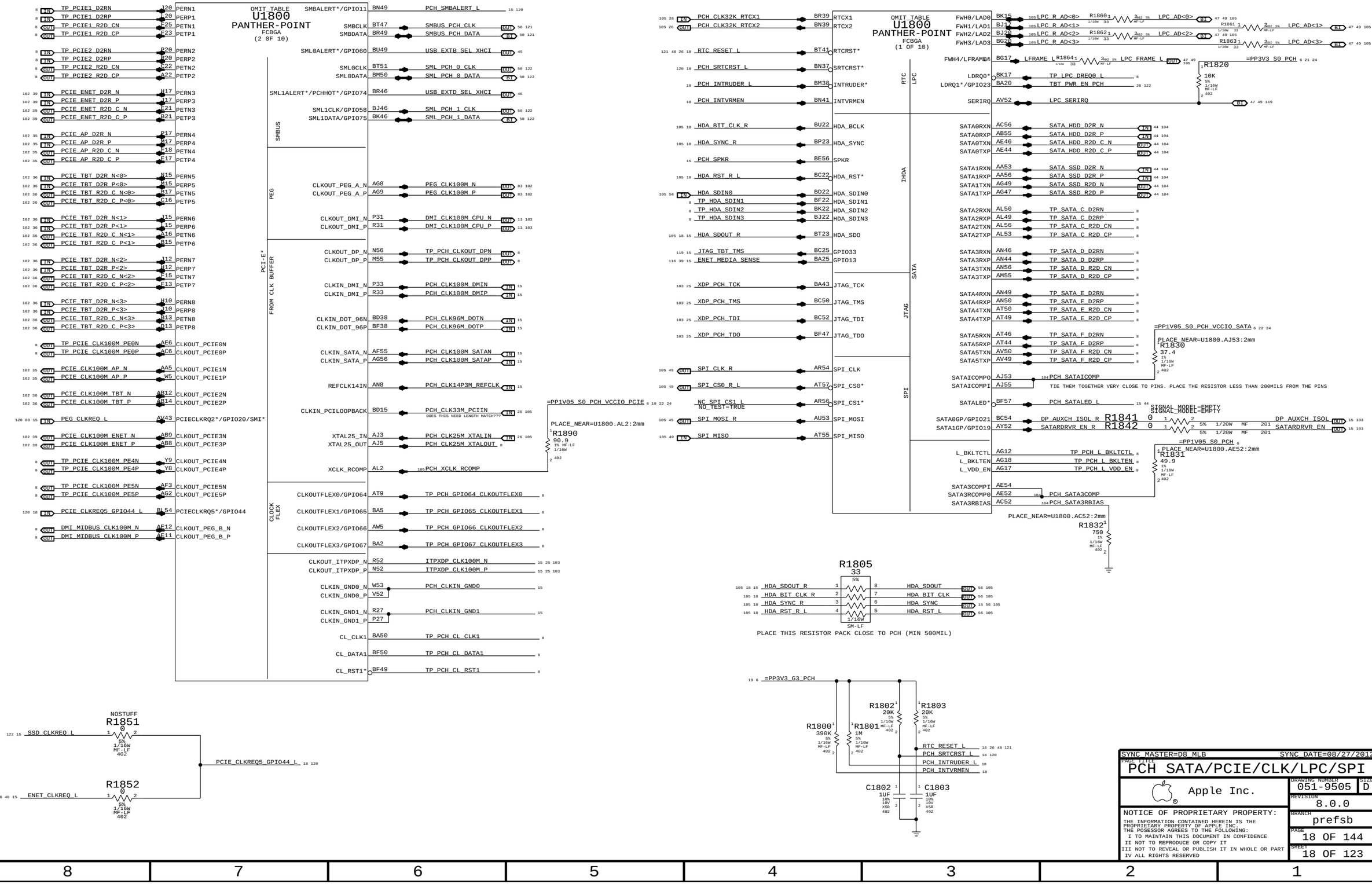
OMIT TABLE
U1800
PANTHER-POINT
FCBGA
(2 0F 10)
PCI-E*
FROM CLK BUFFER
SMBUS
PEG
CLOCK FLEX
TP_PCIE1_D2RN
TP_PCIE1_D2RP
TP_PCIE1_R2D_CN
TP_PCIE1_R2D_CP
TP_PCIE2_D2RN
TP_PCIE2_D2RP
TP_PCIE2_R2D_CN
TP_PCIE2_R2D_CP
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_C_P<3>
TP_PCIE_CLK100M_PE0N
TP_PCIE_CLK100M_PE0P
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PEG_CLKREQ_L
PCIE_CLK100M_ENET_N
PCIE_CLK100M_ENET_P
TP_PCIE_CLK100M_PE4N
TP_PCIE_CLK100M_PE4P
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
PCIE_CLKREQ5_GPIO44_L
DMI_MIDBUS_CLK100M_N
DMI_MIDBUS_CLK100M_P
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20/SMI*
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKIN_GND0_N
CLKIN_GND0_P
CLKIN_GND1_N
CLKIN_GND1_P
CL_CLK1
CL_DATA1
CL_RST1*
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
USB_EXTB_SEL_XHCI
SML_PCH_0_CLK
SML_PCH_0_DATA
USB_EXTD_SEL_XHCI
SML_PCH_1_CLK
SML_PCH_1_DATA
PEG_CLK100M_N
PEG_CLK100M_P
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
TP_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP
PCH_CLK100M_DMIN
PCH_CLK100M_DMIP
PCH_CLK96M_DOTN
PCH_CLK96M_DOTP
PCH_CLK100M_SATAN
PCH_CLK100M_SATAP
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
DOES THIS NEED LENGTH MATCH???
PCH_CLK25M_XTALIN
PCH_CLK25M_XTALOUT
PCH_XCLK_RCOMP
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
PCH_CLKIN_GND0
PCH_CLKIN_GND1
TP_PCH_CL_CLK1
TP_PCH_CL_DATA1
TP_PCH_CL_RST1
=PP1V05_S0_PCH_VCCIO_PCIE
PLACE_NEAR=U1800.AL2:2mm
R1890
90.9
1% MF-LF 1/16W
402
NOSTUFF
R1851
0
R1852
SSD_CLKREQ_L
ENET_CLKREQ_L
PCIE_CLKREQ5_GPIO44_L
5% 1/16W MF-LF 402
OMIT TABLE
U1800
PANTHER-POINT
FCBGA
(1 OF 10)
RTC
LPC
IHDA
SATA
JTAG
SPI
PCH_CLK32K_RTCX1
PCH_CLK32K_RTCX2
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN
HDA_BIT_CLK_R
HDA_SYNC_R
PCH_SPKR
HDA_RST_R_L
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
JTAG_TBT_TMS
ENET_MEDIA_SENSE
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
NC_SPI_CS1_L
NO_TEST=TRUE
SPI_MOSI_R
SPI_MISO
RTCX1
RTCX2
RTCRST*
SRTCRST*
INTRUDER*
INTVRMEN
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST*
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
GPIO33
GPIO13
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
SPI_CLK
SPI_CS0*
SPI_CS1*
SPI_MOSI
SPI_MISO
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME*
LDRQ0*
LDRQ1*/GPIO23
SERIRQ
LPC_R_AD<0>
LPC_R_AD<1>
LPC_R_AD<2>
LPC_R_AD<3>
LFRAME_L
LPC_FRAME_L
TP_LPC_DREQ0_L
TBT_PWR_EN_PCH
LPC_SERIRQ
=PP3V3_S0_PCH
R1820
10K
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_SSD_D2R_N
SATA_SSD_D2R_P
SATA_SSD_R2D_N
SATA_SSD_R2D_P
TP_SATA_C_D2RN
TP_SATA_C_D2RP
TP_SATA_C_R2D_CN
TP_SATA_C_R2D_CP
TP_SATA_D_D2RN
TP_SATA_D_D2RP
TP_SATA_D_R2D_CN
TP_SATA_D_R2D_CP
TP_SATA_E_D2RN
TP_SATA_E_D2RP
TP_SATA_E_R2D_CN
TP_SATA_E_R2D_CP
TP_SATA_F_D2RN
TP_SATA_F_D2RP
TP_SATA_F_R2D_CN
TP_SATA_F_R2D_CP
=PP1V05_S0_PCH_VCCIO_SATA
PLACE_NEAR=U1800.AJ53:2mm
R1830
37.4
SATAICOMPO
SATAICOMPI
PCH_SATAICOMPI
TIE THEM TOGETHER VERY CLOSE TO PINS. PLACE THE RESISTOR LESS THAN 200MILS FROM THE PINS
SATALED*
PCH_SATALED_L
SATA0GP/GPIO21
SATA1GP/GPIO19
DP_AUXCH_ISOL_R
SATARDRVR_EN_R
R1841
R1842
DP_AUXCH_ISOL
SATARDRVR_EN
SIGNAL_MODEL=EMPTY
L_BKLTCTL
L_BKLTEN
L_VDD_EN
TP_PCH_L_BKLTCTL
TP_PCH_L_BKLTEN
TP_PCH_L_VDD_EN
=PP1V05_S0_PCH
PLACE_NEAR=U1800.AE52:2mm
R1831
49.9
SATA3COMPI
SATA3RCOMP0
SATA3RBIAS
PCH_SATA3COMP
PCH_SATA3RBIAS
PLACE_NEAR=U1800.AC52:2mm
R1832
750
R1805
33
5%
HDA_SDOUT_R
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_RST_R_L
HDA_SDOUT
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
1/16W
SM-LF
PLACE THIS RESISTOR PACK CLOSE TO PCH (MIN 500MIL)
=PP3V3_G3_PCH
R1800
390K
R1801
1M
R1802
20K
R1803
20K
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN
C1802
1UF
C1803
1UF
SYNC_MASTER=D8_MLB
SYNC_DATE=08/27/2012
PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI
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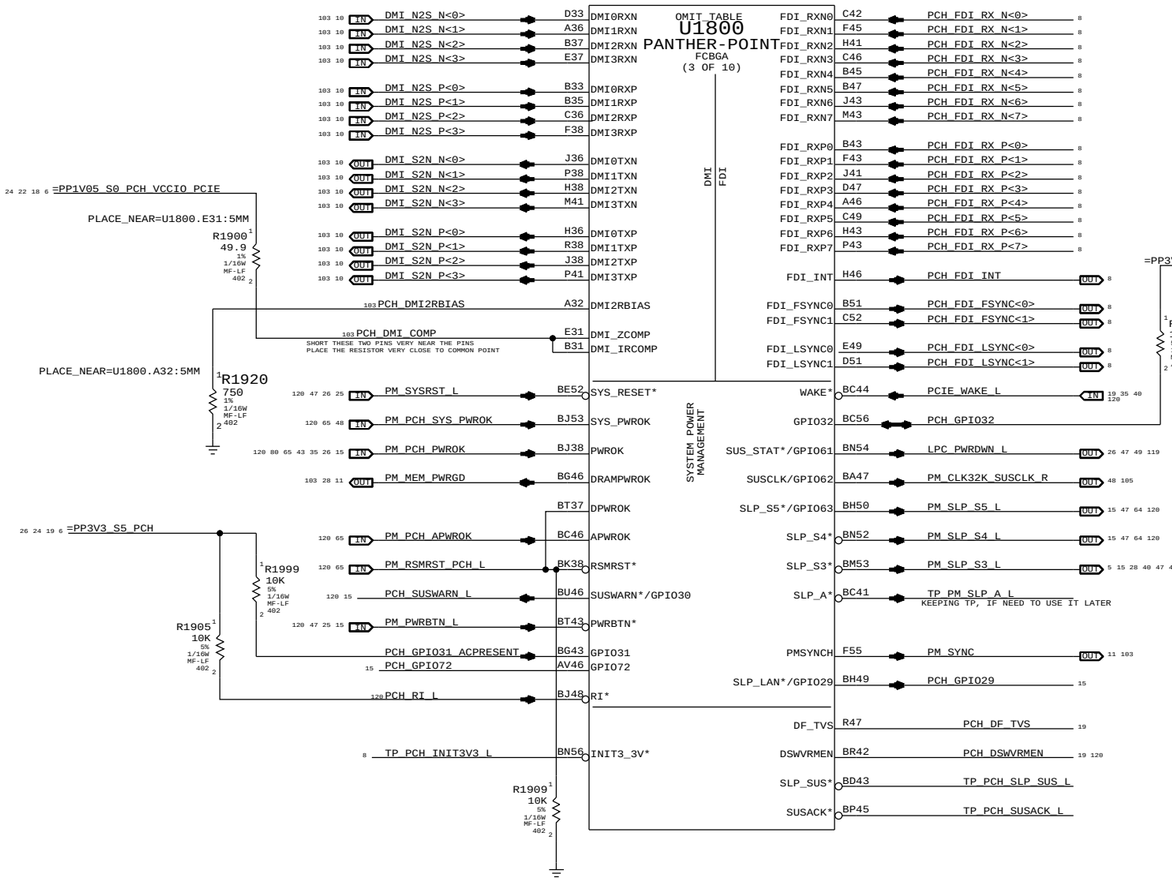

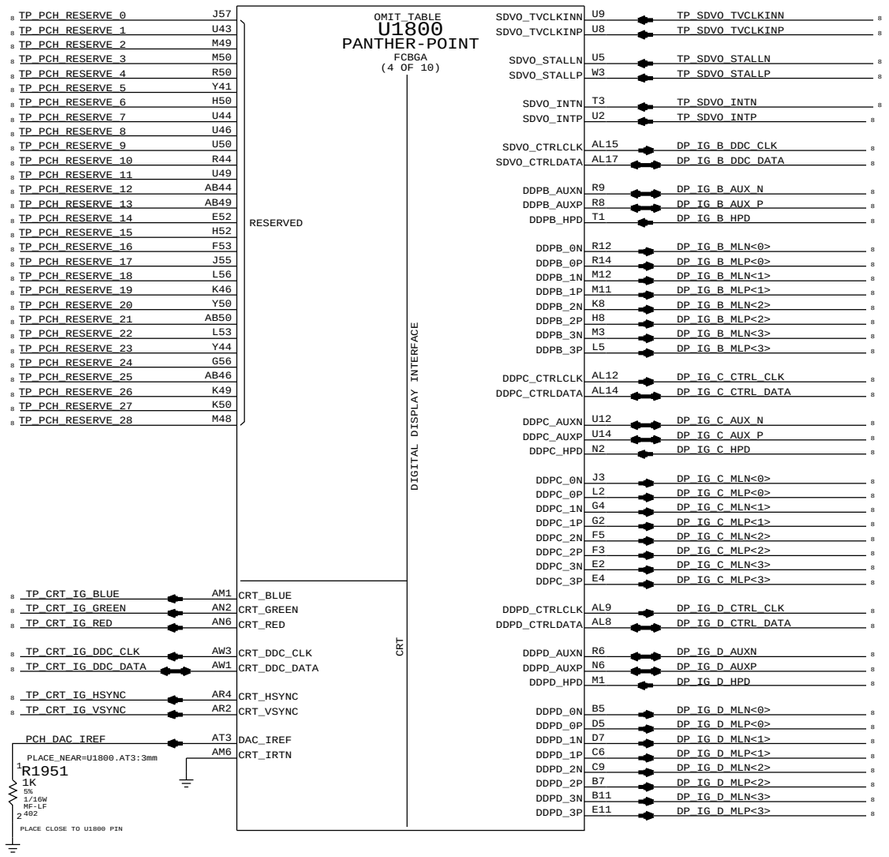

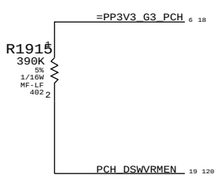

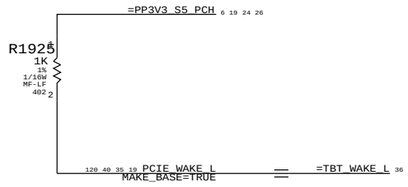

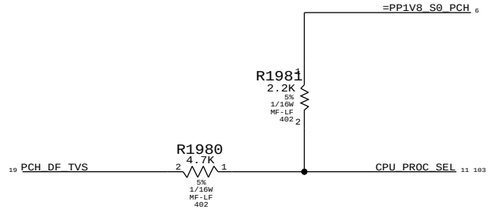

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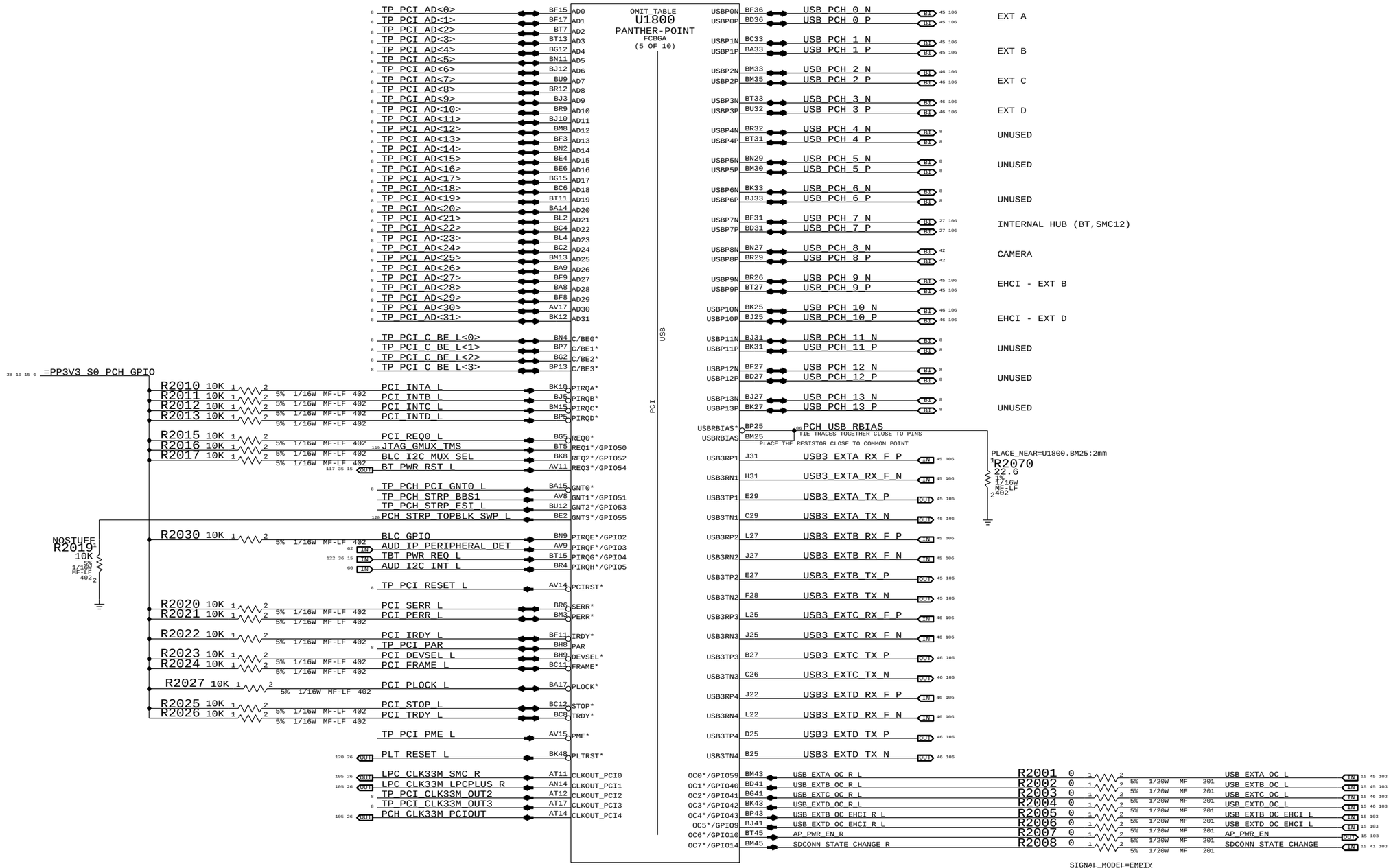

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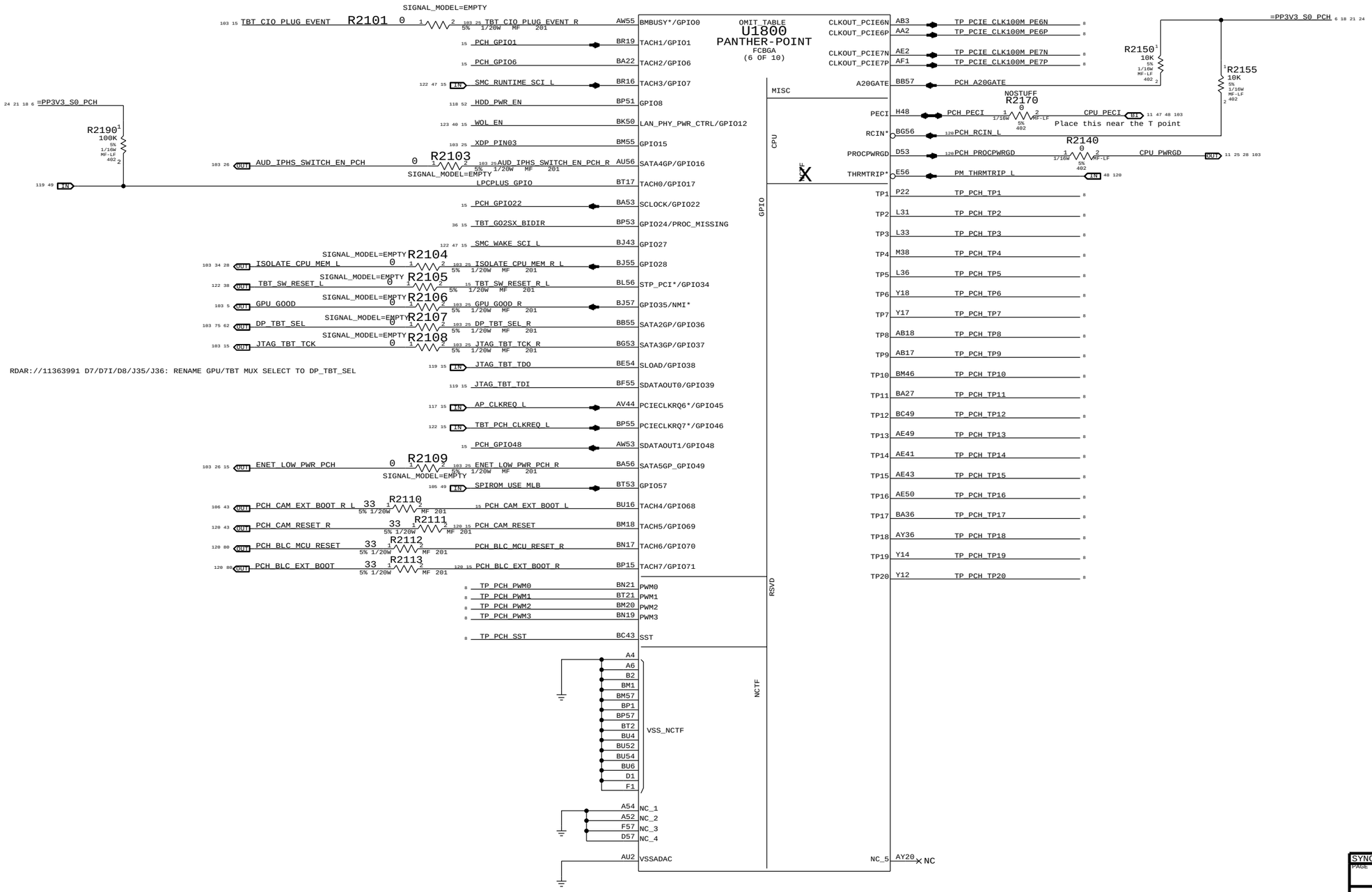

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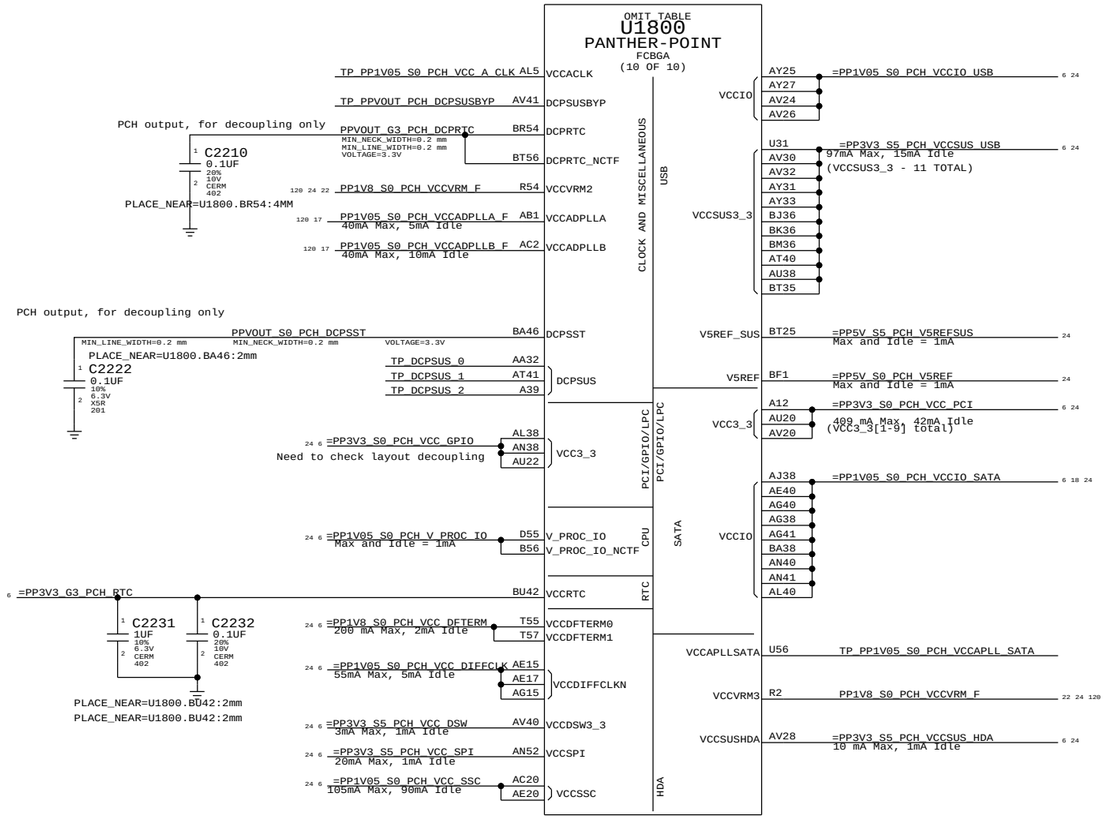

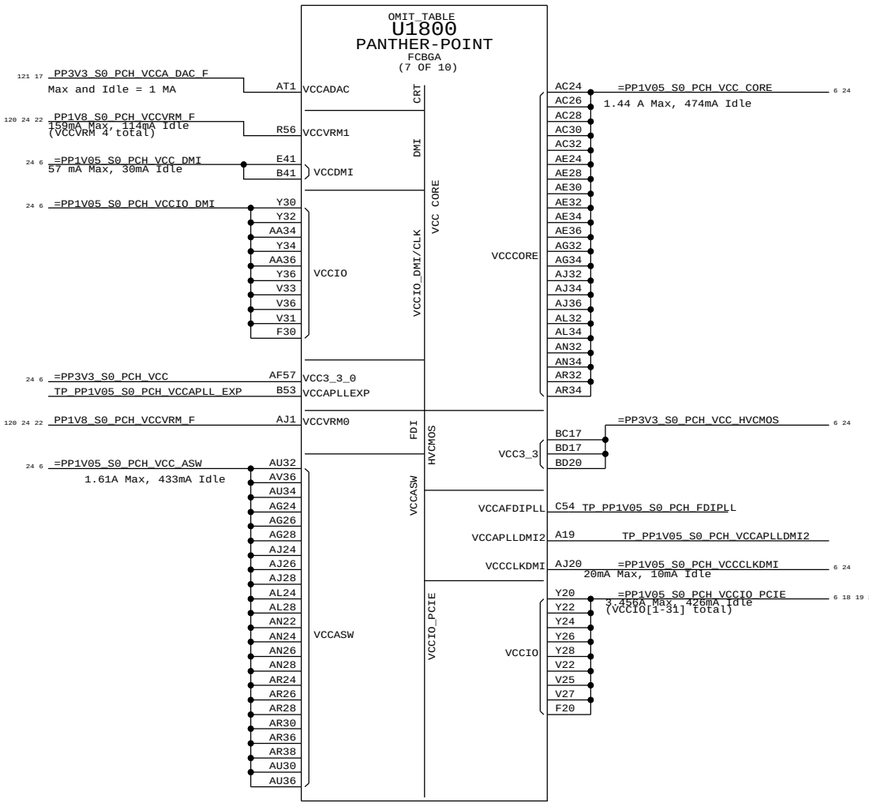

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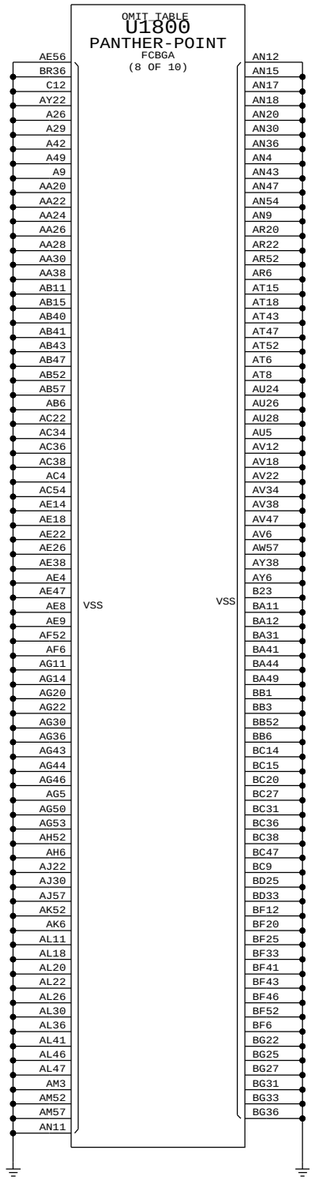

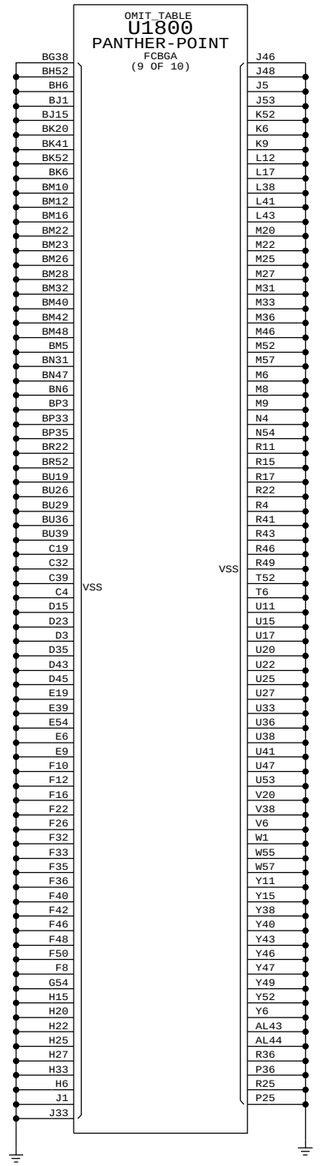

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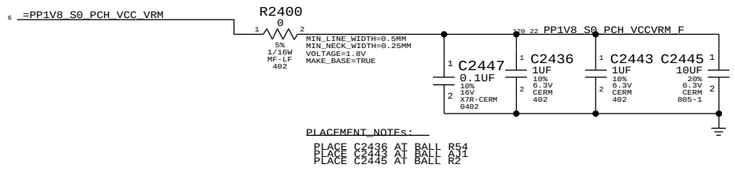

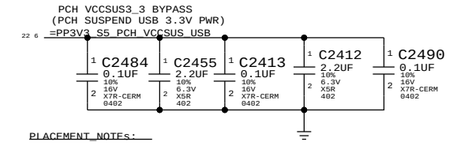

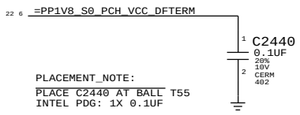

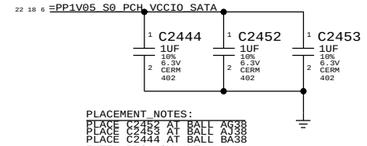

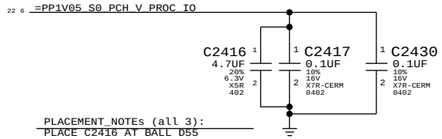

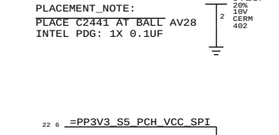

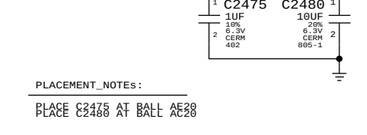

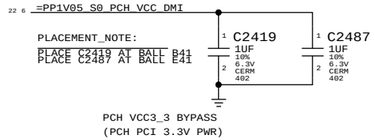

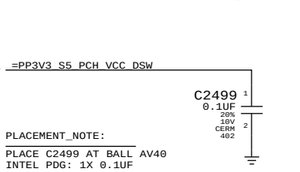

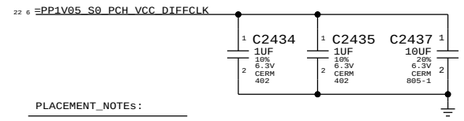

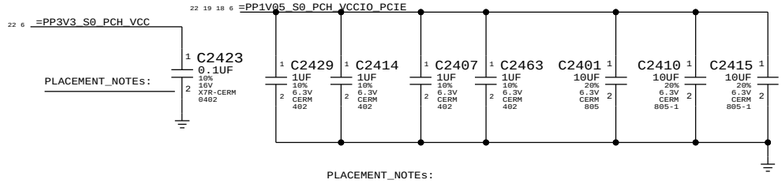

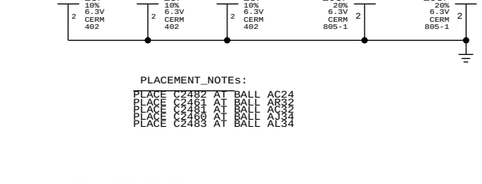

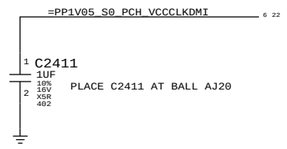

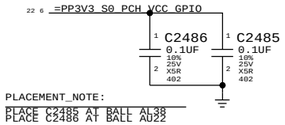

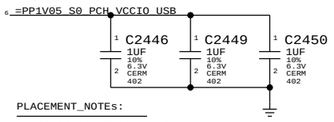

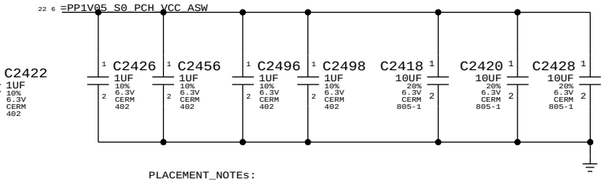

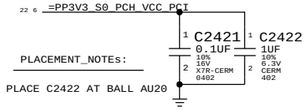

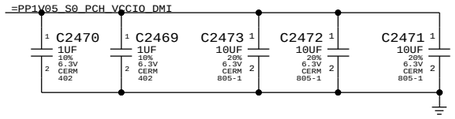

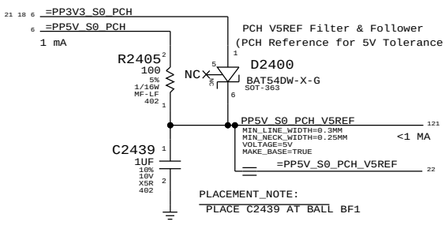

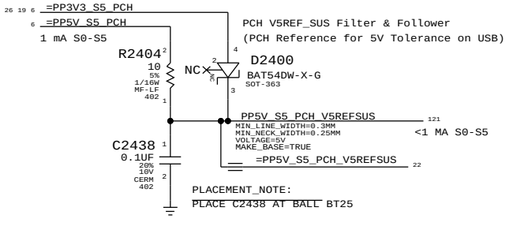

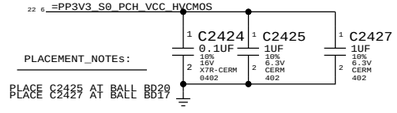

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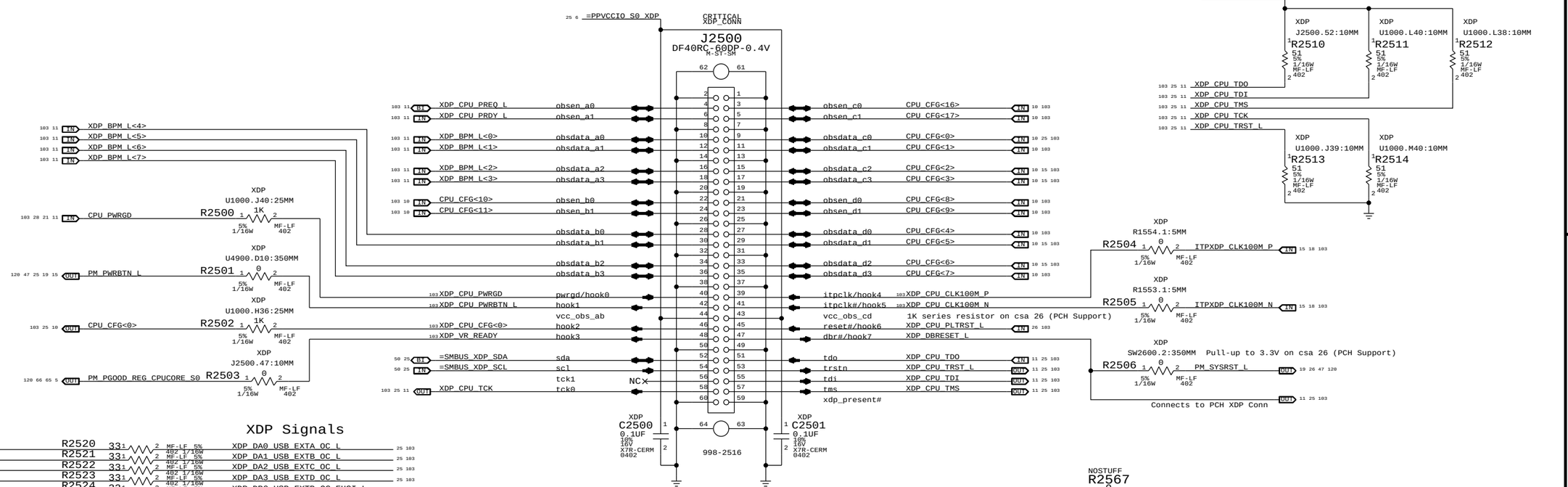
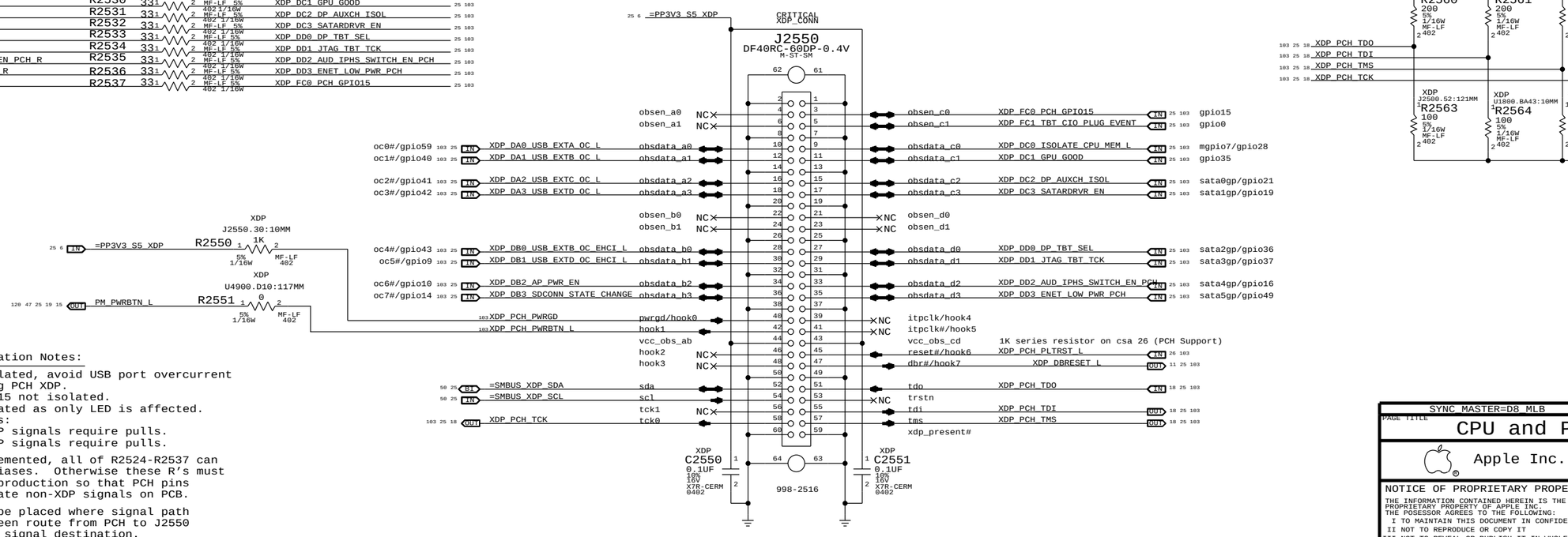
CPU Micro2-XDP



PCH Signals

USB_EXTA_OC_R_L	R2520	33 MF-LF 5% 402 1/16W	XDP_DA0_USB_EXTA_OC_L
USB_EXTB_OC_R_L	R2521	33 MF-LF 5% 402 1/16W	XDP_DA1_USB_EXTB_OC_L
USB_EXTC_OC_R_L	R2522	33 MF-LF 5% 402 1/16W	XDP_DA2_USB_EXTC_OC_L
USB_EXTD_OC_R_L	R2523	33 MF-LF 5% 402 1/16W	XDP_DA3_USB_EXTD_OC_L
USB_EXTB_OC_EHCI_R_L	R2524	33 MF-LF 5% 402 1/16W	XDP_DB0_USB_EXTB_OC_EHCI_L
USB_EXTD_OC_EHCI_R_L	R2525	33 MF-LF 5% 402 1/16W	XDP_DB1_USB_EXTD_OC_EHCI_L
AP_PWR_EN_R	R2526	33 MF-LF 5% 402 1/16W	XDP_DB2_AP_PWR_EN
SDCONN_STATE_CHANGE_R	R2527	33 MF-LF 5% 402 1/16W	XDP_DB3_SDCONN_STATE_CHANGE
TBT_CIO_PLUG_EVENT_R	R2528	33 MF-LF 5% 402 1/16W	XDP_FC1_TBT_CIO_PLUG_EVENT
ISOLATE_CPU_MEM_R_L	R2529	33 MF-LF 5% 402 1/16W	XDP_DC0_ISOLATE_CPU_MEM_L
GPU_GOOD_R	R2530	33 MF-LF 5% 402 1/16W	XDP_DC1_GPU_GOOD
DP_AUXCH_ISOL_R	R2531	33 MF-LF 5% 402 1/16W	XDP_DC2_DP_AUXCH_ISOL
SATARDRVR_EN_R	R2532	33 MF-LF 5% 402 1/16W	XDP_DC3_SATARDRVR_EN
DP_TBT_SEL_R	R2533	33 MF-LF 5% 402 1/16W	XDP_DD0_DP_TBT_SEL
JTAG_TBT_TCK_R	R2534	33 MF-LF 5% 402 1/16W	XDP_DD1_JTAG_TBT_TCK
AUD_IPHS_SWITCH_EN_PCH_R	R2535	33 MF-LF 5% 402 1/16W	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH
ENET_LOW_PWR_PCH_R	R2536	33 MF-LF 5% 402 1/16W	XDP_DD3_ENET_LOW_PWR_PCH
XDP_PIN03	R2537	33 MF-LF 5% 402 1/16W	XDP_FC0_PCH_GPIO15

PCH Micro2-XDP



PCH/XDP Signal Isolation Notes:

- USB OC#'s not isolated, avoid USB port overcurrent events while using PCH XDP.
- Unused GPIOs 0 & 15 not isolated.
- MXM_GOOD not isolated as only LED is affected.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

If PCH XDP not implemented, all of R2524-R2537 can be replaced with aliases. Otherwise these R's must be stuffed even in production so that PCH pins connect to appropriate non-XDP signals on PCB.

R2524-R2537 should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

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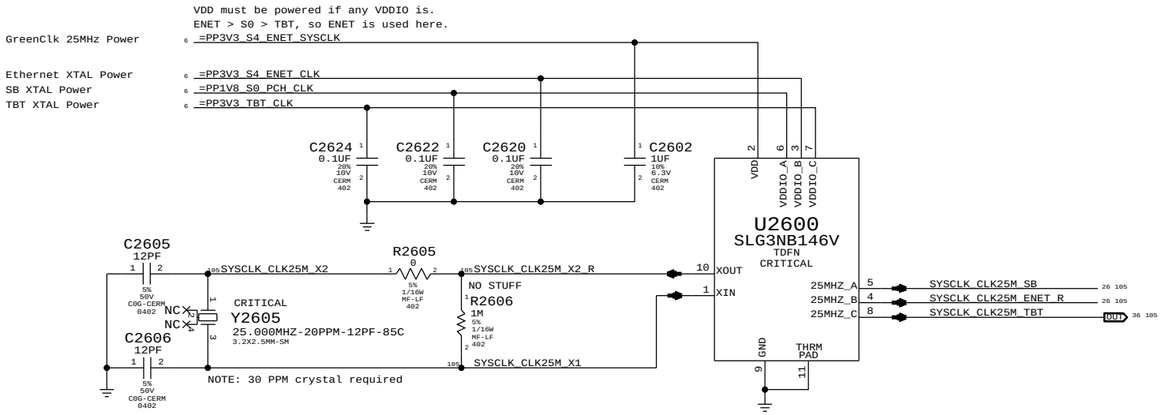
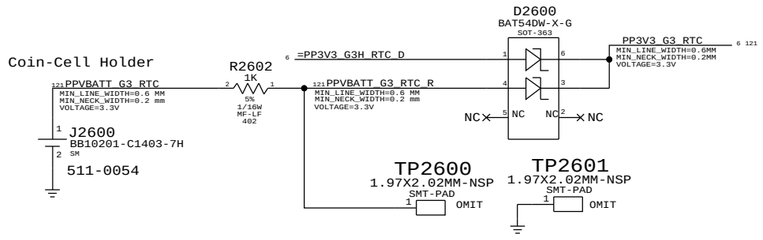
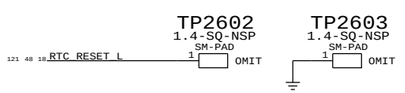
System 25MHz Clock Generator



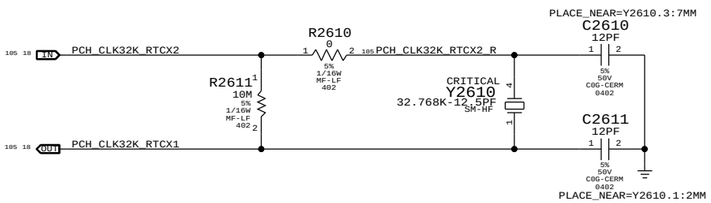
RTC Power Sources



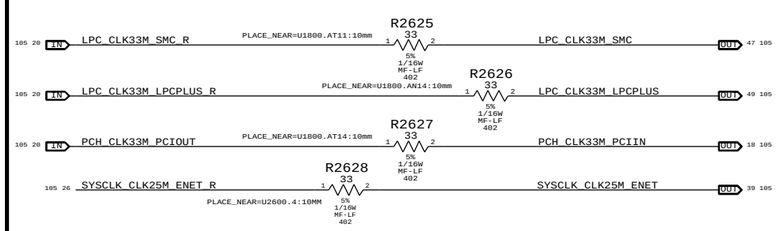
RDAR://11218892 TESTPOINT TO RESET RTC FOR APPLE CARE



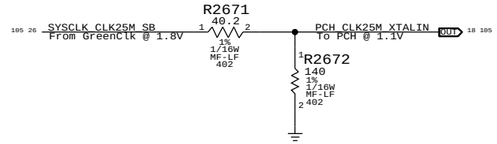
PCH RTC Crystal



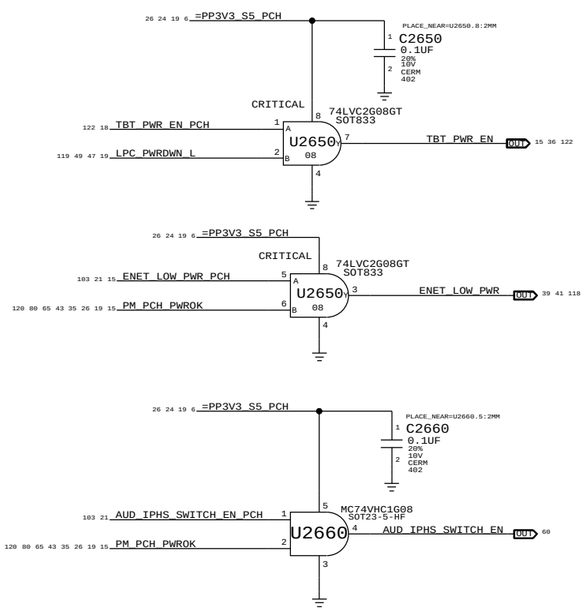
Clock series termination



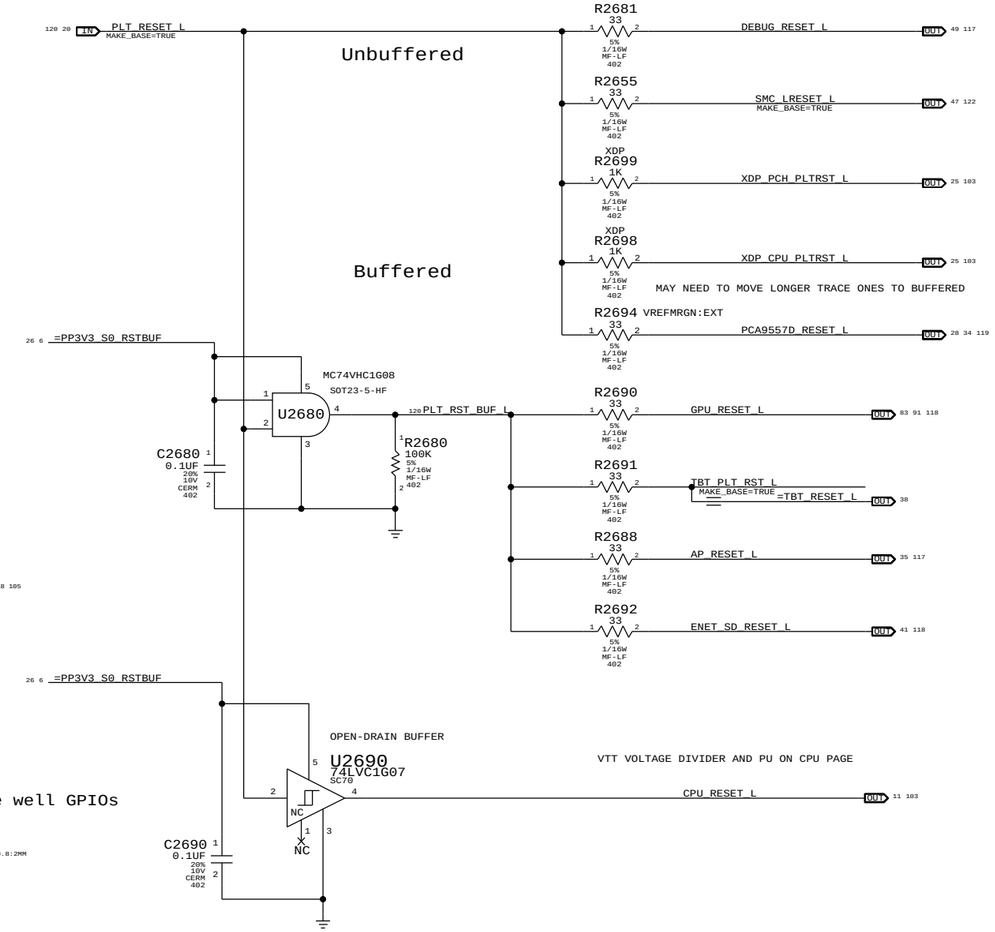
PCH 25MHZ CLOCK



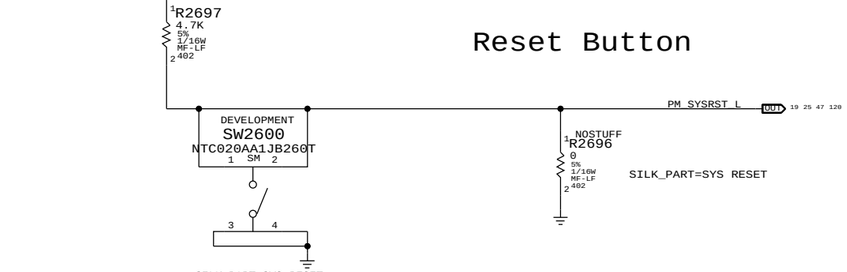
GPIO Isolation to prevent glitches on critical core well GPIOs



Platform Reset Connections



Reset Button



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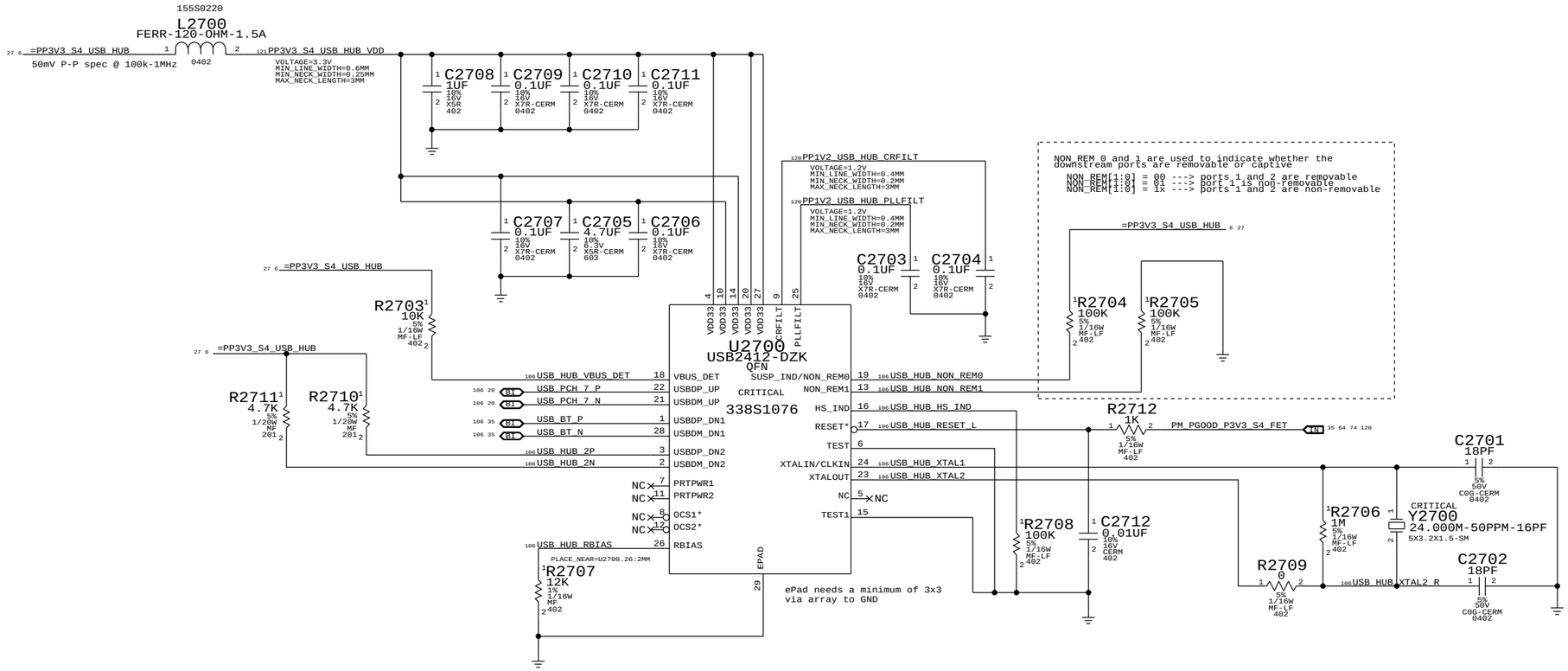

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

USB 2.0 HUB (BT/SMC)

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

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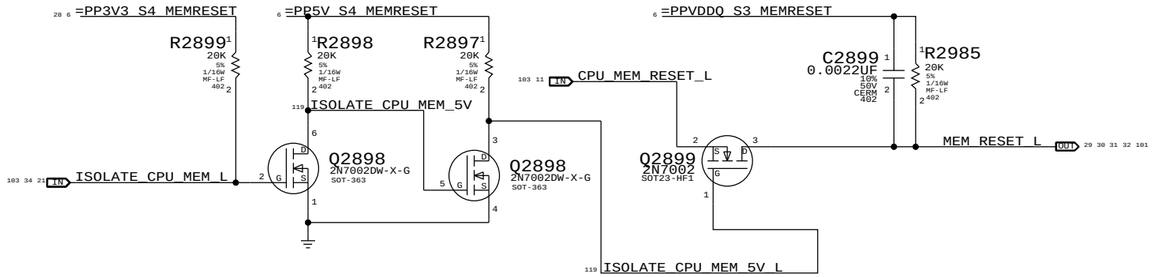
MEM_RESET_L Generator

The circuits below handle MEMVTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behaviour of signals.
WHEN HIGH: MEM_RESET_L NOT ISOLATED.
WHEN LOW: MEM_RESET_L IS ISOLATED.
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L (Block CPU from driving MEM_RESET_L in S3)

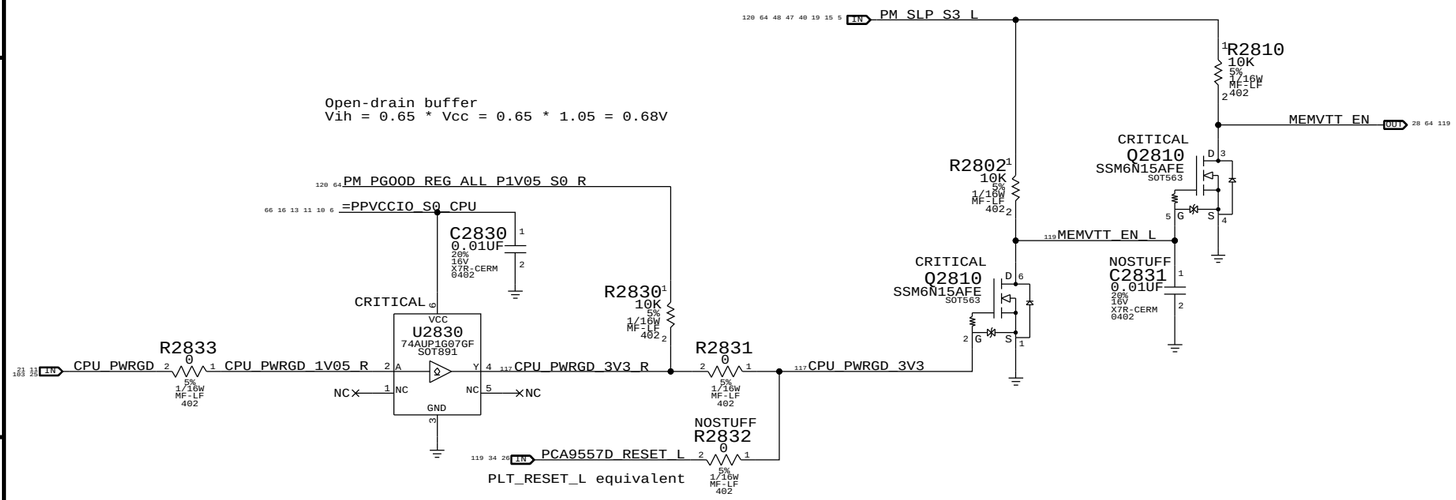


MEMVTT_EN Generator

rdar://11117167

Enables MEMVTT when PCH drives CPU PWRGD.

CPU does not drive MEM_CKE until VCCORE activated but CPU 1V5 (VDDQ) leaks into it.
Clamping MEMVTT will keep the MEM_CKE low until CPU actively controls it.
MEMVTT Clamp actively holds MEMVTT rail low until MEMVTT is enabled.
MEMVTT_EN = CPU_PWRGD * PM_SLP_S3_L (VTT is enabled when PCH tells CPU to enable VCCORE)



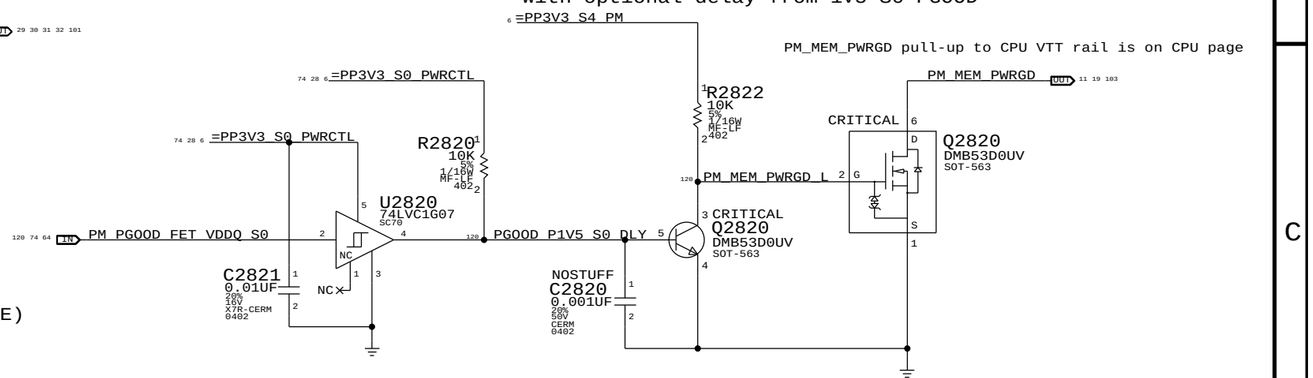
	Step	ISOLATE_CPU_MEM_L	PM_SLP_S3_L	CPU_PWRGD	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1
S3	2	0	1	1	1	1	1
	3	0	0	0	X	1	0
to	4	0	0	0	X	1	0
S0	5	0	1	1	0 (*)	1	1
	6	0	1	1	1	1	1
	7	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: On a S5->S0 transition, ISOLATE_CPU_MEM_L will default low.
Rails will power-up as if from S3, but MEM_RESET_L now needs to be asserted in S0. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

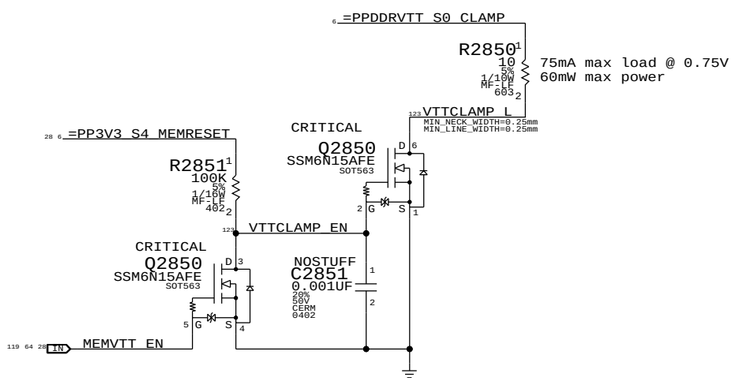
1V5 S0 "PGOOD" for CPU

With optional delay from 1V5 S0 PGOOD



MEMVTT Clamp

Ensures CKE signals are held low in S3 and in S0 before CPU PWRGD



SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	CPU Memory S3 Support
Apple Inc.	DRAWING NUMBER 051-9505 · SIZE D
	REVISION 8.0.0
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

=PPDDRVREF_DQ_MEM_A

C2930 2.2UF 20% 6.3V CERM 402-LF
C2931 0.1UF 20% 10V CERM 402

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_A

C2910 0.1UF 20% 10V CERM 402
C2911 0.1UF 20% 10V CERM 402
C2912 0.1UF 20% 10V CERM 402
C2913 0.1UF 20% 10V CERM 402
C2914 0.1UF 20% 10V CERM 402
C2915 0.1UF 20% 10V CERM 402
C2916 0.1UF 20% 10V CERM 402
C2917 0.1UF 20% 10V CERM 402

C2900 10UF 20% 6.3V X5R 603
C2901 10UF 20% 6.3V X5R 603
C2918 0.1UF 20% 10V CERM 402
C2919 0.1UF 20% 10V CERM 402
C2920 0.1UF 20% 10V CERM 402
C2921 0.1UF 20% 10V CERM 402
C2922 0.1UF 20% 10V CERM 402
C2923 0.1UF 20% 10V CERM 402

MEM_DIMM0_SA<1>
MEM_DIMM0_SA<0>
=PP3V3_S0_MEM_A_SPD

C2940 2.2UF 20% 6.3V CERM 402-LF
R2940 10K 5% 1/16W MF-LF 402
R2941 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_A

J2900 F-ANG-SM-2 SODIMM-P0.60-D8 SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

SODIMM-P0.60-D8 F-ANG-SM-2 SYM 1 OF 2

J2900 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 2 OF 2

205	MTG HOLE
206	
207	
208	
209	

P/N: 516S1030

=PPDDRVREF_CA_MEM_A

C2935 2.2UF 20% 6.3V CERM 402-LF
C2936 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A

C2950 1UF 10% 10V X5R 402
C2951 1UF 10% 10V X5R 402
C2952 1UF 10% 10V X5R 402
C2953 1UF 10% 10V X5R 402

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2013
PAGE TITLE	DDR3 SO-DIMM Connector A Slot0
Apple Inc.	DRAWING NUMBER 051-9505 SIZE D
	REVISION 8.0.0
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

=PPDDRVREF_DQ_MEM_A

C3030 2.2UF 20% 6.3V CERM 402-LF
C3031 0.1UF 20% 10V CERM 402

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_A

C3010 0.1UF 20% 10V CERM 402
C3011 0.1UF 20% 10V CERM 402
C3012 0.1UF 20% 10V CERM 402
C3013 0.1UF 20% 10V CERM 402
C3014 0.1UF 20% 10V CERM 402
C3015 0.1UF 20% 10V CERM 402
C3016 0.1UF 20% 10V CERM 402
C3017 0.1UF 20% 10V CERM 402

C3000 10UF 20% 6.3V X5R 603
C3001 10UF 20% 6.3V X5R 603
C3018 0.1UF 20% 10V CERM 402
C3019 0.1UF 20% 10V CERM 402
C3020 0.1UF 20% 10V CERM 402
C3021 0.1UF 20% 10V CERM 402
C3022 0.1UF 20% 10V CERM 402
C3023 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_A_SPD

R3040 10K 5% 1/16W MF-LF 402
MEM_DIMM1_SA<0>
MEM_DIMM1_SA<1>
=PP3V3_S0_MEM_A_SPD
C3040 2.2UF 20% 6.3V CERM 402-LF
R3041 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_A

J3000
F-ANG-SM-2
SODIMM-P0.60-D8
SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

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MEM_A_DQ<4>, MEM_A_DQ<5>, MEM_A_DQS_N<0>, MEM_A_DQS_P<0>, MEM_A_DQ<6>, MEM_A_DQ<7>, MEM_A_DQ<12>, MEM_A_DQ<13>, MEM_RESET_L, MEM_A_DQ<14>, MEM_A_DQ<15>, MEM_A_DQ<20>, MEM_A_DQ<21>, MEM_A_DQ<22>, MEM_A_DQ<23>, MEM_A_DQ<28>, MEM_A_DQ<29>, MEM_A_DQS_N<3>, MEM_A_DQS_P<3>, MEM_A_DQ<30>, MEM_A_DQ<31>, MEM_A_CKE<3>, MEM_A_A<15>, MEM_A_A<14>, MEM_A_A<11>, MEM_A_A<7>, MEM_A_A<6>, MEM_A_A<4>, MEM_A_A<2>, MEM_A_A<0>, MEM_A_CLK_P<3>, MEM_A_CLK_N<3>, MEM_A_BA<1>, MEM_A_RAS_L, MEM_A_CS_L<2>, MEM_A_ODT<2>, MEM_A_ODT<3>, MEM_A_DQ<36>, MEM_A_DQ<37>, MEM_A_DQ<38>, MEM_A_DQ<39>, MEM_A_DQ<44>, MEM_A_DQ<45>, MEM_A_DQS_N<5>, MEM_A_DQS_P<5>, MEM_A_DQ<46>, MEM_A_DQ<47>, MEM_A_DQ<52>, MEM_A_DQ<53>, MEM_A_DQ<54>, MEM_A_DQ<55>, MEM_A_DQ<60>, MEM_A_DQ<61>, MEM_A_DQS_N<7>, MEM_A_DQS_P<7>, MEM_A_DQ<62>, MEM_A_DQ<63>, MEM_EVENT_L, =I2C_SODIMMA_SDA, =I2C_SODIMMA_SCL

=PPVDDQ_S3_MEM_A

P/N: 516S1030

J3000
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 2 OF 2

205, 206, 207, 208, 209, MTG HOLE

=PPDDRVREF_CA_MEM_A

C3035 2.2UF 20% 6.3V CERM 402-LF
C3036 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_A

C3050 1UF 10% 10V X5R 402
C3051 1UF 10% 10V X5R 402
C3052 1UF 10% 10V X5R 402
C3053 1UF 10% 10V X5R 402

SYNC_MASTER=D8_MLB
SYNC_DATE=08/27/2013

PAGE TITLE
DDR3 SO-DIMM Connector A Slot1

Apple Inc.

DRAWING NUMBER 051-9505
SIZE D
REVISION 8.0.0
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Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

J3100
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 1 OF 2

J3100
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 2 OF 2

1	VREFDQ		2	VSS_0					
3	VSS_1		4	DQ4	=MEM_B_DQ<4>	B1	32	33	
5	DQ0	=MEM_B_DQ<0>	6	DQ5	=MEM_B_DQ<5>	B1	32	33	
7	DQ1	=MEM_B_DQ<1>	8	VSS_2					
9	VSS_3		10	DQS0*	=MEM_B_DQS_N<0>	B1	32	33	
11	DM0		12	DQS0	=MEM_B_DQS_P<0>	B1	32	33	
13	VSS_4		14	VSS_5					
15	DQ2	=MEM_B_DQ<2>	16	DQ6	=MEM_B_DQ<6>	B1	32	33	
17	DQ3	=MEM_B_DQ<3>	18	DQ7	=MEM_B_DQ<7>	B1	32	33	
19	VSS_6		20	VSS_7					
21	DQ8	=MEM_B_DQ<8>	22	DQ12	=MEM_B_DQ<12>	B1	32	33	
23	DQ9	=MEM_B_DQ<9>	24	DQ13	=MEM_B_DQ<13>	B1	32	33	
25	VSS_8		26	VSS_9					
27	DQS1*	=MEM_B_DQS_N<1>	28	DM1					
29	DQS1	=MEM_B_DQS_P<1>	30	RESET*	MEM_RESET_L	IN	28	29	30	32	101
31	VSS_10		32	VSS_11					
33	DQ10	=MEM_B_DQ<10>	34	DQ14	=MEM_B_DQ<14>	B1	32	33	
35	DQ11	=MEM_B_DQ<11>	36	DQ15	=MEM_B_DQ<15>	B1	32	33	
37	VSS_12		38	VSS_13					
39	DQ16	=MEM_B_DQ<16>	40	DQ20	=MEM_B_DQ<20>	B1	32	33	
41	DQ17	=MEM_B_DQ<17>	42	DQ21	=MEM_B_DQ<21>	B1	32	33	
43	VSS_14		44	VSS_15					
45	DQS2*	=MEM_B_DQS_N<2>	46	DM2					
47	DQS2	=MEM_B_DQS_P<2>	48	VSS_16					
49	VSS_17		50	DQ22	=MEM_B_DQ<22>	B1	32	33	
51	DQ18	=MEM_B_DQ<18>	52	DQ23	=MEM_B_DQ<23>	B1	32	33	
53	DQ19	=MEM_B_DQ<19>	54	VSS_18					
55	VSS_19		56	DQ28	=MEM_B_DQ<28>	B1	32	33	
57	DQ24	=MEM_B_DQ<24>	58	DQ29	=MEM_B_DQ<29>	B1	32	33	
59	DQ25	=MEM_B_DQ<25>	60	VSS_20					
61	VSS_21		62	DQS3*	=MEM_B_DQS_N<3>	B1	32	33	
63	DM3		64	DQS3	=MEM_B_DQS_P<3>	B1	32	33	
65	VSS_22		66	VSS_23					
67	DQ26	=MEM_B_DQ<26>	68	DQ30	=MEM_B_DQ<30>	B1	32	33	
69	DQ27	=MEM_B_DQ<27>	70	DQ31	=MEM_B_DQ<31>	B1	32	33	
71	VSS_24		72	VSS_25					
KEY									
73	CKE0	MEM_B_CKE<0> IN 101 12	74	CKE1	MEM_B_CKE<1> IN 12 101
75	VDD_0		76	VDD_1	=PPVDDQ_S3_MEM_B 6 31 32
77	NC_0	NCX	78	A15	MEM_B_A<15> IN 12 32 101
79	BA2	MEM_B_BA<2> IN 101 32 12	80	A14	MEM_B_A<14> IN 12 32 101
81	VDD_2		82	VDD_3	
83	A12/BC*	MEM_B_A<12> IN 101 32 12	84	A11	MEM_B_A<11> IN 12 32 101
85	A9	MEM_B_A<9> IN 101 32 12	86	A7	MEM_B_A<7> IN 12 32 101
87	VDD_4		88	VDD_5	
89	A8	MEM_B_A<8> IN 101 32 12	90	A6	MEM_B_A<6> IN 12 32 101
91	A5	MEM_B_A<5> IN 101 32 12	92	A4	MEM_B_A<4> IN 12 32 101
93	VDD_6		94	VDD_7	
95	A3	MEM_B_A<3> IN 101 32 12	96	A2	MEM_B_A<2> IN 12 32 101
97	A1	MEM_B_A<1> IN 101 32 12	98	A0	MEM_B_A<0> IN 12 32 101
99	VDD_8		100	VDD_9	
101	CK0	MEM_B_CLK_P<0> IN 101 12	102	CK1	MEM_B_CLK_P<1> IN 12 101
103	CK0*	MEM_B_CLK_N<0> IN 101 12	104	CK1*	MEM_B_CLK_N<1> IN 12 101
105	VDD_10		106	VDD_11	
107	A10_AP	MEM_B_A<10> IN 101 32 12	108	BA1	MEM_B_BA<1> IN 12 32 101
109	BA0	MEM_B_BA<0> IN 101 32 12	110	RAS*	MEM_B_RAS_L IN 12 32 101
111	VDD_12		112	VDD_13	
113	WE*	MEM_B_WE_L IN 101 32 12	114	S0*	MEM_B_CS_L<0> IN 12 101
115	CAS*	MEM_B_CAS_L IN 101 32 12	116	ODT0	MEM_B_ODT<0> IN 12 101
117	VDD_14		118	VDD_15	
119	A13	MEM_B_A<13> IN 101 32 12	120	ODT1	MEM_B_ODT<1> IN 12 101
121	S1*	MEM_B_CS_L<1> IN 101 12	122	NC_1	NCX
123	VDD_16		124	VDD_17	
125	TEST	NCX	126	VREFCA	=PPDDRVREF_CA_MEM_B 6 32
127	VSS_26		128	VSS_27	
129	DQ32	=MEM_B_DQ<32>	130	DQ36	=MEM_B_DQ<36>	B1	32	33	
131	DQ33	=MEM_B_DQ<33>	132	DQ37	=MEM_B_DQ<37>	B1	32	33	
133	VSS_28		134	VSS_29					
135	DQS4*	=MEM_B_DQS_N<4>	136	DM4					
137	DQS4	=MEM_B_DQS_P<4>	138	VSS_30					
139	VSS_31		140	DQ38	=MEM_B_DQ<38>	B1	32	33	
141	DQ34	=MEM_B_DQ<34>	142	DQ39	=MEM_B_DQ<39>	B1	32	33	
143	DQ35	=MEM_B_DQ<35>	144	VSS_32					
145	VSS_33		146	DQ44	=MEM_B_DQ<44>	B1	32	33	
147	DQ40	=MEM_B_DQ<40>	148	DQ45	=MEM_B_DQ<45>	B1	32	33	
149	DQ41	=MEM_B_DQ<41>	150	VSS_34					
151	VSS_35		152	DQS5*	=MEM_B_DQS_N<5>	B1	32	33	
153	DM5		154	DQS5	=MEM_B_DQS_P<5>	B1	32	33	
155	VSS_36		156	VSS_37					
157	DQ42	=MEM_B_DQ<42>	158	DQ46	=MEM_B_DQ<46>	B1	32	33	
159	DQ43	=MEM_B_DQ<43>	160	DQ47	=MEM_B_DQ<47>	B1	32	33	
161	VSS_38		162	VSS_39					
163	DQ48	=MEM_B_DQ<48>	164	DQ52	=MEM_B_DQ<52>	B1	32	33	
165	DQ49	=MEM_B_DQ<49>	166	DQ53	=MEM_B_DQ<53>	B1	32	33	
167	VSS_40		168	VSS_41					
169	DQS6*	=MEM_B_DQS_N<6>	170	DM6					
171	DQS6	=MEM_B_DQS_P<6>	172	VSS_42					
173	VSS_43		174	DQ54	=MEM_B_DQ<54>	B1	32	33	
175	DQ50	=MEM_B_DQ<50>	176	DQ55	=MEM_B_DQ<55>	B1	32	33	
177	DQ51	=MEM_B_DQ<51>	178	VSS_44					
179	VSS_45		180	DQ60	=MEM_B_DQ<60>	B1	32	33	
181	DQ56	=MEM_B_DQ<56>	182	DQ61	=MEM_B_DQ<61>	B1	32	33	
183	DQ57	=MEM_B_DQ<57>	184	VSS_46					
185	VSS_47		186	DQS7*	=MEM_B_DQS_N<7>	B1	32	33	
187	DM7		188	DQS7	=MEM_B_DQS_P<7>	B1	32	33	
189	VSS_48		190	VSS_49					
191	DQ58	=MEM_B_DQ<58>	192	DQ62	=MEM_B_DQ<62>	B1	32	33	
193	DQ59	=MEM_B_DQ<59>	194	DQ63	=MEM_B_DQ<63>	B1	32	33	
195	VSS_50		196	VSS_51					
197	SA0	MEM_DIMM2_SA<0> 31	198	EVENT*	MEM_EVENT_L OUT 29 30 32 47 48 119
199	VDDSPD	=PP3V3_S0_MEM_B_SPD 32 31 6	200	SDA	=I2C_SODIMMB_SDA B1 32 50
201	SA1	MEM_DIMM2_SA<1> 31	202	SCL	=I2C_SODIMMB_SCL IN 32 50
203	VTT_0		204	VTT_1	

205	MTG_HOLE	
206	MTG_HOLE	
207	MTG_HOLE	
208	MTG_HOLE	
209	MTG_HOLE	

=PPDDRVREF_DQ_MEM_B 32 6

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

C3110 C3111 C3112 C3113 C3114 C3115 C3116 C3117 0.1UF 20% 10V CERM 402

C3100 C3101 10UF 20% 6.3V X5R 603

C3118 C3119 C3120 C3121 C3122 C3123 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD 32 31 6

R3141 10K 5% 1/16W MF-LF 402
MEM_DIMM2_SA<1> 31
MEM_DIMM2_SA<0> 31

=PP3V3_S0_MEM_B_SPD 32 31 6

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402

=PPDDRVTT_S0_MEM_B 32 31 6

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

=PPDDRVREF_CA_MEM_B 6 32

C3150 C3151 C3152 C3153 1UF 10% 10V X5R 402

=PPDDRVTT_S0_MEM_B 6 31 32

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: DDR3 SO-DIMM CONNECTOR B SLOT0

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D
REVISION: 8.0.0
BRANCH: prefsb
PAGE: 31 OF 144
SHEET: 31 OF 123

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

=PPDDRVREF_DQ_MEM_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X6S 603
C3201 10UF 20% 6.3V X6S 603
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD

R3241 10K 5% 1/16W MF-LF 402
R3240 10K 5% 1/16W MF-LF 402

MEM_DIMM3_SA<1>
MEM_DIMM3_SA<0>

=PP3V3_S0_MEM_B_SPD

C3240 2.2UF 20% 6.3V CERM 402-LF

=PPDDRVTT_S0_MEM_B

J3200 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 1 OF 2

1	VREFDQ	VSS_0	2
3	VSS_1	DQ4	4
5	DQ0	DQ5	6
7	DQ1	VSS_2	8
9	VSS_3	DQS0*	10
11	DM0	DQS0	12
13	VSS_4	VSS_5	14
15	DQ2	DQ6	16
17	DQ3	DQ7	18
19	VSS_6	VSS_7	20
21	DQ8	DQ12	22
23	DQ9	DQ13	24
25	VSS_8	VSS_9	26
27	DQS1*	DM1	28
29	DQS1	RESET*	30
31	VSS_10	VSS_11	32
33	DQ10	DQ14	34
35	DQ11	DQ15	36
37	VSS_12	VSS_13	38
39	DQ16	DQ20	40
41	DQ17	DQ21	42
43	VSS_14	VSS_15	44
45	DQS2*	DM2	46
47	DQS2	VSS_16	48
49	VSS_17	DQ22	50
51	DQ18	DQ23	52
53	DQ19	VSS_18	54
55	VSS_19	DQ28	56
57	DQ24	DQ29	58
59	DQ25	VSS_20	60
61	VSS_21	DQS3*	62
63	DM3	DQS3	64
65	VSS_22	VSS_23	66
67	DQ26	DQ30	68
69	DQ27	DQ31	70
71	VSS_24	VSS_25	72
KEY			
73	CKE0	CKE1	74
75	VDD_0	VDD_1	76
77	NC_0	A15	78
79	BA2	A14	80
81	VDD_2	VDD_3	82
83	A12/BC*	A11	84
85	A9	A7	86
87	VDD_4	VDD_5	88
89	A8	A6	90
91	A5	A4	92
93	VDD_6	VDD_7	94
95	A3	A2	96
97	A1	A0	98
99	VDD_8	VDD_9	100
101	CK0	CK1	102
103	CK0*	CK1*	104
105	VDD_10	VDD_11	106
107	A10_AP	BA1	108
109	BA0	RAS*	110
111	VDD_12	VDD_13	112
113	WE*	S0*	114
115	CAS*	ODT0	116
117	VDD_14	VDD_15	118
119	A13	ODT1	120
121	S1*	NC_1	122
123	VDD_16	VDD_17	124
125	TEST	VREFCA	126
127	VSS_26	VSS_27	128
129	DQ32	DQ36	130
131	DQ33	DQ37	132
133	VSS_28	VSS_29	134
135	DQS4*	DM4	136
137	DQS4	VSS_30	138
139	VSS_31	DQ38	140
141	DQ34	DQ39	142
143	DQ35	VSS_32	144
145	VSS_33	DQ44	146
147	DQ40	DQ45	148
149	DQ41	VSS_34	150
151	VSS_35	DQS5*	152
153	DM5	DQS5	154
155	VSS_36	VSS_37	156
157	DQ42	DQ46	158
159	DQ43	DQ47	160
161	VSS_38	VSS_39	162
163	DQ48	DQ52	164
165	DQ49	DQ53	166
167	VSS_40	VSS_41	168
169	DQS6*	DM6	170
171	DQS6	VSS_42	172
173	VSS_43	DQ54	174
175	DQ50	DQ55	176
177	DQ51	VSS_44	178
179	VSS_45	DQ60	180
181	DQ56	DQ61	182
183	DQ57	VSS_46	184
185	VSS_47	DQS7*	186
187	DM7	DQS7	188
189	VSS_48	VSS_49	190
191	DQ58	DQ62	192
193	DQ59	DQ63	194
195	VSS_50	VSS_51	196
197	SA0	EVENT*	198
199	VDDSPD	SDA	200
201	SA1	SCL	202
203	VTT_0	VTT_1	204

SODIMM-P0.60-D8 SYM 1 OF 2

J3200 SODIMM-P0.60-D8 F-ANG-SM-2 SYM 2 OF 2

205	MTG HOLE
206	
207	
208	
209	

=PPDDRVREF_CA_MEM_B

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_B

C3250 1UF 10% 10V X5R 402
C3251 1UF 10% 10V X5R 402
C3252 1UF 10% 10V X5R 402
C3253 1UF 10% 10V X5R 402

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	DDR3 SO-DIMM CONNECTOR B SLOT1
Apple Inc.	DRAWING NUMBER 051-9505 SIZE D
	REVISION 8.0.0
	BRANCH prefsb
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MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	
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MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	
MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	
MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	
MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	
MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	
MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	
MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	

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PAGE TITLE

DDR3 ALIASES AND BITSWAPS

Apple Inc.

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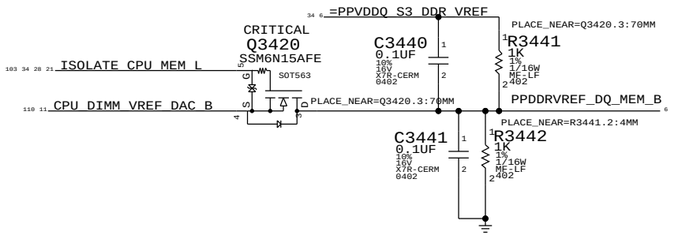
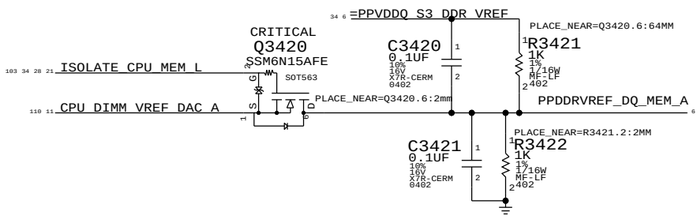
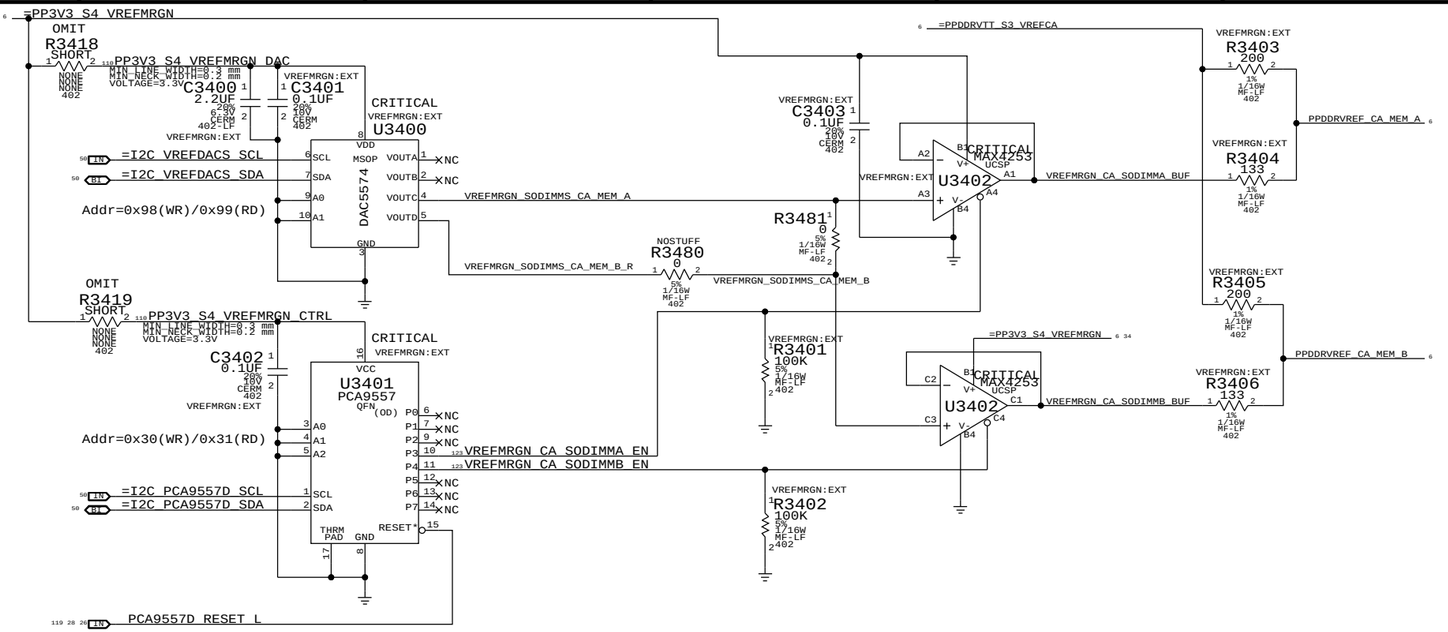
VRef DQ

Driven by CPU

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step







RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FLM,0,5%,402,SM,LF	R3403,R3405		VREFMRGN:N

	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	C	C	D	D
PCA9557D Pin:	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)		1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)		0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)		+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

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PAGE TITLE
DDR3/FRAMEBUF VREF MARGINING

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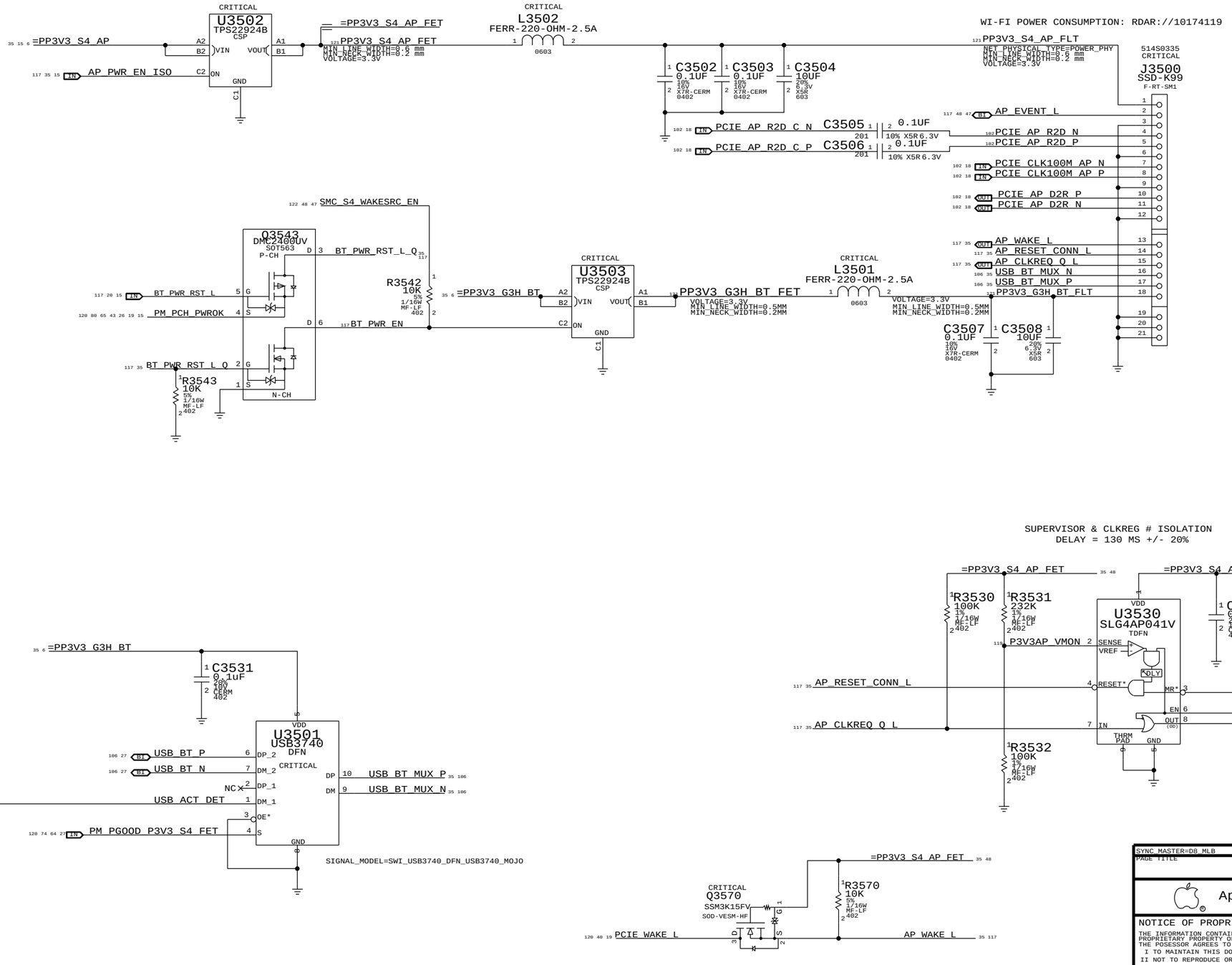
AIRPORT BLUETOOTH



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CRITICAL
OMIT_TABLE
U3600
CACTUSRIDGE4C
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE
PERP_0 / PERN_0
PERP_1 / PERN_1
PERP_2 / PERN_2
PERP_3 / PERN_3

TRANSMIT
PETP_0 / PETN_0
PETP_1 / PETN_1
PETP_2 / PETN_2
PETP_3 / PETN_3

PCIE_TBT_R2D_C_N<0> C3600 0.1UF PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_C_P<0> C3601 0.1UF PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_C_N<1> C3602 0.1UF PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_C_P<1> C3603 0.1UF PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_C_N<2> C3604 0.1UF PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_C_P<2> C3605 0.1UF PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_C_P<3> C3606 0.1UF PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_C_N<3> C3607 0.1UF PCIE_TBT_R2D_N<3>

PCIE_TBT_D2R_C_N<0> C3640 0.1UF PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_C_P<0> C3641 0.1UF PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_C_N<1> C3642 0.1UF PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_C_P<1> C3643 0.1UF PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_C_P<2> C3644 0.1UF PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_C_N<2> C3645 0.1UF PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_C_N<3> C3646 0.1UF PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_C_P<3> C3647 0.1UF PCIE_TBT_D2R_P<3>

=PP3V3_S4_TBT
R3610 47K 5% 1/16W MF-LF 402

TBT_PCIE_RESET_L → PERST_N
TBT_PWR_ON_POC_RST_L → PWR_ON_POC_RSTN

NO STUFF
C3610 0.1UF 10% 16V X5R 402

MISC

MONDC0 / MONDC1
TP_TBT_MONDC0 AD23
TP_TBT_MONDC1 AC24

OMIT
R3615 NOSTUFF NONE 402
DEBUG: For monitoring current/voltage
TBT_MONOBSP W18
TBT_MONOBSN W16
MONOBS_P / MONOBS_N

DEBUG: For monitoring clock
TP_TBT_THERM_DP Y7
Use AA8 GND ball for THERM_DN
THERMDA

=PP3V3_TBTLC_RTR
R3690 3.3K 5% 1/16W MF-LF 402
R3691 3.3K 5% 1/16W MF-LF 402
C3690 1UF 10% 6.3V CERM 402
R3692 3.3K 5% 1/16W MF-LF 402
R3693 3.3K 5% 1/16W MF-LF 402
CRITICAL
OMIT_TABLE
VCC
U3690 M95256-RMC6XG MLP
(TBT_SPI_MOSI) D
(TBT_SPI_CLK) C
(TBT_SPI_CS_L) S*
TBTROM_WP_L W*
TBTROM_HOLD_L HOLD*
(TBT_SPI_MISO) Q
VSS
THM PAD

EEPROM
EE_DI / EE_DO / EE_CS_N / EE_CLK
TBT_SPI_MOSI R4
TBT_SPI_MISO P5
TBT_SPI_CS_L AD3
TBT_SPI_CLK W4

JTAG/TEST PORT
TDI / TMS / TCK / TDO / TEST_EN / TEST_PWR_GOOD
JTAG_TBT_TDI_ISOL V1
JTAG_TBT_TMS_ISOL AB3
JTAG_TBT_TCK_ISOL AA6
JTAG_TBT_TDO_ISOL R2
TBT_TEST_EN N4
TBT_TEST_PWR_GOOD AB5

R3625 0 5% 1/16W MF-LF 402
R3629 0 5% 1/16W MF-LF 402

SINK PORT 0
DPSNK0_3_P / DPSNK0_3_N
DPSNK0_2_P / DPSNK0_2_N
DPSNK0_1_P / DPSNK0_1_N
DPSNK0_0_P / DPSNK0_0_N
DPSNK0_AUX_P / DPSNK0_AUX_N
DPSNK0_HPD
DP_TBTSNK0_ML_P<3> E14
DP_TBTSNK0_ML_N<3> D13
DP_TBTSNK0_ML_P<2> E16
DP_TBTSNK0_ML_N<2> D15
DP_TBTSNK0_ML_P<1> E18
DP_TBTSNK0_ML_N<1> D17
DP_TBTSNK0_ML_P<0> E20
DP_TBTSNK0_ML_N<0> D19
DP_TBTSNK0_AUXCH_P A6
DP_TBTSNK0_AUXCH_N B5
DP_TBTSNK0_HPD U6

SINK PORT 1
DPSNK1_3_P / DPSNK1_3_N
DPSNK1_2_P / DPSNK1_2_N
DPSNK1_1_P / DPSNK1_1_N
DPSNK1_0_P / DPSNK1_0_N
DPSNK1_AUX_P / DPSNK1_AUX_N
DPSNK1_HPD
DP_TBTSNK1_ML_P<3> E6
DP_TBTSNK1_ML_N<3> D5
DP_TBTSNK1_ML_P<2> E8
DP_TBTSNK1_ML_N<2> D7
DP_TBTSNK1_ML_P<1> E10
DP_TBTSNK1_ML_N<1> D9
DP_TBTSNK1_ML_P<0> E12
DP_TBTSNK1_ML_N<0> D11
DP_TBTSNK1_AUXCH_P A4
DP_TBTSNK1_AUXCH_N B3
DP_TBTSNK1_HPD T5

R3630 100K 5% 1/16W MF-LF 402
R3631 100K 5% 1/16W MF-LF 402

DISPLAYPORT

SOURCE PORT 0
DPSRC_3_P / DPSRC_3_N
DPSRC_2_P / DPSRC_2_N
DPSRC_1_P / DPSRC_1_N
DPSRC_0_P / DPSRC_0_N
DPSRC_AUX_P / DPSRC_AUX_N
DPSRC_HPD_OD
TP_DP_TBTSRC_ML_CP<3> A14
TP_DP_TBTSRC_ML_CN<3> B15
TP_DP_TBTSRC_ML_CP<2> A12
TP_DP_TBTSRC_ML_CN<2> B13
TP_DP_TBTSRC_ML_CP<1> A10
TP_DP_TBTSRC_ML_CN<1> B11
TP_DP_TBTSRC_ML_CP<0> A8
TP_DP_TBTSRC_ML_CN<0> B9
TP_DP_TBTSRC_AUXCH_CP C2
TP_DP_TBTSRC_AUXCH_CN D3
DP_TBTSRC_HPD V3

R3632 100K 5% 1/16W MF-LF 402

GPIO_2/GO2SX TBT_GO2SX_BIDIR Y1
(FORCE_PWR) GPIO_3 TBT_PWR_EN W2
GPIO_4/WAKE_N_OD =TBT_WAKE_L J4
GPIO_5/CIO_PLUG_EVENT TBT_CIO_PLUG_EVENT_ISOL AA2
GPIO_6/CIO_SDA_OD I2C_TBTRTR_SDA AB1
GPIO_7/CIO_SCL_OD I2C_TBTRTR_SCL AC2
GPIO_8/EN_CIO_PWR_OD* (TBT_EN_CIO_PWR_L) P3
GPIO_9/OK2GO2SX_OD* TBT_GPIO_9 M5
GPIO_14 TBT_GPIO_14 T3
GPIO_15 TBT_DDC_XBAR_EN_L V5

TBT_PWR_REQ_L
TBT_EN_CIO_PWR_L
MAKE_BASE=TRUE

PORT0
PA_CIO0_TX_P/DP_SRC_0_P / PA_CIO0_TX_N/DP_SRC_0_N
PA_CIO0_RX_P / PA_CIO0_RX_N
PA_CONFIG1/CIO_0_LSEO
PA_CONFIG2/CIO_0_LSOE
TBT_A_R2D_C_P<0> G24
TBT_A_R2D_C_N<0> E24
TBT_A_D2R_P<0> G22
TBT_A_D2R_N<0> E22
TBT_A_CONFIG1_BUF K1
TBT_A_CONFIG2_RC G4

PORT1
PA_CIO1_TX_P/DP_SRC_2_P / PA_CIO1_TX_N/DP_SRC_2_N
PA_CIO1_RX_P / PA_CIO1_RX_N
PA_LSTX/CIO_1_LSEO
PA_LSRX/CIO_1_LSOE
TBT_A_R2D_C_P<1> L24
TBT_A_R2D_C_N<1> J24
TBT_A_D2R_P<1> L22
TBT_A_D2R_N<1> J22
TBT_A_LSTX N2
TBT_A_LSRX J6

PORT2
PB_CIO2_TX_P/DP_SRC_0_P / PB_CIO2_TX_N/DP_SRC_0_N
PB_CIO2_RX_P / PB_CIO2_RX_N
PB_CONFIG1/CIO_2_LSEO
PB_CONFIG2/CIO_2_LSOE
TBT_B_R2D_C_P<0> R24
TBT_B_R2D_C_N<0> N24
TBT_B_D2R_P<0> R22
TBT_B_D2R_N<0> N22
TBT_B_CONFIG1_BUF P1
TBT_B_CONFIG2_RC H5

PORT3
PB_CIO3_TX_P/DP_SRC_2_P / PB_CIO3_TX_N/DP_SRC_2_N
PB_CIO3_RX_P / PB_CIO3_RX_N
PB_LSTX/CIO_3_LSEO
PB_LSRX/CIO_3_LSOE
TBT_B_R2D_C_P<1> W24
TBT_B_R2D_C_N<1> U24
TBT_B_D2R_P<1> W22
TBT_B_D2R_N<1> U22
TBT_B_LSTX L6
TBT_B_LSRX G6

PORTS

PA_DPSRC_1_P / PA_DPSRC_1_N
PA_DPSRC_3_P / PA_DPSRC_3_N
DP_TBTPA_ML_C_P<1> A16
DP_TBTPA_ML_C_N<1> B17
DP_TBTPA_ML_C_P<3> A18
DP_TBTPA_ML_C_N<3> B19
PA_AUX_P / PA_AUX_N
DP_TBTPA_AUXCH_C_P F3
DP_TBTPA_AUXCH_C_N F1
PA_DPSRC_HPD
DP_TBTPA_HPD H1
GPIO_0/PA_HV_EN/BYP0
GPIO_10/PA_CIO_SEL/BYP1
GPIO_12/PA_DP_PWRDN/BYP2
TBT_A_HV_EN G2
TBT_A_CIO_SEL M3
TBT_A_DP_PWRDN H3

PB_DPSRC_1_P / PB_DPSRC_1_N
PB_DPSRC_3_P / PB_DPSRC_3_N
DP_TBTPB_ML_C_P<1> A20
DP_TBTPB_ML_C_N<1> B21
DP_TBTPB_ML_C_P<3> A22
DP_TBTPB_ML_C_N<3> B23
PB_AUX_P / PB_AUX_N
DP_TBTPB_AUXCH_C_P D1
DP_TBTPB_AUXCH_C_N E2
PB_DPSRC_HPD
DP_TBTPB_HPD K3
GPIO_1/PB_HV_EN/BYP0
GPIO_11/PB_CIO_SEL/BYP1
GPIO_13/PB_DP_PWRDN/BYP2
TBT_B_HV_EN M1
TBT_B_CIO_SEL L2
TBT_B_DP_PWRDN L4

Not used in host mode.
PCIE RESET
PCIE_RST_0_N TP_TBT_PCIE_RESET0_L N6
PCIE_RST_1_N TP_TBT_PCIE_RESET1_L T1
PCIE_RST_2_N TP_TBT_PCIE_RESET2_L Y5
PCIE_RST_3_N TP_TBT_PCIE_RESET3_L U2
PCIE_CLKREQ_OD_N =TBT_CLKREQ_L W6
EN_LC_PWR TBT_EN_LC_PWR K5

CLOCKS
REFCLK_100_IN_P PCIE_CLK100M_TBT_P AB21
REFCLK_100_IN_N PCIE_CLK100M_TBT_N AD21
XTAL_25_IN SYSCLK_CLK25M_TBT_R AA24
XTAL_25_OUT TP_TBT_XTAL25OUT AB23
TMU_CLK_OUT TBT_TMU_CLK_OUT AA4
TMU_CLK_IN TBT_TMU_CLK_IN Y3

RSENSE TBT_RSENSE U20
RBIAS TBT_RBIAS W20
R3655 1K 1% 1/20W MF 201
NC NC U4

NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX

=PP3V3_TBTLC_RTR
R3698 10K 5% 1/16W MF-LF 402
R3695 806 1% 1/16W MF-LF 402
SYSCLK_CLK25M_TBT
Divides 3.3V to 1.8V

NO STUFF
R3697 100K 5% 1/16W MF-LF 402
R3699 10K 5% 1/16W MF-LF 402
R3696 1K 5% 1/16W MF-LF 402

=PP3V3_TBTLC_RTR
R3680 10K 5% 1/16W MF-LF 402

TBT_DDC_XBAR_EN_L
TBT_GO2SX_BIDIR
R3681 for CYA, allows separation of GPIO_2/GPIO_9 if necessary. Stuff one of R3861/2.
R3681 0 5% 1/16W MF-LF 402
TBT_GPIO_9
TBT_GPIO_14

NO STUFF
R3683 10K 5% 1/16W MF-LF 402
R3682 10K 5% 1/16W MF-LF 402

=PP3V3_S4_TBT
R3685 10K 5% 1/16W MF-LF 402
R3686 10K 5% 1/16W MF-LF 402
TBT_A_DP_PWRDN
TBT_B_DP_PWRDN
TBT_A_HV_EN
TBT_B_HV_EN

R3688 10K 5% 1/16W MF-LF 402
R3687 10K 5% 1/16W MF-LF 402

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0> C3620 0.1UF DP_TBTSNK0_ML_P<0>
DP_TBTSNK0_ML_C_N<0> C3621 0.1UF DP_TBTSNK0_ML_N<0>
DP_TBTSNK0_ML_C_P<1> C3622 0.1UF DP_TBTSNK0_ML_P<1>
DP_TBTSNK0_ML_C_N<1> C3623 0.1UF DP_TBTSNK0_ML_N<1>
DP_TBTSNK0_ML_C_P<2> C3624 0.1UF DP_TBTSNK0_ML_P<2>
DP_TBTSNK0_ML_C_N<2> C3625 0.1UF DP_TBTSNK0_ML_N<2>
DP_TBTSNK0_ML_C_P<3> C3626 0.1UF DP_TBTSNK0_ML_P<3>
DP_TBTSNK0_ML_C_N<3> C3627 0.1UF DP_TBTSNK0_ML_N<3>
DP_TBTSNK0_AUXCH_C_P C3628 0.1UF DP_TBTSNK0_AUXCH_P
DP_TBTSNK0_AUXCH_C_N C3629 0.1UF DP_TBTSNK0_AUXCH_N

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0> C3630 0.1UF DP_TBTSNK1_ML_P<0>
DP_TBTSNK1_ML_C_N<0> C3631 0.1UF DP_TBTSNK1_ML_N<0>
DP_TBTSNK1_ML_C_P<1> C3632 0.1UF DP_TBTSNK1_ML_P<1>
DP_TBTSNK1_ML_C_N<1> C3633 0.1UF DP_TBTSNK1_ML_N<1>
DP_TBTSNK1_ML_C_P<2> C3634 0.1UF DP_TBTSNK1_ML_P<2>
DP_TBTSNK1_ML_C_N<2> C3635 0.1UF DP_TBTSNK1_ML_N<2>
DP_TBTSNK1_ML_C_P<3> C3636 0.1UF DP_TBTSNK1_ML_P<3>
DP_TBTSNK1_ML_C_N<3> C3637 0.1UF DP_TBTSNK1_ML_N<3>
DP_TBTSNK1_AUXCH_C_P C3638 0.1UF DP_TBTSNK1_AUXCH_P
DP_TBTSNK1_AUXCH_C_N C3639 0.1UF DP_TBTSNK1_AUXCH_N

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

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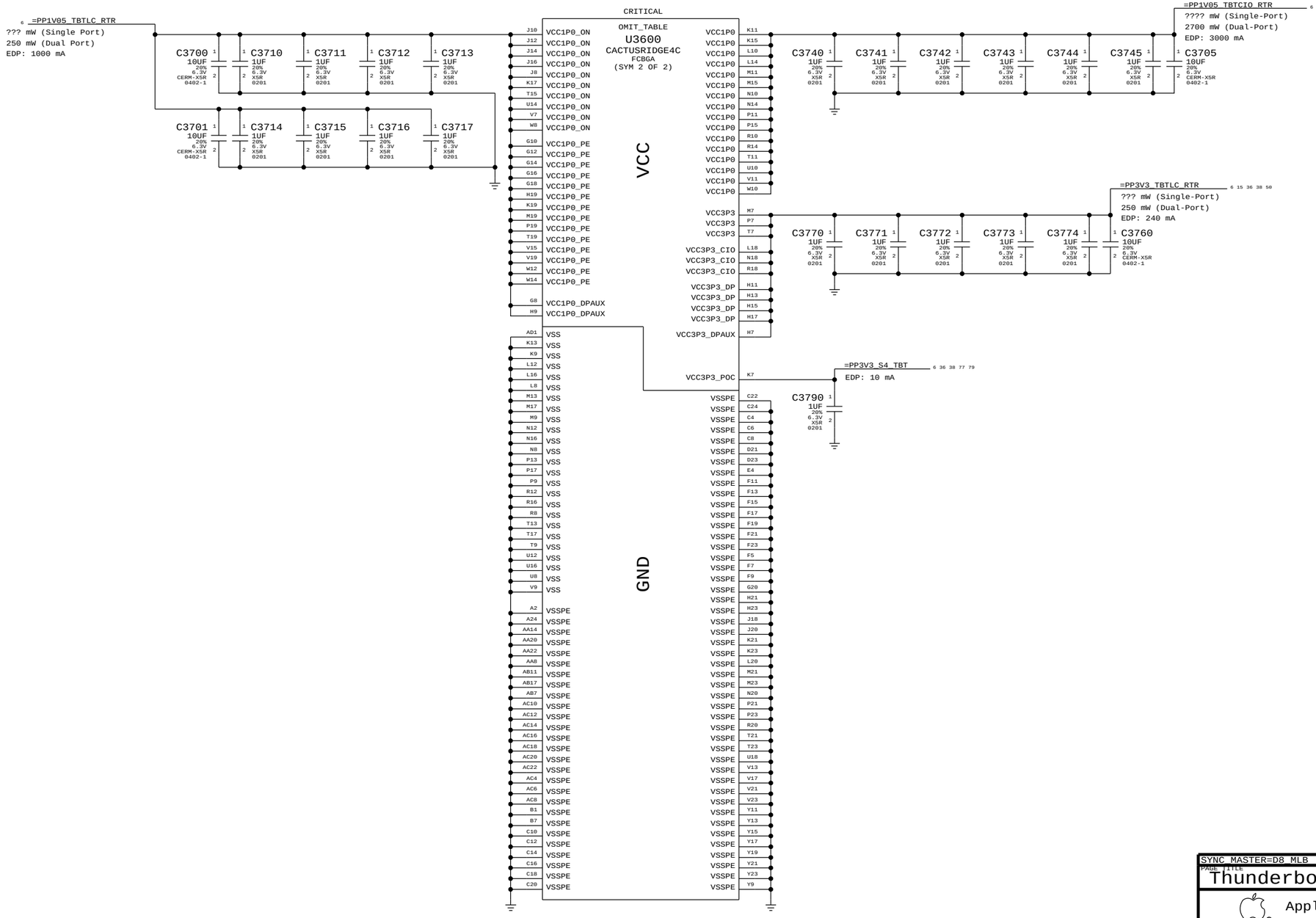

EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

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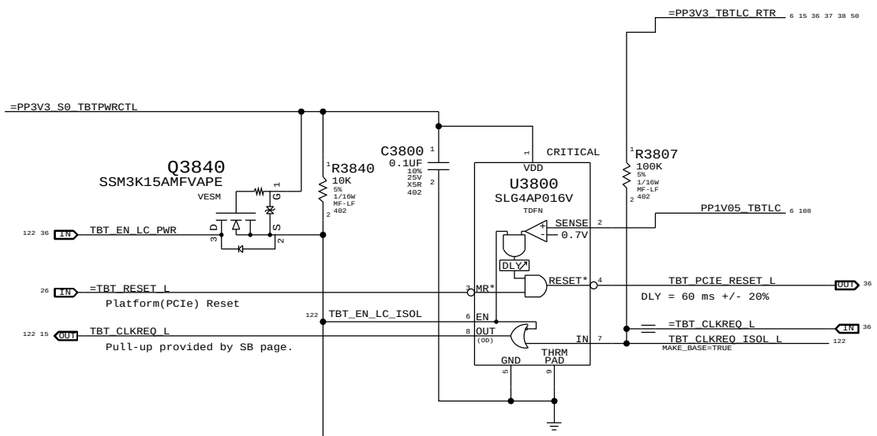
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

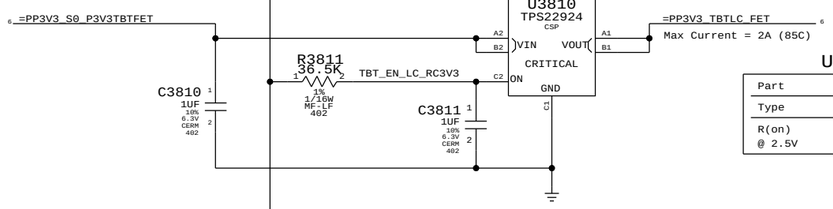
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation



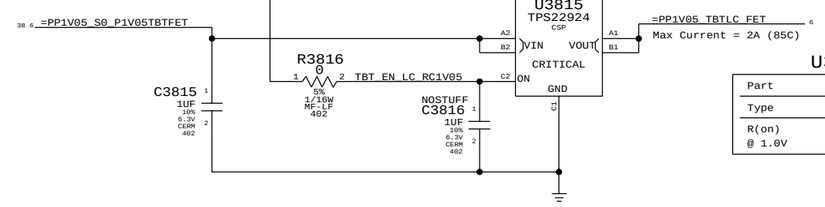
3.3V TBT "LC" Switch



U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

1.05V TBT "LC" Switch

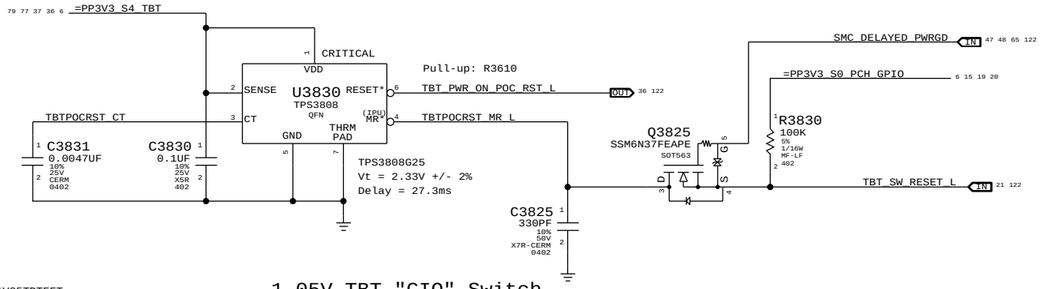


U3815

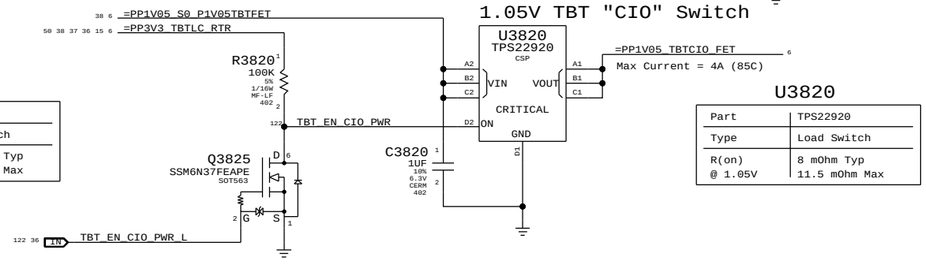
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.



1.05V TBT "CIO" Switch



U3820

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_S4_ENET_FET
281mA (1000base-T max power, Caesar IV)

R3901 0 5% 1/16W MF-LF 402
PP3V3_S4_ENET_FET_SRVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3979 4.7UF 20% 6.3V X5R-CERM 402
C3996 0.1UF 10% 16V X5R-CERM 0201
C3997 0.1UF 10% 16V X5R-CERM 0201
=PP3V3R1V8_CR_IOPWR_OUT
VDD for Card Reader I/O

CRITICAL
L3900 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_S4_ENET_FET_XTALVDDH
C3900 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L3905 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_S4_ENET_FET_BIASVDDH
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL
L3910 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_S4_ENET_FET_AVDDH
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201
C3912 1.0UF 10% 6.3V X5R-CERM 0201

C3915 4.7UF 20% 6.3V X5R-CERM 402
C3999 0.1UF 10% 16V X5R-CERM 0201
C3998 0.1UF 10% 16V X5R-CERM 0201
C3916 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402

=PP3V3_S0_ENET
Current Limiting Resistor
R3942 1K 5% 1/16W MF-LF 402

AVDDH BIASVDDH XTALVDDH VDDO SR_VDD SR_VDDP SR_LX SR_VFB AVDDL PCIE_PLLVDDL GPHY_PLLVDDL VDDC

OMIT_TABLE
U3900
BCM57765
QFN-8X8

ENET_SR_LX
ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_S4_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL
L3920 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_S4_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402
C3913 1.0UF 10% 6.3V X5R-CERM 0201

CRITICAL
L3925 FERR-600-OHM-0.5A SM
PP1V2_S4_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL
L3930 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_S4_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_P
PCIE_ENET_R2D_C_N
C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

=ENET_WAKE_L
(See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT → VMAIN_PRSNT (IPD-ENET)
PCIE_ENET_D2R_C_N → PCIE_TXD_N
PCIE_ENET_D2R_C_P → PCIE_TXD_P
PCIE_ENET_R2D_P → PCIE_RXD_P
PCIE_ENET_R2D_N → PCIE_RXD_N
PCIE_CLK100M_ENET_P → PCIE_REFCLK_P
PCIE_CLK100M_ENET_N → PCIE_REFCLK_N
ENET_RESET_L → PERST* (IPD)
ENET_CLKREQ_L_Q → CLKREQ* (OD)
WAKE* (OD)
ENET_LOW_PWR → LOW_PWR (IPD)
SMB_ENET_SCL → SMB_CLK
SMB_ENET_SDA → SMD_DATA (IPD-ENETM)
ENET_SCLK → SCLK
ENET_MISO → SI/LINKLED*
ENET_MOSI → SO
ENET_CS_L → CS*
TP_ENET_CR_3V3_EN_L → SPD100LED*/SERIAL_DO (OD)
ENET_TRAFFICLED_L → TRAFFICLED*/SERIAL_DI (OD)
SYSCLK_CLK25M_ENET → XTALI
NC → XTALO
ENET_RDAC → RDAC
THRM_PAD

R3965 1.24K 1% 1/16W MF-LF 402

NOTE: "IPx" == Programmable pull-up/down (IPx-ENETM)
SD_DETECT can only be used active low due to errata. (IPU-ENET)

GPIO_0 → TP_ENET_CR_1V8_EN
GPIO_1/CR_BUS_PWR → PP3V3R1V8_ENET_LR_OUT_REG
RE*/GPIO_2 → ENET_MEDIA_SENSE
SD_DETECT/WE* → ENET_SD_DETECT_L
CR_CMD/CLE → ENET_SD_CMD
CR_CLK/RY_BY* → ENET_SD_CLK
CR_DATA0 → ENET_CR_DATA<0>
CR_DATA1 → ENET_CR_DATA<1>
CR_DATA2 → ENET_CR_DATA<2>
CR_DATA3 → ENET_CR_DATA<3>
CR_DATA4 → ENET_CR_DATA<4>
CR_DATA5 → ENET_CR_DATA<5>
CR_DATA6 → ENET_CR_DATA<6>
CR_DATA7 → ENET_CR_DATA<7>
CE*/MS_INS* → NC_ENET_CE_L_MS_INS_L (NO_TEST=TRUE)
CR_LED/ALE → ENET_CR_PWREN
CR_WP*/XD_WP* → ENET_SR_DISABLE
XD_DETECT

R3961 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.26:5MM → SDCONN_CMD
R3979 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.21:5MM → SDCONN_CLK
R3971 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.25:5MM → SDCONN_DATA<0>
R3972 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.24:5MM → SDCONN_DATA<1>
R3973 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.23:5MM → SDCONN_DATA<2>
R3974 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.22:5MM → SDCONN_DATA<3>
R3975 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.52:5MM → SDCONN_DATA<4>
R3976 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.53:5MM → SDCONN_DATA<5>
R3977 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.54:5MM → SDCONN_DATA<6>
R3978 33 5% 1/20W MF 201 — 2PLACE_NEAR=U3900.55:5MM → SDCONN_DATA<7>

ENETCONN_MDI_P<0> TRD0_P
ENETCONN_MDI_N<0> TRD0_N
ENETCONN_MDI_P<1> TRD1_P
ENETCONN_MDI_N<1> TRD1_N
ENETCONN_MDI_P<2> TRD2_P
ENETCONN_MDI_N<2> TRD2_N
ENETCONN_MDI_P<3> TRD3_P
ENETCONN_MDI_N<3> TRD3_N

MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3R1V8_CR_IOPWR_OUT

ENET_SD_DETECT_L
SDCONN_CMD
SDCONN_CLK
SDCONN_DATA<0>
SDCONN_DATA<1>
SDCONN_DATA<2>
SDCONN_DATA<3>
SDCONN_DATA<4>
SDCONN_DATA<5>
SDCONN_DATA<6>
SDCONN_DATA<7>

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.
SDCONN_WP

R3981 1K 5% 1/16W MF-LF 402
ENET supports both active-levels for WP.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
IF ENET SWITCHING REGULATOR IS USED, THIS PIN SHOULD HAVE A 1K PD TO GND

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_S4_ENET_FET
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC GND SCK CS* WP* RESET* SI SO
ENET_SCLK
ENET_CS_L
ENET_MOSI
ENET_MISO
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	ETHERNET PHY (CAESAR IV+)
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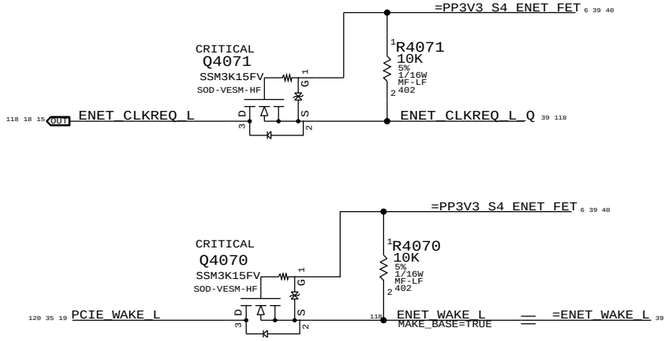
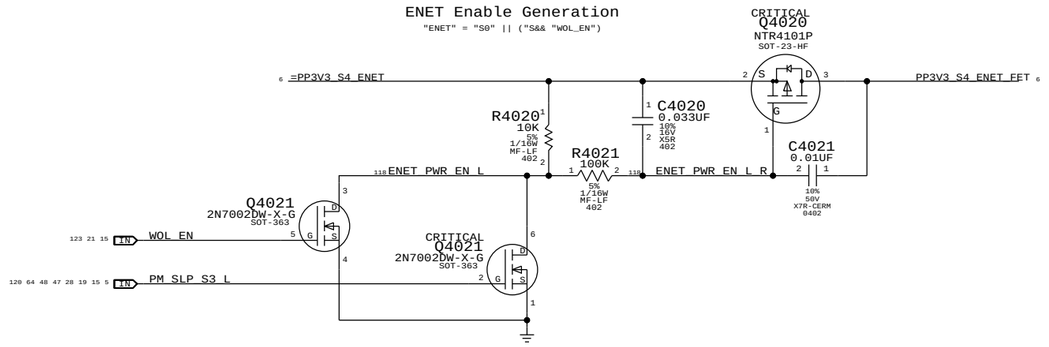
CAESAR IV WAKE# ISOLATION

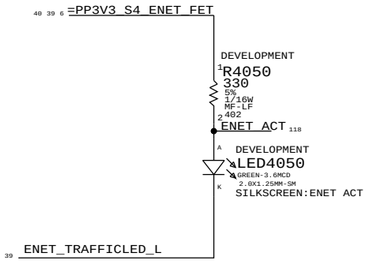


ENET Enable Generation

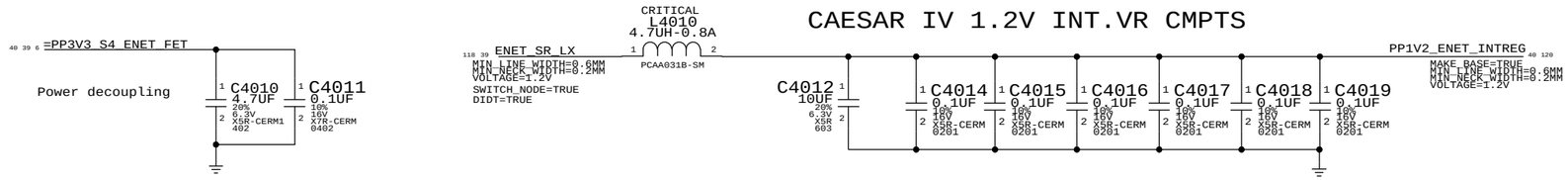
"ENET" = "S0" || ("S&& "WOL_EN")



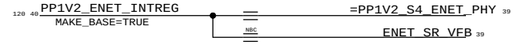
CAESAR IV ACTIVITY LED

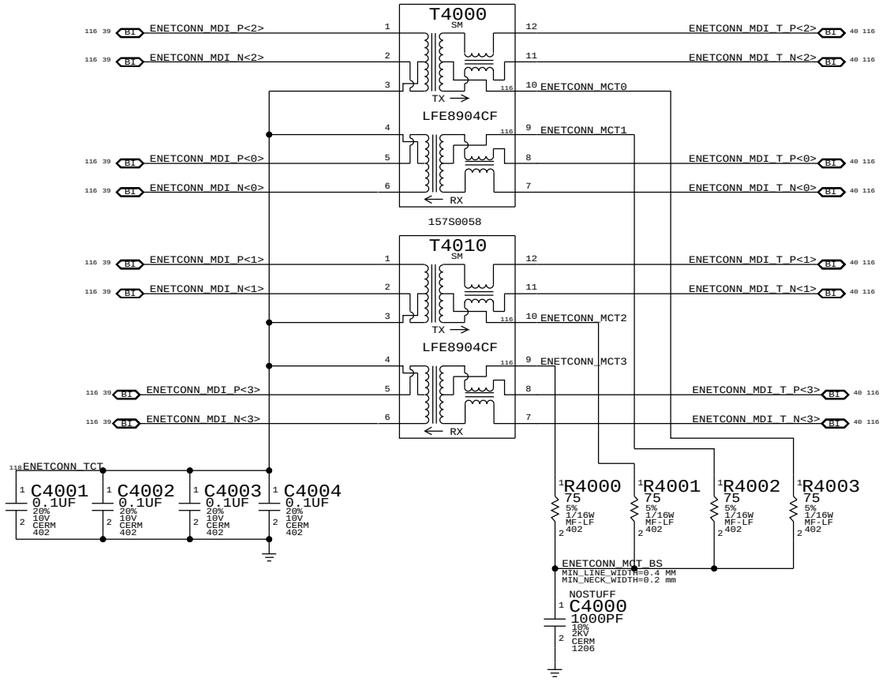


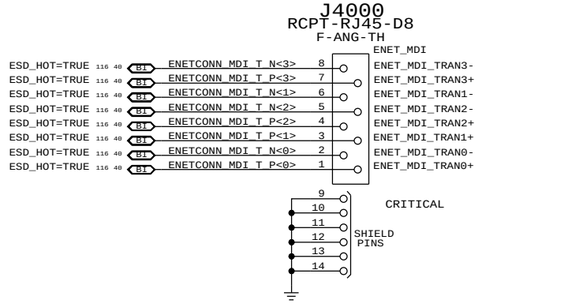
CAESAR IV 1.2V INT.VR CMPTS

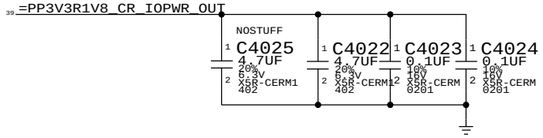


Feedback loop









SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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Ethernet Support & Connector

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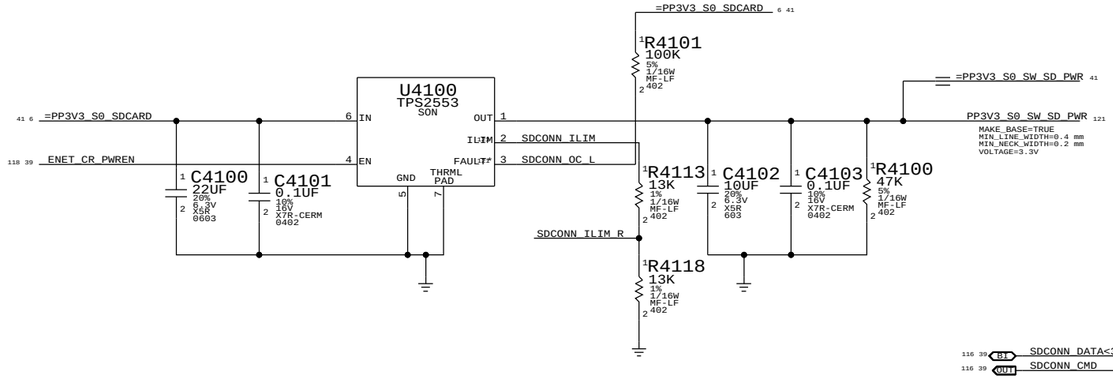
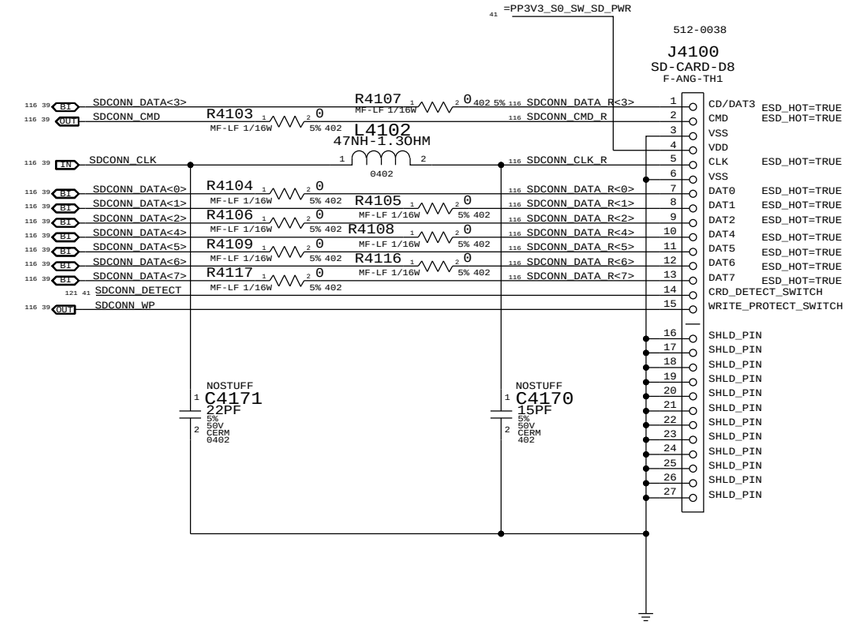
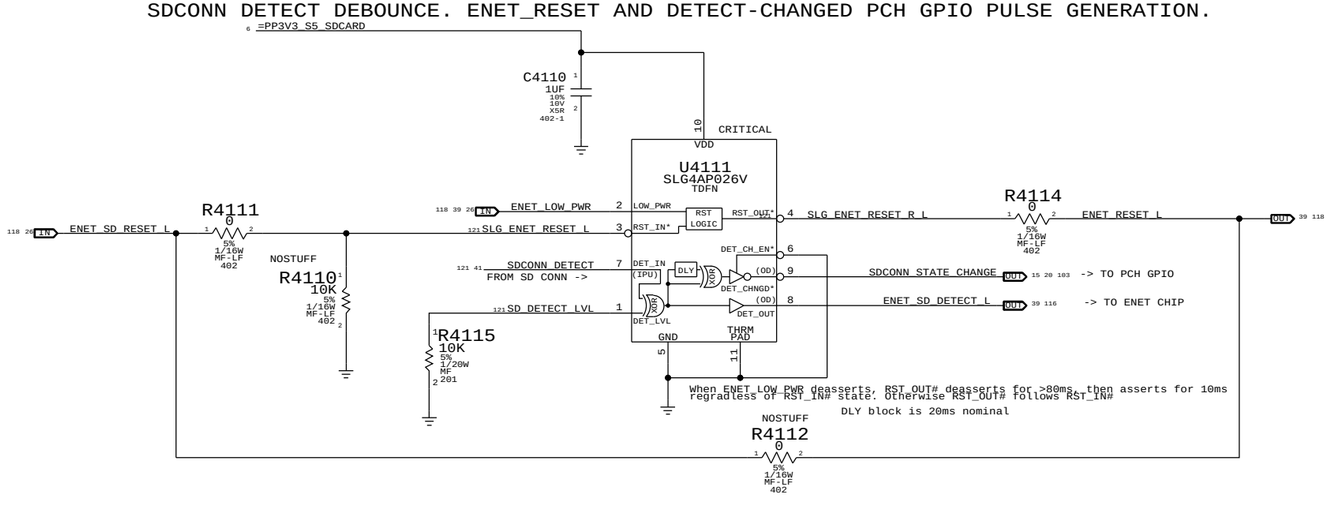
SD CARD 3.3V OVERCURRENT PROTECTION





SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

SD READER CONNECTOR

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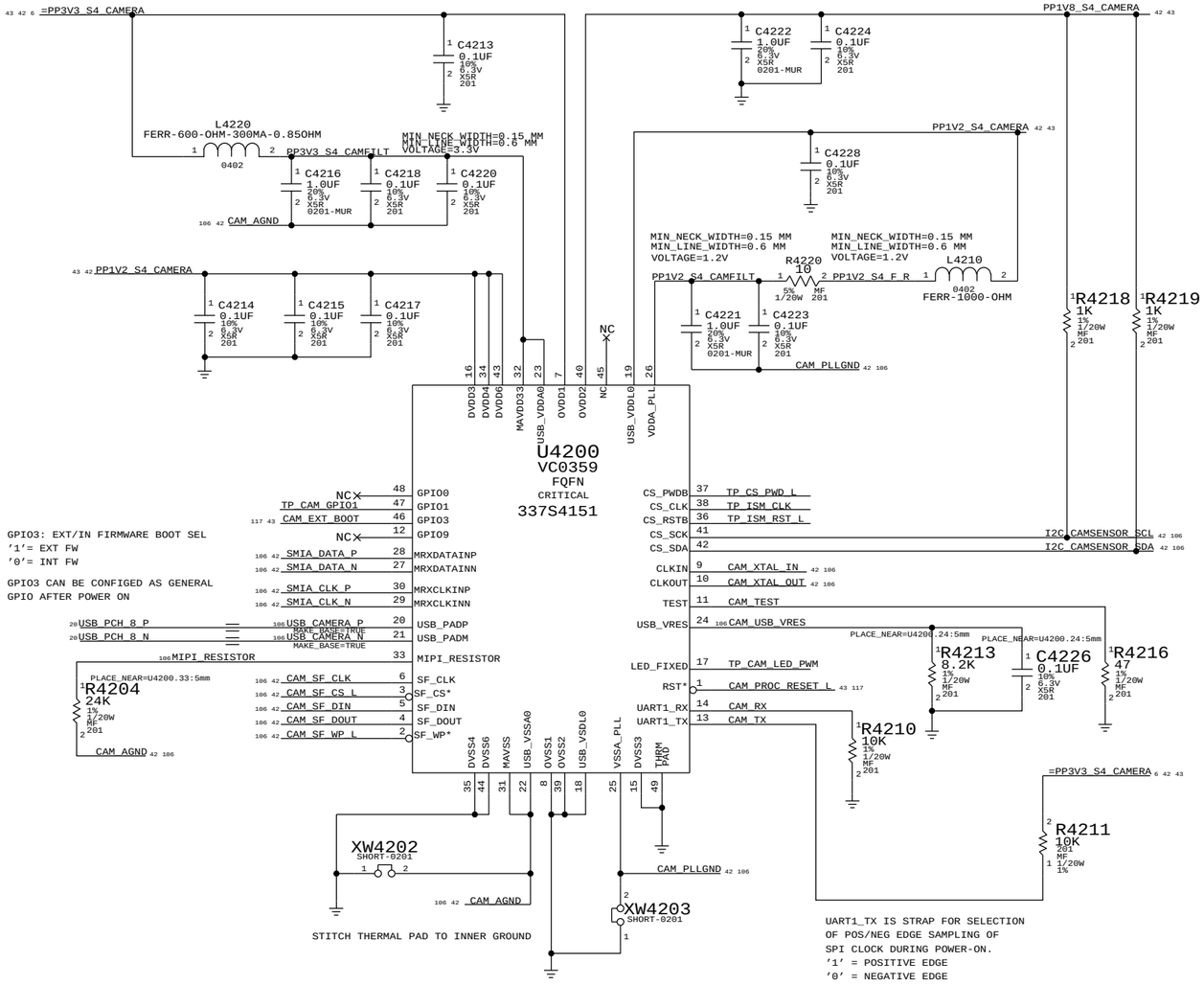
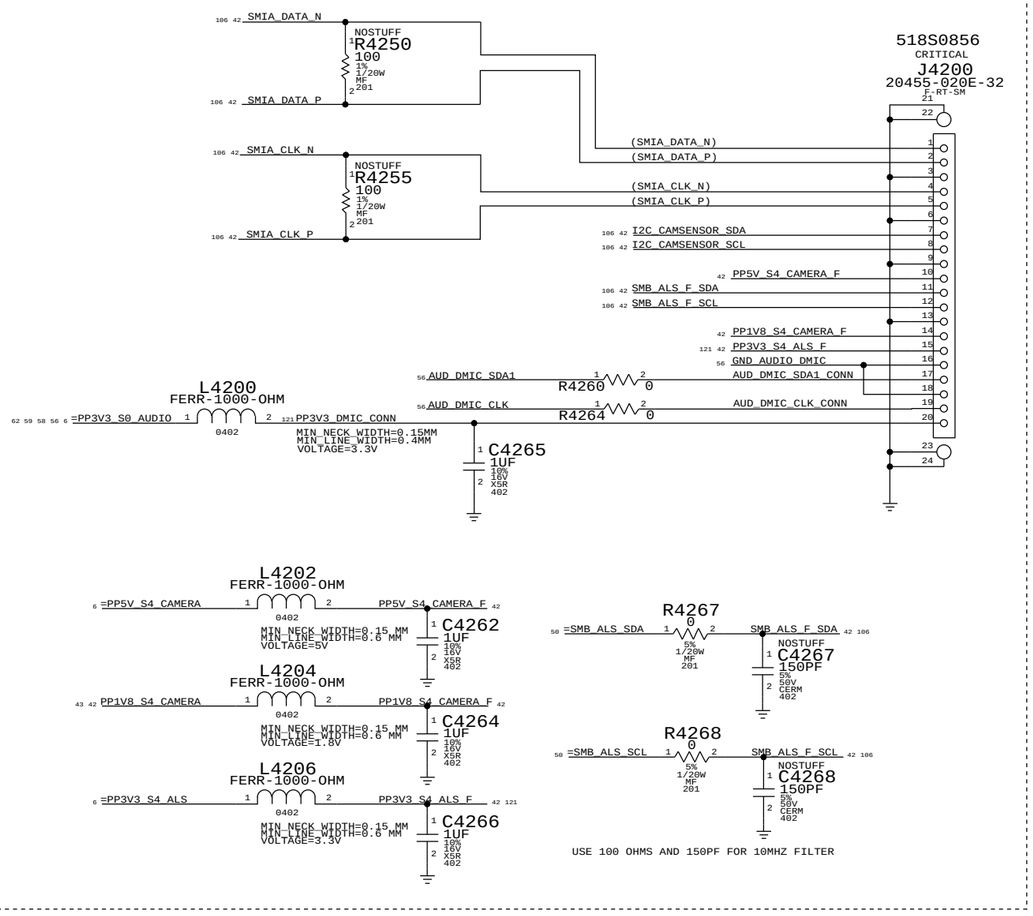
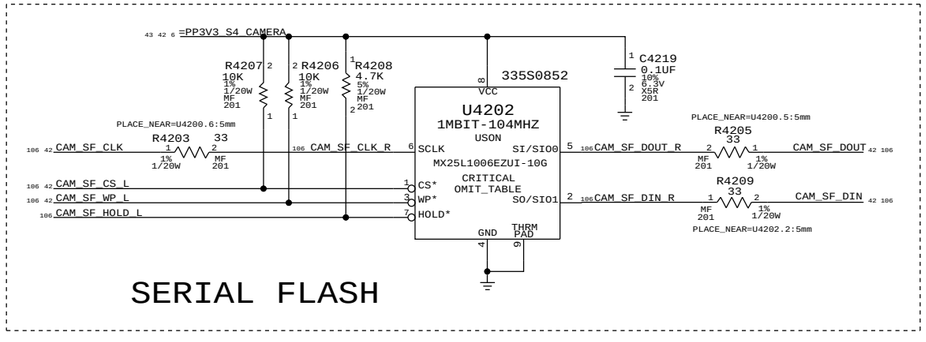
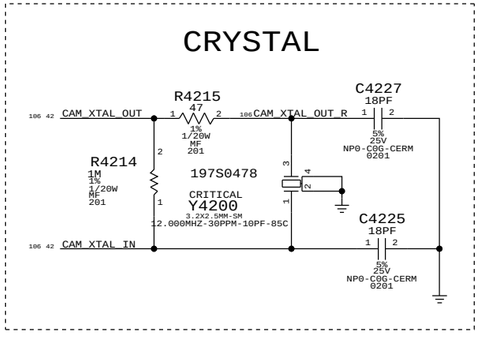
USB CAMERA CONTROLLER



CAMERA/ALS/DMIC CONNECTOR







SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Camera Controller

Apple Inc.

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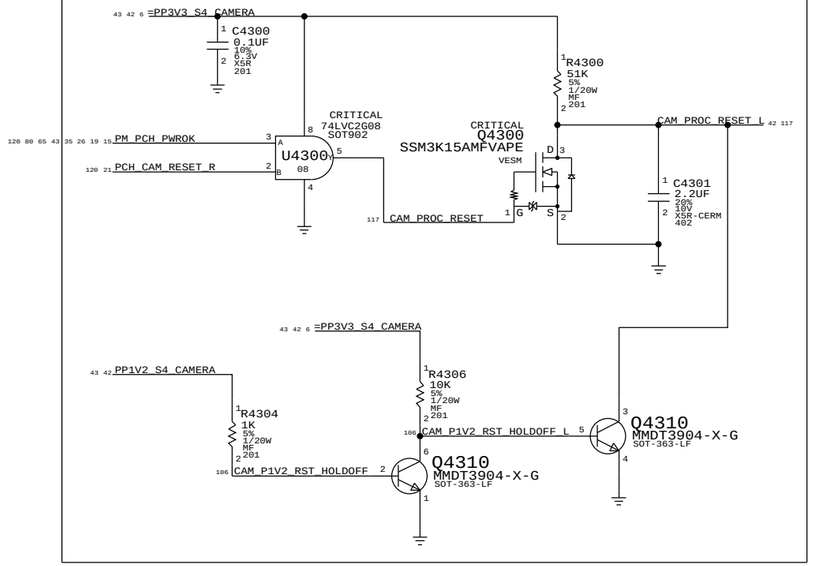
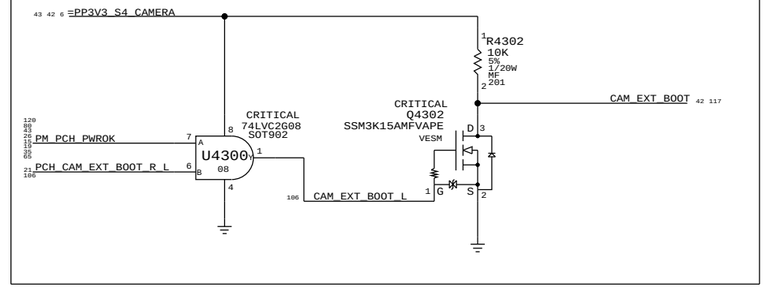
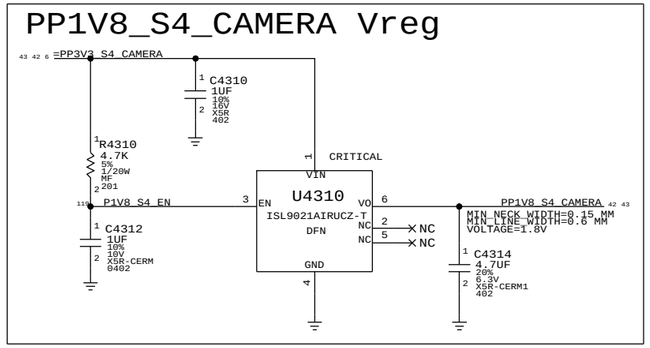
Camera Processor Reset



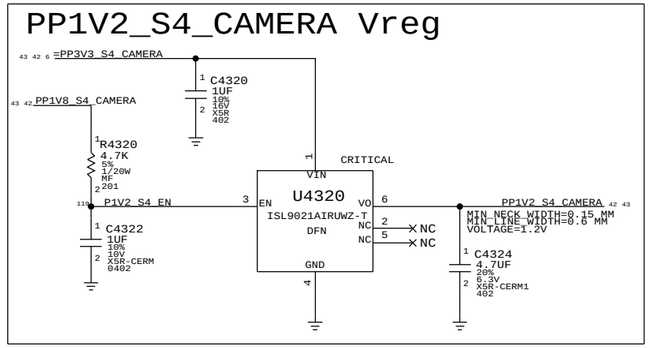
Camera Processor ExtBoot Cntl



PP1V8_S4_CAMERA Vreg



PP1V2_S4_CAMERA Vreg



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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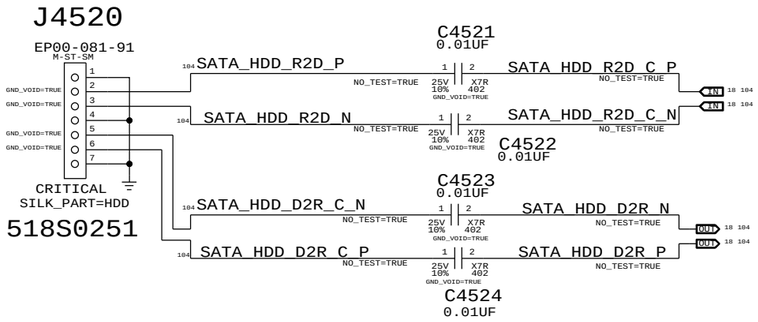
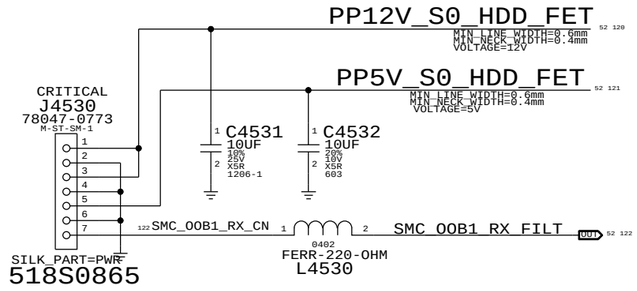
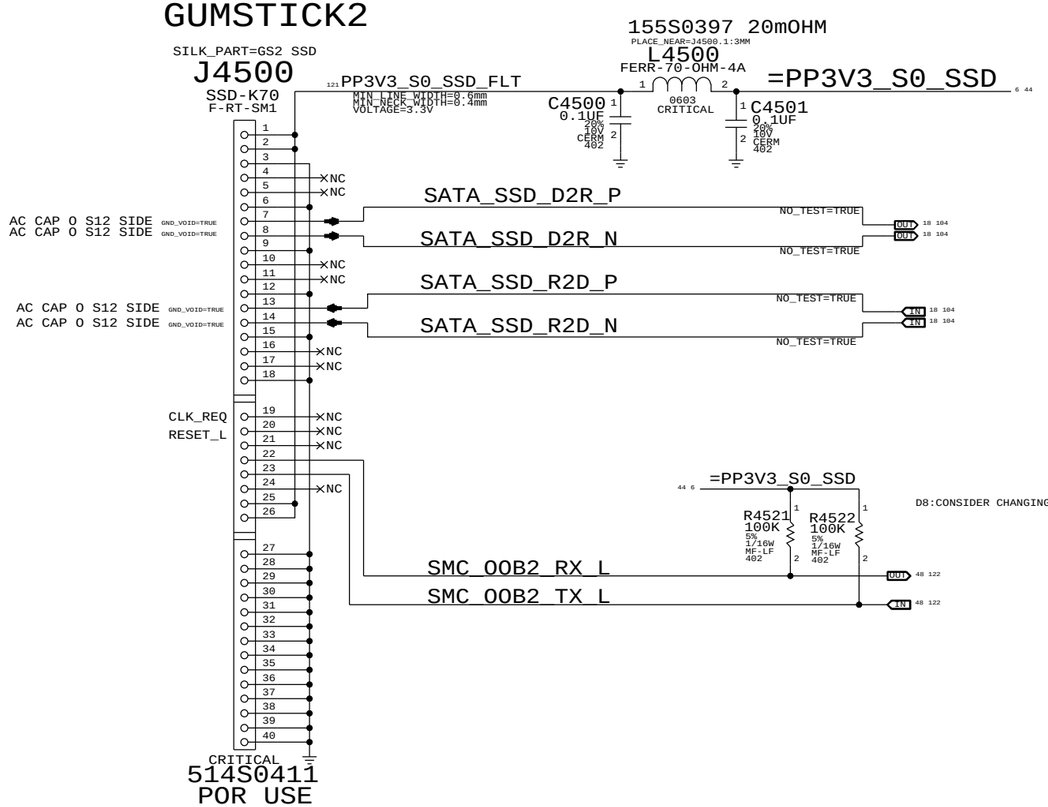
HDD DATA



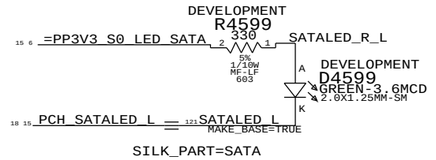
HDD POWER



GUMSTICK2



SATA Activity LED



D8:CONSIDER CHANGING SMC_OOB2_RX/TX_L PULL-UP TO 100K (FROM 10K) RDAR://10817697

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EXTERNAL USB PORTS A & B

USB/SMC DEBUG MUX

=PP5V_S4_USB
C4602 330UF-25MOHM 20% 6.3V TANT CASE-D2E
C4601 0.1UF 20% 10V CERM 402
PLACE_NEAR=U4600.2:2MM

353S3052 CRITICAL
U4600 TPS2561DR SON
IN_0, IN_1, OUT1, OUT2, FAULT1*, FAULT2*, ILIM, EN1, EN2, GND, THRM PAD

44 mOHM
3ms Rise Time

USB_EXTB_OC_L
USB_EXTA_OC_L
PM_EN_USB_PWR
USB_EXTAB_ILIM
PLACE_NEAR=U4600.7:2MM
R4602 11.5K 1% 1/10W MF-LF 402
USB_EXTAB_ILIM_R
PLACE_NEAR=R4602.2:2MM
R4603 11.5K 1% 1/10W MF-LF 402
23.2K (1%)
=> 2.19A MIN
=> 2.63A MAX
2x ILIM resistors rdar://11104691

NOSTUFF C4603 10UF 20% 10V X5R 603
=PP5V_S4_EXTA
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
155S0367 L4601 BLM18S121: 25 mOHM FERR-120-OHM-3A 0603
=PP5V_S4_EXTA_F
C4605 0.01UF 20% 16V X7R-CERM 0402
C4607 0.1UF 20% 10V CERM 402

R4604 0 5% 1/10W MF-LF 402
=PP3V3_G3H_SMC_USBMUX
=PP3V3_G3H_SMC_USBMUX_R
VOLTAGE=3.3V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM
R4605 10K 5% 1/10W MF-LF 402
C4606 0.1UF 20% 10V CERM 402

U4610 USB3740 DFN 353S3603 CRITICAL
VDD, DP_2, DM_2, DP_1, DM_1, OE*, S, GND, DP, DM

USB_PCH_0_P
USB_PCH_0_N
MOJO_RX_L
MOJO_TX_L
USB_DEBUGPRT_EN_L
SEL: 0 MOJO
SEL: 1 USB
SIGNAL_MODEL=SWI_USB3740_DFN_USB3740_MOJO

USB2_EXTA_MUXED_P
USB2_EXTA_MUXED_N
NO_TEST=TRUE

155S0430 CRITICAL L4602 120-OHM-90MA DLP0NS
377S0126 CRITICAL SLP1210N6 RCLAMP0582N D4601
NOSTUFF

377S0104 CRITICAL D4602 ESD0P2RF-02LS TSSLP-2-1
377S0104 CRITICAL D4603 ESD0P2RF-02LS TSSLP-2-1

155S0721 CRITICAL L4603 80OHM-25%-100MA L2 L1 0504
GND_VOID=TRUE
USB3_EXTA_RX_F_N
USB3_EXTA_RX_F_P
USB3_EXTA_TX_N
USB3_EXTA_TX_P
USB3_EXTA_TX_C_N
USB3_EXTA_TX_C_P
C4608 0.1UF X5R 10% 6.3V 201
C4609 0.1UF X5R 10% 6.3V 201

155S0721 CRITICAL L4604 80OHM-25%-100MA L2 L1 0504
377S0104 CRITICAL D4604 ESD0P2RF-02LS TSSLP-2-1
377S0104 CRITICAL D4605 ESD0P2RF-02LS TSSLP-2-1

USB3_EXTA_RX_N
USB3_EXTA_RX_P
USB3_EXTA_TX_F_N
USB3_EXTA_TX_F_P
USB2_EXTA_MUXED_F_N
USB2_EXTA_MUXED_F_P

EXT PORT A
514-0839 CRITICAL J4600 USB-NO1-T86-D8 F-ANG-TH
VBUS, D-, D+, GND, STDA_SSRX-, STDA_SSRX+, GND_DRAIN, STDA_SSTX-, STDA_SSTX+, SHIELD

155S0367 L4611 BLM18S121: 25 mOHM FERR-120-OHM-3A 0603
=PP5V_S4_EXTB
=PP5V_S4_EXTB_F
C4615 0.01UF 20% 16V X7R-CERM 0402
C4617 0.1UF 20% 10V CERM 402

NOSTUFF C4613 10UF 20% 10V X5R 603
=PP3V3_S5_SMC_USBMUX
C4616 0.1UF 20% 10V CERM 402
R4615 10K 5% 1/10W MF-LF 402

U4630 USB3740 DFN 353S3603 CRITICAL
XHCI
EHCI
USB_PCH_1_P
USB_PCH_1_N
USB_PCH_9_P
USB_PCH_9_N
USB_EXTB_SEL_XHCI
PCH GPIO60

USB2_EXTB_MUXED_P
USB2_EXTB_MUXED_N
NO_TEST=TRUE

155S0430 CRITICAL L4612 120-OHM-90MA DLP0NS
377S0126 CRITICAL SLP1210N6 RCLAMP0582N D4611
NOSTUFF

377S0104 CRITICAL D4612 ESD0P2RF-02LS TSSLP-2-1
377S0104 CRITICAL D4613 ESD0P2RF-02LS TSSLP-2-1

155S0721 CRITICAL L4613 80OHM-25%-100MA L2 L1 0504
GND_VOID=TRUE
USB3_EXTB_RX_F_N
USB3_EXTB_RX_F_P
USB3_EXTB_TX_N
USB3_EXTB_TX_P
USB3_EXTB_TX_C_N
USB3_EXTB_TX_C_P
C4619 0.1UF X5R 10% 6.3V 201

155S0721 CRITICAL L4614 80OHM-25%-100MA L2 L1 0504
377S0104 CRITICAL D4614 ESD0P2RF-02LS TSSLP-2-1
377S0104 CRITICAL D4615 ESD0P2RF-02LS TSSLP-2-1

USB3_EXTB_RX_N
USB3_EXTB_RX_P
USB3_EXTB_TX_F_N
USB3_EXTB_TX_F_P
USB2_EXTB_MUXED_F_N
USB2_EXTB_MUXED_F_P

EXT PORT B
514-0840 CRITICAL J4610 USB-NO2-T86-D8 F-ANG-TH
VBUS, D-, D+, GND, STDA_SSRX-, STDA_SSRX+, GND_DRAIN, STDA_SSTX-, STDA_SSTX+, SHIELD

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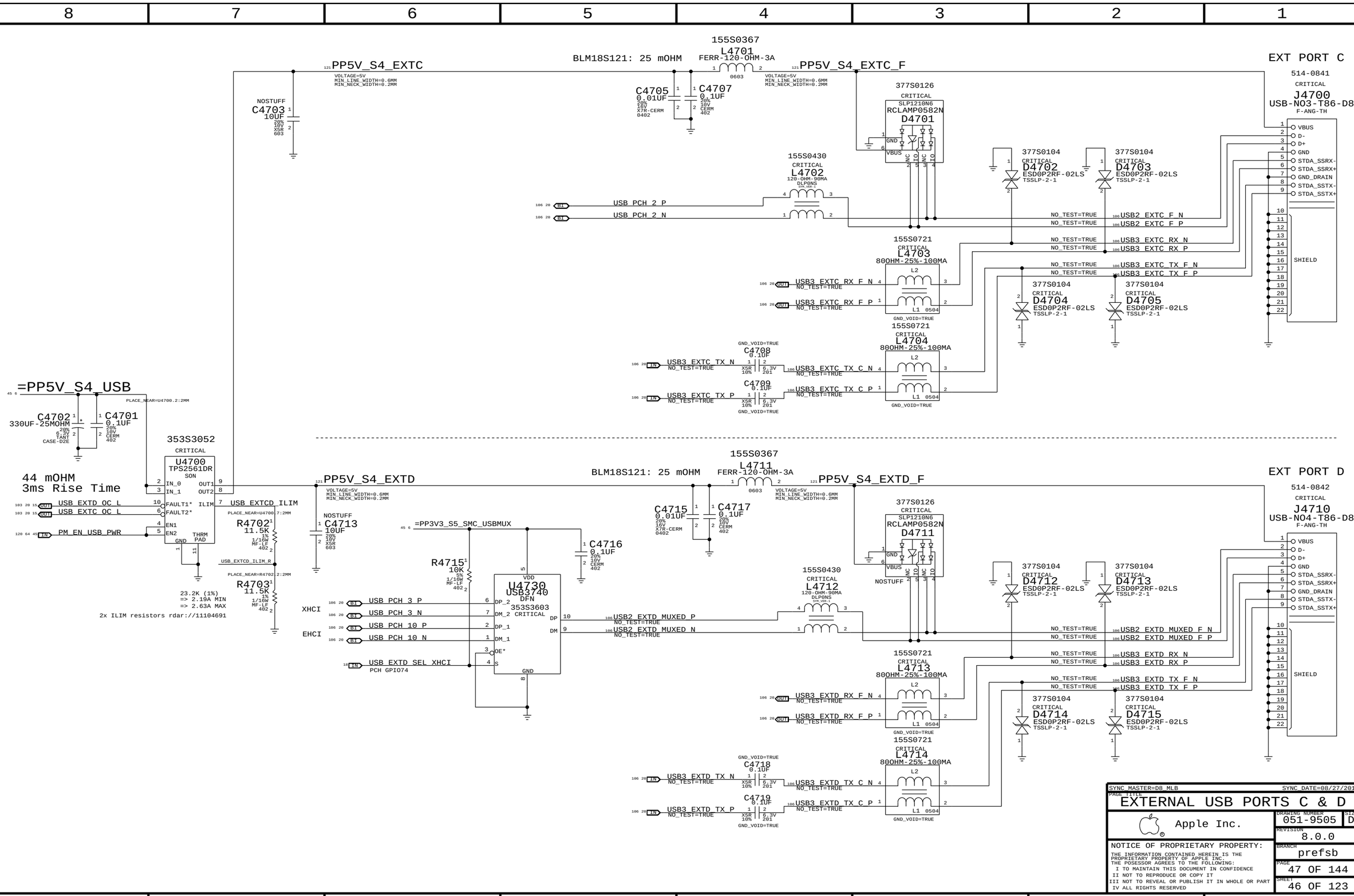
155S0367
L4701
BLM18S121: 25 mOHM
FERR-120-OHM-3A
0603
121 PP5V_S4_EXTC
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NOSTUFF
C4703
10UF
20%
10V
X5R
603
C4705
0.01UF
20%
16V
X7R-CERM
0402
C4707
0.1UF
20%
10V
CERM
402
121 PP5V_S4_EXTC_F
377S0126
CRITICAL
SLP1210N6
RCLAMP0582N
D4701
GND
VBUS
NC
NC
NC
NC
155S0430
CRITICAL
L4702
120-OHM-90MA
DLP0NS
106 20 BI USB_PCH_2_P
106 20 BI USB_PCH_2_N
377S0104
CRITICAL
D4702
ESD0P2RF-02LS
TSSLP-2-1
377S0104
CRITICAL
D4703
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT C
514-0841
CRITICAL
J4700
USB-NO3-T86-D8
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
NO_TEST=TRUE
106 USB2_EXTC_F_N
106 USB2_EXTC_F_P
106 USB3_EXTC_RX_N
106 USB3_EXTC_RX_P
106 USB3_EXTC_TX_F_N
106 USB3_EXTC_TX_F_P
155S0721
CRITICAL
L4703
80OHM-25%-100MA
L2
L1 0504
GND_VOID=TRUE
106 20 OUT USB3_EXTC_RX_F_N
106 20 OUT USB3_EXTC_RX_F_P
377S0104
CRITICAL
D4704
ESD0P2RF-02LS
TSSLP-2-1
377S0104
CRITICAL
D4705
ESD0P2RF-02LS
TSSLP-2-1
155S0721
CRITICAL
L4704
80OHM-25%-100MA
C4708
0.1UF
C4709
0.1UF
106 20 IN USB3_EXTC_TX_N
106 20 IN USB3_EXTC_TX_P
106 USB3_EXTC_TX_C_N
106 USB3_EXTC_TX_C_P
=PP5V_S4_USB
45 6
C4702
330UF-25MOHM
6.3V
TANT
CASE-D2E
C4701
0.1UF
353S3052
CRITICAL
U4700
TPS2561DR
SON
IN_0
IN_1
OUT1
OUT2
FAULT1*
FAULT2*
ILIM
EN1
EN2
THRM PAD
GND
44 mOHM
3ms Rise Time
103 20 15 OUT USB_EXTD_OC_L
103 20 15 OUT USB_EXTC_OC_L
120 64 48 IN PM_EN_USB_PWR
USB_EXTCD_ILIM
R4702
11.5K
1/16W
MF-LF
402
USB_EXTCD_ILIM_R
R4703
11.5K
1/16W
MF-LF
402
23.2K (1%)
=> 2.19A MIN
=> 2.63A MAX
2x ILIM resistors rdar://11104691
121 PP5V_S4_EXTD
NOSTUFF
C4713
10UF
155S0367
L4711
BLM18S121: 25 mOHM
FERR-120-OHM-3A
C4715
0.01UF
C4717
0.1UF
121 PP5V_S4_EXTD_F
377S0126
CRITICAL
SLP1210N6
RCLAMP0582N
D4711
NOSTUFF
=PP3V3_S5_SMC_USBMUX
C4716
0.1UF
R4715
10K
U4730
USB3740
DFN
353S3603
CRITICAL
VDD
DP_2
DM_2
DP_1
DM_1
OE*
S
GND
DP
DM
XHCI
EHCI
106 20 BI USB_PCH_3_P
106 20 BI USB_PCH_3_N
106 20 BI USB_PCH_10_P
106 20 BI USB_PCH_10_N
18 IN USB_EXTD_SEL_XHCI
PCH GPIO74
106 USB2_EXTD_MUXED_P
106 USB2_EXTD_MUXED_N
155S0430
CRITICAL
L4712
120-OHM-90MA
DLP0NS
377S0104
CRITICAL
D4712
ESD0P2RF-02LS
TSSLP-2-1
377S0104
CRITICAL
D4713
ESD0P2RF-02LS
TSSLP-2-1
EXT PORT D
514-0842
CRITICAL
J4710
USB-NO4-T86-D8
F-ANG-TH
VBUS
D-
D+
GND
STDA_SSRX-
STDA_SSRX+
GND_DRAIN
STDA_SSTX-
STDA_SSTX+
SHIELD
NO_TEST=TRUE
106 USB2_EXTD_MUXED_F_N
106 USB2_EXTD_MUXED_F_P
106 USB3_EXTD_RX_N
106 USB3_EXTD_RX_P
106 USB3_EXTD_TX_F_N
106 USB3_EXTD_TX_F_P
155S0721
CRITICAL
L4713
80OHM-25%-100MA
L2
L1 0504
GND_VOID=TRUE
106 20 OUT USB3_EXTD_RX_F_N
106 20 OUT USB3_EXTD_RX_F_P
377S0104
CRITICAL
D4714
ESD0P2RF-02LS
TSSLP-2-1
377S0104
CRITICAL
D4715
ESD0P2RF-02LS
TSSLP-2-1
155S0721
CRITICAL
L4714
80OHM-25%-100MA
C4718
0.1UF
C4719
0.1UF
106 20 IN USB3_EXTD_TX_N
106 20 IN USB3_EXTD_TX_P
106 USB3_EXTD_TX_C_N
106 USB3_EXTD_TX_C_P
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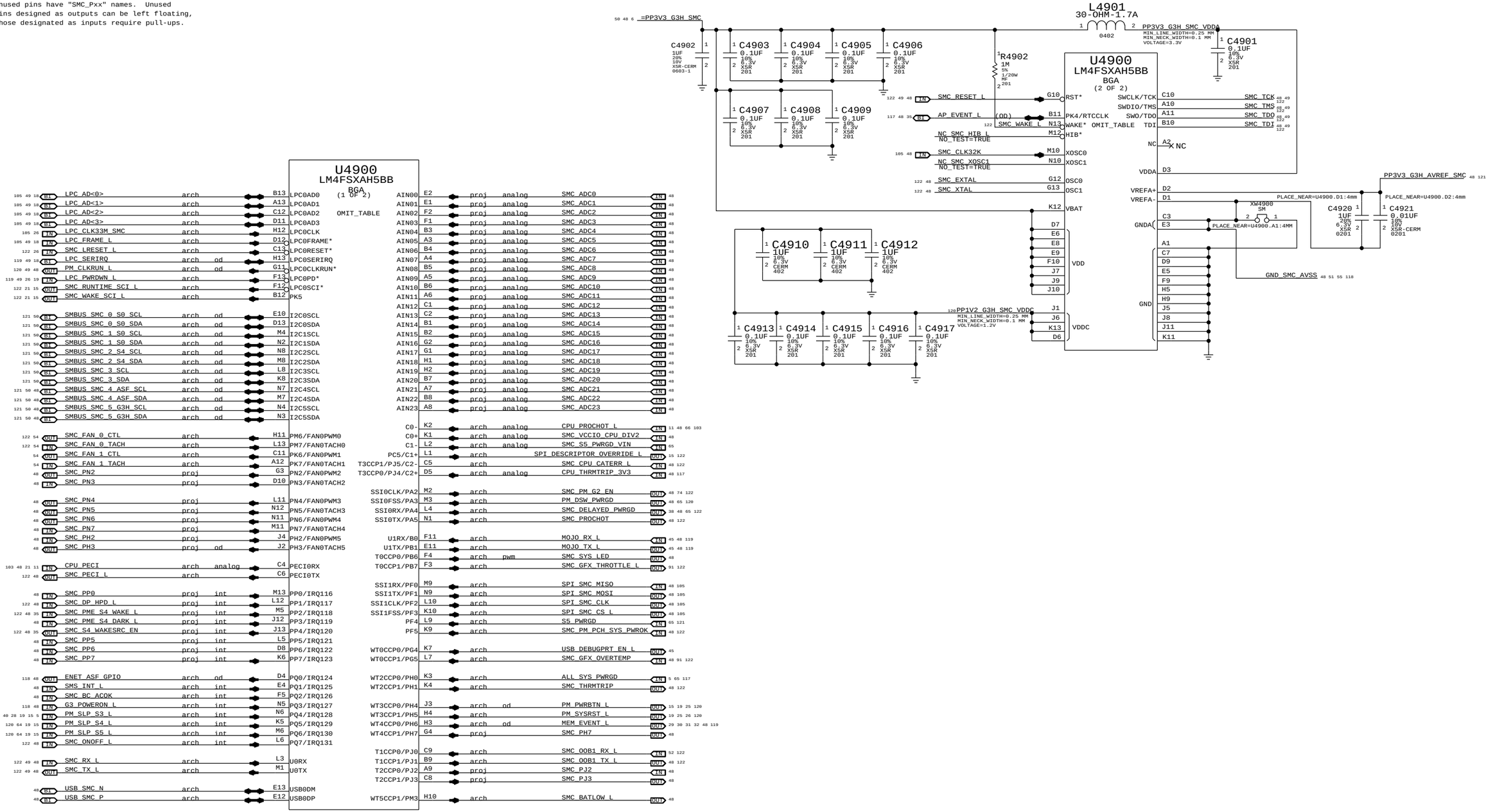
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



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SMC Supervisor and AVREF Supply

rdar://11180279 SMC_RESET_L workaround

=PP3V3_G3H_SMC → R5009 47 5% 1/16W MF-LF 402 → PP3V42_G3H_SMC_SPVSR (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.1MM, VOLTAGE=3.42V)

C5009 4.7UF 10% 25V X5R-CERM 0603 — GND_SMC_AVSS

=PPVIN_G3H_SMCVREF

C5000 0.47UF 10% 6.3V CERM-X5R 402

U5000 VREF-3.3V-VDET-3.0V DFN SN0903048 (V+, VIN, MR1*(ipu), MR2*(ipu), RESET*, DELAY, CRITICAL, REFOUT, GND, THRM PAD)

R5005 100K 5% 1/16W MF-LF 402

SILK_PART=PWR BTN

S5000 NTC020AA1JB260T (SM)

NC — MR1*(ipu)

NC — MR2*(ipu)

SMC_RESET_L (OUT 47 49 122)

SMC_MANUAL_RST_L

PP3V3_G3H_AVREF_SMC (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.1MM, VOLTAGE=3.3V)

C5001 0.01UF 10% 16V X7R-CERM 0402

C5005 1UF 20% 10V X5R-CERM 0603-1

C5006 0.01UF 10% 16V X7R-CERM 0402

GND_SMC_AVSS (MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.1MM, VOLTAGE=0V)

Note: IPU are pulled to VIN rail

ADC Channel Aliases

SMC_ADC0	SMCVSNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC1	SMCISNS_P12VG3H	MAKE_BASE=TRUE
SMC_ADC2	SMCVSNS_GPUCORE	MAKE_BASE=TRUE
SMC_ADC3	SMCISNS_GPUCORE	MAKE_BASE=TRUE
SMC_ADC4	SMCVSNS_P1V5S0_CPU_MEM	MAKE_BASE=TRUE
SMC_ADC5	SMCISNS_P1V5S0_CPU_MEM	MAKE_BASE=TRUE
SMC_ADC6	SMCVSNS_PVDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC7	SMCISNS_PVDDQS3_DDR	MAKE_BASE=TRUE
SMC_ADC8	SMCISNS_P12VS0_P1V05	MAKE_BASE=TRUE
SMC_ADC9	SMCISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE
SMC_ADC10	SMCVSNS_CPUCORE	MAKE_BASE=TRUE
SMC_ADC11	SMCISNS_CPUCORE	MAKE_BASE=TRUE
SMC_ADC12	SMCVSNS_CPUAXG	MAKE_BASE=TRUE
SMC_ADC13	SMCISNS_CPUAXG	MAKE_BASE=TRUE
SMC_ADC14	SMCVSNS_P5VS0_HDD	MAKE_BASE=TRUE
SMC_ADC15	SMCISNS_P5VS0_HDD	MAKE_BASE=TRUE
SMC_ADC16	SMCVSNS_P1V05S0_PCH	MAKE_BASE=TRUE
SMC_ADC17	SMCISNS_P1V05S0_PCH	MAKE_BASE=TRUE
SMC_ADC18	SMCISNS_P12VS0_HDD	MAKE_BASE=TRUE
SMC_ADC19	SMCISNS_P3V3S4_AP	MAKE_BASE=TRUE
SMC_ADC20	SMCVSNS_P3V3S0	MAKE_BASE=TRUE
SMC_ADC21	SMCISNS_P3V3S0_SSD	MAKE_BASE=TRUE
SMC_ADC22	SMCISNS_P12VS0_CPU_VCCSA	MAKE_BASE=TRUE
SMC_ADC23	SMCISNS_P12VS0_CPU_P1V05	MAKE_BASE=TRUE

Project-specific Aliases

SMC_PH3	BDV_BKL_PWM	MAKE_BASE=TRUE
SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE
SMC_PJ3	SMC_OOB2_TX_L	MAKE_BASE=TRUE
SMC_PJ2	SMC_OOB2_RX_L	MAKE_BASE=TRUE
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE
SMC_PN4	SMC_BLC_FAULT	MAKE_BASE=TRUE

Unused Project-specific

radar://11033060 Remove USB hookup from SMC (not needed)

USB_SMC_P	NC_USB_SMC_P	MAKE_BASE=TRUE, NO_TEST=TRUE
USB_SMC_N	NC_USB_SMC_N	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PN2	NC_SMC_PN2	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PN6	NC_SMC_PN6	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PN7	NC_SMC_PN7	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_PH7	TP_SMC_PH7	MAKE_BASE=TRUE, NO_TEST=TRUE

TP for access if ZPB re-instated

SMBUS_SMC_4_ASF_SCL	NC_SMC_4_ASF_SCL	MAKE_BASE=TRUE, NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE, NO_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE, NO_TEST=TRUE
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE, NO_TEST=TRUE
SMC_OOB1_TX_L	NC_SMB_OOB1_TX_L	MAKE_BASE=TRUE, NO_TEST=TRUE

SMC SPI Support

RDAR://11158919 D8:DETERMINE VALUE AND STUFF SERIES R FOR SPI BUS

R5050 24.9 1% 1/10W MF-LF 402 — SPI_SMC_MISO (IN) — SPI_MLB_MISO (OUT)

R5051 15 1% 1/10W MF-LF 402 — SPI_SMC_MOSI (IN) — SPI_MLB_MOSI (OUT)

R5052 15 1% 1/10W MF-LF 402 — SPI_SMC_CLK (IN) — SPI_MLB_CLK (OUT)

R5053 15 1% 1/10W MF-LF 402 — SPI_SMC_CS_L (IN) — SPI_MLB_CS_L (OUT)

SMC 32KHz Clock

R5060 22 5% 1/10W MF-LF 402 — PM_CLK32K_SUSCLK_R (IN) — SMC_CLK32K (OUT)

PLACE_NEAR=U1800.BA47:6MM

SMC Crystal

RDAR://10350663 SMC CRYSTAL SELECTION

SMC_EXTAL

NOSTUFF R5066 1M 5% 1/10W MF-LF 402

CRITICAL Y5065 12.000MHZ-50PPM-8PF-1000HM 5X3.2X1.2-SM 197S0472

SMC_XTAL_R — R5065 0 5% 1/10W MF-LF 402 — SMC_XTAL

C5065 12PF 5% 50V C0G-CERM 0402

C5066 12PF 5% 50V C0G-CERM 0402

Power Button

=PP3V3_G3H_SMC → R5020 10K 5% 1/20W MF 201 → SILK_PART=PWR BTN → S5020 NTC020AA1JB260T (SM) → SMC_ONOFF_L (MAKE_BASE=TRUE, OUT 47 122)

PWR_BTN (IN 121 6)

Enable S4 Wake Sources

=PP3V3_S4_TBTAPWRSW (IN 77 6) — =TBTAPWRSW_EN (OUT 77)

=PP3V3_S4_TBTBPWRSW (IN 79 6) — =TBTBPWRSW_EN (OUT 79)

SMC Controlled RTC Reset

To absorb current from discharging RTC Reset Cap

CRITICAL Q5099 SSM3K15AMFVAPE VESM

RTC_RESET_L_R (121) → R5094 330 5% 1/10W MF-LF 402 → RTC_RESET_L (OUT 18 26 121)

SMC_ASSERT_RTCRST (122 48)

R5099 10K 5% 1/16W MF-LF 402 — NOSTUFF C5099 1.0UF 20% 6.3V X5R-CERM 0402

PROCHOT Support

Level-shifter that allows SMC to drive PROCHOT

CRITICAL Q5025 SSM3K15AMFVAPE VESM

CPU_PROCHOT_L (BI 11 47 66 103)

SMC_PROCHOT (IN 122 47)

PECI Support

Level-shifter that allows unidir SMC to drive bidir PECI

PLACEMENT_NOTE: Place this circuit near the Tee point to minimize reflections

=PPVCCIO_S0_SMC (48 6)

CRITICAL Q5035 SSM3K15AMFVAPE VESM

SMC_PECI_L (IN 122 47) → R5035 0 5% 1/10W MF-LF 402 → SMC_PECI_L_R (122)

OMIT R5036 NOSTUFF NONE NONE NONE 402

SMC_CPU_PECI (122) → R5037 330 5% 1/16W MF-LF 402

CPU_PECI (BI 11 21 47 103) ← R5038 43 5% 1/16W MF-LF 402

Comparator VCCIO Reference

=PPVCCIO_S0_SMC (48 6)

PLACE_NEAR=U4900.K1:6MM

R5030 10K 1% 1/16W MF-LF 402 — SMC_VCCIO_CPU_DIV2 (OUT 47)

PLACE_NEAR=U4900.K1:5MM

R5031 10K 1% 1/16W MF-LF 402

C5031 0.1UF 10% 16V X7R-CERM 0402

PLACE_NEAR=U4900.K1:4MM

AC/DC Burst Mode Enable

=PP3V3_S5_SMC (6) — R5040 10K 5% 1/20W MF 201

=PP3V3_S4_SMC (6) — R5041 10K 5% 1/20W MF 201

BURSTMODE_EN_L (OUT 6 71 117)

Q5040 SSM6N15AFE SOT563

ACDC_BURST_EN (117)

Q5040 SSM6N15AFE SOT563

C5040 0.01UF 10% 16V X5R-CERM 0201

ACDC_BURST_EN_L (IN 117 48)

PM_SLP_S3_L (64 47 40 28 19 15 5 120)

Note:
Open-drain stage on S4 to account case when SMC is initializing in S5, and chip is not yet configured. and ACDC_BURST_EN_L could be floating.

SMC to monitor 12V G3H power in S3 If power high (i.e. charging iPad) enable BURSTMODE to avoid the AC/DC from oscillating in and out.

rdar://10506970
rdar://10196882

Platform Thermal Control

Allow either GFX_OVERTEMP, SMC-driven THRMTRIP or CPU-driven THRMTRIP to drive PCH PM_THRMTRIP

RDAR://10107203

=PPVCCIO_S0_SMC (48 6) → R5023 51 5% 1/20W MF 201

PM_THRMTRIP_L (BI 21 120)

=PP3V3_S0_SMC (91 51 48 6)

CRITICAL Q5023 SSM6N15AFE SOT563

SMC_GFX_OVERTEMP (IN 122 91 47) → R5024 10K 5% 1/20W MF 201

R5028 3.3K 5% 1/20W MF 201 — CRITICAL Q5027 MMDT3904-X-G SOT-363-LF

R5026 10K 5% 1/20W MF 201

SMC_ROMBOOT (IN 122 48) → R5025 1K 5% 1/20W MF 201

Note: Previously SMC_NMI. Matt card pulls low. SMC samples on power on to enter recovery flasher mode.

SMC_THRMTRIP (IN 122 47)

CPU_THRMTRIP_3V3 (OUT 47 117)

CPU_THRMTRIP_L (IN 103 117) → R5027 3.3K 5% 1/20W MF 201 → CPU_THRMTRIP_R_L (117)

CRITICAL Q5027 MMDT3904-X-G SOT-363-LF

SEE(RADAR://PROBLEM/11724870) THIS CIRCUIT WILL NOT WORK SECOND STAGE FET WILL NOT FIX THIS S0 COLLAPSES BEFORE SIGNAL REACHES 3.3 SOLUTION WILL REQUIRE LATCHING OF TT

Connect BLC Serial through Mojo Mux

For a debug ability to communicate to BLC MCU through SMC

MOJO_TX_L (IN 119 48 47 45) — MOJO_RX_L (OUT 119 48 47 45)

NOSTUFF R5058 0 5% 1/16W MF-LF 402 — CRITICAL Q5024 SSM6N15AFE SOT563

NOSTUFF R5059 0 5% 1/16W MF-LF 402 — CRITICAL Q5024 SSM6N15AFE SOT563

BLC_EXT_BOOT (IN 117 80 48)

=PP3V3_S0_SMC (6 48 51 91)

C5060 0.01UF 10% 16V X7R-CERM 0402

U5060 USB3740 DFN (VDD, DP_2, DM_2, DP_1, DM_1, OE*, S, GND)

SMC_TO_BLC_TX_L (122) → SMC_BLC_MUX_TX_L (OUT 80 122)

SMC_TO_BLC_RX_L (122) ← SMC_BLC_MUX_RX_L (IN 80 122)

NC — NC

BLC_EXT_BOOT (IN 48 80 117)

PCH and CPU PM signals to SMC

To let SMC log if a CATERR or SYS_PWROK abruptly occurs

PM_PCH_SYS_PWROK (IN 120 65 19) → R5048 0 5% 1/20W MF 201 → SMC_PM_PCH_SYS_PWROK (OUT 47 122)

CPU_CATERR_L (IN 103 11) → R5049 0 5% 1/20W MF 201 → SMC_CPU_CATERR_L (OUT 47 122)

Arch Pull Up/Down

=PP3V3_S0_SMC (91 51 48 6)

MEM_EVENT_L (119 47 32 31 30 29)	R5070	10K	5% 1/20W MF 201
PM_CLKRUN_L (120 49 47)	R5071	10K	5% 1/20W MF 201
SMC_BLC_FAULT (48)	R5072	10K	NOSTUFF 5% 1/20W MF 201

=PP3V3_G3H_SMC (50 48 47 6)

ENET_ASF_GPIO (118 47)	R5075	10K	5% 1/20W MF 201
G3_POWERON_L (118 47)	R5076	10K	5% 1/20W MF 201
SMC_BATLOW_L (47)	R5077	100K	5% 1/20W MF 201
SMC_BC_ACOK (47)	R5078	100K	5% 1/20W MF 201
SMC_SYS_LED (47)	R5079	100K	5% 1/20W MF 201
SMS_INT_L (47)	R5080	10K	5% 1/20W MF 201
SMC_PME_S4_WAKE_L (122 47 35)	R5081	10K	5% 1/20W MF 201

=PP3V3_S4_AP_FET (35)

AP_EVENT_L (117 47 35)	R5085	10K	5% 1/20W MF 201
SMC_S4_WAKESRC_EN (122 47 35)	R5017	100K	5% 1/16W MF-LF 402
SMC_DELAYED_PWRGD (122 65 47 38)	R5086	100K	5% 1/16W MF-LF 402
PM_DSW_PWRGD (120 65 47)	R5084	100K	5% 1/16W MF-LF 402
SMC_PM_G2_EN (122 74 47)	R5087	100K	5% 1/20W MF 201

Note:
Pull-down needed for SMC SSI signals

Serial/JTAG Interface Pull-ups

=PP3V3_G3H_SMC (50 48 47 6)

SMC_TX_L (122 49 47)	R5090	10K	5% 1/20W MF 201
SMC_RX_L (122 49 47)	R5091	100K	5% 1/20W MF 201
MOJO_TX_L (119 48 47 45)	R5092	10K	5% 1/20W MF 201
MOJO_RX_L (119 48 47 45)	R5093	100K	5% 1/20W MF 201
SMC_TCK (122 49 47)	R5095	10K	5% 1/20W MF 201
SMC_TDI (122 49 47)	R5096	10K	5% 1/20W MF 201
SMC_TDO (122 49 47)	R5097	10K	5% 1/20W MF 201
SMC_TMS (122 49 47)	R5098	10K	5% 1/20W MF 201

SYNC_MASTER=D8_MLB — SYNC_DATE=08/27/2012

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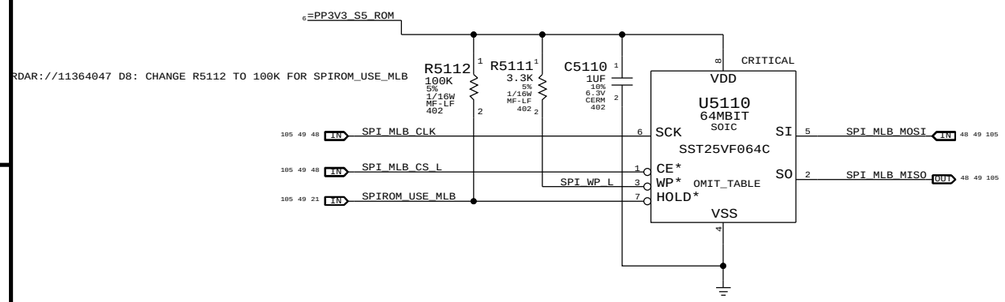
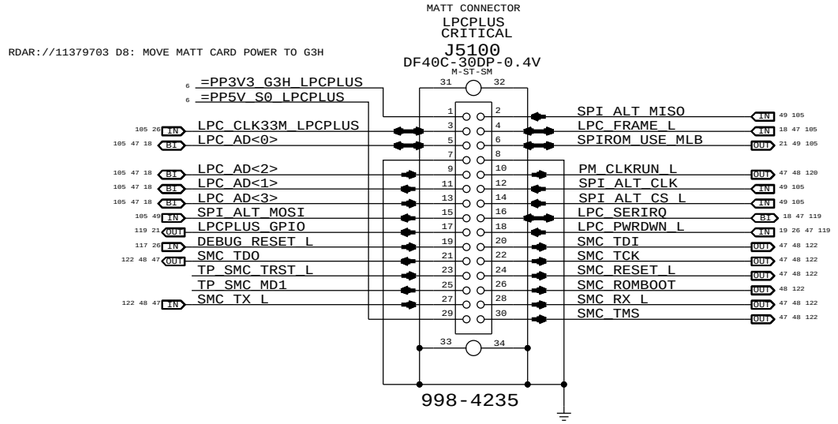
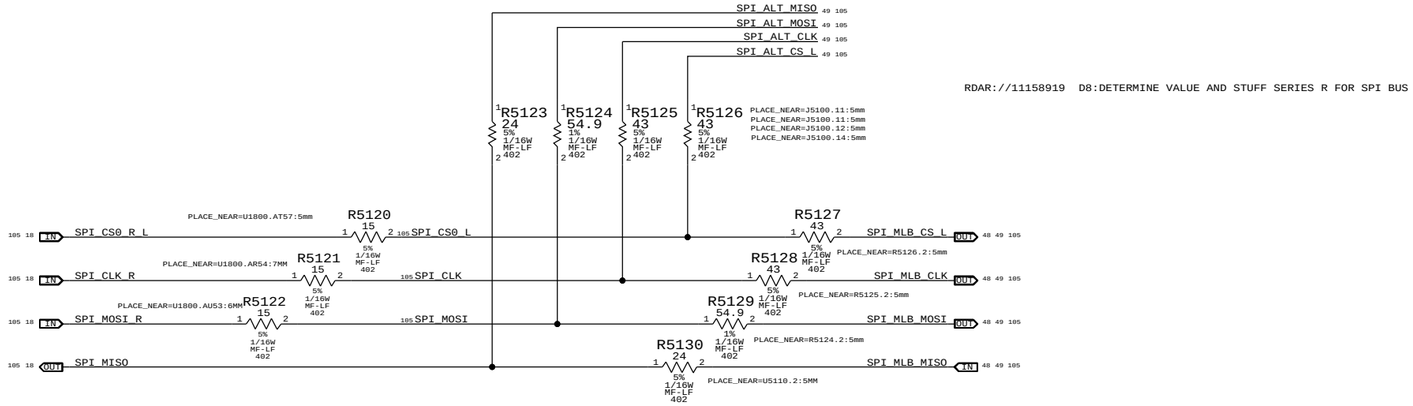
SPI BootROM



LPC+SPI Connector



SPI Series Termination



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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SPI and Debug Connector

Apple Inc.

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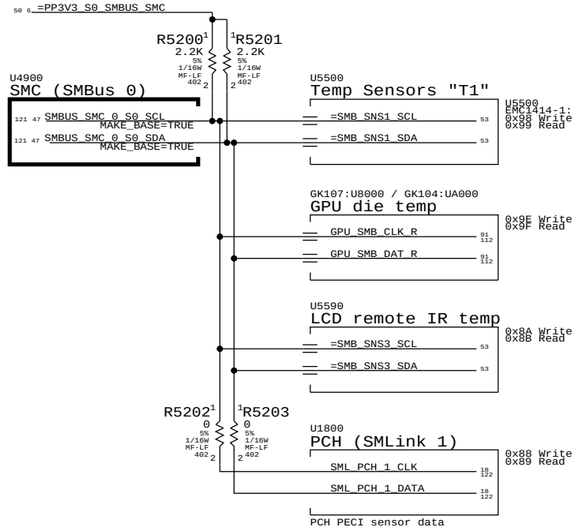

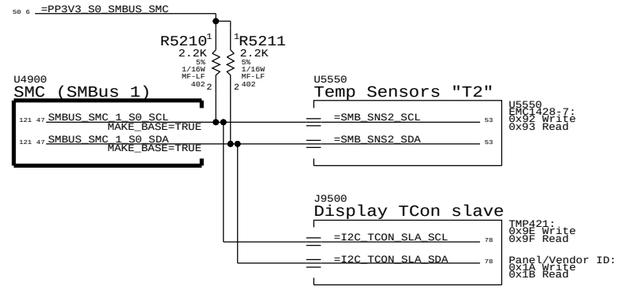

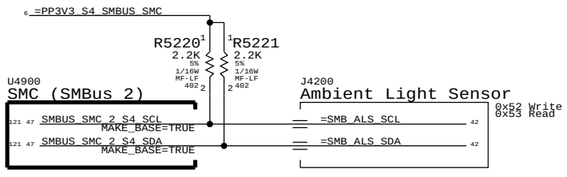

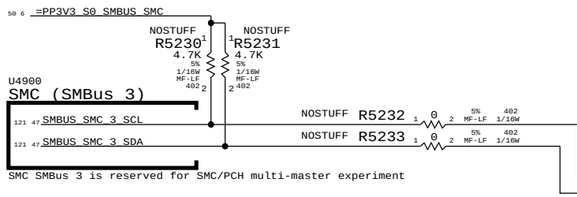

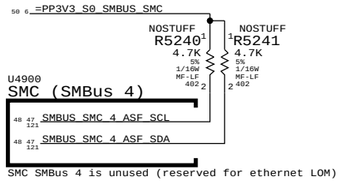

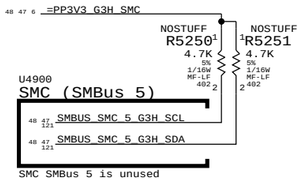

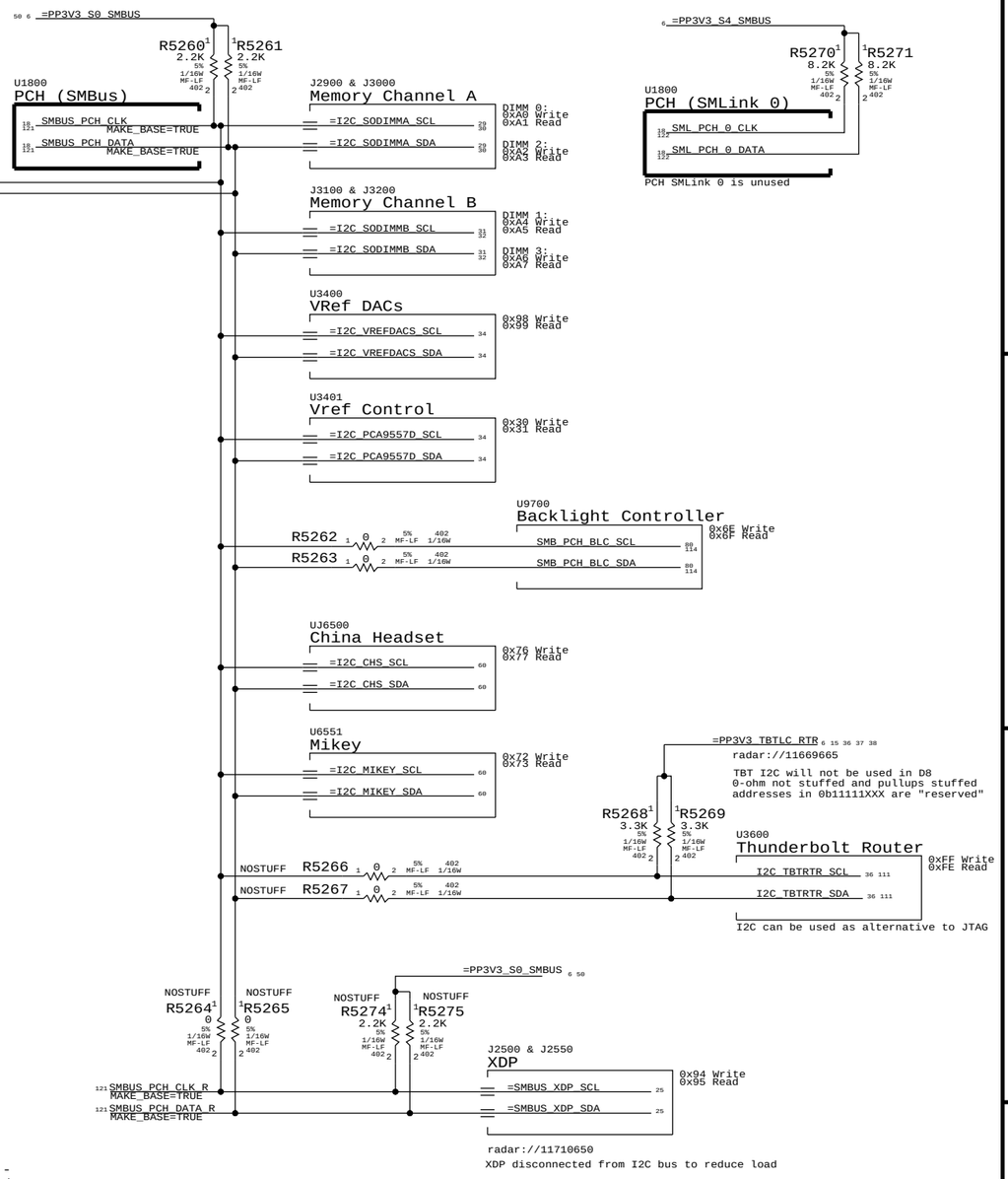

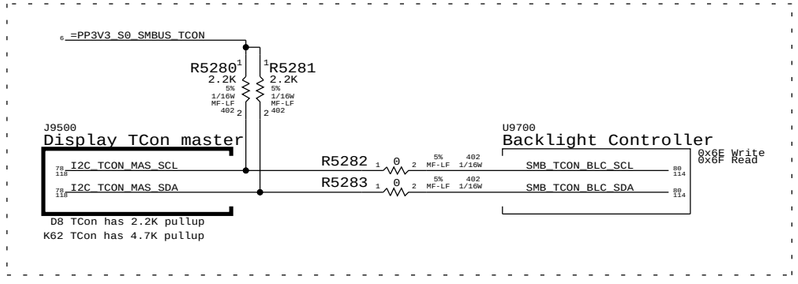

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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SMBus Connections

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ADC 0/1 12V G3H (ID2R/VD2R)

AC/DC lowside sense (System total)

AC/DC CURRENT SENSOR TO 100V/V: RDAR://10645440

TDP: 25 A
SCALE:33 A

R5300 0.001 1% 1W MF-1 0612

=PP12V_G3H_PWR → PP12V_G3H_SNS (OUT 6)

R5301 10K 1% 1/16W MF-LF 402 — U4900.E2:10mm

=PP12V_S5_SNS → SMCVSNS_P12VG3H (OUT 48 122)

R5302 3.32K 1% 1/16W MF-LF 402 — U4900.E2:10mm C5302 0.1UF 20% 10V CERM 402

=PP3V3_S5_SENSE → C5300 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

U5300 INA214 SC70 (V+, IN-, IN+, OUT, REF, GND)

ISNSA_P12VG3H_N, ISNSA_P12VG3H_P → ISNS_P12VG3H_R → R5303 4.53K 1% 1/16W MF-LF 402 — U4900.E1:10mm

SMCISNS_P12VG3H (OUT 48 122) — U4900.E1:10mm C5303 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

353S2208
GAIN: 100 V/V

ADC 9 FBVDDQ 12V S0 (IG0F)

GPU FB highside sense

PEAK: 2.35 A
TDP: 1.70 A
SCALE:3.30 A

R5320 0.005 1% 1W MF 0612-2

=PP12V_S0_FBVDDQ_PWR → PP12V_S0_FBVDDQ_SNS (OUT 6)

=PP3V3_S0_SENSE (52 51 6 55 53) → C5320 0.22UF 20% 6.3V X5R 402

U5320 INA210 SC70 (V+, IN-, IN+, OUT, REF, GND)

ISNSA_P12VS0_FBVDDQ_N, ISNSA_P12VS0_FBVDDQ_P → ISNS_P12VS0_FBVDDQ_R → R5323 4.53K 1% 1/16W MF-LF 402 — U4900.A5:10mm

SMCISNS_P12VS0_FBVDDQ (OUT 48 122) — U4900.A5:10mm C5323 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

353S2073
Gain: 200 V/V

ADC 16/17 PCH 1.05V S0 (IN1R/VN1R)

PCH Vcc 1.05V lowside sense

PEAK: 5.93 A
TDP: 4.15 A
SCALE:8.25 A

R5340 0.002 1% 1W MF-1 0612

=PP1V05_S0_PCH_PWR → PP1V05_S0_PCH_SNS (OUT 6)

=PP3V3_S0_SENSE (52 51 6 55 53) → C5340 0.22UF 20% 6.3V X5R 402

U5340 INA210 SC70 (V+, IN-, IN+, OUT, REF, GND)

ISNSA_P1V05S0_PCH_N, ISNSA_P1V05S0_PCH_P → ISNS_P1V05S0_PCH_R → R5343 4.53K 1% 1/16W MF-LF 402 — U4900.G1:10MM

SMCISNS_P1V05S0_PCH (OUT 48 122) — U4900.G1:10MM C5343 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

R5342 4.53K 1% 1/16W MF-LF 402 — U4900.G2:10MM

SMCVSNS_P1V05S0_PCH (OUT 48 122) — U4900.G2:10MM C5342 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

353S2073
Gain: 200 V/V

ADC 2/3 GPUCORE IMON S0 (IG0C/VG0C)

GPU Core

GK104: PEAK: 120 A TDP: 95 A SCALE:141 A
GK107: PEAK: 30 A TDP: 24 A SCALE:141 A

=PPVCORE_S0_GPU → R5308 4.53K 1% 1/16W MF-LF 402 — U4900.F2:10mm

SMCVSNS_GPUCORE (OUT 48 122) — U4900.F2:10mm C5308 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

=PP5V_S0_ISENSE (51 6) → C5305 0.01UF 20% 16V X7R-CERM 0402

VR IMON SCALE TENTATIVE

OpAmp Gain = 3.1 V/V

VMAX = 0.9V @ 120 A

VR_GPU_IMON (LIN 115 96) → R5305 10K 1% 1/16W MF-LF 402

U5305 OPA348 SC70-5 (CRITICAL)

ISNS_GPUCORE_P, ISNS_GPUCORE_N → R5309 5.1K 5% 1/16W MF-LF 402 — U4900.F1:10mm

SMCISNS_GPUCORE (OUT 48 122) — U4900.F1:10mm C5309 0.22UF 10% 6.3V X5R-CERM 0402

GND_SMC_AVSS (47 48 51 55 118)

R5306 10K 1% 1/16W MF-LF 402

R5307 21K 1% 1/16W MF-LF 402 → ISNS_GPUCORE_FB

ADC 10/11 CPUCORE IMON S0 (VC0C/IC0C)

CPU VCCore

PEAK: 112 A
TDP: 83 A
SCALE:142 A

=PPVCORE_S0_CPU → R5328 4.53K 1% 1/16W MF-LF 402 — U4900.B6:10mm

SMCVSNS_CPUCORE (OUT 48 122) — U4900.B6:10mm C5328 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

=PP5V_S0_ISENSE (51 6) → C5325 0.01UF 20% 16V X7R-CERM 0402

OpAmp Gain = 3.1 V/V

VMax = 0.9V @ 120A

REG_CPUCORE_IMON (LIN 109 66) → R5325 10K 1% 1/16W MF-LF 402

U5325 OPA348 SC70-5 (CRITICAL)

ISNS_CPUCORE_P, ISNS_CPUCORE_N → R5329 5.1K 5% 1/16W MF-LF 402 — U4900.A6:10mm

SMCISNS_CPUCORE (OUT 48 122) — U4900.A6:10mm C5329 0.22UF 10% 6.3V X5R-CERM 0402

GND_SMC_AVSS (47 48 51 55 118)

R5326 10K 1% 1/16W MF-LF 402

R5327 21K 1% 1/16W MF-LF 402 → ISNS_CPUCORE_FB

ADC18 HDD 12V S0 (IH02/VH02)

HIGHSIDE SENSE FOR HDD 12V

PEAK: 2.0 A
TDP: 0.8 A
SCALE:3.3 A

R5345 0.005 1% 1W MF 0612-2

=PP12V_S0_HDD_PWR → PP12V_S0_HDD_SNS (OUT 6)

=PP3V3_S0_SENSE (52 51 6 55 53) → C5345 0.22UF 20% 6.3V X5R 402

U5345 INA210 SC70 (V+, IN-, IN+, OUT, REF, GND)

ISNSA_P12VS0_HDD_N, ISNSA_P12VS0_HDD_P → ISNS_P12VS0_HDD_R → R5348 4.53K 1% 1/16W MF-LF 402 — U4900.H1:10MM

SMCISNS_P12VS0_HDD (OUT 48 122) — U4900.H1:10MM C5348 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

353S2073
Gain: 200 V/V

ADC 4/5 CPU DDR3 S0 (IC0M/VC0M)

CPU VDD (DDR3) lowside sense

PEAK: 4.75 A
TDP: 3.25 A
SCALE:6.00 A

R5310 0.001 1% 1W MF-1 0612

=PP1V5_S0_CPU_MEM_PWR → PP1V5_S0_CPU_MEM_SNS (OUT 6)

=PP3V3_S0_SENSE (52 51 6 55 53) → C5310 0.22UF 20% 6.3V X5R 402

U5310 INA211 SC70 (V+, IN-, IN+, OUT, REF, GND)

ISNSA_P1V5S0_CPU_MEM_N, ISNSA_P1V5S0_CPU_MEM_P → ISNS_P1V5S0_CPU_MEM_R → R5313 4.53K 1% 1/16W MF-LF 402 — U4900.A3:10mm

SMCISNS_P1V5S0_CPU_MEM (OUT 48 122) — U4900.A3:10mm C5313 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

R5312 4.53K 1% 1/16W MF-LF 402 — U4900.B3:10mm

SMCVSNS_P1V5S0_CPU_MEM (OUT 48 122) — U4900.B3:10mm C5312 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

353S2216
Gain: 500 V/V

ADC12/13 CPUAXG IMON S0 (VC0G/IC0G)

CPU VCCAXG

PEAK: 35.0 A
TDP: 25.0 A
SCALE:41.4 A

=PPVAXG_S0_CPU (48 122 13 6 66 17) → R5333 4.53K 1% 1/16W MF-LF 402 — U4900.C1:10mm

SMCVSNS_CPUAXG (OUT 48 122) — U4900.C1:10mm C5333 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

=PP5V_S0_ISENSE (51 6) → C5330 0.01UF 20% 16V X7R-CERM 0402

OpAmp Gain = 3.1 V/V

VMax = 0.9V @ 35A

REG_CPUAXG_IMON (LIN 109 66) → R5330 10K 1% 1/16W MF-LF 402

U5330 OPA348 SC70-5 (CRITICAL)

ISNS_CPUAXG_P, ISNS_CPUAXG_N → R5334 5.1K 5% 1/16W MF-LF 402 — U4900.C2:10mm

SMCISNS_CPUAXG (OUT 48 122) — U4900.C2:10mm C5334 0.22UF 10% 6.3V X5R-CERM 0402

GND_SMC_AVSS (47 48 51 55 118)

R5331 10K 1% 1/16W MF-LF 402

R5332 21K 1% 1/16W MF-LF 402 → ISNS_CPUAXG_FB

ADC20/21 SSD 3.3V S0 (IH1R/VR3R)

Voltage sense of 3.3V S0
(radar://problem/1056794)
Current sense of SSD 3.3V FET

PEAK: 3.0A
TDP: 2.1 A
SCALE:3.3 A

R5350 0.002 1% 1W MF 0612

=PP3V3_S0_SSD_PWR → PP3V3_S0_SSD_SNS (OUT 6)

=PP3V3_S0_SMC (91 48 6)

U5350 INA216A4YFFX WCSP-4 (IN+, IN-, OUT, GND)

ISNSA_P3V3S0_SSD_P, ISNSA_P3V3S0_SSD_N → ISNS_P3V3S0_SSD_R → R5353 4.53K 1% 1/16W MF-LF 402 — U4900.A7:10MM

SMCISNS_P3V3S0_SSD (OUT 48 122) — U4900.A7:10MM C5353 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

R5351 4.53K 1% 1/16W MF-LF 402 — U4900.B7:10MM

SMCVSNS_P3V3S0 (OUT 48 122) — U4900.B7:10MM C5352 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

353S3597
Gain: 200 V/V

ADC 6/7 SODIMM DDR3 S3 (IM0R/VM0R)

DIMM 1.5V lowside sense

PEAK: 11.3 A
TDP: 10.0 A
SCALE:13.2 A

R5315 0.0005 1% 1W MF 0612

=PPVDDQ_S3_DDR_PWR → PPVDDQ_S3_DDR_SNS (OUT 6)

R5316 0 5% 1/16W MF-LF 402

=PP3V3_S4_SENSE → NOSTUFF

R5319 0 5% 1/16W MF-LF 402

=PP3V3_S0_SENSE (52 51 6 55 53) → PP3V3_PVDDQS3_ISNS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C5315 0.22UF 20% 6.3V X5R 402

U5315 INA211 SC70 (V+, IN-, IN+, OUT, REF, GND)

ISNSA_PVDDQS3_DDR_N, ISNSA_PVDDQS3_DDR_P → ISNS_PVDDQS3_DDR_R → R5318 4.53K 1% 1/16W MF-LF 402 — U4900.A4:10MM

SMCISNS_PVDDQS3_DDR (OUT 48 122) — U4900.A4:10MM C5318 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

R5317 4.53K 1% 1/16W MF-LF 402 — U4900.B4:10MM

SMCVSNS_PVDDQS3_DDR (OUT 48 122) — U4900.B4:10MM C5317 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

353S2216
Gain: 500 V/V

ADC14/15 HDD 5V S0 (VH05/IH05)

Highside sense for HDD 5V

PEAK: 1.2 A
TDP: 0.5 A
SCALE:3.3 A

R5335 0.005 1% 1W MF 0612-2

=PP5V_S0_HDD_PWR → PP5V_S0_HDD_SNS (OUT 6)

U5335 INA216A4YFFX WCSP-4 (IN+, IN-, OUT, GND)

ISNSA_P5VS0_HDD_P, ISNSA_P5VS0_HDD_N → ISNS_P5VS0_HDD_R → R5338 4.53K 1% 1/16W MF-LF 402 — U4900.B2:10MM

SMCISNS_P5VS0_HDD (OUT 48 122) — U4900.B2:10MM C5338 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

R5336 4.53K 1% 1/16W MF-LF 402 — U4900.B1:10MM

SMCVSNS_P5VS0_HDD (OUT 48 122) — U4900.B1:10MM C5337 0.22UF 20% 6.3V X5R 402

GND_SMC_AVSS (47 48 51 55 118)

R5337 6.65K 1% 1/16W MF-LF 402

NOTE, MUST KEEP 5V OUT BELOW 3.3V

353S2073
Gain: 200 V/V

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
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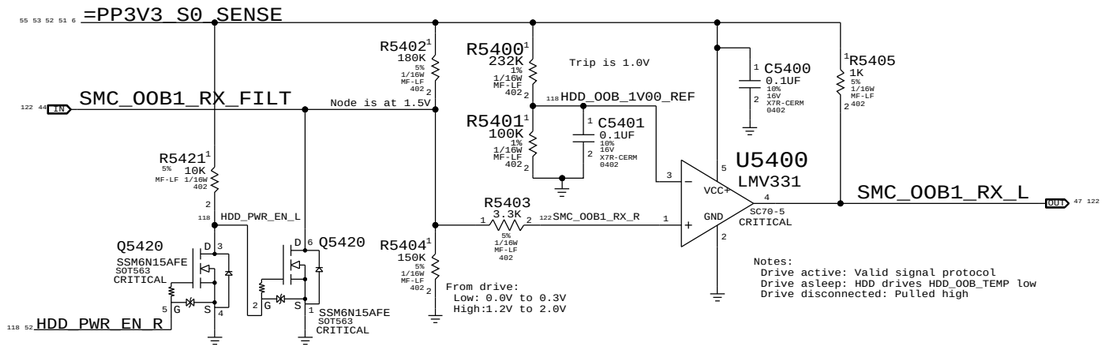
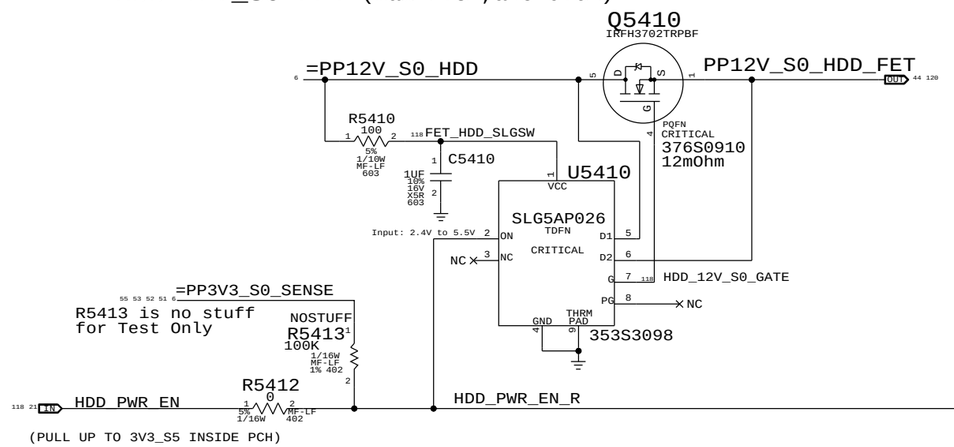
HDD Out-of-Band Temp Sensing

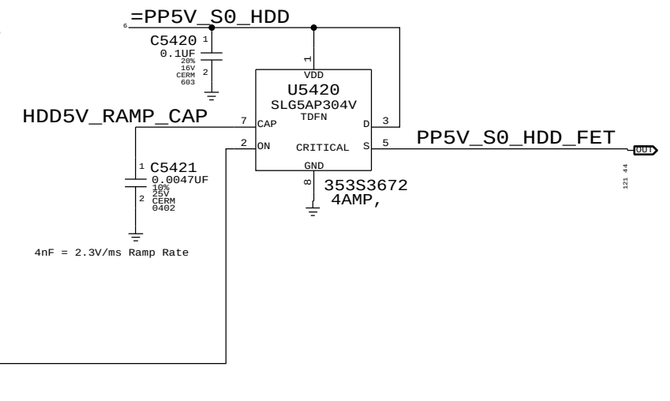
Temperature read from SATA power connecter pin 11



HDD 12V_S0 FET (max 2.8A,ave 0.6A)



HDD 5V_S0 FET (max 0.7A,ave 0.3A)



REMOVE R5413 AND SHORT R5412 AFTER HDD_PWR_EN WORKS

SYNC-MASTER=D8-MLB- SYNC-DATE=08/27/2012

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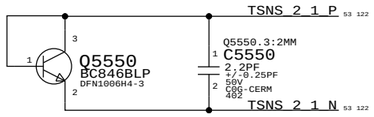
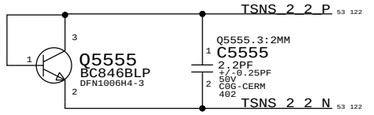
Temperature Sensor T2 EMC1428: Near GPU VR

GPU Proximity



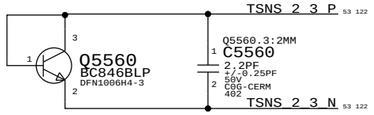
PLACEMENT_NOTE=Place Q5550 near GPU and GDDR5

Ambient



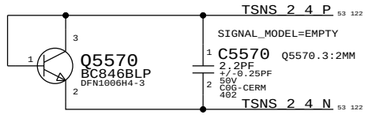
PLACEMENT_NOTE=Place Q5555 near bottom of board

BLC Proximity



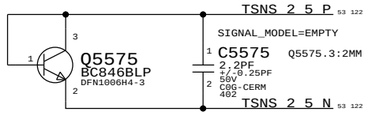
PLACEMENT_NOTE=Place Q5560 near BLC VR

SO-DIMM Proximity 1



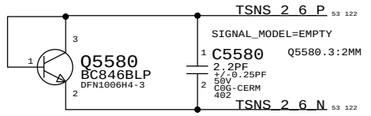
PLACEMENT_NOTE=Place Q5570 near SO-DIMM connectors (top left)

SO-DIMM Proximity 2



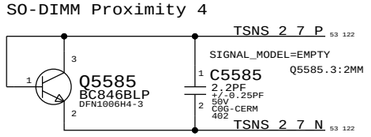
PLACEMENT_NOTE=Place Q5575 near SO-DIMM connectors (top right)

SO-DIMM Proximity 3



PLACEMENT_NOTE=Place Q5580 near SO-DIMM connectors (bottom left)

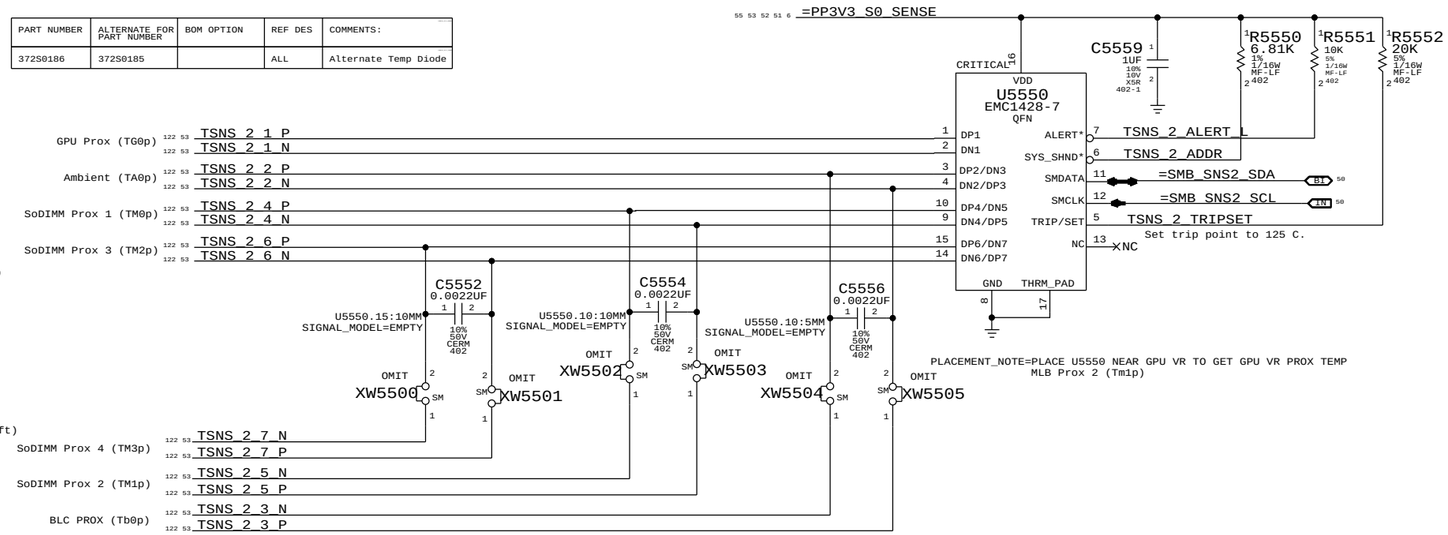
SO-DIMM Proximity 4



PLACEMENT_NOTE=Place Q5585 near SO-DIMM connectors (bottom right)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

SNS T2: TEMP SENSOR IC

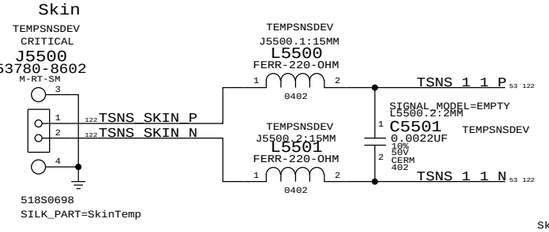


PLACEMENT_NOTE=PLACE U5550 NEAR GPU VR TO GET GPU VR PROX TEMP
MLB Prox 2 (Tm1p)

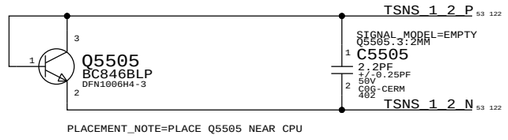
EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

Temperature Sensor T1 EMC1414: Near PSU Conn

Skin

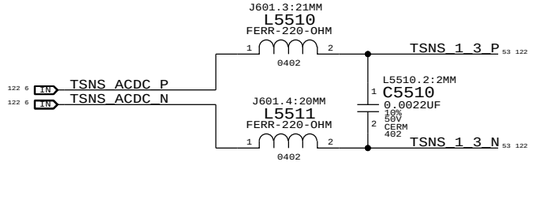


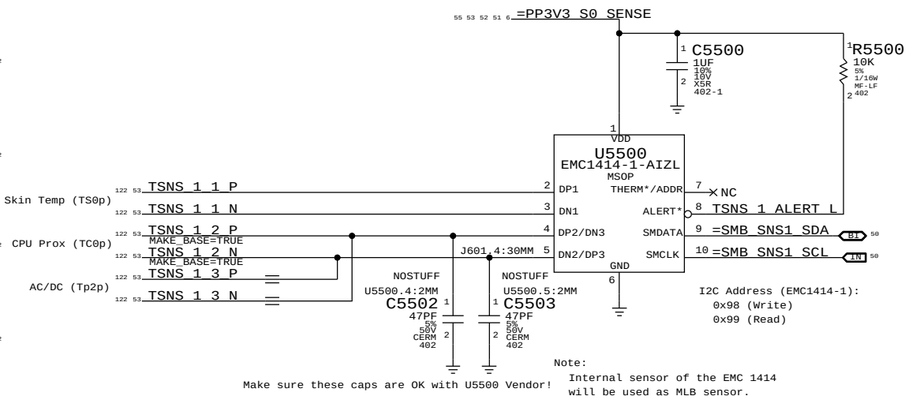
CPU Proximity



PLACEMENT_NOTE=PLACE Q5505 NEAR CPU

AC/DC Via connector to diode inside PSU





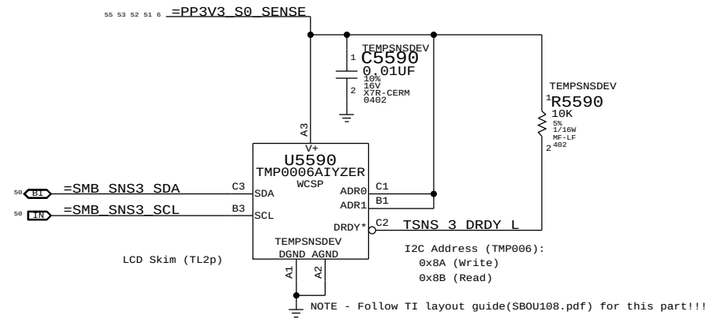
I2C Address (EMC1414-1):
0x98 (Write)
0x99 (Read)

Make sure these caps are OK with U5500 Vendor!

Note:
Internal sensor of the EMC 1414
will be used as MLB sensor.
MLB Prox 1 (Tm0p)

PLACEMENT_NOTE=PLACE U5500 NEAR PSU CONNECTOR

Temperature Sensor T3: LCD Remote Sensor(Dev4Now)



I2C Address (TMP006):
0x8A (Write)
0x8B (Read)

NOTE - Follow TI layout guide(SBOU108.pdf) for this part!!!

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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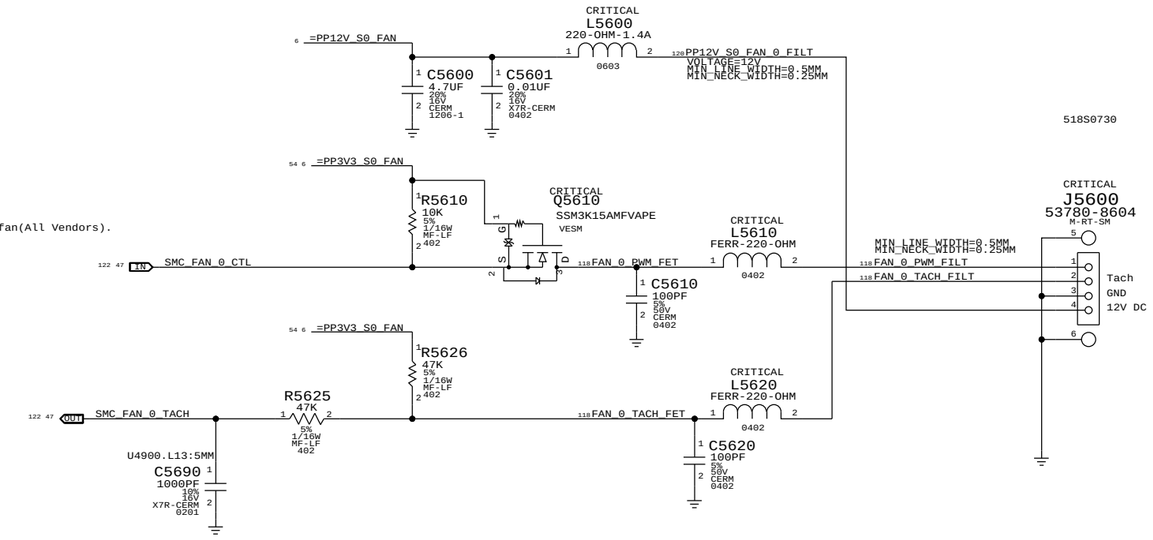
SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q5610 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q5610 is at common and the SMC sinks current when Q5610 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



SMC Fan 1 (Unused)

47 IN SMC_FAN_1_CTL — NC_SMC_FAN_1_CTL
MAKE_BASE=TRUE NO_TEST=TRUE

47 OUT SMC_FAN_1_TACH — NC_SMC_FAN_1_TACH
MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
System Fan

Apple Inc.

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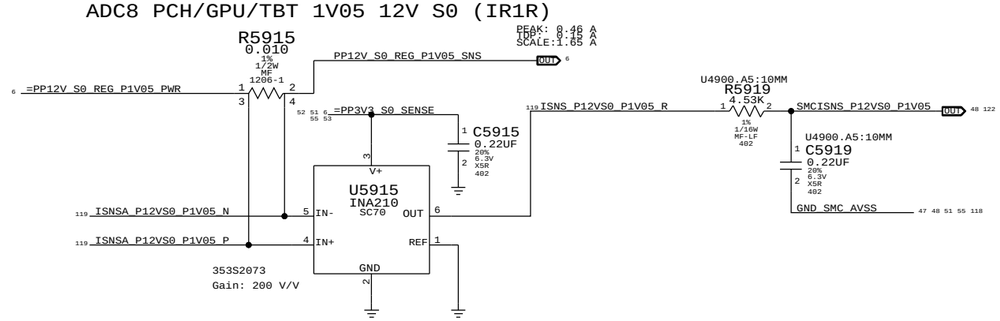
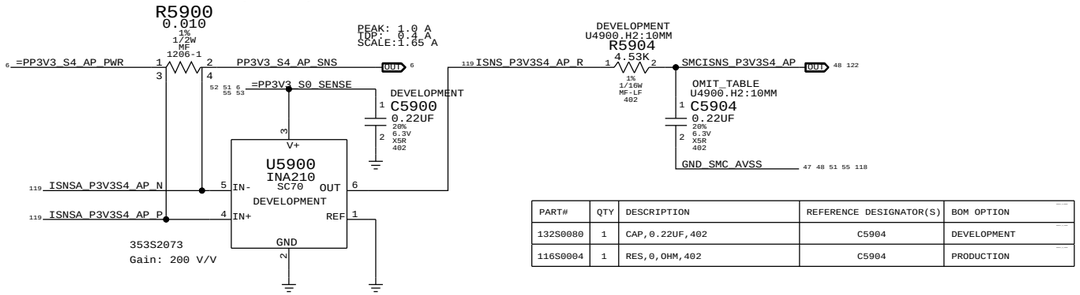
ADC8 PCH/GPU/TBT 1V05 12V S0 (IR1R)



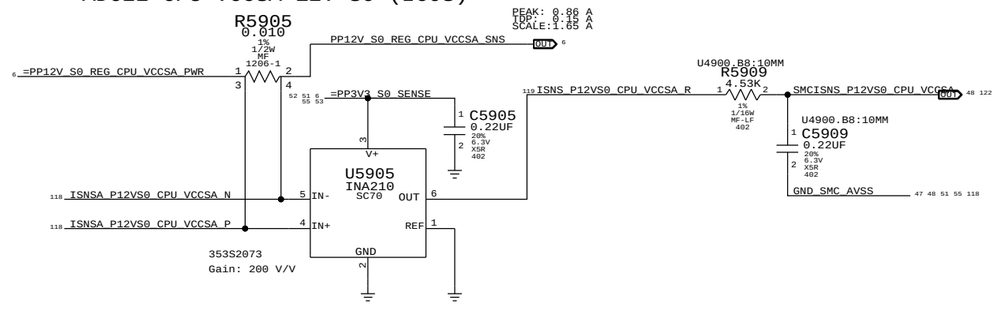
ADC19 AP 3.3V S4 (IW0R)

Current sense of AP 3.3V FET

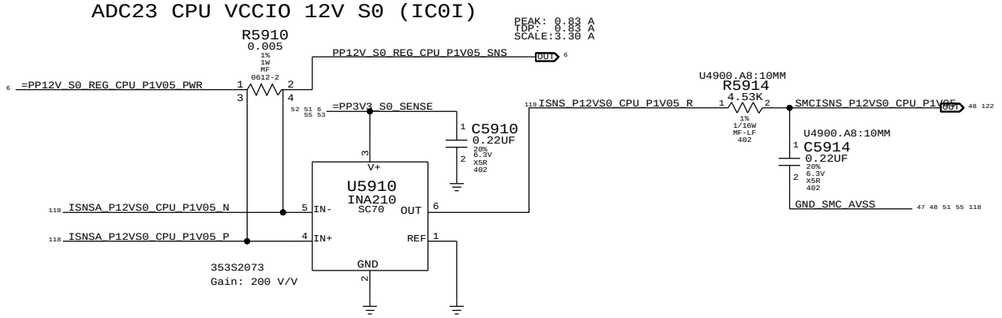


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	1	CAP,0.22UF,402	C5904	DEVELOPMENT
116S0004	1	RES,0,OHM,402	C5904	PRODUCTION

ADC22 CPU VCCSA 12V S0 (IC0S)



ADC23 CPU VCCIO 12V S0 (IC0I)



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

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Apple Inc.

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AUDIO CODEC

APPLE P/N 353S2592

PLACE C6200 AS CLOSE TO PIN 9 AS POSSIBLE

VD MUST BE LESS THAN OR EQUAL TO VL_HD

=PP1V5_S0_AUD_DIG

C6101 4.7UF 20% 4V X5R-1 402

C6100 0.47UF 10% 10V X5R 0402

GND_AUDIO_CODEC

PP4V5_AUDIO_ANALOG

R6100 2.67K 1% 1/16W MF-LF 402

C6109 2.2UF 20% 6.3V CERM 402-LF

C6110 2.2UF 20% 6.3V CERM 402-LF

C6108 10UF 20% 16V POLY-TANT CASE-B2-SM

VBIAS_DAC

CS4206_FP

CS4206_FN

C6102 0.47UF 10% 10V X5R 0402

C6103 10UF 20% 16V POLY-TANT CASE-B2-SM

C6105 1UF 10% 10V X5R 402-1

C6104 0.47UF 10% 10V X5R 0402

C6106 0.47UF 10% 10V X5R 0402

C6107 CRITICAL 10UF 20% 16V X5R-CERM 0402-1

PP5V_AUDIO_HPAMP

=PP3V3_S0_AUDIO

PP4V5_AUDIO_ANALOG

GND_AUDIO_CODEC

R6105 0 5% 1/16W MF-LF 402

U6101 CRITICAL CS4206B QFN

VD VA_REF VA_HP VA

VBIAS_DAC	29		
VHP_FILT+	44	HPOUT_L	38
VHP_FILT-	41	HPOUT_R	40
		HPREF	39
GPIO0/DMIC_SDA1	2	LINEOUT_L1+	35
GPIO1/DMIC_SDA2/SPDIF_OUT2	12	LINEOUT_L1-	34
GPIO2	14	LINEOUT_R1+	36
GPIO3	15	LINEOUT_R1-	37
SENSE_A	13	LINEOUT_L2+	31
		LINEOUT_L2-	30
		LINEOUT_R2+	32
		LINEOUT_R2-	33
FLYP	45		
FLYC	43		
FLYN	42		
VL_HD	3		
VL_IF	1		
MICBIAS	16		
VCOM	28		
BITCLK	6	LINEIN_L+	21
SYNC	10	LINEIN_C-	22
SDI	8	LINEIN_R+	23
SDO	5		
RESET*	11	MICIN_L+	18
		MICIN_L-	17
		MICIN_R+	19
		MICIN_R-	20
SPDIF_IN	47		
SPDIF_OUT	48		
		VREF+_ADC	27
		DMIC_SCL	4
DGND THRM_PAD AGND	7 49 26		

MIN_LINE_WIDTH=0.1MM MIN_NECK_WIDTH=0.1MM

MIN_LINE_WIDTH=0.2MM MIN_NECK_WIDTH=0.1MM

CS4206_VCOM MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

CS4206_VREF_ADC NC MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM

TP_AUD_HP_L NC

TP_AUD_HP_R NC

CS4206_HPREF

AUD_LO1_L_P

AUD_LO1_L_N

AUD_LO1_R_P

AUD_LO1_R_N

AUD_LO2_L_P

AUD_LO2_L_N

AUD_LO2_R_P

AUD_LO2_R_N

AUD_CODEC_MICBIAS

NC_AUD_LI_P_L NC

NC_AUD_LI_COM NC

NC_AUD_LI_P_R NC

AUD_MIC_INL_P

AUD_MIC_INL_N

NC_AUD_MIC_INP_R NC

NC_AUD_MIC_INN_R NC

CS4206_DMIC_SCL

R6104 22 5% 1/16W MF-LF 402

AUD_DMIC_CLK

HP AMP/LINE OUT

TWEETERS

RESERVE SPACE FOR POSSIBLE LATCH CIRCUIT

WOOFERS

Q6170_P_S

Q6170 DMC2400UV SOT563

R6170 0 5% 1/16W MF-LF 402

Q6170_P_G

Q6170_N_G

R6171 0 5% 1/16W MF-LF 402

Q6170_N_S

Q6171_P_S

Q6171 DMC2400UV SOT563

R6172 0 5% 1/16W MF-LF 402

Q6171_P_G

Q6171_N_G

R6173 0 5% 1/16W MF-LF 402

Q6171_N_S

DEVEL_AUDIO CRITICAL

P-CHN

N-CHN

NC

DMICS 1 & 2

AUD_DMIC_SDA1

NC TP_AUD_GPIO_1

HP AMP CNTRL

AUD_GPIO_2

MAC SPKR AMP CNTRL

AUD_CODEC_MICBIAS

D6100 SOD-523 BAT54XV2T1

WIN SPKR AMP CNTRL

AUD_GPIO_3

AUD_SENSE_A

C6111 2.2UF 20% 6.3V CERM 402-LF

C6112 2.2UF 20% 6.3V CERM 402-LF

CS4206_FLYP

CS4206_FLYC

CS4206_FLYN

PLACE TP FOR ALL HDA SIGNALS NEAR CODEC

HDA_BIT_CLK

HDA_SYNC

HDA_SDIN0

R6101 22 5% 1/16W MF-LF 402

AUD_SDI_R

HDA_SDOUT

HDA_RST_L

DP_INT_SPDIF_AUDIO

AUD_SPDIF_CHIP

AUD_SPDIF_OUT

R6102 22 5% 1/16W MF-LF 402

R6103 100K 1% 1/16W MF-LF 402

DMICS SHOULD HAVE OWN GND ON CONNECTOR SHARED WITH CAMERA

GND_AUDIO_DMIC MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.15MM VOLTAGE=0V

XW6100 SM

GND_AUDIO_CODEC

C6113 CRITICAL 1UF 10% 25V TANT CASE-P3-HF

C6114 CRITICAL 10UF 20% 16V POLY-TANT CASE-B2-SM

C6115 0.47UF 10% 10V X5R 0402

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0134	127S0111		C6113	THAILAND ALTERNATE

APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC

L6111 FERR-220-OHM 0402

MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.20MM VOLTAGE=5V

PP5V_AUDIO_HPAMP

L6110 FERR-220-OHM 0402

=PP5V_S0_AUDIO

=PP3V3_S0_AUDIO

R6120 0 5% 1/16W MF-LF 402

VR6101 TPS71745 CRITICAL

4V5_REG_IN

4V5_REG_EN

4V5_NR

PP4V5_AUDIO_ANALOG MIN_LINE_WIDTH=0.40MM MIN_NECK_WIDTH=0.15MM VOLTAGE=4.5V

MIN_LINE_WIDTH=0.4MM MIN_NECK_WIDTH=0.2MM

C6122 1UF 10% 10V X5R 402-1

XW6110 SM

C6123 0.1UF 10% 16V X7R-CERM 0402

C6124 1UF 10% 10V X5R 402-1

GND_AUDIO_CODEC MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

XW6111 SM

GND_AUDIO_HPAMP MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2MM VOLTAGE=0V

PLACE XW6110 BENEATH U6101, BETWEEN PINS 2 & 5

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: CODEC/REGULATORS

Apple Inc.

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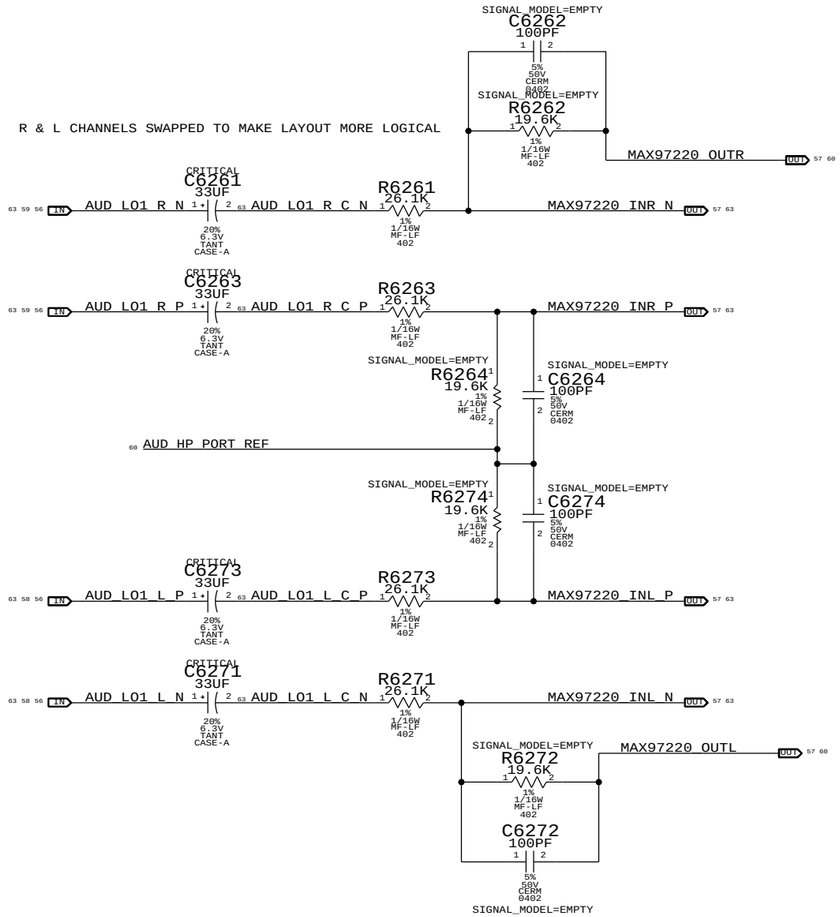

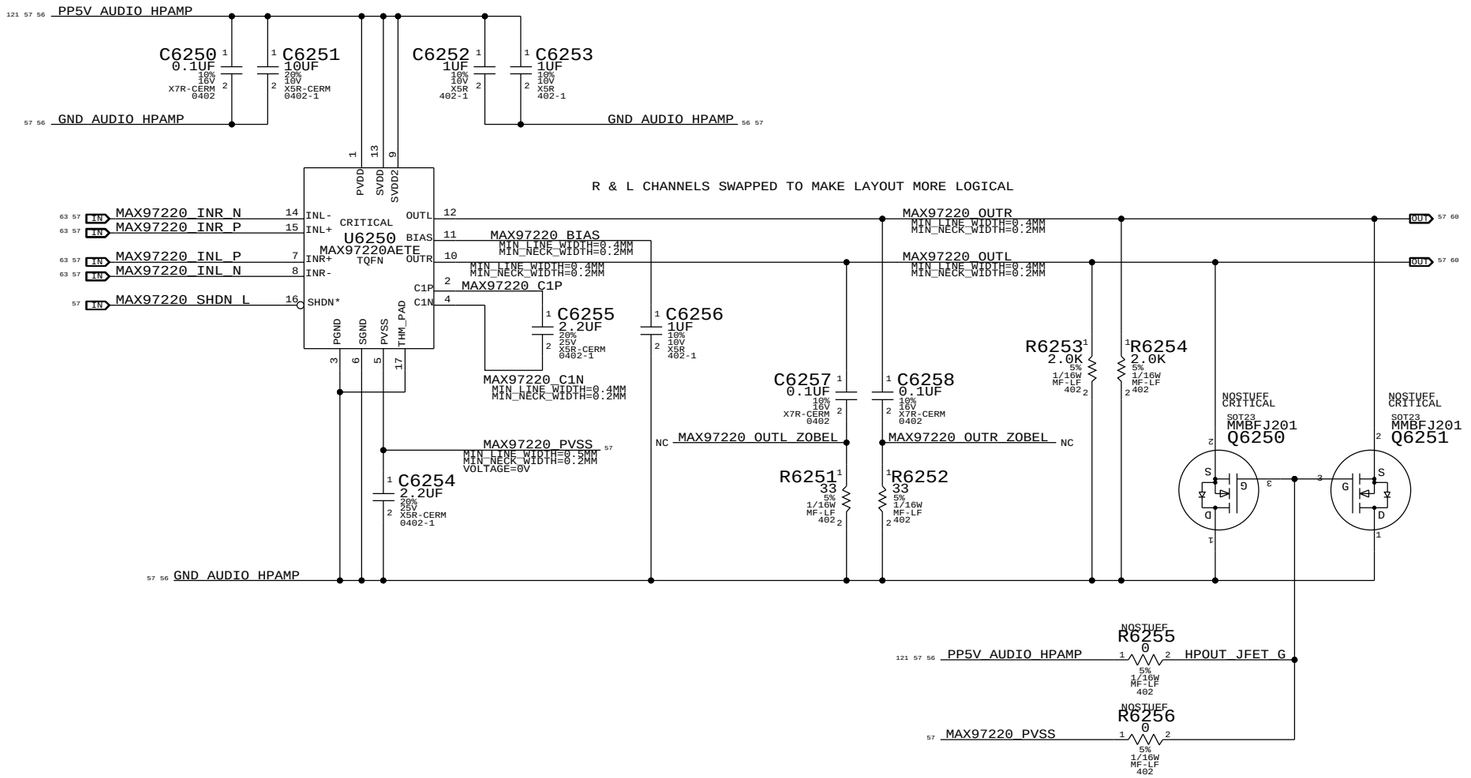

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0135	127S0120		C6261	THAILAND ALTERNATE
127S0135	127S0120		C6263	THAILAND ALTERNATE
127S0135	127S0120		C6271	THAILAND ALTERNATE
127S0135	127S0120		C6273	THAILAND ALTERNATE

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
AUDIO: HEADPHONE AMP

Apple Inc.

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LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6300 10UF 10% 25V X5R 805
C6301 10UF 10% 25V X5R 805
C6302 0.1UF 10% 25V X5R 402
C6303 1UF 10% 25V X5R 603-1
C6304 0.1UF 10% 25V X5R 402
C6305 1UF 10% 25V X5R 603-1
CRITICAL C6306 220UF 20% 16V ELEC SM-CASE-C1-HF
CRITICAL C6307 220UF 20% 16V ELEC SM-CASE-C1-HF

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6300 FERR-1000-OHM 0402 — AUD_LO2_L_N — C6308 1UF 10% 25V X5R 0402 — AUD_LAMP_RINC_P — AUD_LAMP_RIN_P
L6301 FERR-1000-OHM 0402 — AUD_LO2_L_P — C6309 1UF 10% 25V X5R 0402 — AUD_LAMP_RINC_N — AUD_LAMP_RIN_N
L6302 FERR-1000-OHM 0402 — AUD_LO1_L_P — C6310 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_LINC_P — AUD_LAMP_LIN_P
L6303 FERR-1000-OHM 0402 — AUD_LO1_L_N — C6311 4700PF 5% 50V NPO-C0G-CERM 0805 — AUD_LAMP_LINC_N — AUD_LAMP_LIN_N

=PP3V3_S0_AUDIO

CRITICAL U6300 SSM3302 LFCSP

20	INR+	
19	INR-	
22	SDNR*	AUD_SPKRAMP_WIN_SHDN_L (ONLY WOOFERS ON UNDER WINDOWS)
16	MONO	AUD_LAMP_MONO
9	SDNL*	AUD_SPKRAMP_MAC_SHDN_L (WOOFERS & TWEETERS ON UNDER MAC OS)
11	INL+	
12	INL-	
21	GAIN	AUD_LAMP_GAIN
8	VREG/AVDD	AUD_LAMP_AVDD (MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V)
23	REGEN	
34,35,36,37	PVDD	
7,24,41	AGND	
31,32,33,38,39,40	PGND	
17	THERM	TP_AUD_LAMP_THERM = NC
30	BOOTR+	C6313 0.22UF 20% 25V X5R 603
28,29	OUTR+	AUD_LAMP_OUTPR
26,27	OUTR-	AUD_LAMP_OUTNR
25	BOOTR-	C6314 0.22UF 20% 25V X5R 603
10	EDGE	AUD_LAMP_EDGE
1	BOOTL+	C6315 0.22UF 20% 25V X5R 603
2,3	OUTL+	AUD_LAMP_OUTPL
4,5	OUTL-	AUD_LAMP_OUTNL
6	BOOTL-	C6316 0.22UF 20% 25V X5R 603
18	NC	NC
13	NC	NC
14	TEST	
15	TEST	

C6317 2.2UF 20% 10V X5R-CERM 402

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

AUD_LAMP_BOOTRP — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM — C6313 0.22UF 20% 25V X5R 603
AUD_LAMP_BOOTRN — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM — C6314 0.22UF 20% 25V X5R 603
AUD_LAMP_BOOTLP — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM — C6315 0.22UF 20% 25V X5R 603
AUD_LAMP_BOOTLN — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM — C6316 0.22UF 20% 25V X5R 603

AUD_LAMP_OUTPR — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM — SIGNAL_MODEL=EMPTY — CRITICAL L6305 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_LWFR_OUT_P — SIGNAL_MODEL=EMPTY CRITICAL C6323 1000PF 5% 25V NP0-C0G 402 — AUD_SPKR_LWFR_OUT_N
AUD_LAMP_OUTNR — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
AUD_LAMP_OUTPL — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM — SIGNAL_MODEL=EMPTY — CRITICAL L6307 110-OHM-3A DLY5ATN111SQ2 — AUD_SPKR_LTWT_OUT_P — SIGNAL_MODEL=EMPTY CRITICAL C6324 1000PF 5% 25V NP0-C0G 402 — AUD_SPKR_LTWT_OUT_N
AUD_LAMP_OUTNL — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM

CRITICAL C6320 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY
CRITICAL C6322 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY
CRITICAL C6319 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY
CRITICAL C6321 1000PF 5% 25V NP0-C0G 402 — SIGNAL_MODEL=EMPTY

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

L6308 FERR-1000-OHM 0402 — AUD_CODEC_MICBIAS — AUD_SPKRAMP_MAC_SHDN_L
R6301 100K 5% 1/16W MF-LF 402 — C6312 100PF 5% 50V CERM 402 (NOSTUFF)

R6308 0 5% 1/16W MF-LF 402 — AUD_GPIO_3 — AUD_SPKRAMP_WIN_SHDN_L
R6309 100K 5% 1/16W MF-LF 402 — C6318 100PF 5% 50V CERM 402 (NOSTUFF)

EDGE RATE CONTROL	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

AUD_LAMP_AVDD
R6304 0 5% 1/16W MF-LF 402 — AUD_LAMP_EDGE
R6305 NOSTUFF 0 5% 1/16W MF-LF 402
R6303 0 5% 1/16W MF-LF 402 — AUD_LAMP_MONO
R6306 NOSTUFF 0 5% 1/16W MF-LF 402 — AUD_LAMP_GAIN
R6307 47K 5% 1/16W MF-LF 402

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012
PAGE TITLE: AUDIO: LEFT SPKR AMP

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RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)

=PP12V_S0_AUDIO_SPKRAMP

C6400 10UF 10% 25V X5R 805
C6401 10UF 10% 25V X5R 805
C6402 0.1UF 10% 25V X5R 402
C6403 1UF 10% 25V X5R 603-1
C6404 0.1UF 10% 25V X5R 402
C6405 1UF 10% 25V X5R 603-1
CRITICAL C6406 470UF 20% 16V POLY SM

INPUT POLARITY FLIP OK -- TRUE DIFF INPUTS

L6400 FERR-1000-OHM 0402 — AUD_LO2_R_N — AUD_RAMP_RINC_P — C6408 1UF 10% 25V X5R 0402 — AUD_RAMP_RIN_P
L6401 FERR-1000-OHM 0402 — AUD_LO2_R_P — AUD_RAMP_RINC_N — C6409 1UF 10% 25V X5R 0402 — AUD_RAMP_RIN_N
L6402 FERR-1000-OHM 0402 — AUD_LO1_R_P — AUD_RAMP_LINC_P — C6410 4700PF 5% 50V NPO-C0G-CERM 0805 — AUDRAMP_LIN_P
L6403 FERR-1000-OHM 0402 — AUD_LO1_R_N — AUD_RAMP_LINC_N — C6411 4700PF 5% 50V NPO-C0G-CERM 0805 — AUDRAMP_LIN_N

=PP3V3_S0_AUDIO

PVDD (34, 35, 36, 37)

CRITICAL U6400 SSM3302 LFCSP

20	INR+
19	INR-
22	SDNR*
16	MONO
9	SDNL*
11	INL+
12	INL-
21	GAIN
8	VREG/AVDD
23	REGEN
7, 24	AGND
41	THRM_PAD
31, 32, 33, 38, 39, 40	PGND
17	THERM
30	BOOTR+
28	OUTR+
26, 27	OUTR-
25	BOOTR-
10	EDGE
1	BOOTL+
2, 3	OUTL+
4, 5	OUTL-
6	BOOTL-
18	NC
13	NC
14	TEST
15	

ONLY WOOFERS ON UNDER WINDOWS
AUD_SPKRAMP_WIN_SHDN_L

WOOFERS & TWEETERS ON UNDER MAC OS
AUD_SPKRAMP_MAC_SHDN_L

AUD_RAMP_MONO
AUD_RAMP_GAIN
AUD_RAMP_AVDD — MIN_LINE_WIDTH=0.20MM, MIN_NECK_WIDTH=0.15MM, VOLTAGE=5V

C6417 2.2UF 20% 10V X5R-CERM 402

PINS 14 & 15 ARE TEST PINS AND SHOULD BE TIED TO GND

OUTPUT POLARITY FLIP TO MAKE LAYOUT MORE LOGICAL

TP_AUD_RAMP_THERM — NC

C6413 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTRP — AUD_RAMP_OUTPR
C6414 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTRN — AUD_RAMP_OUTNR
C6415 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTLP — AUD_RAMP_OUTPL
C6416 0.22UF 20% 25V X5R 603 — AUD_RAMP_BOOTLN — AUD_RAMP_OUTNL

AUD_RAMP_OUTPR, AUD_RAMP_OUTNR: MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
AUD_RAMP_OUTPL, AUD_RAMP_OUTNL: MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM

SIGNAL_MODEL=EMPTY
CRITICAL L6405 110-OHM-3A DLY5ATN111SQ2
CRITICAL L6407 110-OHM-3A DLY5ATN111SQ2

AUD_SPKR_RWFR_OUT_P
AUD_SPKR_RWFR_OUT_N
AUD_SPKR_RTWT_OUT_P
AUD_SPKR_RTWT_OUT_N

CRITICAL C6423 1000PF 5% 25V NP0-C0G 402
CRITICAL C6424 1000PF 5% 25V NP0-C0G 402
CRITICAL C6420 1000PF 5% 25V NP0-C0G 402
CRITICAL C6422 1000PF 5% 25V NP0-C0G 402
CRITICAL C6419 1000PF 5% 25V NP0-C0G 402
CRITICAL C6421 1000PF 5% 25V NP0-C0G 402

SIGNAL_MODEL=EMPTY

EDGE RATE CONTROL

	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF

AUD_RAMP_AVDD
R6404 0 5% 1/16W MF-LF 402 — AUD_RAMP_EDGE
NOSTUFF R6405 0 5% 1/16W MF-LF 402
R6403 0 5% 1/16W MF-LF 402 — AUD_RAMP_MONO
NOSTUFF R6406 0 5% 1/16W MF-LF 402
R6407 47K 5% 1/16W MF-LF 402 — AUD_RAMP_GAIN

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: RIGHT SPKR AMP

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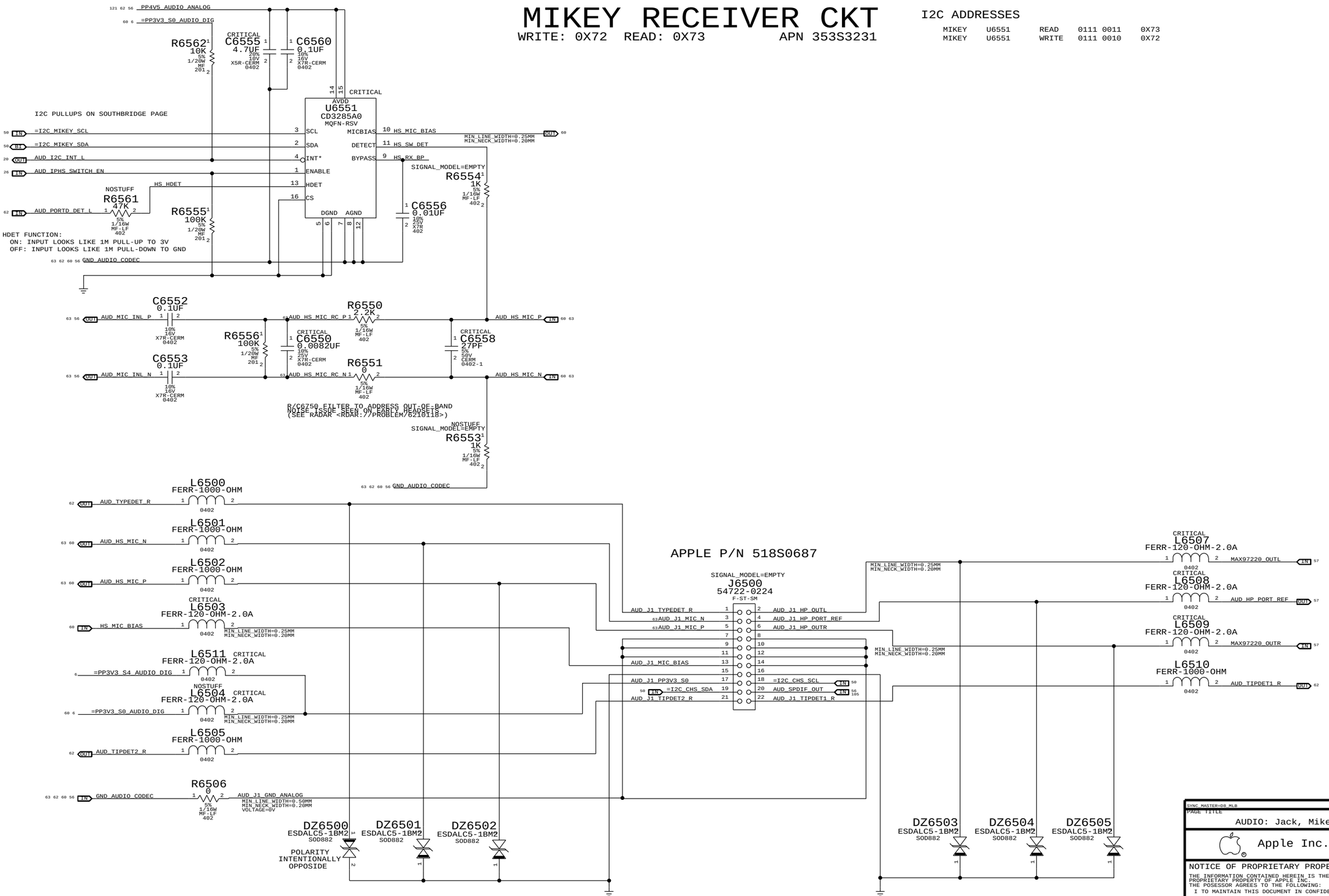
MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S3231

I2C ADDRESSES

MIKEY	U6551	READ	0111 0011	0X73
MIKEY	U6551	WRITE	0111 0010	0X72



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

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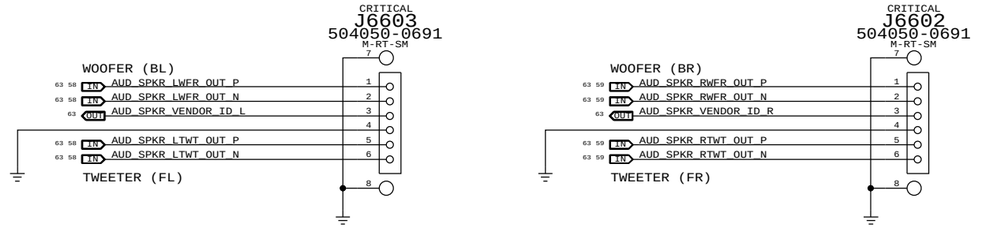
SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

Audio: Spkr/Mic Conn.

Apple Inc.

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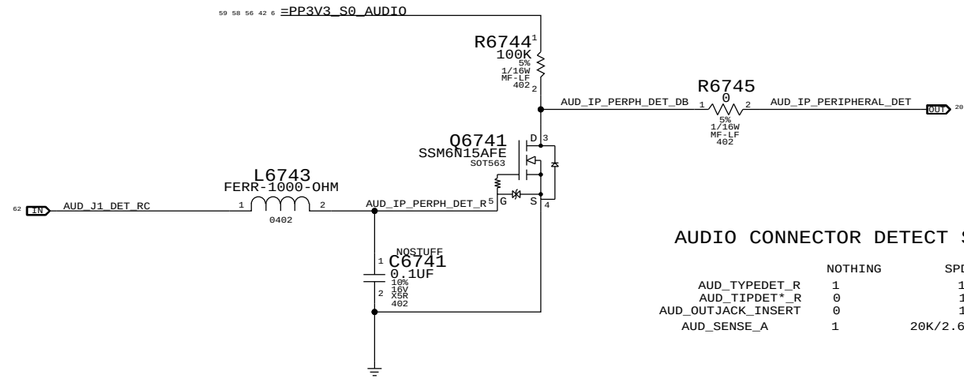
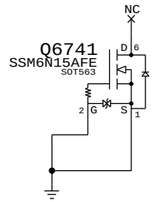
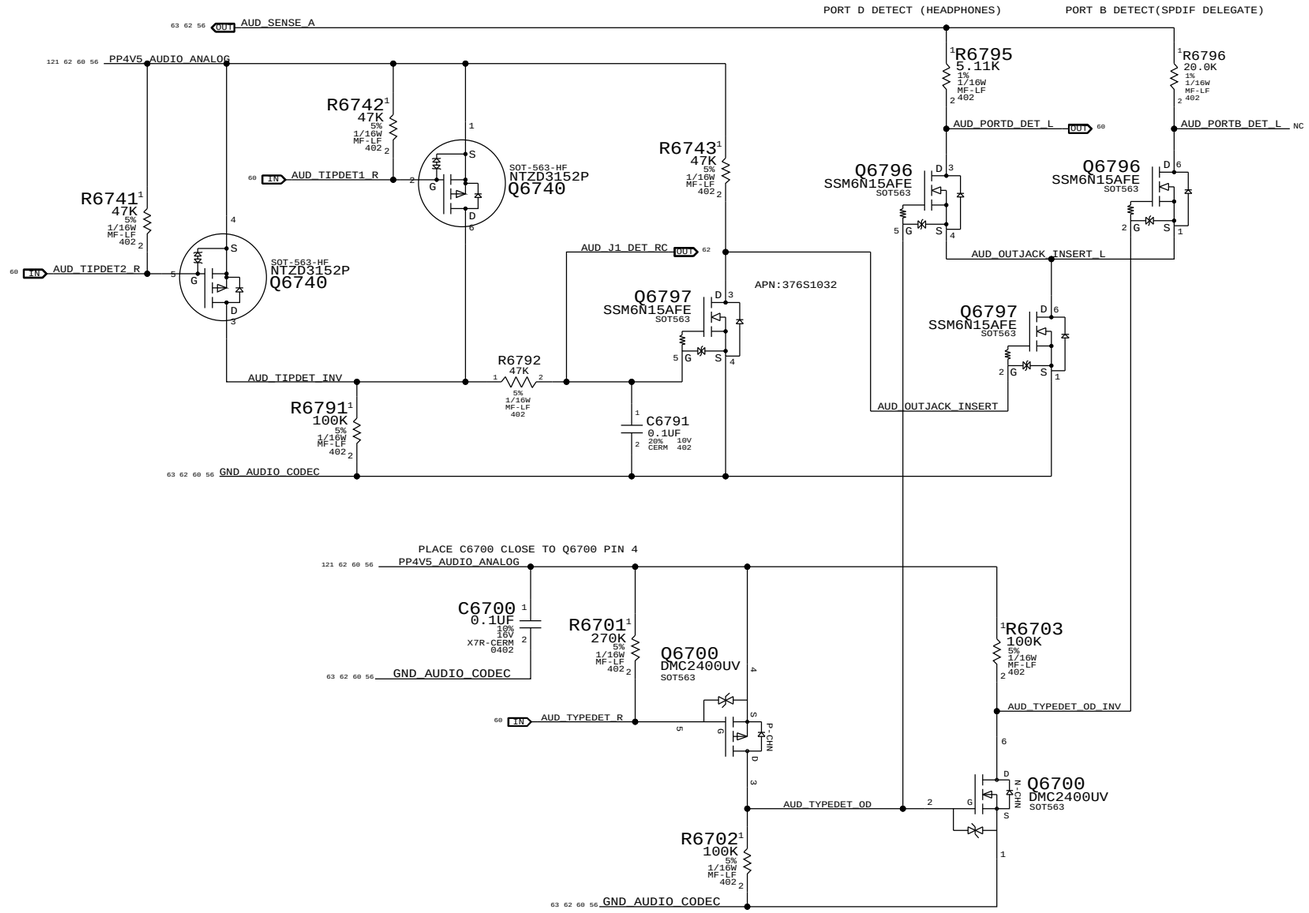
IPHS HS Detect Debounce CKT



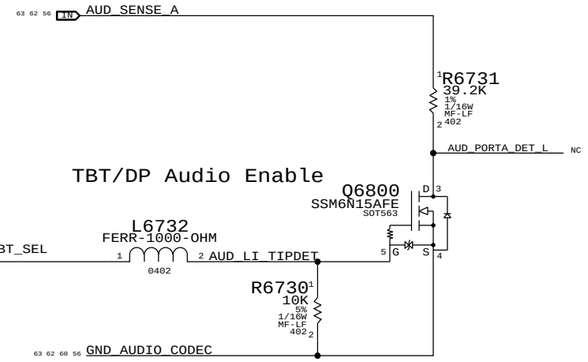
AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_TYPEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV





LI Insert Detect (DETECT A)



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: Detects/Grounding

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	PANTHER POINT GPIO 16	PANTHER POINT GPIO 5 (RCV0_INT) PANTHER POINT GPIO 3 (PERIPH DET)

OTHER DETECT

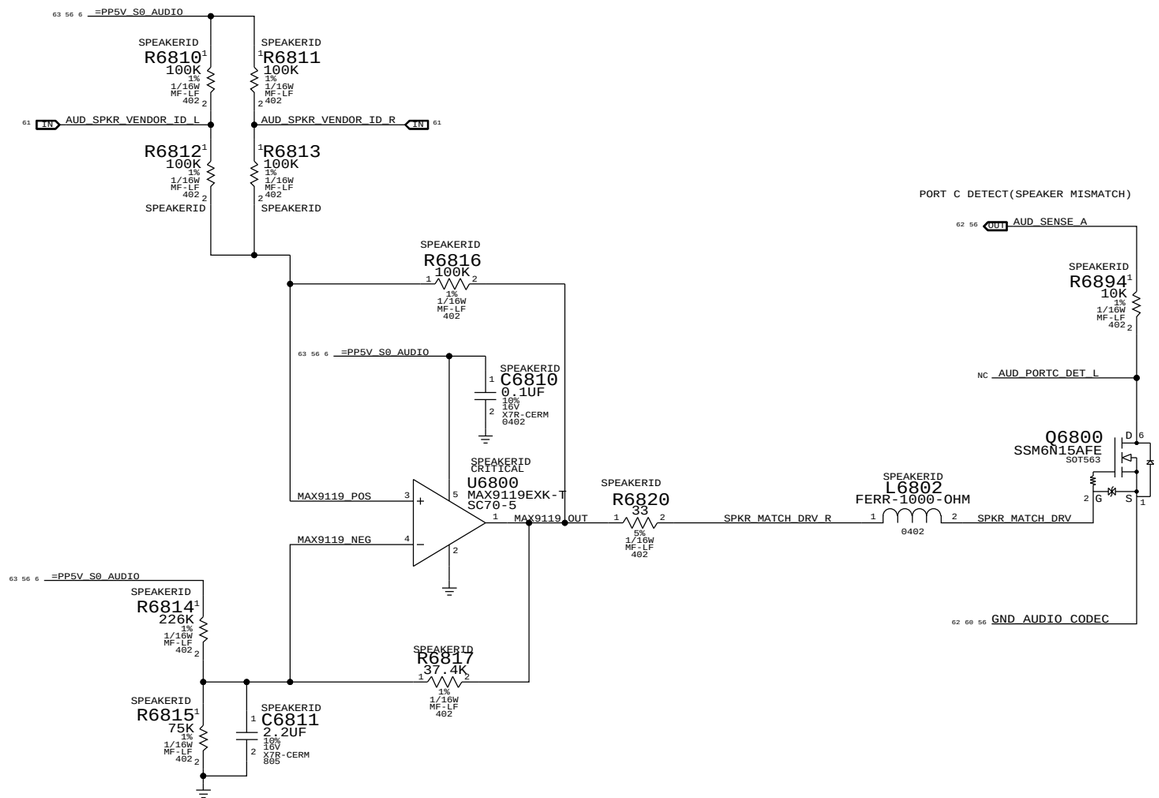
FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>



ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
1545 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	56 57 58
1546 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	56 57 58
1547 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	57
1548 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	57
1549 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 57 59
1550 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 57 59
1551 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	57
1552 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	57
1553 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 58
1554 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 58
1555 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 59
1556 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 59
1557 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	59
1558 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	59
1559 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	59
1560 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	59
1561 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	59
1562 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	59
1563 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	59
1564 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	59
1565 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	58
1566 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	58
1567 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	58
1568 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	58
1569 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	58
1570 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	58
1571 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	58
1572 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	58
1573 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_P	57
1574 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INL_N	57
1575 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_P	57
1576 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX9722D_INR_N	57
1577 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	59 61
1578 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	59 61
1579 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	59 61
1580 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	59 61
1581 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	58 61
1582 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	58 61
1583 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	58 61
1584 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	58 61
1585 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	56 60
1586 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	56 60
1587 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	60
1588 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	60
1589 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	60
1590 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	60
1591 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	60
1592 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	60

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: AUDIO: Speaker ID

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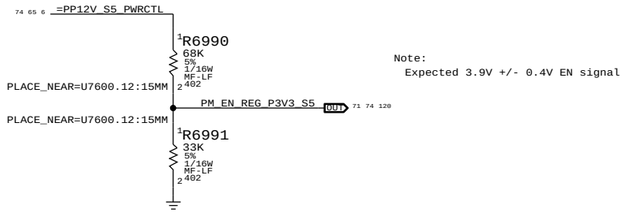
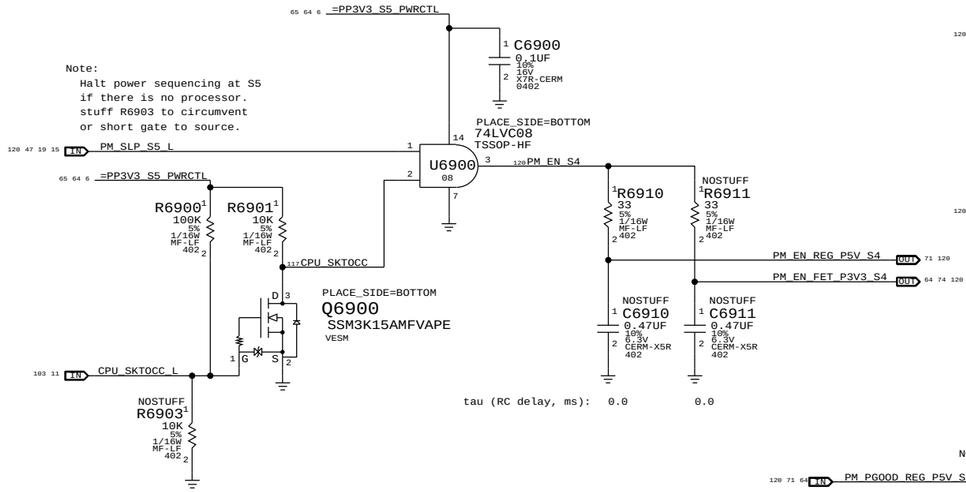
S5 3V3 Soft Enable



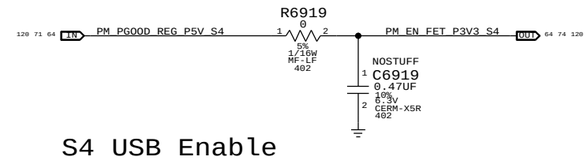
Note:
Expected 3.9V +/- 0.4V EN signal

S4 5V Enable

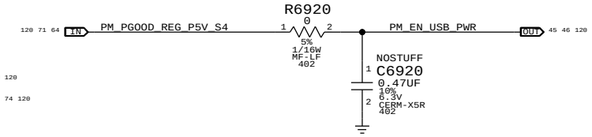


tau (RC delay, ms): 0.0 0.0

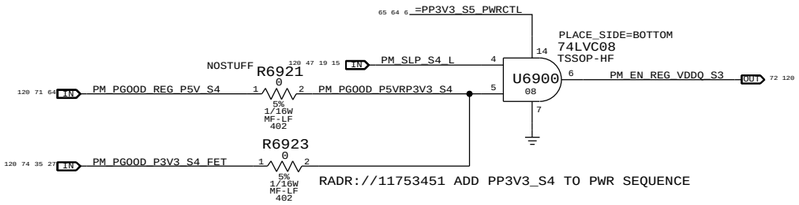
S4 3V3 Enable



S4 USB Enable

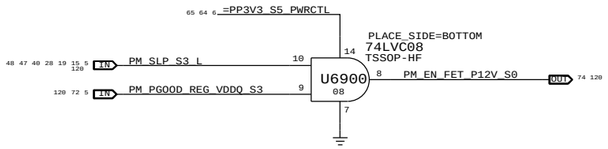


S3 1V5 Reg (S0/S3) Enable

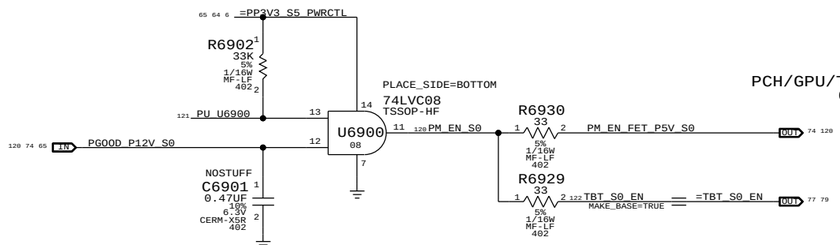


RADR://11753451 ADD PP3V3_S4 TO PWR SEQUENCE

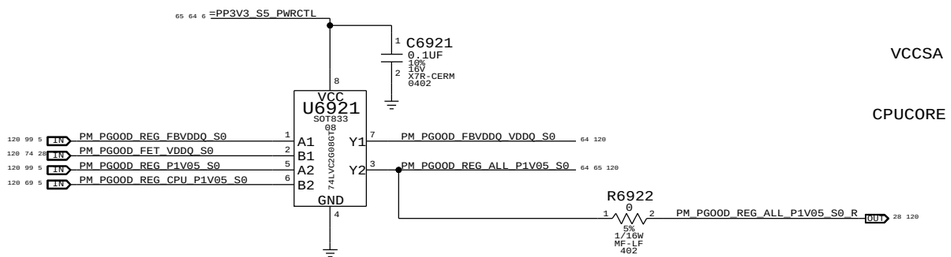
S0 12V Enable



S0 5V and TBT Enable

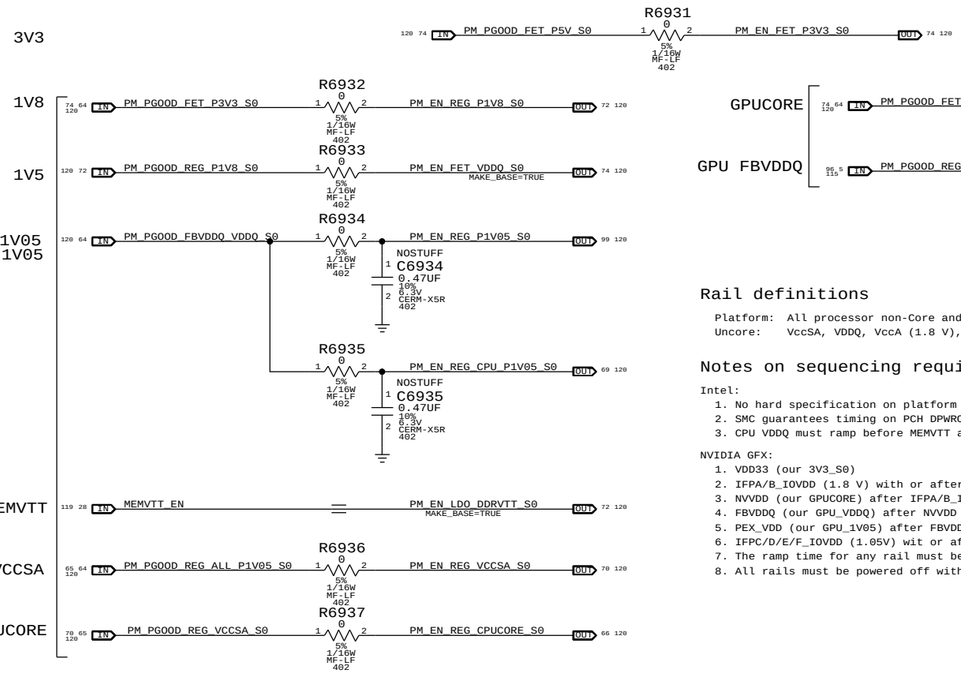


Parallel Enable PGOOD combinator

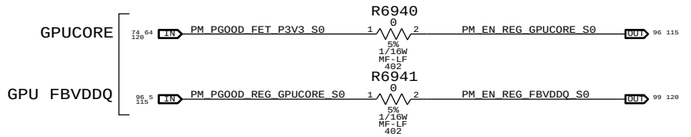


S0 Platform Parallel Sequence Enable

CPU/PCH Sequencing



GPU Sequencing



Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.8 V 1.5 V, PCH Core/PLL/VRM)
Uncore: VccSA, VDDQ, VccA (1.8 V), VccIO (VccSA, VccA, and VccIO must ramp within 50 ms of each other)

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. CPU VDDQ must ramp before MEMVTT and vice versa on power down. It has no relationship to any other rails.

NVIDIA GFX:
1. VDD33 (our 3V3_S0)
2. IFPA/B_IOVDD (1.8 V) with or after 3V3_S0 (unused in our implementation)
3. NVVDD (our GPUCORE) after IFPA/B_IOVDD
4. FBVDDQ (our GPU_VDDQ) after NVVDD
5. PEX_VDD (our GPU_1V05) after FBVDDQ
6. IFPC/D/E/F_IOVDD (1.05V) wit or after PEX_VDD
7. The ramp time for any rail must be more than 40 uS
8. All rails must be powered off within 10 ms from first rail powering off

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PM Regulator Enables

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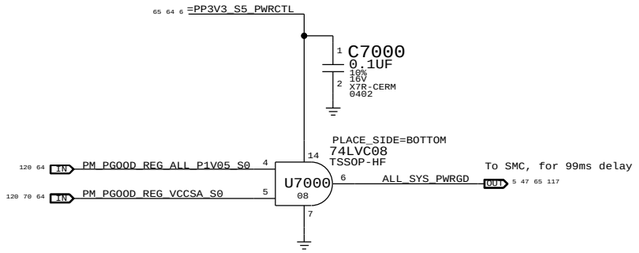
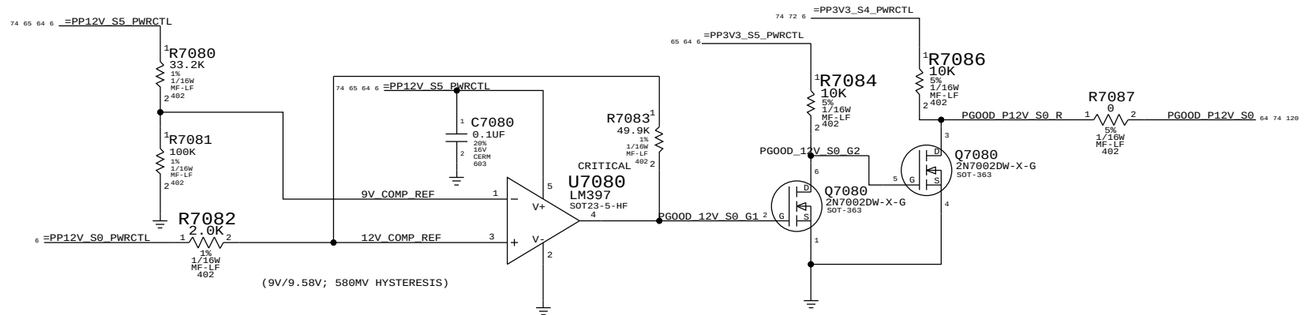
Platform Power Good Derive SMC ALL_SYS_PWRGD

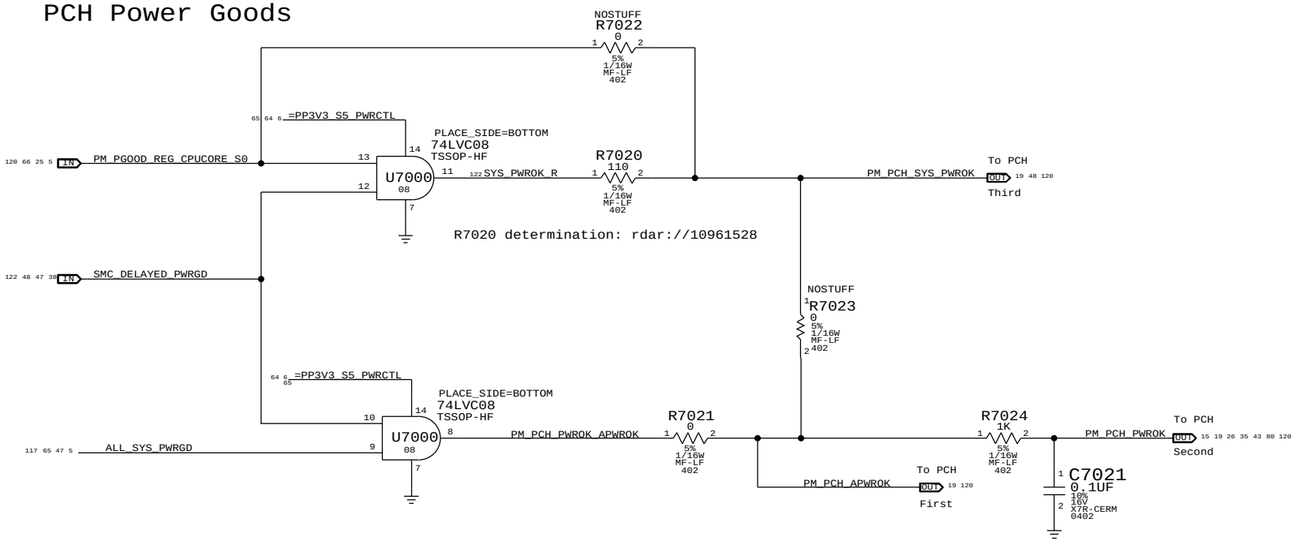
The end of the power sequence for S0 rails except CPU CORE.



PGOOD COMPARATORS FOR PP12V_S0



PCH Power Goods



radar://11043352 Need AND Gate to deassert PM_PCH_PWROK to PCH when unexpected power loss happens

Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

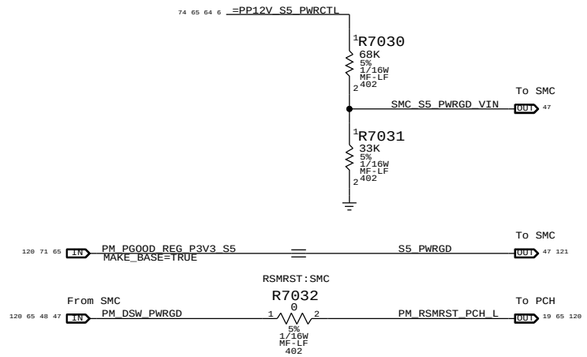
Note:
The iMac K70K72 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Primary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation.

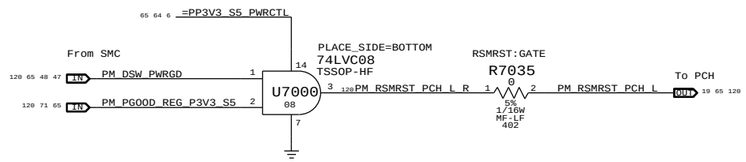
SMC de-asserts RSMRST# (PM_DSW_PWRGD) when S5_PWRGD input is asserted and SMC_S5_PWRGD_VIN input is above comparator input level of 1.5 V.

SMC asserts RSMRST# (PM_DSW_PWRGD) when SMC_S5_PWRGD_VIN input drops from 1.8 V to 1.5 V (as implemented) when 12 V S5 rail drops to 10 V.



Secondary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



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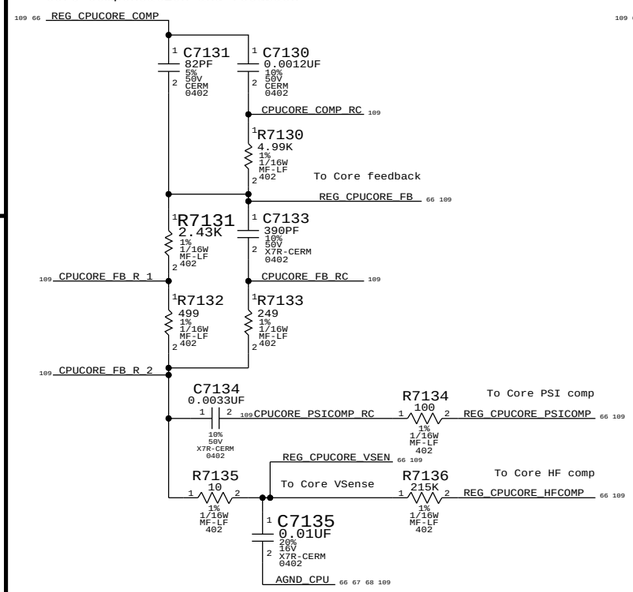
CPU Core S0 Regulator

Max avg current: 63 A (BUDGET)
Max peak current: 110 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

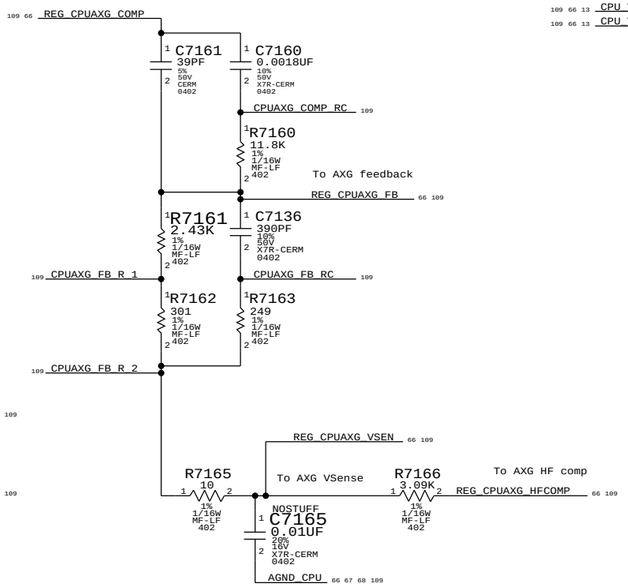
Core compensation and feedback



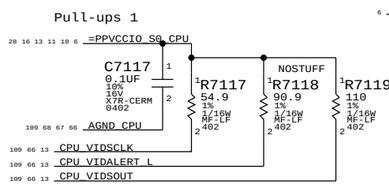
CPU AXG S0 Regulator

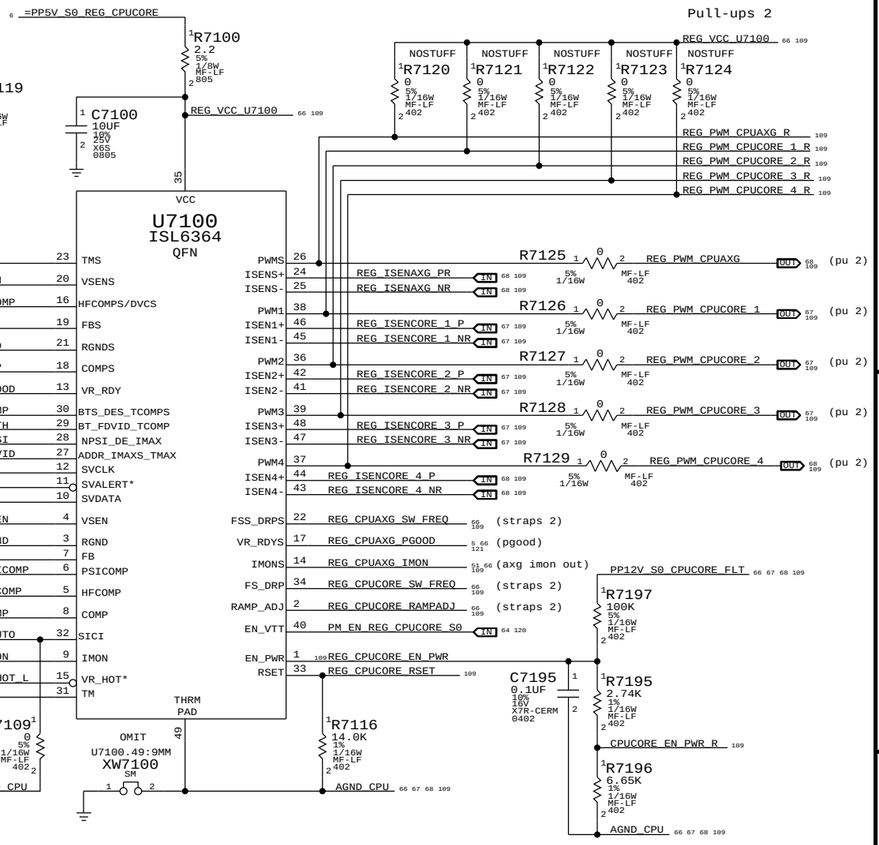
Max avg current: 12.7 A (BUDGET)
Max peak current: 30.0 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 290 kHz

AXG compensation and feedback



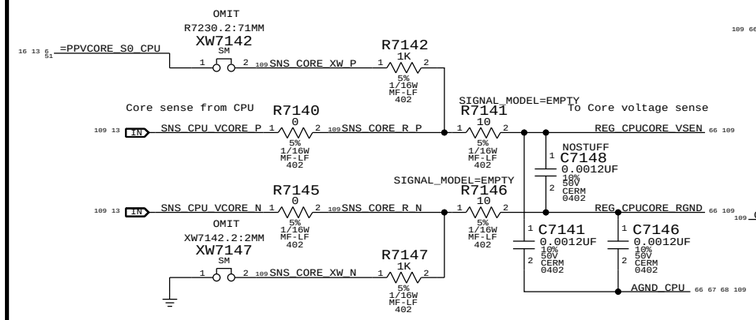
Pull-ups 1



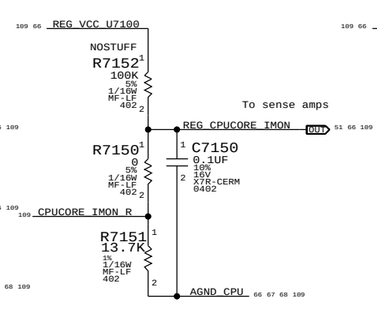


Pull-ups 2

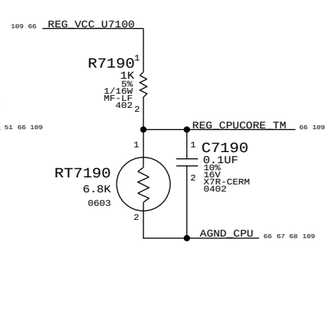
Core voltage sense input



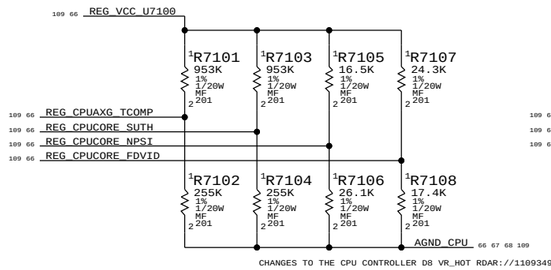
Core IMON output



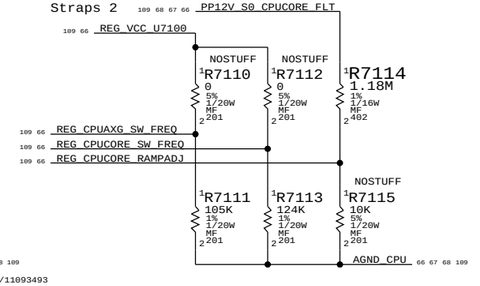
Core temp measurement



Straps 1

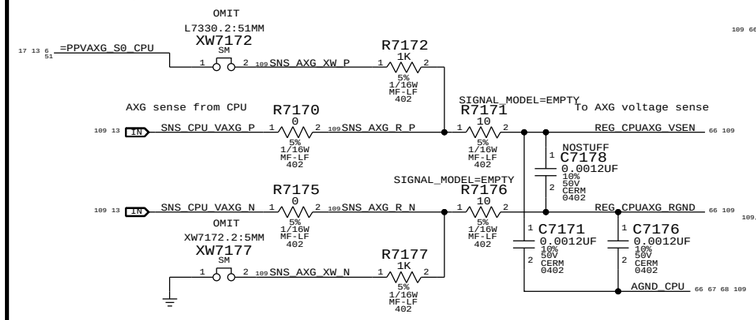


Straps 2

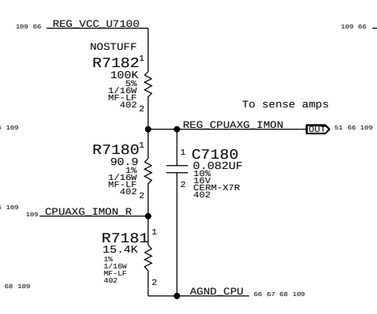


CHANGES TO THE CPU CONTROLLER D8 VR_HOT RDAR://11093493

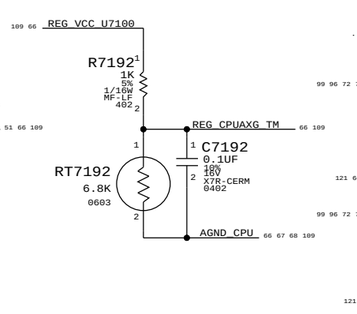
AXG voltage sense input



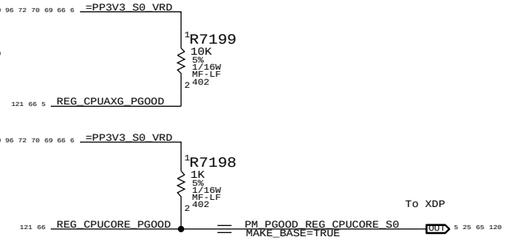
AXG IMON output



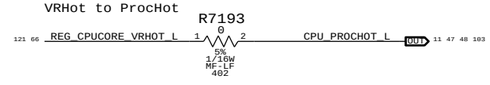
AXG temp measurement



Power goods



VRHot to ProcHot



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VReg CPU Core/AXG Cntl

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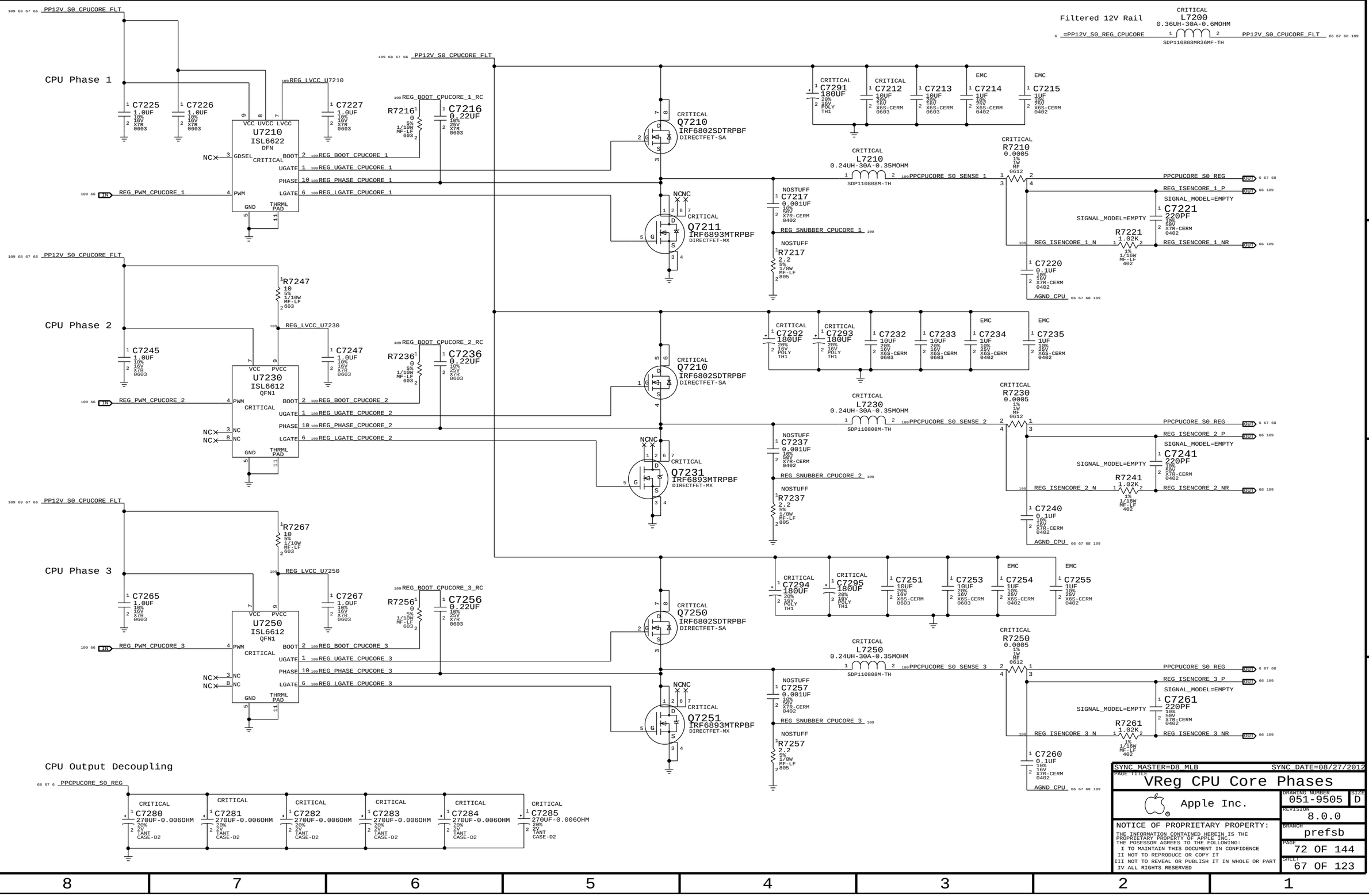
PP12V_S0_CPUCORE_FLT
CPU Phase 1
CPU Phase 2
CPU Phase 3
CPU Output Decoupling
U7210
ISL6622
DFN
U7230
ISL6612
QFN1
U7250
ISL6612
QFN1
REG_LVCC_U7210
REG_LVCC_U7230
REG_LVCC_U7250
REG_PWM_CPUCORE_1
REG_PWM_CPUCORE_2
REG_PWM_CPUCORE_3
REG_BOOT_CPUCORE_1_RC
REG_BOOT_CPUCORE_2_RC
REG_BOOT_CPUCORE_3_RC
REG_BOOT_CPUCORE_1
REG_UGATE_CPUCORE_1
REG_PHASE_CPUCORE_1
REG_LGATE_CPUCORE_1
REG_BOOT_CPUCORE_2
REG_UGATE_CPUCORE_2
REG_PHASE_CPUCORE_2
REG_LGATE_CPUCORE_2
REG_BOOT_CPUCORE_3
REG_UGATE_CPUCORE_3
REG_PHASE_CPUCORE_3
REG_LGATE_CPUCORE_3
Q7210
IRF6802SDTRPBF
DIRECTFET-SA
Q7211
IRF6893MTRPBF
DIRECTFET-MX
Q7231
Q7251
Filtered 12V Rail
L7200
0.36UH-30A-0.6MOHM
SDP110808MR36MF-TH
L7210
L7230
L7250
0.24UH-30A-0.35MOHM
SDP110808M-TH
PPCPUCORE_S0_SENSE_1
PPCPUCORE_S0_SENSE_2
PPCPUCORE_S0_SENSE_3
R7210
R7230
R7250
0.0005
PPCPUCORE_S0_REG
REG_ISENCORE_1_P
REG_ISENCORE_1_N
REG_ISENCORE_1_NR
REG_ISENCORE_2_P
REG_ISENCORE_2_N
REG_ISENCORE_2_NR
REG_ISENCORE_3_P
REG_ISENCORE_3_N
REG_ISENCORE_3_NR
SIGNAL_MODEL=EMPTY
REG_SNUBBER_CPUCORE_1
REG_SNUBBER_CPUCORE_2
REG_SNUBBER_CPUCORE_3
AGND_CPU
PPCPUCORE_S0_REG
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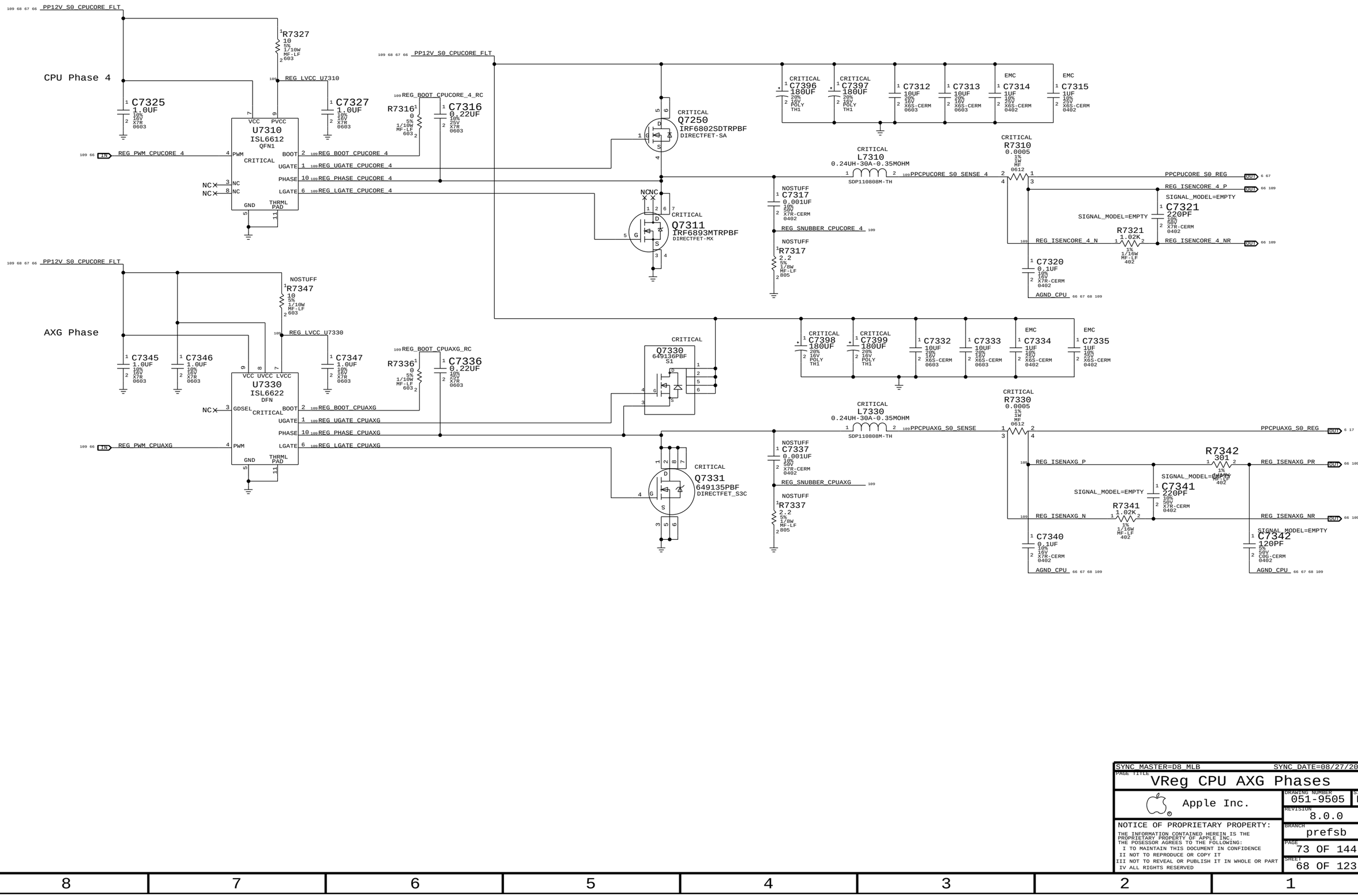

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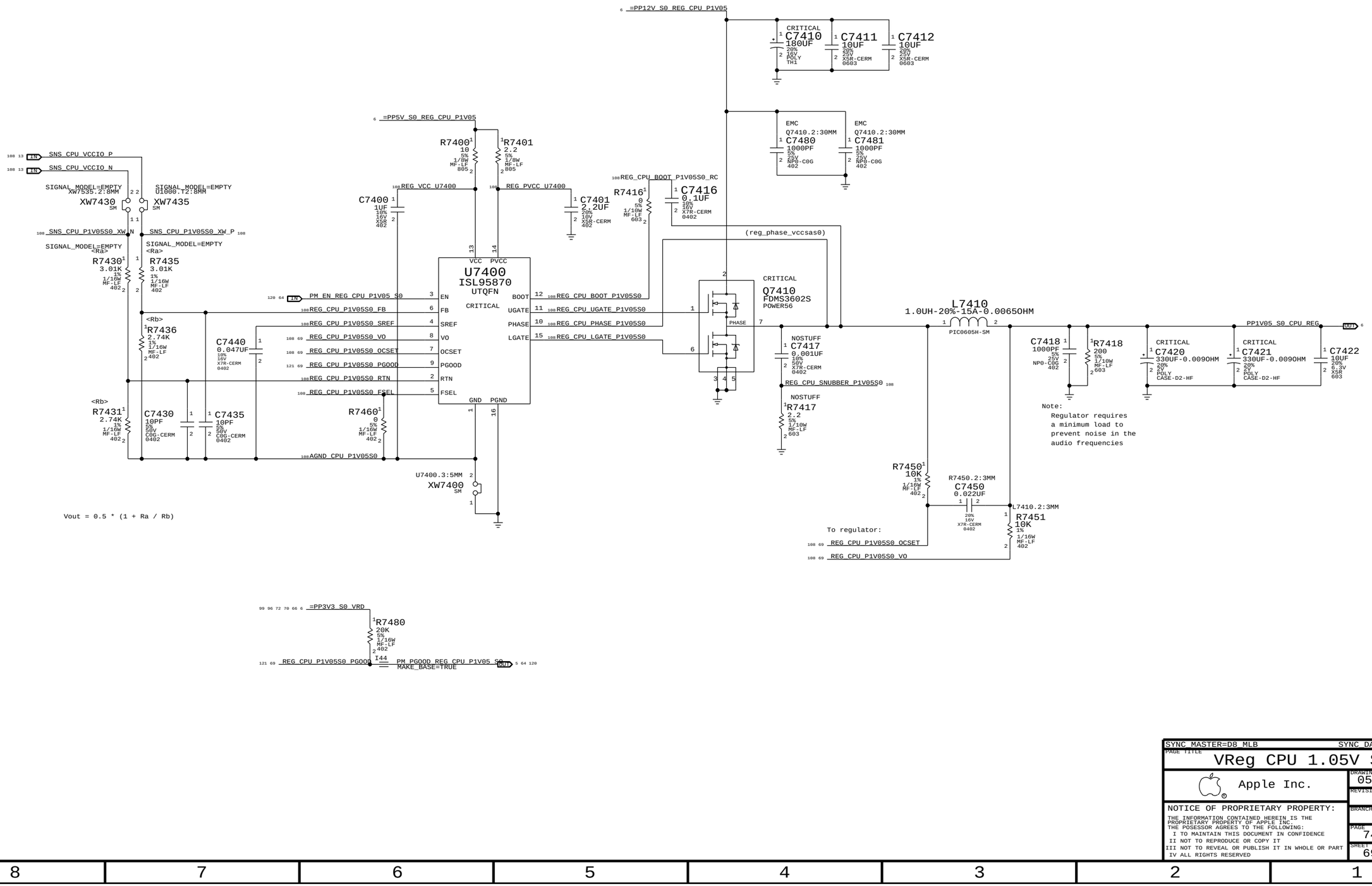
CPU VccIO (1.05V) S0 Regulator

Max avg current: 8.10 A (BUDGET)
Max peak current: 8.50 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



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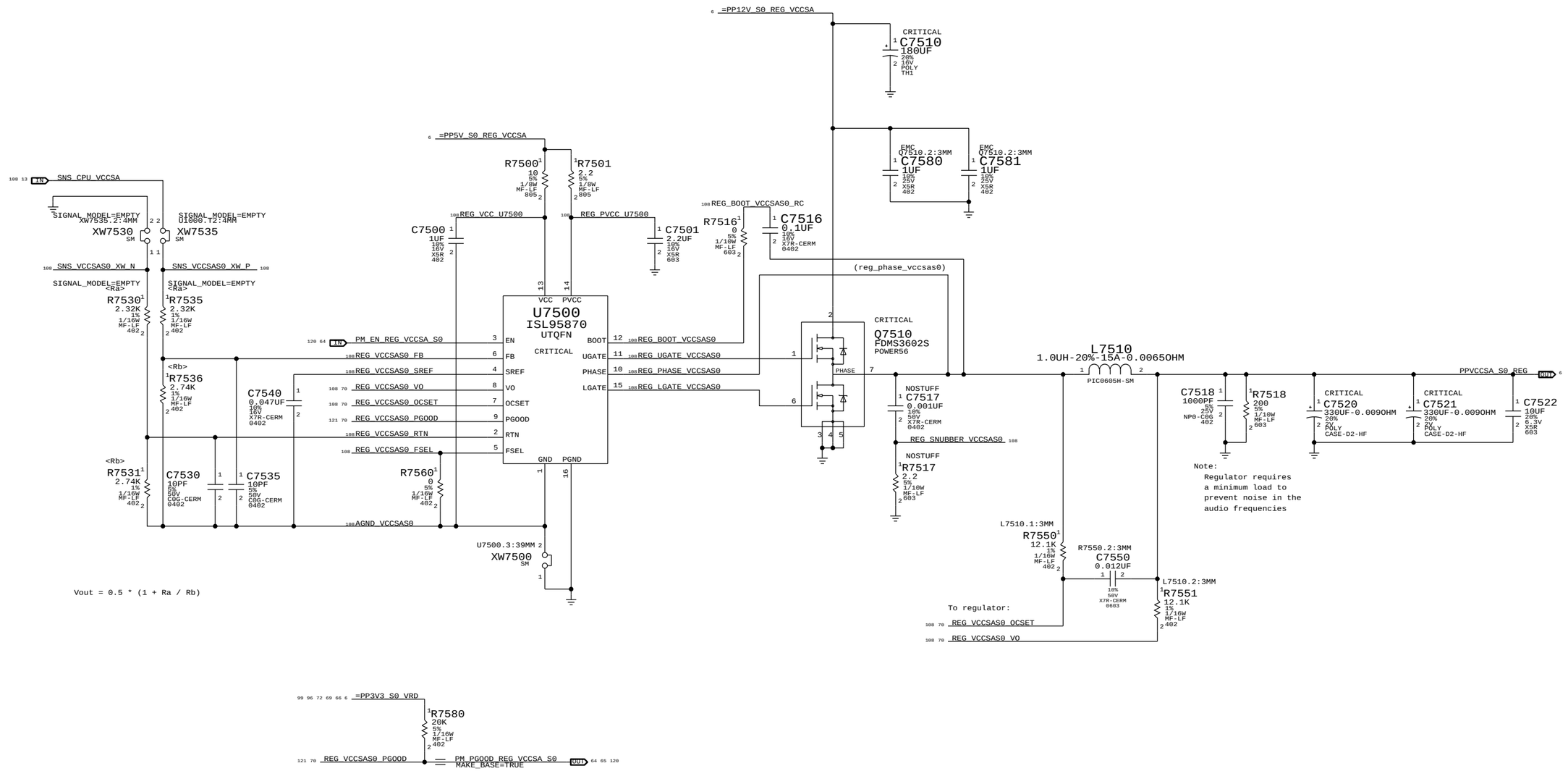
CPU VccSA (0.925V) S0 Regulator

Max avg current: 12.07 A (BUDGET)
Max peak current: 30 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



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VReg CPU VccSA S0

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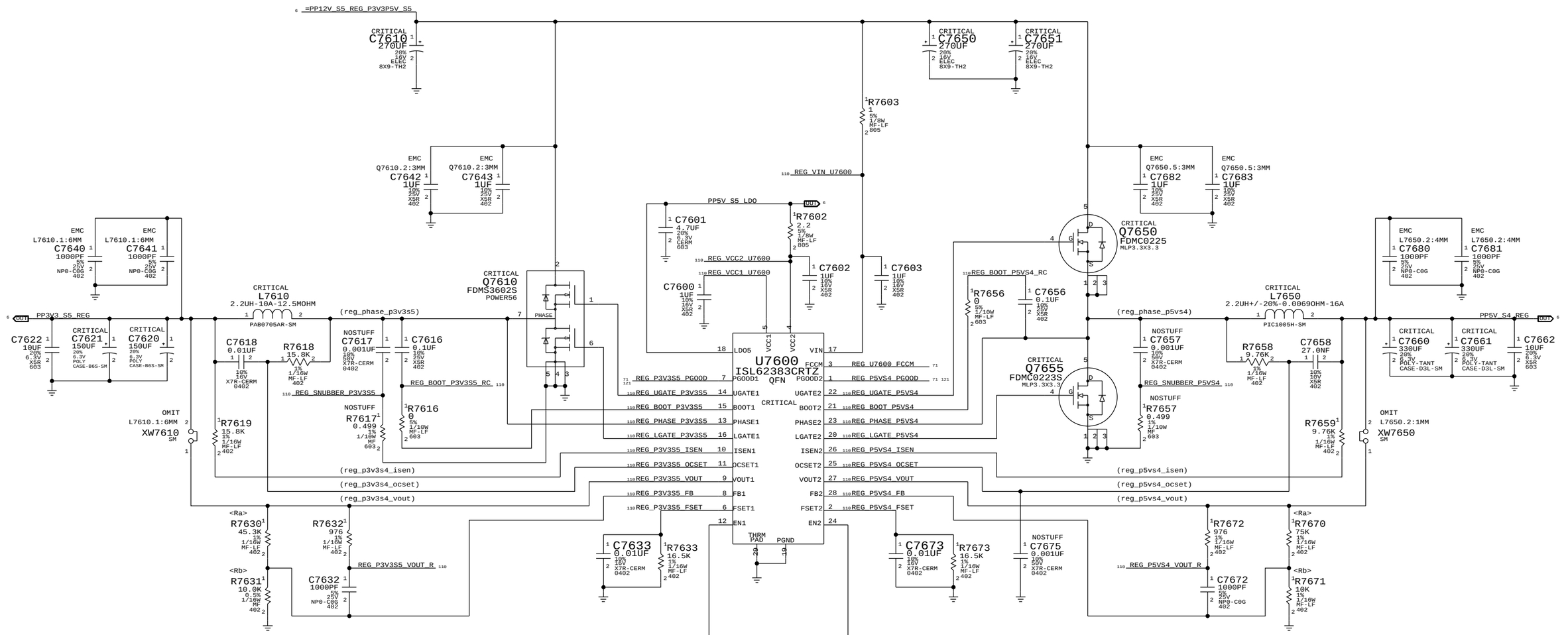
3.3V S5 Regulator

Max avg current: 6 A (design)/ 4.85 A (budget)
Max peak current: ? A (design)/ 6.6 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz

5V S4 Regulator

Max avg current: 10 A (design)/ 6.08 A (budget)
Max peak current: ? A (design)/ 6.9 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz



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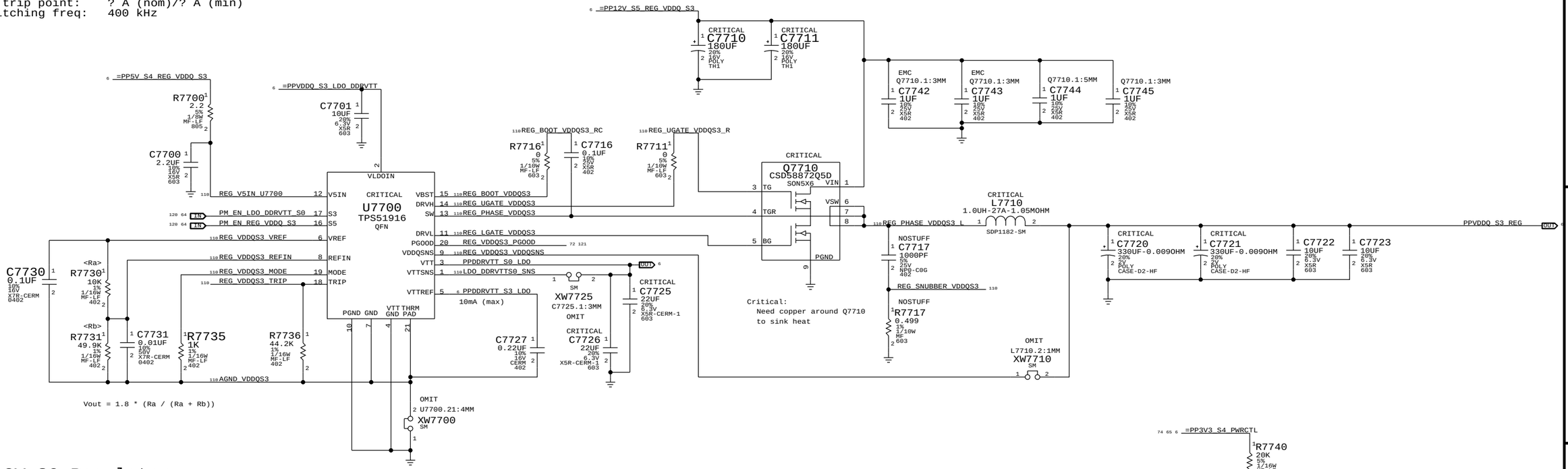
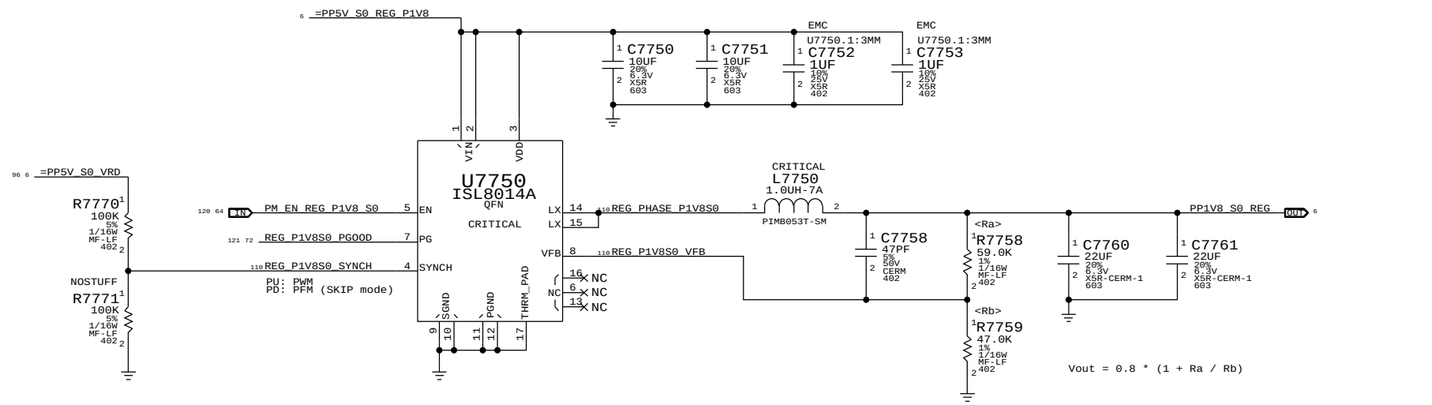
VDDQ (1.5V) S3 Regulator

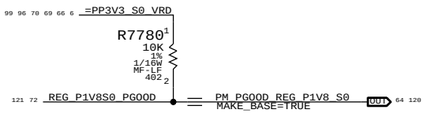
Max avg current: 9.0 A (BUDGET)
Max peak current: 11.3 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 400 kHz



1.8V S0 Regulator

Max avg current: 0.6 A (BUDGET)
Max peak current: 1.7 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz





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VReg VDDQ and 1.8V S0

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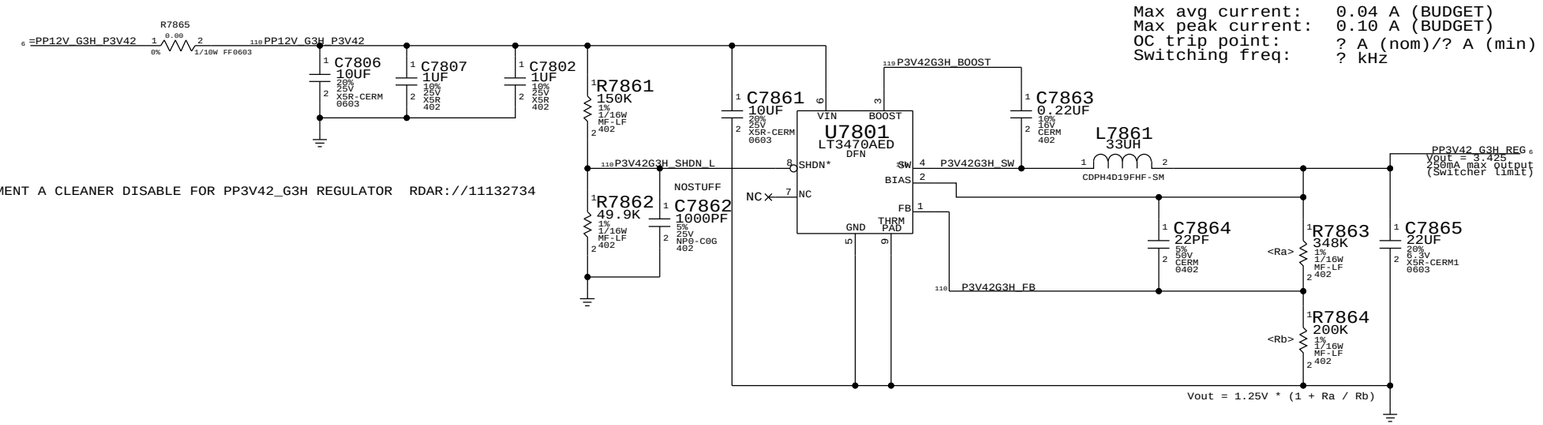
D8:CONTROLLER CHANGE FOR 3.42V SMC SUPPLY RDAR://11003901

D7/D7I: IMPLEMENT A CLEANER DISABLE FOR PP3V42_G3H REGULATOR RDAR://11132734

3.425V "G3Hot" Regulator

Max avg current: 0.04 A (BUDGET)
Max peak current: 0.10 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE: VREG 3.42V G3HOT	
Apple Inc.	DRAWING NUMBER: 051-9505 SIZE: D
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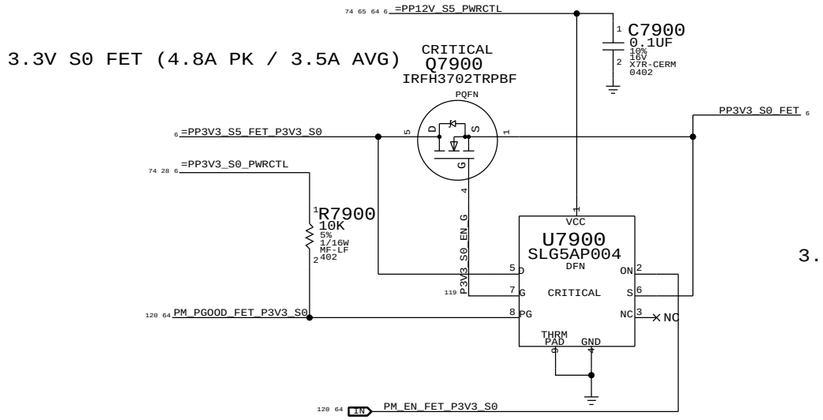
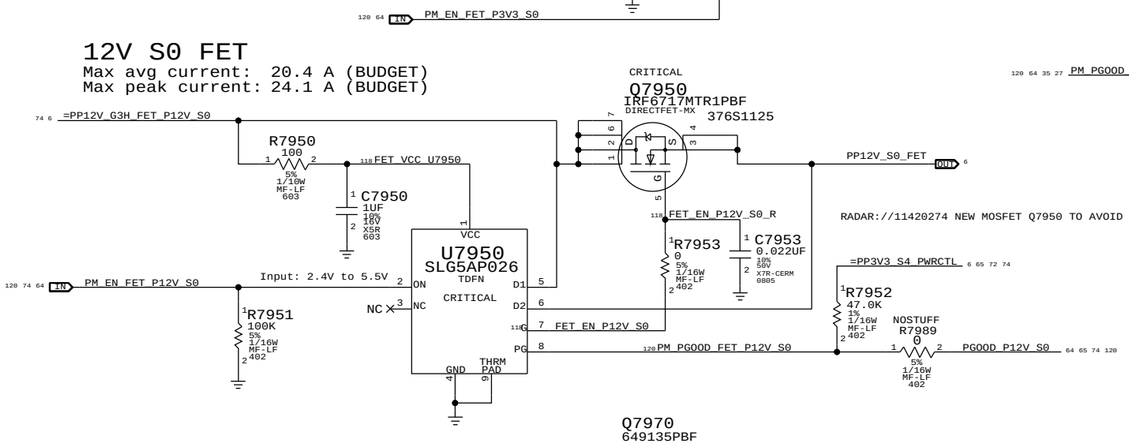
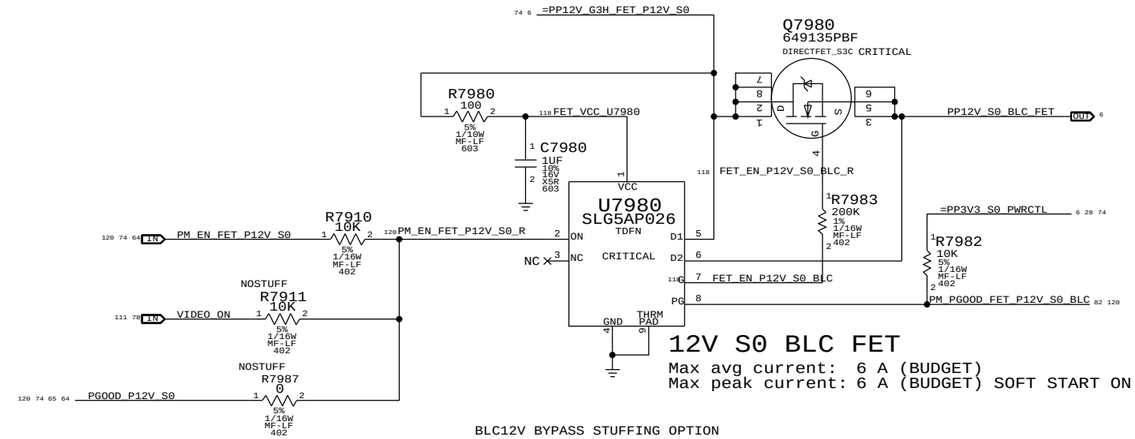


12V S0 FET

Max avg current: 20.4 A (BUDGET)
Max peak current: 24.1 A (BUDGET)



RADAR://11420274 NEW MOSFET Q7950 TO AVOID 50A 100US PULSE ON 12V S0.

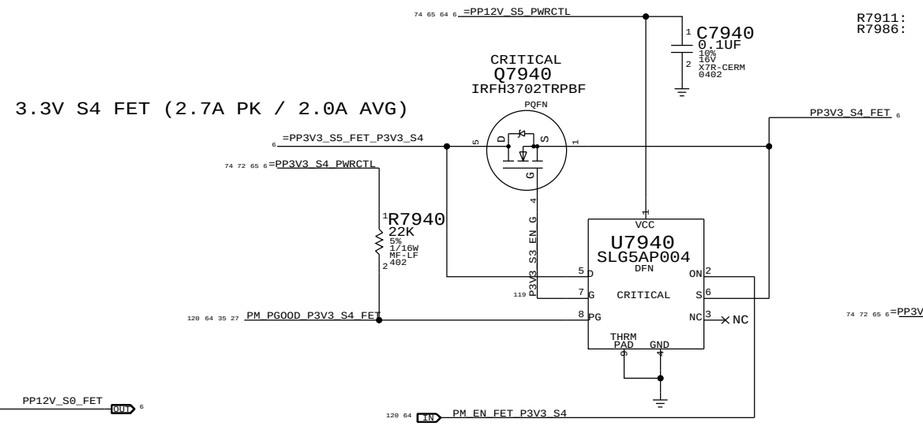


12V S0 BLC FET

Max avg current: 6 A (BUDGET)
Max peak current: 6 A (BUDGET) SOFT START ON BLC

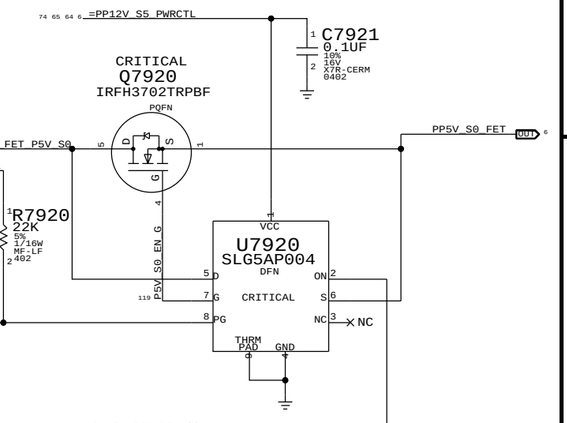
BLC12V BYPASS STUFFING OPTION

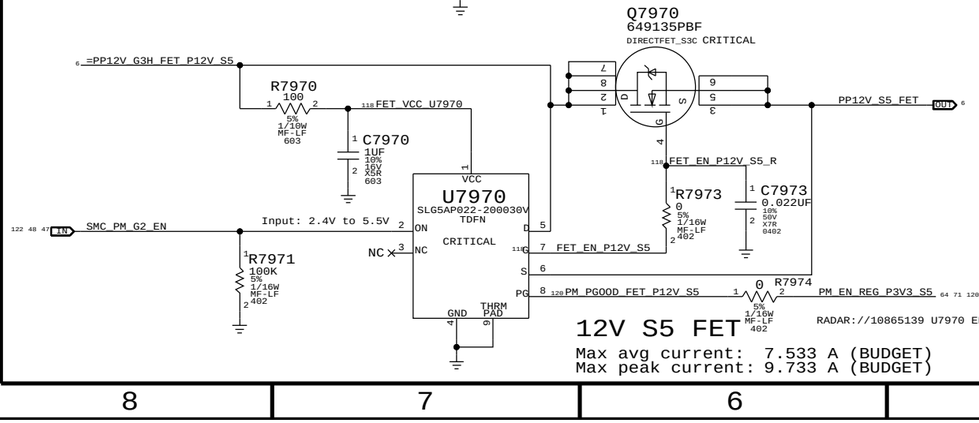
	BYPASS	NO BYPASS
R7911:	STUFF	NOSTUFF
R7986:	STUFF	NOSTUFF



5V S0 FET

Max avg current: 2.7 A (BUDGET)
Max peak current: 3.9 A (BUDGET)

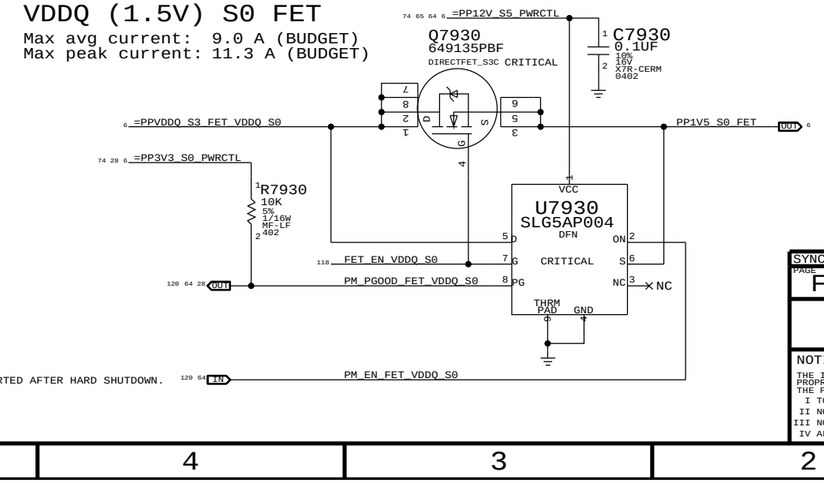




12V S5 FET

Max avg current: 7.533 A (BUDGET)
Max peak current: 9.733 A (BUDGET)

RADAR://10865139 U7970 ENSURES S5_PWRGD ISN'T ASSERTED AFTER HARD SHUTDOWN.



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE
FET-Controlled S0 and S4

Apple Inc.

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TP to DP aliases

TP_DP_TBTSRC_ML_CP<0>	=	DP_TBTSRC_ML_P<0>
TP_DP_TBTSRC_ML_CN<0>	=	DP_TBTSRC_ML_N<0>
TP_DP_TBTSRC_ML_CP<1>	=	DP_TBTSRC_ML_P<1>
TP_DP_TBTSRC_ML_CN<1>	=	DP_TBTSRC_ML_N<1>
TP_DP_TBTSRC_ML_CP<2>	=	DP_TBTSRC_ML_P<2>
TP_DP_TBTSRC_ML_CN<2>	=	DP_TBTSRC_ML_N<2>
TP_DP_TBTSRC_ML_CP<3>	=	DP_TBTSRC_ML_P<3>
TP_DP_TBTSRC_ML_CN<3>	=	DP_TBTSRC_ML_N<3>
TP_DP_TBTSRC_AUXCH_CP	=	DP_TBTSRC_AUXCH_P
TP_DP_TBTSRC_AUXCH_CN	=	DP_TBTSRC_AUXCH_N

All: MAKE_BASE=TRUE

=PP1V5_S0_DP

R9210 470K 5% 1/20W MF 201

R9211 470K 5% 1/20W MF 201

C9208 0.1UF 10% 16V X5R 6.3V 201

C9209 0.1UF 10% 16V X5R 6.3V 201

DP_INT_EG_AUX_P

DP_INT_EG_AUX_N

DP_INT_EG_AUX_C_P

DP_INT_EG_AUX_C_N

=PP1V5_S0_DP

R9212 470K 5% 1/20W MF 201

R9213 470K 5% 1/20W MF 201

C9210 0.1UF 10% 16V X5R 6.3V 201

C9211 0.1UF 10% 16V X5R 6.3V 201

DP_TBTSRC_AUXCH_P

DP_TBTSRC_AUXCH_N

DP_TBTSRC_AUX_C_P

DP_TBTSRC_AUX_C_N

=PP3V3_S0_INTDPMUX

R9204 10K 5% 1/20W MF 201

DP_GPU_MUX_EN

DP_INT_EG_HPD

R9200 100K 5% 1/20W MF 201

DP_TBTSRC_HPD

PD is on the LR page

DP_TBT_SEL

R9201 10K 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX

C9268 0.1UF 10% 16V X5R 201

C9269 0.1UF 10% 16V X5R 201

U9200 CBTL06142EEE TFBGA CRITICAL

DP_INT_EG_ML_P<0>	B4	DIN1_0+	
DP_INT_EG_ML_N<0>	A4	DIN1_0-	
DP_INT_EG_ML_P<1>	B5	DIN1_1+	
DP_INT_EG_ML_N<1>	A5	DIN1_1-	
DP_INT_EG_ML_P<2>	B6	DIN1_2+	
DP_INT_EG_ML_N<2>	A6	DIN1_2-	
DP_INT_EG_ML_P<3>	A8	DIN1_3+	
DP_INT_EG_ML_N<3>	A9	DIN1_3-	
	H9	DAUX1+	
	J9	DAUX1-	
NC	H8	DDC_CLK1	
NC	J8	DDC_DAT1	
	J2	HPD_1	
DP_TBTSRC_ML_C_P<0>	B8	DIN2_0+	
DP_TBTSRC_ML_C_N<0>	B9	DIN2_0-	
DP_TBTSRC_ML_C_P<1>	D8	DIN2_1+	
DP_TBTSRC_ML_C_N<1>	D9	DIN2_1-	
DP_TBTSRC_ML_C_P<2>	E8	DIN2_2+	
DP_TBTSRC_ML_C_N<2>	E9	DIN2_2-	
DP_TBTSRC_ML_C_P<3>	F8	DIN2_3+	
DP_TBTSRC_ML_C_N<3>	F9	DIN2_3-	
	H6	DAUX2+	
	J6	DAUX2-	
NC	H5	DDC_CLK2	
NC	J5	DDC_DAT2	
	H3	HPD_2	
	A1	GPU_SEL	DDC_AUX_SEL C2
	B7	XSD*	
	B2	DOUT_0+	
	B1	DOUT_0-	
	D2	DOUT_1+	
	D1	DOUT_1-	
	E2	DOUT_2+	
	E1	DOUT_2-	
	F2	DOUT_3+	
	F1	DOUT_3-	
	H2	AUX+	
	H1	AUX-	
	J1	HPDIN	

GND: B3, C8, G8, H4, H7, G2

C9200 0.15UF 0201 10% X5R 6.3V

C9201 0.15UF 0201 10% X5R 6.3V

C9202 0.15UF 0201 10% X5R 6.3V

C9203 0.15UF 0201 10% X5R 6.3V

C9204 0.15UF 0201 10% X5R 6.3V

C9205 0.15UF 0201 10% X5R 6.3V

C9206 0.15UF 0201 10% X5R 6.3V

C9207 0.15UF 0201 10% X5R 6.3V

DP_INTPNL_ML_C_P<0> DP_INTPNL_ML_P<0>

DP_INTPNL_ML_C_N<0> DP_INTPNL_ML_N<0>

DP_INTPNL_ML_C_P<1> DP_INTPNL_ML_P<1>

DP_INTPNL_ML_C_N<1> DP_INTPNL_ML_N<1>

DP_INTPNL_ML_C_P<2> DP_INTPNL_ML_P<2>

DP_INTPNL_ML_C_N<2> DP_INTPNL_ML_N<2>

DP_INTPNL_ML_C_P<3> DP_INTPNL_ML_P<3>

DP_INTPNL_ML_C_N<3> DP_INTPNL_ML_N<3>

DP_INTPNL_AUX_P

DP_INTPNL_AUX_N

DP_INTPNL_HPD

R9202 100K 5% 1/20W MF 201

R9203 100K 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX

=PP3V3_S0_INTDPMUX

BKLT_PWM C9270 0.1uF 10% 16V X5R 402

BKLT_PWM U9220 74LVC1G157 SOT487

BDV_BKL_PWM

GPU_LCD_BKLT_PWM

DP_TBT_SEL

BKLT_PWM R9222 47 5% 1/16W MF-LF 402

LCD_BL_PWM

LCD_BL_FILT

BKLT_PWM L9201 FERR-220-OHM 0402

LCD_BKLT_PWM

=PP1V5_S0_DP

R9290 0 5% 1/16W MF-LF 402

PP1V5_S0_DP_BIAS

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=1.5V

C9290 1UF 10% 16V X5R 402

C9291 0.1UF 10% 16V X7R-CERM 0402

R9260 470K 5% 1/20W MF 201

R9261 470K 5% 1/20W MF 201

R9262 470K 5% 1/20W MF 201

R9263 470K 5% 1/20W MF 201

R9264 470K 5% 1/20W MF 201

R9265 470K 5% 1/20W MF 201

R9266 470K 5% 1/20W MF 201

R9267 470K 5% 1/20W MF 201

DP_TBTSRC_ML_P<0>	C9250 0.22UF	DP_TBTSRC_ML_C_P<0>
DP_TBTSRC_ML_N<0>	C9251 0.22UF	DP_TBTSRC_ML_C_N<0>
DP_TBTSRC_ML_P<1>	C9252 0.22UF	DP_TBTSRC_ML_C_P<1>
DP_TBTSRC_ML_N<1>	C9253 0.22UF	DP_TBTSRC_ML_C_N<1>
DP_TBTSRC_ML_P<2>	C9254 0.22UF	DP_TBTSRC_ML_C_P<2>
DP_TBTSRC_ML_N<2>	C9255 0.22UF	DP_TBTSRC_ML_C_N<2>
DP_TBTSRC_ML_P<3>	C9256 0.22UF	DP_TBTSRC_ML_C_P<3>
DP_TBTSRC_ML_N<3>	C9257 0.22UF	DP_TBTSRC_ML_C_N<3>

All: 20% 6.3V XSR 0201

SYNC_MASTER=D8_MLB	SYNC_DATE=08/27/2012
PAGE TITLE	Internal DP MUXing
Apple Inc.	DRAWING NUMBER 051-9505 SIZE D
	REVISION 8.0.0
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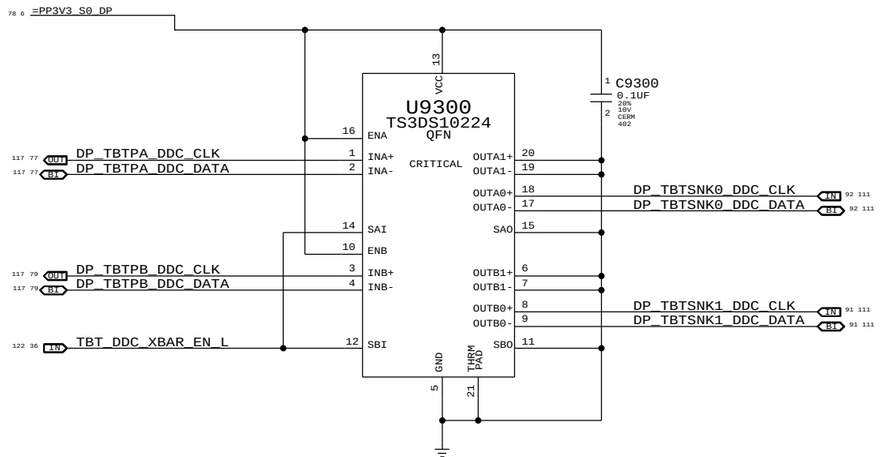
Dual-Port Host DDC Crossbar



SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE

TBT DDC Crossbar

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

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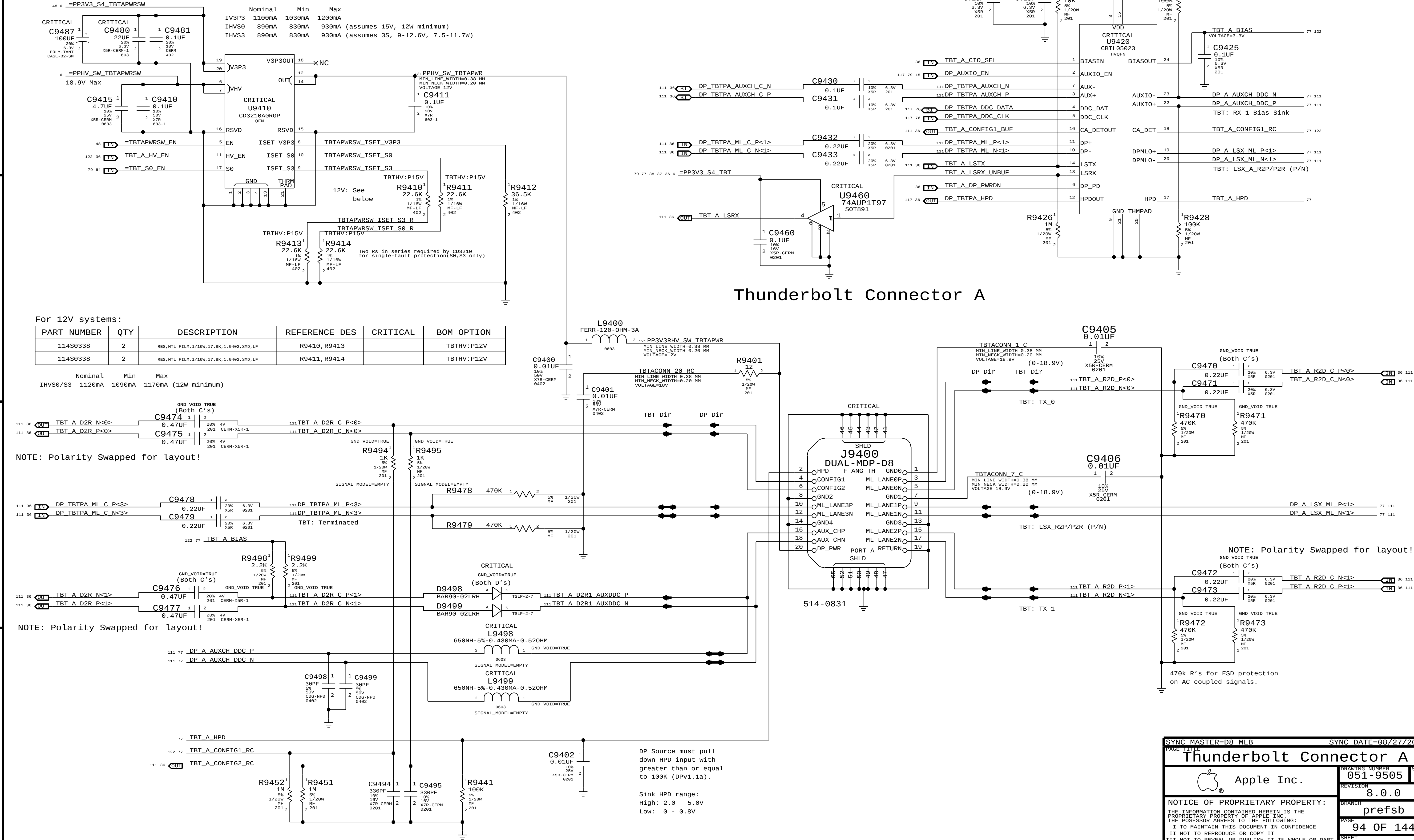
3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)



=PP3V3_S4_TBTAPWRSW
CRITICAL
C9487
100UF
CRITICAL
C9480
22UF
C9481
0.1UF
=PPHV_SW_TBTAPWRSW
18.9V Max
C9415
4.7UF
C9410
0.1UF
CRITICAL
U9410
CD3210A0RGP
QFN
V3P3
VHV
RSVD
EN
HV_EN
S0
V3P3OUT
NC
OUT
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
PPHV_SW_TBTAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=12V
C9411
0.1UF
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
12V: See below
TBTHV:P15V
R9410
22.6K
R9411
22.6K
R9412
36.5K
TBTAPWRSW_ISET_S3_R
TBTAPWRSW_ISET_S0_R
R9413
22.6K
R9414
22.6K
Two Rs in series required by CD3210
for single-fault protection(S0,S3 only)
=PP3V3_S4_TBT
C9420
0.1UF
C9421
0.1UF
R9427
10K
R9429
100K
VDD
CRITICAL
U9420
CBTL05023
HVQFN
BIASIN
AUXIO_EN
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
DP_PD
HPDOUT
BIASOUT
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
GND
THMPAD
TBT_A_BIAS
VOLTAGE=3.3V
C9425
0.1UF
TBT_A_CIO_SEL
DP_AUXIO_EN
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
C9430
0.1UF
C9431
0.1UF
DP_TBTPA_AUXCH_N
DP_TBTPA_AUXCH_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
C9432
0.22UF
C9433
0.22UF
DP_TBTPA_ML_P<1>
DP_TBTPA_ML_N<1>
TBT_A_LSTX
TBT_A_LSRX_UNBUF
TBT_A_DP_PWRDN
DP_TBTPA_HPD
DP_A_AUXCH_DDC_N
DP_A_AUXCH_DDC_P
TBT: RX_1 Bias Sink
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
CRITICAL
U9460
74AUP1T97
SOT891
TBT_A_LSRX
C9460
0.1UF
R9426
1M
R9428
100K
Thunderbolt Connector A
L9400
FERR-120-OHM-3A
PP3V3RHV_SW_TBTAPWR
C9400
0.01UF
C9401
0.01UF
TBTACONN_20_RC
R9401
12
C9405
0.01UF
TBTACONN_1_C
(0-18.9V)
DP Dir
TBT Dir
C9470
0.22UF
C9471
0.22UF
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
TBT: TX_0
R9470
470K
R9471
470K
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
C9474
0.47UF
C9475
0.47UF
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
NOTE: Polarity Swapped for layout!
R9494
1K
R9495
1K
CRITICAL
J9400
DUAL-MDP-D8
F-ANG-TH
SHLD
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
PORT A
514-0831
C9406
0.01UF
TBTACONN_7_C
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
C9478
0.22UF
C9479
0.22UF
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: Terminated
R9478
470K
R9479
470K
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_R2P/P2R (P/N)
TBT_A_BIAS
R9498
2.2K
R9499
2.2K
CRITICAL
D9498
BAR90-02LRH
D9499
BAR90-02LRH
(Both D's)
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R_N<1>
TBT_A_D2R_P<1>
C9476
0.47UF
C9477
0.47UF
TBT_A_D2R_C_P<1>
TBT_A_D2R_C_N<1>
NOTE: Polarity Swapped for layout!
C9472
0.22UF
C9473
0.22UF
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
TBT: TX_1
R9472
470K
R9473
470K
470k R's for ESD protection
on AC-coupled signals.
CRITICAL
L9498
650NH-5%-0.430MA-0.520HM
DP_A_AUXCH_DDC_P
DP_A_AUXCH_DDC_N
C9498
30PF
C9499
30PF
CRITICAL
L9499
650NH-5%-0.430MA-0.520HM
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R9452
1M
R9451
1M
C9494
330PF
C9495
330PF
R9441
100K
C9402
0.01UF
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9410,R9413		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9411,R9414		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

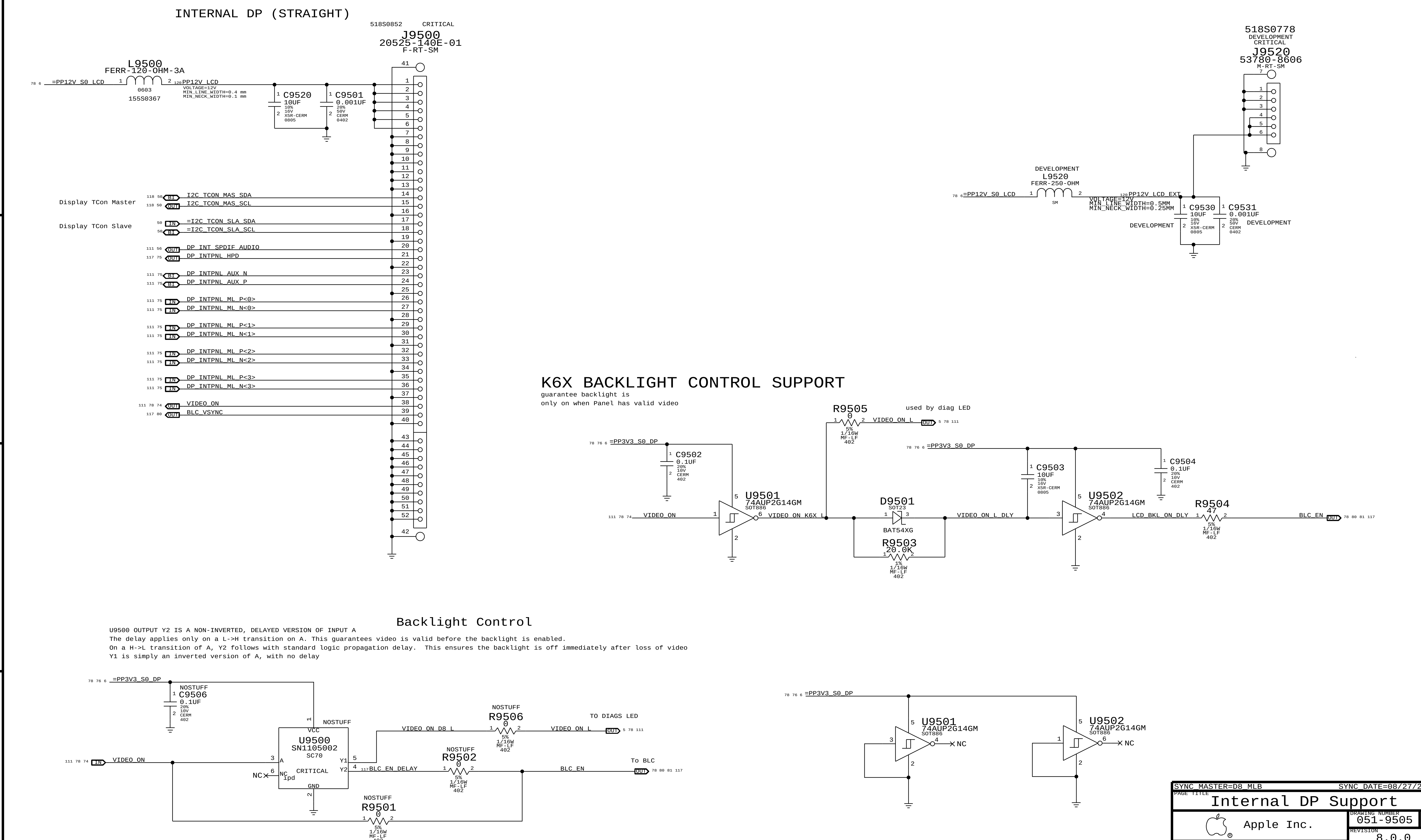
PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D

REVISION: 8.0.0

BRANCH: prefsb


INTERNAL DP (STRAIGHT)
518S0852 CRITICAL
J9500
20525-140E-01
F-RT-SM
L9500
FERR-120-OHM-3A
0603
155S0367
=PP12V_S0_LCD
PP12V_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.1 mm
C9520
10UF
C9501
0.001UF
Display TCon Master
I2C_TCON_MAS_SDA
I2C_TCON_MAS_SCL
Display TCon Slave
=I2C_TCON_SLA_SDA
=I2C_TCON_SLA_SCL
DP_INT_SPDIF_AUDIO
DP_INTPNL_HPD
DP_INTPNL_AUX_N
DP_INTPNL_AUX_P
DP_INTPNL_ML_P<0>
DP_INTPNL_ML_N<0>
DP_INTPNL_ML_P<1>
DP_INTPNL_ML_N<1>
DP_INTPNL_ML_P<2>
DP_INTPNL_ML_N<2>
DP_INTPNL_ML_P<3>
DP_INTPNL_ML_N<3>
VIDEO_ON
BLC_VSYNC
518S0778
DEVELOPMENT
CRITICAL
J9520
53780-8606
M-RT-SM
DEVELOPMENT
L9520
FERR-250-OHM
=PP12V_S0_LCD
PP12V_LCD_EXT
VOLTAGE=12V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9530
10UF
C9531
0.001UF
K6X BACKLIGHT CONTROL SUPPORT
guarantee backlight is
only on when Panel has valid video
R9505
used by diag LED
VIDEO_ON_L
=PP3V3_S0_DP
C9502
0.1UF
U9501
74AUP2G14GM
VIDEO_ON_K6X_L
D9501
BAT54XG
R9503
20.0K
VIDEO_ON_L_DLY
C9503
10UF
C9504
0.1UF
U9502
74AUP2G14GM
LCD_BKL_ON_DLY
R9504
47
BLC_EN
Backlight Control
U9500 OUTPUT Y2 IS A NON-INVERTED, DELAYED VERSION OF INPUT A
The delay applies only on a L->H transition on A. This guarantees video is valid before the backlight is enabled.
On a H->L transition of A, Y2 follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video
Y1 is simply an inverted version of A, with no delay
NOSTUFF
C9506
0.1UF
U9500
SN1105002
SC70
CRITICAL
VIDEO_ON_D8_L
R9506
TO DIAGS LED
R9502
BLC_EN_DELAY
To BLC
R9501
NC

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Internal DP Support

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

REVISION 8.0.0

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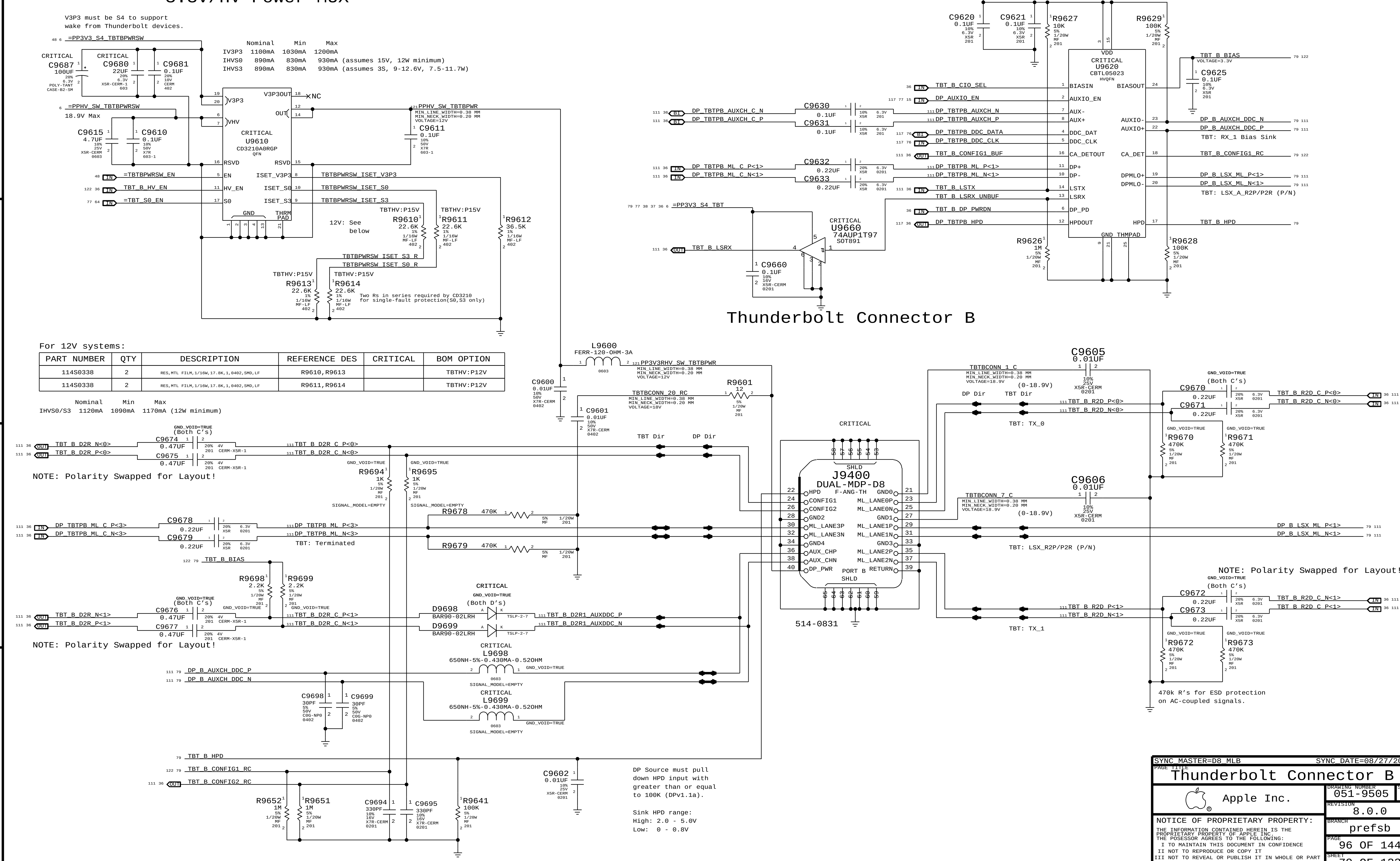
3.3V/HV Power MUX



For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9610,R9613		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9611,R9614		TBTHV:P12V

Nominal Min Max
IHVS0/S3 1120mA 1090mA 1170mA (12W minimum)

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

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REVISION 8.0.0

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14V BLC PRE-REGULATOR

L9703 1KOHM-25%-0.6A 0603 — BLC_P3V3S
L9704 1KOHM-25%-0.6A 0603 — BLC_P3V3A
NOSTUFF L9702 1KOHM-25%-0.6A 0603 — BLC_P3V3_REF
=PP3V3_S0_BLC — R9701 0.100 0.1% 1/4W MF 1206 — PP3V3_S0_BLC_R
C9735 2.2UF 10% 16V X5R 603
C9733 1000PF 5% 25V CERM 603
C9734 2.2UF 10% 10V X6R 603

PP12V_S0_BLC_VINP — R9752 0.001 1% 1W MF-LF 2512 — L9740 12UH-7A-0.02OHM PIMB137T-SM NOSTUFF
D9740 TO277A SS12P4S
Q9741 NOSTUFF FDMS6681Z POWER56
PRE_REG_OUT
C9748 10UF 10% 35V X5R 1210
C9749 470UF 20% 25V ELEC 10X10.8-SM
C9747 0.068UF 10% 50V X7R-CERM 0603
R9751 49.9K 1% 1/10W MF-LF 603
R9750 49.9K 1% 1/10W MF-LF 603
BOOST_BYPASS_GATE
BOOST_BYPASS
Q9740 CSD16412Q5A MLP5X6-LFPAK-Q5A

BLC_P3V3S — NOSTUFF R9711 100K 5% 1/16W MF-LF 402 — BLC_EXT_BOOT_L
CRITICAL Q9711 SSM3K15AMFVAPE VESM
CRITICAL 74LVC2G08 SOT902 U9710 08
PM_PCH_PWROK
PCH_BLC_EXT_BOOT
BLC_EXT_BOOT
0 R9712 5% 1/16W MF-LF 402 — SMB_PCH_BLC_SDA

U9740 TPS40210 MSOP
DIS/EN* — BOOST_VDD — BOOST_BP — BOOST_GDRV — ISNS — BOOST_COMP — COMP — BOOST_FB — FB — BOOST_SS — SS — BOOST_RC — RC — GND — THRM_PAD

PRE_BOOST:Y
R9742 10K 1% 1/10W MF-LF 603
C9741 0.1UF 10% 50V X7R 603-1
C9740 1500PF 10% 50V CERM 603
R9740 0 5% 1/10W MF-LF 603
R9741 22K 5% 1/10W MF-LF 603
R9743 330K 5% 1/10W MF-LF 603
C9742 270PF 5% 50V CERM 603
C9743 1.0UF 10% 50V X7R 0805
R9744 10 1% 1/8W MF-LF 805
R9745 1.10K 1% 1/8W MF-LF 805
C9746 0.1UF 10% 50V X7R 603-1
C9744 1.0UF 10% 50V X7R 0805
R9747 30.1 1% 1/10W MF-LF 603
R9748 1.0K 1% 1/10W MF-LF 603
C9745 390PF 10% 50V X7R-CERM 0402
R9749 0.010 1% 1W MF 2010

BLC_P3V3S — C9790 0.1UF 10% 16V X7R-CERM 0402
74LVC1G08GW SOT353 U9780
BLC_BL — BLC_ENA — BLC_ENA1
R9780 100K 1% 1/10W MF-LF 603

D8:SUOPERTEX GPIOS FOR BLC ISP RDAR://10987156

BLC_P3V3S — C9710 0.1UF 10% 6.3V X5R 201
NOSTUFF R9710 100K 5% 1/16W MF-LF 402 — BLC_MCU_RESET_R_L
0 R9713 5% 1/16W MF-LF 402 — BLC_MCU_RESET_L
CRITICAL 74LVC2G08 SOT902 U9710 08
PM_PCH_PWROK
PCH_BLC_MCU_RESET
CRITICAL Q9710 SSM3K15AMFVAPE VESM
BLC_MCU_RESET

BLC_P3V3S — NOSTUFF R9732 10K 5% 1/16W MF-LF 402
R9733 10K 5% 1/16W MF-LF 402

BLC_P3V3A — C9704 0.1UF 10% 16V X7R-CERM 0402 — C9708 0.1UF 10% 16V X7R-CERM 0402
BLC_P3V3S — C9701 1000PF 5% 50V C0G-CERM 603 — C9702 1000PF 5% 50V C0G-CERM 603 — C9703 1000PF 5% 50V C0G-CERM 603
C9709 1000PF 5% 50V C0G-CERM 603

U9700 LPC2132FBD64 LQFP

VDD — VDDA VREF VBAT OMIT_TABLE

P0.0/TXD0/PWM1 — BLC_MCU_TXD0
P0.1/RXD0/PWM3/EINT0 — BLC_MCU_RXD0
P0.2/SCL0/CAP0.0 — SMB_TCON_BLC_SCL
P0.3/SDA0/MAT0.0/EINT1 — SMB_TCON_BLC_SDA
P0.4/SCK0/CAP0.1/AD0.6 — BLC_GOOD
P0.5/MISO0/MAT0.1/AD0.7 — BLC_MCU_UVLO
P0.6/MOSI0/CAP0.2 — BLC_VSYNC_R
P0.7/SSEL0/PWM2/EINT2 — BLC_PWM_1_R
P0.8/TXD1/PWM4 — BLC_PWM_2_R
P0.9/RXD1/PWM6/EINT3 — BLC_PWM_3_R
P0.10/CAP1.0
P0.11/CAP1.1/SCL1 — TP_BLC_MCU_TP_2
P0.12/MAT1.0
P0.13/MAT1.1
P0.14/EINT1/SDA1
P0.15/EINT2
P0.16/EINT0/MAT0.2/CAP0.2
P0.17/CAP1.2/SCK1/MAT1.2
P0.18/CAP1.3/MISO1/MAT1.3
P0.19/MAT1.2/MOSI1/CAP1.2
P0.20/MAT1.3/SSEL1/EINT3
P0.21/PWM5/CAP1.3 — BLC_MCU_PWM5
P0.22/CAP0.0/MAT0.0
P0.23
P0.25/AD0.4/AOUT
P0.26/AD0.5
P0.27/AD0.0/CAP0.1/MAT0.1
P0.28/AD0.1/CAP0.2/MAT0.2
P0.29/AD0.2/CAP0.3/MAT0.3
P0.30/AD0.3/EINT3/CAP0.0
P0.31

P1.16/TRACEPKT0 — TP_PCH_GPIO6_TACH2
P1.17/TRACEPKT1 — BLC_EN_R
P1.18/TRACEPKT2 — NC
P1.19/TRACEPKT3 — NC
P1.20/TRACESYNC — NC
P1.21/PIPESTAT0 — NC
P1.22/PIPESTAT1 — NC
P1.23/PIPESTAT2 — NC
P1.24/TRACECLK — NC
P1.25/EXTIN0 — NC
P1.26/RTCK — BLC_MCU_RTCK
P1.27/TDO — BLC_MCU_TDO
P1.28/TDI — BLC_MCU_TDI
P1.29/TCK — BLC_MCU_TCK
P1.30/TMS — BLC_MCU_TMS
P1.31/TRST* (IPU) — BLC_MCU_TRST

RESET* — BLC_MCU_RESET_L
XTALIN — BLC_MCU_XTAL_IN
XTALOUT — BLC_MCU_XTAL_OUT_R
RTCX1 — NC
RTCX2 — NC
BLC_MCU_XTAL_OUT

VSS — VSSA

(WAS BLC_GPIO)
R9727 10K 1% 1/10W MF-LF 402
C9725 1000PF 5% 50V C0G-CERM 603
R9728 1K 5% 1/10W MF-LF 402 — BLC_EN
BLC_EN IS DRIVEN BY TCON (CSA95)

D9700 BAS316DG SOD323-SM
C9705 1UF 10% 16V X5R 402
R9715 10K 5% 1/10W MF-LF 402
R9716 0 5% 1/10W MF-LF 402
R9717 10M 5% 1/10W MF-LF 402
CRITICAL Y9705 3.2X2.5MM-SM 12.000MHZ-30PPM-10PF-85C
C9706 18PF 5% 50V C0G-CERM 0402
C9707 18PF 5% 50V C0G-CERM 0402
R9781 100K 5% 1/10W MF-LF 402 — FLAG_V

MCU ISP PROG AND TEST CONNECTOR

DEVELOPMENT J9700 CF20151D0R0-NH F-RT-SM
=PP3V3_S0_BLC
(WAS BLC_BLON)
BLC_EN
LCD_BKLT_PWM
BLC_VSYNC
BLC_MCU_TXD0
BLC_MCU_RXD0
BLC_MCU_B_SDA_CONN
BLC_MCU_RESET_L
BLC_MCU_TRST
BLC_MCU_TDI
BLC_MCU_TMS
BLC_MCU_TCK
BLC_MCU_RTCK
BLC_MCU_TDO
APN 998-3605

SMB_PCH_BLC_SDA — NOSTUFF J9701 HB3902U-L M-ST-TH

SMC_BLC_MUX_RX_L — 0 R9730 5% 1/16W MF-LF 402 — BLC_MCU_TXD0
SMC_BLC_MUX_TX_L — 0 R9731 5% 1/16W MF-LF 402 — BLC_MCU_RXD0

BLC_UVLO — NOSTUFF 0 R9726 5% 1/16W MF-LF 402
BLC_VSYNC — 1K R9702 5% 1/16W MF-LF 402
R9703 100K 5% 1/16W MF-LF 402
SMB_PCH_BLC_SCL
SMB_PCH_BLC_SDA

FLAG_V — R9797 0 5% 1/16W MF-LF 402
STRCLK_R1 — R9705 10K 5% 1/16W MF-LF 402

LCD_BKLT_PWM — R9706 1K 1% 1/16W MF-LF 402 — BLC_DIM_MCU
R9707 100K 5% 1/16W MF-LF 402
LED_DRIVER_OVP1P
LED_DRIVER_OVP2P
LED_DRIVER_OVP3P

BLC_P3V3S — C9791 0.1UF 10% 16V X7R-CERM 0402
PP5V_S0_BLC_R — R9792 10K 1% 1/16W MF-LF 402
74LVC1G08GW SOT353 U9790
BLC_P_ON — R9791 10K 5% 1/16W MF-LF 402 — BLC_BST_R — R9790 10K 5% 1/16W MF-LF 402 — BLC_BST
C9792 0.1UF 10% 16V X7R-CERM 0402
BOOST_EN_GATE — Q9701 2N7002 SOT23-HF1 — BOOST_EN_L
R9793 10K 5% 1/16W MF-LF 402

PP5V_S0_BLC_R — R9725 10K 1% 1/10W MF-LF 603 — BLC_MCU_BV
Q9700 BSH111DG SOT23-3
BLC_MCU_PWM5_R — R9724 10K 1% 1/10W MF-LF 603
C9722 1000PF 5% 50V C0G-CERM 603
R9722 0 5% 1/16W MF-LF 402

PP5V_S0_BLC_R — C9720 2.2UF 10% 16V X5R 603
U9720 REF3333 SOT23-3 (IN, GND, OUT) — BLC_P3V3_REF
C9721 4.7UF 10% 6.3V X5R-CERM 603

D8 PROTO 2 BLC ADDING 3.3V VOLTAGE REFERENCE RDAR://11280328

BLC MCU

353S3748
U9770 L78M08ABDT DPAK (IN, GND, OUT)
PP12V_S0_BLC_VIN2 — PP8V_BLC
C9770 4.7UF 10% 16V X5R-CERM 0603
C9771 2.2UF 10% 25V X5R-CERM 603

SYNC_MASTER=D8_MLB — SYNC_DATE=08/27/2012
PAGE TITLE: Backlight Controller MCU
Apple Inc.
DRAWING NUMBER: 051-9505 — SIZE: D
REVISION: 8.0.0
BRANCH: prefsb
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SHEET: 80 OF 123

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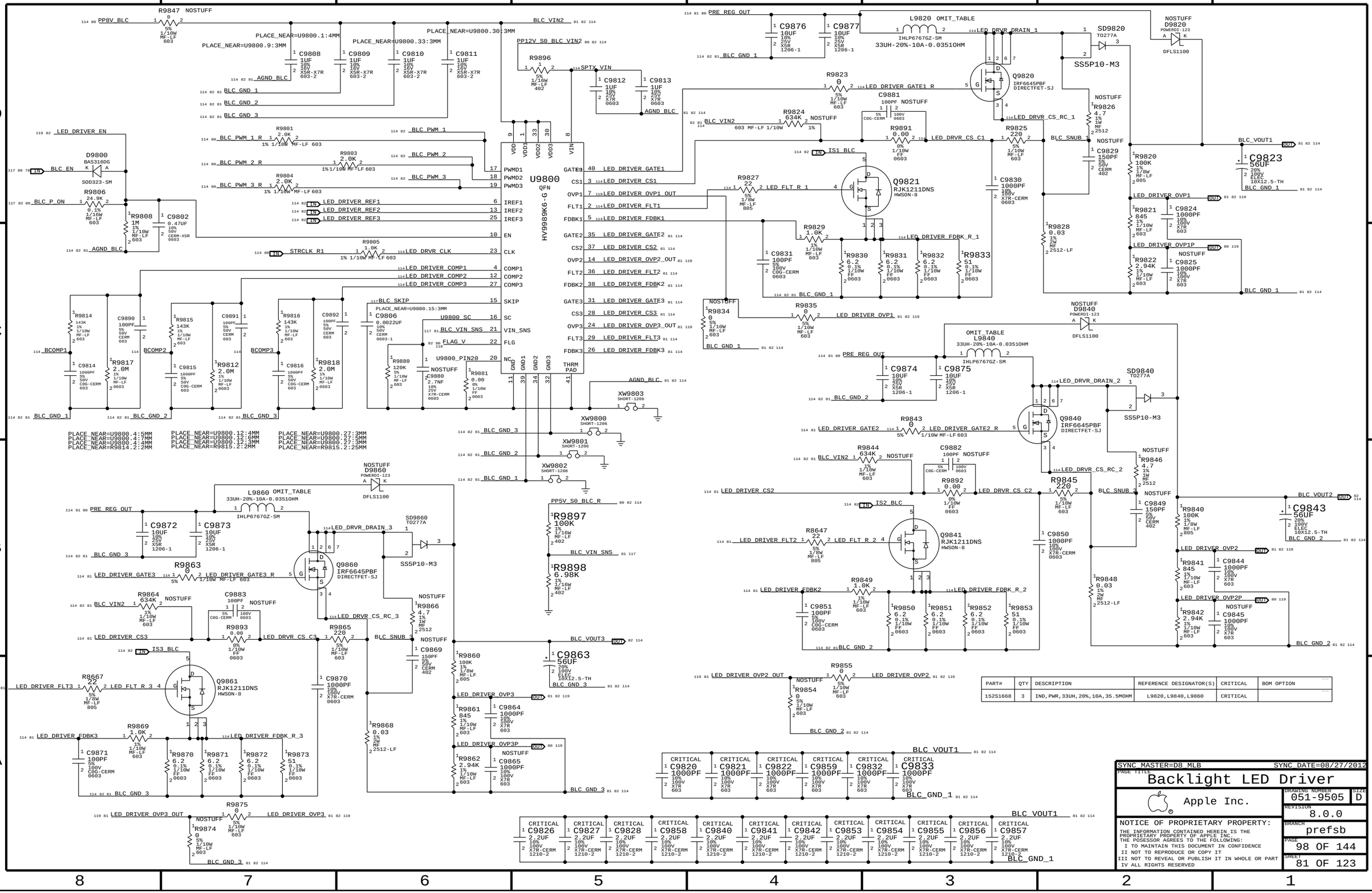

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	3	IND,PWR,33UH,20%,10A,35.5MOHM	L9820,L9840,L9860	CRITICAL	

Output Current Adjustment

IN-RUSH CURRENT LIMITER

OVP PROTECTION

Backlight Connector

BLC12V BYPASS STUFFING OPTION

	BYPASS	NO BYPASS
R9998:	STUFF	NOSTUFF
R9995:	NOSTUFF	STUFF
R9999:	STUFF	NOSTUFF
R9994:	NOSTUFF	STUFF
R9976:	STUFF	NOSTUFF

UVP PROTECTION

PWM <= 50% -> TURN ON BOOST
PWM > 50% -> TURN OFF BOOST

UVLO VIN2 BLC_BL

2.5V @12V = "1"
2.0V @10V = "0" (SHUTDOWN)

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: Backlight Controller

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D
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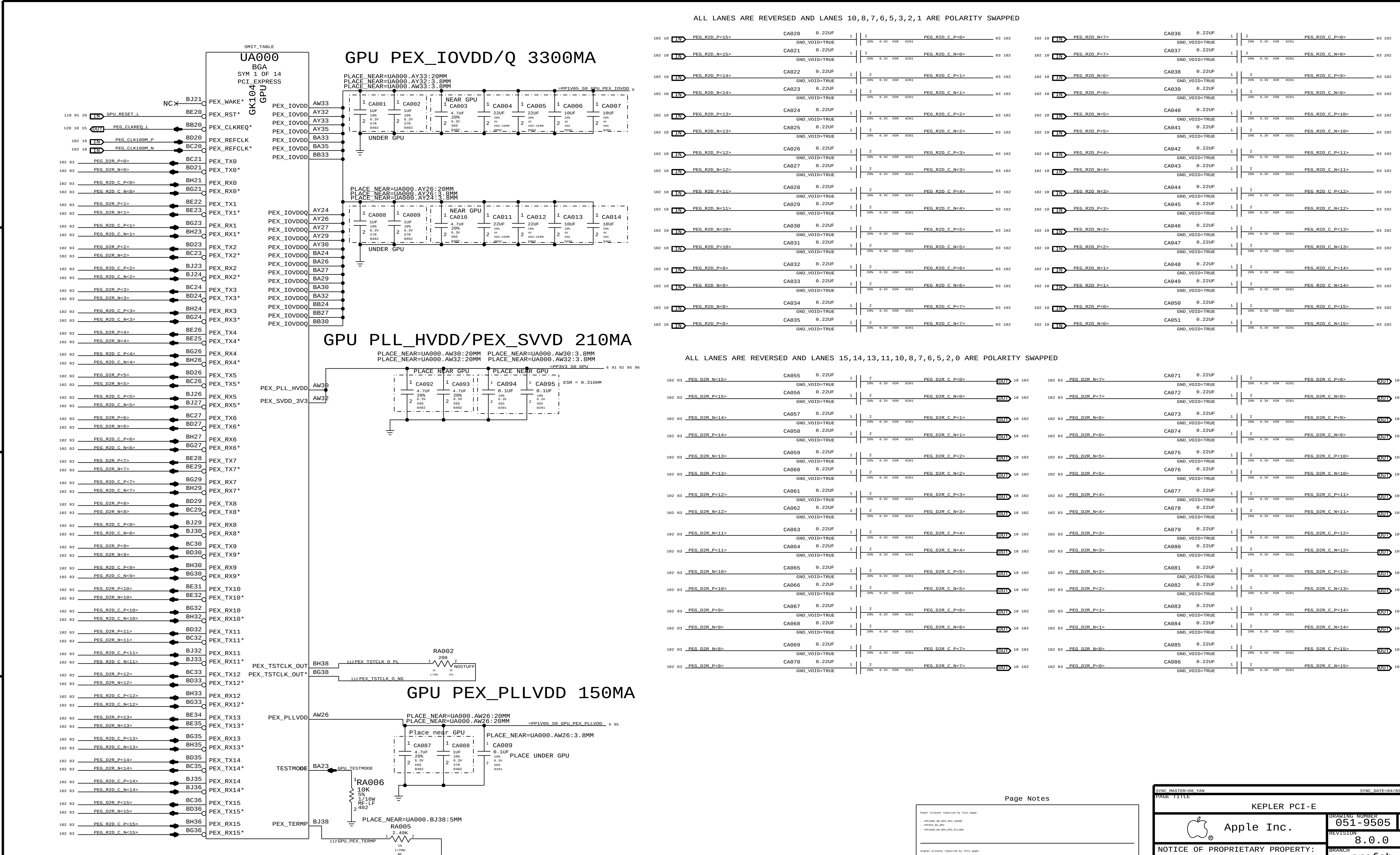

SYNC_MASTER=D8_YAN
SYNC_DATE=04/09/2012

PAGE TITLE
KEPLER PCI-E

Apple Inc.

DRAWING NUMBER 051-9505
SIZE D
REVISION 8.0.0
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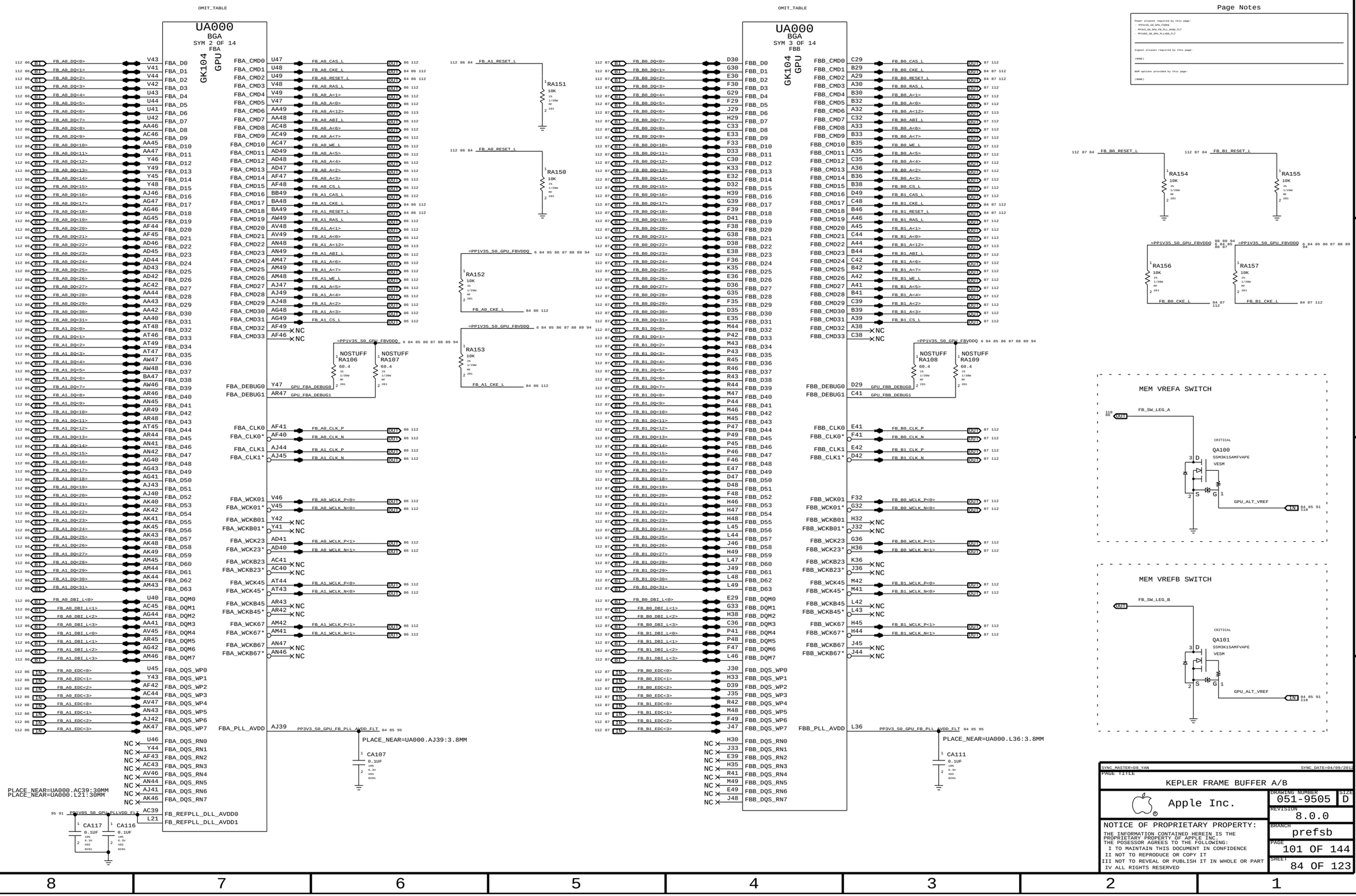
OMIT_TABLE
UA000
BGA
SYM 2 OF 14
FBA
GK104 GPU
FBA_D0
FBA_D1
FBA_D2
FBA_D3
FBA_D4
FBA_D5
FBA_D6
FBA_D7
FBA_D8
FBA_D9
FBA_D10
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FBA_D59
FBA_D60
FBA_D61
FBA_D62
FBA_D63
FBA_DQM0
FBA_DQM1
FBA_DQM2
FBA_DQM3
FBA_DQM4
FBA_DQM5
FBA_DQM6
FBA_DQM7
FBA_DQS_WP0
FBA_DQS_WP1
FBA_DQS_WP2
FBA_DQS_WP3
FBA_DQS_WP4
FBA_DQS_WP5
FBA_DQS_WP6
FBA_DQS_WP7
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FBA_DQS_RN1
FBA_DQS_RN2
FBA_DQS_RN3
FBA_DQS_RN4
FBA_DQS_RN5
FBA_DQS_RN6
FBA_DQS_RN7
FB_REFPLL_DLL_AVDD0
FB_REFPLL_DLL_AVDD1
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
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FBA_CMD26
FBA_CMD27
FBA_CMD28
FBA_CMD29
FBA_CMD30
FBA_CMD31
FBA_CMD32
FBA_CMD33
FBA_DEBUG0
FBA_DEBUG1
FBA_CLK0
FBA_CLK0*
FBA_CLK1
FBA_CLK1*
FBA_WCK01
FBA_WCK01*
FBA_WCKB01
FBA_WCKB01*
FBA_WCK23
FBA_WCK23*
FBA_WCKB23
FBA_WCKB23*
FBA_WCK45
FBA_WCK45*
FBA_WCKB45
FBA_WCKB45*
FBA_WCK67
FBA_WCK67*
FBA_WCKB67
FBA_WCKB67*
FBA_PLL_AVDD
FB_A0_RESET_L
FB_A1_RESET_L
FB_A0_CKE_L
FB_A1_CKE_L
FB_A0_CLK_P
FB_A0_CLK_N
FB_A1_CLK_P
FB_A1_CLK_N
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FB_A0_WCLK_N<0>
FB_A0_WCLK_P<1>
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FB_A1_WCLK_N<0>
FB_A1_WCLK_P<1>
FB_A1_WCLK_N<1>
RA151
RA150
RA152
RA153
NOSTUFF
RA106
RA107
CA107
CA117
CA116
PLACE_NEAR=UA000.AC39:30MM
PLACE_NEAR=UA000.L21:30MM
PLACE_NEAR=UA000.AJ39:3.8MM
OMIT_TABLE
UA000
BGA
SYM 3 OF 14
FBB
GK104 GPU
FBB_D0
FBB_D1
FBB_D2
FBB_D3
FBB_D4
FBB_D5
FBB_D6
FBB_D7
FBB_D8
FBB_D9
FBB_D10
FBB_D11
FBB_D12
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FBB_DQM5
FBB_DQM6
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FBB_DQS_WP6
FBB_DQS_WP7
FBB_DQS_RN0
FBB_DQS_RN1
FBB_DQS_RN2
FBB_DQS_RN3
FBB_DQS_RN4
FBB_DQS_RN5
FBB_DQS_RN6
FBB_DQS_RN7
FBB_CMD0
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FBB_CMD2
FBB_CMD3
FBB_CMD4
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FBB_WCKB67
FBB_WCKB67*
FBB_PLL_AVDD
FB_B0_RESET_L
FB_B1_RESET_L
FB_B0_CKE_L
FB_B1_CKE_L
FB_B0_CLK_P
FB_B0_CLK_N
FB_B1_CLK_P
FB_B1_CLK_N
FB_B0_WCLK_P<0>
FB_B0_WCLK_N<0>
FB_B0_WCLK_P<1>
FB_B0_WCLK_N<1>
FB_B1_WCLK_P<0>
FB_B1_WCLK_N<0>
FB_B1_WCLK_P<1>
FB_B1_WCLK_N<1>
RA154
RA155
RA156
RA157
NOSTUFF
RA108
RA109
CA111
PLACE_NEAR=UA000.L36:3.8MM
Page Notes
MEM VREFA SWITCH
MEM VREFB SWITCH
QA100
QA101
SSM3K15AMFVAPE
VESM
CRITICAL
GPU_ALT_VREF
SYNC_MASTER=D8_YAN
SYNC_DATE=04/09/2012
PAGE TITLE
KEPLER FRAME BUFFER A/B
Apple Inc.
DRAWING NUMBER
051-9505
SIZE
D
REVISION
8.0.0
BRANCH
prefsb
PAGE
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84 OF 123
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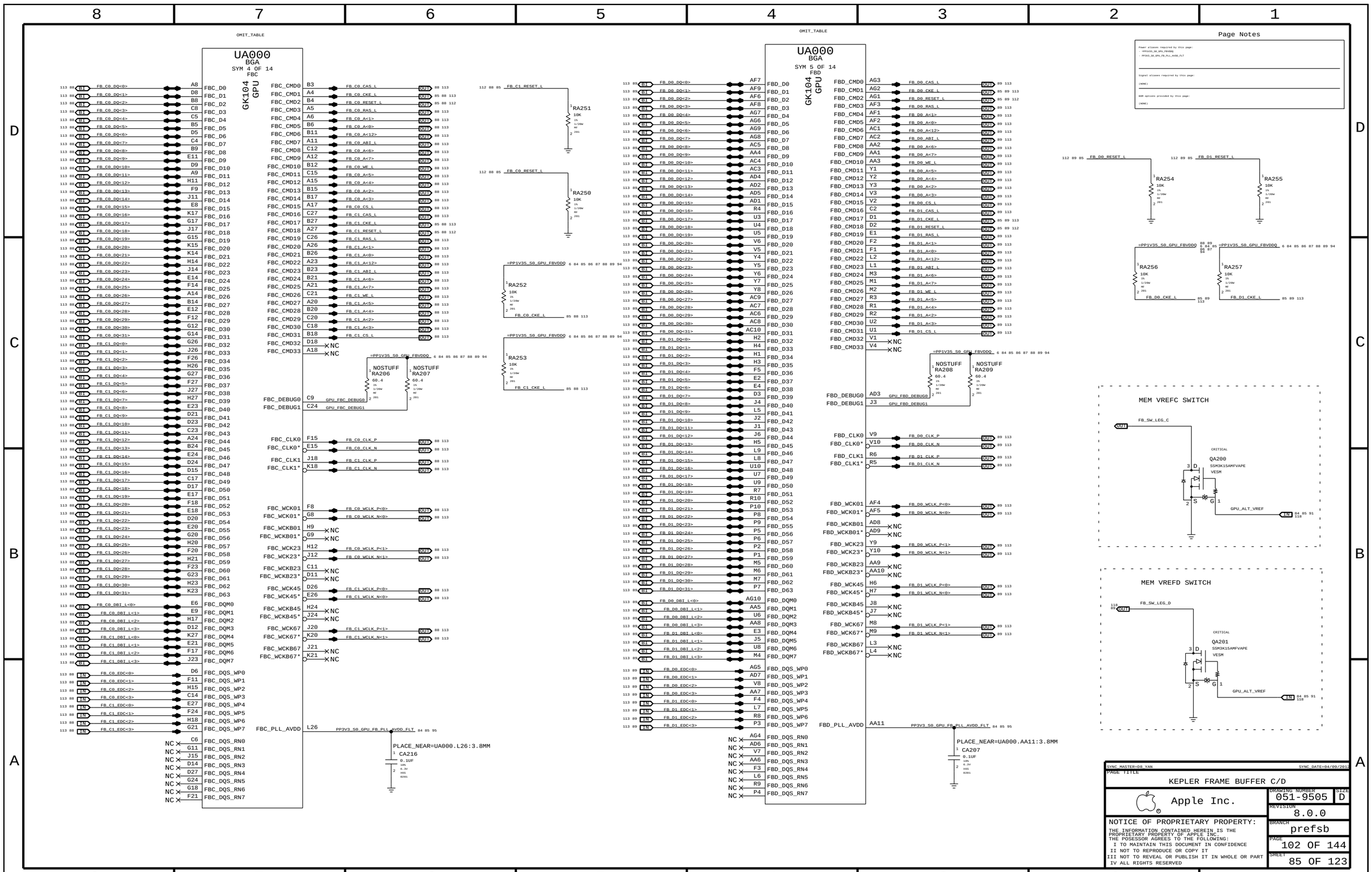
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BGA
SYM 4 OF 14
FBC
GK104
GPU
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FBC_CMD1
FBC_CMD2
FBC_CMD3
FBC_CMD4
FBC_CMD5
FBC_CMD6
FBC_CMD7
FBC_CMD8
FBC_CMD9
FBC_CMD10
FBC_CMD11
FBC_CMD12
FBC_CMD13
FBC_CMD14
FBC_CMD15
FBC_CMD16
FBC_CMD17
FBC_CMD18
FBC_CMD19
FBC_CMD20
FBC_CMD21
FBC_CMD22
FBC_CMD23
FBC_CMD24
FBC_CMD25
FBC_CMD26
FBC_CMD27
FBC_CMD28
FBC_CMD29
FBC_CMD30
FBC_CMD31
FBC_CMD32
FBC_CMD33
FBC_DEBUG0
FBC_DEBUG1
FBC_CLK0
FBC_CLK0*
FBC_CLK1
FBC_CLK1*
FBC_WCK01
FBC_WCK01*
FBC_WCKB01
FBC_WCKB01*
FBC_WCK23
FBC_WCK23*
FBC_WCKB23
FBC_WCKB23*
FBC_WCK45
FBC_WCK45*
FBC_WCKB45
FBC_WCKB45*
FBC_WCK67
FBC_WCK67*
FBC_WCKB67
FBC_WCKB67*
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FB_C0_RESET_L
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FB_C0_A<7>
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FB_C0_A<2>
FB_C0_A<3>
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FB_C1_RESET_L
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FB_C0_CLK_N
FB_C1_CLK_P
FB_C1_CLK_N
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RA250
RA252
RA253
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RA206
RA207
60.4
PP3V3_S0_GPU_FB_PLL_AVDD_FLT
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0.1UF
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UA000
BGA
SYM 5 OF 14
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GK104
GPU
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FBD_CMD1
FBD_CMD2
FBD_CMD3
FBD_CMD4
FBD_CMD5
FBD_CMD6
FBD_CMD7
FBD_CMD8
FBD_CMD9
FBD_CMD10
FBD_CMD11
FBD_CMD12
FBD_CMD13
FBD_CMD14
FBD_CMD15
FBD_CMD16
FBD_CMD17
FBD_CMD18
FBD_CMD19
FBD_CMD20
FBD_CMD21
FBD_CMD22
FBD_CMD23
FBD_CMD24
FBD_CMD25
FBD_CMD26
FBD_CMD27
FBD_CMD28
FBD_CMD29
FBD_CMD30
FBD_CMD31
FBD_CMD32
FBD_CMD33
FBD_DEBUG0
FBD_DEBUG1
FBD_CLK0
FBD_CLK0*
FBD_CLK1
FBD_CLK1*
FBD_WCK01
FBD_WCK01*
FBD_WCKB01
FBD_WCKB01*
FBD_WCK23
FBD_WCK23*
FBD_WCKB23
FBD_WCKB23*
FBD_WCK45
FBD_WCK45*
FBD_WCKB45
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FBD_WCKB67
FBD_WCKB67*
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FB_D0_RAS_L
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FB_D0_A<12>
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FB_D0_A<6>
FB_D0_A<7>
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FB_D0_A<5>
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FB_D0_A<3>
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FB_D1_CAS_L
FB_D1_CKE_L
FB_D1_RESET_L
FB_D1_RAS_L
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FB_D1_A<7>
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FB_D1_A<2>
FB_D1_A<3>
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FB_D0_CLK_N
FB_D1_CLK_P
FB_D1_CLK_N
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FB_D0_DBI_L<3>
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FB_D1_EDC<3>
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FBD_DQM1
FBD_DQM2
FBD_DQM3
FBD_DQM4
FBD_DQM5
FBD_DQM6
FBD_DQM7
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FBD_DQS_WP1
FBD_DQS_WP2
FBD_DQS_WP3
FBD_DQS_WP4
FBD_DQS_WP5
FBD_DQS_WP6
FBD_DQS_WP7
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FBD_DQS_RN1
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FBD_DQS_RN4
FBD_DQS_RN5
FBD_DQS_RN6
FBD_DQS_RN7
Page Notes
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MEM VREFD SWITCH
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FB_SW_LEG_D
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QA201
SSM3K15AMFVAPE
VESM
CRITICAL
GPU_ALT_VREF
PLACE_NEAR=UA000.AA11:3.8MM
CA207
SYNC_MASTER=D8_YAN
SYNC_DATE=04/09/2013
PAGE TITLE
KEPLER FRAME BUFFER C/D
Apple Inc.
DRAWING NUMBER
051-9505
SIZE
D
REVISION
8.0.0
BRANCH
prefsb
PAGE
102 OF 144
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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

CK TERMINATION - A0

RA301 40.2 1% 1/20W MF 201 — FB_A0_CLK_P — FB_A0_CK_MID
RA302 40.2 1% 1/20W MF 201 — FB_A0_CK_MID — FB_A0_CLK_N
CA390 0.01UF 10% 10V X5R-CERM 0201

CK TERMINATION - A1

RA351 40.2 1% 1/20W MF 201 — FB_A1_CLK_P — FB_A1_CK_MID
RA352 40.2 1% 1/20W MF 201 — FB_A1_CK_MID — FB_A1_CLK_N
CA391 0.01UF 10% 10V X5R-CERM 0201

RA300 120 1% 1/20W MF 201
RA304 1K 1% 1/20W MF 201
RA303 1K 1% 1/20W MF 201

MIRRORED

UA300
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(1 OF 2)

FB_A0_A<2>	K11	BA0/A2	
FB_A0_A<5>	H10	BA1/A5	
FB_A0_A<4>	H11	BA2/A4	
FB_A0_A<3>	K10	BA3/A3	
FB_A0_A<7>	H4	A8/A7	
FB_A0_A<1>	K5	A9/A1	
FB_A0_A<0>	K4	A10/A0	
FB_A0_A<6>	H5	A11/A6	
FB_A0_CKE_L	J3	CKE*	
FB_A0_CLK_P	J12	CK	
FB_A0_CLK_N	J11	CK*	
FB_A0_CS_L	L12	CS*	
FB_A0_WE_L	G12	WE*	
FB_A0_CAS_L	G3	CAS*	
FB_A0_RAS_L	L3	RAS*	
FB_A0_ZQ	J13	ZQ	
FB_A0_MF	J1	MF (MF=1)	
FB_A0_SEN	J10	SEN	
FB_A0_RESET_L	J2	RESET*	
FB_A0_ABI_L	J4	ABI*	
FB_A0_EDC<0>	R2	EDC0	
FB_A0_EDC<1>	R13	EDC1	
FB_A0_EDC<2>	C13	EDC2	
FB_A0_EDC<3>	C2	EDC3	
FB_A0_WCLK_P<0>	P4	WCK01	
FB_A0_WCLK_N<0>	P5	WCK01*	
FB_A0_WCLK_P<1>	D4	WCK23	
FB_A0_WCLK_N<1>	D5	WCK23*	

OMIT_TABLE

DBI1*	P13	FB_A0_DBI_L<1>	B1
DBI2*	D13	FB_A0_DBI_L<2>	B1
DBI0*	P2	FB_A0_DBI_L<0>	B1
DBI3*	D2	FB_A0_DBI_L<3>	B1
DQ0	U4	FB_A0_DQ<0>	B1
DQ1	U2	FB_A0_DQ<1>	B1
DQ2	T4	FB_A0_DQ<2>	B1
DQ3	T2	FB_A0_DQ<3>	B1
DQ4	N4	FB_A0_DQ<4>	B1
DQ5	N2	FB_A0_DQ<5>	B1
DQ6	M4	FB_A0_DQ<6>	B1
DQ7	M2	FB_A0_DQ<7>	B1
DQ8	U11	FB_A0_DQ<8>	B1
DQ9	U13	FB_A0_DQ<9>	B1
DQ10	T11	FB_A0_DQ<10>	B1
DQ11	T13	FB_A0_DQ<11>	B1
DQ12	N11	FB_A0_DQ<12>	B1
DQ13	N13	FB_A0_DQ<13>	B1
DQ14	M11	FB_A0_DQ<14>	B1
DQ15	M13	FB_A0_DQ<15>	B1
DQ16	A11	FB_A0_DQ<16>	B1
DQ17	A13	FB_A0_DQ<17>	B1
DQ18	B11	FB_A0_DQ<18>	B1
DQ19	B13	FB_A0_DQ<19>	B1
DQ20	E11	FB_A0_DQ<20>	B1
DQ21	E13	FB_A0_DQ<21>	B1
DQ22	F11	FB_A0_DQ<22>	B1
DQ23	F13	FB_A0_DQ<23>	B1
DQ24	A4	FB_A0_DQ<24>	B1
DQ25	A2	FB_A0_DQ<25>	B1
DQ26	B4	FB_A0_DQ<26>	B1
DQ27	B2	FB_A0_DQ<27>	B1
DQ28	E4	FB_A0_DQ<28>	B1
DQ29	E2	FB_A0_DQ<29>	B1
DQ30	F4	FB_A0_DQ<30>	B1
DQ31	F2	FB_A0_DQ<31>	B1
NC	A5	NC	
A12/RFU/NC	J5	FB_A0_A<12>	IN 84 113
NC	U5	NC	

OMIT_TABLE

NORMAL

UA350
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(1 OF 2)

FB_A1_A<2>	H11	BA0/A2	
FB_A1_A<5>	K10	BA1/A5	
FB_A1_A<4>	K11	BA2/A4	
FB_A1_A<3>	H10	BA3/A3	
FB_A1_A<7>	K4	A8/A7	
FB_A1_A<1>	H5	A9/A1	
FB_A1_A<0>	H4	A10/A0	
FB_A1_A<6>	K5	A11/A6	
FB_A1_CKE_L	J3	CKE*	
FB_A1_CLK_P	J12	CK	
FB_A1_CLK_N	J11	CK*	
FB_A1_CS_L	G12	CS*	
FB_A1_WE_L	L12	WE*	
FB_A1_CAS_L	L3	CAS*	
FB_A1_RAS_L	G3	RAS*	
FB_A1_ZQ	J13	ZQ	
FB_A1_MF	J1	MF (MF=0)	
FB_A1_SEN	J10	SEN	
FB_A1_RESET_L	J2	RESET*	
FB_A1_ABI_L	J4	ABI*	
FB_A1_EDC<0>	C2	EDC0	
FB_A1_EDC<1>	C13	EDC1	
FB_A1_EDC<2>	R13	EDC2	
FB_A1_EDC<3>	R2	EDC3	
FB_A1_WCLK_P<0>	D4	WCK01	
FB_A1_WCLK_N<0>	D5	WCK01*	
FB_A1_WCLK_P<1>	P4	WCK23	
FB_A1_WCLK_N<1>	P5	WCK23*	

OMIT_TABLE

DBI0*	D2	FB_A1_DBI_L<0>	B1
DBI1*	D13	FB_A1_DBI_L<1>	B1
DBI2*	P13	FB_A1_DBI_L<2>	B1
DBI3*	P2	FB_A1_DBI_L<3>	B1
DQ0	A4	FB_A1_DQ<0>	B1
DQ1	A2	FB_A1_DQ<1>	B1
DQ2	B4	FB_A1_DQ<2>	B1
DQ3	B2	FB_A1_DQ<3>	B1
DQ4	E4	FB_A1_DQ<4>	B1
DQ5	E2	FB_A1_DQ<5>	B1
DQ6	F4	FB_A1_DQ<6>	B1
DQ7	F2	FB_A1_DQ<7>	B1
DQ8	A11	FB_A1_DQ<8>	B1
DQ9	A13	FB_A1_DQ<9>	B1
DQ10	B11	FB_A1_DQ<10>	B1
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DQ15	F13	FB_A1_DQ<15>	B1
DQ16	U11	FB_A1_DQ<16>	B1
DQ17	U13	FB_A1_DQ<17>	B1
DQ18	T11	FB_A1_DQ<18>	B1
DQ19	T13	FB_A1_DQ<19>	B1
DQ20	N11	FB_A1_DQ<20>	B1
DQ21	N13	FB_A1_DQ<21>	B1
DQ22	M11	FB_A1_DQ<22>	B1
DQ23	M13	FB_A1_DQ<23>	B1
DQ24	U4	FB_A1_DQ<24>	B1
DQ25	U2	FB_A1_DQ<25>	B1
DQ26	T4	FB_A1_DQ<26>	B1
DQ27	T2	FB_A1_DQ<27>	B1
DQ28	N4	FB_A1_DQ<28>	B1
DQ29	N2	FB_A1_DQ<29>	B1
DQ30	M4	FB_A1_DQ<30>	B1
DQ31	M2	FB_A1_DQ<31>	B1
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NC	U5	NC	

UA300
32MX32-1.5GHZ-MFH
BGA
K4G10325FG-HC03
(2 OF 2)

VDD	C5, L11, L14, P11, R5, R10, C10, D11, G1, G4, G11, G14, L1, L4		
VDDQ	B1, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, B3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, B12, P3, P12, P14, T1, T3, T12, T14, B14, D1, D3, D12, D14, E5		
VSS	B5, L5, L10, P10, T5, T10, B10, D10, G5, G10, H1, H14, K1, K14, A1, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, A3, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, A12, R11, R12, R14, U1, U3, U12, U14, A14, C1, C3, C4, C11, C12		
VSSQ	A10, E1, E3, E12, E14, F5, F10, H2, H13, K2, A3, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, A12, R11, R12, R14, U1, U3, U12, U14, A14, C1, C3, C4, C11, C12		
VREFC	J14	FB_A0_VREFC	118 86
VREFD	U10	FB_A0_VREFD	118 86

OMIT_TABLE

PLACE CLOSE TO UA300

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CA301 10UF 20% 6.3V X5R 603-3
CA303 4.7UF 20% 6.3V X5R 402
CA304 4.7UF 20% 6.3V X5R 402
CA306 1UF 20% 6.3V X5R 0201
CA307 1UF 20% 6.3V X5R 0201
CA308 1UF 20% 6.3V X5R 0201
CA309 1UF 20% 6.3V X5R 0201
CA310 1UF 20% 6.3V X5R 0201
CA311 1UF 20% 6.3V X5R 0201
CA312 1UF 20% 6.3V X5R 0201
CA313 1UF 20% 6.3V X5R 0201
CA314 1UF 20% 6.3V X5R 0201
CA315 1UF 20% 6.3V X5R 0201
CA316 0.1UF 10% 6.3V X5R 201
CA317 0.1UF 10% 6.3V X5R 201
CA318 0.1UF 10% 6.3V X5R 201
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CA320 0.1UF 10% 6.3V X5R 201
CA321 0.1UF 10% 6.3V X5R 201
CA322 0.1UF 10% 6.3V X5R 201
CA323 0.1UF 10% 6.3V X5R 201
CA324 0.1UF 10% 6.3V X5R 201
CA325 0.1UF 10% 6.3V X5R 201

RA330 549 1% 1/20W MF 201 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 MM — FB_A0_VREFC
CA331 820PF 10% 50V CERM 0402
RA331 1.33K 1% 1/20W MF 201
RA334 931 1% 1/20W MF 201 — FB_SW_LEG_A

RA332 549 1% 1/20W MF 201 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm — FB_A0_VREFD
CA340 820PF 10% 50V CERM 0402
CA333 820PF 10% 50V CERM 0402
RA333 1.33K 1% 1/20W MF 201
RA335 931 1% 1/20W MF 201 — FB_SW_LEG_A

UA350
32MX32-1.5GHZ-MFL
BGA
K4G10325FG-HC03
(2 OF 2)

VDD	C5, C10, D11, G1, G4, G11, G14, L1, L4, L11, L14, P11, R5, R10		
VDDQ	B1, B3, B12, B14, D1, D3, D12, D14, E5, E10, F1, F3, F12, F14, G2, G13, H3, H12, K3, K12, L2, L13, M1, M3, M12, M14, N5, N10, P1, P3, P12, P14, T1, T3, T12, T14		
VSS	B5, B10, D10, G5, G10, H1, H14, K1, K14, L5, L10, P10, T5, T10, A1, A3, A12, A14, C1, C3, C4, C11, C12, C14, E1, E3, E12, E14, F5, F10, H2, H13, K2, K13, M5, M10, N1, N3, N12, N14, R1, R3, R4, R11, R12, R14, U1, U3, U12, U14		
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VREFC	J14	FB_A1_VREFC	118 86
VREFD	U10	FB_A1_VREFD	118 86

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ

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CA351 10UF 20% 6.3V X5R 603-3
CA353 4.7UF 20% 6.3V X5R 402
CA354 4.7UF 20% 6.3V X5R 402
CA356 1UF 20% 6.3V X5R 0201
CA357 1UF 20% 6.3V X5R 0201
CA358 1UF 20% 6.3V X5R 0201
CA359 1UF 20% 6.3V X5R 0201
CA360 1UF 20% 6.3V X5R 0201
CA361 1UF 20% 6.3V X5R 0201
CA362 1UF 20% 6.3V X5R 0201
CA363 1UF 20% 6.3V X5R 0201
CA364 1UF 20% 6.3V X5R 0201
CA365 1UF 20% 6.3V X5R 0201
CA366 0.1UF 10% 6.3V X5R 201
CA367 0.1UF 10% 6.3V X5R 201
CA368 0.1UF 10% 6.3V X5R 201
CA369 0.1UF 10% 6.3V X5R 201
CA370 0.1UF 10% 6.3V X5R 201
CA371 0.1UF 10% 6.3V X5R 201
CA372 0.1UF 10% 6.3V X5R 201
CA373 0.1UF 10% 6.3V X5R 201
CA374 0.1UF 10% 6.3V X5R 201
CA375 0.1UF 10% 6.3V X5R 201

RA336 549 1% 1/20W MF 201 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm — FB_A1_VREFC
CA381 820PF 10% 50V CERM 0402
RA337 1.33K 1% 1/20W MF 201
RA338 931 1% 1/20W MF 201 — FB_SW_LEG_A

RA339 549 1% 1/20W MF 201 — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm — FB_A1_VREFD
CA341 820PF 10% 50V CERM 0402
CA383 820PF 10% 50V CERM 0402
RA340 1.33K 1% 1/20W MF 201
RA341 931 1% 1/20W MF 201 — FB_SW_LEG_A

SYNC_MASTER=D8_YAN — SYNC_DATE=04/09/2013

PAGE TITLE: GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER	051-9505
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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

CK TERMINATION - B0

FB_B0_CLK_P — RA401 40.2 1% 1/20W MF 201 — FB_B0_CK_MID — RA402 40.2 1% 1/20W MF 201 — FB_B0_CLK_N

PLACE_NEAR=UA400.J12:20MM

PLACE_NEAR=UA400.J11:20MM

CA490 0.01UF 10% 10V X5R-CERM 0201

CK TERMINATION - B1

FB_B1_CLK_P — RA451 40.2 1% 1/20W MF 201 — FB_B1_CK_MID — RA452 40.2 1% 1/20W MF 201 — FB_B1_CLK_N

PLACE_NEAR=UA450.J12:20MM

PLACE_NEAR=UA450.J11:20MM

CA491 0.01UF 10% 10V X5R-CERM 0201

MIRRORED

UA400 32MX32-1.5GHZ-MFH

BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

FB_B0_A<2>	K11	BA0/A2	
FB_B0_A<5>	H10	BA1/A5	
FB_B0_A<4>	H11	BA2/A4	
FB_B0_A<3>	K10	BA3/A3	
FB_B0_A<7>	H4	A8/A7	
FB_B0_A<1>	K5	A9/A1	
FB_B0_A<0>	K4	A10/A0	
FB_B0_A<6>	H5	A11/A6	
FB_B0_CKE_L	J3	CKE*	
FB_B0_CLK_P	J12	CK	
FB_B0_CLK_N	J11	CK*	
FB_B0_CS_L	L12	CS*	
FB_B0_WE_L	G12	WE*	
FB_B0_CAS_L	G3	CAS*	
FB_B0_RAS_L	L3	RAS*	
FB_B0_ZQ	J13	ZQ	
FB_B0_MF	J1	MF (MF=1)	
FB_B0_SEN	J10	SEN	
FB_B0_RESET_L	J2	RESET*	
FB_B0_ABI_L	J4	ABI*	
FB_B0_EDC<0>	R2	EDC0	
FB_B0_EDC<1>	R13	EDC1	
FB_B0_EDC<2>	C13	EDC2	
FB_B0_EDC<3>	C2	EDC3	
FB_B0_WCLK_P<0>	P4	WCK01	
FB_B0_WCLK_N<0>	P5	WCK01*	
FB_B0_WCLK_P<1>	D4	WCK23	
FB_B0_WCLK_N<1>	D5	WCK23*	

DBI1*	P13	FB_B0_DBI_L<1>	
DBI2*	D13	FB_B0_DBI_L<2>	
DBI0*	P2	FB_B0_DBI_L<0>	
DBI3*	D2	FB_B0_DBI_L<3>	
DQ0	U4	FB_B0_DQ<0>	
DQ1	U2	FB_B0_DQ<1>	
DQ2	T4	FB_B0_DQ<2>	
DQ3	T2	FB_B0_DQ<3>	
DQ4	N4	FB_B0_DQ<4>	
DQ5	N2	FB_B0_DQ<5>	
DQ6	M4	FB_B0_DQ<6>	
DQ7	M2	FB_B0_DQ<7>	
DQ8	U11	FB_B0_DQ<8>	
DQ9	U13	FB_B0_DQ<9>	
DQ10	T11	FB_B0_DQ<10>	
DQ11	T13	FB_B0_DQ<11>	
DQ12	N11	FB_B0_DQ<12>	
DQ13	N13	FB_B0_DQ<13>	
DQ14	M11	FB_B0_DQ<14>	
DQ15	M13	FB_B0_DQ<15>	
DQ16	A11	FB_B0_DQ<16>	
DQ17	A13	FB_B0_DQ<17>	
DQ18	B11	FB_B0_DQ<18>	
DQ19	B13	FB_B0_DQ<19>	
DQ20	E11	FB_B0_DQ<20>	
DQ21	E13	FB_B0_DQ<21>	
DQ22	F11	FB_B0_DQ<22>	
DQ23	F13	FB_B0_DQ<23>	
DQ24	A4	FB_B0_DQ<24>	
DQ25	A2	FB_B0_DQ<25>	
DQ26	B4	FB_B0_DQ<26>	
DQ27	B2	FB_B0_DQ<27>	
DQ28	E4	FB_B0_DQ<28>	
DQ29	E2	FB_B0_DQ<29>	
DQ30	F4	FB_B0_DQ<30>	
DQ31	F2	FB_B0_DQ<31>	
NC	A5	NC	
A12/RFU/NC	J5	FB_B0_A<12>	
NC	U5	NC	

UA400 32MX32-1.5GHZ-MFH

BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ	C5	
	L11	
	L14	
	P11	
	R5	
	R10	
	C10	
VDD	D11	
	G1	
	G4	
	G11	
	G14	
	L1	
	L4	
	B1	
	E10	
	F1	
	F3	
	F12	
	F14	
	G2	
	G13	
	H3	
	H12	
	K3	
	B3	
	K12	
	L2	
	L13	
VDDQ	M1	
	M3	
	M12	
	M14	
	N5	
	N10	
	P1	
	B12	
	P3	
	P12	
	P14	
	T1	
	T3	
	T12	
	T14	
	B14	
	D1	
	D3	
	D12	
	D14	
	E5	
FB_B0_VREFC	J14	VREFC
FB_B0_VREFD	A10	
	U10	VREFD

VSS	B5	
	L5	
	L10	
	P10	
	T5	
	T10	
	B10	
	D10	
	G5	
	G10	
	H1	
	H14	
	K1	
	K14	
	A1	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	A3	
	K13	
	M5	
	M10	
	N1	
	N3	
	N12	
VSSQ	N14	
	R1	
	R3	
	R4	
	A12	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm

FB_B0_VREFC — RA430 549 1% 1/20W MF 201 — CA431 820PF 10% 50V CERM 0402 — RA431 1.33K 1% 1/20W MF 201 — RA434 931 1% 1/20W MF 201 — FB_SW_LEG_B

PLACE CLOSE TO UA400

FB_B0_VREFD — RA432 549 1% 1/20W MF 201 — CA440 820PF 10% 50V CERM 0402 — CA433 820PF 10% 50V CERM 0402 — RA433 1.33K 1% 1/20W MF 201 — RA435 931 1% 1/20W MF 201 — FB_SW_LEG_B

NORMAL

UA450 32MX32-1.5GHZ-MFL

BGA
K4G10325FG-HC03
(1 OF 2)

OMIT_TABLE

FB_B1_A<2>	H11	BA0/A2	
FB_B1_A<5>	K10	BA1/A5	
FB_B1_A<4>	K11	BA2/A4	
FB_B1_A<3>	H10	BA3/A3	
FB_B1_A<7>	K4	A8/A7	
FB_B1_A<1>	H5	A9/A1	
FB_B1_A<0>	H4	A10/A0	
FB_B1_A<6>	K5	A11/A6	
FB_B1_CKE_L	J3	CKE*	
FB_B1_CLK_P	J12	CK	
FB_B1_CLK_N	J11	CK*	
FB_B1_CS_L	G12	CS*	
FB_B1_WE_L	L12	WE*	
FB_B1_CAS_L	L3	CAS*	
FB_B1_RAS_L	G3	RAS*	
FB_B1_ZQ	J13	ZQ	
FB_B1_MF	J1	MF (MF=0)	
FB_B1_SEN	J10	SEN	
FB_B1_RESET_L	J2	RESET*	
FB_B1_ABI_L	J4	ABI*	
FB_B1_EDC<0>	C2	EDC0	
FB_B1_EDC<1>	C13	EDC1	
FB_B1_EDC<2>	R13	EDC2	
FB_B1_EDC<3>	R2	EDC3	
FB_B1_WCLK_P<0>	D4	WCK01	
FB_B1_WCLK_N<0>	D5	WCK01*	
FB_B1_WCLK_P<1>	P4	WCK23	
FB_B1_WCLK_N<1>	P5	WCK23*	

DBI0*	D2	FB_B1_DBI_L<0>	
DBI1*	D13	FB_B1_DBI_L<1>	
DBI2*	P13	FB_B1_DBI_L<2>	
DBI3*	P2	FB_B1_DBI_L<3>	
DQ0	A4	FB_B1_DQ<0>	
DQ1	A2	FB_B1_DQ<1>	
DQ2	B4	FB_B1_DQ<2>	
DQ3	B2	FB_B1_DQ<3>	
DQ4	E4	FB_B1_DQ<4>	
DQ5	E2	FB_B1_DQ<5>	
DQ6	F4	FB_B1_DQ<6>	
DQ7	F2	FB_B1_DQ<7>	
DQ8	A11	FB_B1_DQ<8>	
DQ9	A13	FB_B1_DQ<9>	
DQ10	B11	FB_B1_DQ<10>	
DQ11	B13	FB_B1_DQ<11>	
DQ12	E11	FB_B1_DQ<12>	
DQ13	E13	FB_B1_DQ<13>	
DQ14	F11	FB_B1_DQ<14>	
DQ15	F13	FB_B1_DQ<15>	
DQ16	U11	FB_B1_DQ<16>	
DQ17	U13	FB_B1_DQ<17>	
DQ18	T11	FB_B1_DQ<18>	
DQ19	T13	FB_B1_DQ<19>	
DQ20	N11	FB_B1_DQ<20>	
DQ21	N13	FB_B1_DQ<21>	
DQ22	M11	FB_B1_DQ<22>	
DQ23	M13	FB_B1_DQ<23>	
DQ24	U4	FB_B1_DQ<24>	
DQ25	U2	FB_B1_DQ<25>	
DQ26	T4	FB_B1_DQ<26>	
DQ27	T2	FB_B1_DQ<27>	
DQ28	N4	FB_B1_DQ<28>	
DQ29	N2	FB_B1_DQ<29>	
DQ30	M4	FB_B1_DQ<30>	
DQ31	M2	FB_B1_DQ<31>	
NC	A5	NC	
A12/RFU/NC	J5	FB_B1_A<12>	
NC	U5	NC	

UA450 32MX32-1.5GHZ-MFL

BGA
K4G10325FG-HC03
(2 OF 2)

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ	C5	
	C10	
	D11	
	G1	
	G4	
	G11	
	G14	
	L1	
	L4	
	L11	
	L14	
	P11	
	R5	
	R10	
VDD	B1	
	B3	
	B12	
	B14	
	D1	
	D3	
	D12	
	D14	
	E5	
	E10	
	F1	
	F3	
	F12	
	F14	
	G2	
	G13	
	H3	
	H12	
	K3	
	K12	
	L2	
	L13	
VDDQ	M1	
	M3	
	M12	
	M14	
	N5	
	N10	
	P1	
	P3	
	P12	
	P14	
	T1	
	T3	
	T12	
	T14	
FB_B1_VREFC	J14	VREFC
FB_B1_VREFD	A10	
	U10	VREFD

VSS	B5	
	B10	
	D10	
	G5	
	G10	
	H1	
	H14	
	K1	
	K14	
	L5	
	L10	
	P10	
	T5	
	T10	
	A1	
	A3	
	A12	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	K13	
	M5	
	M10	
	N1	
	N3	
	N12	
VSSQ	N14	
	R1	
	R3	
	R4	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	

MIN_NECK_WIDTH=0.1 mm
MIN_LINE_WIDTH=0.25 MM

FB_B1_VREFC — RA436 549 1% 1/20W MF 201 — CA481 820PF 10% 50V CERM 0402 — RA437 1.33K 1% 1/20W MF 201 — RA438 931 1% 1/20W MF 201 — FB_SW_LEG_B

PLACE CLOSE TO UA450

FB_B1_VREFD — RA439 549 1% 1/20W MF 201 — CA441 820PF 10% 50V CERM 0402 — CA483 820PF 10% 50V CERM 0402 — RA440 1.33K 1% 1/20W MF 201 — RA441 931 1% 1/20W MF 201 — FB_SW_LEG_B

SYNC_MASTER=D8_YAN	SYNC_DATE=04/09/2012
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-9505 SIZE D
	REVISION 8.0.0
	BRANCH prefsb
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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

CK TERMINATION - C0

RA501 40.2 1% 1/20W MF 201 — FB_C0_CLK_P — FB_C0_CK_MID — RA502 40.2 1% 1/20W MF 201 — FB_C0_CLK_N

PLACE_NEAR=UA500.J12:20MM — PLACE_NEAR=UA500.J11:20MM

CA590 0.01UF 10% 10V X5R-CERM 0201

CK TERMINATION - C1

RA551 40.2 1% 1/20W MF 201 — FB_C1_CLK_P — FB_C1_CK_MID — RA552 40.2 1% 1/20W MF 201 — FB_C1_CLK_N

PLACE_NEAR=UA550.J12:20MM — PLACE_NEAR=UA550.J11:20MM

CA591 0.01UF 10% 10V X5R-CERM 0201

MIRRORED

UA500 32MX32-1.5GHZ-MFH

BGA
K4G10325FG-HC03
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FB_C0_A<2>	K11	BA0/A2
FB_C0_A<5>	H10	BA1/A5
FB_C0_A<4>	H11	BA2/A4
FB_C0_A<3>	K10	BA3/A3
FB_C0_A<7>	H4	A8/A7
FB_C0_A<1>	K5	A9/A1
FB_C0_A<0>	K4	A10/A0
FB_C0_A<6>	H5	A11/A6
FB_C0_CKE_L	J3	CKE*
FB_C0_CLK_P	J12	CK
FB_C0_CLK_N	J11	CK*
FB_C0_CS_L	L12	CS*
FB_C0_WE_L	G12	WE*
FB_C0_CAS_L	G3	CAS*
FB_C0_RAS_L	L3	RAS*
FB_C0_ZQ	J13	ZQ
FB_C0_MF	J1	MF (MF=1)
FB_C0_SEN	J10	SEN
FB_C0_RESET_L	J2	RESET*
FB_C0_ABI_L	J4	ABI*
FB_C0_EDC<0>	R2	EDC0
FB_C0_EDC<1>	R13	EDC1
FB_C0_EDC<2>	C13	EDC2
FB_C0_EDC<3>	C2	EDC3
FB_C0_WCLK_P<0>	P4	WCK01
FB_C0_WCLK_N<0>	P5	WCK01*
FB_C0_WCLK_P<1>	D4	WCK23
FB_C0_WCLK_N<1>	D5	WCK23*

OMIT_TABLE

DBI1*	P13	FB_C0_DBI_L<1>
DBI2*	D13	FB_C0_DBI_L<2>
DBI0*	P2	FB_C0_DBI_L<0>
DBI3*	D2	FB_C0_DBI_L<3>
DQ0	U4	FB_C0_DQ<0>
DQ1	U2	FB_C0_DQ<1>
DQ2	T4	FB_C0_DQ<2>
DQ3	T2	FB_C0_DQ<3>
DQ4	N4	FB_C0_DQ<4>
DQ5	N2	FB_C0_DQ<5>
DQ6	M4	FB_C0_DQ<6>
DQ7	M2	FB_C0_DQ<7>
DQ8	U11	FB_C0_DQ<8>
DQ9	U13	FB_C0_DQ<9>
DQ10	T11	FB_C0_DQ<10>
DQ11	T13	FB_C0_DQ<11>
DQ12	N11	FB_C0_DQ<12>
DQ13	N13	FB_C0_DQ<13>
DQ14	M11	FB_C0_DQ<14>
DQ15	M13	FB_C0_DQ<15>
DQ16	A11	FB_C0_DQ<16>
DQ17	A13	FB_C0_DQ<17>
DQ18	B11	FB_C0_DQ<18>
DQ19	B13	FB_C0_DQ<19>
DQ20	E11	FB_C0_DQ<20>
DQ21	E13	FB_C0_DQ<21>
DQ22	F11	FB_C0_DQ<22>
DQ23	F13	FB_C0_DQ<23>
DQ24	A4	FB_C0_DQ<24>
DQ25	A2	FB_C0_DQ<25>
DQ26	B4	FB_C0_DQ<26>
DQ27	B2	FB_C0_DQ<27>
DQ28	E4	FB_C0_DQ<28>
DQ29	E2	FB_C0_DQ<29>
DQ30	F4	FB_C0_DQ<30>
DQ31	F2	FB_C0_DQ<31>
NC	A5	NC
A12/RFU/NC	J5	FB_C0_A<12>
NC	U5	NC

UA500 32MX32-1.5GHZ-MFH

BGA
K4G10325FG-HC03
(2 OF 2)

=PP1V35_S0_GPU_FBVDDQ	C5	VDD
	L11	
	L14	
	P11	
	R5	
	R10	
	C10	
	D11	
	G1	
	G4	
	G11	
	G14	
	L1	
	L4	
	B1	VDDQ
	E10	
	F1	
	F3	
	F12	
	F14	
	G2	
	G13	
	H3	
	H12	
	K3	
	B3	
	K12	
	L2	
	L13	
	M1	
	M3	
	M12	
	M14	
	N5	
	N10	
	P1	
	B12	
	P3	
	P12	
	P14	
	T1	
	T3	
	T12	
	T14	
	B14	
	D1	
	D3	
	D12	
	D14	
	E5	
FB_C0_VREFC	J14	VREFC
FB_C0_VREFD	A10	VREFD
	U10	

CA500 10UF 20% 6.3V X5R 603-3 — CA501 10UF 20% 6.3V X5R 603-3

CA503 4.7UF 20% 6.3V X5R 402 — CA504 4.7UF 20% 6.3V X5R 402

CA506 1UF 20% 6.3V X5R 0201 — CA507 1UF 20% 6.3V X5R 0201 — CA508 1UF 20% 6.3V X5R 0201 — CA509 1UF 20% 6.3V X5R 0201

CA510 1UF 20% 6.3V X5R 0201 — CA511 1UF 20% 6.3V X5R 0201 — CA512 1UF 20% 6.3V X5R 0201 — CA513 1UF 20% 6.3V X5R 0201

CA514 1UF 20% 6.3V X5R 0201 — CA515 1UF 20% 6.3V X5R 0201 — CA516 0.1UF 10% 6.3V X5R 201 — CA517 0.1UF 10% 6.3V X5R 201

CA518 0.1UF 10% 6.3V X5R 201 — CA519 0.1UF 10% 6.3V X5R 201 — CA520 0.1UF 10% 6.3V X5R 201 — CA521 0.1UF 10% 6.3V X5R 201

CA522 0.1UF 10% 6.3V X5R 201 — CA523 0.1UF 10% 6.3V X5R 201 — CA524 0.1UF 10% 6.3V X5R 201 — CA525 0.1UF 10% 6.3V X5R 201

UA500 32MX32-1.5GHZ-MFH

BGA
K4G10325FG-HC03
(2 OF 2)

	B5	VSS
	L5	
	L10	
	P10	
	T5	
	T10	
	B10	
	D10	
	G5	
	G10	
	H1	
	H14	
	K1	
	K14	
	A1	VSSQ
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	A3	
	K13	
	M5	
	M10	
	N1	
	N3	
	N12	
	N14	
	R1	
	R3	
	R4	
	A12	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm

RA530 549 1% 1/20W MF 201 — PLACE_NEAR=UA500.J14:8.4MM

FB_C0_VREFC — CA531 820PF 10% 50V CERM 0402 — RA531 1.33K 1% 1/20W MF 201 — RA534 931 1% 1/20W MF 201 — FB_SW_LEG_C

PLACE CLOSE TO UA500

RA532 549 1% 1/20W MF 201 — PLACE_NEAR=UA500.U10:8.4MM

FB_C0_VREFD — CA540 820PF 10% 50V CERM 0402 — CA533 820PF 10% 50V CERM 0402 — RA533 1.33K 1% 1/20W MF 201 — RA535 931 1% 1/20W MF 201 — FB_SW_LEG_C

PLACE_NEAR=UA500.A10:30MM — PLACE_NEAR=UA500.U10:30MM

NORMAL

UA550 32MX32-1.5GHZ-MFL

BGA
K4G10325FG-HC03
(1 OF 2)

FB_C1_A<2>	H11	BA0/A2
FB_C1_A<5>	K10	BA1/A5
FB_C1_A<4>	K11	BA2/A4
FB_C1_A<3>	H10	BA3/A3
FB_C1_A<7>	K4	A8/A7
FB_C1_A<1>	H5	A9/A1
FB_C1_A<0>	H4	A10/A0
FB_C1_A<6>	K5	A11/A6
FB_C1_CKE_L	J3	CKE*
FB_C1_CLK_P	J12	CK
FB_C1_CLK_N	J11	CK*
FB_C1_CS_L	G12	CS*
FB_C1_WE_L	L12	WE*
FB_C1_CAS_L	L3	CAS*
FB_C1_RAS_L	G3	RAS*
FB_C1_ZQ	J13	ZQ
FB_C1_MF	J1	MF (MF=0)
FB_C1_SEN	J10	SEN
FB_C1_RESET_L	J2	RESET*
FB_C1_ABI_L	J4	ABI*
FB_C1_EDC<0>	C2	EDC0
FB_C1_EDC<1>	C13	EDC1
FB_C1_EDC<2>	R13	EDC2
FB_C1_EDC<3>	R2	EDC3
FB_C1_WCLK_P<0>	D4	WCK01
FB_C1_WCLK_N<0>	D5	WCK01*
FB_C1_WCLK_P<1>	P4	WCK23
FB_C1_WCLK_N<1>	P5	WCK23*

OMIT_TABLE

DBI0*	D2	FB_C1_DBI_L<0>
DBI1*	D13	FB_C1_DBI_L<1>
DBI2*	P13	FB_C1_DBI_L<2>
DBI3*	P2	FB_C1_DBI_L<3>
DQ0	A4	FB_C1_DQ<0>
DQ1	A2	FB_C1_DQ<1>
DQ2	B4	FB_C1_DQ<2>
DQ3	B2	FB_C1_DQ<3>
DQ4	E4	FB_C1_DQ<4>
DQ5	E2	FB_C1_DQ<5>
DQ6	F4	FB_C1_DQ<6>
DQ7	F2	FB_C1_DQ<7>
DQ8	A11	FB_C1_DQ<8>
DQ9	A13	FB_C1_DQ<9>
DQ10	B11	FB_C1_DQ<10>
DQ11	B13	FB_C1_DQ<11>
DQ12	E11	FB_C1_DQ<12>
DQ13	E13	FB_C1_DQ<13>
DQ14	F11	FB_C1_DQ<14>
DQ15	F13	FB_C1_DQ<15>
DQ16	U11	FB_C1_DQ<16>
DQ17	U13	FB_C1_DQ<17>
DQ18	T11	FB_C1_DQ<18>
DQ19	T13	FB_C1_DQ<19>
DQ20	N11	FB_C1_DQ<20>
DQ21	N13	FB_C1_DQ<21>
DQ22	M11	FB_C1_DQ<22>
DQ23	M13	FB_C1_DQ<23>
DQ24	U4	FB_C1_DQ<24>
DQ25	U2	FB_C1_DQ<25>
DQ26	T4	FB_C1_DQ<26>
DQ27	T2	FB_C1_DQ<27>
DQ28	N4	FB_C1_DQ<28>
DQ29	N2	FB_C1_DQ<29>
DQ30	M4	FB_C1_DQ<30>
DQ31	M2	FB_C1_DQ<31>
NC	A5	NC
A12/RFU/NC	J5	FB_C1_A<12>
NC	U5	NC

RA550 120 1% 1/20W MF 201 — RA554 1K 1% 1/20W MF 201 — RA553 1K 1% 1/20W MF 201

PLACE_NEAR=UA550.J13:8.4MM — PLACE_NEAR=UA550.J10:8.4MM

UA550 32MX32-1.5GHZ-MFL

BGA
K4G10325FG-HC03
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	B5	VSS
	B10	
	D10	
	G5	
	G10	
	H1	
	H14	
	K1	
	K14	
	L5	
	L10	
	P10	
	T5	
	T10	
	A1	VSSQ
	A3	
	A12	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	K13	
	M5	
	M10	
	N1	
	N3	
	N12	
	N14	
	R1	
	R3	
	R4	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	

OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ

CA550 10UF 20% 6.3V X5R 603-3 — CA551 10UF 20% 6.3V X5R 603-3

CA553 4.7UF 20% 6.3V X5R 402 — CA554 4.7UF 20% 6.3V X5R 402

CA556 1UF 20% 6.3V X5R 0201 — CA557 1UF 20% 6.3V X5R 0201 — CA558 1UF 20% 6.3V X5R 0201 — CA559 1UF 20% 6.3V X5R 0201

CA560 1UF 20% 6.3V X5R 0201 — CA561 1UF 20% 6.3V X5R 0201 — CA562 1UF 20% 6.3V X5R 0201 — CA563 1UF 20% 6.3V X5R 0201

CA564 1UF 20% 6.3V X5R 0201 — CA565 1UF 20% 6.3V X5R 0201 — CA566 0.1UF 10% 6.3V X5R 201 — CA567 0.1UF 10% 6.3V X5R 201

CA568 0.1UF 10% 6.3V X5R 201 — CA569 0.1UF 10% 6.3V X5R 201 — CA570 0.1UF 10% 6.3V X5R 201 — CA571 0.1UF 10% 6.3V X5R 201

CA572 0.1UF 10% 6.3V X5R 201 — CA573 0.1UF 10% 6.3V X5R 201 — CA574 0.1UF 10% 6.3V X5R 201 — CA575 0.1UF 10% 6.3V X5R 201

FB_C1_VREFC — VREFC

FB_C1_VREFD — VREFD

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm

RA536 549 1% 1/20W MF 201 — PLACE_NEAR=UA550.J14:8.4MM

FB_C1_VREFC — CA581 820PF 10% 50V CERM 0402 — RA537 1.33K 1% 1/20W MF 201 — RA538 931 1% 1/20W MF 201 — FB_SW_LEG_C

RA539 549 1% 1/20W MF 201 — PLACE_NEAR=UA550.U10:8.4MM

FB_C1_VREFD — CA541 820PF 10% 50V CERM 0402 — CA583 820PF 10% 50V CERM 0402 — RA540 1.33K 1% 1/20W MF 201 — RA541 931 1% 1/20W MF 201 — FB_SW_LEG_C

PLACE_NEAR=UA550.A10:8.4MM — PLACE_NEAR=UA550.U10:8.4MM

SYNC_MASTER=D8_YAN — SYNC_DATE=04/09/2012

PAGE TITLE

GDDR5 FRAME BUFFER C

Apple Inc.

DRAWING NUMBER 051-9505 — SIZE D

REVISION 8.0.0

BRANCH prefsb

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Page Notes

Power aliases required by this page:

- =PP1V35_S0_GPU_FBVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

CK TERMINATION - D0

FB_D0_CLK_P — RA601 40.2 1% 1/20W MF 201 — FB_D0_CK_MID — RA602 40.2 1% 1/20W MF 201 — FB_D0_CLK_N

PLACE_NEAR=UA600.J12:20MM, PLACE_NEAR=UA600.J11:20MM

CA690 0.01UF 10% 10V X5R-CERM 0201

CK TERMINATION - D1

FB_D1_CLK_P — RA651 40.2 1% 1/20W MF 201 — FB_D1_CK_MID — RA652 40.2 1% 1/20W MF 201 — FB_D1_CLK_N

PLACE_NEAR=UA650.J12:20MM, PLACE_NEAR=UA650.J11:20MM

CA691 0.01UF 10% 10V X5R-CERM 0201

PLACE_NEAR=UA600.J1:30MM

=PP1V35_S0_GPU_FBVDDQ — RA600 120 1% 1/20W MF 201 — FB_D0_MF

RA604 1K 1% 1/20W MF 201 — FB_D0_SEN

RA603 1K 1% 1/20W MF 201 — FB_D0_RESET_L

PLACE_NEAR=UA600.J10:8.4MM

PLACE_NEAR=UA650.J13:8.4MM

=PP1V35_S0_GPU_FBVDDQ — RA650 120 1% 1/20W MF 201 — FB_D1_MF

RA654 1K 1% 1/20W MF 201 — FB_D1_SEN

RA653 1K 1% 1/20W MF 201 — FB_D1_RESET_L

PLACE_NEAR=UA650.J10:8.4MM

UA600 32MX32-1.5GHZ-MFH

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MIRRORED

OMIT_TABLE

FB_D0_A<2>	K11	BA0/A2	
FB_D0_A<5>	H10	BA1/A5	
FB_D0_A<4>	H11	BA2/A4	
FB_D0_A<3>	K10	BA3/A3	
FB_D0_A<7>	H4	A8/A7	
FB_D0_A<1>	K5	A9/A1	
FB_D0_A<0>	K4	A10/A0	
FB_D0_A<6>	H5	A11/A6	
FB_D0_CKE_L	J3	CKE*	
FB_D0_CLK_P	J12	CK	
FB_D0_CLK_N	J11	CK*	
FB_D0_CS_L	L12	CS*	
FB_D0_WE_L	G12	WE*	
FB_D0_CAS_L	G3	CAS*	
FB_D0_RAS_L	L3	RAS*	
FB_D0_ZQ	J13	ZQ	
FB_D0_MF	J1	MF (MF=1)	
FB_D0_SEN	J10	SEN	
FB_D0_RESET_L	J2	RESET*	
FB_D0_ABI_L	J4	ABI*	
FB_D0_EDC<0>	R2	EDC0	
FB_D0_EDC<1>	R13	EDC1	
FB_D0_EDC<2>	C13	EDC2	
FB_D0_EDC<3>	C2	EDC3	
FB_D0_WCLK_P<0>	P4	WCK01	
FB_D0_WCLK_N<0>	P5	WCK01*	
FB_D0_WCLK_P<1>	D4	WCK23	
FB_D0_WCLK_N<1>	D5	WCK23*	

DBI1*	P13		FB_D0_DBI_L<1>
DBI2*	D13		FB_D0_DBI_L<2>
DBI0*	P2		FB_D0_DBI_L<0>
DBI3*	D2		FB_D0_DBI_L<3>
DQ0	U4		FB_D0_DQ<0>
DQ1	U2		FB_D0_DQ<1>
DQ2	T4		FB_D0_DQ<2>
DQ3	T2		FB_D0_DQ<3>
DQ4	N4		FB_D0_DQ<4>
DQ5	N2		FB_D0_DQ<5>
DQ6	M4		FB_D0_DQ<6>
DQ7	M2		FB_D0_DQ<7>
DQ8	U11		FB_D0_DQ<8>
DQ9	U13		FB_D0_DQ<9>
DQ10	T11		FB_D0_DQ<10>
DQ11	T13		FB_D0_DQ<11>
DQ12	N11		FB_D0_DQ<12>
DQ13	N13		FB_D0_DQ<13>
DQ14	M11		FB_D0_DQ<14>
DQ15	M13		FB_D0_DQ<15>
DQ16	A11		FB_D0_DQ<16>
DQ17	A13		FB_D0_DQ<17>
DQ18	B11		FB_D0_DQ<18>
DQ19	B13		FB_D0_DQ<19>
DQ20	E11		FB_D0_DQ<20>
DQ21	E13		FB_D0_DQ<21>
DQ22	F11		FB_D0_DQ<22>
DQ23	F13		FB_D0_DQ<23>
DQ24	A4		FB_D0_DQ<24>
DQ25	A2		FB_D0_DQ<25>
DQ26	B4		FB_D0_DQ<26>
DQ27	B2		FB_D0_DQ<27>
DQ28	E4		FB_D0_DQ<28>
DQ29	E2		FB_D0_DQ<29>
DQ30	F4		FB_D0_DQ<30>
DQ31	F2		FB_D0_DQ<31>
NC	A5		
A12/RFU/NC	J5		FB_D0_A<12>
NC	U5		

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BGA
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NORMAL

OMIT_TABLE

FB_D1_A<2>	H11	BA0/A2	
FB_D1_A<5>	K10	BA1/A5	
FB_D1_A<4>	K11	BA2/A4	
FB_D1_A<3>	H10	BA3/A3	
FB_D1_A<7>	K4	A8/A7	
FB_D1_A<1>	H5	A9/A1	
FB_D1_A<0>	H4	A10/A0	
FB_D1_A<6>	K5	A11/A6	
FB_D1_CKE_L	J3	CKE*	
FB_D1_CLK_P	J12	CK	
FB_D1_CLK_N	J11	CK*	
FB_D1_CS_L	G12	CS*	
FB_D1_WE_L	L12	WE*	
FB_D1_CAS_L	L3	CAS*	
FB_D1_RAS_L	G3	RAS*	
FB_D1_ZQ	J13	ZQ	
FB_D1_MF	J1	MF (MF=0)	
FB_D1_SEN	J10	SEN	
FB_D1_RESET_L	J2	RESET*	
FB_D1_ABI_L	J4	ABI*	
FB_D1_EDC<0>	C2	EDC0	
FB_D1_EDC<1>	C13	EDC1	
FB_D1_EDC<2>	R13	EDC2	
FB_D1_EDC<3>	R2	EDC3	
FB_D1_WCLK_P<0>	D4	WCK01	
FB_D1_WCLK_N<0>	D5	WCK01*	
FB_D1_WCLK_P<1>	P4	WCK23	
FB_D1_WCLK_N<1>	P5	WCK23*	

DBI0*	D2		FB_D1_DBI_L<0>
DBI1*	D13		FB_D1_DBI_L<1>
DBI2*	P13		FB_D1_DBI_L<2>
DBI3*	P2		FB_D1_DBI_L<3>
DQ0	A4		FB_D1_DQ<0>
DQ1	A2		FB_D1_DQ<1>
DQ2	B4		FB_D1_DQ<2>
DQ3	B2		FB_D1_DQ<3>
DQ4	E4		FB_D1_DQ<4>
DQ5	E2		FB_D1_DQ<5>
DQ6	F4		FB_D1_DQ<6>
DQ7	F2		FB_D1_DQ<7>
DQ8	A11		FB_D1_DQ<8>
DQ9	A13		FB_D1_DQ<9>
DQ10	B11		FB_D1_DQ<10>
DQ11	B13		FB_D1_DQ<11>
DQ12	E11		FB_D1_DQ<12>
DQ13	E13		FB_D1_DQ<13>
DQ14	F11		FB_D1_DQ<14>
DQ15	F13		FB_D1_DQ<15>
DQ16	U11		FB_D1_DQ<16>
DQ17	U13		FB_D1_DQ<17>
DQ18	T11		FB_D1_DQ<18>
DQ19	T13		FB_D1_DQ<19>
DQ20	N11		FB_D1_DQ<20>
DQ21	N13		FB_D1_DQ<21>
DQ22	M11		FB_D1_DQ<22>
DQ23	M13		FB_D1_DQ<23>
DQ24	U4		FB_D1_DQ<24>
DQ25	U2		FB_D1_DQ<25>
DQ26	T4		FB_D1_DQ<26>
DQ27	T2		FB_D1_DQ<27>
DQ28	N4		FB_D1_DQ<28>
DQ29	N2		FB_D1_DQ<29>
DQ30	M4		FB_D1_DQ<30>
DQ31	M2		FB_D1_DQ<31>
NC	A5		
A12/RFU/NC	J5		FB_D1_A<12>
NC	U5		

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BGA
K4G10325FG-HC03
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OMIT_TABLE

PLACE CLOSE TO UA600

=PP1V35_S0_GPU_FBVDDQ	C5	
	L11	
	L14	
	P11	
	R5	
	R10	
	C10	
	D11	VDD
	G1	
	G4	
	G11	
	G14	
	L1	
	L4	
	B1	
	E10	
	F1	
	F3	
	F12	
	F14	
	G2	
	G13	
	H3	
	H12	
	K3	
	B3	
	K12	
	L2	
	L13	
	M1	VDDQ
	M3	
	M12	
	M14	
	N5	
	N10	
	P1	
	B12	
	P3	
	P12	
	P14	
	T1	
	T3	
	T12	
	T14	
	B14	
	D1	
	D3	
	D12	
	D14	
	E5	
FB_D0_VREFC	J14	VREFC
FB_D0_VREFD	A10	
	U10	VREFD
	B5	
	L5	
	L10	
	P10	
	T5	
	T10	
	B10	
	D10	
	G5	VSS
	G10	
	H1	
	H14	
	K1	
	K14	
	A1	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	A3	
	K13	
	M5	VSSQ
	M10	
	N1	
	N3	
	N12	
	N14	
	R1	
	R3	
	R4	
	A12	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	

=PP1V35_S0_GPU_FBVDDQ — RA630 549 1% 1/20W MF 201 — FB_D0_VREFC

MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm

CA631 820PF 10% 50V CERM 0402 — RA631 1.33K 1% 1/20W MF 201 — RA634 931 1% 1/20W MF 201 — FB_SW_LEG_D

=PP1V35_S0_GPU_FBVDDQ — RA632 549 1% 1/20W MF 201 — FB_D0_VREFD

MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm

CA640 820PF 10% 50V CERM 0402, CA633 820PF 10% 50V CERM 0402 — RA633 1.33K 1% 1/20W MF 201 — RA635 931 1% 1/20W MF 201 — FB_SW_LEG_D

UA650 32MX32-1.5GHZ-MFL

BGA
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OMIT_TABLE

=PP1V35_S0_GPU_FBVDDQ	C5	
	C10	
	D11	
	G1	
	G4	
	G11	
	G14	VDD
	L1	
	L4	
	L11	
	L14	
	P11	
	R5	
	R10	
	B1	
	B3	
	B12	
	B14	
	D1	
	D3	
	D12	
	D14	
	E5	
	E10	
	F1	
	F3	
	F12	
	F14	
	G2	
	G13	
	H3	
	H12	
	K3	
	K12	
	L2	
	L13	
	M1	VDDQ
	M3	
	M12	
	M14	
	N5	
	N10	
	P1	
	P3	
	P12	
	P14	
	T1	
	T3	
	T12	
	T14	
FB_D1_VREFC	J14	VREFC
FB_D1_VREFD	A10	
	U10	VREFD
	B5	
	B10	
	D10	
	G5	
	G10	
	H1	
	H14	VSS
	K1	
	K14	
	L5	
	L10	
	P10	
	T5	
	T10	
	A1	
	A3	
	A12	
	A14	
	C1	
	C3	
	C4	
	C11	
	C12	
	C14	
	E1	
	E3	
	E12	
	E14	
	F5	
	F10	
	H2	
	H13	
	K2	
	K13	VSSQ
	M5	
	M10	
	N1	
	N3	
	N12	
	N14	
	R1	
	R3	
	R4	
	R11	
	R12	
	R14	
	U1	
	U3	
	U12	
	U14	

=PP1V35_S0_GPU_FBVDDQ — RA636 549 1% 1/20W MF 201 — FB_D1_VREFC

MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm

CA681 820PF 10% 50V CERM 0402 — RA637 1.33K 1% 1/20W MF 201 — RA638 931 1% 1/20W MF 201 — FB_SW_LEG_D

=PP1V35_S0_GPU_FBVDDQ — RA639 549 1% 1/20W MF 201 — FB_D1_VREFD

MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.1 mm

CA641 820PF 10% 50V CERM 0402, CA683 820PF 10% 50V CERM 0402 — RA640 1.33K 1% 1/20W MF 201 — RA641 931 1% 1/20W MF 201 — FB_SW_LEG_D

CA600 10UF 20% 6.3V X5R 603-3 — CA601 10UF 20% 6.3V X5R 603-3

CA603 4.7UF 20% 6.3V X5R 402 — CA604 4.7UF 20% 6.3V X5R 402

CA606 1UF 20% 6.3V X5R 0201 — CA607 1UF 20% 6.3V X5R 0201 — CA608 1UF 20% 6.3V X5R 0201 — CA609 1UF 20% 6.3V X5R 0201

CA610 1UF 20% 6.3V X5R 0201 — CA611 1UF 20% 6.3V X5R 0201 — CA612 1UF 20% 6.3V X5R 0201 — CA613 1UF 20% 6.3V X5R 0201

CA614 1UF 20% 6.3V X5R 0201 — CA615 1UF 20% 6.3V X5R 0201 — CA616 0.1UF 10% 6.3V X5R 201 — CA617 0.1UF 10% 6.3V X5R 201

CA618 0.1UF 10% 6.3V X5R 201 — CA619 0.1UF 10% 6.3V X5R 201 — CA620 0.1UF 10% 6.3V X5R 201 — CA621 0.1UF 10% 6.3V X5R 201

CA622 0.1UF 10% 6.3V X5R 201 — CA623 0.1UF 10% 6.3V X5R 201 — CA624 0.1UF 10% 6.3V X5R 201 — CA625 0.1UF 10% 6.3V X5R 201

CA650 10UF 20% 6.3V X5R 603-3 — CA651 10UF 20% 6.3V X5R 603-3

CA653 4.7UF 20% 6.3V X5R 402 — CA654 4.7UF 20% 6.3V X5R 402

CA656 1UF 20% 6.3V X5R 0201 — CA657 1UF 20% 6.3V X5R 0201 — CA658 1UF 20% 6.3V X5R 0201 — CA659 1UF 20% 6.3V X5R 0201

CA660 1UF 20% 6.3V X5R 0201 — CA661 1UF 20% 6.3V X5R 0201 — CA662 1UF 20% 6.3V X5R 0201 — CA663 1UF 20% 6.3V X5R 0201

CA664 1UF 20% 6.3V X5R 0201 — CA665 1UF 20% 6.3V X5R 0201 — CA666 0.1UF 10% 6.3V X5R 201 — CA667 0.1UF 10% 6.3V X5R 201

CA668 0.1UF 10% 6.3V X5R 201 — CA669 0.1UF 10% 6.3V X5R 201 — CA670 0.1UF 10% 6.3V X5R 201 — CA671 0.1UF 10% 6.3V X5R 201

CA672 0.1UF 10% 6.3V X5R 201 — CA673 0.1UF 10% 6.3V X5R 201 — CA674 0.1UF 10% 6.3V X5R 201 — CA675 0.1UF 10% 6.3V X5R 201

SYNC_MASTER=D8_YAN — SYNC_DATE=04/09/2012

PAGE TITLE: GDDR5 FRAME BUFFER D

Apple Inc.

DRAWING NUMBER: 051-9505 — SIZE: D

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DISABLE PHYS A, B & C FOR D8

OMIT_TABLE
CRITICAL

UA000
BGA
SYM 6 OF 14
GK104 GPU

NC BE18 IFPAB_RSET
118 GPU_IFPAB_PLLVDD BB15 IFPAB_PLLVDD
RA704 10K 1% 1/20W MF 201
118 GPU_IFPA_IOVDD BB17 BA17 IFPA_IOVDD
RA701 10K 1% 1/20W MF 201
118 GPU_IFPB_IOVDD BA18 BB18 IFPB_IOVDD
RA702 10K 1% 1/20W MF 201
NC BB14 IFPC_RSET
118 GPU_IFPC_PLLVDD BB12 IFPC_PLLVDD
RA719 10K 1% 1/20W MF 201
118 GPU_IFPC_IOVDD BA11 BA12 IFPC_IOVDD
RA703 10K 1% 1/20W MF 201
118 IFPD_RSET BE12 IFPD_RSET
PLACE_NEAR=UA000.BE12:5MM
RA706 1K 1% 1/20W MF 201
90 PP3V3_GPU_IFPX_PLLVDD_FLT BB11 IFPD_PLLVDD
PD FOR RSET
BA14 BA15 IFPD_IOVDD
118 IFPEF_RSET BF11 IFPEF_RSET
PLACE_NEAR=UA000.BF11:5MM
RA707 1K 1% 1/20W MF 201
90 PP3V3_GPU_IFPX_PLLVDD_FLT BB9 IFPEF_PLLVDD
BC8 BD8 IFPE_IOVDD
BC9 BD9 IFPF_IOVDD

IFPA_TXC* BD18 NC
IFPA_TXC BC18 NC
IFPA_TXD0* BG14 NC
IFPA_TXD0 BH14 NC
IFPA_TXD1* BC15 NC
IFPA_TXD1 BD15 NC
IFPA_TXD2* BE17 NC
IFPA_TXD2 BF17 NC
IFPA_TXD3* BC17 NC
IFPA_TXD3 BD17 NC
IFPB_TXC* BG18 NC
IFPB_TXC BH18 NC
IFPB_TXD4* BJ14 NC
IFPB_TXD4 BJ15 NC
IFPB_TXD5* BH15 NC
IFPB_TXD5 BG15 NC
IFPB_TXD6* BG17 NC
IFPB_TXD6 BH17 NC
IFPB_TXD7* BJ18 NC
IFPB_TXD7 BJ17 NC
IFPAB GPIO14 AW5 NC
IFPC_AUX_I2CW_SDA* BF2 NC
IFPC_AUX_I2CW_SCL BG2 NC
IFPC
IFPC_L3* BE11 NC
IFPC_L3 BD11 NC
IFPC_L2* BC12 NC
IFPC_L2 BD12 NC
IFPC_L1* BE14 NC
IFPC_L1 BF14 NC
IFPC_L0* BD14 NC
IFPC_L0 BC14 NC
GPIO15 AV6 NC
IFPD_AUX_I2CX_SDA* BF4 BG4 DP_INT_EG_AUX_N B1 75 90 111
IFPD_AUX_I2CX_SCL DP_INT_EG_AUX_P B1 75 90 111
IFPD
IFPD_L3* BH9 DP_INT_EG_ML_N<3> OUT 75 111
IFPD_L3 BG9 DP_INT_EG_ML_P<3> OUT 75 111
IFPD_L2* BG11 DP_INT_EG_ML_N<2> OUT 75 111
IFPD_L2 BH11 DP_INT_EG_ML_P<2> OUT 75 111
IFPD_L1* BJ11 DP_INT_EG_ML_N<1> OUT 75 111
IFPD_L1 BJ12 DP_INT_EG_ML_P<1> OUT 75 111
IFPD_L0* BH12 DP_INT_EG_ML_N<0> OUT 75 111
IFPD_L0 BG12 DP_INT_EG_ML_P<0> OUT 75 111
GPIO17 AW6 DP_INT_EG_HPD 75 117
IFPE_AUX_I2CY_SDA* BH3 BG3 DP_TBTSNK0_EG_AUXCH_N B1 90
IFPE_AUX_I2CY_SCL DP_TBTSNK0_EG_AUXCH_P B1 90
IFPEF
IFPE_L3* BE5 DP_TBTSNK0_ML_C_N<3> OUT 36 111
IFPE_L3 BD5 DP_TBTSNK0_ML_C_P<3> OUT 36 111
IFPE_L2* BE6 DP_TBTSNK0_ML_C_N<2> OUT 36 111
IFPE_L2 BD6 DP_TBTSNK0_ML_C_P<2> OUT 36 111
IFPE_L1* BG6 DP_TBTSNK0_ML_C_N<1> OUT 36 111
IFPE_L1 BF6 DP_TBTSNK0_ML_C_P<1> OUT 36 111
IFPE_L0* BF8 DP_TBTSNK0_ML_C_N<0> OUT 36 111
IFPE_L0 BE8 DP_TBTSNK0_ML_C_P<0> OUT 36 111
GPIO18 AW3 DP_TBTSNK0_HPD 36 111
IFPF_AUX_I2CZ_SDA* BH4 BJ4 DP_TBTSNK1_EG_AUXCH_N B1 90
IFPF_AUX_I2CZ_SCL DP_TBTSNK1_EG_AUXCH_P B1 90
IFPF_L3* BH6 DP_TBTSNK1_ML_C_N<3> OUT 36 111
IFPF_L3 BJ6 DP_TBTSNK1_ML_C_P<3> OUT 36 111
IFPF_L2* BG8 DP_TBTSNK1_ML_C_N<2> OUT 36 111
IFPF_L2 BH8 DP_TBTSNK1_ML_C_P<2> OUT 36 111
IFPF_L1* BJ8 DP_TBTSNK1_ML_C_N<1> OUT 36 111
IFPF_L1 BJ9 DP_TBTSNK1_ML_C_P<1> OUT 36 111
IFPF_L0* BE9 DP_TBTSNK1_ML_C_N<0> OUT 36 111
IFPF_L0 BF9 DP_TBTSNK1_ML_C_P<0> OUT 36 111
GPIO16 AW2 DP_TBTSNK1_HPD 36 111

PD FOR AUX CHANNELS (FOR NVIDIA)
111 90 75 DP_INT_EG_AUX_P
111 90 75 DP_INT_EG_AUX_N
RA714 100K 1% 1/20W MF 201
RA713 100K 1% 1/20W MF 201
90 DP_TBTSNK0_EG_AUXCH_P
90 DP_TBTSNK0_EG_AUXCH_N
RA715 100K 1% 1/20W MF 201
RA716 100K 1% 1/20W MF 201
90 DP_TBTSNK1_EG_AUXCH_P
90 DP_TBTSNK1_EG_AUXCH_N
RA717 100K 1% 1/20W MF 201
RA718 100K 1% 1/20W MF 201

CRITICAL
LA704 330-OHM-1.2A 0603
6 =PP3V3_S0_GPU_IFPX_PLLVDD IFPX PLLVDD
PP3V3_GPU_IFPX_PLLVDD_FLT 90
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=3.3V

PLACE BELOW GPU NEAR DISPLAY SECTION
PLACE_NEAR=UA000.BB11:20MM PLACE_NEAR=UA000.BB9:20MM
Place near GPU
CA719 4.7UF 20% 6.3V X6S 0402
CA715 1UF 10% 6.3V X7R 0402
PLACE_NEAR=UA000.BB11:3.8MM PLACE_NEAR=UA000.BB9:3.8MM
Place under GPU
CA718 0.1UF 10% 6.3V X6S 0201
CA712 0.1UF 10% 6.3V X6S 0201

PLACE_NEAR=UA000.BA14:20MM
LA705 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.05OHM
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2mm VOLTAGE=1.05V
6 =PP1V05_S0_GPU_IFPCD_IOVDD
PP1V05_GPU_IFPD_IOVDD_FLT
IFP CD IOVDD
PLACE_NEAR=UA000.BA14:20MM PLACE_NEAR=UA000.BA14:20MM
PLACE_NEAR=UA000.BA14:3.8MM PLACE_NEAR=UA000.BA15:3.8MM
Place near GPU
CA725 4.7UF 20% 6.3V X6S 0402
CA756 1UF 10% 6.3V X7R 0402
Place under GPU
CA757 0.1UF 10% 6.3V X6S 0201
CA758 0.1UF 10% 6.3V X6S 0201

PLACE_NEAR=UA000.BC8:20MM
LA706 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.05OHM
MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.2mm VOLTAGE=1.05V
6 =PP1V05_S0_GPU_IFPEF_IOVDD
PP1V05_GPU_IFPEF_IOVDD_FLT
IFP EF IOVDD
PLACE_NEAR=UA000.BC8:20MM PLACE_NEAR=UA000.BC8:5MM
PLACE_NEAR=UA000.BD8:20MM PLACE_NEAR=UA000.BD8:5MM
PLACE_NEAR=UA000.BD8:20MM PLACE_NEAR=UA000.BC9:5MM
PLACE_NEAR=UA000.BD9:20MM PLACE_NEAR=UA000.BD9:3.8MM
Place near GPU
CA733 4.7UF 20% 6.3V X6S 0402
CA734 4.7UF 20% 6.3V X6S 0402
CA735 1.0UF 20% 4V X6S 0201
CA736 1.0UF 20% 4V X6S 0201
Place under GPU
CA737 0.1UF 10% 6.3V X6S 0201
CA738 0.1UF 10% 6.3V X6S 0201
CA731 0.1UF 10% 6.3V X6S 0201
CA732 0.1UF 10% 6.3V X6S 0201

90 DP_TBTSNK0_EG_AUXCH_P = DP_TBTSNK0_AUXCH_C_P 36 111 MAKE_BASE=TRUE
90 DP_TBTSNK0_EG_AUXCH_N = DP_TBTSNK0_AUXCH_C_N 36 111 MAKE_BASE=TRUE
90 DP_TBTSNK1_EG_AUXCH_P = DP_TBTSNK1_AUXCH_C_P 36 111 MAKE_BASE=TRUE
90 DP_TBTSNK1_EG_AUXCH_N = DP_TBTSNK1_AUXCH_C_N 36 111 MAKE_BASE=TRUE

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012
PAGE TITLE
KEPLER EDP/DP/GPIO
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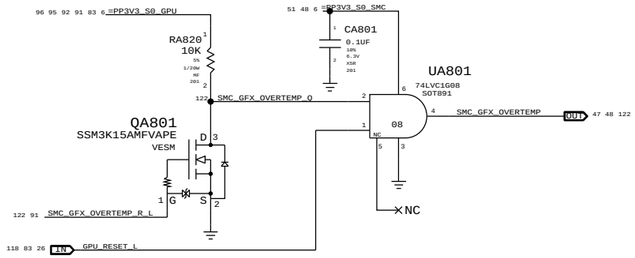
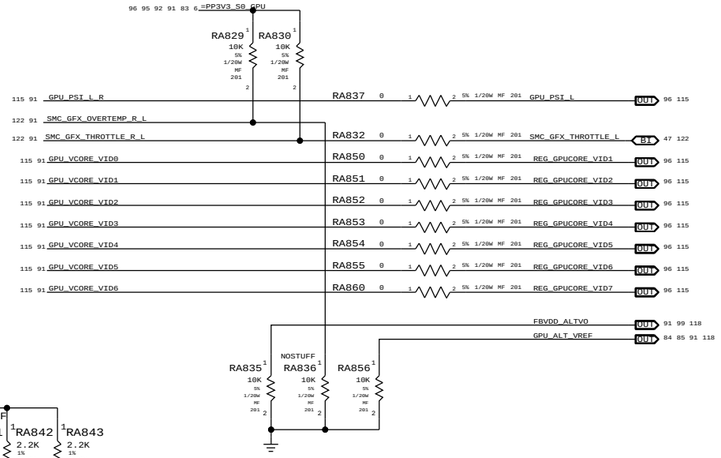
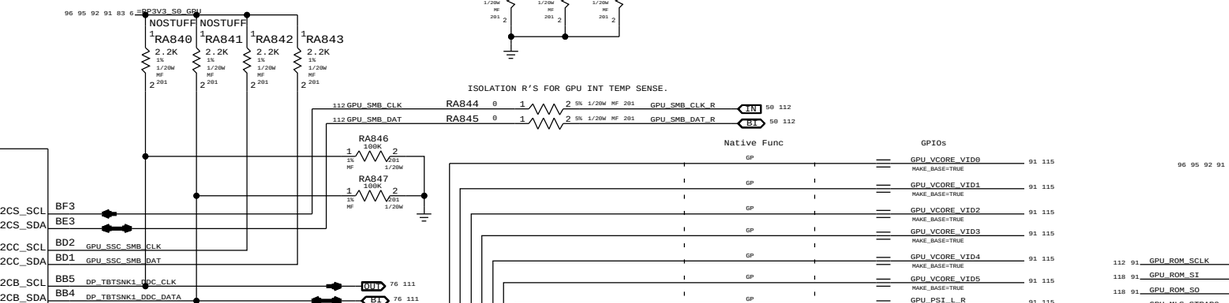
GPU overtemp masking

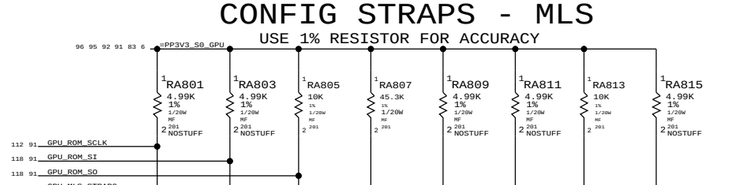




PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0175	1	RES,MF,20KOHM,1,1/20W,0201	RA804		FB:1G_SAMSUNG
118S0105	1	RES,MF,15KOHM,1,1/20W,0201	RA804		FB:1G_HYNIX
118S0385	1	RES,MF,45.3KOHM,1,1/20W,0201	RA804		FB:2G_SAMSUNG
118S0315	1	RES,MF,34.8KOHM,1,1/20W,0201	RA804		FB:2G_HYNIX
118S0175	1	RES,MF,20KOHM,1,1/20W,0201	RA812		GPU:104GTX
118S0105	1	RES,MF,15KOHM,1,1/20W,0201	RA812		GPU:104GT
118S0105	1	RES,MF,15KOHM,1,1/20W,0201	RA812		GPU:104GT2

GPU JTAG





CONFIG STRAPS - MLS

USE 1% RESISTOR FOR ACCURACY

SYNC_MASTER=D8_YAN SYNC_DATE=07/27/2013

PAGE TITLE

KEPLER GPIO/STRAPPING

Apple Inc.

DRAWING NUMBER 051-9505 SIZE D

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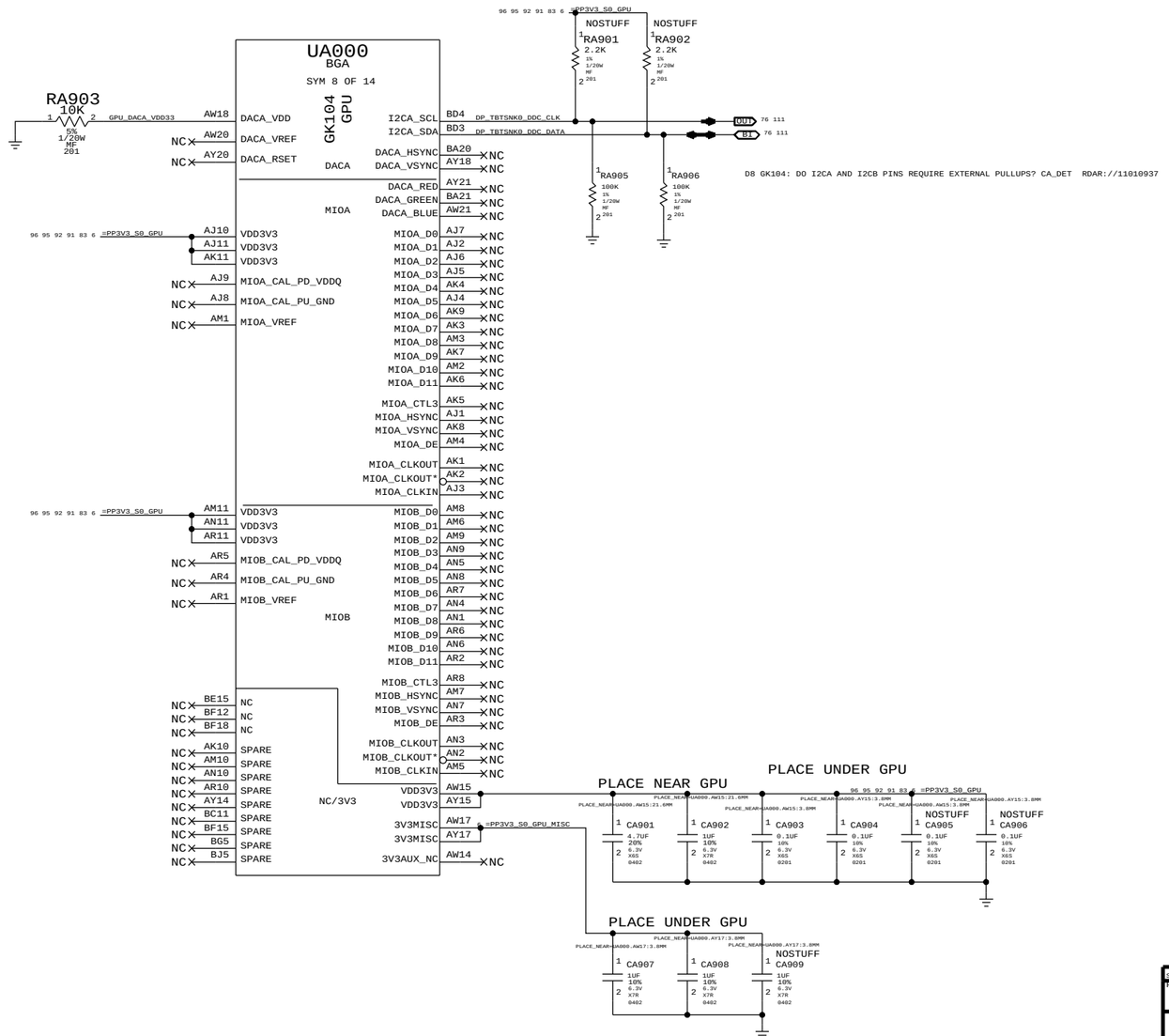

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2013

PAGE TITLE

KEPLER MISC

Apple Inc.

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GPU NVVDD DECOUPLING I(EDP)=95A

Page Notes

Power aliases required by this page:

- =PPVCORE_S0_GPU

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

93 51 6 =PPVCORE_S0_GPU

UA000 BGA SYM 10 OF 14 VDD 1/2 GK104-GPU-A2

BA39	VDD	VDD	BH48
BA42	VDD	VDD	BH49
BA43	VDD	VDD	BJ39
BA44	VDD	VDD	BJ41
BA45	VDD	VDD	BJ42
BA46	VDD	VDD	BJ44
BB37	VDD	VDD	BJ45
BB38	VDD	VDD	BJ46
BB39	VDD	VDD	BJ47
BB40	VDD	VDD	BJ48
BB41	VDD	VDD	P15
BB42	VDD	VDD	P17
BB43	VDD	VDD	P19
BB44	VDD	VDD	P21
BB45	VDD	VDD	P23
BB46	VDD	VDD	P25
BB47	VDD	VDD	P27
BC38	VDD	VDD	P29
BC39	VDD	VDD	P31
BC41	VDD	VDD	R14
BC42	VDD	VDD	R16
BC45	VDD	VDD	R18
BC46	VDD	VDD	R20
BD38	VDD	VDD	R22
BD39	VDD	VDD	R24
BD41	VDD	VDD	R26
BD42	VDD	VDD	R28
BD44	VDD	VDD	R30
BD45	VDD	VDD	R32
BD46	VDD	VDD	T15
BD47	VDD	VDD	T17
BD48	VDD	VDD	T19
BD49	VDD	VDD	T21
BE38	VDD	VDD	T23
BE39	VDD	VDD	T25
BE40	VDD	VDD	T27
BE41	VDD	VDD	T29
BE42	VDD	VDD	T31
BE43	VDD	VDD	U14
BE44	VDD	VDD	U16
BE45	VDD	VDD	U18
BE46	VDD	VDD	U20
BE47	VDD	VDD	U22
BE48	VDD	VDD	U24
BE49	VDD	VDD	U26
BF38	VDD	VDD	U28
BF39	VDD	VDD	U30
BF40	VDD	VDD	U32
BF41	VDD	VDD	V15
BF42	VDD	VDD	V17
BF43	VDD	VDD	V19
BF44	VDD	VDD	V21
BF45	VDD	VDD	V23
BF46	VDD	VDD	V25
BF47	VDD	VDD	V27
BF48	VDD	VDD	V29
BF49	VDD	VDD	V31
BG39	VDD	VDD	W14
BG41	VDD	VDD	W16
BG42	VDD	VDD	W18
BG44	VDD	VDD	W20
BG45	VDD	VDD	W22
BG46	VDD	VDD	W24
BG47	VDD	VDD	W26
BG48	VDD	VDD	W28
BG49	VDD	VDD	W30
BH39	VDD	VDD	W32
BH40	VDD	VDD	Y15
BH41	VDD	VDD	Y17
BH42	VDD	VDD	Y19
BH43	VDD	VDD	Y21
BH44	VDD	VDD	Y23
BH45	VDD	VDD	Y25
BH46	VDD	VDD	Y27
BH47	VDD	VDD	Y29

UA000 BGA SYM 9 OF 14 VDD 1/2 GK104-GPU-A2

AA14	VDD	VDD	AH31
AA16	VDD	VDD	AJ14
AA18	VDD	VDD	AJ16
AA20	VDD	VDD	AJ18
AA22	VDD	VDD	AJ20
AA24	VDD	VDD	AJ22
AA26	VDD	VDD	AJ24
AA28	VDD	VDD	AJ26
AA30	VDD	VDD	AJ28
AA32	VDD	VDD	AJ30
AB15	VDD	VDD	AJ32
AB17	VDD	VDD	AK15
AB19	VDD	VDD	AK17
AB21	VDD	VDD	AK19
AB23	VDD	VDD	AK21
AB25	VDD	VDD	AK23
AB27	VDD	VDD	AK25
AB29	VDD	VDD	AK27
AB31	VDD	VDD	AK29
AC14	VDD	VDD	AK31
AC16	VDD	VDD	AL14
AC18	VDD	VDD	AL16
AC20	VDD	VDD	AL18
AC22	VDD	VDD	AL20
AC24	VDD	VDD	AL22
AC26	VDD	VDD	AL24
AC28	VDD	VDD	AL26
AC30	VDD	VDD	AL28
AC32	VDD	VDD	AL30
AD15	VDD	VDD	AL32
AD17	VDD	VDD	AM15
AD19	VDD	VDD	AM17
AD21	VDD	VDD	AM19
AD23	VDD	VDD	AM21
AD25	VDD	VDD	AM23
AD27	VDD	VDD	AM25
AD29	VDD	VDD	AM27
AD31	VDD	VDD	AM29
AE14	VDD	VDD	AM31
AE16	VDD	VDD	AM32
AE18	VDD	VDD	AN39
AE20	VDD	VDD	AP39
AE22	VDD	VDD	AR39
AE24	VDD	VDD	AR40
AE26	VDD	VDD	AR41
AE28	VDD	VDD	AT39
AE30	VDD	VDD	AT40
AE32	VDD	VDD	AT41
AF15	VDD	VDD	AU39
AF17	VDD	VDD	AU41
AF19	VDD	VDD	AU42
AF21	VDD	VDD	AV41
AF23	VDD	VDD	AV42
AF25	VDD	VDD	AV43
AF27	VDD	VDD	AV44
AF29	VDD	VDD	AW35
AF31	VDD	VDD	AW36
AG14	VDD	VDD	AW37
AG16	VDD	VDD	AW41
AG18	VDD	VDD	AW42
AG20	VDD	VDD	AW43
AG22	VDD	VDD	AW44
AG24	VDD	VDD	AW45
AG26	VDD	VDD	AY36
AG28	VDD	VDD	AY42
AG30	VDD	VDD	AY45
AG32	VDD	VDD	BA36
AH15	VDD	VDD	BA37
AH17	VDD	VDD	BA38
AH19	VDD	VDD	Y31
AH21	VDD		
AH23	VDD		
AH25	VDD		
AH27	VDD		
AH29	VDD		

VDD_SENSE AY23
GND_SENSE AW23

=PPVCORE_S0_GPU 6 51 93

NOSTUFF
RB101 100 5% 1/20W MF 201

NOSTUFF
RB102 100 5% 1/20W MF 201

MIN_LINE_WIDTH=0.41 MM
MIN_NECK_WIDTH=0.10 MM
VOLTAGE=1.0V
VSNS_GPU_VDD → 96 115

MIN_LINE_WIDTH=0.41MM
MIN_NECK_WIDTH=0.10 MM
VOLTAGE=0V
VSNS_GPU_VSS → 96 115

PLACE UNDER GPU

CB101 4.7UF 20% 6.3V X6S 0402
CB102 4.7UF 20% 6.3V X6S 0402
CB103 4.7UF 20% 6.3V X6S 0402
CB104 4.7UF 20% 6.3V X6S 0402
CB105 4.7UF 20% 6.3V X6S 0402
CB106 4.7UF 20% 6.3V X6S 0402
CB107 4.7UF 20% 6.3V X6S 0402
CB108 4.7UF 20% 6.3V X6S 0402
CB109 4.7UF 20% 6.3V X6S 0402
CB110 4.7UF 20% 6.3V X6S 0402
CB111 4.7UF 20% 6.3V X6S 0402
CB112 4.7UF 20% 6.3V X6S 0402
CB113 4.7UF 20% 6.3V X6S 0402
CB114 4.7UF 20% 6.3V X6S 0402
CB115 4.7UF 20% 6.3V X6S 0402
CB116 4.7UF 20% 6.3V X6S 0402
CB117 4.7UF 20% 6.3V X6S 0402
CB118 4.7UF 20% 6.3V X6S 0402
CB119 4.7UF 20% 6.3V X6S 0402
CB120 4.7UF 20% 6.3V X6S 0402

PLACE UNDER GPU

CB121 4.7UF 20% 6.3V X6S 0402
CB122 4.7UF 20% 6.3V X6S 0402
CB123 4.7UF 20% 6.3V X6S 0402
CB124 4.7UF 20% 6.3V X6S 0402
CB125 4.7UF 20% 6.3V X6S 0402
CB126 4.7UF 20% 6.3V X6S 0402
CB127 4.7UF 20% 6.3V X6S 0402
CB128 4.7UF 20% 6.3V X6S 0402
CB129 4.7UF 20% 6.3V X6S 0402
CB130 4.7UF 20% 6.3V X6S 0402
CB131 4.7UF 20% 6.3V X6S 0402
CB132 4.7UF 20% 6.3V X6S 0402
CB133 4.7UF 20% 6.3V X6S 0402
CB134 4.7UF 20% 6.3V X6S 0402
CB135 4.7UF 20% 6.3V X6S 0402
CB136 4.7UF 20% 6.3V X6S 0402
CB137 4.7UF 20% 6.3V X6S 0402
CB138 4.7UF 20% 6.3V X6S 0402
CB139 4.7UF 20% 6.3V X6S 0402
CB140 4.7UF 20% 6.3V X6S 0402

PLACE UNDER GPU

CB141 1.0UF 20% 4V X6S 0201
CB142 1.0UF 20% 4V X6S 0201
CB143 1.0UF 20% 4V X6S 0201
CB144 1.0UF 20% 4V X6S 0201
CB145 1.0UF 20% 4V X6S 0201
CB146 1.0UF 20% 4V X6S 0201
CB147 1.0UF 20% 4V X6S 0201
CB148 1.0UF 20% 4V X6S 0201
CB149 1.0UF 20% 4V X6S 0201
CB150 1.0UF 20% 4V X6S 0201
CB151 1.0UF 20% 4V X6S 0201
CB152 1.0UF 20% 4V X6S 0201
CB153 1.0UF 20% 4V X6S 0201
CB154 1.0UF 20% 4V X6S 0201
CB155 1.0UF 20% 4V X6S 0201
CB156 1.0UF 20% 4V X6S 0201
CB157 1.0UF 20% 4V X6S 0201
CB158 1.0UF 20% 4V X6S 0201
CB159 1.0UF 20% 4V X6S 0201
CB160 1.0UF 20% 4V X6S 0201

PLACE UNDER GPU

CB161 10UF 20% 4V X6S 0402
CB162 10UF 20% 4V X6S 0402
CB163 10UF 20% 4V X6S 0402
CB164 10UF 20% 4V X6S 0402
CB171 22UF 20% 4V X6S-CERM 0603
CB172 22UF 20% 4V X6S-CERM 0603
CB173 22UF 20% 4V X6S-CERM 0603
CB174 22UF 20% 4V X6S-CERM 0603
CB175 22UF 20% 4V X6S-CERM 0603
CB176 22UF 20% 4V X6S-CERM 0603
CB177 22UF 20% 4V X6S-CERM 0603
CB178 22UF 20% 4V X6S-CERM 0603
CB179 22UF 20% 4V X6S-CERM 0603
CB180 22UF 20% 4V X6S-CERM 0603
CB181 22UF 20% 4V X6S-CERM 0603
CB191 47UF 20% 4V X6S 0805
CB192 47UF 20% 4V X6S 0805
CB193 47UF 20% 4V X6S 0805
CB194 47UF 20% 4V X6S 0805

PLACE NEAR GPU W/ 35MM FROM GPU CENTER

PLACE_NEAR=UA000.AT40:35MM
CRITICAL
CB165 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=UA000.AT40:35MM
CRITICAL
CB166 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=UA000.AT40:42MM
CRITICAL
CB167 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=UA000.AT40:38MM
CRITICAL
CB168 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2012

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GPU FBVDD/Q DECOUPLING I(EDP PEAK)=26A

Page Notes

Power aliases required by this page:

- +PP1V35_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

PLACE UNDER GPU

CB201 0.1UF 10% 6.3V X6S 0201
CB202 0.1UF 10% 6.3V X6S 0201
CB203 0.1UF 10% 6.3V X6S 0201
CB204 0.1UF 10% 6.3V X6S 0201
CB205 0.1UF 10% 6.3V X6S 0201
CB206 0.1UF 10% 6.3V X6S 0201
CB207 0.1UF 10% 6.3V X6S 0201
CB208 0.1UF 10% 6.3V X6S 0201

PLACE UNDER GPU

CB211 1UF 10% 6.3V X7R 0402
CB212 1UF 10% 6.3V X7R 0402
CB213 1UF 10% 6.3V X7R 0402
CB214 1UF 10% 6.3V X7R 0402
CB215 1UF 10% 6.3V X7R 0402
CB216 1UF 10% 6.3V X7R 0402
CB217 1UF 10% 6.3V X7R 0402
CB218 1UF 10% 6.3V X7R 0402

PLACE UNDER GPU

CB221 4.7UF 20% 6.3V X6S 0402
CB222 4.7UF 20% 6.3V X6S 0402
CB223 4.7UF 20% 6.3V X6S 0402
CB224 4.7UF 20% 6.3V X6S 0402
CB225 4.7UF 20% 6.3V X6S 0402
CB226 4.7UF 20% 6.3V X6S 0402
CB227 4.7UF 20% 6.3V X6S 0402
CB228 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB229 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB230 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB231 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB232 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB233 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB234 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB235 4.7UF 20% 6.3V X6S 0402
NOSTUFF CB236 4.7UF 20% 6.3V X6S 0402

PLACE UNDER GPU

CB240 22UF 20% 4V X6S-CERM 0603
CB241 22UF 20% 4V X6S-CERM 0603
CB242 22UF 20% 4V X6S-CERM 0603
CB243 22UF 20% 4V X6S-CERM 0603
NOSTUFF CB244 22UF 20% 4V X6S-CERM 0603
NOSTUFF CB245 22UF 20% 4V X6S-CERM 0603
CB246 10UF 20% 4V X6S 0402
CB247 10UF 20% 4V X6S 0402
CB248 10UF 20% 4V X6S 0402
CB249 10UF 20% 4V X6S 0402
NOSTUFF CB250 10UF 20% 4V X6S 0402
NOSTUFF CB251 10UF 20% 4V X6S 0402

94 89 88 87 86 85 84 6 +PP1V35_S0_GPU_FBVDDQ

UA000
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GK104 GPU

AA39	FBVDDQ	FBVDDQ	J43
AC11	FBVDDQ	FBVDDQ	K24
AD10	FBVDDQ	FBVDDQ	K26
AD39	FBVDDQ	FBVDDQ	K29
AF11	FBVDDQ	FBVDDQ	K30
AF39	FBVDDQ	FBVDDQ	K32
AG39	FBVDDQ	FBVDDQ	L14
AK39	FBVDDQ	FBVDDQ	L15
AM39	FBVDDQ	FBVDDQ	L17
AM40	FBVDDQ	FBVDDQ	L18
AN40	FBVDDQ	FBVDDQ	L20
B47	FBVDDQ	FBVDDQ	L23
C45	FBVDDQ	FBVDDQ	L24
C46	FBVDDQ	FBVDDQ	L27
C47	FBVDDQ	FBVDDQ	L29
D44	FBVDDQ	FBVDDQ	L30
D45	FBVDDQ	FBVDDQ	L32
D46	FBVDDQ	FBVDDQ	L33
E44	FBVDDQ	FBVDDQ	L35
E45	FBVDDQ	FBVDDQ	L41
F42	FBVDDQ	FBVDDQ	P11
F44	FBVDDQ	FBVDDQ	P39
F45	FBVDDQ	FBVDDQ	R11
G41	FBVDDQ	FBVDDQ	R40
G42	FBVDDQ	FBVDDQ	U11
H41	FBVDDQ	FBVDDQ	U39
H42	FBVDDQ	FBVDDQ	V11
H43	FBVDDQ	FBVDDQ	V39
J38	FBVDDQ	FBVDDQ	V40
J39	FBVDDQ	FBVDDQ	Y11
J42	FBVDDQ	FBVDDQ	Y40

FBVDDQ_SENSE	R49 115	FBVDDQ_SENSE_R
FB_CLAMP	BB48	FB_CLAMP
FB_VREF	R39 118	FB_VREF_GPU
PROBE_FBVDDQ	AG11	FB_PROBE_VDDQ
PROBE_FB_GND	AF10	FB_PROBE_GND
FB_CAL_PD_VDDQ	P40 112	FB_CAL_PD_VDDQ
FB_CAL_PU_GND	R48 112	FB_CAL_PU_GND
FB_CALTERM_GND	R47 112	FB_CAL_TERM_GND

94 89 88 87 86 85 84 6 +PP1V35_S0_GPU_FBVDDQ

NOSTUFF RB202 40.2 1% 1/20W MF 201
NOSTUFF RB201 60.4 1% 1/20W MF 201
NOSTUFF RB208 1.33K 1% 1/20W MF 201
RB203 0 5% 1/20W MF 201
XWB201 SM SIGNAL_MODEL=EMPTY VSNS_FBVDDQ VSNS_FBVDDQ_P
XWB200 SM SIGNAL_MODEL=EMPTY VSNS_FBVDDQ_N
RB204 60.4 1% 1/20W MF 201
RB205 40.2 1% 1/20W MF 201
NOSTUFF RB206 60.4 1% 1/20W MF 201
RB207 10K 5% 1/20W MF 201
NOSTUFF RB209 1.33K 1% 1/20W MF 201
NOSTUFF CB252 0.1UF 10% 16V X7R-CERM 402

SYNC_MASTER=D8_YAN SYNC_DATE=04/09/2013

PAGE TITLE: KEPLER FBVDD/Q POWER

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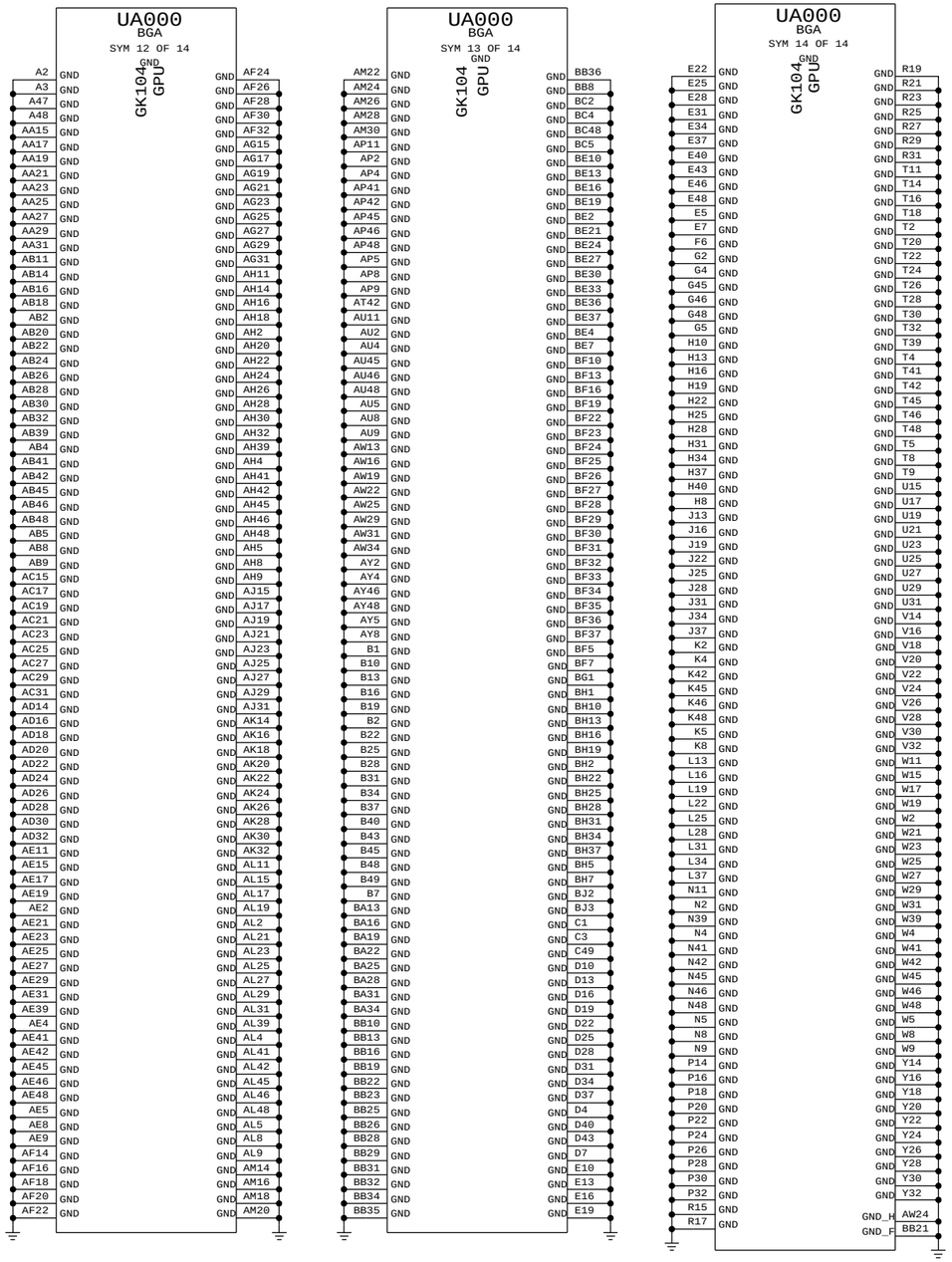
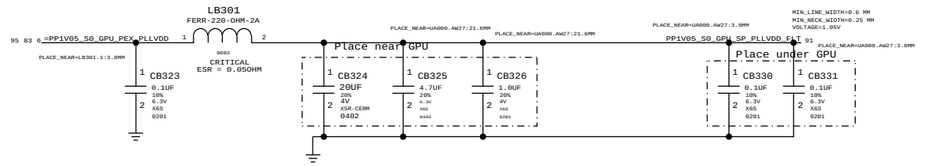
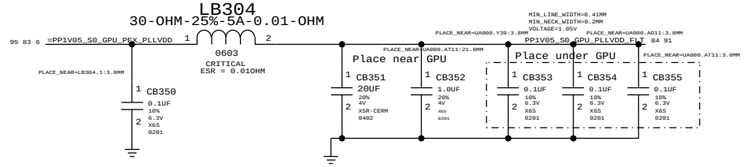


GPU SP_PLLVDD/VID_PLLVDD 47MA+41MA

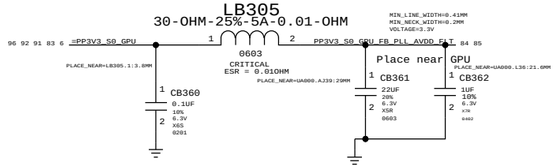


RDAR://11427653 D8: REPLACE 138S0682 WITH 138S0802

GPU GPC_PLLAVDD/LXS_PLLVDD/FB_DLL_AVDD 52MA+39MA+50MA



GPU GPU_FB_PLL_AVDD 120MA X 4 = 480MA



Page Notes

Power aliases required by this page:

- =PP3V3_GPU_VDD33
- =PP1V05_GPU_PEX_IOVDD
- =PP1V05_GPU_PEX_PLLVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

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PAGE TITLE	KEPLER PEX PWR/GNDS
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GPU CORE REG 1.1V/???A O/P= PPGPUCORE_S0_REG

GPU VCORE
VOUT = VCORE
PEAK = ???A
AVG = ???A

=PP5V_S0_VRD
RB418 2.2 5% 1/8W MF-LF 805
MAX_NECK_LENGTH=3MM MIN_NECK_WIDTH=0.3MM MIN_LINE_WIDTH=0.6MM VOLTAGE=5V

PP5V_S0_GPU_VCORE_VCC
NOSTUFF RB447 0 5% 1/10W MF-LF 402
NOSTUFF RB448 0 5% 1/10W MF-LF 402
NOSTUFF RB444 0 5% 1/10W MF-LF 402
NOSTUFF RB455 0 5% 1/16W MF-LF 402

VR_GPU_PWM1_R
VR_GPU_PWM2_R
VR_GPU_PWM3_R
VR_GPU_PWM4_R

VSNS_GPU_VDD
SM XWB420 OMIT
VOLTAGE=1.1V NET_PHYSICAL_TYPE=SNS_DIFF_PHY
VR_GPU_VSEN
SIGNAL_MODEL=EMPTY
1.25 mOhm loadline
VSNS_GPU_SSS
XWB430 SM OMIT
VOLTAGE=0V NET_PHYSICAL_TYPE=SNS_DIFF_PHY
VR_GPU_RGND

NOSTUFF CB401 0.0022UF 10% 50V CERM 402
CB402 0.0022UF 10% 50V CERM 402
CB403 0.0022UF 10% 50V CERM 402
AGND_GPU

CB404 47PF 5% 50V CERM 402
VR_GPU_FB_R
VR_GPU_COMP_R
RB401 8.06K 1% 1/16W MF-LF 402
VR_GPU_COMP_RC
CB405 0.0047UF 10% 25V CERM 402
RB479 0 5% 1/10W MF-LF 402
LOCAL 5V
RB402 1K 1% 1/16W MF-LF 402
VR_VDF_R1
RB403 287 1% 1/16W MF-LF 402
NOSTUFF RB446 1M 5% 1/16W MF-LF 402
RB404 0 5% 1/16W MF-LF 402
CB407 1UF 10% 10V X6S-CERM 0402
AGND_GPU
CB406 0.001UF 10% 50V X7R-CERM 0402
VR_VDF_R2
RB449 47.5 1% 1/16W MF-LF 402

PP5V_S0_GPU_VCORE_VCC
VR_HOT goes HIGH when VTM/VCC < 28% and LOW when VTM/VCC > 33%.
RB400 1.02K 1% 1/16W MF-LF 402
NOSTUFF RB405 20.0K 1% 1/16W MF-LF 402
NOSTUFF RB498 0 5% 1/16W MF-LF 402
RB477 100K 1% 1/16W MF-LF 402

LAYOUT: PLACE RTB401 NEAR HOT SPOT
RTB401 6.8K 0603
CB480 0.1UF 10% 16V CERM 402
NOSTUFF RB406 0 5% 1/16W MF-LF 402
NOSTUFF RB407 21K 1% 1/16W MF-LF 402
NOSTUFF RB408 75K 1% 1/16W MF-LF 402
NOSTUFF RB409 100K 1% 1/16W MF-LF 402
AGND_GPU
CB410 0.0033UF 10% 50V X7R-CERM 0402
RB410 2.15K 1% 1/16W MF-LF 402

=PP5V_S0_VRD
RB411 10K 0.1% 1/16W MF-LF 0402
PP5V_S0_GPU_VCORE_VCC
=PP3V3_S0_VRD
=PP3V3_S0_GPU
RB412 2.0K 1% 1/16W MF-LF 402
RB499 10K 0.1% 1/16W MF-LF 0402
PM_PGOOD_REG_GPUCORE_S0
GPU_PSI_L
VR_GPU_IMON

RB414 49.9K 1% 1/16W MF-LF 402
RB415 49.9K 1% 1/16W MF-LF 402

RB445 0 5% 1/16W MF-LF 402
RB417 10K 1% 1/16W MF-LF 402
CB412 0.022UF 10% 16V X5R-X7R-CERM 0402
RB416 0 5% 1/16W MF-LF 402
VR_GPU_IOUT_PD

DEFAULT: 0.9000V STEP: 12.5MV

=PP3V3_S0_GPU
NOSTUFF RB478 1K 1% 1/16W MF-LF 402
RB470 1K 1% 1/16W MF-LF 402
RB471 1K 1% 1/16W MF-LF 402
RB472 1K 1% 1/16W MF-LF 402
RB473 1K 1% 1/16W MF-LF 402
RB474 1K 1% 1/16W MF-LF 402
RB475 1K 1% 1/16W MF-LF 402
NOSTUFF RB476 1K 1% 1/16W MF-LF 402

REG_GPUCORE_VID7
REG_GPUCORE_VID6
REG_GPUCORE_VID5
REG_GPUCORE_VID4
REG_GPUCORE_VID3
REG_GPUCORE_VID2
REG_GPUCORE_VID1
REG_GPUCORE_VID0

NOSTUFF RB495 1K 1% 1/16W MF-LF 402
RB496 1K 1% 1/16W MF-LF 402
RB497 1K 1% 1/16W MF-LF 402
NOSTUFF RB480 1K 1% 1/16W MF-LF 402
RB481 1K 1% 1/16W MF-LF 402
RB482 1K 1% 1/16W MF-LF 402
RB485 1K 1% 1/16W MF-LF 402
RB483 1K 1% 1/16W MF-LF 402

VR_GPU_TCOMP
VR_GPU_OFS
VR_GPU_FS
VR_GPU_SS
VR_GPU_DAC
VR_GPU_REF
VR_GPU_TM
VR_GPU_EN_VTT
VR_GPU_IMON_R
VR_GPU_FAN
VR_GPU_VRDHOT

UB400 ISL6334D QFN
VCC CRITICAL SYM_VER_2
COMP 13
FB 14
VDIFF 15
VSEN 17
RGND 16
TCOMP 18
OFS 9
FS 34
SS 35
DAC 11
REF 12
TM 39
EN_VTT 33
VR_RDY 36
VID0 7
VID1 6
VID2 5
VID3 4
VID4 3
VID5 2
VID6 1
VID7 40
PSI* 8
IMON 10
H_CPURST_N 37
VR_HOT 38
PWM1 26
ISEN1+ 28
ISEN1- 27
PWM2 20
ISEN2+ 22
ISEN2- 21
PWM3 31
ISEN3+ 29
ISEN3- 30
PWM4 25
ISEN4+ 23
ISEN4- 24
EN_PWR 32
THRM PAD 41

VR_GPU_ISNS1_R_P
VR_GPU_ISNS1_R_N
VR_GPU_ISNS2_R_P
VR_GPU_ISNS2_R_N
VR_GPU_ISNS3_R_P
VR_GPU_ISNS3_R_N
VR_GPU_ISNS4_R_P
VR_GPU_ISNS4_R_N

RB434 0 5% 1/10W MF-LF 402
REG_PWM_GPUCORE_1
RB431 178 1% 1/10W MF-LF 402
VR_GPU_ISNS1_RR_2
RB432 0 5% 1/16W MF-LF 402
NOSTUFF CB430 15PF 1% 50V C0G 402
CB431 150PF 5% 50V CERM 402
CB432 0.1UF 10% 16V X7R-CERM 0402
CB433 220PF 5% 25V C0G-CERM 0402
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_1
REG_ISEN_GCORE_1_P
REG_ISEN_GCORE_1_N
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_1
RB433 1.02K 1% 1/16W MF-LF 402

RB440 0 5% 1/10W MF-LF 402
REG_PWM_GPUCORE_2
RB441 178 1% 1/10W MF-LF 402
VR_GPU_ISNS2_RR_2
RB442 0 5% 1/16W MF-LF 402
NOSTUFF CB440 15PF 1% 50V C0G 402
CB441 150PF 5% 50V CERM 402
CB442 0.1UF 10% 16V X7R-CERM 0402
CB443 220PF 5% 25V C0G-CERM 0402
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_2
REG_ISEN_GCORE_2_P
REG_ISEN_GCORE_2_N
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_2
RB443 1.02K 1% 1/16W MF-LF 402

RB450 0 5% 1/10W MF-LF 402
REG_PWM_GPUCORE_3
RB451 178 1% 1/10W MF-LF 402
VR_GPU_ISNS3_RR_2
RB452 0 5% 1/16W MF-LF 402
NOSTUFF CB450 15PF 1% 50V C0G 402
CB451 150PF 5% 50V CERM 402
CB452 0.1UF 10% 16V X7R-CERM 0402
CB453 220PF 5% 25V C0G-CERM 0402
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_3
REG_ISEN_GCORE_3_P
REG_ISEN_GCORE_3_N
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_3
RB453 1.02K 1% 1/16W MF-LF 402

RB438 0 5% 1/10W MF-LF 402
REG_PWM_GPUCORE_4
RB439 178 1% 1/10W MF-LF 402
VR_GPU_ISNS4_RR_2
RB420 0 5% 1/16W MF-LF 402
NOSTUFF CB460 15PF 1% 50V C0G 402
CB461 150PF 5% 50V CERM 402
CB462 0.1UF 10% 16V X7R-CERM 0402
CB463 220PF 5% 25V C0G-CERM 0402
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_4
REG_ISEN_GCORE_4_P
REG_ISEN_GCORE_4_N
DIFFERENTIAL_PAIR=REG_ISEN_GCORE_4
RB421 1.02K 1% 1/16W MF-LF 402

OMIT XWB401 SM
AGND_GPU
MAX_NECK_LENGTH=9MM MIN_NECK_WIDTH=0.3MM MIN_LINE_WIDTH=0.6MM VOLTAGE=0V

RB484 0 5% 1/16W MF-LF 402
PM_EN_REG_GPUCORE_S0
NOSTUFF CB409 0.01UF 10% 16V X7R-CERM 0402
AGND_GPU

NEED TO FIGURE OUT SEQUENCING FOR ENABLE

=PP12V_S0_REG_GPUCORE
IMAX = 10.5A
CRITICAL LB400 0.36UH-30A-0.6MOHM SDP110808MR36MF-TH
PP12V_S0_GPUCORE_FLT
152-0110

GPU CORE INPUT Filtering

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012
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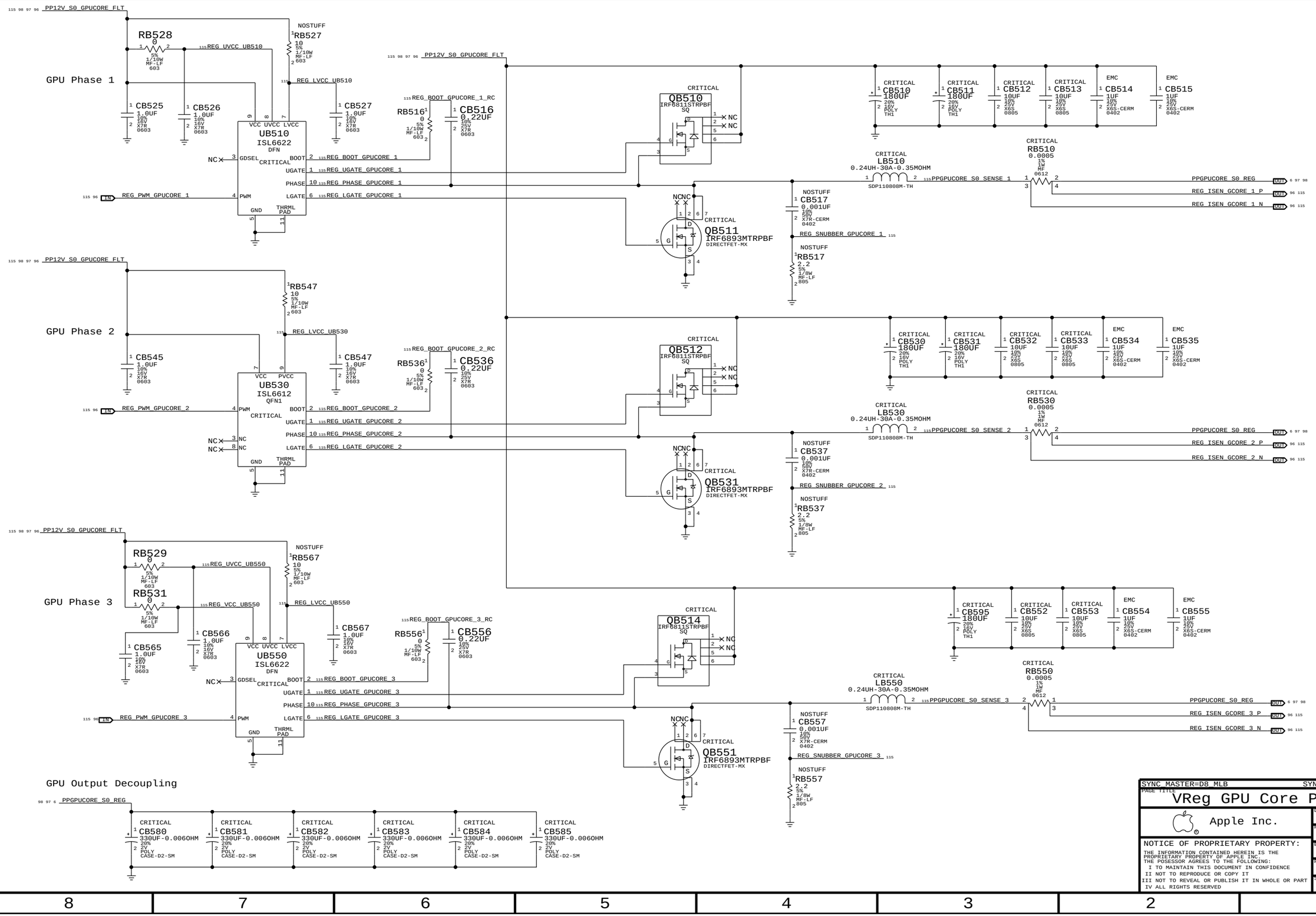
GPU Phase 1
GPU Phase 2
GPU Phase 3
GPU Output Decoupling
PP12V_S0_GPUCORE_FLT
REG_UVCC_UB510
REG_LVCC_UB510
REG_BOOT_GPUCORE_1_RC
REG_BOOT_GPUCORE_1
REG_UGATE_GPUCORE_1
REG_PHASE_GPUCORE_1
REG_LGATE_GPUCORE_1
REG_PWM_GPUCORE_1
UB510
ISL6622
DFN
QB510
QB511
IRF6811STRPBF
IRF6893MTRPBF
LB510
0.24UH-30A-0.35MOHM
SDP110808M-TH
PPGPUCORE_S0_SENSE_1
RB510
0.0005
PPGPUCORE_S0_REG
REG_ISEN_GCORE_1_P
REG_ISEN_GCORE_1_N
REG_SNUBBER_GPUCORE_1
REG_LVCC_UB530
REG_BOOT_GPUCORE_2_RC
REG_BOOT_GPUCORE_2
REG_UGATE_GPUCORE_2
REG_PHASE_GPUCORE_2
REG_LGATE_GPUCORE_2
REG_PWM_GPUCORE_2
UB530
ISL6612
QFN1
QB512
QB531
LB530
PPGPUCORE_S0_SENSE_2
RB530
REG_ISEN_GCORE_2_P
REG_ISEN_GCORE_2_N
REG_SNUBBER_GPUCORE_2
REG_VCC_UB550
REG_LVCC_UB550
REG_BOOT_GPUCORE_3_RC
REG_BOOT_GPUCORE_3
REG_UGATE_GPUCORE_3
REG_PHASE_GPUCORE_3
REG_LGATE_GPUCORE_3
REG_PWM_GPUCORE_3
UB550
QB514
QB551
LB550
PPGPUCORE_S0_SENSE_3
RB550
REG_ISEN_GCORE_3_P
REG_ISEN_GCORE_3_N
REG_SNUBBER_GPUCORE_3
PPGPUCORE_S0_REG
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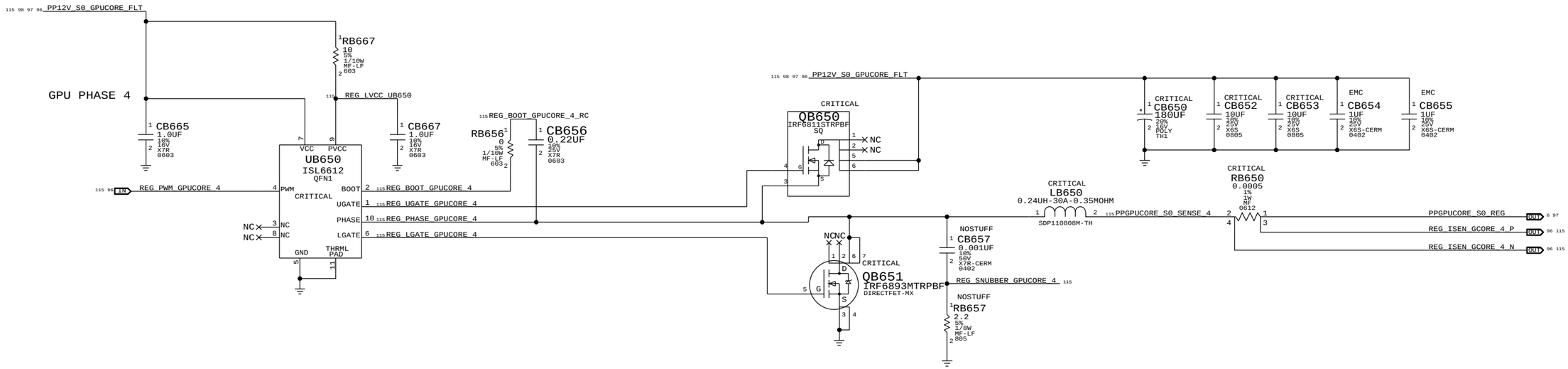

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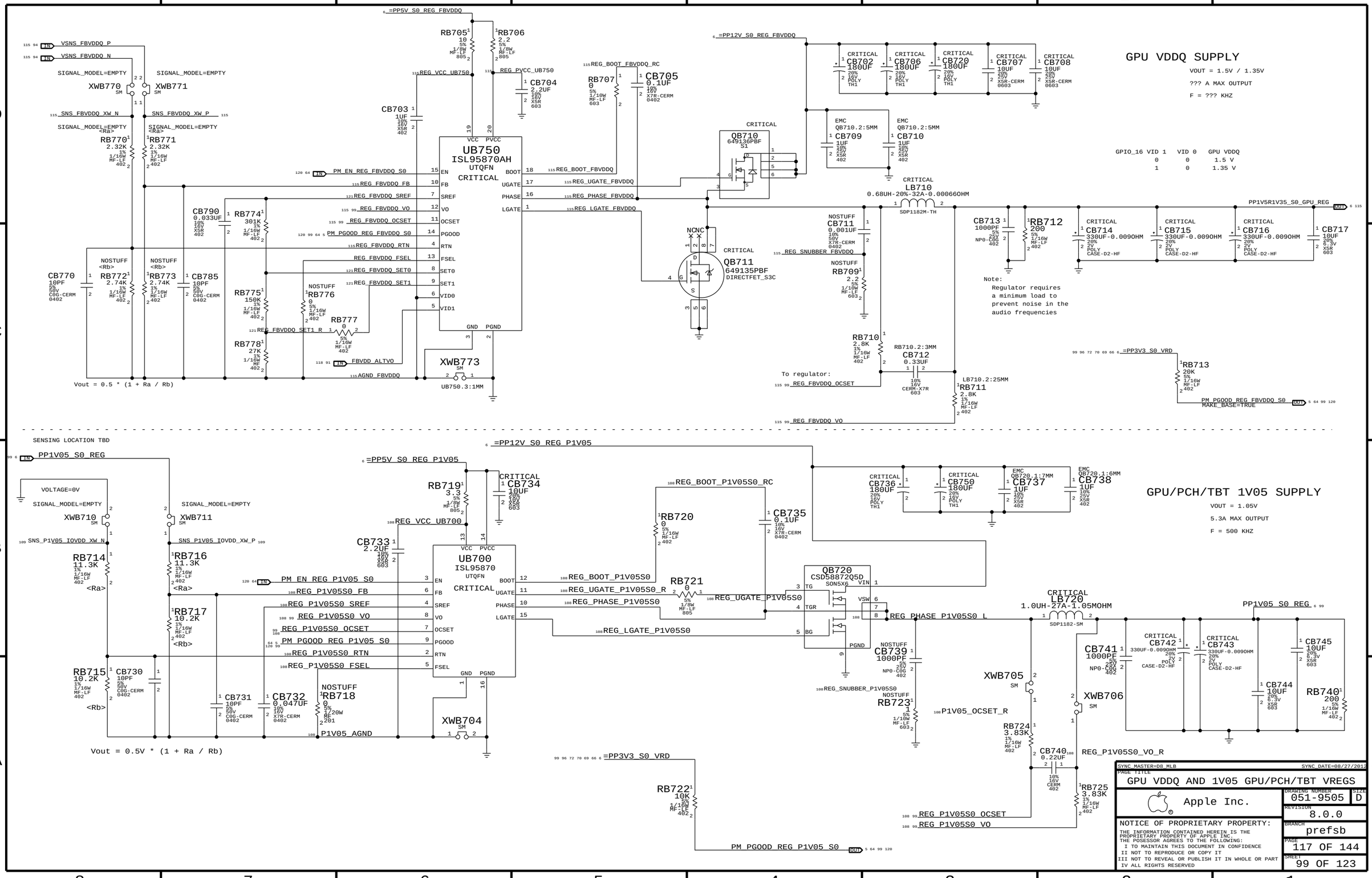
GPU VDDQ SUPPLY
VOUT = 1.5V / 1.35V
??? A MAX OUTPUT
F = ??? KHZ
GPIO_16 VID 1 VID 0 GPU VDDQ
0 0 1.5 V
1 0 1.35 V
UB750
ISL95870AH
UTQFN
CRITICAL
QB710
649136PBF
QB711
649135PBF
DIRECTFET_S3C
LB710
0.68UH-20%-32A-0.000660HM
SDP1182M-TH
Note:
Regulator requires
a minimum load to
prevent noise in the
audio frequencies
To regulator:
Vout = 0.5 * (1 + Ra / Rb)
SENSING LOCATION TBD
GPU/PCH/TBT 1V05 SUPPLY
VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ
UB700
ISL95870
UTQFN
CRITICAL
QB720
CSD58872Q5D
LB720
1.0UH-27A-1.05MOHM
SDP1182-SM
Vout = 0.5V * (1 + Ra / Rb)
GPU VDDQ AND 1V05 GPU/PCH/TBT VREGS
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D8 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OF MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

Compensation Physical Rule Definition

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
COMP_SE	*	Y	0.305 MM	0.105 MM	3 MM	=STANDARD	=STANDARD

NOTE: line width based on 12 mil recommendation
NOTE: neck width based on 4 mil recommendation

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

Top	Signal	0.5 oz (Cu plated)	
	Prepreg	0.071 MM	
2	Plane	1 oz	
	Core	0.101 MM	
3	Signal	0.5 oz	
	Prepreg	0.115 MM	
4	Plane	1 oz	
	Core	0.076 MM	
5	Signal	0.5 oz	
	Prepreg	0.380 MM	
6	Plane	1 oz	
	Core	0.076 MM	
7	Plane	1 oz	
	Prepreg	0.380 MM	
8	Signal	0.5 oz	
	Core	0.076 MM	
9	Plane	1 oz	
	Prepreg	0.115 MM	
10	Signal	0.5 oz	
	Core	0.101 MM	
11	Plane	1 oz	
	Prepreg	0.071 MM	
Btm	Signal	0.5 oz (Cu plated)	

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?
PM_ISO	*	=1:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	PM_ISO
PM	GND	*	DEFAULT

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012

PAGE TITLE: D8 RULE DEFINITIONS

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_34S	BOTTOM	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S	BOTTOM	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_42S	ISL5,ISL8	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_42S_D	BOTTOM	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	0.1016 MM	0.1016 MM
DDR_42S_D	ISL5,ISL8	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF

Minimum diff spacing is 4 mil
Table 3-5, Intel Doc# 473718

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR_PHY	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	TOP,BOTTOM	=5.5X_DIELECTRIC	?
DDR_CLK_ISO	ISL3,ISL10	=4.9X_DIELECTRIC	?
DDR_CLK_ISO	*	=6.5X_DIELECTRIC	?
DDR_CTRL_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_CTRL_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_CTRL_ISO	*	=5.3X_DIELECTRIC	?
DDR_CTRL2CTRL	TOP,BOTTOM	=3.0X_DIELECTRIC	?
DDR_CTRL2CTRL	ISL3,ISL10	=2.6X_DIELECTRIC	?
DDR_CTRL2CTRL	*	=3.5X_DIELECTRIC	?
DDR_CMD_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_CMD_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_CMD_ISO	*	=5.3X_DIELECTRIC	?
DDR_CMD2CMD	TOP,BOTTOM	=2.3X_DIELECTRIC	?
DDR_CMD2CMD	ISL3,ISL10	=2.0X_DIELECTRIC	?
DDR_CMD2CMD	*	=2.7X_DIELECTRIC	?
DDR_DATA_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_DATA_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_DATA_ISO	*	=5.3X_DIELECTRIC	?
DDR_DQ2DQ	TOP,BOTTOM	=3.2X_DIELECTRIC	900
DDR_DQ2DQ	ISL3,ISL10	=2.8X_DIELECTRIC	900
DDR_DQ2DQ	*	=3.8X_DIELECTRIC	900
DDR_DQ2DQS	TOP,BOTTOM	=3.7X_DIELECTRIC	?
DDR_DQ2DQS	ISL3,ISL10	=3.3X_DIELECTRIC	?
DDR_DQ2DQS	*	=4.4X_DIELECTRIC	?
DDR_BL2BL	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_BL2BL	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_BL2BL	*	=5.3X_DIELECTRIC	?
DDR_CH2CH	TOP,BOTTOM	=9.1X_DIELECTRIC	?
DDR_CH2CH	ISL3,ISL10	=8.2X_DIELECTRIC	?
DDR_CH2CH	*	=10.9X_DIELECTRIC	?
CMD2DATA_ISO	TOP,BOTTOM	=7X_DIELECTRIC	?
CMD2DATA_ISO	ISL3,ISL10	=5X_DIELECTRIC	?
CMD2DATA_ISO	*	=5X_DIELECTRIC	?

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR_ISO	*	=4.3X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER_DDR	*	*	POWER_DDR_ISO

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD
DDR_CMD	DDR_A_DQ_BYTE*	*	CMD2DATA_ISO
DDR_CMD	DDR_A_DQS*	*	CMD2DATA_ISO
DDR_CMD	DDR_B_DQ_BYTE*	*	CMD2DATA_ISO
DDR_CMD	DDR_B_DQS*	*	CMD2DATA_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
A17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	12 29
A17 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	12 29
A25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	12 30
A25 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	12 30
A16 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	12 29
A18 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	12 29
A16 DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	12 29
A24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	12 30
A26 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	12 30
A24 DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	12 30
A16 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	12 29 30
A16 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	12 29 30
A16 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	12 29 30
A16 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	12 29 30
A16 DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	12 29 30
A18 DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 33
A18 DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 33
A19 DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 33
A19 DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 33
A19 DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 33
A19 DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 33
A19 DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 33
A19 DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 33
A19 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	12 33
A17 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	12 33
A19 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	12 33
A17 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	12 33
A26 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	12 33
A28 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	12 33
A28 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	12 33
A26 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	12 33
A24 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	12 33
A20 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	12 33
A20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	12 33
A20 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	12 33
A20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	12 33
A20 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	12 33
A21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	12 33
A21 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	12 33
Channel B				
A21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	12 31
A21 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	12 31
A25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	12 32
A25 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	12 32
A21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	12 31
A21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	12 31
A21 DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	12 31
A25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	12 32
A26 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	12 32
A25 DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	12 32
A21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	12 31 32
A21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	12 31 32
A21 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	12 31 32
A22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	12 31 32
A22 DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	12 31 32
A22 DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 33
A22 DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 33
A22 DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 33
A22 DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 33
A22 DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 33
A22 DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 33
A22 DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 33
A22 DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 33
A23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	12 33
A23 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	12 33
A23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	12 33
A23 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	12 33
A23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	12 33
A23 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	12 33
A23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	12 33
A23 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	12 33
A23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	12 33
A23 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	12 33
A24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	12 33
A24 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	12 33
A24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	12 33
A24 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	12 33
A24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	12 33
A24 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	12 33
Reset				
A24	DDR_50S	CPU	MEM_RESET_L	28 29 30 31 32

SYNC_MASTER=D8_MLB SYNC_DATE=08/27/2012
PAGE TITLE: DDR3 Constraints

Apple Inc.

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PCI EXPRESS

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	COMP_SE

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_ISO	*	=4X_DIELECTRIC	?
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO

PCIe Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	85	16	15.75	PCIe Gen2, PCIe Gen3, DMI

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing		
x1 AirPort				
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	NO_TEST=TRUE 35
PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	NO_TEST=TRUE 35
	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	NO_TEST=TRUE 18 35
	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	NO_TEST=TRUE 18 35
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	NO_TEST=TRUE 18 35
PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	NO_TEST=TRUE 18 35
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	18 35
PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	18 35
x1 Caesar IV				
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	NO_TEST=TRUE 39
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	NO_TEST=TRUE 39
	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	NO_TEST=TRUE 18 39
	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	NO_TEST=TRUE 18 39
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	NO_TEST=TRUE 18 39
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	NO_TEST=TRUE 18 39
	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	NO_TEST=TRUE 39
	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	NO_TEST=TRUE 39
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	18 39
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	18 39

PCIE (PCH - TBT)

Electrical Contraint Set	Physical	Spacing		
x4 Thunderbolt				
PCIE_GEN2_R2D_PINV	PCIE_PHY	PCIE	PCIE_TBT_R2D_P<2..0>	NO_TEST=TRUE 36
PCIE_GEN2_R2D_PINV	PCIE_PHY	PCIE	PCIE_TBT_R2D_N<2..0>	NO_TEST=TRUE 36
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_TBT_R2D_P<3>	NO_TEST=TRUE 36
PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_TBT_R2D_N<3>	NO_TEST=TRUE 36
	PCIE_PHY	PCIE	PCIE_TBT_R2D_C_P<3..0>	NO_TEST=TRUE 18 36
	PCIE_PHY	PCIE	PCIE_TBT_R2D_C_N<3..0>	NO_TEST=TRUE 18 36
	PCIE_PHY	PCIE	PCIE_TBT_D2R_P<3..0>	NO_TEST=TRUE 18 36
	PCIE_PHY	PCIE	PCIE_TBT_D2R_N<3..0>	NO_TEST=TRUE 18 36
PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<1..0>	NO_TEST=TRUE 36
PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<1..0>	NO_TEST=TRUE 36
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<2>	NO_TEST=TRUE 36
PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<2>	NO_TEST=TRUE 36
PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<3>	NO_TEST=TRUE 36
PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<3>	NO_TEST=TRUE 36
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	18 36
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	18 36

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<15>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<15>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<15>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<15>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<15>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<15>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<15>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<15>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<14>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<14>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<14>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<14>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<14>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<14>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<14>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<14>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<13>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<13>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<13>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<13>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<13>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<13>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<13>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<13>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<12>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<12>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<12>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<12>	NO_TEST=TRUE 83
PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<12>	NO_TEST=TRUE 83
PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<12>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<12>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<12>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<11>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<11>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<11>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<11>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<11>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<11>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<11>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<11>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<10>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<10>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<10>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<10>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<10>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<10>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<10>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<10>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<9>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<9>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<9>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<9>	NO_TEST=TRUE 83
PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<9>	NO_TEST=TRUE 83
PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<9>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<9>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<9>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<8>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<8>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<8>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<8>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<8>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<8>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<8>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<8>	NO_TEST=TRUE 10 83

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
x16 Graphics				
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<7>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<7>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<7>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<7>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<7>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<7>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<7>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<7>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<6>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<6>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<6>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<6>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<6>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<6>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<6>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<6>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<5>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<5>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<5>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<5>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<5>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<5>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<5>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<5>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<4>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<4>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<4>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<4>	NO_TEST=TRUE 83
PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<4>	NO_TEST=TRUE 83
PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<4>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<4>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<4>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<3>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<3>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<3>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<3>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<3>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<3>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<3>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<3>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<2>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<2>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<2>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<2>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<2>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<2>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<2>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<2>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<1>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<1>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<1>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<1>	NO_TEST=TRUE 83
PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<1>	NO_TEST=TRUE 83
PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<1>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<1>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<1>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<0>	NO_TEST=TRUE 10 83
PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<0>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_R2D_C_P<0>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_R2D_C_N<0>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<0>	NO_TEST=TRUE 83
PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<0>	NO_TEST=TRUE 83
	PCIE_PHY	PCIE	PEG_D2R_C_P<0>	NO_TEST=TRUE 10 83
	PCIE_PHY	PCIE	PEG_D2R_C_N<0>	NO_TEST=TRUE 10 83
CPU PCIe Clocks				
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P	NO_TEST=TRUE 10 83
PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N	NO_TEST=TRUE 10 83
CPU PCIe Compensation				
	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_COMP	10

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DMI

DMI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DMI_PHY	*	DMI_85D

CPU Misc / FDI

CPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI_SE	*	Y	0.3 MM	0.25 MM	3 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_PHY	*	CPU_50S
COMP_FDI_PHY	*	COMP_FDI_SE

CPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU	*	*	CPU_ISO
COMP_FDI	*	*	COMP_FDI_ISO

FDI Compensation Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_50S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
XDP_CLK_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	XDP_CLK_ISO
OBS_STROBE	*	*	XDP_CLK_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	50	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
U16 DMI_N2S	DMI_PHY	PCIE	DMI_N2S_P<3..0> NO_TEST=TRUE	10 19
U16 DMI_N2S	DMI_PHY	PCIE	DMI_N2S_N<3..0> NO_TEST=TRUE	10 19
U16 DMI_S2N	DMI_PHY	PCIE	DMI_S2N_P<3..0> NO_TEST=TRUE	10 19
U16 DMI_S2N	DMI_PHY	PCIE	DMI_S2N_N<3..0> NO_TEST=TRUE	10 19
U28 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
U28 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
DMI Compensation				
U17	COMP_PCIE_PHY	COMP_PCIE	PCH_DMI_COMP	19
U22	COMP_PCIE_PHY	COMP_PCIE	PCH_DMI2RBIAS	19

CPU Misc.

Electrical Contraint Set	Physical	Spacing		
CPU Misc.				
U24	CPU_PHY	CPU	CPU_SKTOCC_L	11 64
U24	CPU_PHY	CPU	CPU_PROC_SEL	11 19
U26	CPU_PHY	CPU	CPU_CATERR_L	11 48
U25	CPU_PHY	CPU	CPU_PECI	11 21 47 48
U25	CPU_PHY	CPU	CPU_PROCHOT_L	11 47 48 66
U26	CPU_PHY	CPU	CPU_PROCHOT_R_L	11
U24	CPU_PHY	CPU	CPU_THRMTRIP_L	11 48
U24	CPU_PHY	CPU	CPU_RESET_L	11 26
U24	CPU_PHY	CPU	PLT_RESET_LS1V05_L	11
U25	CPU_PHY	CPU	PM_SYNC	11 19
U25	CPU_PHY	CPU	CPU_PWRGD	11 21 25 28
U26	CPU_PHY	CPU	PM_MEM_PWRGD	11 19 28
U25	CPU_PHY	CPU	PM_MEM_PWRGD_R	11
U28	CPU_PHY	CPU	CPU_MEM_RESET_L	11 28

FDI

Electrical Contraint Set	Physical	Spacing		
FDI Compensation				
U26	COMP_FDI_PHY	COMP_FDI	CPU_FDI_COMPIO	10

XDP

Electrical Contraint Set	Physical	Spacing		
XDP MISC.				
U17 XDP_BPM_L	XDP_PHY	XDP	XDP_BPM_L<7..0>	11 25
U17	XDP_PHY	XDP	CPU_CFG<17..16>	10 25
U25	XDP_PHY	XDP	CPU_CFG<11..0>	10 15 25
U26	XDP_PHY	XDP	XDP_DBRESET_L	11 25
U26	XDP_PHY	XDP	XDP_CPU_PWRGD	25
U25	XDP_PHY	XDP	XDP_CPU_PWRBTN_L	25
U26	XDP_PHY	XDP	XDP_CPU_CFG<0>	25
U25	XDP_PHY	XDP	XDP_VR_READY	25
U27	XDP_PHY	XDP	XDP_CPU_PLTRST_L	25 26
U26	XDP_PHY	XDP	XDP_PCH_PWRGD	25
U26	XDP_PHY	XDP	XDP_PCH_PWRBTN_L	25
U27	XDP_PHY	XDP	XDP_PCH_PLTRST_L	25 26
U17	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	11 15
U17	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	11 15
U17 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	15 18 25
U18 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	15 18 25
U17	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	25
U18	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	25
CPU JTAG				
U18	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	11 25
U18	XDP_PHY	XDP	XDP_CPU_TMS	11 25
U18	XDP_PHY	XDP	XDP_CPU_TDI	11 25
U18	XDP_PHY	XDP	XDP_CPU_TDO	11 25
U19	XDP_PHY	XDP	XDP_CPU_TRST_L	11 25
U25	XDP_PHY	XDP	XDP_CPU_PRDY_L	11 25
U25	XDP_PHY	XDP	XDP_CPU_PREQ_L	11 25
PCH JTAG				
U18	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	18 25
U18	XDP_PHY	XDP	XDP_PCH_TMS	18 25
U18	XDP_PHY	XDP	XDP_PCH_TDI	18 25
U18	XDP_PHY	XDP	XDP_PCH_TDO	18 25

Chipset Test Interface

Electrical Contraint Set	Physical	Spacing		
OBS PCH Side				
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTA_OC_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTB_OC_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTC_OC_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTD_OC_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTB_OC_EHCI_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTD_OC_EHCI_R_L	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	AP_PWR_EN_R	20 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	SDCONN_STATE_CHANGE_R	20 25
U19 XDP_PCH_OBS	XDP_PHY	OBS_STROBE	TBT_CIO_PLUG_EVENT_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	ISOLATE_CPU_MEM_R_L	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	GPU_GOOD_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	DP_AUXCH_ISOL_R	18 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	SATARDRVR_EN_R	18 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	DP_TBT_SEL_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	JTAG_TBT_TCK_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	AUD_IPHS_SWITCH_EN_PCH_R	21 25
U19 XDP_PCH_OBS	XDP_PHY	XDP	ENET_LOW_PWR_PCH_R	21 25
U19 XDP_PCH_OBS_UNUSED	XDP_PHY	OBS_STROBE	XDP_PIN03	21 25
OBS XDP Side				
U16	XDP_PHY	XDP	XDP_DA0_USB_EXTA_OC_L	25
U16	XDP_PHY	XDP	XDP_DA1_USB_EXTB_OC_L	25
U16	XDP_PHY	XDP	XDP_DA2_USB_EXTC_OC_L	25
U16	XDP_PHY	XDP	XDP_DA3_USB_EXTD_OC_L	25
U16	XDP_PHY	XDP	XDP_DB0_USB_EXTB_OC_EHCI_L	25
U16	XDP_PHY	XDP	XDP_DB1_USB_EXTD_OC_EHCI_L	25
U16	XDP_PHY	XDP	XDP_DB2_AP_PWR_EN	25
U16	XDP_PHY	XDP	XDP_DB3_SDCONN_STATE_CHANGE	25
U17	XDP_PHY	OBS_STROBE	XDP_FC1_TBT_CIO_PLUG_EVENT	25
U16	XDP_PHY	XDP	XDP_DC0_ISOLATE_CPU_MEM_L	25
U15	XDP_PHY	XDP	XDP_DC1_GPU_GOOD	25
U22	XDP_PHY	XDP	XDP_DC2_DP_AUXCH_ISOL	25
U22	XDP_PHY	XDP	XDP_DC3_SATARDRVR_EN	25
U22	XDP_PHY	XDP	XDP_DD0_DP_TBT_SEL	25
U22	XDP_PHY	XDP	XDP_DD1_JTAG_TBT_TCK	25
U22	XDP_PHY	XDP	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH	25
U22	XDP_PHY	XDP	XDP_DD3_ENET_LOW_PWR_PCH	25
U22	XDP_PHY	OBS_STROBE	XDP_FC0_PCH_GPIO15	25
Standard usage branch off from OBS				
U22	XDP_PHY	XDP	USB_EXTA_OC_L	15 20 45
U22	XDP_PHY	XDP	USB_EXTB_OC_L	15 20 45
U20	XDP_PHY	XDP	USB_EXTC_OC_L	15 20 46
U20	XDP_PHY	XDP	USB_EXTD_OC_L	15 20 46
U20	XDP_PHY	XDP	USB_EXTB_OC_EHCI_L	15 20
U21	XDP_PHY	XDP	USB_EXTD_OC_EHCI_L	15 20
U21	XDP_PHY	XDP	AP_PWR_EN	15 20
U21	XDP_PHY	XDP	SDCONN_STATE_CHANGE	15 20 41
U20	XDP_PHY	OBS_STROBE	TBT_CIO_PLUG_EVENT	15 21
U20	XDP_PHY	XDP	ISOLATE_CPU_MEM_L	21 28 34
U20	XDP_PHY	XDP	GPU_GOOD	5 21
U20	XDP_PHY	XDP	DP_AUXCH_ISOL	15 18
U20	XDP_PHY	XDP	SATARDRVR_EN	15 18
U20	XDP_PHY	XDP	DP_TBT_SEL	21 62 75
U20	XDP_PHY	XDP	JTAG_TBT_TCK	15 21
U21	XDP_PHY	XDP	JTAG_TBT_TCK_ISOL	15 36
U22	XDP_PHY	XDP	AUD_IPHS_SWITCH_EN_PCH	21 26
U22	XDP_PHY	XDP	ENET_LOW_PWR_PCH	15 21 26
U22	XDP_PHY	XDP	DP_AUXCH_ISOL_EN	15

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_90D
COMP_SATA_PHY	*	SATA_50S

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=7.2X_DIELECTRIC	?
COMP_SATA_ISO	*	=5.4X_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

SATA

Electrical Contraint Set		Physical	Spacing		
PCH SATA Port 0 (HDD)					
180	SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_P	44
182	SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_N	44
183		SATA_PHY	SATA	SATA_HDD_R2D_C_P	18 44
189		SATA_PHY	SATA	SATA_HDD_R2D_C_N	18 44
184	SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_P	18 44
185	SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_N	18 44
101		SATA_PHY	SATA	SATA_HDD_D2R_C_P	44
103		SATA_PHY	SATA	SATA_HDD_D2R_C_N	44
PCH SATA Port 1 (SSD)					
187	SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_P	18 44
189	SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_N	18 44
186	SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_P	18 44
182	SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_N	18 44
PCH SATA Compensation					
180		COMP_SATA_PHY	COMP_SATA	PCH_SATA1COMP	18
180		COMP_SATA_PHY	COMP_SATA	PCH_SATA3COMP	18
180		COMP_SATA_PHY	COMP_SATA	PCH_SATA3RBIAS	18

Unused

Electrical Contraint Set	Physical	Spacing

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH_ISO	*	=6.5X_DIELECTRIC	?
COMP_PCH_ISO	*	=2:1_SPACING	?
PCH_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCH	*	*	CLK_PCH_ISO
COMP_PCH	*	*	COMP_PCH_ISO
PCH	*	*	PCH_ISO

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI_ISO	*	=3.6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCI	*	*	CLK_PCI_ISO

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC_ISO	*	=1.5:1_SPACING	?
CLK_LPC_ISO	*	=3.6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LPC	*	*	LPC_ISO
CLK_LPC	*	*	CLK_LPC_ISO

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA_ISO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	HDA_ISO

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL_ISO	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XTAL	*	*	XTAL_ISO

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI_ISO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	SPI_ISO

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
H33J	CLK_PCI_50S	CLK_PCI	PCH_CLK33M_PCIIN	18 26
H32J	CLK_PCI_50S	CLK_PCI	PCH_CLK33M_PCIOUT	20 26

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
H33D	LPC_50S	LPC	LPC_AD<3..0>	18 47 49
H33B	LPC_50S	LPC	LPC_R_AD<3..0>	18
H33C	LPC_50S	LPC	LPC_FRAME_L	18 47 49
H33F	LPC_50S	LPC	LFRAME_L	18
LPC Clocks				
H33G	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 49
H34G	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 26
H34J	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	26 47
H34F	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	20 26

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
H38D	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_SB	26
H36D	CLK_PCH_50S	CLK_PCH	PCH_CLK25M_XTALIN	18 26
PCH Ref Clock Comp				
H34D	PCH_50S	COMP_PCH	PCH_XCLK_RCOMP	18
PCH RTC 32K				
H44J	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 26
H44H	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 26
H45J	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	26
SMC 32K				
H42D	CLK_PCH_50S	CLK_PCH	PM_CLK32K_SUSCLK_R	19 48
H45D	CLK_PCH_50S	CLK_PCH	SMC_CLK32K	47 48

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
H47J	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	26
H48D	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	26
H48H	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	26
25M Reference Clocks				
H48C	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_ENET	26 39
H48G	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_ENET_R	26
H48D	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_TBT	26 36
H48F	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_TBT_R	36

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
H49D	HDA_50S	HDA	HDA_BIT_CLK	18 56
H48J	HDA_50S	HDA	HDA_BIT_CLK_R	18
H49G	HDA_50S	HDA	HDA_RST_L	18 56
H48F	HDA_50S	HDA	HDA_RST_R_L	18
H46G	HDA_50S	HDA	HDA_SDOUT	18 56
H46J	HDA_50S	HDA	HDA_SDOUT_R	15 18
H49C	HDA_50S	HDA	HDA_SYNC	15 18 56
H46D	HDA_50S	HDA	HDA_SYNC_R	18
H49D	HDA_50S	HDA	HDA_SDIN0	18 56
H46C	HDA_50S	HDA	AUD_SDI_R	56
H41C	HDA_50S	HDA	SPI_DESCRIPTOR_OVERRIDE_R	15
SPDIF				
H47C		HDA	AUD_SPDIF_CHIP	56
H47F		HDA	AUD_SPDIF_OUT	56 60

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
H49J	SPI_50S	SPI	SPI_CLK_R	18 49
H49F	SPI_50S	SPI	SPI_CLK	49
H49H	SPI_50S	SPI	SPI_ALT_CLK	49
H48H	SPI_50S	SPI	SPI_SMC_CLK	47 48
H48F	SPI_50S	SPI	SPI_MLB_CLK	48 49
H39G	SPI_50S	SPI	SPI_CS0_R_L	18 49
H39D	SPI_50S	SPI	SPI_CS0_L	49
H39H	SPI_50S	SPI	SPI_ALT_CS_L	49
H40H	SPI_50S	SPI	SPI_SMC_CS_L	47 48
H39F	SPI_50S	SPI	SPI_MLB_CS_L	48 49
H39C	SPI_50S	SPI	SPI_MOSI_R	18 49
H40G	SPI_50S	SPI	SPI_MOSI	49
H40J	SPI_50S	SPI	SPI_ALT_MOSI	49
H43H	SPI_50S	SPI	SPI_SMC_MOSI	47 48
H43F	SPI_50S	SPI	SPI_MLB_MOSI	48 49
H40C	SPI_50S	SPI	SPI_MISO	18 49
H40F	SPI_50S	SPI	SPI_ALT_MISO	49
H43J	SPI_50S	SPI	SPI_SMC_MISO	47 48
H43G	SPI_50S	SPI	SPI_MLB_MISO	48 49
H49G	SPI_50S	SPI	SPIROM_USE_MLB	21 49

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
USB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D
USB_HUB_PHY	*	USB_50S

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Comments
12.2.1	90	90	12/2.8 mils = 4.29:1	USB 2.0
13.3.1	85	85	20/2.8 mils = 7.14:1	USB 3.0
			50/2.8 mils = 17.9:1	USB 2.0/3.0

SMSC Hub Application Note 15.17
Single-ended impedance range from 45-80 ohm is acceptable

USB 2.0 Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=4.4X_DIELECTRIC	?
USB2_ISO	TOP,BOTTOM	=4.4X_DIELECTRIC	?
USB2_CLK_ISO	*	=18X_DIELECTRIC	?
USB2_CLK_ISO	TOP,BOTTOM	=18X_DIELECTRIC	?
USB_HUB_ISO	*	=2:1_SPACING	?

USB 3.0 Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_ISO	*	=7.3X_DIELECTRIC	?
USB3_ISO	TOP,BOTTOM	=7.3X_DIELECTRIC	?
USB3_CLK_ISO	*	=18X_DIELECTRIC	?
USB3_CLK_ISO	TOP,BOTTOM	=18X_DIELECTRIC	?
USB3_USB3_ISO	*	=7.3X_DIELECTRIC	?
USB3_USB3_ISO	TOP,BOTTOM	=7.3X_DIELECTRIC	?
USB3_USB3_ISO	ISL10	=5X_DIELECTRIC	?

USB 2.0 Spacing Rules

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB2	*CLK*	*	USB2_CLK_ISO
USB2	DISPLAYPORT	*	USB2_CLK_ISO
USB2	*TBT*	*	USB2_CLK_ISO
USB2	*ENET*	*	USB2_CLK_ISO
USB2	*SD*	*	USB2_CLK_ISO
USB3	PCIE	*	USB3_CLK_ISO
USB3	SATA	*	USB3_CLK_ISO
USB_HUB	*	*	USB_HUB_ISO

USB 3.0 Spacing Rules

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3	*	*	USB3_ISO
USB3	*CLK*	*	USB3_CLK_ISO
USB3	DISPLAYPORT	*	USB3_CLK_ISO
USB3	*TBT*	*	USB3_CLK_ISO
USB3	*ENET*	*	USB3_CLK_ISO
USB3	*SD*	*	USB3_CLK_ISO
USB3	PCIE	*	USB3_CLK_ISO
USB3	SATA	*	USB3_CLK_ISO
USB3	USB3	*	USB3_USB3_ISO

CAMERA CONTROLLER

Camera Controller's SMIA Interface & MISC. Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CAM_SE	*	Y	0.2 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D
CAM_PHY	*	CAM_SE

Camera Controller's SMIA Interface & MISC. Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?
CAM_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF
CAM	*	*	CAM_ISO

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
H49 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P	45
H50 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N	45
H52	USB3_PHY	USB3	USB3_EXTA_RX_F_P	20 45
H53	USB3_PHY	USB3	USB3_EXTA_RX_F_N	20 45
H45 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P	20 45
H46 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N	20 45
H42	USB3_PHY	USB3	USB3_EXTA_TX_F_P	45
H43	USB3_PHY	USB3	USB3_EXTA_TX_F_N	45
H48	USB3_PHY	USB3	USB3_EXTA_TX_C_P	45
H47	USB3_PHY	USB3	USB3_EXTA_TX_C_N	45
H37 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_P	20 45
H38 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_N	20 45
H33	USB2_PHY	USB2	USB2_EXTA_MUXED_P	45
H36	USB2_PHY	USB2	USB2_EXTA_MUXED_N	45
H39	USB2_PHY	USB2	USB2_EXTA_MUXED_F_P	45
H35	USB2_PHY	USB2	USB2_EXTA_MUXED_F_N	45
External Port B (J4610)				
H32 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P	45
H30 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N	45
H28	USB3_PHY	USB3	USB3_EXTB_RX_F_P	20 45
H24	USB3_PHY	USB3	USB3_EXTB_RX_F_N	20 45
H34 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P	20 45
H27 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N	20 45
H26	USB3_PHY	USB3	USB3_EXTB_TX_F_P	45
H29	USB3_PHY	USB3	USB3_EXTB_TX_F_N	45
H40	USB3_PHY	USB3	USB3_EXTB_TX_C_P	45
H44	USB3_PHY	USB3	USB3_EXTB_TX_C_N	45
H31 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_P	20 45
H25 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_N	20 45
H23	USB2_PHY	USB2	USB_PCH_9_P	20 45
H22	USB2_PHY	USB2	USB_PCH_9_N	20 45
H41	USB2_PHY	USB2	USB2_EXTB_MUXED_P	45
H21	USB2_PHY	USB2	USB2_EXTB_MUXED_N	45
H20	USB2_PHY	USB2	USB2_EXTB_MUXED_F_P	45
H18	USB2_PHY	USB2	USB2_EXTB_MUXED_F_N	45
External Port C (J4700)				
H17 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P	46
H15 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N	46
H13	USB3_PHY	USB3	USB3_EXTC_RX_F_P	20 46
H14	USB3_PHY	USB3	USB3_EXTC_RX_F_N	20 46
H11 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P	20 46
H12 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N	20 46
H10	USB3_PHY	USB3	USB3_EXTC_TX_F_P	46
H19	USB3_PHY	USB3	USB3_EXTC_TX_F_N	46
H16	USB3_PHY	USB3	USB3_EXTC_TX_C_P	46
H9	USB3_PHY	USB3	USB3_EXTC_TX_C_N	46
H48 USB2_CONN	USB2_PHY	USB2	USB_PCH_2_P	20 46
H49 USB2_CONN	USB2_PHY	USB2	USB_PCH_2_N	20 46
H50	USB2_PHY	USB2	USB2_EXTC_F_P	46
H52	USB2_PHY	USB2	USB2_EXTC_F_N	46
External Port D (J4710)				
H55 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P	46
H56 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N	46
H58	USB3_PHY	USB3	USB3_EXTD_RX_F_P	20 46
H60	USB3_PHY	USB3	USB3_EXTD_RX_F_N	20 46
H57 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P	20 46
H54 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N	20 46
H59	USB3_PHY	USB3	USB3_EXTD_TX_F_P	46
H51	USB3_PHY	USB3	USB3_EXTD_TX_F_N	46
H53	USB3_PHY	USB3	USB3_EXTD_TX_C_P	46
H61	USB3_PHY	USB3	USB3_EXTD_TX_C_N	46
H62 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_P	20 46
H63 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_N	20 46
H64	USB2_PHY	USB2	USB_PCH_10_P	20 46
H65	USB2_PHY	USB2	USB_PCH_10_N	20 46
H66	USB2_PHY	USB2	USB2_EXTD_MUXED_P	46
H67	USB2_PHY	USB2	USB2_EXTD_MUXED_N	46
H68	USB2_PHY	USB2	USB2_EXTD_MUXED_F_P	46
H69	USB2_PHY	USB2	USB2_EXTD_MUXED_F_N	46
Camera (U4200)				
H75 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P	42
H76 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_N	42
PCH USB Compensation				
H95	PCH_50S	COMP_PCH	PCH_USB_RBIAS	20

Electrical Contraint Set	Physical	Spacing	Voltage	
Camera Controller Local Ground				
H97	GND_PHY	GND	0V	CAM_AGND 42
H72	GND_PHY	GND	0V	CAM_PLLGND 42

USB Hub

Electrical Contraint Set	Physical	Spacing		
USB 2.0 Hub				
H48 USB2_HUB_PCH	USB2_PHY	USB2	USB_PCH_7_P	20 27
H49 USB2_HUB_PCH	USB2_PHY	USB2	USB_PCH_7_N	20 27
H49 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_P	27 35
H41 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_N	27 35
H50 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_MUX_P	35
H56 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_MUX_N	35
	USB_HUB_PHY	USB_HUB	USB_HUB_2P	27
H42	USB_HUB_PHY	USB_HUB	USB_HUB_2N	27
USB 2.0 Hub Misc.				
H55	USB_HUB_PHY	USB_HUB	USB_HUB_RESET_L	27
H62	USB_HUB_PHY	USB_HUB	USB_HUB_VBUS_DET	27
H51	USB_HUB_PHY	USB_HUB	USB_HUB_NON_REM0	27
H54	USB_HUB_PHY	USB_HUB	USB_HUB_NON_REM1	27
H57	USB_HUB_PHY	USB_HUB	USB_HUB_HS_IND	27
USB 2.0 Hub Compensation				
H47	PCH_50S	COMP_PCH	USB_HUB_RBIAS	27
USB 2.0 Hub Crystal				
H37	CLK_XTAL	XTAL	USB_HUB_XTAL1	27
H47	CLK_XTAL	XTAL	USB_HUB_XTAL2	27
H51	CLK_XTAL	XTAL	USB_HUB_XTAL2_R	27

Camera Controller

Electrical Contraint Set	Physical	Spacing		
SMIA				
H49 SMIA_DATA	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	42
H50 SMIA_DATA	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	42
H52 SMIA_CLK	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	42
H53 SMIA_CLK	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	42
MISC				
H59	SPI_50S	SPI	CAM_SF_CLK	42
H60	SPI_50S	SPI	CAM_SF_CLK_R	42
H58	SPI_50S	SPI	CAM_SF_DIN	42
H61	SPI_50S	SPI	CAM_SF_DIN_R	42
H63	SPI_50S	SPI	CAM_SF_CS_L	42
H53	SPI_50S	SPI	CAM_SF_WP_L	42
H52	SPI_50S	SPI	CAM_SF_DOUT	42
H54	SPI_50S	SPI	CAM_SF_DOUT_R	42
H44	SPI_50S	SPI	CAM_SF_HOLD_L	42
H62	CAM_PHY	CAM	CAM_USB_VRES	42
H52	CAM_PHY	CAM	MIPI_RESISTOR	42
H63		PM	CAM_EXT_BOOT_L	43
H63		PM	PCH_CAM_EXT_BOOT_R_L	21 43
H57		PM	CAM_P1V2_RST_HOLDOFF	43
H63		PM	CAM_P1V2_RST_HOLDOFF_L	43
I2C				
H43	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	42
H38	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	42
H42	SMB_PHY	SMB	SMB_ALS_F_SDA	42
H39	SMB_PHY	SMB	SMB_ALS_F_SCL	42
Camera Controller Crystal				
H29	CLK_XTAL	XTAL	CAM_XTAL_IN	42
H26	CLK_XTAL	XTAL	CAM_XTAL_OUT	42
H27	CLK_XTAL	XTAL	CAM_XTAL_OUT_R	42

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
SNS_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR
SNS_PHY	*	SNS_50S

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P5MM	*	Y	0.500 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_CTL_PHY	*	POWER_P5MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S
POWER_PHY	*	POWER_P6MM
GND_PHY	*	GND_P5MM

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?
SWNODE_LG2SW	*	=3:1_SPACING	?

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND
VR_LGATE	*	*	SWNODE_ISO
VR_LGATE	VR_SWITCH	*	SWNODE_LG2SW

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

CPU VccSA

Electrical Contraint Set		Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus								
I24		POWER_PHY	POWER	5V			REG_VCC_U7500	70
I25		POWER_PHY	POWER	5V			REG_PVCC_U7500	70
Local Ground								
I26		GND_PHY	GND	0V			AGND_VCCSAS0	70
VCCIO								
I27		POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VCCSAS0	70
I28		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VCCSAS0	70
I29		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VCCSAS0_RC	70
I31		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VCCSAS0	70
I30		VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_VCCSAS0	70
I33		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_VCCSAS0	70
I32		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_OCSET	70
I35		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_VO	70
I34			SENSE				SNS_CPU_VCCSA	13 70
I37	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_P	70
I36	VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_N	70
I38			SENSE				REG_VCCSAS0_FB	70
I39			SENSE				REG_VCCSAS0_RTN	70
I40		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_SREF	70
I41		VR_CTL_PHY	VR_CTL				REG_VCCSAS0_FSEL	70
Output Bus								
I42		POWER_PHY	POWER	0.925V			PPVCCSA_S0	6

CPU VccIO PCH 1.05V S0

Electrical Contraint Set		Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus								
I1		POWER_PHY	POWER	5V			REG_VCC_U7400	69
I2		POWER_PHY	POWER	5V			REG_PVCC_U7400	69
Local Ground								
I3		GND_PHY	GND	0V			AGND_CPU_P1V05S0	69
1.05V S0								
I5		POWER_PHY	VR_SWITCH	12V	TRUE		REG_CPU_PHASE_P1V05S0	69
I7		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_BOOT_P1V05S0	69
I6		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_CPU_BOOT_P1V05S0_RC	69
I8		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_UGATE_P1V05S0	69
I9		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_UGATE_P1V05S0_R	
I10		VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_CPU_LGATE_P1V05S0	69
I12		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_CPU_SNUBBER_P1V05S0	69
I11		VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_OCSET	69
I14		VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_VO	69
I13	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_P	13 69
I15	VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_N	13 69
I16		SNS_DIFF_PHY	SENSE				SNS_CPU_P1V05S0_XW_P	69
I17		SNS_DIFF_PHY	SENSE				SNS_CPU_P1V05S0_XW_N	69
I19			SENSE				REG_CPU_P1V05S0_FB	69
I18			SENSE				REG_CPU_P1V05S0_RTN	69
I21		VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_SREF	69
I20		VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_FSEL	69
Output Bus								
I22		POWER_PHY	POWER	1.05V			PP1V05_S0_CPU	6

PCH/GPU/TBT 1.05V S0

Electrical Contraint Set		Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus								
I44		POWER_PHY	POWER	5V			REG_VCC_UB700	99
Local Ground								
I45		GND_PHY	GND	0V			P1V05_AGND	99
1.05V S0								
I47		POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	99
I48		POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	99
I49		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	99
I50		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC	99
I51		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	99
I52		VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	99
I53		VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P1V05S0	99
I54		VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_P1V05S0	99
I55		VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	99
I56		VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	99
I72		POWER_PHY	VR_SWITCH	12V			REG_P1V05S0_VO_R	99
I73		POWER_PHY	VR_SWITCH	12V			P1V05_OCSET_R	99
I61			SENSE				REG_P1V05S0_FB	99
I62			SENSE				REG_P1V05S0_RTN	99
I63		VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	99
I64		VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	99
Output Bus								
I68		POWER_PHY	POWER	1.05V			PP1V05_S0_PCH	6
I66		POWER_PHY	POWER	1.05V			PP1V05_S0	6
FET Switched								
I67		POWER_PHY	POWER	1.05V			PP1V05_TBTLC	6 38
I69		POWER_PHY	POWER	1.05V			PP1V05_TBTCIO	6

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CPU Core Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H103	POWER_PHY	POWER	12V			PP12V_S0_CPUCORE_FLT — 66 67 68
H104	POWER_PHY	POWER	5V			REG_VCC_U7100 — 66
Local Ground						
H105	GND_PHY	GND	0V			AGND_CPU — 66 67 68
Phase 1						
H106	POWER_PHY	POWER	12V			REG_LVCC_U7210 — 67
H107	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1 — 66 67
H108	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1_R — 66
H109	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_1 — 67
H110	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_1 — 67
H111	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_1_RC — 67
H112	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_1 — 67
H113	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_1 — 67
H114	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_1 — 67
H115	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_1 — 67
H116 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_P — 66 67
H117 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_N — 67
H118		SENSE				REG_ISENCORE_1_NR — 66 67
Phase 2						
H119	POWER_PHY	POWER	12V			REG_LVCC_U7230 — 67
H120	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2 — 66 67
H121	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2_R — 66
H122	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_2 — 67
H123	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_2 — 67
H124	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_2_RC — 67
H125	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_2 — 67
H126	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_2 — 67
H127	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_2 — 67
H128	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_2 — 67
H129 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_P — 66 67
H130 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_N — 67
H131		SENSE				REG_ISENCORE_2_NR — 66 67
Phase 3						
H132	POWER_PHY	POWER	12V			REG_LVCC_U7250 — 67
H133	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3 — 66 67
H134	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3_R — 66
H135	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_3 — 67
H136	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_3 — 67
H137	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_3_RC — 67
H138	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_3 — 67
H139	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_3 — 67
H140	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_3 — 67
H141	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_3 — 67
H142 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_P — 66 67
H143 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_N — 67
H144		SENSE				REG_ISENCORE_3_NR — 66 67
Phase 4						
H145	POWER_PHY	POWER	12V			REG_LVCC_U7310 — 68
H146	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_4 — 66 68
H147	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_4_R — 66
H148	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_4 — 68
H149	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_4 — 68
H150	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_4_RC — 68
H151	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_4 — 68
H152	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_4 — 68
H153	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_4 — 68
H154	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_4 — 68
H155 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_4_P — 66 68
H156 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_4_N — 68
H157		SENSE				REG_ISENCORE_4_NR — 66 68
H158 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_XW_P — 66
H159 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_XW_N — 66
H160 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_R_P — 66
H161 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_R_N — 66
H162 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_P — 13 66
H163 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_N — 13 66
H164 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_P — 13 66
H165 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_N — 13 66
H166 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_P1V05_IOVDD_XW_P — 99
H167 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_P1V05_IOVDD_XW_N — 99

CPU AXG Phase and Core Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
AXG						
H168	POWER_PHY	POWER	12V			REG_LVCC_U7330 — 68
H169	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG — 66 68
H170	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG_R — 66
H171	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUAXG — 68
H172	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUAXG — 68
H173	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUAXG_RC — 68
H174	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUAXG — 68
H175	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUAXG — 68
H176	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUAXG — 68
H177	POWER_PHY	POWER	1.1V			PPCPUAXG_S0_SENSE — 68
H178 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_P — 68
H179 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_N — 68
H180		SENSE				REG_ISENAXG_PR — 66 68
H181		SENSE				REG_ISENAXG_NR — 66 68
H182 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_R_P — 66
H183 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_R_N — 66
H184 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_XW_P — 66
H185 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_XW_N — 66
ISL6364						
H186	VR_CTL_PHY	VR_CTL				REG_CPUCORE_COMP — 66
H187	VR_CTL_PHY	VR_CTL				CPUCORE_COMP_RC — 66
H188	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FB — 66
H189	VR_CTL_PHY	VR_CTL				CPUCORE_FB_RC — 66
H190	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_1 — 66
H191	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_2 — 66
H192	VR_CTL_PHY	VR_CTL				CPUCORE_PSICOMP_RC — 66
H193	VR_CTL_PHY	VR_CTL				REG_CPUCORE_PSICOMP — 66
H194	VR_CTL_PHY	VR_CTL				REG_CPUCORE_HFCOMP — 66
H195		SENSE				REG_CPUCORE_VSEN — 66
H196		SENSE				REG_CPUCORE_RGND — 66
H197	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IMON — 51 66
H198	VR_CTL_PHY	VR_CTL				CPUCORE_IMON_R — 66
H199	VR_CTL_PHY	VR_CTL				REG_CPUCORE_TM — 66
H200	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SUTH — 66
H201	VR_CTL_PHY	VR_CTL				REG_CPUCORE_NPSI — 66
H202	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FDVID — 66
H203	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IAUTO — 66
H204	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SW_FREQ — 66
H205	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RAMPADJ — 66
H206	VR_CTL_PHY	VR_CTL				REG_CPUCORE_EN_PWR — 66
H207	VR_CTL_PHY	VR_CTL				CPUCORE_EN_PWR_R — 66
H208	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RSET — 66
H209	VR_CTL_PHY	VR_CTL				REG_CPUAXG_COMP — 66
H210	VR_CTL_PHY	VR_CTL				CPUAXG_COMP_RC — 66
H211	VR_CTL_PHY	VR_CTL				REG_CPUAXG_FB — 66
H212	VR_CTL_PHY	VR_CTL				CPUAXG_FB_RC — 66
H213	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_1 — 66
H214	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_2 — 66
H215	VR_CTL_PHY	VR_CTL				REG_CPUAXG_HFCOMP — 66
H216		SENSE				REG_CPUAXG_VSEN — 66
H217		SENSE				REG_CPUAXG_RGND — 66
H218	VR_CTL_PHY	VR_CTL				REG_CPUAXG_IMON — 51 66
H219	VR_CTL_PHY	VR_CTL				CPUAXG_IMON_R — 66
H220	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TM — 66
H221	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TCOMP — 66
H222	VR_CTL_PHY	VR_CTL				REG_CPUAXG_SW_FREQ — 66
H223	VR_VID_PHY	VR_VID				CPU_VIDSCLK — 13 66
H224	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R — 13
H225	VR_VID_PHY	VR_VID				CPU_VIDALERT_L — 13 66
H226	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L — 13
H227	VR_VID_PHY	VR_VID				CPU_VIDSOUT — 13 66
H228	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R — 13
Output Bus						
H229	POWER_PHY	POWER	1.1V			PPVCORE_S0_CPU — 6
H230	POWER_PHY	POWER	1.1V			PPVAXG_S0 — 6

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3.3V S5/5V S4

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H1840	POWER_PHY	POWER	12V			REG_VIN_U7600	71
H1841	POWER_PHY	POWER	5V			REG_VCC1_U7600	71
H1842	POWER_PHY	POWER	5V			REG_VCC2_U7600	71
3.3V S5							
H1843	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5	71
H1844	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5	71
H1845	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC	71
H1846	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5	71
H1847	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P3V3S5	71
H1848	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5	71
H1849	VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN	71
H1850	VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET	71
H1851	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET	71
H1852	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT	71
H1853	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R	71
H1854	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB	71
5V S3							
H1855	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4	71
H1856	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4	71
H1857	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC	71
H1858	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4	71
H1859	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P5VS4	71
H1860	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4	71
H1861	VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN	71
H1862	VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET	71
H1863	VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET	71
H1864	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT	71
H1865	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R	71
H1866	VR_CTL_PHY	VR_CTL				REG_P5VS4_FB	71
Output Bus							
H1867	POWER_PHY	POWER	5V			PP5V_S5	6
H1868	POWER_PHY	POWER	5V			PP5V_S4	6
H1869	POWER_PHY	POWER	3.3V			PP3V3_S5	6
FET Switched							
H1870	POWER_PHY	POWER	5V			PP5V_S0	6
H1871	POWER_PHY	POWER	3.3V			PP3V3_S4	6
H1872	POWER_PHY	POWER	3.3V			PP3V3_S0	6
H1873	POWER_PHY	POWER	3.3V			PP3V3_S4_ENET	6
H1874	POWER_PHY	POWER	3.3V			PP3V3_TBTLC	6
H1875	POWER_PHY	POWER	3.3V			PP3V3_S4_AP	6
H1876	POWER_PHY	POWER	3.3V			PP3V3_S0_SSD	6

VDDQ S3 (1.5V)/VTT S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H1877	POWER_PHY	POWER	5V			REG_V5IN_U7700	72
Local Ground							
H1878	GND_PHY	GND	0V			AGND_VDDQS3	72
VDDQ S3							
H1879	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3	72
H1880	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L	72
H1881	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3	72
H1882	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC	72
H1883	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3	72
H1884	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R	72
H1885	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_VDDQS3	72
H1886	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3	72
H1887	POWER_PHY	POWER	1.5V			PPVDDQ_S3_SENSE	
H1888	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS	72
H1889	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF	72
H1890	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN	72
H1891	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE	72
H1892	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP	72
H1893	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS	72
Output Bus							
H1894	POWER_PHY	POWER	1.5V			PPVDDQ_S3	6
H1895	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVTT_S0	6
FET Switched							
H1896	POWER_PHY	POWER	1.5V			PP1V5_S0	6
Sensed							
H1897	POWER_PHY	POWER	1.5V			PPVDDQ_S3_DDR	6
H1898	POWER_PHY	POWER	1.5V			PP1V5_S0_CPU_MEM	6
H1899	POWER_PHY	POWER	1.5V			PPFBVDDQ_S0_GPU	6

DDR3 Vref

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Memory Vref							
H1900	POWER_PHY	POWER	3.3V			PP3V3_S4_VREFMRGN_DAC	34
H1901	POWER_PHY	POWER	3.3V			PP3V3_S4_VREFMRGN_CTRL	34
H1902	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_A_S3	6
H1903	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_B_S3	6
H1904	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_A	11 34
H1905	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_B	11 34
H1906	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_A_S3	6
H1907	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_B_S3	6
H1908	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DDR_VREF	11
H1909	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVTT_S3	6

1.8V S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
1.8V S0							
H1910	POWER_PHY	VR_SWITCH	5V	TRUE		REG_PHASE_P1V8S0	72
H1911	VR_CTL_PHY	VR_CTL				REG_P1V8S0_VFB	72
H1912	VR_CTL_PHY	VR_CTL				REG_P1V8S0_SYNCH	72
Output Bus							
H1913	POWER_PHY	POWER	1.8V			PP1V8_S0	6

HDD S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
HDD S0							
H1914	POWER_PHY	POWER	5V			PP5V_S0_HDD	6

12V S5

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
H1915	POWER_PHY	POWER	12V			PP12V_ACDC	6
FET Switched							
H1916	POWER_PHY	POWER	12V			PP12V_S0	6
Sensed							
H1917	POWER_PHY	POWER	12V			PP12V_S5	6
H1918	POWER_PHY	POWER	12V			PP12V_G3H	6
H1919	POWER_PHY	POWER	12V			PP12V_G3H_P3V42	73
H1920	POWER_PHY	POWER	12V			PP12V_S0_FBVDDQ	6
H1921	POWER_PHY	POWER	12V			PP12V_S0_CPU_P1V05	6
H1922	POWER_PHY	POWER	12V			PP12V_S0_VCCSA	6
H1923	POWER_PHY	POWER	12V			PP12V_S0_P1V05	6
H1924	POWER_PHY	POWER	12V			PP12V_S0_HDD	6
H1925	POWER_PHY	POWER	12V			PP12V_S0_BLC	6

Ground/Common

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Common							
H1926	GND_PHY	GND	0V			GND	

3V42 S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
3V42 S0							
H1927	POWER_PHY	VR_SWITCH	5V	TRUE		P3V42G3H_SW	73
H1928	VR_CTL_PHY	VR_CTL				P3V42G3H_FB	73
H1929	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L	73
H1930	POWER_PHY	POWER	3.3V			PP3V3_G3	6
H1931	POWER_PHY	POWER	3.3V			PP3V42_G3H	6

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	0.075MM
TBT_GEN_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C_ISO	*	=2x_DIELECTRIC	?
TBT_SPI_ISO	*	=2x_DIELECTRIC	?
TBTDP_ISO	*	=5x_DIELECTRIC	?
TBTDP_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?
TBT_GEN_ISO	*	=2x_DIELECTRIC	?
BGA_TBT_AREA	*	0.075MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_TBT	BGA_TBT_AREA
TBT_I2C	*	*	TBT_I2C_ISO
TBT_SPI	*	*	TBT_SPI_ISO
TBTDP	*	*	TBTDP_ISO
TBT_GEN	*	*	TBT_GEN_ISO

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_ISO	*	=6.7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_ISO

MAX LENGTH OF DISPLAYPORT TRACES: 6 INCHES

DISPLAYPORT INTRA-PAIR MATCHING SHOULD BE 1 PS. INTER-PAIR MATCHING SHOULD BE WITHIN 150 PS.
DISPLAYPORT AUX CHANNEL INTRA-PAIR MATCHING SHOULD BE 5 PS.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing		
H51	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	NO_TEST=TRUE 36 90
H52	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	NO_TEST=TRUE 36 90
H53 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	NO_TEST=TRUE 36
H54 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	NO_TEST=TRUE 36
H48	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	36 90
H47	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	36 90
H57 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	36
H58 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	36
H31	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	NO_TEST=TRUE 36 90
H32	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	NO_TEST=TRUE 36 90
H29 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	NO_TEST=TRUE 36
H22 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	NO_TEST=TRUE 36
H23	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	36 90
H24	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	36 90
H26 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	36
H25 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	36
H89 DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	NO_TEST=TRUE 75
H90 DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	NO_TEST=TRUE 75
H87 DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	NO_TEST=TRUE 75
H88 DP_TNTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	NO_TEST=TRUE 75
H92 DP_TNTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P	75
H91 DP_TNTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N	75
H93	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P	75
H94	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N	75
H31	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SCL	36 50
H32	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SDA	36 50
H53 TBT_SPI_CLK	TBT_I2C_55S	TBT_SPI	TBT_SPI_CLK	36
H52 TBT_SPI_MOSI	TBT_I2C_55S	TBT_SPI	TBT_SPI_MOSI	36
H51 TBT_SPI_MISO	TBT_I2C_55S	TBT_SPI	TBT_SPI_MISO	36
H54 TBT_SPI_CS_L	TBT_I2C_55S	TBT_SPI	TBT_SPI_CS_L	36
H86	TBT_GEN_55S	TBT_GEN	TBT_A_CONFIG1_BUF	36 77
H85	TBT_GEN_55S	TBT_GEN	TBT_A_CONFIG2_RC	36 77
H83	TBT_GEN_55S	TBT_GEN	TBT_B_CONFIG1_BUF	36 79
H96	TBT_GEN_55S	TBT_GEN	TBT_B_CONFIG2_RC	36 79
H95	TBT_GEN_55S	TBT_GEN	TBT_A_LSTX	36 77
H97	TBT_GEN_55S	TBT_GEN	TBT_A_LSRX	36 77
H99	TBT_GEN_55S	TBT_GEN	TBT_B_LSTX	36 79
H98	TBT_GEN_55S	TBT_GEN	TBT_B_LSRX	36 79
H67	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_HPD	36 90
H66	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_HPD	36 90
H68	TBT_GEN_55S	TBT_GEN	DP_TBTSRC_HPD	36 75
H69	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_DDC_CLK	76 92
H70	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_DDC_DATA	76 92
H65	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_DDC_CLK	76 91
H64	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_DDC_DATA	76 91
H76	TBT_GEN_55S	TBT_GEN	VIDEO_ON	74 78
H74	TBT_GEN_55S	TBT_GEN	VIDEO_ON_L	5 78
H75	TBT_GEN_55S	TBT_GEN	BDV_BKL_PWM	48 75
H73	TBT_GEN_55S	TBT_GEN	GPU_LCD_BKLT_PWM	75 91
H72	TBT_GEN_55S	TBT_GEN	LCD_BL_PWM	75
H71	TBT_GEN_55S	TBT_GEN	LCD_BL_FILT	75
H78	TBT_GEN_55S	TBT_GEN	LCD_BKLT_PWM	75 80

*: Only used on hosts supporting T29 video-in

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing		
Port A				
T641 TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	NO_TEST=TRUE 36 77
T642 TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	NO_TEST=TRUE 36 77
T720 TBT_A_R2D_PINV	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	NO_TEST=TRUE 36 77
T721 TBT_A_R2D_PINV	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	NO_TEST=TRUE 36 77
T644	TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	NO_TEST=TRUE 77
T645	TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	NO_TEST=TRUE 77
T660 DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	NO_TEST=TRUE 36 77
T659 DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	NO_TEST=TRUE 36 77
T658 DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	NO_TEST=TRUE 36 77
T657 DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	NO_TEST=TRUE 36 77
T643	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	NO_TEST=TRUE 77
T647	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	NO_TEST=TRUE 77
T679	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	NO_TEST=TRUE 77
T678	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	NO_TEST=TRUE 77
T649	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	77
T648	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	77
T646	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	NO_TEST=TRUE 77
T650	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	NO_TEST=TRUE 77
T654 TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	NO_TEST=TRUE 36 77
T655 TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	NO_TEST=TRUE 36 77
T652 TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	NO_TEST=TRUE 36 77
T653 TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	NO_TEST=TRUE 36 77
T662 DP_TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	36 77
T661 DP_TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	36 77
T665	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	77
T664	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	77
T641	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P	77
T640	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N	77
T656	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	NO_TEST=TRUE 77
T651	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	NO_TEST=TRUE 77
Port B				
T663 TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1..0>	NO_TEST=TRUE 36 79
T662 TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1..0>	NO_TEST=TRUE 36 79
T666	TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	NO_TEST=TRUE 79
T667	TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	NO_TEST=TRUE 79
T668 DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	NO_TEST=TRUE 36 79
T669 DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	NO_TEST=TRUE 36 79
T670 DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	NO_TEST=TRUE 36 79
T671 DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	NO_TEST=TRUE 36 79
T672	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	NO_TEST=TRUE 79
T673	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	NO_TEST=TRUE 79
T674	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	NO_TEST=TRUE 79
T675	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	NO_TEST=TRUE 79
T676	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	NO_TEST=TRUE 79
T677	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	NO_TEST=TRUE 79
T681	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	NO_TEST=TRUE 79
T680	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	NO_TEST=TRUE 79
T685 TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	NO_TEST=TRUE 36 79
T684 TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	NO_TEST=TRUE 36 79
T682 TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	NO_TEST=TRUE 36 79
T683 TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	NO_TEST=TRUE 36 79
T686 DP_TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	36 79
T687 DP_TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	36 79
T688	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	79
T689	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	79
T690	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P	79
T691	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N	79
T694	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	NO_TEST=TRUE 79
T693	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	NO_TEST=TRUE 79

DisplayPort

Electrical Contraint Set	Physical	Spacing		
Graphics Source				
T644 DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	NO_TEST=TRUE 75 90
T643 DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	NO_TEST=TRUE 75 90
T642 DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	NO_TEST=TRUE 75 90
T645 DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	NO_TEST=TRUE 75 90
T646	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P	75
T647	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N	75
Internal Panel				
T600	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	NO_TEST=TRUE 75
T600	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	NO_TEST=TRUE 75
T604 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	NO_TEST=TRUE 75 78
T603 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	NO_TEST=TRUE 75 78
T600 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	75 78
T601 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	75 78
Internal DP SPDIF				
T611		HDA	DP_INT_SPDIF_AUDIO	56 78

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GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

	Trace-to-Trace				Isolation				
Table	Micro	Design	Strip	Design	Micro	Design	Strip	Design	Comments
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Memory address (MA). Implented 4.5 Gbps or less rules for K70.
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Address dynamic bus inversion (ADBI)
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Control (CTRL)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Clock (CLK)
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data (DQ)
5-6/5-7	7:1	7:1	7:1	7:1	7:1	7:1	7:1	7:1	Error detection pins (EDC). Using larger isolation rules,
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data dynamic bus inversion (DBI)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Forwarded clock (WCK)

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=3X_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR_MA2MA	*	=2x_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=3X_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CLK2CLK	*	=3X_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3x_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_EDC_ISO	*	=3X_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_EDC2EDC	*	=3X_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_DBI2DBI	*	=3x_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_WCK2WCK	*	=3X_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=5x_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

GPU

GPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_GPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

GPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_GPU_ISO	*	=4:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_GPU	*	*	CLK_GPU_ISO

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing				
Memory Address						
1642 GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	NO_TEST=TRUE	84	86
1643 GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	NO_TEST=TRUE	84	86
Address Dynamic Bus Inv						
1644 GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	NO_TEST=TRUE	84	86
1645 GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	NO_TEST=TRUE	84	86
Control						
1647 GDDR_A0_CKE	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	NO_TEST=TRUE	84	86
1648 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	NO_TEST=TRUE	84	86
1649 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	NO_TEST=TRUE	84	86
1650 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	NO_TEST=TRUE	84	86
1651 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	NO_TEST=TRUE	84	86
1652 GDDR_A1_CKE	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	NO_TEST=TRUE	84	86
1653 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	NO_TEST=TRUE	84	86
1654 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	NO_TEST=TRUE	84	86
1655 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	NO_TEST=TRUE	84	86
1656 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	NO_TEST=TRUE	84	86
Clock						
1657 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	NO_TEST=TRUE	84	86
1658 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	NO_TEST=TRUE	84	86
1659 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	NO_TEST=TRUE	84	86
1660 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	NO_TEST=TRUE	84	86
Data						
1661 GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	NO_TEST=TRUE	84	86
1662 GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	NO_TEST=TRUE	84	86
1663 GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	NO_TEST=TRUE	84	86
1664 GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	NO_TEST=TRUE	84	86
1665 GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	NO_TEST=TRUE	84	86
1666 GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	NO_TEST=TRUE	84	86
1667 GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	NO_TEST=TRUE	84	86
1668 GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	NO_TEST=TRUE	84	86
Error Detection						
1637 GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	NO_TEST=TRUE	84	86
1638 GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	NO_TEST=TRUE	84	86
1639 GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	NO_TEST=TRUE	84	86
1640 GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	NO_TEST=TRUE	84	86
1697 GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	NO_TEST=TRUE	84	86
1696 GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	NO_TEST=TRUE	84	86
1695 GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	NO_TEST=TRUE	84	86
1694 GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	NO_TEST=TRUE	84	86
Data Dynamic Bus Inv						
1637 GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	NO_TEST=TRUE	84	86
1638 GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	NO_TEST=TRUE	84	86
1639 GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	NO_TEST=TRUE	84	86
1640 GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	NO_TEST=TRUE	84	86
1689 GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	NO_TEST=TRUE	84	86
1688 GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	NO_TEST=TRUE	84	86
1687 GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	NO_TEST=TRUE	84	86
1686 GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	NO_TEST=TRUE	84	86
Forwarded Clock						
1648 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	NO_TEST=TRUE	84	86
1647 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	NO_TEST=TRUE	84	86
1650 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	NO_TEST=TRUE	84	86
1649 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	NO_TEST=TRUE	84	86
1690 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	NO_TEST=TRUE	84	86
1691 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	NO_TEST=TRUE	84	86
1692 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	NO_TEST=TRUE	84	86
1693 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	NO_TEST=TRUE	84	86

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing				
Memory Address						
1698 GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	NO_TEST=TRUE	84	87
1699 GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	NO_TEST=TRUE	84	87
Address Dynamic Bus Inv						
1696 GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	NO_TEST=TRUE	84	87
1697 GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	NO_TEST=TRUE	84	87
Control						
1698 GDDR_B0_CKE	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	NO_TEST=TRUE	84	87
1701 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	NO_TEST=TRUE	84	87
1702 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	NO_TEST=TRUE	84	87
1703 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	NO_TEST=TRUE	84	87
1704 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	NO_TEST=TRUE	84	87
1705 GDDR_B1_CKE	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	NO_TEST=TRUE	84	87
1706 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	NO_TEST=TRUE	84	87
1707 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	NO_TEST=TRUE	84	87
1708 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	NO_TEST=TRUE	84	87
1709 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	NO_TEST=TRUE	84	87
Clock						
1699 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	NO_TEST=TRUE	84	87
1710 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	NO_TEST=TRUE	84	87
1700 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	NO_TEST=TRUE	84	87
1711 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	NO_TEST=TRUE	84	87
Data						
1712 GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	NO_TEST=TRUE	84	87
1713 GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	NO_TEST=TRUE	84	87
1714 GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	NO_TEST=TRUE	84	87
1715 GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	NO_TEST=TRUE	84	87
1716 GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	NO_TEST=TRUE	84	87
1717 GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	NO_TEST=TRUE	84	87
1718 GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	NO_TEST=TRUE	84	87
1719 GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	NO_TEST=TRUE	84	87
Error Detection						
1720 GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	NO_TEST=TRUE	84	87
1721 GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	NO_TEST=TRUE	84	87
1722 GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	NO_TEST=TRUE	84	87
1723 GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	NO_TEST=TRUE	84	87
1724 GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	NO_TEST=TRUE	84	87
1725 GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	NO_TEST=TRUE	84	87
1726 GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	NO_TEST=TRUE	84	87
1727 GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	NO_TEST=TRUE	84	87
Data Dynamic Bus Inv						
1720 GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	NO_TEST=TRUE	84	87
1721 GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	NO_TEST=TRUE	84	87
1722 GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	NO_TEST=TRUE	84	87
1723 GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	NO_TEST=TRUE	84	87
1724 GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	NO_TEST=TRUE	84	87
1725 GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	NO_TEST=TRUE	84	87
1726 GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	NO_TEST=TRUE	84	87
1727 GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	NO_TEST=TRUE	84	87
Forwarded Clock						
1728 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	NO_TEST=TRUE	84	87
1727 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	NO_TEST=TRUE	84	87
1730 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	NO_TEST=TRUE	84	87
1729 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	NO_TEST=TRUE	84	87
1740 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	NO_TEST=TRUE	84	87
1741 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	NO_TEST=TRUE	84	87
1742 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	NO_TEST=TRUE	84	87
1743 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	NO_TEST=TRUE	84	87

GPU

Electrical Contraint Set	Physical	Spacing				
Clocks						
1747	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_PL		83	
1748	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_NG		83	
1749	CLK_PCIE_PHY	CLK_PCIE	GPU_TESTMODE		83	
1750	CLK_PCIE_PHY	CLK_PCIE	GPU_PEX_TERMP		83	
1751	CLK_GPU_55S	CLK_GPU	FB_A0_CK_MID	NO_TEST=TRUE	86	
1752	CLK_GPU_55S	CLK_GPU	FB_A1_CK_MID	NO_TEST=TRUE	86	
1753	CLK_GPU_55S	CLK_GPU	FB_B0_CK_MID	NO_TEST=TRUE	87	
1754	CLK_GPU_55S	CLK_GPU	FB_B1_CK_MID	NO_TEST=TRUE	87	
1755	CLK_GPU_55S	CLK_GPU	FB_C0_CK_MID	NO_TEST=TRUE	88	
1756	CLK_GPU_55S	CLK_GPU	FB_C1_CK_MID	NO_TEST=TRUE	88	
1757	CLK_GPU_55S	CLK_GPU	FB_D0_CK_MID	NO_TEST=TRUE	89	
1758	CLK_GPU_55S	CLK_GPU	FB_D1_CK_MID	NO_TEST=TRUE	89	
1772	CLK_GPU_55S	CLK_GPU	GPU_JTAG_TCK		91	
1773	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK		91	
1774	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK_R		91	
1775	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTAL_P		91	
1776	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTAL_N		91	
SMB						
1564	SMB_PHY	SMB	GPU_SMB_CLK		91	
1565	SMB_PHY	SMB	GPU_SMB_DAT		91	
1566	SMB_PHY	SMB	GPU_SMB_CLK_R		50	91
1567	SMB_PHY	SMB	GPU_SMB_DAT_R		50	91
PCIe Compensation						
1569	PCIE_50S	COMP_PCIE	FB_CAL_PD_VDDQ		94	
1568	PCIE_50S	COMP_PCIE	FB_CAL_PU_GND		94	
1570	PCIE_50S	COMP_PCIE	FB_CAL_TERM_GND		94	

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing				
Reset						
1744 GDDR_A0_RESET	GDDR_50S	GDDR_CTRL	FB_A0_RESET_L		84	86
1745 GDDR_A1_RESET	GDDR_50S	GDDR_CTRL	FB_A1_RESET_L		84	86
1746 GDDR_B0_RESET	GDDR_50S	GDDR_CTRL	FB_B0_RESET_L		84	87
1747 GDDR_B1_RESET	GDDR_50S	GDDR_CTRL	FB_B1_RESET_L		84	87
1760 GDDR_C0_RESET	GDDR_50S	GDDR_CTRL	FB_C0_RESET_L		85	88
1761 GDDR_C1_RESET	GDDR_50S	GDDR_CTRL	FB_C1_RESET_L		85	88
1762 GDDR_D0_RESET	GDDR_50S	GDDR_CTRL	FB_D0_RESET_L		85	89
1763 GDDR_D1_RESET	GDDR_50S	GDDR_CTRL	FB_D1_RESET_L		85	89

SYNC_MASTER=D8_MLB SYNC_DATE=01/11/2012

PAGE TITLE: GDDR5/GPU Constraints

Apple Inc.

DRAWING NUMBER: 051-9505 SIZE: D

REVISION: 8.0.0

BRANCH: prefsb

PAGE: 132 OF 144

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GDDR5 FRAME BUFFER C

Electrical Contraint Set	Physical	Spacing			
Memory Address					
1644 GDDR_C0_MA	GDDR_MA_PHY	GDDR_C_0_MA	FB_C0_A<8..0>	NO_TEST=TRUE	85 88
1645 GDDR_C1_MA	GDDR_MA_PHY	GDDR_C_1_MA	FB_C1_A<8..0>	NO_TEST=TRUE	85 88
Address Dynamic Bus Inv					
1646 GDDR_C0_ADBI	GDDR_ADBI_PHY	GDDR_C_0_ADBI	FB_C0_ABI_L	NO_TEST=TRUE	85 88
1647 GDDR_C1_ADBI	GDDR_ADBI_PHY	GDDR_C_1_ADBI	FB_C1_ABI_L	NO_TEST=TRUE	85 88
Control					
1649 GDDR_C0_CKE	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_CKE_L	NO_TEST=TRUE	85 88
1650 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_CS_L	NO_TEST=TRUE	85 88
1651 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_WE_L	NO_TEST=TRUE	85 88
1652 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_CAS_L	NO_TEST=TRUE	85 88
1653 GDDR_C0_CTRL	GDDR_CTRL_PHY	GDDR_C_0_CTRL	FB_C0_RAS_L	NO_TEST=TRUE	85 88
1655 GDDR_C1_CKE	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_CKE_L	NO_TEST=TRUE	85 88
1656 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_CS_L	NO_TEST=TRUE	85 88
1657 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_WE_L	NO_TEST=TRUE	85 88
1658 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_CAS_L	NO_TEST=TRUE	85 88
1659 GDDR_C1_CTRL	GDDR_CTRL_PHY	GDDR_C_1_CTRL	FB_C1_RAS_L	NO_TEST=TRUE	85 88
Clock					
1661 GDDR_C0_CLK	GDDR_CLK_PHY	GDDR_C_0_CLK	FB_C0_CLK_P	NO_TEST=TRUE	85 88
1662 GDDR_C0_CLK	GDDR_CLK_PHY	GDDR_C_0_CLK	FB_C0_CLK_N	NO_TEST=TRUE	85 88
1664 GDDR_C1_CLK	GDDR_CLK_PHY	GDDR_C_1_CLK	FB_C1_CLK_P	NO_TEST=TRUE	85 88
1665 GDDR_C1_CLK	GDDR_CLK_PHY	GDDR_C_1_CLK	FB_C1_CLK_N	NO_TEST=TRUE	85 88
Data					
1667 GDDR_C0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<7..0>	NO_TEST=TRUE	85 88
1668 GDDR_C0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<15..8>	NO_TEST=TRUE	85 88
1669 GDDR_C0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<23..16>	NO_TEST=TRUE	85 88
1670 GDDR_C0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_C_0_DQ	FB_C0_DQ<31..24>	NO_TEST=TRUE	85 88
1672 GDDR_C1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<7..0>	NO_TEST=TRUE	85 88
1673 GDDR_C1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<15..8>	NO_TEST=TRUE	85 88
1674 GDDR_C1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<23..16>	NO_TEST=TRUE	85 88
1675 GDDR_C1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_C_1_DQ	FB_C1_DQ<31..24>	NO_TEST=TRUE	85 88
Error Detection					
1676 GDDR_C0_EDC0	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<0>	NO_TEST=TRUE	85 88
1677 GDDR_C0_EDC1	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<1>	NO_TEST=TRUE	85 88
1678 GDDR_C0_EDC2	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<2>	NO_TEST=TRUE	85 88
1679 GDDR_C0_EDC3	GDDR_EDC_PHY	GDDR_C_0_EDC	FB_C0_EDC<3>	NO_TEST=TRUE	85 88
1681 GDDR_C1_EDC0	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<0>	NO_TEST=TRUE	85 88
1682 GDDR_C1_EDC1	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<1>	NO_TEST=TRUE	85 88
1683 GDDR_C1_EDC2	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<2>	NO_TEST=TRUE	85 88
1684 GDDR_C1_EDC3	GDDR_EDC_PHY	GDDR_C_1_EDC	FB_C1_EDC<3>	NO_TEST=TRUE	85 88
Data Dynamic Bus Inv					
1685 GDDR_C0_DBI0	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<0>	NO_TEST=TRUE	85 88
1686 GDDR_C0_DBI1	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<1>	NO_TEST=TRUE	85 88
1687 GDDR_C0_DBI2	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<2>	NO_TEST=TRUE	85 88
1688 GDDR_C0_DBI3	GDDR_DBI_PHY	GDDR_C_0_DBI	FB_C0_DBI_L<3>	NO_TEST=TRUE	85 88
1690 GDDR_C1_DBI0	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<0>	NO_TEST=TRUE	85 88
1691 GDDR_C1_DBI1	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<1>	NO_TEST=TRUE	85 88
1692 GDDR_C1_DBI2	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<2>	NO_TEST=TRUE	85 88
1693 GDDR_C1_DBI3	GDDR_DBI_PHY	GDDR_C_1_DBI	FB_C1_DBI_L<3>	NO_TEST=TRUE	85 88
Forwarded Clock					
1695 GDDR_C0_WCK0	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_P<0>	NO_TEST=TRUE	85 88
1696 GDDR_C0_WCK0	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_N<0>	NO_TEST=TRUE	85 88
1697 GDDR_C0_WCK1	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_P<1>	NO_TEST=TRUE	85 88
1698 GDDR_C0_WCK1	GDDR_WCK_PHY	GDDR_C_0_WCK	FB_C0_WCLK_N<1>	NO_TEST=TRUE	85 88
1699 GDDR_C1_WCK0	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_P<0>	NO_TEST=TRUE	85 88
1700 GDDR_C1_WCK0	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_N<0>	NO_TEST=TRUE	85 88
1701 GDDR_C1_WCK1	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_P<1>	NO_TEST=TRUE	85 88
1702 GDDR_C1_WCK1	GDDR_WCK_PHY	GDDR_C_1_WCK	FB_C1_WCLK_N<1>	NO_TEST=TRUE	85 88
Memory Address					
1745 GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<12>	NO_TEST=TRUE	84 86
1746 GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<12>	NO_TEST=TRUE	84 86
1746 GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<12>	NO_TEST=TRUE	84 87
1747 GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<12>	NO_TEST=TRUE	84 87
1748 GDDR_C0_MA	GDDR_MA_PHY	GDDR_C_0_MA	FB_C0_A<12>	NO_TEST=TRUE	85 88
1749 GDDR_C1_MA	GDDR_MA_PHY	GDDR_C_1_MA	FB_C1_A<12>	NO_TEST=TRUE	85 88
1750 GDDR_D0_MA	GDDR_MA_PHY	GDDR_D_0_MA	FB_D0_A<12>	NO_TEST=TRUE	85 89
1751 GDDR_D1_MA	GDDR_MA_PHY	GDDR_D_1_MA	FB_D1_A<12>	NO_TEST=TRUE	85 89

GDDR5 FRAME BUFFER D

Electrical Contraint Set	Physical	Spacing			
Memory Address					
1695 GDDR_D0_MA	GDDR_MA_PHY	GDDR_D_0_MA	FB_D0_A<8..0>	NO_TEST=TRUE	85 89
1696 GDDR_D1_MA	GDDR_MA_PHY	GDDR_D_1_MA	FB_D1_A<8..0>	NO_TEST=TRUE	85 89
Address Dynamic Bus Inv					
1695 GDDR_D0_ADBI	GDDR_ADBI_PHY	GDDR_D_0_ADBI	FB_D0_ABI_L	NO_TEST=TRUE	85 89
1697 GDDR_D1_ADBI	GDDR_ADBI_PHY	GDDR_D_1_ADBI	FB_D1_ABI_L	NO_TEST=TRUE	85 89
Control					
1698 GDDR_D0_CKE	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_CKE_L	NO_TEST=TRUE	85 89
1703 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_CS_L	NO_TEST=TRUE	85 89
1700 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_WE_L	NO_TEST=TRUE	85 89
1702 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_CAS_L	NO_TEST=TRUE	85 89
1701 GDDR_D0_CTRL	GDDR_CTRL_PHY	GDDR_D_0_CTRL	FB_D0_RAS_L	NO_TEST=TRUE	85 89
1705 GDDR_D1_CKE	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_CKE_L	NO_TEST=TRUE	85 89
1706 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_CS_L	NO_TEST=TRUE	85 89
1707 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_WE_L	NO_TEST=TRUE	85 89
1708 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_CAS_L	NO_TEST=TRUE	85 89
1707 GDDR_D1_CTRL	GDDR_CTRL_PHY	GDDR_D_1_CTRL	FB_D1_RAS_L	NO_TEST=TRUE	85 89
Clock					
1709 GDDR_D0_CLK	GDDR_CLK_PHY	GDDR_D_0_CLK	FB_D0_CLK_P	NO_TEST=TRUE	85 89
1710 GDDR_D0_CLK	GDDR_CLK_PHY	GDDR_D_0_CLK	FB_D0_CLK_N	NO_TEST=TRUE	85 89
1709 GDDR_D1_CLK	GDDR_CLK_PHY	GDDR_D_1_CLK	FB_D1_CLK_P	NO_TEST=TRUE	85 89
1711 GDDR_D1_CLK	GDDR_CLK_PHY	GDDR_D_1_CLK	FB_D1_CLK_N	NO_TEST=TRUE	85 89
Data					
1713 GDDR_D0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<7..0>	NO_TEST=TRUE	85 89
1714 GDDR_D0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<15..8>	NO_TEST=TRUE	85 89
1715 GDDR_D0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<23..16>	NO_TEST=TRUE	85 89
1716 GDDR_D0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_D_0_DQ	FB_D0_DQ<31..24>	NO_TEST=TRUE	85 89
1718 GDDR_D1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<7..0>	NO_TEST=TRUE	85 89
1719 GDDR_D1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<15..8>	NO_TEST=TRUE	85 89
1717 GDDR_D1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<23..16>	NO_TEST=TRUE	85 89
1720 GDDR_D1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_D_1_DQ	FB_D1_DQ<31..24>	NO_TEST=TRUE	85 89
Error Detection					
1720 GDDR_D0_EDC0	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<0>	NO_TEST=TRUE	85 89
1721 GDDR_D0_EDC1	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<1>	NO_TEST=TRUE	85 89
1722 GDDR_D0_EDC2	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<2>	NO_TEST=TRUE	85 89
1723 GDDR_D0_EDC3	GDDR_EDC_PHY	GDDR_D_0_EDC	FB_D0_EDC<3>	NO_TEST=TRUE	85 89
1725 GDDR_D1_EDC0	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<0>	NO_TEST=TRUE	85 89
1724 GDDR_D1_EDC1	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<1>	NO_TEST=TRUE	85 89
1726 GDDR_D1_EDC2	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<2>	NO_TEST=TRUE	85 89
1727 GDDR_D1_EDC3	GDDR_EDC_PHY	GDDR_D_1_EDC	FB_D1_EDC<3>	NO_TEST=TRUE	85 89
Data Dynamic Bus Inv					
1730 GDDR_D0_DBI0	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<0>	NO_TEST=TRUE	85 89
1731 GDDR_D0_DBI1	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<1>	NO_TEST=TRUE	85 89
1732 GDDR_D0_DBI2	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<2>	NO_TEST=TRUE	85 89
1733 GDDR_D0_DBI3	GDDR_DBI_PHY	GDDR_D_0_DBI	FB_D0_DBI_L<3>	NO_TEST=TRUE	85 89
1735 GDDR_D1_DBI0	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<0>	NO_TEST=TRUE	85 89
1734 GDDR_D1_DBI1	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<1>	NO_TEST=TRUE	85 89
1736 GDDR_D1_DBI2	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<2>	NO_TEST=TRUE	85 89
1737 GDDR_D1_DBI3	GDDR_DBI_PHY	GDDR_D_1_DBI	FB_D1_DBI_L<3>	NO_TEST=TRUE	85 89
Forwarded Clock					
1738 GDDR_D0_WCK0	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_P<0>	NO_TEST=TRUE	85 89
1739 GDDR_D0_WCK0	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_N<0>	NO_TEST=TRUE	85 89
1740 GDDR_D0_WCK1	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_P<1>	NO_TEST=TRUE	85 89
1741 GDDR_D0_WCK1	GDDR_WCK_PHY	GDDR_D_0_WCK	FB_D0_WCLK_N<1>	NO_TEST=TRUE	85 89
1742 GDDR_D1_WCK0	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_P<0>	NO_TEST=TRUE	85 89
1743 GDDR_D1_WCK0	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_N<0>	NO_TEST=TRUE	85 89
1745 GDDR_D1_WCK1	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_P<1>	NO_TEST=TRUE	85 89
1744 GDDR_D1_WCK1	GDDR_WCK_PHY	GDDR_D_1_WCK	FB_D1_WCLK_N<1>	NO_TEST=TRUE	85 89

SYNC_MASTER=D8_MLB SYNC_DATE=12/20/2011

PAGE TITLE
GDDR5 FB C/D CONSTRAINTS

Apple Inc.

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions

BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	1.00MM	1000

Constraints

BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

BKLT MISCELLANEOUS

Electrical Contraint Set	Physical	Spacing		
SPI				
J56	SMB_PHY	SMB	SMB_PCH_BLC_SCL	50 80
J56	SMB_PHY	SMB	SMB_PCH_BLC_SDA	50 80
J81	SMB_PHY	SMB	SMB_TCON_BLC_SCL	50 80
J81	SMB_PHY	SMB	SMB_TCON_BLC_SDA	50 80
12M REFERENCE CRYSTAL				
J84	CLK_XTAL	XTAL	BLC_MCU_XTAL_IN	80
J84	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT	80
J84	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT_R	80
250K REFERENCE CLOCKS				
J84	CLK_PCH_50S	CLK_PCH	STRCLK_R1	80 81
J84	CLK_PCH_50S	CLK_PCH	LED_DRVR_CLK	81

Input Bus	Physical	Spacing	Voltage	DIDT	NO_TEST		
J46	POWER_PHY	POWER	12V			PP12V_S0_BLC_VIN2	80 81 82
J72	POWER_PHY	POWER	12V			PP12V_S0_BLC_VINP	80 82
J68	POWER_PHY	POWER	14V			PRE_REG_OUT	80 81
J87	POWER_PHY	POWER	3.3V			BLC_P3V3S	80 82
J87	POWER_PHY	POWER	3.3V			BLC_P3V3_REF	80 82
J88	POWER_PHY	POWER	3.3V			BLC_P3V3	
J45	POWER_PHY	POWER	3.3V			PP3V3_S0_BLC_R	80
J41	POWER_PHY	POWER	8V			SPTX_VIN	81
J40	POWER_PHY	POWER	8V			PP8V_BLC	80 81
J47	POWER_PHY	POWER	8V			BLC_VIN2	81 82
J62	POWER_PHY	POWER	14V			BOOST_FET_DRAIN	80
J63	POWER_PHY	POWER	12V			BOOST_VDD	80
J65	POWER_PHY	POWER	5V			PP5V_S0_BLC_R	80 81 82
J66	POWER_PHY	POWER	12V			PP12V_S0_BLC_F	82
Local Ground							
J43	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_1	81 82
J64	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_2	81 82
J85	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_3	81 82
J44	GND_PHY	GND	0V			AGND_BLC	81 82
Backlight							
J55	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1	81
J56	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1_R	81
J76	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2	81
J77	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2_R	81
J86	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3	81
J78	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3_R	81
J95	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_1	81
J94	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_2	81
J96	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_3	81
J51	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS1	81
J50	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS2	81
J52	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS3	81
J75	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C1	81
J74	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C2	81
J73	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C3	81
J53	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_1	81
J54	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_2	81
J41	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_3	81
J48	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK1	81
J49	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK2	81
J50	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK3	81
J53	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1_R	80 81
J54	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2_R	80 81
J67	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3_R	80 81
J40	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1	81 82
J59	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2	81 82
J58	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3	81 82
J42	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF1	81 82
J43	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF2	81 82
J61	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF3	81 82
J46	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP1	81
J45	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP2	81
J71	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP3	81
J69	BLC_CTL_PHY	BLC_CTL				BCOMP1	81
J70	BLC_CTL_PHY	BLC_CTL				BCOMP2	81
J60	BLC_CTL_PHY	BLC_CTL				BCOMP3	81
J44	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT1	81
J47	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT2	81
J48	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT3	81
J83	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_1	81
J82	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_2	81
J80	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_3	81
J66	BLC_CTL_PHY	BLC_CTL				PRE_REG_OUT_R	80
J55	BLC_CTL_PHY	BLC_CTL				BOOST_FB	80
J54	BLC_CTL_PHY	BLC_CTL				BOOST_COMP	80
J57	BLC_CTL_PHY	BLC_CTL				BOOST_COMP_C	80
J60	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV	80
J61	BLC_CTL_PHY	BLC_CTL			TRUE	BOOST_GDRV_R	80
J65	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS	80
J38	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS_R	80
J52	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_1	81
J53	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_2	81
J54	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_3	81
OUTPUT BUS							
J49	POWER_BLC_RET	BLC_HV	80V			IS1_BLC_F	82
J48	POWER_BLC_RET	BLC_HV	80V			IS2_BLC_F	82
J50	POWER_BLC_RET	BLC_HV	80V			IS3_BLC_F	82
J43	POWER_BLC_RET	BLC_HV	80V			IS1_BLC	81 82
J72	POWER_BLC_RET	BLC_HV	80V			IS2_BLC	81 82
J75	POWER_BLC_RET	BLC_HV	80V			IS3_BLC	81 82
J78	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_1	82
J79	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_1	82
J84	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_2	82
J85	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_2	82
J86	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_3	82
J87	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_3	82
J62	POWER_BLC	BLC_HV	80V			BLC_VOUT1	81 82
J63	POWER_BLC	BLC_HV	80V			BLC_VOUT2	81 82
J63	POWER_BLC	BLC_HV	80V			BLC_VOUT3	81 82

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BLC Constraints

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GPU CORE PHASES

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
1B0	POWER_PHY	POWER	12V			PP12V_S0_GPUCORE_FLT 96 97 98
1B1	POWER_PHY	POWER	5V			PP5V_S0_GPU_VCORE_VCC 96
Local Ground						
1AP0	GND_PHY	GND	0V			AGND_GPU 96
Phase 1						
1B0A	POWER_PHY	POWER	12V			REG_LVCC_UB510 97
1AE0	POWER_PHY	POWER	12V			REG_UVCC_UB510 97
1B0K	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_1 96 97
1B0B	VR_CTL_PHY	VR_CTL				VR_GPU_PWM1_R 96
1B0V	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1 97
1B0R	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1 97
1B0C	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC 97
1B0E	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1 97
1B0Y	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_1 97
1B0Z	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_1 97
1B0X	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_1 97
1B0M ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_P 96 97
1B0N ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_N 96 97
1B46 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_P 96
1B4G ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_N 96
1B4B ISNS_GPU_CORE		SENSE				VR_GPU_ISNS1_RR_2 96
Phase 2						
1B1B	POWER_PHY	POWER	12V			REG_LVCC_UB530 97
1B1K	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_2 96 97
1B1C	VR_CTL_PHY	VR_CTL				VR_GPU_PWM2_R 96
1B1V	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2 97
1B1R	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2 97
1B1C	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC 97
1B1E	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2 97
1B1Y	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_2 97
1B1Z	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_2 97
1B1X	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_2 97
1B1M ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_P 96 97
1B1N ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_N 96 97
1B46 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_P 96
1B4H ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_N 96
1B4C ISNS_GPU_CORE		SENSE				VR_GPU_ISNS2_RR_2 96
Phase 3						
1B4D	POWER_PHY	POWER	12V			REG_VCC_UB550 97
1B4F	POWER_PHY	POWER	12V			REG_UVCC_UB550 97
1B4G	POWER_PHY	POWER	12V			REG_LVCC_UB550 97
1B4K	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_3 96 97
1B4L	VR_CTL_PHY	VR_CTL				VR_GPU_PWM3_R 96
1B4V	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_3 97
1B4R	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_3 97
1B4C	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_3_RC 97
1B4E	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_3 97
1B4Y	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_3 97
1B4Z	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_3 97
1B4X	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_3 97
1B4M ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_P 96 97
1B4N ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_N 96 97
1B56 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_P 96
1B5G ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_N 96
1B5B ISNS_GPU_CORE		SENSE				VR_GPU_ISNS3_RR_2 96
Phase 4						
1B5D	POWER_PHY	POWER	12V			REG_LVCC_UB650 98
1B5K	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_4 96 98
1B5C	VR_CTL_PHY	VR_CTL				VR_GPU_PWM4_R 96
1B5V	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_4 98
1B5R	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_4 98
1B5C	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_4_RC 98
1B5E	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_4 98
1B5Y	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_4 98
1B5Z	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_4 98
1B5X	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_4 98
1B5M ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_P 96 98
1B5N ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_N 96 98
1B66 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_P 96
1B6H ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_N 96
1B6C ISNS_GPU_CORE		SENSE				VR_GPU_ISNS4_RR_2 96

GPU CORE CONTROLLER

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
ISL6334						
1B4A	VR_CTL_PHY	VR_CTL				VR_GPU_COMP 96
1B3G	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_R 96
1B3H	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_RC 96
1B3K	VR_CTL_PHY	VR_CTL				VR_GPU_FB 96
1B3J	VR_CTL_PHY	VR_CTL				VR_GPU_FB_R 96
1B3F	VR_CTL_PHY	VR_CTL				VR_GPU_VDIFF 96
1B3C	VR_CTL_PHY	VR_CTL				VR_VDF_R1 96
1B3D	VR_CTL_PHY	VR_CTL				VR_VDF_R2 96
1B3E	VR_CTL_PHY	VR_CTL				VR_GPU_TCOMP 96
1B3B	VR_CTL_PHY	VR_CTL				VR_GPU_OFS 96
1B4P	VR_CTL_PHY	VR_CTL				VR_GPU_FS 96
1B4J		VR_CTL				VR_GPU_EN_VTT 96
1B4T		VR_CTL				PM_EN_REG_GPUCORE_S0 64 96
1B4U		VR_CTL				PM_PGOOD_REG_GPUCORE_S0 5 64 96
1B4W		VR_CTL				GPU_PSI_L 91 96
1B4X	VR_CTL_PHY	VR_CTL				VR_GPU_IOUT
1B4Y	VR_CTL_PHY	VR_CTL				VR_GPU_IMON 51 96 115
1B4Z	VR_CTL_PHY	VR_CTL				VR_GPU_FAN 96 115
1B4R		VR_CTL				VR_GPU_VRDHOT 96
1B4V		VR_CTL				VR_GPU_EN_PWR
1B4S	VR_CTL_PHY	VR_CTL				VR_GPU_SS 96
1B4B	VR_CTL_PHY	VR_CTL				VR_GPU_DAC 96
1B4C	VR_CTL_PHY	VR_CTL				VR_GPU_REF 96
1B4D	VR_CTL_PHY	VR_CTL				VR_GPU_TM 96
1B4E	VR_CTL_PHY	VR_CTL				VR_GPU_IMON 51 96 115
1B4F	VR_CTL_PHY	VR_CTL				VR_GPU_FAN 96 115
1B4G	VR_CTL_PHY	VR_CTL				VR_GPU_VRHOT
1B4H		VR_CTL				GPU_PSI_R
1B4K		VR_CTL				GPU_PSI_L_R 91
1B4L	VR_CTL_PHY	VR_CTL				VR_GPU_IMON_R 96
1B3T VSNS_GPU_VDD	SNS_DIFF_PHY	SENSE				VSNS_GPU_VDD 93 96
1B3U VSNS_GPU_VSS	SNS_DIFF_PHY	SENSE				VSNS_GPU_VSS 93 96
1B3V	SNS_DIFF_PHY	SENSE				VR_GPU_VSEN 96
1B3W	SNS_DIFF_PHY	SENSE				VR_GPU_RGND 96
GPU VIDS						
1B4N		VR_VID				REG_GPUCORE_VID7 91 96
1B4P		VR_VID				REG_GPUCORE_VID6 91 96
1B4R		VR_VID				REG_GPUCORE_VID5 91 96
1B4T		VR_VID				REG_GPUCORE_VID4 91 96
1B4U		VR_VID				REG_GPUCORE_VID3 91 96
1B4V		VR_VID				REG_GPUCORE_VID2 91 96
1B4W		VR_VID				REG_GPUCORE_VID1 91 96
1B4X		VR_VID				REG_GPUCORE_VID0 96
1B4M		VR_VID				GPU_VCORE_VID6 91
1B4N		VR_VID				GPU_VCORE_VID5 91
1B4P		VR_VID				GPU_VCORE_VID4 91
1B4R		VR_VID				GPU_VCORE_VID3 91
1B4T		VR_VID				GPU_VCORE_VID2 91
1B4U		VR_VID				GPU_VCORE_VID1 91
1B4V		VR_VID				GPU_VCORE_VID0 91
Output Bus						
1B4Q	POWER_PHY	POWER	0.9V			PPVCORE_S0_GPU 6

GPU FBVDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
1B4A	POWER_PHY	POWER	5V			REG_VCC_UB750 99
1B4A	POWER_PHY	POWER	5V			REG_PVCC_UB750 99
Local Ground						
1B4A	GND_PHY	GND	0V			AGND_FBVDDQ 99
FBVDDQ						
1B4A	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_FBVDDQ 99
1B4A	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_FBVDDQ 99
1B4A	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_FBVDDQ_RC 99
1B4A	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ 99
1B4A	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ_R
1B4A	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_FBVDDQ 99
1B4A	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_FBVDDQ 99
1B4A		SENSE				VSNS_FBVDDQ 94
1B4A ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_P 94 99
1B4A ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_N 94 99
1B4A ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_FBVDDQ_XW_P 99
1B4A ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_FBVDDQ_XW_N 99
1B4A		SENSE				FBVDDQ_SENSE_R 94
1B4A	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_OCSET
1B4A	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_VO 99
1B4A		SENSE				REG_FBVDDQ_FB 99
1B4A		SENSE				REG_FBVDDQ_RTN 99
Output Bus						
1B4A	POWER_PHY	POWER	1.5V			PP1V5R1V35_S0_GPU_REG 6 99

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Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S

CIV-specific Spacing Definitions
Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints
Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
ENET_DIFF	*	*	ENET_DIFF_ISO	
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF	
ENET_TRANS	*	*	ENET_TRANS_ISO	2 kV isolation
COMP_ENET	*	*	COMP_ENET_ISO	
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF	

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

VENI, VIDI, VICI!

Electrical Contraint Set	Physical	Spacing		
Ethernet				
J47G ENET_MDI_NORM	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>	39 40
J47G ENET_MDI_NORM	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>	39 40
J47G	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>	40
J47G	ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>	40
J46D		ENET_TRANS	ENETCONN_MCT3	40
J46D		ENET_TRANS	ENETCONN_MCT2	40
J46D		ENET_TRANS	ENETCONN_MCT1	40
J46D		ENET_TRANS	ENETCONN_MCT0	40
J47G	ENET_COMP_PHY	COMP_ENET	ENET_RDAC	39
SD				
J47G SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0> NO_TEST=TRUE	39
J48B	SD_PHY	SD	SDCONN_DATA<7..0>	39 41
J49G	SD_PHY	SD	SDCONN_DATA_R<7..0> NO_TEST=TRUE	41
J48F SD_CMD	SD_PHY	SD	ENET_SD_CMD NO_TEST=TRUE	39
J48F	SD_PHY	SD	SDCONN_CMD NO_TEST=TRUE	39 41
J49G	SD_PHY	SD	SDCONN_CMD_R NO_TEST=TRUE	41
J48B SD_CLK	SD_PHY	SD	ENET_SD_CLK NO_TEST=TRUE	39
J48B	SD_PHY	SD	SDCONN_CLK NO_TEST=TRUE	39 41
J48B	SD_PHY	SD	SDCONN_CLK_R NO_TEST=TRUE	41
J48B	SD_PHY	SD	ENET_MEDIA_SENSE	15 18 39
J48B	SD_PHY	SD	ENET_SD_DETECT_L	39 41
J48F	SD_PHY	SD	SDCONN_WP	39 41
CIV SPI				
J49K	SPI_50S	SPI	ENET_SCLK	39
J48K	SPI_50S	SPI	ENET_MISO	39
J49J	SPI_50S	SPI	ENET_MOSI	39
J49J	SPI_50S	SPI	ENET_CS_L	39

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4V5_*

	Physical	Spacing	Netname	
I1		PM	4V5_REG_EN	56
I2	POWER_PHY	POWER	4V5_REG_IN	56

ACDC_*

	Spacing	Netname	
I4	PM	ACDC_BURST_EN	48
I5	PM	ACDC_BURST_EN_L	48

ALL_*

	Spacing	Netname	
I6	PM	ALL_SYS_PWRGD	5 47 65

AP_*

	Spacing	Netname	
I6	GENERIC_ISO	AP_CLKREQ_L	15 21
I7	GENERIC_ISO	AP_CLKREQ_L_ISO	15 35
I8	GENERIC_ISO	AP_CLKREQ_Q_L	35
I9	GENERIC_ISO	AP_EVENT_L	35 47 48
I10	GENERIC_ISO	AP_PWR_EN_ISO	15 35
I11	PM	AP_RESET_CONN_L	35
I12	PM	AP_RESET_L	26 35
I13	PM	AP_WAKE_L	35

BLC12V_*

	Spacing	Netname
I14	PM	BLC12V_FAULT
I15	PM	BLC12V_FAULT_L
I16	PM	BLC12V_UVLO
I17	PM	BLC12V_UVLO_OUT
I18	PM	BLC12V_UVLO_REF

BLC_*

	Physical	Spacing	Voltage	Netname	
I19		GENERIC_ISO		BLC_BL	80 82
I20		GENERIC_ISO		BLC_BL_GATE	82
I21		GENERIC_ISO		BLC_BST	80 82
I22		GENERIC_ISO		BLC_BST_R	80
I23		GENERIC_ISO		BLC_BYPASS_GATE	82
I24		GENERIC_ISO		BLC_DIM_MCU	80
I25		PM		BLC_EN	78 80 81
I26		GENERIC_ISO		BLC_ENA	80
I27		GENERIC_ISO		BLC_ENA1	80 82
I28		PM		BLC_EN_DELAY	78
I29		PM		BLC_EN_R	80

BLC_*

	Physical	Spacing	Voltage	Netname	
I30		PM		BLC_EXT_BOOT	48 80
I31		PM		BLC_EXT_BOOT_L	80
I32	BLC_CTL_PHY	BLC_CTL	5V	BLC_MCU_AOUT_R	82
I33		GENERIC_ISO		BLC_MCU_BV	80 82
I34		GENERIC_ISO		BLC_MCU_BV_D	82
I35		GENERIC_ISO		BLC_MCU_BV_R	82
I36	SMB_PHY	SMB		BLC_MCU_B_SDA_CONN	80
I37		GENERIC_ISO		BLC_MCU_FLAG_V	80
I38		GENERIC_ISO		BLC_MCU_PWM5	80
I39		GENERIC_ISO		BLC_MCU_PWM5_R	80
I40		PM		BLC_MCU_RESET	80
I41		PM		BLC_MCU_RESET_L	80
I42		PM		BLC_MCU_RESET_R_L	80
I43	XDP_PHY	CLK_JTAG		BLC_MCU_RTCK	80
I44		GENERIC_ISO		BLC_MCU_RXD0	80
I45	XDP_PHY	XDP		BLC_MCU_TCK	80
I46	XDP_PHY	XDP		BLC_MCU_TDI	80
I47	XDP_PHY	XDP		BLC_MCU_TDO	80
I48	XDP_PHY	XDP		BLC_MCU_TMS	80
I49	XDP_PHY	XDP		BLC_MCU_TRST	80
I50	XDP_PHY	XDP		BLC_MCU_TXD0	80
I51		GENERIC_ISO		BLC_MCU_UVLO	80
I52		GENERIC_ISO		BLC_ON	82
I53		GENERIC_ISO		BLC_ON_DRAIN	82
I54		GENERIC_ISO		BLC_ON_R	82
I55		GENERIC_ISO		BLC_P_ON	80 81 82
I56		GENERIC_ISO		BLC_P_ON_BYPASS	82
I57		GENERIC_ISO		BLC_P_ON_D	82
I58		GENERIC_ISO		BLC_P_ON_DRAIN	82
I59		GENERIC_ISO		BLC_P_ON_D_R	82
I60		GENERIC_ISO		BLC_P_ON_GATE	82
I61		GENERIC_ISO		BLC_P_ON_R	82
I62		GENERIC_ISO		BLC_SKIP	81
I63		GENERIC_ISO		BLC_SNUB_1	81
I64		GENERIC_ISO		BLC_SNUB_2	81
I65		GENERIC_ISO		BLC_SNUB_3	81
I66		GENERIC_ISO		BLC_UVLO	80 82
I67		GENERIC_ISO		BLC_VIN2_GATE	82
I68		GENERIC_ISO		BLC_VIN2_SRC	82
I69		GENERIC_ISO		BLC_VINP_GATE	82
I70		GENERIC_ISO		BLC_VIN_SNS	81
I71		GENERIC_ISO		BLC_VSYNC	78 80
I72		GENERIC_ISO		BLC_VSYNC_R	80

BOOST_*

	Spacing	Netname	
I73	GENERIC_ISO	BOOST_BP	80
I74	GENERIC_ISO	BOOST_BYPASS	80 82
I75	GENERIC_ISO	BOOST_BYPASS_GATE	80
I76	PM	BOOST_EN_GATE	80
I77	PM	BOOST_EN_L	80
I78	GENERIC_ISO	BOOST_RC	80
I79	GENERIC_ISO	BOOST_SS	80

BT_*

	Spacing	Netname	
I80	PM	BT_PWR_EN	35
I81	PM	BT_PWR_RST_L	15 20 35
I82	PM	BT_PWR_RST_L_Q	35

BURSTMODE_*

	Spacing	Netname	
I83	PM	BURSTMODE_EN	71
I84	PM	BURSTMODE_EN_L	6 48 71

CAM_*

	Spacing	Netname	
I85	PM	CAM_EXT_BOOT	42 43
I86	PM	CAM_PROC_RESET	43
I87	PM	CAM_PROC_RESET_L	42 43

CPU_*

	Physical	Spacing	Netname	
I88		PM	CPU_PWRGD_1V05_R	28
I89		PM	CPU_PWRGD_3V3	28
I90		PM	CPU_PWRGD_3V3_R	28
I91		GENERIC_ISO	CPU_SKTOCC	64
I92	CPU_PHY	CPU	CPU_THRMTRIP_3V3	47 48
I93	CPU_PHY	CPU	CPU_THRMTRIP_R_L	48

DEBUG_*

	Spacing	Netname	
I94	PM	DEBUG_RESET_L	26 49

DP_*

	Physical	Spacing	Netname	
I95		PM	DP_AUXIO_EN	15 77 79
I96		PM	DP_GPU_MUX_EN	75
I97		GENERIC_ISO	DP_INTPNL_HPD	75 78
I98		GENERIC_ISO	DP_INT_EG_HPD	75 90
I99	TBT_GEN_5SS	TBT_GEN	DP_TBTPA_DDC_CLK	76 77
I100	TBT_GEN_5SS	TBT_GEN	DP_TBTPA_DDC_DATA	76 77
I101		GENERIC_ISO	DP_TBTPA_HPD	36 77
I102	TBT_GEN_5SS	TBT_GEN	DP_TBTPB_DDC_CLK	76 79
I103	TBT_GEN_5SS	TBT_GEN	DP_TBTPB_DDC_DATA	76 79
I104		GENERIC_ISO	DP_TBTPB_HPD	36 79

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ENETCONN_*

	Spacing	Netname	
I1	GENERIC_ISO	ENETCONN_TCT	40

ENET_*

	Physical	Spacing	Netname	
I2		GENERIC_ISO	ENET_ACT	40
I3		GENERIC_ISO	ENET_ASF_GPIO	47 48
I4		GENERIC_ISO	ENET_CLKREQ_L	15 18 40
I5		PM	ENET_CLKREQ_L_Q	39 40
I6		PM	ENET_CR_1V8_EN	
I7		PM	ENET_CR_1V8_EN_R	
I8		PM	ENET_CR_3V3_EN_L	
I9		PM	ENET_CR_3V3_EN_L_R	
I10		PM	ENET_CR_PWREN	39 41
I11	XDP_PHY	XDP	ENET_LOW_PWR	26 39 41
I12		PM	ENET_PWR_EN_L	40
I13		PM	ENET_PWR_EN_L_R	40
I14		PM	ENET_RESET_L	39 41
I15		PM	ENET_SD_RESET_L	26 41
I16		GENERIC_ISO	ENET_SR_DISABLE	39
I17		GENERIC_ISO	ENET_SR_LX	39 40
I18		PM	ENET_WAKE_L	40

FAN_*

	Spacing	Netname	
I19	GENERIC_ISO	FAN_0_PWM_FET	54
I20	GENERIC_ISO	FAN_0_PWM_FILT	54
I21	GENERIC_ISO	FAN_0_TACH_FET	54
I22	GENERIC_ISO	FAN_0_TACH_FILT	54

FBVDD_*

	Spacing	Netname	
I23	GENERIC_ISO	FBVDD_ALTVO	91 99

FB_*

	Spacing	Netname	
I24	GENERIC_ISO	FB_A0_VREFC	86
I25	GENERIC_ISO	FB_A0_VREFD	86
I26	GENERIC_ISO	FB_A1_VREFC	86
I27	GENERIC_ISO	FB_A1_VREFD	86
I28	GENERIC_ISO	FB_B0_VREFC	87
I29	GENERIC_ISO	FB_B0_VREFD	87
I30	GENERIC_ISO	FB_B1_VREFC	87
I31	GENERIC_ISO	FB_B1_VREFD	87
I32	GENERIC_ISO	FB_C0_VREFC	88
I33	GENERIC_ISO	FB_C0_VREFD	88
I34	GENERIC_ISO	FB_C1_VREFC	88
I35	GENERIC_ISO	FB_C1_VREFD	88
I36	GENERIC_ISO	FB_D0_VREFC	89
I37	GENERIC_ISO	FB_D0_VREFD	89
I38	GENERIC_ISO	FB_D1_VREFC	89
I39	GENERIC_ISO	FB_D1_VREFD	89
I40	GENERIC_ISO	FB_SW_LEG_A	84 86

FB_*

	Spacing	Netname	
I41	GENERIC_ISO	FB_SW_LEG_B	84 87
I42	GENERIC_ISO	FB_SW_LEG_C	85 88
I43	GENERIC_ISO	FB_SW_LEG_D	85 89
I44	GENERIC_ISO	FB_VREF_GPU	94

FET_*

	Physical	Spacing	Voltage	Netname	
I45		GENERIC_ISO		FET_EN_P12V_S0	74
I46		GENERIC_ISO		FET_EN_P12V_S0_BLC	74
I47		GENERIC_ISO		FET_EN_P12V_S0_BLC_R	74
I48		GENERIC_ISO		FET_EN_P12V_S0_R	74
I49		GENERIC_ISO		FET_EN_P12V_S5	74
I50		GENERIC_ISO		FET_EN_P12V_S5_R	74
I51		GENERIC_ISO		FET_EN_VDDQ_S0	74
I52		GENERIC_ISO		FET_HDD_SLGSW	52
I53	POWER_PHY	POWER	12V	FET_VCC_U7950	74
I54	POWER_PHY	POWER	12V	FET_VCC_U7970	74
I55	POWER_PHY	POWER	12V	FET_VCC_U7980	74

FLAG_*

	Spacing	Netname	
I56	GENERIC_ISO	FLAG_V	80 81 82

G3_*

	Spacing	Netname	
I57	GENERIC_ISO	G3_POWERON_L	47 48

GND_*

	Spacing	Netname	
I58	SENSE	GND_SMC_AVSS	47 48 51 55

GPU_*

	Physical	Spacing	Netname	
I59		GENERIC_ISO	GPU_ALT_VREF	84 85 91
I60		GENERIC_ISO	GPU_BUFRSTN	91
I61		GENERIC_ISO	GPU_IFPAB_PLLVDD	90
I62		GENERIC_ISO	GPU_IFPA_IOVDD	90
I63		GENERIC_ISO	GPU_IFPB_IOVDD	90
I64		GENERIC_ISO	GPU_IFPC_IOVDD	90
I65		GENERIC_ISO	GPU_IFPC_PLLVDD	90
I66	XDP_PHY	XDP	GPU_JTAG_TDI	91
I67	XDP_PHY	XDP	GPU_JTAG_TDO	91
I68	XDP_PHY	XDP	GPU_JTAG_TMS	91
I69	XDP_PHY	XDP	GPU_JTAG_TRST_L	91
I70		GENERIC_ISO	GPU_MLS_STRAP0	91
I71		GENERIC_ISO	GPU_MLS_STRAP1	91

GPU_*

	Physical	Spacing	Netname	
I72		GENERIC_ISO	GPU_MLS_STRAP2	91
I73		GENERIC_ISO	GPU_MLS_STRAP3	91
I74		GENERIC_ISO	GPU_MLS_STRAP4	91
I75		GENERIC_ISO	GPU_RESET_L	26 83 91
I76	SPI_50S	SPI	GPU_ROM_CS_L	91
I77	SPI_50S	SPI	GPU_ROM_CS_L_R	91
I78		GENERIC_ISO	GPU_ROM_HOLD_L	91
I79	SPI_50S	SPI	GPU_ROM_SI	91
I80	SPI_50S	SPI	GPU_ROM_SI_R	91
I81	SPI_50S	SPI	GPU_ROM_SO	91
I82	SPI_50S	SPI	GPU_ROM_SO_R	91
I83	SPI_50S	SPI	GPU_ROM_WP_L	91

HDD_*

	Spacing	Netname	
I84	GENERIC_ISO	HDD_12V_S0_GATE	52
I85	GENERIC_ISO	HDD_OOB_1V00_REF	52
I86	PM	HDD_PWR_EN	21 52
I87	GENERIC_ISO	HDD_PWR_EN_L	52
I88	GENERIC_ISO	HDD_PWR_EN_R	52

I2C_*

	Physical	Spacing	Netname	
I89	SMB_PHY	SMB	I2C_TCON_MAS_SCL	50 78
I90	SMB_PHY	SMB	I2C_TCON_MAS_SDA	50 78

IFPD_*

	Spacing	Netname	
I91	GENERIC_ISO	IFPD_RSET	90

IFPEF_*

	Spacing	Netname	
I92	GENERIC_ISO	IFPEF_RSET	90

ISNSA_*

	Electrical	Physical	Spacing	Netname	
I93	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VG3H_N	51
I94	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VG3H_P	51
I95	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_P1V05_N	55
I96	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_P1V05_P	55
I97	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_VCCSA_N	55
I98	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_VCCSA_P	55
I99	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_FBVDDQ_N	51
I100	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_FBVDDQ_P	51
I101	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_HDD_N	51
I102	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_HDD_P	51

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ISNSA_*

	Electrical	Physical	Spacing	Netname	
I1	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_P1V05_N	55
I2	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_P1V05_P	55
I3	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V05S0_PCH_N	51
I4	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V05S0_PCH_P	51
I5	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V5S0_CPU_MEM_N	51
I6	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V5S0_CPU_MEM_P	51
I7	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S0_SSD_N	51
I8	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S0_SSD_P	51
I9	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S4_AP_N	55
I10	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S4_AP_P	55
I11	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P5VS0_HDD_N	51
I12	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P5VS0_HDD_P	51
I13	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_PVDDQS3_DDR_N	51
I14	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_PVDDQS3_DDR_P	51

ISNS_*

	Physical	Spacing	Netname	
I15	SNS_PHY	SENSE	ISNS_CPUAXG_FB	51
I16	SNS_PHY	SENSE	ISNS_CPUAXG_N	51
I17	SNS_PHY	SENSE	ISNS_CPUAXG_P	51
I18	SNS_PHY	SENSE	ISNS_CPUCORE_FB	51
I19	SNS_PHY	SENSE	ISNS_CPUCORE_N	51
I20	SNS_PHY	SENSE	ISNS_CPUCORE_P	51
I21	SNS_PHY	SENSE	ISNS_GPUCORE_FB	51
I22	SNS_PHY	SENSE	ISNS_GPUCORE_N	51
I23	SNS_PHY	SENSE	ISNS_GPUCORE_P	51
I24	SNS_PHY	SENSE	ISNS_P12VG3H_R	51
I25	SNS_PHY	SENSE	ISNS_P12VS0_CPU_P1V05_R	55
I26	SNS_PHY	SENSE	ISNS_P12VS0_CPU_VCCSA_R	55
I27	SNS_PHY	SENSE	ISNS_P12VS0_FBVDDQ_R	51
I28	SNS_PHY	SENSE	ISNS_P12VS0_HDD_R	51
I29	SNS_PHY	SENSE	ISNS_P12VS0_P1V05_R	55
I30	SNS_PHY	SENSE	ISNS_P1V05S0_PCH_R	51
I31	SNS_PHY	SENSE	ISNS_P1V5S0_CPU_MEM_R	51
I32	SNS_PHY	SENSE	ISNS_P3V3S0_SSD_R	51
I33	SNS_PHY	SENSE	ISNS_P3V3S4_AP_R	55
I34	SNS_PHY	SENSE	ISNS_P5VS0_HDD_R	51
I35	SNS_PHY	SENSE	ISNS_PVDDQS3_DDR_R	51

ISOLATE_*

	Spacing	Netname	
I36	PM	ISOLATE_CPU_MEM_5V	28
I37	PM	ISOLATE_CPU_MEM_5V_L	28

JTAG_*

	Physical	Spacing	Netname	
I38	XDP_PHY	XDP	JTAG_GMUX_TMS	20
I39	XDP_PHY	XDP	JTAG_TBT_TDI	15 21
I40	XDP_PHY	XDP	JTAG_TBT_TDI_ISOL	15 36
I41	XDP_PHY	XDP	JTAG_TBT_TDO	15 21
I42	XDP_PHY	XDP	JTAG_TBT_TDO_ISOL	15 36
I43	XDP_PHY	XDP	JTAG_TBT_TMS	15 18
I44	XDP_PHY	XDP	JTAG_TBT_TMS_ISOL	15 36

LED_*

	Spacing	Netname	
I45	PM	LED_DRIVER_EN	81 82
I46	PM	LED_DRIVER_EN_L	82
I47	PM	LED_DRIVER_EN_L_R	82
I48	GENERIC_ISO	LED_DRIVER_OVP1	81 82
I49	GENERIC_ISO	LED_DRIVER_OVP1P	80 81
I50	GENERIC_ISO	LED_DRIVER_OVP1_OUT	81
I51	GENERIC_ISO	LED_DRIVER_OVP2	81 82
I52	GENERIC_ISO	LED_DRIVER_OVP2P	80 81
I53	GENERIC_ISO	LED_DRIVER_OVP2_OUT	81
I54	GENERIC_ISO	LED_DRIVER_OVP3	81 82
I55	GENERIC_ISO	LED_DRIVER_OVP3P	80 81
I56	GENERIC_ISO	LED_DRIVER_OVP3_OUT	81

LPCPLUS_*

	Spacing	Netname	
I57	GENERIC_ISO	LPCPLUS_GPIO	21 49

LPC_*

	Spacing	Netname	
I58	GENERIC_ISO	LPC_PWRDWN_L	19 26 47 49
I59	GENERIC_ISO	LPC_SERIRQ	18 47 49

MEMVTT_*

	Spacing	Netname	
I60	PM	MEMVTT_EN	28 64
I61	PM	MEMVTT_EN_L	28

MEM_*

	Spacing	Netname	
I62	GENERIC_ISO	MEM_EVENT_L	29 30 31 32 47 48

MOJO_*

	Physical	Spacing	Netname	
I63	XDP_PHY	XDP	MOJO_RX_L	45 47 48
I64	XDP_PHY	XDP	MOJO_TX_L	45 47 48

OCA_*

	Spacing	Netname	
I65	GENERIC_ISO	OCA_FET_DRAIN	82

OVP_*

	Spacing	Netname	
I66	GENERIC_ISO	OVP_OREF	82
I67	GENERIC_ISO	OVP_OUT1	82
I68	GENERIC_ISO	OVP_OUT1_R	82
I69	GENERIC_ISO	OVP_OUT2	82
I70	GENERIC_ISO	OVP_OUT2_R	82
I71	GENERIC_ISO	OVP_OUT3	82
I72	GENERIC_ISO	OVP_OUT3_R	82

P1V2_*

	Spacing	Netname	
I73	PM	P1V2_S4_EN	43

P1V8_*

	Spacing	Netname	
I74	PM	P1V8_S4_EN	43

P3V3AP_*

	Spacing	Netname	
I75	GENERIC_ISO	P3V3AP_VMON	35

P3V3_*

	Spacing	Netname	
I76	GENERIC_ISO	P3V3_S0_EN_G	74
I77	GENERIC_ISO	P3V3_S3_EN_G	74

P3V42G3H_*

	Spacing	Netname	
I78	GENERIC_ISO	P3V42G3H_BOOST	73

P5V_*

	Spacing	Netname	
I79	GENERIC_ISO	P5V_S0_EN_G	74

PCA9557D_*

	Spacing	Netname	
I80	GENERIC_ISO	PCA9557D_RESET_L	26 28 34

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PCH_*

	Physical	Spacing	Netname	
A1		PM	PCH_BLC_EXT_BOOT	21 80
A2		PM	PCH_BLC_EXT_BOOT_R	15 21
A3		PM	PCH_BLC_MCU_RESET	21 80
A4		PM	PCH_BLC_MCU_RESET_R	15 21
A5		PM	PCH_CAM_RESET	15 21
A6		PM	PCH_CAM_RESET_R	21 43
A7		GENERIC_ISO	PCH_DSWVRMEN	19
A8	CPU_PHY	CPU	PCH_PECI	21
A9	CPU_PHY	CPU	PCH_PROCPWRGD	21
A10		GENERIC_ISO	PCH_RCIN_L	21
A11		GENERIC_ISO	PCH_RI_L	19
A12		GENERIC_ISO	PCH_SMBALERT_L	15 18
A13		GENERIC_ISO	PCH_SRTCRST_L	18
A14		GENERIC_ISO	PCH_STRP_TOPBLK_SWP_L	20
A15		GENERIC_ISO	PCH_SUSWARN_L	15 19

PCIE_*

	Spacing	Netname	
A16	GENERIC_ISO	PCIE_CLKREQ5_GPIO44_L	18
A17	PM	PCIE_WAKE_L	19 35 40

PEG_*

	Spacing	Netname	
A18	GENERIC_ISO	PEG_CLKREQ_L	15 18 83

PGOOD_*

	Spacing	Netname	
A19	PM	PGOOD_P1V5_S0_DLY	28

PLT_*

	Spacing	Netname	
A20	PCH	PLT_RESET_L	20 26
A21	PCH	PLT_RST_BUF_L	26

PM_*

	Spacing	Netname	
A22	PM	PM_CLKRUN_L	47 48 49
A23	PM	PM_DSW_PWRGD	47 48 65
A24	PM	PM_EN_FET_P12V_S0	64 74
A25	PM	PM_EN_FET_P12V_S0_R	74
A26	PM	PM_EN_FET_P3V3_S0	64 74
A27	PM	PM_EN_FET_P3V3_S4	64 74
A28	PM	PM_EN_FET_P5V_S0	64 74
A29	PM	PM_EN_FET_VDDQ_S0	64 74
A30	PM	PM_EN_LDO_DDRVTT_S0	64 72
A31	PM	PM_EN_REG_CPUCORE_S0	64 66

PM_*

	Spacing	Netname	
A32	PM	PM_EN_REG_CPU_P1V05_S0	64 69
A33	PM	PM_EN_REG_FBVDDQ_S0	64 99
A34	PM	PM_EN_REG_GPUCORE_S0_R	96
A35	PM	PM_EN_REG_P1V05_S0	64 99
A36	PM	PM_EN_REG_P1V8_S0	64 72
A37	PM	PM_EN_REG_P3V3_S5	64 71 74
A38	PM	PM_EN_REG_P5V_S4	64 71
A39	PM	PM_EN_REG_VCCSA_S0	64 70
A40	PM	PM_EN_REG_VDDQ_S3	64 72
A41	PM	PM_EN_S0	64
A42	PM	PM_EN_S4	64
A43	PM	PM_EN_USB_PWR	45 46 64
A44	PM	PM_LED_A_ALL_SYS_PWRGD	5
A45	PM	PM_LED_A_BLC_GOOD	5
A46	PM	PM_LED_A_CPUAXG_PGOOD	5
A47	PM	PM_LED_A_GPU_GOOD	5
A48	PM	PM_LED_A_PGOOD_CPUCORE_S0	5
A49	PM	PM_LED_A_PGOOD_CPU_P1V05_S0	5
A50	PM	PM_LED_A_PGOOD_REG_FBVDDQ_S0	5
A51	PM	PM_LED_A_PGOOD_REG_GPUCORE_S0	5
A52	PM	PM_LED_A_PGOOD_REG_P1V05	5
A53	PM	PM_LED_A_PGOOD_REG_VDDQ_S3	5
A54	PM	PM_LED_A_S4	5
A55	PM	PM_LED_A_S5	5
A56	PM	PM_LED_A_SLP_S3	5
A57	PM	PM_LED_A_VIDEO_ON	5
A58	PM	PM_LED_K_ALL_SYS_PWRGD	5
A59	PM	PM_LED_K_BLC_GOOD	5
A60	PM	PM_LED_K_CPUAXG_PGOOD	5
A61	PM	PM_LED_K_GPU_GOOD	5
A62	PM	PM_LED_K_PGOOD_CPUCORE_S0	5
A63	PM	PM_LED_K_PGOOD_CPU_P1V05_S0	5
A64	PM	PM_LED_K_PGOOD_REG_FBVDDQ_S0	5
A65	PM	PM_LED_K_PGOOD_REG_GPUCORE_S0	5
A66	PM	PM_LED_K_PGOOD_REG_P1V05	5
A67	PM	PM_LED_K_PGOOD_REG_VDDQ_S3	5
A68	PM	PM_LED_K_SLP_S3	5
A69	PM	PM_MEM_PWRGD_L	28
A70	PM	PM_PCH_APWROK	19 65
A71	PM	PM_PCH_PWROK	15 19 26 35 43 65 80
A72	PM	PM_PCH_PWROK_APWROK	65
A73	PM	PM_PCH_SYS_PWROK	19 48 65
A74	PM	PM_PGOOD_FBVDDQ_VDDQ_S0	64
A75	PM	PM_PGOOD_FET_P12V_S0	74
A76	PM	PM_PGOOD_FET_P12V_S0_BLC	74 82
A77	PM	PM_PGOOD_FET_P12V_S5	74
A78	PM	PM_PGOOD_FET_P3V3_S0	64 74
A79	PM	PM_PGOOD_FET_P5V_S0	64 74
A80	PM	PM_PGOOD_FET_VDDQ_S0	28 64 74
A81	PM	PM_PGOOD_P3V3_S4_FET	27 35 64 74
A82	PM	PM_PGOOD_REG_ALL_P1V05_S0	64 65
A83	PM	PM_PGOOD_REG_ALL_P1V05_S0_R	28 64
A84	PM	PM_PGOOD_REG_CPUCORE_S0	5 25 65 66
A85	PM	PM_PGOOD_REG_CPU_P1V05_S0	5 64 69
A86	PM	PM_PGOOD_REG_FBVDDQ_S0	5 64 99
A87	PM	PM_PGOOD_REG_P1V05_S0	5 64 99
A88	PM	PM_PGOOD_REG_P1V8_S0	64 72
A89	PM	PM_PGOOD_REG_P3V3_S5	65 71
A90	PM	PM_PGOOD_REG_P5V_S4	64 71
A91	PM	PM_PGOOD_REG_VCCSA_S0	64 65 70
A92	PM	PM_PGOOD_REG_VDDQ_S3	5 64 72
A93	PM	PM_PWRBTN_L	15 19 25 47
A94	PM	PM_RSMRST_PCH_L	19 65
A95	PM	PM_RSMRST_PCH_L_R	65
A96	PM	PM_SLP_S3_L	5 15 19 28 40 47 48 64
A97	PM	PM_SLP_S4_L	15 19 47 64
A98	PM	PM_SLP_S5_L	15 19 47 64
A99	PCH	PM_SYSRST_L	19 25 26 47
A100	PCH	PM_THRMTRIP_L	21 48
A101	PM	PGOOD_P12V_S0_R	65
A102	PM	PGOOD_P12V_S0	64 65 74

PP12V_*

	Physical	Spacing	Voltage	Netname	
A103	POWER_PHY	POWER	12V	PP12V_LCD	78
A104	POWER_PHY	POWER	12V	PP12V_LCD_EXT	78
A105	POWER_PHY	POWER	12V	PP12V_S0_FAN_0_FILT	54
A106	POWER_PHY	POWER	12V	PP12V_S0_HDD_FET	44 52

PP1V05_*

	Physical	Spacing	Voltage	Netname	
A107	POWER_PHY	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	17 22
A108	POWER_PHY	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	17 22

PP1V2_*

	Physical	Spacing	Voltage	Netname	
A109	POWER_PHY	POWER	1.2V	PP1V2_ENET_INTREG	40
A110	POWER_PHY	POWER	1.2V	PP1V2_G3H_SMC_VDDC	47
A111	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_AVDDL	39
A112	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_GPHYPLL	39
A113	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_PCIEPLL	39
A114	POWER_PHY	POWER	1.2V	PP1V2_USB_HUB_CRFILT	27
A115	POWER_PHY	POWER	1.2V	PP1V2_USB_HUB_PLLFILT	27

PP1V5_*

	Physical	Spacing	Voltage	Netname	
A116	POWER_PHY	POWER	1.5V	PP1V5_S0_DP_BIAS	75

PP1V8_*

	Physical	Spacing	Voltage	Netname	
A117	POWER_PHY	POWER	1.8V	PP1V8_S0_PCH_VCCVRM_F	22 24

PP3V3R1V8_*

	Physical	Spacing	Netname	
A118	POWER_PHY	POWER	PP3V3R1V8_ENET_LR_OUT_REG	39

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PP3V3RHV_*

	Physical	Spacing	Voltage	Netname	
I34	POWER_PHY	POWER	12V	PP3V3RHV_SW_TBTAPWR	77
I35	POWER_PHY	POWER	12V	PP3V3RHV_SW_TBTBPWR	79

PPHV_*

	Physical	Spacing	Voltage	Netname	
I36	POWER_PHY	POWER	12V	PPHV_SW_TBTAPWR	77
I37	POWER_PHY	POWER	12V	PPHV_SW_TBTBPWR	79

S5_*

	Spacing	Netname	
I68	PM	S5_PWRGD	47 65

PP3V3_*

	Physical	Spacing	Voltage	Netname	
I3	POWER_PHY	POWER	3.3V	PP3V3_DMIC_CONN	42
I4	POWER_PHY	POWER	3.3V	PP3V3_G3H_AVREF_SMC	47 48
I5	POWER_PHY	POWER	3.3V	PP3V3_G3H_BT_FET	35
I6	POWER_PHY	POWER	3.3V	PP3V3_G3H_BT_FLT	35
I7	POWER_PHY	POWER	3.3V	PP3V3_G3H_SMC_USBMUX_R	45
I8	POWER_PHY	POWER	3.3V	PP3V3_G3H_SMC_VDDA	47
I9	POWER_PHY	POWER	3.3V	PP3V3_G3_RTC	6 26
I10	POWER_PHY	POWER	3.3V	PP3V3_PVDDQS3_ISNS	51
I11	POWER_PHY	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	17 22
I12	POWER_PHY	POWER	3.3V	PP3V3_S0_SSD_FLT	44
I13	POWER_PHY	POWER	3.3V	PP3V3_S0_SW_SD_PWR	41
I14	POWER_PHY	POWER	3.3V	PP3V3_S4_ALS_F	42
I15	POWER_PHY	POWER	3.3V	PP3V3_S4_AP_FET	35
I16	POWER_PHY	POWER	3.3V	PP3V3_S4_AP_FLT	35
I17	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_AVDDH	39
I18	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_BIASVDDH	39
I19	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_SRVDD	39
I20	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_XTALVDDH	39
I21	POWER_PHY	POWER	3.3V	PP3V3_S4_USB_HUB_VDD	27
I22	POWER_PHY	POWER	3.3V	PP3V3_S5_XDP_R	25

PPVBATT_*

	Physical	Spacing	Voltage	Netname	
I38	POWER_PHY	POWER	3.3V	PPVBATT_G3_RTC	26
I39	POWER_PHY	POWER	3.3V	PPVBATT_G3_RTC_R	26

SATALED_*

	Spacing	Netname	
I59	GENERIC_ISO	SATALED_L	44

PU_*

	Spacing	Netname	
I40	GENERIC_ISO	PU_U6900	64

SDCONN_*

	Spacing	Netname	
I60	GENERIC_ISO	SDCONN_DETECT	41
I61	GENERIC_ISO	SDCONN_ILIM	41
I62	GENERIC_ISO	SDCONN_OC_L	41

PWR_*

	Spacing	Netname	
I41	PM	PWR_BTN	6 48
I42	PM	PWR_BTN_R	6

SD_*

	Spacing	Netname	
I63	GENERIC_ISO	SD_DETECT_LVL	41

PP4V5_*

	Physical	Spacing	Voltage	Netname	
I23	POWER_PHY	POWER	4.5V	PP4V5_AUDIO_ANALOG	56 60 62

REG_*

	Physical	Spacing	Netname	
I43		PM	REG_CPUAXG_PGOOD	5 66
I44		PM	REG_CPUCORE_PGOOD	66
I45	CPU_PHY	CPU	REG_CPUCORE_VRHOT_L	66
I46		PM	REG_CPU_P1V05S0_PGOOD	69
I47	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET0	99
I48	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1	99
I49	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1_R	99
I50	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SREF	99
I51		PM	REG_P1V8S0_PGOOD	72
I52		PM	REG_P3V3S5_PGOOD	71
I53		PM	REG_P5VS4_PGOOD	71
I54		PM	REG_VCCSAS0_PGOOD	70
I55		PM	REG_VDDQS3_PGOOD	72

SLG_*

	Spacing	Netname	
I64	PM	SLG_ENET_RESET_L	41
I65	PM	SLG_ENET_RESET_R_L	41

PP5V_*

	Physical	Spacing	Voltage	Netname	
I24	POWER_PHY	POWER	5V	PP5V_AUDIO_HPAMP	56 57
I25	POWER_PHY	POWER	5V	PP5V_S0_HDD_FET	44 52
I26	POWER_PHY	POWER	5V	PP5V_S0_PCH_V5REF	24
I27	POWER_PHY	POWER	5V	PP5V_S4_EXTA	45
I28	POWER_PHY	POWER	5V	PP5V_S4_EXTA_F	45
I29	POWER_PHY	POWER	5V	PP5V_S4_EXTB	45
I30	POWER_PHY	POWER	5V	PP5V_S4_EXTB_F	45
I31	POWER_PHY	POWER	5V	PP5V_S4_EXTC	46
I32	POWER_PHY	POWER	5V	PP5V_S4_EXTC_F	46
I33	POWER_PHY	POWER	5V	PP5V_S4_EXTD	46
I34	POWER_PHY	POWER	5V	PP5V_S4_EXTD_F	46
I35	POWER_PHY	POWER	5V	PP5V_S5_PCH_V5REFSUS	24

SMBUS_*

	Physical	Spacing	Netname	
I66	SMB_PHY	SMB	SMBUS_PCH_CLK	18 50
I67	SMB_PHY	SMB	SMBUS_PCH_CLK_R	50
I68	SMB_PHY	SMB	SMBUS_PCH_DATA	18 50
I69	SMB_PHY	SMB	SMBUS_PCH_DATA_R	50
I70	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	47 50
I71	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	47 50
I72	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	47 50
I73	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	47 50
I74	SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL	47 50
I75	SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA	47 50
I76	SMB_PHY	SMB	SMBUS_SMC_3_SCL	47 50
I77	SMB_PHY	SMB	SMBUS_SMC_3_SDA	47 50
I78	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SCL	47 48 50
I79	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SDA	47 48 50
I80	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	47 48 50
I81	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	47 48 50

RTC_*

	Spacing	Netname	
I56	PM	RTC_RESET_L	18 26 48
I57	PM	RTC_RESET_L_R	48

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SMCISNS_*

	Physical	Spacing	Netname	
I41	SNS_PHY	SENSE	SMCISNS_CPUAXG	48 51
I42	SNS_PHY	SENSE	SMCISNS_CPUCORE	48 51
I43	SNS_PHY	SENSE	SMCISNS_GPUCORE	48 51
I44	SNS_PHY	SENSE	SMCISNS_P12VG3H	48 51
I45	SNS_PHY	SENSE	SMCISNS_P12VS0_CPU_P1V05	48 55
I46	SNS_PHY	SENSE	SMCISNS_P12VS0_CPU_VCCSA	48 55
I47	SNS_PHY	SENSE	SMCISNS_P12VS0_FBVDDQ	48 51
I48	SNS_PHY	SENSE	SMCISNS_P12VS0_HDD	48 51
I49	SNS_PHY	SENSE	SMCISNS_P12VS0_P1V05	48 55
I410	SNS_PHY	SENSE	SMCISNS_P1V05S0_PCH	48 51
I411	SNS_PHY	SENSE	SMCISNS_P1V5S0_CPU_MEM	48 51
I412	SNS_PHY	SENSE	SMCISNS_P3V3S0_SSD	48 51
I413	SNS_PHY	SENSE	SMCISNS_P3V3S4_AP	48 55
I414	SNS_PHY	SENSE	SMCISNS_P5VS0_HDD	48 51
I415	SNS_PHY	SENSE	SMCISNS_PVDDQS3_DDR	48 51

SMCVSNS_*

	Physical	Spacing	Netname	
I416	SNS_PHY	SENSE	SMCVSNS_CPUAXG	48 51
I417	SNS_PHY	SENSE	SMCVSNS_CPUCORE	48 51
I418	SNS_PHY	SENSE	SMCVSNS_GPUCORE	48 51
I419	SNS_PHY	SENSE	SMCVSNS_P12VG3H	48 51
I420	SNS_PHY	SENSE	SMCVSNS_P1V05S0_PCH	48 51
I421	SNS_PHY	SENSE	SMCVSNS_P1V5S0_CPU_MEM	48 51
I422	SNS_PHY	SENSE	SMCVSNS_P3V3S0	48 51
I423	SNS_PHY	SENSE	SMCVSNS_P5VS0_HDD	48 51
I424	SNS_PHY	SENSE	SMCVSNS_PVDDQS3_DDR	48 51

SMC_*

	Physical	Spacing	Netname	
I425		GENERIC_ISO	SMC_ACDC_ID	6 48
I426		GENERIC_ISO	SMC_ACDC_ID_R	6
I427		PM	SMC_ASSERT_RTCRST	48
I428		GENERIC_ISO	SMC_BLC_MUX_RX_L	48 80
I429		GENERIC_ISO	SMC_BLC_MUX_TX_L	48 80
I430		GENERIC_ISO	SMC_CPU_CATERR_L	47 48
I431	CPU_PHY	CPU	SMC_CPU_PECI	48
I432		PM	SMC_DELAYED_PWRGD	38 47 48 65
I433		GENERIC_ISO	SMC_DP_HPD_L	47 48
I434	CLK_XTAL	XTAL	SMC_EXTAL	47 48
I435		GENERIC_ISO	SMC_FAN_0_CTL	47 54
I436		GENERIC_ISO	SMC_FAN_0_TACH	47 54
I437		GENERIC_ISO	SMC_GFX_OVERTEMP	47 48 91
I438		GENERIC_ISO	SMC_GFX_OVERTEMP_Q	91
I439		GENERIC_ISO	SMC_GFX_OVERTEMP_R_L	91
I440		PM	SMC_GFX_THROTTLE_L	47 91
I441		PM	SMC_GFX_THROTTLE_R_L	91
I442		PM	SMC_LRESET_L	26 47
I443		PM	SMC_MANUAL_RST_L	48
I444		PM	SMC_ONOFF_L	47 48
I445		SENSE	SMC_OOB1_RX_CN	44
I446		SENSE	SMC_OOB1_RX_FILT	44 52
I447		SENSE	SMC_OOB1_RX_L	47 52
I448		SENSE	SMC_OOB1_RX_R	52
I449		SENSE	SMC_OOB1_TX_L	47 48
I450		SENSE	SMC_OOB2_RX_L	44 48
I451		SENSE	SMC_OOB2_TX_L	44 48
I452	CPU_PHY	CPU	SMC_PECI_L	47 48
I453	CPU_PHY	CPU	SMC_PECI_L_R	48
I454		PM	SMC_PME_S4_WAKE_L	35 47 48
I455		GENERIC_ISO	SMC_PM_G2_EN	47 48 74
I456		PM	SMC_PM_PCH_SYS_PWROK	47 48
I457		CPU	SMC_PROCHOT	47 48
I458		PM	SMC_RESET_L	47 48 49

SMC_*

	Physical	Spacing	Netname	
I459		GENERIC_ISO	SMC_ROMBOOT	48 49
I460		GENERIC_ISO	SMC_RUNTIME_SCI_L	15 21 47
I461		GENERIC_ISO	SMC_RX_L	47 48 49
I462		PM	SMC_S4_WAKESRC_EN	35 47 48
I463		GENERIC_ISO	SMC_TCK	47 48 49
I464		GENERIC_ISO	SMC_TDI	47 48 49
I465		GENERIC_ISO	SMC_TDO	47 48 49
I466		PM	SMC_THRMTRIP	47 48
I467		GENERIC_ISO	SMC_TMS	47 48 49
I468		GENERIC_ISO	SMC_TO_BLC_RX_L	48
I469		GENERIC_ISO	SMC_TO_BLC_TX_L	48
I470		GENERIC_ISO	SMC_TX_L	47 48 49
I471		PM	SMC_WAKE_L	47
I472		GENERIC_ISO	SMC_WAKE_SCI_L	15 21 47
I473	CLK_XTAL	XTAL	SMC_XTAL	47 48
I474	CLK_XTAL	XTAL	SMC_XTAL_R	48

SML_*

	Physical	Spacing	Netname	
I475	SMB_PHY	SMB	SML_PCH_0_CLK	18 50
I476	SMB_PHY	SMB	SML_PCH_0_DATA	18 50
I477	SMB_PHY	SMB	SML_PCH_1_CLK	18 50
I478	SMB_PHY	SMB	SML_PCH_1_DATA	18 50

SPI_*

	Spacing	Netname	
I479	GENERIC_ISO	SPI_DESCRIPTOR_OVERRIDE_L	15 47

SSD_*

	Spacing	Netname	
I480	GENERIC_ISO	SSD_CLKREQ_L	15 18

SYS_*

	Spacing	Netname	
I481	PM	SYS_PWROK_R	65

TBT_*

	Physical	Spacing	Voltage	Netname	
I482		GENERIC_ISO	3.3V	TBT_A_BIAS	77
I483	TBT_GEN_55S	TBT_GEN		TBT_A_CONFIG1_RC	77
I484		PM		TBT_A_HV_EN	36 77
I485		GENERIC_ISO	3.3V	TBT_B_BIAS	79
I486	TBT_GEN_55S	TBT_GEN		TBT_B_CONFIG1_RC	79
I487		PM		TBT_B_HV_EN	36 79
I488		GENERIC_ISO		TBT_CLKREQ_ISOL_L	38
I489		GENERIC_ISO		TBT_CLKREQ_L	15 38
I490		GENERIC_ISO		TBT_DDC_XBAR_EN_L	36 76
I491		GENERIC_ISO		TBT_EN_CIO_PWR	38
I492		PM		TBT_EN_CIO_PWR_L	36 38
I493		GENERIC_ISO		TBT_EN_LC_ISOL	38
I494		GENERIC_ISO		TBT_EN_LC_PWR	36 38
I495		GENERIC_ISO		TBT_PCH_CLKREQ_L	15 21
I496		PM		TBT_PWR_EN	15 26 36
I497		PM		TBT_PWR_EN_PCH	18 26
I498		PM		TBT_PWR_ON_POC_RST_L	36 38
I499		PM		TBT_PWR_REQ_L	15 20 36
I4100		PM		TBT_S0_EN	64
I4101		PM		TBT_SW_RESET_L	21 38

TSNS_*

	Electrical	Physical	Spacing	Netname	
I4102	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_N	53
I4103	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_P	53
I4104	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_N	53
I4105	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_P	53
I4106	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_N	53
I4107	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_P	53
I4108	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_N	53
I4109	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_P	53
I4110	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_N	53
I4111	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_P	53
I4112	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_N	53
I4113	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_P	53
I4114	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_N	53
I4115	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_P	53
I4116	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_N	53
I4117	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_P	53
I4118	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_N	53
I4119	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_P	53
I4120	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_N	53
I4121	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_P	53
I4122	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_ACDC_N	6 53
I4123	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_ACDC_P	6 53
I4124	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_N	53
I4125	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_P	53

UVP_*

	Spacing	Netname	
I4126	PM	UVP_IN_1	82
I4127	PM	UVP_IN_1_REF	82
I4128	PM	UVP_IN_2	82
I4129	PM	UVP_IN_3	82
I4130	PM	UVP_IN_4	82
I4131	PM	UVP_REF	82

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VREFMRGN_*

Spacing	Netname	
GENERIC_ISO	VREFMRGN_CA_SODIMMA_EN	34
GENERIC_ISO	VREFMRGN_CA_SODIMMB_EN	34

VTTCLAMP_*

Spacing	Netname	
GENERIC_ISO	VTTCLAMP_EN	28
GENERIC_ISO	VTTCLAMP_L	28

WOL_*

Spacing	Netname	
GENERIC_ISO	WOL_EN	15 21 40

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