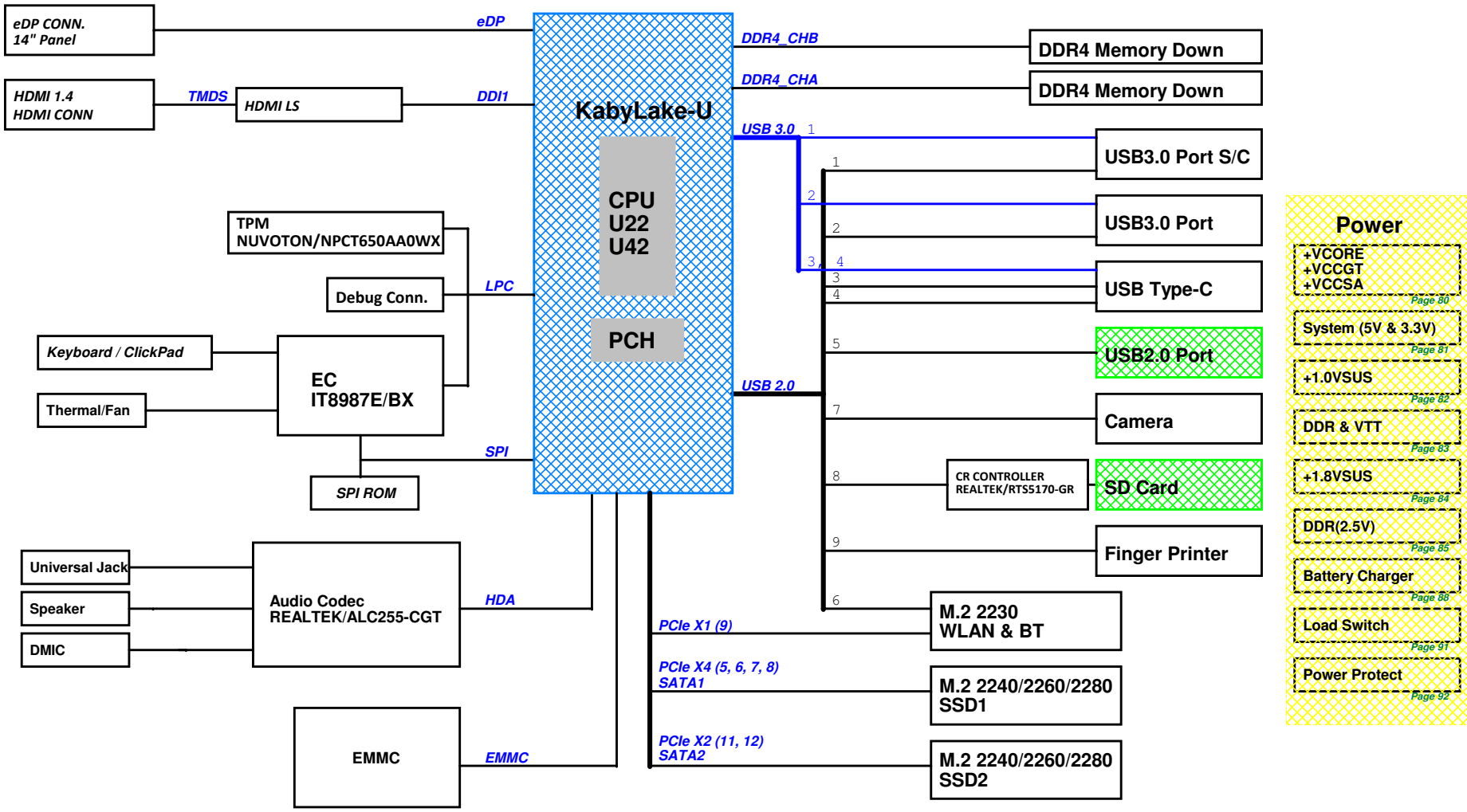
SU4EA Block Diagram



PEGATRON Title : Block Diagram

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BGT-HW3 RD

Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

Date: Monday, February 20, 2017 Sheet 1 of 94

Option

Optional	Remark
N/A	Mount
/@	Ummount
/Debug	Debug only
/EMI	Reserved EMI part
/UMA	Support UMA
/VGA	Support VGA
/SDP	Support SDP DRAM
/DDP	Support DDP DRAM
/U22	Support 2+2 CPU
/U42	Support 4+2 CPU
/14inch	Support 14"
/15inch	Support 15"
/TPM	Support TPM function
/IOAC	Support IOAC
/NON-IOAC	Not support IOAC
/PTP	Support PTP
/NON-PTP	Not support PTP

/SSD1	Support M.2 SSD1
/SSD2	Support M.2 SSD2
/EMMC	Support EMMC

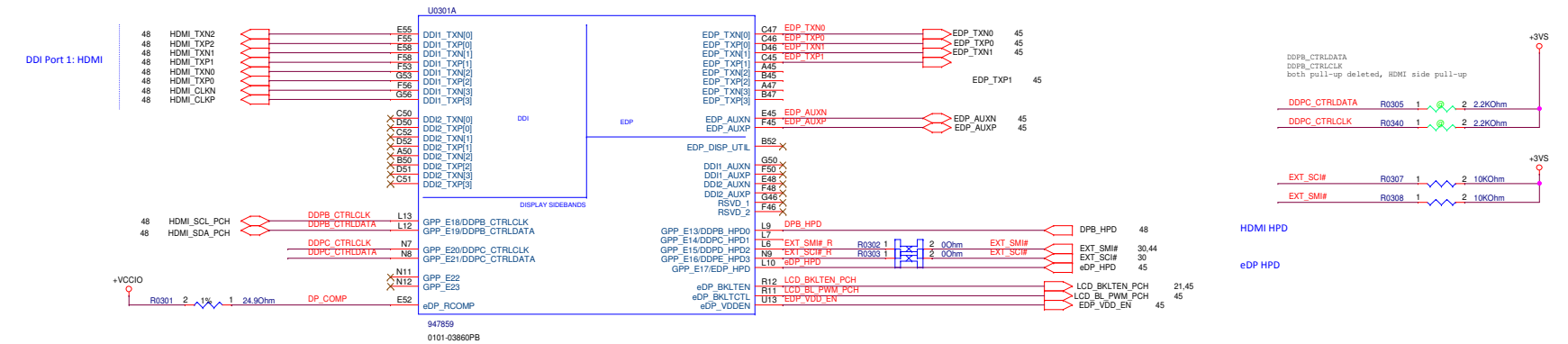
03

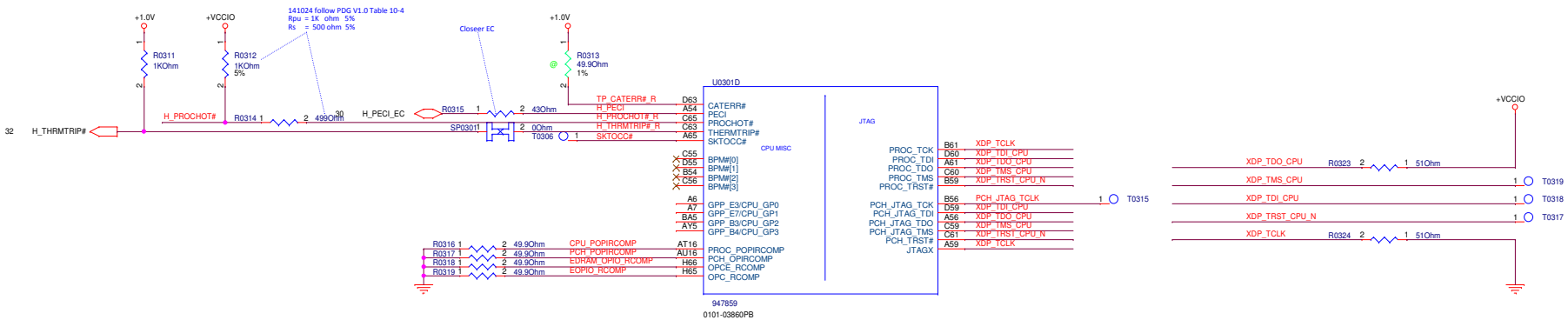
CPU(1)_DDI_eDP

+VCCIO — +VCCIO 5,7,9,57,91
+VCCST_CPU — +VCCST_CPU 7
+VCCSTG — +VCCSTG 7
+3VS — +3VS 4,20,21,22,23,24,30,31,32,36,41,44,45,48,49,50,51,53,56,57,62,64,65,91,92

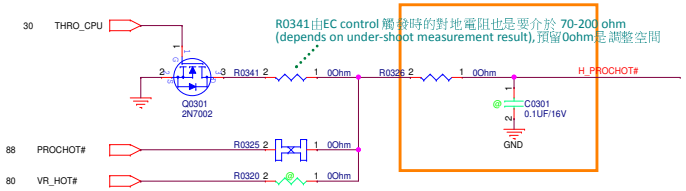
DDI#1 DDPB_CTRLDATA
DDI#2 DDPC_CTRLDATA
DDPD_CTRLDATA
- Internal weak pull down 20k ohm
- 0 : port is not detected
 1 : port is detecced

SKYLAKE-U symbol ReV0.53 #545316 / Ballout_Rev0_71 #543787 / PEGA local PN is 4201-0062000





R1.2 MB_Lesson learnt template



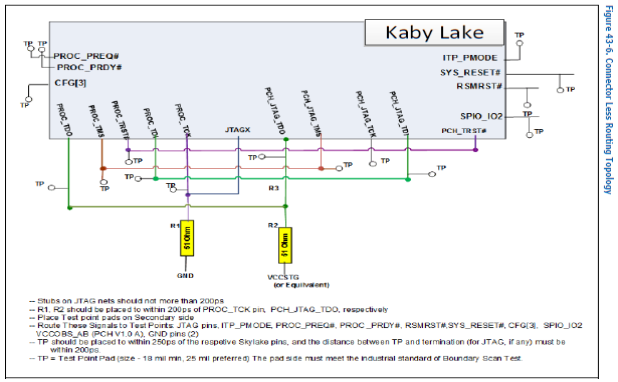


Figure 49-6 Connector Less Routing Topology

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RGT-HWS RD

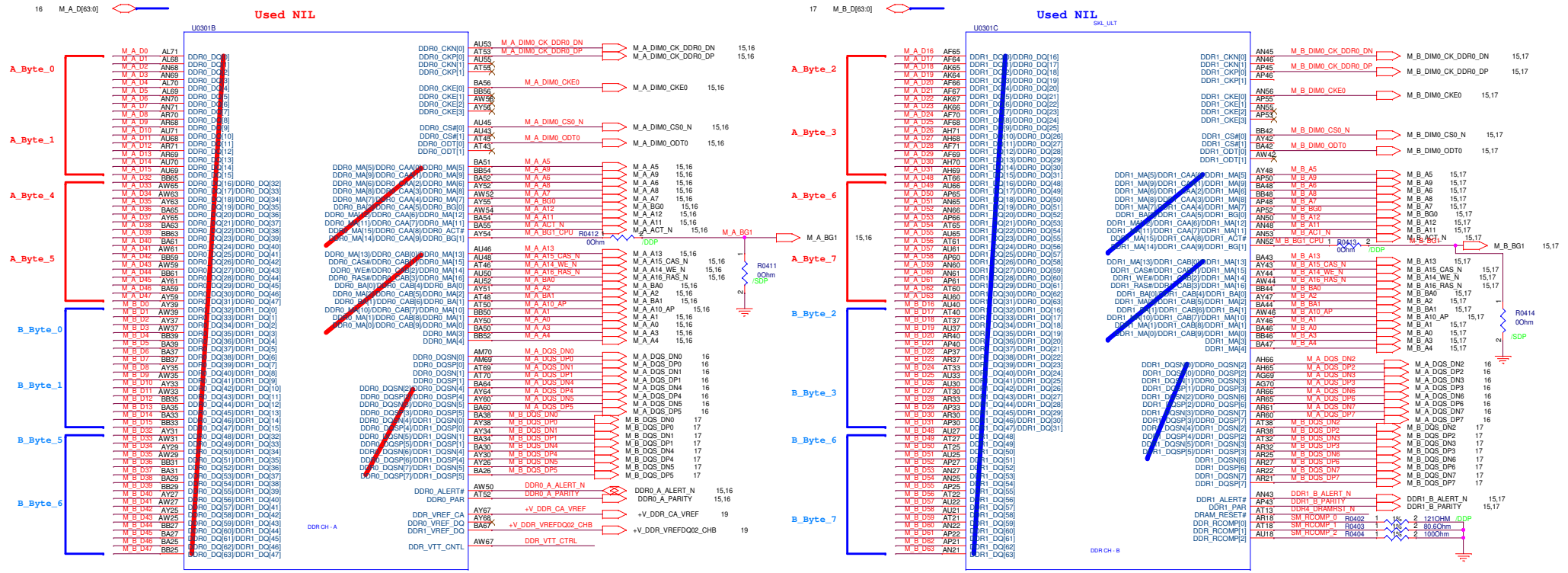
Title : CPU(1)_DDI_eDP

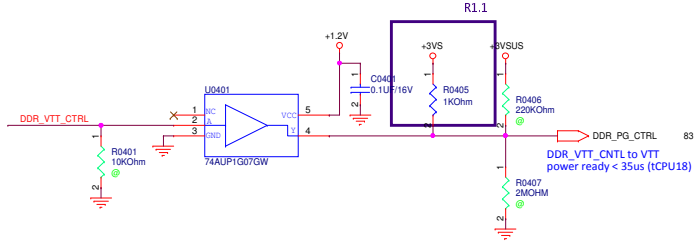
Engineer: James_Liao

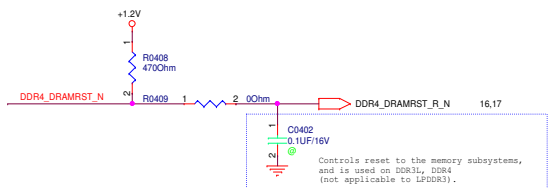
Size	Project Name	Rev
C	SU4EA	1.0

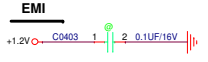
Date: Thursday, February 23, 2017 Sheet 3 of 94

04 Memory bus_DDR4









Symbol U0301 B

	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelA DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[0..15] DQS/DQS#[0,1]
BYTE 1		ChannelADQ[32..47] DQS/DQS#[4,5]
BYTE 2		ChannelB DQ[0..15] DQS/DQS#[0,1]
BYTE 3		ChannelB DQ[32..47] DQS/DQS#[4,5]
BYTE 4		
BYTE 5		
BYTE 6		
BYTE 7		

Symbol U0301 C

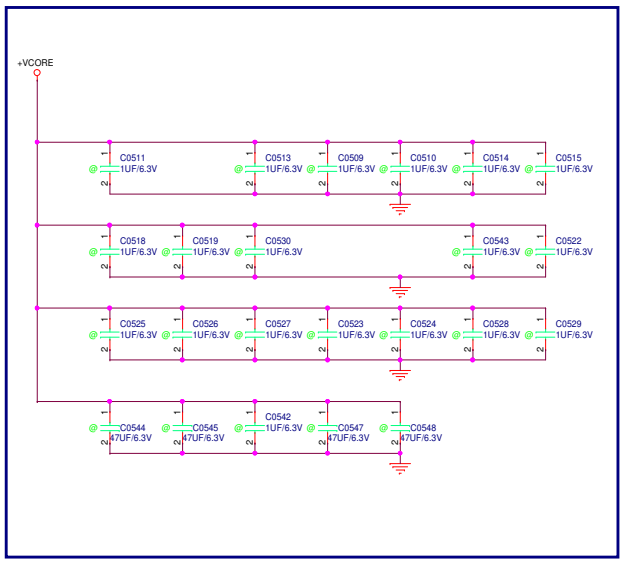
	interleaved(Symbol default)	Non-interleaved
BYTE 0	ChannelB DQ[0..63] DQS/DQS#[0..7]	ChannelA DQ[16..31] DQS/DQS#[2,3]
BYTE 1		ChannelADQ[48..63] DQS/DQS#[6,7]
BYTE 2		ChannelB DQ[16..31] DQS/DQS#[2,3]
BYTE 3		ChannelB DQ[48..63] DQS/DQS#[6,7]
BYTE 4		
BYTE 5		
BYTE 6		
BYTE 7		

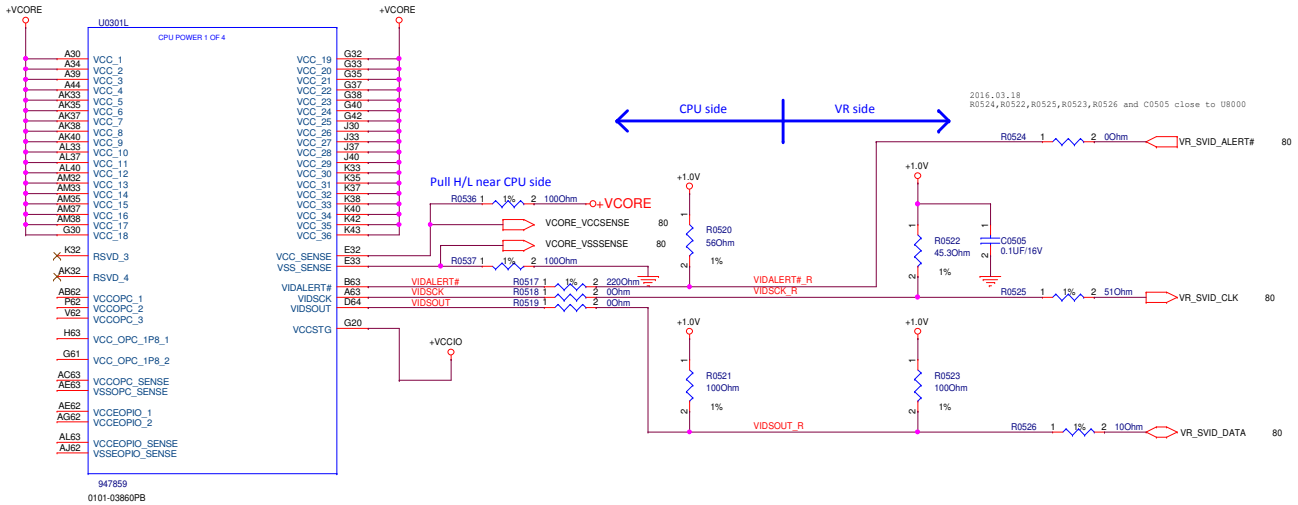
PEGATRON Title : Memory bus_DDR4
PEGATRON PROPRIETARY AND CONFIDENTIAL
BGT-HWS RD
Engineer: James_Liao
Size: C | Project Name: SU4EA | Rev: 1.0
Date: Thursday, February 23, 2017 | Sheet 4 of 94

05

CPU(3)_+VCCCORE

R1.1 follow intel PDG_James





PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
RGT-HW3 RD

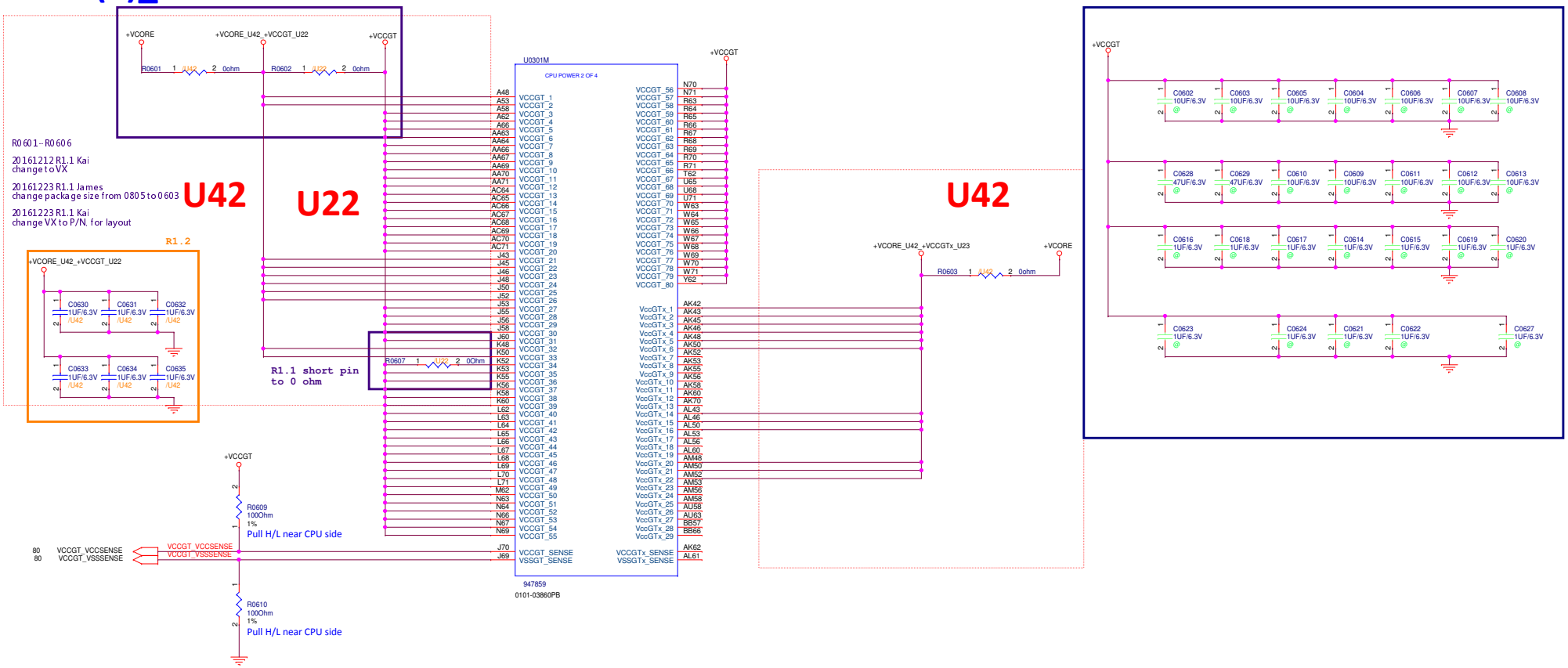
Title : CPU(3)_+VCCCORE
Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

Date: Thursday, February 23, 2017 Sheet 5 of 94

06 CPU(4)_+VCCGT

R1.1 follow intel PDG



Ball #	Ball Names R-U42		Ball #	Ball Names U22		X[um]	Y[um]	R-U42/U22 common baord guidelines
C7	XTAL24_OUT		C7	NC		16791.178	-10013.696	connect to R-U42 XTAL24_OUT
E3	XTAL24_IN		E3	NC		19013.678	-9039.86	connect to R-U42 XTAL24_IN
E35	NC		E35	XTAL24_OUT		280.416	-8591.296	connect to U22 XTAL24_OUT
E37	NC		E37	XTAL24_IN		-633.984	-8591.296	connect to U22 XTAL24_IN
AK42	VCCCORE		AK42	VccGTx		-3377.184	4009.136	
AK43	VCCCORE		AK43	VccGTx		-4291.584	4009.136	
AK45	VCCCORE		AK45	VccGTx		-5205.984	4009.136	
AK46	VCCCORE		AK46	VccGTx		-6120.384	4009.136	
AK48	VCCCORE		AK48	VccGTx		-7034.784	4009.136	
AK50	VCCCORE		AK50	VccGTx		-7949.184	4009.136	connect to VccGTx/VCCCORE
AL43	VCCCORE		AL43	VccGTx		-3834.384	4473.956	power plane island
AL46	VCCCORE		AL46	VccGTx		-5663.184	4473.956	
AL50	VCCCORE		AL50	VccGTx		-7491.984	4473.956	
AM48	VCCCORE		AM48	VccGTx		-7034.784	4946.396	
AM50	VCCCORE		AM50	VccGTx		-7949.184	4946.396	
AM52	VCCCORE		AM52	VccGTx		-8863.584	4946.396	
J43	VCCCORE		J43	VCCGT		-4748.784	-6826.504	
J45	VCCCORE		J45	VCCGT		-5663.184	-6826.504	
J46	VCCCORE		J46	VCCGT		-6577.584	-6826.504	
J48	VCCCORE		J48	VCCGT		-7491.984	-6826.504	
J50	VCCCORE		J50	VCCGT		-8406.384	-6826.504	connect to VccGT/VCCCORE
J52	VCCCORE		J52	VCCGT		-9320.784	-6826.504	power plane island
K48	VCCCORE		K48	VCCGT		-7034.784	-6361.684	
K50	VCCCORE		K50	VCCGT		-7949.184	-6361.684	
A48	VCCCORE		A48	VCCGT		-7313.422	-10989.056	
A53	VCCCORE		A53	VCCGT		-9791.446	-10989.056	
AK52	RSVD		AK52	VccGTx		-8863.584	4009.136	Not Connected
K52	RSVD		K52	VCCGT		-8863.584	-6361.684	Not Connected

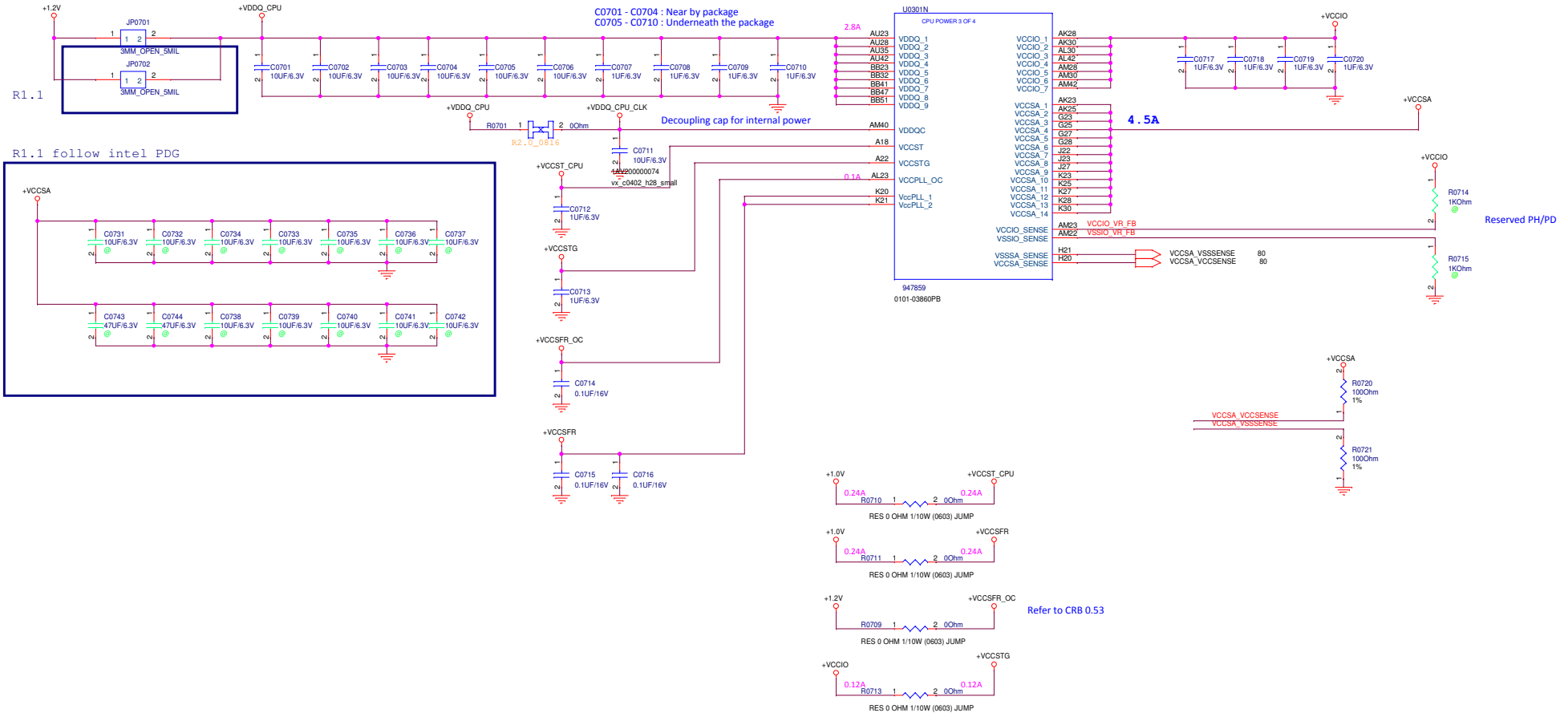
PEGATRON Title : CPU(4)_+VCCGT
PEGATRON PROPRIETARY AND CONFIDENTIAL
BGT-HWS RD
Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 6 of 94

07

CPU(5)_+VDDQ/IO/SA



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RGT-HWS RD

Title: CPU(5)_+VDDQ/IO/SA

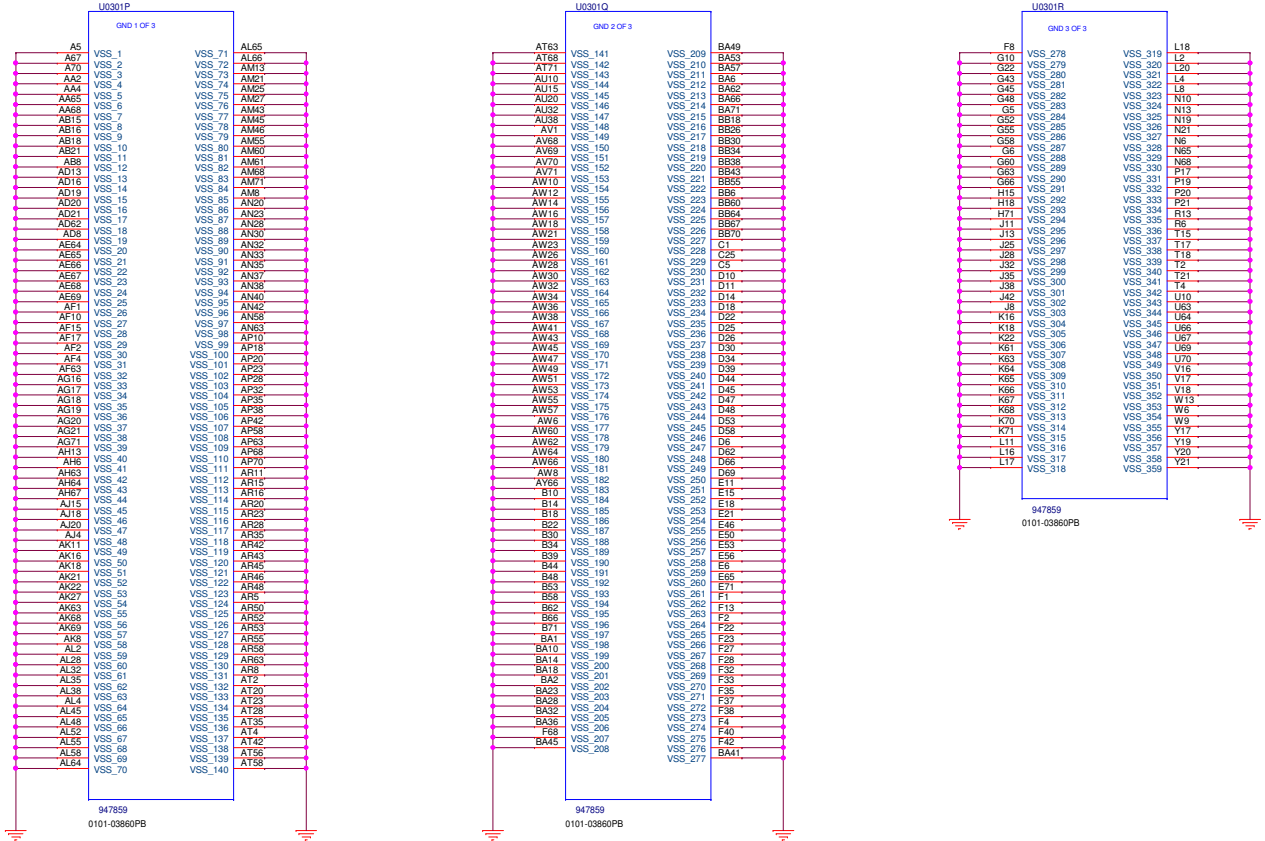
Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

Date: Thursday, February 23, 2017 Sheet 7 of 94

08

CPU(6)_CPU GND



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RGT-HW3 RD

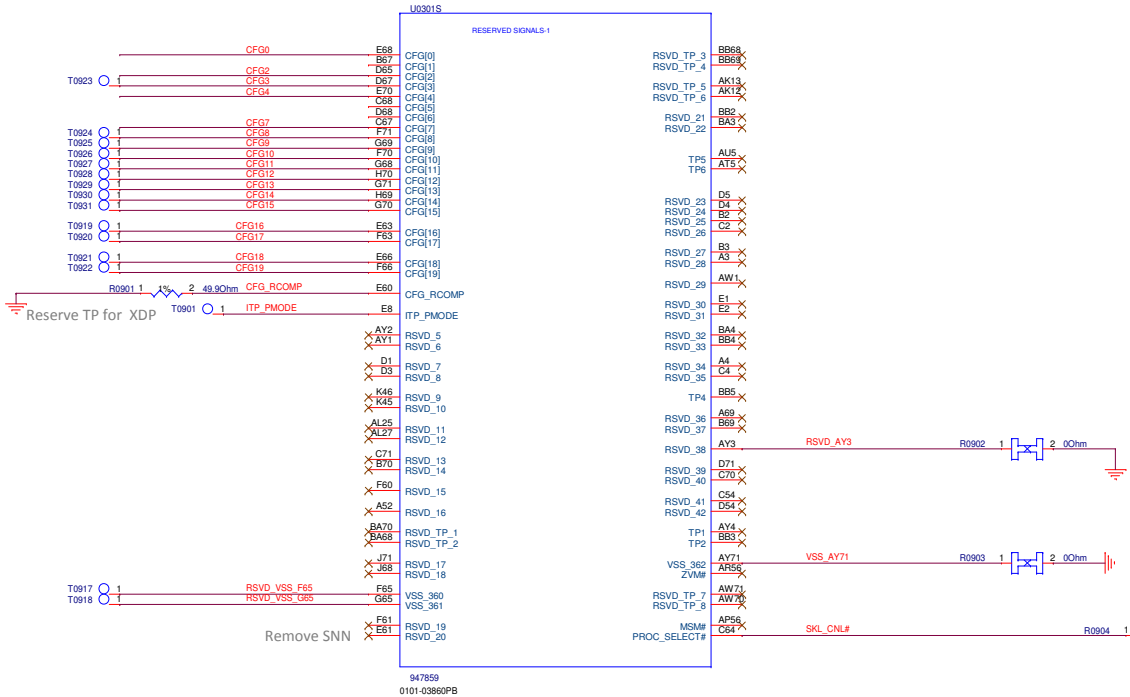
Title : CPU(6)_CPU GND

Engineer: James_Liao

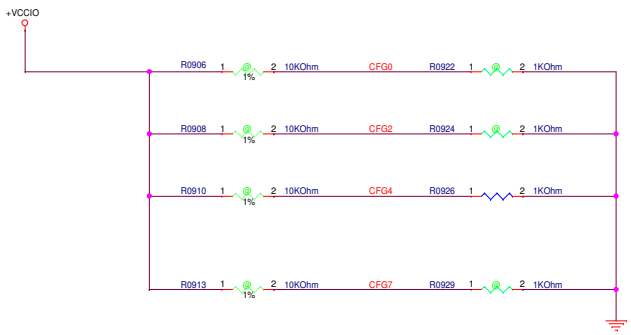
Size	Project Name	Rev
C	SU4EA	1.0

Date: Monday, February 20, 2017 Sheet 8 of 94

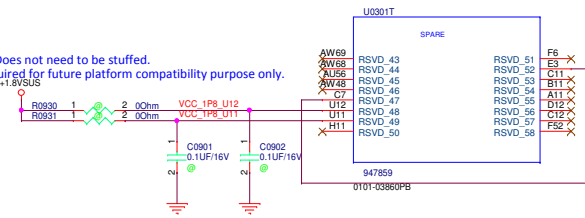
09CPU(7)_CFG/RSVD

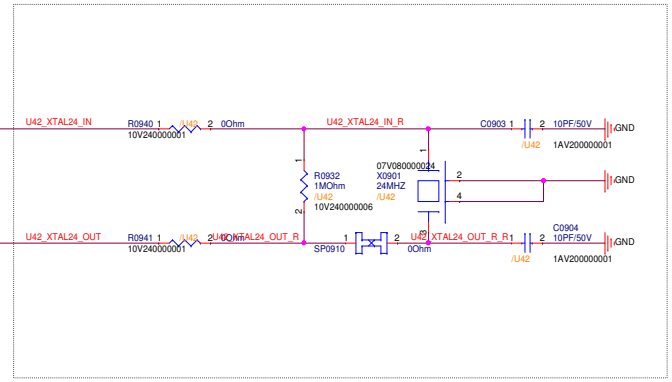


MOW WW48
1. Ball C64 which is PROC_SELECT# needs to be pulled to VCCST for Cannonlake support via 100K ohm resistor and with no resistor populated (floating pin) for Skylake.



PDG 1.2
Placeholder only. Does not need to be stuffed.
Placement are required for future platform compatibility purpose only.





Name	P5HCJ_KBL	Description
CFG0	1	1 = (Default) Normal Operation; No stall 0 = Stall
CFG1	1	Reserved configuration lane
CFG2	1	PCI Express* Static x16 Lane Numbering Reversal 1 = Normal operation 0 = Lane numbers reversed
CFG3	1	Reserved configuration lane
CFG4	0	CFG[4]: eDP* enable: 1 = Disabled. 0 = Enabled
CFG5 CFG6	1	CFG[6:5]: PCI Express* Bifurcation 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express*
CFG7	1	CFG[7]: PEG Training: 1 = (default) PEG Train immediately following RESET# de assertion 0 = PEG Wait for BIOS for training.
CFG[19:8]	1	Reserved configuration lane

From EDS_Intel_CPU(Kabylake.UY)_Vol1_559100_Rev0p91 Page.123

The CFG signals have a default value of '1' if not terminated on the board.

*All processor lines.
CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them

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RGT-HW3 RD
Title : CPU(7)_CFG/RSVD
Engineer: James_Liao
Size: C | Project Name: SU4EA | Rev: 1.0
Date: Friday, March 10, 2017 | Sheet 9 of 94

PEGATRON

Title : Block Diagram

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BG1-HW3 RD

Engineer: *James_Liao*

Size	Project Name	Rev
A	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 10 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	11 of 94

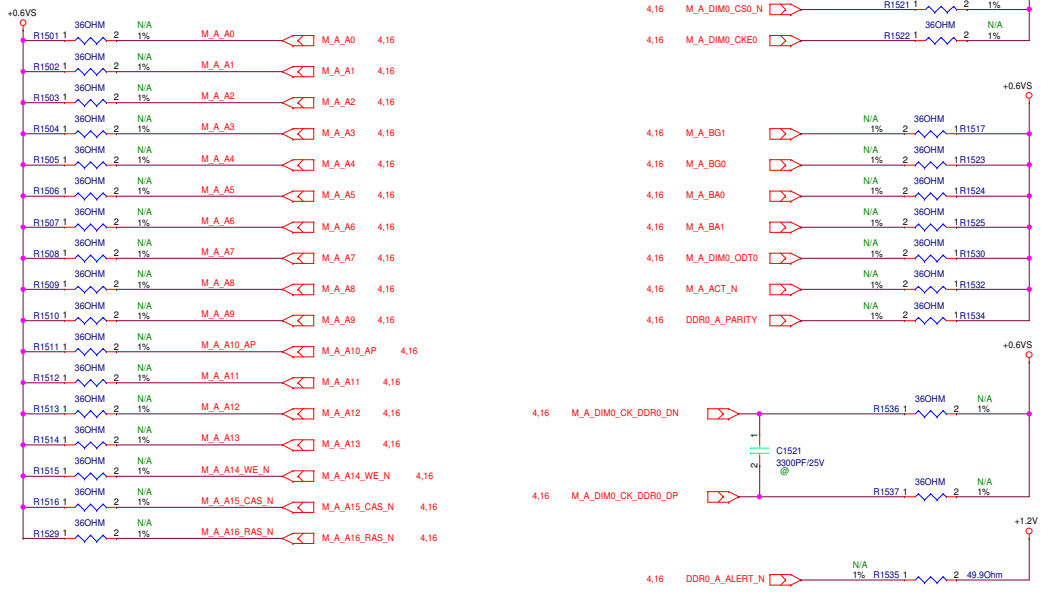
Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	12 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	13 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	14 of 94

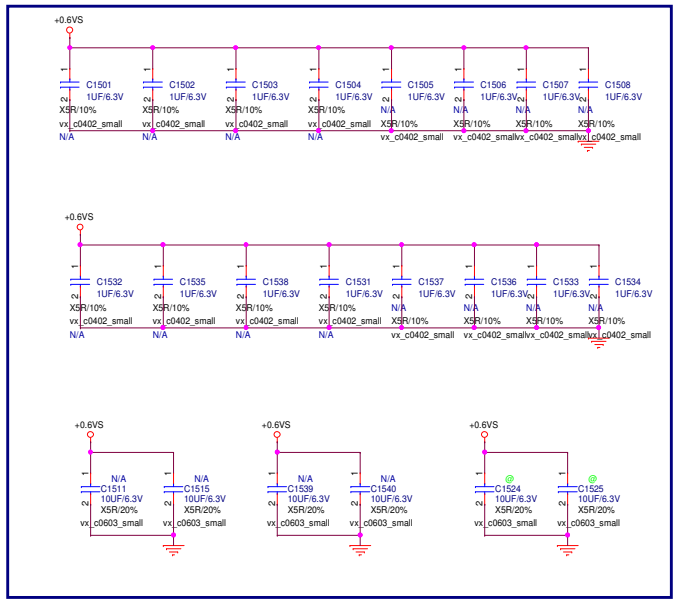
15 DDR4(0)_Termination

CHA

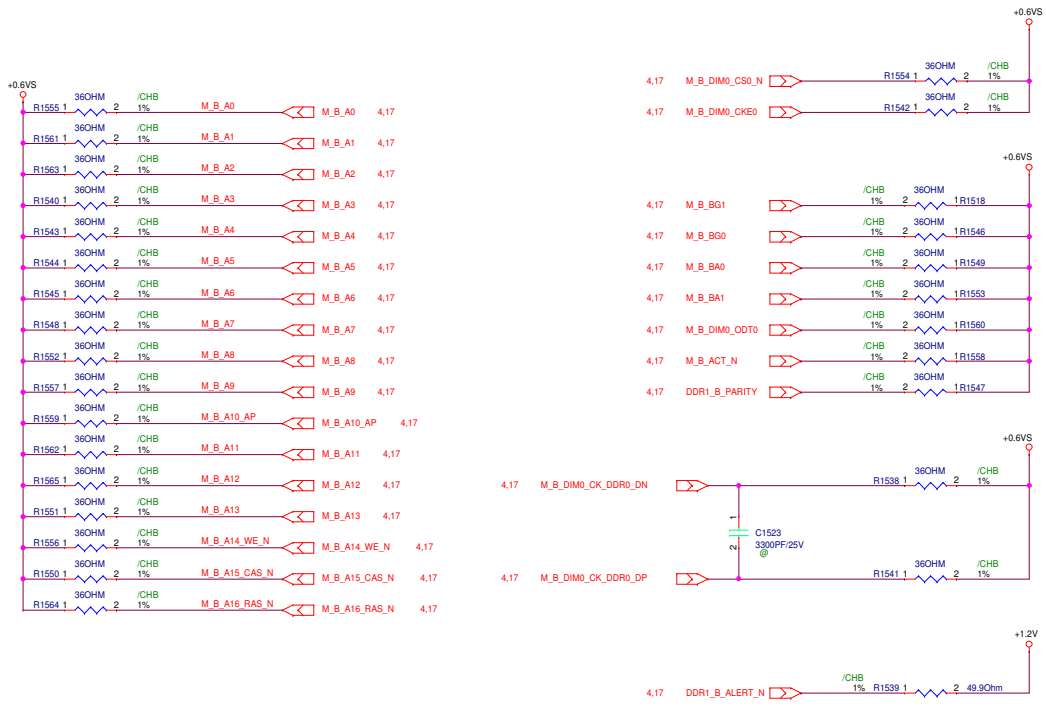


Average placed close to +VDDQ_VTT power plane

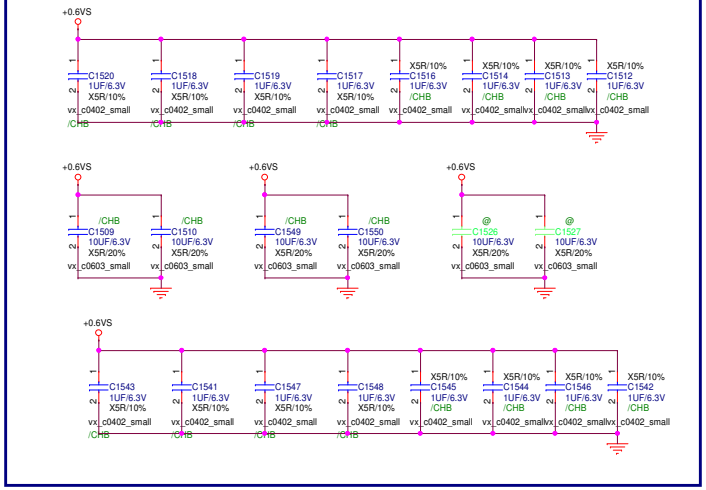
R1.1 follow intel PDG



CHB



R1.1 follow intel PDG



PEGATRON Title : DDR4(0)_Termination

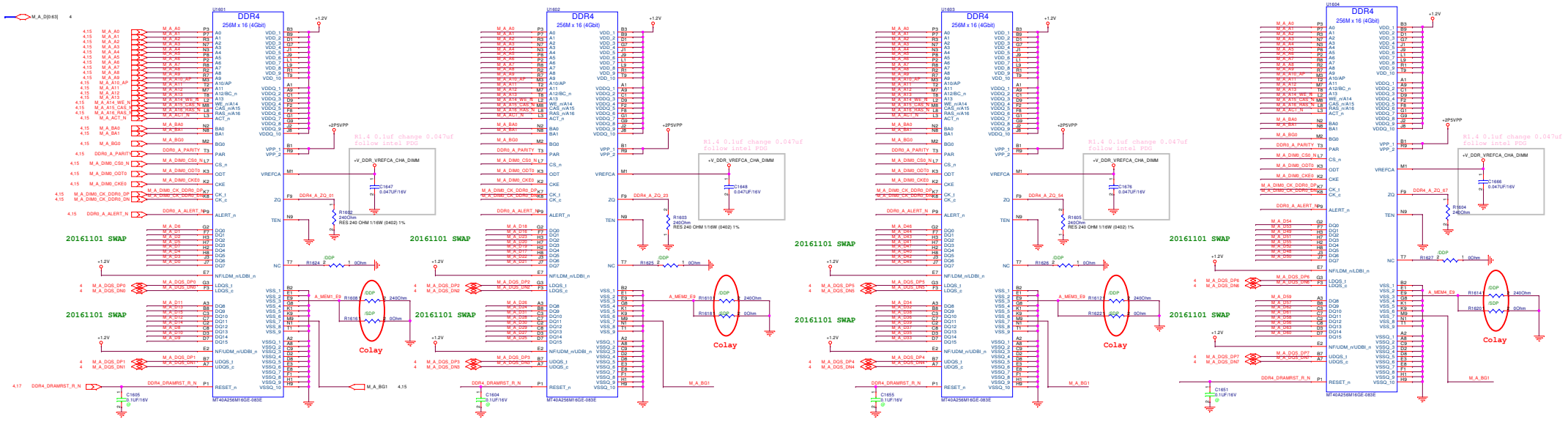
PEGATRON PROPRIETARY AND CONFIDENTIAL

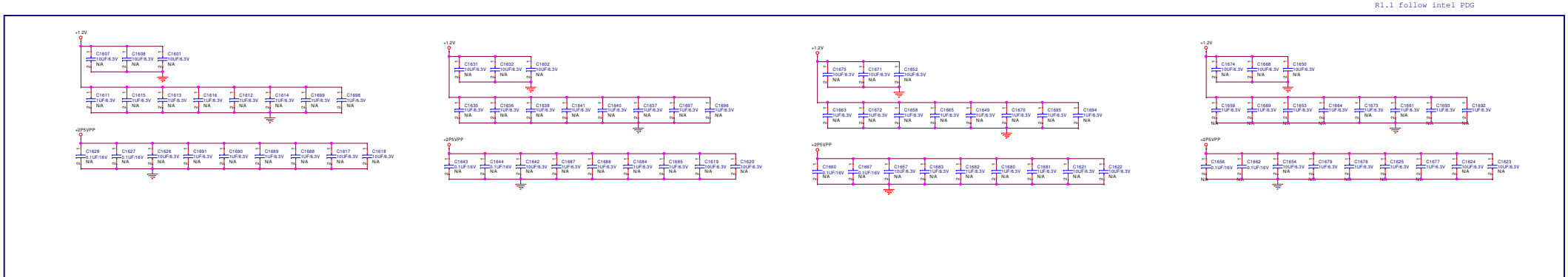
BGT-HWS RD Engineer:

Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 15 of 94

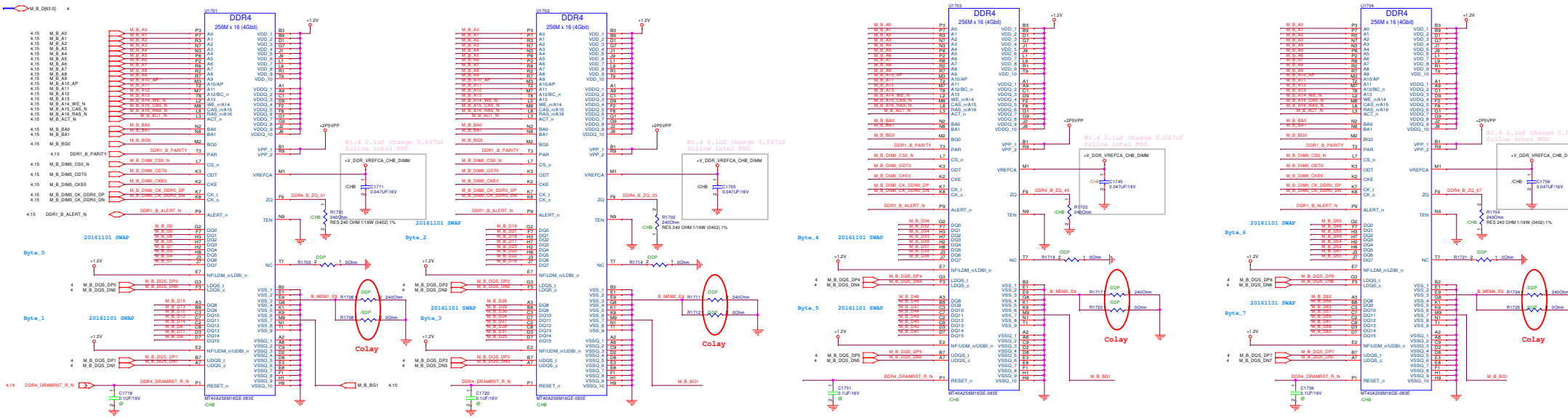
16 DDR4(1)_CH0

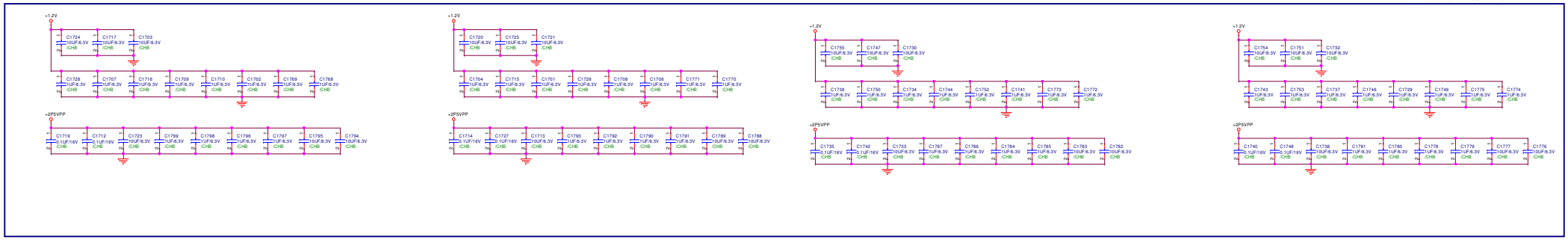




PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : DDR4(1)_CH0
Engineer:
Size: D | Project Name: SU4EA | Rev: 1.0
Date: Friday, March 10, 2017 | Sheet 16 of 94

17 DDR4(2)_CH1

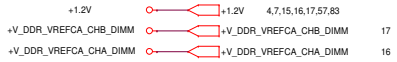




PEGATRON Title : DDR4(2)_CH0
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer:
Size: D | Project Name: SU4EA | Rev: 1.0
Date: Friday, March 10, 2017 | Sheet 17 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	18 of 94

19 DDR4(3)_CA/DQ Voltage



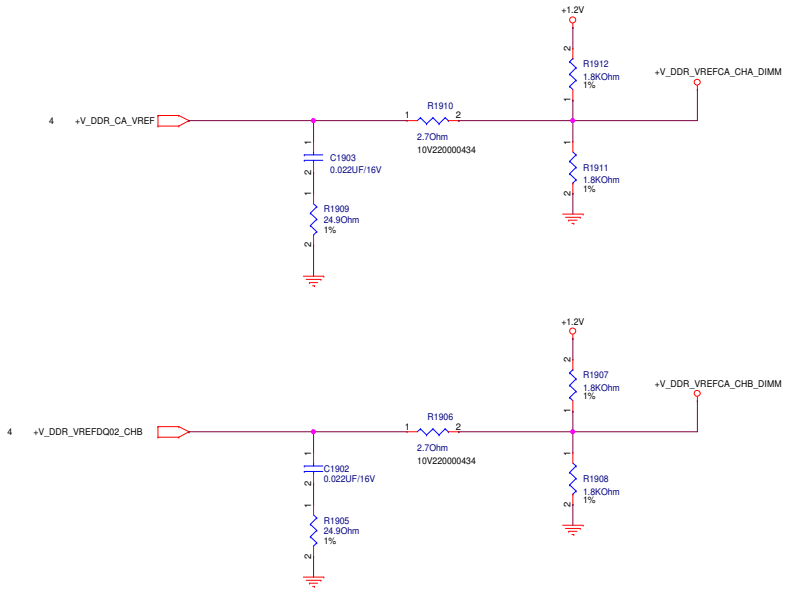
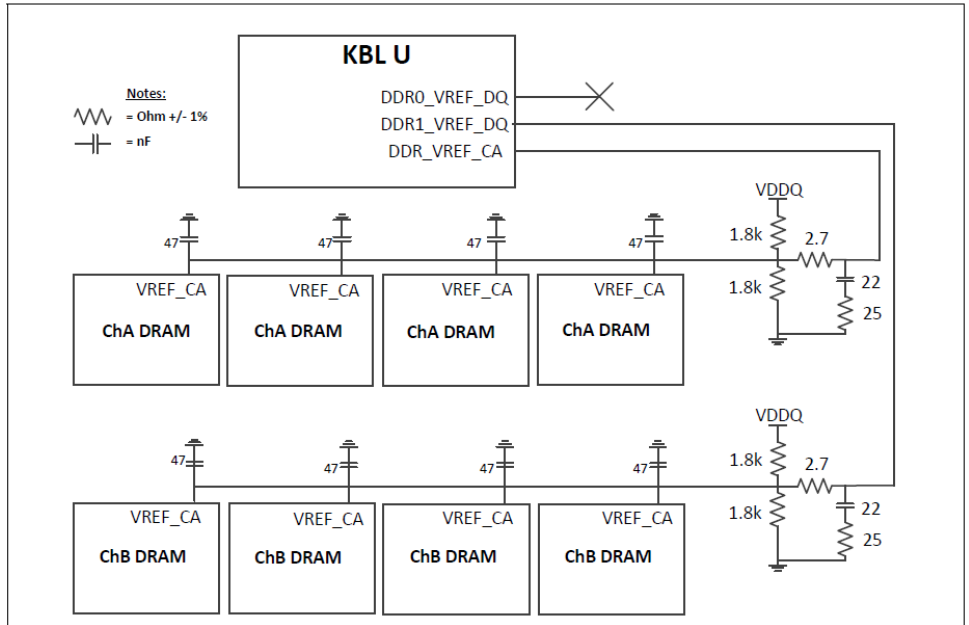


Figure 4-50. KBL U DDR4 x16 Devices Memory Down V_{REF-CA} Overview

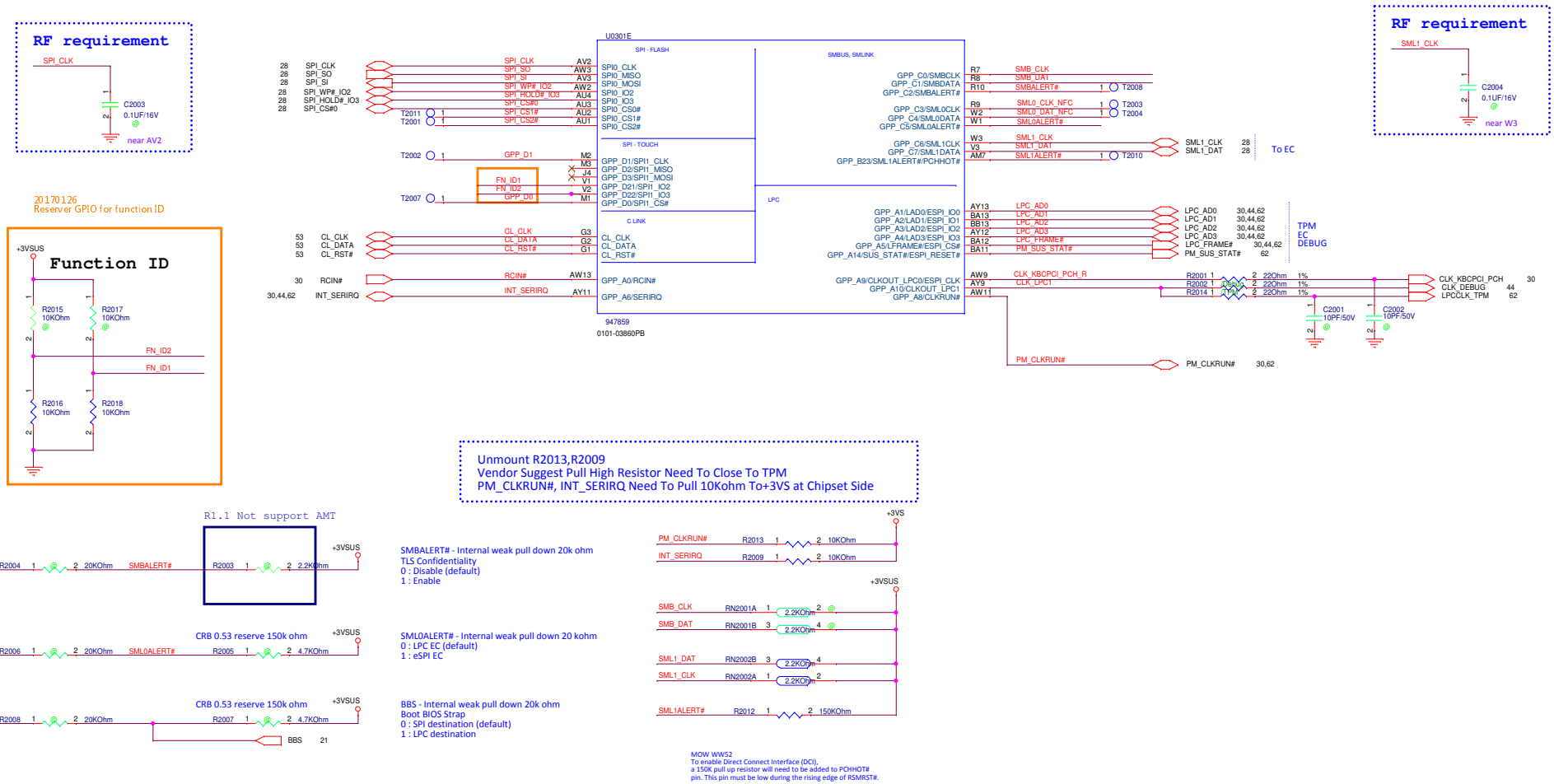


Notes:

1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

PEGATRON Title : DDR4(3)_CA/DQ Voltage
BG1-HW3 RD Engineer: James_Liao
Size C | Project Name SU4EA | Rev 1.0
Date: Friday, March 10, 2017 | Sheet 19 of 94

PCH(1)_SPI/LPC



PEGATRON Title : PCH(1)_SPI/LPC

PEGATRON PROPRIETARY AND CONFIDENTIAL

RGT-HW3 RD

Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

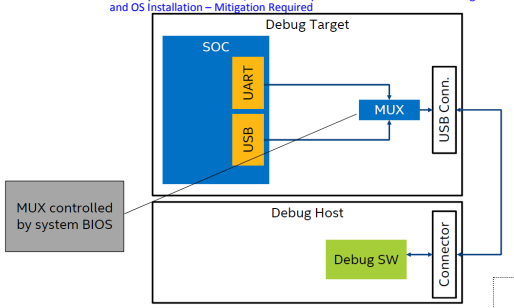
Date: Friday, March 10, 2017 Sheet 20 of 94

21

PCH(2)_ISH

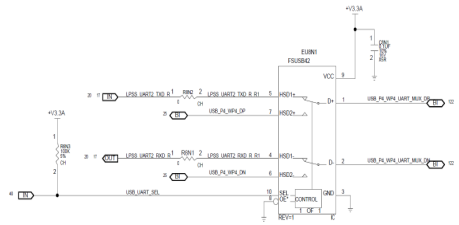
Microsoft* Windows* 7 System WHCK Requirement – OEM platforms are required to include a supported OS debug interface, accessible by an enduser. This allows developers to help in driver debug. The supported Windows 7 debug interfaces are EHCI, 1394 port and COM port.

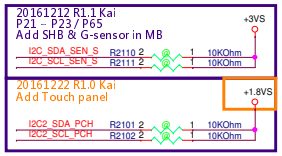
With skylake EHCI Removal, Potential Gap with Windows* 7 Kernel Debug and OS Installation – Mitigation Required

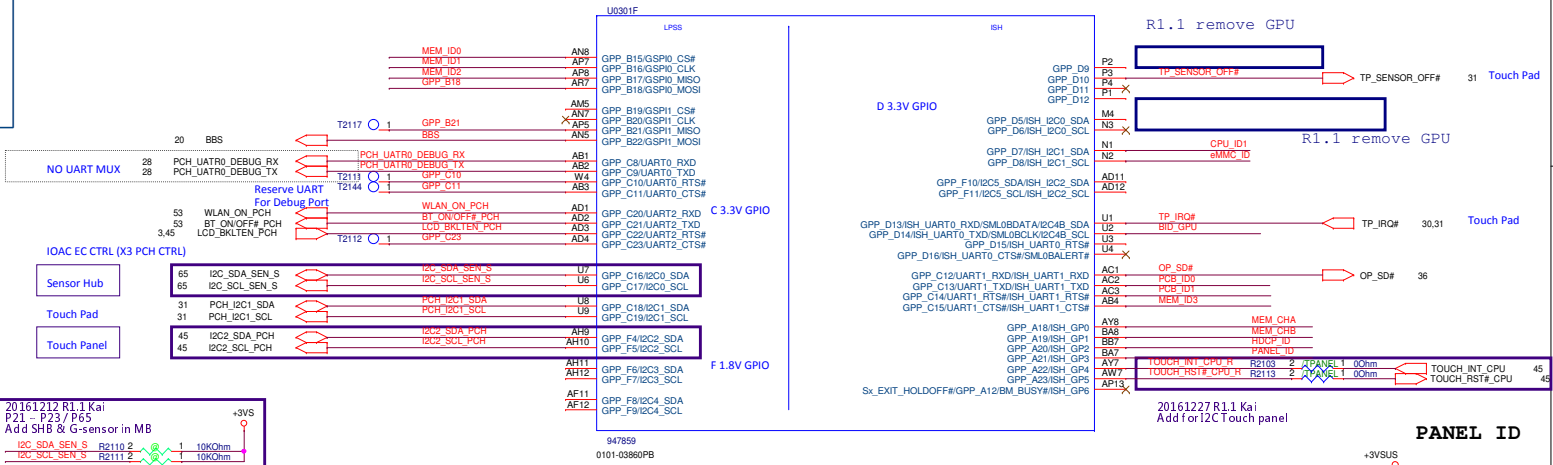


To implement UART for WIN7 WHCK requirement if need

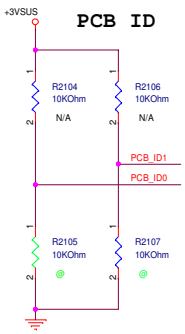
Please refer to Intel document #548689 - RVP5





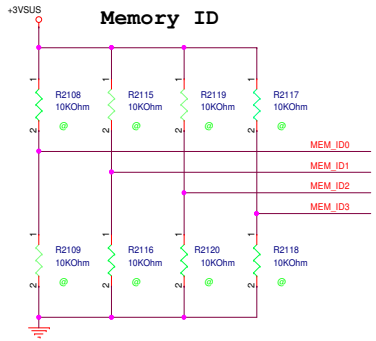


PCB ID



	PCB_ID1 (GPP_C14)	PCB_ID0 (GPP_C13)
R10	0	0
R11	0	1
R12	1	0
R20	1	1

Memory ID

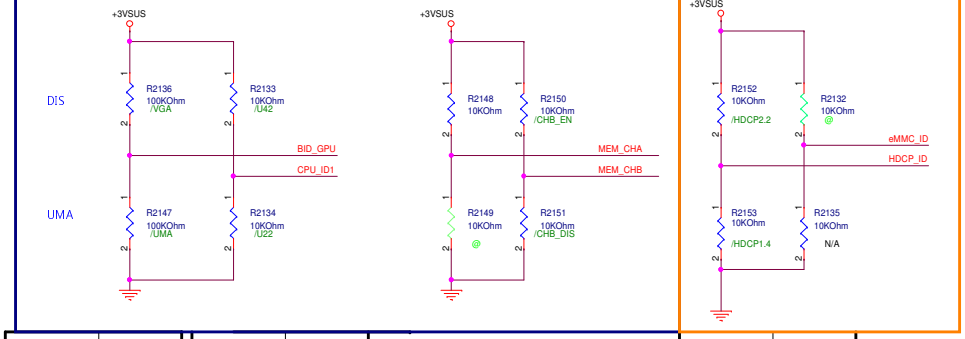


	MEM_ID3 (GPP_C15)	MEM_ID2 (GPP_B17)	MEM_ID1 (GPP_B16)	MEM_ID0 (GPP_B15)
HYNIX DDR4 2400 8Gb H5AN8G6NAFR-UHC 0315-01W60PB	0	0	0	0
MICRON DDR4 2400 4Gb MT40A256M16GE-083E:B 0315-01W80PB	0	0	0	1
MICRON DDR4 2400 8Gb MT40A512M16JY-083E:B 0315-01W90PB	0	0	1	0
SAMSUNG DDR4 2400 4Gb K4A4G165WE-BCRC 0315-01VV0PB	0	0	1	1
HYNIX DDR4 2400 4Gb H5AN4G6NAFR-UHC 0315-01WM0PB	0	1	0	0
SAMSUNG DDR4 2400 8Gb K4A8G165WB-BCRC 0315-01C80PB	0	1	0	1
HYNIX DDR4 2133 4Gb H5AN4G6NAFR-TF 0315-01EK0PB	0	1	1	0
MICRON/MT40A1G16WBU-083E:B 0315-01YC0PB	0	1	1	1

R1.1 change setting

R1.2 change setting

MB BD ID



	BID_GPU
UMA	0
DIS	1

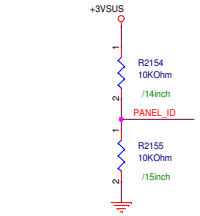
	CPU_ID1
U22	0
U42	1

	CHA	CHB
GPP_A18(0)	Disable	
GPP_A18(1)	Enable	
GPP_A19(0)		Disable
GPP_A19(1)		Enable

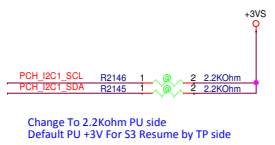
	eMMC_ID
disable	0
enable	1

	HDCP_ID
1.4	0
2.2	1

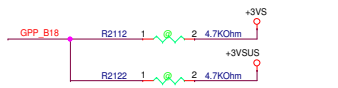
PANEL ID



R1.1 remove GPU



Change To 2.2Kohm PU side
Default PU +3V For S3 Resume by TP side

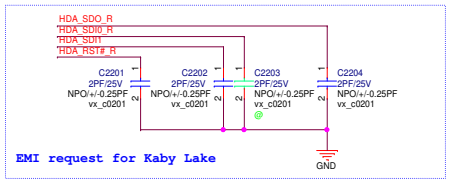


GSPI0_MOSI / GPP_B18 - Internal weak pull down 20k ohm
0 : Disable No Reboot mode(default)
1 : Enable NO Reboot Enable mode

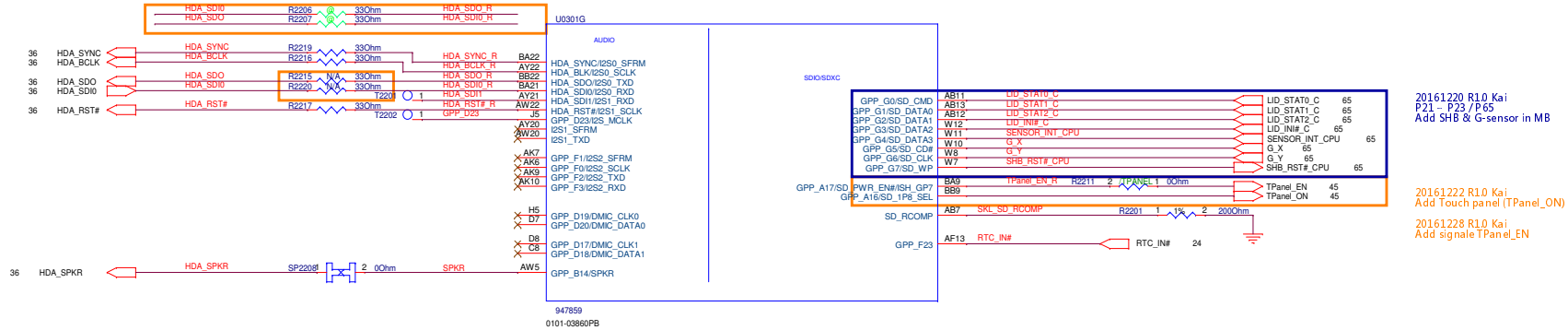
Default is GPO, to reserve pull high to +3VSUS_ORG

PEGATRON Title : PCH(2)_ISH
PEGATRON PROPRIETARY AND CONFIDENTIAL
RGT-HWS RD Engineer: James_Liao
Size C | Project Name SU4EA | Rev 1.0
Date: Monday, March 20, 2017 | Sheet 21 of 94

PCH(3)_HDA_SDIO



Recommended Routing : Stripline < 2"
Alternative Routing : Microstrip <1" (less noise-reduction)

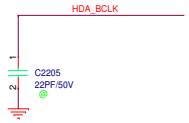


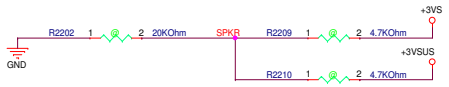
20161220 R1.0 Kai
P21 -- P23 / P65
Add SHB & G-sensor in MB

20161222 R1.0 Kai
Add Touch panel (TPanel_ON)

20161228 R1.0 Kai
Add signale TPanel_EN

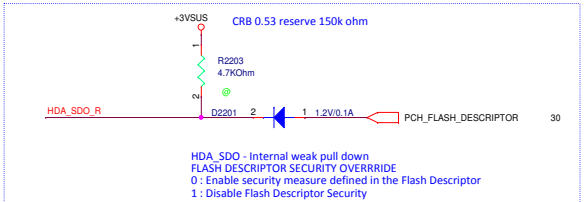
RF requirement





SPKR - Internal weak pull down
0 : Disable TOP Swap mode (default)
1 : Enable Top Swap Enable

Default is GPO, to reserve pull high to +3VSUS_ORG



HDA_SDO - Internal weak pull down
FLASH DESCRIPTOR SECURITY OVERRRIDE
0 : Enable security measure defined in the Flash Descriptor
1 : Disable Flash Descriptor Security

* The signal has a weak internal Pull-down.

Name	P5HCJ_KBL	Description
GPP_B14	0	0 = Disable "Top Swap" mode. (Default) 1 = Enable "Top Swap" mode.
GPP_B18	0	0 = Disable "No Reboot" mode. (Default) 1 = Enable "No Reboot" mode
GPP_B22	0	0 = SPI (Default) 1 = LPC
GPP_C5	0	0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC.
HDA_SDO	0	0 = Enable security measures defined in the Flash Descriptor. (Default) 1 = Disable Flash Descriptor Security (override).
GPP_C2	0	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).
GPP_E19	0	0 = Port B is not detected. (Default) 1 = Port B is detected.
GPP_E21	0	0 = Port C is not detected. (Default) 1 = Port C is detected.

From EDS_Intel_PCH(Skylake.UY_Kabylake.UY)_Vol1_545659_Rev2p0 Page.55-57

PCH(4)_USB/PCIE/SATA

R1.1 remove GPU

U0301H

PCIE/USB3/SATA

SSIC / USB3

USB2

M.2 SATA/PCIE x 4 -SSD

WLAN

M.2 SATA/PCIE x 2 -SSD

PCIE_RCOMP PDG 0.9 need 100 ohm 0.1% / CRB 0.53 use 100 ohm +-1%

Reserve TP for XDP

If SATA driver need change port,
Also must change reltaed "DEVSLP and SATAXPCIE" pin

947859
0101-03860PB

USB3.0 S/C
USB3.0
USB3.0 Type C
USB3.0 Type C
USB3.0 S/C
USB3.0
USB3.0 Type C
USB3.0 Type C
USB20 (IO BD)
Bluetooth
Camera (EDP CONN)
Card reader (IO BD)
FingerPrinter

USB30

20161220 R1.1 Kai
P21 -- P23 / P65
Add SHB & G-sensor in MB

USB2_COMP PDG 1.0 R=113 +-1%
MOW 5.1.3 If the platform does not support Dual Role, then USB2_ID pin shall be connected directly to GND.

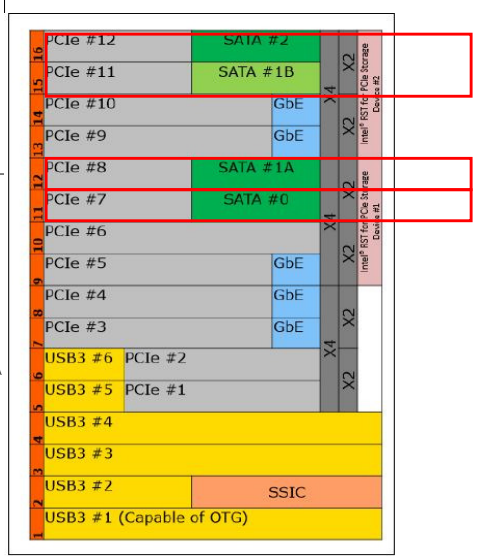
USB30 with USB Chager
USB30
USB20(IO BD)
Type C

SATA SSD1
SATA SSD2

20161227 R1.0 Kai
Add USB Hub connec to SHB / TPanel
Co-lay USB Hub / TPanel

+3VSUS

+3VS



Capture from 545659_545659_SKL_PCH_LP_EDS_Rev1_0_pub
Please refer the latest Doc.

Table 1-2. PCH-LP SKUs (Sheet 2 of 2)

Features	Base-U	Premium-U	Premium-Y
Total Intel® RST capable PCIe and SATA Express[4] Storage Devices	0	2	2

Notes:
1. USB 2.0 port numbers: 1-8
2. USB 2.0 port numbers: 1-10
3. USB 2.0 port numbers: 1-6
4. SATA Express Capable Ports (x2)

Table 1-3. PCH-LP HSIO Detail

SKU	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Base-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe	PCIe	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	SATA	SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A
Premium-U	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	PCIe/ SATA	PCIe/ SATA
Premium-Y	USB 3.0/ OTG	USB 3.0/ SSIC	USB 3.0	USB 3.0	PCIe/ USB 3.0	PCIe/ USB 3.0	PCIe/ LAN	PCIe/ LAN	PCIe/ LAN	PCIe	PCIe/ SATA	PCIe/ SATA	PCIe/ LAN	PCIe/ LAN	N/A	N/A

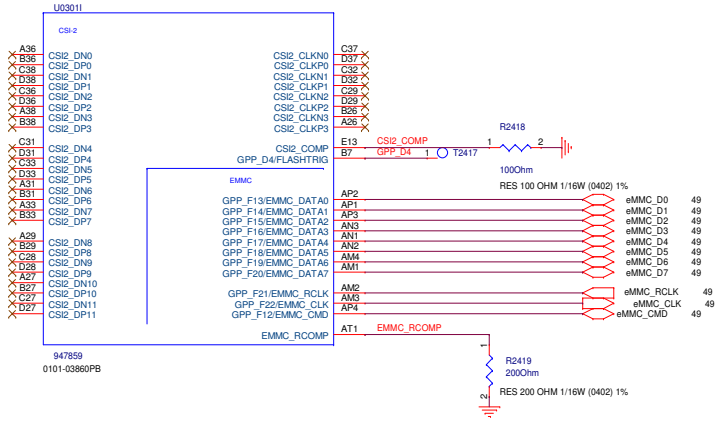
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PCH(4)_USB/PCIE/SATA
ES1-HW3 RD
Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

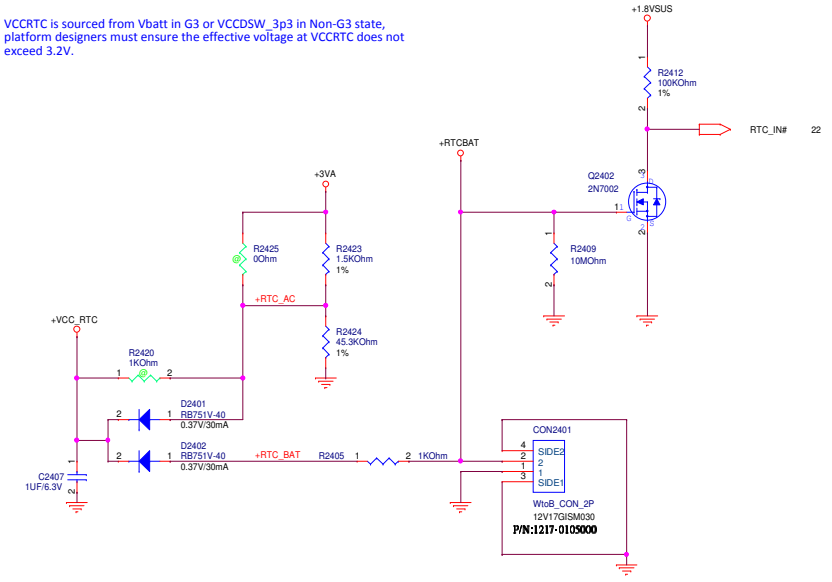
Date: Friday, March 10, 2017 Sheet 23 of 94

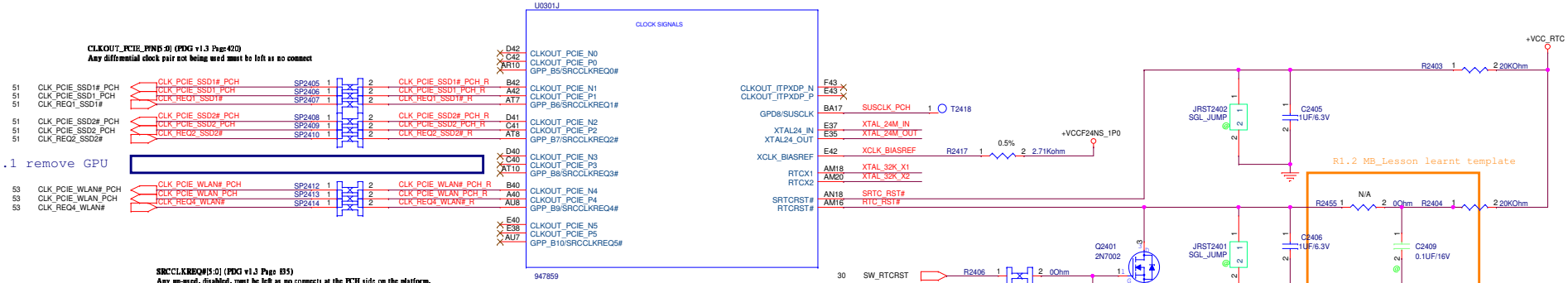
24

PCH(5)_CLK



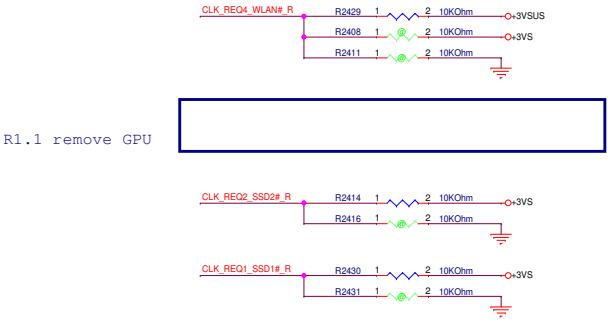
VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V.

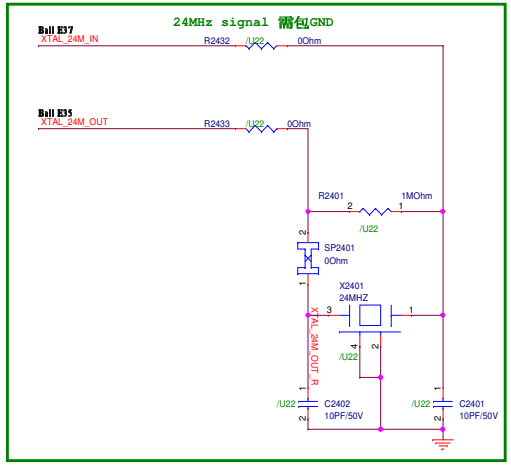


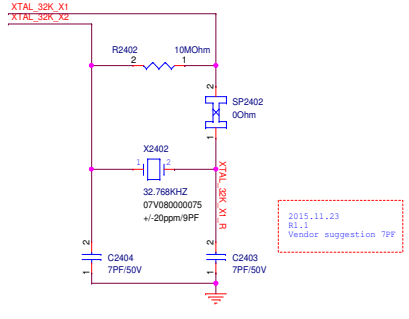


CLKOUT_PCIE_P/N[5:0] (PDG v1.3 Page420)
Any differential clock pair not being used must be left as no connect

R1.1 remove GPU







2015.11.23
R1.1
Vendor suggestion 7PF

PEGATRON Title PCH(5)_CLK
PEGATRON PROPRIETARY AND CONFIDENTIAL
RGT-HWS RD
Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 24 of 94

PCH(6)_POWER MANAGE

In Table 42-1 of PDG (#561280, Rev1p0)
PROCPWRGD is PCH to CPU, but KBL-U don't has this pin at CPU side.
we assume it's conted in MCP package.
So follow CRB to reserve TP only.

U0301K
SYSTEM POWER MANAGEMENT
947859
0101-03860PB

ALL_SYS_PWRGD delay 99 ms from EC

DSW function / non-AMT

If Deep Sx is not implemented on the platform, this signal may be left as no connect

internal pull high

PCH_PWROK logic

SLP_S3# and SLP_S4# logic

R1.2 MB_Lesson learnt template

20161227 R1.1 Kai Correct location

For Intel power sequence requestment
ALL_SYS_PWRGD to Delay_ALL_SYS_PGD >2ms
Delay By EC(2ms+ EC processing time (3ms~33ms)

For shut down Sequence
Tplt17 < 1us

SYS_PWROK logic

internal pull high

Set to GPI

VCCST_PWRGD logic

R1.1 mount

+VDDQ/+VCCST_CPU/+VCCSTG to VCCST_PWRGD must > 1ms

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : PCH(6)_POWER MANAGE
BSI-HW3 RD
Engineer: James_Liao
Size: C | Project Name: SU4EA | Rev: 1.0
Date: Friday, March 10, 2017 | Sheet 25 of 94

26 PCH(7)_POWER

Table 10-5. SKL U / SKL Y PCH-LP
VCCMPHY_1p0 Icc Adder Per HSIO Lane

Icc (A)	Details
0.064	All HSIO disabled.
0.154	Each PCIe Gen3 Lane
0.102	Each PCIe Gen2 Lane
0.132	Each USB3 Port
0.099	SSIC
0.044	GbE Port
0.132	Each SATA Gen3 Port

PCIe Gen3 Lane X10
USB3 Port X3
All HSIO disabled (basic comsunption)
=0.154x10+0.132x3+0.064
=2 A

+1.0VSUS 4A R2640 0Ohm 2A +VCCMPHYGTAON_1P0_LS_SIP
R2637 0Ohm 0.642A +VCCSRAM_1P0
R2638 0Ohm 0.088A +VCCAMPHYPLL_1P0
R2639 0Ohm 0.033A +VCCAPLLEBB_1P0
S1V080500001 S1V040200001 C2628 0.1UF/16V

R1.2 MB_Lesson learnt template

+1.0VSUS_ORG near AB19 C2601 1UF/6.3V vx_c0402_small
+VCCPRIM_CORE near AF18 C2602 1UF/6.3V vx_c0402_small
+1.0VSUS_ORG near K17 C2603 1UF/6.3V vx_c0402_small

2.574A
Decoupling cap for internal power
+VCCDSW_1P0 C2604 1UF/6.3V near AL1

+VCCMPHYGTAON_1P0_LS_SIP 2A
C2605 47UF/6.3V near N15 C2606 1UF/6.3V near N15
+VCCAMPHYPLL_1P0 near K15 C2607 1UF/6.3V vx_c0402_small

R1.2 MB_Lesson learnt template

+1.0VSUS_ORG R2648 0Ohm C2644 0.1UF/16V +VCCPDSW_3P3
+VCCAPLL_1P0_SOC +VCCPAZIO_SOC +VCCSRAM_1P0 +VCCPRIM_3P3_1 +VCCPRIM_1P0_6
+3VSUS_ORG near V19 C2611 1UF/6.3V vx_c0402_small
+VCCAPLLEBB_1P0 near N18 C2612 1UF/6.3V
+1.0VSUS_ORG R2649 0Ohm C2645 0.1UF/16V

R1.2 MB_Lesson learnt template

U0301O
CPU POWER 4 OF 4

0.696A	AB19	VCCPRIM_1P0_1	
	AB20	VCCPRIM_1P0_2	
	P18	VCCPRIM_1P0_3	
	AF18	VCCPRIM_CORE_1	
	AF19	VCCPRIM_CORE_2	
	V20	VCCPRIM_CORE_3	
	V21	VCCPRIM_CORE_4	
	AL1	DCPDSW_1p0	
0.022A	K17	VCCMPHYAON_1P0_1	
	L1	VCCMPHYAON_1P0_2	
	N15	VCCMPHYGT_1P0_1	
	N16	VCCMPHYGT_1P0_2	
	N17	VCCMPHYGT_1P0_3	
	P15	VCCMPHYGT_1P0_4	
	P16	VCCMPHYGT_1P0_5	
0.088A	K15	VCCAMPHYPLL_1P0_1	
	L15	VCCAMPHYPLL_1P0_2	
0.026A	V15	VCCAPLL_1P0	
0.696A	AB17	VCCPRIM_1P0_4	
	Y18	VCCPRIM_1P0_5	
0.118A	AD17	VCCDSW_3p3_1	
	AD18	VCCDSW_3p3_2	
	AJ17	VCCDSW_3p3_3	
0.068A	AJ19	VCCHDA	
0.011A	AJ16	VCCSPI	
0.642A	AP20	VCCSRAM_1P0_1	
	AP21	VCCSRAM_1P0_2	
	T19	VCCSRAM_1P0_3	
	T20	VCCSRAM_1P0_4	
0.075A	AJ21	VCCPRIM_3p3_1	
0.696A	AK20	VCCPRIM_1P0_6	
0.033A	N18	VCCAPLLEBB_1P0	

947859
0101-03860PB

VCCPGPPA	AK15	0.02A	
VCCPGPPB	AG15	0.004A	
VCCPGPPC	Y16	0.006A	
VCCPGPPD	Y15	0.008A	
VCCPGPPE	T16	0.006A	
VCCPGPPF	AF16	0.161A	
VCCPGPPG	AD15	0.0031A	
VCCPRIM_3p3_2	V19	0.075A	
VCCPRIM_1P0_7	T1	0.696A	
VCCATS_1p8	AA1	0.006A	
VCCRTCPRIM_3p3	AK17	0.001A	
VCCRTC_1	AK19		
VCCRTC_2	BB14		
DCPRTC	BB10		
VCCCLK1	A14	0.035A	
VCCCLK2	K19	0.029A	
VCCCLK3	L21	0.024A	
VCCCLK4	N20	0.033A	
VCCCLK5	L19	0.004A	
VCCCLK6	A10	0.0039A	
GPP_B0/CORE_VID0	AN11		
GPP_B1/CORE_VID1	AN13		

R2646 1KOhm R2647 1KOhm
Intel confirm pull down 1k

+3VSUS_ORG
C2613 vx_c0402_small 2 1UF/6.3V near Y16
C2614 vx_c0402_small 2 1UF/6.3V near T16
+1.8VSUS_ORG
R1.2 MB_Lesson learnt template
R2650 0Ohm C2646 0.1UF/16V
+V1.8A_SIP R2624 0Ohm S1V040200001 C2615 1UF/6.3V near AA1
+1.0VSUS_ORG
C2625 1UF/6.3V near AK17 C2617 1UF/6.3V near AK17 C2618 1UF/6.3V near AK17
C2634 2 1UF/6.3V near AK19 GND
+VCC_RTC
VCCRTCEXT C2620 2 1UF/6.3V near BB10 GND
C2619 2 1UF/6.3V near AK19 GND

+VCC19P2_1P0 R2627 0Ohm S1V040200001 +1.0VSUS_ORG
+VCCF100_1P0 R2628 0Ohm S1V040200001 +1.0VSUS_ORG
+VCCF135_1P0 R2629 0Ohm S1V040200001 +1.0VSUS_ORG
+VCCF100OC_1P0 R2630 0Ohm S1V040200001 +1.0VSUS_ORG
+VCCF24NS_1P0 R2631 0Ohm S1V040200001 +1.0VSUS_ORG
+VCC24TBT_1P0 R2632 0Ohm S1V040200001 +1.0VSUS_ORG
near A10
C2624 1UF/6.3V vx_c0402_small

+1.0VSUS R2604 0Ohm +VCCAPLL_1P0
C2608 47uF/6.3V C2636 0.1UF/16V
B2601 09V010000096 75OHM
C2640 2PF/25V NPO/+/-0.25PF vx_c0201 C2641 2PF/25V NPO/+/-0.25PF vx_c0201
+VCCAPLL_1P0_SOC near V15 GND

+3VSUS R2602 0Ohm S1V040200001 +VCCPAZIO
C2609 1UF/10V C2637 0.1UF/16V
B2602 09V010000096 75OHM
C2642 2PF/25V NPO/+/-0.25PF vx_c0201 C2643 2PF/25V NPO/+/-0.25PF vx_c0201
+VCCPAZIO_SOC near AJ19 GND

EMI request for Kaby Lake
Recommended Routing : Stripline < 2"
Alternative Routing : Microstrip <1"
(less noise reduction)

+3VSUS R2601 0Ohm S1V040200001 0.5A +3VSUS_ORG
+1.0VSUS R2603 0Ohm S1V060300001 1A +1.0VSUS_ORG
+1.8VSUS R2605 0Ohm S1V040200001 0.5A +1.8VSUS_ORG

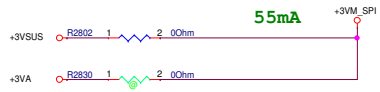
R1.1 USB short mount
R2636 0Ohm
+3VSUS Q2601 PJA3411 +VCCPDSW_3P3
R2635 100KOhm N/A
Q2602 BC856BS N/A
R2634 100KOhm N/A

PEGATRON Title PCH(7)_POWER
PEGATRON PROPRIETARY AND CONFIDENTIAL
Engineer: James_Liao
Size C | Project Name SU4EA | Rev 1.0
Date: Friday, March 10, 2017 | Sheet 26 of 94

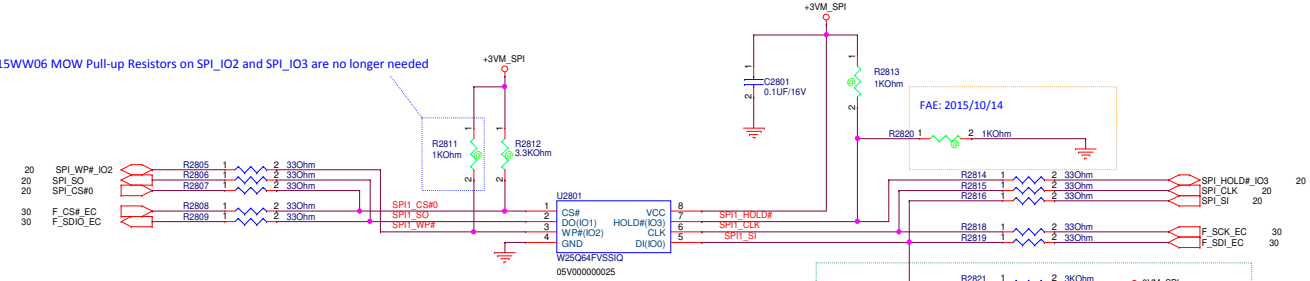
Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	27 of 94

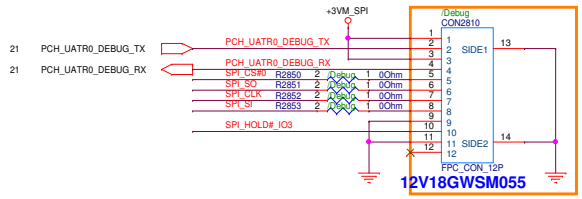
28

PCH(9)_SPI_SMB

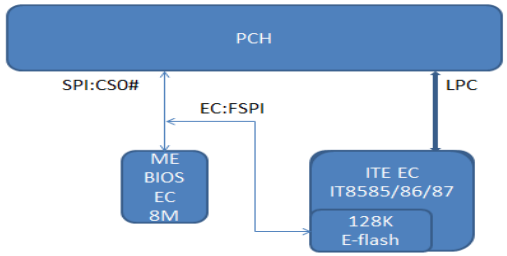


15WW06 MOW Pull-up Resistors on SPI_IO2 and SPI_IO3 are no longer needed

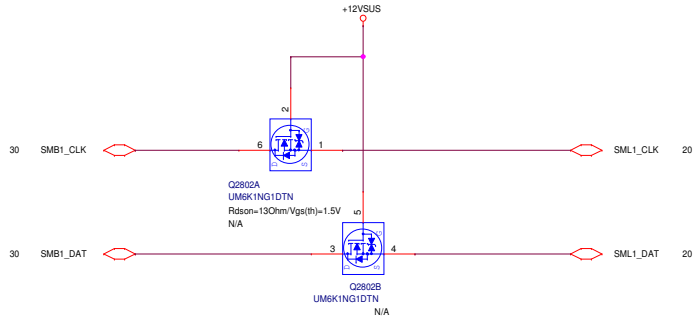




SPI ROM size		
T-pad function	P/N	Size
NON-POA ★	05V000000025	8M
POA	05V000000031	16M



PCH SMBus



EC

GPU

PCH

PEGATRON Title : PCH(9)_SPI_SMB

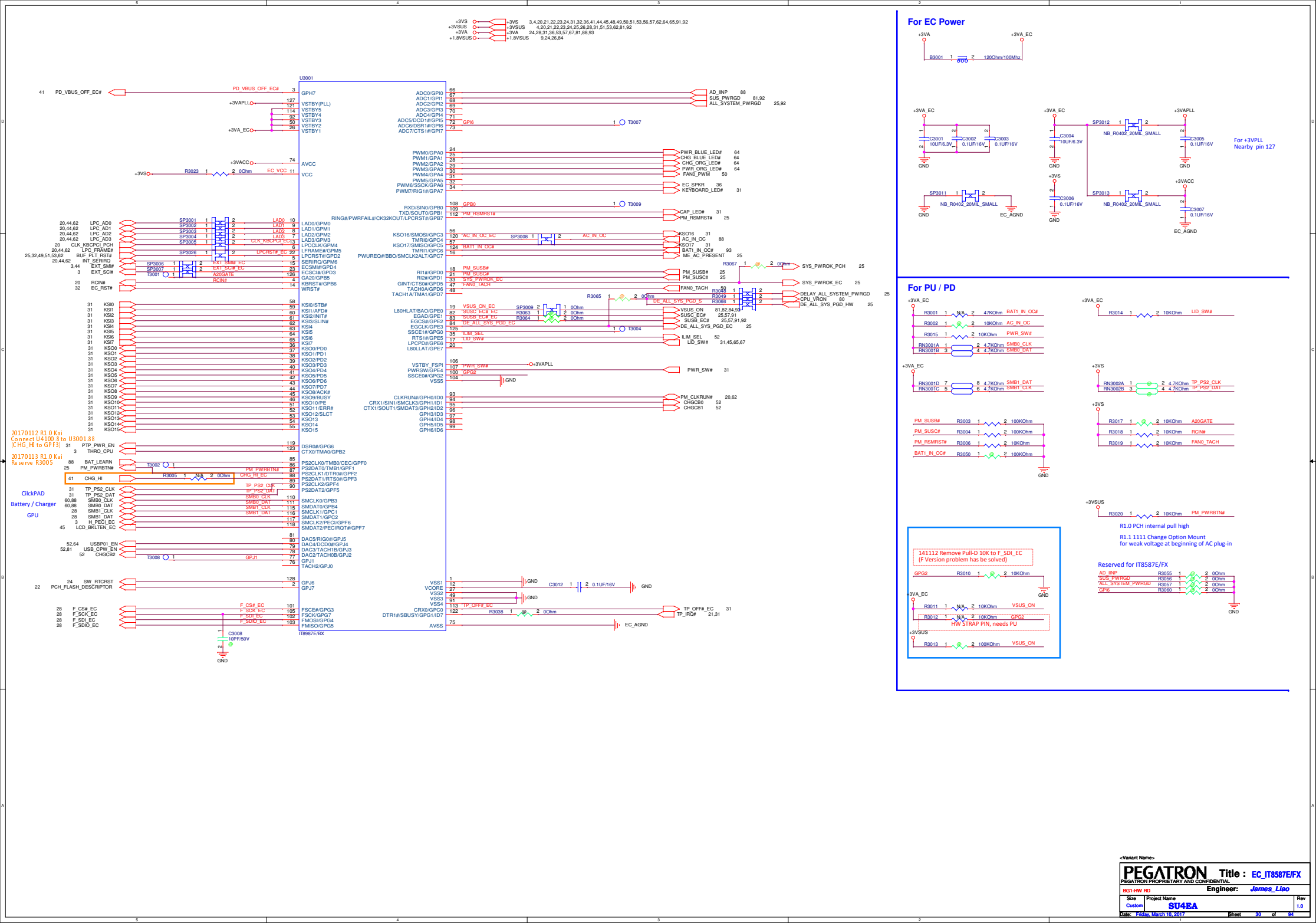
PEGATRON PROPRIETARY AND CONFIDENTIAL

RST-HW3 RD Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

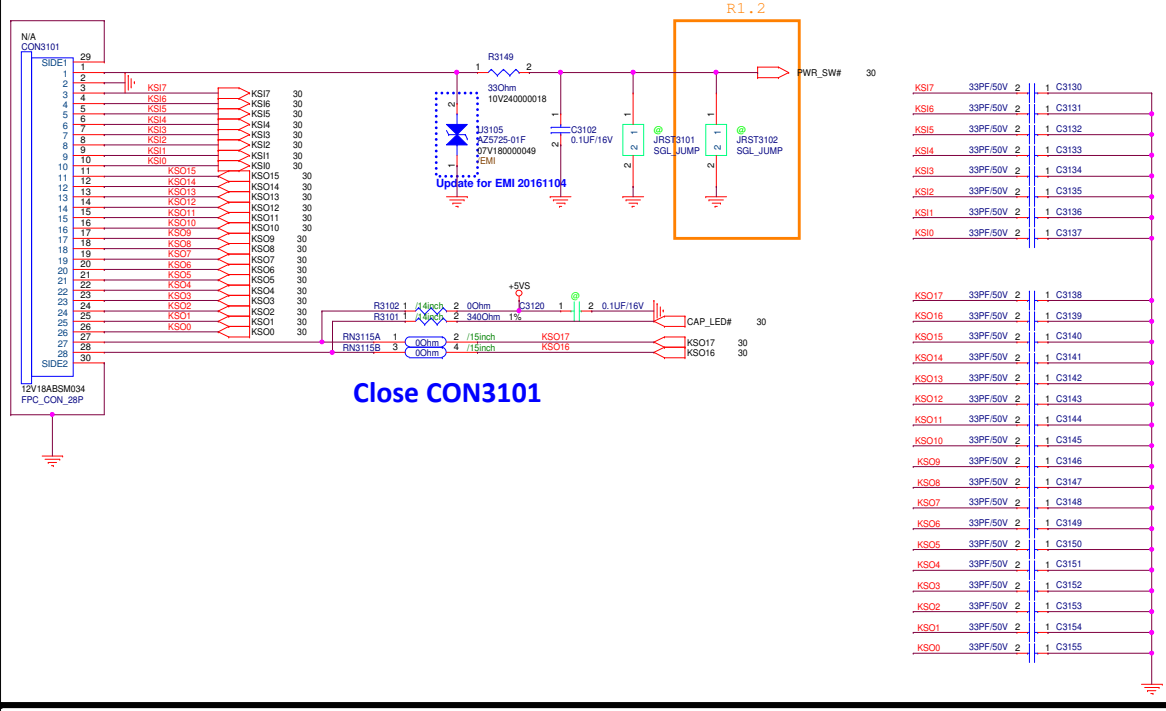
Date: Friday, March 10, 2017 Sheet 28 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	29 of 94

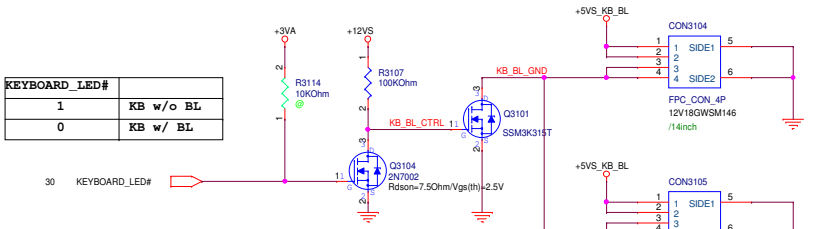

+3VS 3,4,20,21,22,23,24,31,32,36,41,44,45,48,49,50,51,53,56,57,62,64,65,91,92
+3VSUS 4,20,21,22,23,24,25,26,28,31,51,53,62,81,92
+3VA 24,28,31,36,53,57,67,81,88,93
+1.8VSUS 9,24,26,84
U3001
IT8987E/BX
For EC Power
B3001 120Ohm/100Mhz
For +3VPLL
Nearby pin 127
NB_R0402_20MIL_SMALL
For PU / PD
141112 Remove Pull-D 10K to F_SDI_EC
(F Version problem has be solved)
HW STRAP PIN, needs PU
R1.0 PCH internal pull high
R1.1 1111 Change Option Mount
for weak voltage at beginning of AC plug-in
Reserved for IT8587E/FX
20170112 R1.0 Kai
Connect U4100.8 to U3001.88
(CHG_HI to GPF3)
20170113 R1.0 Kai
Reserve R3005
ClickPAD
Battery / Charger
GPU
<Variant Name>
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title : EC_IT8587E/FX
BG1-HW RD
Engineer: James_Liao
Size Custom
Project Name SU4EA
Rev 1.0
Date: Friday, March 10, 2017
Sheet 30 of 84

31 KB_TP

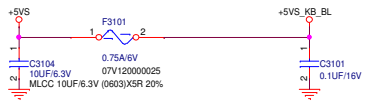
Keyboard Backlight

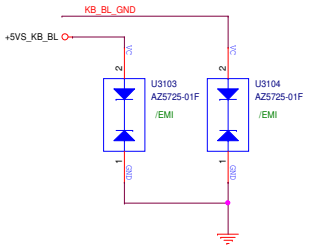


KEYBOARD_LED#	
1	KB w/o BL
0	KB w/ BL

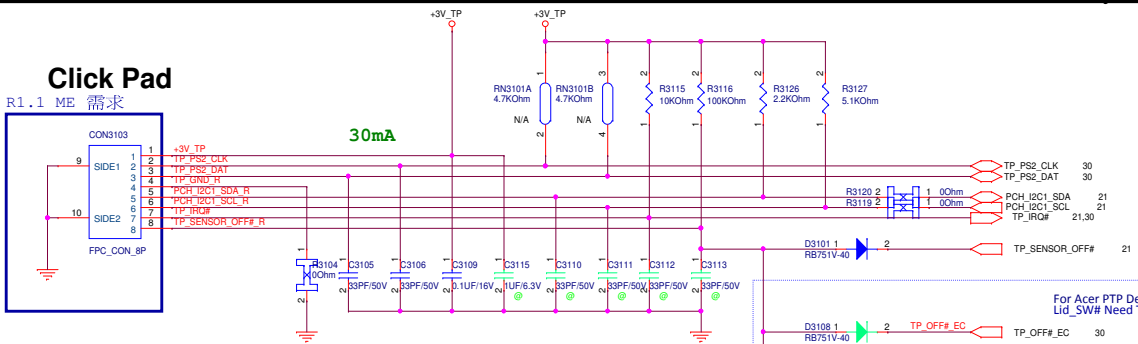


+5VS_KB_BL trace >20mils

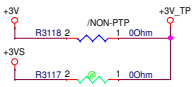


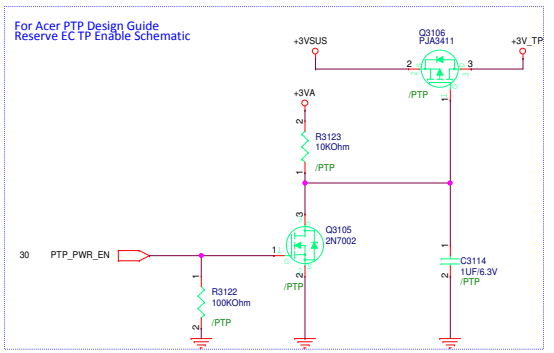


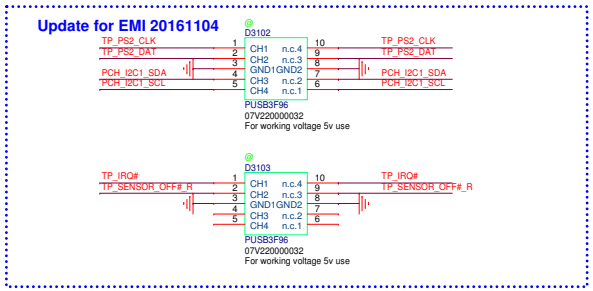
Click Pad



Touch Pad Wake Up S3







PEGATRON

Title : KB_TP

BG1-HW3 RD

Engineer: James_Liao

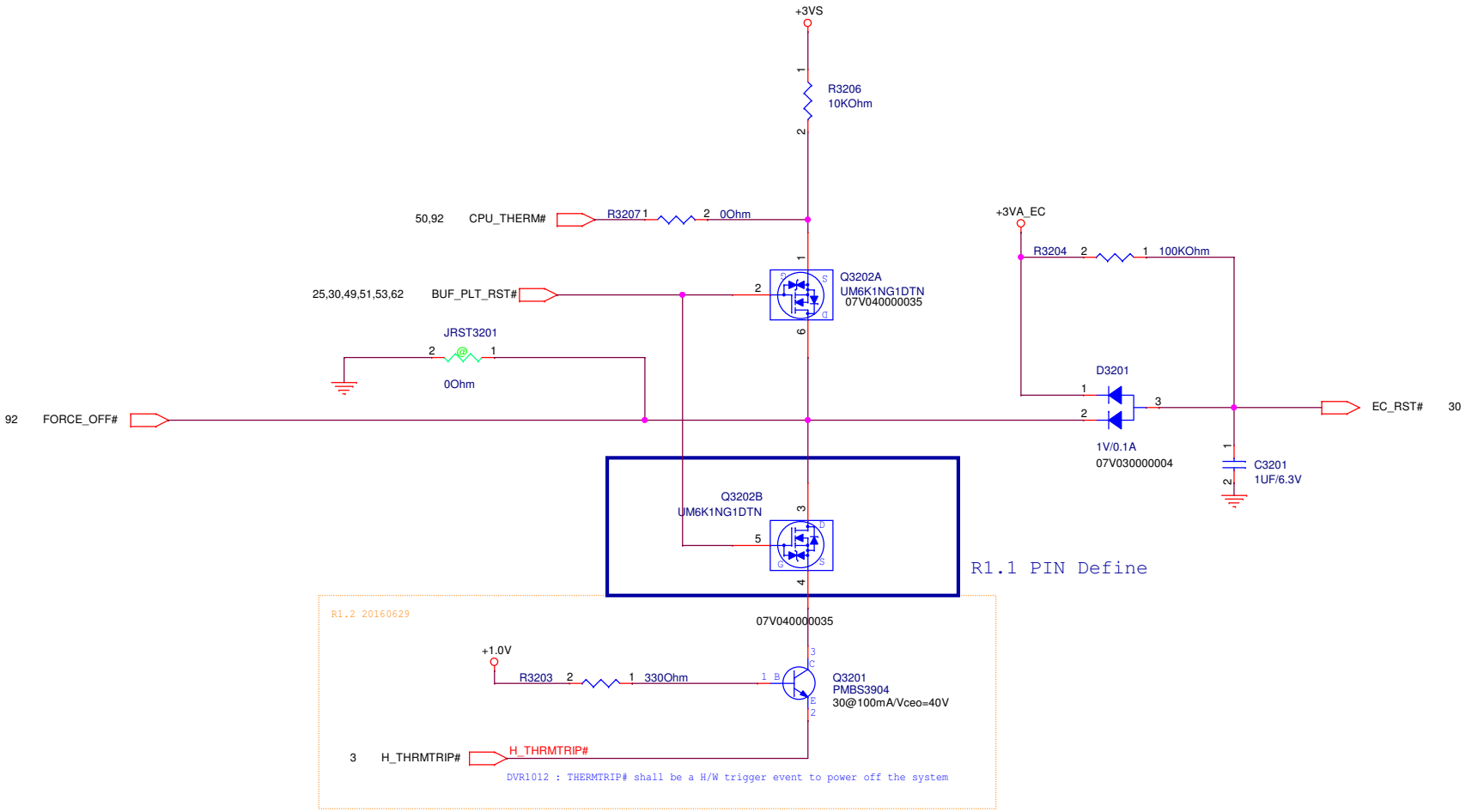
Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 31 of 94

32 RST_Reset Circuit

+3VA_EC <-> +3VA_EC 30

+3VS <-> +3VS 3,4,20,21,22,23,24,30,31,36,41,44,45,48,49,50,51,53,56,57,62,64,65,91,92



PEGATRON

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BG1-HW3 RD

Title : RST_Reset Circuit

Engineer: James_Liao

Size	Project Name	Rev
B	SU4EA	1.0

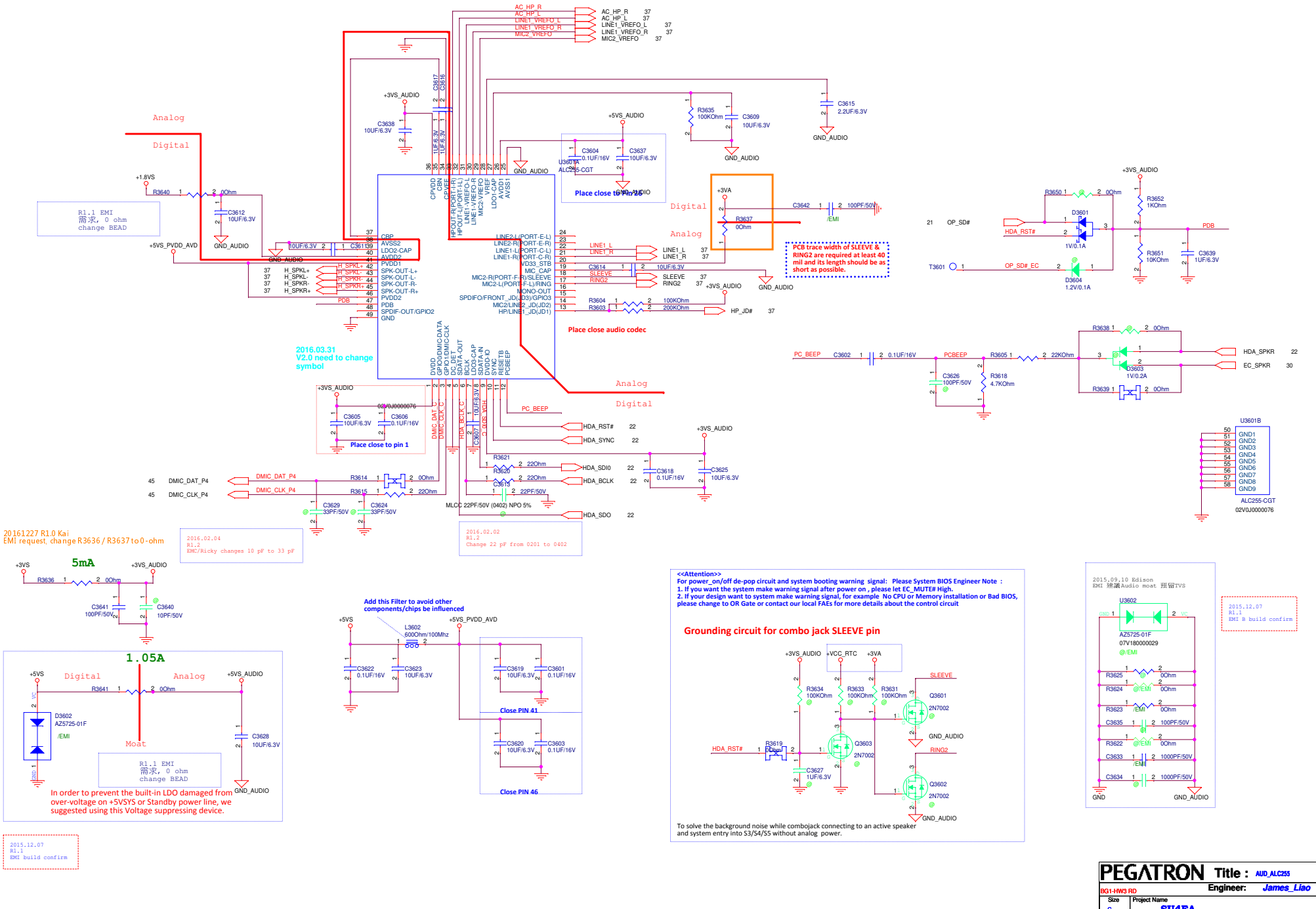
Date: Friday, March 10, 2017 Sheet 32 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	33 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	34 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	35 of 94

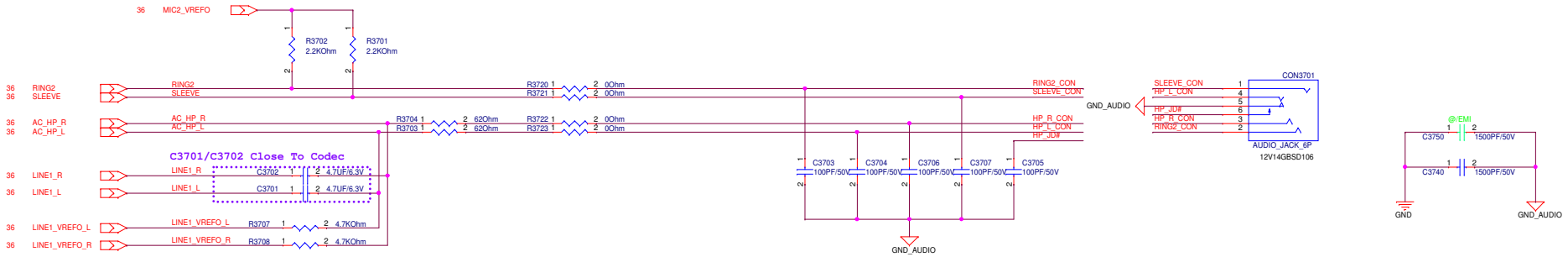
AUD_ALC255



PEGATRON	Title : AUD_ALC255		
BG1-HW3 RD	Engineer: James_Liao		
Size: C	Project Name: SU4EA		Rev: 1.0
Date: Friday, March 10, 2017	Sheet 36 of 94		

AUD_HP/SPK

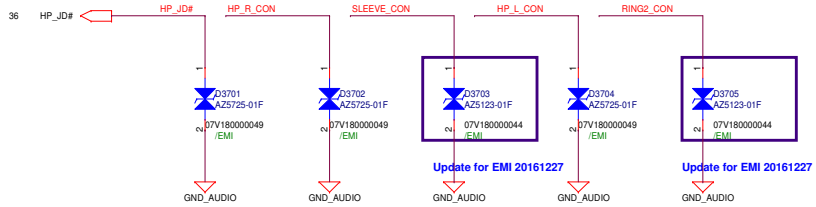
Universal Audio Jack



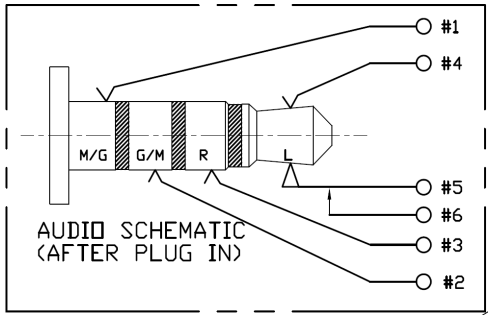
Close to CON3701

20161227 R1.0 Kai
Change D3703 / D3705 to VX

20160225 EMI suggest



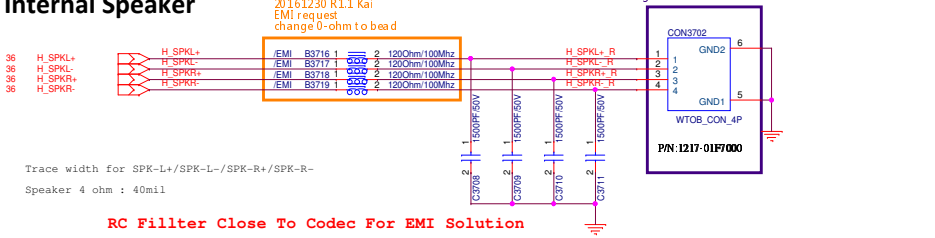
12V14GBSD104, sch. 20161031 updated



Internal Speaker

20161230 R1.1 Kai
EMI request
change 0-ohm to bead

20161229 R1.1 Kai
ME request
change CON3702 from 12V17GRM002 to 12V17ABSM000



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-

Speaker 4 ohm : 40mil

RC Fillter Close To Codec For EMI Solution

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
RST-HW3 RD

Title : AUD_HP/DMIC/SPK
Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

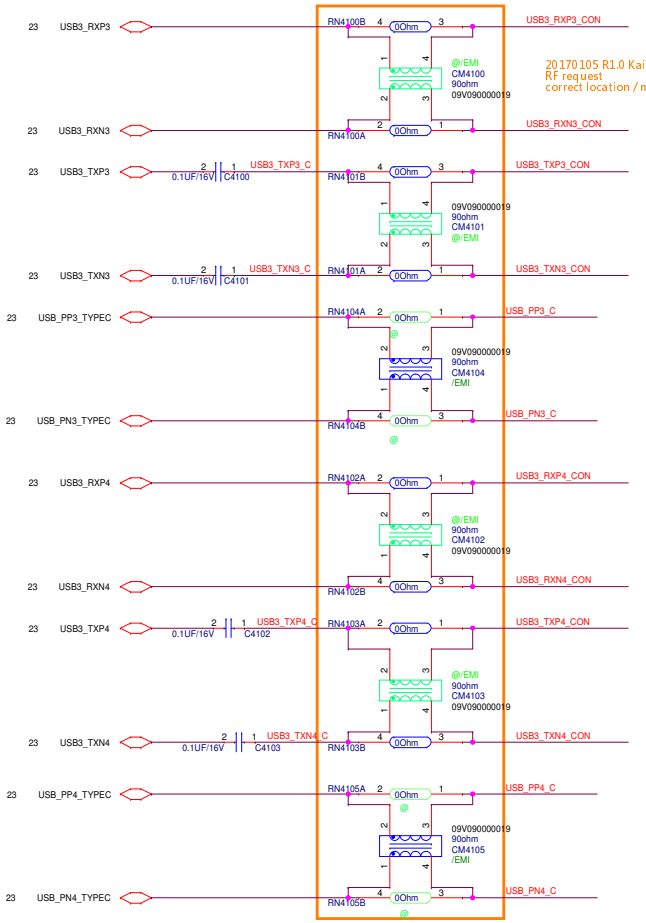
Date: Friday, March 10, 2017 Sheet 37 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	38 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	39 of 94

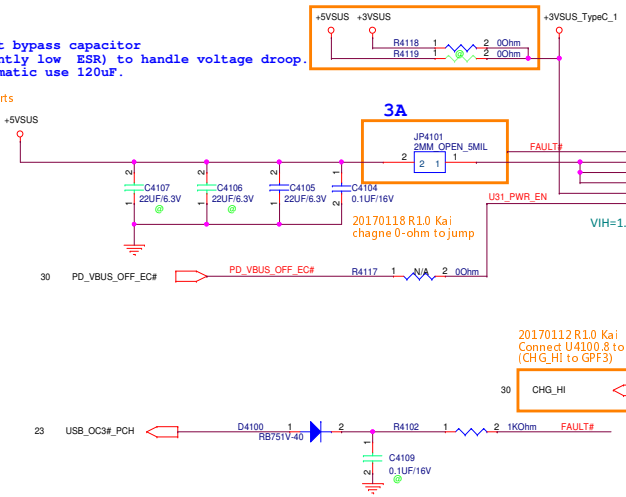
Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	40 of 94

USB3.1 Type C TPS25810

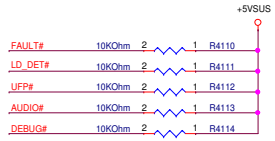


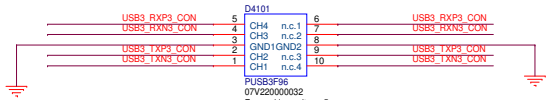
20170105 R1.0 Kai
RF request
correct location / mount parts / change parts

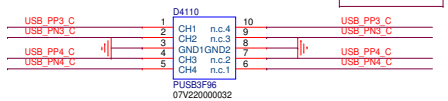
Need sufficient bypass capacitor (with sufficiently low ESR) to handle voltage droop. Reference schematic use 120uF.

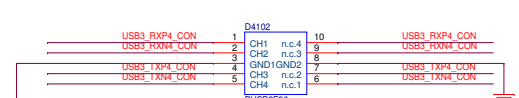


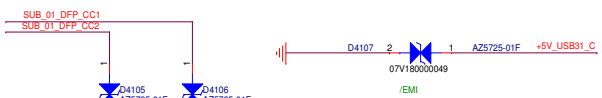
FAULTb pin is an open drain output that assert (active low) when device OUT current exceeds its programmed value and/or over temperature threshold is cressed.

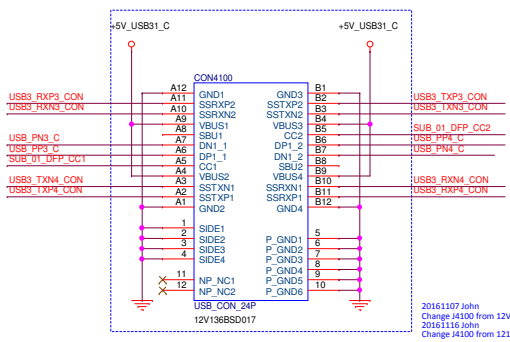






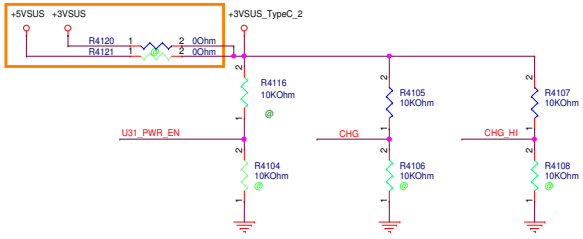




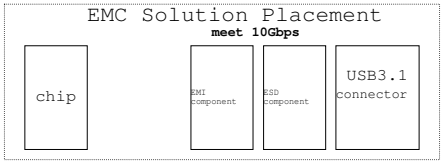


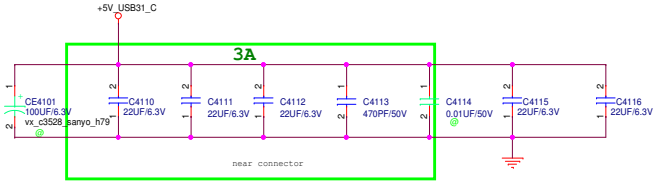
20161107 John
Change J4100 from 12V136BSD015 to 1213-02DG000
20161116 John
Change J4100 from 1213-02DG000 to 12V136BSD017

12V136BSD017



A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	Vbus	CC1	D+	D-	SBU1	Vbus	RX2-	RX2+	GND
GND	RX1+	RX1-	Vbus	SBU2	D-	D+	CC2	Vbus	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1





USB3 Connector(Diff. Z = 85 ohm)

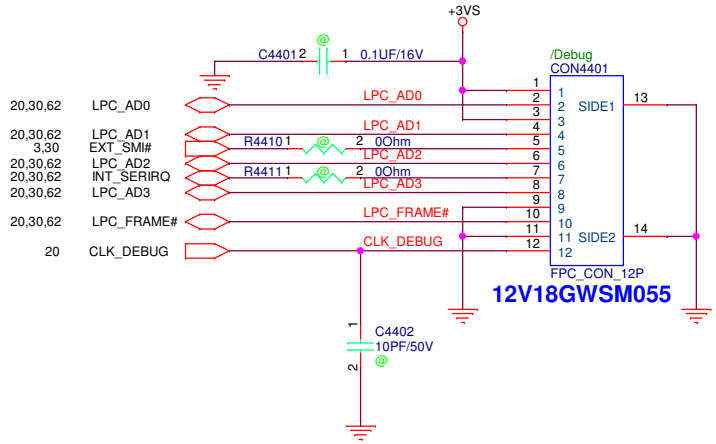
PEGATRON	Title	USB3.1 TPS25810
PEGATRON PROPRIETARY AND CONFIDENTIAL		
EG1-NB4	Engineer:	James_Liao
Size: Custom	Project Name: SU4EA	Rev: 1.0
Date: Friday, March 17, 2017	Sheet 41 of 94	

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	42 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	43 of 94

44

DEBUG CONN



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : DEBUG CONN.

BG1-HW3 RD

Engineer: James_Liao

Size	Project Name	Rev
B	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 44 of 94

Controller circuit

EC

30 LCD_BKLTEN_EC
30,31,65,67 LID_SW#

CPU

3,21 LCD_BKLTEN_PCH

R4568 0Ohm eDP_BL_EN_R

D4502 1V/0.1A

D4501 RB751V-40

R4507 100KOhm

+LCD_VCC

R4506 10KOhm

BACK_EN_C

C4500 100PF/50V @

C4546 22PF/25V /EMI

20161227 R1.0 Kai
Change R4568 package size from 0805 to 0402
from 10V440000001 to 10V240000001

3 LCD_BL_PWM_PCH

B4502 1kOhm/100Mhz

LCD_BL_PWM_C

C4501 100PF/50V

C4545 22PF/25V /EMI

LCD_VCC for eDP

+LCD_VCC

C4502 4.7UF/6.3V

R4560 0Ohm +LCD_VCC_OUT

U4501 G5244T11U
OUT IN GND EN DSG

+3VS

R4508 150Ohm +LCD_VCC_OUT

C4503 1UF/6.3V

CPU 3 eDP_VDD_EN

R4572 0Ohm DP_VDD_EN_R

R4509 100KOhm

+3VS +3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,48,49,50,51,53,56,57,62,64,65,91,92
+AC_BAT_SYS +AC_BAT_SYS 80,81,82,83,88
+3V +3V 25,31,57,63,65,91
+5VS +5VS 31,36,48,50,57,69,80,91

Check PCH/FCH or CPU PD

AC_INV

C4506 39PF/50V @

C4507 0.1UF/25V

C4508 1UF/25V

+AC_BAT_SYS

B4505 80Ohm/100Mhz Irat=2A

B4503 80Ohm/100Mhz Irat=2A @

Reserve another path for factory request

+LCD_VCC

C4529 47PF/50V

Camera

RN4501B 0Ohm

23 USB_PN7_CCD

23 USB_PP7_CCD

@/EMI CM4506 90Ohm/100MHz 09V090000001

USBP7-

USBP7+

RN4501A 0Ohm

20170105 R1.0 Kai
RF request
correct location / mount parts / change parts

+3V_CAM

+3V B4501 120Ohm/100Mhz

+3VS B4504 120Ohm/100Mhz

C4509 0.1UF/16V

eDP HPD

+3VS

R4541 100KOhm EDP_HPD
R4523 100KOhm LCD_BKLTEN_EC
R4570 100KOhm EDP_AUXN_C
R4503 100KOhm EDP_AUXP_C

Intel Solution

20161227 R1.0 Kai
Add USB Hub connect to SHB / Touch

Touch panel

23 USB_PN10_TP
23 USB_PP10_TP
63 USB_HUB_U20_PN2_Touch
63 USB_HUB_U20_PP2_Touch

R4501 0Ohm
R4513 0Ohm
R4514 0Ohm
R4515 0Ohm

RN4502A 0Ohm /TPANEL

09V090000001 90Ohm/100MHz CM4501 @/EMI

RN4502B 0Ohm /TPANEL

USBHUBP1-
USBHUBP1+

eDP Connector

NOTE:
Entire trace of Panel_VCC & LCD_VCC should be wider than 80-mil

co-lay

CON4501 WTOB_CON_30P

Camera

36 DMIC_DAT_P4
36 DMIC_CLK_P4
USBP7+
USBP7-
+3V_CAM

3 EDP_TXN1
3 EDP_TXP1
3 EDP_TXN0
3 EDP_TXP0
3 EDP_AUXP
3 EDP_AUXN
3 EDP_HPD

0.1UF/16V C4521 EDP_TXN1_C EDP_TXP1_C
0.1UF/16V C4536 EDP_TXN0_C EDP_TXP0_C
0.1UF/16V C4539 EDP_AUXP_C
0.1UF/16V C4540 EDP_AUXN_C

EDP_HPD
BACK_EN_C
LCD_BL_PWM_C
+LCD_VCC
AC_INV

R4512 100KOhm @

SIDE1 36
SIDE2 35
SIDE4 34
SIDE3 33

NP_NC1
NP_NC2

12V37GISM007

20161227 R1.0 Kai

Reserve for USB touch panel
CON4501.8 / CON4501.9 / CON4502.18 / CON4502.19

Add for I2C touch panel
CON4502.4 / CON4502.15

20161222 R1.0 Kai
Add Touch panel / DMIC

不開鋼版

+3VS_Touch

JP4501 1MM_OPEN_M1M2 @/TPANEL

C4510 1UF/6.3V /TPANEL

Q4502 SI2305CDS-T1-GE3 07V040000109 /TPANEL

C4505 @ 0.1UF/16V

R4505 0Ohm
R4502 /TPANEL 0Ohm

+5VS +3VS

R4511 100KOhm /TPANEL

R4510 10KOhm /TPANEL

Q4503B UM6K1NG1DTN /TPANEL

Q4503A UM6K1NG1DTN /TPANEL

TPanel_ON 22

21 I2C2_SDA_PCH
21 I2C2_SCL_PCH

PCH

20161228 R1.0 Kai

Recover CON4501 pin-define
Modify CON4502.1 ~ CON4502.10
Remove TP_LID_SW# circuit
Remove DMIC power
Change TPanel power from +5VS to +3VS

Q4501A UM6K1NG1DTN /TPANEL

Q4501B UM6K1NG1DTN /TPANEL

R4504 10KOhm /TPANEL

R4516 10KOhm /TPANEL

I2C2_SDA_Touch
I2C2_SCL_Touch

TPanel

21 TOUCH_RST#_CPU
21 TOUCH_INT_CPU
22 TPanel_EN
+3VS_Touch

CON4502 WTOB_CON_40P

NP_NC1 41
GND1 43
GND3 45
GND4 46
GND5 47
GND6 48
GND2 44
NP_NC2 42

12V37GISM000

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : LVDS Out

BG1-HW3 RD

Engineer: James_Liao

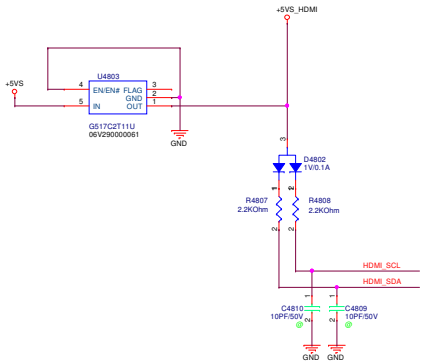
Size	Project Name	Rev
C	SU4EA	1.0

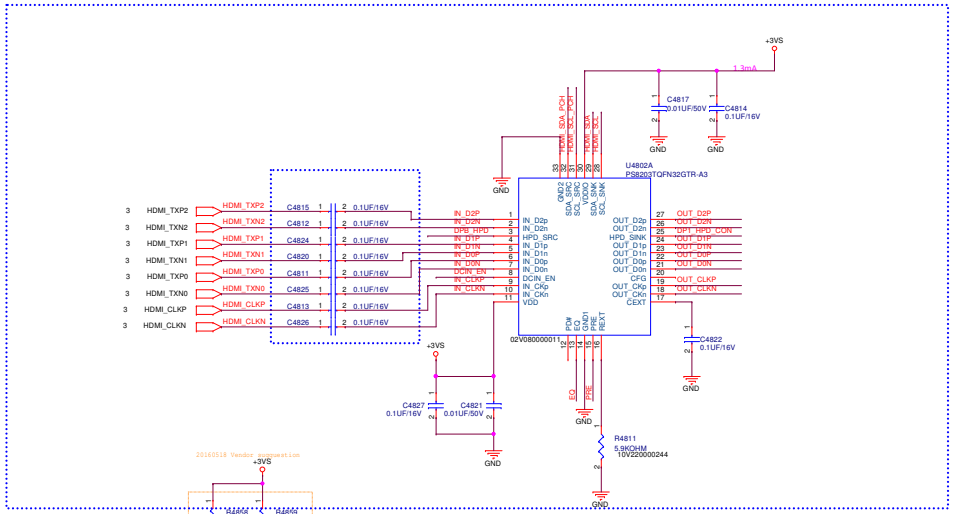
Date: Friday, March 10, 2017 Sheet 45 of 94

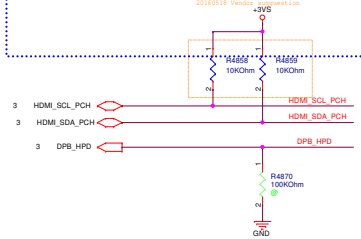
Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	46 of 94

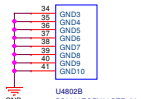
Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	47 of 94

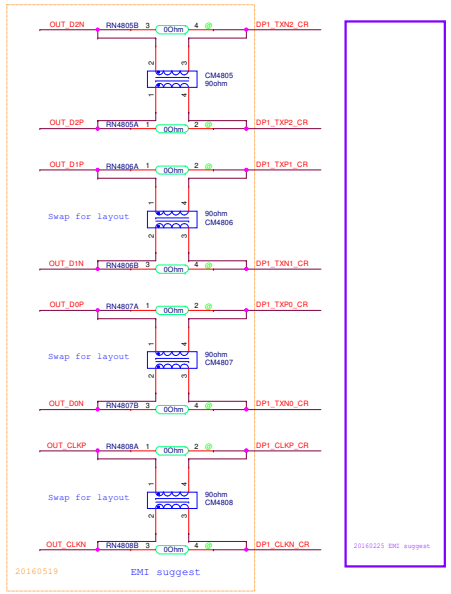
48 HDMI

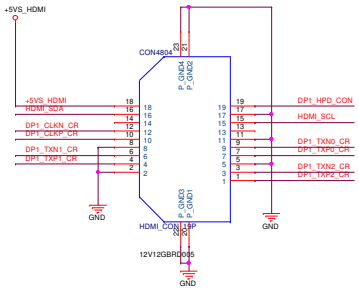


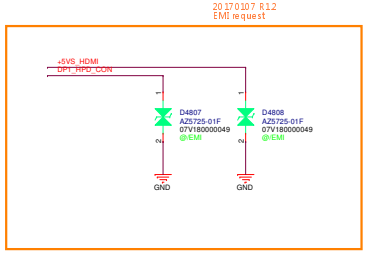


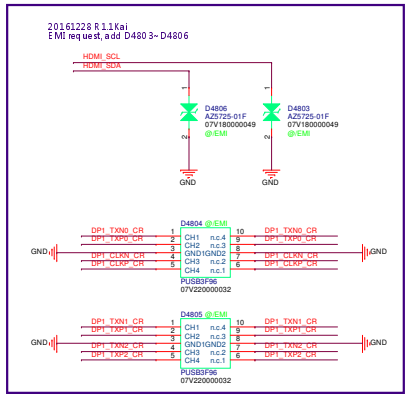








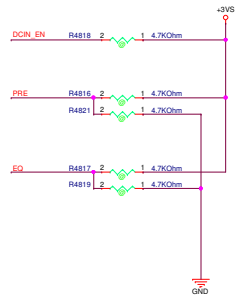


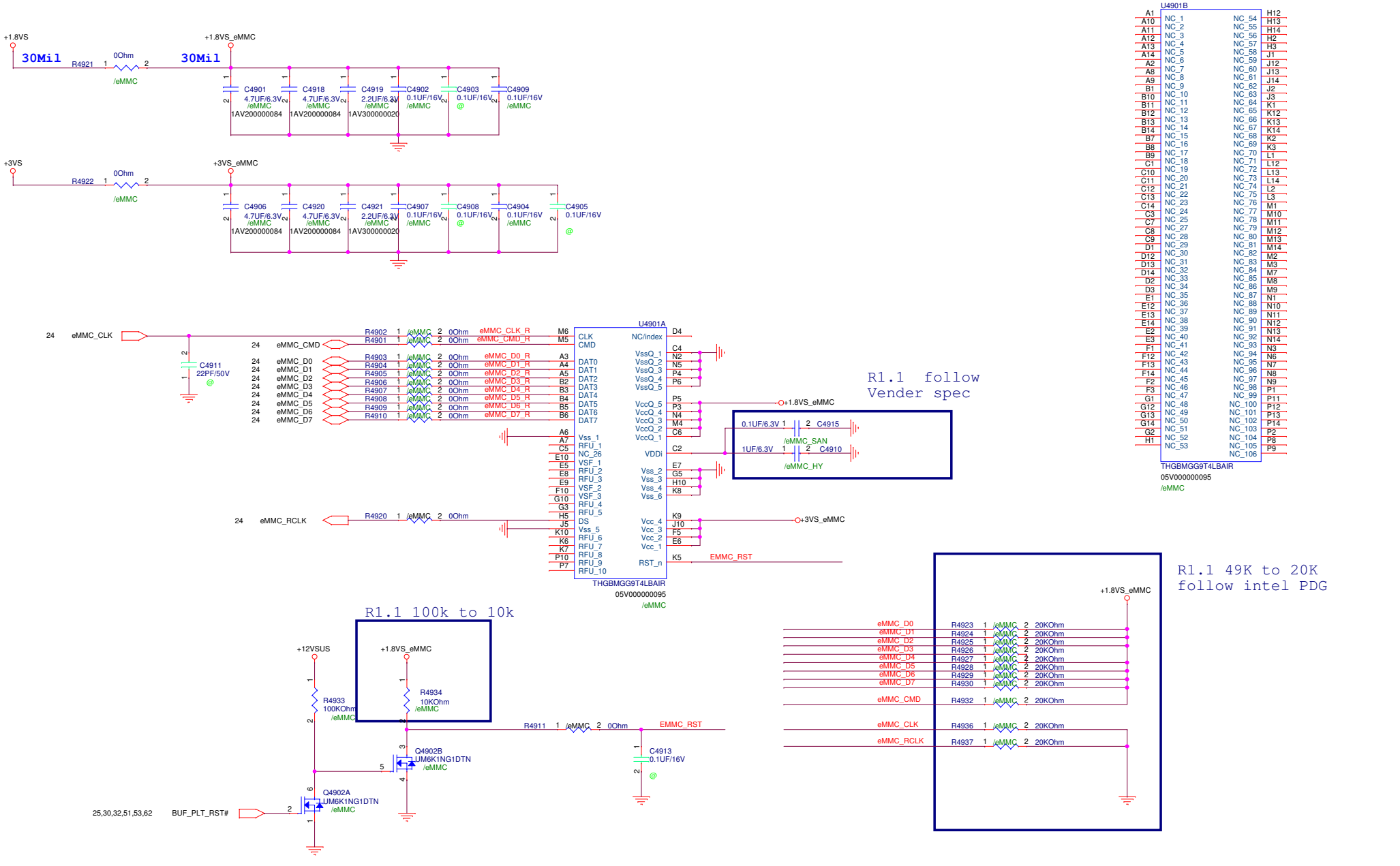



```
Output pre-emphasis setting; Internal pull down at ~150kΩ, 3.3V I/O.
   L: no pre-emphasis
   H: 2.5dB pre-emphasis
```

```
Receiver equalization setting; Internal pull down at ~150kΩ, 3.3V I/O.
   L: programmable EQ for channel loss up to 12.4dB @ 3Gbps
   H: programmable EQ for channel loss up to 4.3dB @ 3Gbps
   M: programmable EQ for channel loss up to 8.6dB @ 3Gbps
```

```
DC cou;ing enable; Internal pull down at ~150kΩ, 3.3V I/O.
   L: default, AC coupling input
   H: DC coupling input
```





<Variant Name>

PEGATRON Title : eMMC

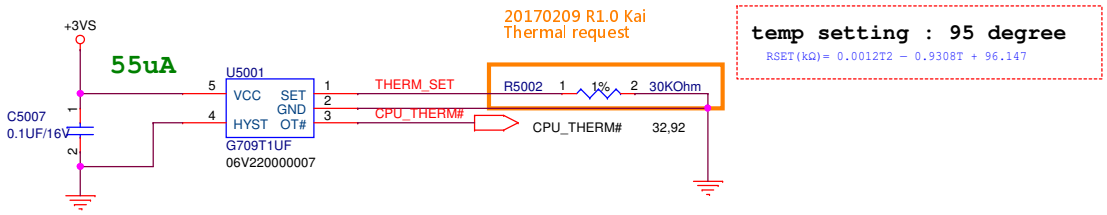
BG1-HW3 RD Engineer: James_Liao

Size	Project Name	Rev
Custom	SU4EA	1.0

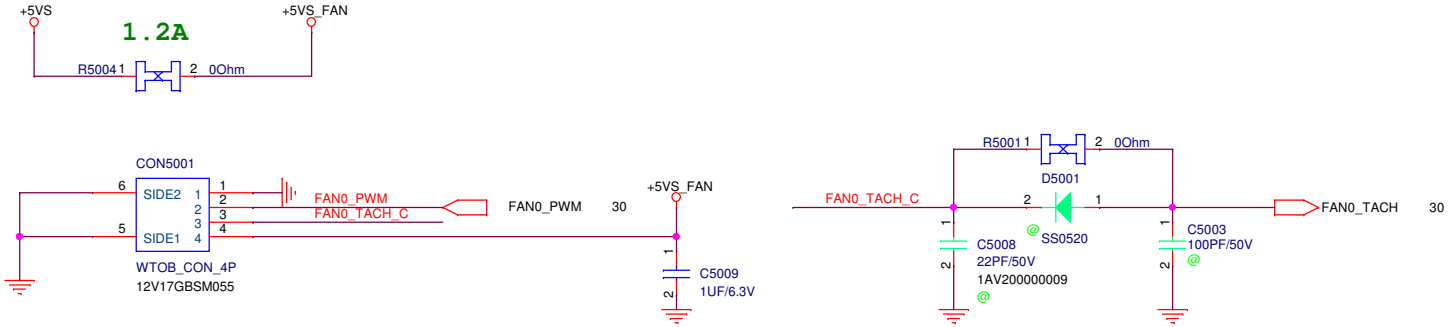
Date: Friday, March 10, 2017 Sheet 49 of 94

50 Thermal_Fan

G709 Thermal Sensor



PWM FAN



PEGATRON Title : Thermal_Fan

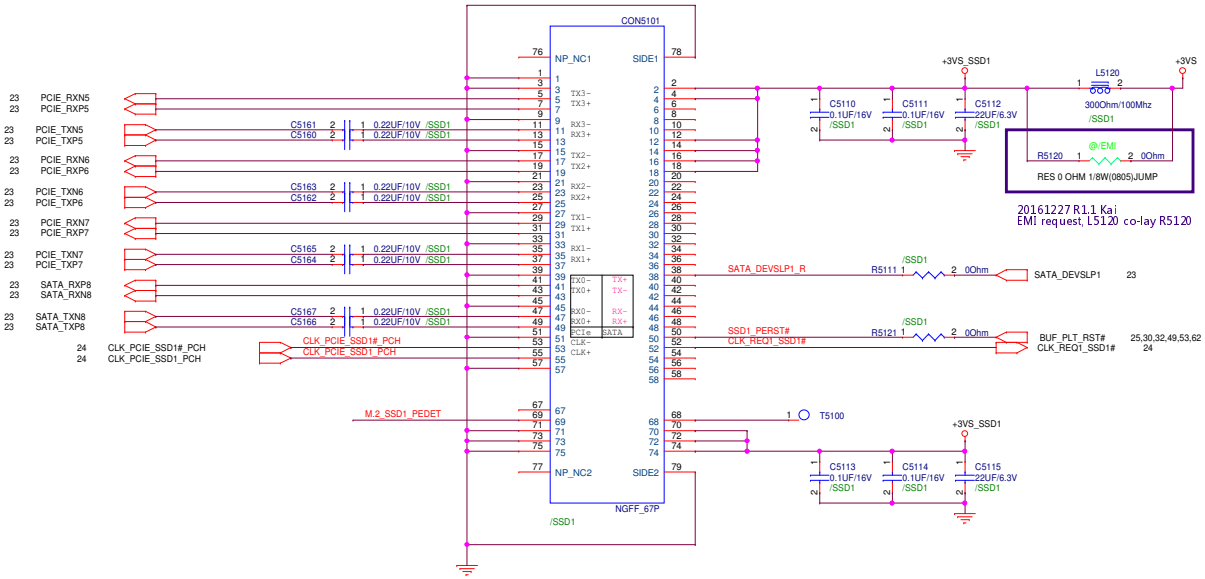
BG1-HW3 RD Engineer: James_Liao

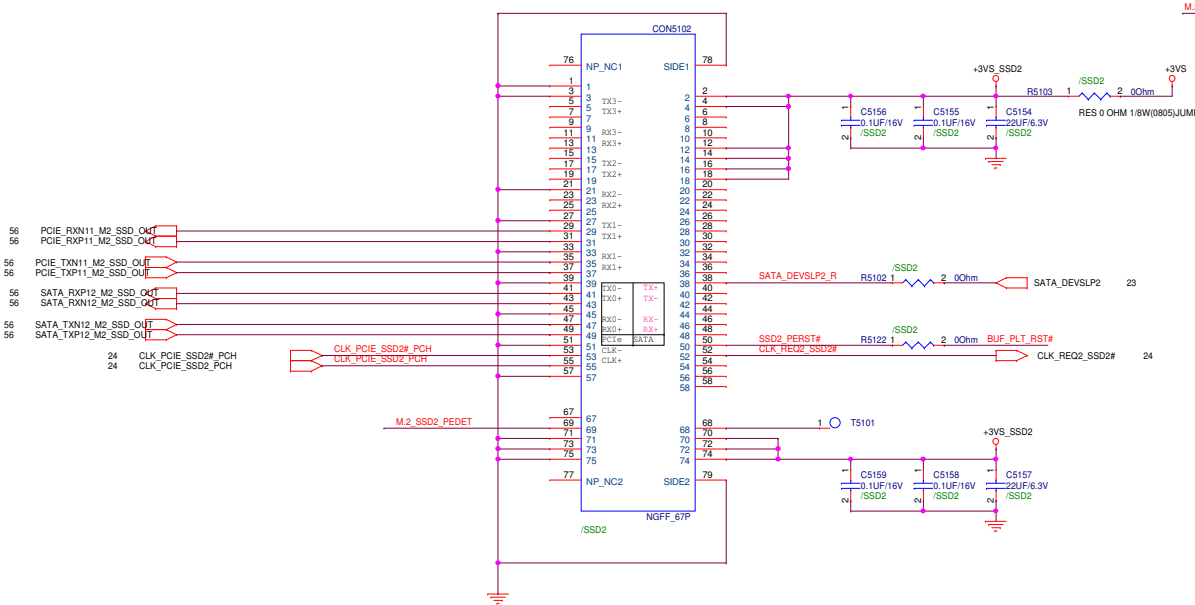
Size	Project Name	Rev
B	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 50 of 94

51

SSD1





SSD2

SSD type detection		
Interface	**Device side**	**PCH side**
PCIe	Hi-z	H
SATA	L	L
NO SSD	Hi-z	H

PCIe_M.2_Electromechanical_Spec_Rev_0.9-3_07312013_RS_Clean

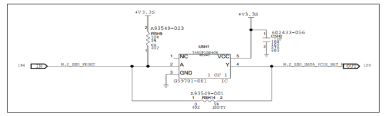
Table 46. Socket 2 Module Configuration Table

Module Configuration Decodes					
CONFIG_0 (Pin 21)	CONFIG_1 (Pin 69)	CONFIG_2 (Pin 75	CONFIG_3 (Pin 1)	Module Type and Main Host Interface[1]	Port Configuration[2]
0	0	0	0	SSD - SATA	N/A
0	1	0	0	SSD - PCIe	N/A

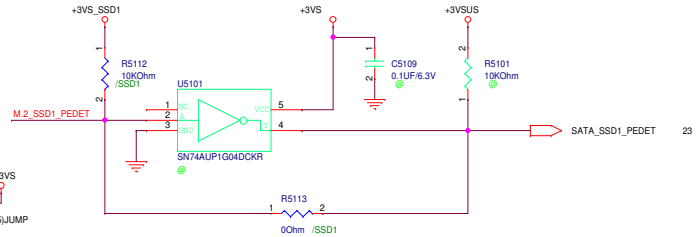
36.3.2.3 PEDET Guidelines

PEDET is the Interface detect used by PCH to determine the communication protocol that the M.2 card uses; PCIe* signaling (high) or SATA signaling (low) in conjunction with a platform located pull-up resistor.

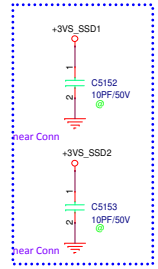
Figure 36-6. PEDET Circuitry Example

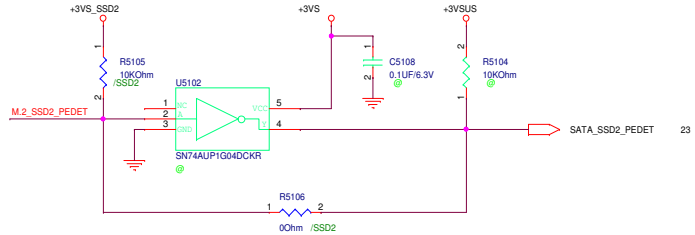


For Skylake platforms, need to implement the polarity inversion on the board using a NOT gate IC so that PCH will correctly interpret the Interface detect signaling from the M.2 device.



RF requirement





Reserve for resversal.
If BIOS can set resversal, unmount these parts.

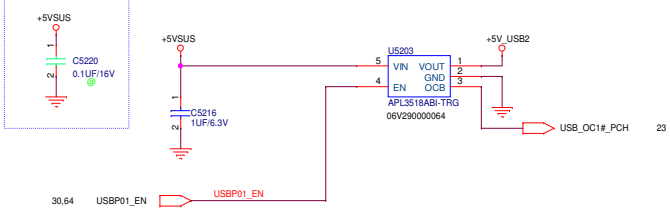
PEGATRON Title: SATA SSD_HDD
PEGATRON PROPRIETARY AND CONFIDENTIAL
RST-HWS RD
Engineer: James_Liao

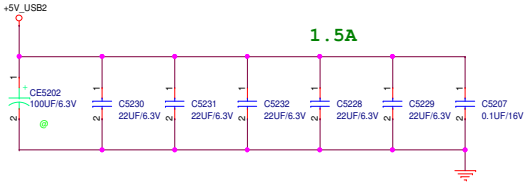
Size	Project Name	Rev
C	SU4EA	1.0

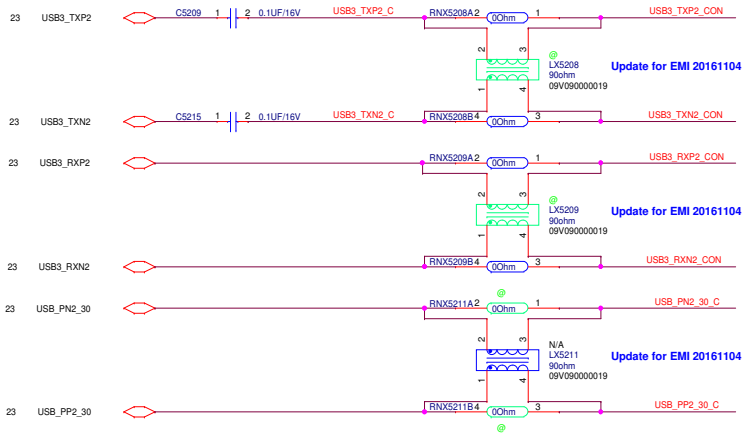
Date: Friday, March 10, 2017 Sheet 51 of 94

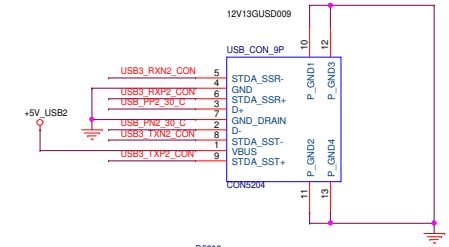
52 USB3.0

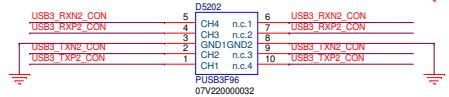
EMI 2016/03/17



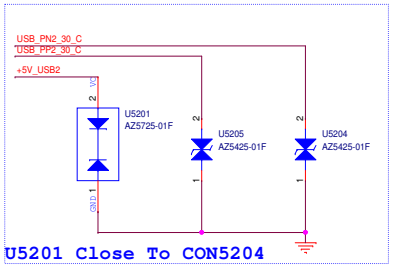






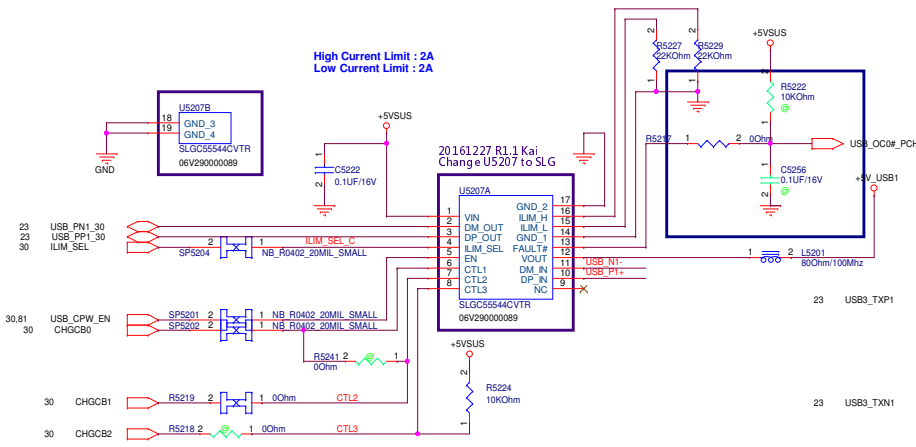


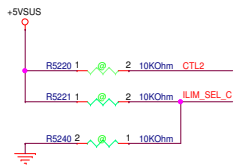
PLACE ESD Diodes near USB Connector



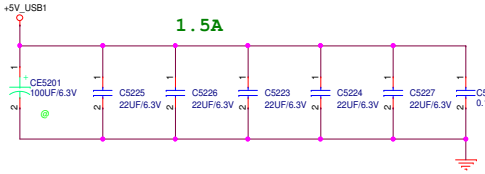
USB 3.0 ports x 1 with Sleep & Charge Left_Down

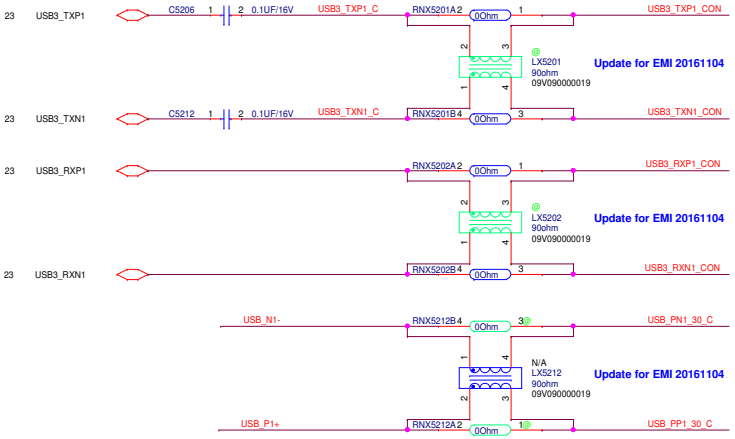
Device	Pega No.	VX No.
SLGC55544CVTR	0629-00TJ000	06V290000089 (Default)

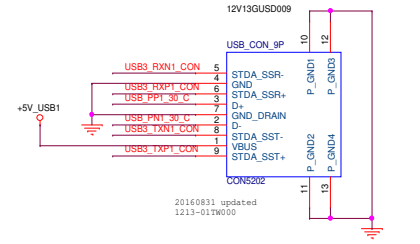




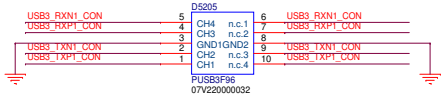
System Global Power State	TPS2544 Charging Mode	CTL1	CTL2	CTL3	ILIM_SEL	Current Limit Setting
S0	SDP (Standard Downstream)	1	1	0	1 or 0	ILIM_HI / ILIM_LO
S0	SDP, no discharge to / from CDP	1	1	1	0	ILIM_LO
S0	CDP, if a BC1.2 primary detection occurs	1	1	1	1	ILIM_HI
S3/S4/S5	Auto mode, no mouse wake	0	0	1	0	ILIM_HI
S3	Dedicated Charging Port Auto mode, keyboard/mouse wake up	0	1	1	X	ILIM_HI
S3	SDP, keyboard/ mouse wake-up	0	1	0	1 or 0	ILIM_HI / ILIM_LO

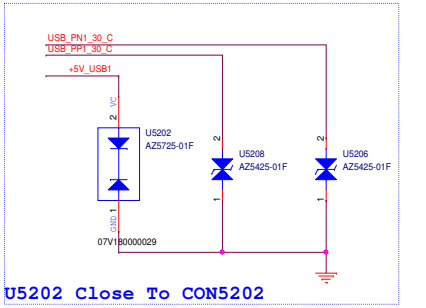






PLACE ESD Diodes near USB Connector



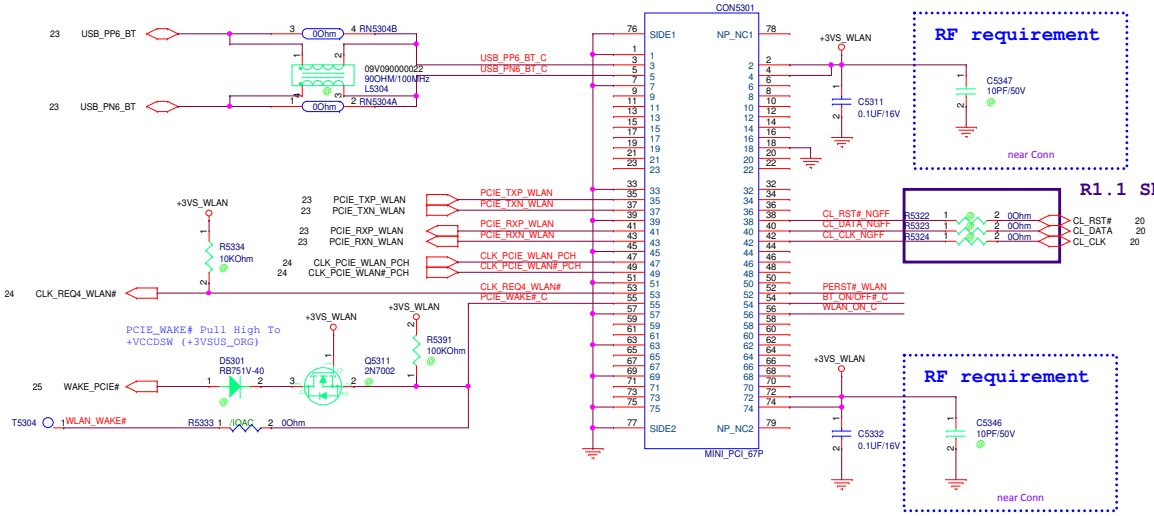


PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
Title: USB3.0_Charge IC
RST-HW3 RD
Engineer: James_Liao

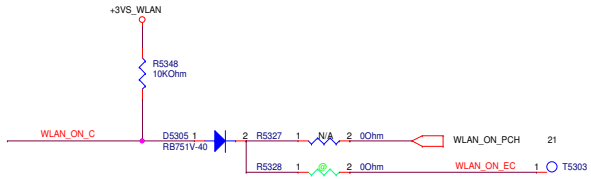
Size	Project Name	Rev
C	SU4EA	1.0

Date: Monday, March 13, 2017 Sheet 52 of 94

53 PCIE_WLAN_BT



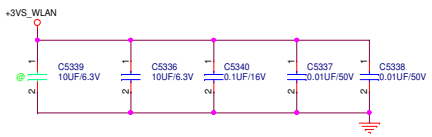
WLAN/BT with NGFF socket E

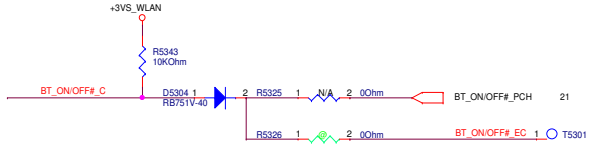


+3V_WLAN_WP1 bypass capactor:

Place 0.1UF near pin 2,4

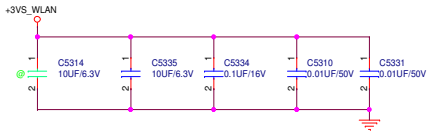
Place 10UF near +3V_WLAN_WP1 source side.

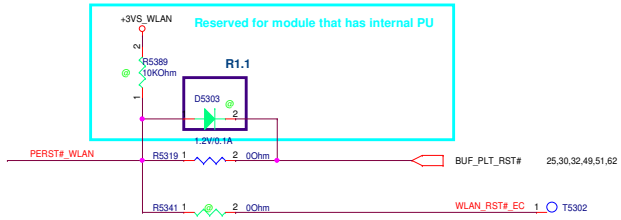


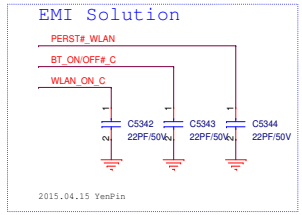


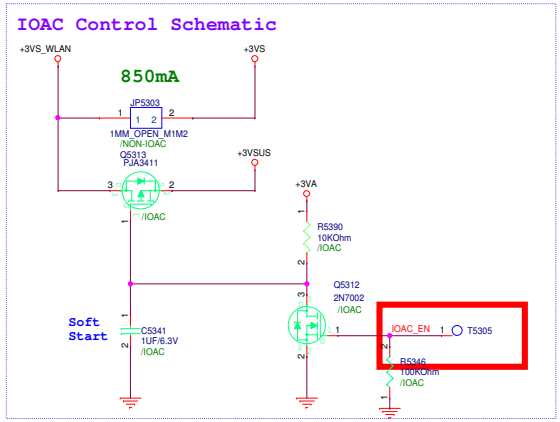
Place 0.1UF near pin 72,74.

Place 10UF near +3V_WLAN_WP1 source side.









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RST-HW3 RD

Title : PCIE_WLAN_BT

Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 53 of 94

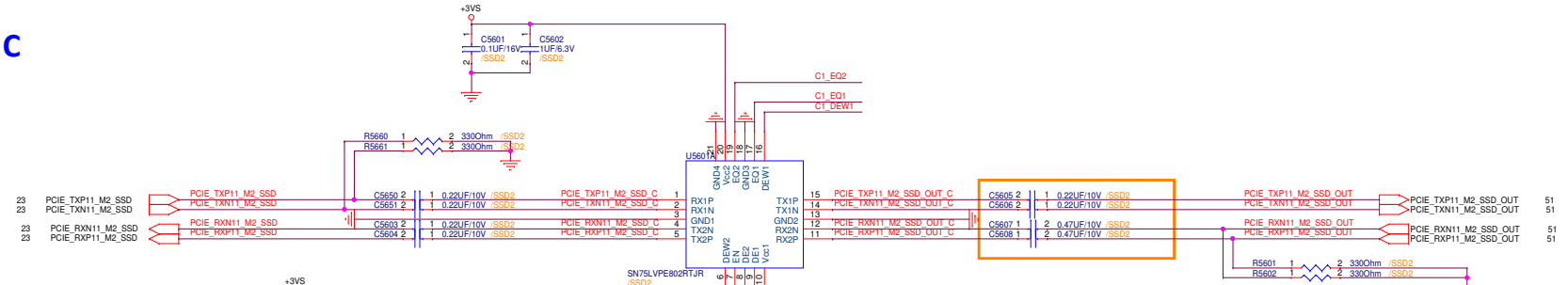
Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	54 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	55 of 94

+5VA +5VA 64,81

PCIE Re-driver

C



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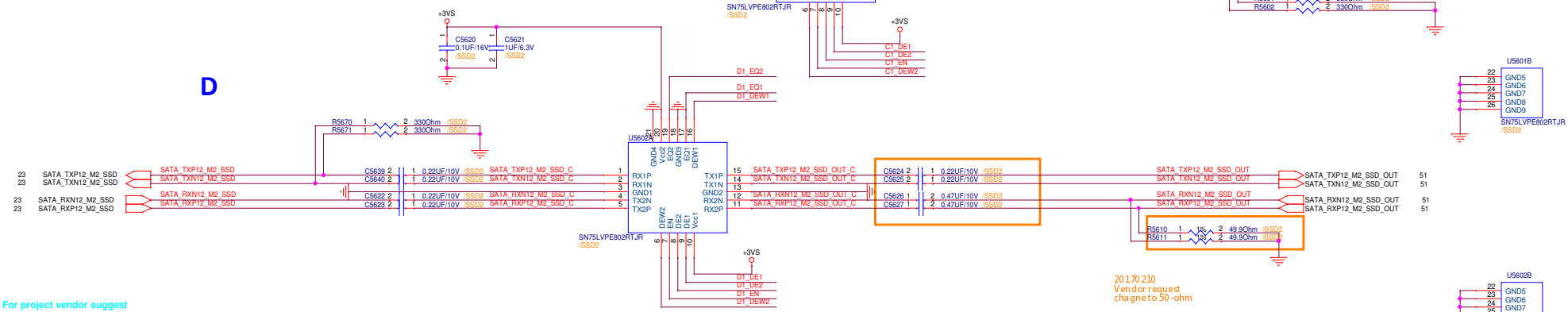


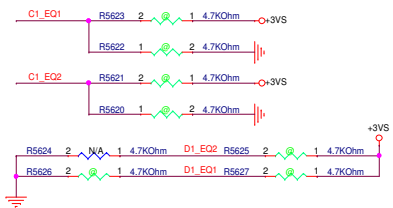
20170210
Vendor request
chagne to 50-ohm

For project vendor suggest

Equalizer control

EQ1 / EQ2	Channel 1 / Channel 2
NC	0 dB (Default)
H	7 dB
L	14 dB

Internally biased to VCC / 2 with >200-Ωk pullup or ulldown.
When 3-state pins are left as NC, board leakage at the pin pad must be <1 μA; otherwise, drive to VCC / 2 to assert mid-level

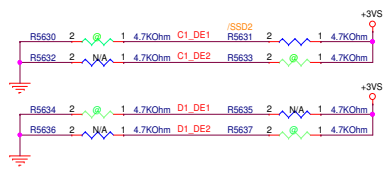


!!-R5602 Using TI's new source, imported by PN substitution,
R12 should use right way to import when VX and symbol application is done

De-Emphasis setting

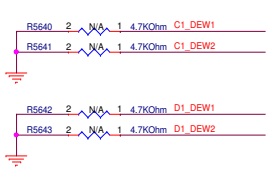
DE1 / DE2	Channel 1 / Channel 2
NC	-4 dB (Default)
H	0 dB
L	-2 dB

Internally biased to VCC / 2 with >200-Ωk pullup or ulldown.
When 3-state pins are left as NC, board leakage at the pin pad must be <1 μA; otherwise, drive to VCC / 2 to assert mid-level



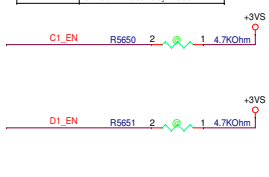
De-Emphasis width control

DEW1 or DEW2	Channel 1 / Channel 2
H	De-emphasis plse duration, Long (Default)
L	De-emphasis plse duration, Sfort



Device enable

EN	Device
H	Device enabled (Default)
L	Device in standby mode



PEGATRON Title: SATA SSD_HDD
PEGATRON PROPRIETARY AND CONFIDENTIAL
RGT-HWS RD
Engineer: James_Liao

Size	Project Name	Rev
C	SU4EA	1.0

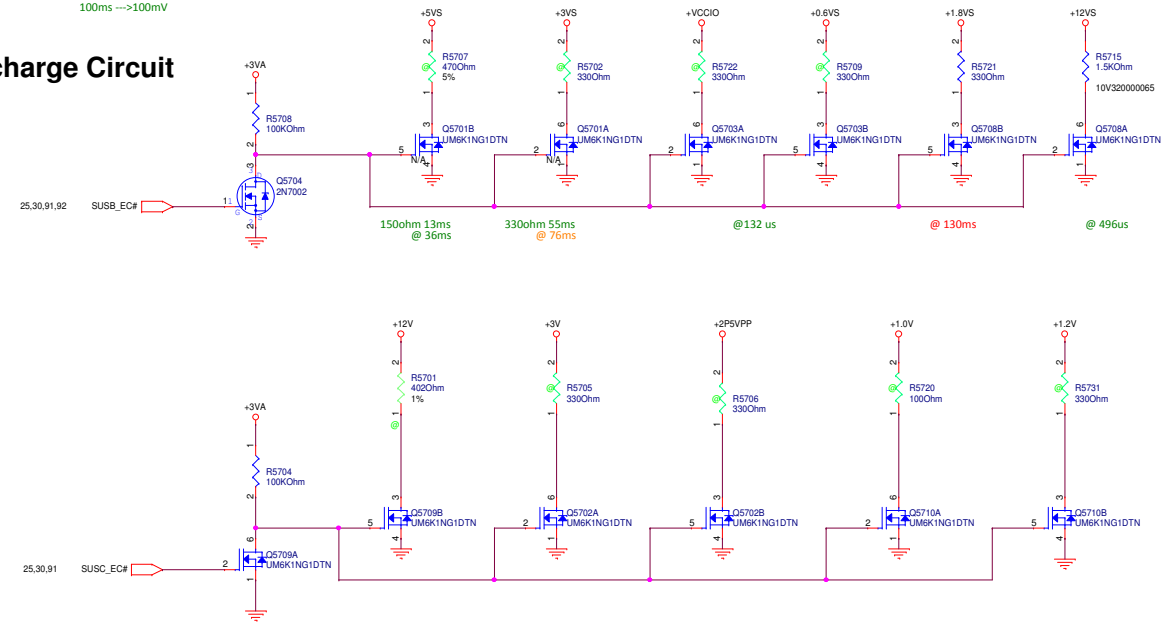
Date: Friday, March 10, 2017 Sheet 56 of 94

DISCHARGE

0402 1/16W min. resister
5V 400 OHM
3V 144 OHM
12V 2304 OHN

100ms --->100mV

Discharge Circuit



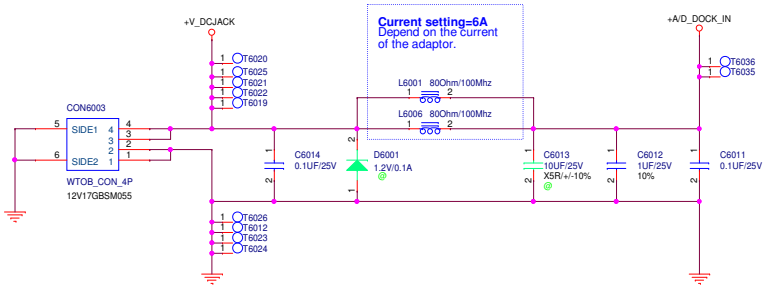
R1.1 remove GPU

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	58 of 94

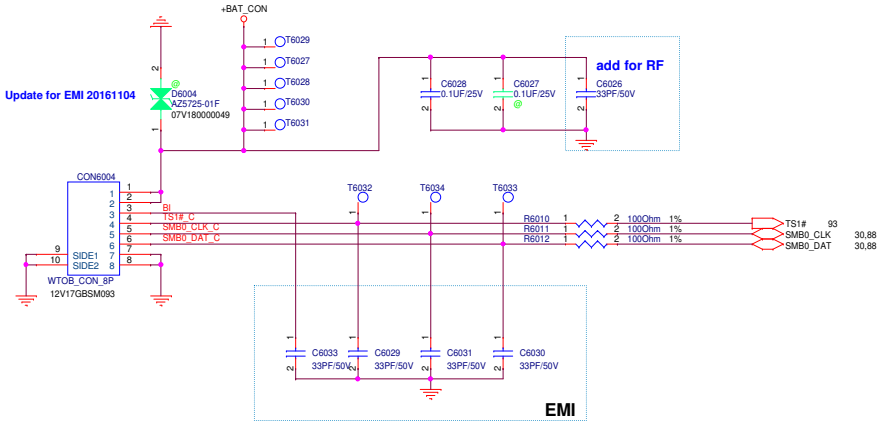
Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	59 of 94

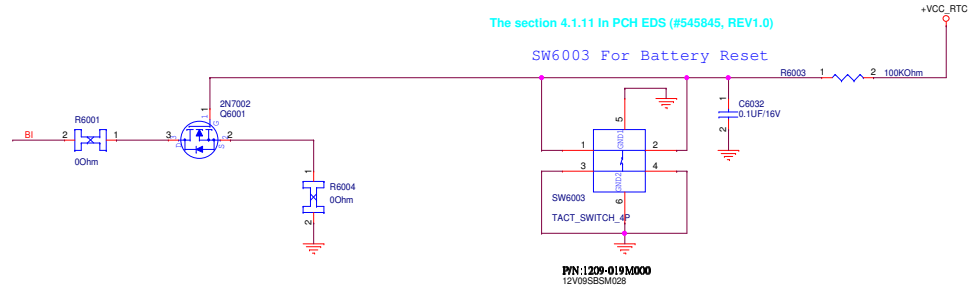
60 DC_BAT_CONN

DC Jack WTB CONN

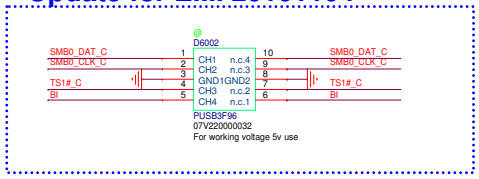


Battery Connector





Update for EMI 20161104



PEGATRON Title : DC_BAT_CONN

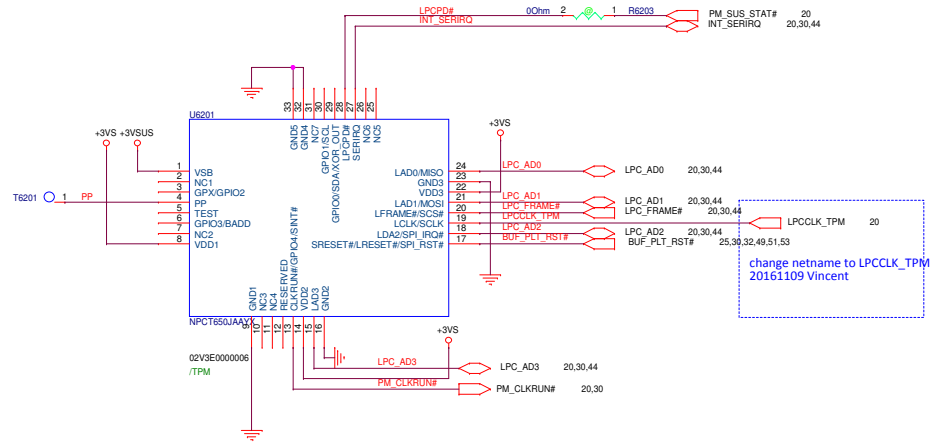
BG1-HW3 RD Engineer: James_Liao

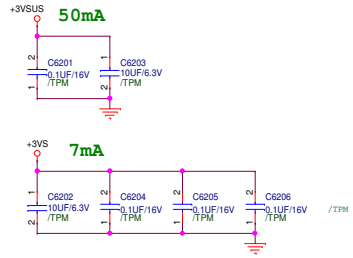
Size	Project Name	Rev
C	SU4EA	1.0

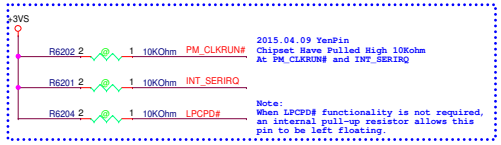
Date: Friday, March 10, 2017 Sheet 60 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	61 of 94

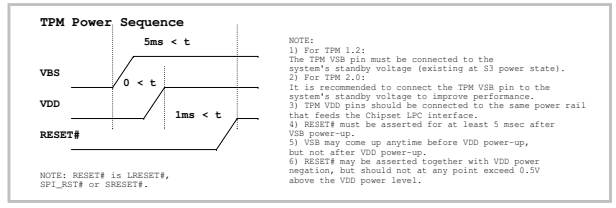
TPM NPCT650



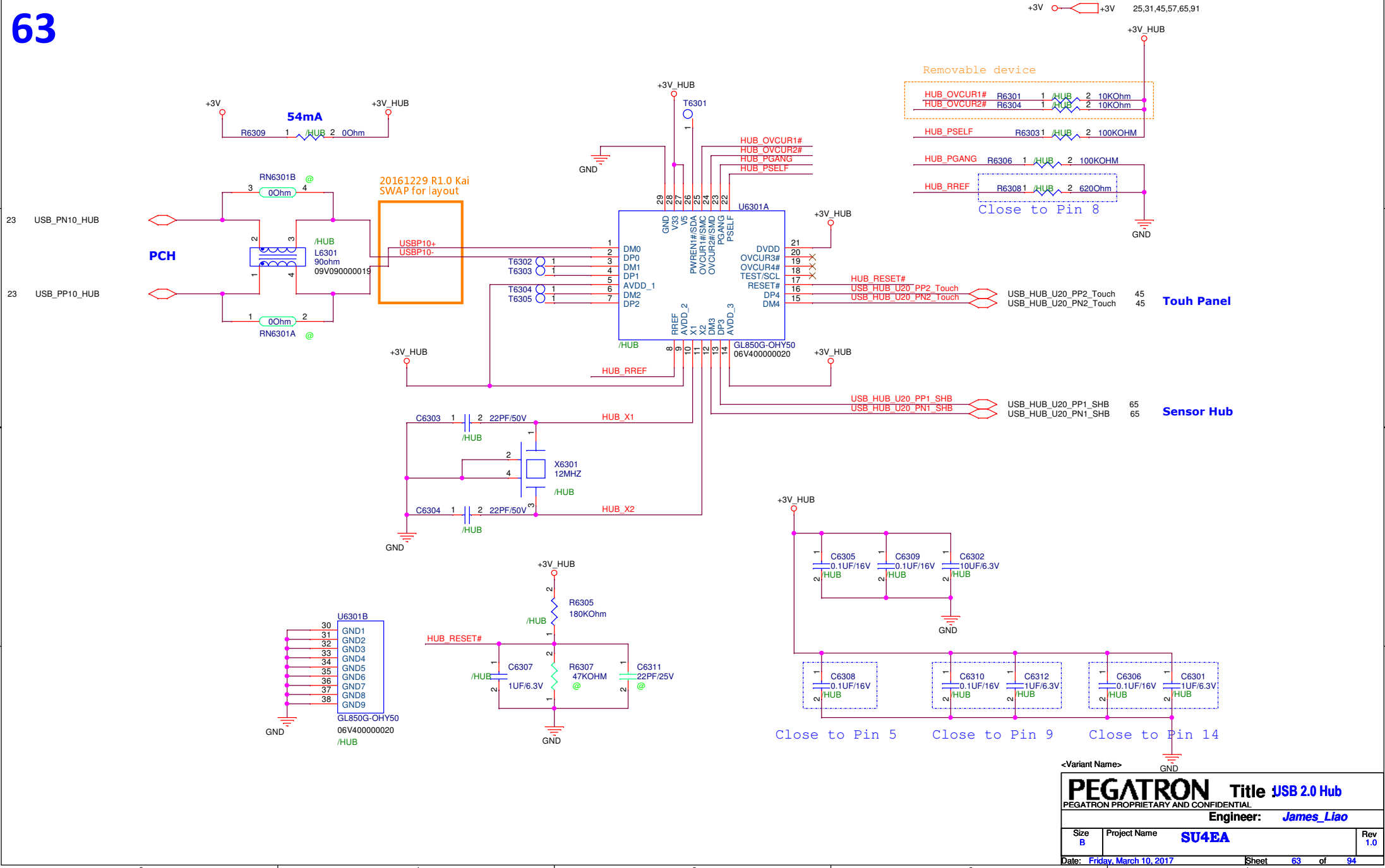




TPM VDD: Power the I/O buffers of the GPIO ports and the Host Interface
VSB: Standby 3.3V Power Supply. Powers the on-chip Core.



PEGATRON Title : TPM NPCT650
BG1-HW3 RD Engineer: James_Liao
Size C | Project Name SU4EA | Rev 1.0
Date: Friday, March 10, 2017 | Sheet 62 of 94



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

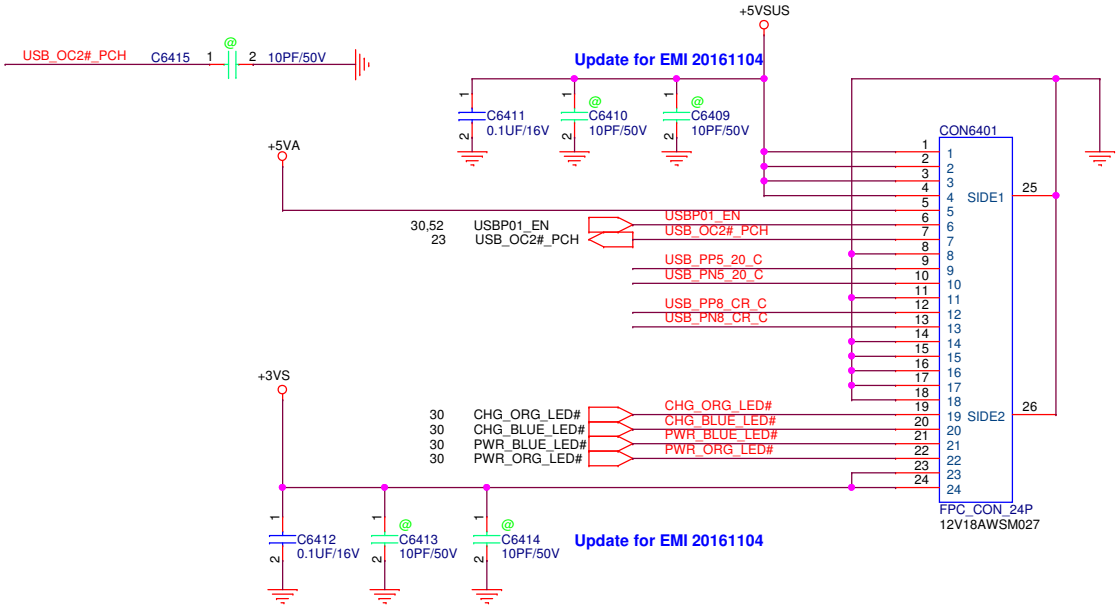
Title: USB 2.0 Hub

Engineer: James_Liao

Size	Project Name	Rev
B	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 63 of 94

64 DB CONN

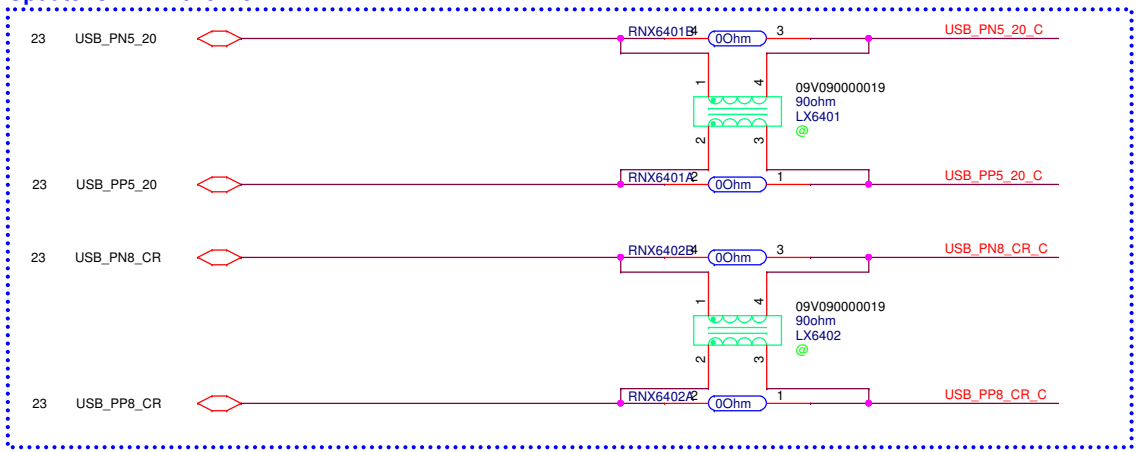


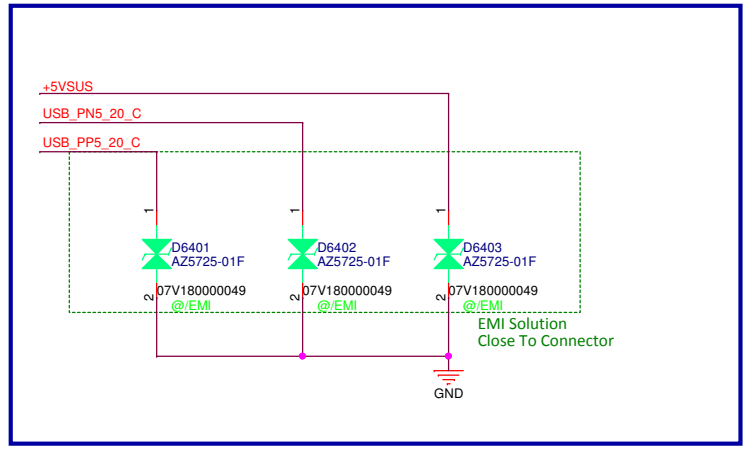
DB Connector Pin Define(MB Side)

1	+5VSUS
2	+5VSUS
3	+5VSUS
4	+5VSUS
5	+5VA
6	USB_EN
7	USB_OC
8	GND_IO
9	USB_PP1_20
10	USB_PN1_20
11	GND_IO
12	USB_PP2_20
13	USB_PN2_20
14	GND_IO
15	GND_IO
16	GND_IO
17	GND_IO
18	GND_IO
19	CHG_ORG_LED#
20	CHG_BLUE_LED#
21	PWR_BLUE_LED#
22	PWR_ORG_LED#
23	+3VS
24	+3VS

R1.1 EMI 需求

Update for EMI 20161104





PEGATRON

Title : IO Board

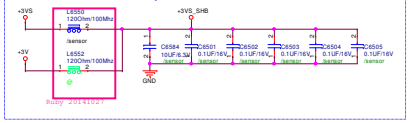
BG1-HW3 RD

Engineer: James_Liao

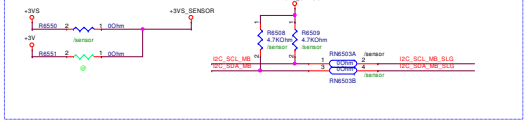
Size	Project Name	Rev
B	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 64 of 94

Sensor HUB Power Decouple



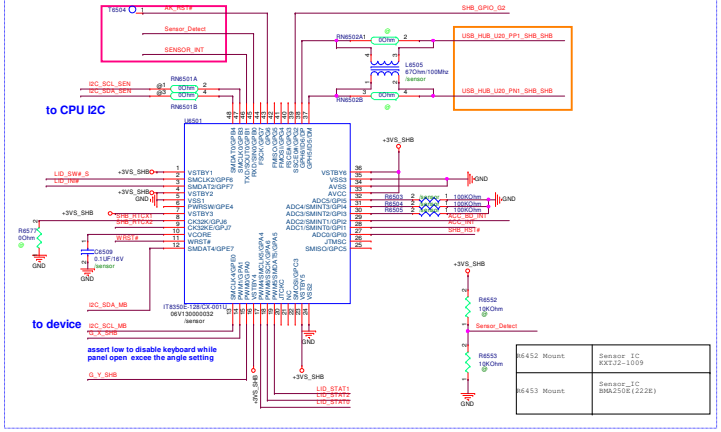
DB G-Sensor

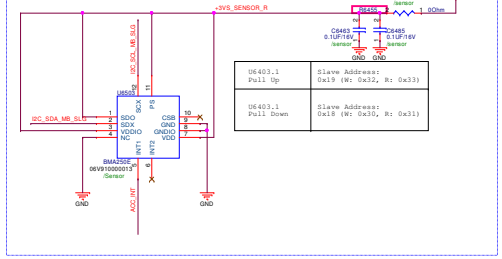


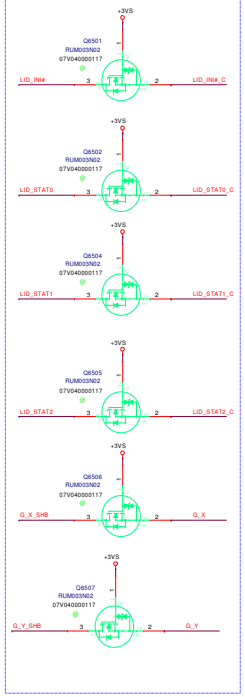
+3VS 3,4,20,21,22,23,24,30,31,32,36,41,44,45,48,49,50,51,53,56,57,62,64,91,92

+3V 25,31,45,57,63,91

ITE8350 Sensor HUB



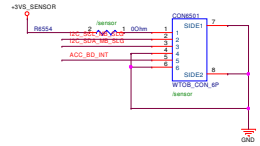




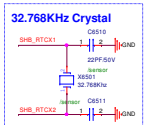
Before Tapping

20161227 RL0 Kai
Connect USB Hub to SHB /Touch

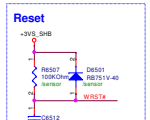
12V17GISM003



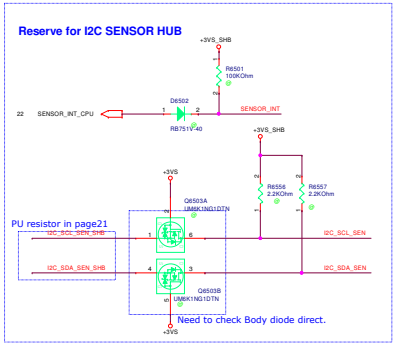
32.768KHz Crystal

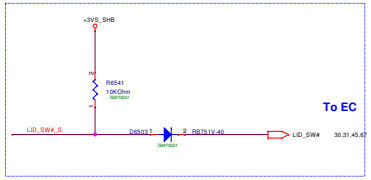


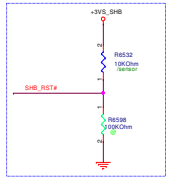
Reset

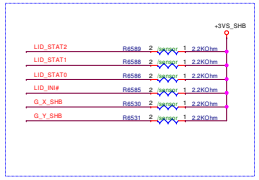


Reserve for I2C SENSOR HUB









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PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

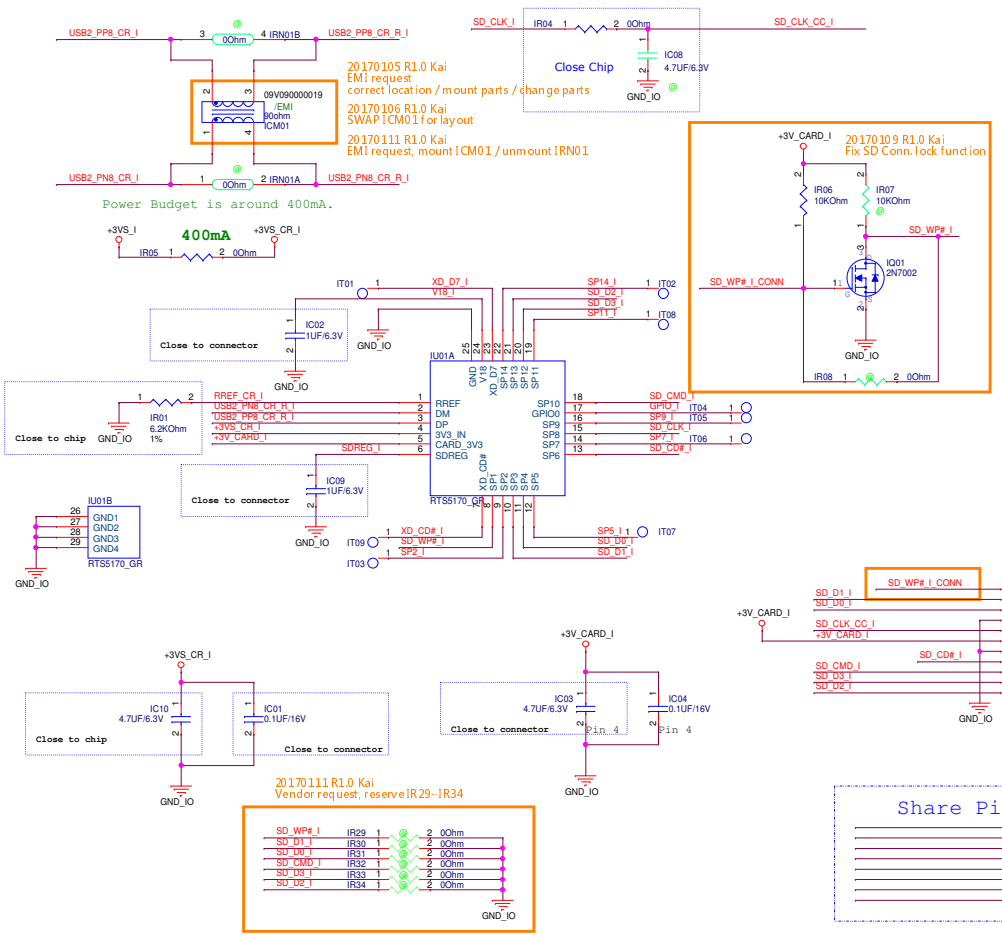
Title :G-Sensor
Engineer: James_Liao

Size	Project Name	Rev
D	SU42A	1.0

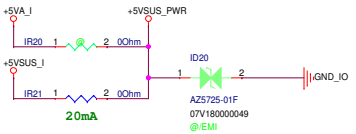
Date: Friday, March 10, 2017 Sheet 65 of 94

66 IO Board

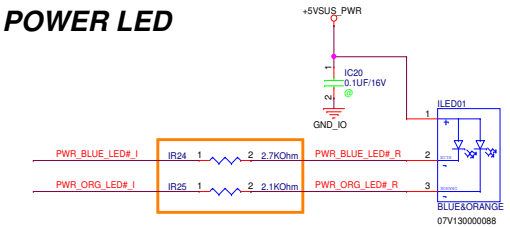
Card Reader



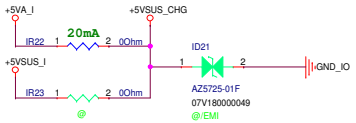
POWER LED



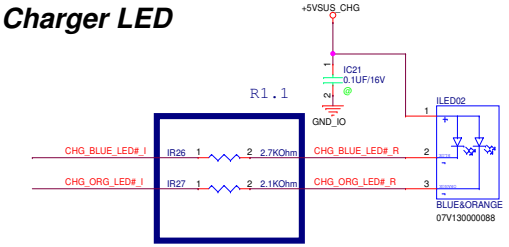
POWER LED

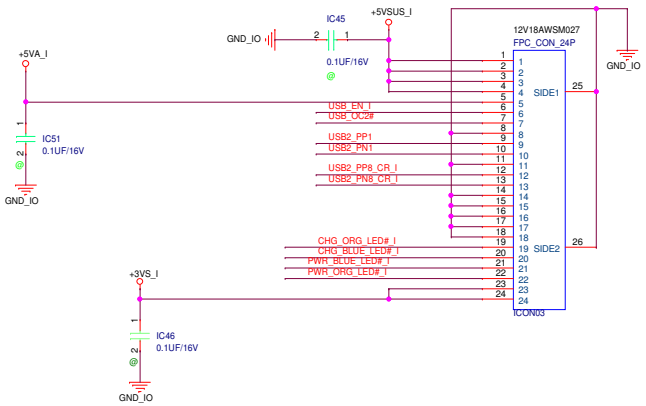


Charger LED

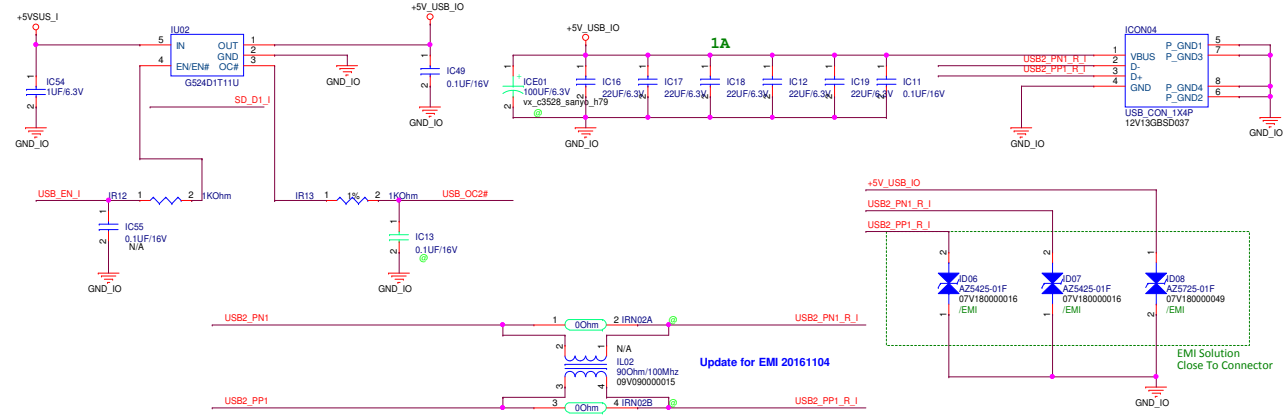


Charger LED





USB 2.0



PEGATRON Title : IO Board

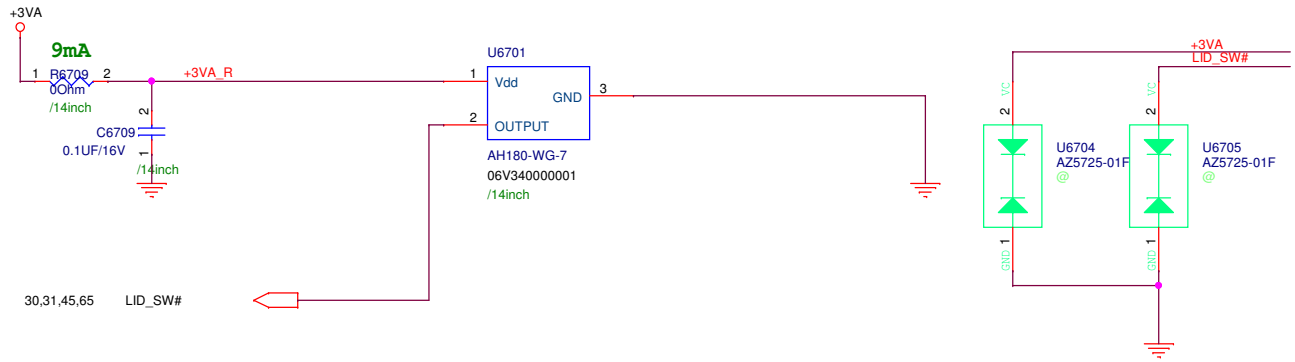
PEGATRON PROPRIETARY AND CONFIDENTIAL

BG1-HW3 RD Engineer: James_Liao

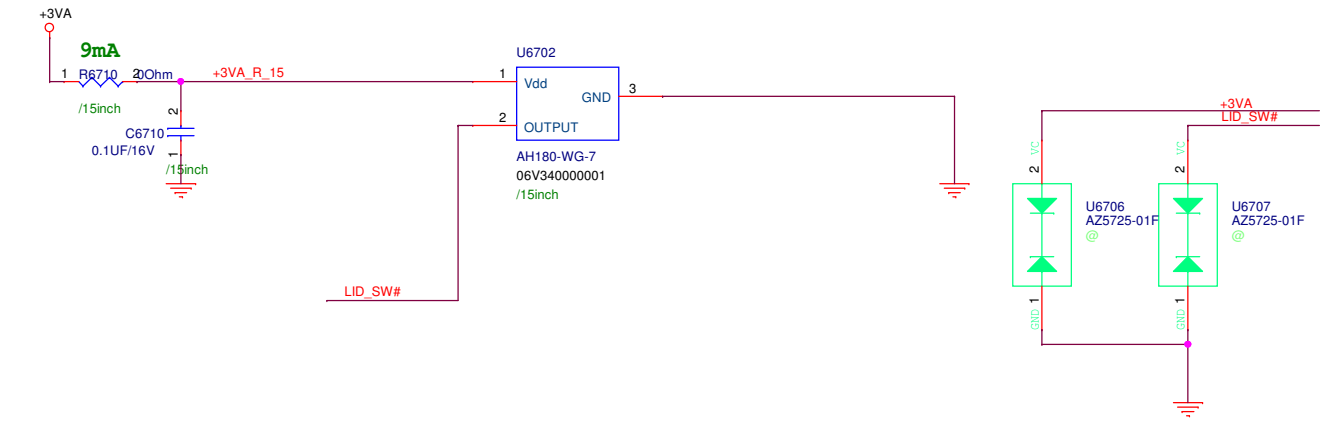
Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 66 of 94

LID Switch 14 inch



LID Switch 15 inch



PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : Sensor Board

BG1-HW3 RD

Engineer: James_Liao

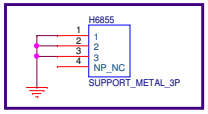
Size	Project Name	Rev
B	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 67 of 94

68 ME Hole

靠近M.2 CONN

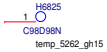
R1.1



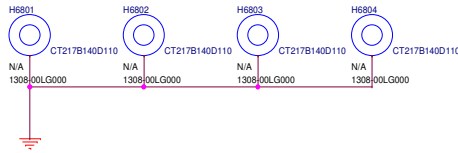
20161230 R1.1 Kai
Connect PTH to GND

鎖IOPORT SHIELDING螺絲孔

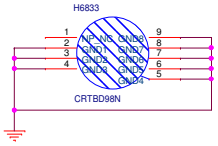
2.5X3.0 橢圓孔

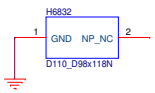


CPU NUT

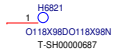


Main shielding 定位孔



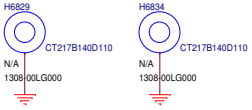


2.5 圓孔

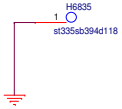


R1.1

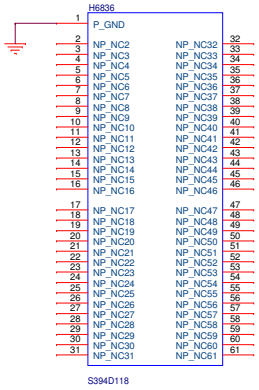
Main Shielding NUT



Audio Jack下孔

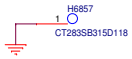


斷熱孔

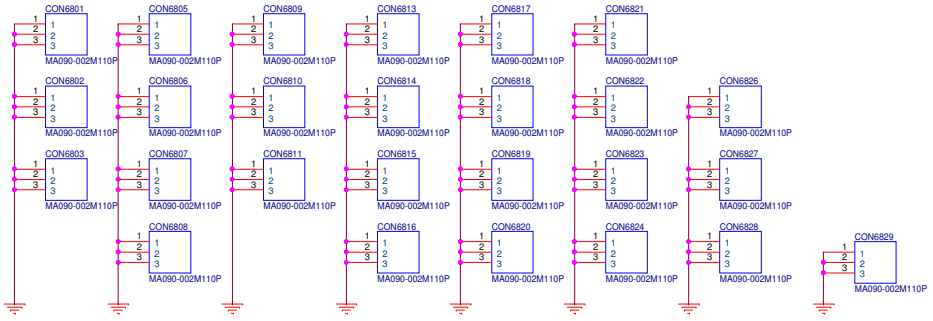


20161228 R1.0 Kai
Remove H6856
Connect H6857 to GND
Remove clip x1 (CON6825)

主板PTH孔



Clip



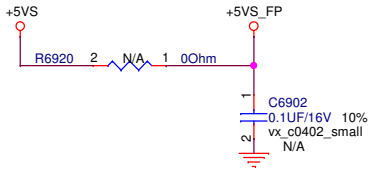
PEGATRON Title : ME Hole
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD
Engineer: James_Liao

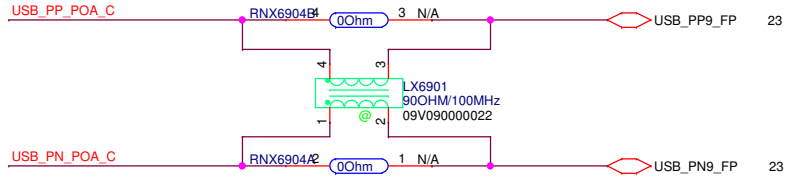
Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 68 of 94

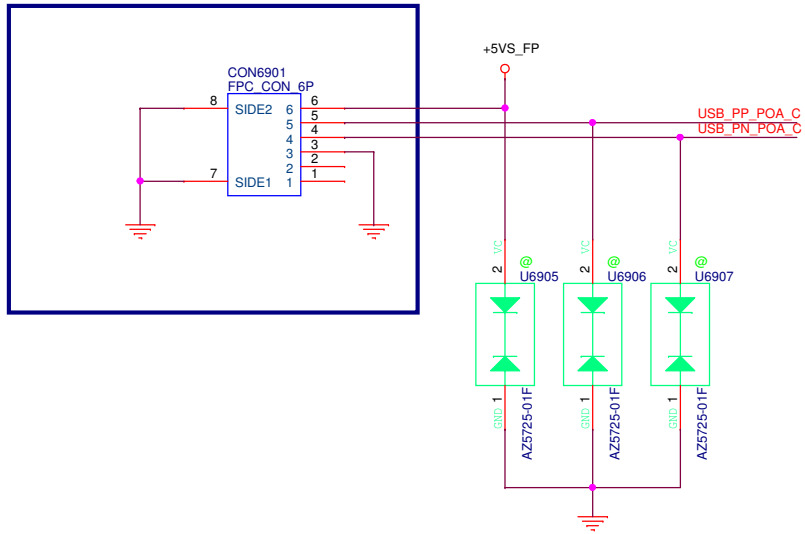
69 Finger printer

Close to CON6901





R1.1



Pin	Definition
1	+PP_VCC
2	USBP
3	USBN
4	GND
5	NC
6	NC

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL
BG1-HW3 RD

Title : Finger printer
Engineer: James_Liao

Size	Project Name	Rev
B	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 69 of 94

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU--PCIE

BG1-HW3 RD

Engineer: James_Liao

Size	Project Name	Rev
A	SU4EA	1.0

Date:

Sheet 70 of 94

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU-DISPLAY

Engineer: James_Liao

BG1-HW3 RD

Size	Project Name	Rev
Custom	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 71 of 94

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU-MEM_CTRL_CHA

Engineer: James_Liao

BG1-HW3 RD

Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 72 of 94

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU-MEM_CTRL_CHB

Engineer: James_Liao

BG1-HW3 RD

Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 73 of 94

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU-STRAP/MISC

Engineer: James_Liao

BG1-HW3 RD

Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 74 of 94

PEGATRON

Title : (1)GPU-POWER/GND

Engineer: James_Liao

BG1-HW3 RD

Size	Project Name	Rev
Custom	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 75 of 94

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : (2)GPU--Thermal/JTAG/SEQ

Engineer: James_Liao

BG1-HW3 RD

Size	Project Name	Rev
Custom	James_Liao	1.0

Date: Friday, March 10, 2017 Sheet 76 of 94

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU-MEM CHA

Engineer: James_Liao

BG1-HW3 RD

Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 77 of 94

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : GPU-MEM CHB

Engineer: James_Liao

BG1-HW3 RD

Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 78 of 94

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: GPU-POWER FLOW

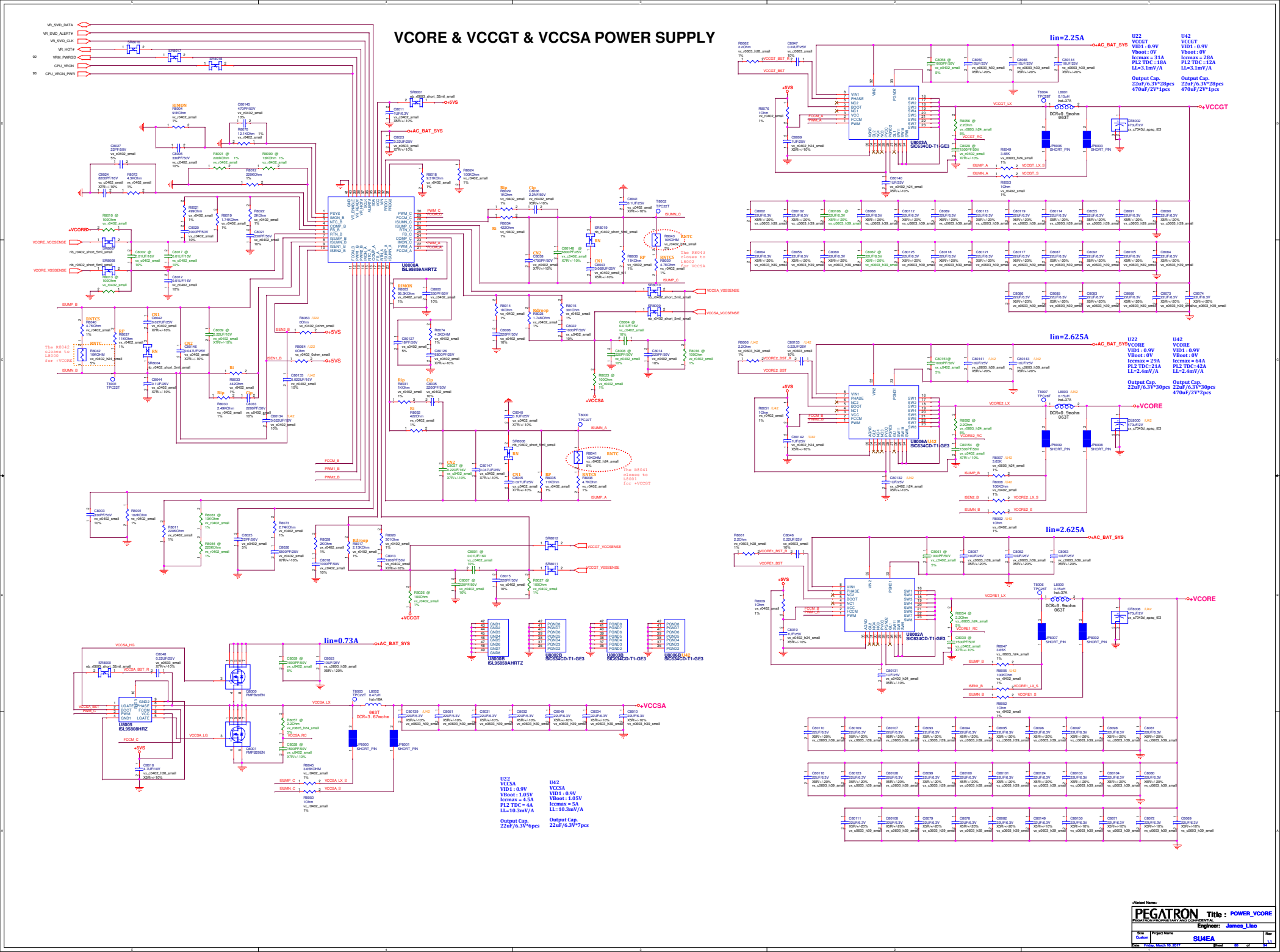
Engineer: James_Liao

BG1-HW3 RD

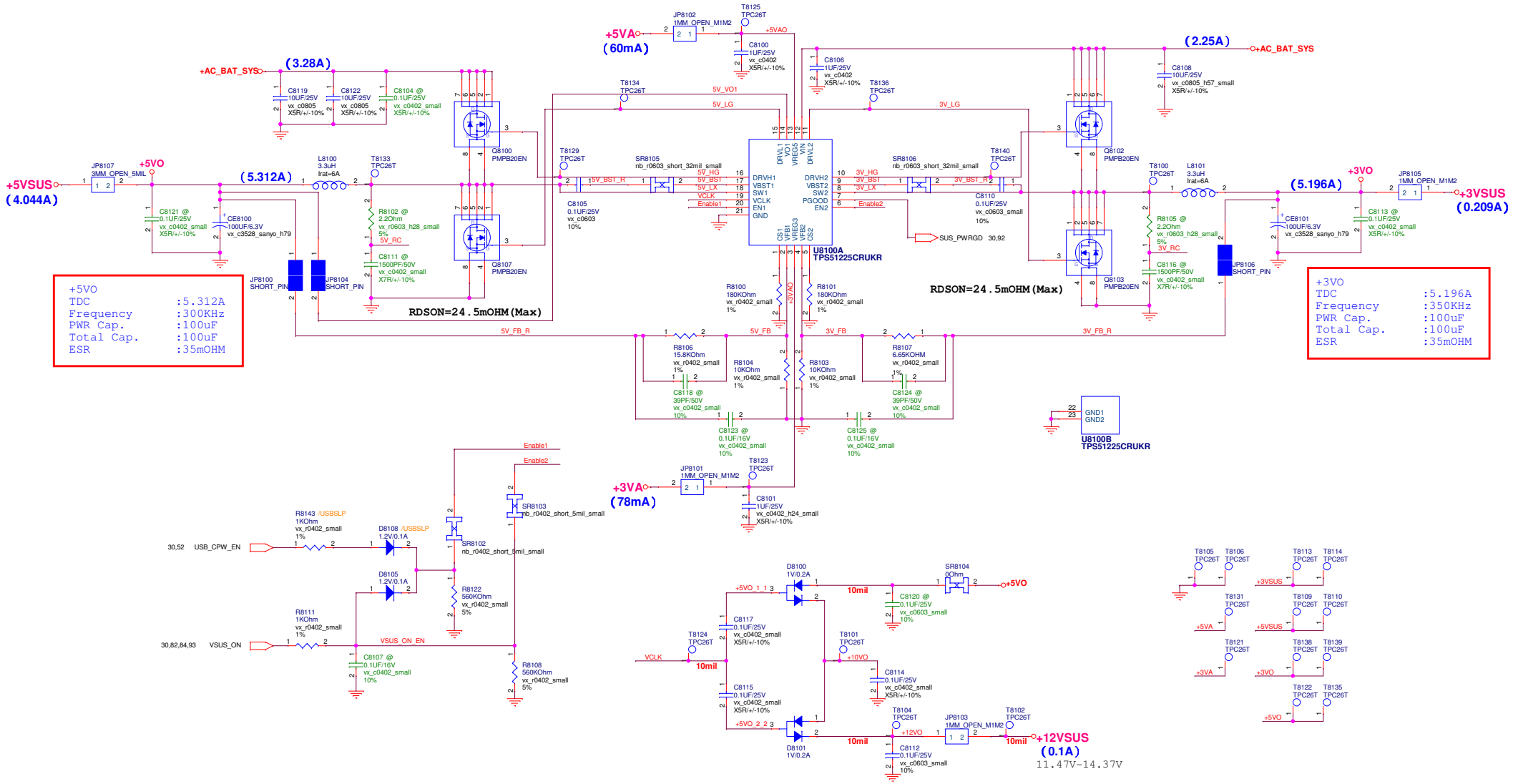
Size	Project Name	Rev
C	SU4EA	1.0

Date: Friday, March 10, 2017 Sheet 79 of 94

VCORE & VCCGT & VCCSA POWER SUPPLY



5VO & 3VO POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_SYSTEM

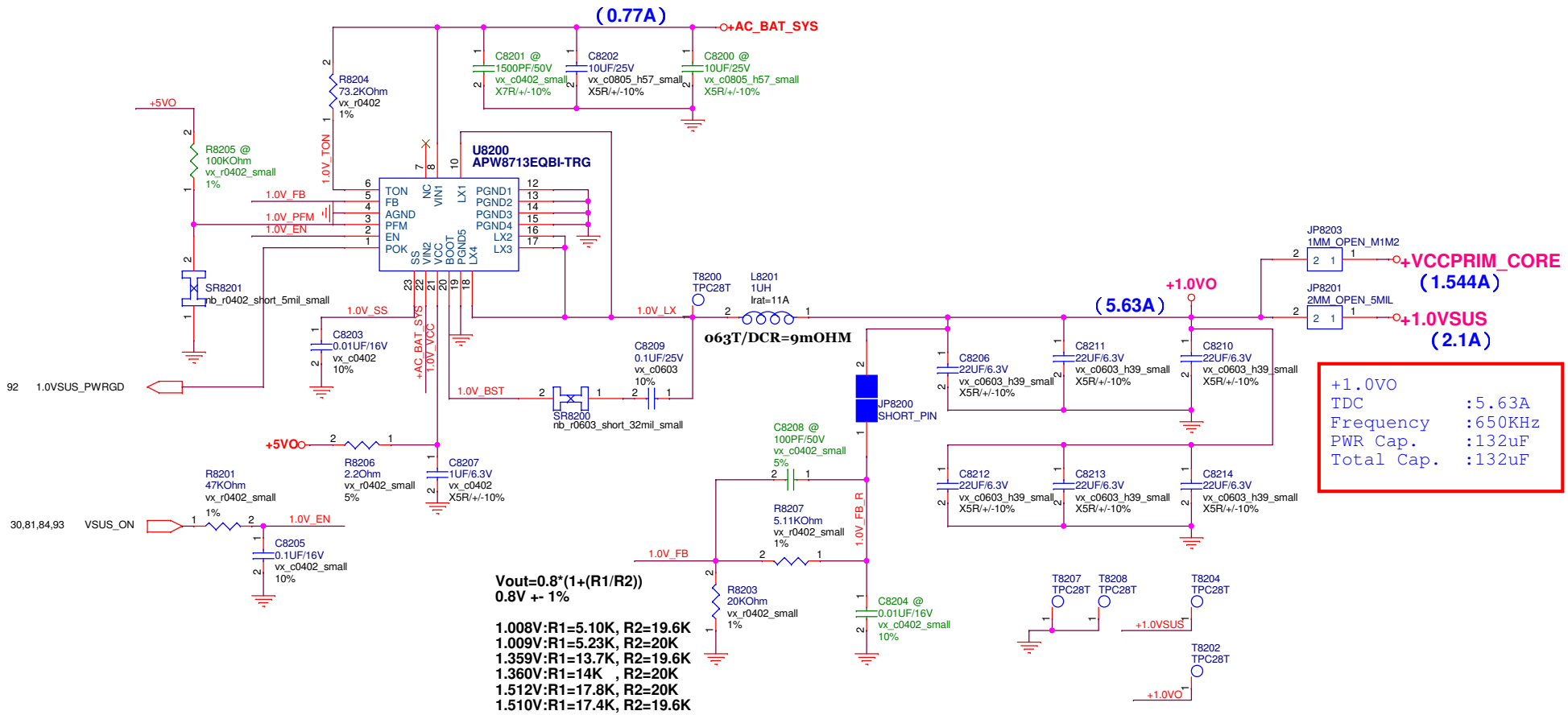
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: James_Liao

Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 81 of 94

+1.0VSUS POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

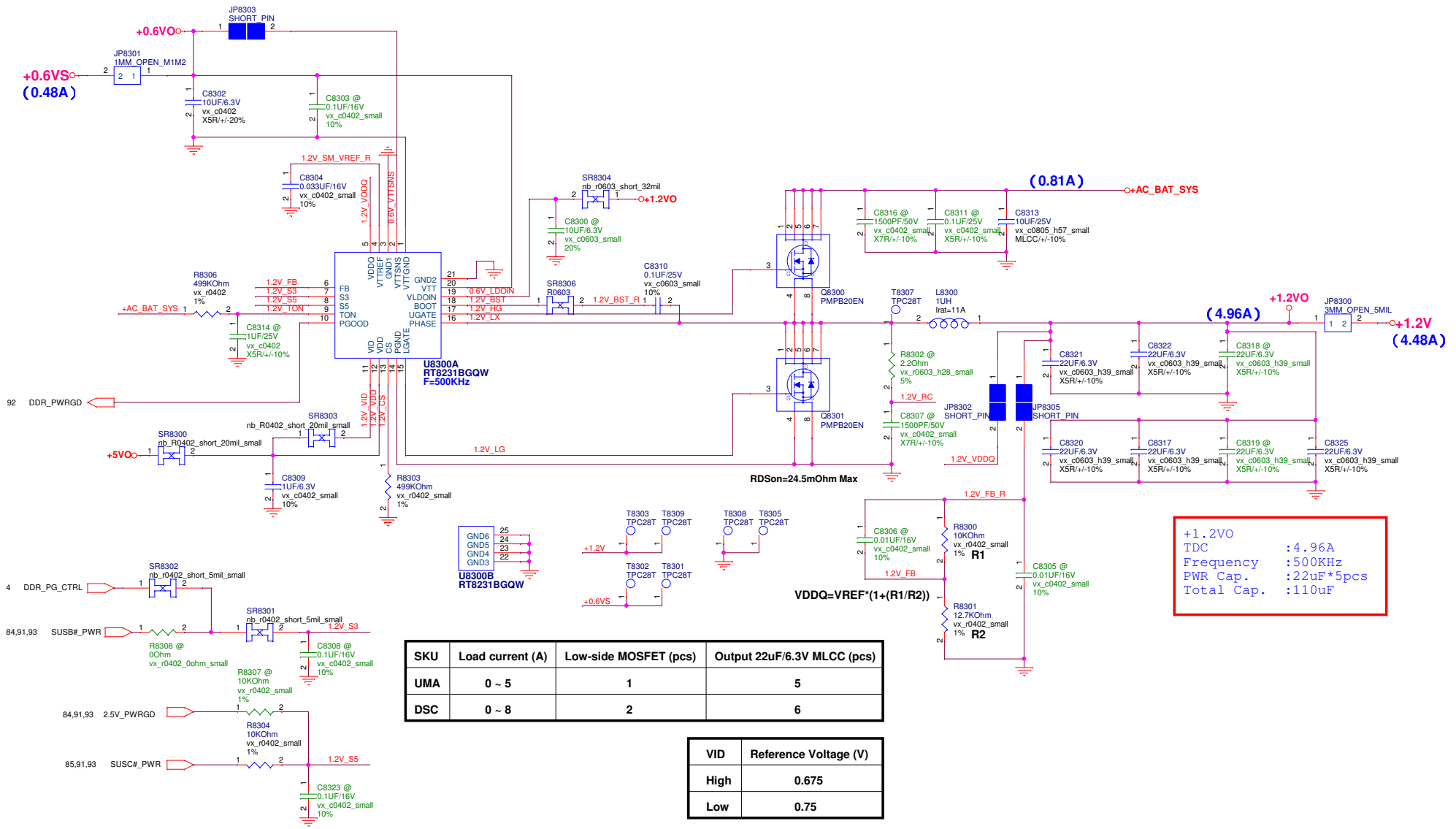
Title : P82_+1.0VSUS & +2.5V

Engineer: James_Liao

Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 82 of 94

DDR & VTT POWER SUPPLY



SKU	Load current (A)	Low-side MOSFET (pcs)	Output 22uF/6.3V MLCC (pcs)
UMA	0 ~ 5	1	5
DSC	0 ~ 8	2	6

VID	Reference Voltage (V)
High	0.675
Low	0.75

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

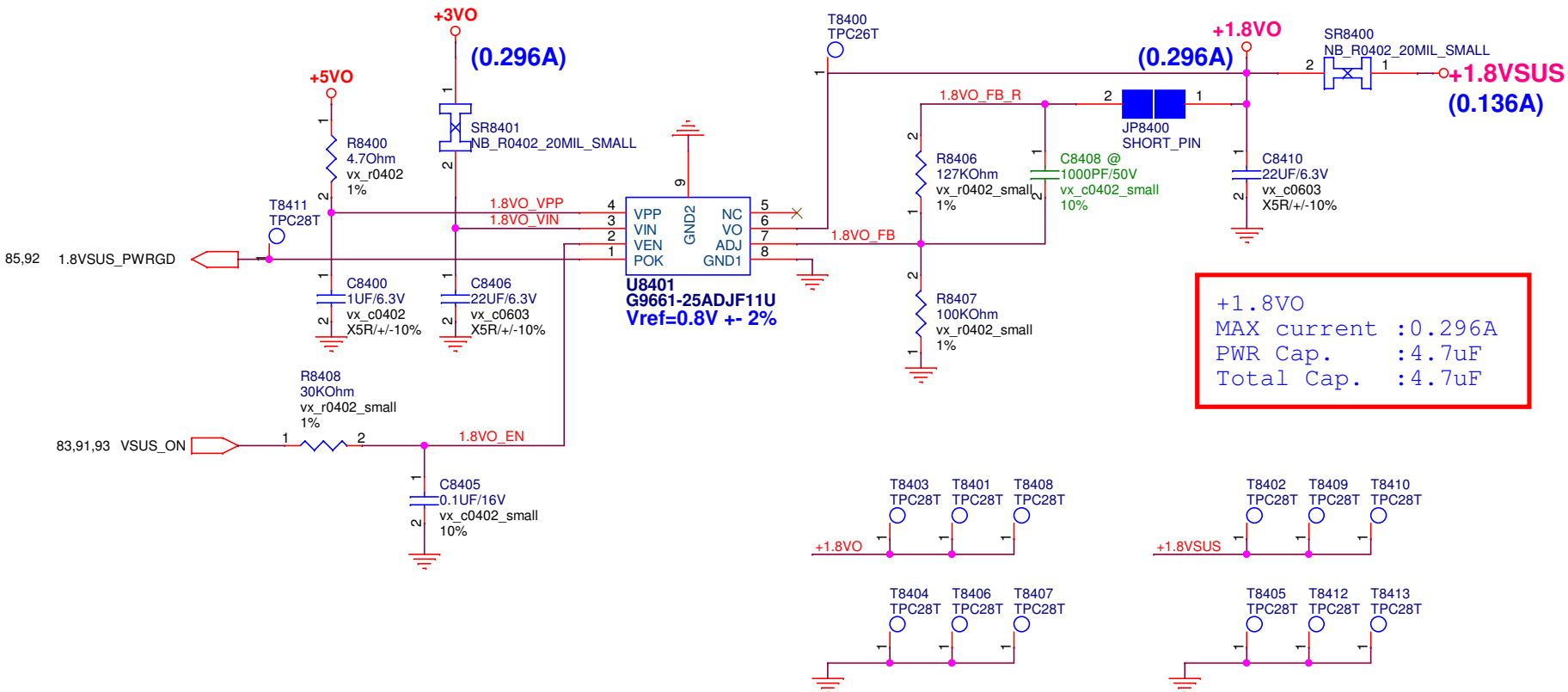
Title : POWER_DDR & VTT

Engineer: James_Liao

Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 83 of 94

1.8VSUS POWER SUPPLY



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

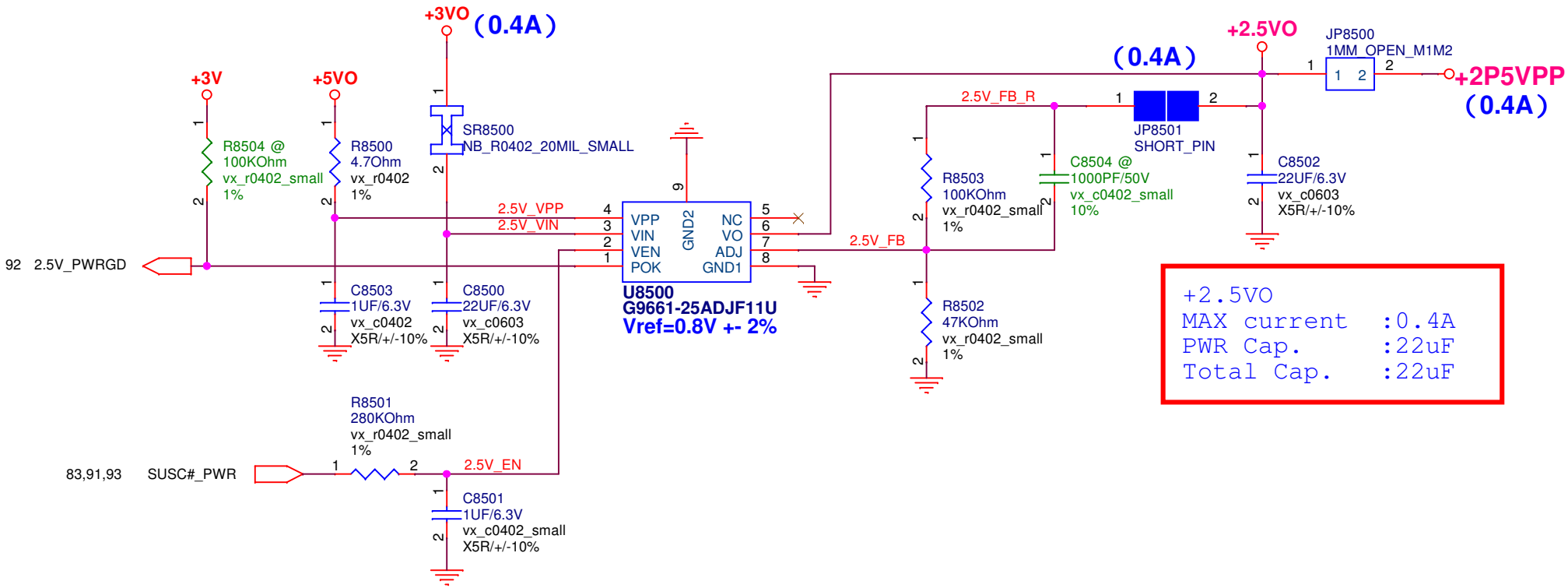
Title : POWER_1.8VSUS

Engineer: James_Liao

Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 84 of 94

2.5V POWER SUPPLY



<Variant Name>

PEGATRON Title : POWER_+2.5V

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: James_Liao

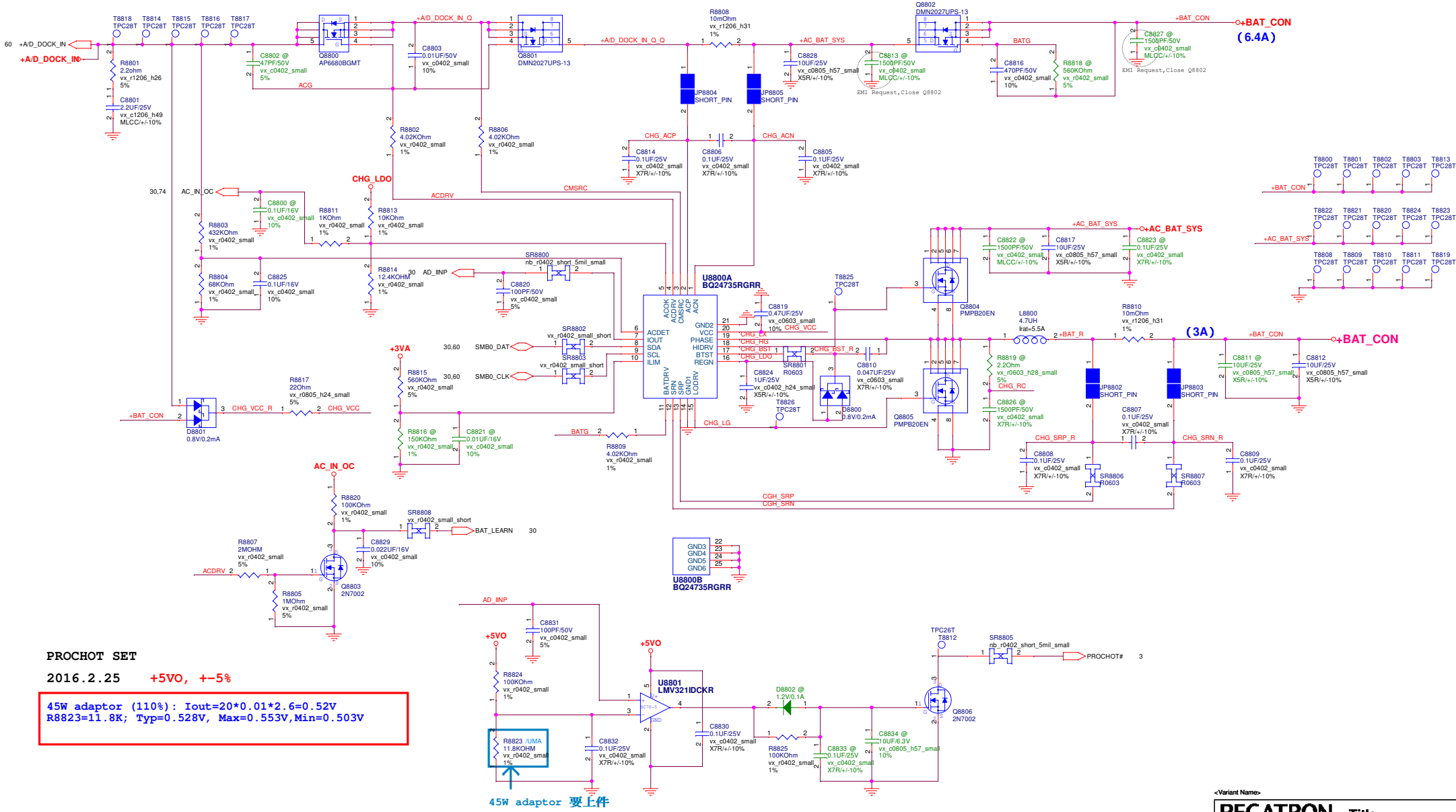
Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 85 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	86 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	87 of 94

BATTERY CHARGER



PROCHOT SET

2016.2.25 **+5VO, +-5%**

45W adaptor (110%): Iout=20*0.01*2.6=0.52V
R8823=11.8K; Typ=0.528V, Max=0.553V,Min=0.503V

<Variant Name>

PEGATRON Title : POWER_CHARGER

PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: James_Liao

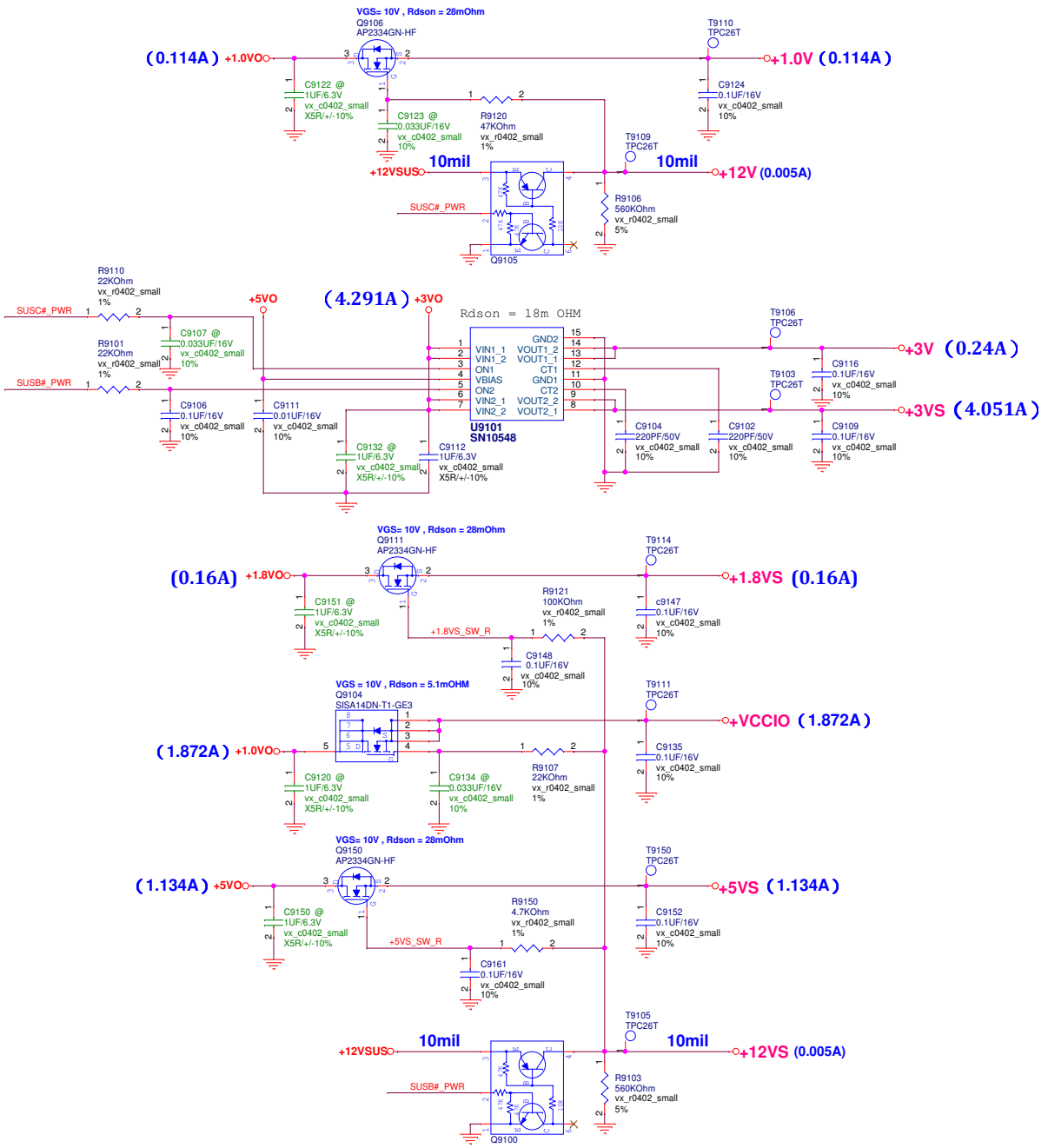
Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 88 of 94

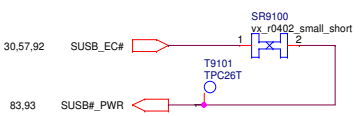
Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	89 of 94

Title	<Title>
Size: A	Document Number: SU4EA
Rev	<RevCode>
Date:	Friday, March 10, 2017
Sheet	90 of 94

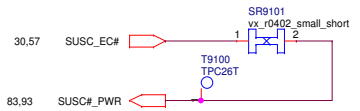
SUSB#_PWR POWER
SUSC#_PWR POWER



SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

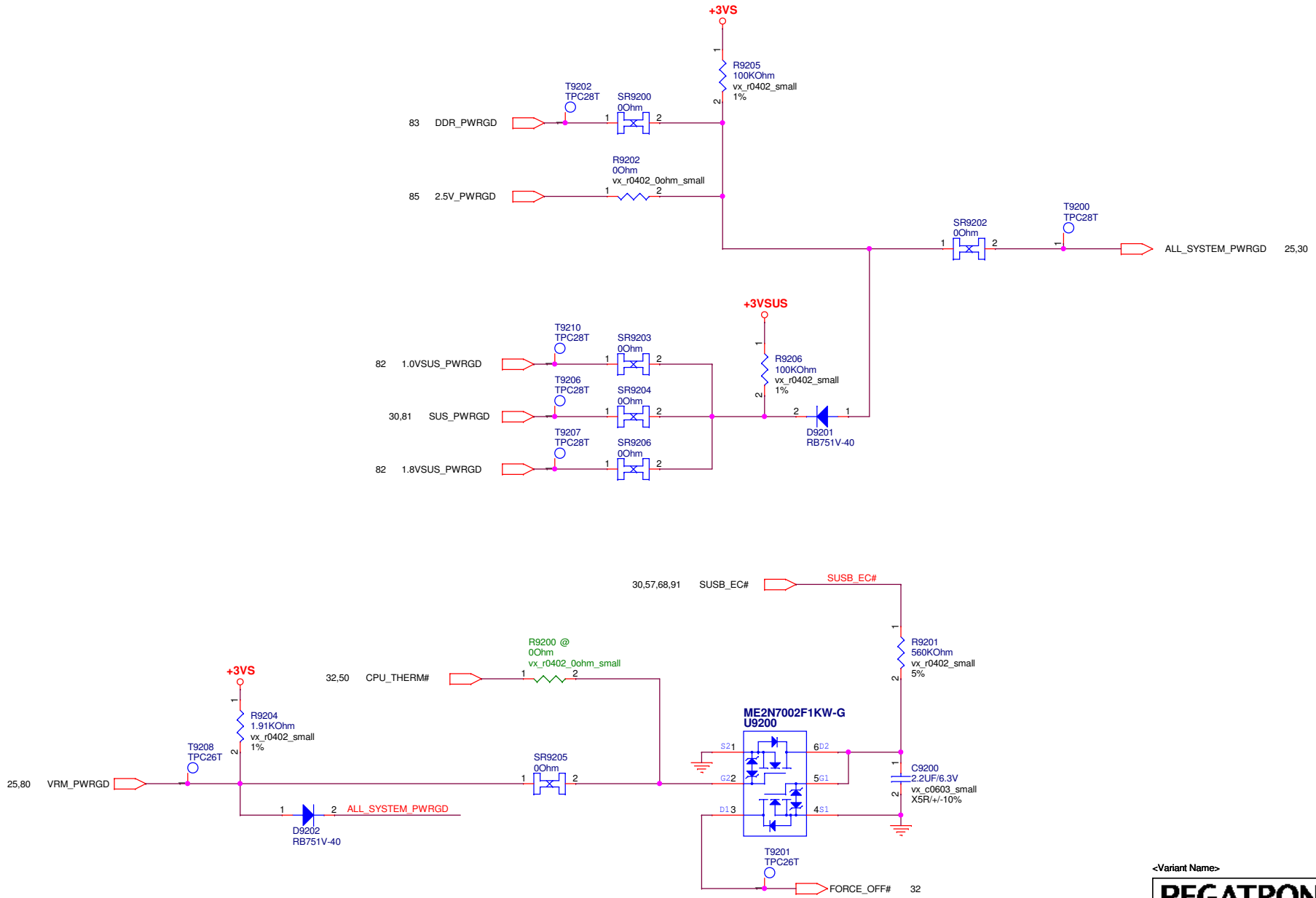
Title : POWER_LOAD SWITCH

Engineer: James_Liao

Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 91 of 94

POWER GOOD DETECTER



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_PROTECT

Engineer: James_Liao

Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 92 of 94

+A/D_DOCK_IN → +A/D_DOCK_IN 60,88

+BAT_CON → +BAT_CON 60,88

+AC_BAT_SYS → +AC_BAT_SYS 45,80,81,82,83,86,88,97

+5VA → +5VA 56,81

+3VA → +3VA 24,30,31,36,53,56,57,81,88

+5VO → +5VO 26,81,82,83,84,85,86,88,91

+3VO → +3VO 81,84,85,91,96

+2.5VO → +2.5VO 84

+1.8VO → +1.8VO 84,91

+1.2VO → +1.2VO 83

+1.0VO → +1.0VO 82,91

+0.6VO → +0.6VO 83

+12VSUS → +12VSUS 81,91

+5VSUS → +5VSUS 52,56,81

+3VSUS → +3VSUS 4,25,26,28,30,31,33,51,52,53,68,81,92

+1.8VSUS → +1.8VSUS 9,26,84

+1.0VSUS → +1.0VSUS 26,82

+12V → +12V 91

+3V → +3V 25,31,44,45,57,91,92

+2P5VPP → +2P5VPP 36,57,84

+1.2V → +1.2V 4,7,15,16,17,18,57,83

+1.0V → +1.0V 7,57,91

+12VS → +12VS 28,57,91

+5VS → +5VS 36,48,50,51,57,61,80,91,97

+3VS → +3VS 3,4,17,20,21,22,23,24,30,31,32,33,36,37,40,45,48,50,51,52,53,57,61,91,92

+1.8VS → +1.8VS 36,48,50,51,57,61,80,91,97

+0.6VS → +0.6VS 15,17,57,83

+VCCPRIM_CORE → +VCCPRIM_CORE 26,82

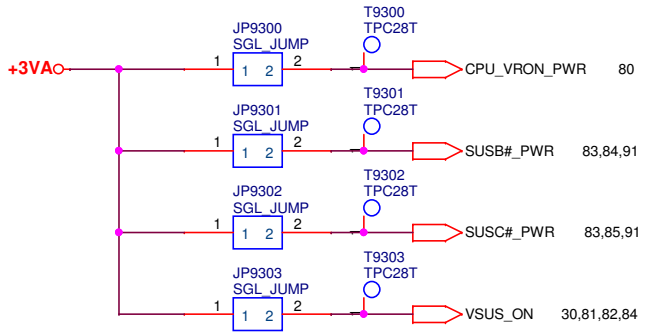
+VCCIO → +VCCIO 3,7,57,91

+VCCSA → +VCCSA 7,57,80

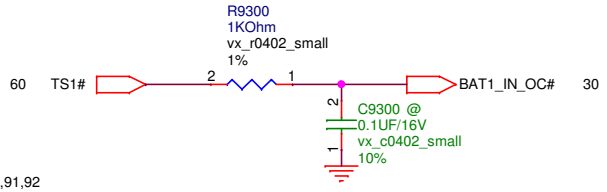
+VCCGT → +VCCGT 6,57,80

+VCORE → +VCORE 5,57,80

FOR POWER TEST



BATTERY IN DETECT



<Variant Name>

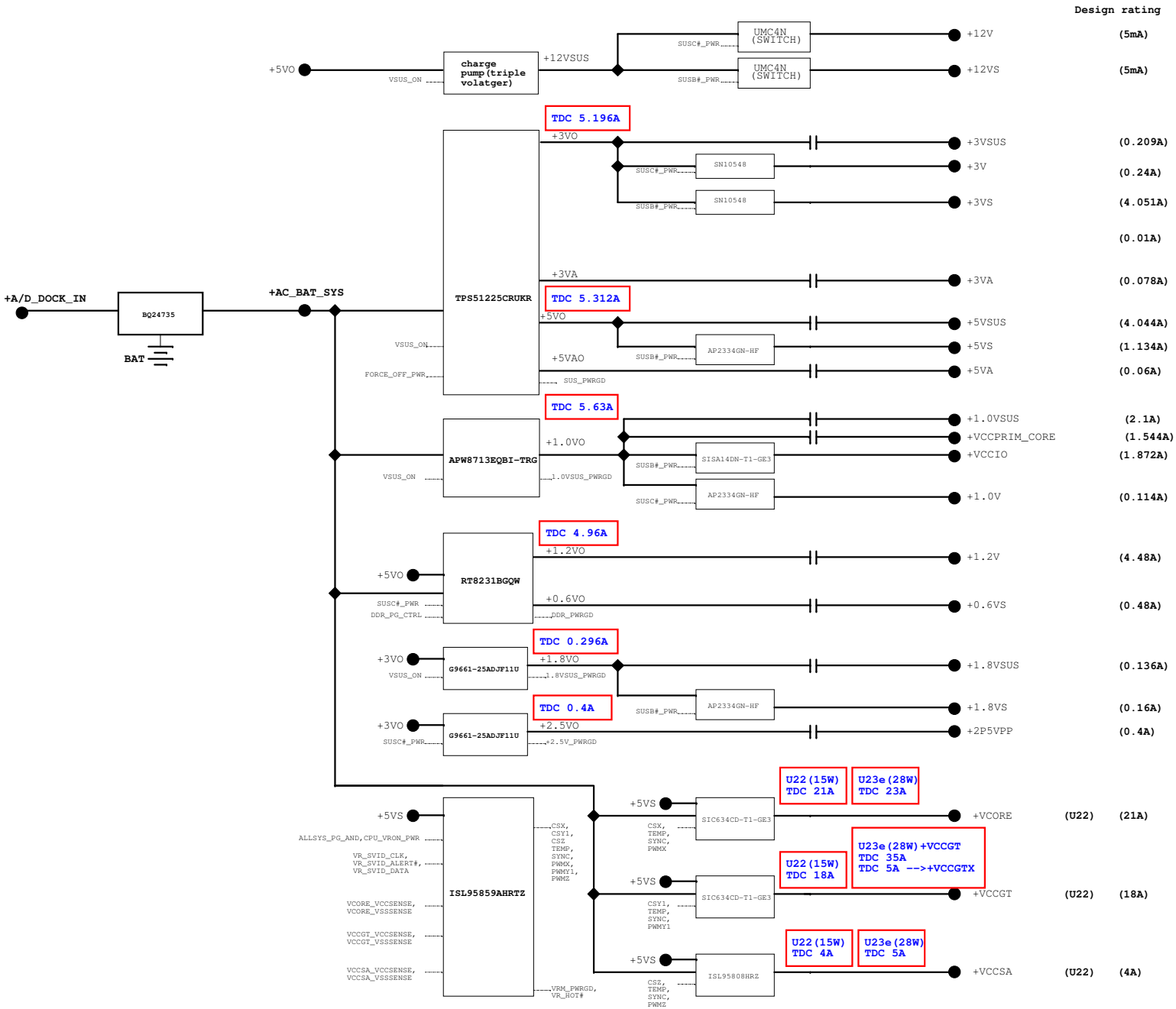
PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title : POWER_SIGNAL

Engineer: James_Liao

Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 93 of 94



<Variant Name>

PEGATRON
PEGATRON PROPRIETARY AND CONFIDENTIAL

Title: POWER_FLOWCHART

Engineer: James_Liao

Size	Project Name	Rev
Custom	SU4EA	1.1

Date: Friday, March 10, 2017 Sheet 94 of 94