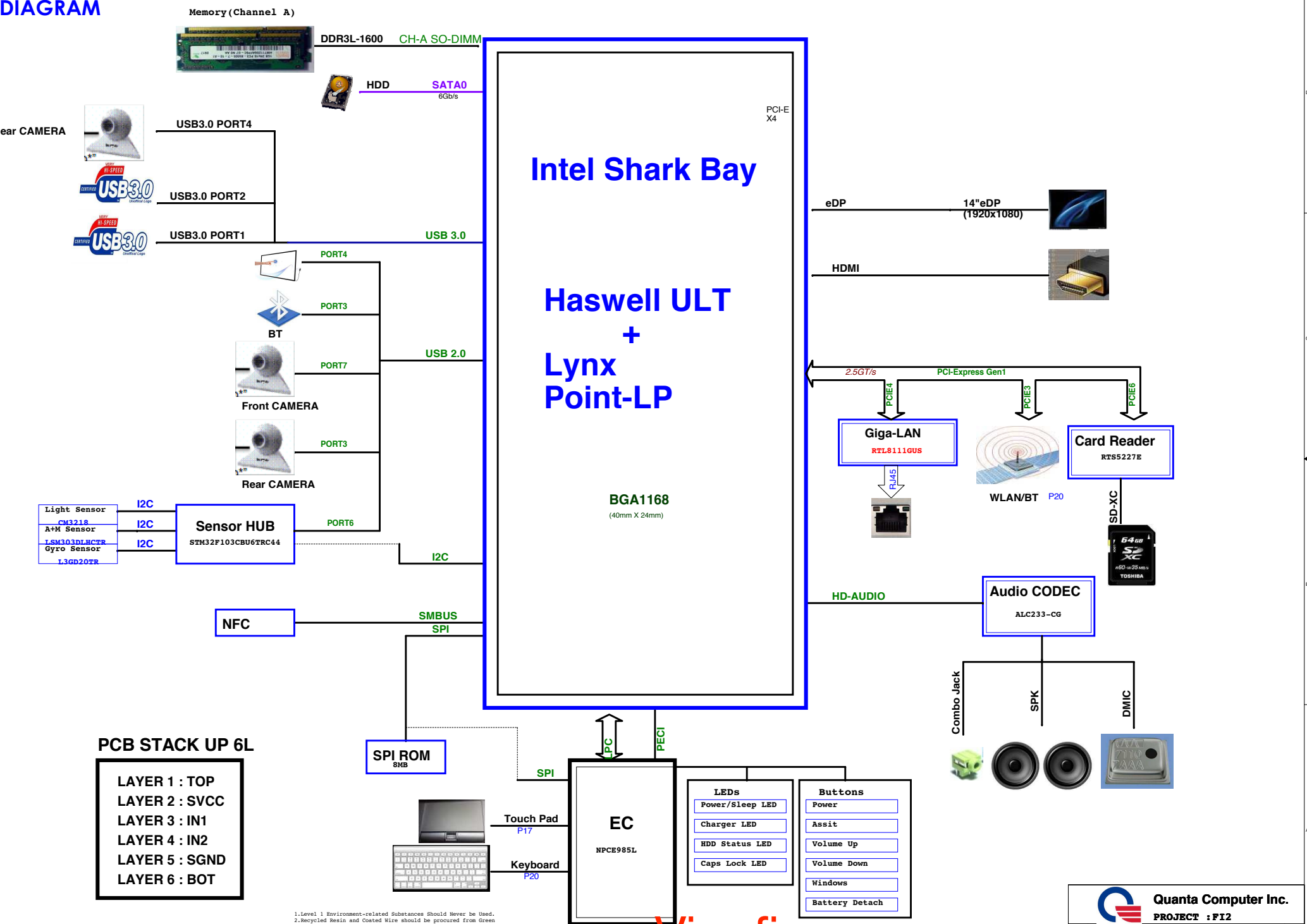


Page	Title of schematic page	Rev.	Date
01	Page List	1A	
02	Block Diagram	1A	
03	Change List	1A	
04	HSW MCP(DISPLAY/Sideband)	1A	
05	HSW MCP(MEMORY/GND)	1A	
06	HSW MCP(CFG/PwrMGT)	1A	
07	HSW MCP(POWER)	1A	
08	HSW PCH(RTC/HDA/SATA)	1A	
09	HSW PCH(PCI/USB)	1A	
10	HSW PCH(CLK/LPC/SPI/SMB)	1A	
11	HSW PCH(GPIO/LPIO/MISC)	1A	
12	HSW PCH(POWER)	1A	
13	DDR3L DIMM1-STD 4H (CH-A)	1A	
14	HOLE/EMI/KB	1A	
15	WPCE985L & FLASH	1A	
16	LVDS\TS\NFC	1A	
17	HDD/Gsensor/TP/FAN	1A	
18	HDMI/THERMAL	1A	
19	USB Charger/IO connector	1A	
20	WLAN/KB-BL	1A	
21	LED	1A	
22	Sensors Hub & Sensors	1A	
23	POWER +VCC_CORE (NCP81101)	1A	
24	POWER 3VPCU&RVCC5(TPS51427)	1A	
25	POWER 1.35VSUS/VTT_MEM	1A	
26	POWER +1.05V(G5602R41U)	1A	
27	POWER VCC1.5/Thermal	1A	
28	POWER(BAT IN / ADA IN/ UL)	1A	
29	POWER CHARGER (ISL88732)	1A	
30	IO PORT LIST	1A	
31	SMBUS	1A	
32	Power Table	1A	
33	Power Sequence	1A	

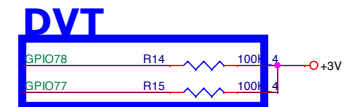
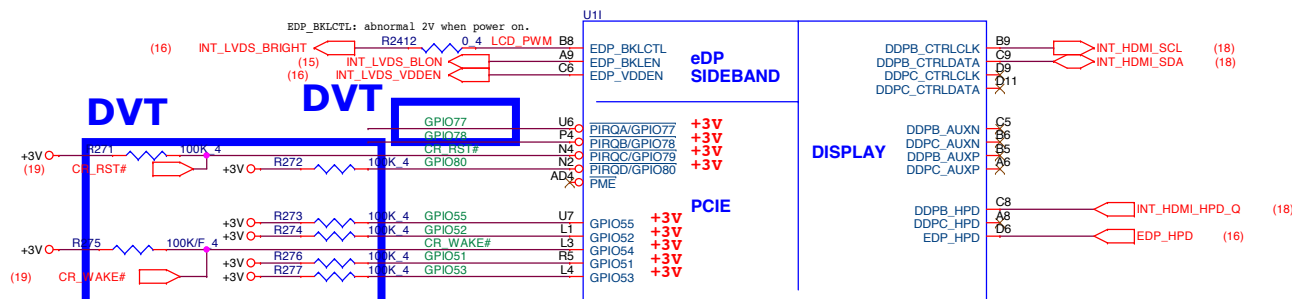
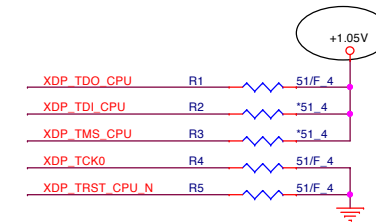
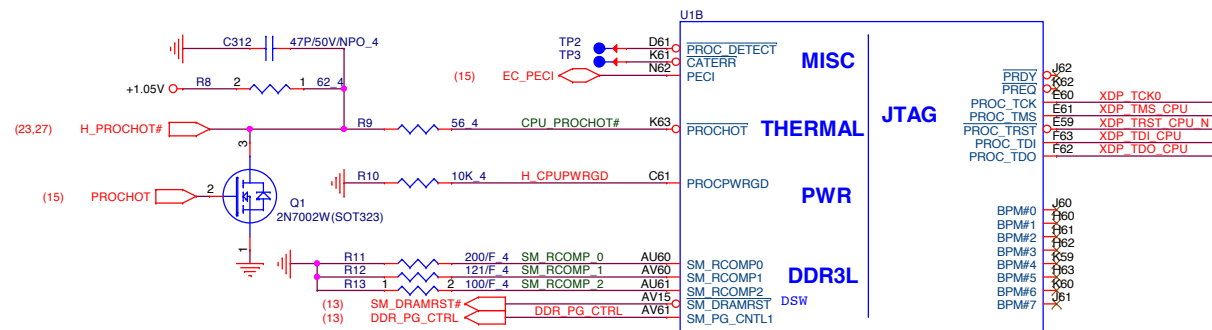
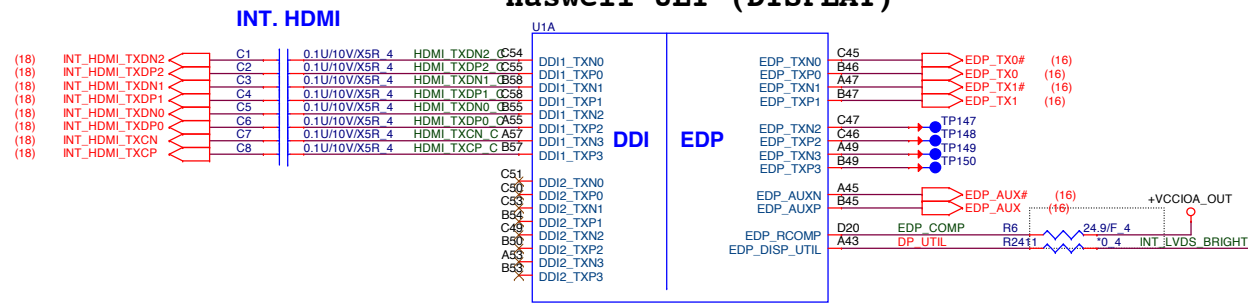
Page	Title of schematic page	Rev.	Date

* : No mount
L@ : For LVDS output
D@ : For eDP output
E@ : For DIS GFX
I@ : For UMA

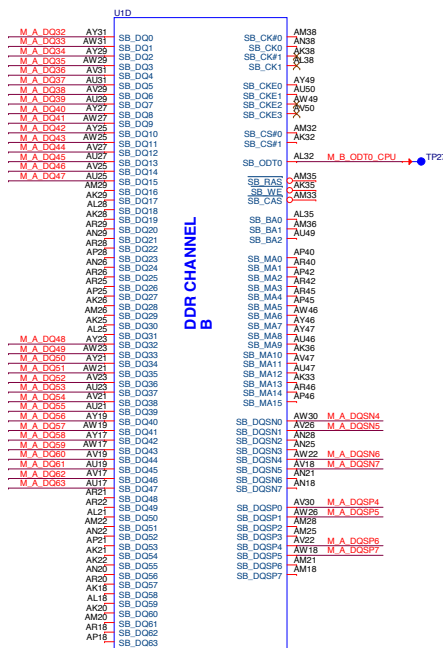
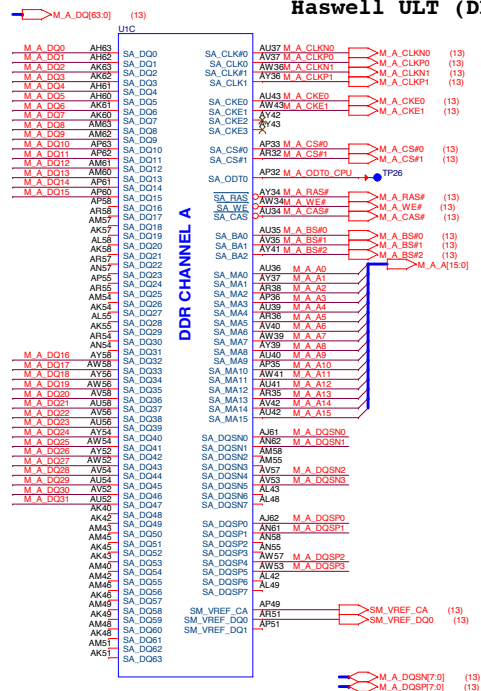
FI2 BLOCK
DIAGRAM



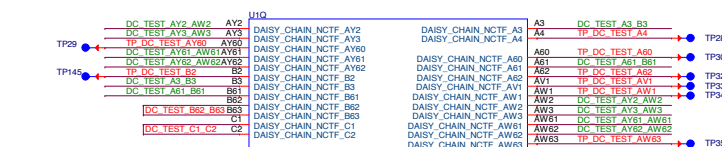
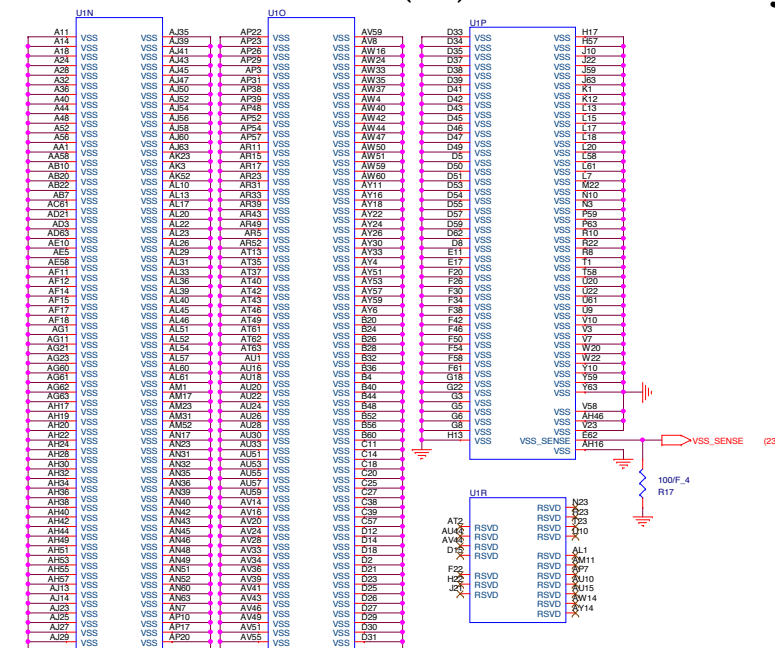
1.Level 1 Environment-related Substances should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

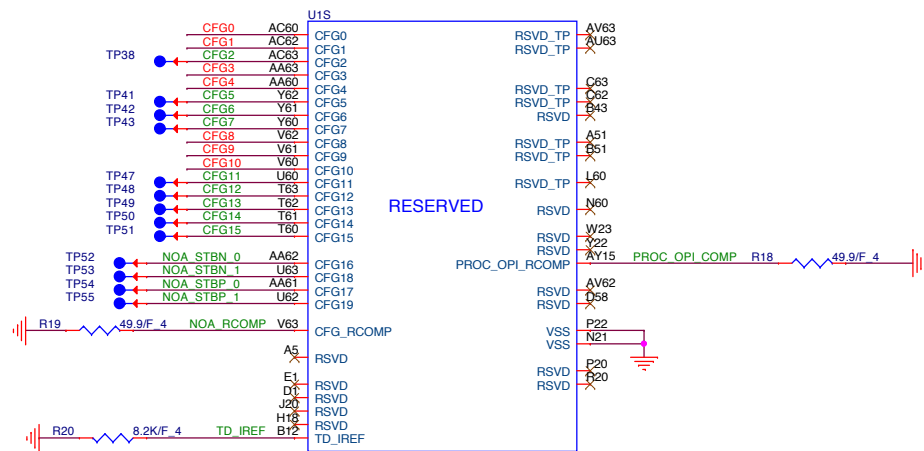


Haswell ULT (DDR3L)



HSW ULT (GND



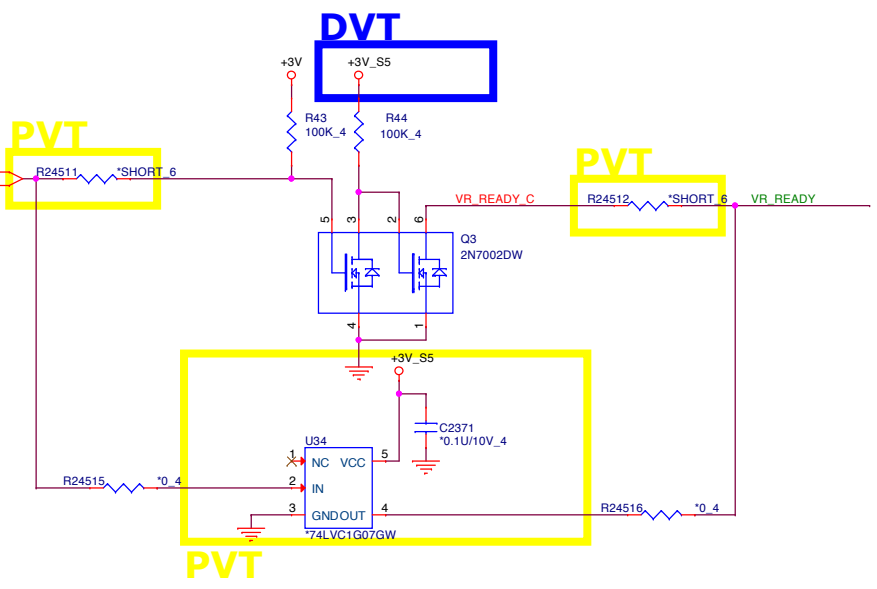
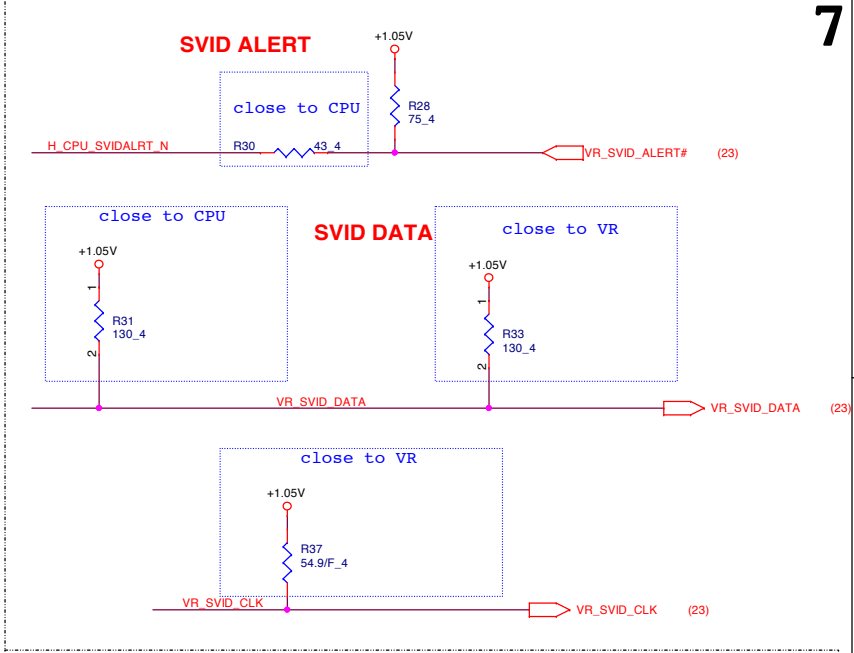
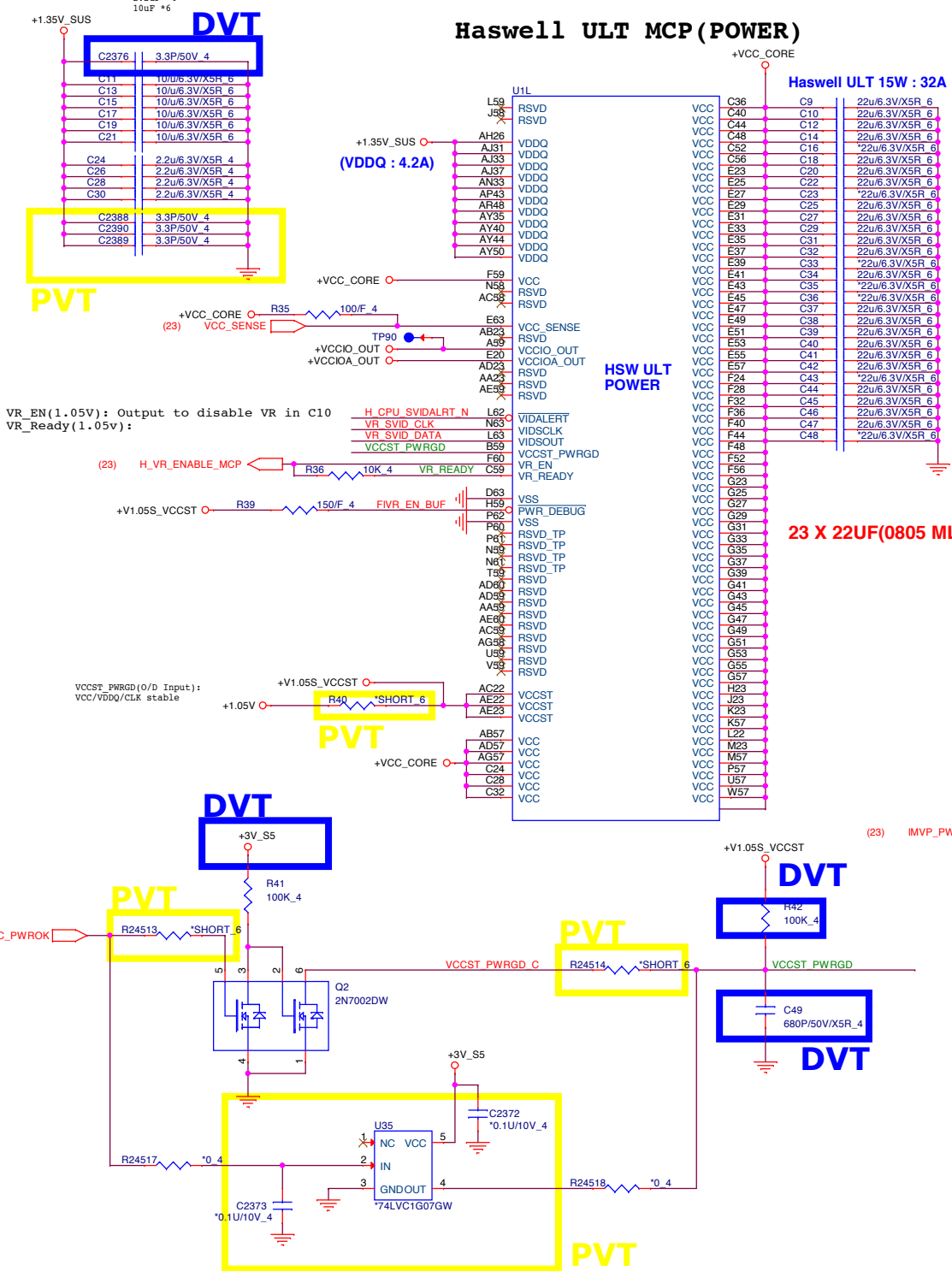


Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	

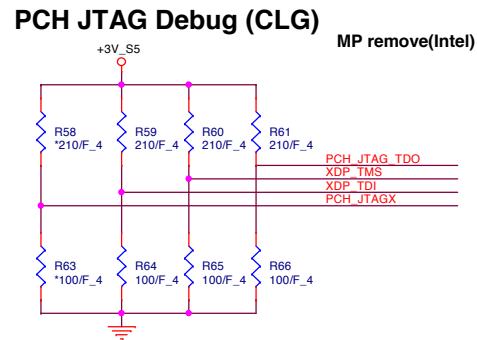
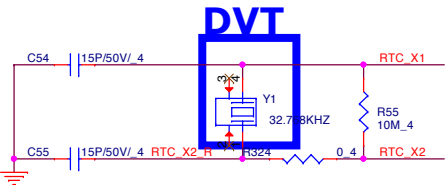
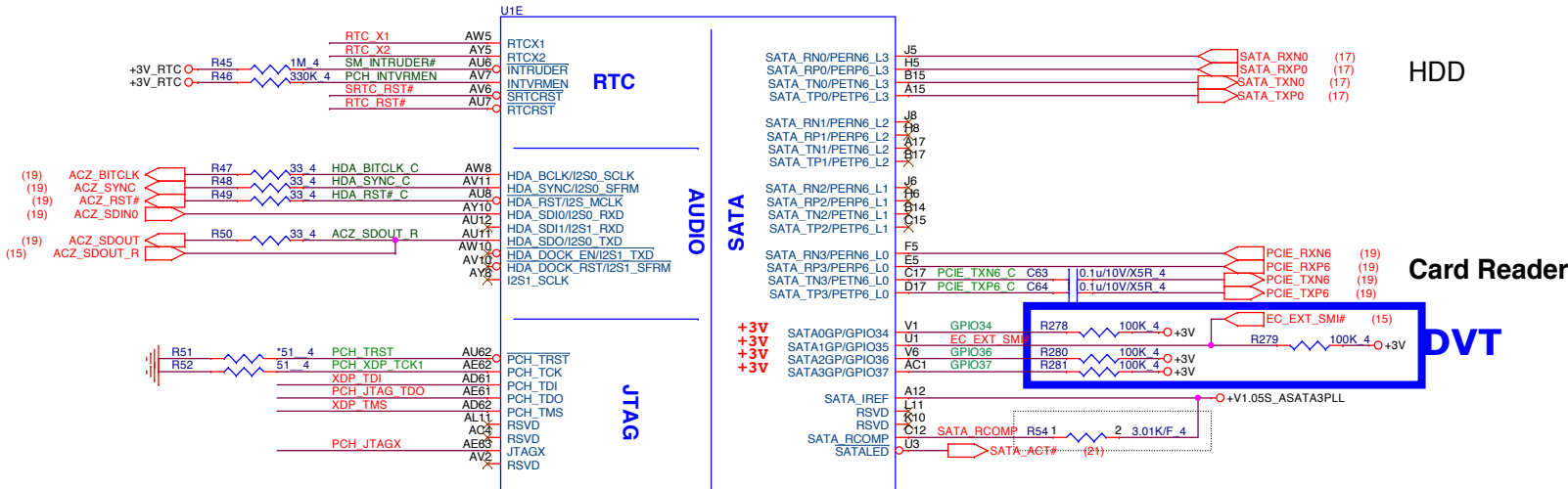


Haswell ULT MCP (POWER)

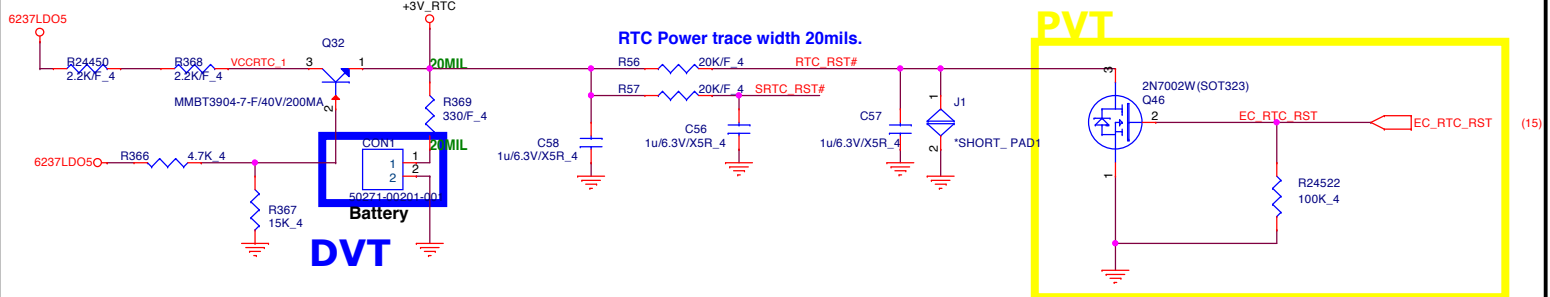


Haswell ULT (RTC, HDA, JTAG, SATA)

8



RTC Circuitry (RTC) (Rechargeable BATT)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V O R67 *1K_4 SPKR (11,19)
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	

Quanta Computer Inc.

PROJECT : F12

HSW PCH(RTC/HDA/SATA)

Size Document Number Rev 1A

Date: Wednesday, August 21, 2013 Sheet 8 of 33

Haswell ULT (CLK)

WIFI/BT(NGFF)

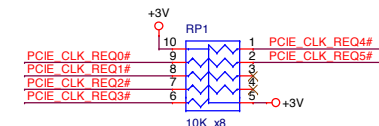
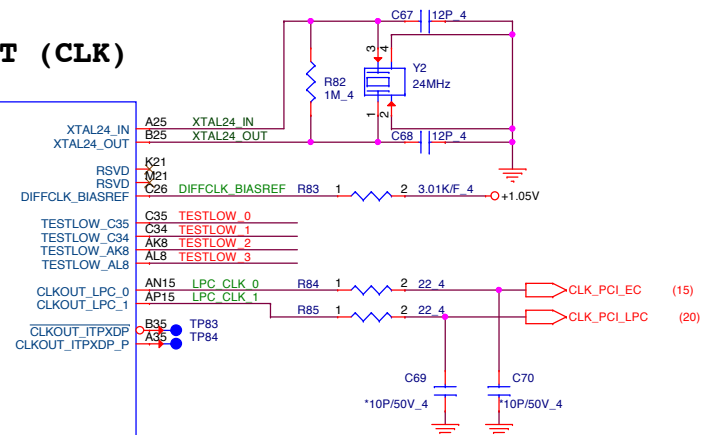
LAN

GFX

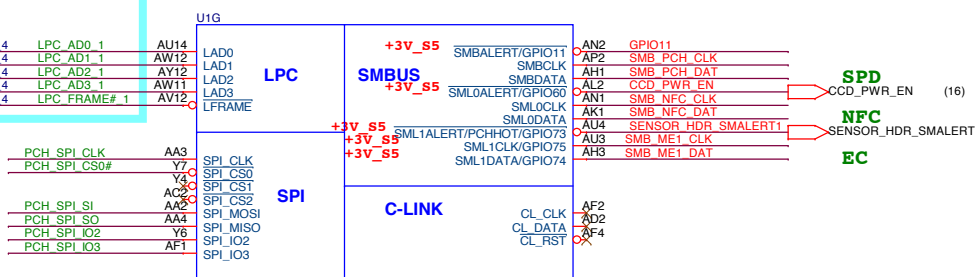
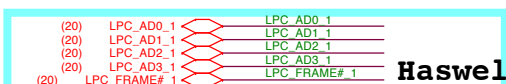
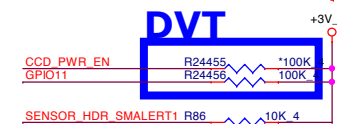
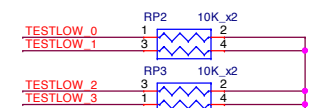
Card Reader

MP

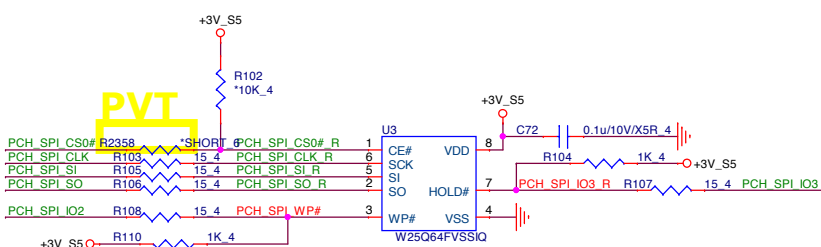
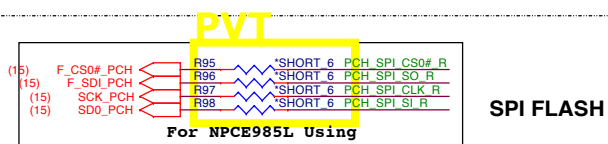
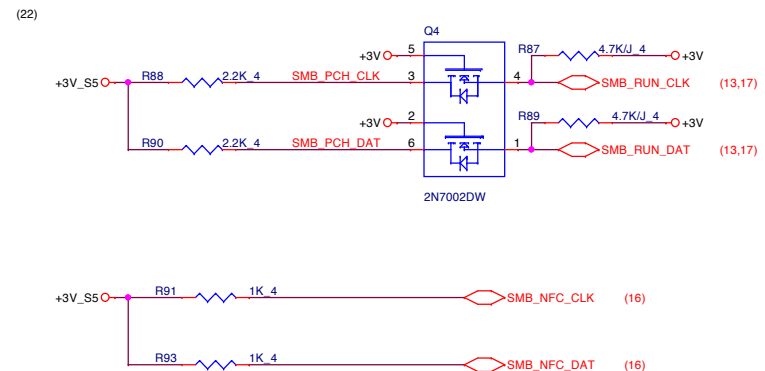
Haswell ULT (LPC/SPI/SMB/CLINK)



Do not short the testlow pins together.



SMBus/Pull-up(CLG)

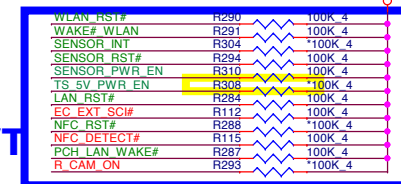


Haswell ULT(GPIO, LPIO, MISC)

GPIO27

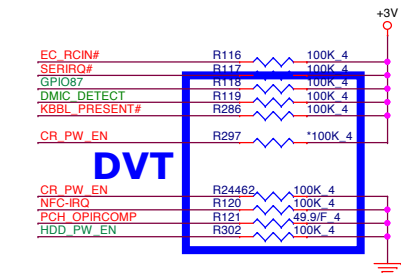
With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSX

GPIO Pull-up/Pull-down(CLG)



PVT

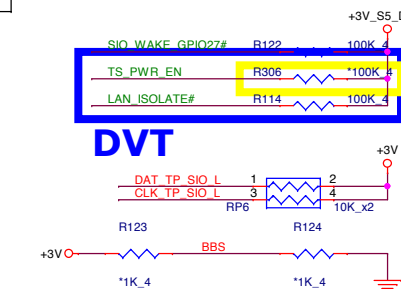
DVT



DVT

PVT

DVT



GPIO86	
PU	LPC
PD	SPI (Default IPD)

No Reboot Strap(GPIO81)

NC	Default
PU	EN

TLS CONFIDENTIALITY STRAP(GPIO15)

NC	Default
PU	EN

Quanta Computer Inc.
PROJECT : F12

Size	Document Number	Rev
		1A
HSW PCH(GPIO/LPIO/MISC)		
Date	Wednesday, August 14, 2013	Sheet 11 of 33

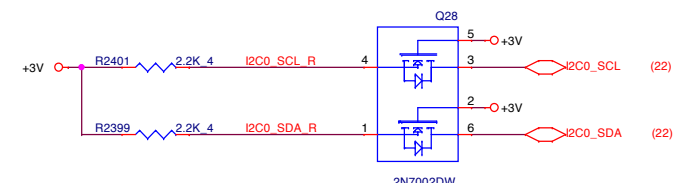
DSW
CPU/
MISC

SERIAL

+3V	GPIO_CS/GPIO83
+3V	GPIO_CLK/GPIO84
+3V	GPIO_MISO/GPIO85
+3V	*GPIO_MOSI/GPIO86
+3V	GPIO_CS/GPIO87
+3V	GPIO_CLK/GPIO88
+3V	GPIO_MISO/GPIO89
+3V	GPIO_MOSI/GPIO90
+3V	UART0_RXD/GPIO91
+3V	UART0_TXD/GPIO92
+3V	UART0_RTS/GPIO93
+3V	UART0_CTS/GPIO94
+3V	UART1_RXD/GPIO0
+3V	UART1_TXD/GPIO1
+3V	UART1_RTS/GPIO2
+3V	UART1_CTS/GPIO3
+3V	I2C0_SDA/GPIO4
+3V	I2C0_SCL/GPIO5
+3V	I2C1_SDA/GPIO6
+3V	I2C1_SCL/GPIO7
+3V	SDIO_CLK/GPIO64
+3V	SDIO_CMD/GPIO65
+3V	SDIO_D0/GPIO66
+3V	SDIO_D1/GPIO67
+3V	SDIO_D2/GPIO68
+3V	SDIO_D3/GPIO69

DMIC_DETECT:
High : Single DMIC
Low : Dual DMIC

GPIO66	
High	ENABLE
NC	DISABLE(Default)



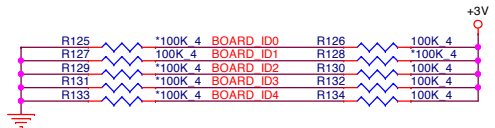
2N7002DW

DVT

DVT

DVT

DVT



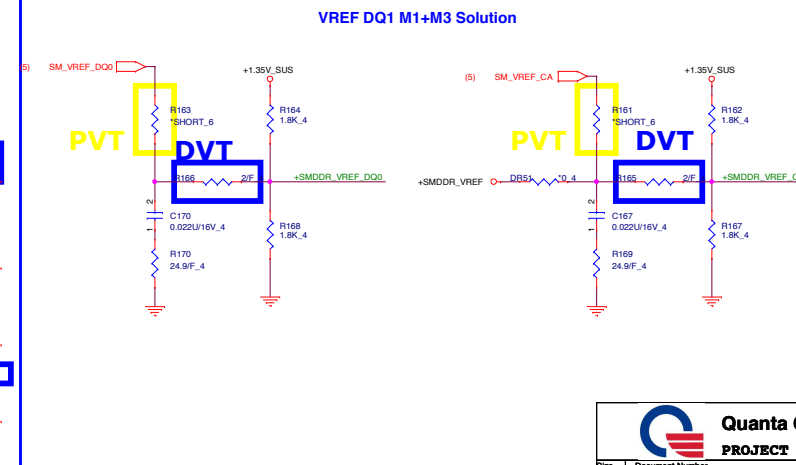
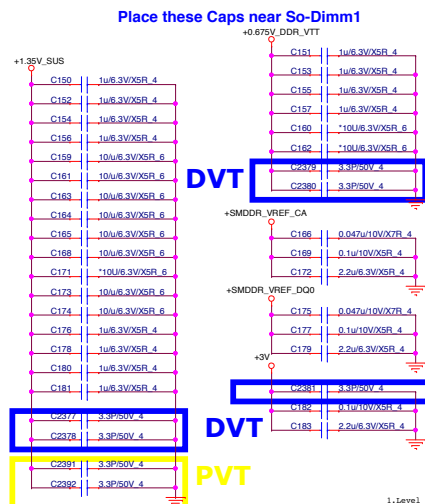
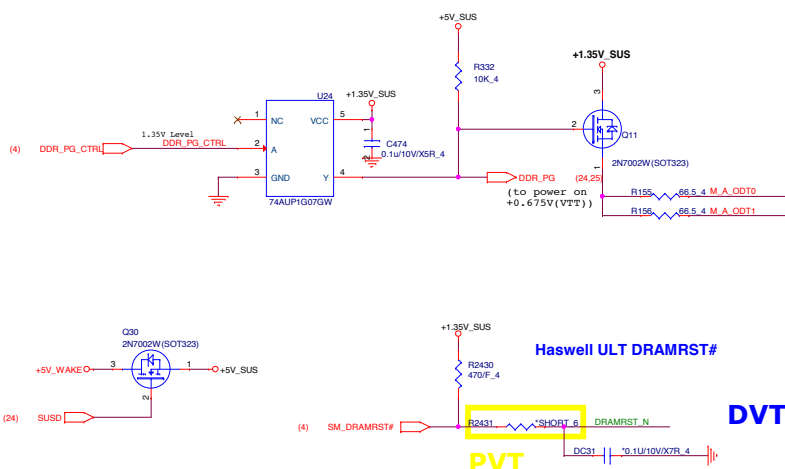
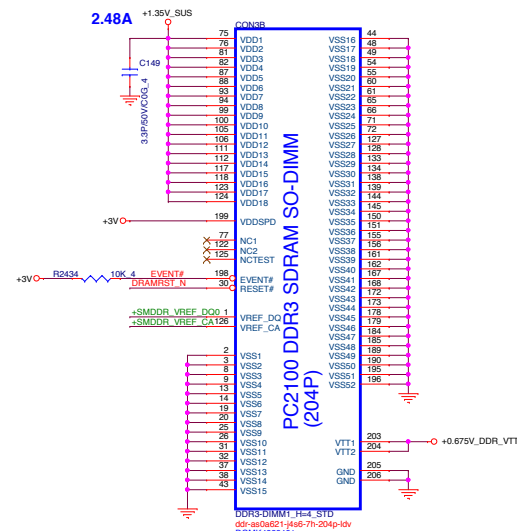
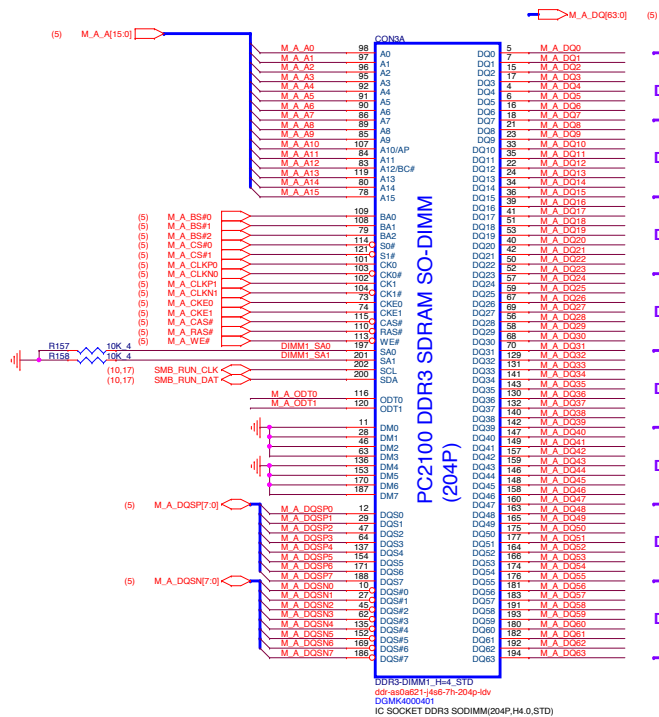
R127(Low)
R128(High)

R125(Low)
R126(High)

	Board ID1	Board ID0
Mule F11	0	0
HuronSH1 F12	0	1
HuronSHB1 F13_UMA	1	0
HuronSHB1 F13_DGPU	1	1



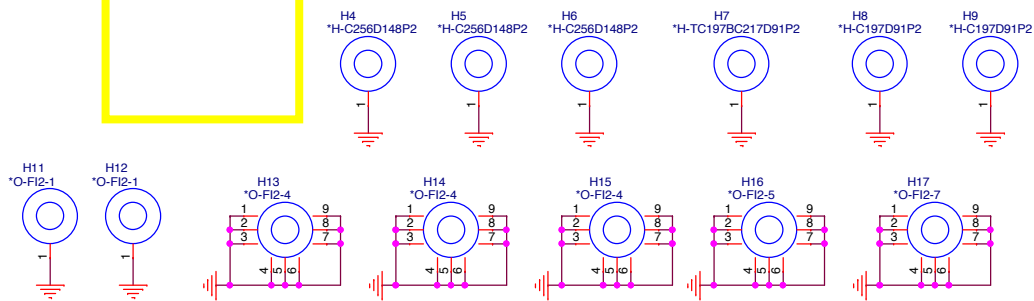
PCBA SKU	Discrete	UMA
R135(Pull High)	Stuff	No Stuff
R136(Pull Low)	No Stuff	Stuff



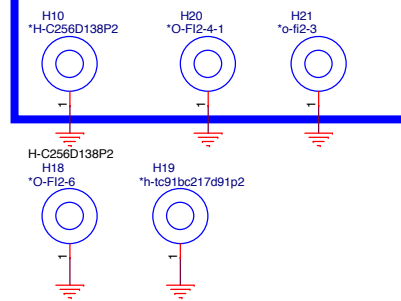
- 1.Level 1 Environment-related Substances Should Never be Used.
- 2.Recycled Resin and Coated Wire should be procured from Green Partners.

HOLE

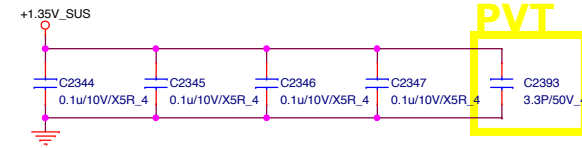
PVT



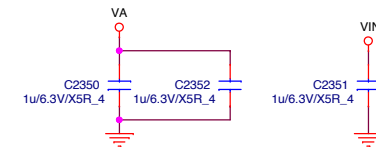
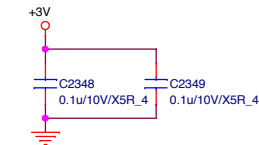
DVT



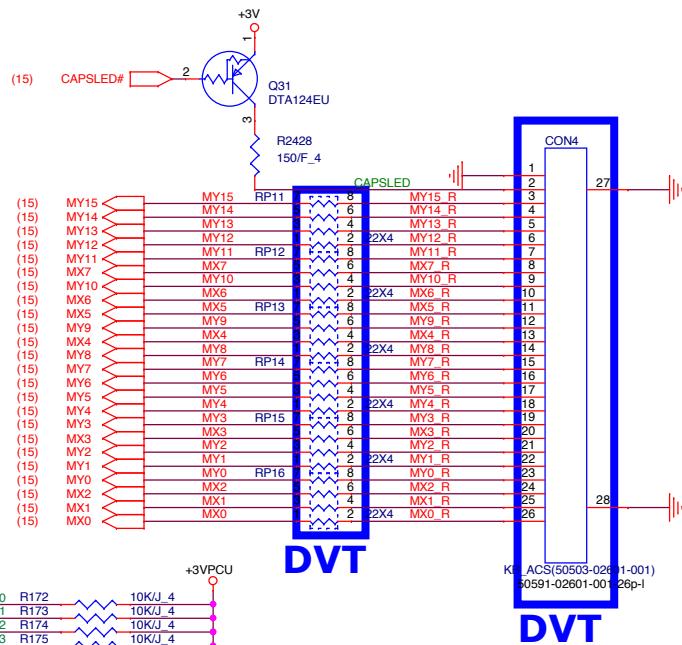
EMI



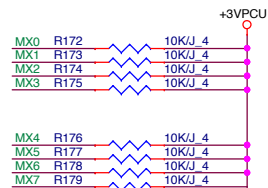
14



KEYBOARD Connector



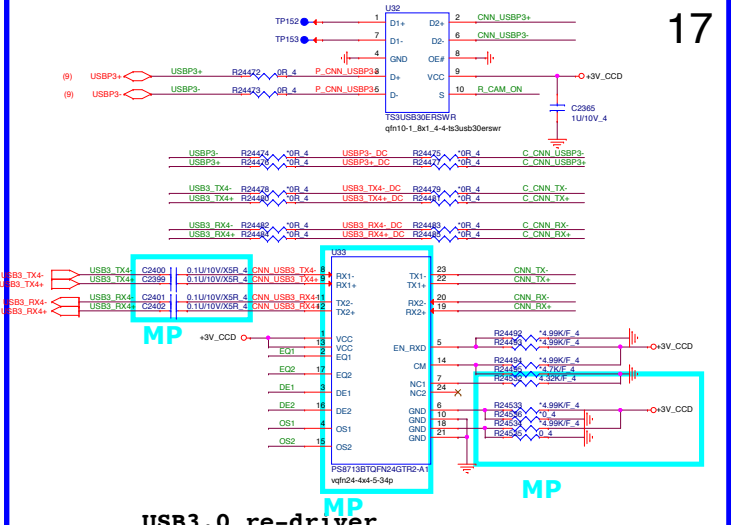
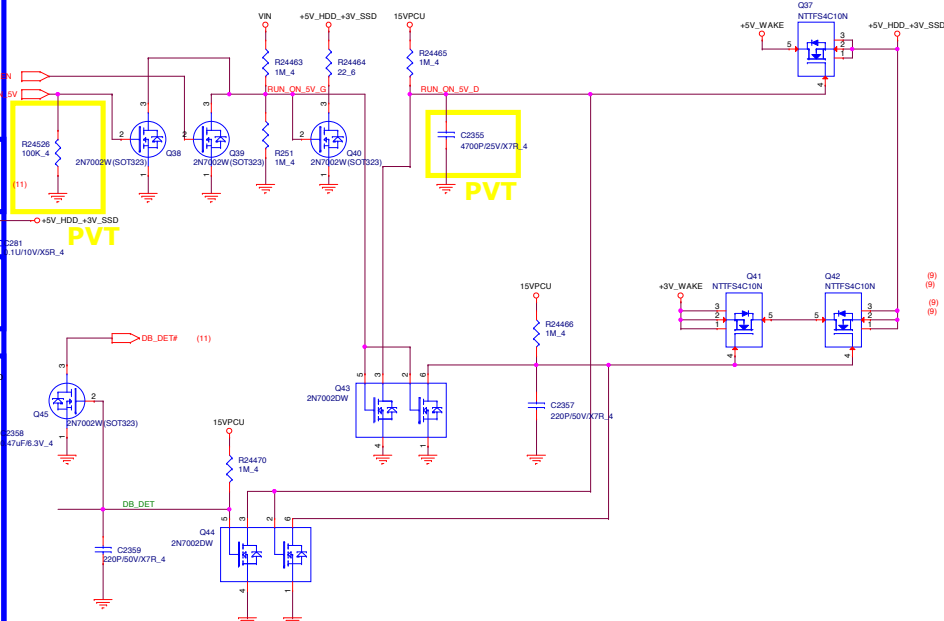
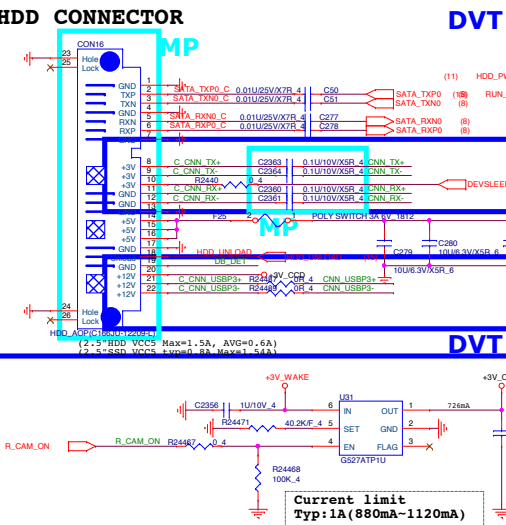
CAPSLED	C298	*0.1U/10V/X5R_4
MX0	C184	220P_4
MX1	C185	220P_4
MX2	C186	220P_4
MY0	C187	220P_4
MY1	C188	220P_4
MY2	C189	220P_4
MX3	C190	220P_4
MY3	C191	220P_4
MY4	C192	220P_4
MY5	C193	220P_4
MY6	C194	220P_4
MY7	C195	220P_4
MY8	C196	220P_4
MX4	C197	220P_4
MY9	C198	220P_4
MX5	C199	220P_4
MX6	C200	220P_4
MY10	C201	220P_4
MX7	C202	220P_4
MY11	C203	220P_4
MY12	C204	220P_4
MY13	C205	220P_4
MY14	C206	220P_4
MY15	C207	220P_4

K0 ACS(50503-02601-001)
50591-02601-001 26p-I

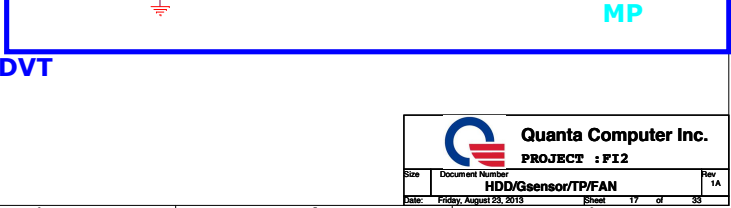
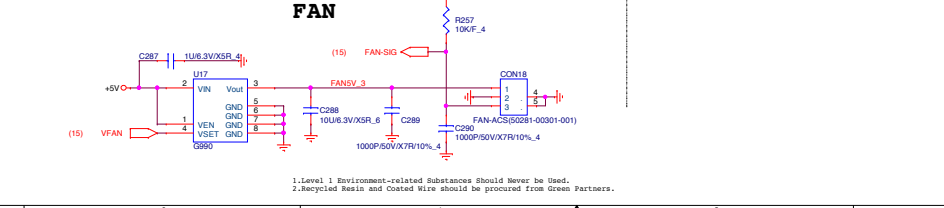
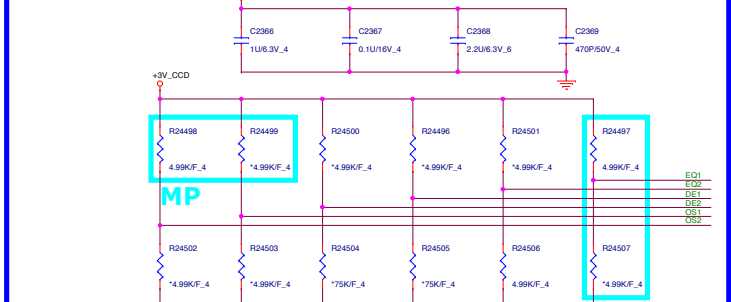
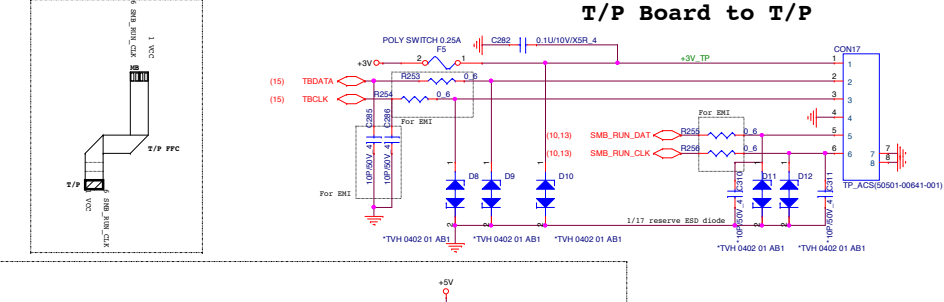
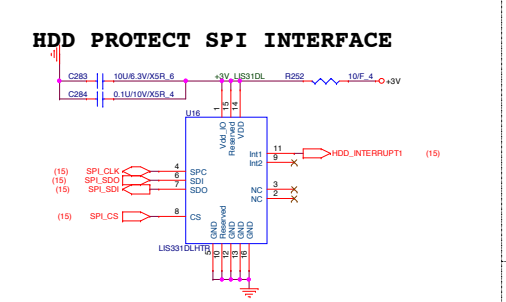
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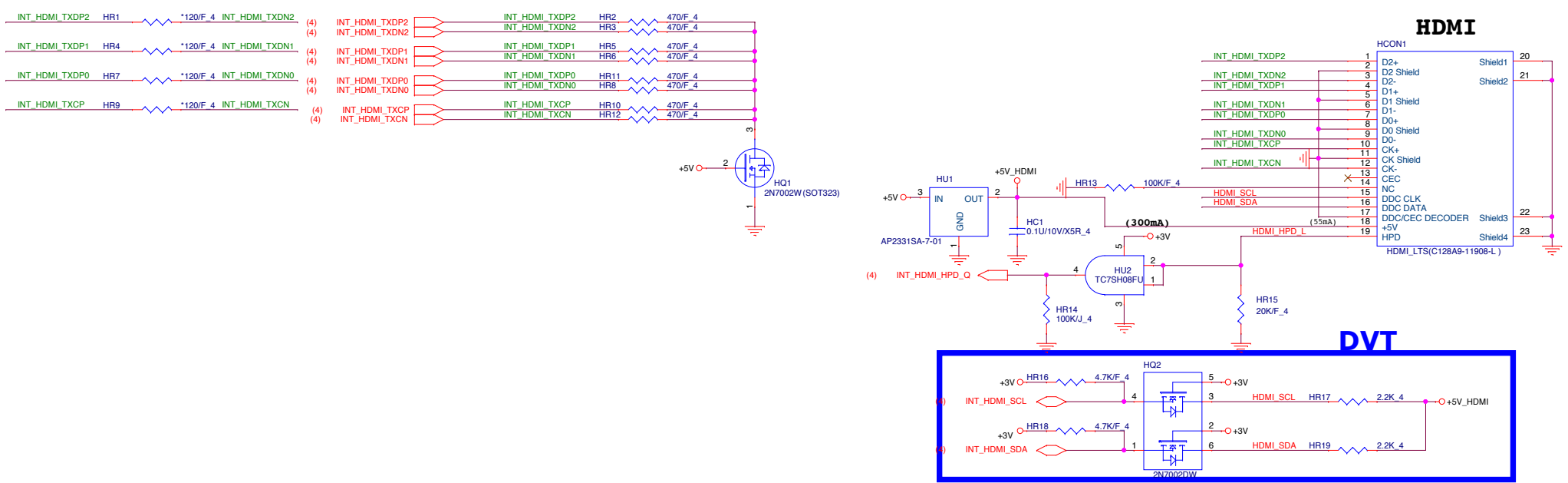
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

		Quanta Computer Inc.	
		PROJECT :FI2	
Size	Document Number	HOLE/EMI/KB	
Date:	Friday, August 16, 2013	Sheet	14 of 33
		Rev	1A

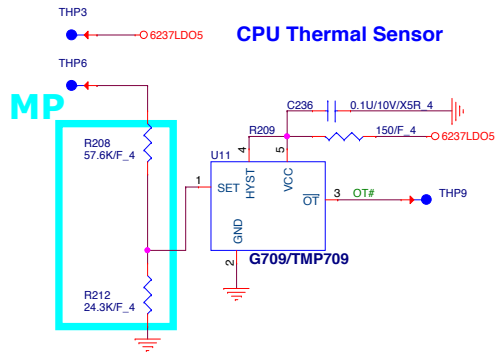


Control pins setting			
EN_RXD	Device function	CM	Device function
1(default)	Normal Operation	0(default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode

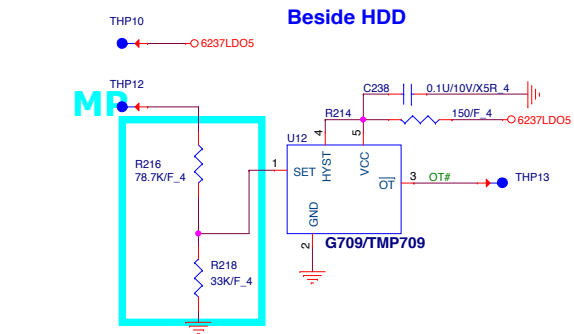




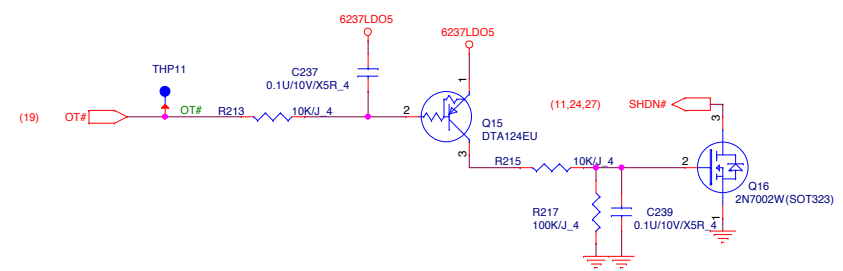
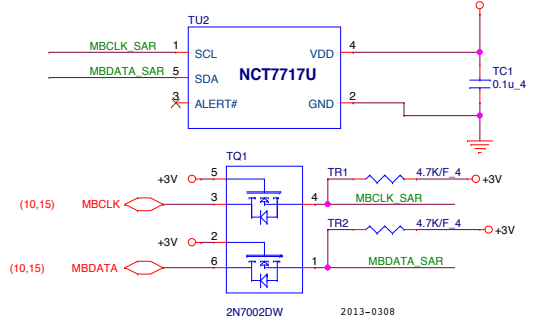
H/W Thermal Protect



Move to Daughter Board



Motherboard ambient temperature

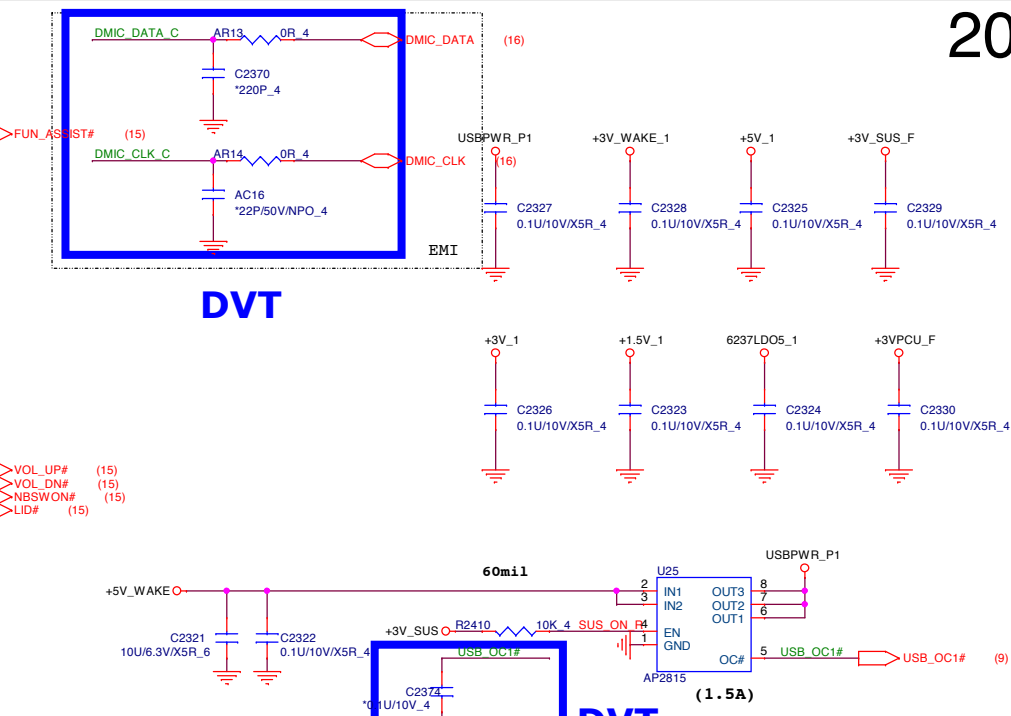
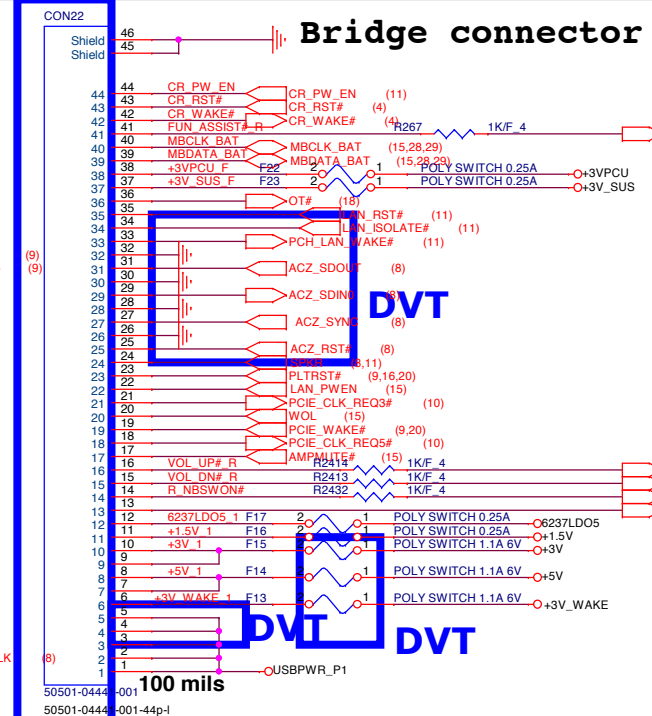
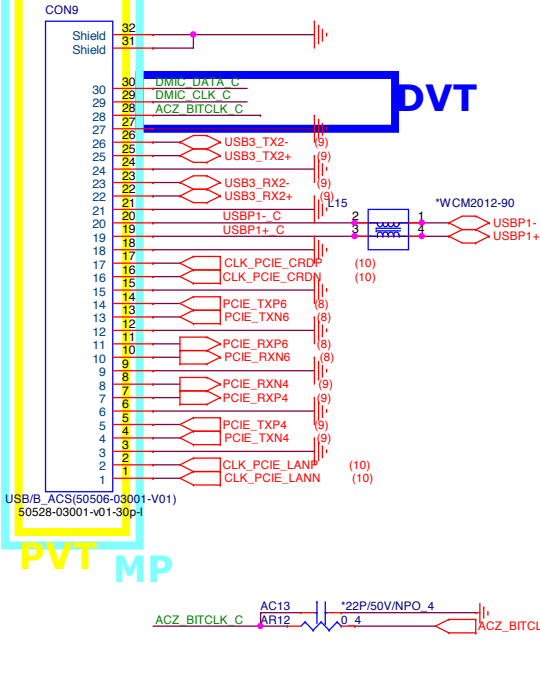


UMA SKU					
Location of IC	Temp	R-Set	Parts in BOM	Max	Min
Near CPU sensor temp	TBD	R208=68K	68K	TBD	TBD
Near AUDIO sensor temp	TBD	R216=113K	113K	TBD	TBD

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

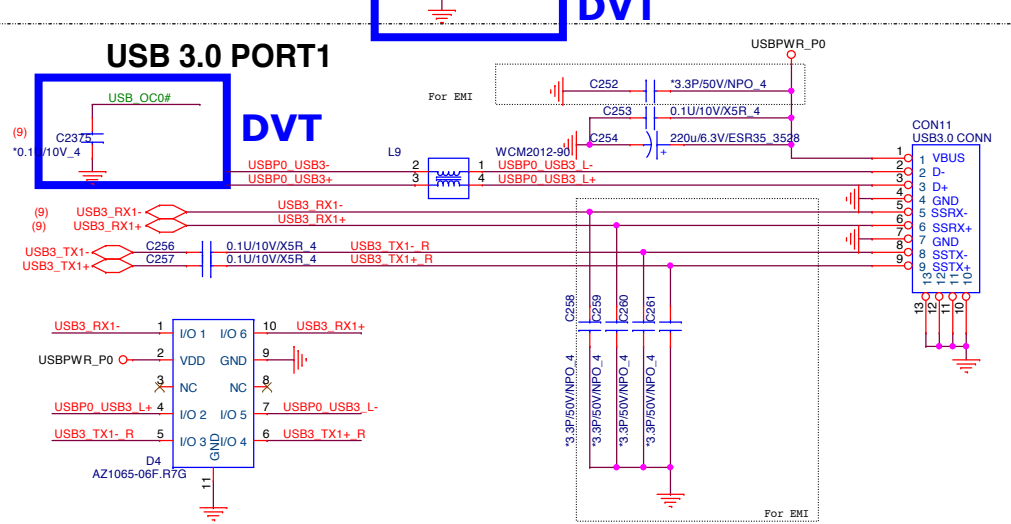
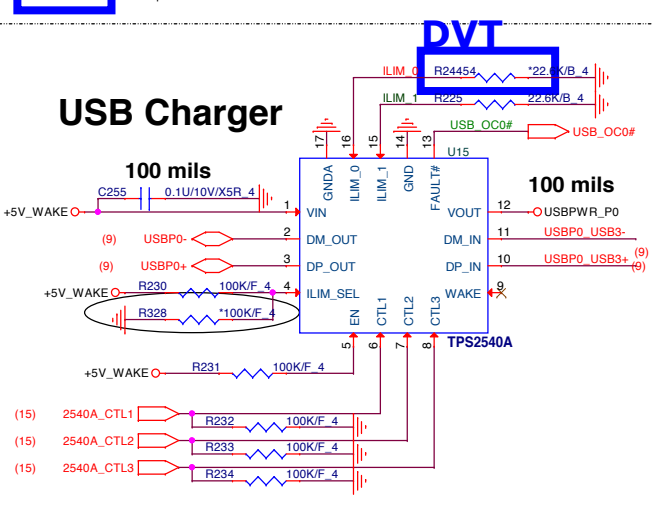
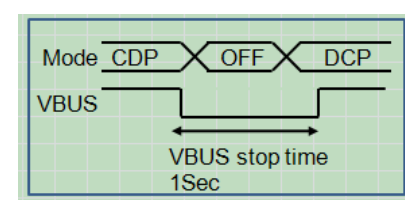
Quanta Computer Inc.
PROJECT : F12

Size	Document Number	Rev
	HDMI/Thermal	1A
Date:	Wednesday, August 14, 2013	Sheet 18 of 33



	TPS2540A		TPS2543	
ILIM_SEL	Pin15	Pin16	Pin15	Pin16
High	V			V
Low		V	V	


SDP : Standard Downstream Port
CDP : Charging downstream port
DCP : Dedicated Charging Port
Enable/Disable : setting by BIOS



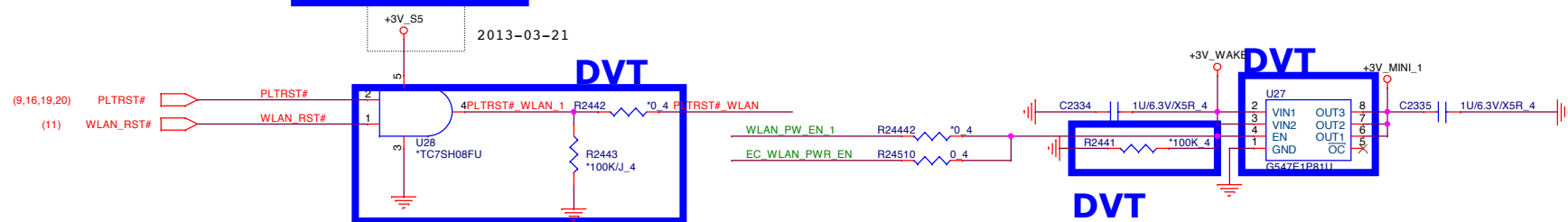
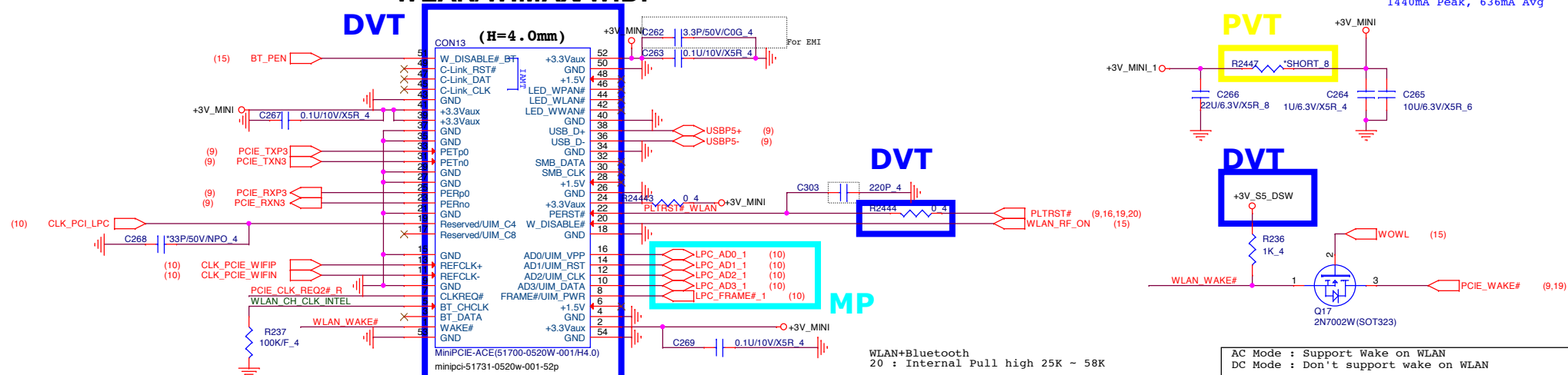
CTL_1	CTL_2	CTL_3	TPS 2540A/2543 Truth Table
0	0	0	OUT discharge, power switch OFF
0	X	1	DCP, Auto-detect(S3/S4/S5, 1.5A)
X	1	0	SDP, USB2.0 mode(S0, 0.5A)
1	0	0	DCP, BC SPEC1.2 only(S3/Deep standby/S4/S5, 1.5A)
1	0	1	DCP, Divider mode only(S3/S4/S5, 1.5A)
1	1	1	CDP (S0, 1.5A)

System State	USB Battery Charging Setting	
	Disable C(1 2 3)	Enable C(1 2 3)
S0	SDP (X 1 0)	CDP (1 1 1)
S3	SDP (X 1 0)	DCP BC (1 0 0)
DS3	Charger OFF (0 0 0)	DCP BC (1 0 0)
S4	Charger OFF (0 0 0)	DCP BC (1 0 0)
S5	Charger OFF (0 0 0)	DCP BC (1 0 0)

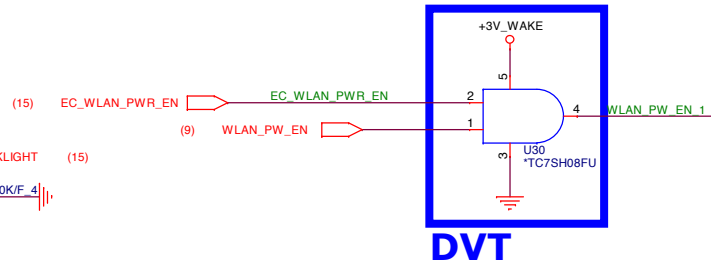
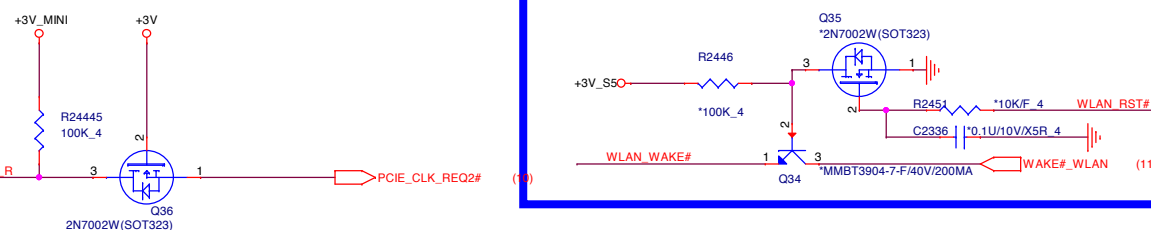
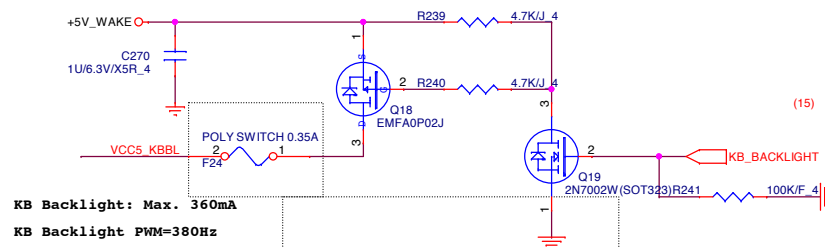
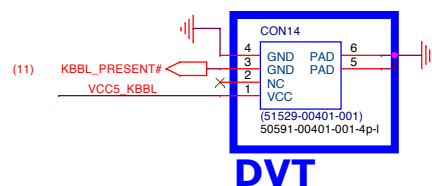
ILIM_SEL (I LIMIT(A)= 48000/R)		
HI	I_LIM_1	
LO	I_LIM_0	48000/22.6K=2.123A

		Quanta Computer Inc. PROJECT : F12	
Size	Document Number	USB Charger/IO connector	Rev 1A
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WLAN/WIMAX/WIDI



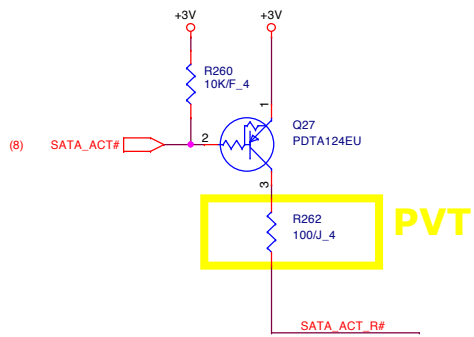
KB BACKLIGHT



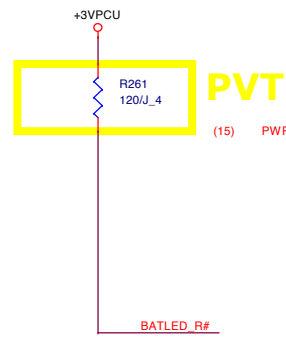
2013-03-21



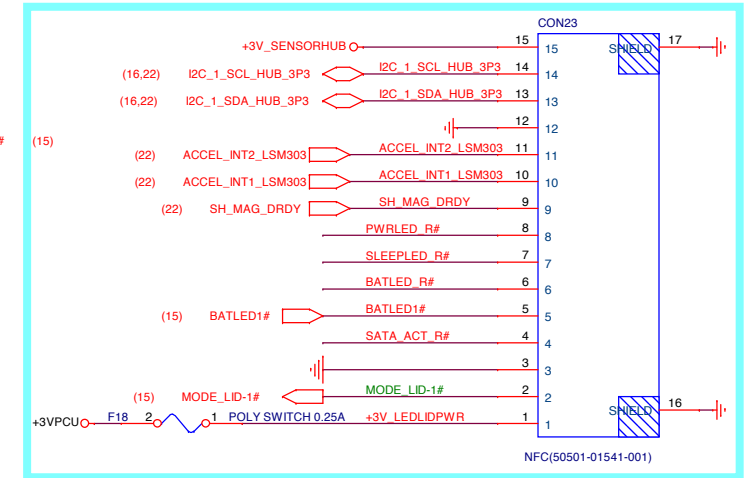
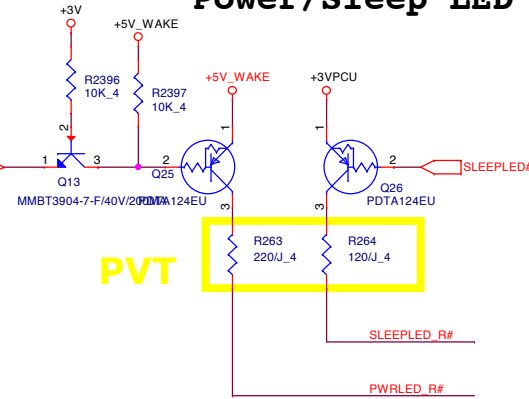
SATA LED



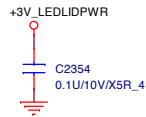
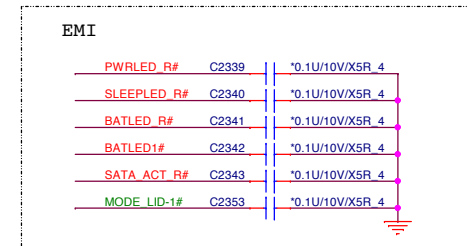
BATTERY LED

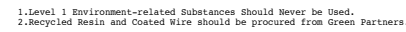


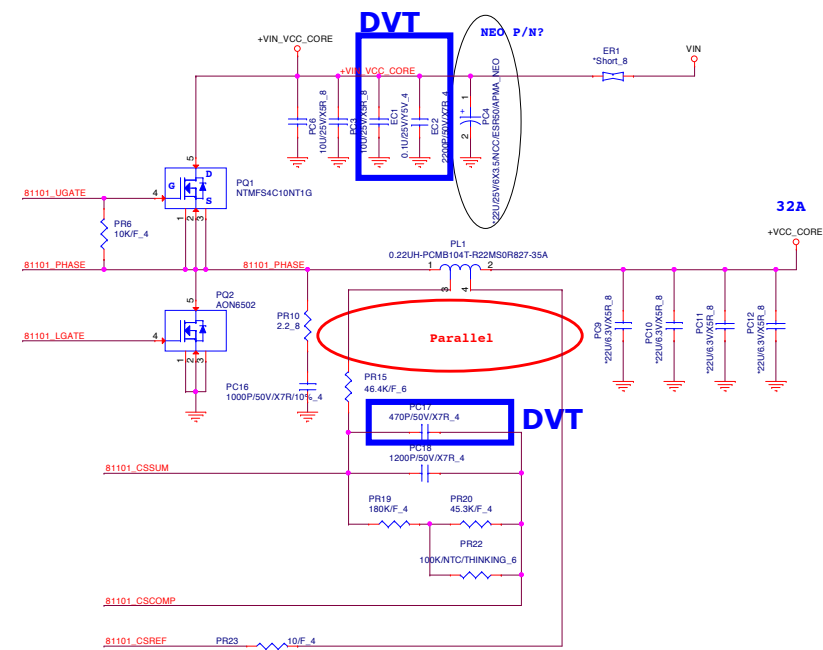
Power/Sleep LED

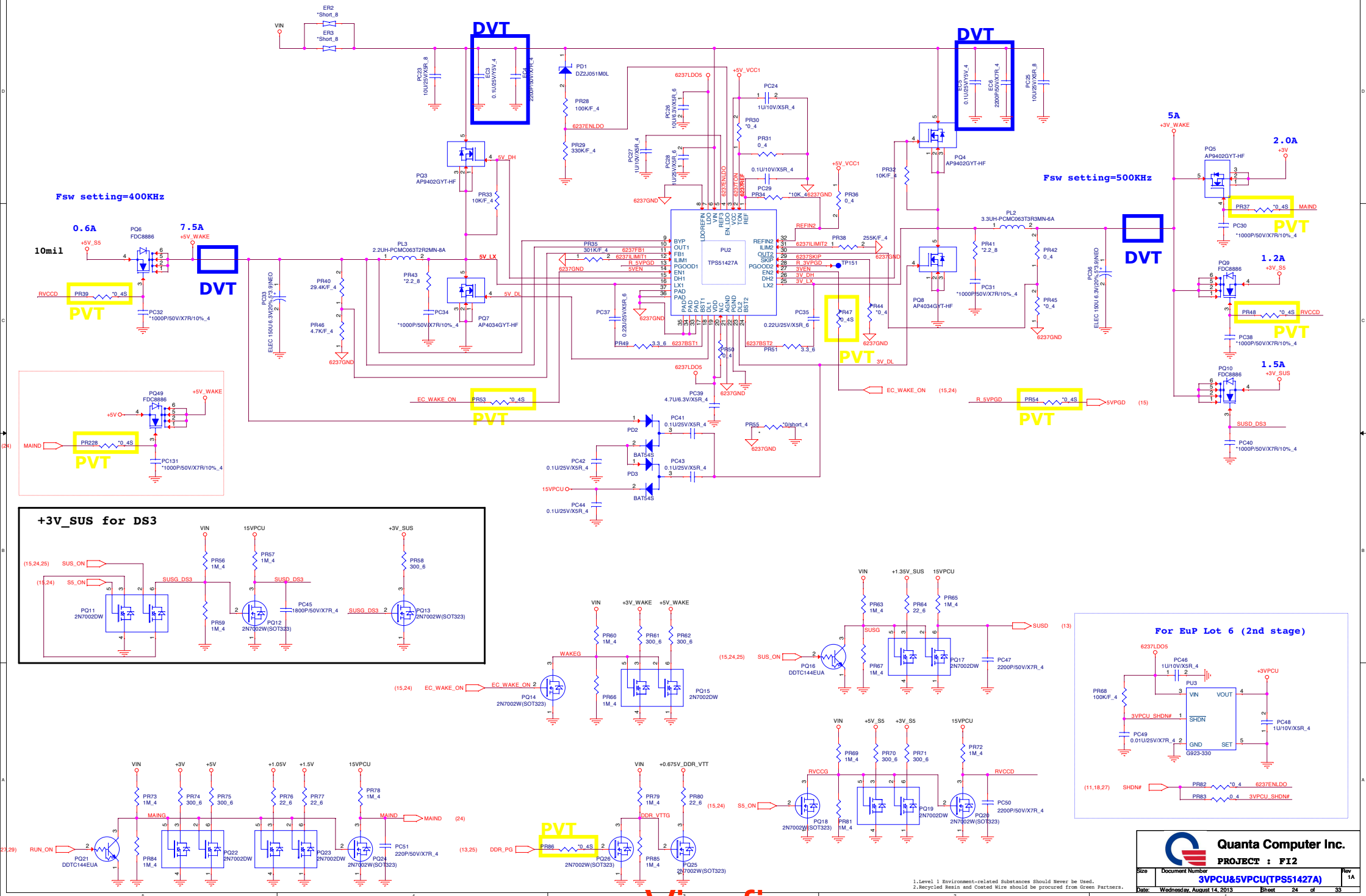


MP

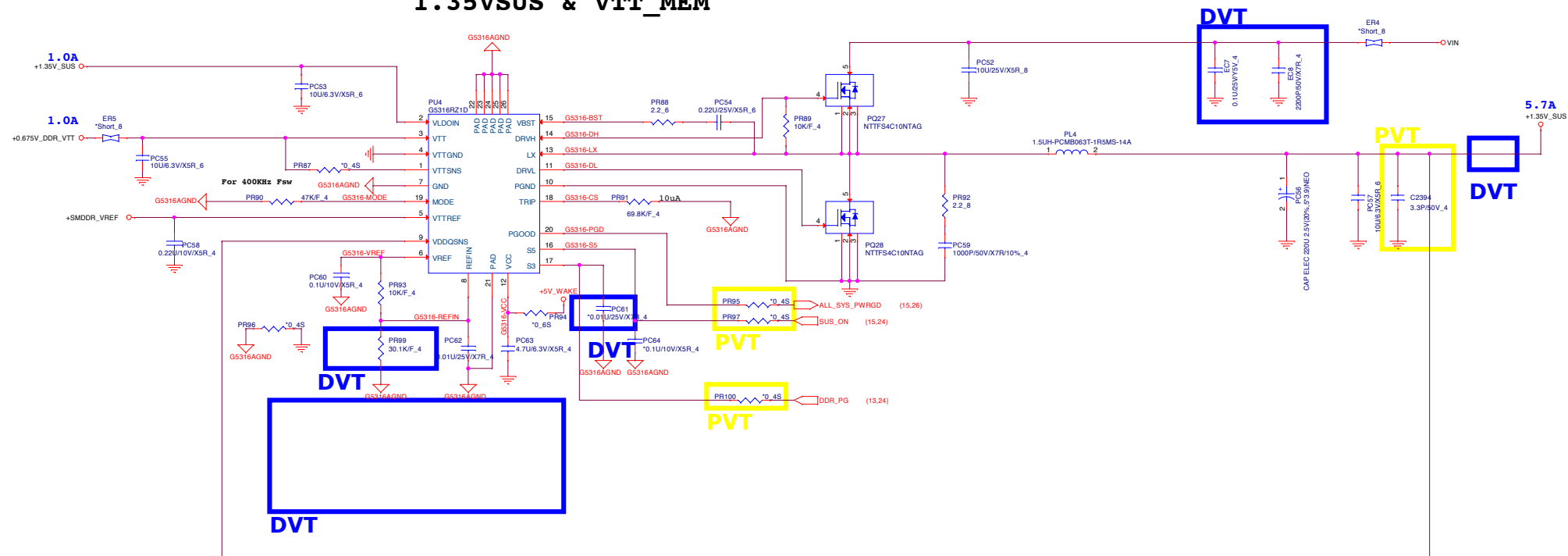








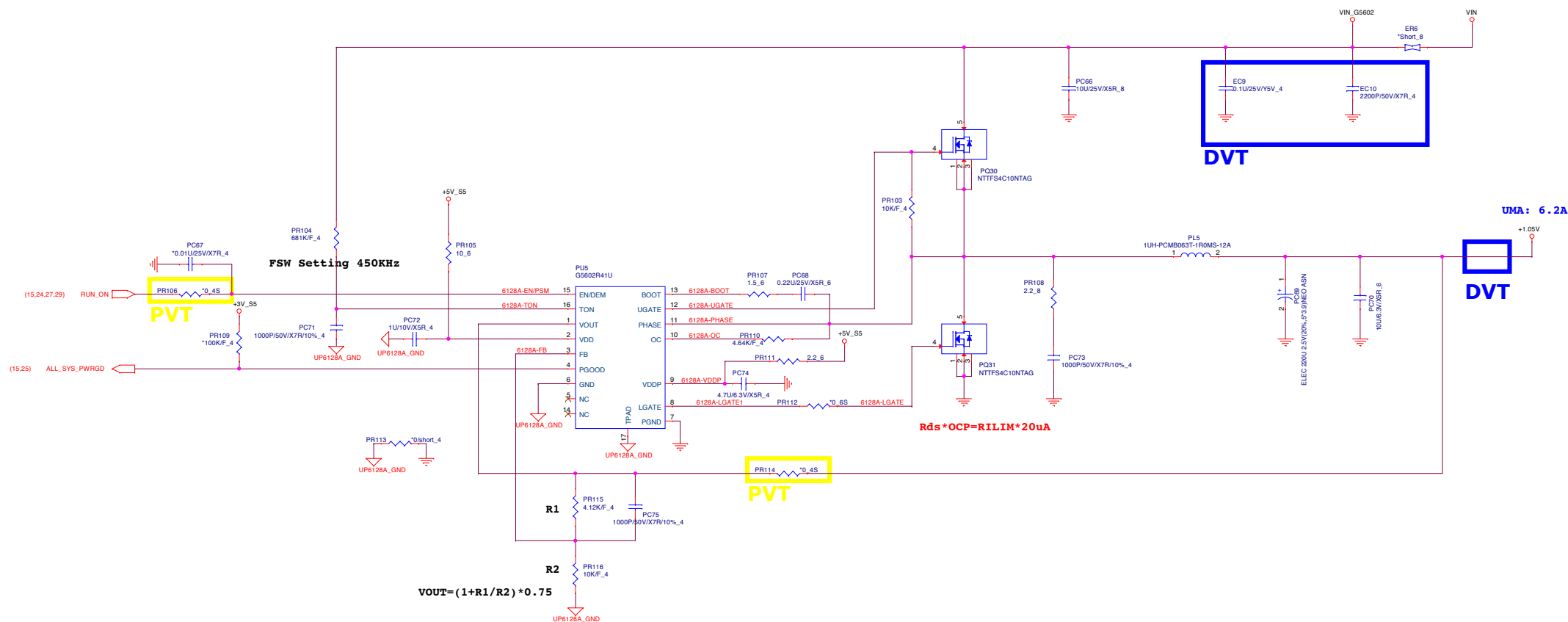
1.35VSUS & VTT MEM



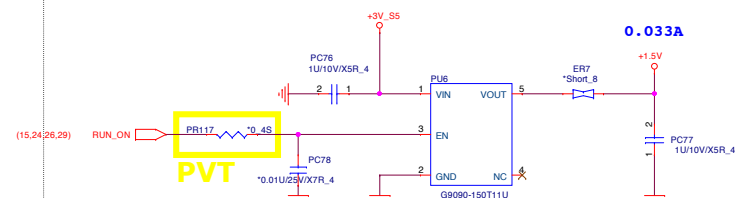
MODE	Resistor on Mode	Fsw	Discharge Mode
3	200Kohm	400KHz	Tracking discharge
2	100Kohm	300KHz	
1	68Kohm	300KHz	Non-tracking discharge
0	47Kohm	400KHz	

STATE	S3	S5	1.5VSUS	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	Off/High Z
S4/S5	0	0	Off	Off	Off

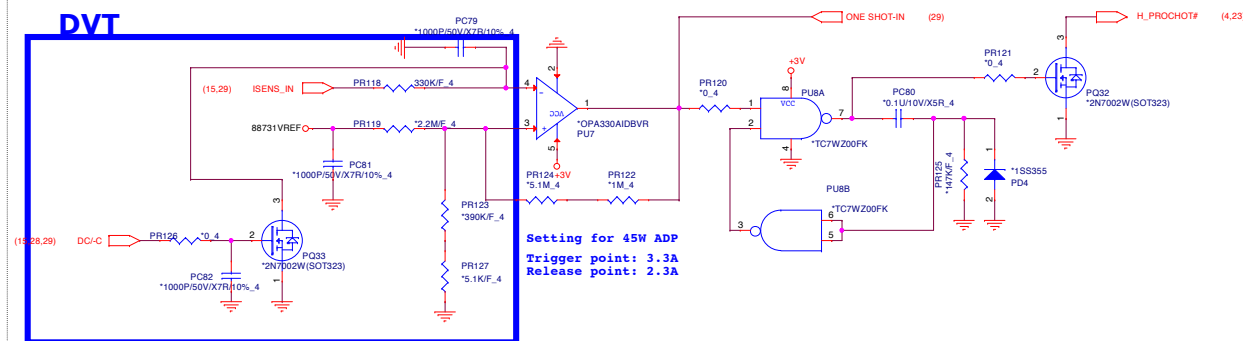
+1.05V



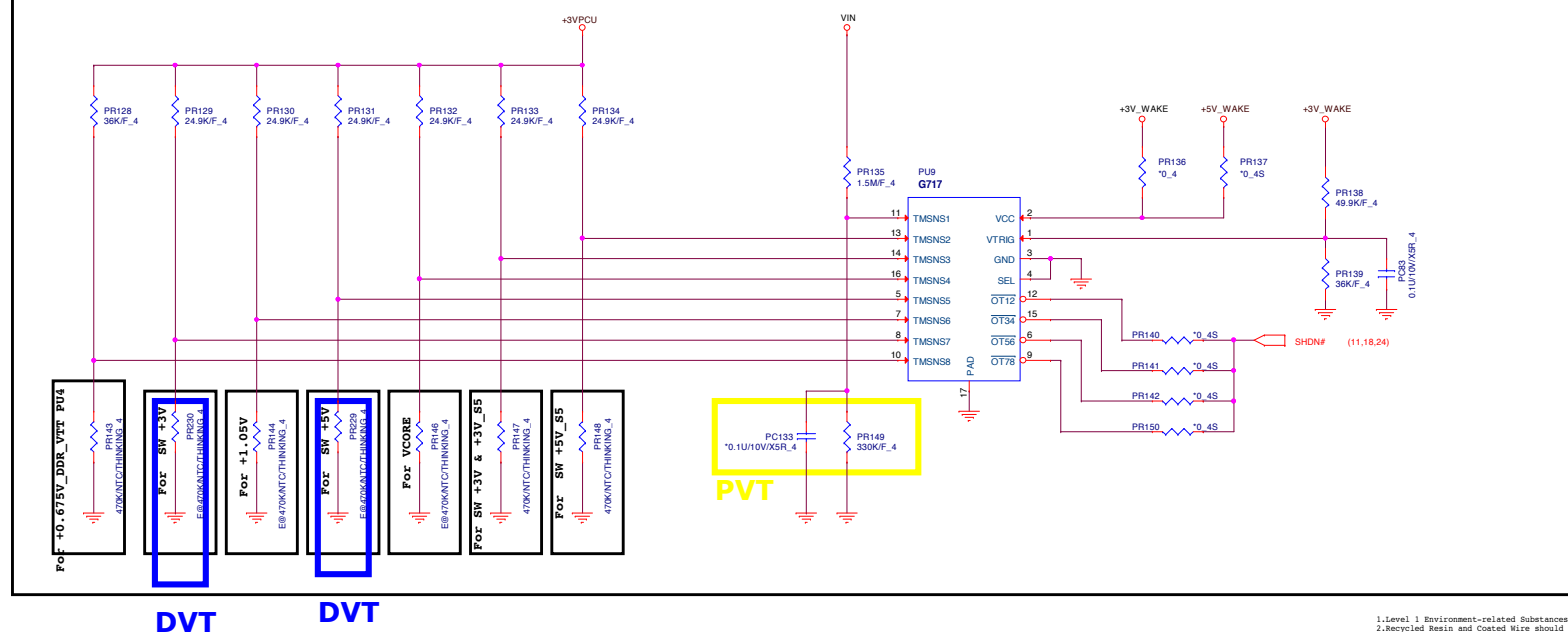
VCC1.5

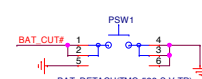
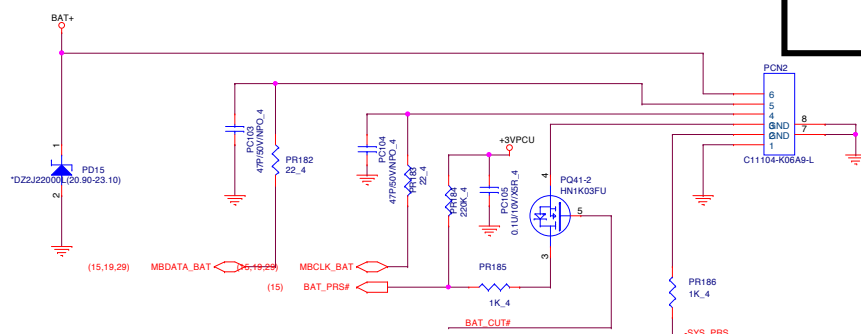
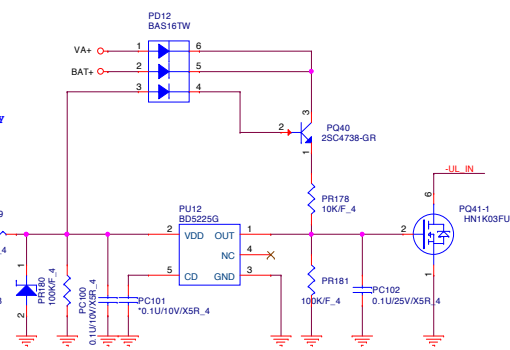
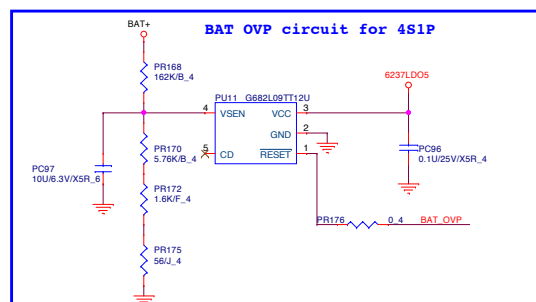
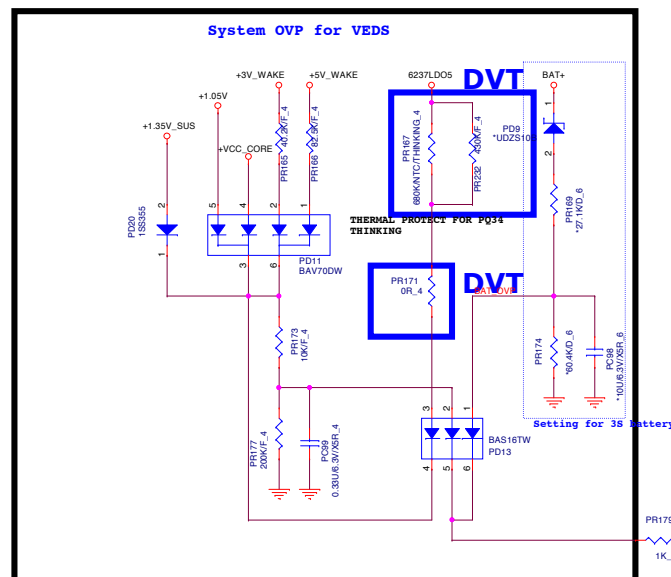
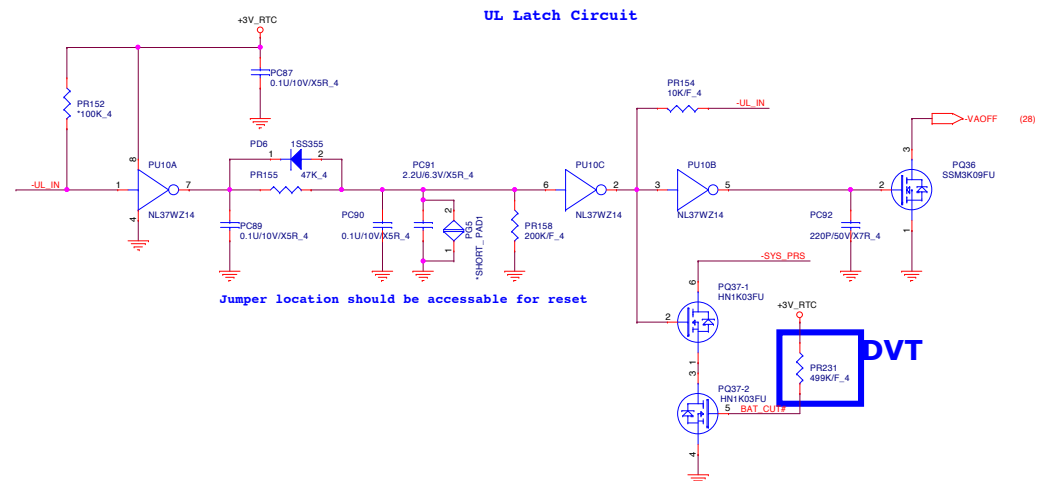


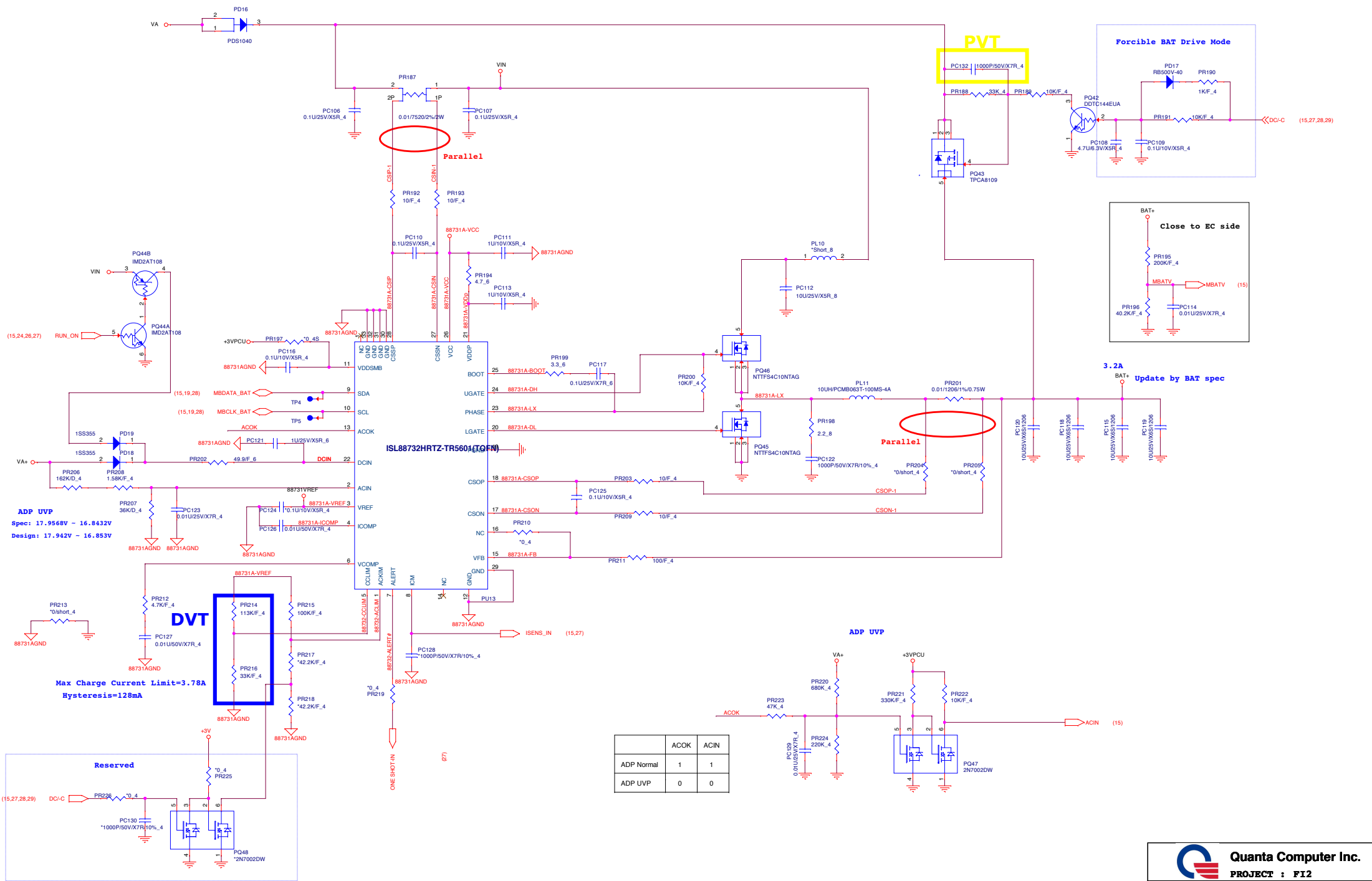
One-Shot 10ms PROCHOT# For ADP



Thermal Protection and Battery UVP for VEDS Abnormal







USB PORT Architecture	
PORT 0	USB3.0
PORT 1	USB3.0
PORT 2	Touch Screen
PORT 3	WiMax/BT
PORT 4	Sensor Hub
PORT 5	Camera
PORT 6	N/A
PORT 7	N/A

PCIE BUS	
PORT 1	N/A
PORT 2	N/A
PORT 3	WLAN Port
PORT 4	GLAN(RTL8111GS)
PORT 5	N/A
PORT 6	CARD READER

SATA BUS	
PORT 0	HDD
PORT 1	N/A
PORT 2	N/A
PORT 3	N/A

SM BUS	MBCLK/MBDATA	WRITE	READ	Function
ISL88732	0001 001X	0001 0010	0001 0011	Charger
LIS331DL	0011 101X	0011 1010	0011 1011	G Sensor

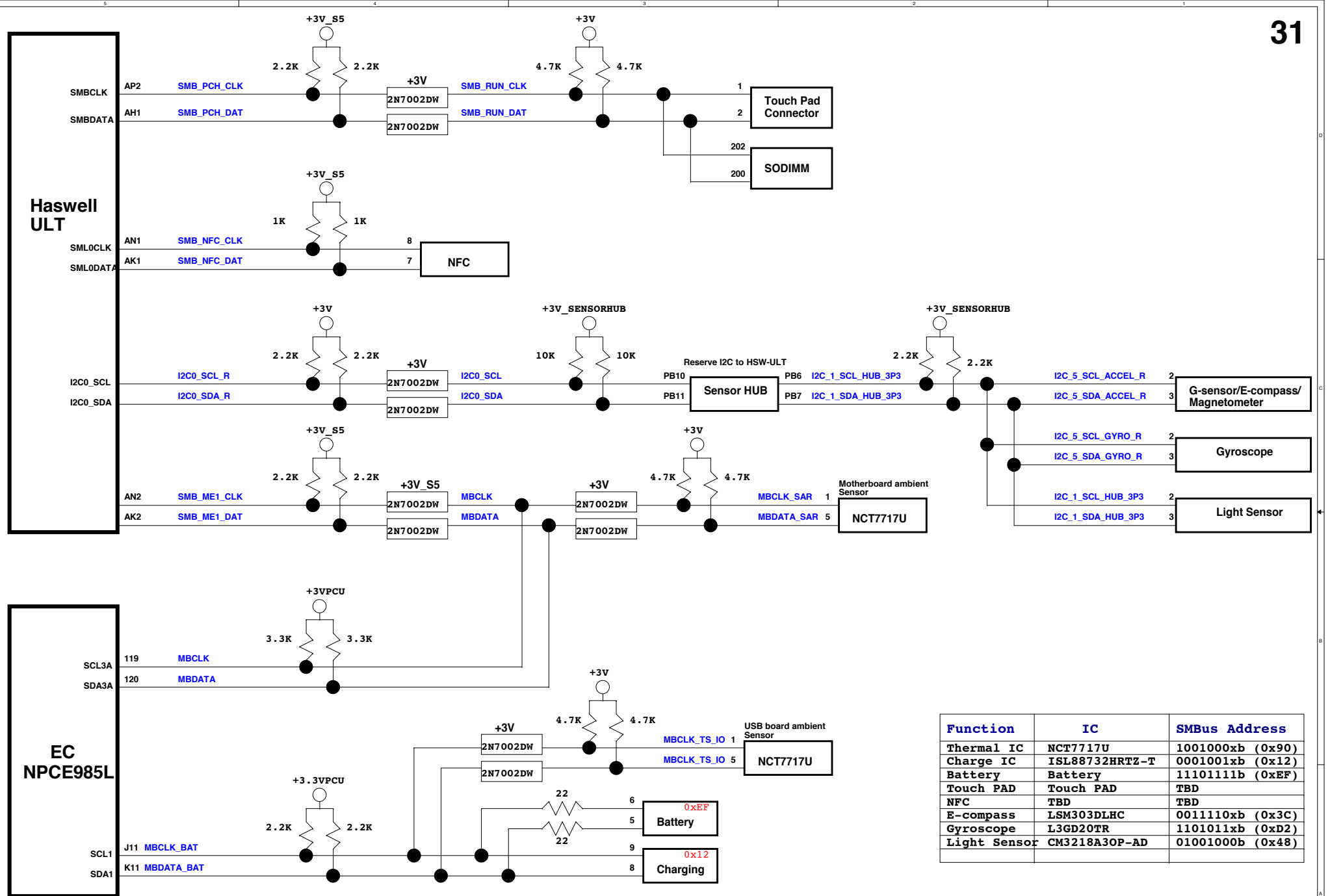
SM BUS	MBCLK_BAT/MBDATA_BAT	WRITE	READ	Function
T.B.D	0011 0010			Battery

SM BUS	SMB_PCH_CLK/SMB_PCH_DAT	WRITE	READ	Function
DIMM Module0	1010 000X	1010 0000	1010 0001	DDRIII
Synaptics	0010 110X	0010 1100	0010 1101	Click PAD

	R127 (Low) R128 (High)	R125 (Low) R126 (High)
Board ID1	Board ID0	
Mule FI1	0	0
HuronSHA1 FI2	0	1
HuronSHB1 FI3_UMA	1	0
HuronSHB1 FI3_DGPU	1	1

PCBA SKU	Discrete	UMA
R135(Pull High)	Stuff	No Stuff
R136(Pull Low)	No Stuff	Stuff

OS status	S0	S3	DS3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	DS3	S4 (Win8 off) RTC wake Enable WOLAN Enable	S4 (Win8 off) RTC wake Disable WOLAN Disable	S5 Charge Enable	S5 Charge Disable WoL Disable	S5 WoL Enable
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.675V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+0.85V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.35V_SUS	H	H	H	L	L	L	L	L
+3V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	L	H	L	H
+3V_WAKE	H	H	H	H	L	H	L	H
+5V_WAKE	H	H	H	H	L	H	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L
+3V_SUS	H	H	L	L	L	L	L	L



1.Level 1 Environment-related Substances should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

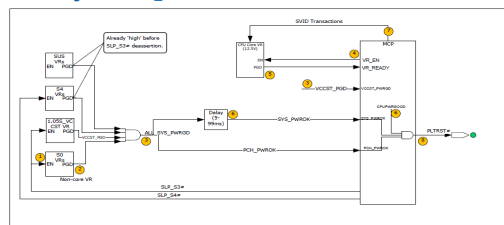
OS status	S0	S3	DS3	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)	(Soft OFF)
H/W status	S0	S3	DS3	S4 (Win8 off) RTC wake Enable WOLAN Enable	S4 (Win8 off) RTC wake Disable WOLAN Disable	S5 Charge Enable	S5 Charge Disable WoL Disable	S5 WoL Enable
RUN_ON	H	L	L	L	L	L	L	L
+3V	H	L	L	L	L	L	L	L
+5V	H	L	L	L	L	L	L	L
+0.675V_DDR_VTT	H	L	L	L	L	L	L	L
+1.05V	H	L	L	L	L	L	L	L
+0.85V	H	L	L	L	L	L	L	L
+1.5V	H	L	L	L	L	L	L	L
+VCC_CORE	H	L	L	L	L	L	L	L
SUS_ON	H	H	H	L	L	L	L	L
+1.35V_SUS	H	H	H	L	L	L	L	L
+3V_SUS	H	H	H	L	L	L	L	L
S5_ON	H	H	L	H	L	L	L	H
+5V_S5	H	H	L	H	L	L	L	H
+3V_S5	H	H	L	H	L	L	L	H
EC_WAKE_ON	H	H	H	H	L	H	L	H
+3V_WAKE	H	H	H	H	L	H	L	H
+5V_WAKE	H	H	H	H	L	H	L	H
DEEP_EC_EN	H	H	H	H	L	L	L	L
+3V_S5_DSW	H	H	H	H	L	L	L	L
+3V_SUS	H	H	L	L	L	L	L	L



Quanta Computer Inc.

PROJECT : FI2

Size	Document Number	Rev 1A
Power Table		
Date:	Wednesday, August 14, 2013	Sheet 32 of 33



Timing diagram for the 'load code' sequence. The diagram shows the relationship between several signals: AC10, *10PC1, BC_LOAD_OB, S1_OB, *10_READY, *10_S1, J10G2, *10_READY, and *10_S1. The signals are represented by horizontal lines with vertical steps indicating state changes. A label 'BC load code finish' points to a specific event in the BC_LOAD_OB signal.

