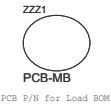


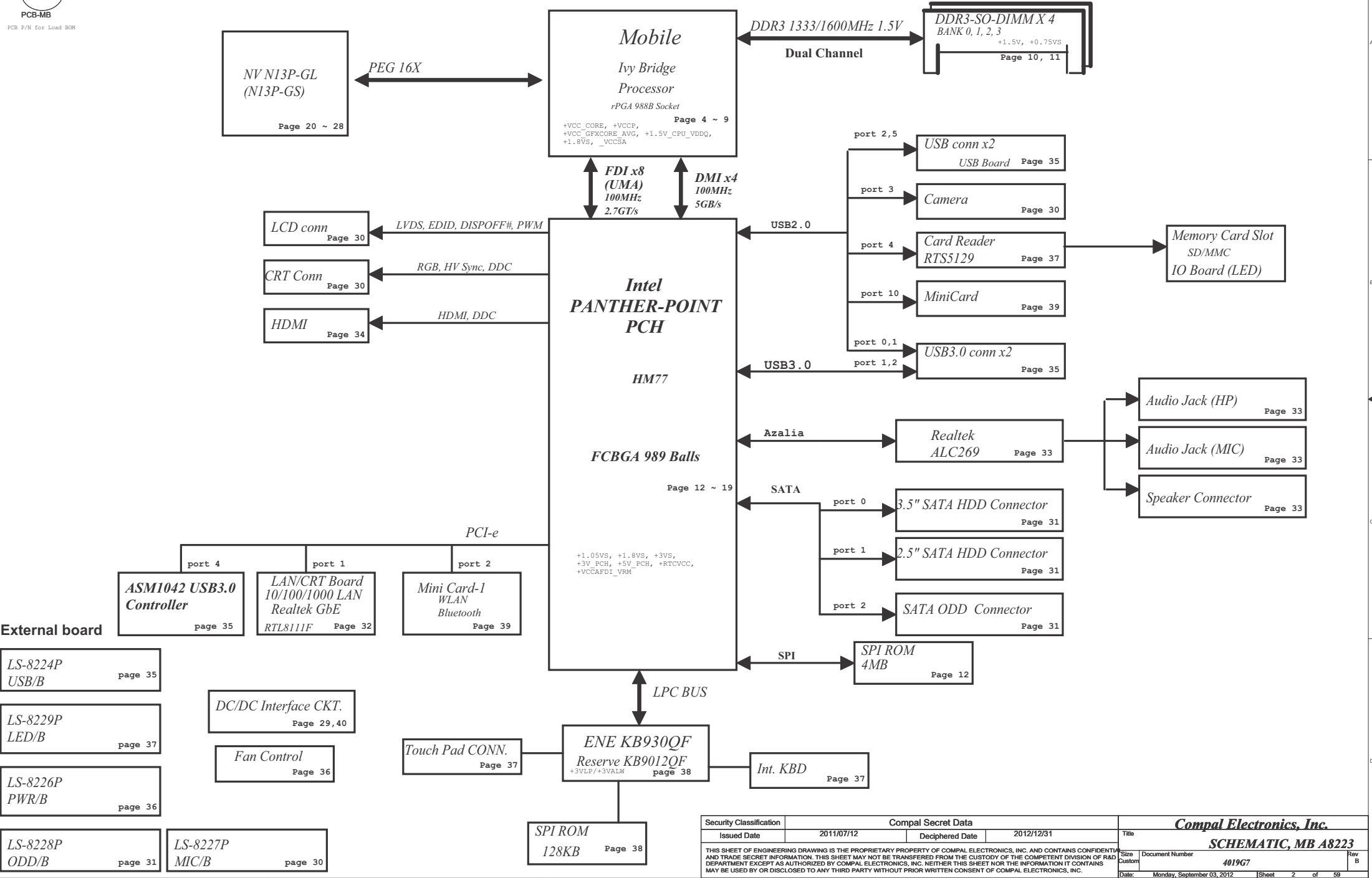
Compal Confidential

QCL90 MB Schematic Document

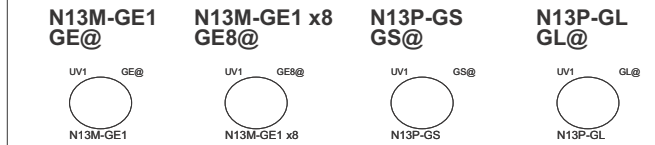
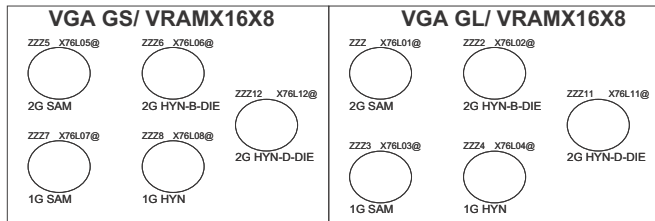
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				4019G7	B
Date: Monday, September 03, 2012		Sheet 1 of 59			



QCL90



X76@:

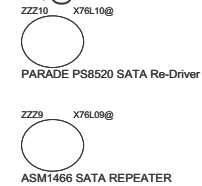


GE@: N13M-GE1 or N13P-GL
GS@: N13P-GS
DIS@: VGA componet
9012@: EC(ENE 9012 chip)
930@: EC(FNF 930 chip)

USB30@: USB3.0 by ASMEDIA
IU3@: USB3.0 by PCH

AI@: AI Charger
NAI@: Non AI Charger

SATA Re-Driver
X76@



SMBUS Control Table

	SOURCE	MINI1	BATT	PCH	EC	SODIMM	DGPU
EC_SMB_CK1 EC_SMB_DAI	KB930	X	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DAI2	KB930	X	X	V	X	X	V
PCH_SMBCLK PCH_SMBDATA	PCH	V	X	X	X	V	X
PCH_SMLCLK PCH_SMLDATA	PCH	X	X	X	V	X	V

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	CLK_SD_48M
	CLKOUT_PCIE1	MINI CARD WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	ASMEDIA USB3.0	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		



CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	None
PCI3	LPC Debug Port
PCI4	None

Voltage Rails

Power Plane	Description	S1	S3	Deep S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+3VLP	3.3V power rail for 510N power management	ON	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+LAN_IO	3.3V power rail for ethernet	ON	ON	OFF	OFF
+3VS_WLAN	3.3V power rail for WLAN/BT Combo	ON	OFF	OFF	OFF
+3V_PCH	3.3V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+3VS	3.3V power rail for DDR SPI,PCH,HDD,Audio,Card Reader	ON	OFF	OFF	OFF
+3VSG	3.3V power rail for VGA	ON	OFF	OFF	OFF
+LCDVDD	3.3V power rail for LCD	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	AC/ON; DC/OFF
+5V_PCH	5V power rail for PCH suspend well plane	ON	ON	OFF	OFF
+5VS	5V power rail for HDD,AUDIO,FAN,Touch PAD	ON	OFF	OFF	OFF
+5VS_ODD	5V power rail for SATA ODD	ON	OFF	OFF	OFF
+1.8VS	1.8V power rail for CPU,PCH	ON	OFF	OFF	OFF
+1.05VS	1.05V power rail for PCH	ON	OFF	OFF	OFF
+VCCP	1.05V power rail for CPU VCCIO,PCH	ON	OFF	OFF	OFF
+1.05VSG	1.05V power rail for N13P	ON	OFF	OFF	OFF
+1.5V	1.5V power rail for DDR3 system memory	ON	ON	ON	OFF
+1.5V_CPU_VDDQ	1.5V power rail CPU VDDQ	ON	OFF	OFF	OFF
+1.5VSG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+1.5VS	1.5V power rail for PCH,WLAN/BT combo	ON	OFF	OFF	OFF
+0.75VS	0.75V power rail for DDR VREF	ON	OFF	OFF	OFF
+VCCSA	VCCSA for CPU system agent	ON	OFF	OFF	OFF
+VCC_CORE	CORE Voltage for CPU	ON	OFF	OFF	OFF
+VCC_GFXCORE_AXG	1.5V power rail for N13P,VRAM	ON	OFF	OFF	OFF
+VGA_CORE	CORE Voltage for N13P Graphics ON OFF OFF	ON	OFF	OFF	OFF

SATA	DESTINATION
SATA0	3.5" HDD
SATA1	2.5" HDD
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

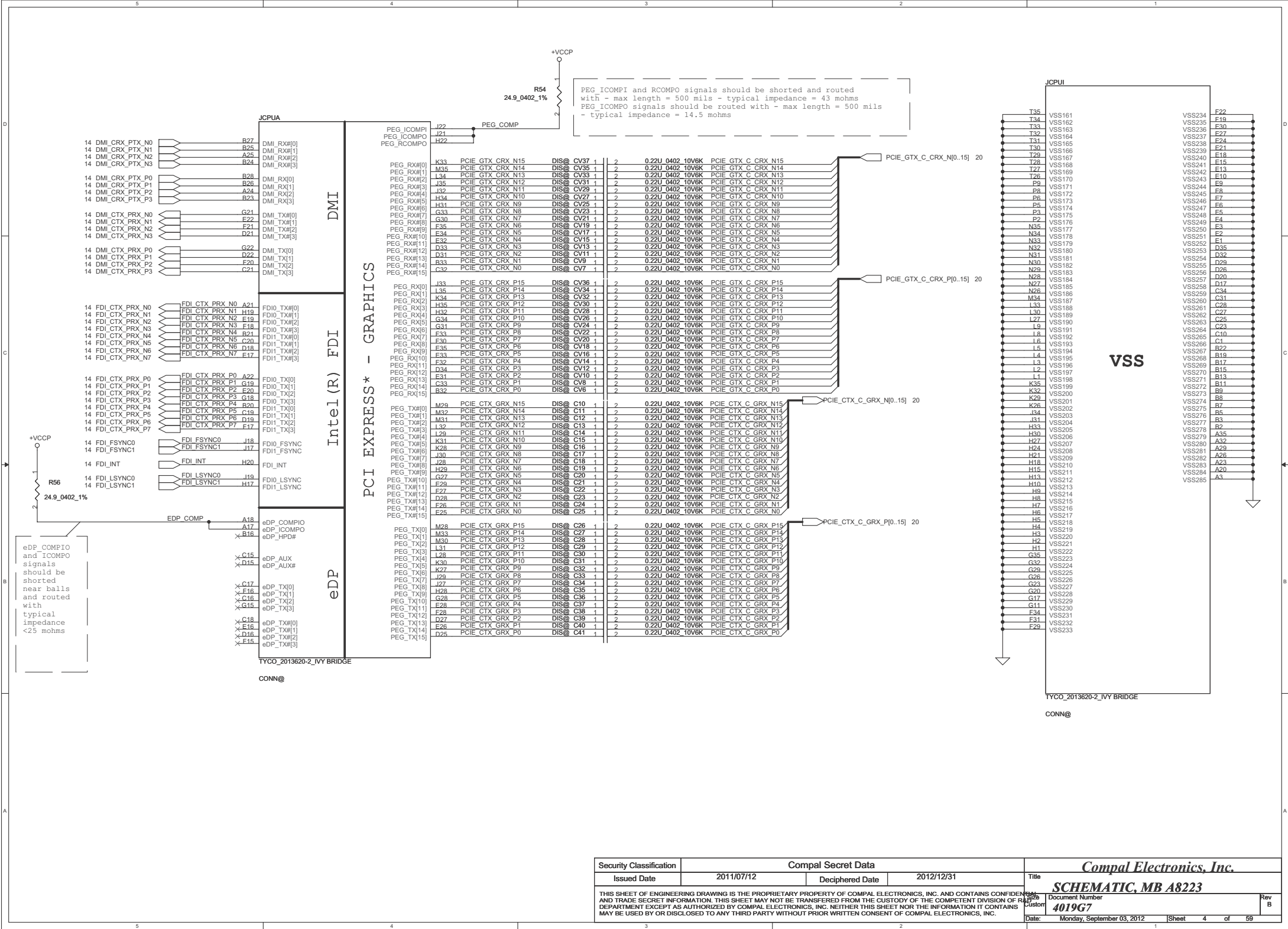
PCH	USB3 PORT	DESTINATION
	1	USB2.0+3.0
	2	USB2.0+3.0
	3	None
	4	None

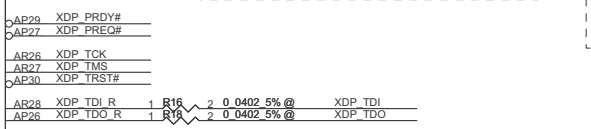
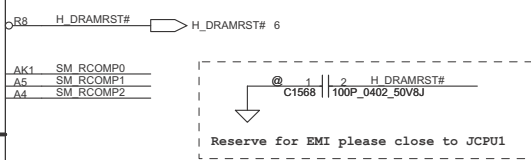
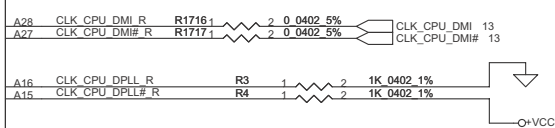
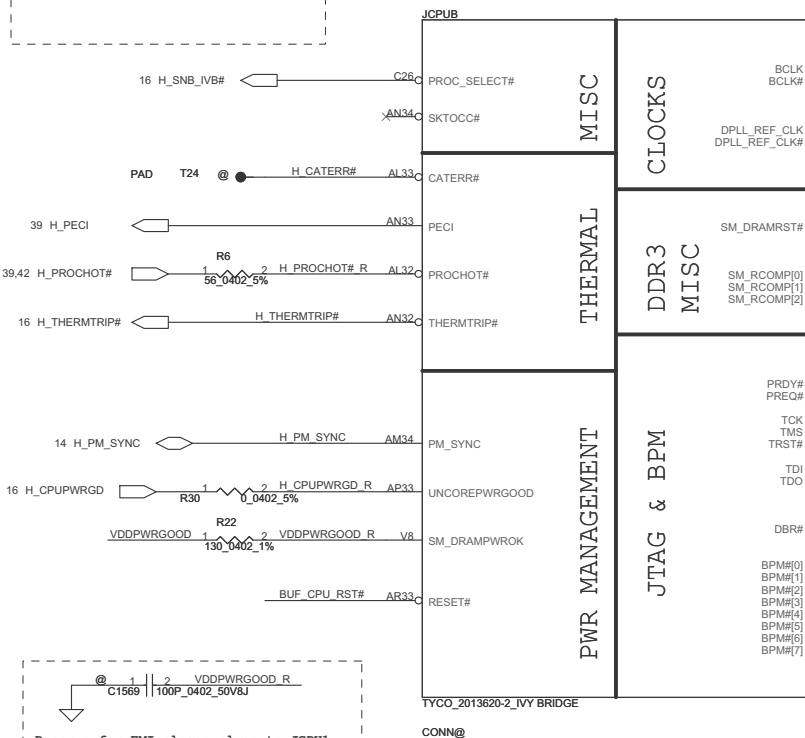
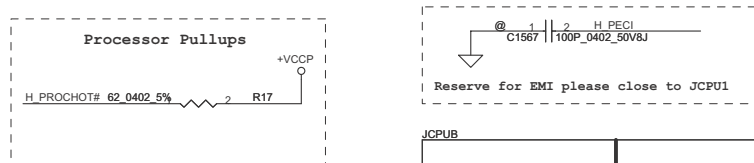
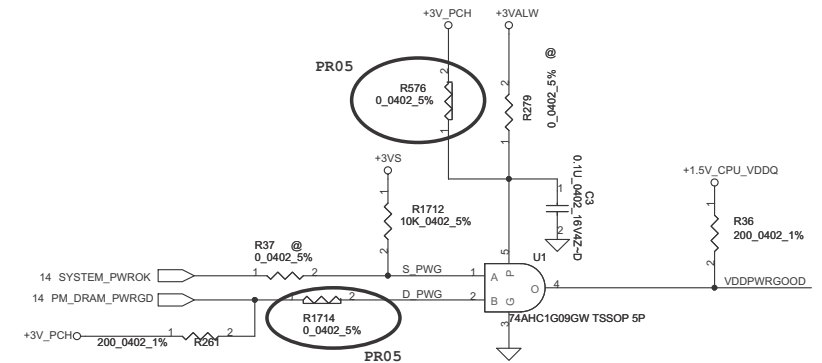
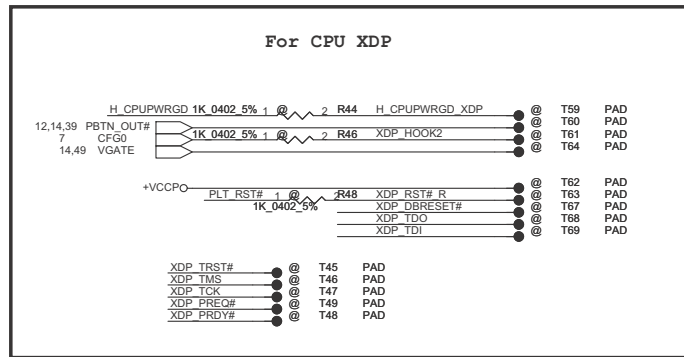
PCH	USB2 PORT	DESTINATION
	0	USB2.0+3.0
	1	USB2.0+3.0
	2	USB2
	3	CAMERA
	4	Card Reader
	5	USB2
	6	None
	7	None
	8	None
	9	None
	10	JMINI1 (WLAN) Bluetooth
	11	None
	12	None
	13	None

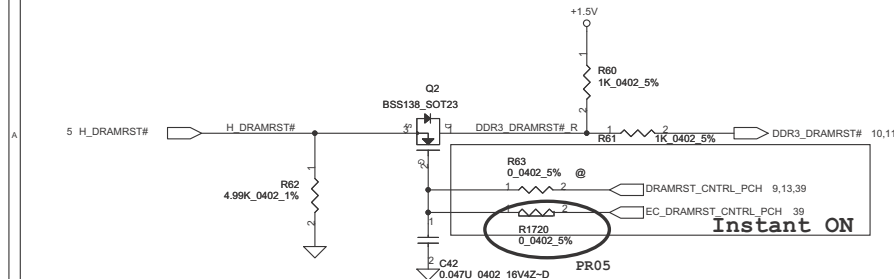
PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD WLAN
Lane 3	None
Lane 4	ASMEDIA USB3.0
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

QCL90 * 16 (LA8223P)
Board ID Table for AD channel

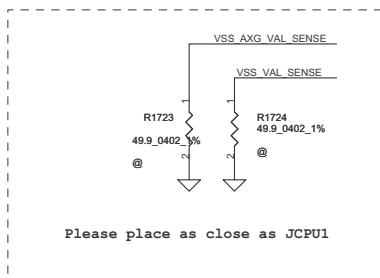
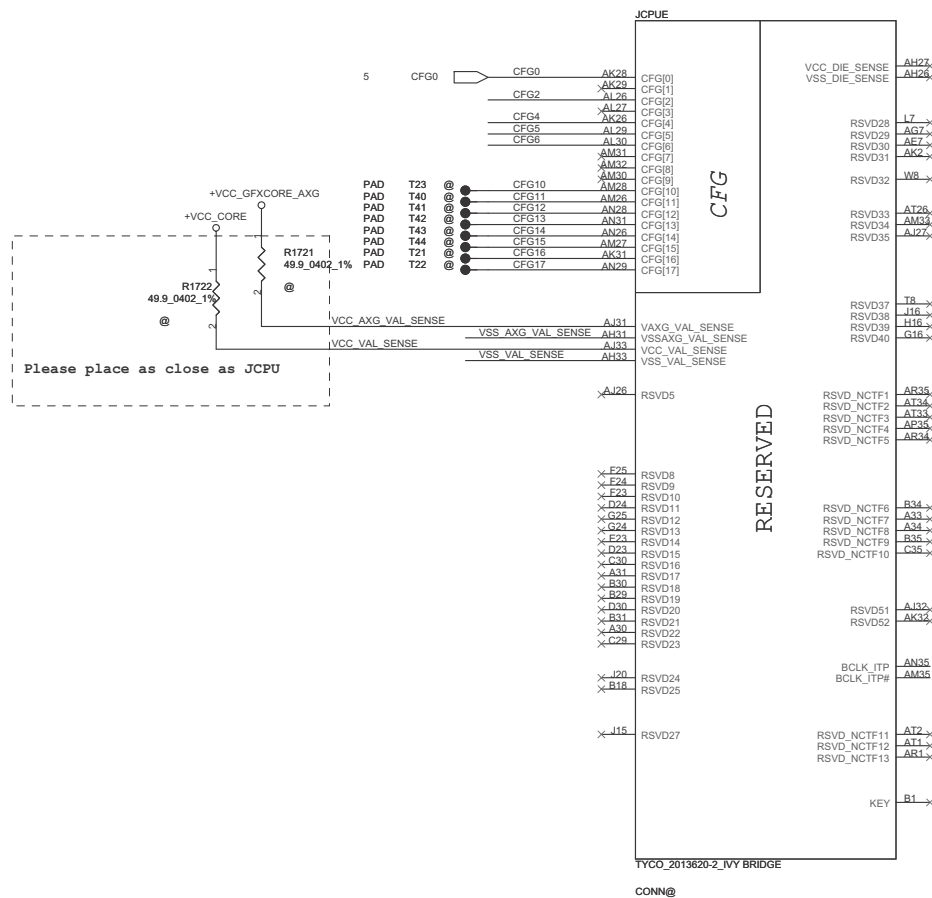
Vcc	3.3V +/- 5%	typ: 0.958~1.359V		
Ra / Rc	100K +/- 5%			
Board ID	Rb / Rd	VAD_BID min	VAD_BID typ	VAD_BID max
*	56K +/- 5%	0.958 V	1.185 V	1.359 V



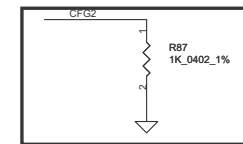




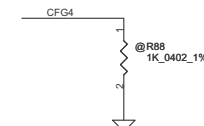
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Date:	Monday, September 03, 2012	Sheet	6	of 60



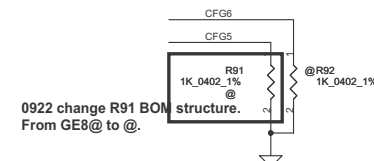
CFG Straps for Processor



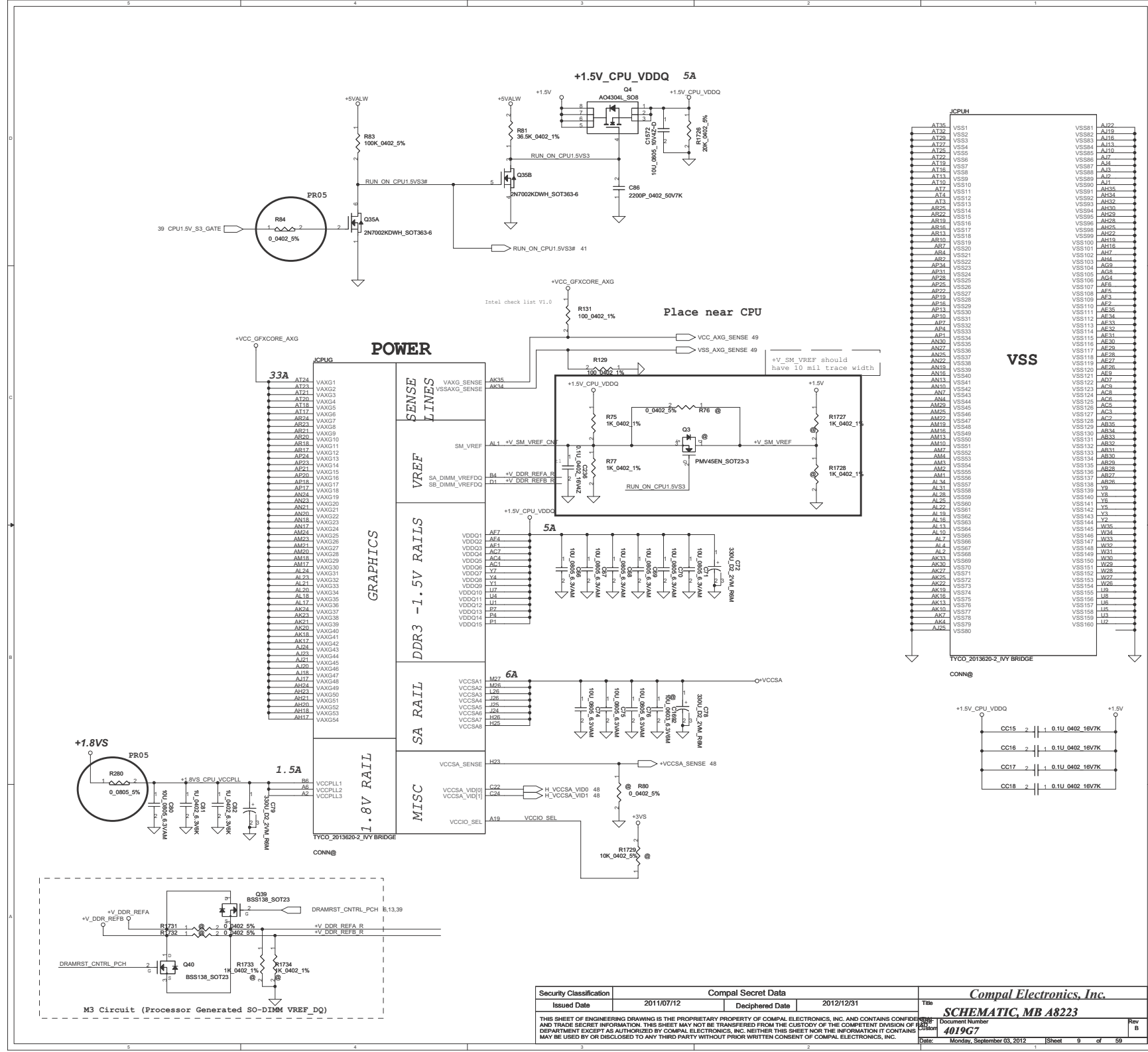
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

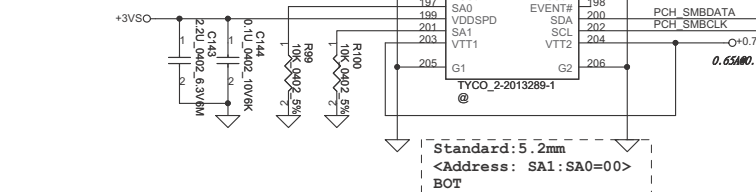


Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

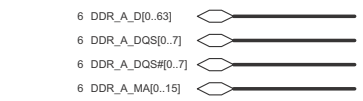


PCIE Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

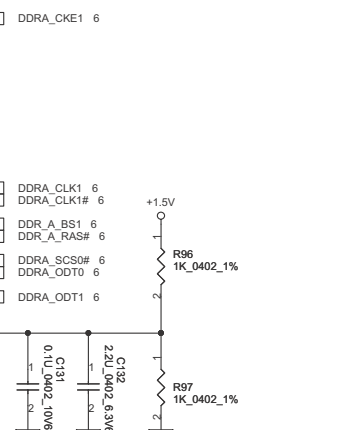
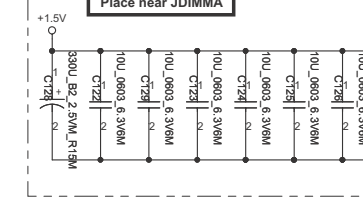




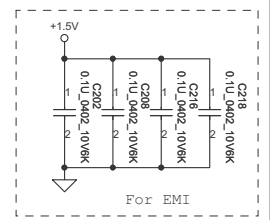
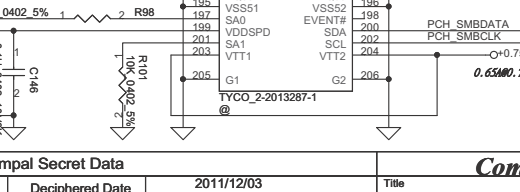
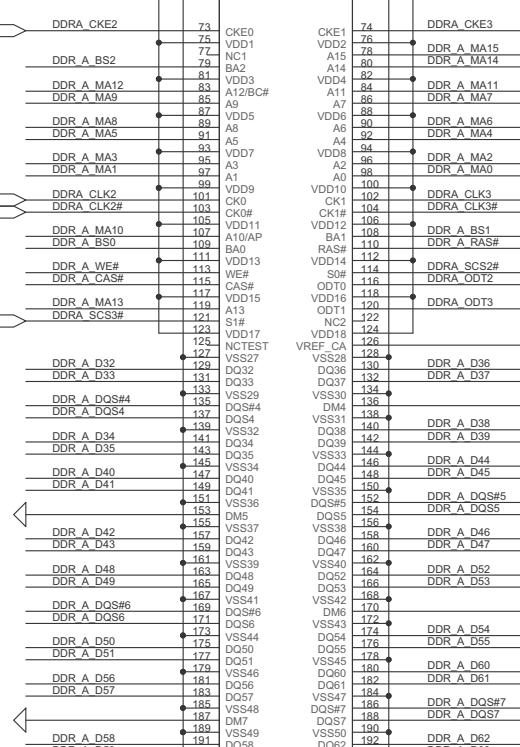
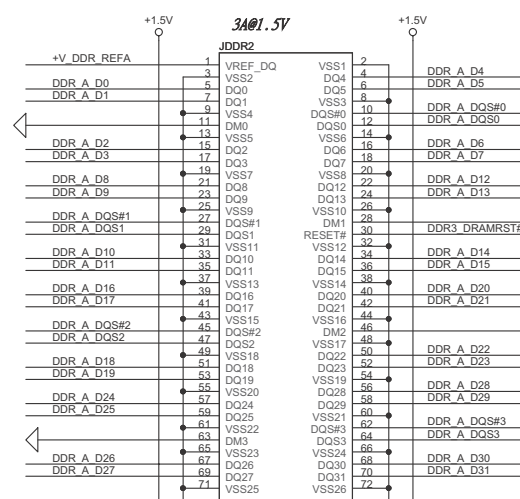
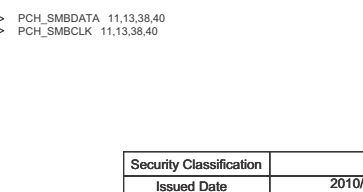
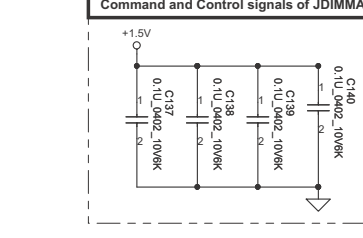
Support SO DIMM X 4
Support 1066/1333MHz



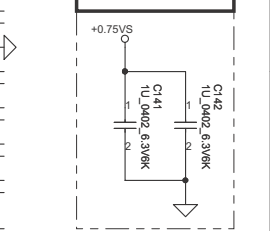
Layout Note:
Please refer to DIMM



Layout Note: Place these 4 Caps near

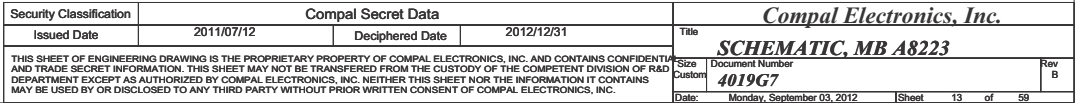


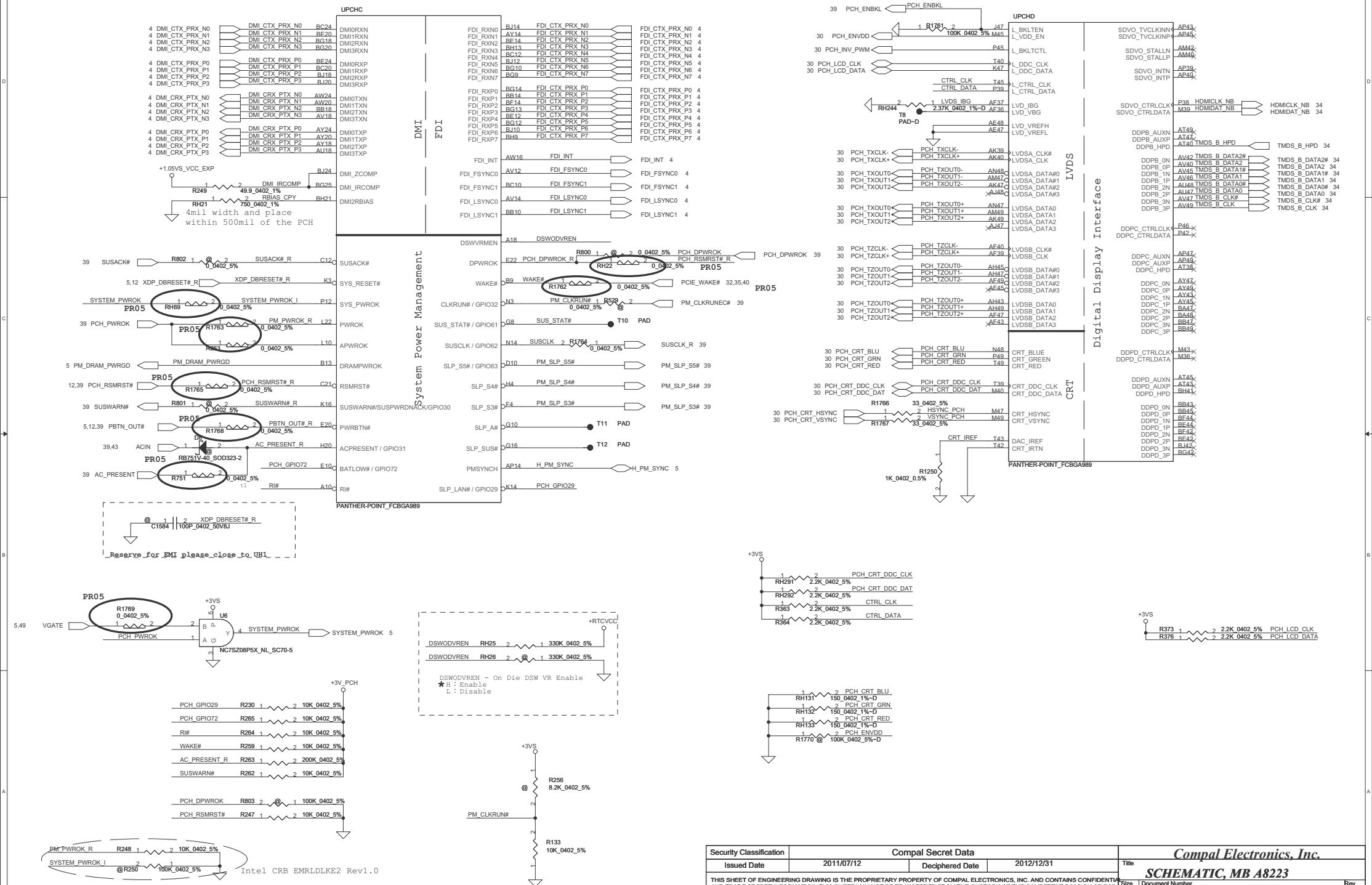
Layout Note:
Place near
JDIMMA2.203,204



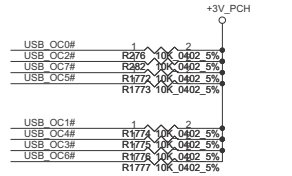
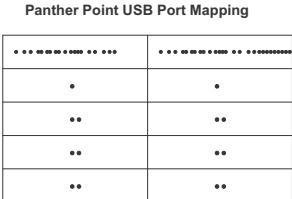
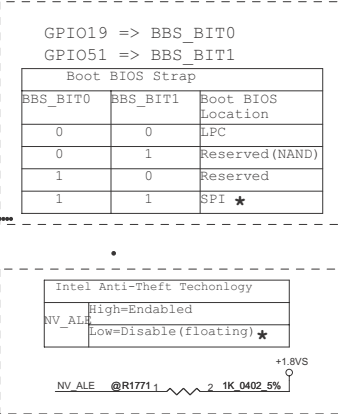
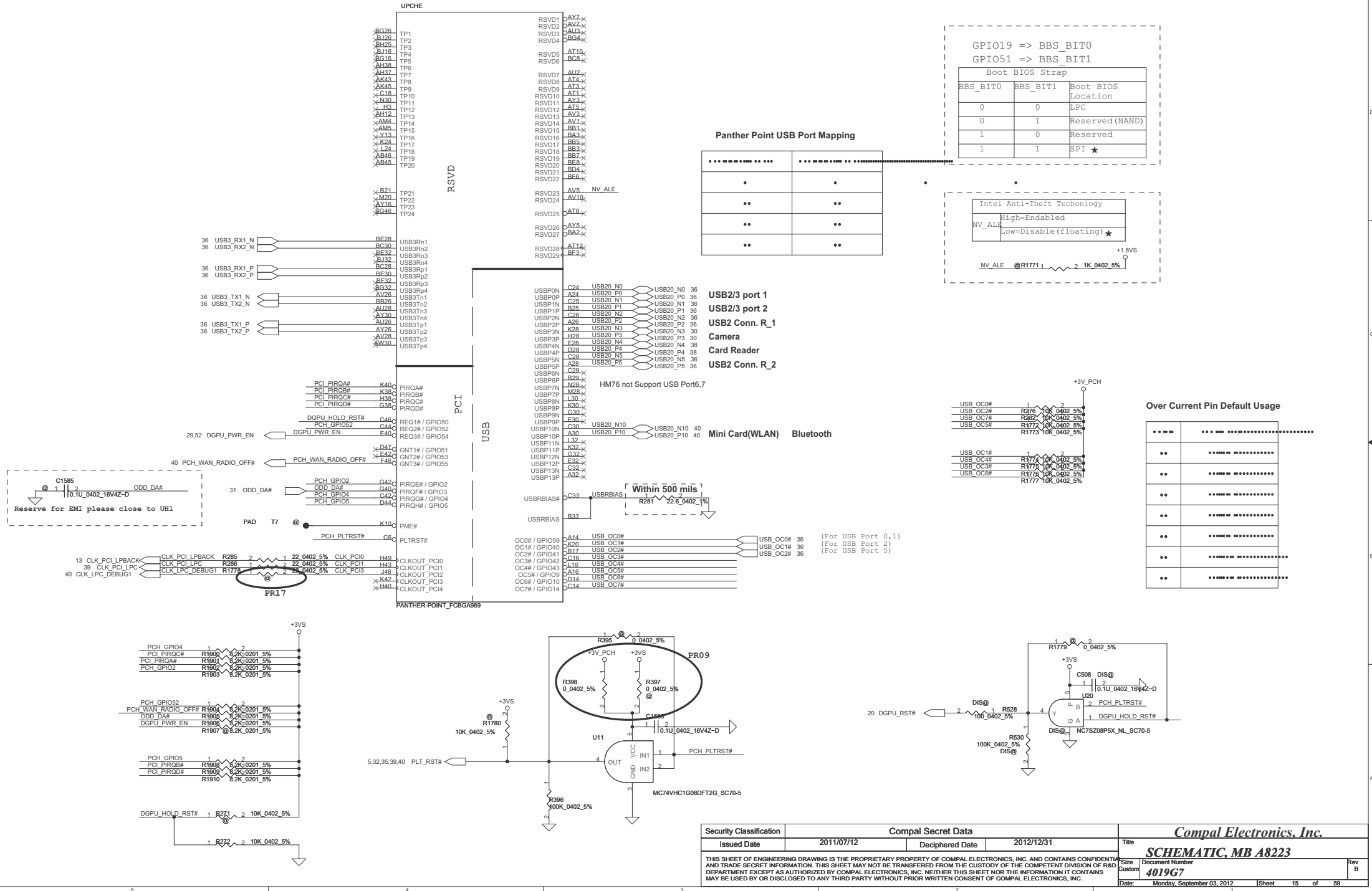
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Reverse: 4mm
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						Doc Number	Rev B
						4019G7	
Date:		Monday	September 03, 2012	Sheet	12	of 50	



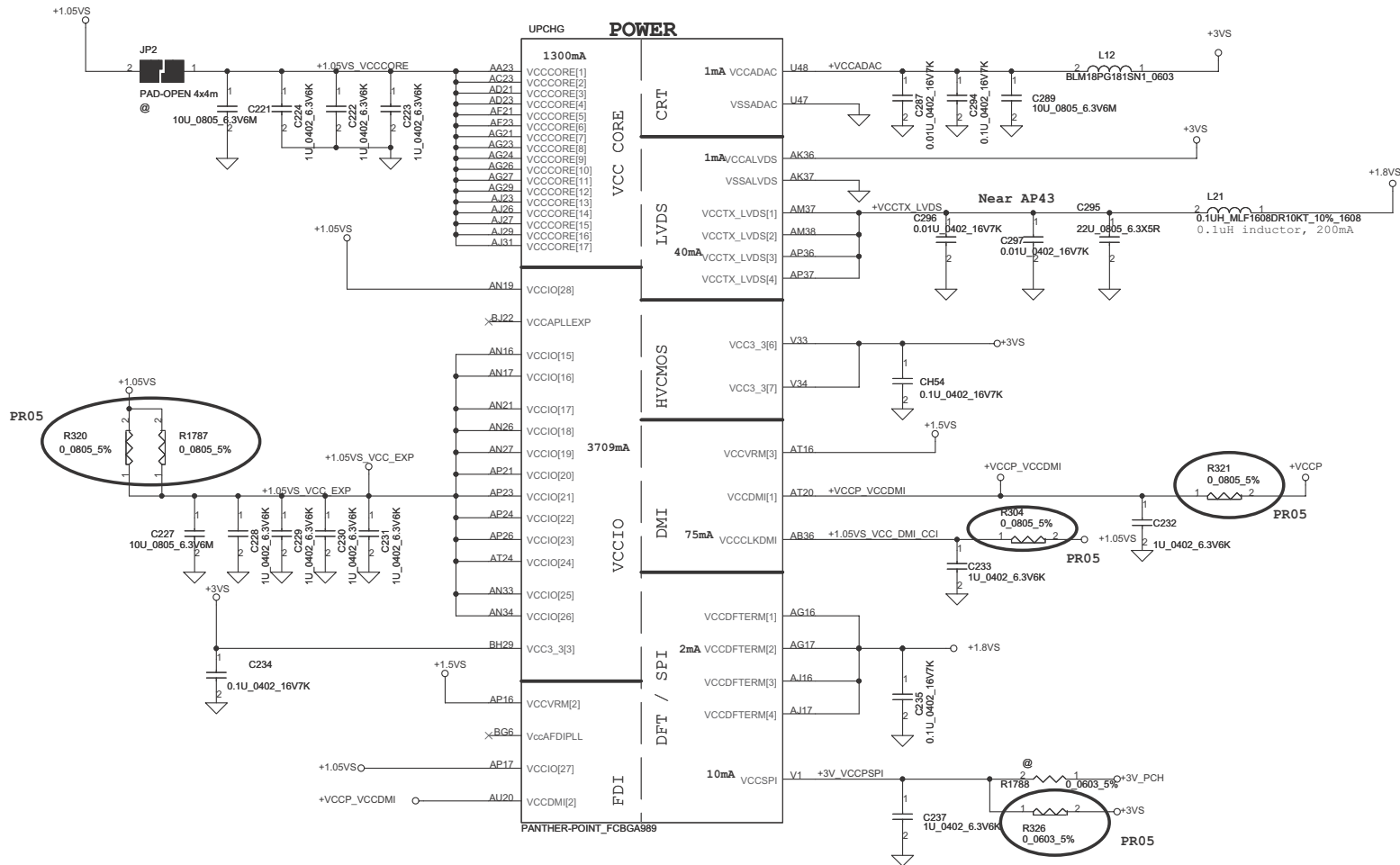


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				Date:	Monday, September 03, 2012
				Sheet	14 of 59

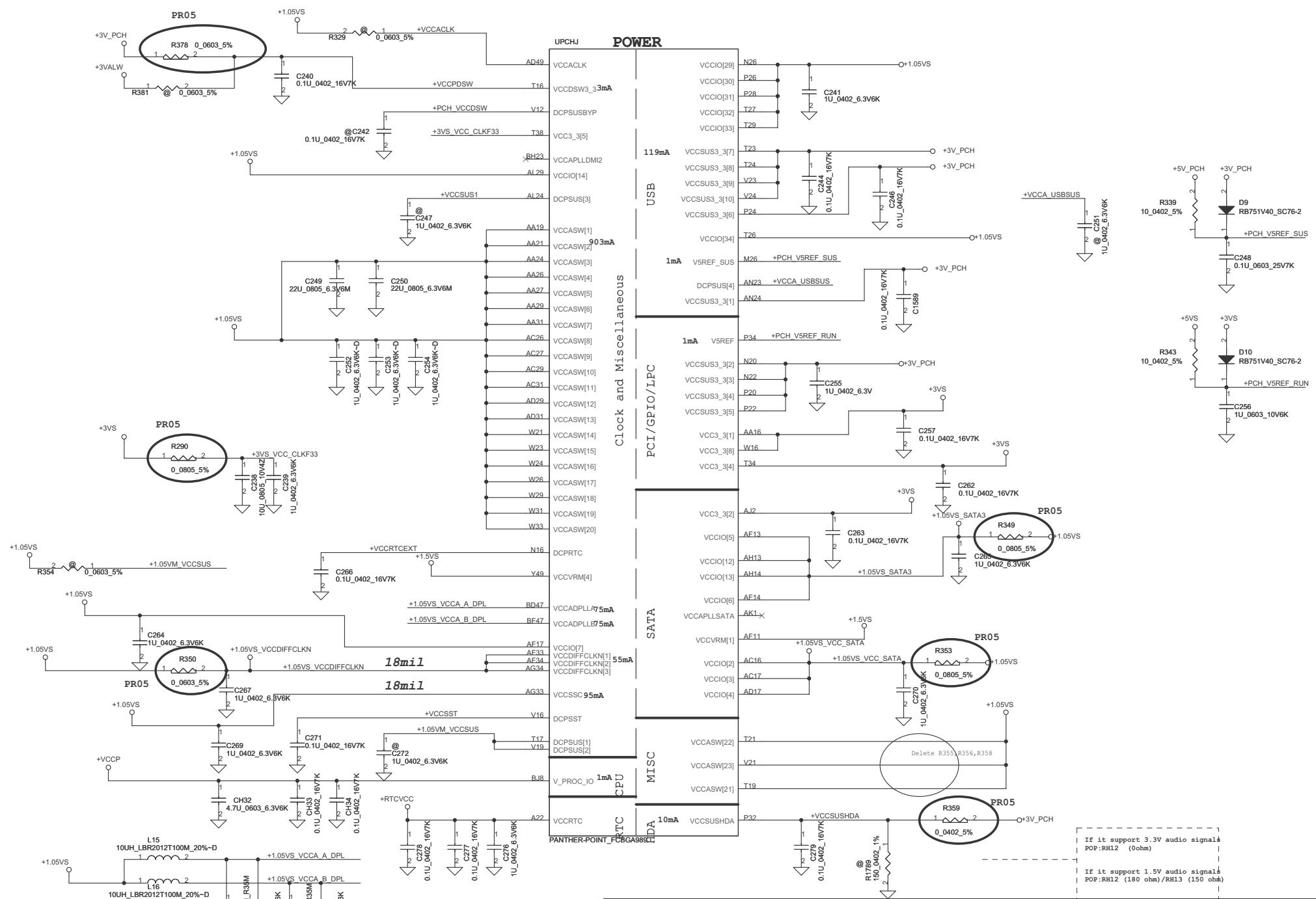


Mini Card(WLAN) Bluetooth

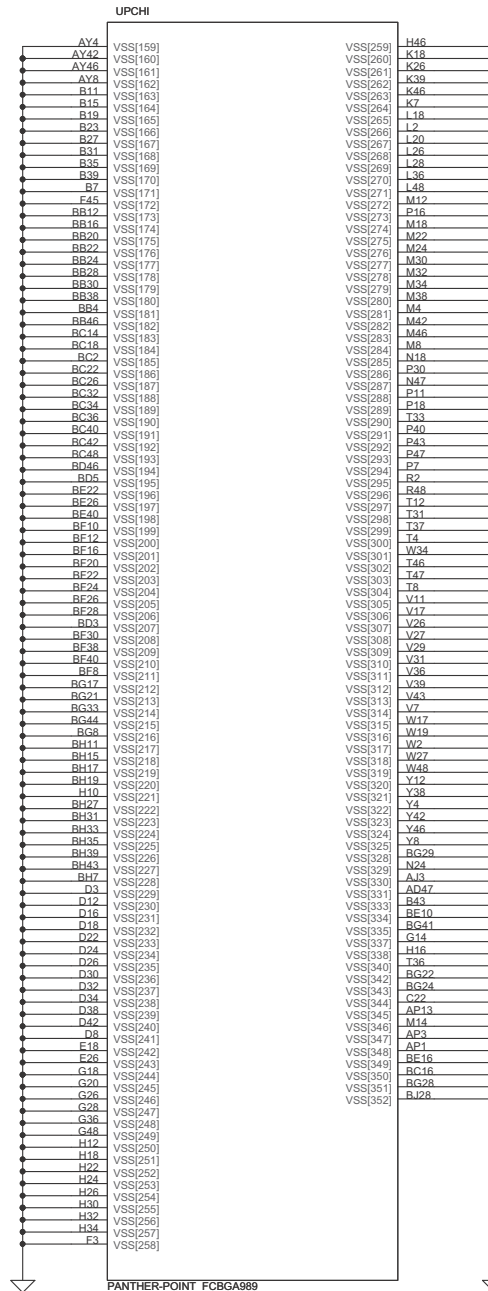
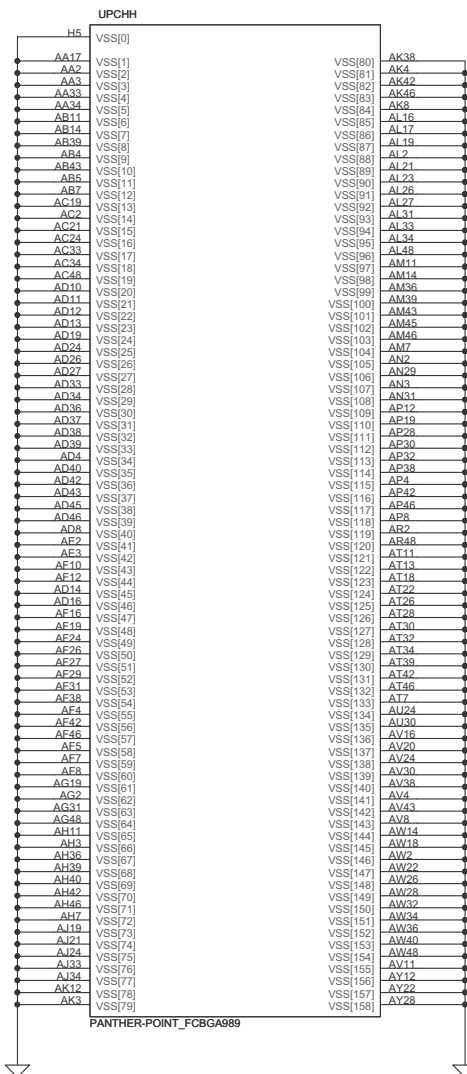
(For USB Port 0,1)
(For USB Port 2)
(For USB Port 5)

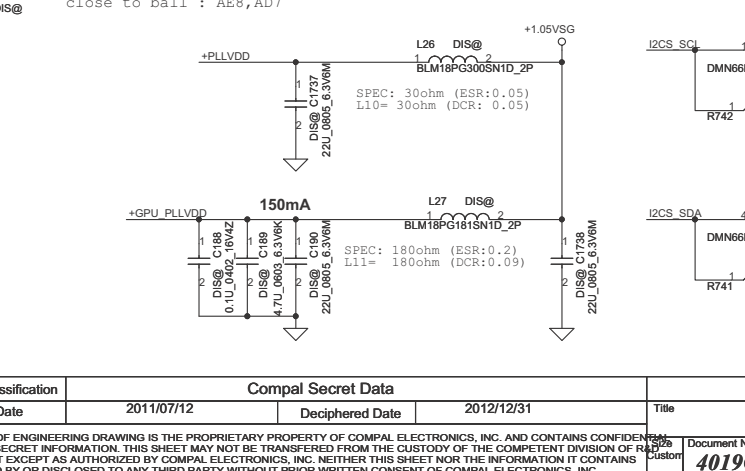
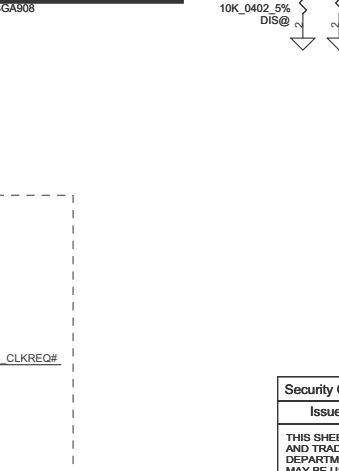
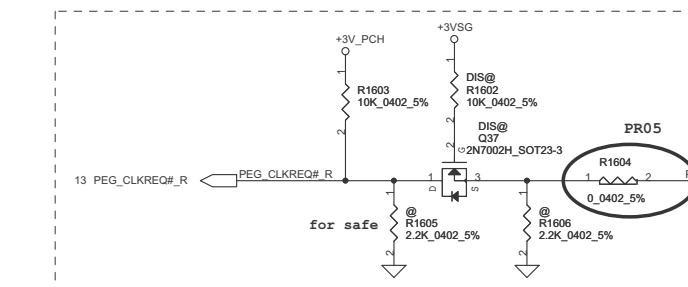
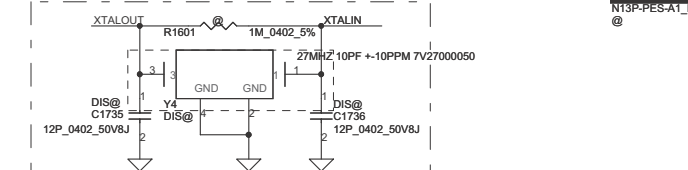
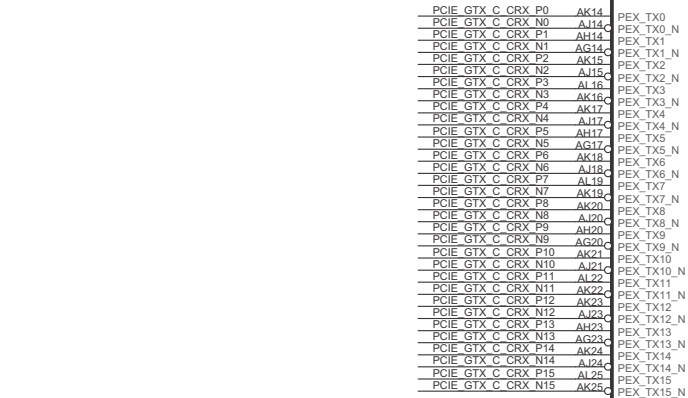


PCH Power Rail Table Refer to CPU EDS R1.5		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.001
VccADPLLA	1.05	0.075
VccADPLLB	1.05	0.075
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	3.709
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTerm	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.065
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.075
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04



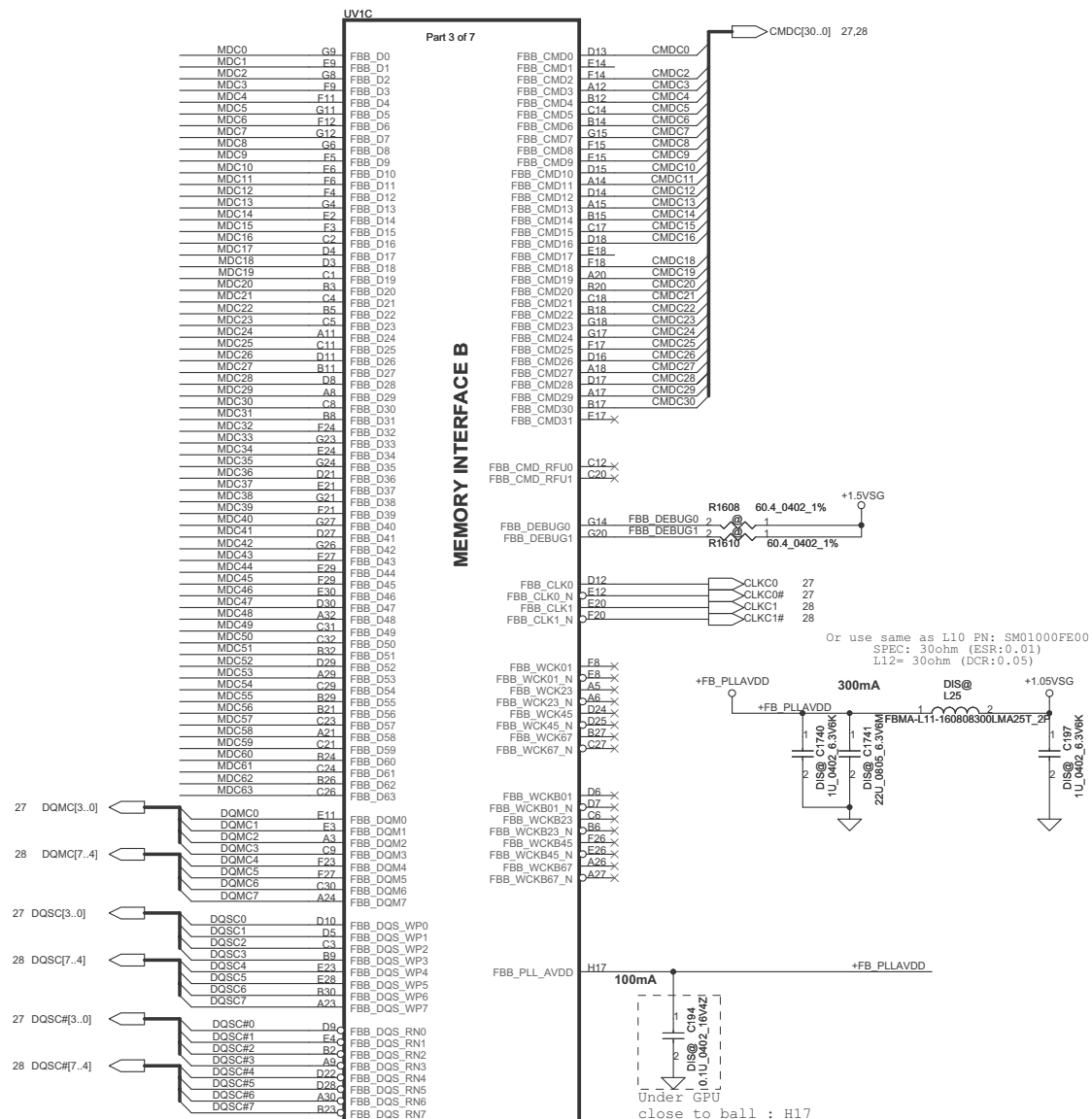
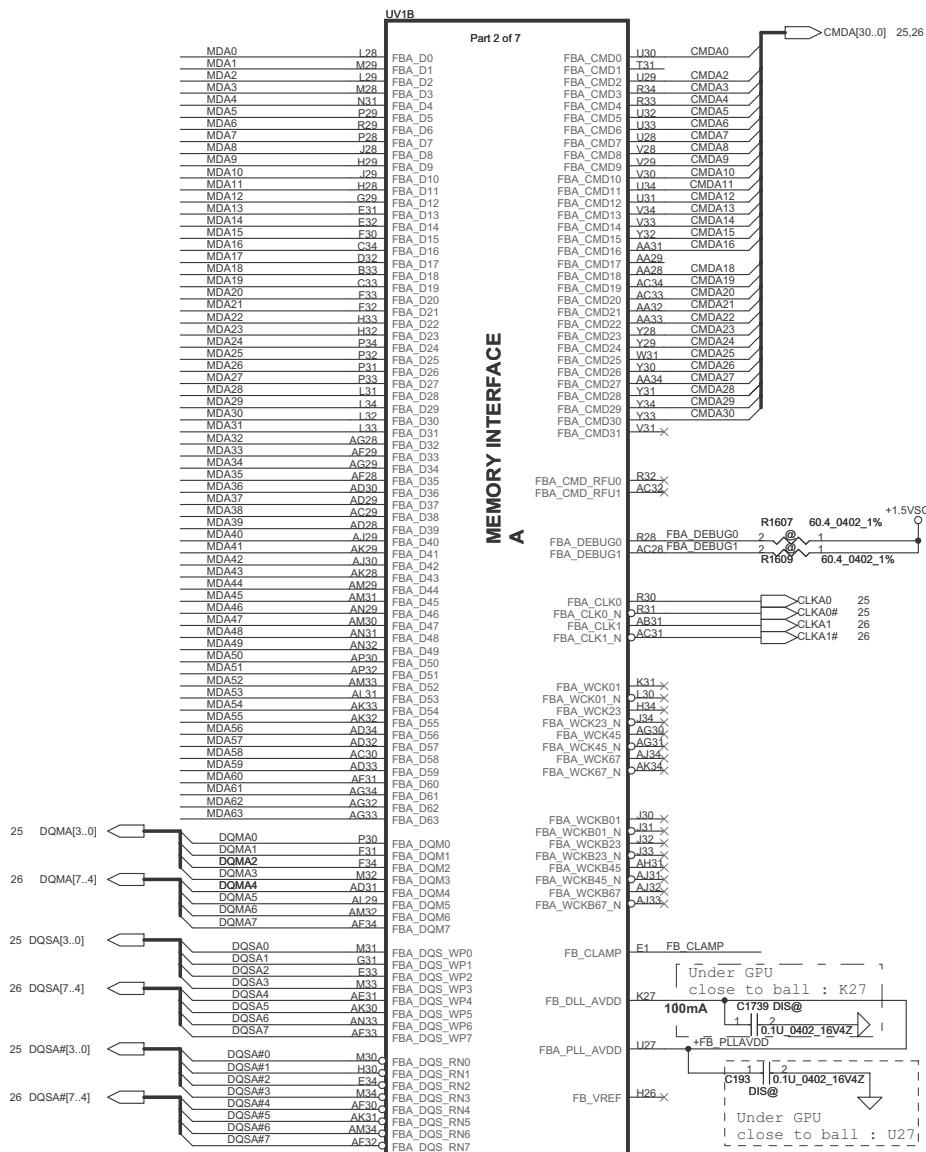
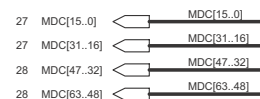
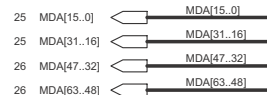
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Date:		Monday, September 03, 2012		Sheet		18		of 59	



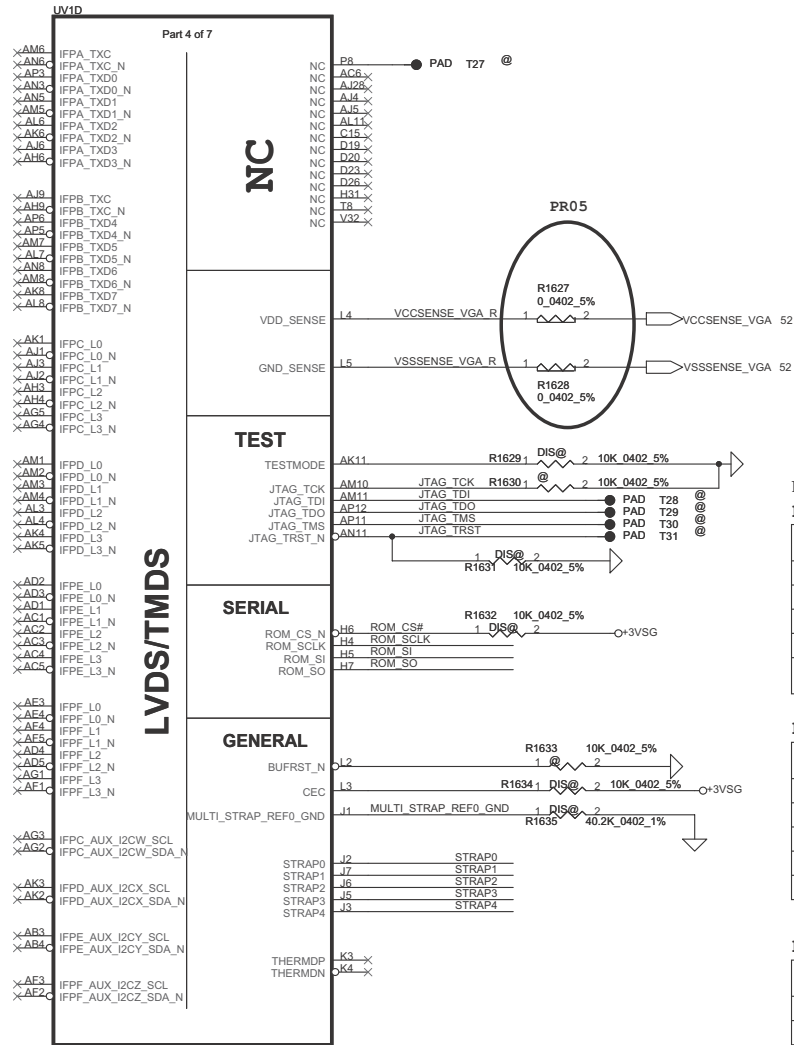


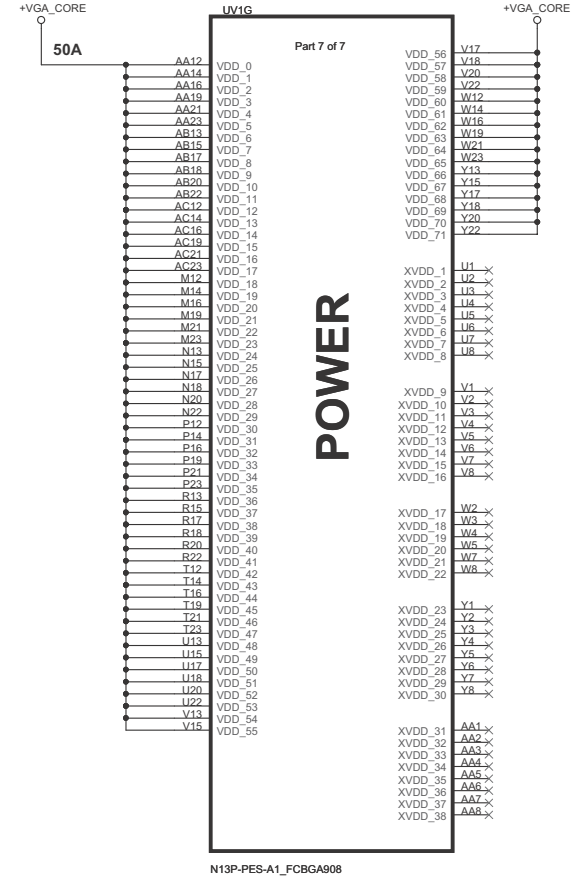
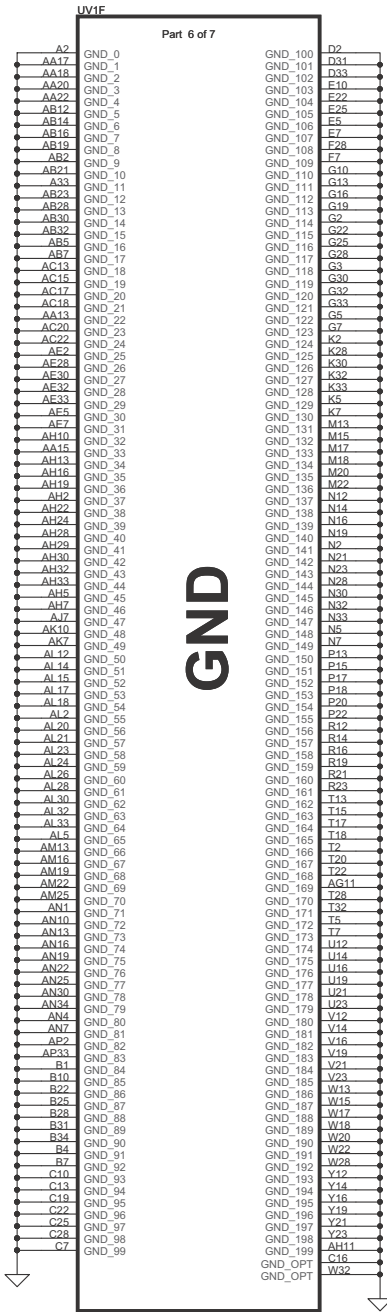
GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

VRAM Interface



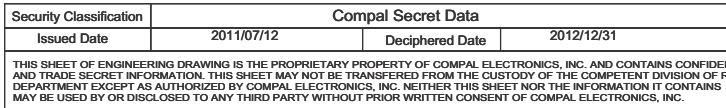
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					Doc Number		Rev B	
					Customer			
					Date:		Monday, September 03, 2012	
					Sheet 21 of 59			





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								m			
								Number			
								4019G7			
Date:								Monday, September 03, 2012		Sheet 24 of 59	

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)
AMD :SA00003PF10
(S IC D3 64M16/800 23EY2387MB-12 PG-TFBGA 96P 1.5V)

128Mx16 DDR3 *8==>2GB



The schematic shows a power supply section starting from a +1.5VSG input at the top left. This input passes through a series of components connected to ground:

- A diode labeled DS@ C1647.
- An inductor labeled IU_0402_3.VKR.
- A diode labeled DS@ C1648.
- An inductor labeled IU_0402_3.VKR.
- A diode labeled DS@ C1649.
- An inductor labeled IU_0402_3.VKR.
- A diode labeled DS@ C1650.
- An inductor labeled IU_0402_3.VKR.

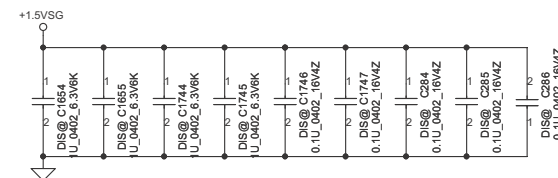
Following these components, there are four parallel branches, each consisting of a diode in series with an inductor:

- Branch 1: Diode DS@ C1651 in series with inductor IU_0402_16VKZ.
- Branch 2: Diode CZ73 in series with inductor IU_0402_16VKZ.
- Branch 3: Diode CZ74 in series with inductor IU_0402_16VKZ.
- Branch 4: Diode CZ75 in series with inductor IU_0402_16VKZ.

Finally, there are two more parallel branches at the bottom:

- Branch 5: Diode DS@ C1652 in series with inductor IU_0402_16VKZ.
- Branch 6: Diode DS@ C1653 in series with inductor IU_0402_16VKZ.

All components are connected to a common ground plane at the bottom of the schematic.

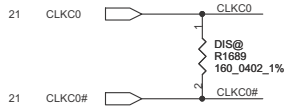
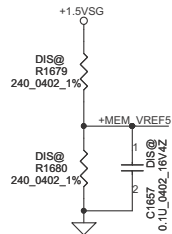
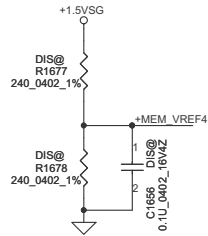
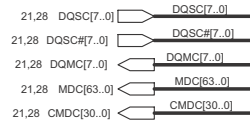


LOW HIGH

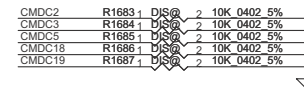
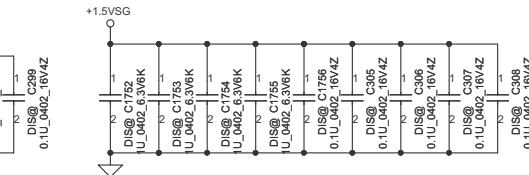
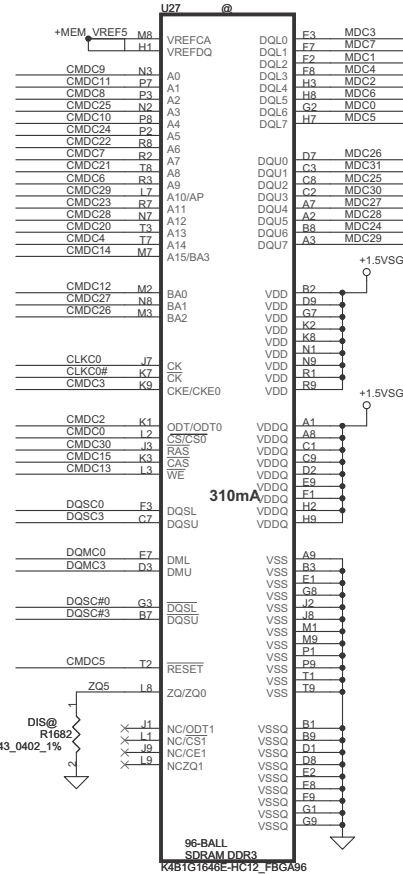
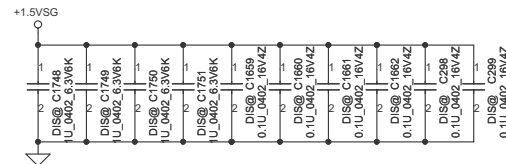
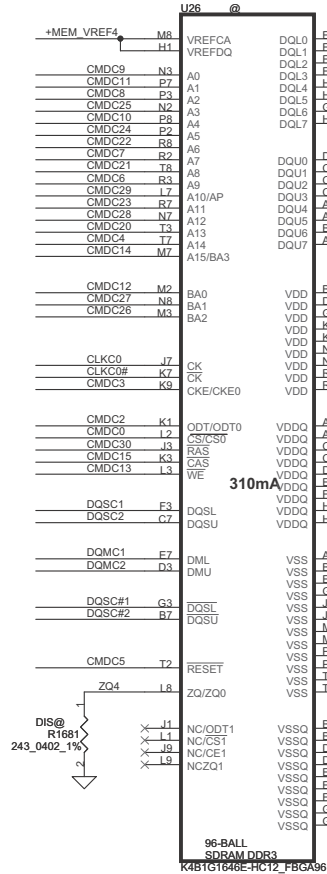
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



NV recommend 0720



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CHE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

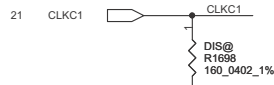
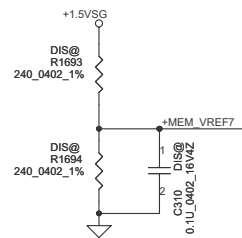
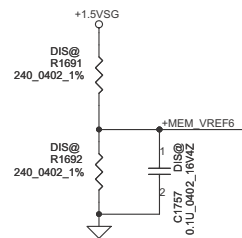
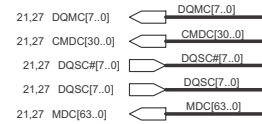
LOW HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CHEx	10k
	RST	10k
	CS*	No Termination

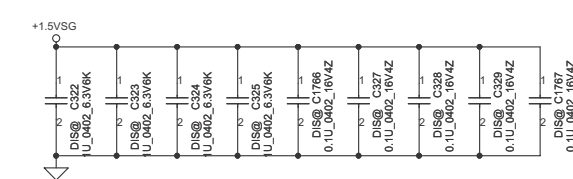
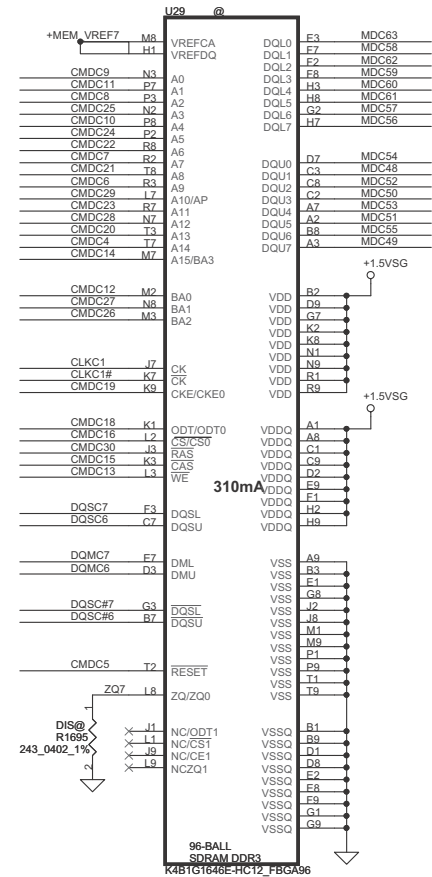
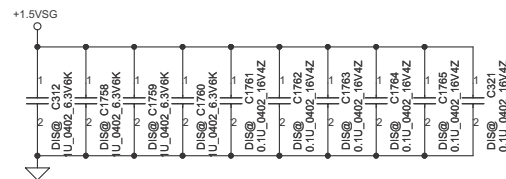
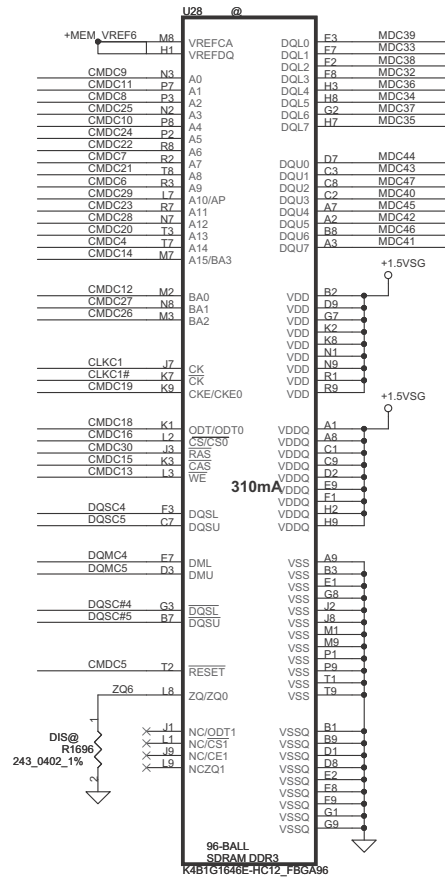
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



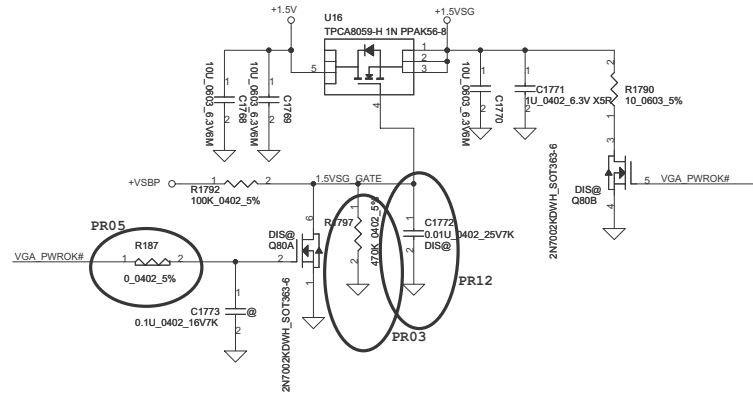
NV recommend 0720



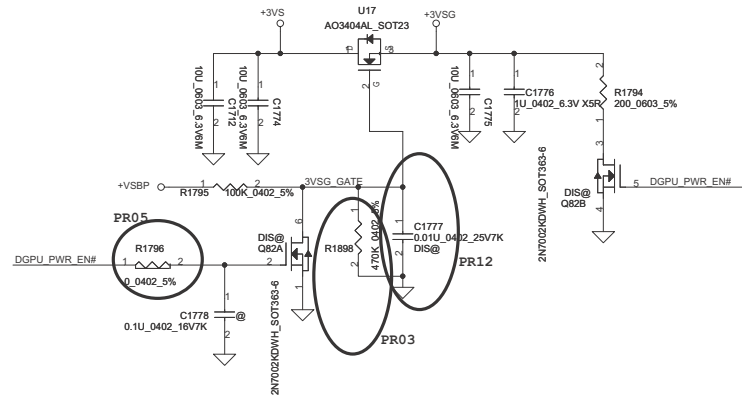
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

LOW HIGH

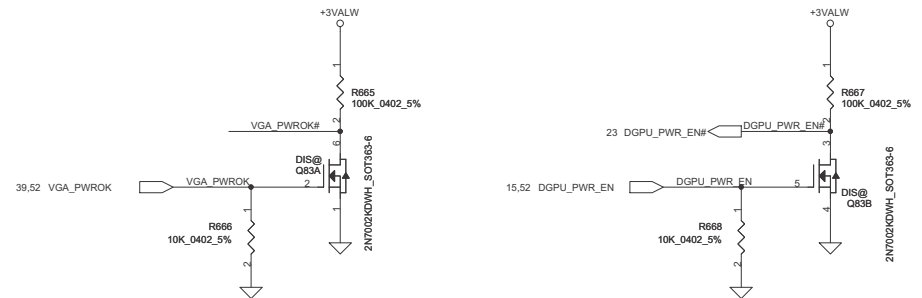
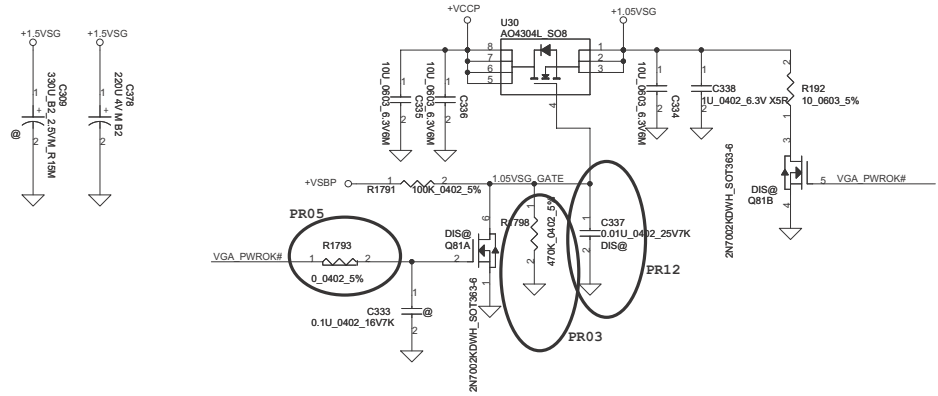
+1.5V to +1.5VSG



+3VS to +3VSG

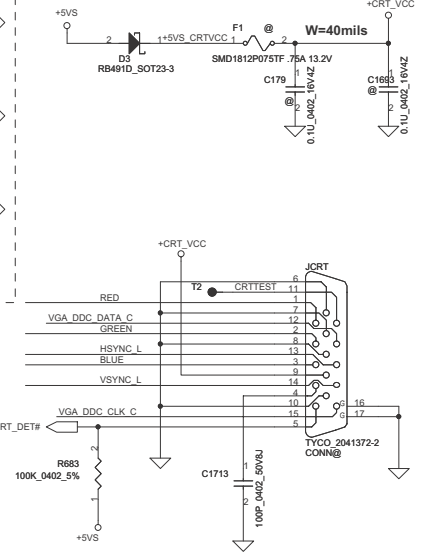
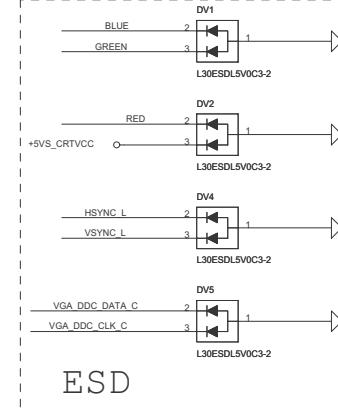
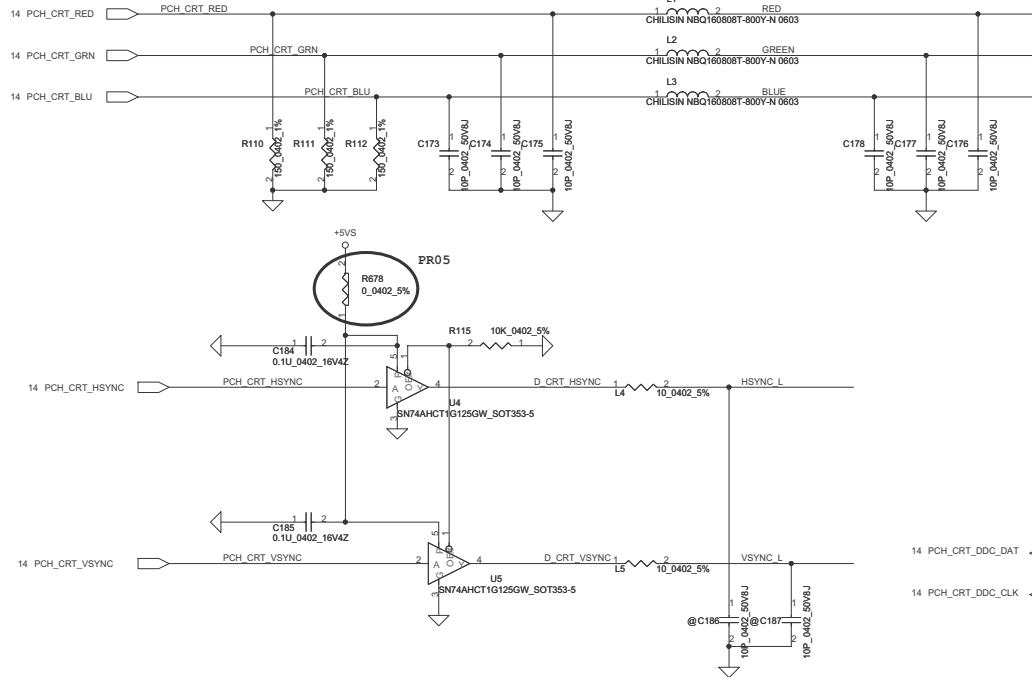


+VCCP to +1.05VSG

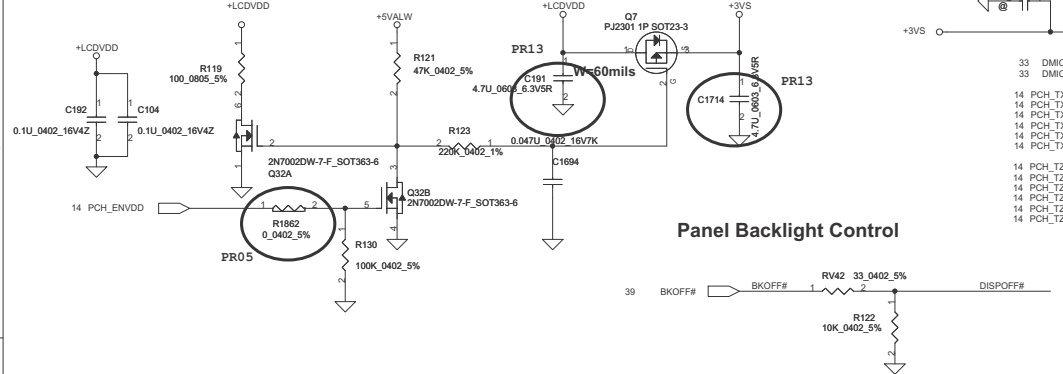


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				Date:	Monday, September 03, 2012
				Sheet	29 of 59
				Rev	8

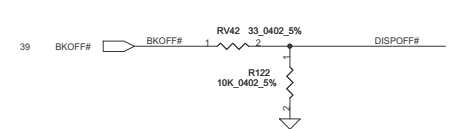
CRT



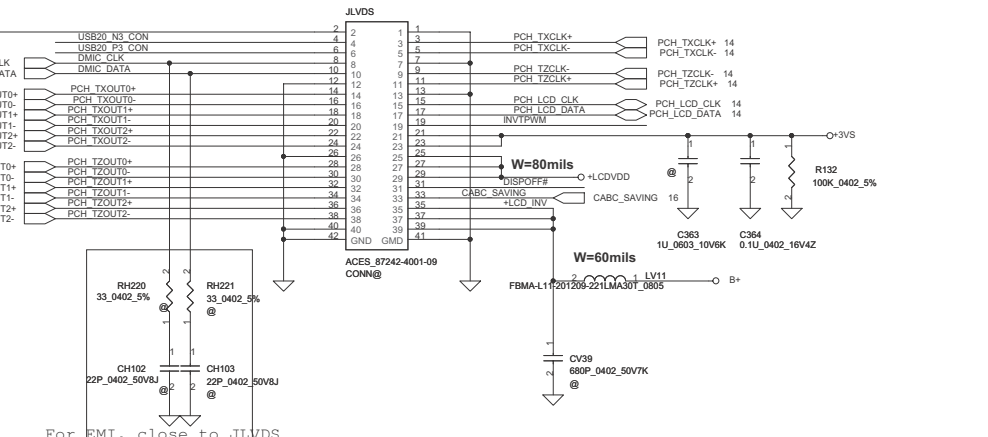
LCD POWER CIRCUIT



Panel Backlight Control



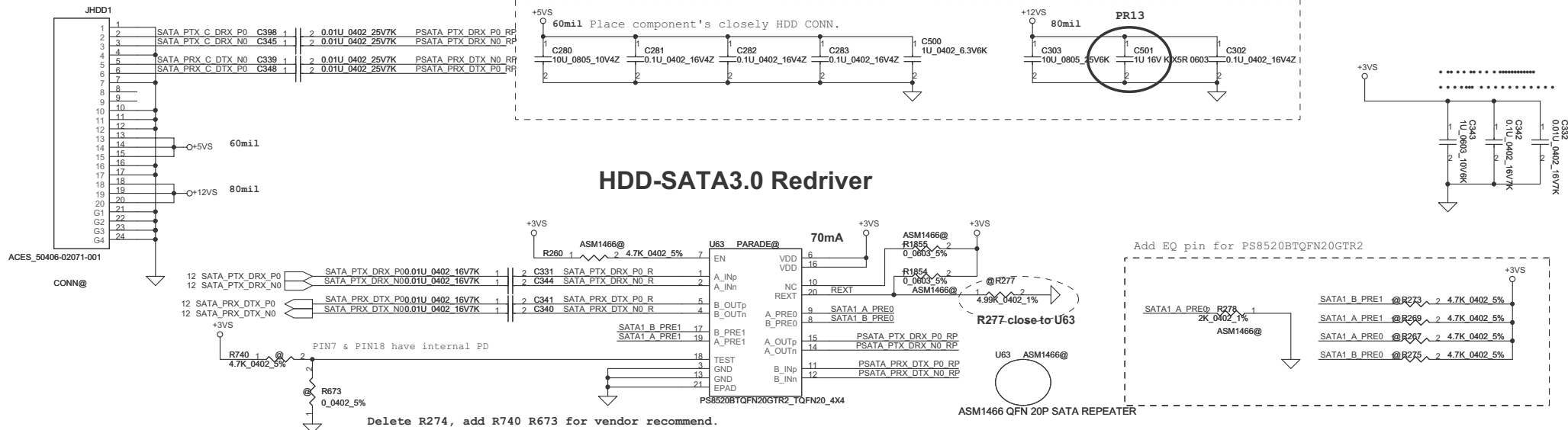
Panel PWM Control



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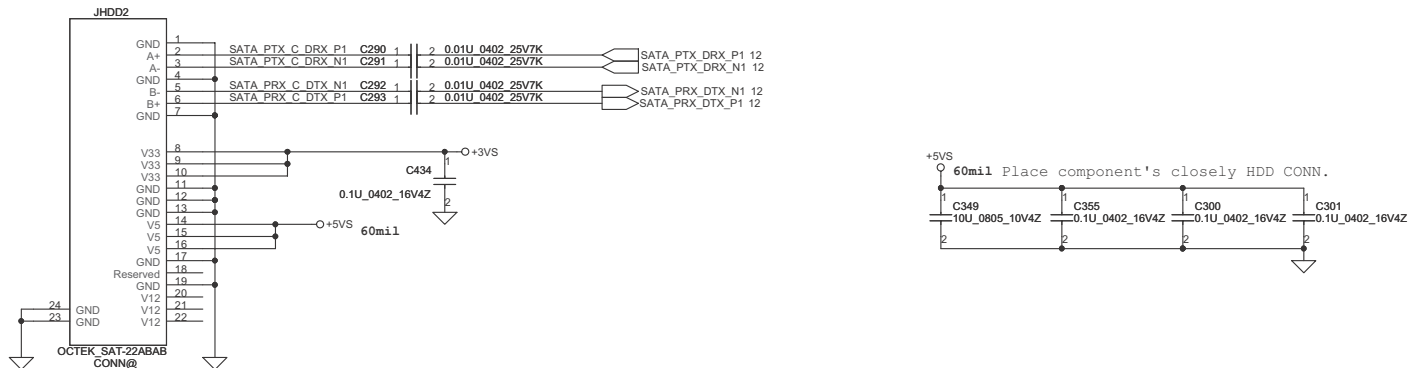
HDD1

SATA HDD 3.5" Conn.



HDD2

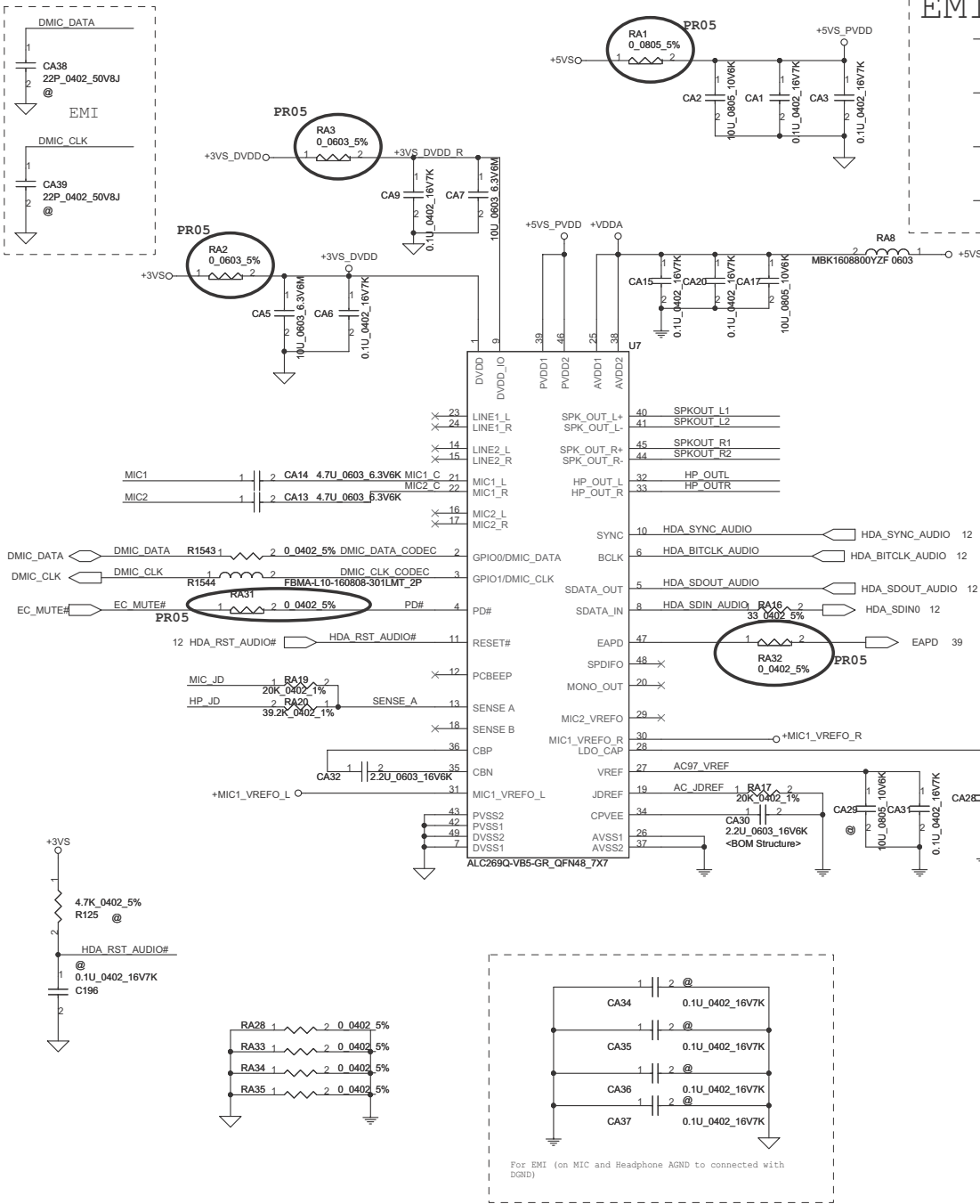
SATA HDD 2.5" Conn.



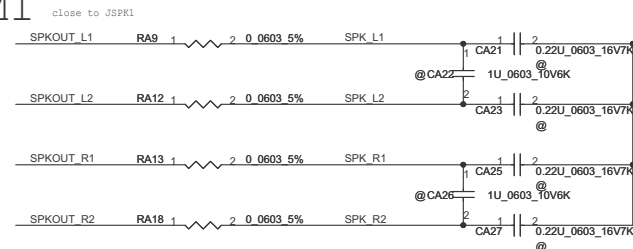
SATA ODD/B Conn.



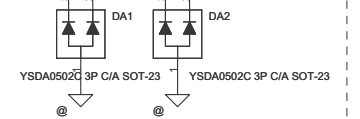
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4019G7			Monday, September 03, 2012	
Sheet 31 of 59				



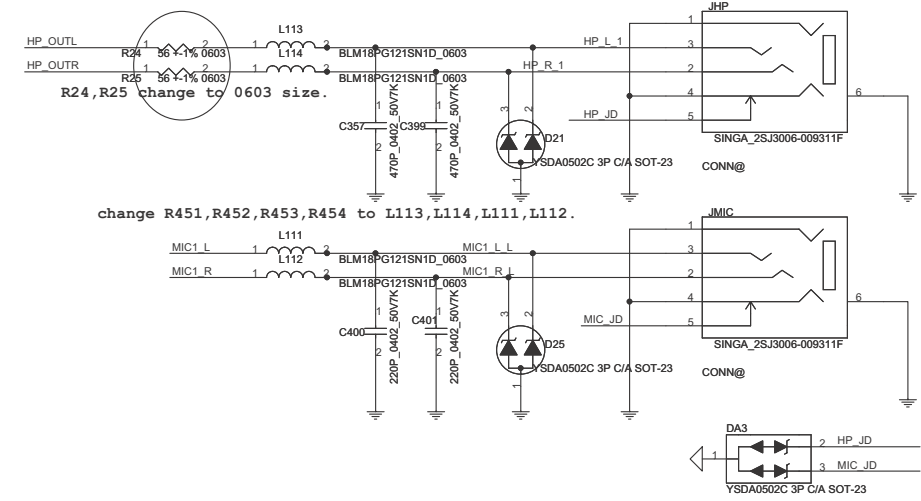
EMI



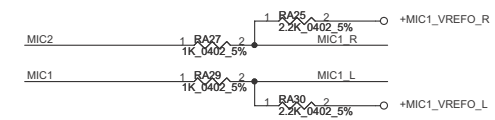
ESD



HP CONN & MIC CONN



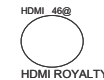
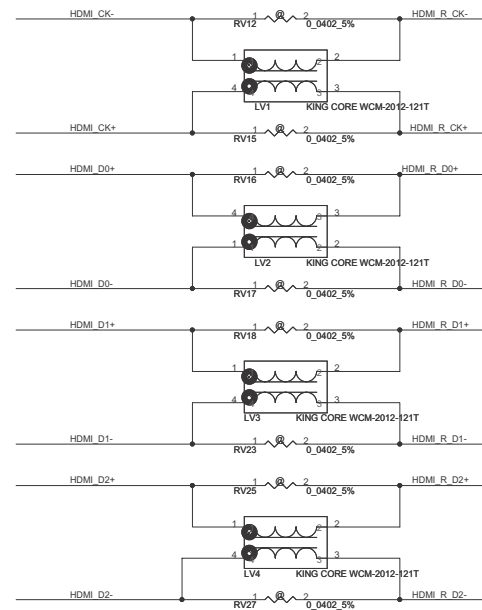
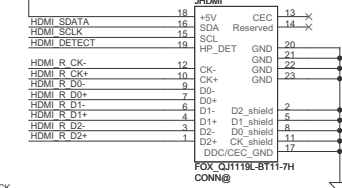
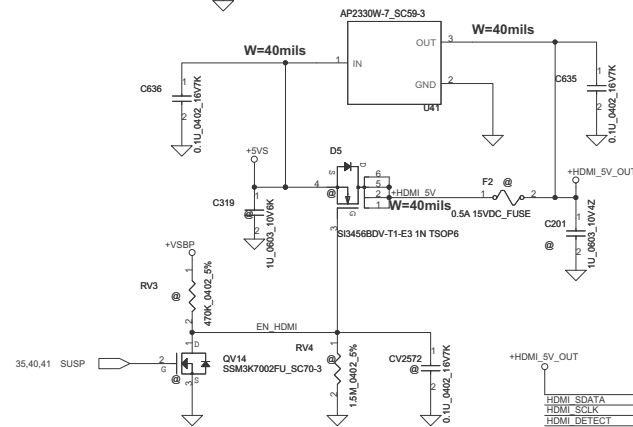
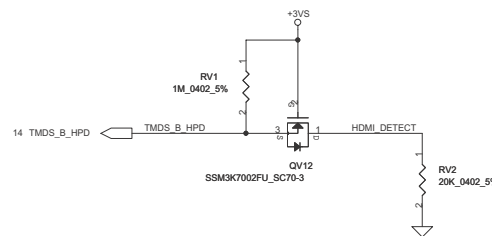
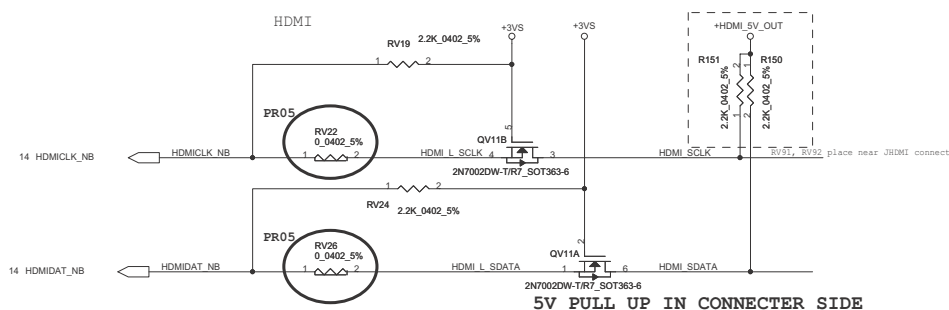
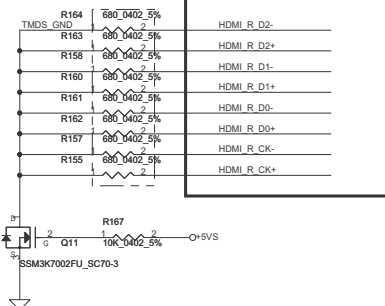
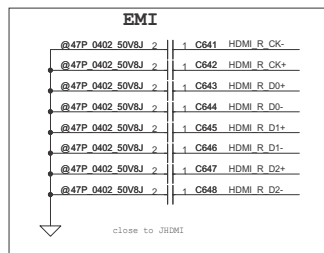
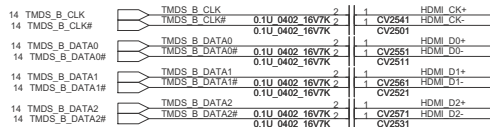
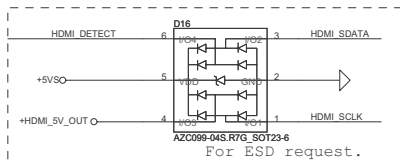
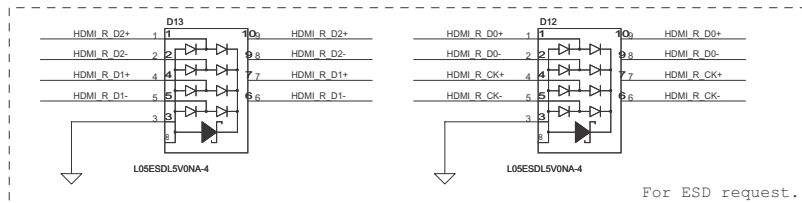
Ext.MIC/LINE IN JACK

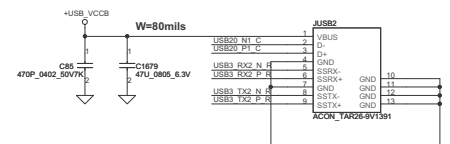
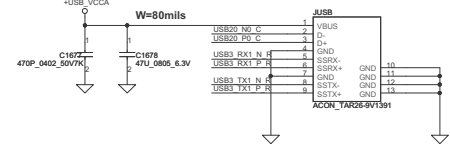
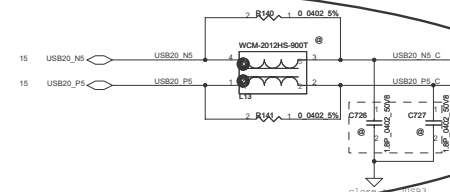
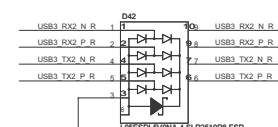
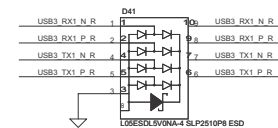
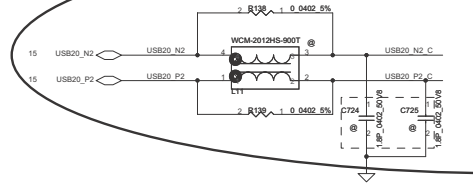
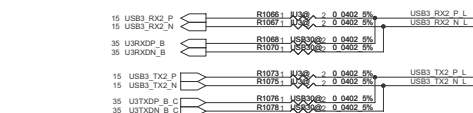
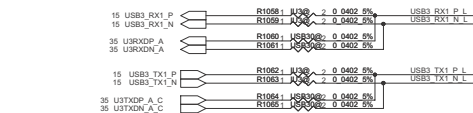
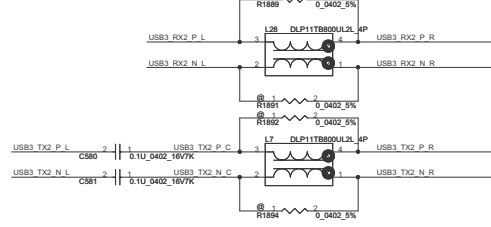
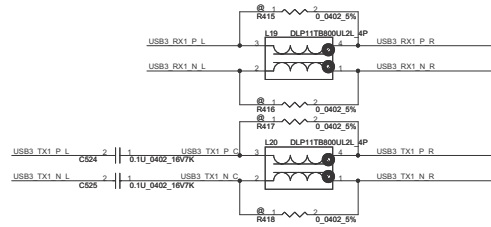


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				Date	Monday, September 03, 2012
				Sheet	33 of 59

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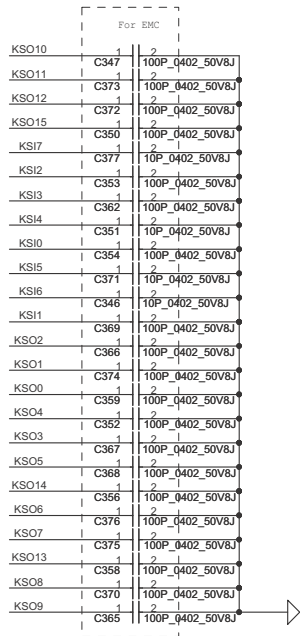
Rev B



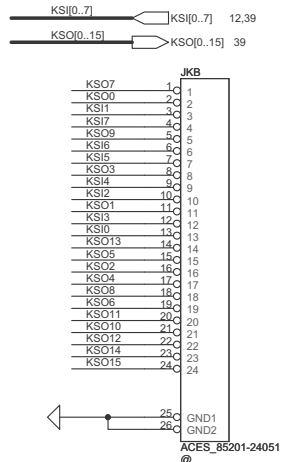


CB	SELCDP	Function
0	X	DCP autodetect charger mode
1	0	S0 charging with SDP only
1	1	S0 charging with SDP or CDP

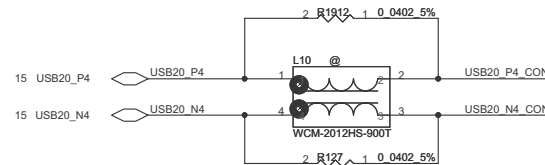
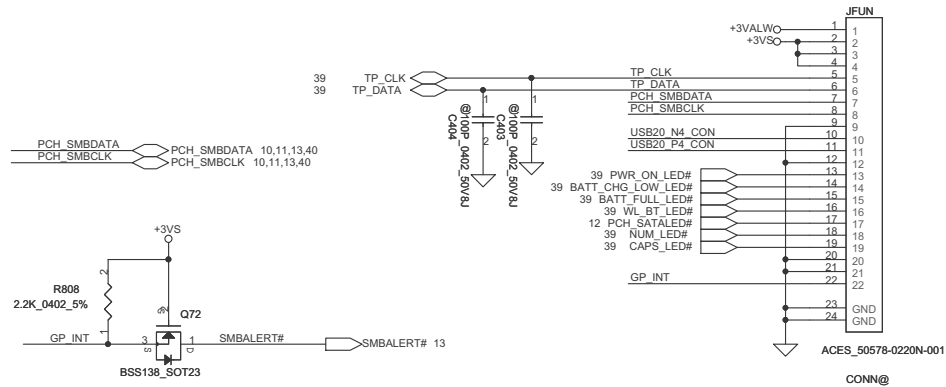
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			Document Number	Rev B
			4019G	
Date	Monday, September 05, 2012		Sheet	36 of 59



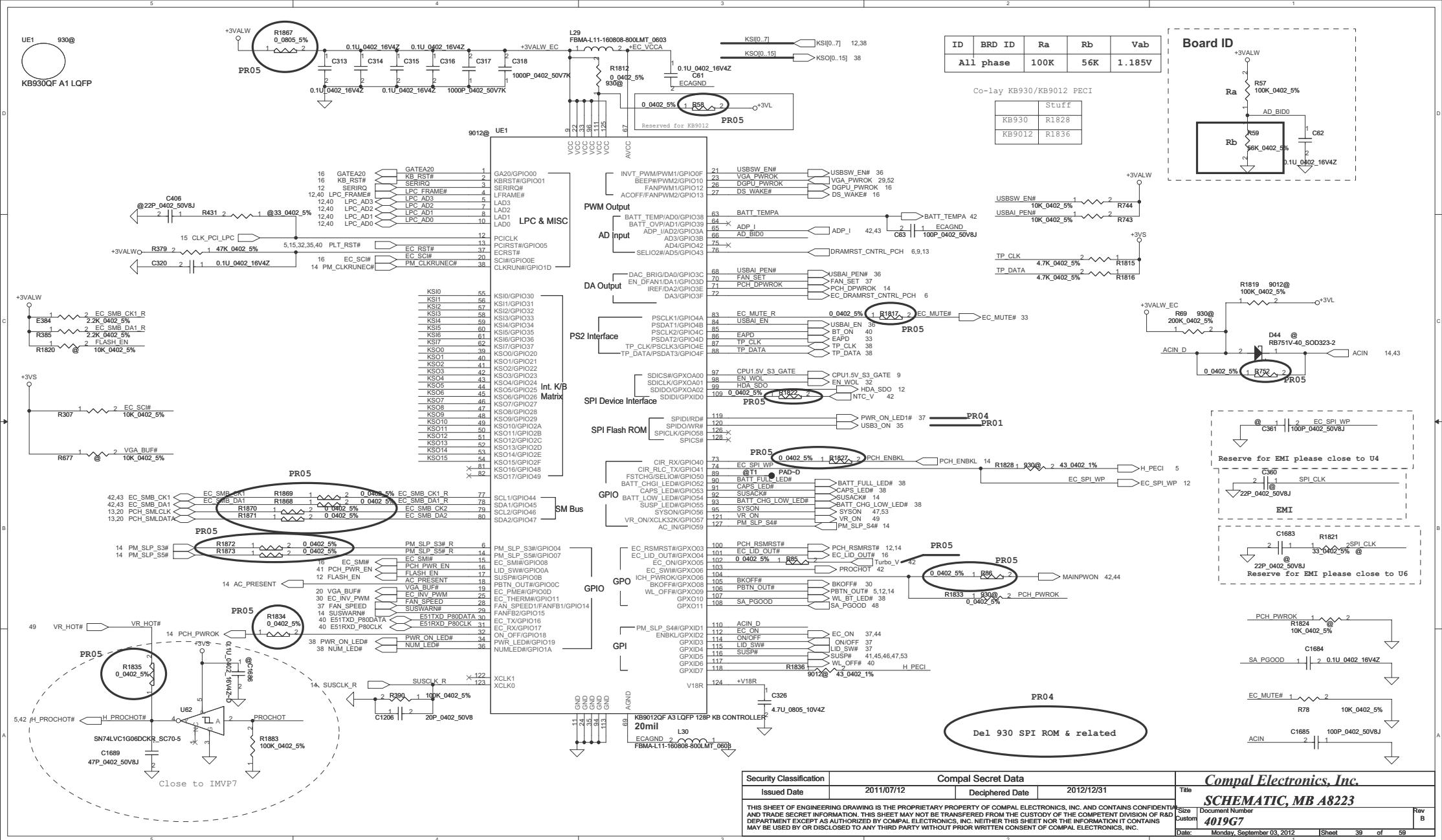
INT_KBD Conn.



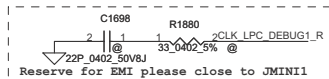
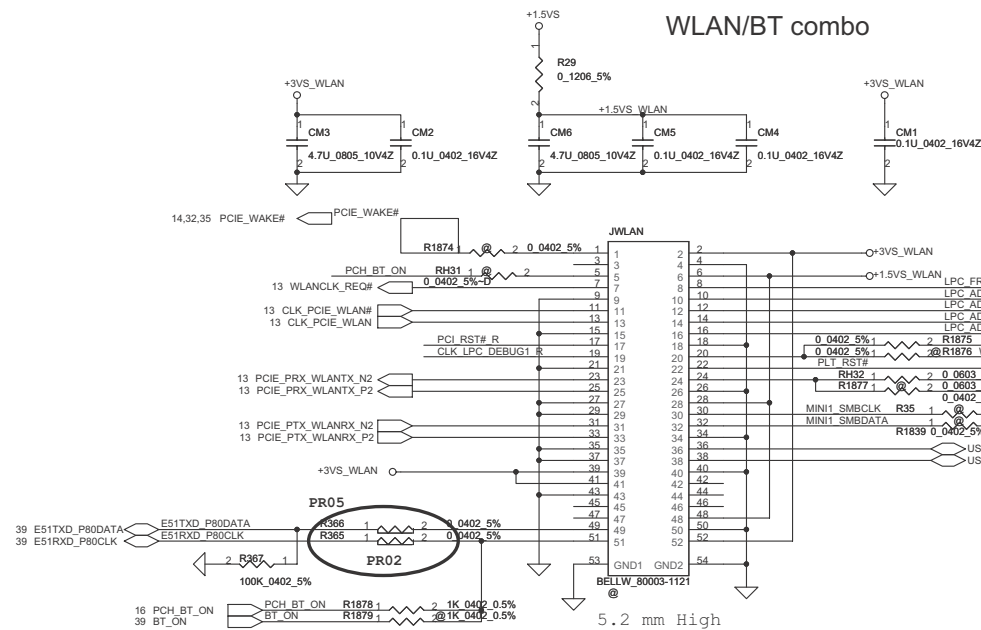
Touch pad & LID & Card Reader & LED small board Connector



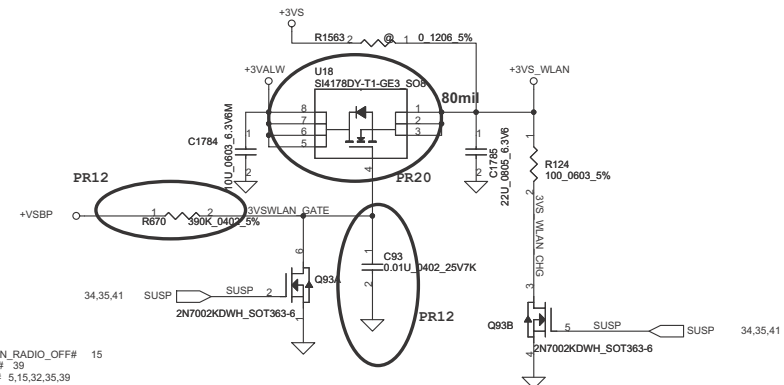
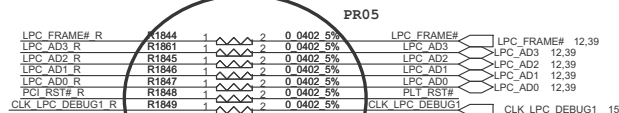
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				Rev	B
				Date:	Monday, September 03, 2012
				Sheet	38 of 59



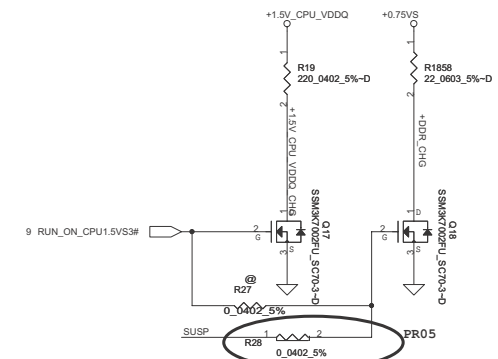
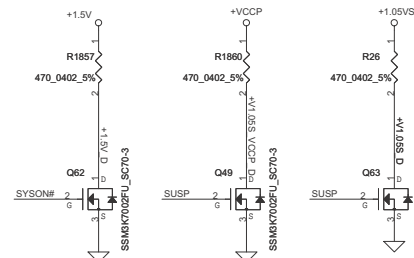
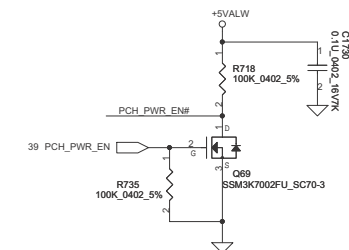
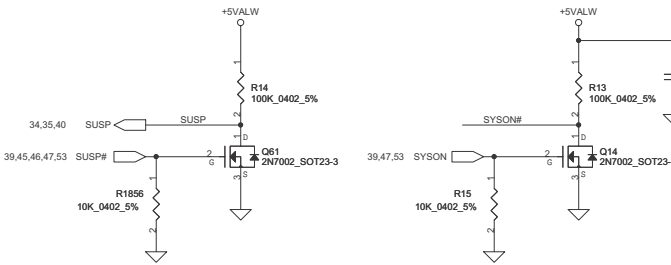
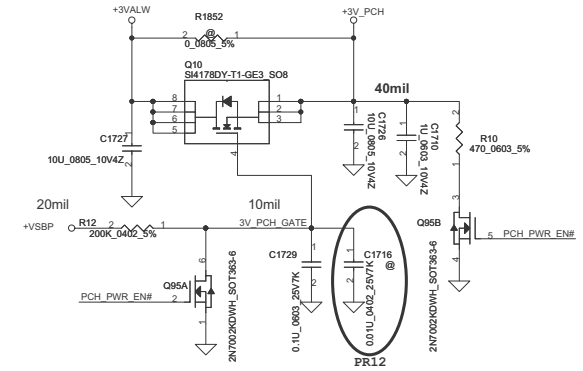
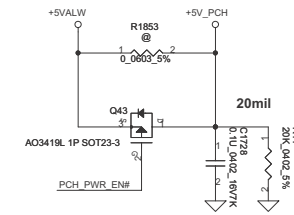
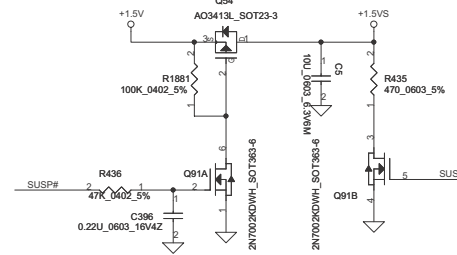
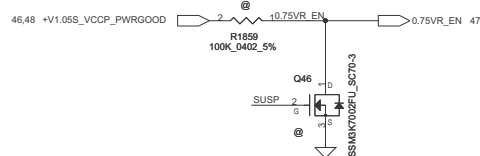
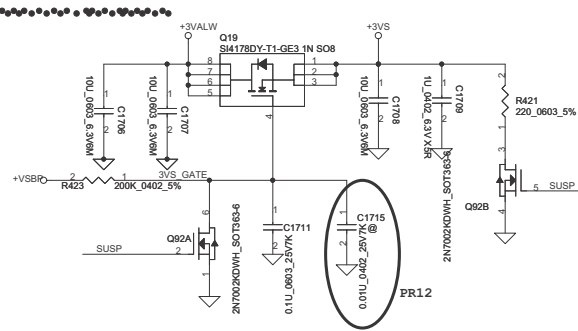
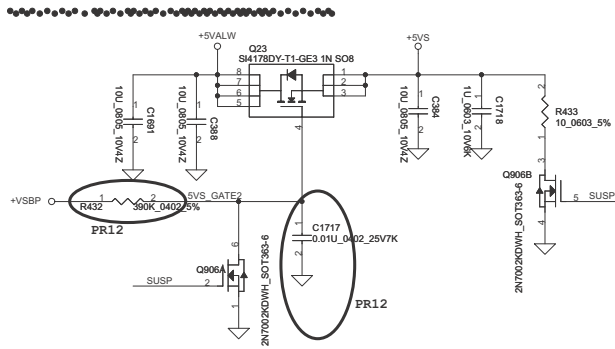
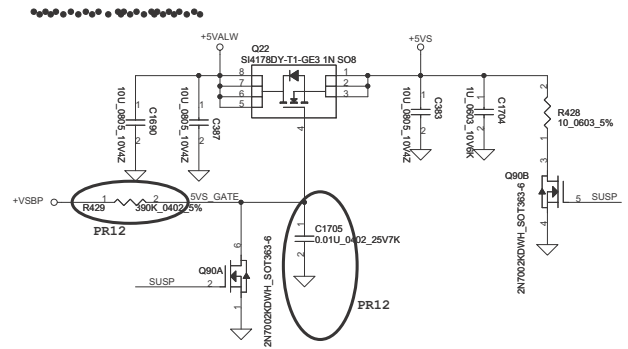
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				Size			Document Number			Rev B		
				Custom			4019G7					
				Date:			Monday, September 03, 2012			Sheet 39 of 59		



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

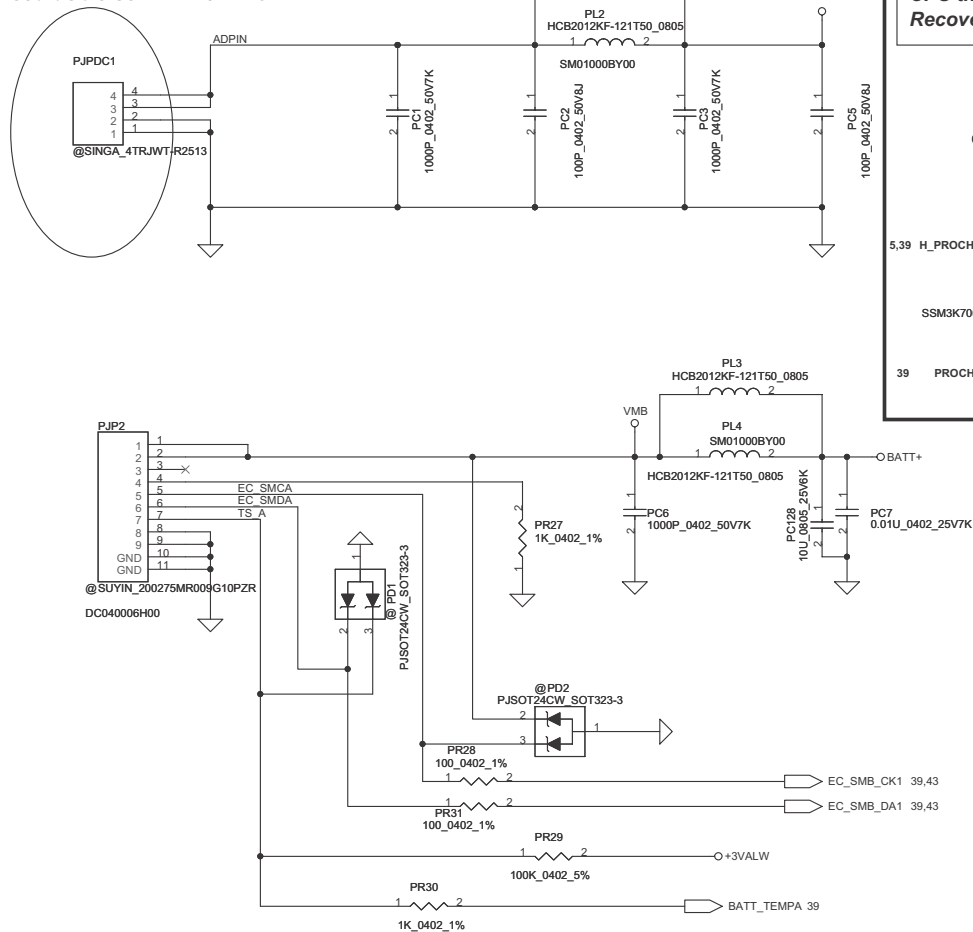


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				Date	Monday, September 03, 2012
				Sheet	40 of 59

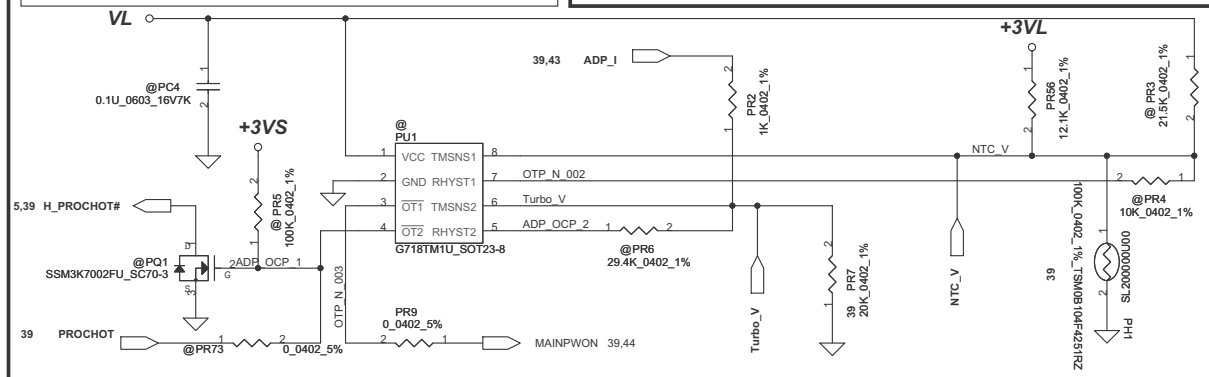


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				Date	Monday, September 03, 2012
				Sheet	41 of 59

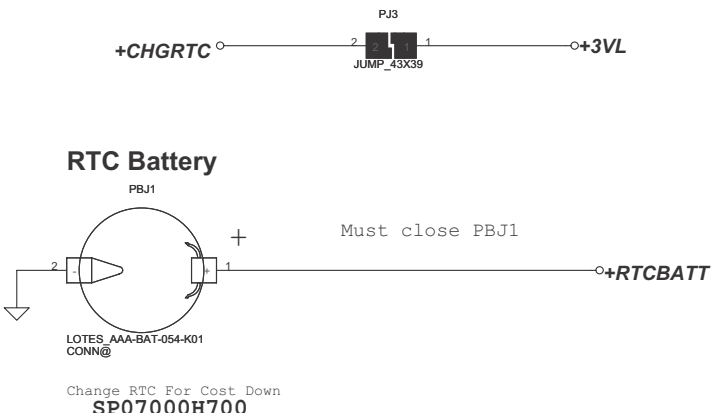
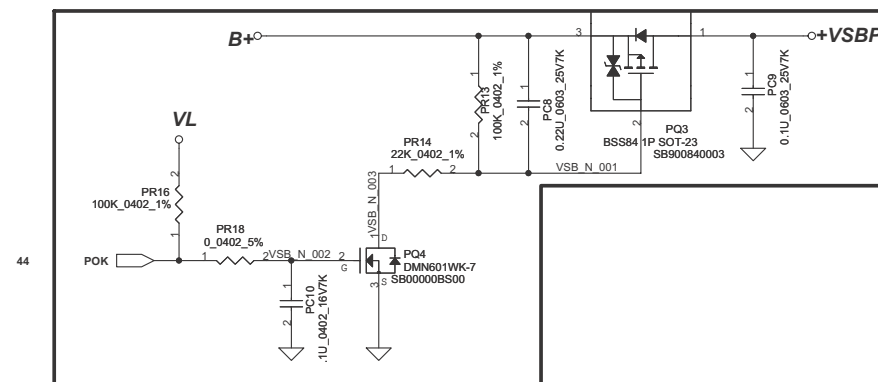
DCIN jack P/N:DC301008L00,
need doble confirm P/N with ME



PH1 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C



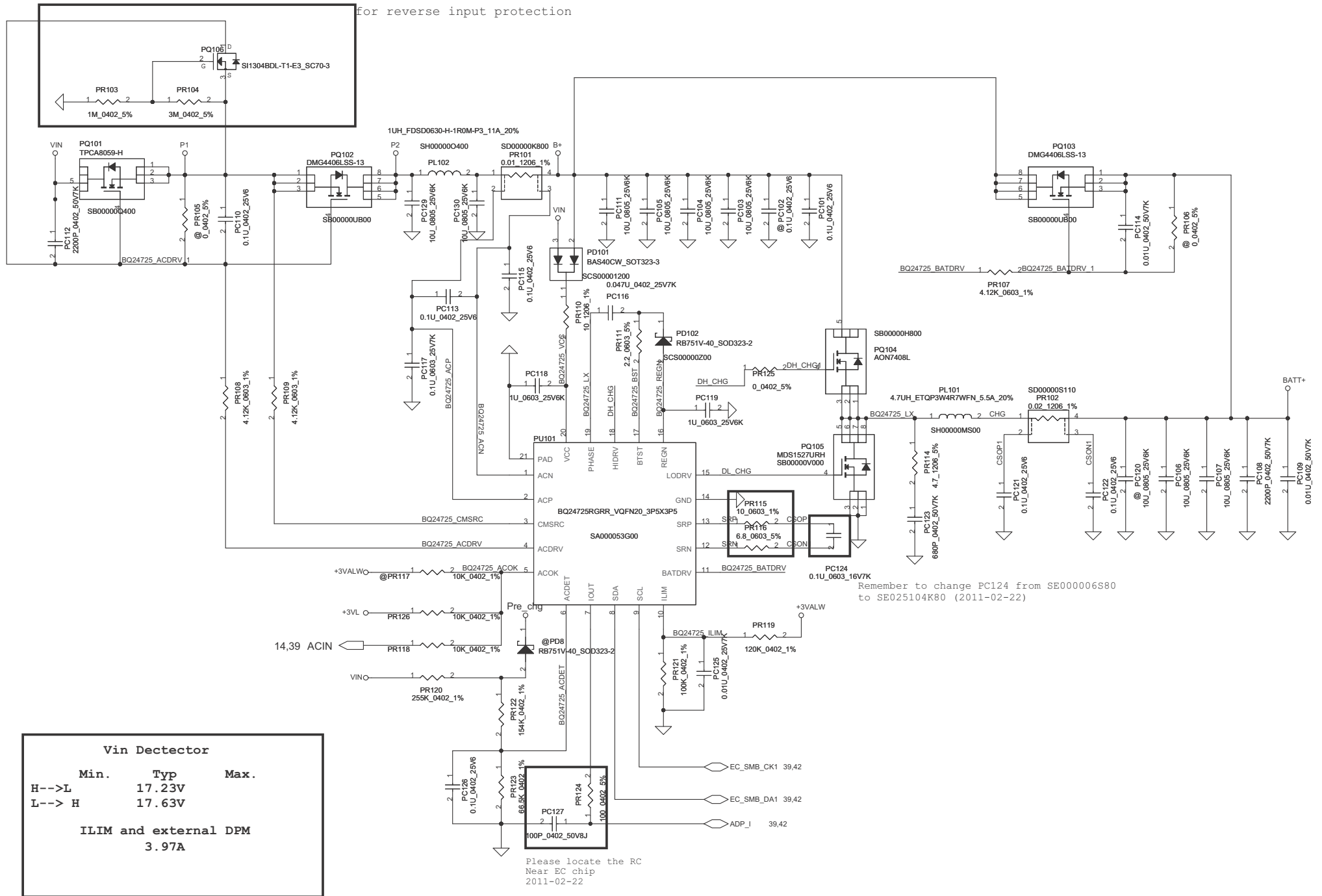
For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR56
PH1, PR2, PQ1, PR7, PQ15, PR73, PR56

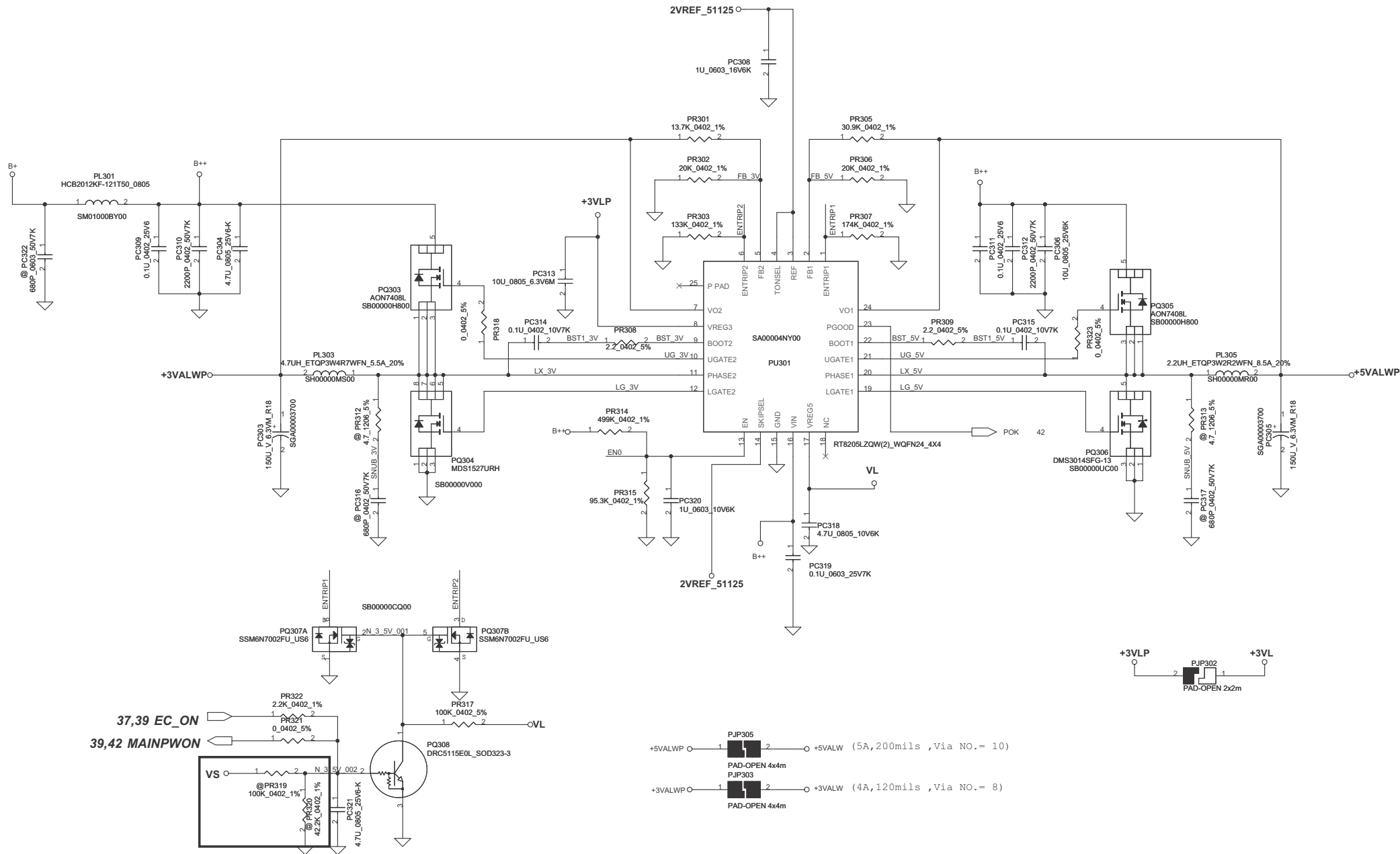


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				Date:	Monday, September 03, 2012
				Sheet	42 of 59

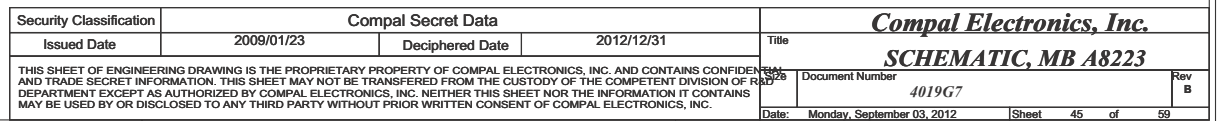
For KB9012 --> Remove all 51_ON# circuit

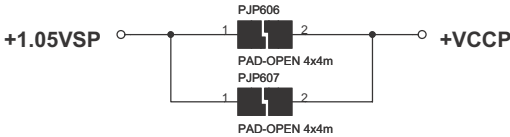
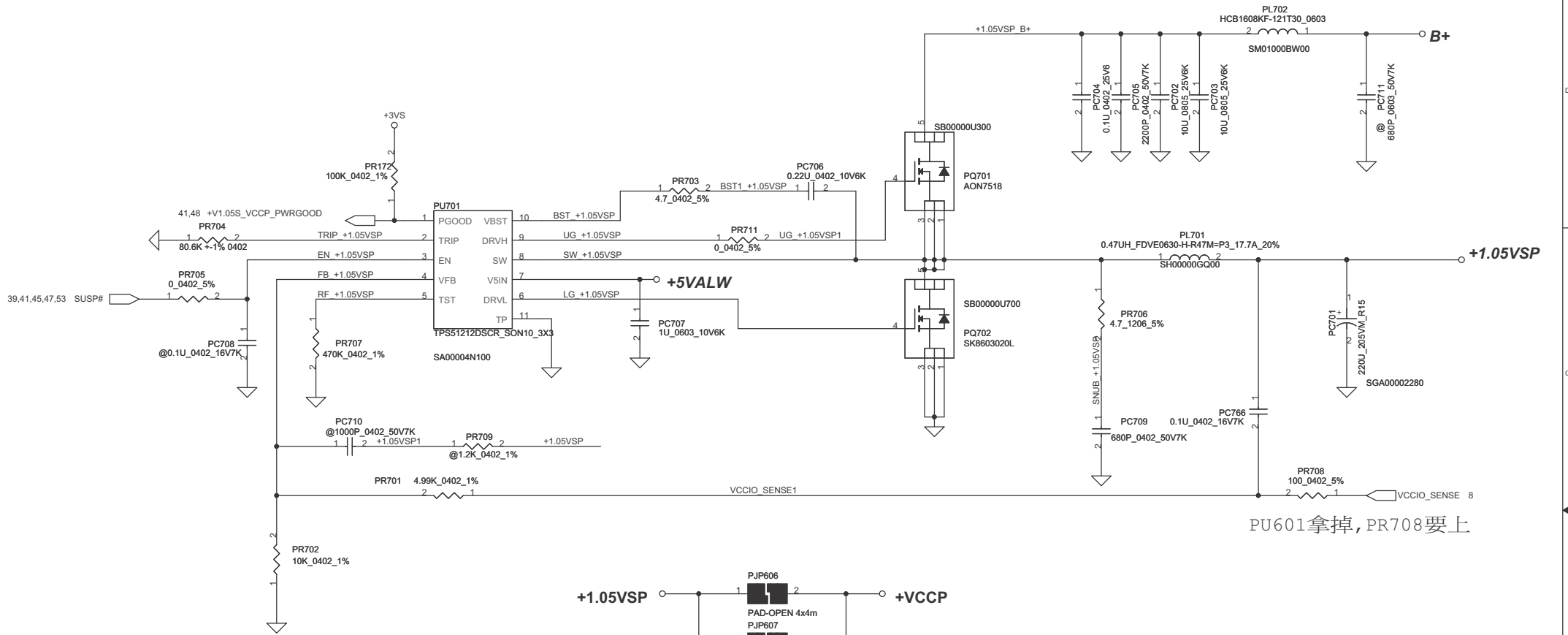
For reverse input protection



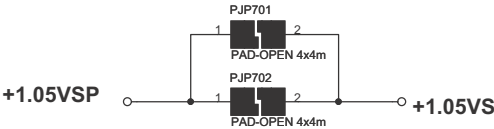


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						Document Number		4019G7		Rev B	
						Date:		Monday, September 03, 2012		Sheet 44 of 59	





(8.5A, 360mils , Via NO.= 17)



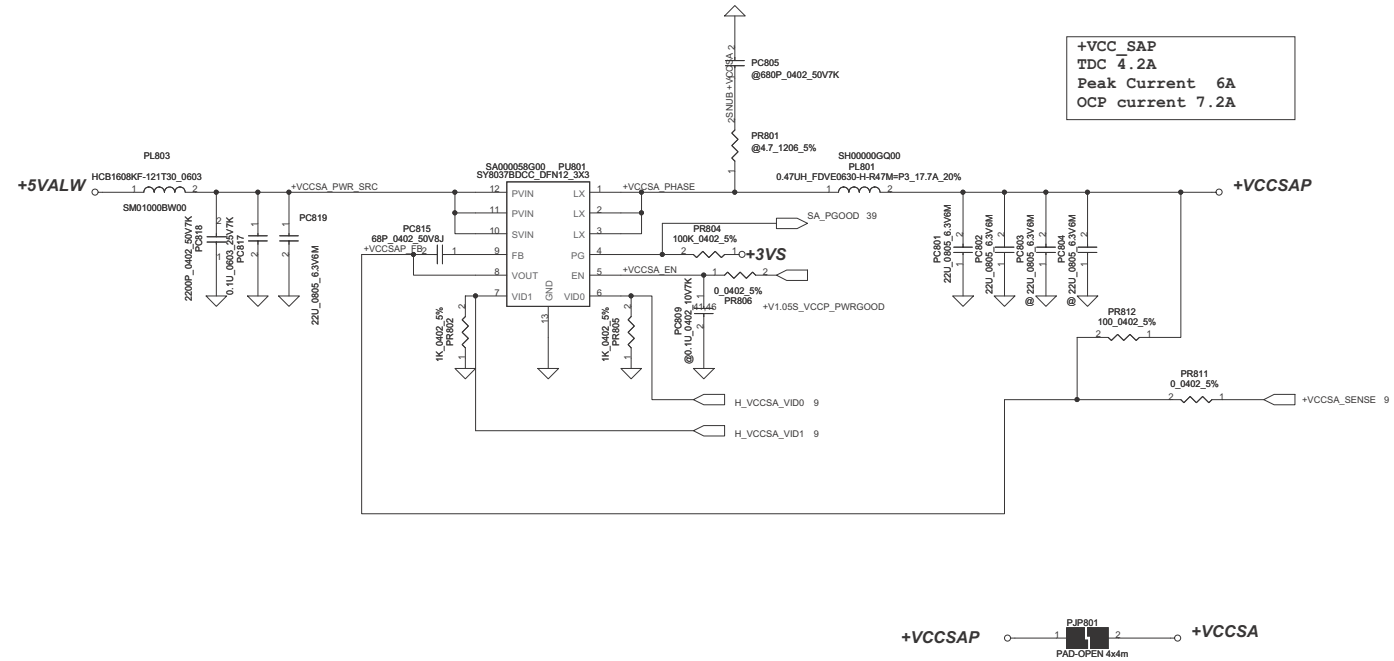
(12A, 480mils , Via NO.= 24)

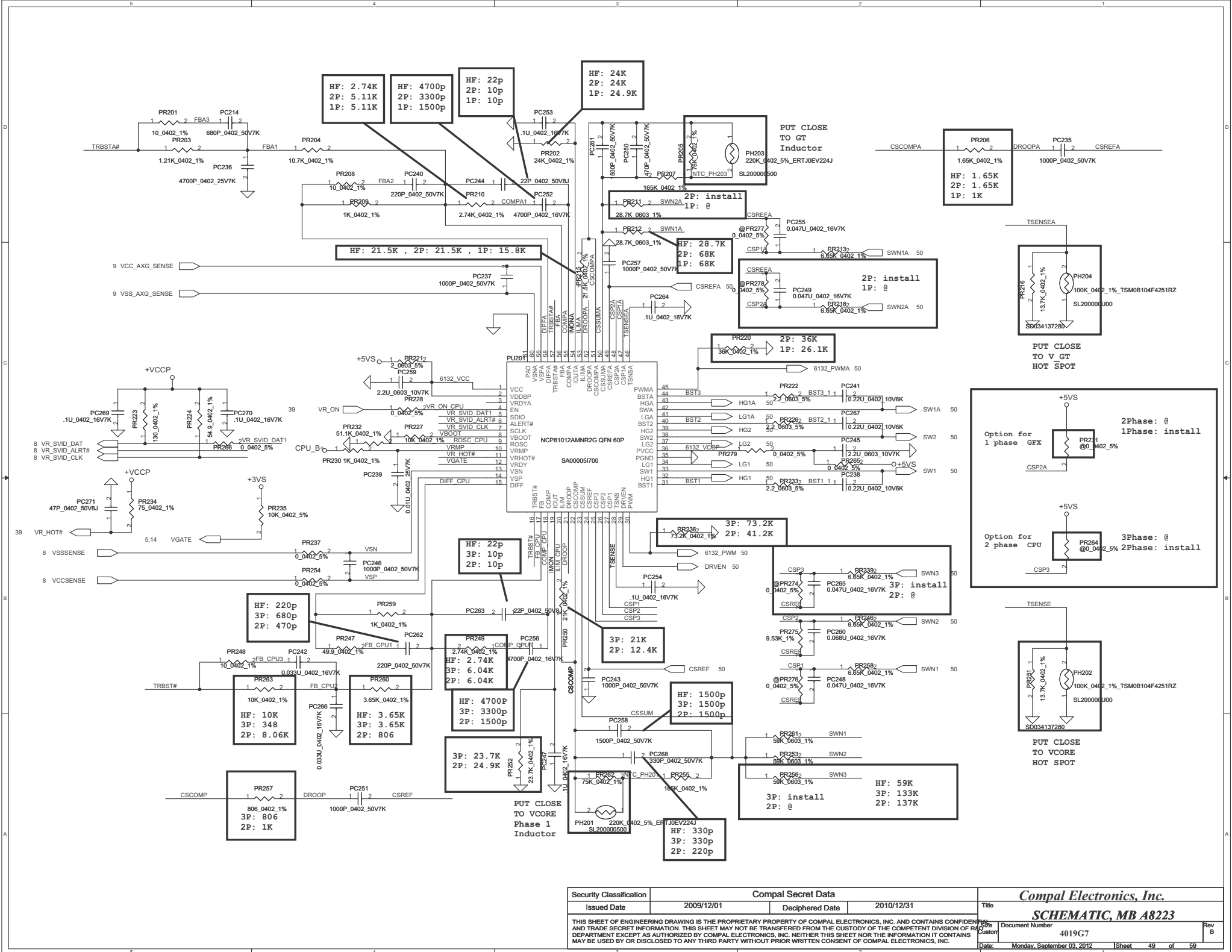
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				Customer	
				4019G7	
				Date:	
				Monday, September 03, 2012	
				Sheet	
				46	
				of	
				59	

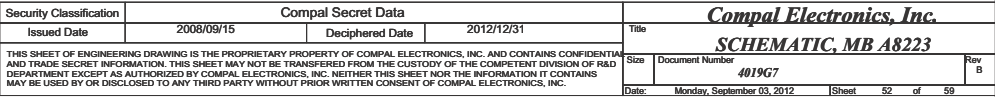
The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.

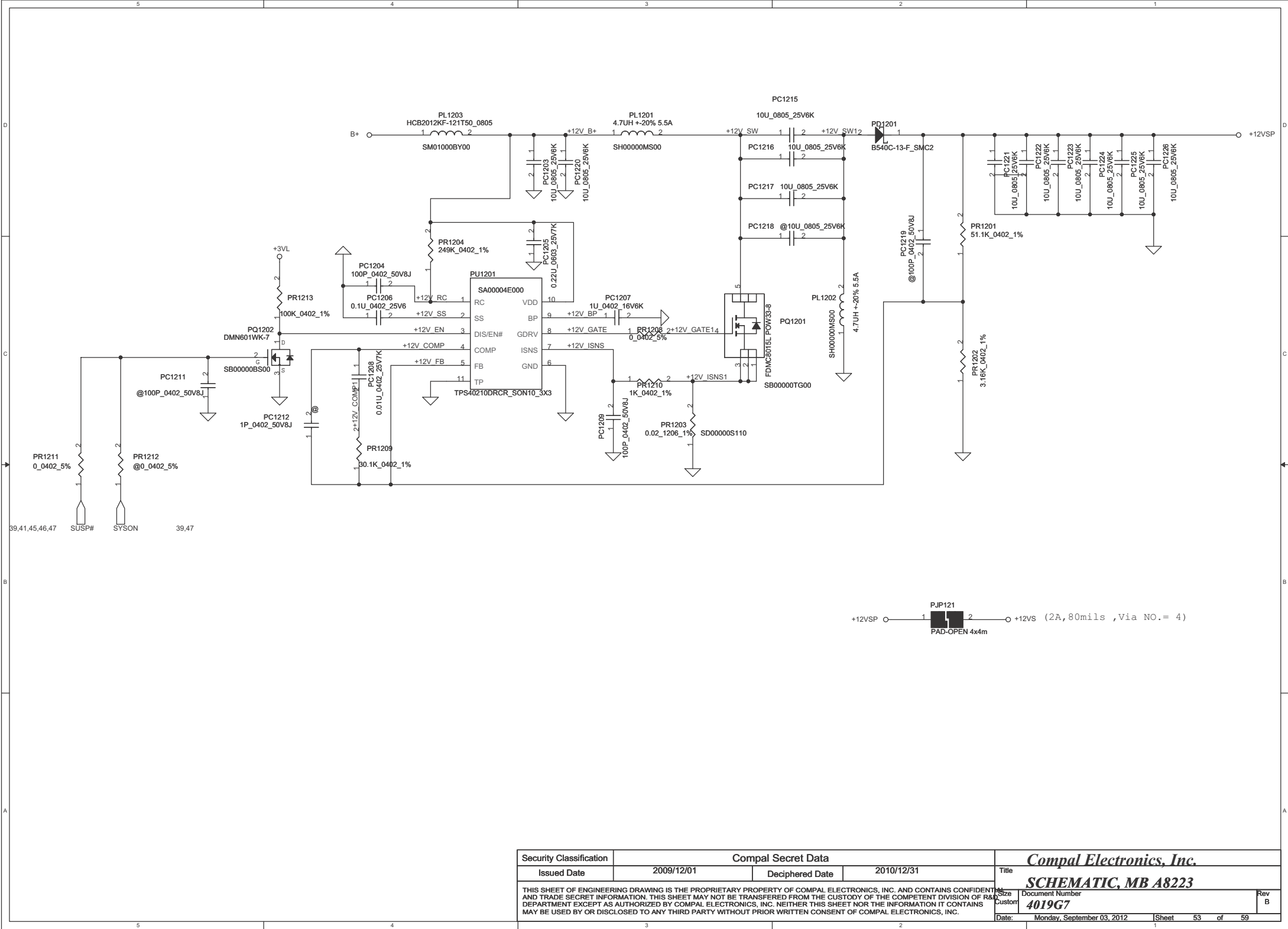
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network



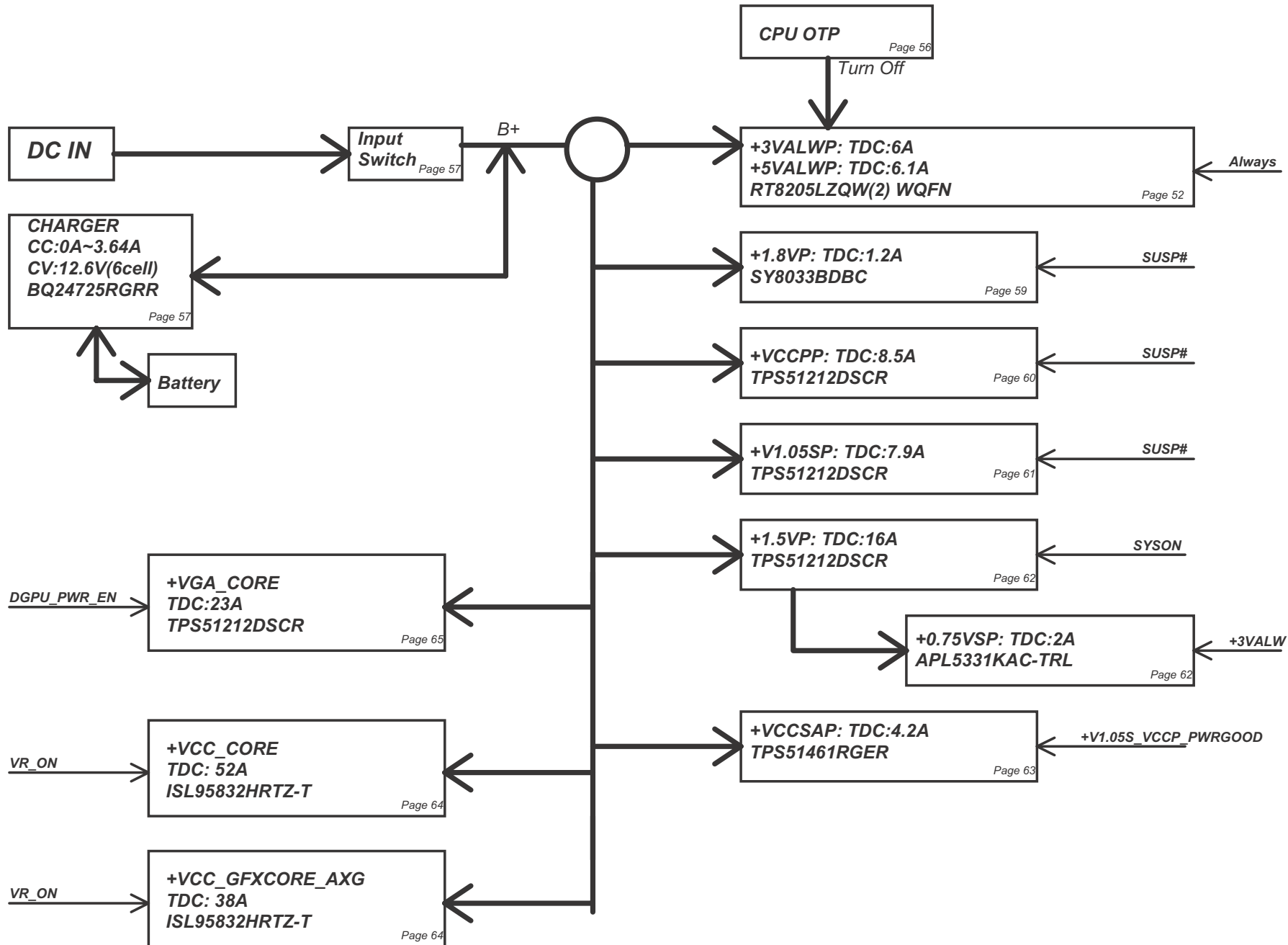






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				Date:	Monday, September 03, 2012
				Sheet	53 of 59
				Rev	B

Power block

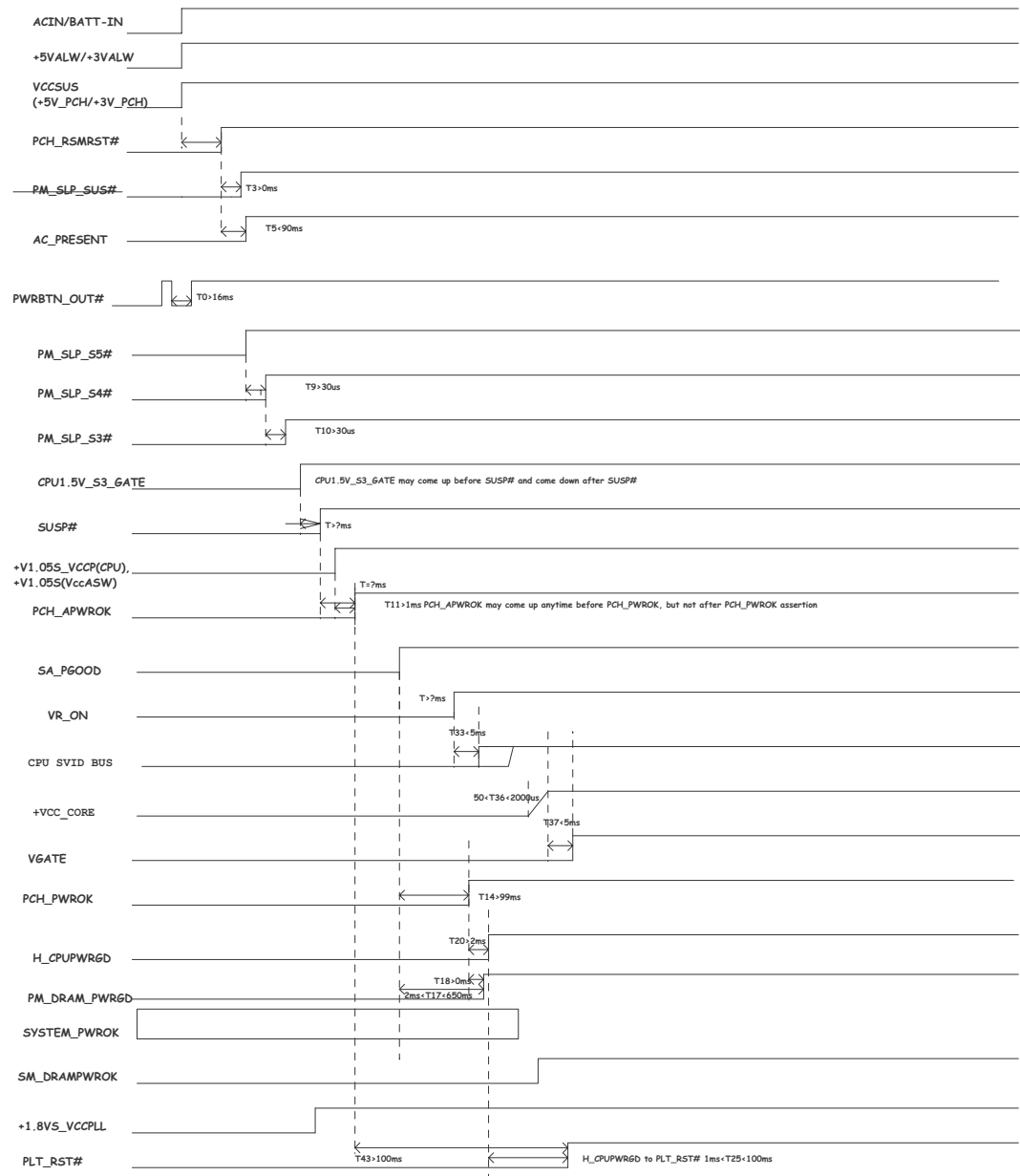


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				Date:	Monday, September 03, 2012
				Sheet	54 of 59

Page 1

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				4019G7	
Date: Monday, September 03, 2012		Sheet 55 of 59			

Timing Diagram for 63 or S4-5/M-off (Suspend Well Off) to S0/M0 [non Deep S4/S5 Platform]



Color	Command
Signal Names	Timing of these signals is set by PCH or processor
Signal Names	Timing of these signals should be met by the platform (EC)
Signal Names	Timing of these signals is set by IntelR MVP
Signal Names	Voltage rails or chip-to-chip buses

HW Version Change List (P. I. R. List)

Page 1/3

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
ER01	02#	Block Diagram	0830	ShouYi	Modify the external USB 3.0 page.		0.2
ER03	35#	PCIe USB3.0 ASM1042	0830	ShouYi	Add External USB3.0 controller circuit.		0.2
ER04	13#	PCH SMBUS,CLK	0830	ShouYi	Add External USB3.0 circuit of PCIE Port4	Modify PCIE-Port4 of PCH circuit.	0.2
ER05	13#	PCH SMBUS,CLK	0830	ShouYi	Add circuit of CLK port3 for external USB3.0	Modify CLK port3 of PCH circuit.	0.2
ER07	16#	CPU RSVD,CFG	0831	ShouYi	Add USB30_SMI# for external USB3.0	Add USB3.0 SMI signal.	0.2
ER08	40#	MINI CARD	0906	ShouYi	Can't boot.	Stuff 0.1uF of C93.	0.2
ER09	07#	CPU RSVD,CFG	0913	ShouYi	For improve layout space.	Add CLK_RES_ITP and CLK_RES_ITP# to TP.	0.2
ER10	13#	PCH SMBUS,CLK	0913	ShouYi	For improve layout space.	Del RH19,RH20,R1758,R1759.	0.2
ER11	37#	FAN/PWRBTN/PCB PN	0914	ShouYi	For mechanic's requirement.	H7 change from 3P3 to 4P1.	0.2
ER12	13#	PCH PCIE,SMBUS,CLK	0922	ShouYi	Reserve R1899 to GND		0.2
ER13	35#	PCIe USB3.0 ASM1042	0922	ShouYi	Modify USB3.0 circuit.	Modify +1.2VUSB to 1.2VS circuit and swap signals. Change R1040 to 47K and ADD R1029 to GND.	0.2
ER14	18#	PCH PWR(7/8)	0922	ShouYi	For support WLAN wake up.	Reserve R381 to +3VALW.	0.2
ER15	05#	CPU PM,XDP,CLK	0922	ShouYi	For improve layout space.	Delete T65,T66.	0.2
ER16	35#	PCIe USB3.0 ASM1042	0922	ShouYi	Delete USB3.0 delay PORST circuit.		0.2
ER17	41#	DC/DC Interface	0922	ShouYi	Modify Q54 P/N.	Change Q54 to SB934130020.	0.2
ER18	29#	VGA DC/DC Interface	0922	ShouYi	Modify U17 P/N and Reserve R1898.		0.2
ER20	14#	PCH DMI,FDI,PM,GFX, DP	0923	ShouYi	HDMI Detect modify.	Delete R213.	0.2
ER21	13#	PCH SMBUS,CLK	0923	ShouYi	For improve +3VS leakage voltage on S3/S4/S5.	Delete Q33 circuit.	0.2
ER22	13#	PCH PCIE,SMBUS,CLK	0923	ShouYi	For 48M CLK EA fail.	Change R1797 from 0 ohm to 22 ohm.	0.2
ER23	36#	USB2.0 USB	0923	ShouYi	Reserve 0 ohm for un-discharge.	Reserve R1886 and R1895.	0.2
ER24	39#	EC KB930	0923	ShouYi	SMBus circuit modify.	Delete R386, R387.	0.2
ER25	37#	FAN/PWRBTN/PCB PN	0927	ShouYi	For LID signal floating.	Add R578 to +3VALW.	0.2
ER26	29#	VGA DC/DC Interface	0927	ShouYi	For DGPU Power Sequence	Change R1793 to 0 ohm and C333 to unstuff.	0.2
ER27	07#	CPU RSVD,CFG	0928	ShouYi	Delete T70,T71 (no need)		0.2
ER28	31#	HDD,ODD/B Conn	0928	ShouYi	For co-lay ASM1466.	Delete R268,R272,R270. Change R278 to 2K and modify to ASM1466@. Reserve R1854,R1855 to +3VS.	0.2
ER29	35#	PCIe USB3.0 ASM1042	0928	ShouYi	Remove no use the signals.	Delete R1021,R1033,R1034,R1028,R1031.	0.2
ER30	39#	EC KB930	0929	ShouYi	Remove no use item of crystal circuit.	Delete Y5, C94, C1783.	0.2
ER31	29#	VGA DC/DC Interface	0929	ShouYi	Prevent R1792 for big current damage.	Change R1792 to 10K.	0.2
ER32	29#	VGA DC/DC Interface	0929	ShouYi	For +3VSG voltage issue on power off status.	Change R1794 to 200.	0.2
ER33	12#	PCH SATA,HDA, SPI,LPC	1004	ShouYi	For Crystal Vendor's recommendation.	Change C204,C207 from 12pF to 18pF.	0.2
ER34	32#	LAN RTL8111F	1004	ShouYi	For Crystal Vendor's recommendation.	Change C89,90 from 20pF to 12pF. Change Y2 to SJ10000E800.	0.2
ER35	13#	PCH PCIE,SMBUS,CLK	1004	ShouYi	For Crystal Vendor's recommendation.	Change C288,C243 from 20pF to 12pF. Change Y3 to SJ10000E800	0.2
ER36	20#	N13P PEG & DAC	1004	ShouYi	For Crystal Vendor's recommendation.	Change C1735,C1736 from 18pF to 12pF. Change Y4 to SJ100009700.	0.2
ER37	41#	DC/DC Interface	1004	ShouYi	Improve the +5VS charge current.	Change R428 from 220 to 10 ohm.	0.2
ER38	15#	PCH PCI,USB,NVRAM	1005	ShouYi	Change resistor type to from RP type to 0201.	Change RP1,RP2,RP3 to 0201 size. (R1900~R1910)	0.2
ER39	35#	PCIe USB3.0 ASM1042	1006	ShouYi	For crystal vendor's recommend.	Change Y9 for cost down. Change C1004, C1006 to 12pF.	0.2
ER40	37# 39#	FAN/PWRBTN/PCB PN EC ENE KB930	1006	ShouYi	For Power team's requirement.	Change the +3VLP to +3VL.	0.2
ER41	05#	CPU PM,XDP,CLK	1006	ShouYi	Reserve pull high +3V_PCH to U1.	Change the +3VS to +3V_PCH.	0.2
ER42	13#	PCH PCIE,SMBUS,CLK	1006	ShouYi	Reserve pull down to GND for Deep S3.	Reserve R1911 to GND.	0.2
ER44	41#	DC/DC Interface	1012	ShouYi	For EMI's requirement.	Add R1781, R1730 0.1uF to GND.	0.2
ER45	32#	LAN RTL8111F	1012	ShouYi	For EMI's requirement.	Change RL437,RL438 to C268,C311 (0.1uF).	0.2
ER46	06#	CPU DDR3	1020	ShouYi	For Deep S3 modified.	Change R63 to un-stuff. Change R1720 to stuff.	0.2
ER47	09#	CPU PWR/VSS	1020	ShouYi	For EMI's requirement.	Add C236.	0.2
ER48	09#	CPU PWR/VSS	1020	ShouYi	For Intel review feedback item.	Add R280	0.2

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<small>Date</small> Monday, September 03, 2012				<small>Sheet</small> 57 of 58	

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
ER49	10#,11# 36#,37#,31#		1020	ShouYi	Change size from 0603 to 0402.	C121,C132,C134,C143,C145,C148,C158,C160 C169,C171,C1680,C1779,C1780,C500	0.2
ER50	12#		1020	ShouYi	For crystal's recommend.	Change Y1 to SJ10000DM00	0.2
ER51	15#	PCH PCI,USB,NVRAM	1020	ShouYi	For Intel review feedback item.	Add R271 to +3VS.	0.2
ER52	14#,16#		1020	ShouYi	For Deep S3 circuit modified.	Add R751,R230. Reserve R805,R804,R803,R802,R801,R800	0.2
ER53	17#	PCH PWR	1020	ShouYi	For Intel review feedback item.	Change L24 to R304.	0.2
ER54	18#	PCH PWR	1020	ShouYi	For Intel review feedback item.	Change L13 to R290.	0.2
ER55	05#	CPU PM,XDP,CLK	1020	ShouYi	For EMI's requirement.	Add R30.	0.2
ER56	22#	N13P LVDS TMDS	1020	ShouYi	For NV's recommend.	Change R1620 to 45K.	0.2
ER57	39#	EC KB930	1020	ShouYi	For Deep S3 reserve circuit.	Modified EC GPIO.	0.2
ER58	20# 39#	N13P PEG&DAC EC KB930	1020	ShouYi	For dGPU thermal throttling.	Add R430. Change R677 to unstuff.	0.2
ER59	12# 39#	PCH SATA,HDA,SPI. EC ENE KB930	1020	ShouYi	SPI flash data crisis prevention.	Add Q71, Reserve R137 and R135.	0.2
ER60	30# 32# 33# 34#	LVDS & CRT ; LAN HDMI ; HD Audio Codec	1024	ShouYi	Change IO connector symbol.	Modify JHDMI, JHP, JM1C Modify JCRT, JLAN	0.2
ER61	32#	LAN RTL8111F	1028	ShouYi	For EMI's requirement.	Change UL2 to SP050007G00	0.2
ER62	34# 36#	HDMI USB2/USB3	1028	ShouYi	For EMI's requirement.	Change D12,D13,D41,D42 to SC300002C00	0.2
ER62	30#	LVDS & CRT	1028	ShouYi	For EMI's requirement.	Change DV1,DV2,DV4,DV5 to SCA00001L00	0.2
ER63	33#	Audio Codec ALC269	1028	ShouYi	For EMI's requirement.	Change D21,D25,DA3 to SCA00001I00	0.2
ER2-01	38#	KB/TP/LED/FUNC/LID	1122	ShouYi	For change Click Pad from Glide Pad.	Add PCH_SMBDATA&CLK & GP_INT signals	0.3
ER2-02	13#	PCH PCIE,SMBUS,CLK	1122	ShouYi	For change Click Pad from Glide Pad.	Add SMBALERT# signals page connect	0.3
ER2-03	39#	EC ENE-KB9012	1122	ShouYi	For change Click Pad from Glide Pad.	Change TP_CLK&DATA pull up to +3VS.	0.3
ER2-04	34#	HDMI/Level Shift	1122	ShouYi	For HDMI LOYALTY.	Add HDMI 46@ for HDMI logo.	0.3
ER2-05	15#	HDMI/Level Shift	1125	ShouYi	For +3VSG leakage current.	Change R271 to un-stuff. Add R272 to GND.	0.3
ER2-06	12#	PCH SATA,HDA,SPI,LPC	1205	ShouYi	For Crystal vendor's requirement.	Change C204 from 18pf to 15pf.	0.3
ER2-07	35#	USB3.0 ASM1042	1205	ShouYi	Modify the USB3.0 power sequence.	Change R1040 to 51K. Change C1011 to 2.2uf.	0.3
ER2-08	38#	KB/TP/LED/FUN/LID	1205	ShouYi	Change LED/B connector and modify the schematic.	Change JFUN to 22pin and modify the circuit.	0.3
ER2-09	12#	PCH SATA,HDA,SPI,LPC	1209	ShouYi	Add SPI-ROM for WIN8	Add SA000039A20 to U59 location.	0.3
ER2-10	17# 40#	PCH PWR MINI CARD	1212	ShouYi	Change Cap for cost down.	Change C295 & C1785 to SE000000I10.	0.3
ER2-11	29# 41#	VGA DC/DC DC/DC	1212	ShouYi	Change Cap for cost down.	Change C338,C1709,C1771,C1776 to SE000000K80.	0.3
ER2-12	09# 13# 17# 18# 36#		1212	ShouYi	Change Cap for cost down.	Change C210,C211,C212,C215,C234,C235,C240,C244,C257, C262,C283,C286,C271,C277,C278,C279,C284,C324, C525,C580,C1043,C1044,C1589,CC15,CC16,CC17, CC18,CH33,CH34,CH54. SE102104K00 to SE076104K80.	0.3
ER2-13	12#	PCH SATA,HDA,SPI,LPC	1212	ShouYi	For improve S5 power consumption.	Change R199,R198,R200 to Un-stuff.	0.3
ER2-14	16#	PCH GPIO,CPU,MISC	1212	ShouYi	For HW design. (EMI's requirement change USB port)	Change R309 to un-stuff. Add R812, for PCH_GPIO22 pull down. (debug port)	0.3
ER2-15	20#	N13P PEG&DAC	1212	ShouYi	For HW design.	Change R1602 pull up to +3VSG.	0.3
ER2-16	39# 14#	EC ENE KB9012 PCH DMI,FDI,PM	1212	ShouYi	For HW design.	Change R1824 to un-stuff. Change R248 to stuff.	0.3
ER2-17	15#	PCH PCI,USB,NVRAM	1212	ShouYi	For EMI's requirement change the USB port.	Modified the USB port.	0.3
ER2-18	36#	USB2/USB3	1212	ShouYi	For HW design.	Modified the USBAI_PEN#R signals design.	0.3
ER2-19	36#	USB2/USB3	1212	ShouYi	For EMI's requirement change the USB port.	Modified the USB port.	0.3
ER2-20	34#	HDMI	1212	ShouYi	For EMI's requirement.	Reserve C641~C648 for EMI.	0.3
ER2-21	29# 41#	VGA DC/DC DC/DC	1212	ShouYi	For HW design. (single channel MOS change to dual channel)		0.3
ER2-22	30#	LVDS & CRT	1212	ShouYi	For EMI's requirement.	Modified the USB port signals.	0.3
ER2-23	32#	LAN RTL8111F	1212	ShouYi	For HW design. (single channel MOS change to dual channel)	Change the QL53 and QL52 to Q94.	0.3
ER2-24	30#	LVDS & CRT	1214	ShouYi	For EMI's requirement.	Add L9,R126,R1897.	0.3
ER2-25	22#	N13P LVDS&TMDS	1214	ShouYi	For Vendor's requirement.	Modified the X76 BOM for VGA and VRAM.	0.3
ER2-26	38#	KB/TP/FUN	1214	ShouYi	For EMI's requirement.	Add L10,R1912,R127.	0.3

Page 3/3

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				Unit	401967
				Date	Monthly September 2017
				Issue	68 of 68