1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

J117 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
3	0003501996	ENGINEERING RELEASED	2014-12-09

LAST_MODIFIED=Thu Sep 18 13:37:48 2014
LAST_MODIFICATION=Thu Sep 18 13:37:48 2014

DRAWING
TITLE=J16 MLB_IG
ABBREV=DRAWING
LAST_MODIFIED=Thu Sep 18 13:37:48 2014

DRAWING TITLE: SCHEM,MLB,J117

Apple Inc.

DRAWING NUMBER: 051-00081 | SIZE: D
REVISION: 3.0.0
BRANCH:
PAGE: 1 OF 123
SHEET: 1 OF 81

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-00081	1	SCH,MLB,J117	SCH	CRITICAL	
820-00034	1	PCBF,MLB,J117	PCB	CRITICAL	
685-00013	1	PCBA,MLB,J117,COMMON PARTS	CMNPTS		MLB_CMNPTS

Main BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
985-00016	PCBA,MLB,DEV,J117	DEVELOPMENT,J117_DEVEL
939-00158	PCBA,MLB,DEV,J117,CPU_INT	MLB_CMNPTS,ALTERNATE,CPU:SOCKET,DDR3:HYNIX_8GB_1866,SSD:Y
639-00910	PCBA,MLB,J117,HY_8GB_29NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_8GB_1866,SSD:N
639-00911	PCBA,MLB,J117,EL_8GB_25NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_8GB_1866,SSD:N
639-00912	PCBA,MLB,J117,SA_8GB_23NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:SAMSUNG_8GB_1866,SSD:N
639-00913	PCBA,MLB,J117,EL_16GB_25NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_16GB_1866,SSD:N
639-00914	PCBA,MLB,J117,HY_16GB_25NM,HDD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_16GB_1866,SSD:N
639-00713	PCBA,MLB,J117,HY_8GB_29NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_8GB_1866,SSD:Y
639-00714	PCBA,MLB,J117,EL_8GB_25NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_8GB_1866,SSD:Y
639-00715	PCBA,MLB,J117,SA_8GB_23NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:SAMSUNG_8GB_1866,SSD:Y
639-00716	PCBA,MLB,J117,EL_16GB_25NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:ELPIDA_16GB_1866,SSD:Y
639-00717	PCBA,MLB,J117,HY_16GB_25NM,SSD,1866	MLB_CMNPTS,ALTERNATE,CPU:ULT,DDR3:HYNIX_16GB_1866,SSD:Y
685-00013	PCBA,MLB,J117,COMMON PARTS	J117_COMMON

BOM Groups

BOM GROUP	BOM OPTIONS
J117_COMMON	COMMON,ALTERNATE,J117_PROGPARTS,SMCREG:SUP,XDP,SMBUS1:ISOL,USB_OC_ISO:Y,RTCRST:Y,AUDIO_DP_SNS:N
J117_PROGPARTS	SMC:PROG,BOOTROM:PROG,CAMROM:PROG,TBTROM:PROG,ENETROM:PROG
J117_DEVEL	XDP_CONN,TEMPSNSDEV,SAMCONN

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S00101	1	IC,CPU,BDW-ULT,QM3Y,BS,65-82,2/3,1.6,15W,.95,1168	U0500	CRITICAL	CPU:ULT
998-7866	1	INTERPOSER,BGA1168,SINGLE SIDE	U0500	CRITICAL	CPU:SOCKET

ASIC Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1247	1	IC,TBT,FR-4C,A0,PBQ,CIO,SRLJC,FCBGA288	U2800	CRITICAL	
343S0616	1	IC,BCM57766A,CIV+,A0,8x8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S00158	1	IC,EFI,V0108,J117	U5210	CRITICAL	BOOTROM:PROG
335S00006	1	IC,SERIAL FLASH,64MBIT,3V,8P,WSON,QE=1	U5210	CRITICAL	BOOTROM:BLANK
341S00110	1	IC,SMC-B1,EXTERNAL,V2.24A19,POC,J117	U5000	CRITICAL	SMC:PROG
338S1214	1	IC,SMC12-B1,40MHZ/50MIPS,MCU,176BGA	U5000	CRITICAL	SMC:BLANK
341S3778	1	IC,CAMERA,FLASH,V7229,J16	U4202	CRITICAL	CAMROM:PROG
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK
341S00154	1	IC,EPROM,T29,FALCON RIDGE,V27.1,J117	U2890	CRITICAL	TBTROM:PROG
335S0915	1	IC,FLASH,SPI,4MBIT,50MHZ	U2890	CRITICAL	TBTROM:BLANK
341S3912	1	IC,ENET SPI ROM,NVMONYX,V1.15,216/2160/217	U3990	CRITICAL	ENETROM:PROG
335S1025	1	IC,SERIAL FLASH,2MBIT,2.7V,REV F	U3990	CRITICAL	ENETROM:BLANK

Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S00011	377S0155		ALL	USB3 diodes
377S0184	377S0155		ALL	USB3 diodes
377S0124	377S0057		ALL	TVS
155S0578	155S0367		ALL	120OHM EMI BEAD
128S0368	128S0365		ALL	150UF AL POLY
138S0681	138S0638		ALL	Taiyo 10uf 805 alt
197S0479	197S0478		ALL	12 MHz Cam. Xtal
197S0486	197S0478		ALL	12 MHz Cam. Xtal
107S0251	107S0249		ALL	Sense resistor
197S0481	197S0480		ALL	25MHz Xtal
197S0343	197S0480		ALL	25MHz Xtal
138S0860	138S0775		ALL	Single-source 1uF 402
138S0859	138S0788		ALL	Single-source 10uF
378S0391	378S0390		ALL	Debug LEDs
341S00016	341S3912		ALL	ENET ROM,ADESTO,V1.15
138S0747	138S0773		ALL	1uF,X6S,402
197S0542	197S0544		ALL	24 MHz PCH XTal
197S0545	197S0544		ALL	24 MHz PCH XTal
197S0369	197S0392		ALL	32 KHz PCH Xtal
197S0399	197S0392		ALL	32 KHz PCH Xtal
376S0572	376S0659		ALL	Single P-Ch FET
376S0972	376S00075		ALL	Single N-Ch FET
132S00012	132S0401		ALL	0.22uF,X7R,0402
138S00012	138S0771		ALL	1uF,X6S,0402
138S1103	138S0719		ALL	4.7uF,X5R,0402
155S0830	155S0316		ALL	FER BD,600 OHM,0.5A,0603
155S00076	155S0546		ALL	FER BD,600 OHM,300MA,402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1089	376S1128		ALL	Single N-Ch FET
155S0660	155S0513		ALL	220HM EMI BEAD
155S0694	155S0387		ALL	470OHM EMI BEAD
127S0164	127S0162		ALL	1UF 25V TANT
376S00074	376S0855		ALL	Dual N-Ch FET
376S1129	376S0855		ALL	Dual N-Ch FET
376S00074	376S0855	SSD:Y	ALL	Dual N-Ch FET
376S1129	376S0855	SSD:Y	ALL	Dual N-Ch FET
311S0649	311S0541		ALL	Single AND Gate
107S0375	107S00039		ALL	DDR Sense Res
107S00011	107S0372		ALL	CPU VR Sense Res
353S3814	353S3812		ALL	TBT mux
353S4376	353S3384		ALL	HDD OOBV1 comparator
311S00014	311S0515		ALL	TBT JTAG ISOLATION BUFFER
311S00013	311S0508		ALL	Single Buffer Driver OD
371S00019	371S0463		ALL	Rohm Schottky Barrier Diode
376S00037	376S1193		ALL	30V,64A,Single N-Channel FET
376S00036	376S1194		ALL	30V,52A,Single N-channel FET
138S0746	138S0705		ALL	CAP,CER,X5R,10uF,20%,10V,402
152S1757	152S1821		ALL	IND,0.4uH,23A
138S00013	138S0772		ALL	CAP,CER,2.2UF,20%,10V,X6S,402
371S00017	371S0749		ALL	DIODE,SCHOTTKY,30V,1A,SOD-323

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00065	08	CPU,BDW-ULT,2+GT3
338S1247	02	TBT,Falcon Ridge-4c
335S00006	07	IC,SERIAL FLASH,Quad-IO
333S0784	07	32Gb,25nm LPDDR3-1866
333S0786	07	16Gb,29nm LPDDR3-1866
333S0790	07	32Gb,25nm LPDDR3-1866
333S0792	07	16Gb,25nm LPDDR3-1866
333S00004	07	16Gb,23nm LPDDR3-1866

CPU DRAM SPD Straps

BOM GROUP	BOM OPTIONS
DDR3:HYNIX_8GB_1600	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:L,HYNIX_8GB_1600
DDR3:HYNIX_16GB_1600	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,RAMCFG4:L,HYNIX_16GB_1600
DDR3:HYNIX_8GB_1866	RAMCFG0:L,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:H,HYNIX_8GB_1866
DDR3:HYNIX_16GB_1866	RAMCFG0:L,RAMCFG1:L,RAMCFG2:H,RAMCFG3:L,RAMCFG4:H,HYNIX_16GB_1866
DDR3:ELPIDA_8GB_1600	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,RAMCFG4:L,ELPIDA_8GB_1600
DDR3:ELPIDA_16GB_1600	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,RAMCFG4:L,ELPIDA_16GB_1600
DDR3:ELPIDA_8GB_1866	RAMCFG0:H,RAMCFG1:H,RAMCFG2:L,RAMCFG3:L,RAMCFG4:H,ELPIDA_8GB_1866
DDR3:ELPIDA_16GB_1866	RAMCFG0:H,RAMCFG1:H,RAMCFG2:H,RAMCFG3:L,RAMCFG4:H,ELPIDA_16GB_1866
DDR3:SAMSUNG_8GB_1600	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:L,SAMSUNG_8GB_1600
DDR3:SAMSUNG_8GB_1866	RAMCFG0:H,RAMCFG1:L,RAMCFG2:L,RAMCFG3:L,RAMCFG4:H,SAMSUNG_8GB_1866

CPU DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	0	1
N/A	1	0
ELPIDA	1	1

SIZE	CFG 2
8GB	0
16GB	1

DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0783	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_16GB_1600
333S0784	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_16GB_1866
333S0785	4	IC,SDRAM,29nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_8GB_1600
333S0786	4	IC,SDRAM,29nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	HYNIX_8GB_1866
333S0789	4	IC,SDRAM,25nm 32Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_16GB_1600
333S0790	4	IC,SDRAM,25nm 32Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_16GB_1866
333S0791	4	IC,SDRAM,25nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_8GB_1600
333S0792	4	IC,SDRAM,25nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	ELPIDA_8GB_1866
333S00003	4	IC,SDRAM,23nm 16Gb,LPDDR3-1600,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	SAMSUNG_8GB_1600
333S00004	4	IC,SDRAM,23nm 16Gb,LPDDR3-1866,178P FBGA	U2300,U2400,U2500,U2600	CRITICAL	SAMSUNG_8GB_1866

DIE REV	CFG 3
A	0
B	1

SPEED	CFG 4
1600	0
1866	1

SYNC_MASTER=J117_TONY SYNC_DATE=05/05/2014

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

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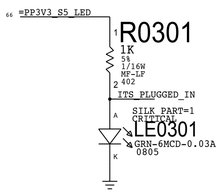
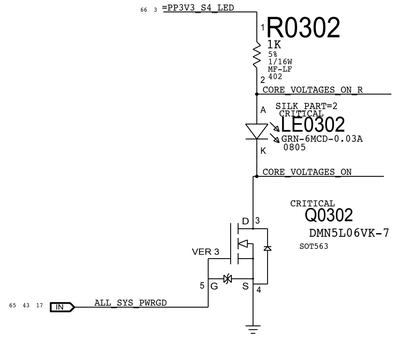
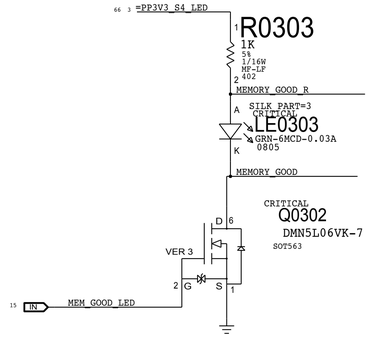
S5 Led



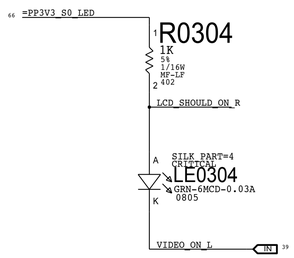
ALL_SYS_PWRGD Led



MEM_GOOD Led



VIDEO ON Led



SYNC_MASTER=J70_GAREN SYNC_DATE=10/22/2013

PAGE TITLE

DEBUG LEDS

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

REVISION 3.0.0

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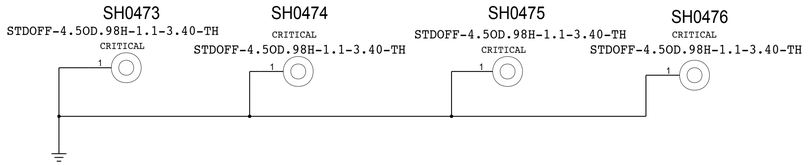
CPU HEATSINK MOUNTING FEATURES

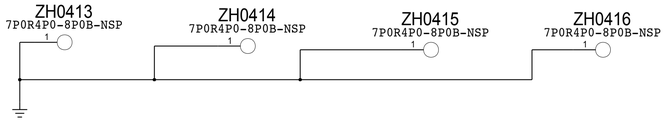


HEATSINK STABILITY MOUNTING FEATURES

APN:860-1532

Rear Cover

APN:998-4559 (Plated holes, 4mm inner diameter, 8mm pad)



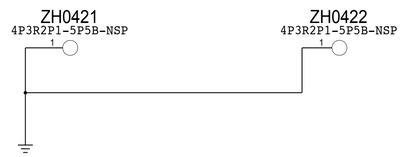
J117 SPRINGS

APN:870-00908 SPRING FINGER 4.2X2.5X5.3

APN:870-00909 SPRING FINGER 4.2X2.5X5.81

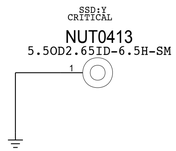
WIRELESS CARD MTG HOLES

APN:998-01406 (Plated holes, 2.1mm inner diameter, 4.3mm top pad, 5.1mm bottom pad)



SSD STANDOFF

APN: 860-00198



SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE: Holes/PD parts

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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DDI Port Assignments:

TBT Sink 0

TBT Sink 1
(MUXed with HDMI
if necessary)

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 1 OF 19

DP_TBTSNK0_ML_C_N<0>	C54	DDI1_TXN0			
DP_TBTSNK0_ML_C_P<0>	C55	DDI1_TXP0			
DP_TBTSNK0_ML_C_N<1>	B58	DDI1_TXN1			
DP_TBTSNK0_ML_C_P<1>	C58	DDI1_TXP1			
DP_TBTSNK0_ML_C_N<2>	B55	DDI1_TXN2			
DP_TBTSNK0_ML_C_P<2>	A55	DDI1_TXP2			
DP_TBTSNK0_ML_C_N<3>	A57	DDI1_TXN3			
DP_TBTSNK0_ML_C_P<3>	B57	DDI1_TXP3			
DP_TBTSNK1_ML_C_N<0>	C51	DDI2_TXN0			
DP_TBTSNK1_ML_C_P<0>	C50	DDI2_TXP0			
DP_TBTSNK1_ML_C_N<1>	C53	DDI2_TXN1			
DP_TBTSNK1_ML_C_P<1>	B54	DDI2_TXP1			
DP_TBTSNK1_ML_C_N<2>	C49	DDI2_TXN2			
DP_TBTSNK1_ML_C_P<2>	B50	DDI2_TXP2			
DP_TBTSNK1_ML_C_N<3>	A53	DDI2_TXN3			
DP_TBTSNK1_ML_C_P<3>	B53	DDI2_TXP3			

DDI / EDP

EDP_TXN0	C45	DP_INT_ML_N<0>	OUT	40 80
EDP_TXP0	B46	DP_INT_ML_P<0>	OUT	40 80
EDP_TXN1	A47	DP_INT_ML_N<1>	OUT	40 80
EDP_TXP1	B47	DP_INT_ML_P<1>	OUT	40 80
EDP_TXN2	C47	DP_INT_ML_N<2>	OUT	40
EDP_TXP2	C46	DP_INT_ML_P<2>	OUT	40
EDP_TXN3	A49	DP_INT_ML_N<3>	OUT	40
EDP_TXP3	B49	DP_INT_ML_P<3>	OUT	40
EDP_AUXN	A45	DP_INT_AUX_N	BI	40 80
EDP_AUXP	B45	DP_INT_AUX_P	BI	40 80
EDP_RCOMP	D20	71 MCP_EDP_RCOMP		
EDP_DISP_UTIL	A43	NC_EDP_DISP_UTIL		

eDP Port Assignment:

Internal panel

PPVCOMP_S0_CPU 8

R0530
24.9
1%
1/20W
MF
201
PLACE_NEAR=U0500.D20:12.7mm

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 17 OF 19

NO_TEST

MCP_DC_AW2_AY2	AY2	DAISY_CHAIN_NCTF			
MCP_DC_AW3_AY3	AY3	DAISY_CHAIN_NCTF			
MCP_DC_AY60	AY60	DAISY_CHAIN_NCTF			
MCP_DC_AW61_AY61	AY61	DAISY_CHAIN_NCTF			
MCP_DC_AW62_AY62	AY62	DAISY_CHAIN_NCTF			
MCP_DC_B2	B2	DAISY_CHAIN_NCTF			
MCP_DC_A3_B3	B3	DAISY_CHAIN_NCTF			
MCP_DC_A61_B61	B61	DAISY_CHAIN_NCTF			
MCP_DC_B62_B63	B62	DAISY_CHAIN_NCTF			
	B63	DAISY_CHAIN_NCTF			
MCP_DC_C1_C2	C1	DAISY_CHAIN_NCTF			
	C2	DAISY_CHAIN_NCTF			

TP0531 (TP-P6)
TP0501 (TP-P6)

NO_TEST

A3	MCP_DC_A3_B3			
A4	MCP_DC_A4	TP	TP-P6	TP0500
A60	MCP_DC_A60	TP	TP-P6	TP0510
A61	MCP_DC_A61_B61			
A62	MCP_DC_A62	TP	TP-P6	TP0511
AV1	MCP_DC_AV1	TP	TP-P6	TP0520
AW1	MCP_DC_AW1	TP	TP-P6	TP0521
AW2	MCP_DC_AW2_AY2			
AW3	MCP_DC_AW3_AY3			
AW61	MCP_DC_AW61_AY61			
AW62	MCP_DC_AW62_AY62			
AW63	MCP_DC_AW63	TP	TP-P6	TP0530

MCP Daisy-Chain Strategy:

Each corner of CPU has two testpoints.
Other corner test signals connected in
daisy-chain fashion. Continuity should
exist between both TP's on each corner.

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 18 OF 19
SPARE

AT2	RSVD	N23	RSVD	NC
AU44	RSVD	R23	RSVD	NC
AV44	RSVD	T23	RSVD	NC
D15	RSVD	U10	RSVD	NC
F22	RSVD	AL1	RSVD	NC
H22	RSVD	AM11	RSVD	NC
J21	RSVD	AP7	RSVD	NC
		AU10	RSVD	NC
		AU15	RSVD	NC
		AW14	RSVD	NC
		AY14	RSVD	NC

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE
CPU GFX/NCTF/RSVD

Apple Inc.

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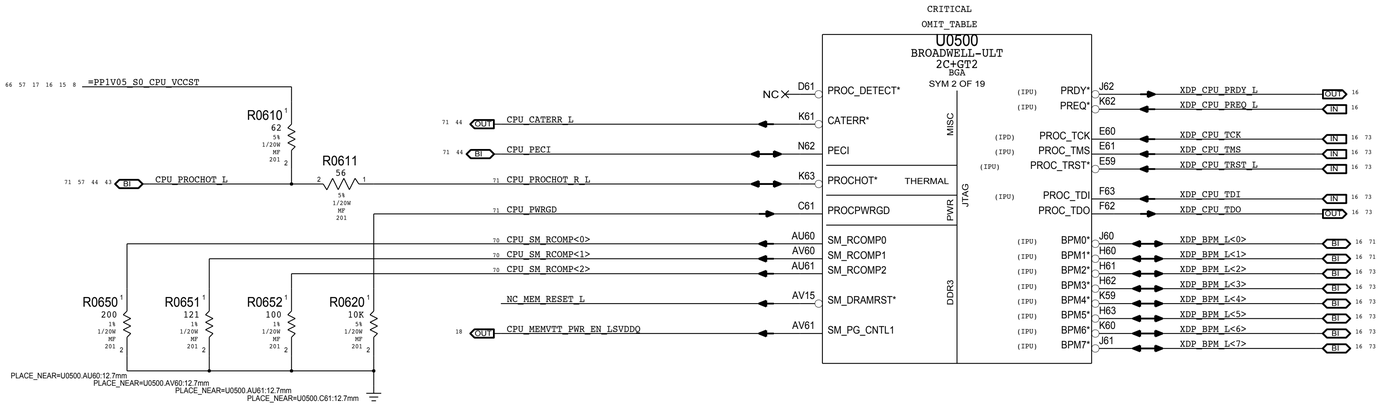
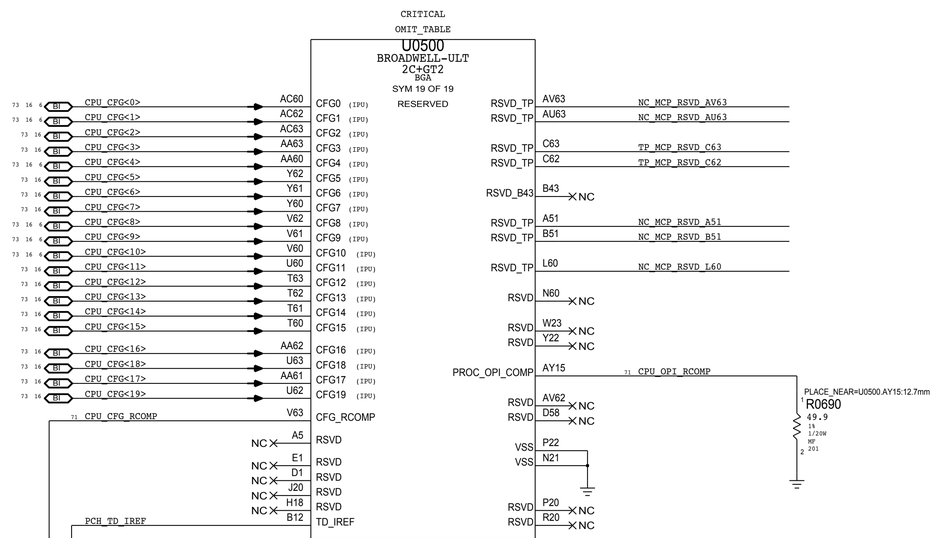
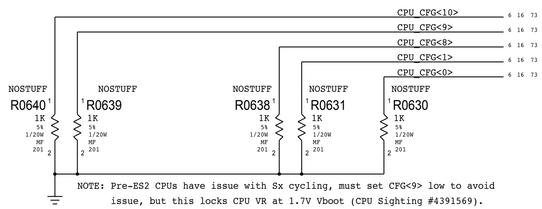


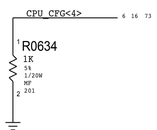


CFG<10>:SAFE MODE BOOT	1 = NORMAL OPERATION	0 = POWER FEATURES NOT ACTIVE	
CFG<9> :NO SVID-CAPABLE VR	1 = VR SUPPORTS SVID	0 = VR DOES NOT SUPPORT SVID	
CFG<8> :ALLOW NOA ON LOCKED UNITS	1 = NORMAL OPERATION	0 = NOA ALWAYS UNLOCKED	
CFG<4> :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED	
CFG<1> :PCH-LESS MODE	1 = NORMAL OPERATION	0 = PCH-LESS MODE	
CFG<0> :RESET SEQUENCE STALL	1 = NORMAL OPERATION	0 = STALL AFTER PCU PLL LOCK	

These can be placed close to J1800
and are only for debug access



NOTE: Pre-ES2 CPUs have issue with Sx cycling, must set CFG<9> low to avoid issue, but this locks CPU VR at 1.7V Vboot (CPU Sighting #4391569).



SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: CPU Misc/JTAG/CFG/RSVD

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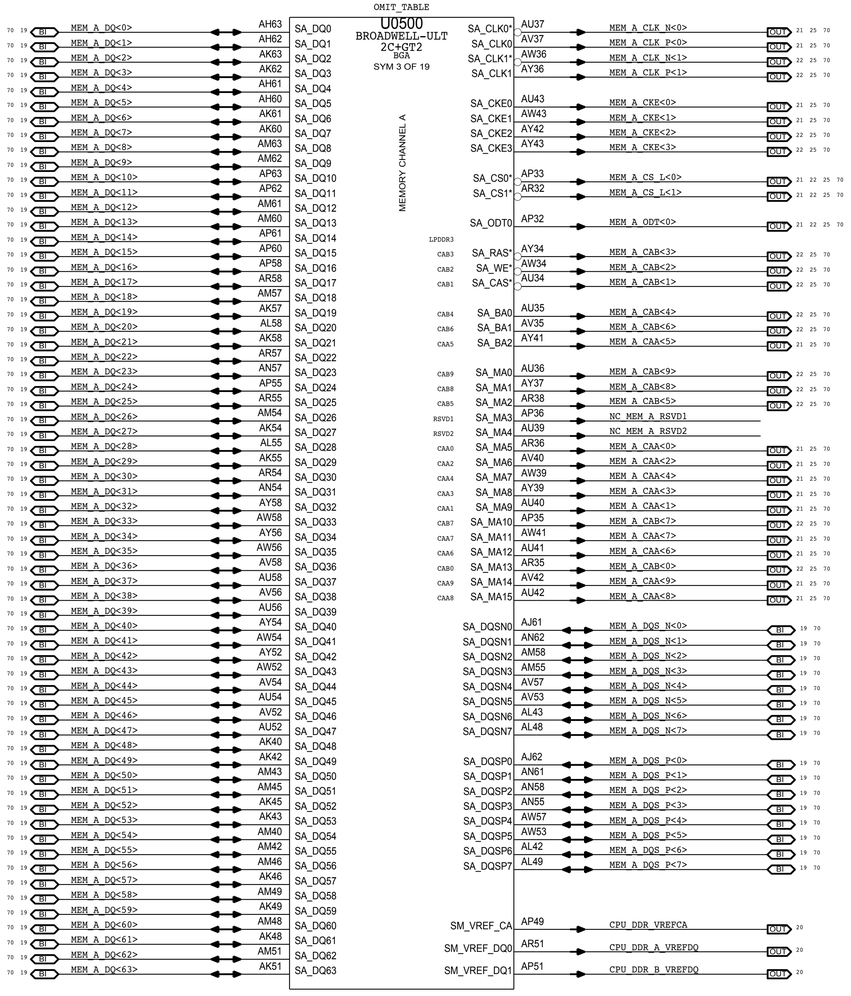

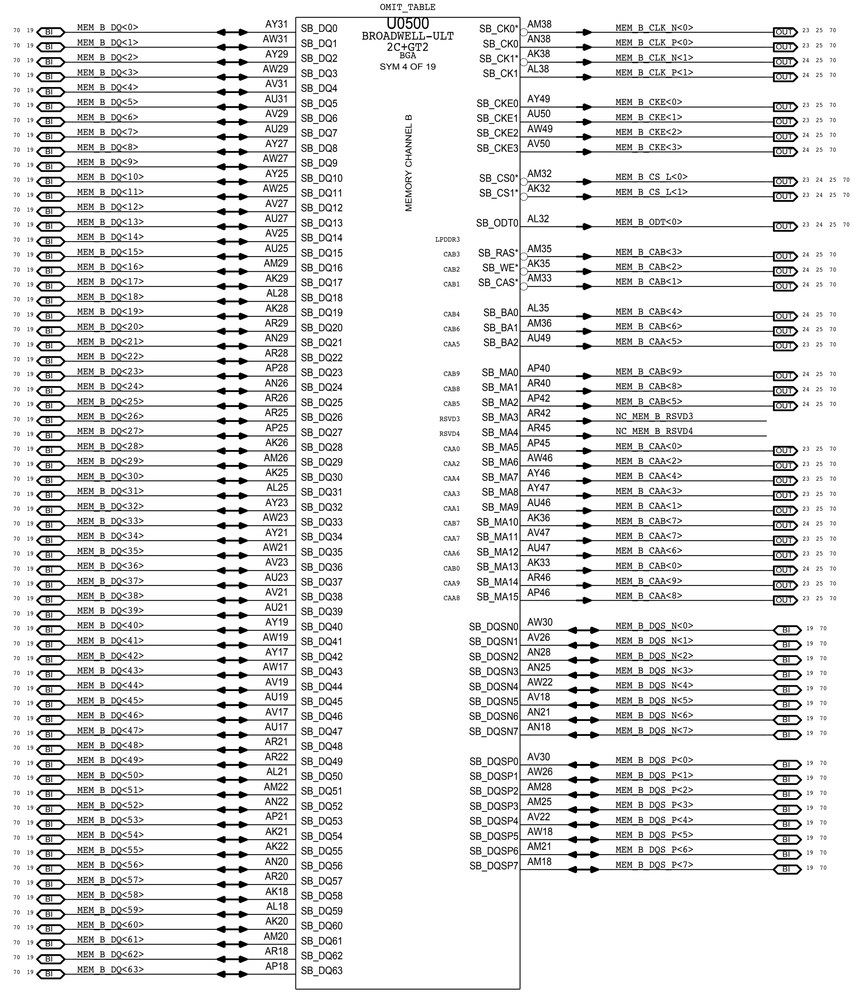

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

CPU DDR3/LPDDR3 Interfaces

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BDW-ULT current estimates from Broadwell Mobile ULT Processor EDS vol 1, doc #514405, v1.5.
WPT-LP current estimates from Wildcat Point-LP PCH EDS, doc #515621, v1.0.
Numbers may not be accurate values as of 08/26/2014

CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
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HSW ULT POWER

=PPVMEMIO_S0_CPU
1.4A Max (DDR3: 1.5-1.35V)
1.1A Max (LPDDR3: 1.2V)

=PPVCC_S0_CPU
32A Max

=PP1V05_S0_CPU_VCCST
R0800 75 1% 1/20W MF 201
R0802 130 1% 1/20W MF 201
Max load: 300mA
Max load: 300mA
R0810 43 5% 1/20W MF 201
R0811 0 5% 1/20W MF 0201
R0812 0 5% 1/20W MF 0201
CPU_VIDALERT_L
CPU_VIDSCLK
CPU_VIDSOUT
R0802.2: PLACE_NEAR=U0500.L63:6.35mm
R0810.2: PLACE_NEAR=U0500.L62:38.1mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm

R0860 100 5% 1/20W MF 201
PLACE_NEAR=U0500.C50:50.8mm
CPU_VCCSENSE_P
PPVCCIO_S0_CPU
PPVCOMP_S0_CPU
NOTE: Aliases not used on CPU supply outputs to avoid any extraneous connections.

L59	RSVD	
J58	RSVD	
AH26	VDDQ	
AJ31	VDDQ	
AJ33	VDDQ	
AJ37	VDDQ	
AN33	VDDQ	
AP43	VDDQ	
AR48	VDDQ	
AY35	VDDQ	
AY40	VDDQ	
AY44	VDDQ	
AY50	VDDQ	
F59	VCC	
N58	RSVD	
AC58	RSVD	
E63	VCC_SENSE	
AB23	RSVD	
A59	VCCIO_OUT	
E20	VCCIOA_OUT	
AD23	RSVD	
AA23	RSVD	
AE59	RSVD	
L62	VIDALERT*	CPU_VIDALERT_R_L
N63	VIDSCLK	CPU_VIDSCLK_R
L63	VIDSOUT	CPU_VIDSOUT_R
B59	VCCST_PWRGD	CPU_VCCST_PWRGD
F60	VR_EN	CPU_VR_EN
C59	VR_READY	CPU_VR_READY
D63	VSS	
H59	PWR_DEBUG*	CPU_PWR_DEBUG
P62	VSS	
P60	RSVD_TP	NC_CPU_RSVD_P60
P61	RSVD_TP	NC_CPU_RSVD_P61
N59	RSVD_TP	NC_CPU_RSVD_N59
N61	RSVD_TP	TP_CPU_RSVD_N61
T59	RSVD	
AD60	RSVD	
AD59	RSVD	
AA59	RSVD	
AE60	RSVD	
AC59	RSVD	
AG58	RSVD	
U59	RSVD	
V59	RSVD	
AC22	VCCST	
AE22	VCCST	
AE23	VCCST	
AB57	VCC	
AD57	VCC	
AG57	VCC	
C24	VCC	
C28	VCC	
C32	VCC	

C36	VCC	=PPVCC_S0_CPU
C40	VCC	
C44	VCC	
C48	VCC	
C52	VCC	
C56	VCC	
E23	VCC	
E25	VCC	
E27	VCC	
E29	VCC	
E31	VCC	
E33	VCC	
E35	VCC	
E37	VCC	
E39	VCC	
E41	VCC	
E43	VCC	
E45	VCC	
E47	VCC	
E49	VCC	
E51	VCC	
E53	VCC	
E55	VCC	
E57	VCC	
F24	VCC	
F28	VCC	
F32	VCC	
F36	VCC	
F40	VCC	
F44	VCC	
F48	VCC	
F52	VCC	
F56	VCC	
G23	VCC	
G25	VCC	
G27	VCC	
G29	VCC	
G31	VCC	
G33	VCC	
G35	VCC	
G37	VCC	
G39	VCC	
G41	VCC	
G43	VCC	
G45	VCC	
G47	VCC	
G49	VCC	
G51	VCC	
G53	VCC	
G55	VCC	
G57	VCC	
H23	VCC	
J23	VCC	
K23	VCC	
K57	VCC	
L22	VCC	
M23	VCC	
M57	VCC	
P57	VCC	
U57	VCC	
W57	VCC	

=PP1V05_S0_CPU_VCCST
???mA Max
=PPVRTC_G3_PCH
C0892 0.1UF 20% 10V CERM 402
C0891 0.1UF 20% 10V CERM 402
C0890 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG10:6.35mm
BYPASS=U0500.AG10:6.35mm
BYPASS=U0500.AG10:6.35mm

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OMIT_TABLE
U0500
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LPT LP POWER

=PP1V05_S0_PCH_VCCHSIO	K9	VCCHSIO	HSIO	VCCSUS3_3	=PP3V3_SUS_PCH_VCCSUS_RTC
1838mA Max	L10	VCCHSIO			0.3mA Max[1]
	M9	VCCHSIO		VCCRTC	=PPVRTC_G3_PCH
=PP1V05_S0_PCH_VCCIO_HSIO	N8	VCC1_05	RTC	DCPRTC	PPVOUT_S0_PCH_DCPRTC
29mA Max[1]	P9	VCC1_05			MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.05V
PP1V05_S0_PCH_VCCUSB3PLL	B18	VCCUSB3PLL	SPI	VCCSPI	=PP3V3_SUS_PCH_VCC_SPI
41mA Max					18mA Max
PP1V05_S0_PCH_VCCSATA3PLL	B11	VCCSATA3PLL		VCCASW	=PP1V05_S0_PCH_VCCASW
42mA Max				VCCASW	185mA Max[1]
WF: RSVD on Sawtooth Peak rev 1.0	Y20	VCCAPLL	OPI		
PP1V05_S0_PCH_VCCAPLL_OPI	AA21	VCCAPLL		VCC1P05	=PP1V05_S0_PCH_VCC
57mA Max	W21	VCCAPLL		VCC1P05	1499mA Max[1]
	J13	DCPSUS3	USB3	VCC1P05	
				VCC1P05	
				VCC1P05	
=PP1V5_S0_PCH_VCCSUSHDA	AH14	VCCHDA	AZALIA/HDA	DCPSUSBYP	PPVOUT_S5_PCH_DCPSUSBYP_R
11mA Max				DCPSUSBYP	MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.05V
	AH13	DCPSUS2	VRM/USB2/AZALIA		Powered in DeepSx
=PP3V3_SUS_PCH_VCCSUS_GPIO	AC9	VCCSUS3_3	CORE	VCCASW	=PP1V05_S0_PCH_VCCASW
59mA Max[1]	AA9	VCCSUS3_3		VCCASW	473mA Max[1]
				VCCASW	
=PP3V3_S5_PCH_VCCDSW	AH10	VCCDSW3_3	GPIO/LCC	DCPSUS1	NC
114mA Max				DCPSUS1	NC
=PP3V3_S0_PCH_VCC3_3_GPIO	V8	VCC3_3			
40mA Max[1]	W9	VCC3_3			
			THERMAL SENSOR	VCCTS1_5	=PP1V5_S0_PCH_VCCTS
					3mA Max
PP1V05_S0_PCH_VCC_ICC	J18	VCCCLK	ICC	VCC3_3	=PP3V3_S0_PCH_VCCTS
VCCCLK: 200mA Max	K19	VCCCLK		VCC3_3	1mA Max[1]
PP1V05_S0_PCH_VCCACLKPLL	A20	VCCACLKPLL	SERIAL IO		
31mA Max				VCCSDIO	=PP3V3_S0_PCH_VCCSDIO
=PP1V05_S0_PCH_VCCCLK	J17	VCCCLK		VCCSDIO	17mA Max
VCCCLK: 200mA Max	R21	VCCCLK			
	T21	VCCCLK	SUS OSCILLATOR		
WF: RSVD on Sawtooth Peak rev 1.0	K18	RSVD		DCPSUS4	NC
	M20	RSVD			
	V21	RSVD		RSVD	NC WF: RSVD on Sawtooth Peak rev 1.0
=PP3V3_SUS_PCH_VCCSUS_ICC	AE20	VCCSUS3_3	USB2		
3.3mA Max[1]	AE21	VCCSUS3_3		VCC1_05	=PP1V05_S0_PCH_VCCIO_USB2
				VCC1_05	213mA Max[1]

C0895 0.1UF 10% 6.3V CERM-X5R 0201

PLACE_NEAR=U0500.AG19:2.54mm
R0899 5.11 1% 1/20W MF-LF 201
PPVOUT_S5_PCH_DCPSUSBYP
C0899 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG19:2.54mm

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SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014
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A11	VSS	VSS	AJ35
A14	VSS	VSS	AJ39
A18	VSS	VSS	AJ41
A24	VSS	VSS	AJ43
A28	VSS	VSS	AJ45
A32	VSS	VSS	AJ47
A36	VSS	VSS	AJ50
A40	VSS	VSS	AJ52
A44	VSS	VSS	AJ54
A48	VSS	VSS	AJ56
A52	VSS	VSS	AJ58
A56	VSS	VSS	AJ60
AA1	VSS	VSS	AJ63
AA58	VSS	VSS	AK23
AB10	VSS	VSS	AK3
AB20	VSS	VSS	AK52
AB22	VSS	VSS	AL10
AB7	VSS	VSS	AL13
AC61	VSS	VSS	AL17
AD21	VSS	VSS	AL20
AD3	VSS	VSS	AL22
AD63	VSS	VSS	AL23
AE10	VSS	VSS	AL26
AE5	VSS	VSS	AL29
AE58	VSS	VSS	AL31
AF11	VSS	VSS	AL33
AF12	VSS	VSS	AL36
AF14	VSS	VSS	AL39
AF15	VSS	VSS	AL40
AF17	VSS	VSS	AL45
AF18	VSS	VSS	AL46
AG1	VSS	VSS	AL51
AG11	VSS	VSS	AL52
AG21	VSS	VSS	AL54
AG23	VSS	VSS	AL57
AG60	VSS	VSS	AL60
AG61	VSS	VSS	AL61
AG62	VSS	VSS	AM1
AG63	VSS	VSS	AM17
AH17	VSS	VSS	AM23
AH19	VSS	VSS	AM31
AH20	VSS	VSS	AM52
AH22	VSS	VSS	AN17
AH24	VSS	VSS	AN23
AH28	VSS	VSS	AN31
AH30	VSS	VSS	AN32
AH32	VSS	VSS	AN35
AH34	VSS	VSS	AN36
AH36	VSS	VSS	AN39
AH38	VSS	VSS	AN40
AH40	VSS	VSS	AN42
AH42	VSS	VSS	AN43
AH44	VSS	VSS	AN45
AH49	VSS	VSS	AN46
AH51	VSS	VSS	AN48
AH53	VSS	VSS	AN49
AH55	VSS	VSS	AN51
AH57	VSS	VSS	AN52
AJ13	VSS	VSS	AN60
AJ14	VSS	VSS	AN63
AJ23	VSS	VSS	AN7
AJ25	VSS	VSS	AP10
AJ27	VSS	VSS	AP17
AJ29	VSS	VSS	AP20

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
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AP22	VSS	VSS	AV59
AP23	VSS	VSS	AV8
AP26	VSS	VSS	AW16
AP29	VSS	VSS	AW24
AP3	VSS	VSS	AW33
AP31	VSS	VSS	AW35
AP38	VSS	VSS	AW37
AP39	VSS	VSS	AW4
AP48	VSS	VSS	AW40
AP52	VSS	VSS	AW42
AP54	VSS	VSS	AW44
AP57	VSS	VSS	AW47
AR11	VSS	VSS	AW50
AR15	VSS	VSS	AW51
AR17	VSS	VSS	AW59
AR23	VSS	VSS	AW60
AR31	VSS	VSS	AY11
AR33	VSS	VSS	AY16
AR39	VSS	VSS	AY18
AR43	VSS	VSS	AY22
AR49	VSS	VSS	AY24
AR5	VSS	VSS	AY26
AR52	VSS	VSS	AY30
AT13	VSS	VSS	AY33
AT35	VSS	VSS	AY4
AT37	VSS	VSS	AY51
AT40	VSS	VSS	AY53
AT42	VSS	VSS	AY57
AT43	VSS	VSS	AY59
AT46	VSS	VSS	AY6
AT49	VSS	VSS	B20
AT61	VSS	VSS	B24
AT62	VSS	VSS	B26
AT63	VSS	VSS	B28
AU1	VSS	VSS	B32
AU16	VSS	VSS	B36
AU18	VSS	VSS	B4
AU20	VSS	VSS	B40
AU22	VSS	VSS	B44
AU24	VSS	VSS	B48
AU26	VSS	VSS	B52
AU28	VSS	VSS	B56
AU30	VSS	VSS	B60
AU33	VSS	VSS	C11
AU51	VSS	VSS	C14
AU53	VSS	VSS	C18
AU55	VSS	VSS	C20
AU57	VSS	VSS	C25
AU59	VSS	VSS	C27
AV14	VSS	VSS	C38
AV16	VSS	VSS	C39
AV20	VSS	VSS	C57
AV24	VSS	VSS	D12
AV28	VSS	VSS	D14
AV33	VSS	VSS	D18
AV34	VSS	VSS	D2
AV36	VSS	VSS	D21
AV39	VSS	VSS	D23
AV41	VSS	VSS	D25
AV43	VSS	VSS	D26
AV46	VSS	VSS	D27
AV49	VSS	VSS	D29
AV51	VSS	VSS	D30
AV55	VSS	VSS	D31

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
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D33	VSS	VSS	H17
D34	VSS	VSS	H57
D35	VSS	VSS	J10
D37	VSS	VSS	J22
D38	VSS	VSS	J59
D39	VSS	VSS	J63
D41	VSS	VSS	K1
D42	VSS	VSS	K12
D43	VSS	VSS	L13
D45	VSS	VSS	L15
D46	VSS	VSS	L17
D47	VSS	VSS	L18
D49	VSS	VSS	L20
D5	VSS	VSS	L58
D50	VSS	VSS	L61
D51	VSS	VSS	L7
D53	VSS	VSS	M22
D54	VSS	VSS	N10
D55	VSS	VSS	N3
D57	VSS	VSS	P59
D59	VSS	VSS	P63
D62	VSS	VSS	R10
D8	VSS	VSS	R22
E11	VSS	VSS	R8
E17	VSS	VSS	T1
F20	VSS	VSS	T58
F26	VSS	VSS	U20
F30	VSS	VSS	U22
F34	VSS	VSS	U61
F38	VSS	VSS	U9
F42	VSS	VSS	V10
F46	VSS	VSS	V3
F50	VSS	VSS	V7
F54	VSS	VSS	W20
F58	VSS	VSS	W22
F61	VSS	VSS	Y10
G18	VSS	VSS	Y59
G22	VSS	VSS	Y63
G3	VSS		
G5	VSS	VSS	V58
G6	VSS	VSS	AH46
G8	VSS	VSS	V23
H13	VSS	VSS_SENSE	E62
		VSS	AH16

CPU_VCCSENSE_N → OUT 97 78

R0960
100
5%
1/20W
MF
201
2

PLACE_NEAR=U0500.E62:50.8mm

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

CPU/PCH GROUNDS

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All Intel recommendations from Intel doc #503160 Shark Bay Ultrabook Platform Power Delivery Design Guide Rev 1.0 unless stated otherwise

CPU VCC Decoupling

Intel recommendation (Table 5-1): 23x 22uF 0805 stuff, 7x 22uF 0805 nostuff
Apple implementation : 18x 10uF 0402 mirrored stuff, 1x 470uF stuff, 50x 10uF mirrored no stuff, 50x 10uF single sided no stuff
J70 implementation : 18x 10uF 0402 mirrored stuff, 32x 10uF single sided no stuff

66 8 =PPVCC_S0_CPU

CRITICAL C105A 10UF 20% 6.3V CERM 0402
CRITICAL C105B 10UF 20% 6.3V CERM 0402
CRITICAL C105D 10UF 20% 6.3V CERM 0402
CRITICAL C107C 10UF 20% 6.3V CERM 0402
CRITICAL C107D 10UF 20% 6.3V CERM 0402
CRITICAL C104A 10UF 20% 6.3V CERM 0402
CRITICAL C104B 10UF 20% 6.3V CERM 0402
CRITICAL C104C 10UF 20% 6.3V CERM 0402
CRITICAL C104D 10UF 20% 6.3V CERM 0402
CRITICAL C104E 10UF 20% 6.3V CERM 0402
CRITICAL C104F 10UF 20% 6.3V CERM 0402
CRITICAL C108A 10UF 20% 6.3V CERM 0402
CRITICAL C108C 10UF 20% 6.3V CERM 0402
CRITICAL C108D 10UF 20% 6.3V CERM 0402
CRITICAL C1060 10UF 20% 6.3V CERM 0402
CRITICAL C1061 10UF 20% 6.3V CERM 0402
CRITICAL C1062 10UF 20% 6.3V CERM 0402
CRITICAL C1063 10UF 20% 6.3V CERM 0402

These caps are on the top side.

CRITICAL C1076 10UF 20% 6.3V CERM 0402
CRITICAL C1077 10UF 20% 6.3V CERM 0402
CRITICAL C107A 10UF 20% 6.3V CERM 0402
CRITICAL C107B 10UF 20% 6.3V CERM 0402
CRITICAL C105E 10UF 20% 6.3V CERM 0402
CRITICAL C105F 10UF 20% 6.3V CERM 0402
CRITICAL C106A 10UF 20% 6.3V CERM 0402
CRITICAL C106B 10UF 20% 6.3V CERM 0402
CRITICAL C106C 10UF 20% 6.3V CERM 0402
CRITICAL C106D 10UF 20% 6.3V CERM 0402
CRITICAL C106E 10UF 20% 6.3V CERM 0402
CRITICAL C107E 10UF 20% 6.3V CERM 0402
CRITICAL C107F 10UF 20% 6.3V CERM 0402
CRITICAL C108B 10UF 20% 6.3V CERM 0402
CRITICAL C1064 10UF 20% 6.3V CERM 0402
CRITICAL C1065 10UF 20% 6.3V CERM 0402
CRITICAL C1066 10UF 20% 6.3V CERM 0402
CRITICAL C1067 10UF 20% 6.3V CERM 0402

These caps are on the bottom side.

These caps are mirrored top and bottom.

CRITICAL C1030 1UF 10% 10V X6S-CERM 0402
CRITICAL C105C 1UF 10% 10V X6S-CERM 0402
CRITICAL C1070 1UF 10% 10V X6S-CERM 0402
CRITICAL C1071 1UF 10% 10V X6S-CERM 0402
CRITICAL C1072 1UF 10% 10V X6S-CERM 0402
CRITICAL C1078 1UF 10% 10V X6S-CERM 0402
CRITICAL C1079 1UF 10% 10V X6S-CERM 0402
CRITICAL C1080 1UF 10% 10V X6S-CERM 0402
CRITICAL C1081 1UF 10% 10V X6S-CERM 0402
CRITICAL C1082 1UF 10% 10V X6S-CERM 0402
CRITICAL C1083 1UF 10% 10V X6S-CERM 0402
CRITICAL C1084 1UF 10% 10V X6S-CERM 0402
CRITICAL C1085 1UF 10% 10V X6S-CERM 0402
CRITICAL C1086 1UF 10% 10V X6S-CERM 0402
CRITICAL C1087 1UF 10% 10V X6S-CERM 0402
CRITICAL C1091 1UF 10% 10V X6S-CERM 0402
CRITICAL C1092 1UF 10% 10V X6S-CERM 0402
CRITICAL C1093 1UF 10% 10V X6S-CERM 0402
CRITICAL C1094 1UF 10% 10V X6S-CERM 0402
CRITICAL C1095 1UF 10% 10V X6S-CERM 0402
CRITICAL C1096 1UF 10% 10V X6S-CERM 0402
CRITICAL C1097 1UF 10% 10V X6S-CERM 0402

These caps are beneath the CPU.

CPU VDDQ DECOUPLING

Intel recommendation (Table 5-4): 4x 2.2uF 0402, 6x 10uF 0603
Apple implementation : 4x 2.2uF 0402, 6x 10uF 0402, 6x 10uF no stuff, 1x 270 uF Bulk

66 8 =PPVMEMIO_S0_CPU

CRITICAL C1040 2.2UF 20% 10V X6S-CERM 0402
CRITICAL C1042 2.2UF 20% 10V X6S-CERM 0402
CRITICAL C1043 2.2UF 20% 10V X6S-CERM 0402
CRITICAL C1050 10UF 20% 4V X6S 0402
CRITICAL C1051 10UF 20% 4V X6S 0402
CRITICAL NO STUFF C109A 10UF 20% 4V X6S 0402
CRITICAL C1054 10UF 20% 4V X6S 0402
CRITICAL C1055 10UF 20% 4V X6S 0402

These caps are on the bottom side.

NO STUFF CRITICAL C109E 10UF 20% 6.3V CERM-X5R 0402-1
NO STUFF CRITICAL C109D 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1053 10UF 20% 6.3V CERM-X5R 0402-1
NO STUFF CRITICAL C109C 10UF 20% 6.3V CERM-X5R 0402-1

These caps are on the bottom side.

CRITICAL C1041 2.2UF 20% 10V X6S-CERM 0402

These caps are on the top side.

NO STUFF CRITICAL C109F 10UF 20% 6.3V CERM-X5R 0402-1
NO STUFF CRITICAL C109B 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1052 10UF 20% 6.3V CERM-X5R 0402-1
NO STUFF CRITICAL C1099 10UF 20% 6.3V CERM-X5R 0402-1

These caps are on the top side.

These caps are mirrored top and bottom.

CRITICAL C1056 270UF-0.006OHM 20% 2V TANT CASE-D2

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: CPU Decoupling

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D
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BRANCH:
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PCH VCCDSW3_3 BYPASS
(PCH 3.3V DSW PWR)
66 8 =PP3V3_S5_PCH_VCCDSW
NO STUFF
C1200 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH10::6.35mm

PCH VCCSPI BYPASS
(PCH 3.3V SPI PWR)
66 14 8 =PP3V3_SUS_PCH_VCC_SPI
NO STUFF
C1202 0.1UF 20% 10V CERM 402
BYPASS=U0500.Y8::6.35mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND PWR)
66 8 =PP3V3_SUS_PCH_VCCSUS_GPIO
C1204 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.AC9::12.7mm

PCH VCCSUS3_3 BYPASS
(PCH 3.3V SUSPEND RTC PWR)
66 8 =PP3V3_SUS_PCH_VCCSUS_RTC
C1206 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH11::6.35mm

PCH VCCSDIO BYPASS
(PCH 3.3V SDIO PWR)
66 8 =PP3V3_S0_PCH_VCCSDIO
C1208 1UF 10% 6.3V CERM 402
BYPASS=U0500.U8::6.35mm

PCH VCCSUSHDA BYPASS
(PCH 1.5V HDA PWR)
66 17 8 =PP1V5_S0_PCH_VCCSUSHDA
C1210 1UF 10% 6.3V CERM 402
BYPASS=U0500.AH14::6.35mm

PCH VCC3_3 BYPASS
(PCH 3.3V GPIO/LPC PWR)
66 8 =PP3V3_S0_PCH_VCC3_3_GPIO
C1212 22UF 20% 6.3V X5R-CERM-1 603
BYPASS=U0500.V8::12.7mm

PCH VCC3_3 BYPASS
(PCH 3.3V THERMAL PWR)
66 8 =PP3V3_S0_PCH_VCCTS
C1214 0.1UF 20% 10V CERM 402
BYPASS=U0500.K14::6.35mm

PCH VCCASW BYPASS
(PCH 1.05V ME CORE PWR)
66 8 =PP1V05_S0_PCH_VCCASW
NO STUFF
C1250 22UF 20% 6.3V X5R-CERM-1 603
C1251 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG9::12.7mm
BYPASS=U0500.AE9::6.35mm

PCH VCC BYPASS
(PCH 1.05V CORE PWR)
66 8 =PP1V05_S0_PCH_VCC
C1255 10UF 20% 6.3V CERM-X5R 0402-1
C1256 1UF 10% 6.3V CERM 402
C1257 1UF 10% 6.3V CERM 402
BYPASS=U0500.J11::12.7mm
BYPASS=U0500.J11::6.35mm
BYPASS=U0500.AE8::6.35mm

PCH VCCHSIO BYPASS
(PCH 1.05V PCIe/SATA/USB3 PWR)
66 8 =PP1V05_S0_PCH_VCCHSIO
C1260 1UF 10% 6.3V CERM 402
C1261 1UF 10% 6.3V CERM 402
C1262 10UF 20% 6.3V CERM-X5R 0402-1
BYPASS=U0500.K9::6.35mm
BYPASS=U0500.L10::6.35mm
BYPASS=U0500.M9::6.35mm

PCH VCCIO BYPASS
(PCH 1.05V USB2 PWR)
66 8 =PP1V05_S0_PCH_VCCIO_USB2
C1264 1UF 10% 6.3V CERM 402
BYPASS=U0500.AG16::6.35mm

PCH VCCCLK BYPASS
(PCH 1.05V CLK PWR)
66 8 =PP1V05_S0_PCH_VCCCLK
C1266 1UF 10% 6.3V CERM 402
C1267 1UF 10% 6.3V CERM 402
BYPASS=U0500.J17::6.35mm
BYPASS=U0500.R21::6.35mm

66 =PP1V05_S0_PCH_PLLFILTERS
R1270 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCCACLKPLL_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.05V
CRITICAL
L1270 2.2UH-240MA-0.221OHM 0603
PCH VCCACLKPLL FILTER/BYPASS
(PCH 1.05V ACLK PLL PWR)
PP1V05_S0_PCH_VCCACLKPLL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
8 12
31mA Max
C1270 47UF 20% 4V CERM-X5R 0805-1
C1271 47UF 20% 4V CERM-X5R 0805-1
C1272 1UF 10% 10V X5R 402-1
BYPASS=U0500.A20::12.7mm
BYPASS=U0500.A20::12.7mm
BYPASS=U0500.A20::6.35mm

R1275 0 5% 1/16W MF-LF 402
PP1V05_S0_PCH_VCC_ICC_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.05V
CRITICAL
L1275 2.2UH-240MA-0.221OHM 0603
PCH VCCCLK FILTER/BYPASS
(PCH 1.05V VCCCLK PWR)
PP1V05_S0_PCH_VCC_ICC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
8
??mA Max
C1275 47UF 20% 4V CERM-X5R 0805-1
C1276 47UF 20% 4V CERM-X5R 0805-1
C1277 1UF 10% 10V X5R 402-1
BYPASS=U0500.J18::12.7mm
BYPASS=U0500.J18::12.7mm
BYPASS=U0500.J18::6.35mm

R1280 0 5% 1/16W MF-LF 402
CRITICAL
NO STUFF
L1280 2.2UH-240MA-0.221OHM 0603
PCH OPI VCCAPLL FILTER/BYPASS
(PCH 1.05V OPI PLL PWR)
PP1V05_S0_PCH_VCCAPLL_OPI
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
8
57mA Max
NO STUFF C1280 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1281 47UF 20% 4V CERM-X5R 0805-1
C1282 1UF 10% 10V X5R 402-1
BYPASS=U0500.AA21::12.7mm
BYPASS=U0500.AA21::12.7mm
BYPASS=U0500.AA21::6.35mm

66 =PP1V05_S0_PCH_VCCPLL_HSIO
83mA Max
CRITICAL
L1290 2.2UH-240MA-0.221OHM 0603
PCH VCCSATA3PLL FILTER/BYPASS
(PCH 1.05V SATA3 PLL PWR)
PP1V05_S0_PCH_VCCSATA3PLL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
8 12
42mA Max
C1290 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1291 47UF 20% 4V CERM-X5R 0805-1
C1292 1UF 10% 10V X5R 402-1
BYPASS=U0500.B11::12.7mm
BYPASS=U0500.B11::12.7mm
BYPASS=U0500.B11::6.35mm

CRITICAL
L1295 2.2UH-240MA-0.221OHM 0603
PCH VCCUSB3PLL FILTER/BYPASS
(PCH 1.05V USB3 PLL PWR)
PP1V05_S0_PCH_VCCUSB3PLL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0750
VOLTAGE=1.05V
8 14
41mA Max
C1295 47UF 20% 4V CERM-X5R 0805-1
NO STUFF C1296 47UF 20% 4V CERM-X5R 0805-1
C1297 1UF 10% 10V X5R 402-1
BYPASS=U0500.B18::12.7mm
BYPASS=U0500.B18::12.7mm
BYPASS=U0500.B18::6.35mm

WPT-LP current estimates from Wildcat Point-LP PCH EDS, doc #515621, v1.0
These numbers may not be accurate as of 08/26/2014

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014
PAGE TITLE
PCH Decoupling
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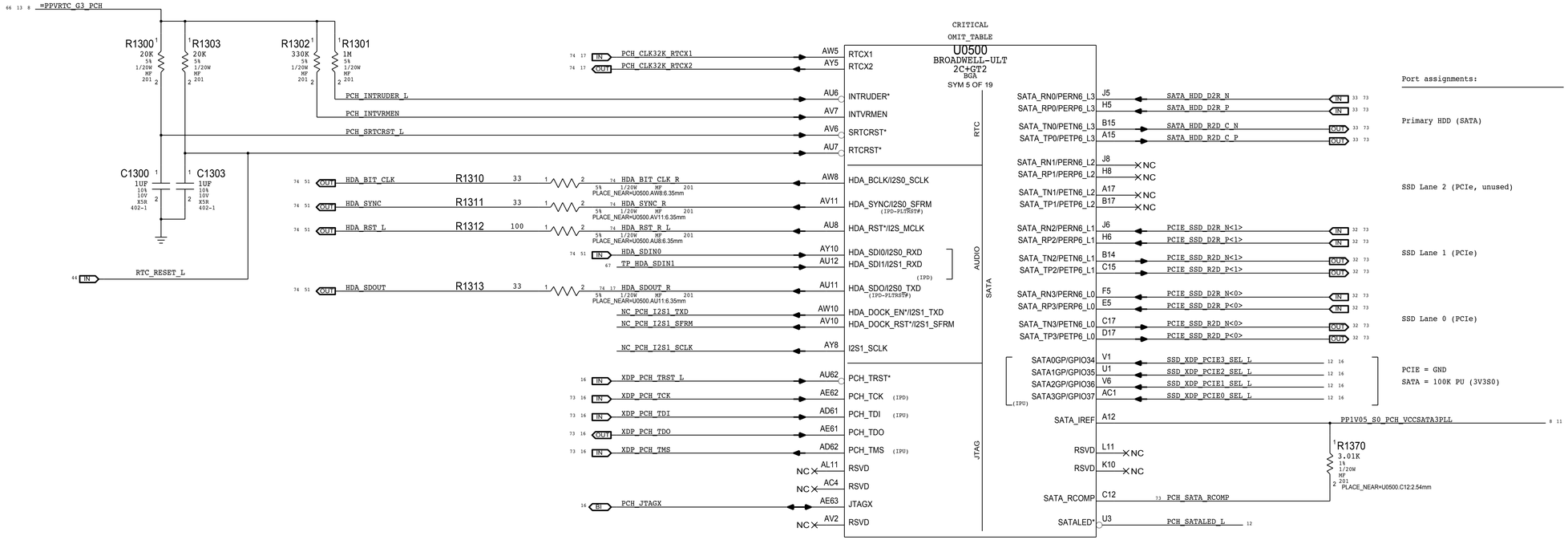
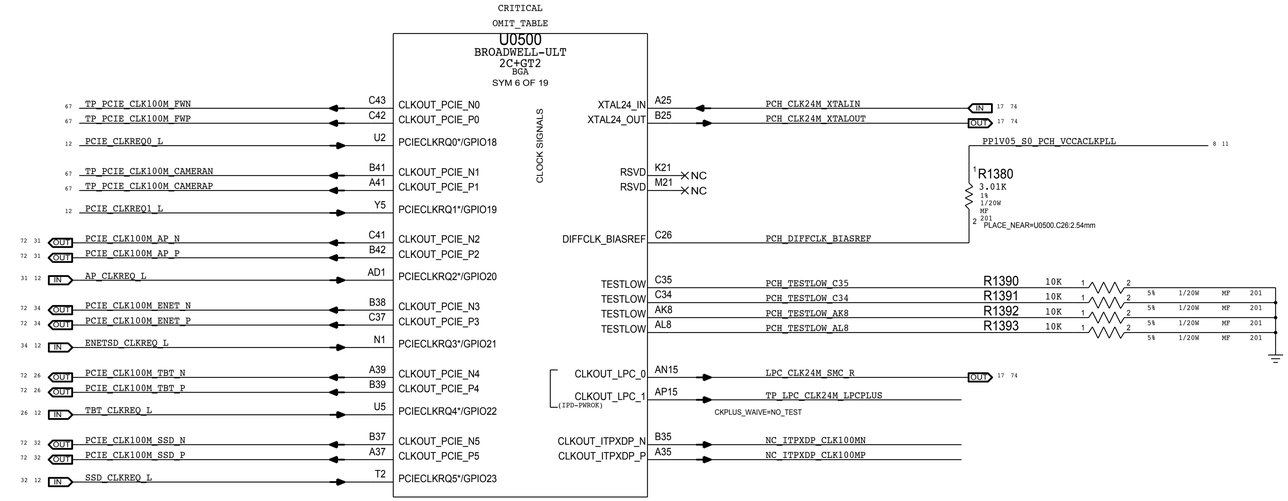
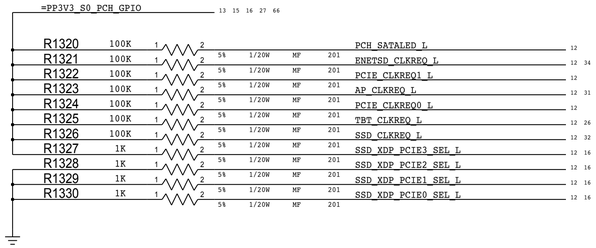


NOTE: Haswell ULT requires that CLQREQ_n be mapped to ROOT_PORT_n+1 to properly support CLKREQs for PCIE devices.





SYNC_MASTER=J117_TONY SYNC_DATE=05/05/2014

PAGE TITLE

PCH Audio/JTAG/SATA/CLK

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

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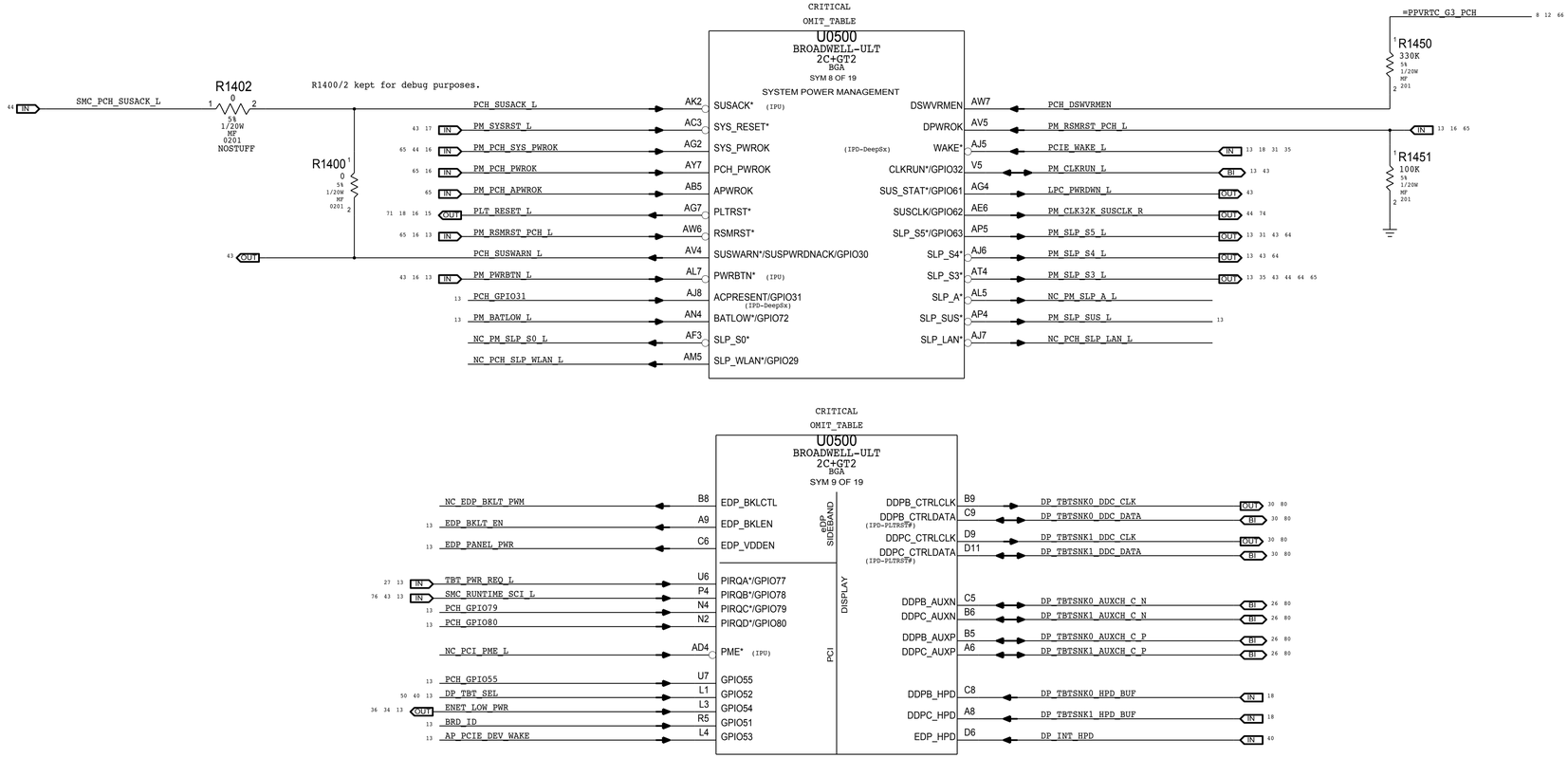

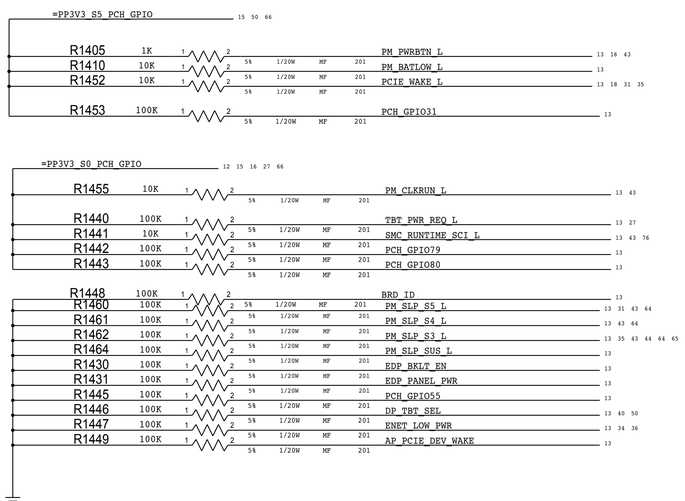

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

PCH PM/PCI/GFX

Apple Inc.

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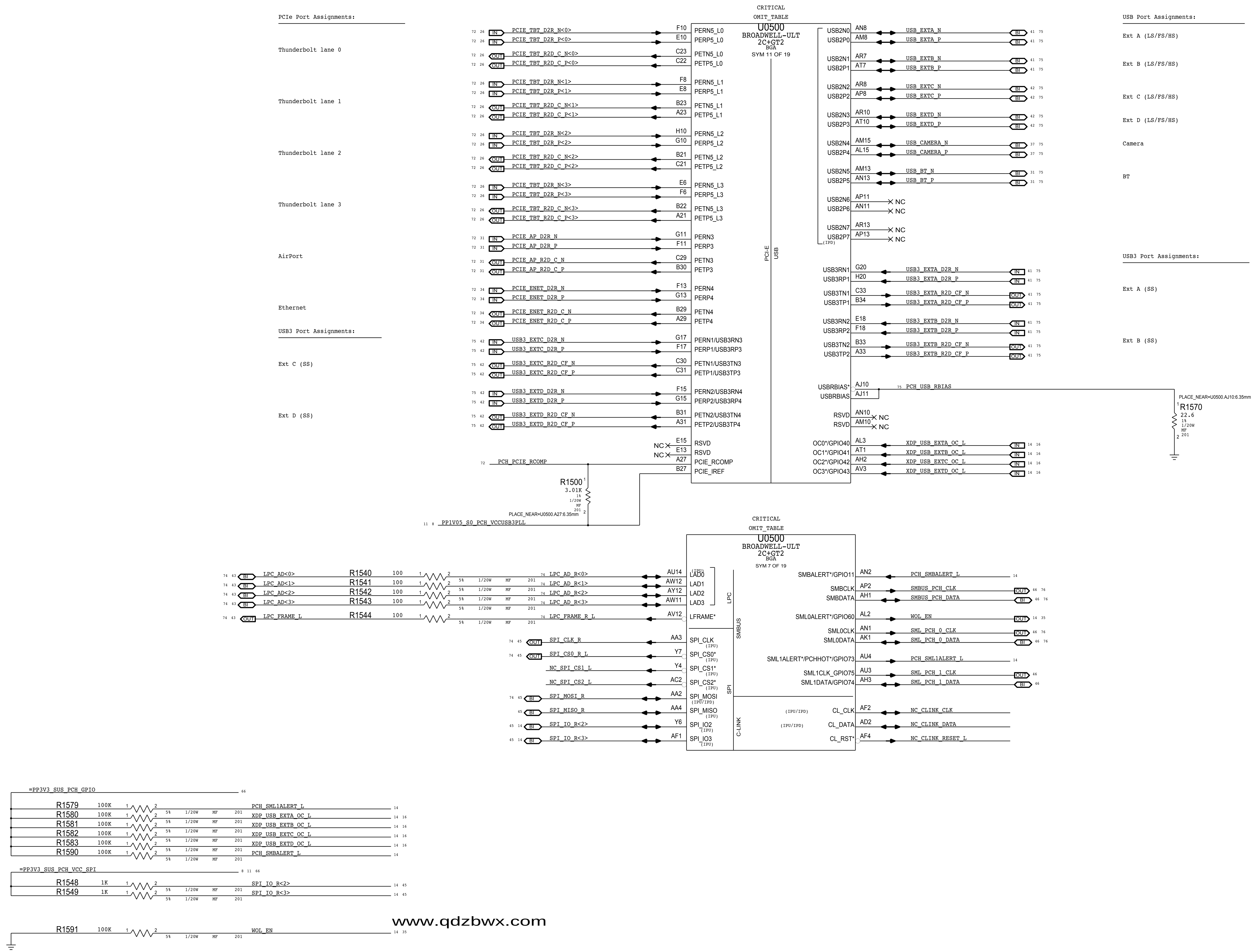

PCIe Port Assignments:
Thunderbolt lane 0
Thunderbolt lane 1
Thunderbolt lane 2
Thunderbolt lane 3
AirPort
Ethernet
USB3 Port Assignments:
Ext C (SS)
Ext D (SS)
CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 11 OF 19
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_C_P<3>
PCIE_AP_D2R_N
PCIE_AP_D2R_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_C_P
PCIE_ENET_D2R_N
PCIE_ENET_D2R_P
PCIE_ENET_R2D_C_N
PCIE_ENET_R2D_C_P
USB3_EXTC_D2R_N
USB3_EXTC_D2R_P
USB3_EXTC_R2D_CF_N
USB3_EXTC_R2D_CF_P
USB3_EXTD_D2R_N
USB3_EXTD_D2R_P
USB3_EXTD_R2D_CF_N
USB3_EXTD_R2D_CF_P
PCH_PCIE_RCOMP
PERN5_L0
PERP5_L0
PETN5_L0
PETP5_L0
PERN5_L1
PERP5_L1
PETN5_L1
PETP5_L1
PERN5_L2
PERP5_L2
PETN5_L2
PETP5_L2
PERN5_L3
PERP5_L3
PETN5_L3
PETP5_L3
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN1/USB3RN3
PERP1/USB3RP3
PETN1/USB3TN3
PETP1/USB3TP3
PERN2/USB3RN4
PERP2/USB3RP4
PETN2/USB3TN4
PETP2/USB3TP4
RSVD
RSVD
PCIE_RCOMP
PCIE_IREF
PCI-E
USB
R1500
3.01K
PLACE_NEAR=U0500.A27:6.35mm
PP1V05_S0_PCH_VCCUSB3PLL
USB2N0
USB2P0
USB2N1
USB2P1
USB2N2
USB2P2
USB2N3
USB2P3
USB2N4
USB2P4
USB2N5
USB2P5
USB2N6
USB2P6
USB2N7
USB2P7
USB3RN1
USB3RP1
USB3TN1
USB3TP1
USB3RN2
USB3RP2
USB3TN2
USB3TP2
USBRBIAS*
USBRBIAS
RSVD
RSVD
OC0*/GPIO40
OC1*/GPIO41
OC2*/GPIO42
OC3*/GPIO43
NC
USB_EXTA_N
USB_EXTA_P
USB_EXTB_N
USB_EXTB_P
USB_EXTC_N
USB_EXTC_P
USB_EXTD_N
USB_EXTD_P
USB_CAMERA_N
USB_CAMERA_P
USB_BT_N
USB_BT_P
USB3_EXTA_D2R_N
USB3_EXTA_D2R_P
USB3_EXTA_R2D_CF_N
USB3_EXTA_R2D_CF_P
USB3_EXTB_D2R_N
USB3_EXTB_D2R_P
USB3_EXTB_R2D_CF_N
USB3_EXTB_R2D_CF_P
PCH_USB_RBIAS
PLACE_NEAR=U0500.AJ10:6.35mm
R1570
22.6
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L
USB Port Assignments:
Ext A (LS/FS/HS)
Ext B (LS/FS/HS)
Ext C (LS/FS/HS)
Ext D (LS/FS/HS)
Camera
BT
USB3 Port Assignments:
Ext A (SS)
Ext B (SS)
CRITICAL
OMIT_TABLE
U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 7 OF 19
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_FRAME_L
R1540
R1541
R1542
R1543
R1544
100
LPC_AD_R<0>
LPC_AD_R<1>
LPC_AD_R<2>
LPC_AD_R<3>
LPC_FRAME_R_L
SPI_CLK_R
SPI_CS0_R_L
NC_SPI_CS1_L
NC_SPI_CS2_L
SPI_MOSI_R
SPI_MISO_R
SPI_IO_R<2>
SPI_IO_R<3>
LAD0
LAD1
LAD2
LAD3
LFRAME*
SPI_CLK
SPI_CS0*
SPI_CS1*
SPI_CS2*
SPI_MOSI
SPI_MISO
SPI_IO2
SPI_IO3
LPC
SMBUS
SPI
C-LINK
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO73
SML1CLK_GPIO75
SML1DATA/GPIO74
CL_CLK
CL_DATA
CL_RST*
PCH_SMBALERT_L
SMBUS_PCH_CLK
SMBUS_PCH_DATA
WOL_EN
SML_PCH_0_CLK
SML_PCH_0_DATA
PCH_SML1ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
NC_CLINK_CLK
NC_CLINK_DATA
NC_CLINK_RESET_L
=PP3V3_SUS_PCH_GPIO
R1579
R1580
R1581
R1582
R1583
R1590
100K
PCH_SML1ALERT_L
XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L
PCH_SMBALERT_L
=PP3V3_SUS_PCH_VCC_SPI
R1548
R1549
1K
SPI_IO_R<2>
SPI_IO_R<3>
R1591
100K
WOL_EN

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

PCH PCIe/USB/LPC/SPI/SMBus

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

REVISION 3.0.0

BRANCH

GPIO12:

CR: TBT_GO2SX_BIDIR, requires 100k pull-up to SUS
RR/FR: DPHDMIMUX_SEL_TBT, requires 100k pull-up to TBTLC

Required JTAG pullups are on the XDP connector page.

CRITICAL
OMIT_TABLE

U0500
BROADWELL-ULT
2C+GT2
BGA
SYM 10 OF 19

P1	BMBUSY*/GPIO76	MLB_RAMCFG4	BI
AU2	GPIO8	MLB_RAMCFG0	BI
AM7	LAN_PHY_PWR_CTRL/GPIO12	HDMITBTMUX_SEL_TBT	BI
AD6	GPIO15 (IPD-RSMRST#)	NC_MEM_VDD_SEL_1V5_L (NO_TEST=1)	
Y1	GPIO16	XDP_LPCPLUS_GPIO	IN
T3	GPIO17	XDP_PCH_GPIO17	IN
AD5	GPIO24	ENET_SD_RESET_L	
AN5	GPIO27 (IPD-DeepSx)	SMC_WAKE_SCI_L	IN
AD7	GPIO28	TPAD_SPI_INT_L	
AN3	GPIO26	ENET_MEDIA_SENSE	IN
AG6	GPIO56	SSD_PWR_EN	OUT
AP1	GPIO57	PCH_TBT_PCIE_RESET_L	
AL4	GPIO58	HDD_PWR_EN	OUT
AT5	GPIO59	XDP_SDCONN_STATE_CHANGE_L	BI
AK4	GPIO44	SD_PWR_EN	
AB6	GPIO47	TBT_PWR_EN	OUT
U4	GPIO48	XDP_JTAG_ISP_TCK	OUT
Y3	GPIO49	XDP_JTAG_ISP_TDI	OUT
P3	GPIO50	JTAG_TBT_TMS_PCH	OUT
Y2	HSIOPC/GPIO71	PCH_HSIO_PWR_EN	
AT3	GPIO13	TPAD_SPI_IF_EN	
AH4	GPIO14	MLB_RAMCFG3	BI
AM4	GPIO25	SPIROM_USE_MLB	BI
AG5	GPIO45	SSD_RESET_L	
AG3	GPIO46	SSD_SR_EN_L	OUT
AM3	GPIO9	MLB_RAMCFG1	BI
AM2	GPIO10	MLB_RAMCFG2	BI
P2	DEVSLP0/GPIO33	PCH_GPIO33	
C4	SDIO_POWER_EN/GPIO70	AP_S0IX_WAKE_SEL	
L2	DEVSLP1/GPIO38	PCH_GPIO38	
N5	DEVSLP2/GPIO39	PCH_GPIO39	
V2	SPKR/GPIO81 (IPD-PLTRST#)	PCH_TCO_TIMER_DISABLE	

CPU/MISC

D60	THERMTRIP*	PM_THRMTRIP_L	OUT
V4	RCIN*/GPIO82	TBT_CIO_PLUG_EVENT_L	IN
T4	SERIRQ	LPC_SERIRQ	BI
AW15	PCH_OPI_COMP	PCH_OPI_COMP	
AF20	RSVD	NC	
AB21	RSVD	NC	

GPIO
LPIO

R6	GSPI0_CS*/GPIO83	MEM_GOOD_LED	OUT
L6	GSPI0_CLK/GPIO84	PCH_CAM_RESET_L	OUT
N6	GSPI0_MISO/GPIO85 (IPD)	PCH_CAM_EXT_BOOT	OUT
L8	GSPI0_MOSI/GPIO86 (IPD-PLTRST#)	AUD_SPI_MOSI	
R7	GSPI1_CS*/GPIO87	PCH_GSPI1_CS_L	
L5	GSPI1_CLK/GPIO88	SDCONN_OC_L	IN
N7	GSPI1_MISO/GPIO89 (IPD)	PCH_GSPI1_MISO	
K2	GSPI_MOSI/GPIO90	PCH_GSPI1_MOSI	
J1	UART0_RXD/GPIO91	AP_S0IX_WAKE_L	
K3	UART0_TXD/GPIO92	HDMITBTMUX_FLAG_L	
J2	UART0_RTS*/GPIO93	PCH_BT_UART_RTS_L	
G1	UART0_CTS*/GPIO94	PCH_BT_UART_CTS_L	
K4	UART1_RXD/GPIO0	PCH_UART1_RXD	
G2	UART1_TXD/GPIO1	PCH_UART1_TXD	
J3	UART1_RST*/GPIO2	JTAG_ISP_TDO	IN
J4	UART1_CTS*/GPIO3	PCH_UART1_CTS_L	
F2	I2C0_SDA/GPIO4	PCH_GPIO4	
F3	I2C0_SCL/GPIO5	AP_RESET_L	
G4	I2C1_SDA/GPIO6	PCH_I2C1_SDA	
F1	I2C1_SCL/GPIO7	PCH_I2C1_SCL	
E3	SDIO_CLK/GPIO64	TBT_POC_RESET_L	OUT
F4	SDIO_CMD/GPIO65	BT_PWR_RST_L	
D3	SDIO_D0/GPIO66 (IPD-PLTRST#)	PCH_STRP_TOPBLK_SWP_L	IN
E4	SDIO_D1/GPIO67	PCH_GPIO67	
C3	SDIO_D2/GPIO68	LCD_IRQ_L	
E2	SDIO_D3/GPIO69	LCD_PSR_EN	

66 57 17 16 8 6 =PP1V05_S0_CPU_VCCST

R1600 1K 5% 1/20W MF 201

Pull-up/down on chipset support page (depends on TBT controller)
Cactus Ridge: Alias to TBT_CIO_PLUG_EVENT, requires pull-down.
Redwood Ridge: Alias to TBT_CIO_PLUG_EVENT_L, requires pull-up (S0).

R1601 49.9 1% 1/20W MF 201 — PLACE_NEAR=U0500.AW15:12.7mm

R1602 100K 5% 1/20W MF 201 — PLT_RESET_L

Pull-up on TBT page

Requires connection to SMC via 1K series R

71 18 16 15 13 PLT_RESET_L

R1606 100K 5% 1/20W MF 201 — 36 ENET_SD_RESET_L

R1603 100K 5% 1/20W MF 201 — 26 PCH_TBT_PCIE_RESET_L

R1604 1K 5% 1/20W MF 201 — 32 SSD_RESET_L

R1605 1K 5% 1/20W MF 201 — 66 27 16 15 13 12 =PP3V3_S0_PCH_GPIO — PCH_TCO_TIMER_DISABLE

=PP3V3_S5_PCH_GPIO 13 50 66
=PP3V3_S4_PCH_GPIO 18 41 42 66
=PP3V3_S0_PCH_GPIO 12 13 15 16 27 66

R1628	100K	PCH_GPIO38	15
R1624	100K	JTAG_TBT_TMS_PCH	15 18
R1634	100K	JTAG_ISP_TDO	15 18
R1609	100K	TBT_CIO_PLUG_EVENT_L	15 26
R1611	100K	XDP_LPCPLUS_GPIO	15 16
R1618	100K	HDD_PWR_EN	15 63
R1621	100K	TBT_PWR_EN	15 26
R1625	100K	PCH_HSIO_PWR_EN	15
R1630	100K	PCH_GPIO33	15
R1632	100K	PCH_GPIO39	15
R1633	10K	LPC_SERIRQ	15 43
R1635	100K	BT_PWR_RST_L	15
R1637	100K	LCD_IRQ_L	15
R1617	100K	SSD_PWR_EN	15 63
R1629	100K	SSD_SR_EN_L	15 32
R1615	100K	TPAD_SPI_INT_L	15
R1619	100K	XDP_SDCONN_STATE_CHANGE_L	15 16
R1620	100K	SD_PWR_EN	15
R1614	100K	SMC_WAKE_SCI_L	15 43 76
R1613	100K	SPIROM_USE_MLB	15 45 74
R1616	100K	PCH_GPIO67	15
R1612	100K	XDP_PCH_GPIO17	15 16
R1622	100K	XDP_JTAG_ISP_TCK	15 16 18
R1623	100K	XDP_JTAG_ISP_TDI	15 16 18
R1626	100K	TPAD_SPI_IF_EN	15
R1631	100K	AP_S0IX_WAKE_SEL	15
R1636	100K	ENET_MEDIA_SENSE	15 34 75
R1638	100K	LCD_PSR_EN	15

TBTLC for CR, S0 for RR

RAM Configuration Straps

For chip-down RAM systems

66 27 16 15 13 12 =PP3V3_S0_PCH_GPIO

	RAMCFG4:H	RAMCFG3:H	RAMCFG2:H	RAMCFG1:H	RAMCFG0:H
	R1688	R1680	R1681	R1682	R1683
	100K 5% 1/20W MF 201	100K 5% 1/20W MF 201	100K 5% 1/20W MF 201	100K 5% 1/20W MF 201	100K 5% 1/20W MF 201
16 15	MLB_RAMCFG0				
16 15	MLB_RAMCFG1				
16 15	MLB_RAMCFG2				
16 15	MLB_RAMCFG3				
16 15	MLB_RAMCFG4				
	RAMCFG4:L	RAMCFG3:L	RAMCFG2:L	RAMCFG1:L	RAMCFG0:L
	R1689	R1684	R1685	R1686	R1687
	10K 5% 1/20W MF 201	10K 5% 1/20W MF 201	10K 5% 1/20W MF 201	10K 5% 1/20W MF 201	10K 5% 1/20W MF 201

66 27 16 15 13 12 =PP3V3_S0_PCH_GPIO

15	AP_S0IX_WAKE_L	R1658	100K 5% 1/20W MF 201
15	HDMITBTMUX_FLAG_L	R1659	100K 5% 1/20W MF 201
15	PCH_I2C1_SDA	R1666	100K 5% 1/20W MF 201
15	PCH_I2C1_SCL	R1667	100K 5% 1/20W MF 201
15	PCH_UART1_TXD	R1661	47K 5% 1/20W MF 201
15	PCH_GSPI1_CS_L	R1654	47K 5% 1/20W MF 201
15	PCH_GSPI1_MOSI	R1653	47K 5% 1/20W MF 201
15	PCH_GPIO4	R1664	47K 5% 1/20W MF 201
16 15	SDCONN_OC_L	R1651	47K 5% 1/20W MF 201
15	AUD_SPI_MOSI	R1657	100K 5% 1/20W MF 201
15 3	MEM_GOOD_LED	R1650	100K 5% 1/20W MF 201
38 15	PCH_CAM_RESET_L NOSTUFF	R1668	100K 5% 1/20W MF 201
38 15	PCH_CAM_EXT_BOOT NOSTUFF	R1669	100K 5% 1/20W MF 201
15	PCH_BT_UART_RTS_L	R1670	47K 5% 1/20W MF 201
15	PCH_BT_UART_CTS_L	R1671	47K 5% 1/20W MF 201
15	PCH_UART1_RXD	R1660	47K 5% 1/20W MF 201
15	PCH_UART1_CTS_L	R1663	47K 5% 1/20W MF 201
15	PCH_GSPI1_MISO	R1652	47K 5% 1/20W MF 201

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

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PCH GPIO/MISC/LPIO

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

CPU Micro2-XDP

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

PPVCCIO_S0_CPU
=PP1V05_S0_XDP → R1832 150 5% 1/16W MF-LF 402
OMIT XW1800 SHORT 402
OMIT XW1801 SHORT 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1

XDP_CPU_PREQ_L	OBSFN_A0	OBSFN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSFN_A1	OBSFN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSFN_B0	OBSFN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSFN_B1	OBSFN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>
XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
XDP_CPU_OBSAB	VCC_OBS_AB	VCC_OBS_CD	XDP_CPU_OBSCD
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_CPU_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_CPU_TRST_L
TP_XDP_TCK1	TCK1	TDI	XDP_CPU_TDI
XDP_CPU_TCK	TCK0	TMS	XDP_CPU_TMS
		XDP_PRESENT#	

518S0847

XDP_CPU_PRESENT_L

XDP C1800 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.48:28mm
XDP C1804 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.48:28mm
XDP R1831 1K 5% 1/16W MF-LF 402 — PLACE_NEAR=U0500.AA63:50mm
XDP C1801 0.1UF 10% 6.3V CERM-X5R 0201
XDP C1806 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.47:28mm

CPU_VCCST_PWRGD → R1800 1K 5% 1/20W MF 201 → XDP_CPU_VCCST_PWRGD — PLACE_NEAR=U0500.C61:12.7mm
PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201 → XDP_CPU_PWRBTN_L — PLACE_NEAR=U5000.J3:12.7mm
PM_PCH_SYS_PWROK → R1804 220 5% 1/16W MF-LF 402 → XDP_SYS_PWROK

R1805 1K 5% 1/20W MF 201 — PLT_RESET_L — PLACE_NEAR=U0500.AG7:12.7mm

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

=PP1V05_S0_CPU_VCCST
XDP_CPU_TDO → R1810 51 5% 1/20W MF 201 — PLACE_NEAR=J1800.51:28mm
XDP_CPU_TRST_L → R1811 51 5% 1/20W MF 201 — PLACE_NEAR=U0500.E59:28mm
XDP_CPU_TCK → R1813 51 5% 1/20W MF 201 — PLACE_NEAR=U0500.E60:28mm

TDI and TMS are terminated in CPU.

1.05V S5 LDO

Power to the JTAG debug lines

=PP3V3_S5_PWRCTL
XDP C1830 0.1UF 10% 16V X7R-CERM 0402
XDP R1833 150 5% 1/16W MF-LF 402
PM_EN_REG_P1V05_S5
XDP C1832 0.1UF 10% 6.3V CERM-X5R 0201

U1830
TPS720105
SON
BIAS (4) — CRITICAL XDP
IN (6)
EN (3)
OUT (1) → PP1V05_S5
NC (2) → NC
GND (5)
THRM PAD (7)

XDP C1831 2.2UF 10% 6.3V X5R 402

MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500

PP1V05_S5
R1890 51 1% 1/20W MF 201 XDP
R1891 51 1% 1/20W MF 201 XDP
R1892 51 1% 1/20W MF 201 XDP
NOSTUFF R1899 1K 1% 1/20W MF 201 XDP

XDP_PCH_TDO
XDP_PCH_TDI
XDP_PCH_TMS
XDP_PCH_JTAGX

XDP_PCH_TCK → R1896 51 NOSTUFF — PLACE_NEAR=U0500.AE62:28mm
XDP_PCH_TRST_L → R1897 51 NOSTUFF — PLACE_NEAR=U0500.AU62:28mm

R1881 1K 5% 1/20W MF 201 — PM_PCH_PWROK
R1882 0 5% 1/20W MF 0201 NOSTUFF — XDP_PCH_TRST_L

PCH_JTAGX → R1835 0 5% 1/20W MF 0201 XDP → PCH_JTAGX_R → TP1888
PLACE_NEAR=J1800.58:28mm

PCH Micro2-XDP

=PP3V3_S5_XDP

CRITICAL
XDP_CONN
J1850
DF40RC-60DP-0.4V
M-ST-SM1

OMIT XW1850 SHORT 402

	OBSFN_A0	OBSFN_C0	XDP_MLB_RAMCFG0
	OBSFN_A1	OBSFN_C1	XDP_JTAG_ISP_TCK
XDP_USB_EXTA_OC_L	OBSDATA_A0	OBSDATA_C0	SSD_XDP_PCIE3_SEL_L
XDP_USB_EXTB_OC_L	OBSDATA_A1	OBSDATA_C1	SSD_XDP_PCIE2_SEL_L
XDP_USB_EXTC_OC_L	OBSDATA_A2	OBSDATA_C2	SSD_XDP_PCIE1_SEL_L
XDP_USB_EXTD_OC_L	OBSDATA_A3	OBSDATA_C3	SSD_XDP_PCIE0_SEL_L
	OBSFN_B0	OBSFN_D0	
	OBSFN_B1	OBSFN_D1	
XDP_SDCONN_STATE_CHANGE_L	OBSDATA_B0	OBSDATA_D0	XDP_LPCPLUS_GPIO
XDP_MLB_RAMCFG1	OBSDATA_B1	OBSDATA_D1	XDP_PCH_GPIO17
XDP_MLB_RAMCFG2	OBSDATA_B2	OBSDATA_D2	XDP_MLB_RAMCFG4
XDP_MLB_RAMCFG3	OBSDATA_B3	OBSDATA_D3	XDP_JTAG_ISP_TDI
PM_RSMRST_PCH_L → R1883 1K 5% 1/20W MF 201 → XDP_PM_RSMRST_PCH_L	HOOK0	HOOK4	=PP1V05_S0_XDP
XDP_CPU_PWRBTN_L	HOOK1	HOOK5	
XDP_PCH_OBSAB	VCC_OBS_AB	VCC_OBS_CD	=PP3V3_S0_PCH_GPIO
	HOOK2	HOOK6	XDP_PM_PCH_PWROK
	HOOK3	HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_PCH_TRST_L_R
	TCK1	TDI	XDP_PCH_TDI
XDP_PCH_TCK	TCK0	TMS	XDP_PCH_TMS

XDP C1850 0.1UF 10% 6.3V CERM-X5R 0201
XDP C1851 0.1UF 10% 6.3V CERM-X5R 0201
XDP C1852 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1850.47:28mm

PCH XDP Signals

These signals do not connect to XDP connector in this architecture, only accessible via Top-Side Probe. Nets are listed here to show XDP associations and to make clear what restrictions exist on PCH GPIOs when Top-Side Probe is used for PCH debug.

PCH/XDP Signals	Non-XDP Signals
XDP_USB_EXTA_OC_L	USB_EXTA_OC_L
XDP_USB_EXTB_OC_L	USB_EXTB_OC_L
XDP_USB_EXTC_OC_L	USB_EXTC_OC_L
XDP_USB_EXTD_OC_L	USB_EXTD_OC_L
XDP_MLB_RAMCFG0	MLB_RAMCFG0
XDP_MLB_RAMCFG1	MLB_RAMCFG1
XDP_MLB_RAMCFG2	MLB_RAMCFG2
XDP_MLB_RAMCFG3	MLB_RAMCFG3
XDP_MLB_RAMCFG4	MLB_RAMCFG4
XDP_SDCONN_STATE_CHANGE_L	SDCONN_STATE_CHANGE_L

MAKE_BASE=TRUE

MLB_RAMCFGx GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

SDCONN_STATE_CHANGE_L is aliased, do not plug/unplug SD Cards during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

NOTE: Should force PCH GPIO47 high to ensure TBT router powered to avoid leakage/clamping of signals.

LPCPLUS_GPIO is aliased, do not attempt use during PCH debug.

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014
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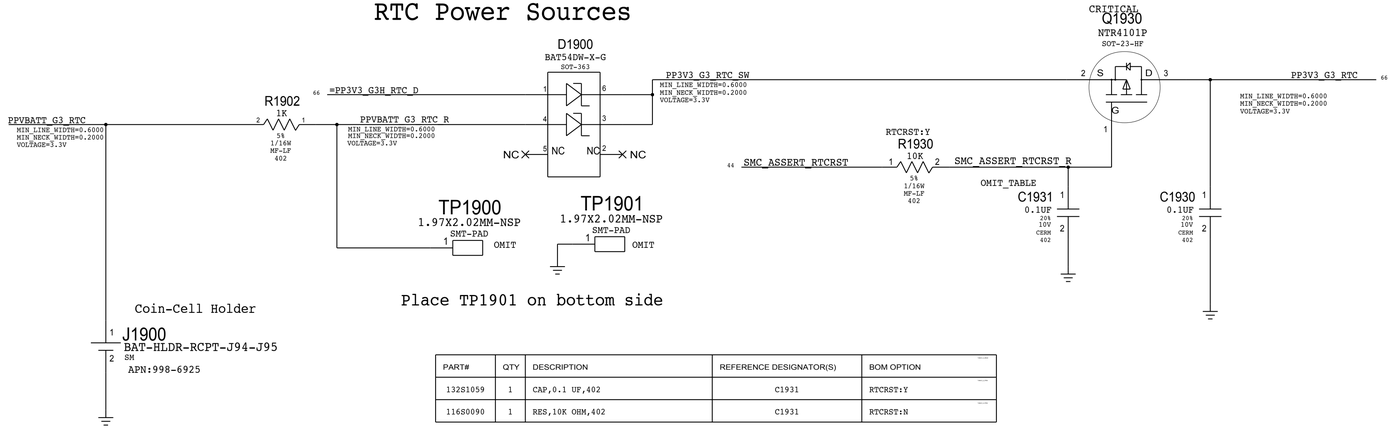
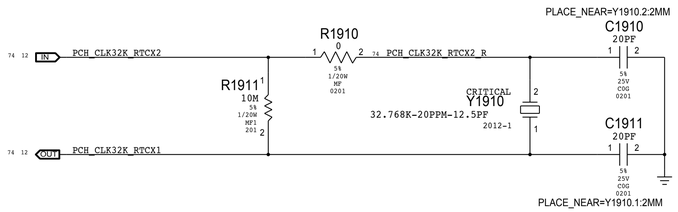
RTC Power Sources



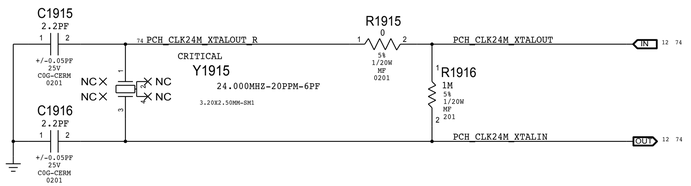
Place TP1901 on bottom side

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S1059	1	CAP,0.1 UF,402	C1931	RTCRST:Y
116S0090	1	RES,10K OHM,402	C1931	RTCRST:N

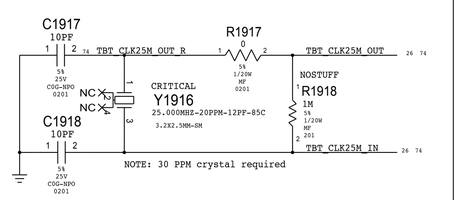
PCH RTC Crystal



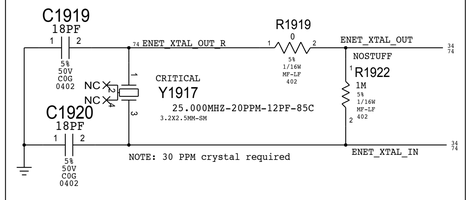
PCH 24MHz Crystal



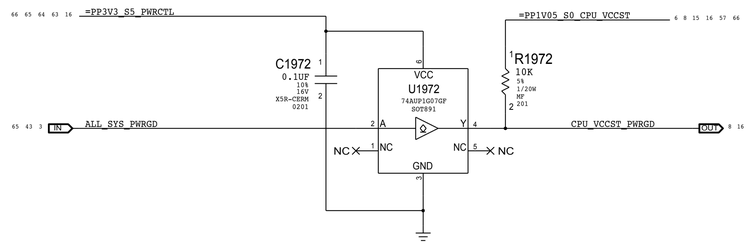
TBT 25MHz Crystal



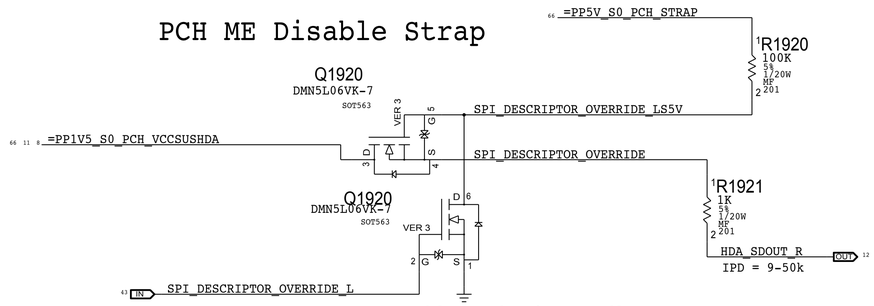
Ethernet 25MHz Crystal



ALL_SYS_PWRGD/CPU_VCCST_PWRGD Level-Shifter

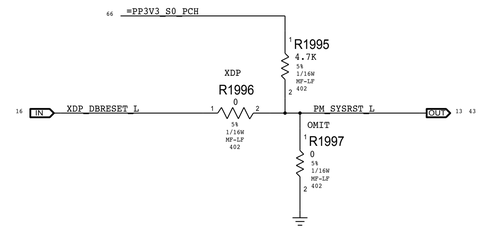


PCH ME Disable Strap

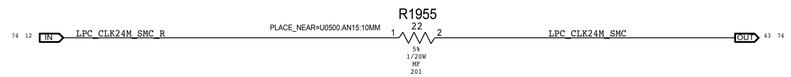


PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.

PCH Reset Button



Clock series termination



SYNC_MASTER=J70_NICK SYNC_DATE=02/25/2014

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Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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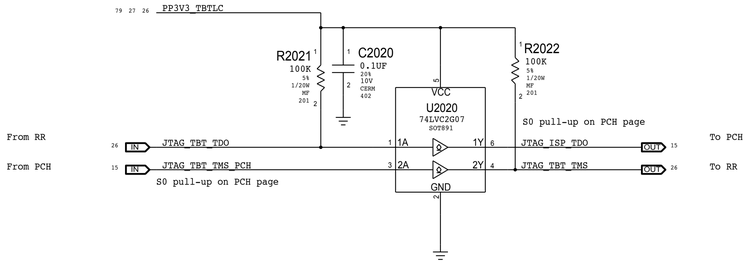
Falcon Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH

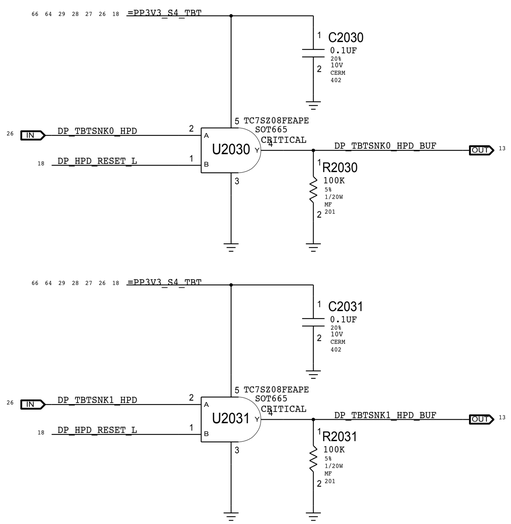


NOTE: Solution shown is for WPT-LP. Other PCH's may require isolation on TCK and TDI as well for PCH glitch-prevention.

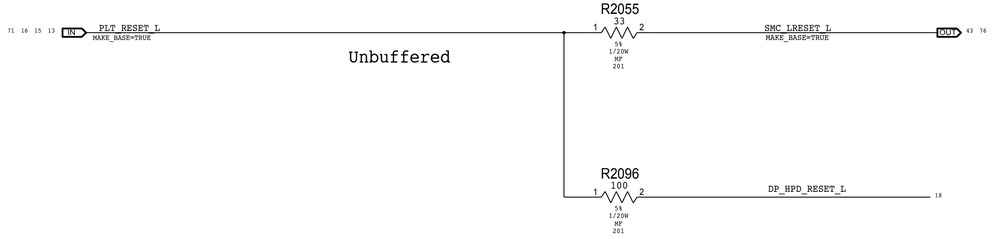
NOTE: This reference schematic assumes PCH JTAG GPIOs are only used for Thunderbolt. If other ASIC JTAG signals are wired into these GPIOs different isolation techniques will likely be necessary. Multi-router designs also require different circuitry.

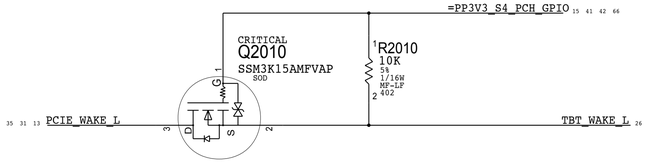
Falcon Ridge HPD Isolation

NOTE: PLT_RESET_L used as the other input to the AND gate so that HPD is only driven high to the PCH in S0.



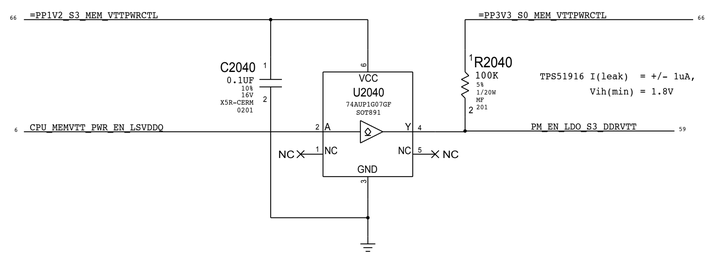
Platform Reset Connections





Memory VTT Enable Level-Shifter

CPU output is on VDDQ rail (1.2V), TPS51916 has 1.8V Vih(min).



SYNC_MASTER=J70_NICK	SYNC_DATE=11/20/2013
PAGE TITLE: Project Chipset Support	
Apple Inc.	DRAWING NUMBER: 051-00081 SIZE: D
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Memory Bit/Byte Swizzle

=MEM_A_DQ<0>	MAKE_BASE	TRUE	MEM_A_DQ<0>	?	?
=MEM_A_DQ<1>		TRUE	MEM_A_DQ<1>	?	?
=MEM_A_DQ<2>		TRUE	MEM_A_DQ<2>	?	?
=MEM_A_DQ<3>		TRUE	MEM_A_DQ<3>	?	?
=MEM_A_DQ<6>		TRUE	MEM_A_DQ<4>	?	?
=MEM_A_DQ<5>		TRUE	MEM_A_DQ<5>	?	?
=MEM_A_DQ<7>		TRUE	MEM_A_DQ<6>	?	?
=MEM_A_DQ<4>		TRUE	MEM_A_DQ<7>	?	?
=MEM_A_DQ<17>		TRUE	MEM_A_DQ<8>	?	?
=MEM_A_DQ<18>		TRUE	MEM_A_DQ<9>	?	?
=MEM_A_DQ<19>		TRUE	MEM_A_DQ<10>	?	?
=MEM_A_DQ<23>		TRUE	MEM_A_DQ<11>	?	?
=MEM_A_DQ<21>		TRUE	MEM_A_DQ<12>	?	?
=MEM_A_DQ<16>		TRUE	MEM_A_DQ<13>	?	?
=MEM_A_DQ<22>		TRUE	MEM_A_DQ<14>	?	?
=MEM_A_DQ<20>		TRUE	MEM_A_DQ<15>	?	?
=MEM_A_DQ<8>		TRUE	MEM_A_DQ<16>	?	?
=MEM_A_DQ<12>		TRUE	MEM_A_DQ<17>	?	?
=MEM_A_DQ<11>		TRUE	MEM_A_DQ<18>	?	?
=MEM_A_DQ<14>		TRUE	MEM_A_DQ<19>	?	?
=MEM_A_DQ<9>		TRUE	MEM_A_DQ<20>	?	?
=MEM_A_DQ<13>		TRUE	MEM_A_DQ<21>	?	?
=MEM_A_DQ<15>		TRUE	MEM_A_DQ<22>	?	?
=MEM_A_DQ<10>		TRUE	MEM_A_DQ<23>	?	?
=MEM_A_DQ<28>		TRUE	MEM_A_DQ<24>	?	?
=MEM_A_DQ<25>		TRUE	MEM_A_DQ<25>	?	?
=MEM_A_DQ<24>		TRUE	MEM_A_DQ<26>	?	?
=MEM_A_DQ<27>		TRUE	MEM_A_DQ<27>	?	?
=MEM_A_DQ<26>		TRUE	MEM_A_DQ<28>	?	?
=MEM_A_DQ<31>		TRUE	MEM_A_DQ<29>	?	?
=MEM_A_DQ<30>		TRUE	MEM_A_DQ<30>	?	?
=MEM_A_DQ<29>		TRUE	MEM_A_DQ<31>	?	?
=MEM_A_DQ<32>		TRUE	MEM_A_DQ<32>	?	?
=MEM_A_DQ<33>		TRUE	MEM_A_DQ<33>	?	?
=MEM_A_DQ<39>		TRUE	MEM_A_DQ<34>	?	?
=MEM_A_DQ<38>		TRUE	MEM_A_DQ<35>	?	?
=MEM_A_DQ<37>		TRUE	MEM_A_DQ<36>	?	?
=MEM_A_DQ<36>		TRUE	MEM_A_DQ<37>	?	?
=MEM_A_DQ<35>		TRUE	MEM_A_DQ<38>	?	?
=MEM_A_DQ<34>		TRUE	MEM_A_DQ<39>	?	?
=MEM_A_DQ<55>		TRUE	MEM_A_DQ<40>	?	?
=MEM_A_DQ<51>		TRUE	MEM_A_DQ<41>	?	?
=MEM_A_DQ<53>		TRUE	MEM_A_DQ<42>	?	?
=MEM_A_DQ<49>		TRUE	MEM_A_DQ<43>	?	?
=MEM_A_DQ<50>		TRUE	MEM_A_DQ<44>	?	?
=MEM_A_DQ<54>		TRUE	MEM_A_DQ<45>	?	?
=MEM_A_DQ<48>		TRUE	MEM_A_DQ<46>	?	?
=MEM_A_DQ<52>		TRUE	MEM_A_DQ<47>	?	?
=MEM_A_DQ<47>		TRUE	MEM_A_DQ<48>	?	?
=MEM_A_DQ<46>		TRUE	MEM_A_DQ<49>	?	?
=MEM_A_DQ<40>		TRUE	MEM_A_DQ<50>	?	?
=MEM_A_DQ<42>		TRUE	MEM_A_DQ<51>	?	?
=MEM_A_DQ<43>		TRUE	MEM_A_DQ<52>	?	?
=MEM_A_DQ<41>		TRUE	MEM_A_DQ<53>	?	?
=MEM_A_DQ<45>		TRUE	MEM_A_DQ<54>	?	?
=MEM_A_DQ<44>		TRUE	MEM_A_DQ<55>	?	?
=MEM_A_DQ<60>		TRUE	MEM_A_DQ<56>	?	?
=MEM_A_DQ<61>		TRUE	MEM_A_DQ<57>	?	?
=MEM_A_DQ<58>		TRUE	MEM_A_DQ<58>	?	?
=MEM_A_DQ<59>		TRUE	MEM_A_DQ<59>	?	?
=MEM_A_DQ<56>		TRUE	MEM_A_DQ<60>	?	?
=MEM_A_DQ<57>		TRUE	MEM_A_DQ<61>	?	?
=MEM_A_DQ<62>		TRUE	MEM_A_DQ<62>	?	?
=MEM_A_DQ<63>		TRUE	MEM_A_DQ<63>	?	?
=MEM_A_DQS_P<0>		TRUE	MEM_A_DQS_P<0>	?	?
=MEM_A_DQS_N<0>		TRUE	MEM_A_DQS_N<0>	?	?
=MEM_A_DQS_P<2>		TRUE	MEM_A_DQS_P<1>	?	?
=MEM_A_DQS_N<2>		TRUE	MEM_A_DQS_N<1>	?	?
=MEM_A_DQS_P<1>		TRUE	MEM_A_DQS_P<2>	?	?
=MEM_A_DQS_N<1>		TRUE	MEM_A_DQS_N<2>	?	?
=MEM_A_DQS_P<3>		TRUE	MEM_A_DQS_P<3>	?	?
=MEM_A_DQS_N<3>		TRUE	MEM_A_DQS_N<3>	?	?
=MEM_A_DQS_P<4>		TRUE	MEM_A_DQS_P<4>	?	?
=MEM_A_DQS_N<4>		TRUE	MEM_A_DQS_N<4>	?	?
=MEM_A_DQS_P<6>		TRUE	MEM_A_DQS_P<5>	?	?
=MEM_A_DQS_N<6>		TRUE	MEM_A_DQS_N<5>	?	?
=MEM_A_DQS_P<5>		TRUE	MEM_A_DQS_P<6>	?	?
=MEM_A_DQS_N<5>		TRUE	MEM_A_DQS_N<6>	?	?
=MEM_A_DQS_P<7>		TRUE	MEM_A_DQS_P<7>	?	?
=MEM_A_DQS_N<7>		TRUE	MEM_A_DQS_N<7>	?	?

=MEM_B_DQ<7>	MAKE_BASE	TRUE	MEM_B_DQ<0>	?	?
=MEM_B_DQ<3>		TRUE	MEM_B_DQ<1>	?	?
=MEM_B_DQ<1>		TRUE	MEM_B_DQ<2>	?	?
=MEM_B_DQ<5>		TRUE	MEM_B_DQ<3>	?	?
=MEM_B_DQ<6>		TRUE	MEM_B_DQ<4>	?	?
=MEM_B_DQ<2>		TRUE	MEM_B_DQ<5>	?	?
=MEM_B_DQ<0>		TRUE	MEM_B_DQ<6>	?	?
=MEM_B_DQ<4>		TRUE	MEM_B_DQ<7>	?	?
=MEM_B_DQ<8>		TRUE	MEM_B_DQ<8>	?	?
=MEM_B_DQ<9>		TRUE	MEM_B_DQ<9>	?	?
=MEM_B_DQ<14>		TRUE	MEM_B_DQ<10>	?	?
=MEM_B_DQ<15>		TRUE	MEM_B_DQ<11>	?	?
=MEM_B_DQ<10>		TRUE	MEM_B_DQ<12>	?	?
=MEM_B_DQ<13>		TRUE	MEM_B_DQ<13>	?	?
=MEM_B_DQ<12>		TRUE	MEM_B_DQ<14>	?	?
=MEM_B_DQ<11>		TRUE	MEM_B_DQ<15>	?	?
=MEM_B_DQ<22>		TRUE	MEM_B_DQ<16>	?	?
=MEM_B_DQ<18>		TRUE	MEM_B_DQ<17>	?	?
=MEM_B_DQ<16>		TRUE	MEM_B_DQ<18>	?	?
=MEM_B_DQ<20>		TRUE	MEM_B_DQ<19>	?	?
=MEM_B_DQ<23>		TRUE	MEM_B_DQ<20>	?	?
=MEM_B_DQ<19>		TRUE	MEM_B_DQ<21>	?	?
=MEM_B_DQ<17>		TRUE	MEM_B_DQ<22>	?	?
=MEM_B_DQ<21>		TRUE	MEM_B_DQ<23>	?	?
=MEM_B_DQ<29>		TRUE	MEM_B_DQ<24>	?	?
=MEM_B_DQ<25>		TRUE	MEM_B_DQ<25>	?	?
=MEM_B_DQ<24>		TRUE	MEM_B_DQ<26>	?	?
=MEM_B_DQ<28>		TRUE	MEM_B_DQ<27>	?	?
=MEM_B_DQ<30>		TRUE	MEM_B_DQ<28>	?	?
=MEM_B_DQ<26>		TRUE	MEM_B_DQ<29>	?	?
=MEM_B_DQ<31>		TRUE	MEM_B_DQ<30>	?	?
=MEM_B_DQ<27>		TRUE	MEM_B_DQ<31>	?	?
=MEM_B_DQ<34>		TRUE	MEM_B_DQ<32>	?	?
=MEM_B_DQ<37>		TRUE	MEM_B_DQ<33>	?	?
=MEM_B_DQ<39>		TRUE	MEM_B_DQ<34>	?	?
=MEM_B_DQ<35>		TRUE	MEM_B_DQ<35>	?	?
=MEM_B_DQ<33>		TRUE	MEM_B_DQ<36>	?	?
=MEM_B_DQ<32>		TRUE	MEM_B_DQ<37>	?	?
=MEM_B_DQ<38>		TRUE	MEM_B_DQ<38>	?	?
=MEM_B_DQ<36>		TRUE	MEM_B_DQ<39>	?	?
=MEM_B_DQ<42>		TRUE	MEM_B_DQ<40>	?	?
=MEM_B_DQ<43>		TRUE	MEM_B_DQ<41>	?	?
=MEM_B_DQ<40>		TRUE	MEM_B_DQ<42>	?	?
=MEM_B_DQ<41>		TRUE	MEM_B_DQ<43>	?	?
=MEM_B_DQ<45>		TRUE	MEM_B_DQ<44>	?	?
=MEM_B_DQ<47>		TRUE	MEM_B_DQ<45>	?	?
=MEM_B_DQ<44>		TRUE	MEM_B_DQ<46>	?	?
=MEM_B_DQ<46>		TRUE	MEM_B_DQ<47>	?	?
=MEM_B_DQ<51>		TRUE	MEM_B_DQ<48>	?	?
=MEM_B_DQ<48>		TRUE	MEM_B_DQ<49>	?	?
=MEM_B_DQ<54>		TRUE	MEM_B_DQ<50>	?	?
=MEM_B_DQ<50>		TRUE	MEM_B_DQ<51>	?	?
=MEM_B_DQ<49>		TRUE	MEM_B_DQ<52>	?	?
=MEM_B_DQ<55>		TRUE	MEM_B_DQ<53>	?	?
=MEM_B_DQ<52>		TRUE	MEM_B_DQ<54>	?	?
=MEM_B_DQ<53>		TRUE	MEM_B_DQ<55>	?	?
=MEM_B_DQ<56>		TRUE	MEM_B_DQ<56>	?	?
=MEM_B_DQ<58>		TRUE	MEM_B_DQ<57>	?	?
=MEM_B_DQ<62>		TRUE	MEM_B_DQ<58>	?	?
=MEM_B_DQ<60>		TRUE	MEM_B_DQ<59>	?	?
=MEM_B_DQ<63>		TRUE	MEM_B_DQ<60>	?	?
=MEM_B_DQ<61>		TRUE	MEM_B_DQ<61>	?	?
=MEM_B_DQ<59>		TRUE	MEM_B_DQ<62>	?	?
=MEM_B_DQ<57>		TRUE	MEM_B_DQ<63>	?	?
=MEM_B_DQS_P<0>		TRUE	MEM_B_DQS_P<0>	?	?
=MEM_B_DQS_N<0>		TRUE	MEM_B_DQS_N<0>	?	?
=MEM_B_DQS_P<1>		TRUE	MEM_B_DQS_P<1>	?	?
=MEM_B_DQS_N<1>		TRUE	MEM_B_DQS_N<1>	?	?
=MEM_B_DQS_P<2>		TRUE	MEM_B_DQS_P<2>	?	?
=MEM_B_DQS_N<2>		TRUE	MEM_B_DQS_N<2>	?	?
=MEM_B_DQS_P<3>		TRUE	MEM_B_DQS_P<3>	?	?
=MEM_B_DQS_N<3>		TRUE	MEM_B_DQS_N<3>	?	?
=MEM_B_DQS_P<4>		TRUE	MEM_B_DQS_P<4>	?	?
=MEM_B_DQS_N<4>		TRUE	MEM_B_DQS_N<4>	?	?
=MEM_B_DQS_P<5>		TRUE	MEM_B_DQS_P<5>	?	?
=MEM_B_DQS_N<5>		TRUE	MEM_B_DQS_N<5>	?	?
=MEM_B_DQS_P<6>		TRUE	MEM_B_DQS_P<6>	?	?
=MEM_B_DQS_N<6>		TRUE	MEM_B_DQS_N<6>	?	?
=MEM_B_DQS_P<7>		TRUE	MEM_B_DQS_P<7>	?	?
=MEM_B_DQS_N<7>		TRUE	MEM_B_DQS_N<7>	?	?

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE

DDR3 Signal Aliases

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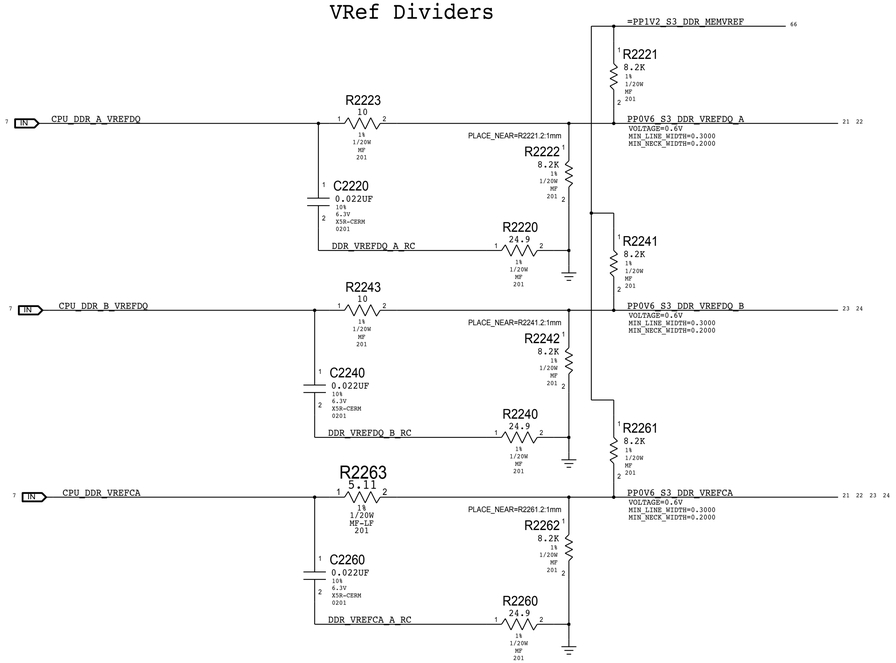
VRef Dividers



SYNC_MASTER=J117_ANDRES SYNC_DATE=02/27/2014

PAGE TITLE

DDR3 VREF MARGINING

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

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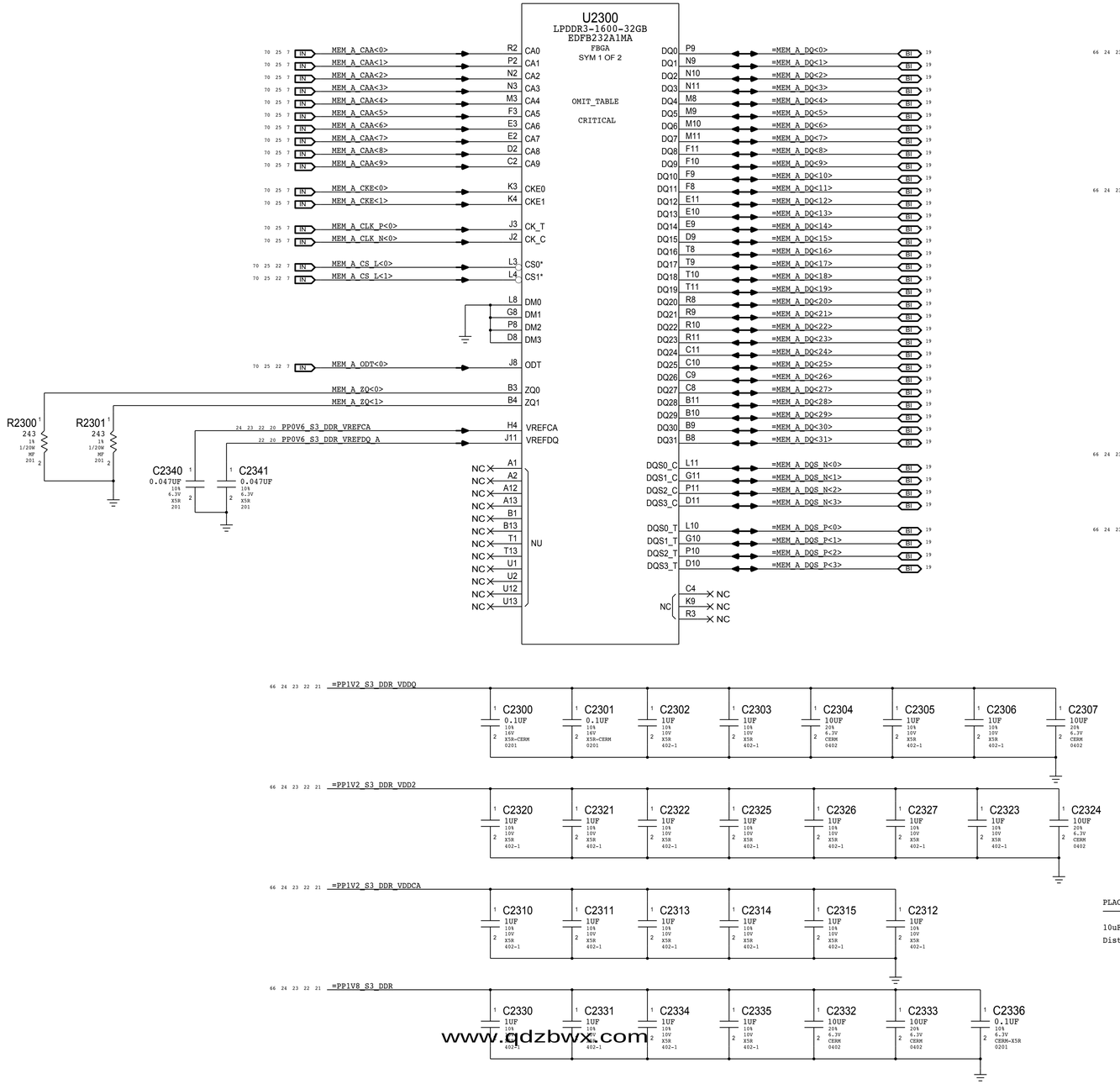
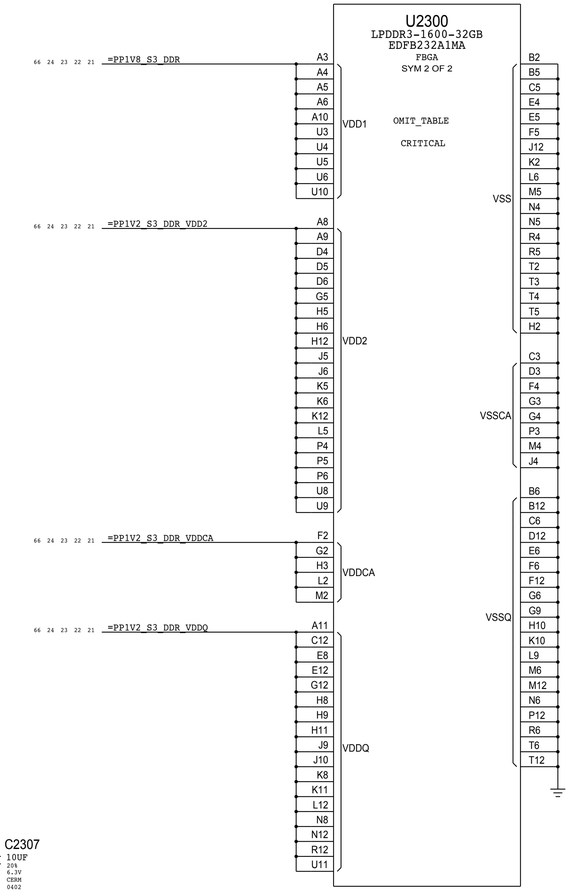
LPDDR3 CHANNEL A (0-31)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB	SYNC_DATE=09/03/2013
PAGE TITLE	LPDDR3 DRAM Channel A (0-31)
Apple Inc.	DRAWING NUMBER 051-00081 · SIZE D
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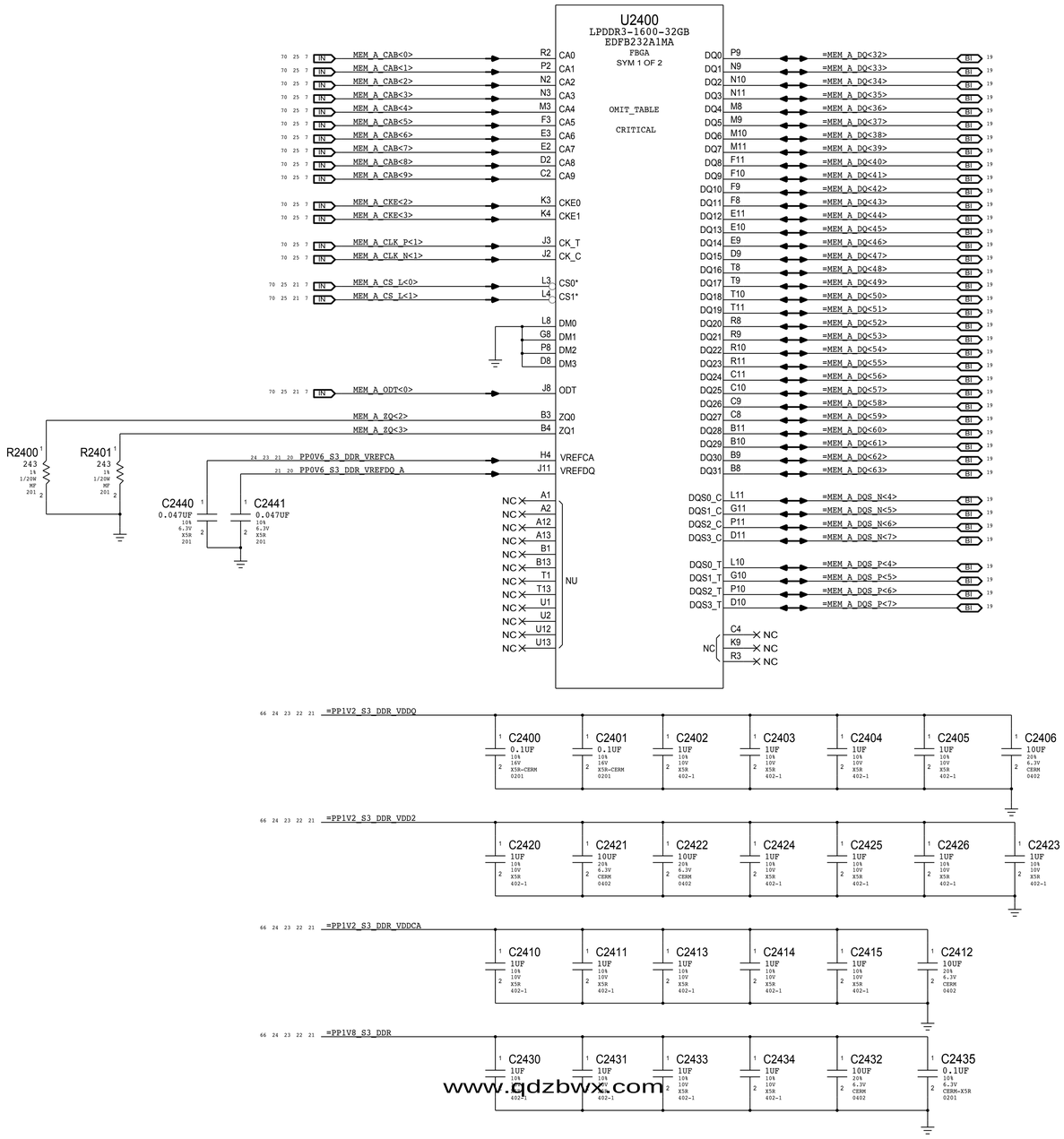
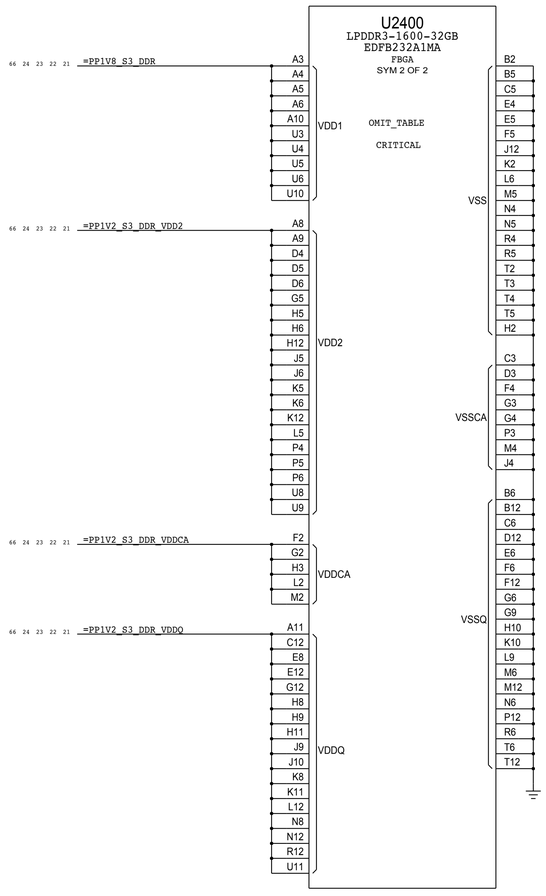
LPDDR3 CHANNEL A (32-63)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB	SYNC_DATE=09/03/2013
PAGE TITLE	LPDDR3 DRAM Channel A (32-63)
Apple Inc.	DRAWING NUMBER 051-00081 · SIZE D
	REVISION 3.0.0
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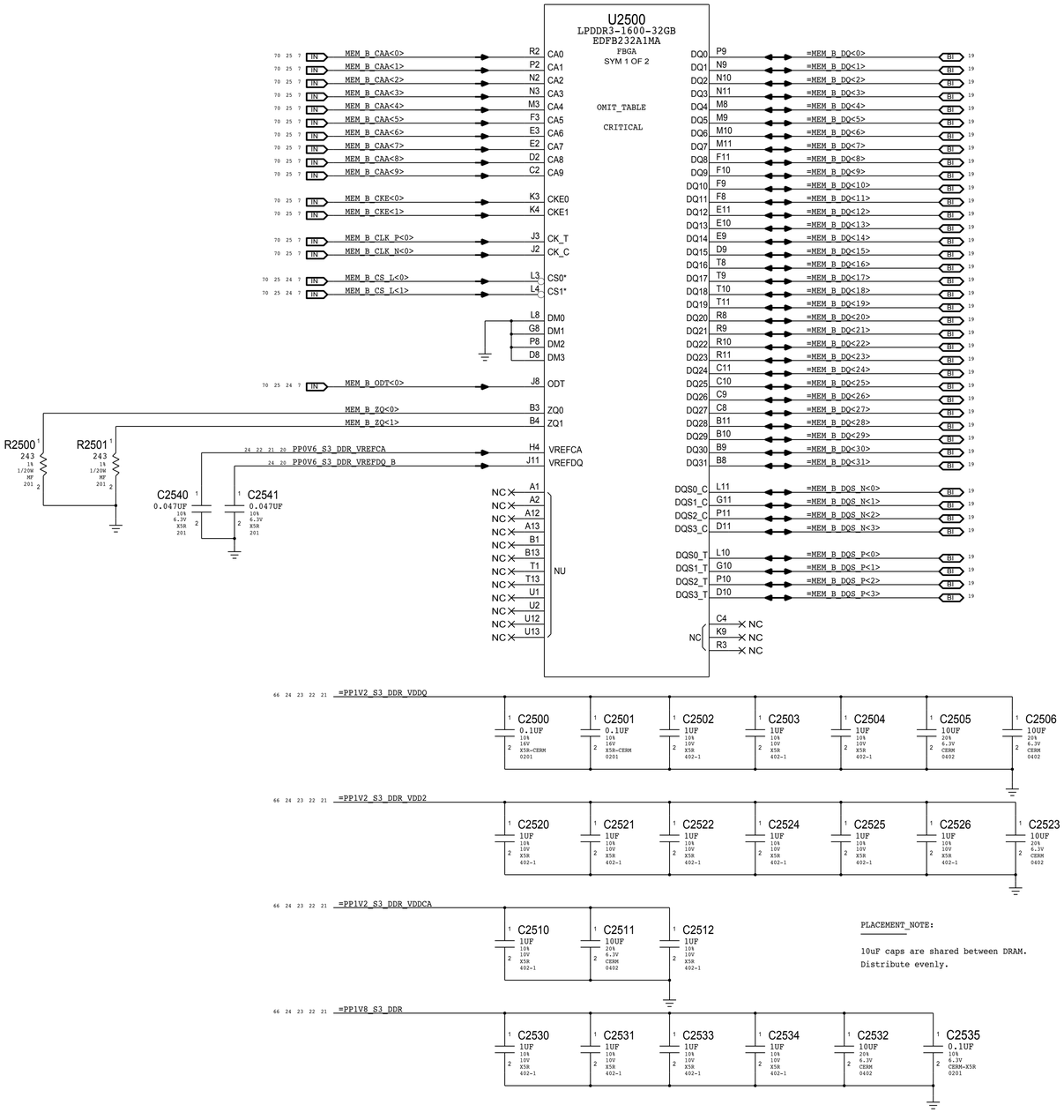
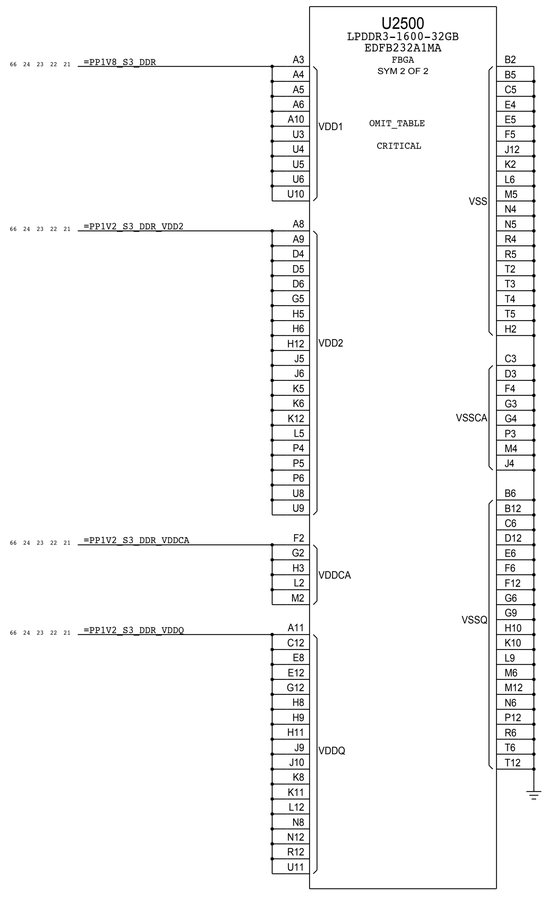
LPDDR3 CHANNEL B (0-31)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

LPDDR3 DRAM Channel B (0-31)

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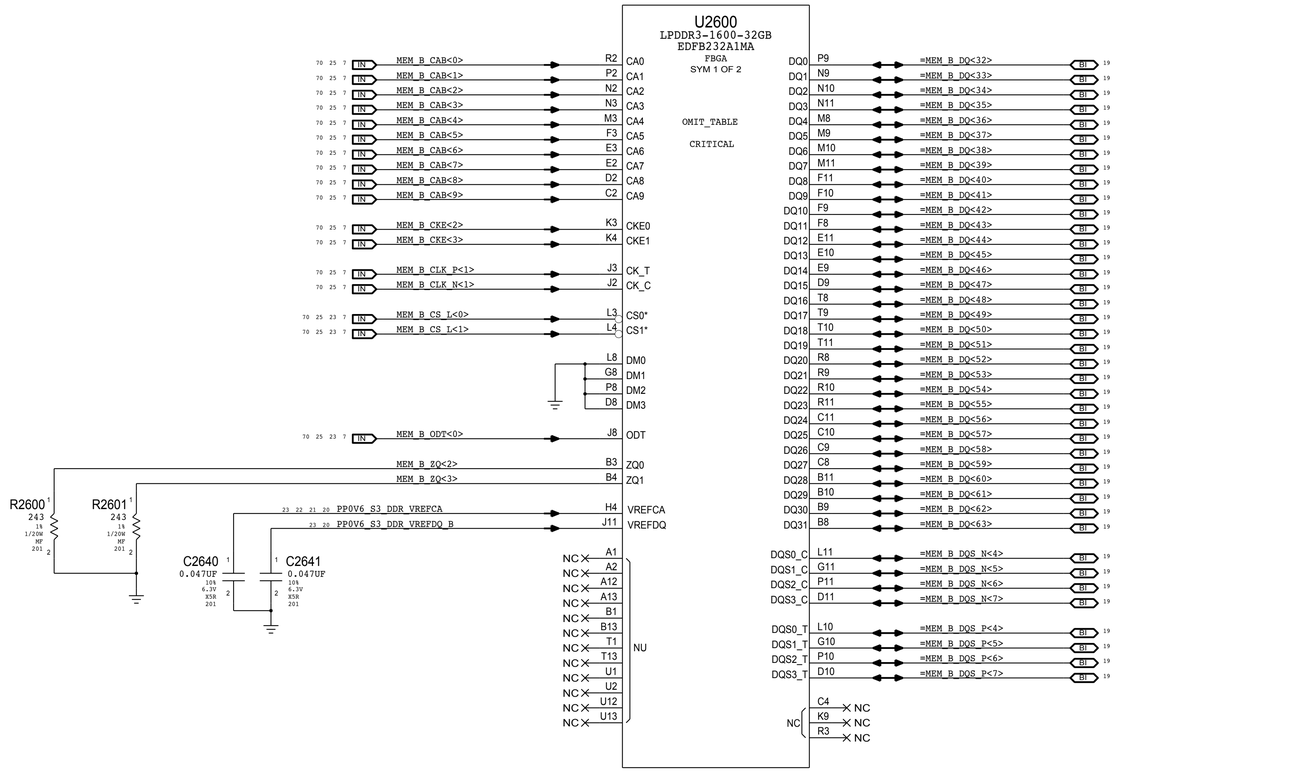
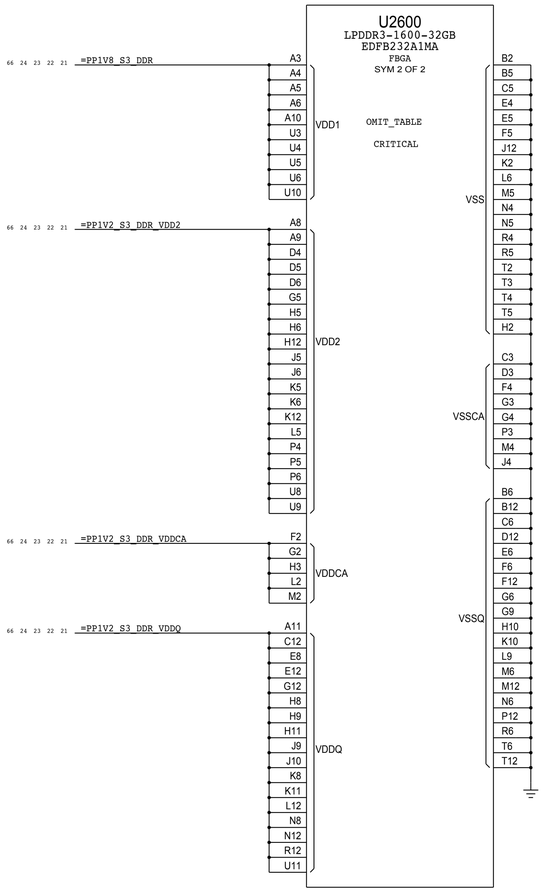
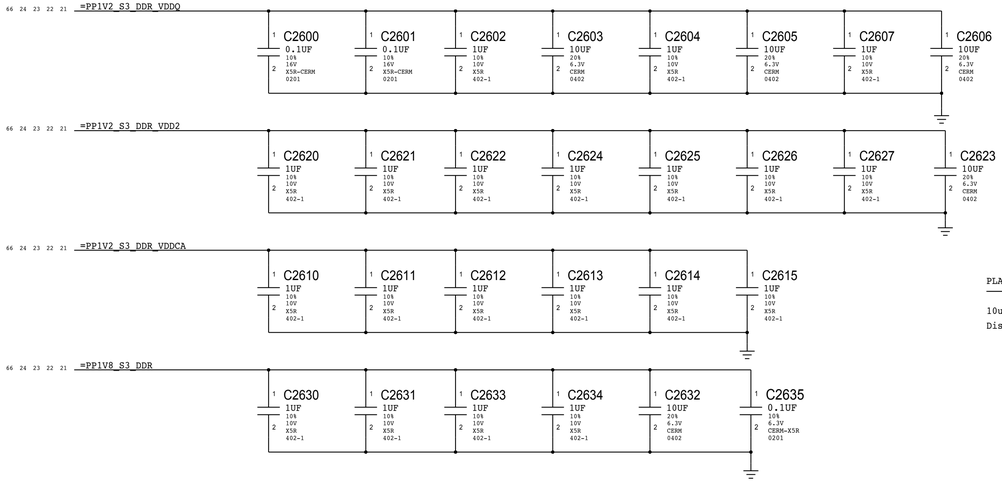
LPDDR3 CHANNEL B (32-63)







PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE

LPDDR3 DRAM Channel B (32-63)

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Intel reccomends 55 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK

66 =PP0V6_S3_DDRVTT_A

70 21 7	IN	MEM_A_CAA<9>	RP2701	56	4	5	5%	1/32W	4X0201-HF	
70 21 7	IN	MEM_A_CAA<8>	RP2701	56	3	6	5%	1/32W	4X0201-HF	
70 21 7	IN	MEM_A_CAA<6>	RP2701	56	2	7	5%	1/32W	4X0201-HF	
70 21 7	IN	MEM_A_CAA<7>	RP2701	56	1	8	5%	1/32W	4X0201-HF	
70 21 7	IN	MEM_A_CAA<5>	R2700	56	1	2	5%	1/32W	4X0201-HF	
70 21 7	IN	MEM_A_CLK_P<0>	R2701	39	1	2	5%	1/20W	201 MF	
70 21 7	IN	MEM_A_CLK_N<0>	R2702	39	1	2	5%	1/20W	201 MF	
70 21 7	IN	MEM_A_CKE<1>	R2703	82	1	2	5%	1/20W	201 MF	
70 21 7	IN	MEM_A_CKE<0>	R2704	82	1	2	5%	1/20W	201 MF	
70 21 7	IN	MEM_A_CAA<4>	R2705	56	1	2	5%	1/20W	201 MF	
70 21 7	IN	MEM_A_CAA<3>	R2706	56	1	2	5%	1/20W	201 MF	
70 21 7	IN	MEM_A_CAA<2>	RP2703	56	4	5	5%	1/32W	4X0201-HF	
70 21 7	IN	MEM_A_CAA<1>	RP2703	56	3	6	5%	1/32W	4X0201-HF	
70 21 7	IN	MEM_A_CAA<0>	RP2703	56	2	7	5%	1/32W	4X0201-HF	
70 22 7	IN	MEM_A_CAB<9>	R2725	56	1	2	5%	1/32W	4X0201-HF	
70 22 7	IN	MEM_A_CAB<8>	RP2707	56	4	5	5%	1/20W	201 MF	
70 22 7	IN	MEM_A_CAB<6>	RP2707	56	3	6	5%	1/32W	4X0201-HF	
70 22 7	IN	MEM_A_CAB<7>	RP2707	56	2	7	5%	1/32W	4X0201-HF	
70 22 7	IN	MEM_A_CAB<5>	RP2707	56	1	8	5%	1/32W	4X0201-HF	
70 22 7	IN	MEM_A_CLK_P<1>	R2707	39	1	2	5%	1/20W	201 MF	
70 22 7	IN	MEM_A_CLK_N<1>	R2708	39	1	2	5%	1/20W	201 MF	
70 22 7	IN	MEM_A_CKE<2>	R2709	82	1	2	5%	1/20W	201 MF	
70 22 7	IN	MEM_A_CKE<3>	R2720	82	1	2	5%	1/20W	201 MF	
70 22 7	IN	MEM_A_CAB<4>	R2721	56	1	2	5%	1/20W	201 MF	
70 22 7	IN	MEM_A_CAB<2>	RP2704	56	4	5	5%	1/32W	4X0201-HF	
70 22 7	IN	MEM_A_CAB<3>	RP2704	56	3	6	5%	1/32W	4X0201-HF	
70 22 7	IN	MEM_A_CAB<1>	RP2704	56	2	7	5%	1/32W	4X0201-HF	
70 22 7	IN	MEM_A_CAB<0>	RP2704	56	1	8	5%	1/32W	4X0201-HF	
70 22 21 7	IN	MEM_A_CS_L<0>	R2722	82	1	2	5%	1/20W	201 MF	
70 22 21 7	IN	MEM_A_CS_L<1>	R2723	82	1	2	5%	1/20W	201 MF	
70 22 21 7	IN	MEM_A_ODT<0>	R2724	82	1	2	5%	1/20W	201 MF	

C2700 0.47UF 20% 4V CERM-X5R-1 201

C2701 0.47UF 20% 4V CERM-X5R-1 201

C2702 0.47UF 20% 4V CERM-X5R-1 201

C2703 0.47UF 20% 4V CERM-X5R-1 201

C2704 0.47UF 20% 4V CERM-X5R-1 201

C2705 0.47UF 20% 4V CERM-X5R-1 201

C2706 0.47UF 20% 4V CERM-X5R-1 201

C2707 0.47UF 20% 4V CERM-X5R-1 201

C2708 0.47UF 20% 4V CERM-X5R-1 201

C2709 0.47UF 20% 4V CERM-X5R-1 201

CRITICAL
C2720 22UF 20% 6.3V X5R-CERM-1 603

Spare
RP2703
56
1 8
34
1/32W
4X0201-HF
NC NC

PLACE_NEAR=RP2701.5:4mm

66 =PP0V6_S3_DDRVTT_B

70 23 7	IN	MEM_B_CAA<9>	RP2712	56	4	5	5%	1/32W	4X0201-HF	
70 23 7	IN	MEM_B_CAA<8>	RP2712	56	3	6	5%	1/32W	4X0201-HF	
70 23 7	IN	MEM_B_CAA<7>	RP2712	56	2	7	5%	1/32W	4X0201-HF	
70 23 7	IN	MEM_B_CAA<6>	RP2712	56	1	8	5%	1/32W	4X0201-HF	
70 23 7	IN	MEM_B_CAA<5>	R2710	56	1	2	5%	1/20W	201 MF	
70 23 7	IN	MEM_B_CLK_P<0>	R2711	39	1	2	5%	1/20W	201 MF	
70 23 7	IN	MEM_B_CLK_N<0>	R2712	39	1	2	5%	1/20W	201 MF	
70 23 7	IN	MEM_B_CKE<1>	R2713	82	1	2	5%	1/20W	201 MF	
70 23 7	IN	MEM_B_CKE<0>	R2714	82	1	2	5%	1/20W	201 MF	
70 23 7	IN	MEM_B_CAA<4>	R2715	56	1	2	5%	1/20W	201 MF	
70 23 7	IN	MEM_B_CAA<2>	R2716	56	1	2	5%	1/20W	201 MF	
70 23 7	IN	MEM_B_CAA<3>	RP2713	56	4	5	5%	1/32W	4X0201-HF	
70 23 7	IN	MEM_B_CAA<1>	RP2713	56	3	6	5%	1/32W	4X0201-HF	
70 23 7	IN	MEM_B_CAA<0>	RP2713	56	2	7	5%	1/32W	4X0201-HF	
70 24 7	IN	MEM_B_CAB<9>	R2735	56	1	2	5%	1/32W	4X0201-HF	
70 24 7	IN	MEM_B_CAB<8>	RP2717	56	4	5	5%	1/20W	201 MF	
70 24 7	IN	MEM_B_CAB<7>	RP2717	56	3	6	5%	1/32W	4X0201-HF	
70 24 7	IN	MEM_B_CAB<6>	RP2717	56	2	7	5%	1/32W	4X0201-HF	
70 24 7	IN	MEM_B_CAB<5>	RP2717	56	1	8	5%	1/32W	4X0201-HF	
70 24 7	IN	MEM_B_CLK_N<1>	R2717	39	1	2	5%	1/20W	201 MF	
70 24 7	IN	MEM_B_CLK_P<1>	R2718	39	1	2	5%	1/20W	201 MF	
70 24 7	IN	MEM_B_CKE<2>	R2719	82	1	2	5%	1/20W	201 MF	
70 24 7	IN	MEM_B_CKE<3>	R2730	82	1	2	5%	1/20W	201 MF	
70 24 7	IN	MEM_B_CAB<4>	R2731	56	1	2	5%	1/20W	201 MF	
70 24 7	IN	MEM_B_CAB<2>	RP2714	56	4	5	5%	1/32W	4X0201-HF	
70 24 7	IN	MEM_B_CAB<3>	RP2714	56	3	6	5%	1/32W	4X0201-HF	
70 24 7	IN	MEM_B_CAB<1>	RP2714	56	2	7	5%	1/32W	4X0201-HF	
70 24 7	IN	MEM_B_CAB<0>	RP2714	56	1	8	5%	1/32W	4X0201-HF	
70 24 23 7	IN	MEM_B_CS_L<0>	R2732	82	1	2	5%	1/20W	201 MF	
70 24 23 7	IN	MEM_B_CS_L<1>	R2733	82	1	2	5%	1/20W	201 MF	
70 24 23 7	IN	MEM_B_ODT<0>	R2734	82	1	2	5%	1/20W	201 MF	

C2710 0.47UF 20% 4V CERM-X5R-1 201

C2711 0.47UF 20% 4V CERM-X5R-1 201

C2712 0.47UF 20% 4V CERM-X5R-1 201

C2713 0.47UF 20% 4V CERM-X5R-1 201

C2714 0.47UF 20% 4V CERM-X5R-1 201

C2715 0.47UF 20% 4V CERM-X5R-1 201

C2716 0.47UF 20% 4V CERM-X5R-1 201

C2717 0.47UF 20% 4V CERM-X5R-1 201

C2718 0.47UF 20% 4V CERM-X5R-1 201

C2719 0.47UF 20% 4V CERM-X5R-1 201

CRITICAL
C2740 22UF 20% 6.3V X5R-CERM-1 603

Spare
RP2713
56
1 8
35
1/32W
4X0201-HF
NC NC

PLACE_NEAR=RP2714.8:4.5mm

SYNC_MASTER=J41_MLB SYNC_DATE=09/03/2013

PAGE TITLE
LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D
REVISION 3.0.0
BRANCH
PAGE 27 OF 123
SHEET 25 OF 81

CRITICAL
OMIT_TABLE

U2800
FALCON RIDGE
FCBGA
SYM 1 OF 2

PCIE GEN2

PCIE_TBT_R2D_C_P<0>	C2800 0.1UF	PCIE_TBT_R2D_P<0>	AB9 PERP_0
PCIE_TBT_R2D_C_N<0>	C2801 0.1UF	PCIE_TBT_R2D_N<0>	AA10 PERN_0
PCIE_TBT_R2D_C_P<1>	C2802 0.1UF	PCIE_TBT_R2D_P<1>	AA12 PERP_1
PCIE_TBT_R2D_C_N<1>	C2803 0.1UF	PCIE_TBT_R2D_N<1>	AB13 PERN_1
PCIE_TBT_R2D_C_P<2>	C2804 0.1UF	PCIE_TBT_R2D_P<2>	AB15 PERP_2
PCIE_TBT_R2D_C_N<2>	C2805 0.1UF	PCIE_TBT_R2D_N<2>	AA16 PERN_2
PCIE_TBT_R2D_C_N<3>	C2806 0.1UF	PCIE_TBT_R2D_P<3>	AA18 PERP_3
PCIE_TBT_R2D_C_P<3>	C2807 0.1UF	PCIE_TBT_R2D_N<3>	AB19 PERN_3

PIN SWAPPED

PCH_TBT_PCIE_RESET_L			P5 PERST_OD_N
TBT_PWR_ON_POC_RST_L			R4 PWR_ON_POC_RSTN

MISC

NC_TBT_MONDC0			AD23 MONDC0
NC_TBT_MONDC1			AC24 MONDC1
TBT_MONOBSP			W18 MONOBSP
TBT_MONOBSN			W16 MONOBSN
TBT_THERM_DP			AB7 THERMDA
TBT_SPI_MOSI			AA2 EE_DI
TBT_SPI_MISO			Y3 EE_DO
TBT_SPI_CS_L			T5 EE_CS_N
TBT_SPI_CLK			U8 EE_CLK
JTAG_TBT_TDI			W2 TDI
JTAG_TBT_TMS			AB1 TMS
JTAG_TBT_TCK			AA6 TCK
JTAG_TBT_TDO			U6 TDO
TBT_TEST_EN			R6 TEST_EN
TBT_TEST_PWR_GOOD			W8 TEST_PWR_GOOD

DISPLAY PORT

DP_TBTSNK0_ML_P<3>			E14 DPSNK0_3_P
DP_TBTSNK0_ML_N<3>			D13 DPSNK0_3_N
DP_TBTSNK0_ML_P<2>			E16 DPSNK0_2_P
DP_TBTSNK0_ML_N<2>			D15 DPSNK0_2_N
DP_TBTSNK0_ML_P<1>			E18 DPSNK0_1_P
DP_TBTSNK0_ML_N<1>			D17 DPSNK0_1_N
DP_TBTSNK0_ML_P<0>			E20 DPSNK0_0_P
DP_TBTSNK0_ML_N<0>			D19 DPSNK0_0_N
DP_TBTSNK0_AUXCH_P			G4 DPSNK0_AUX_P
DP_TBTSNK0_AUXCH_N			G2 DPSNK0_AUX_N
DP_TBTSNK0_HPD			AB5 DPSNK0_HPD
DP_TBTSNK1_ML_P<3>			E6 DPSNK1_3_P
DP_TBTSNK1_ML_N<3>			D5 DPSNK1_3_N
DP_TBTSNK1_ML_P<2>			E8 DPSNK1_2_P
DP_TBTSNK1_ML_N<2>			D7 DPSNK1_2_N
DP_TBTSNK1_ML_P<1>			E10 DPSNK1_1_P
DP_TBTSNK1_ML_N<1>			D9 DPSNK1_1_N
DP_TBTSNK1_ML_P<0>			E12 DPSNK1_0_P
DP_TBTSNK1_ML_N<0>			D11 DPSNK1_0_N
DP_TBTSNK1_AUXCH_P			H3 DPSNK1_AUX_P
DP_TBTSNK1_AUXCH_N			H1 DPSNK1_AUX_N
DP_TBTSNK1_HPD			U4 DPSNK1_HPD
TBT_A_R2D_C_P<0>			G24 PA_CIO0_TX_P/DPSRC_0_P
TBT_A_R2D_C_N<0>			E24 PA_CIO0_TX_N/DPSRC_0_N
TBT_A_D2R_P<0>			G22 PA_CIO0_RX_P
TBT_A_D2R_N<0>			E22 PA_CIO0_RX_N
TBT_A_CONFIG1_BUF			P1 PA_CONFIG1/CIO_0_LSEO
TBT_A_CONFIG2_RC			K5 PA_CONFIG2/CIO_0_LSOE
TBT_A_R2D_C_P<1>			L24 PA_CIO1_TX_P/DPSRC_2_P
TBT_A_R2D_C_N<1>			J24 PA_CIO1_TX_N/DPSRC_2_N
TBT_A_D2R_P<1>			L22 PA_CIO1_RX_P
TBT_A_D2R_N<1>			J22 PA_CIO1_RX_N
TBT_A_LSTX			N8 PA_LSTX/CIO_1_LSEO
TBT_A_LSRX			J6 PA_LSRX/CIO_1_LSOE
DP_TBTPA_ML_C_P<1>			A16 PA_DPSRC_1_P
DP_TBTPA_ML_C_N<1>			B17 PA_DPSRC_1_N
DP_TBTPA_ML_C_P<3>			A18 PA_DPSRC_3_P
DP_TBTPA_ML_C_N<3>			B19 PA_DPSRC_3_N
DP_TBTPA_AUXCH_C_P			L4 PA_AUX_P
DP_TBTPA_AUXCH_C_N			L2 PA_AUX_N
DP_TBTPA_HPD			M3 PA_DPSRC_HPD
TBT_A_HV_EN			R8 GPIO_0/PA_HV_EN/BYP0
TBT_A_CIO_SEL			N2 GPIO_10/PA_CIO_SEL/BYP1
TBT_A_DP_PWRDN			P3 GPIO_12/PA_DP_PWRDN/BYP2

For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.

DP_TBTSRC_ML_P<3>			A14 DPSRC_3_P
DP_TBTSRC_ML_N<3>			B15 DPSRC_3_N
DP_TBTSRC_ML_P<2>			A12 DPSRC_2_P
DP_TBTSRC_ML_N<2>			B13 DPSRC_2_N
DP_TBTSRC_ML_P<1>			A10 DPSRC_1_P
DP_TBTSRC_ML_N<1>			B11 DPSRC_1_N
DP_TBTSRC_ML_P<0>			A8 DPSRC_0_P
DP_TBTSRC_ML_N<0>			B9 DPSRC_0_N
DP_TBTSRC_AUX_P			J4 DPSRC_AUX_P
DP_TBTSRC_AUX_N			J2 DPSRC_AUX_N
DP_TBTSRC_HPD			AC2 DPSRC_HPD_OD

PORTS

			U2 GPIO_2/TMU_CLK_IN/AC_PRESENT
TBT_PWR_EN			L6 GPIO_3/FORCE_PWR
TBT_WAKE_L			H5 GPIO_4/WAKE_OD_N
TBT_CIO_PLUG_EVENT_L			Y7 GPIO_5/CIO_PLUG_EVENT_N/HV_OK_OD
HDMITBTMUX_SEL_TBT			Y1 GPIO_6_OD/CIO_SDA_OD
TBT_GPIO7			T7 GPIO_7_OD/CIO_SCL_OD
TBT_EN_CIO_PWR_L			V7 GPIO_8/EN_CIO_PWR_N_OD
TBT_BATLOW_L			M7 GPIO_9/SX_CTRL_OD*
TBTDP_AUXIO_EN			T1 GPIO_14
TBT_DDC_XBAR_EN_L			T3 GPIO_15
TBT_B_R2D_C_P<0>			R24 PB_CIO2_TX_P/DPSRC_0_P
TBT_B_R2D_C_N<0>			N24 PB_CIO2_TX_N/DPSRC_0_N
TBT_B_D2R_P<0>			R22 PB_CIO2_RX_P
TBT_B_D2R_N<0>			N22 PB_CIO2_RX_N
TBT_B_CONFIG1_BUF			D3 PB_CONFIG1/CIO_2_LSEO
TBT_B_CONFIG2_RC			M1 PB_CONFIG2/CIO_2_LSOE
TBT_B_R2D_C_P<1>			W24 PB_CIO3_TX_P/DPSRC_2_P
TBT_B_R2D_C_N<1>			U24 PB_CIO3_TX_N/DPSRC_2_N
TBT_B_D2R_P<1>			W22 PB_CIO3_RX_P
TBT_B_D2R_N<1>			U22 PB_CIO3_RX_N
TBT_B_LSTX			M5 PB_LSTX/CIO_3_LSEO
TBT_B_LSRX			P7 PB_LSRX/CIO_3_LSOE
DP_TBTPB_ML_C_P<1>			A20 PB_DPSRC_1_P
DP_TBTPB_ML_C_N<1>			B21 PB_DPSRC_1_N
DP_TBTPB_ML_C_P<3>			A22 PB_DPSRC_3_P
DP_TBTPB_ML_C_N<3>			B23 PB_DPSRC_3_N
DP_TBTPB_AUXCH_C_P			K3 PB_AUX_P
DP_TBTPB_AUXCH_C_N			K1 PB_AUX_N
DP_TBTPB_HPD			N6 PB_DPSRC_HPD
TBT_B_HV_EN			F1 GPIO_1/PB_HV_EN/BYP0
TBT_B_CIO_SEL			R2 GPIO_11/PB_CIO_SEL/BYP1
TBT_B_DP_PWRDN			F3 GPIO_13/PB_DP_PWRDN/BYP2

			U20 RSENSE
TBT_RBIAS			W20 RBIAS
			AD1 RSVD_GND
TBT_RSENSE			R2855 1K 1% 1/20W MF 201

TP_TBT_PCIE_RESET0_L			W6 GPIO_16/DEVICE_PCIE_RST_N
TBT_DFT_STRAP_1			AB3 GPIO_17
TBT_ROM_SECURITY_XOR			AD3 GPIO_18
TBT_DFT_STRAP_3			V1 GPIO_19
TBT_CLKREQ_L			V3 PCIE_CLKREQ_OD_N
PCIE_CLK100M_TBT_P			AB21 REFCLK_100_IN_P
PCIE_CLK100M_TBT_N			AD21 REFCLK_100_IN_N
TBT_CLK25M_IN			AA24 XTAL_25_IN
TBT_CLK25M_OUT			AB23 XTAL_25_OUT
TBT_TMU_CLK_OUT			AA4 TMU_CLK_OUT

Used for straps in host mode

PCIE_TBT_D2R_C_P<0>	C2840 0.1UF	PCIE_TBT_D2R_P<0>	AD5 PETP_0
PCIE_TBT_D2R_C_N<0>	C2841 0.1UF	PCIE_TBT_D2R_N<0>	AD7 PETN_0
PCIE_TBT_D2R_C_P<1>	C2842 0.1UF	PCIE_TBT_D2R_N<1>	AD9 PETP_1
PCIE_TBT_D2R_C_N<1>	C2843 0.1UF	PCIE_TBT_D2R_P<1>	AD11 PETN_1
PCIE_TBT_D2R_C_P<2>	C2844 0.1UF	PCIE_TBT_D2R_N<2>	AD13 PETP_2
PCIE_TBT_D2R_C_N<2>	C2845 0.1UF	PCIE_TBT_D2R_P<2>	AD15 PETN_2
PCIE_TBT_D2R_C_P<3>	C2846 0.1UF	PCIE_TBT_D2R_N<3>	AD17 PETP_3
PCIE_TBT_D2R_C_N<3>	C2847 0.1UF	PCIE_TBT_D2R_P<3>	AD19 PETN_3

PIN SWAPPED

PIN SWAPPED

PP3V3_TBTLC

R2890 3.3K 5% 1/20W MF 201
R2891 3.3K 5% 1/20W MF 201
C2890 1UF 10% 6.3V CERM 402
R2892 3.3K 5% 1/20W MF 201
R2893 3.3K 5% 1/20W MF 201

BYPASS=U2890.8::2mm

CRITICAL
OMIT_TABLE

U2890
4MBIT
W25X40CLXIG
USON

TBT_SPI_MOSI_R	5	DI/IO0
TBT_SPI_CLK_R	6	CLK
(TBT_SPI_CS_L)	1	CS*
TBTROM_WP_L	3	WP*
TBTROM_HOLD_L	7	HOLD*
	2	DO/IO1
	4	GND
	9	THRM_PAD

TBT_SPI_MISO_R

R2894 33 5% 1/20W MF 201
R2895 33 5% 1/20W MF 201

OMIT
R2815 NOSTUFF NONE NONE NONE 0201

DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
Use AA8 GND ball for THERM_DN

R2896 0 5% 1/20W MF 0201

R2829 10K 5% 1/20W MF 201

R2825 100 5% 1/20W MF 201

SNK0 AC Coupling

DP_TBTSNK0_ML_C_P<0>	C2820 0.1UF	DP_TBTSNK0_ML_P<0>	
DP_TBTSNK0_ML_C_N<0>	C2821 0.1UF	DP_TBTSNK0_ML_N<0>	
DP_TBTSNK0_ML_C_P<1>	C2822 0.1UF	DP_TBTSNK0_ML_P<1>	
DP_TBTSNK0_ML_C_N<1>	C2823 0.1UF	DP_TBTSNK0_ML_N<1>	
DP_TBTSNK0_ML_C_P<2>	C2824 0.1UF	DP_TBTSNK0_ML_P<2>	
DP_TBTSNK0_ML_C_N<2>	C2825 0.1UF	DP_TBTSNK0_ML_N<2>	
DP_TBTSNK0_ML_C_P<3>	C2826 0.1UF	DP_TBTSNK0_ML_P<3>	
DP_TBTSNK0_ML_C_N<3>	C2827 0.1UF	DP_TBTSNK0_ML_N<3>	
DP_TBTSNK0_AUXCH_C_P	C2828 0.1UF	DP_TBTSNK0_AUXCH_P	
DP_TBTSNK0_AUXCH_C_N	C2829 0.1UF	DP_TBTSNK0_AUXCH_N	

SNK1 AC Coupling

DP_TBTSNK1_ML_C_P<0>	C2830 0.1UF	DP_TBTSNK1_ML_P<0>	
DP_TBTSNK1_ML_C_N<0>	C2831 0.1UF	DP_TBTSNK1_ML_N<0>	
DP_TBTSNK1_ML_C_P<1>	C2832 0.1UF	DP_TBTSNK1_ML_P<1>	
DP_TBTSNK1_ML_C_N<1>	C2833 0.1UF	DP_TBTSNK1_ML_N<1>	
DP_TBTSNK1_ML_C_P<2>	C2834 0.1UF	DP_TBTSNK1_ML_P<2>	
DP_TBTSNK1_ML_C_N<2>	C2835 0.1UF	DP_TBTSNK1_ML_N<2>	
DP_TBTSNK1_ML_C_P<3>	C2836 0.1UF	DP_TBTSNK1_ML_P<3>	
DP_TBTSNK1_ML_C_N<3>	C2837 0.1UF	DP_TBTSNK1_ML_N<3>	
DP_TBTSNK1_AUXCH_C_P	C2838 0.1UF	DP_TBTSNK1_AUXCH_P	
DP_TBTSNK1_AUXCH_C_N	C2839 0.1UF	DP_TBTSNK1_AUXCH_N	

Security strap setting is XORed with bit in the flash, so the active-level depends on the code in the flash.

If strap != bit then security is enabled?

PP3V3_TBTLC

NO STUFF
R2867 10K 5% 1/20W MF 201

R2861 10K 5% 1/20W MF 201
R2862 10K 5% 1/20W MF 201
R2863 10K 5% 1/20W MF 201

NO STUFF
R2899 10K 5% 1/20W MF 201

PP3V3_TBTLC
=PP3V3_S4_TBT

R2881 100K 5% 1/20W MF 201
R2880 100K 5% 1/20W MF 201
R2882 100K 5% 1/20W MF 201

TBT_EN_CIO_PWR_L	
TBT_DDC_XBAR_EN_L	
HDMITBTMUX_SEL_TBT	
TBTDP_AUXIO_EN	
DP_TBTSRC_HPD	

PP3V3_TBTLC

R2878 100K 5% 1/20W MF 201
R2879 100K 5% 1/20W MF 201

R2832 100K 5% 1/20W MF 201
R2883 100K 5% 1/20W MF 201

=PP3V3_S4_TBT

R2884 100K 5% 1/20W MF 201

NO STUFF
R2885 10K 5% 1/20W MF 201

NO STUFF
R2886 10K 5% 1/20W MF 201

TBT_BATLOW_L	
TBT_A_DP_PWRDN	
TBT_B_DP_PWRDN	
TBT_A_HV_EN	
TBT_B_HV_EN	

R2888 10K 5% 1/20W MF 201
R2887 10K 5% 1/20W MF 201

NOTE: The following pins require testpoints:

0 - GPIO_13	8 - GPIO_15
1 - GPIO_1	9 - GPIO_11
2 - GPIO_2	10 - GPIO_14
3 - GPIO_3	11 - GPIO_0
4 - GPIO_5	12 - GPIO_12
5 - PCIE_RST_1_N	13 - GPIO_10
6 - PCIE_RST_2_N	14 - PB_LSTX
7 - PCIE_RST_3_N	15 - PB_LSRX

SYNC_MASTER=J117_NICK
SYNC_DATE=01/27/2014

PAGE TITLE

Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER 051-00081
SIZE D
REVISION 3.0.0
BRANCH
PAGE 28 OF 123
SHEET 26 OF 81

U2950

Part	SLG5AP304V
Type	Load Switch
R(on) @ 1.05V	7.8 mOhm Typ 9.6 mOhm Max

Max Current = 4A (85C)

1.05V TBT "CIO" Switch

Internal switch not functional on RR.

66 64 29 28 27 26 18 =PP3V3_S4_TBT

C2940 1.0UF 20% 6.3V X5R 0201-1

27 PP1V05_TBT

U2940 SLG5AP304V TDFN CRITICAL

VDD, CAP, ON, GND, D, S

PP3V3_TBTLC 18 26 27 79

R2945 100K 1% 1/20W MF 201

C2941 0.0022UF 10% 50V CERM 402

Q2945 DMN5L06VK-7 SOT563

66 27 16 15 13 12 =PP3V3_S0_PCH_GPIO

13 OUT TBT_PWR_REQ_L

TBT_EN_CIO_PWR_L IN 24

Pull-up (S0) on PCH page

Q2945 DMN5L06VK-7 SOT563

C2900 C2901 C2902 C2903 C2904 C2905 C2906 1.0UF 20% 6.3V X5R 0201-1

PP1V05_TBTRDV MIN_LINE_WIDTH=0.3800 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.05V

700 mA EDP

U2800 FALCON RIDGE FCBGA SYM 2 OF 2

VCC1P0_RDV_DECAP

VCC1P0_CIO

C2930 C2931 C2932 1.0UF 20% 6.3V X5R 0201-1

PP1V05_TBTCIO MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.05V

1200 mA EDP

SVR input to RR - 1100 mA EDP

POC input to RR - 150 mA EDP

Isolated to reduce noise from SVR

VCC3P3

VCC3P3_LC

PP3V3_TBTLC MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=3.3V

100 mA EDP

C2970 1.0UF 20% 6.3V X5R 0201-1

VCC3P3_RDV_DECAP

PP3V3_TBTRDV MIN_LINE_WIDTH=0.3800 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

25 mA EDP

C2980 C2981 1.0UF 20% 6.3V X5R 0201-1

=PP3V3_S4_TBT 18 26 27 28 29 64 66

3.1 W (Dual-Port)

2.4 W (Single-Port)

EDP: 1.25 A

PLACE_NEAR=C2952:1.3mm

C2950 C2951 C2952 C2953 10UF 20% 6.3V CERM-X5R 0402-1

XW2960 SM

PP3V3_S4_TBT_F MIN_LINE_WIDTH=0.3800 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V

C2960 C2961 1.0UF 20% 6.3V X5R 0201-1

27 PP1V05_TBT MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.05V

C2910 C2911 1.0UF 20% 6.3V X5R 0201-1

SVR_VCC1P0

CRITICAL L2920 680NH-30%-3.6A-35MOHM SM

1900 mA EDP

P1V05TBT_SW MIN_LINE_WIDTH=0.5000 MIN_NECK_WIDTH=0.2000 DIDT=TRUE SWITCH_NODE=TRUE

SVR_IND

C2923 C2922 C2921 C2920 10UF 20% 6.3V CERM-X5R 0402-1

CRITICAL D2920 SOD-323 NSR1020MW2T1G

NC SVR_AMON

A2, B1, and C2 are the ground current pins for A4, A6, and B3.
They should be routed as a shape to the annode of D2920.

VSS

GND

TBT "POC" Power-up Reset

66 64 29 28 27 26 18 =PP3V3_S4_TBT

65 64 43 IN SMC_DELAYED_PWRGD

66 27 16 15 13 12 =PP3V3_S0_PCH_GPIO

R2995 100K 1% 1/20W MF 201

Q2995 DMN32D2LFB4 DFN1006B4-3

SYM_VER_3

R2990 100K 1% 1/20W MF 201

R2992 100K 1% 1/20W MF 201

CRITICAL

U2990 TPS3895ADRY USON

VCC, ENABLE, SENSE, GND, SENSE_OUT, CT

C2990 0.1UF 10% 25V X5R 402

15 IN TBT_POC_RESET_L

TBTPOCRST_MR_L

TBTPOCRST_SENSE

TBTPOCRST_CT

Push-pull output

TBT_PWR_ON_POC_RST_L OUT 26

C2995 330PF 10% 16V X7R 0201

R2991 24.9K 1% 1/20W MF 201

C2991 0.001UF 10% 50V X7R-CERM 0402

Vth = 2.508V nominal

Delay = 4.04ms nominal

EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC_MASTER=J70_NICK	SYNC_DATE=01/12/2014
PAGE TITLE	Thunderbolt Host (2 of 2)
Apple Inc.	DRAWING NUMBER 051-00081 SIZE D
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	PAGE 29 OF 123
	SHEET 27 OF 81

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

For 12V systems:

I(min) = 38429/R - 0.0161A
I(max) = 41571/R + 0.0161A

	Min	Max	
IV3P3	1040mA	1155mA	
IHVS0/S3	1060mA	1180mA	(12W minimum)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0398	128S0220		ALL	3.3V INPUT CAP

Thunderbolt Connector A

CRITICAL
U3210
CD3211A1RGP
QFN
V3P3
VHV
ENHVU
EN
HV_EN
S0
V3P3OUT
OUT
FAULTZ
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
=PP3V3_S4_TBTAPWRSW
=PPHV_SW_TBTAPWRSW
18.9V Max
=TBTAPWRSW_EN
TBT_A_HV_EN
=TBT_S0_EN
PPHV_SW_TBTAPWR
TBTAPWRSW_ISET_V3P3
TBTAPWRSW_ISET_S0
TBTAPWRSW_ISET_S3
C3287
C3280
C3281
C3215
C3210
C3211
R3210
R3211
R3212
L3200
FERR-120-OHM-3A
PP3V3RHV_SW_TBTAPWR
C3200
C3201
R3201
TBTACONN_20_RC
=PP3V3_S4_TBT
C3220
C3221
CRITICAL
U3220
CBTL05024
HVQFN24-COMBO
VDD
TB-
TB+
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
HPDOUT
TB_ENA
AUXIO_EN
DP_PD
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
GND
THMPAD
POLARITY SWAPPED
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
DP_TBTPA_AUXCH_C_N
DP_TBTPA_AUXCH_C_P
DP_TBTPA_DDC_DATA
DP_TBTPA_DDC_CLK
TBT_A_CONFIG1_BUF
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
TBT_A_LSTX
TBT_A_LSRX
DP_TBTPA_HPD
TBT_A_CIO_SEL
TBTDP_AUXIO_EN
TBT_A_DP_PWRDN
TBT_A_D2R1_AUXDDC_N
TBT_A_D2R1_AUXDDC_P
TBT: RX_1
TBT_A_CONFIG1_RC
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT: LSX_A_R2P/P2R (P/N)
TBT_A_HPD
C3277
C3276
C3230
C3231
C3232
C3233
CRITICAL
J3200
DUAL-MDP-K70
F-ANG-TH
SHLD
PORT A
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
J70:514-0824 / J78:514-0831
C3205
C3206
TBTACONN_1_C
TBTACONN_7_C
(0-18.9V)
C3270
C3271
C3272
C3273
R3270
R3271
R3272
R3273
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_R2D_P<0>
TBT_A_R2D_N<0>
DP: Lane 0
TBT: TX_0
DP: Lane 1
DP_A_LSX_ML_P<1>
DP_A_LSX_ML_N<1>
TBT_A_R2D_C_N<1>
TBT_A_R2D_C_P<1>
TBT_A_R2D_P<1>
TBT_A_R2D_N<1>
DP: Lane 2
TBT: TX_1
C3274
C3275
TBT_A_D2R_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_C_P<0>
TBT_A_D2R_C_N<0>
TBT: RX_0
R3294
R3295
NO_XNET_CONNECTION=1
C3278
C3279
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_ML_P<3>
DP_TBTPA_ML_N<3>
TBT: Terminated
R3278
R3279
DP: Lane 3
TBT_A_D2R1_AUXDDC_P
TBT_A_D2R1_AUXDDC_N
TBT: RX_1
TBT_A_HPD
TBT_A_CONFIG1_RC
TBT_A_CONFIG2_RC
R3252
R3251
C3294
C3295
R3241
C3202

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=J70_NICK SYNC_DATE=10/16/2013

PAGE TITLE
Thunderbolt Connector A

DRAWING NUMBER 051-00081 SIZE D

Apple Inc.

REVISION 3.0.0

BRANCH

3.3V/HV Power MUX

Thunderbolt Connector B

V3P3 must be S4 to support
wake from Thunderbolt devices.
For 12V systems:
I(min) = 38429/R - 0.0161A
I(max) = 41571/R + 0.0161A
Min Max
IV3P3 1040mA 1155mA
IHVS0/S3 1060mA 1180mA (12W minimum)
=PP3V3_S4_TBTBPWRSW
=PPHV_SW_TBTBPWRSW
18.9V Max
CRITICAL
C3387
100UF
CRITICAL
C3380
22UF
C3381
0.1UF
C3315
4.7UF
C3310
0.1UF
CRITICAL
U3310
CD3211A1RGP
QFN
V3P3
VHV
ENHVU
EN
HV_EN
S0
V3P3OUT
NC
OUT
FAULTZ
ISET_V3P3
ISET_S0
ISET_S3
GND
THRM PAD
=TBTBPWRSW_EN
TBT_B_HV_EN
=TBT_S0_EN
PPHV_SW_TBTBPWR
C3311
0.1UF
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
R3312
36.5K
R3310
35.7K
R3311
35.7K
=PP3V3_S4_TBT
C3320
0.1UF
C3321
0.1UF
VDD
CRITICAL
U3320
CBTL05024
HVQFN24-COMBO
TB-
TB+
AUX-
AUX+
DDC_DAT
DDC_CLK
CA_DETOUT
DP+
DP-
LSTX
LSRX
HPDOUT
GND THMPAD
TB_ENA
AUXIO_EN
DP_PD
AUXIO-
AUXIO+
CA_DET
DPMLO+
DPMLO-
HPD
GND_VOID=TRUE
(Both C's)
POLARITY SWAPPED
C3377
0.47UF
C3376
0.47UF
C3330
0.1UF
C3331
0.1UF
C3332
0.22UF
C3333
0.22UF
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>
DP_TBTPB_AUXCH_C_N
DP_TBTPB_AUXCH_C_P
TBT_B_D2R_C_N<1>
TBT_B_D2R_C_P<1>
DP_TBTPB_AUXCH_N
DP_TBTPB_AUXCH_P
DP_TBTPB_DDC_DATA
DP_TBTPB_DDC_CLK
TBT_B_CONFIG1_BUF
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_P<1>
DP_TBTPB_ML_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPB_HPD
TBT_B_CIO_SEL
TBTDP_AUXIO_EN
TBT_B_DP_PWRDN
TBT_B_D2R1_AUXDDC_N
TBT_B_D2R1_AUXDDC_P
TBT: RX_1
TBT_B_CONFIG1_RC
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
TBT: LSX_B_R2P/P2R (P/N)
TBT_B_HPD
L3300
FERR-120-OHM-3A
PP3V3RHV_SW_TBTBPWR
C3300
0.01UF
C3301
0.01UF
TBTCONN_20_RC
R3301
12
C3305
0.01UF
TBTCONN_1_C
(0-18.9V)
C3306
0.01UF
TBTCONN_7_C
C3370
0.22UF
C3371
0.22UF
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_R2D_P<0>
TBT_B_R2D_N<0>
DP: Lane 0
TBT: TX_0
R3370
470K
R3371
470K
C3374
0.47UF
C3375
0.47UF
TBT_B_D2R_N<0>
TBT_B_D2R_P<0>
TBT_B_D2R_C_P<0>
TBT_B_D2R_C_N<0>
TBT: RX_0
R3394
1K
R3395
1K
NO_XNET_CONNECTION=1
CRITICAL
J3200
DUAL-MDP-K70
F-ANG-TH
SHLD
HPD
CONFIG1
CONFIG2
GND2
ML_LANE3P
ML_LANE3N
GND4
AUX_CHP
AUX_CHN
DP_PWR
GND0
ML_LANE0P
ML_LANE0N
GND1
ML_LANE1P
ML_LANE1N
GND3
ML_LANE2P
ML_LANE2N
RETURN
PORT B
C3379
0.22UF
C3378
0.22UF
DP_TBTPB_ML_C_N<3>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_P<3>
DP_TBTPB_ML_N<3>
TBT: Terminated
R3378
470K
R3379
470K
DP: Lane 3
DP_B_LSX_ML_P<1>
DP_B_LSX_ML_N<1>
DP: Lane 1
C3372
0.22UF
C3373
0.22UF
TBT_B_R2D_C_N<1>
TBT_B_R2D_C_P<1>
TBT_B_R2D_P<1>
TBT_B_R2D_N<1>
DP: Lane 2
TBT: TX_1
R3372
470K
R3373
470K
TBT_B_D2R1_AUXDDC_P
TBT_B_D2R1_AUXDDC_N
TBT: RX_1
J70:514-0824 / J78:514-0831
TBT_B_HPD
TBT_B_CONFIG1_RC
TBT_B_CONFIG2_RC
R3352
1M
R3351
1M
C3394
330PF
C3395
330PF
R3341
100K
C3302
0.01UF
DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V
470k R's for ESD protection
on AC-coupled signals.

SYNC_MASTER=J70_NICK SYNC_DATE=10/16/2013

PAGE TITLE

Thunderbolt Connector B

DRAWING NUMBER 051-00081 SIZE D

Apple Inc.

REVISION 3.0.0

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DDC Pull-Ups

2.2k pull-ups are required by PCH
to indicate active display interface.

DP++ spec violation, should remove!

NOTE: Only DDC_DATA is sensed, so DDC_CLK
pull-ups are unstuffed.

66 39 =PP3V3_S0_DP

DDC Crossbar

Only necessary on dual-port hosts.
On single-port hosts alias TBTPA_DDC to TBTSNK0_DDC.
NEVER SEND AUXCH THROUGH CROSSBAR!

R3485 100K 5% 1/20W MF 201

C3480 0.1UF 20% 10V CERM 402

U3400
TS3DS10224
QFN
CRITICAL

80 28 OUT	DP_TBTPA_DDC_CLK	1 INA+	OUTA1+ 20
80 28 BI	DP_TBTPA_DDC_DATA	2 INA-	OUTA1- 19
			OUTA0+ 18
			OUTA0- 17
		14 SAI	SAO 15
		10 ENB	
80 29 OUT	DP_TBTPB_DDC_CLK	3 INB+	OUTB1+ 6
80 29 BI	DP_TBTPB_DDC_DATA	4 INB-	OUTB1- 7
			OUTB0+ 8
			OUTB0- 9
	TBT_DDC_XBAR_EN	12 SBI	SBO 11
		16 VCC	
		5 GND	21 THRM PAD

R3451 2.2K 1% 1/20W MF 201
R3452 2.2K 1% 1/20W MF 201
R3453 2.2K 1% 1/20W MF 201
R3454 2.2K 1% 1/20W MF 201

DP_TBTSNK1_DDC_CLK — IN 13 80
DP_TBTSNK1_DDC_DATA — BI 13 80
DP_TBTSNK0_DDC_CLK — IN 13 80
DP_TBTSNK0_DDC_DATA — BI 13 80

SAI/SBI = 1: INA == OUTA0, INB == OUTB0
SAI/SBI = 0: INA == OUTB0, INB == OUTA0

Q3400
DMN32D2LFB4
DFN1006B4-3
SYM_VER_2

1	G	
2	S	
3	D	

24 IN TBT_DDC_XBAR_EN_L

SYNC_MASTER=J70_TONY SYNC_DATE=09/13/2013

PAGE TITLE: DDC Crossbar

Apple Inc.

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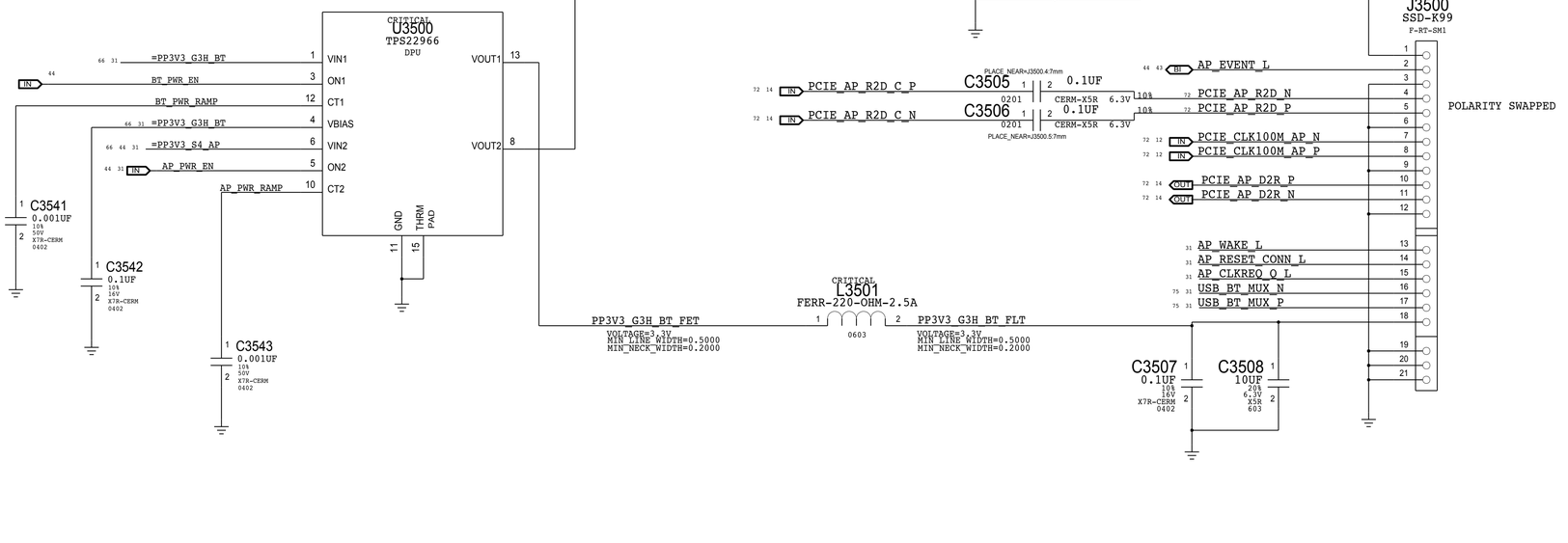
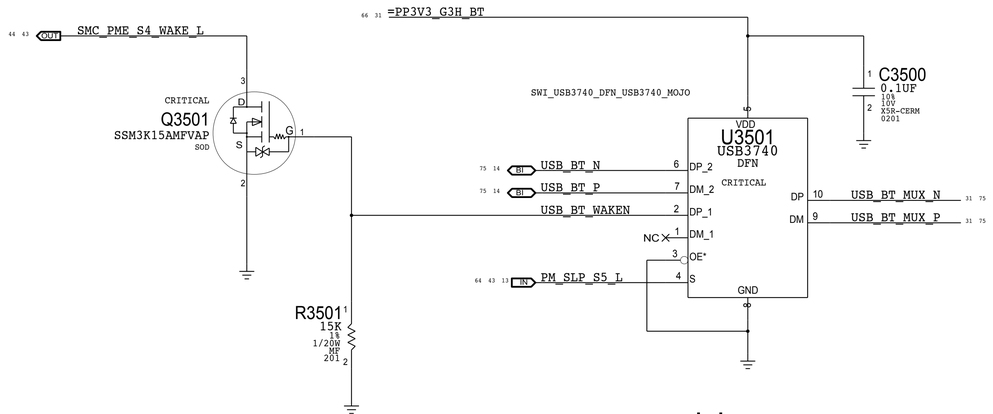
AIRPORT BLUETOOTH

AP & BT Load Switch

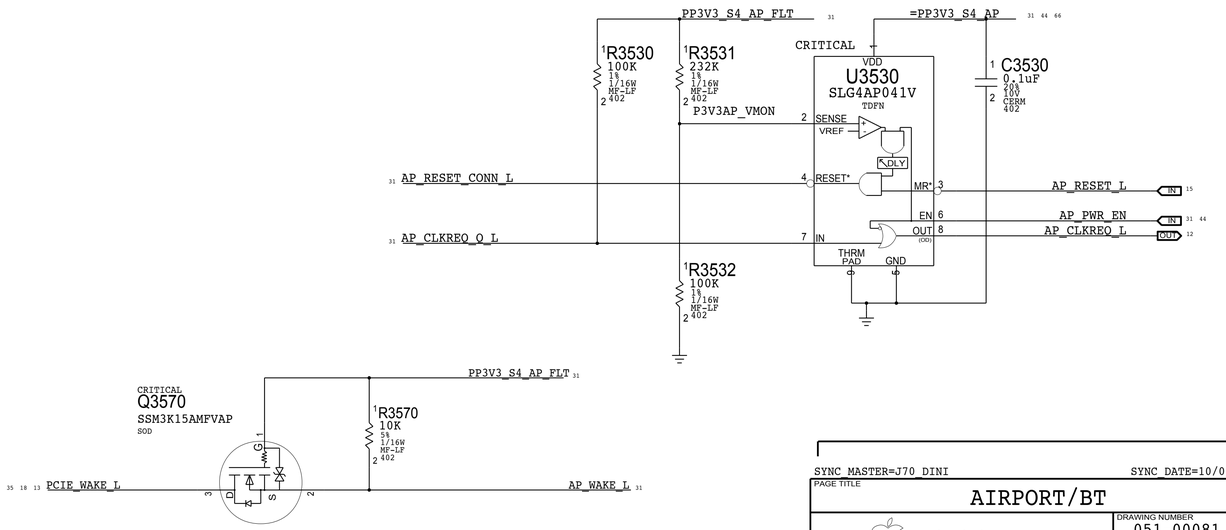
SWITCH	TPS22966
AP SLEW RATE	1185 us
BT SLEW RATE	1185 us
Equation	0.32*Ct + 13.7



Wake from BT in G3H circuit



Supervisor & CLKREQ# Isolation
Delay = 130 ms +/- 20%



SYNC MASTER=J70_DINI SYNC DATE=10/08/2013

PAGE TITLE: AIRPORT/BT

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

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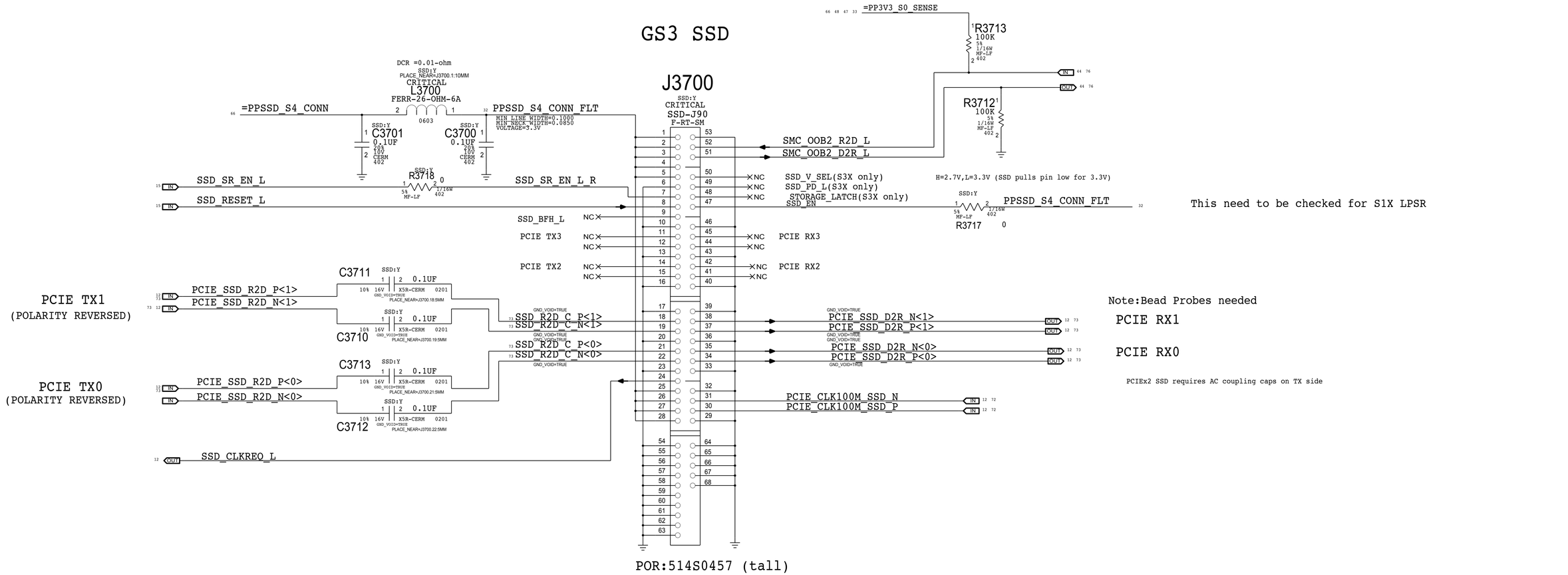
GS3 SSD



This need to be checked for S1X LPSR

Note:Bead Probes needed

PCIE RX1

PCIE RX0

PCIEx2 SSD requires AC coupling caps on TX side

POR:514S0457 (tall)

SYNC_MASTER=J70_DINI	SYNC_DATE=10/14/2013
PAGE TITLE: SSD Connectors	
Apple Inc.	DRAWING NUMBER: 051-00081 SIZE: D
	REVISION: 3.0.0
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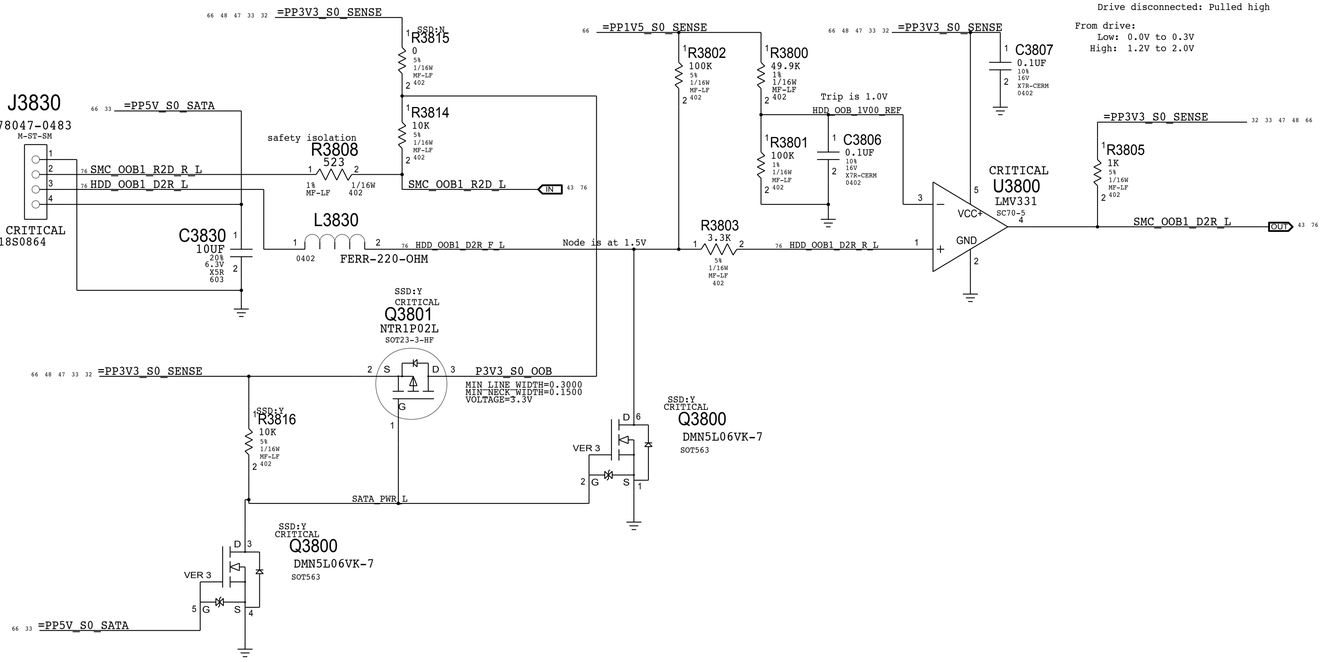
HDD POWER/OOB CONNECTOR

HDD Out-of-Band Temperature Sensing



Notes:

Drive active: Valid signal protocol

Drive asleep: HDD drives HDD_OOB_TEMP low

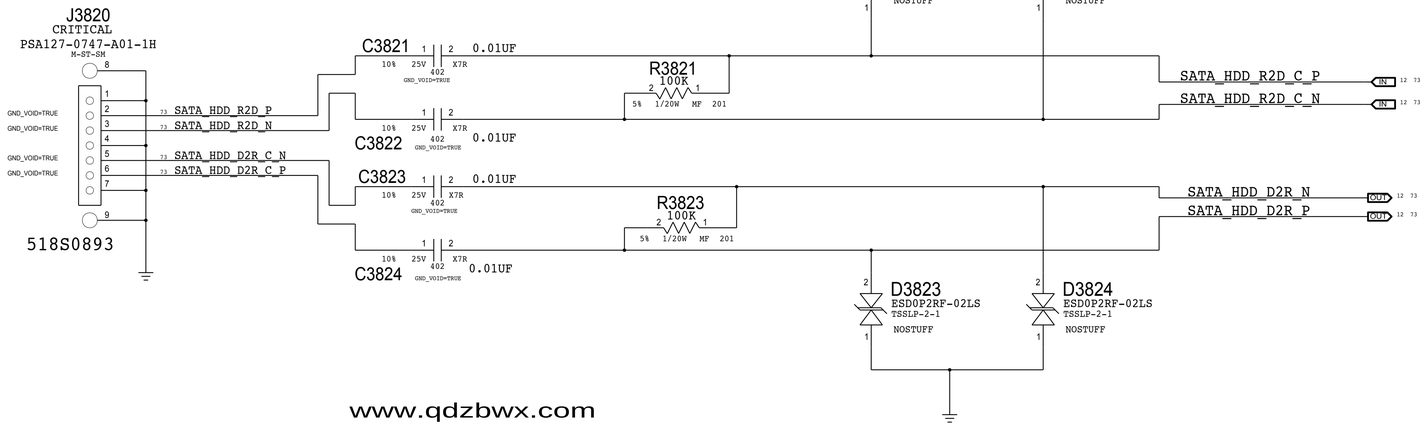
Drive disconnected: Pulled high

From drive:

Low: 0.0V to 0.3V

High: 1.2V to 2.0V

HDD SIGNAL CONNECTOR



SYNC_MASTER=J16_MLB_IG	SYNC_DATE=08/27/2013
PAGE TITLE	HDD Connector
Apple Inc.	DRAWING NUMBER 051-00081 · SIZE D
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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

66 35 34 =PP3V3_ENET_PHY

281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
34 =PP3V3R1V8_CR_VDDIO

ENET_SR_LX 35

=ENET_SR_VFB 35

Internal 1.2V Switching Regulator pins.

=PP1V2_ENET_PHY 35

396mA (1000base-T, Caesar II)

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
ENET_XTALVDDH
C3900 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
PP3V3_ENET_PHY_BIASVDDH
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=3.3V
PP3V3_ENET_PHY_AVDDH
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3916 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
PP1V2_ENET_PHY_AVDDL
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3925 FERR-600-OHM-0.5A SM
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000 VOLTAGE=1.2V
PP1V2_ENET_PHY_PCIEPLL
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402
MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.1500 VOLTAGE=1.2V
PP1V2_ENET_PHY_GPHYPLL
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

66 =PP3V3_S0_ENET
R3942 1K 5% 1/16W MF-LF 402 Current Limiting Resistor

C3950 0.1UF 10% 16V X5R-CERM 0201
C3951 0.1UF 10% 16V X5R-CERM 0201
C3955 0.1UF 10% 16V X5R-CERM 0201
C3956 0.1UF 10% 16V X5R-CERM 0201

72 14 OUT PCIE_ENET_D2R_N
72 14 OUT PCIE_ENET_D2R_P
72 14 IN PCIE_ENET_R2D_C_P
72 14 IN PCIE_ENET_R2D_C_N
35 OUT =ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

OMIT_TABLE
U3900 BCM57766C0KMLG QFN-8X8

72 PCIE_ENET_D2R_C_N	27	PCIE_TXD_N	
72 PCIE_ENET_D2R_C_P	28	PCIE_TXD_P	
72 PCIE_ENET_R2D_P	33	PCIE_RXD_P	
72 PCIE_ENET_R2D_N	34	PCIE_RXD_N	
72 12 IN PCIE_CLK100M_ENET_P	31	PCIE_REFCLK_P	
72 12 IN PCIE_CLK100M_ENET_N	30	PCIE_REFCLK_N	
ENET_VMAIN_PRSNT	58	VMAIN_PRSNT	(IPD-ENET)
36 IN ENET_RESET_L	11	PERST*	(IPD)
12 OUT ENETSD_CLKREQ_L	12	CLKREQ*	(OD)
	3	WAKE*	(OD)
36 13 IN ENET_LOW_PWR	4	LOW_PWR	(IPD)
SMB_ENET_SCL	6	SMB_CLK	
SMB_ENET_SDA	10	SMB_DATA	(IPD-ENETM)
75 34 BI ENET_SCLK	66	SCLK_SPD1000LED*	
75 34 IN ENET_MISO	64	SI/EEDATA	
75 34 BI ENET_MOSI	65	SO_LINKLED*	
75 34 BI ENET_CS_L	63	CS*/EECLK	(IPU)
NC	2	SPD100LED*/SERIAL_DO	(OD)
35 OUT ENET_TRAFFICLED_L	67	TRAFFICLED*/SERIAL_DI	(OD)
74 17 IN ENET_XTAL_IN	18	XTALI	
74 17 OUT ENET_XTAL_OUT	19	XTALO	
75 ENET_RDAC	38	RDAC	
	69	THRM_PAD	(NO IPU OR IPD-ENET)

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

R3965 1.24K 1% 1/16W MF-LF 402

AVDDH	42		
BIASVDDH	48		
XTALVDDH	37		
VDDO	17		
SR_VDD	7		
SR_VDDP	20		
SR_LX	56		
SR_VFB	62		
AVDDL	14		
PCIE_PLLVDDL	15		
GPHY_PLLVDDL	16		
VDDC	13		
	39		
	45		
	51		
	29		
	32		
	36		
	35		
	61		

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

TRD0_P	40	ENETCONN_MDI_P<0>	BI 35 75
TRD0_N	41	ENETCONN_MDI_N<0>	BI 35 75
TRD1_P	44	ENETCONN_MDI_P<1>	BI 35 75
TRD1_N	43	ENETCONN_MDI_N<1>	BI 35 75
TRD2_P	46	ENETCONN_MDI_P<2>	BI 35 75
TRD2_N	47	ENETCONN_MDI_N<2>	BI 35 75
TRD3_P	50	ENETCONN_MDI_P<3>	BI 35 75
TRD3_N	49	ENETCONN_MDI_N<3>	BI 35 75
GPIO_0/CR_ACT_LED*	5	NC	
GPIO_1/LR_OUT	8		
GPIO_2/MEDIA_SENSE	9		ENET_MEDIA_SENSE OUT 15 35
SD_DETECT	1		ENET_SD_DETECT_L IN 36 75
CR_CMD	26	ENET_SD_CMD	SDCONN_CMD IN 36 75
CR_CLK	21	ENET_SD_CLK	SDCONN_CLK OUT 36 75
CR_DATA0	25	ENET_CR_DATA<0>	SDCONN_DATA<0> BI 36 75
CR_DATA1	24	ENET_CR_DATA<1>	SDCONN_DATA<1> BI 36 75
CR_DATA2	23	ENET_CR_DATA<2>	SDCONN_DATA<2> BI 36 75
CR_DATA3	22	ENET_CR_DATA<3>	SDCONN_DATA<3> BI 36 75
CR_DATA4	52	ENET_CR_DATA<4>	SDCONN_DATA<4> BI 36 75
CR_DATA5	53	ENET_CR_DATA<5>	SDCONN_DATA<5> BI 36 75
CR_DATA6	54	ENET_CR_DATA<6>	SDCONN_DATA<6> BI 36 75
CR_DATA7	55	ENET_CR_DATA<7>	SDCONN_DATA<7> BI 36 75
MS_INS*	59	NC	
CR_LED*/CR_BUS_PWR	60	ENET_CR_PWREN	OUT 36
CR_WP*	57		SDCONN_WP IN 36
SR_DISABLE	68		

R3961 33 5% 1/20W MF 201
R3979 33 5% 1/20W MF 201
R3971 33 5% 1/20W MF 201
R3972 33 5% 1/20W MF 201
R3973 33 5% 1/20W MF 201
R3974 33 5% 1/20W MF 201
R3975 33 5% 1/20W MF 201
R3976 33 5% 1/20W MF 201
R3977 33 5% 1/20W MF 201
R3978 33 5% 1/20W MF 201

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

R3981 1K 5% 1/16W MF-LF 402 (See note)

ENET 1.2V SR IS ENABLED IF FLOATING.

ENET supports both active-levels for WP.

PP3V3R1V8_ENET_LR_OUT
MIN_LINE_WIDTH=0.3000 MIN_NECK_WIDTH=0.1500 VOLTAGE=3.3V
MAKE_BASE=TRUE

=PP3V3R1V8_CR_VDDIO 34
C3980 4.7UF 20% 6.3V X5R-CERM1 402
C3981 0.1UF 10% 16V X5R-CERM 0201
C3982 0.1UF 10% 16V X5R-CERM 0201

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE

If ENET switching regulator is used, this pin should have a 1K pull-down to GND

PLACEMENT_NOTE=PLACE R3961 NEAR U3900
PLACEMENT_NOTE=PLACE R3979 NEAR U3900
PLACEMENT_NOTE=PLACE R3971 NEAR U3900
PLACEMENT_NOTE=PLACE R3972 NEAR U3900
PLACEMENT_NOTE=PLACE R3973 NEAR U3900
PLACEMENT_NOTE=PLACE R3974 NEAR U3900
PLACEMENT_NOTE=PLACE R3975 NEAR U3900
PLACEMENT_NOTE=PLACE R3976 NEAR U3900
PLACEMENT_NOTE=PLACE R3977 NEAR U3900
PLACEMENT_NOTE=PLACE R3978 NEAR U3900

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

66 35 34 =PP3V3_ENET_PHY
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC 8, SCK 2, CS* 4, WP* 5, RESET* 3, SI 1, SO 8, GND 7
75 34 IN ENET_SCLK
75 34 IN ENET_CS_L
ENET_MOSI IN 34 75
ENET_MISO OUT 34 75
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=J70_GAREN SYNC_DATE=09/19/2013
PAGE TITLE: ETHERNET PHY (CAESAR IV)
Apple Inc.
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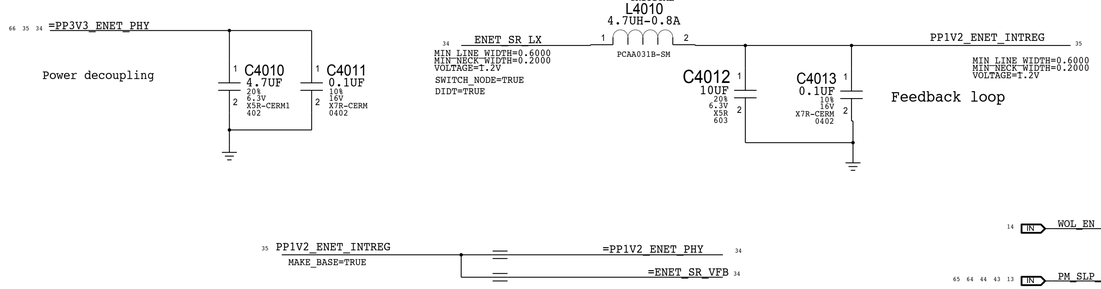
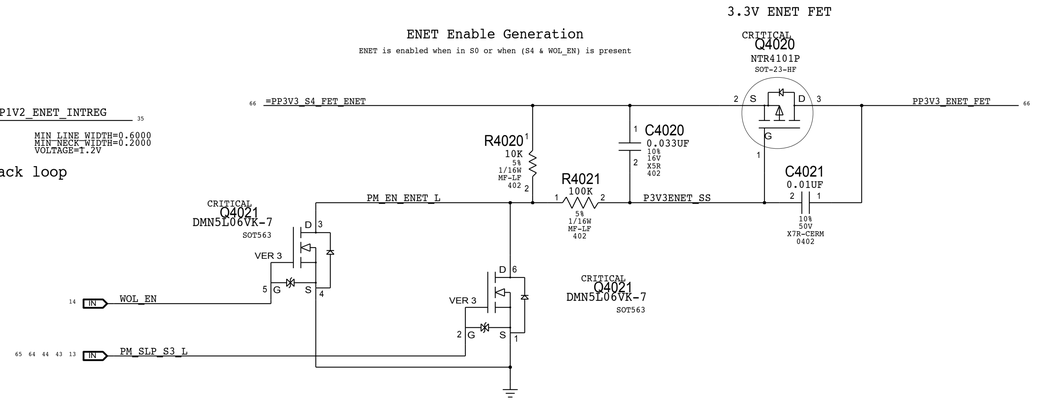
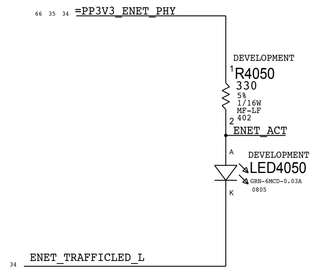
CAESAR IV 1.2V INT.VR CMPTS



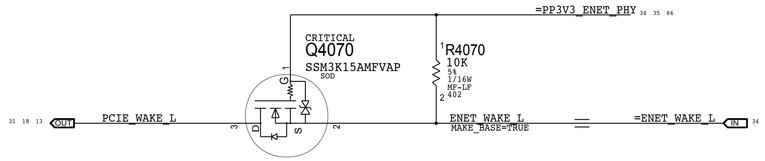
3.3V ENET FET

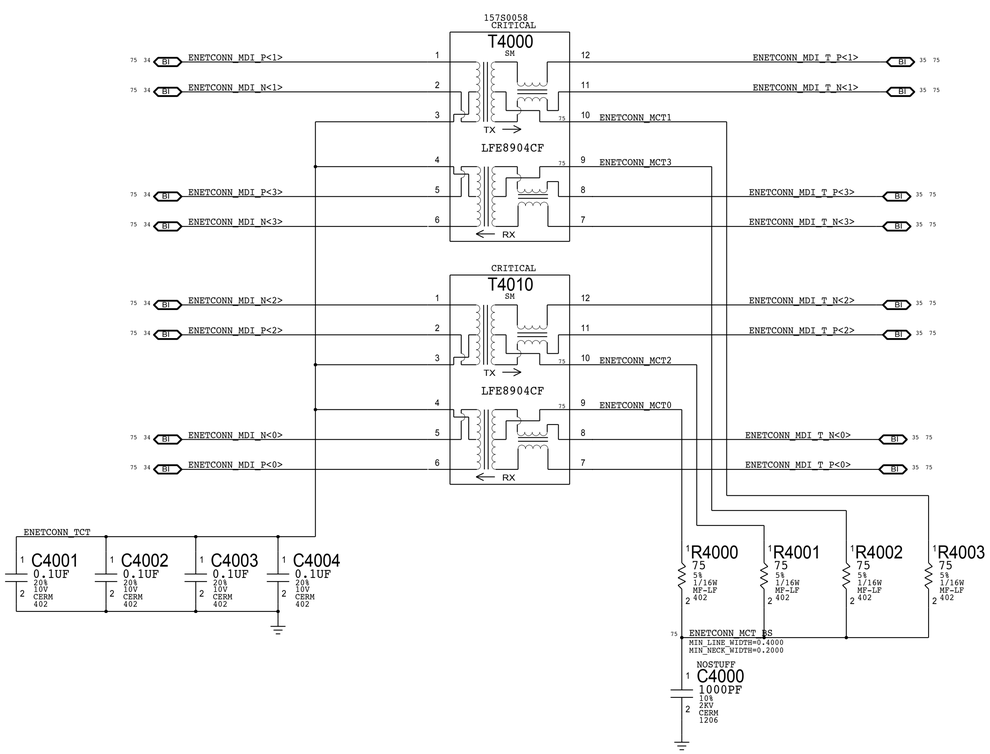


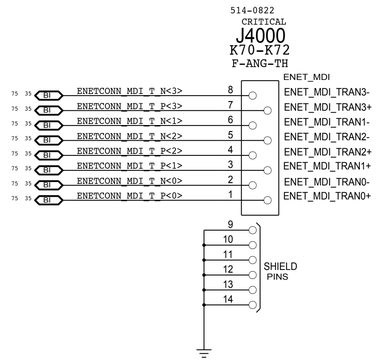
CAESAR IV ACTIVITY LED



CAESAR IV WAKE# ISOLATION







SYNC_MASTER=J16_MLB_IG SYNC_DATE=05/01/2013

PAGE TITLE
Ethernet Support & Connector

Apple Inc.

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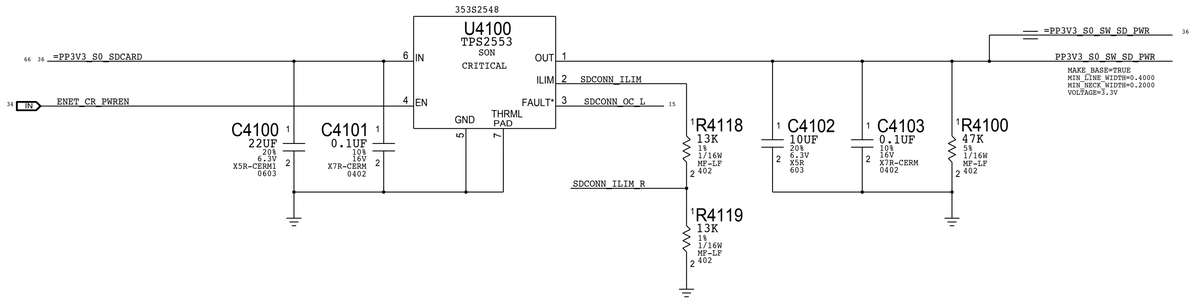
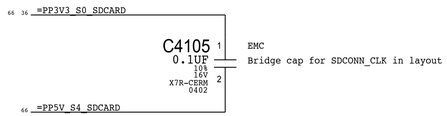
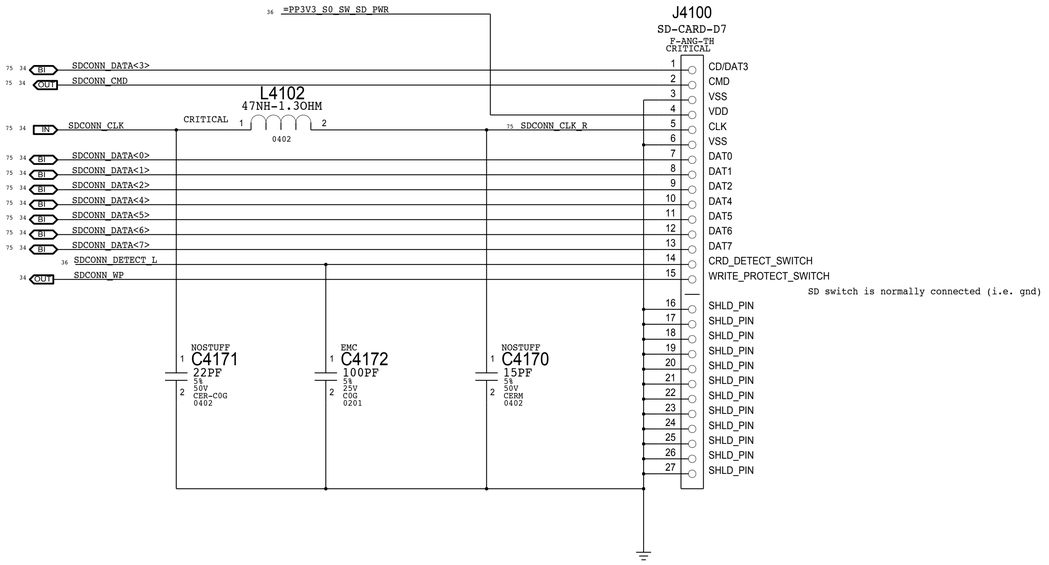
SD CARD 3.3V OVERCURRENT PROTECTION CHIP



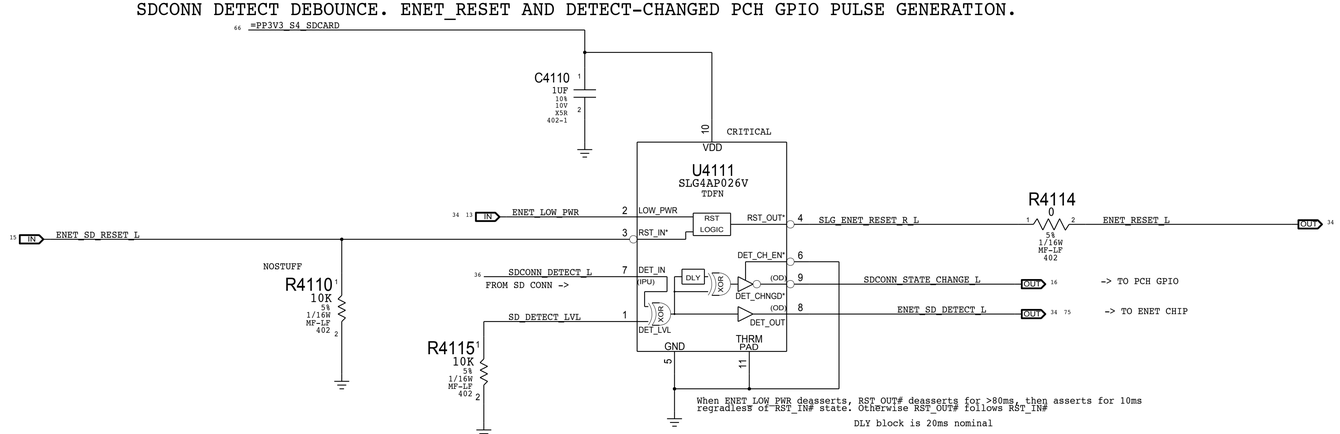


J16:516-0249 / J17:512-0038

SD CARD CONNECTOR



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC_MASTER=J70_GAREN SYNC_DATE=09/23/2013

PAGE TITLE: SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

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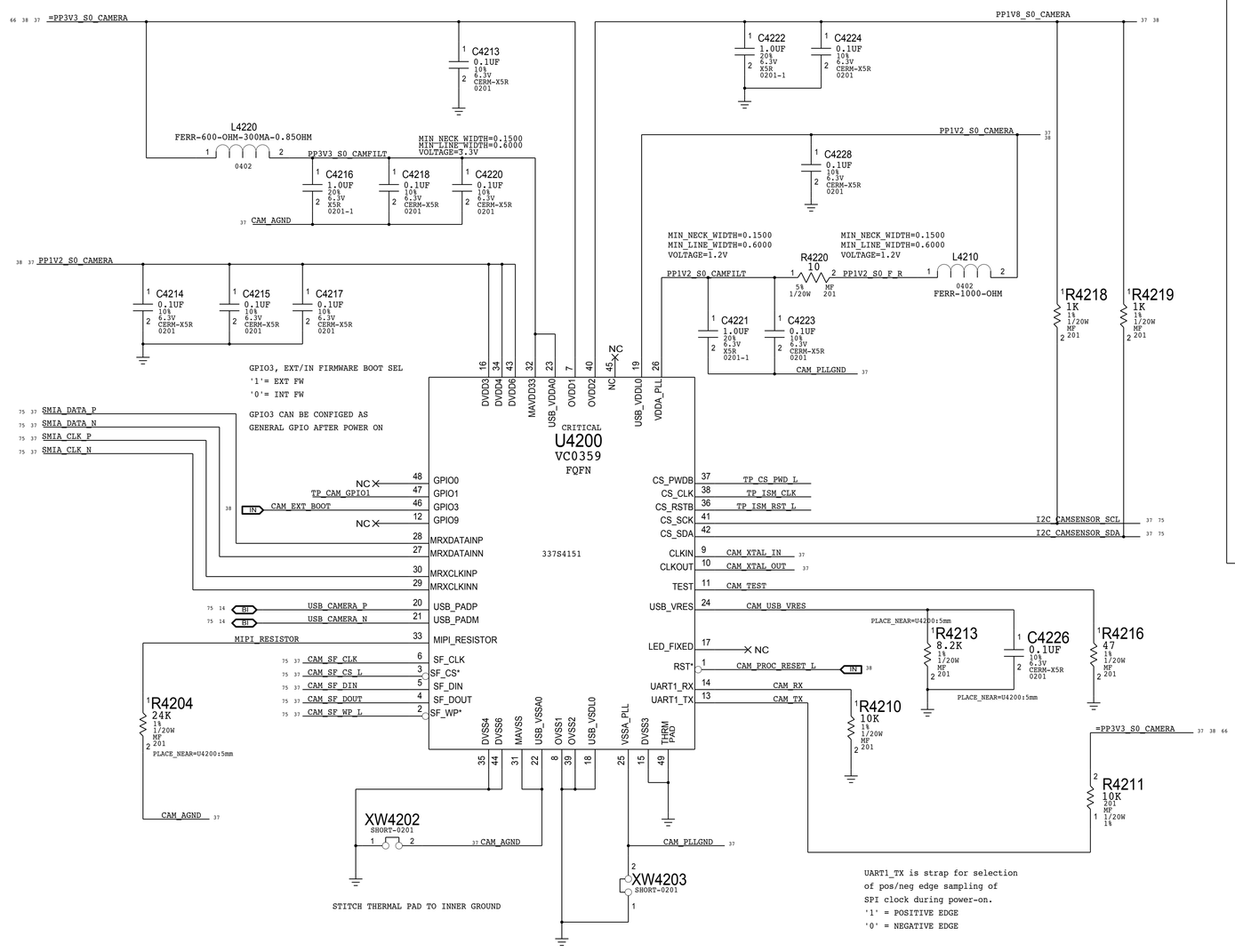
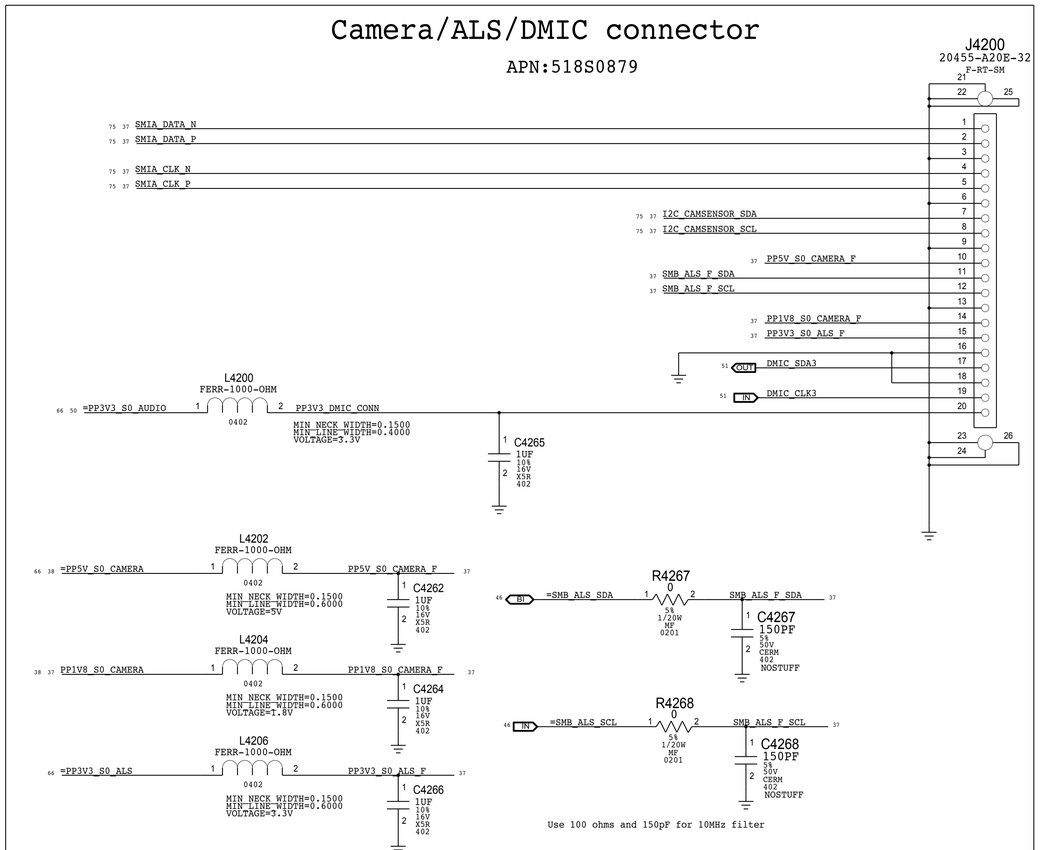
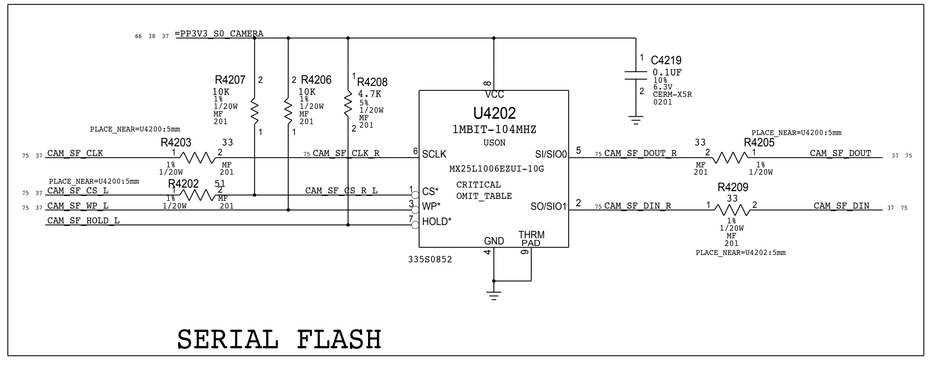
USB CAMERA CONTROLLER



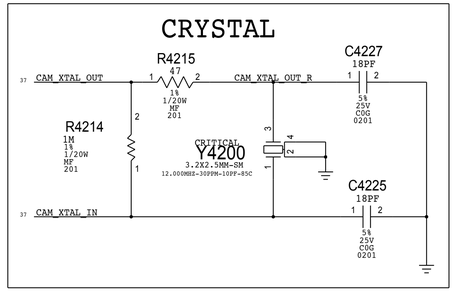
Camera/ALS/DMIC connector

APN:518S0879





SERIAL FLASH



SYNC_MASTER=J70_GAREN	SYNC_DATE=02/05/2014
PAGE TITLE	Camera Controller
Apple Inc.	DRAWING NUMBER 051-00081 · SIZE D
	REVISION 3.0.0
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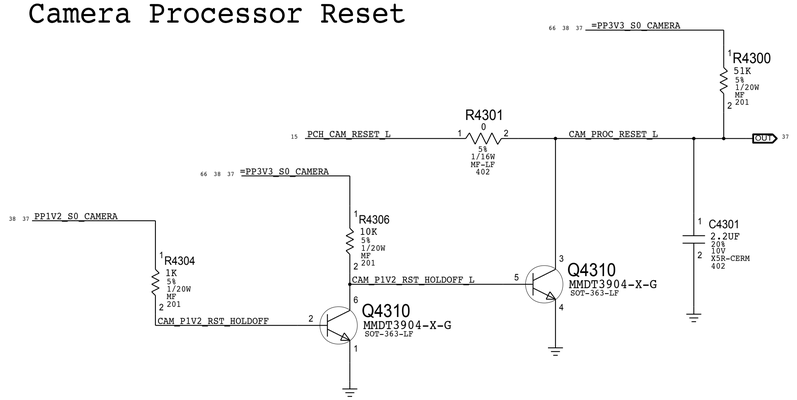
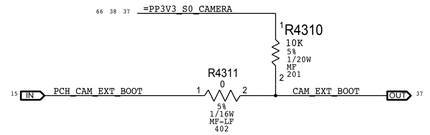
Camera Processor Reset

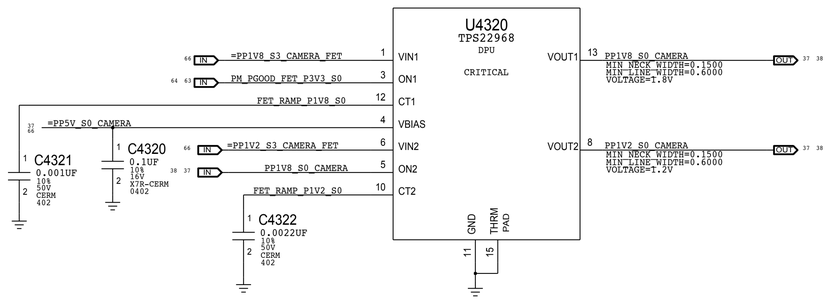


Camera Processor ExtBoot Cntl



1.8V S0 and 1.2V S0 Load Switch

POWER SEQUENCE
3.3V => 1.8V => 1.2V
Enable 1.8V camera rail when 3.3V S0 rail is on
Enable 1.2V camera rail when 1.8V S0 rail is on



Capacitor Values Found Using
Slew Rate(us/V) = 0.32*CT(pF) + 13.7

Rise Times:
1.8V S0 -- 1000 pF -- 600 us
1.2V S0 -- 2200 pF -- 861 us

SYNC_MASTER=J70_GAREN SYNC_DATE=10/24/2013

PAGE TITLE
Camera Controller Support

Apple Inc.

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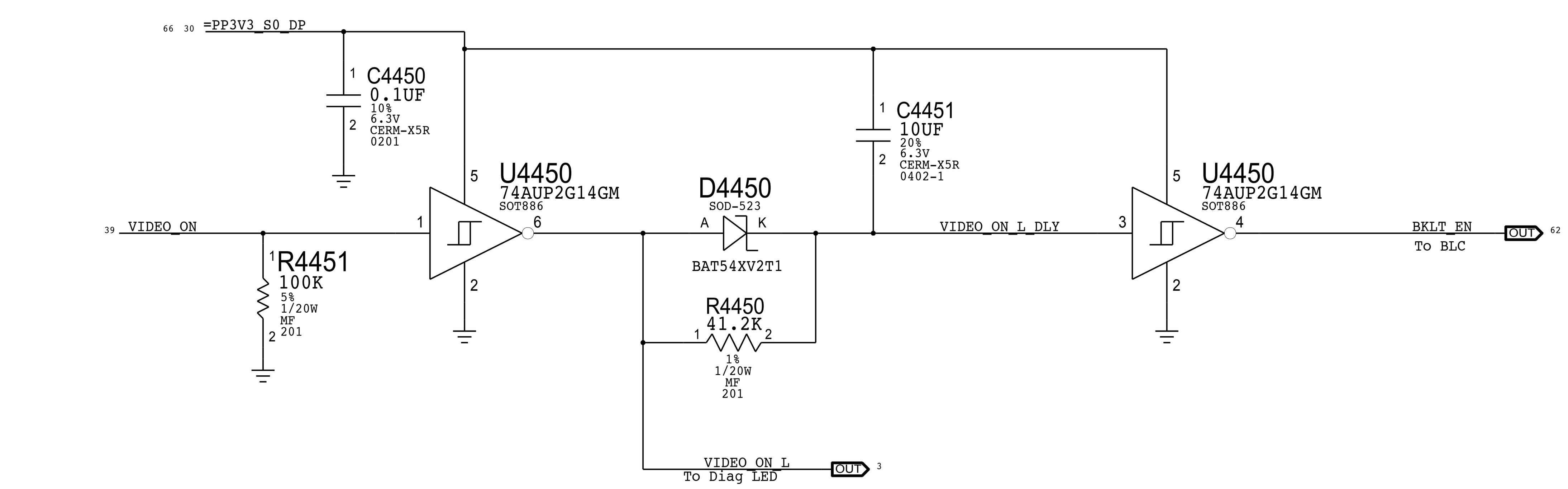
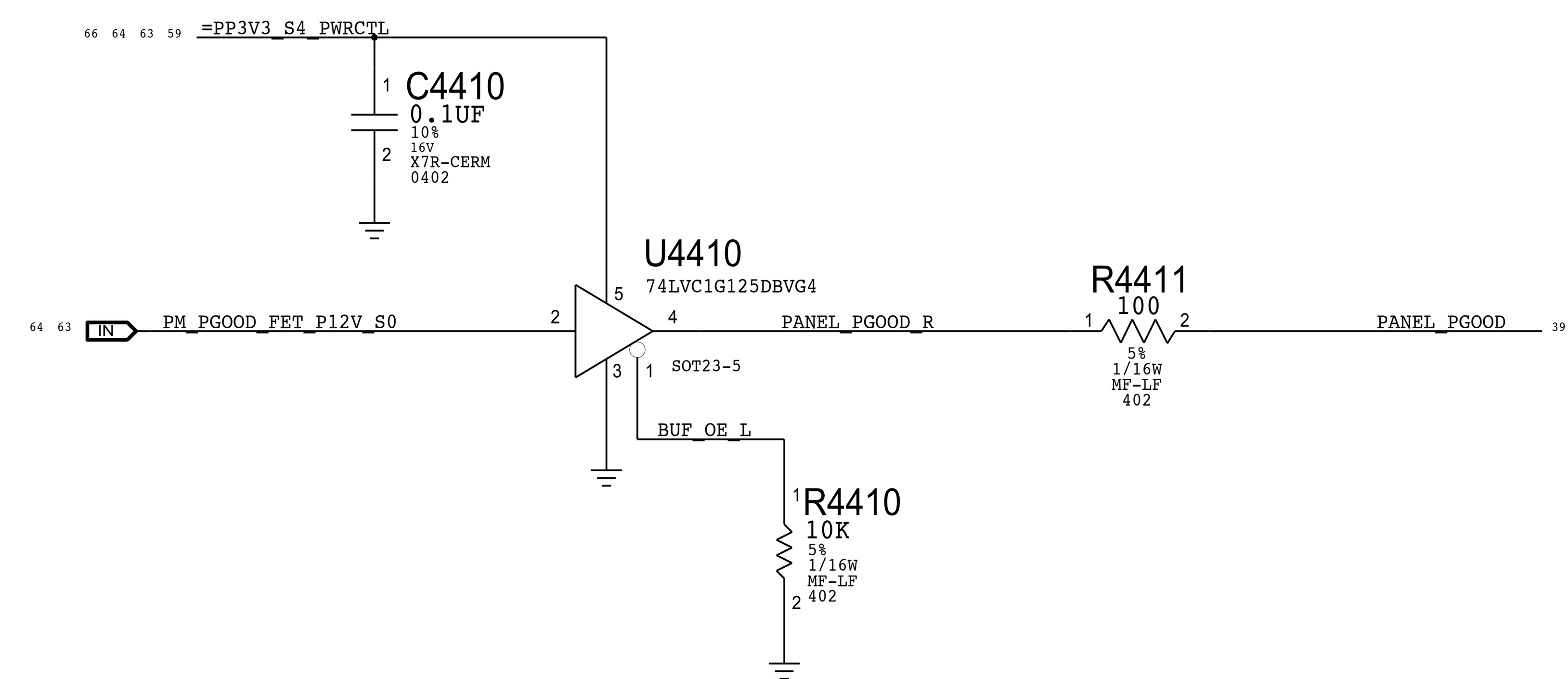
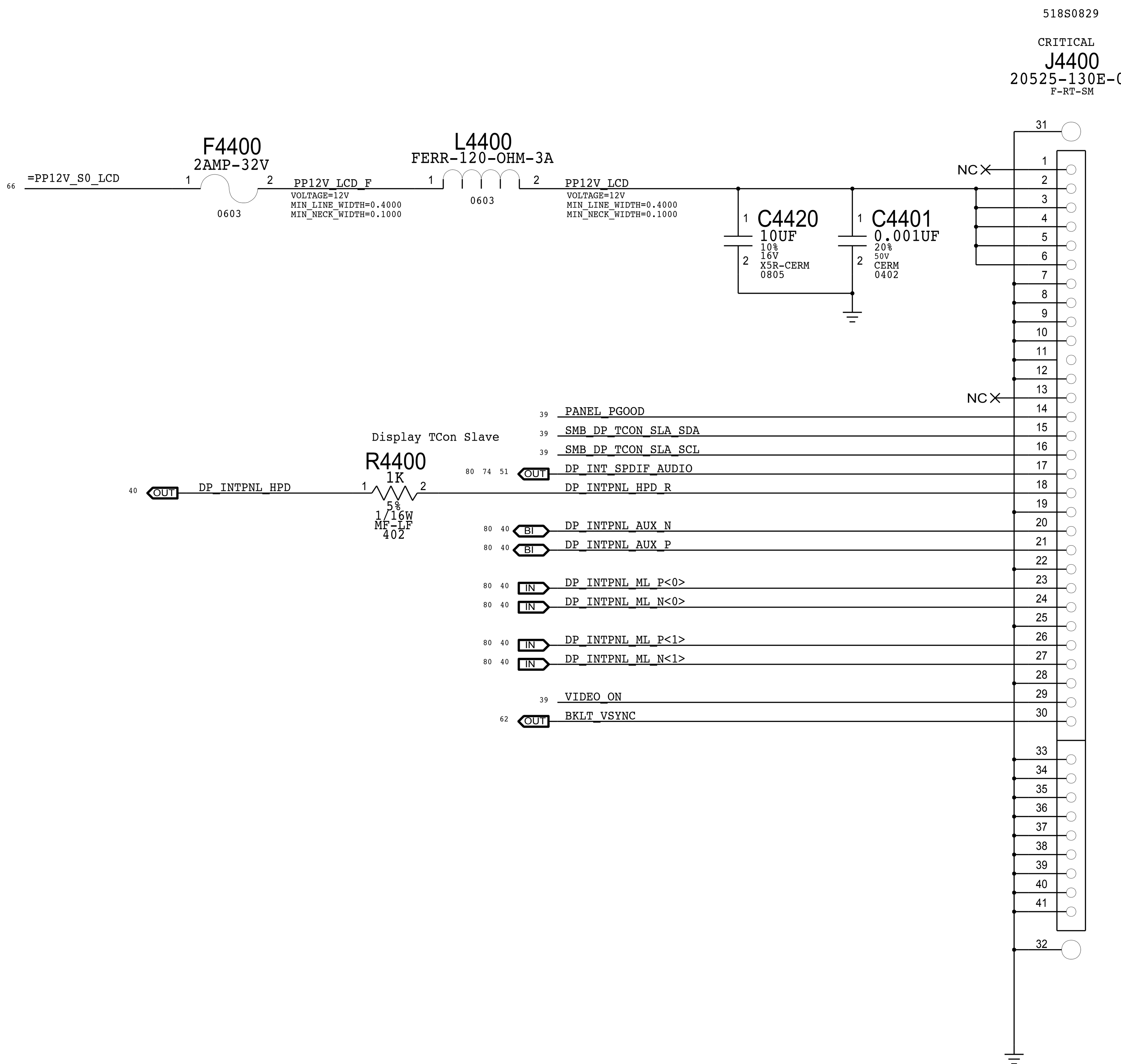
Backlight Control

Delay applies only on a L->H transition on VIDEO_ON. This guarantees video is valid before the backlight is enabled.
On a H->L transition, output follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video



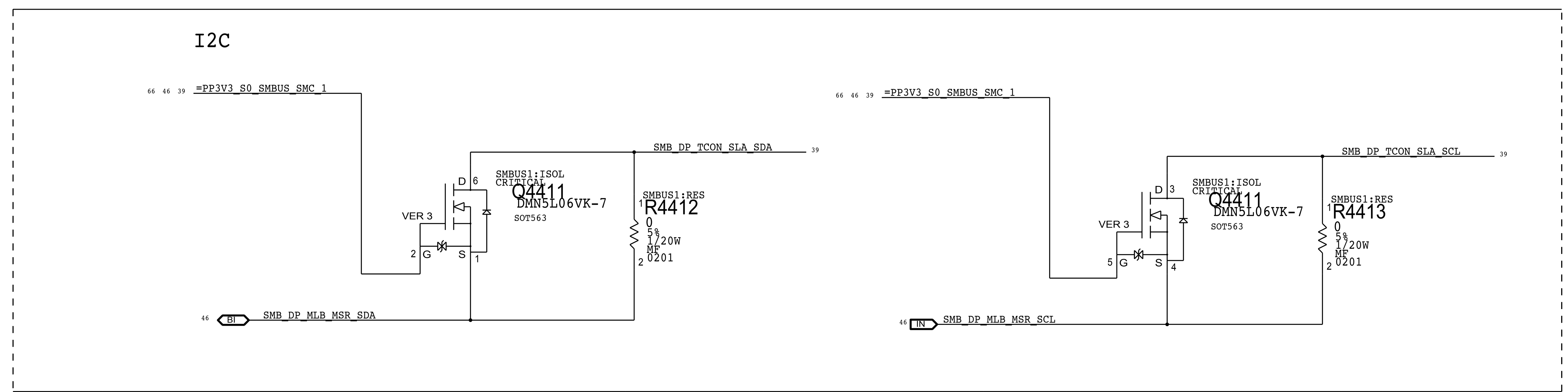


Internal DP Connector



518S0829
CRITICAL
J4400
20525-130E-01
F-RT-SM
F4400
2AMP-32V
L4400
FERR-120-OHM-3A
=PP12V_S0_LCD
PP12V_LCD_F
PP12V_LCD
C4420
10UF
C4401
0.001UF
Display TCon Slave
R4400
1K
DP_INTPNL_HPD
PANEL_PGOOD
SMB_DP_TCON_SLA_SDA
SMB_DP_TCON_SLA_SCL
DP_INT_SPDIF_AUDIO
DP_INTPNL_HPD_R
DP_INTPNL_AUX_N
DP_INTPNL_AUX_P
DP_INTPNL_ML_P<0>
DP_INTPNL_ML_N<0>
DP_INTPNL_ML_P<1>
DP_INTPNL_ML_N<1>
VIDEO_ON
BKLT_VSYNC

SMBus Isolation



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SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE: Internal DP Support

DRAWING NUMBER: 051-00081 SIZE: D

Apple Inc.

REVISION: 3.0.0

BRANCH

NC aliases

26	IN	DP_TBTSRC_ML_P<2>	NC_DP_TBTSRC_ML_P<2>	NO_TEST=1	MAKE_BASE=TRUE
26	IN	DP_TBTSRC_ML_N<2>	NC_DP_TBTSRC_ML_N<2>	NO_TEST=1	MAKE_BASE=TRUE
26	IN	DP_TBTSRC_ML_P<3>	NC_DP_TBTSRC_ML_P<3>	NO_TEST=1	MAKE_BASE=TRUE
26	IN	DP_TBTSRC_ML_N<3>	NC_DP_TBTSRC_ML_N<3>	NO_TEST=1	MAKE_BASE=TRUE
5	IN	DP_INT_ML_P<2>	NC_DP_INT_ML_P<2>	NO_TEST=1	MAKE_BASE=TRUE
5	IN	DP_INT_ML_N<2>	NC_DP_INT_ML_N<2>	NO_TEST=1	MAKE_BASE=TRUE
5	IN	DP_INT_ML_P<3>	NC_DP_INT_ML_P<3>	NO_TEST=1	MAKE_BASE=TRUE
5	IN	DP_INT_ML_N<3>	NC_DP_INT_ML_N<3>	NO_TEST=1	MAKE_BASE=TRUE

40 13 DP_INT_HPD

R4500
100K
5%
1/20W
MF
201

=PP3V3_S0_INTDPMUX 40 66

C4568 0.1UF 10% 6.3V CERM-X5R 0201

C4569 0.1UF 10% 6.3V CERM-X5R 0201

U4500
PI3VEDP212
TQFN
CRITICAL

VDD: 29, 20, 16, 12, 6, 3

80 5	IN	DP_INT_ML_P<0>	31	D0+A
80 5	IN	DP_INT_ML_N<0>	30	D0-A
80 5	IN	DP_INT_ML_P<1>	27	D1+A
80 5	IN	DP_INT_ML_N<1>	26	D1-A
80 5	BI	DP_INT_AUX_P	19	AUX+A
80 5	BI	DP_INT_AUX_N	18	AUX-A
40 13	OUT	DP_INT_HPD	17	HPD_A
80 26		DP_TBTSRC_ML_P<0>	25	D0+B
80 26		DP_TBTSRC_ML_N<0>	24	D0-B
80 26		DP_TBTSRC_ML_P<1>	23	D1+B
80 26		DP_TBTSRC_ML_N<1>	22	D1-B
80 26	BI	DP_TBTSRC_AUX_P	15	AUX+B
80 26	BI	DP_TBTSRC_AUX_N	14	AUX-B
26	OUT	DP_TBTSRC_HPD	13	HPD_B
		PD is on the CR page		
50 13	IN	DP_TBT_SEL	10	SEL
			32	AUX_SEL
			11	HPD_SEL

THMPAD: 33, 28, 21 → GND

D0+	1	80 DP_INTPNL_ML_C_P<0>	C4500 0.1UF	DP_INTPNL_ML_P<0>	OUT 39 80
D0-	2	80 DP_INTPNL_ML_C_N<0>	C4501 0.1UF	DP_INTPNL_ML_N<0>	OUT 39 80
D1+	4	80 DP_INTPNL_ML_C_P<1>	C4502 0.1UF	DP_INTPNL_ML_P<1>	OUT 39 80
D1-	5	80 DP_INTPNL_ML_C_N<1>	C4503 0.1UF	DP_INTPNL_ML_N<1>	OUT 39 80
AUX+	6	DP_INTPNL_AUX_C_P	C4504 0.1UF	DP_INTPNL_AUX_P	BI 39 80
AUX-	7	DP_INTPNL_AUX_C_N	C4505 0.1UF	DP_INTPNL_AUX_N	BI 39 80
HPD	8	DP_INTPNL_HPD	IN 39		

R4502 100K 5% 1/20W MF 201

R4503 100K 5% 1/20W MF 201

=PP3V3_S0_INTDPMUX 40 66

SYNC_MASTER=J70_TONY SYNC_DATE=09/05/2013

PAGE TITLE: Internal DP MUXing

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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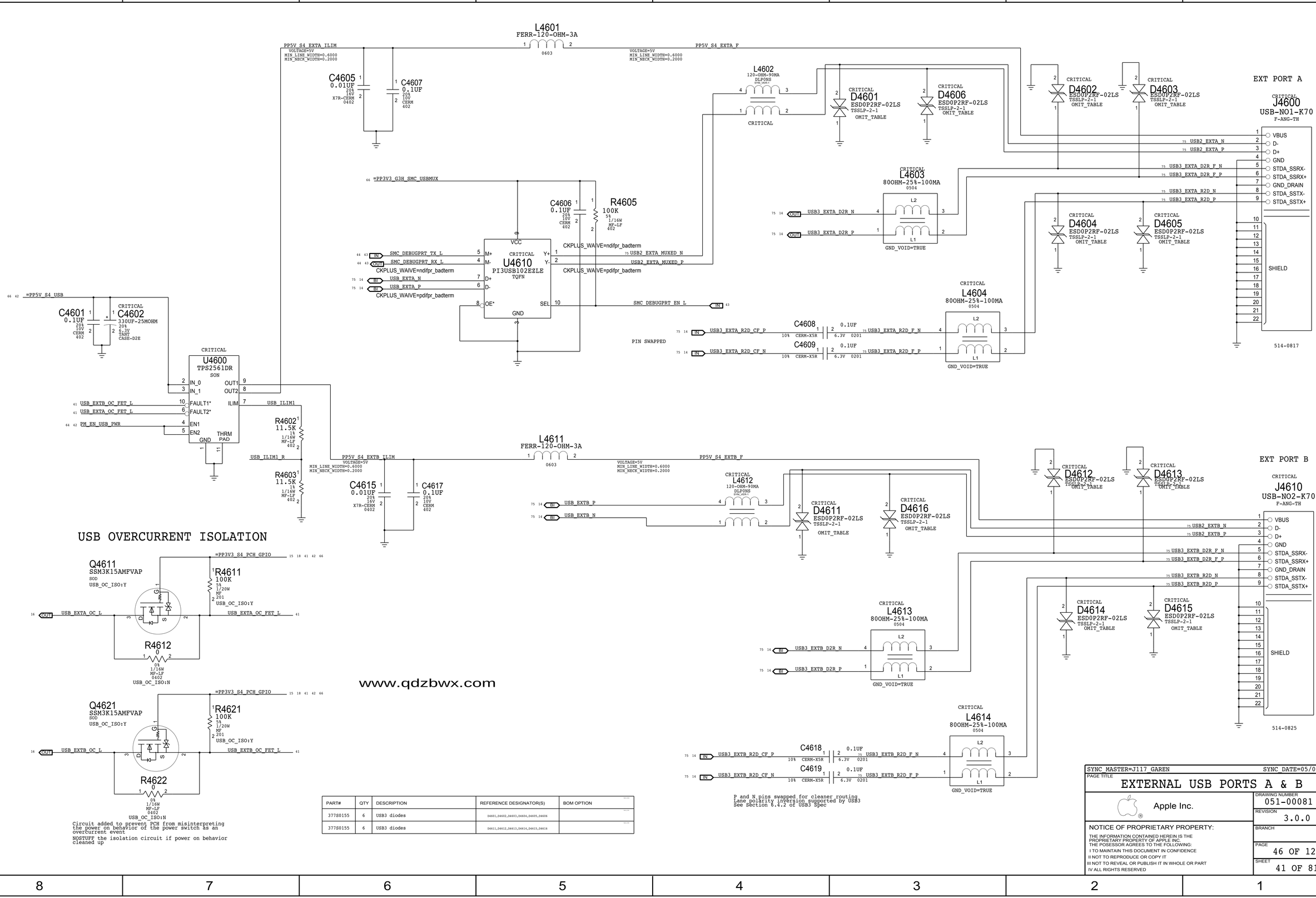

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
377S0155	6	USB3 diodes	D4601,D4602,D4603,D4604,D4605,D4606	
377S0155	6	USB3 diodes	D4611,D4612,D4613,D4614,D4615,D4616	

SYNC_MASTER=J117_GAREN SYNC_DATE=05/05/2014

PAGE TITLE

EXTERNAL USB PORTS A & B

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

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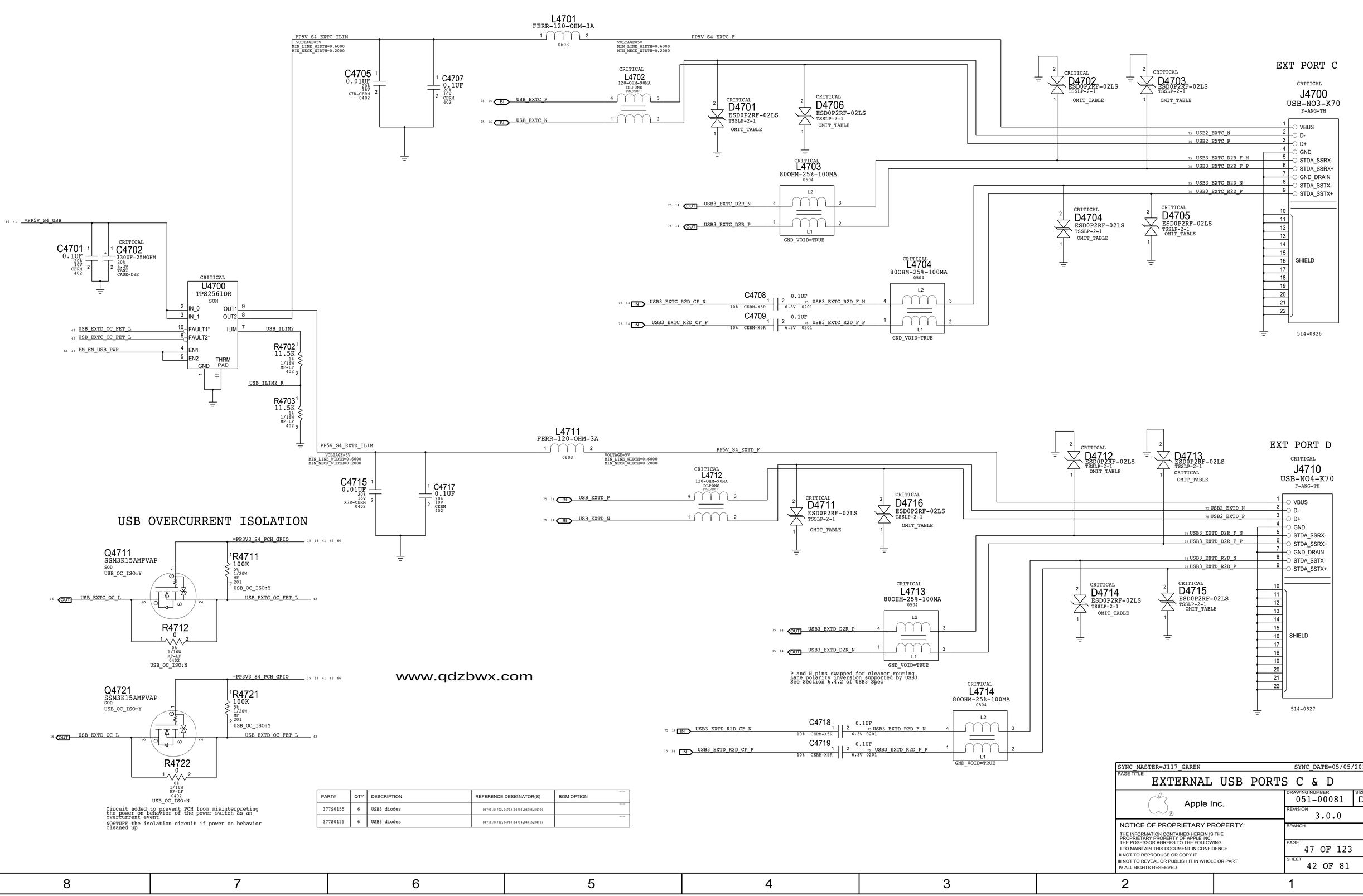

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
377S0155	6	USB3 diodes	D4701,D4702,D4703,D4704,D4705,D4706	
377S0155	6	USB3 diodes	D4711,D4712,D4713,D4714,D4715,D4716	

SYNC_MASTER=J117_GAREN SYNC_DATE=05/05/2014

PAGE TITLE

EXTERNAL USB PORTS C & D

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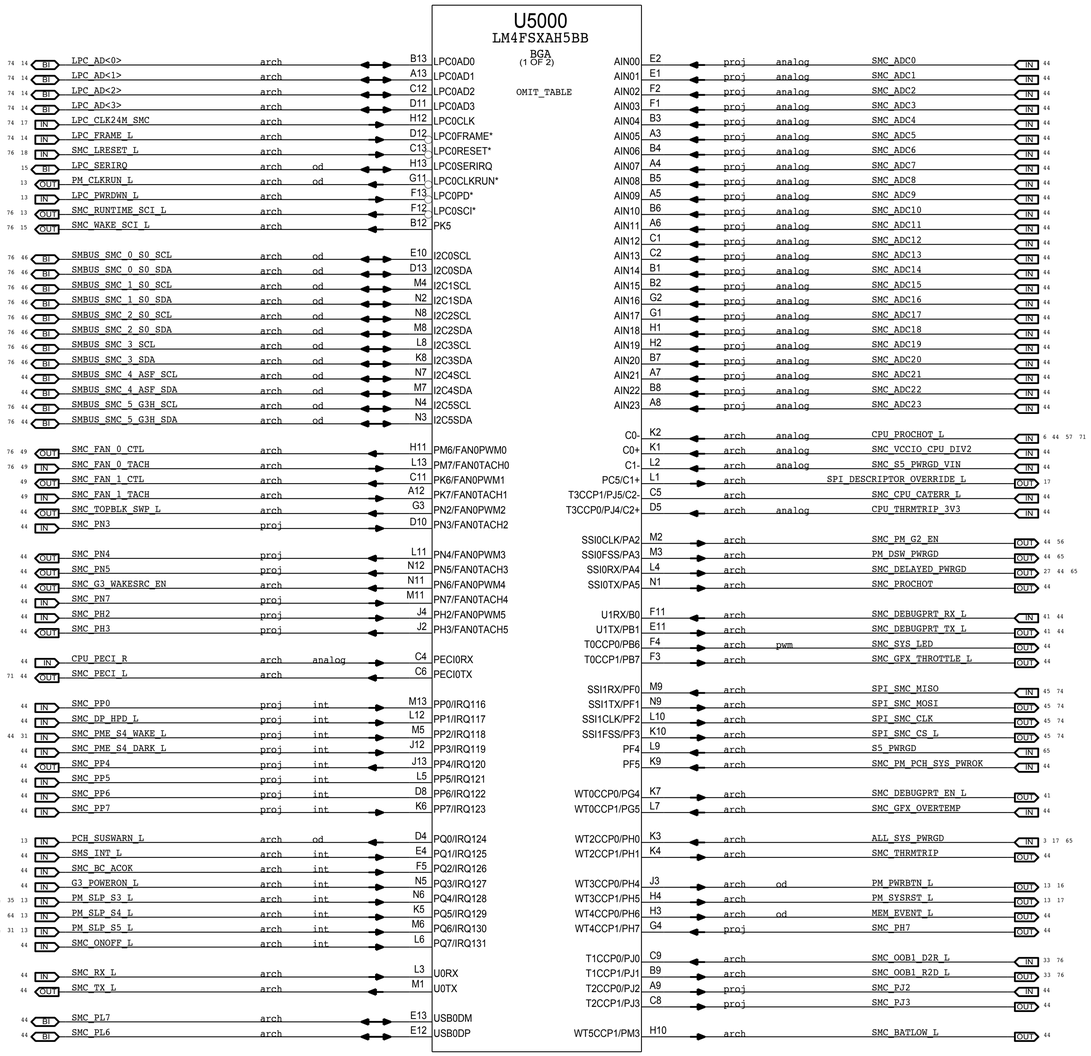
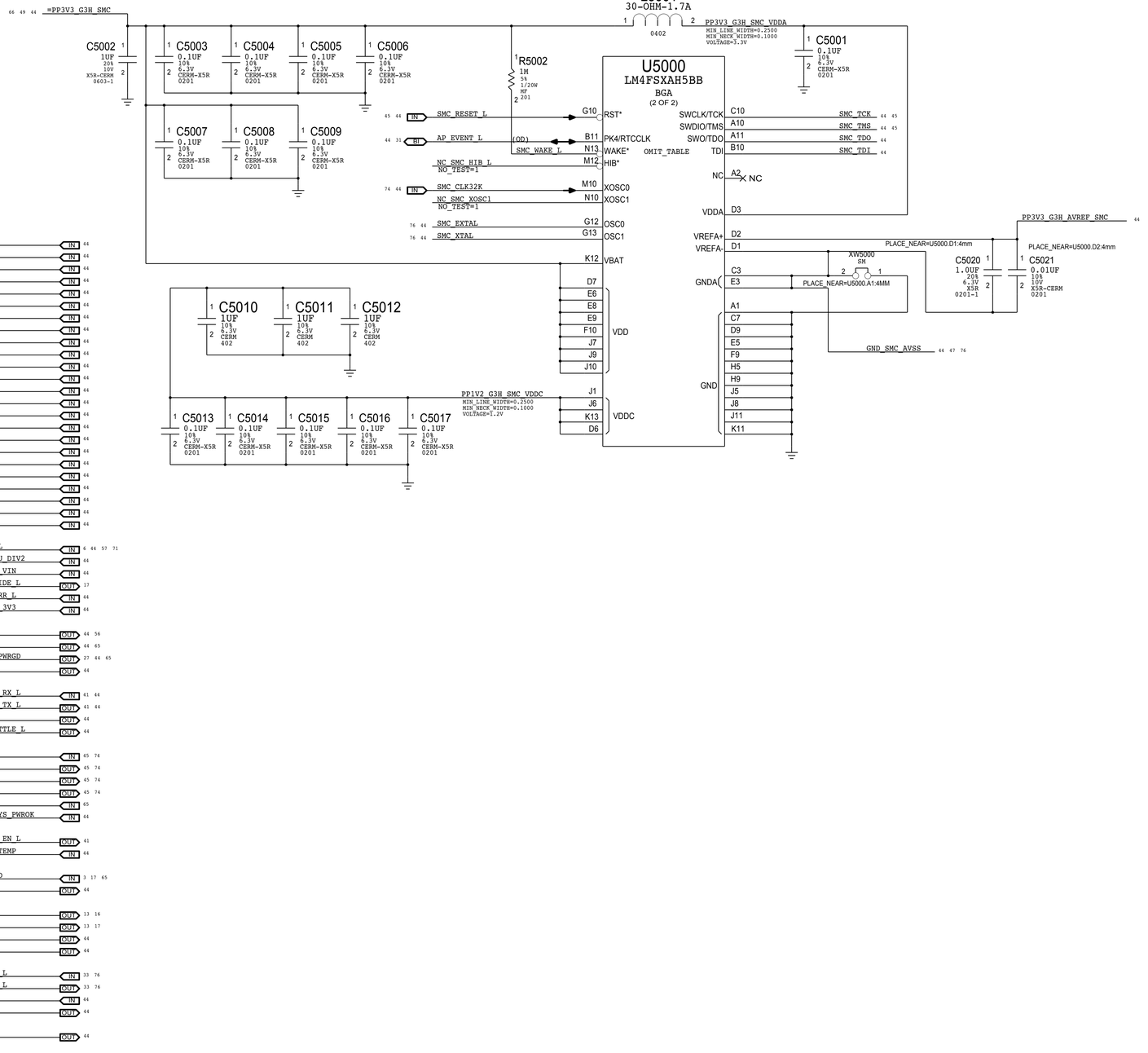
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SYNC_MASTER=J70_NICK	SYNC_DATE=09/24/2013
PAGE TITLE	SMC
Apple Inc.	DRAWING NUMBER 051-00081
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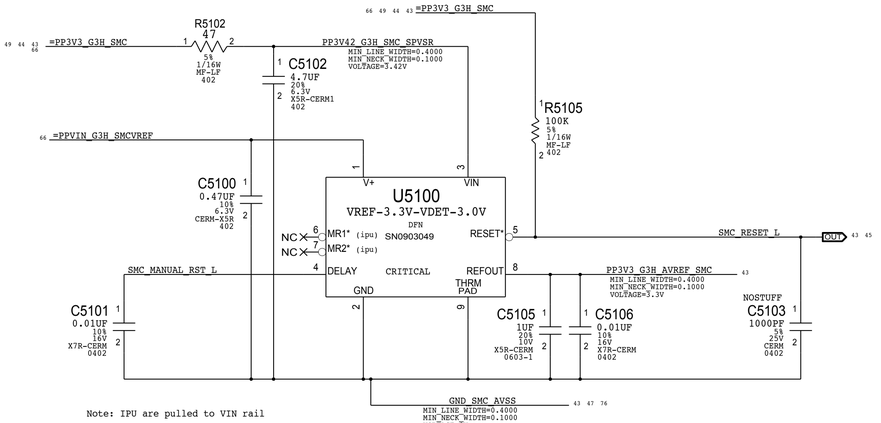
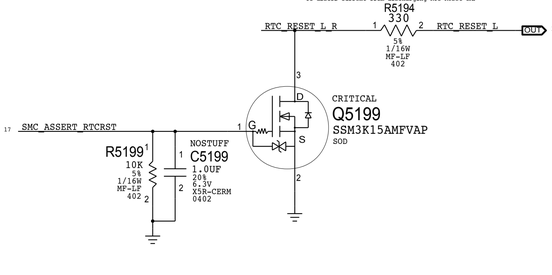
SMC Supervisor and AVREF Supply



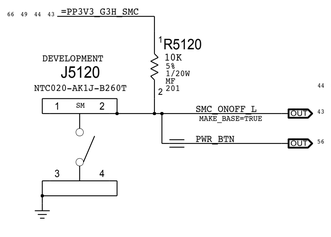
Note: IPU are pulled to VIN rail

SMC Controlled RTC Reset

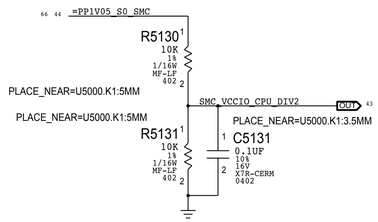
To absorb current from discharging RTC Reset CAP



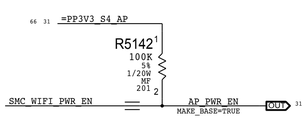
Power Button



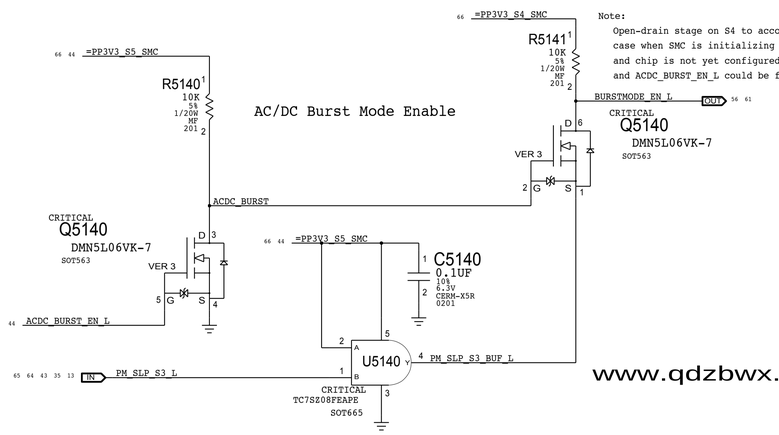
Comparator Reference



SMC control for AirPort power



AC/DC Burst Mode Enable



Note:
Open-drain stage on S4 to account case when SMC is initializing in S5, and chip is not yet configured. and ACDC_BURST_EN_L could be floating.

ADC Channel Aliases

SMC_ADC0	VSNS_P12VG3H
SMC_ADC1	ISNS_P12VG3H
SMC_ADC6	VSNS_P1V2_S3_DDR
SMC_ADC7	ISNS_P1V2_S3_DDR
SMC_ADC10	VSNS_CPUVCC
SMC_ADC11	ISNS_CPUVCC
SMC_ADC20	VSNS_P3V3_SSD
SMC_ADC21	ISNS_SSDS4

Unused ADC Channels

SMC_ADC2	NC_VSNS_P12VS0_GPUCORE	NO_TEST=1
SMC_ADC3	NC_ISNS_P12VS0_GPUCORE	NO_TEST=1
SMC_ADC4	NC_VSNS_PVDDQS0	NO_TEST=1
SMC_ADC5	NC_ISNS_PVDDQS0	NO_TEST=1
SMC_ADC8	NC_VSNS_P12VS0_FBVDDQ	NO_TEST=1
SMC_ADC9	NC_ISNS_P12VS0_FBVDDQ	NO_TEST=1
SMC_ADC12	NC_VSNS_GPUCORE_ALT	NO_TEST=1
SMC_ADC13	NC_ISNS_GPUCORE_ALT	NO_TEST=1
SMC_ADC14	NC_VSNS_HDDS0	NO_TEST=1
SMC_ADC15	NC_ISNS_HDDS0	NO_TEST=1
SMC_ADC16	NC_SMC_ADC16	NO_TEST=1
SMC_ADC17	NC_SMC_ADC17	NO_TEST=1
SMC_ADC18	NC_VSNS_P1V05S0_PCH	NO_TEST=1
SMC_ADC19	NC_ISNS_P3V3S4_AP	NO_TEST=1
SMC_ADC22	NC_SMC_ADC22	NO_TEST=1
SMC_ADC23	NC_SMC_ADC23	NO_TEST=1

Project-specific Aliases

SMC_PN5	ACDC_BURST_EN_L
SMC_PJ3	SMC_OOB2_R2D_L
SMC_PJ2	SMC_OOB2_D2R_L
SMC_PP0	SMC_ACDC_ID
SMC_PH2	SMC_ASSERT_RTCRST
SMC_PL6	SMC_WIFI_PWR_EN
SMC_PH3	SMC_PCH_SUSACK_L
SMC_PL7	BT_PWR_EN

Unused Project-specific

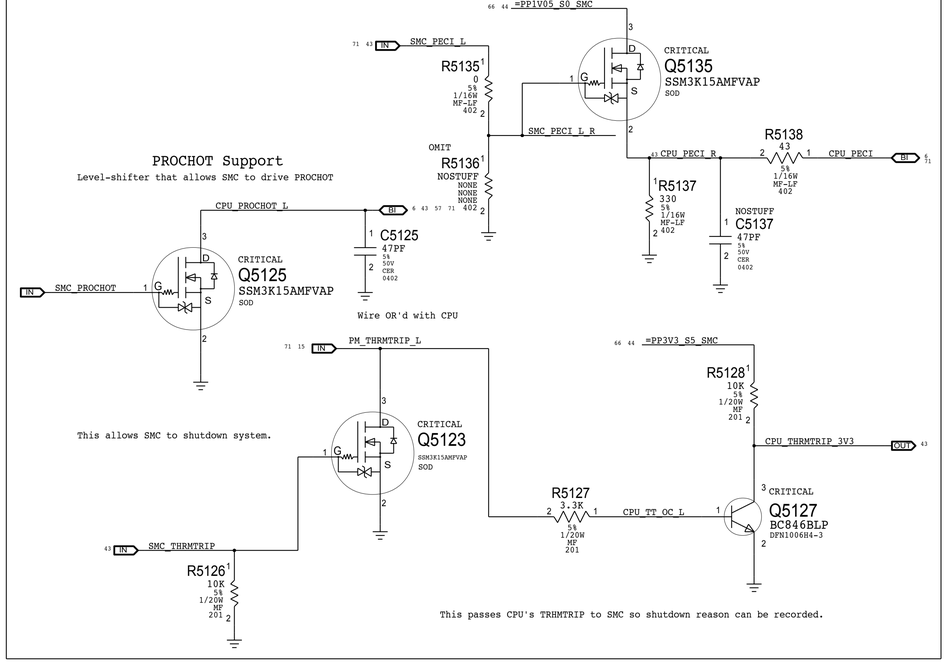
SMC_S5_PWRGD_VIN	NC_SMC_S5_PWRGD_VIN	
SMC_PN3	NC_SMC_PN3	
SMC_PN4	NC_SMC_PN4	
SMC_PP4	NC_SMC_S4_WAKESRC_EN	
SMC_PN7	NC_SMC_PN7	
SMC_PP5	NC_SMC_PP5	
SMC_PP6	NC_SMC_PP6	
SMC_PP7	NC_SMC_PP7	
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	
SMC_PH7	NC_SMC_PH7	
TP for access if ZPB re-intstated		
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	
SMC_BATLOW_L	NC_SMC_BATLOW_L	
SMC_GFX_THROTTLE_L	NC_SMC_GFX_THROTTLE_L	
SMC_GFX_OVERTEMP	NC_SMC_GFX_OVERTEMP	
MEM_EVENT_L	NC_MEM_EVENT_L	

All: MAKE_BASE=TRUE, NO_TEST=1

Platform Thermal Control

PECI Support

Level-shifter that allows SMC to drive PECI
Place this circuit near the Tee point to minimize reflections



PROCHOT Support

Level-shifter that allows SMC to drive PROCHOT

Wire OR'd with CPU

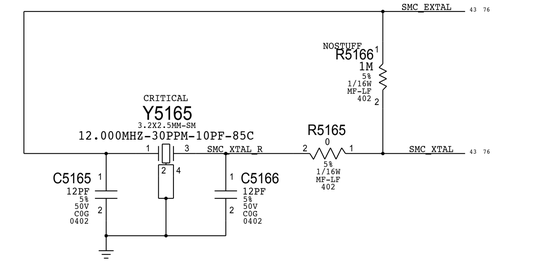
This allows SMC to shutdown system.

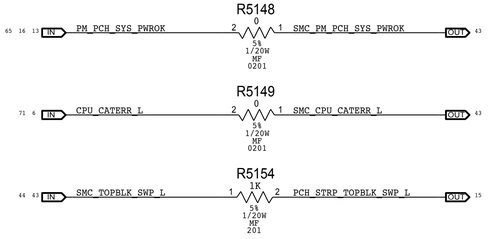
This passes CPU's TRHMTRIP to SMC so shutdown reason can be recorded.

SMC 32KHz Clock

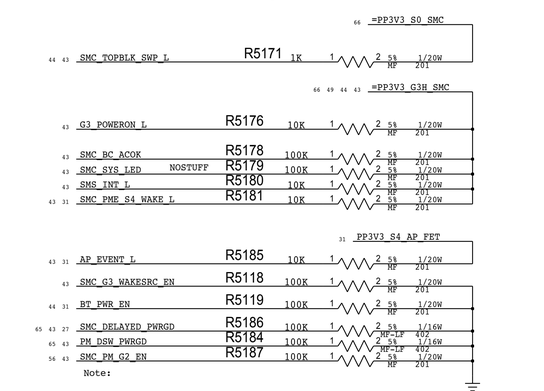
SMC Crystal

NOTE: SMC team wants 12MHz for this Xtal



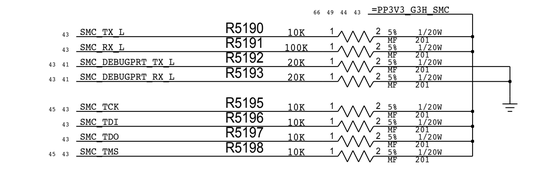


Arch Pull Up/Down



Note:

Serial/JTAG Interface Pull-ups



All: 5% MF 1/20W 201

SYNC_MASTER=J70_NICK	SYNC_DATE=01/15/2014
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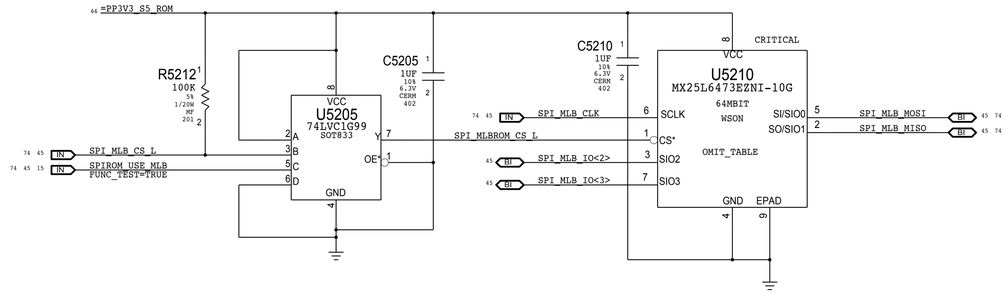
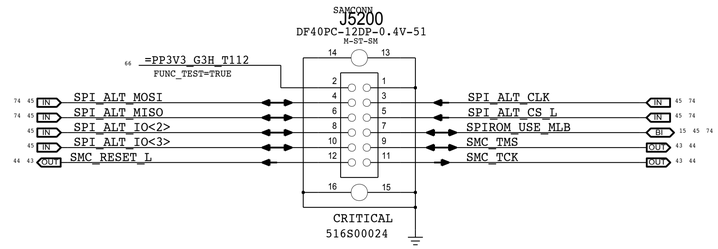
SPI BootROM

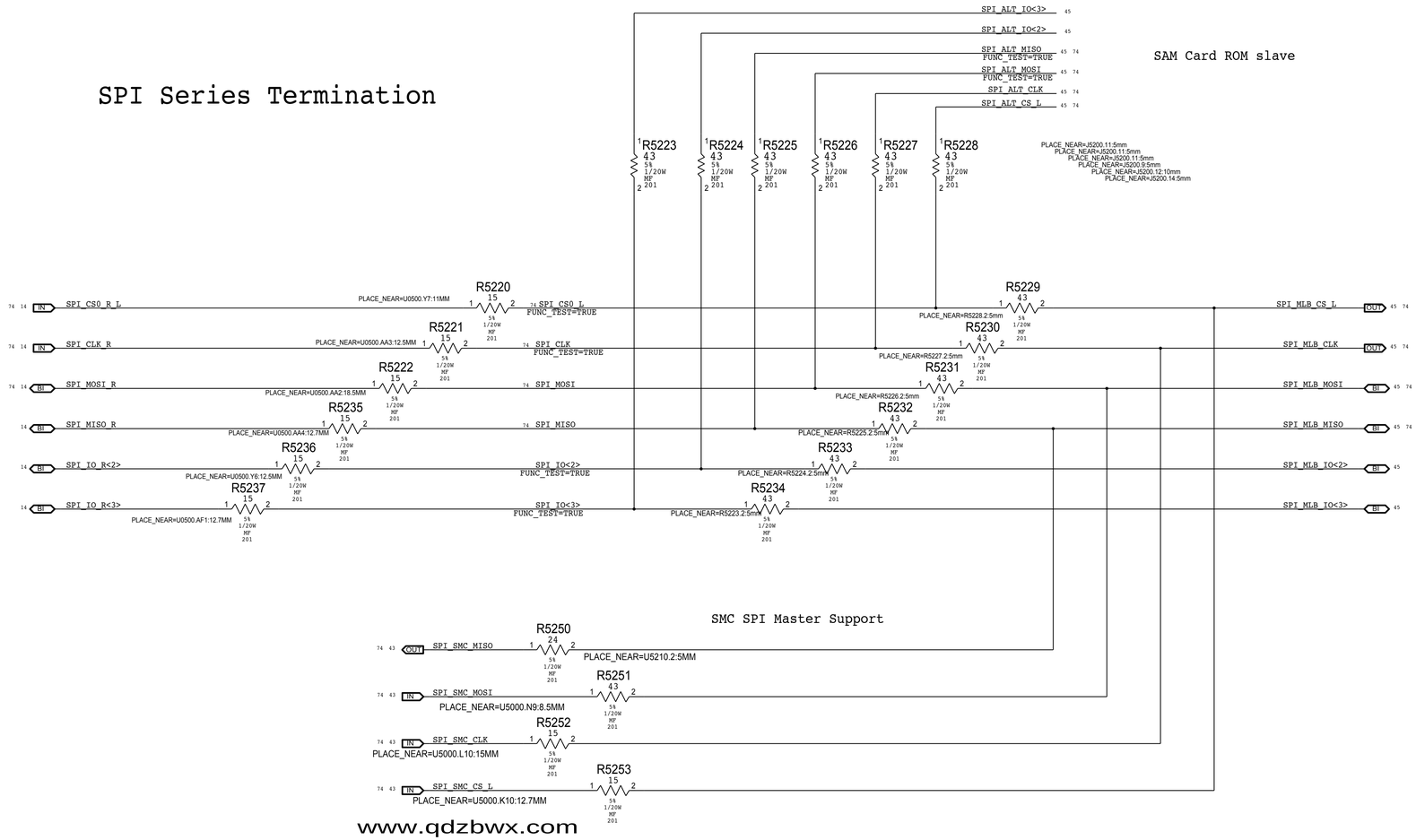
Quad_IO Mode (Mode 0 & 3) supported
SPI Freq: 50MHz for PCH, 20 MHz for SMC



SPI+SWD SAM Connector



SPI Series Termination



SYNC_MASTER=J117_TONY SYNC_DATE=05/05/2014

PAGE TITLE
SPI and Debug Connector

Apple Inc.

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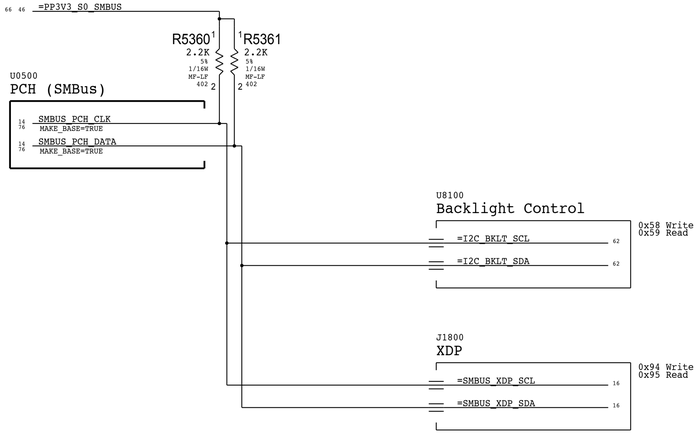
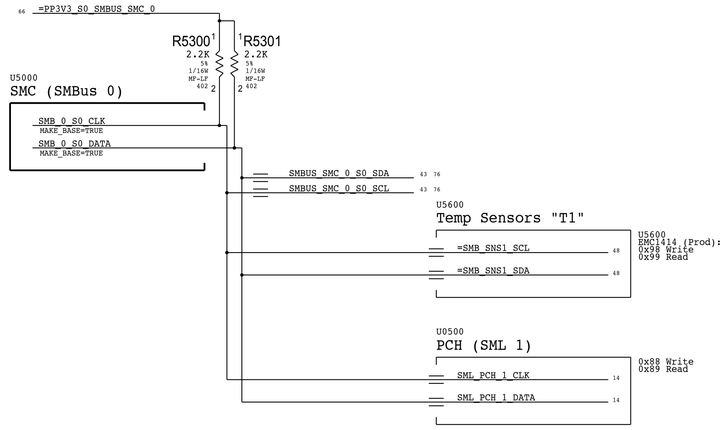
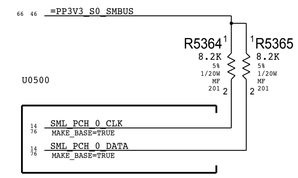
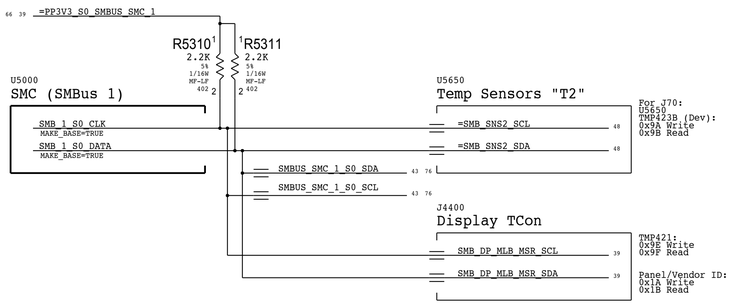
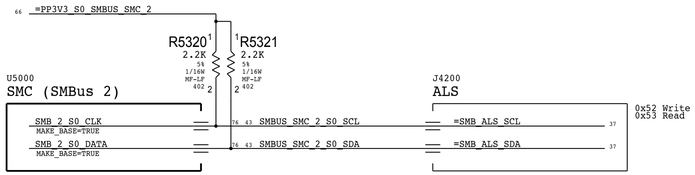


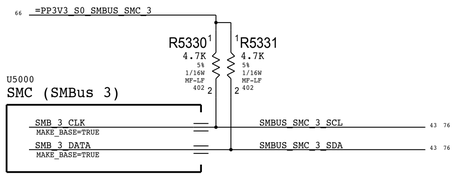




Unused PCH SM Link







SMC multi-master experiment

Line Legend
- Master
- Slave
- Mux

SYNC_MASTER=J70_NICK SYNC_DATE=02/14/2014

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SMBus Connections

Apple Inc.

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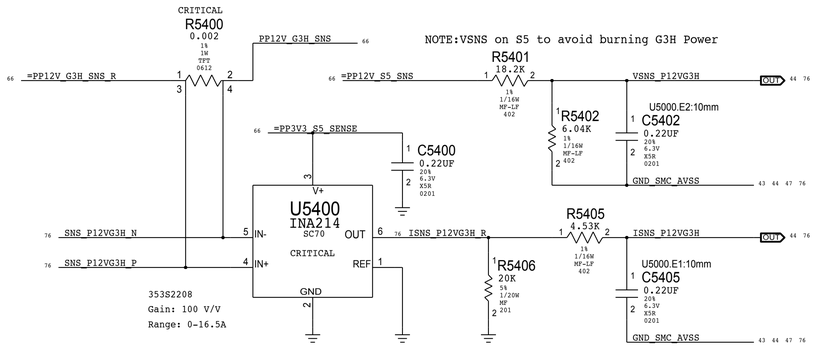
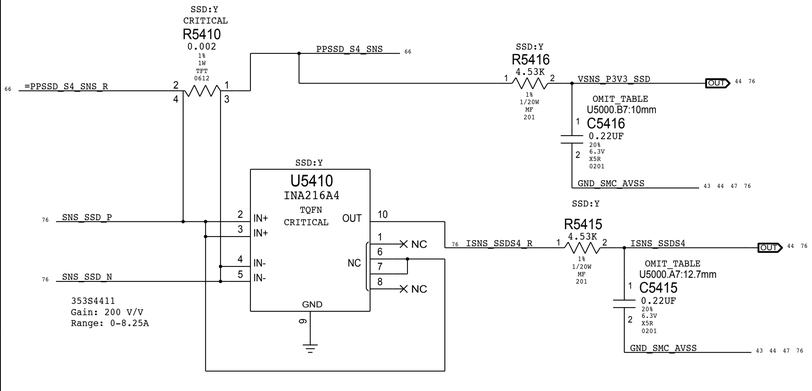
12V G3H (VD2R:ADC0/ID2R:ADC1)

AC/DC lowside sense (System total)



SSD S4 (IH1R:ADC21/VR3R:ADC20)

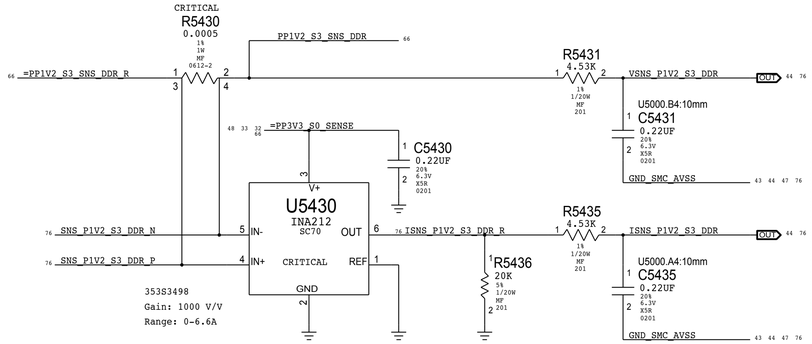
I-sense / V-sense for SSD



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
13280304	2	CAP,0.22UF,201	C5415,C5416	SSD:Y
11780201	2	RES,0 OHM,201	C5415,C5416	SSD:N

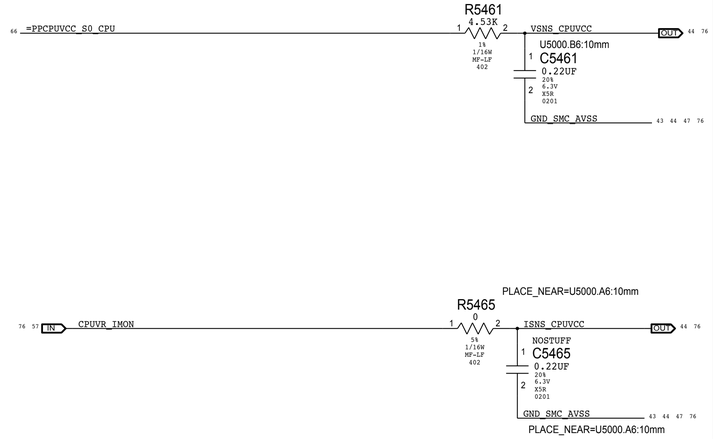
VDDQ S3 (VM0R:ADC6/IM0R:ADC7)

VDDQ lowside sense for DDR



CPU Core (VC0C:ADC10/IC0C:ADC11)

Voltage sense and IMON amp (VC0C, IC0C)



SYNC_MASTER=J70_NICK SYNC_DATE=11/05/2013

PAGE TITLE: I and V Sense

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

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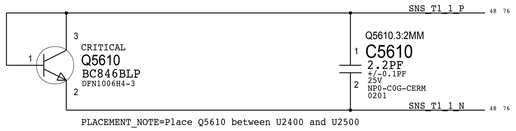
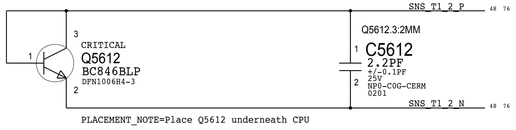
Temperature Sensor T1

LPDDR3 Proximity



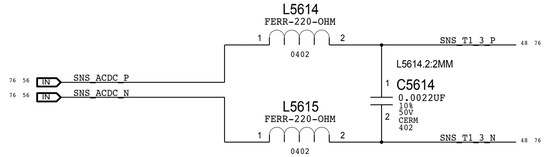
PLACEMENT_NOTE=Place Q5610 between U2400 and U2500

CPU Proximity

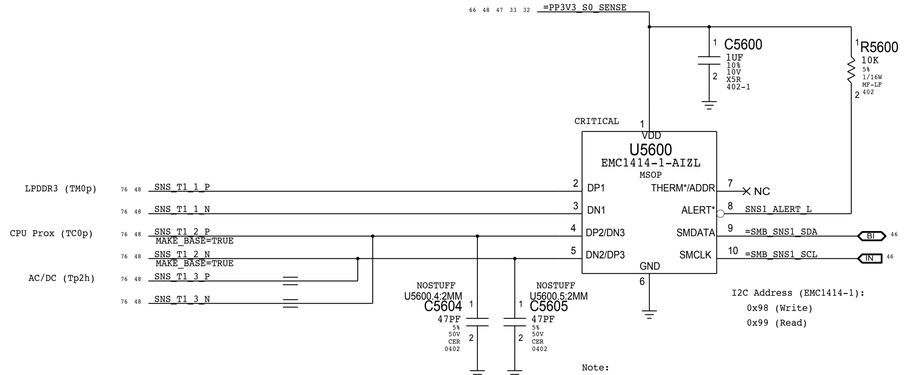


PLACEMENT_NOTE=Place Q5612 underneath CPU

AC/DC Diode on supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

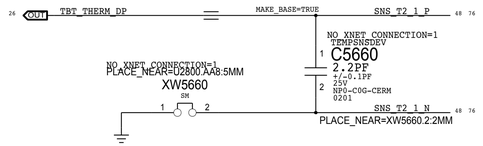


Filter Caps: Stuff if needed for PSU sensor SI

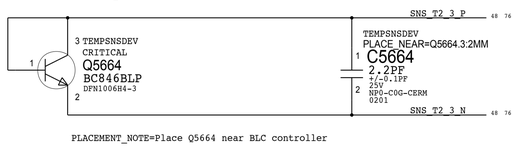
Note:
Internal sensor of the EMC 1414
will be used as the ambient sensor.
Place U5600 at the coolest location
on the MLB.

Temperature Sensor T2

TBT On Die

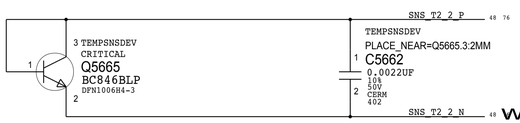


BLC Proximity

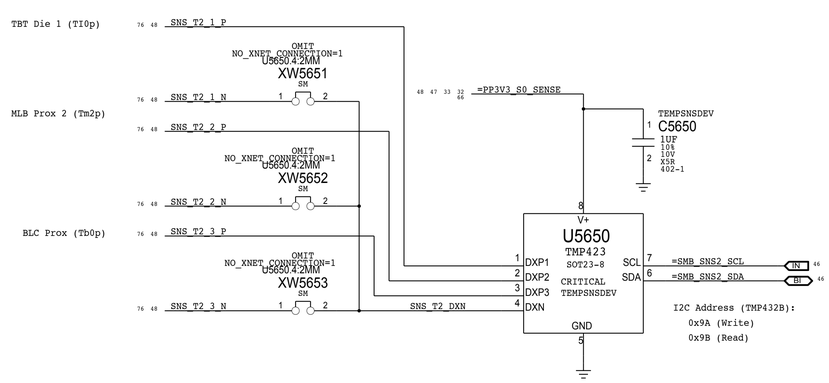


PLACEMENT_NOTE=Place Q5664 near BLC controller

MLB Misc 0



PLACEMENT_NOTE=PLACE Q5665 near CPU



SYNC_MASTER=J70_NICK SYNC_DATE=11/05/2013

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Temperature Sensors

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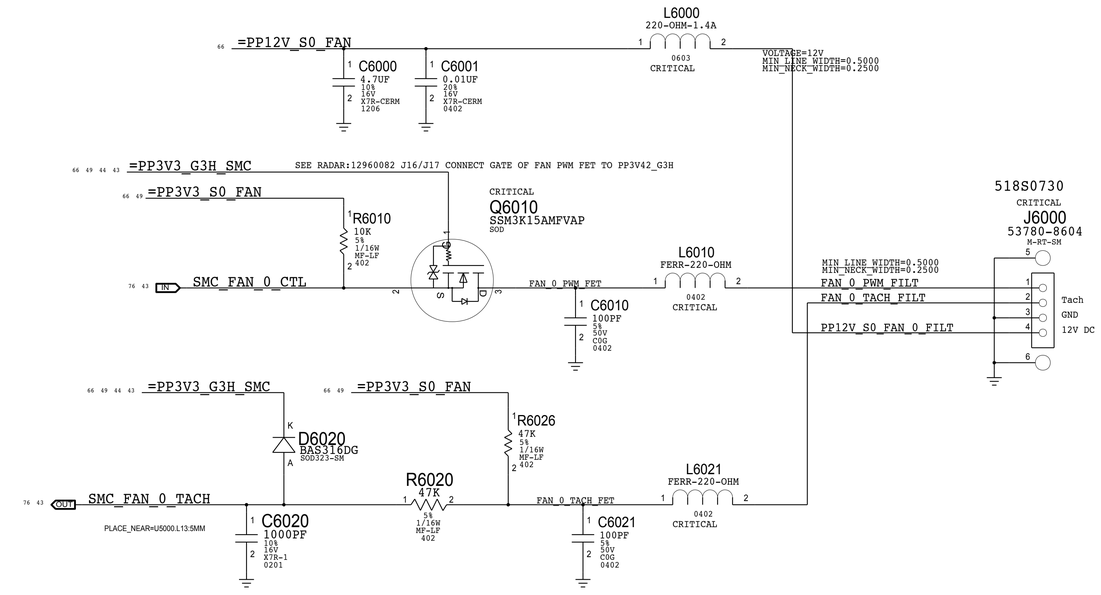
Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q6010 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q6010 is at common and the SMC sinks current when Q6010 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).

SMC Fan 0 (System)



Add C6020 1000pF Cap, Change R6020 to 47K -- Radar 11661918 D8 Protol Fan Tach instability.

SMC Fan 1 (Unused)

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE: System Fan

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

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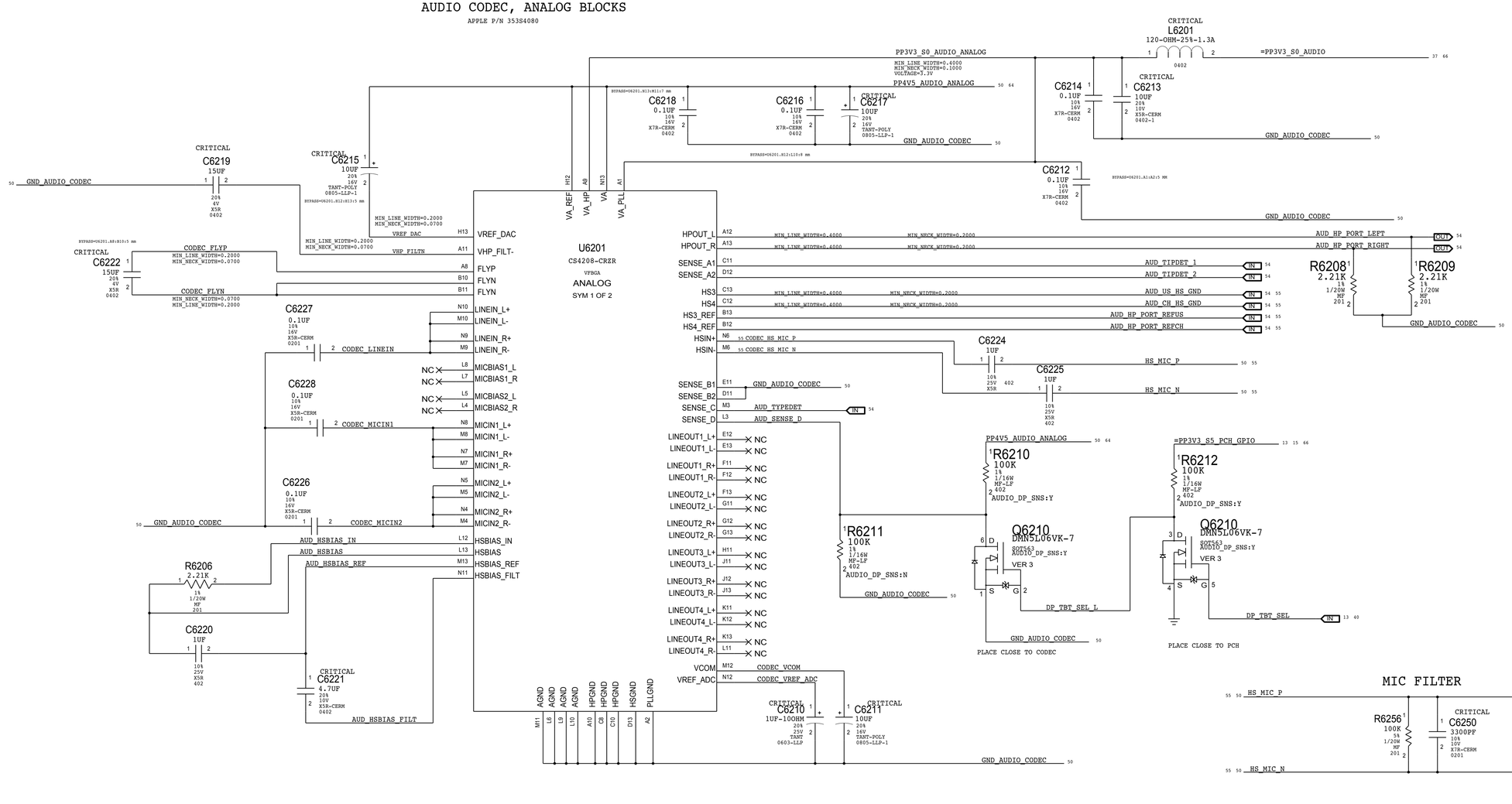
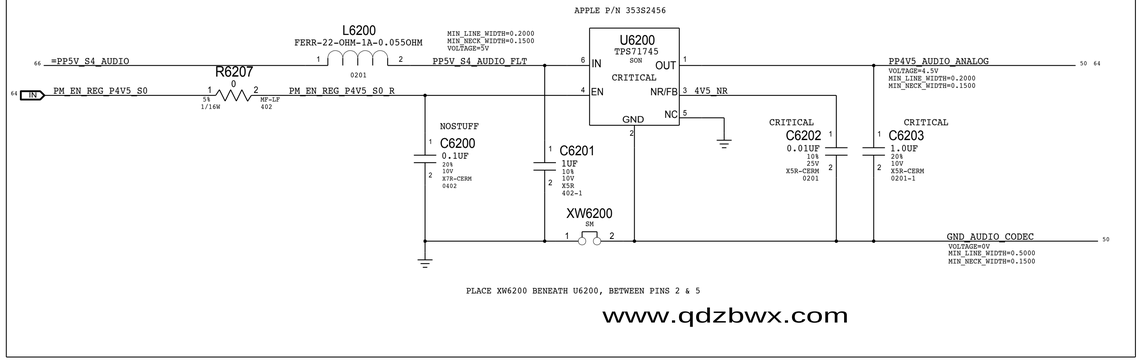
AUDIO CODEC, ANALOG BLOCKS

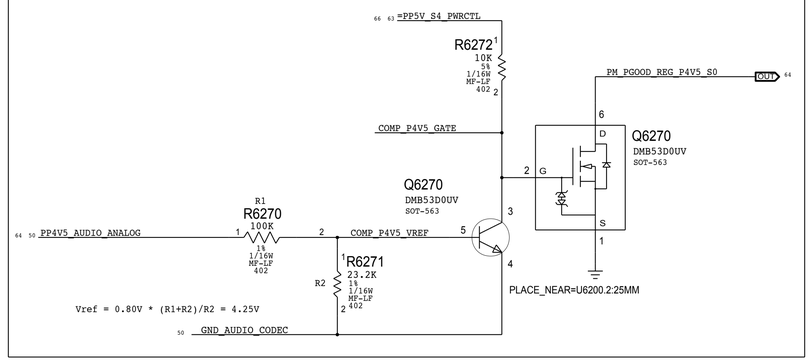
APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC



4.5V COMPARATOR



SYNC_MASTER=J117_GAREN SYNC_DATE=05/05/2014

PAGE TITLE: AUDIO: Codec (Analog)

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D

REVISION 3.0.0

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SHEET 50 OF 81

AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080

L6300
FERR-22-OHM-1A-0.055OHM
0201

=PP1V5_S0_AUDIO_DIG → PP1V5_S0_AUDIO_DIG_FILT
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.0700
VOLTAGE=1.5V

C6300 4.7UF 20% 4V X5R-1 402
C6301 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.J2:J1:13 mm
C6302 0.1UF 10% 16V X7R-CERM 0402
BYPASS=U6201.E1:F1:11 mm

=PP3V3_S0_AUDIO_DIG
BYPASS=U6201.G1:F1:12 mm
C6303 0.1UF 10% 6.3V CERM-X5R 0201
BYPASS=U6201.K1:K3:6 mm
C6304 0.1UF 10% 6.3V CERM-X5R 0201
C6305 10UF 20% 10V X5R-CERM 0402-1
C6306 10UF 20% 10V X5R-CERM 0402-1
BYPASS=U6201.A7:E3:6 mm
C6307 0.1UF 10% 6.3V CERM-X5R 0201

=PP3V3_S0_AUDIO_DIG
R6358 1K 1% 1/16W MF-LF 402
R6359 1K 1% 1/16W MF-LF 402
R6324 100K 5% 1/20W MF 201
R6325 100K 5% 1/20W MF 201
R6326 47.0K 1% 1/16W MF-LF 402
R6327 47.0K 1% 1/16W MF-LF 402

CODEC_SDA
CODEC_SCL
SPKR_AMP_SD (OUT)
SPKR_AMP_FAULT (IN)
AUD_CONN_SPKR_VENDOR_ID_LEFT (IN)
AUD_CONN_SPKR_VENDOR_ID_RIGHT (IN)
DFET_OPENUS (OUT)
DFET_OPENCH (OUT)

R6340 0 5% 1/20W MF 0201
HDA_BIT_CLK (IN) → HDA_BIT_CLK_PORT
R6341 0 5% 1/20W MF 0201
HDA_SYNC (IN) → HDA_SYNC_PORT
R6342 22 5% 1/20W MF 201
HDA_SDIN0 (OUT) → CS4208_HDA_SDOUT0_R → NC_CS4208_HDA_SDOUT1
R6343 0 5% 1/20W MF 0201
HDA_SDOUT (IN) → HDA_SDOUT_PORT
HDA_RST_L (IN)

R6350 33 1% 1/20W MF 201
R6351 33 1% 1/20W MF 201
R6352 33 1% 1/20W MF 201
R6353 33 1% 1/20W MF 201
MCLKA_SPKR_LEFT (OUT)
SCLKA_SPKR_LEFT (OUT)
LRCLKA_SPKR_LEFT (OUT)
SDOUTA_SPKR_LEFT (OUT)

R6360 33 1% 1/20W MF 201
R6361 33 1% 1/20W MF 201
R6362 33 1% 1/20W MF 201
R6363 33 1% 1/20W MF 201
MCLKB_SPKR_RIGHT (OUT)
SCLKB_SPKR_RIGHT (OUT)
LRCLKB_SPKR_RIGHT (OUT)
SDOUTB_SPKR_RIGHT (OUT)

U6201
CS4208-CRZR
VFBGA
DIGITAL
SYM 2 OF 2

H3	GPIO0	
H2	GPIO1	
H1	GPIO2	
C4	GPIO3	
C5	GPIO4	
C7	GPIO5	
C9	GPO0	NC
B9	GPO1	NC
F2	BCLK	
E2	SYNC	
D1	SDI0	
C1	SDI1	
D2	SDO0	
C2	SDO1	
C3	SDO2	
B1	SDO3	
D3	RST*	
A5	MCLK_A	MCLKA_SPKR_LEFT_R
B2	SCLK_A	SCLKA_SPKR_LEFT_R
B4	LRCK_A	LRCLKA_SPKR_LEFT_R
A3	SDOUT_A	SDOUTA_SPKR_LEFT_R
B3	SDIN_A	
A6	MCLK_B	MCLKB_SPKR_RIGHT_R
B6	SCLK_B	SCLKB_SPKR_RIGHT_R
B5	LRCK_B	LRCLKB_SPKR_RIGHT_R
B8	SDOUT_B	SDOUTB_SPKR_RIGHT_R
A4	SDIN_B	
C6	SDA	CODEC_SDA
B7	SCL	CODEC_SCL

VD, VL_HD, VL_SP, VL_LF, VL_DM
J2, E1, A7, G1, K1

DGND, LGND, LGND, LGND, LGND, LGND
J1, F1, E3, F3, J3, K3

R6302 0 5% 1/20W MF 0201
DP_INT_SPDIF_AUDIO (IN)
SPDIF_IN (G3) ← CS4208_SPDIF_IN
SPDIF_OUT (G2) → CS4208_SPDIF_OUT
R6330 33 5% 1/16W MF-LF 402
SPDIF_OUT_JACK (OUT)

DMIC_SDA0 (N3)
DMIC_SCL0 (N2) — NC
DMIC_SDA1 (N1)
DMIC_SCL1 (M1) — NC
DMIC_SDA2 (M2)
DMIC_SCL2 (L1) — NC
DMIC_SDA3 (K2)
DMIC_SCL3 (L2)
R6333 0 5% 1/20W MF 0201
DMIC_SDA3_R → DMIC_SDA3 (IN)
R6332 75 1% 1/16W MF-LF 402
DMIC_CLK3_R → DMIC_CLK3 (OUT)

NC: F6, F7, F8, G6, G7, G8, H6, H7, H8

SYNC_MASTER=J117_GASEN SYNC_DATE=05/05/2014

PAGE TITLE: AUDIO:CODEC, DIGITAL

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D
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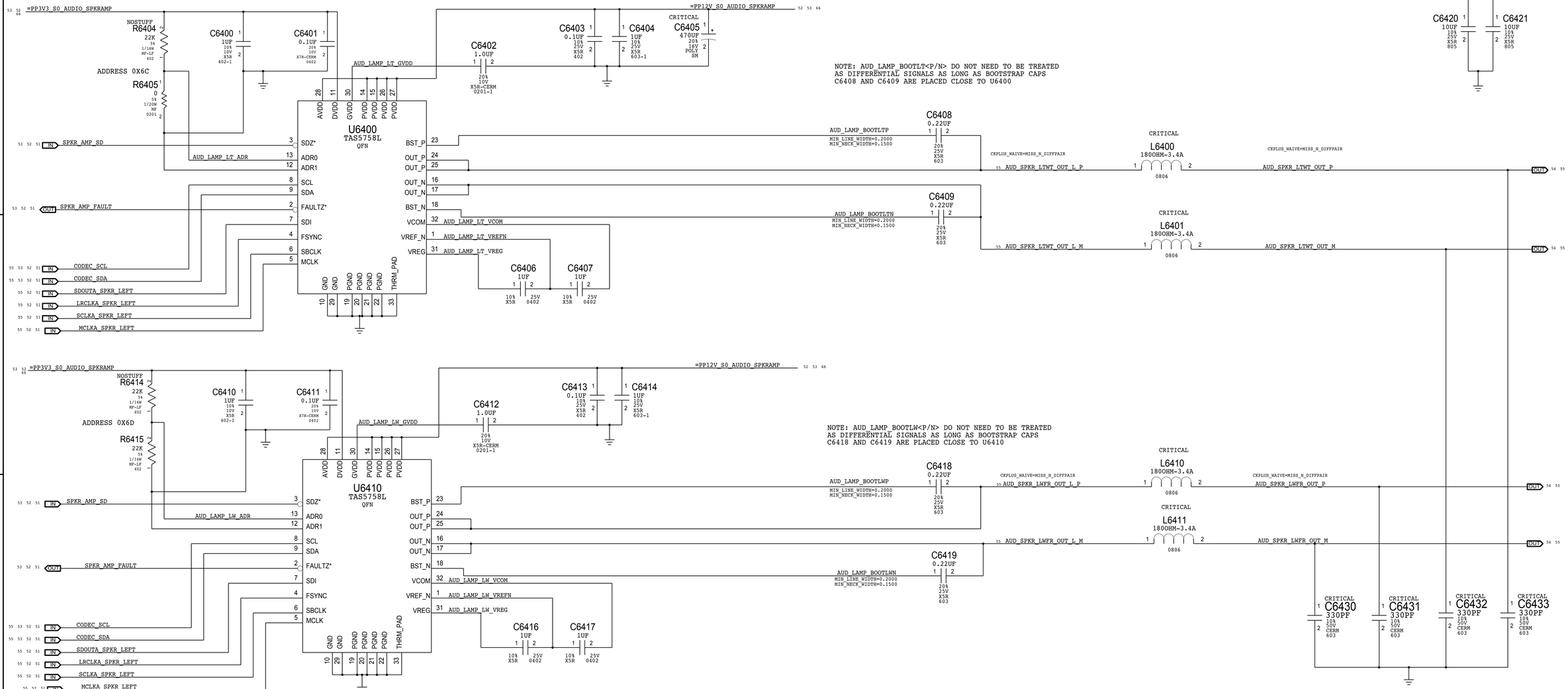
SHEET 51 OF 81

2X MONO SPEAKER AMPLIFIERS (TAS5758L)

APN: TBD

GAIN = TBD

SPEAKER AMPLIFIERS - LEFT CHANNEL



SYNC_MASTER=J117_GAKEN SYNC_DATE=05/05/2014

PAGE TITLE: AUDIO: SPEAKER AMP, LEFT CHANNEL

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

BRANCH:

PAGE: 64 OF 123

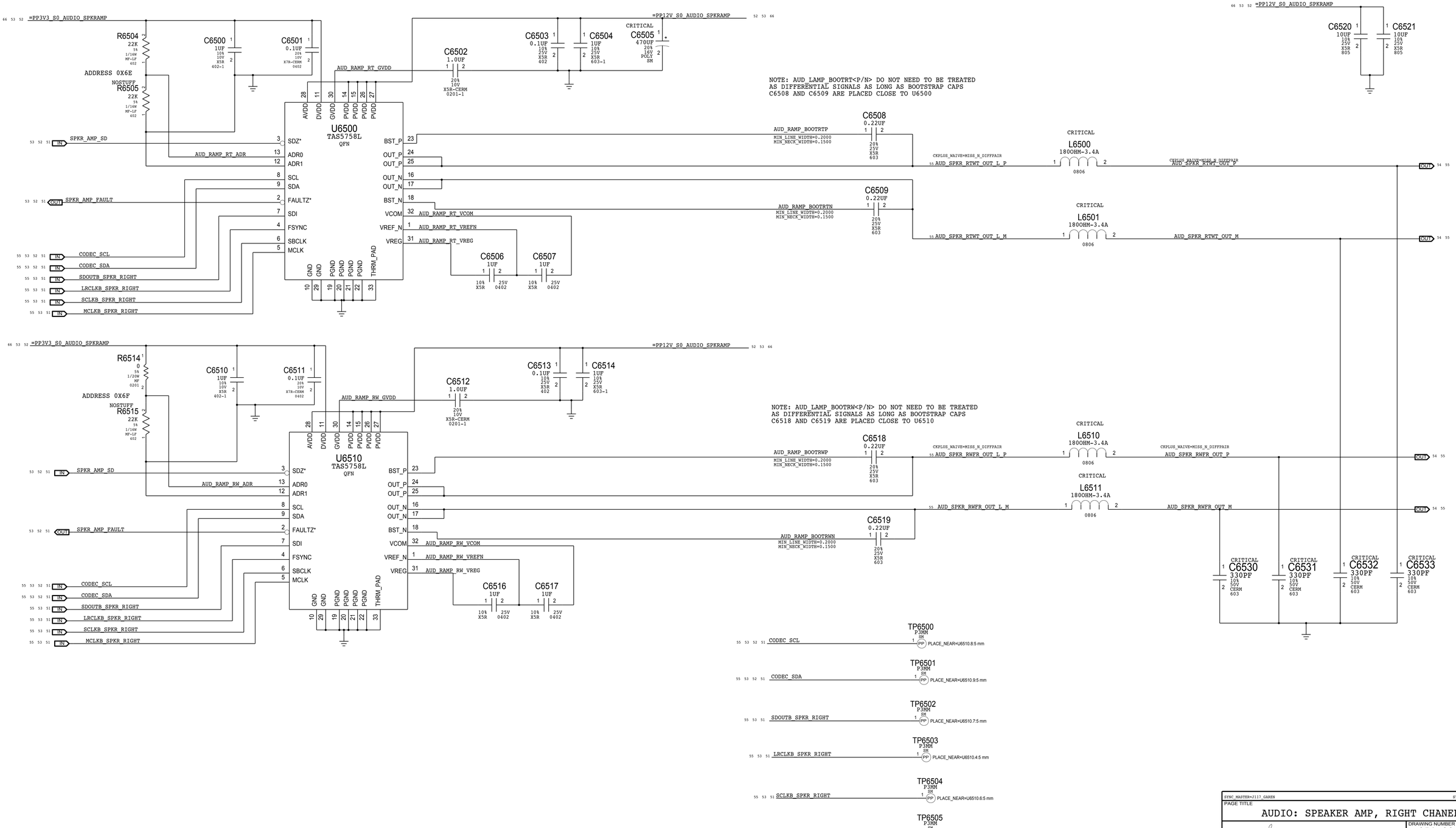
SHEET: 52 OF 81

2X MONO SPEAKER AMPLIFIERS (TAS5758L)

APN: TBD

GAIN = TBD

SPEAKER AMPLIFIERS - RIGHT CHANNEL



SYNC_MASTER=J117_GAREN SYNC_DATE=05/05/2014

PAGE TITLE: AUDIO: SPEAKER AMP, RIGHT CHANEL

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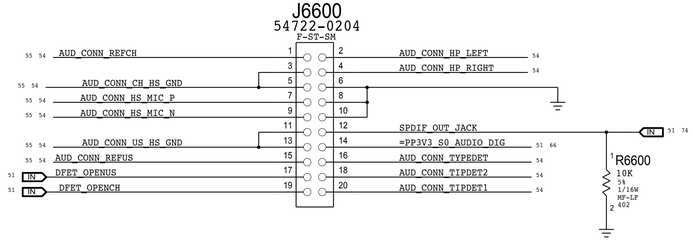
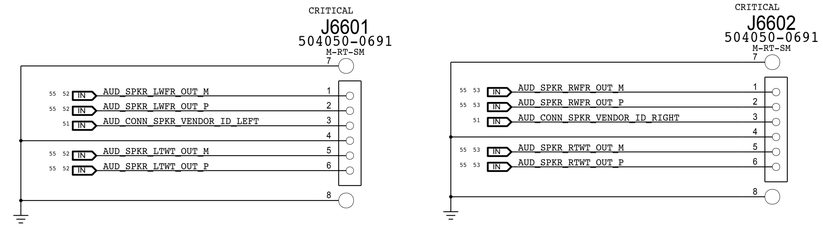
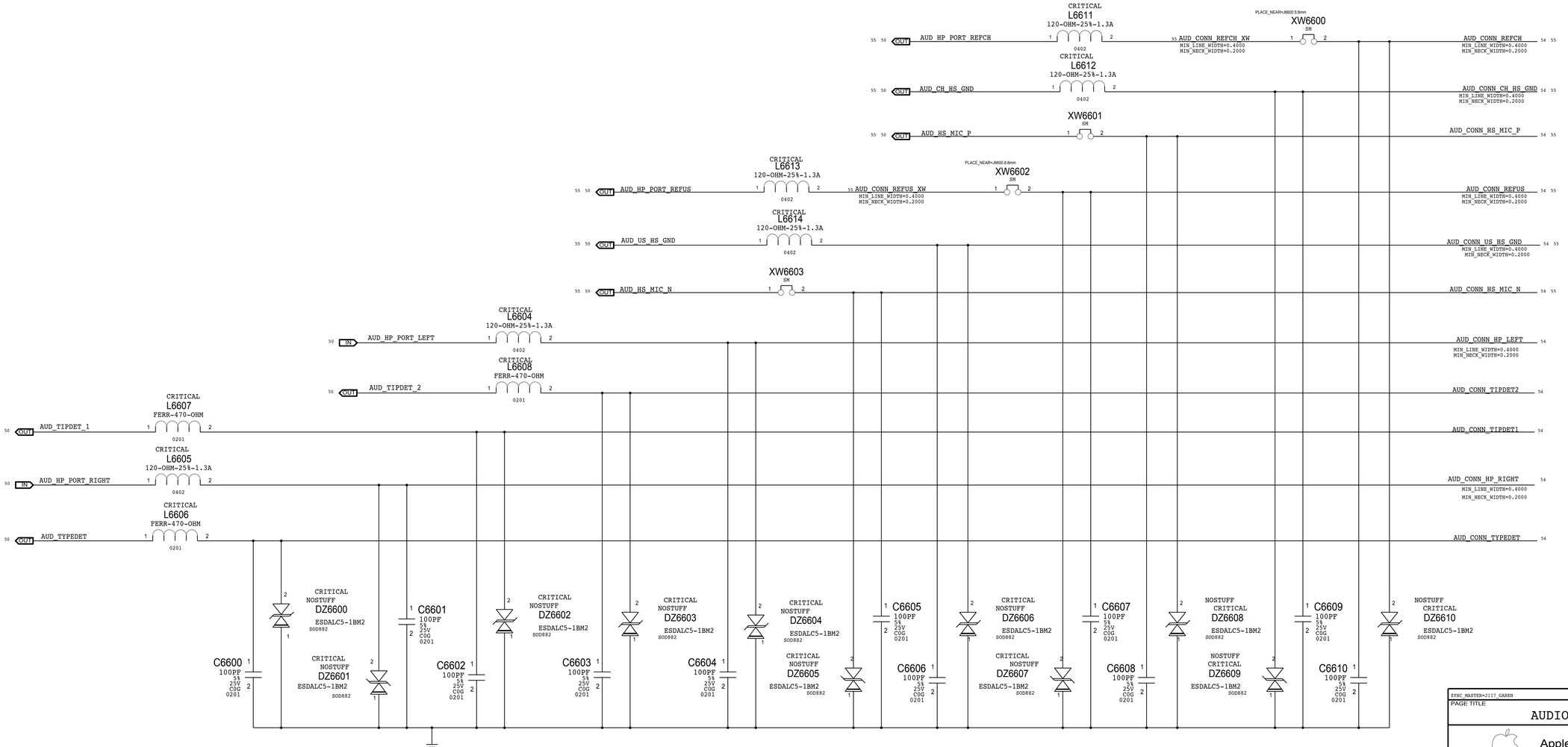
SHEET: 53 OF 81

SPEAKER CONNECTOR





Reversed Phases 1 & 2 and 5 & 6 on J6601 and J6602 Ref J16



ESD DIODES (DZ6600 -> DZ6610) NOW NOSTUFF - MAY BE ADDED FOLLOWING ESD TESTING

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SYNC_MASTER=J117_GARSEN	SYNC_DATE=05/05/2014
PAGE TITLE	AUDIO: JACK TRANSLATORS
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	REVISION 3.0.0
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	SHEET 54 OF 81

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	Lynx POINT GPIO 16	Lynx POINT GPIO 5 (RCVR_INT) Lynx POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO_ISO	*	0.1 MM	?
SPKROUT_ISO	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
AUDIODIFF_2MM	*	Y	0.2 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	AUDIO_ISO
SPKROUT	*	*	SPKROUT_ISO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
SPEAKER OUTPUTS				
J205 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	53 54
J203 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_M	53 54
J220	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_L_P	53
J219	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_L_M	53
J333 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	53 54
J332 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_M	53 54
J330	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_L_P	53
J331	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_L_M	53
J337 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	52 54
J336 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_M	52 54
J334	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_L_P	52
J335	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_L_M	52
J341 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	52 54
J340 AUDIO_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_M	52 54
J338	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_L_P	52
J339	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_L_M	52
HEADSET MIC				
J348 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_CONN_HS_MIC_P	54
J349 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_CONN_HS_MIC_N	54
J254 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	50 54
J255 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	50 54
J324 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_P	50
J325 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	HS_MIC_N	50
J343 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CODEC_HS_MIC_P	50
J342 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CODEC_HS_MIC_N	50
J352		AUDIO	AUD_CONN_CH_HS_GND	54
J350		AUDIO	AUD_CONN_US_HS_GND	54
J368		AUDIO	AUD_CH_HS_GND	50 54
J369		AUDIO	AUD_US_HS_GND	50 54
J356		AUDIO	AUD_CONN_REFCH	54
J357		AUDIO	AUD_CONN_REFUS	54
J374		AUDIO	AUD_CONN_REFCH_XW	54
J370		AUDIO	AUD_CONN_REFUS_XW	54
J378		AUDIO	AUD_HP_PORT_REFCH	50 54
J372		AUDIO	AUD_HP_PORT_REFUS	50 54

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
CODEC SCL & SDA				
J358			CODEC_SCL	51 52 53
J359			CODEC_SDA	51 52 53
TDM				
J360		SDA	MCLKA_SPKR_LEFT	51 52
J361		SDA	SCLKA_SPKR_LEFT	51 52
J362		SDA	LRCLKA_SPKR_LEFT	51 52
J363		SDA	SDOUTA_SPKR_LEFT	51 52
J374			MCLKA_SPKR_LEFT_R	51
J375			SCLKA_SPKR_LEFT_R	51
J376			LRCLKA_SPKR_LEFT_R	51
J377			SDOUTA_SPKR_LEFT_R	51
J364		SDA	MCLKB_SPKR_RIGHT	51 53
J365		SDA	SCLKB_SPKR_RIGHT	51 53
J367		SDA	LRCLKB_SPKR_RIGHT	51 53
J366		SDA	SDOUTB_SPKR_RIGHT	51 53
J379			MCLKB_SPKR_RIGHT_R	51
J378			SCLKB_SPKR_RIGHT_R	51
J380			LRCLKB_SPKR_RIGHT_R	51
J381			SDOUTB_SPKR_RIGHT_R	51

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE

AUDIO: Speaker ID

Apple Inc.

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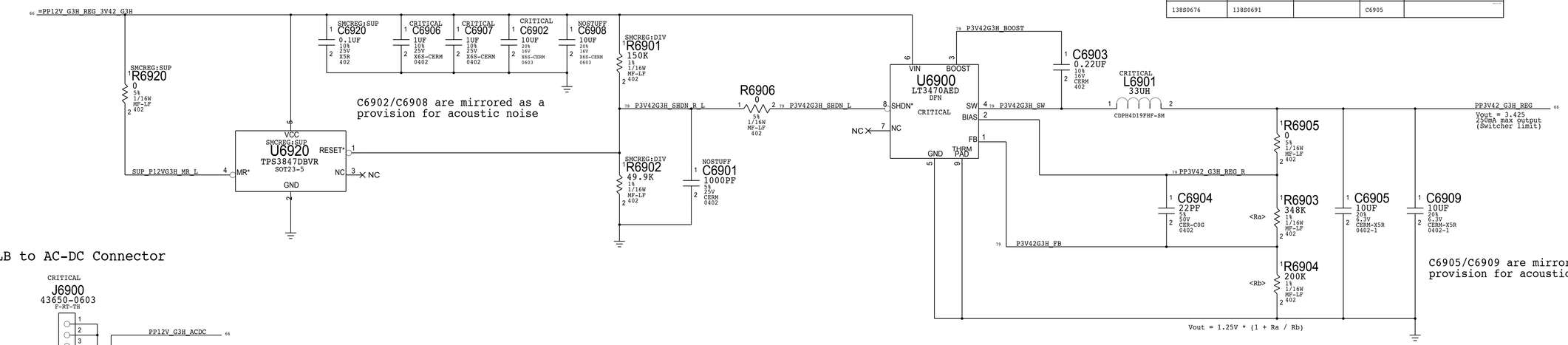
SHEET 55 OF 81

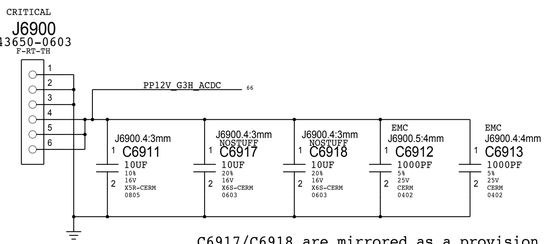
3.425V "G3Hot" Regulator

Switching freq: 409 kHz = $\frac{13.5}{L6901}$

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0676	138S0691		C6905	

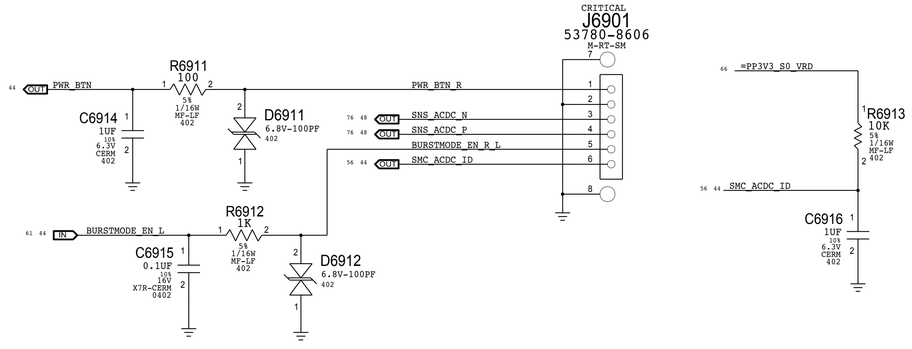


MLB to AC-DC Connector

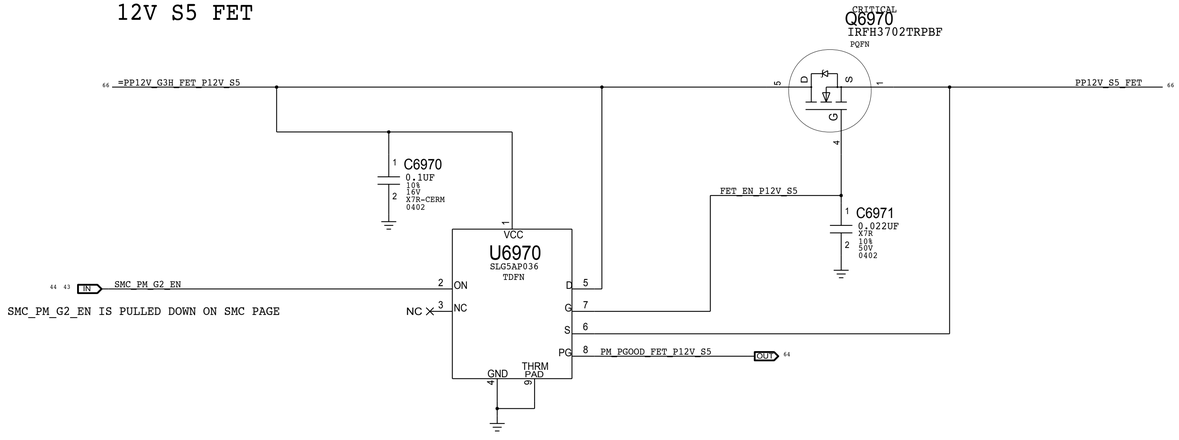


C6917/C6918 are mirrored as a provision for acoustic noise to replace C6911 if needed

MLB to AC-DC Supplemental Signal Connector



12V S5 FET



SMC_PM_G2_EN IS PULLED DOWN ON SMC PAGE

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: Power Connectors / VReg G3Hot

Apple Inc.

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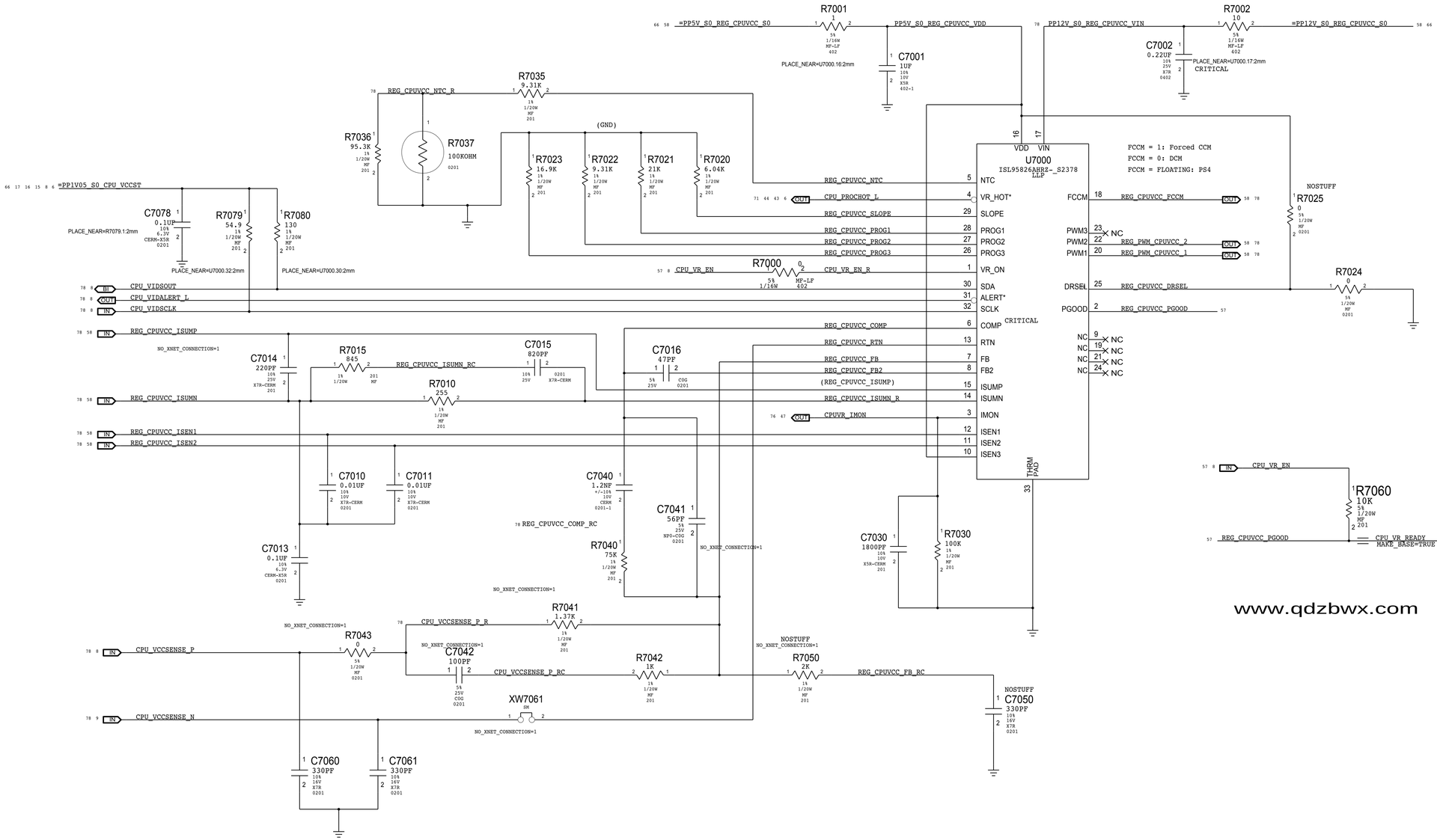
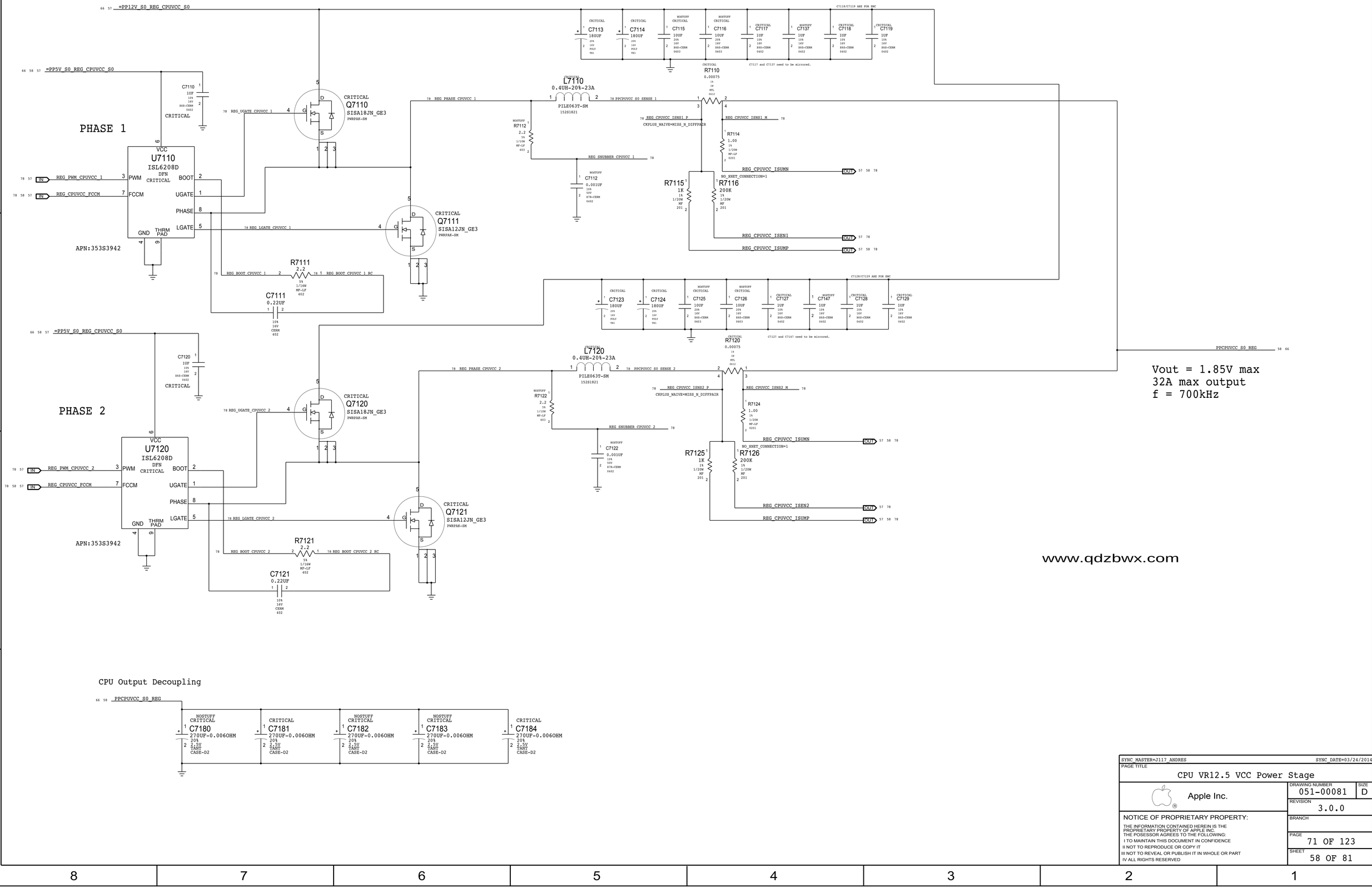


SYNC_MASTER=J70_ROSSANA	SYNC_DATE=09/17/2013
PAGE TITLE	CPU VR12.6 VCC Regulator IC
Apple Inc.	DRAWING NUMBER 051-00081 · SIZE D
	REVISION 3.0.0
	BRANCH
	PAGE 70 OF 123
	SHEET 57 OF 81



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SYNC_MASTER=J117_ANDRES	SYNC_DATE=03/24/2014
PAGE TITLE: CPU VR12.5 VCC Power Stage	
Apple Inc.	DRAWING NUMBER: 051-00081 SIZE: D
	REVISION: 3.0.0
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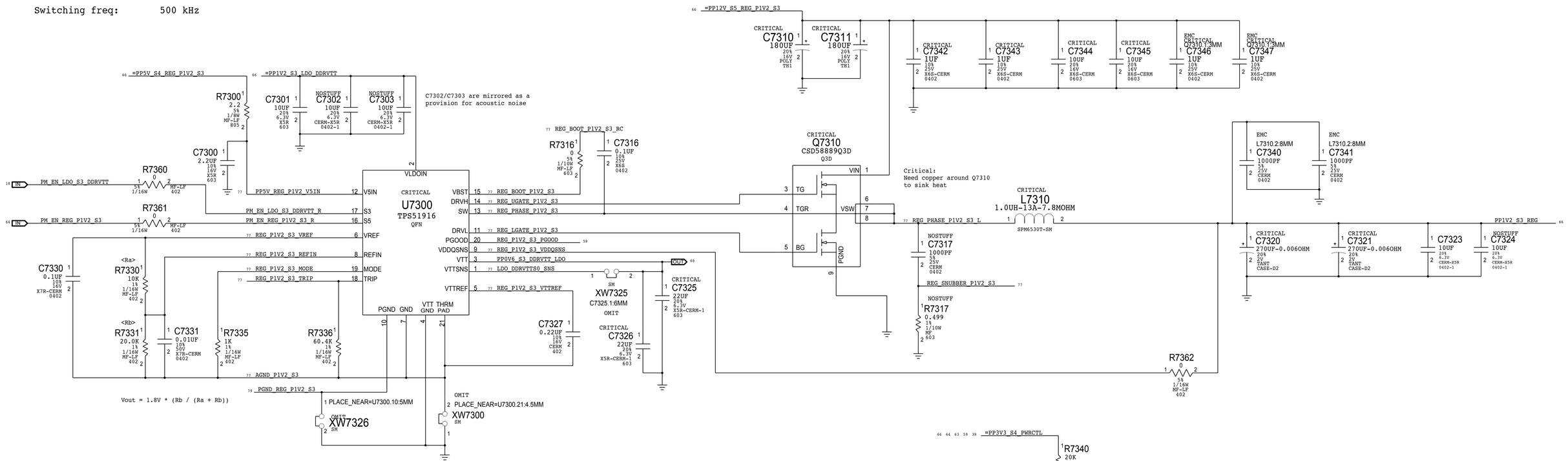
	PAGE: 71 OF 123
	SHEET: 58 OF 81

VDDQ 1.2V S3 Regulator

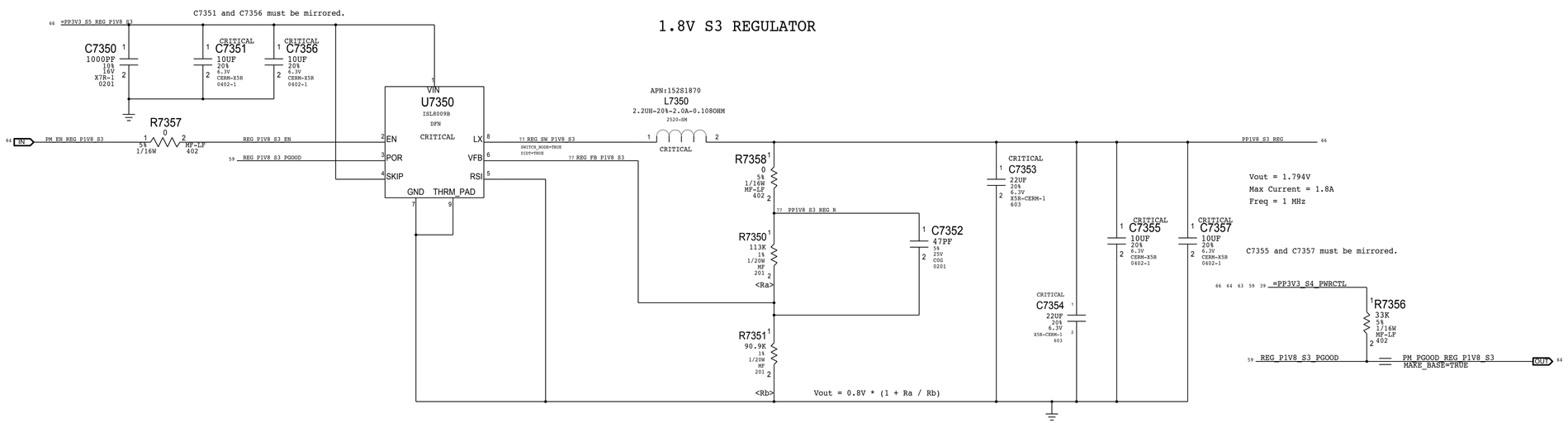
OC trip point: 30.4 A VDDQ = $\frac{R7336}{8\ E5 * Rds(Q7310)} + \frac{0.65625}{L7310 * f(switch)}$

3 A VTT (FIXED)
10 mA VTTREF (FIXED)

Switching freq: 500 kHz



1.8V S3 REGULATOR



SYNC_MASTER=J70_ROSSANA	SYNC_DATE=09/12/2013
PAGE TITLE	VReg VDDQ S3 / 1.8V S3
Apple Inc.	DRAWING NUMBER 051-00081 SIZE D
	REVISION 3.0.0
	BRANCH
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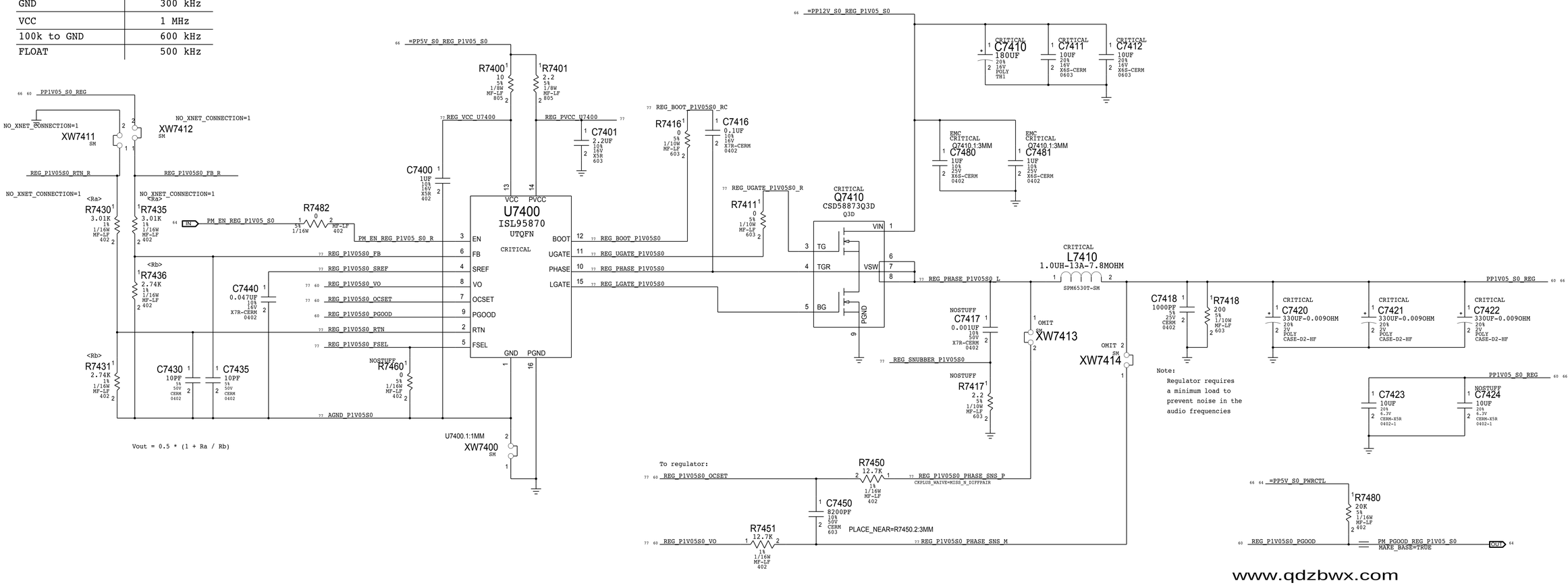
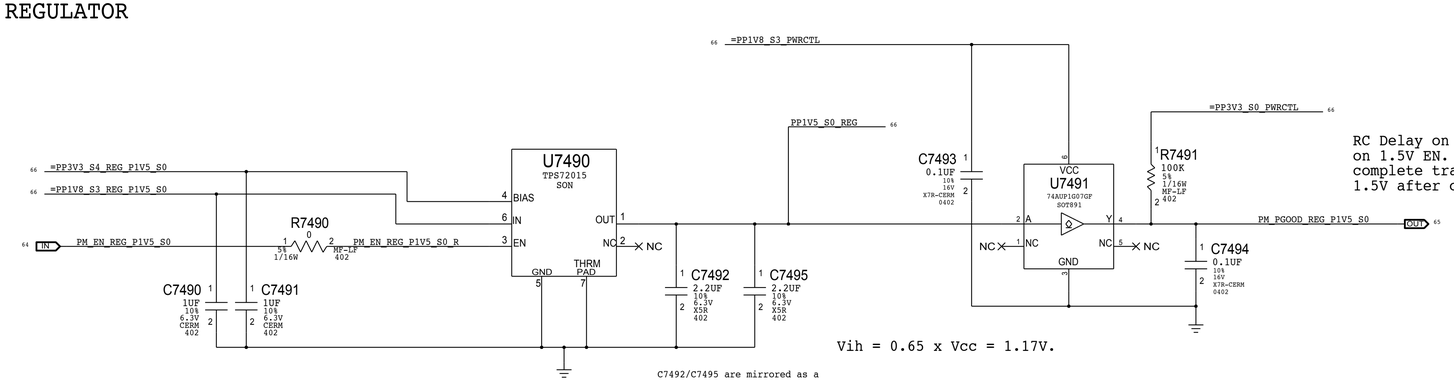
PCH (1.05V) S0 REGULATOR

Switching freq: 500 kHz OC trip point: 12.4 A = $\frac{R7450 * 8.5\ E\text{-}6}{DCR(L7410)}$

FSEL STRAP	SW FREQ
GND	300 kHz
VCC	1 MHz
100k to GND	600 kHz
FLOAT	500 kHz



1.5V S0 REGULATOR



RC Delay on 1.5V PGOOD must be longer than delay on 1.5V EN. This allows for rail voltage to complete transition from Vih min (1.17V) to 1.5V after output shifts to OD.

SYNC_MASTER=J117_ANDRES	SYNC_DATE=03/24/2014
PAGE TITLE: VREG 1V05 S0 / 1V5 S0	
Apple Inc.	DRAWING NUMBER: 051-00081 SIZE: D
	REVISION: 3.0.0
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	PAGE: 74 OF 123
	SHEET: 60 OF 81

3.3V S5 Regulator

OC trip point: 12.5 A = R7618 * 10 E-6 / DCR(L7610)

Switching freq: 356 kHz = 1 / 170 E-12 * R7633

5V S4 Regulator

OC trip point: 14.1 A = R7658 * 10 E-6 / DCR(L7650)

Switching freq: 356 kHz = 1 / 170 E-12 * R7673

=PP12V_S5_REG_P3V3P5V_S5

CRITICAL C7610 180UF 20% 16V POLY TH1

CRITICAL C7650 180UF 20% 16V POLY TH1

CRITICAL C7651 180UF 20% 16V POLY TH1

R7603 1 5% 1/10W MF-LF 603

EMC CRITICAL Q7610 2.3MM C7642 1UF 10% 25V X6S-CERM 0402

EMC CRITICAL Q7610 2.3MM C7643 1UF 10% 25V X6S-CERM 0402

REG_VIN_U7600

EMC CRITICAL Q7650.5.3MM C7682 1UF 10% 25V X6S-CERM 0402

EMC CRITICAL Q7650.5.3MM C7683 1UF 10% 25V X6S-CERM 0402

PP5V_S5_LDO

C7601 4.7UF 20% 6.3V CERM 603

R7602 2.2 5% 1/8W MF-LF 805

REG_VCC2_U7600

REG_VCC1_U7600

C7600 1UF 10% 16V X5R 402

C7602 1UF 10% 16V X5R 402

C7603 1UF 10% 16V X5R 402

CRITICAL Q7650 FDMC0225 MLP3.3X3.3

REG_BOOT_P5VS4_RC

R7656 0 5% 1/10W MF-LF 603

C7656 0.1UF 10% 25V X6S 0402

EMC L7610.1:8MM C7640 1000PF 5% 25V CERM 0402

EMC L7610.1:8MM C7641 1000PF 5% 25V CERM 0402

DCR(L7610) = 11.2 MOHM (TYP) / 12.5 MOHM (MAX)
Check this text note for accuracy

CRITICAL L7610 2.2UH-20%-8A-0.0112OHM PIMB065T-SM

CRITICAL Q7610 FDMS3602S POWER56

PP3V3_S5_REG

C7622 10UF 20% 6.3V CERM-X5R 0402-1

CRITICAL C7621 150UF 20% 6.3V POLY B1A-SM-1

CRITICAL C7620 150UF 20% 6.3V POLY B1A-SM-1

OMIT SM XW7610

OMIT 2 SM XW7611

C7618 0.01UF 10% 16V X7R-CERM 0402

NOSTUFF C7617 0.001UF 10% 50V CERM 402

C7616 0.1UF 10% 25V X6S 0402

(reg_phase_p3v3s5)

REG_SNUBBER_P3V3S5

REG_P3V3S5_PHASE_SNS_P

CKPLUS_WAIVE=MISS_N_DIFFPAIR

REG_BOOT_P3V3S5_RC

REG_P3V3S5_PHASE_SNS_M

R7690 0 5% 1/16W MF-LF 402

R7619 18.2K 1% 1/16W MF-LF 402

R7618 18.2K 1% 1/16W MF-LF 402

NOSTUFF R7617 0.499 1% 1/10W MF 603

R7616 0 5% 1/10W MF-LF 603

U7600 ISL62383CRTZ QFN

18	LDO5	VIN	17
5	VCC1	VCC2	4
3	FCCM	FCCM	REG_U7600_FCCM
7	PGOOD1	PGOOD2	1 REG_P5VS4_PGOOD
14	UGATE1	UGATE2	22 REG_UGATE_P5VS4
15	BOOT1	BOOT2	21 REG_BOOT_P5VS4
13	PHASE1	PHASE2	23 REG_PHASE_P5VS4
16	LGATE1	LGATE2	20 REG_LGATE_P5VS4
10	ISEN1	ISEN2	26 REG_P5VS4_ISEN
11	OCSET1	OCSET2	25 REG_P5VS4_OCSET
9	VOUT1	VOUT2	27 REG_P5VS4_VOUT
8	FB1	FB2	28 REG_P5VS4_FB
6	FSET1	FSET2	2 REG_P5VS4_FSET
12	EN1	EN2	24

CRITICAL

THRM PAD, PGND

REG_P3V3S5_PGOOD

REG_UGATE_P3V3S5

REG_BOOT_P3V3S5

REG_PHASE_P3V3S5

REG_LGATE_P3V3S5

REG_P3V3S5_ISEN

REG_P3V3S5_OCSET

REG_P3V3S5_VOUT

REG_P3V3S5_FB

REG_P3V3S5_FSET

(reg_p3v3s4_isen)

(reg_p3v3s4_ocset)

(reg_p3v3s4_vout)

<Ra> R7630 45.3K 1% 1/16W MF-LF 402

<Rb> R7631 10.0K 0.5% 1/16W MF 402

R7632 976 1% 1/16W MF-LF 402

REG_P3V3S5_VOUT_R

C7632 1000PF 5% 25V CERM 0402

C7633 0.01UF 10% 16V X7R-CERM 0402

R7633 16.5K 1% 1/16W MF-LF 402

Vout = 0.6 * (1 + Ra / Rb)

PM_EN_REG_P3V3_S5_R

R7692 0 5% 1/16W MF-LF 402

PM_EN_REG_P3V3_S5

PM_EN_REG_P5V_S4

R7693 0 5% 1/16W MF-LF 402

PM_EN_REG_P5V_S4_R

C7673 0.01UF 10% 16V X7R-CERM 0402

R7673 16.5K 1% 1/16W MF-LF 402

CRITICAL Q7655 FDMC0223S MLP3.3X3.3

NOSTUFF R7657 0.499 1% 1/10W MF 603

REG_P5VS4_PGOOD

PM_PGOOD_REG_P5V_S4 MAKE_BASE=TRUE

REG_P3V3S5_PGOOD

PM_PGOOD_REG_P3V3_S5 MAKE_BASE=TRUE

R7680 20K 5% 1/16W MF-LF 402

R7640 20K 5% 1/16W MF-LF 402

=PP3V3_S5_VRD

Check this text note for accuracy
DCR(L7650) = 6.2 MOHM (TYP) / 6.9 MOHM (MAX)

CRITICAL L7650 2.2UH-20%-0.0058OHM-16A PCMB104E-SM

(reg_phase_p5vs4)

EMC L7650.2:4MM C7680 1000PF 5% 25V CERM 0402

EMC L7650.2:4MM C7681 1000PF 5% 25V CERM 0402

CRITICAL C7660 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

CRITICAL C7661 330UF 20% 6.3V POLY-TANT CASE-D3L-SM

C7662 10UF 20% 10V X5R-CERM 0402-1

PP5V_S4_REG

NOSTUFF C7663 10UF 20% 10V X5R-CERM 0402-1

NOSTUFF C7664 10UF 20% 10V X5R-CERM 0402-1

C7663/C7664 are mirrored as a provision for acoustic noise

NOSTUFF C7657 0.001UF 10% 50V X7R-CERM 0402

REG_SNUBBER_P5VS4

REG_P5VS4_PHASE_SNS_P

CKPLUS_WAIVE=MISS_N_DIFFPAIR

REG_P5VS4_PHASE_SNS_M

OMIT SM XW7650

OMIT 2 SM XW7651

R7658 9.31K 1% 1/16W MF-LF 402

C7658 0.033UF 10% X5R 2 16V 402

R7659 9.31K 1% 1/16W MF-LF 402

R7691 0 5% 1/16W MF-LF 402

(reg_p5vs4_isen)

(reg_p5vs4_ocset)

(reg_p5vs4_vout)

R7672 976 1% 1/16W MF-LF 402

REG_P5VS4_VOUT_R

C7672 1000PF 5% 25V CERM 0402

<Ra> R7670 75K 1% 1/16W MF-LF 402

<Rb> R7671 10K 1% 1/16W MF-LF 402

Vout = 0.6 * (1 + Ra / Rb)

C7623 NOSTUFF 10UF 20% 6.3V CERM-X5R 0402-1

C7624 NOSTUFF 10UF 20% 6.3V CERM-X5R 0402-1

C7623/C7624 are mirrored as a provision for acoustic noise

NOSTUFF Q7600 SSM6L36FEAPL SOT563 P-CH N-CH

REG_U7600_FCCM_R

NOSTUFF R7600 1K 5% 1/16W MF-LF 402

NOSTUFF R7601 10K 5% 1/16W MF-LF 402

=PP5V_S5_PWRCTL

BURSTMODE_EN

BURSTMODE_EN_L

This circuit toggles the Vreg between PWM and ultrasonic DCM modes based on load requirements

BURSTMODE_EN_L	Vreg Mode
0	PWM
1	DCM

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: VReg 3.3V S5/5V S4

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0648	371S0694		D8100	BLC Switch Diode

ACOUSTICS E-NOISE COMPONENTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
371S0748	371S0731		D8101	INPUT DIODE
138S1078	138S0810		2.2UF_CAP	BLC 2.2uF OUTPUT CAPS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1256	376S1073		ALL	Short Protection FET
155S0831	155S0797		ALL	FB8100 to FB8107

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S1121	376S1116		Q8102	BLC Inrush FET
740S0145	740S0146		F8100	BLC Fuse

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: LCD Backlight Driver (LP8561)

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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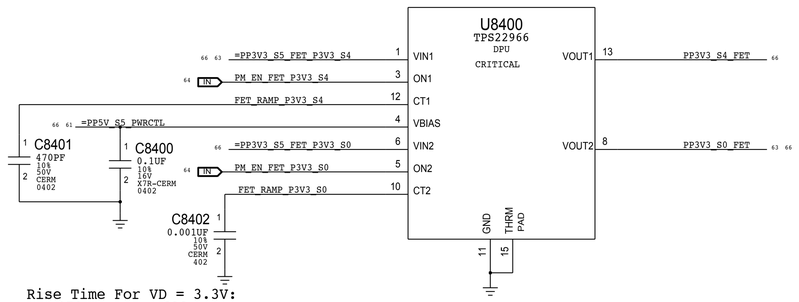
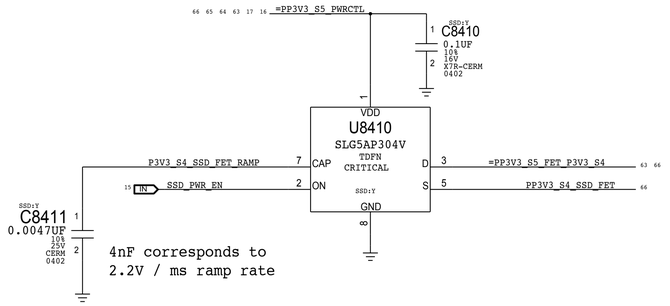
3.3V S4/S0 FET



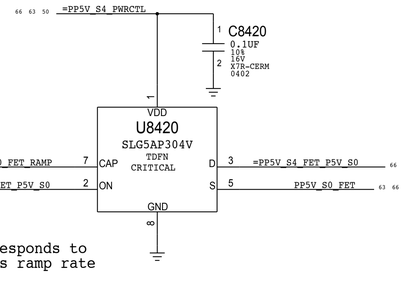
Rise Time For VD = 3.3V:
470 pF -- 603 us
1000 pF -- 1185 us

3V3 S4 SSD

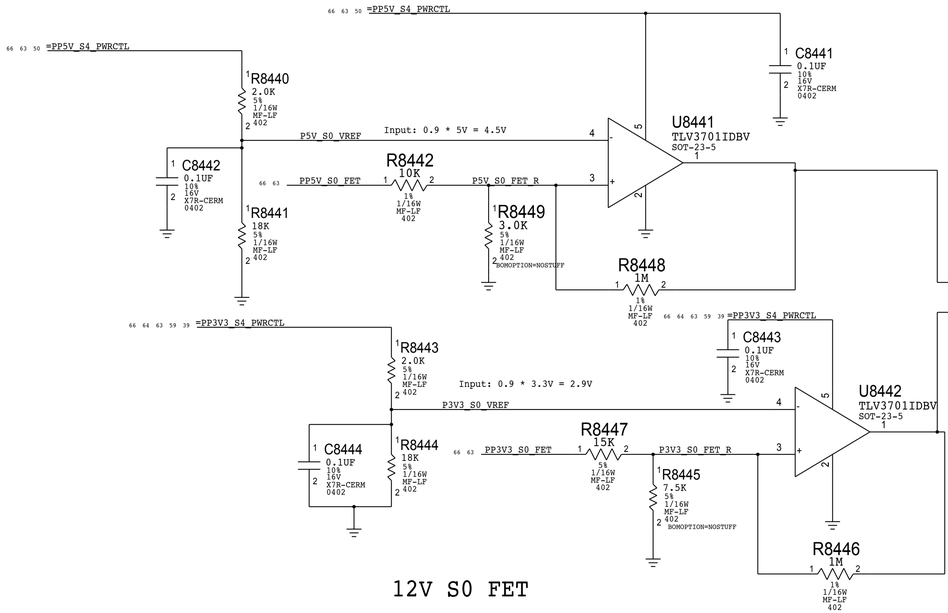


4nF corresponds to
2.2V / ms ramp rate

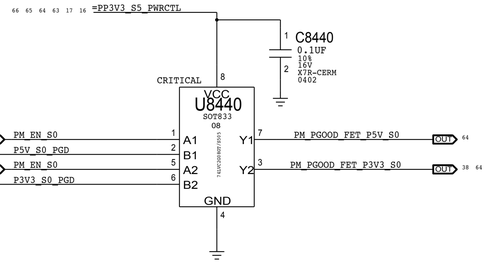
5V S0 FET



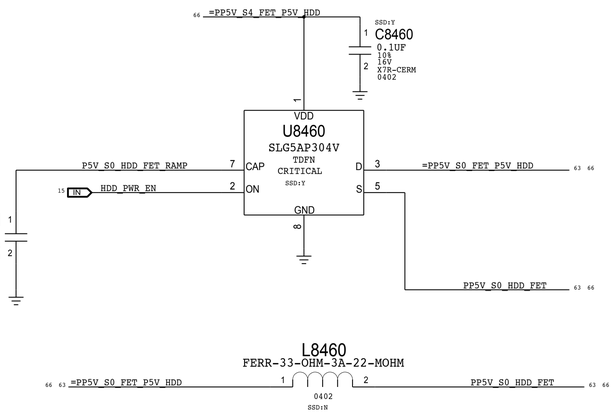
4nF corresponds to
2.2V / ms ramp rate



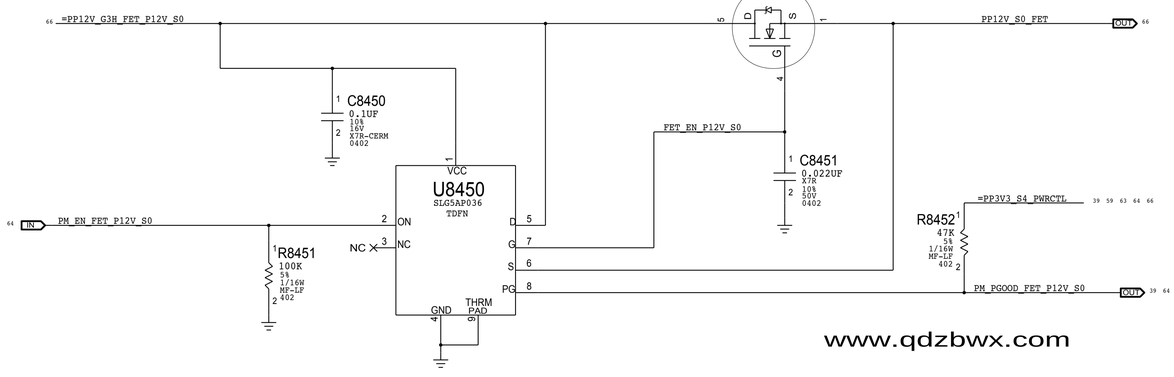
5V / 3V3 S0 PGOODs



5V HDD FET



12V S0 FET



SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE
PM FETs/LDOs

Apple Inc.

DRAWING NUMBER 051-00081 SIZE D
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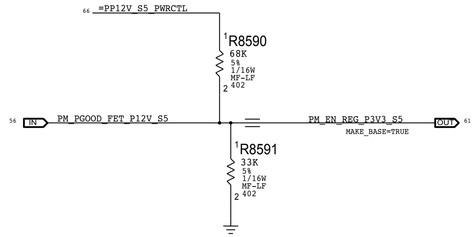
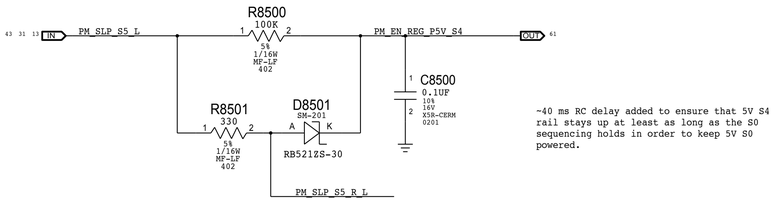
S5 Enable

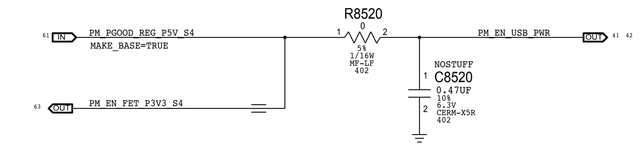


S4 Enables



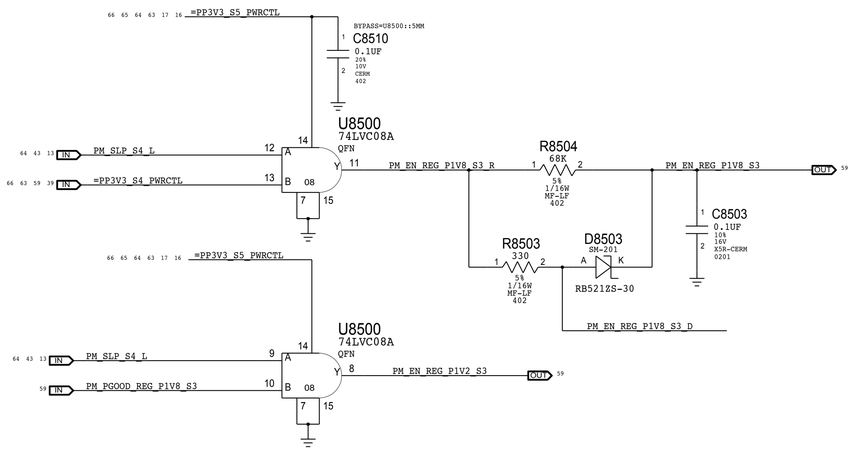
~40 ms RC delay added to ensure that 5V S4 rail stays up at least as long as the S0 sequencing holds in order to keep 5V S0 powered.

S4 USB Enable

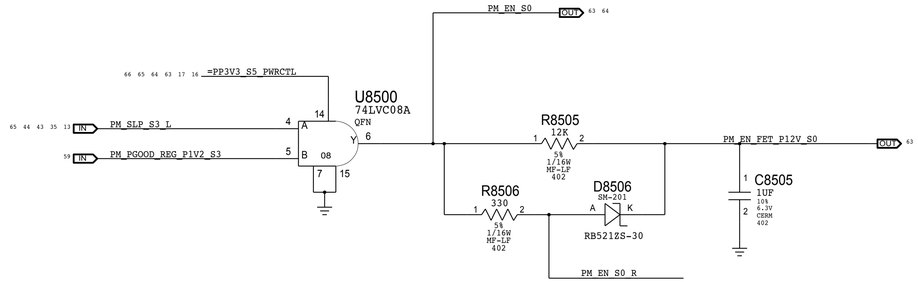


S4 TBT Port Enable

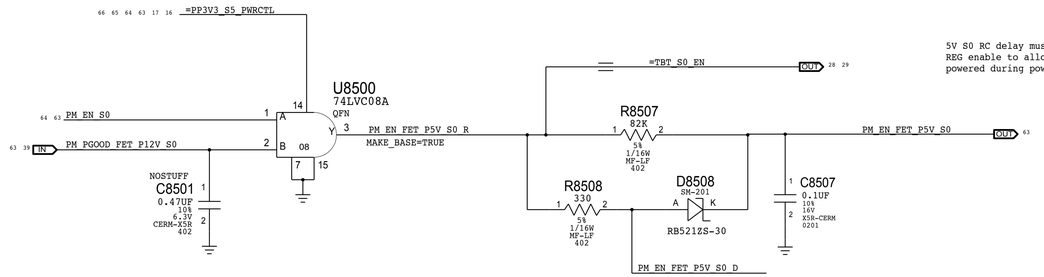
S3 Enables



S0 Enables

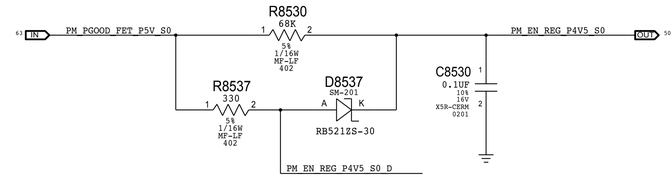


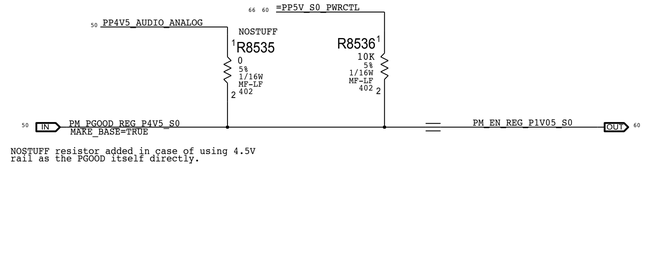
12V S0 EN RC delay must be >= downstream delay on 4.5V REG enable which in turn enables 1.05V S0. This allows for 12V S0 to hold as long as 1.05V S0 regulator is powered.



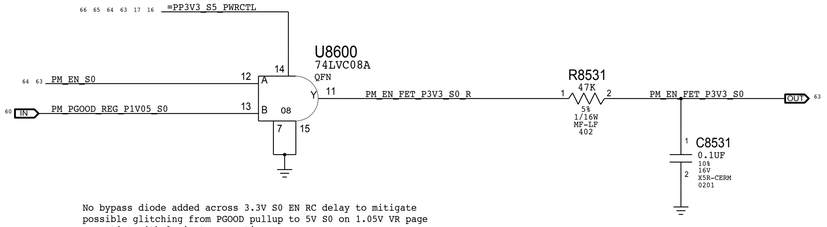
5V S0 RC delay must be >= downstream delay on 4.5V REG enable to allow for 4.5V regulator to remain powered during power down sequence.

Audio + PCH Sequencing Requirements:
4.5V -> 1.05V -> 3.3V -> 1.5V -> ALL SYS GOOD

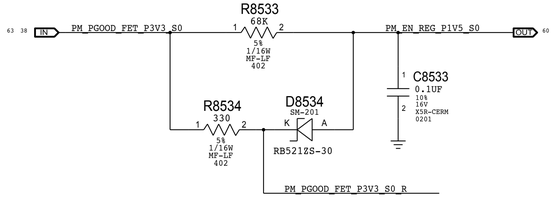




NOSTUFF resistor added in case of using 4.5V rail as the PGOOD itself directly.



No bypass diode added across 3.3V S0 EN RC delay to mitigate possible glitching from PGOOD pullup to 5V S0 on 1.05V VR page competing with logic turn on time.



SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE: PM Regulator Enables

Apple Inc.

DRAWING NUMBER: 051-00081 SIZE: D

REVISION: 3.0.0

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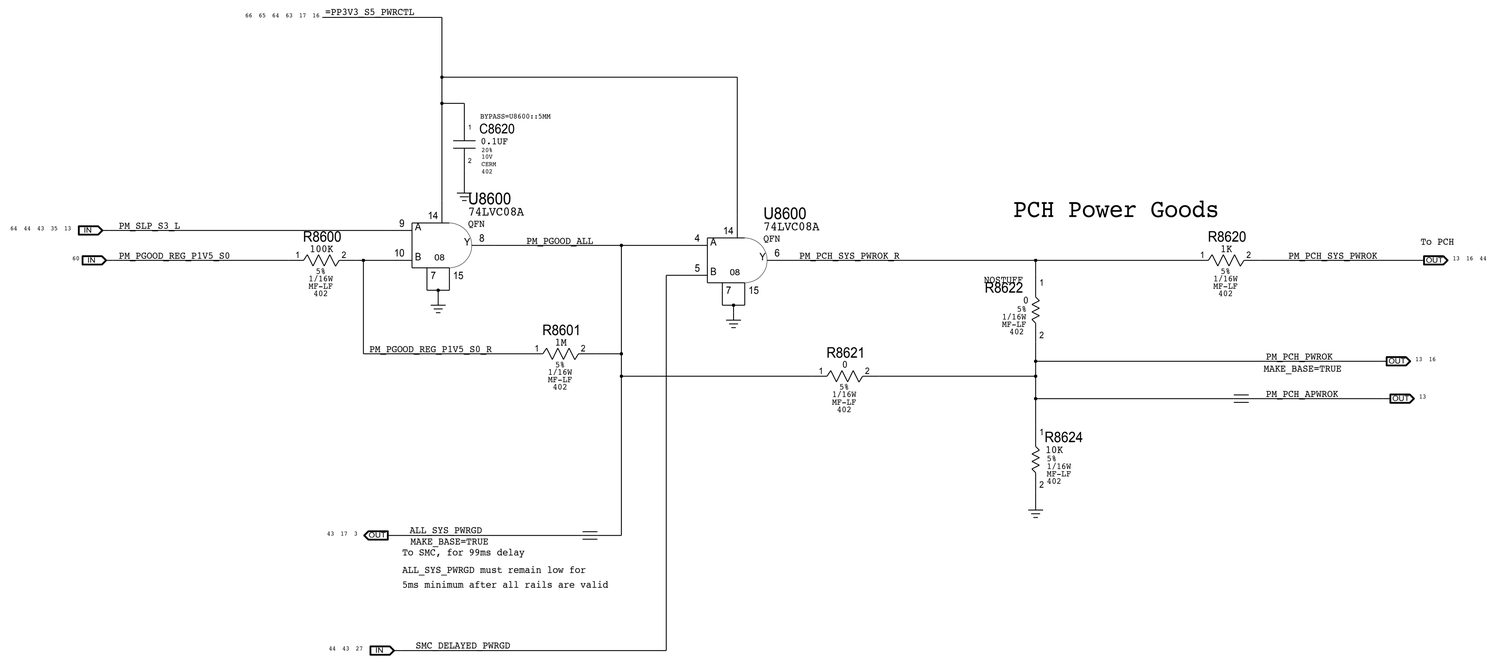
ALL_SYS_PWRGD,PCH_PWROK & SYS_PWROK Generation



Resume Reset

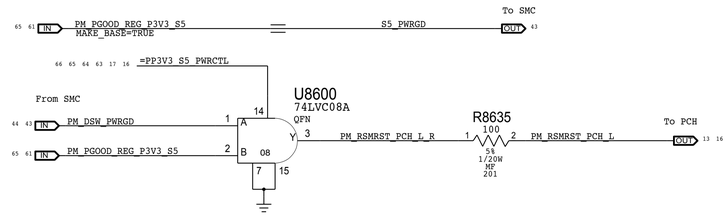
Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

Note:
The iMac J70 design does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
to allow PCH to switch suspend well to battery without excessive loading

Method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.



Rail definitions

Platform: All processor non-Core and non-Graphics (5V, 3.3V, 1.5V, 1.05V for PCH/TBT/GPU)
Uncore: 1.8V and 1.2V for DDR3

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. VCC3_3 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC3V3 ramping to 2.6V
4. VCC1_5 may power up before VCC, VCC must ramp to 0.6V within 25ms of VCC1V5 ramping to 1.35V
5. VCC may power down before VCC3_3, VCC3_3 must ramp down to 2.6V within 35ms
6. VCC may power down before VCC1_5, VCC1_5 must ramp down to 1.35V within 35ms

SYNC_MASTER=J117_ANDRES SYNC_DATE=03/24/2014

PAGE TITLE
PM Power Good

Apple Inc.

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G3 Rails

Always on: Keeps the PCH RTC alive

79 PP3V3_G3 (MAKE_BASE=TRUE)
- PP3V3_G3_RTC 17
- =PPVRTC_G3_PCH 8 12 13

G3H Rails

79 PP12V_ACDC (MAKE_BASE=TRUE)
- PP12V_G3H_ACDC 56
- =PP12V_G3H_SNS_R 47

79 PP12V_G3H (MAKE_BASE=TRUE)
- PP12V_G3H_SNS 47
- =PP12V_G3H_REG_3V42_G3H 56
- =PP12V_G3H_FET_P12V_S5 56
- =PP12V_G3H_FET_P12V_S0 63

79 PP3V42_G3H (MAKE_BASE=TRUE)
- PP3V42_G3H_REG 56
- =PP3V3_G3H_BT 31
- =PP3V3_G3H_SMC 43 44 49
- =PP3V3_G3H_RTC_D 17
- =PPVIN_G3H_SMCVREF 44
- =PP3V3_G3H_SMC_USBMUX 41
- =PP3V3_G3H_T112 45

Ground/Common

GND\G (MAKE_BASE=TRUE)

S5 Rails

Enabled when system has AC and is in S5

79 PP12V_S5 (MAKE_BASE=TRUE)
- PP12V_S5_FET 56
- =PP12V_S5_REG_P3V3P5V_S5 61
- =PP12V_S5_REG_P1V2_S3 59
- =PPHV_SW_TBTAPWRSW 28
- =PPHV_SW_TBTBPWRSW 29
- =PP12V_S5_SNS 47
- =PP12V_S5_PWRCTL 64

79 PP5V_S5 (MAKE_BASE=TRUE)

I2326
- PP5V_S5_LDO 61
- NEC =PP5V_S5_PWRCTL 61 63

79 PP3V3_S5 (MAKE_BASE=TRUE)
- PP3V3_S5_REG 61
- =PP3V3_S5_FET_P3V3_S4 63
- =PP3V3_S5_FET_P3V3_S0 63
- =PP3V3_S5_PWRCTL 16 17 63 64 65
- =PP3V3_S5_VRD 61
- =PP3V3_S5_LED 3
- =PP3V3_SUS_PCH_VCCSUS_GPIO 8 11
- =PP3V3_S5_PCH_VCCDSW 8 11
- =PP3V3_SUS_PCH_VCC_SPI 8 11 14
- =PP3V3_SUS_PCH_VCCSUS_RTC 8 11
- =PP3V3_SUS_PCH_VCCSUS_ICC 8
- =PP3V3_S5_ROM 45
- =PP3V3_S5_SENSE 47
- =PP3V3_S5_SMC 44
- =PP3V3_S4_TBTAPWRSW 28
- =PP3V3_S4_TBTBPWRSW 29
- =PP3V3_SUS_PCH_GPIO 14
- =PP3V3_S5_PCH_GPIO 13 15 50
- =PP3V3_S5_REG_P1V8_S3 59
- =PP3V3_S5_XDP 16

S4 Rails

Enabled when system has AC and is in run or sleep

79 PP5V_S4 (MAKE_BASE=TRUE)
- PP5V_S4_REG 61
- =PP5V_S4_REG_P1V2_S3 59
- =PP5V_S4_FET_P5V_S0 63
- =PP5V_S4_PWRCTL 50 63
- =PP5V_S4_USB 41 42
- =PP5V_S4_AUDIO 50
- =PP5V_S4_FET_P5V_HDD 63
- =PP5V_S4_SDCARD 36

79 PP3V3_S4 (MAKE_BASE=TRUE)
- PP3V3_S4_FET 63
- =PP3V3_S4_FET_ENET 35
- =PP3V3_S4_PWRCTL 39 59 63 64
- =PP3V3_S4_LED 3
- =PP3V3_S4_PCH_GPIO 15 18 41 42
- =PP3V3_S4_SDCARD 36
- =PP3V3_S4_SMC 44
- =PP3V3_S4_TBT 18 26 27 28 29 64
- =PP3V3_S4_AP 31 44
- =PP3V3_S4_REG_P1V5_S0 60

S3 Rails

Enabled when system is in run or sleep

79 PP3V3_ENET (MAKE_BASE=TRUE)
- PP3V3_ENET_FET 35
- =PP3V3_ENET_PHY 34 35

77 PP1V8_S3 (MAKE_BASE=TRUE)
- PP1V8_S3_REG 59
- =PP1V8_S3_DDR 21 22 23 24
- =PP1V8_S3_CAMERA_FET 38
- =PP1V8_S3_PWRCTL 60
- =PP1V8_S3_REG_P1V5_S0 60

77 PP1V2_S3 (MAKE_BASE=TRUE)
- PP1V2_S3_REG 59
- =PP1V2_S3_SNS_DDR_R 47

77 PP1V2_S3_DDR (MAKE_BASE=TRUE)
- PP1V2_S3_SNS_DDR 47
- =PP1V2_S3_LDO_DDRVTT 59
- =PP1V2_S3_DDR_MEMVREF 20
- =PP1V2_S3_DDR_VDD2 21 22 23 24
- =PP1V2_S3_DDR_VDDCA 21 22 23 24
- =PP1V2_S3_DDR_VDDQ 21 22 23 24
- =PP1V2_S3_MEM_VTTPWRCTL 18
- =PPVMEMIO_S0_CPU 8 10
- =PP1V2_S3_CAMERA_FET 38

77 PP0V6_S3_DDRVTT (MAKE_BASE=TRUE)
- PP0V6_S3_DDRVTT_LDO 59
- =PP0V6_S3_DDRVTT_A 25
- =PP0V6_S3_DDRVTT_B 25

S0 Rails

Enabled when system is in run

79 PP12V_S0 (MAKE_BASE=TRUE)
- PP12V_S0_FET 63
- =PP12V_S0_REG_CPUVCC_S0 57 58
- =PP12V_S0_REG_P1V05_S0 60
- =PP12V_S0_AUDIO_SPKRAMP 52 53
- =PP12V_S0_BKLT 62
- =PP12V_S0_FAN 49
- =PP12V_S0_LCD 39

79 PP5V_S0 (MAKE_BASE=TRUE)
- PP5V_S0_FET 63
- =PP5V_S0_REG_CPUVCC_S0 57 58
- =PP5V_S0_REG_P1V05_S0 60
- =PP5V_S0_BKLT 62
- =PP5V_S0_FET_P5V_HDD 63
- =PP5V_S0_CAMERA 37 38
- =PP5V_S0_PCH_STRAP 17
- =PP5V_S0_PWRCTL 60 64

79 PP5V_S0_HDD (MAKE_BASE=TRUE)
- PP5V_S0_HDD_FET 63
- =PP5V_S0_SATA 33

79 PP3V3_S0 (MAKE_BASE=TRUE)
- PP3V3_S0_FET 63
- =PP3V3_S0_VRD 56
- =PP3V3_S0_AUDIO 37 50
- =PP3V3_S0_AUDIO_DIG 51 54
- =PP3V3_S0_AUDIO_SPKRAMP 52 53
- =PP3V3_S0_DP 30 39
- =PP3V3_S0_ENET 34
- =PP3V3_S0_FAN 49
- =PP3V3_S0_INTDPMUX 40
- =PP3V3_S0_LED 3
- =PP3V3_S0_PCH 17
- =PP3V3_S0_PCH_VCC3_3_GPIO 8 11
- =PP3V3_S0_PCH_VCCTS 8 11
- =PP3V3_S0_PCH_VCCSDIO 8 11
- =PP3V3_S0_CAMPWREN
- =PP3V3_S0_SDCARD 36
- =PP3V3_S0_SENSE 32 33 47 48
- =PP3V3_S0_SMBUS 46
- =PP3V3_S0_SMBUS_SMC_0 46
- =PP3V3_S0_SMBUS_SMC_1 39 46
- =PP3V3_S0_SMBUS_SMC_2 46
- =PP3V3_S0_SMBUS_SMC_3 46
- =PP3V3_S0_SMC 44
- =PP3V3_S0_BKLT_VDDIO 62
- =PP3V3_S0_PCH_GPIO 12 13 15 16 27
- =PP3V3_S0_CAMERA 37 38
- =PP3V3_S0_ALS 37
- =PP3V3_S0_MEM_VTTPWRCTL 18
- =PP3V3_S0_PWRCTL 60

79 PP3V3_S4_SSD (MAKE_BASE=TRUE)
- PP3V3_S4_SSD_FET 63
- =PPSSD_S4_SNS_R 47

79 PPSSD_S4 (MAKE_BASE=TRUE)
- PPSSD_S4_SNS 47
- =PPSSD_S4_CONN 32

79 PP1V5_S0 (MAKE_BASE=TRUE)
- PP1V5_S0_REG 60
- =PP1V5_S0_SENSE 33
- =PP1V5_S0_PCH_VCCTS 8
- =PP1V5_S0_AUDIO_DIG 51
- =PP1V5_S0_PCH_VCCSUSHDA 8 11 17

77 PP1V05_S0 (MAKE_BASE=TRUE)
- PP1V05_S0_REG 60
- =PP1V05_S0_PCH_VCC 8 11
- =PP1V05_S0_PCH_VCCASW 8 11
- =PP1V05_S0_PCH_VCCCLK 8 11
- =PP1V05_S0_PCH_VCCIO_USB2 8 11
- =PP1V05_S0_PCH_VCCHSIO 8 11
- =PP1V05_S0_PCH_VCCIO_HSIO 8
- =PP1V05_S0_PCH_PLLFILTERS 11
- =PP1V05_S0_SMC 44
- =PP1V05_S0_XDP 16
- =PP1V05_S0_CPU_VCCST 6 8 15 16 17
- =PP1V05_S0_PCH_VCCPLL_HSIO 11

78 PPCPUVCC_S0_CPU (MAKE_BASE=TRUE)
- PPCPUVCC_S0_REG 58
- =PPCPUVCC_S0_CPU 47
- =PPVCC_S0_CPU 8 10

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE: Power Aliases

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PCH Miscellaneous

12 TP_HDA_SDIN1 — NC_HDA_SDIN1
MAKE_BASE=TRUE NO_TEST=1

12 TP_PCIE_CLK100M_CAMERAP — NC_PCIE_CLK100M_CAMERAP
MAKE_BASE=TRUE NO_TEST=1

12 TP_PCIE_CLK100M_CAMERAN — NC_PCIE_CLK100M_CAMERAN
MAKE_BASE=TRUE NO_TEST=1

12 TP_PCIE_CLK100M_FWP — NC_PCIE_CLK100M_FWP
MAKE_BASE=TRUE NO_TEST=1

12 TP_PCIE_CLK100M_FWN — NC_PCIE_CLK100M_FWN
MAKE_BASE=TRUE NO_TEST=1

Unused Thunderbolt Aliases

26 TP_TBT_PCIE_RESET0_L — NC_TBT_PCIE_RESET0_L
MAKE_BASE=TRUE NO_TEST=1

SYNC_MASTER=J16_MLB_IG SYNC_DATE=08/27/2013

PAGE TITLE: Unused Signal Aliases

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Functional / ICT Test

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J70 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	*	Y	0.145 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.092 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.150 MM	0.076 MM	=STANDARD	0.120 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.174 MM	0.085 MM	=STANDARD	0.120 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
73_OHM_DIFF	*	Y	0.141 MM	0.076 MM	=STANDARD	0.130 MM	0.1 MM
73_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.120 MM	0.076 MM	=STANDARD	0.140 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.085 MM	=STANDARD	0.140 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.108 MM	0.076 MM	=STANDARD	0.150 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.099 MM	0.076 MM	=STANDARD	0.170 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.085 MM	=STANDARD	0.175 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.076 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.095 MM	0.085 MM	=STANDARD	0.210 MM	0.1 MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	*	0.070 MM	?

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

Board Stack-up

Finished board thickness: 1.58 mm

_____	Top	Signal	1/3 OZ (CU PLATED)
_____		Prepreg	0.070 MM
_____	2	Plane	1/3 OZ (CU PLATED)
_____		Prepreg	0.070 MM
_____	3	Signal	0.5 OZ
_____		Prepreg	0.435 MM
_____	4	Plane	1 OZ
_____		Core	0.152 MM
_____	5	Plane	1 OZ
_____		Prepreg	0.435 MM
_____	6	Signal	0.5 OZ
_____		Prepreg	0.070 MM
_____	2	Plane	1/3 OZ (CU PLATED)
_____		Prepreg	0.070 MM
_____	Btm	Signal	1/3 OZ (CU PLATED)

SYNC_MASTER=J70_NICK SYNC_DATE=09/12/2013

PAGE TITLE: J70 RULE DEFINITIONS

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DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
DDR_73D	*	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF	=73_OHM_DIFF
DDR_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

Minimum diff spacing is 4 mil
Table 4-5, Intel Doc# 486712

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_70D
DDR_CTRL_PHY	*	DDR_40S
DDR_CMD_PHY	*	DDR_40S
DDR_DQ_PHY	*	DDR_40S
DDR_DQS_PHY	*	DDR_70D
DDR_COMP_PHY	*	DDR_COMP

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR	*	=2:1_SPACING	?

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	*	=5:1_SPACING	?
DDR_CTRL_ISO	*	=3.5:1_SPACING	?
DDR_CTRL2CTRL	*	=2:1_SPACING	?
DDR_CMD_ISO	*	=3.5:1_SPACING	?
DDR_CMD2CMD	*	=2:1_SPACING	?
DDR_DATA_ISO	*	=4:1_SPACING	?
DDR_STROBE_ISO	*	=3:1_SPACING	?
DDR_DQ2DQ	*	=2:1_SPACING	900
DDR_DQ2DQS	*	=3:1_SPACING	?
DDR_BL2BL	*	=3:1_SPACING	?
DDR_CH2CH	*	=6.5:1_SPACING	?
DDR_COMP_ISO	*	0.381 MM	?

Main Segment Min Spacing Rules (mils) (HSW U/Y PDG, Intel Doc# 502636)

BDW does not have a separate power spec from HSW, so this document is still accurate

Table	Trace	Design	Iso	Design	Comments
6-14	4	(diff)	16	19.69	CLK trace spacing controlled by =70_OHM_DIFF.
6-14	7.5	7.87	12	13.78	
6-14	7.5	7.87	12	13.78	
6-14	7.5	7.87	16	11.81	DQ to other signals not in the same bytelane (but not ch)
			12	11.81	DQS to other signals of the same channel
			7.5	7.87	DQ to DQ in the same bytelane of the same channel
			12	11.81	DQ to DQS in the same bytelane of the same channel
			16	11.81	DQ or DQS in different bytelanes of the same channel
			?	25.59	DQ or DQS in different channels. ISO RULE NOT IN PDG
			-	25.59	DDR3 to any other signal not DDR3

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_COMP	*	*	DDR_COMP_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_STROBE_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_STROBE_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME to win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set	Physical	Spacing		
Channel A				
T178 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<0>	? 21 25
T179 DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<0>	? 21 25
T258 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1>	? 22 25
T259 DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1>	? 22 25
T262 DDR_A_CS0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<0>	? 21 22 25
T181 DDR_A_CS1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1>	? 21 22 25
T182 DDR_A_ODT	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<0>	? 21 22 25
T180 ?	?	?	MEM_A_CKE<1..0>	? 21 25
T247 ?	?	?	MEM_A_CKE<3..2>	? 22 25
T187 ?	?	?	MEM_A_CAA<9..0>	? 21 25
T184 ?	?	?	MEM_A_CAB<9..0>	? 22 25
T188 ?	?	?	MEM_A_DQ<7..0>	? 19
T189 ?	?	?	MEM_A_DQ<15..8>	? 19
T191 ?	?	?	MEM_A_DQ<23..16>	? 19
T190 ?	?	?	MEM_A_DQ<31..24>	? 19
T192 ?	?	?	MEM_A_DQ<39..32>	? 19
T193 ?	?	?	MEM_A_DQ<47..40>	? 19
T194 ?	?	?	MEM_A_DQ<55..48>	? 19
T195 ?	?	?	MEM_A_DQ<63..56>	? 19
T196 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	? 19
T197 DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	? 19
T198 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	? 19
T199 DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	? 19
T200 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	? 19
T201 DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	? 19
T202 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	? 19
T203 DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	? 19
T204 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	? 19
T205 DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	? 19
T206 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	? 19
T207 DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	? 19
T208 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	? 19
T209 DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	? 19
T210 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	? 19
T211 DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	? 19
Channel B				
T212 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<0>	? 23 25
T213 DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<0>	? 23 25
T260 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1>	? 24 25
T261 DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1>	? 24 25
T263 DDR_B_CS0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<0>	? 23 24 25
T215 DDR_B_CS1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1>	? 23 24 25
T216 DDR_B_ODT	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<0>	? 23 24 25
T214 ?	?	?	MEM_B_CKE<1..0>	? 23 25
T250 ?	?	?	MEM_B_CKE<3..2>	? 24 25
T217 ?	?	?	MEM_B_CAA<9..0>	? 23 25
T218 ?	?	?	MEM_B_CAB<9..0>	? 24 25
T222 ?	?	?	MEM_B_DQ<7..0>	? 19
T223 ?	?	?	MEM_B_DQ<15..8>	? 19
T225 ?	?	?	MEM_B_DQ<23..16>	? 19
T226 ?	?	?	MEM_B_DQ<31..24>	? 19
T224 ?	?	?	MEM_B_DQ<39..32>	? 19
T227 ?	?	?	MEM_B_DQ<47..40>	? 19
T228 ?	?	?	MEM_B_DQ<55..48>	? 19
T229 ?	?	?	MEM_B_DQ<63..56>	? 19
T230 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	? 19
T231 DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	? 19
T232 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	? 19
T233 DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	? 19
T234 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	? 19
T235 DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	? 19
T237 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	? 19
T236 DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	? 19
T238 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	? 19
T239 DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	? 19
T240 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	? 19
T241 DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	? 19
T242 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	? 19
T243 DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	? 19
T244 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	? 19
T245 DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	? 19
SM COMP				
T257	?	?	CPU_SM_RCOMP<0..2>	6

SYNC_MASTER=J70_NICK SYNC_DATE=09/30/2013

PAGE TITLE: DDR3 Constraints

Apple Inc.

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PCI Express

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
PCIE_COMP	*	Y	0.305 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	PCIE_COMP
CPU_ASYNC_PHY	*	CPU_50S

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?
CPU_ASYNC_ISO	*	=3:1_SPACING	?
CPU_MS_ISO	TOP,BOTTOM	=4.5:1_SPACING	?
CPU_MS_ISO	*	=3:1_SPACING	?

Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO
CPU_ASYNC	*	*	CPU_ASYNC_ISO
CPU_ASYNC_MS	*	*	CPU_MS_ISO

PEG Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	80	16	15.75	PCIe Gen3. Allow looser spacing for same direction on stripline per Anil

CPU ASYNCHRONOUS

Electrical Contraint Set	Physical	Spacing		
1573	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_L	6 43 44 57
1574	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PROCHOT_R_L	6
1575 PECI	CPU_ASYNC_PHY	CPU_ASYNC_MS	CPU_PECI	6 44
1576	CPU_ASYNC_PHY	CPU_ASYNC_MS	SMC_PECI_L	43 44
1578	CPU_ASYNC_PHY	CPU_ASYNC	CPU_CATERR_L	6 44
1577	CPU_ASYNC_PHY	CPU_ASYNC	CPU_PWRGD	6
1581	CPU_ASYNC_PHY	CPU_ASYNC	PM_THRMTRIP_L	15 44
1581	CPU_ASYNC_PHY	CPU_ASYNC	CPU_VCCST_PWRGD	8 16 17
1584	CPU_ASYNC_PHY	CPU_ASYNC	XDP_CPU_VCCST_PWRGD	16
1585	CPU_ASYNC_PHY	CPU_ASYNC	PLT_RESET_L	13 15 16 18
1582 ?	?	?	XDP_BPM_L<1..0>	6 16

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing		
CPU OPI Compensation				
1570	COMP_PCIE_PHY	COMP_PCIE	CPU_OPI_RCOMP	6
CPU eDP Compensation				
1571	COMP_PCIE_PHY	COMP_PCIE	MCP_EDP_RCOMP	5
1572	COMP_PCIE_PHY	COMP_PCIE	CPU_CFG_RCOMP	6

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PAGE TITLE: CPU CONSTRAINTS

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Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_85D

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_SAME_DIR	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_SAME_DIR	*	=3.5X_DIELECTRIC	?
PCIE_ALT_DIR	*	=5X_DIELECTRIC	?
PCIE_ISO	*	=4:1_SPACING	?

TBT x4 PCIE Spacing Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_TBT_R2D	PCIE_TBT_R2D	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_D2R	*	PCIE_SAME_DIR
PCIE_TBT_D2R	PCIE_TBT_R2D	*	PCIE_ALT_DIR
PCIE_TBT_D2R	*	*	PCIE_ISO
PCIE_TBT_R2D	*	*	PCIE_ISO

PCH x1 PCIE Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO

PCIe (PCH)

Electrical Contraint Set		Physical	Spacing		
x4 Thunderbolt					
H140	PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P	12 26
H141	PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N	12 26
H132	?	?	?	PCIE_TBT_R2D_P<2..0>	26
H133	?	?	?	PCIE_TBT_R2D_N<2..0>	26
H134		?	?	PCIE_TBT_R2D_C_P<2..0>	14 26
H135		?	?	PCIE_TBT_R2D_C_N<2..0>	14 26
H179	PCIE_GEN2_R2D_RVSD	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_P<3>	26
H180	PCIE_GEN2_R2D_RVSD	PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_N<3>	26
H181		PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_P<3>	14 26
H182		PCIE_PHY	PCIE_TBT_R2D	PCIE_TBT_R2D_C_N<3>	14 26
H183	PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<0>	14 26
H184	PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<0>	14 26
H185		PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<0>	26
H186		PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<0>	26
H176	?	?	?	PCIE_TBT_D2R_P<2..1>	14 26
H177	?	?	?	PCIE_TBT_D2R_N<2..1>	14 26
H178		?	?	PCIE_TBT_D2R_C_P<2..1>	26
H179		?	?	PCIE_TBT_D2R_C_N<2..1>	26
H187	PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_P<3>	14 26
H188	PCIE_GEN2_D2R	PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_N<3>	14 26
H189		PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_P<3>	26
H190		PCIE_PHY	PCIE_TBT_D2R	PCIE_TBT_D2R_C_N<3>	26
x1 AirPort					
H142	PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	31
H143	PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	31
H144		PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	14 31
H146		PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	14 31
H145	PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	14 31
H147	PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	14 31
H148	PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P	12 31
H149	PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N	12 31
x1 Caesar IV					
H151	PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	34
H150	PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	34
H152		PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	14 34
H154		PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	14 34
H153	PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	14 34
H155	PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	14 34
H156		PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	34
H157		PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	34
H158	PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P	12 34
H159	PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N	12 34
x2 SSD					
H172	PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_P	12 32
H173	PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_SSD_N	12 32
PCH PCIE Compensation					
H178		COMP_PCIE_PHY	COMP_PCIE	PCH_PCIE_RCOMP	14

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PCH PCIe/DMI Constaints

Apple Inc.

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SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_85D
COMP_SATA_PHY	*	SATA_50S
SATA_PHY_90	*	SATA_90D

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=6:1_SPACING	?
COMP_SATA_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
J97 SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_P	33
J92 SATA_R2D	SATA_PHY_90	SATA	SATA_HDD_R2D_N	33
J85	SATA_PHY_90	SATA	SATA_HDD_R2D_C_P	12 33
J84	SATA_PHY_90	SATA	SATA_HDD_R2D_C_N	12 33
J74 SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_P	12 33
J75 SATA_D2R	SATA_PHY_90	SATA	SATA_HDD_D2R_N	12 33
J87	SATA_PHY_90	SATA	SATA_HDD_D2R_C_P	33
J97	SATA_PHY_90	SATA	SATA_HDD_D2R_C_N	33
PCH SATA Port 1 (SSD)				
J96 ?	?	?	PCIE_SSD_R2D_P<0..1>	12 32
J97 ?	?	?	PCIE_SSD_R2D_N<0..1>	12 32
J115 ?	?	?	SSD_R2D_C_P<0..1>	32
J116 ?	?	?	SSD_R2D_C_N<0..1>	32
J103 ?	?	?	PCIE_SSD_D2R_P<0..1>	12 32
J102 ?	?	?	PCIE_SSD_D2R_N<0..1>	12 32
PCH SATA Compensation				
J104	COMP_SATA_PHY	COMP_SATA	PCH_SATA_RCOMP	12

XDP

Electrical Contraint Set	Physical	Spacing		
CPU XDP				
J37 ?	?	?	XDP_BPM_L<7..2>	6 16
J38 XDP_CPU_CFG_PD	XDP_PHY	XDP	CPU_CFG<0>	6 16
J124 XDP_CPU_CFG1_PD	XDP_PHY	XDP	CPU_CFG<1>	6 16
J117 XDP_CPU_CFG	XDP_PHY	XDP	CPU_CFG<2>	6 16
J100 ?	XDP_PHY	XDP	CPU_CFG<3>	6 16
J118 XDP_CPU_CFG_PD	XDP_PHY	XDP	CPU_CFG<4>	6 16
J101 ?	?	?	CPU_CFG<7..5>	6 16
J103 ?	?	?	CPU_CFG<10..8>	6 16
J122 ?	?	?	CPU_CFG<19..11>	6 16
J45 XDP_CPU_TCK	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	6 16
J44 XDP_CPU_TMS	XDP_PHY	XDP	XDP_CPU_TMS	6 16
J47	XDP_PHY	XDP	XDP_CPU_TDI	6 16
J48	XDP_PHY	XDP	XDP_CPU_TDO	6 16
J119 XDP_CPU_TRST_L	XDP_PHY	XDP	XDP_CPU_TRST_L	6 16
PCH XDP				
J43	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	12 16
J56	XDP_PHY	XDP	XDP_PCH_TMS	12 16
J51	XDP_PHY	XDP	XDP_PCH_TDI	12 16
J52	XDP_PHY	XDP	XDP_PCH_TDO	12 16

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_55S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
CLK_JTAG_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	CLK_JTAG_ISO

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	55	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

SYNC_MASTER=J70_TONY SYNC_DATE=10/23/2013

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SATA/FDI/XDP Constraints

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PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH_ISO	*	=4:1_SPACING	?
COMP_PCH_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCH	*	*	CLK_PCH_ISO
COMP_PCH	*	*	COMP_PCH_ISO

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC_ISO	*	=1.5:1_SPACING	?
CLK_LPC_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LPC	*	*	LPC_ISO
CLK_LPC	*	*	CLK_LPC_ISO

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA_ISO	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	HDA_ISO

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL_ISO	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XTAL	*	*	XTAL_ISO

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	SPI_ISO

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
R336	?	?	LPC_AD<3..0>	14 43
R335	?	?	LPC_AD_R<3..0>	14
R338	LPC_55S	LPC	LPC_FRAME_L	14 43
R337	LPC_55S	LPC	LPC_FRAME_R_L	14
LPC Clocks				
R341	CLK_LPC_55S	CLK_LPC	LPC_CLK24M_SMC	17 43
R342	CLK_LPC_55S	CLK_LPC	LPC_CLK24M_SMC_R	12 17

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
R417	CLK_XTAL	XTAL	PCH_CLK24M_XTALIN	12 17
R418	CLK_XTAL	XTAL	PCH_CLK24M_XTALOUT	12 17
R419	CLK_XTAL	XTAL	PCH_CLK24M_XTALOUT_R	17
PCH RTC 32K				
R347	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	12 17
R348	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	12 17
R352	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	17
SMC 32K				
R349	CLK_PCH_55S	CLK_PCH	PM_CLK32K_SUSCLK_R	13 44
R350	CLK_PCH_55S	CLK_PCH	SMC_CLK32K	43 44

25 MHz XTALS

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
R378	CLK_XTAL	XTAL	TBT_CLK25M_IN	17 26
R380	CLK_XTAL	XTAL	TBT_CLK25M_OUT	17 26
R381	CLK_XTAL	XTAL	TBT_CLK25M_OUT_R	17
R384	CLK_XTAL	XTAL	ENET_XTAL_IN	17 34
R385	CLK_XTAL	XTAL	ENET_XTAL_OUT	17 34
R386	CLK_XTAL	XTAL	ENET_XTAL_OUT_R	17

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
R353 HDA_CLK	HDA	HDA	HDA_BIT_CLK	12 51
R361	HDA	HDA	HDA_BIT_CLK_R	12
R363 HDA_RST	HDA	HDA	HDA_RST_L	12 51
R362	HDA	HDA	HDA_RST_R_L	12
R364 HDA_OUT	HDA	HDA	HDA_SDOUT	12 51
R367	HDA	HDA	HDA_SDOUT_R	12 17
R366 HDA_SYNC	HDA	HDA	HDA_SYNC	12 51
R368	HDA	HDA	HDA_SYNC_R	12
R365 HDA_IN	HDA	HDA	HDA_SDIN0	12 51
SPDIF				
R370	HDA	HDA	DP_INT_SPDIF_AUDIO	39 51 80
R371	HDA_55S	?	SPDIF_OUT_JACK	51 54
R420	HDA_55S	?	CS4208_SPDIF_IN	51
R421	HDA_55S	?	CS4208_SPDIF_OUT	51

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
R391	SPI_50S	SPI	SPI_CLK_R	14 45
R392	SPI_50S	SPI	SPI_CLK	45
R393	SPI_50S	SPI	SPI_ALT_CLK	45
R406	SPI_50S	SPI	SPI_SMC_CLK	43 45
R407	SPI_50S	SPI	SPI_MLB_CLK	45
R394	SPI_50S	SPI	SPI_CS0_R_L	14 45
R395	SPI_50S	SPI	SPI_CS0_L	45
R396	SPI_50S	SPI	SPI_ALT_CS_L	45
R409	SPI_50S	SPI	SPI_SMC_CS_L	43 45
R397	SPI_50S	SPI	SPI_MLB_CS_L	45
R399	SPI_50S	SPI	SPI_MOSI_R	14 45
R400	SPI_50S	SPI	SPI_MOSI	45
R401	SPI_50S	SPI	SPI_ALT_MOSI	45
R410	SPI_50S	SPI	SPI_SMC_MOSI	43 45
R411	SPI_50S	SPI	SPI_MLB_MOSI	45
R404	SPI_50S	SPI	SPI_MISO	45
R403	SPI_50S	SPI	SPI_ALT_MISO	45
R412	SPI_50S	SPI	SPI_SMC_MISO	43 45
R413	SPI_50S	SPI	SPI_MLB_MISO	45
R405	SPI_50S	SPI	SPIROM_USE_MLB	15 45

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PCH and BR Constraints

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USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D

USB-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=3:1_SPACING	?
USB2_ISO	TOP,BOTTOM	=3:1_SPACING	?
USB3_ISO	*	=5.5:1_SPACING	?
USB3_ISO	TOP,BOTTOM	=5.5:1_SPACING	?

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
12.2.1	90	90	12	11.81	USB 2.0
13.3.1	85	85	20	21.65	USB 3.0

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB3	*	*	USB3_ISO

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S
CIV_SPI	*	SPI_55S

CIV-specific Spacing Definitions

Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints

Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_DIFF	*	*	ENET_DIFF_ISO
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF
ENET_TRANS	*	*	ENET_TRANS_ISO
COMP_ENET	*	*	COMP_ENET_ISO
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF

2 kV isolation

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

Camera Processor-to-Camera Sensor I/F (SMIA/MIPI)

Camera Processor's SMIA Interface Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D

Camera Processor's SMIA Interface Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
J326 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_D2R_P	14 41
J325 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_D2R_N	14 41
J331	USB3_PHY	USB3	USB3_EXTA_D2R_F_P	41
J332	USB3_PHY	USB3	USB3_EXTA_D2R_F_N	41
J417 USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTA_R2D_P	41
J418 USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTA_R2D_N	41
J415	USB3_PHY	USB3	USB3_EXTA_R2D_F_P	41
J416	USB3_PHY	USB3	USB3_EXTA_R2D_F_N	41
J403	USB3_PHY	USB3	USB3_EXTA_R2D_CF_P	14 41
J404	USB3_PHY	USB3	USB3_EXTA_R2D_CF_N	14 41
J417 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_P	14 41
J418 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_EXTA_N	14 41
J419	USB2_PHY	USB2	USB2_EXTA_MUXED_P	41
J420	USB2_PHY	USB2	USB2_EXTA_MUXED_N	41
J331	USB2_PHY	USB2	USB2_EXTA_P	41
J324	USB2_PHY	USB2	USB2_EXTA_N	41
External Port B (J4610)				
J421 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_D2R_P	14 41
J422 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_D2R_N	14 41
J423	USB3_PHY	USB3	USB3_EXTB_D2R_F_P	41
J424	USB3_PHY	USB3	USB3_EXTB_D2R_F_N	41
J425 USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTB_R2D_P	41
J427 USB3_TX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTB_R2D_N	41
J426	USB3_PHY	USB3	USB3_EXTB_R2D_F_P	41
J428	USB3_PHY	USB3	USB3_EXTB_R2D_F_N	41
J405	USB3_PHY	USB3	USB3_EXTB_R2D_CF_P	14 41
J406	USB3_PHY	USB3	USB3_EXTB_R2D_CF_N	14 41
J429 USB2_CONN	USB2_PHY	USB2	USB_EXTB_P	14 41
J430 USB2_CONN	USB2_PHY	USB2	USB_EXTB_N	14 41
J414	USB2_PHY	USB2	USB2_EXTB_P	41
J433	USB2_PHY	USB2	USB2_EXTB_N	41
External Port C (J4700)				
J437 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_D2R_P	14 42
J439 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_D2R_N	14 42
J438	USB3_PHY	USB3	USB3_EXTC_D2R_F_P	42
J440	USB3_PHY	USB3	USB3_EXTC_D2R_F_N	42
J441 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_R2D_P	42
J442 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_R2D_N	42
J444	USB3_PHY	USB3	USB3_EXTC_R2D_F_P	42
J443	USB3_PHY	USB3	USB3_EXTC_R2D_F_N	42
J498	USB3_PHY	USB3	USB3_EXTC_R2D_CF_P	14 42
J497	USB3_PHY	USB3	USB3_EXTC_R2D_CF_N	14 42
J446 USB2_CONN	USB2_PHY	USB2	USB_EXTC_P	14 42
J445 USB2_CONN	USB2_PHY	USB2	USB_EXTC_N	14 42
J450	USB2_PHY	USB2	USB2_EXTC_P	42
J452	USB2_PHY	USB2	USB2_EXTC_N	42
External Port D (J4710)				
J453 USB3_RX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTD_D2R_P	14 42
J455 USB3_RX_CONN_RVSD	USB3_PHY	USB3	USB3_EXTD_D2R_N	14 42
J454	USB3_PHY	USB3	USB3_EXTD_D2R_F_P	42
J456	USB3_PHY	USB3	USB3_EXTD_D2R_F_N	42
J457 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_R2D_P	42
J458 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_R2D_N	42
J460	USB3_PHY	USB3	USB3_EXTD_R2D_F_P	42
J459	USB3_PHY	USB3	USB3_EXTD_R2D_F_N	42
J499	USB3_PHY	USB3	USB3_EXTD_R2D_CF_P	14 42
J500	USB3_PHY	USB3	USB3_EXTD_R2D_CF_N	14 42
J462 USB2_CONN	USB2_PHY	USB2	USB_EXTD_P	14 42
J461 USB2_CONN	USB2_PHY	USB2	USB_EXTD_N	14 42
J466	USB2_PHY	USB2	USB2_EXTD_P	42
J468	USB2_PHY	USB2	USB2_EXTD_N	42
Camera (J3510)				
J374 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P	14 37
J376 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_N	14 37
PCH USB Compensation				
J381	PCH_55S	COMP_PCH	PCH_USB_RBIAS	14

RMH Love

Electrical Contraint Set	Physical	Spacing		
J409 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_P	14 31
J410 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_N	14 31
J505 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_P	31
J506 USB2_MUXED_BT	USB2_PHY	USB2	USB_BT_MUX_N	31

Et tu Brute?

Electrical Contraint Set	Physical	Spacing		
Ethernet				
J474 ?	?	?	ENETCONN_MDI_P<3..0>	34 35
J475 ?	?	?	ENETCONN_MDI_N<3..0>	34 35
J476	?	?	ENETCONN_MDI_T_P<3..0>	35
J477	?	?	ENETCONN_MDI_T_N<3..0>	35
J519		ENET_TRANS	ENETCONN_MCT0	35
J520		ENET_TRANS	ENETCONN_MCT1	35
J521		ENET_TRANS	ENETCONN_MCT2	35
J522		ENET_TRANS	ENETCONN_MCT3	35
J523		ENET_TRANS	ENETCONN_MCT_BS	35
J478	ENET_COMP_PHY	COMP_ENET	ENET_RDAC	34
SD				
J479 ?	?	?	ENET_CR_DATA<7..0>	34
J480	?	?	SDCONN_DATA<7..0>	34 36
J481 SD_CMD	SD_PHY	SD	ENET_SD_CMD	34
J482	SD_PHY	SD	SDCONN_CMD	34 36
J483 SD_CLK	SD_PHY	SD	ENET_SD_CLK	34
J484	SD_PHY	SD	SDCONN_CLK	34 36
J486	SD_PHY	SD	SDCONN_CLK_R	36
J485	SD_PHY	SD	ENET_MEDIA_SENSE	15 34
J488	SD_PHY	SD	ENET_SD_DETECT_L	34 36
CIV SPI				
J490	CIV_SPI	SPI	ENET_SCLK	34
J489	CIV_SPI	SPI	ENET_MISO	34
J492	CIV_SPI	SPI	ENET_MOSI	34
J493	CIV_SPI	SPI	ENET_CS_L	34

Camera Processor-Camera Sensor I/F

Electrical Contraint Set	Physical	Spacing		
J501 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	37
J502 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	37
J504 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	37
J503 SMIA_DP	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	37
J507	SPI_50S	SPI	CAM_SF_CLK	37
J508	SPI_50S	SPI	CAM_SF_CLK_R	37
J509	SPI_50S	SPI	CAM_SF_DIN	37
J510	SPI_50S	SPI	CAM_SF_DIN_R	37
J511	SPI_50S	SPI	CAM_SF_CS_L	37
J513	SPI_50S	SPI	CAM_SF_WP_L	37
J512	SPI_50S	SPI	CAM_SF_DOUT	37
J514	SPI_50S	SPI	CAM_SF_DOUT_R	37
J517	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	37
J518	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	37

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SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=1.5:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SMC Generic Control Line Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMC_ISO	*	=1:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMC_CTRL	*	*	SMC_ISO

SMC Generic Control Line Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMC_GEN	*	SMC_50S

Current/Voltage Sense

Electrical Contraint Set	Physical	Spacing		
Common				
T3		SENSE	GND_SMC_AVSS	43 44 47
12V S5 (System Total)				
T4 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_P	47
T5 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P12VG3H_N	47
T6		SENSE	ISNS_P12VG3H_R	47
T7		SENSE	ISNS_P12VG3H	44 47
T8		SENSE	VSNS_P12VG3H	44 47
SSD				
T85 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_P	47
T87 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_SSD_N	47
T86		?	ISNS_SSDS4_R	47
T88		?	ISNS_SSDS4	44 47
T89		SENSE	VSNS_P3V3_SSD	44 47
VDDQ S3 (DDR)				
T83 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V2_S3_DDR_P	47
T82 SNS_CURRENT	SNS_DIFF_PHY	SENSE	SNS_P1V2_S3_DDR_N	47
T85		SENSE	ISNS_P1V2_S3_DDR_R	47
T84		SENSE	ISNS_P1V2_S3_DDR	44 47
T86		SENSE	VSNS_P1V2_S3_DDR	44 47
CPU Core				
T42		SENSE	CPUVR_IMON	47 57
T45		SENSE	ISNS_CPUVCC	44 47
T46		SENSE	VSNS_CPUVCC	44 47

SMC

Electrical Contraint Set	Physical	Spacing		
SMC				
E1	CLK_XTAL	XTAL	SMC_XTAL	43 44
E2	CLK_XTAL	XTAL	SMC_EXTAL	43 44
E91	SMC_GEN	SMC_CTRL	SMC_LRESET_L	18 43
E90	SMC_GEN	SMC_CTRL	SMC_RUNTIME_SCI_L	13 43
E92	SMC_GEN	SMC_CTRL	SMC_WAKE_SCI_L	15 43
E93	SMC_GEN	SMC_CTRL	SMC_FAN_0_CTL	43 49
E94	SMC_GEN	SMC_CTRL	SMC_FAN_0_TACH	43 49

SMBus

Electrical Contraint Set	Physical	Spacing		
SMC				
E10	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	43 46
E9	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	43 46
E11	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	43 46
E12	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	43 46
E13	SMB_PHY	SMB	SMBUS_SMC_2_S0_SCL	43 46
E14	SMB_PHY	SMB	SMBUS_SMC_2_S0_SDA	43 46
E15	SMB_PHY	SMB	SMBUS_SMC_3_SCL	43 46
E16	SMB_PHY	SMB	SMBUS_SMC_3_SDA	43 46
E19	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	43 44
E20	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	43 44
PCH				
E21	TBT_I2C_5S8	TBT_I2C	SMBUS_PCH_CLK	14 46
E52	TBT_I2C_5S8	TBT_I2C	SMBUS_PCH_DATA	14 46
E53	SMB_PHY	SMB	SML_PCH_0_CLK	14 46
E54	SMB_PHY	SMB	SML_PCH_0_DATA	14 46

Temperature Sense

Electrical Contraint Set	Physical	Spacing		
EMC1414-1 (Production)				
E57 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_P	48
E58 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_1_N	48
E59 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_3_P	48
E60 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T1_3_N	48
E65 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_P	48 56
E66 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_ACDC_N	48 56
E122	SNS_DIFF_PHY	SENSE	SNS_T1_2_P	48
E124	SNS_DIFF_PHY	SENSE	SNS_T1_2_N	48
TMP423 (Development)				
E67 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_P	48
E68 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_1_N	48
E69 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_P	48
E70 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_2_N	48
E71 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_P	48
E72 SNS_TEMP	SNS_DIFF_PHY	SENSE	SNS_T2_3_N	48
HDD Out-of-Band				
E73		SENSE	HDD_OOB1_D2R_L	33
E74		SENSE	HDD_OOB1_D2R_F_L	33
E75		SENSE	HDD_OOB1_D2R_R_L	33
E115		SENSE	SMC_OOB1_D2R_L	33 43
E76		SENSE	SMC_OOB1_R2D_L	33 43
E116		SENSE	SMC_OOB1_R2D_R_L	33
SSD Out-of-Band				
E77		SENSE	SMC_OOB2_R2D_L	32 44
E78		SENSE	SMC_OOB2_D2R_L	32 44

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DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.150 MM	12.7 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_P5MM
GND	BGA	GND_P3MM
POWER	*	POWER_P6MM
POWER	BGA	POWER_P3MM
VR_CTL_PHY	*	POWER_P3MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_DIDT_PHY	*	POWER_P6MM
VR_DIDT_PHY	BGA	STANDARD

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?
GND_ISO	*	=STANDARD	?

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

VDDQ (1.2V)/VTT (0.6V) S3

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I43	POWER	POWER	5V			PP5V_REG_P1V2_V5IN	59 77
Local Ground							
I44	GND	GND	0V			AGND_P1V2_S3	59 77
VDDQ S3							
I45	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V2_S3	59
I47	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V2_S3_L	59
I46	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V2_S3	59
I48	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V2_S3_RC	59
I49	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V2_S3	59
I52	VR_DIDT_PHY	VR_SWITCH		TRUE		REG_LGATE_P1V2_S3	59
I51	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V2_S3	59
I63	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_VDDQSNS	59
I55	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_VREF	59
I56	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_REFIN	59
I57	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_MODE	59
I58	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_TRIP	59
I59	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS	59
I61	VR_CTL_PHY	VR_CTL				REG_P1V2_S3_VTTREF	59
Output Bus							
I60	POWER	POWER	1.2V			PP1V2_S3	66
I62	POWER_DDR	POWER_DDR	0.6V			PP0V6_S3_DDRVTT	66
Sensed							
I64	POWER	POWER	1.2V			PP1V2_S3_DDR	66

PCH 1.05V S0

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus								
I1		POWER	POWER	5V			REG_VCC_U7400	60
I2		POWER	POWER	5V			REG_PVCC_U7400	60
Local Ground								
I3		GND	GND	0V			AGND_P1V05S0	60
1.05V S0								
I5		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	60
I4		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	60
I7		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	60
I6		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0_RC	60
I8		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	60
I9		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	60
I10		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P1V05S0	60
I12		VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P1V05S0	60
I11		VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	60
I14		VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	60
I86	SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P1V05S0_PHASE_SNS_P	60
I85	SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P1V05S0_PHASE_SNS_M	60
I19			SENSE				REG_P1V05S0_FB	60
I18			SENSE				REG_P1V05S0_RTN	60
I21		VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	60
I20		VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	60
Output Bus								
I22		POWER	POWER	1.05V			PP1V05_S0	66

1.8V S3

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
I67	POWER	POWER	5V			PP5V_REG_P1V2_V5IN	59 77
Local Ground							
I68	GND	GND	0V			AGND_P1V2_S3	59 77
Switch							
I69	VR_DIDT_PHY	VR_SWITCH	3.3V	TRUE		REG_SW_P1V8_S3	59
I70	VR_DIDT_PHY	VR_SWITCH	3.3V	TRUE		REG_FB_P1V8_S3	59
Output Bus							
I83	POWER	POWER	1.8V			PP1V8_S3_REG_R	59
I84	POWER	POWER	1.8V			PP1V8_S3	66

1.05V S5

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
Switch							
Output Bus							
I92			1.05V			PP1V05_S5	16

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CPU VCC Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
H24	POWER	POWER	12V			PP12V_S0_REG_CPUVCC_VIN 57
H13	POWER	POWER	5V			PP5V_S0_REG_CPUVCC_VDD 57
Phase 1						
H84	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_1 57 58
H87	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_1 58
H88	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1 58
H90	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_1_RC 58
H27	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_1 58
H24	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_1 58
H92	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_1 58
H93	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_1 58
H91	VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_CPUVCC_ISNS1_M 58
H95	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_CPUVCC_ISNS1_P 58
H96			SENSE			REG_CPUVCC_ISEN1 57 58
H27			SENSE			REG_CPUVCC_ISUMN 57 58
H27			SENSE			REG_CPUVCC_ISUMP 57 58
Phase 2						
H14	VR_CTL_PHY	VR_CTL				REG_PWM_CPUVCC_2 57 58
H14	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUVCC_2 58
H14	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2 58
H14	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUVCC_2_RC 58
H27	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUVCC_2 58
H27	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_CPUVCC_2 58
H14	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_CPUVCC_2 58
H14	POWER	POWER	1.8V			PPCPUVCC_S0_SENSE_2 58
H14	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_CPUVCC_ISNS2_M 58
H15	ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE			REG_CPUVCC_ISNS2_P 58
H15			SENSE			REG_CPUVCC_ISEN2 57 58

CPU VCC Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
ISL95826HRZ						
H102	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FCCM 57 58
H107	VR_CTL_PHY	VR_CTL				REG_CPUVCC_DRSEL 57
H107	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP 57
H107	VR_CTL_PHY	VR_CTL				REG_CPUVCC_COMP_RC 57
H107	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB 57
H107	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB_RC 57
H107	VR_CTL_PHY	VR_CTL				REG_CPUVCC_FB2 57
H103	VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE			CPU_VCCSENSE_P 8 57
H104	VSNS_CPU_CORE	SNS_DIFF_PHY	SENSE			CPU_VCCSENSE_N 9 57
H107			SENSE			CPU_VCCSENSE_P_R 57
H107			SENSE			CPU_VCCSENSE_P_RC 57
H107			SENSE			REG_CPUVCC_ISUMN_RC 57
H107			SENSE			REG_CPUVCC_ISUMN_R 57
H103			SENSE			REG_CPUVCC_RTN 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NTC 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_NTC_R 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_SLOPE 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PROG1 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PROG2 57
H105	VR_CTL_PHY	VR_CTL				REG_CPUVCC_PROG3 57
H106	VR_VID_PHY	VR_VID				CPU_VIDSCLK 8 57
H106	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R 8
H106	VR_VID_PHY	VR_VID				CPU_VIDALERT_L 8 57
H106	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L 8
H106	VR_VID_PHY	VR_VID				CPU_VIDSOUT 8 57
H106	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R 8
Output Bus						
H104	POWER	POWER	1.8V			PPCPUVCC_S0_CPU 44

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12V

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
I1449	POWER	POWER	12V			PP12V_ACDC 66
FET Switched						
I1448	POWER	POWER	12V			PP12V_S5 66
I1451	POWER	POWER	12V			PP12V_S0 66
Sensed						
I1453	POWER	POWER	12V			PP12V_G3H 66

3.42V G3H

	Physical	Spacing	Voltage	DIDT	NO_TEST	
3.42V G3H						
I1443	POWER	POWER	12V	TRUE		P3V42G3H_BOOST 56
I1442	POWER	POWER	12V	TRUE		P3V42G3H_SW 56
I1444	VR_CTL_PHY	VR_CTL				P3V42G3H_FB 56
I1445	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L 56
I1485	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_R_L 56
Output Bus						
I1446	POWER	POWER	3.425V			PP3V42_G3H 66
I1484	POWER	POWER	3.425V			PP3V42_G3H_REG_R 56

3.3V G3

	Physical	Spacing	Voltage	DIDT	NO_TEST	
I1476	POWER	POWER	3.3V			PP3V3_G3 66

3.3V S5/5V S4

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Input Bus						
I843	POWER	POWER	12V			REG_VIN_U7600 61
I1254	POWER	POWER	5V			REG_VCC1_U7600 61
I1255	POWER	POWER	5V			REG_VCC2_U7600 61
3.3V S5						
I849	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5 61
I847	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5 61
I851	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5_RC 61
I848	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5 61
I850	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P3V3S5 61
I852	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5 61
I1071	VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN 61
I1072	VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET 61
I1139	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET 61
I1087	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT 61
I1075	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R 61
I1073	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB 61
5V S4						
I1132	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4 61
I1130	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4 61
I1133	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4_RC 61
I1140	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4 61
I1141	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_LGATE_P5VS4 61
I1142	VR_DIDT_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4 61
I1143	VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN 61
I1144	VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET 61
I1145	VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET 61
I1146	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT 61
I1148	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R 61
I1147	VR_CTL_PHY	VR_CTL				REG_P5VS4_FB 61
Output Bus						
I1153	POWER	POWER	5V			PP5V_S5 66
I1155	POWER	POWER	5V			PP5V_S4 66
I1149	POWER	POWER	3.3V			PP3V3_S5 66
FET Switched						
I1220	POWER	POWER	5V			PP5V_S0 66
I1219	POWER	POWER	3.3V			PP3V3_S4 66
I1223	POWER	POWER	3.3V			PP3V3_S0 66
I1455	?	?	3.3V			PP3V3_S4_SSD 66
I1218	POWER	POWER	3.3V			PP3V3_ENET 66
I1138	POWER	POWER	3.3V			PP3V3_TBTLC 18 26 27
Sensed						
I1454	?	?	3.3V			PPSSD_S4 66

HDD S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
FET Switched						
I1160	POWER	POWER	5V			PP5V_S0_HDD 66

1V5 S0

	Physical	Spacing	Voltage	DIDT	NO_TEST	
OUTPUT BUS						
I1477	POWER	POWER	1.5V			PP1V5_S0 66

Ground/Common

	Physical	Spacing	Voltage	DIDT	NO_TEST	
Common						
	GND	GND				GND\G
I1486	GND	GND	0V			PGND_REG_P1V2_S3 59

	Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST	
I1509	SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P3V3S5_PHASE_SNS_P 61
I1510	SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P3V3S5_PHASE_SNS_M 61
I1505	SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P5VS4_PHASE_SNS_P 61
I1506	SNS_CURRENT	SNS_DIFF_PHY	SENSE				REG_P5VS4_PHASE_SNS_M 61

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Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C_ISO	*	=2x_DIELECTRIC	?
TBT_SPI_ISO	*	=2x_DIELECTRIC	?
TBTDP_ISO	*	=5x_DIELECTRIC	?
TBTDP_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP	*	*	TBTDP_ISO
TBT_SPI	*	*	TBT_SPI_ISO
TBT_I2C	*	*	TBT_I2C_ISO

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_ISO

Pairs should be within 100 mils of clock length.
Max length of DisplayPort traces: 12 inches

DisplayPort intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DisplayPort AUX channel intra-pair matching should be 5 ps. No relationship to other signals.

TBT IC Net Properties

	Electrical Contraint Set	Physical	Spacing		
1511		?	?	DP_TBTSNK0_ML_C_P<3..0>	5 26
1512		?	?	DP_TBTSNK0_ML_C_N<3..0>	5 26
1513	?	?	?	DP_TBTSNK0_ML_P<3..0>	26
1514	?	?	?	DP_TBTSNK0_ML_N<3..0>	26
1515		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P	13 26
1516		DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N	13 26
1517	DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P	26
1518	DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N	26
1519		?	?	DP_TBTSNK1_ML_C_P<3..0>	5 26
1521		?	?	DP_TBTSNK1_ML_C_N<3..0>	5 26
1520	?	?	?	DP_TBTSNK1_ML_P<3..0>	26
1523	?	?	?	DP_TBTSNK1_ML_N<3..0>	26
1522		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P	13 26
1524		DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N	13 26
1526	DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P	26
1525	DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N	26
1603	?	?	?	DP_TBTSRC_ML_P<1..0>	26 40
1604	?	?	?	DP_TBTSRC_ML_N<1..0>	26 40
1606	?	?	?	DP_TBTSRC_ML_C_P<1..0>	
1607	?	?	?	DP_TBTSRC_ML_C_N<1..0>	
1529	DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_P	26 40
1530	DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_N	26 40
1601		?	?	DP_TBTSRC_AUX_C_P	
1602		?	?	DP_TBTSRC_AUX_C_N	
1531	TBT_SPI_CLK	TBT_SPI_55S	TBT_SPI	TBT_SPI_CLK	26
1534	TBT_SPI_MOSI	TBT_SPI_55S	TBT_SPI	TBT_SPI_MOSI	26
1532	TBT_SPI_MISO	TBT_SPI_55S	TBT_SPI	TBT_SPI_MISO	26
1535	TBT_SPI_CS_L	TBT_SPI_55S	TBT_SPI	TBT_SPI_CS_L	26

*: Only used on hosts supporting T29 video-in

DisplayPort

	Electrical Contraint Set	Physical	Spacing		
	Graphics Source				
1643	?	?	?	DP_INT_ML_P<1..0>	5 40
1644	?	?	?	DP_INT_ML_N<1..0>	5 40
1645	DP_INTPNL_IG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_AUX_P	5 40
1646	DP_INTPNL_IG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_AUX_N	5 40
1648		?	?	DP_INT_AUX_C_P	
1647		?	?	DP_INT_AUX_C_N	
	Internal Panel				
1605		?	?	DP_INTPNL_ML_C_P<1..0>	40
1606		?	?	DP_INTPNL_ML_C_N<1..0>	40
1607	?	?	?	DP_INTPNL_ML_P<1..0>	39 40
1608	?	?	?	DP_INTPNL_ML_N<1..0>	39 40
1609	DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P	39 40
1610	DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N	39 40
	Internal DP SPDIF				
1611			HDA	DP_INT_SPDIF_AUDIO	39 51 74
	DDC				
1692		TBT_I2C_55S	TBT_I2C	DP_TBTSNK0_DDC_CLK	13 30
1693		TBT_I2C_55S	TBT_I2C	DP_TBTSNK0_DDC_DATA	13 30
1694		TBT_I2C_55S	TBT_I2C	DP_TBTSNK1_DDC_CLK	13 30
1695		TBT_I2C_55S	TBT_I2C	DP_TBTSNK1_DDC_DATA	13 30
1698		TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_CLK	28 30
1699		TBT_I2C_55S	TBT_I2C	DP_TBTPA_DDC_DATA	28 30
1697		TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_CLK	29 30
1696		TBT_I2C_55S	TBT_I2C	DP_TBTPB_DDC_DATA	29 30

TBT/DP Net Properties

	Electrical Contraint Set	Physical	Spacing		
	Port A				
1541	TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	26 28
1542	TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	26 28
1544		TBTDP_90D	TBTDP	TBT_A_R2D_P<1>	28
1543		TBTDP_90D	TBTDP	TBT_A_R2D_N<1>	28
1700	TBT_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	26 28
1701	TBT_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	26 28
1702		TBTDP_90D	TBTDP	TBT_A_R2D_P<0>	28
1703		TBTDP_90D	TBTDP	TBT_A_R2D_N<0>	28
1535	DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	26 28
1536	DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	26 28
1545		DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	28
1547		DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	28
1680	DP_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	26 28
1681	DP_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	26 28
1678		DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	28
1679		DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	28
1546	DP_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	28
1548	DP_LSX	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	28
1554	TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	26 28
1553	TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	26 28
1551		TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1>	28
1552		TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1>	28
1675	TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	26 28
1674	TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	26 28
1549		TBTDP_90D	TBTDP	TBT_A_D2R_C_P<0>	28
1550		TBTDP_90D	TBTDP	TBT_A_D2R_C_N<0>	28
1650	TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	28
1651	TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	28
1599	TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P	26 28
1600	TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N	26 28
1555		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P	28
1556		DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N	28
	Port B				
1652	TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1>	26 29
1653	TBT_R2D_RVSD	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1>	26 29
1655		TBTDP_90D	TBTDP	TBT_B_R2D_P<1>	29
1654		TBTDP_90D	TBTDP	TBT_B_R2D_N<1>	29
1704	TBT_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<0>	26 29
1705	TBT_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<0>	26 29
1707		TBTDP_90D	TBTDP	TBT_B_R2D_P<0>	29
1706		TBTDP_90D	TBTDP	TBT_B_R2D_N<0>	29
1657	DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	26 29
1658	DP_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	26 29
1661		DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	29
1663		DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	29
1662	DP_ML3_RVSD	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	26 29
1664	DP_ML3_RVSD	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	26 29
1656		DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	29
1660		DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	29
1659	DP_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	29
1662	DP_LSX	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	29
1665	TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	26 29
1666	TBT_D2R1_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	26 29
1708		TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1>	29
1709		TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1>	29
1676	TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	26 29
1677	TBT_D2R0_RVSD	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	26 29
1681		TBTDP_90D	TBTDP	TBT_B_D2R_C_P<0>	29
1682		TBTDP_90D	TBTDP	TBT_B_D2R_C_N<0>	29
1671	TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	29
1672	TBT_AUXDDC	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	29
1668	TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P	26 29
1667	TBT_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N	26 29
1669		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P	29
1670		DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N	29

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Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions

BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	0.45mm	1000

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

Constraints

BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_CTL	*	BLC_CTL_ISO
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

Is it chel'oh or sel'oh?

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
P727	POWER	POWER	12V			PP12V_BKLT_SNS	62
P749	POWER	POWER	12V			PP12V_BKLT_FUSED	62
P750	POWER	POWER	12V			PP12V_S0_BKLT_FILT	62
P772	POWER	POWER	12V			PP12V_S0_BKLT_PWR	62
P794	POWER	POWER	12V			PP12V_S0_BKLT_PWR_R	62
P795	POWER	POWER	5V			PP5V_S0_BKLT_R	62
P796	POWER	POWER	3.3V			PP3V3_S0_BKLT_VDDIO_R	62
Local Ground							
P751	BLC_CTL_PHY	BLC_PHASE	0V			PGND_BKLT	62
P798	BLC_CTL_PHY	BLC_PHASE	0V			DGND_BKLT	62
P805	BLC_CTL_PHY	BLC_PHASE	0V			LGND_BKLT	62
Backlight							
P752	POWER_BLC	BLC_PHASE	80V	TRUE		BKLT_PHASE	62
P753	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE	62
P754	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_GATE_R	62
P755	BLC_CTL_PHY	BLC_PHASE	80V	TRUE		BKLT_SNUBBER	62
P757	BLC_CTL_PHY	BLC_PHASE	12V	TRUE		BKLT_SW_R	62
P759	BLC_CTL_PHY	BLC_CTL				BKLT_ISET	62
P763	BLC_CTL_PHY	BLC_CTL				BKLT_FLT	62
P765	BLC_CTL_PHY	BLC_CTL				BKLT_FLT_RC	62
P797	SNS_DIFF_PHY	SENSE				BKLT_SW_P	62
P758	SNS_DIFF_PHY	SENSE				BKLT_SW_M	62
P762		SENSE				BKLT_FB	62
P801		BLC_HV	67V			BKLT_FB_XW	62
P764		BLC_HV	67V			BKLT_FB_R	62
P776	POWER_BLC_RET	BLC_CTL				BKLT_ISEN1	62
P775	POWER_BLC_RET	BLC_CTL				BKLT_ISEN2	62
P778	POWER_BLC_RET	BLC_CTL				BKLT_ISEN3	62
P777	POWER_BLC_RET	BLC_CTL				BKLT_ISEN4	62
P780	POWER_BLC_RET	BLC_CTL				BKLT_ISEN5	62
P779	POWER_BLC_RET	BLC_CTL				BKLT_ISEN6	62
P787	POWER_BLC_RET	BLC_HV				BKLT_ISEN1_R	62
P788	POWER_BLC_RET	BLC_HV				BKLT_ISEN2_R	62
P790	POWER_BLC_RET	BLC_HV				BKLT_ISEN3_R	62
P791	POWER_BLC_RET	BLC_HV				BKLT_ISEN4_R	62
P792	POWER_BLC_RET	BLC_HV				BKLT_ISEN5_R	62
P793	POWER_BLC_RET	BLC_HV				BKLT_ISEN6_R	62
P781	POWER_BLC_RET	BLC_HV				LED_RETURN_1	62
P782	POWER_BLC_RET	BLC_HV				LED_RETURN_2	62
P784	POWER_BLC_RET	BLC_HV				LED_RETURN_3	62
P785	POWER_BLC_RET	BLC_HV				LED_RETURN_4	62
P786	POWER_BLC_RET	BLC_HV				LED_RETURN_5	62
P787	POWER_BLC_RET	BLC_HV				LED_RETURN_6	62
Output Bus							
P770	POWER_BLC	BLC_HV	67V			BKLT_BOOST	62
P773	POWER_BLC	BLC_HV	67V			BKLT_BOOST_1	62
P774	POWER_BLC	BLC_HV	67V			BKLT_BOOST_2	62

Cello Miscellaneous

Electrical Contraint Set	Physical	Spacing		
SPI				
P544	SMB_PHY	SMB	BKLT_SCL	62
P543	SMB_PHY	SMB	BKLT_SDA	62

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