Foxconn Precision Co. Inc.
G31M05 Schematic

Fab.A
Data: 2008/1/03

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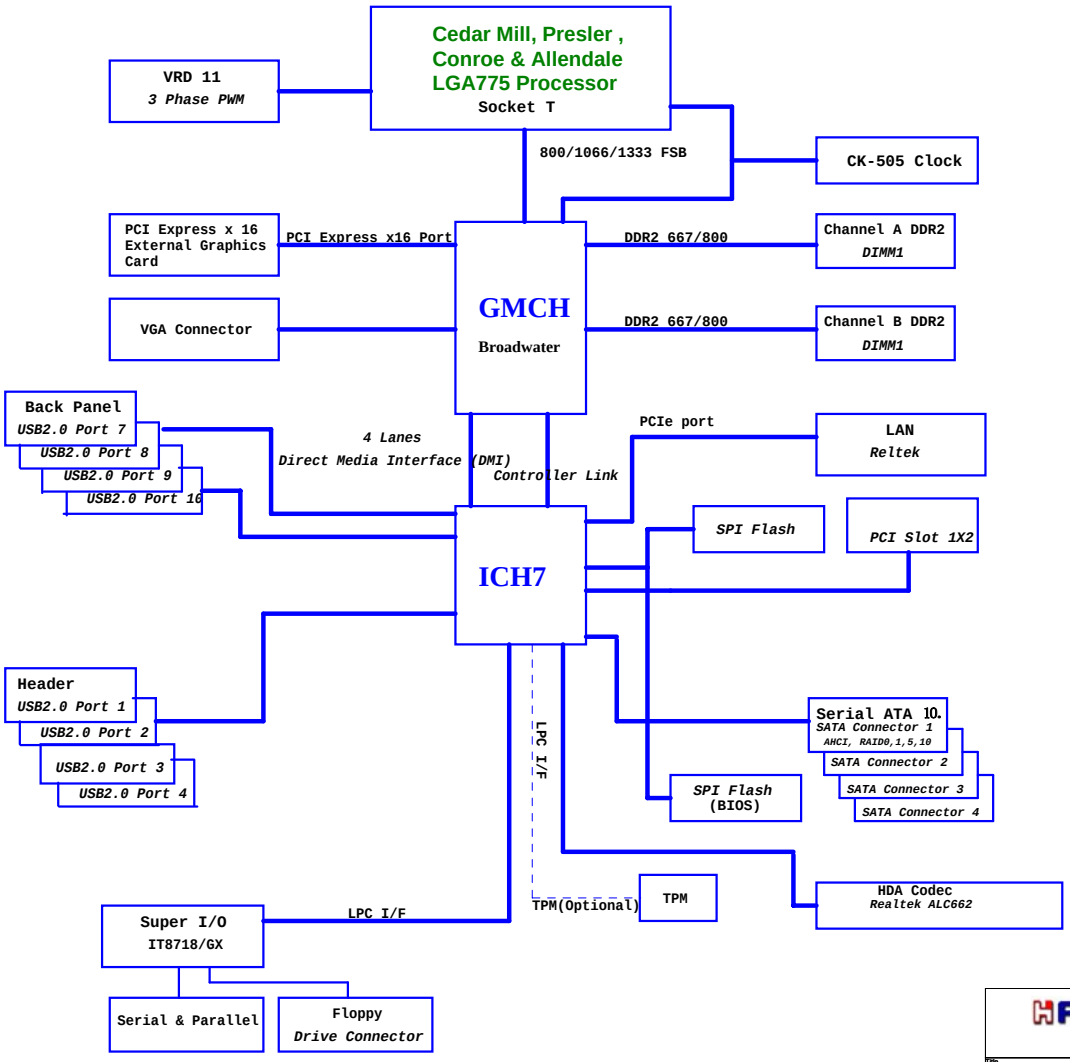

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Title: TOPOLOGY

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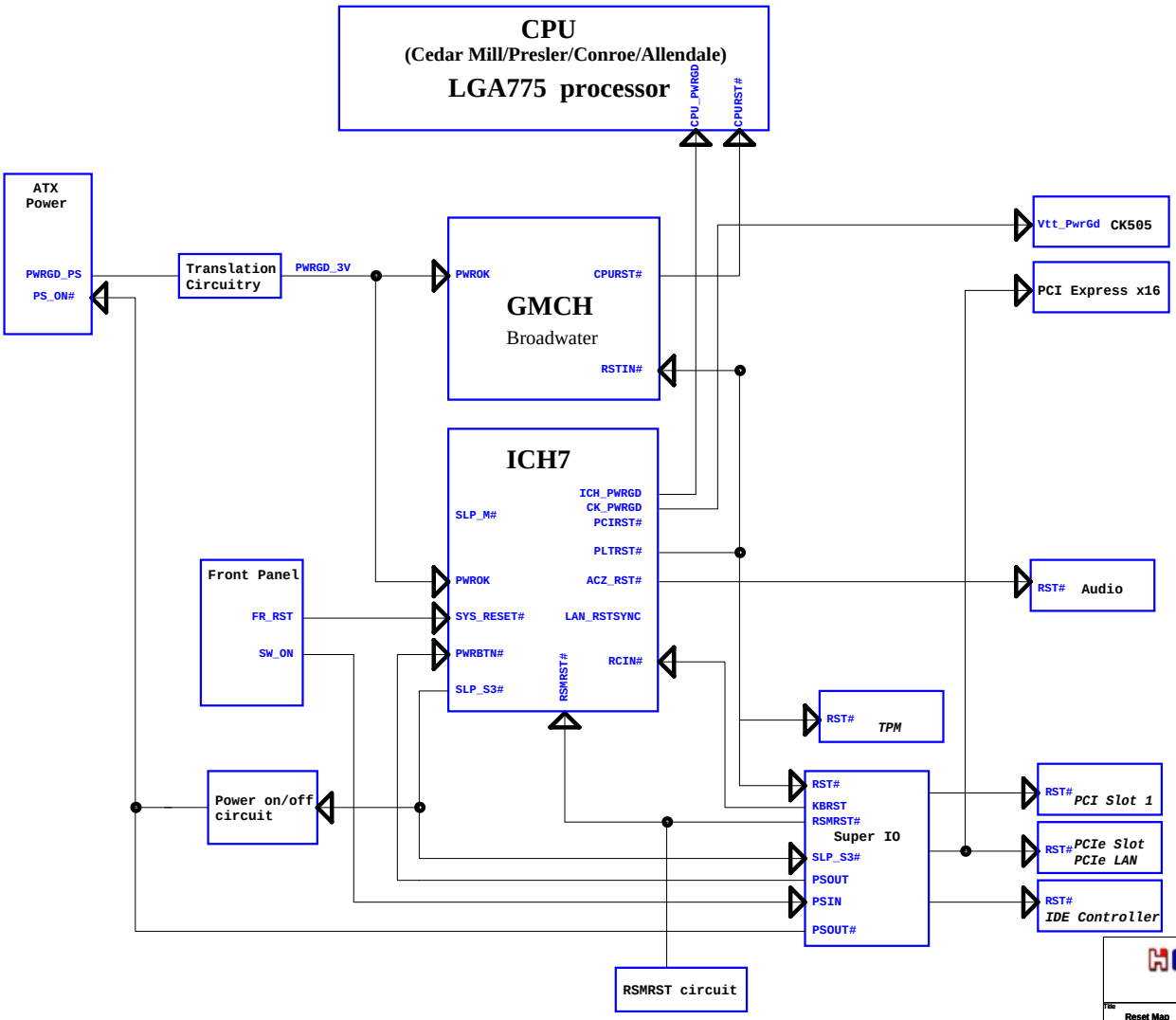
CPU
(Cedar Mill/Presler/Conroe/Allendale)
LGA775 processor
CPU_PWRGD
CPURST#
ATX
Power
PWRGD_PS
PS_ON#
Translation
Circuitry
PWRGD_3V
PWROK
CPURST#
GMCH
Broadwater
RSTIN#
Vtt_PwrGd
CK505
PCI Express x16
ICH7
ICH_PWRGD
CK_PWRGD
SLP_M#
PCIRST#
PLTRST#
Front Panel
PWROK
ACZ_RST#
RST#
Audio
FR_RST
SYS_RESET#
LAN_RSTSYNC
SW_ON
PWRBTN#
RCIN#
SLP_S3#
RSMRST#
RST#
TPM
Power on/off
circuit
RST#
KBRST
RSMRST#
Super IO
SLP_S3#
PSOUT
PSIN
PSOUT#
RST#
PCI Slot 1
RST#
PCIe Slot
PCIe LAN
RST#
IDE Controller
RSMRST circuit
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Reset Map
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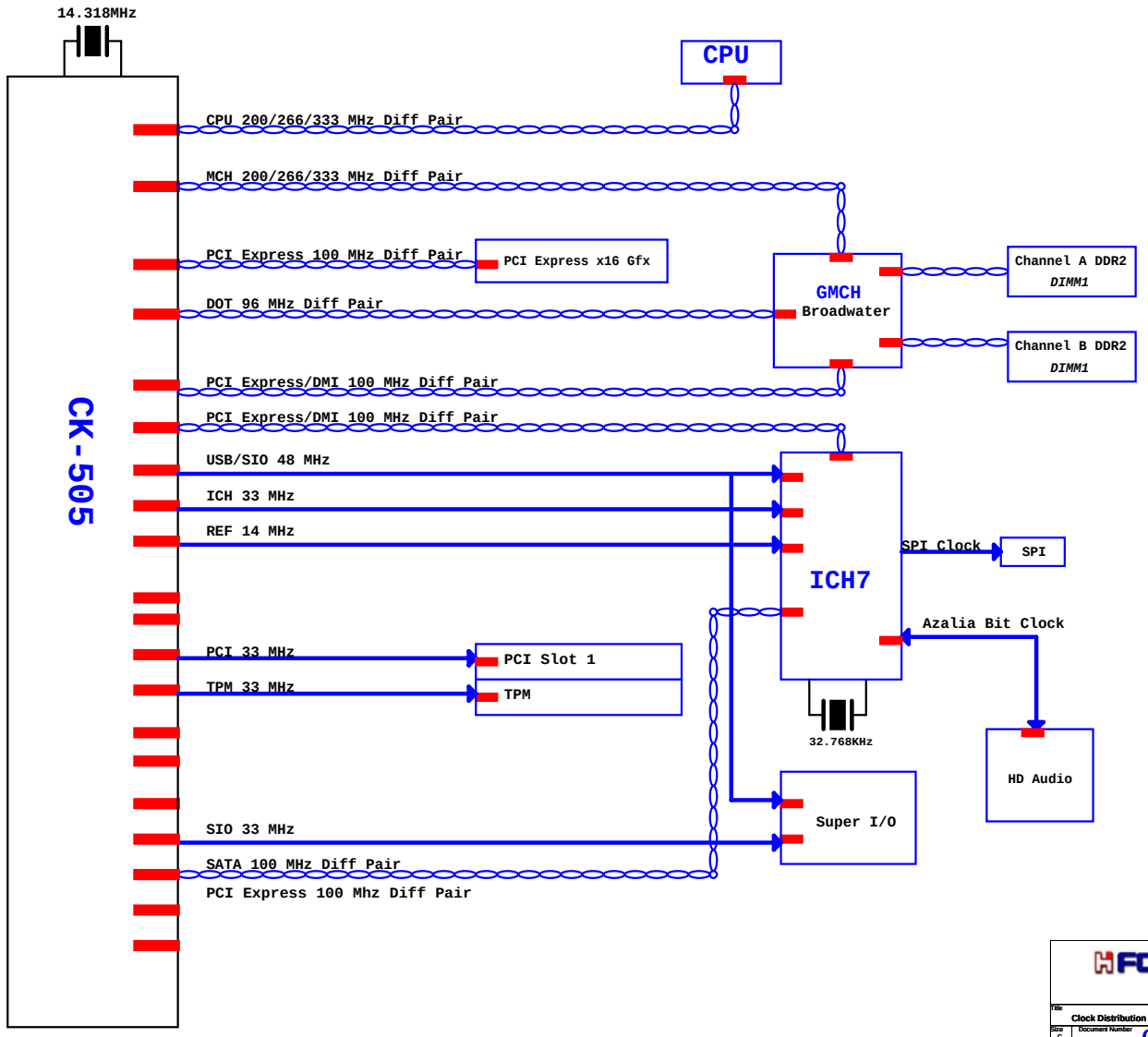

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Title: Clock Distribution

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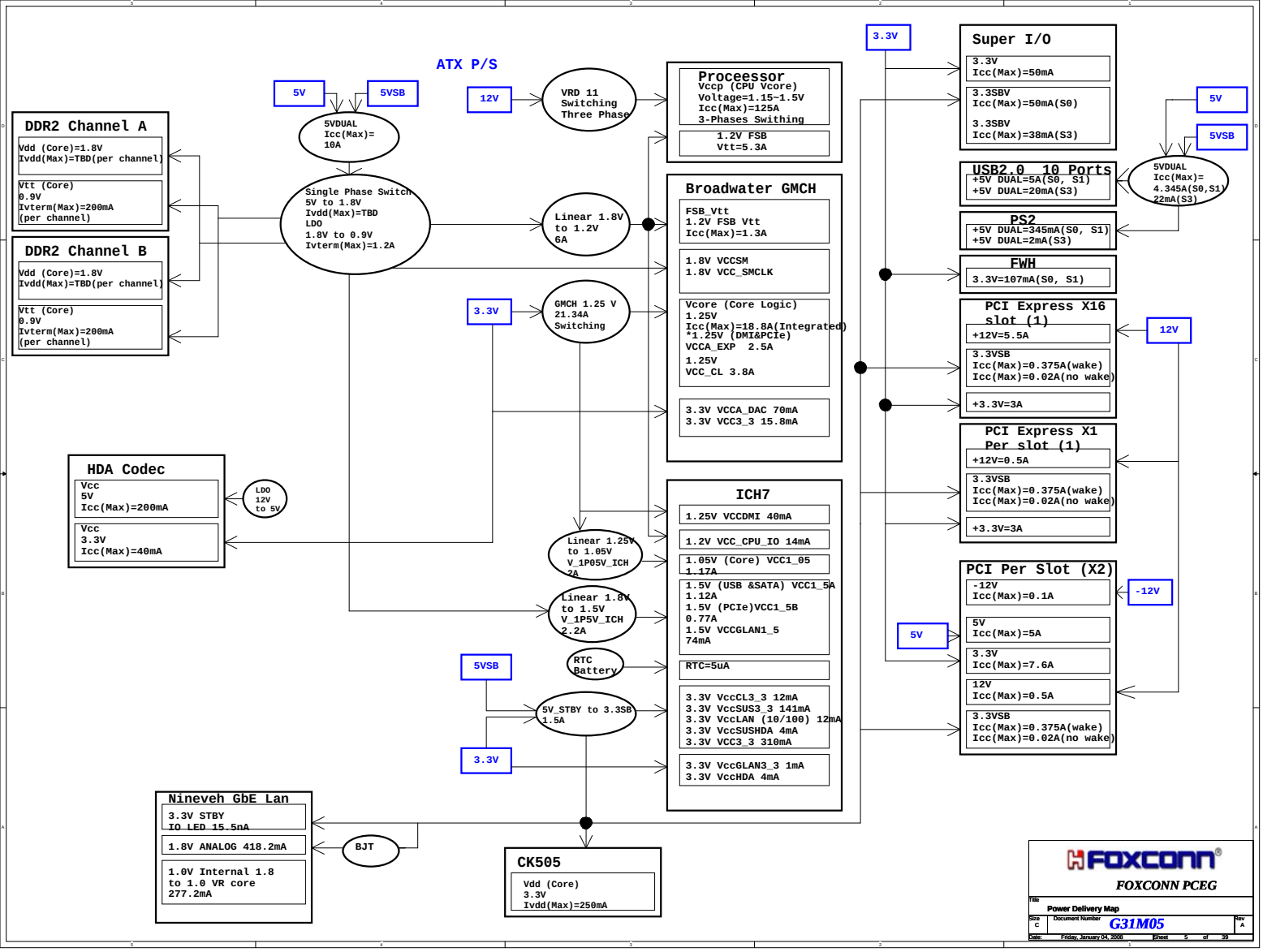

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Title: Power Delivery Map

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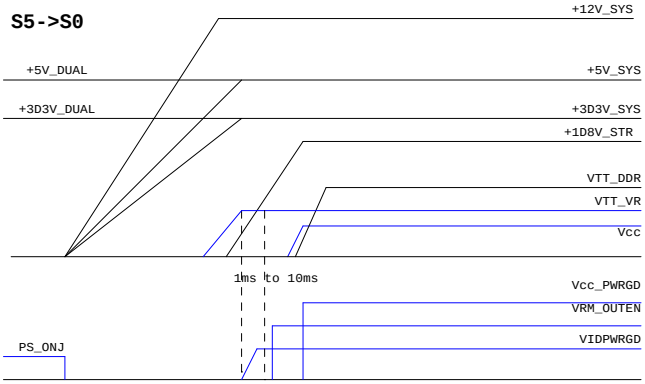
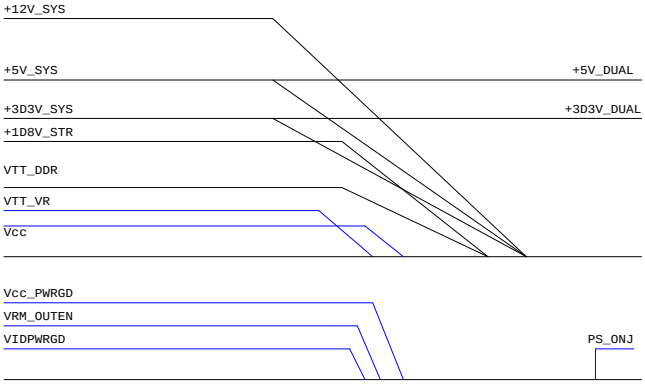
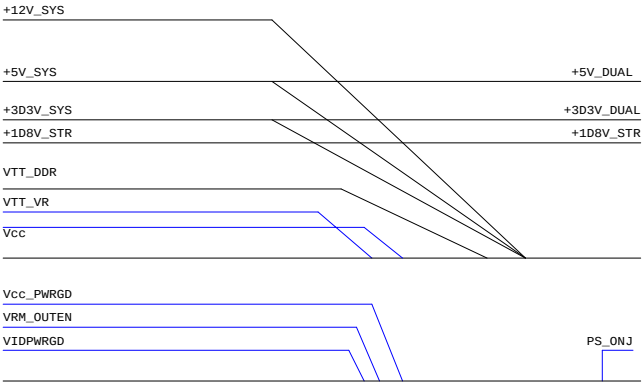
S5->S0



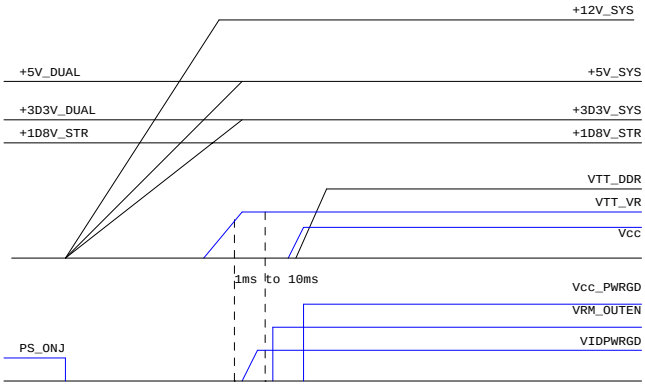
S0->S5



S0->S3



S3->S0



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Title: Power Sequence		
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Title: BLANK

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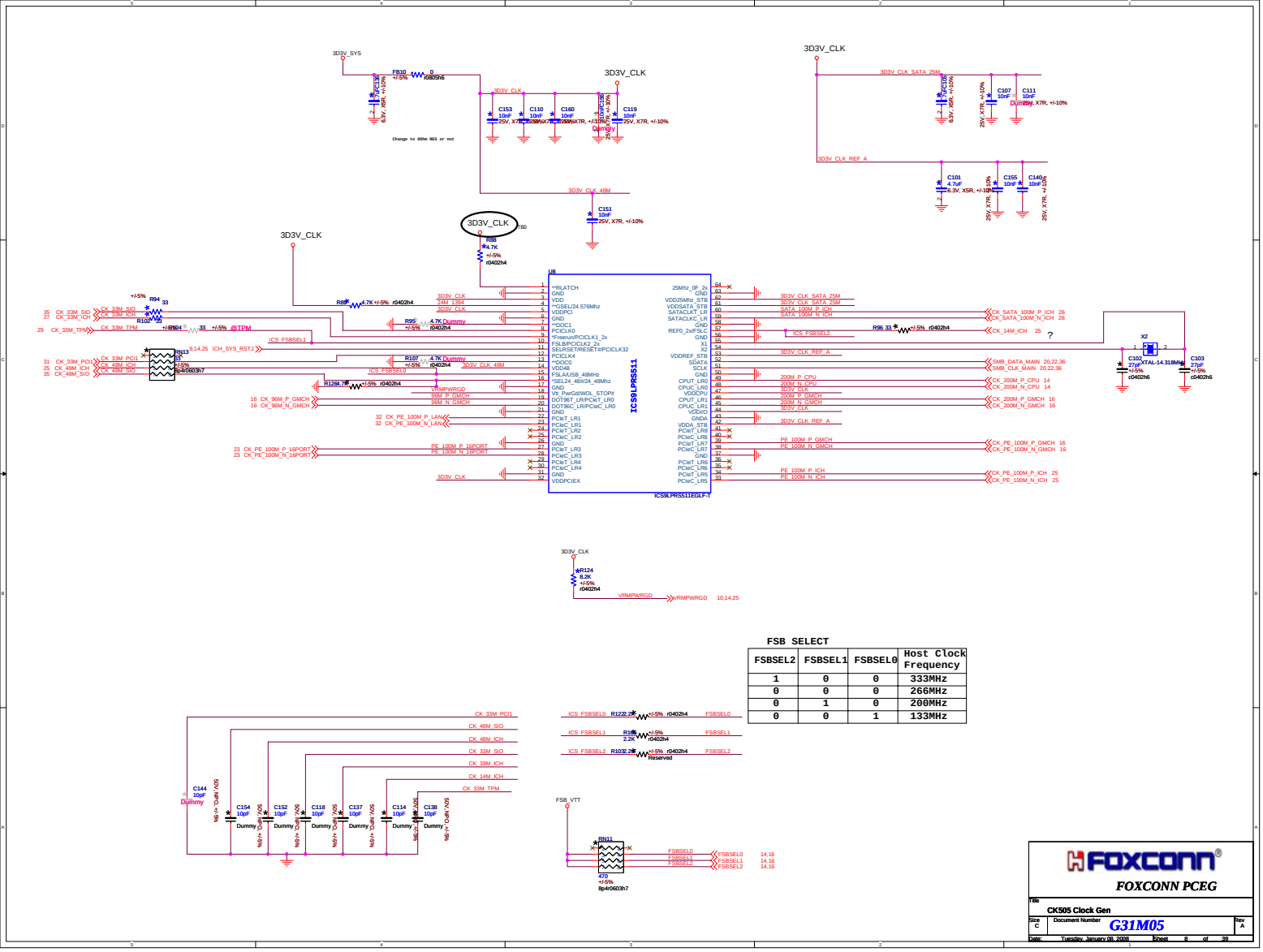
3D3V_SYS
3D3V_CLK
3D3V_CLK_SATA_25M
3D3V_CLK_REF_A
3D3V_CLK_48M
ICS9LPRS511
ICS9LPRS511EGLF-T
FSB SELECT
FSBSEL2 FSBSEL1 FSBSEL0 Host Clock Frequency
1 0 0 333MHz
0 0 0 266MHz
0 1 0 200MHz
0 0 1 133MHz
FSB_VTT
FOXCONN PCEG
CK505 Clock Gen
G31M05
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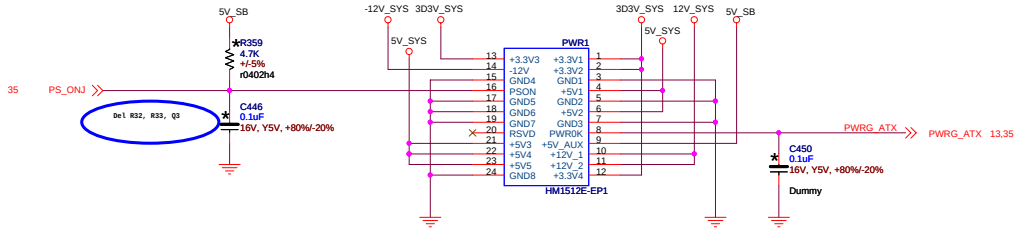
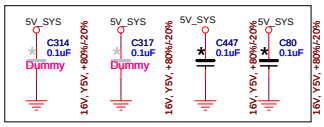
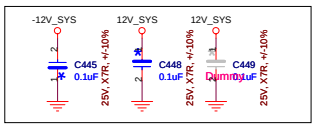
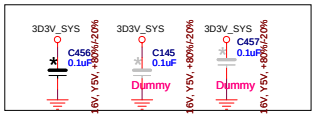
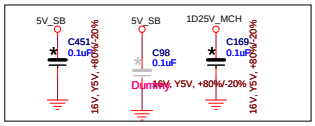
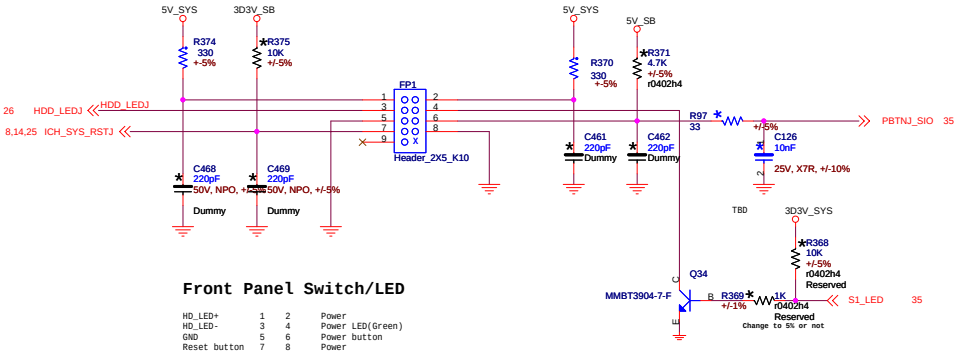








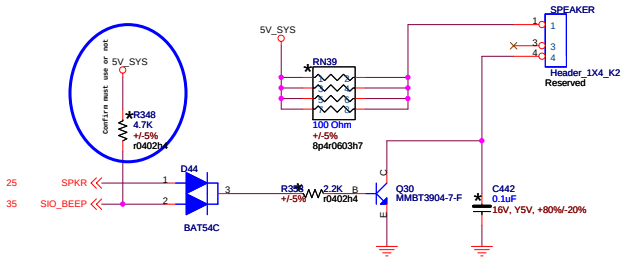




Front Panel Switch/LED

HD_LED+	1	2	Power
HD_LED-	3	4	Power LED(Green)
GND	5	6	Power button
Reset button	7	8	Power
NC	9	10	Key

SPEAKER HEADER



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Title	Power/MISC Connectors		
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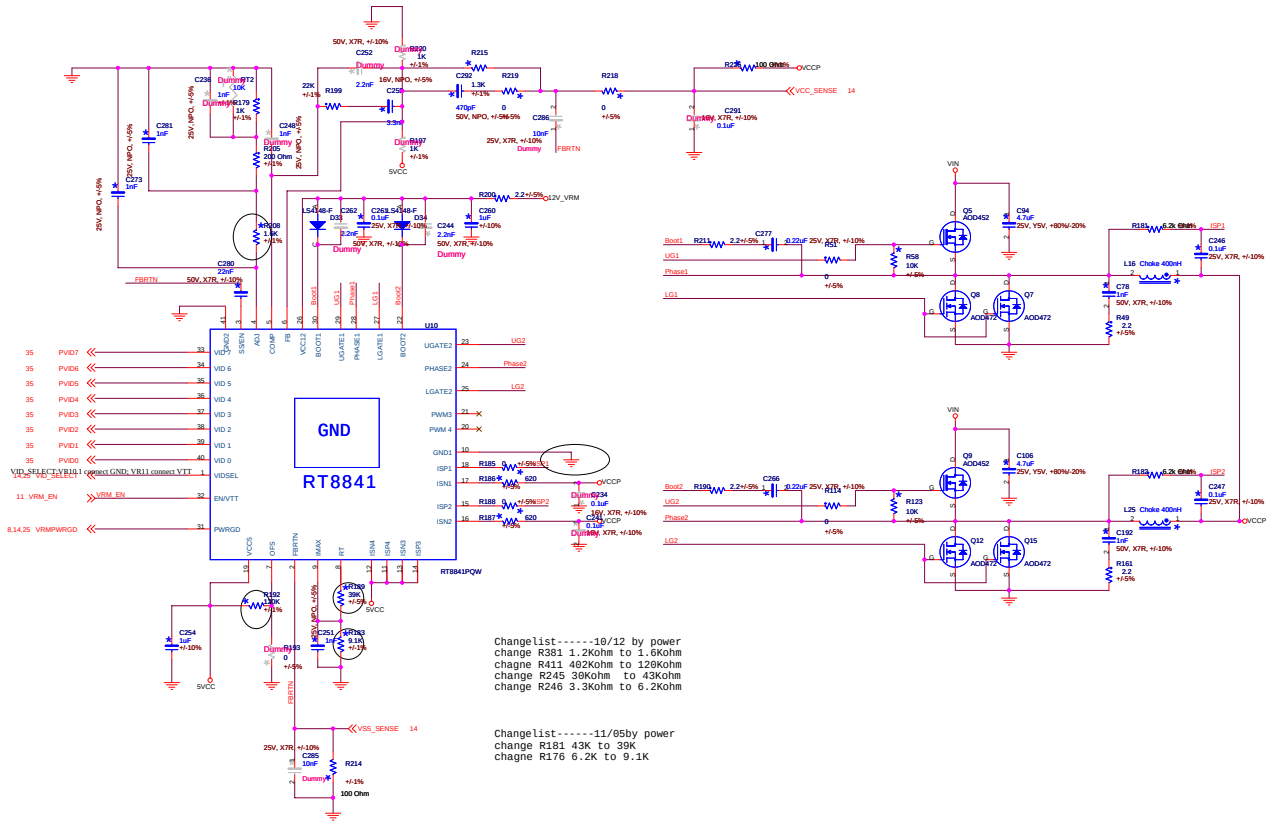

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Title: Voltage Regulator Down 11

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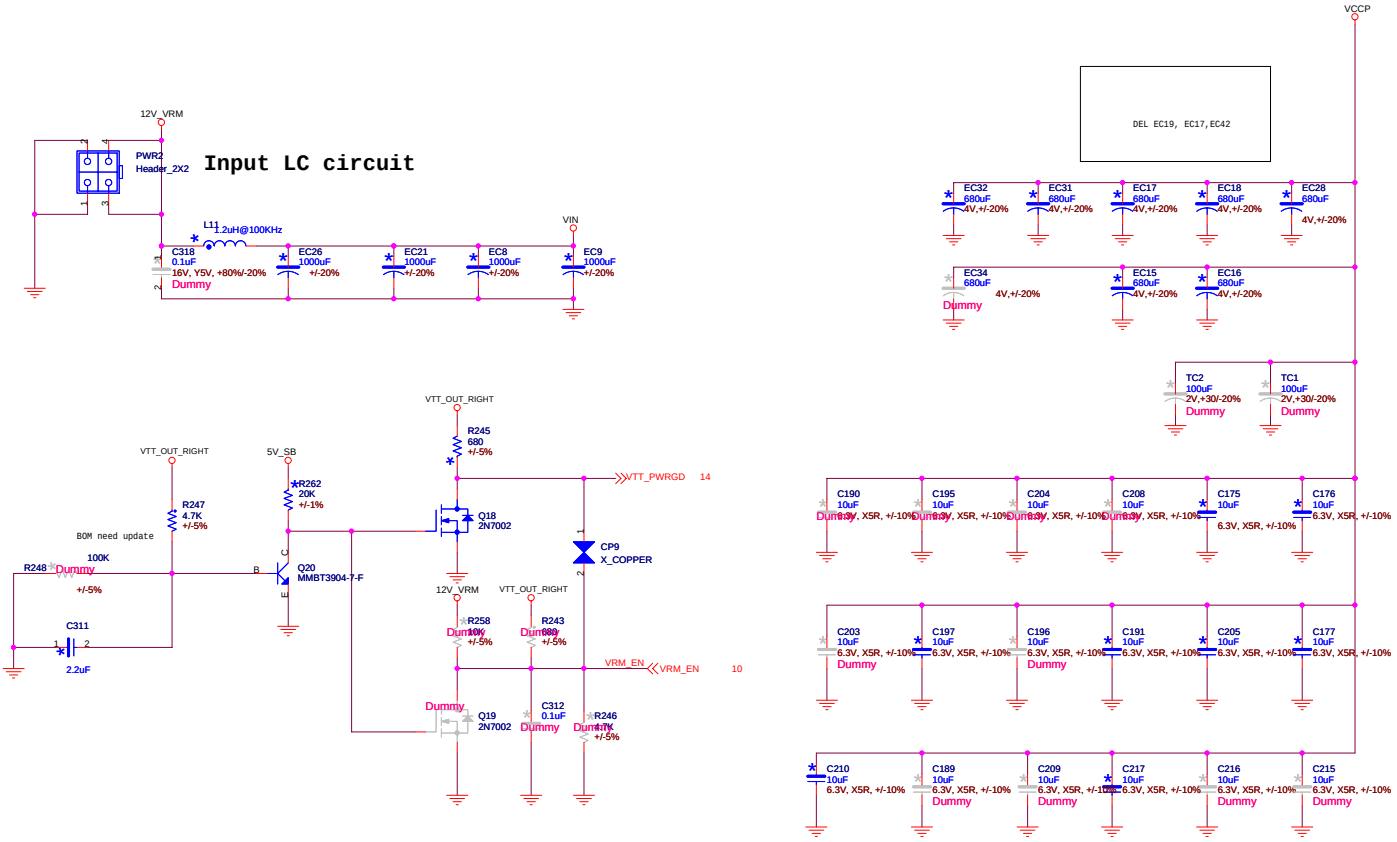

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Title: OUTPUT CAP

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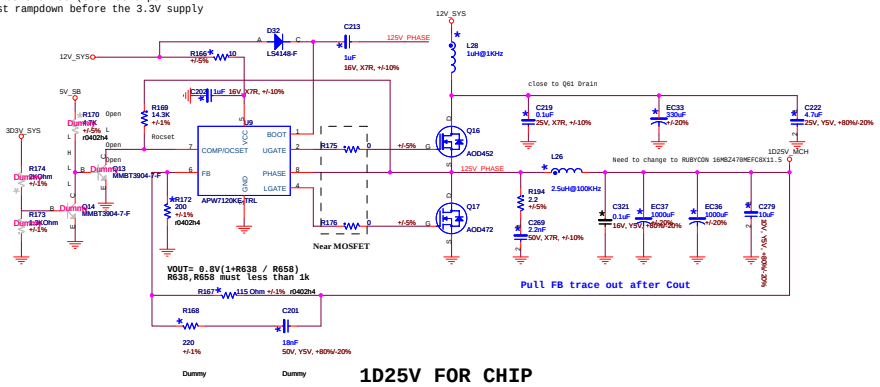
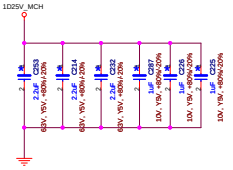
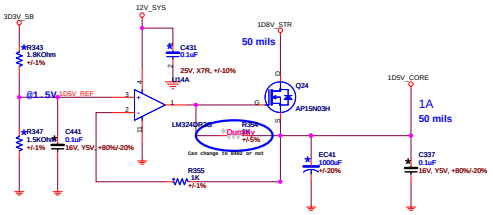
Intel design guide (333):
3.3V SUPPLY must ramp up before VCC (GMCH Core power
VCC (GMCH Core power) must rampdown before the 3.3V supply

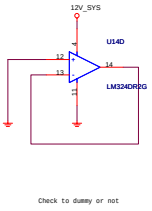


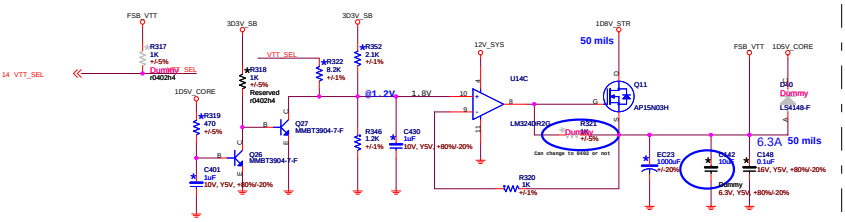
1D25V FOR CHIP



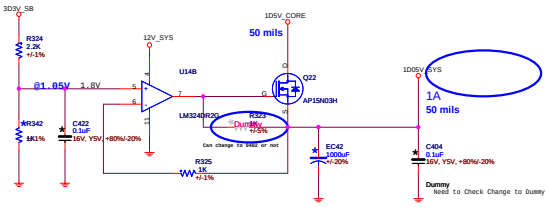


1D5V_SYS





FSB_VTT



1D05V_SYS

FOXCONN

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Title	1D25V 1D5V FSB	
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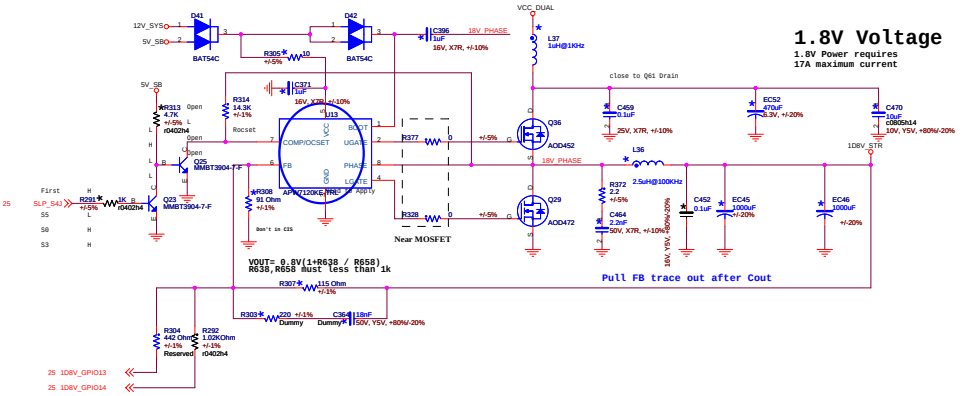
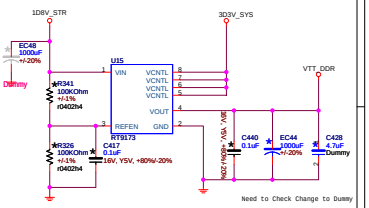
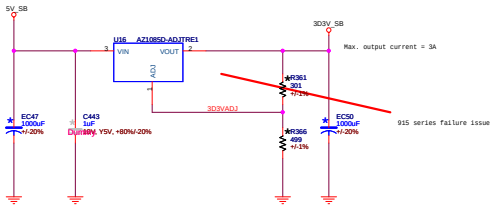


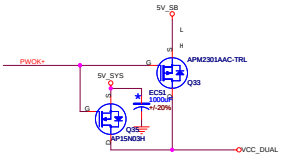
1D8V_STR

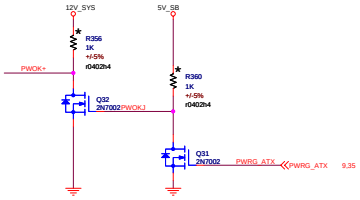




Vout=Vref(1+R2/R1)+IadjR2
R1 is Up Resistor.
Iadj=50uA
Vref=1.25V

3D3V_DUAL





5V_DUAL

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Title	STR 1D8V 3D3V_DUAL 5V_DUAL	
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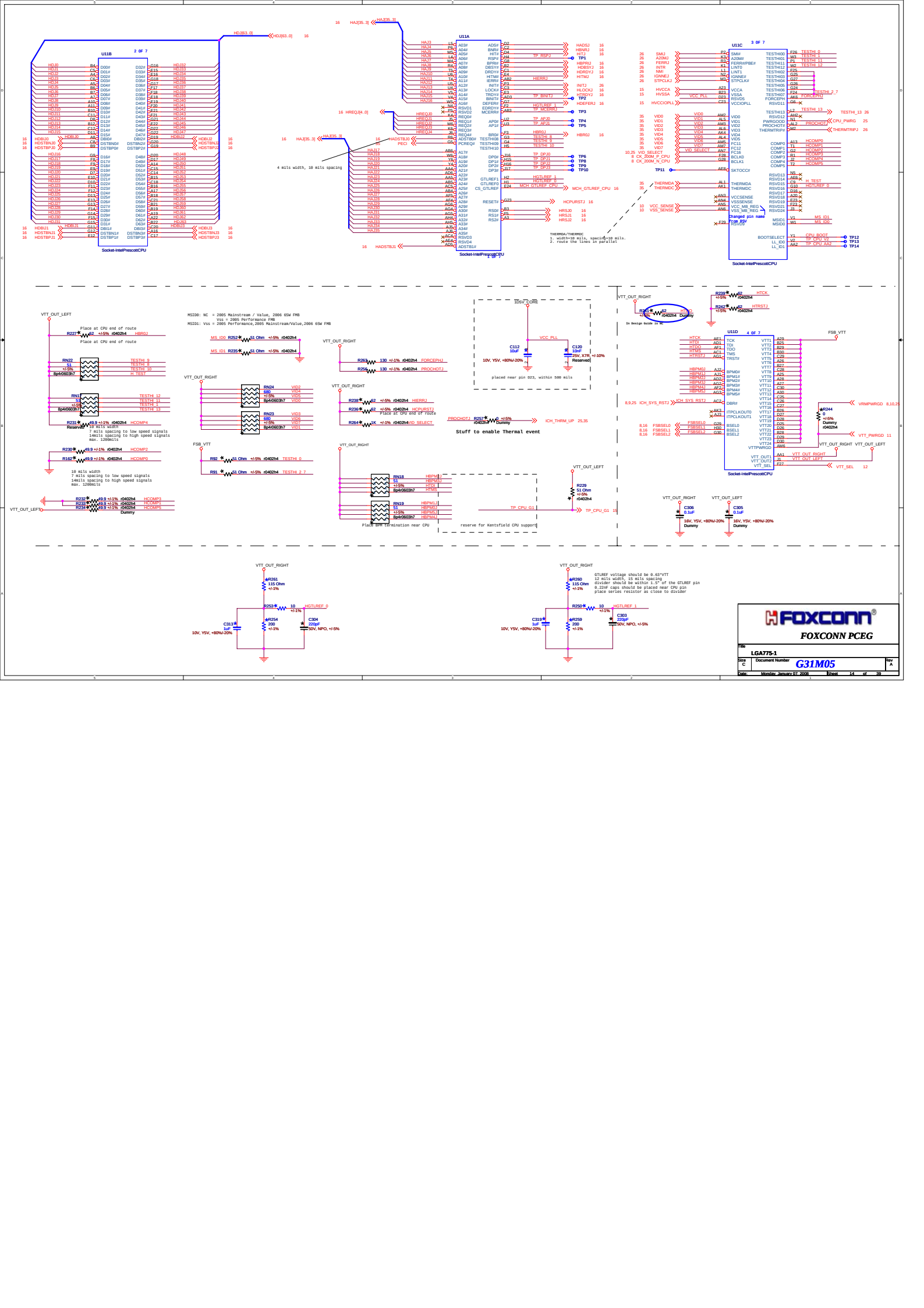
U11B
2 OF 7
Socket-IntelPrescottCPU
U11A
1 OF 7
Socket-IntelPrescottCPU
U11C
3 OF 7
Socket-IntelPrescottCPU
4 mils width, 10 mils spacing
THERMDA/THERMDC
1. width=10 mils, spacing=10 mils.
2. route the lines in parallel
U11D
4 OF 7
Socket-IntelPrescottCPU
Changed pin name from RSV
VTT_OUT_LEFT
Place at CPU end of route
MSID0: NC = 2005 Mainstream / Value, 2006 65W FMB
Vss = 2005 Performance FMB
MSID1: Vss = 2005 Performance,2005 Mainstream/Value,2006 65W FMB
10 mils width
7 mils spacing to low speed signals
14mils spacing to high speed signals
max. 1200mils
Stuff to enable Thermal event
reserve for Kentsfield CPU support
Place EMA termination near CPU
GTLREF voltage should be 0.63*VTT
12 mils width, 15 mils spacing
divider should be within 1.5" of the GTLREF pin
0.22nF caps should be placed near CPU pin
place series resistor as close to divider
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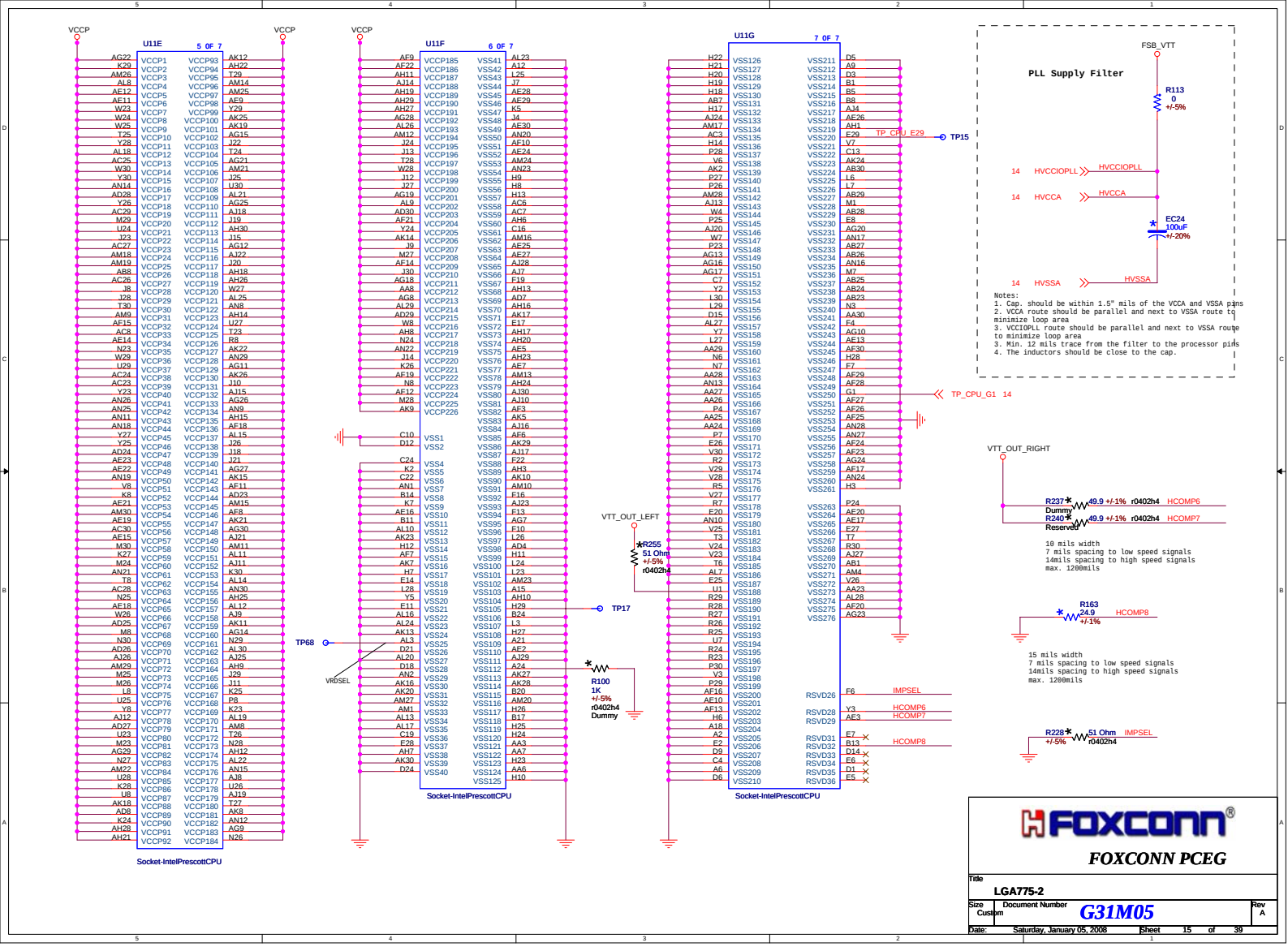

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Title	LGA775-2		
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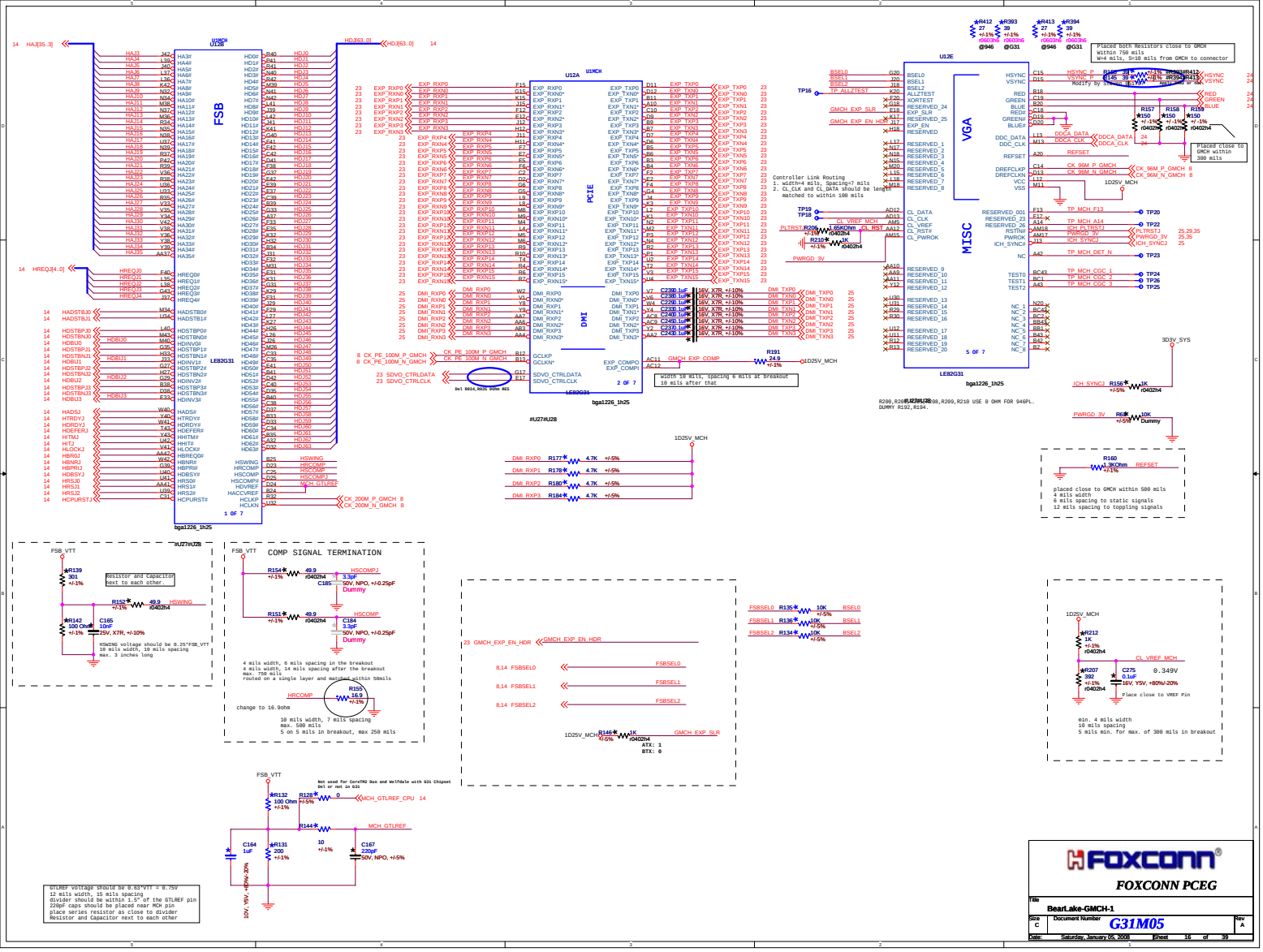
FSB
PCIE
DMI
VGA
MISC
COMP SIGNAL TERMINATION
FOXCONN PCEG
Bear Lake-GMCH-1
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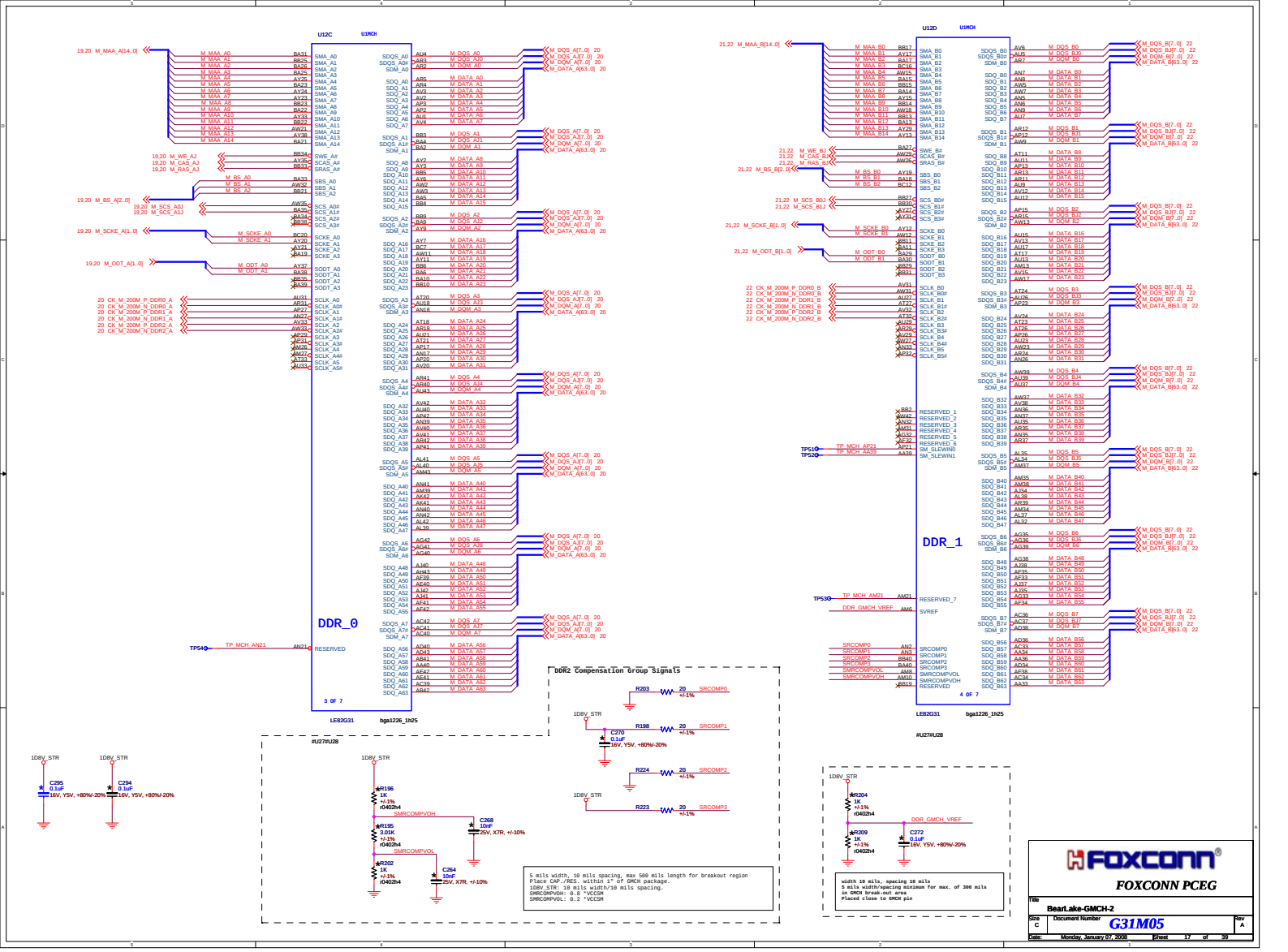

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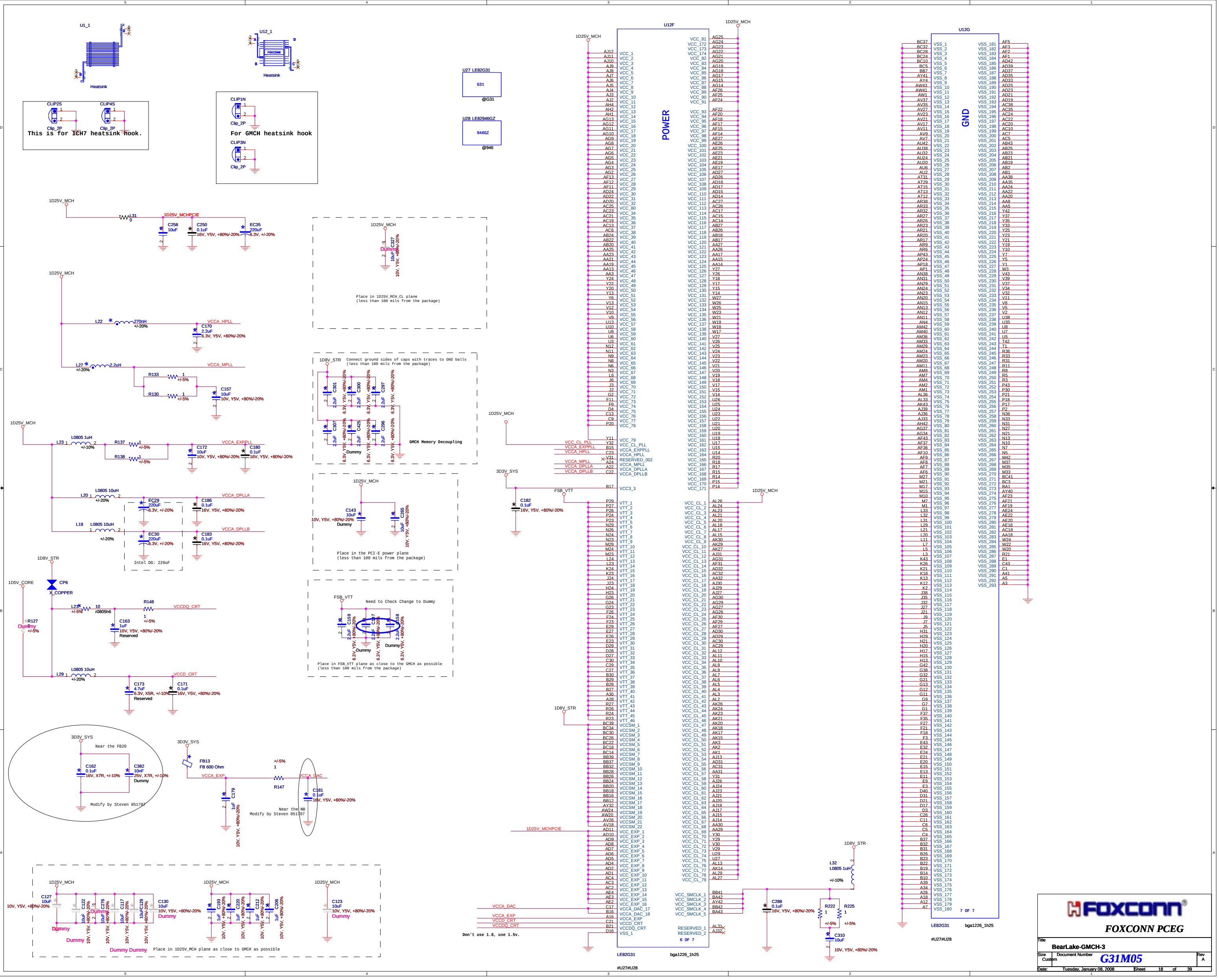

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Title: BearLake-GMCH-3

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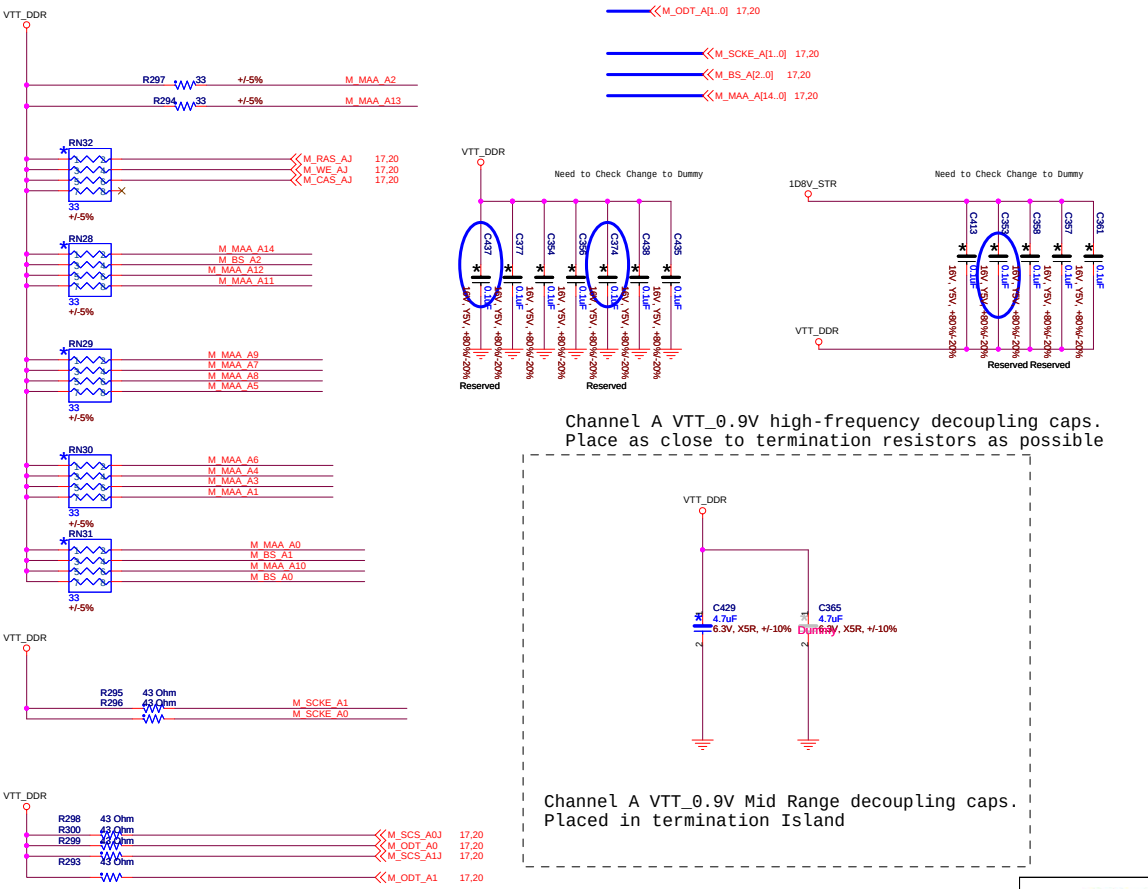

Channel A VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

Channel A VTT_0.9V Mid Range decoupling caps.
Placed in termination Island

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Title: DDR2 Channel A Termination			
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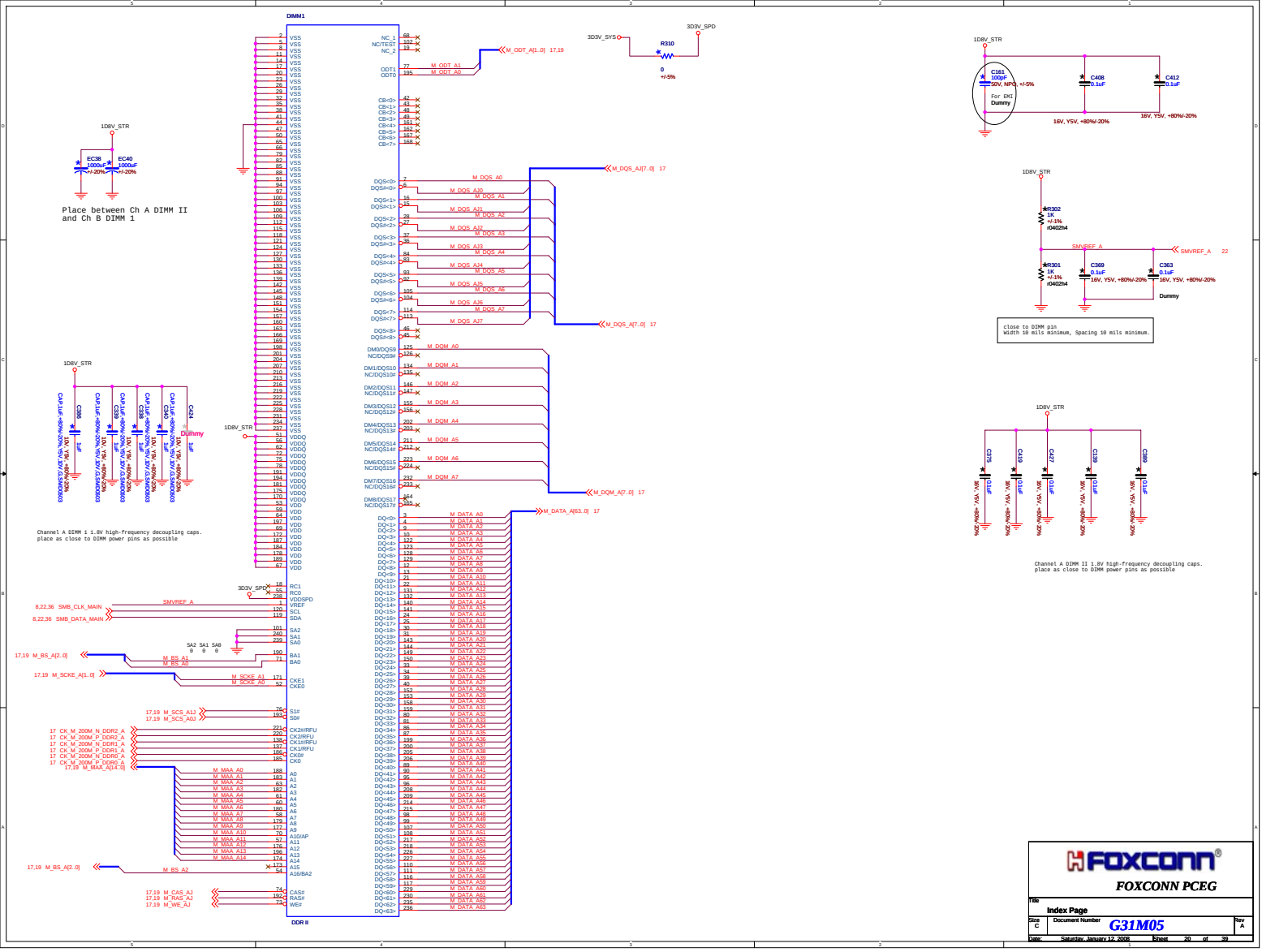
DIMM1
DDR II
1DBV_STR
3D3V_SYS
3D3V_SPD
R310
0
+/-5%
M_ODT_A[1..0] 17,19
M_DQS_A[7..0] 17
M_DQM_A[7..0] 17
M_DATA_A[63..0] 17
EC38
1000uF
+/-20%
EC40
1000uF
+/-20%
Place between Ch A DIMM II
and Ch B DIMM 1
C161
100uF
50V, NPO, +/-5%
For EMI
Dummy
C408
0.1uF
C412
0.1uF
16V, Y5V, +80%/-20%
R302
1K
+/-1%
r0402fr4
SMVREF_A
R301
1K
+/-1%
r0402fr4
C369
0.1uF
16V, Y5V, +80%/-20%
C363
0.1uF
16V, Y5V, +80%/-20%
Dummy
close to DIMM pin
Width 10 mils minimum, Spacing 10 mils minimum.
Channel A DIMM 1 1.8V high-frequency decoupling caps.
place as close to DIMM power pins as possible
Channel A DIMM II 1.8V high-frequency decoupling caps.
place as close to DIMM power pins as possible
8,22,36 SMB_CLK_MAIN
8,22,36 SMB_DATA_MAIN
SA2 SA1 SA0
0 0 0
17,19 M_BS_A[2..0]
17,19 M_SCKE_A[1..0]
17,19 M_SCS_A[1..0]
17 CK_M_200M_N_DDR2_A
17 CK_M_200M_P_DDR2_A
17 CK_M_200M_N_DDR1_A
17 CK_M_200M_P_DDR1_A
17 CK_M_200M_N_DDR0_A
17 CK_M_200M_P_DDR0_A
17,19 M_MAA_A[14:0]
17,19 M_CAS_AJ
17,19 M_RAS_AJ
17,19 M_WE_AJ
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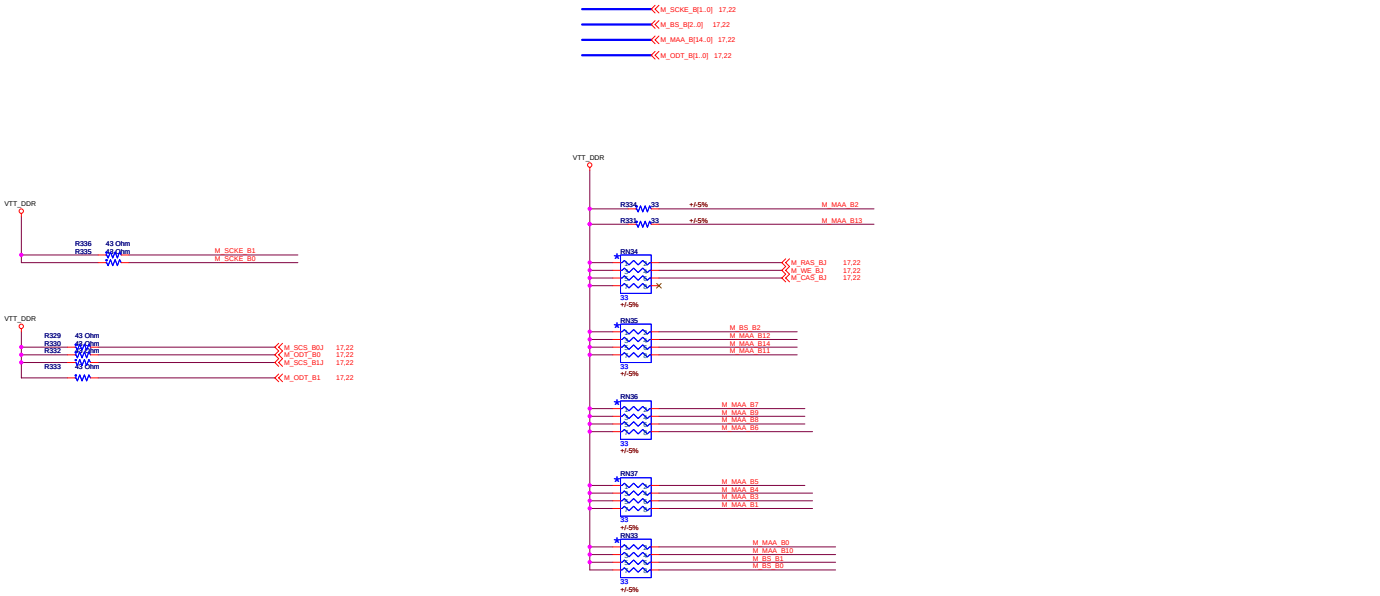
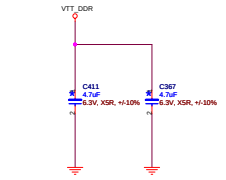
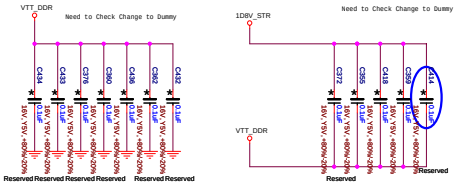




Channel B VTT_0.9V Mid Range decoupling caps.
Placed in termination Island



Channel B VTT_0.9V high-frequency decoupling caps.
Place as close to termination resistors as possible

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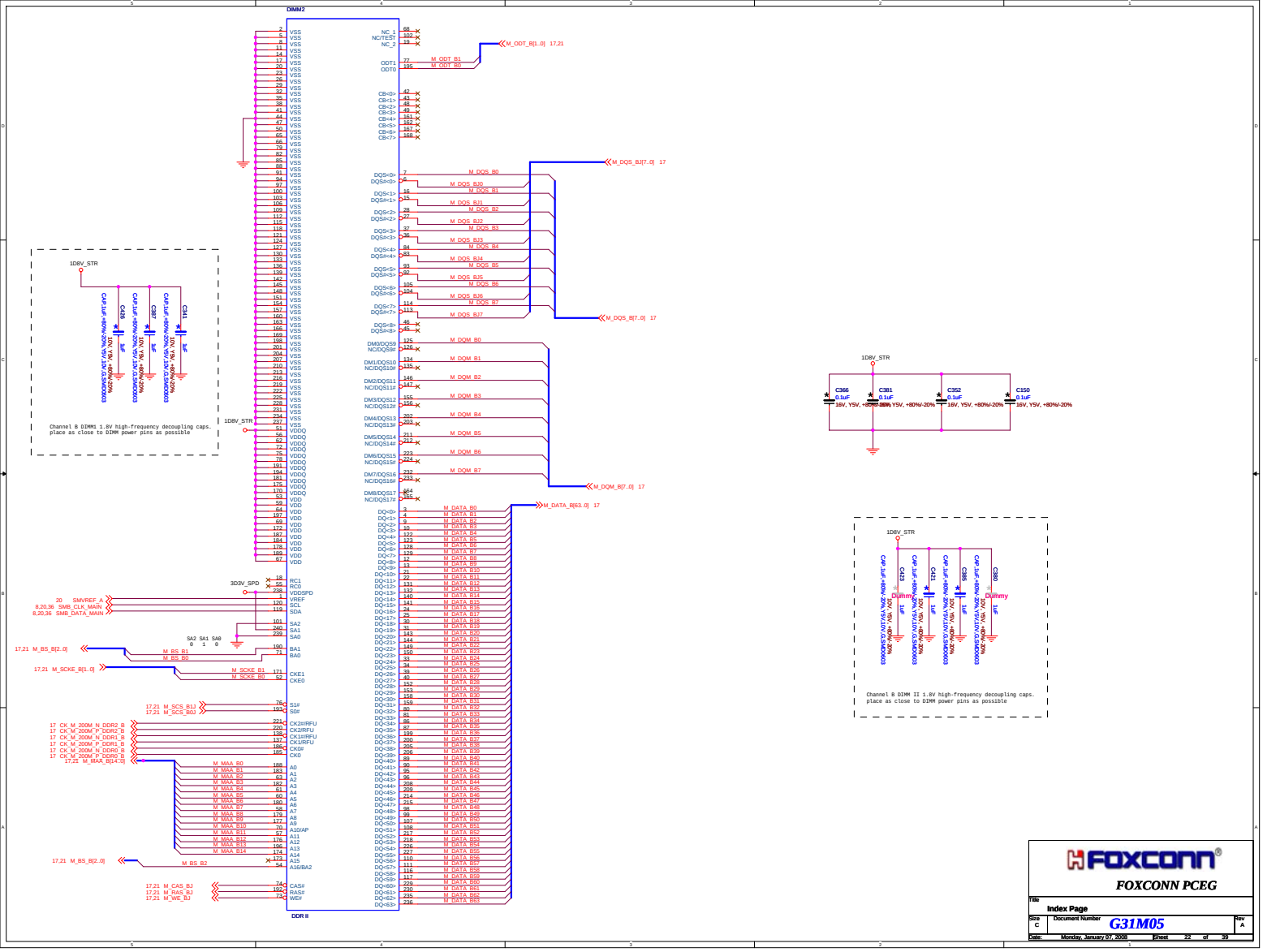

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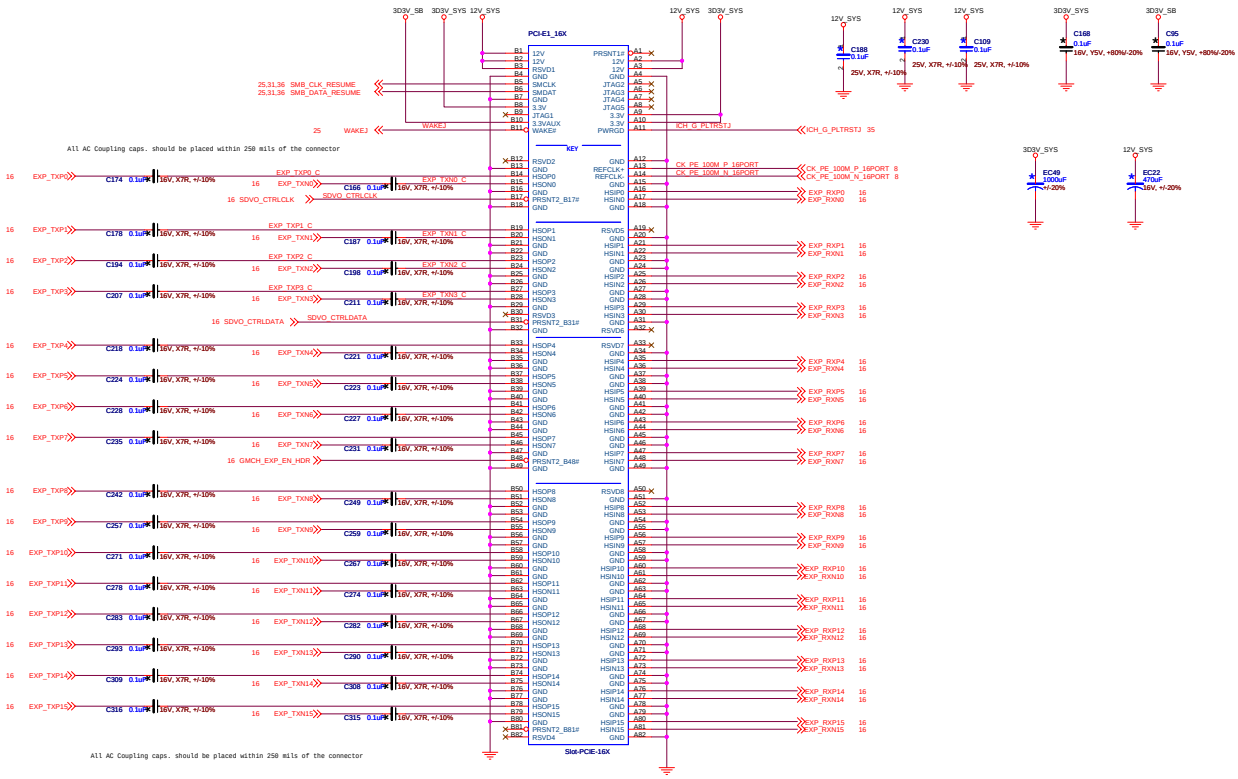

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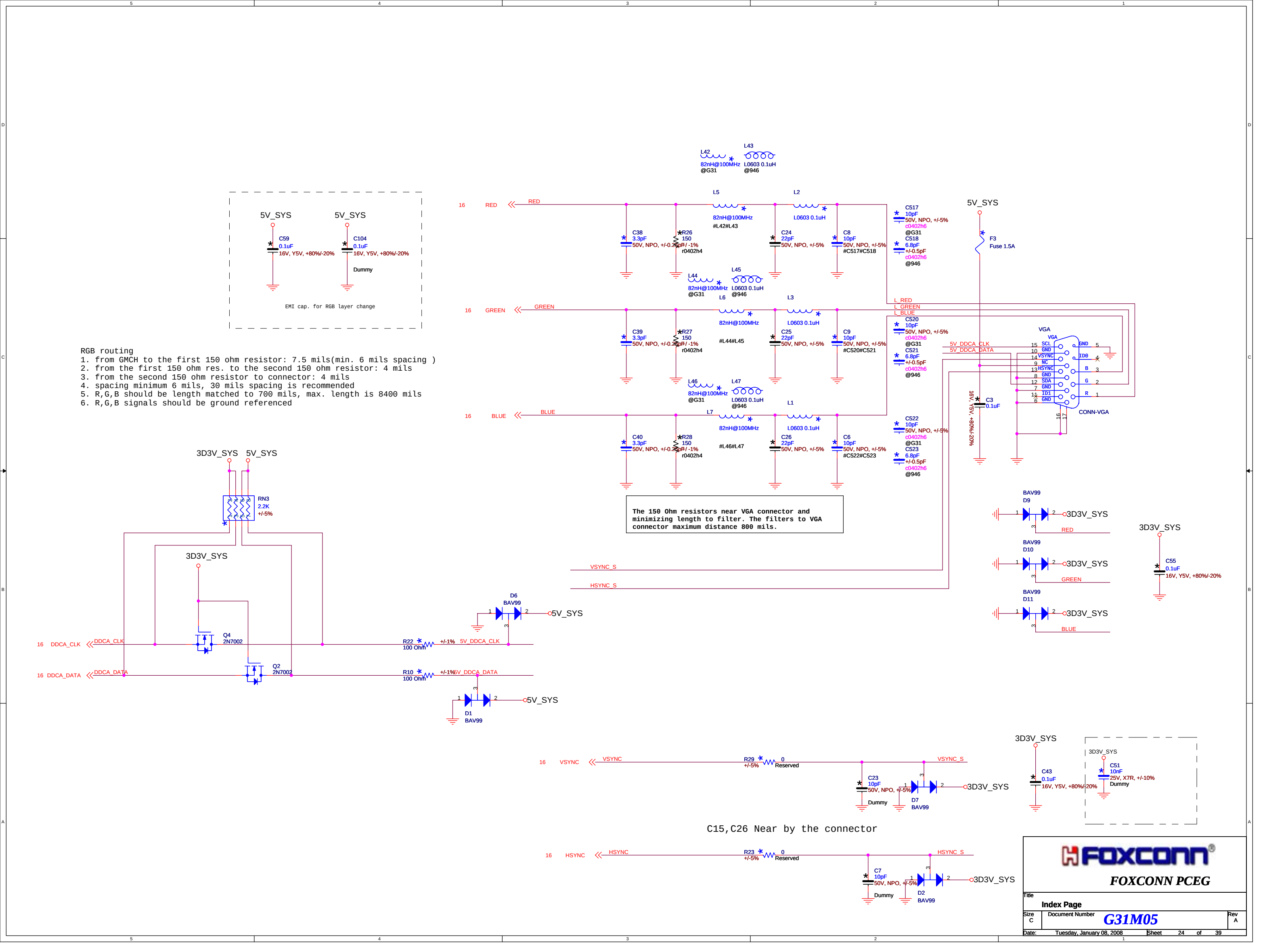

RGB routing
1. from GMCH to the first 150 ohm resistor: 7.5 mils(min. 6 mils spacing)
2. from the first 150 ohm res. to the second 150 ohm resistor: 4 mils
3. from the second 150 ohm resistor to connector: 4 mils
4. spacing minimum 6 mils, 30 mils spacing is recommended
5. R,G,B should be length matched to 700 mils, max. length is 8400 mils
6. R,G,B signals should be ground referenced
EMI cap. for RGB layer change
The 150 Ohm resistors near VGA connector and minimizing length to filter. The filters to VGA connector maximum distance 800 mils.
C15,C26 Near by the connector
5V_SYS
3D3V_SYS
C59
0.1uF
16V, Y5V, +80%/-20%
C104
Dummy
RED
GREEN
BLUE
L_RED
L_GREEN
L_BLUE
VSYNC
HSYNC
VSYNC_S
HSYNC_S
DDCA_CLK
DDCA_DATA
5V_DDCA_CLK
5V_DDCA_DATA
L42
L43
82nH@100MHz
L0603 0.1uH
@G31
@946
L5
L2
L44
L45
L6
L3
L46
L47
L7
L1
#L42#L43
#L44#L45
#L46#L47
C38
C39
C40
3.3pF
R26
R27
R28
150
r0402h4
C24
C25
C26
22pF
50V, NPO, +/-5%
C8
C9
C6
10pF
#C517#C518
#C520#C521
#C522#C523
C517
C518
C520
C521
C522
C523
6.8pF
+/-0.5pF
c0402h6
F3
Fuse 1.5A
C3
0.1uF
VGA
CONN-VGA
RN3
2.2K
+/-5%
Q4
Q2
2N7002
R22
R10
100 Ohm
+/-1%
D6
D1
D9
D10
D11
D7
D2
BAV99
C55
C43
C51
10nF
25V, X7R, +/-10%
R29
R23
0
Reserved
C23
C7
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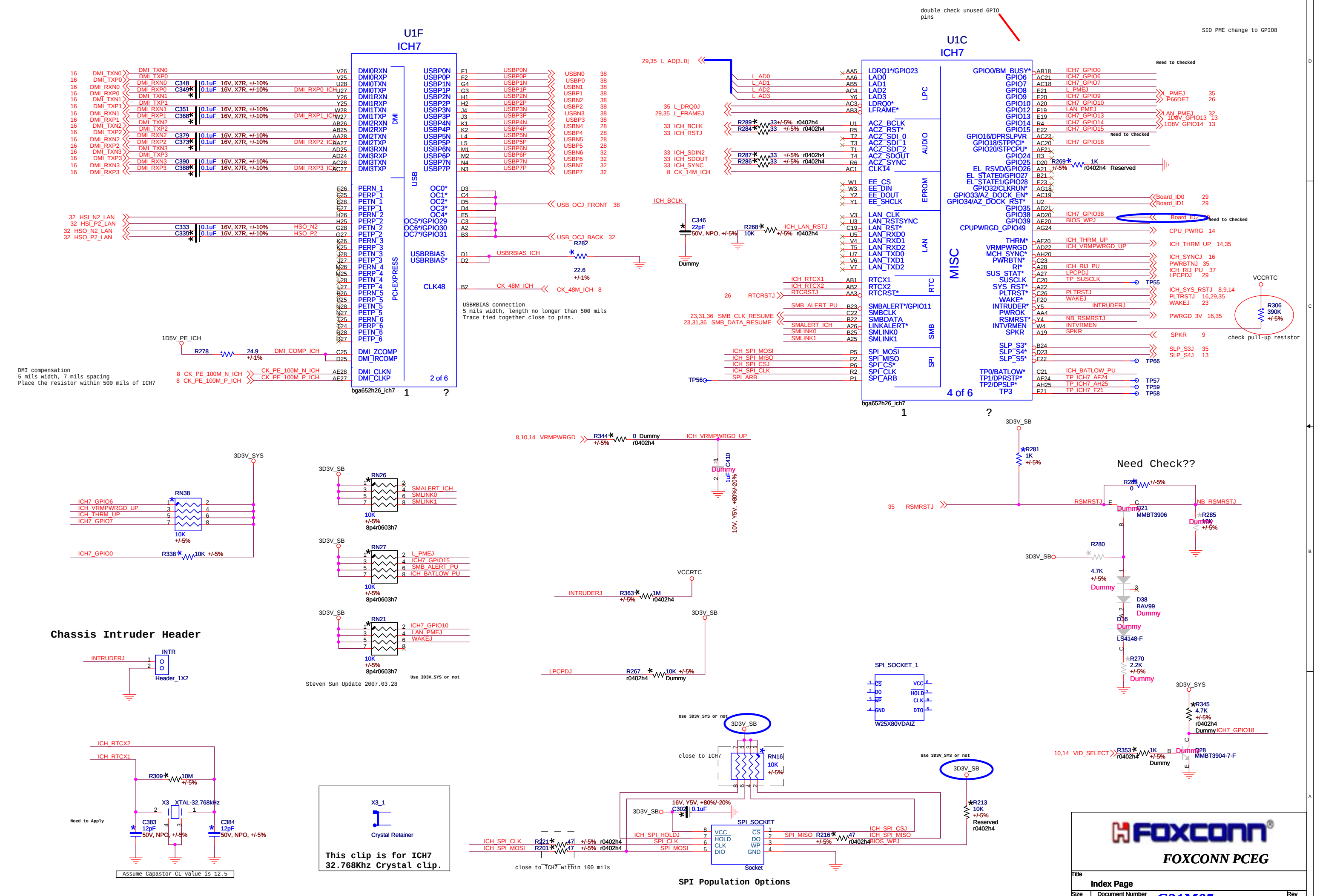
GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.



U1F
ICH7
DMI
USB
PCI-EXPRESS
2 of 6
bga652h26_ich7
U1C
ICH7
LPC
AUDIO
EPROM
LAN
RTC
SMB
SPI
MISC
4 of 6
double check unused GPIO pins
SIO PME change to GPIO8
Need to Checked
DMI compensation
5 mils width, 7 mils spacing
Place the resistor within 500 mils of ICH7
USBRBIAS connection
5 mils width, length no longer than 500 mils
Trace tied together close to pins.
check pull-up resistor
Need Check??
Chassis Intruder Header
Steven Sun Update 2007.03.28
Use 3D3V_SYS or not
SPI_SOCKET_1
W25X80VDAIZ
close to ICH7
close to ICH7 within 100 mils
SPI Population Options
Need to Apply
Assume Capastor CL value is 12.5
X3_1
Crystal Retainer
This clip is for ICH7
32.768Khz Crystal clip.

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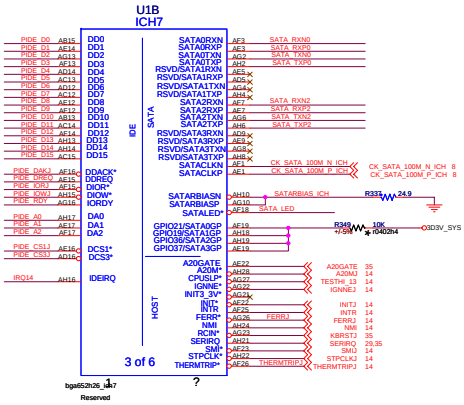
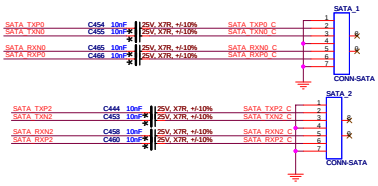
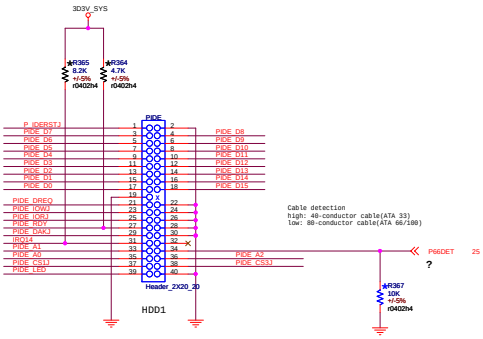
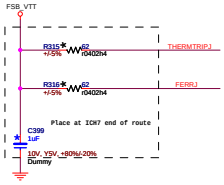


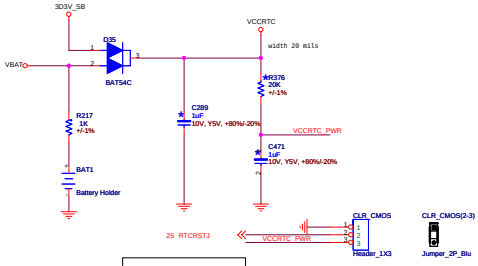


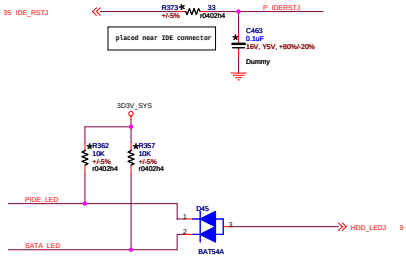
SATARBIAS connection
5 mils width, length no longer than 500 mils
Trace tied together close to pins.



IDE data lines should be matched to strobes(IORJ, IOWJ)within +/- 250 mils, strobes should be matched to their complement within +/- 10 mils







BAT1_1
Battery
For battery cell.

Clear CMOS

CLR_CMOS	CMOS
Clear	(1-2)
Normal	(2-3) **Default**

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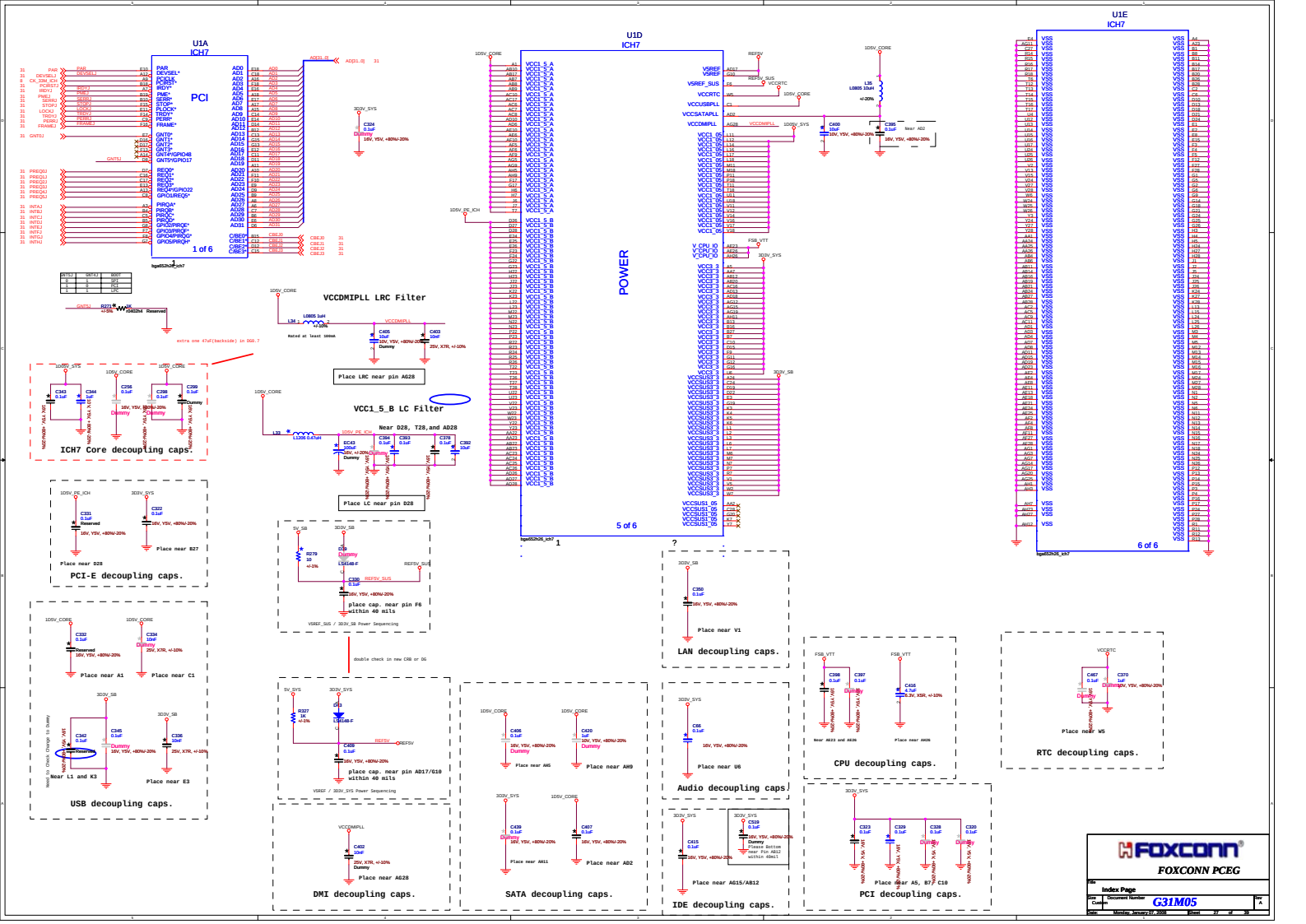
U1A
ICH7
PCI
1 of 6
U1D
ICH7
POWER
5 of 6
U1E
ICH7
6 of 6
VCCDMIPLL LRC Filter
VCC1_5_B LC Filter
Near D28, T28,and AD28
Place LRC near pin AG28
Place LC near pin D28
ICH7 Core decoupling caps.
PCI-E decoupling caps.
USB decoupling caps.
DMI decoupling caps.
SATA decoupling caps.
LAN decoupling caps.
Audio decoupling caps
IDE decoupling caps.
CPU decoupling caps.
RTC decoupling caps.
PCI decoupling caps.
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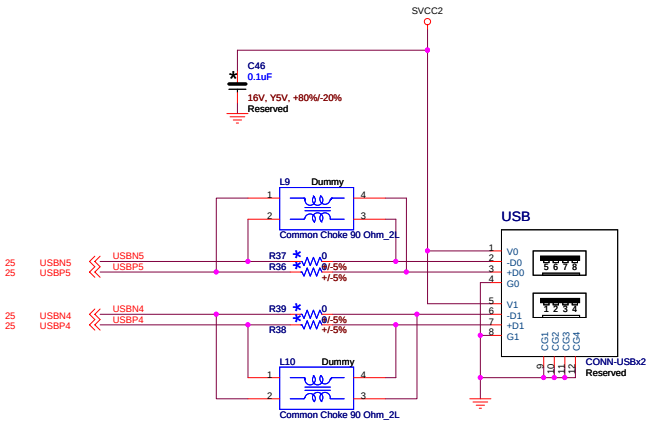
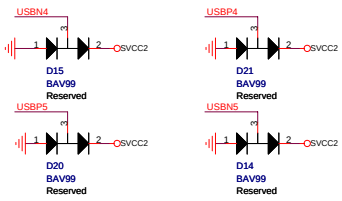
Rear Dual USB Connector





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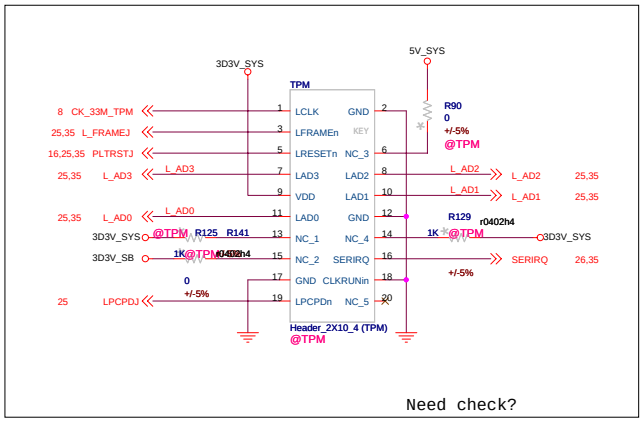
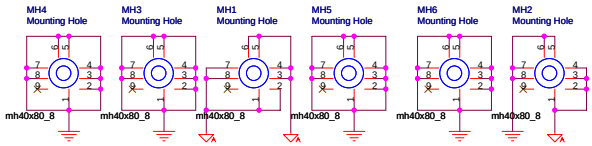
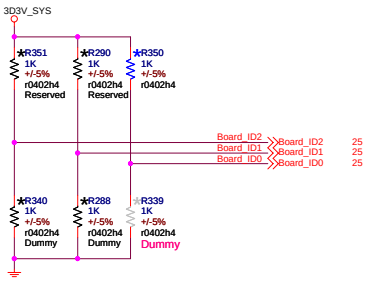
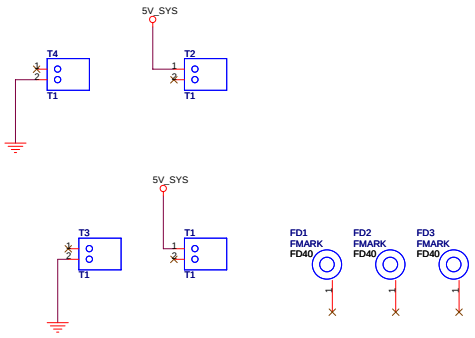


Need check?







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Title: PCI Express x1 Slot

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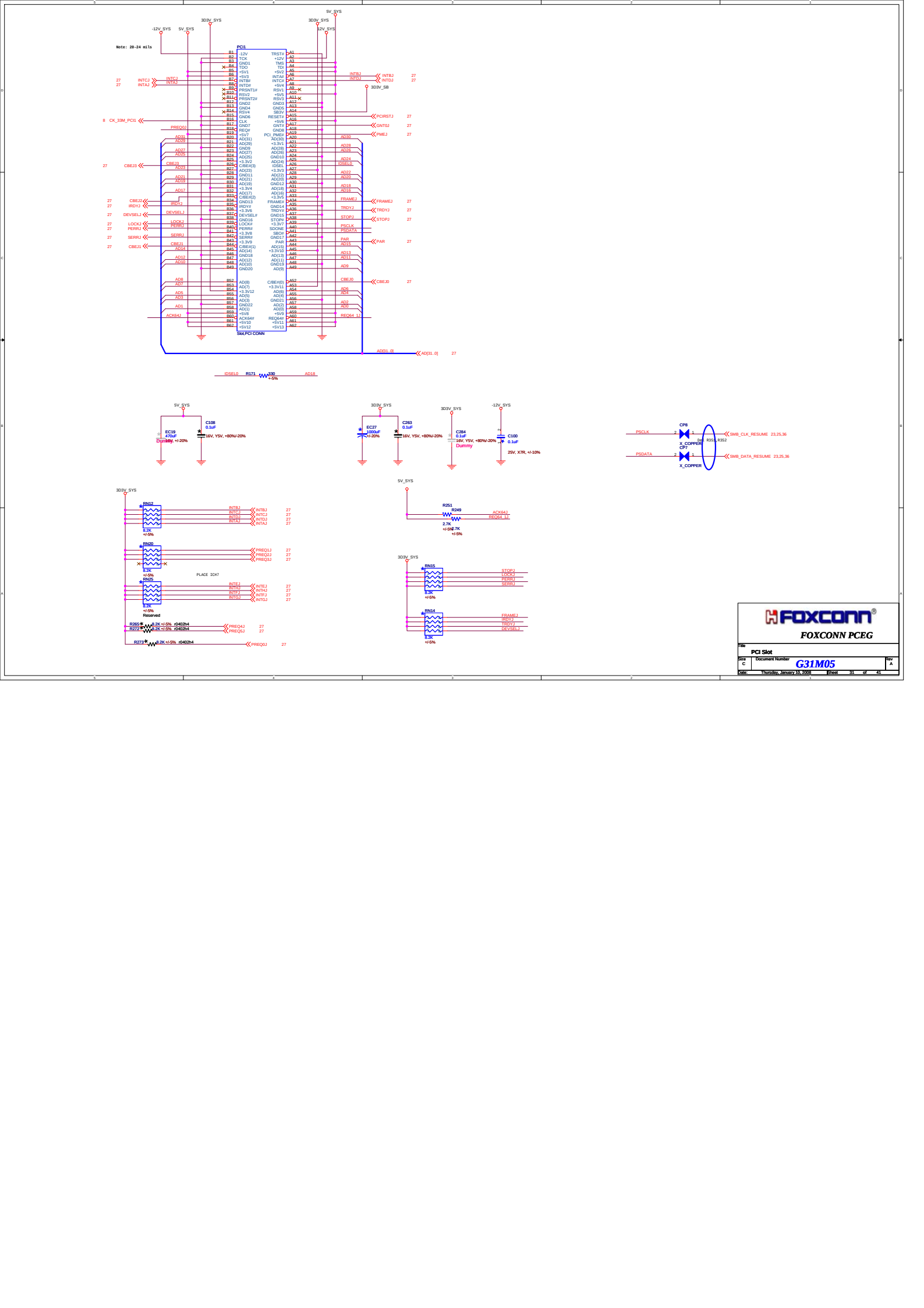

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Title	PCI Slot	
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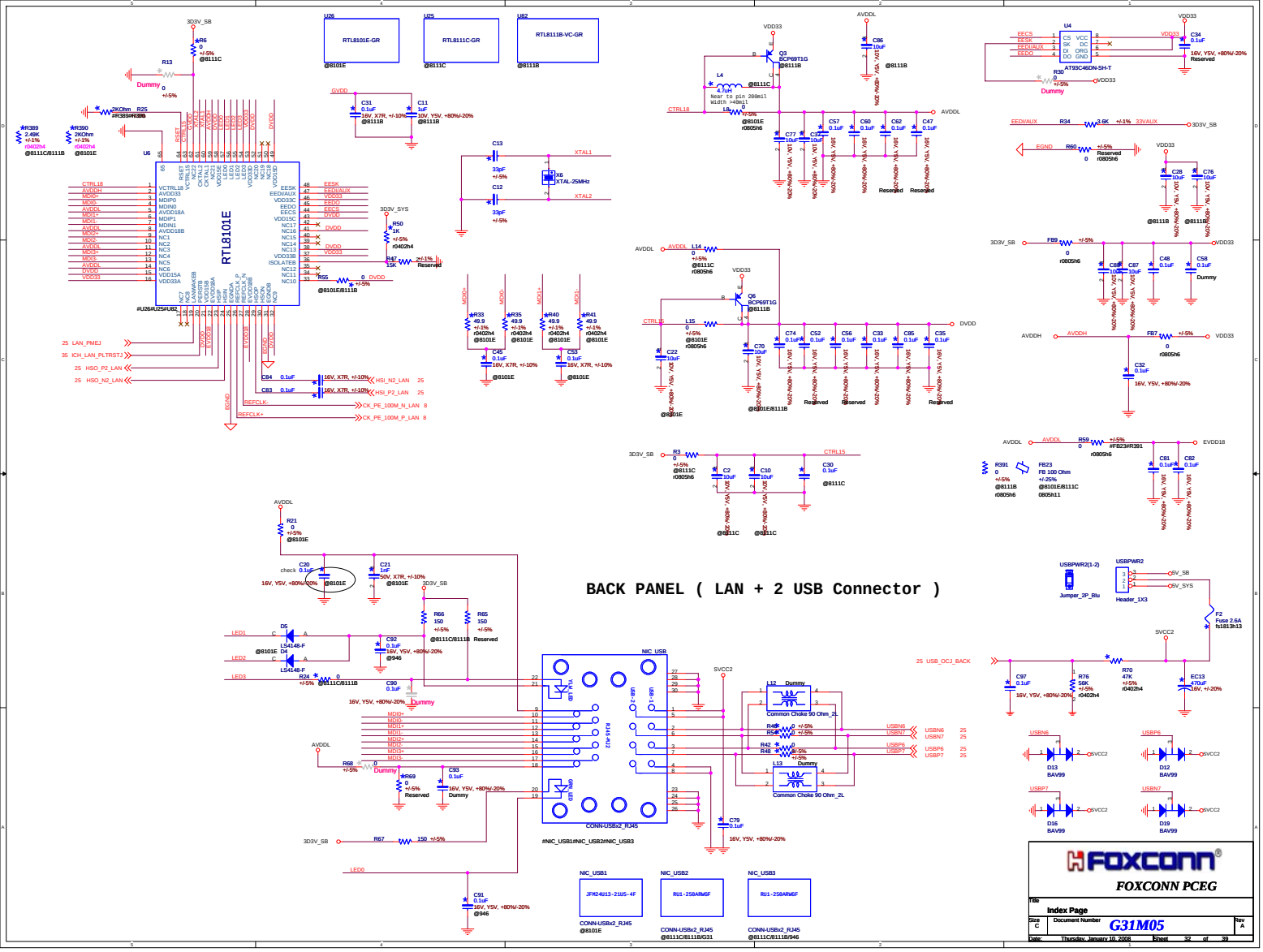

BACK PANEL (LAN + 2 USB Connector)

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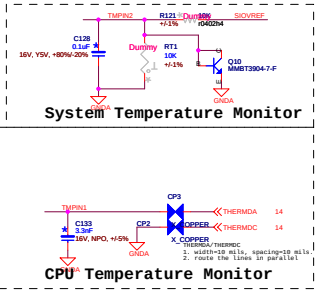

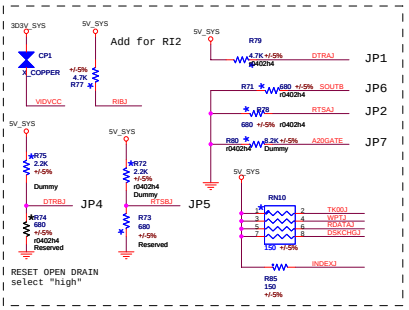

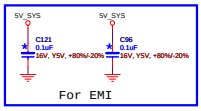

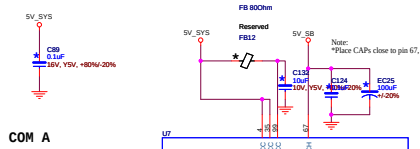

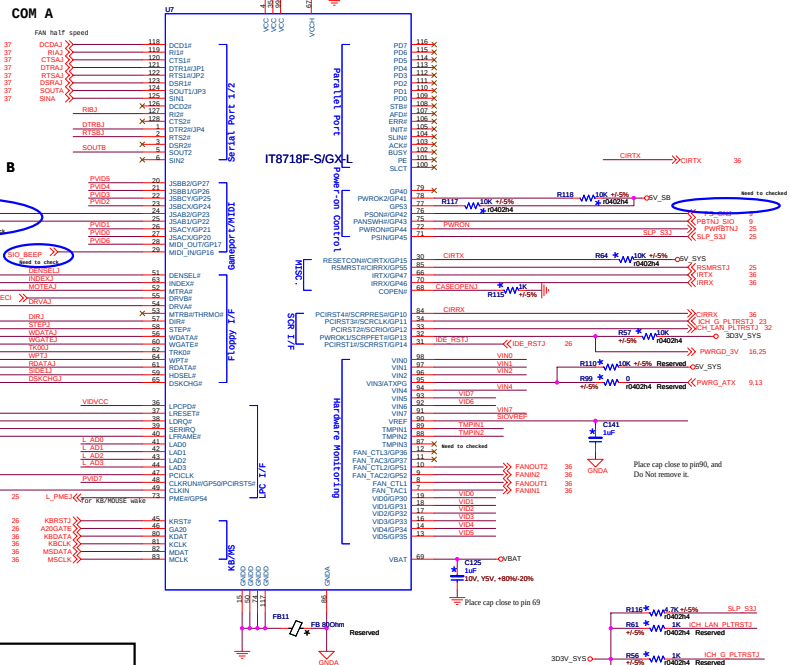

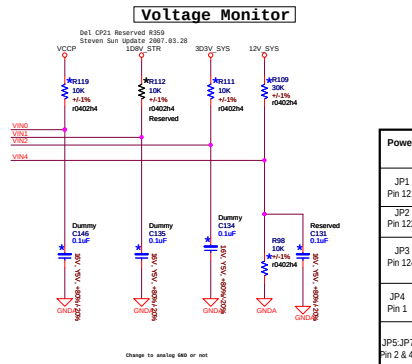

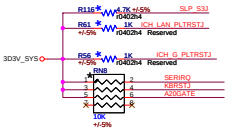

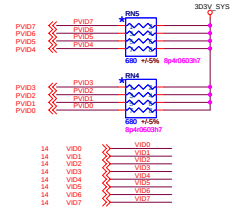

Power On Strapping Options

	Symbol	value	Description
JP1 Pin 121	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 (FFF8_0000h~FFFF_FFFFh, 000E_0000h~000F_FFFFh) is enabled
JP2 Pin 122	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 124	CHIP_SEL	1	Use for chip 1 when two IT8718F exit in the same system. Chip is selected in conjunction with "Global Configuration Register - Index 22, bit 7
		0	Use for chip 0 when two IT8718F exit in the same system. Chip is selected in conjunction with "Global Configuration Register - Index 22, bit 7
JP4 Pin 1	BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3# and PCIRST4# are open-drain.
		0	The output buffers are push-pull.
JP5:JP7 Pin 2 & 46	FAN_CTL_SEL	11	The default value of EC Index 15h / 16h / 17h is 00h
		10	The default value of EC Index 15h / 16h / 17h is 20h
		01	The default value of EC Index 15h / 16h / 17h is 40h
		00	The default value of EC Index 15h / 16h / 17h is 60h
JP6 Pin 5	VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
		0	The threshold voltage of VID is 0.8 / 0.4V
JP7 Pin 46	WDT_EN	1	Disable WDT to reset PWROK
		0	Enable WDT to reset PWROK

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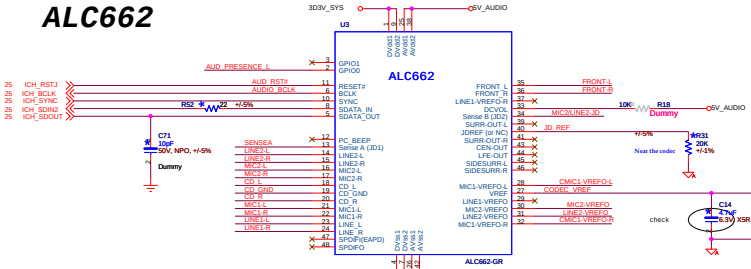
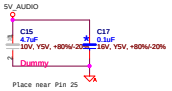
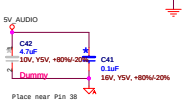
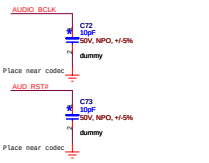
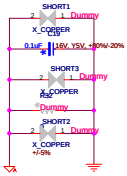
ALC662

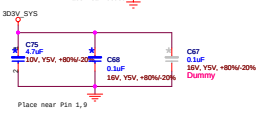


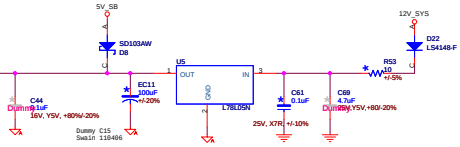










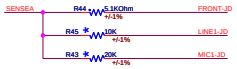


12V to 5V Power Regulator

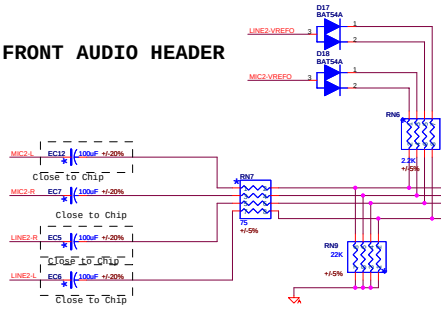
SPDIF Header

del SPDIF OUT

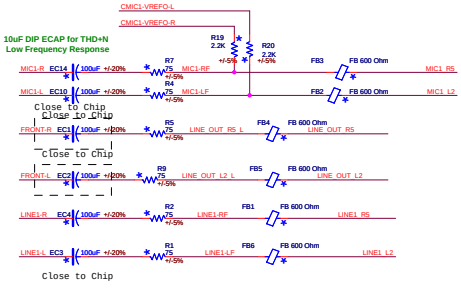
All JD resistors should be placed near CODEC

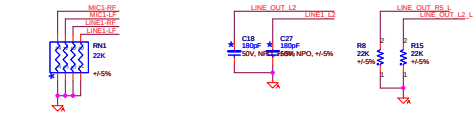


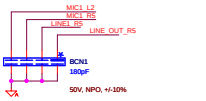
FRONT AUDIO HEADER

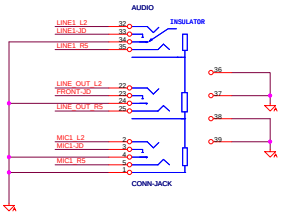


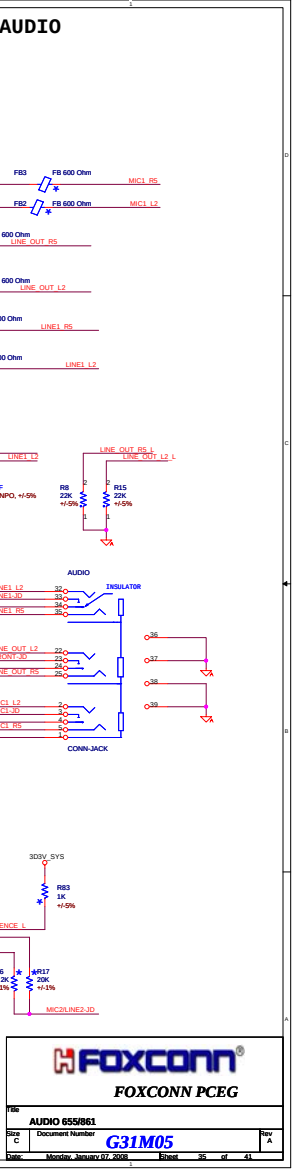
Rear AUDIO



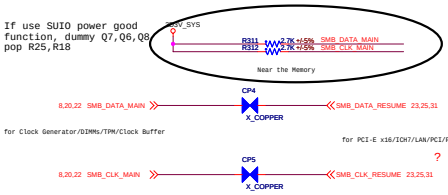


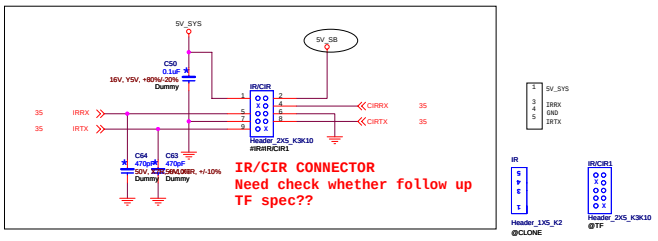


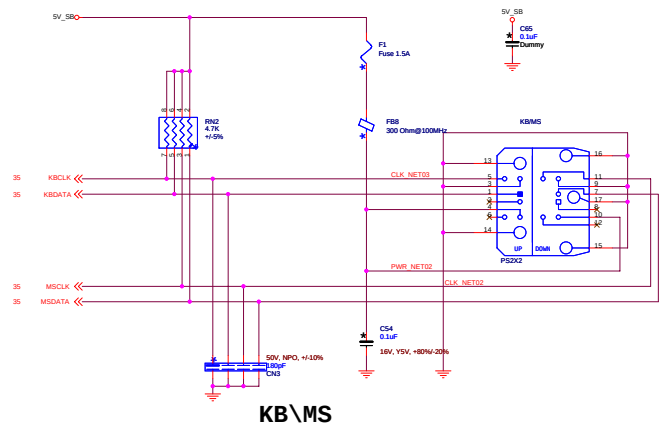




SM Bus Bridge

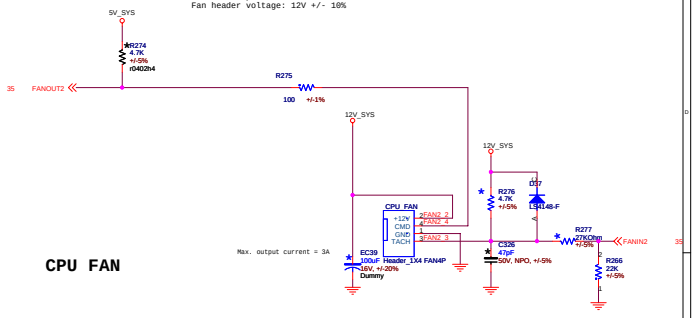




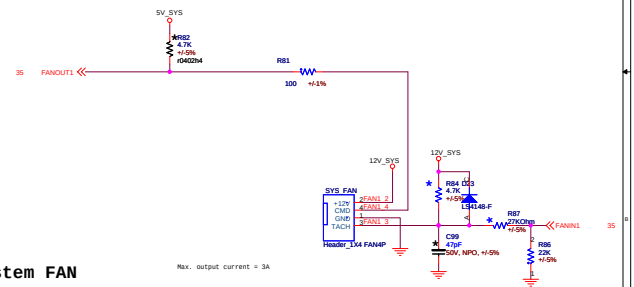


KB\MS

Peak fan current draw: 1.5A
Average fan current draw: 1.1A
Fan start-up current draw: 2.2A
Fan start-up current draw maximum duration: 1.0 second
Fan header voltage: 12V +/- 10%



CPU FAN



System FAN

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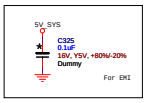
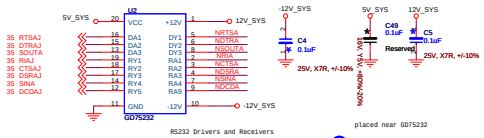
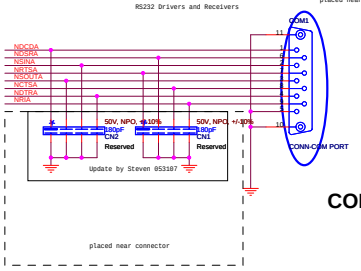
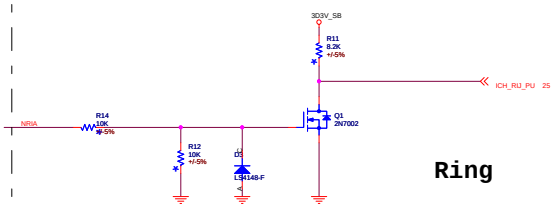






COM 1

PRT PORT



Ring

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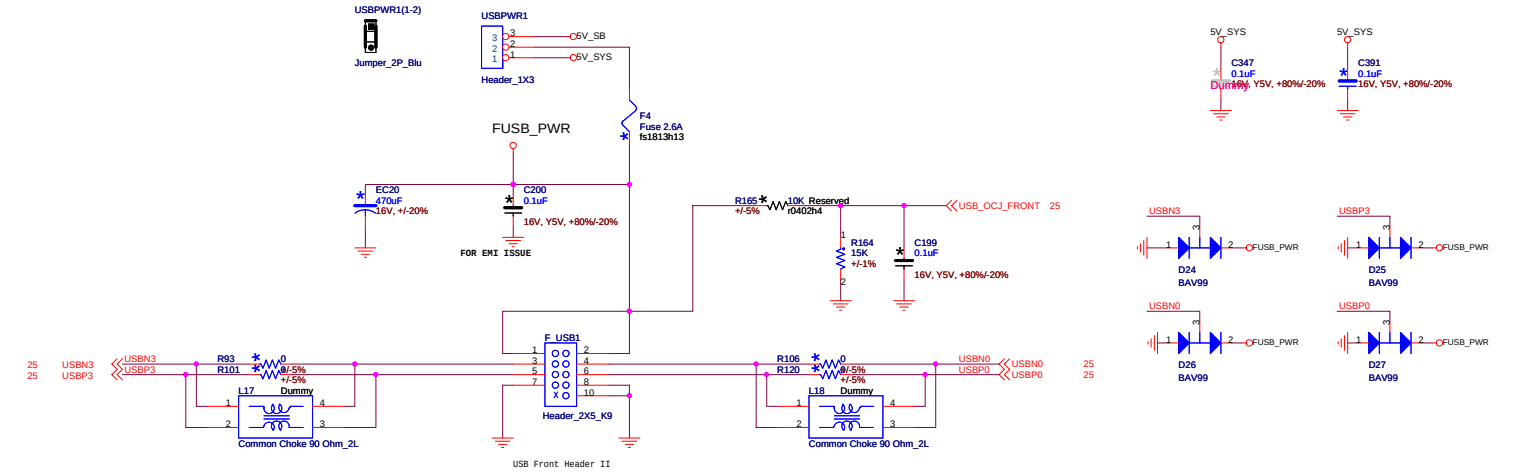

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1. Change Lan RTL8111B colay RTL8101E to RTL8111C colay RTL8101E
2. Change Audio ALC888 colay ALC883 to ALC662 colay ALC888
3. Reserved Memory ratio schematic for over clock.
4. Del R108,C139,Q22,Q20,R107 and then connect VRMPWGD directly for VRD11.
5. Add R371,C501 for power button debounce circuit.
6. Reserved U15,U17 for TF spec.
7. Reserved TPM Header for TF spec.
8. Reserved U3,U6 for TF spec.
9. Add R8,R1,R5,R10,R6,R14,R87,R86,R85,R84,R78,R76,R73,R75,R41,R55 for Audio ESD
10. Reserved CIR function for TF spec.
11. Reserved NB FAN.
12. Reserved C307,C314,C324,C318,C348,C350,C360,C357 for TF Front Panel
13. Change R335 to 91ohm,R337 to 115ohm for Memory Power
14. Remove R338 and stuff R332 for FAN half speed when Power on.
15. Reserved R46 for realtek's suggestion
16. Reserved U9,C144,C145 for VCCA_DAC
17. Add RT8111B SCH
18. Del EC72,EC55,EC54,EC73 for placement issue
19. Reserved R40,R25 For EMI
21. Add C16,C17 For RTL8111B LAN Chip EMI
22. Add FB22 For ITE suggestion
23. Reserved C497 for Front Panel ESD
24. Del Power V15SFR SCH
25. Add R208,R220 for further CPU
26. Reserved R321,R109,R320 for PCI RST
27. Disconnect SLP_S4 with CLK Gen
28. Change C368,C371 from 18pF to 12pF
29. Change F_AUDIO Pin7 connect to Audio_GND directly and connect Pin6,Pin10 to codec through the resistor.

After Gerber Out:

30. Reserved C506
31. Change R363 size from 0402 to 0603
32. Change R111 to 33ohm 1%
33. Add R400 100ohm 1%
34. Dummy Q24 C146
35. Reserved R94 In 8KS2H SKU
36. Reserved R114,C147,R110,Q23,Q26
37. Change R116,R118 to 10K 1%
38. Change C160 to 1uF 0603
39. Reserved Q39
40. Del CP2
41. Del EC29
42. Reserved R356
43. Change PCIe_16x slot to 2EG48211-S7Y-4F
44. Del EC65,EC66
45. Add EC68
46. Change L25,L38 to 630307400-176-G
47. Reserved C451,C396,C375,C381,C430,C441,C355,C436,C447,C448,C397,C385,C446,C427,C405,C401,C395,C353,C390
48. Del RN17
49. Add R401,R402,R403 10K 5%
50. Add JP1,JP2, JP1(P1&P2),JP2(P1&P2)
51. Add R404 470ohm
52. Add EC69
53. Del EC46,EC47
54. Change L26,L37 to APL1108P-2R5L
55. Change C5,C6,C7 to 10pf
56. Change L8,L9,L10 to GL1608082NJT
57. Reserved C38,C65
58. Change CP14 to L40 10uH
59. Change L23 to 10uH
60. Add C139,C513,C514 10uF
61. Add EC65
62. Del CP24
63. Add R25 for EMC
64. Add R409,R410,R411 for Audio codec ESD protection
65. Change EC55 to 680uF
66. Change L23 From 10uH Inductor to 10ohm Resistor

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