Homa (TM15") Block Diagram

Project code: 91.4Z401.001
PCB P/N : 48.4Z401.011
REVISION : 07245-1

CLK GEN.
ICS 9LPRS365
3

Mobile CPU
Penryn
4, 5

EMC2102
25

HOST BUS 667/800/1066MHz@1.05V

DDR2
667/800 MHz
12,13

667/800MHz

DDR2
667/800 MHz
12,13

667/800MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11

CRT 19
LCD 16
HDMI 56

PCIex16

VGA Borad 34

X4 DMI 400MHz

C-Link0

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
20,21,22,23

Line In
41

MIC In
41

41
Line Out
(No-SPDIF)

41
INT.SPKR

RealTek
ALC268
39

AZALIA

OP AMP
G1412
40

OP AMP
G1454
40

RJ11

MODEM
MDC Card
28

PCI

Cardbus
OZ711MZ
36

MS/MS Pro/xD
/MMC/SD
5 in 1
31

PCMCIA
SLOT 37

LAN
Giga LAN
BCM5764M 32

TXFM
33

RJ45
33

New card
35

PWR SW
TPS2231 35

PCIex1

Mini Card
Kedron a/b/g/n 38

C Link1

Mini Card
Kedron a/b/g/n 38

LPC BUS

SATA

USB

HDD SATA
26

ODD SATA
25

Mini USB
Blue Tooth 27

Finger
Printer 57

Camera

USB
4 Port 29

KBC
Winbond
WPC775
42

Touch
Pad 42

INT.
KB 42

BIOS
Winbond
W25X80
43

Launch
Buttom
14

LPC
DEBUG
CONN.43

CRT
DVI
RJ45
USBX4
HP OUT
MIC IN
LINE IN

Port Replicator

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC
TPS51125 49

INPUTS	OUTPUTS
DCBATOUT	5V_S5(7A) 3D3V_S5(7A)

SYSTEM DC/DC
TPS51124 51

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(16A) 1D8V_S3(16A)

TPS51100 50

5V_S5	DDR_VREF_S3 (1.5A) DDR_VREF_S3_1

G9131

3D3V_S0	2D5V_S0 (300mA)

APL5912 50

1D8V_S3	1D5V_S0 (2.5A)

CHARGER
BQ24750 53

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC
ISL6266A 48

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 38A

GFX DC/DC
ISL6263 48

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 5.5A

970

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Title: BLOCK DIAGRAM
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Date: Thursday, April 03, 2008 | Sheet 1 of 57

ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config 1 bit 0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved, Rising Edge of PWROK.	This signal has a weak internal pull-down. This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	Tying this strap low configures DMI for ESI-compatible operation. This signal has a weak internal pull up. ESI compatible mode is for server platforms only.This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing. It has a weak internal pull up.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 10K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LAD[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1066 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG12	ALLZ	0 = ALLZ mode enabled (Note 3) **1 = Disabled (default)**
CFG13	XOR	0 = XOR mode enabled (Note 3) **1 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

3. Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

PCI Routing

page 31

	IDSEL	INT	REQ	GNT
RTS5158	AD25	G:CARDBUS	0	0

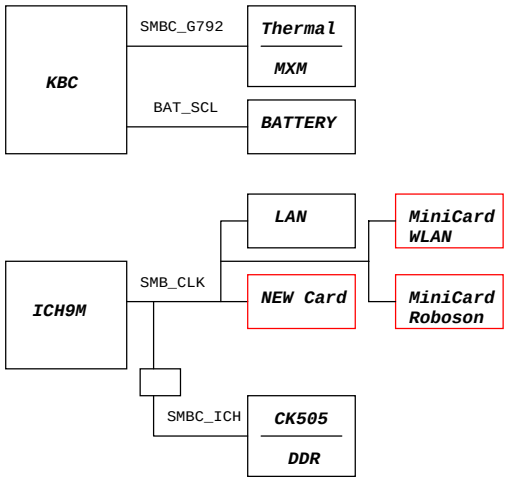
PCIE Routing

LANE1	LAN BCM5764MKMLG
LANE2	MiniCard WLAN
LANE3	MiniCard Roboson
LANE4	NewCard

USB Table

USB	
Pair	Device
0	USB1
1	USB4
2	USB2
3	DOCK USB
4	USB3
5	Bluetooth
6	FP
7	MINIC1
8	WEBCAM
9	NEW1
10	MINIC2
11	NC

SMBus



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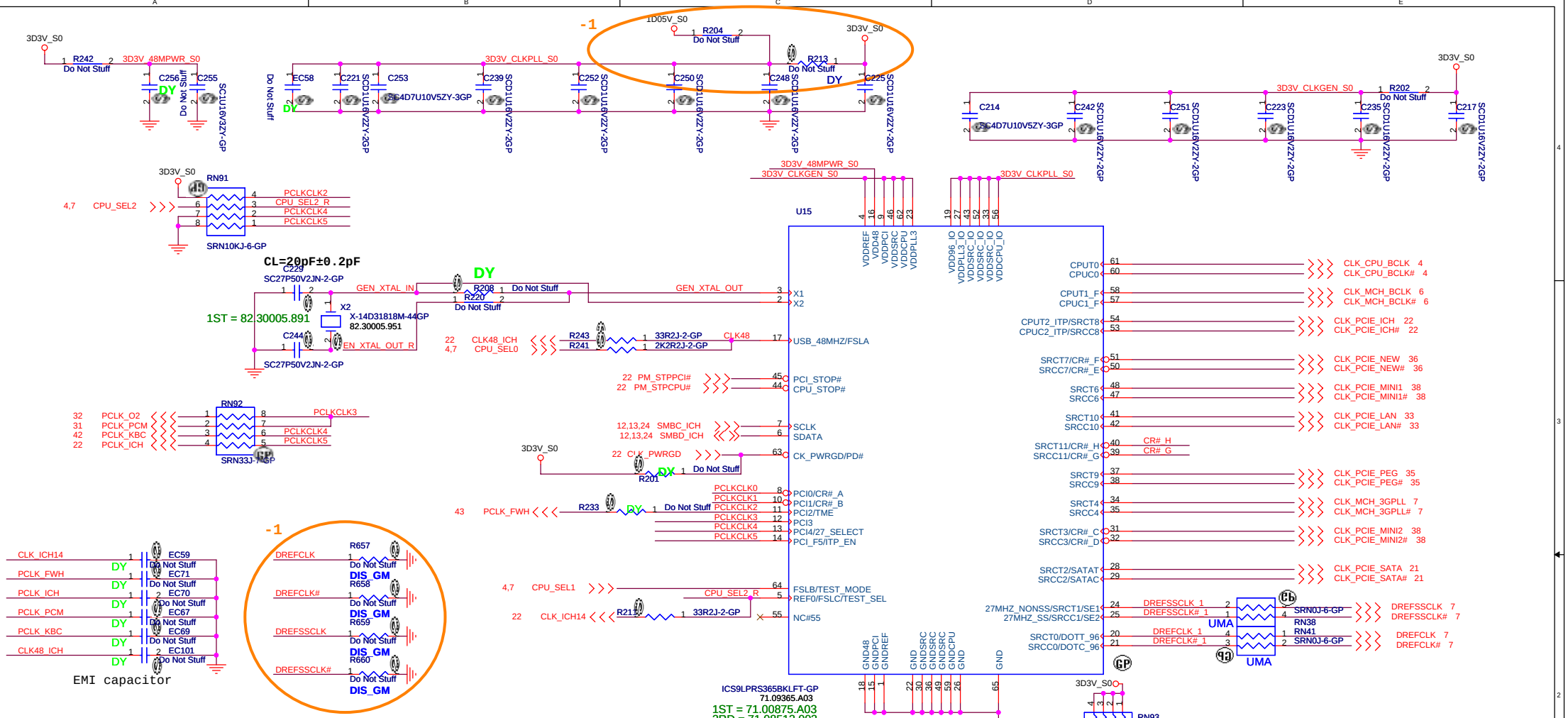

ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

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Title: *Clock Generator*

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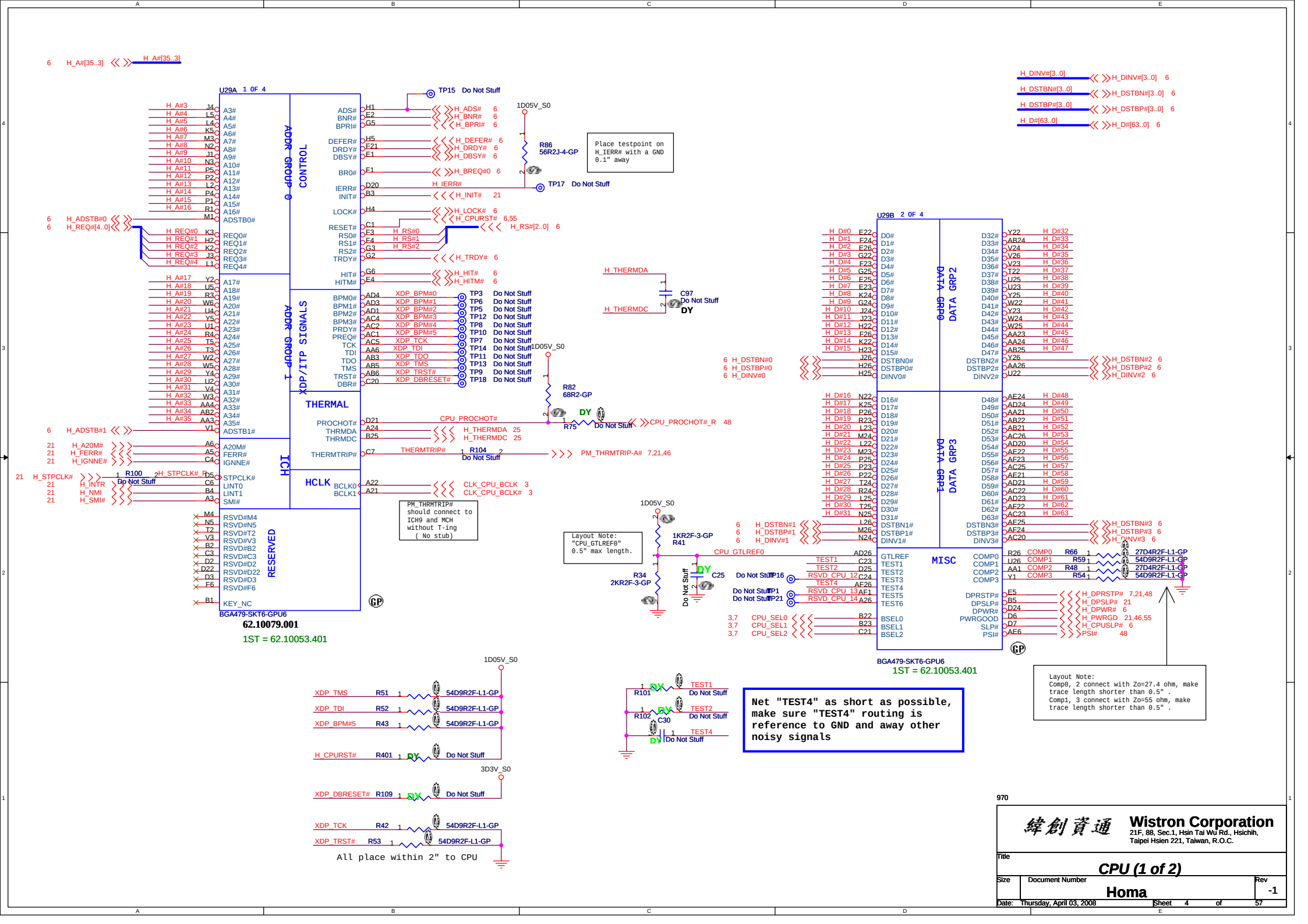
U29A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU6
62.10079.001
1ST = 62.10053.401
U29B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP1
DATA GRP3
MISC
BGA479-SKT6-GPU6
1ST = 62.10053.401
TP15 Do Not Stuff
TP17 Do Not Stuff
R86 56R2J-4-GP
Place testpoint on H_IERR# with a GND 0.1" away
R82 68R2-GP
R75 Do Not Stuff
R104 Do Not Stuff
R100 Do Not Stuff
C97 Do Not Stuff DY
C25 Do Not Stuff
R41 1KR2F-3-GP
R34 2KR2F-3-GP
Layout Note: "CPU_GTLREF0" 0.5" max length.
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
All place within 2" to CPU
1D05V_S0
3D3V_S0
XDP_TMS R51 54D9R2F-L1-GP
XDP_TDI R52 54D9R2F-L1-GP
XDP_BPM#5 R43 54D9R2F-L1-GP
H_CPURST# R401 DY Do Not Stuff
XDP_DBRESET# R109 DY Do Not Stuff
XDP_TCK R42 54D9R2F-L1-GP
XDP_TRST# R53 54D9R2F-L1-GP
R101 DY TEST1 Do Not Stuff
R102 DY TEST2 Do Not Stuff
C30 DY TEST4 Do Not Stuff
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Title
CPU (1 of 2)
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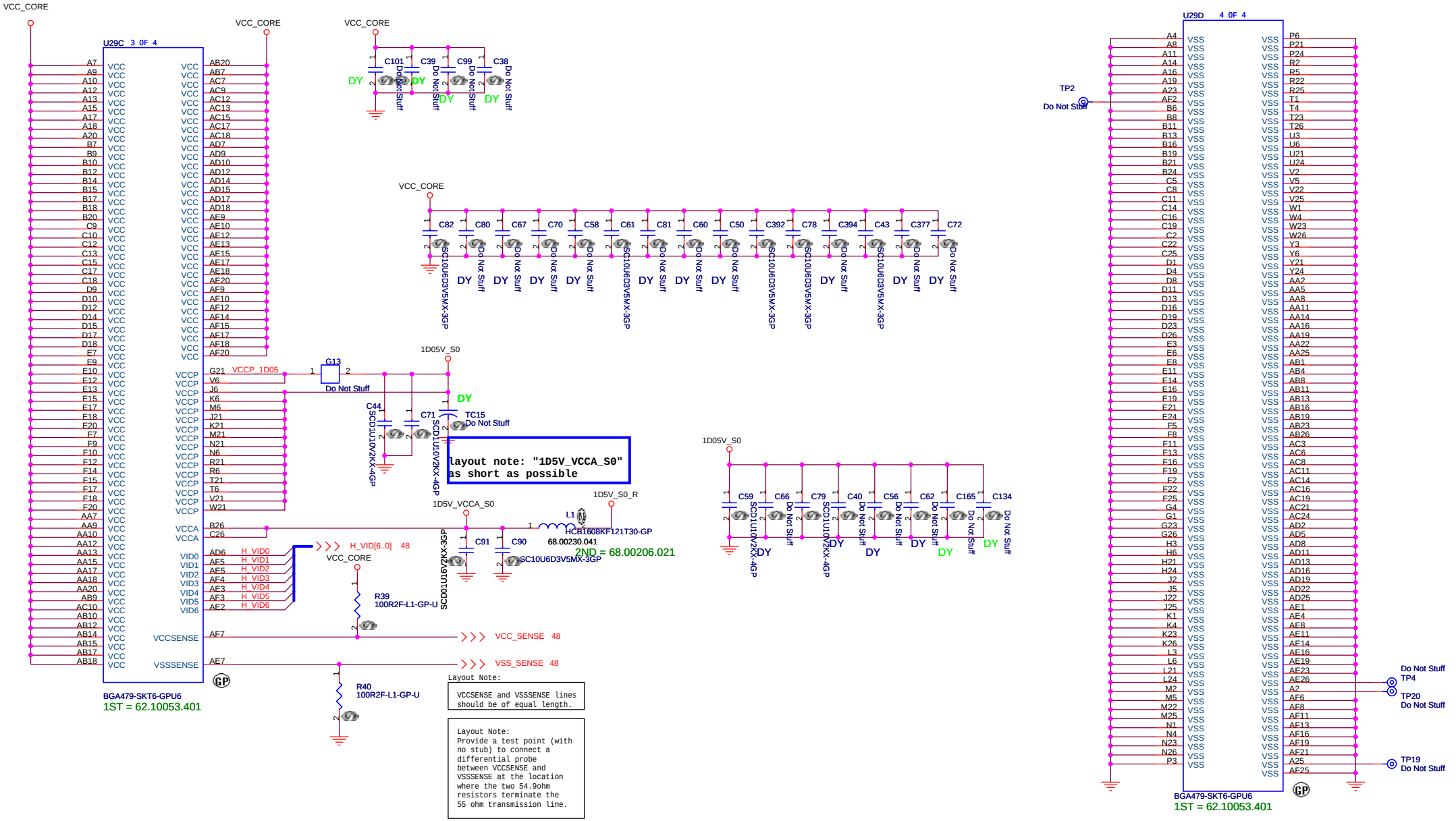

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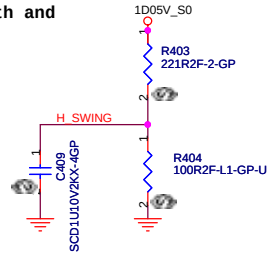
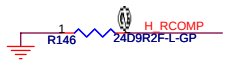
H_SWING routing Trace width and Spacing use 10 / 20 mil

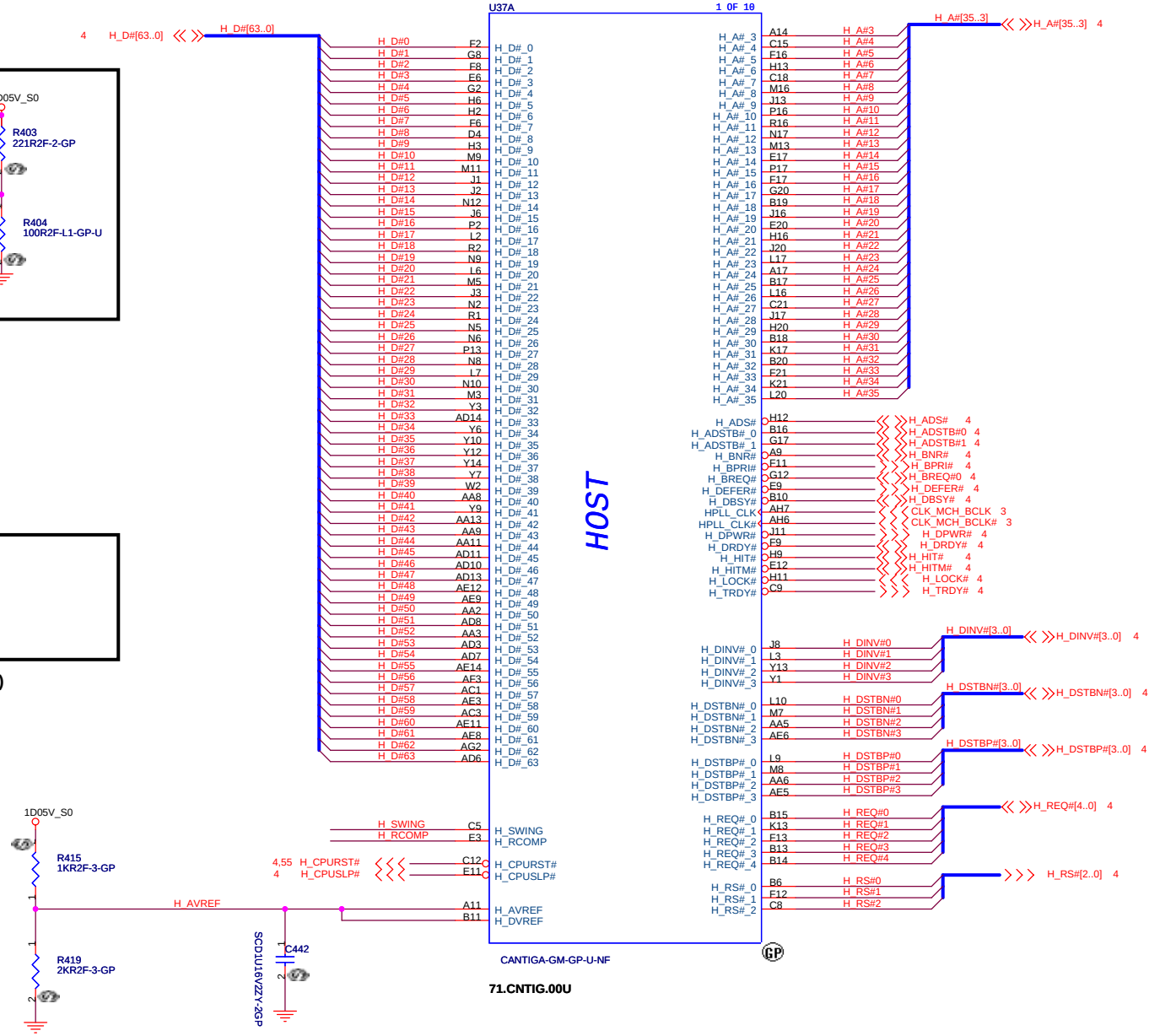
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



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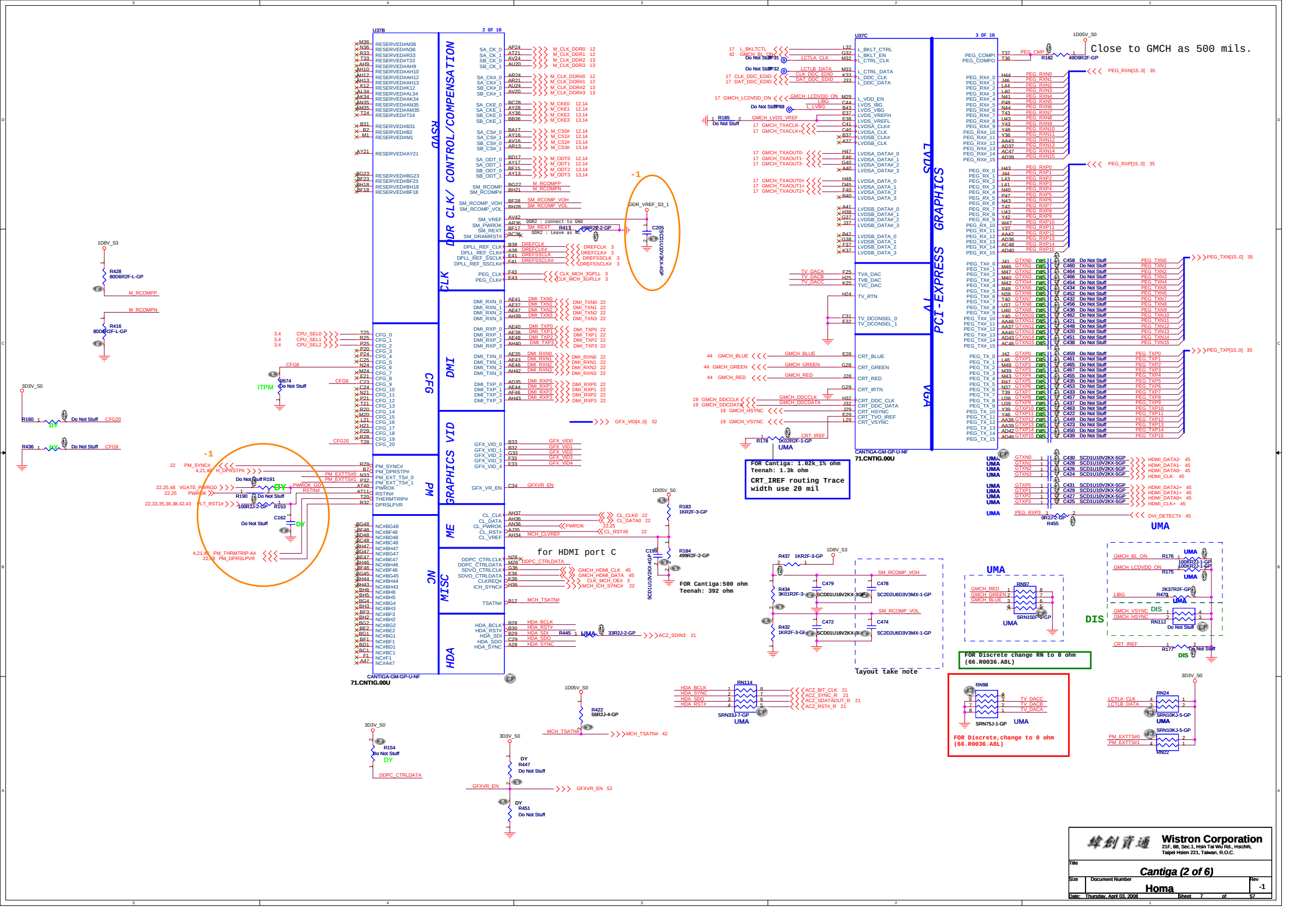
Close to GMCH as 500 mils.
U37B
2 OF 10
RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
HDA
U37C
3 OF 10
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
FOR Cantiga: 1.02k_1% ohm
Teenah: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
for HDMI port C
FOR Cantiga:500 ohm
Teenah: 392 ohm
layout take note
FOR Discrete change RN to 0 ohm (66.R0036.A8L)
FOR Discrete,change to 0 ohm (66.R0036.A8L)
UMA
DIS
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Cantiga (2 of 6)
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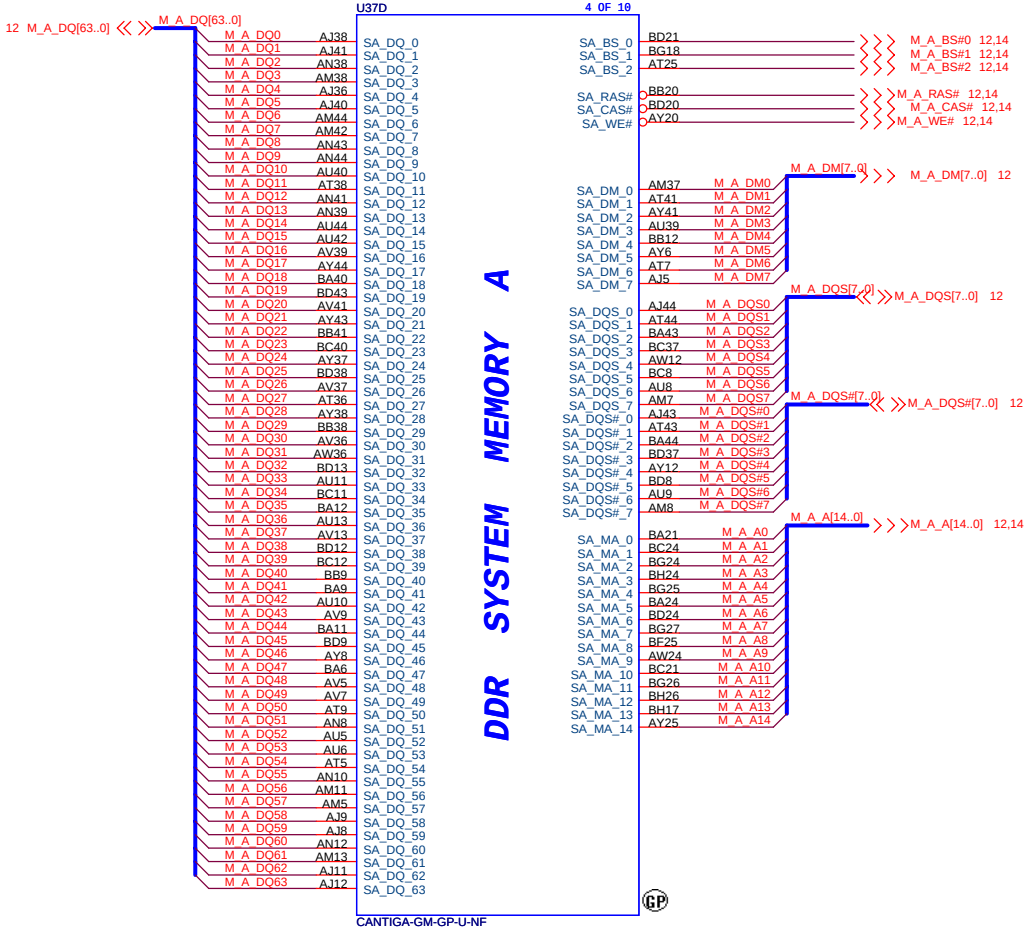

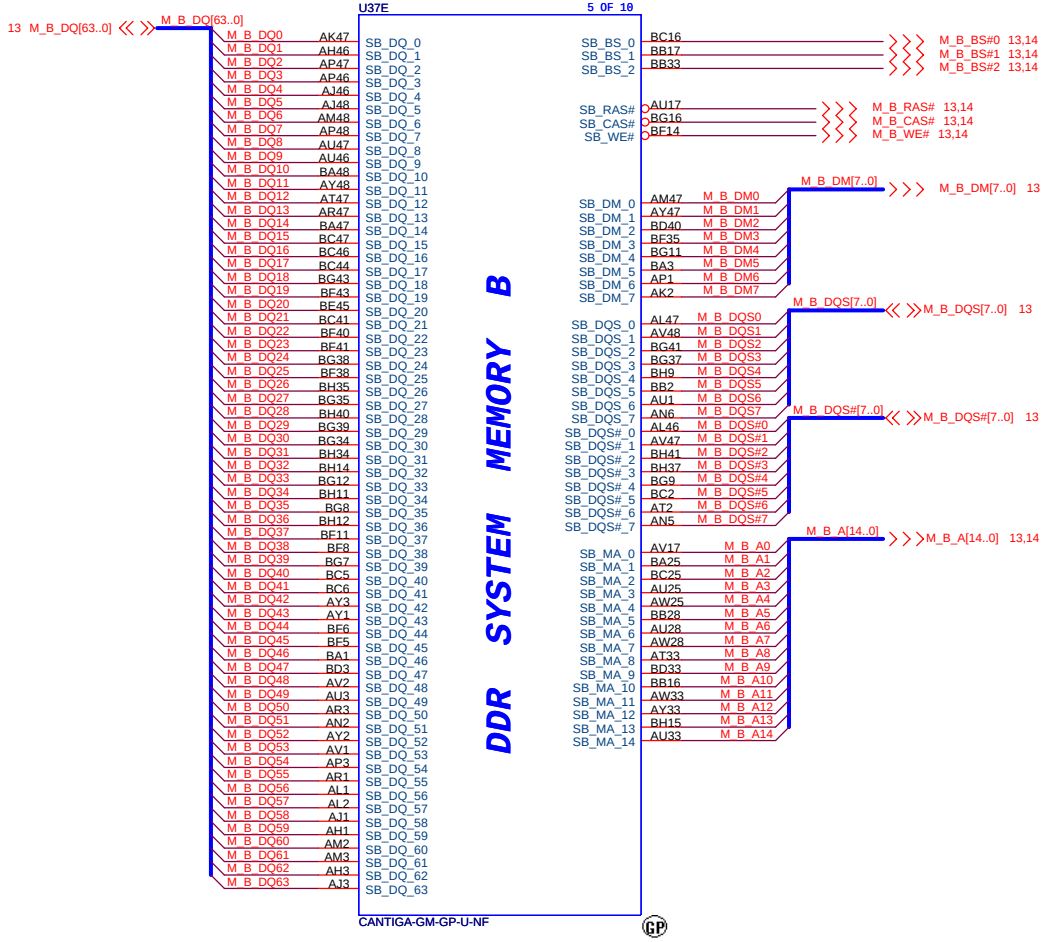

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Title: ***Cantiga (3 of 6)***

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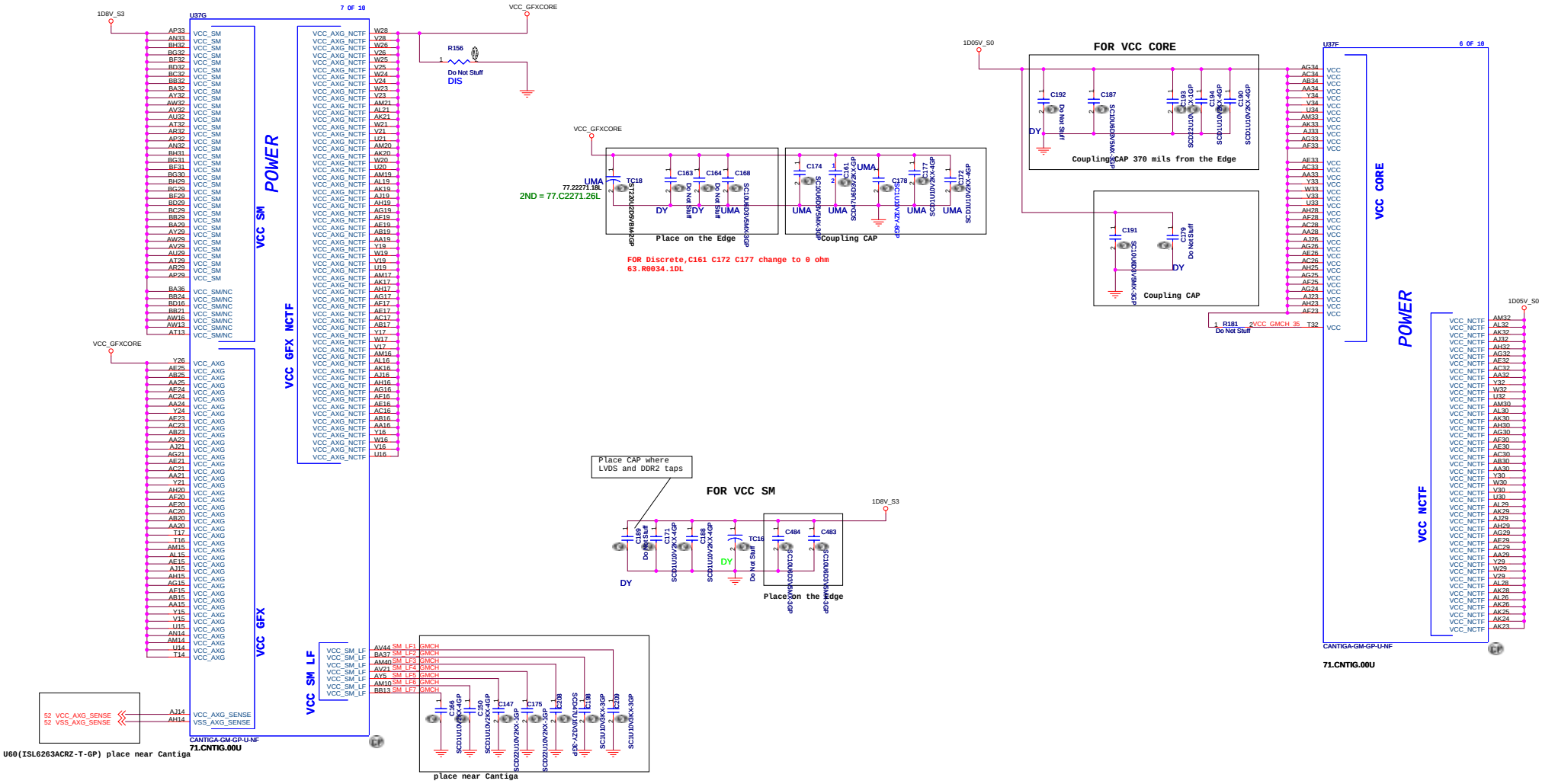
U37G
7 OF 10
VCC SM
POWER
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC_GFXCORE
1D8V_S3
R156
Do Not Stuff
DIS
FOR VCC CORE
1D05V_S0
Coupling CAP 370 mils from the Edge
Coupling CAP
U37F
6 OF 10
VCC CORE
POWER
VCC NCTF
1D05V_S0
FOR Discrete,C161 C172 C177 change to 0 ohm
63.R0634.1DL
2ND = 77.C2271.26L
Place on the Edge
Coupling CAP
Place CAP where
LVDS and DDR2 taps
FOR VCC SM
Place on the Edge
place near Cantiga
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
U60(ISL6263ACRZ-T-GP) place near Cantiga
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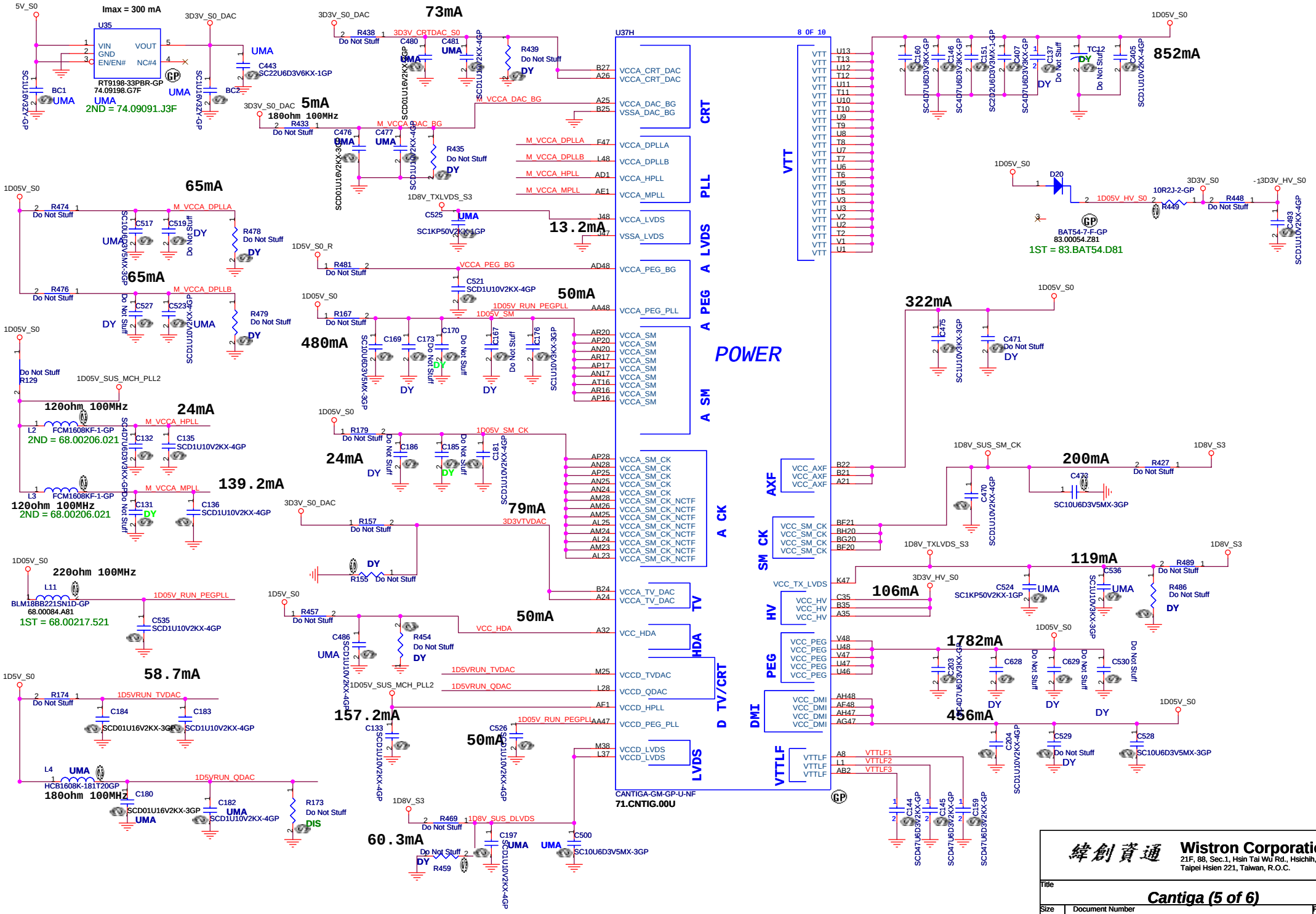
POWER
U37H
CANTIGA-GM-GP-U-NF
71.CNTIG.00U
8 OF 10
CRT
PLL
A LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
73mA
5mA
65mA
65mA
13.2mA
50mA
480mA
24mA
139.2mA
79mA
50mA
157.2mA
50mA
60.3mA
322mA
200mA
119mA
106mA
1782mA
456mA
852mA
58.7mA
24mA
Imax = 300 mA
RT9198-33PBR-GP
74.09198.G7F
2ND = 74.09091.J3F
180ohm 100MHz
120ohm 100MHz
2ND = 68.00206.021
220ohm 100MHz
68.00084.A81
1ST = 68.00217.521
HCB1608K-181T20GP
BAT54-7-F-GP
83.00054.Z81
1ST = 83.BAT54.D81
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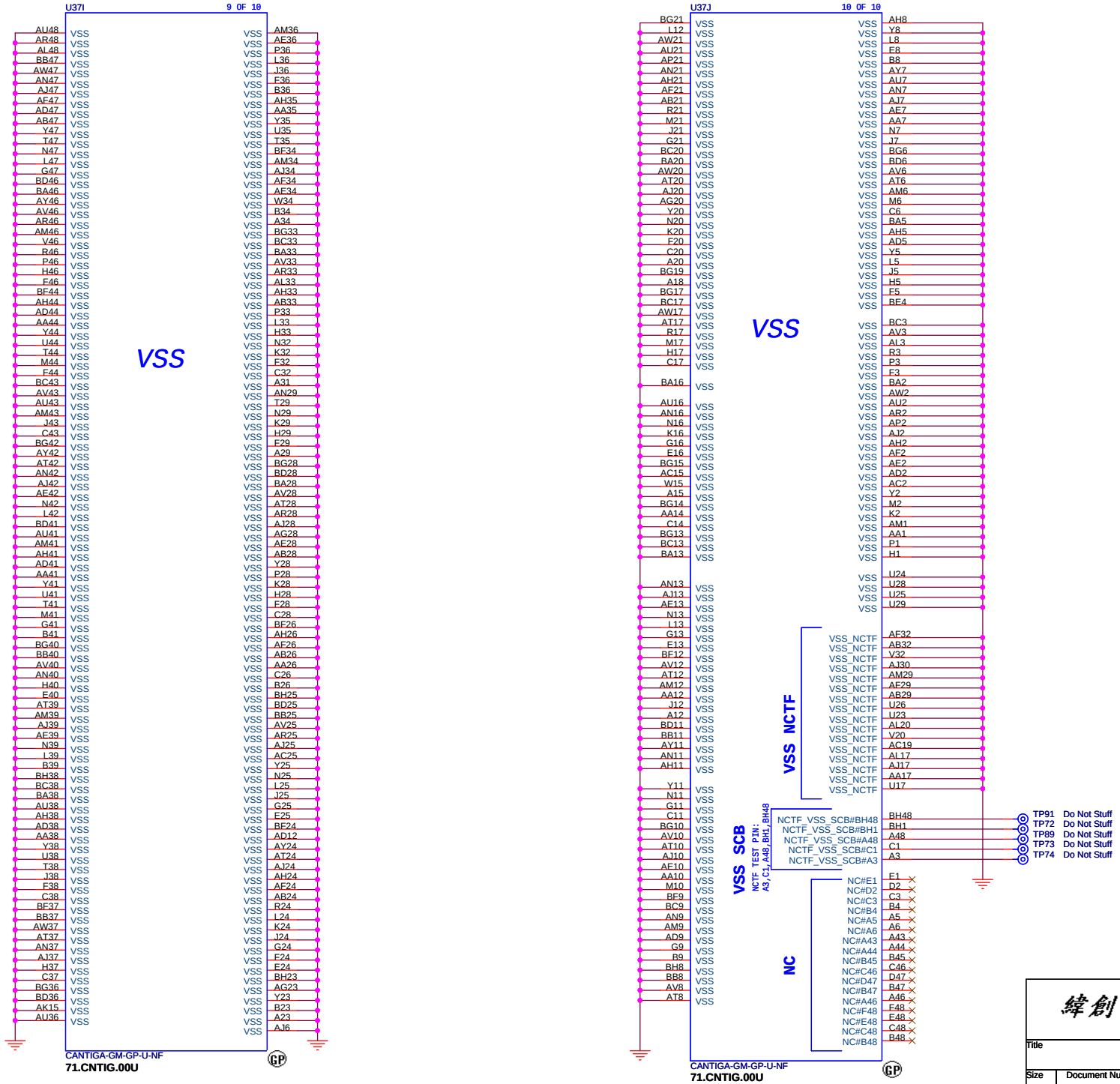

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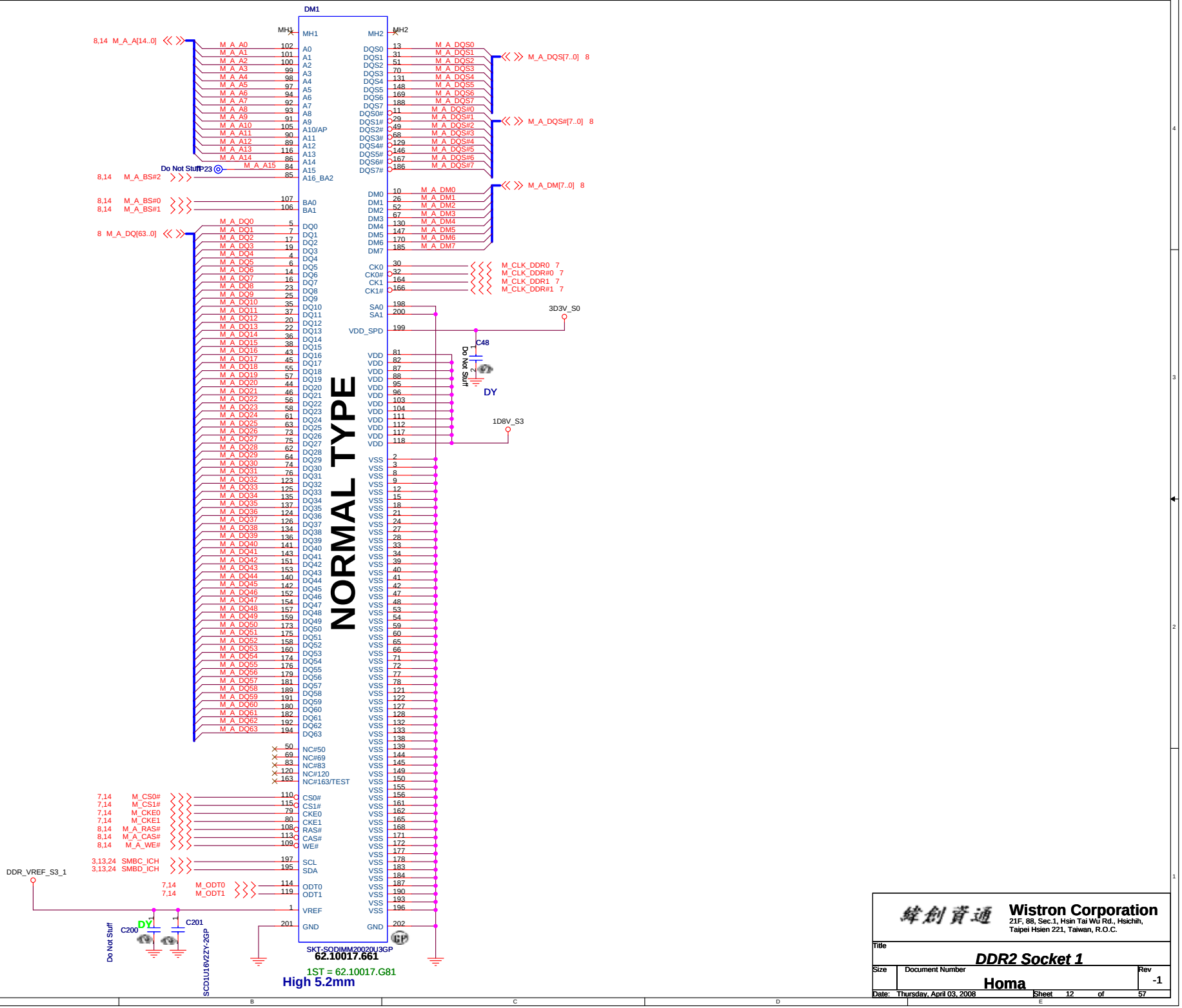
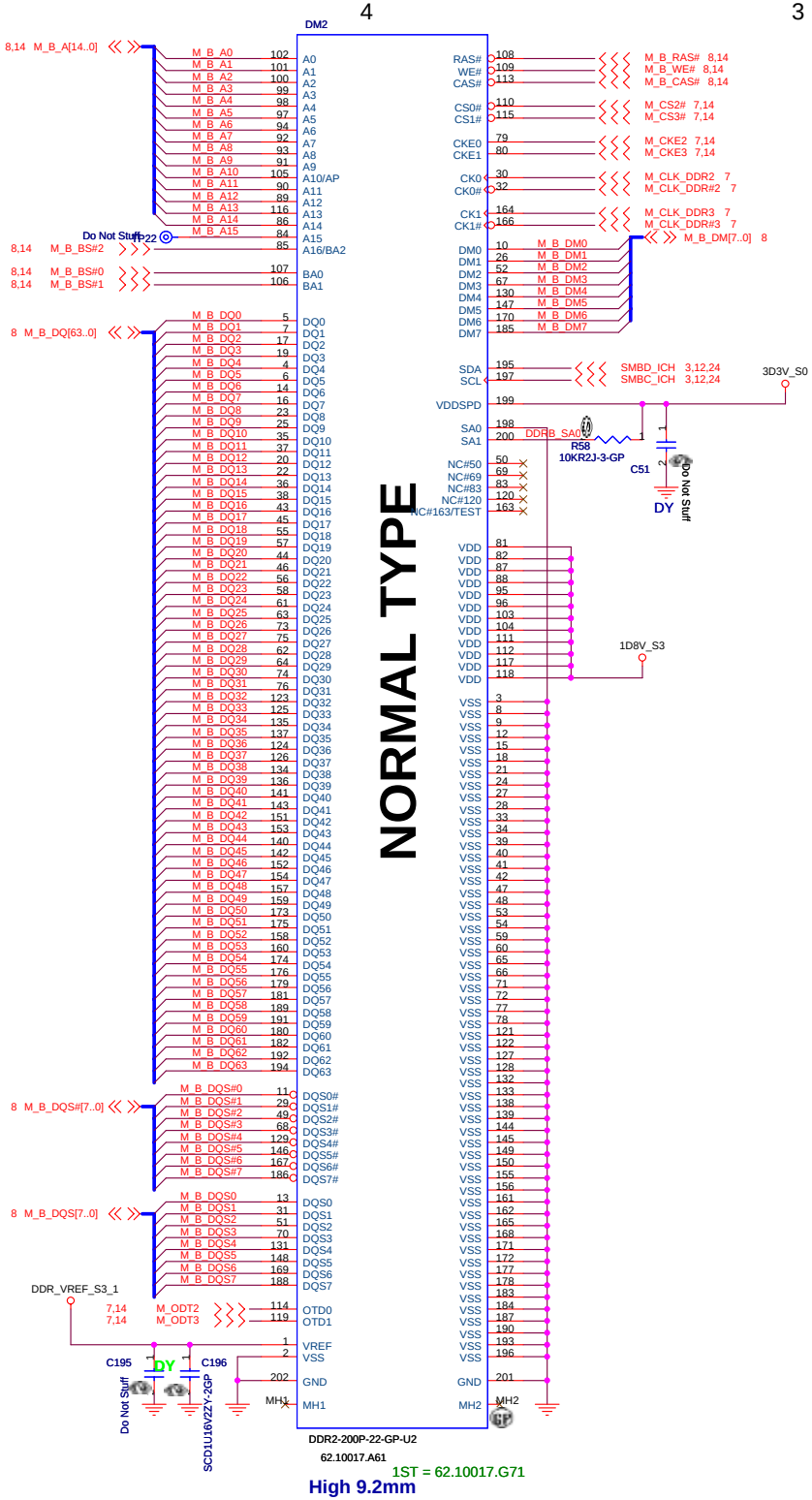
Title: ***Cantiga (6 of 6)***

Size	Document Number	Rev
	Homa	-1

Date: Thursday, April 03, 2008 Sheet 11 of 57



Company	Wistron Corporation
Address	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR2 Socket 1
Size	
Document Number	Homa
Rev	-1
Date	Thursday, April 03, 2008
Sheet	12 of 57



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	DDR2 Socket 2
Size	Document Number: Homa
Rev	-1
Date: Thursday, April 03, 2008	Sheet 13 of 57

PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S3

RN15 SRN56J-5-GP — M_A_A12 — M_CKE0 7,12

RN12 SRN56J-5-GP — M_B_A9, M_B_A8, M_B_A5 — M_B_BS#1 8,13

RN14 SRN56J-5-GP — M_B_A12 — M_B_BS#2 8,13; M_CKE2 7,13

RN8 SRN56J-5-GP — M_B_A10, M_B_A1, M_B_A3 — M_B_BS#0 8,13

RN3 SRN56J-5-GP — M_B_A13 — M_ODT2 7,13; M_CS2# 7,13

RN6 SRN56J-5-GP — M_B_A0, M_B_A2, M_B_A4 — M_B_RAS# 8,13

RN10 SRN56J-5-GP — M_B_A14, M_B_A11, M_B_A7, M_B_A6

RN5 SRN56J-5-GP — M_B_WE# 8,13; M_B_CAS# 8,13; M_ODT3 7,13; M_CS3# 7,13

R140 56R2J-4-GP — M_CKE1 7,12

R139 56R2J-4-GP — M_CKE3 7,13

RN4 SRN56J-5-GP — M_A_A13 — M_CS0# 7,12; M_ODT0 7,12; M_A_RAS# 8,12

RN7 SRN56J-5-GP — M_A_A4, M_A_A2, M_A_A0 — M_A_BS#1 8,12

RN2 SRN56J-5-GP — M_A_WE# 8,12; M_A_CAS# 8,12; M_CS1# 7,12; M_ODT1 7,12

RN13 SRN56J-5-GP — M_A_A8, M_A_A9, M_A_A3 — M_A_BS#2 8,12

RN11 SRN56J-5-GP — M_A_A6, M_A_A11, M_A_A7, M_A_A14

RN9 SRN56J-5-GP — M_A_A5, M_A_A1, M_A_A10 — M_A_BS#0 8,12

M_A_A[14..0] — M_A_A[14..0] 8,12

M_B_A[14..0] — M_B_A[14..0] 8,13

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

DDR_VREF_S3

C139 SCD1U16V2ZY-2GP — C127 Do Not Stuff DY — C117 SCD1U16V2ZY-2GP — C148 SCD1U16V2ZY-2GP — C107 SCD1U16V2ZY-2GP — C126 SCD1U16V2ZY-2GP — C138 SCD1U16V2ZY-2GP — C103 Do Not Stuff DY — C106 Do Not Stuff DY — C149 Do Not Stuff DY — C116 SCD1U16V2ZY-2GP

C140 SCD1U16V2ZY-2GP — C158 Do Not Stuff DY — C124 Do Not Stuff DY — C115 SCD1U16V2ZY-2GP — C141 SCD1U16V2ZY-2GP — C104 Do Not Stuff DY — C155 Do Not Stuff DY — C118 SCD1U16V2ZY-2GP — C129 Do Not Stuff DY — C128 Do Not Stuff DY — C108 Do Not Stuff DY

Place these Caps near DM1

1D8V_S3

C404 Do Not Stuff DY — C406 Do Not Stuff DY — C386 SC2D2U6D3V3MX-1-GP — C395 Do Not Stuff DY — C413 SC2D2U6D3V3MX-1-GP

C398 Do Not Stuff DY — C401 Do Not Stuff DY — C397 Do Not Stuff DY — C411 Do Not Stuff DY

Place these Caps near DM2

1D8V_S3

C399 SC2D2U6D3V3MX-1-GP — C387 SC2D2U6D3V3MX-1-GP — C412 SC2D2U6D3V3MX-1-GP — C396 Do Not Stuff DY — C400 SC2D2U6D3V3MX-1-GP

C388 Do Not Stuff DY — C408 Do Not Stuff DY — C403 Do Not Stuff DY — C393 Do Not Stuff DY

緯創資通 **Wistron Corporation**
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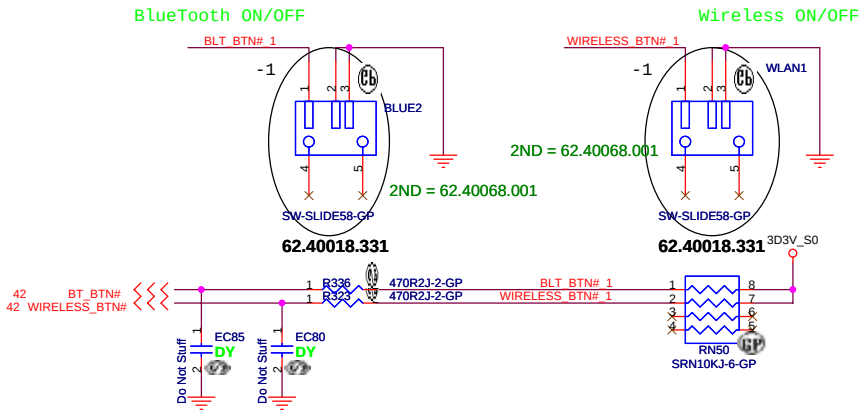
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***DDR2 Termination Resistor***

Size | Document Number: **Homa** | Rev: -1

Date: Thursday, April 03, 2008 | Sheet 14 of 57



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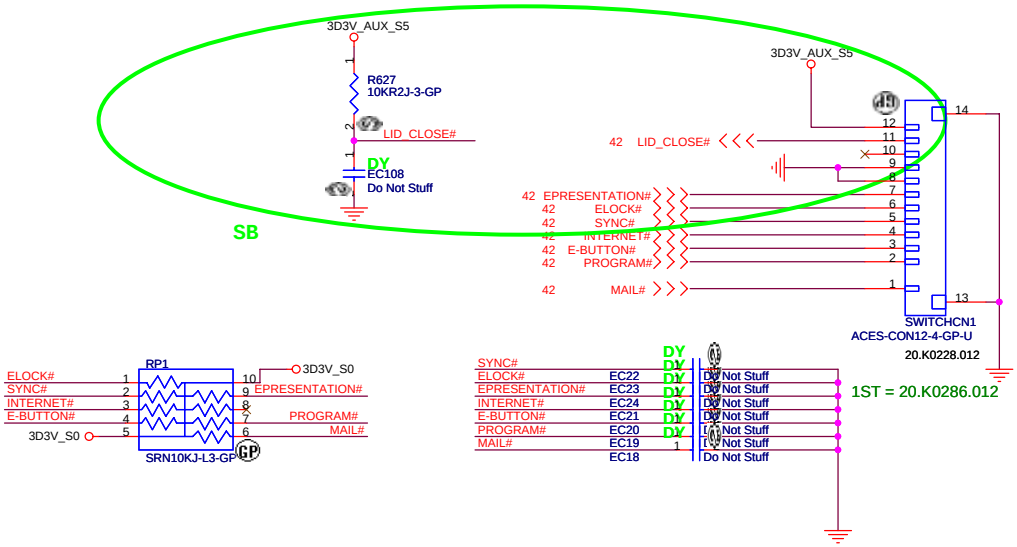
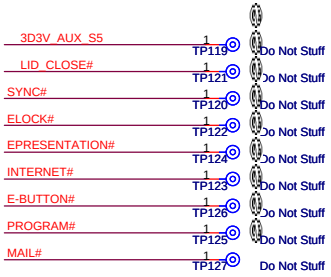
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SWITCH***

Size	Document Number	Rev
	Homa	-1

Date: Thursday, April 03, 2008 Sheet 15 of 57





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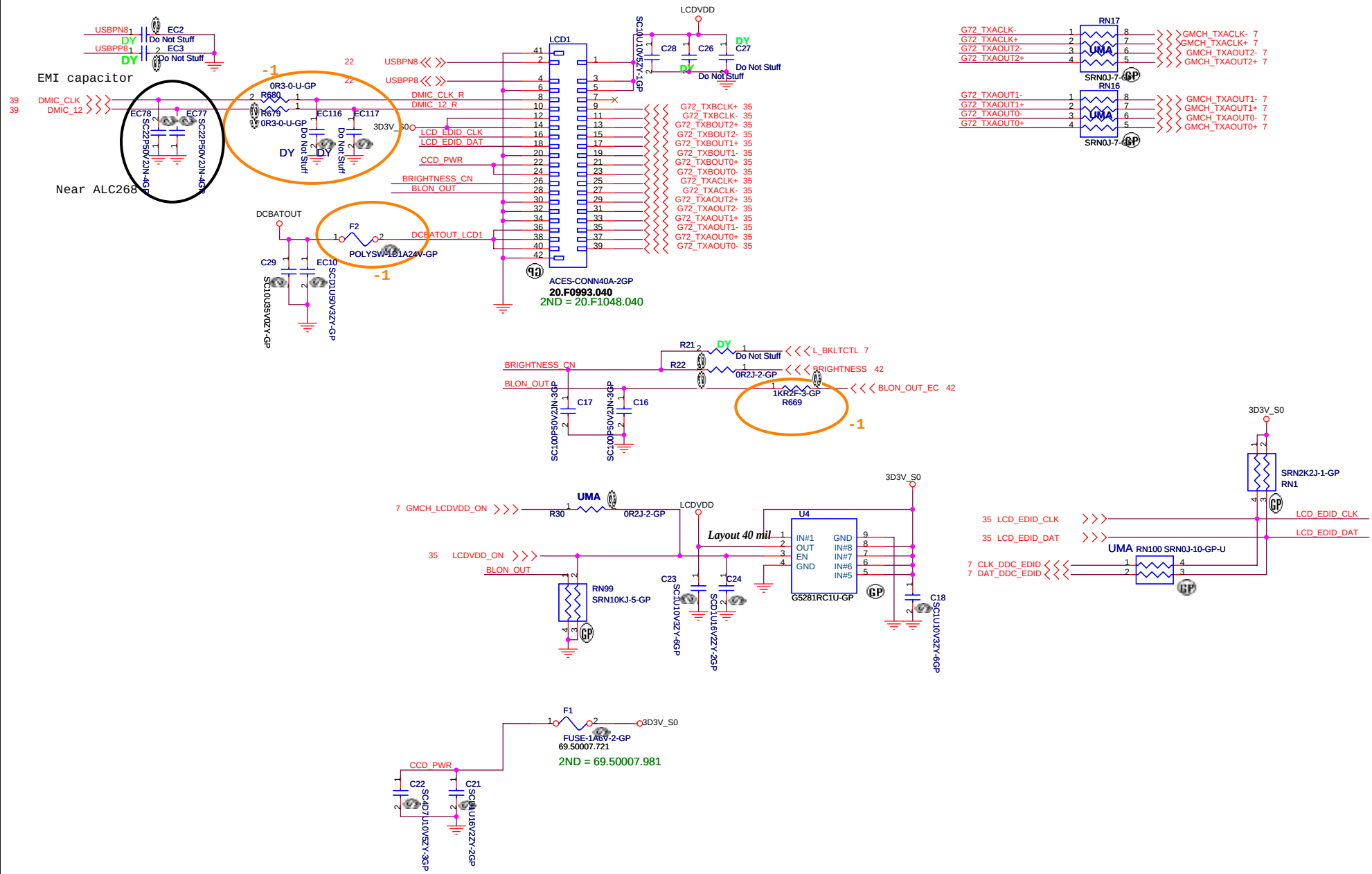
Title	***LAUNCH***	
Size	Document Number **Homa**	Rev -1
Date: Thursday, April 03, 2008	Sheet 16 of 57	

LCD/INVERTER/CCD CONN



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	LCD CONN	
Size	Document Number: Homa	Rev: -1
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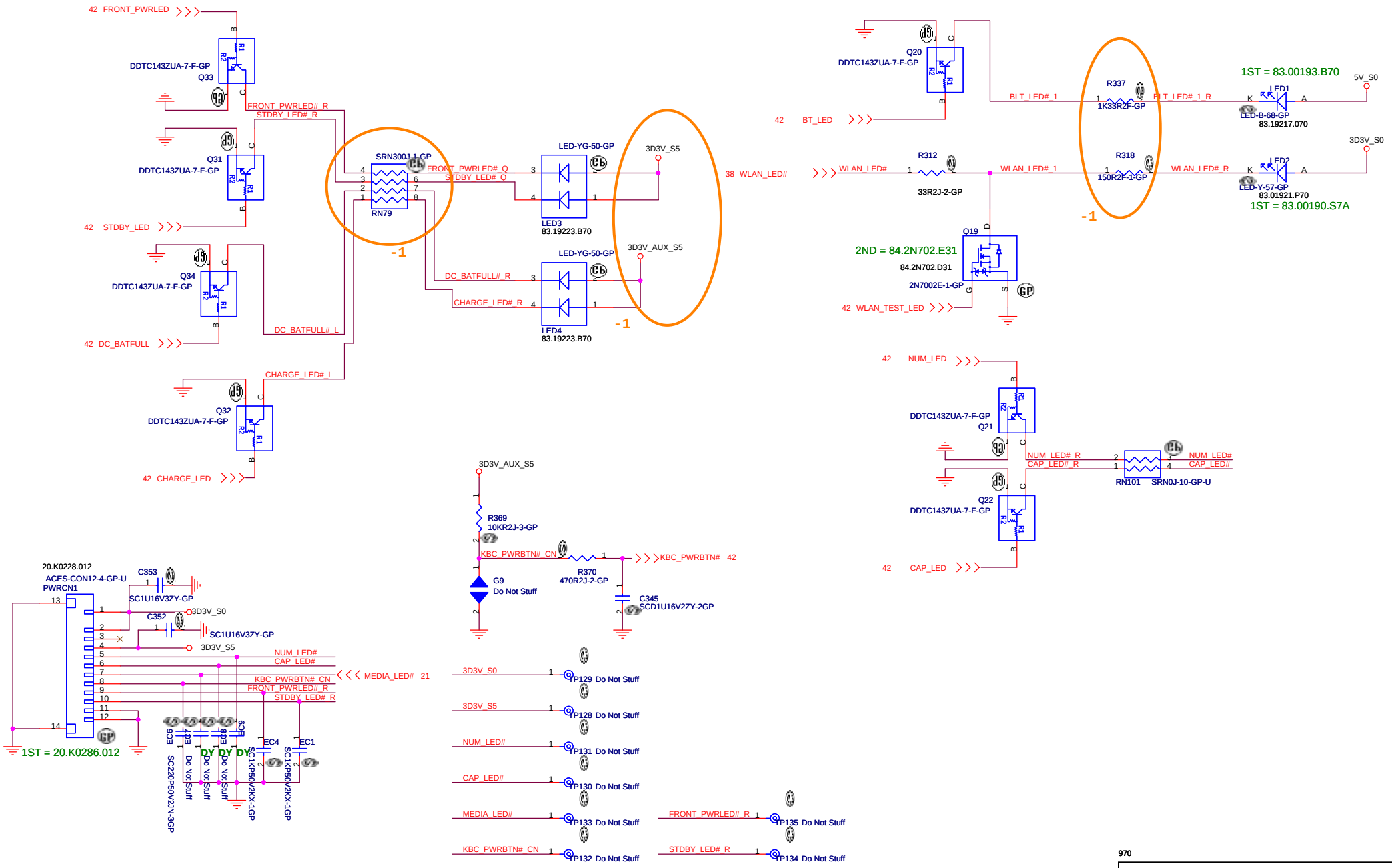
LED



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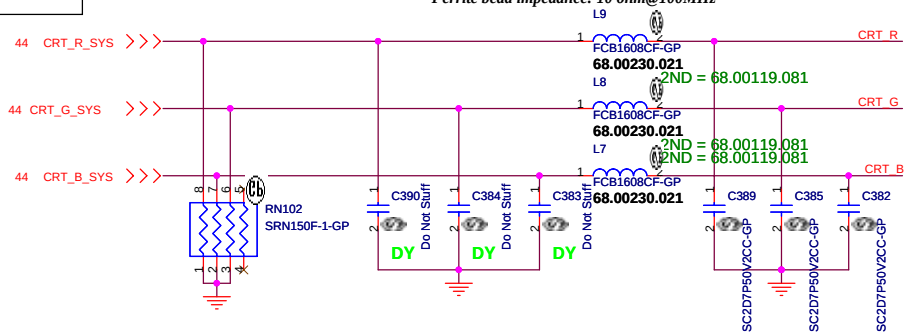
Title	***LED***	
Size	Document Number **Homa**	Rev -1
Date: Thursday, April 03, 2008	Sheet 18 of 57	

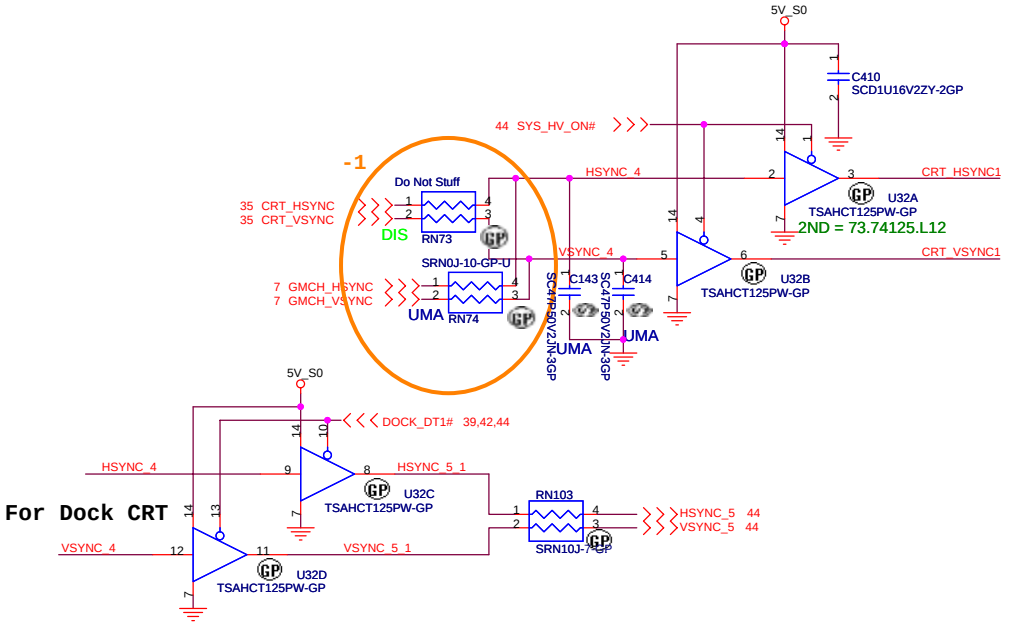
Layout Note:
Place these resistors close to the CRT-out connector

Ferrite bead impedance: 10 ohm@100MHz

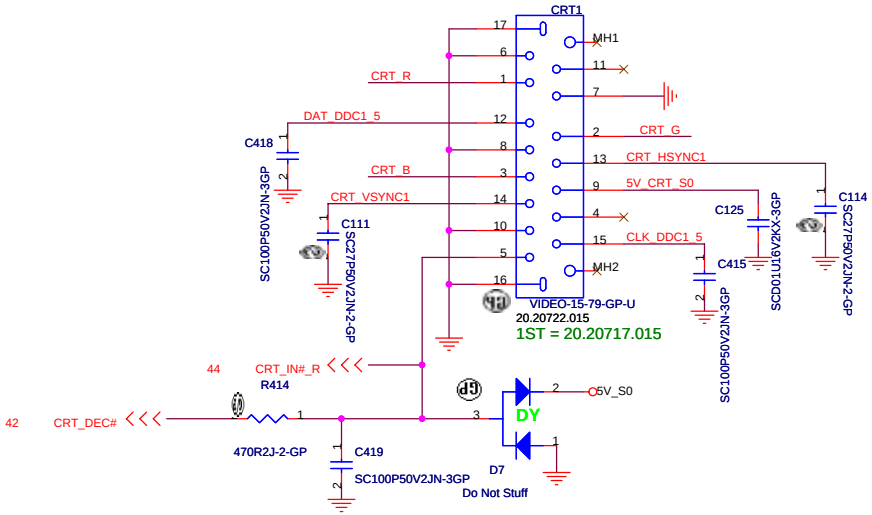


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

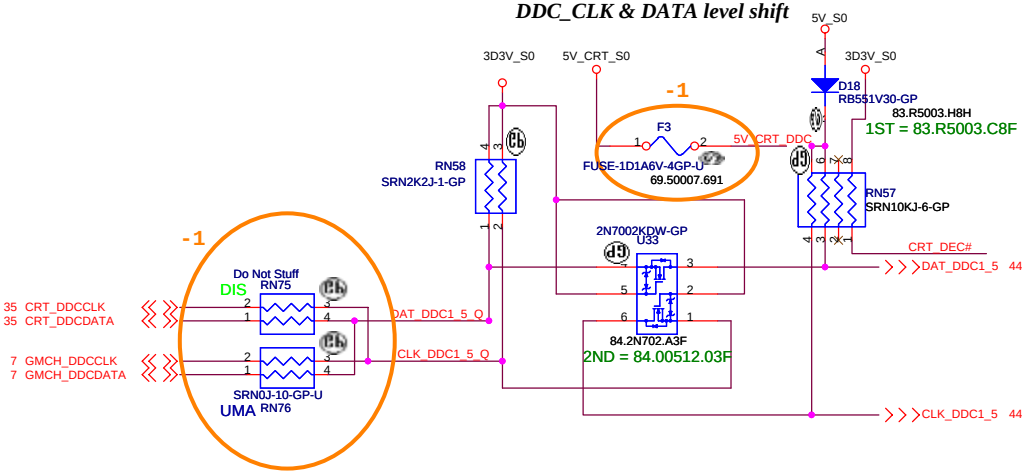
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



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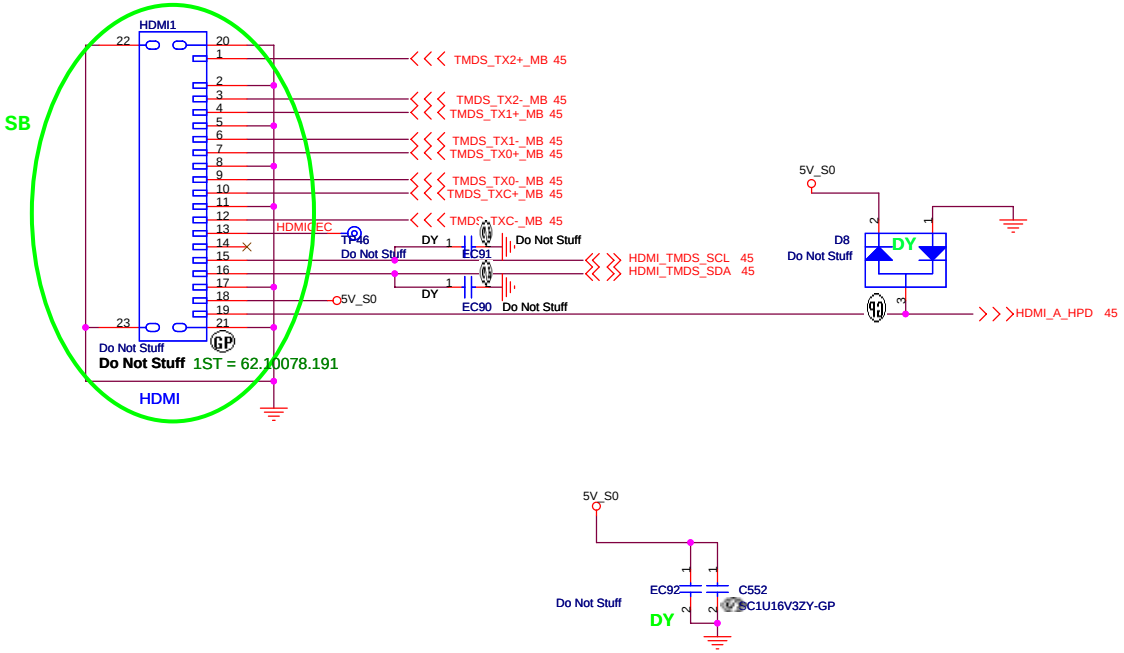
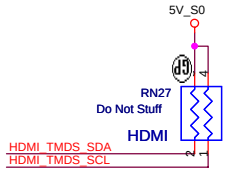
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT Connector***	
Size	Document Number **Homa**	Rev -1
Date: Thursday, April 03, 2008	Sheet 19 of 57	





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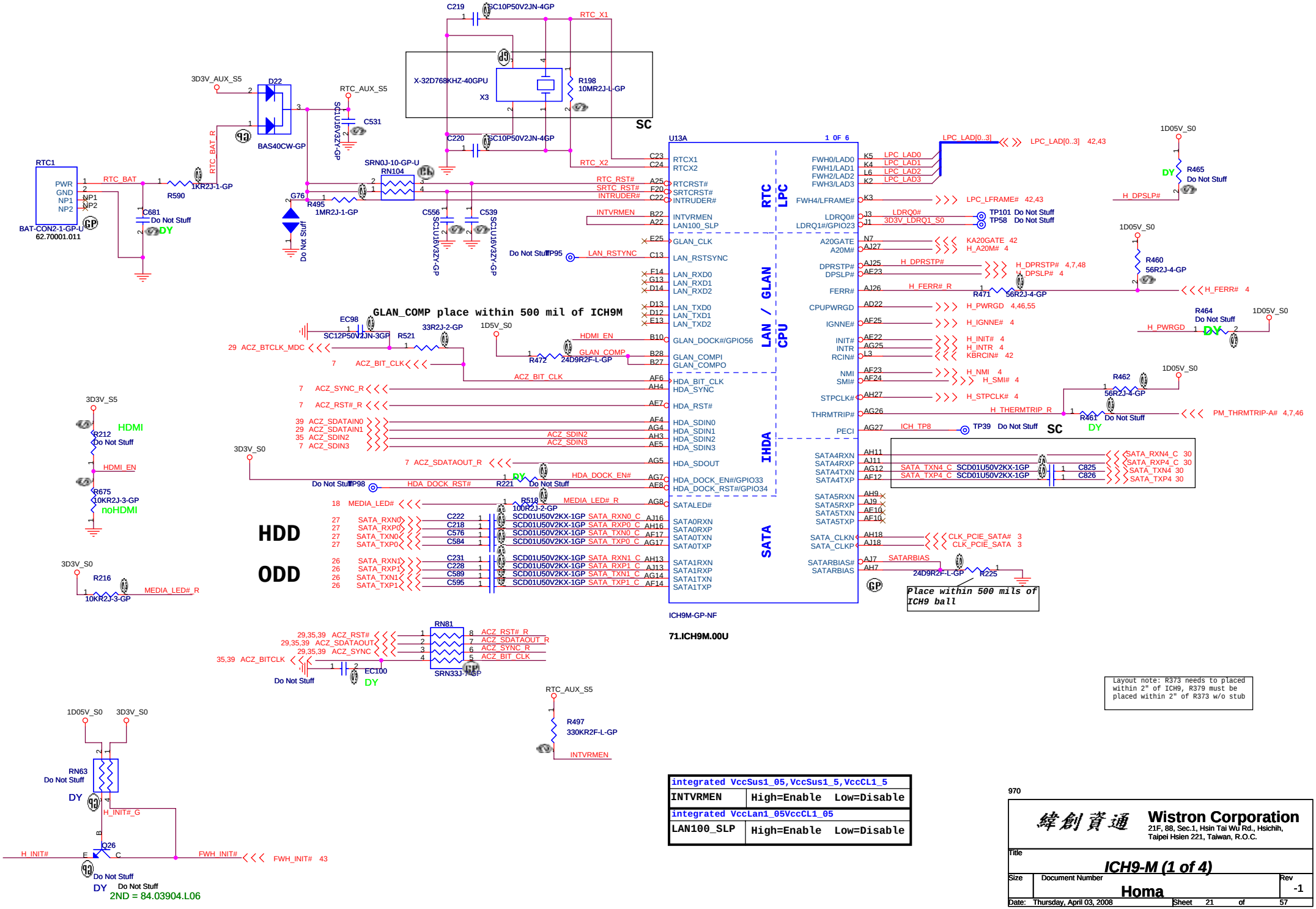
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: HDMI CONNECTOR		
Size: A3	Document Number: Homa	Rev: -1
Date: Thursday, April 03, 2008	Sheet 20 of 57	


RTC1
BAT-CON2-1-GP-U
62.70001.011
RTC_BAT
1KR2J-1-GP
R590
C681
Do Not Stuff
DY
RTC_BAT_R
D22
BAS40CW-GP
3D3V_AUX_S5
RTC_AUX_S5
SCD1U16V2Z2Y-GP
C531
C219
SC10P50V2JN-4GP
X-32D768KHZ-40GPU
X3
R198
10MR2J-L-GP
C220
SC10P50V2JN-4GP
RTC_X1
RTC_X2
SRN0J-10-GP-U
RN104
RTC_RST#
SRTC_RST#
INTRUDER#
INTVRMEN
LAN_RSTSYNC
R495
1MR2J-1-GP
G76
C556
C539
SCD1U16V3Z2Y-GP
Do Not Stuff
TP95
SC
U13A
1 OF 6
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M-GP-NF
71.ICH9M.00U
LPC_LAD[0..3]
LPC_LFRAME#
TP101 Do Not Stuff
TP58 Do Not Stuff
3D3V_LDRQ1_S0
KA20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
KBRCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
PM_THRMTRIP-A#
TP39 Do Not Stuff
ICH_TP8
R471
56R2J-4-GP
R460
R462
R461 Do Not Stuff
R464 Do Not Stuff
R465 Do Not Stuff
1D05V_S0
Place within 500 mils of ICH9 ball
GLAN_COMP place within 500 mil of ICH9M
EC98
SC12P50V2JN-3GP
33R2J-2-GP
R521
R472
24D9R2F-L-GP
HDMI_EN
GLAN_COMP
ACZ_BTCLK_MDC
ACZ_BIT_CLK
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_SDIN2
ACZ_SDIN3
ACZ_SDATAOUT_R
HDA_DOCK_EN#
HDA_DOCK_RST#
R221
TP98
MEDIA_LED#
MEDIA_LED#_R
R518
100R2J-2-GP
HDD
ODD
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
SCD01U50V2KX-1GP
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1_C
SATA_TXP1_C
C222
C218
C576
C584
C231
C228
C589
C595
C825
C826
SATA_RXN4_C
SATA_RXP4_C
SATA_TXN4
SATA_TXP4
HDMI
noHDMI
R212
R675
10KR2J-3-GP
R216
RN81
SRN33J-1-GP
EC100
ACZ_RST#
ACZ_SDATAOUT
ACZ_SYNC
ACZ_BITCLK
ACZ_RST#_R
ACZ_SDATAOUT_R
ACZ_SYNC_R
ACZ_BIT_CLK
R497
330KR2F-L-GP
INTVRMEN
RN63
Do Not Stuff
DY
H_INIT#_G
Q26
H_INIT#
FWH_INIT#
FWH_INIT# 43
2ND = 84.03904.L06
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATARBIAS
R225
24D9R2F-L-GP
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN
High=Enable
Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP
High=Enable
Low=Disable
970
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (1 of 4)
Size
Document Number
Homa
Rev
-1
Date: Thursday, April 03, 2008
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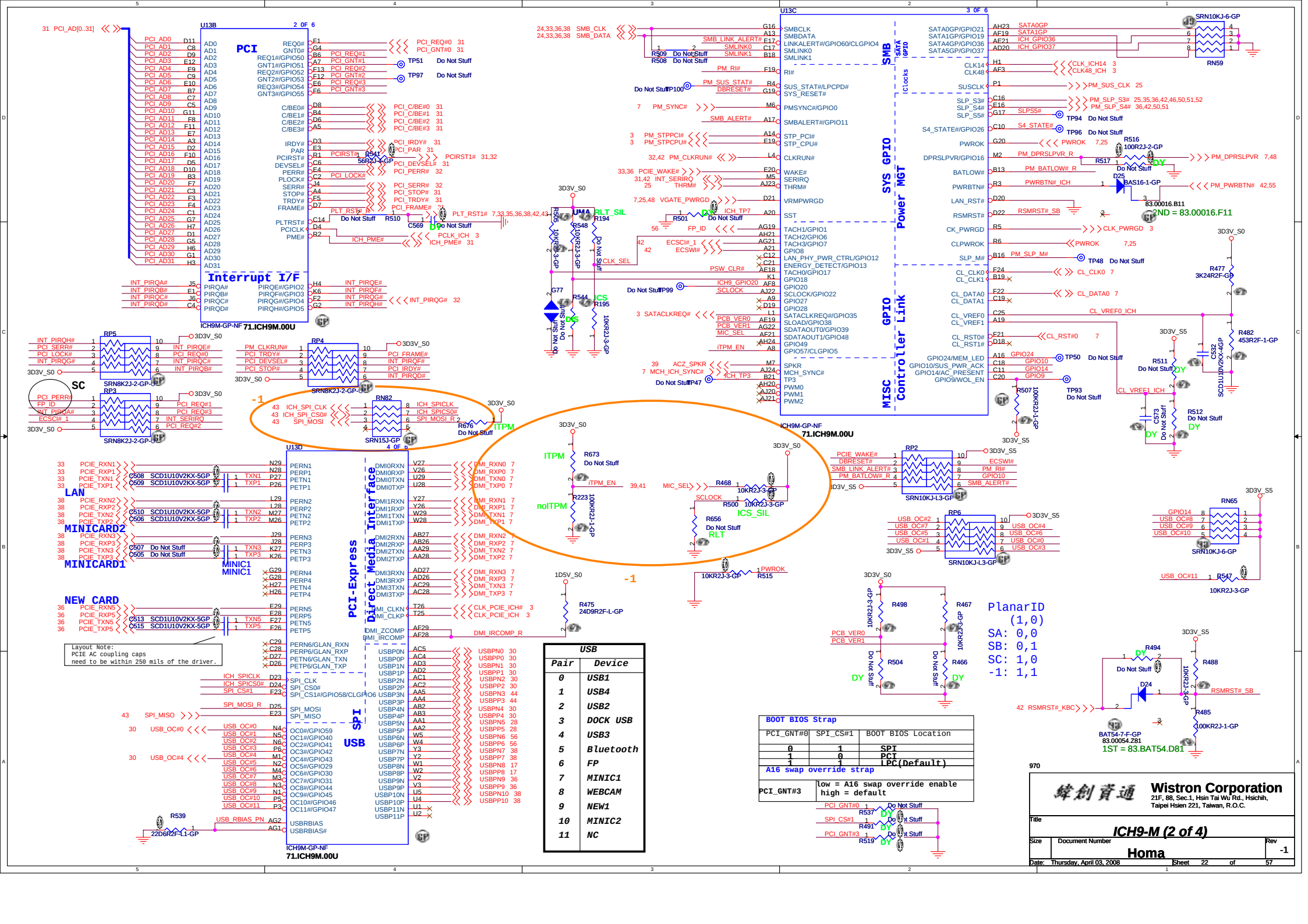
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMB
SATA GPIO
Clocks
LAN
MINICARD2
MINICARD1
NEW CARD
PCI-Express
Direct Media Interface
SPI
USB
SC
ITPM
noITPM
ICS_SIL
RLT_SIL
RLT
PlanarID
(1,0)
SA: 0,0
SB: 0,1
SC: 1,0
-1: 1,1
USB
Pair
Device
0
USB1
1
USB4
2
USB2
3
DOCK USB
4
USB3
5
Bluetooth
6
FP
7
MINIC1
8
WEBCAM
9
NEW1
10
MINIC2
11
NC
BOOT BIOS Strap
PCI_GNT#0
SPI_CS#1
BOOT BIOS Location
SPI
PCI
LPC(Default)
A16 swap override strap
PCI_GNT#3
low = A16 swap override enable
high = default
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (2 of 4)
Size
Document Number
Homa
Rev
-1
Date: Thursday, April 03, 2008
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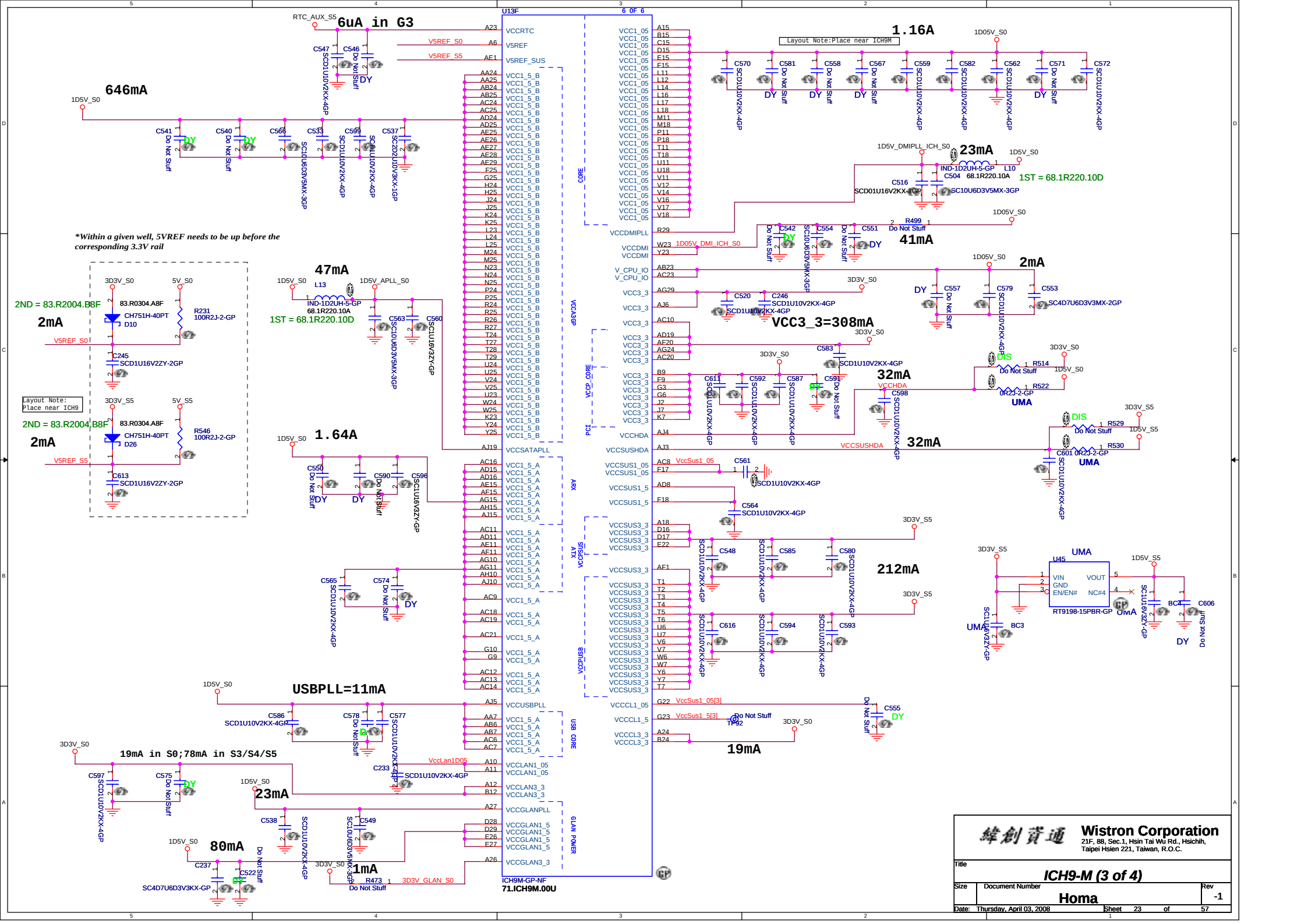
6uA in G3
646mA
1.16A
23mA
41mA
2mA
47mA
1.64A
VCC3_3=308mA
32mA
212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
2ND = 83.R2004.B8F
2mA
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
1ST = 68.1R220.10D
U13F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ICH9-M (3 of 4)
Homa
Rev -1
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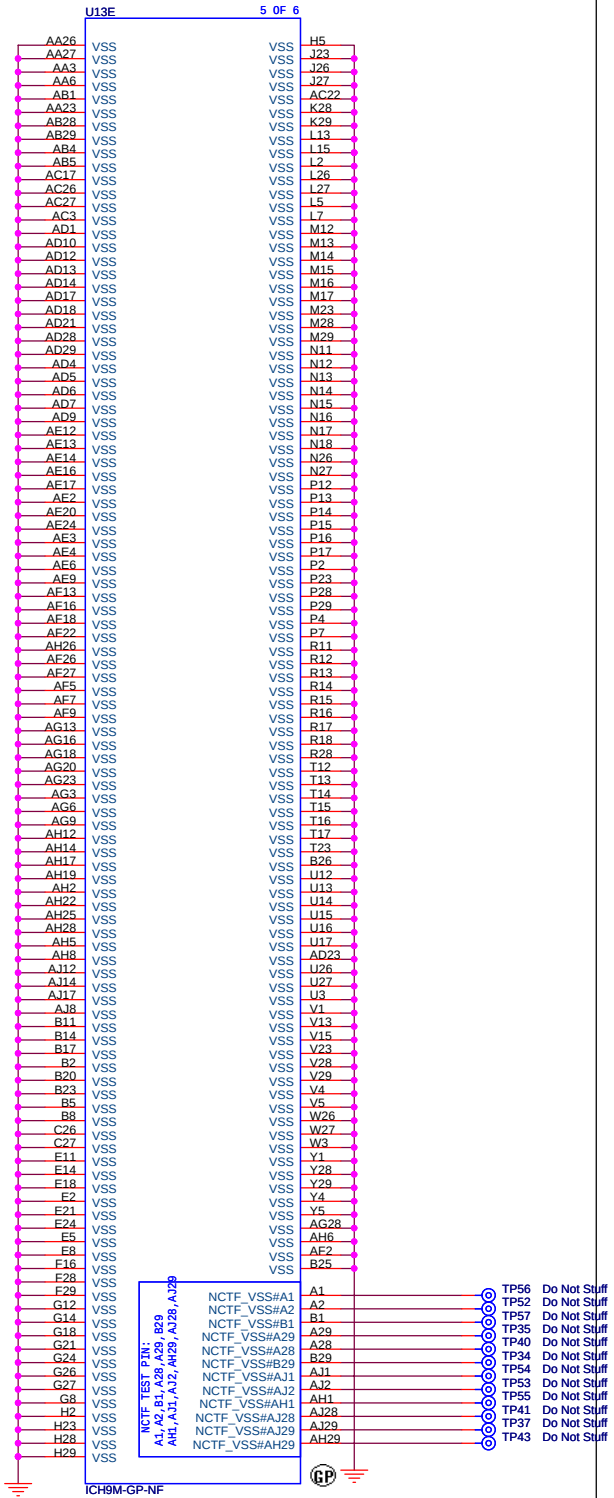

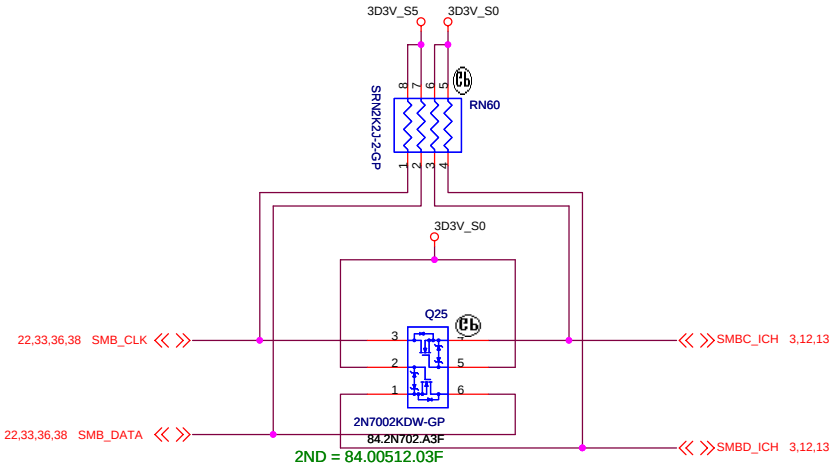

Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ICH9-M (4 of 4)	
Size	Document Number: Homa	Rev: -1
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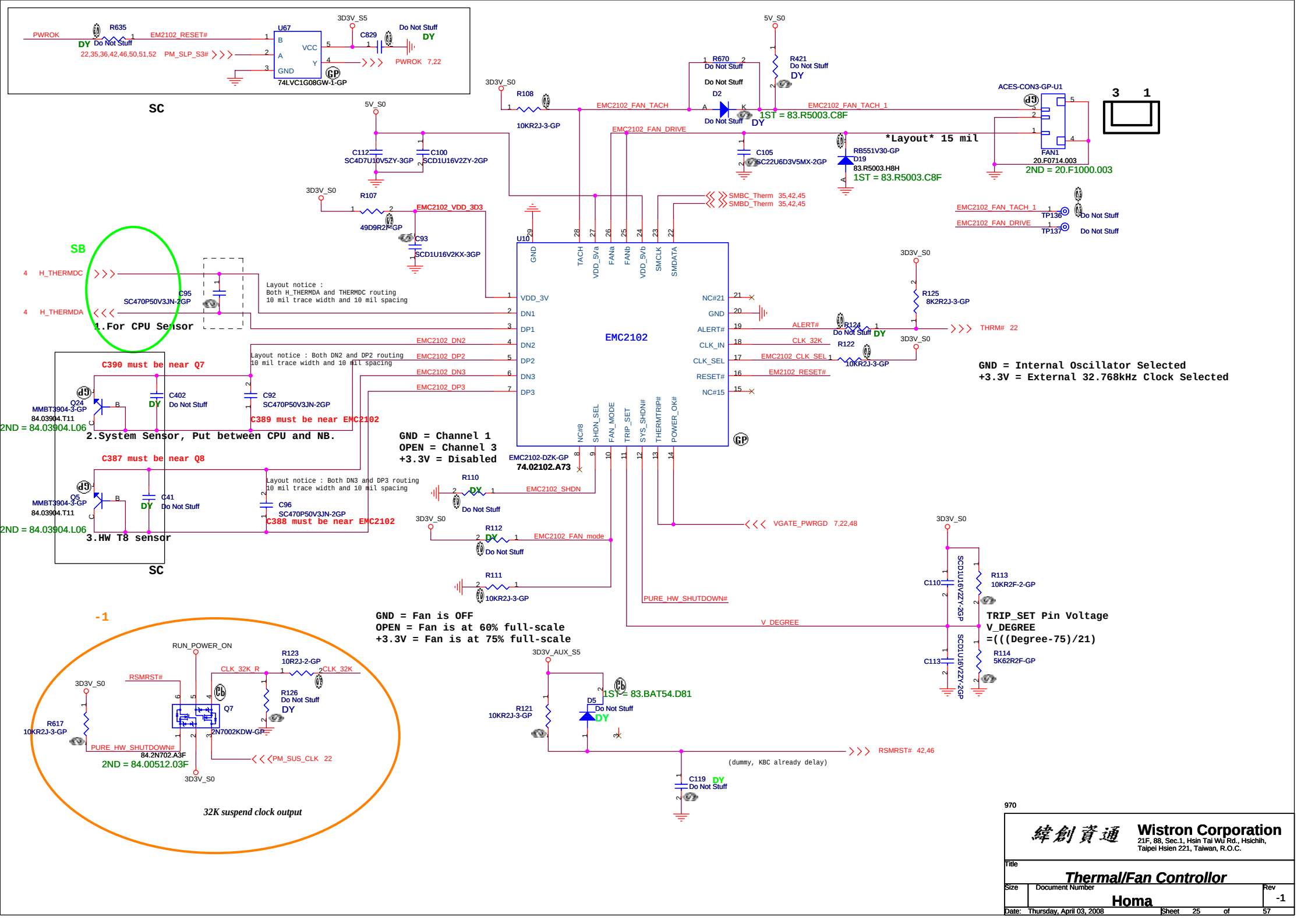

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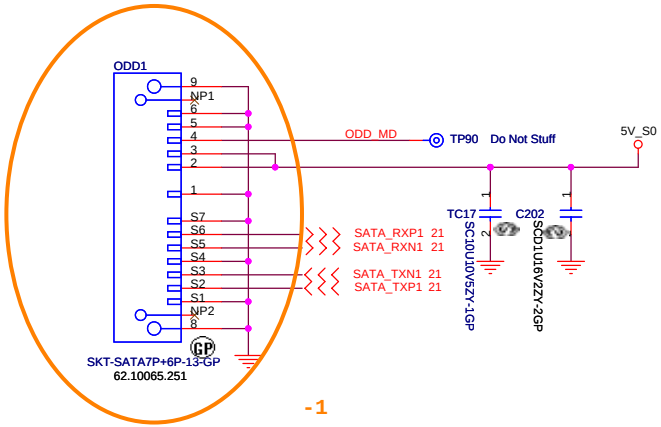
緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	***Thermal/Fan Controllor***	
Size	Document Number: **Homa**	Rev: -1
Date: Thursday, April 03, 2008	Sheet 25 of 57	

ODD Connector



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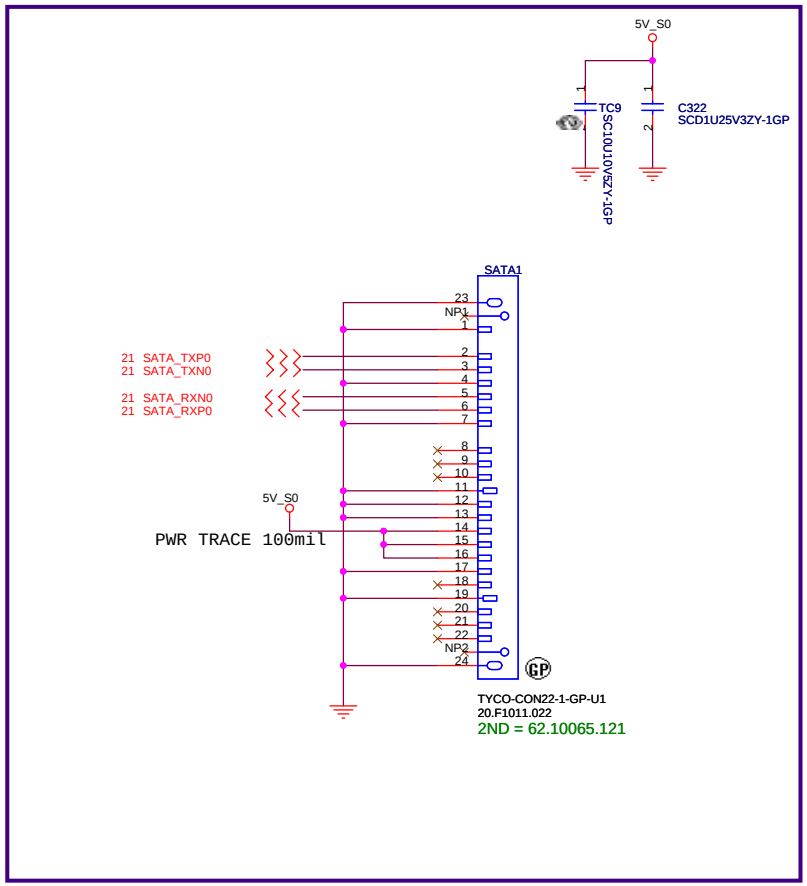
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CDROM		
Size	Document Number: Homa	Rev: -1
Date: Thursday, April 03, 2008	Sheet 26 of 57	

SATA Connector



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD		
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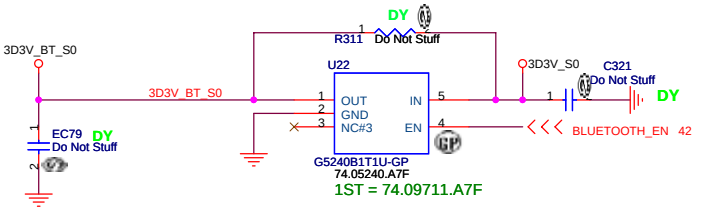
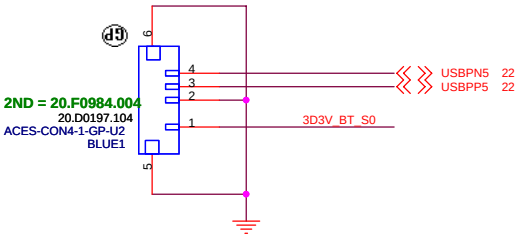
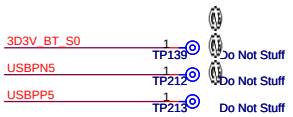
BLUETOOTH MODULE



EC21 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request





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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***BLUETOOTH***	
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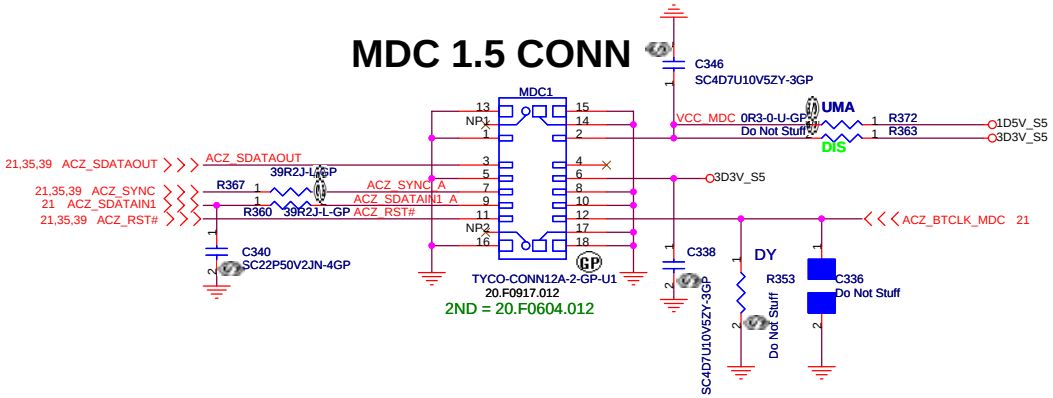
MDC 1.5 CONN



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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
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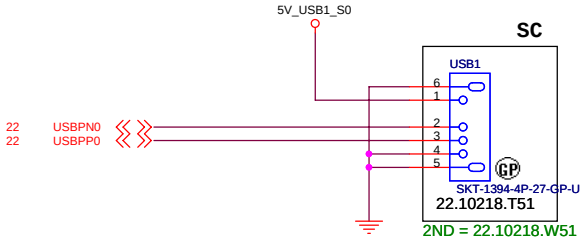

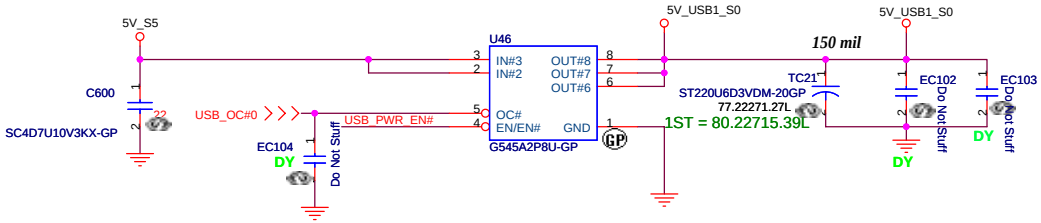

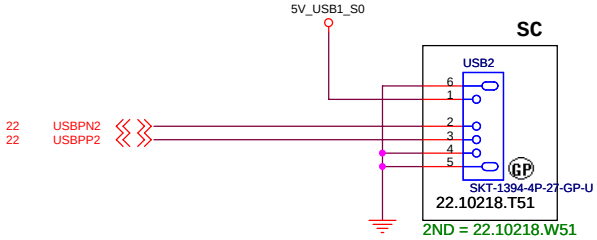

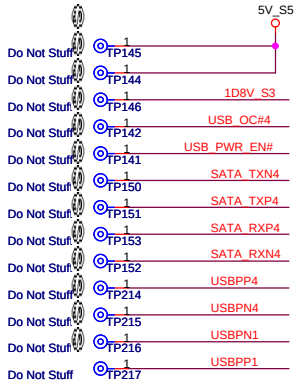

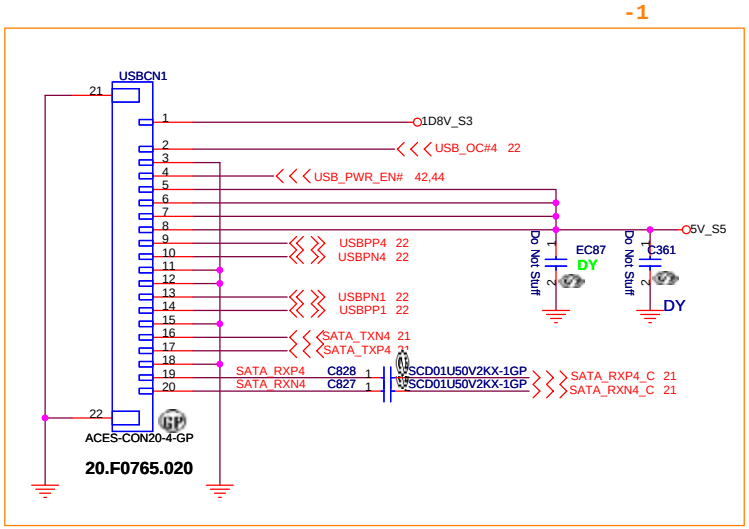

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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB		
Size	Document Number: Homa	Rev: -1
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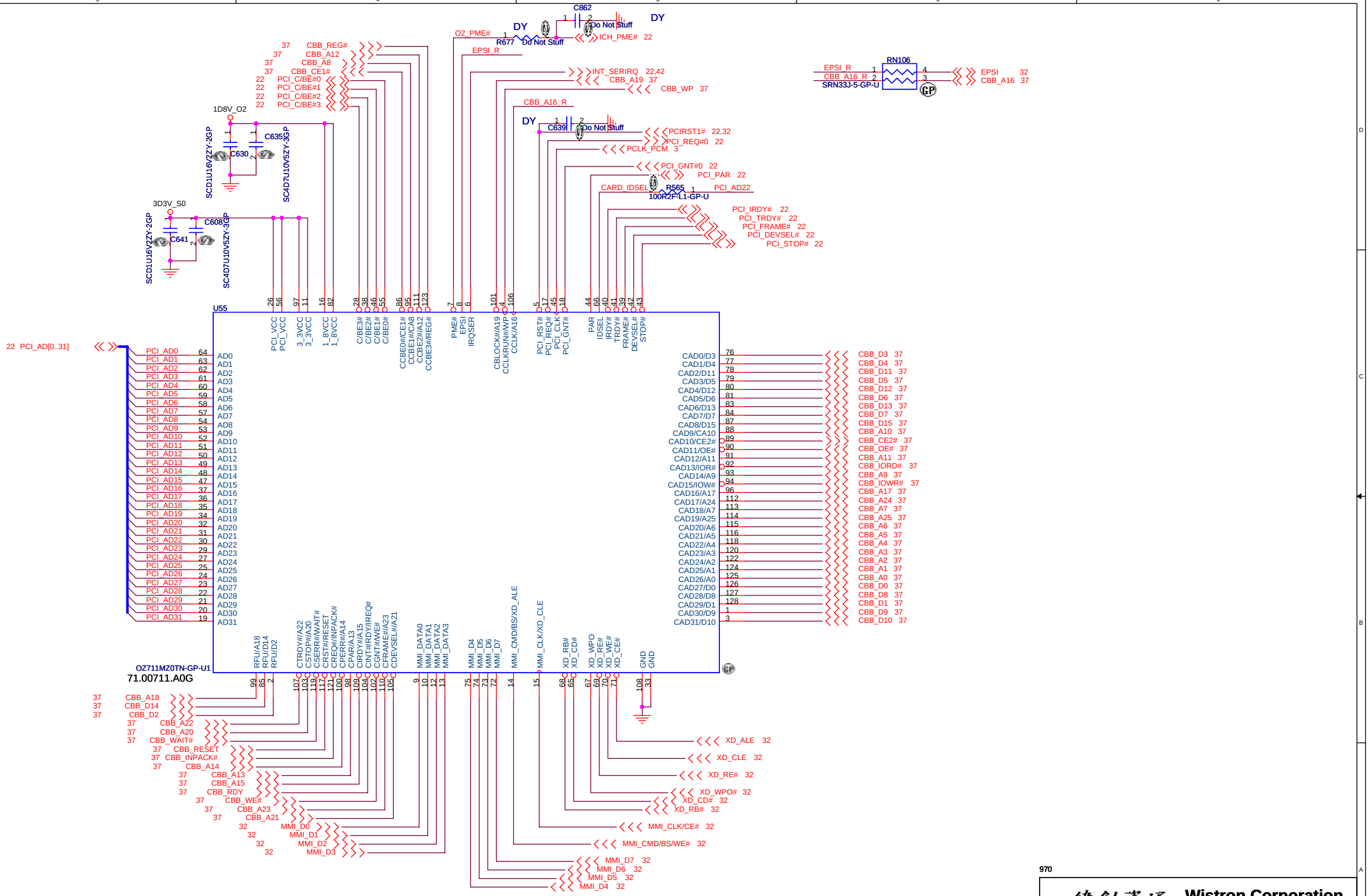

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Card Reader Controller - OZ711*
Size	Document Number: Homa; Rev: -1
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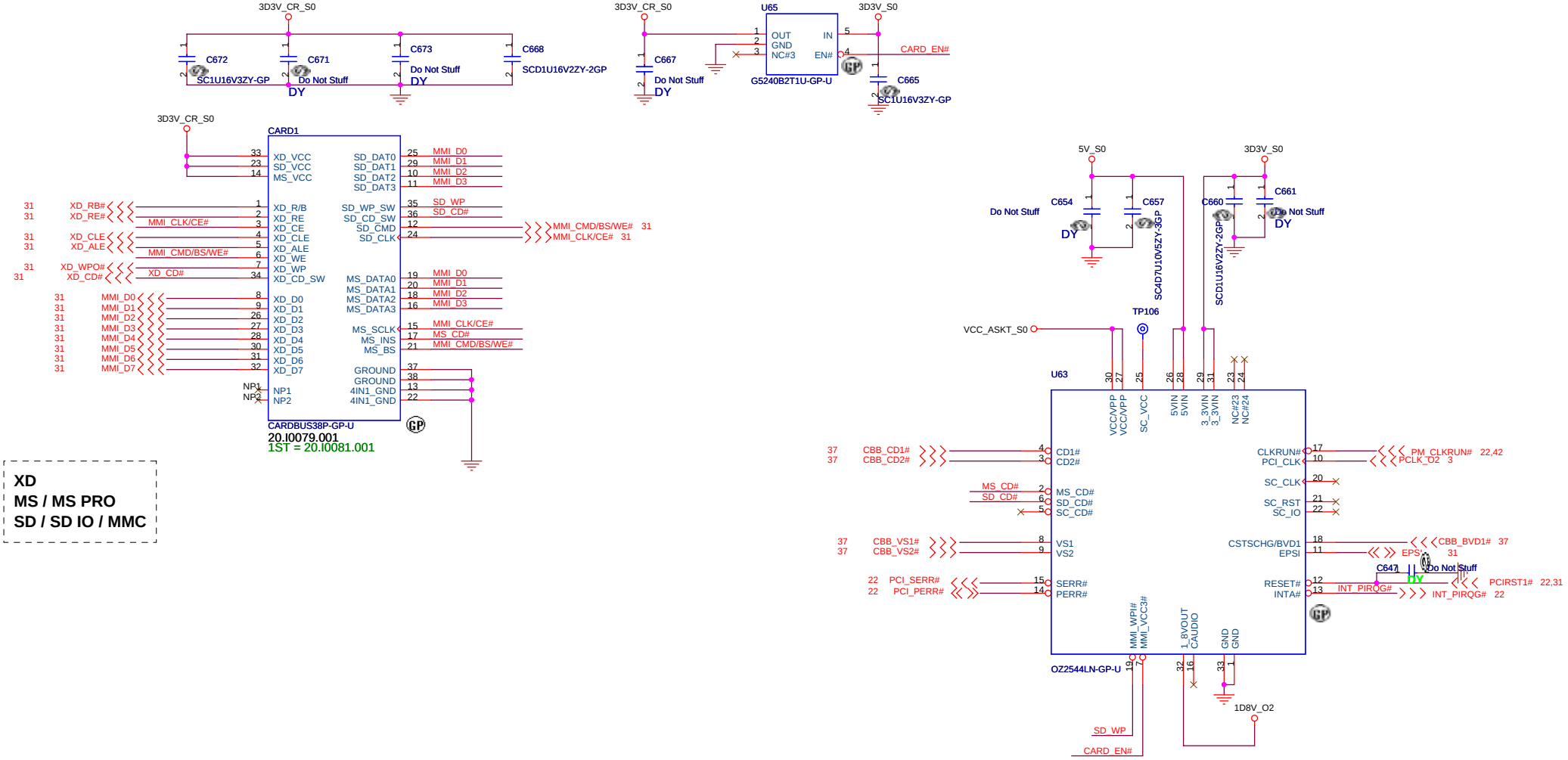

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader Connector

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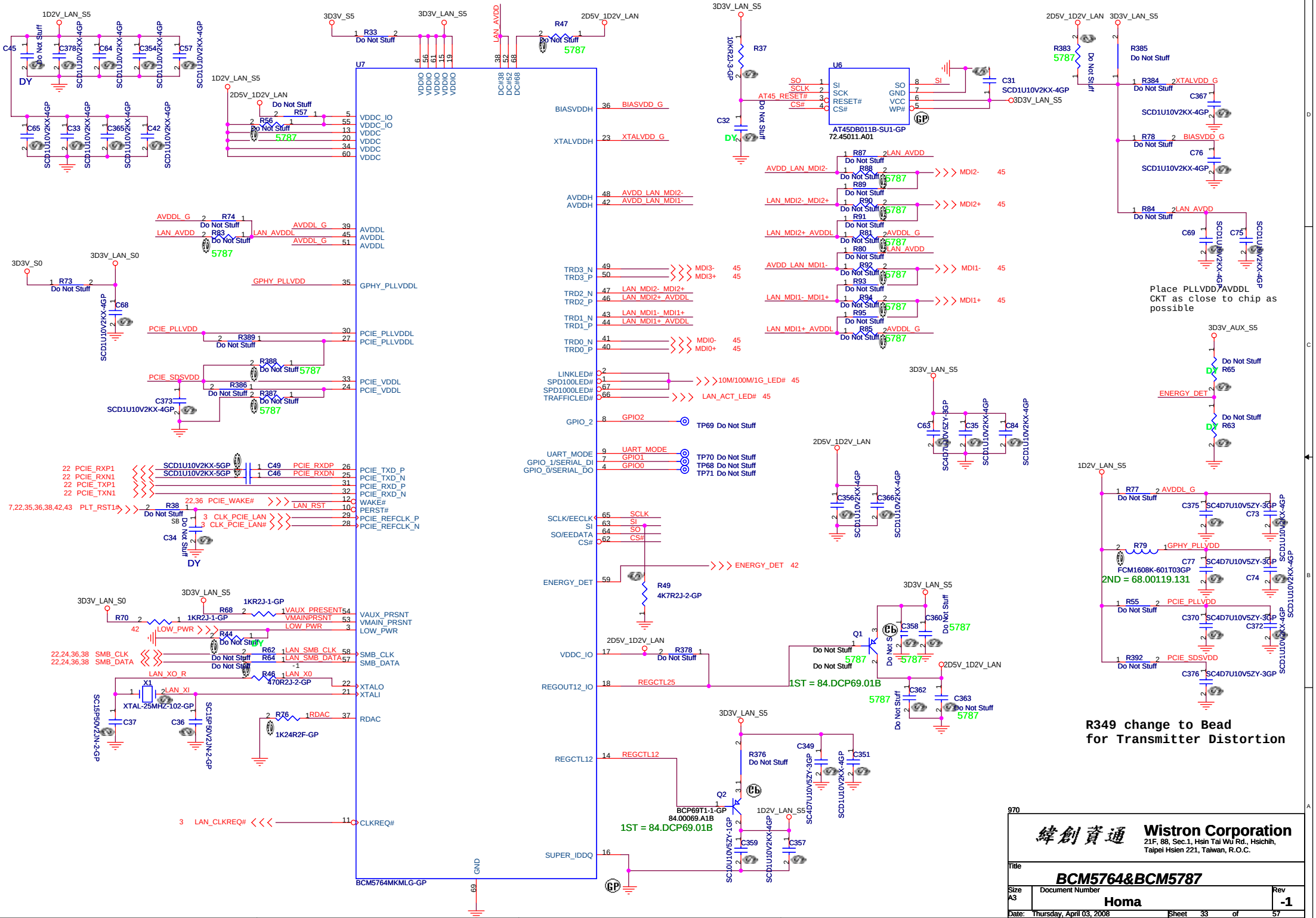
U7
BCM5764MKMLG-GP
Place PLLVDD/AVDDL CKT as close to chip as possible
R349 change to Bead for Transmitter Distortion
1ST = 84.DCP69.01B
1ST = 84.DCP69.01B
2ND = 68.00119.131
970
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764&BCM5787
Size A3
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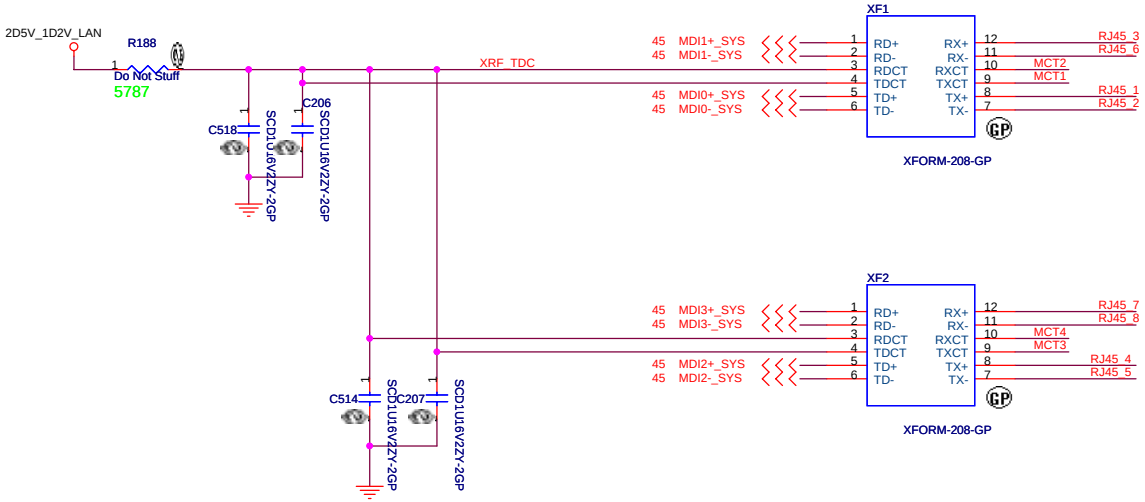
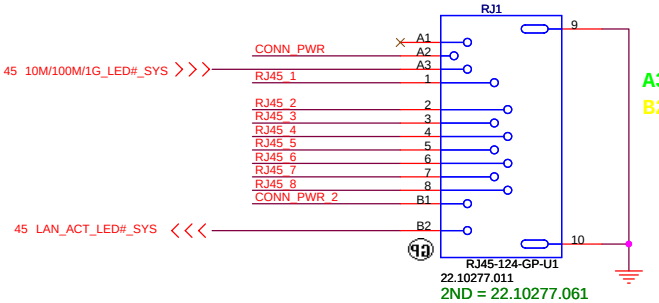
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector

LAN Connector

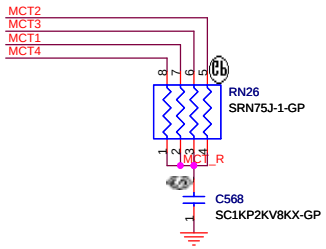
GIGA Lan Transformer

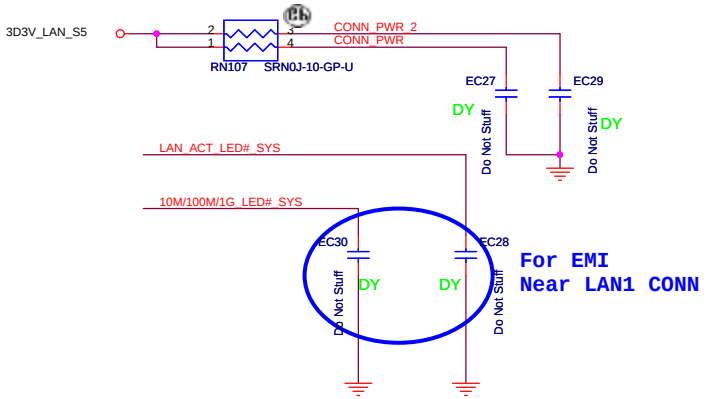




LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.





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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN CONN		
Size: A3	Document Number	Rev: -1
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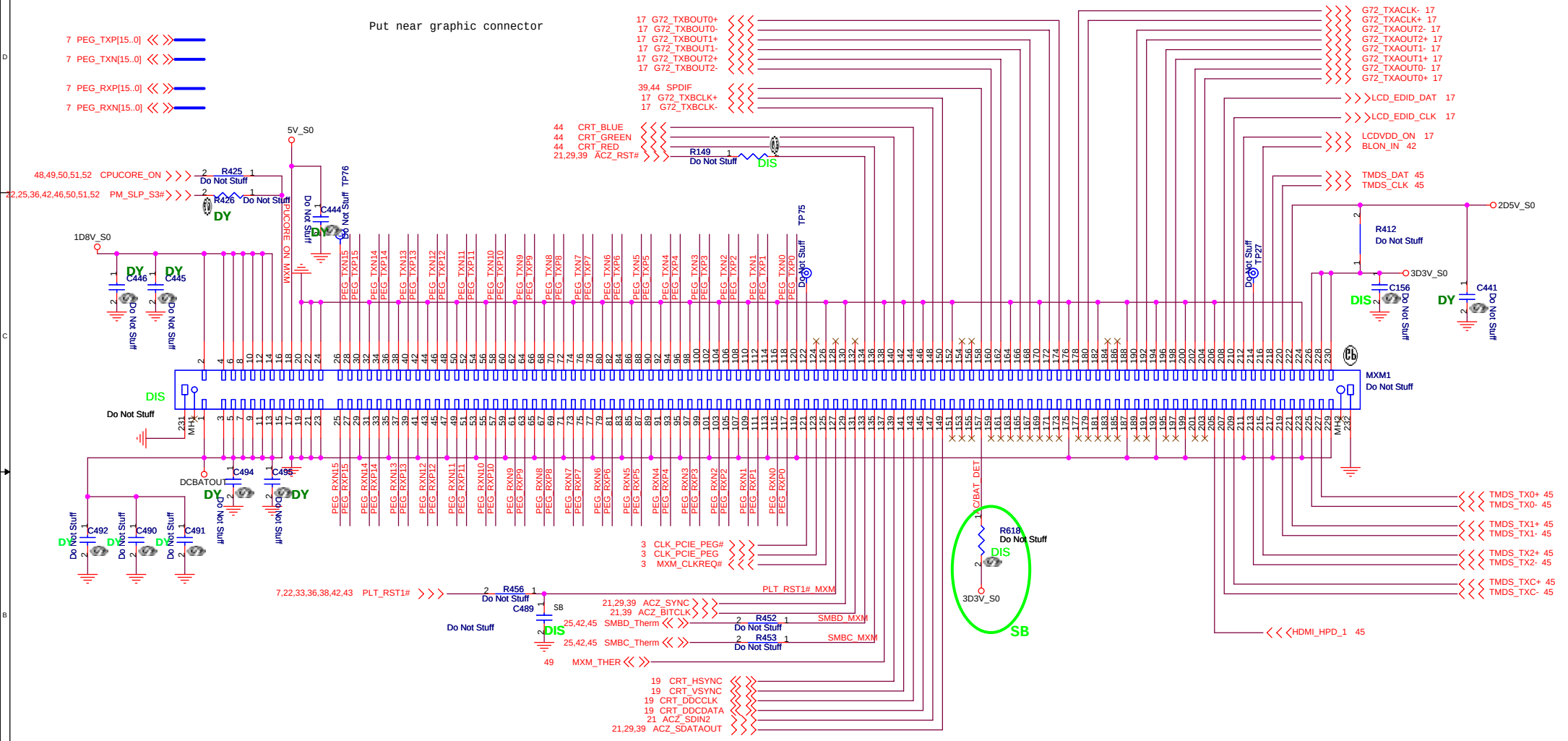
NV SMBus
A(pin143&145) : VGA(CRT) / DOCK
B(pin218&220) : DVI
C(pin208&210) : HDMI / TPI / LVDS

Put near graphic connector



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Graphic MXM CONN**	
Size A3	Document Number **Homa**	Rev -1
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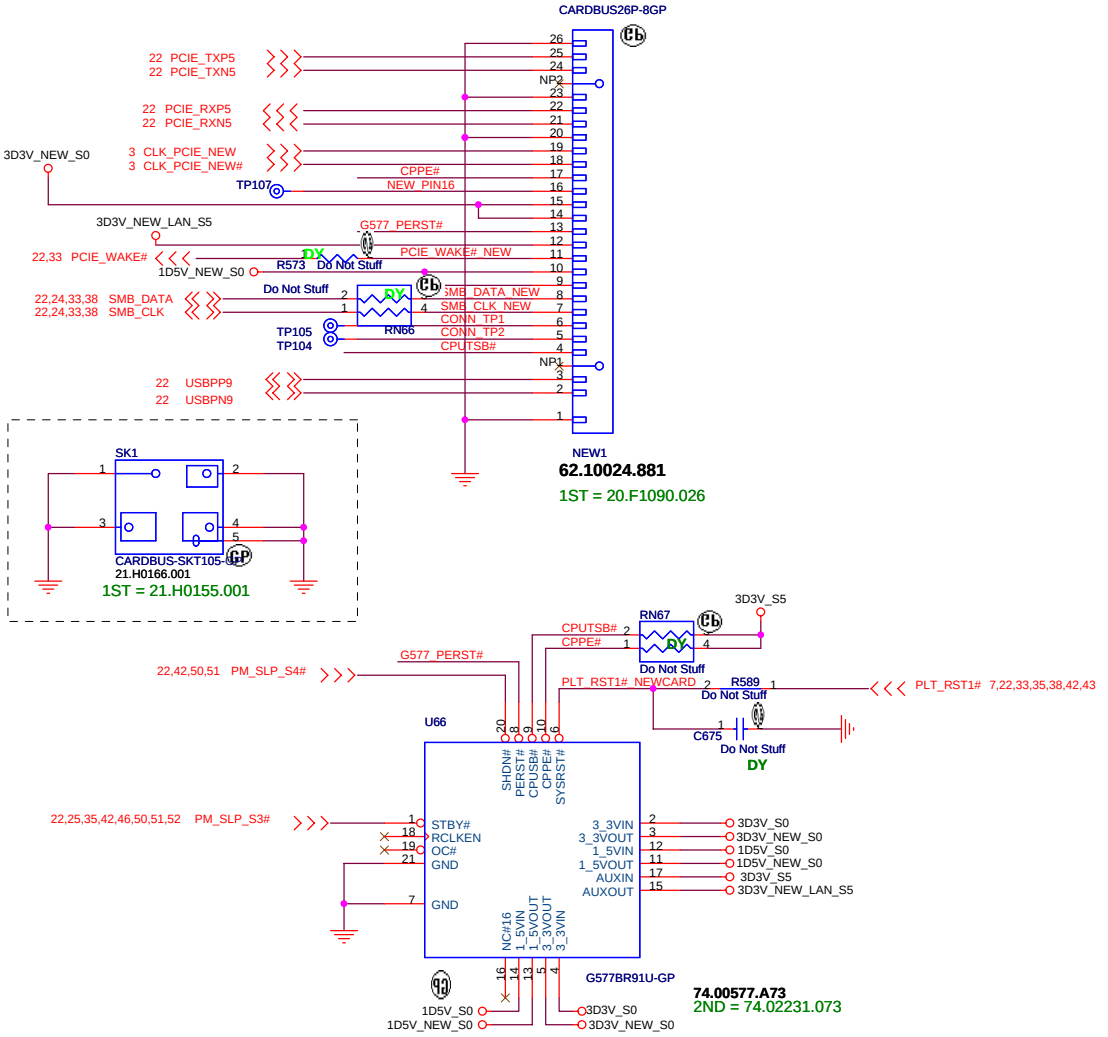
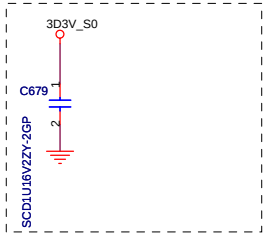
NEWCARD Connector

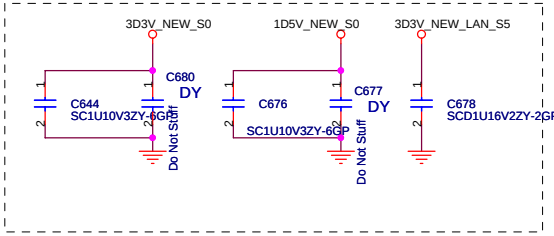
Reserve the symbol
for bottom side
connector



Place them Near to Chip



Place them Near to Connector



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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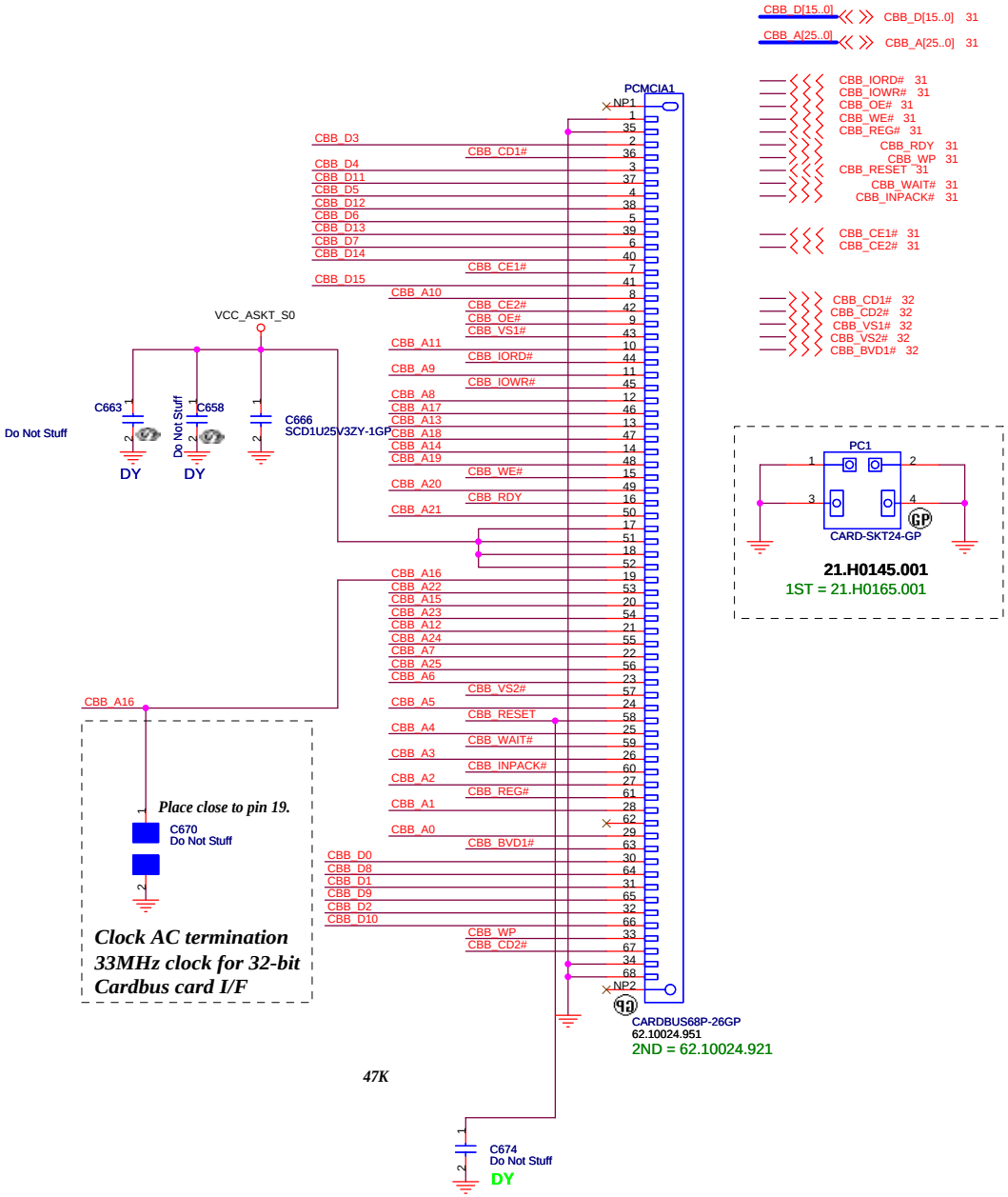
PCMCIA Socket

Cardbus I/F



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***PCMCIA***	
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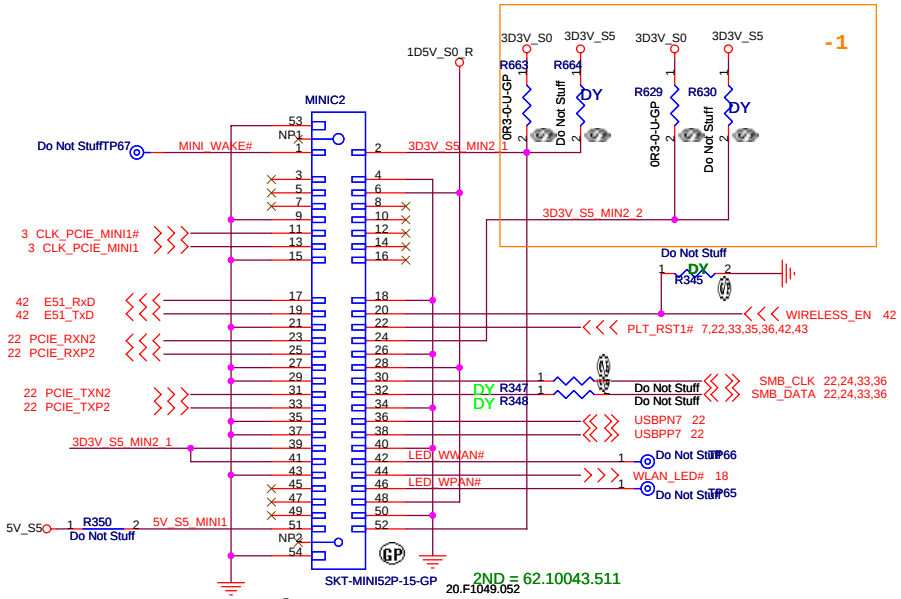
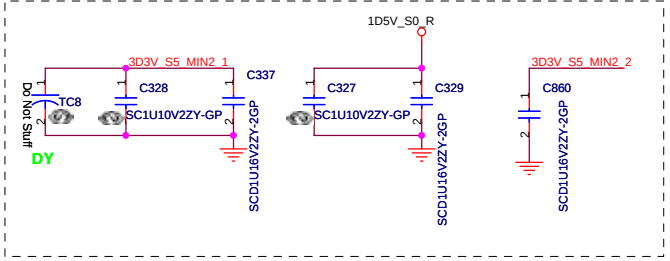
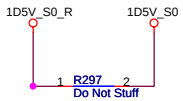
Mini Card Connector(WLAN)

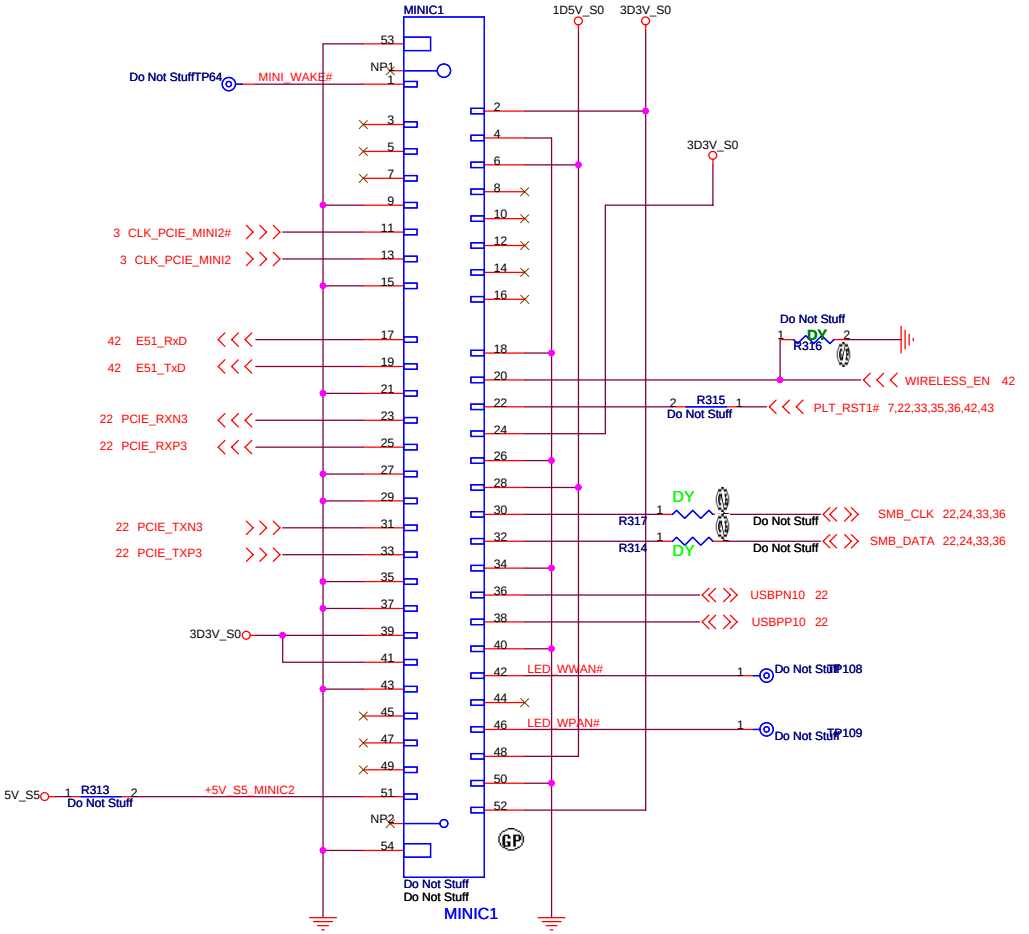


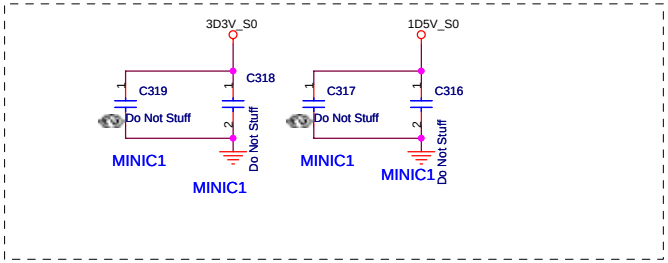


Vo(cal.)=1.5024V **OCP>3.2A**



Mini Card Connector





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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **MINI CARD**		
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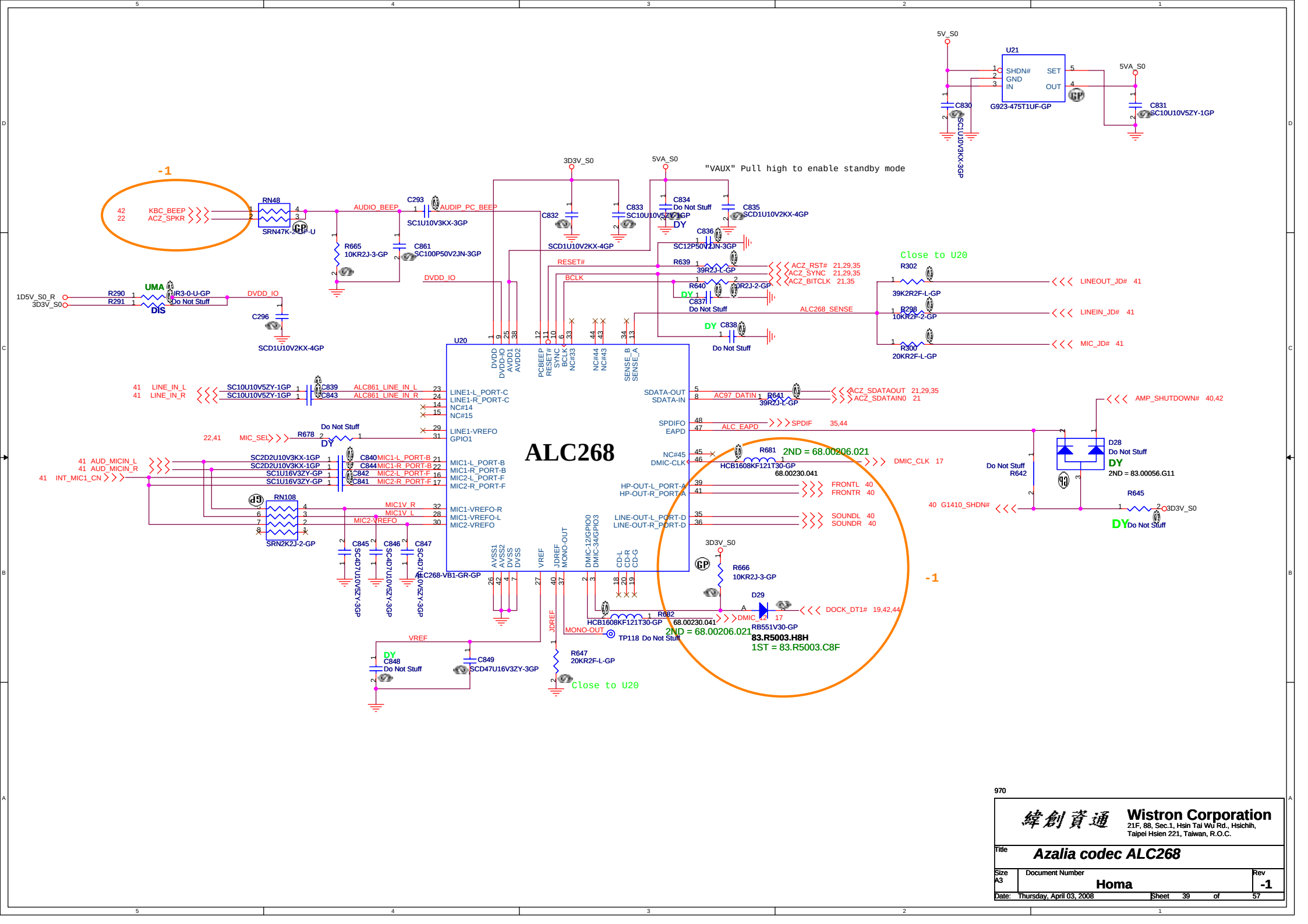
ALC268
U20
ALC268-VB1-GR-GP
U21
G923-475T1UF-GP
"VAUX" Pull high to enable standby mode
Close to U20
-1
2ND = 68.00206.021
83.R5003.H8H
1ST = 83.R5003.C8F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Azalia codec ALC268
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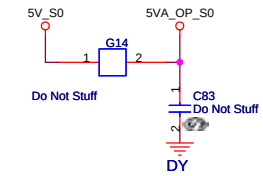
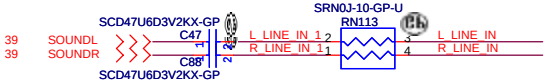
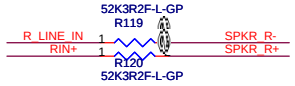
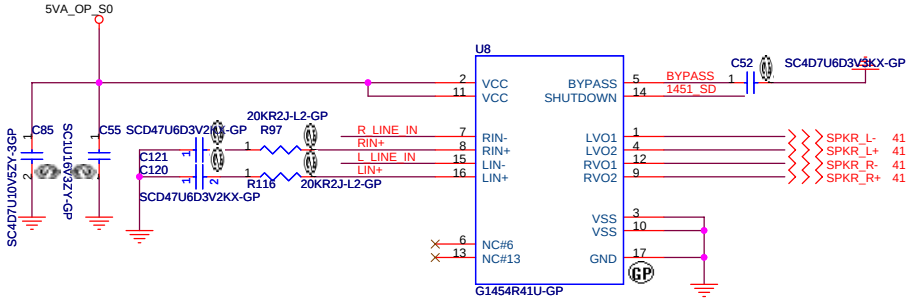
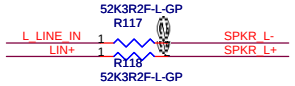
AUDIO OP AMPLIFIER

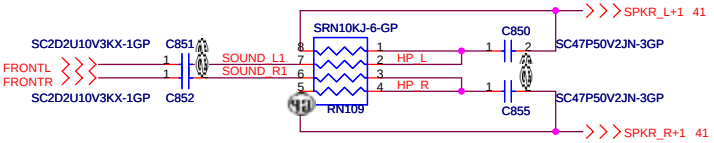


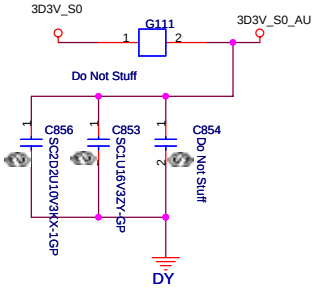


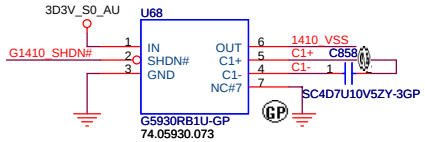


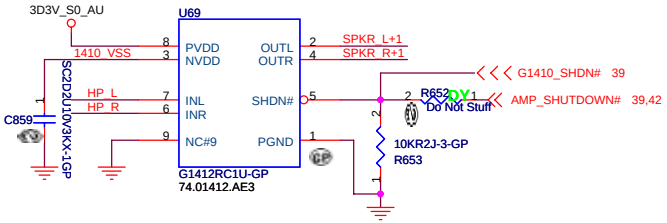




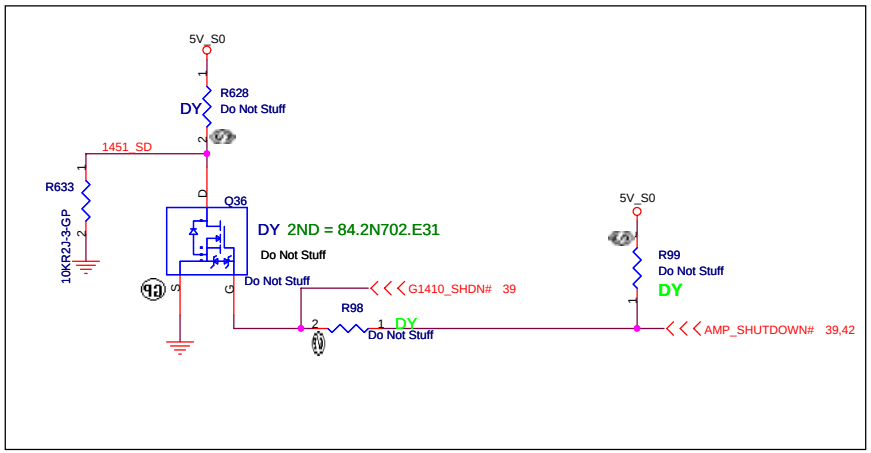








SC



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*AUDIO AMP AND JACK*
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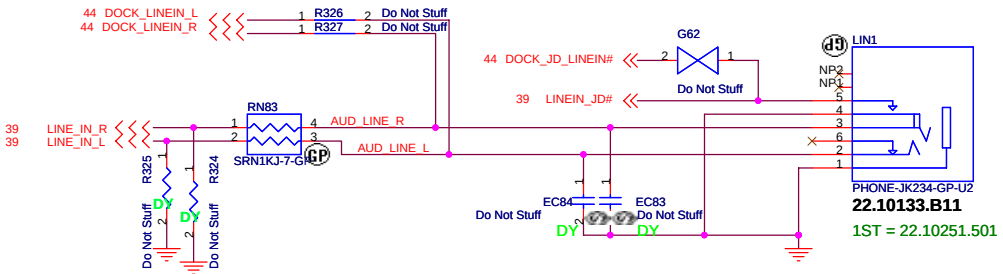
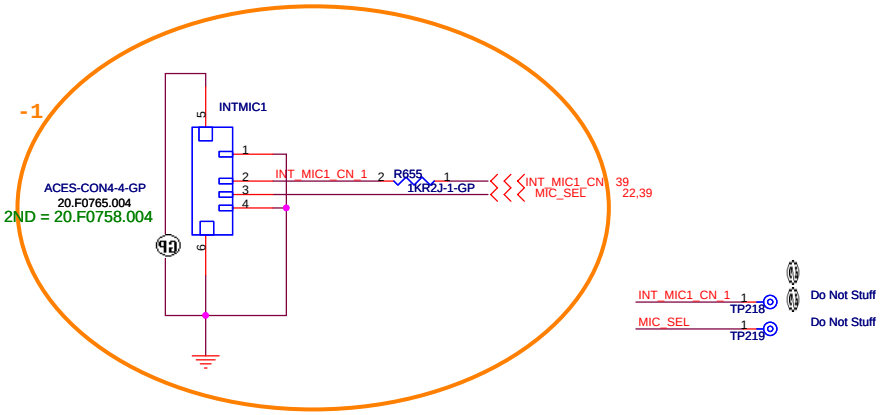
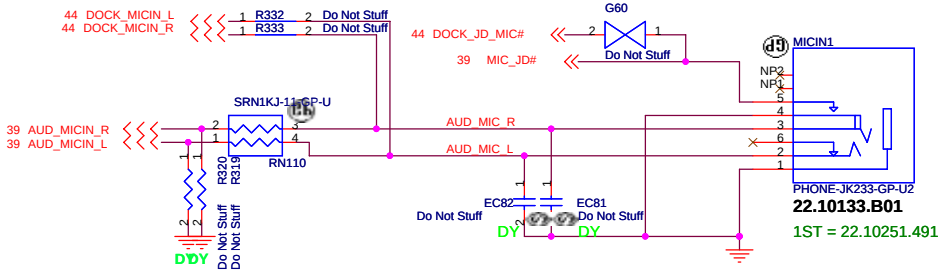
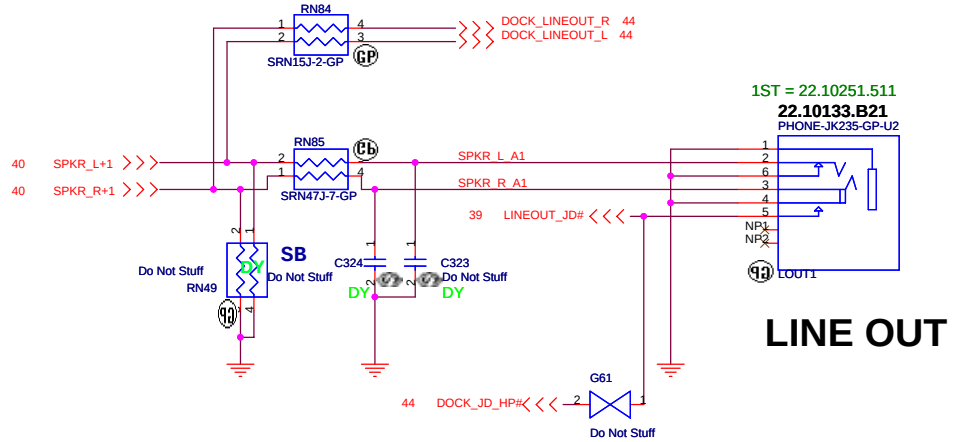
LINE IN





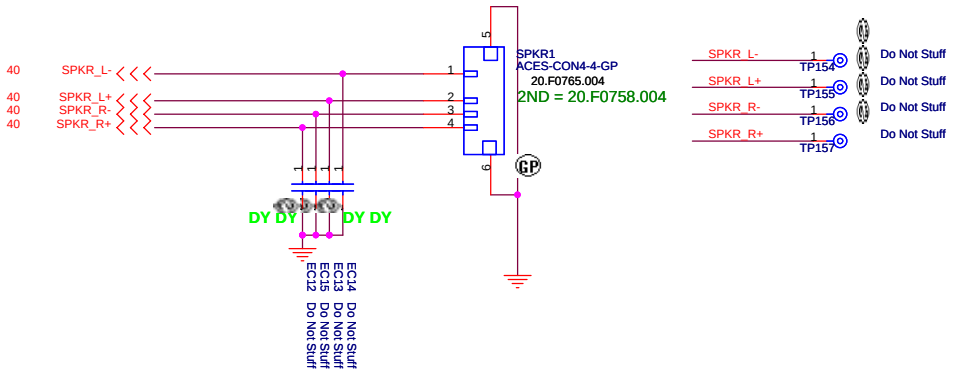
MIC IN





LINE OUT

Internal Speaker



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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*AUDIO JACK*	
Size	Document Number Homa	Rev -1
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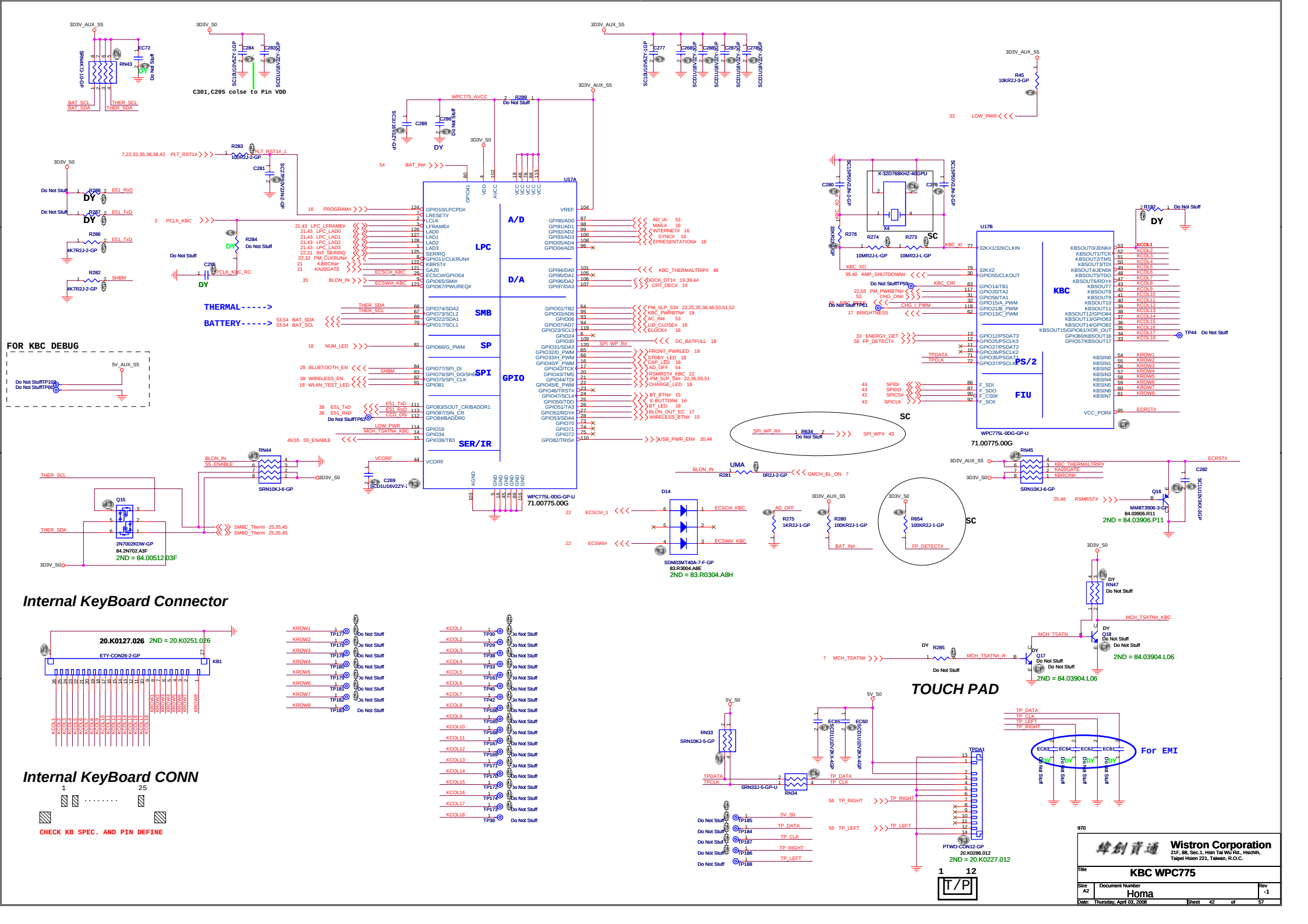
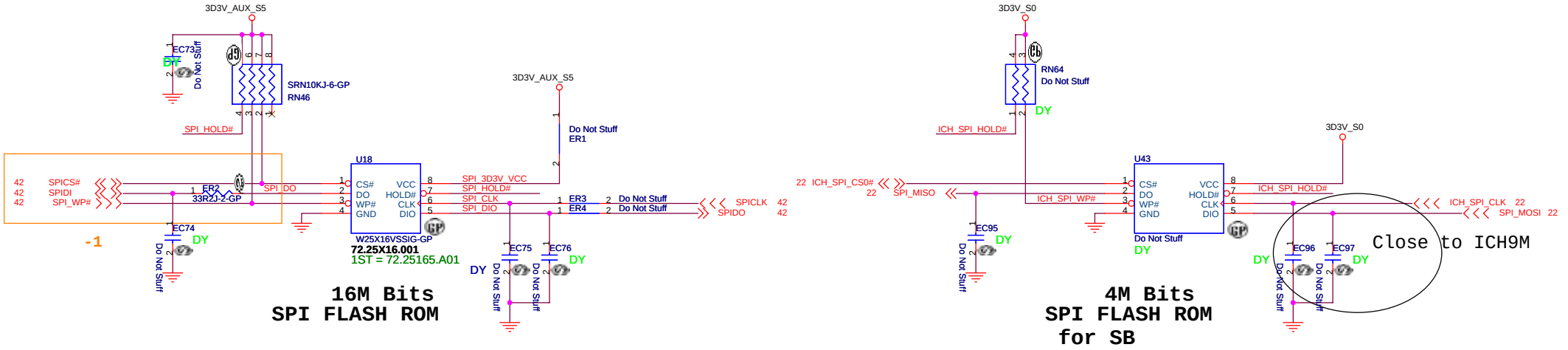
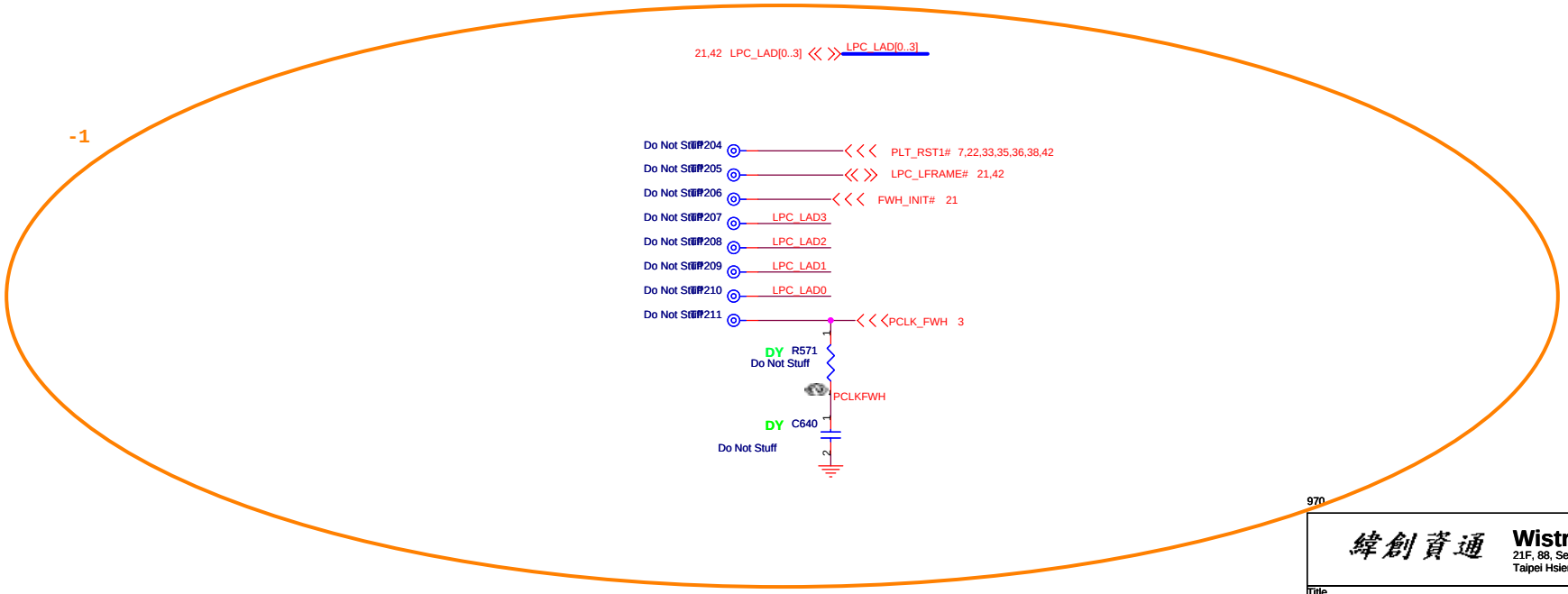

C301,C295 colse to Pin VDD
FOR KBC DEBUG
THERMAL----->
BATTERY----->
WPC775L-0DG-GP-U
71.00775.00G
2ND = 84.00512.03F
2ND = 83.R0304.A8H
2ND = 84.03906.P11
2ND = 84.03904.L06
2ND = 84.03904.L06
Internal KeyBoard Connector
20.K0127.026 2ND = 20.K0251.026
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
TOUCH PAD
2ND = 20.K0227.012
For EMI
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
Homa
Thursday, April 03, 2008





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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***BIOS***	
Size	Document Number **Homa**	Rev -1
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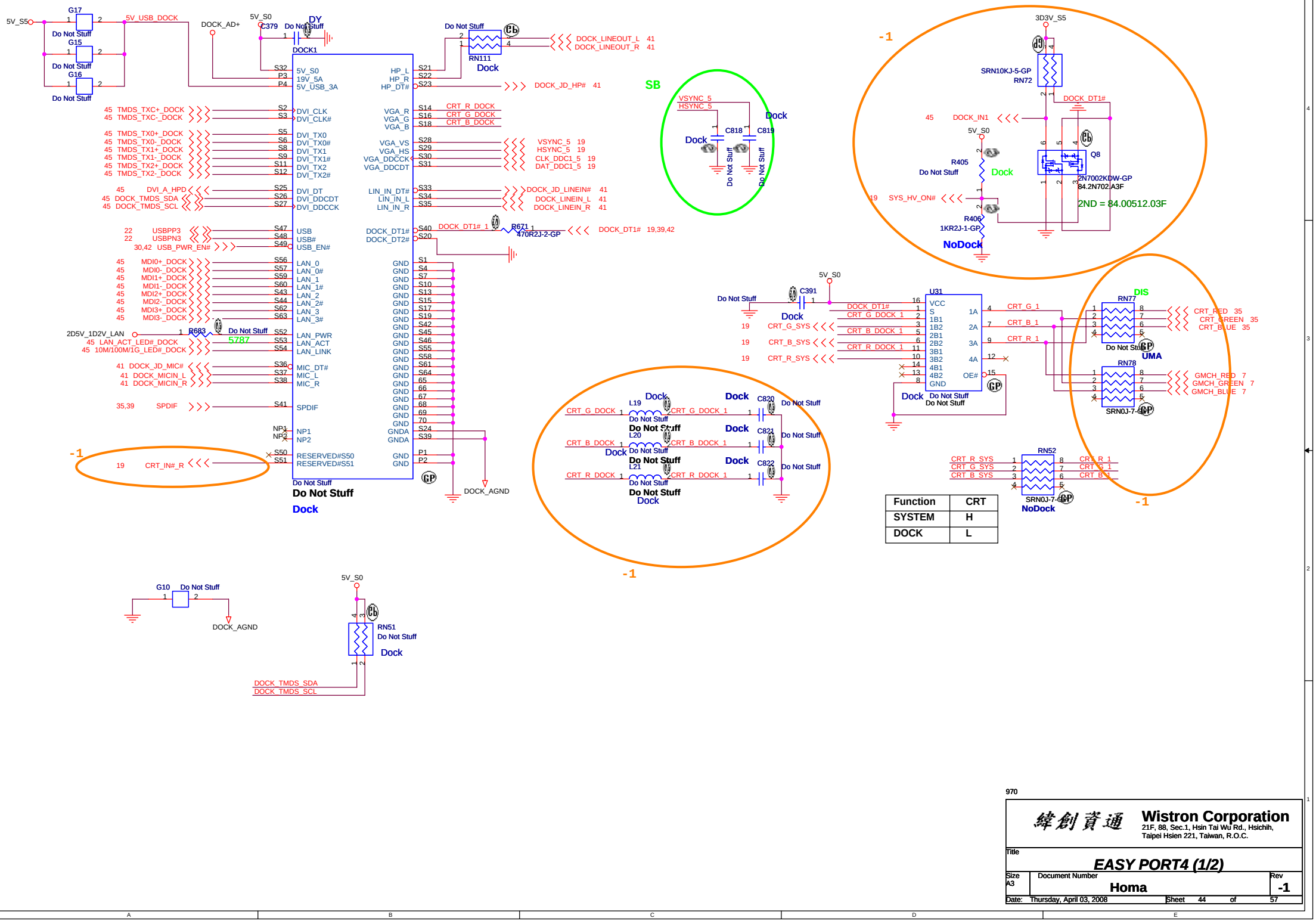
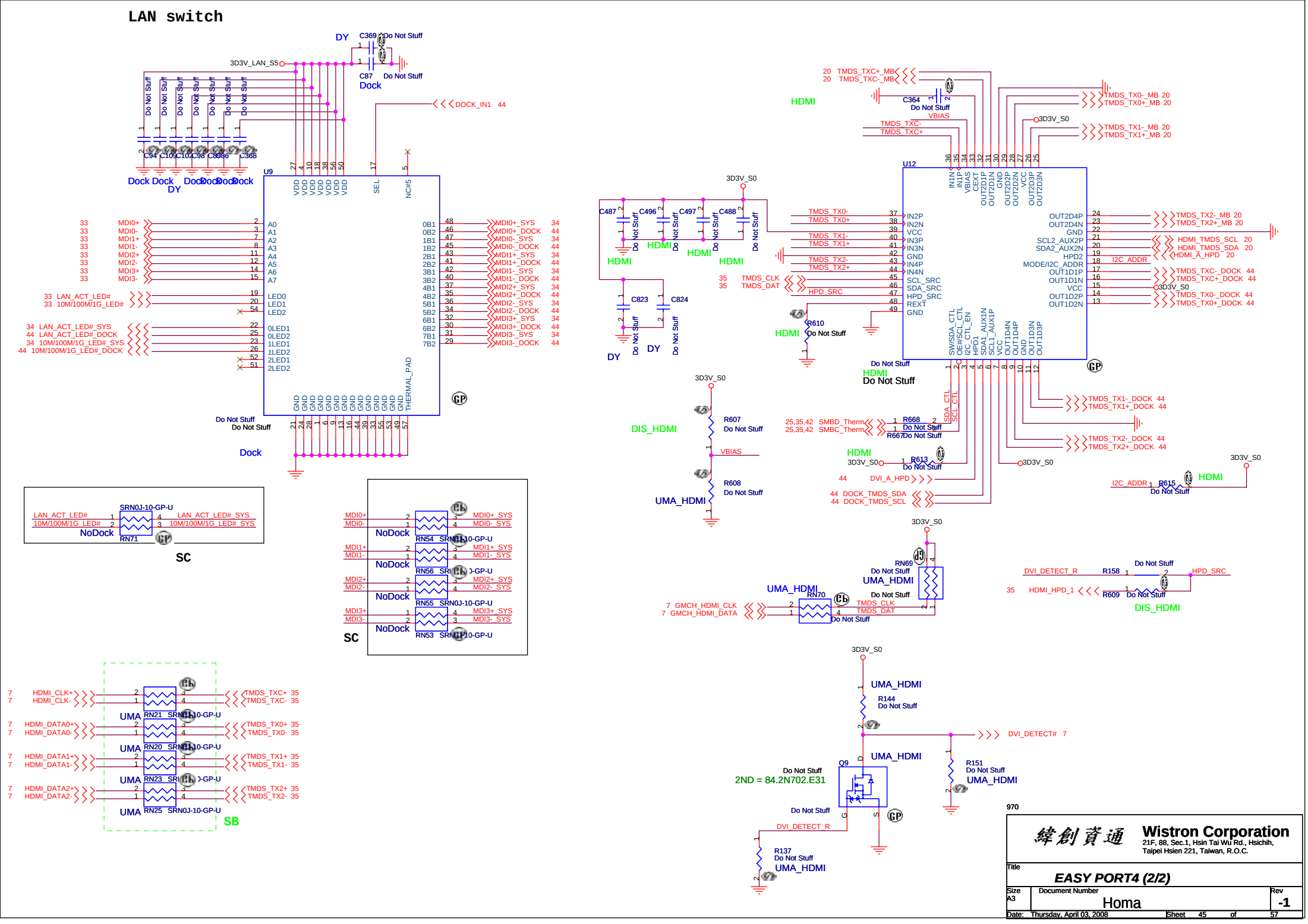

DOCK1
DOCK_AGND
Do Not Stuff
Dock
SB
-1
NoDock
DIS
UMA
RN72
RN77
RN78
RN52
RN51
RN111
U31
Q8
2N7002KDW-GP
84.2N702.A3F
2ND = 84.00512.03F
SRN10KJ-5-GP
1KR2J-1-GP
470R2J-2-GP
SRN0J-7-GP
5787
Function
CRT
SYSTEM
H
DOCK
L
970
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EASY PORT4 (1/2)
Size
A3
Document Number
Homa
Rev
-1
Date: Thursday, April 03, 2008
Sheet 44 of 57

LAN switch



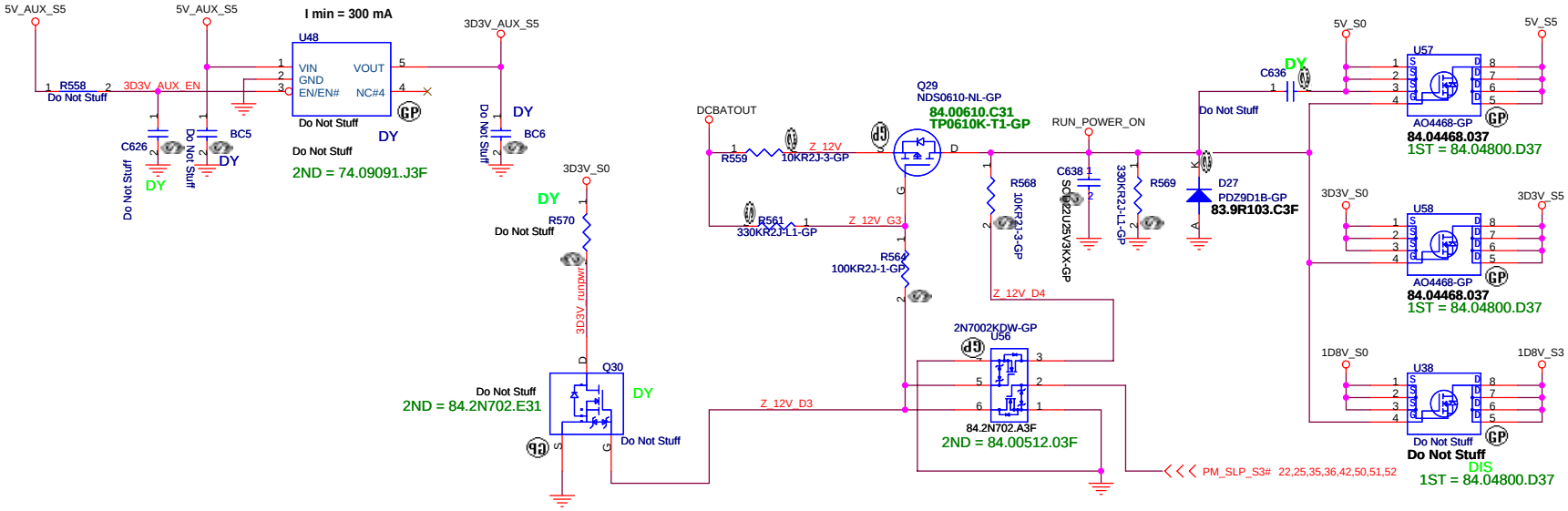
970

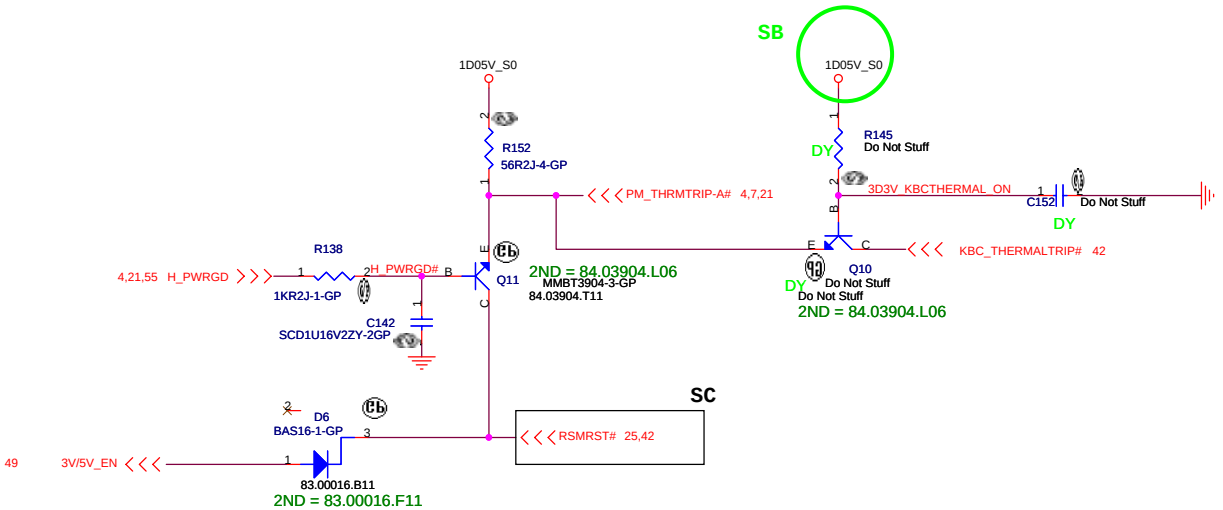
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: EASY PORT4 (2/2)		
Size: A3	Document Number: Homa	Rev: -1
Date: Thursday, April 03, 2008	Sheet 45 of 57	

Aux Power

3D3V_AUX_S5

Run Power





970

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RUN POWER and 3D3V_AUX_S5***	
Size	Document Number **Homa**	Rev -1
Date: Thursday, April 03, 2008	Sheet 46 of 57	

CPU_CORE
ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6266A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

Output Power
VCC_CORE_PWR(O)

VGATE_PWRGD
VCC_CORE(Imax=38A)

TPS51125
5V/3D3V

DCBATOUT_51125
PM_SLP_S4#
ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)

RT9018A
1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN

1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

RT9026
0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5

VTT
VTTREF

0D9V_S3 (1A)
0D9V_S3_1

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

Output Power
VGFXCORE (O)

CPUCORE_ON
VCC_GFXCORE(5.5A)

G9131
2D5V_S0

3D3V_S0

INPUT
OUT

2D5V_S0(0.3A)

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_51124

PM_SLP_S4#
PM_SLP_S3#

CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (15A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

Charger BQ24750

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

AC_IN#
AD_IA
BT+
DCBATOUT

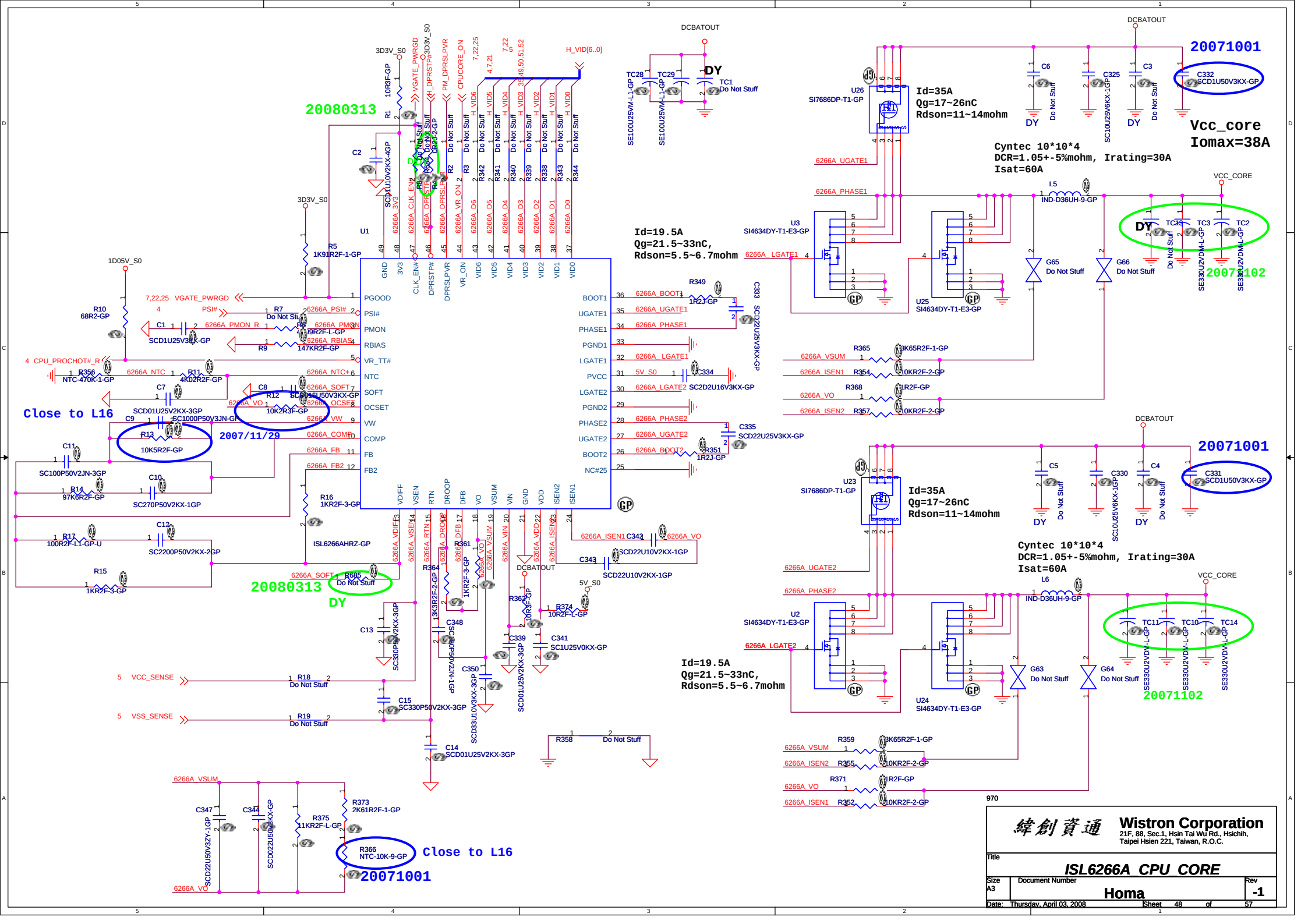
970

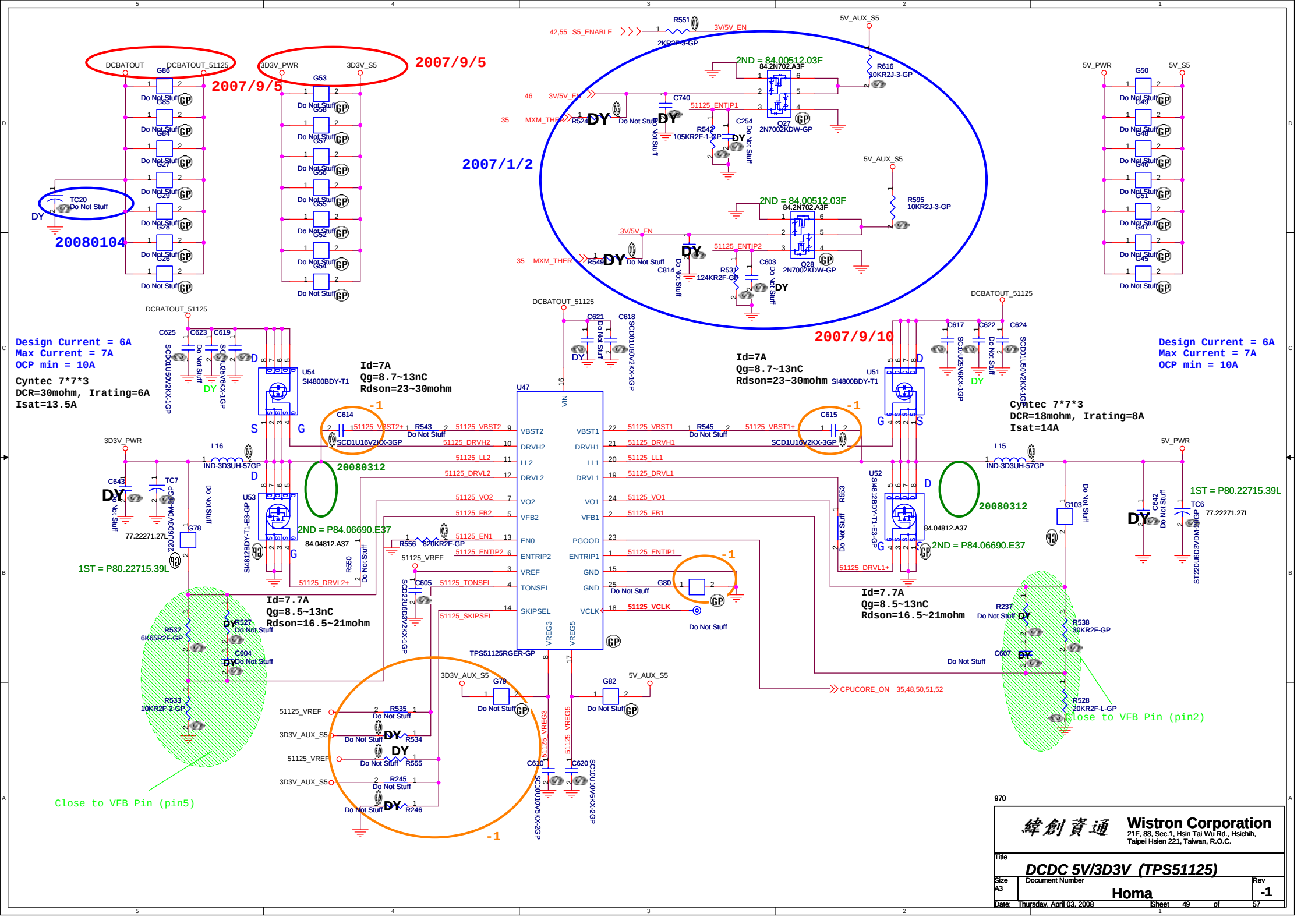
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Logic

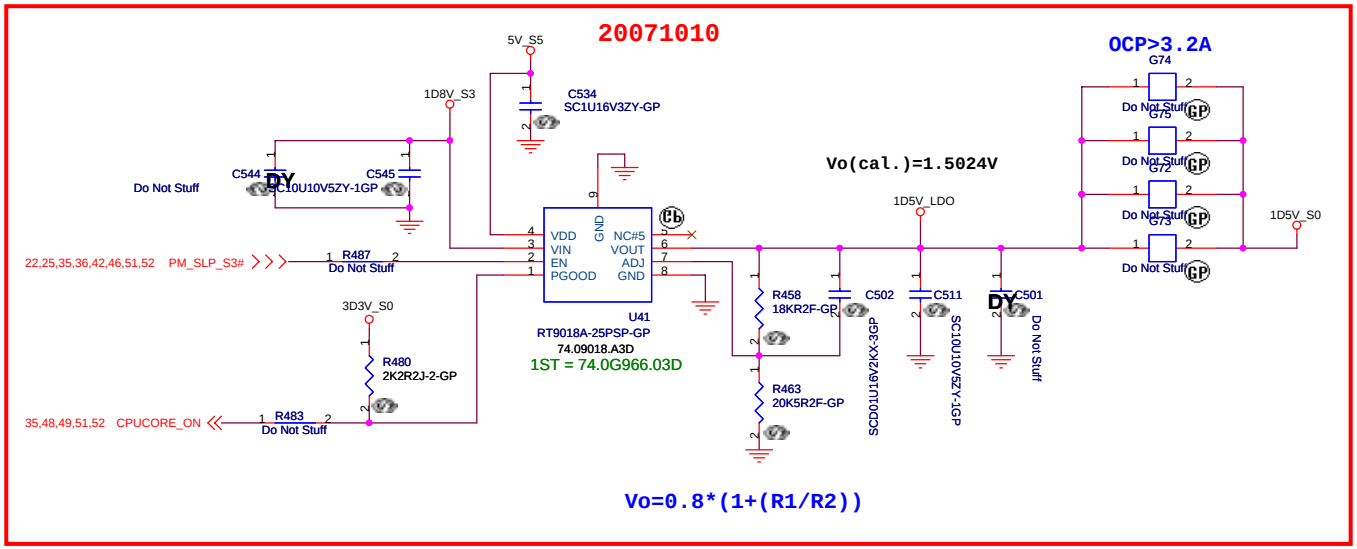
Size: B | Document Number: Homa | Rev: -1

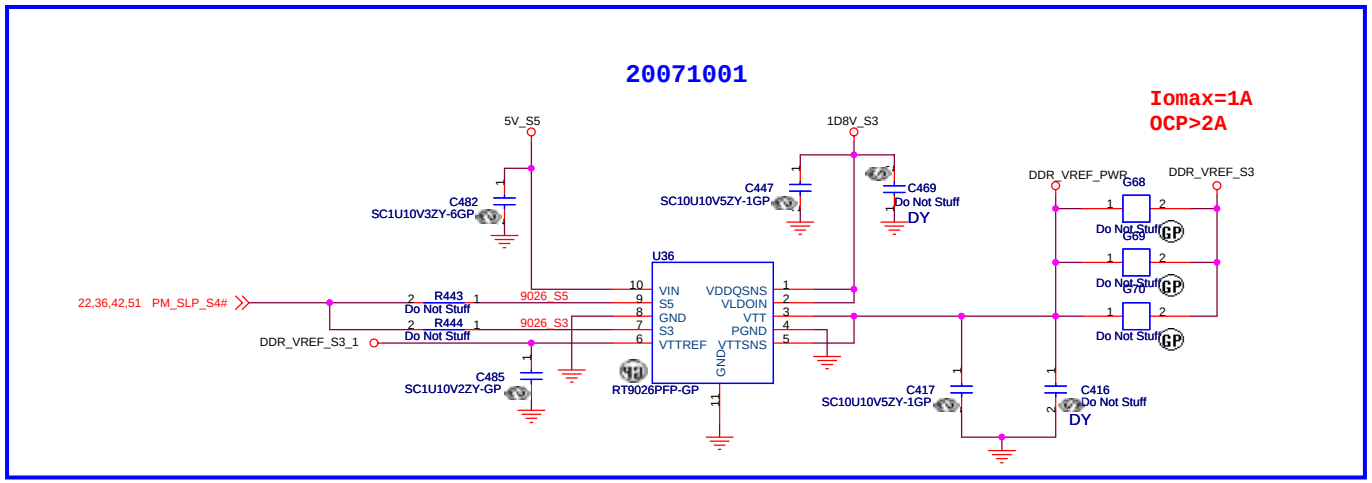
Date: Thursday, April 03, 2008 | Sheet 47 of 57


20080313
Close to L16
2007/11/29
20080313
DY
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Vcc_core
Iomax=38A
20071001
20071102
Close to L16
20071001
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A_CPU_CORE
Homa
Date: Thursday, April 03, 2008
Sheet 48 of 57

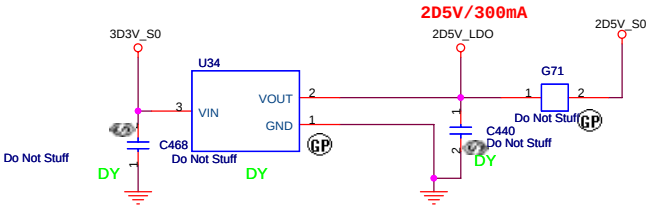

2007/9/5
2007/1/2
20080104
2007/9/10
20080312
Design Current = 6A
Max Current = 7A
OCP min = 10A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=18mohm, Irating=8A
Isat=14A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
2ND = 84.00512.03F
2ND = P84.06690.E37
1ST = P80.22715.39L
TPS51125RGER-GP
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
DCDC 5V/3D3V (TPS51125)
Homa
Date: Thursday, April 03, 2008
Sheet 49 of 57

1D5V_S0
Iomax=2.5A





2D5V_S0
Iomax=0.3A



970

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D5V & 0D9V & 2D5V		
Size: A3	Document Number: Homa	Rev: -1
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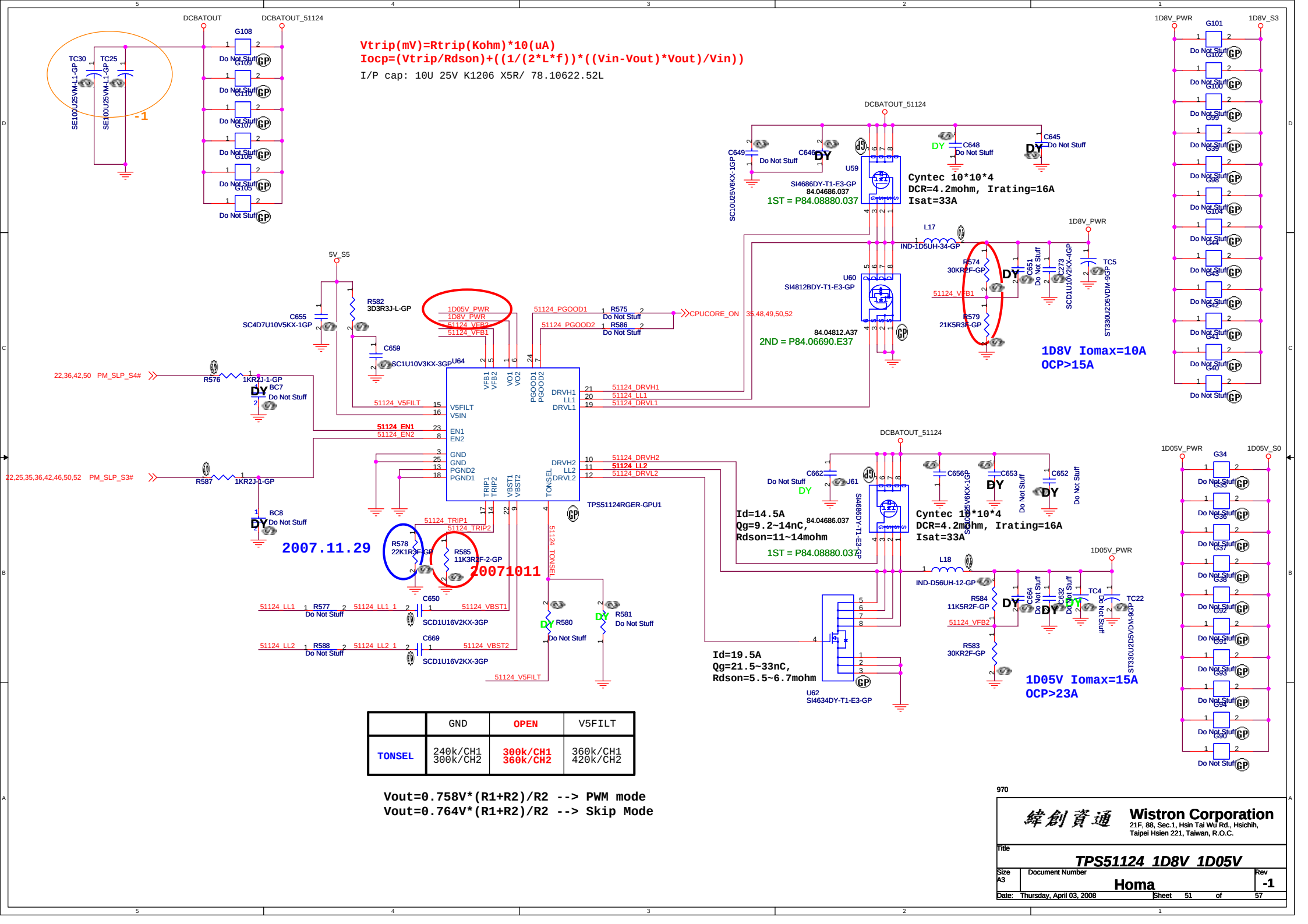

	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

970

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124 1D8V 1D05V

Size	Document Number	Rev
A3	Homa	-1

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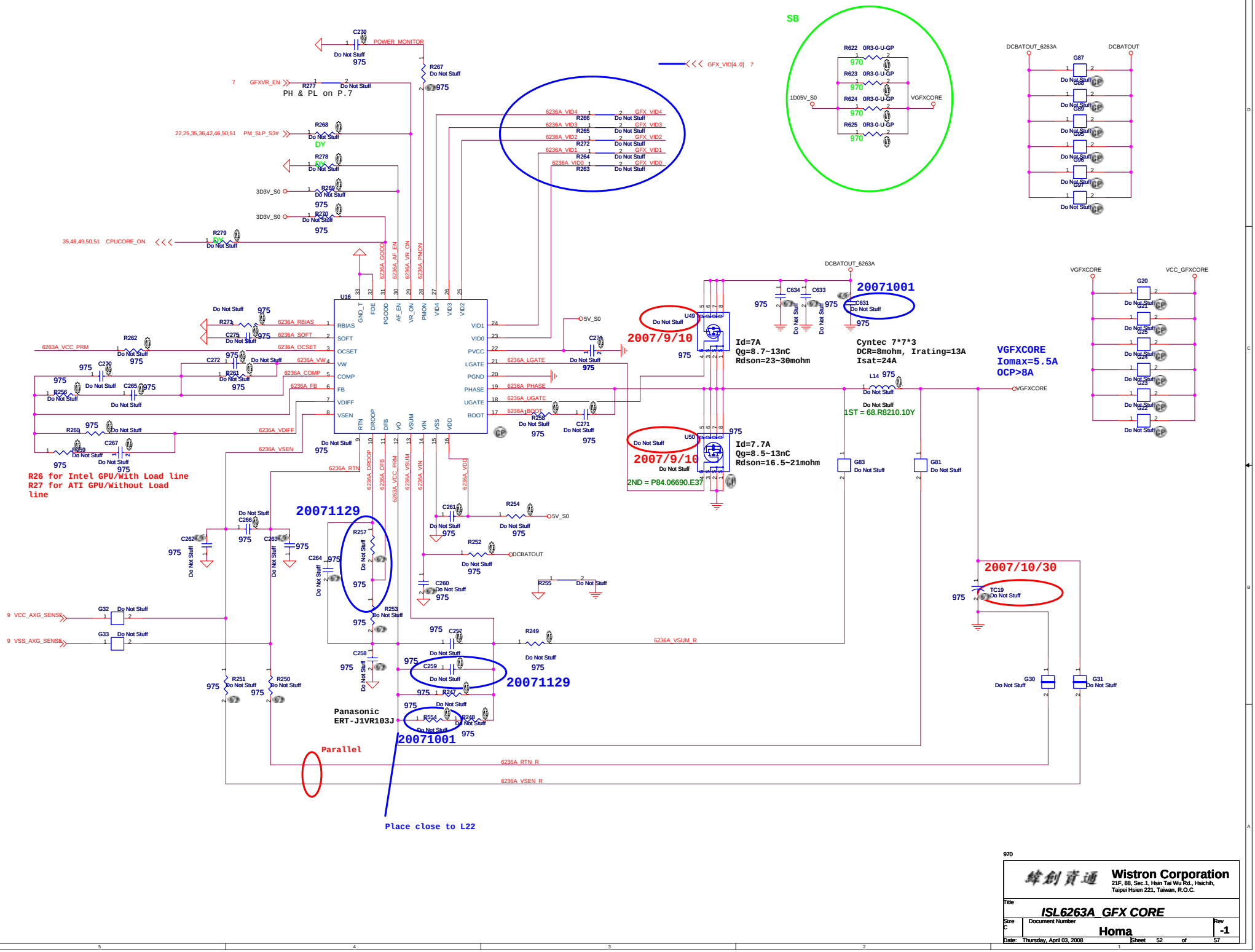
SB
U16
RBIAS
SOFT
OCSET
VW
COMP
FB
VDIFF
VSEN
RTN
DROOP
DFB
VO
VSUM
VIN
VSS
VDD
GND_T
FDE
PGOOD
AE_EN
VR_ON
PMON
VID4
VID3
VID2
VID1
VID0
PVCC
LGATE
PGND
PHASE
UGATE
BOOT
U49
U50
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
VGFXCORE
Iomax=5.5A
OCP>8A
2007/9/10
2007/9/10
20071001
20071129
20071129
20071001
2007/10/30
1ST = 68.R8210.10Y
2ND = P84.06690.E37
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
Panasonic
ERT-J1VR103J
Parallel
Place close to L22
PH & PL on P.7
DY
DCBATOUT_6263A
DCBATOUT
VGFXCORE
VCC_GFXCORE
GFX_VID[4..0]
POWER_MONITOR
GFXVR_EN
PM_SLP_S3#
CPUCORE_ON
6263A_VCC_PRM
6236A_RBIAS
6236A_SOFT
6236A_OCSET
6236A_VW
6236A_COMP
6236A_FB
6236A_VDIFF
6236A_VSEN
6236A_RTN
6236A_DROOP
6236A_DFB
6236A_VCC_PRM
6236A_VSUM
6236A_VIN
6236A_VDD
6236A_LGATE
6236A_PHASE
6236A_UGATE
6236A_BOOT
6236A_VID4
6236A_VID3
6236A_VID2
6236A_VID1
6236A_VID0
6236A_GOOD
6236A_AE_EN
6236A_VR_ON
6236A_PMON
GFX_VID4
GFX_VID3
GFX_VID2
GFX_VID1
GFX_VID0
VCC_AXG_SENSE
VSS_AXG_SENSE
6236A_VSUM_R
6236A_RTN_R
6236A_VSEN_R
1D05V_S0
VGFXCORE
5V_S0
3D3V_S0
DCBATOUT
R622 0R3-0-U-GP
R623 0R3-0-U-GP
R624 0R3-0-U-GP
R625 0R3-0-U-GP
970
975
Do Not Stuff
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6263A_GFX CORE
Homa
Rev -1
Thursday, April 03, 2008
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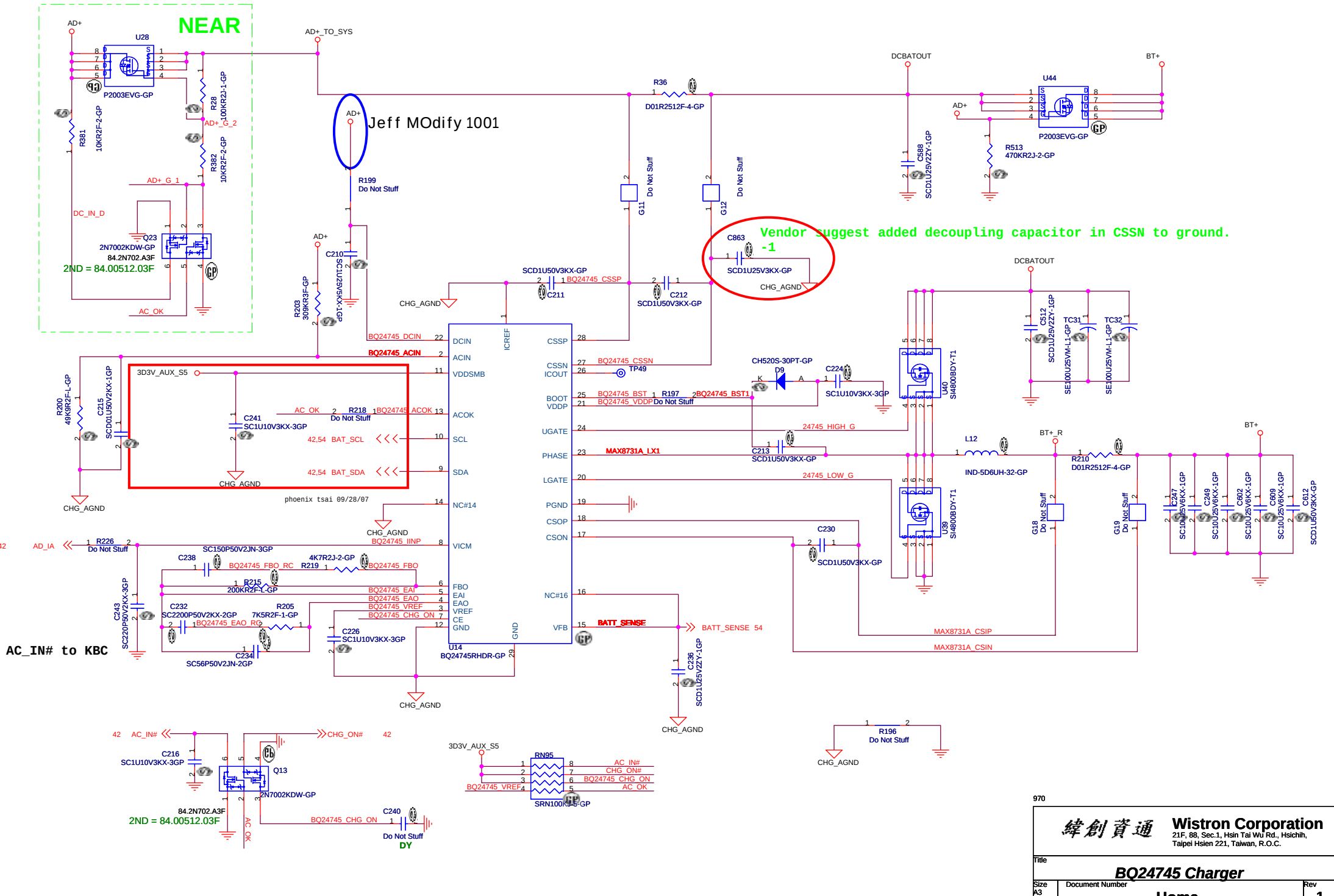
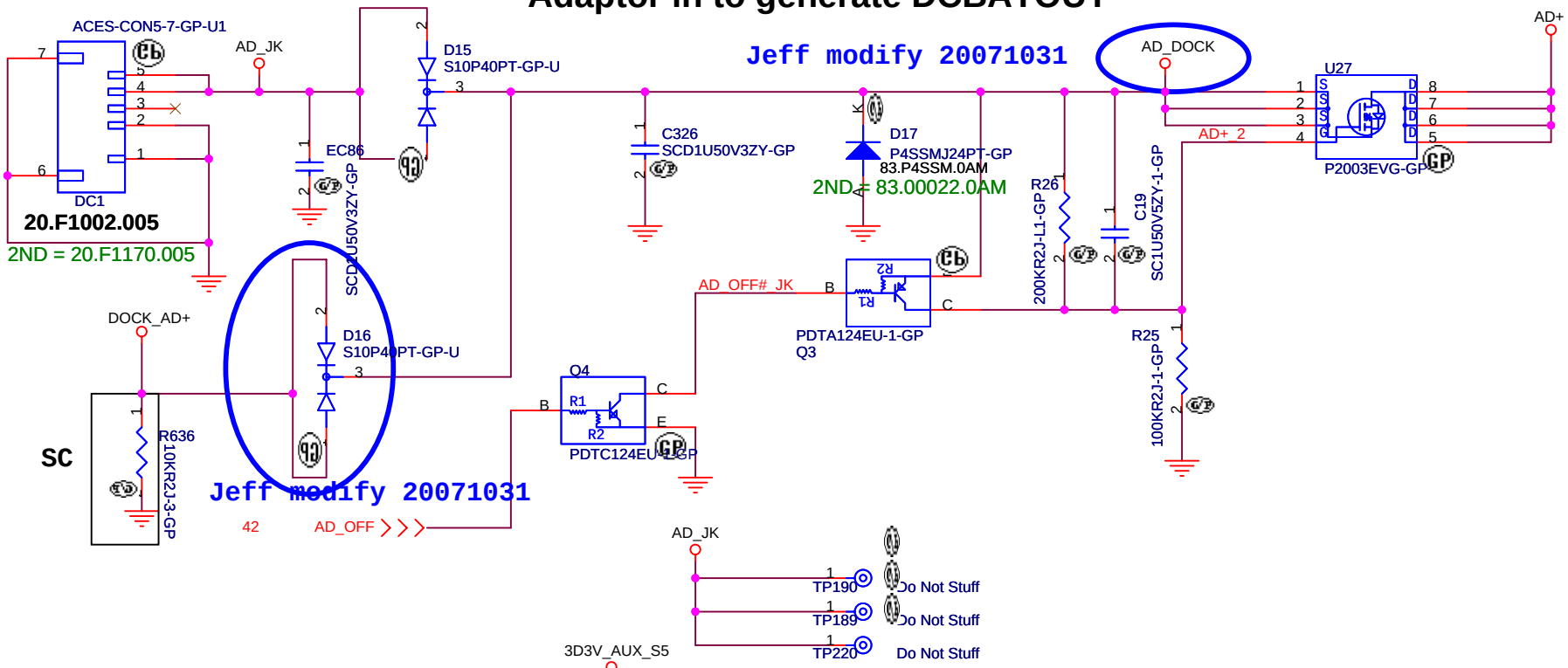
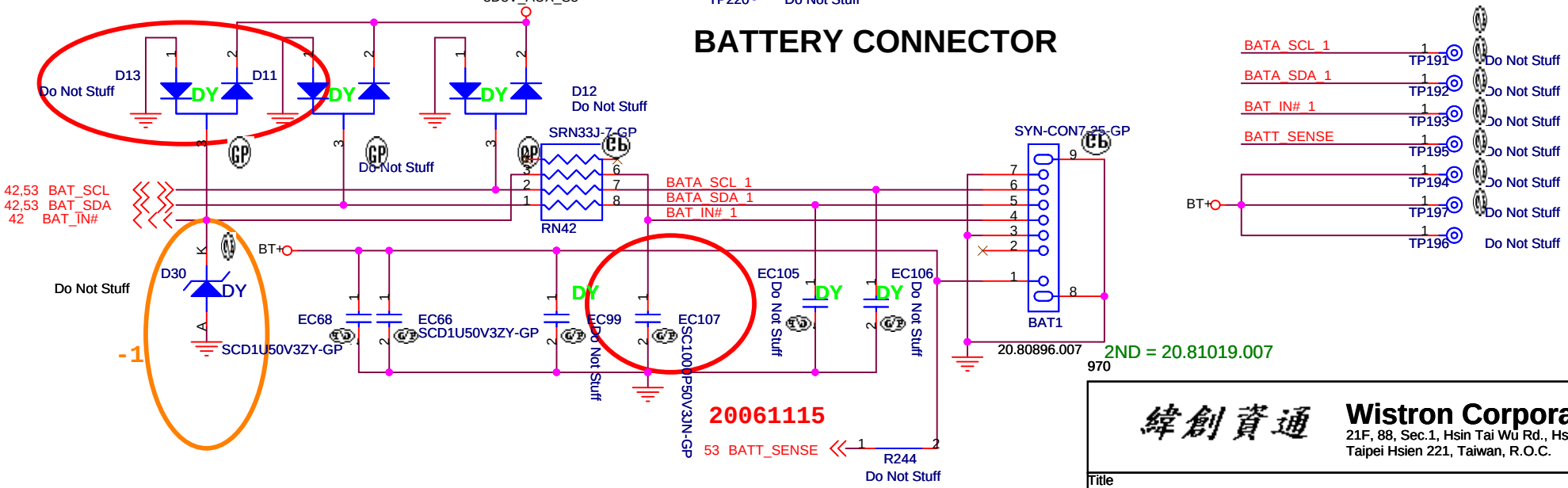

NEAR
AD+
U28
P2003EVG-GP
R381
10KR2F-2-GP
R28
100KR2J-1-GP
R382
10KR2F-2-GP
AD+_G_2
AD+_G_1
DC_IN_D
Q23
2N7002KDW-GP
84.2N702.A3F
2ND = 84.00512.03F
AC_OK
AD+_TO_SYS
Jeff MOdify 1001
R199
Do Not Stuff
C210
SCD1U25V5KX-1GP
R203
309KR3F-GP
CHG_AGND
R36
D01R2512F-4-GP
G11
G12
Do Not Stuff
DCBATOUT
BT+
U44
P2003EVG-GP
R513
470KR2J-2-GP
C588
SCD1U25V2ZY-1GP
Vendor suggest added decoupling capacitor in CSSN to ground.
C863
-1
SCD1U25V3KX-GP
SCD1U50V3KX-GP
C211
C212
BQ24745_CSSP
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
R200
49K9R2F-L-GP
C215
SCD01U50V2KX-1GP
C241
SC1U10V3KX-3GP
R218
Do Not Stuff
BQ24745_ACOK
AC_OK
42,54 BAT_SCL
42,54 BAT_SDA
phoenix tsai 09/28/07
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
U14
BQ24745RHDR-GP
BQ24745_CSSN
TP49
BQ24745_BST
BQ24745_VDDP
R197
BQ24745_BST1
CH520S-30PT-GP
D9
C224
SC1U10V3KX-3GP
24745_HIGH_G
MAX8731A_LX1
C213
24745_LOW_G
L12
IND-5D6UH-32-GP
U40
SI4800BDY-T1
U39
SI4800BDY-T1
C512
SCD1U25V2ZY-1GP
TC31
TC32
SE100U25VM-L1-GP
BT+_R
R210
D01R2512F-4-GP
C247
C249
C602
C609
C612
SC10U25V6KX-1GP
SCD1U50V3KX-GP
G18
G19
Do Not Stuff
C230
MAX8731A_CSIP
MAX8731A_CSIN
AD_IA
R226
Do Not Stuff
SC150P50V2JN-3GP
C238
BQ24745_FBO_RC
4K7R2J-2-GP
R219
BQ24745_FBO
R215
200KR2F-1-GP
C232
SC2200P50V2KX-2GP
R205
7K5R2F-1-GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BQ24745_EAO_RC
C226
SC1U10V3KX-3GP
C234
SC56P50V2JN-2GP
C243
SC220P50V2KX-3GP
BQ24745_IINP
BATT_SENSE
BATT_SENSE_54
C236
SCD1U25V2ZY-1GP
AC_IN# to KBC
AC_IN#
CHG_ON#
C216
SC1U10V3KX-3GP
Q13
2N7002KDW-GP
84.2N702.A3F
2ND = 84.00512.03F
C240
Do Not Stuff
DY
3D3V_AUX_S5
RN95
SRN100K5-GP
AC_IN#
CHG_ON#
BQ24745_CHG_ON
AC_OK
BQ24745_VREF
R196
Do Not Stuff
970
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BQ24745 Charger
Size
A3
Document Number
Homa
Rev
-1
Date: Thursday, April 03, 2008
Sheet 53 of 57

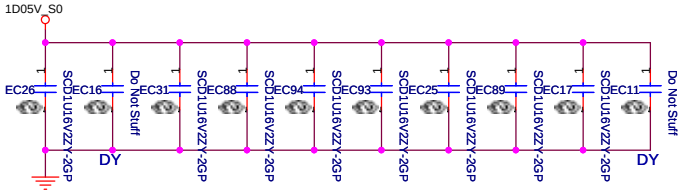
Adaptor in to generate DCBATOUT

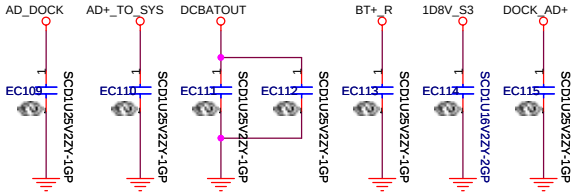


BATTERY CONNECTOR



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AD/BATT CONN
Size	Document Number: Homa
Rev	-1
Date: Thursday, April 03, 2008	Sheet 54 of 57





Check test point

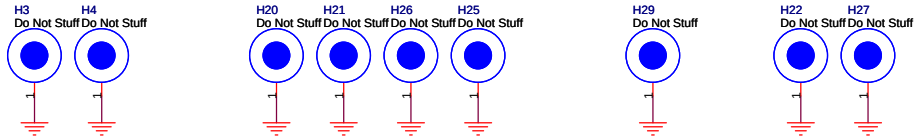
Test Point放在Dimm Door打開可量測處

SC

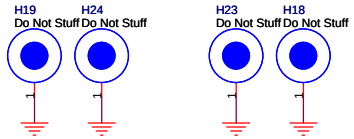
SC

Stand off Location

34.42Y01.031

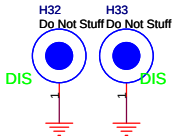


34.4G502.021

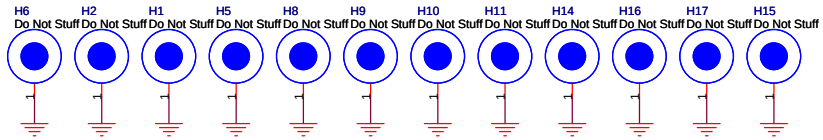


34.4Z402.011

34.4Z401.011



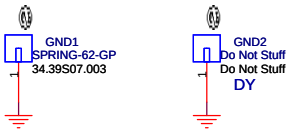
DELETE MXM
STAND-OFF
H7;H28;H30;H31



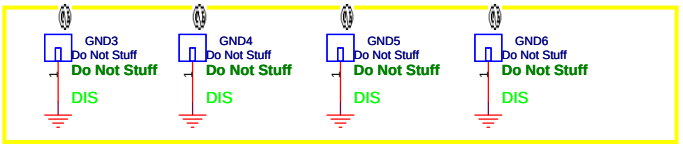
SC

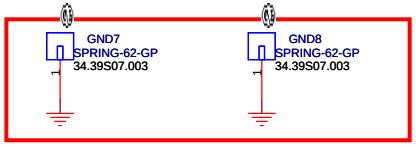
SPRING ON BOTTOM

DIMM **Heat Sink**



MXM SPRING -1 20080307





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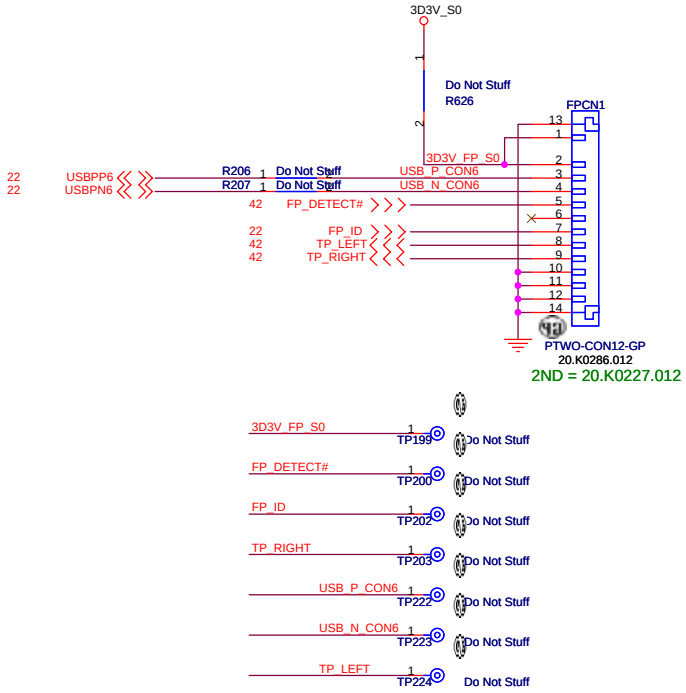

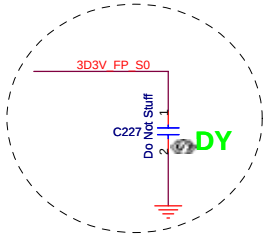

For EMI

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SA --> SB

1.page25,Change Q24 and Q5 Pin_C and Pin_E net, Swap H_THERMDA and H_THERMDC(only close to C95)
2.page46,Change R145_Pin1 pull hige power to 1D05V_S0
3.page42,Add the Net let link U17_Pin101 and RN45_Pin3
4.page16,SWITCHCN1 pin12 connect to 3D3V_AUX_S5 and pin 11 connect to LID_CLOSE#
5.page20,HDMI1 change to 62.10078.171
6.page44,DOCK1 pin51 connect to CRT_DEC#
7.page53,R214 change to connect BQ24745_VREF as charger modify
8.page26,change ODD1 to 22.10300.141
9.page45,change U12 to PS8122QFN48G-GP and add some components
10.page44,Del U5
11.page20,Del U11,U42,Q9….
12.del G1~G8
13.page45,R614 changed to “DOCK_DT1#” and U12 output port1 and port2 swap,RN68 pin1&2 change to KBC SMBUS,
RN69 pin3&4 change to connect”3D3V_S0”,R615 change to 4K7R2F-GP
14.page49,change Q27&Q28 to 2N7002SPT ,add R595 R616
15.page48,change R12 to 10K2R3F-GP ,R13 to 16K5R2F-1-GP
16.page51,R578 change to 22K1R3-GP
17.page52,R257 change to 2K87R2F-1-GP ,C259 change to SCD033U50V
18.page40,change U8 to G1454R41U-GP
19.page42,Del R29 R27 C20 EC5
20.page41,LID1 change to INTMIC1 and connect to “MIC_L_CN”&”MIC_R_CN”
21.page39,add R619 C815 R621 R620 C816 C817
22.page38,Del C355 C320
23.page56,Del F4 addR626
24.page3,R204 change to connect”3D3V_CLKPLL_S0”
25.page52,add R622~R625
26.page44,add C818~C822 and L19 L20 L21
27.page35,Del TP77~TP82 TP84 TP86 TP87 TP24 TP25 TP26 TP28,add R618 pull up to 3D3V_S0
28.page25,add R617 Q35 del R115
29.page30,change C600 to 4.7U10V
30.page45, swap U12 output port1&pot2
31.page48~52, change power GAPs to close GAPs
32.page49,L15 change to 1ND-3D3UH by power modify
33.page16,add R627 EC108
34.page45,add C823 C824   and R144 R151 Q9 R137

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