1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
4	0011084069	ENGINEERING RELEASED	2018-01-26

SCHEM,MLB,X1190

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43	44	SoC Power 2	H9M and PMIC	03/02/2017
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46	47	SoC Shared Support	SILU	08/09/2017
47	48	SoC Project Support	SILU	07/27/2017
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49	50	Secure Element	SILU	05/05/2017
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65	67	Keyboard & Trackpad 1	j132	03/23/2017
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67	69	VR 3.3V G3H & Battery Conn	SILU	04/27/2017
68	70	PBUS Supply & Battery Charger	ZIFENG	05/24/2017
69	71	IMVP IC	SILU	05/24/2017
70	72	IMVP VCC Block	SILU	05/24/2017
71	73	IMVP SA Block	SILU	05/10/2017
72	74	IMVP GT Block	SILU	05/24/2017
73	76	Power - 5V 3.3V Supply	SILU	05/16/2017
74	77	VR 2.5V & 1.2V/VTT	SILU	05/01/2017
75	78	PMIC BUCKS AND SWs	SILU	06/06/2017
76	79	PMIC LDOs	SILU	07/10/2017
77	80	PMIC GPIOs & Control	SILU	07/27/2017
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79	82	Power FETs	SILU	06/27/2017
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95	100	GPU Baffin PCIe	SEAN	11/09/2017
96	101	GPU Baffin Core/FB Power	SEAN	06/21/2017
97	102	GPU Baffin FB	SEAN	04/19/2017
98	103	VR 1.05V GPU & 1.35V FB	SILU	04/27/2017
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100	105	GDDR5 VRAM FB 2	SEAN	04/19/2017
101	106	VR GPU Core	SILU	05/24/2017
102	107	GPU Baffin GPIO/CLK/Straps	SEAN	04/19/2017
103	108	GPU Baffin DP/GPIO	SILU	07/27/2017
104	109	GPU Baffin VSS/Misc	SEAN	11/09/2017
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108	113	USB-C PORT CONTROLLER A	ZIFENG	05/26/2017
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111	116	USBC T Connector Support	ADITYA	04/05/2017
112	117	USB-C T 5V VR	SILU	05/11/2017
113	118	GDDR5 VRAM FB 3	j680_copy	02/01/2017
114	119	GDDR5 VRAM FB 4	j680_copy	02/01/2017
115	120	Power Alias 1	SILU	05/01/2017
116	121	Power Alias 2	SILU	06/27/2017
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118	123	High speed No Testpoints	RAYMOND	06/02/2017
119	124	DFU TEST POINTS	RAYMOND	08/07/2017
120	125	FCT TESTPOINTS 2	RAYMOND	08/07/2017
121	126	ICT, MAC-1 ,EE Testpoints	RAYMOND	08/31/2017
122	127	Desense Caps 1	SEAN	06/27/2017
123	128	Desense Caps 2	j380_mlb	02/09/2017
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125	130	Memory Bite/Byte Swizzle	j380_mlb	02/09/2017
126	140	Dev Support	Debug	05/03/2017
127	141	BOM-639 2.2GHz	SEAN	11/29/2017
128	143	BOM-639 2.6GHz	j380_mlb	02/09/2017
129	144	BOM-639 2.9GHz	j380_mlb	02/09/2017
130	147	BOM Alt Table	SEAN	11/29/2017
131	200	Dev Support	ADITYA	03/22/2017

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LAST_MODIFICATION=Fri Jan 26 13:24:05 2018

LAST_MODIFICATION=Fri Jan 26 13:24:05 2018

DRAWING

TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Fri Jan 26 13:24:05 2018

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION

DRAWING TITLE: SCHEM,MLB,X1190

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X1190 BOM Groups

BOM GROUP	BOM OPTIONS
X1190_8L	ALTERNATE,S4E_L5,S4E_L6,S4E_L7,S4E_L8,OCARINA_2,S4E_X4PLUS,S4E_X8
X1190_6L	ALTERNATE,S4E_L5,S4E_L6,OCARINA_2,S4E_X4PLUS,S4E_X6
X1190_COMMON	SCH,PCB,COMMON,ALTERNATE,X1190_COMMON1,X1190_COMMON2,X1190_PROGPARTS,VRAM_ALTS
X1190_COMMON1	CPUPEG:X8X4X4,EDP:YES,BOARD_ID,BOARD_REV:011,SE:PROD_2017,EN_VP0R_LPS:YES
X1190_COMMON2	SKIP_5V3V3:AUDIBLE,XDP:YES,SYSDET:FET,VCCSPI:3V3,OCARINA_I2C:1K,SVID_PU:CORE,RF_TUNING,PBUS:3S
X1190_PROGPARTS	UPCROM_PROG:P1,WIFI_ROM:P0,BT_ROM:P2
X1190_SNS	LOADISNS,LOADRC:YES,SENSOR:DEV
X1190_DEVEL:ENG	ALTERNATE,X1190_SNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,WIFI_DBG,DBG_FAN,GPUROM:BLANK,VITAMIN-C:YES,PCC:YES,GPU_ROM:YES,BOOTCFG0
X1190_DEVEL:DVT	ALTERNATE,LOADRC:NO
X1190_DEVEL:PVT	ALTERNATE,LOADRC:NO

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00179	COMMON PARTS,MLB,X1190	X1190_COMMON
685-00193	S4E 8L Parts,MLB,X1190	X1190_8L
685-00198	S4E 6L Parts,MLB,X1190	X1190_6L
985-00362	DEV,MLB,X1190	X1190_DEVEL:ENG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00179	1	COMMON PARTS, MLB, X1190	BASE	CRITICAL	BASE_BOM
685-00193	1	S4E 8L PARTS (8L),MLB,X1190	8L	CRITICAL	BOM_8L
985-00362	1	DEV PARTS,MLB,X1190	DEVEL	CRITICAL	DEVEL_BOM
685-00198	1	S4E 6L PARTS (6L),MLB,X1190	6L	CRITICAL	BOM_6L

DRAM Options

BOM GROUP	BOM OPTIONS
MC_32G	32G_MICRON_2400,RAMCFG4:L,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L
HY_32G	32G_HYNIX_2400,RAMCFG4:L,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
HY_16G	16G_HYNIX_2400,RAMCFG4:L,RAMCFG3:L,RAMCFG1:L,RAMCFG0:L
MC_16G	16G_MICRON_2400,RAMCFG4:L,RAMCFG3:L,RAMCFG1:L

S4E Options

BOM GROUP	BOM OPTIONS
TS_256_PMLC	S4E_256_TB,SOC:1GB,SSD0_NAND_VCC:2.5V
WD_256_PMLC	S4E_256_WD,SOC:1GB,SSD0_NAND_VCC:2.5V
TS_512_PMLC	S4E_512_TB,SOC:1GB,SSD0_NAND_VCC:2.5V
WD_512_PMLC	S4E_512_WD,SOC:1GB,SSD0_NAND_VCC:2.5V
TS_1TB_PMLC	S4E_1TB_TB,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V
WD_1TB_PMLC	S4E_1TB_WD,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V
TS_2TB_PMLC	S4E_2TB_TB,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V
WD_2TB_PMLC	S4E_2TB_WD,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V
SM_2TB_3DV4	S4E_2TB_SM,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V
SM_4TB_3DV4	S4E_4TB_SM,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V
TS_2TB_TLC	TLC_2TB_TB,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V
WD_2TB_TLC	TLC_2TB_WD,SOC:2GB,SSD0_NAND_VCC:2.5V,SSD1_NAND_VCC:2.5V

BOARD ID

BOM GROUP	BOM OPTIONS
BOARD_ID	BOARDID0,BOARDID1,BOARDID3

VRAM ALT BOM GROUPS

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00221	VRAM PARTS,HYNIX,2X,MLB,X1190	FB_4GB_HYNIX
685-00222	VRAM PARTS,MICRON,2X,MLB,X1190	FB_4GB_MICRON
685-00223	VRAM PARTS,SAMSUNG,2X,MLB,X1190	FB_4GB_SAMSUNG
685-00224	VRAM PARTS,HYNIX,1Z,MLB,X1190	FB_4GB_HYNIX_1Z
685-00225	VRAM PARTS,MICRON,1Z,MLB,X1190	FB_4GB_MICRON_1Z

VRAM SUB-BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00221	1	VRAM PARTS,HYNIX,2X,MLB,X1190	VRAMSSSS	CRITICAL	VRAM_ALTS

SYNC_MASTER=SEAN SYNC_DATE=11/29/2017

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BOM Configuration 1

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GPU Baffin

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00493	1	GPU,AMD,BAFFIN,ULX,A3,0.83,QS,BGA769	UA000	CRITICAL	BAFFIN_ULX
337S00494	1	GPU,AMD,BAFFIN,PROX,A3,0.83,QS,BGA769	UA000	CRITICAL	BAFFIN_PROX
998-04866	1	INTERPOSER,AMD,C989,BGA769,VDDCI/MVDD	UA000	CRITICAL	STARDUST:VDDCI_MVDD
998-04867	1	INTERPOSER,AMD,C988,BGA769,VDDC	UA000	CRITICAL	STARDUST:VDDC

FB VDRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00074	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,B,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_SAMSUNG
333S00075	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_MICRON
333S00100	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_HYNIX
333S00173	4	IC,GDDR5,8Gb,7Gbps,1.5V,1ZNM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_MICRON_1Z
333S00175	4	IC,GDDR5,8Gb,7Gbps,1.5V,1ZNM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_HYNIX_1Z

CPU Parts CFL (Needs to be updated)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00509	1	CPU,CFLH,QP87,QS,U0,2.2,45W,1.1,LGA1440	U0500	CRITICAL	CPU_CFL:2.2
337S00510	1	CPU,CFL-H,QP86,QS,U0,2.6,6C,45W,1.15,BGA1440	U0500	CRITICAL	CPU_CFL:2.6
337S00513	1	CPU,CFL-H,QPQG,QS,U0,2.9,6C,45W,1.2,BGA1440	U0500	CRITICAL	CPU_CFL:2.9
998-12472	1	INTERPOSER,CFH-H,BGA1440	U0500	CRITICAL	CPU_SKL:SOCKET

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00131	16	IC,SDRAM,DDR4-2400,16GBIT,20NM,BGA78	———————————	CRITICAL	32G_MICRON_2400
333S00134	16	IC,SDRAM,DDR4-2400,16GBIT,20NM,BGA78	———————————	CRITICAL	32G_HYNIX_2400
333S00147	16	IC,SDRAM,DDR4-2400,8GBIT,20NM,BGA78	———————————	CRITICAL	16G_HYNIX_2400
333S00163	16	IC,SDRAM,DDR4-2400,8GBIT,20NM,BGA78	———————————	CRITICAL	16G_MICRON_2400

PCH CNL-H (Needs to be updated)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00523	1	IC,CNL,PCH-H,USFF,QNYP,QS,B0,BGA499	U1200	CRITICAL	

ACE & Ridges (Needs to Be Updated)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S01442	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	
338S00408	2	IC,TBT,TITAN RIDGE DP,QUJK,QS,C1,CSP337	U2800,UB000	CRITICAL	

Hall Effect AMR

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
677-10608	2	SUBASSY T600 PCBA, AMR, INTERPOSER, X1190	J4800,J4801	CRITICAL	

Power Controllers

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S01525	1	IC,ISL9240HIB1Z,PMU,SOUNA,WCSP40,2.1X3.3MM	U7000	CRITICAL	
338S00267	1	IC,PMU,P650839,7X7MM.BGA168	U7800	CRITICAL	
353S01229	1	IC,SUPPLY,INTERSIL,ISL6277AHRZ,SVI2.0,QFN48	UA600	CRITICAL	
353S00928	1	IC,ISL95828A,IMVP8 CPU REG,QFN48,6X6MM	U7100	CRITICAL	

Harpoon

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00458	1	IC,MODULE,WIFI/BT,MURATA,HARPOON,M,ES7.7,LGA385	U3730	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00428	339S00458		ALL	IC,MODULE,WIFI/BT,HARPOON,USI,ES7.5,LGA385

USB-C Connector

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-12556	2	CONN,RCPT,56+4,P=0.35,H=0.7,SHLD,THKR	J3300,JB500	CRITICAL	

Ocarina

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00410	1	IC,PMU,OCARINA,D2499A0,OTP-AG,WLCSP56	U9000	CRITICAL	
338S00410	1	IC,PMU,OCARINA,D2499A0,OTP-AG,WLCSP56	U9500	CRITICAL	OCARINA_2

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
335S00199	1	IC,1Mbit SERIAL FLASH 2X3X0.6MM UFDFPN8 PKG	UA701	CRITICAL	GPUROM:BLANK	
341S01017	1	T29,TR1(V2.1),NEW-PROTO-2,X1190	U2890	CRITICAL	UPCROM_PROG:P1	Updated-P1
341S01018	1	T29,TR2(V2.1),NEW-PROTO-2,X1190	UB090	CRITICAL	UPCROM_PROG:P1	Updated-P1
341S01025	1	IC, BT ROM, EVT,VXX, X1190	U3750	CRITICAL	BT_ROM:P2	Updated
341S00725	1	IC, WIFI ROM, PROTO0, X1190	U3710	CRITICAL	WIFI_ROM:P0	Updated

H9M

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00373	1	POP,GIBRALTAR+2GB 21NM,H,B0,SCK,CSP1406	U3900	CRITICAL	SOC:2GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00373	339S00372		ALL	2GB,20NM,M,B0,SCK,CSP1406
339S00378	339S00372		ALL	2GB,21NM,H,B0,ATK,CSP1406
339S00377	339S00372		ALL	2GB,20NM,M,B0,ATK,CSP1406

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00376	1	POP,GIBRALTAR+1GB 21NM,H,B0,ATK,CSP1406	U3900	CRITICAL	SOC:1GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00375	339S00376		ALL	1GB,20NM,M,B0,ATK,CSP1406
339S00371	339S00376		ALL	1GB,21NM,H,B0,SCK,CSP1406
339S00370	339S00376		ALL	1GB,21NM,M,B0,SCK,CSP1406

S4E Parts

256GB

335S00324	4	NAND,3DV3,85GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	S4E_256_WD
998-12418	4	NAND,3DV3,85GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	S4E_256_TB

998-12419	998-12418		ALL	SUBW

512GB

335S00325	4	NAND,3DV3,128GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	S4E_512_WD
998-12420	4	NAND,3DV3,128GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8700,U8800,U8900	CRITICAL	S4E_512_TB

998-12421	998-12420		ALL	SUBW

1TB

335S00326	6	NAND,3DV3,170GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900,U9100,U9200	CRITICAL	S4E_1TB_WD
998-12422	6	NAND,3DV3,170GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8700,U8800,U8900,U9100,U9200	CRITICAL	S4E_1TB_TB

998-12423	998-12422		ALL	SUBW

2TB

335S00327	8	NAND,3DV3,256GBP,XXX,S4E,170G,SD,ULGA110	U8600,U8700,U8800,U8900,U9100,U9200,U9400	CRITICAL	S4E_2TB_WD
335S00321	8	NAND,3DV4,256GBP,XXX,S4E,256G,SS,ULGA110	U8600,U8700,U8800,U8900,U9100,U9200,U9400	CRITICAL	S4E_2TB_SM
998-12424	8	NAND,3DV3,256GBP,S4E,170G,T,SUBX,ULGA110	U8600,U8700,U8800,U8900,U9100,U9200,U9400	CRITICAL	S4E_2TB_TB

998-12426	998-12424		ALL	SUBW

4TB

335S00322	8	NAND,3DV4,512GBP,S4E,256G,SS,ULGA110	U8600,U8700,U8800,U8900,U9100,U9200,U9400	CRITICAL	S4E_4TB_SM

2TB TLC

335S00228	8	NAND,3DV3,256GBT,S4E,256G,SD,ULGA110	U8600,U8700,U8800,U8900,U9100,U9200,U9300,U9400	CRITICAL	TLC_2TB_TB
335S00247	8	NAND,3DV3,256GBT,S4E,256G,SD,SLGA110	U8600,U8700,U8800,U8900,U9100,U9200,U9300,U9400	CRITICAL	TLC_2TB_WD

PAGE TITLE

BOM Configuration 2

Apple Inc.

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Bumpers

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
860-00986	1	bumper 1	BM0411	CRITICAL	
860-00948	1	bumper 2	BM0400	CRITICAL	
860-00954	5	bumper 3	BM0484,BM0485,BM0486,BM0487,BM0488	CRITICAL	
860-00949	11	bumper 4	BM0401,BM0402,BM0403,BM0406,BM0410,BM0407,BM0408,BM0483,BM0405,BM0409,BM0404	CRITICAL	

Shield Cans

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-11170	1	SHIELD,FENCE,DIPLEX,X1181	SH0400	CRITICAL	
806-13323	2	SHIELD,FENCE,NAND_L5_L6,X1181	SH0401,SH0402	CRITICAL	S4E_X6
806-13323	4	SHIELD,FENCE,NAND_L5_L6_L7_L8,X1181	SH0401,SH0402,SH0403,SH0404	CRITICAL	S4E_X8
806-13325	1	SHIELD,FENCE,H9M,X1181	SH0405	CRITICAL	
806-13326	1	SHIELD,FENCE,VRAM,X1181	SH0406	CRITICAL	
806-13327	1	SHIELD,FENCE,TR,RT,X1181	SH0407	CRITICAL	
806-13328	2	SHIELD,FENCE,NAND_L1_L2_L3_L4,X1181	SH0408,SH0409	CRITICAL	
806-13329	1	SHIELD,FENCE,TR,LT,X1181	SH0410	CRITICAL	
806-13324	2	SHIELD,FENCE,DRAM,X1181	SH0411,SH0412	CRITICAL	
806-13996	2	SHIELD,SLED,GPU,X1181	SH0413,SH0415	CRITICAL	
806-13997	2	SHIELD,SLED,CPU,X1181	SH0414,SH0416	CRITICAL	

BOM_COST_GROUP=MECHANICALS

PAGE TITLE
PD Parts

Apple Inc.

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From Intel EDS
PEG RCOMP Range = 24.76,25.25
Voltage = VCCIO (Page 121, Note 3)

PPVCCIO_S0_CPU 5 8 10 115

R0510 24.9 1% 1/16W MF-LF 402 — PLACE_NEAR=U0500.G2:5mm

U0500 CFL-H_DDR4-IL
BGA 45W SYM 1 OF 13 CRITICAL OMIT_TABLE

DMI_S2N_N<0>	IN	E8	DMI_RXN0	PEG_RCOMP	G2	CPU_PEG_RCOMP
DMI_S2N_N<1>	IN	F6	DMI_RXN1			
DMI_S2N_N<2>	IN	E5	DMI_RXN2	PEG_RXN0	D25	PEG_GPU_D2R_N<0> IN 117
DMI_S2N_N<3>	IN	J9	DMI_RXN3	PEG_RXN1	F24	PEG_GPU_D2R_N<1> IN 117
DMI_S2N_P<0>	IN	D8	DMI_RXP0	PEG_RXN2	D23	PEG_GPU_D2R_N<2> IN 117
DMI_S2N_P<1>	IN	E6	DMI_RXP1	PEG_RXN3	F22	PEG_GPU_D2R_N<3> IN 117
DMI_S2N_P<2>	IN	D5	DMI_RXP2	PEG_RXN4	D21	PEG_GPU_D2R_N<4> IN 117
DMI_S2N_P<3>	IN	J8	DMI_RXP3	PEG_RXN5	F20	PEG_GPU_D2R_N<5> IN 117
DMI_N2S_N<0>	OUT	A8	DMI_TXN0	PEG_RXN6	D19	PEG_GPU_D2R_N<6> IN 117
DMI_N2S_N<1>	OUT	B6	DMI_TXN1	PEG_RXN7	F18	PEG_GPU_D2R_N<7> IN 117
DMI_N2S_N<2>	OUT	A5	DMI_TXN2	PEG_RXN8	E17	PCIE_TBT_X_D2R_N<0> IN 117
DMI_N2S_N<3>	OUT	B4	DMI_TXN3	PEG_RXN9	E16	PCIE_TBT_X_D2R_N<1> IN 117
DMI_N2S_P<0>	OUT	B8	DMI_TXP0	PEG_RXN10	E15	PCIE_TBT_X_D2R_N<2> IN 117
DMI_N2S_P<1>	OUT	C6	DMI_TXP1	PEG_RXN11	E14	PCIE_TBT_X_D2R_N<3> IN 117
DMI_N2S_P<2>	OUT	B5	DMI_TXP2	PEG_RXN12	E13	PCIE_TBT_T_D2R_N<0> IN 117
DMI_N2S_P<3>	OUT	D4	DMI_TXP3	PEG_RXN13	E12	PCIE_TBT_T_D2R_N<1> IN 117
				PEG_RXN14	E11	PCIE_TBT_T_D2R_N<2> IN 117
				PEG_RXN15	E10	PCIE_TBT_T_D2R_N<3> IN 117
				PEG_RXP0	E25	PEG_GPU_D2R_P<0> IN 117
				PEG_RXP1	E24	PEG_GPU_D2R_P<1> IN 117
				PEG_RXP2	E23	PEG_GPU_D2R_P<2> IN 117
				PEG_RXP3	E22	PEG_GPU_D2R_P<3> IN 117
				PEG_RXP4	E21	PEG_GPU_D2R_P<4> IN 117
				PEG_RXP5	E20	PEG_GPU_D2R_P<5> IN 117
				PEG_RXP6	E19	PEG_GPU_D2R_P<6> IN 117
				PEG_RXP7	E18	PEG_GPU_D2R_P<7> IN 117
				PEG_RXP8	D17	PCIE_TBT_X_D2R_P<0> IN 117
				PEG_RXP9	F16	PCIE_TBT_X_D2R_P<1> IN 117
				PEG_RXP10	D15	PCIE_TBT_X_D2R_P<2> IN 117
				PEG_RXP11	F14	PCIE_TBT_X_D2R_P<3> IN 117
				PEG_RXP12	D13	PCIE_TBT_T_D2R_P<0> IN 117
				PEG_RXP13	F12	PCIE_TBT_T_D2R_P<1> IN 117
				PEG_RXP14	D11	PCIE_TBT_T_D2R_P<2> IN 117
				PEG_RXP15	F10	PCIE_TBT_T_D2R_P<3> IN 117
				PEG_TXN0	A25	PEG_GPU_R2D_C_N<0> OUT 117
				PEG_TXN1	C24	PEG_GPU_R2D_C_N<1> OUT 117
				PEG_TXN2	A23	PEG_GPU_R2D_C_N<2> OUT 117
				PEG_TXN3	C22	PEG_GPU_R2D_C_N<3> OUT 117
				PEG_TXN4	A21	PEG_GPU_R2D_C_N<4> OUT 117
				PEG_TXN5	C20	PEG_GPU_R2D_C_N<5> OUT 117
				PEG_TXN6	A19	PEG_GPU_R2D_C_N<6> OUT 117
				PEG_TXN7	C18	PEG_GPU_R2D_C_N<7> OUT 117
				PEG_TXN8	B17	PCIE_TBT_X_R2D_C_N<0> OUT 117
				PEG_TXN9	B16	PCIE_TBT_X_R2D_C_N<1> OUT 117
				PEG_TXN10	B15	PCIE_TBT_X_R2D_C_N<2> OUT 117
				PEG_TXN11	B14	PCIE_TBT_X_R2D_C_N<3> OUT 117
				PEG_TXN12	B13	PCIE_TBT_T_R2D_C_N<0> OUT 117
				PEG_TXN13	B12	PCIE_TBT_T_R2D_C_N<1> OUT 117
				PEG_TXN14	B11	PCIE_TBT_T_R2D_C_N<2> OUT 117
				PEG_TXN15	B10	PCIE_TBT_T_R2D_C_N<3> OUT 117
				PEG_TXP0	B25	PEG_GPU_R2D_C_P<0> OUT 117
				PEG_TXP1	B24	PEG_GPU_R2D_C_P<1> OUT 117
				PEG_TXP2	B23	PEG_GPU_R2D_C_P<2> OUT 117
				PEG_TXP3	B22	PEG_GPU_R2D_C_P<3> OUT 117
				PEG_TXP4	B21	PEG_GPU_R2D_C_P<4> OUT 117
				PEG_TXP5	B20	PEG_GPU_R2D_C_P<5> OUT 117
				PEG_TXP6	B19	PEG_GPU_R2D_C_P<6> OUT 117
				PEG_TXP7	B18	PEG_GPU_R2D_C_P<7> OUT 117
				PEG_TXP8	A17	PCIE_TBT_X_R2D_C_P<0> OUT 117
				PEG_TXP9	C16	PCIE_TBT_X_R2D_C_P<1> OUT 117
				PEG_TXP10	A15	PCIE_TBT_X_R2D_C_P<2> OUT 117
				PEG_TXP11	C14	PCIE_TBT_X_R2D_C_P<3> OUT 117
				PEG_TXP12	A13	PCIE_TBT_T_R2D_C_P<0> OUT 117
				PEG_TXP13	C12	PCIE_TBT_T_R2D_C_P<1> OUT 117
				PEG_TXP14	A11	PCIE_TBT_T_R2D_C_P<2> OUT 117
				PEG_TXP15	C10	PCIE_TBT_T_R2D_C_P<3> OUT 117

DMI
PCI EXPRESS BASED INTERFACE SIGNALS

U0500 CFL-H_DDR4-IL
BGA 45W SYM 11 OF 13 CRITICAL OMIT_TABLE

NC_DDI1_ML_C_N<0>	117	K37	DDI1_TXN0	EDP_AUXN	B26	DP_INT_IG_AUX_N 93 118
NC_DDI1_ML_C_P<0>	117	K36	DDI1_TXP0	EDP_AUXP	C26	DP_INT_IG_AUX_P 93 118
NC_DDI1_ML_C_N<1>	117	J34	DDI1_TXN1			
NC_DDI1_ML_C_P<1>	117	J35	DDI1_TXP1			
NC_DDI1_ML_C_N<2>	117	H36	DDI1_TXN2	EDP_TXN0	E29	DP_INT_IG_ML_N<0> 93 118
NC_DDI1_ML_C_P<2>	117	H37	DDI1_TXP2	EDP_TXN1	E28	DP_INT_IG_ML_N<1> 93 118
NC_DDI1_ML_C_N<3>	117	J38	DDI1_TXN3	EDP_TXN2	B29	DP_INT_IG_ML_N<2> 93 118
NC_DDI1_ML_C_P<3>	117	J37	DDI1_TXP3	EDP_TXN3	B28	DP_INT_IG_ML_N<3> 93 118
NC_DDI2_ML_C_N<0>	117	H33	DDI2_TXN0	EDP_TXP0	D29	DP_INT_IG_ML_P<0> 93 118
NC_DDI2_ML_C_P<0>	117	H34	DDI2_TXP0	EDP_TXP1	F28	DP_INT_IG_ML_P<1> 93 118
NC_DDI2_ML_C_N<1>	117	G38	DDI2_TXN1	EDP_TXP2	A29	DP_INT_IG_ML_P<2> 93 118
NC_DDI2_ML_C_P<1>	117	F37	DDI2_TXP1	EDP_TXP3	C28	DP_INT_IG_ML_P<3> 93 118
NC_DDI2_ML_C_N<2>	117	F35	DDI2_TXN2			
NC_DDI2_ML_C_P<2>	117	F34	DDI2_TXP2			
NC_DDI2_ML_C_N<3>	117	E36	DDI2_TXN3	DISP_RCOMP	D37	CPU_EDP_RCOMP
NC_DDI2_ML_C_P<3>	117	E37	DDI2_TXP3	EDP_DISP_UTIL	A33	NC
NC_DDI3_ML_N<2>	117	E33	DDI3_TXN2	DDI1_AUXN	F27	NC_DDI1_AUXCH_C_N 117
NC_DDI3_ML_P<2>	117	F33	DDI3_TXP2	DDI1_AUXP	D27	NC_DDI1_AUXCH_C_P 117
NC_DDI3_ML_N<3>	117	B33	DDI3_TXN3	DDI2_AUXN	F26	NC_DDI2_AUXCH_C_N 117
NC_DDI3_ML_P<3>	117	C33	DDI3_TXP3	DDI2_AUXP	F26	NC_DDI2_AUXCH_C_P 117
NC_DDI3_ML_N<0>	117	D34	DDI3_TXN0	DDI3_AUXN	B27	NC_DDI3_AUXCH_N 117
NC_DDI3_ML_P<0>	117	C34	DDI3_TXP0	DDI3_AUXP	A27	NC_DDI3_AUXCH_P 117
NC_DDI3_ML_N<1>	117	B34	DDI3_TXN1			
NC_DDI3_ML_P<1>	117	B36	DDI3_TXP1			

EDP
DIGITAL DISPLAY INTERFACES

Port D pins out of order to match Intel symbol.

PPVCCIO_S0_CPU 5 8 10 115

R0530 24.9 1% 1/16W MF-LF 402 — PLACE_NEAR=U0500.D37:5mm

TP0501	CPU_DC_B2_C1	B2 RSVD
TP0502	CPU_DC_B38_C38	B38 RSVD
		NC BP1 RSVD
TP0503	CPU_DC_BR2_BR1	BR2 RSVD
TP0504	CPU_DC_C1_B2	C1 RSVD
TP0505	CPU_DC_C38_B38	C38 RSVD
		NC BR33 SKTOCC*
		NC AT13 ZVM*
		NC AW13 MSM*

U0500 CFL-H-DDR4-IL
BGA 45W SYM 13 OF 13

IST_TRIG	E3	CPU_IST_TRIG	Impedance Spectrum Tool
PROC_TRIGIN	H23	PCH_CPU_TRIGGER	IN 13
PROC_TRIGOUT	J23	CPU_PCH_TRIGGER_R	5
PROC_AUDIO_CLK	G27	PCH_DISPA_BCLK	IN 29
PROC_AUDIO_SDI	G25	PCH_DISPA_SDO	IN 29
PROC_AUDIO_SDO	G29	CPU_PROC_AUD_SDO_R	5
DDR_VTT_CNTL	BT13	PM_MEMVTT_EN	OUT 74 119
PM_DOWN	BP31	CPU_PCH_PM_DOWN_R	5

TP0506 TP-P6 A
TP0507 TP-P6 A
PLACE_NEAR=TP0506.1:5mm

Each corner of CPU has two testpoints. Other corner test signals connected in daisy-chain fashion. Continuity should exist between both TP's on each corner.

R0524 30 5% 1/20W MF 201: 5 CPU_PCH_TRIGGER_R → CPU_PCH_TRIGGER OUT 13

R0525 20 5% 1/20W MF 201: 5 CPU_PCH_PM_DOWN_R → CPU_PCH_PM_DOWN OUT 13

R0526 20 5% 1/20W MF 201: 5 CPU_PROC_AUD_SDO_R → PCH_DISPA_SDI OUT 20

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

Apple Inc.

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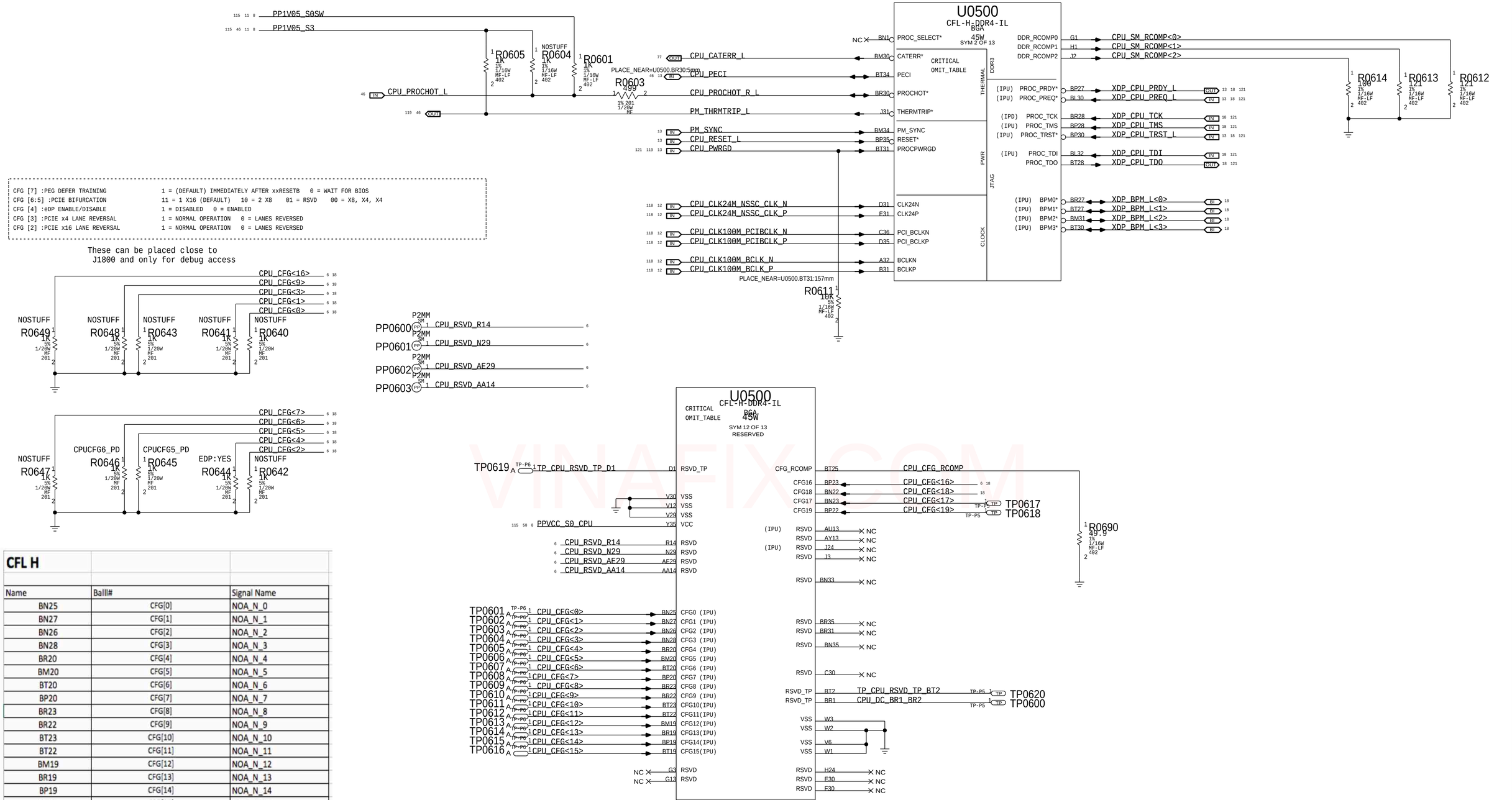


CFL H		
Name	Ball#	Signal Name
BN25	CFG[0]	NOA_N_0
BN27	CFG[1]	NOA_N_1
BN26	CFG[2]	NOA_N_2
BN28	CFG[3]	NOA_N_3
BR20	CFG[4]	NOA_N_4
BM20	CFG[5]	NOA_N_5
BT20	CFG[6]	NOA_N_6
BP20	CFG[7]	NOA_N_7
BR23	CFG[8]	NOA_N_8
BR22	CFG[9]	NOA_N_9
BT23	CFG[10]	NOA_N_10
BT22	CFG[11]	NOA_N_11
BM19	CFG[12]	NOA_N_12
BR19	CFG[13]	NOA_N_13
BP19	CFG[14]	NOA_N_14
BT19	CFG[15]	NOA_N_15
BN23	CFG[17]	NOA_STB_P_0
BP22	CFG[19]	NOA_STB_P_1
D1	RSVD_TP	PEG_VIEW0
E1	RSVD_TP	PEG_VIEW1
E2	RSVD_TP	PEG_VIEW3
E3	IST_TRIG	PEG_VIEW2
BT2	RSVD_TP	DDR_VIEW1
BR1	RSVD_TP	DDR_VIEW0

BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

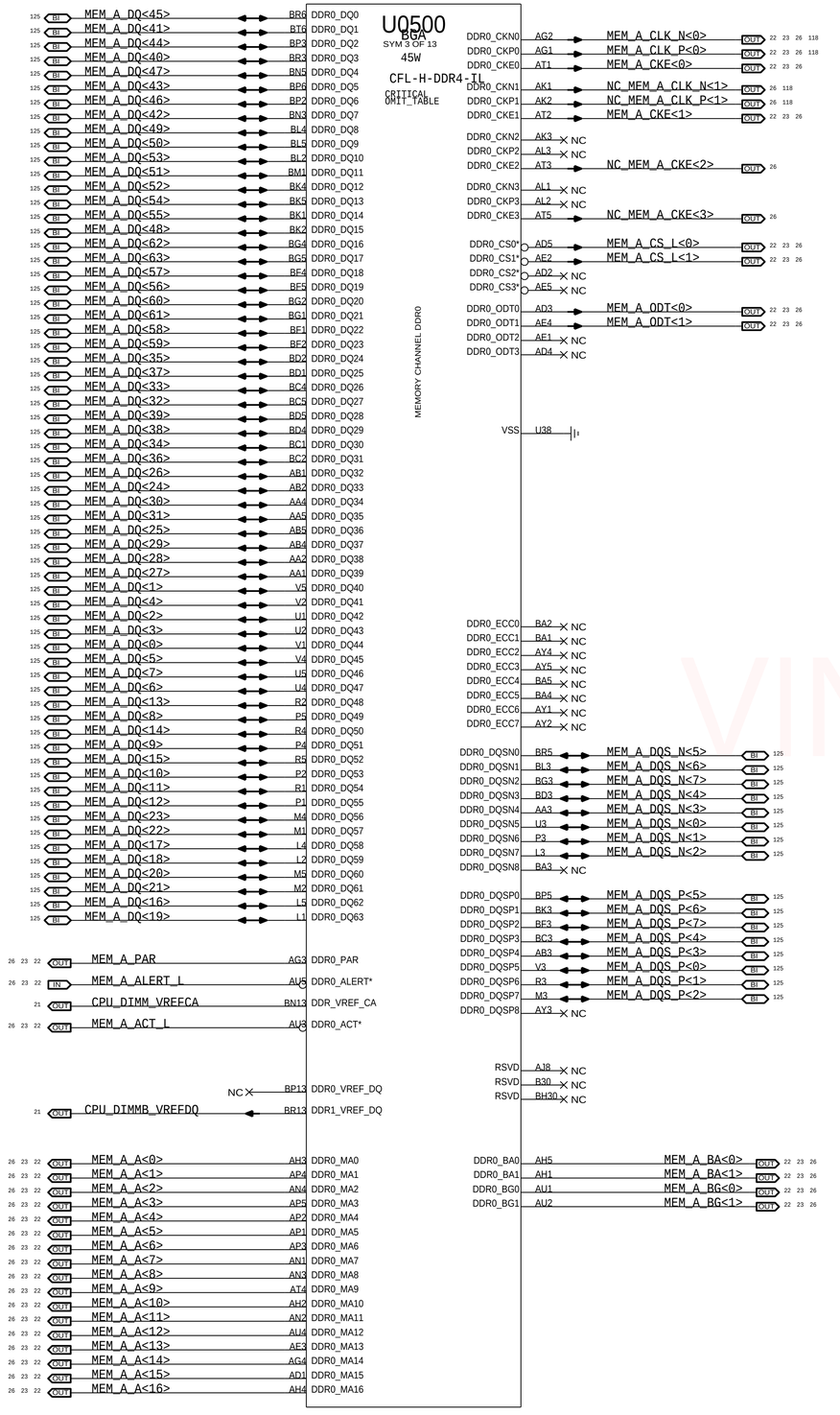
To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

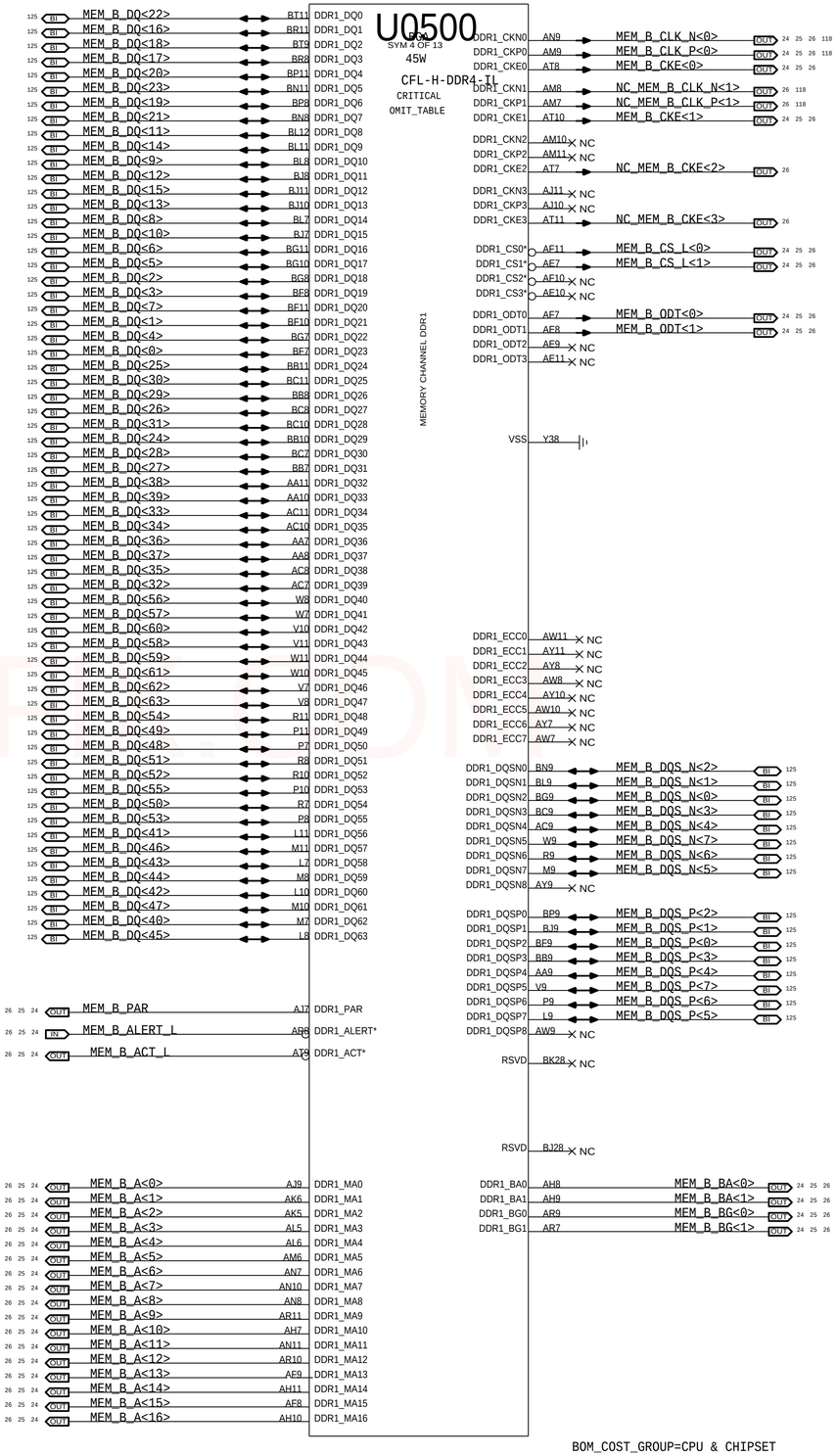
BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU Clock/Misc/JTAG/CFG

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
PAGE: 6 OF 200
SHEET: 6 OF 131





BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

CPU DDR4 Interfaces

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
REVISION 4.0.0
BRANCH evt-0
PAGE 7 OF 200
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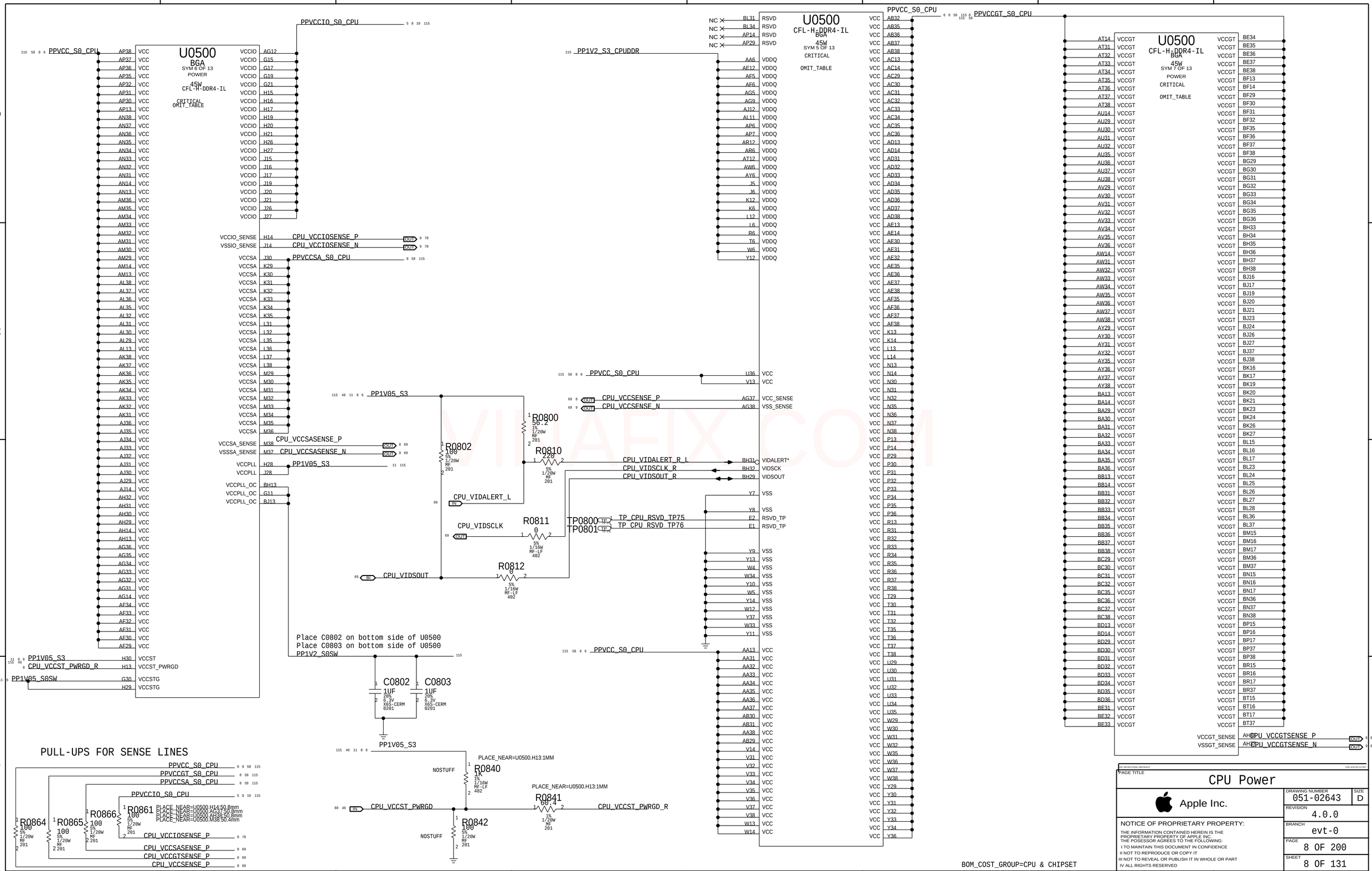

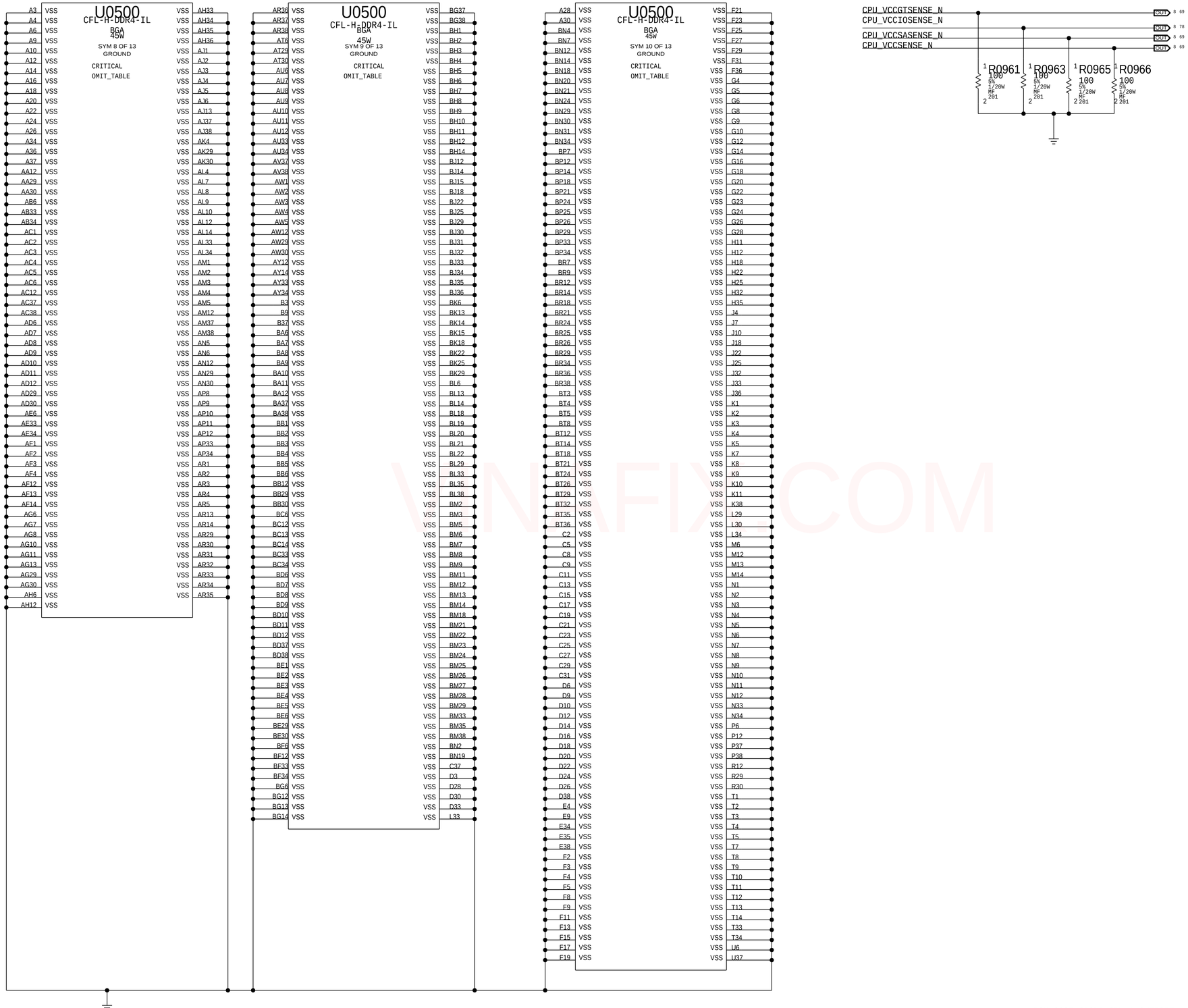

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	CPU Ground
	Apple Inc.
DRAWING NUMBER	051-02643
SIZE	D
REVISION	4.0.0
BRANCH	evt-0
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Vcc CPU Core Decoupling from 20140905 BOM

CPU VCORE Decoupling

Intel recommendation: 5x 220uF ESR 5m ohms ESL 1.9nH each,4x 47uF 0805 8x22uF 0603, 28x 10uF 0402, 3x 10uF 0402, 69x 1uF 0201 Board Edge: 2x 220uF, 4x 47uF rest on the back side
Apple Implementation:

115 PPVCC_S0_CPU

Place on bottom side of U0500

C1000 C1001 C1002 C1003 C1004 C1005 C1006 C1007 C1008 C1009 C1010 C1011 C1012 C1013 C1014 C1015 C1016 C1017 C1018 C1019 C1020 C1021 C1022
1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1023 C1024 C1025 C1026 C1027 C1028 C1029 C1030 C1031 C1032 C1033 C1034 C1035 C1036 C1037 C1038 C1039 C1040 C1041 C1042 C1043 C1044 C1045
1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1046 C1047 C1048 C1049 C1050 C1051 C1052 C1053 C1054 C1055 C1056 C1057 C1058 C1059 C1060 C1061 C1062
1UF 20% 4V CERM-X6S 0201

Place near inductors on bottom side.

C10A0 C10A3 C10A4 C10Z4 C10A6 C10A7 C10A8 C10ZB C10B0 C10B1 C10B4 C10C0 C10C1 C10C4 C10C5 C10C6 C10C7
20UF 20% 2.5V X6S-CERM 0402-1

Noise Floor caps

C10D1 C10D2 C10D3 C10D4 C10D5 C10D6 C10E2 C10E3 C10N1 C10N2 C10N3 C10N4 C10N5 C10N6 C10N7
20UF 20% 2.5V X6S-CERM 0402-1 (C10N1–C10N2)
12PF 5% 25V NP0-C0G 0201 (C10N3–C10N7)

C10F0 C10F1 C10F2 C10F3 C10F4 C10F5 C10F6 C10F7 C10F8 C10F9 C10G0
20UF 20% 2.5V X6S-CERM 0402-1

C1068 C1069 C1070 C1072 C1073
220UF 20% 2V ELEC SM-COMBO

122 115 PP1V2_S3_CPUDDR

Place on bottom side of U0500.

C1080 C1081 C1082 C1083 C1084 C1085
20UF 20% 2.5V X6S-CERM 0402-1

Place on bottom side of U0500

C1090 C1091 C1092 C1093 C1094 C1095
20UF 20% 2.5V X6S-CERM 0402-1

C1096
220UF 20% 2V ELEC SM-COMBO

CPU VDDQ Decoupling

Intel recommendation: 10x 10uF 0402, 4x 22uF 0602
Apple Implementation:

CPU VCCIO Decoupling

Intel recommendation: 3x 10uF 0402 (opposite CPU)
Apple Implementation:

115 8 5 PPVCCIO_S0_CPU

Place near U0500 on bottom side

C1086 C1087 C1088 C1089 C108A C108B C108C C108D
20UF 20% 2.5V X6S-CERM 0402-1

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
CPU Decoupling 1

Apple Inc.

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Vcc GT Slice Core Decoupling from 20140905 BOM

CPU VGTSlice Decoupling

Intel recommendation: 7x 220uF, 6x 47uF 0805, 6x 22uF 0603, 35x 10uF 0402, 68 1uF 0201
Apple Implementation:

Board Edge: 4x220uF, 7x 47uF rest on back side

122 116 PPVCCGT_S0_CPU

Place on bottom side of U0500

C1100 C1101 C1102 C1103 C1104 C1105 C1106 C1107 C1108 C1109 C1110 C1111 C1112 C1113 C1114 C1115 C1116 C1117 C1118 C1119 C1120 C1121 C1122 C1123
1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1124 C1125 C1126 C1127 C1128 C1129 C1130 C1131 C1132 C1133 C1134 C1135 C1136 C1137 C1138 C1139 C1140 C1141 C1142 C1143 C1144 C1145 C1146 C1147
1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1148 C1149 C1150 C1151 C1152 C1153 C1154 C1155 C1156 C1157 C1158 C1159 C1160 C1161 C1162 C1163 C1164 C1165 C1166 C1167
1UF 20% 4V CERM-X6S 0201

NOSTUFF

C11A0 C11A1 C11A2 C11A3 C11A4 C11A5 C11A6 C11A7 C11A8 C11A9 C11B0 C11B1 C11B2 C11B3 C11B4 C11B5 C11B6 C11B7 C11B8 C11B9 C11C0 C11C1 C11C2 C11C3 C11C4 C11C5 C11C6 C11C7 C11C8 C11C9 C11D0
20UF 20% 2.5V X6S-CERM 0402-1

C11F0 C11F1 C11F2 C11F3 C11F4 C11F5 C11F6 C11F7 C11E0 C11E1 C11E2 C11E3 C11E4 C11E5
20UF 20% 2.5V X6S-CERM 0402-1

C11D4 C11D3 C11D2 C11D1
20UF 20% 2.5V X6S-CERM 0402-1

C1168 C1170 C1171 C1172
220UF 20% 2V ELEC SM-COMBO

CPU VCCSTG Decoupling

115 8 6 PP1V05_S0SW

Place near U0500 on bottom side

C11L1 C11L2
1UF 20% 4V CERM-X6S 0201

CPU VCCPLL and VCCST Decoupling

115 8 PP1V05_S3

46 8 PP1V05_S3

C11M1 C11M2
1UF 20% 4V CERM-X6S 0201

Place near U0500 on bottom side

115 PPVCCSA_S0_CPU

Place on bottom side of U0500

C11H0 C11H1 C11H2
1UF 20% 4V CERM-X6S 0201

NOSTUFF

C11I0 C11I1 C11I2 C11I3 C11I4 C11I5 C11I6 C11I7
20UF 20% 2.5V X6S-CERM 0402-1

C11K9
220UF 20% 2V ELEC SM-COMBO

CPU VCCSA Decoupling

Intel recommendation: 2x 220uF, 1x 47uF 0805. 1x 22uF. 7x 10uF 0402, 3x 1uF 0201_
2x 220uF, 1x 22uF on board edge, everything else on back side
Apple Implementation:

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

BOM_COST_GROUP=CPU & CHIPSET

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OMIT_TABLE

U1200
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SYSTEM POWER MANAGEMENT
(IPU)

PM_SYSRST_L	AL17	SYS_RESET*	DRAM_RESET*	K25	PCH_DRAM_RESET_L
PM_PCH_SYS_PWROK	AK16	SYS_PWROK	(OD) DSW_PWROK	H25	PM_RSMRST_L
PM_PCH_PWROK	H23	PCH_PWROK	(IPD-DeepSx) WAKE*	K23	PCIE_WAKE_L
PLT_RST_L	U25	GPP_B13/PLTRST*	GPP_A14/SUS_STAT*/ESPI_RESET* (IPU-RSMRST#)	P23	ESPI_RESET_L
PM_RSMRST_L	J24	RSMRST*	GPD10/SLP_S5*	H22	PM_SLP_S5_L
			GPD5/SLP_S4*	J21	PM_SLP_S4_L
PM_PWRBTN_L	K22	GPD3/PWRBTN*	GPD4/SLP_S3*	K20	PM_SLP_S3_L
SPIROM_USE_MLB	L22	GPD1/ACPRESENT			
PCH_BATLOW_L	L24	GPD0/BATLOW*	SLP_SUS*	J25	TP_PCH_SLP_SUS_L
PM_SLP_S0_L	U23	GPP_B12/SLP_S0*			

RTC
ESPI/LPC

PCH_CLK32K_RTCX1	G24	RTCX1	GPP_A0/RCIN*/ESPI_ALERT1*	R24	PCH_GPP_A0_PU
NC_PCH_CLK32K_RTCX	G22	RTCX2	GPP_A1/LAD0/ESPI_IO0	N20	ESPI_IO_PCH<0>
PCH_INTRUDER_L	H20	INTRUDER*	GPP_A2/LAD1/ESPI_IO1	N21	ESPI_IO_PCH<1>
	F25	SRTCRST*	GPP_A3/LAD2/ESPI_IO2	M20	ESPI_IO_PCH<2>
PCH_RTC_RESET_L	F23	RTCRST*	GPP_A4/LAD3/ESPI_IO3	M22	ESPI_IO_PCH<3>
			GPP_A5/LFRAME*/ESPI_CS0*	M25	ESPI_CS_L
			GPP_A6/SERIRQ/ESPI_CS1*	N25	PCH_SOC_SYNC
			GPP_A7/PIRQA*/ESPI_ALERT0*	N24	PCH_ESPI_ALERT0_L
			GPD7	J20	PCH_STRP_GPD7

PP3V0_G3H_RTC

R1201 1M 5% 1/20W MF 201

PMU_CLK32K_PCH

R1220 100K 1/20W 201 MF 5%

R1221 127K 1% 1/20W MF 201

PCH_INTRUDER_L

ESPI_IO<0> R1260 22 1% 1/20W MF 201
ESPI_IO<1> R1261 22 1% 1/20W MF 201
ESPI_IO<2> R1262 22 1% 1/20W MF 201
ESPI_IO<3> R1263 22 1% 1/20W MF 201

NEED TO CHANGE PER INTEL SPEC

PP3V3_S5
PP1V8_S5
PP1V8_S5
PP3V3_S5

PCH_STRP_GPD7	R1204	100K	5% 1/20W MF 201	
SPIROM_USE_MLB	R1205	100K	5% 1/20W MF 201	NOSTUFF
PCIE_WAKE_L	R1206	100K	5% 1/20W MF 201	
PCH_BATLOW_L	R1208	10K	5% 1/20W MF 201	
PCH_ESPI_ALERT0_L	R1209	100K	5% 1/20W MF 201	
PCH_GPP_A0_PU	R1210	100K	5% 1/20W MF 201	
SOC_CLKREQ_L	R1211	47K	201	
DEBUG_CLKREQ_L	R1213	47K	201	
PM_SYSRST_L	R1214	3.0K	5% 1/20W MF 201	

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CLOCK SIGNALS

PCIE_CLK100M_SOC_N	AR10	CLKOUT_PCIE_N0	XTAL_IN	AN3	PCH_CLK24M_XTALIN
PCIE_CLK100M_SOC_P	AN10	CLKOUT_PCIE_P0	XTAL_OUT	AN1	PCH_CLK24M_XTALOUT
PCH_PCIE_CLK100M_WLAN_N	AP9	CLKOUT_PCIE_N1	CLKIN_XTAL	AR4	PCH_CLKIN_XTAL
PCH_PCIE_CLK100M_WLAN_P	AM9	CLKOUT_PCIE_P1			
EG_PEG_CLK100M_N	AR8	CLKOUT_PCIE_N2			
EG_PEG_CLK100M_P	AN8	CLKOUT_PCIE_P2			
PCIE_CLK100M_DEBUG_N	AM6	CLKOUT_PCIE_N3			
PCIE_CLK100M_DEBUG_P	AK6	CLKOUT_PCIE_P3			
NC	AM8	CLKOUT_PCIE_N4			
NC	AK8	CLKOUT_PCIE_P4			
NC	AL7	CLKOUT_PCIE_N5			
NC	AJ7	CLKOUT_PCIE_P5			
PCIE_CLK100M_TBT_X_N	AK1	CLKOUT_PCIE_N6			
PCIE_CLK100M_TBT_X_P	AK3	CLKOUT_PCIE_P6			
PCIE_CLK100M_TBT_T_N	AJ5	CLKOUT_PCIE_N7			
PCIE_CLK100M_TBT_T_P	AK4	CLKOUT_PCIE_P7			
			XCLK_BIASREF	AP2	PCH_XCLK_BIASREF
			GPP_A9/CLKOUT_LPC0 /ESPI_CLK	M23	ESPI_CLK60M_PCH_R

R1237 22 1% 1/20W MF 201
ESPI_CLK60M_PCH
PLACE_NEAR=U1200.M23:4mm

CRITICAL C1250 10PF 5% 50V C0G 0201
CRITICAL C1251 10PF 5% 50V C0G 0201
R1251 200K 1% 1/20W MF 201
R1250 0 5% 1/20W MF 0201
Y1250 24MHZ_10PPM-8PF-30OHM 2.5X2.0-SM
PCH_CLK24M_XTALOUT_R

Ce1=Ce2=2*(C_L - C_S - C_I) = 2*(8-0.7)=14.6pF
C_L = Load Capacitance = 8pF
C_S = Trace Capacitance + XTAL Pad Capacitance = 0.7pF
C_I= PCH Pin Capacitance = 0

CLKOUT_CPUBCLK_N	AR7	CPU_CLK100M_BCLK_N			
CLKOUT_CPUBCLK_P	AP7	CPU_CLK100M_BCLK_P			
CLKOUT_CPUNSSC_N	AR6	CPU_CLK24M_NSSC_CLK_N			
CLKOUT_CPUNSSC_P	AN6	CPU_CLK24M_NSSC_CLK_P			
CLKOUT_CPUPCIBCLK_N	AP5	CPU_CLK100M_PCIBCLK_N			
CLKOUT_CPUPCIBCLK_P	AM5	CPU_CLK100M_PCIBCLK_P			

PCI EXPRESS
CLOCKS & CONTROL

GPP_B5/SRCCLKREQ0*	W22	SOC_CLKREQ_L			
GPP_B6/SRCCLKREQ1*	AB22	PCH_WLAN_CLKREQ_L			
GPP_B7/SRCCLKREQ2*	U20	PCH_GPU_CLKREQ_L			
GPP_B8/SRCCLKREQ3*	V20	DEBUG_CLKREQ_L			
GPP_B9/SRCCLKREQ4*	W20	NC			
GPP_B10/SRCCLKREQ5*	V21	NC			
GPP_H0/SRCCLKREQ6*	D12	TBT_X_CLKREQ_L			
GPP_H1/SRCCLKREQ7*	A10	TBT_T_CLKREQ_L			

PP1V8_S5

R1236 PM_SLP_S0_L 100K 5% 1/20W MF 201 NOSTUFF

PM_SLP_S5_L	R1230	100K	5% 1/20W MF 201
PM_SLP_S4_L	R1231	100K	5% 1/20W MF 201
PM_SLP_S3_L	R1232	100K	5% 1/20W MF 201
PM_SLP_S0_L	R1233	100K	5% 1/20W MF 201
PCH_SOC_SYNC	R1215	100K	5% 1/20W MF 201
PCH_CLKIN_XTAL	R1235	10K	5% 1/20W MF 201
PCH_XCLK_BIASREF	R1234	60.4	1% 1/20W MF 201

PLACE_NEAR=U1200.AP2:2.54mm

PP3V3_S5

R1207 10K 1/20W 201 5% MF PM_PWRBTN_L

BOM_COST_GROUP=CPU & CHIPSET

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Intel Spec: 1k Pull-up for IO2 and IO3

PP1V8_S5 — 12 15 16 19 20 52 80

PPVCCSPI_PRIM_PCH — 16

R1330 100K 5% 1/20W MF 201 — VCCSPI:3V3 — SPI_MOSI_R — 13 18

R1331 100K 5% 1/20W MF 201 — VCCSPI:3V3 — SPI_IO<2> — 13 18

R1332 100K 5% 1/20W MF 201 — VCCSPI:3V3 — SPI_IO<3> — 13

R1318 1K 5% 1/20W MF 201 — NOSTUFF — PCH_STRP_BSSB_SEL_GPIO — 13

R1303 1K 5% 1/20W MF 201 — PCH_STRP_NO_REBOOT — 13

R1317 100K 5% 1/20W MF 201 — PCH_WLAN_DEV_WAKE — 13 36 37

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0134	3	RES,MF,5%,1/20W,201,75K	R1330,R1331,R1332		VCCSPI:1V8

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DMI / CPU/MISC

DMI_S2N_N<0>	H3	DMI0_TXN	118 5 OUT
DMI_S2N_P<0>	H1	DMI0_TXP	118 5 OUT
DMI_S2N_N<1>	J2	DMI1_TXN	118 5 OUT
DMI_S2N_P<1>	J1	DMI1_TXP	118 5 OUT
DMI_S2N_N<2>	K3	DMI2_TXN	118 5 OUT
DMI_S2N_P<2>	K1	DMI2_TXP	118 5 OUT
DMI_S2N_N<3>	L4	DMI3_TXN	118 5 OUT
DMI_S2N_P<3>	L2	DMI3_TXP	118 5 OUT
DMI_N2S_N<0>	C3	DMI0_RXN	118 5 IN
DMI_N2S_P<0>	B2	DMI0_RXP	118 5 IN
DMI_N2S_N<1>	C1	DMI1_RXN	118 5 IN
DMI_N2S_P<1>	E1	DMI1_RXP	118 5 IN
DMI_N2S_N<2>	E2	DMI2_RXN	118 5 IN
DMI_N2S_P<2>	F1	DMI2_RXP	118 5 IN
DMI_N2S_N<3>	F4	DMI3_RXN	118 5 IN
DMI_N2S_P<3>	F3	DMI3_RXP	118 5 IN

CPUPWRGD	AR16	PCH_PROCPWRGD	R1308 0 1/20W MF 0201 → CPU_PWRGD — 6 119 121 OUT
THRMTRIP*	AP12	PCH_PM_THRMTRIP_L_R	R1309 620 1/20W MF 201 → PCH_PMTHRMTRIP_L — 46 IN
PECI	AR12	PCH_PECI	R1315 13 1/20W MF 201 → CPU_PECI — 6 46 BI
GPP_B3/CPU_GP2	V25	PCH_WLAN_PERST_L	20 36 37 OUT
GPP_B4/CPU_GP3	V24	PCH_WLAN_DEV_WAKE	13 36 37 IN
GPP_E3/CPU_GP0	B12	XDP_PCH_OBSDATA_A2	18 OUT
GPP_E7/CPU_GP1	C13	XDP_PCH_OBSDATA_B2	18 OUT
(IPD) GPP_B23/SML1ALERT*/PCHHOT*	U22	PCH_STRP_BSSB_SEL_GPIO	13
CPU_TRST*	AR17	XDP_CPU_TRST_L	6 18 121 OUT
PLTRST_CPU*	AM14	CPU_RESET_L	6 OUT
PRDY*	AJ16	XDP_CPU_PRDY_L	6 18 121 OUT
PREQ*	AP14	XDP_CPU_PREQ_L	6 18 121 OUT
TRIGGER_IN	AR13	CPU_PCH_TRIGGER	5 IN
TRIGGER_OUT	AN13	PCH_CPU_TRIGGER_R	R1314 33 1/20W MF 201 (PLACE_NEAR=U1200.AN13:5mm) → PCH_CPU_TRIGGER — 5 OUT
PM_DOWN	AL12	CPU_PCH_PM_DOWN	IN 5
PM_SYNC	AJ12	PM_SYNC_R	R1319 33 1/20W MF 201 (PLACE_NEAR=U1200.AJ12:10mm) → PM_SYNC — 6 OUT

BSS GPIO 0=BSSB CLK/DI on USB-SS

NOSTUFF R1326 150K 5% 1/20W MF 201

OMIT_TABLE

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RSVD & TP PINS / AUDIO

NC	A24	RSVD
NC	AB1	RSVD
NC	AJ10	RSVD
NC	AJ2	RSVD
NC	AJ4	RSVD
NC	AJ8	RSVD
NC	AK10	RSVD
NC	AM10	RSVD
NC	AR24	RSVD
NC	G2	RSVD
NC	G4	RSVD
NC	M1	RSVD
NC	M3	RSVD
NC	V1	RSVD
NC	V2	RSVD

HDA_BCLK/I2S0_SCLK	AC24	NC	
HDA_SYNC/I2S0_SFRM	AD23	NC	
HDA_SDI0/I2S0_RXD	AD25	NC	
HDA_SDI1/I2S1_RXD	AD22	TP_HDA_SDI1	TP-P5 TP TP1306
(IPD) HDA_SDO/I2S0_TXD	AC25	TP_HDA_SDO	TP-P5 TP TP1307
HDA_RST*/I2S1_SCLK	AD20	TP_HDA_RST	TP-P5 TP TP1308
HDACPU_SCLK	AJ13	PCH_DISPA_BCLK_R	R1320 33 1/20W MF 201 → PCH_DISPA_BCLK — 20 OUT
HDACPU_SDI	AK13		PCH_DISPA_SDI — 20 IN
HDACPU_SDO	AM13	PCH_DISPA_SDO_R	R1321 33 1/20W MF 201 → PCH_DISPA_SDO — 20 OUT
GPP_D5/I2S2_SFRM/CNV_RF_RESET*	L21	NC	
GPP_D6/I2S2_TXD/MODEM_CLKREQ	AJ21	NC	

TP1300 TP-P5 TP_PCH_TP1_F22 — F22 TP1
TP1301 TP-P5 TP_PCH_TP3_B24 — B24 TP2

JTAG

PCH_ITP_PMODE	AN16	ITP_PMODE	121 18 IN
XDP_PCH_TCK	AP17	PCH_JTAG_TCK	(IPD) 121 18 IN
XDP_PCH_TDI	AR18	PCH_JTAG_TDI	(IPU) 121 18 IN
XDP_PCH_TDO	AM16	PCH_JTAG_TDO	(Undriven) 121 18 OUT
XDP_PCH_TMS	AL14	PCH_JTAG_TMS	(IPU) 121 18 IN
XDP_PCH_JTAGX	AN18	PCH_JTAGX	121 18 IN

OMIT_TABLE

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SPI / GSPI

NC	C23	SPI0_CLK		
NC	E25	SPI0_CS0*		
NC	C25	SPI0_CS1*		
(IPD) GPP_B18/GSPI0_MOSI	P20	PCH_STRP_NO_REBOOT	13	No Rebort: 0=Disable; 1=Enable
(IPD) GPP_B22/GSPI1_MOSI	P22	TP_PCH_STRP_BOOT_SPI_L		BootBIOS Strap: 0=SPI; 1=LPC
18 13 BI SPI_MOSI_R	D21	SPI0_MOSI	(IPU 20K)	
NC	A20	SPI0_MISO		
18 13 BI SPI_IO<2>	E22	SPI0_IO2	(IPU 20K)	
13 BI SPI_IO<3>	B21	SPI0_IO3	(IPU 20K)	

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: PCH DMI/JTAG/SPI/HDA

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USB3_EXTA_D2R_N — AA4 USB31_1_RXN
USB3_EXTA_D2R_P — AA2 USB31_1_RXP
USB3_EXTA_R2D_C_N — AD3 USB31_1_TXN
USB3_EXTA_R2D_C_P — AD1 USB31_1_TXP
USB3_TEST_D2R_N — W3 USB31_2_RXN
USB3_TEST_D2R_P — W1 USB31_2_RXP
USB3_TEST_R2D_N — AC2 USB31_2_TXN
USB3_TEST_R2D_P — AC1 USB31_2_TXP

USB2N_1 AG1 USB2_UPC_TA_N
USB2P_1 AG2 USB2_UPC_TA_P
USB2N_2 AF1 USB2_UPC_TB_N
USB2P_2 AF3 USB2_UPC_TB_P
USB2N_3 AH1 USB2_UPC_XA_N
USB2P_3 AH3 USB2_UPC_XA_P
USB2N_4 AF4 USB2_UPC_XB_N
USB2P_4 AE5 USB2_UPC_XB_P

USB3
USB2

GPP_E9/USB2_OC0* E12 XDP_USB_EXTA_OC_L
GPP_E10/USB2_OC1* G10 XDP_USB_EXTB_OC_L
GPP_E11/USB2_OC2* D10 XDP_USB_EXTC_OC_L
GPP_E12/USB2_OC3* F10 XDP_USB_EXTD_OC_L
GPP_F15/USB2_OC4* B17 NC
GPP_F16/USB2_OC5* D17 NC

USB2_COMP AB6 USB2_COMP PLACE_NEAR=U1200.AB6:10.0mm
USB2_ID AE4 USB2_ID
USB2_VBUSSENSE AE2 USB2_VBUSSENSE

R1410 1K 5% 1/20W MF 201
R1411 1K 5% 1/20W MF 201
R1470 113 1% 1/20W MF 201

PP3V3_S5
PM_SLP_S3_L
PP3V3_S0SW_TBT_T_SNS
PP3V3_S0SW_TBT_X_SNS
PM_SLP_S3_L

R1491 100K 5% 1/20W MF 201 TBT_X_CIO_PWR_EN
R1492 100K 5% 1/20W MF 201 TBT_X_USB_PWR_EN
R1493 100K 5% 1/20W MF 201 TBT_T_CIO_PWR_EN
R1494 100K 5% 1/20W MF 201 TBT_T_USB_PWR_EN
R1441 100K 5% 1/20W MF 201 NOSTUFF TBT_X_CIO_PWR_EN
R1442 100K 5% 1/20W MF 201 NOSTUFF TBT_X_USB_PWR_EN
R1443 100K 5% 1/20W MF 201 NOSTUFF TBT_T_CIO_PWR_EN
R1444 100K 5% 1/20W MF 201 NOSTUFF TBT_T_USB_PWR_EN
R1446 100K 5% 1/20W MF 201 TBT_T_PLUG_EVENT_L
R1445 100K 5% 1/20W MF 201 TBT_X_PLUG_EVENT_L
R1447 10K 5% 1/20W MF 201 XDP_JTAG_ISP_TDO
R1460 10K 5% 1/20W MF 201 XDP_USB_EXTA_OC_L
R1461 10K 5% 1/20W MF 201 XDP_USB_EXTB_OC_L
R1420 10K 5% 1/20W MF 201 XDP_USB_EXTC_OC_L
R1421 10K 5% 1/20W MF 201 XDP_USB_EXTD_OC_L
R1448 100K 5% 1/20W MF 201 XDP_JTAG_ISP_TDI

MAKE_BASE=TRUE
XDP_JTAG_ISP_TDO = XDP_JTAG_ISP_TDO
XDP_USB_EXTA_OC_L = XDP_USB_EXTA_OC_L
XDP_USB_EXTB_OC_L = XDP_USB_EXTB_OC_L
XDP_USB_EXTC_OC_L = XDP_USB_EXTC_OC_L
XDP_USB_EXTD_OC_L = XDP_USB_EXTD_OC_L
XDP_JTAG_ISP_TDI = XDP_JTAG_ISP_TDI
XDP_JTAG_ISP_TCK = XDP_JTAG_ISP_TCK

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PCIE/SATA/USB3

PCH_PCIE_WLAN_D2R_N — W4 PCIE1_RXN/USB31_7_RXN
PCH_PCIE_WLAN_D2R_P — W6 PCIE1_RXP/USB31_7_RXP
PCH_PCIE_WLAN_R2D_C_N — U1 PCIE1_TXN/USB31_7_TXN
PCH_PCIE_WLAN_R2D_C_P — U3 PCIE1_TXP/USB31_7_TXP
USB3_TEST2_D2R_N — U6 PCIE2_RXN/USB31_8_RXN
USB3_TEST2_D2R_P — V5 PCIE2_RXP/USB31_8_RXP
USB3_TEST2_R2D_N — R2 PCIE2_TXN/USB31_8_TXN
USB3_TEST2_R2D_P — R1 PCIE2_TXP/USB31_8_TXP
USB3_SOCDEBUG_D2R_N — P4 PCIE3_RXN/USB31_9_RXN
USB3_SOCDEBUG_D2R_P — R5 PCIE3_RXP/USB31_9_RXP
USB3_SOCDEBUG_R2D_C_N — P3 PCIE3_TXN/USB31_9_TXN
USB3_SOCDEBUG_R2D_C_P — P1 PCIE3_TXP/USB31_9_TXP
NC — P6 PCIE4_RXN/USB31_10_RXN
NC — N5 PCIE4_RXP/USB31_10_RXP
NC — N2 PCIE4_TXN/USB31_10_TXN
NC — N1 PCIE4_TXP/USB31_10_TXP

PCIE17_RXN/SATA4_RXN — F6 PCIE_SOC_D2R_N<0>
PCIE17_RXP/SATA4_RXP — D6 PCIE_SOC_D2R_P<0>
PCIE17_TXN/SATA4_TXN — B4 PCIE_SOC_R2D_C_N<0>
PCIE17_TXP/SATA4_TXP — A4 PCIE_SOC_R2D_C_P<0>
PCIE18_RXN/SATA5_RXN — G8 PCIE_SOC_D2R_N<1>
PCIE18_RXP/SATA5_RXP — G7 PCIE_SOC_D2R_P<1>
PCIE18_TXN/SATA5_TXN — B5 PCIE_SOC_R2D_C_N<1>
PCIE18_TXP/SATA5_TXP — A5 PCIE_SOC_R2D_C_P<1>
PCIE19_RXN/SATA6_RXN — F8 PCIE_SOC_D2R_N<2>
PCIE19_RXP/SATA6_RXP — D8 PCIE_SOC_D2R_P<2>
PCIE19_TXN/SATA6_TXN — C6 PCIE_SOC_R2D_C_N<2>
PCIE19_TXP/SATA6_TXP — A6 PCIE_SOC_R2D_C_P<2>
PCIE20_RXN/SATA7_RXN — G9 PCIE_SOC_D2R_N<3>
PCIE20_RXP/SATA7_RXP — E9 PCIE_SOC_D2R_P<3>
PCIE20_TXN/SATA7_TXN — B7 PCIE_SOC_R2D_C_N<3>
PCIE20_TXP/SATA7_TXP — A7 PCIE_SOC_R2D_C_P<3>

XDP_PCH_OBSFN_C0 — D16 GPP_E0/SATAXPCIE0/SATAGP0
XDP_PCH_OBSDATA_A0 — F16 GPP_E1/SATAXPCIE1/SATAGP1
XDP_PCH_OBSDATA_A1 — G14 GPP_E2/SATAXPCIE2/SATAGP2
XDP_PCH_OBSDATA_D0 — C20 GPP_F0/SATAXPCIE3/SATAGP3
XDP_PCH_OBSDATA_D1 — A19 GPP_F1/SATAXPCIE4/SATAGP4
XDP_JTAG_ISP_TCK — B19 GPP_F2/SATAXPCIE5/SATAGP5
XDP_JTAG_ISP_TDI — A22 GPP_F3/SATAXPCIE6/SATAGP6
XDP_JTAG_ISP_TDO — G18 GPP_F4/SATAXPCIE7/SATAGP7
TBT_T_USB_PWR_EN — D18 GPP_F10/SATA_SCLOCK
TBT_X_PLUG_EVENT_L — C18 GPP_F11/SATA_SLOAD
TBT_T_PLUG_EVENT_L — G16 GPP_F12/SATA_SDATAOUT1
NC — E17 GPP_F13/SATA_SDATAOUT0

GPP_E4/SATA_DEVSLP0 — E14 XDP_PCH_OBSDATA_A3
GPP_E5/SATA_DEVSLP1 — F13 XDP_PCH_OBSDATA_B0
GPP_E6/SATA_DEVSLP2 — D13 XDP_PCH_OBSDATA_B1
GPP_F5/SATA_DEVSLP3 — F20 TBT_X_PCI_RESET_L
GPP_F6/SATA_DEVSLP4 — G19 TBT_T_PCI_RESET_L
GPP_F7/SATA_DEVSLP5 — D20 TBT_X_CIO_PWR_EN
GPP_F8/SATA_DEVSLP6 — E19 TBT_X_USB_PWR_EN
GPP_F9/SATA_DEVSLP7 — F18 TBT_T_CIO_PWR_EN
GPP_E8/SATALED* — G13 XDP_PCH_OBSDATA_B3

PCH_PCIE_RCOMPP — L5 PCIE_RCOMPP
PCH_PCIE_RCOMPN — K4 PCIE_RCOMPN

R1400 100 1% 1/20W MF 201

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: PCH PCI-E/USB

Apple Inc.

DRAWING NUMBER: 051-02643
SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
PAGE: 14 OF 200
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SPEED	CONGIF3
2400MHZ	0
2133MHZ	1

STORAGE	CONGIF2
16GB	1
32GB	0

VENDOR	CONGIF1	CONGIF0
SAMSUNG	1	0
MICRON	0	1
HYNIX	0	0

RAMCFG0:L R1530 1K 5% 1/20W MF 201
RAMCFG1:L R1531 1K 5% 1/20W MF 201
RAMCFG2:L R1532 1K 5% 1/20W MF 201
RAMCFG3:L R1533 1K 5% 1/20W MF 201
R1534 1K 5% 1/20W MF 201 RAMCFG4:L

MLB_RAMCFG0 15
MLB_RAMCFG1 15
MLB_RAMCFG2 15
MLB_RAMCFG3 15
MLB_RAMCFG4 15

OMIT_TABLE

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CNL-PCH-H-USFF-QNYP
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J680 Display Port DDPF Disabled

PDG recommends to NC the HPD lines not being used

J680 Display Port DDPB/C/D Disabled

eSPI Flash Mode: 0=MAF; 1=SAF

	NC	A18	GPP_F14/PS_ON*	
93 15 OUT	EDP_IG_PANEL_PWR	A16	GPP_F19/EDP_VDDEN	GPPF/ BACKLIGHT
93 15 OUT	EDP_IG_BKLT_EN	C16	GPP_F20/EDP_BKLTEN	
	NC	A14	GPP_F21/EDP_BKLTCTL	
	NC	B14	GPP_F22/DDPF_CTRLCLK	
	NC	A13	GPP_F23/DDPF_CTRLDATA	
	NC	AN23	GPP_I0/DDPB_HPD0/DISP_MISC0	GPPI/DISPLAY GPPG
	NC	AN25	GPP_I1/DDPC_HPD1/DISP_MISC1	
	NC	AP24	GPP_I2/DDPD_HPD2_DISP_MISC2	
	NC	AP22	GPP_I3/DDPF_HPD3_DISP_MISC3	
93 15 IN	DP_INT_IG_HPD	AR22	GPP_I4/EDP_HPD/DISP_MISC4	
	NC	AP19	GPP_I5/DDPB_CTRLCLK	
	NC	AM19	GPP_I6/DDPB_CTRLDATA	
	NC	AR20	GPP_I7/DDPC_CTRLCLK	
	NC	AN20	GPP_I8/DDPC_CTRLDATA	
	NC	AP21	GPP_I9/DDPD_CTRLCLK	
	NC	AR21	GPP_I10/DDPD_CTRLDATA	
	NC	AL24	GPP_I11/M2_SKT2_CFG0	
	NC	AL25	GPP_I12/M2_SKT2_CFG1	
	NC	AK25	GPP_I13/M2_SKT2_CFG2	
107 29 15 OUT	TBT_POC_RESET			
15	PCH_STRP_SPIROM_SAF	A9	GPP_H12/SML2ALERT* (IPD)	GPPH/I2C/INTEGRATED SENSOR /SMLINK
15	PCH_STRP_GPP_H15	B9	GPP_H15/SML3ALERT*	
19 15 IN	WLAN_AUDIO_SYNC_LS3V3	C10	GPP_H23/TIME_SYNC0	

AM18	SOC_SWD_MUX_SEL_PCH	15	
AK18	CPU_C10_GATE_L	OUT 15 76 78 79 131	GPP_J2:Unused
AL19	PCH_SWD_SOC_CLK	15	GPP_J3:Unused
AJ18	PCH_SWD_SOC_IO	15	GPP_J4: 0=38.4MHz 1=24MHz XTAL
AJ22	PCH_STRP_XTAL_24MHZ	15	
AH23	MLB_RAMCFG2	15	
AJ25	PCH_STRP_CNV_L	15	GPP_J6: 0=ENABLE 1=DISABLE
AH25	MLB_RAMCFG3	15	
AK22	MLB_RAMCFG4	15	
AK23	PCH_STRP_VCCPSPI_1V8	15	GPP_J9: 0=3.3V; 1=1.8V
AM20	PCH_BT_ROM_BOOT_L	15 36	
AK20	PCH_BT_DEV_WAKE	15 36	
A8	MLB_RAMCFG0	15	
C8	MLB_RAMCFG1	15	
AJ17	PCH_GPPJ_RCOMP_1P8	15	

GPP_J0/CNV_PA_BLANKING		
GPP_J1/CPU_C10_GATE*		
GPP_J2		
GPP_J3		
(IPD) GPP_J4/CNV_BRI_DT/UART0B_RTS*		
GPP_J5/CNV_BRI_RSP/UART0B_RXD		
GPP_J6/CNV_RGI_DT/UART0B_TXD		
GPP_J7/CNV_RGI_RSP/UART0B_CTS*		
GPP_J8/CNV_MFUART2_RXD		
(IPD) GPP_J9/CNV_MFUART2_TXD		
GPP_J10		
GPP_J11/A4WP_PRESENT		
GPP_K20	A24	NC
GPP_K21	A25	NC
CNV_WR_CLKP	AF23	NC
CNV_WR_CLKN	AF25	NC
CNV_WR_D0P	AE22	NC
CNV_WR_D0N	AE24	NC
CNV_WR_D1P	AH22	NC
CNV_WR_D1N	AH20	NC
CNV_WT_CLKP	AG21	NC
CNV_WT_CLKN	AG20	NC
CNV_WT_D0P	AF22	NC
CNV_WT_D0N	AF20	NC
CNV_WT_D1P	AE21	NC
CNV_WT_D1N		
CNV_WT_RCOMP		

PP1V8_S5 80
PP3V3_S5 16 19 80
PP1V8_S5 12 13 16 19 20 52 80
PP3V3_S5 16 80

R1501	10K	5% 1/20W MF 201	JTAG_TBT_X_TMS	15 27 121
R1502	10K	5% 1/20W MF 201	JTAG_TBT_T_TMS	15 105 121
R1503	1K	5% 1/20W MF 201	PCH_STRP_ESPI	15
R1505	47K	5% 1/20W MF 201	PCH_UART_BT_D2R	15 35
R1506	47K	5% 1/20W MF 201	PCH_UART_BT_R2D	15 35
R1507	47K	5% 1/20W MF 201	PCH_UART_BT_RTS_L	15 35
R1508	47K	5% 1/20W MF 201	PCH_UART_BT_CTS_L	15 35
R1509	47K	5% 1/20W MF 201	PCH_UART_DEBUG_D2R	15 29 119 126
R1510	47K	5% 1/20W MF 201	PCH_UART_DEBUG_R2D	15 29 119 126
R1511	1K	5% 1/20W MF 201	PCH_STRP_SPIROM_SAF	15
R1512	100K	5% 1/20W MF 201	PCH_STRP_GPP_H15	15
R1526	20K	1% 1/20W MF 201	PCH_STRP_CNV_L	15
R1543	1K	5% 1/20W MF 201	PCH_STRP_XTAL_24MHZ	15
R1514	100K	5% 1/20W MF 201	PCH_SWD_SOC_CLK	15
R1515	100K	5% 1/20W MF 201	PCH_SWD_SOC_IO	15
R1516	100K	5% 1/20W MF 201	CPU_C10_GATE_L	15 76 78 79 131
R1517	1K (VCCSPI:1V8)	5% 1/20W MF 201	PCH_STRP_VCCPSPI_1V8	15
R1518	1K (VCCSPI:3V3)	5% 1/20W MF 201		

R1522	100K	5% 1/20W MF 201	DP_INT_IG_HPD	15 93
R1523	100K	5% 1/20W MF 201	TBT_POC_RESET	15 29 107
R1524	100K	5% 1/20W MF 201	WLAN_AUDIO_SYNC_LS3V3	15 19
R1525	100K	NOSTUFF 5% 1/20W MF 201	PCH_BT_DEV_WAKE	15 36
R1527	100K	5% 1/20W MF 201	EDP_IG_PANEL_PWR	15 93
R1528	100K	5% 1/20W MF 201	EDP_IG_BKLT_EN	15 93
R1529	100K	5% 1/20W MF 201	SOC_SWD_MUX_SEL_PCH	15
R1540	100K	NOSTUFF 5% 1/20W MF 201	PCH_BT_ROM_BOOT_L	15 36
R1542	200	1% 1/20W MF 201	PCH_GPPJ_RCOMP_1P8	15

OMIT_TABLE

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39 29 OUT 39 IN	SOC_PERST_L / PCH_GCON_INT_L	R22 / P25	GPP_A20/ISH_GP2 / GPP_A21/ISH_GP3
TP1501 TP-P5	TP_PCH_STRP_TOPBLK_SWP_L (PLACE_SIDE=BOTTOM)	R21	GPP_B14/SPKR (IPD)
121 27 15 OUT	JTAG_TBT_X_TMS	AC20	GPP_D0/SPI1_CS*/SBK0/BK0
121 105 15 OUT	JTAG_TBT_T_TMS	AC21	GPP_D1/SPI1_CLK/SBK1/BK1
NC		AB20	GPP_D12/ISH_SPI_MOSI/GP_BSSB_DI/GSPI2_MOSI

GPPA/ INTEGRATED SENSOR
GPPB
GPPC/SMLINK0/I2C/UART
GPPD/INTEGRATED SENSOR/UART/I2C

GPP_C0/SMBCLK	W23	SMBUS_PCH_CLK	OUT 52
GPP_C1/SMBDATA	W25	SMBUS_PCH_DATA	IN 52
(IPD) GPP_C2/SMBALERT*	AA22	TP_PCH_STRP_TLSCONF	PROJ-SPECIFIC PULLUP / TLS: 0=Disbale; 1=Enable
(IPD) GPP_C5/SML0ALERT*	AB19	PCH_STRP_ESPI 15	GPP_C5: 0=LPC; 1=eSPI
GPP_C8/UART0A_RXD	AA24	PCH_UART_BT_D2R	IN 15 35
GPP_C9/UART0A_TXD	AA21	PCH_UART_BT_R2D	OUT 15 35
GPP_C10/UART0A_RTS*	AA18	PCH_UART_BT_RTS_L	OUT 15 35
GPP_C11/UART0A_CTS*	Y19	PCH_UART_BT_CTS_L	IN 15 35
GPP_C20/UART2_RXD	AB25	PCH_UART_DEBUG_D2R	IN 15 29 119 126
GPP_C21/UART2_TXD	AB23	PCH_UART_DEBUG_R2D	OUT 15 29 119 126

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
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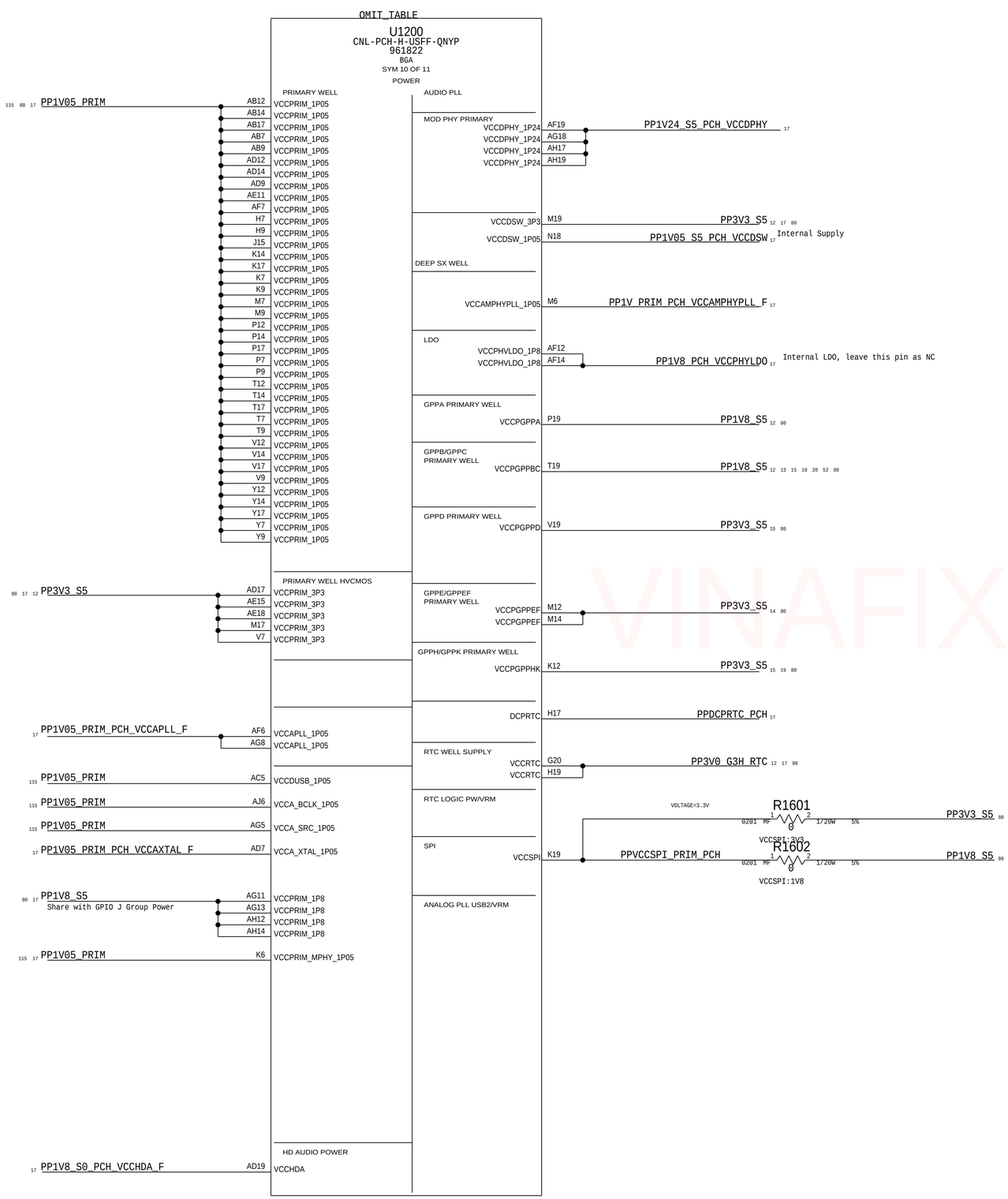

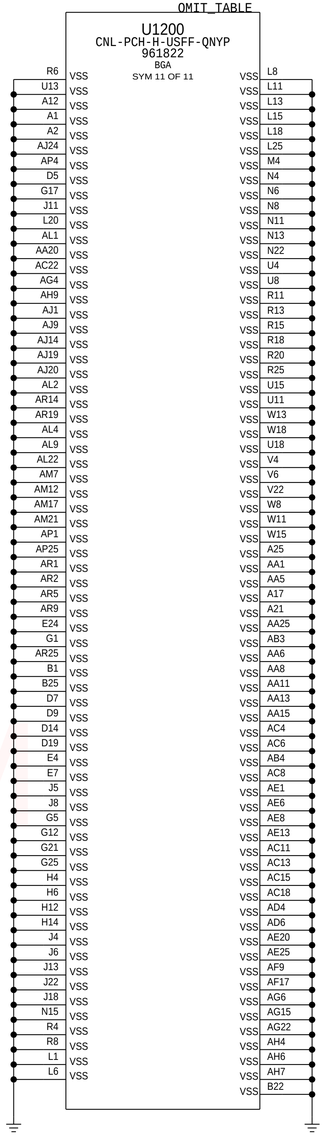

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH Power

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
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BRANCH evt-0
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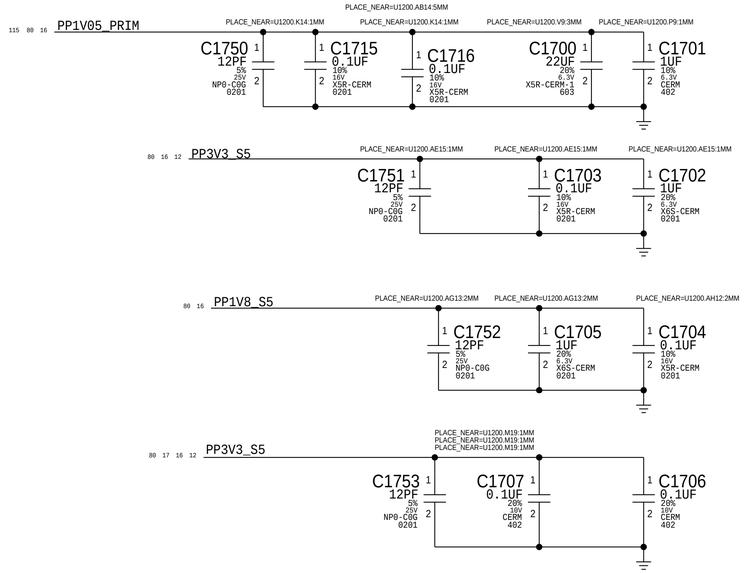

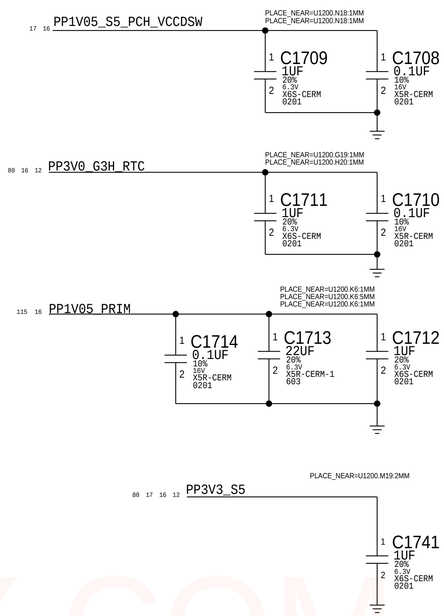

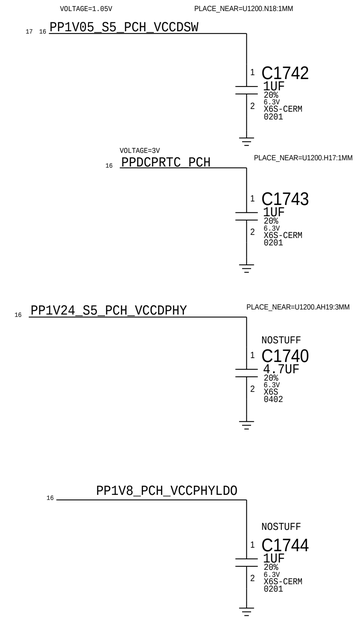

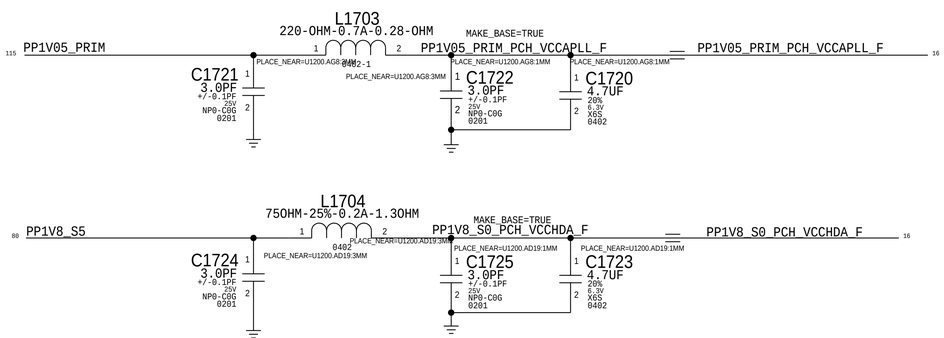

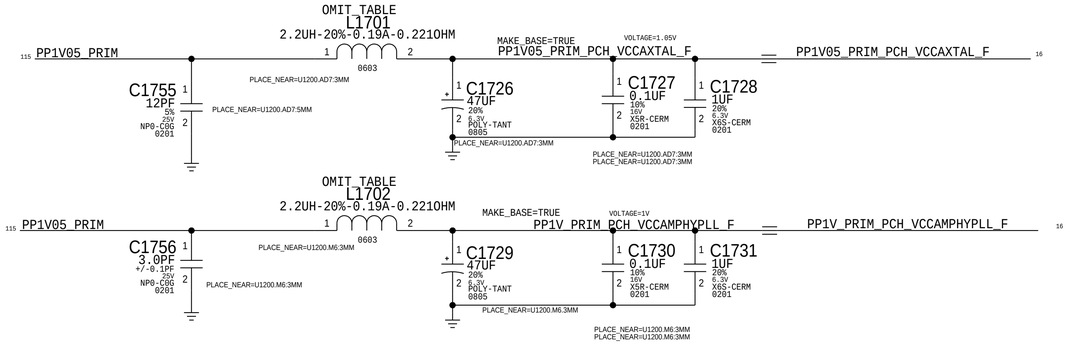

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	2	RES,MF,1A MAX,00HM,5%,0603	L1701,L1702		

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH Decoupling

Apple Inc.

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Extra BPM Testpoints
XDP_BPM_L<0> TP1800
XDP_BPM_L<1> TP1801
XDP_BPM_L<2> TP1802
XDP_BPM_L<3> TP1803
Primary / Merged (CPU/PCH) Micro2-XDP
PP1V05_PRIM
PULL CFG<3> LOW WHEN XDP PRESENT
R1801 1.5K
XDP:YES
NO_XNET_CONNECTION
PLACE_NEAR=J1800.2:5MM
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847
NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.
XDP_PRESENT_CPU
XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
CPU_CFG<8>
CPU_CFG<9>
CPU_CFG<10>
CPU_CFG<11>
CPU_CFG<12>
CPU_CFG<13>
CPU_CFG<14>
CPU_CFG<15>
CPU_CFG<16>
CPU_CFG<17>
CPU_CFG<18>
CPU_CFG<19>
PP3V3_S5
PLACE_NEAR=J1800.48:2.54MM
R1804 1K
PM_RSMRST_L
R1800 1K
PLACE_NEAR=U1200.H25:2.54MM
PM_PWRBTN_L
R1802 10
PLACE_NEAR=U1200.K22:5MM
SPI_MOSI_R
R1803 1.5K
PLACE_NEAR=U1200.D21:10MM
XDP_PM_RSMRST_L
XDP_CPU_PWRBTN_L
SPI_MOSI_R_CONN
XDP_PCH_TCK
XDP_CPU_TCK
XDP_PCH_JTAGX
R1835 0
PLACE_NEAR=J1800.58:28MM
C1804 0.1UF
C1800 0.1UF
C1801 0.1UF
C1806 0.1UF
PLACE_NEAR=J1800.42:28MM
PLACE_NEAR=J1800.44:28MM
PLACE_NEAR=J1800.43:28MM
PLACE_NEAR=J1800.47:28MM
NC_ITPXDP_CLK100MP
NC_ITPXDP_CLK100MN
PCH_ITP_PMODE
XDP_DBRESET_L
PP1V05_S0SW
XDP_PCH_TDO R1890 100
XDP_PCH_TDI R1891 51
XDP_PCH_TMS R1892 51
XDP_CPU_TDO R1810 100
XDP_CPU_TCK R1813 51
XDP_PCH_TCK R1897 51
XDP_PCH_TRST_L R1898 51
PROPER WAY TO TERMINATE?
NOSTUFF
R1830 1K
PLACE_NEAR=U0500.E8:2.54MM
R1806 0
PM_SYSRST_L
ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.
R1821 0 XDP_CPU_TDO
R1822 0 XDP_CPU_TRST_L
R1823 0 XDP_CPU_TDI
R1824 0 XDP_CPU_TMS
XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS
PP1V8_S5
C1830 0.1UF
U1830
74AUP1G07GF
SOT891
R1850 100K
SPI_IO2_STRAP_L
R1831 1.5K
SPI_IO<2>
(STRAP TO PCH)
R1832 49.9
NO_XNET_CONNECTION
XDP_PRESENT_L
NEED TO CONNECT TO VCCST, *STG POWER LOGIC
PCH XDP Signals
PCH/XDP Signals
XDP_PCH_OBSDATA_A0 TP1810
XDP_PCH_OBSDATA_A1 TP1811
XDP_PCH_OBSDATA_A2 TP1812
XDP_PCH_OBSDATA_A3 TP1813
XDP_PCH_OBSDATA_B0 TP1814
XDP_PCH_OBSDATA_B1 TP1815
XDP_PCH_OBSDATA_B2 TP1816
XDP_PCH_OBSDATA_B3 TP1817
XDP_PCH_OBSFN_C0 TP1818
XDP_USB_EXTA_OC_L TP1820
XDP_USB_EXTB_OC_L TP1821
XDP_USB_EXTC_OC_L TP1822
XDP_USB_EXTD_OC_L TP1823
XDP_PCH_OBSDATA_D0 TP1824
XDP_PCH_OBSDATA_D1 TP1825
Non-XDP Signals
XDP_JTAG_ISP_TDO TP1819
XDP_JTAG_ISP_TCK TP1826
XDP_JTAG_ISP_TDI TP1827
BOM_COST_GROUP=DEBUG

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

DESIGN: X502/MLB
LAST CHANGE: Mon Jun 15 22:04:28 2015

PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

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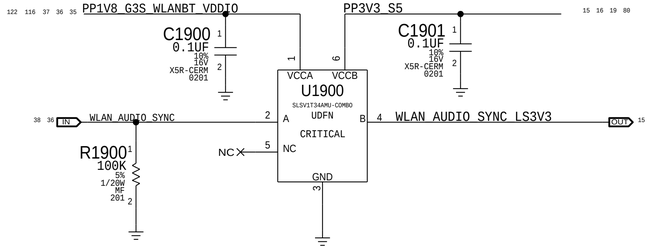
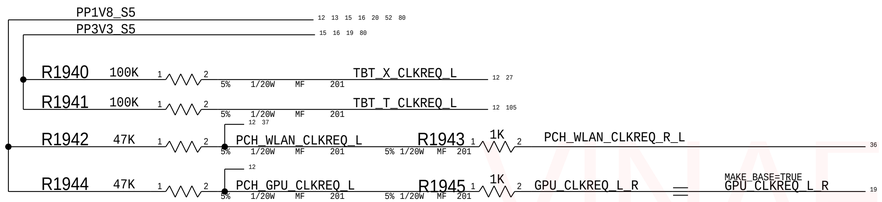
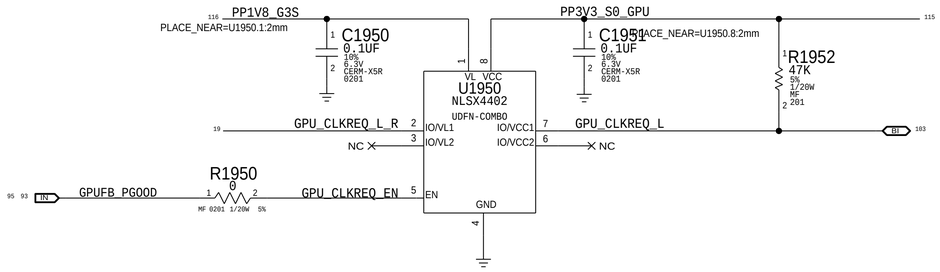


Will be reomved

PCIE CLKREQS





BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: Chipset Support 1

Apple Inc.

DRAWING NUMBER: 051-02643
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BRANCH: evt-0
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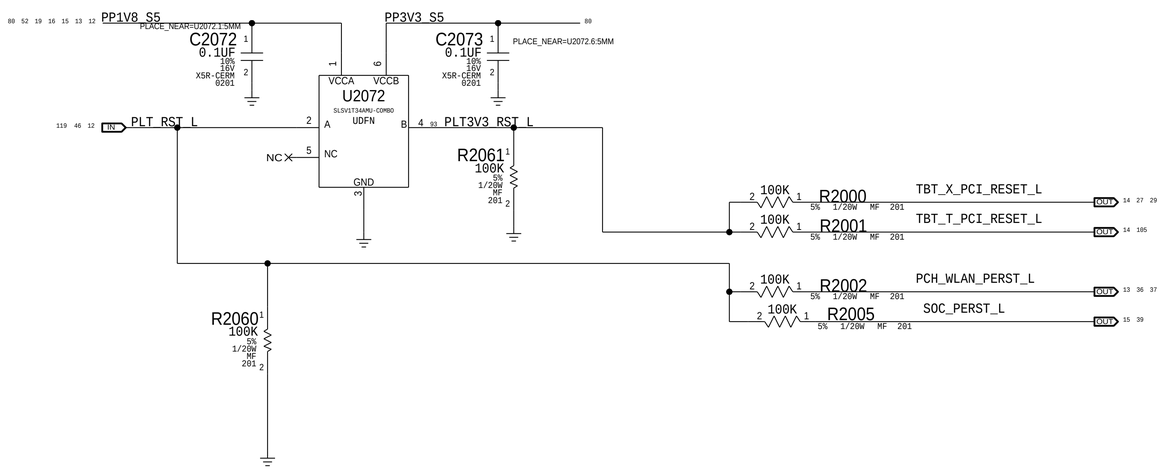
Platform Reset Connections



NC ALIASES 3

NC_PCH_CLK32K_RTCX2 — MAKE_BASE=TRUE — NC_PCH_CLK32K_RTCX2

SIGNAL ALIASES

PCH_DISPA_BCLK — MAKE_BASE=TRUE — PCH_DISPA_BCLK

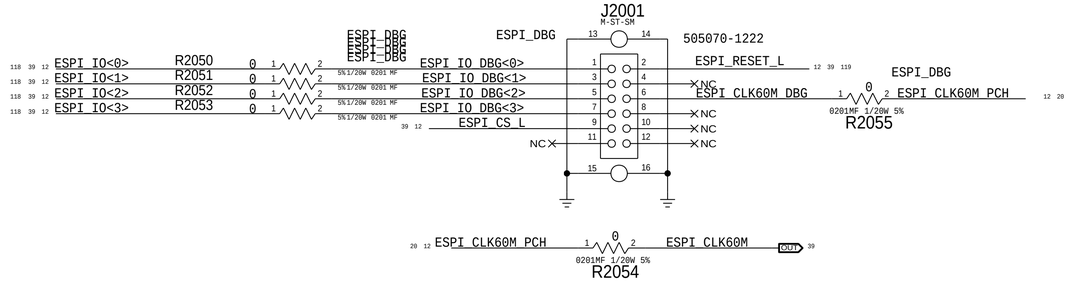
PCH_DISPA_SDI — MAKE_BASE=TRUE — PCH_DISPA_SDI

PCH_DISPA_SDO — MAKE_BASE=TRUE — PCH_DISPA_SDO

NC_ITPXDP_CLK100MN — TRUE — NC_ITPXDP_CLK100MN

NC_ITPXDP_CLK100MP — TRUE — NC_ITPXDP_CLK100MP

eSPI Analyzer
Placement study first



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: Chipset Support 2

Apple Inc.

DRAWING NUMBER: 051-02643 | SIZE: D

REVISION: 4.0.0

BRANCH: evt-0

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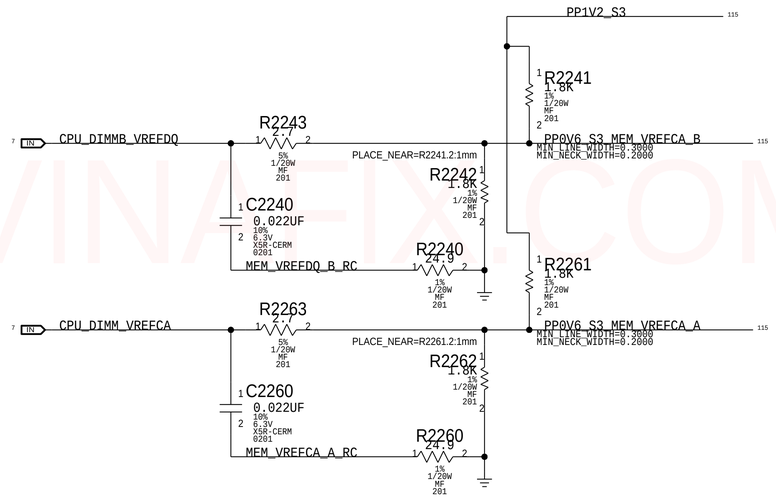
CPU-Based Margining
VRef Dividers

DDR4 VDDQ = 1.2V

MINIMUM Step Size = 0.50% * VDDQ = 6.0mV per step
TYPICAL Step Size = 0.65% * VDDQ = 7.8mV per step
MAXIMUM Step Size = 0.80% * VDDQ = 9.6mV per step

KBL PLATFORM GUIDE Page.102 FOR DDR4 X8 MEMORY DOWN

DDR0_VREF_DQ = Not Used
DDR1_VREF_DQ = Reference For Channel B
DDR_vREF_cA = Reference For Channel A



BOM_COST_GROUP=DRAM

PAGE TITLE: DDR4 VREF Margining

Apple Inc.

DRAWING NUMBER: 051-02643 | SIZE: D
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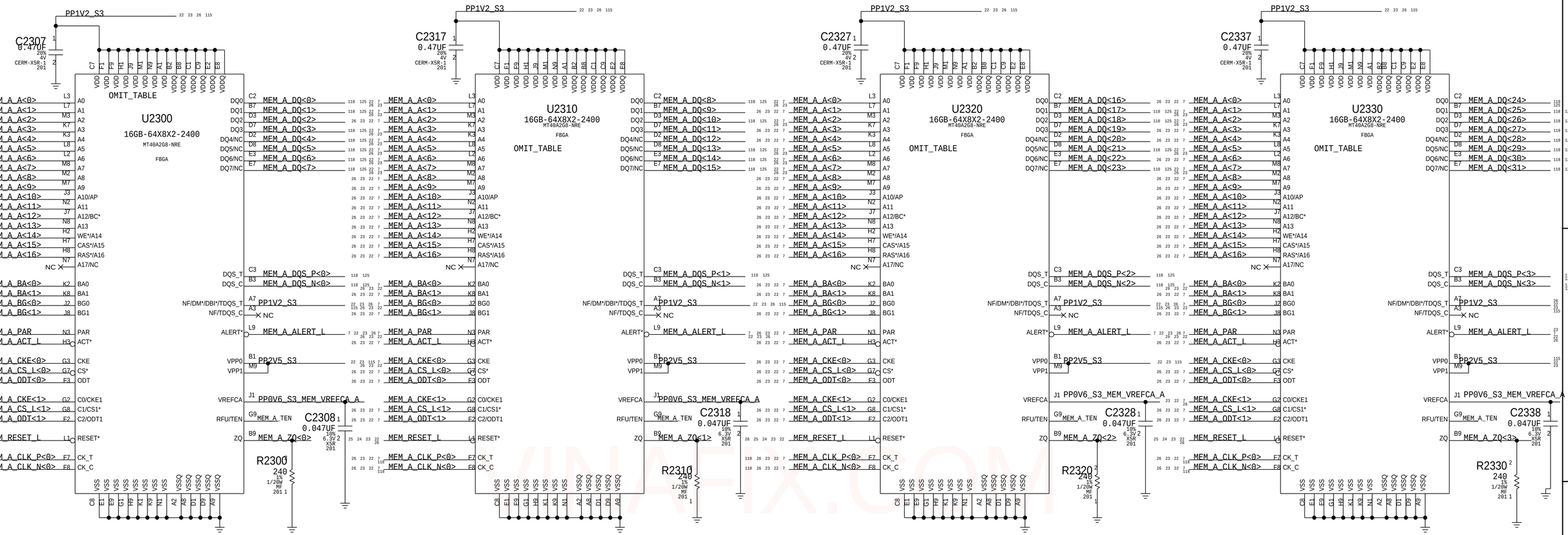
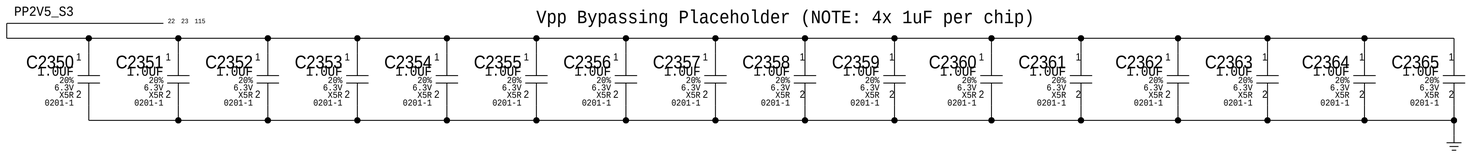
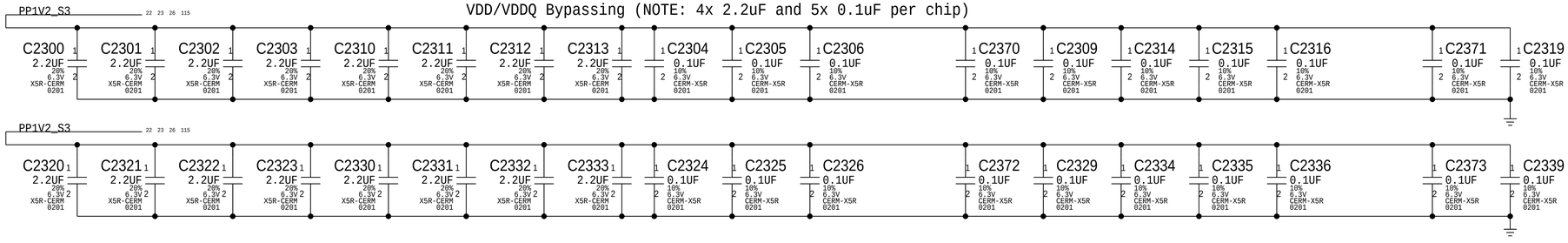


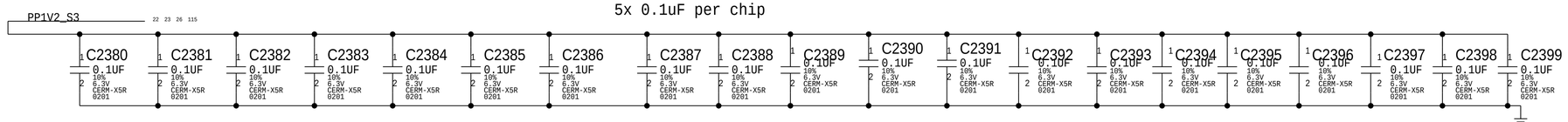
Vpp Bypassing Placeholder (NOTE: 4x 1uF per chip)



VDD/VDDQ Bypassing (NOTE: 4x 2.2uF and 5x 0.1uF per chip)



5x 0.1uF per chip



BOM_COST_GROUP=DRAM

PAGE TITLE	DDR4 SDRAM Channel A 1
	Apple Inc.
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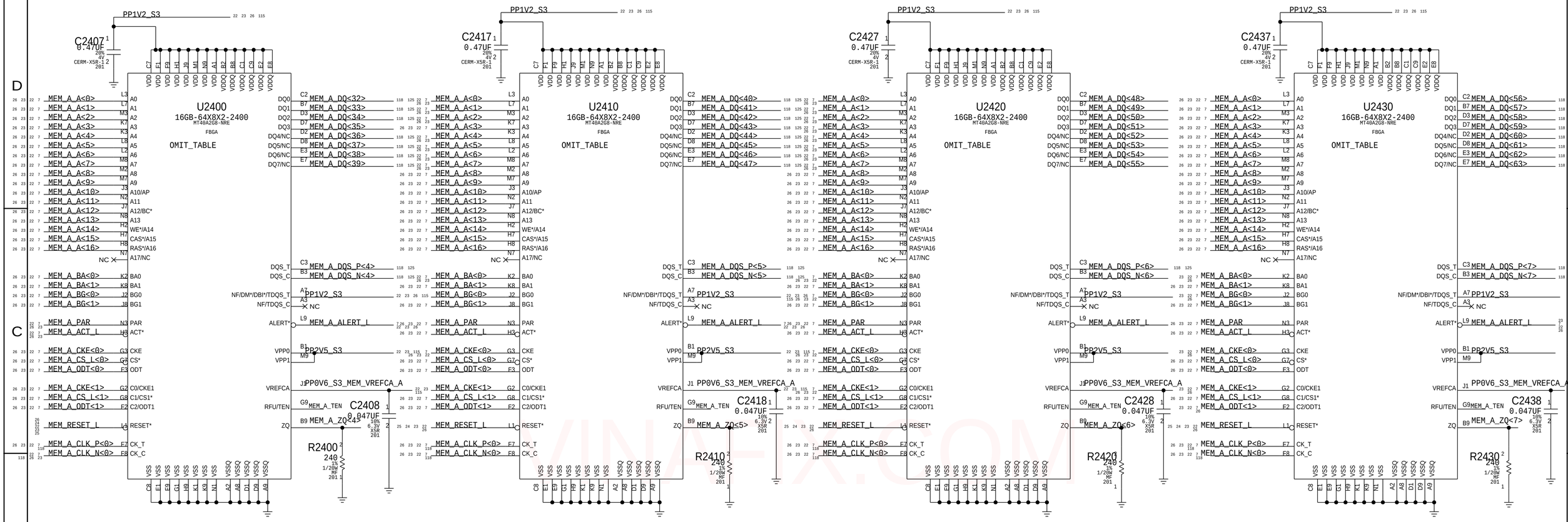

PAGE TITLE	DDR4 SDRAM Channel A 2
Apple Inc.	DRAWING NUMBER 051-02643 · SIZE D
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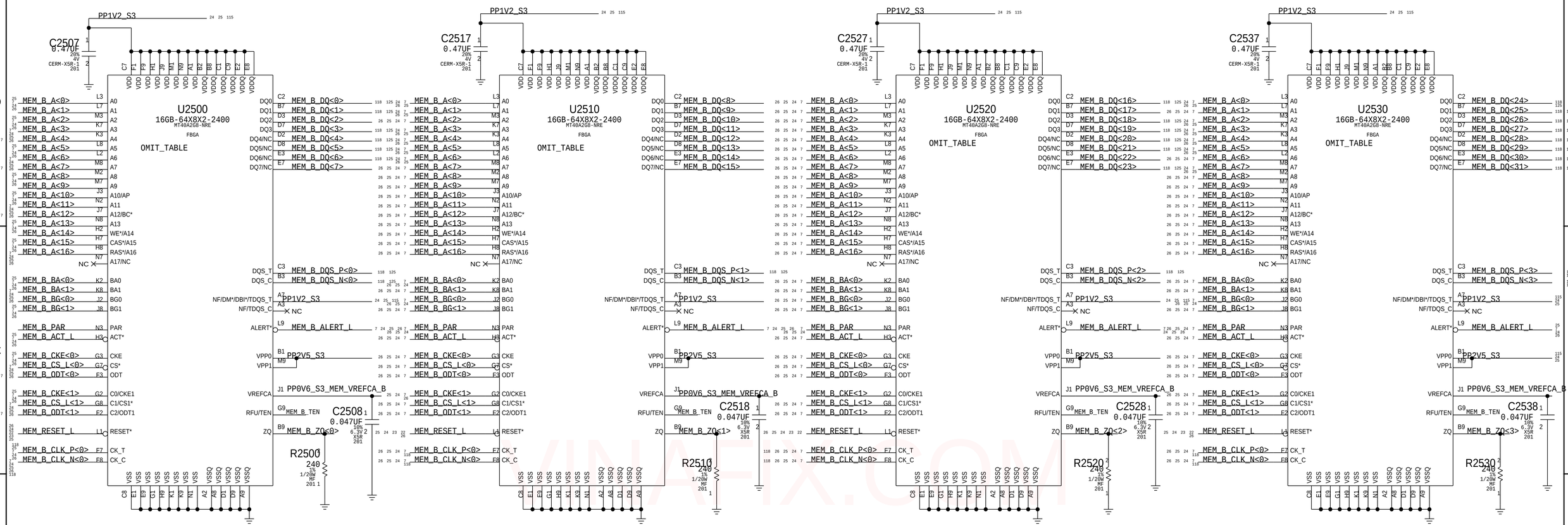

PAGE TITLE

DDR4 SDRAM Channel B 1

Apple Inc.

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U2600 / U2610 / U2620 / U2630
16GB-64X8X2-2400
MT40A2G8-NRE
FBGA
OMIT_TABLE

PP1V2_S3
C2607 0.47UF 20% 4V CERM-X5R-1 201
C2617 0.47UF 20% 4V CERM-X5R-1 201
C2627 0.47UF 20% 4V CERM-X5R-1 201
C2637 0.47UF 20% 4V CERM-X5R-1 201

MEM_B_A<0:16>
MEM_B_BA<0:1>
MEM_B_BG<0:1>
MEM_B_PAR
MEM_B_ACT_L
MEM_B_CKE<0:1>
MEM_B_CS_L<0:1>
MEM_B_ODT<0:1>
MEM_RESET_L
MEM_B_CLK_P<0:1>
MEM_B_CLK_N<0:1>
MEM_B_DQ<0:63>
MEM_B_DQS_P<0:7>
MEM_B_DQS_N<0:7>
MEM_B_ALERT_L
PP1V2_S3
PP2V5_S3
PP0V6_S3_MEM_VREFCA_B
MEM_B_TEN
MEM_B_ZQ<0:7>
R2600 240 1% 1/20W MF 201
R2610 240 1% 1/20W MF 201
R2620 240 1% 1/20W MF 201
R2630 240 1% 1/20W MF 201
C2608 0.047UF 10% 6.3V X5R 201
C2618 0.047UF 10% 6.3V X5R 201
C2628 0.047UF 10% 6.3V X5R 201
C2638 0.047UF 10% 6.3V X5R 201

Vpp Bypassing Placeholder (NOTE: 4x 1uF per chip)

PP2V5_S3
C2650 C2651 C2652 C2653 C2654 C2655 C2656 C2657 C2658 C2659 C2660 C2661 C2662 C2663 C2664 C2665
1.0UF 20% 6.3V X5R 0201-1

VDD/VDDQ Bypassing (NOTE: 4x 2.2uF and 5x 0.1uF per chip)

PP1V2_S3
C2600 C2601 C2602 C2603 C2610 C2611 C2612 C2613 C2604 C2605 C2606 C2670 C2609 C2614 C2615 C2616 C2671 C2619
2.2UF 20% 6.3V X5R-CERM 0201

VDD/VDDQ Bypassing (NOTE: 4x 2.2uF and 5x 0.1uF per chip)

PP1V2_S3
C2620 C2621 C2622 C2623 C2630 C2631 C2632 C2633 C2624 C2625 C2626 C2672 C2629 C2634 C2635 C2636 C2673 C2639
2.2UF 20% 6.3V X5R-CERM 0201

5x 0.1uF per chip

PP1V2_S3
C2680 C2681 C2682 C2683 C2684 C2685 C2686 C2687 C2688 C2689 C2690 C2691 C2692 C2693 C2694 C2695 C2696 C2697 C2698 C2699
0.1UF 10% 6.3V CERM-X5R 0201

BOM_COST_GROUP=DRAM

PAGE TITLE	DDR4 SDRAM Channel B 2
Apple Inc.	DRAWING NUMBER 051-02643
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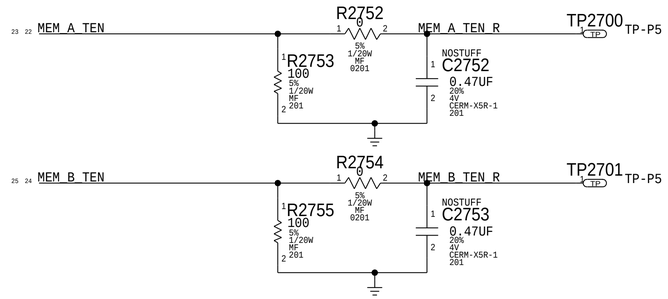
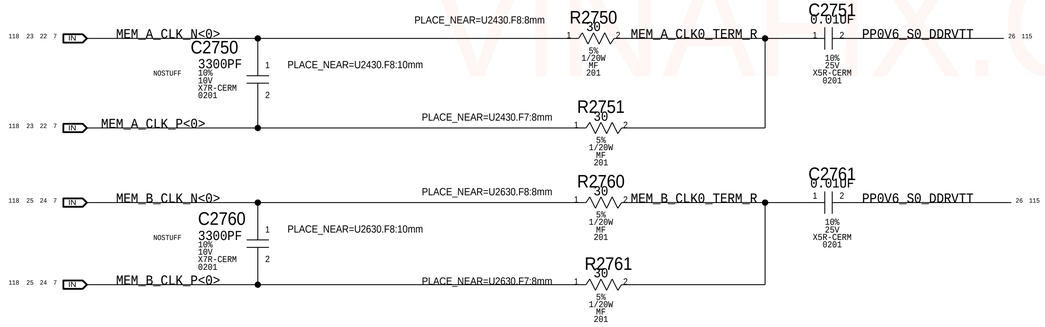
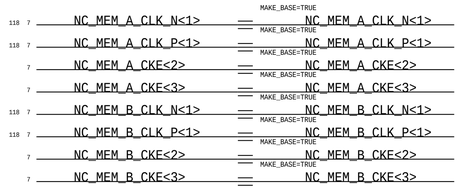
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

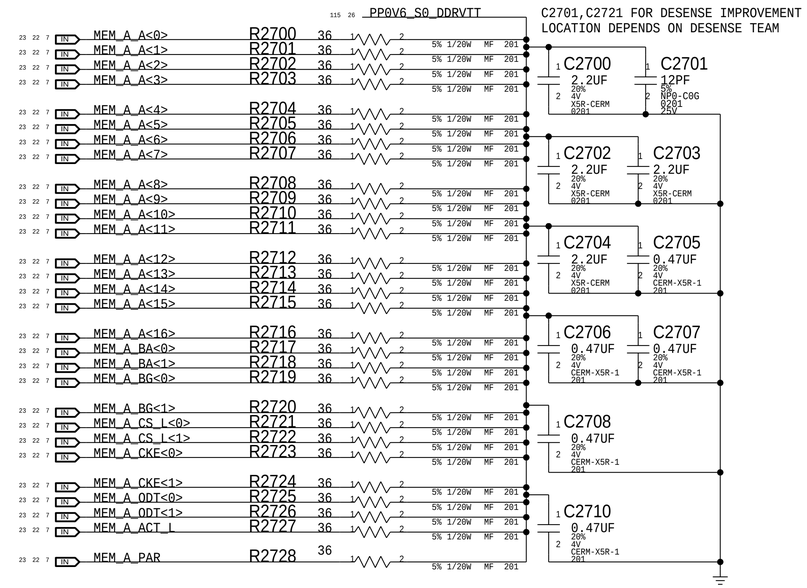


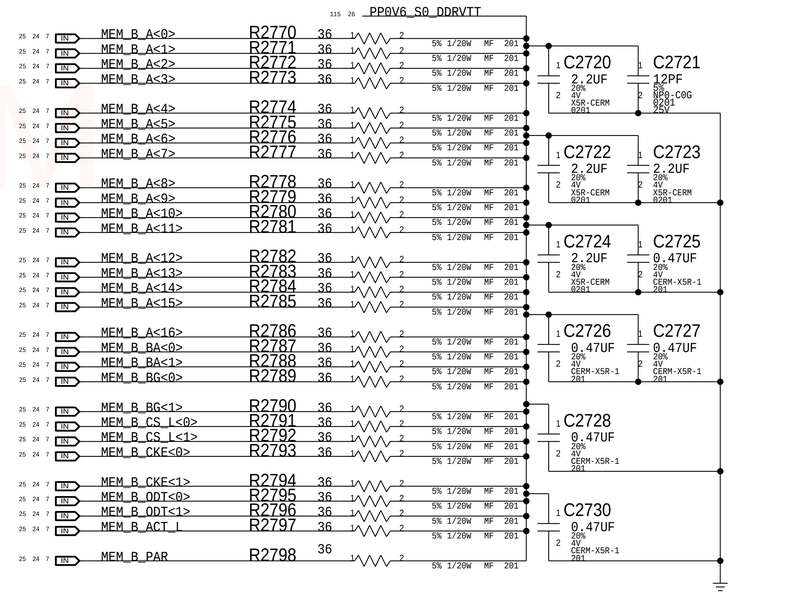
MEM Clock Termination

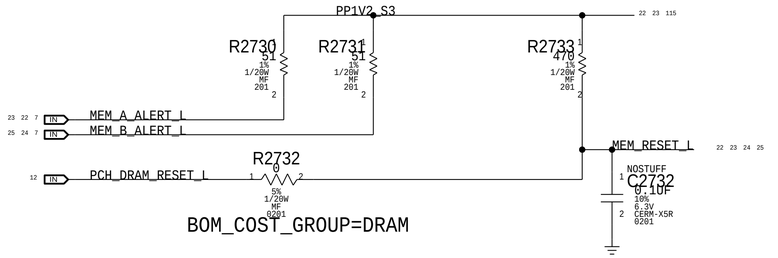
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM











BOM_COST_GROUP=DRAM

PAGE TITLE

DDR4 Termination

Apple Inc.

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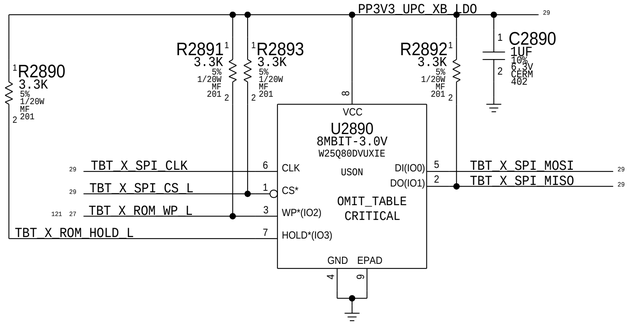
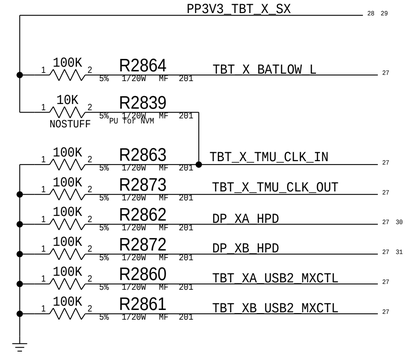


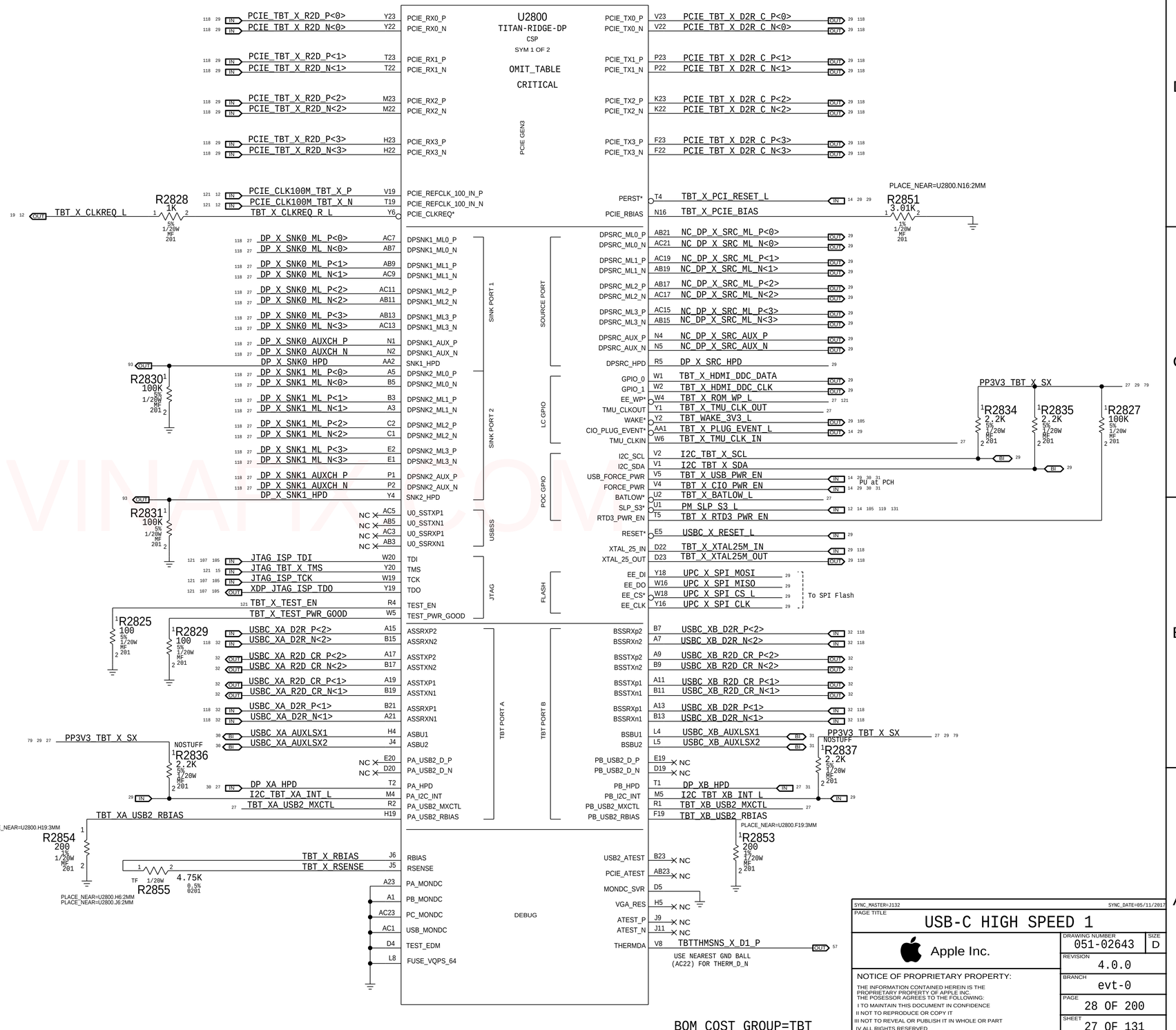
SNK0 AC Coupling

DP_X_SNK0_ML_C_P<0>	C2820	0.22UF	DP_X_SNK0_ML_P<0>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<0>	C2821	0.22UF	DP_X_SNK0_ML_N<0>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<1>	C2822	0.22UF	DP_X_SNK0_ML_P<1>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<1>	C2823	0.22UF	DP_X_SNK0_ML_N<1>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<2>	C2824	0.22UF	DP_X_SNK0_ML_P<2>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<2>	C2825	0.22UF	DP_X_SNK0_ML_N<2>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<3>	C2826	0.22UF	DP_X_SNK0_ML_P<3>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<3>	C2827	0.22UF	DP_X_SNK0_ML_N<3>	GND_VOID=TRUE
DP_X_SNK0_AUXCH_C_P	C2828	0.1UF	DP_X_SNK0_AUXCH_P	GND_VOID=TRUE
DP_X_SNK0_AUXCH_C_N	C2829	0.1UF	DP_X_SNK0_AUXCH_N	GND_VOID=TRUE

SNK1 AC Coupling

DP_X_SNK1_ML_C_P<0>	C2830	0.22UF	DP_X_SNK1_ML_P<0>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<0>	C2831	0.22UF	DP_X_SNK1_ML_N<0>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<1>	C2832	0.22UF	DP_X_SNK1_ML_P<1>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<1>	C2833	0.22UF	DP_X_SNK1_ML_N<1>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<2>	C2834	0.22UF	DP_X_SNK1_ML_P<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<2>	C2835	0.22UF	DP_X_SNK1_ML_N<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<3>	C2836	0.22UF	DP_X_SNK1_ML_P<3>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<3>	C2837	0.22UF	DP_X_SNK1_ML_N<3>	GND_VOID=TRUE
DP_X_SNK1_AUXCH_C_P	C2838	0.1UF	DP_X_SNK1_AUXCH_P	GND_VOID=TRUE
DP_X_SNK1_AUXCH_C_N	C2839	0.1UF	DP_X_SNK1_AUXCH_N	





SYNC_MASTER=J132 SYNC_DATE=05/11/2017

PAGE TITLE

USB-C HIGH SPEED 1

Apple Inc.

DRAWING NUMBER 051-02643 SIZE D

REVISION 4.0.0

BRANCH evt-0

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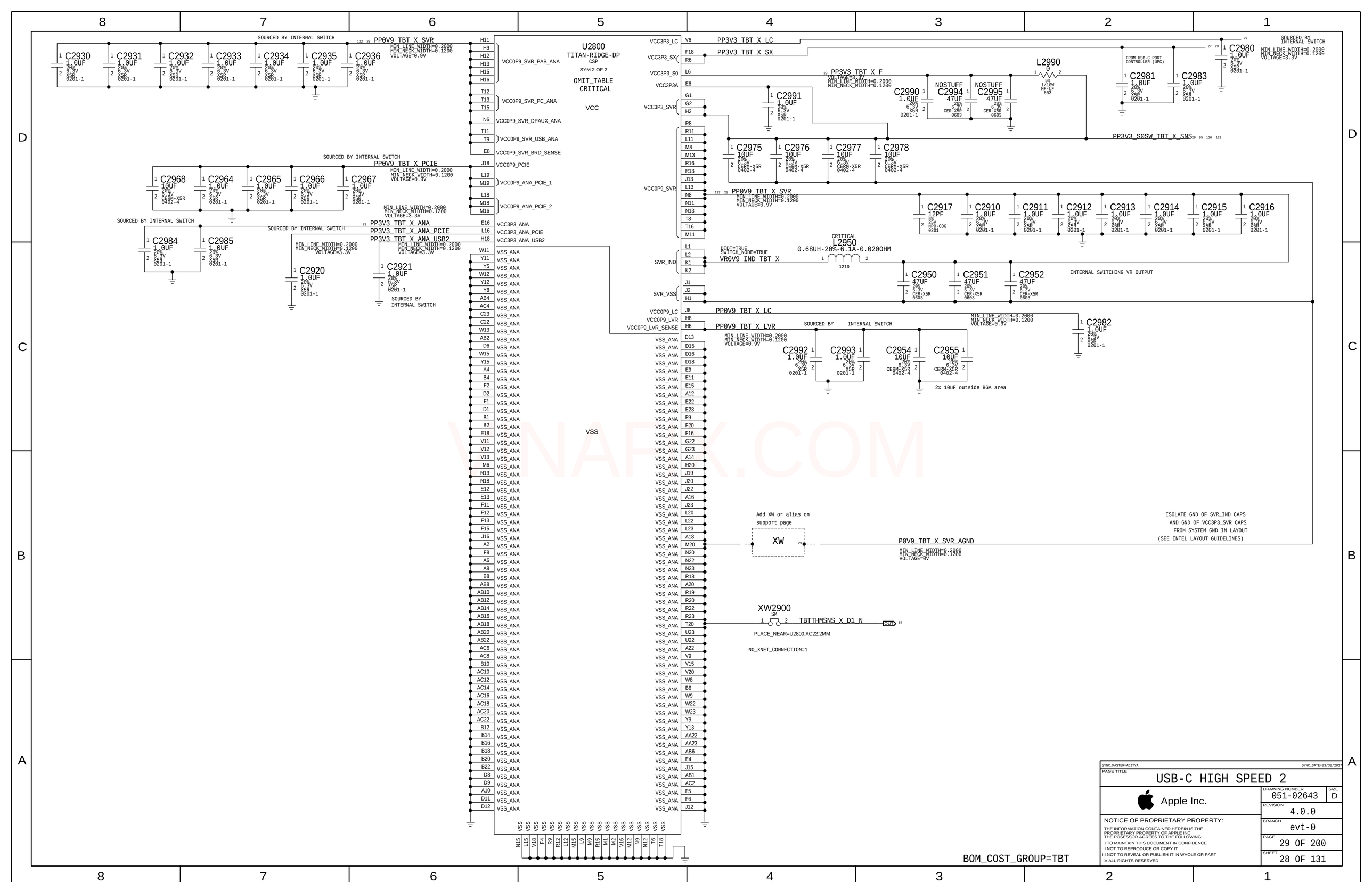


TBT WAKE LEVEL SHIFTER

PP3V3_G3H_RTC_X (116 29) → R3065 100K 5% 1/20W MF 0201

Q3001 DMN32D2LFB4 PDFN1006H4-3

PP1V8_SLPS2R (80 29 107) → Q3001 G

SMC HAS IPU

TBT_WAKE_L (39) → OUT

Q3001 S → GND

Q3001 D → TBT_WAKE_3V3_L → IN (27 29 105)

DP SRC OPTIONS

IF DP SRC NOT USED

DP_X_SRC_HPD (27) → R3040 100K 1/20W 5% MF 201

=DP_X_SRC_ML_P<3..0> (27)	NC_DP_X_SRC_ML_P<3..0>	MAKE_BASE=TRUE NO_TEST=1
=DP_X_SRC_ML_N<3..0> (27)	NC_DP_X_SRC_ML_N<3..0>	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_AUX_P (27)	NC_DP_X_SRC_AUX_P	MAKE_BASE=TRUE NO_TEST=1
NC_DP_X_SRC_AUX_N (27)	NC_DP_X_SRC_AUX_N	MAKE_BASE=TRUE NO_TEST=1

FUSES FOR UPC

PLACE_NEAR=Q3100:5MM

CRITICAL

F3000 0603 6AMP-32V-0.00950HM

PP20V_USBC_XA_VBUS (30 29) → F3000 → PP20V_USBC_XA_VBUS_F (29 30)

PLACE_NEAR=Q3200:5MM

CRITICAL

F3001 0603 740S0135 6AMP-32V-0.00950HM

PP20V_USBC_XB_VBUS (31 29) → F3001 → PP20V_USBC_XB_VBUS_F (31)

25MHz xtal

TBT_X_XTAL25M_OUT (IN) → C3002 20PF 5% 25V C0G 0201 → Y3000

to/from Ridge

CRITICAL

Y3000 25MHZ-25PPM-20PF-500HM 2.00X1.60-SM

Y3000 → C3003 20PF 5% 25V C0G 0201 → TBT_X_XTAL25M_IN (OUT)

TR/ACE SPI BUS SERIES R'S

USBC DEBUG CONN

TBT_X_SPI_CLK (27)	R3094 100	TBT_X_SPI_CLK_DBG	29
TBT_X_SPI_CS_L (27)	R3095 15	UPC_XB_SPI_CLK	IN 31
TBT_X_SPI_MOSI (27)	R3096 15	UPC_XB_SPI_CS_L	IN 31
TBT_X_SPI_MISO (27)	R3097 15	UPC_XB_SPI_MOSI	IN 31
	R3098 15	UPC_XB_SPI_MISO	OUT 31
ROM	R3090 15	UPC_X_SPI_CLK	IN 27 29
	R3091 15	UPC_X_SPI_CS_L	IN 27 29
	R3092 15	UPC_X_SPI_MOSI	IN 27 29
	R3093 15	UPC_X_SPI_MISO	OUT 27 29

Ace

AR

Ridge and ACE PDs

UPC_X_5V_EN (30 29)	R3032 100K	2
TBT_XA_LSTX (30)	R3020 1M	2
TBT_XA_LSRX (30)	R3021 1M	2
TBT_XB_LSTX (31)	R3022 1M	2
TBT_XB_LSRX (31)	R3023 1M	2
USB_UPC_XA_P (30)	R3024 1M	2
USB_UPC_XA_N (30)	R3025 1M	2

5% 1/20W MF 201

RIDGE ARKANOID CONN

Place on bottom

J3001 M-ST-SM 505070-1222

USBC_DBG (13)

TBT_X_PLUG_EVENT_L (27 14)	1	2 TBT_X_PCI_RESET_L (14 20 27)
TBT_WAKE_3V3_L (105 29 27)	3	4 USBC_X_RESET_L (27 29)
TBT_X_CIO_PWR_EN (30 27 14 31)	5	6 PP3V3_TBT_X_SX (27 29 79)
TBT_X_USB_PWR_EN (30 27 14 31)	7	8 PP3V3_TBT_T_ANA_PCIE (106)
TBT_POC_RESET (31 30 29)	9	10 PP3V3_TBT_X_ANA (28)
PP3V3_TBT_X_F (28)	11	12 PP3V3_TBT_X_LC (28)
	15	16

ACE ARKANOID CONN

Place on bottom

USBC_DBG

J3000 505070-1222 M-ST-SM

CKPLUS_WAIVE=I2C_PULLUP (29)

I2C_TBT_XB_INT_L	1	2 I2C_TBT_XA_INT_L (27 29)
I2C_UPC_X_SCL2	3	4 I2C_TBT_X_SDA (27 29)
I2C_UPC_X_SDA2	5	6 I2C_TBT_X_SCL (27 29)
UPC_I2C_INT_L (107 51 39)	7	8 I2C_UPC_XA_DBG_CTL_SDA (29 30)
TBT_X_SPI_CLK_DBG (29)	9	10 I2C_UPC_XA_DBG_CTL_SCL (29 30)
UPC_XA_UART_TX (31 30)	11	12 UPC_XA_UART_RX (30 31)
	15	16

ACE A RPD STRAPPING

USBC_XA_CC1 (30) = USBC_XA_CC1 (30 33) MAKE_BASE=TRUE

USBC_XA_CC2 (30) = USBC_XA_CC2 (30 33) MAKE_BASE=TRUE

ACE B RPD STRAPPING

USBC_XB_CC1 (31) = USBC_XB_CC1 (31 33) MAKE_BASE=TRUE

USBC_XB_CC2 (31) = USBC_XB_CC2 (31 33) MAKE_BASE=TRUE

GND ALIASES

MAKE_BASE=TRUE

GND (31) GND (30) GND (30) GND (30) GND (30) GND (30) GND (31) GND (30)

RIDGE 0.9V SVR XW

P0V9_TBT_X_SVR_AGND (28) → XW3000 SM → NO_XNET_CONNECTION=1

NC ALIASES / NO TEST

NO_TEST=1

NC_UPC_XB_I2C_ADDR (31) IN

NC_USBC_XA_USB_BOTP (30) = NC_USBC_XA_USB_BOTP MAKE_BASE=TRUE

NC_USBC_XA_USB_BOTN (30) = NC_USBC_XA_USB_BOTN MAKE_BASE=TRUE NO_TEST=1

SIGNAL ALIASES

UPC_X_5V_EN (30 29)	= UPC_X_5V_EN	(34) MAKE_BASE=TRUE
UPC_X_5V_EN (31)		
USB2_UPC_XB_P (31)	= USB2_UPC_XB_P	MAKE_BASE=TRUE
USB2_UPC_XB_P (14)		
USB2_UPC_XB_N (31)	= USB2_UPC_XB_N	MAKE_BASE=TRUE
USB2_UPC_XB_N (14)		
USB2_UPC_XA_P (29)	= USB2_UPC_XA_P	MAKE_BASE=TRUE
USB2_UPC_XA_P (14)		
USB2_UPC_XA_N (29)	= USB2_UPC_XA_N	MAKE_BASE=TRUE
USB2_UPC_XA_N (14)		
UPC_PMU_RESET (30)	= UPC_PMU_RESET	MAKE_BASE=TRUE (67 77 107 119)
UPC_PMU_RESET (31)		
USBC_X_RESET_L (31)	= USBC_X_RESET_L	MAKE_BASE=TRUE (27 29)
UPC_X_SPI_CLK (29 27)	= UPC_X_SPI_CLK	MAKE_BASE=TRUE
UPC_X_SPI_CS_L (29 27)	= UPC_X_SPI_CS_L	MAKE_BASE=TRUE
UPC_X_SPI_MOSI (29 27)	= UPC_X_SPI_MOSI	MAKE_BASE=TRUE
UPC_X_SPI_MISO (29 27)	= UPC_X_SPI_MISO	MAKE_BASE=TRUE
UPC_T_SPI_CLK (107 105)	= UPC_T_SPI_CLK	MAKE_BASE=TRUE
UPC_T_SPI_CS_L (107 105)	= UPC_T_SPI_CS_L	MAKE_BASE=TRUE
UPC_T_SPI_MOSI (107 105)	= UPC_T_SPI_MOSI	MAKE_BASE=TRUE
UPC_T_SPI_MISO (107 105)	= UPC_T_SPI_MISO	MAKE_BASE=TRUE

TBT_POC_RESET (31 30 29 IN) = TBT_POC_RESET (OUT 15 107) MAKE_BASE=TRUE

UPC_XA_FAULT_L (30 IN) → R3078 0 5% MF 1/20W 0201 → XDP_USB_EXTA_OC_L (14)

UPC_XB_FAULT_L (31 IN) → R3079 0 5% MF 1/20W 0201 → XDP_USB_EXTB_OC_L (14)

TP_USBC_XA_RESET_L (30) = TP_USBC_XA_RESET_L MAKE_BASE=TRUE

TBT_X_HDMI_DDC_DATA (27) = TBT_X_HDMI_DDC_DATA (95 120) MAKE_BASE=TRUE

TBT_X_HDMI_DDC_CLK (27) = TBT_X_HDMI_DDC_CLK (95 120) MAKE_BASE=TRUE

POWER ALIASES

PP3V3_UPC_XB_LDO (27)	= PP3V3_UPC_XB_LDO	(31) MAKE_BASE=TRUE
PP3V3_UPC_XB_LDO (31)		
PP3V3_UPC_XA_LDO (30)	= PP3V3_UPC_XA_LDO	MAKE_BASE=TRUE
PP20V_USBC_XA_VBUS (30 29)	= PP20V_USBC_XA_VBUS	MAKE_BASE=TRUE (32 119 120 122)
PP20V_USBC_XB_VBUS (31 29)	= PP20V_USBC_XB_VBUS	MAKE_BASE=TRUE (32 120 122)
PPDCIN_G3H (108 107 31 30 109)	= PPDCIN_G3H	MAKE_BASE=TRUE MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=5V (63 55 68 119 122)
PP5V_S4_X_USBC (30)	= PP5V_S4_X_USBC	MAKE_BASE=TRUE MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=5V
PP5V_S4_X_USBC (31)		
PP5V_S4_X_USBC (122 34)		
PP3V3_S0SW_TBT_X_SNS (122 116 95 28)	= PP3V3_S0SW_TBT_X_SNS	MAKE_BASE=TRUE MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V
PP3V3_TBT_X_SX (30)	= PP3V3_TBT_X_SX	MAKE_BASE=TRUE MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000 (27 29 79)
PP3V3_TBT_X_SX (31)		
PP3V3_TBT_X_SX (28 27)		
PP1V8_SLPS2R (30)	= PP1V8_SLPS2R	(29 80 107) MAKE_BASE=TRUE
PP1V8_SLPS2R (31)		

DEBUG ALIASES

PCH_UART_DEBUG_R2D (31)	= PCH_UART_DEBUG_R2D	MAKE_BASE=TRUE (15 119 126)
PCH_UART_DEBUG_D2R (31)	= PCH_UART_DEBUG_D2R	MAKE_BASE=TRUE (15 119 126)
SOC_DFU_STATUS (30)	= SOC_DFU_STATUS	MAKE_BASE=TRUE (38 119 131)
SOC_FORCE_DFU (30)	= SOC_FORCE_DFU	MAKE_BASE=TRUE (38 77 119 131)

SWD_SOC_SWCLK (47 29) → R3076 0 5% MF 1/20W 0201 → UPC_XB_DBG3 (BI 31 119)

PLACE_NEAR=U3000.24:5mm

SWD_SOC_SWDIO (47 29) → R3077 0 5% MF 1/20W 0201 → UPC_XB_DBG4 (BI 31 119)

PLACE_NEAR=U3000.23:5mm

Diodes for USB2

USBC_XA_USB_DBG_BOT_P (32 29)

USBC_XA_USB_DBG_BOT_N (32 29)

USBC_XA_USB_DBG_TOP_N (32 29)

USBC_XA_USB_DBG_TOP_P (32 29)

PLACE_NEAR=U3000.19:10mm

PLACE_NEAR=U3000.18:10mm

PLACE_NEAR=U3000.15:10mm

PLACE_NEAR=U3000.16:10mm

D3001 BAS70LP DFN1006-2 (K A)

D3002 BAS70LP DFN1006-2 (K A)

D3003 BAS70LP DFN1006-2 (K A)

D3004 BAS70LP DFN1006-2 (K A)

I2C SERIES R'S

I2C_UPC_X_SDA2 (30)	R3041 33	I2C_UPC_SDA (51)
I2C_UPC_X_SDA2 (31)		I2C_UPC_SDA (51)
I2C_UPC_X_SDA2 (29)		
I2C_UPC_X_SCL2 (30)	R3042 33	I2C_UPC_SCL (51)
I2C_UPC_X_SCL2 (31)		I2C_UPC_SCL (51)
I2C_UPC_X_SCL2 (29)		

PLACE_NEAR=U3900.J4:5mm

PLACE_NEAR=U3900.M3:10mm

5% 1/20W MF 201

MAKE_BASE=TRUE

PP20V_USBC_XA_VBUS_F (30 29) → R3080 30K 5% 1/20W MF 201 → SOC_USB_VBUS (30 119 126)

D3080 DFN1006 BZT52C3V0LP (K A)

TBT to ACE

TBT
Alpine Ridge U2800
(MASTER)

MAKE_BASE=TRUE (27 29)	I2C_TBT_X_SCL	I2C_TBT_X_SCL (30)
MAKE_BASE=TRUE (27 29)	I2C_TBT_X_SDA	I2C_TBT_X_SDA (30)
MAKE_BASE=TRUE (27 29)	I2C_TBT_XA_INT_L	I2C_TBT_XA_INT_L (30)
MAKE_BASE=TRUE	I2C_TBT_XB_INT_L	

Pri ACE
U3100
(Write: 0x70 Read: 0x71)

I2C_TBT_X_SCL	I2C_TBT_X_SCL (30)
I2C_TBT_X_SDA	I2C_TBT_X_SDA (30)
I2C_TBT_XA_INT_L	I2C_TBT_XA_INT_L (30)

Sec ACE
U3200
(Write: 0x7E Read: 0x7F)

I2C_TBT_X_SCL	I2C_TBT_X_SCL (31)
I2C_TBT_X_SDA	I2C_TBT_X_SDA (31)
I2C_TBT_XB_INT_L	I2C_TBT_XB_INT_L (31)

Ridge PCIE Caps

GND_VOID=TRUE

PCIE_TBT_X_R2D_C_P<0> (117 118)	C3040 0.22UF	PCIE_TBT_X_R2D_P<0> (OUT 27 118)
PCIE_TBT_X_R2D_C_N<0> (117 118)	C3041 0.22UF	PCIE_TBT_X_R2D_N<0> (OUT 27 118)
PCIE_TBT_X_R2D_C_P<1> (117 118)	C3042 0.22UF	PCIE_TBT_X_R2D_P<1> (OUT 27 118)
PCIE_TBT_X_R2D_C_N<1> (117 118)	C3043 0.22UF	PCIE_TBT_X_R2D_N<1> (OUT 27 118)
PCIE_TBT_X_R2D_C_P<2> (117 118)	C3044 0.22UF	PCIE_TBT_X_R2D_P<2> (OUT 27 118)
PCIE_TBT_X_R2D_C_N<2> (117 118)	C3045 0.22UF	PCIE_TBT_X_R2D_N<2> (OUT 27 118)
PCIE_TBT_X_R2D_C_P<3> (117 118)	C3046 0.22UF	PCIE_TBT_X_R2D_P<3> (OUT 27 118)
PCIE_TBT_X_R2D_C_N<3> (118 117)	C3047 0.22UF	PCIE_TBT_X_R2D_N<3> (OUT 27 118)
PCIE_TBT_X_D2R_C_P<0> (118 27)	C3050 0.22UF	PCIE_TBT_X_D2R_P<0> (OUT 117 118)
PCIE_TBT_X_D2R_C_N<0> (118 27)	C3051 0.22UF	PCIE_TBT_X_D2R_N<0> (OUT 117 118)
PCIE_TBT_X_D2R_C_P<1> (118 27)	C3052 0.22UF	PCIE_TBT_X_D2R_P<1> (OUT 117 118)
PCIE_TBT_X_D2R_C_N<1> (118 27)	C3053 0.22UF	PCIE_TBT_X_D2R_N<1> (OUT 117 118)
PCIE_TBT_X_D2R_C_P<2> (118 27)	C3054 0.22UF	PCIE_TBT_X_D2R_P<2> (OUT 117 118)
PCIE_TBT_X_D2R_C_N<2> (118 27)	C3055 0.22UF	PCIE_TBT_X_D2R_N<2> (OUT 117 118)
PCIE_TBT_X_D2R_C_P<3> (118 27)	C3056 0.22UF	PCIE_TBT_X_D2R_P<3> (OUT 117 118)
PCIE_TBT_X_D2R_C_N<3> (118 27)	C3057 0.22UF	PCIE_TBT_X_D2R_N<3> (OUT 117 118)

GND_VOID=TRUE

0201 X5R 6.3V 20%

DCI / PCH USB3

USB3_EXTA_R2D_C_P (14 IN) → C3020 0.1UF 10% 16V X5R-CERM 0201 → USB3_EXTA_R2D_P

USB3_EXTA_R2D_C_N (14 IN) → C3021 0.1UF 10% 16V X5R-CERM 0201 → USB3_EXTA_R2D_N

PP3V3_G3H_RTC_X (116 29) → C3022 0.1UF 10% 16V X5R-CERM 0201

L3000 90-OHM-0.1A EXC4X4E_CMC-SCP-1

USB2_UPC_XA_P (29) ↔ USB2_UPC_XA_N (29)

PLACE_NEAR=U3000:5mm

U3000 PI3USB32324 QFN-20

USB3_EXTA_D2R_P (14 OUT)	PCH_USB3_RX_P 3	USB2_RP_P 8	USB_DBG_PCH_XA_F_P
USB3_EXTA_D2R_N (14 OUT)	PCH_USB3_RX_N 4	USB2_RP_N 9	USB_DBG_PCH_XA_F_N
USB3_EXTA_R2D_P	PCH_USB3_TX_P 6	USB2_B_P 16	USBC_XA_USB_DBG_BOT_P (BI 29 32)
USB3_EXTA_R2D_N	PCH_USB3_TX_N 7	USB2_B_N 15	USBC_XA_USB_DBG_BOT_N (BI 29 32)
USB_SOC_TYPEC_P (126 119 BI)	USB2_EP_P 1	USB2_T_N 18	USBC_XA_USB_DBG_TOP_N (BI 29 32)
USB_SOC_TYPEC_N (126 119 BI)	USB2_EP_N 2	USB2_T_P 19	USBC_XA_USB_DBG_TOP_P (BI 29 32)
SWD_SOC_SWCLK (47 29 OUT)	SWCLK 24	SDA 10	I2C_UPC_XA_DBG_CTL_SDA (BI 29 30)
SWD_SOC_SWDIO (47 29 BI)	SWDIO 23	SCL 13	I2C_UPC_XA_DBG_CTL_SCL (BI 29 30)
USBC_XA_USB_TOP_P (30 BI)	ANALOG1 11	DEBUG1 22	UPC_XA_DBG1 (BI 30)
USBC_XA_USB_TOP_N (30 BI)	ANALOG2 12	DEBUG2 21	UPC_XA_DBG2 (BI 30)

GND 5 14 17 25 EPAD

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C X Support

Apple Inc.

DRAWING NUMBER 051-02643 SIZE D

REVISION 4.0.0

BRANCH evt-0

PAGE 30 OF 200

SHEET 29 OF 131

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

CRITICAL
Q3100
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

29 PP20V_USBC_XA_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V

29 PP20V_USBC_XA_VBUS

C3101 1UF 10% 50V X5R 0402

PPDCIN_G3H 29 31 107 108 109
MAX 100uF TOTAL ON RAIL

UPC_XA_GATE1
TP_Q3100_DRAIN
UPC_XA_GATE2

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
PP3V3_UPC_XA_LDO 29

PP3V3_TBT_X_SX 29

PP1V8_UPC_XA_LDOA
PP1V8_UPC_XA_LDOD
PP1V1_UPC_XA_LDO_BMC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V

29 PP1V8_SLPS2R
C3115 1.0UF 20% 6.3V X5R 0201-1

116 PP3V3_G3H_RTC_X
R3169 100K 5% 1/20W MF 201
PHV_INT_XA_G3H

29 PP5V_S4_X_USBC
CAP FOR PP_5V0 ON VR PAGE

C3100 10UF 20% 6.3V CERM-X5R 0402-1

C3104 2.2UF 20% 6.3V X5R-CERM 0201
C3105 1.0UF 20% 6.3V X5R 0201-1
C3106 0.47UF 10% 6.3V CERM-X5R 0201
C3108 10UF 20% 6.3V CERM-X5R 0402-1

PULL R3109 AND R3108 UP TO ACE1 LDOS FOR 1ST BRIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES

PP3V3_UPC_XA_LDO 29

1M R3109 5% 1/20W MF 201 I2C_UPC_XA_DBG_CTL_SCL 29 30
1M R3108 5% 1/20W MF 201 I2C_UPC_XA_DBG_CTL_SDA 29 30

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR

USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS

U3100
CD3215A
BGA

31 29 IN	TBT_POC_RESET	E11	MRESET	PRIMARY ONLY
29 OUT	TP_USBC_XA_RESET_L	F11	RESET*	PRIMARY ONLY
121 IN	UPC_XA_GPIO0	B2	GPIO0	
119 77 141 IN	PMU_ACTIVE_READY	C2	GPIO1	
31 29 27 14 IN	TBT_X_CIO_PWR_EN	D10	GPIO2	
31 29 27 14 IN	TBT_X_USB_PWR_EN	G11	GPIO3	
27 OUT	DP_XA_HPD	C10	GPIO4	
29 OUT	UPC_PMU_RESET	E10	GPIO5	
29 OUT	UPC_X_5V_EN	G10	GPIO6	
119 39 31 OUT	SOC_DOCK_CONNECT	D7	GPIO7	
29 OUT	UPC_XA_FAULT_L	H6	GPIO8	
29 IN	GND	F10	BUSPOWERZ	
GND I2C ADDR PRIMARY ONLY	GND	F1	I2C_ADDR	
	UPC_XA_R_OSC	G2	R_OSC	
30 29	I2C_UPC_XA_DBG_CTL_SCL	E4	DEBUG_CTL1	
30 29	I2C_UPC_XA_DBG_CTL_SDA	D5	DEBUG_CTL2	
29 BI	I2C_TBT_X_SDA	D1	I2C_SDA1	
29 BI	I2C_TBT_X_SCL	D2	I2C_SCL1	
29 OUT	I2C_TBT_XA_INT_L	C1	I2C_IRQ1*	
29 BI	I2C_UPC_X_SDA2	A5	I2C_SDA2	
29 BI	I2C_UPC_X_SCL2	B5	I2C_SCL2	
51 OUT	UPC_I2C_INT_L	B6	I2C_IRQ2*	
29 OUT	GND	A3	SPI_CLK	
29 OUT	GND	B4	SPI_MOSI	
29 IN	GND	A4	SPI_MISO	
29 OUT	GND	B3	SPI_SSZ	
	TP_UPC_XA_SWD_DATA	F4	SWD_DATA	
	TP_UPC_XA_SWD_CLK	G4	SWD_CLK	
31 30 29 IN	UPC_XA_UART_RX	F2	UART_RX	
31 29 OUT	UPC_XA_UART_TX	E2	UART_TX	
29	TBT_XA_LSTX	L4	LSX_R2P	
29	TBT_XA_LSRX	K4	LSX_P2R	
29	USB_UPC_XA_P	L5	USB_RP_P	
29	USB_UPC_XA_N	K5	USB_RP_N	
27 BI	USBC_XA_AUXLSX1	J1	AUX_P	
27 BI	USBC_XA_AUXLSX2	J2	AUX_N	
29 BI	UPC_XA_DBG1	L2	DEBUG1	
29 BI	UPC_XA_DBG2	K2	DEBUG2	
29 BI	SOC_DFU_STATUS	L3	DEBUG3	
29 BI	SOC_FORCE_DFU	K3	DEBUG4	

DIGITAL CORE I/O AND CONTROL
HV FET/SENSE
TYPE-C
PORT MUX

CRITICAL
OMIT_TABLE

SS H7 UPC_XA_SS
SENSEP B10
SENSEN A10
HV_GATE1 B9
HV_GATE2 A9

C3109 0.47UF 10% 6.3V CERM-X5R 0201

C_CC1 L9 USBC_XA_CC1 BI 29 33
C_CC2 L10 USBC_XA_CC2 BI 29 33
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

RPD_G1 K9 USBC_XA_CC1 BI 29
RPD_G2 K10 USBC_XA_CC2 BI 29

C3114 220PF 10% 16V CER-X7R 0201
C3113 220PF 10% 16V CER-X7R 0201

C_USB_TP K6 USBC_XA_USB_TOP_P BI 29
C_USB_TN L6 USBC_XA_USB_TOP_N BI 29
C_USB_BP K7 NC_USBC_XA_USB_BOTP BI 29
C_USB_BN L7 NC_USBC_XA_USB_BOTN BI 29
C_SBU1 K8 USBC_XA_SBU1 BI 32 120
C_SBU2 L8 USBC_XA_SBU2 BI 32 120

GROUND
NC L11
NC or GND to dissipate heat

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

1M R3105 5% 1/20W MF 201 UPC_XA_UART_RX 29 30 31

CRITICAL
R3103 15K 0.1% 1/20W TF-LF 0201

TO SMC

A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7 GND

GND 29

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

SYNC_MASTER=ZIFENG SYNC_DATE=05/26/2017

PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
REVISION 4.0.0
BRANCH evt-0
PAGE 31 OF 200
SHEET 30 OF 131

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

PULL R3209 AND R3208 UP TO ACEs LDOs FOR 1ST BRIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

PP3V3_UPC_XB_LDO
1M R3209 I2C_UPC_XB_DBG_CTL_SCL
1M R3208 I2C_UPC_XB_DBG_CTL_SDA

1M R3212 UPC_XB_GPIO1
1M R3205 UPC_XA_UART_TX

CRITICAL
Q3200
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

PP20V_USBC_XB_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V

PP20V_USBC_XB_VBUS
C3201 1UF 10% 16V X5R 0402

PP1V8_SLPS2R
C3219 1.0UF 20% 6.3V X6S 0201-1

PP3V3_G3H_RTC_X
R3269 100K 5% 1/20W MF 201
PHV_INT_XB_G3H

PP5V_S4_X_USBC
CAP FOR PP_5V0 ON VR PAGE
C3200 10UF 20% 6.3V CERM-X5R 0402-1

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

CRITICAL
R3203 15K 0.1% 1/20W TF-LF 0201
NEED 0.1%

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

L3200
90-OHM-0.1A
EXCX4CE

USB2_UPC_XB_P
USB2_UPC_XB_N
PLACE_NEAR=U3200.L5:5mm
PLACE_NEAR=U3200.K5:5mm

U3200
CD3215A
BGA
CRITICAL
OMIT_TABLE

TBT_POC_RESET	E11	MRESET
USBC_X_RESET_L	F11	RESET*
UPC_XB_GPIO0	B2	GPIO0
UPC_XB_GPIO1	C2	GPIO1
TBT_X_CIO_PWR_EN	D10	GPIO2
TBT_X_USB_PWR_EN	G11	GPIO3
DP_XB_HPD	C10	GPIO4
UPC_PMU_RESET	E10	GPIO5
UPC_X_5V_EN	G10	GPIO6
SOC_DOCK_CONNECT	D7	GPIO7
UPC_XB_FAULT_L	H6	GPIO8
GND	F10	BUSPOWERZ
NC_UPC_XB_I2C_ADDR	F1	I2C_ADDR
UPC_XB_R_OSC	G2	R_OSC
I2C_UPC_XB_DBG_CTL_SCL	E4	DEBUG_CTL1
I2C_UPC_XB_DBG_CTL_SDA	D5	DEBUG_CTL2
I2C_TBT_X_SDA	D1	I2C_SDA1
I2C_TBT_X_SCL	D2	I2C_SCL1
I2C_TBT_XB_INT_L	C1	I2C_IRQ1*
I2C_UPC_X_SDA2	A5	I2C_SDA2
I2C_UPC_X_SCL2	B5	I2C_SCL2
UPC_I2C_INT_L	B6	I2C_IRQ2*
UPC_XB_SPI_CLK	A3	SPI_CLK
UPC_XB_SPI_MOSI	B4	SPI_MOSI
UPC_XB_SPI_MISO	A4	SPI_MISO
UPC_XB_SPI_CS_L	B3	SPI_SSZ
TP_UPC_XB_SWD_DATA	F4	SWD_DATA
TP_UPC_XB_SWD_CLK	G4	SWD_CLK
UPC_XA_UART_TX	F2	UART_RX
UPC_XA_UART_RX	E2	UART_TX
TBT_XB_LSTX	L4	LSX_R2P
TBT_XB_LSRX	K4	LSX_P2R
USB_UPC_XB_F_P	L5	USB_RP_P
USB_UPC_XB_F_N	K5	USB_RP_N
USBC_XB_AUXLSX1	J1	AUX_P
USBC_XB_AUXLSX2	J2	AUX_N
PCH_UART_DEBUG_R2D	L2	DEBUG1
PCH_UART_DEBUG_D2R	K2	DEBUG2
UPC_XB_DBG3	L3	DEBUG3
UPC_XB_DBG4	K3	DEBUG4

PP_5V0 A11 B11 C11 D11
PP_HV A6 A7 A8 B7
PP_CABLE H10
VBUS H11 J10 J11 K11
VIN_3V3 H1
VDDIO B1
LDO_3V3 G1 H2
VOUT_3V3 K1 A2
LDO_1V8A E1
LDO_1V8D
LDO_BMC

HV FETSENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX

SS H7 UPC_XB_SS
SENSEP B10
SENSEN A10
HV_GATE1 B9
HV_GATE2 A9
C3209 0.47UF 10% 6.3V CERM-X5R 0201

C_CC1 L9 USBC_XB_CC1
C_CC2 L10 USBC_XB_CC2
RPD_G1 K9 USBC_XB_CC1
RPD_G2 K10 USBC_XB_CC2
C_USB_TP K6 USBC_XB_USB_TOP_P
C_USB_TN L6 USBC_XB_USB_TOP_N
C_USB_BP K7 USBC_XB_USB_BOT_P
C_USB_BN L7 USBC_XB_USB_BOT_N
C_SBU1 K8 USBC_XB_SBU1
C_SBU2 L8 USBC_XB_SBU2
C3214 220PF 10% 16V CER-X7R 0201
C3213 220PF 10% 16V CER-X7R 0201

GROUND
NC L11
NC or GND to dissipate heat

GND A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7
GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

NC

UPC_XB_GATE1
TP_Q3200_DRAIN
UPC_XB_GATE2

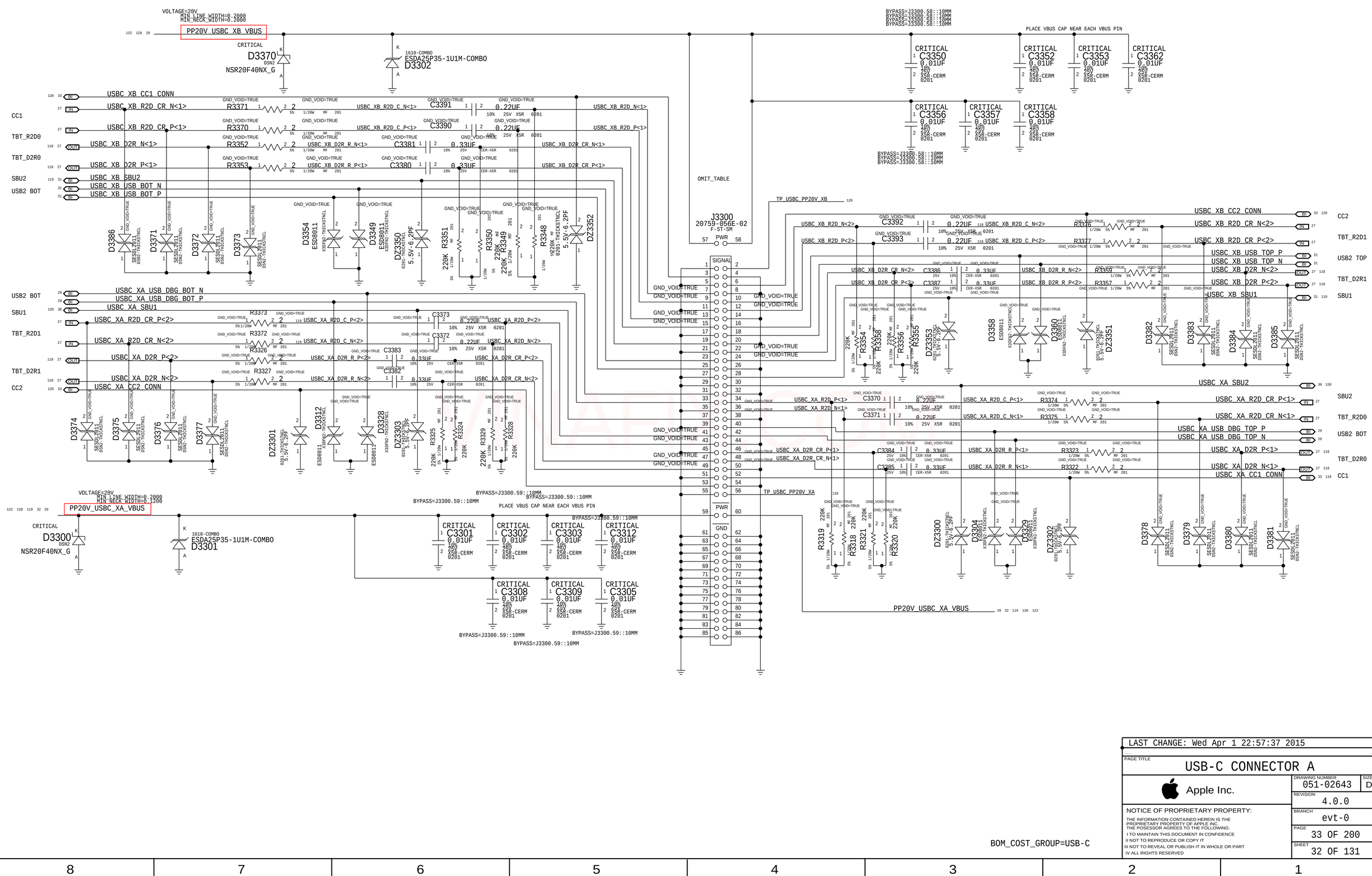
PPDCIN_G3H
MAX 100uF TOTAL ON RAIL

PP3V3_UPC_XB_LDO
PP3V3_TBT_X_SX
PP1V8_UPC_XB_LDOA
PP1V8_UPC_XB_LDOD
PP1V1_UPC_XB_LDO_BMC

C3204 2.2UF 20% 10V X5R-CERM 0201
C3205 1.0UF 20% 6.3V X6S 0201-1
C3206 0.47UF 10% 6.3V CERM-X5R 0201
C3208 10UF 20% 6.3V CERM-X5R 0402-1

BOM_COST_GROUP=USB-C

SYNC_MASTER=ZIFENG	SYNC_DATE=05/26/2017
PAGE TITLE	USB-C PORT CONTROLLER B
Apple Inc.	DRAWING NUMBER 051-02643 SIZE D
	REVISION 4.0.0
	BRANCH evt-0
	PAGE 32 OF 200
	SHEET 31 OF 131



LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE

USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER 051-02643 | SIZE D

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BRANCH evt-0

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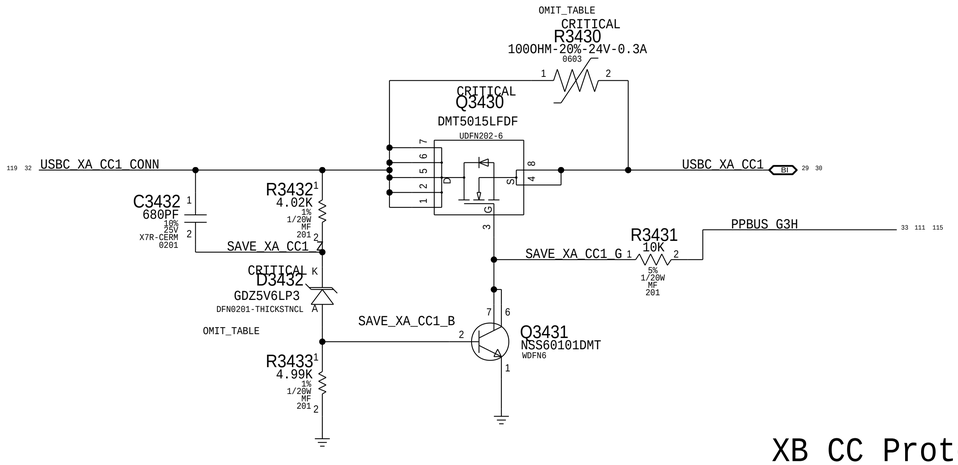
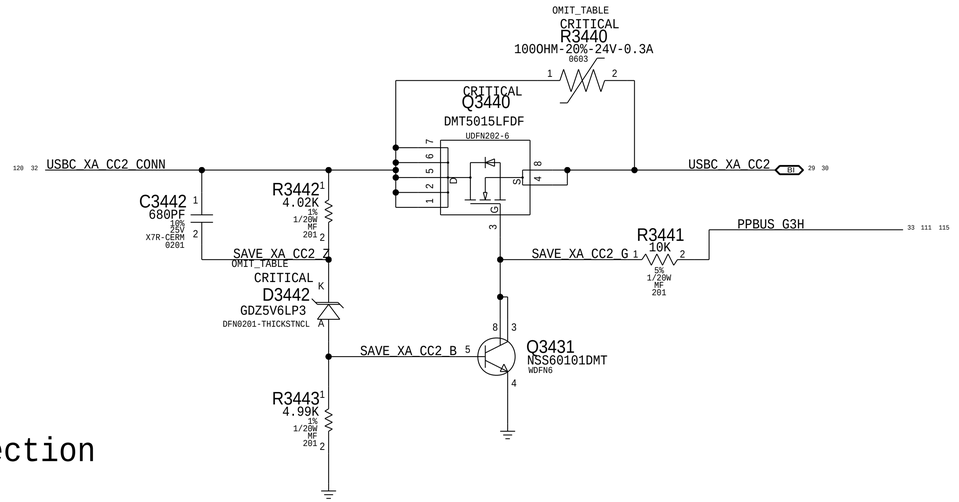
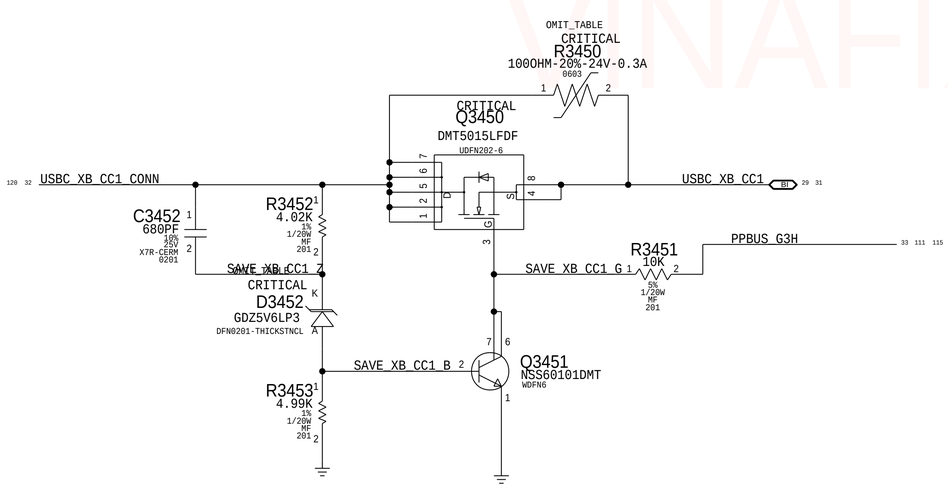
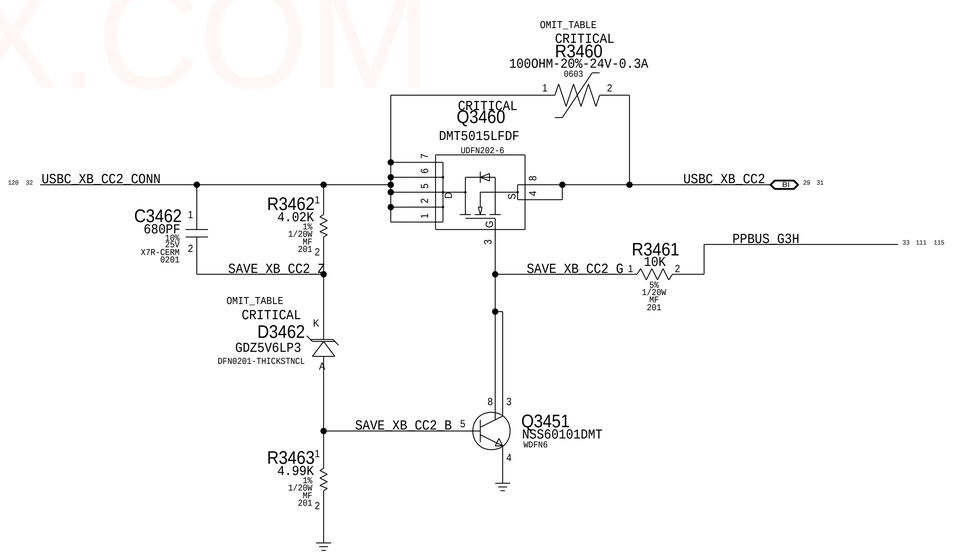
XA CC Protection





XB CC Protection





PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
371S00181	4	DIODE,ZENER,5.6V,250MW,DFN0201	D3432,D3442,D3452,D3462	CRITICAL	
740S00050	4	FUSE,THRMSTR,PTC,470OHM,24V,60MA,0603	R3430,R3440,R3450,R3460	CRITICAL	

BOM_COST_GROUP=USB-C

DESIGN: X1032/MLB_P4BP
LAST CHANGE: Fri Jan 6 16:01:21 2017

PAGE TITLE
USBC X Connector Support

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
REVISION 4.0.0
BRANCH evt-0
PAGE 34 OF 200
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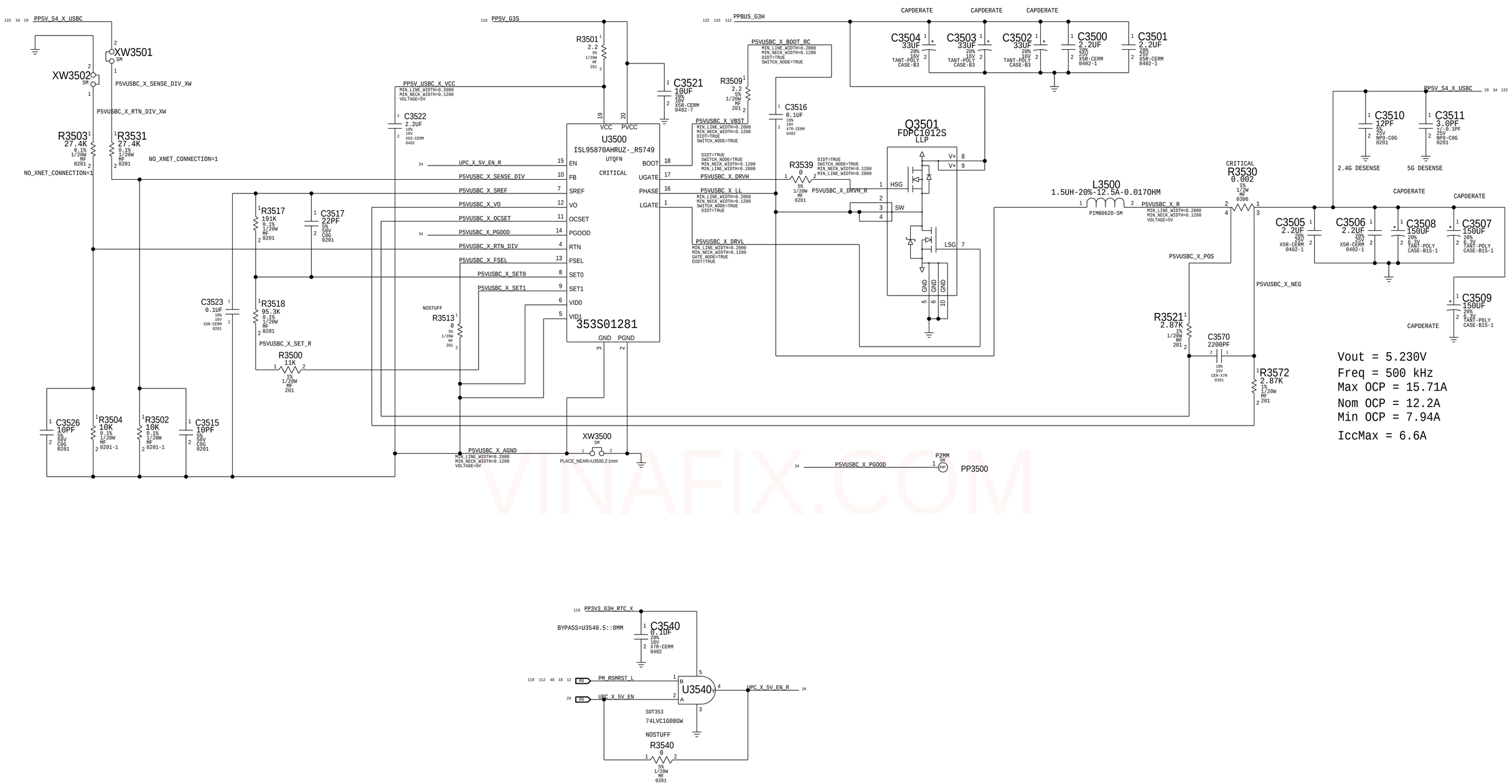

PAGE TITLE: TBT 5V REGULATOR

Apple Inc.

DRAWING NUMBER: 051-02643 | SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
PAGE: 35 OF 200
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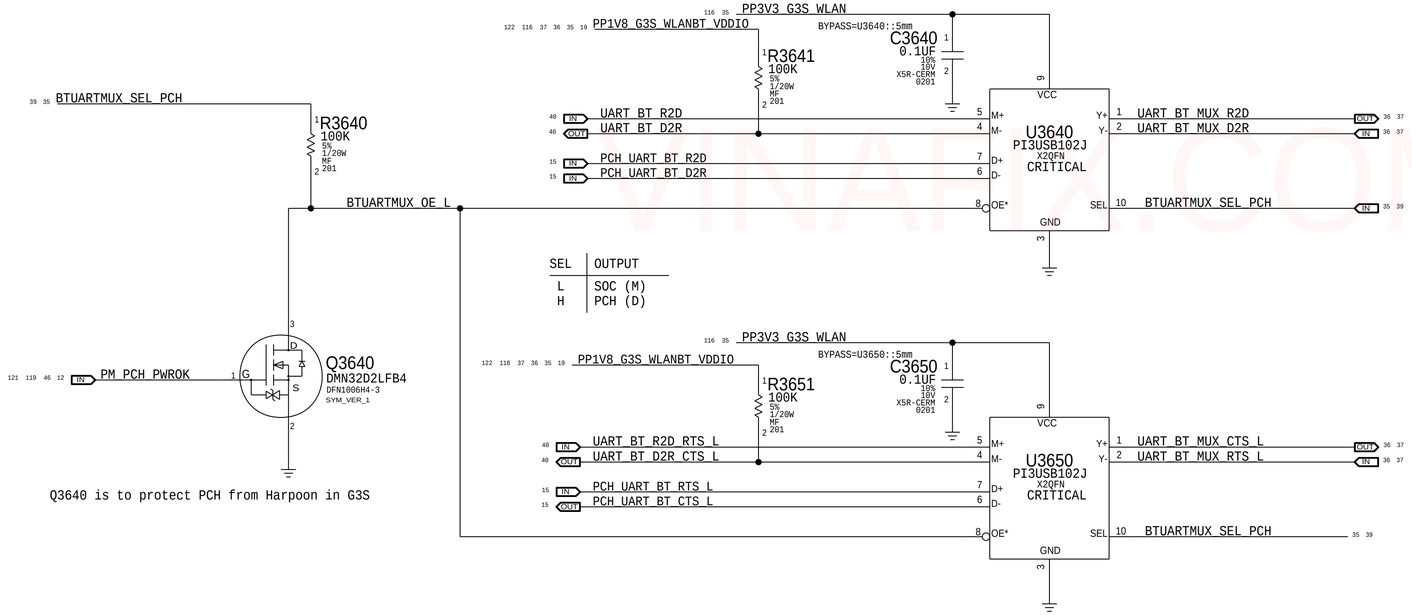

BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J132 SYNC_DATE=03/29/2017

PAGE TITLE

WIFI/BT: Support

Apple Inc.

DRAWING NUMBER 051-02643 SIZE D

REVISION 4.0.0

BRANCH evt-0

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SHEET 35 OF 131

PP3V3_G3S_WLAN

C3725 10UF 20% 6.3V CERM-X5R 0402-4 (PLACE_NEAR=U3730.89:5MM)
C3721 10UF 20% 6.3V CERM-X5R 0402-4 (PLACE_NEAR=U3730.74:5MM)
C3722 10UF 20% 6.3V CERM-X5R 0402-4 (PLACE_NEAR=U3730.42:3MM)
C3724 10UF 20% 6.3V CERM-X5R 0402-4 (PLACE_NEAR=U3730.63:5MM)

PP1V8_G3S_WLANBT_VDDIO
C3723 0.1UF 10% 6.3V CERM-X5R 0201 (PLACE_NEAR=U3730.3:1MM)

U3730
LBEE5ZZ1HP-049
LGA
SYM 1 OF 3
CRITICAL
OMIT_TABLE

VDDBAT_HP, VDDBAT_LP, VDD3P3_BT, VDD3P3_PAD, VDD3P3_FEM_CORE0, VDD3P3_FEM_CORE1, VDD3P3_FEM_CORE2, VDDIO_RFSW, VDDIO_PMU, VDD3P3_SDKOTP, VDDIO_DIG

50_G_0_MATCH	91	2G_ANT_CORE0
50_A_0_MATCH	87	5G_ANT_CORE0
50_G_1_MATCH	76	2G_ANT_CORE1
50_A_1_MATCH	72	5G_ANT_CORE1
50_G_2_MATCH	49	2G_ANT_CORE2
50_A_2_MATCH	65	5G_ANT_CORE2
NC	44	BT_ONLY_ANT
WLAN_JTAG_SEL	1	WL_JTAG_SEL
WLAN_JTAG_TCK	81	WL_JTAG_TCK
WLAN_JTAG_TDI	82	WL_JTAG_TDI
WLAN_JTAG_TMS	83	WL_JTAG_TMS
WLAN_JTAG_TRST_L	84	WL_JTAG_TRST
WLAN_JTAG_TDO	85	WL_JTAG_TDO
UART_WLAN_R2D	93	WL_UART_RX
UART_WLAN_D2R	94	WL_UART_TX
UART_WLAN_D2R_CTS_L	95	WL_UART_RTS
UART_WLAN_R2D_RTS_L	96	WL_UART_CTS
SPROM_DOUT	67	WL_SPROM_MO
SPROM_DIN	68	WL_SPROM_MI
SPROM_CLK	69	WL_SPROM_CLK
SPROM_CS	70	WL_SPROM_CS
WL_GPIO_13	97	WL_GPIO_13
WLAN_CONTEXT_B	100	WL_GPIO_21
WLAN_AUDIO_SYNC	99	WL_GPIO_20
WLAN_SROM_STRAP	98	WL_GPIO_17
TP_WLAN_PMU_TEST	159	WL_PMU_TEST_O
NC_WLAN_GPIO_14	161	WL_GPIO_14
WLAN_CONTEXT_A	163	WL_GPIO_12
WLAN_HOST_WAKE	78	WL_HOST_WAKE
PCH_WLAN_DEV_WAKE	79	WL_DEV_WAKE

R3700 10K 5% 1/20W MF 201 (PP1V8_G3S_WLANBT_VDDIO)
R3791 100K 5% 1/20W MF 201
R3790 100K 5% 1/20W MF 201
PP3700 P2MM SMD
TP3701 A TP-P5
TP3700 A TP-P5 (NO_TEST=1)

PCIE_REFCLK_P	6	PCH_PCIE_CLK100M_WLAN_P
PCIE_REFCLK_N	5	PCH_PCIE_CLK100M_WLAN_N
PCIE_TX_P	9	PCH_PCIE_WLAN_D2R_C_P
PCIE_TX_N	8	PCH_PCIE_WLAN_D2R_C_N
PCIE_RX_P	12	PCH_PCIE_WLAN_R2D_P
PCIE_RX_N	11	PCH_PCIE_WLAN_R2D_N
PCIE_CLKREQ*	14	PCH_WLAN_CLKREQ_R_L
PCIE_WAKE*	15	AP_PCIE_WAKE_L
PERST*	16	PCH_WLAN_PERST_L
BT_UART_RX	54	UART_BT_MUX_R2D
BT_UART_TX	55	UART_BT_MUX_D2R
BT_UART_CTS	56	UART_BT_MUX_CTS_L
BT_UART_RTS	57	UART_BT_MUX_RTS_L
BT_GPIO_2/BT_SF_STRAP	53	BT_ROM_BOOT_HPN_L
BT_JTAG_STRAP	60	TP_BT_JTAG_STRAP
BT_SF_CS	36	BT_SPI2_CSN
BT_SF_CLK	37	BT_SPI2_CLK
BT_SF_MISO	38	BT_SPI2_MISO
BT_SF_MOSI	39	BT_SPI2_MOSI
BT_I2S_WS	40	UART_BT_LH_R2D
BT_I2S_DO	41	NC
BT_I2S_CLK	123	UART_BT_LH_D2R
BT_I2S_DI	124	NC
BT_GPIO_3	59	BT_GPIO_3
BT_GPIO_4	58	BT_GPIO_4
BT_DEV_WAKE	61	HRN_BT_DEV_WAKE
BT_HOST_WAKE	62	BT_HOST_WAKE

C3707 C3706 C3709 C3708 0.1UF 10% 6.3V X7R 0201 (GND_VOID=TRUE)
PCH_PCIE_WLAN_D2R_P, PCH_PCIE_WLAN_D2R_N, PCH_PCIE_WLAN_R2D_C_P, PCH_PCIE_WLAN_R2D_C_N
PP1V8_G3S_WLANBT_VDDIO, PP1V8_S5
R3715 10K 5% 1/20W MF 201 (PCH) PCH_BT_ROM_BOOT_L
R3713 NOSTUFF 10K 5% 1/20W MF 201
R3717 0 0201MF 1/20W 5% (PCH) PCH_BT_ROM_BOOT_L
R3716 NOSTUFF 0 0201MF 1/20W 5% (SOC) BT_ROM_BOOT_L
R3750 100K 5% 1/20W MF 201 (PP1V8_G3S_WLANBT_VDDIO)
UART_BT_LH_R2D (MAKE_BASE=TRUE), UART_BT_LH_D2R (MAKE_BASE=TRUE)
R3718 NOSTUFF 0 0201MF 1/20W 5% PCH_BT_DEV_WAKE
R3719 0 0201MF 1/20W 5% BT_DEV_WAKE

WL_REG_ON, BT_REG_ON, VDD1P5_1X1, SR1P4_VLX, SR1P8_VLX, VIN_RFLDO, SR1P2_VLX, VDD1P2_3X3, CLK32K

WLAN_PWR_EN	19	WL_REG_ON
BT_PWR_EN	20	BT_REG_ON
PP1V5_WLANBT	21	VDD1P5_1X1
P1V5_WLANBT_VLX	22	SR1P4_VLX
PVIN_RFLDO_WLANBT_VLX	23	SR1P8_VLX
PPVIN_RFLDO_WLANBT	24	VIN_RFLDO
P1V2_WLANBT_VLX	25	SR1P2_VLX
PP1V2_WLANBT	32	VDD1P2_3X3
PMU_CLK32K_WLANBT	33	CLK32K

L3701 2.2UH-1.2A 0806 (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.5V) (PLACE_NEAR=U3730.23:10MM, PLACE_NEAR=L3701.2:10MM)
P1V5_WLANBT_VLX → PP1V5_WLANBT_C, DIDT=TRUE, SWITCH_NODE=TRUE
C3701 7.5UF 20% 4V 0402-THICKSTNCL → PP1V5_WLANBT

L3702 1UH-20%-4.1A-0.048OHM 2520-1 (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.2V) (PLACE_NEAR=U3730.25:10MM, PLACE_NEAR=L3702.2:10MM)
P1V2_WLANBT_VLX → PP1V2_WLANBT_C, DIDT=TRUE, SWITCH_NODE=TRUE
C3702 7.5UF 20% 4V 0402-THICKSTNCL → PP1V2_WLANBT

L3703 2.2UH-1.2A 0806 (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=1.8V) (PLACE_NEAR=U3730.24:5MM, PLACE_NEAR=L3703.1:5MM)
PVIN_RFLDO_WLANBT_VLX → PPVIN_RFLDO_WLANBT_C, DIDT=TRUE, SWITCH_NODE=TRUE
C3703 7.5UF 20% 4V 0402-THICKSTNCL → PPVIN_RFLDO_WLANBT

PMU_CLK32K_WLANBT (IN) = PMU_CLK32K_WLANBT (MAKE_BASE=TRUE)

BLUETOOTH SERIAL FLASH

PP1V8_G3S_WLANBT_VDDIO
R3751 100K 5% 1/20W MF 201
R3752 100K 5% 1/20W MF 201
R3753 100K 5% 1/20W MF 201
R3754 1K 5% 1/20W MF 201
C3710 0.1UF 10% 6.3V CERM-X5R 0201 (PLACE_NEAR=U3750.8:2MM)
C3712 10UF 20% 6.3V CERM-X5R 0402-4 (PLACE_NEAR=U3750.8:4MM)
U3750 2MBIT USON (OMIT_TABLE) MX25L2006EZUI-12G
BT_SPI2_CLK, BT_SPI2_CSN, BT_SPI2_MOSI, BT_SPI2_MISO, BT_SFLASH_CS_L, BT_SFLASH_WP_L, BT_SFLASH_HOLD_L

BOOT_STRAPS

WLAN_SROM_STRAP
R3705 10K 5% 1/20W MF 201

WLAN_SROM_STRAP:
LOW: SROM Enabled
HIGH: SROM Disabled

WLAN SERIAL EEPROM

PP3V3_G3S_WLAN (PLACE_NEAR=U3710.8:2MM)
C3711 0.1UF 10% 6.3V CERM-X5R 0201
R3701 10K 5% 1/20W MF 201
U3710 CAS93C86B UDFN8 (OMIT_TABLE) GND_EPAD
SPROM_DOUT, SPROM_CS, SPROM_CLK, SPROM_DIN, WIFI_SROM_ORG
R3712 10K 5% 1/20W MF 201

BOM_COST_GROUP=WIRELESS

PAGE TITLE: WIFI/BT: MODULE 1
Apple Inc.
DRAWING NUMBER: 051-02643 SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
PAGE: 37 OF 200
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S00196	2	FILTER,DIPLEXER,LB/HB,LGA6	U3810,U3830	CRITICAL	RF_TUNING

U3730 LBEE5ZZ1HP-049 LGA SYM 2 OF 3

CRITICAL

OMIT_TABLE

GND: 4, 7, 10, 13, 27, 31, 43, 45, 46, 47, 48, 50, 51, 64, 66, 71, 73, 75, 77, 80, 86, 88, 90, 92

THRM_PAD: 101, 102, 103, 104, 105, 106, 107, 108, 109, 110, 111, 112, 113, 114, 115, 116, 117, 118, 119, 120, 121, 122, 125, 126, 127, 128, 129, 130, 131, 132, 133, 134, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144, 145, 146, 147, 148, 149, 150, 151, 152, 153

U3730 LBEE5ZZ1HP-049 LGA SYM 3 OF 3

CRITICAL

OMIT_TABLE

THRM_PAD: 154, 155, 156, 157, 158, 160, 162, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179, 180, 181, 182, 183, 184, 185, 186, 187, 188, 189, 190, 191, 192, 193, 194, 195, 196, 197, 198, 199, 200, 201, 202, 203, 204, 205, 206, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229, 230, 231, 232

THRM_PAD: 233, 234, 235, 236, 237, 238, 239, 240, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 257, 258, 259, 260, 261, 262, 263, 264, 265, 266, 267, 268, 269, 270, 271, 272, 273, 274, 275, 276, 277, 278, 279, 280, 281, 282, 283, 284, 285, 286, 287, 288, 289, 290, 291, 292, 293, 294, 295, 296, 297, 298, 299, 300, 301, 302, 303, 304, 305, 306, 307, 308

THRM_PAD: 309, 310, 311, 312, 313, 314, 315, 316, 317, 318, 319, 320, 321, 322, 323, 324, 325, 326, 327, 328, 329, 330, 331, 332, 333, 335, 336, 337, 338, 339, 340, 341, 342, 343, 344, 345, 346, 347, 348, 349, 350, 351, 352, 353, 354, 355, 356, 357, 358, 359, 360, 361, 362, 363, 364, 365, 366, 367, 368, 369, 370, 371, 372, 373, 375, 376, 377, 378, 379, 380, 381, 382, 383, 384, 385

DEBUG CONNECTOR

WIFI_DBG
J3801
AA25D-S038VA1
F-ST-SM

36 13	PCH_WLAN_DEV_WAKE	1	2	HRN_BT_DEV_WAKE
39 36	WLAN_HOST_WAKE	3	4	BT_HOST_WAKE
77 36	WLAN_PWR_EN	5	6	BT_PWR_EN
40 36	UART_WLAN_D2R	7	8	UART_BT_MUX_D2R
40 36	UART_WLAN_R2D	9	10	UART_BT_MUX_R2D
40 36	UART_WLAN_R2D_RTS_L	11	12	UART_BT_MUX_CTS_L
40 36	UART_WLAN_D2R_CTS_L	13	14	UART_BT_MUX_RTS_L
37 36	WLAN_JTAG_TCK	15	16	BT_SPI2_CLK_R
37 36	WLAN_JTAG_TMS	17	18	BT_SPI2_CSN_R
37 36	WLAN_JTAG_TDI	19	20	BT_SPI2_MISO_R
121 36	WLAN_JTAG_TDO	21	22	BT_SPI2_MOSI_R
121 36	WLAN_JTAG_TRST_L	23	24	BT_GPIO_3
121 36	WLAN_JTAG_SEL	25	26	BT_GPIO_4
		27	28	
		29	30	
19 12	PCH_WLAN_CLKREQ_L	31	32	PMU_CLK32K_WLANBT
36 20 13	PCH_WLAN_PERST_L	33	34	
36 19	AP_PCIE_WAKE_L	35	36	PP1V8_G3S_WLANBT_VDDIO
122 116 36	PP3V3_G3S_WLAN	37	38	
		41	42	

R3880 0 1 2 PLACE_NEAR=U3730.37:20MM WIFI_DBG 5% 1/20W MF 0201 BT_SPI2_CLK (IN 36)
R3881 0 1 2 PLACE_NEAR=U3730.36:20MM WIFI_DBG 5% 1/20W MF 0201 BT_SPI2_CSN (IN 36)
R3882 0 1 2 PLACE_NEAR=U3730.35:20MM WIFI_DBG 5% 1/20W MF 0201 BT_SPI2_MISO (IN 35)
R3883 0 1 2 PLACE_NEAR=U3730.39:20MM WIFI_DBG 5% 1/20W MF 0201 BT_SPI2_MOSI (OUT 36)

37 36 WLAN_JTAG_TCK MAKE_BASE=TRUE — WLAN_JTAG_TCK 39 121
37 36 WLAN_JTAG_TMS MAKE_BASE=TRUE — WLAN_JTAG_TMS 39 121
37 36 WLAN_JTAG_TDI MAKE_BASE=TRUE — WLAN_JTAG_TDI 40 121

ACCELERATION SENSOR

PLACE_NEAR=U3840.8:2MM
PLACE_NEAR=U3840.8:2MM

L3841
240-OHM-25%-0.42A-0.31DCR
0201

VOLTAGE=1.8V PP1V8_ACCEL_FILT — PP1V8_G3S 37 116 119

C3842 0.22UF 20% 10V 0201
C3841 0.22UF 20% 10V 0201

U3840
BMA282
LGA

VDD VDDIO

37 SPI_ACCEL_CS_L — CS*
SCX 1 SPI_AOP_SENSOR_CLK 37 47
SDX 2 SPI_AOP_SENSOR_MOSI 37 47
SDO 3 SPI_AOP_SENSOR_MISO_R 37 47
37 ACCEL_INT1 — 6 INT1
37 ACCEL_INT2 — 5 INT2
PS 13
GND GNDIO 9 11 12 14 10

37 SPI_ACCEL_CS_L MAKE_BASE=TRUE — SPI_ACCEL_CS_L 39
37 ACCEL_INT1 MAKE_BASE=TRUE — ACCEL_INT1 39
37 ACCEL_INT2 MAKE_BASE=TRUE — ACCEL_INT2 39

PP1V8_G3S 119 116 37

R3870 100K 1 2 5% 1/20W MF 201 SPI_ACCEL_CS_L 37
R3871 100K 1 2 5% 1/20W MF 201 SPI_AOP_SENSOR_MISO_R 37 47
R3872 100K 1 2 5% 1/20W MF 201 SPI_AOP_SENSOR_MOSI 37 47
R3873 100K 1 2 5% 1/20W MF 201 SPI_AOP_SENSOR_CLK 37 47

CORE0 DIPLEXER AND MATCHING NETWORK

RF_TUNING

CRITICAL J3810 20449-001E-03 F-ST-SM 118

50_0_ANT 1 — NO STUFF C3817 0.2PF +/-0.05PF 25V COG-CERM 0201

CRITICAL L3810 1.2NH-+/-0.05NH-1.1A-0.040HM 0201 RF_TUNING

50_0_COM — CRITICAL C3816 0.2PF +/-0.05PF 25V COG-CERM 0201 RF_TUNING

U3810 DPX205950DT-9063B2SJ 0805 CRITICAL
COM 2, HI 4, LO 6, GND 5 3 1
OMIT_TABLE

50_0_DIPLEXER 118 — CRITICAL L3814 2.7NH+/-0.1NH-0.6A 0201 RF_TUNING — 50_A_0_MATCH 36 118

NO STUFF C3815 0.2PF +/-0.05PF 25V COG-CERM 0201

NO STUFF C3813 0.2PF +/-0.05PF 25V COG-CERM 0201

50_G_0_DIPLEXER 118 — CRITICAL L3811 1.0NH-+/-0.05NH-1.1A-0.040HM 0201 RF_TUNING — 50_G_0_MATCH 36 118

NO STUFF C3812 0.2PF +/-0.05PF 25V COG-CERM 0201

CRITICAL L3812 5.1NH-3%-0.4A 0201

CORE1 DIPLEXER AND MATCHING NETWORK

RF_TUNING

CRITICAL J3820 20449-001E-03 F-ST-SM 118

50_1_ANT 1 — NO STUFF C3827 0.2PF +/-0.05PF 25V COG-CERM 0201

CRITICAL L3820 1.2NH-+/-0.05NH-1.1A-0.040HM 0201 RF_TUNING

50_1_COM — CRITICAL C3826 0.2PF +/-0.05PF 25V COG-CERM 0201 RF_TUNING

U3820 DPX205950DT-9163C1SJ 0805 CRITICAL
COM 2, HI 6, LO 4, GND 5 3 1
RF_TUNING

50_A_1_DIPLEXER 118 — CRITICAL L3824 2.7NH+/-0.1NH-0.6A 0201 RF_TUNING — 50_A_1_MATCH 36 118

NO STUFF C3825 0.2PF +/-0.05PF 25V COG-CERM 0201

NO STUFF C3823 0.2PF +/-0.05PF 25V COG-CERM 0201

50_G_1_DIPLEXER 118 — CRITICAL L3821 1.2NH-+/-0.05NH-1.1A-0.040HM 0201 RF_TUNING — 50_G_1_MATCH 36 118

NO STUFF C3822 0.2PF +/-0.05PF 25V COG-CERM 0201

CRITICAL L3822 5.1NH-3%-0.4A 0201

CORE2/Aux DIPLEXER AND MATCHING NETWORK

RF_TUNING

CRITICAL J3830 20449-001E-03 F-ST-SM

50_2_ANT 1 — NO STUFF C3837 0.2PF +/-0.05PF 25V COG-CERM 0201

CRITICAL L3830 1.2NH-+/-0.05NH-1.1A-0.040HM 0201 RF_TUNING

50_2_COM — CRITICAL C3836 0.2PF +/-0.05PF 25V COG-CERM 0201 RF_TUNING

U3830 DPX205950DT-9063B2SJ 0805 CRITICAL
COM 2, HI 4, LO 6, GND 5 3 1
OMIT_TABLE

50_G_2_DIPLEXER 118 — CRITICAL L3834 2.9NH+/-0.1NH-0.6A 0201 RF_TUNING — 50_G_2_MATCH 36 118

C3835 0.2PF +/-0.05PF 25V COG-CERM 0201 NO STUFF

NO STUFF C3833 0.2PF +/-0.05PF 25V COG-CERM 0201

50_A_2_DIPLEXER 118 — CRITICAL L3831 1.2NH-+/-0.05NH-1.1A-0.040HM 0201 RF_TUNING — 50_A_2_MATCH 36 118

NO STUFF C3832 0.2PF +/-0.05PF 25V COG-CERM 0201

CRITICAL L3832 5.1NH-3%-0.4A 0201

BOM_COST_GROUP=WIRELESS

SYNC_MASTER=PETE SYNC_DATE=08/11/2017

PAGE TITLE: AP & BT Conn

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D
REVISION: 4.0.0
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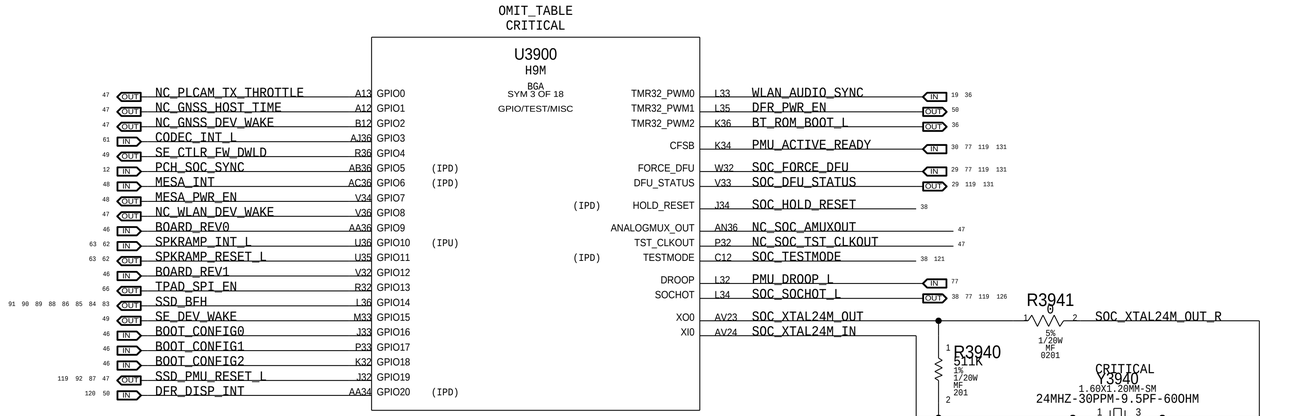
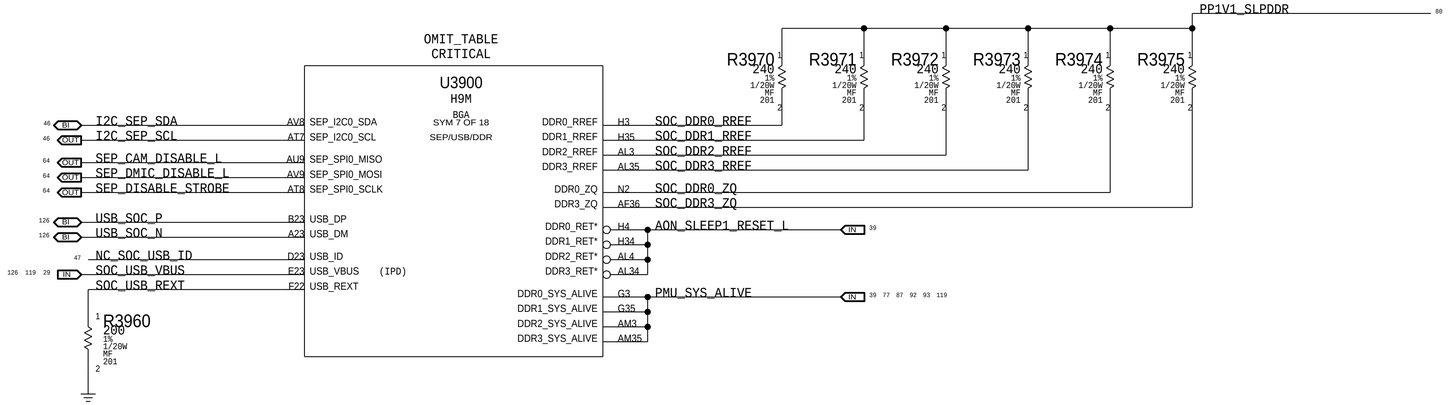
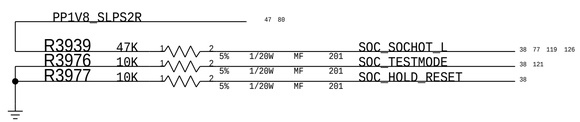
Note 1) IPU represents SW configured state, not HW default







BOM_COST_GROUP=SOC

SYNC_MASTER=SILU SYNC_DATE=05/26/2017

PAGE TITLE

SoC GPIO/SEP/USB/DDR/Test

Apple Inc.

DRAWING NUMBER 051-02643 SIZE D

REVISION 4.0.0

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36	OUT	WLAN_CONTEXT_A	D3	AOP_FUNC[0]		AOP_PDM_CLK0	P6	PDM_DMIC_CLK0_R
36	OUT	WLAN_CONTEXT_B	F4	AOP_FUNC[1]		AOP_PDM_CLK1	K2	PDM_DMIC_CLK1_R
37	IN	ACCEL_INT1	M6	AOP_FUNC[2]	(IPD)	AOP_PDM_CLK2	J6	SMC_FIXTURE_MODE_L
37	IN	ACCEL_INT2	D4	AOP_FUNC[3]	(IPD)	AOP_PDM_CLK3	L6	NC_PLCAM_PROX_INT_L
35	OUT	BTUARTMUX_SEL_PCH	F3	AOP_FUNC[4]		AOP_PDM_CLK4	L5	NC_PLCAM_ROMEO_B2B_DETECT
20 15	IN	SOC_PERST_L	K6	AOP_FUNC[5]				
47	IN	NC_ALTIMETER_INT	E4	AOP_FUNC[6]	(IPD)	AOP_PDM_DATA0	J5	PDM_DMIC_DATA0
37	OUT	SPI_ACCEL_CS_L	J3	AOP_FUNC[7]		AOP_PDM_DATA1	K4	PDM_DMIC_DATA1
47	OUT	NC_SPI_ALTIMETER_CS_L	H6	AOP_FUNC[8]				
						AOP_SPI_MOSI	D2	SPI_AOP_SENSOR_MOSI_R
47	OUT	NC_I2C_AOP_SCL	N6	AOP_I2C0_SCL		AOP_SPI_SCLK	F2	SPI_AOP_SENSOR_CLK_R
47	BI	NC_I2C_AOP_SDA	G5	AOP_I2C0_SDA		AOP_SPI_MISO	E2	SPI_AOP_SENSOR_MISO

OMIT_TABLE
CRITICAL

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120 50	IN	DFR_TOUCH_INT_L	AL6	AON_GPIO0		JTAG_TCK	AK6	SWD_SOC_SWCLK
46	IN	CPU_SMC_THRMTRIP_L	AE6	AON_GPIO1	(IPU)	JTAG_TMS	AN5	SWD_SOC_SWDIO
117	IN	GFX_SELF_THROTTLE_1V8	AT5	AON_GPIO2	(IPD)	JTAG_TDI	AH6	DEBUG_JTAG_SOC_TDI
47	OUT	SMC_GPU_THRMTRIP	AN4	AON_GPIO3		JTAG_TDO	AP4	DEBUG_JTAG_SOC_TDO
18	IN	XDP_PRESENT_L	AK4	AON_GPIO4		JTAG_TRST*	AJ6	TP_JTAG_SOC_TRST_L
61	OUT	CODEC_RESET_L	AV5	AON_GPIO5		JTAG_SEL	AC6	SOC_JTAG_SEL (DAP=0, TAP=1)
36	OUT	BT_DEV_WAKE	AR3	AON_GPIO6				
47	IN	NC_PCIEDN_WAKE_L	AG6	AON_GPIO7	(IPU)	DOCK_CONNECT	AN2	SOC_DOCK_CONNECT
47	OUT	NC_ENET_LOW_PWR	AU5	AON_GPIO8				
47	IN	TPAD_SPI_INT_L	AP2	AON_GPIO9		AON_SWD0_TMS	AJ4	WLAN_JTAG_TMS
47	IN	NC_SDCONN_STATE_CHANGE_L	AR4	AON_GPIO10	(IPU)	AON_SWD1_TMS	AH4	NC_MESA_MENUKEY_L
47	IN	NC_ENET_MEDIA_SENSE	AN3	AON_GPIO11	(IPD)	AON_SWD01_TCK	AJ2	WLAN_JTAG_TCK
77	IN	PMU_INT_L	AT6	AON_GPIO12	(IPU)			
						WDOG	AJ5	SOC_WDOG
						AON_SLEEP1_RESET*	AF6	AON_SLEEP1_RESET_L

PLACE_NEAR=U3900.AD6:5MM
PLACE_NEAR=U7800.M7:5MM

77 OUT SPMI_CLK — R4036 20 1/20W MF 201 5% — SPMI_CLK_R — AD6 AON_SPMI_SCLK
77 BI SPMI_DATA — R4037 20 1/20W MF 201 5% — SPMI_DATA_R — AR2 AON_SPMI_SDATA

119 77 IN PMU_CLK32K_SOC — AR5 RT_CLK32768

SOC_COLD_RESET_L — AK2 COLD_RESET*
R4039 4.7K 1/20W MF 201 5% — AK3 CFSB_AON

121 119 77 64 IN PMU_COLD_RESET_L

OMIT_TABLE
CRITICAL

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PLACE_NEAR=U3900.U2:5MM
PLACE_NEAR=U3900.V2:5MM
PLACE_NEAR=U3900.U3:5MM
PLACE_NEAR=U3900.V4:5MM

118 39 20 12	BI	ESPI_IO<0> — R4050 20 1/20W MF 201 5%	V2	SMC_ESPI_IO0		SMC_GPIO0	Y4	CODEC_WAKE_L
118 39 20 12	BI	ESPI_IO<1> — R4051 20 1/20W MF 201 5%	U3	SMC_ESPI_IO1		SMC_GPIO1	Y8	BT_HOST_WAKE
118 39 20 12	BI	ESPI_IO<2> — R4052 20 1/20W MF 201 5%	U4	SMC_ESPI_IO2		SMC_GPIO2	Y5	WLAN_HOST_WAKE
118 39 20 12	BI	ESPI_IO<3> — R4053 20 1/20W MF 201 5%	V3	SMC_ESPI_IO3		SMC_GPIO3	AA2	GFX_THROTTLE_1V8_L
20	IN	ESPI_CLK60M	U2	SMC_ESPI_CLK	(IPD)	SMC_GPIO4	Y7	LID_OPEN_RIGHT
39 20 12	IN	ESPI_CS_L	V1	SMC_ESPI_CS*		SMC_GPIO5	Y6	PCC_EVENT
119 20 12	IN	ESPI_RESET_L	V6	SMC_ESPI_RESET*	(IPD)	SMC_GPIO6	AB2	NC_TPAD_VIBE_L
						SMC_GPIO7	AD5	TPAD_KBD_WAKE_L
46	IN	SMC_PECI_RX	M5	SMC_PECI_IN	(IPD)	SMC_GPIO8	AD2	LID_OPEN_LEFT
46	OUT	SMC_PECI_TX	T6	SMC_PECI_OUT		SMC_GPIO9	AB4	NC_SPI_DSCRPTR_OVERRIDE_L
121 46	OUT	SMC_PCH_PWROK	W7	PCH_PWROK		SMC_GPIO10	AC2	DISP_GCON_INT_L
121 46	OUT	SMC_PCH_SYS_PWROK	W8	SYS_PWROK		SMC_GPIO11	AC3	PCH_GCON_INT_L
						SMC_GPIO12	AA8	TPAD_ACTUATOR_DISABLE_L
46	OUT	SMC_RSMRST_L	W6	RSMRST*		SMC_GPIO13	AB3	TBT_WAKE_L
121 119 46	OUT	SMC_SYSRST_L	W4	SYS_RESET*		SMC_GPIO14	AE2	UPC_I2C_INT_L
131 119 77 12	IN	PM_SLP_S0_L	AA4	SLP_S0B		SMC_GPIO15	L4	NC_GNSS_HOST_WAKE
69 47 46	BI	SMC_PROCHOT_L	R5	PROCHOT*				
119 93 92 87 77 38	IN	PMU_SYS_ALIVE	AA6	SYS_ALIVE		SMC_ADC0	AG2	SMC_DCIN_VSENSE
						SMC_ADC1	AC4	SMC_DCIN_ISENSE
119 51	OUT	I2C_UPC_SCL	M3	SMC_I2C0_SCL		SMC_ADC2	AH3	SMC_PBUS_VSENSE
119 51	BI	I2C_UPC_SDA	J4	SMC_I2C0_SDA		SMC_ADC3	AD4	SMC_BMON_ISENSE
						SMC_ADC4	AB6	SMC_CPU_HI_ISENSE
51	OUT	I2C_SNS0_S0_SCL	N4	SMC_I2C1_SCL		SMC_ADC5	AH2	SMC_GPU_HS_ISENSE
51	BI	I2C_SNS0_S0_SDA	P4	SMC_I2C1_SDA		SMC_ADC6	AG4	SMC_P3V3_WLAN_ISENSE
						SMC_ADC7	AC5	SMC_P3V3_CAPLE_ISENSE
51	OUT	I2C_SNS1_S0_SCL	U5	SMC_I2C2_SCL				
51	BI	I2C_SNS1_S0_SDA	M2	SMC_I2C2_SDA		REFP_ADC	AF4	PP1V25_SLPS2R_SMC_AVREF
						58 REFM_ADC	AG3	GND_SMC_AVSS
51	OUT	I2C_DISP_SCL	U6	SMC_I2C3_SCL				
51	BI	I2C_DISP_SDA	R4	SMC_I2C3_SDA		SMC_PWM0	J2	SMC_FAN_0_PWM
						SMC_TACH0	L3	SMC_FAN_0_TACH
119 51	OUT	I2C_PWR_SCL	P3	SMC_I2C4_SCL				
119 51	BI	I2C_PWR_SDA	T4	SMC_I2C4_SDA		SMC_PWM1	R6	SMC_FAN_1_PWM
						SMC_TACH1	L2	SMC_FAN_1_TACH
51	OUT	I2C_SNS_G3S_SCL	R2	SMC_I2C5_SCL				
51	BI	I2C_SNS_G3S_SDA	P2	SMC_I2C5_SDA		SMC_PWM2	M4	NC_SMC_LED_ONEWIRE
						SMC_UART0_RXD	V4	SMC_DEBUGPRT_RX
51	OUT	I2C_SSD_SCL	R3	SMC_I2C6_SCL	(IPU)	SMC_UART0_TXD	V5	SMC_DEBUGPRT_TX
51	BI	I2C_SSD_SDA	T2	SMC_I2C6_SDA				
						SWD_OUT0_TCK	AE3	SSD0_SWCLK_UART_R2D
						SWD_OUT0_TMS	AA5	SSD0_SWDIO_UART_D2R
						SWD_OUT1_TCK	AF2	SSD1_SWCLK_UART_R2D
						SWD_OUT1_TMS	AA7	SSD1_SWDIO_UART_D2R

XW4089
SM
PLACE_NEAR=U3900.AF3:4MM

PP1V8_S5 — 80

R4046	10K 1/20W MF 201 5%	SOC_JTAG_SEL	39 121
R4047	100K 1/20W MF 201 5%	SOC_DOCK_CONNECT	30 31 39 119
R4054	100K 1/20W MF 201 5%	ESPI_IO<0>	12 20 39 118
R4055	100K 1/20W MF 201 5%	ESPI_IO<1>	12 20 39 118
R4056	100K 1/20W MF 201 5%	ESPI_IO<2>	12 20 39 118
R4057	100K 1/20W MF 201 5%	ESPI_IO<3>	12 20 39 118
R4059	100K 1/20W MF 201 5%	ESPI_CS_L	12 20 39

BOM_COST_GROUP=SOC

SYNC_MASTER=SILU
SYNC_DATE=03/22/2017

PAGE TITLE
SoC AOP/AON/SMC

Apple Inc.

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SIZE D
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OMIT_TABLE
CRITICAL

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ISP

82 47	IN	MIPI_FTCAM_DATA_P<0>	B27	MIPI0C_DATA0_P	ISP_I2C0_SDA	AF32	I2C_FTCAM_SDA	BI 52
82 47	IN	MIPI_FTCAM_DATA_N<0>	A27	MIPI0C_DATA0_N	ISP_I2C0_SCL	AH36	I2C_FTCAM_SCL	OUT 52
47	IN	GND	B25	MIPI0C_DATA1_P	ISP_I2C1_SDA	AB32	NC_I2C_PLCAM_SDA	BI 52
47	IN	GND	A25	MIPI0C_DATA1_N	ISP_I2C1_SCL	AG32	NC_I2C_PLCAM_SCL	OUT 52
82 47	IN	MIPI_FTCAM_CLK_P	B26	MIPI0C_CLK_P	SENSOR0_CLK	AK35	NC_FTCAM_CLK12M_R	OUT 47
82 47	IN	MIPI_FTCAM_CLK_N	A26	MIPI0C_CLK_N	SENSOR0_RST	AK34	NC_FTCAM_RESET_L	OUT 47
					SENSOR0_ISTRB	AJ33	DFR_TOUCH_RESET_L	OUT 50 120
47	IN	GND	B28	MIPI1C_DATA0_P	SENSOR1_CLK	AD33	NC_PLCAM_RX_CLK12M_R	OUT 47
47	IN	GND	A28	MIPI1C_DATA0_N	SENSOR1_RST	AC32	NC_PLCAM_RX_RESET_L	OUT 47
47	IN	GND	B30	MIPI1C_DATA1_P	SENSOR1_ISTRB	AC34	DFR_DISP_RESET_L	OUT 50 120
47	IN	GND	A30	MIPI1C_DATA1_N	SENSOR2_CLK	AD32	NC_PLCAM_TX_CLK12M_R	OUT 47
47	IN	GND	B29	MIPI1C_CLK_P	SENSOR2_RST	AJ32	NC_PLCAM_TX_RESET_L	OUT 47
47	IN	GND	A29	MIPI1C_CLK_N	(IPD) SENSOR_INT	AA33	NC_PLCAM_TX_INT	IN 47
50	OUT	MIPI_DFR_DATA_P	B33	MIPID_DATA0_P	(IPD) DISP_TE	H32	DFR_DISP_TE	IN 50 120
50	OUT	MIPI_DFR_DATA_N	A33	MIPID_DATA0_N	DISP_VSYNC	T36	BOARD_REV2	IN 46
50	OUT	MIPI_DFR_CLK_P	B32	MIPID_CLK_P	CLK32K_OUT	AK33	DFR_TOUCH_CLK32K_RESET_L	OUT 50 120
50	OUT	MIPI_DFR_CLK_N	A32	MIPID_CLK_N				
		SOC_MIPI0C_REXT	F23	MIPI0C_REXT				
		SOC_MIPI1C_REXT	F26	MIPI1C_REXT				
		SOC_MIPID_REXT	F27	MIPID_REXT				

R4100 4.02K 1% 1/20W MF 201
R4101 4.02K 1% 1/20W MF 201
R4102 4.02K 1% 1/20W MF 201

OMIT_TABLE
CRITICAL

U3900
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I2C/UART/SPI/I2S

52	BI	I2C_SPKRAMP_L_SDA	AE35	I2C0_SDA	SPI0_MISO	AR9	SPI_SOCROM_MISO	IN 46
52	OUT	I2C_SPKRAMP_L_SCL	AD35	I2C0_SCL	SPI0_MOSI	AR7	SPI_SOCROM_MOSI_R	R4171 20 1% 1/20W MF 201 SPI_SOCROM_MOSI OUT 46
52	BI	I2C_SPKRAMP_R_SDA	AE34	I2C1_SDA	SPI0_SCLK	AU7	SPI_SOCROM_CLK_R	R4172 20 1% 1/20W MF 201 SPI_SOCROM_CLK OUT 46
52	OUT	I2C_SPKRAMP_R_SCL	AG35	I2C1_SCL	SPI0_SSIN	AT9	SPI_SOCROM_CS_L	OUT 46
52	BI	I2C_CODEC_SDA	M34	I2C2_SDA	(IPU) SPI1_MISO	P36	SPI_TPAD_MISO	IN 46 47
52	OUT	I2C_CODEC_SCL	R33	I2C2_SCL	SPI1_MOSI	N34	SPI_TPAD_MOSI_R	OUT 47
120 52	BI	I2C_ALS_SDA	Y32	I2C3_SDA	SPI1_SCLK	P35	SPI_TPAD_CLK_R	OUT 47
120 52	OUT	I2C_ALS_SCL	AE34	I2C3_SCL	SPI1_SSIN	T32	SPI_TPAD_CS_L	OUT 66
52	BI	I2C_DFR_SDA	T34	I2C4_SDA	SPI2_MISO	A19	SPI_MESA_MISO	IN 48
52	OUT	I2C_DFR_SCL	U32	I2C4_SCL	SPI2_MOSI	A20	SPI_MESA_MOSI_R	OUT 47
52	BI	NC_I2C_SOC_5_SDA	R35	I2C5_SDA	SPI2_SCLK	C19	SPI_MESA_CLK_R	OUT 47
52	OUT	NC_I2C_SOC_5_SCL	U33	I2C5_SCL	SPI2_SSIN	A18	WLAN_JTAG_TDI	OUT 37 121
47	IN	NC_SPKR_ID1	P34	I2C6_SDA (IPU)	SPI3_MISO	C17	SPI_DFR_MISO	IN 47
120 63	IN	SPKR_ID0	R34	I2C6_SCL (IPU)	SPI3_MOSI	C18	SPI_DFR_MOSI_R	OUT 47
					SPI3_SCLK	B18	SPI_DFR_CLK_R	OUT 47
126 119	IN	SOC_DEBUGPRT_RX	Y33	UART0_RXD (IPU)	SPI3_SSIN	A17	SPI_DFR_CS_L	OUT 50 120
126 119	OUT	SOC_DEBUGPRT_TX	Y34	UART0_TXD				
49	IN	UART_SE_D2R	B15	UART1_RXD	(IPD) I2S0_DIN	AC33	I2S_SPKRAMP_L_D2R	IN 62 63
49	OUT	UART_SE_R2D	A15	UART1_TXD	I2S0_DOUT	AG34	I2S_SPKRAMP_L_R2D_R	OUT 47
49	IN	UART_SE_D2R_CTS_L	C15	UART1_CTS*	I2S0_BCLK	AA32	I2S_SPKRAMP_L_BCLK_R	OUT 47
49	OUT	UART_SE_R2D_RTS_L	D15	UART1_RTS*	I2S0_LRCK	AG33	I2S_SPKRAMP_L_LRCLK	OUT 47
35	IN	UART_BT_D2R	J36	UART2_RXD	I2S0_MCK	AR35	NC_DFR_TOUCH_RSVD	BI 47
35	OUT	UART_BT_R2D	J35	UART2_TXD	(IPD) I2S1_DIN	B20	I2S_SPKRAMP_R_D2R	IN 47
35	IN	UART_BT_D2R_CTS_L	N38	UART2_CTS*	I2S1_DOUT	C20	I2S_SPKRAMP_R_R2D_R	OUT 47
35	OUT	UART_BT_R2D_RTS_L	M38	UART2_RTS*	I2S1_BCLK	C21	I2S_SPKRAMP_R_BCLK_R	OUT 47
36	IN	UART_BT_LH_D2R	M36	UART3_RXD	I2S1_LRCK	A21	I2S_SPKRAMP_R_LRCLK	OUT 47
36	OUT	UART_BT_LH_R2D	N36	UART3_TXD	I2S1_MCK	D21	NC_PCHROM_SW_EN	OUT 47
47	IN	NC_UART_GNSS_D2R_CTS_L	M35	UART3_CTS*	(IPD) I2S2_DIN	AH34	I2S_CODEC_D2R	IN 61
47	OUT	NC_UART_GNSS_R2D_RTS_L	U34	UART3_RTS*	I2S2_DOUT	AB34	I2S_CODEC_R2D_R	OUT 47
37 36	IN	UART_WLAN_D2R	B14	UART4_RXD	I2S2_BCLK	AE33	I2S_CODEC_BCLK_R	OUT 47
37 36	OUT	UART_WLAN_R2D	A14	UART4_TXD	I2S2_LRCK	AH35	I2S_CODEC_LRCLK	OUT 47
37 36	IN	UART_WLAN_D2R_CTS_L	C14	UART4_CTS*	I2S2_MCK	AR33	NC_I2S_CODEC_MCLK	OUT 47
37 36	OUT	UART_WLAN_R2D_RTS_L	C13	UART4_RTS*	(IPD) I2S3_DIN	AD36	NC_I2S_HAWKING_D2R	IN 47
					I2S3_DOUT	AB35	NC_I2S_CODEC1_R2D_R	OUT 47
					I2S3_BCLK	AE36	NC_I2S_HAWKING_BCLK	OUT 47
					I2S3_LRCK	W34	NC_I2S_HAWKING_LRCLK	OUT 47
					I2S3_MCK	AG36	NC_I2S_CODEC1_MCLK	OUT 47

PLACE_NEAR=U3900.AR7:5MM
PLACE_NEAR=U3900.AU7:5MM

SYNC_MASTER=H9M and PMIC
SYNC_DATE=03/07/2017

PAGE TITLE
SoC ISP/I2C/UART/SPI/I2S

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
REVISION 4.0.0
BRANCH evt-0
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BOM_COST_GROUP=SOC

(All Caps)
GND_VOID=TRUE

C4210 0.22UF 20% 6.3V X5R 0201
C4211 0.22UF 20% 6.3V X5R 0201
C4212 0.22UF 20% 6.3V X5R 0201
C4213 0.22UF 20% 6.3V X5R 0201
C4214 0.22UF 20% 6.3V X5R 0201
C4215 0.22UF 20% 6.3V X5R 0201
C4216 0.22UF 20% 6.3V X5R 0201
C4217 0.22UF 20% 6.3V X5R 0201

R4218 1K 5% 1/20W MF 201

R4200 3.01K 1% 1/20W MF 201

OMIT_TABLE
CRITICAL

U3900
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BGA
SYM 1 OF 18
PCIE UP/DN

118 14 OUT	PCIE_SOC_D2R_P<0>		PCIE_SOC_D2R_C_P<0>	B10	PCIE_UP_TX0_P	AV31	NC_PCIE_WLAN_R2D_C_P OUT 47
118 14 OUT	PCIE_SOC_D2R_N<0>		PCIE_SOC_D2R_C_N<0>	C10	PCIE_UP_TX0_N	AU31	NC_PCIE_WLAN_R2D_C_N OUT 47
		118 47 IN	PCIE_SOC_R2D_P<0>	E10	PCIE_UP_RX0_P	AR31	NC_PCIE_WLAN_D2R_P IN 47
		118 47 IN	PCIE_SOC_R2D_N<0>	F10	PCIE_UP_RX0_N	AP31	NC_PCIE_WLAN_D2R_N IN 47
118 14 OUT	PCIE_SOC_D2R_P<1>		PCIE_SOC_D2R_C_P<1>	A9	PCIE_UP_TX1_P	AU30	NC_PCIE_ENET_R2D_C_P OUT 47
118 14 OUT	PCIE_SOC_D2R_N<1>		PCIE_SOC_D2R_C_N<1>	B9	PCIE_UP_TX1_N	AT30	NC_PCIE_ENET_R2D_C_N OUT 47
		118 47 IN	PCIE_SOC_R2D_P<1>	D9	PCIE_UP_RX1_P	AP30	NC_PCIE_ENET_D2R_P IN 47
		118 47 IN	PCIE_SOC_R2D_N<1>	E9	PCIE_UP_RX1_N	AN30	NC_PCIE_ENET_D2R_N IN 47
118 14 OUT	PCIE_SOC_D2R_P<2>		PCIE_SOC_D2R_C_P<2>	B8	PCIE_UP_TX2_P	AV29	PCIE_LIFEBOAT_R2D_C_P 47
118 14 OUT	PCIE_SOC_D2R_N<2>		PCIE_SOC_D2R_C_N<2>	C8	PCIE_UP_TX2_N	AU29	PCIE_LIFEBOAT_R2D_C_N 47
		118 47 IN	PCIE_SOC_R2D_P<2>	E8	PCIE_UP_RX2_P	AR29	PCIE_LIFEBOAT_D2R_P 47
		118 47 IN	PCIE_SOC_R2D_N<2>	F8	PCIE_UP_RX2_N	AP29	PCIE_LIFEBOAT_D2R_N 47
118 14 OUT	PCIE_SOC_D2R_P<3>		PCIE_SOC_D2R_C_P<3>	A7	PCIE_UP_TX3_P	AU28	NC_PCIE_DN3_R2D_CP 47
118 14 OUT	PCIE_SOC_D2R_N<3>		PCIE_SOC_D2R_C_N<3>	B7	PCIE_UP_TX3_N	AT28	NC_PCIE_DN3_R2D_CN 47
		118 47 IN	PCIE_SOC_R2D_P<3>	D7	PCIE_UP_RX3_P	AP28	NC_PCIE_DN3_D2RP 47
		118 47 IN	PCIE_SOC_R2D_N<3>	E7	PCIE_UP_RX3_N	AN28	NC_PCIE_DN3_D2RN 47
12 OUT	SOC_CLKREQ_L		SOC_CLKREQ_R_L	B21	PCIE_UP_CLKREQ*	AP26	NC_PCIE_CLK100M_WLAN_P OUT 47
		121 12 IN	PCIE_CLK100M_SOC_P	G13	PCIE_UP_EXT_REFCLK_P	AR26	NC_PCIE_CLK100M_WLAN_N OUT 47
		121 12 IN	PCIE_CLK100M_SOC_N	G12	PCIE_UP_EXT_REFCLK_N	AM33	NC_WLAN_CLKREQ_L IN 47
			SOC_PCIE_UP_REXT	G11	PCIE_UP_REXT	AN34	NC_WLAN_PERST_L OUT 47
						AN25	NC_PCIE_CLK100M_ENET_P OUT 47
						AP25	NC_PCIE_CLK100M_ENET_N OUT 47
						AN35	ENET_CLKREQ_L 41
						AK32	NC_ENET_RESET_L OUT 47
						AU26	PCIE_CLK100M_LIFEBOAT_P 47
						AV26	PCIE_CLK100M_LIFEBOAT_N 47
						AH32	PCIE_LIFEBOAT_CLKREQ_L 47
						AE32	PCIE_LIFEBOAT_RESET_L 47
						AT25	NC_PCIE_CLK100M_DN3P 47
						AU25	NC_PCIE_CLK100M_DN3N 47
						AJ34	NC_PCIEDN3_CLKREQ_L 47
						AK36	NC_PCIEDN3_RESET_L 47
					PCIE_DN_EXT_REFCLK_P	AM27	
					PCIE_DN_EXT_REFCLK_N	AM26	
					PCIE_DN_REXT	AM25	SOC_PCIE_DN_REXT

(UID_MODE strap on A00)

R4201 3.01K 1% 1/20W MF 201

OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 8 OF 18
PCIE STG 0/1

118 83 OUT	PCIE_SSD0_R2D_C_P<0>		AU11	PCIE_STG0_TX0_P	AU16	PCIE_SSD1_R2D_C_P<0>	OUT 88 118
118 83 OUT	PCIE_SSD0_R2D_C_N<0>		AT11	PCIE_STG0_TX0_N	AT16	PCIE_SSD1_R2D_C_N<0>	OUT 88 118
118 83 IN	PCIE_SSD0_D2R_P<0>		AP11	PCIE_STG0_RX0_P	AP16	PCIE_SSD1_D2R_P<0>	IN 88 118
118 83 IN	PCIE_SSD0_D2R_N<0>		AN11	PCIE_STG0_RX0_N	AN16	PCIE_SSD1_D2R_N<0>	IN 88 118
118 84 OUT	PCIE_SSD0_R2D_C_P<1>		AV12	PCIE_STG0_TX1_P	AV17	PCIE_SSD1_R2D_C_P<1>	OUT 89 118
118 84 OUT	PCIE_SSD0_R2D_C_N<1>		AU12	PCIE_STG0_TX1_N	AU17	PCIE_SSD1_R2D_C_N<1>	OUT 89 118
118 84 IN	PCIE_SSD0_D2R_P<1>		AR12	PCIE_STG0_RX1_P	AR17	PCIE_SSD1_D2R_P<1>	IN 89 118
118 84 IN	PCIE_SSD0_D2R_N<1>		AP12	PCIE_STG0_RX1_N	AP17	PCIE_SSD1_D2R_N<1>	IN 89 118
118 85 OUT	PCIE_SSD0_R2D_C_P<2>		AU13	PCIE_STG0_TX2_P	AU18	PCIE_SSD1_R2D_C_P<2>	OUT 90 118
118 85 OUT	PCIE_SSD0_R2D_C_N<2>		AT13	PCIE_STG0_TX2_N	AT18	PCIE_SSD1_R2D_C_N<2>	OUT 90 118
118 85 IN	PCIE_SSD0_D2R_P<2>		AP13	PCIE_STG0_RX2_P	AP18	PCIE_SSD1_D2R_P<2>	IN 90 118
118 85 IN	PCIE_SSD0_D2R_N<2>		AN13	PCIE_STG0_RX2_N	AN18	PCIE_SSD1_D2R_N<2>	IN 90 118
118 86 OUT	PCIE_SSD0_R2D_C_P<3>		AV14	PCIE_STG0_TX3_P	AV19	PCIE_SSD1_R2D_C_P<3>	OUT 91 118
118 86 OUT	PCIE_SSD0_R2D_C_N<3>		AU14	PCIE_STG0_TX3_N	AU19	PCIE_SSD1_R2D_C_N<3>	OUT 91 118
118 86 IN	PCIE_SSD0_D2R_P<3>		AR14	PCIE_STG0_RX3_P	AR19	PCIE_SSD1_D2R_P<3>	IN 91 118
118 86 IN	PCIE_SSD0_D2R_N<3>		AP14	PCIE_STG0_RX3_N	AP19	PCIE_SSD1_D2R_N<3>	IN 91 118
84 83 OUT	PCIE_CLK100M_SSD0_01_P		AP21	PCIE_STG0_REFCLK01_P	AU21	PCIE_CLK100M_SSD1_01_P	OUT 88 89
84 83 OUT	PCIE_CLK100M_SSD0_01_N		AR21	PCIE_STG0_REFCLK01_N	AV21	PCIE_CLK100M_SSD1_01_N	OUT 88 89
83 47 IN	SSD0_CLKREQ0_L		AT38	PCIE_STG0_CLKREQ0*	B17	SSD1_CLKREQ0_L	IN 47 88
84 47 IN	SSD0_CLKREQ1_L		AR34	PCIE_STG0_CLKREQ1*	D18	SSD1_CLKREQ1_L	IN 47 89
86 85 OUT	PCIE_CLK100M_SSD0_23_P		AN22	PCIE_STG0_REFCLK23_P	AT22	PCIE_CLK100M_SSD1_23_P	OUT 90 91
86 85 OUT	PCIE_CLK100M_SSD0_23_N		AP22	PCIE_STG0_REFCLK23_N	AU22	PCIE_CLK100M_SSD1_23_N	OUT 90 91
121 85 47 IN	SSD0_CLKREQ2_L		AP34	PCIE_STG0_CLKREQ2*	C16	SSD1_CLKREQ2_L	IN 47 90
121 86 47 IN	SSD0_CLKREQ3_L		AN38	PCIE_STG0_CLKREQ3*	A16	SSD1_CLKREQ3_L	IN 47 91
86 85 84 83 47 OUT	SSD0_PCIE_RESET_L		AR36	PCIE_STG0_PERST*	AP36	SSD1_PCIE_RESET_L	OUT 47 88 89 90 91
47 OUT	SSD0_CLK24M_R		AP7	PCIE_STG0_NANDCLK	AV7	SSD1_CLK24M_R	OUT 47
			AM14	PCIE_STG0_EXT_REFCLK_P	AM19	PCIE_STG1_EXT_REFCLK_P	
			AM15	PCIE_STG0_EXT_REFCLK_N	AM20	PCIE_STG1_EXT_REFCLK_N	
	SOC_PCIE_STG0_REXT		AM16	PCIE_STG0_REXT	AM21	PCIE_STG1_REXT	SOC_PCIE_STG1_REXT

R4250 3.01K 1% 1/20W MF 201

R4251 3.01K 1% 1/20W MF 201

PP1V8_AWAKE 46 47 80
R4232 47K 5% 1/20W MF 201
ENET_CLKREQ_L 41

BOM_COST_GROUP=SOC

SYNC_MASTER=SILU SYNC_DATE=03/15/2017

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SoC PCIe

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
REVISION 4.0.0
BRANCH evt-0
PAGE 42 OF 200
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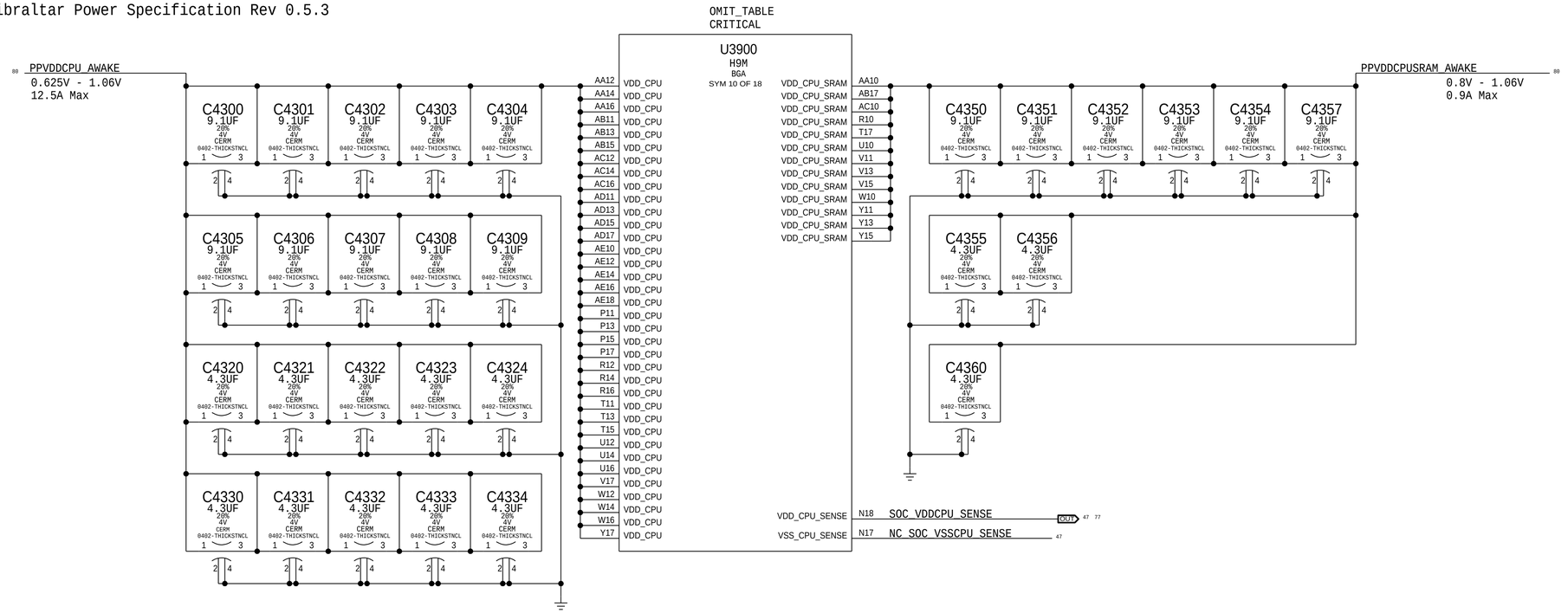
Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



SYNC_MASTER=SILU SYNC_DATE=04/04/2017

PAGE TITLE

SoC Power 1

Apple Inc.

DRAWING NUMBER 051-02643 SIZE D

REVISION 4.0.0

BRANCH evt-0

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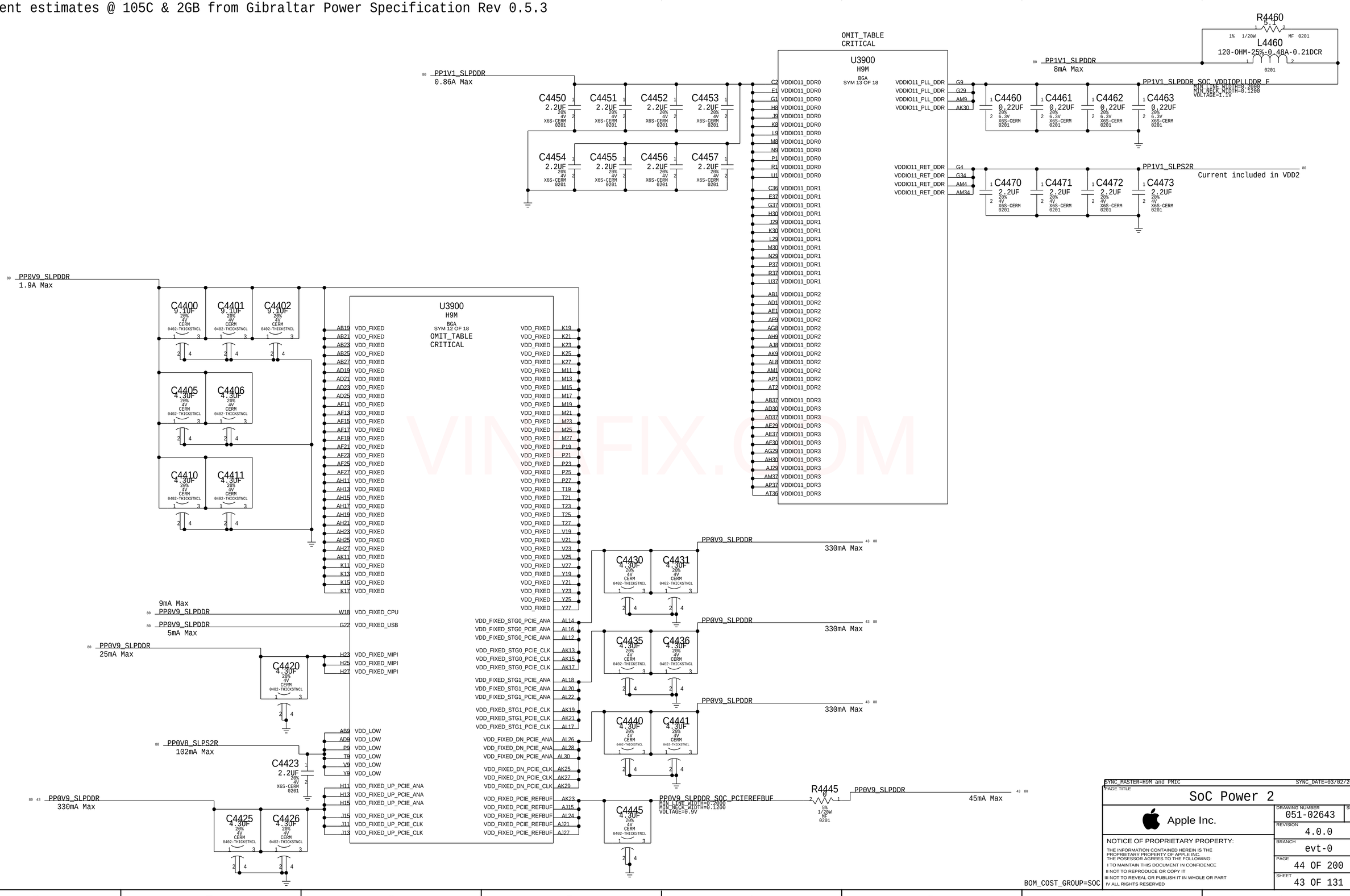
SHEET 42 OF 131

Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3



Current estimates @ 105C & 2GB from Gibraltar Power Specification Rev 0.5.3

OMIT_TABLE
CRITICAL

U3900
H9M
BGA
SYM 14 OF 18

PP1V8_SLPS2R
134mA Max

C4500 2.2UF 20% 4V X6S-CERM 0201
C4501 2.2UF 20% 4V X6S-CERM 0201
C4502 2.2UF 20% 4V X6S-CERM 0201
C4503 2.2UF 20% 4V X6S-CERM 0201

A4 VDD1
AV34 VDD1
AV4 VDD1
B35 VDD1
W1 VDD1
W37 VDD1
Y1 VDD1
Y37 VDD1

PP1V8_SLPS2R
20mA Max

C4510 2.2UF 20% 4V X6S-CERM 0201
C4511 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4512 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4513 0.1UF 10% 6.3V X6S 0201

AA9 VDDIO18_AOP1
P8 VDDIO18_AOP1
R9 VDDIO18_AOP1
T8 VDDIO18_AOP1
U9 VDDIO18_AOP1
W9 VDDIO18_AOP1
AC9 VDDIO18_AOP2
AD8 VDDIO18_AOP2
AE9 VDDIO18_AOP2

PP1V8_SLPS2R
1mA Max

R4546 49.9 1% 1/20W MF 201

MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.8V

PP1V8_SLPS2R_SOC_LPADC_RC

AB8 VDD18_LPADC

PP1V8_SLPS2R
1mA Max

R4519 49.9 1% 1/20W MF 201

PP1V8_SLPS2R_SOC_LPOSC_RC
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

AB10 VDD18_LPOSC

C4519 2.2UF 20% 4V X6S-CERM 0201
C4515 20UF 20% 2.5V X6S-CERM 0402

AA29 VDDIO18_GRP1
AB30 VDDIO18_GRP1
AC29 VDDIO18_GRP1
P30 VDDIO18_GRP1
R29 VDDIO18_GRP1
T30 VDDIO18_GRP1
U29 VDDIO18_GRP1
V30 VDDIO18_GRP1
W29 VDDIO18_GRP1
Y30 VDDIO18_GRP1

PP1V8_AWAKE
40mA Max

C4521 2.2UF 20% 4V X6S-CERM 0201
C4522 2.2UF 20% 4V X6S-CERM 0201
C4523 2.2UF 20% 4V X6S-CERM 0201
C4524 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4525 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4526 4.3UF 20% 4V CERM 0402-THICKSTNCL
C4527 4.3UF 20% 4V CERM 0402-THICKSTNCL

G16 VDDIO18_GRP2
G18 VDDIO18_GRP2
G20 VDDIO18_GRP2
H17 VDDIO18_GRP2
H19 VDDIO18_GRP2
H21 VDDIO18_GRP2

AK31 VDDIO18_GRP3
AM31 VDDIO18_GRP3

AL11 VDDIO18_GRP4
AM10 VDDIO18_GRP4

PP1V8_AWAKE
2mA Max

R4530 0 5% 1/20W MF 0201

MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000
VOLTAGE=1.8V

PP1V8_AWAKE_SOC_TSADC_RC

C4530 1UF 20% 16V CER-XSR 0201

AA18 VDD18_TSADC
P16 VDD18_TSADC
AD16 VDD18_TSADC
AE18 VDD18_TSADC
H28 VDD18_TSADC

PP1V8_AWAKE
7mA Max

C4535 2.2UF 20% 4V X6S-CERM 0201
C4536 0.1UF 10% 6.3V X6S 0201

G23 VDD18_MIPI
G25 VDD18_MIPI
G27 VDD18_MIPI

PP1V8_AWAKE
20mA Max

C4540 0.1UF 10% 6.3V X6S 0201

PP1V8_AWAKE_SOC_FMON_RC
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

H22 VDD18_USB
AF12 VDD18_FMON

AM30 VDD18_EFUSE1
AK12 VDD18_EFUSE2

PP1V8_AWAKE
1mA Max

R4545 49.9 1% 1/20W MF 201

C4545 1UF 20% 16V CER-XSR 0201

VDD12_CPU_UVD Y18
PP1V2_AWAKE
10mA Max

C4550 2.2UF 20% 4V X6S-CERM 0201

VOLTAGE=1.2V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

VDD12_PLL_CPU V18
PP1V2_AWAKE_SOC_PLLCPU_F

VDD12_PCIE_REFBUF AK24
VDD12_PCIE_REFBUF AM23
PP1V2_AWAKE_SOC_PCIEREFBUF_F

VDD12_DN_PCIE AM29
VDD12_UP_PCIE G14
VDD12_STG0_PCIE AM13
VDD12_STG1_PCIE AM18
PP1V2_AWAKE_SOC_PCIEPLL_F

VDD12_PLL_SOC AC23
VDD12_PLL_SOC AD24
VDD12_PLL_SOC AE23
PP1V2_AWAKE_SOC_PLLSOC_F

VDD2 AG1
VDD2 AG37
VDD2 AJ1
VDD2 AJ37
VDD2 AK1
VDD2 AK37
VDD2 AU3
VDD2 AU34
VDD2 AU35
VDD2 AU4
VDD2 B3
VDD2 B4
VDD2 C34
VDD2 D34
VDD2 J1
VDD2 J37
VDD2 K1
VDD2 K37
VDD2 M1
VDD2 M37
VDD2 W3
VDD2 W35
VDD2 Y3
VDD2 Y35

VDD11_XTAL AN23
PP1V1_SLPDDR_SOC_XTAL_F

VDD33_USB F21
PP3V3_AWAKE
12mA Max

C4595 0.1UF 10% 6.3V X6S 0201

R4555 0 5% 1/20W MF 0201
PP1V2_AWAKE
13mA Max

C4555 0.1UF 10% 6.3V X6S 0201

R4560 0 5% 1/20W MF 0201
PP1V2_AWAKE
80mA Max

C4560 0.1UF 10% 6.3V X6S 0201
C4561 0.1UF 10% 6.3V X6S 0201
C4562 2.2UF 20% 4V X6S-CERM 0201

R4565 0 5% 1/20W MF 0201
PP1V2_AWAKE
60mA Max

C4565 2.2UF 20% 4V X6S-CERM 0201
C4566 2.2UF 20% 4V X6S-CERM 0201
C4567 2.2UF 20% 4V X6S-CERM 0201
C4568 2.2UF 20% 4V X6S-CERM 0201

R4570 0 5% 1/20W MF 0201
PP1V2_AWAKE
31mA Max

C4570 0.1UF 10% 6.3V X6S 0201
C4571 0.1UF 10% 6.3V X6S 0201
C4572 2.2UF 20% 4V X6S-CERM 0201

PP1V1_SLPS2R
1.74A Max

C4580 2.2UF 20% 4V X6S-CERM 0201
C4581 2.2UF 20% 4V X6S-CERM 0201
C4582 2.2UF 20% 4V X6S-CERM 0201
C4583 2.2UF 20% 4V X6S-CERM 0201

R4590 5.1 1% 1/20W MF 0201

L4590 240-OHM-25%-0.42A-0.31DCR_PP1V1_SLPDDR 0201

PP1V1_SLPDDR
4mA Max

C4590 0.1UF 10% 6.3V X6S 0201
C4591 2.2UF 20% 4V X6S-CERM 0201

BOM_COST_GROUP=SOC

SYNC_MASTER=SILU SYNC_DATE=05/26/2017

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SoC Power 3

Apple Inc.

DRAWING NUMBER 051-02643
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REVISION 4.0.0
BRANCH evt-0
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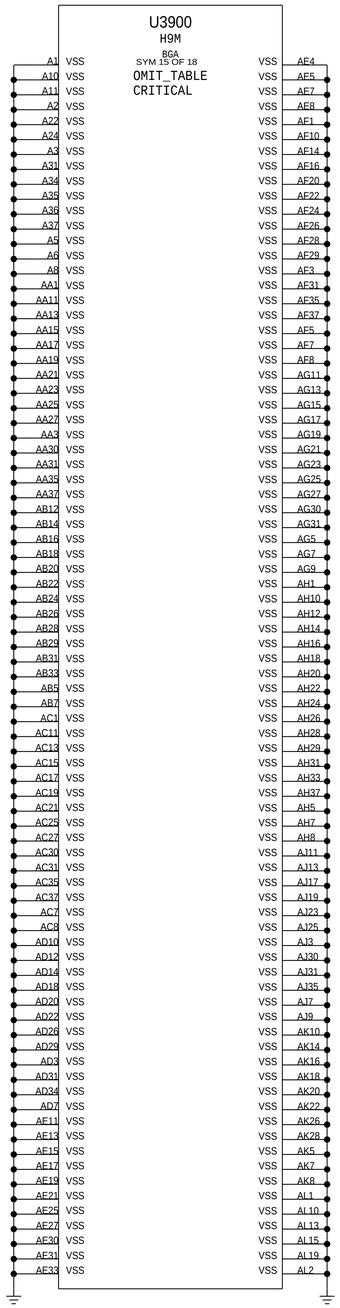

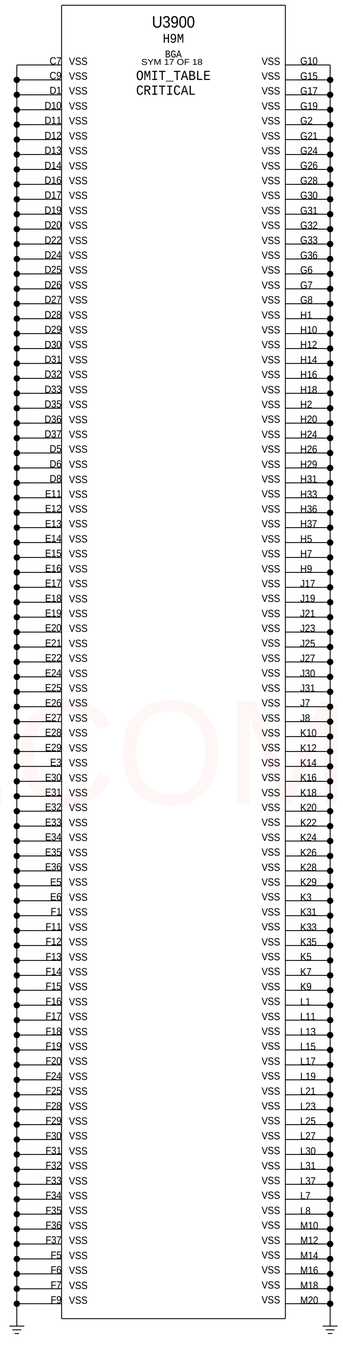

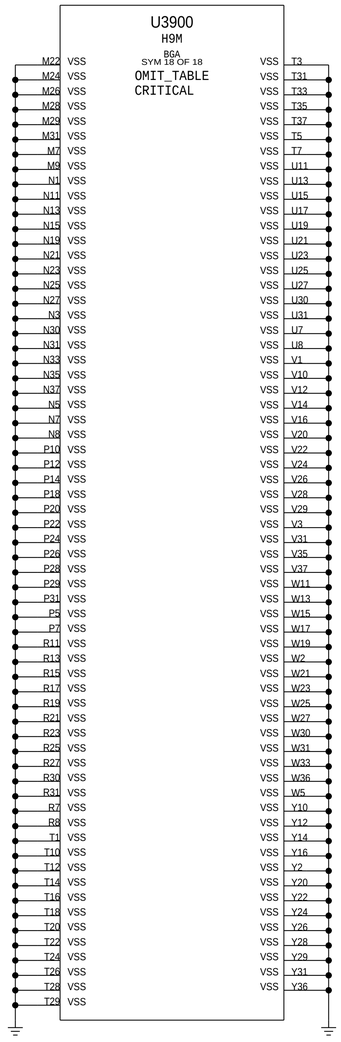

SYNC_MASTER=H9M and PMIC SYNC_DATE=03/02/2017

PAGE TITLE

SoC Ground

Apple Inc.

DRAWING NUMBER 051-02643 SIZE D

REVISION 4.0.0

BRANCH evt-0

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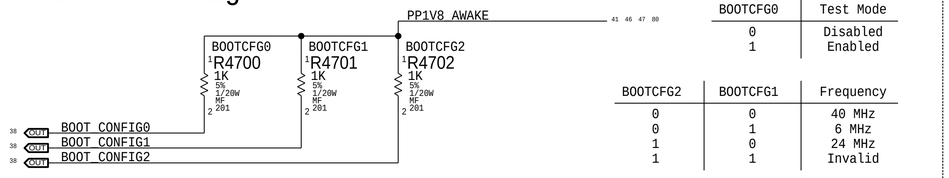
BOM_COST_GROUP=SOC

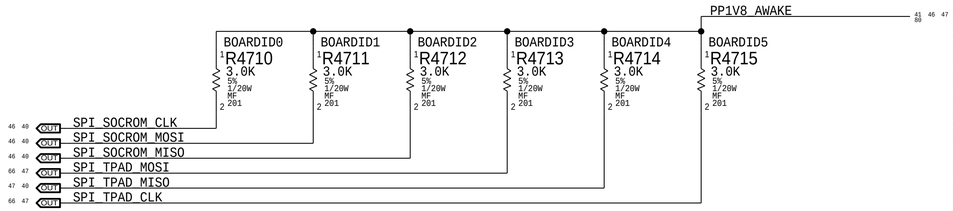
Boot Config



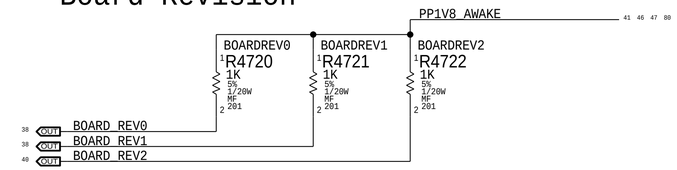
BOOTCFG0	Test Mode
0	Disabled
1	Enabled

BOOTCFG2	BOOTCFG1	Frequency
0	0	40 MHz
0	1	6 MHz
1	0	24 MHz
1	1	Invalid

Board ID

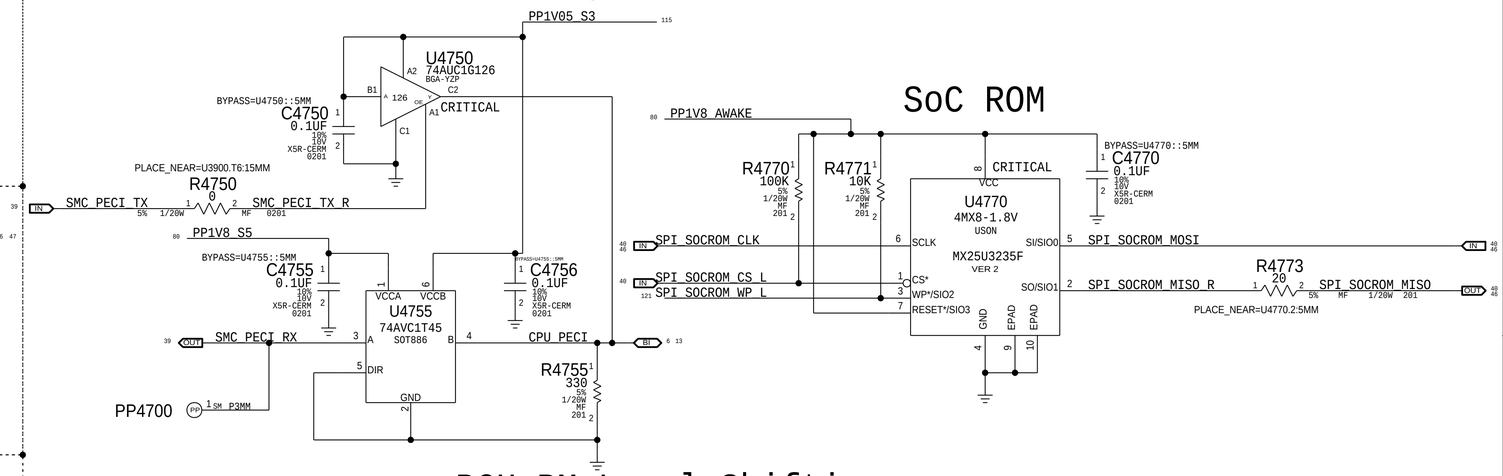


Board Revision



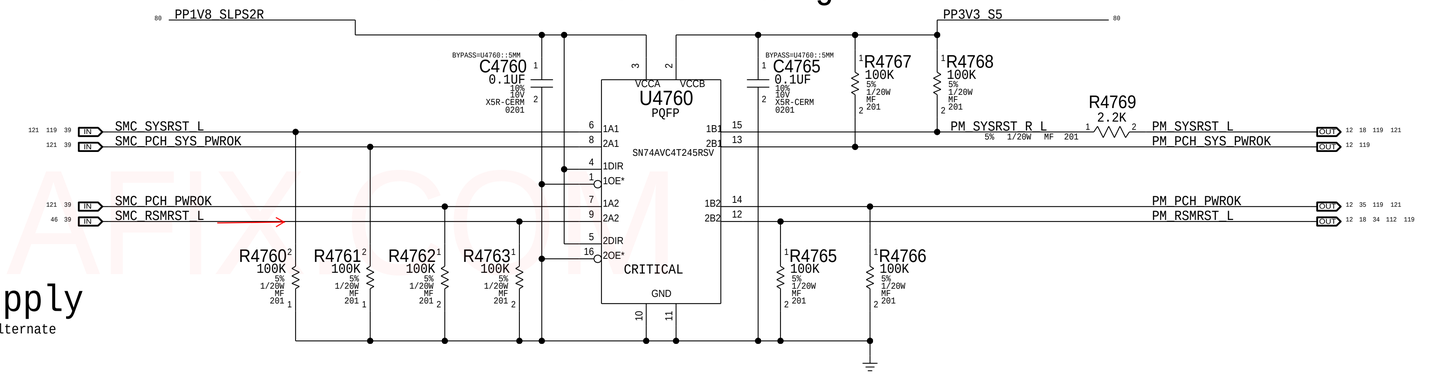
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00234	1	IC,SLG4AP41484,THERMTRIP,STQFN14	U4740	CRITICAL	

PECI Level Shifting



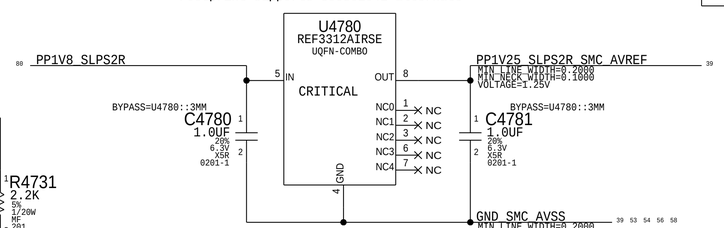
SoC ROM

PCH PM Level Shifting



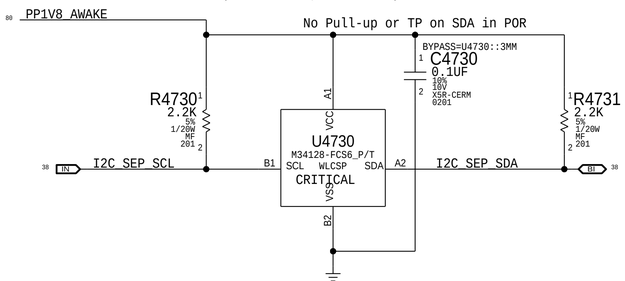
SMC AVREF Supply

Footprint supports 353S01042 alternate

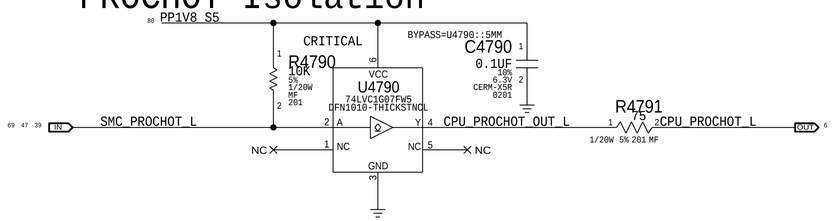


SEP EEPROM

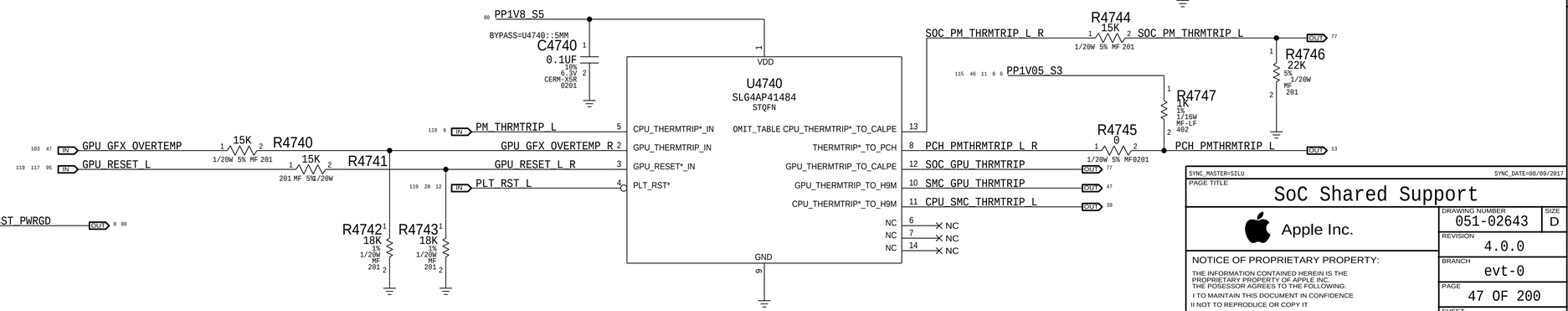
(Write: 0xA2, Read 0xA3)



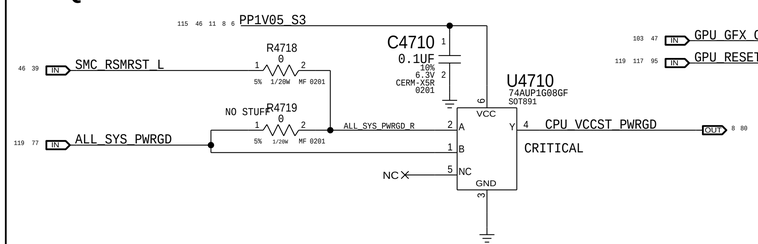
PROCHOT Isolation



THRMTRIP# Isolation



Qualifier with RSMRST#



PCIe Up R2D AC Caps

(All Caps)

118 14	IN	PCIE_SOC_R2D_C_P<0>	C4820	0.22UF	20% 6.3V X5R 0201	PCIE_SOC_R2D_P<0>	OUT	41 118
118 14	IN	PCIE_SOC_R2D_C_N<0>	C4821	0.22UF	20% 6.3V X5R 0201	PCIE_SOC_R2D_N<0>	OUT	41 118
118 14	IN	PCIE_SOC_R2D_C_P<1>	C4822	0.22UF	20% 6.3V X5R 0201	PCIE_SOC_R2D_P<1>	OUT	41 118
118 14	IN	PCIE_SOC_R2D_C_N<1>	C4823	0.22UF	20% 6.3V X5R 0201	PCIE_SOC_R2D_N<1>	OUT	41 118
118 14	IN	PCIE_SOC_R2D_C_P<2>	C4824	0.22UF	20% 6.3V X5R 0201	PCIE_SOC_R2D_P<2>	OUT	41 118
118 14	IN	PCIE_SOC_R2D_C_N<2>	C4825	0.22UF	20% 6.3V X5R 0201	PCIE_SOC_R2D_N<2>	OUT	41 118
118 14	IN	PCIE_SOC_R2D_C_P<3>	C4826	0.22UF	20% 6.3V X5R 0201	PCIE_SOC_R2D_P<3>	OUT	41 118
118 14	IN	PCIE_SOC_R2D_C_N<3>	C4827	0.22UF	20% 6.3V X5R 0201	PCIE_SOC_R2D_N<3>	OUT	41 118

GPIO Source Termination

40	IN	I2S_SPKRAMP_L_R2D_R	R4843	20	PLACE_NEAR=U3900.AG34:5MM	I2S_SPKRAMP_L_R2D	OUT	62
40	IN	I2S_SPKRAMP_L_BCLK_R	R4844	20	PLACE_NEAR=U3900.AA32:5MM	I2S_SPKRAMP_L_BCLK	OUT	62
62	IN	I2S_SPKRAMP_L_LRCLK_R	R4863	20	PLACE_NEAR=U3900.AA32:10MM	I2S_SPKRAMP_L_LRCLK	OUT	40
40	IN	I2S_SPKRAMP_R_R2D_R	R4845	20	PLACE_NEAR=U3900.C20:5MM	I2S_SPKRAMP_R_R2D	OUT	63
40	IN	I2S_SPKRAMP_R_BCLK_R	R4846	20	PLACE_NEAR=U3900.C21:5MM	I2S_SPKRAMP_R_BCLK	OUT	63
63	IN	I2S_SPKRAMP_R_LRCLK_R	R4864	20	PLACE_NEAR=U3900.C21:10MM	I2S_SPKRAMP_R_LRCLK	OUT	40
40	IN	I2S_CODEC_R2D_R	R4847	20	PLACE_NEAR=U3900.AB34:5MM	I2S_CODEC_R2D	OUT	61
40	IN	I2S_CODEC_BCLK_R	R4848	20	PLACE_NEAR=U3900.AF33:5MM	I2S_CODEC_BCLK	OUT	61
61	IN	I2S_CODEC_LRCLK_R	R4865	20	PLACE_NEAR=U3900.AF33:5MM	I2S_CODEC_LRCLK	OUT	40
40	IN	SPI_TPAD_MOSI_R	R4851	20	PLACE_NEAR=U3900.N34:5MM	SPI_TPAD_MOSI	OUT	46 66
40	IN	SPI_TPAD_CLK_R	R4852	20	PLACE_NEAR=U3900.P35:5MM	SPI_TPAD_CLK	OUT	46 66
40	IN	SPI_MESA_MOSI_R	R4853	20	PLACE_NEAR=U3900.A20:5MM	SPI_MESA_MOSI	OUT	48
40	IN	SPI_MESA_CLK_R	R4854	20	PLACE_NEAR=U3900.C19:5MM	SPI_MESA_CLK	OUT	48
120 50	OUT	SPI_DFR_MISO_R	R4866	20	PLACE_NEAR=J5100.7:5MM	SPI_DFR_MISO	IN	40
40	IN	SPI_DFR_MOSI_R	R4855	20	PLACE_NEAR=U3900.C18:5MM	SPI_DFR_MOSI	OUT	50 120
40	IN	SPI_DFR_CLK_R	R4856	20	PLACE_NEAR=U3900.B18:5MM	SPI_DFR_CLK	OUT	50 120
41	IN	SSD0_CLK24M_R	R4857	20	PLACE_NEAR=U3900.AP7:5MM	SSD0_CLK24M	OUT	47 83 85
41	IN	SSD1_CLK24M_R	R4858	20	PLACE_NEAR=U3900.AV7:5MM	SSD1_CLK24M	OUT	47 88 90
39	IN	PDM_DMIC_CLK0_R	R4859	20	PLACE_NEAR=U3900.P6:15MM	PDM_DMIC_CLK0	OUT	64
39	IN	PDM_DMIC_CLK1_R	R4860	20	PLACE_NEAR=U3900.K2:15MM	PDM_DMIC_CLK1	OUT	64
39	IN	SPI_AOP_SENSOR_MOSI_R	R4861	20	PLACE_NEAR=U3900.F2:15MM	SPI_AOP_SENSOR_MOSI	OUT	37
39	IN	SPI_AOP_SENSOR_CLK_R	R4862	20	PLACE_NEAR=U3900.E2:15MM	SPI_AOP_SENSOR_CLK	OUT	37
37	OUT	SPI_AOP_SENSOR_MISO_R	R4869	20	PLACE_NEAR=U3900.E3:5MM	SPI_AOP_SENSOR_MISO	IN	39
46 40	OUT	SPI_TPAD_MISO	R4809	20	PLACE_NEAR=U3900.P36:20MM	SPI_TPAD_MISO_R	IN	66

S4E_X4PLUS

Lifeboat

41	PCIE_LIFEBOAT_R2D_C_P	PCIE_LIFEBOAT_R2D_C_P	TP4800
41	PCIE_LIFEBOAT_R2D_C_N	PCIE_LIFEBOAT_R2D_C_N	TP4801
41	PCIE_LIFEBOAT_D2R_P	PCIE_LIFEBOAT_D2R_P	TP4802
41	PCIE_LIFEBOAT_D2R_N	PCIE_LIFEBOAT_D2R_N	TP4803
41	PCIE_CLK100M_LIFEBOAT_P	PCIE_CLK100M_LIFEBOAT_P	TP4804
41	PCIE_CLK100M_LIFEBOAT_N	PCIE_CLK100M_LIFEBOAT_N	TP4805
41	PCIE_LIFEBOAT_CLKREQ_L	PCIE_LIFEBOAT_CLKREQ_L	TP4806
41	PCIE_LIFEBOAT_RESET_L	PCIE_LIFEBOAT_RESET_L	TP4807

MAKE_BASE=TRUE; TP-P5

119 39 SMC_FIXTURE_MODE_L — MAKE_BASE — SMC_FIXTURE_MODE_L

FIXMODE_NO: R4801 100K 5% 1/20W MF 201

Clamshell Open = High / Clamshell Closed = Low

Lid Detect Sensors

80 47 PP1V8_SLPS2R

OMIT_TABLE
J4800
AMR-MLB-X502
SM

AMR_PU R4807 330K 5% 1/20W MF 201

SMC_LID_LEFT — R4804 10K 5% 1/20W MF 201 — LID_OPEN_LEFT — OUT 39
PP1V8_SLPS2R 47 80

LID_OPEN_LEFT — MAKE_BASE — 64 120

OMIT_TABLE
J4801
AMR-MLB-X502
SM

AMR_PU R4808 330K 5% 1/20W MF 201

SMC_LID_RIGHT — R4805 10K 5% 1/20W MF 201 — LID_OPEN_RIGHT — OUT 39
PP1V8_SLPS2R 47 80

LID_OPEN_RIGHT — MAKE_BASE — 64 120

PP1V8_SLPS2R 80 47
BYPASS=U4802::5MM
C4802 0.1UF 10% 6.3V CERM-X5R 0201

U4802 74LVC1G32 SOT891
IPD_LID_OPEN — OUT 50 65 120
NC

No Connects

39	NC_SPI_ALTIMETER_CS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_ALTIMETER_CS_L
39	NC_ALTIMETER_INT	MAKE_BASE=TRUE	NO_TEST=1	NC_ALTIMETER_INT
77	NC_PMU_CLK32K_GNSS_R	MAKE_BASE=TRUE	NO_TEST=1	NC_PMU_CLK32K_GNSS_R
40	NC_UART_GNSS_D2R_CTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART_GNSS_D2R_CTS_L
40	NC_UART_GNSS_R2D_RTS_L	MAKE_BASE=TRUE	NO_TEST=1	NC_UART_GNSS_R2D_RTS_L
38	NC_GNSS_HOST_TIME	MAKE_BASE=TRUE	NO_TEST=1	NC_GNSS_HOST_TIME
39	NC_GNSS_HOST_WAKE	MAKE_BASE=TRUE	NO_TEST=1	NC_GNSS_HOST_WAKE
38	NC_GNSS_DEV_WAKE	MAKE_BASE=TRUE	NO_TEST=1	NC_GNSS_DEV_WAKE
39	NC_ENET_MEDIA_SENSE	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_MEDIA_SENSE
39	NC_ENET_LOW_PWR	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_LOW_PWR
40	NC_I2S_HAWKING_D2R	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_HAWKING_D2R
40	NC_I2S_HAWKING_LRCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_HAWKING_LRCLK
40	NC_I2S_HAWKING_BCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_HAWKING_BCLK
40	NC_I2S_CODEC1_R2D_R	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_CODEC1_R2D_R
40	NC_PLCAM_RX_CLK12M_R	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_RX_CLK12M_R
40	NC_PLCAM_RX_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_RX_RESET_L
40	NC_PLCAM_TX_CLK12M_R	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_TX_CLK12M_R
40	NC_PLCAM_TX_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_TX_RESET_L
40	NC_PLCAM_TX_INT	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_TX_INT
38	NC_PLCAM_TX_THROTTLE	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_TX_THROTTLE
39	NC_PLCAM_PROX_INT_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_PROX_INT_L
39	NC_PLCAM_ROMEO_B2B_DETECT	MAKE_BASE=TRUE	NO_TEST=1	NC_PLCAM_ROMEO_B2B_DETECT
40	NC_PCHROM_SW_EN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCHROM_SW_EN
39	NC_SDCONN_STATE_CHANGE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SDCONN_STATE_CHANGE_L
40	NC_FTCAM_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_RESET_L
40	NC_FTCAM_CLK12M_R	MAKE_BASE=TRUE	NO_TEST=1	NC_FTCAM_CLK12M_R
40	NC_I2S_CODEC_MCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_CODEC_MCLK
40	NC_I2S_CODEC1_MCLK	MAKE_BASE=TRUE	NO_TEST=1	NC_I2S_CODEC1_MCLK
39	NC_SPI_DSCRPTR_OVERRIDE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_SPI_DSCRPTR_OVERRIDE_L
39	NC_I2C_AOP_SCL	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_AOP_SCL
39	NC_I2C_AOP_SDA	MAKE_BASE=TRUE	NO_TEST=1	NC_I2C_AOP_SDA
38	NC_SOC_USB_ID	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_USB_ID
38	NC_SOC_TST_CLKOUT	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_TST_CLKOUT
38	NC_SOC_AMUXOUT	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_AMUXOUT

40	NC_SPKR_ID1	MAKE_BASE=TRUE	NO_TEST=1	NC_SPKR_ID1
39	NC_SMC_LED_ONEWIRE	MAKE_BASE=TRUE	NO_TEST=1	NC_SMC_LED_ONEWIRE
39	NC_PCIEDN_WAKE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIEDN_WAKE_L
39	NC_MESA_MENUKEY_L	MAKE_BASE=TRUE	NO_TEST=1	NC_MESA_MENUKEY_L
39	NC_TPAD_VIBE_L	MAKE_BASE=TRUE	NO_TEST=1	NC_TPAD_VIBE_L
41	NC_ENET_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_ENET_RESET_L
38	NC_WLAN_DEV_WAKE	MAKE_BASE=TRUE	NO_TEST=1	NC_WLAN_DEV_WAKE
42	NC_SOC_VSSCPU_SENSE	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_VSSCPU_SENSE
42	NC_SOC_VSSSOC_SENSE	MAKE_BASE=TRUE	NO_TEST=1	NC_SOC_VSSSOC_SENSE
40	NC_DFR_TOUCH_RSVD	MAKE_BASE=TRUE	NO_TEST=1	NC_DFR_TOUCH_RSVD
41	NC_PCIE_DN3_R2D_CP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN3_R2D_CP
41	NC_PCIE_DN3_R2D_CN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN3_R2D_CN
41	NC_PCIE_DN3_D2RP	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN3_D2RP
41	NC_PCIE_DN3_D2RN	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_DN3_D2RN
41	NC_PCIE_CLK100M_DN3P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_DN3P
41	NC_PCIE_CLK100M_DN3N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_DN3N
41	NC_PCIEDN3_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIEDN3_CLKREQ_L
41	NC_PCIEDN3_RESET_L	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIEDN3_RESET_L
41	NC_PCIE_WLAN_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_WLAN_R2D_C_P
41	NC_PCIE_WLAN_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_WLAN_R2D_C_N
41	NC_PCIE_WLAN_D2R_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_WLAN_D2R_P
41	NC_PCIE_WLAN_D2R_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_WLAN_D2R_N
41	NC_WLAN_CLKREQ_L	MAKE_BASE=TRUE	NO_TEST=1	NC_WLAN_CLKREQ_L
41	NC_WLAN_PERST_L	MAKE_BASE=TRUE	NO_TEST=1	NC_WLAN_PERST_L
41	NC_PCIE_ENET_R2D_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2D_C_P
41	NC_PCIE_ENET_R2D_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_R2D_C_N
41	NC_PCIE_ENET_D2R_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2R_P
41	NC_PCIE_ENET_D2R_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_ENET_D2R_N
41	NC_PCIE_CLK100M_ENET_P	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENET_P
41	NC_PCIE_CLK100M_ENET_N	MAKE_BASE=TRUE	NO_TEST=1	NC_PCIE_CLK100M_ENET_N
41	NC_PCIE_CLK100M_WLAN_P	MAKE_BASE	NO_TEST=1	NC_PCIE_CLK100M_WLAN_P
41	NC_PCIE_CLK100M_WLAN_N	MAKE_BASE	NO_TEST=1	NC_PCIE_CLK100M_WLAN_N

Signal Aliases

39	TPAD_KBD_WAKE_L	MAKE_BASE	TPAD_KBD_WAKE_L 65 66 120
39	TPAD_SPI_INT_L	MAKE_BASE	TPAD_SPI_INT_L 66
39	TPAD_ACTUATOR_DISABLE_L	MAKE_BASE	TPAD_ACTUATOR_DISABLE_L 66
	GPU_GFX_OVERTEMP	MAKE_BASE	GPU_GFX_OVERTEMP 46 103
126 119 39	SMC_DEBUGPRT_RX	MAKE_BASE	SMC_DEBUGPRT_RX 107 108
126 119 39	SMC_DEBUGPRT_TX	MAKE_BASE	SMC_DEBUGPRT_TX 107 108
39	SMC_GPU_THRMTRIP	MAKE_BASE	SMC_GPU_THRMTRIP 46
40	GND	MAKE_BASE	
40	GND	MAKE_BASE	
40	GND	MAKE_BASE	
40	GND	MAKE_BASE	
40	GND	MAKE_BASE	
40	GND	MAKE_BASE	
40	GND	MAKE_BASE	
40	GND	MAKE_BASE	

42 SOC_VDDSOC_SENSE — P3MM SM — PP4800
77 42 SOC_VDDCPU_SENSE — P3MM SM — PP4801
87 86 85 84 83 SSD0_OCARINA_WP_L — P5MM-SP SM-SP — PP4802
92 91 90 89 88 SSD1_OCARINA_WP_L — P5MM-SP SM-SP — PP4803
69 46 39 SMC_PROCHOT_L — P3MM SM — PP4808

126 39 OUT SWD_SOC_SWCLK — MAKE_BASE=TRUE — SWD_SOC_SWCLK — IN 29
126 39 BI SWD_SOC_SWDIO — MAKE_BASE=TRUE — SWD_SOC_SWDIO — BI 29
INT PU SOC 50k

77 68 IN CHGR_INT_L — PLACE_SIDE=BOTTOM — SM P2MM — PP4809

82 40 IN MIPI_FTCAM_DATA_P<0> — PLACE_NEAR=U3900.B27:10MM — SM P2MM — PP4804
82 40 IN MIPI_FTCAM_DATA_N<0> — PLACE_NEAR=U3900.A26:10MM — SM P2MM — PP4805
82 40 IN MIPI_FTCAM_CLK_P — PLACE_NEAR=U3900.B26:10MM — SM P2MM — PP4806
82 40 IN MIPI_FTCAM_CLK_N — PLACE_NEAR=U3900.A26:10MM — SM P2MM — PP4807

PP1V8_SLPS2R 38 80
PP1V8_AWAKE 41 46 80

R4883	47K	5%	1/20W	MF	201	SSD0_CLKREQ0_L		41 83
R4884	47K	5%	1/20W	MF	201	SSD0_CLKREQ1_L		41 84
R4887	47K	5%	1/20W	MF	201	SSD0_CLKREQ2_L		41 85 121
R4888	47K	5%	1/20W	MF	201	SSD0_CLKREQ3_L		41 86 121
R4889	47K	5%	1/20W	MF	201	SSD1_CLKREQ0_L	S4E_X4PLUS	41 88
R4890	47K	5%	1/20W	MF	201	SSD1_CLKREQ1_L	S4E_X4PLUS	41 89
R4891	47K	5%	1/20W	MF	201	SSD1_CLKREQ2_L	S4E_X4PLUS	41 90
R4892	47K	5%	1/20W	MF	201	SSD1_CLKREQ3_L	S4E_X4PLUS	41 91
R4895	100K	5%	1/20W	MF	201	SSD_PMU_RESET_L		38 87 92 119
R4885	100K	5%	1/20W	MF	201	SSD0_PCIE_RESET_L		41 83 84 85 86
R4886	47K	5%	1/20W	MF	201	SSD0_CLK24M	S4E_X4PLUS	47 83 85
R4893	100K	5%	1/20W	MF	201	SSD1_PCIE_RESET_L	S4E_X4PLUS	41 88 89 90 91
R4894	47K	5%	1/20W	MF	201	SSD1_CLK24M	S4E_X4PLUS	47 88 90
R4870	0	5%	1/20W	MF	0201	I2S_SPKRAMP_R_D2R		40

BOM GROUP	BOM OPTIONS
Proto 0	
Proto 1	
Proto 2	
Pre-EVT	
EVT	
DVT	
PVT	
BOARD_REV:111	BOARDREV2,BOARDREV1,BOARDREV0
BOARD_REV:110	BOARDREV2,BOARDREV1
BOARD_REV:101	BOARDREV2,BOARDREV0
BOARD_REV:100	BOARDREV2
BOARD_REV:011	BOARDREV1,BOARDREV0
BOARD_REV:010	BOARDREV1
BOARD_REV:001	BOARDREV0
BOARD_REV:000	

BOM_COST_GROUP=SOC

PAGE TITLE: SoC Project Support

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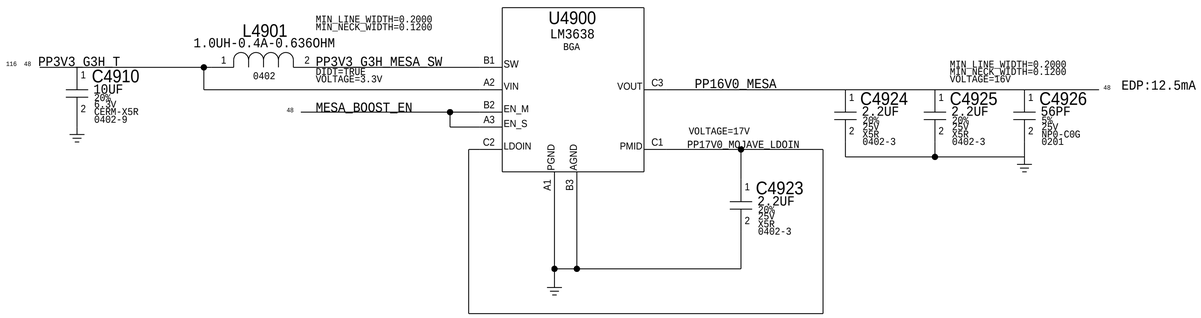
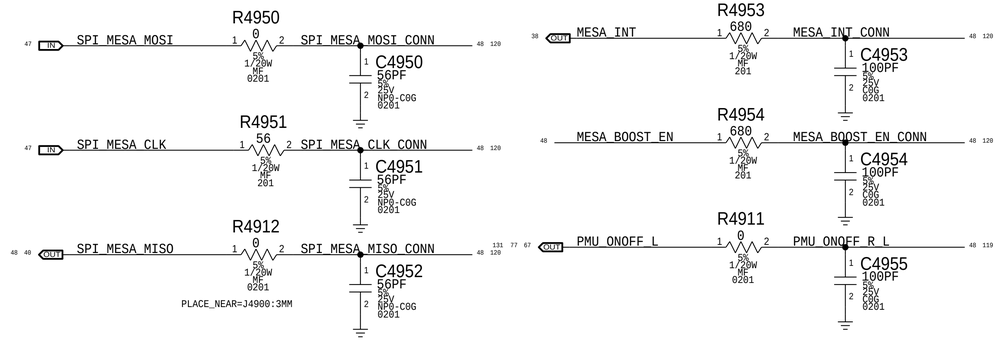
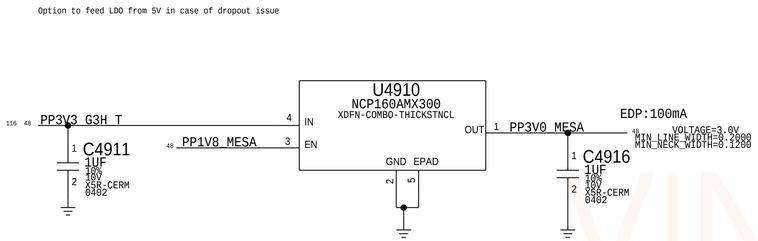
ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

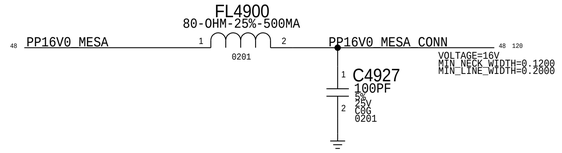
MOJAVE 16V BOOST





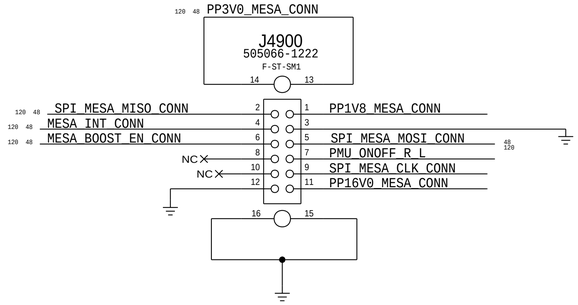
3.0V MESA





MESA FLEX CONNECTOR

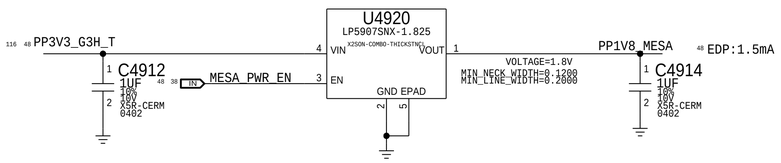
Proto1 Connector for X434/X435 Support
PLUG (516S00115) - X434/ X435 Jumper
Recptacle (516S00203) - X362/X363 MLB

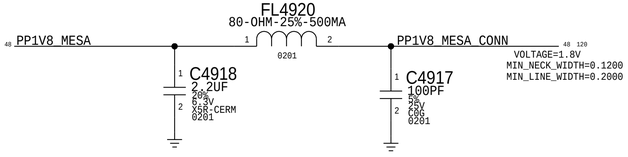


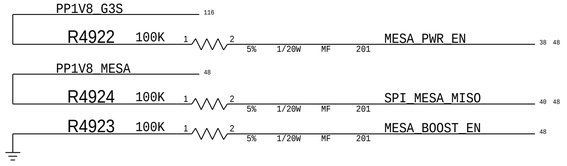
Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0

1.8V MESA







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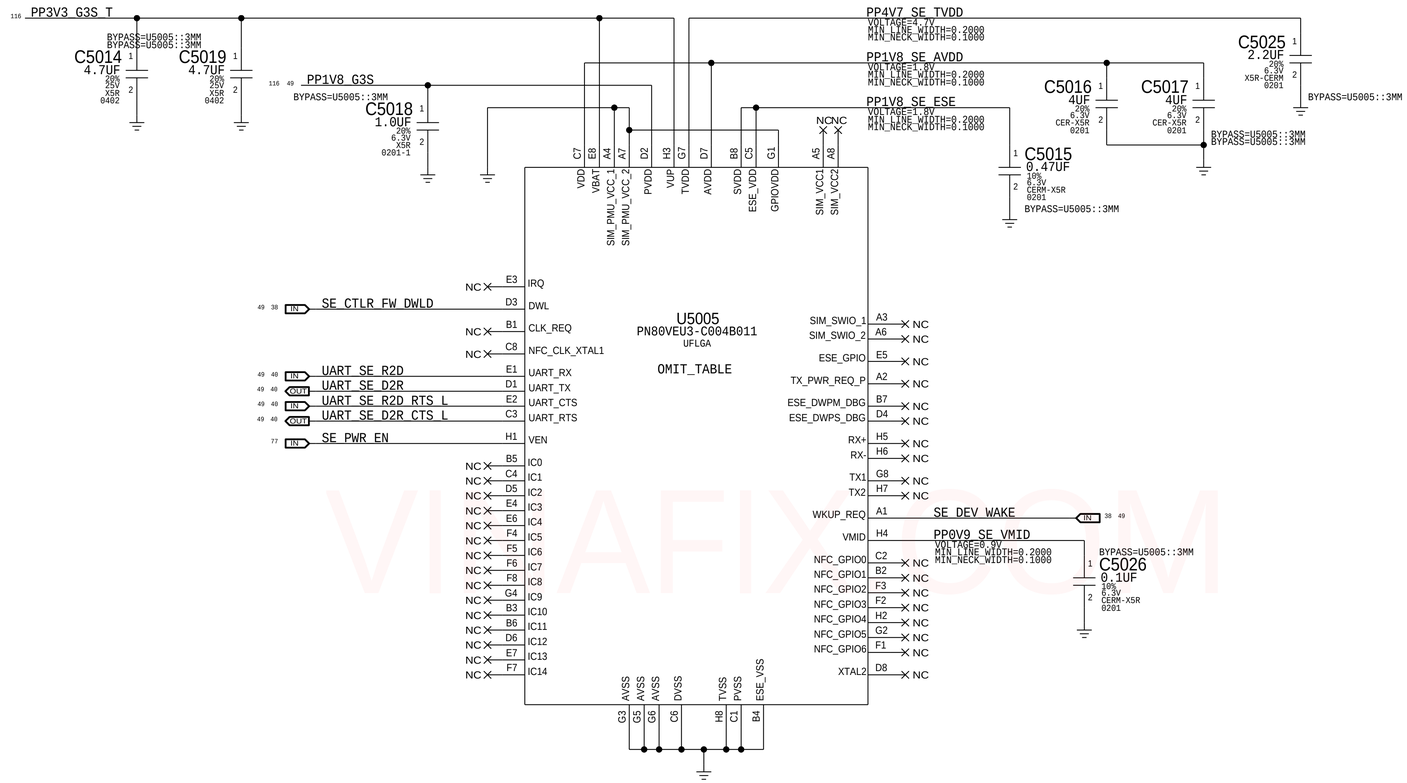
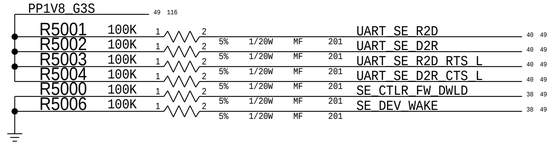


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-11132	1	IC,RTM4,ES2.1,PN80V,DEV,UFLGA64	U5005	CRITICAL	SE:DEV_2017
338S00253	1	IC,RTM4,ES2.1,PN80V,PRD,UFLGA64	U5005	CRITICAL	SE:PROD_2017



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SYNC_MASTER=SILU SYNC_DATE=05/05/2017

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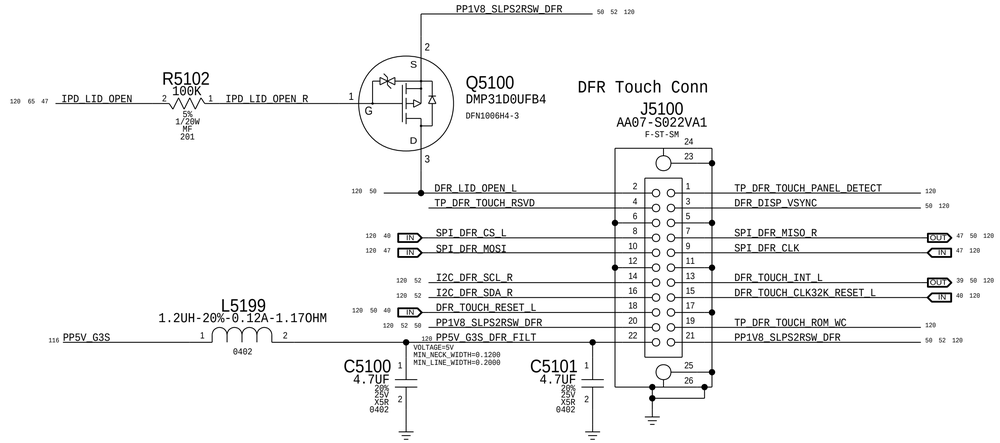
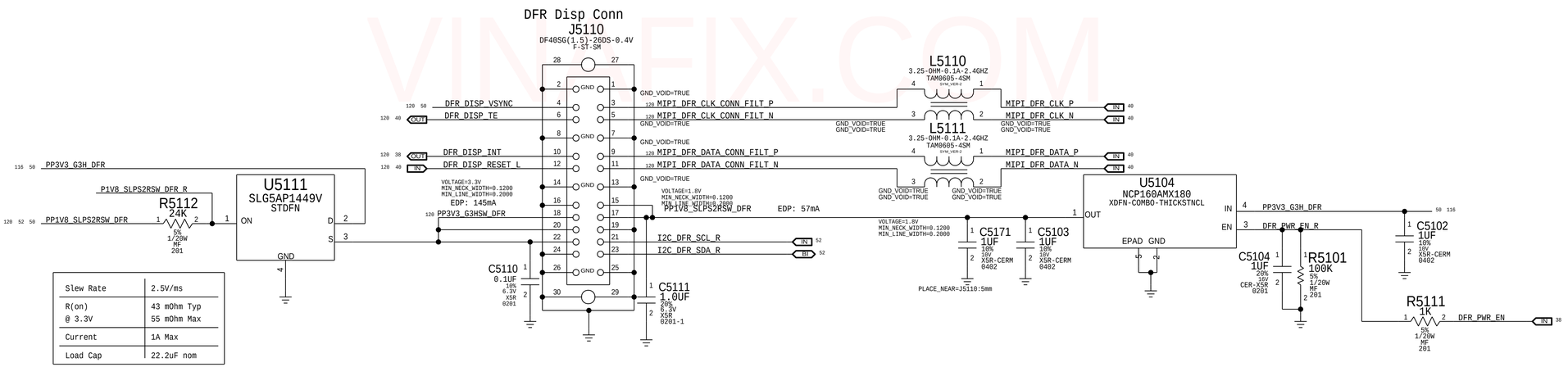
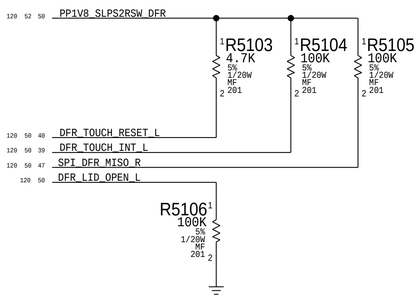
T208 Support





Slew Rate	2.5V/ms
R(on) @ 3.3V	43 mOhm Typ 55 mOhm Max
Current	1A Max
Load Cap	22.2uF nom



BOM_COST_GROUP=T151

PAGE TITLE: DFR & T208 Support

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D

REVISION: 4.0.0

BRANCH: evt-0

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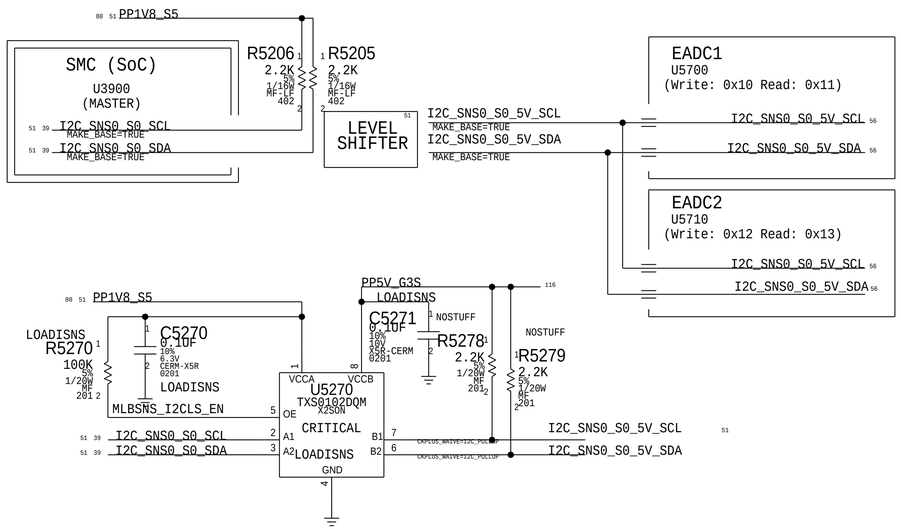
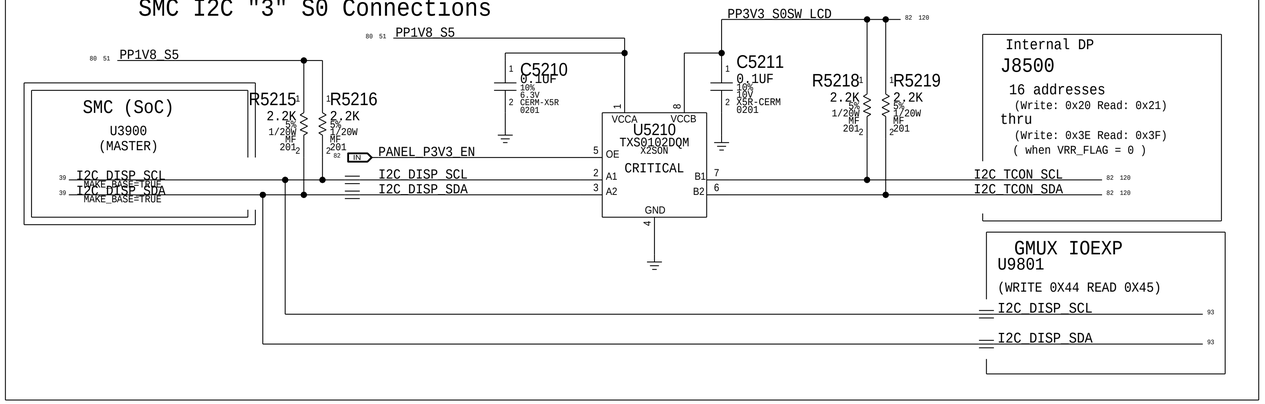
SMC I2C "1" S0 Connections

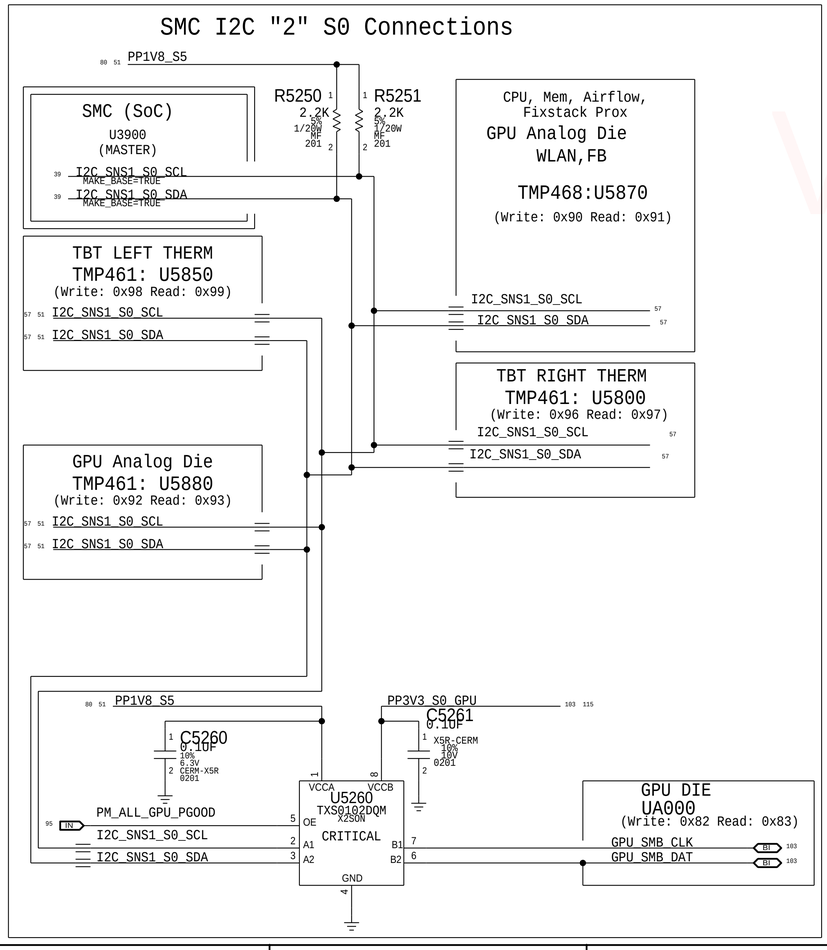


SMC I2C "3" S0 Connections

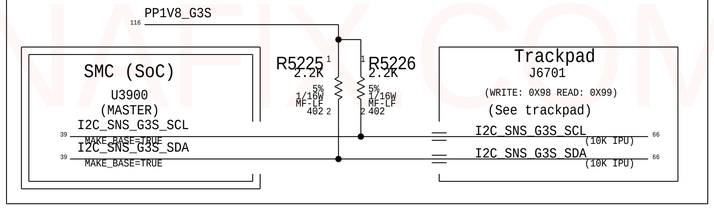


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0059	2	RES,2.2K,1/20W,0201,SMD,MF	R5230,R5231		OCARINA_I2C:2.2K

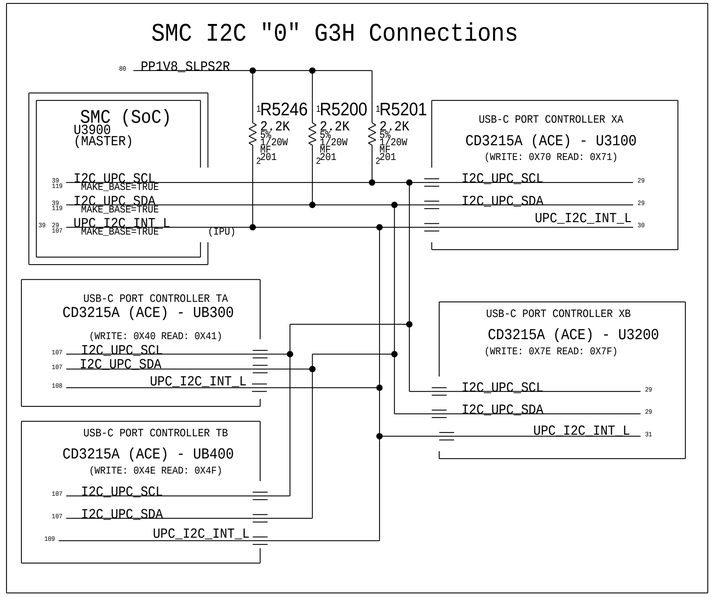
SMC I2C "2" S0 Connections



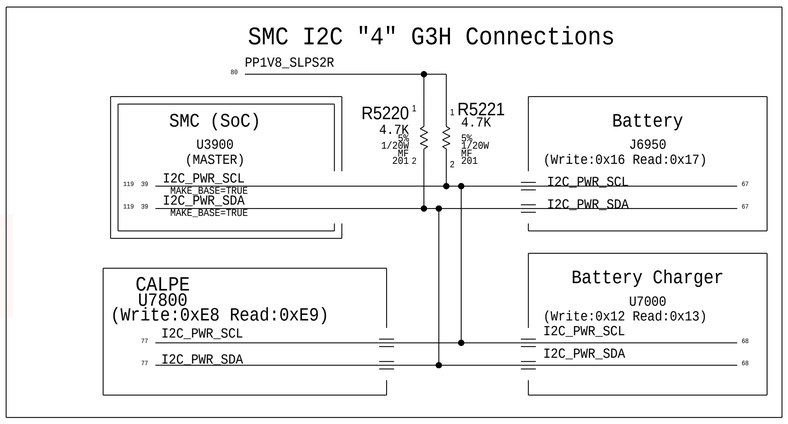
SMC I2C "5" G3S Connections



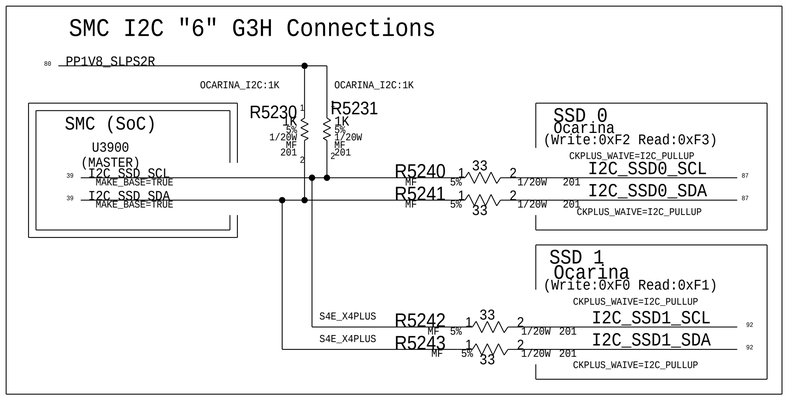
SMC I2C "0" G3H Connections



SMC I2C "4" G3H Connections



SMC I2C "6" G3H Connections



BOM_COST_GROUP=SMC

PAGE TITLE

I2C Connections 1

Apple Inc.

DRAWING NUMBER	051-02643
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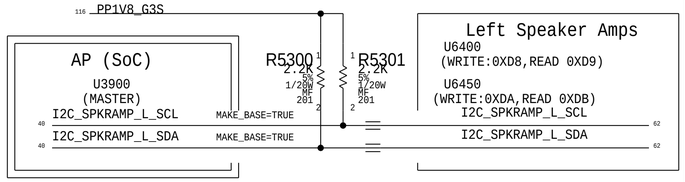
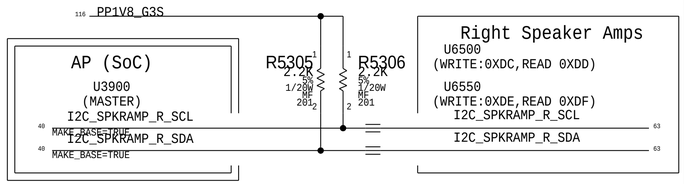
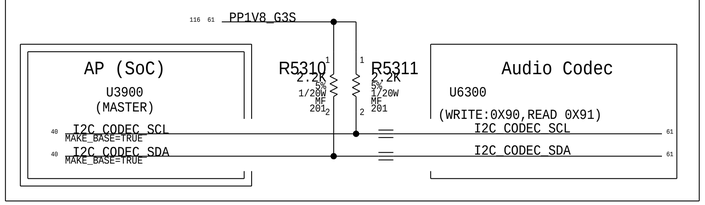
AP I2C "0" G3S Connections



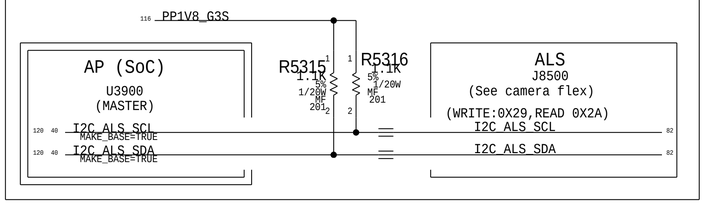
AP I2C "1" G3S Connections



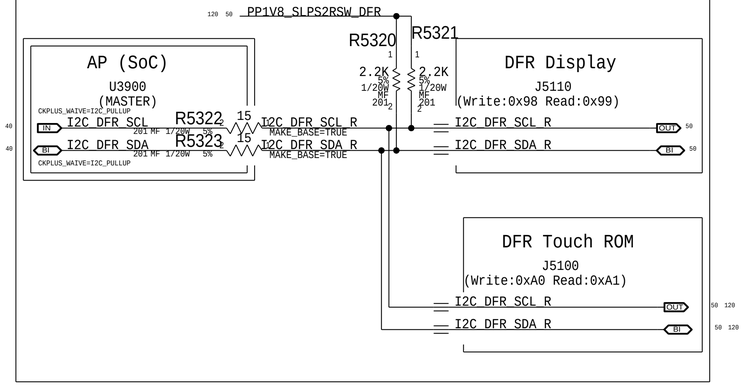
AP I2C "2" Codec Connections



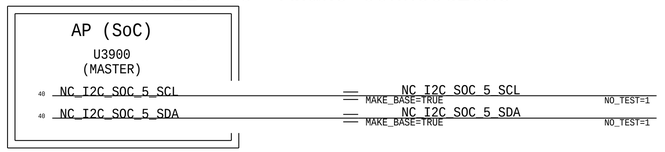
AP I2C "3" G3S Connections



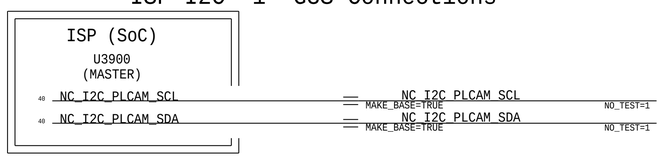
AP I2C "4" DFR Connections



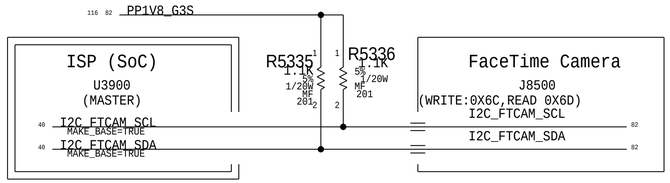
AP I2C "5" Awake Connections



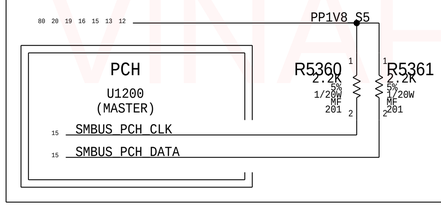
ISP I2C "1" G3S Connections



ISP I2C "0" G3S Connections



CNL-H uSFF SMBUS Connections



I2C Device Address

Device	SMC IF	ADDR. (8b)
ACE XA	I2C0	0X70/1
ACE XB	I2C0	0X7E/F
ACE TA	I2C0	0X40/1
ACE TB	I2C0	0X4E/F
EADC1	I2C1	0X10/1
EADC2	I2C1	0X12/3
Temp. Sensor Left	I2C2	0X98/9
Temp. Sensor Right	I2C2	0X96/7
CPU,MEM,WLAN Thermal	I2C2	0X90/1
GPU Analog Die Thermal	I2C2	0X92/3
GPU Digital Die Thermal	I2C2	0X82/3
TCON	I2C3	0X20-3F
GMUX IOEXP	I2C3	0X44/5
Charger	I2C4	0X12/3
Battery	I2C4	0X16/7
Calpe	I2C4	0XE8/9
Trackpad	I2C5	0X98/9
SSD0	I2C6	0XF2/3
SSD1	I2C6	0XF0/1
SoC IF		
Left Spkr Amp.(U6400)	I2C0	0XD8/9
Left Spkr Amp.(U6450)	I2C0	0XDA/B
Right Spkr Amp.(U6500)	I2C1	0XDC/D
Right Spkr Amp.(U6550)	I2C1	0XDE/F
Audio Codec	I2C2	0X90/1
ALS	I2C3	0X29/A
DFR Display	I2C4	0X98/9
DFR Touch	I2C4	0XA0/1
NC.	I2C5	
NC. Spkr ID1	I2C6_SDA	
Spkr ID0	I2C6_SCL	
ISP IF		
FT Camera	I2C0	0X6C/D
NC.	I2C1	
AOP IF		
NC.	I2C0	
PCH IF		
NC.	PULL-UP	

BOM_COST_GROUP=SMC

PAGE TITLE
I2C Connections 2

Apple Inc.

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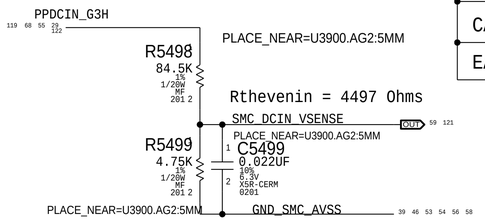
DC-IN Voltage Sense (VD0R)

Gain: 0.05322x
Vnominal: 20 V, Range: 23.49 V
SMC ADC: 00
Enables DC-In VSense
divider when AC present.
2.2KHz

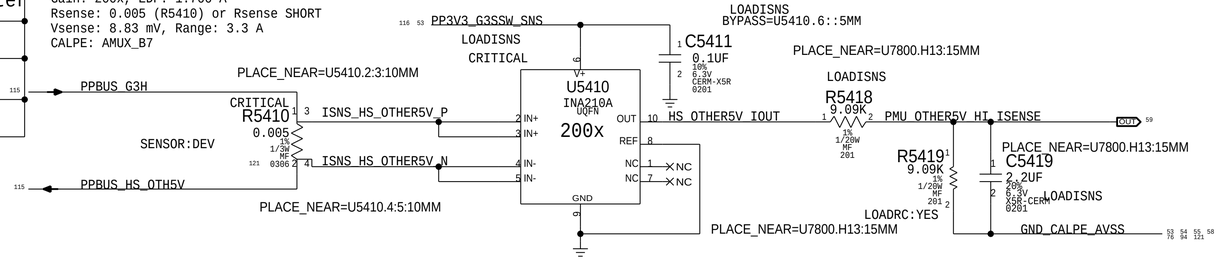


J680 SENSOR SETTINGS

CHIP	Vref(V)	Vmax	SMC sample Freq.	ADR RC filter
H9M	1.25	1.8	10khz	0.1ms
CALPE	1.5	5	100hz	10ms
EADC	2.5	5	1-2hz(10hz)	100ms

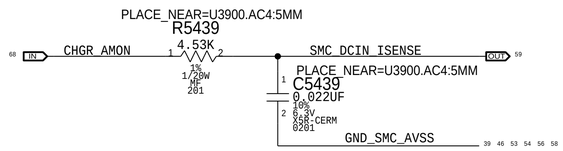
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.766 A
Rsense: 0.005 (R5410) or Rsense SHORT
Vsense: 8.83 mV, Range: 3.3 A
CALPE: AMUX_B7



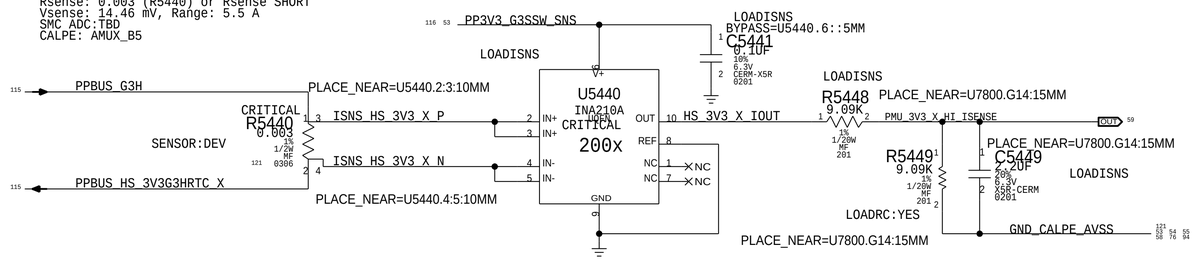
DC-IN Current Sense (ID0R)

DISCharger Gain: 20x, EDP: 4.6 A
Rsense: 0.010 (R7020)
SMC ADC: 01



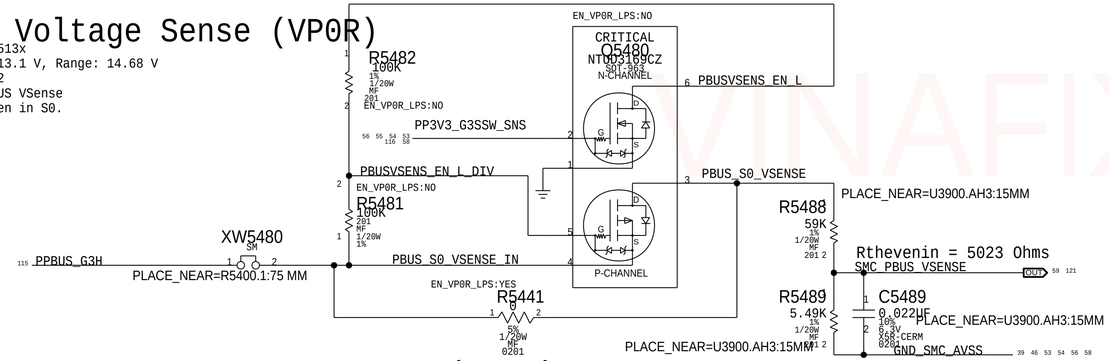
LEFT SIDE 3.3V High Side Current Sense (IOLR)

Gain: 200x, EDP: 4.82 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 14.46 mV, Range: 5.5 A
SMC ADC:TBD
CALPE: AMUX_B5



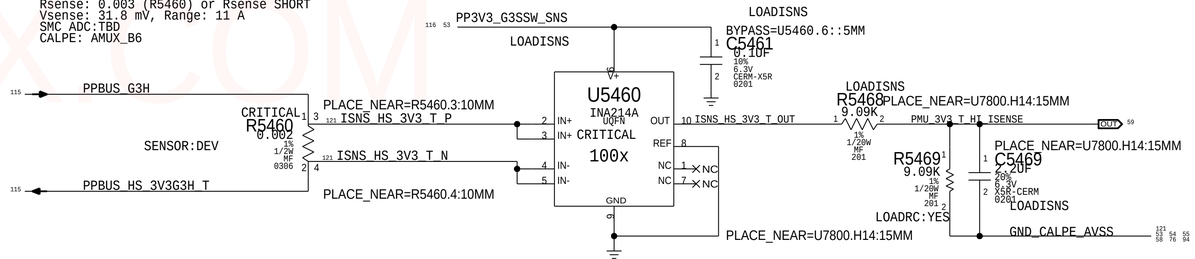
PBUS Voltage Sense (VP0R)

Gain: 0.08513x
Vnominal: 13.1 V, Range: 14.68 V
SMC ADC: 02
Enables PBUS VSense
divider when in S0.



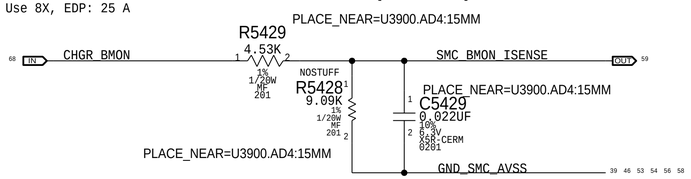
RIGHT SIDE 3.3V High Side Current Sense (IORR)

Gain: 100x, EDP: 10.6 A
Rsense: 0.003 (R5460) or Rsense SHORT
Vsense: 31.8 mV, Range: 11 A
SMC ADC:TBD
CALPE: AMUX_B6



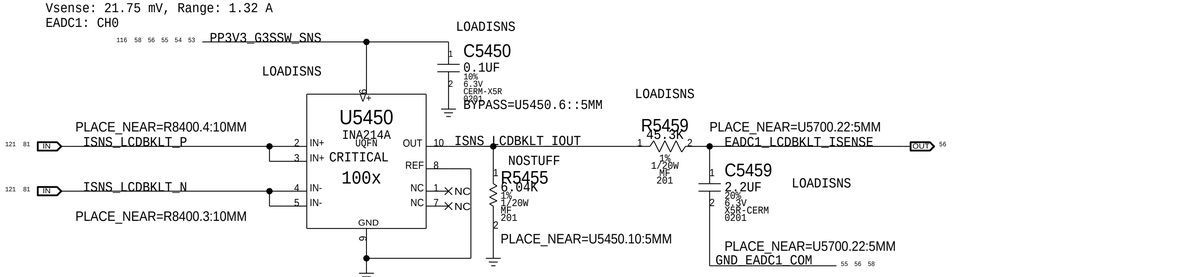
Discharger BMON Current Sense (IPBR)

Charger Gain: 8X OR 64x, Use 8X, EDP: 25 A
Rsense: 0.005 (R7060)
SMC ADC: 03



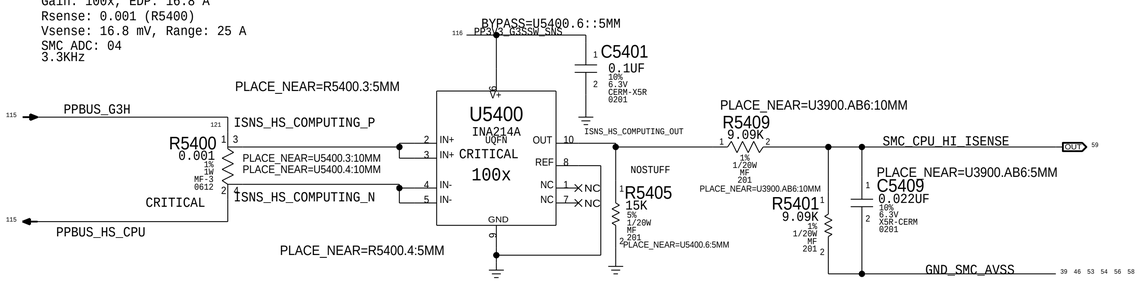
LCD Backlight Current Sense (IBLR)

Gain: 100x. EDP: 0.87 A
Rsense: 0.025 (R8400)
Vsense: 21.75 mV, Range: 1.32 A
EADC1: CH0



CPU High Side Curent Sense (IC0R)

Gain: 100x, EDP: 16.8 A
Rsense: 0.001 (R5400)
Vsense: 16.8 mV, Range: 25 A
SMC ADC: 04
3.3KHz



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	3	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5449,R5469,R5419		LOADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE
Power Sensors High Side

Apple Inc.

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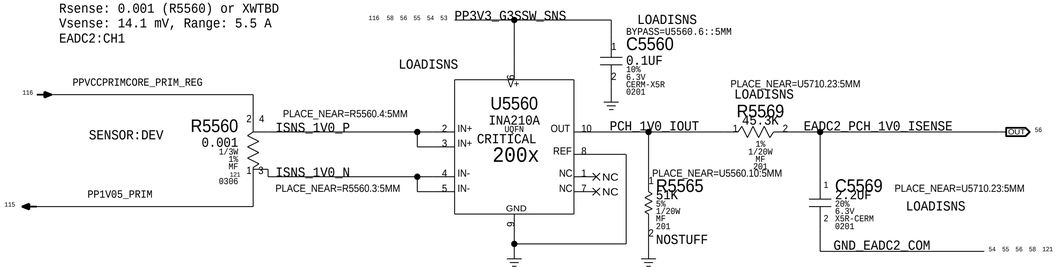
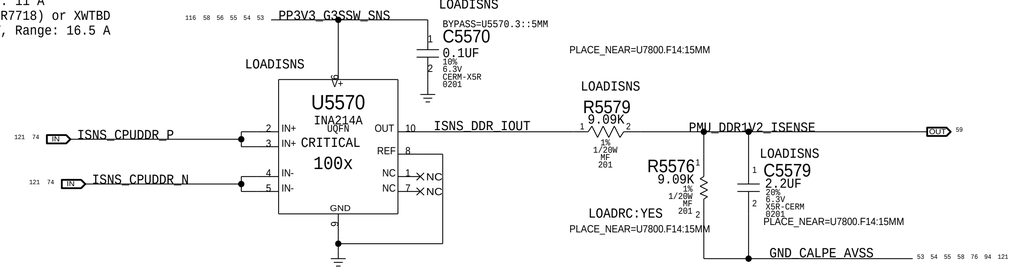
PCH 1.0V Current Sense (IS1C)

Gain: 200x, EDP: 4.7 A
Rsense: 0.001 (R5560) or XWTBD
Vsense: 14.1 mV, Range: 5.5 A
EADC2:CH1



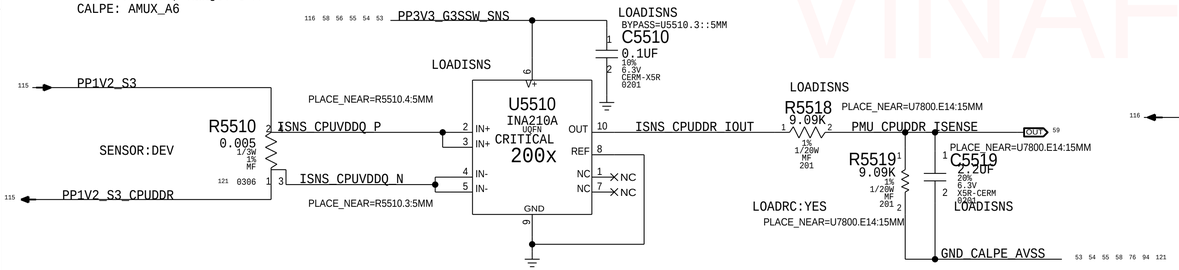
DDR4 1.2V Current Sense (IM0C)

Gain: 100x, EDP: 11 A
Rsense: 0.002 (R7718) or XWTBD
Vsense: 22.2 mV, Range: 16.5 A
CALPE: AMUX_A7



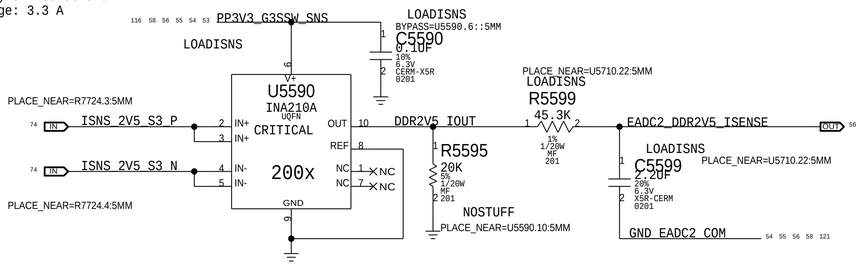
CPUDDR 1.2V Curent Sense (IMCC)

Gain: 200x, EDP: 2.8 A
Rsense: 0.005 (R5510)
Vsense: 14 mV, Range: 3 A
CALPE: AMUX_A6



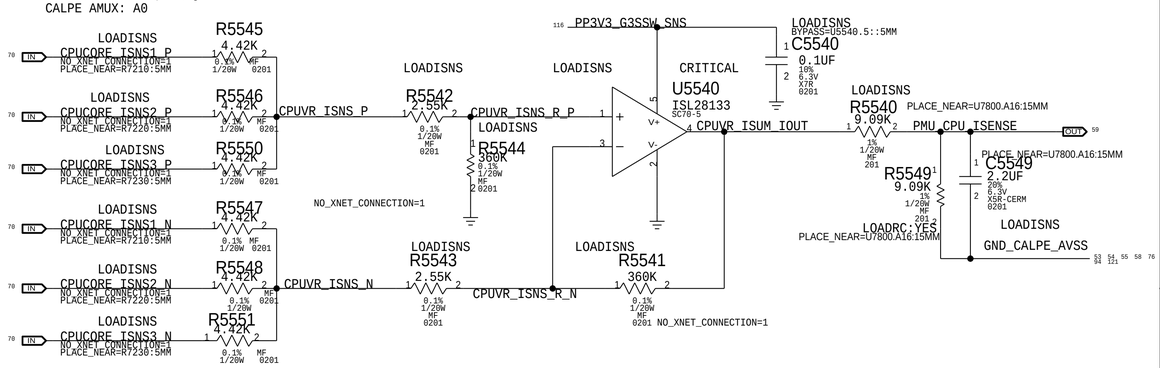
2.5V Current Sense (IM1C)

Gain: 200x, EDP: 2.24 A
Rsense: 0.005 (R7724) or Rsense SHORT
Vsense: 11.2 mV, Range: 3.3 A
EADC2: CH0



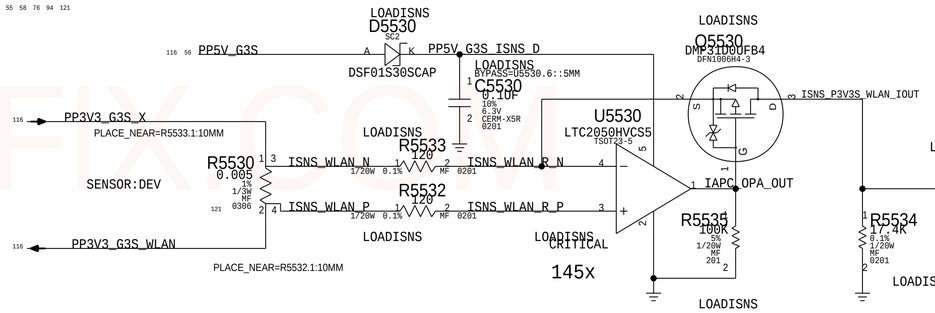
CPU Core Curent Sense (ICAC)

Gain: 89.48x, EDP: 128 A
Rsense: 3x of 0.00075
R7210,R7220,R7230),Rsum: 0.00025
Vsense:16.75 mV, Range: 134.11 A
CALPE AMUX: A0



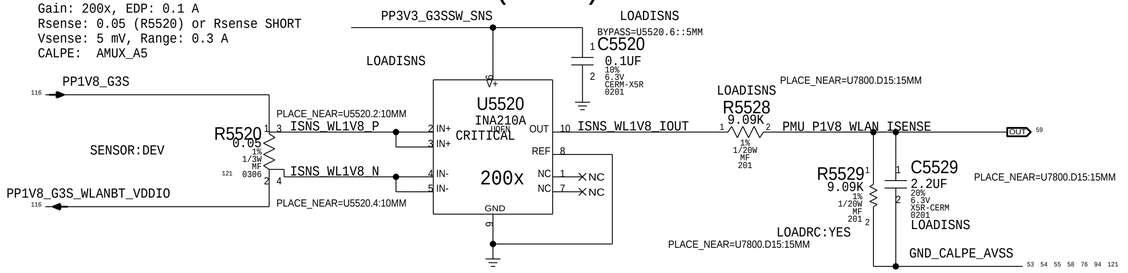
WLANBT 3V3 Current Sense (IAPC)

Gain: 200x, EDP: 1.5 A
Rsense: 0.005 (R5530) or Rsense SHORT
Vsense: 7.5 mV, Range: 1.72 A
SMC: ADC 06



WLANBT 1V8 Current Sense (IA8C)

Gain: 200x, EDP: 0.1 A
Rsense: 0.05 (R5520) or Rsense SHORT
Vsense: 5 mV, Range: 0.3 A
CALPE: AMUX_A5



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5576,R5519,R5549,C5539,R5529		LOADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors Load Side

Apple Inc.

DRAWING NUMBER: 051-02643
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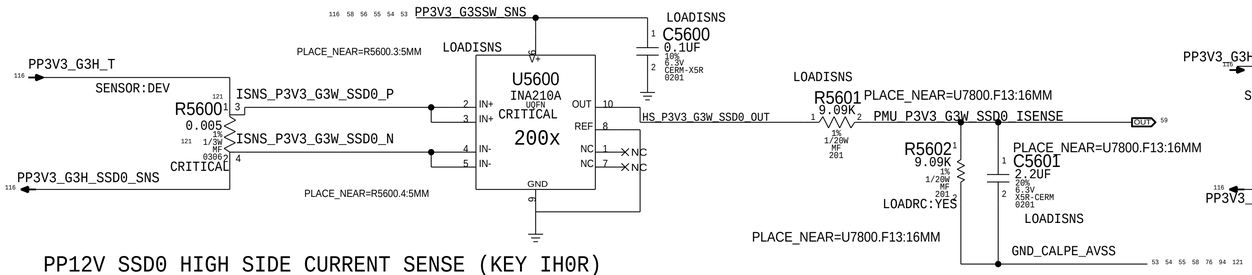
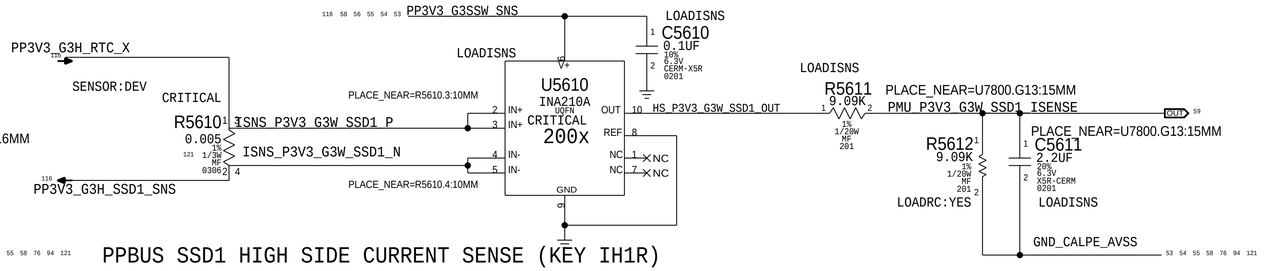
PP3V3_G3W_SSD0 HIGH SIDE CURRENT SENSE (KEY IH0C)

GAIN: 200X, EDP: 1.48 A
RSENSE: 0.005 (RK710) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B3



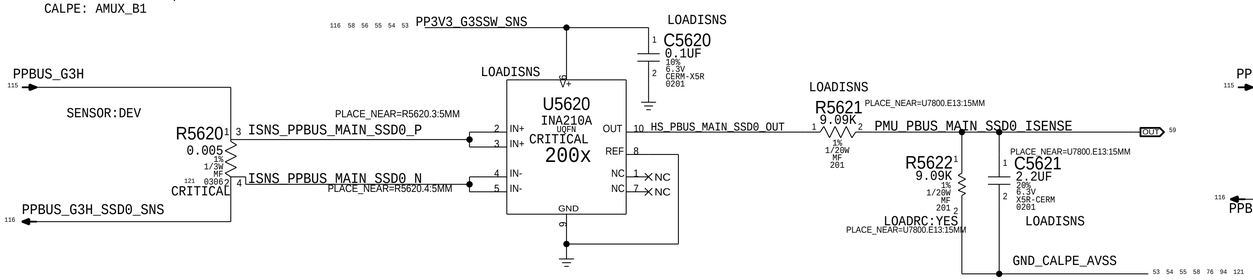
PP3V3_G3W_SSD1 HIGH SIDE CURRENT SENSE (KEY IH1C)

GAIN: 200X, EDP: 1.48 A
RSENSE: 0.005 (RK760) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B4



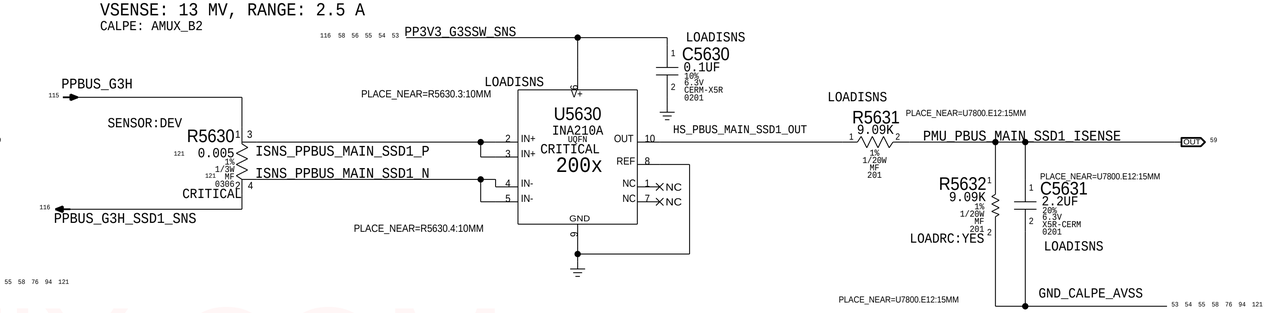
PP12V SSD0 HIGH SIDE CURRENT SENSE (KEY IH0R)

GAIN: 200X, EDP: 0.5 A
RSENSE: 0.005 (RK610) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B1



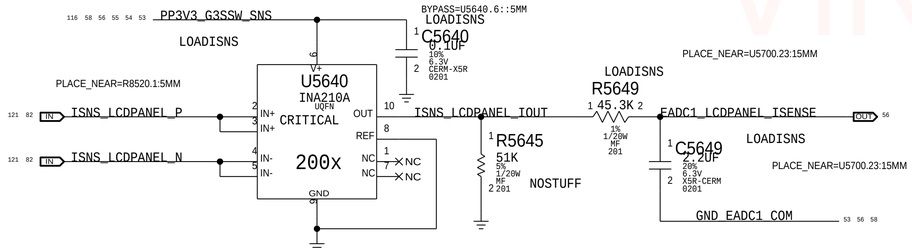
PPBUS SSD1 HIGH SIDE CURRENT SENSE (KEY IH1R)

GAIN: 200X, EDP: 0.5 A
RSENSE: 0.005 (R5607) OR RSENSE SHORT
VSENSE: 13 MV, RANGE: 2.5 A
CALPE: AMUX_B2



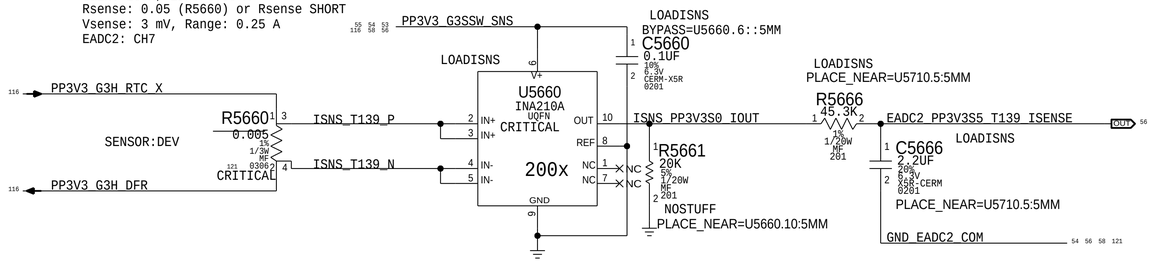
LCD Panel Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC1: CH1



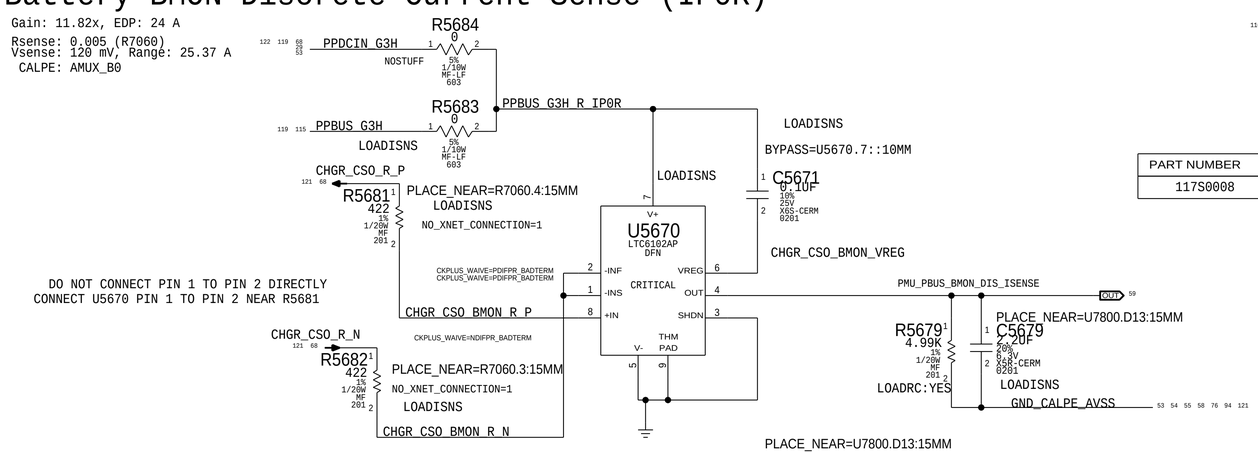
T139 Current Sense (IF3C)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5660) or Rsense SHORT
Vsense: 3 mV, Range: 0.25 A
EADC2: CH7



Battery BMON Discrete Current Sense (IP0R)

Gain: 11.82x, EDP: 24 A
Rsense: 0.005 (R7060)
Vsense: 120 mV, Range: 25.37 A
CALPE: AMUX_B0



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5602,R5612,R5622,R5632,R5679		LOADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors Extended 1

Apple Inc.

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REVISION: 4.0.0
BRANCH: evt-0
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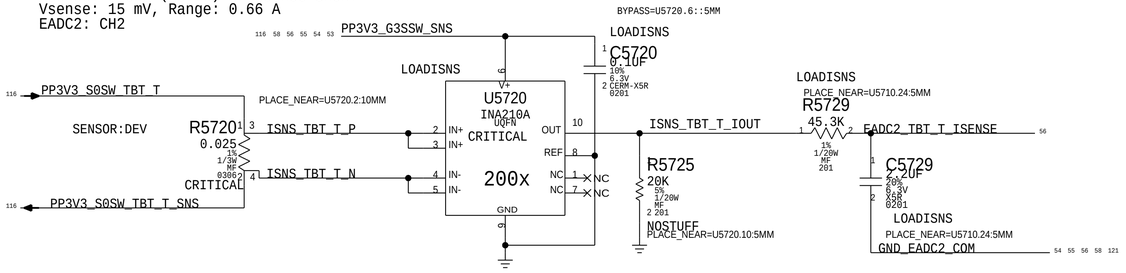
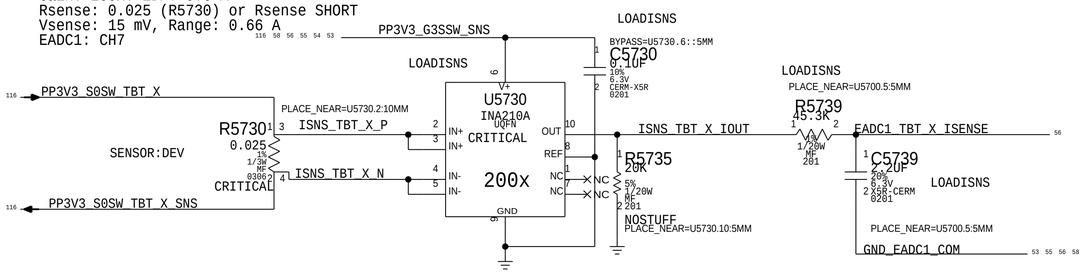
Thunderbolt TBT RIGHT Current Sense (IURC)

Gain: 200x. EDP: 0.6 A
Rsense: 0.025 (R5720) or Rsense SHORT
Vsense: 15 mV, Range: 0.66 A
EADC2: CH2



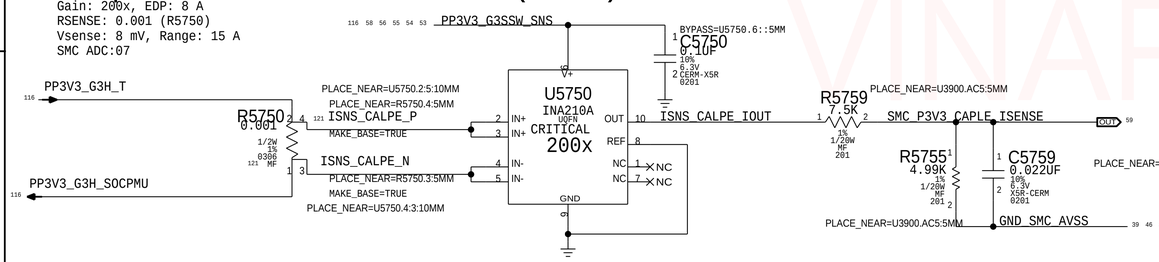
Thunderbolt TBT LEFT Current Sense (IULC)

Gain: 200x. EDP: 0.6 A
Rsense: 0.025 (R5730) or Rsense SHORT
Vsense: 15 mV, Range: 0.66 A
EADC1: CH7

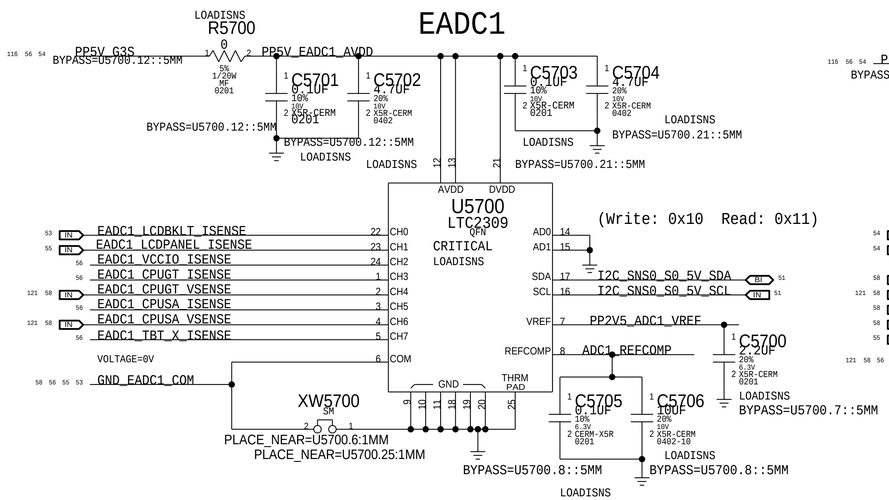


Calpe 3V3 Current Sense (ISLC)

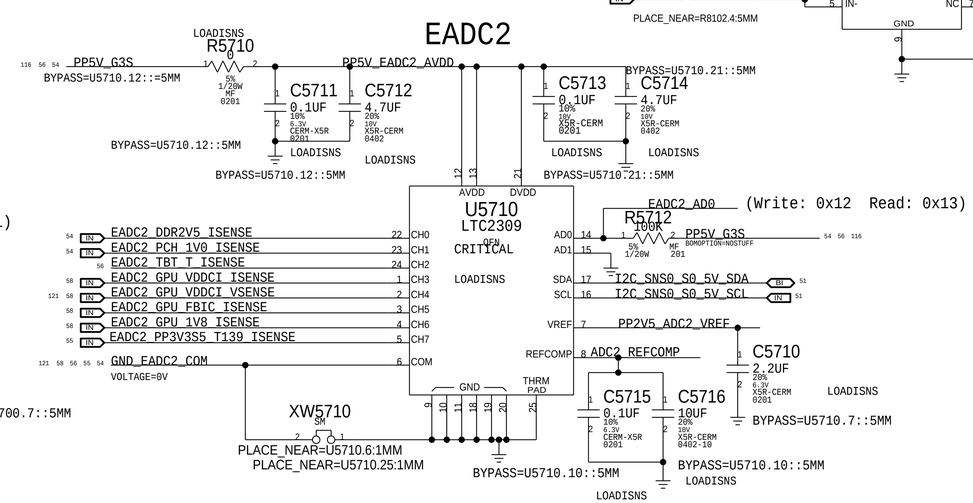
Gain: 200x, EDP: 8 A
RSENSE: 0.001 (R5750)
Vsense: 8 mV, Range: 15 A
SMC ADC:07



EADC1

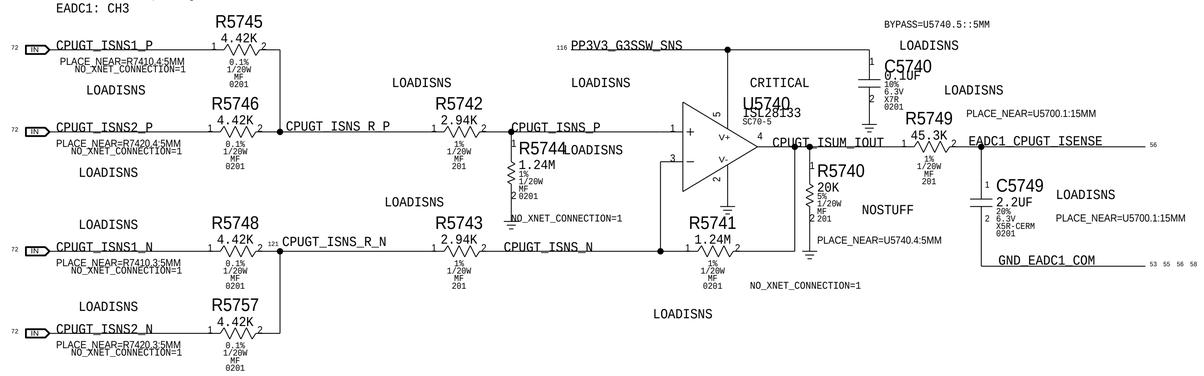


EADC2



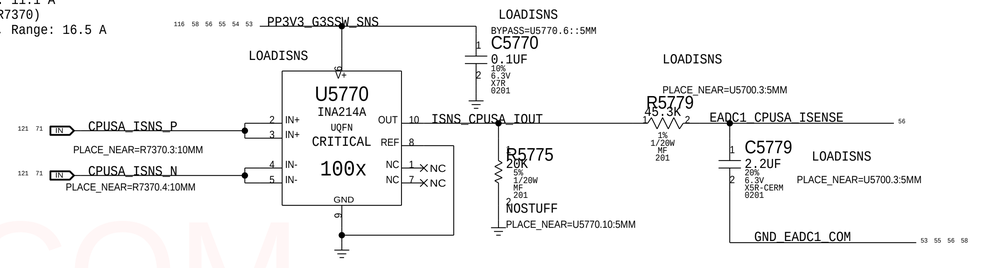
CPU GT Current Sense (ICTC)

Gain: 240.78x, EDP: 32 A
Rsense: 2x of 0.00075 (R7410, R7420), Rsum: 0.000375
Vsense: 12 mV, Range:36.55 A
EADC1: CH3



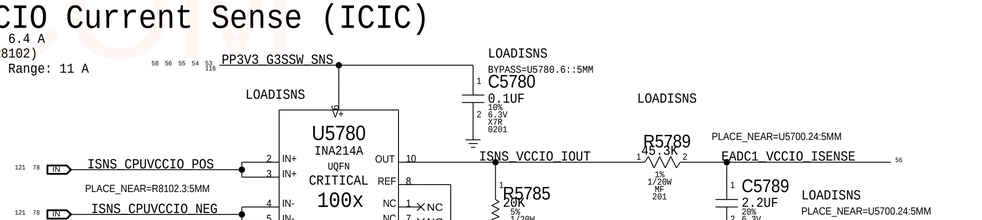
CPU SA Current Sense (ICSC)

Gain: 100x, EDP: 11.1 A
Rsense: 0.002 (R7370)
Vsense: 22.2 mV, Range: 16.5 A
EADC1: CH5



CPU VCCIO Current Sense (ICIC)

Gain: 100x, EDP: 6.4 A
Rsense: 0.003 (R8102)
Vsense: 19.2 mV, Range: 11 A
EADC1: CH2



BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors Extended 2

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BRANCH	evt-0
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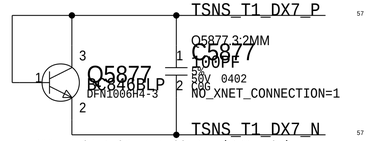
THERMAL DIODE: VRAM PROXIMITY (KEY)

Place Q5877 Bottom,underVRAM shiled can, but not within 2mm of any IC



THERMAL DIODE: GPU ANALOG DIE (KEY TA0P)

Connect GPU Analog Die to U5870 channel 8

GPU Digital DIE TG0D:

U5880 I2C Address:TMP461 A0->Floating A1->GND 0X92/0X93

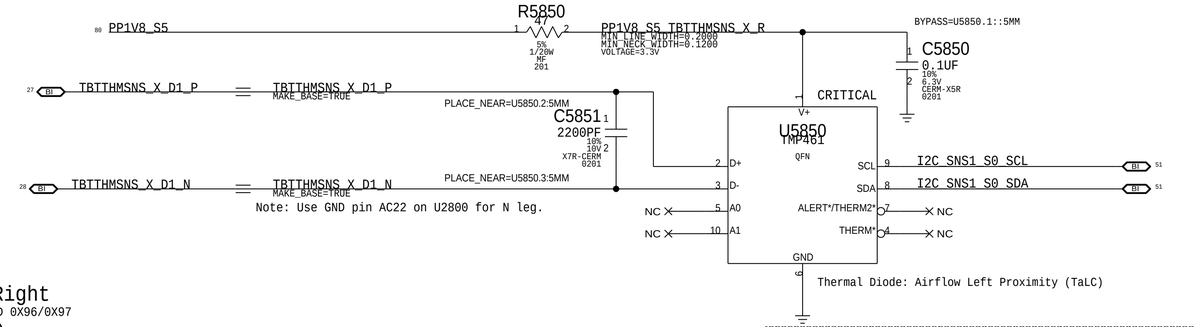
Thermal Sensor A:

Thunderbolt Die, Airflow Left

U5850 I2C Address:TMP461 A1->Floating A0->Floating 0X98/0X99

Thermal Diode: TBT Die (TTLD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Note: Use GND pin AC22 on U2800 for N leg.

Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

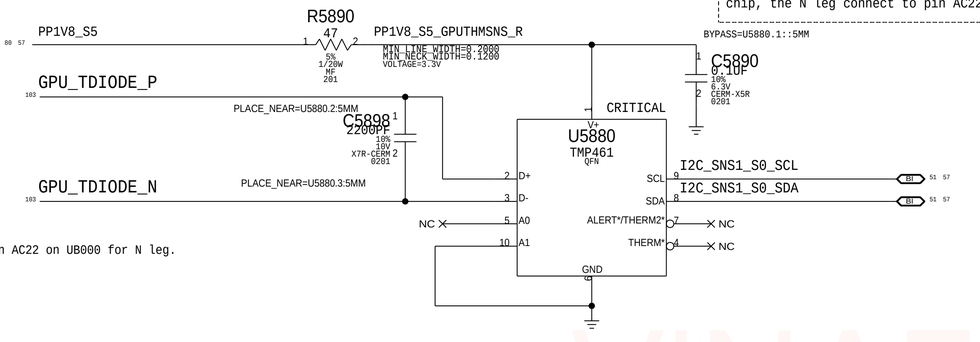
Thermal Sensor C:

Thunderbolt Die, Air Flow Right

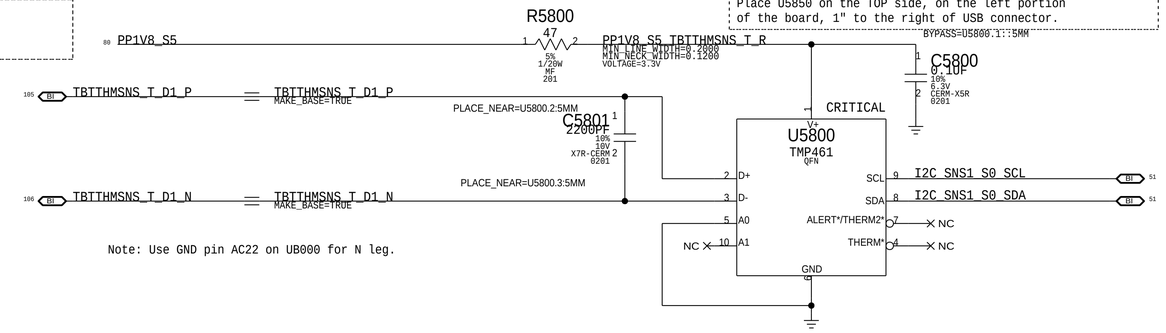
U5800 I2C Address:TMP461 A1->Floating A0->GND 0X96/0X97

Thermal Diode: TBT Die (TTRD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



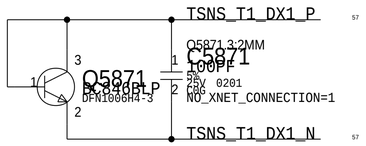
Note: Use GND pin AC22 on UB000 for N leg.



Note: Use GND pin AC22 on UB000 for N leg.

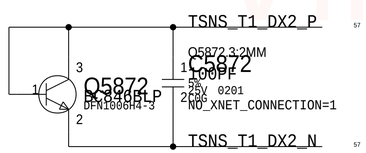
THERMAL DIODE: CPU PROX (KEY TC0P)

Placement Note:
Place Q5871 under the CPU ON BOTTOM SIDE



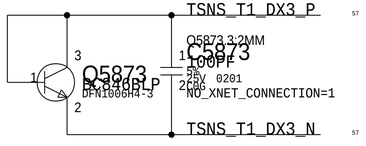
THERMAL DIODE: FIN STACK LEFT (KEY TH2H)

Placement Note:
Place Q5872,AIRFLOW THERMAL INDICATOR,ABOVETHE X100, ON THE TOP SIDE



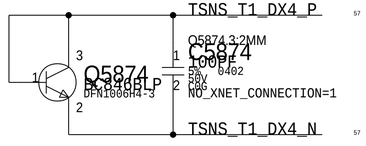
THERMAL DIODE: FIN STACK RIGHT (KEY TH1H)

Placement Note:
Place Q5873 AT THE CORNER NEAR RIGHT FAN, ON THE TOP SIDE



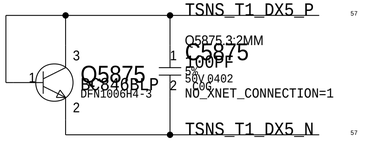
THERMAL DIODE: Memory Proximity (KEY TM0P)

Place Q5874 between two rows of Memory devices, between channel A and CHANNEHL b PN BOTTOM SIDES



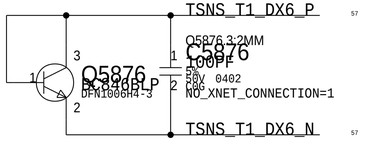
THERMAL DIODE: X100 PROXIMITY (KEY TW0P)

Place Q5875 near X100 on bottom



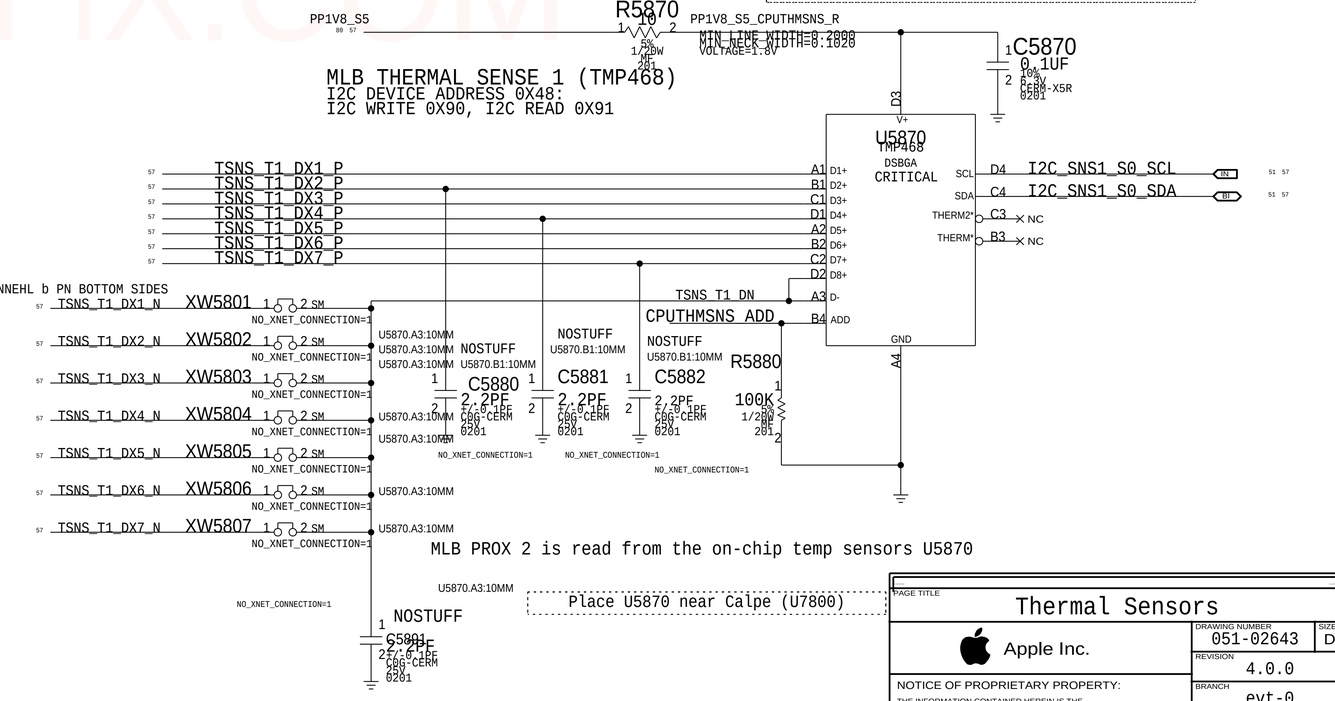
THERMAL DIODE: GPU PROXIMITY(KEY)

Place Q5876 near GPU, Top side



Thermal Diode: Airflow Right Proximity (TaRC)

Placement Note:
Place U5800 on the TOP side, on the left portion of the board, 1" to the right of USB connector.



BOM_COST_GROUP=SENSORS

PAGE TITLE: Thermal Sensors

Apple Inc.

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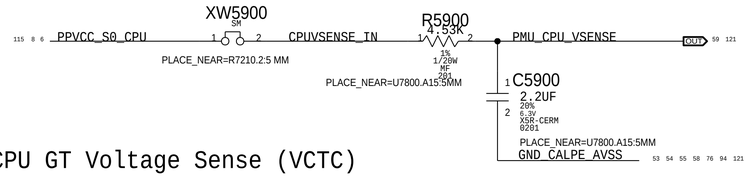
GPU SENSORS

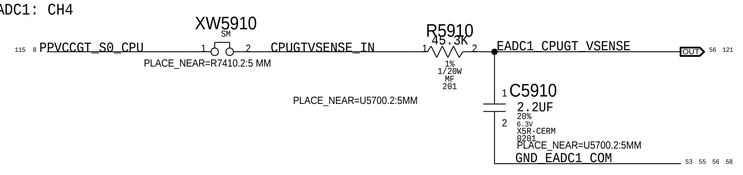
CPU Core Voltage Sense (VCAC)

CALPE : AMUX-A1



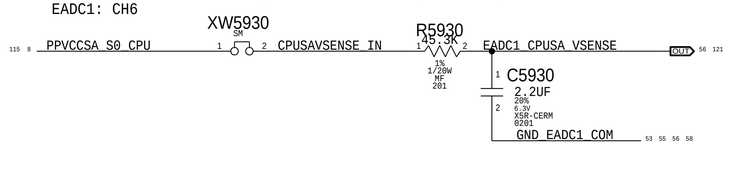
CPU GT Voltage Sense (VCTC)

EADC1: CH4



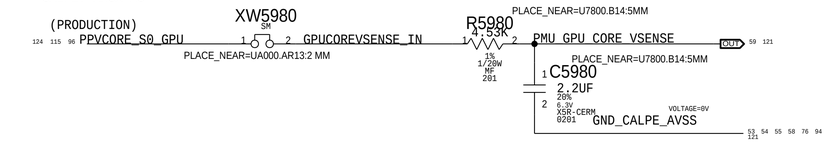
CPU SA Voltage Sense (VCSC)

EADC1: CH6



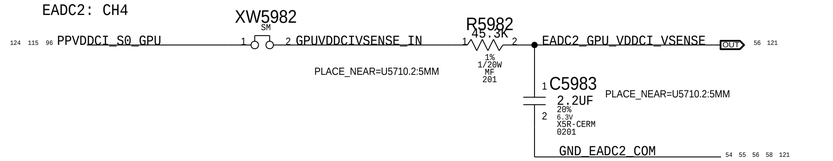
GPU CORE Voltage Sense (VG0C)

CALPE: AMUX-A3



GPU VDDCI Voltage Sense (VG2C)

EADC2: CH4



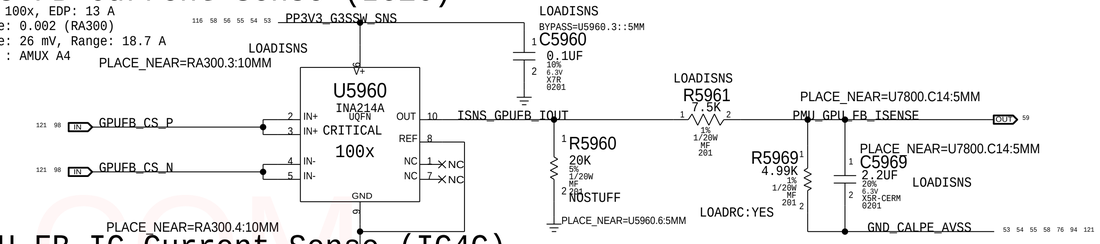
GPU CORE Current Sense (IG0C)

no longer lives on this page
it's merged with the PCC circuit
on CSA 99

Gain: 154.87x, EDP: 78 A
Rsense: 3X OF 0.00075 (RA651,RA641,RA346)
Vsense: 19.5 mV, Range: 109 A
CALPE : AMUX A2

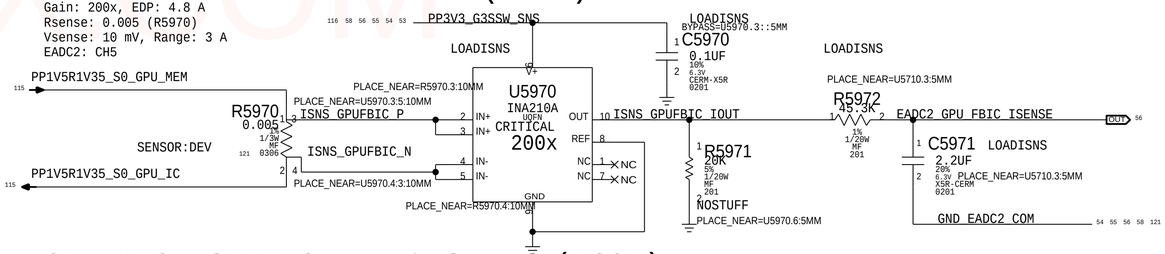
GPU FB Current Sense (IG1C)

Gain: 100x, EDP: 13 A
Rsense: 0.002 (RA300)
Vsense: 26 mV, Range: 18.7 A
CALPE : AMUX A4



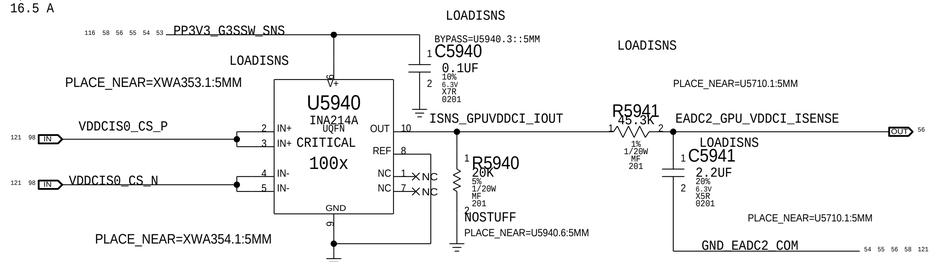
GPU FB IC Current Sense (IG4C)

Gain: 200x, EDP: 4.8 A
Rsense: 0.005 (R5970)
Vsense: 10 mV, Range: 3 A
EADC2: CH5



GPU VDDCI Current Sense (IG2C)

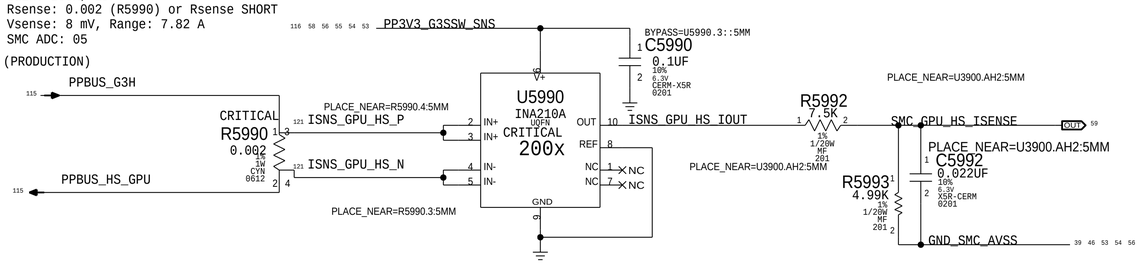
Gain: 100x, EDP: 10 A
Rsense: 0.003 (RA368)
Vsense: 20 mV, Range: 16.5 A
EADC2: CH3



GPU HIGH SIDE Current Sense (IG0R)

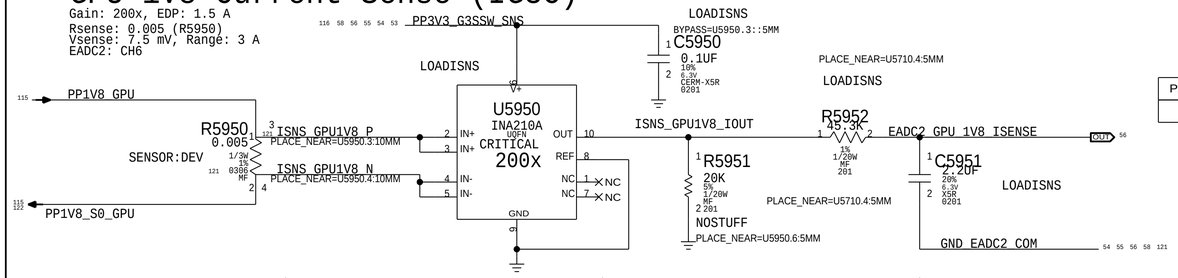
Gain: 200x, EDP: 4 A
Rsense: 0.002 (R5990) or Rsense SHORT
Vsense: 8 mV, Range: 7.82 A
SMC ADC: 05

(PRODUCTION)



GPU 1V8 Current Sense (IG3C)

Gain: 200x, EDP: 1.5 A
Rsense: 0.005 (R5950)
Vsense: 7.5 mV, Range: 3 A
EADC2: CH6



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R5969		LOADRC:NO

BOM_COST_GROUP=SENSORS

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Power Sensor Extended 3

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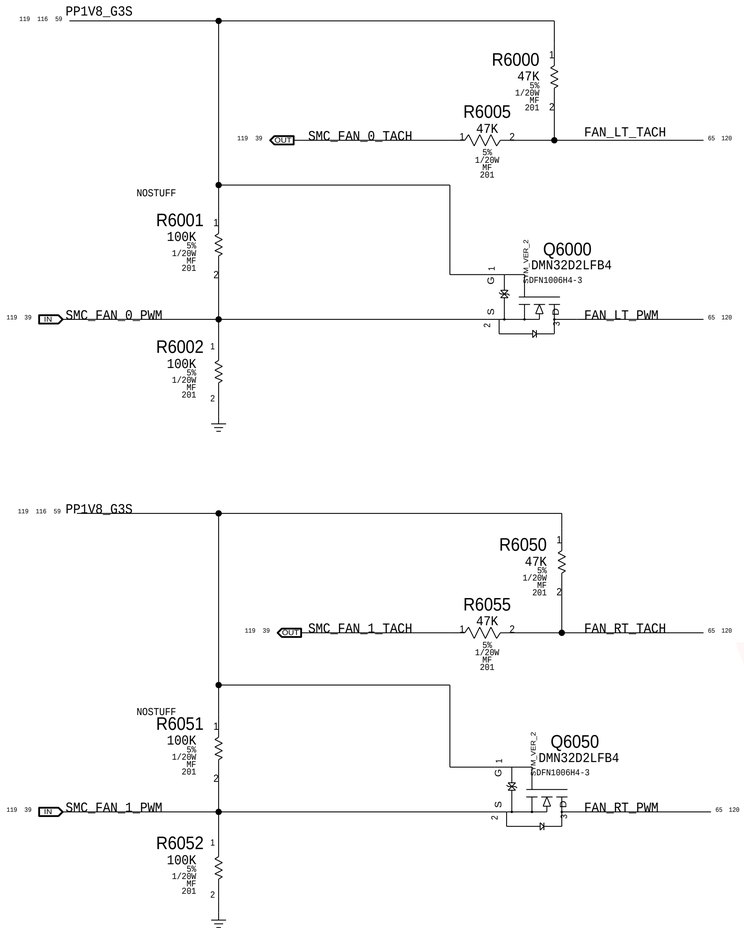
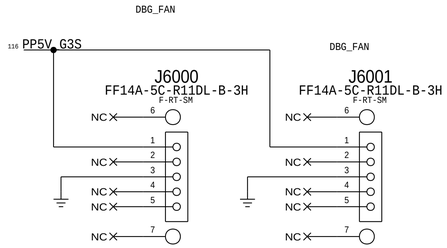
FAN CONNECTOR



DBG_FAN



H9M SMC ADC Assignments

SMC_DCIN_VSENSE	MAKE_BASE=TRUE	SMC_DCIN_VSENSE	
SMC_DCIN_ISENSE	MAKE_BASE=TRUE	SMC_DCIN_ISENSE	
SMC_PBUS_VSENSE	MAKE_BASE=TRUE	SMC_PBUS_VSENSE	
SMC_BMON_ISENSE	MAKE_BASE=TRUE	SMC_BMON_ISENSE	
SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	SMC_CPU_HI_ISENSE	
SMC_GPU_HS_ISENSE	MAKE_BASE=TRUE	SMC_GPU_HS_ISENSE	
SMC_P3V3_WLAN_ISENSE	MAKE_BASE=TRUE	SMC_P3V3_WLAN_ISENSE	
SMC_P3V3_CAPLE_ISENSE	MAKE_BASE=TRUE	SMC_P3V3_CAPLE_ISENSE	

CALPE AMUX Assignments

PMU_CPU_ISENSE	MAKE_BASE=TRUE	PMU_CPU_ISENSE	
PMU_CPU_VSENSE	MAKE_BASE=TRUE	PMU_CPU_VSENSE	
PMU_GPU_CORE_ISENSE	MAKE_BASE=TRUE	PMU_GPU_CORE_ISENSE	
PMU_GPU_CORE_VSENSE	MAKE_BASE=TRUE	PMU_GPU_CORE_VSENSE	
PMU_GPU_FB_ISENSE	MAKE_BASE=TRUE	PMU_GPU_FB_ISENSE	
PMU_P1V8_WLAN_ISENSE	MAKE_BASE=TRUE	PMU_P1V8_WLAN_ISENSE	
PMU_CPUDDR_ISENSE	MAKE_BASE=TRUE	PMU_CPUDDR_ISENSE	
PMU_DDR1V2_ISENSE	MAKE_BASE=TRUE	PMU_DDR1V2_ISENSE	

MAKE_BASE=TRUE

PMU_PBUS_BMON_DIS_ISENSE		PMU_PBUS_BMON_DIS_ISENSE	
PMU_PBUS_MAIN_SSD0_ISENSE	MAKE_BASE=TRUE	PMU_PBUS_MAIN_SSD0_ISENSE	
PMU_PBUS_MAIN_SSD1_ISENSE	MAKE_BASE=TRUE	PMU_PBUS_MAIN_SSD1_ISENSE	
PMU_P3V3_G3W_SSD0_ISENSE	MAKE_BASE=TRUE	PMU_P3V3_G3W_SSD0_ISENSE	
PMU_P3V3_G3W_SSD1_ISENSE	MAKE_BASE=TRUE	PMU_P3V3_G3W_SSD1_ISENSE	
PMU_3V3_X_HI_ISENSE	MAKE_BASE=TRUE	PMU_3V3_X_HI_ISENSE	
PMU_3V3_T_HI_ISENSE	MAKE_BASE=TRUE	PMU_3V3_T_HI_ISENSE	
PMU_OTHER5V_HI_ISENSE	MAKE_BASE=TRUE	PMU_OTHER5V_HI_ISENSE	

BOM_COST_GROUP=FAN

PAGE TITLE
Fans/SMC/AMUX Support

Apple Inc.

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BOM_COST_GROUP=AUDIO

DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17.12.24 2015

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Audio Placeholder

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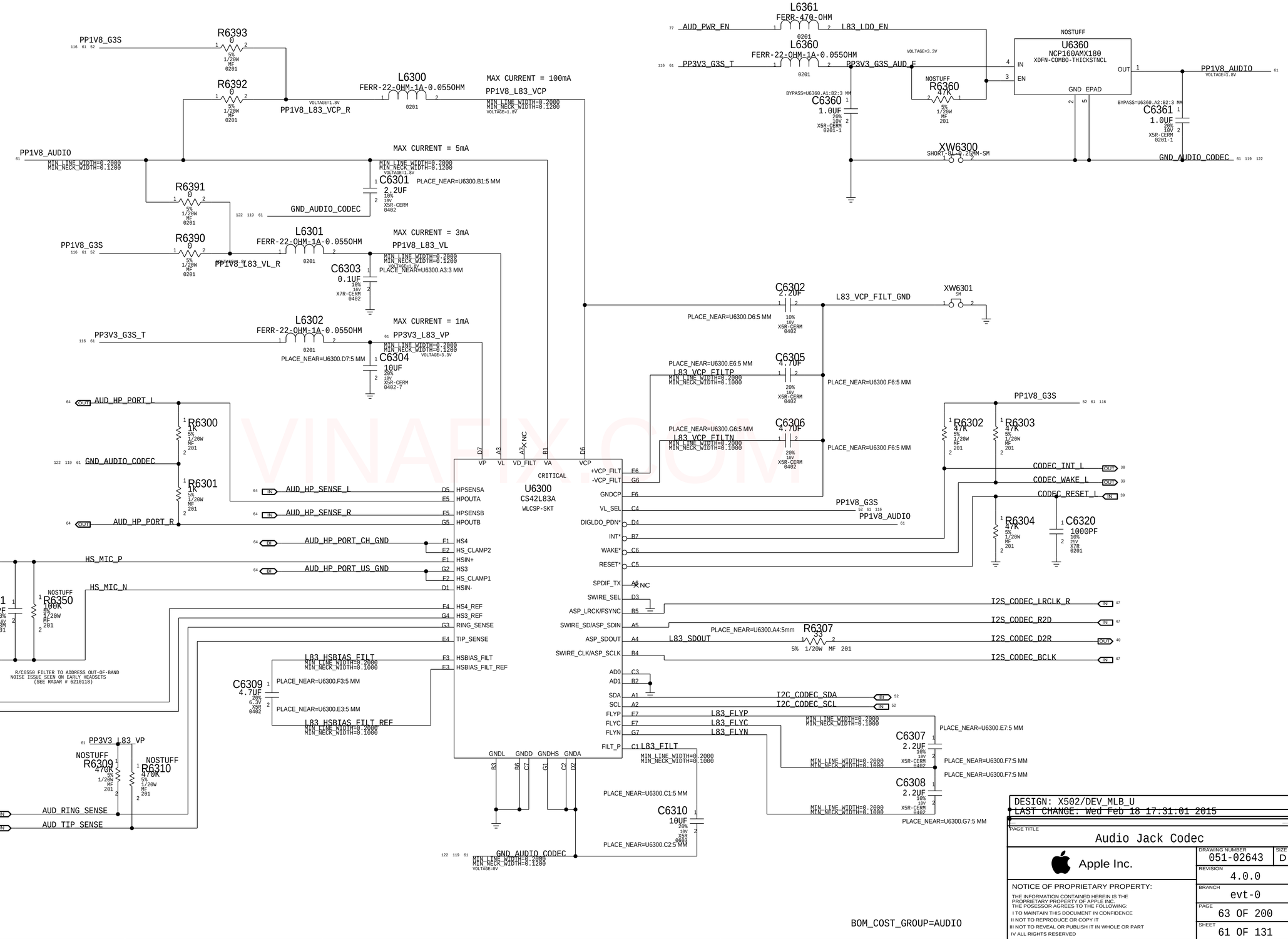
AUDIO JACK CODEC I2C ADDRESS		
AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B



DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:31.01 2015

PAGE TITLE

Audio Jack Codec

Apple Inc.

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2X MONO SPEAKER LEFT AMPLIFIERS

APN: 353S01252
GAIN: 0DBFS = xxVRMS

MAX CURRENT = 15mA PER AMPLIFIER

PLACE_NEAR=U6400.C1:5 MM
PLACE_NEAR=U6400.D2:5 MM
PLACE_NEAR=U6400.C4:3 MM
PLACE_NEAR=U6400.C1:3 MM

PP1V8_G3S

R6400 47K 5% 1/20W MF 201 2

C6400 1UF 10% 10V X5R 402-1
C6401 0.1UF 10% 25V X7R-CERM-1 0402
C6402 1UF 10% 10V X5R 402-1
C6403 0.1UF 10% 25V X7R-CERM-1 0402

PLACE_NEAR=U6400.C4:3 MM
PLACE_NEAR=U6400.C4:10 MM
PLACE_NEAR=U6400.C4:10 MM

MAX CURRENT = 2A PER AMPLIFIER

PPBUS_G3H_SPKRAMPL

C6404 0.1UF 10% 25V X7R-CERM-1 0402
C6405 22UF 20% 25V X5R-CERM 0805-1
C6406 22UF 20% 25V X5R-CERM 0805-1

SENSOR:DEV
NO_XNET_CONNECTION=1
CRITICAL
R6470 0.01 0.5% 1W MF 0612-6
PPBUS_G3H
TP_ISNS_SKPRLP
TP_ISNS_SKPRLN

C6470 3.0PF +/-0.1PF 25V NP0-C0G 0201

SPKRAMP_RESET_L
R6401 47K 5% 1/20W MF 201

C1 AVDD
D2 IOVDD
C4 VBAT
C5

U6400
PTAS5770LB2
CSP
CRITICAL

SDZ* C3
SDA F3
SCL F4
IRQZ D4
MODE D3
SDIN F2
SDOUT E1
FSYNC E2
SBCLK F1
PDMD0 E4
PDMCK0 E3
PDMD1 E5
PDMCK1 F5
GND C2
PGND A4 B4

I2C_SPKRAMP_L_SDA
I2C_SPKRAMP_L_SCL
SPKRAMP_INT_L
SPKRAMP_LW_MODE
PLACE_NEAR=U6400.E1:5 MM
I2S_SPKRAMP_L_R2D
I2S_SPKRAMP_L_D2R
I2S_SPKRAMP_L_LRCLK_R
I2S_SPKRAMP_L_BCLK

R6410 33 5% 1/20W MF 201
I2S_SPKRAMP_L_D2R_R1

BST_P B2 SPKRAMP_LW_BSTP
OUT_P A3 SPKRAMP_LW_OUTP
OUT_P B3 DIDT=TRUE
VSNS_P A1 SPKRAMP_LW_SNSP
BST_N A2 SPKRAMP_LW_BSTN
OUT_N A5 DIDT=TRUE
OUT_N B5 SPKRAMP_LW_OUTN
VSNS_N B1 SPKRAMP_LW_SNSN
AREG D5 SPKRAMP_LW_AREG
DREG D1 SPKRAMP_LW_DREG

C6411 0.1UF 10% 25V X7R-CERM-1 0402
BYPASS=U6400.B2:B3:5 MM
NO_XNET_CONNECTION=1
L6400 1800HM-3.4A 0806
PLACE_NEAR=U6400.A3:10 MM
CRITICAL
DIDT=TRUE
SHORT-8L-0.25MM-SM
XW6400
PLACE_NEAR=J6410.2:3 MM

C6412 0.1UF 10% 25V X7R-CERM-1 0402
BYPASS=U6400.A2:A5:5 MM
NO_XNET_CONNECTION=1
PLACE_NEAR=U6400.A5:10 MM
CRITICAL
L6401 1800HM-3.4A 0806
DIDT=TRUE
SHORT-8L-0.25MM-SM
XW6401
PLACE_NEAR=J6410.1:3 MM

LEFT WOOFER

SPKRCONN_LW_OUTP
SPKRCONN_LW_OUTN

APN: 518S0521
J6410 78171-0004 M-RT-SM

CRITICAL C6413 220PF 5% 25V C0G-CERM 0402
CRITICAL C6414 220PF 5% 25V C0G-CERM 0402

C6407 0.1UF 10% 25V X7R-CERM-1 0402
C6408 1UF 10% 10V X5R 402-1
C6409 0.1UF 10% 25V X7R-CERM-1 0402
C6410 1UF 10% 10V X5R 402-1

PLACE_NEAR=U6400.D1:3 MM
PLACE_NEAR=U6400.D1:5 MM
PLACE_NEAR=U6400.D2:5 MM
PLACE_NEAR=U6400.D5:5 MM

PLACE_NEAR=U6450.C1:5 MM
PLACE_NEAR=U6450.D2:5 MM
PLACE_NEAR=U6450.D2:3 MM
PLACE_NEAR=U6450.C1:3 MM

MAX CURRENT = 15mA PER AMPLIFIER

PP1V8_G3S

C6450 1UF 10% 10V X5R 402-1
C6451 0.1UF 10% 25V X7R-CERM-1 0402
C6452 1UF 10% 10V X5R 402-1
C6453 0.1UF 10% 25V X7R-CERM-1 0402

PLACE_NEAR=U6450.C4:10 MM
PLACE_NEAR=U6450.C4:10 MM
PLACE_NEAR=U6450.C4:3 MM

MAX CURRENT = 2A PER AMPLIFIER

PPBUS_G3H_SPKRAMPL

C6454 0.1UF 10% 25V X7R-CERM-1 0402
C6455 22UF 20% 25V X5R-CERM 0805-1
C6456 22UF 20% 25V X5R-CERM 0805-1

C1 AVDD
D2 IOVDD
C4 VBAT
C5

U6450
PTAS5770LB2
CSP
CRITICAL

SDZ* C3
SDA F3
SCL F4
IRQZ D4
MODE D3
SDIN F2
SDOUT E1
FSYNC E2
SBCLK F1
PDMD0 E4
PDMCK0 E3
PDMD1 E5
PDMCK1 F5
GND C2
PGND A4 B4

SPKRAMP_RESET_L
I2C_SPKRAMP_L_SDA
I2C_SPKRAMP_L_SCL
SPKRAMP_INT_L
SPKRAMP_LT_MODE
PLACE_NEAR=U6450.E1:5 MM
I2S_SPKRAMP_L_R2D
I2S_SPKRAMP_L_D2R
I2S_SPKRAMP_L_LRCLK_R
I2S_SPKRAMP_L_BCLK

R6460 33 5% 1/20W MF 201
I2S_SPKRAMP_L_D2R_R2

BST_P B2 SPKRAMP_LT_BSTP
OUT_P A3 SPKRAMP_LT_OUTP
OUT_P B3 DIDT=TRUE
VSNS_P A1 SPKRAMP_LT_SNSP
BST_N A2 SPKRAMP_LT_BSTN
OUT_N A5 DIDT=TRUE
OUT_N B5 SPKRAMP_LT_OUTN
VSNS_N B1 SPKRAMP_LT_SNSN
AREG D5 SPKRAMP_LT_AREG
DREG D1 SPKRAMP_LT_DREG

C6461 0.1UF 10% 25V X7R-CERM-1 0402
BYPASS=U6450.B2:B3:5 MM
NO_XNET_CONNECTION=1
L6450 1800HM-3.4A 0806
CRITICAL
PLACE_NEAR=U6450.A3:10 MM
SHORT-8L-0.25MM-SM
XW6450
PLACE_NEAR=J6410.3:3 MM

C6462 0.1UF 10% 25V X7R-CERM-1 0402
BYPASS=U6450.A2:A5:5 MM
NO_XNET_CONNECTION=1
L6451 1800HM-3.4A 0806
CRITICAL
PLACE_NEAR=U6450.A5:10 MM
SHORT-8L-0.25MM-SM
XW6451
PLACE_NEAR=J6410.4:3 MM

LEFT TWEETER

SPKRCONN_LT_OUTP
SPKRCONN_LT_OUTN

CRITICAL C6463 220PF 5% 25V C0G-CERM 0402
CRITICAL C6464 220PF 5% 25V C0G-CERM 0402

C6457 0.1UF 10% 25V X7R-CERM-1 0402
C6458 1UF 10% 10V X5R 402-1
C6459 0.1UF 10% 25V X7R-CERM-1 0402
C6460 1UF 10% 10V X5R 402-1

PLACE_NEAR=U6450.D1:3 MM
PLACE_NEAR=U6450.D1:5 MM
PLACE_NEAR=U6450.D2:5 MM
PLACE_NEAR=U6450.D5:5 MM

LEFT BULK CAPACITANCE

CAPDERATE CAPDERATE CAPDERATE CAPDERATE

PPBUS_G3H_SPKRAMPL

C6480 330UF 20% 16V TANT-POLY CASE-B3
C6481 330UF 20% 16V TANT-POLY CASE-B3
C6482 330UF 20% 16V TANT-POLY CASE-B3
C6483 330UF 20% 16V TANT-POLY CASE-B3
C6484 330UF 20% 16V TANT-POLY CASE-B3
C6485 330UF 20% 16V TANT-POLY CASE-B3

CAPDERATE CAPDERATE

PP1V8_G3S

NOSTUFF R6480 10K 5% 1/20W MF 201
NOSTUFF R6482 2.2K 5% 1/20W MF 201

SPKRAMP_LW_MODE
SPKRAMP_LT_MODE

R6481 470 5% 1/20W MF 201
R6483 0 5% 1/20W MF 0201

I2C ADDRESS

MODE PIN	7-BIT	CHANNEL
GND	0x31	L TW
470 to GND	0x32	L WF
470 to IOVDD	0x33	R TW
2K2 to GND	0x34	R WF
2K2 to IOVDD	0x35	
10K to GND	0x36	
10K to IOVDD	0x37	
47K to IOVDD	0x38	

BOM_COST_GROUP=AUDIO

SYNC_MASTER=TROY SYNC_DATE=12/11/2017

PAGE TITLE: Audio Left Amplifiers

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
PAGE: 64 OF 200
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2X MONO SPEAKER RIGHT AMPLIFIERS

APN: 353S01252
GAIN: 0DBFS = xxVRMS

MAX CURRENT = 15mA PER AMPLIFIER

PP1V8_G3S

C6508 1UF 10% 10V X5R 402-1
C6500 0.1UF 10% 25V X7R-CERM-1 0402
C6509 1UF 10% 10V X5R 402-1
C6505 0.1UF 10% 10V X5R-CERM 0201

PLACE_NEAR=U6500.D2:3 MM
PLACE_NEAR=U6500.C4:3 MM
PLACE_NEAR=U6500.C1:5 MM

MAX CURRENT = 2A PER AMPLIFIER

PPBUS_G3H

C6501 0.1UF 10% 25V X7R-CERM-1 0402
C6503 22UF 20% 25V X5R-CERM 0805-1
C6504 22UF 20% 25V X5R-CERM 0805-1

PLACE_NEAR=U6500.C4:10 MM
PLACE_NEAR=U6500.C4:10 MM
PLACE_NEAR=U6500.C4:3 MM

U6500
PTAS5770LB2
CSP
CRITICAL

SPKRAMP_RESET_L	C3	SDZ*
I2C_SPKRAMP_R_SDA	F3	SDA
I2C_SPKRAMP_R_SCL	F4	SCL
SPKRAMP_INT_L	D4	IRQZ
SPKRAMP_RT_MODE	D3	MODE
I2S_SPKRAMP_R_R2D	F2	SDIN
I2S_SPKRAMP_L_D2R	E1	SDOUT
I2S_SPKRAMP_R_LRCLK_R	E2	FSYNC
I2S_SPKRAMP_R_BCLK	F1	SBCLK
	E4	PDMD0
	E3	PDMCK0
	E5	PDMD1
	F5	PDMCK1
	AVDD, IOVDD, VBAT, GND, PGND	
SPKRAMP_RT_BSTP	B2	BST_P
SPKRAMP_RT_OUTP	A3	OUT_P
	B3	OUT_P
SPKRAMP_RT_SNSP	A1	VSNS_P
SPKRAMP_RT_BSTN	A2	BST_N
	A5	OUT_N
SPKRAMP_RT_OUTN	B5	OUT_N
SPKRAMP_RT_SNSN	B1	VSNS_N
SPKRAMP_RT_AREG	D5	AREG
SPKRAMP_RT_DREG	D1	DREG

R6510 33 5% 1/20W MF 201
PLACE_NEAR=U6500.E1:5 MM

C6511 0.1UF 10% 25V X7R-CERM-1 0402 BYPASS=U6500.B2:B3:5 MM NO_XNET_CONNECTION=1
C6512 0.1UF 10% 25V X7R-CERM-1 0402 BYPASS=U6500.A2:A5:5 MM NO_XNET_CONNECTION=1

L6500 1800HM-3.4A 0806 CRITICAL PLACE_NEAR=U6500.A3:10 MM
L6501 1800HM-3.4A 0806 CRITICAL PLACE_NEAR=U6500.A5:10 MM

DIDT=TRUE

XW6500 SHORT-8L-0.25MM-SM PLACE_NEAR=J6500.2:3 MM
XW6501 SHORT-8L-0.25MM-SM PLACE_NEAR=J6500.1:3 MM

C6513 0.1UF 10% 25V X7R-CERM-1 0402
C6514 1UF 10% 10V X5R 402-1
C6515 0.1UF 10% 25V X7R-CERM-1 0402
C6516 1UF 10% 10V X5R 402-1

PLACE_NEAR=U6500.D1:3 MM
PLACE_NEAR=U6500.D1:5 MM
PLACE_NEAR=U6500.D5:3 MM
PLACE_NEAR=U6500.D5:5 MM

RIGHT TWEETER

SPKRCONN_RT_OUTP
SPKRCONN_RT_OUTN

C6506 220PF 5% 25V C0G-CERM 0402 CRITICAL
C6507 220PF 5% 25V C0G-CERM 0402 CRITICAL

PP1V8_G3S
R6590 47K 5% 1/20W MF 201
SPKR_ID0

APN: 518S0672
J6500 78171-6006 M-RT-SM

MAX CURRENT = 15mA PER AMPLIFIER

PP1V8_G3S

C6558 1UF 10% 10V X5R 402-1
C6550 0.1UF 10% 25V X7R-CERM-1 0402
C6559 1UF 10% 10V X5R 402-1
C6555 0.1UF 10% 10V X7R-CERM-1 0402

PLACE_NEAR=U6550.D2:3 MM
PLACE_NEAR=U6550.C4:3 MM
PLACE_NEAR=U6550.C1:5 MM

MAX CURRENT = 2A PER AMPLIFIER

PPBUS_G3H

C6551 0.1UF 10% 25V X7R-CERM-1 0402
C6553 22UF 20% 25V X5R-CERM 0805-1
C6554 22UF 20% 25V X5R-CERM 0805-1

PLACE_NEAR=U6550.C4:10 MM
PLACE_NEAR=U6550.C4:10 MM
PLACE_NEAR=U6550.C4:3 MM

U6550
PTAS5770LB2
CSP
CRITICAL

SPKRAMP_RESET_L	C3	SDZ*
I2C_SPKRAMP_R_SDA	F3	SDA
I2C_SPKRAMP_R_SCL	F4	SCL
SPKRAMP_INT_L	D4	IRQZ
SPKRAMP_RW_MODE	D3	MODE
I2S_SPKRAMP_R_R2D	F2	SDIN
I2S_SPKRAMP_L_D2R	E1	SDOUT
I2S_SPKRAMP_R_LRCLK_R	E2	FSYNC
I2S_SPKRAMP_R_BCLK	F1	SBCLK
	E4	PDMD0
	E3	PDMCK0
	E5	PDMD1
	F5	PDMCK1
	AVDD, IOVDD, VBAT, GND, PGND	
SPKRAMP_RW_BSTP	B2	BST_P
SPKRAMP_RW_OUTP	A3	OUT_P
	B3	OUT_P
SPKRAMP_RW_SNSP	A1	VSNS_P
SPKRAMP_RW_BSTN	A2	BST_N
	A5	OUT_N
SPKRAMP_RW_OUTN	B5	OUT_N
SPKRAMP_RW_SNSN	B1	VSNS_N
SPKRAMP_RW_AREG	D5	AREG
SPKRAMP_RW_DREG	D1	DREG

R6560 33 5% 1/20W MF 201
PLACE_NEAR=U6550.E1:5 MM

C6561 0.1UF 10% 25V X7R-CERM-1 0402 BYPASS=U6550.B2:B3:5 MM NO_XNET_CONNECTION=1
C6562 0.1UF 10% 25V X7R-CERM-1 0402 BYPASS=U6550.A2:A5:5 MM NO_XNET_CONNECTION=1

L6550 1800HM-3.4A 0806 CRITICAL PLACE_NEAR=U6550.A3:10 MM
L6551 1800HM-3.4A 0806 CRITICAL PLACE_NEAR=U6550.A5:10 MM

DIDT=TRUE

XW6550 SHORT-8L-0.25MM-SM PLACE_NEAR=J6500.5:3 MM
XW6551 SHORT-8L-0.25MM-SM PLACE_NEAR=J6500.6:3 MM

C6563 0.1UF 10% 25V X7R-CERM-1 0402
C6564 1UF 10% 10V X5R 402-1
C6565 0.1UF 10% 25V X7R-CERM-1 0402
C6566 1UF 10% 10V X5R 402-1

PLACE_NEAR=U6550.D5:5 MM
PLACE_NEAR=U6550.D5:3 MM
PLACE_NEAR=U6550.D1:5 MM
PLACE_NEAR=U6550.D1:3 MM

RIGHT WOOFER

SPKRCONN_RW_OUTP
SPKRCONN_RW_OUTN

C6556 220PF 5% 25V C0G-CERM 0402 CRITICAL
C6557 220PF 5% 25V C0G-CERM 0402 CRITICAL

CAPDERATE

PPBUS_G3H

C6580 33UF 20% 16V TANT-POLY CASE-B3
C6581 33UF 20% 16V TANT-POLY CASE-B3
C6582 33UF 20% 16V TANT-POLY CASE-B3
C6583 33UF 20% 16V TANT-POLY CASE-B3
C6584 33UF 20% 16V TANT-POLY CASE-B3
C6585 33UF 20% 16V TANT-POLY CASE-B3

PP1V8_G3S

R6580 470 5% 1/20W MF 201
NOSTUFF R6582 2.2K 5% 1/20W MF 201
SPKRAMP_RT_MODE
SPKRAMP_RW_MODE
NOSTUFF R6581 0 5% 1/20W MF 0201
R6583 2.2K 5% 1/20W MF 201

I2C ADDRESS

MODE PIN	7-BIT	CHANNEL
GND	0x31	L TW
470 to GND	0x32	L WF
470 to IOVDD	0x33	R TW
2K2 to GND	0x34	R WF
2K2 to IOVDD	0x35	
10k to GND	0x36	
10k to IOVDD	0x37	
47k to IOVDD	0x38	

BOM_COST_GROUP=AUDIO

PAGE TITLE: Audio Right Amplifiers

Apple Inc.

DRAWING NUMBER: 051-02643
SIZE: D
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BRANCH: evt-0
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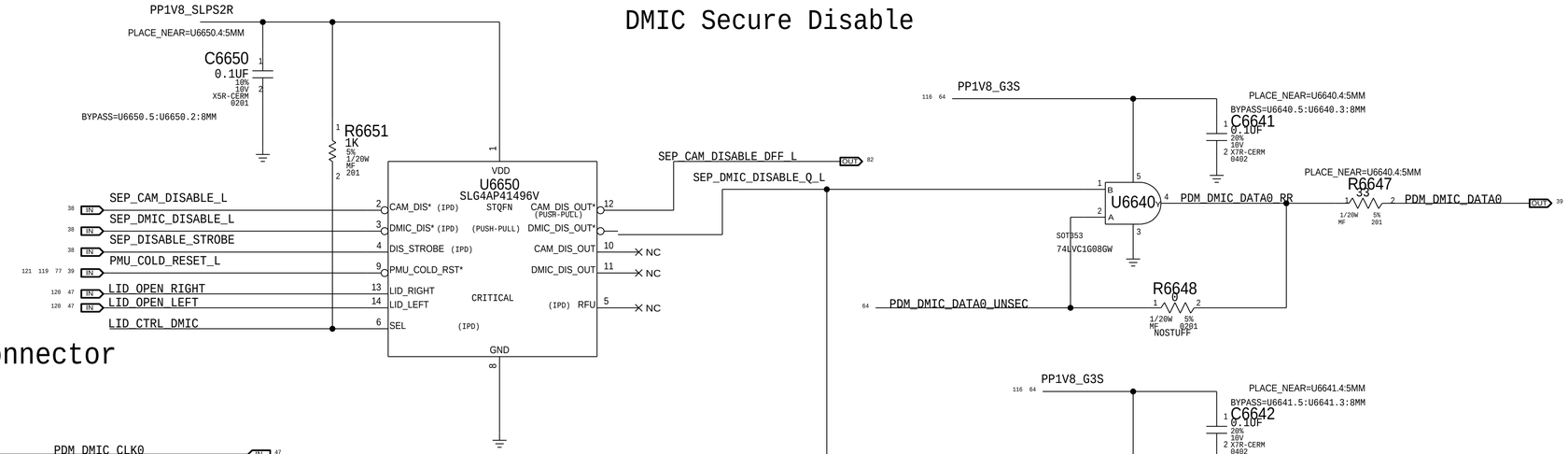
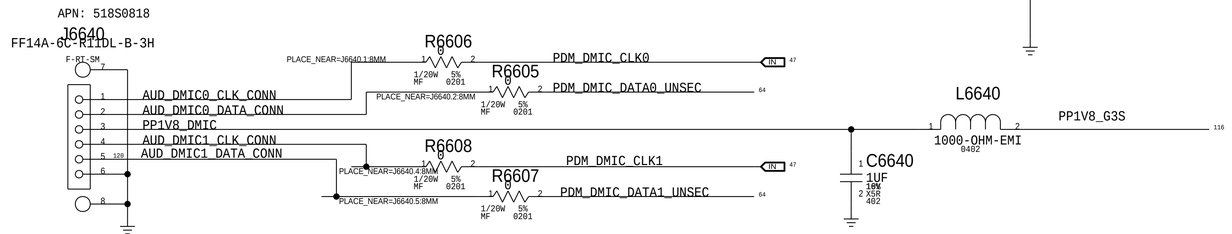
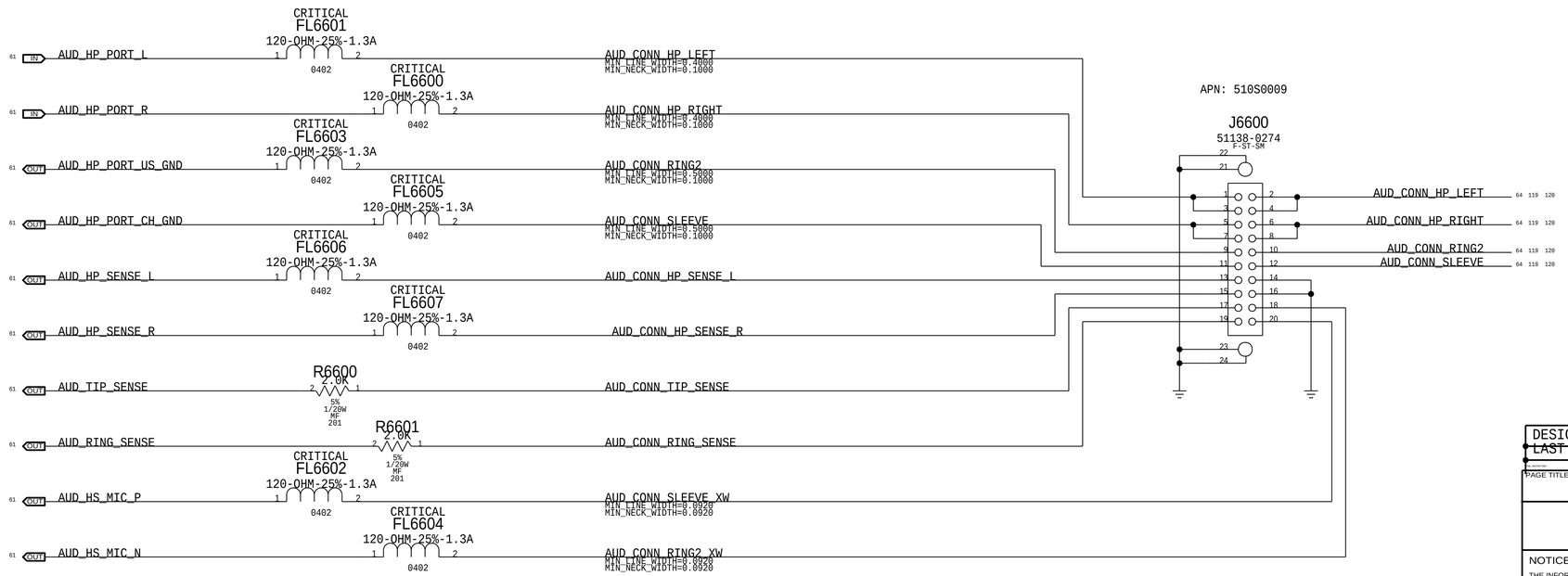
DMIC Secure Disable



Digital Mic Flex Connector



Audio Jack Flex Connector



DESIGN: X502/DEV_MLB_U
LAST CHANGE: Wed Feb 18 17:12:24 2015

PAGE TITLE

Audio Flex Connectors

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
REVISION 4.0.0
BRANCH evt-0
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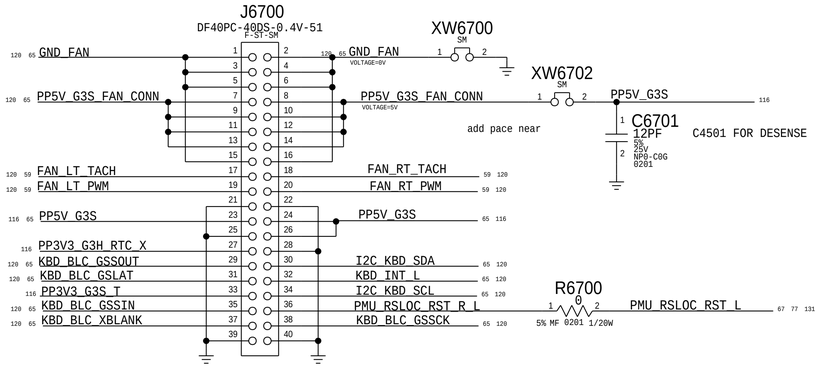
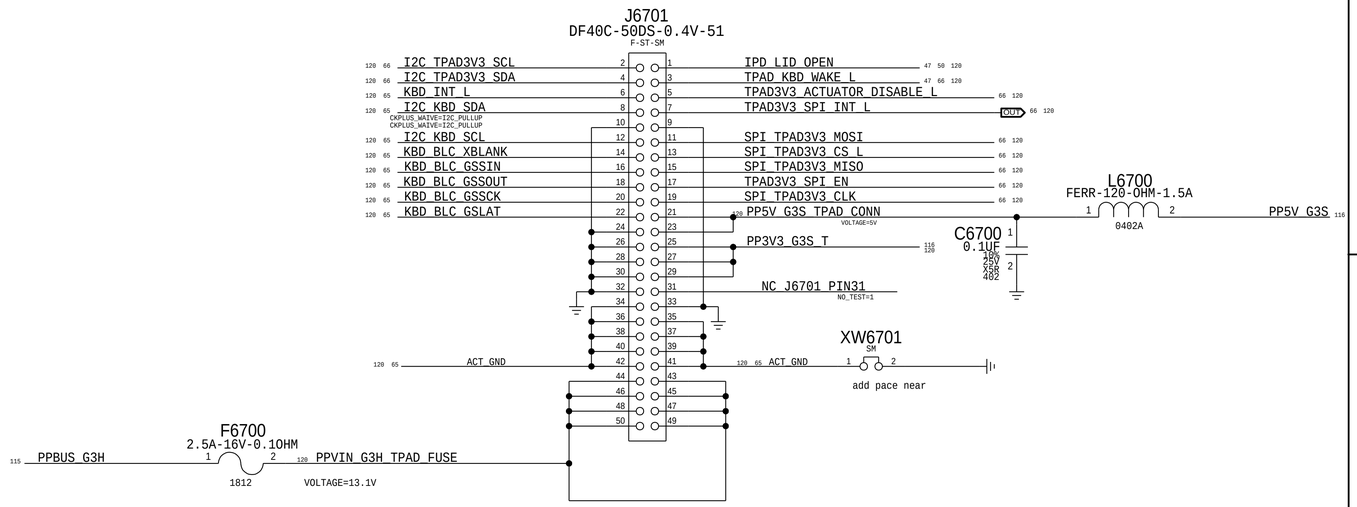
KBD CONNECTOR



516S00177 (RCPT, 0.3A per pin)
MATE WITH PLUG 516S00054

TPAD CONNECTOR



516S00187, MATE WITH 516S00188

BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=1332 SYNC_DATE=03/23/2017

PAGE TITLE: Keyboard & Trackpad 1

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
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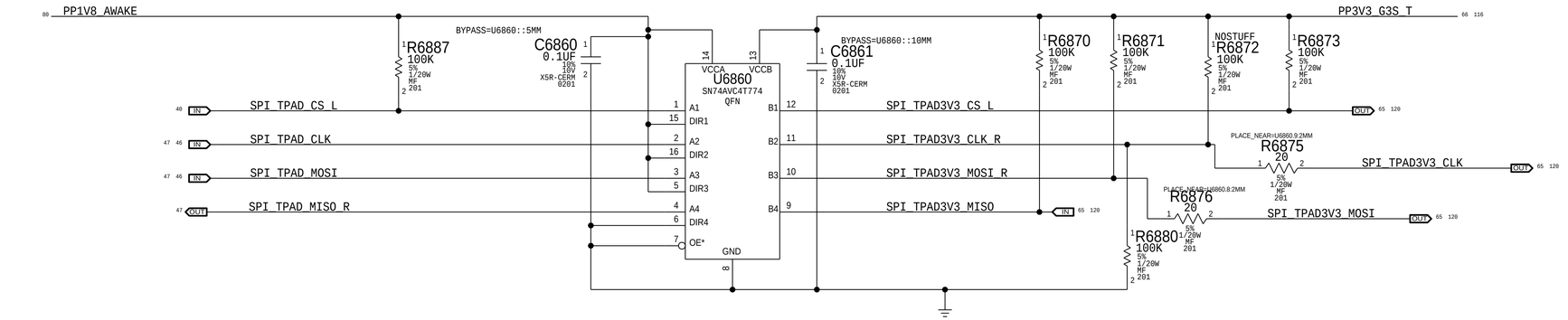
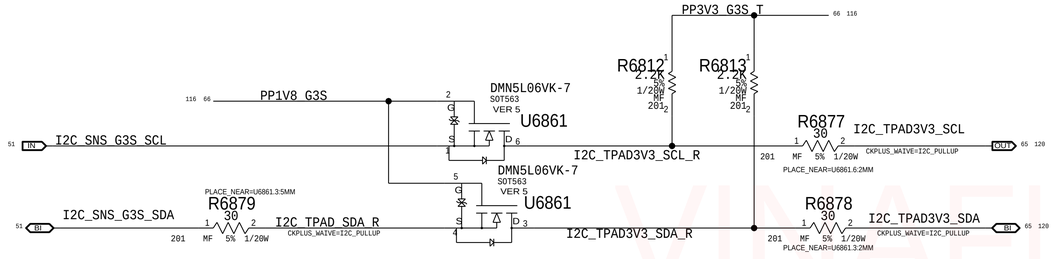
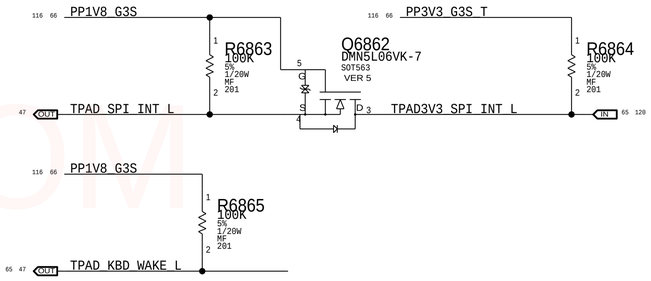
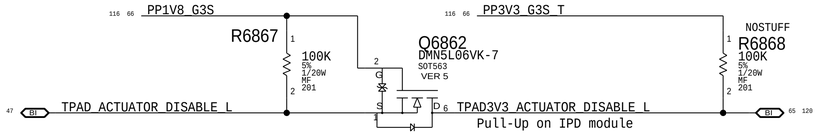
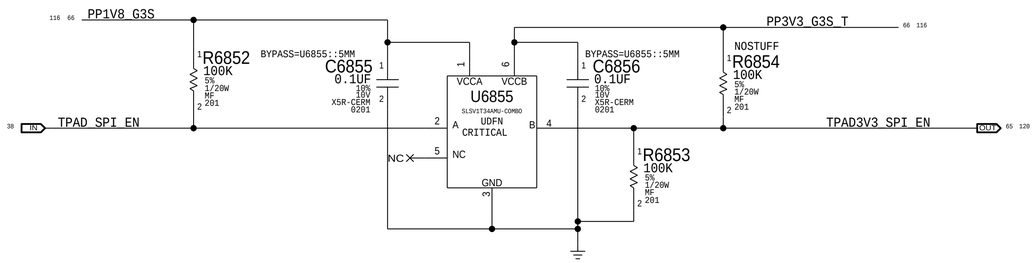
Trackpad Level Shifting











BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=j132	SYNC_DATE=03/23/2017
PAGE TITLE	Keyboard & Trackpad 2
Apple Inc.	DRAWING NUMBER 051-02643 SIZE D
	REVISION 4.0.0
	BRANCH evt-0
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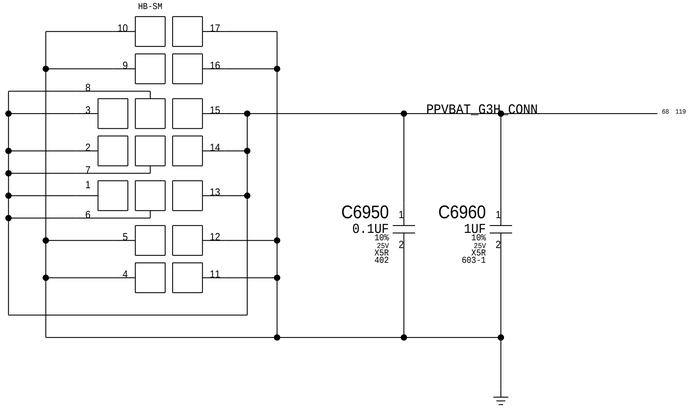
J80 Battery Hotbar Flex Pads 998-03902
Flex Pad TO MLB 998-03780.

CRITICAL
OMIT_TABLE

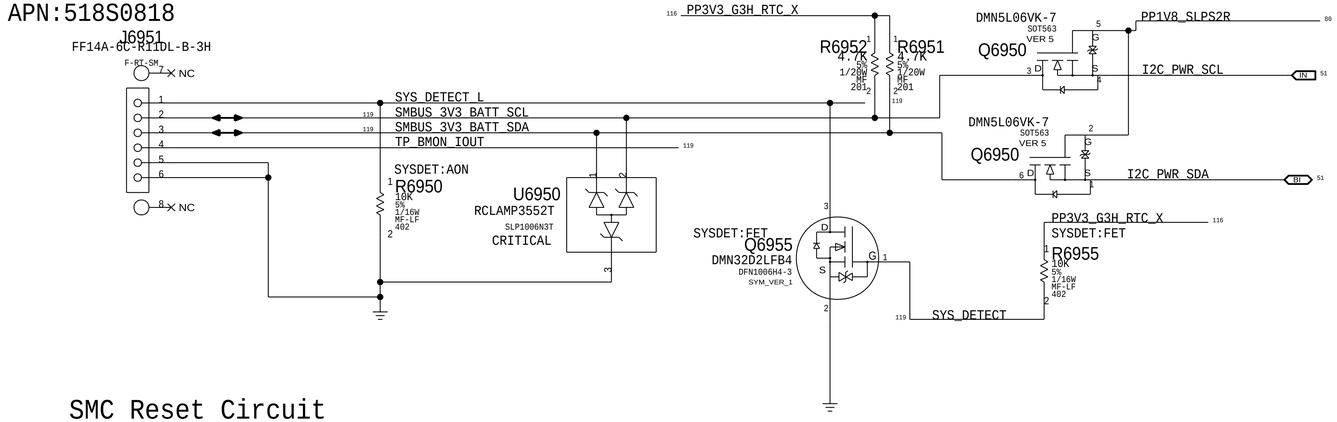
J6950
PWR-MLB-X363
HB-SM



BMU POWER FLEX HOTBAR'd TO THE MLB:

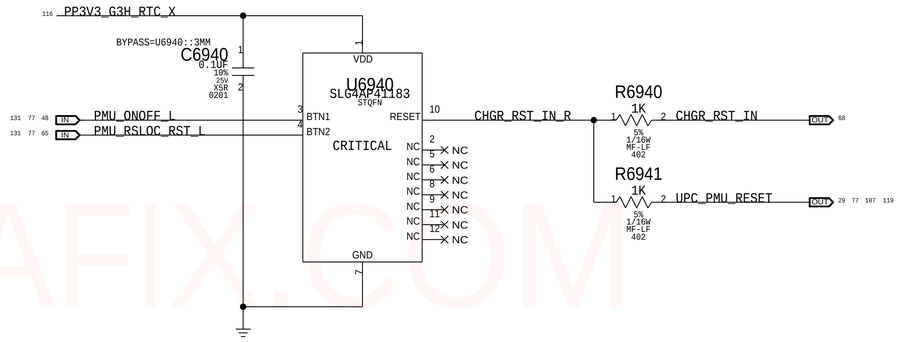
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00862	1	PCBA,FLEX,BMU PWR,X363	J6950	CRITICAL	

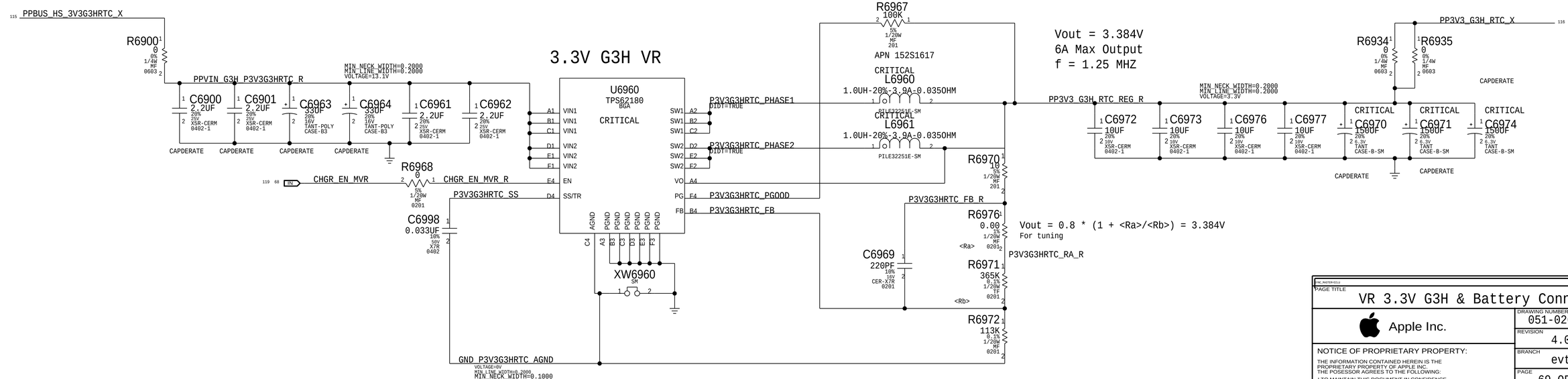
APN:518S0818



SMC Reset Circuit

Right Shift & Left Option Control
followed by ON OFF button press.



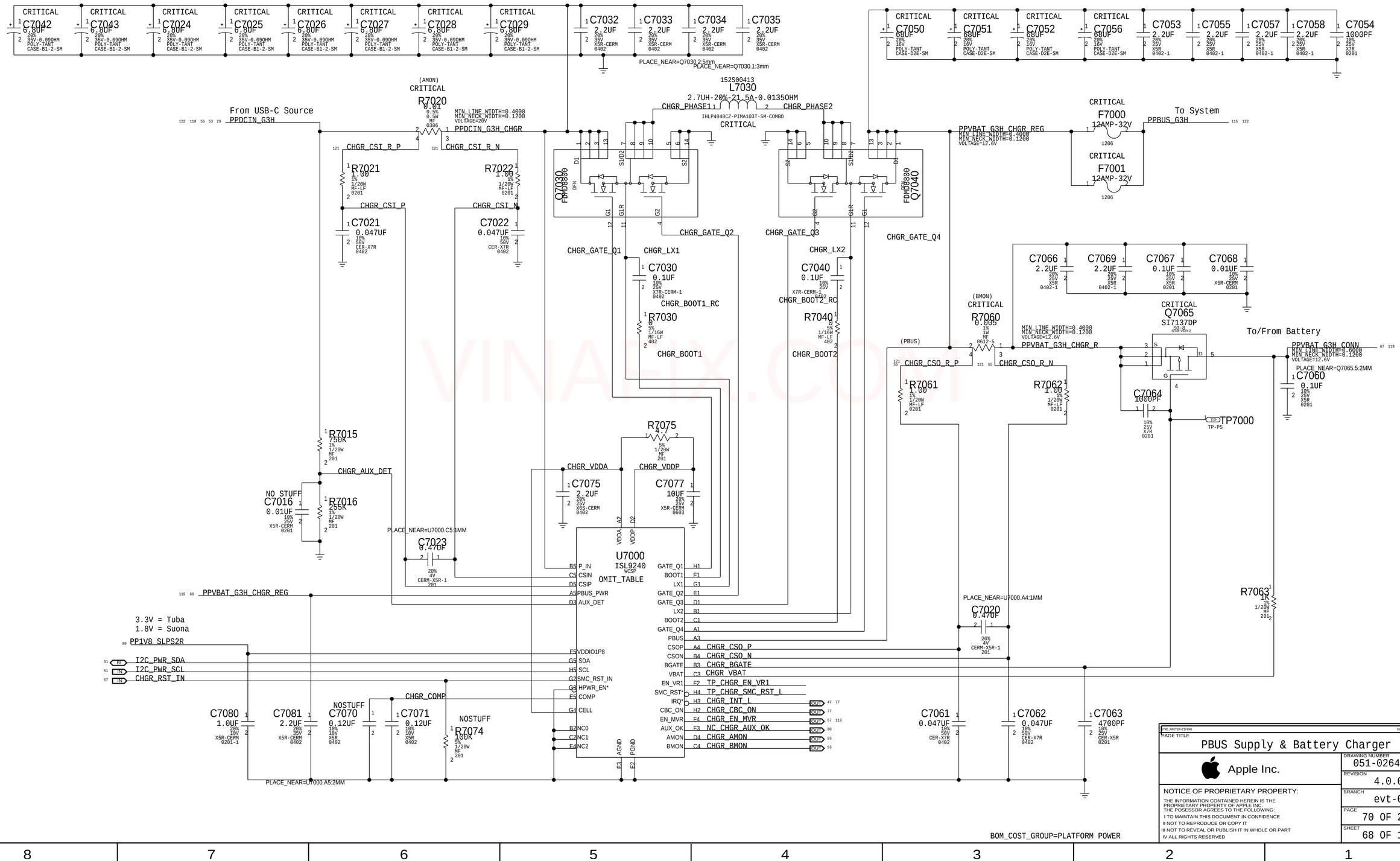


BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
VR 3.3V G3H & Battery Conn

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
REVISION 4.0.0
BRANCH evt-0
PAGE 69 OF 200
SHEET 67 OF 131



PAGE TITLE

IMVP IC

Apple Inc.

DRAWING NUMBER 051-02643 SIZE D

REVISION 4.0.0

BRANCH evt-0

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00519	3	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7210,U7220,U7230	CRITICAL	

PAGE TITLE
IMVP VCC Block

Apple Inc.

DRAWING NUMBER 051-02643 SIZE D
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BRANCH evt-0
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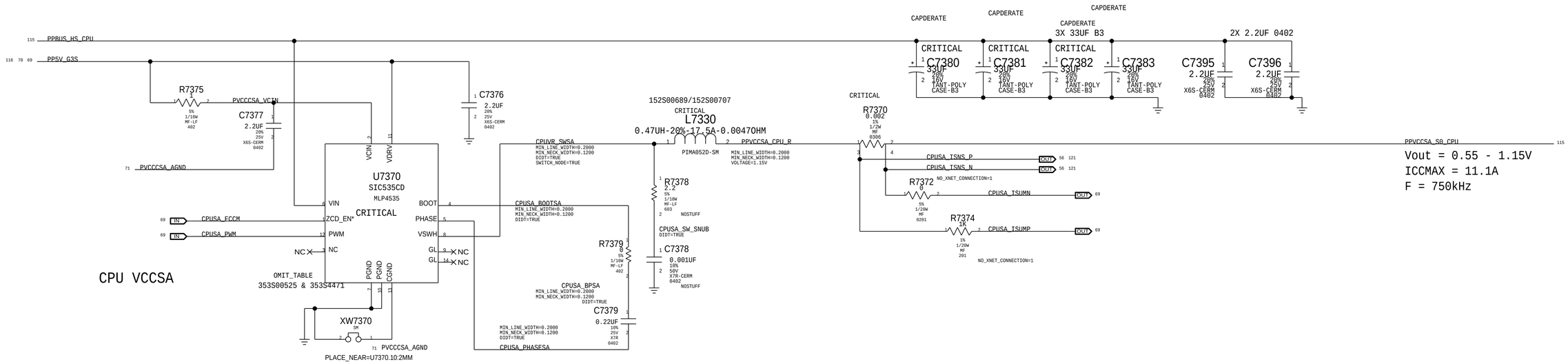
SHEET 70 OF 131



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00525	1	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7370	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=S11U SYNC_DATE=05/19/2017

PAGE TITLE

IMVP SA Block

Apple Inc.

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BRANCH evt-0

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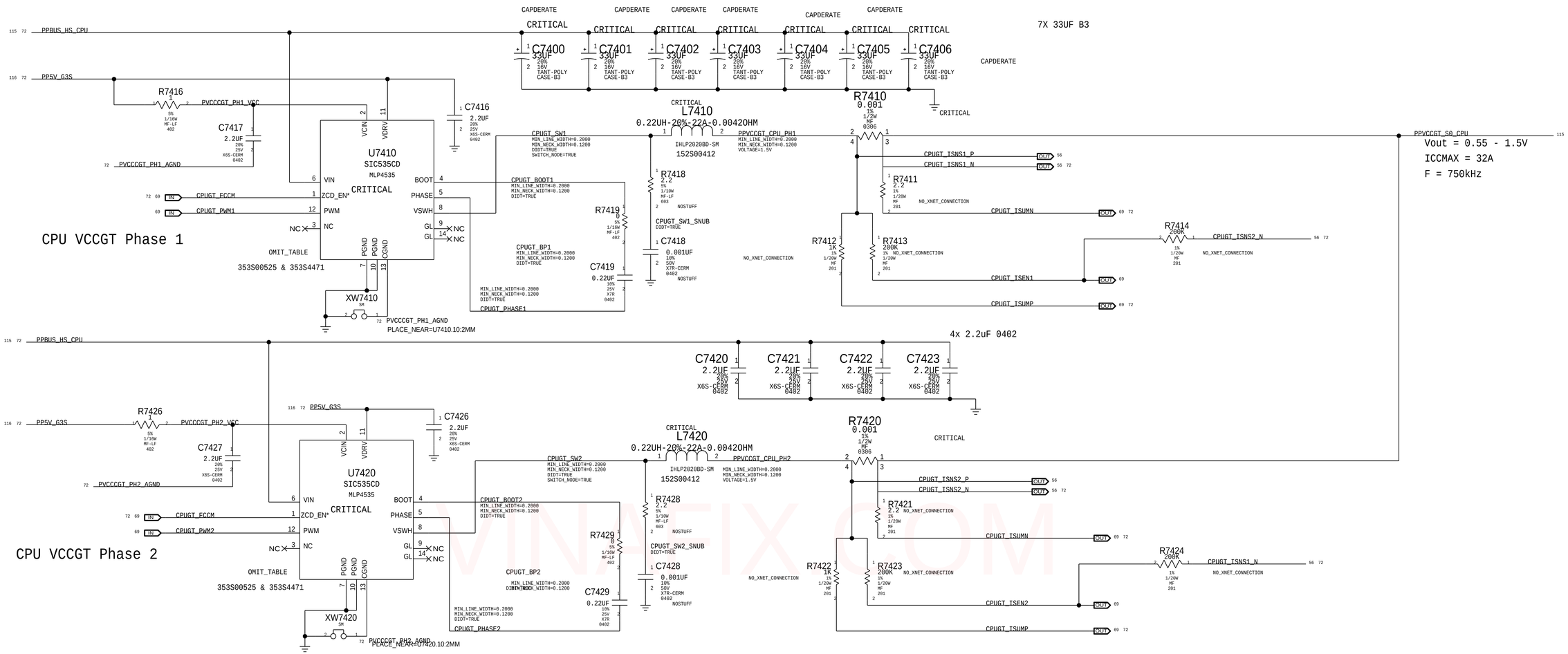

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00525	2	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7410,U7420	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: IMVP GT Block

Apple Inc.

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BRANCH: evt-0
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5V S0 - V5

3.3V DSW - V6

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00703	1	IND,MLD,2.2UH,20%,43mOHM,5.5A,4.2x4x2MM	L7600	CRITICAL	

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: Power - 5V 3.3V Supply

Apple Inc.

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2.5V VPP

PPBUS_HS_CPU

CAPDERATE

CRITICAL C7700 12PF 5% 25V NP0-C0G 0201

CRITICAL C7701 3.0PF +/-0.1PF 25V NP0-C0G 0201

CRITICAL C7702 33UF 20% 16V TANT-POLY CASE-B3

CRITICAL C7703 2.2UF 20% 25V X6S-CERM 0402

CRITICAL C7704 2.2UF 20% 25V X6S-CERM 0402

R7700 10 5% 1/20W MF 201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=2.5V

PPVIN_S3_DDR2V5_RC

PVDDQ_EN

R8153 47K 5% 1/20W MF 201

R7709 0 5% 1/20W MF 0201

PVPP_EN_R

U7700 TPS62130B-S VQFN

AVIN, DEF, EN, FSW, PVIN, PGND, AGND, THRM PAD

SW: REG_PHASE_2V5S3

DIDT=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

CRITICAL L7700 1.5UH-20%-2.61A-0.068OHM PIFE32251B-SM

P2V5S3_REG

MIN_LINE_WIDTH=0.6920
MIN_NECK_WIDTH=0.0850
VOLTAGE=2.5V

SENSOR:DEV R7724 0.005 1% 1W CYN 0612

ISNS_2V5_S3_N

ISNS_2V5_S3_P

R7701 10 5% 1/20W MF 201

VOS: REG_VOS_P2V5S3

FB: REG_FB_P2V5S3

PG: P2V5_VPP_PGOOD

SS/TR: REG_SSTR_P2V5S3

C7705 0.1UF 10% 25V X6S 0402

C7706 4700PF 10% 10V X7R 201

R7702 162K 0.1% 1/16W TK 0402 <Ra>

R7703 76.8K 0.1% 1/16W MF 0402 <Rb>

XW7700 SM

XW7701 SM

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
AGND_P2V5S3
P2V5S3_FSW

Output voltage: 2.5 V
Max peak current: 2.24 A
Switching freq: 1250 kHz

NOSTUFF D7700 SOD523 PMEG3010EB/S500

NOSTUFF D7701 SOD523 PMEG3010EB/S500

PP1V2_S3

PP2V5_S3

CRITICAL C7707 100UF 20% 6.3V TANT-POLY CASE-A3-LLP

CRITICAL C7708 100UF 20% 6.3V TANT-POLY CASE-A3-LLP

CRITICAL C7709 100UF 20% 6.3V TANT-POLY CASE-A3-LLP

C7764 10UF 20% 4V X6S 0402

C7765 10UF 20% 4V X6S 0402

1.2V VDDQ & 0.6V VTT

PP1V2_S3

PP5V_G3S

R7754 0 5% 1/20W MF 0201 VOLTAGE=5V
PP5V_EDRAM_V5IN
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

BYPASS=U7701.12::10mm

BYPASS=U7701.2::10mm

C7714 10UF 20% 10V X5R-CERM 0402-1

C7711 10UF 20% 10V X5R-CERM 0402-1

C7710 10UF 20% 10V X5R-CERM 0402-1

MEMVTT_EN

P2V5_VPP_PGOOD

R7756 0 5% 1/20W MF 0201

R7755 0 5% 1/20W MF 0201

MEMVTT_EN_R

PVDDQ_EN_R

P1V2REG_VREF

P1V2REG_MODE

P1V2REG_TRIP

VLDOIN

U7701 TPS51916 QFN CRITICAL

V5IN, S3, S5, VREF, REFIN, MODE, TRIP

VBST, DRVH, SW, DRVL, PGOOD, VDDQSNS, VTT, VTTSNS, VTTREF

PGND GND, VTT THRM GND PAD

R7730 2.2 5% 1/20W MF 201

DIDT=TRUE
SWITCH_NODE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

P1V2_VBST

C7730 0.1UF 10% 25V X6S-CERM 0201

SWITCH_NODE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
DIDT=TRUE

P1V2_SW

P1V2_DRVH

R7733 1 5% 1/20W MF 201

P1V2_DRVH_R

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
SWITCH_NODE=TRUE
DIDT=TRUE

P1V2_DRVL

R7732 1 5% 1/20W MF 201

P1V2_DRVL_R

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
GATE_NODE=TRUE
DIDT=TRUE

PVDDQ_PGOOD

Q7700 CSD58873Q3D Q3D

TG, TGR, BG, VIN, VSW, PGND

MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
SWITCH_NODE=TRUE
DIDT=TRUE

P1V2_PHASE

L7701 0.68UH-20%-14A PILE063T-SM

152S00140

R7718 0.002 1% 1W CYN 0612

PP1V2_S3_REG_R

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.2V

ISNS_CPUDDR_P

ISNS_CPUDDR_N

R7710 2.2 5% 1/10W MF-LF 603

DIDT=TRUE
SWITCH_NODE=TRUE
P1V2_LL_SNUB

C7712 0.001UF 10% 50V X7R-CERM 0402

CRITICAL C7713 330UF 20% 2.0V POLY-TANT CASE-B2-SM1

CRITICAL C7717 330UF 20% 2.0V POLY-TANT CASE-B2-SM1

CRITICAL C7718 330UF 20% 2.0V POLY-TANT CASE-B2-SM1

CRITICAL C7719 10UF 20% 4V X6S 0402

CRITICAL C7720 10UF 20% 4V X6S 0402

CRITICAL C7727 220UF 20% 2V ELEC SM-COMBO

CRITICAL C7728 220UF 20% 2V ELEC SM-COMBO

PP1V2_S3
Vout = 1.2V
8.2A MAX OUTPUT
F = 400 KHZ

PLACE_NEAR=C7713.1:5mm

XW7710 SM

R7741 10 5% 1/20W MF 201

P1V2_SNS

P1V2_SNS_R

MIN_LINE_WIDTH=0.0920
MIN_NECK_WIDTH=0.0850

PP0V6_S0_DDRVTT

C7731 15UF 20% 2.2V X6S 0402

C7732 15UF 20% 2.2V X6S 0402

C7733 15UF 20% 2.2V X6S 0402

C7734 15UF 20% 2.2V X6S 0402

C7736 15UF 20% 2.2V X6S 0402

C7737 15UF 20% 2.2V X6S 0402

PPBUS_HS_CPU

CAPDERATE

C7721 33UF 20% 16V TANT-POLY CASE-B3

C7722 33UF 20% 16V TANT-POLY CASE-B3

C7725 33UF 20% 16V TANT-POLY CASE-B3

C7723 2.2UF 20% 25V X6S-CERM 0402

C7724 2.2UF 20% 25V X6S-CERM 0402

BYPASS=U7701.6::5mm

PLACE_NEAR=U7701.19:5mm

C7715 0.1UF 10% 6.3V X7R 0201

R7711 3.3K 1% 1/20W MF 201

P1V2REG_VREF_R

R7717 21K 0.1% 1/20W MF 0201

PLACE_NEAR=U7701.8:5mm

R7712 49.7K 0.1% 1/20W MF 0201

BYPASS=U7701.8::5mm

C7716 0.01UF 10% 10V X7R-CERM 0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

P1V2REG_AGND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0V

PLACE_NEAR=U7701.19:3mm

R7713 47K 1% 1/20W MF 201

R7714 57.6K 1% 1/20W MF 201

PLACE_NEAR=U7701.18:3mm

PLACE_NEAR=U7701.21:1mm

PPVTT_VTTREF
VOLTAGE=0.6V

C7740 0.22UF 10% 16V CERM 402

XW7702 SM

PVTT_VTTSNS

R7757 0 5% 1/20W MF 0201

PLACE_NEAR=U7701.1:5mm

DDRREG_VTTSNS

XW7705 SM

PLACE_NEAR=C7737.1:5mm

LEVEL SHIFT

PP1V05_PRIM

PP1V8_S5

C7790 0.1UF 10% 10V X5R-CERM 0201

C7791 0.1UF 10% 10V X5R-CERM 0201

U7790 SLSV173AMU-COMBO UDFN CRITICAL

VCCA, VCCB, A, B, NC, GND

TPS51916 Ileak) = +/-1uA
Vih(min) = 1.5V
33uW when driven-low

PM_MEMVTT_EN

MEMVTT_EN

R7791 100K 5% 1/20W MF 201

PP2V5_S3

R7758 1.5K 1% 1/20W MF 201

P2V5_VPP_PGOOD

PP1V8_S5

R7716 100K 5% 1/20W MF 201

PVDDQ_PGOOD

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: VR 2.5V & 1.2V/VTT

Apple Inc.

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Note : Design based on Calpe ERS - D2449-A0-110-00_0v3.pdf (Radar# 24696002)
System Block Diagram - T290 Power System Architecture . v9
Optimize componentS for individual projects based on EDP(A)

Note : All Bucks are default Local Sense

Buck 0,2, and 8 have option for Remote Sense for Future Use.

PAGE TITLE	PMIC BUCKS AND SWs
Apple Inc.	DRAWING NUMBER 051-02643 SIZE D
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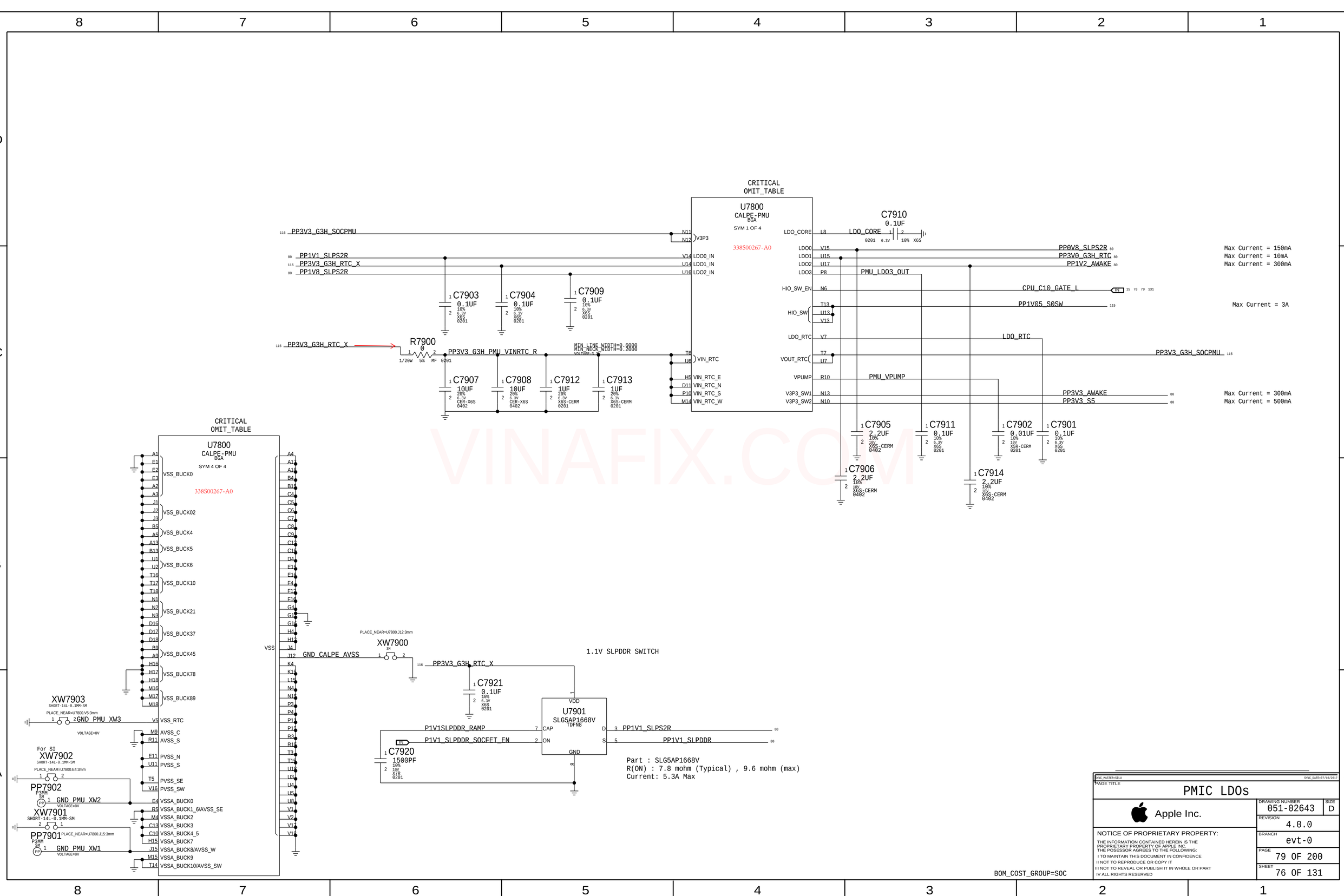

CRITICAL
OMIT_TABLE

U7800
CALPE-PMU
BGA
SYM 3 OF 4
338S00267-A0

SOC_WDOG	F5	RESET_IN1 (IPD)	
SOC_SOCHOT_L	E5	RESET_IN2	
UPC_PMU_RESET	K5	RESET_IN3 (IPD)	
SOC_PM_THRMTRIP_L	K6	RESET_IN4	
SOC_GPU_THRMTRIP	N5	RESET_IN5 (IPD)	
PMU_COLD_RESET_L	L13	RESET*	
PM_SLP_S0_L	M12	SYS_SLEEP*	
PMU_ACTIVE_READY	J5	ACTIVE_RDY	
PMU_CLK32K_SOC_R	H6	CLKOUT0_32K	
PMU_CLK32K_PCH_R	H7	CLKOUT1_32K	
PMU_CLK32K_WLANBT	J7	CLKOUT2_32K	
NC_PMU_CLK32K_GNSS_R	K7	CLKOUT3_32K	
NC_PMU_CLK32K	K8	CLKOUT4_32K	
PMU_SYS_ALIVE	L11	SYS_ALIVE	
PMU_FORCE_DFU	D6	FORCE_DFU	
PMU_INT_L	L9	IRQ*	
I2C_PWR_SCL	M11	SCL	
I2C_PWR_SDA	L10	SDA	
SPMI_CLK	M8	SCLK	
SPMI_DATA	M7	SDATA	
ALL_SYS_PWRGD	K11	SYS_ACTIVE	
PM_PWRBTN_L	C11	SYS_BTN	
PMU_CPU_ISENSE	A16	AMUX_A0	
PMU_CPU_VSENSE	A15	AMUX_A1	
PMU_GPU_CORE_ISENSE	A14	AMUX_A2	
PMU_GPU_CORE_VSENSE	B14	AMUX_A3	
PMU_GPU_FB_ISENSE	C14	AMUX_A4	
PMU_P1V8_WLAN_ISENSE	D15	AMUX_A5	
PMU_CPUDDR_ISENSE	E14	AMUX_A6	
PMU_DDR1V2_ISENSE	F14	AMUX_A7	
NC_PMU_AMUX_AY	J14	AMUX_AY	
PMU_PBUS_BMON_DIS_ISENSE	D13	AMUX_B0	
PMU_PBUS_MAIN_SSD0_ISENSE	E13	AMUX_B1	
PMU_PBUS_MAIN_SSD1_ISENSE	E12	AMUX_B2	
PMU_P3V3_G3W_SSD0_ISENSE	F13	AMUX_B3	
PMU_P3V3_G3W_SSD1_ISENSE	G13	AMUX_B4	
PMU_3V3_X_HI_ISENSE	G14	AMUX_B5	
PMU_3V3_T_HI_ISENSE	H14	AMUX_B6	
PMU_OTHER5V_HI_ISENSE	H13	AMUX_B7	
NC_PMU_AMUX_BY	J13	AMUX_BY	
NC	N9	LS_BID1 (IPU)	
NC	M10	LS_BID2 (IPU)	
PMU_XTAL1	V3	XTAL1	
PMU_XTAL2	V4	XTAL2	
CPU_CATERR_L	L6	SYS_ERR*	
PMU_VDD_MAX	N8	VDD_MAX	
	E6	VDD_OTP	

	L12	IREF	PMU_IREF
	K12	VREF	PMU_VREF
PMU_DROOP_L	L7	VDROOP	
SOC_VDDCPU_SENSE	M5	VDROOP_DET	
CHGR_CBC_ON	D9	CHG_CBC_ON	
CHGR_INT_L	J6	NCHG_INT	
GND	L4	CHG_POK	
PMU_PVDDMAIN_EN	D5	VPWR_EN	
PCH_RTC_RESET_L	M13	LDO1_POK	
NC	D8	PFN	
GND	V6	VIN_BBAT	
PMU_ONOFF_L	N7	(IPU) BUTTON1	
PMU_RSLOC_RST_L	M6	(IPU) BUTTON2	
P3V3MAIN_PGOOD	E9	GPIO1	
NC_P3V3G3W_EN	E8	GPIO2	
NC_P3V3G3W_PGOOD	E7	GPIO3	
P5VG3S_EN	F6	GPIO4	
P5VG3S_PGOOD	F7	GPIO5	
P3V3G3S_EN	F8	GPIO6	
P1V8G3S_EN	F9	GPIO7	
CPUVR_PGOOD	F10	GPIO8	
PVCCIO_EN	G10	GPIO9	
PVCCIO_PGOOD	G9	GPIO10	
PVDDQ_EN	G8	GPIO11	
PVDDQ_PGOOD	G7	GPIO12	
AUD_PWR_EN	G6	GPIO13	
WLAN_PWR_EN	H8	GPIO14	
BT_PWR_EN	H9	GPIO15	
SE_PWR_EN	J9	GPIO16	
SENSOR_PWR_EN	J8	GPIO17	
PVCCPLLOC_EN	K9	GPIO18	
NC_PVCCEOPIOEDRAM_P2V7NAND_PGOOD	K10	GPIO19	
NC_PEARL_P2V7NAND_EN	J10	GPIO20	
NC_NAND_DISCHARGE_HDD_PWR_EN	H10	GPIO21	
NC_NAND_RESET_L_SD_PWR_EN	H11	GPIO22	
NC_NAND_WP_L_ENET_PWR_EN	G11	GPIO23	
TBT_PWR_EN	F11	GPIO24	
P1V1_SLPDDR_SOCFET_EN	E10	GPIO25	

R8012 33 5% 1/20W MF 201
R8011 33 5% 1/20W MF 201
R8010 2.2K 5% 1/20W MF 201
R8001 200K 1% 1/20W MF 201
C8001 0.1UF 10% 6.3V X6S 0201
C8002 22PF 5% 50V C0G 0201
C8003 22PF 5% 50V C0G 0201
C8004 0.1UF 10% 6.3V X6S 0201
R8013 0 1/20W 5% MF 0201
R8018 1M 5% 1/20W MF 201
Y8001 32.768KHZ-20PPM-12.5PF 1.60X1.00-SM NOSTUFF

PMU_CLK32K_SOC
PMU_CLK32K_PCH
SOC_FORCE_DFU

Use SOC's Internal Pull Up

PP1V05_S3
PP3V3_G3H_RTC_X
PP1V8_AWAKE
PP1V8_S5
PP1V8_SLPS2R

R8002 10K PMU_COLD_RESET_L
R8003 10K PMU_SYS_ALIVE
R8006 10K PMU_DROOP_L
R8005 10K ALL_SYS_PWRGD
R8015 10K PMU_ONOFF_L
R8014 10K PMU_RSLOC_RST_L
R8017 51 CPU_CATERR_L
R8007 47K PMU_ACTIVE_READY NOSTUFF

Caution : AMUX programmed with Gain 1 should not have inputs greater than 1.5V

To be Grounded on Portables Only, RC on Coin Cell on Desktops

VDD_HI Threshold Select

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0481	1	RES,MF,649K,1%,1/20W,0201	R8050	CRITICAL	PBUS:2S
118S00077	1	RES,MF,1.15M,1%,1/16W,0201	R8050	CRITICAL	PBUS:3S
118S00077	1	RES,MF,1.15M,1%,1/16W,0201	R8050	CRITICAL	PBUS:12V

PPBUS_G3H
R8050 1.15M 1% 1/20W TK 0201 OMIT_TABLE
PMU_VDD_HI
C8051 220PF 10% 16V CER-X7R 0201 NOSTUFF
R8051 357K 1% 1/20W MF 201

PBUS	Rising Vth	Falling Vth
2S	6.059V	5.636V
3S	9.076V	8.443V
12V	9.076V	8.443V

BOM_COST_GROUP=SOC

PAGE TITLE: PMIC GPIOs & Control
Apple Inc.
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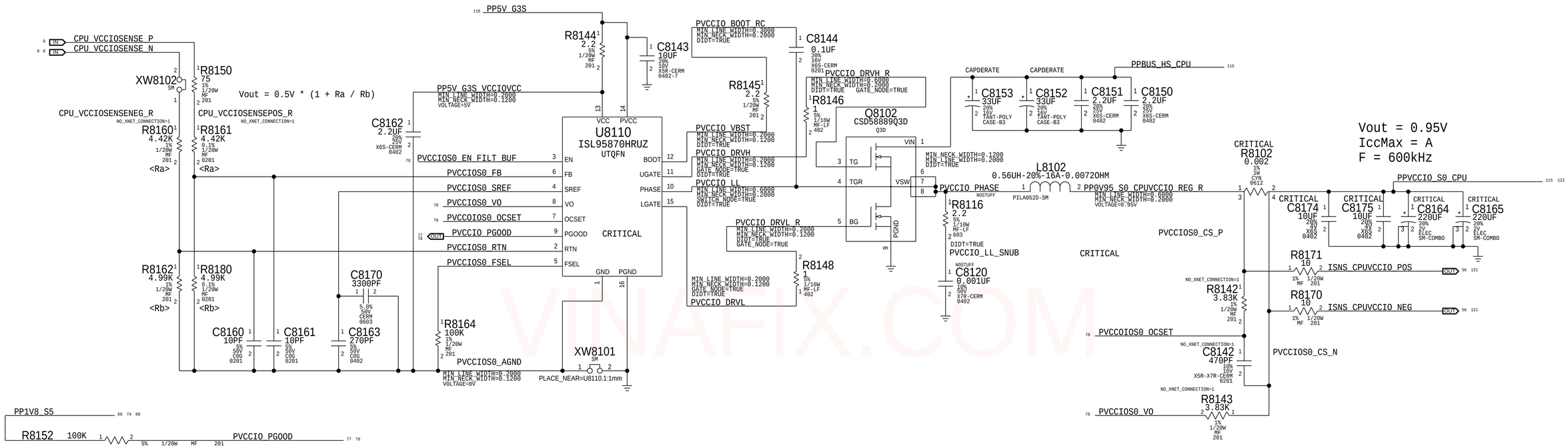
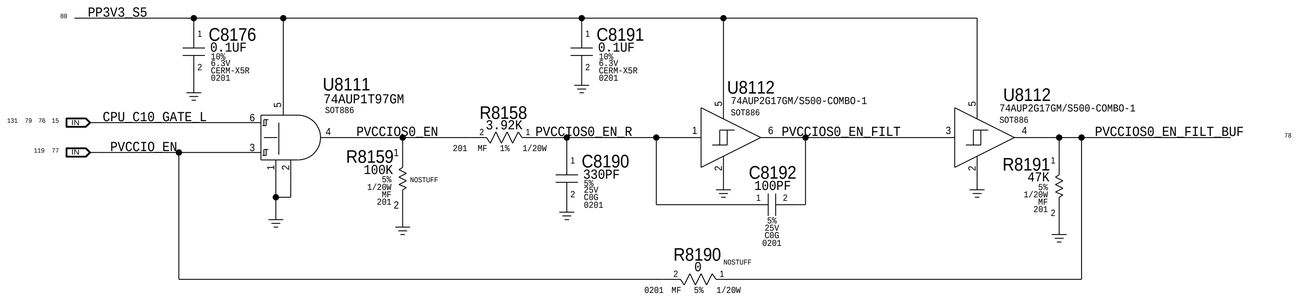
0.95V VCCIO



VCCIO ENABLE LOGIC



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: VR VCCIO

Apple Inc.

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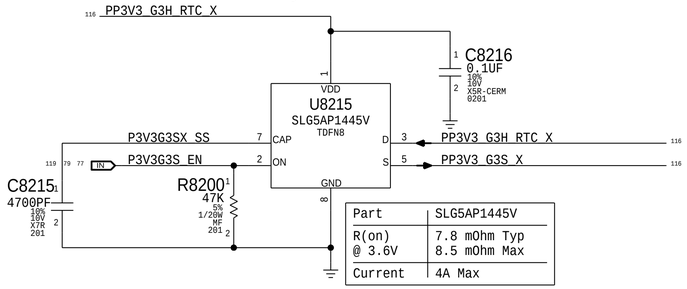
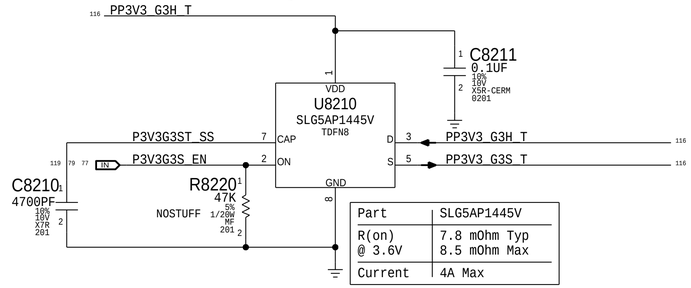
3.3V G3 Standby Switch X



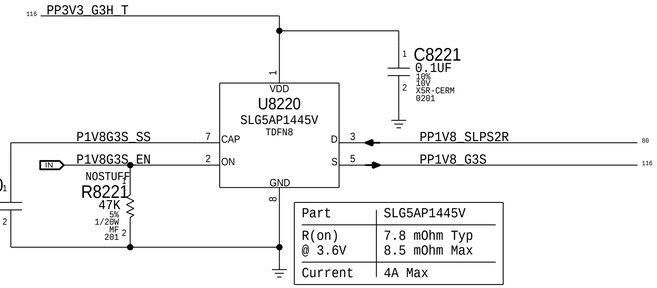
Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

3.3V G3 Standby Switch T



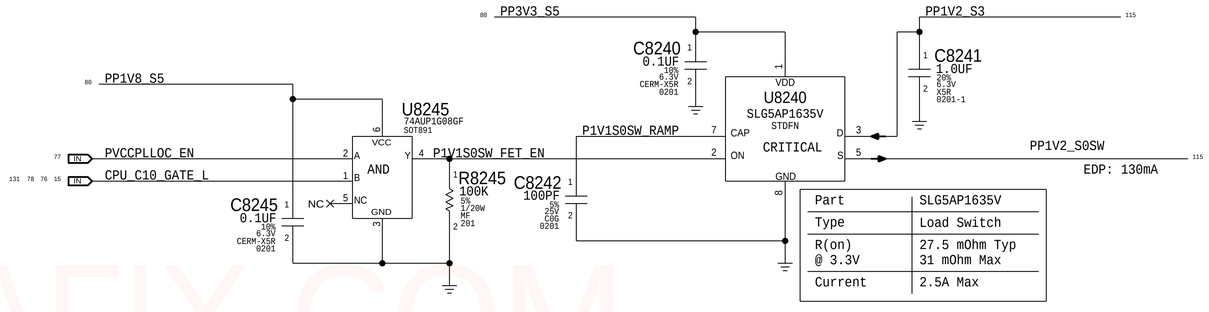
Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

1.8V G3 Standby Switch



Part	SLG5AP1445V
R(on) @ 3.6V	7.8 mOhm Typ 8.5 mOhm Max
Current	4A Max

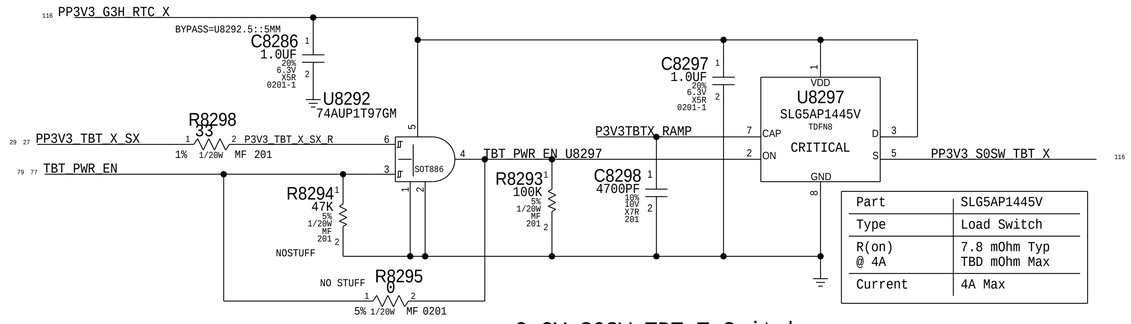
1.1V S0SW VCCPLL_OC Switch



Part	SLG5AP1635V
Type	Load Switch
R(on) @ 3.3V	27.5 mOhm Typ 31 mOhm Max
Current	2.5A Max

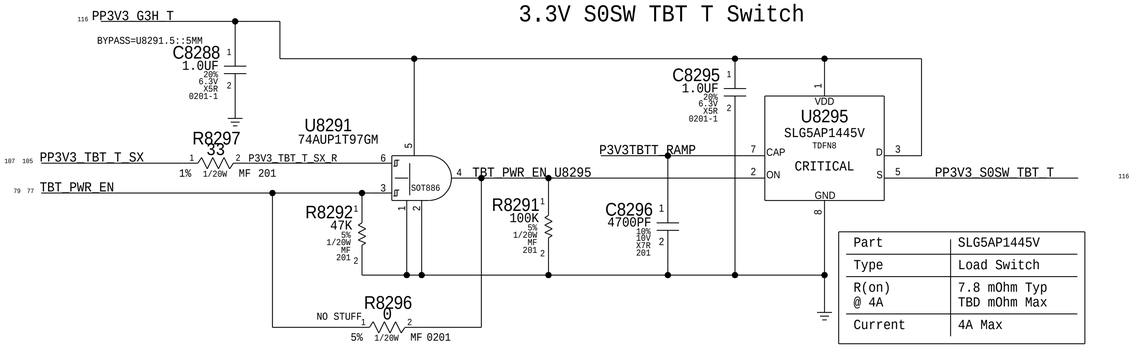
VCCPLL_OC has turn-on requirement of
11uS min and 240uS max
from EN to 1.1V

3.3V S0SW TBT X Switch



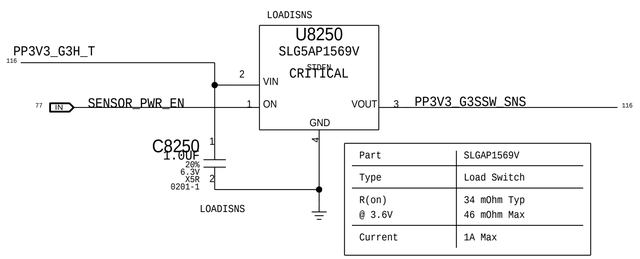
Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

3.3V S0SW TBT T Switch



Part	SLG5AP1445V
Type	Load Switch
R(on) @ 4A	7.8 mOhm Typ TBD mOhm Max
Current	4A Max

3.3V Sensor Switch



Part	SLGAP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=SILU

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
PAGE: 82 OF 200
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PMIC Buck0 - SoC VDD_CPU

122 75 PPVDDCPU_AWAKE
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.06V
MAKE_BASE=TRUE
119
PPVDDCPU_AWAKE
42 80

PMIC Buck1 - SoC VDD_CPU_SRAM

122 75 PPVDDCPUSRAM_AWAKE
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.06V
MAKE_BASE=TRUE
119
PPVDDCPUSRAM_AWAKE
42

PMIC Buck2 - SoC VDD_SOC

75 PP0V82_SLPDDR
MIN_LINE_WIDTH=0.7000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.82V
MAKE_BASE=TRUE
119
PP0V82_SLPDDR
42 80

PMIC BUCK3 - SoC AOP/SMC/VDD1

131 122 75 PP1V8_SLPS2R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
119
PP1V8_SLPS2R
75
PP1V8_SLPS2R
79
PP1V8_SLPS2R
76
PP1V8_SLPS2R
46
PP1V8_SLPS2R
77
PP1V8_SLPS2R
64
PP1V8_SLPS2R
46
PP1V8_SLPS2R
38 47
PP1V8_SLPS2R
44
PP1V8_SLPS2R
44
PP1V8_SLPS2R
44
PP1V8_SLPS2R
44
PP1V8_SLPS2R
68
PP1V8_SLPS2R
51
PP1V8_SLPS2R
51
PP1V8_SLPS2R
51
PP1V8_SLPS2R
47
PP1V8_SLPS2R
29 107
PP1V8_SLPS2R
67
PP1V8_SLPS2R
126 131
PP1V8_SLPS2R
107

PMIC BUCK3 SW 1

131 75 PP1V8_AWAKE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
119
PP1V8_AWAKE
77
PP1V8_AWAKE
46
PP1V8_AWAKE
44
PP1V8_AWAKE
44
PP1V8_AWAKE
44
PP1V8_AWAKE
44
PP1V8_AWAKE
44
PP1V8_AWAKE
41 46 47
PP1V8_AWAKE
46
PP1V8_AWAKE
66
PP1V8_AWAKE
126

PMIC BUCK3 SW 3

75 PP1V8_S5
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE
119
PP1V8_S5
46
PP1V8_S5
16 17
PP1V8_S5
39
PP1V8_S5
12 16
PP1V8_S5
12 13 15 16 19 20 52
PP1V8_S5
15
PP1V8_S5
126
PP1V8_S5
17
PP1V8_S5
PP1V8_S5
12 36 77
PP1V8_S5
51
PP1V8_S5
51
PP1V8_S5
46
PP1V8_S5
94
PP1V8_S5
PP1V8_S5
69 74 78
PP1V8_S5
93
PP1V8_S5
79
PP1V8_S5
74
PP1V8_S5
16
PP1V8_S5
57
PP1V8_S5
57
PP1V8_S5
57
PP1V8_S5
46
PP1V8_S5
18

PMIC BUCK3 SW 4/5

75 NC_PP1V8_S3
NC_PP1V8_S3
MAKE_BASE=TRUE
NO_TEST=1
75 NC_PP1V8_S0
NC_PP1V8_S0
MAKE_BASE=TRUE
NO_TEST=1

PMIC Buck4 - SDRAM VDD2

122 75 PP1V1_SLPS2R
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V
MAKE_BASE=TRUE
119
PP1V1_SLPS2R
76
PP1V1_SLPS2R
76
PP1V1_SLPS2R
43
PP1V1_SLPS2R
44

Buck 4 Ext. SW U7901 - VDDIO_DDR & PLL

76 PP1V1_SLPDDR
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V
MAKE_BASE=TRUE
119
PP1V1_SLPDDR
38
PP1V1_SLPDDR
43
PP1V1_SLPDDR
43
PP1V1_SLPDDR
44

PMIC Buck5 - VDD_FIXED

122 75 PP0V9_SLPDDR
MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.9V
MAKE_BASE=TRUE
119
PP0V9_SLPDDR
43
PP0V9_SLPDDR
43
PP0V9_SLPDDR
43
PP0V9_SLPDDR
43
PP0V9_SLPDDR
43

PMIC LDO0 - VDD_LOW

76 PP0V8_SLPS2R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=0.8V
MAKE_BASE=TRUE
119
PP0V8_SLPS2R
43

PMIC LDO2 - PCIE_REFBUF/PLL

76 PP1V2_AWAKE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.2V
MAKE_BASE=TRUE
119
PP1V2_AWAKE
44
PP1V2_AWAKE
44
PP1V2_AWAKE
44
PP1V2_AWAKE
44

PMIC V3P3 SW 1 - USB

76 PP3V3_AWAKE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE
PP3V3_AWAKE
44

PMIC V3P3 SW 2 (Internal) -

76 PP3V3_S5
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1750
VOLTAGE=3.3V
MAKE_BASE=TRUE
119
PP3V3_S5
12 16 17
PP3V3_S5
46
PP3V3_S5
78
PP3V3_S5
15 16 19
PP3V3_S5
14 16
PP3V3_S5
15 16
PP3V3_S5
18
PP3V3_S5
20
PP3V3_S5
12 16 17
PP3V3_S5
79
PP3V3_S5
12
PP3V3_S5
93 124
PP3V3_S5
126 131
PP3V3_S5
16
PP3V3_S5

PMIC LDO 1 - PCH VCCRTC

76 PP3V0_G3H_RTC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.0V
MAKE_BASE=TRUE
119
PP3V0_G3H_RTC
12 16 17

NC Aliases

77 NC_PVCCEOPIOEDRAM_P2V7NAND_PGOOD
MAKE_BASE
NO_TEST
NC_PVCCEOPIOEDRAM_P2V7NAND_PGOOD
77 NC_PEARL_P2V7NAND_EN
MAKE_BASE
NO_TEST
NC_PEARL_P2V7NAND_EN
77 NC_NAND_DISCHARGE_HDD_PWR_EN
MAKE_BASE
NO_TEST
NC_NAND_DISCHARGE_HDD_PWR_EN
77 NC_NAND_RESET_L_SD_PWR_EN
MAKE_BASE
NO_TEST
NC_NAND_RESET_L_SD_PWR_EN
77 NC_NAND_WP_L_ENET_PWR_EN
MAKE_BASE
NO_TEST
NC_NAND_WP_L_ENET_PWR_EN
77 NC_P3V3G3W_PGOOD
MAKE_BASE
NO_TEST
NC_P3V3G3W_PGOOD
77 NC_P3V3G3W_EN
MAKE_BASE
NO_TEST
NC_P3V3G3W_EN

Alternate Feedback Sesne

NOSTUFF
R8320
0
5%
1/16W
MF-LF
402
PLACE_NEAR=R7806.1:5MM
XW8320
SM
75 OUT PVDDCPUAWAKE_FB
Buck0 - Remote
PVDDCPUAWAKE_FB_R
PLACE_NEAR=U3900.AA12:4MM
PVPDDCPU_AWAKE
42 80

NOSTUFF
R8321
0
5%
1/16W
MF-LF
402
PLACE_NEAR=R7812.1:5MM
XW8321
SM
75 OUT P0V8SLPDDR_FB
Buck2 - Remote
P0V8SLPDDR_FB_R
PLACE_NEAR=U3900.AA20:6MM
PP0V82_SLPDDR
42 80

R8322
0
5%
1/16W
MF-LF
402
PLACE_NEAR=R7820.2:5MM
XW8322
SM
75 OUT PVCCPRIMCORE_FB
Buck8 - Remote
PVCCPRIMCORE_FB_R
PLACE_NEAR=U1200.AB12:4MM
PP1V05_PRIM
16 17 115

NC_CHGR_AUX_OK
NO_TEST=1
MAKE_BASE
NC_CHGR_AUX_OK
68
119 18 PM_PWRBTN_L
MAKE_BASE
PM_PWRBTN_L
12 77
119 77 CPUVR_PGOOD
MAKE_BASE
CPUVR_PGOOD
69
46 8 CPU_VCCST_PWRGD
MAKE_BASE
CPU_VCCST_PWRGD
69
NC_PMU_CLK32K
NO_TEST=1
MAKE_BASE
NC_PMU_CLK32K
77
NC_PMU_AMUX_BY
NO_TEST=1
MAKE_BASE
NC_PMU_AMUX_BY
77
NC_PMU_AMUX_AY
NO_TEST=1
MAKE_BASE
NC_PMU_AMUX_AY
77

77 GND
MAKE_BASE
77 GND
MAKE_BASE

PAGE TITLE
SOC/PMIC Aliases
Apple Inc.
DRAWING NUMBER
051-02643
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REVISION
4.0.0
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Page Notes

Power aliases required by this page:

- +PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- +PP5V_G3S_BKLT (5V BACKLIGHT DRIVER INPUT)

PBUS LINE WIDTHS

PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

LCD BKLT LINE WIDTHS

BOM_COST_GROUP=DISPLAY

VOUT = 52V TYP, 59V MAX
IOUT = 0.135A TYP, 0.15A MAX
FS = 625KHZ TYP (+/- 7%)

PAGE TITLE	LCD Backlight Driver
Apple Inc.	DRAWING NUMBER 051-02643 · SIZE D
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LCD PANEL INTERFACE (eDP) + Camera (MIPI)

MIPIC FILTERING

PP5V_G3S
CRITICAL
U8500 SLG5AP1443V TDFN
R8515 150K 1% 1/20W MF 201
LCD_PWR_SLEW
PANEL_P5V_EN
VOLTAGE=5V
PP5V_S0SW_LCD
R8517 330 5% 1/20W MF 201
PANEL_P5V_EN_D
D8517 SC2 DSF01S30SCAP
C8515 0.1UF 10% 10V X5R-CERM 0201
C8509 4700PF 10% 10V X7R 201
C8511 0.1UF 10% 10V X5R-CERM 0201
C8512 10UF 20% 10V X5R-CERM 0402-7
PP3V3_G3H_RTC_X
CRITICAL
U8501 SLG5AP1443V TDFN
R8516 200K 1% 1/20W MF 201
PANEL_P3V3_EN
LCD_PWR_SLEW_3V3
VOLTAGE=3.3V
PP3V3_S0SW_LCD_R
C8516 0.47UF 10% 6.3V CERM-X5R 0201
C8513 4700PF 10% 10V X7R 201
C8510 1.0UF 20% 6.3V X5R 0201-1
R8518 330 5% 1/20W MF 201
PANEL_P3V3_EN_D
D8518 SC2 DSF01S30SCAP
ISNS_LCDPANEL_P
ISNS_LCDPANEL_N
SENSOR:DEV
R8520 0.01 1% 1/3W MF 0306
NO_XNET_CONNECTION=1
PP3V3_S0SW_LCD
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3V

L8502 3.25-OHM-0.1A-2.4GHZ TAM0605-4SM PLACE_NEAR=J8500.33:5mm
MIPI_FTCAM_DATA_ISOL_P<0> ↔ MIPI_FTCAM_DATA_CONN_P<0>
MIPI_FTCAM_DATA_ISOL_N<0> ↔ MIPI_FTCAM_DATA_CONN_N<0>
L8503 3.25-OHM-0.1A-2.4GHZ TAM0605-4SM PLACE_NEAR=J8500.39:5mm
MIPI_FTCAM_CLK_ISOL_P ↔ MIPI_FTCAM_CLK_CONN_P
MIPI_FTCAM_CLK_ISOL_N ↔ MIPI_FTCAM_CLK_CONN_N
L8504 FERR-120-OHM-1.5A 0402A
PP5V_G3S → PP5V_S0_ALSCAM_F
VOLTAGE=5V
C8504 0.1UF 10% 10V X5R-CERM 0201
PPVOUT_S0_LCDBKLT
C8500 1000PF 10% 100V X7R-CERM 0603
LCD Panel HPD & AUX strapping
PP3V3_G3H_RTC_X
NO_XNET_CONNECTION=1
R8503 1M 5% 1/20W MF 201 NOSTUFF
EDP_INT_AUX_N
EDP_INT_AUX_P
NO_XNET_CONNECTION=1
R8502 1M 5% 1/20W MF 201 NOSTUFF
PP3V3_S0SW_LCD
R8508 10K 5% 1/20W MF 201 NOSTUFF
BKLT_PWM_MLB2TCON
R8507 10K 5% 1/20W MF 201

J8500 20759-042E-02 F-ST-SM

PPVOUT_S0_LCDBKLT	43	44	PP3V3_S0SW_LCD
EDP_INT_AUX_N	1	2	
EDP_INT_AUX_P	3	4	EDP_PANEL_PWR_BUF_EN
	5	6	DP_INT_HPD
EDP_INT_ML_N<0>	7	8	LCD_FSS
EDP_INT_ML_P<0>	9	10	TP_LCD_IRQ_L
	11	12	
EDP_INT_ML_N<1>	13	14	✕ NC (TCON PWM is NCed)
EDP_INT_ML_P<1>	15	16	BKLT_PWM_MLB2TCON
	17	18	
EDP_INT_ML_N<2>	19	20	
EDP_INT_ML_P<2>	21	22	
	23	24	I2C_BKLT_SDA
EDP_INT_ML_N<3>	25	26	I2C_BKLT_SCL
EDP_INT_ML_P<3>	27	28	I2C_TCON_SDA
	29	30	I2C_TCON_SCL
MIPI_FTCAM_DATA_CONN_N<0>	31	32	
MIPI_FTCAM_DATA_CONN_P<0>	33	34	I2C_ALS_SDA
	35	36	I2C_ALS_SCL
MIPI_FTCAM_CLK_CONN_N	37	38	I2C_CAM_ISOL_SCL
MIPI_FTCAM_CLK_CONN_P	39	40	I2C_CAM_ISOL_SDA
	41	42	
PP5V_S0SW_LCD	45	46	PP5V_S0_ALSCAM_F
	47	48	
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	

EDP_PANEL_PWR_DLY_EN
DP_INT_HPD
R8551 100K 5% 1/20W MF 201

PP3V3_G3H_RTC_X
R8570 100K 5% 1/20W MF 201
R8571 100K 5% 1/20W MF 201
C8570 0.1UF 10% 10V X5R-CERM 0201 BYPASS=U8510::2mm
PM_SLP_TIEOFF
U8510 SLG4AP4998 STQFN
EDP_PANEL_PWR_EN
EDP_PANEL_PWR_BUF_EN
SMCRST_TIEOFF
NC
NC
NC
NC
NC

PP3V3_G3S_X
C8502 0.1UF 10% 10V X5R-CERM 0201 BYPASS=U8502::2mm
U8502 NX3DV642GU QFN-COMBO
Resistor needed?

MIPI_FTCAM_CLK_P	CLK+	CLK2+	MIPI_FTCAM_CLK_ISOL_P
MIPI_FTCAM_CLK_N	CLK-	CLK2-	MIPI_FTCAM_CLK_ISOL_N
MIPI_FTCAM_DATA_P<0>	1D+	2D+	MIPI_FTCAM_DATA_ISOL_P<0>
MIPI_FTCAM_DATA_N<0>	1D-	2D-	MIPI_FTCAM_DATA_ISOL_N<0>
I2C_FTCAM_SDA	2D+	2D2+	I2C_CAM_ISOL_SDA
I2C_FTCAM_SCL	2D-	2D2-	I2C_CAM_ISOL_SCL

HOST SIDE
PP1V8_G3S
R8510 100K 5% 1/20W MF 201
R8511 100K 5% 1/20W MF 201
PP3V3_G3S_X
R8505 100K 5% 1/20W MF 201 NOSTUFF
R8544 0 5% 1/20W MF 0201
SEP_CAM_DISABLE_DFF_L
SEP_CAM_DISABLE_DFF_R_L

S	OUTPUT
L	Camera Disable
H	Camera Enable

Alternate: OnSemi FSA642 (353S01346)

I2C pulls needed on both sides???
PP3V3_S0SW_LCD
PP5V_S0SW_LCD
PP5V_S0_ALSCAM_F
I2C_BKLT_SDA
I2C_BKLT_SCL
C8550 12PF 5% 25V NP0-C0G 0201
C8551 12PF 5% 25V NP0-C0G 0201
C8552 12PF 5% 25V NP0-C0G 0201
C8553 12PF 5% 25V NP0-C0G 0201 NOSTUFF
C8554 12PF 5% 25V NP0-C0G 0201 NOSTUFF

BOM_COST_GROUP=DISPLAY

PAGE TITLE: eDP Display Connector
Apple Inc.
DRAWING NUMBER: 051-02643
SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
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S4E0

PP1V8_SSD0
C8632 10UF 20% 6.3V CERM-X6S 0402 CRITICAL
C8636 4.3UF 20% 4V CERM 0402-THICKSTNCL CRITICAL
C8637 2.2UF 20% 6.3V X5R-CERM 0201
PP2V5_NAND_SSD0
C8648 10UF 20% 6.3V CERM-X6S 0402 CRITICAL
C8649 2.2UF 20% 6.3V X5R-CERM 0201
C8650 2.2UF 20% 6.3V X5R-CERM 0201
PP0V9_SSD0
SSD0_S4E0_VPP
NOSTUFF R8630 0 5% 1/20W MF 201
U8600
KLAFGAKWCM-E0T2
ULGA-COMBO
OMIT_TABLE
CRITICAL
VPP F3
VDD_PLL R4
VCC R2 L12 G4 E12 D3
VDDIO P9 T5 N2 K9 J2 E10 E2
VDD R8 R6 L8 L6 G8 G6
ANI_VREF H4
ANO_VREF G12
AVDD18_PLL L2
PCI_VDD_2 J8
PCI_VDD_1 H8
PCI_AVDD_H J6
PCI_AVDD_CLK_2 H9
PCI_AVDD_CLK_1 H6
TP_SSD0_S4E0_ANI1_VREF
TP_SSD0_S4E0_ANO0_VREF
PP1V8_SSD0_S4E0_AVDD18_PLL
PP1V8_SSD0_S4E0_PCI_AVDD_H
PP0V9_SSD0
SSD0_OCARINA_LPB_L B3 EXT_D0/BOOT0
SSD_BFH C4 EXT_D1/BOOT1
SSD0_S4E_BOOT2 B5 EXT_D2/BOOT2/SPINAND_SCLK
SSD0_S4E0_SWD_UID0 C6 EXT_D3/SWD_UID0/SPINAND_MISO
SSD0_S4E_UART_RX B7 EXT_D4/UART_RX
SSD0_S4E0_SWD_UID1 C8 EXT_D5/SWD_UID1/SPINAND_MOSI
SSD0_S4E0_UART_TX B9 EXT_D6/UART_TX
SSD0_OCARINA_PFN B11 EXT_D7/SPF
SSD0_PCIE_RESET_L E8 EXT_NCE/PERST*
SSD0_SWDIO_UART_D2R D7 EXT_NRE/JTAG_TMS
SSD0_SWCLK_UART_R2D E6 EXT_NWE/JTAG_TCK
SSD0_S4E0_JTAG_TDO E4 EXT_RNB/JTAG_TDO
TPA8601 TP-P6 SSD0_S4E0_JTAG_TDI D5 EXT_CLE/JTAG_TDI
SSD0_S4E_JTAG_SEL D9 EXT_ALE/JTAG_SEL
SSD0_S4E0_DROOP_L T3 DROOP_N
SSD0_OCARINA_WP_L G2 WP_N
VSS
PP1V8_SSD0
NOSTUFF
R8602 4.7K 1% 1/20W MF 201
R8603 4.7K 1% 1/20W MF 201
SSD0_OCARINA_PFN
SSD0_S4E0_DROOP_L
SSD0_S4E_BOOT2
SSD0_S4E0_SWD_UID0
SSD0_S4E0_SWD_UID1
R8620 100K 1% 1/20W MF 201
R8608 100K 1% 1/20W MF 201
R8609 100K 1% 1/20W MF 201
C8610 10UF 20% 6.3V CERM-X6S 0402 CRITICAL
C8611 2.2UF 20% 6.3V X5R-CERM 0201
C8612 2.2UF 20% 6.3V X5R-CERM 0201
C8613 0.1UF 10% 16V X5R-CERM 0201
C8614 0.1UF 10% 16V X5R-CERM 0201
C8615 0.1UF 10% 16V X5R-CERM 0201
PP0V9_SSD0
R8601 0 5% 1/20W MF 0201
PP1V8_SSD0
C8646 1.0UF 20% 10V X5R-CERM 0201-1
C8647 0.1UF 10% 16V X5R-CERM 0201
R8699 0 5% 1/20W MF 0201
C8644 1.0UF 20% 10V X5R-CERM 0201-1
C8645 0.1UF 10% 16V X5R-CERM 0201
R8640 100 1% 1/20W MF 201
SSD0_CLK24M
CLK_IN M3 SSD0_CLK24M_01
PCIE_REFCLK_P K11 PCIE_CLK100M_SSD0_01_P
PCIE_REFCLK_M J12 PCIE_CLK100M_SSD0_01_N
PCIE_CLKREQ_N P5 SSD0_CLKREQ0_L
PCI_RESREF H7 SSD0_S4E0_PCIE_RESREF
C8603 0.22UF 20% 6.3V X5R-CERM 0201
C8604 0.22UF 20% 6.3V X5R-CERM 0201
C8601 0.22UF 20% 6.3V X5R-CERM 0201
C8602 0.22UF 20% 6.3V X5R-CERM 0201
R8604 3.01K 1% 1/20W MF 201
PCIE_RX0_P M11 PCIE_SSD0_R2D_P<0>
PCIE_RX0_M N12 PCIE_SSD0_R2D_N<0>
PCIE_TX0_P R12 PCIE_SSD0_D2R_C_P<0>
PCIE_TX0_M T11 PCIE_SSD0_D2R_C_N<0>
PCIE_SSD0_R2D_C_P<0>
PCIE_SSD0_R2D_C_N<0>
PCIE_SSD0_D2R_P<0>
PCIE_SSD0_D2R_N<0>
RESET* L4 SSD0_OCARINA_RESET_L
TRST* G10 SSD0_S4E_JTAG_TRST_L
ZQ_C K3 SSD0_S4E0_ZQ_C
ZQ_N C10 SSD0_S4E0_ZQ_L
PLACE_NEAR=U8600.C10:5mm
R8605 300 1% 1/20W MF 201
R8606 100 1% 1/20W MF 201
R8600 100K 1% 1/20W MF 201
BOM_COST_GROUP=SDD

SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017
PAGE TITLE: SSD0 S4E 0
Apple Inc.
DRAWING NUMBER 051-02643 SIZE D
REVISION 4.0.0
BRANCH evt-0
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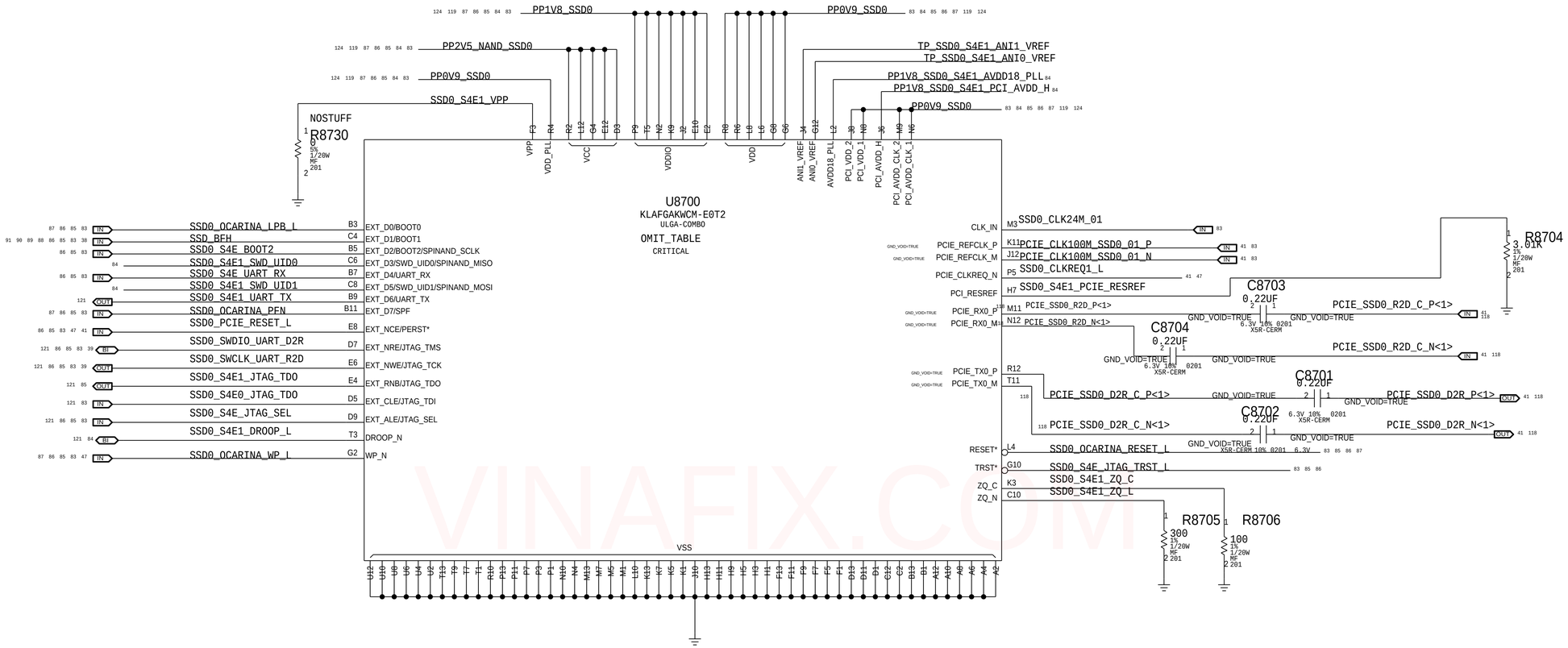
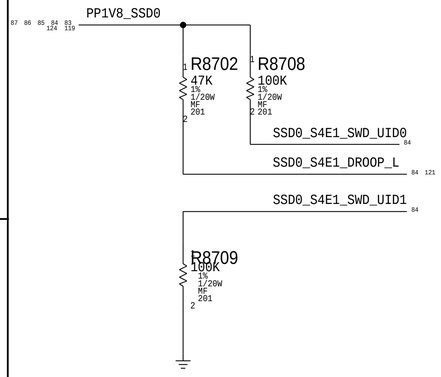
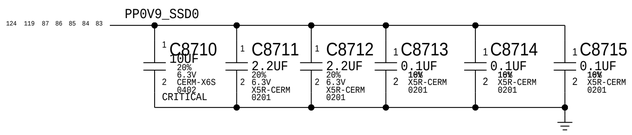
S4E1

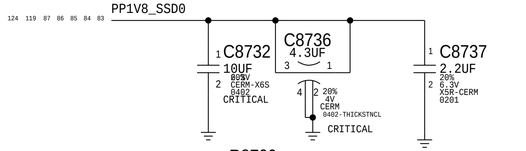




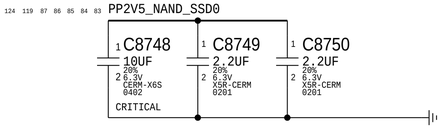
S4E VDD

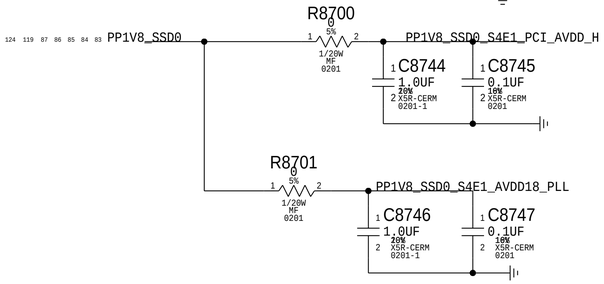


S4E VDDIO



VCC CAP





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SYNC_MASTER=J137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE: SSD0 S4E 1

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D
REVISION: 4.0.0
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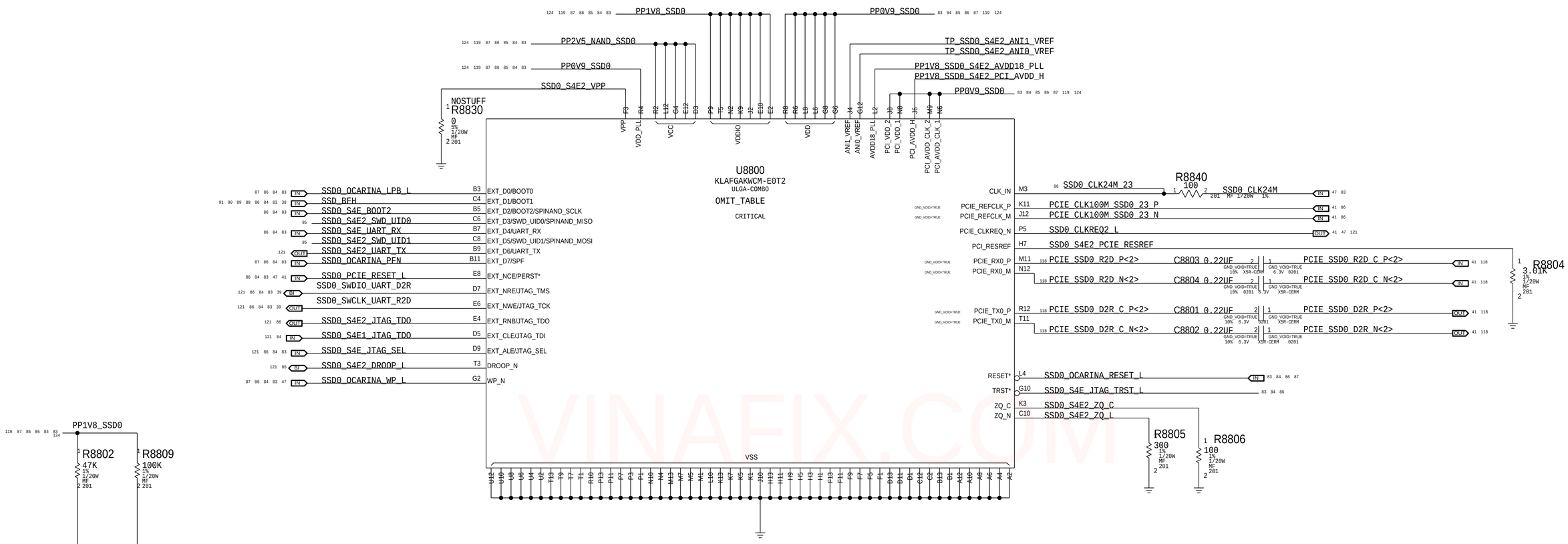
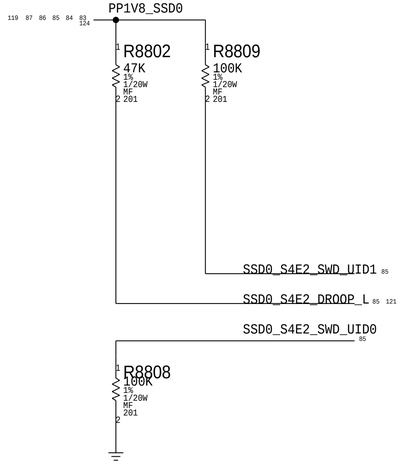
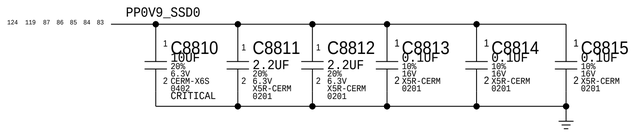
S4E2





S4E VDD



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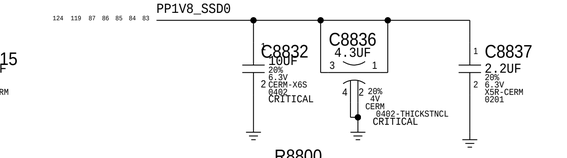

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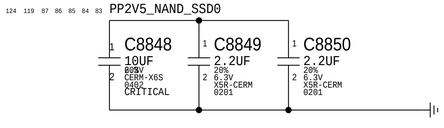

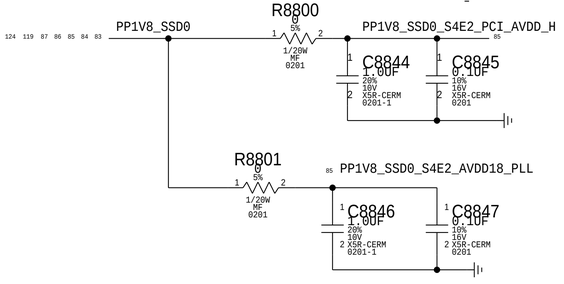

BOM_COST_GROUP=SDD

SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE: SSD0 S4E 2

Apple Inc.

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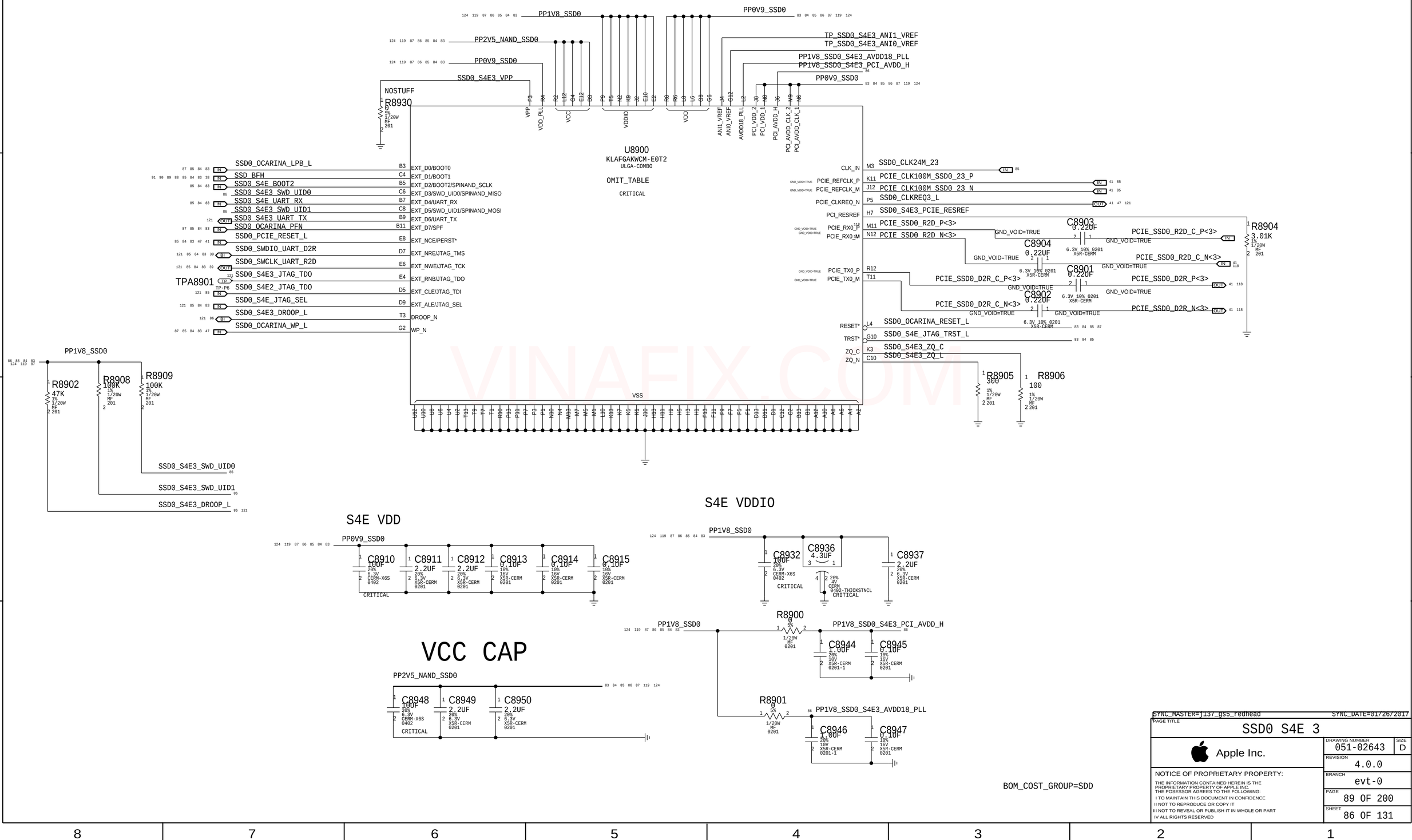
S4E3



SYNC_MASTER=J137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE: SSD0 S4E 3

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D

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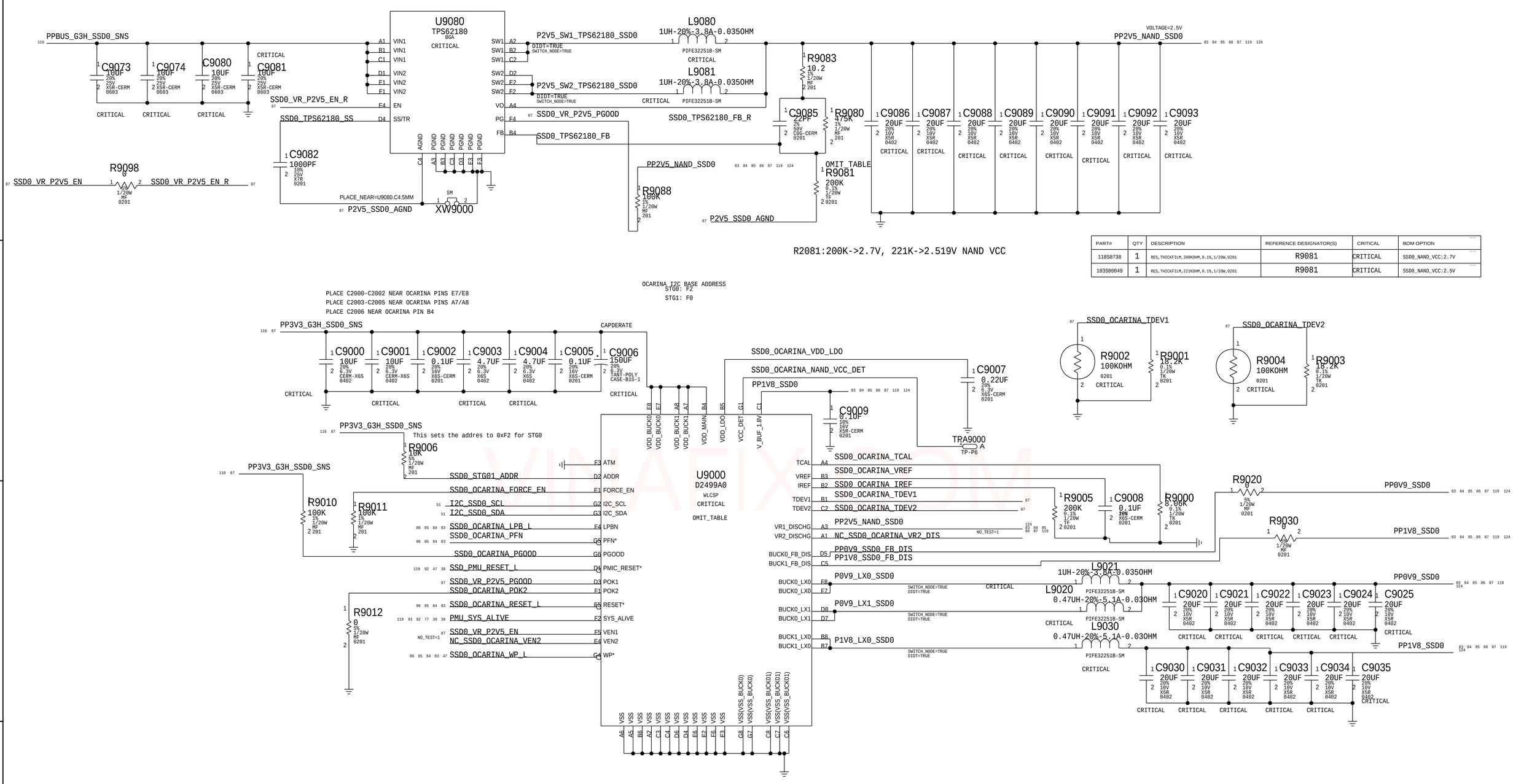

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0738	1	RES,THICKFILM,200KOHM,0.1%,1/20W,0201	R9081	CRITICAL	SSD0_NAND_VCC:2.7V
103S00049	1	RES,THICKFILM,221KOHM,0.1%,1/20W,0201	R9081	CRITICAL	SSD0_NAND_VCC:2.5V

SYNC_MASTER=J137_GS5_redhead SYNC_DATE=01/26/2017

PAGE TITLE: SSD0 PMIC & VR

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D

REVISION: 4.0.0

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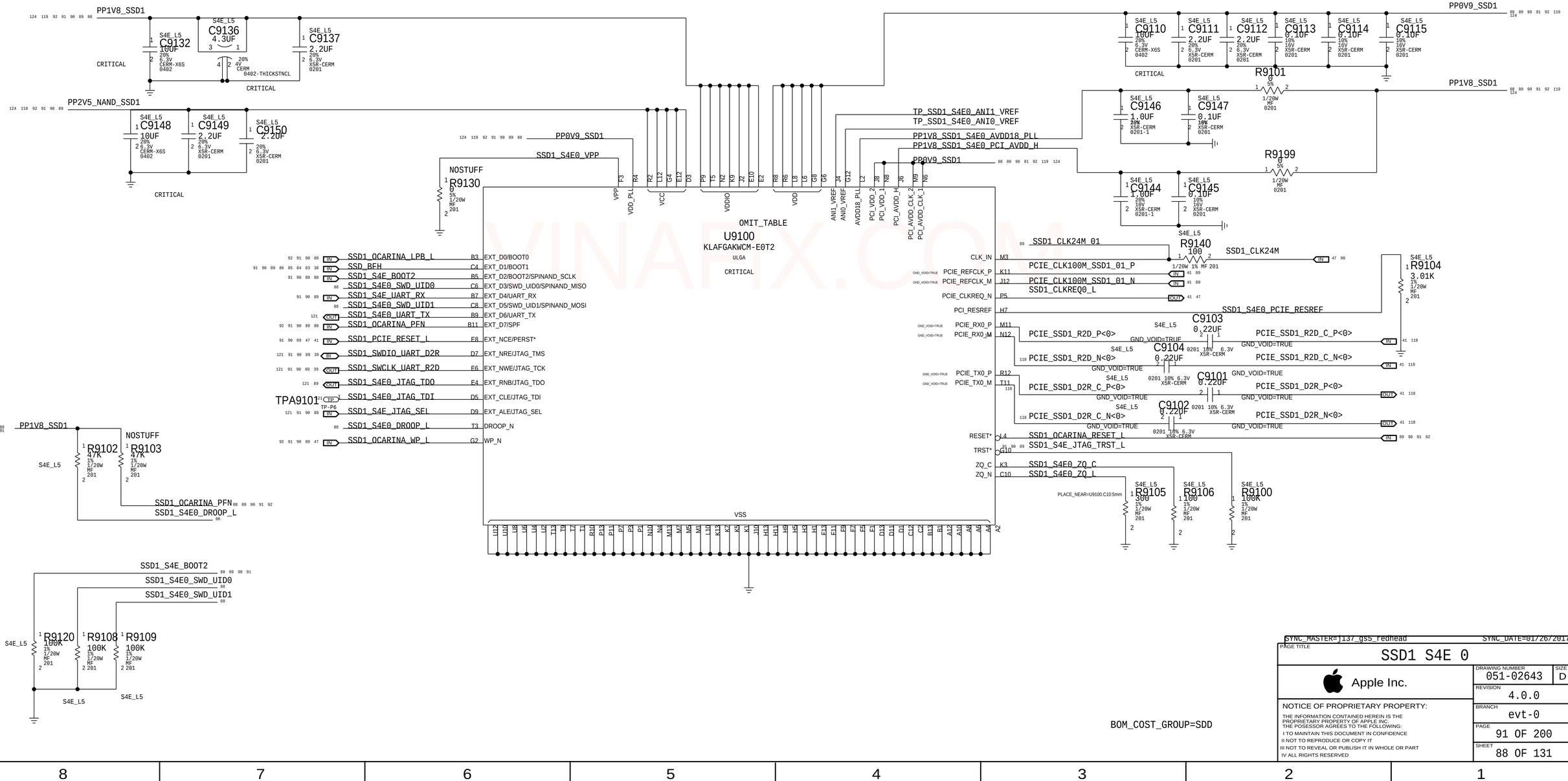
S4E0

VCC CAP



SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017

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S4E1

PP1V8_SSD1
PP2V5_NAND_SSD1
PP0V9_SSD1
SSD1_S4E1_VPP
NOSTUFF
R9230 0 5% 1/20W MF 201
VPP F3
VDD_PLL R4
VCC R2 L12 G4 E12 D3
VDDIO P9 T5 N2 K9 J2 E10
VDD R8 K6 L8 L6 G8 G6
ANI_VREF J4
AVD_VREF G12
AVDD18_PLL L2
PCI_VDD_2 J8
PCI_VDD_1 N8
PCI_AVDD_H J6
PCI_AVDD_CLK_2 M9
PCI_AVDD_CLK_1 N6
PP0V9_SSD1
TP_SSD1_S4E1_ANI1_VREF
TP_SSD1_S4E1_ANI0_VREF
PP1V8_SSD1_S4E1_AVDD18_PLL
PP1V8_SSD1_S4E1_PCI_AVDD_H
PP0V9_SSD1

OMIT_TABLE
U9200
KLAFGAKWCM-E0T2
ULGA
CRITICAL

SSD1_OCARINA_LPB_L → B3 EXT_D0/BOOT0
SSD_BFH → C4 EXT_D1/BOOT1
SSD1_S4E_BOOT2 → B5 EXT_D2/BOOT2/SPINAND_SCLK
SSD1_S4E1_SWD_UID0 → C6 EXT_D3/SWD_UID0/SPINAND_MISO
SSD1_S4E_UART_RX → B7 EXT_D4/UART_RX
SSD1_S4E1_SWD_UID1 → C8 EXT_D5/SWD_UID1/SPINAND_MOSI
SSD1_S4E1_UART_TX → B9 EXT_D6/UART_TX
SSD1_OCARINA_PFN → B11 EXT_D7/SPF
SSD1_PCIE_RESET_L → E8 EXT_NCE/PERST*
SSD1_SWDIO_UART_D2R → D7 EXT_NRE/JTAG_TMS
SSD1_SWCLK_UART_R2D → E6 EXT_NWE/JTAG_TCK
SSD1_S4E1_JTAG_TDO → E4 EXT_RNB/JTAG_TDO
SSD1_S4E0_JTAG_TDO → D5 EXT_CLE/JTAG_TDI
SSD1_S4E_JTAG_SEL → D9 EXT_ALE/JTAG_SEL
SSD1_S4E1_DROOP_L → T3 DROOP_N
SSD1_OCARINA_WP_L → G2 WP_N

CLK_IN M3 ← SSD1_CLK24M_01
PCIE_REFCLK_P K11 ← PCIE_CLK100M_SSD1_01_P
PCIE_REFCLK_M J12 ← PCIE_CLK100M_SSD1_01_N
PCIE_CLKREQ_N P5 ← SSD1_CLKREQ1_L
PCI_RESREF H7 ← SSD1_S4E1_PCIE_RESREF
PCIE_RX0_P M11 ← PCIE_SSD1_R2D_P<1>
PCIE_RX0_M N12 ← PCIE_SSD1_R2D_N<1>
PCIE_TX0_P R12 → PCIE_SSD1_R2D_C_P<1>
PCIE_TX0_M T11 → PCIE_SSD1_R2D_C_N<1>
RESET* L4 ← SSD1_OCARINA_RESET_L
TRST* G10 ← SSD1_S4E_JTAG_TRST_L
ZQ_C K3 ← SSD1_S4E1_ZQ_C
ZQ_N C10 ← SSD1_S4E1_ZQ_L

PCIE_SSD1_R2D_C_P<1> → C9203 0.22UF → PCIE_SSD1_R2D_C_P<1>
PCIE_SSD1_R2D_C_N<1> → C9204 0.22UF → PCIE_SSD1_R2D_C_N<1>
PCIE_SSD1_D2R_C_P<1> → C9201 0.22UF → PCIE_SSD1_D2R_P<1>
PCIE_SSD1_D2R_C_N<1> → C9202 0.22UF → PCIE_SSD1_D2R_N<1>

R9204 3.01K 1% 1/20W MF 201
R9205 300 1% 1/20W MF 201
R9206 100 1% 1/20W MF 201

VSS

S4E_X6
R9231 0 5% 1/20W MF 0201
SSD1_S4E1_JTAG_TDO → SSD1_S4E3_JTAG_TDO

PP1V8_SSD1
R9202 47K 1% 1/20W MF 201
R9208 100K 1% 1/20W MF 201
SSD1_S4E1_SWD_UID0
SSD1_S4E1_DROOP_L
SSD1_S4E1_SWD_UID1
R9209 100K 1% 1/20W MF 201

S4E VDD

PP0V9_SSD1
C9210 10UF 20% 6.3V CERM-X6S 0402 CRITICAL
C9211 2.2UF 20% 6.3V X5R-CERM 0201
C9212 2.2UF 20% 6.3V X5R-CERM 0201
C9213 0.1UF 10% 16V X5R-CERM 0201
C9214 0.1UF 10% 16V X5R-CERM 0201
C9215 0.1UF 10% 16V X5R-CERM 0201

S4E VDDIO

PP1V8_SSD1
C9232 10UF 20% 6.3V CERM-X6S 0402 CRITICAL
C9236 4.3UF
C9237 2.2UF 20% 6.3V X5R-CERM 0201
20% 4V CERM 0402-THICKSTNCL CRITICAL

VCC CAP

PP2V5_NAND_SSD1
C9248 10UF 20% 6.3V CERM-X6S 0402 CRITICAL
C9249 2.2UF 20% 6.3V X5R-CERM 0201
C9250 2.2UF 20% 6.3V X5R-CERM 0201

R9200 0 5% 1/20W MF 0201
PP1V8_SSD1 → PP1V8_SSD1_S4E1_PCI_AVDD_H
C9244 1.0UF 20% 6.3V X5R-CERM 0201-1
C9245 0.1UF 10% 16V X5R-CERM 0201

R9201 0 5% 1/20W MF 0201
PP1V8_SSD1_S4E1_AVDD18_PLL
C9246 1.0UF 20% 16V X5R-CERM 0201-1
C9247 0.1UF 10% 16V X5R-CERM 0201

BOM_COST_GROUP=SDD

SYNC_MASTER=j137_gs5_redhead SYNC_DATE=01/26/2017

PAGE TITLE: SSD1 S4E 1

Apple Inc.

DRAWING NUMBER: 051-02643 SIZE: D
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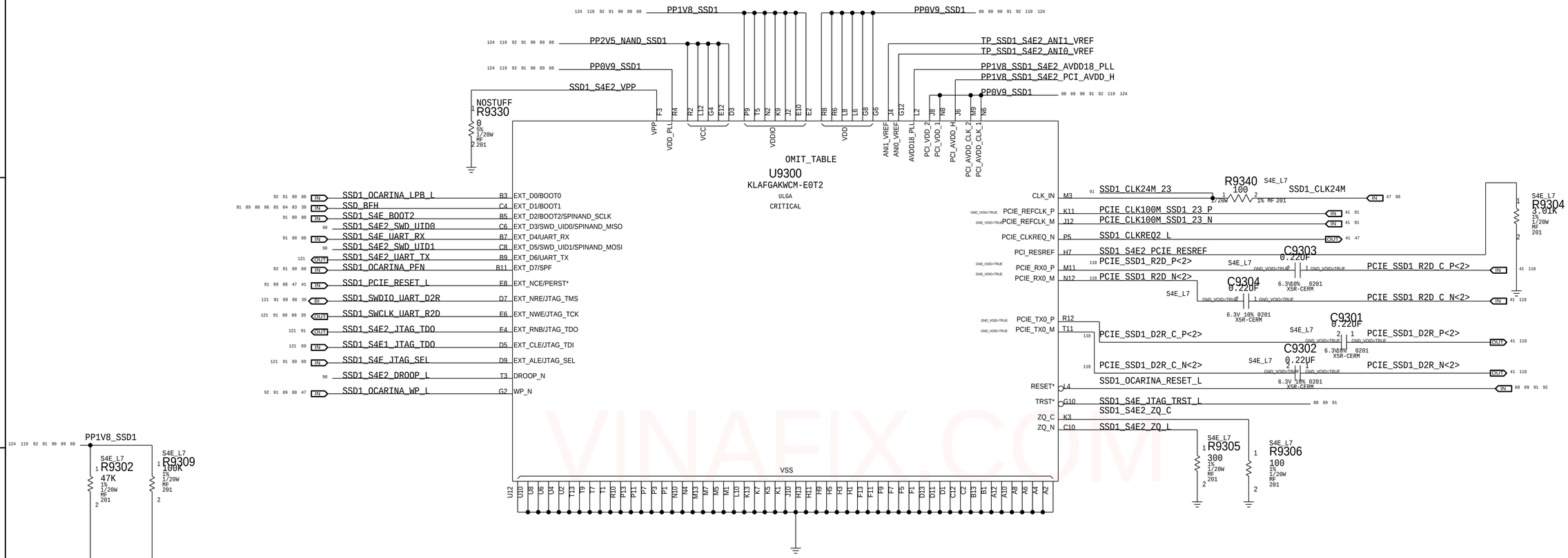
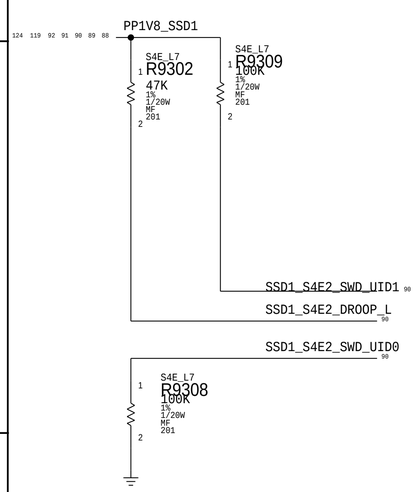
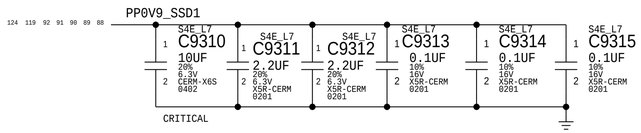
S4E2

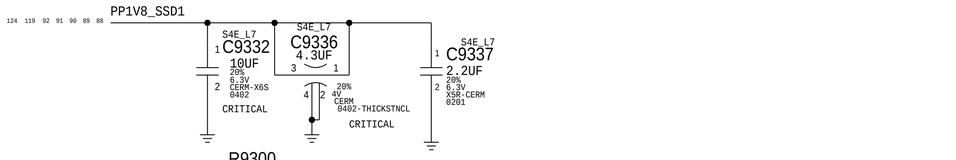




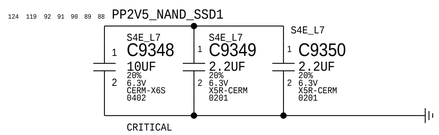
S4E VDD



S4E VDDIO



VCC CAP



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PAGE TITLE: SSD1 S4E 2

Apple Inc.

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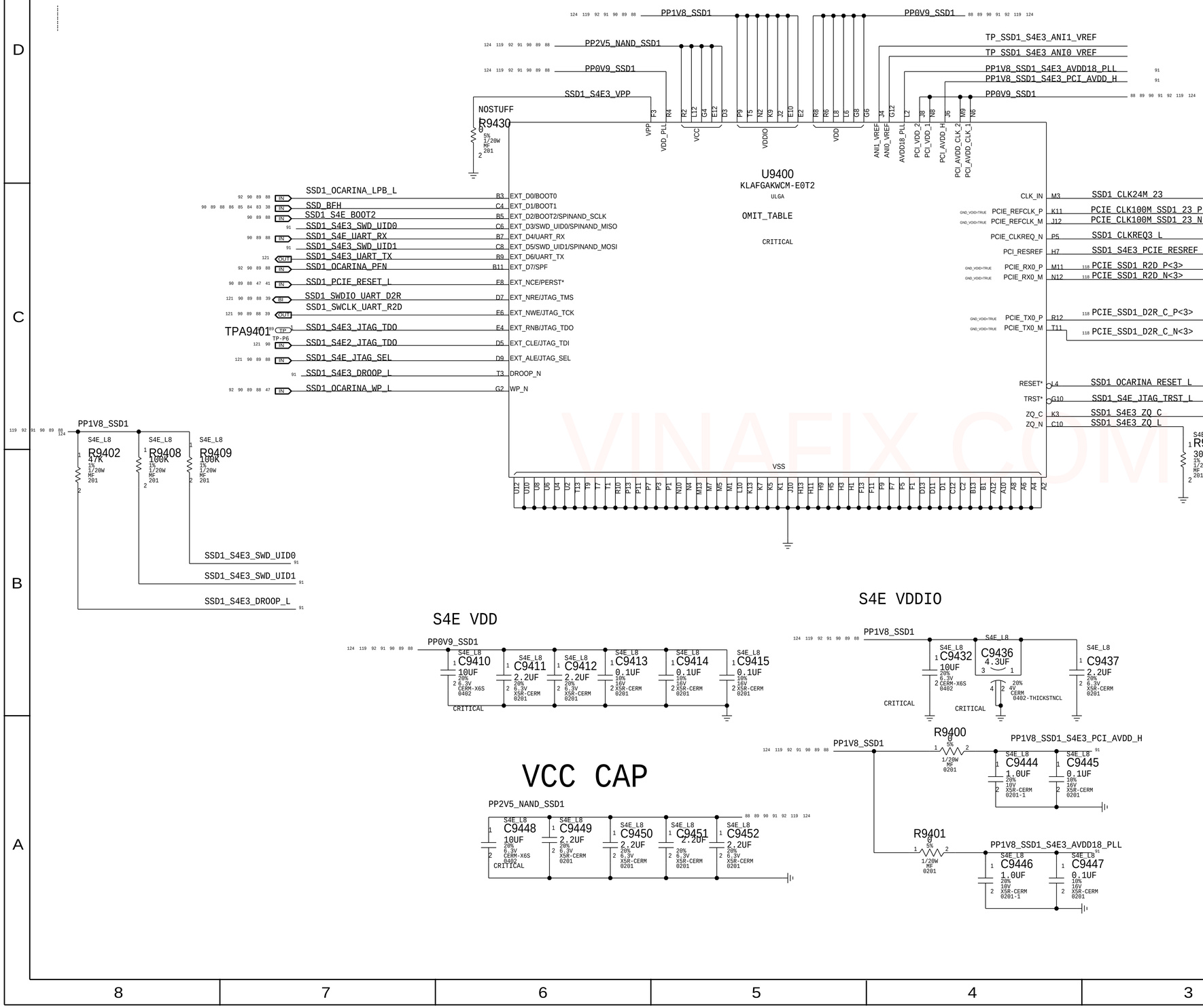
S4E3



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	Apple Inc.
DRAWING NUMBER	051-02643
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REVISION	4.0.0
BRANCH	evt-0
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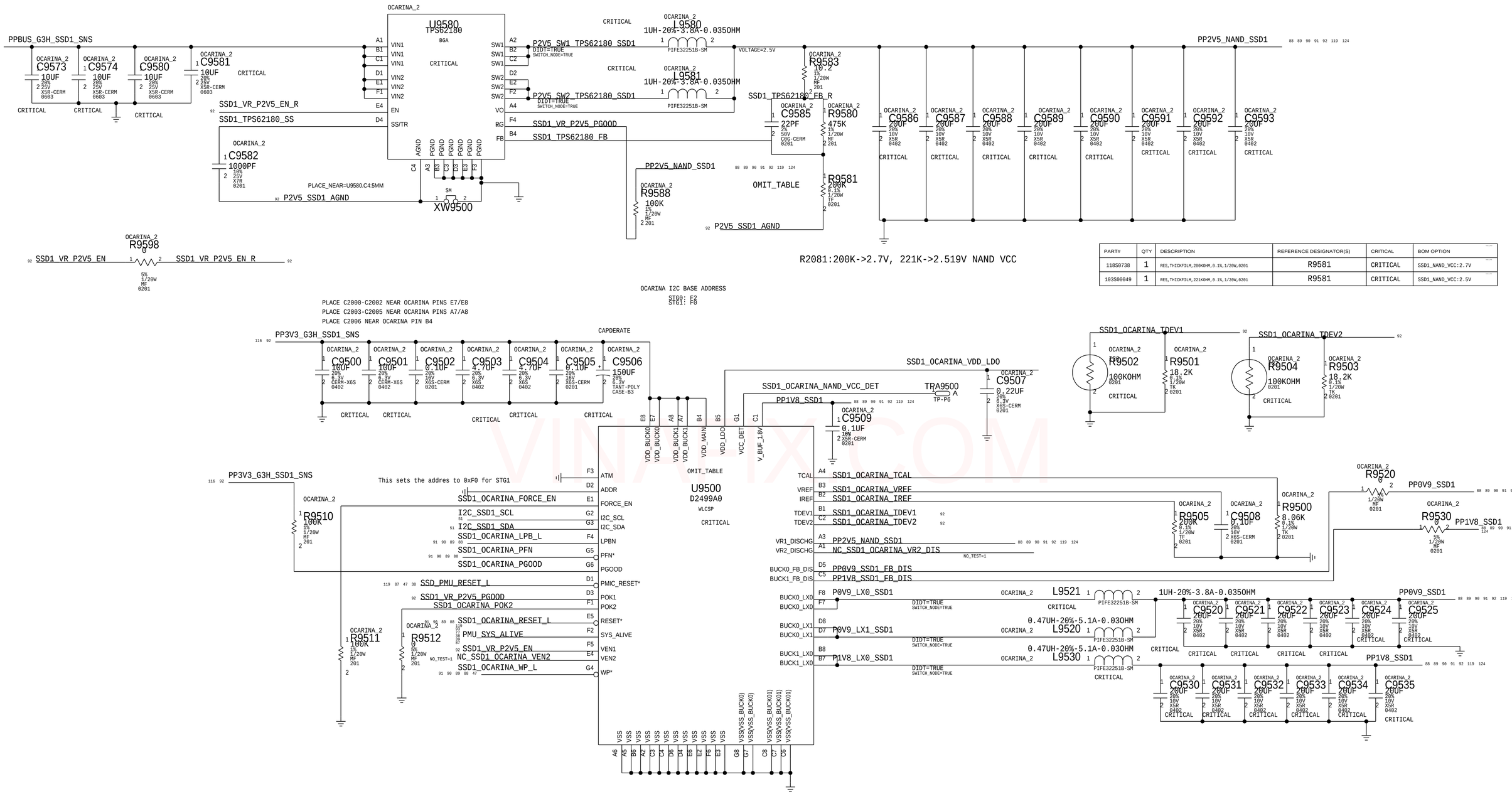

GMUX GPIO Expander

R9802 0 MF-LF 5% 1/16W 402 — PP3V3_S5 (124 93 80) → PP3V3_S5_GPIOX_R (VOLTAGE=3.3V)

R9803 0 402 MF-LF 5% 1/16W — PP1V8_S5 (93 80) → PP1V8_S5_GPIOX_R (VOLTAGE=1.8V)

C9801 0.1UF 10% 6.3V CERM-X5R 0201 (PP1V8_S5_GPIOX_R)

C9802 0.1UF 10% 6.3V CERM-X5R 0201 (PP3V3_S5_GPIOX_R)

R9801 NOSTUFF 10K 5% 1/20W MF 201 (PP3V3_S5_GPIOX_R)

U9801 PCAL6524 VFBGA

C4	INT*		
A5	ADDR		
A3	SCL	I2C_DISP_SCL	(51 IN)
A2	SDA	I2C_DISP_SDA	(51 BI)
B4	RESET*	DISP_GCON_RESET_L	(119 93)
A1	VDD(I2C-BUS)	PP1V8_S5	(93 80)
A4	VDD(P)	PP3V3_S5	(124 93 80)
A6	VSS	GND	
B1	P0_0	EG_VR0_PGOOD	IN (93 95)
D4	P0_1	P1V8GPU_PGOOD	IN (95)
C1	P0_2	PVDDCI_PGOOD	IN (95)
D2	P0_3	GPUVCORE_PGOOD	IN (95)
D1	P0_4	GPUFB_PGOOD	IN (19 93 95)
E1	P0_5	DP_INT_HPD_R	
D3	P0_6	USBC_HPD_DET	(93)
F1	P0_7	TP_BKLT_FAULT_L	
E2	P1_0	DP_INT_EG_HPD	BI (93 103)
F2	P1_1	DP_INT_IG_HPD	BI (15 93)
E3	P1_2	EDP_MUXSEL_OVR	(93)
F3	P1_3	EDP_IG_PANEL_PWR	IN (15)
F4	P1_4	EDP_IG_BKLT_EN	IN (15)
E4	P1_5	EG_LCD_PWR_EN	IN (103)
F5	P1_6	EG_BKLT_EN	IN (103)
E5	P1_7	TP_BKLT_BOOST_EN	
F6	P2_0	EG_VR0_EN	OUT (93 95)
E6	P2_1	EG_VR1_EN	OUT (93 95)
D5	P2_2	EG_VR2_EN	(93)
D6	P2_3	EG_VR3_EN	OUT (93 95)
C5	P2_4	EG_VR4_EN	OUT (93 95)
C6	P2_5	EG_RESET_L_BUFF	(93)
B5	P2_6	EDP_PANEL_PWR_EN	OUT (82 93)
B6	P2_7	EDP_BKLT_EN	OUT (81 93)
B2	NC		
B3	NC		
C2	NC		
C3	NC		

I2C Addr:
Read: 45h
Write: 44h

R9804 NOSTUFF 10K 5% 1/20W MF 201 (PP1V8_S5 (93 80) → GMUX_IOEXP_ADDR_SEL)

R9805 0 5% 1/20W MF 201 (GMUX_IOEXP_ADDR_SEL)

R9806 200 1% 1/10W MF-LF 402 (DP_INT_EG_HPD → DP_INT_HPD (82 93 120))

LAST RAIL PGOOD HAS TO BE VR4_PGOOD

R9820 47K 1/20W MF 201 5% — EG_VR0_EN (93 95)
R9821 47K 1/20W MF 201 5% — EG_VR1_EN (93 95)
R9822 47K 1/20W MF 201 5% — EG_VR2_EN (93)
R9823 47K 1/20W MF 201 5% — EG_VR3_EN (93 95)
R9824 47K 1/20W MF 201 5% — EG_VR4_EN (93 95)
R9825 100K 1/20W MF 201 5% — DP_INT_EG_HPD (93 103)
R9826 100K 1/20W MF 201 5% — DP_X_SNK0_HPD_EG (93 103)
R9827 100K 1/20W MF 201 5% — DP_X_SNK1_HPD_EG (93 103)
R9828 100K 1/20W MF 201 5% — DP_T_SNK0_HPD_EG (93 103)
R9830 100K 1/20W MF 201 5% — DP_T_SNK1_HPD_EG (93 103)
R9832 47K 1/20W MF 201 5% — EDP_PANEL_PWR_EN (82 93)
R9833 47K 1/20W MF 201 5% — EDP_BKLT_EN (81 93)

C9860 0.1UF 10% 6.3V CERM-X5R 0201 (PP3V3_S5 (124 93 80))

U9860 74LVC1G11GW-S500 SOT363

1	A	EG_RESET_L_BUFF (93)
3	B	EG_VR0_PGOOD (95 93)
6	C	PLT3V3_RST_L (20 IN)
5	VCC	
2	GND	
4	Y	GPU_RESET_L (OUT 117)

R9860 100K 5% 1/20W MF 201 (GPU_RESET_L)

C9840 0.1UF 10% 6.3V CERM-X5R 0201 (PP3V3_S5 (124 93 80))

U9840 SLG4AP41422 STQFN

1	VDD		
2	HPD_X_SNK0	DP_X_SNK0_HPD (27 IN)	
3	HPD_X_SNK1	DP_X_SNK1_HPD (27 IN)	
4	HPD_T_SNK0	DP_T_SNK0_HPD (105 IN)	
5	HPD_T_SNK1	DP_T_SNK1_HPD (105 IN)	
6	GPU_RESET_L	GPUFB_PGOOD (95 93 19 IN)	
7	GND		
12	HPD_X_SNK0_ISO	DP_X_SNK0_HPD_EG	OUT (93 103)
11	HPD_X_SNK1_ISO	DP_X_SNK1_HPD_EG	OUT (93 103)
10	HPD_T_SNK0_ISO	DP_T_SNK0_HPD_EG	OUT (93 103)
9	HPD_T_SNK1_ISO	DP_T_SNK1_HPD_EG	OUT (93 103)
8	HPD_DET_ANY	USBC_HPD_DET	(93)

DP 2:1 ANALOG MUX

PP3V3_S5 (124 93 80)

C9850 0.1UF 20% 10V X7R-CERM 0402
C9851 0.1UF 20% 10V X7R-CERM 0402

U9850 CBTL06142EEE TFBGA CRITICAL

A2	VDD	PP3V3_S5	
J4	VDD		
B4	DIN1_0+	DP_INT_EG_ML_P<0>	IN (118 103)
A4	DIN1_0-	DP_INT_EG_ML_N<0>	IN (118 103)
B5	DIN1_1+	DP_INT_EG_ML_P<1>	IN (118 103)
A5	DIN1_1-	DP_INT_EG_ML_N<1>	IN (118 103)
B6	DIN1_2+	DP_INT_EG_ML_P<2>	IN (118 103)
A6	DIN1_2-	DP_INT_EG_ML_N<2>	IN (118 103)
A8	DIN1_3+	DP_INT_EG_ML_P<3>	IN (118 103)
A9	DIN1_3-	DP_INT_EG_ML_N<3>	IN (118 103)
H9	DAUX1+	DP_INT_EG_AUX_P	BI (118 103)
J9	DAUX1-	DP_INT_EG_AUX_N	BI (118 103)
H8	DDC_CLK1	NC	
J8	DDC_DAT1	NC	
J2	HPD_1	DP_INT_EG_HPD_R	(103 93)
B8	DIN2_0+	DP_INT_IG_ML_P<0>	IN (118 5)
B9	DIN2_0-	DP_INT_IG_ML_N<0>	IN (118 5)
D8	DIN2_1+	DP_INT_IG_ML_P<1>	IN (118 5)
D9	DIN2_1-	DP_INT_IG_ML_N<1>	IN (118 5)
F8	DIN2_2+	DP_INT_IG_ML_P<2>	IN (118 5)
F9	DIN2_2-	DP_INT_IG_ML_N<2>	IN (118 5)
F8	DIN2_3+	DP_INT_IG_ML_P<3>	IN (118 5)
F9	DIN2_3-	DP_INT_IG_ML_N<3>	IN (118 5)
H6	DAUX2+	DP_INT_IG_AUX_P	BI (118 6)
J6	DAUX2-	DP_INT_IG_AUX_N	BI (118 6)
H5	DDC_CLK2	NC	
J5	DDC_DAT2	NC	
H3	HPD_2	DP_INT_IG_HPD_R	(93 15 OUT)
A1	GPU_SEL	EDP_MUXSEL_OVR	(120 82 IN)
B7	XSD*	LCD_MUX_EN	
B2	DOUT_0+	EDP_INT_ML_P<0>	OUT (82 120)
B1	DOUT_0-	EDP_INT_ML_N<0>	OUT (82 120)
D2	DOUT_1+	EDP_INT_ML_P<1>	OUT (82 120)
D1	DOUT_1-	EDP_INT_ML_N<1>	OUT (82 120)
E2	DOUT_2+	EDP_INT_ML_P<2>	OUT (82 120)
E1	DOUT_2-	EDP_INT_ML_N<2>	OUT (82 120)
F2	DOUT_3+	EDP_INT_ML_P<3>	OUT (82 120)
F1	DOUT_3-	EDP_INT_ML_N<3>	OUT (82 120)
H2	AUX+	EDP_INT_AUX_P	BI (82 120)
H1	AUX-	EDP_INT_AUX_N	BI (82 120)
J1	HPDIN	DP_INT_HPD	IN (82 93 120)
C2	DDC_AUX_SEL		
B3	GND		
C8	GND		
G8	GND		
H4	GND		
H7	GND		
G2	GND		

Pull down on eDP connector page

R9851 4.7K 1% 1/16W MF-LF 402 (DP_INT_IG_HPD (93 15 OUT) → DP_INT_IG_HPD_R)

R9819 2.26K 1% 1/16W MF-LF 402 (LCD_FSS (120 82 IN) → EDP_MUXSEL_OVR)

R9807 100K 5% 1/20W MF 201 (LCD_MUX_EN)

R9852 100K 5% 1/20W MF 201 (PP3V3_S5 (124 93 80))

MUXSEL is default low.
EG is the default option

PP1V8_S5 (93 80)

R9810 100K 5% 1/20W MF 201 (PP1V8_S5)

C9810 0.1UF 10% 6.3V CERM-X5R 0201 (PP1V8_S5)

U9810 74LVC1G08GW SOT353

1	B	P1V8S5_VALID
2	A	PMU_SYS_ALIVE (119 92 87 77 39 38 IN)
3		
4	Y	DISP_GCON_RESET_L_R
5		

R9811 0 5% NOSTUFF 1/10W MF-LF 402 (DISP_GCON_RESET_L_R)

R9812 0 5% 1/10W MF-LF 402 (DISP_GCON_RESET_L_R → DISP_GCON_RESET_L (93 119))

BOM_COST_GROUP=GRAPHICS

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	R9961		LOADRC:NO

High Speed Summing AMP

VOLTAGE=5V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

104 95 94 PP5V_S0_GPUFET → R9900 1 5% 1/16W MF-LF 402 → PP5V_S0_PCCAMP

C9900 10UF 20% 10V X6S-CERM 0603
C9901 0.1UF 10% 6.3V X6S 0201

R9904 604K 0.1% 1/20W TK 0201 — NO_XNET_CONNECTION=1 — GPUVR_ISUM_IOUT

101 98 IN GFXIMVP_ISNS1_N	NO_XNET_CONNECTION=1	R9940	2.43K	0.1% 1/20W TK 0201
101 98 IN GFXIMVP_ISNS2_N	NO_XNET_CONNECTION=1	R9941	2.43K	0.1% 1/20W TK 0201
101 98 IN GFXIMVP_ISNS3_N	NO_XNET_CONNECTION=1	R9942	2.43K	0.1% 1/20W TK 0201
101 IN GFXIMVP_ISNS1_P	NO_XNET_CONNECTION=1	R9943	2.43K	0.1% 1/20W TK 0201
101 IN GFXIMVP_ISNS2_P	NO_XNET_CONNECTION=1	R9944	2.43K	0.1% 1/20W TK 0201
98 IN GFXIMVP_ISNS3_P	NO_XNET_CONNECTION=1	R9945	2.43K	0.1% 1/20W TK 0201

GFXIMVP_ISNS_R_N → R9946 3.09K 0.1% 1/20W TK 0201 → GFXIMVP_ISNS_N
GFXIMVP_ISNS_R_P → R9947 3.09K 0.1% 1/20W TK 0201 → GFXIMVP_ISNS_P

NOSTUFF C9902 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U9900.3:2.54MM
PLACE_NEAR=U9900.1:2.54MM
NO_XNET_CONNECTION=1

R9903 604K 0.1% 1/20W TK 0201

U9900 LMV693 UQFN

R9905 0 1/20W 5% 0201 MF — GPUVR_ISUM_IOUT_R → GPU_VCORE_IOUT_REF_R

NOSTUFF C9903 0.1UF 10% 6.3V X6S 0201

TP9900

PCC:YES R9906 1M 1/20W 1% 201 MF

PLACE_NEAR=U9901.5:2.54MM
94 95 104 PP5V_S0_GPUFET
PCC:YES C9904 0.1UF 10% 6.3V X6S 0201

PCC:YES U9901 LMV331 SC70-5

GPUVDDC_PCC_ALERT_R_L → PCC:YES R9907 0 1/20W 5% 0201 MF → GPUVDDC_PCC_ALERT_L (94 103 OUT)

PP3V3_S0_GPU (94 115) → ALWAYS STUFF ME R9908 10K 5% 1/20W MF 201

NOSTUFF C9905 0.22UF 20% 6.3V X6S-CERM 0201

TP9902

TP9901

R9911 10K 0.1% 1/20W MF 0201-1 — GPU_VCORE_IOUT_REF

PLACE_NEAR=U7800.A14:5MM
R9960 10K 0.1% 1/20W MF 0201-1 — PMU_GPU_CORE_ISENSE (59 OUT)
PLACE_NEAR=U7800.A14:5MM
R9961 5.49K 0.1% 1/20W TK 0201 2 LOADRC:YES
C9960 2.2UF 20% 6.3V X5R-CERM 0201
PLACE_NEAR=U7800.A14:5MM
GND_CALPE_AVSS (53 54 55 58 76 121)

IG0C to Calpe

PCC flag to GPU

Comparator

Active LOW

Trip Point Voltage Gen

PCC:YES U9902 SC4437 SOT23-3

104 95 94 PP5V_S0_GPUFET → PCC:YES R9909 2.2 5% 1/20W MF 201 → PP5V_VREF_PCC
VOLTAGE=5V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200
PCC:YES C9906 1UF 20% 6.3V X6S-CERM 0201

IN ← PP5V_S0_GPUFET
OUT → PP3V3_VREF_PCC
VOLTAGE=3.3V MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200
PCC:YES C9907 1UF 20% 6.3V X6S-CERM 0201

PCC:YES R9910 1K 1/20W 0.1% 0201 TK — PP3V3_VREF_PCC → GPU_VCORE_IOUT_REF
PCC:YES R9912 11.8K 0.1% 1/20W TK 0201

Pulse Stretcher

115 94 PP3V3_S0_GPU

PCC:YES R9913 0 5% 1/20W MF 0201
PCC:YES R9914 0 5% 1/20W MF 0201
PCC:YES C9908 0.1UF 10% 6.3V X6S 0201

PCC:YES C9909 0.1UF 10% 6.3V X6S 0201

PCC:YES U9903 SN74LVC1G123 BGA

103 94 GPUVDDC_PCC_ALERT_L → A1
PCC_B → B1
PCC_CLR_L → C1
A2 → VCC
Q → D2 → PCC_EVENT_3V3
REXT_CEXT ↔ B2 ↔ PCC_CEXT
CEXT ↔ C2
GND → D1

PCC:YES R9915 200K 1% 1/20W MF 201

PCC:YES C9910 1UF 20% 6.3V X6S-CERM 0201

PP1V8_S5 (80)
PCC:YES C9911 0.1UF 10% 6.3V X6S 0201

PCC:YES U9904 74LVC1G17DRL SOT-553

PCC_EVENT_3V3 → PCC_EVENT_R

PCC:YES R9916 33 1/20W 5% 201 MF

TP9903

PCC:NO R9917 100K 5% 1/20W MF 201

PCC_EVENT → to H9M (39 OUT)

PCC flag to H9M

Active HIGH

BOM_COST_GROUP=GRAPHICS

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BOMOPTION=OMIT_TABLE

UA000
100-CK4803-ES
BGA
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PEG_GPU_R2D_C_P<0>	AT41	PCIE_RX0+	PCIE_TX0+ AV35 PEG_GPU_D2R_C_P<0>
PEG_GPU_R2D_C_N<0>	AT40	PCIE_RX0-	PCIE_TX0- AU35 PEG_GPU_D2R_C_N<0>
PEG_GPU_R2D_C_P<1>	AR41	PCIE_RX1+	PCIE_TX1+ AU38 PEG_GPU_D2R_C_P<1>
PEG_GPU_R2D_C_N<1>	AR40	PCIE_RX1-	PCIE_TX1- AU39 PEG_GPU_D2R_C_N<1>
PEG_GPU_R2D_C_P<2>	AP41	PCIE_RX2+	PCIE_TX2+ AR37 PEG_GPU_D2R_C_P<2>
PEG_GPU_R2D_C_N<2>	AP40	PCIE_RX2-	PCIE_TX2- AR38 PEG_GPU_D2R_C_N<2>
PEG_GPU_R2D_C_P<3>	AM41	PCIE_RX3+	PCIE_TX3+ AN37 PEG_GPU_D2R_C_P<3>
PEG_GPU_R2D_C_N<3>	AM40	PCIE_RX3-	PCIE_TX3- AN38 PEG_GPU_D2R_C_N<3>
PEG_GPU_R2D_C_P<4>	AL41	PCIE_RX4+	PCIE_TX4+ AL37 PEG_GPU_D2R_C_P<4>
PEG_GPU_R2D_C_N<4>	AL40	PCIE_RX4-	PCIE_TX4- AL38 PEG_GPU_D2R_C_N<4>
PEG_GPU_R2D_C_P<5>	AK41	PCIE_RX5+	PCIE_TX5+ AJ37 PEG_GPU_D2R_C_P<5>
PEG_GPU_R2D_C_N<5>	AK40	PCIE_RX5-	PCIE_TX5- AJ38 PEG_GPU_D2R_C_N<5>
PEG_GPU_R2D_C_P<6>	AJ41	PCIE_RX6+	PCIE_TX6+ AG37 PEG_GPU_D2R_C_P<6>
PEG_GPU_R2D_C_N<6>	AJ40	PCIE_RX6-	PCIE_TX6- AG38 PEG_GPU_D2R_C_N<6>
PEG_GPU_R2D_C_P<7>	AH41	PCIE_RX7+	PCIE_TX7+ AE37 PEG_GPU_D2R_C_P<7>
PEG_GPU_R2D_C_N<7>	AH40	PCIE_RX7-	PCIE_TX7- AE38 PEG_GPU_D2R_C_N<7>
EG_PEG_CLK100M_P	AV33	PCIE_REFCLK+	
EG_PEG_CLK100M_N	AU33	PCIE_REFCLK-	
GPU_TEST_PG	AY13	TEST_PG	
GPU_RESET_R_L	AV40	PERST*	

PEG_GPU_R2D_C_P<0> → CA020 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_N<0> → CA021 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_P<1> → CA022 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_N<1> → CA023 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_P<2> → CA024 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_N<2> → CA025 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_P<3> → CA026 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_N<3> → CA027 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_P<4> → CA028 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_N<4> → CA029 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_P<5> → CA039 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_N<5> → CA047 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_P<6> → CA048 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_N<6> → CA059 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_P<7> → CA060 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201
PEG_GPU_R2D_C_N<7> → CA061 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201

PP1V8_S0_GPU → RA000 1K 1% 1/20W MF 201 (PLACE_NEAR=UA000.AY13:5MM) → GPU_TEST_PG

GPU_RESET_L → RA002 0 1/20W MF 5% 0201 → GPU_RESET_R_L

CA077 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_P<0> OUT
CA062 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_N<0> OUT
CA063 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_P<1> OUT
CA064 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_N<1> OUT
CA065 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_P<2> OUT
CA066 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_N<2> OUT
CA067 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_P<3> OUT
CA075 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_N<3> OUT
CA068 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_P<4> OUT
CA069 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_N<4> OUT
CA070 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_P<5> OUT
CA071 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_N<5> OUT
CA076 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_P<6> OUT
CA072 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_N<6> OUT
CA073 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_P<7> OUT
CA074 0.22UF GND_VOID=TRUE 20% 6.3V X6S-CERM 0201 → PEG_GPU_D2R_N<7> OUT

EG_VR0_EN → RA010 0 1/20W 5% 0201 MF → P3V3GPU_EN (MAKE_BASE=TRUE)
EG_VR1_EN → RA011 0 1/20W 5% 0201 MF → P1V8GPU_EN
EG_VR3_EN → RA012 0 1/20W 5% 0201 MF MAKE_BASE=TRUE → GPUVCORE_EN
EG_VR4_EN → RA014 0 1/20W 5% 0201 MF MAKE_BASE=TRUE → P1V35FB_EN

SPARE
DBGLED
QA000 DMN5L06VK-7 SOT563 VER 3 (NC, D, G, S, NC)

PP3V3_S0_GPU
PP5V_S0_GPUFET

RA021 180K 1/20W 1% 201
RA015 100K 1/20W 1% 201
RA016 100K 1/20W 1% 201
RA017 100K 1/20W 1% 201
RA018 100K 1/20W 1% 201
RA019 100K 1/20W 1% 201
RA099 100K 1/20W 1% 201
NOSTUFF

DBGLED
RA022 20K 5% 1/20W MF 201
DBGLED_GPU
DBGLED
DA000 GRN-90MCD-5MA-2.85V 0402 BLACK SIDE=BOTTOM
SILK_PART=S0_ON

CA090 0.1UF 10% 6.3V CERM-X5R 0201

P5_S0GPU_PGOOD (MAKE_BASE=TRUE)
P3V3_S0GPU_PGOOD (MAKE_BASE=TRUE)
P1V8GPU_PGOOD (MAKE_BASE=TRUE) → P1V8GPU_PGOOD
PVDDCI_PGOOD (MAKE_BASE=TRUE) → PVDDCI_PGOOD
GPUVCORE_PGOOD (MAKE_BASE=TRUE) → GPUVCORE_PGOOD
GPUFB_PGOOD (MAKE_BASE=TRUE) → GPUFB_PGOOD

UA090 74LVC1G08GW SOT353
A, B → EG_VR0_PGOOD

RA023 330K 1/20W 1% 201
DBGLED
QA000 DMN5L06VK-7 SOT563 VER 3
DBGLED_GPU_D

RA020 0 1/20W 5% 0201 MF
GPUFB_PGOOD → PM_ALL_GPU_PGOOD (MAKE_BASE=TRUE) → PM_ALL_GPU_PGOOD

PP3V3_S0SW_TBT_T_SNS
PP3V3_S0SW_TBT_X_SNS

RA031 100K 1/20W 1% 201
RA033 100K 1/20W 1% 201

Tieing off Ridge GPIOs
Both SNK0 and SNK1 shown
as always available

TBT_X_HDMI_DDC_DATA
TBT_X_HDMI_DDC_CLK
TBT_T_HDMI_DDC_DATA
TBT_T_HDMI_DDC_CLK

PCH pins mirror
TBT_X hookup

RA030 100K 1/20W 1% 201
RA032 100K 1/20W 1% 201

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: GPU Baffin PCIe

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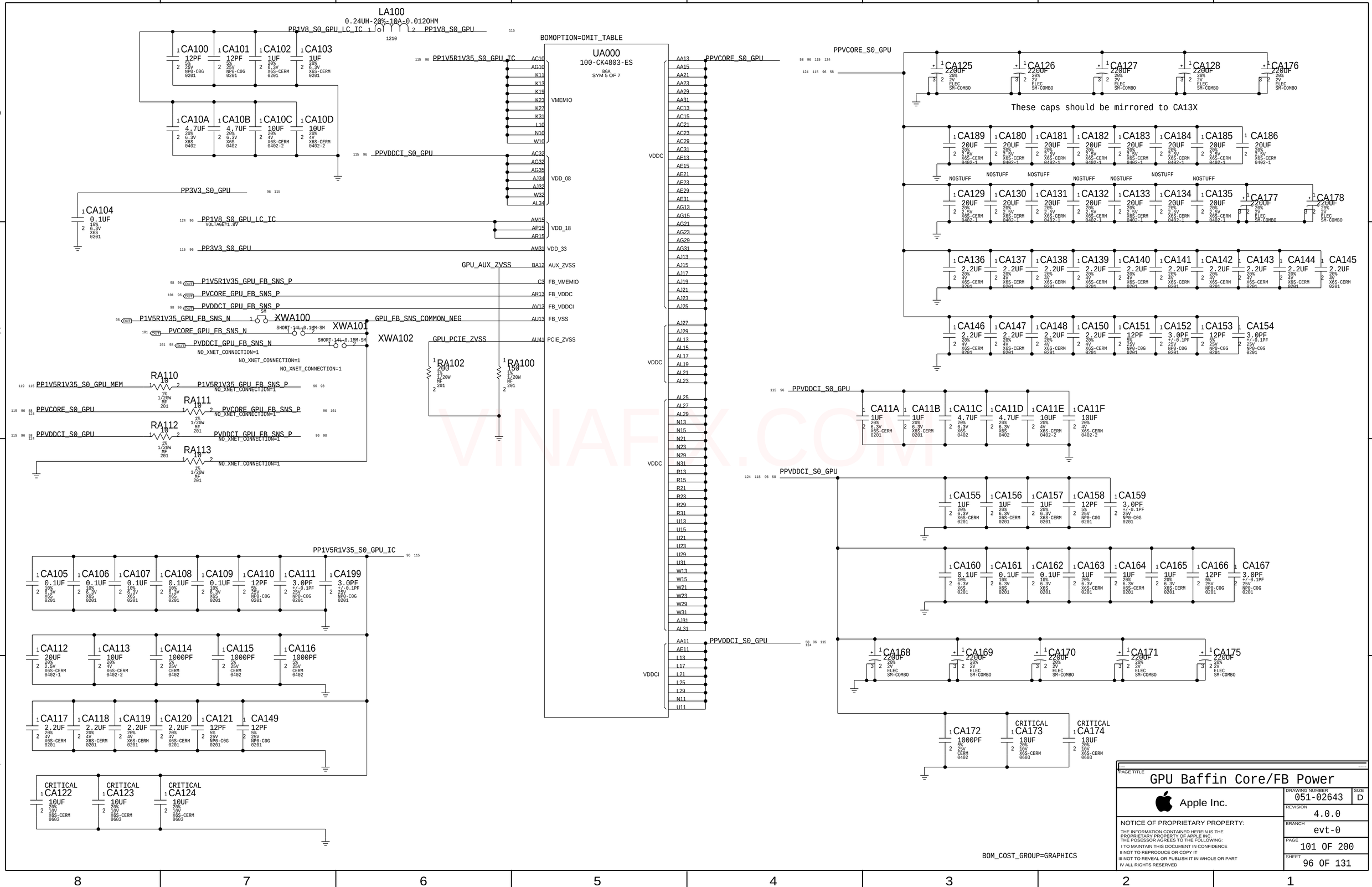

PAGE TITLE: GPU Baffin Core/FB Power

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BOMOPTION=OMIT_TABLE

UA000
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BGA
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FB_A0_DQ<0> L34 DQA0_0
FB_A0_DQ<1> L37 DQA0_1
FB_A0_DQ<2> L38 DQA0_2
FB_A0_DQ<3> J35 DQA0_3
FB_A0_DQ<4> G37 DQA0_4
FB_A0_DQ<5> E38 DQA0_5
FB_A0_DQ<6> E35 DQA0_6
FB_A0_DQ<7> D35 DQA0_7
FB_A0_DQ<8> H41 DQA0_8
FB_A0_DQ<9> H40 DQA0_9
FB_A0_DQ<10> G41 DQA0_10
FB_A0_DQ<11> G40 DQA0_11
FB_A0_DQ<12> E40 DQA0_12
FB_A0_DQ<13> D41 DQA0_13
FB_A0_DQ<14> D40 DQA0_14
FB_A0_DQ<15> C41 DQA0_15
FB_A0_DQ<16> C40 DQA0_16
FB_A0_DQ<17> B39 DQA0_17
FB_A0_DQ<18> A39 DQA0_18
FB_A0_DQ<19> B38 DQA0_19
FB_A0_DQ<20> B36 DQA0_20
FB_A0_DQ<21> A36 DQA0_21
FB_A0_DQ<22> B35 DQA0_22
FB_A0_DQ<23> A35 DQA0_23
FB_A0_DQ<24> B33 DQA0_24
FB_A0_DQ<25> B32 DQA0_25
FB_A0_DQ<26> A32 DQA0_26
FB_A0_DQ<27> B31 DQA0_27
FB_A0_DQ<28> A30 DQA0_28
FB_A0_DQ<29> B29 DQA0_29
FB_A0_DQ<30> B28 DQA0_30
FB_A0_DQ<31> A28 DQA0_31

FB_A1_DQ<0> B27 DQA1_0
FB_A1_DQ<1> A27 DQA1_1
FB_A1_DQ<2> B26 DQA1_2
FB_A1_DQ<3> A26 DQA1_3
FB_A1_DQ<4> A24 DQA1_4
FB_A1_DQ<5> B23 DQA1_5
FB_A1_DQ<6> A23 DQA1_6
FB_A1_DQ<7> B22 DQA1_7
FB_A1_DQ<8> B20 DQA1_8
FB_A1_DQ<9> A20 DQA1_9
FB_A1_DQ<10> B19 DQA1_10
FB_A1_DQ<11> A19 DQA1_11
FB_A1_DQ<12> B17 DQA1_12
FB_A1_DQ<13> A16 DQA1_13
FB_A1_DQ<14> B16 DQA1_14
FB_A1_DQ<15> A15 DQA1_15
FB_A1_DQ<16> B15 DQA1_16
FB_A1_DQ<17> A14 DQA1_17
FB_A1_DQ<18> B14 DQA1_18
FB_A1_DQ<19> B13 DQA1_19
FB_A1_DQ<20> A11 DQA1_20
FB_A1_DQ<21> B11 DQA1_21
FB_A1_DQ<22> A10 DQA1_22
FB_A1_DQ<23> B10 DQA1_23
FB_A1_DQ<24> B8 DQA1_24
FB_A1_DQ<25> A7 DQA1_25
FB_A1_DQ<26> B7 DQA1_26
FB_A1_DQ<27> A6 DQA1_27
FB_A1_DQ<28> A4 DQA1_28
FB_A1_DQ<29> B4 DQA1_29
FB_A1_DQ<30> A3 DQA1_30
FB_A1_DQ<31> B3 DQA1_31

FB_A_MVREFD K17 MVREFDA

FB_A_CALR K15 MEM_CALRA

RA202
120
1% 1/20W MF 201
NOSTUFF
PLACE_NEAR=UA000.K15:2.54MM

MAA0_0 G25 FB_A0_A<0>
MAA0_1 H25 FB_A0_A<1>
MAA0_2 E27 FB_A0_A<2>
MAA0_3 D27 FB_A0_A<3>
MAA0_4 D29 FB_A0_A<4>
MAA0_5 H27 FB_A0_A<5>
MAA0_6 H23 FB_A0_A<6>
MAA0_7 E23 FB_A0_A<7>

MAA1_0 E15 FB_A1_A<0>
MAA1_1 H15 FB_A1_A<1>
MAA1_2 G13 FB_A1_A<2>
MAA1_3 D13 FB_A1_A<3>
MAA1_4 H11 FB_A1_A<4>
MAA1_5 H13 FB_A1_A<5>
MAA1_6 H17 FB_A1_A<6>
MAA1_7 G17 FB_A1_A<7>

WCKA0_0 D33 FB_A0_WCLK_P<0>
WCKA0_0* E33 FB_A0_WCLK_N<0>

WCKA0_1 A34 FB_A0_WCLK_P<1>
WCKA0_1* B34 FB_A0_WCLK_N<1>

WCKA1_0 A22 FB_A1_WCLK_P<0>
WCKA1_0* B21 FB_A1_WCLK_N<0>

WCKA1_1 A8 FB_A1_WCLK_P<1>
WCKA1_1* B9 FB_A1_WCLK_N<1>

EDCA0_0 G38 FB_A0_EDC<0>
EDCA0_1 F41 FB_A0_EDC<1>
EDCA0_2 B37 FB_A0_EDC<2>
EDCA0_3 A31 FB_A0_EDC<3>

EDCA1_0 B24 FB_A1_EDC<0>
EDCA1_1 A18 FB_A1_EDC<1>
EDCA1_2 B12 FB_A1_EDC<2>
EDCA1_3 B6 FB_A1_EDC<3>

DDBIA0_0 J38 FB_A0_DBI_L<0>
DDBIA0_1 F40 FB_A0_DBI_L<1>
DDBIA0_2 A38 FB_A0_DBI_L<2>
DDBIA0_3 B30 FB_A0_DBI_L<3>

DDBIA1_0 B25 FB_A1_DBI_L<0>
DDBIA1_1 B18 FB_A1_DBI_L<1>
DDBIA1_2 A12 FB_A1_DBI_L<2>
DDBIA1_3 B5 FB_A1_DBI_L<3>

ADBIA0 H21 FB_A0_ABI_L
ADBIA1 H19 FB_A1_ABI_L

CLKA0 E31 FB_A0_CLK_P
CLKA0* D31 FB_A0_CLK_N

CLKA1 D7 FB_A1_CLK_P
CLKA1* D9 FB_A1_CLK_N

RASA0* D21 FB_A0_RAS_L
RASA1* D19 FB_A1_RAS_L

CASA0* D23 FB_A0_CAS_L
CASA1* D17 FB_A1_CAS_L

CSA0_0* H31 FB_A0_CS_L

CSA1_0* E7 FB_A1_CS_L

CKEA0 G21 FB_A0_CKE_L
CKEA1 E19 FB_A1_CKE_L

WEA0* G29 FB_A0_WE_L
WEA1* D11 FB_A1_WE_L

MAA0_8 D25 FB_A0_A<8>
MAA0_9 H29 NC

MAA1_8 D15 FB_A1_A<8>
MAA1_9 F11 NC

DRAM_RSTA L32 FB_A_RESET_PIN_A

RA291
10
1% 1/20W MF 201

RA293
49.9
1% 1/20W MF 201

FB_A_RESET_L

RA290
5.1K
1% 1/20W MF 201

CA290
120PF
10% 25V X7R 0201

PP1V5R1V35_S0_GPU_IC

RA204
40.2
1% 1/20W MF 201
NOSTUFF
note: to be unstuffed after initial baffin bringup
PLACE_NEAR=UA000.K17:2.54MM

FB_A_MVREFD
PLACE_NEAR=UA000.K17:2.54MM

RA206
100
1% 1/20W MF 201
NOSTUFF

CA200
1UF
20% 6.3V X6S-CERM
NOSTUFF

BOMOPTION=OMIT_TABLE

UA000
100-CK4803-ES
BGA
SYM 4 OF 7

FB_B0_DQ<0> C2 DQB0_0
FB_B0_DQ<1> C1 DQB0_1
FB_B0_DQ<2> D2 DQB0_2
FB_B0_DQ<3> D1 DQB0_3
FB_B0_DQ<4> F1 DQB0_4
FB_B0_DQ<5> G2 DQB0_5
FB_B0_DQ<6> G1 DQB0_6
FB_B0_DQ<7> H2 DQB0_7
FB_B0_DQ<8> K2 DQB0_8
FB_B0_DQ<9> K1 DQB0_9
FB_B0_DQ<10> L2 DQB0_10
FB_B0_DQ<11> L1 DQB0_11
FB_B0_DQ<12> N2 DQB0_12
FB_B0_DQ<13> P2 DQB0_13
FB_B0_DQ<14> P1 DQB0_14
FB_B0_DQ<15> R2 DQB0_15
FB_B0_DQ<16> R1 DQB0_16
FB_B0_DQ<17> T2 DQB0_17
FB_B0_DQ<18> T1 DQB0_18
FB_B0_DQ<19> U2 DQB0_19
FB_B0_DQ<20> W1 DQB0_20
FB_B0_DQ<21> W2 DQB0_21
FB_B0_DQ<22> Y1 DQB0_22
FB_B0_DQ<23> Y2 DQB0_23
FB_B0_DQ<24> AB2 DQB0_24
FB_B0_DQ<25> AC1 DQB0_25
FB_B0_DQ<26> AC2 DQB0_26
FB_B0_DQ<27> AD1 DQB0_27
FB_B0_DQ<28> AF1 DQB0_28
FB_B0_DQ<29> AF2 DQB0_29
FB_B0_DQ<30> AG1 DQB0_30
FB_B0_DQ<31> AG2 DQB0_31

FB_B1_DQ<0> AH1 DQB1_0
FB_B1_DQ<1> AH2 DQB1_1
FB_B1_DQ<2> AJ2 DQB1_2
FB_B1_DQ<3> AK1 DQB1_3
FB_B1_DQ<4> AL2 DQB1_4
FB_B1_DQ<5> AM1 DQB1_5
FB_B1_DQ<6> AM2 DQB1_6
FB_B1_DQ<7> AN2 DQB1_7
FB_B1_DQ<8> AR1 DQB1_8
FB_B1_DQ<9> AR2 DQB1_9
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FB_B1_DQ<11> AT2 DQB1_11
FB_B1_DQ<12> AV2 DQB1_12
FB_B1_DQ<13> AW1 DQB1_13
FB_B1_DQ<14> AW2 DQB1_14
FB_B1_DQ<15> AY3 DQB1_15
FB_B1_DQ<16> BA3 DQB1_16
FB_B1_DQ<17> AY4 DQB1_17
FB_B1_DQ<18> BA4 DQB1_18
FB_B1_DQ<19> AY5 DQB1_19
FB_B1_DQ<20> BA7 DQB1_20
FB_B1_DQ<21> AY7 DQB1_21
FB_B1_DQ<22> AY8 DQB1_22
FB_B1_DQ<23> BA8 DQB1_23
FB_B1_DQ<24> AR4 DQB1_24
FB_B1_DQ<25> AR5 DQB1_25
FB_B1_DQ<26> AU4 DQB1_26
FB_B1_DQ<27> AU7 DQB1_27
FB_B1_DQ<28> AN8 DQB1_28
FB_B1_DQ<29> AV11 DQB1_29
FB_B1_DQ<30> AU11 DQB1_30
FB_B1_DQ<31> AP11 DQB1_31

FB_B_MVREFD U10 MVREFDB

PP3V3_S0_GPU

RA200
10K
NOSTUFF
5% 1/20W MF 201

GPU_TEST_EN AF40 TESTEN

RA201
10K
5% 1/20W MF 201

FB_B_CALR R10 MEM_CALRB

RA203
120
1% 1/20W MF 201
NOSTUFF
PLACE_NEAR=UA000.R10:2.54MM

MAB0_0 R5 FB_B0_A<0>
MAB0_1 R8 FB_B0_A<1>
MAB0_2 N7 FB_B0_A<2>
MAB0_3 N4 FB_B0_A<3>
MAB0_4 L8 FB_B0_A<4>
MAB0_5 N8 FB_B0_A<5>
MAB0_6 U8 FB_B0_A<6>
MAB0_7 U7 FB_B0_A<7>

MAB1_0 AE7 FB_B1_A<0>
MAB1_1 AF8 FB_B1_A<1>
MAB1_2 AG5 FB_B1_A<2>
MAB1_3 AG4 FB_B1_A<3>
MAB1_4 AJ4 FB_B1_A<4>
MAB1_5 AG8 FB_B1_A<5>
MAB1_6 AC8 FB_B1_A<6>
MAB1_7 AC5 FB_B1_A<7>

WCKB0_0 H1 FB_B0_WCLK_P<0>
WCKB0_0* J2 FB_B0_WCLK_N<0>

WCKB0_1 AB1 FB_B0_WCLK_P<1>
WCKB0_1* AA2 FB_B0_WCLK_N<1>

WCKB1_0 AP1 FB_B1_WCLK_P<0>
WCKB1_0* AP2 FB_B1_WCLK_N<0>

WCKB1_1 AN4 FB_B1_WCLK_P<1>
WCKB1_1* AN5 FB_B1_WCLK_N<1>

EDCB0_0 F2 FB_B0_EDC<0>
EDCB0_1 M2 FB_B0_EDC<1>
EDCB0_2 V1 FB_B0_EDC<2>
EDCB0_3 AD2 FB_B0_EDC<3>

EDCB1_0 AL1 FB_B1_EDC<0>
EDCB1_1 AU2 FB_B1_EDC<1>
EDCB1_2 BA6 FB_B1_EDC<2>
EDCB1_3 AV7 FB_B1_EDC<3>

DDBIB0_0 E2 FB_B0_DBI_L<0>
DDBIB0_1 M1 FB_B0_DBI_L<1>
DDBIB0_2 V2 FB_B0_DBI_L<2>
DDBIB0_3 AE2 FB_B0_DBI_L<3>

DDBIB1_0 AK2 FB_B1_DBI_L<0>
DDBIB1_1 AV1 FB_B1_DBI_L<1>
DDBIB1_2 AY6 FB_B1_DBI_L<2>
DDBIB1_3 AV9 FB_B1_DBI_L<3>

ADBIB0 W8 FB_B0_ABI_L
ADBIB1 AA8 FB_B1_ABI_L

CLKB0 G4 FB_B0_CLK_P
CLKB0* J4 FB_B0_CLK_N

CLKB1 AL5 FB_B1_CLK_P
CLKB1* AL4 FB_B1_CLK_N

RASB0* W4 FB_B0_RAS_L
RASB1* AA4 FB_B1_RAS_L

CASB0* U4 FB_B0_CAS_L
CASB1* AC4 FB_B1_CAS_L

CSB0_0* G5 FB_B0_CS_L

CSB1_0* AL8 FB_B1_CS_L

CKEB0 W5 FB_B0_CKE_L
CKEB1 AA7 FB_B1_CKE_L

WEB0* L4 FB_B0_WE_L
WEB1* AJ7 FB_B1_WE_L

MAB0_8 R4 FB_B0_A<8>
MAB0_9 L5 NC

MAB1_8 AF4 FB_B1_A<8>
MAB1_9 AJ8 NC

DRAM_RSTB AM11 FB_B_RESET_PIN_A

RA296
10
1% 1/20W MF 201

RA297
49.9
1% 1/20W MF 201

FB_B_RESET_L

RA295
5.1K
1% 1/20W MF 201

CA295
120PF
10% 25V X7R 0201

PP1V5R1V35_S0_GPU_IC

RA205
40.2
1% 1/20W MF 201
NOSTUFF
note: to be unstuffed after initial baffin bringup
PLACE_NEAR=UA000.U10:2.54MM

FB_B_MVREFD
PLACE_NEAR=UA000.U10:2.54MM

RA207
100
1% 1/20W MF 201
NOSTUFF

CA201
1UF
20% 6.3V X6S-CERM
NOSTUFF

BOM_COST_GROUP=GRAPHICS

PAGE TITLE
GPU Baffin FB

Apple Inc.

DRAWING NUMBER 051-02643
SIZE D
REVISION 4.0.0
BRANCH evt-0
PAGE 102 OF 200
SHEET 97 OF 131

GPU FB SUPPLY
VOUT = 1.5V / 1.35V
10.7A MAX OUTPUT
F = 500 KHZ

VID1	VID0	FBVDD
0	0	1.5V
1	0	1.35V

GPU VDDCI SUPPLY
VOUT = 0.8V-0.9V
?9.7A? MAX OUTPUT
F = 450 KHZ

Note:
Regulator requires a minimum load to prevent noise in the audio frequencies

BOM_COST_GROUP=GRAPHICS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00174	1	MOSFET,CTRL+SYNC,25V,4.1/1.4MΩ,QFN32,6x6	QA340	CRITICAL	

PAGE TITLE
VR 1.05V GPU & 1.35V FB

Apple Inc.

DRAWING NUMBER	051-02643
SIZE	D
REVISION	4.0.0
BRANCH	evt-0
PAGE	103 OF 200
SHEET	98 OF 131


UA400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
(2 OF 2)
OMIT_TABLE
UA450
PP1V5R1V35_S0_GPU_MEM
CK TERMINATION - A0
CK TERMINATION - A1
FB_A0_CLK_P
FB_A0_CLK_N
FB_A1_CLK_P
FB_A1_CLK_N
RA401
RA402
RA451
RA452
60.4
PLACE_NEAR=UA400.J11:8.4MM
PLACE_NEAR=UA400.J12:8.4MM
PLACE_NEAR=UA450.J11:8.4MM
PLACE_NEAR=UA450.J12:8.4MM
RA400
RA403
RA404
RA450
RA453
RA454
120
FB_A0_ZQ
FB_A0_MF
FB_A0_SEN
FB_A_RESET_L
FB_A0_ABI_L
FB_A0_CKE_L
FB_A0_CS_L
FB_A0_WE_L
FB_A0_CAS_L
FB_A0_RAS_L
FB_A0_EDC<0>
FB_A0_WCLK_P<0>
FB_A0_WCLK_N<0>
FB_A0_WCLK_P<1>
FB_A0_WCLK_N<1>
FB_A0_DBI_L<0>
FB_A0_DQ<0>
FB_A0_DQ<31>
FB_A0_A<8>
FB_A0_ZQ1
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN
FB_A1_ABI_L
FB_A1_DQ<0>
FB_A1_DQ<31>
FB_A1_A<8>
FB_A1_ZQ1
RA460
RA461
NOSTUFF
VDD
VSS
VDDQ
VSSQ
FB_A0_VREFC
FB_A0_VREFD
FB_A1_VREFC
FB_A1_VREFD
RA430
RA431
RA432
RA433
RA434
RA435
RA480
RA481
RA482
RA483
RA484
RA485
549
1.33K
931
CA431
CA432
CA433
CA481
CA482
CA483
820PF
FB_SW_LEG
MIN_LINE_WIDTH=0.0920
MIN_NECK_WIDTH=0.0850
PLACE_NEAR=UA400.J14:8.4MM
PLACE_NEAR=UA450.J14:8.4MM
PLACE_NEAR=UA450.U10:8.4MM
PLACE_NEAR=UA450.A10:8.4MM
PLACE CLOSE TO U9000
PLACE CLOSE TO U9050
CA400
CA496
12PF
CA497
3.0PF
4.7UF
1UF
0.1UF
CA450
CA475
BOM_COST_GROUP=GRAPHICS

PAGE TITLE

GDDR5 VRAM FB 1 [104]

Apple Inc.

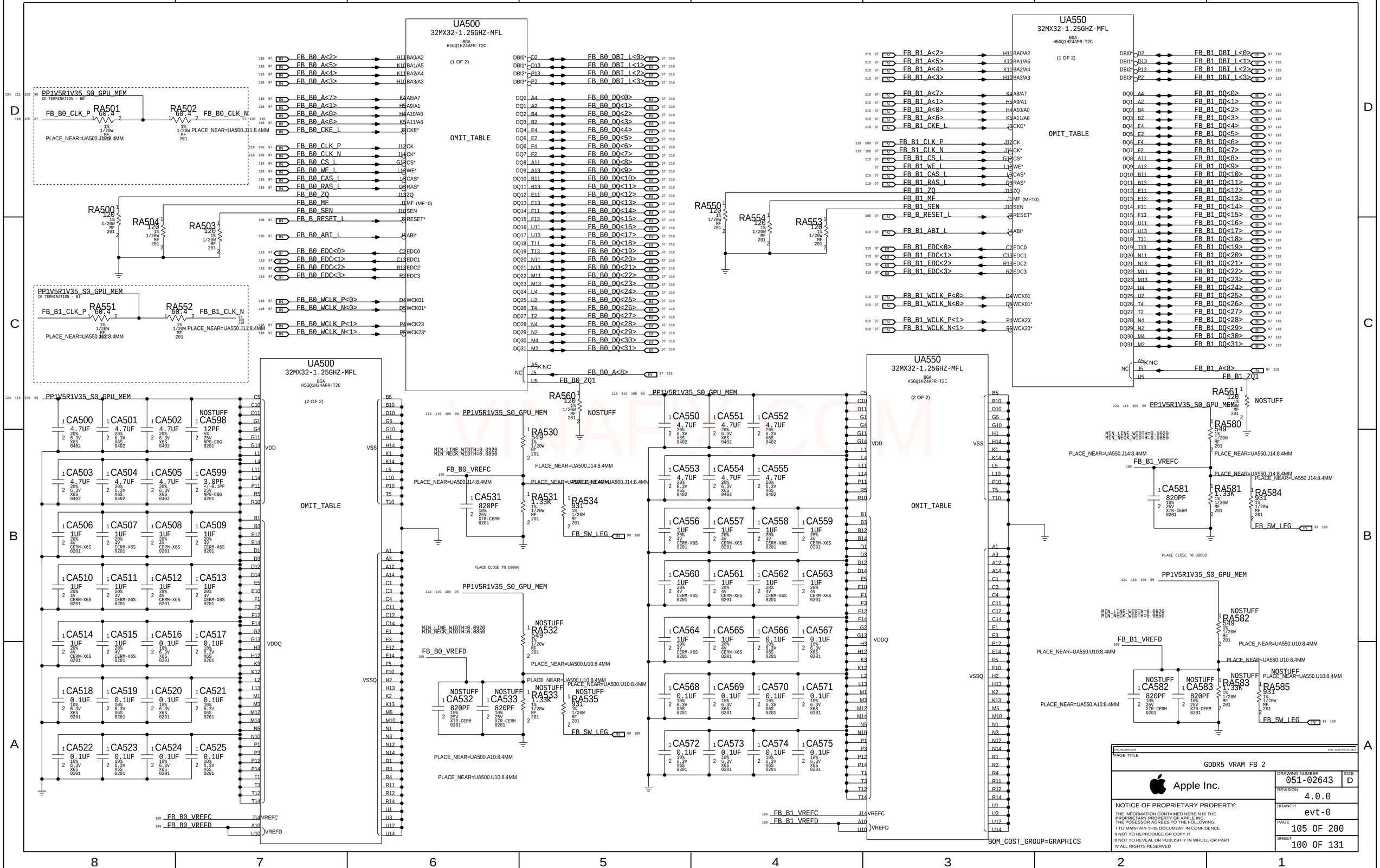
DRAWING NUMBER 051-02643 SIZE D

REVISION 4.0.0

BRANCH evt-0

PAGE 104 OF 200

SHEET 99 OF 131



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00174	2	MOSFET,CTRL+SYNC,25V,4.1/1.4MΩ,QFN32,6x6	QA640,QA650	CRITICAL	

GPU CORE SUPPLY

VOUT = 0.75-1.00V
64.2A MAX OUTPUT
F = 450 KHZ

UA600
ISL6277AHRZ-TR5740
QFN
BOMOPTION=OMIT_TABLE
CRITICAL

VDDIO = 1.14V - 1.95V

QA640 / QA650
IRF3575
CRITICAL

376S1136

LA640 / LA650
0.2UH-20%-28A-0.0011OHM
CRITICAL

RA641 / RA651
0.00075
CRITICAL

Line Width & DIDT on all DIDT nets

For 80A EDP

TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

ISL6277A datasheet (December 19,2012)

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: VR GPU Core

Apple Inc.

DRAWING NUMBER: 051-02643
SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
PAGE: 106 OF 200
SHEET: 101 OF 131

NOTICE THE ANNOYING MIX OF 3.3V AND 1.0V PULL-UPS

118 PP3V3_S0_GPU
118 PP1V8_S0_GPU

RA770 NOSTUFF 5.1K 1% 1/20W MF 201
RA771 NOSTUFF 5.1K 1% 1/20W MF 201
RA772 NOSTUFF 5.1K 1% 1/20W MF 201
RA773 NOSTUFF 5.1K 1% 1/20W MF 201
RA774 5.1K 1% 1/20W MF 201
RA775 NOSTUFF 5.1K 1% 1/20W MF 201
RA776 NOSTUFF 5.1K 1% 1/20W MF 201
RA777 NOSTUFF 5.1K 1% 1/20W MF 201
RA778 NOSTUFF 5.1K 1% 1/20W MF 201
RA79A NOSTUFF 5.1K 1% 1/20W MF 201

RA77A NOSTUFF 5.1K 1% 1/20W MF 201
RA77B 5.1K 1% 1/20W MF 201
RA77C NOSTUFF 5.1K 1% 1/20W MF 201
RA77D 5.1K 1% 1/20W MF 201
RA77E 5.1K 1% 1/20W MF 201
RA780 NOSTUFF 5.1K 1% 1/20W MF 201
RA781 5.1K 1% 1/20W MF 201
RA782 NOSTUFF 5.1K 1% 1/20W MF 201
RA783 NOSTUFF 5.1K 1% 1/20W MF 201
RA784 5.1K 1% 1/20W MF 201
RA79B NOSTUFF 5.1K 1% 1/20W MF 201

103	GPU_ROM_CONFIG<2>	0
103	GPU_ROM_CONFIG<1>	0
103	GPU_ROM_CONFIG<0>	1
103	GPU_AUD_PORT_CONN<2>	0
103	GPU_AUD_PORT_CONN<1>	0
103	GPU_AUD_PORT_CONN<0>	0
103	GPU_BIF_GEN3_EN_A	1
103	GPU_TX_HALF_SWING	0
103	GPU_TX_DEEMPH_EN	1
103 102	GPU_ROM_SO (strap BIF_CLK_PM_EN)	1
103 102	GPU_ROM_CS_L_R (strap BIOS_ROM_EN)	0
103	GPU_VGA_DIS	0
103	GPU_AUD<1>	1
103	GPU_AUD<0>	0
103	GPU_BRD_CFG<2>	0
103	GPU_BRD_CFG<1>	0
103	GPU_BRD_CFG<0>	0
103	GPU_SMBUS_ADDR<1>	0
103	GPU_SMBUS_ADDR<0>	1

RA785 5.1K 1% 1/20W MF 201
RA786 NOSTUFF 5.1K 1% 1/20W MF 201
RA787 5.1K 1% 1/20W MF 201
RA788 NOSTUFF 5.1K 1% 1/20W MF 201
RA789 NOSTUFF 5.1K 1% 1/20W MF 201
RA78A 5.1K 1% 1/20W MF 201
RA78B NOSTUFF 5.1K 1% 1/20W MF 201
RA78C 5.1K 1% 1/20W MF 201
RA78D 5.1K 1% 1/20W MF 201
RA78E NOSTUFF 5.1K 1% 1/20W MF 201

GPU_ROM_SI_R (strap reserved) 102 103
GPU_RESERVED 103

RA78F 5.1K 1% 1/20W MF 201
RA790 5.1K 1% 1/20W MF 201
RA791 5.1K 1% 1/20W MF 201
RA792 5.1K 1% 1/20W MF 201
RA793 NOSTUFF 5.1K 1% 1/20W MF 201
RA794 5.1K 1% 1/20W MF 201
RA795 5.1K 1% 1/20W MF 201
RA796 5.1K 1% 1/20W MF 201
RA797 5.1K 1% 1/20W MF 201
RA798 5.1K 1% 1/20W MF 201
RA799 5.1K 1% 1/20W MF 201

BAFFIN STRAPS

PCIe Gen3 enabled, FULL-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled, CLKREQ_L enabled
All power audio-capable display output
Audio for DP or HDMI dongle
256MB FB Aperture Size
SMBUS address 41

103 GPU_GPIO_SVC_R — RA750 22 1/20W 5% MF 201 — GPUVCORE_SVC_R OUT 101

103 GPU_GPIO_SVD_R — RA751 22 1/20W 5% MF 201 — GPUVCORE_SVD_R OUT 101

103 GPUVCORE_SVT = GPUVCORE_SVT IN 101
MAKE_BASE=TRUE

GPU ROM

115 PP3V3_S0_GPU
BOMOPTION=NOSTUFF

GPU_ROM:YES RA723 33 5% 1/20W MF 201 — GPU_ROM_SI_R 102 103 — GPU_ROM_SI
GPU_ROM:YES RA724 33 5% 1/20W MF 201 — GPU_ROM_SCLK_R 103 — GPU_ROM_SCLK
GPU_ROM:YES RA725 33 5% 1/20W MF 201 — GPU_ROM_CS_L_R 102 103 — GPU_ROM_CS_L

GPU_ROM:YES RA721 0 5% 1/20W MF 0201
RA720 5.1K 1% 1/20W MF 201 — GPU_ROM_WP_L 121
NO STUFF RA722 0 5% 1/20W MF 0201

UA701 M25P10A UFDFPN8
8 VCC
5 D
6 C
S* OMIT_TABLE
W*
HOLD*
VSS 4
THRM PAD 9
Q 2

GPU_ROM:YES CA721 0.1UF 10% 6.3V X6S 0201
GPU_ROM:YES RA726 33 5% 1/20W MF 201 — GPU_ROM_SO_R — GPU_ROM_SO

GPU JTAG

115 PP3V3_S0_GPU

NOSTUFF RA731 10K 5% 1/10W MF-LF 402
NOSTUFF RA732 10K 5% 1/10W MF-LF 402
NOSTUFF RA733 10K 5% 1/10W MF-LF 402
NOSTUFF RA734 10K 5% 1/10W MF-LF 402

102 103 NOSTUFF — GPU_JTAG_TDI 103 121
GPU_JTAG_TRST_L 103 121
GPU_JTAG_TMS 103 121
GPU_JTAG_TDO 103 121
GPU_JTAG_TCK 103 121

NOSTUFF RA730 10K 5% 1/10W MF-LF 402

GPU OSC 100 MHZ

116 PP1V8_S0_GPU — LA740 FERR-470-OHM 0201 — PP1V8_VDD_XTAL

CA742 0.1UF 10% 6.3V CERM-X5R 0201

RA741 10K 5% 1/20W MF 201

YA740 100MHZ-20PPM-1.8V 2.5X2.0-SM
VDD 4
OE/ST* 1
OUT 3
GND 2

GPU_CLK_YA740_OE — GPU_CLK_IN_R — RA743 33 1/20W 5% MF 201 — GPU_CLK_IN 103 118

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: GPU Baffin GPIO/CLK/Straps

Apple Inc.

DRAWING NUMBER: 051-02643
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BRANCH: evt-0
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BOMOPTION=OMIT_TABLE

PP1V8_S0_GPU
RA800 10K 5% 1/20W MF 201
GPU_BP_0
PP1V8_S0_GPU
RA802 10K 5% 1/20W MF 201
GPU_BP_1
PP3V3_S0_GPU
RA805 4.7K 5% 1/20W MF 201
RA806 4.7K 5% 1/20W MF 201
I2C isolation now on CSA 52 level shifting and isolation done by U5200
GPU_SMB_CLK
GPU_SMB_DAT
PP1V8_S0_GPU
PP3V3_S0_GPU
RA816 100K 5% 1/20W MF 201
GFX_THROTTLE_1V8_L
from H9M
UA802 SLSV1T344MU-COMBO UDFN CRITICAL
VCCA VCCB A B NC GND
NC_I2C_GPU_PCC_SCL
NC_I2C_GPU_PCC_SDA
GFX_THROTTLE_L
GPUVCORE_VR_HOT_L
GFX_SELF_THROTTLE_1V8
to H9M
RA813 1.5K MF 5% 1/20W
RA833 1.8K 5% 1/20W MF 201
GFX_SELF_THROTTLE
GPU_VRAM_STRAP
RA823 10K 5% 1/20W MF 201
PLACE_NEAR=LA800.1:2.54MM
LA800 1200HM-25%-1.8A-0.06DCR 0402
VOLTAGE=1.8V MIN_LINE_WIDTH=0.4000 MIN_NECK_WIDTH=0.2000
PP1V8_S0_GPU
PP1V8_GPU_TSVDD
CA850 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=UA000.AM13:2.54MM
CA851 10UF 20% 6.3V CERM-X6S 0402
CA852 1UF 20% 6.3V X6S-CERM 0201
CA853 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=UA000.AM13:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM

EG_BKLT_EN
RA821 10K 5% 1/20W MF 201
NC_EG_BKLT_PWM

GPU_BP_0
GPU_BP_1
GPU_AUD_PORT_CONN<0>
GPU_AUD_PORT_CONN<1>
GPU_AUD_PORT_CONN<2>
GPU_BRD_CFG<0>
GPU_BRD_CFG<1>
GPU_BRD_CFG<2>
GPU_SMBUS_ADDR<0>
GPU_SMBUS_ADDR<1>
TPA802 GPU_DBG_8
TPA803 GPU_DBG_9
TPA804 GPU_DBG_10
TPA805 GPU_DBG_11
TPA807 GPU_MPLS_PS_0
TPA808 GPU_MPLS_PS_1
TPA809 GPU_MPLS_PS_2
TPA810 GPU_MPLS_PS_3
WAKE*
ANALOGIO
GPU_GPIO_SVC_R
GPU_GPIO_SVD_R
GPUVCORE_SVT
SWAPLOCKA
SWAPLOCKB
NC_GPU_XTAL_OUT
GPU_TX_HALF_SWING
NC_GFX_VDDCI_ALTV_ZERO
GPU_BIF_GEN3_EN_A
SMBCLK
SMBDAT
GFX_THROTTLE_L
GPUVCORE_VR_HOT_L
GPU_ROM_SO (strap BIFCLK_PM_EN)
GPU_ROM_SI_R (strap reserved)
GPU_ROM_SCLK_R
GPU_ROM_CONFIG<0>
GPU_ROM_CONFIG<1>
GPU_ROM_CONFIG<2>
DP_X_SNK0_HPD_EG
GPU_RESERVED
GFX_VDDCI_ALTV_ONE
GFX_SELF_THROTTLE
DP_X_SNK1_HPD_EG
GPU_GFX_OVERTEMP
GPU_TX_DEEMPH_EN
GPU_VRAM_STRAP
GPU_ROM_CS_L_R (strap BIOS_ROM_EN)
GPU_VGA_DIS
GPUVDDC_PCC_ALERT_L
GPU_JTAG_TRST_L
GPU_JTAG_TDI
GPU_JTAG_TCK
GPU_JTAG_TMS
GPU_JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
DP_T_SNK0_HPD_EG
DP_T_SNK1_HPD_EG
GENERICG
DP_INT_EG_HPD
GPU_CLK_IN
NC_GPU_XTAL_OUT
GPU_TDIODE_P
GPU_TDIODE_N
TS_A

UA000 100-CK4803-ES BGA SYM 2 OF 7

PLLCHARZ_H
PLLCHARZ_L
BL_ENABLE
BL_PWM_DIM
BP_0
BP_1
DBGDATA_0
DBGDATA_1
DBGDATA_2
DBGDATA_3
DBGDATA_4
DBGDATA_5
DBGDATA_6
DBGDATA_7
DBGDATA_8
DBGDATA_9
DBGDATA_10
DBGDATA_11
DBGDATA_12
DBGDATA_13
DBGDATA_14
DBGDATA_15
GPIO_SVC
GPIO_SVD
GPIO_SVT
SCL
SDA
GPIO_0
GPIO_1
GPIO_2
GPIO_5_REG_HOT_AC_BATT
GPIO_6_TACH
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15
GPIO_16_8P_DETECT
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20
GPIO_21
GPIO_22_ROMCS*
GPIO_28_FDO
GPIO_29
GPIO_30
JTAG_TRST*
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF_HPD5
GENERICG
HPD1
XTALIN
XTALOUT
DPLUS
DMINUS
TS_A
TSVDD

TXCAP_DPA3+ AY33 DP_INT_EG_ML_P<3>
TXCAM_DPA3- BA33 DP_INT_EG_ML_N<3>
TX3P_DPA2+ AY34 DP_INT_EG_ML_P<2>
TX3M_DPA2- BA34 DP_INT_EG_ML_N<2>
TX4P_DPA1+ AY35 DP_INT_EG_ML_P<1>
TX4M_DPA1- BA35 DP_INT_EG_ML_N<1>
TX5P_DPA0+ AY36 DP_INT_EG_ML_P<0>
TX5M_DPA0- BA36 DP_INT_EG_ML_N<0>
TXCBP_DPB3+ AY28 DP_X_SNK0_ML_C_P<3>
TXCBM_DPB3- BA28 DP_X_SNK0_ML_C_N<3>
TX0P_DPB2+ AY30 DP_X_SNK0_ML_C_P<2>
TX0M_DPB2- BA30 DP_X_SNK0_ML_C_N<2>
TX1P_DPB1+ AY31 DP_X_SNK0_ML_C_P<1>
TX1M_DPB1- BA31 DP_X_SNK0_ML_C_N<1>
TX2P_DPB0+ AY32 DP_X_SNK0_ML_C_P<0>
TX2M_DPB0- BA32 DP_X_SNK0_ML_C_N<0>
TXCCP_DPC3+ AY24 DP_X_SNK1_ML_C_P<3>
TXCCM_DPC3- BA24 DP_X_SNK1_ML_C_N<3>
TX3P_DPC2+ AY25 DP_X_SNK1_ML_C_P<2>
TX3M_DPC2- BA25 DP_X_SNK1_ML_C_N<2>
TX4P_DPC1+ AY26 DP_X_SNK1_ML_C_P<1>
TX4M_DPC1- BA26 DP_X_SNK1_ML_C_N<1>
TX5P_DPC0+ AY27 DP_X_SNK1_ML_C_P<0>
TX5M_DPC0- BA27 DP_X_SNK1_ML_C_N<0>
TXCDP_DPD3+ AY19 DP_T_SNK0_ML_C_P<3>
TXCDM_DPD3- BA19 DP_T_SNK0_ML_C_N<3>
librarian reordered pins to follow tx
TX2P_DPD0+ AY22 DP_T_SNK0_ML_C_P<0>
TX2M_DPD0- BA22 DP_T_SNK0_ML_C_N<0>
TX1P_DPD1+ AY21 DP_T_SNK0_ML_C_P<1>
TX1M_DPD1- BA21 DP_T_SNK0_ML_C_N<1>
librarian reordered pins to follow tx
TX0P_DPD2+ AY20 DP_T_SNK0_ML_C_P<2>
TX0M_DPD2- BA20 DP_T_SNK0_ML_C_N<2>
TXCEP_DPE3+ AY14 DP_T_SNK1_ML_C_P<3>
TXCEM_DPE3- BA14 DP_T_SNK1_ML_C_N<3>
TX0P_DPE2+ AY15 DP_T_SNK1_ML_C_P<2>
TX0M_DPE2- BA15 DP_T_SNK1_ML_C_N<2>
TX1P_DPE1+ AY16 DP_T_SNK1_ML_C_P<1>
TX1M_DPE1- BA16 DP_T_SNK1_ML_C_N<1>
TX2P_DPE0+ AY18 DP_T_SNK1_ML_C_P<0>
TX2M_DPE0- BA18 DP_T_SNK1_ML_C_N<0>
HSYNC W34 GPU_AUD<1>
VSYNC W35 GPU_AUD<0>
DIGON AC40 EG_LCD_PWR_EN
TEMPIN0 J8 NC
TEMPINRETURN J7 NC
TEST6 B2 GPU_DIECRACKMON
TEST_PG_BACO BA13 GPU_TEST_PG_BACON
GENLK_CLK AP28 NC
GENLK_VSYNC AP29 NC
CLKREQ* AV40 GPU_CLKREQ_L
RA811 0 5% 1/20W MF 0201
RA815 10K 5% 1/20W MF 201
RA810 1K 5% 1/20W MF 201
PP1V8_S0_GPU
DDC1CLK AY10 NC
DDC1DATA BA10 NC
AUX1+ AY11 DP_INT_EG_AUX_P
AUX1- BA11 DP_INT_EG_AUX_N
DDC2CLK AY12 NC
DDC2DATA AY13 NC
AUX2+ AP19 DP_X_SNK0_AUXCH_C_P
AUX2- AM19 DP_X_SNK0_AUXCH_C_N
DDCAUX3+ AM21 DP_X_SNK1_AUXCH_C_P
DDCAUX3- AP21 DP_X_SNK1_AUXCH_C_N
DDCAUX4+ AR23 DP_T_SNK0_AUXCH_C_P
DDCAUX4- AP23 DP_T_SNK0_AUXCH_C_N
DDCAUX5+ AU27 DP_T_SNK1_AUXCH_C_P
DDCAUX5- AV27 DP_T_SNK1_AUXCH_C_N
DDCVGACLK AP24 NC
DDCVGADATA AP25 NC
RSVD K41 NC
RSVD B34 NC

GPU_PLLCHARZ_H
GPU_PLLCHARZ_L
GPU_PLLCHARZ_RC_H
NOSTUFF CA880 0.1UF 10% 6.3V X6S 0201
NOSTUFF CA881 0.1UF 10% 6.3V X6S 0201
GPU_PLLCHARZ_RC_L
NOSTUFF RA880 51.1 1% 1/20W MF 201
NOSTUFF RA881 51.1 1% 1/20W MF 201

BOM_COST_GROUP=GRAPHICS

PAGE TITLE
GPU Baffin DP/GPIO
Apple Inc.
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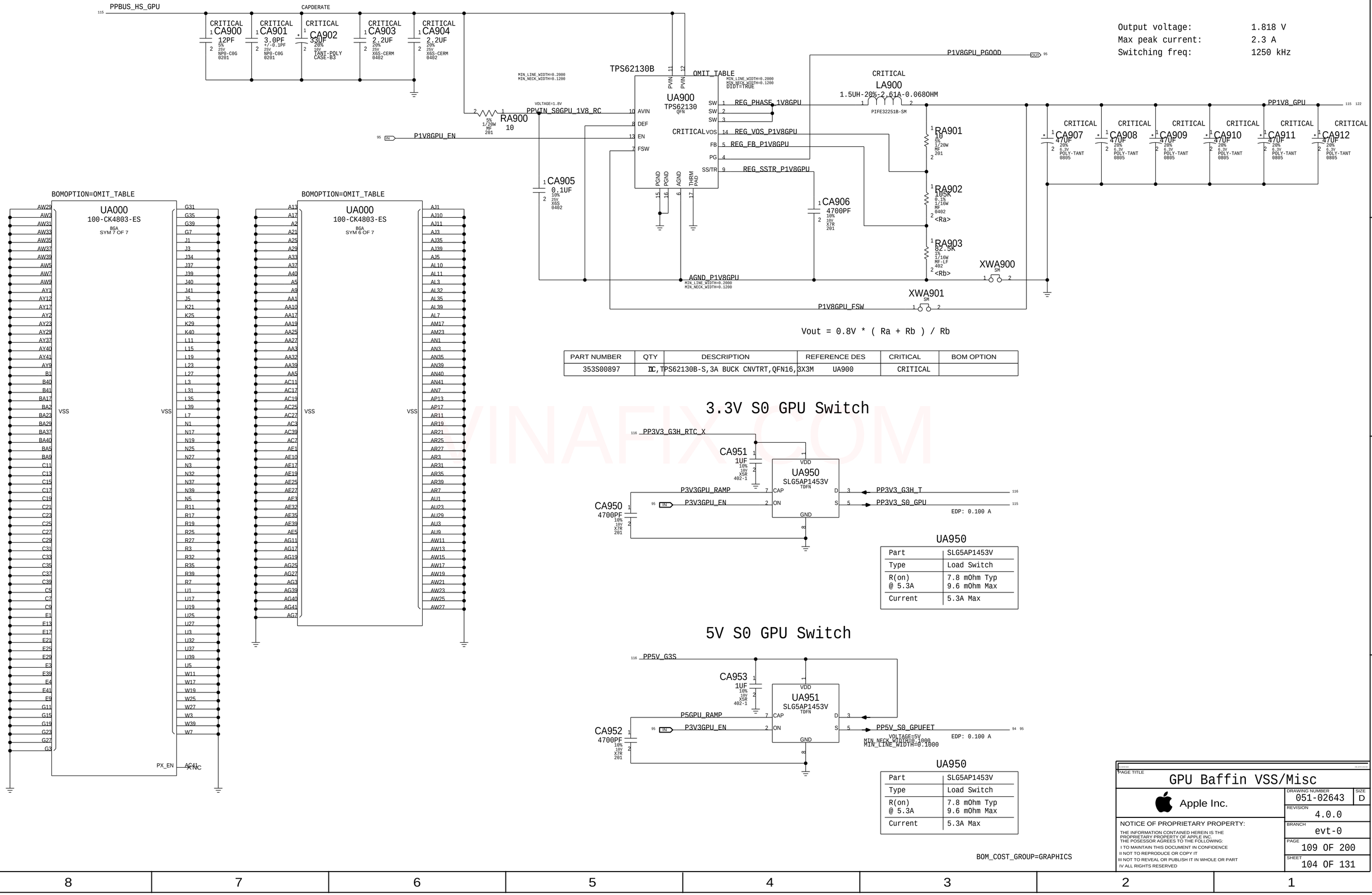

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00897	1	IC,TPS62130B-S,3A BUCK CNVTRT,QFN16,3X3M	UA900	CRITICAL	

3.3V S0 GPU Switch

UA950

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

5V S0 GPU Switch

UA950

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: GPU Baffin VSS/Misc

Apple Inc.

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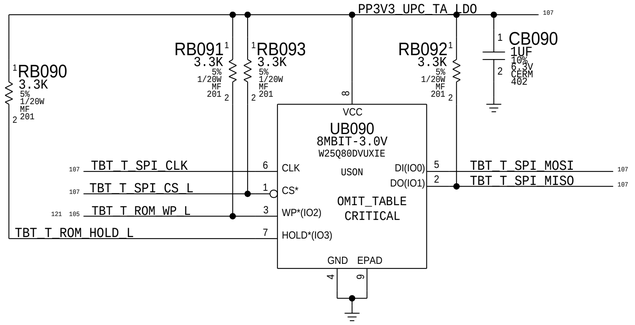
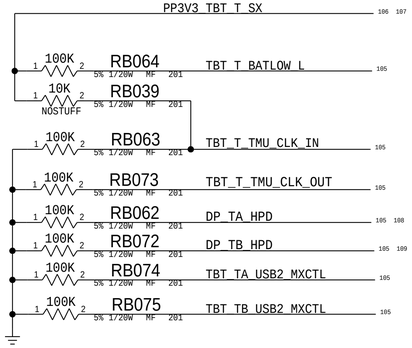


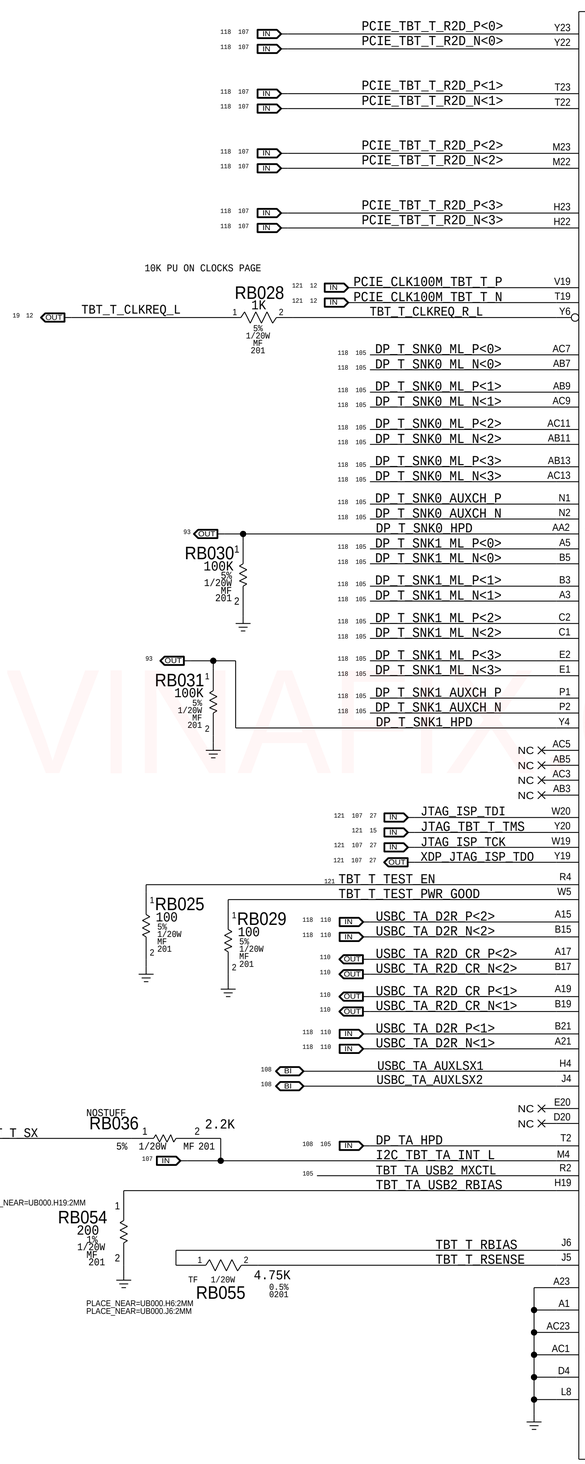
SNK0 AC Coupling

DP_T_SNK0_ML_C_P<0>	CB020	0.22UF	DP_T_SNK0_ML_P<0>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<0>	CB021	0.22UF	DP_T_SNK0_ML_N<0>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<1>	CB022	0.22UF	DP_T_SNK0_ML_P<1>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<1>	CB023	0.22UF	DP_T_SNK0_ML_N<1>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<2>	CB024	0.22UF	DP_T_SNK0_ML_P<2>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<2>	CB025	0.22UF	DP_T_SNK0_ML_N<2>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<3>	CB026	0.22UF	DP_T_SNK0_ML_P<3>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<3>	CB027	0.22UF	DP_T_SNK0_ML_N<3>	GND_VOID=TRUE	
DP_T_SNK0_AUXCH_C_P	CB028	0.1UF	DP_T_SNK0_AUXCH_P	GND_VOID=TRUE	
DP_T_SNK0_AUXCH_C_N	CB029	0.1UF	DP_T_SNK0_AUXCH_N	GND_VOID=TRUE	

SNK1 AC Coupling

DP_T_SNK1_ML_C_P<0>	CB030	0.22UF	DP_T_SNK1_ML_P<0>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<0>	CB031	0.22UF	DP_T_SNK1_ML_N<0>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<1>	CB032	0.22UF	DP_T_SNK1_ML_P<1>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<1>	CB033	0.22UF	DP_T_SNK1_ML_N<1>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<2>	CB034	0.22UF	DP_T_SNK1_ML_P<2>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<2>	CB035	0.22UF	DP_T_SNK1_ML_N<2>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<3>	CB036	0.22UF	DP_T_SNK1_ML_P<3>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<3>	CB037	0.22UF	DP_T_SNK1_ML_N<3>	GND_VOID=TRUE	
DP_T_SNK1_AUXCH_C_P	CB038	0.1UF	DP_T_SNK1_AUXCH_P	GND_VOID=TRUE	
DP_T_SNK1_AUXCH_C_N	CB039	0.1UF	DP_T_SNK1_AUXCH_N	GND_VOID=TRUE	





BOM_COST_GROUP=TBT

DRAWING	LAST_MODIFIED=Fri Jan 26 13:26:51 2018
PAGE TITLE	USB-C HIGH SPEED 1
Apple Inc.	DRAWING NUMBER 051-02643
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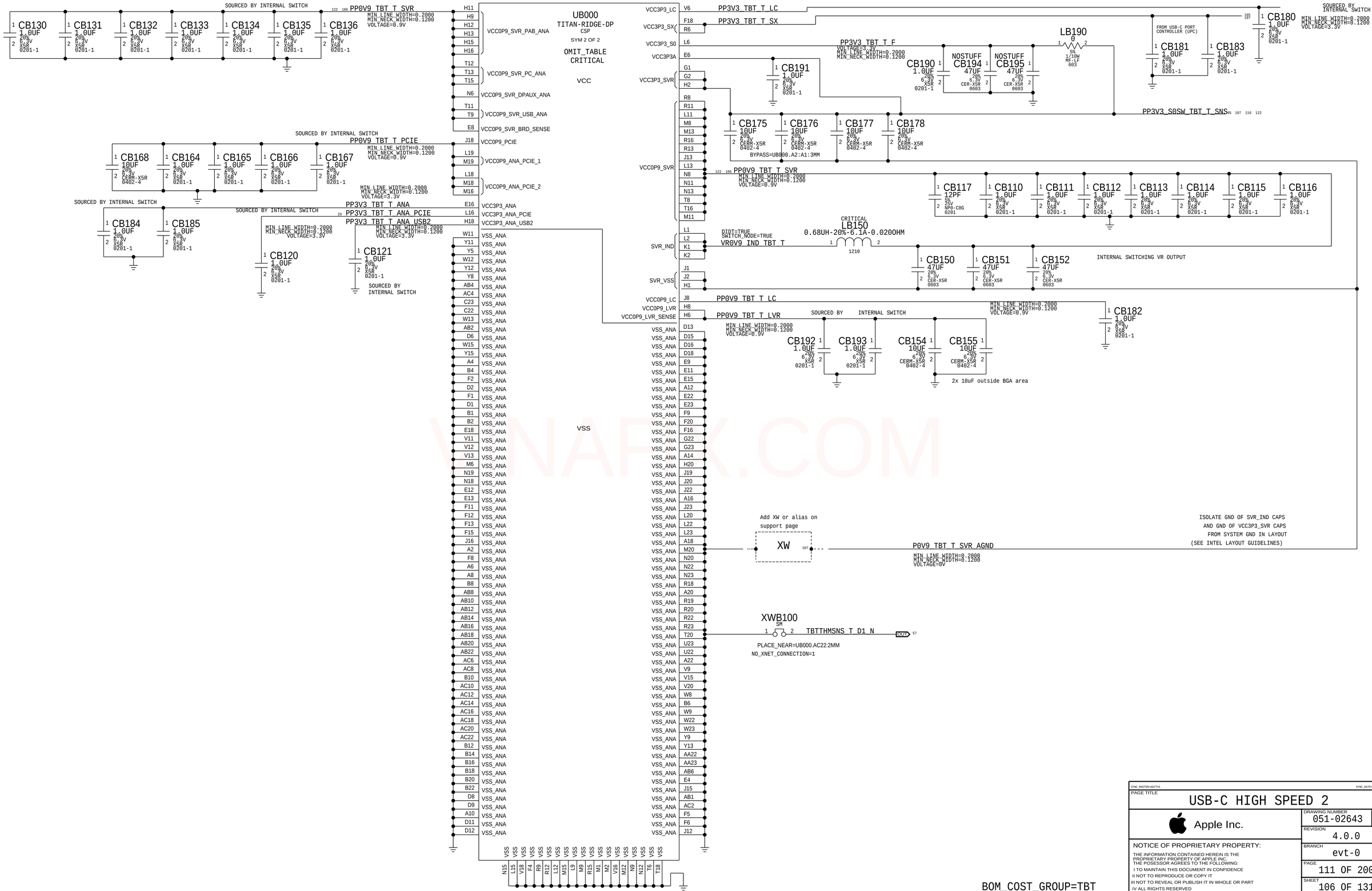

SYNC_MASTER=ADDTYA SYNC_DATE=04/03/2017

PAGE TITLE

USB-C HIGH SPEED 2

Apple Inc.

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DP SRC OPTIONS
IF DP SRC NOT USED

RB240 100K 5% 1/20W MF 201
105 DP_T_SRC_HPD

105 =DP_T_SRC_ML_P<3..0> = NC_DP_T_SRC_ML_P<3..0> MAKE_BASE=TRUE NO_TEST=1
105 =DP_T_SRC_ML_N<3..0> = NC_DP_T_SRC_ML_N<3..0> MAKE_BASE=TRUE NO_TEST=1
105 NC_DP_T_SRC_AUX_P = NC_DP_T_SRC_AUX_P MAKE_BASE=TRUE NO_TEST=1
105 NC_DP_T_SRC_AUX_N = NC_DP_T_SRC_AUX_N MAKE_BASE=TRUE NO_TEST=1

FUSES FOR UPC

PLACE_NEAR=QB300:5MM
CRITICAL
FB200 0603 6AMP-32V-0.00950HM
108 107 PP20V_USBC_TA_VBUS 1 2 PP20V_USBC_TA_VBUS_F 108

PLACE_NEAR=QB400:5MM
CRITICAL
FB201 0603 740S0135 6AMP-32V-0.00950HM
109 107 PP20V_USBC_TB_VBUS 1 2 PP20V_USBC_TB_VBUS_F 109

25MHz xtal

118 105 IN TBT_T_XTAL25M_OUT
118 105 OUT TBT_T_XTAL25M_IN
to/from Ridge
CRITICAL
YB200 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
CB202 20PF 5% 25V C0G 0201
CB203 20PF 5% 25V C0G 0201

AR/ACE SPI BUS SERIES R'S

ROM
105 TBT_T_SPI_CLK
105 TBT_T_SPI_CS_L
105 TBT_T_SPI_MOSI
105 TBT_T_SPI_MISO

RB290 100 5% 1/20W MF 201 TBT_T_SPI_CLK_DBG 107
RB280 15 5% 1/20W MF 201 UPC_TA_SPI_CLK IN 108
RB281 15 5% 1/20W MF 201 UPC_TA_SPI_CS_L IN 108
RB282 15 5% 1/20W MF 201 UPC_TA_SPI_MOSI IN 108
RB283 15 5% 1/20W MF 201 UPC_TA_SPI_MISO OUT 108
RB284 15 5% 1/20W MF 201 UPC_T_SPI_CLK IN 29 105
RB285 15 5% 1/20W MF 201 UPC_T_SPI_CS_L IN 29 105
RB286 15 5% 1/20W MF 201 UPC_T_SPI_MOSI IN 29 105
RB287 15 5% 1/20W MF 201 UPC_T_SPI_MISO OUT 29 105

Ace
AR

TBT to ACE

TBT
Alpine Ridge U2800
(MASTER)

Pri ACE
U3100
(Write: 0x70 Read: 0x71)

MAKE_BASE=TRUE I2C_TBT_T_SCL = I2C_TBT_T_SCL 108
MAKE_BASE=TRUE I2C_TBT_T_SDA = I2C_TBT_T_SDA 108
MAKE_BASE=TRUE I2C_TBT_TA_INT_L = I2C_TBT_TA_INT_L 108
MAKE_BASE=TRUE I2C_TBT_TB_INT_L

Sec ACE
U3200
(Write: 0x7E Read: 0x7F)

I2C_TBT_T_SCL 109
I2C_TBT_T_SDA 109
I2C_TBT_TB_INT_L 109

Ridge PCIE Caps

R2D

GND_VOID=TRUE
118 117 IN PCIE_TBT_T_R2D_C_P<0> 2 1 CB240 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_R2D_P<0> OUT 105 118
GND_VOID=TRUE
118 117 IN PCIE_TBT_T_R2D_C_N<0> 2 1 CB241 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_R2D_N<0> OUT 105 118
GND_VOID=TRUE
118 117 IN PCIE_TBT_T_R2D_C_P<1> 2 1 CB242 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_R2D_P<1> OUT 105 118
GND_VOID=TRUE
118 117 IN PCIE_TBT_T_R2D_C_N<1> 2 1 CB243 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_R2D_N<1> OUT 105 118
GND_VOID=TRUE
118 117 IN PCIE_TBT_T_R2D_C_P<2> 2 1 CB244 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_R2D_P<2> OUT 105 118
GND_VOID=TRUE
118 117 IN PCIE_TBT_T_R2D_C_N<2> 2 1 CB245 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_R2D_N<2> OUT 105 118
GND_VOID=TRUE
118 117 IN PCIE_TBT_T_R2D_C_P<3> 2 1 CB246 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_R2D_P<3> OUT 105 118
GND_VOID=TRUE
118 117 IN PCIE_TBT_T_R2D_C_N<3> 2 1 CB247 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_R2D_N<3> OUT 105 118

D2R

GND_VOID=TRUE
118 105 IN PCIE_TBT_T_D2R_C_P<0> 2 1 CB250 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_D2R_P<0> OUT 117 118
GND_VOID=TRUE
118 105 IN PCIE_TBT_T_D2R_C_N<0> 2 1 CB251 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_D2R_N<0> OUT 117 118
GND_VOID=TRUE
118 105 IN PCIE_TBT_T_D2R_C_P<1> 2 1 CB252 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_D2R_P<1> OUT 117 118
GND_VOID=TRUE
118 105 IN PCIE_TBT_T_D2R_C_N<1> 2 1 CB253 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_D2R_N<1> OUT 117 118
GND_VOID=TRUE
118 105 IN PCIE_TBT_T_D2R_C_P<2> 2 1 CB254 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_D2R_P<2> OUT 117 118
GND_VOID=TRUE
118 105 IN PCIE_TBT_T_D2R_C_N<2> 2 1 CB255 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_D2R_N<2> OUT 117 118
GND_VOID=TRUE
118 105 IN PCIE_TBT_T_D2R_C_P<3> 2 1 CB256 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_D2R_P<3> OUT 117 118
GND_VOID=TRUE
118 105 IN PCIE_TBT_T_D2R_C_N<3> 2 1 CB257 0201 X5R 6.3V 20% 0.22UF PCIE_TBT_T_D2R_N<3> OUT 117 118

USBC 5V EN PD

112 107 UPC_T_5V_EN RB232 100K 5% 1/20W MF 201 108

ACE FET DCIN Bypass Caps

PPDCIN_G3H 29 30 31 108 109
CB211 0.10UF 10% 35V CER-X5R 0201
CB212 0.10UF 10% 35V CER-X5R 0201
CB213 0.10UF 10% 35V CER-X5R 0201
CB214 0.10UF 10% 35V CER-X5R 0201

ACE A/B RPD STRAPPING

108 USBC_TA_CC1 = USBC_TA_CC1 MAKE_BASE=TRUE 108 111
109 USBC_TB_CC1 = USBC_TB_CC1 MAKE_BASE=TRUE 109 111
108 USBC_TA_CC2 = USBC_TA_CC2 MAKE_BASE=TRUE 108 111
109 USBC_TB_CC2 = USBC_TB_CC2 MAKE_BASE=TRUE 109 111

ACE PDs

80 PP1V8_SLPS2R
NOSTUFF RB268 47K 5% 1/20W MF 201
NOSTUFF RB267 47K 5% 1/20W MF 201

108 UPC_TA_DBG3 RB260 100K 5% 1/20W MF 201
108 UPC_TA_DBG4 RB261 100K 5% 1/20W MF 201
109 UPC_TB_DBG3 RB262 100K 5% 1/20W MF 201
109 UPC_TB_DBG4 RB263 100K 5% 1/20W MF 201
NOSTUFF SMC_DEBUGPRT_TX RB264 100K 5% 1/20W MF 201
NOSTUFF SMC_DEBUGPRT_RX RB265 100K 5% 1/20W MF 201
108 TBT_TA_LSTX RB235 100K 5% 1/20W MF 201
108 TBT_TA_LSRX RB236 100K 5% 1/20W MF 201
109 TBT_TB_LSTX RB237 100K 5% 1/20W MF 201
109 TBT_TB_LSRX RB238 100K 5% 1/20W MF 201
109 UPC_TB_DBG1 RB266 100K 5% 1/20W MF 201
109 UPC_TB_DBG2 RB239 100K 5% 1/20W MF 201
108 UPC_TA_GPIO7 RB243 100K 5% 1/20W MF 201
109 UPC_TB_GPIO7 RB249 100K 5% 1/20W MF 201

GND ALIASES

MAKE_BASE=TRUE
108 GND
109 GND
108 GND
109 GND
108 GND
100 GND
109 GND
109 GND
109 GND
108 GND
109 GND

I2C SERIES R'S

108 I2C_UPC_T_SDA2 RB241 33 5% 1/20W MF 201 PLACE_NEAR=U3900.J4:5mm I2C_UPC_SDA 51
109 I2C_UPC_T_SDA2 MAKE_BASE=TRUE
107 I2C_UPC_T_SDA2
108 I2C_UPC_T_SCL2 RB242 33 5% 1/20W MF 201 PLACE_NEAR=U3900.M3:5mm I2C_UPC_SCL 51
109 I2C_UPC_T_SCL2 MAKE_BASE=TRUE
107 I2C_UPC_T_SCL2

ACE ARKANOID CONN

Place on bottom
USBC_DBG
JB200 505076-1222 M-ST-SM

107 100 CKPLUS_WAIVE=I2C_PULLUP	I2C_TBT_TB_INT_L 1	2 I2C_TBT_TA_INT_L	105 107
CKPLUS_WAIVE=I2C_PULLUP	I2C_UPC_T_SCL2 3	4 I2C_TBT_T_SDA	105 107
107	I2C_UPC_T_SDA2 5	6 I2C_TBT_T_SCL	105 107
51 39 29	UPC_I2C_INT_L 7	8 TBT_T_CIO_PWR_EN	14 105 108 109
107	TBT_T_SPI_CLK_DBG 9	10 TBT_T_USB_PWR_EN	14 105 108 109
109 108	UPC_TA_UART_TX 11	12 UPC_TA_UART_RX	108 109
	15	16	

SIGNAL ALIASES

MAKE_BASE=TRUE
USB2_UPC_TB_P = USB2_UPC_TB_P 14 119
USB2_UPC_TB_N = USB2_UPC_TB_N 14 119
USB2_UPC_TA_P = USB2_UPC_TA_P 14 119
USB2_UPC_TA_N = USB2_UPC_TA_N 14 119

MAKE_BASE=TRUE
108 USBC_T_RESET_L = USBC_T_RESET_L 105
108 UPC_T_5V_EN = UPC_T_5V_EN 107 112
109 UPC_T_5V_EN
109 TP_USBC_TB_RESET_L = TP_USBC_TB_RESET_L
109 108 IN TBT_POC_RESET = TBT_POC_RESET OUT 15 29
108 UPC_PMU_RESET = UPC_PMU_RESET 29 67 77 119
109 UPC_PMU_RESET
121 105 27 XDP_JTAG_ISP_TDO = XDP_JTAG_ISP_TDO 14
105 TBT_T_HDMI_DDC_DATA = TBT_T_HDMI_DDC_DATA 95 120
105 TBT_T_HDMI_DDC_CLK = TBT_T_HDMI_DDC_CLK 95 120

121 105 27 JTAG_ISP_TDI RB256 0 5% 1/20W MF 0201 XDP_JTAG_ISP_TDI 14
121 105 27 JTAG_ISP_TCK RB257 0 5% 1/20W MF 0201 XDP_JTAG_ISP_TCK 14
108 IN UPC_TA_FAULT_L RB258 0 5% 1/20W MF 0201 XDP_USB_EXTC_OC_L 14
109 IN UPC_TB_FAULT_L RB259 0 5% 1/20W MF 0201 XDP_USB_EXTD_OC_L 14

POWER ALIASES

105 PP3V3_UPC_TA_LDO = MAKE_BASE=TRUE PP3V3_UPC_TA_LDO 108
108 107 PP20V_USBC_TA_VBUS = MAKE_BASE=TRUE PP20V_USBC_TA_VBUS 110 120 122
109 107 PP20V_USBC_TB_VBUS = MAKE_BASE=TRUE PP20V_USBC_TB_VBUS 110 120 122

108 PP5V_S4_T_USBC
109 PP5V_S4_T_USBC
122 112 PP5V_S4_T_USBC = MAKE_BASE=TRUE PP5V_S4_T_USBC MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=5V
96 122 PP3V3_S0SW_TBT_T_SNS = MAKE_BASE=TRUE PP3V3_S0SW_TBT_T_SNS MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V
108 PP3V3_TBT_T_SX
109 PP3V3_TBT_T_SX = MAKE_BASE=TRUE PP3V3_TBT_T_SX MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 PP3V3_TBT_T_SX 105 106

108 PP1V8_SLPS2R
109 PP1V8_SLPS2R = PP1V8_SLPS2R 29 80

NO TEST

109 IN NC_UPC_TB_I2C_ADDR

RIDGE 0.9V SVR XW

XWB200 SM
106 P0V9_TBT_T_SVR_AGND
NO_XNET_CONNECTION=1

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C T Support

Apple Inc.

DRAWING NUMBER: 051-02643
SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
PAGE: 112 OF 200
SHEET: 107 OF 131

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

QB300
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

107 PP20V_USBC_TA_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V

107 PP20V_USBC_TA_VBUS

CB301 1UF 10% 50V X5R 0402

PPDCIN_G3H 29 30 31 107 109
MAX 100uF TOTAL ON RAIL

UPC_TA_GATE1
UPC_TA_GATE2

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
PP3V3_UPC_TA_LDO 107

PP3V3_TBT_T_SX 107

PP1V8_UPC_TA_LDOA

PP1V8_UPC_TA_LDOD

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V

PP1V1_UPC_TA_LDO_BMC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V

CB304 2.2UF 20% 6.3V X5R-CERM 0201
CB305 1.0UF 20% 6.3V X5R 0201-1
CB306 0.47UF 10% 6.3V CERM-X5R 0201
CB308 10UF 20% 6.3V CERM-X5R 0402-1

107 PP1V8_SLPS2R
116 PP3V3_G3H_RTC_X
107 PP5V_S4_T_USBC

CAP FOR PP_5V0 ON VR PAGE

RB369 100K 5% 1/20W MF 201
PHV_INT_TA_G3H

CB302 1.0UF 20% 6.3V X5R 0201-1
CB300 10UF 20% 6.3V CERM-X5R 0402-1

PULL R3109 AND R3108 UP TO ACE's LDO5 FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES

GND 107

RB309 1M 5% 1/20W MF 201 I2C_UPC_TA_DBG_CTL_SCL CKPLUS_WAIVE=I2C_PULLUP 108
RB308 1M 5% 1/20W MF 201 I2C_UPC_TA_DBG_CTL_SDA CKPLUS_WAIVE=I2C_PULLUP 108

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

UB300
CD3215A
BGA
CRITICAL
OMIT_TABLE

109 107 IN	TBT_POC_RESET	E11	MRESET	PRIMARY ONLY
107 OUT	USBC_T_RESET_L	F11	RESET*	PRIMARY ONLY
121	UPC_TA_GPIO0	B2	GPIO0	
121	UPC_TA_GPIO1	C2	GPIO1	
109 107 105 14 IN	TBT_T_CIO_PWR_EN	D10	GPIO2	
109 107 105 14 IN	TBT_T_USB_PWR_EN	G11	GPIO3	
105 OUT	DP_TA_HPD	C10	GPIO4	
107	UPC_PMU_RESET	E10	GPIO5	
107 OUT	UPC_T_5V_EN	G10	GPIO6	
107 OUT	UPC_TA_GPIO7	D7	GPIO7	
107 OUT	UPC_TA_FAULT_L	H6	GPIO8	
107 IN	GND	F10	BUSPOWERZ	
GND I2C ADDR PRIMARY ONLY	GND	F1	I2C_ADDR	
CRITICAL	UPC_TA_R_OSC	G2	R_OSC	
108	I2C_UPC_TA_DBG_CTL_SCL	E4	DEBUG_CTL1	
108	I2C_UPC_TA_DBG_CTL_SDA	D5	DEBUG_CTL2	
107 BI	I2C_TBT_T_SDA	D1	I2C_SDA1	
107 BI	I2C_TBT_T_SCL	D2	I2C_SCL1	
107 OUT	I2C_TBT_TA_INT_L	C1	I2C_IRQ1*	
107 BI	I2C_UPC_T_SDA2	A5	I2C_SDA2	
107 BI	I2C_UPC_T_SCL2	B5	I2C_SCL2	
51 OUT	UPC_I2C_INT_L	B6	I2C_IRQ2*	
107 OUT	UPC_TA_SPI_CLK	A3	SPI_CLK	
107 OUT	UPC_TA_SPI_MOSI	B4	SPI_MOSI	
107 IN	UPC_TA_SPI_MISO	A4	SPI_MISO	
107 OUT	UPC_TA_SPI_CS_L	B3	SPI_SSZ	
	TP_UPC_TA_SWD_DATA	F4	SWD_DATA	
	TP_UPC_TA_SWD_CLK	G4	SWD_CLK	
109 108 107 IN	UPC_TA_UART_RX	F2	UART_RX	
109 107 OUT	UPC_TA_UART_TX	E2	UART_TX	
107 IN	TBT_TA_LSTX	L4	LSX_R2P	
107 OUT	TBT_TA_LSRX	K4	LSX_P2R	
	USB_UPC_TA_F_P	L5	USB_RP_P	
	USB_UPC_TA_F_N	K5	USB_RP_N	
105 BI	USBC_TA_AUXLSX1	J1	AUX_P	
105 BI	USBC_TA_AUXLSX2	J2	AUX_N	
107 47 BI	SMC_DEBUGPRT_TX	L2	DEBUG1	
107 47 BI	SMC_DEBUGPRT_RX	K2	DEBUG2	
107 BI	UPC_TA_DBG3	L3	DEBUG3	
107 BI	UPC_TA_DBG4	K3	DEBUG4	

PP_5V0 A11 B11 C11 D11
PP_HV A6 A7 A8 B7
PP_CABLE H10
VBUS H11 J10 J11 K11
VIN_3V3 H1
VDDIO B1
LDO_3V3 G1
VOUT_3V3 H2
LDO_1V8A K1
LDO_1V8D A2
LDO_BMC E1

HV FET/SENSE
SS H7
SENSEP B10
SENSEN A10
HV_GATE1 B9
HV_GATE2 A9

UPC_TA_SS
CB309 0.47UF 10% 6.3V CERM-X5R 0201

DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX

C_CC1 L9 USBC_TA_CC1 BI 107 111
C_CC2 L10 USBC_TA_CC2 BI 107 111
RPD_G1 K9 USBC_TA_CC1 BI 107
RPD_G2 K10 USBC_TA_CC2 BI 107
C_USB_TP K6 USBC_TA_USB_TOP_P BI 110
C_USB_TN L6 USBC_TA_USB_TOP_N BI 110
C_USB_BP K7 USBC_TA_USB_BOT_P BI 110
C_USB_BN L7 USBC_TA_USB_BOT_N BI 110
C_SBU1 K8 USBC_TA_SBU1 BI 110
C_SBU2 L8 USBC_TA_SBU2 BI 110
NC L11 GROUND
NC or GND to dissipate heat

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

CB314 220PF 10% 16V CER-X7R 0201
CB313 220PF 10% 16V CER-X7R 0201

RB305 1M 5% 1/20W MF 201 UPC_TA_UART_RX 107 108 109

RB303 15K 0.1% 1/20W TF-LF 0201 NEED 0.1%

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

LB300
90-ONM-0.1A
EXCX4CE

USB2_UPC_TA_P 107 BI
USB2_UPC_TA_N 107 BI
PLACE_NEAR=UB300.L5:5mm
PLACE_NEAR=UB300.K5:5mm

PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_TA_LDO

GND A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7

GND 107

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER	051-02643
SIZE	D
REVISION	4.0.0
BRANCH	evt-0
PAGE	113 OF 200
SHEET	108 OF 131

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

QB400
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

PP20V_USBC_TB_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V

PP20V_USBC_TB_VBUS

CB401 1UF 10% 16V X5R 0402

PPDCIN_G3H
MAX 100uF TOTAL ON RAIL

UPC_TB_GATE1
UPC_TB_GATE2

PP3V3_UPC_TB_LDO
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V

PP3V3_TBT_T_SX

PP1V8_UPC_TB_LDOA

PP1V8_UPC_TB_LDOD

PP1V1_UPC_TB_LDO_BMC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V

PP1V8_SLPS2R
PP3V3_G3H_RTC_X
RB469 100K 5% 1/20W MF 201
PHV_INT_TB_G3H
PP5V_S4_T_USBC
CAP FOR PP_5V0 ON VR PAGE

CB402 1.0UF 20% 6.3V X5R 0201-1
CB400 10UF 20% 6.3V CERM-X5R 0402-1
CB404 2.2UF 20% 6.3V X5R-CERM 0201
CB405 1.0UF 20% 6.3V X5R 0201-1
CB406 0.47UF 10% 6.3V CERM-X5R 0201
CB408 10UF 20% 6.3V CERM-X5R 0402-1

PP_5V0 A11 B11 C11 D11
PP_HV A6 A7 A8 B7
PP_CABLE H10
VBUS H11 J10 J11 K11
VIN_3V3 H1
VDDIO B1
LDO_3V3 G1
VOUT_3V3 H2
LDO_1V8A K1
LDO_1V8D A2
LDO_BMC E1

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

UB400
CD3215A
BGA
CRITICAL
OMIT_TABLE

TBT_POC_RESET	E11	MRESET
TP_USBC_TB_RESET_L	F11	RESET*
UPC_TB_GPIO0	B2	GPIO0
UPC_TB_GPIO1	C2	GPIO1
TBT_T_CIO_PWR_EN	D10	GPIO2
TBT_T_USB_PWR_EN	G11	GPIO3
DP_TB_HPD	C10	GPIO4
UPC_PMU_RESET	E10	GPIO5
UPC_T_5V_EN	G10	GPIO6
UPC_TB_GPIO7	D7	GPIO7
UPC_TB_FAULT_L	H6	GPIO8
GND	F10	BUSPOWERZ
NC_UPC_TB_I2C_ADDR	F1	I2C_ADDR
UPC_TB_R_OSC	G2	R_OSC
I2C_UPC_TB_DBG_CTL_SCL	E4	DEBUG_CTL1
I2C_UPC_TB_DBG_CTL_SDA	D5	DEBUG_CTL2
I2C_TBT_T_SDA	D1	I2C_SDA1
I2C_TBT_T_SCL	D2	I2C_SCL1
I2C_TBT_TB_INT_L	C1	I2C_IRQ1*
I2C_UPC_T_SDA2	A5	I2C_SDA2
I2C_UPC_T_SCL2	B5	I2C_SCL2
UPC_I2C_INT_L	B6	I2C_IRQ2*
GND	A3	SPI_CLK
GND	B4	SPI_MOSI
GND	A4	SPI_MISO
GND	B3	SPI_SSZ
TP_UPC_TB_SWD_DATA	F4	SWD_DATA
TP_UPC_TB_SWD_CLK	G4	SWD_CLK
UPC_TA_UART_TX	F2	UART_RX
UPC_TA_UART_RX	E2	UART_TX
TBT_TB_LSTX	L4	LSX_R2P
TBT_TB_LSRX	K4	LSX_P2R
USB_UPC_TB_F_P	L5	USB_RP_P
USB_UPC_TB_F_N	K5	USB_RP_N
USBC_TB_AUXLSX1	J1	AUX_P
USBC_TB_AUXLSX2	J2	AUX_N
UPC_TB_DBG1	L2	DEBUG1
UPC_TB_DBG2	K2	DEBUG2
UPC_TB_DBG3	L3	DEBUG3
UPC_TB_DBG4	K3	DEBUG4

HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX

SS H7 UPC_TB_SS
SENSEP B10
SENSEN A10
HV_GATE1 B9
HV_GATE2 A9

CB409 0.47UF 10% 6.3V CERM-X5R 0201

C_CC1 L9 USBC_TB_CC1
C_CC2 L10 USBC_TB_CC2
RPD_G1 K9 USBC_TB_CC1
RPD_G2 K10 USBC_TB_CC2
C_USB_TP K6 USBC_TB_USB_TOP_P
C_USB_TN L6 USBC_TB_USB_TOP_N
C_USB_BP K7 USBC_TB_USB_BOT_P
C_USB_BN L7 USBC_TB_USB_BOT_N
C_SBU1 K8 USBC_TB_SBU1
C_SBU2 L8 USBC_TB_SBU2
NC L11 GROUND
NC or GND to dissipate heat

CB414 220PF 10% 16V C0G-CER-X7R 0201
CB413 220PF 10% 16V C0G-CER-X7R 0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

PULL B3200 AND B3208 UP TO ACEs LDOs FOR 1ST BRIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

GND

RB409 1M 5% 1/20W MF 201 I2C_UPC_TB_DBG_CTL_SCL (CKPLUS_WAIVE=I2C_PULLUP)
RB408 1M 5% 1/20W MF 201 I2C_UPC_TB_DBG_CTL_SDA (CKPLUS_WAIVE=I2C_PULLUP)
RB405 1M 5% 1/20W MF 201 UPC_TA_UART_TX

CRITICAL
RB403 15K 0.1% 1/20W TF-LF 0201 NEED 0.1%

TO SMC

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

LB400
90-OHM-0.1A
EXCX4CE
SYM_VER_1

USB2_UPC_TB_P
USB2_UPC_TB_N
PLACE_NEAR=UB400.L5:5mm
PLACE_NEAR=UB400.K5:5mm

GND pins: A1 D6 E5 E6 E7 F5 G5 H4 H5 G6 H6 L1 B8 D8 E8 F6 F7 F8 G6 G7

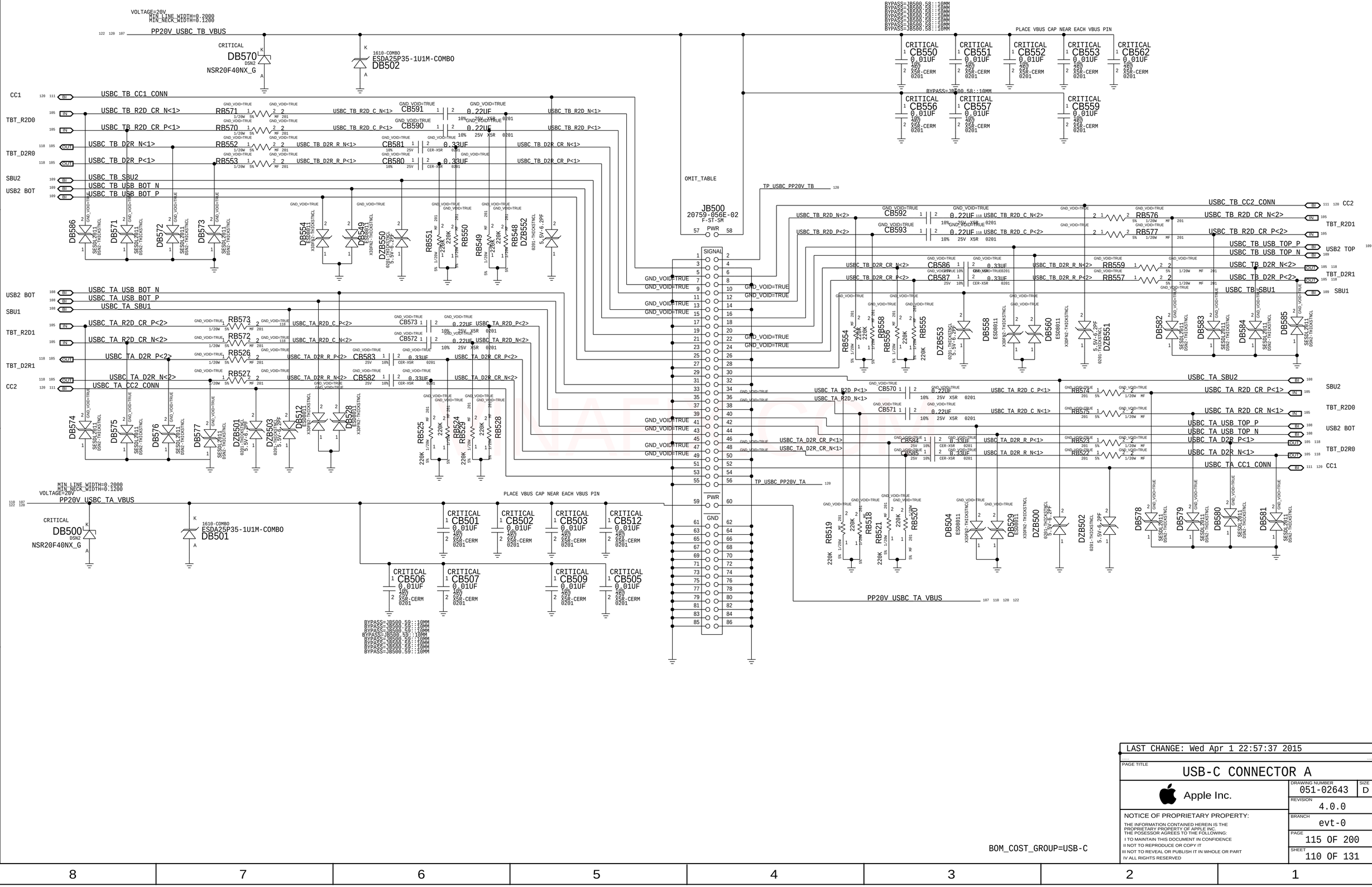
GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER: 051-02643
SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
PAGE: 114 OF 200
SHEET: 109 OF 131


VOLTAGE=20V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
PP20V_USBC_TB_VBUS
CRITICAL
DB570
DSN2
NSR20F40NX_G
1610-COMBO
ESDA25P35-1U1M-COMBO
DB502
CC1
USBC_TB_CC1_CONN
TBT_R2D0
USBC_TB_R2D_CR_N<1>
USBC_TB_R2D_CR_P<1>
TBT_D2R0
USBC_TB_D2R_N<1>
USBC_TB_D2R_P<1>
SBU2
USBC_TB_SBU2
USB2 BOT
USBC_TB_USB_BOT_N
USBC_TB_USB_BOT_P
RB571
RB570
RB552
RB553
CB591
CB590
CB581
CB580
0.22UF
0.33UF
OMIT_TABLE
JB500
20759-056E-02
F-ST-SM
PWR
SIGNAL
GND
TP_USBC_PP20V_TB
PLACE VBUS CAP NEAR EACH VBUS PIN
CB550
CB551
CB552
CB553
CB562
CB556
CB557
CB559
0.01UF
BYPASS=JB500.58::10MM
USBC_TB_CC2_CONN
USBC_TB_R2D_CR_N<2>
USBC_TB_R2D_CR_P<2>
USBC_TB_USB_TOP_P
USBC_TB_USB_TOP_N
USBC_TB_D2R_N<2>
USBC_TB_D2R_P<2>
USBC_TB_SBU1
USB2 TOP
TBT_D2R1
SBU1
CC2
RB576
RB577
RB559
RB557
CB592
CB593
CB586
CB587
USBC_TA_SBU2
USBC_TA_R2D_CR_P<1>
USBC_TA_R2D_CR_N<1>
USBC_TA_USB_TOP_P
USBC_TA_USB_TOP_N
USBC_TA_D2R_P<1>
USBC_TA_D2R_N<1>
USBC_TA_CC1_CONN
USB2 BOT
TBT_D2R0
CC1
RB574
RB575
RB523
RB522
CB570
CB571
CB584
CB585
USBC_TA_USB_BOT_N
USBC_TA_USB_BOT_P
USBC_TA_SBU1
TBT_R2D1
USBC_TA_R2D_CR_P<2>
USBC_TA_R2D_CR_N<2>
USBC_TA_D2R_P<2>
USBC_TA_D2R_N<2>
USBC_TA_CC2_CONN
RB573
RB572
RB526
RB527
CB573
CB572
CB583
CB582
RB525
RB524
RB529
RB528
DZB503
DB512
DB528
DZB501
PP20V_USBC_TA_VBUS
DB500
DB501
CB501
CB502
CB503
CB512
CB506
CB507
CB509
CB505
RB519
RB518
RB521
RB520
DB504
DB529
DZB500
DZB502
DB578
DB579
DB580
DB581
BOM_COST_GROUP=USB-C
LAST CHANGE: Wed Apr 1 22:57:37 2015
PAGE TITLE
USB-C CONNECTOR A
Apple Inc.
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051-02643
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BRANCH
evt-0
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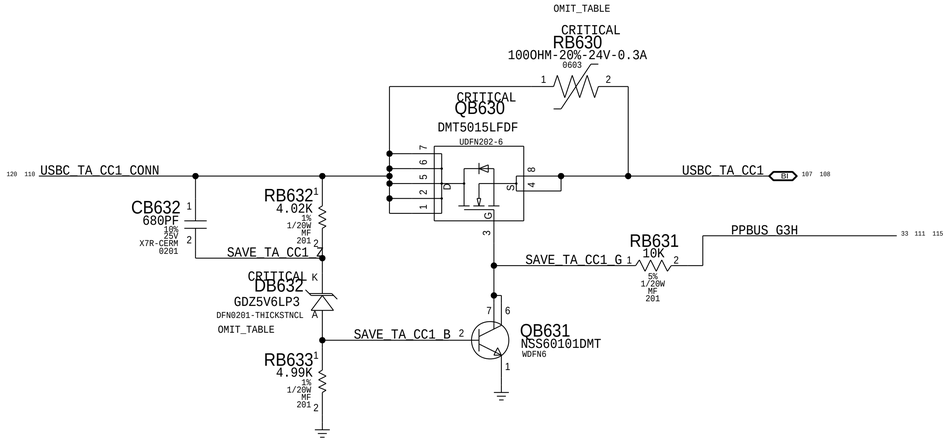
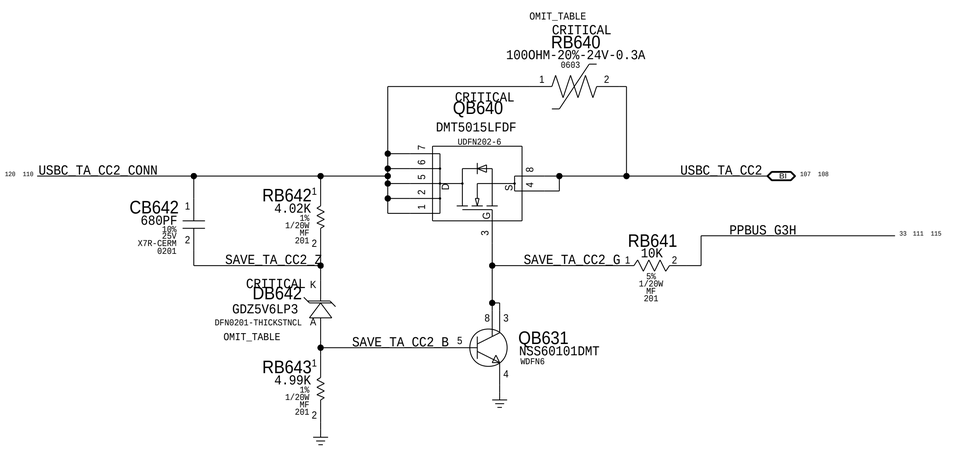
TA CC Protection





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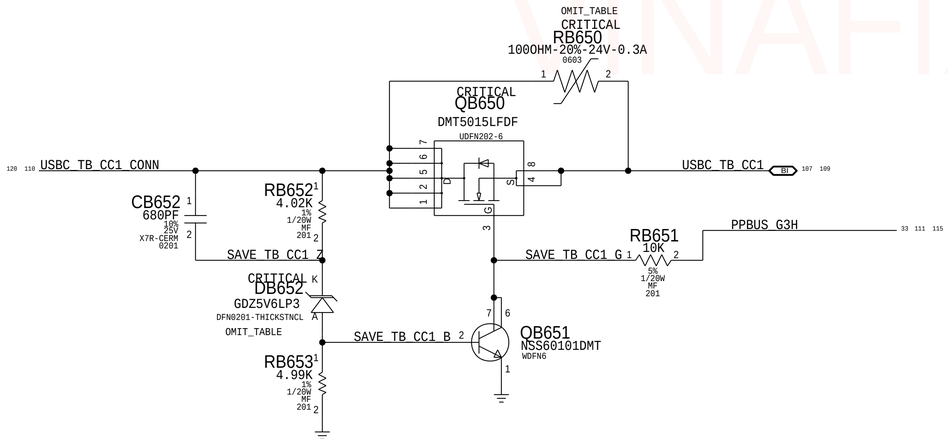

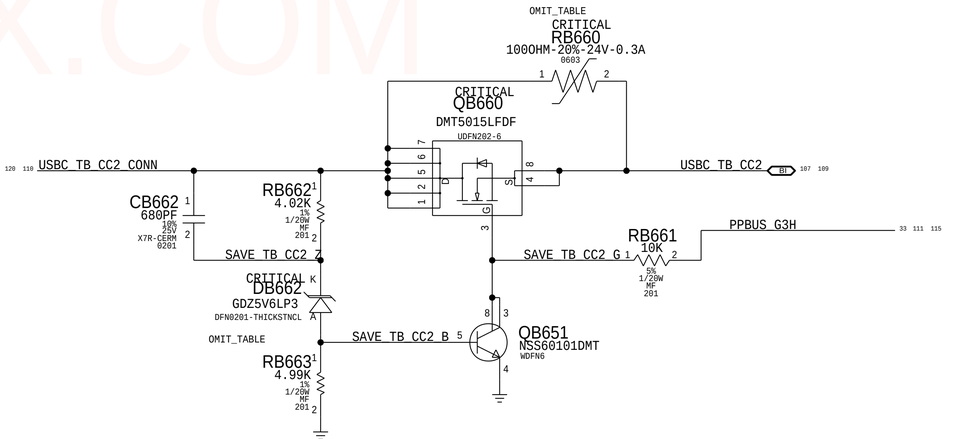

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
371S00181	4	DIODE,ZENER,5.6V,250MW,DFN0201	DB632,DB642,DB652,DB662	CRITICAL	
740S00050	4	FUSE,THRMSTR,PTC,470OHM,24V,60MA,0603	RB630,RB640,RB650,RB660	CRITICAL	

BOM_COST_GROUP=USB-C

DESIGN: X1032/MLB_P4BP
LAST CHANGE: Fri Jan 6 16:01:21 2017

PAGE TITLE
USBC T Connector Support

Apple Inc.

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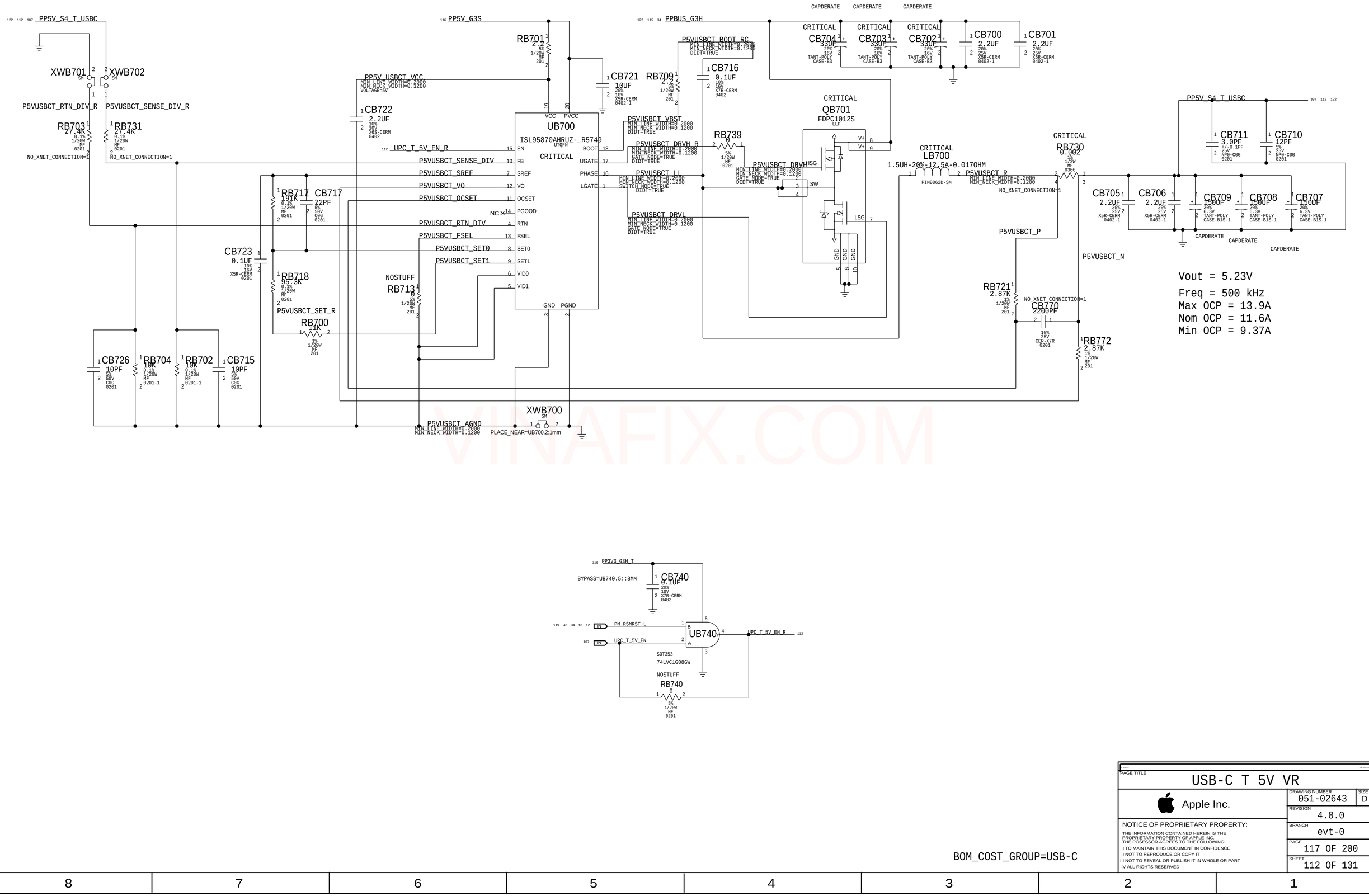

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Apple Inc.

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BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=j998_copy SYNC_DATE=02/01/2017

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Apple Inc.

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BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=j998_copy SYNC_DATE=02/01/2017

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PBUS & High Side

122 68 PPBUS_G3H
- PPBUS_G3H — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 55 119 122 74
- PPBUS_G3H — 53
- PPBUS_G3H — 53
- PPBUS_G3H — 53
- PPBUS_G3H — 53
- PPBUS_G3H — 58
- PPBUS_G3H — 53
- PPBUS_G3H — 34 112 122
- PPBUS_G3H — 65
- PPBUS_G3H — 62 63
- PPBUS_G3H — 33 111
- PPBUS_G3H — 77
- PPBUS_G3H — 55
- PPBUS_G3H — 55
- PPBUS_G3H — 81

53 PPBUS_HS_CPU
- PPBUS_HS_CPU — MIN_LINE_WIDTH=0.0000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 122 124
- PPBUS_HS_CPU — 70
- PPBUS_HS_CPU — 71
- PPBUS_HS_CPU — 72
- PPBUS_HS_CPU — 74
- PPBUS_HS_CPU — 78
- PPBUS_HS_CPU — 74
- PPBUS_HS_CPU — 69

58 PPBUS_HS_GPU
- PPBUS_HS_GPU — MIN_LINE_WIDTH=0.0000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 101 119 124
- PPBUS_HS_GPU — 98
- PPBUS_HS_GPU — 104
- PPBUS_HS_GPU — 98 101
- PPBUS_HS_GPU — 98

53 PPBUS_HS_OTH5V
- PPBUS_HS_OTH5V — MIN_LINE_WIDTH=0.0000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_OTH5V — 73

53 PPBUS_HS_3V3G3H_T
- PPBUS_HS_3V3G3H_T — MIN_LINE_WIDTH=0.0000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_3V3G3H_T — 73

53 PPBUS_HS_3V3G3HRTC_X
- PPBUS_HS_3V3G3HRTC_X — MIN_LINE_WIDTH=0.0000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_3V3G3HRTC_X — 67

CPU Rails

78 PPVCC_S0_CPU
- PPVCC_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.02V, MAKE_BASE=TRUE — 119
- PPVCC_S0_CPU — 6 8 58
- PPVCC_S0_CPU — 10

71 PPVCCSA_S0_CPU
- PPVCCSA_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.02V, MAKE_BASE=TRUE — 119
- PPVCCSA_S0_CPU — 8 58
- PPVCCSA_S0_CPU — 11

72 PPVCCGT_S0_CPU
- PPVCCGT_S0_CPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.02V, MAKE_BASE=TRUE — 119
- PPVCCGT_S0_CPU — 8 58
- PPVCCGT_S0_CPU — 11 122

122 78 PPVCCIO_S0_CPU
- PPVCCIO_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.95V, MAKE_BASE=TRUE — 119
- PPVCCIO_S0_CPU — 5 8 10

DDR4 1.2V

74 PP1V2_S3
- PP1V2_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE — 119 122 123
- PP1V2_S3 — 24 25
- PP1V2_S3 — 21
- PP1V2_S3 — 22 23 26
- PP1V2_S3 — 54
- PP1V2_S3 — 79

54 PP1V2_S3_CPUDDR
- PP1V2_S3_CPUDDR — MIN_NECK_WIDTH=0.1200, MIN_LINE_WIDTH=0.2000, MAKE_BASE=TRUE, VOLTAGE=1.2V — 120
- PP1V2_S3_CPUDDR — 8
- PP1V2_S3_CPUDDR — 10 122

79 PP1V2_S0SW
- PP1V2_S0SW — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE — 119
- PP1V2_S0SW — 8

21 PP0V6_S3_MEM_VREFCA_A
- PP0V6_S3_MEM_VREFCA_A — MAKE_BASE=TRUE, VOLTAGE=0.6V — 22 23

21 PP0V6_S3_MEM_VREFCA_B
- PP0V6_S3_MEM_VREFCA_B — MAKE_BASE=TRUE, VOLTAGE=0.6V — 24 25

DDR4 0.6V VTT

74 PP0V6_S0_DDRVTT
- PP0V6_S0_DDRVTT — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.6V, MAKE_BASE=TRUE — 119
- PP0V6_S0_DDRVTT — 122
- PP0V6_S0_DDRVTT — 122
- PP0V6_S0_DDRVTT — 26
- PP0V6_S0_DDRVTT — 26

DDR4 2.5V

74 PP2V5_S3
- PP2V5_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=2.5V, MAKE_BASE=TRUE — 119 122 123
- PP2V5_S3 — 22 23
- PP2V5_S3 — 24 25
- PP2V5_S3 — 74

PMIC Buck 8 - PCH 1.05V Prime

54 PP1V05_PRIM
- PP1V05_PRIM — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 119
- PP1V05_PRIM — 16 17 80
- PP1V05_PRIM — 17
- PP1V05_PRIM — 16
- PP1V05_PRIM — 16
- PP1V05_PRIM — 16
- PP1V05_PRIM — 17
- PP1V05_PRIM — 16 17
- PP1V05_PRIM — 17
- PP1V05_PRIM — 18
- PP1V05_PRIM — 74

PMIC Buck8 SW2

78 PP1V05_S3
- PP1V05_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 119
- PP1V05_S3 — 6 8 11 46
- PP1V05_S3 — 69
- PP1V05_S3 — 8 11
- PP1V05_S3 — 46
- PP1V05_S3 — 77

PMIC HIO SW

76 PP1V05_S0SW
- PP1V05_S0SW — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 119
- PP1V05_S0SW — 6 8 11
- PP1V05_S0SW — 18

GPU Rails

101 98 PPVCORE_S0_GPU
- PPVCORE_S0_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.1V, MAKE_BASE=TRUE — 119 124
- PPVCORE_S0_GPU — 58 96 124

98 PPVDDCI_S0_GPU
- PPVDDCI_S0_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.1V, MAKE_BASE=TRUE — 119
- PPVDDCI_S0_GPU — 58 96 124
- PPVDDCI_S0_GPU — 96

122 98 PP1V5R1V35_S0_GPU_MEM
- PP1V5R1V35_S0_GPU_MEM — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.35V, MAKE_BASE=TRUE — 96 119
- PP1V5R1V35_S0_GPU_MEM — 99 100 124
- PP1V5R1V35_S0_GPU_MEM — 58

58 PP1V5R1V35_S0_GPU_IC
- PP1V5R1V35_S0_GPU_IC — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.05V, MAKE_BASE=TRUE — 97 124
- PP1V5R1V35_S0_GPU_IC — 96

122 104 PP1V8_GPU
- PP1V8_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_GPU — 58

122 58 PP1V8_S0_GPU
- PP1V8_S0_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE — 95 103
- PP1V8_S0_GPU — 96
- PP1V8_S0_GPU — 103
- PP1V8_S0_GPU — 102
- PP1V8_S0_GPU — 102
- PP1V8_S0_GPU — 101

104 PP3V3_S0_GPU
- PP3V3_S0_GPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.3V, MAKE_BASE=TRUE — 97 103
- PP3V3_S0_GPU — 96
- PP3V3_S0_GPU — 19
- PP3V3_S0_GPU — 95
- PP3V3_S0_GPU — 102
- PP3V3_S0_GPU — 102
- PP3V3_S0_GPU — 51 103
- PP3V3_S0_GPU — 98 101
- PP3V3_S0_GPU — 102
- PP3V3_S0_GPU — 94

Digital Ground

GND — MIN_NECK_WIDTH=0.1000, MIN_LINE_WIDTH=0.2000

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Apple Inc.

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1.8V G3S

79 PP1V8_G3S

PP1V8_G3S
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_G3S — 37 119
PP1V8_G3S — 51
PP1V8_G3S — 66
PP1V8_G3S — 52 61
PP1V8_G3S — 73
PP1V8_G3S — 59 119
PP1V8_G3S — 63
PP1V8_G3S — 62
PP1V8_G3S — 64
PP1V8_G3S — 19
PP1V8_G3S — 54
PP1V8_G3S — 49
PP1V8_G3S — 64
PP1V8_G3S — 52
PP1V8_G3S — 52
PP1V8_G3S — 52
PP1V8_G3S — 52 82
PP1V8_G3S — 48

5V G3S

73 PP5V_G3S

PP5V_G3S
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
MAKE_BASE=TRUE

PP5V_G3S — 119 120
PP5V_G3S — 65
PP5V_G3S — 78 116
PP5V_G3S — 74
PP5V_G3S — 112
PP5V_G3S — 69 70 71
PP5V_G3S — 98 101
PP5V_G3S — 98
PP5V_G3S — 65
PP5V_G3S — 65
PP5V_G3S — 50
PP5V_G3S — 82
PP5V_G3S — 72
PP5V_G3S — 81
PP5V_G3S — 54 56
PP5V_G3S — 51
PP5V_G3S — 78 116
PP5V_G3S — 34
PP5V_G3S — 104
PP5V_G3S — 59
PP5V_G3S — 82
PP5V_G3S — 126

3V3 G3H "T"

73 PP3V3_G3H_T

PP3V3_G3H_T
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1500
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_T — 119
PP3V3_G3H_T — 79
PP3V3_G3H_T — 79
PP3V3_G3H_T — 79
PP3V3_G3H_T — 79
PP3V3_G3H_T — 56
PP3V3_G3H_T — 48
PP3V3_G3H_T — 79
PP3V3_G3H_T — 104
PP3V3_G3H_T — 55
PP3V3_G3H_T — 112

3V3 G3H "X"

67 PP3V3_G3H_RTC_X

PP3V3_G3H_RTC_X
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_RTC_X — 120
PP3V3_G3H_RTC_X — 79
PP3V3_G3H_RTC_X — 104
PP3V3_G3H_RTC_X — 31
PP3V3_G3H_RTC_X — 30
PP3V3_G3H_RTC_X — 126
PP3V3_G3H_RTC_X — 82
PP3V3_G3H_RTC_X — 67
PP3V3_G3H_RTC_X — 67
PP3V3_G3H_RTC_X — 77
PP3V3_G3H_RTC_X — 55
PP3V3_G3H_RTC_X — 79
PP3V3_G3H_RTC_X — 65
PP3V3_G3H_RTC_X — 76
PP3V3_G3H_RTC_X — 79
PP3V3_G3H_RTC_X — 76
PP3V3_G3H_RTC_X — 76
PP3V3_G3H_RTC_X — 29
PP3V3_G3H_RTC_X — 55
PP3V3_G3H_RTC_X — 67
PP3V3_G3H_RTC_X — 126
PP3V3_G3H_RTC_X — 131
PP3V3_G3H_RTC_X — 34
PP3V3_G3H_RTC_X — 108
PP3V3_G3H_RTC_X — 109

3V3 G3S "T"

79 PP3V3_G3S_T

PP3V3_G3S_T
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3S_T — 65
PP3V3_G3S_T — 65 120
PP3V3_G3S_T — 66
PP3V3_G3S_T — 49
PP3V3_G3S_T — 61

3V3 G3S "X"

79 PP3V3_G3S_X

PP3V3_G3S_X
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3S_X — 119
PP3V3_G3S_X — 54
PP3V3_G3S_X — 82

79 PP3V3_S0SW_TBT_X

PP3V3_S0SW_TBT_X
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0SW_TBT_X — 119
PP3V3_S0SW_TBT_X — 56

79 PP3V3_S0SW_TBT_T

PP3V3_S0SW_TBT_T
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0SW_TBT_T — 56

56 PP3V3_S0SW_TBT_X_SNS

PP3V3_S0SW_TBT_X_SNS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0SW_TBT_X_SNS — 28 29 95 122
PP3V3_S0SW_TBT_X_SNS — 14

56 PP3V3_S0SW_TBT_T_SNS

PP3V3_S0SW_TBT_T_SNS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_S0SW_TBT_T_SNS — 95 106 107 122
PP3V3_S0SW_TBT_T_SNS — 14

75 PP3V3_G3SSW_SNS

PP3V3_G3SSW_SNS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3SSW_SNS — 53
PP3V3_G3SSW_SNS — 53 54 55 56 58
PP3V3_G3SSW_SNS — 54
PP3V3_G3SSW_SNS — 53
PP3V3_G3SSW_SNS — 56

56 PP3V3_G3H_SOCPMU

PP3V3_G3H_SOCPMU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_SOCPMU — 119
PP3V3_G3H_SOCPMU — 75
PP3V3_G3H_SOCPMU — 76
PP3V3_G3H_SOCPMU — 76

54 PP3V3_G3S_WLAN

PP3V3_G3S_WLAN
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1000
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3S_WLAN — 120
PP3V3_G3S_WLAN — 36 37 122
PP3V3_G3S_WLAN — 35

122 75 PPVCCPRIMCORE_PRIM_REG

PPVCCPRIMCORE_PRIM_REG
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.05V
MAKE_BASE=TRUE

PPVCCPRIMCORE_PRIM_REG — 54

54 PP1V8_G3S_WLANBT_VDDIO

PP1V8_G3S_WLANBT_VDDIO
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
MAKE_BASE=TRUE

PP1V8_G3S_WLANBT_VDDIO — 19 35 36 37 122

55 PP3V3_G3H_DFR

PP3V3_G3H_DFR
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_DFR — 50

SSD 3V3_G3H AND PPBUS_G3H

55 PP3V3_G3H_SSD0_SNS

PP3V3_G3H_SSD0_SNS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_SSD0_SNS — 87

55 PP3V3_G3H_SSD1_SNS

PP3V3_G3H_SSD1_SNS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PP3V3_G3H_SSD1_SNS — 92

55 PPBUS_G3H_SSD0_SNS

PPBUS_G3H_SSD0_SNS
MIN_LINE_WIDTH=0.6000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.1V
MAKE_BASE=TRUE

PPBUS_G3H_SSD0_SNS — 87

55 PPBUS_G3H_SSD1_SNS

PPBUS_G3H_SSD1_SNS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
MAKE_BASE=TRUE

PPBUS_G3H_SSD1_SNS — 92

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PEG X16 CPU-GPU

118 95	IN	PEG_GPU_D2R_P<7..0>	MAKE_BASE=TRUE	=PEG_D2R_P<7..0>	OUT	5
118 95	IN	PEG_GPU_D2R_N<7..0>	MAKE_BASE=TRUE	=PEG_D2R_N<7..0>	OUT	5
118 95	OUT	PEG_GPU_R2D_C_P<7..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<7..0>	IN	5
118 95	OUT	PEG_GPU_R2D_C_N<7..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<7..0>	IN	5

GPU Throttle

H9M Side (After LS)		GPU Side	
103 GFX_SELF_THROTTLE_1V8	MAKE_BASE=TRUE	GFX_SELF_THROTTLE_1V8	39
103 GFX_THROTTLE_1V8_L	MAKE_BASE=TRUE	GFX_THROTTLE_1V8_L	39

CPU Display Aliases

NC_DDI1_ML_C_P<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI1_ML_C_P<3..0>	IN 5
NC_DDI1_ML_C_N<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI1_ML_C_N<3..0>	IN 5
NC_DDI1_AUXCH_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI1_AUXCH_C_P	IN 5
NC_DDI1_AUXCH_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI1_AUXCH_C_N	IN 5
NC_DDI2_ML_C_P<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI2_ML_C_P<3..0>	IN 5
NC_DDI2_ML_C_N<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI2_ML_C_N<3..0>	IN 5
NC_DDI2_AUXCH_C_P	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI2_AUXCH_C_P	IN 5
NC_DDI2_AUXCH_C_N	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI2_AUXCH_C_N	IN 5
NC_DDI3_ML_P<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI3_ML_P<3..0>	IN 5
NC_DDI3_ML_N<3..0>	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI3_ML_N<3..0>	IN 5
NC_DDI3_AUXCH_P	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI3_AUXCH_P	IN 5
NC_DDI3_AUXCH_N	MAKE_BASE=TRUE	NO_TEST=1	NC_DDI3_AUXCH_N	IN 5

Thunderbolt Signals Through PEG

118 29	IN	PCIE_TBT_X_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<11..8>	OUT	5
118 29	IN	PCIE_TBT_X_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<11..8>	OUT	5
118 29	OUT	PCIE_TBT_X_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<11..8>	IN	5
118 29	OUT	PCIE_TBT_X_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<11..8>	IN	5
118 107	IN	PCIE_TBT_T_D2R_P<3..0>	MAKE_BASE=TRUE	=PEG_D2R_P<15..12>	OUT	5
118 107	IN	PCIE_TBT_T_D2R_N<3..0>	MAKE_BASE=TRUE	=PEG_D2R_N<15..12>	OUT	5
118 107	OUT	PCIE_TBT_T_R2D_C_P<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_P<15..12>	IN	5
118 107	OUT	PCIE_TBT_T_R2D_C_N<3..0>	MAKE_BASE=TRUE	=PEG_R2D_C_N<15..12>	IN	5

GPU ALIAS

93	IN	GPU_RESET_L	MAKE_BASE=TRUE	GPU_RESET_L	OUT	46 95 119
121 12	IN	EG_PEG_CLK100M_N	MAKE_BASE=TRUE	EG_PEG_CLK100M_N	OUT	95
121 12	IN	EG_PEG_CLK100M_P	MAKE_BASE=TRUE	EG_PEG_CLK100M_P	OUT	95

PAGE TITLE

Signal Alias

Apple Inc.

DRAWING NUMBER 051-02643

SIZE D

REVISION 4.0.0

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ICT TESTPOINTS , High Speed NO_TEST

PEG

- PEG_GPU_D2R_N<7..0> NO_TEST=1
- PEG_GPU_D2R_P<7..0> NO_TEST=1
- PEG_GPU_R2D_C_N<7..0> NO_TEST=1
- PEG_GPU_R2D_C_P<7..0> NO_TEST=1
- PCIE_TBT_X_D2R_P<3..0> NO_TEST=1
- PCIE_TBT_X_D2R_N<3..0> NO_TEST=1
- PCIE_TBT_X_R2D_C_P<3..0> NO_TEST=1
- PCIE_TBT_X_R2D_C_N<3..0> NO_TEST=1
- PCIE_TBT_T_D2R_P<3..0> NO_TEST=1
- PCIE_TBT_T_D2R_N<3..0> NO_TEST=1
- PCIE_TBT_T_D2R_C_P<3..0> NO_TEST=1
- PCIE_TBT_T_D2R_C_N<3..0> NO_TEST=1
- PCIE_TBT_X_D2R_C_P<3..0> NO_TEST=1
- PCIE_TBT_X_D2R_C_N<3..0> NO_TEST=1
- PCIE_TBT_X_R2D_P<3..0> NO_TEST=1
- PCIE_TBT_X_R2D_N<3..0> NO_TEST=1
- PCIE_TBT_T_R2D_P<3..0> NO_TEST=1
- PCIE_TBT_T_R2D_N<3..0> NO_TEST=1
- PCIE_TBT_T_R2D_C_P<3..0> NO_TEST=1
- PCIE_TBT_T_R2D_C_N<3..0> NO_TEST=1
- PEG_GPU_D2R_C_N<7..0> NO_TEST=1
- PEG_GPU_D2R_C_P<7..0> NO_TEST=1
- PEG_GPU_R2D_N<7..0> NO_TEST=1
- PEG_GPU_R2D_P<7..0> NO_TEST=1

BAFFIN FRAME BUFFER

- FB_A1_CS_L NO_TEST=1
- FB_A0_CKE_L NO_TEST=1
- FB_A1_CKE_L NO_TEST=1
- FB_A0_WE_L NO_TEST=1
- FB_A1_WE_L NO_TEST=1
- FB_B1_CS_L NO_TEST=1
- FB_B0_CKE_L NO_TEST=1
- FB_B1_CKE_L NO_TEST=1
- FB_B0_WE_L NO_TEST=1
- FB_B0_WE_L NO_TEST=1
- FB_B0_CLK_P NO_TEST=1
- FB_B1_CLK_N NO_TEST=1
- FB_B1_CLK_P NO_TEST=1
- FB_B0_RAS_L NO_TEST=1
- FB_B1_RAS_L NO_TEST=1
- FB_B0_CAS_L NO_TEST=1
- FB_B1_CAS_L NO_TEST=1
- FB_B0_CS_L NO_TEST=1
- FB_A0_DQ<31..0> NO_TEST=1
- FB_A1_DQ<31..0> NO_TEST=1
- FB_A0_A<8..0> NO_TEST=1
- FB_A1_A<8..0> NO_TEST=1
- FB_A0_WCLK_N<1..0> NO_TEST=1
- FB_A0_WCLK_P<1..0> NO_TEST=1
- FB_A1_WCLK_N<1..0> NO_TEST=1
- FB_A1_WCLK_P<1..0> NO_TEST=1
- FB_A0_EDC<3..0> NO_TEST=1
- FB_A1_EDC<3..0> NO_TEST=1
- FB_A0_DBI_L<3..0> NO_TEST=1
- FB_A1_DBI_L<3..0> NO_TEST=1
- FB_A0_ABI_L NO_TEST=1
- FB_A1_ABI_L NO_TEST=1
- FB_A0_CLK_N NO_TEST=1
- FB_A0_CLK_P NO_TEST=1
- FB_A1_CLK_N NO_TEST=1
- FB_A1_CLK_P NO_TEST=1
- FB_A0_RAS_L NO_TEST=1
- FB_A1_RAS_L NO_TEST=1
- FB_A0_CAS_L NO_TEST=1
- FB_A1_CAS_L NO_TEST=1
- FB_A0_CS_L NO_TEST=1
- FB_B0_CLK_N NO_TEST=1
- FB_B0_DQ<31..0> NO_TEST=1
- FB_B1_DQ<31..0> NO_TEST=1
- FB_B0_A<8..0> NO_TEST=1
- FB_B1_A<8..0> NO_TEST=1
- FB_B0_WCLK_N<1..0> NO_TEST=1
- FB_B0_WCLK_P<1..0> NO_TEST=1
- FB_B1_WCLK_N<1..0> NO_TEST=1
- FB_B1_WCLK_P<1..0> NO_TEST=1
- FB_B0_EDC<3..0> NO_TEST=1
- FB_B1_EDC<3..0> NO_TEST=1
- FB_B0_DBI_L<3..0> NO_TEST=1
- FB_B1_DBI_L<3..0> NO_TEST=1
- FB_B0_ABI_L NO_TEST=1
- FB_B1_ABI_L NO_TEST=1

CPU/PCH CLK

- CPU_CLK24M_NSSC_CLK_N NO_TEST=1
- CPU_CLK24M_NSSC_CLK_P NO_TEST=1
- CPU_CLK100M_PCIBCLK_N NO_TEST=1
- CPU_CLK100M_PCIBCLK_P NO_TEST=1
- CPU_CLK100M_BCLK_N NO_TEST=1
- CPU_CLK100M_BCLK_P NO_TEST=1
- NC_ITPXDP_CLK100MN
- NC_ITPXDP_CLK100MP

MUX

- DP_INT_IG_ML_N<3..0> NO_TEST=1
- DP_INT_IG_ML_P<3..0> NO_TEST=1
- DP_INT_IG_AUX_N NO_TEST=1
- DP_INT_IG_AUX_P NO_TEST=1
- DP_INT_EG_ML_N<3..0> NO_TEST=1
- DP_INT_EG_ML_P<3..0> NO_TEST=1
- DP_INT_EG_AUX_N NO_TEST=1
- DP_INT_EG_AUX_P NO_TEST=1

USB-C X

- USBC_XB_D2R_N<2..1> NO_TEST=1
- USBC_XB_D2R_P<2..1> NO_TEST=1
- USBC_XA_D2R_P<2..1> NO_TEST=1
- USBC_XB_R2D_C_P<2..1> NO_TEST=1
- USBC_XA_D2R_N<2..1> NO_TEST=1
- USBC_XB_R2D_C_N<2..1> NO_TEST=1
- USBC_XA_R2D_C_P<2..1> NO_TEST=1
- USBC_XA_R2D_C_N<2..1> NO_TEST=1

DMI

- DMI_S2N_P<3..0> NO_TEST=1
- DMI_S2N_N<3..0> NO_TEST=1
- DMI_N2S_P<3..0> NO_TEST=1
- DMI_N2S_N<3..0> NO_TEST=1

DP - CPU/ACE

- DP_X_SNK0_ML_C_N<3..0> NO_TEST=1
- DP_X_SNK0_ML_C_P<3..0> NO_TEST=1
- DP_X_SNK0_ML_N<3..0> NO_TEST=1
- DP_X_SNK0_ML_P<3..0> NO_TEST=1
- DP_X_SNK1_ML_C_N<3..0> NO_TEST=1
- DP_X_SNK1_ML_C_P<3..0> NO_TEST=1
- DP_X_SNK1_ML_N<3..0> NO_TEST=1
- DP_X_SNK1_ML_P<3..0> NO_TEST=1
- DP_T_SNK0_ML_C_N<3..0> NO_TEST=1
- DP_T_SNK0_ML_C_P<3..0> NO_TEST=1
- DP_T_SNK0_ML_N<3..0> NO_TEST=1
- DP_T_SNK0_ML_P<3..0> NO_TEST=1
- DP_T_SNK1_ML_C_N<3..0> NO_TEST=1
- DP_T_SNK1_ML_C_P<3..0> NO_TEST=1
- DP_T_SNK1_ML_N<3..0> NO_TEST=1
- DP_T_SNK1_ML_P<3..0> NO_TEST=1
- DP_X_SNK0_AUXCH_C_P NO_TEST=1
- DP_X_SNK0_AUXCH_C_N NO_TEST=1
- DP_T_SNK0_AUXCH_C_P NO_TEST=1
- DP_T_SNK0_AUXCH_C_N NO_TEST=1
- DP_X_SNK0_AUXCH_P NO_TEST=1
- DP_X_SNK0_AUXCH_N NO_TEST=1
- DP_T_SNK0_AUXCH_P
- DP_T_SNK0_AUXCH_N
- DP_X_SNK1_AUXCH_C_P NO_TEST=1
- DP_X_SNK1_AUXCH_C_N NO_TEST=1
- DP_T_SNK1_AUXCH_C_P NO_TEST=1
- DP_T_SNK1_AUXCH_C_N NO_TEST=1
- DP_X_SNK1_AUXCH_P NO_TEST=1
- DP_X_SNK1_AUXCH_N NO_TEST=1
- DP_T_SNK1_AUXCH_P
- DP_T_SNK1_AUXCH_N

CPU/EDP

H9M ESPI

- ESPI_IO<0> NO_TEST=1
- ESPI_IO<1> NO_TEST=1
- ESPI_IO<2> NO_TEST=1
- ESPI_IO<3> NO_TEST=1
- ESPI_IO_R<0> NO_TEST=1
- ESPI_IO_R<1> NO_TEST=1
- ESPI_IO_R<3> NO_TEST=1
- ESPI_IO_R<3> NO_TEST=1

- TBT_X_XTAL25M_OUT NO_TEST=1
- TBT_X_XTAL25M_IN NO_TEST=1
- TBT_T_XTAL25M_OUT NO_TEST=1
- TBT_T_XTAL25M_IN NO_TEST=1
- GPU_CLK_IN NO_TEST=1

MEM

- MEM_A_CLK_P<1..0> NO_TEST=1
- MEM_A_CLK_N<1..0> NO_TEST=1
- MEM_A_DQ<63..0> NO_TEST=1
- MEM_B_DQ<63..0> NO_TEST=1
- MEM_A_DQS_P<7..0> NO_TEST=1
- MEM_A_DQS_N<7..0> NO_TEST=1
- MEM_B_DQS_P<7..0> NO_TEST=1
- MEM_B_DQS_N<7..0> NO_TEST=1

- MEM_B_CLK_P<1..0> NO_TEST=1
- MEM_B_CLK_N<1..0> NO_TEST=1

WIFI

- 50_0_ANT NO_TEST=1
- 50_1_ANT NO_TEST=1
- 50_2_ANT NO_TEST=1
- 50_0_COM NO_TEST=1
- 50_1_COM NO_TEST=1
- 50_2_COM NO_TEST=1
- 50_A_0_DIPLEXER NO_TEST=1
- 50_A_0_MATCH NO_TEST=1
- 50_G_0_DIPLEXER NO_TEST=1
- 50_G_0_MATCH NO_TEST=1
- 50_A_1_DIPLEXER NO_TEST=1
- 50_A_1_MATCH NO_TEST=1
- 50_G_1_DIPLEXER NO_TEST=1
- 50_G_1_MATCH NO_TEST=1
- 50_A_2_DIPLEXER NO_TEST=1
- 50_A_2_MATCH NO_TEST=1
- 50_G_2_DIPLEXER NO_TEST=1
- 50_G_2_MATCH NO_TEST=1

USB-C T

- USBC_TA_D2R_P<2..1> NO_TEST=1
- USBC_TA_D2R_N<2..1> NO_TEST=1
- USBC_TA_R2D_C_P<2..1> NO_TEST=1
- USBC_TA_R2D_C_N<2..1> NO_TEST=1

- USBC_TB_D2R_P<2..1> NO_TEST=1
- USBC_TB_D2R_N<2..1> NO_TEST=1
- USBC_TB_R2D_C_P<2..1> NO_TEST=1
- USBC_TB_R2D_C_N<2..1> NO_TEST=1

H9M SSD NAND

- PCIE_SSD0_R2D_P<3..0> NO_TEST=1
- PCIE_SSD0_R2D_N<3..0> NO_TEST=1
- PCIE_SSD0_D2R_P<3..0> NO_TEST=1
- PCIE_SSD0_D2R_N<3..0> NO_TEST=1
- PCIE_SSD0_R2D_C_P<3..0> NO_TEST=1
- PCIE_SSD0_R2D_C_N<3..0> NO_TEST=1
- PCIE_SSD0_D2R_C_P<3..0> NO_TEST=1
- PCIE_SSD0_D2R_C_N<3..0> NO_TEST=1

- PCIE_SSD1_R2D_P<3..0> NO_TEST=1
- PCIE_SSD1_R2D_N<3..0> NO_TEST=1
- PCIE_SSD1_D2R_P<3..0> NO_TEST=1
- PCIE_SSD1_D2R_N<3..0> NO_TEST=1
- PCIE_SSD1_R2D_C_P<3..0> NO_TEST=1
- PCIE_SSD1_R2D_C_N<3..0> NO_TEST=1
- PCIE_SSD1_D2R_C_P<3..0> NO_TEST=1
- PCIE_SSD1_D2R_C_N<3..0> NO_TEST=1

XTAL

- TBT_X_XTAL25M_OUT NO_TEST=1
- PCH_CLK24M_XTALOUT NO_TEST=1
- PMU_XTAL1 NO_TEST=1
- PMU_XTAL2 NO_TEST=1

PCH/AR

- PCH_PCIE_WLAN_D2R_N NO_TEST=1
- PCH_PCIE_WLAN_D2R_P NO_TEST=1
- PCH_PCIE_WLAN_R2D_C_N NO_TEST=1
- PCH_PCIE_WLAN_R2D_C_P NO_TEST=1
- PCH_PCIE_WLAN_D2R_C_P NO_TEST=1
- PCH_PCIE_WLAN_D2R_C_N NO_TEST=1
- PCH_PCIE_WLAN_R2D_P NO_TEST=1
- PCH_PCIE_WLAN_R2D_N NO_TEST=1

PCH/SOC

- PCIE_SOC_R2D_P<3..0> NO_TEST=1
- PCIE_SOC_R2D_N<3..0> NO_TEST=1
- PCIE_SOC_D2R_P<3..0> NO_TEST=1
- PCIE_SOC_D2R_N<3..0> NO_TEST=1
- PCIE_SOC_R2D_C_P<3..0> NO_TEST=1
- PCIE_SOC_R2D_C_N<3..0> NO_TEST=1
- PCIE_SOC_D2R_C_P<3..0> NO_TEST=1
- PCIE_SOC_D2R_C_N<3..0> NO_TEST=1

PAGE TITLE: High speed No Testpoints

Apple Inc.

DRAWING NUMBER 051-02643 | SIZE D

REVISION 4.0.0

BRANCH evt-0

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DFU AND FCT TESTPOINTS placed on top side of MLB, oppsite from CPU.

DFU TEST POINTS <RDAR://31619312>

Possibly useful panda signals

TPC4H8	A	1 TP-P5	SOC_DEBUGPRT_RX	40 126
TPC4H9	A	1 TP-P5	SOC_DEBUGPRT_TX	40 126
TPC402	A	TP-P5	DEBUG_JTAG_SOC_TDO	39 126
TPC403	A	TP-P5	DEBUG_JTAG_SOC_TDI	39 126
TPC404	A	TP-P5	PP1V8_SLPS2R	80
TPC405	A	TP-P5	SOC_SOCHOT_L	38 77 126
TPC406	A	TP-P5	I2C_PWR_SDA	39 51
TPC407	A	TP-P5	I2C_UPC_SCL	39 51
TPC4E9	A	TP-P5	I2C_UPC_SDA	39 51
TPC4Z5	A	TP-P5	I2C_PWR_SCL	39 51

PSU Power input

TPC441	A	TP-P5	PPBUS_HS_GPU	101 115 124
TPC442	A	TP-P5	PP2V5_S3	115 122 123
TPC443	A	TP-P5	PP0V6_S0_DDRVTT	115 119
TPC444	A	TP-P5	PP3V3_S5	80
TPC4Z6	A	TP-P5	PPVBAT_G3H_CHGR_REG	68
TPC4Z7	A	TP-P5	PPDCIN_G3H_CHGR	68 122
TPC448	A	TP-P5		
TPC449	A	TP-P5		
TPC450	A	TP-P5		

DFU NON-CUSTOMER-FACING USB PORTS

PLACE IN ACCESSIBLE BOARD AREA

SWDL

TPC408	A	TP-P5	USB3_TEST_D2R_N	OUT 14
TPC409	A	TP-P5	USB3_TEST_D2R_P	OUT 14
TPC410	A	TP-P5	USB3_TEST_R2D_N	IN 14
TPC411	A	TP-P5	USB3_TEST_R2D_P	IN 14
TPC412	A	TP-P5		
TPC413	A	TP-P5		
TPC414	A	TP-P5		
TPC415	A	TP-P5		
TPC416	A	TP-P5	USB2_UPC_TA_N	BI 14 107
TPC417	A	TP-P5	USB2_UPC_TA_P	BI 14 107
TPC418	A	TP-P5		

DZC400, DZC401, DZC402, DZC403: 5.5V-0.28PF, 0201-THICKSTNCL

DZC408, DZC409: 5.5V-0.28PF, 0201-THICKSTNCL

NON-CUSTOMER-FACING USB PORTS FOR ETHERNET DONGLE(Bristol OS Testing)

PLACE IN ACCESSIBLE BOARD AREA

Ethenet

TPC422	A	TP-P5	USB3_TEST2_D2R_N	OUT 14
TPC423	A	TP-P5	USB3_TEST2_D2R_P	OUT 14
TPC424	A	TP-P5	USB3_TEST2_R2D_N	IN 14
TPC425	A	TP-P5	USB3_TEST2_R2D_P	IN 14
TPC426	A	TP-P5		
TPC427	A	TP-P5		
TPC428	A	TP-P5		
TPC429	A	TP-P5		
TPC419	A	TP-P5	USB2_UPC_TB_N	BI 14 107
TPC420	A	TP-P5	USB2_UPC_TB_P	BI 14 107
TPC421	A	TP-P5		
TPC430	A	TP-P5	PP5V_G3S	116 119 120

DZC410, DZC411, DZC412, DZC413: 5.5V-0.28PF, 0201-THICKSTNCL

DZC406, DZC407: 5.5V-0.28PF, 0201-THICKSTNCL

Battery

TPC431	A	1 TP-P5	SYS_DETECT_L	67
TPC432	A	1 TP-P5	SMBUS_3V3_BATT_SCL	67
TPC433	A	1 TP-P5	SMBUS_3V3_BATT_SDA	67
TPC434	A	1 TP-P5	TP_BMON_IOUT	67
TPC435	A	1 TP-P5	PPVBAT_G3H_CONN	67 68
TPC436	A	1 TP-P5	PPVBAT_G3H_CONN	67 68 119
TPC437	A	1 TP-P5	PPVBAT_G3H_CONN	67 68 119
TPC4D5	A	1 TP-P5	PPVBAT_G3H_CONN	67 68 119
TPC4D6	A	1 TP-P5	PPVBAT_G3H_CONN	67 68 119
TPC4D7	A	1 TP-P5	PPVBAT_G3H_CONN	67 68 119
TPC4I7	A	1 TP-P5	PPVBAT_G3H_CONN	67 68 119
TPC4Z8	A	TP-P5	SYS_DETECT	67
TPC4D8	A	1 TP-P5		
TPC4D9	A	1 TP-P5		
TPC4E0	A	1 TP-P5		
TPC4E1	A	1 TP-P5		
TPC4E2	A	1 TP-P5		
TPC440	A	1 TP-P5		
TPC4I6	A	1 TP-P5		

AUDIO_JACK

	120 64	IN	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE
	120 64	IN	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE
	120 64	IN	AUD_CONN_RING2	FUNC_TEST=TRUE
	120 64	IN	AUD_CONN_SLEEVE	FUNC_TEST=TRUE
	120 64	IN	AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE
	120 64	IN	AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE
	120 64	IN	AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE
	120 64	IN	AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE
	120 64	IN	AUD_CONN_RING2_XW	FUNC_TEST=TRUE
			GND X2	
TPC4Z9	A	TP-P5	GND_AUDIO_CODEC	61 122

FAN

TPC4N0	A	1 TP-P5	SMC_FAN_0_PWM	39 59
TPC4N1	A	1 TP-P5	SMC_FAN_0_TACH	39 59
TPC4N2	A	1 TP-P5	SMC_FAN_1_PWM	39 59
TPC4N3	A	1 TP-P5	SMC_FAN_1_TACH	39 59
TPC4N4	A	1 TP-P5	PP1V8_G3S	59 116 119
TPC4N5	A	1 TP-P5	PP1V8_G3S	59 116 119
TPC4N6	A	1 TP-P5		
TPC4N7	A	1 TP-P5		

DEBUG MOJO

TPC451	A	1 TP-P5	PCH_UART_DEBUG_R2D	15 29 126
TPC452	A	1 TP-P5	PCH_UART_DEBUG_D2R	15 29 126
TPC4F1	A	1 TP-P5	SMC_DEBUGPRT_TX	39 47 126
TPC4F2	A	1 TP-P5	SMC_DEBUGPRT_RX	39 47 126
TPC453	A	1 TP-P5		

Soc Access w/o Potassium

TPC454	A	1 TP-P5	SOC_USB_VBUS	29 38 126
TPC455	A	1 TP-P5	USB_SOC_TYPEC_P	29 126
TPC456	A	1 TP-P5	USB_SOC_TYPEC_N	29 126
TPC457	A	1 TP-P5	PMU_ACTIVE_READY	30 38 77 131
TPC458	A	1 TP-P5	SOC_FORCE_DFU	29 38 77 131
TPC459	A	1 TP-P5	SOC_DFU_STATUS	29 38 131
TPC460	A	1 TP-P5	UPC_XB_DBG3	29 31
TPC461	A	1 TP-P5	UPC_XB_DBG4	29 31
TPC462	A	1 TP-P5	SOC_DOCK_CONNECT	30 31 39
TPC464	A	1 TP-P5		

Power Sequence,status,charging

TPC466	A	TP-P5	PP3V3_G3H_SOCPMU	116 119
TPC468	A	TP-P5	PPBUS_G3H	55 115
TPC469	A	TP-P5	PP1V2_S3	115 122 123
TPC470	A	TP-P5	PPVCC_S0_CPU	115
TPC471	A	TP-P5	PP5V_G3S	120
TPC472	A	TP-P5	PP1V5R1V35_S0_GPU_MEM	96 115
TPC473	A	TP-P5	PPVCORE_S0_GPU	115 124
TPC4L6	A	TP-P5	CPU_PWRGD	6 13 121
TPC474	A	TP-P5	PMU_ONOFF_R_L	48
TPC475	A	TP-P5	PM_SLP_S3_L	12 14 27 105 131
TPC476	A	TP-P5	PM_SLP_S4_L	12
TPC477	A	TP-P5	PM_SLP_S5_L	12
TPC479	A	TP-P5	PP0V6_S0_DDRVTT	115 119
TPC481	A	TP-P5	PP1V05_S3	115
TPC482	A	TP-P5	PM_SYSRST_L	12 18 46 121
TPC483	A	TP-P5	PM_PCH_SYS_PWROK	12 46
TPC484	A	TP-P5	PM_PCH_PWROK	12 35 46 121
TPC485	A	TP-P5	PLT_RST_L	12 20 46
TPC486	A	TP-P5	PM_RSMRST_L	12 18 34 46 112
TPC487	A	TP-P5	PM_SLP_S0_L	12 39 77 121
TPC488	A	TP-P5	SMC_FIXTURE_MODE_L	39 47
TPC489	A	TP-P5	PP1V8_G3S	37 116
TPC490	A	TP-P5	PP5V_G3S	116 119 120
TPC491	A	TP-P5	PP3V3_G3H_T	116
TPC492	A	TP-P5	PP3V3_G3H_SSD0_SNS	116
TPC493	A	TP-P5	PP3V3_S0SW_TBT_X	116
TPC495	A	TP-P5	PP3V3_G3H_SOCPMU	116 119
TPC4B4	A	TP-P5	PPVDDCPU_AWAKE	80
TPC4B6	A	1 TP-P5	PVDDQ_EN_R	74
TPC4B7	A	1 TP-P5	PVCCIO_EN	77 78
TPC4B8	A	1 TP-P5	PP0V9_SLPDDR	80
TPC4B9	A	1 TP-P5	PP1V1_SLPDDR	80
TPC4C0	A	1 TP-P5	PP1V1_SLPS2R	80
TPC4C1	A	1 TP-P5	PP1V8_AWAKE	80
TPC4J1	A	1 TP-P5	SMC_SYSRST_L	39 46 121
TPC4C4	A	1 TP-P5	PP1V8_SLPS2R_PMUVDDGPIO	75
TPC4C5	A	1 TP-P5	P1V1_SLPDDR_SOCFET_EN	76 77 131
TPC4C6	A	1 TP-P5	PMU_CLK32K_WLANBT	36 77
TPC4C7	A	1 TP-P5	SOC_WDOG	39 77
TPC4C8	A	1 TP-P5	PMU_CLK32K_SOC	39 77
TPC4C9	A	1 TP-P5	PMU_SYS_ALIVE	38 39 77 87 92 93
TPC496	A	TP-P5		

BOM_COST_GROUP=DEBUG

Power Sequence,status,charging

TPC4D0	A	1 TP-P5	P5VG3S_EN	73 77
TPC4D1	A	1 TP-P5	PP0V8_SLPS2R	80
TPC4D2	A	1 TP-P5	PPVDDCPUSRAM_AWAKE	80
TPC4D3	A	1 TP-P5	P5VG3S_PGOOD	73 77
TPC4D4	A	1 TP-P5	CPUVR_PGOOD	77 80
TPC4L7	A	TP-P5	PPVCCGT_S0_CPU	115
TPC4F3	A	TP-P5	PPVCCSA_S0_CPU	115
TPC4L0	A	TP-P5	PPVCCIO_S0_CPU	115
TPC4F4	A	TP-P5	PP1V05_S0SW	115
TPC4F5	A	TP-P5	PP1V2_S0SW	115
TPC4F6	A	TP-P5	PP1V05_PRIM	115
TPC4F7	A	TP-P5	PP1V8_S5	80
TPC4F8	A	TP-P5	PP3V0_G3H_RTC	80
TPC4F9	A	TP-P5	ALL_SYS_PWRGD	46 77
TPC4G0	A	TP-P5	PCH_RTC_RESET_L	12 77
TPC4G1	A	TP-P5	PM_THRMTRIP_L	6 46
TPC4G2	A	TP-P5	PM_PWRBTN_L	18 80
TPC4G3	A	TP-P5	CPU_PROCHOT_R_L	6
TPC4G4	A	TP-P5	PPVDDCI_S0_GPU	115
TPC4G5	A	TP-P5	DISP_GCON_RESET_L	93
TPC4G6	A	TP-P5	GPU_RESET_L	46 95 117
TPC4G7	A	TP-P5	PM_MEMVTT_EN	5 74
TPC4G8	A	TP-P5	ESPI_RESET_L	12 20 39
TPC4G9	A	TP-P5	GFX_THROTTLE_L	103
TPC4H0	A	TP-P5	PMU_COLD_RESET_L	39 64 77 121
TPC4H1	A	TP-P5	PP0V82_SLPDDR	80
TPC4H2	A	TP-P5	CHGR_EN_MVR	67 68
TPC4H3	A	TP-P5	PMU_PVDDMAIN_EN	73 77
TPC4H4	A	TP-P5	UPC_PMU_RESET	39 67 77 107
TPC4H5	A	TP-P5	P3V3G3S_EN	77 79
TPC4H6	A	TP-P5	PP3V3_G3S_X	116
TPC4H7	A	TP-P5	P1V8G3S_EN	77 79 131
TPC4L1	A	TP-P5	SSD_PMU_RESET_L	38 47 87 92
TPC4L2	A	TP-P5	PP2V5_NAND_SSD0	83 84 85 86 87 124
TPC4I0	A	TP-P5	PP2V5_NAND_SSD1	88 89 90 91 92 124
TPC4I1	A	TP-P5	PP0V9_SSD0	83 84 85 86 87 124
TPC4I2	A	TP-P5	PP0V9_SSD1	88 89 90 91 92 124
TPC4I3	A	TP-P5	PP1V8_SSD1	88 89 90 91 92 124
TPC4I4	A	TP-P5	PP1V8_SSD0	83 84 85 86 87 124
TPC4I5	A	TP-P5	PP1V2_AWAKE	80

Soc Access with Potassium

TPC499	A	1 TP-P5	USBC_XB_SBU1	31 32
TPC4A0	A	1 TP-P5	USBC_XB_SBU2	31 32
TPC4A1	A	1 TP-P5	USBC_XA_CC1_CONN	32 33
TPC4A2	A	1 TP-P5	PP20V_USBC_XA_VBUS	29 32 120 122
TPC4A3	A	1 TP-P5		

Left Side - Top Layer

PPDCIN_G3H	119 68 55 53 29 122	1 TP-P5	A	TPC4AB
PPDCIN_G3H	119 68 55 53 29 122	1 TP-P5	A	TPC4AA
PPDCIN_G3H	119 68 55 53 29 122	1 TP-P5	A	TPC4A5
PPDCIN_G3H	119 68 55 53 29 122	1 TP-P5	A	TPC4A6
PPDCIN_G3H	119 68 55 53 29 122	1 TP-P5	A	TPC4A7
PPDCIN_G3H	119 68 55 53 29 122	1 TP-P5	A	TPC4A8
PPDCIN_G3H	119 68 55 53 29 122	1 TP-P5	A	TPC4E5
PPDCIN_G3H	119 68 55 53 29 122	1 TP-P5	A	TPC4E6
		1 TP-P5	A	TPC4A9
		1 TP-P5	A	TPC4B0
		1 TP-P5	A	TPC4B1
		1 TP-P5	A	TPC4B2
		1 TP-P5	A	TPC4B3
		1 TP-P5	A	TPC4E7
		1 TP-P5	A	TPC4E8

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FCT TEST POINTS (TOP SIDE OF MLB)

DFR/MESA (FCT)

TPC500	A	1	TP-P5	
TPC501	A	1	TP-P5	
TPC502	A	1	TP-P5	MIPI_DFR_CLK_CONN_FILT_P
TPC503	A	1	TP-P5	DFR_DISP_VSYNC
TPC505	A	1	TP-P5	DFR_DISP_TE
TPC504	A	1	TP-P5	MIPI_DFR_CLK_CONN_FILT_N
TPC506	A	1	TP-P5	
TPC507	A	1	TP-P5	MIPI_DFR_DATA_CONN_FILT_P
TPC524	A	1	TP-P5	MIPI_DFR_DATA_CONN_FILT_N
TPC510	A	1	TP-P5	DFR_DISP_RESET_L
TPC516	A	1	TP-P5	PP3V3_G3HSW_DFR
TPC508	A	1	TP-P5	DFR_DISP_INT
TPC518	A	1	TP-P5	PP3V3_G3HSW_DFR
TPC511	A	1	TP-P5	
TPC512	A	1	TP-P5	
TPC521	A	1	TP-P5	TP_DFR_TOUCH_PANEL_DETECT
TPC522	A	1	TP-P5	DFR_LID_OPEN_L
TPC515	A	1	TP-P5	
TPC520	A	1	TP-P5	
TPC527	A	1	TP-P5	SPI_DFR_MISO_R
TPC528	A	1	TP-P5	SPI_DFR_CS_L
TPC533	A	1	TP-P5	DFR_TOUCH_INT_L
TPC535	A	1	TP-P5	DFR_TOUCH_CLK32K_RESET_L
TPC534	A	1	TP-P5	I2C_DFR_SCL_R
TPC536	A	1	TP-P5	I2C_DFR_SDA_R
TPC538	A	1	TP-P5	DFR_TOUCH_RESET_L
TPC530	A	1	TP-P5	SPI_DFR_MOSI
TPC525	A	1	TP-P5	
TPC526	A	1	TP-P5	
TPC529	A	1	TP-P5	SPI_DFR_CLK
TPC539	A	1	TP-P5	TP_DFR_TOUCH_ROM_WC
TPC540	A	1	TP-P5	PP1V8_SLPS2RSW_DFR
TPC542	A	1	TP-P5	PP5V_G3S_DFR_FILT
TPC541	A	1	TP-P5	PP1V8_SLPS2RSW_DFR
TPC544	A	1	TP-P5	SPI_MESA_MISO_CONN
TPC543	A	1	TP-P5	PP1V8_MESA_CONN
TPC550	A	1	TP-P5	SPI_MESA_CLK_CONN
TPC531	A	1	TP-P5	
TPC532	A	1	TP-P5	
TPC546	A	1	TP-P5	MESA_INT_CONN
TPC547	A	1	TP-P5	SPI_MESA_MOSI_CONN
TPC548	A	1	TP-P5	MESA_BOOST_EN_CONN
TPC552	A	1	TP-P5	PP16V0_MESA_CONN
TPC537	A	1	TP-P5	
TPC554	A	1	TP-P5	PP3V0_MESA_CONN
TPC555	A	1	TP-P5	PP3V0_MESA_CONN
TPC545	A	1	TP-P5	
TPC553	A	1	TP-P5	

TBT/DP

TPC5L7	A	1	TP-P5	TBT_X_HDMI_DDC_DATA
TPC5L8	A	1	TP-P5	TBT_X_HDMI_DDC_CLK
TPC5L9	A	1	TP-P5	TBT_T_HDMI_DDC_DATA
TPC5N0	A	1	TP-P5	TBT_T_HDMI_DDC_CLK

FAN , Keyboard,Trackpad Test Points

TPC556	A	1	TP-P5	GND_FAN
TPC557	A	1	TP-P5	GND_FAN
TPC558	A	1	TP-P5	PP5V_G3S_FAN_CONN
TPC559	A	1	TP-P5	PP5V_G3S_FAN_CONN
TPC560	A	1	TP-P5	FAN_LT_TACH
TPC561	A	1	TP-P5	FAN_RT_TACH
TPC562	A	1	TP-P5	FAN_LT_PWM
TPC563	A	1	TP-P5	FAN_RT_PWM
TPC564	A	1	TP-P5	
TPC565	A	1	TP-P5	
TPC5Z1	A	1	TP-P5	GND_FAN
TPC5Z2	A	1	TP-P5	GND_FAN
TPC5Z9	A	1	TP-P5	I2C_TPAD3V3_SCL
TPC5Y0	A	1	TP-P5	TPAD_KBD_WAKE_L
TPC566	A	1	TP-P5	I2C_TPAD3V3_SDA
TPC567	A	1	TP-P5	TPAD3V3_ACTUATOR_DISABLE_L
TPC568	A	1	TP-P5	I2C_KBD_SDA
TPC569	A	1	TP-P5	TPAD3V3_SPI_INT_L
TPC5Z8	A	1	TP-P5	IPD_LID_OPEN
TPC5Z3	A	1	TP-P5	PP5V_G3S
TPC5Z4	A	1	TP-P5	PP5V_G3S
TPC5Z7	A	1	TP-P5	PMU_RSLOC_RST_R_L
TPC5Z5	A	1	TP-P5	PP3V3_G3H_RTC_X
TPC571	A	1	TP-P5	
TPC588	A	1	TP-P5	ACT_GND
TPC586	A	1	TP-P5	ACT_GND
TPC579	A	1	TP-P5	KBD_BLC_GSSOUT
TPC578	A	1	TP-P5	TPAD3V3_SPI_EN
TPC585	A	1	TP-P5	PP3V3_G3S_T
TPC584	A	1	TP-P5	PP3V3_G3S_T
TPC583	A	1	TP-P5	KBD_BLC_GSLAT
TPC582	A	1	TP-P5	PP5V_G3S_TPAD_CONN
TPC581	A	1	TP-P5	KBD_BLC_GSSCK
TPC580	A	1	TP-P5	SPI_TPAD3V3_CLK
TPC591	A	1	TP-P5	PPVIN_G3H_TPAD_FUSE
TPC590	A	1	TP-P5	PPVIN_G3H_TPAD_FUSE
TPC589	A	1	TP-P5	PPVIN_G3H_TPAD_FUSE
TPC577	A	1	TP-P5	KBD_BLC_GSSIN
TPC576	A	1	TP-P5	SPI_TPAD3V3_MISO
TPC575	A	1	TP-P5	KBD_BLC_XBLANK
TPC574	A	1	TP-P5	SPI_TPAD3V3_CS_L
TPC572	A	1	TP-P5	SPI_TPAD3V3_MOSI
TPC573	A	1	TP-P5	I2C_KBD_SCL
TPC587	A	1	TP-P5	
TPC5M0	A	1	TP-P5	KBD_INT_L

WIRELESS

TPC5H9	A	1	TP-P5	PP3V3_G3S_WLAN
TPC5I0	A	1	TP-P5	PP1V8_G3S_WLANBT_VDDIO
TPC5L0	A	1	TP-P5	PPVIN_RFLDO_WLANBT
TPC5L1	A	1	TP-P5	PP1V2_WLANBT
TPC5L2	A	1	TP-P5	PP1V5_WLANBT

HALL EFFECT

TPC5I1	A	1	TP-P5	LID_OPEN_LEFT
TPC5I2	A	1	TP-P5	LID_OPEN_RIGHT

MEMORY

TPC5I3	A	1	TP-P5	PVDDQ_PGOOD
TPC5I7	A	1	TP-P5	PP1V2_S3_CPUDDR

AUDIO

TPC592	A	1	TP-P5	AUD_DMIC0_CLK_CONN
TPC593	A	1	TP-P5	AUD_DMIC0_DATA_CONN
TPC594	A	1	TP-P5	PP1V8_DMIC
TPC595	A	1	TP-P5	AUD_DMIC1_CLK_CONN
TPC596	A	1	TP-P5	AUD_DMIC1_DATA_CONN
TPC597	A	1	TP-P5	
TPC5A1	A	1	TP-P5	SPKRCONN_LW_OUTN
TPC5B1	A	1	TP-P5	SPKRCONN_LW_OUTN
TPC5B4	A	1	TP-P5	SPKRCONN_LW_OUTN
TPC5A0	A	1	TP-P5	SPKRCONN_LW_OUTP
TPC5G0	A	1	TP-P5	SPKRCONN_LW_OUTP
TPC5G1	A	1	TP-P5	SPKRCONN_LW_OUTP
TPC598	A	1	TP-P5	SPKRCONN_LT_OUTN
TPC5G2	A	1	TP-P5	SPKRCONN_LT_OUTN
TPC5M3	A	1	TP-P5	SPKRCONN_LT_OUTN
TPC599	A	1	TP-P5	SPKRCONN_LT_OUTP
TPC5M4	A	1	TP-P5	SPKRCONN_LT_OUTP
TPC5M5	A	1	TP-P5	SPKRCONN_LT_OUTP
TPC5A6	A	1	TP-P5	SPKRCONN_RW_OUTP
TPC5G6	A	1	TP-P5	SPKRCONN_RW_OUTP
TPC5M7	A	1	TP-P5	SPKRCONN_RW_OUTP
TPC5Y9	A	1	TP-P5	SPKRCONN_RW_OUTN
TPC5G8	A	1	TP-P5	SPKRCONN_RW_OUTN
TPC5M9	A	1	TP-P5	SPKRCONN_RW_OUTN
TPC5A3	A	1	TP-P5	SPKRCONN_RT_OUTN
TPC5L3	A	1	TP-P5	SPKRCONN_RT_OUTN
TPC5L4	A	1	TP-P5	SPKRCONN_RT_OUTN
TPC5A4	A	1	TP-P5	SPKRCONN_RT_OUTP
TPC5L5	A	1	TP-P5	SPKRCONN_RT_OUTP
TPC5L6	A	1	TP-P5	SPKRCONN_RT_OUTP
TPC5B8	A	1	TP-P5	AUD_CONN_RING_SENSE
TPC5B7	A	1	TP-P5	AUD_CONN_RING2_XW
TPC5B6	A	1	TP-P5	AUD_CONN_TIP_SENSE
TPC5B5	A	1	TP-P5	AUD_CONN_HP_SENSE_R
TPC5A7	A	1	TP-P5	
TPC5B3	A	1	TP-P5	AUD_CONN_HP_SENSE_L
TPC5A8	A	1	TP-P5	AUD_CONN_HP_LEFT
TPC5A9	A	1	TP-P5	AUD_CONN_HP_RIGHT
TPC5B0	A	1	TP-P5	AUD_CONN_RING2
TPC5B2	A	1	TP-P5	AUD_CONN_SLEEVE
TPC5K0	A	1	TP-P5	
TPC5K1	A	1	TP-P5	AUD_CONN_SLEEVE_XW
TPC5A5	A	1	TP-P5	SPKR_ID0
TPC5A2	A	1	TP-P5	

EDP , CAMERA,ALS

TPC5C0	A	1	TP-P5	EDP_INT_AUX_N
TPC5C1	A	1	TP-P5	
TPC5C2	A	1	TP-P5	EDP_INT_AUX_P
TPC5C3	A	1	TP-P5	EDP_PANEL_PWR_BUF_EN
TPC5C4	A	1	TP-P5	
TPC5C9	A	1	TP-P5	TP_LCD_IRQ_L
TPC5C8	A	1	TP-P5	EDP_INT_ML_P<0>
TPC5C5	A	1	TP-P5	DP_INT_HPD
TPC5C6	A	1	TP-P5	EDP_INT_ML_N<0>
TPC5C7	A	1	TP-P5	LCD_FSS
TPC5D5	A	1	TP-P5	EDP_INT_ML_P<2>
TPC5D3	A	1	TP-P5	EDP_INT_ML_N<2>
TPC5D1	A	1	TP-P5	EDP_INT_ML_N<1>
TPC5D2	A	1	TP-P5	EDP_INT_ML_P<1>
TPC5D0	A	1	TP-P5	
TPC5D7	A	1	TP-P5	I2C_BKLT_SDA
TPC5E0	A	1	TP-P5	EDP_INT_ML_P<3>
TPC5D9	A	1	TP-P5	I2C_BKLT_SCL
TPC5D8	A	1	TP-P5	EDP_INT_ML_N<3>
TPC5D4	A	1	TP-P5	
TPC5E1	A	1	TP-P5	I2C_TCON_SDA
TPC5E4	A	1	TP-P5	MIPI_FTCAM_DATA_CONN_N<0>
TPC5D6	A	1	TP-P5	
TPC5E3	A	1	TP-P5	I2C_TCON_SCL
TPC5F2	A	1	TP-P5	I2C_CAM_ISOL_SDA
TPC5F1	A	1	TP-P5	MIPI_FTCAM_CLK_CONN_P
TPC5F0	A	1	TP-P5	I2C_CAM_ISOL_SCL
TPC5E9	A	1	TP-P5	MIPI_FTCAM_CLK_CONN_N
TPC5E8	A	1	TP-P5	I2C_ALS_SCL
TPC5E2	A	1	TP-P5	
TPC5E6	A	1	TP-P5	MIPI_FTCAM_DATA_CONN_P<0>
TPC5E7	A	1	TP-P5	I2C_ALS_SDA
TPC5F7	A	1	TP-P5	PP5V_S0_ALSCAM_F
TPC5E5	A	1	TP-P5	
TPC5F9	A	1	TP-P6	PPVIN_S0SW_LCDBKLT_R
TPC5F3	A	1	TP-P5	PPVOUT_S0_LCDBKLT
TPC5F4	A	1	TP-P5	PP3V3_S0SW_LCD
TPC5F6	A	1	TP-P5	PP5V_S0SW_LCD
TPC5F5	A	1	TP-P5	PP3V3_S0SW_LCD
TPC5F8	A	1	TP-P5	
TPC5M1	A	1	TP-P5	BKLT_PWM_MLB2TCON

USBC (PLACE NEAR CONNECTOR)

TPC5G3	A	1	TP-P5	TP_USBC_PP20V_XB
TPC5N3	A	1	TP-P5	TP_USBC_PP20V_XA
TPC5G4	A	1	TP-P5	USBC_XA_SBU1
TPC5G5	A	1	TP-P5	USBC_XA_SBU2
TPC5G7	A	1	TP-P5	USBC_XA_CC2_CONN
TPC5G9	A	1	TP-P5	PP20V_USBC_XB_VBUS
TPC5H0	A	1	TP-P5	PP20V_USBC_XA_VBUS
TPC5H1	A	1	TP-P5	TP_USBC_PP20V_TB
TPC5H2	A	1	TP-P5	TP_USBC_PP20V_TA
TPC5H3	A	1	TP-P5	PP20V_USBC_TB_VBUS
TPC5H4	A	1	TP-P5	PP20V_USBC_TA_VBUS
TPC5I8	A	1	TP-P5	PP20V_USBC_XA_VBUS
TPC5I9	A	1	TP-P5	PP20V_USBC_XA_VBUS
TPC5J1	A	1	TP-P5	PP20V_USBC_XB_VBUS
TPC5J0	A	1	TP-P5	PP20V_USBC_XA_VBUS
TPC5J2	A	1	TP-P5	PP20V_USBC_XB_VBUS
TPC5J3	A	1	TP-P5	PP20V_USBC_XB_VBUS
TPC5J4	A	1	TP-P5	PP20V_USBC_TA_VBUS
TPC5H5	A	1	TP-P5	
TPC5H6	A	1	TP-P5	
TPC5H7	A	1	TP-P5	
TPC5H8	A	1	TP-P5	
TPC5M2	A	1	TP-P5	
TPC5K2	A	1	TP-P5	
TPC5K3	A	1	TP-P5	
TPC5K4	A	1	TP-P5	
TPC5J5	A	1	TP-P5	PP20V_USBC_TA_VBUS
TPC5J6	A	1	TP-P5	PP20V_USBC_TA_VBUS
TPC5J7	A	1	TP-P5	PP20V_USBC_TB_VBUS
TPC5J8	A	1	TP-P5	PP20V_USBC_TB_VBUS
TPC5J9	A	1	TP-P5	PP20V_USBC_TB_VBUS
TPC5N9	A	1	TP-P5	USBC_XB_CC1_CONN
TPC5N8	A	1	TP-P5	USBC_XB_CC2_CONN
TPC5O1	A	1	TP-P5	USBC_TA_CC1_CONN
TPC5O2	A	1	TP-P5	USBC_TA_CC2_CONN
TPC5O3	A	1	TP-P5	USBC_TB_CC1_CONN
TPC5O4	A	1	TP-P5	USBC_TB_CC2_CONN

CORE OS DESBUG

PAGE TITLE	FCT TESTPOINTS 2
Apple Inc.	DRAWING NUMBER 051-02643 · SIZE D
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ICT TEST POINTS, ICT BOUNDARY SCAN TESTPOINTS

CPU XDP and PCH Test-Points

18 6	IN	TRUE	XDP_CPU_TCK	
18 13	IN	TRUE	XDP_PCH_TCK	
18 6	IN	TRUE	XDP_CPU_TDI	
18 6	IN	TRUE	XDP_CPU_TDO	
18 13 6	IN	TRUE	XDP_CPU_TRST_L	
18 6	IN	TRUE	XDP_CPU_TMS	
18 13	IN	TRUE	XDP_PCH_TMS	
18 13	IN	TRUE	XDP_PCH_TDI	
18 13	IN	TRUE	XDP_PCH_TDO	
18 13 6	IN	TRUE	XDP_CPU_PREQ_L	
18 13 6	IN	TRUE	XDP_CPU_PRDY_L	
119 46 35 12	IN	TRUE	PM_PCH_PWROK	
119 46 18 12	IN	TRUE	PM_SYSRST_L	
18 13	IN	TRUE	XDP_PCH_JTAGX	
18 13	BI		PCH_ITP_PMODE	FUNC_TEST=TRUE

H9M BOUNDARY SCAN TESTPOINTS ON FCT TESTPOINT PAGE

TP Debug ACE Nets (EE tests)

30	UPC_XA_GPIO0	TPC622
31	UPC_XB_GPIO0	TPC624
31	UPC_XB_GPIO1	TPC625
108	UPC_TA_GPIO0	TPC626
108	UPC_TA_GPIO1	TPC627
109	UPC_TB_GPIO0	TPC628
109	UPC_TB_GPIO1	TPC629

GPU ICT TESTPONTS

ACE

27 15	BI	JTAG_TBT_X_TMS	FUNC_TEST=TRUE
107 105 27	BI	JTAG_ISP_TDI	FUNC_TEST=TRUE
107 105 27	BI	JTAG_ISP_TCK	FUNC_TEST=TRUE
107 105 27	BI	XDP_JTAG_ISP_TDO	FUNC_TEST=TRUE
121 27	BI	TBT_X_TEST_EN	FUNC_TEST=TRUE

WLAN

39 37	BI	WLAN_JTAG_TMS	FUNC_TEST=TRUE
39 37	BI	WLAN_JTAG_TCK	FUNC_TEST=TRUE
40 37	BI	WLAN_JTAG_TDI	FUNC_TEST=TRUE
37 36	BI	WLAN_JTAG_TDO	FUNC_TEST=TRUE
37 36	BI	WLAN_JTAG_TRST_L	FUNC_TEST=TRUE
105 15	BI	JTAG_TBT_T_TMS	FUNC_TEST=TRUE
39	BI	TP_JTAG_SOC_TRST_L	FUNC_TEST=TRUE

GPU

103 102	BI	GPU_JTAG_TCK	FUNC_TEST=TRUE
103 102	BI	GPU_JTAG_TDI	FUNC_TEST=TRUE
103 102	BI	GPU_JTAG_TDO	FUNC_TEST=TRUE
103 102	BI	GPU_JTAG_TMS	FUNC_TEST=TRUE
103 102	BI	GPU_JTAG_TRST_L	FUNC_TEST=TRUE
46 39	BI	SMC_PCH_SYS_PWROK	FUNC_TEST=TRUE
46 39	BI	SMC_PCH_PWROK	FUNC_TEST=TRUE
119 46 39	BI	SMC_SYSRST_L	FUNC_TEST=TRUE
119 13 6	BI	CPU_PWRGD	FUNC_TEST=TRUE
77 64 39 110	BI	PMU_COLD_RESET_L	FUNC_TEST=TRUE
39	BI	SOC_JTAG_SEL	FUNC_TEST=TRUE
38	BI	SOC_TESTMODE	FUNC_TEST=TRUE
37 36	BI	WLAN_JTAG_SEL	FUNC_TEST=TRUE
105	BI	TBT_T_TEST_EN	FUNC_TEST=TRUE
121 27	BI	TBT_X_TEST_EN	FUNC_TEST=TRUE

SSD BOUNDARY SCAN Test-Points

85 84 83 39 86	IN	TRUE	SSD0_SWDIO_UART_D2R
85 84 83 39 86	IN	TRUE	SSD0_SWCLK_UART_R2D
84 83	IN	TRUE	SSD0_S4E0_JTAG_TDO
83	IN	TRUE	SSD0_S4E0_JTAG_TDI
86 85 84 83	IN	TRUE	SSD0_S4E_JTAG_SEL
85 84	IN	TRUE	SSD0_S4E1_JTAG_TDO
121 86 85	IN	TRUE	SSD0_S4E2_JTAG_TDO
86	IN		SSD0_S4E3_JTAG_TDO
121 86 85	IN	TRUE	SSD0_S4E2_JTAG_TDO
90 89 88 39 91	IN	TRUE	SSD1_SWDIO_UART_D2R
90 89 88 39 91	IN	TRUE	SSD1_SWCLK_UART_R2D
89 88	IN	TRUE	SSD1_S4E0_JTAG_TDO
88	IN	TRUE	SSD1_S4E0_JTAG_TDI
91 90 89 88	IN	TRUE	SSD1_S4E_JTAG_SEL
90 89	IN	TRUE	SSD1_S4E1_JTAG_TDO
91 90	IN	TRUE	SSD1_S4E2_JTAG_TDO
91 89	IN	TRUE	SSD1_S4E3_JTAG_TDO

S4E

PPC603	PVDDCPUAWAKE_SW0
PPC604	PVDDCPUAWAKE_SW1
PPC605	PVDDCPUAWAKE_SW2
PPC606	PVDDCPUAWAKE_SW3
PPC607	PVCCPRIMCORE_SW0
PPC608	PVCCPRIMCORE_SW1
PPC609	P0V8SLPDDR_SW0
PPC610	P0V8SLPDDR_SW1
PPC611	P1V8SLPS2R_SW0
PPC612	P1V1SLPS2R_SW0
PPC613	P1V1SLPS2R_SW1
PPC614	P0V9SLPDDR_SW0
PPC615	P0V9SLPDDR_SW1
PPC616	PVDDCPUSRAMAWAKE_SW0

EE TESTS SWE

53	ISNS_HS_COMPUTING_P	TPC650
53	ISNS_HS_COMPUTING_N	TPC651
53	ISNS_HS_OTHER5V_P	TPC652
53	ISNS_HS_OTHER5V_N	TPC653
53	ISNS_HS_3V3_X_P	TPC654
53	ISNS_HS_3V3_X_N	TPC655
53	ISNS_HS_3V3_T_P	TPC656
53	ISNS_HS_3V3_T_N	TPC657
81 53	ISNS_LCDBKLT_P	TPC658
81 53	ISNS_LCDBKLT_N	TPC659
54	ISNS_1V0_P	TPC660
54	ISNS_1V0_N	TPC661
74 54	ISNS_CPUDDR_P	TPC662
74 54	ISNS_CPUDDR_N	TPC663
54	ISNS_CPUVDDQ_P	TPC664
54	ISNS_CPUVDDQ_N	TPC665
54	CPUVR_ISNS_P	TPC666
54	CPUVR_ISNS_N	TPC667
54	ISNS_WLAN_N	TPC668
54	ISNS_WLAN_P	TPC669
54	ISNS_WL1V8_P	TPC670
54	ISNS_WL1V8_N	TPC671
82 55	ISNS_LCDPANEL_P	TPC672
82 55	ISNS_LCDPANEL_N	TPC673
56	ISNS_CALPE_P	TPC674
56	ISNS_CALPE_N	TPC675
56	CPUGT_ISNS_R_P	TPC676
56	CPUGT_ISNS_R_N	TPC677
71 56	CPUSA_ISNS_P	TPC678
71 56	CPUSA_ISNS_N	TPC679
78 56	ISNS_CPUVCCIO_POS	TPC680
78 56	ISNS_CPUVCCIO_NEG	TPC681
94	GFXIMVP_ISNS_R_N	TPC682
94	GFXIMVP_ISNS_R_P	TPC683
98 58	VDDCIS0_CS_P	TPC684
98 58	VDDCIS0_CS_N	TPC685
58	ISNS_GPU1V8_P	TPC686
58	ISNS_GPU1V8_N	TPC687
98 58	GPUFB_CS_P	TPC688
98 58	GPUFB_CS_N	TPC689
58	ISNS_GPUFBIC_P	TPC6A0
58	ISNS_GPUFBIC_N	TPC6A1
58	ISNS_GPU_HS_P	TPC6A2
58	ISNS_GPU_HS_N	TPC6A3
59 53	SMC_PBUS_VSENSE	TPC6A4
59 58	PMU_CPU_VSENSE	TPC6A5
59 58	PMU_GPU_CORE_VSENSE	TPC6A6
58 56	EADC1_CPUGT_VSENSE	TPC6A7
176 53 64 58 84	GND_CALPE_AVSS	TPC6A8
58 56	EADC1_CPUSA_VSENSE	TPC6A9
58 56	EADC2_GPU_VDDCI_VSENSE	TPC6B0
55 54 58 56	GND_EADC2_COM	TPC6B1
59 53	SMC_DCIN_VSENSE	TPC6B2
68	CHGR_CSI_R_P	TPC6B3
68	CHGR_CSI_R_N	TPC6B4
68 55	CHGR_CSO_R_P	TPC6B5
68 55	CHGR_CSO_R_N	TPC6B6
55	ISNS_PPBUS_MAIN_SSD0_P	TPC6B7
55	ISNS_PPBUS_MAIN_SSD0_N	TPC6B8
55	ISNS_PPBUS_MAIN_SSD1_P	TPC6B9

EE TESTS SWE -2

55	ISNS_PPBUS_MAIN_SSD1_N	TPC6C0
55	ISNS_P3V3_G3W_SSD0_P	TPC6C1
55	ISNS_P3V3_G3W_SSD0_N	TPC6C2
55	ISNS_P3V3_G3W_SSD1_P	TPC6C3
55	ISNS_P3V3_G3W_SSD1_N	TPC6C4
55	ISNS_T139_P	TPC6C7
55	ISNS_T139_N	TPC6C8

WP pins of ROMs

36	BT_SFLASH_WP_L	TPC6D0	PLACE_SIDE=TOP
27	TBT_X_ROM_WP_L	TPC6D1	PLACE_SIDE=TOP
105	TBT_T_ROM_WP_L	TPC6D2	PLACE_SIDE=TOP
102	GPU_ROM_WP_L	TPC6D3	PLACE_SIDE=TOP
46	SPI_SOCROM_WP_L	TPC6D4	PLACE_SIDE=TOP

EE TESTS PCH

12	PCIE_CLK100M_DEBUG_N	TPC620	PLACE_NEAR=U1200.AK6:25MM
12	PCIE_CLK100M_DEBUG_P	TPC621	PLACE_NEAR=U1200.AM6:25MM
36 12	PCH_PCIE_CLK100M_WLAN_N	TPC631	
36 12	PCH_PCIE_CLK100M_WLAN_P	TPC632	
41 12	PCIE_CLK100M_SOC_N	PPC633	PLACE_NEAR=U3900.G12:25MM
41 12	PCIE_CLK100M_SOC_P	PPC634	PLACE_NEAR=U3900.G13:25MM

S4E

TPC690A	SSD0_S4E0_UART_TX	83
TPC691A	SSD1_S4E0_UART_TX	88
TPC692A	SSD0_S4E1_UART_TX	84
TPC693A	SSD1_S4E1_UART_TX	89
TPC694A	SSD0_S4E2_UART_TX	85
TPC695A	SSD0_S4E3_UART_TX	86
TPC696A	SSD1_S4E3_UART_TX	91
TPC697A	SSD0_S4E1_DROOP_L	84
TPC698A	SSD1_S4E2_UART_TX	90
TPC699A	SSD0_CLKREQ2_L	41 47 85
TPC69AA	SSD0_S4E3_DROOP_L	86
TPC69BA	SSD1_S4E2_DROOP_L	85
TPC69CA	SSD0_CLKREQ3_L	41 47 86
TPC69DA	SSD0_S4E0_DROOP_L	83

PAGE TITLE

ICT, MAC-1 ,EE Testpoints

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PAGE TITLE
Desense Caps 1

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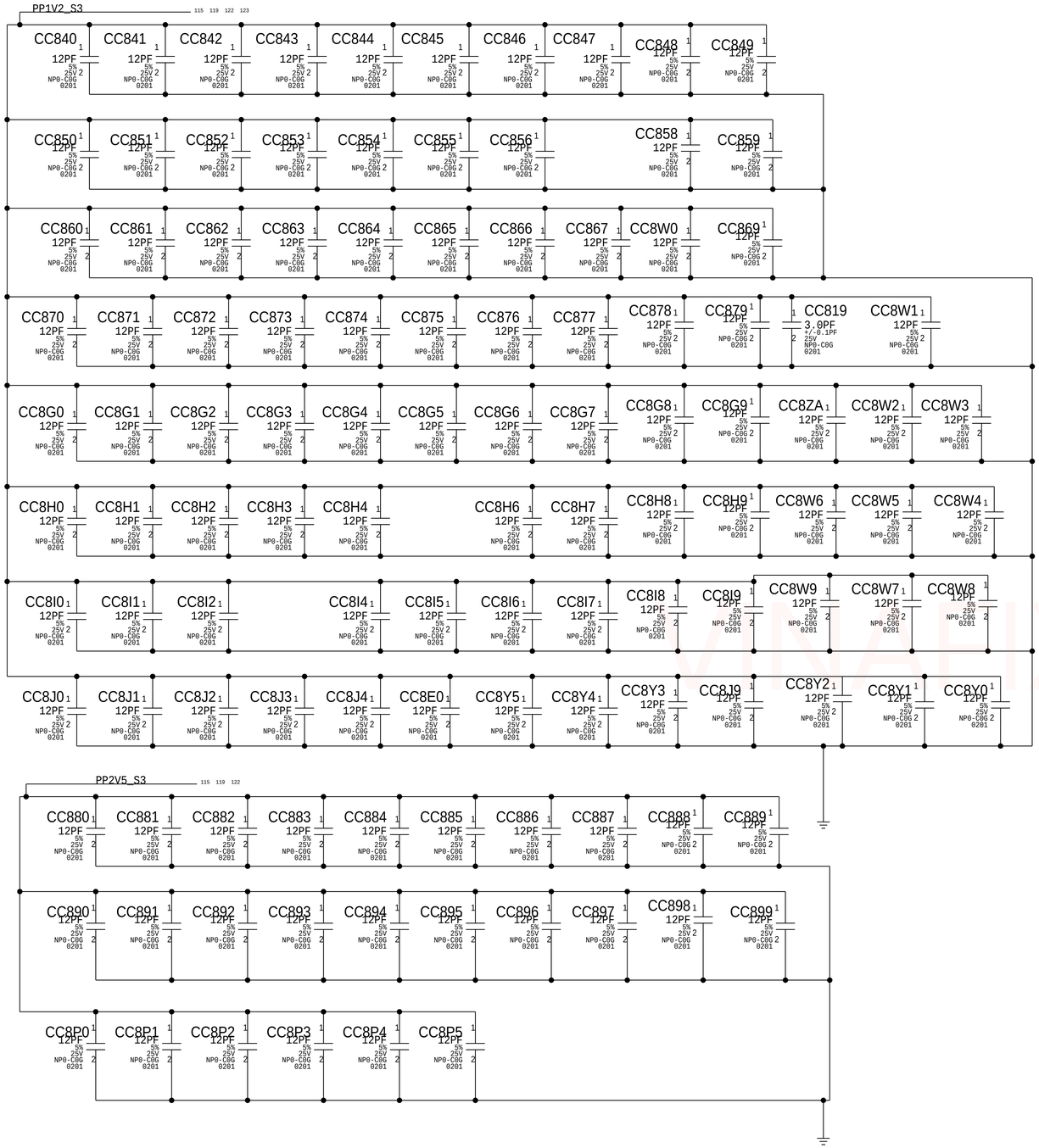

FOR DESENSE IMPROVEMENT
PLACE ONE AT EACH DDR3L MEMORY MODULE.

BOM_COST_GROUP=WIRELESS

PAGE TITLE	Desense Caps 2
	Apple Inc.
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Near NAND IC's

PP1V8_SSD0

CC900 12PF 5% 25V NP0-C0G 0201
CC901 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC902 12PF 5% 25V NP0-C0G 0201
CC903 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC904 12PF 5% 25V NP0-C0G 0201
CC905 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC906 12PF 5% 25V NP0-C0G 0201
CC907 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V9_SSD0

CC908 12PF 5% 25V NP0-C0G 0201
CC909 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC90A 12PF 5% 25V NP0-C0G 0201
CC90B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC90C 12PF 5% 25V NP0-C0G 0201
CC90D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC90E 12PF 5% 25V NP0-C0G 0201
CC90F 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP2V5_NAND_SSD0

CC910 12PF 5% 25V NP0-C0G 0201
CC911 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC912 12PF 5% 25V NP0-C0G 0201
CC913 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC914 12PF 5% 25V NP0-C0G 0201
CC915 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC916 12PF 5% 25V NP0-C0G 0201
CC917 3.0PF +/-0.1PF 25V NP0-C0G 0201

Near GMUX

PP3V3_S5

CC93C 12PF 5% 25V NP0-C0G 0201
CC93D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC93E 12PF 5% 25V NP0-C0G 0201
CC93F 3.0PF +/-0.1PF 25V NP0-C0G 0201

Near VRAMS

PP1V5R1V35_S0_GPU_MEM

CC940 12PF 5% 25V NP0-C0G 0201
CC941 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC942 12PF 5% 25V NP0-C0G 0201
CC943 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC944 12PF 5% 25V NP0-C0G 0201
CC945 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC946 12PF 5% 25V NP0-C0G 0201
CC947 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC948 12PF 5% 25V NP0-C0G 0201
CC949 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC94A 12PF 5% 25V NP0-C0G 0201
CC94B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC94C 12PF 5% 25V NP0-C0G 0201
CC94D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC94E 12PF 5% 25V NP0-C0G 0201
CC94F 3.0PF +/-0.1PF 25V NP0-C0G 0201

Near GPU

PPVCORE_S0_GPU

CC954 12PF 5% 25V NP0-C0G 0201
CC955 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC956 12PF 5% 25V NP0-C0G 0201
CC957 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC958 12PF 5% 25V NP0-C0G 0201
CC959 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC95A 12PF 5% 25V NP0-C0G 0201
CC95B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC95C 12PF 5% 25V NP0-C0G 0201
CC95D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC95E 12PF 5% 25V NP0-C0G 0201
CC95F 3.0PF +/-0.1PF 25V NP0-C0G 0201

Near GPU

PPVDDCI_S0_GPU

CC964 12PF 5% 25V NP0-C0G 0201
CC965 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC966 12PF 5% 25V NP0-C0G 0201
CC967 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC968 12PF 5% 25V NP0-C0G 0201
CC969 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC96A 12PF 5% 25V NP0-C0G 0201
CC96B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC96C 12PF 5% 25V NP0-C0G 0201
CC96D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC96E 12PF 5% 25V NP0-C0G 0201
CC96F 3.0PF +/-0.1PF 25V NP0-C0G 0201

Near Power Shape Top Side

PPBUS_HS_CPU

CC970 12PF 5% 25V NP0-C0G 0201
CC971 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC972 12PF 5% 25V NP0-C0G 0201
CC973 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC974 12PF 5% 25V NP0-C0G 0201
CC975 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC976 12PF 5% 25V NP0-C0G 0201
CC977 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC978 12PF 5% 25V NP0-C0G 0201
CC979 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC97A 12PF 5% 25V NP0-C0G 0201
CC97B 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPBUS_HS_GPU

CC97C 12PF 5% 25V NP0-C0G 0201
CC97D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC97E 12PF 5% 25V NP0-C0G 0201
CC97F 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC980 12PF 5% 25V NP0-C0G 0201
CC981 3.0PF +/-0.1PF 25V NP0-C0G 0201

Near NAND IC's

PP1V8_SSD1

CC918 12PF 5% 25V NP0-C0G 0201
CC919 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC91A 12PF 5% 25V NP0-C0G 0201
CC91B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC91C 12PF 5% 25V NP0-C0G 0201
CC91D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC91E 12PF 5% 25V NP0-C0G 0201
CC91F 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V9_SSD1

CC920 12PF 5% 25V NP0-C0G 0201
CC921 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC922 12PF 5% 25V NP0-C0G 0201
CC923 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC924 12PF 5% 25V NP0-C0G 0201
CC925 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC926 12PF 5% 25V NP0-C0G 0201
CC927 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP2V5_NAND_SSD1

CC928 12PF 5% 25V NP0-C0G 0201
CC929 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC92A 12PF 5% 25V NP0-C0G 0201
CC92B 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC92C 12PF 5% 25V NP0-C0G 0201
CC92D 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC92E 12PF 5% 25V NP0-C0G 0201
CC92F 3.0PF +/-0.1PF 25V NP0-C0G 0201

Near GPU

PP1V8_S0_GPU_LC_IC

CC960 12PF 5% 25V NP0-C0G 0201
CC961 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC962 12PF 5% 25V NP0-C0G 0201
CC963 3.0PF +/-0.1PF 25V NP0-C0G 0201

Near GPU

PP1V5R1V35_S0_GPU_IC

CC950 12PF 5% 25V NP0-C0G 0201
CC951 3.0PF +/-0.1PF 25V NP0-C0G 0201
CC952 12PF 5% 25V NP0-C0G 0201
CC953 3.0PF +/-0.1PF 25V NP0-C0G 0201

Near NAND VR's

PP1V8_SSD0

CC930 12PF 5% 25V NP0-C0G 0201
CC931 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP1V8_SSD1

CC932 12PF 5% 25V NP0-C0G 0201
CC933 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V9_SSD0

CC934 12PF 5% 25V NP0-C0G 0201
CC935 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP0V9_SSD1

CC936 12PF 5% 25V NP0-C0G 0201
CC937 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP2V5_NAND_SSD0

CC938 12PF 5% 25V NP0-C0G 0201
CC939 3.0PF +/-0.1PF 25V NP0-C0G 0201

PP2V5_NAND_SSD1

CC93A 12PF 5% 25V NP0-C0G 0201
CC93B 3.0PF +/-0.1PF 25V NP0-C0G 0201

GFXIMVP_LGATE1

CC987 3.0PF +/-0.1PF 25V NP0-C0G 0201

GFXIMVP_PHASE2

CC988 3.0PF +/-0.1PF 25V NP0-C0G 0201

GFXIMVP_PHASE3

CC98B 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVCORE_S0_GPU

CC98C 3.0PF +/-0.1PF 25V NP0-C0G 0201

GFXIMVP_PHASE1

CC989 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVCORE_S0_GFX_PH1

CC98D 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVCORE_S0_GFX_PH2

CC98E 3.0PF +/-0.1PF 25V NP0-C0G 0201

PPVCORE_S0_GFX_PH3

CC98F 3.0PF +/-0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=WIRELESS

PAGE TITLE: Desense Caps 3

Apple Inc.

DRAWING NUMBER: 051-02643
SIZE: D
REVISION: 4.0.0
BRANCH: evt-0
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DDR4 COMMAND/ADDRESS

Memory Bit/Byte Swizzle

KBL-H DDR4 NET	BIT SWIZZLE
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SYNC_MASTER=j380_mlb SYNC_DATE=02/09/2017

PAGE TITLE

Memory Bite/Byte Swizzle

Apple Inc.

DRAWING NUMBER 051-02643

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REVISION 4.0.0

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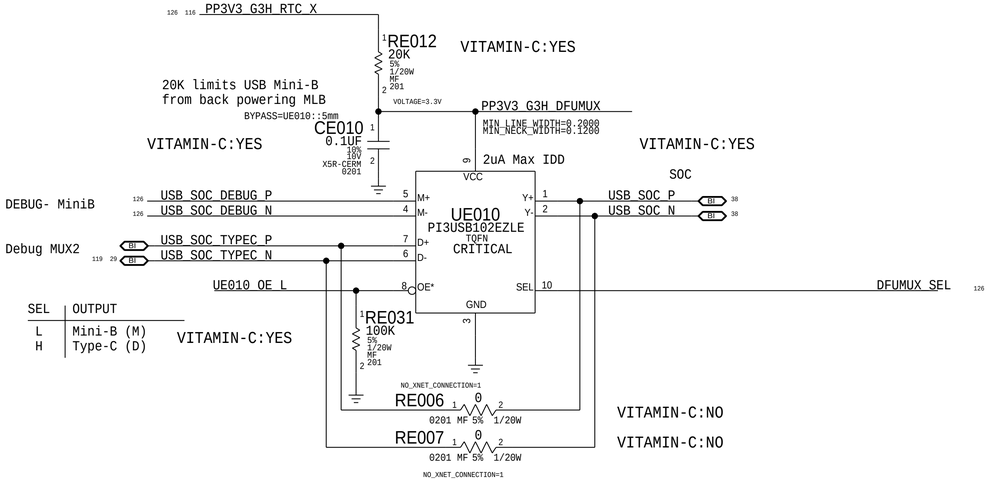
SoC USB DFU Mux



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JE001
AA25D-S038VA1
F-ST-SM

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PCH EXTA USB3

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OUT 38 77 119

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SWD_SOC_SWCLK
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SMC_DEBUGPRT_RX
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MF
201

116 PP3V3_G3H_RTC_X
131 80 PP3V3_S5
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10V
X5R-CERM
0201
CE006
0.1UF
10%
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X5R-CERM
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BYPASS=JE001::15mm
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0402
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Double Check Rails!
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10V
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SYNC_MASTER=Debug
SYNC_DATE=05/03/2017

PAGE TITLE
Dev Support

Apple Inc.

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BRANCH evt-0
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2.2GHZ CPU, 16GB DRAM, PRX GPU, 256GB S4E

EEEE

BOM NUMBER	BOM NAME	BOM OPTIONS
JP4D	639-05681	MLB,2.2GHZ,MC-16,PRX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP4F	639-05682	MLB,2.2GHZ,MC-16,PRX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP4G	639-05683	MLB,2.2GHZ,HY-16,PRX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.2
JP4H	639-05684	MLB,2.2GHZ,HY-16,PRX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 16GB DRAM, PRX GPU, 512GB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP4J	639-05685	MLB,2.2GHZ,MC-16,PRX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP4L	639-05686	MLB,2.2GHZ,MC-16,PRX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP4M	639-05687	MLB,2.2GHZ,HY-16,PRX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.2
JP4P	639-05688	MLB,2.2GHZ,HY-16,PRX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 16GB DRAM, PRX GPU, 1TB S4E

EEEE

BOM NUMBER	BOM NAME	BOM OPTIONS
JP4R	639-05689	MLB,2.2GHZ,MC-16,PRX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP4Q	639-05690	MLB,2.2GHZ,MC-16,PRX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP4W	639-05691	MLB,2.2GHZ,HY-16,PRX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.2
JP4X	639-05692	MLB,2.2GHZ,HY-16,PRX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 16GB DRAM, PRX GPU, 2TB S4E

EEEE

BOM NUMBER	BOM NAME	BOM OPTIONS
JP4Y	639-05693	MLB,2.2GHZ,MC-16,PRX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP50	639-05694	MLB,2.2GHZ,MC-16,PRX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP51	639-05695	MLB,2.2GHZ,MC-16,PRX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP52	639-05696	MLB,2.2GHZ,HY-16,PRX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.2
JP53	639-05697	MLB,2.2GHZ,HY-16,PRX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.2
JP54	639-05698	MLB,2.2GHZ,HY-16,PRX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_16G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 16GB DRAM, PRX GPU, 4TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP55	639-05699	MLB,2.2GHZ,MC-16,PRX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
JP56	639-05700	MLB,2.2GHZ,HY-16,PRX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_16G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, PRX GPU, 256GB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP5Y	639-05721	MLB,2.2GHZ,MC-32,PRX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.2
JP60	639-05722	MLB,2.2GHZ,MC-32,PRX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.2
JP61	639-05723	MLB,2.2GHZ,HY-32,PRX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.2
JP62	639-05724	MLB,2.2GHZ,HY-32,PRX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, PRX GPU, 512GB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP63	639-05725	MLB,2.2GHZ,MC-32,PRX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.2
JP64	639-05726	MLB,2.2GHZ,MC-32,PRX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.2
JP65	639-05727	MLB,2.2GHZ,HY-32,PRX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.2
JP66	639-05728	MLB,2.2GHZ,HY-32,PRX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, PRX GPU, 1TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
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JP68	639-05730	MLB,2.2GHZ,MC-32,PRX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.2
JP69	639-05731	MLB,2.2GHZ,HY-32,PRX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.2
JP6C	639-05732	MLB,2.2GHZ,HY-32,PRX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, PRX GPU, 2TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP6D	639-05733	MLB,2.2GHZ,MC-32,PRX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.2
JP6F	639-05734	MLB,2.2GHZ,MC-32,PRX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.2
JP6G	639-05735	MLB,2.2GHZ,MC-32,PRX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_32G,BAFFIN_PROX,CPU_CFL:2.2
JP6H	639-05736	MLB,2.2GHZ,HY-32,PRX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.2
JP6J	639-05737	MLB,2.2GHZ,HY-32,PRX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.2
JP6K	639-05738	MLB,2.2GHZ,HY-32,PRX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_32G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, PRX GPU, 4TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP6L	639-05739	MLB,2.2GHZ,MC-32,PRX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_32G,BAFFIN_PROX,CPU_CFL:2.2
JP6M	639-05740	MLB,2.2GHZ,HY-32,PRX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_32G,BAFFIN_PROX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, ULX GPU, 4TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP79	639-05759	MLB,2.2GHZ,MC-32,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP7C	639-05760	MLB,2.2GHZ,HY-32,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_32G,BAFFIN_ULX,CPU_CFL:2.2

2.2GHZ CPU, 16GB DRAM, ULX GPU, 256GB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP57	639-05701	MLB,2.2GHZ,MC-16,ULX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP58	639-05702	MLB,2.2GHZ,MC-16,ULX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP59	639-05703	MLB,2.2GHZ,HY-16,ULX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5C	639-05704	MLB,2.2GHZ,HY-16,ULX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.2

2.2GHZ CPU, 16GB DRAM, ULX GPU, 512GB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP5D	639-05705	MLB,2.2GHZ,MC-16,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5F	639-05706	MLB,2.2GHZ,MC-16,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5G	639-05707	MLB,2.2GHZ,HY-16,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5H	639-05708	MLB,2.2GHZ,HY-16,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.2

2.2GHZ CPU, 16GB DRAM, ULX GPU, 1TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP5J	639-05709	MLB,2.2GHZ,MC-16,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5K	639-05710	MLB,2.2GHZ,MC-16,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5L	639-05711	MLB,2.2GHZ,HY-16,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5M	639-05712	MLB,2.2GHZ,HY-16,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.2

2.2GHZ CPU, 16GB DRAM, ULX GPU, 2TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP5N	639-05713	MLB,2.2GHZ,MC-16,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5P	639-05714	MLB,2.2GHZ,MC-16,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5Q	639-05715	MLB,2.2GHZ,MC-16,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5R	639-05716	MLB,2.2GHZ,HY-16,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5T	639-05717	MLB,2.2GHZ,HY-16,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5V	639-05718	MLB,2.2GHZ,HY-16,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_16G,BAFFIN_ULX,CPU_CFL:2.2

2.2GHZ CPU, 16GB DRAM, ULX GPU, 4TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP5W	639-05719	MLB,2.2GHZ,MC-16,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_16G,BAFFIN_ULX,CPU_CFL:2.2
JP5X	639-05720	MLB,2.2GHZ,HY-16,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_16G,BAFFIN_ULX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, ULX GPU, 256GB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP6N	639-05741	MLB,2.2GHZ,MC-32,ULX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP6P	639-05742	MLB,2.2GHZ,MC-32,ULX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP6Q	639-05743	MLB,2.2GHZ,HY-32,ULX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.2
JP6R	639-05744	MLB,2.2GHZ,HY-32,ULX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, ULX GPU, 512GB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP6T	639-05745	MLB,2.2GHZ,MC-32,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP6V	639-05746	MLB,2.2GHZ,MC-32,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP6W	639-05747	MLB,2.2GHZ,HY-32,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.2
JP6X	639-05748	MLB,2.2GHZ,HY-32,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, ULX GPU, 1TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP6Y	639-05749	MLB,2.2GHZ,MC-32,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP70	639-05750	MLB,2.2GHZ,MC-32,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP71	639-05751	MLB,2.2GHZ,HY-32,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.2
JP72	639-05752	MLB,2.2GHZ,HY-32,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.2

2.2GHZ CPU, 32GB DRAM, ULX GPU, 2TB S4E

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BOM NUMBER	BOM NAME	BOM OPTIONS
JP73	639-05753	MLB,2.2GHZ,MC-32,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP74	639-05754	MLB,2.2GHZ,MC-32,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP75	639-05755	MLB,2.2GHZ,MC-32,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_32G,BAFFIN_ULX,CPU_CFL:2.2
JP76	639-05756	MLB,2.2GHZ,HY-32,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.2
JP77	639-05757	MLB,2.2GHZ,HY-32,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.2
JP78	639-05758	MLB,2.2GHZ,HY-32,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_32G,BAFFIN_ULX,CPU_CFL:2.2

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BOM-639 2.2GHz

Apple Inc.

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2.6GHZ CPU, 16GB DRAM, ULX GPU, 512GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP7D	639-05761	MLB,2.6GHZ,MC-16,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7F	639-05762	MLB,2.6GHZ,MC-16,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7G	639-05763	MLB,2.6GHZ,HY-16,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7H	639-05764	MLB,2.6GHZ,HY-16,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.6

2.6GHZ CPU, 16GB DRAM, ULX GPU, 1TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP7J	639-05765	MLB,2.6GHZ,MC-16,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7K	639-05766	MLB,2.6GHZ,MC-16,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7L	639-05767	MLB,2.6GHZ,HY-16,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7M	639-05768	MLB,2.6GHZ,HY-16,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.6

2.6GHZ CPU, 16GB DRAM, ULX GPU, 2TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP7N	639-05769	MLB,2.6GHZ,MC-16,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7P	639-05770	MLB,2.6GHZ,MC-16,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7Q	639-05771	MLB,2.6GHZ,MC-16,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7R	639-05772	MLB,2.6GHZ,HY-16,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7T	639-05773	MLB,2.6GHZ,HY-16,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7V	639-05774	MLB,2.6GHZ,HY-16,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_16G,BAFFIN_ULX,CPU_CFL:2.6

2.6GHZ CPU, 16GB DRAM, ULX GPU, 4TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP7W	639-05775	MLB,2.6GHZ,MC-16,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_16G,BAFFIN_ULX,CPU_CFL:2.6
JP7X	639-05776	MLB,2.6GHZ,HY-16,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_16G,BAFFIN_ULX,CPU_CFL:2.6

2.6GHZ CPU, 32GB DRAM, ULX GPU, 512GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP7Y	639-05777	MLB,2.6GHZ,MC-32,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.6
JP80	639-05778	MLB,2.6GHZ,MC-32,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.6
JP81	639-05779	MLB,2.6GHZ,HY-32,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.6
JP82	639-05780	MLB,2.6GHZ,HY-32,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.6

2.6GHZ CPU, 32GB DRAM, ULX GPU, 1TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP83	639-05781	MLB,2.6GHZ,MC-32,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.6
JP84	639-05782	MLB,2.6GHZ,MC-32,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.6
JP85	639-05783	MLB,2.6GHZ,HY-32,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.6
JP86	639-05784	MLB,2.6GHZ,HY-32,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.6

2.6GHZ CPU, 32GB DRAM, ULX GPU, 2TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP87	639-05785	MLB,2.6GHZ,MC-32,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.6
JP88	639-05786	MLB,2.6GHZ,MC-32,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.6
JP89	639-05787	MLB,2.6GHZ,MC-32,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_32G,BAFFIN_ULX,CPU_CFL:2.6
JP8C	639-05788	MLB,2.6GHZ,HY-32,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.6
JP8D	639-05789	MLB,2.6GHZ,HY-32,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.6
JP8F	639-05790	MLB,2.6GHZ,HY-32,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_32G,BAFFIN_ULX,CPU_CFL:2.6

2.6GHZ CPU, 32GB DRAM, ULX GPU, 4TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP8G	639-05791	MLB,2.6GHZ,MC-32,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_32G,BAFFIN_ULX,CPU_CFL:2.6
JP8H	639-05792	MLB,2.6GHZ,HY-32,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_32G,BAFFIN_ULX,CPU_CFL:2.6

2.2GHZ CPU, 16GB DRAM, PRX GPU, 2TB S4E TLC

BOM NUMBER	BOM NAME	BOM OPTIONS
939-05880	MLB,2.2GHZ,MC-16,PRX,TLC-WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_TLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2
939-05879	MLB,2.2GHZ,MC-16,PRX,TLC-TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_TLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.2

DC-DC BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
939-04900	MLB,CPU-SK-S,NO_GPU,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,BOM_8L,CPU_SKL:SOCKET
939-04901	MLB,NO_CPU,GPU-SK-S,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,BOM_8L,STARDUST:VDDC
939-04904	MLB,NO_CPU,GPU-SK-M,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,BOM_8L,STARDUST:VDDCI_MVDD
939-04902	MLB,NO_CPU,NO_GPU,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,BOM_8L

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2.9GHZ CPU, 16GB DRAM, PRX GPU, 256GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP8J	639-05793	MLB,2.9GHZ,MC-16,PRX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP8K	639-05794	MLB,2.9GHZ,MC-16,PRX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP8L	639-05795	MLB,2.9GHZ,HY-16,PRX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.9
JP8M	639-05796	MLB,2.9GHZ,HY-16,PRX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 16GB DRAM, PRX GPU, 512GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP8N	639-05797	MLB,2.9GHZ,MC-16,PRX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP8P	639-05798	MLB,2.9GHZ,MC-16,PRX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP8Q	639-05799	MLB,2.9GHZ,HY-16,PRX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.9
JP8R	639-05800	MLB,2.9GHZ,HY-16,PRX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 16GB DRAM, PRX GPU, 1TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP8T	639-05801	MLB,2.9GHZ,MC-16,PRX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP8V	639-05802	MLB,2.9GHZ,MC-16,PRX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP8X	639-05803	MLB,2.9GHZ,HY-16,PRX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.9
JP8Y	639-05804	MLB,2.9GHZ,HY-16,PRX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 16GB DRAM, PRX GPU, 2TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP90	639-05805	MLB,2.9GHZ,MC-16,PRX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP91	639-05806	MLB,2.9GHZ,MC-16,PRX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP92	639-05807	MLB,2.9GHZ,MC-16,PRX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP93	639-05808	MLB,2.9GHZ,HY-16,PRX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.9
JP94	639-05809	MLB,2.9GHZ,HY-16,PRX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_16G,BAFFIN_PROX,CPU_CFL:2.9
JP95	639-05810	MLB,2.9GHZ,HY-16,PRX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_16G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 16GB DRAM, PRX GPU, 4TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP96	639-05811	MLB,2.9GHZ,MC-16,PRX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_16G,BAFFIN_PROX,CPU_CFL:2.9
JP97	639-05812	MLB,2.9GHZ,HY-16,PRX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_16G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, PRX GPU, 256GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP9Y	639-05833	MLB,2.9GHZ,MC-32,PRX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPC0	639-05834	MLB,2.9GHZ,MC-32,PRX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPC1	639-05835	MLB,2.9GHZ,HY-32,PRX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.9
JPC2	639-05836	MLB,2.9GHZ,HY-32,PRX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, PRX GPU, 512GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JPC3	639-05837	MLB,2.9GHZ,MC-32,PRX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPC4	639-05838	MLB,2.9GHZ,MC-32,PRX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPC5	639-05839	MLB,2.9GHZ,HY-32,PRX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.9
JPC6	639-05840	MLB,2.9GHZ,HY-32,PRX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, PRX GPU, 1TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JPC7	639-05841	MLB,2.9GHZ,MC-32,PRX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPC8	639-05842	MLB,2.9GHZ,MC-32,PRX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPC9	639-05843	MLB,2.9GHZ,HY-32,PRX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.9
JPCD	639-05844	MLB,2.9GHZ,HY-32,PRX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, PRX GPU, 2TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JPCF	639-05845	MLB,2.9GHZ,MC-32,PRX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPCG	639-05846	MLB,2.9GHZ,MC-32,PRX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPCH	639-05847	MLB,2.9GHZ,MC-32,PRX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPCJ	639-05848	MLB,2.9GHZ,HY-32,PRX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.9
JPCL	639-05849	MLB,2.9GHZ,HY-32,PRX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_32G,BAFFIN_PROX,CPU_CFL:2.9
JPCM	639-05850	MLB,2.9GHZ,HY-32,PRX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_32G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, PRX GPU, 4TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JPCN	639-05851	MLB,2.9GHZ,MC-32,PRX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_32G,BAFFIN_PROX,CPU_CFL:2.9
JPCQ	639-05852	MLB,2.9GHZ,HY-32,PRX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_32G,BAFFIN_PROX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, ULX GPU, 4TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JPDF	639-05871	MLB,2.9GHZ,MC-32,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPDG	639-05872	MLB,2.9GHZ,HY-32,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_32G,BAFFIN_ULX,CPU_CFL:2.9

2.9GHZ CPU, 16GB DRAM, ULX GPU, 256GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP97	639-05813	MLB,2.9GHZ,MC-16,ULX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP98	639-05814	MLB,2.9GHZ,MC-16,ULX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP99	639-05815	MLB,2.9GHZ,HY-16,ULX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9C	639-05816	MLB,2.9GHZ,HY-16,ULX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.9

2.9GHZ CPU, 16GB DRAM, ULX GPU, 512GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP9D	639-05817	MLB,2.9GHZ,MC-16,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9F	639-05818	MLB,2.9GHZ,MC-16,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9G	639-05819	MLB,2.9GHZ,HY-16,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9H	639-05820	MLB,2.9GHZ,HY-16,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.9

2.9GHZ CPU, 16GB DRAM, ULX GPU, 1TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP9J	639-05821	MLB,2.9GHZ,MC-16,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9K	639-05822	MLB,2.9GHZ,MC-16,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9L	639-05823	MLB,2.9GHZ,HY-16,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9M	639-05824	MLB,2.9GHZ,HY-16,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.9

2.9GHZ CPU, 16GB DRAM, ULX GPU, 2TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP9N	639-05825	MLB,2.9GHZ,MC-16,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9P	639-05826	MLB,2.9GHZ,MC-16,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9Q	639-05827	MLB,2.9GHZ,MC-16,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9R	639-05828	MLB,2.9GHZ,HY-16,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9T	639-05829	MLB,2.9GHZ,HY-16,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9V	639-05830	MLB,2.9GHZ,HY-16,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_16G,BAFFIN_ULX,CPU_CFL:2.9

2.9GHZ CPU, 16GB DRAM, ULX GPU, 4TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JP9W	639-05831	MLB,2.9GHZ,MC-16,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,MC_16G,BAFFIN_ULX,CPU_CFL:2.9
JP9X	639-05832	MLB,2.9GHZ,HY-16,ULX,SM-4TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_4TB_3DV4,HY_16G,BAFFIN_ULX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, ULX GPU, 256GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JPCR	639-05853	MLB,2.9GHZ,MC-32,ULX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPCT	639-05854	MLB,2.9GHZ,MC-32,ULX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPCV	639-05855	MLB,2.9GHZ,HY-32,ULX,WD-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_256_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.9
JPCW	639-05856	MLB,2.9GHZ,HY-32,ULX,TS-256,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_256_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, ULX GPU, 512GB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JPCX	639-05857	MLB,2.9GHZ,MC-32,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPCY	639-05858	MLB,2.9GHZ,MC-32,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPD0	639-05859	MLB,2.9GHZ,HY-32,ULX,WD-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,WD_512_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.9
JPD1	639-05860	MLB,2.9GHZ,HY-32,ULX,TS-512,X1190	ALTERNATE,BASE_BOM,DEVEL_BOM,TS_512_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, ULX GPU, 1TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JPD2	639-05861	MLB,2.9GHZ,MC-32,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPD3	639-05862	MLB,2.9GHZ,MC-32,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPD4	639-05863	MLB,2.9GHZ,HY-32,ULX,WD-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,WD_1TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.9
JPD5	639-05864	MLB,2.9GHZ,HY-32,ULX,TS-1TB,X1190	ALTERNATE,BASE_BOM,BOM_6L,DEVEL_BOM,TS_1TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.9

2.9GHZ CPU, 32GB DRAM, ULX GPU, 2TB S4E

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
JPD6	639-05865	MLB,2.9GHZ,MC-32,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPD7	639-05866	MLB,2.9GHZ,MC-32,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPD8	639-05867	MLB,2.9GHZ,MC-32,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,MC_32G,BAFFIN_ULX,CPU_CFL:2.9
JPD9	639-05868	MLB,2.9GHZ,HY-32,ULX,WD-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,WD_2TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.9
JPDC	639-05869	MLB,2.9GHZ,HY-32,ULX,TS-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,TS_2TB_PMLC,HY_32G,BAFFIN_ULX,CPU_CFL:2.9
JPDD	639-05870	MLB,2.9GHZ,HY-32,ULX,SM-2TB,X1190	ALTERNATE,BASE_BOM,BOM_8L,DEVEL_BOM,SM_2TB_3DV4,HY_32G,BAFFIN_ULX,CPU_CFL:2.9

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Apple Inc.

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Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00046	197S00036		ALL	Epson w/ TXC
197S00047	197S00036		ALL	Kyocera w/ TXC
197S00048	197S00036		ALL	Murata w/ TXC
376S1080	376S0820		ALL	
152S00726	152S00592		ALL	
376S1053	376S0604		ALL	Diodes alt to Fairchild
353S00636	353S4037		ALL	
155S00007	155S0667		ALL	
376S1106	376S0678		ALL	Fairchild alt to Vishay
371S00127	371S00182		ALL	
152S00769	152S00659		ALL	
372S00016	372S00015		ALL	
107S00041	107S00039		ALL	
740S00041	740S0159		ALL	
311S00138	311S0436		ALL	
152S00725	152S00590		ALL	
152S00841	152S00238		ALL	
376S00219	376S00079		ALL	TI for Fairchild
311S00121	311S0398		ALL	
311S0596	311S0593		ALL	
353S3526	353S3528		ALL	
353S3527	353S3528		ALL	
197S00131	197S00116		ALL	
197S00117	197S00116		ALL	
197S00115	197S00116		ALL	
152S00398	152S00204		ALL	
152S00786	152S00344		ALL	
311S00165	311S00164		ALL	
128S00050	128S0351		ALL	
138S00047	138S00073		ALL	
353S01041	353S01042		ALL	
155S0665	155S00232		ALL	
740S00051	740S00050		ALL	
152S00724	152S00311		ALL	
155S0694	155S0387		ALL	
103S0321	103S0276		ALL	
740S0144	740S0118		ALL	
740S00028	740S0118		ALL	
138S00077	138S00035		ALL	
138S00093	138S00035		ALL	
138S00056	138S1100		ALL	
107S00015	107S00011		ALL	
152S00543	152S00484		ALL	
155S00018	155S0664		ALL	Murata w/ Taiyo
152S00359	152S00253		ALL	Chillisin alt to Cyntec
311S00118	311S0489		ALL	
155S00365	155S00191		ALL	
107S00070	107S0085		ALL	
138S0660	138S0684		ALL	
138S0846	138S0811		ALL	
155S0914	155S0897		ALL	
155S00190	155S0897		ALL	
138S00117	138S00071		ALL	
353S01346	353S01320		ALL	
376S00281	376S1147		ALL	
376S00230	376S00174		ALL	
128S00022	128S00018		ALL	
376S00304	376S1187		ALL	

311S0426	311S00007		ALL	
138S00229	138S00107		ALL	
353S01614	353S4159		ALL	
132S00202	132S00175		ALL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S00878	353S00599		ALL	
371S00089	371S00085		ALL	
107S0248	107S0250		ALL	
107S00033	107S00034		ALL	
107S00103	107S00058		ALL	Cyntec w/ Yageo
311S00013	311S0508		ALL	Part wi
132S00064	132S0409		ALL	
128S0364	128S0264		ALL	Kemet w/ Panasonic
128S00058	128S00018		ALL	NEC w/ Rohm
107S00071	107S00053		ALL	
376S00014	376S0761		ALL	
376S00086	376S0761		ALL	
107S00044	107S00076		ALL	
740S00003	740S0135		ALL	
128S00070	128S00007		ALL	
740S00019	740S00007		ALL	Bourns w/ Polytronics
353S00852	353S4262		ALL	TI w/ OnSemi
138S0775	138S0860		ALL	
138S0789	138S0941		ALL	Murata w/ SS
152S00363	152S00048		ALL	
152S00415	152S00140		ALL	
155S00204	155S0731		ALL	
311S00060	311S0273		ALL	
128S00009	128S00007		ALL	
138S0738	138S1101		ALL	Samsung alt to Murata
107S00234	107S00235		ALL	
311S00156	311S00129		ALL	
155S0660	155S0513		ALL	
197S00120	197S00118		ALL	
152S00368	152S00269		ALL	
311S0271	311S00008		ALL	NXP w/ Diodes
311S00104	311S00091		ALL	

128S00039	128S00038		ALL	
128S0302	128S00038		ALL	
138S1103	138S0719		ALL	
376S00074	376S0855		ALL	
311S00180	311S00181		ALL	
152S00770	152S0857		ALL	
740S00033	740S00002		ALL	
155S00166	155S0391		ALL	
107S0249	107S0251		ALL	
155S00401	155S00067		ALL	
152S00369	152S00268		ALL	Cyntec w/ NEC
371S00074	371S0602		ALL	
138S0689	138S0701		ALL	
128S00087	128S00011		ALL	
128S00031	128S00011		ALL	
128S00026	128S00011		ALL	
152S00182	152S00703		ALL	
152S00705	152S00412		ALL	
376S00303	376S00012		ALL	
152S00864	152S00851		ALL	
311S00179	311S00166		ALL	
353S01505	353S01389		ALL	
353S01506	353S01404		ALL	
311S00057	311S0612		ALL	
377S0155	377S0184		ALL	
152S00403	152S00322		ALL	

311S00193	311S00192		ALL	
371S00170	371S00125		ALL	
376S00302	376S1038		ALL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
103S00248	103S00247		ALL	8.06K 0.1% RESISTOR
103S00250	103S00249		ALL	18.2K 0.1% RESISTOR
116S00006	116S0175		ALL	0OHM RESISTOR
128S00062	128S00067		ALL	150UF POLY CAP
128S00069	128S00067		ALL	150UF POLY CAP
128S00065	128S00067		ALL	150UF POLY CAP
138S00097	138S0750		ALL	4.7UF CAP
131S00134	131S00041		ALL	12pF Desense:31561601
107S00101	107S00005		ALL	5mOhm :31560708
107S00087	107S00029		ALL	5mOhm :31560843
107S00086	107S00056		ALL	3mOhm : 31560937
107S00100	107S00057		ALL	2mOhm : 31561063
107S0240	107S0255		ALL	1mOhm : 31561401
107S00139	107S0178		ALL	220KOhm :31561213
128S0296	128S0487		ALL	47uF-PT : 31561532
128S00012	128S0487		ALL	47uF-PT : 31561532
138S0786	138S0705		ALL	Murata w/ Samsung
353S00832	353S00525		ALL	IMVP SA
353S00831	353S00519		ALL	IMVP VCORE
152S00782	152SS00772		ALL	IMVP CORE INDUCTOR
138S00105	138S00037		ALL	10uF CER : 31563978
138S0714	138S0713		ALL	10UF : 31564912
138S0648	138S0703		ALL	4.7uF CER : 31564224
138S0715	138S0732		ALL	1UF CER : 31565015
152S00845	152S00815		ALL	
138S00111	138S00036		ALL	20uF CER : 31563894
132S00012	132S0401		ALL	0.22uF : 31563715
138S00084	138S00060		ALL	47uF CER : 31564055
138S0739	138S0706		ALL	NEC w/ Vishay
138S0945	138S0706		ALL	NEC w/ Rohm
138S0641	138S0700		ALL	Murata w/ SS&Taiyo
138S0759	138S0762		ALL	
138S00049	138S0831		ALL	
107S00090	107S00055		ALL	
138S0863	138S0853		ALL	
138S00006	138S0835		ALL	
377S0077	377S0183		ALL	
371S00180	371S00077		ALL	NXP alt to Diodes
138S00104	138S0978		ALL	
138S00024	138S0986		ALL	
152S00434	152S1829		ALL	
197S00053	197S00050		ALL	Kyocera w/ TXC
197S00054	197S00050		ALL	NDK w/ TXC
197S00055	197S00050		ALL	Murata w/ TXC
335S00270	335S00203		ALL	Adesto for Micronix
155S00034	155S0706		ALL	Taiyo w/ Murata
353S00879	353S00754		ALL	
155S00203	155S0894		ALL	
152S00461	152S00112		ALL	
376S00146	376S1061		ALL	
152S00704	152S00413		ALL	
152S00199	152S00413		ALL	
335S00066	335S0946		ALL	
372S0186	372S0185		ALL	
311S00177	311S00178		ALL	
353S00750	353S00877		ALL	
152S00707	152S00689		ALL	
376S00282	376S1128		ALL	

VRAM ALT SUB-BOMS

685-00222	685-00221		ALL	
685-00223	685-00221		ALL	
685-00224	685-00221		ALL	
685-00225	685-00221		ALL	

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BOM Alt Table

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Power Button

PLACE_SIDE=TOP

DBG_BTN SWK000 SOX-152HNT SM

PMU_ONOFF_L

RSLOC Button

DBG_BTN SWK001 SOX-152HNT SM

PMU_RSLOC_RST_L

Power Button

PLACE_SIDE=BOTTOM

DBG_BTN SWK002 SOX-152HNT SM

PMU_ONOFF_L

Button for Force DFU

PLACE_SIDE=BOTTOM

DBG_BTN SWK003 SOX-152HNT SM

SOC_FORCE_DFU

PP1V8_SLPS2R

Power State Debug LEDs

(For development only)

PP3V3_S5

DBGLED RK090 20K 5% 1/20W MF 201

DBGLED_S5

DBGLED DK090 GRN-90MCD-5MA-2.85V 0402

PLACE_SIDE=BOTTOM

SILK_PART=S5_ON

DBGLED RK093 20K 5% 1/20W MF 201

DBGLED_S0I3

DBGLED DK093 GRN-90MCD-5MA-2.85V 0402

PLACE_SIDE=BOTTOM

SILK_PART=S0I3_ON

DBGLED QK092 DMN5L06VK-7 SOT563 VER 3

DBGLED_S0I3_D

PM_SLP_S0_L

CPU_C10_GATE_L

DBGLED RK096 51K 5% 1/20W MF 201

DBGLED_C10

DBGLED QK092 DMN5L06VK-7 SOT563 VER 3

DBGLED DK096 GRN-90MCD-5MA-2.85V 0402

PLACE_SIDE=BOTTOM

SILK_PART=S0_ON

System State LEDs

INPUT					OUTPUT		
PMU_ACT_RDY	SLP_SCFET_EN	SLP_S0_L	VDDQ_EN	1V8G3S_EN	R	G	B
0	0	0	0	0	B	1	1
0	0	0	0	1	0	1	1
1	1	0	0	1	0	0	1
0	0	0	1	1	0	1	0
1	1	0	1	1	1	1	0
1	1	1	1	1	1	0	1

PP3V3_G3H_RTC_X

DBGLED RK022 0 5% 1/20W MF 0201

P3V3_G3H_RTC_DEBUG_LED_R

DBGLED CK007 0.1UF 10% 10V X5R-CERM 0201

BYPASS=UK020::10mm

DBGLED UK020 SLG4AP41990 STQFN

VDD

PMU_ACTIVE_READY (IPD)

P1V1_SLPDDR_SCFET_EN (IPD)

PM_SLP_S0* (IPD)

PVDDQ_EN (IPD)

P1V8G3S_EN (IPD)

CRITICAL

GND

(OD) R SSTATE_RED_R

(OD) G SSTATE_GREEN_R

(OD) B SSTATE_BLUE_R

RFU1 NC

RFU2 NC

RFU3 NC

RFU4 NC

PMU_ACTIVE_READY DBGLED RK027 0 5% 1/20W MF 0201 PMU_ACTIVE_READY_R

P1V1_SLPDDR_SCFET_EN DBGLED RK015 0 5% 1/20W MF 0201 P1V1_SLPDDR_SCFET_EN_R

PM_SLP_S3_L DBGLED RK016 0 5% 1/20W MF 0201 PM_SLP_S0_R_L

PVDDQ_EN DBGLED RK017 0 5% 1/20W MF 0201 PVDDQ_EN_LED

P1V8G3S_EN DBGLED RK018 0 5% 1/20W MF 0201 P1V8G3S_EN_R

DBGLED RK019 2.1K 1% 1/20W MF 201

SSTATE_RED

DBGLED RK020 5.1K 1% 1/20W MF 201

SSTATE_GREEN

DBGLED RK021 4.75K 1% 1/20W MF 201

SSTATE_BLUE

DBGLED DK000 LTST-C32JBGEW SM

SOC State LEDs

PP1V8_SLPS2R

DBGLED QK000 DMN5L06VK-7 SOT563 VER 5

SOC_RED_SLPS2R

DBGLED RK023 2.1K 1% 1/20W MF 201

SOC_RED_R

P1V1_SLPDDR_SOCFET_EN

DBGLED QK000 DMN5L06VK-7 SOT563 VER 5

SOC_GREEN_DDR

DBGLED RK024 5.1K 1% 1/20W MF 201

SOC_GREEN_R

DBGLED DK001 LTST-C32JBGEW SM

PP1V8_AWAKE

DBGLED QK001 DMN5L06VK-7 SOT563 VER 5

SOC_BLUE_AWAKE

DBGLED RK025 4.75K 1% 1/20W MF 201

SOC_BLUE_R

SOC_DFU_STATUS

DBGLED QK001 DMN5L06VK-7 SOT563 VER 5

SOC_AMBER_DFU

DBGLED RK026 5.1K 1% 1/20W MF 201

SOC_AMBER_R

DFU LED

DBGLED DK002 AMBER-605NM-35-56MCD LTST-C281KFKT-SM

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=ADITYA SYNC_DATE=03/22/2017

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