Compal Confidential

DPF50 MB Schematic Document

LA-F841P

Version 0.1

Date : 2017/08/25

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

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Title: Cover Page		
Size: Custom	Document Number: LA-F841P	Rev: 0.1
Date: Monday, August 28, 2017	Sheet 1 of 65	

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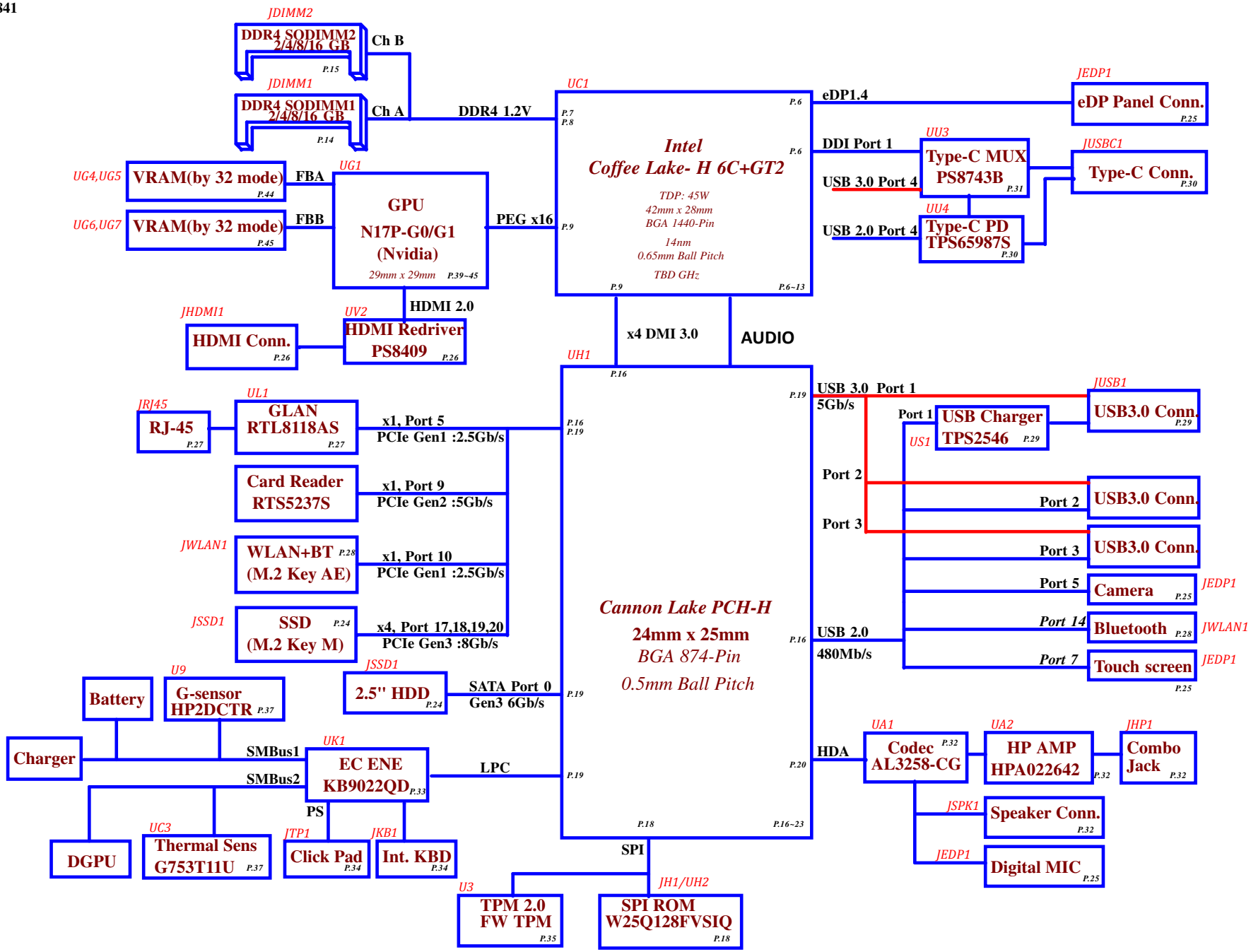
Model Name :Targaryen

File Name : LA-F841



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Size / Document Number	LA-F841P
Custom	Rev 0.1
Date: Monday, August 28, 2017	Sheet 2 of 65

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID /PCB Revision	Rb	V_{AD_BID} min	V_{AD_BID} TYP	V_{AD_BID} Max	EC AD3
0 --> 0.1	0		0 V	0.300 V	0x00 - 0x13
1 --> 0.2	12K +/- 1%	0.347 V	0.354 V	0.36 V	0x14 - 0x1E
2 --> 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25
3 --> 0.4	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30
4 --> 0.5	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A
5 --> 0.6	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45
6 --> 0.7	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54
7 --> 0.8	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64
8 --> 0.9	75K +/- 1%	1.398 V	1.414 V	1.430 V	0x65 - 0x76
9 --> 1.0	100K +/- 1%	1.634 V	1.650 V	1.667 V	0x77 - 0x87
10 --> 1.1	130K +/- 1%	1.849 V	1.865 V	1.881V	0x88 - 0x96
11 --> 1.2	160K +/- 1%	2.015 V	2.031 V	2.046 V	0x97 - 0xA4
12 --> 1.3	200K +/- 1%	2.185 V	2.200 V	2.215 V	0xA5 - 0xAF
13 --> 1.4	240K +/- 1%	2.316V	2.329V	2.343V	0xB0 - 0xB7
14 --> 1.5	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xBF
15 --> 1.6	330K +/- 1%	2.521 V	2.533V	2.544 V	0xC0 - 0xC9
16 --> 1.7	430K +/- 1%	2.667 V	2.677 V	2.687 V	0xCA - 0xD4
17 --> 1.8	560K +/- 1%	2.791 V	2.800 V	2.808 V	0xD5 - 0xDD
18 --> 1.9	750K +/- 1%	2.905 V	2.912 V	2.919 V	0xDE - 0xF0
19 --> 2.0	NC	3.000 V	3.000 V		0xF1 - 0xFF

HSIO Port Table(CPU)

HSIO Port	Device	PCIE CLK&CLKREQ	HPD
PEG	DGPU (DIS)	CLK4 & & CLKREQ#4	
DDI1	TYPE-C PORT		DDPB_HPD0
DDI2	---		DDPC_HPD1
DDI3	---		
eDP	embedded Display		EDP_HPD

Power State

SIGNAL / STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCH SMBUS Address Table

PCH_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
PCH_SMBCLK PCH_SMBDATA	+3V_PCH_PRIM	JDIMM1	0X50	0XA0	0XA1
		JDIMM3	0X52	0XA4	0XA3
		TOUCH PAD			
PCH_SML0CLK PCH_SML0DATA	+3V_PCH_PRIM	NA			
PCH_SML1CLK PCH_SML1DATA	+3V_PCH_PRIM	EC	TBC	TBC	TBC
		GPU	0x4F	0X9E	0X9F

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
SMBUS Port1	+3V_SMBUS	BAT	0x16	TBC	TBC
		CHGR	0x09	0x12	0x13
		G-Sensor	0x29	0x52	0x53
SMBUS Port2	+3VL	PCH	TBC		
		GPU	0x4F	0X9E	0X9F
		THERMAL	0x48	0X90	0x91
		PD	0x38	0X70	0x71
		Type-C MUX	0x10 0x11	0X20 0X22	0x21 0x23

I2C Address Table

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit) Write	Address (8bit) Read
I2C_0_SCL I2C_0_SDA	+3VS				
I2C_1_SCL I2C_1_SDA	+3VS				

BOM Structure Table (1/2)

Function	Stuff	Un-Stuff
CFL-H SKU	CFL_H@	
DGPU SKU	DIS@	
VRAM STRAP/3G	3G@	
VRAM STRAP/6G	6G@	
GC6	GC6@	@GC6@
Touch		TS@
eSPI I/F	LPC@	FSPI@
TPM 9665	9665@	@9665@
TPM 9670	9670@	@9670@
CNVI	CNVI@	@CNVI@
EMI Components	EMI@ VGAEMI@	@EMI@
ESD Components	ESD@	@ESD@
RF Components	RF@	@RF@
XDP	XDP@	
ME Connector	CONN@	
STANDOFF	STD@	
For Signal Test	MP@	
VGA POWER SKU	VGA@	

HSIO Port Table(PCH)

HSIO Port	Capable	USB3.0	PCIE	SATA	Device	PCIE CLK&CLKREQ	NOTE
0	USB3.1_1(OTG)	1			USB3.1 PORT 1		
1	USB3.1_2 /	2			USB3.1 PORT 2		
2	USB3.1_3	3			USB3.1 PORT 3		
3	USB3.1_4	4			TYPE-C PORT		
4	USB3.1_5	5					
5	USB3.1_6	6					
6	USB3.1_7 / PCIE_1	7	1				
7	USB3.1_8 / PCIE_2	8	2				
8	USB3.1_9 / PCIE_3	9	3				
9	USB3.1_10 / PCIE_4	10	4				
10	PCIE_5 / GbE		5		LAN	CLK5 & CLKREQ#5	
11	PCIE_6		6				
12	PCIE_7		7				
13	PCIE_8		8				
14	PCIE_9 / GbE		9		CARD READER	CLK3 & CLKREQ#3	
15	PCIE_10		10		WLAN	CLK1 & CLKREQ#1	
16	PCIE_11 / SATA_0A		11	0	HDD		
17	PCIE_12 / GbE / SATA_1A		12	1			
18	PCIE_13 / GbE / SATA_0B		13	0			
19	PCIE_14 / SATA_1B		14	1			
20	PCIE_15 / SATA_2		15	2			
21	PCIE_16 / SATA_3		16	3			
22	PCIE_17 / SATA_4		17	4			
23	PCIE_18 / SATA_5		18	5	NGFF SSD	CLK2 & CLKREQ#2	Support SATA function on SATA#4
24	PCIE_19		19				
25	PCIE_20		20				
26	PCIE_21		21				
27	PCIE_22		22				
28	PCIE_23		23				
29	PCIE_24		24				

USB2.0 Port Table

USB2	Function
1	USB3.1 PORT 1
2	USB3.1 PORT 2
3	USB3.1 PORT 3
4	TYPE-C PORT
5	IR Camera
6	
7	Touch Panel
8	
9	
10	
11	
12	
13	
14	WLAN+BT Module

Voltage Rails

Power Plane	Description	S0	S0ix	S3	S4/S5	DS3
VIN	Adapter power supply	N/A	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A	N/A
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF	OFF
+VCC_SA	System Agent voltage Supply	ON	OFF	OFF	OFF	OFF
+VCC_GT/+VCC_GTX	Sliced graphics power rail	ON	OFF	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF	OFF
+VCC_EOPIO/+VCC_EDRAM	Processor EOPIO/EDRAM supply	ON	OFF	OFF	OFF	OFF
+1.05VALW	System +1.0V power rail	ON	ON	ON	ON*	OFF
+0.95VS_VCCIO	+1.0VS IO power rail	ON	ON	OFF	OFF	OFF
+1.05V_VCCMPHY	+1.0V power for PCH MODPHY rails	ON/OFF	ON/OFF	ON/OFF	ON/OFF	OFF
+0.95VS_DGPU	+0.95VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	ON	OFF	ON
+1.5VS_MEM_GFX	+1.5VS power rail for GPU/VRAM	ON	OFF	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*	OFF
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF	OFF
+1.8VGS	+1.8VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+2.5V	DDR4 +2.5Vpp power rail	ON	ON	ON	OFF	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*	ON
+3VALW	+3VALW power for PCH suspend rails	ON	ON	ON	ON*	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*	ON
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON	ON
+3VS	System +3VS power rail	ON	ON	OFF	OFF	OFF
+3VGS	+3VS power rail for GPU	ON	OFF	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*	ON
+5VS	System +5VS power rail	ON	ON	OFF	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

Load BOM Option Table

BOM Number	Load BOM Option
431A0H30L02(UMA)	CFL_H@/MP@/CONN@/CMC@/ESPI@/EMI@/ESD@/KB9042@/KXC@/PP_HV@/IN_SPI@/STD@/SW@/SOC_DMIC@/S0IX@/CFL@/UMA@
431A0H30L01(DISCRETE)	CFL_H@/DIS@/MP@/CONN@/CMC@/ESPI@/2G@/AMD_P1_70@/EMI@/ESD@/KB9042@/KXC@/PP_HV@/IN_SPI@/STD@/SW@/SOC_DMIC@/S0IX@/CFL@/VGA@/40W_VGA_EMI@/VGA_EMI@

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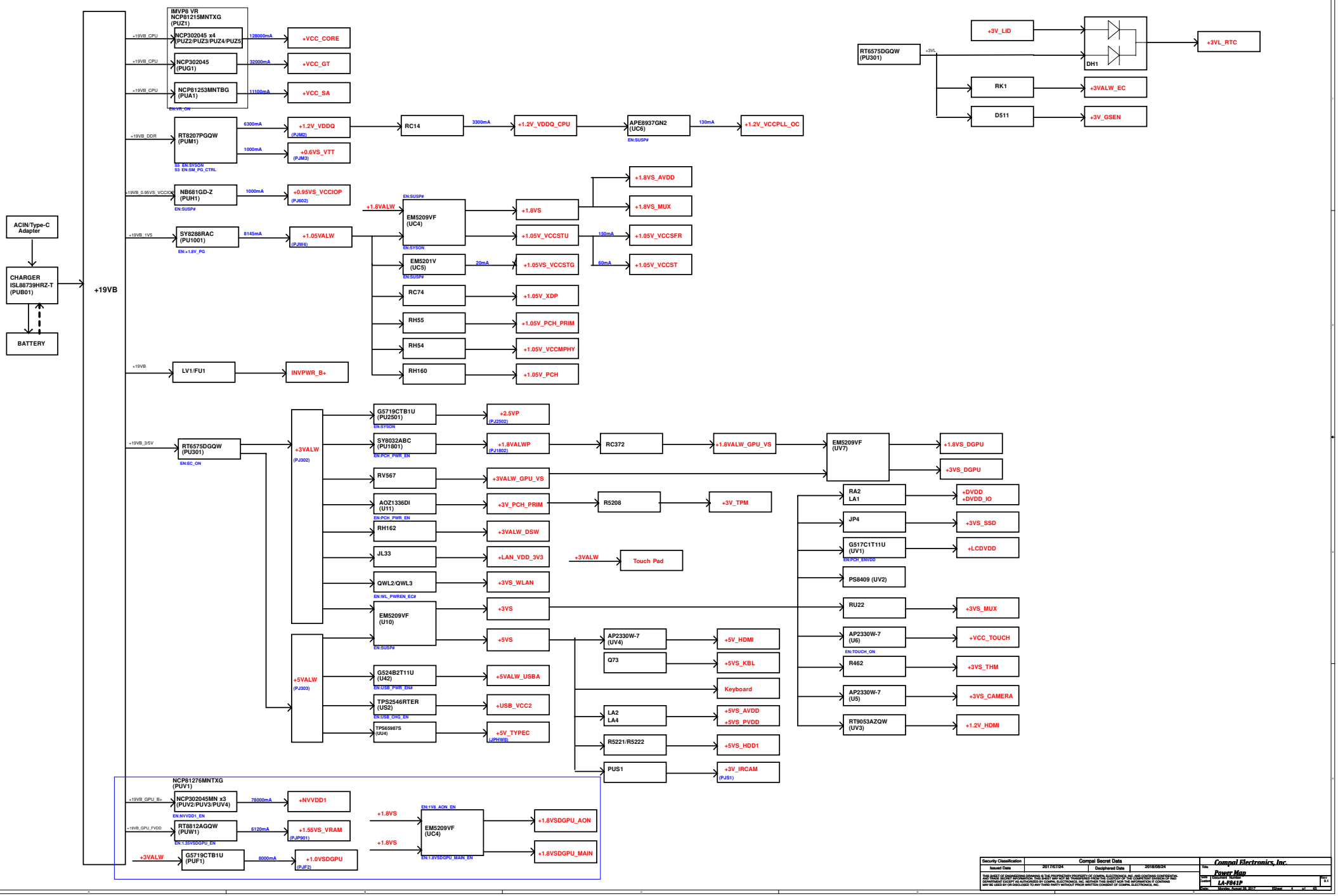
Title: Notes List
Size: Custom | Document Number: LA-F841P | Rev: 0.1
Date: Monday, August 28, 2017 | Sheet 3 of 85



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Title: Power Map

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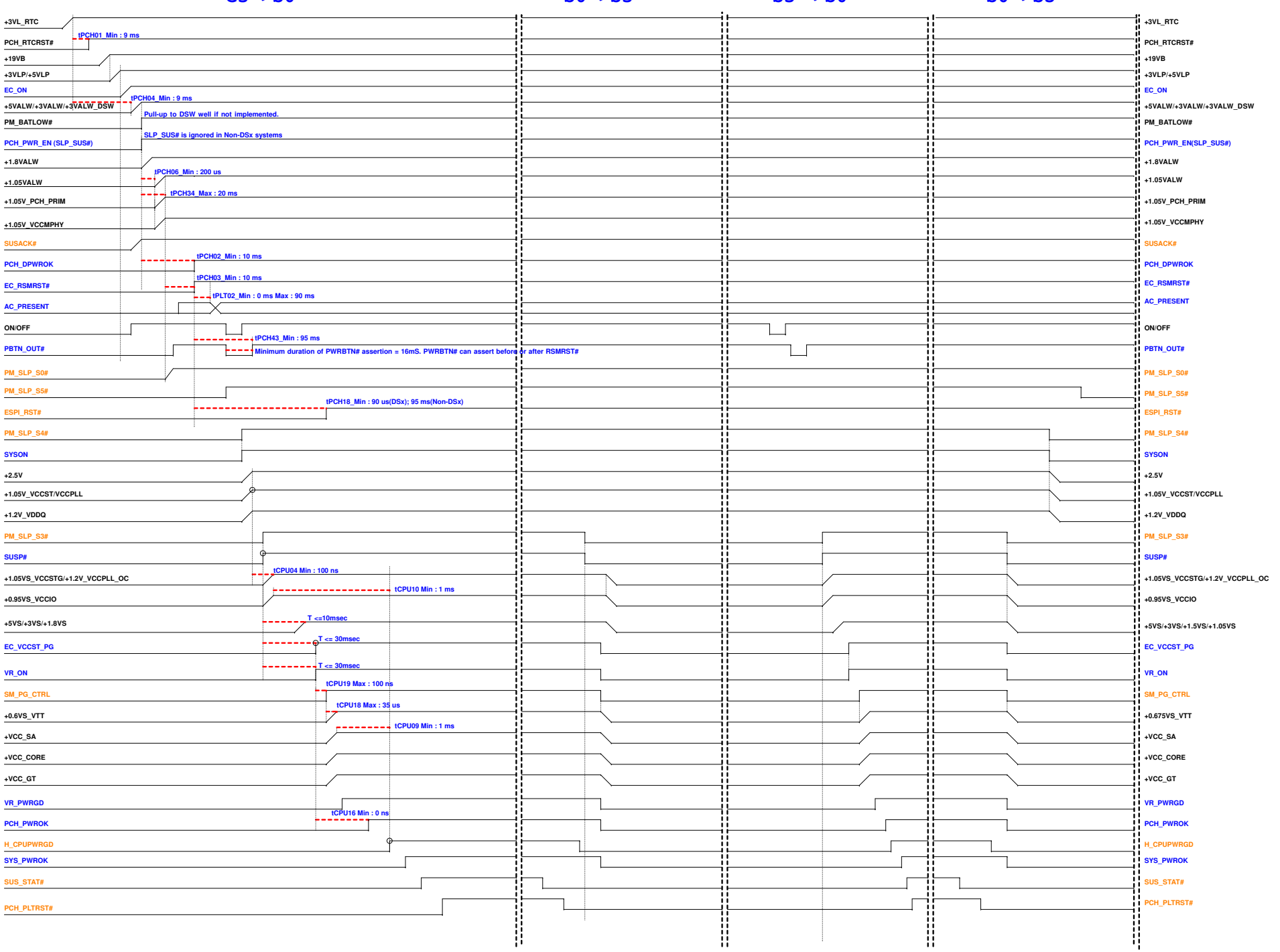
Date: Monday, August 28, 2017 | Sheet 4 of 55

[DDX03 PWR Sequence_CFL-H 6+2_DDR4]



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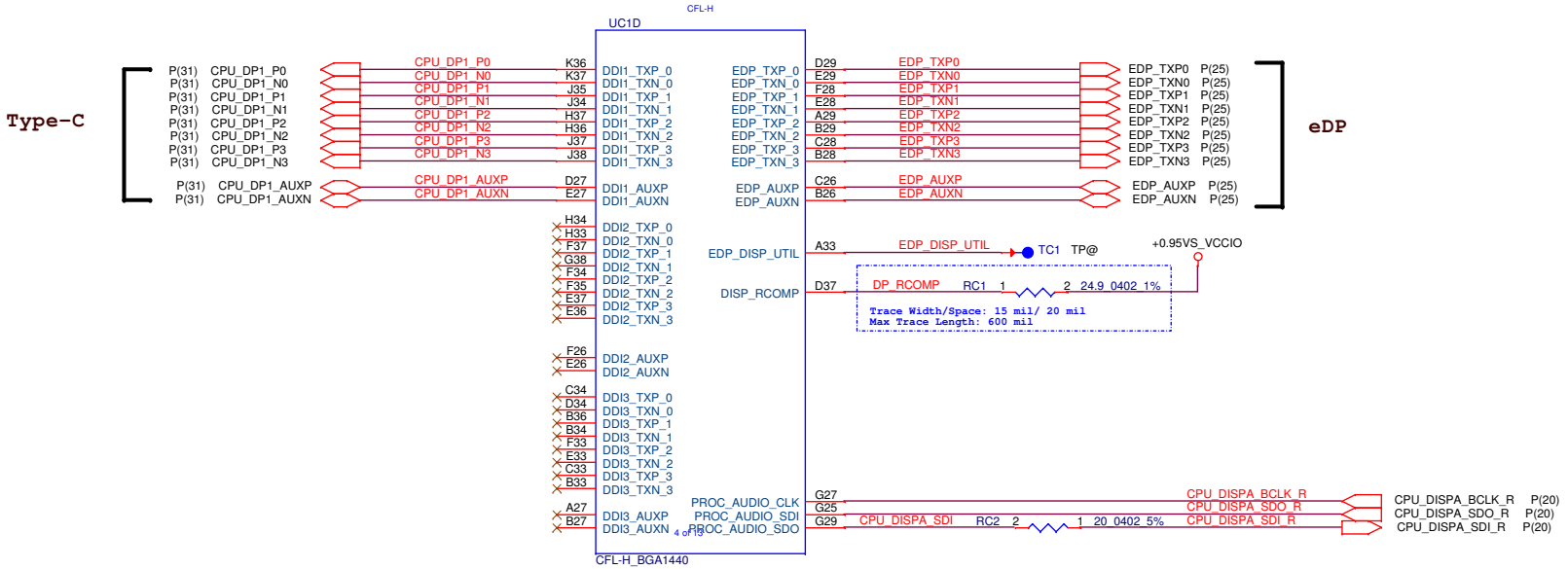
Date: Monday, August 28, 2017 Sheet 5 of 65



Coffee Lake-H CPU SKU

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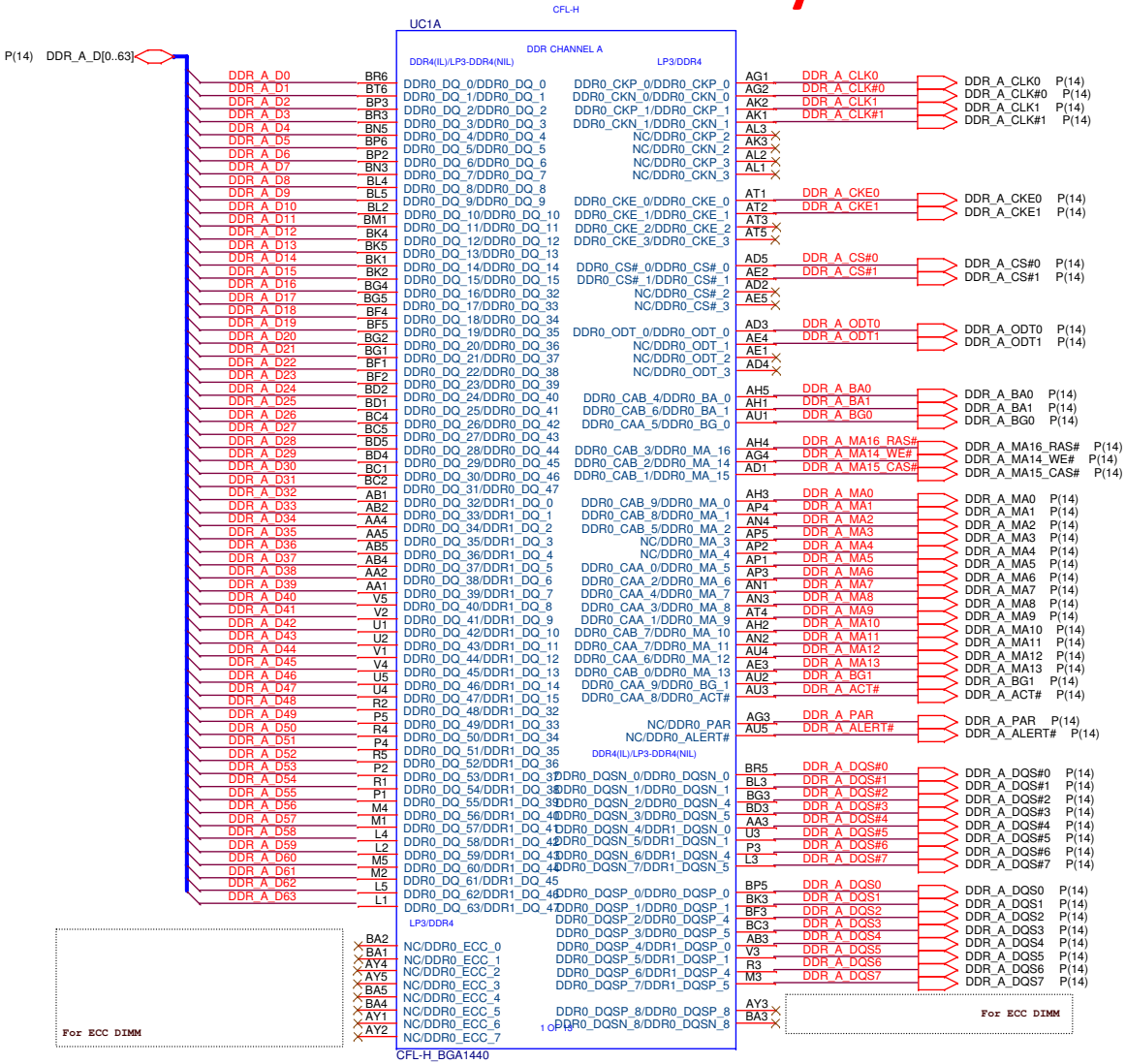
Title: CFL-H(1/8)DDI/eDP			
Size: Custom	Document Number: LA-F841P		Rev: 0.1
Date: Monday, August 28, 2017	Sheet 6 of 65		

CHANNEL-A

Interleaved Memory



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Title: CFL-H(2/8)DIMMA

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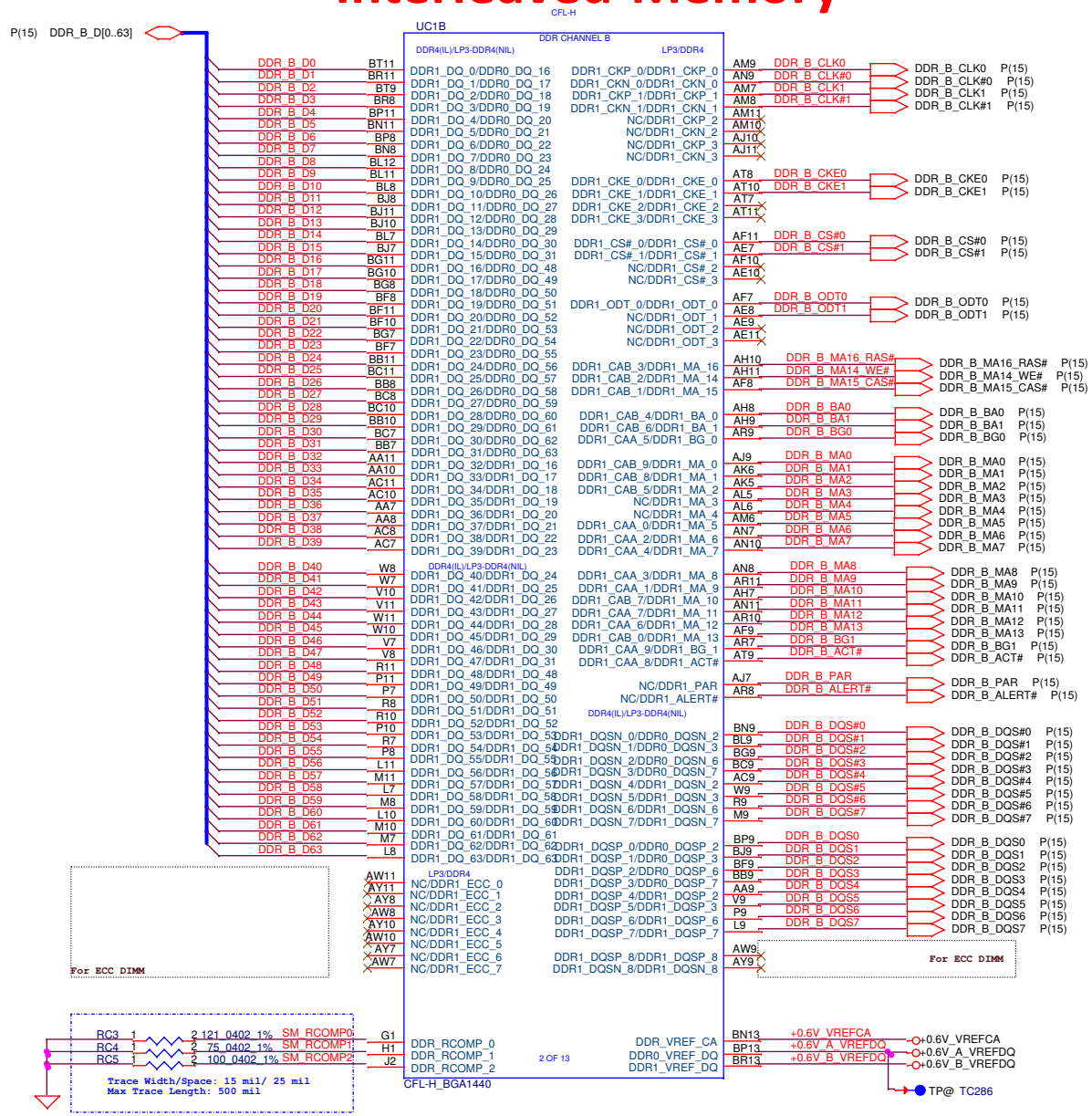
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 7 of 65

CHANNEL-B

Interleaved Memory



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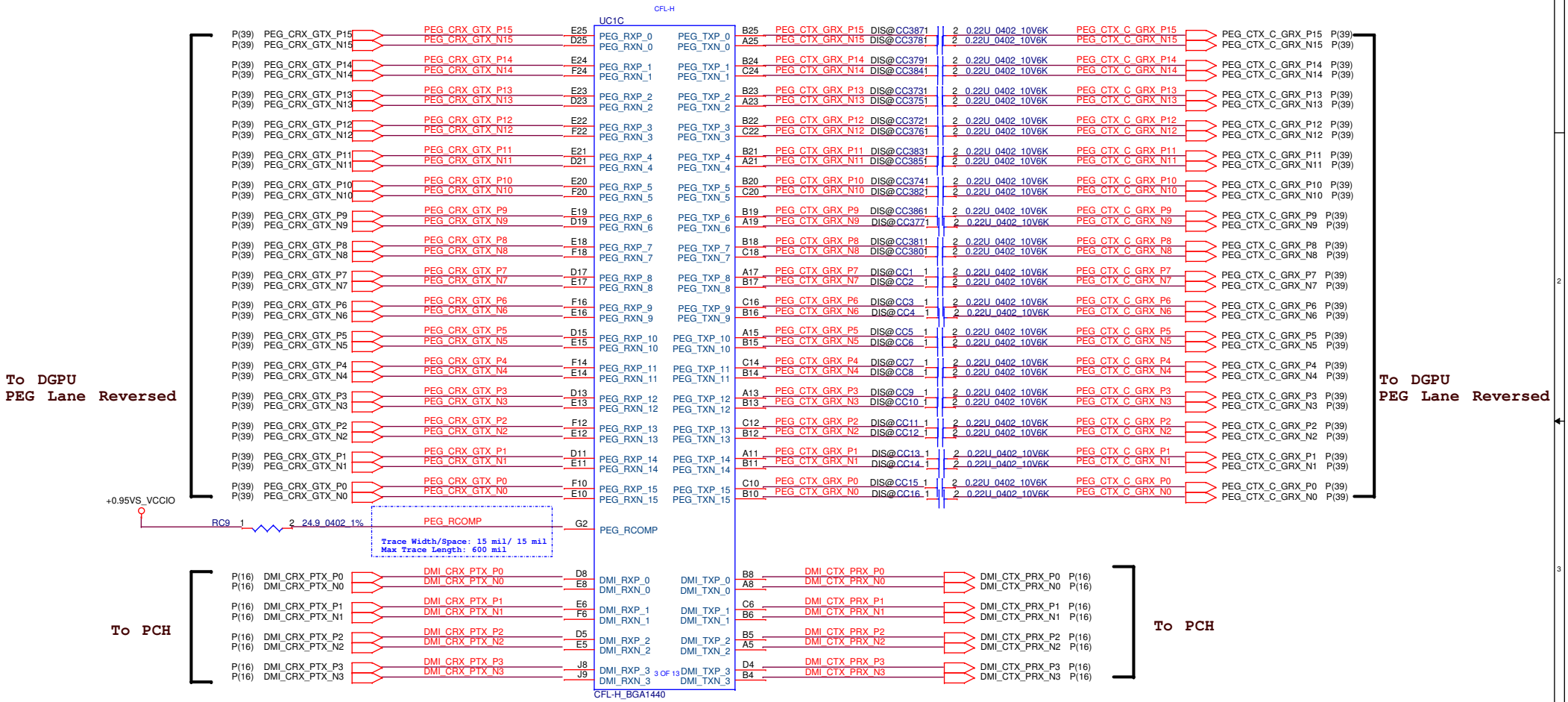
Date: Monday, August 28, 2017	Sheet 8 of 65		



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Title: CFL-H(4/8)PEG

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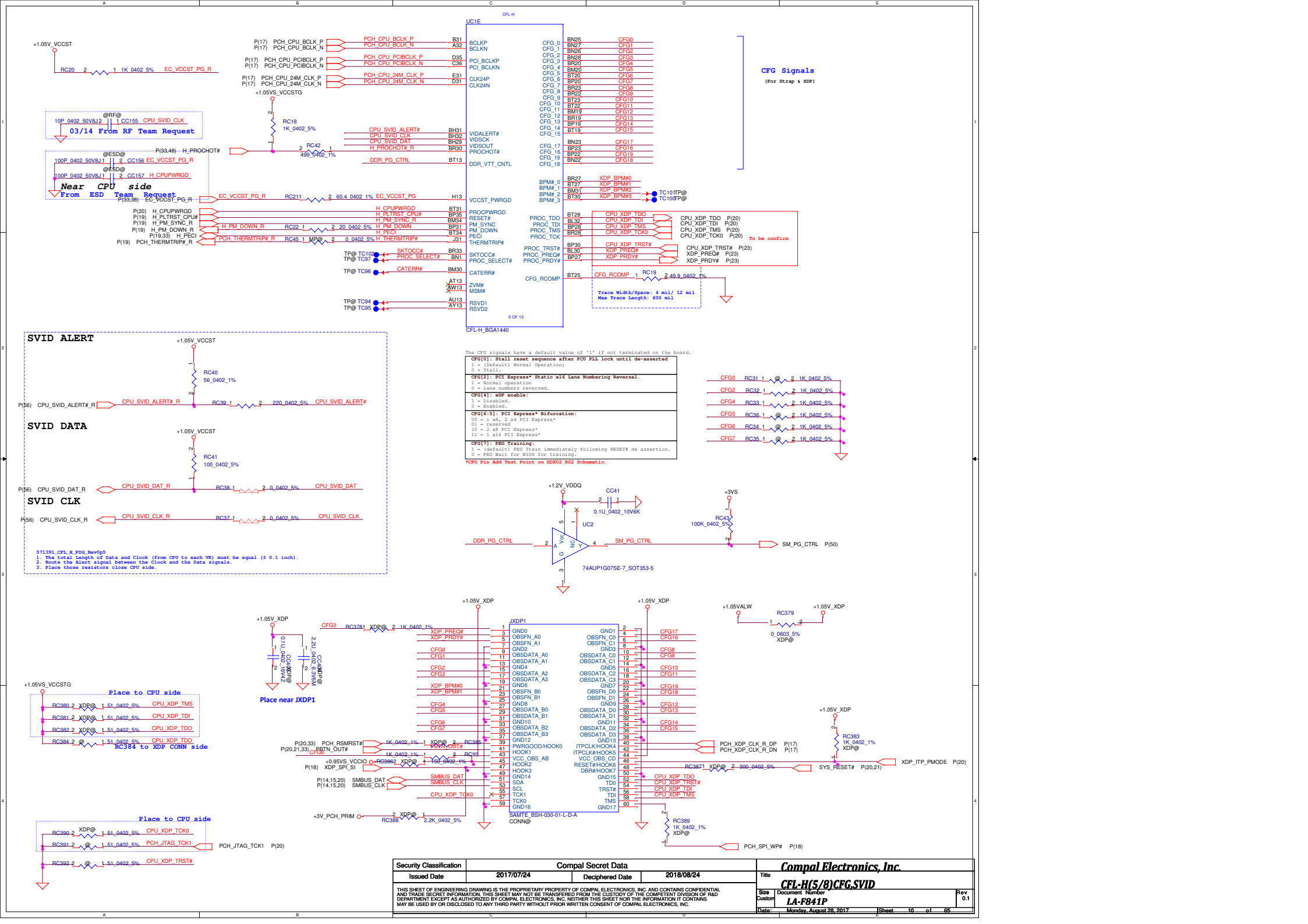
Date: Monday, August 28, 2017 | Sheet 9 of 65



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Title: CFL-H(5/8)CFG,SVID			
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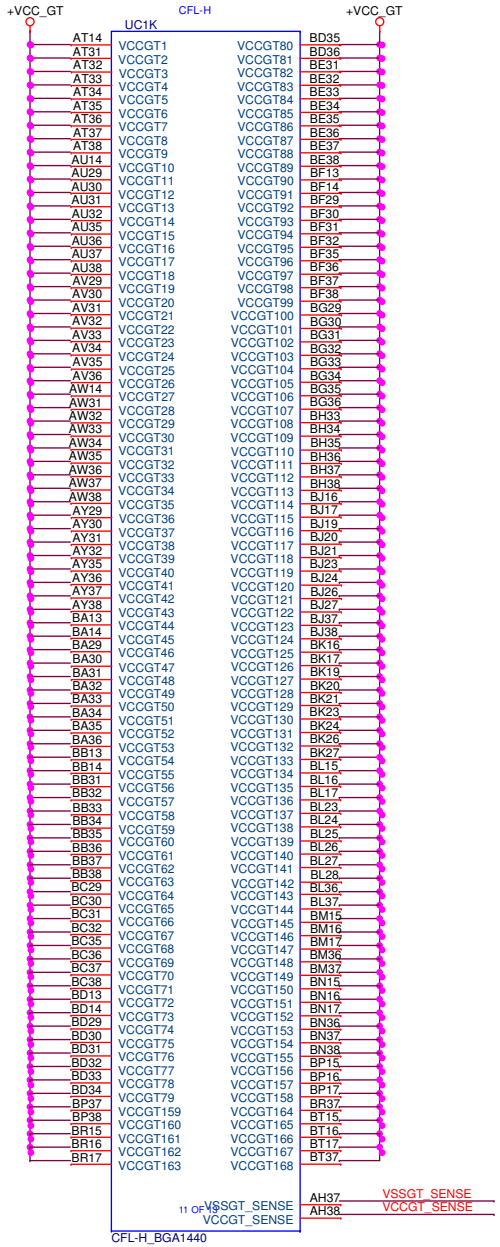
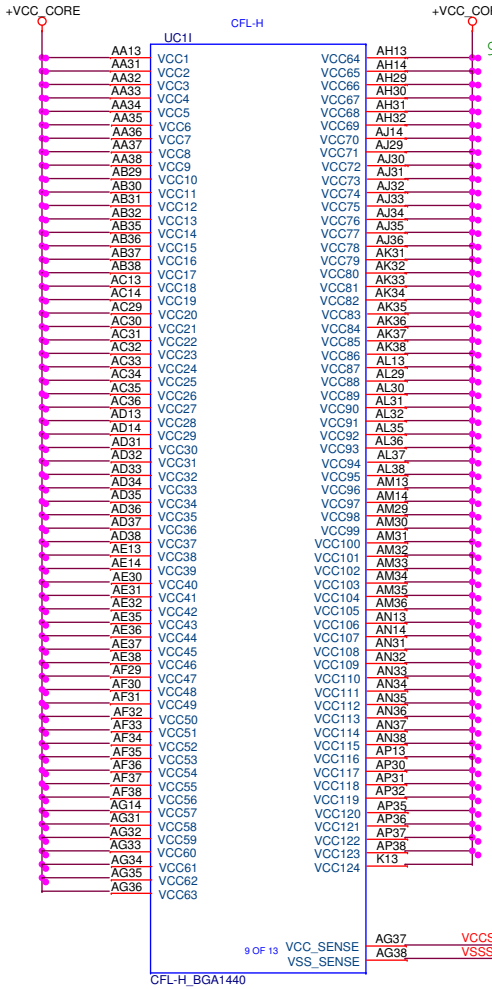
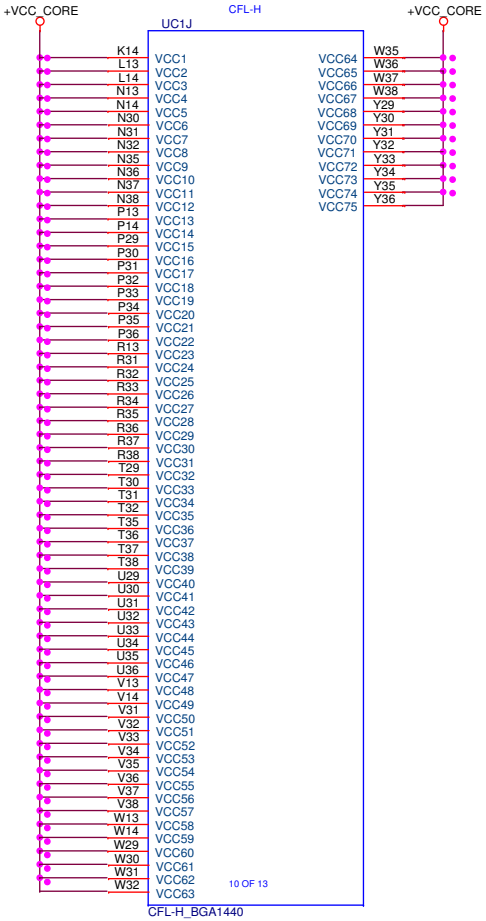
Date: Monday, August 28, 2017	Sheet 10 of 65		

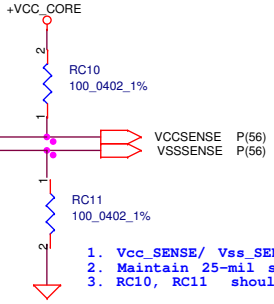
GT
55000mA(Hexa Core GT2)



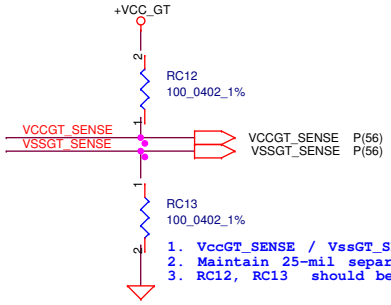


96000mA(Hexa Core GT2)





1. Vcc_SENSE/ Vss_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC10, RC11 should be placed within 2 inches (50.8 mm) of CPU



1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.
3. RC12, RC13 should be placed within 2 inches (50.8 mm) of CPU

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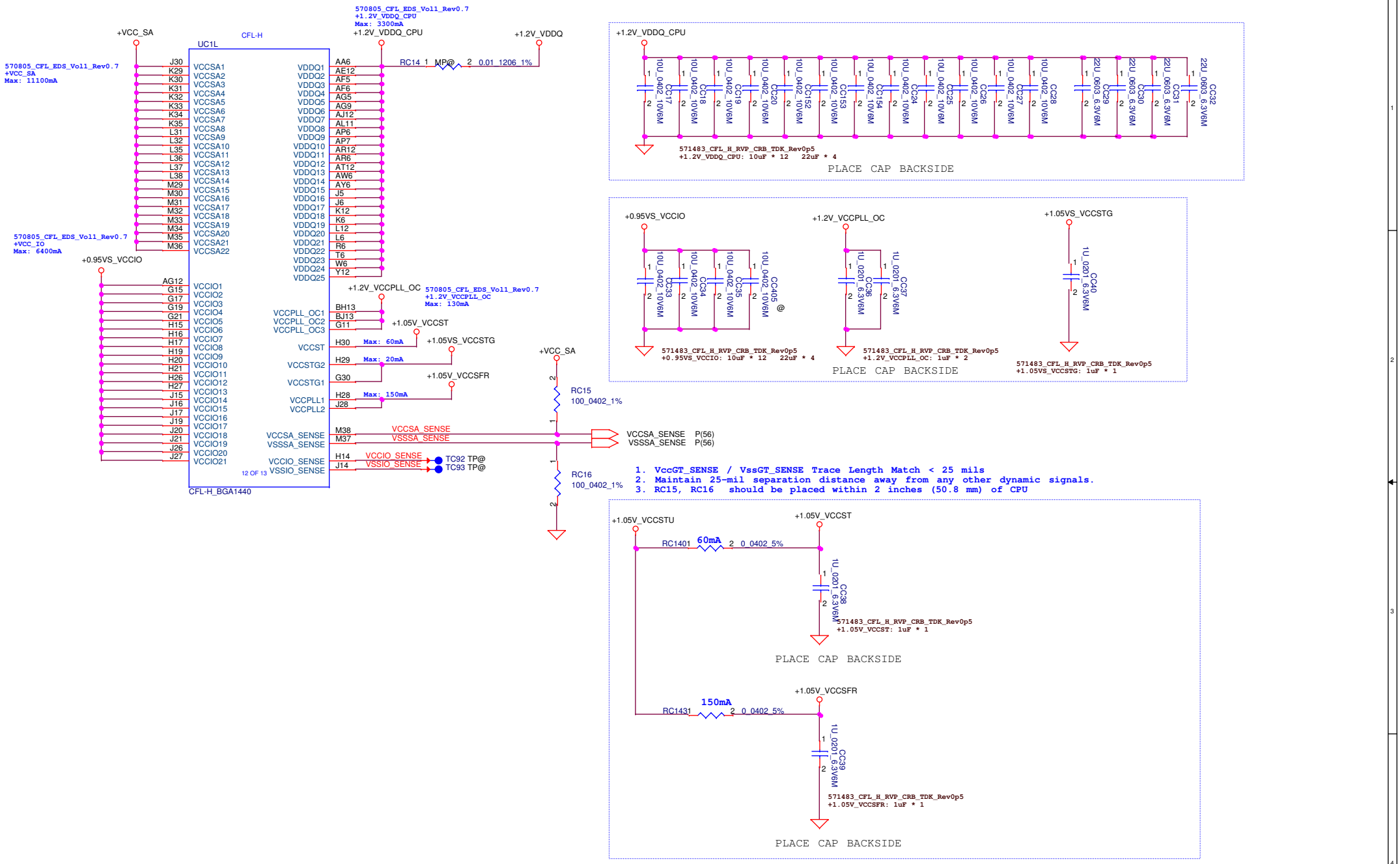
Title: CFL-H(6/8)VCC CORE/GT

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 11 of 65



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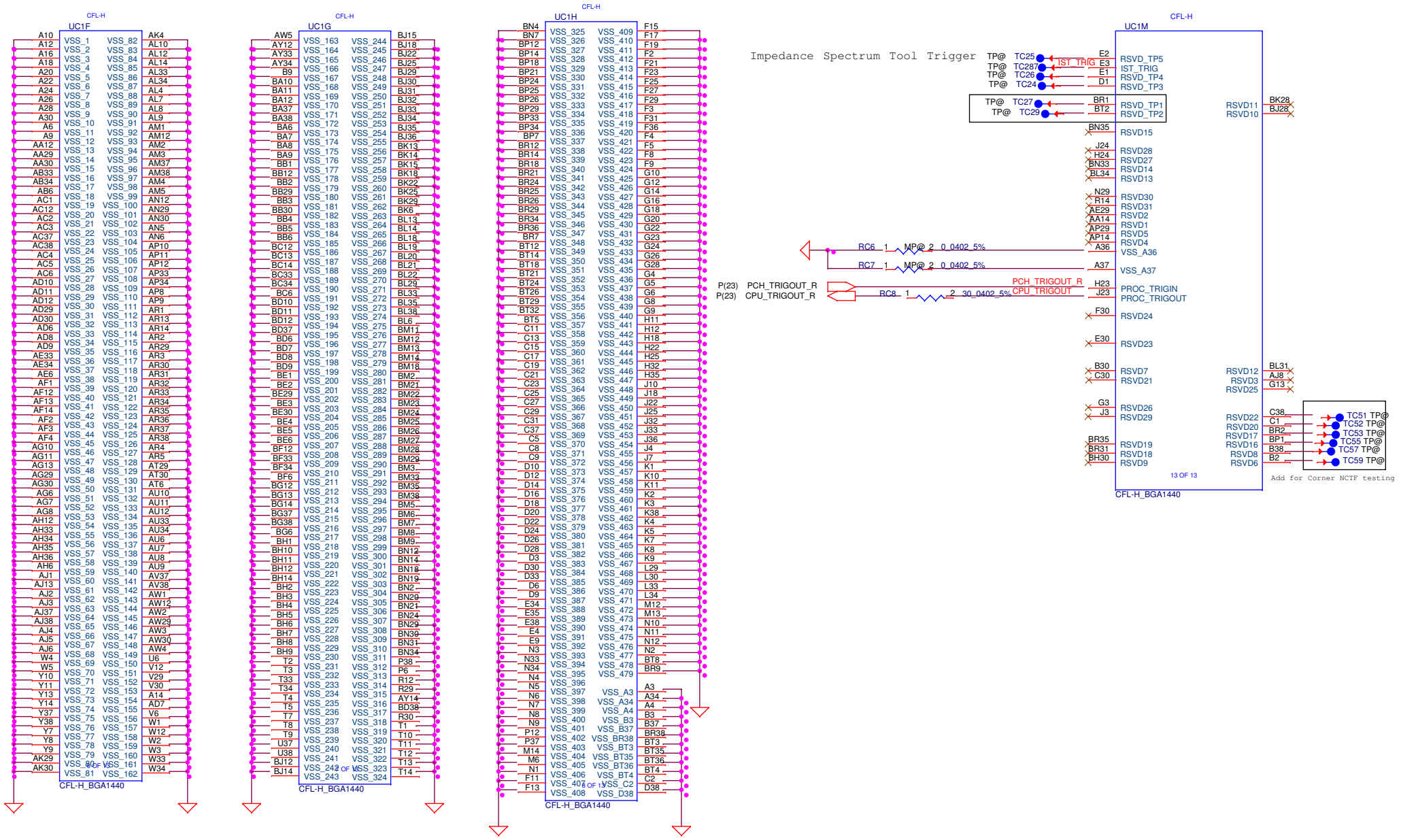
Title: CFL-H(7/8)VCCSA/VCCIO/VDDQ

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 12 of 65



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Issued Date	2017/07/24	Deciphered Date	2018/08/24

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Title: **CFL-H(8/8)GND/RSVD**

Size	Document Number	Rev
Custom	LA-F841P	0.1

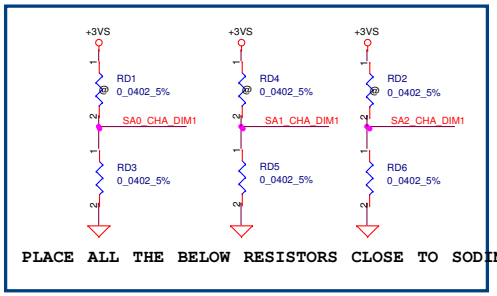
Date: Thursday, August 30, 2018 | Sheet 13 of 65

CHANNEL-A

TOP REVERSE TYPE (4 mm)

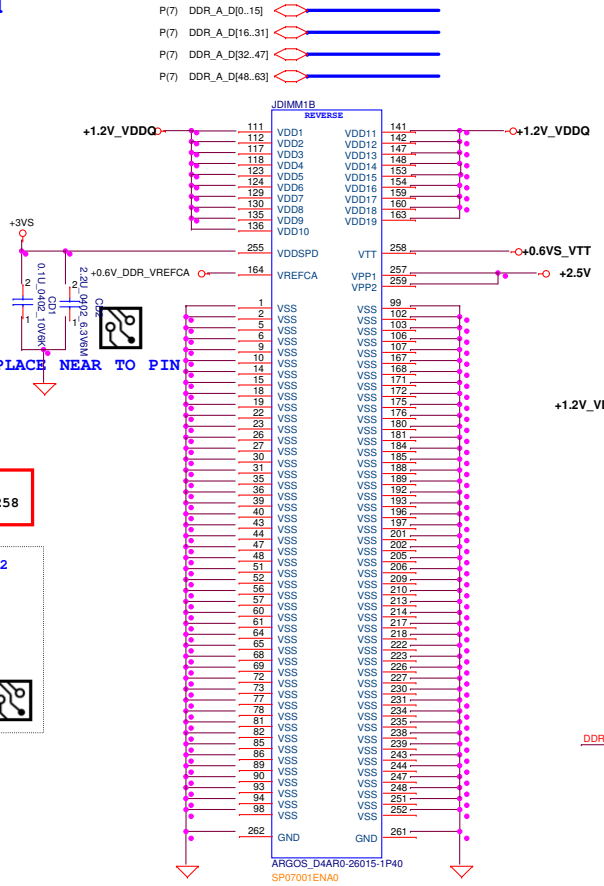
Interleaved Memory

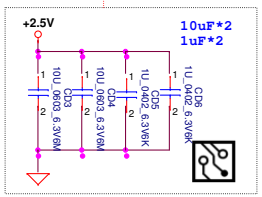
TOP: JDIMM1 CONN Non-ECC DIMM

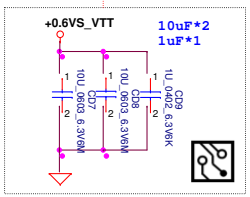


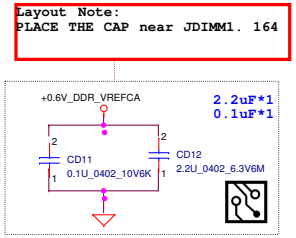
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

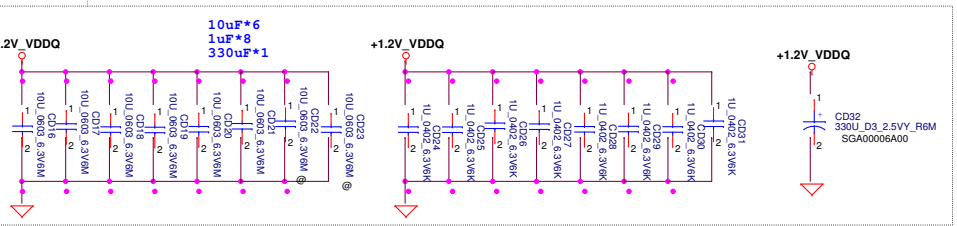
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

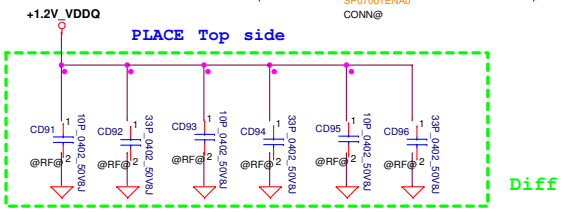


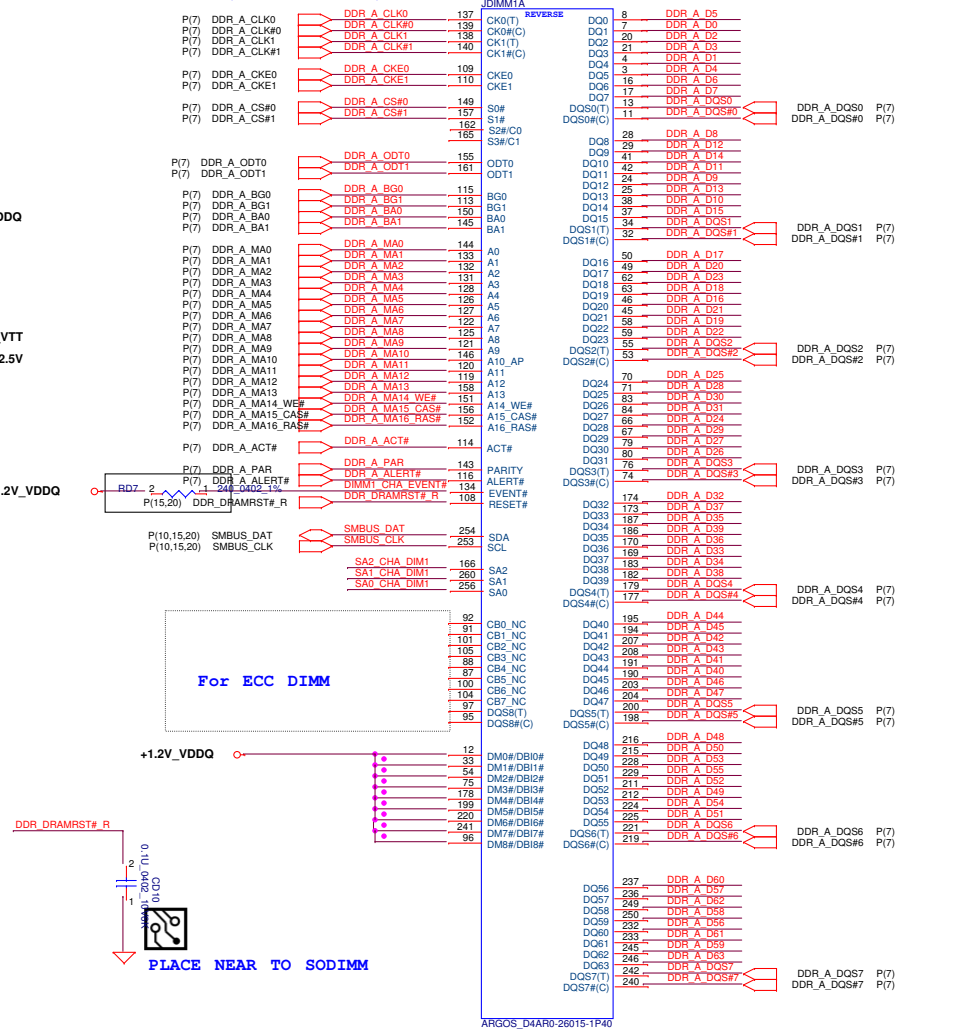


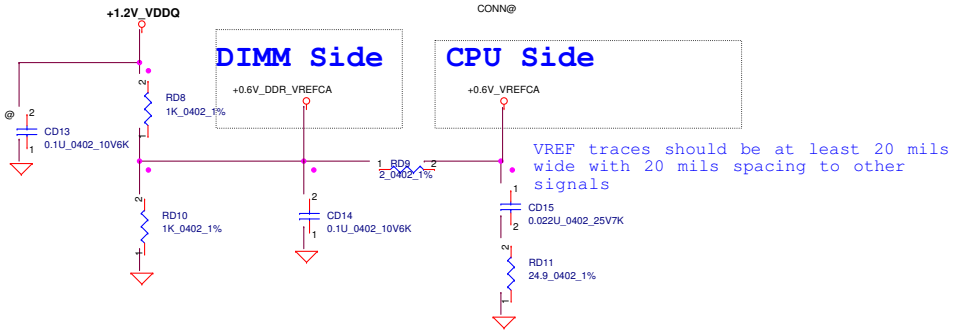










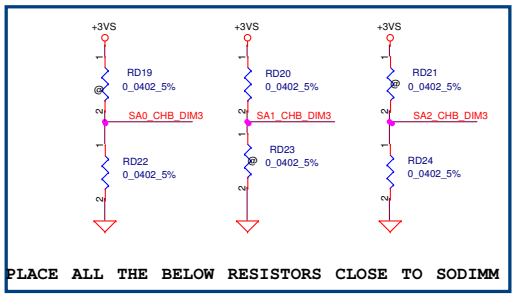


Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.	
Title	DDRIV_CHA: DIMM0
Size	Document Number: LA-F841P
Rev	0.1
Date: Monday, August 28, 2017	Sheet 14 of 65

CHANNEL-B

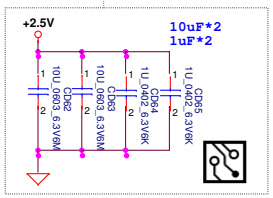
TOP: JDIMM2 CONN Non-ECC DIMM



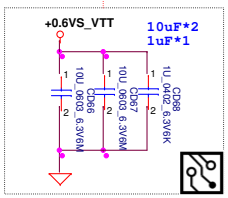
PLACE ALL THE BELOW RESISTORS CLOSE TO SODIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

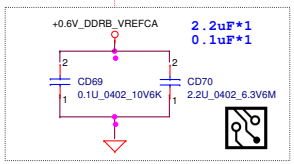
Layout Note:
Place near JDIMM2.257,259



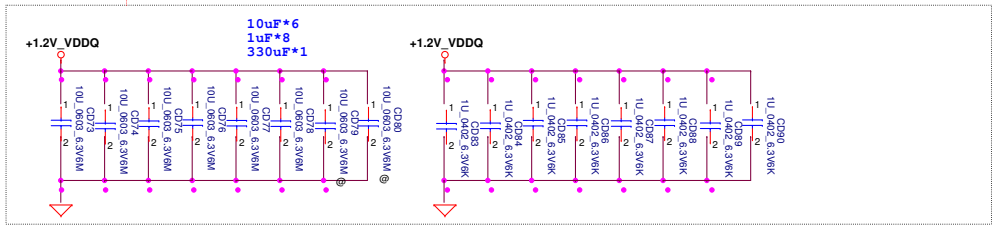
Layout Note:
Place near JDIMM2.258



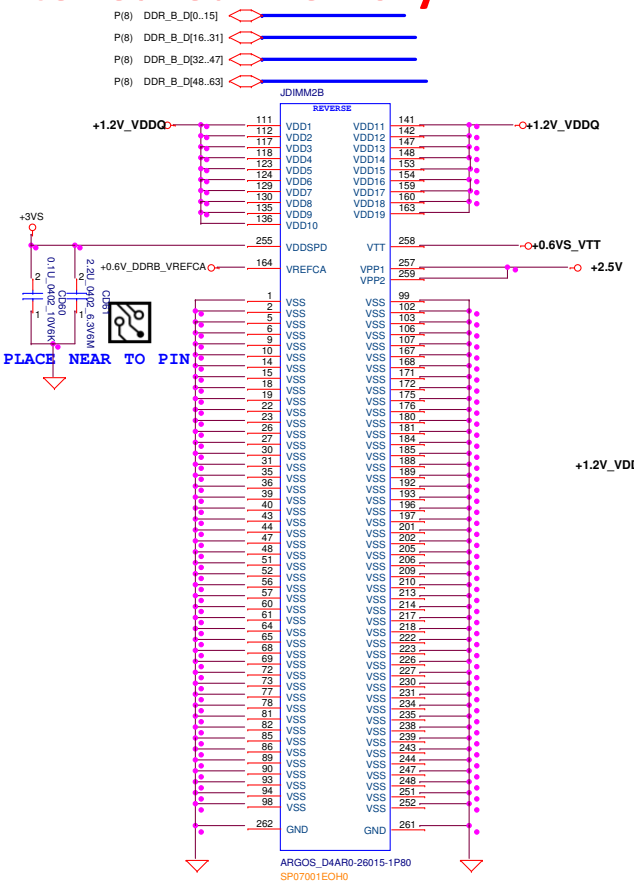
Layout Note:
PLACE THE CAP WITHIN 200 MILS FROM THE JDIMM2



Layout Note:
Place near JDIMM2

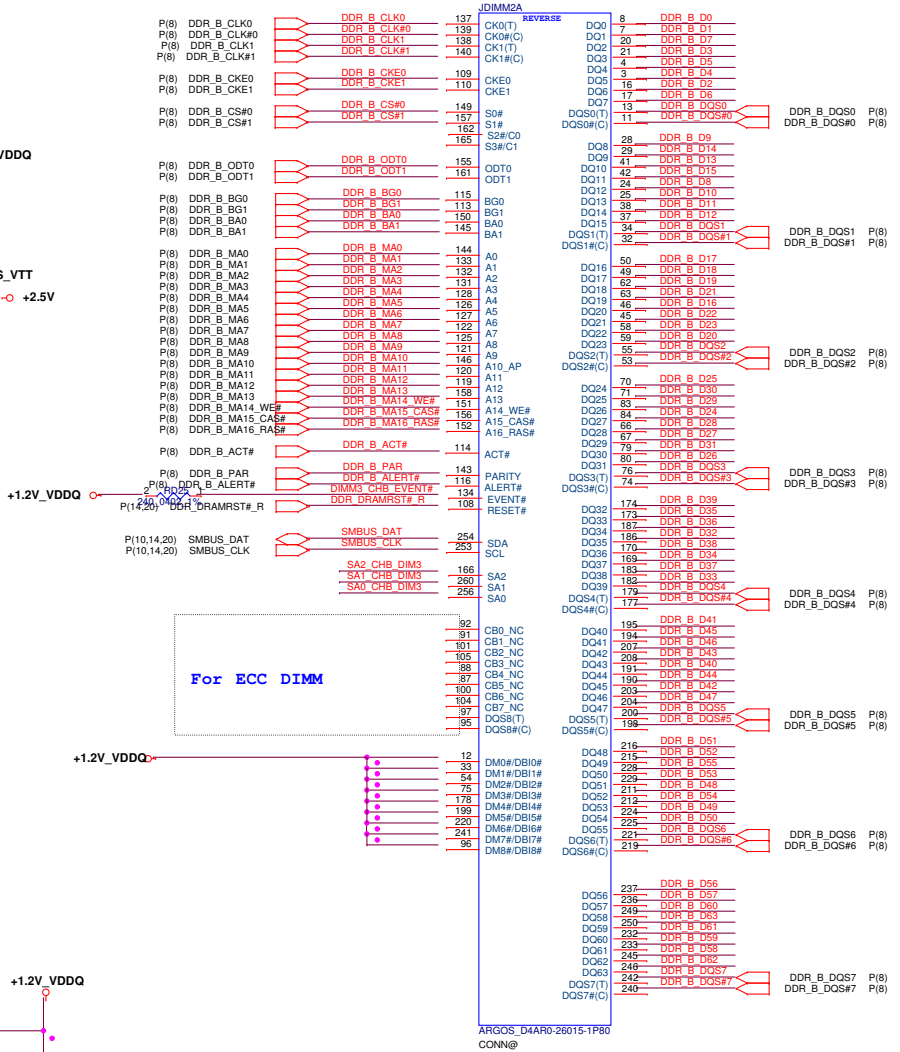


Interleaved Memory

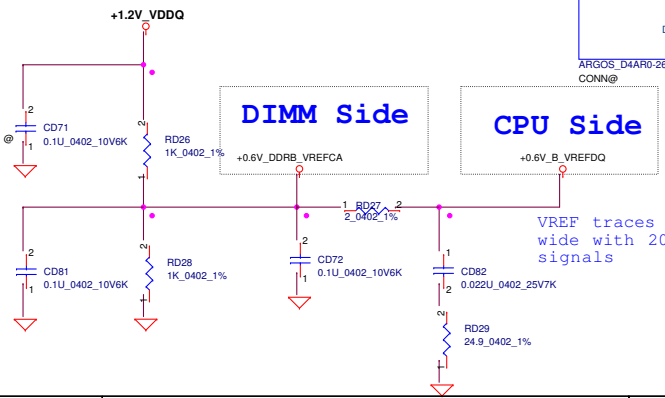


PLACE NEAR TO PIN

TOP Reverse (8 mm)



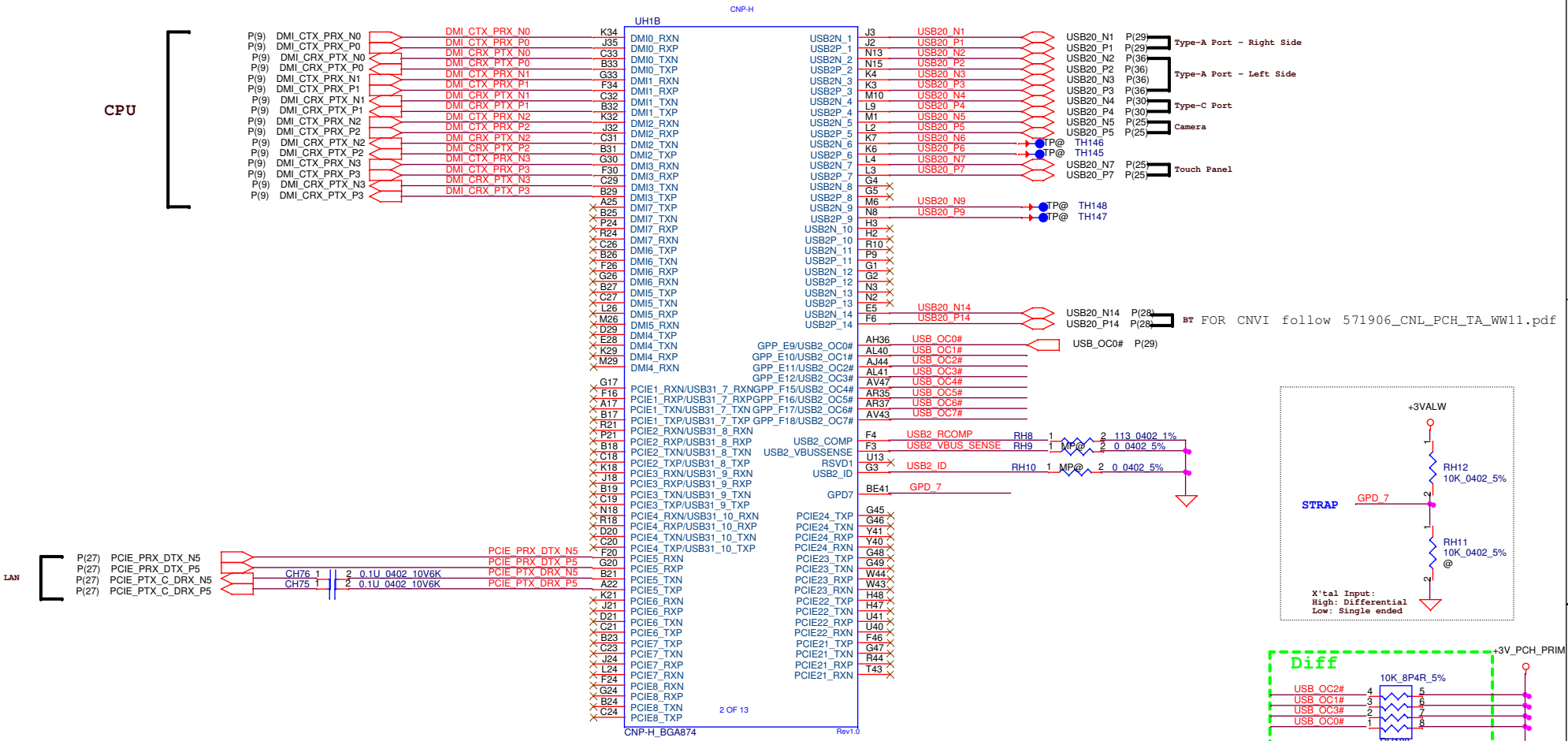
For ECC DIMM



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.			
Title: DDRIV_CHB: DIMM0			
Size	Document Number: LA-F841P		Rev: 0.1
Date: Monday, August 28, 2017		Sheet 15 of 65	



Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7 / PCIe* #1	USB3.1 #8 / PCIe* #2	USB3.1 #9 / PCIe* #3	USB3.1 #10 / PCIe* #4	PCIe* #5 / GbE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9 / GbE	PCIe* #10	PCIe* #11 / SATA 0a	PCIe* #12 / SATA 1a / GbE	PCIe* #13 / SATA 0b / GbE	PCIe* #14 / SATA 1b	PCIe* #15 / SATA 2	PCIe* #16 / SATA 3	PCIe* #17 / SATA 4	PCIe* #18 / SATA 5	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support							No Support				No Support				Yes				No Support				Yes				Yes			

The 30 HSIO lanes on PCH-H supports the following configurations:
1. Up to 24 PCIe* Lanes
– A maximum of 16 PCIe* Ports (or devices) can be enabled
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
Max PCIe* Ports (or devices) = 16 – GbE (0 or 1)
– PCIe* Lanes 1–4 (PCIe* Controller #1), 5–8 (PCIe* Controller #2), 9–12 (PCIe* Controller #3), 13–16 (PCIe* Controller #4), 17–20 (PCIe* Controller #5), and 21–24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA Lanes
– A maximum of 6 SATA Ports (or devices) can be enabled
– SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
– SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 USB 3.1 Lanes
– A maximum of 10 USB 3.1 Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
– A maximum of 1 GbE Port (or device) can be enabled
5. Supports up to 3 Remapped (IntelR Rapid Storage Technology) PCIe* storage devices
– x2 and x4 PCIe* NVMe SSD
– x2 IntelR Optane? Memory Device
– See the " PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers,configuration , and lanes that can be used for IntelR Rapid Storage Technology PCIe* storage support

6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the IntelR Flash Image Tool (FIT) tool.

Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: PCH(1/8)DMI/PCIE/USB2

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 16 of 65

PCH-H XTAL_IN/OUT POR is 24MHz for 571697_CNL_MOW_WW16_2017.pdf

XTAL_24M_PCH_OUT
XTAL_24M_PCH_IN
RH16 1 2 1M_0402_5%
YH1 SJ10000T500
24MHZ_12PF_7M24090001
GND GND
CH4 15P_0402_50V8J
CH5 15P_0402_50V8J

PCH_RTCX1
PCH_RTCX2
RH19 1 2 10M_0402_5%
YH2
32.768KHZ_9PF_X1A000141000200
CH6 8P_0402_50V8D
CH7 8P_0402_50V8D
Trace Space: 15 mil
Max Trace Length: 1000 mil

+3VS
RH157 1 2 10K_0402_5% CLKREQ_PCIE#5
RPH3 10K_0804_8P4R_5%
8 CLKREQ_PCIE#1
7 CLKREQ_PCIE#3
6 CLKREQ_PCIE#4
5 CLKREQ_PCIE#2
Diff

For DDX03 R02

+1.8V_PRIM XTAL Frequency Select
RH26 1 2 4.7K_0402_5% CNV_BRI_PTX_DRX STRAP
This signal has a weak internal pull-down.
0 = 38.4/19.2MHz XTAL frequency selected.
1 = 24MHz XTAL frequency selected. (DDX03)
Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well.

+1.8V_PRIM
RH93 2 @ 1 4.7K_0402_5% GPP_J9 STRAP
The signal has a weak internal pull-down
0 = VCCPSPI is connected to 3.3V rail
1 = VCCPSPI is connected to 1.8V rail
Note: If VCCPSPI is connected to 1.8V rail, this pin strap must be a '1' for the proper functionality of the SPI (Flash) I/Os

+1.8V_PRIM M.2 CNV Mode Select
RH167 2 1 20K_0402_5% CNV_RGI_PTX_DRX STRAP
RH168 2 @ 1 100K_0402_5%
An external pull-up or pull-down is required.
0 = Integrated CNVi enable.
1 = Integrated CNVi disable.
Pulled down by CRF CNVi RGI_DT pin

CNP-H
UH1G
TH74 TP@ BE33 GPP_A16/CLKOUT_48

P(10) PCH_CPU_24M_CLK_P → PCH_CPU_24M_CLK_P D7 CLKOUT_CPUNSSC_P
P(10) PCH_CPU_24M_CLK_N → PCH_CPU_24M_CLK_N C6 CLKOUT_CPUNSSC#
CLKOUT_ITPXDP# Y3 PCH_XDP_CLK_R_DN → PCH_XDP_CLK_R_DN P(10)
CLKOUT_ITPXDP_P Y4 PCH_XDP_CLK_R_DP → PCH_XDP_CLK_R_DP P(10)

P(10) PCH_CPU_BCLK_P → PCH_CPU_BCLK_P B8 CLKOUT_CPUBCLK_P
P(10) PCH_CPU_BCLK_N → PCH_CPU_BCLK_N C8 CLKOUT_CPUBCLK#
CLKOUT_PCIBCLK# B6 PCH_CPU_PCIBCLK_N → PCH_CPU_PCIBCLK_N P(10)
CLKOUT_PCIBCLK_P A6 PCH_CPU_PCIBCLK_P → PCH_CPU_PCIBCLK_P P(10)

XTAL_24M_PCH_OUT RH17 1 2 33_0402_5% XTAL_24M_PCH_OUT_R U9 XTAL_OUT
XTAL_24M_PCH_IN RH18 1 2 33_0402_5% XTAL_24M_PCH_IN_R U10 XTAL_IN
CLKOUT_PCIE_N0 AJ6
CLKOUT_PCIE_P0 AJ7

RH20 1 2 60.4_0402_1% XCLK_BIASREF T3 XCLK_BIASREF
XCLK_BIASREF
Trace Width/Space: 15mil /15 mil
Max Trace Length: 1000 mil

PCH_RTCX1 BA49 RTCX1
PCH_RTCX2 BA48 RTCX2

CLKOUT_PCIE_N1 AH9 CLK_PCIE_N1 → CLK_PCIE_N1 P(28)
CLKOUT_PCIE_P1 AH10 CLK_PCIE_P1 → CLK_PCIE_P1 P(28) WLAN (ON BOARD)
CLKOUT_PCIE_N2 AE14 CLK_PCIE_N2 → CLK_PCIE_N2 P(24)
CLKOUT_PCIE_P2 AE15 CLK_PCIE_P2 → CLK_PCIE_P2 P(24) NGFF SSD(KEY M)
CLKOUT_PCIE_N3 AE6 CLK_PCIE_N3 → CLK_PCIE_N3 P(36)
CLKOUT_PCIE_P3 AE7 CLK_PCIE_P3 → CLK_PCIE_P3 P(36) Card Reader
CLKOUT_PCIE_N4 AC2 CLK_PEG_GPU_N4 → CLK_PEG_GPU_N4 P(39)
CLKOUT_PCIE_P4 AC3 CLK_PEG_GPU_P4 → CLK_PEG_GPU_P4 P(39) GPU
CLKOUT_PCIE_N5 AB2 CLK_PCIE_N5 → CLK_PCIE_N5 P(27)
CLKOUT_PCIE_P5 AB3 CLK_PCIE_P5 → CLK_PCIE_P5 P(27) LAN
CLKOUT_PCIE_N6 W4
CLKOUT_PCIE_P6 W3
CLKOUT_PCIE_N7 W7
CLKOUT_PCIE_P7 W6
CLKOUT_PCIE_N8 AC14
CLKOUT_PCIE_P8 AC15
CLKOUT_PCIE_N9 U2
CLKOUT_PCIE_P9 U3
CLKOUT_PCIE_N10 AC9
CLKOUT_PCIE_P10 AC11
CLKOUT_PCIE_N11 AE9
CLKOUT_PCIE_P11 AE11
CLKIN_XTAL R6 REFCLK_CNV → REFCLK_CNV P(28)

Thunderbolt
WLAN (NGFF) P(28) CLKREQ_PCIE#1 → BF31 GPP_B5/SRCCLKREQ0#
NGFF SSD(KEY M) P(24) CLKREQ_PCIE#2 → BE31 GPP_B6/SRCCLKREQ1#
Card Reader P(36) CLKREQ_PCIE#3 → AR32 GPP_B7/SRCCLKREQ2#
GPU P(39) CLKREQ_PCIE#4 → BB30 GPP_B8/SRCCLKREQ3#
LAN P(27) CLKREQ_PCIE#5 → BA30 GPP_B9/SRCCLKREQ4#
AN29 GPP_B10/SRCCLKREQ5#
AE47 GPP_H0/SRCCLKREQ6#
AC48 GPP_H1/SRCCLKREQ7#
AE41 GPP_H2/SRCCLKREQ8#
AF48 GPP_H3/SRCCLKREQ9#
AC41 GPP_H4/SRCCLKREQ10#
AC39 GPP_H5/SRCCLKREQ11#
AE39 GPP_H6/SRCCLKREQ12#
AB48 GPP_H7/SRCCLKREQ13#
AC44 GPP_H8/SRCCLKREQ14#
AC43 GPP_H9/SRCCLKREQ15#

7 OF 13
CNP-H_BGA874 Rev1.0

+3V_PCH_PRIM
RH178 100K_0402_5%
RH173 10K_0402_5%

CNP-H
UH1M
P(35) TPM_IRQ# → TPM_IRQ# AW13 GPP_G0/SD_CMD
BE9 GPP_G1/SD_DATA0
BF8 GPP_G2/SD_DATA1
BF9 GPP_G3/SD_DATA2
BG8 GPP_G4/SD_DATA3
BE8 GPP_G5/SD_CD#
BD8 GPP_G6/SD_CLK
AV13 GPP_G7/SD_WP

AP3 GPP_I11/M2_SKT2_CFG0
AP2 GPP_I12/M2_SKT2_CFG1
AN4 GPP_I13/M2_SKT2_CFG2
AM7 GPP_I14/M2_SKT2_CFG3

No support S0ix
TH4968TP@ TH135 TP@ TH4969TP@ → CPU_C10_GATE# AV6 GPP_J0/CNV_PA_BLANKING
AY3 GPP_J1/CPU_C10_GATE#
AR13 GPP_J11/A4WP_PRESENT
AV7 GPP_J10
AW3 GPP_J_2
AT10 GPP_J_3
AV4 GPP_J4/CNV_BRI_DT/UART0B_RTS#
AY2 GPP_J5/CNV_BRI_RSP/UART0B_RXD
BA4 GPP_J6/CNV_RGI_DT/UART0B_TXD
AV3 GPP_J7/CNV_RGI_RSP/UART0B_CTS#
AW2 GPP_J8/CNV_MFUART2_RXD
AU9 GPP_J9/CNV_MFUART2_TXD

P(28) CNV_BRI_PTX_DRX → CNV_BRI_PTX_DRX
P(28) CNV_BRI_PRX_DTX → CNV_BRI_PRX_DTX
P(28) CNV_RGI_PTX_DRX → CNV_RGI_PTX_DRX
P(28) CNV_RGI_PRX_DTX → CNV_RGI_PRX_DTX
GPP_J9

3.3V
1.8V

CNV_WR_CLKN BD4 CLK_CNV_PRX_DTX_N → CLK_CNV_PRX_DTX_N P(28)
CNV_WR_CLKP BE3 CLK_CNV_PRX_DTX_P → CLK_CNV_PRX_DTX_P P(28)
CNV_WR_D0N BB3 CNV_PRX_DTX_N0 → CNV_PRX_DTX_N0 P(28)
CNV_WR_D0P BB4 CNV_PRX_DTX_P0 → CNV_PRX_DTX_P0 P(28)
CNV_WR_D1N BA3 CNV_PRX_DTX_N1 → CNV_PRX_DTX_N1 P(28)
CNV_WR_D1P BA2 CNV_PRX_DTX_P1 → CNV_PRX_DTX_P1 P(28)
CNV_WT_CLKN BC5 CLK_CNV_PTX_DRX_N → CLK_CNV_PTX_DRX_N P(28)
CNV_WT_CLKP BB6 CLK_CNV_PTX_DRX_P → CLK_CNV_PTX_DRX_P P(28)
CNV_WT_D0N BE6 CNV_PTX_DRX_N0 → CNV_PTX_DRX_N0 P(28)
CNV_WT_D0P BD7 CNV_PTX_DRX_P0 → CNV_PTX_DRX_P0 P(28)
CNV_WT_D1N BG6 CNV_PTX_DRX_N1 → CNV_PTX_DRX_N1 P(28)
CNV_WT_D1P BF6 CNV_PTX_DRX_P1 → CNV_PTX_DRX_P1 P(28)
CNV_WT_RCOMP BA1 CNV_WT_RCOMP RH25 1 2 150_0402_1%
PCIE_RCOMPN B12 PCIE_RCOMPN RH21 1 2 100_0402_1%
PCIE_RCOMPP A13 PCIE_RCOMPP
SD_1P8_RCOMP BE5 SD_RCOMP_1P8 RH22 1 2 200_0402_1%
SD_3P3_RCOMP BE4 SD_RCOMP_3P3 RH23 1 2 200_0402_1%
GPPJ_RCOMP_1P81 BD1
GPPJ_RCOMP_1P82 BE1 GPPJ_RCOMP_1P8 RH24 1 2 200_0402_1%
GPPJ_RCOMP_1P83 BE2
RSVD2 Y35
RSVD3 Y36
RSVD1 BC1
TP AL35 TP@ TH101
#571483_CFL_H_RVP_CRB_TDK_Rev0p5
Recommend external test point

13 OF 13
CNP-H_BGA874 Rev1.0

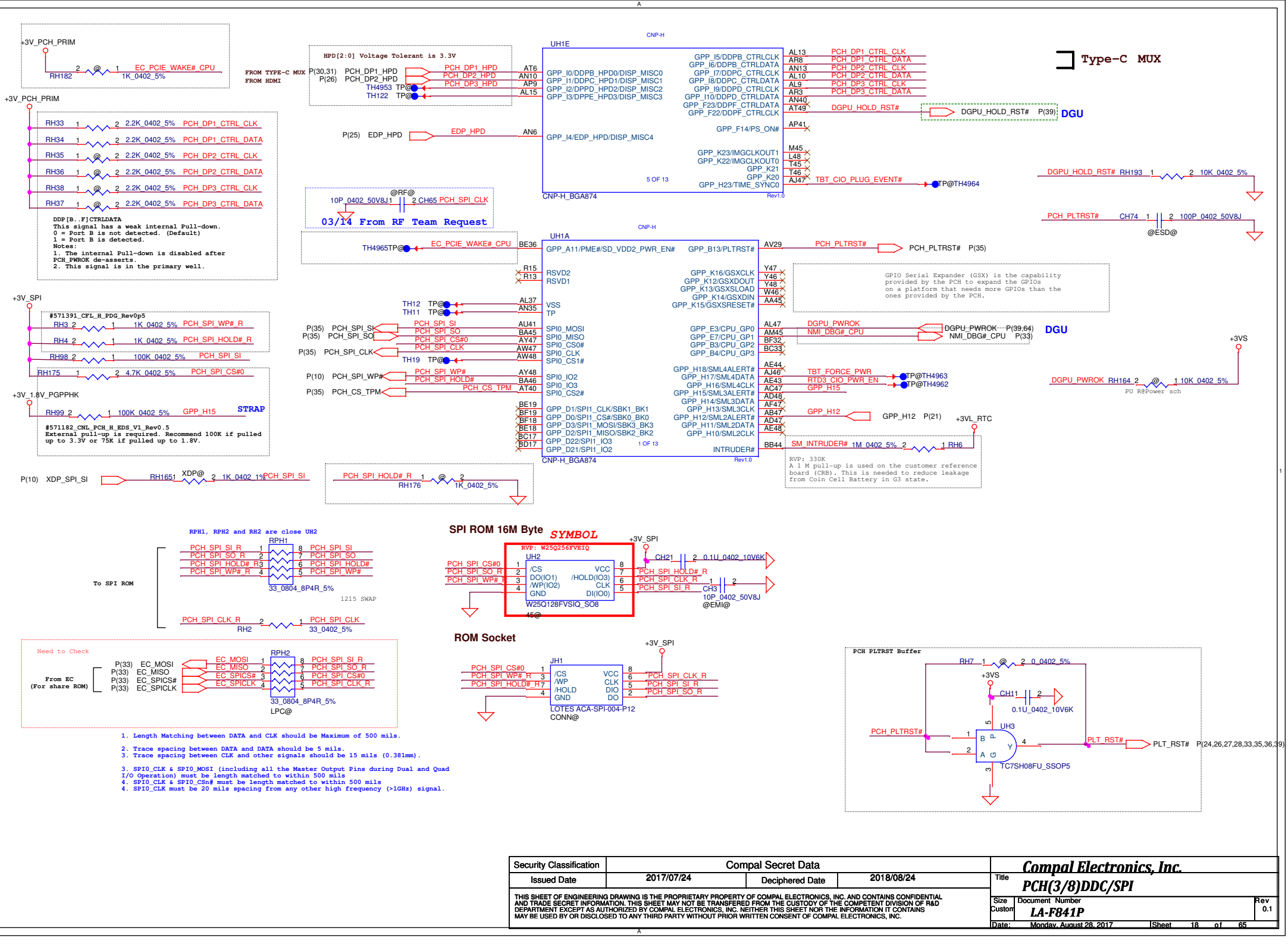
Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: PCH(2/8)CLK/CNVI

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 17 of 65



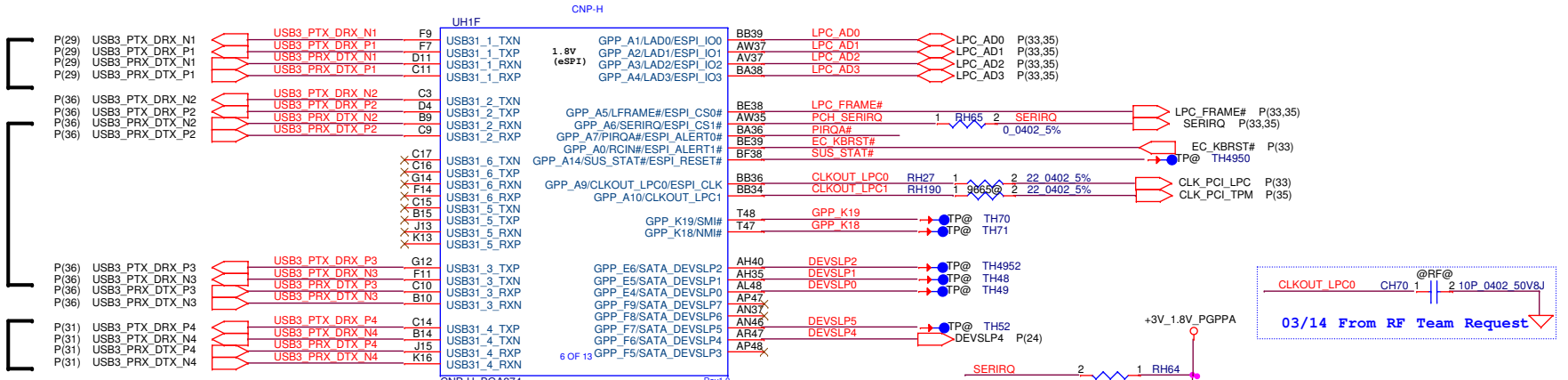
Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

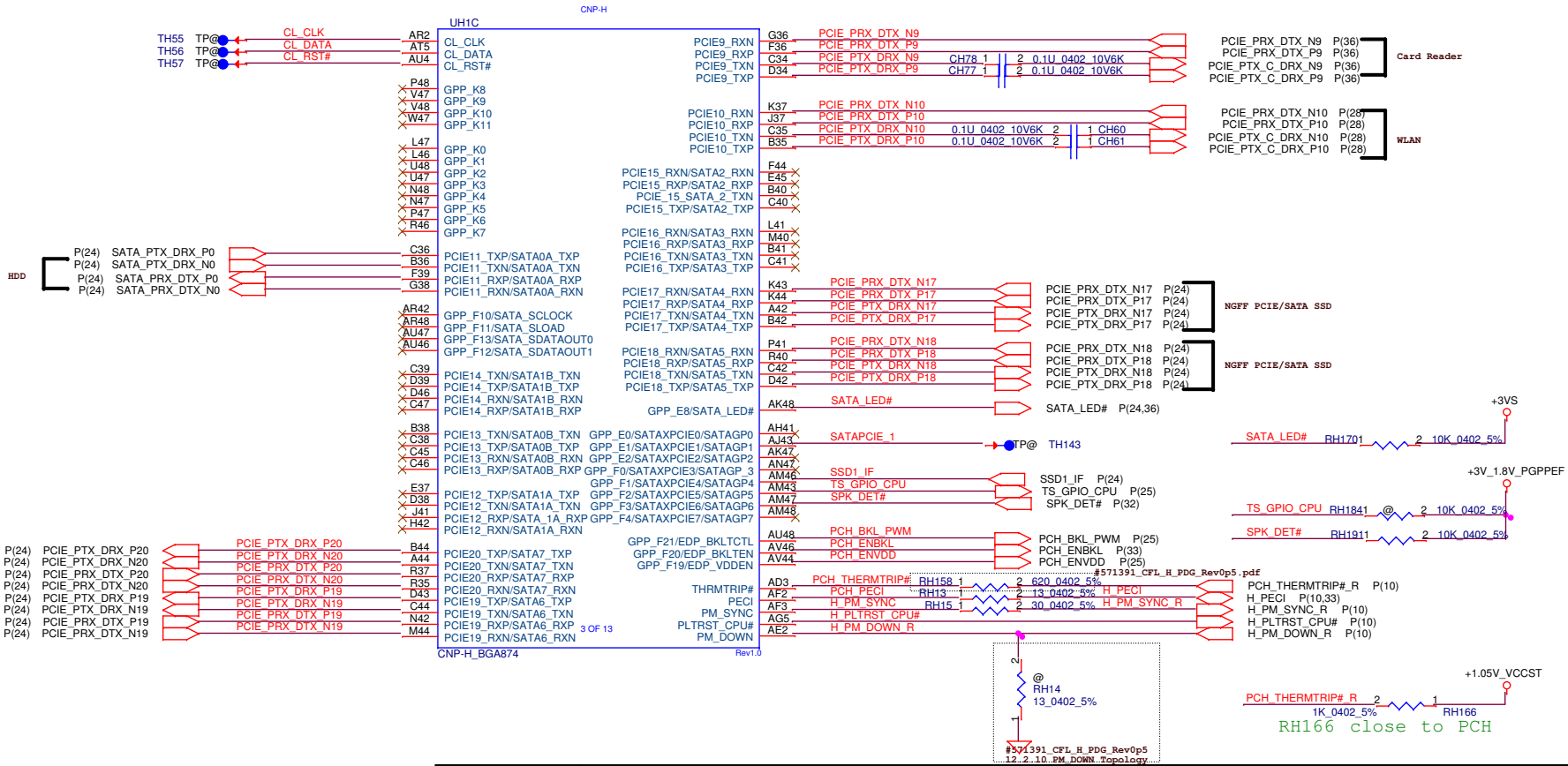
Compal Electronics, Inc.			
Title: PCH(3/8)DDC/SPI			
Size: Custom	Document Number: LA-F841P		Rev: 0.1
Date: Monday, August 28, 2017	Sheet 18 of 65		

Type-A Port - Right Side

Type-A Port - Left Side

Type-C Port





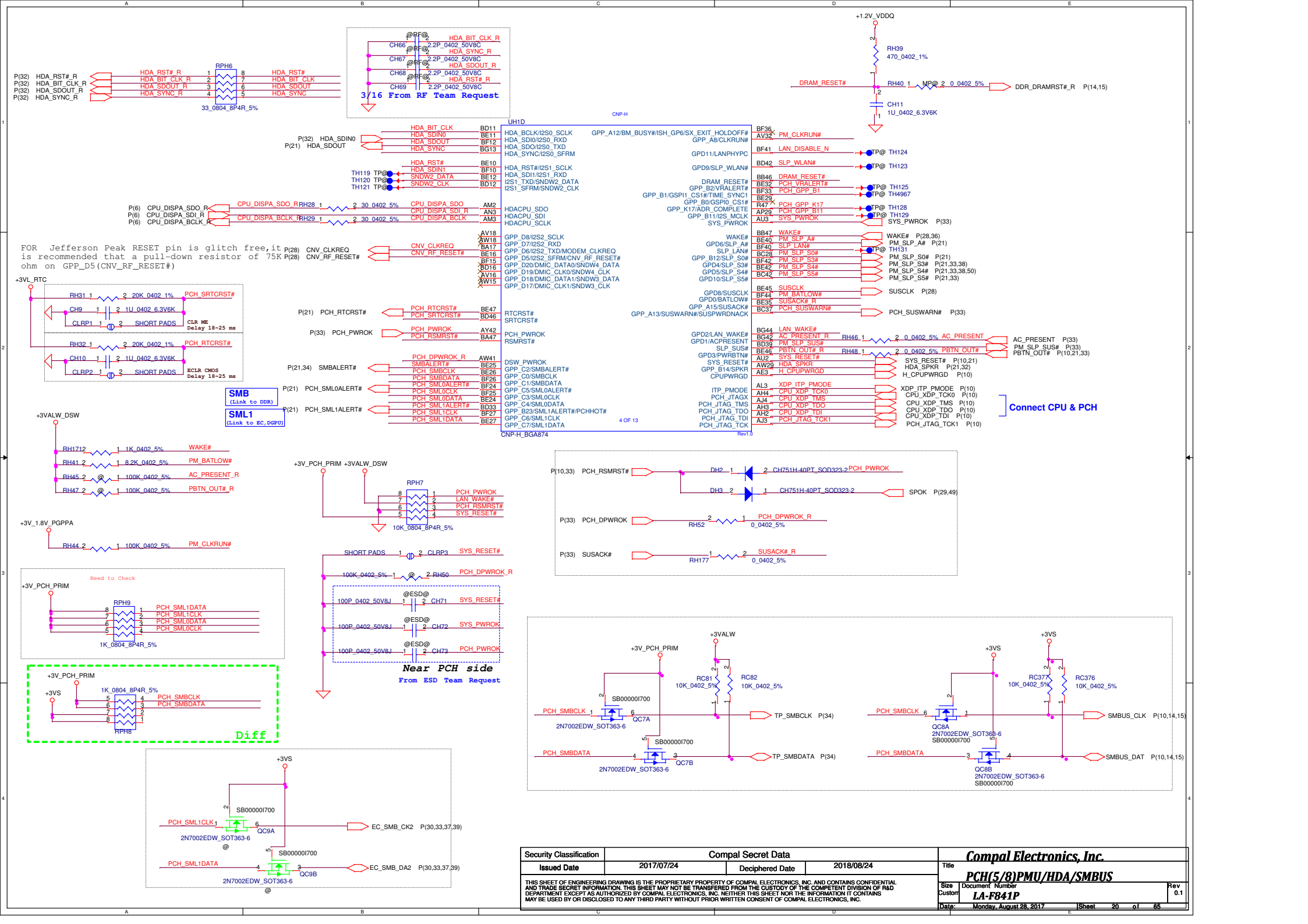
Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: PCIE/SATA/USB3/eSPI

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 19 of 65



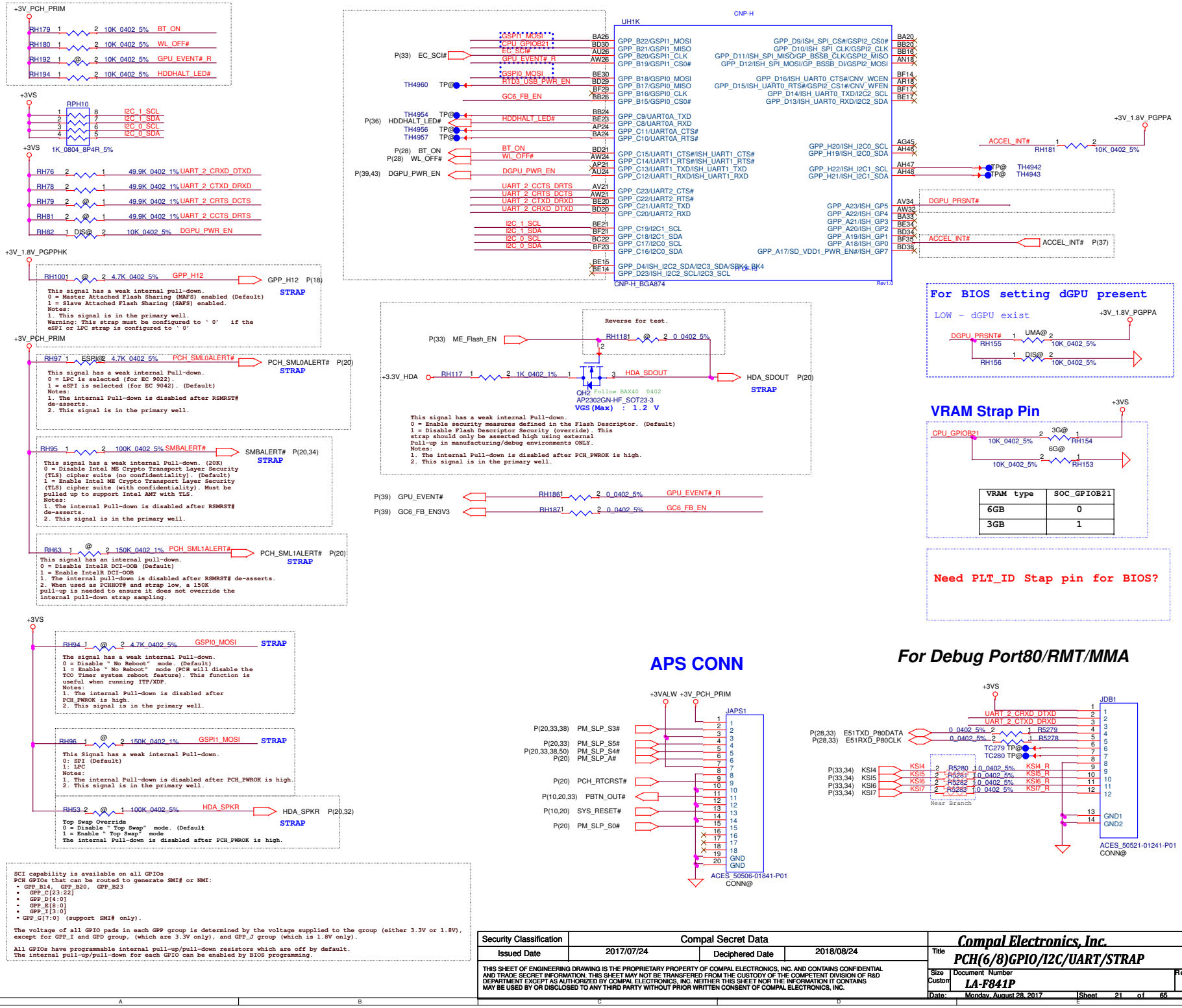
Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: PCH(5/8)PMU/HDA/SMBUS

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 20 of 65



Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.

Title: PCH(6/8)GPIO/I2C/UART/STRAP

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 21 of 65

GPIO Group	Voltage
GPPA	LPC: 3.3V eSPI: 1.8V ★
GPPB GPPC	3.3V
GPPD	1.8V for SOC_DMIC 3.3V for IR_DMIC ★
GPPE GPPF	3.3V
GPPG	3.3V
GPPH GPPK	3.3V
GPPI	3.3V Only
GPPJ	1.8V Only
GPD	3.3V Only

PLACE 3-5MM FROM PACKAGE EDGE

HSIO for DMIU/USB3.1/PCIE=2.196A

Close to BB11

VCCPHVLDO_1P8
(External VRM mode RH172 unmount)

Short pins AJ22,AJ23,AK22,AK23 together at surface layer from PDG Rev0.71

RH174 for 571391_CFL_H_PDG_Rev0p71.pdf

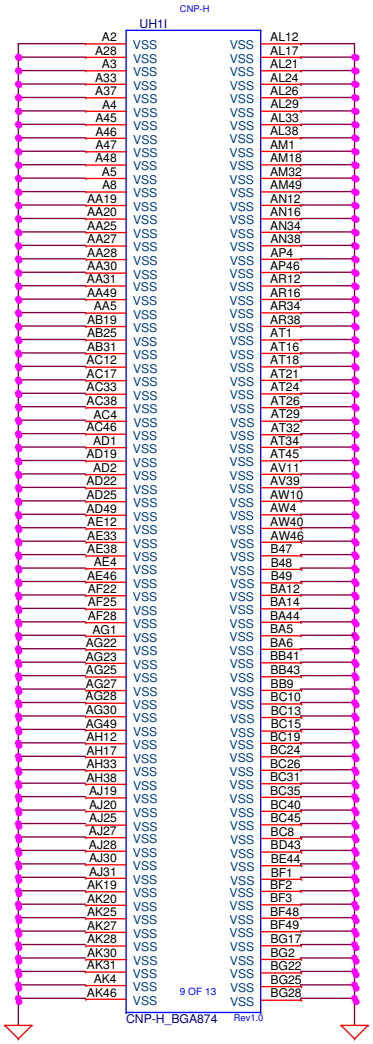
Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

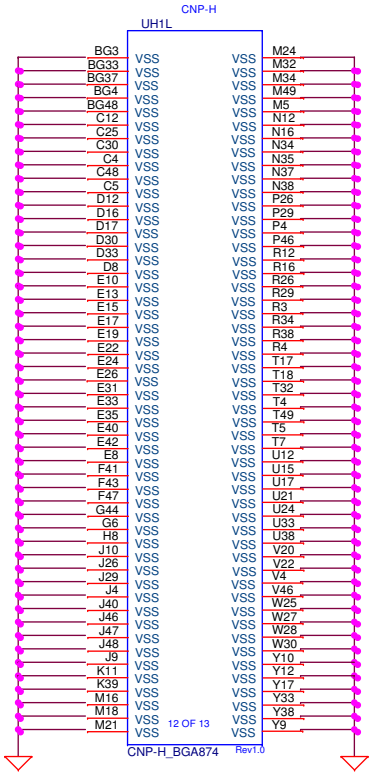
Compal Electronics, Inc.

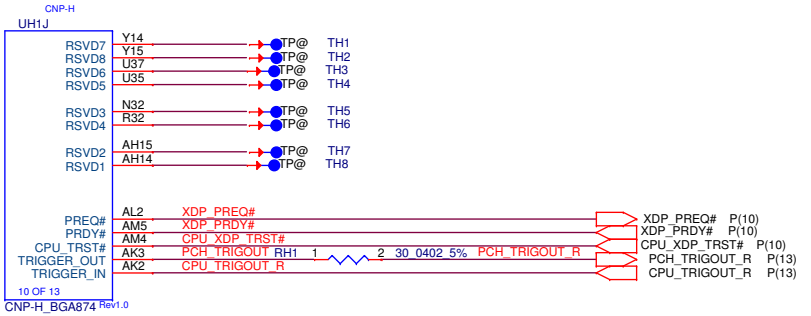
Title: PCH(7/8)Power

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 22 of 65







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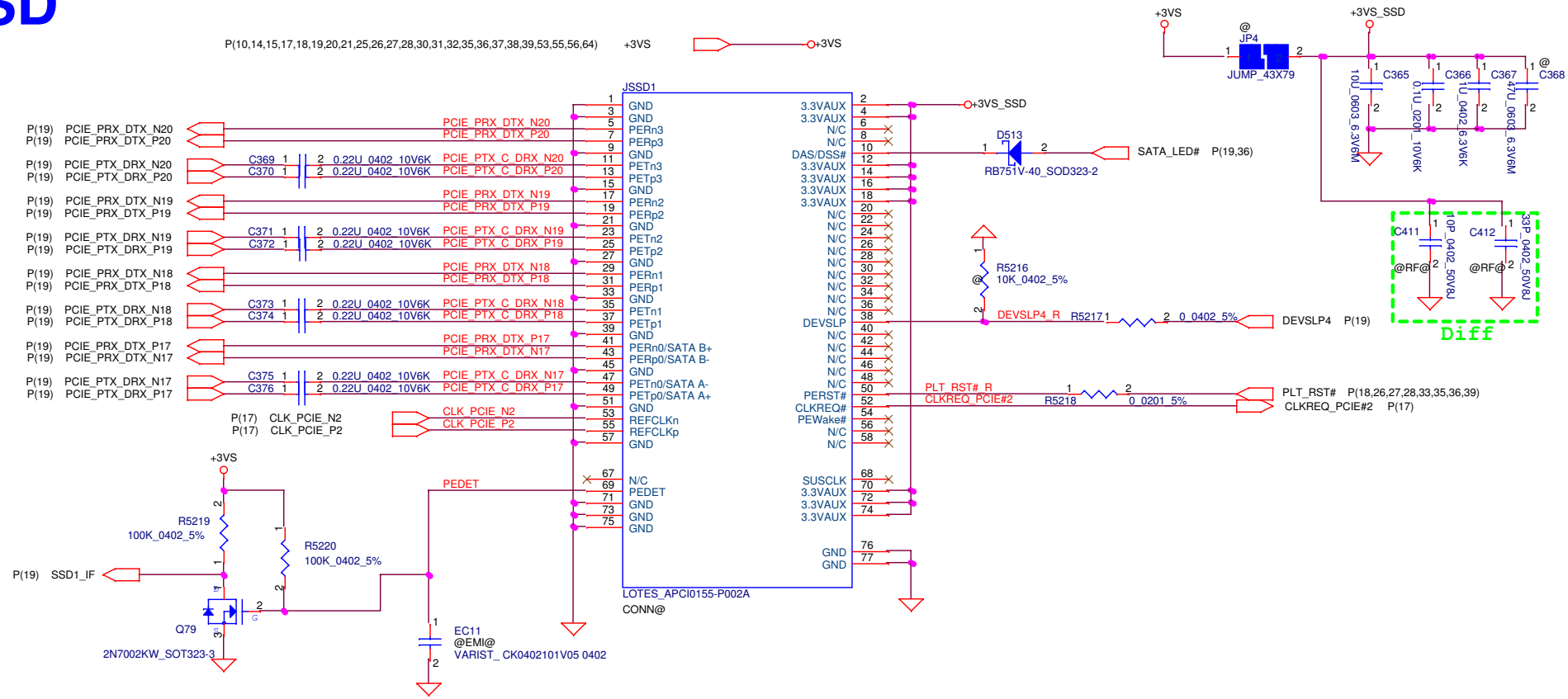
Title: PCH(8/8)GND/RSVD

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 23 of 65

M.2 SSD



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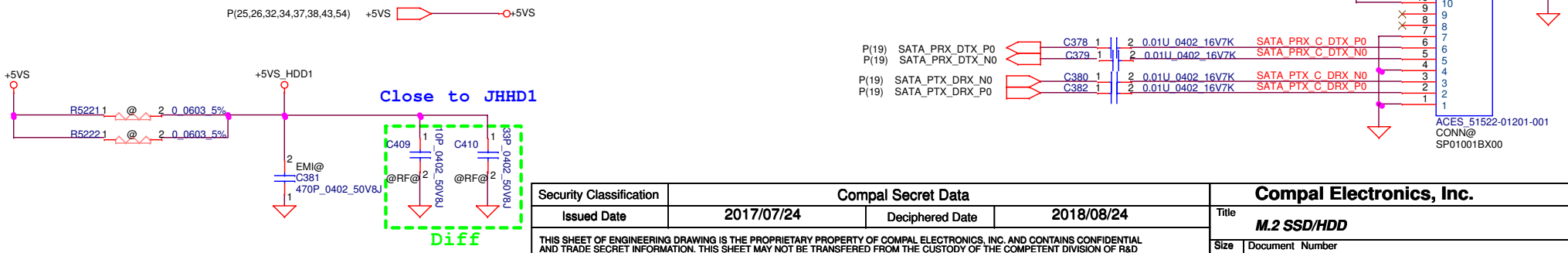

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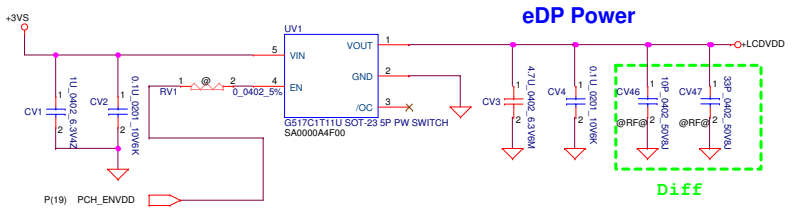
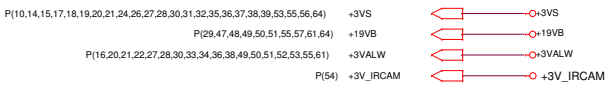
Title	*M.2 SSD/HDD*	
Size	Document Number: LA-F841P	Rev: 0.1
Date: Monday, August 28, 2017	Sheet 24 of 65	





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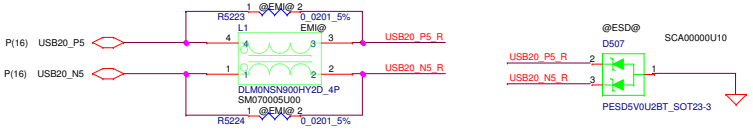
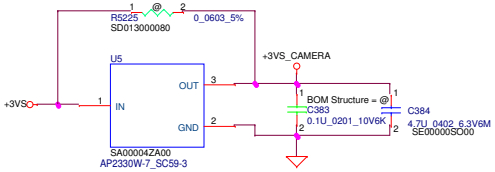
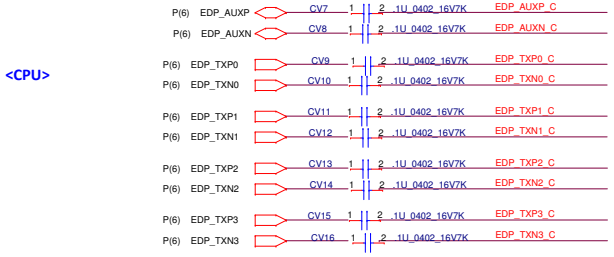
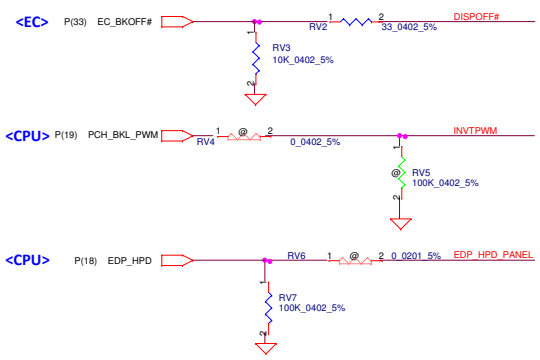
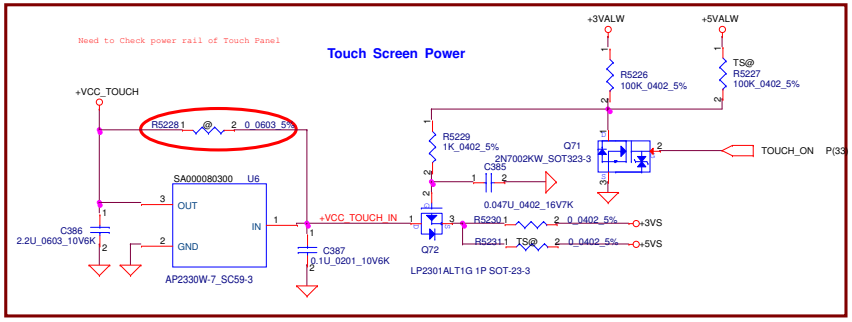


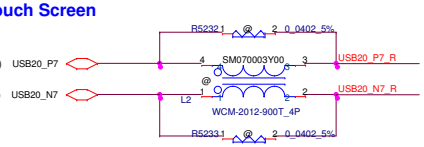


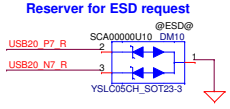


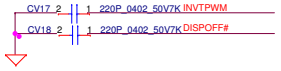


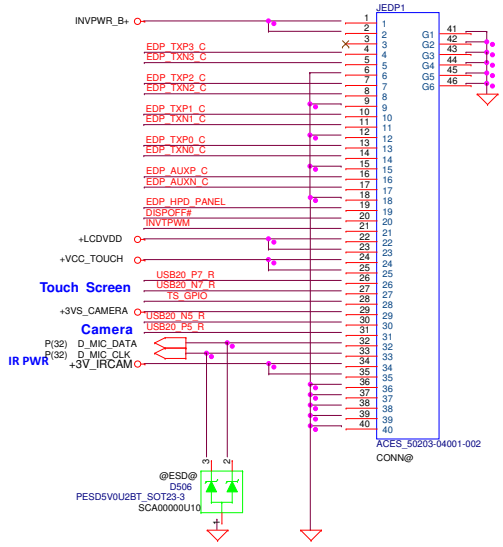
Touch Screen











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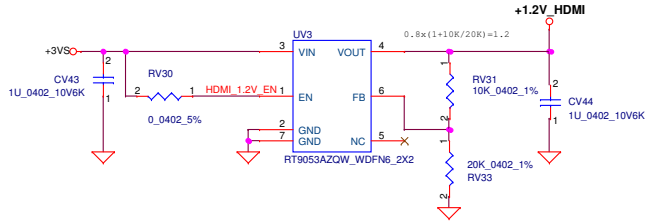
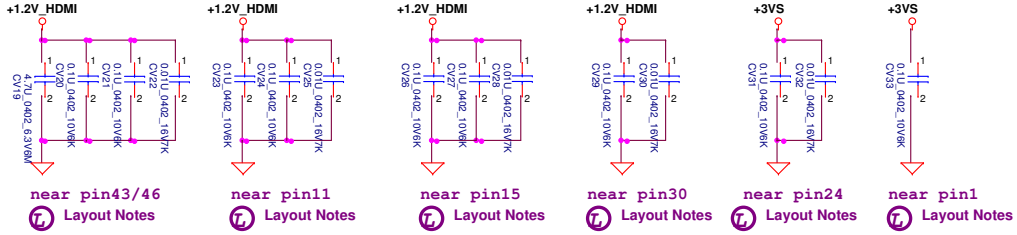
Title: LVDS Connector

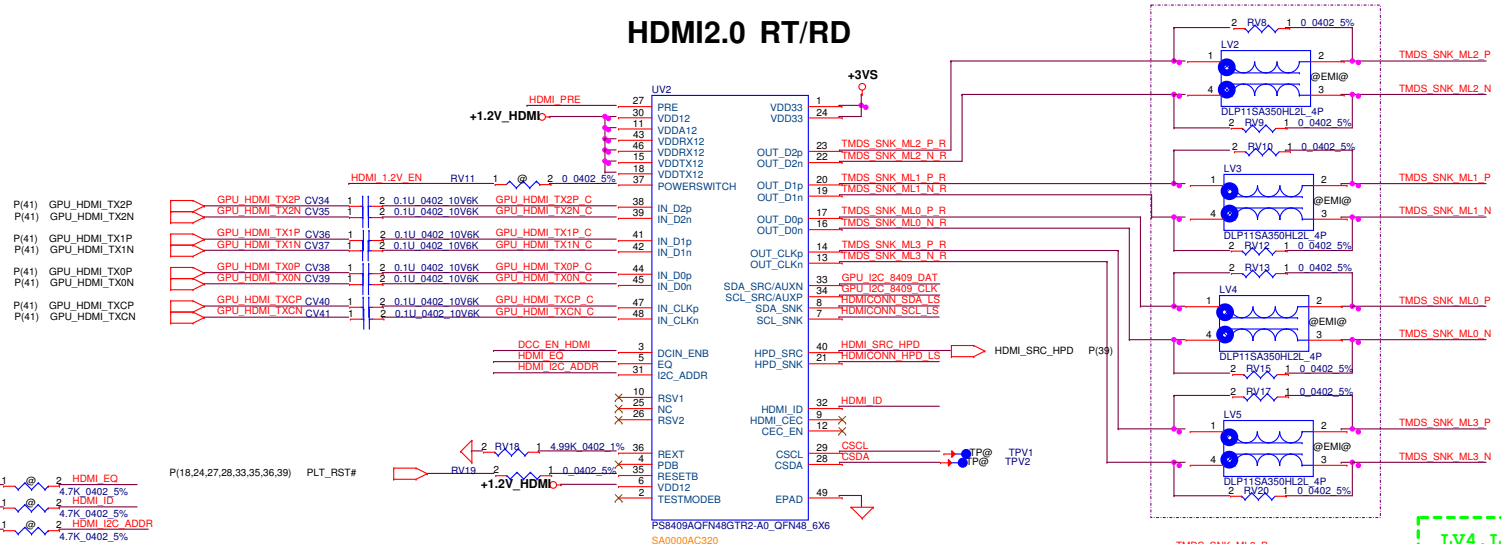
Size	Document Number	Rev
	LA-C707P	0.1

Date: Monday, August 28, 2017 Sheet 25 of 65

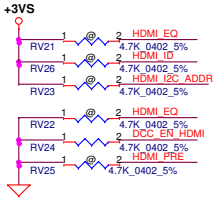
HDMI2.0 RT/RD

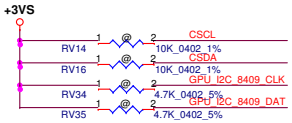


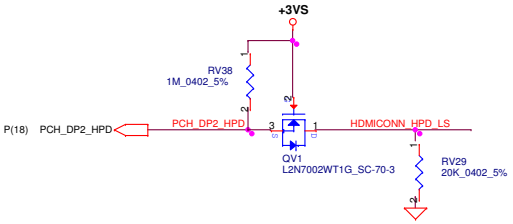


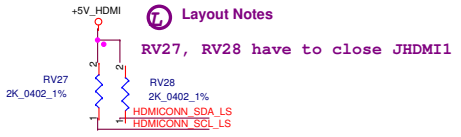


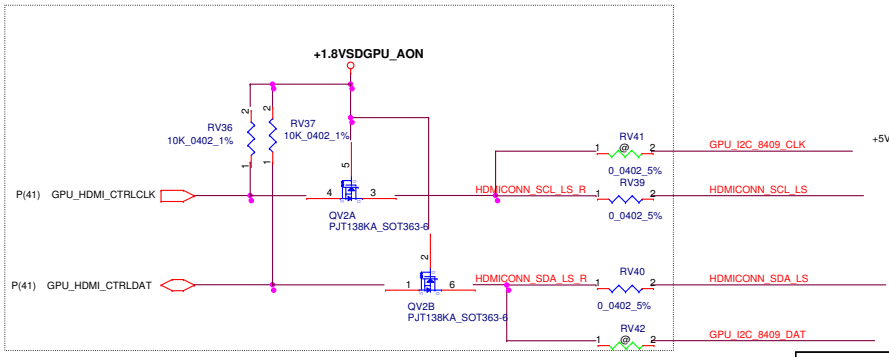
LV4,LV3,LV2,LV5
Diff

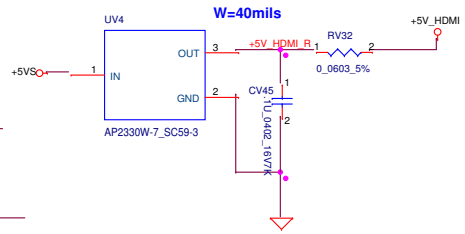


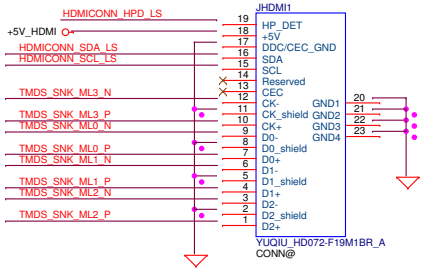








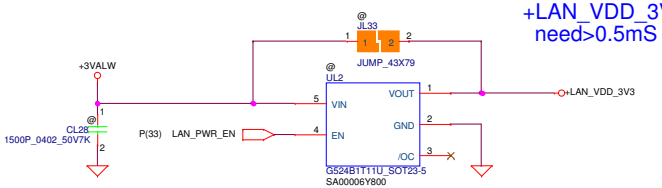


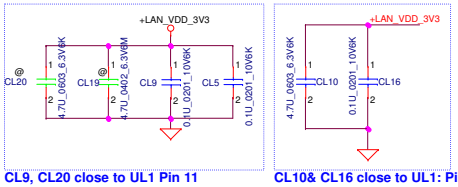


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date		Deciphered Date	Title: LA-F841P

Size	Document Number	Rev
Custom		
Date: Monday, August 28, 2017	Sheet 26 of 65	

+LAN_VDD_3V3 Rising time (10~90%)
need>0.5mS and <100mS

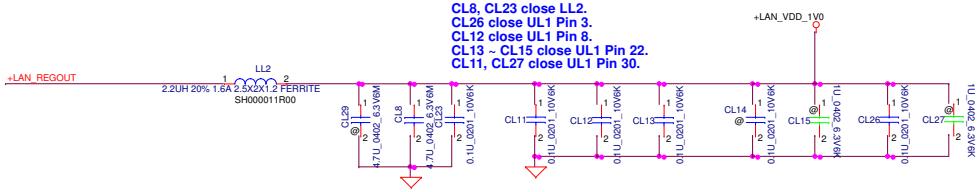




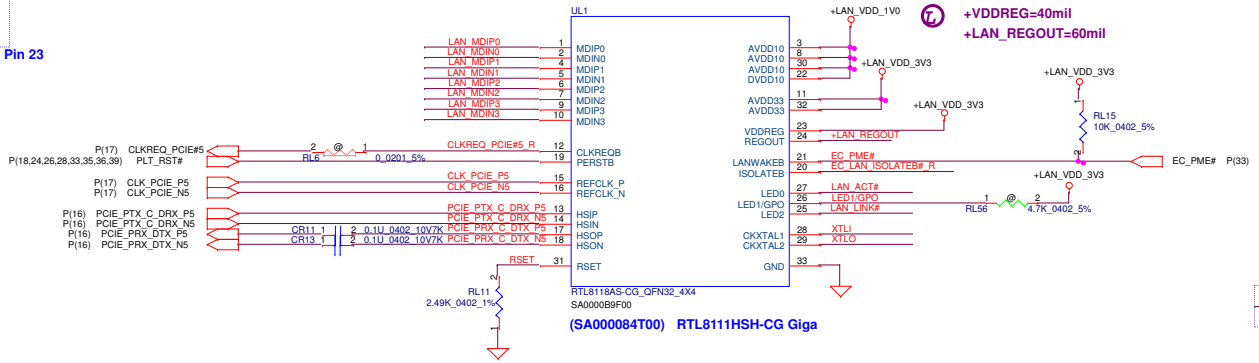
CL9, CL20 close to UL1 Pin 11
CL5 & CL19 close to UL1: Pin 32
CL10& CL16 close to UL1: Pin 23

Note: CL19/CL20 are reserved for surge test

CL8, CL23 close LL2.
CL26 close UL1 Pin 3.
CL12 close UL1 Pin 8.
CL13 ~ CL15 close UL1 Pin 22.
CL11, CL27 close UL1 Pin 30.

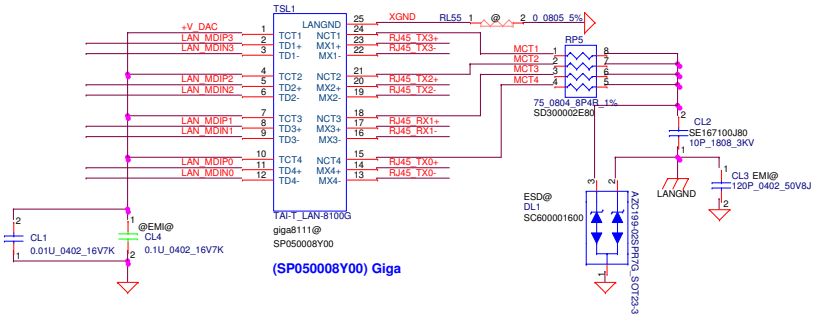


+LAN_VDD_3V3=40mil
+VDDREG=40mil
+LAN_REGOUT=60mil



(SA000084T00) RTL8111HSH-CG Giga

SP050005L00 Footprint



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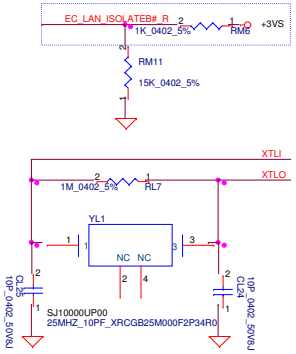

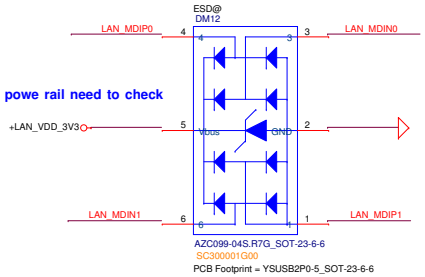

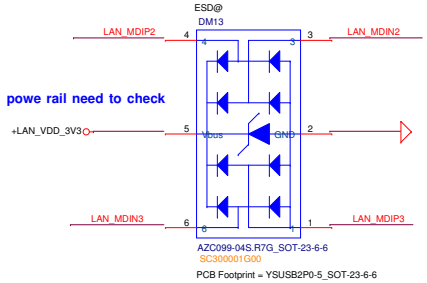

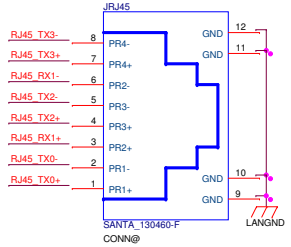

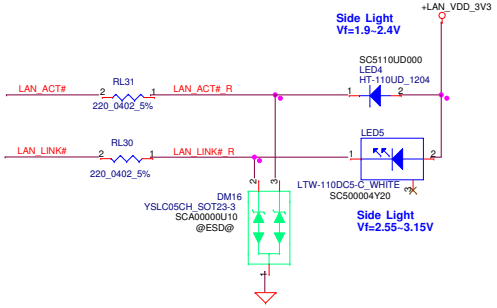

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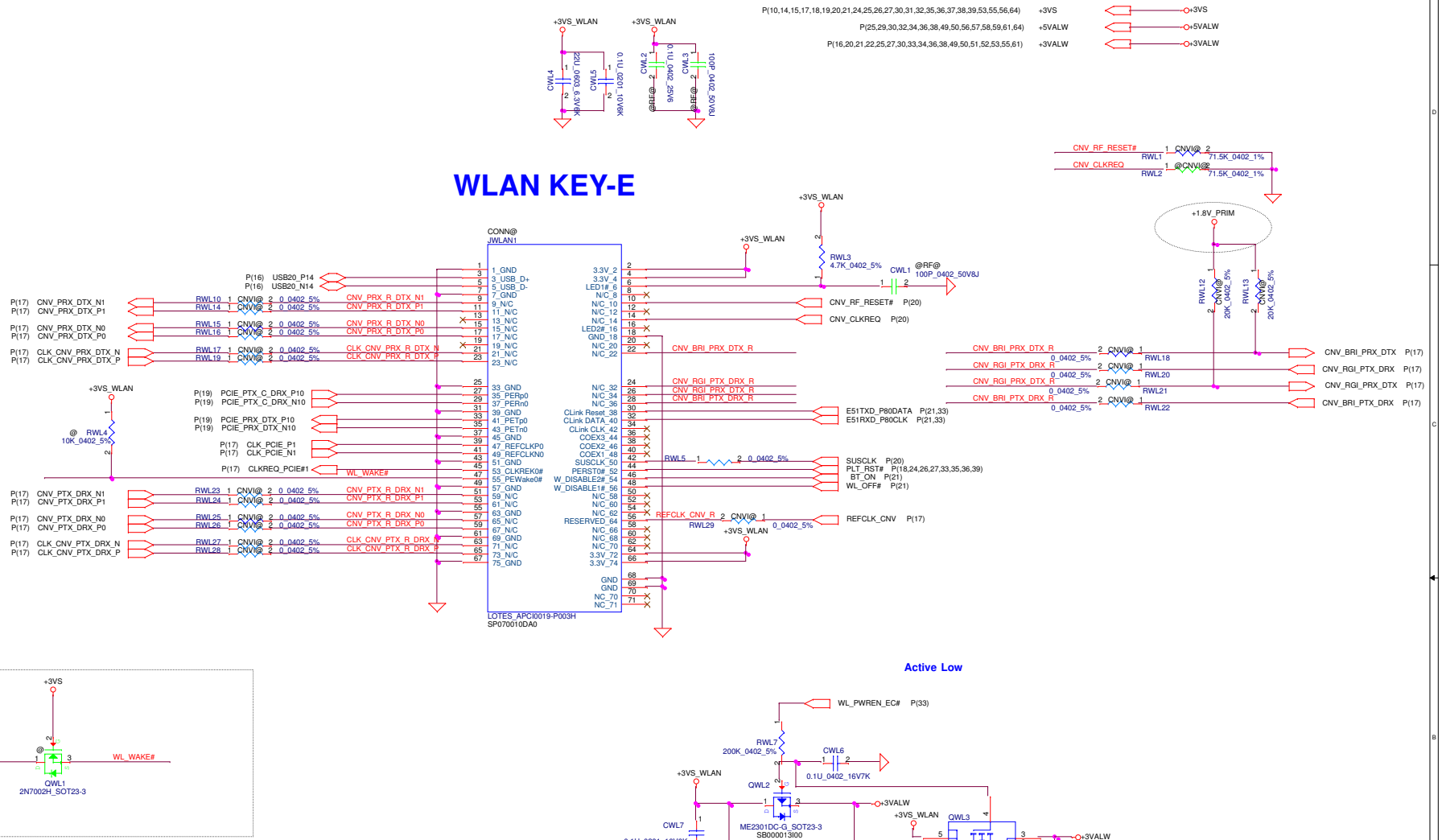
Size	Document Number	Rev
	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 27 of 65

WLAN KEY-E



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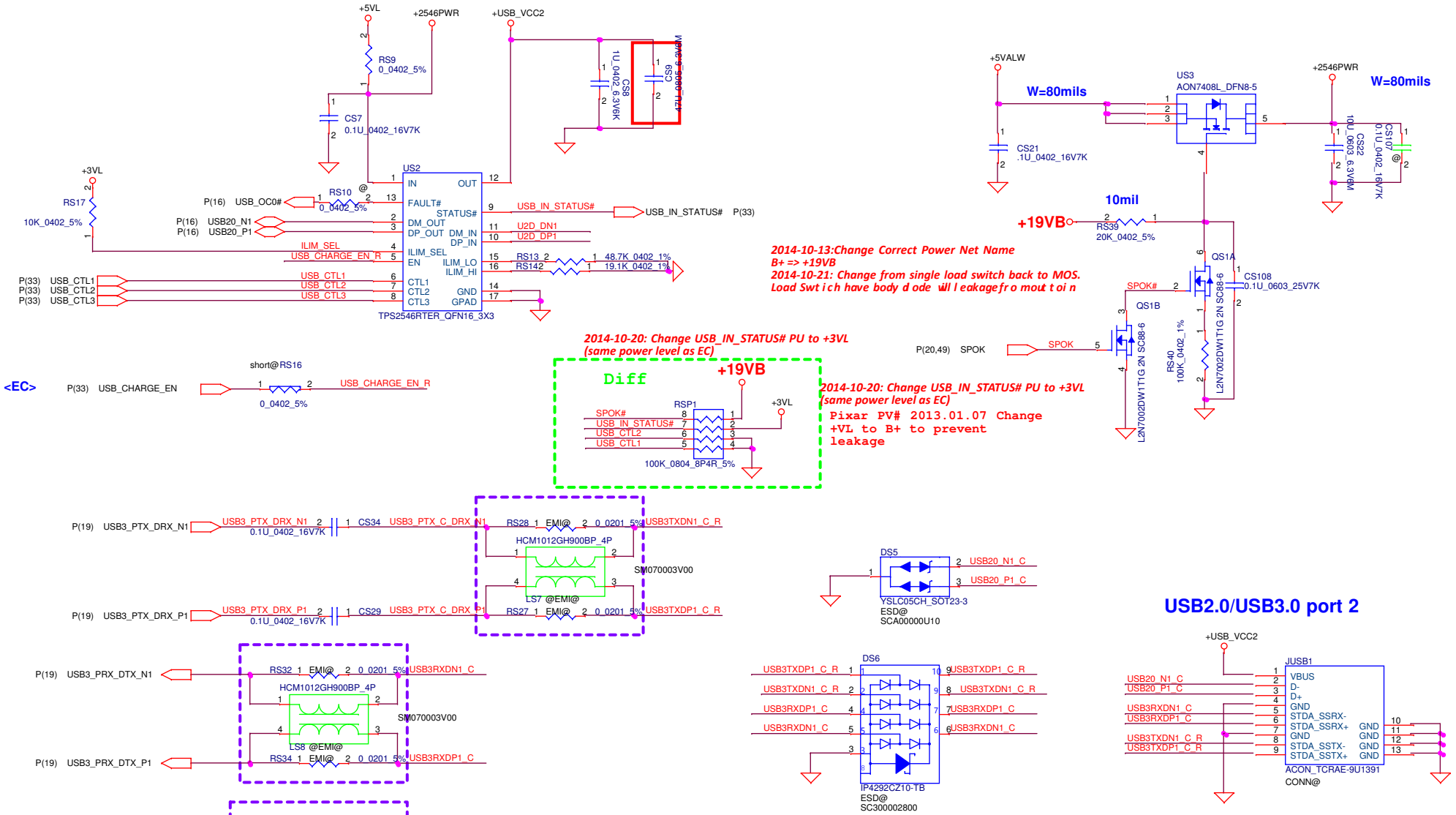
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.			
Title: WLAN-BT			
Size	Document Number: LA-F841P		Rev: 0.1
Date: Monday, August 28, 2017		Sheet 28 of 65	



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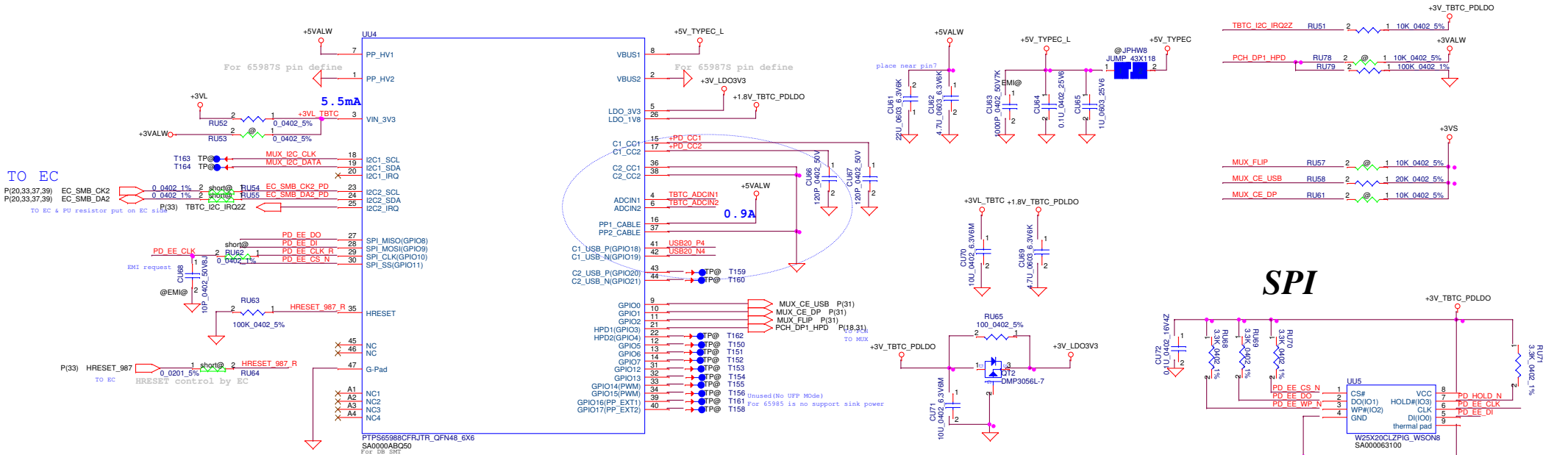
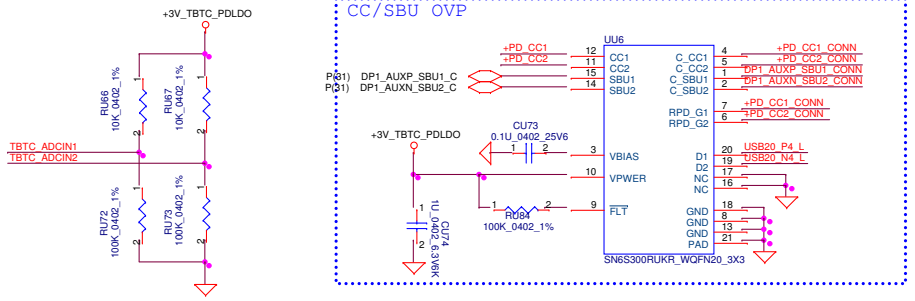
Title: USB Charger

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 29 of 65





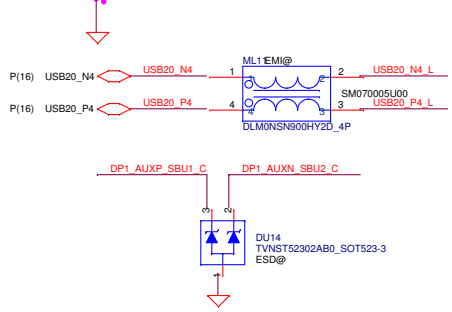
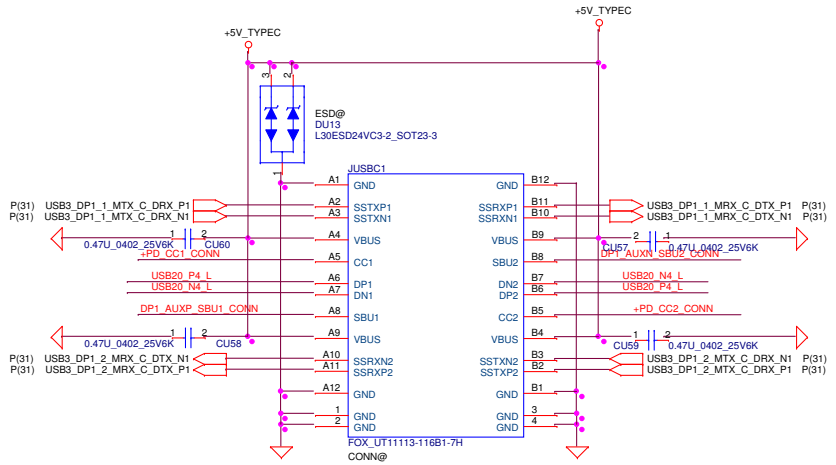


Table 9. I²C Default Unique Address I2C2 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	1	1	1	1	1	R/W
Note 1: Any bit is maskable for each port independently, providing firmware override of the I²C address.							

Table 7. I²C Default Unique Address I2C1 - Port 2

Default I²C Unique Address							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	I2C_ADDR_DECODE_C2[2:0]			R/W
Note 1: Any bit is maskable for each port independently providing firmware override of the I²C address.							



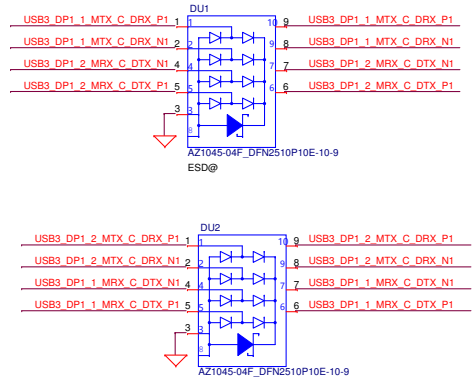


Figure 37. I²C Address Divider

Table 10 lists the external divider needed to set bits [3:1] of the I²C Unique Address.

Table 10. I²C Address Selection

DIV = R2/(R1+R2)(1)		I²C UNIQUE ADDRESS [3:1]	
DIV_min	DIV_max	I2C_ADDR_DECODE_C1	I2C_ADDR_DECODE_C2
0.00	0.18	000b	100b
0.20	0.38	001b	101b
0.40	0.58	010b	110b
0.60	1.00	011b	111b

(1) External resistor tolerance of 1% is required. Resistor values should be chosen to yield a DIV value centered nominally between listed MIN and MAX values.

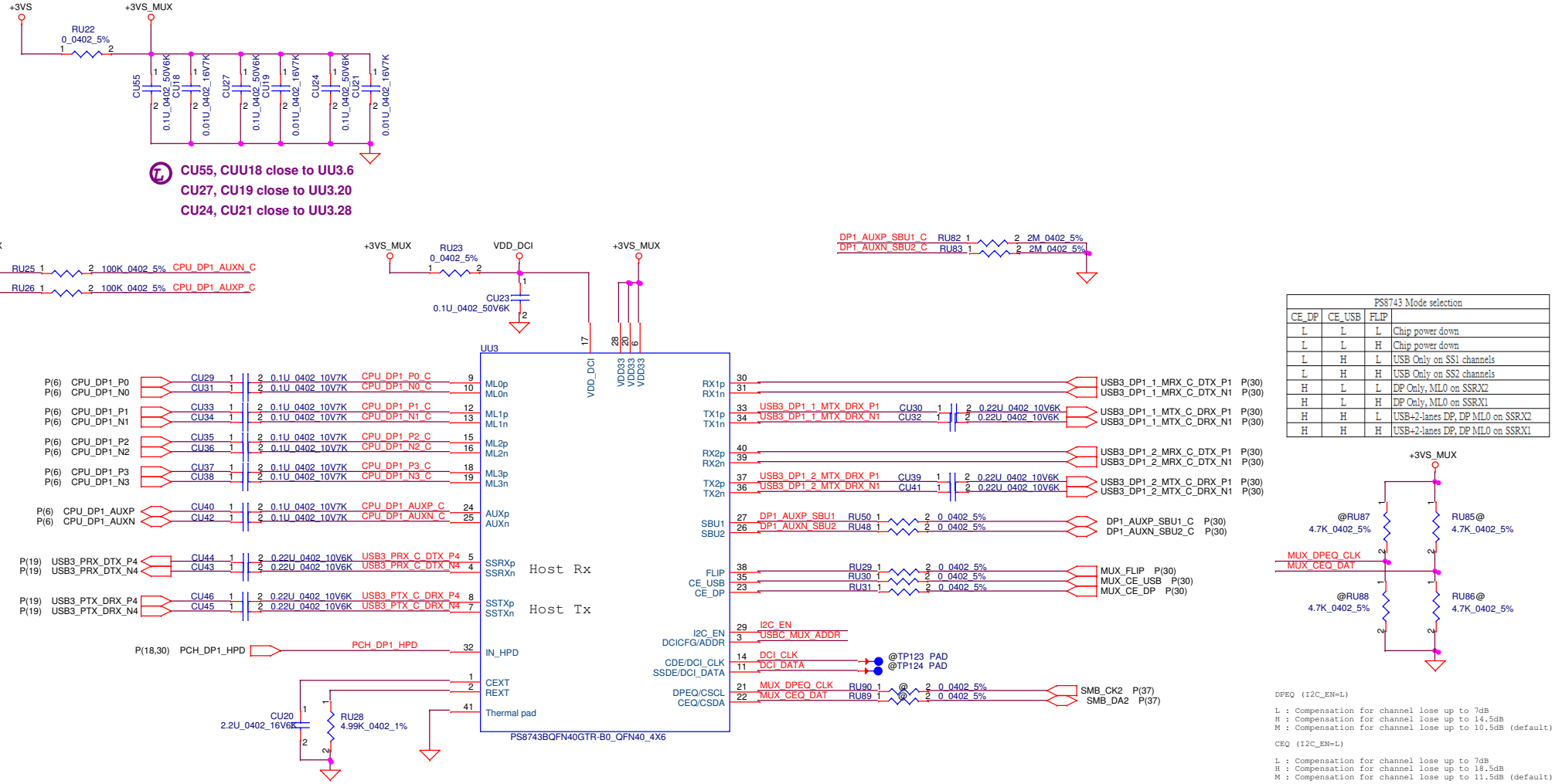
Security Classification	Compal Secret Data		
Issued Date	2017/03/07	Deciphered Date	2018/03/07

Compal Electronics, Inc.

Title: Type-C PORT3-DC IN

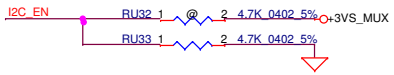
Size: Custom | Document Number: LA-F841P | Rev: 0.1

Date: Monday, August 28, 2017 | Sheet 30 of 65



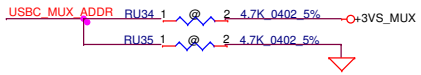
I2C Mode

Pin	Name	I/O	Description
29	I2C_EN	I	I²C Control Enable. Internally pull down at ~150kΩ. 3.3V I/O I2C_EN = L: Pin Control is selected. H: I²C Control is selected.



I2C Address

3	ADDR	I	*For I²C Control Mode only(I2C_EN=H)* ADDR / I²C control bus address LSB. Internally pull down at 150kΩ, 3.3V I/O. [ADDR] = L: 0x20/0x21 H: 0x22/0x23



Security Classification	Compal Secret Data		
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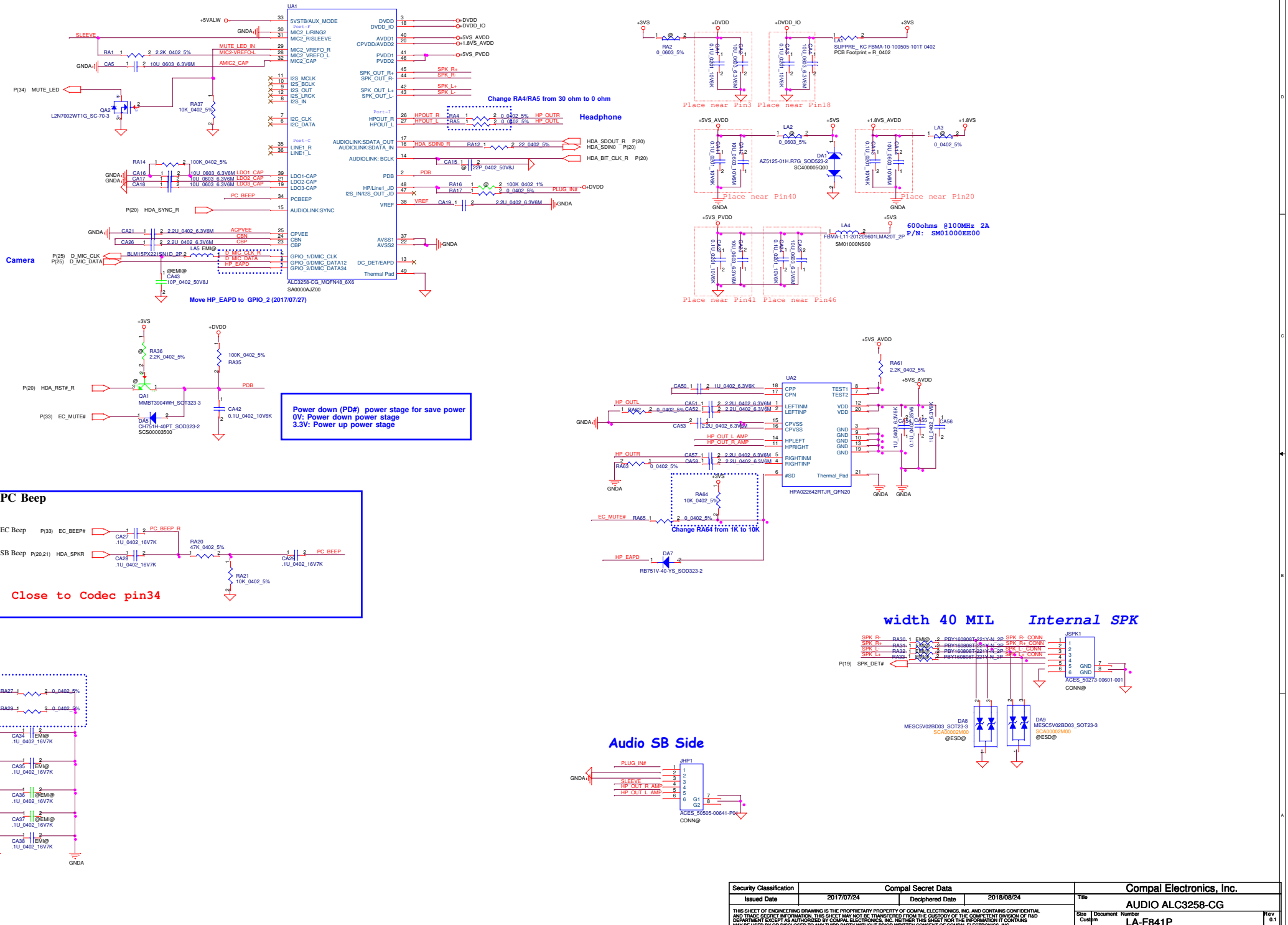
Compal Electronics, Inc.

Title: **USB3.1 10G / DP MUX - ANX7440**

Size	Document Number	Rev
	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 31 of 65



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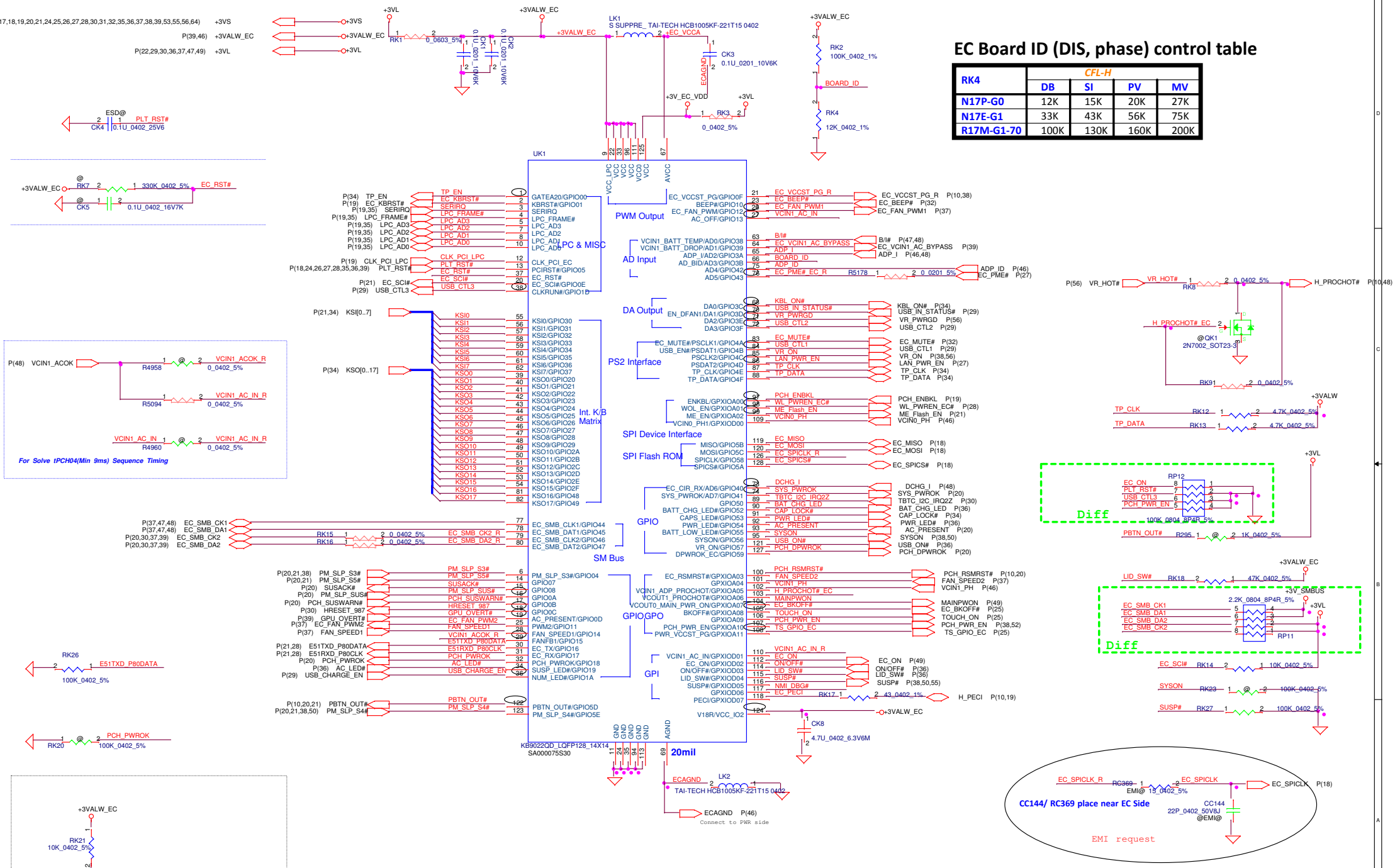
Issued Date	2017/07/24	Deciphered Date	2018/08/24

Compal Electronics, Inc.	
Title	AUDIO ALC3258-CG
Size: Custom	Document Number: LA-F841P
Rev	0.1
Date: Monday, August 28, 2017	Sheet 32 of 65

EC Board ID (DIS, phase) control table

RK4	CFL-H			
	DB	SI	PV	MV
N17P-G0	12K	15K	20K	27K
N17E-G1	33K	43K	56K	75K
R17M-G1-70	100K	130K	160K	200K



Security Classification	Compal Secret Data		
Issued Date	2017/07/24	Deciphered Date	2018/08/24

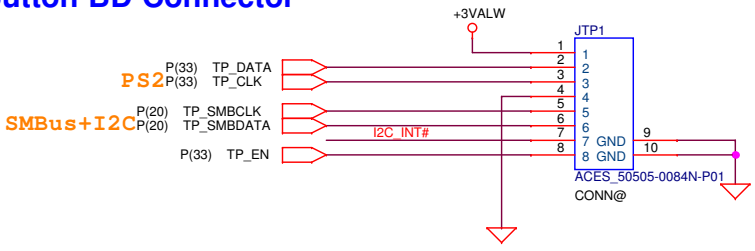
Compal Electronics, Inc.

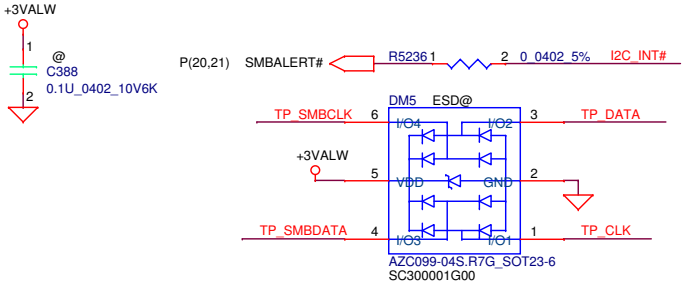
Title: EC ENE-KB9022

Size	Document Number	Rev
Custom	LA-F841P	0.1

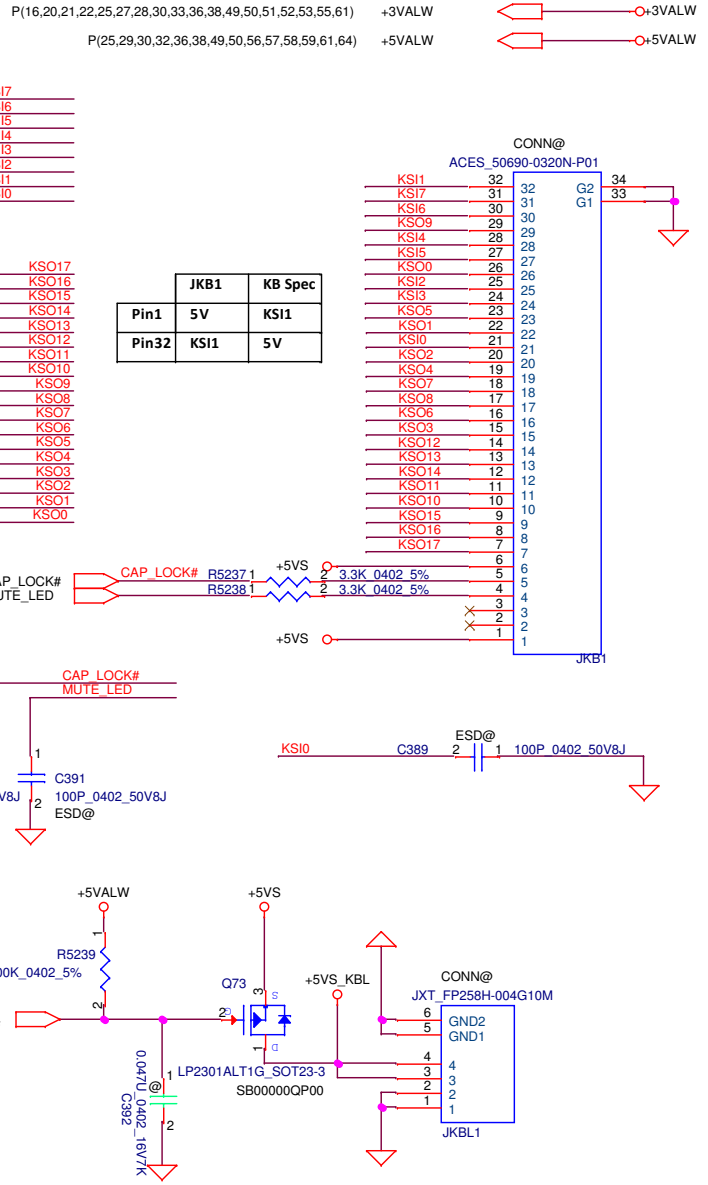
Date: Monday, August 28, 2017 Sheet 33 of 65

TP Button BD Connector





Pin Assignment and Description			
Pin#	Signal	I/O	Description
1	VDD_3.3V	Power	3.3V +/-5%. Power ripple: 100 mVpp max. Power sequence: See section 4.6.
2	PS2_DATA	I/O	PS2 data
3	PS2_CLK	I/O	PS2 clock
4	GND	GND	Ground
5	SMB_CLK	I/O	SMBUS clock I_{Drive} or I_{Sink}: 8 mA max.
6	SMB_DATA	I/O	SMBUS data. I_{Drive} or I_{Sink}: 8 mA max.
7	/INT (/ATTN)	O	For SMBus application, low active, indicates touchpad likes to send data to system (host) if go low.
8	LID_CLOSE (TP Disable/Enable)	I	Enable or disable touchpad, low active Low: Disable TP High: Enable TP



JKB1	KB Spec
Pin1	5V	KSI1
Pin32	KSI1	5V

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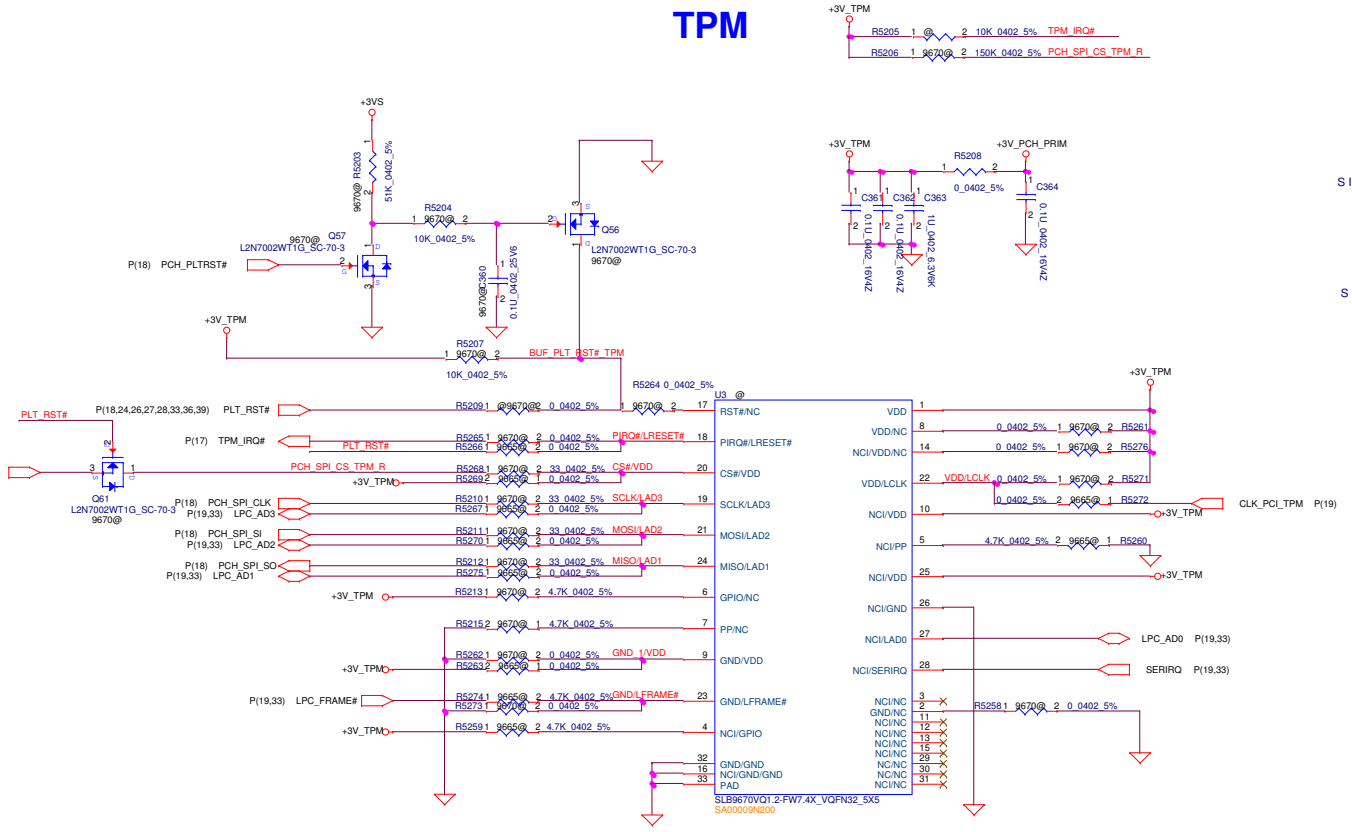
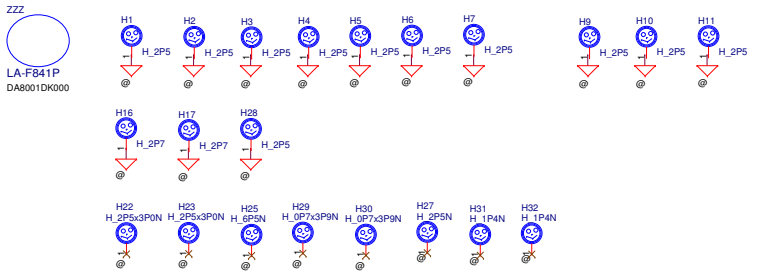
Size: B | Document Number: LA-F841P | Rev: 0.1

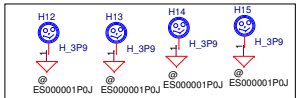
Date: Monday, August 28, 2017 | Sheet 34 of 65

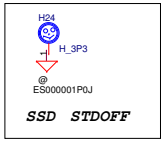
TPM

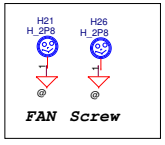


PCB Screw Hole









Fiducial Mark

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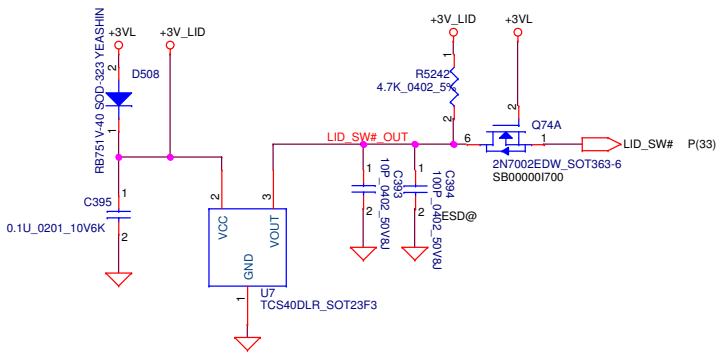
Size	Document Number	Rev
Custom	LA-F841P	0.1

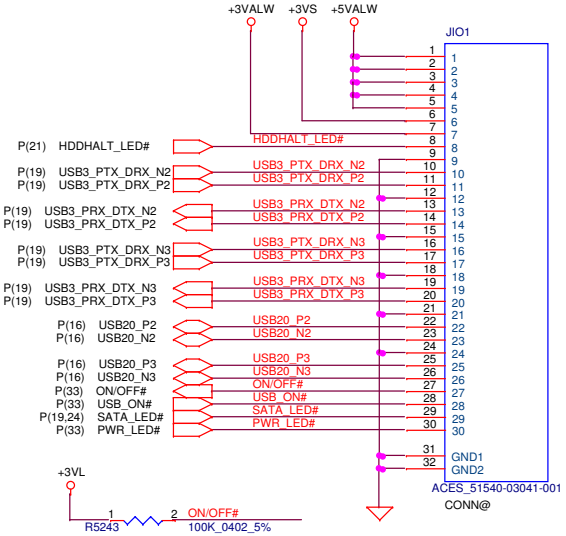
Date: Monday, August 28, 2017 | Sheet 35 of 65

Lid Switch (Hall Effect Sensor)

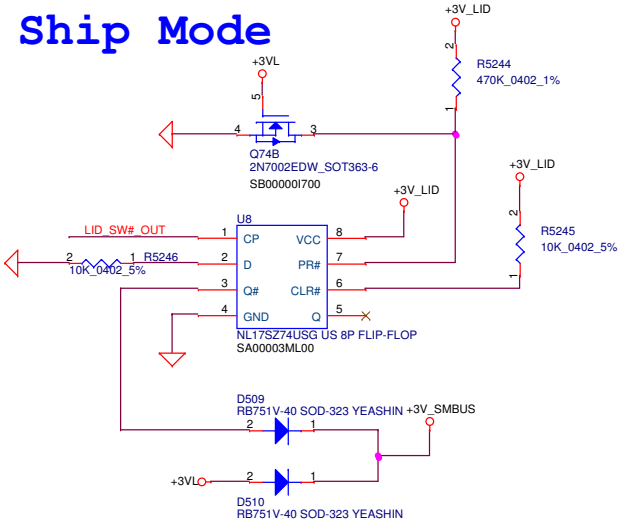


DC-IN LED

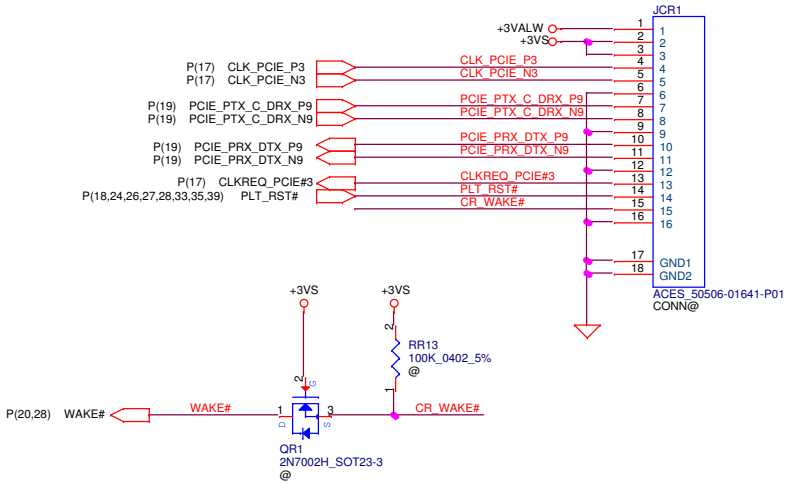
To IO Board



Ship Mode



To Card Reader Board



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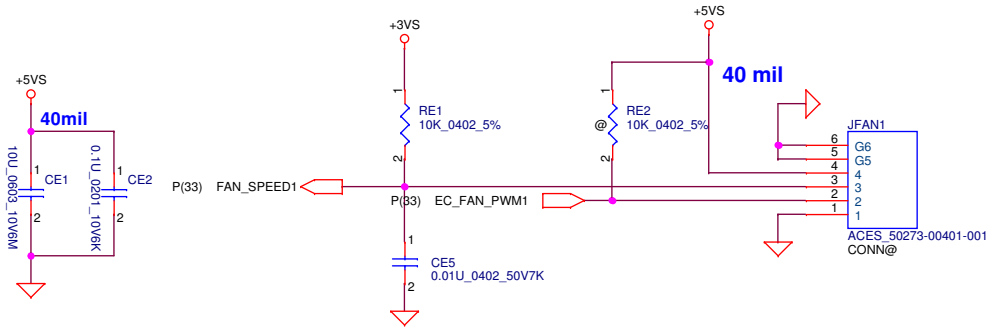
Title: IO CON

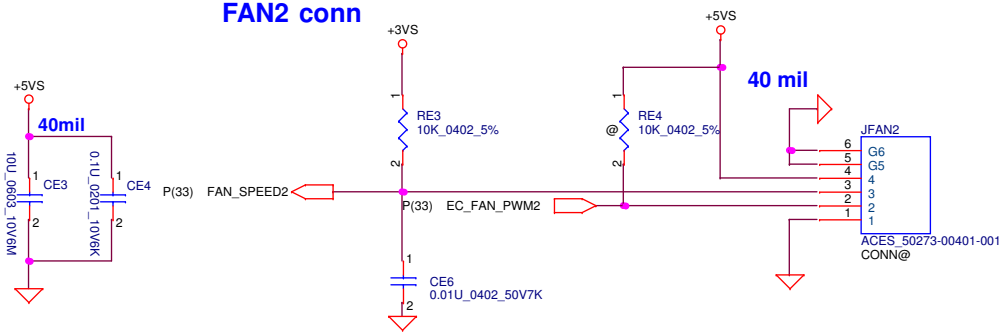
Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 36 of 65

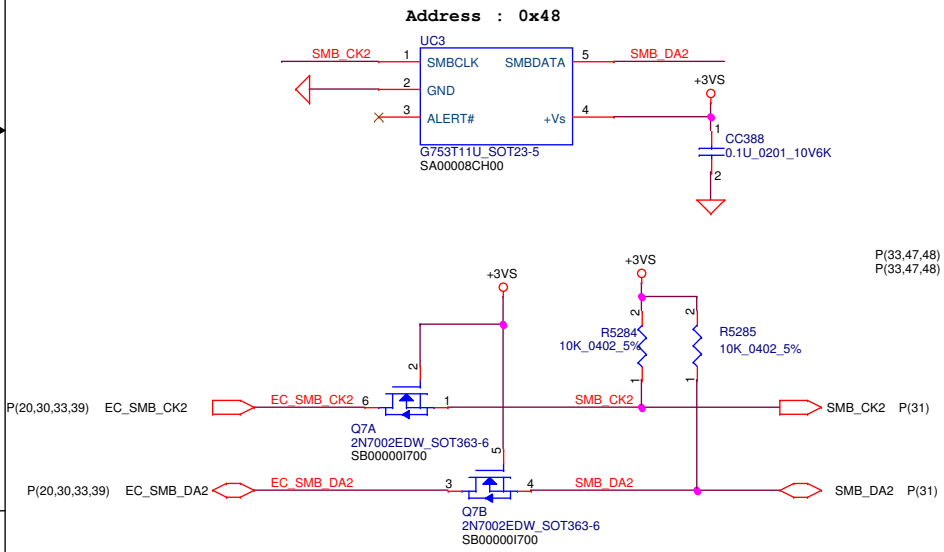
FAN1 conn



FAN2 conn



CPU THERMAL SENSOR



Slave Address

The G753 appears to the SMBus as one device having a common address for both ADC channels.
The G753 has the following SMBus slave address:

	A6	A5	A4	A3	A2	A1	A0
G753	1	0	0	1	0	0	0

ACCELEROMETER
ST Micro HP2DC

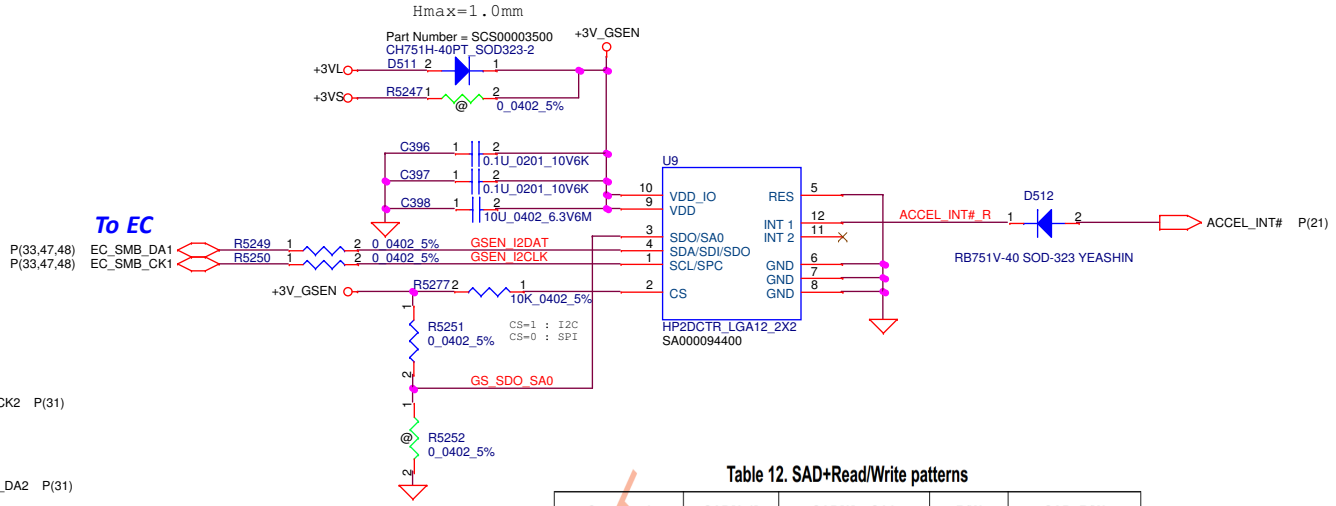


Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

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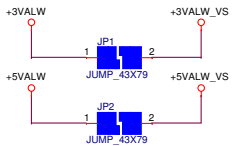
Title: FAN/G-Sensor/Thermal Sensor

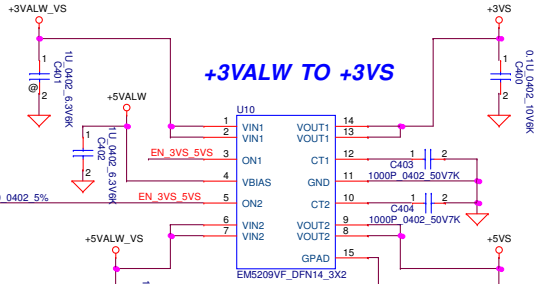
Size: Custom | Document Number: LA-F841P | Rev: 0.1

Date: Monday, August 28, 2017 | Sheet 37 of 65

For Power consumption Measurement

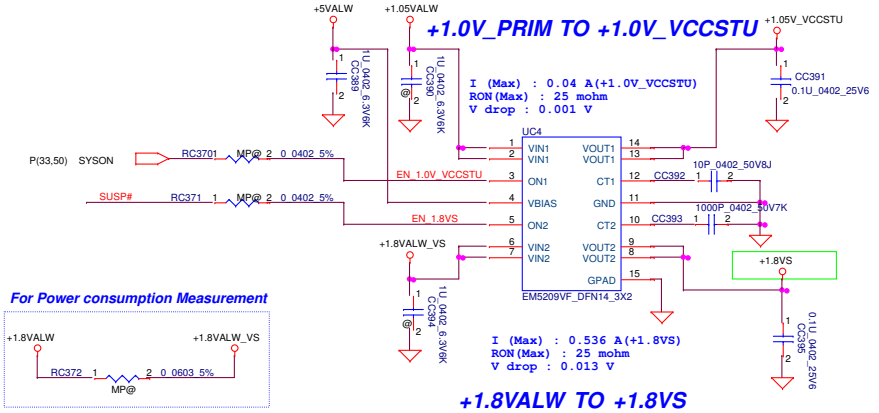


+3VALW TO +3VS



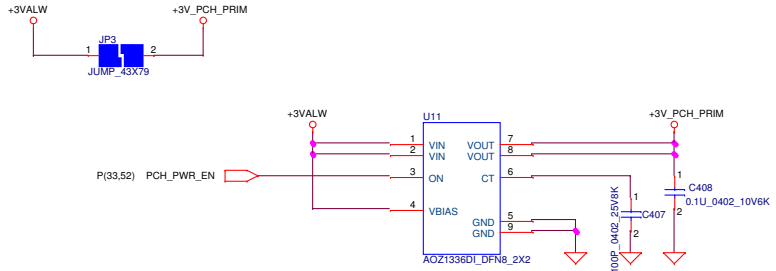
+5VALW TO +5VS

+1.0V_PRIM TO +1.0V_VCCSTU

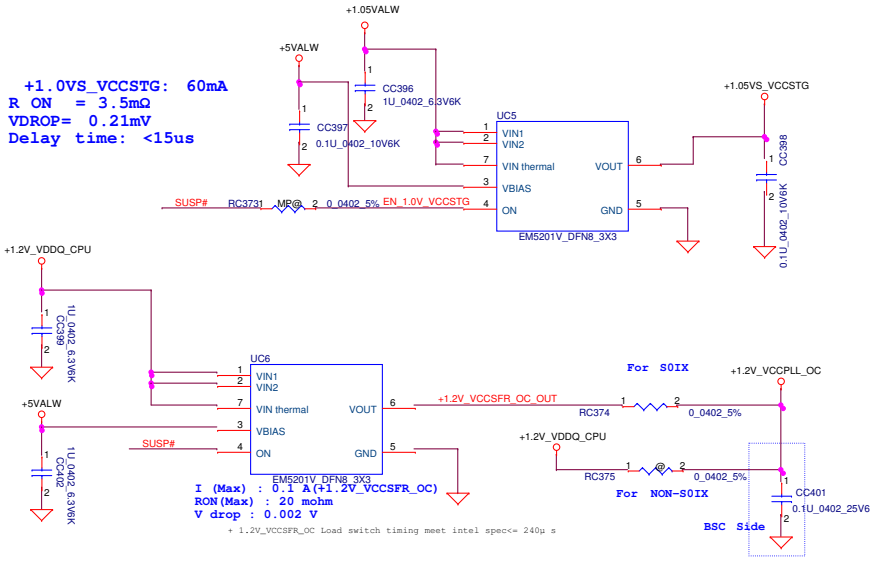


For Power consumption Measurement

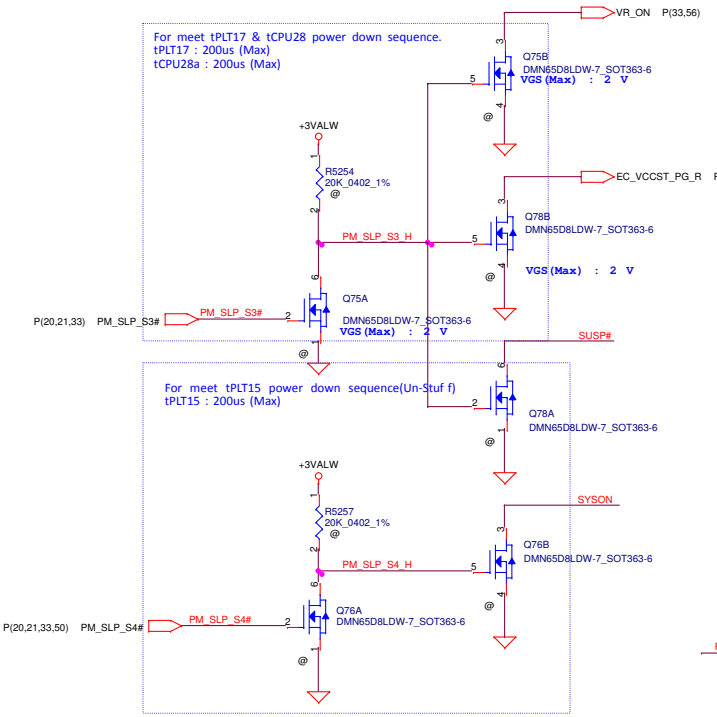
+1.8VALW TO +1.8VS



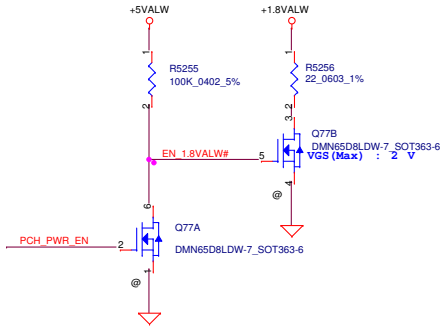
+1VALW TO +1.0VS_VCCSTG



For Power OFF Sequence



For +1.8VALW Discharge



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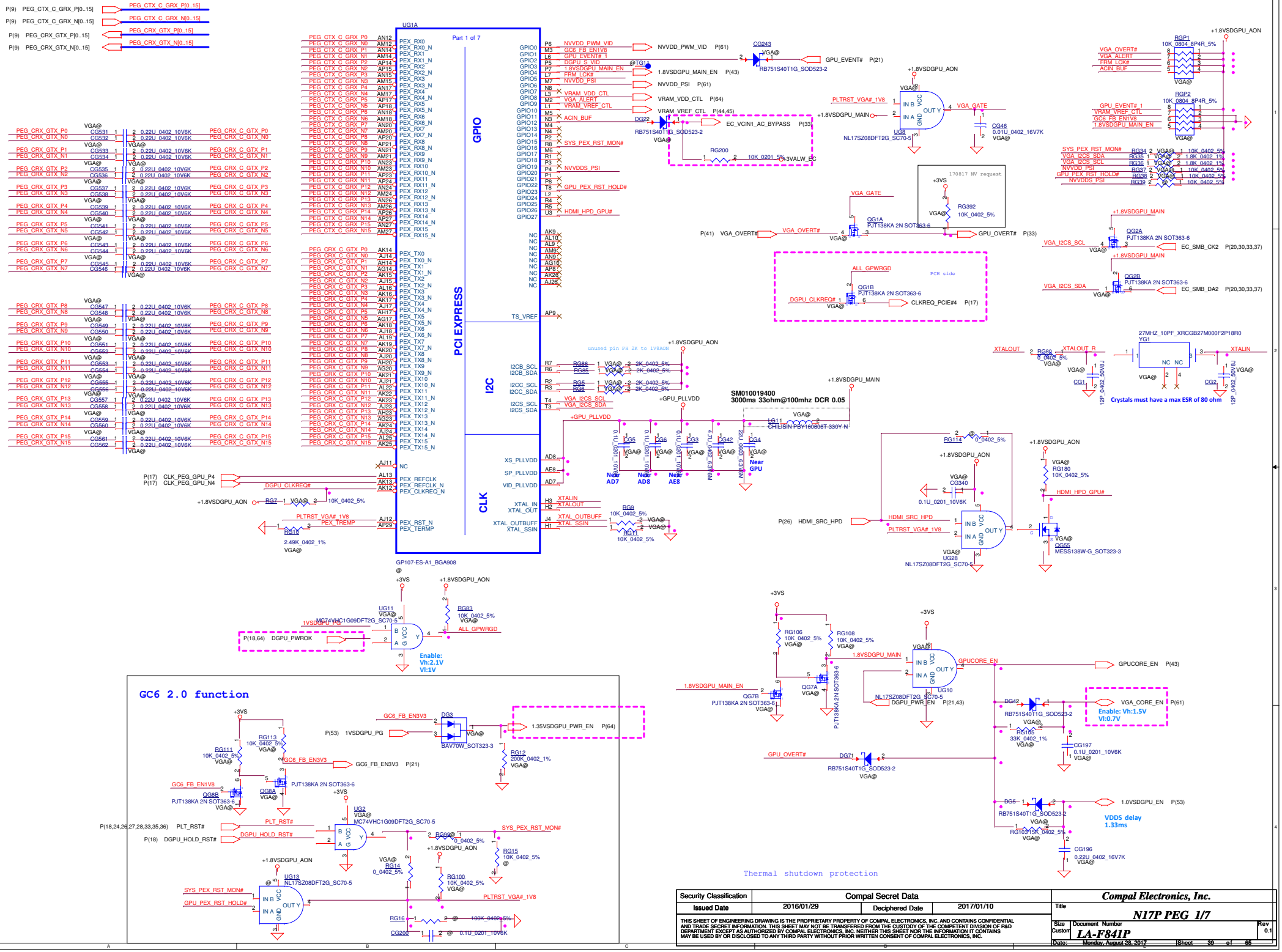
Size	Document Number: LA-F841P
Rev	0.1
Date:	Monday, August 28, 2017
Sheet	38 of 65


PEG_CTX_C_GRX_P[0..15]
PEG_CTX_C_GRX_N[0..15]
PEG_CRX_GTX_P[0..15]
PEG_CRX_GTX_N[0..15]
UG1A
Part 1 of 7
GPIO
PCI EXPRESS
I2C
CLK
GP107-ES-A1_BGA908
GC6 2.0 function
Thermal shutdown protection
SM010019400
3000ma 33ohm@100mhz DCR 0.05
27MHZ_10PF_XRCGB27M000F2P18R0
Crystals must have a max ESR of 80 ohm
Enable: Vh:2.1V Vl:1V
Enable: Vh:1.5V Vl:0.7V
VDDS delay 1.33ms
Security Classification
Compal Secret Data
Issued Date
2016/01/29
Deciphered Date
2017/01/10
Compal Electronics, Inc.
N17P PEG 1/7
LA-F841P
Rev 0.1
Monday, August 28, 2017
Sheet 30 of 65

GDDR5 Mode H Mapping

P(45)	DATA Bus	
Address	0..31	32..63
CMD0	CS#	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE#	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI#	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS#	
CMD13	RST#	
CMD14	CKE#	
CMD15	CAS#	
CMD16		CS#
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE#
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI#
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS#
CMD29		RST#
CMD30		CKE#
CMD31		CAS#

MEMORY INTERFACE A

UG1B

Part 2 of 7

GP107-ES-A1_BGA908

MEMORY INTERFACE B

UG1C

Part 3 of 7

GP107-ES-A1_BGA908

CKE signal

RST signal

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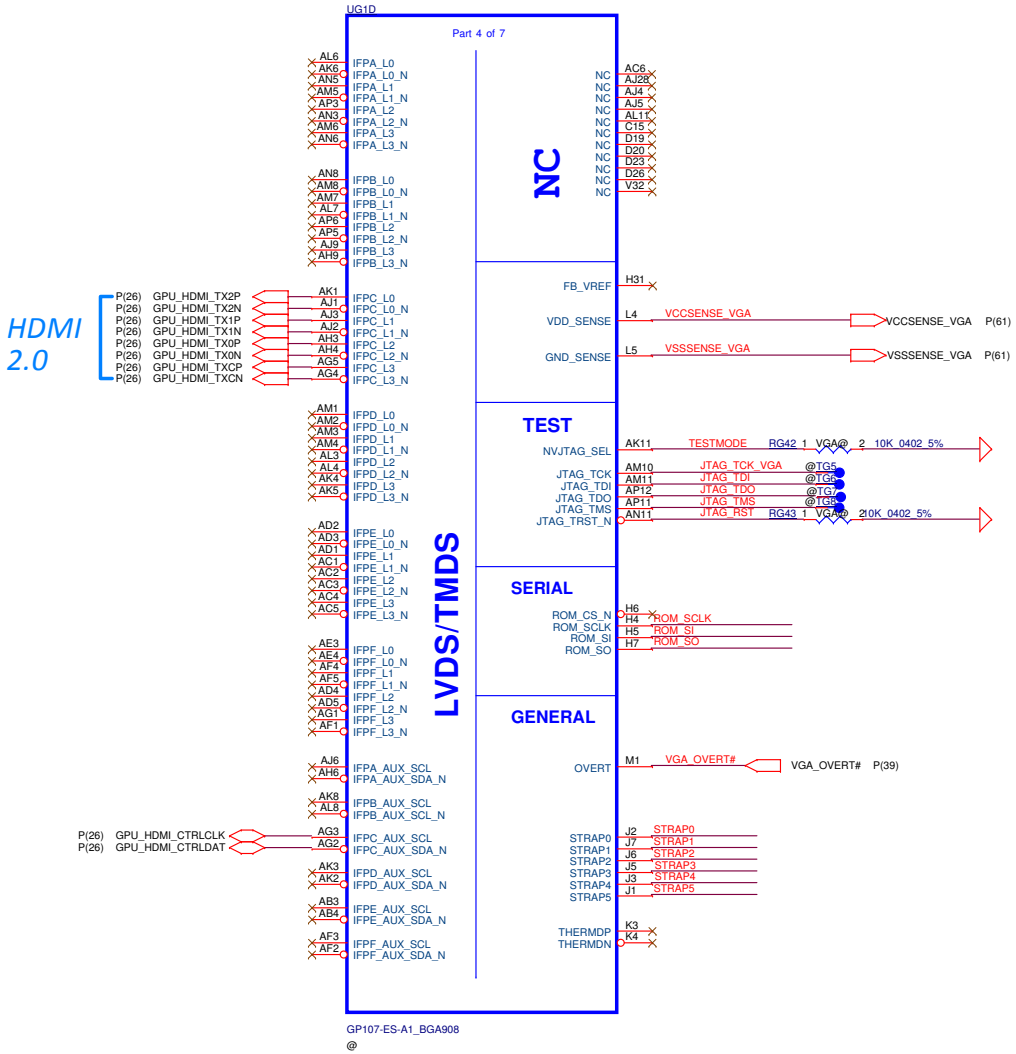
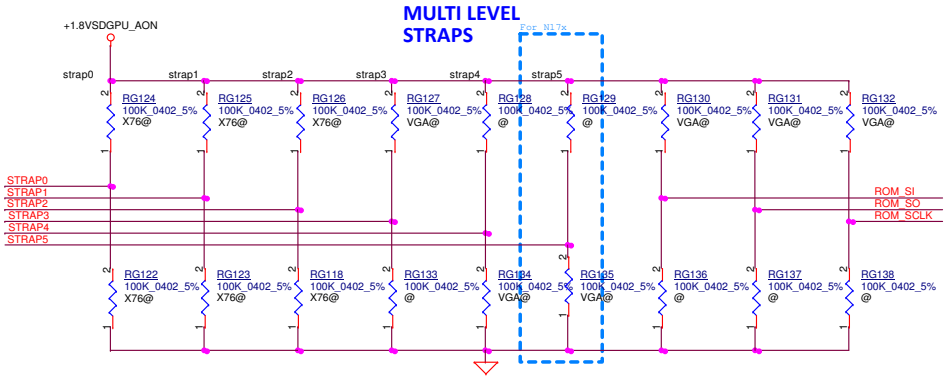
Size: Custom | Document Number: LA-F841P | Rev: 0.1

Date: Monday, August 28, 2017 | Sheet 40 of 65





Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32	1.35V and 1.5V[2]	Samsung	K4G80325FB-HC28	B-die	0x0	7 Gbps	N/A	Full	Production candidate
			Micron	MT51J256M32HF-70:A	A-die	0x1	7 Gbps	N/A	Full	Production candidate
			Hynix	H5GC8H24MJR-R0C	M-die	0x2	7 Gbps	N/A	Full	Post production candidate
4 Gb	128Mx32	1.35V and 1.5V[2]	Samsung	K4G41325FE-HC28	E-die	0x7	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.5V[2]	Hynix	H5GC4H24AJR-R0C	A-die	0x6	7 Gbps	N/A	Full	Production candidate
		1.35V and 1.55V[2]	Micron	EDW4032BABG-70-F	A-die	0x8	7 Gbps	N/A	Full	Post production candidate

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	1	0	0
M	L	H	1	1	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

	SMB_ATL_ADDR	
*	LOW	Single GPU
	High	Dual GPU
	DEVID_SEL	
*	LOW	Orig. Device ID
	High	Support G-Sync GPUID
	VGA_DEVICE	
	LOW	3D Device
*	High	VGA Device
	PCIE_CFG	
*	LOW	Normal signal swing
	High	Reduce the signal amplitude

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Table 5.4 SORx_EXPOSED Strap Enablement for Down Designs

Row Index	Strap Pins see Note			Resulting SORx_EXPOSED Enablements			
	ROM_SO	ROM_SI	ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	disabled	ENABLED	ENABLED
10	H	L	H	ENABLED	disabled	ENABLED	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
	All other Strap Configurations			(Reserved)			

HDMI audio output

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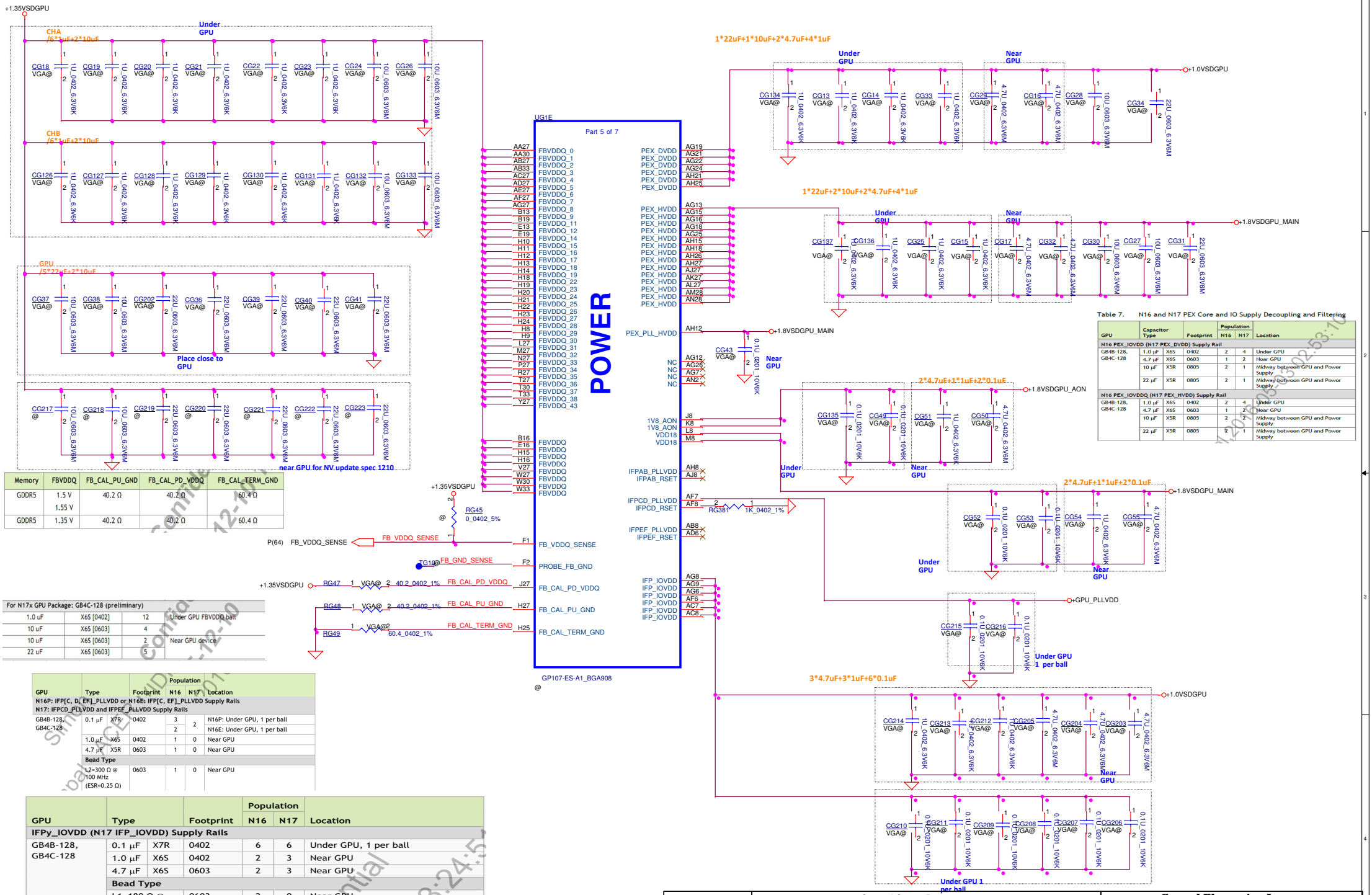
Title: N17P STRAP 3/7
Size: Custom | Document Number: LA-F841P | Rev: 0.1
Date: Monday, August 28, 2017 | Sheet 41 of 65



Memory	FBVDDQ	FB_CAL_PU_GND	FB_CAL_PD_VDDQ	FB_CAL_TERM_GND
GDDR5	1.5 V 1.55 V	40.2 Ω	40.2 Ω	60.4 Ω
GDDR5	1.35 V	40.2 Ω	40.2 Ω	60.4 Ω

For N17x GPU Package: GB4C-128 (preliminary)			
1.0 uF	X6S [0402]	12	Under GPU FBVDDQ ball
10 uF	X6S [0603]	4	
10 uF	X6S [0603]	2	Near GPU device
22 uF	X6S [0603]	5	

GPU	Type		Footprint	Population N16	Population N17	Location
N16P: IFP[C, D, EF]_PLLVDD or N16E: IFP[C, EF]_PLLVDD Supply Rails N17: IFPCD_PLLVDD and IFPEF_PLLVDD Supply Rails						
GB4B-128, GB4C-128	0.1 µF	X7R	0402	3	2	N16P: Under GPU, 1 per ball
				2		N16E: Under GPU, 1 per ball
	1.0 µF	X6S	0402	1	0	Near GPU
	4.7 µF	X5R	0603	1	0	Near GPU
	Bead Type					
	L2=300 Ω @ 100 MHz (ESR=0.25 Ω)		0603	1	0	Near GPU

GPU	Type		Footprint	Population N16	Population N17	Location
IFPy_IOVDD (N17 IFP_IOVDD) Supply Rails						
GB4B-128, GB4C-128	0.1 µF	X7R	0402	6	6	Under GPU, 1 per ball
	1.0 µF	X6S	0402	2	3	Near GPU
	4.7 µF	X6S	0603	2	3	Near GPU
	Bead Type					
	L1=180 Ω @ 100 MHz (ESR=0.2 Ω)		0603	2	0	Near GPU

Table 7. N16 and N17 PEX Core and IO Supply Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population N16	Population N17	Location
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S	0402	2	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X5R	0805	2	1	Midway between GPU and Power Supply
	22 µF	X5R	0805	2	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail					
GB4B-128, GB4C-128	1.0 µF	X6S	0402	2	4	Under GPU
	4.7 µF	X6S	0603	1	2	Near GPU
	10 µF	X5R	0805	2	2	Midway between GPU and Power Supply
	22 µF	X5R	0805	2	1	Midway between GPU and Power Supply

Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

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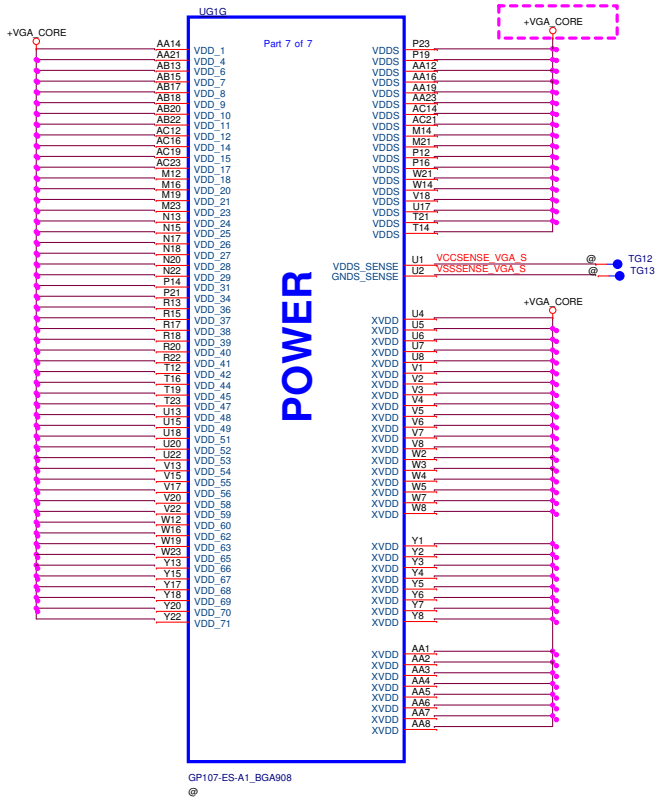
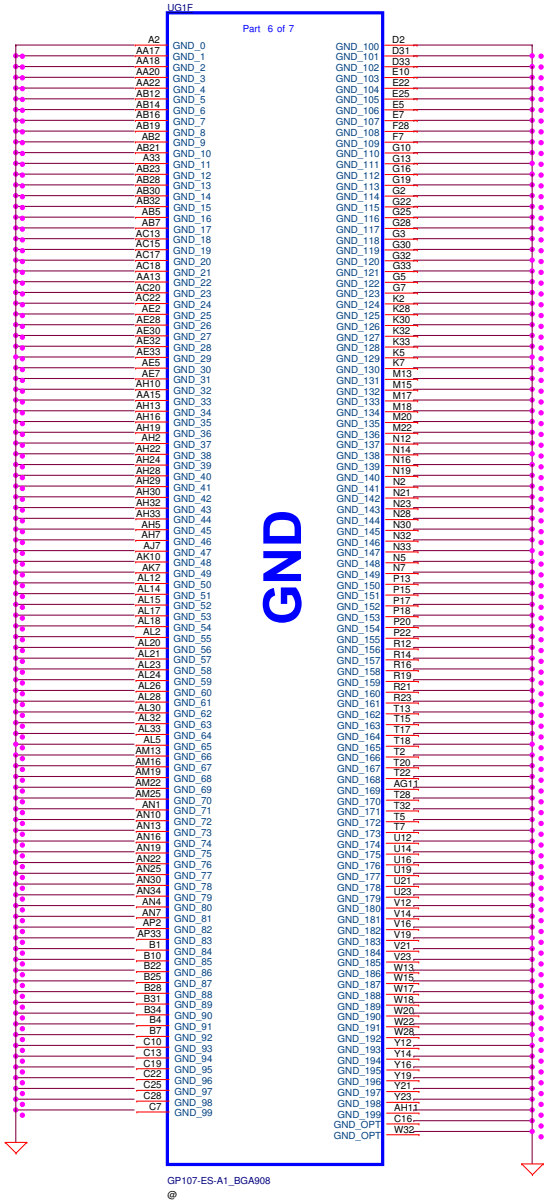
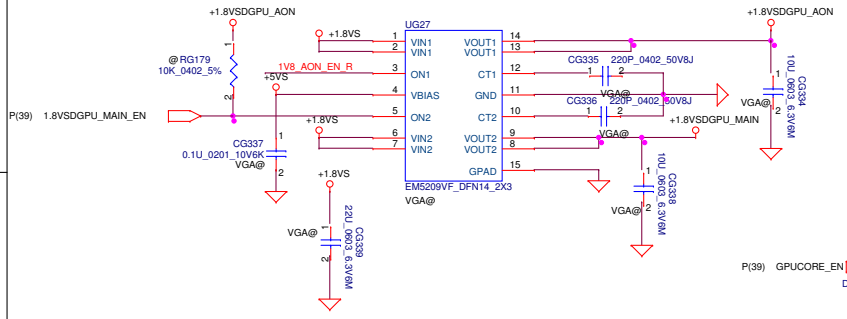
Title	N17P POWER 4/7		
Size: Custom	Document Number: LA-F841P		Rev: 0.1
Date: Monday, August 28, 2017	Sheet 42 of 65		

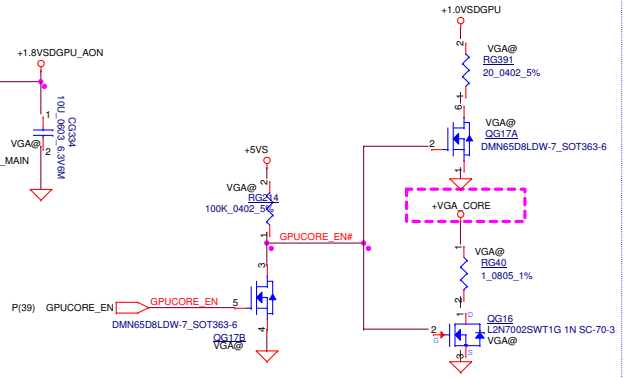
N17P VDDS
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2



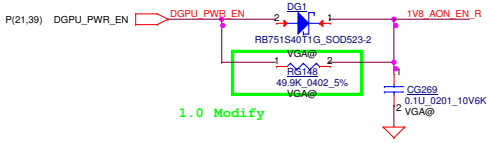


+1.8V_AON/+1.8V_MAIN





For Power down sequence



Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: N17P POWER & GND 5/7

Size: Custom | Document Number: LA-F841P | Rev: 0.1

Date: Monday, August 28, 2017 | Sheet 43 of 65

P(40) FBA_D[63:0]

MF=0

UG4B 2 OF 2

P(40) FBA_CMD6 P(40) FBA_CMD11 P(40) FBA_CMD10 P(40) FBA_CMD7 P(40) FBA_CMD9
P(40) FBA_CMD2 P(40) FBA_CMD4 P(40) FBA_CMD3 P(40) FBA_CMD1
P(40) FBA_CMD8 P(40) FBA_CMD12 P(40) FBA_CMD0 P(40) FBA_CMD15 P(40) FBA_CMD5
P(40) FBA_CLKA0 P(40) FBA_CLKA0# P(40) FBA_CMD14
P(40) FBA_DBI0 P(40) FBA_DBI1 P(40) FBA_DBI2 P(40) FBA_DBI3
P(40) FBA_CMD13
FBA0_ZQ1
P(40) FBA_WCK01 P(40) FBA_WCK01#
P(40) FBA_WCK23 P(40) FBA_WCK23#

A8/A7 A9/A1 A10/A0 A11/A6 A12/RFU#J5/NC#J5
BA0/A2 BA1/A5 BA2/A4 BA3/A3
ABI# RAS# CS# CAS# WE#
CK CK# CKE#
DBI0# DBI1# DBI2# DBI3#
RESET#
SEN ZQ MF
WCK01 WCK01# WCK23 WCK23#
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
EDC0 EDC1 EDC2 EDC3

FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31

FBA_EDC0 P(40) FBA_EDC1 P(40) FBA_EDC2 P(40) FBA_EDC3 P(40)

@5GC2H24BFR-T2C_FBGA170

VGA@ RG57 1K_0402_5% VGA@ RG58 121_0402_1% VGA@ RG59 1K_0402_5%

+1.35VSDGPU

RG50 549_0402_1% VGA@
RG51 931_0402_1% VGA@
FBA0_VREFC
RG52 1.33K_0402_1% VGA@
FBA_VREFC_R
RG53 549_0402_1% VGA@
RG54 931_0402_1% VGA@
FBA1_VREFC
RG56 1.33K_0402_1% VGA@

P(39,45) VRAM_VREF_CTL
MESS138W-G_SOT323-3 QG3 VGA@
1.0 Modify

MF=1

UG5B 2 OF 2

P(40) FBA_CMD26 P(40) FBA_CMD23 P(40) FBA_CMD22 P(40) FBA_CMD27 P(40) FBA_CMD25
P(40) FBA_CMD19 P(40) FBA_CMD17 P(40) FBA_CMD18 P(40) FBA_CMD20
P(40) FBA_CMD24 P(40) FBA_CMD31 P(40) FBA_CMD21 P(40) FBA_CMD28 P(40) FBA_CMD16
P(40) FBA_CLKA1 P(40) FBA_CLKA1# P(40) FBA_CMD30
P(40) FBA_DBI7 P(40) FBA_DBI6 P(40) FBA_DBI5 P(40) FBA_DBI4
P(40) FBA_CMD29
FBA1_ZQ3
P(40) FBA_WCK67 P(40) FBA_WCK67#
P(40) FBA_WCK45 P(40) FBA_WCK45#

A8/A7 A9/A1 A10/A0 A11/A6 A12/RFU#J5/NC#J5
BA0/A2 BA1/A5 BA2/A4 BA3/A3
ABI# RAS# CS# CAS# WE#
CK CK# CKE#
DBI0# DBI1# DBI2# DBI3#
RESET#
SEN ZQ MF
WCK01 WCK01# WCK23 WCK23#
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31
EDC0 EDC1 EDC2 EDC3

FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39

FBA_EDC7 P(40) FBA_EDC6 P(40) FBA_EDC5 P(40) FBA_EDC4 P(40)

@5GC2H24BFR-T2C_FBGA170

+1.35VSDGPU
RG55 VGA@ 1K_0402_5%
VGA@ RG60 1K_0402_5%
VGA@ RG61 121_0402_1%

UG4A 1 OF 2

VDD VSS VDDQ VSSQ VREFC VREFD VPP/NC#A5 VPP/NC#U5

@5GC2H24BFR-T2C_FBGA170

FBA0_VREFC
CG89 VGA@ 820P_0402_50V7K

FBA_CLKA0 FBA_CLKA0#
RG63 40.2_0402_1% VGA@
RG95 40.2_0402_1% VGA@
VGA@ CG190 0.01U_0402_16V7K

FBA_CLKA1 FBA_CLKA1#
RG96 40.2_0402_1% VGA@
RG62 40.2_0402_1% VGA@
VGA@ CG191 0.01U_0402_16V7K
(3GHz and up)

+1.35VSDGPU

CG58 CG59 CG67 CG56 CG57 CG60 CG68 VGA@ 1U_0402_6.3V6K
Close to VRAM
CG141 CG142 CG146 CG73 CG74 CG75 CG76 VGA@ 10U_0402_6.3V6K 10U_0402_6.3V6M
Close to VRAM
CG84 CG85 CG70 CG71 CG72 CG138 CG139 VGA@ 10U_0402_6.3V6K 22U_0603_6.3V6M
Around VRAM
CG161 CG162 CG152 CG163 CG164 CG159 CG165 VGA@ 1U_0402_6.3V6K
x32 only

+1.35VSDGPU

CG61 CG62 CG63 CG64 CG65 CG66 CG69 VGA@ 1U_0402_6.3V6K
Close to VRAM
CG77 CG78 CG79 CG80 CG81 CG82 CG83 VGA@ 10U_0402_6.3V6K 10U_0402_6.3V6M
Close to VRAM
CG86 CG87 CG143 CG144 CG145 CG147 CG148 VGA@ 10U_0402_6.3V6K 22U_0603_6.3V6M
Around VRAM
CG166 CG168 CG167 CG170 CG169 CG172 CG171 CG173 VGA@ 1U_0402_6.3V6K
x32 only

+1.35VSDGPU

UG5A 1 OF 2

VDD VSS VDDQ VSSQ VREFC VREFD VPP/NC#A5 VPP/NC#U5

@5GC2H24BFR-T2C_FBGA170

FBA1_VREFC
CG88 VGA@ 820P_0402_50V7K

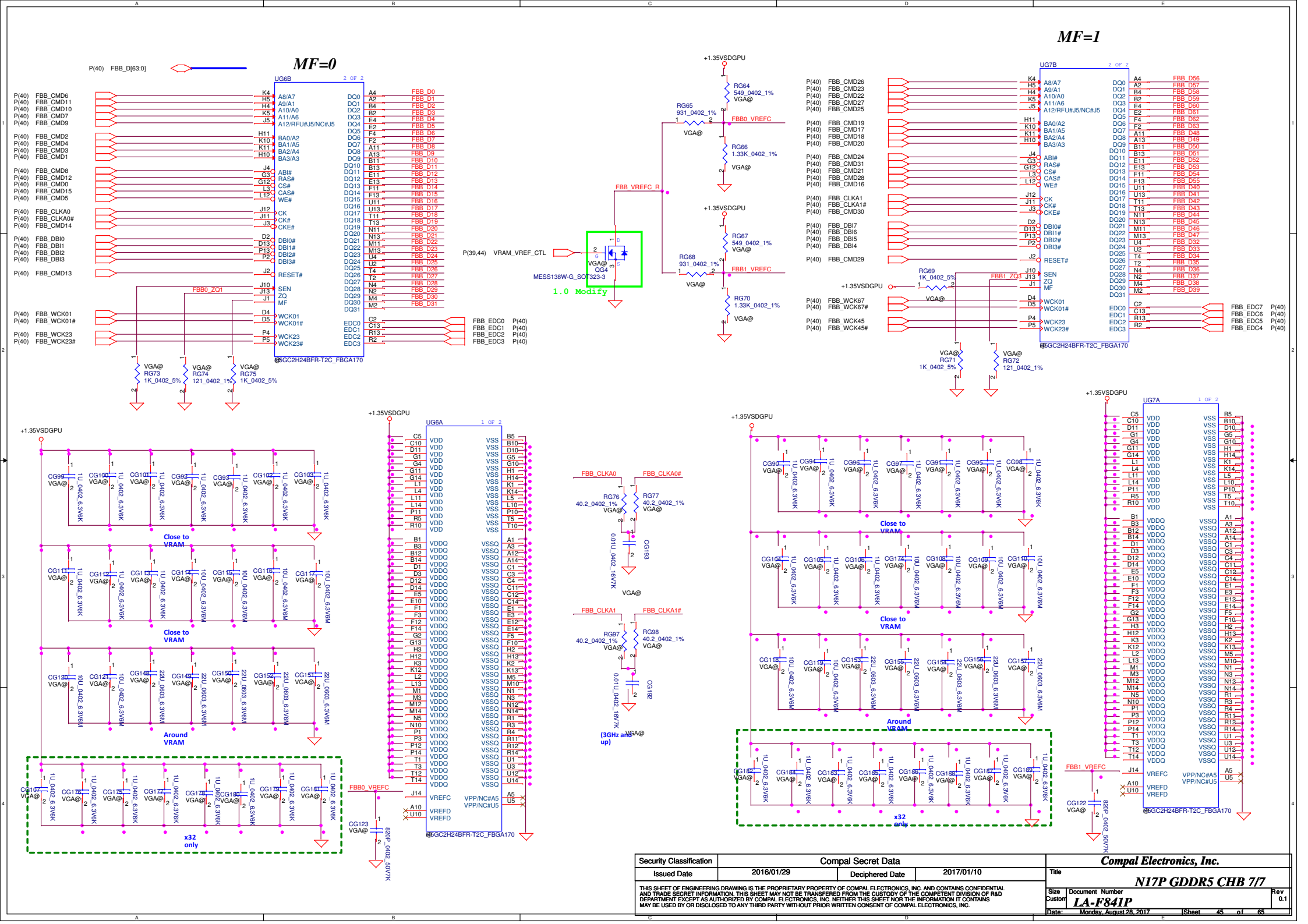
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

Compal Electronics, Inc.

Title: N17P GDDR5 CHA 6/7

Size: Custom | Document Number: LA-F841P | Rev: 0.1

Date: Monday, August 28, 2017 | Sheet 44 of 65



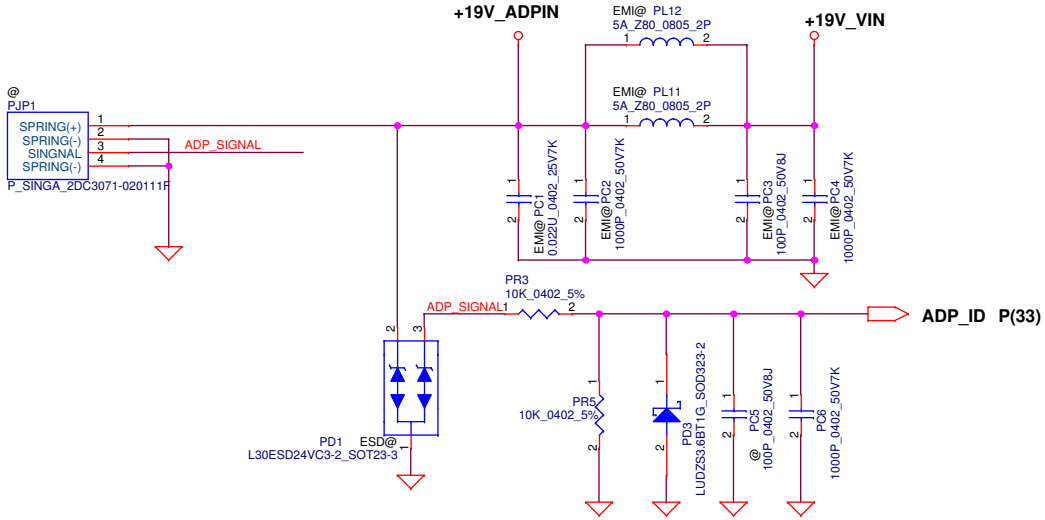
Security Classification	Compal Secret Data		
Issued Date	2016/01/29	Deciphered Date	2017/01/10

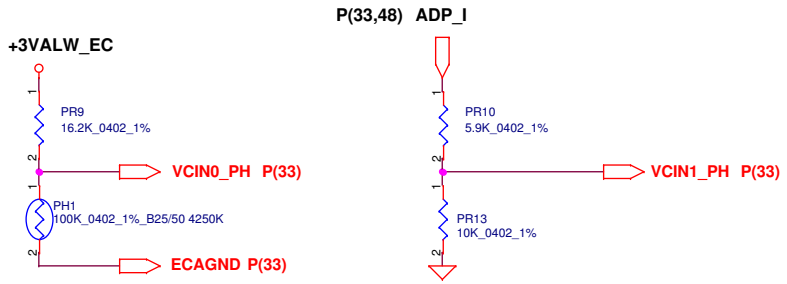
Compal Electronics, Inc.

Title: N17P GDDR5 CHB 7/7

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 45 of 65





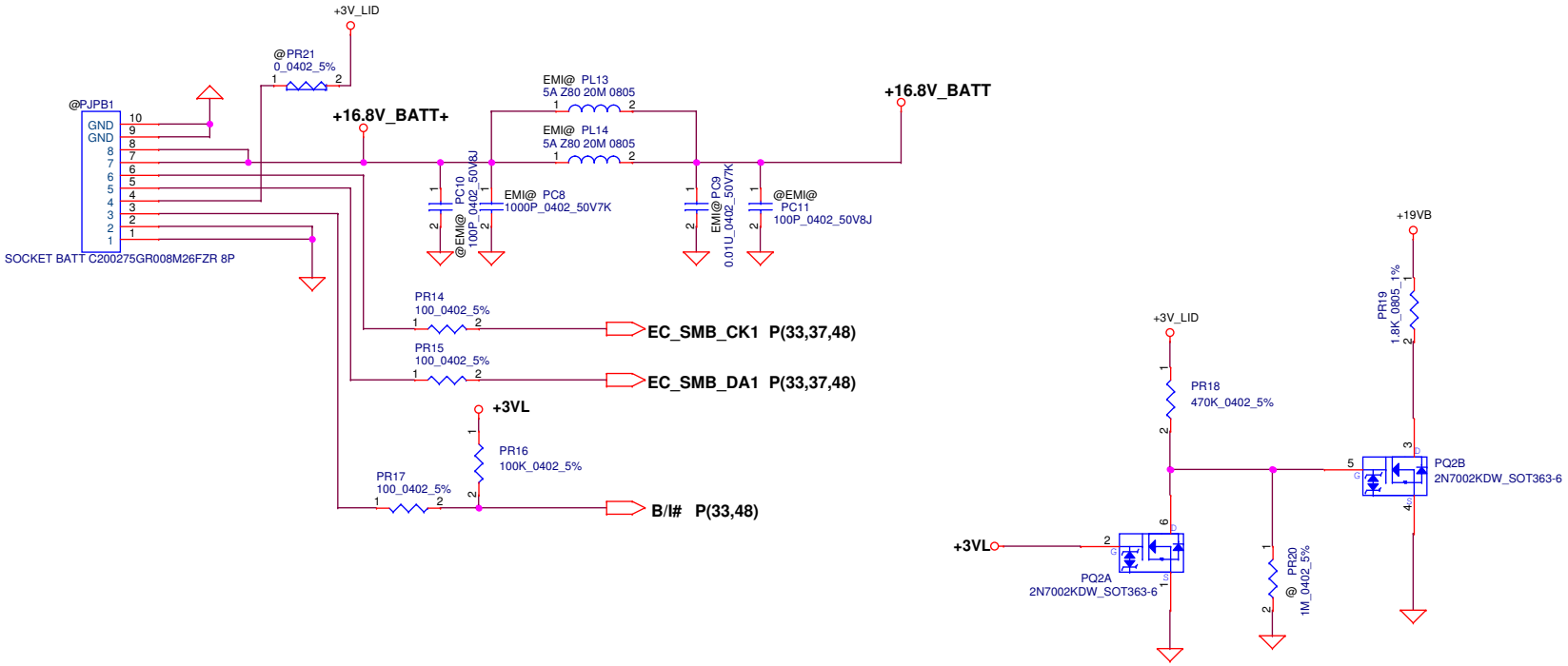
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: *DC Conn*

Size | Document Number: **LA-F841P** | Rev: 0.2

Date: Monday, August 28, 2017 | Sheet 46 of 65

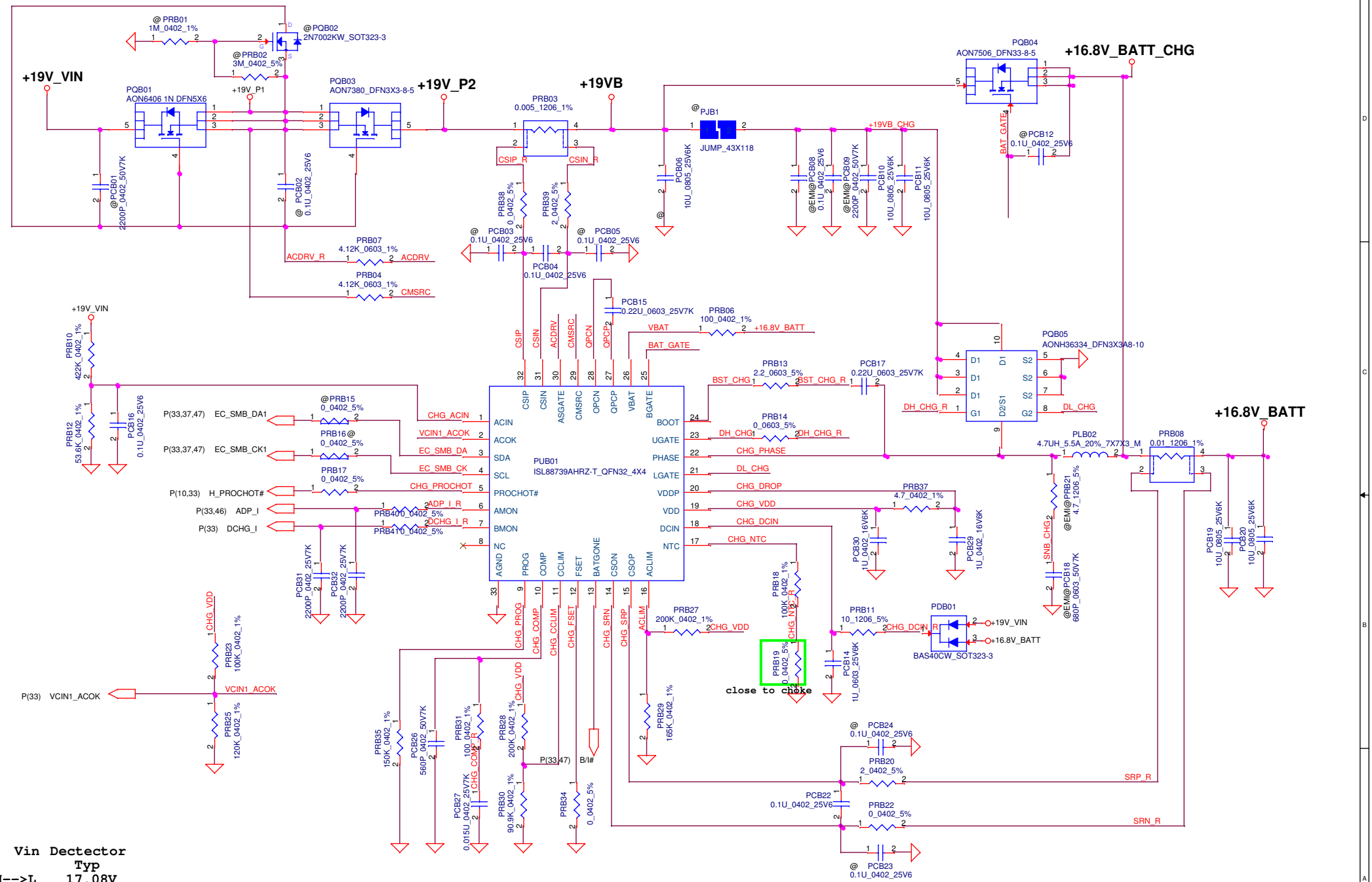


Compal Electronics, Inc.

Title: ***BATT Conn***

Size | Document Number: **LA-F841P** | Rev: 0.2

Date: Monday, August 28, 2017 | Sheet 47 of 65



Vin Dectector

	Typ
H-->L	17.08V
L-->H	17.81V
OVP	23V

Fsw : 620kHz
ILIM : 3.62A

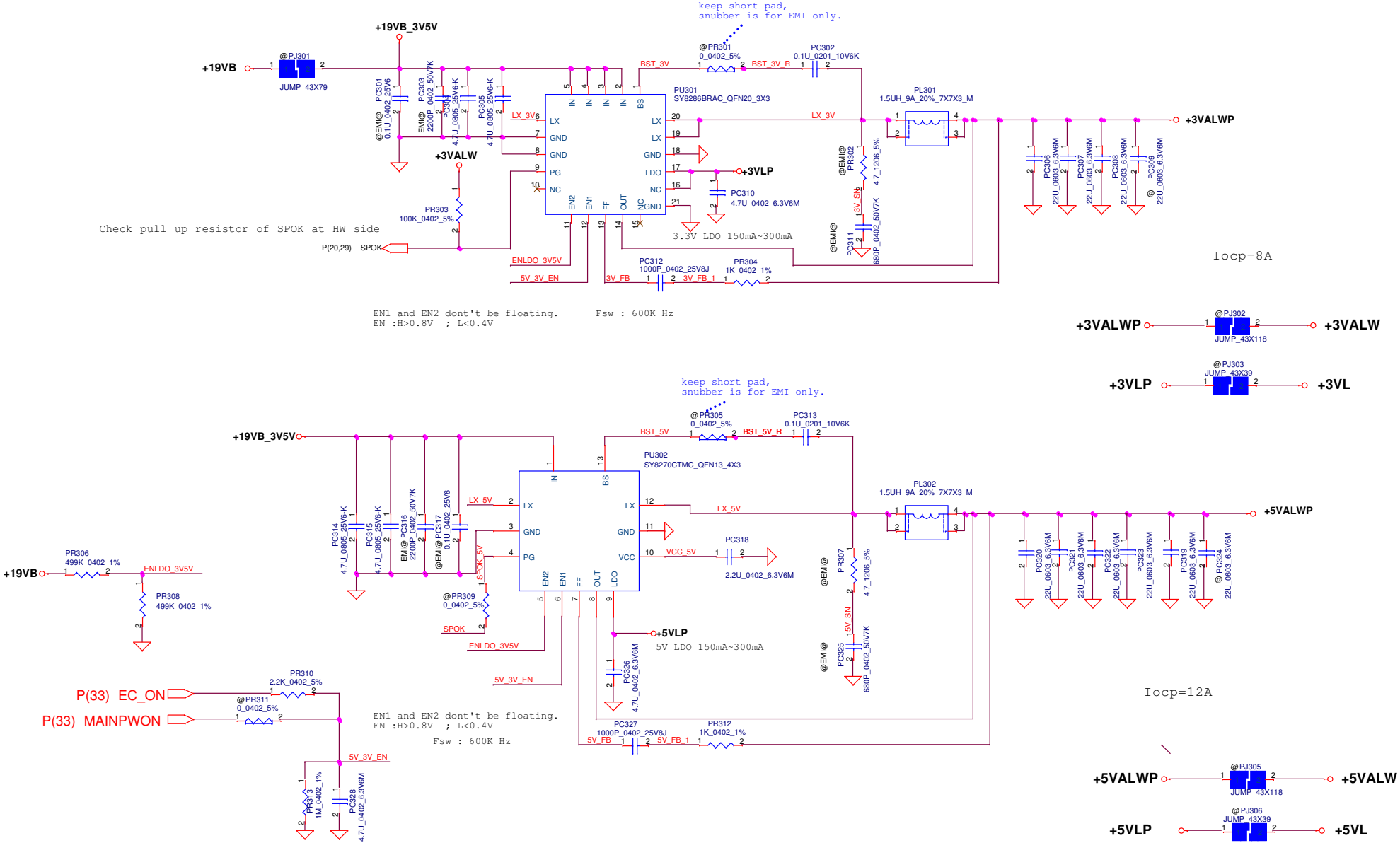
Security Classification	Compal Secret Data		
Issued Date	2014/10/09	Deciphered Date	2015/12/31

Compal Electronics, Inc.

Title: **Charger**

Size	Document Number	Rev
Custom	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 48 of 65



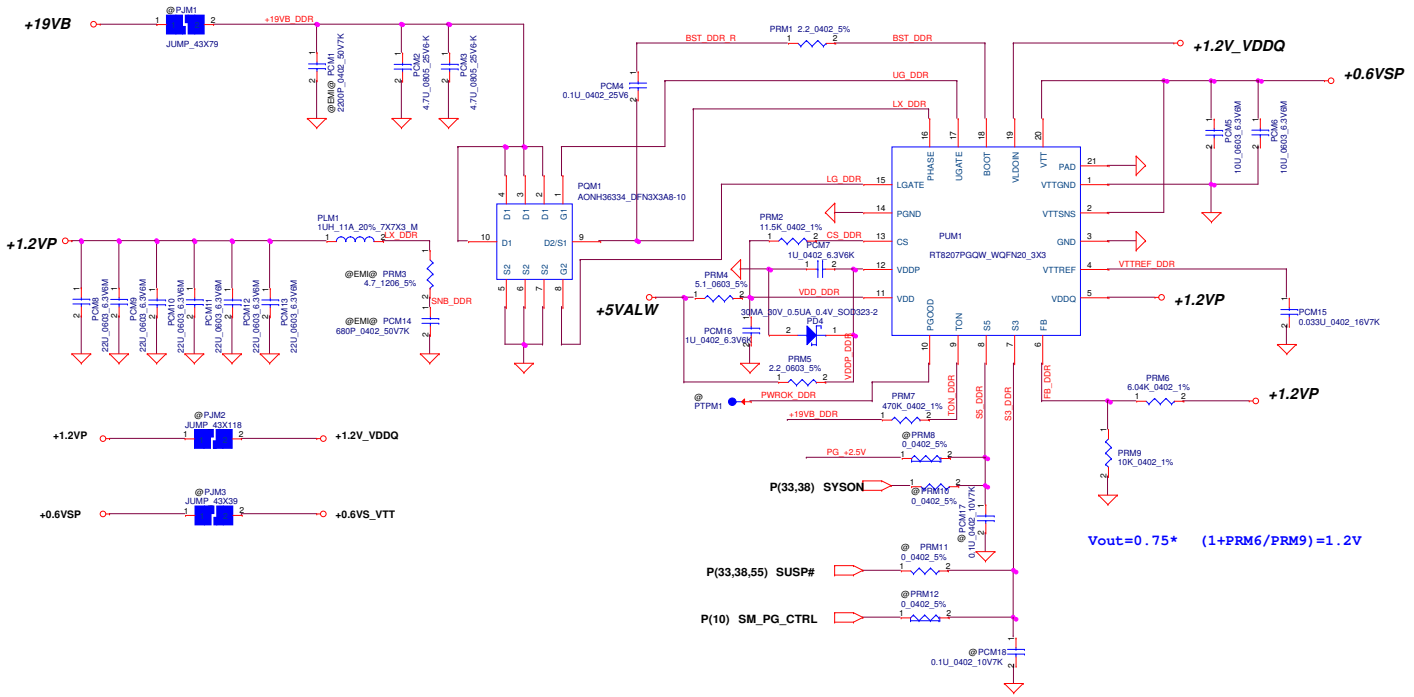
Security Classification	Compal Secret Data		
Issued Date	2011/06/15	Deciphered Date	2012/07/11

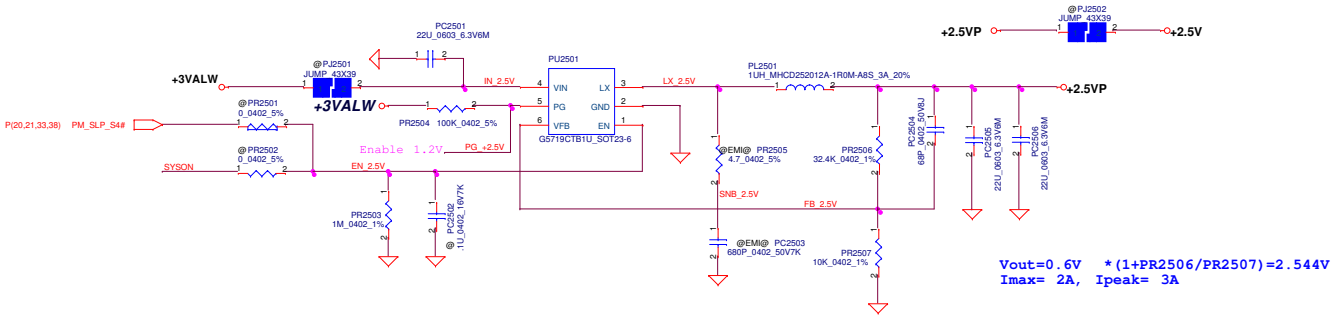
Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size	Document Number	Rev
Custom		0.1

Date: Monday, August 28, 2017 Sheet 49 of 65





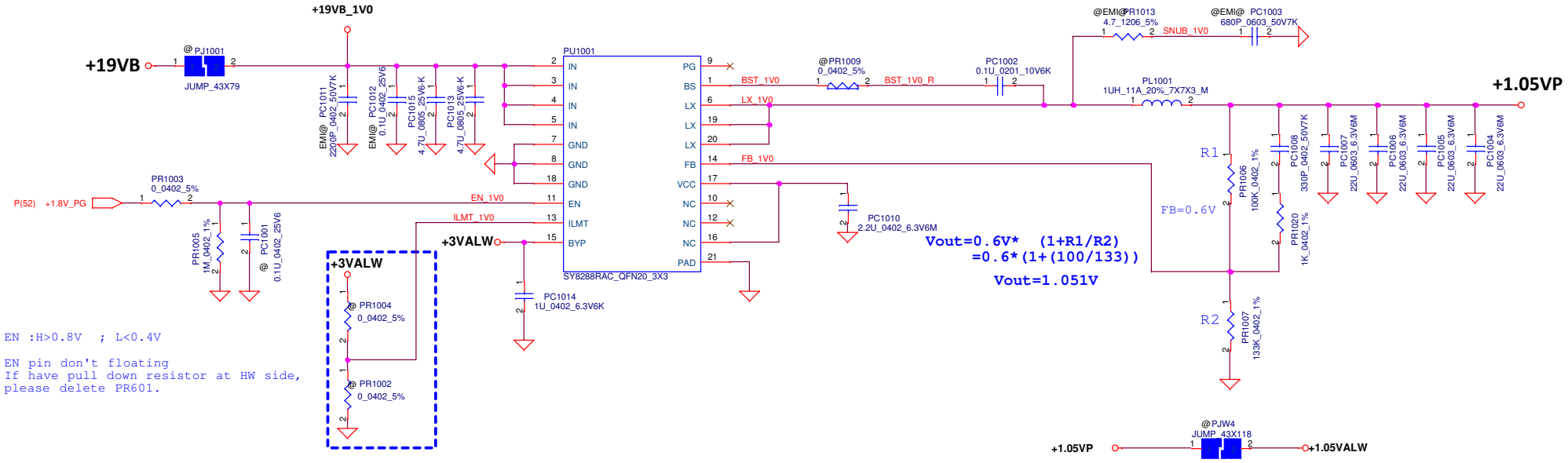
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: 1.2VP/0.6VSP/2.5V

Size: Custom | Document Number | Rev: 0.2

Date: Monday, August 28, 2017 | Sheet 50 of 65

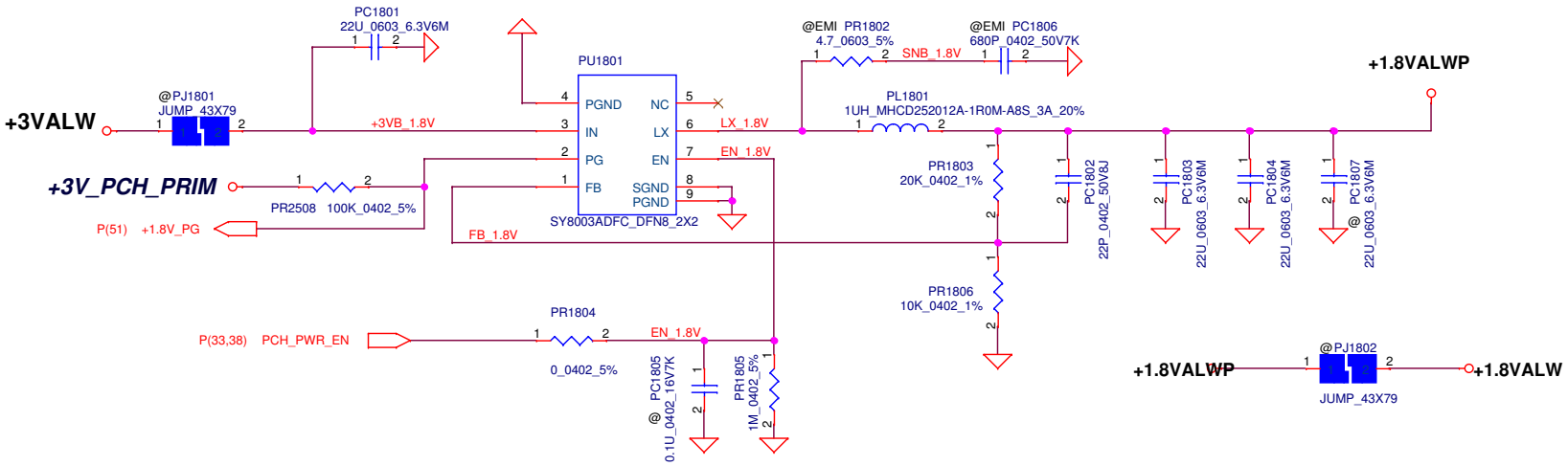


Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Title: **1.0V_PRIM**

Size	Document Number	Rev
Custom		0.2

Date: Monday, August 28, 2017 | Sheet 51 of 65



Vout=0.6V*(1+PR1803/PR1806)=1.8V
Imax= 2A, Ipeak= 3A

3A continuous
3.5A current limit

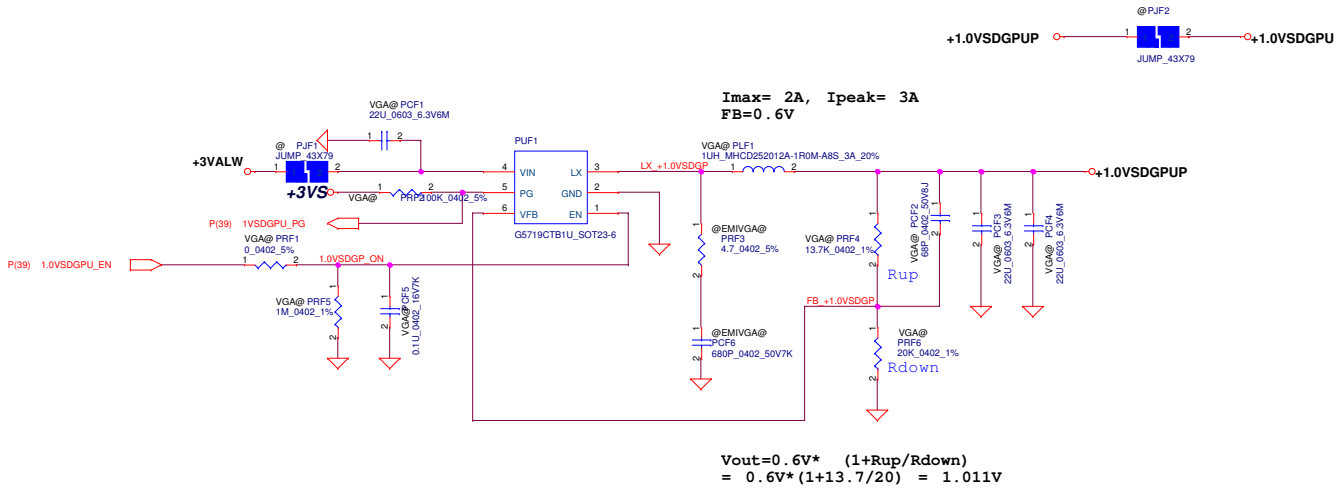
Security Classification	Compal Secret Data		
Issued Date	2016/09/01	Deciphered Date	2019/09/01

Compal Electronics, Inc.

Title: *1.8V_PRIM*

Size	Document Number	Rev
B	LA-F841P	0.2

Date: | Sheet 52 of 65



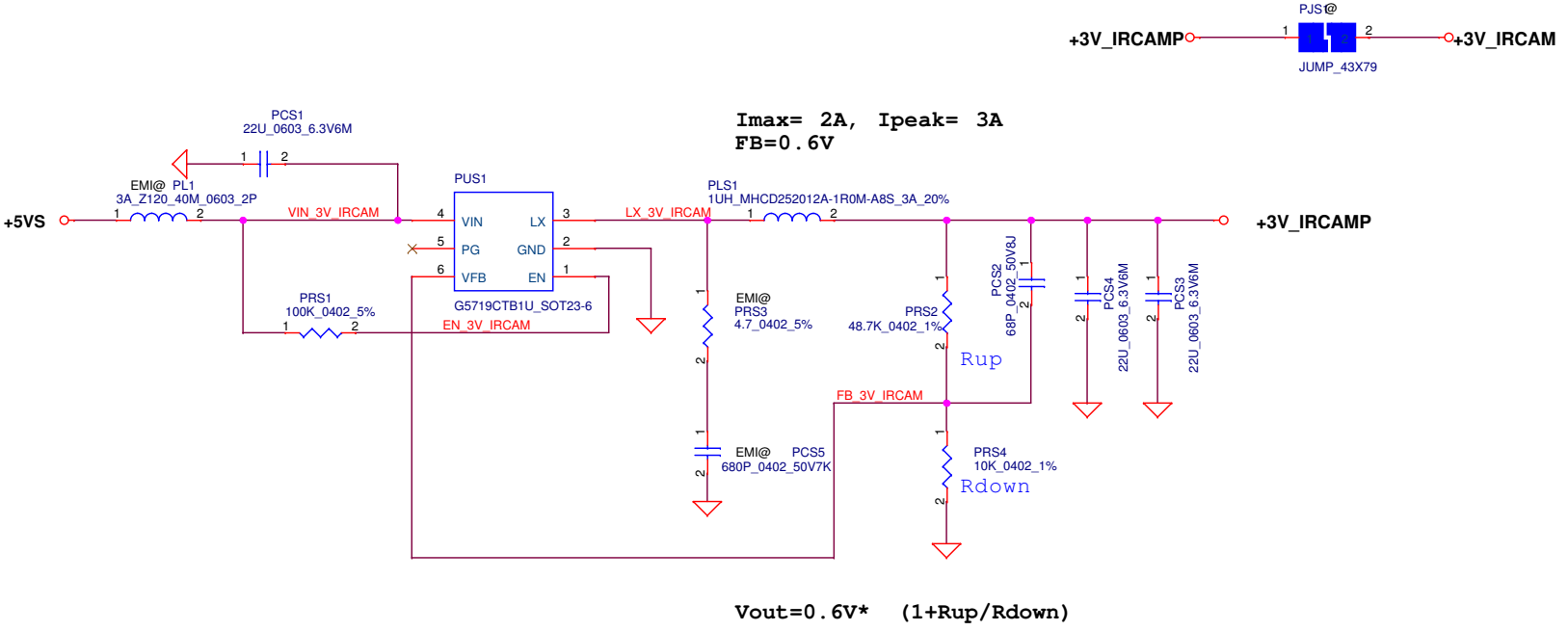
Security Classification	Compal Secret Data		
Issued Date	2011/06/13	Deciphered Date	2012/06/13

Compal Electronics, Inc.

Title: SY8032

Size	Document Number	Rev
C		1.0

Date: Monday, August 28, 2017 | Sheet 53 of 65



Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

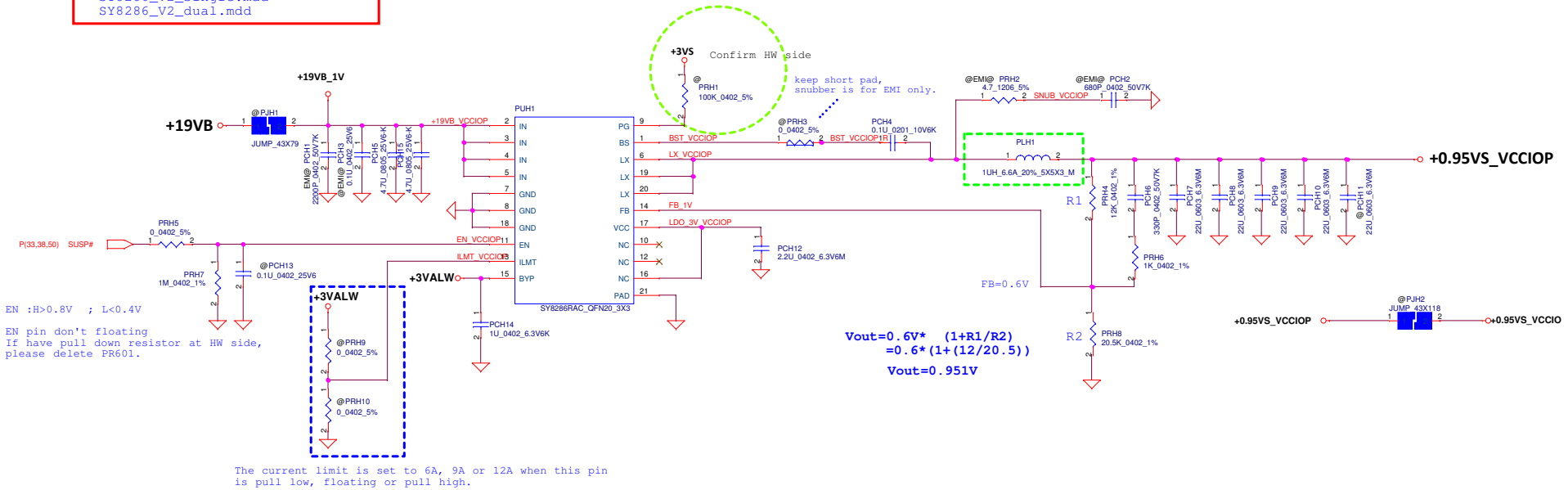
Title: **+3V_IRCAM**

Size	Document Number	Rev
	LA-F841P	0.1

Date: Monday, August 28, 2017 Sheet 54 of 65

Module model information

SY8286_V2_single.mdd
SY8286_V2_dual.mdd



EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

The current limit is set to 6A, 9A or 12A when this pin is pull low, floating or pull high.

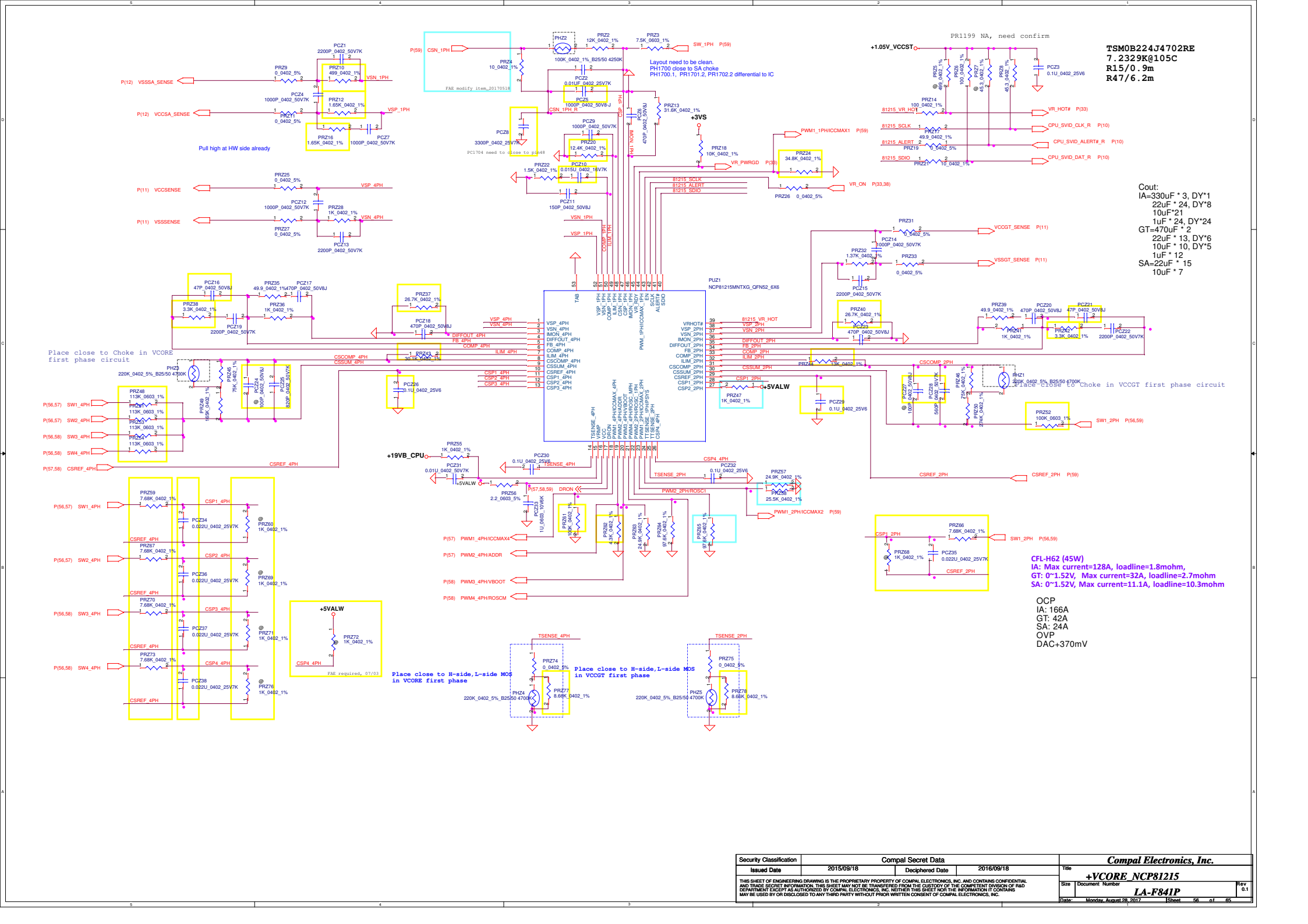
Security Classification	Compal Secret Data		
Issued Date	2014/11/10	Deciphered Date	2016/11/10

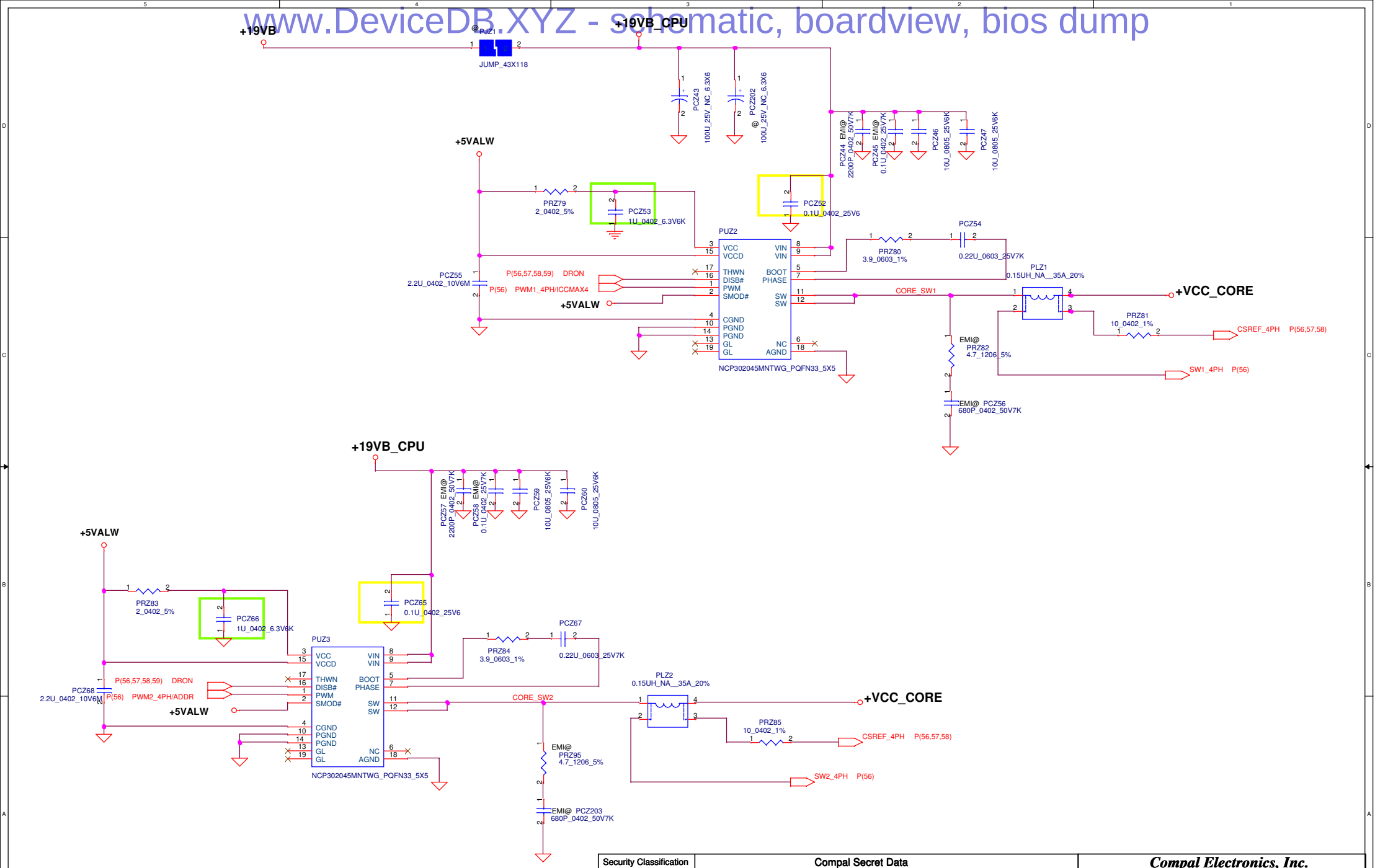
Compal Electronics, Inc.

Title: SY8286

Size	Document Number	Rev
C		0.1

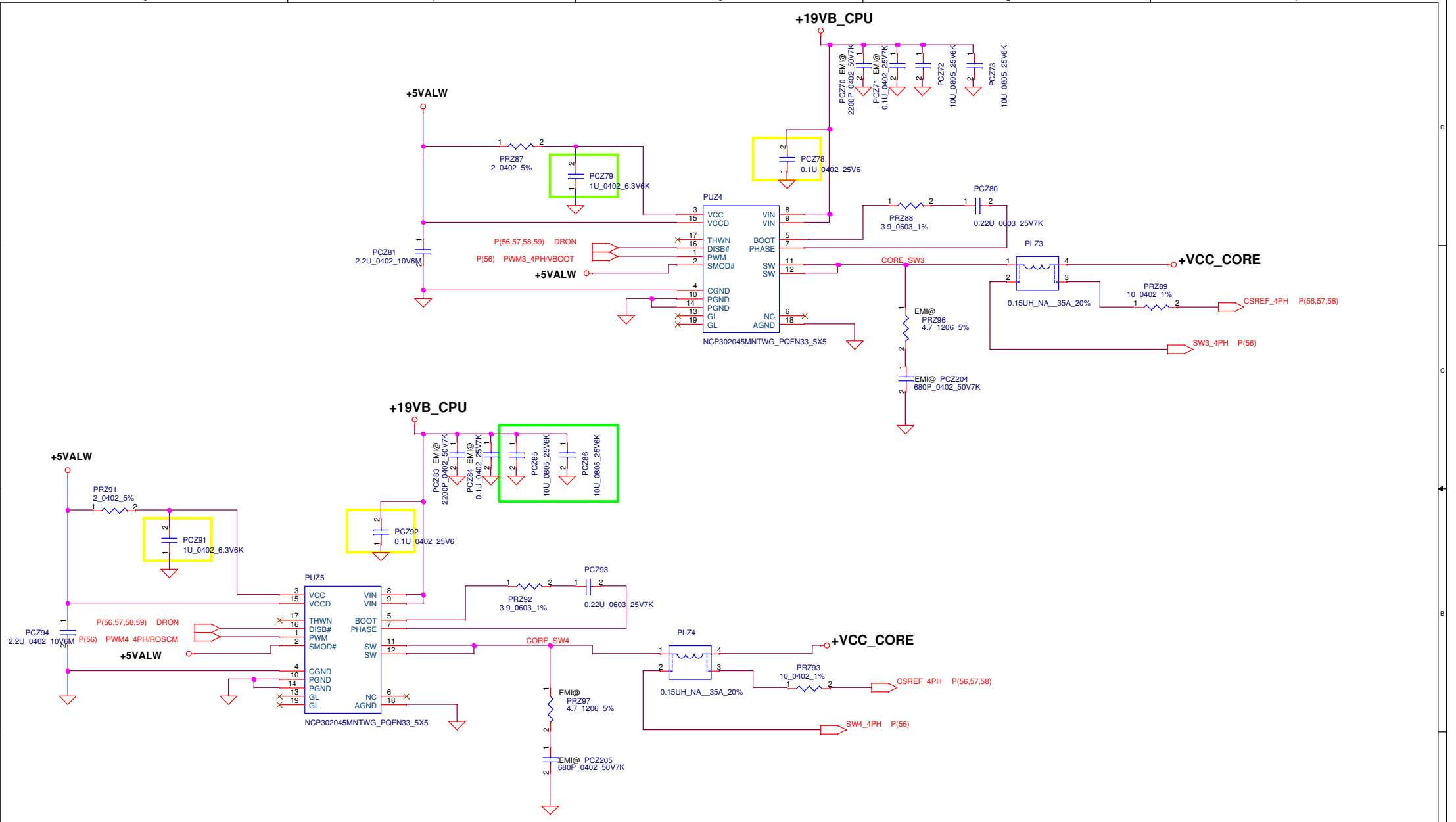
Date: Monday, August 28, 2017 Sheet 55 of 65


PR1199 NA, need confirm
TSM0B224J4702RE
7.2329K@105C
R15/0.9m
R47/6.2m
Cout:
IA=330uF * 3, DY*1
22uF * 24, DY*8
10uF*21
1uF * 24, DY*24
GT=470uF * 2
22uF * 13, DY*6
10uF * 10, DY*5
1uF * 12
SA=22uF * 15
10uF * 7
Layout need to be clean.
PH1700 close to SA choke
PH1700.1, PR1701.2, PR1702.2 differential to IC
Pull high at HW side already
Place close to Choke in VCORE first phase circuit
Place close to Choke in VCCGT first phase circuit
Place close to H-side,L-side MOS in VCORE first phase
Place close to H-side,L-side MOS in VCCGT first phase
PUZ1
NCP81215MNTXG_QFN52_6X6
CFL-H62 (45W)
IA: Max current=128A, loadline=1.8mohm,
GT: 0~1.52V, Max current=32A, loadline=2.7mohm
SA: 0~1.52V, Max current=11.1A, loadline=10.3mohm
OCP
IA: 166A
GT: 42A
SA: 24A
OVP
DAC+370mV
Security Classification
Compal Secret Data
Issued Date
2015/09/18
Deciphered Date
2016/09/18
Compal Electronics, Inc.
+VCORE_NCP81215
LA-F841P
Rev 0.1
Monday, August 28, 2017
Sheet 56 of 85



Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.			
Title	+VCC_CORE_Phase1&2		
Size	Document Number		Rev
	LA-F841P		0.1
Date: Monday, August 28, 2017	Sheet 57 of 65		



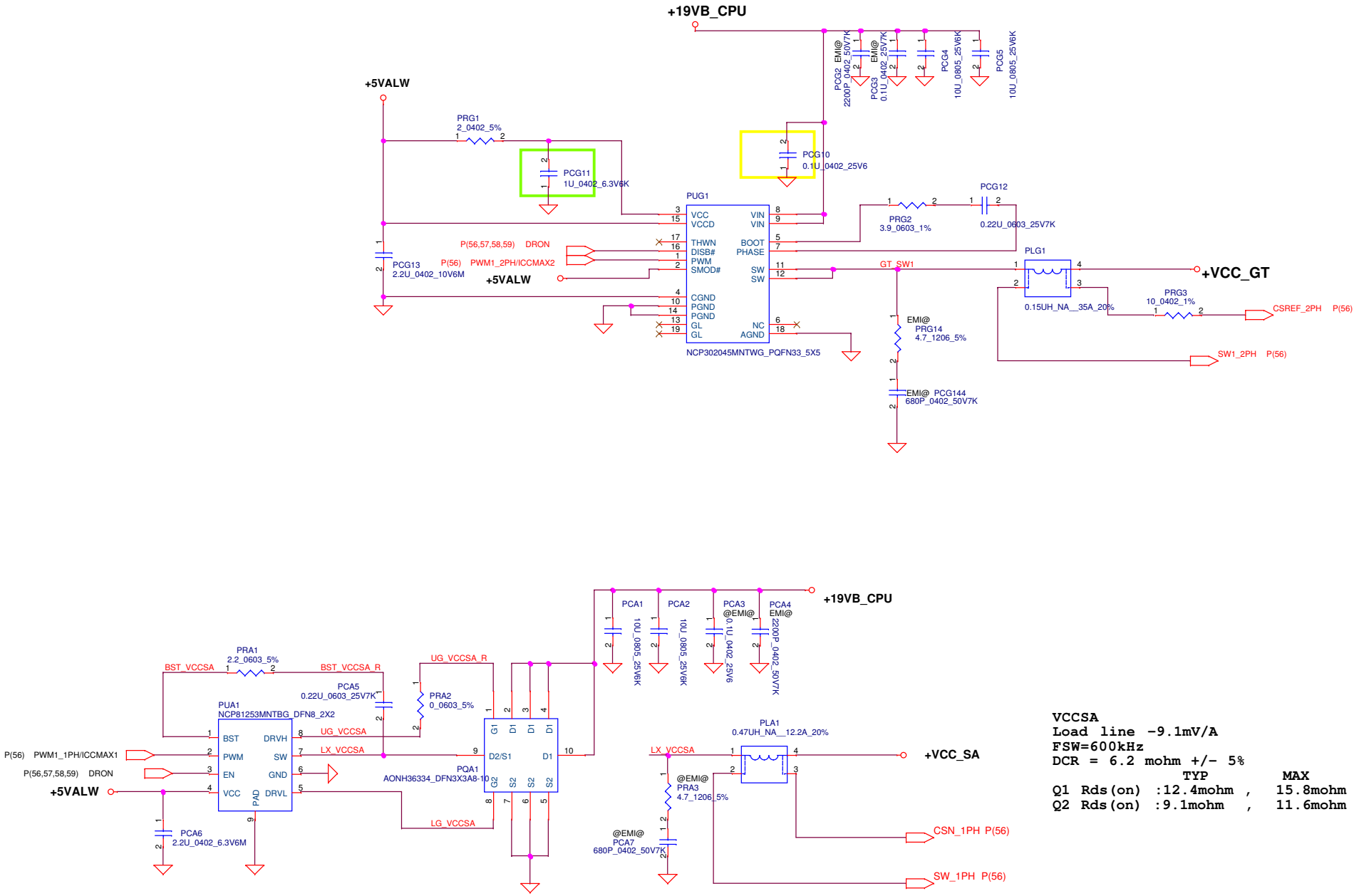
Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: +VCC_CORE_Phase3&4

Size	Document Number	Rev
	LA-F841P	0.1

Date: Monday, August 28, 2017 | Sheet 58 of 65



VCCSA
Load line -9.1mV/A
FSW=600kHz
DCR = 6.2 mohm +/- 5%

	TYP	MAX
Q1 Rds(on)	:12.4mohm ,	15.8mohm
Q2 Rds(on)	:9.1mohm ,	11.6mohm

Must review KBL SA rating.

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

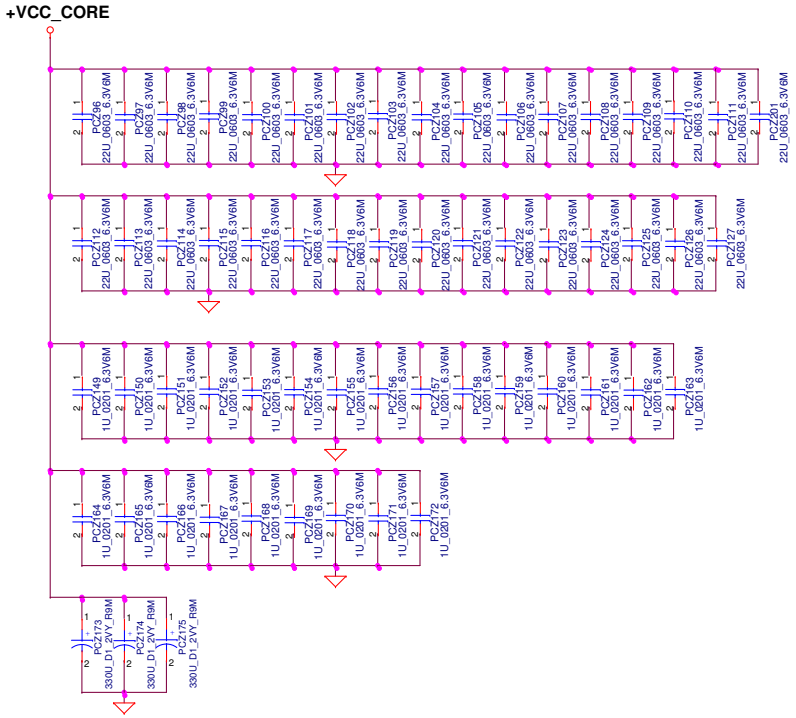
Compal Electronics, Inc.

Title: +VCC_GT/+VCC_SA

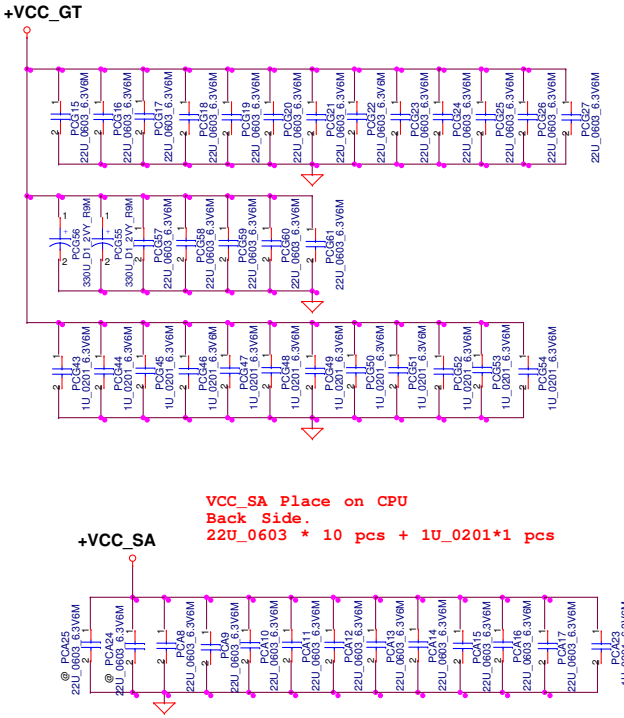
Size | Document Number: LA-F841P | Rev: 0.1

Date: Monday, August 28, 2017 | Sheet 59 of 65

VCC_CORE Place on CPU
Back Side.
330uF_R9 *3 pcs +22U_0603 * 33 pcs + 1U_0201*24 pcs



VCC_GT Place on CPU
Back Side.
330uF_R9 *2 pcs + 22U_0603 * 18 pcs +1U_0201*12 pcs



VCC_SA Place on CPU
Back Side.
22U_0603 * 10 pcs + 1U_0201*1 pcs

Security Classification	Compal Secret Data		
Issued Date	2015/09/18	Deciphered Date	2016/09/18

Compal Electronics, Inc.

Title: CPU BACK SIDE MLCC

Size | Document Number: LA-F841P | Rev: 0.1

Date: Monday, August 28, 2017 | Sheet 60 of 65

Vboot=Vvref*Rref2/(Rref1+Rref2+Rboot)
Rt=Rrefadj // (Rboot+Rref2)
Vmin= Vvref*[Rref2/(Rref2+Rboot)]*[Rt/(Rref1+Rt)]
Vmax=Vvref*Rref2/[(Rref1//Rrefadj)+Rboot+Rref2]
Vout=Vmin+N*Vstep
Vstep=(Vmax-Vmin)/Nmax

Module model information:
RT8813D_V2A for IC module
RT8813D_V2B for SW module

R1, R2, R3, R4, R5, C are based on VGA type to set.

Operation phase	PSI
4 phase with DEM	Voltage setting to 1.2V
1 phase with CCM	Voltage setting to 0.8V
Active phase with CCM	Voltage setting to 5.5V

PWM VID and Output voltage control
1.Boot mode
2.Standby mode (don't support)
3.Normal mode

PWM VID Pull high on HW side

Switching frequency setting:
Fsw=(Vin-0.5)/(2*Vin*Rton*3.2p)=352Khz

Current Limit threshold setting
Rocset= (Ivalley * Rds(on) +40mv) / Iocset

High: >1.6V
Low: <0.8V

Reserve Location

+VGA_CORE
EDP-Continuous 59A/N17P-G0, 50A/N17P-G1
EDP-Peak 124A/N17P-G0, 90A/N17P-G1
OCP > 130A
Please base on GPU spec to calculate.

Please base on GPU spec to modify output cap.

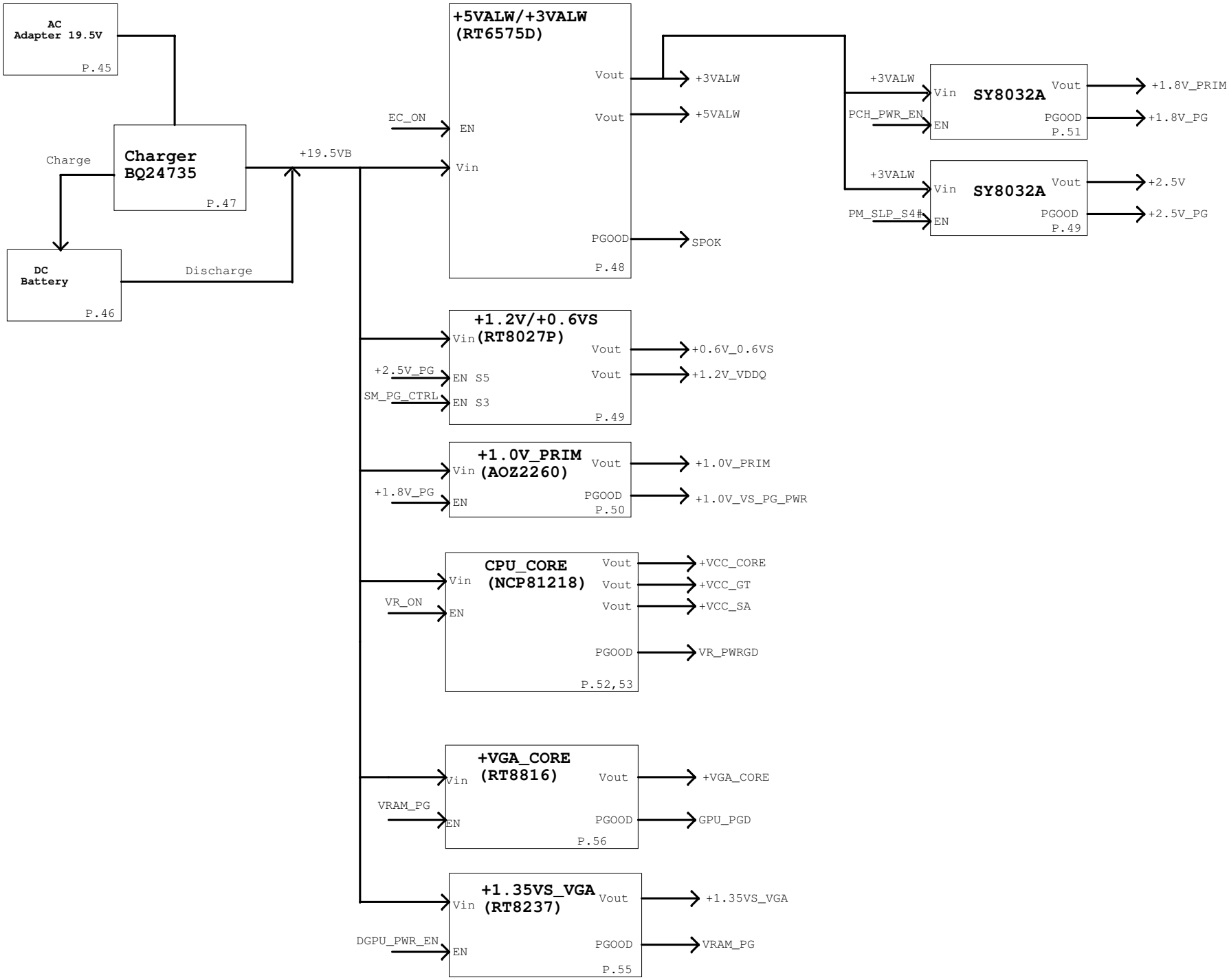
Security Classification	Compal Secret Data		
Issued Date	2008/09/15	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: **RT8813D**

Size | Document Number | Rev 0.1

Date: Monday, August 28, 2017 | Sheet 61 of 65



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Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Power Block Diagram

LA-F841P 0.1

Monday, August 13, 2018 Sheet 62 of 65


```
+VGA_CORE
330uF  X  4
4.7uF_0603X  18
22uF_0603  X  9
10uF_0603  X  16
1uF_0402X  13

Please base on GPU spec to modify output cap.
```

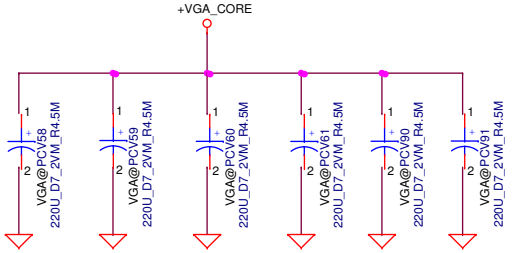

Table 7.17 GB4C-128 Package: Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage; Current	Filtering under GPU	Filtering Near GPU
NVVDD		Varies	8 X 1uF (0402 X6S) 16 X 4.7uF (0603 X6S)	9 X 10uF (0603 X6S) 7 X 22uF (0805 X6S) 1 X 330uF (Poscap)
NVVDDS		Varies	5 X 1uF (0402 X6S) 5 X 10uF (0603 X6S)	2 X 10uF (0603 X6S) 3 X 22uF (0805 X6S)

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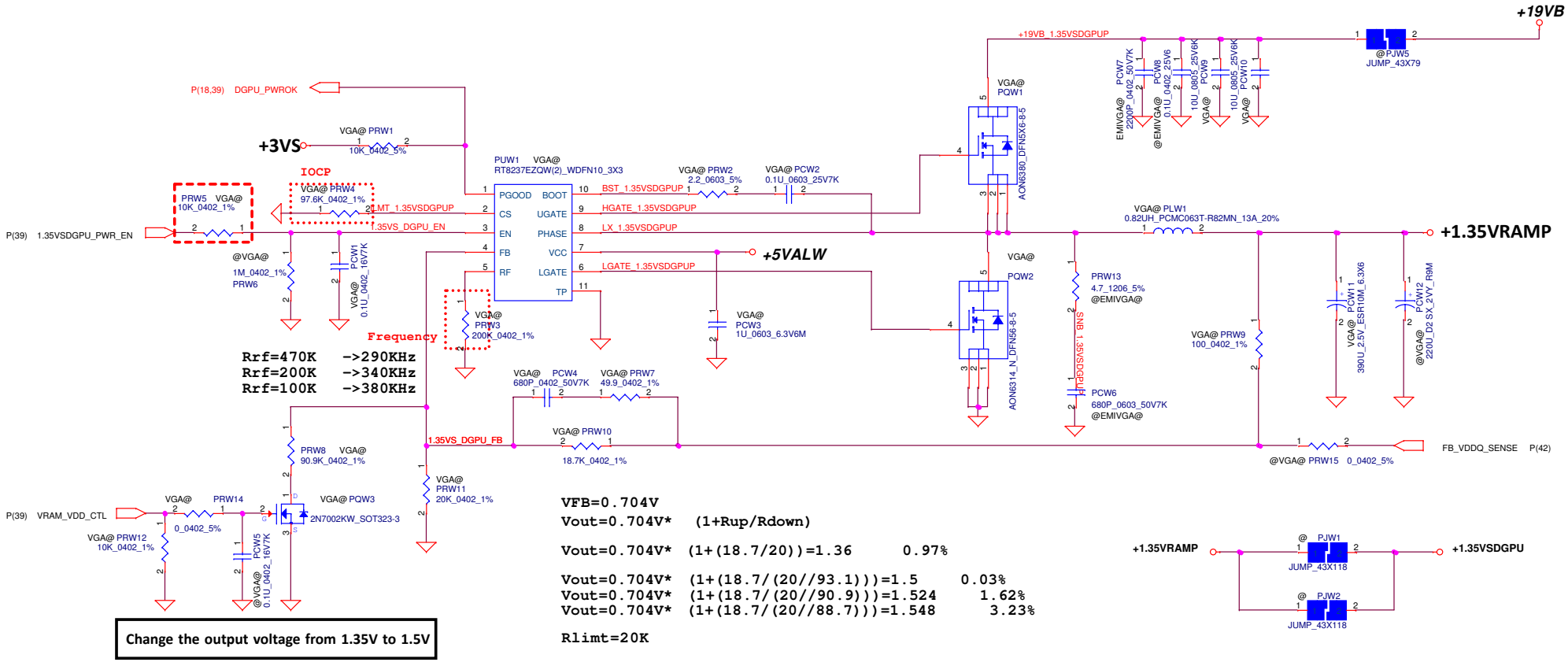
Title: VGA DECOUPLING

Size | Document Number: LA-F841P | Rev: 0.1

Date: Monday, August 28, 2017 | Sheet 63 of 65



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Issued Date	2016/09/01	Deciphered Date	2019/09/01

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Title	*1.35VRAMP*	
Size	Document Number: LA-F841P	Rev: 0.1
Date: Monday, August 28, 2017	Sheet 64 of 65	

Version change list (P.I.R. List)

1					
2					
3					
4					
5					
6					

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Title: PIR

Size	Document Number	Rev
C	LA-F841P	0.2

Date: Monday, August 28, 2017 | Sheet 65 of 65